1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB,X1036

LAST_MODIFICATION=Thu Jul 12 17:54:35 2018

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0013100592	ENGINEERING RELEASED	2018-07-12

Table of Contents

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Thu Jul 12 17:54:35 2018

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

DRAWING TITLE: SCHEM,MLB,X1036

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 1 OF 142
SHEET: 1 OF 115

Schematic / PCB /MCO #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-02424	1	SCHEM,MLB,X1036	SCH	CRITICAL	
820-00939	1	PCBF,MLB,X1036	PCB	CRITICAL	
056-04386	1	MCO,MLB,X1036	MCO	CRITICAL	

Module Parts

TBT X,T

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00356	2	IC,TBT,TITAN RIDGE,QTZZ,ES2,B0,CSP337	U2800,UB000	CRITICAL	TBT_TR:B0
338S00408	2	IC,TBT,TITAN RIDGE,QUJK,QS,C1,CSP337	U2800,UB000	CRITICAL	TBT_TR:C1_QS
338S00441	2	IC,TBT,TITAN RIDGE,QUJK,PRQ,C1,CSP337	U2800,UB000	CRITICAL	TBT_TR:C1

ACE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S01442	4	IC,CD3215,ACE,C0,USB PWR SW,BLNK,BGA96	U3100,U3200,UB300,UB400	CRITICAL	ACE:C0_nFBGA
353S01478	4	IC,CD3215,ACE2,USB PWR SW,BLNK,BGA123	U3100,U3200,UB300,UB400	CRITICAL	ACE2:A0
353S00961	4	IC,CD3215,ACE,C0,USB PWR SW,BLNK,jrBGA96	U3100,U3200,UB300,UB400	CRITICAL	ACE:C0

SOC PMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00342	1	IC,PMU,CALPE_L,D2249A0,OTP-AC,CSP324,0.5	U7800	CRITICAL	PMU:A0_C

SOC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00386	1	POP.SOC,GIBRALTAR+1G 21NM,M,Dev,CSP1122	U3900	CRITICAL	SOC:1G_DEV
339S00388	1	POP.SOC,GIBRALTAR+1G 21NM,M,Dev,CSP1122	U3900	CRITICAL	SOC:2G_DEV

10Gb ETHERNET CONTROLLER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00332	1	IC,ENET CONTROLLER,AQC107,B1,BGA224	U9600	CRITICAL	10G_ENET:B1

1Gb ETHERNET CONTROLLER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0616	1	IC,ENET CONTROLLER,CAESAR,A0	U9300	CRITICAL	1G_ENET:A0

WiFi/BT CONTROLLER (Should have alternatives)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00458	1	IC,MODULE,HARPOON,ES7.7,LGA385	U3730	CRITICAL	WIFI:ES7

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00428	339S00458		ALL	IC,MODULE,WCF2/BT,HARPOON,US1,ES7.5,LGA385

HDMI CONTROLLER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00347	1	PCON,MADEA,A4	UA800	CRITICAL	HDMI:A4

PoWER CONTROLLER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00928	1	IC,ISL95828A,IMVP0 CPU REG,QFN48,6x6mm	U7100	CRITICAL	

CPU

4C CPU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00457	1	CPU,CFL-H	U0500	CRITICAL	CPU:PES
337S00555	1	CPU,CFL-H,QQ5N,EQS,2.8GHz	U0500	CRITICAL	CPU_EQS:2.8G
337S00554	1	CPU,CFL-H,QQ5K,EQS,3.0GHz	U0500	CRITICAL	CPU_EQS:3.0G
337S00553	1	CPU,CFL-H,QQ5C,EQS,3.2GHz	U0500	CRITICAL	CPU_EQS:3.2G
998-12472	1	INTERPOSER,,CFL-H, BGA1440	U0500	CRITICAL	CPU:SOCKET
337S00570	1	CPU,CFL-H,SRCX4,PRQ,2.8GHz	U0500	CRITICAL	CPU:2.8G
337S00569	1	CPU,CFL-H,SRCX3,PRQ,3.0GHz	U0500	CRITICAL	CPU:3.0G
337S00568	1	CPU,CFL-H,SRCX2,PRQ,3.2GHz	U0500	CRITICAL	CPU:3.2G
337S00618	1	CPU,CFL-H,SRDEC,PRQ,3.6GHz	U0500	CRITICAL	CPU:3.6G

PCH

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00470	1	PCH-H,CNL,QNDQ,ES,A1,BGA874	U1200	CRITICAL	PCH:ES
337S00536	1	PCH-H,CNL,QNYJ,QS,B0,BGA874	U1200	CRITICAL	PCH:QS
337S00577	1	PCH-H,CNL,QNYJ,PRQ,B0,BGA874	U1200	CRITICAL	PCH:PRQ

SSD Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-12416	4	NAND,3DV3,42GBP,S4E,170G,T,SUB X,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:128_TB
998-12418	4	NAND,3DV3,85GBP,S4E,170G,T,SUB X,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:256_TB
998-12420	4	NAND,3DV3,128GBP,S4E,170G,T,SUBX,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:512_TB
998-12424	4	NAND,3DV3,256GBP,S4E,170G,T,SUBX,ULGA110	U8600,U8709,U8800,U8900	CRITICAL	SSD:1T_TB
335S00323	4	NAND,3DV3,42GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:128_SD
335S00324	4	NAND,3DV3,85GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:256_SD
335S00325	4	NAND,3DV3,128GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:512_SD
335S00327	4	NAND,3DV3,256GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:1T_SD
335S00321	4	NAND,3DV4,256GB,ULGA110	U8600,U8709,U8800,U8900	CRITICAL	SSD:1T_SM
335S00373	4	NAND,3DV4,512GB,ULGA110	U8600,U8709,U8800,U8900	CRITICAL	SSD:2T_SM

<- new DVT

SSD ALTERNATIVES

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
998-12421	998-12420	ALL	SSD:512 TB W/X	SSD:512_TB

998-12416 SSD:128_TB_X or TB1
998-12417 SSD:128_TB_W or TB2 TB2 dropped per Marketing

998-12418 SSD:256_TB_X or TB1
998-12419 SSD:256_TB_W or TB2 TB2 dropped per Marketing

998-12420 SSD:512_TB_X or TB1
998-12421 SSD:512_TB_W or TB2

998-12424 SSD:1T_TB_X or TB1
998-12426 SSD:1T_TB_W or TB2 TB2 dropped per Marketing

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 2 OF 142
SHEET: 2 OF 115

Programmable Parts

TBT X ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	U2890	CRITICAL	TBT_X_ROM:BLANK
341S00987	1	IC,T29,TR0,V7.1,DEV,X1036	U2890	CRITICAL	TBT_X_ROM:POC
341S00987	1	IC,T29,TR0,V7.1,DEV,X1036	U2890	CRITICAL	TBT_X_ROM:PROTO
341S01094	1	IC,T29,TR0,V7.1,DEV,X1036	U2890	CRITICAL	TBT_X_ROM:PREEVT
341S01111	1	IC,T29,TBT-X,R1,V21.3,EXT,X1036	U2890	CRITICAL	TBT_X_ROM:EVT
341S01171	1	IC,T29,TBT-X,R1,V28.1,DXT,X1036	U2890	CRITICAL	TBT_X_ROM:DVT

TBT T ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	UB090	CRITICAL	TBT_T_ROM:BLANK
341S00988	1	IC,T29,TR1,V7.1,DEV,X1036	UB090	CRITICAL	TBT_T_ROM:POC
341S00988	1	IC,T29,TR1,V7.1,DEV,X1036	UB090	CRITICAL	TBT_T_ROM:PROTO
341S01095	1	IC,T29,TR1,V7.1,DEV,X1036	UB090	CRITICAL	TBT_T_ROM:PREEVT
341S01110	1	IC,T29,TBT-T,R0,V21.3,EVT,X1036	UB090	CRITICAL	TBT_T_ROM:EVT
341S01170	1	IC,T29,TBT-T,R0,V28.1,DVT,X1036	UB090	CRITICAL	TBT_T_ROM:DVT

MADEA(HDMI) SPI ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00049	1	MADEA SPI FLASH,8MB,1.8V,8P,USON	UA801	CRITICAL	HDMI_ROM:BLANK
341S00991	1	IC,HDMI(V1.106),DEV,X1036	UA801	CRITICAL	HDMI_ROM:PROTO
341S01096	1	IC,HDMI(V1.106),DEV,X1036	UA801	CRITICAL	HDMI_ROM:PREEVT
341S01112	1	IC,HDMI(V2.245),EVT,X1036	UA801	CRITICAL	HDMI_ROM:EVT
341S01172	1	IC,HDMI(V2.005),DVT,X1036	UA801	CRITICAL	HDMI_ROM:DVT

10G ETHERNET ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00269	1	IC SPI FLASH,32MBIT,3V,SOIC8	U9890	CRITICAL	10G_ENET_ROM:BLANK
341S00989	1	IC,ETHERNET 10GB (V2.9.15) DEV,X1036	U9890	CRITICAL	10G_ENET_ROM:PROTO
341S01045	1	IC,ETHERNET 10GB (V2.9.15) DEV,X1036	U9890	CRITICAL	10G_ENET_ROM:PREEVT
341S01113	1	IC,ETHERNET 10GB (V2.10.1) EVT,X1036	U9890	CRITICAL	10G_ENET_ROM:EVT
341S01173	1	IC,ETHERNET 10GB (V2.10.8) DVT,X1036	U9890	CRITICAL	10G_ENET_ROM:DVT

1G ETHERNET ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S1025	1	IC,SERIAL FLASH,2MBIT,2.7V,REV E,SOIC-8	U9390	CRITICAL	1G_ENET_ROM:BLANK
341S00990	1	IC,ETHERNET 1GB (V1.15) DEV,X1036	U9390	CRITICAL	1G_ENET_ROM:PROTO
341S01174	1	IC,ETHERNET 1GB (V1.15) DVT,X1036	U9390	CRITICAL	1G_ENET_ROM:DVT

BT SERIAL FLASH

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00256	1	IC,SPI SERIAL FLASH,2MBIT,1.8V,DFN8	U3750	CRITICAL	BT_FLASH:BLANK
341S00965	1	BT SFLASH ROM(V21) PROTO-2,X1036	U3750	CRITICAL	BT_FLASH:POC
341S01025	1	BT SFLASH ROM(V32) proto,X1036	U3750	CRITICAL	BT_FLASH:PROTO
341S01098	1	BT SFLASH ROM(V32) preEVT,X1036	U3750	CRITICAL	BT_FLASH:PREEVT
341S01119	1	IC,BT SFLASH ROM(V45),EVT,X1036	U3750	CRITICAL	BT_FLASH:EVT
341S01175	1	IC,BT SFLASH ROM(V56),DVT,X1036	U3750	CRITICAL	BT_FLASH:DVT

WLAN SERIAL EEPROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00214	1	IC,EEPROM,SER,UWIRE,16K,1.8V,DFN8	U3710	CRITICAL	WLAN_EEPROM:BLANK
341S00725	1	WIFI ROM,V01,WW1,X665	U3710	CRITICAL	WLAN_EEPROM:DVT

The same as proto and later

SOC ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00203	1	IC,FLASH,SPI,4MX8.1V8,DFN8	U4770	CRITICAL	SOC_ROM:BLANK

SEP EEPROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00469	1	IC,MCU,ARM,SC000,STLNX,A0,DIVKEY,DFN8	U4730	CRITICAL	SEPROM:LYNX
335S0888	1	IC,SERIAL I2C EEPROM,128KBIT,8P,MLP8	U4730	CRITICAL	SEPROM:OG

Alternatives section 1

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
152S00573	152S1778	ALL	INDUCTOR	
152S00748	152S00697	ALL	INDUCTOR	
152S00801	152S00695	ALL	INDUCTOR	
155S00363	155S00364	ALL	CMC	
353S00772	353S4070	ALL	DISPLAY MUX	
353S4068	353S4070	ALL	DISPLAY MUX	
376S00074	376S0855	ALL	DUAL FET	
372S0186	372S0185	ALL	TRANSISTOR	
371S00095	371S0567	ALL	DIODE	
371S0684	371S0495	ALL	DIODE	
371S00042	371S00125	ALL	DIODE	
339S00389	339S00388	ALL	H9ML	
311S00013	311S0508	ALL	BUFFER	
335S00270	335S00203	ALL	SoC ROM	
128S00081	128S0264	ALL	CAP	
128S0364	128S0264	ALL	CAP	
377S0155	377S0184	ALL	ESD Diode	
377S0077	377S0183	ALL	ESD Diode	
377S00079	377S00077	ALL	Diode	
377S0178	377S00031	ALL	ESD Diode	
376S00224	376S1128	ALL	FET	
353S01041	353S01042	ALL	Vref IC	
353S00750	353S00877	ALL	LDO	
376S0636	376S1004	ALL	FET	
311S0426	311S00007	ALL	BUFFER	
335S00213	335S0888	ALL	SEP ROM	
311S0596	311S0593	ALL	LOGIC GATE	
311S0372	311S0562	ALL	LOGIC GATE	
311S00138	311S0436	ALL	LEVEL SHIFTER	
311S0562	311S0372	ALL	LOGIC GATE	
311S00133	311S00130	ALL	BUFFER	
197S00118	197S00120	ALL	CRYSTAL	
197S0612	197S00120	ALL	CRYSTAL	
197S00053	197S00050	ALL	Y1900 radar 37073234	
197S00054	197S00050	ALL	Y1900 radar 37073234	
197S00055	197S00050	ALL	Y1900 radar 37073234	
197S00048	197S00036	ALL	Y3800,etc radar 37073152	
311S00121	311S0398	ALL	AND Gate DFN pack	
311S0398	311S00121	ALL	AND Gate DFN pack	
138S0860	138S0775	ALL	C7101,etc radar 38188751	
138S0933	138S0931	ALL	C7525,etc radar 38079576	

Alternatives section continued on CSA 142

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-02424 | SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 3 OF 142
SHEET: 3 OF 115

Boss on TOP side

2x 860-00935.

B0400
8.70D4.2ID-1.75H-SM

B0401
8.70D4.2ID-1.75H-SM

9x 860-00913.

B0406
BOSS-3.00D1.20ID-2.80H-SM

B0409
BOSS-3.00D1.20ID-2.80H-SM

B0410
BOSS-3.00D1.20ID-2.80H-SM

B0412
BOSS-3.00D1.20ID-2.80H-SM

B0413
BOSS-3.00D1.20ID-2.80H-SM

B0414
BOSS-3.00D1.20ID-2.80H-SM

B0415
BOSS-3.00D1.20ID-2.80H-SM

B0417
BOSS-3.00D1.20ID-2.80H-SM

B0416
BOSS-3.00D1.20ID-2.80H-SM

Boss on BOTTOM side

2x 860-00929.

B0407
BOSS-6.00D5.95H-TH-1.4-2.6

B0418
BOSS-6.00D5.95H-TH-1.4-2.6

2x 860-1438.

B0404
4.00D1.55H-M1.6X0.35-ST

B0403 WIFI
4.00D1.55H-M1.6X0.35-ST

2x 860-01020.

B0419
BOSS-4.00D2.2ID-4.25H-SM

B0408
BOSS-4.00D2.2ID-4.25H-SM

CPU Sled on TOP side:

2x 806-16518

CKPLUS_WAIVE=TERMSHORTED
SP0400
SLED-CPU-X1035
SMT-PAD-SP

CKPLUS_WAIVE=TERMSHORTED
SP0401
SLED-CPU-X1035
SMT-PAD-SP

Antenna cable clips:

3x 806-15581.

CKPLUS_WAIVE=TERMSHORTED
CLIP-ANT-LONG-X1035
CL0400
SM

CKPLUS_WAIVE=TERMSHORTED
CLIP-ANT-LONG-X1035
CL0401
SM

CKPLUS_WAIVE=TERMSHORTED
CLIP-ANT-LONG-X1035
CL0402
SM

Shield Cans:

604-19182.DIMM Shield

SH0400
SM
SHLD-FENCE-DIMM-X1035

806-14422.H9ML Fence

SH0401
SM
SHLD-FENCE-GIB-X1035

806-14495.Harpoon Fence

SH0402
SM
SHLD-FENCE-HARPN-X1035

806-16657 HDMI Shield Can

SH0420
SM
SHLD-HDMI-X1035

806-14019.UBSC-IO EMI Fence

SH0404
SM
SHLD-FENCE-TOP-USBC-X1035

806-14020.IO EMI Fence

SH0407
SM
SHLD-FENCE-TOP-IO-X1035

806-14423.Ridge Shield

SH0405
SM
SHLD-FENCE-RIDGE-X1035

806-14022 SSD Fence

SH0406
SM
SHLD-FENCE-SSD-X1035

806-15424.Diplexer Shield Can

SH0408
SM
SHLD-MLB-DIPLEXERS-X1035

Through holes of shields:

DIMM shield holes:2x 998-13324

SL0411
TH-NSP
SL-1.5X0.55-1.9X0.95

SL0413
TH-NSP
SL-1.5X0.55-1.9X0.95

Harpoon shield holes:2x 998-04440

SL0400
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0401
TH-NSP
SL-1.2X0.4-1.5X0.7

USBC IO shield holes:2x 998-04440

SL0403
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0402
TH-NSP
SL-1.2X0.4-1.5X0.7

3-pack IO shield holes:1x 998-04440
1x 998-13325

SL0404
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0412
TH-NSP
SL-1.05X0.4-1.45X0.8

Ridges shield holes:2x 998-04440

SL0406
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0405
TH-NSP
SL-1.2X0.4-1.5X0.7

H9ML shield holes:2x 998-04440

SL0408
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0407
TH-NSP
SL-1.2X0.4-1.5X0.7

SSD shield holes:2x 998-04440

SL0410
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0409
TH-NSP
SL-1.2X0.4-1.5X0.7

HDMI shield holes:2x 998-04440

SL0420
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0421
TH-NSP
SL-1.2X0.4-1.5X0.7

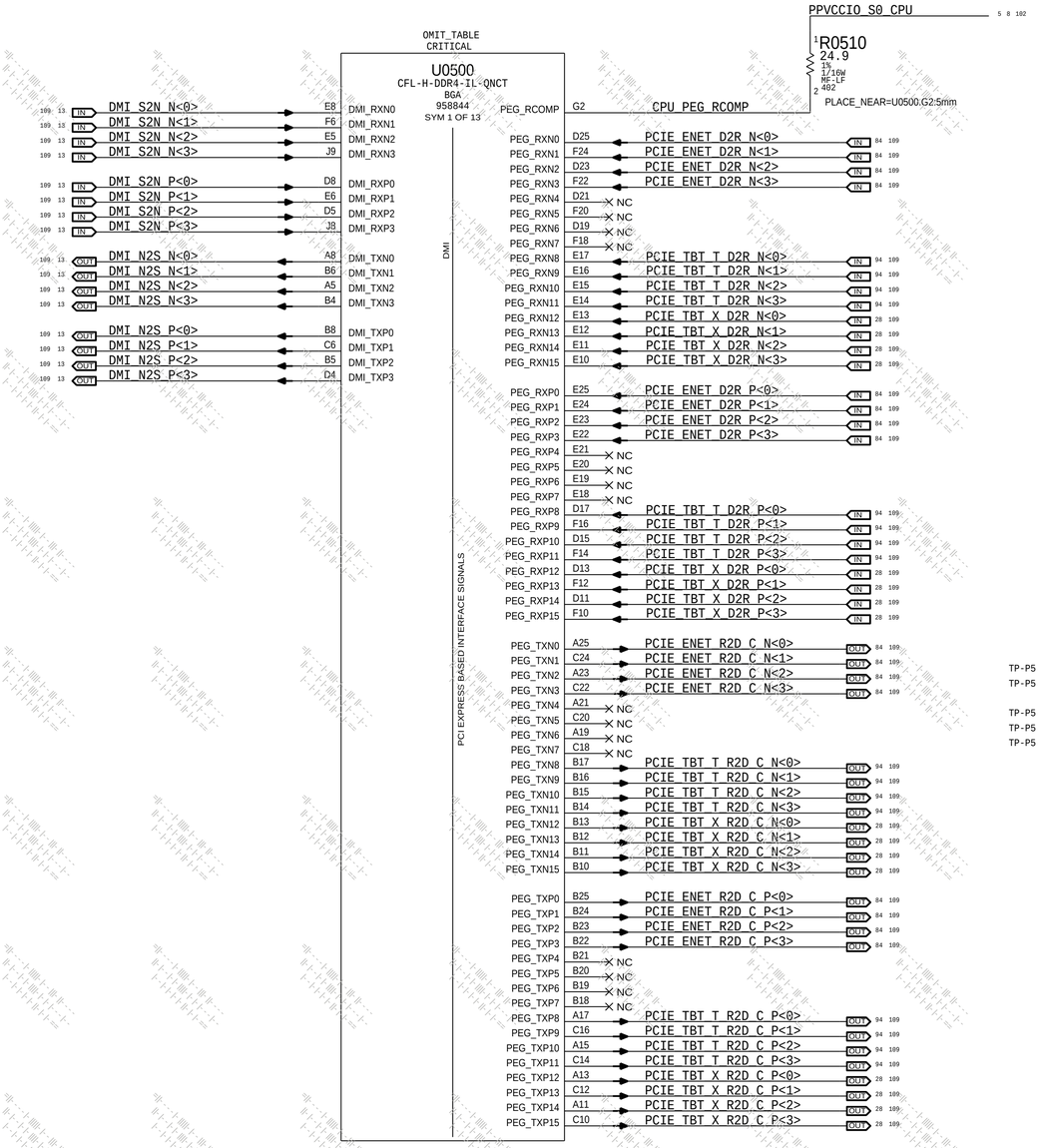
BOM_COST_GROUP=MECHANICALS

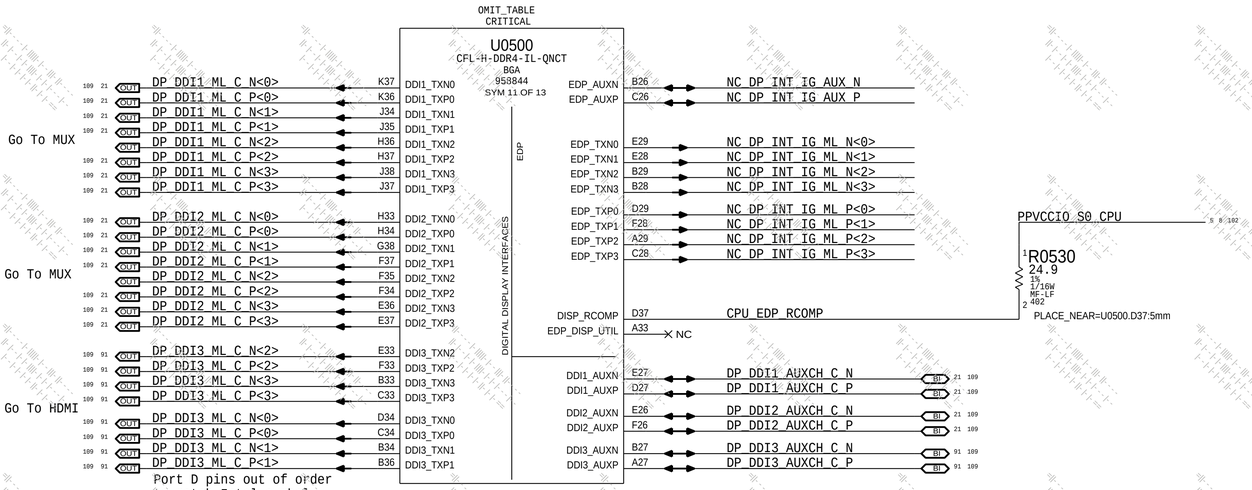
SYNC_MASTER=Mary SYNC_DATE=04/26/2018

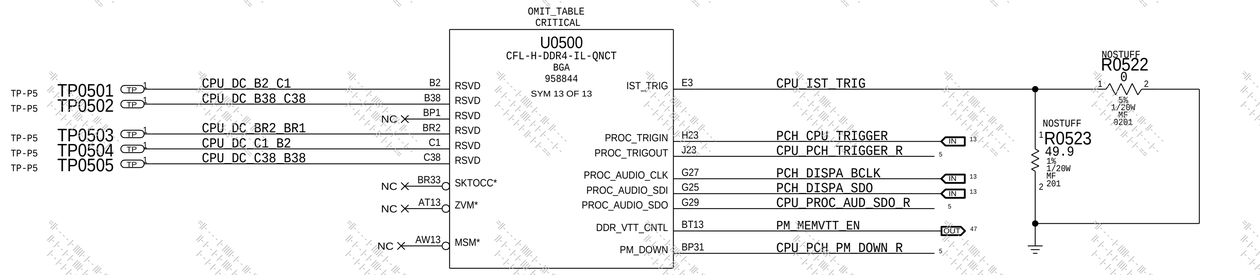
PAGE TITLE
PD Parts

Apple Inc.

DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 4 OF 142
SHEET 4 OF 115

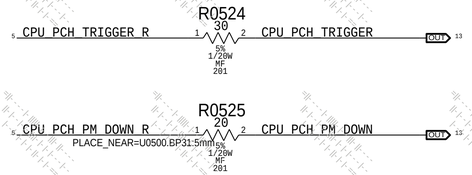






CPU Daisy-Chain Strategy:

Each corner of CPU has two testpoints.
Other corner test signals connected in
daisy-chain fashion. Continuity should
exist between both TP's on each corner.

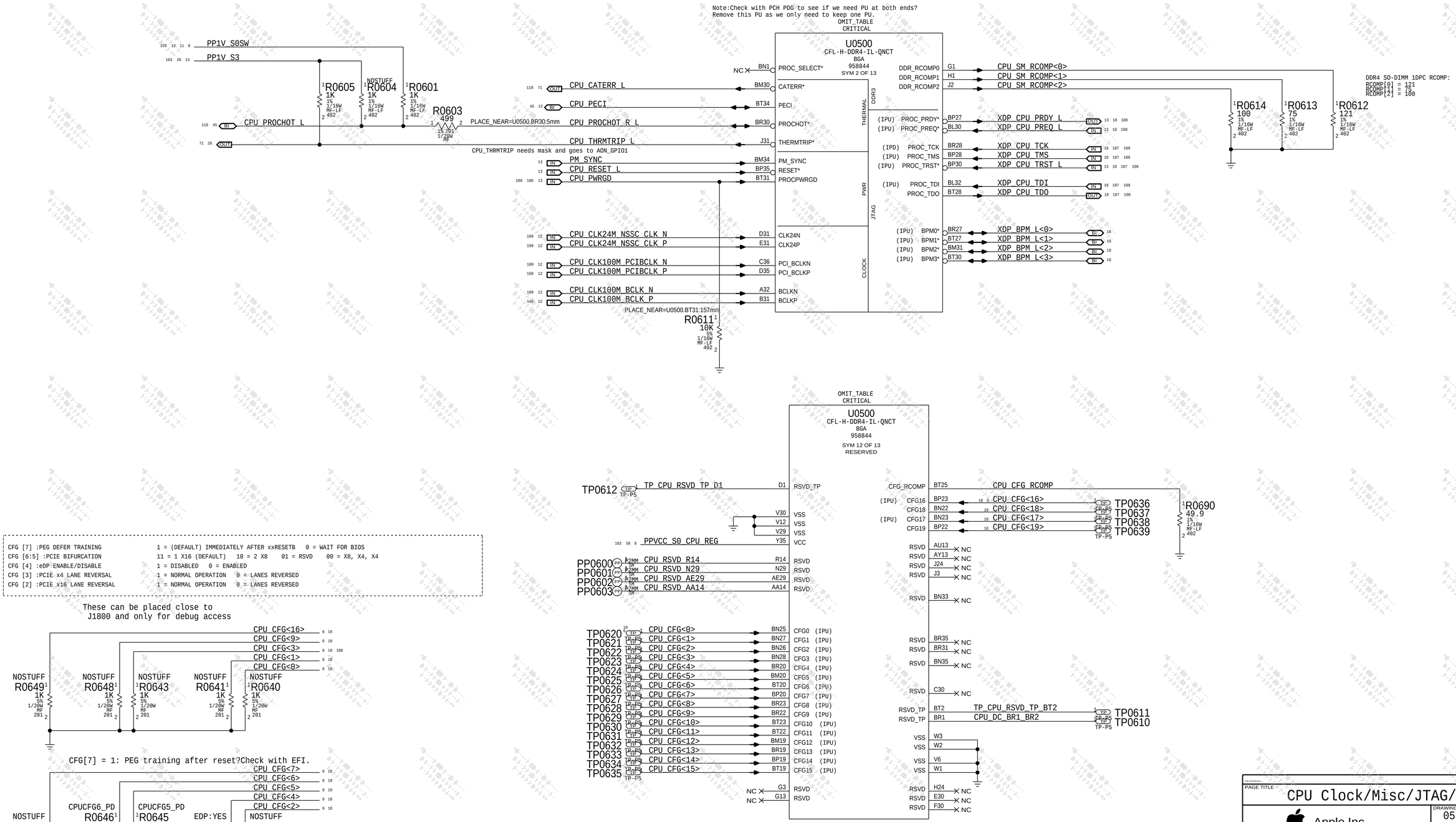


BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

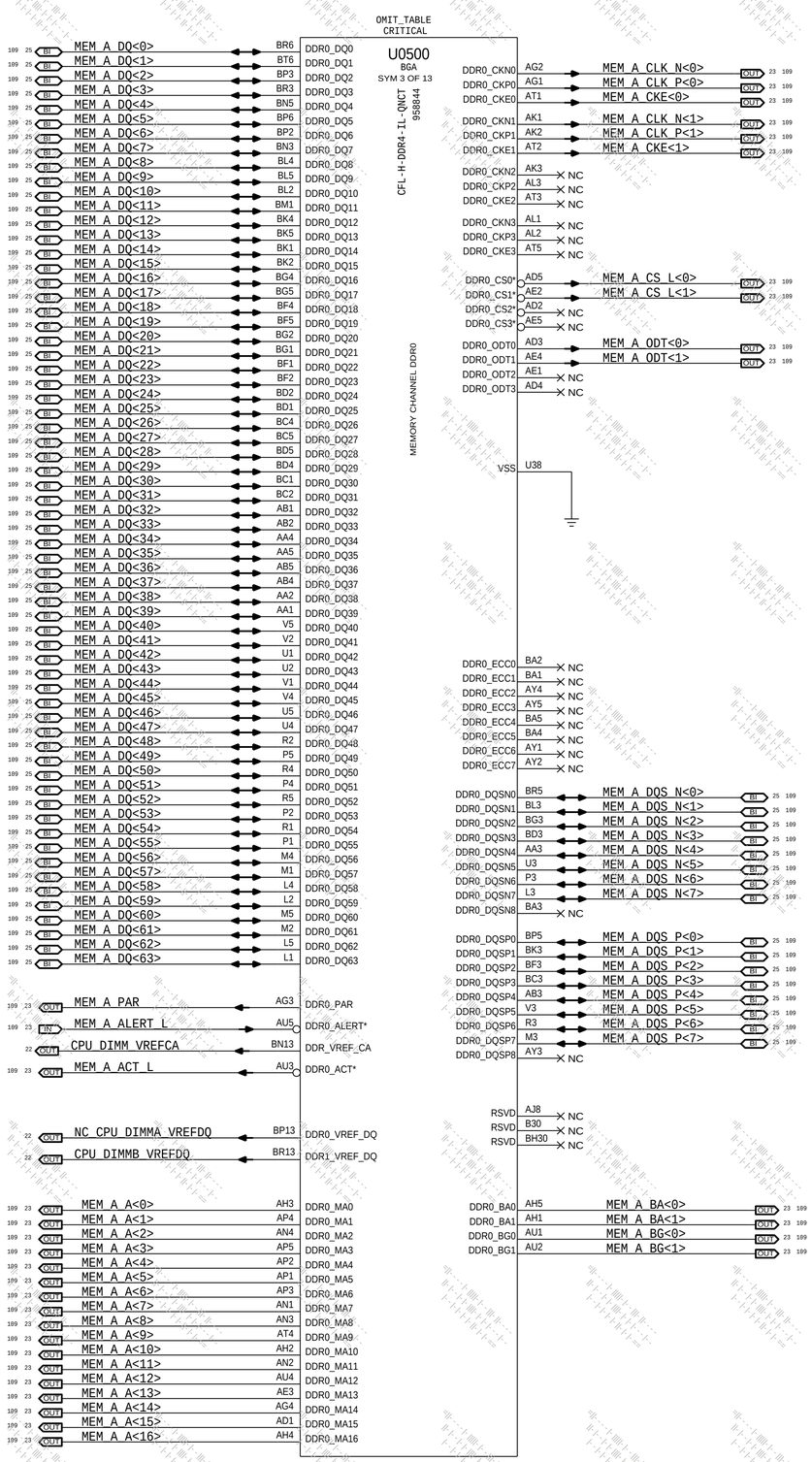
Apple Inc.

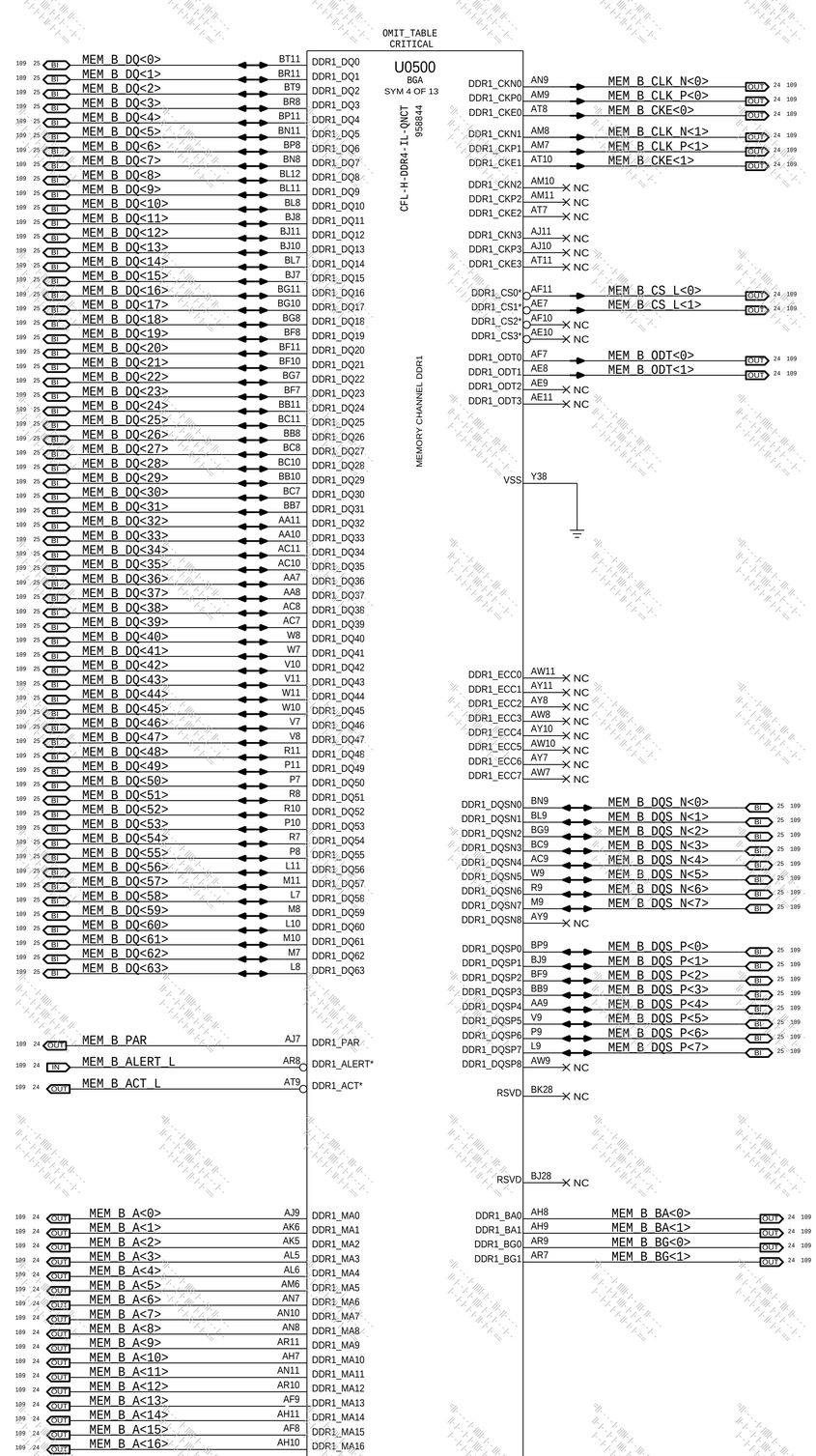
DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 5 OF 142
SHEET: 5 OF 115



BOM GROUP	BOM OPTIONS
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.





BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=n/a SYNC_DATE=04/26/2018

PAGE TITLE

CPU DDR4 Interfaces

Apple Inc.

DRAWING NUMBER 051-02424

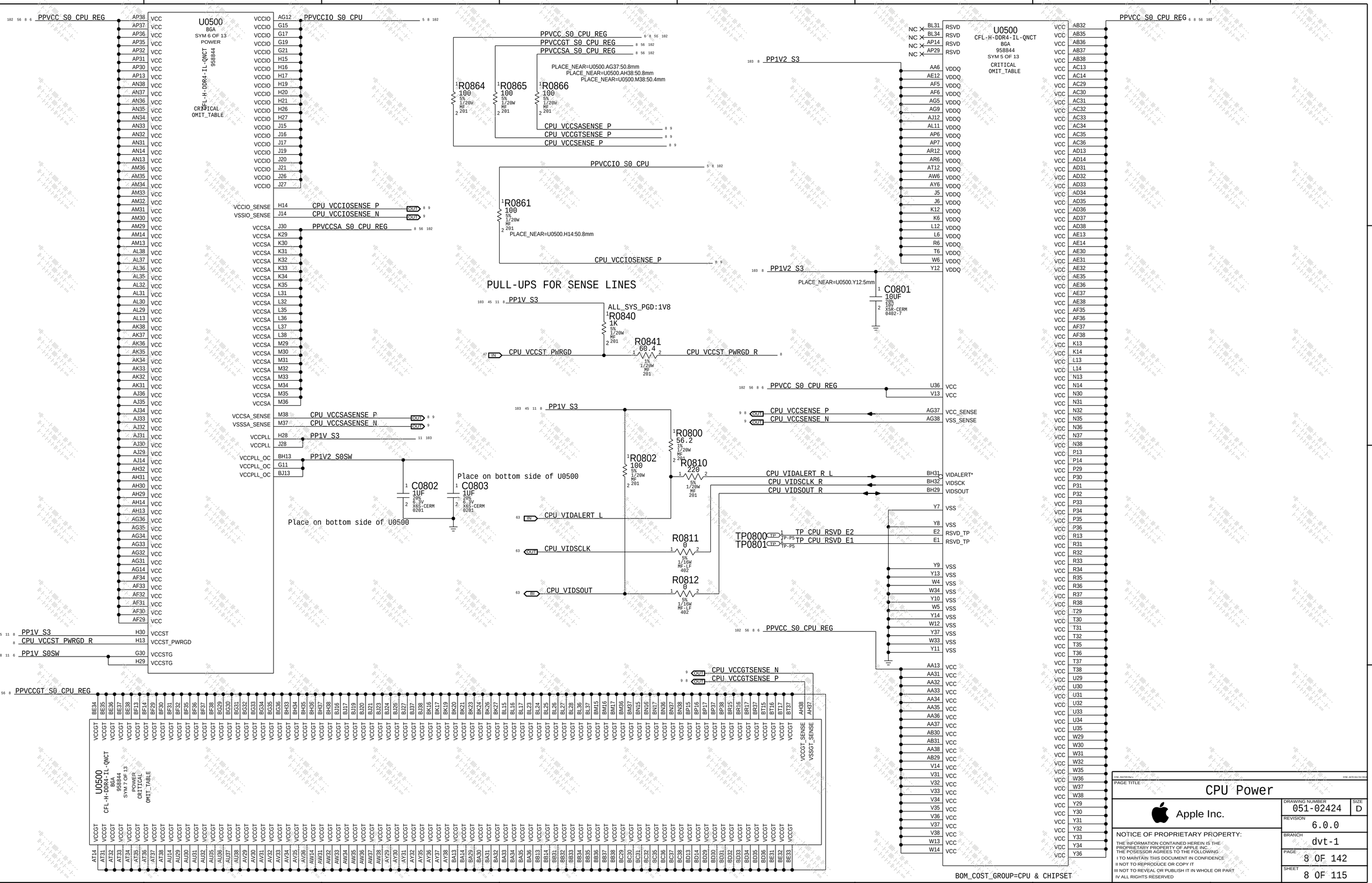
SIZE D

REVISION 6.0.0

BRANCH dvt-1

PAGE 7 OF 142

SHEET 7 OF 115



PAGE TITLE

CPU Power

Apple Inc.

DRAWING NUMBER 051-02424 | SIZE D

REVISION 6.0.0

BRANCH dvt-1

PAGE 8 OF 142

SHEET 8 OF 115

OMIT_TABLE
CRITICAL

U0500
CFL-H-DDR4-IL-QNCT
BGA
958844
SYM 8 OF 13
GROUND

A3	VSS	VSS	AH33
A4	VSS	VSS	AH34
A6	VSS	VSS	AH35
A9	VSS	VSS	AH36
A10	VSS	VSS	AJ1
A12	VSS	VSS	AJ2
A14	VSS	VSS	AJ3
A16	VSS	VSS	AJ4
A18	VSS	VSS	AJ5
A20	VSS	VSS	AJ6
A22	VSS	VSS	AJ13
A24	VSS	VSS	AJ37
A26	VSS	VSS	AJ38
A34	VSS	VSS	AK4
A36	VSS	VSS	AK29
A37	VSS	VSS	AK30
AA12	VSS	VSS	AL4
AA29	VSS	VSS	AL7
AA30	VSS	VSS	AL8
AB6	VSS	VSS	AL9
AB33	VSS	VSS	AL10
AB34	VSS	VSS	AL12
AC1	VSS	VSS	AL14
AC2	VSS	VSS	AL33
AC3	VSS	VSS	AL34
AC4	VSS	VSS	AM1
AC5	VSS	VSS	AM2
AC6	VSS	VSS	AM3
AC12	VSS	VSS	AM4
AC37	VSS	VSS	AM5
AC38	VSS	VSS	AM12
AD6	VSS	VSS	AM37
AD7	VSS	VSS	AM38
AD8	VSS	VSS	AN5
AD9	VSS	VSS	AN6
AD10	VSS	VSS	AN12
AD11	VSS	VSS	AN29
AD12	VSS	VSS	AN30
AD29	VSS	VSS	AP8
AD30	VSS	VSS	AP9
AE6	VSS	VSS	AP10
AE33	VSS	VSS	AP11
AE34	VSS	VSS	AP12
AF1	VSS	VSS	AP33
AF2	VSS	VSS	AP34
AF3	VSS	VSS	AR1
AF4	VSS	VSS	AR2
AF12	VSS	VSS	AR3
AF13	VSS	VSS	AR4
AF14	VSS	VSS	AR5
AG6	VSS	VSS	AR13
AG7	VSS	VSS	AR14
AG8	VSS	VSS	AR29
AG10	VSS	VSS	AR30
AG11	VSS	VSS	AR31
AG13	VSS	VSS	AR32
AG29	VSS	VSS	AR33
AG30	VSS	VSS	AR34
AH6	VSS	VSS	AR35
AH12	VSS		

OMIT_TABLE
CRITICAL

U0500
CFL-H-DDR4-IL-QNCT
BGA
958844
SYM 9 OF 13
GROUND

AR36	VSS	VSS	BG37
AR37	VSS	VSS	BG38
AR38	VSS	VSS	BH1
AT6	VSS	VSS	BH2
AT29	VSS	VSS	BH3
AT30	VSS	VSS	BH4
AU6	VSS	VSS	BH5
AU7	VSS	VSS	BH6
AU8	VSS	VSS	BH7
AU9	VSS	VSS	BH8
AU10	VSS	VSS	BH9
AU11	VSS	VSS	BH10
AU12	VSS	VSS	BH11
AU33	VSS	VSS	BH12
AU34	VSS	VSS	BH14
AV37	VSS	VSS	BJ12
AV38	VSS	VSS	BJ14
AW1	VSS	VSS	BJ15
AW2	VSS	VSS	BJ18
AW3	VSS	VSS	BJ22
AW4	VSS	VSS	BJ25
AW5	VSS	VSS	BJ29
AW12	VSS	VSS	BJ30
AW29	VSS	VSS	BJ31
AW30	VSS	VSS	BJ32
AY12	VSS	VSS	BJ33
AY14	VSS	VSS	BJ34
AY33	VSS	VSS	BJ35
AY34	VSS	VSS	BJ36
B3	VSS	VSS	BK6
B9	VSS	VSS	BK13
B37	VSS	VSS	BK14
BA6	VSS	VSS	BK15
BA7	VSS	VSS	BK18
BA8	VSS	VSS	BK22
BA9	VSS	VSS	BK25
BA10	VSS	VSS	BK29
BA11	VSS	VSS	BL6
BA12	VSS	VSS	BL13
BA37	VSS	VSS	BL14
BA38	VSS	VSS	BL18
BB1	VSS	VSS	BL19
BB2	VSS	VSS	BL20
BB3	VSS	VSS	BL21
BB4	VSS	VSS	BL22
BB5	VSS	VSS	BL29
BB6	VSS	VSS	BL33
BB12	VSS	VSS	BL35
BB29	VSS	VSS	BL38
BB30	VSS	VSS	BM2
BC6	VSS	VSS	BM3
BC12	VSS	VSS	BM5
BC13	VSS	VSS	BM6
BC14	VSS	VSS	BM7
BC33	VSS	VSS	BM8
BC34	VSS	VSS	BM9
BD6	VSS	VSS	BM11
BD7	VSS	VSS	BM12
BD8	VSS	VSS	BM13
BD9	VSS	VSS	BM14
BD10	VSS	VSS	BM18
BD11	VSS	VSS	BM21
BD12	VSS	VSS	BM22
BD37	VSS	VSS	BM23
BD38	VSS	VSS	BM24
BE1	VSS	VSS	BM25
BE2	VSS	VSS	BM26
BE3	VSS	VSS	BM27
BE4	VSS	VSS	BM28
BE5	VSS	VSS	BM29
BE6	VSS	VSS	BM33
BE29	VSS	VSS	BM35
BE30	VSS	VSS	BM38
BF6	VSS	VSS	BN2
BF12	VSS	VSS	BN19
BF33	VSS	VSS	C37
BF34	VSS	VSS	D3
BG6	VSS	VSS	D28
BG12	VSS	VSS	D30
BG13	VSS	VSS	D33
BG14	VSS	VSS	L33

OMIT_TABLE
CRITICAL

U0500
CFL-H-DDR4-IL-QNCT
BGA
958844
SYM 10 OF 13
GROUND

A28	VSS	VSS	F21
A30	VSS	VSS	F23
BN4	VSS	VSS	F25
BN7	VSS	VSS	F27
BN12	VSS	VSS	F29
BN14	VSS	VSS	F31
BN18	VSS	VSS	F36
BN20	VSS	VSS	G4
BN21	VSS	VSS	G5
BN24	VSS	VSS	G6
BN29	VSS	VSS	G8
BN30	VSS	VSS	G9
BN31	VSS	VSS	G10
BN34	VSS	VSS	G12
BP7	VSS	VSS	G14
BP12	VSS	VSS	G16
BP14	VSS	VSS	G18
BP18	VSS	VSS	G20
BP21	VSS	VSS	G22
BP24	VSS	VSS	G23
BP25	VSS	VSS	G24
BP26	VSS	VSS	G26
BP29	VSS	VSS	G28
BP33	VSS	VSS	H11
BP34	VSS	VSS	H12
BR7	VSS	VSS	H18
BR9	VSS	VSS	H22
BR12	VSS	VSS	H25
BR14	VSS	VSS	H32
BR18	VSS	VSS	H35
BR21	VSS	VSS	J4
BR24	VSS	VSS	J7
BR25	VSS	VSS	J10
BR26	VSS	VSS	J18
BR29	VSS	VSS	J22
BR34	VSS	VSS	J25
BR36	VSS	VSS	J32
BR38	VSS	VSS	J33
BT3	VSS	VSS	J36
BT4	VSS	VSS	K1
BT5	VSS	VSS	K2
BT8	VSS	VSS	K3
BT12	VSS	VSS	K4
BT14	VSS	VSS	K5
BT18	VSS	VSS	K7
BT21	VSS	VSS	K8
BT24	VSS	VSS	K9
BT26	VSS	VSS	K10
BT29	VSS	VSS	K11
BT32	VSS	VSS	K38
BT35	VSS	VSS	L29
BT36	VSS	VSS	L30
C2	VSS	VSS	L34
C5	VSS	VSS	M6
C8	VSS	VSS	M12
C9	VSS	VSS	M13
C11	VSS	VSS	M14
C13	VSS	VSS	N1
C15	VSS	VSS	N2
C17	VSS	VSS	N3
C19	VSS	VSS	N4
C21	VSS	VSS	N5
C23	VSS	VSS	N6
C25	VSS	VSS	N7
C27	VSS	VSS	N8
C29	VSS	VSS	N9
C31	VSS	VSS	N10
D6	VSS	VSS	N11
D9	VSS	VSS	N12
D10	VSS	VSS	N33
D12	VSS	VSS	N34
D14	VSS	VSS	P6
D16	VSS	VSS	P12
D18	VSS	VSS	P37
D20	VSS	VSS	P38
D22	VSS	VSS	R12
D24	VSS	VSS	R29
D26	VSS	VSS	R30
D38	VSS	VSS	T1
E4	VSS	VSS	T2
E9	VSS	VSS	T3
E34	VSS	VSS	T4
E35	VSS	VSS	T5
E38	VSS	VSS	T7
F2	VSS	VSS	T8
F3	VSS	VSS	T9
F4	VSS	VSS	T10
F5	VSS	VSS	T11
F8	VSS	VSS	T12
F9	VSS	VSS	T13
F11	VSS	VSS	T14
F13	VSS	VSS	T33
F15	VSS	VSS	T34
F17	VSS	VSS	U6
F19	VSS	VSS	U37

CPU_VCCGTSENSE_N
CPU_VCCIOSENSE_N
CPU_VCCSASENSE_N
CPU_VCCSENSE_N

OUT 8 9

R0961 100 5% 1/20W MF 201
R0963 100 5% 1/20W MF 201
R0965 100 5% 1/20W MF 201
R0966 100 5% 1/20W MF 201

8 IN CPU_VCCGTSENSE_P — CPU_VCCGTSENSE_P OUT 63
9 8 IN CPU_VCCGTSENSE_N — CPU_VCCGTSENSE_N OUT 63
8 IN CPU_VCCSASENSE_P — CPU_VCCSASENSE_P OUT 63
9 8 IN CPU_VCCSASENSE_N — CPU_VCCSASENSE_N OUT 63
8 IN CPU_VCCSENSE_P — CPU_VCCSENSE_P OUT 63
9 8 IN CPU_VCCSENSE_N — CPU_VCCSENSE_N OUT 63
8 IN CPU_VCCIOSENSE_P — CPU_VCCIOSENSE_P OUT 73
9 8 IN CPU_VCCIOSENSE_N — CPU_VCCIOSENSE_N OUT 73

MAKE_BASE=TRUE

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=Mary
SYNC_DATE=04/29/2016

PAGE TITLE
CPU Ground

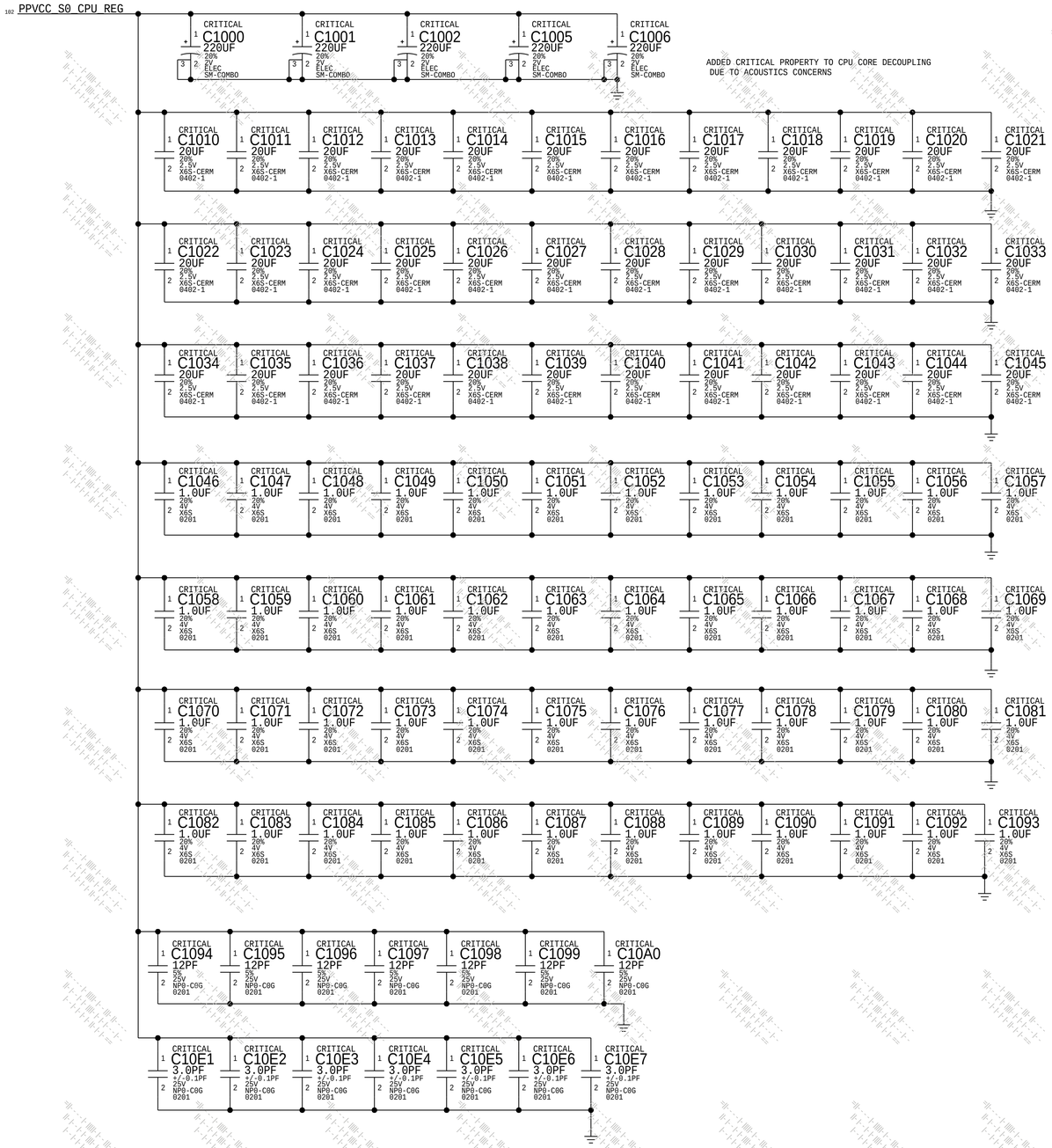
Apple Inc.

DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 9 OF 142
SHEET 9 OF 115

CPU VCORE DECOUPLING

Intel Recommendation:3x 330uF near CPU
5x 47uF 0805 @ board edge
12x 22UF 0603,21x 10uF 0402,24x 1uF 0201,24x 0201(placeholder) @ back side

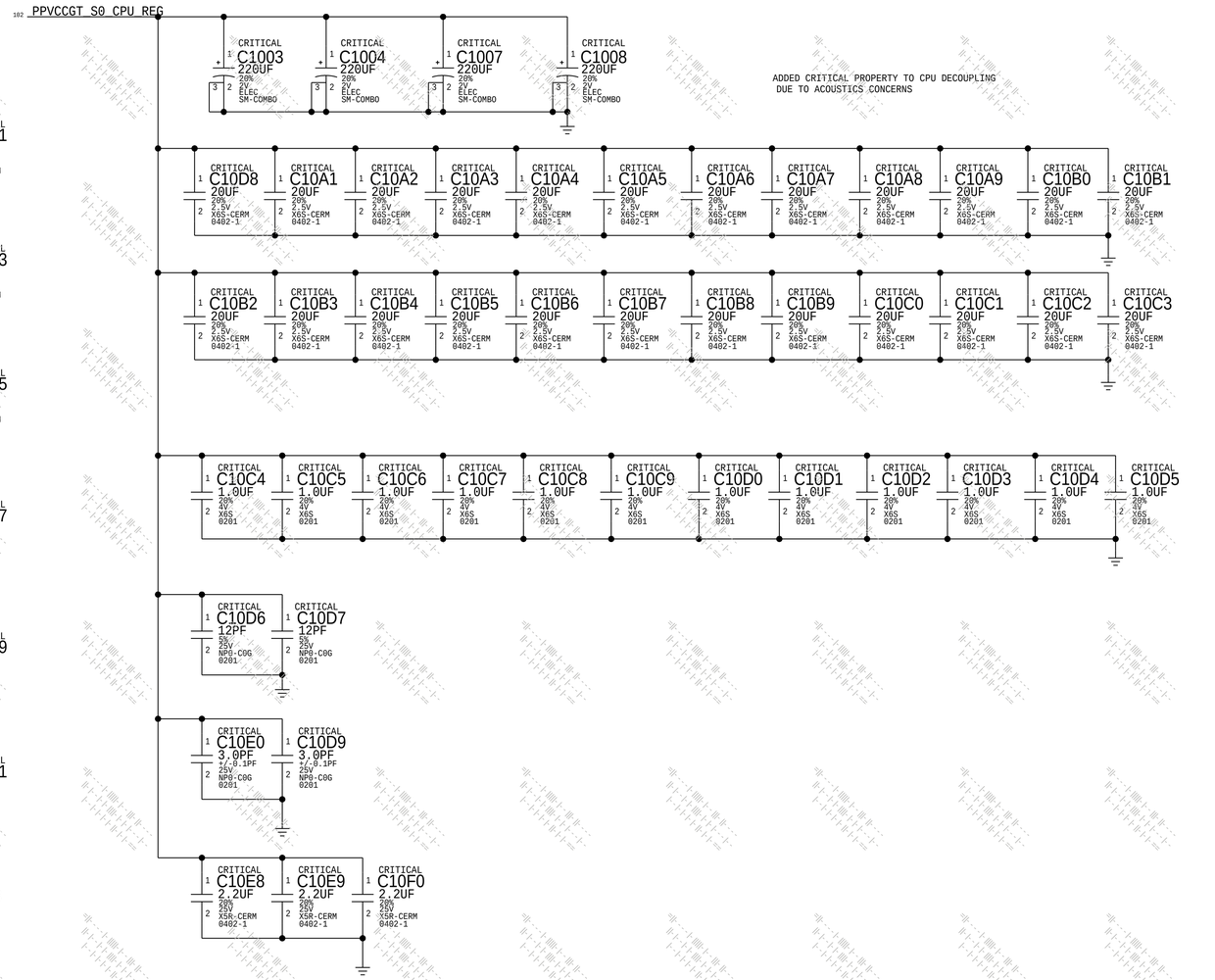
Apple Implementation:5x 220uF
36x 20uF
48x 1uF
7x 12pF and 3pF
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



CPU GT DECOUPLING

INTEL RECOMMENDATION:2X 220uF Near CPU
3X 47uF 0805,7x 22uF 0603 @ board edge
10x 10uF 0402,12x 1uF 0201 @ back side

Apple Implementation: 4x 220uF
24x 20uF
12x 1uF
2x 12pF and 3pF
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: CPU Decoupling 1

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

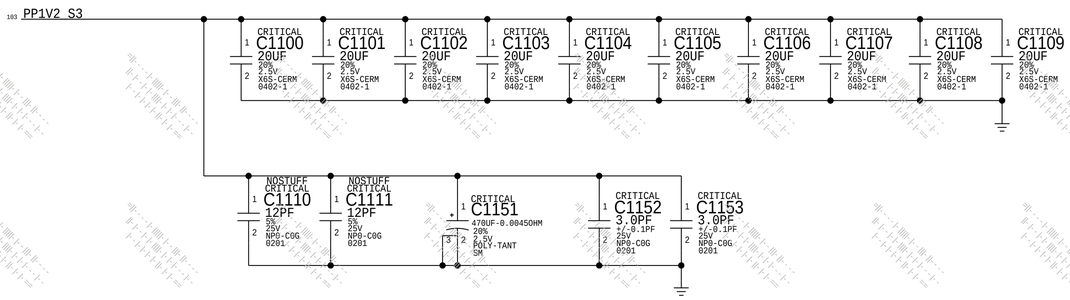
BRANCH: dvt-1

PAGE: 10 OF 142

SHEET: 10 OF 115

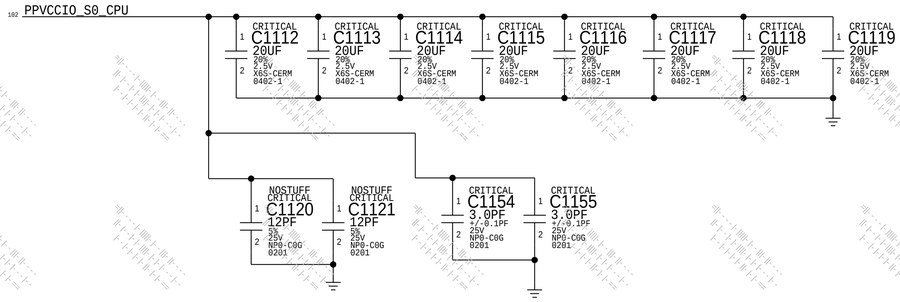
Memory (CPU VCCDDR) DECOUPLING

INTEL RECOMMENDATION:4X 22uF 0603,11x 10uF 0402 (back side)
Apple Implementation:10x 20uF
2x 12pF and 3pF (NO STUFF)
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



CPU VCCIO DECOUPLING

Intel Recommendation:2x 47UF 0805 near VR ouput
3x 10uF 0402,3x 0402 placeholder @ back side
Apple Implementation:8x 20uF
2x 12pF and 3pF (NO STUFF)
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.

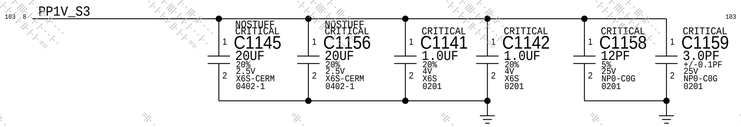


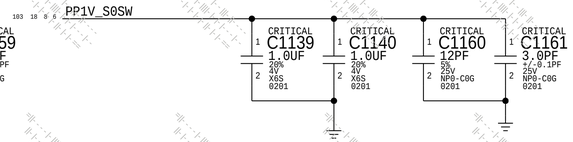
CPU VCCST / VCCSTG / VCCPLL / VCCPLL_OC DECOUPLING

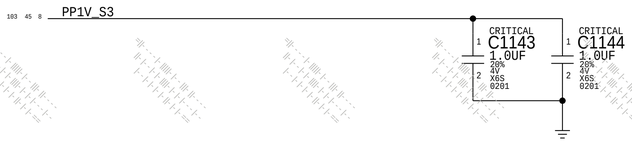
Intel Recommendation: VCCST: 1x 1uF 0201
VCCSTG: 1x 1uF 0201
VCCPLL: 1x 1uF 0201,1x 22uF/47uF 0805 placeholder
VCCPLL_OC: 2x 1uF 0201

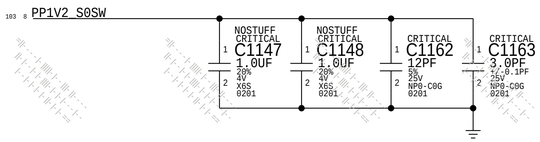
Apple Iimplementation: VCCST: 2x 1uF
VCCSTG: 2x 1uF
VCCPLL: 2x 20uF,2x 1uF
VCCPLL_OC: 2x 1uF

Layout Note: All these Must be Ground referenced.
VCCSTG board routing resistance from BGA to gate should less than 10mOhm.
Do not route VCCSTG closet adjcent layer over any power net other than GND.



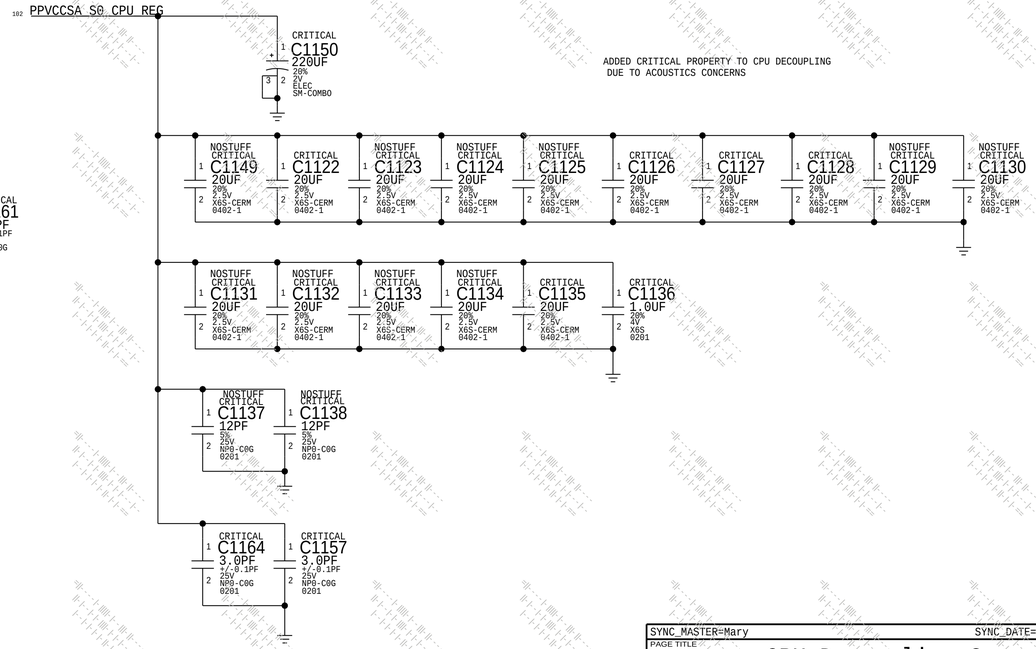






CPU VCCSA DECOUPLING

Intel Recommendation:2x 47uF 0805 near CPU
2x 47uF 0805,2x 22uF 0603 @ board edge
7x 10uF 0402,1x 1uF 0201 @ backside
Apple Implementation:1x 220uF
5x 20uF
1x 1uF
2x 12pF and 3pF (NO STUFF)



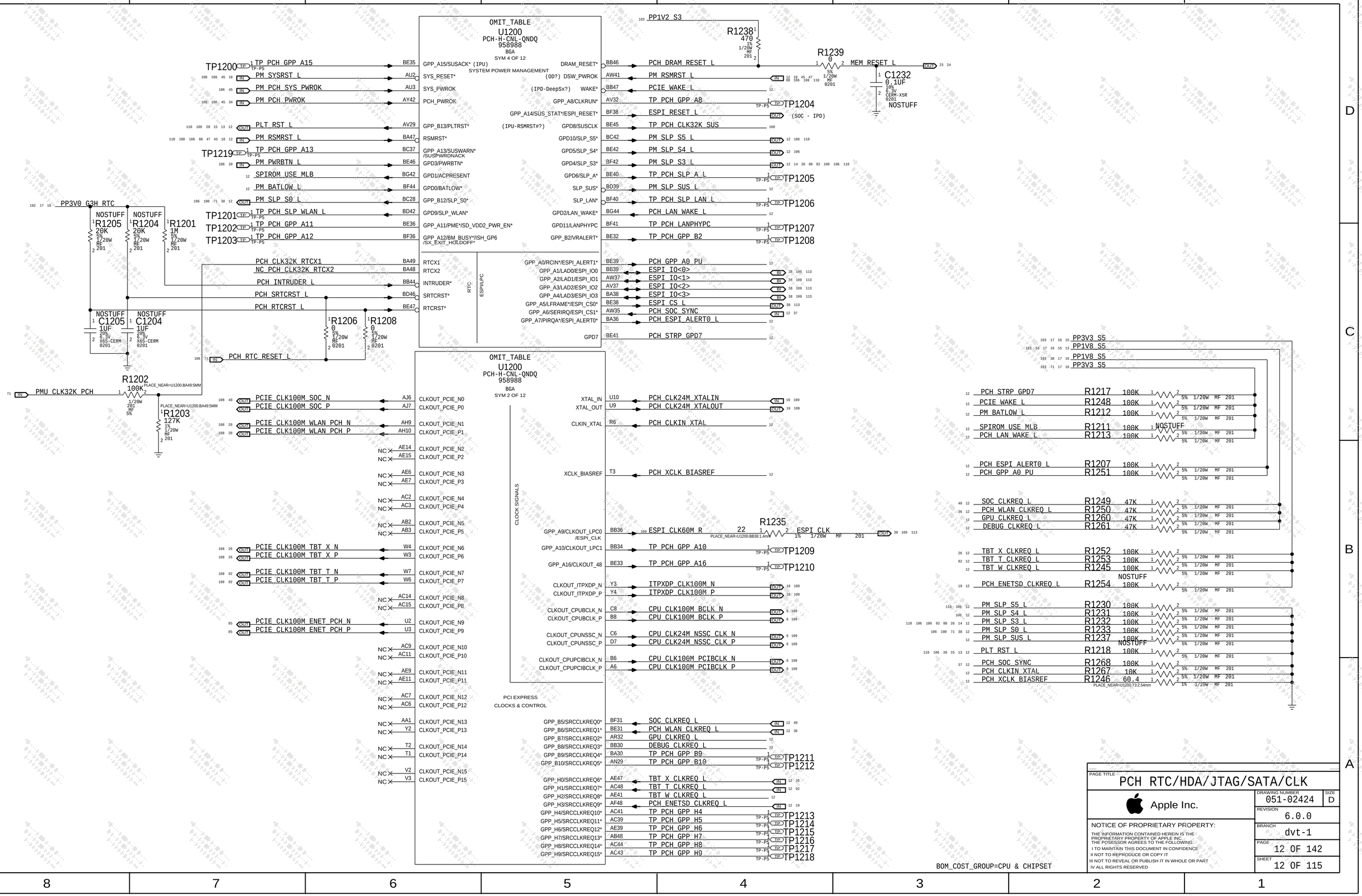
BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: CPU Decoupling 2

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 11 OF 142
SHEET: 11 OF 115


OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 4 OF 12
SYSTEM POWER MANAGEMENT
GPP_A15/SUSACK* (IPU)
SYS_RESET*
SYS_PWROK
PCH_PWROK
GPP_B13/PLTRST*
RSMRST*
GPP_A13/SUSWARN*/SUSPWRDNACK
GPD3/PWRBTN*
GPD1/ACPRESENT
GPD0/BATLOW*
GPP_B12/SLP_S0*
GPD9/SLP_WLAN*
GPP_A11/PME*/SD_VDD2_PWR_EN*
GPP_A12/BM_BUSY*/ISH_GP6/SX_EXIT_HOLDOFF*
DRAM_RESET*
(OD?) DSW_PWROK
(IPD-DeepSx?) WAKE*
GPP_A8/CLKRUN*
GPP_A14/SUS_STAT*/ESPI_RESET*
(IPU-RSMRST#?) GPD8/SUSCLK
GPD10/SLP_S5*
GPD5/SLP_S4*
GPD4/SLP_S3*
GPD6/SLP_A*
SLP_SUS*
SLP_LAN*
GPD2/LAN_WAKE*
GPD11/LANPHYPC
GPP_B2/VRALERT*
RTC
RTCX1
RTCX2
INTRUDER*
SRTCRST*
RTCRST*
ESPI/LPC
GPP_A0/RCIN*/ESPI_ALERT1*
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME*/ESPI_CS0*
GPP_A6/SERIRQ/ESPI_CS1*
GPP_A7/PIRQA*/ESPI_ALERT0*
GPD7
OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 2 OF 12
CLOCK SIGNALS
PCI EXPRESS
CLOCKS & CONTROL
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
CLKOUT_PCIE_N8
CLKOUT_PCIE_P8
CLKOUT_PCIE_N9
CLKOUT_PCIE_P9
CLKOUT_PCIE_N10
CLKOUT_PCIE_P10
CLKOUT_PCIE_N11
CLKOUT_PCIE_P11
CLKOUT_PCIE_N12
CLKOUT_PCIE_P12
CLKOUT_PCIE_N13
CLKOUT_PCIE_P13
CLKOUT_PCIE_N14
CLKOUT_PCIE_P14
CLKOUT_PCIE_N15
CLKOUT_PCIE_P15
XTAL_IN
XTAL_OUT
CLKIN_XTAL
XCLK_BIASREF
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A16/CLKOUT_48
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_CPUBCLK_N
CLKOUT_CPUBCLK_P
CLKOUT_CPUNSSC_N
CLKOUT_CPUNSSC_P
CLKOUT_CPUPCIBCLK_N
CLKOUT_CPUPCIBCLK_P
GPP_B5/SRCCLKREQ0*
GPP_B6/SRCCLKREQ1*
GPP_B7/SRCCLKREQ2*
GPP_B8/SRCCLKREQ3*
GPP_B9/SRCCLKREQ4*
GPP_B10/SRCCLKREQ5*
GPP_H0/SRCCLKREQ6*
GPP_H1/SRCCLKREQ7*
GPP_H2/SRCCLKREQ8*
GPP_H3/SRCCLKREQ9*
GPP_H4/SRCCLKREQ10*
GPP_H5/SRCCLKREQ11*
GPP_H6/SRCCLKREQ12*
GPP_H7/SRCCLKREQ13*
GPP_H8/SRCCLKREQ14*
GPP_H9/SRCCLKREQ15*
PP1V2_S3
R1238 470 1% 1/20W MF 201
R1239 0 5% 1/20W MF 0201
MEM_RESET_L
C1232 0.1UF 10% 6.3V CERM-X5R 0201 NOSTUFF
PCH_DRAM_RESET_L
PM_RSMRST_L
PCIE_WAKE_L
TP_PCH_GPP_A8
ESPI_RESET_L
TP_PCH_CLK32K_SUS
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
TP_PCH_SLP_A_L
PM_SLP_SUS_L
TP_PCH_SLP_LAN_L
PCH_LAN_WAKE_L
TP_PCH_LANPHYPC
TP_PCH_GPP_B2
PCH_GPP_A0_PU
ESPI_IO<0>
ESPI_IO<1>
ESPI_IO<2>
ESPI_IO<3>
ESPI_CS_L
PCH_SOC_SYNC
PCH_ESPI_ALERT0_L
PCH_STRP_GPD7
ESPI_CLK60M_R 22 1% 1/20W MF 201
ESPI_CLK
TP_PCH_GPP_A10
TP_PCH_GPP_A16
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
CPU_CLK100M_BCLK_N
CPU_CLK100M_BCLK_P
CPU_CLK24M_NSSC_CLK_N
CPU_CLK24M_NSSC_CLK_P
CPU_CLK100M_PCIBCLK_N
CPU_CLK100M_PCIBCLK_P
SOC_CLKREQ_L
PCH_WLAN_CLKREQ_L
GPU_CLKREQ_L
DEBUG_CLKREQ_L
TP_PCH_GPP_B9
TP_PCH_GPP_B10
TBT_X_CLKREQ_L
TBT_T_CLKREQ_L
TBT_W_CLKREQ_L
PCH_ENETSD_CLKREQ_L
TP_PCH_GPP_H4
TP_PCH_GPP_H5
TP_PCH_GPP_H6
TP_PCH_GPP_H7
TP_PCH_GPP_H8
TP_PCH_GPP_H9
PCH_CLK24M_XTALIN
PCH_CLK24M_XTALOUT
PCH_CLKIN_XTAL
PCH_XCLK_BIASREF
PCH_CLK32K_RTCX1
NC_PCH_CLK32K_RTCX2
PCH_INTRUDER_L
PCH_SRTCRST_L
PCH_RTCRST_L
PCH_RTC_RESET_L
PMU_CLK32K_PCH
PP3V0_G3H_RTC
R1205 20K 5% 1/20W MF 201
R1204 20K 5% 1/20W MF 201
R1201 1M 5% 1/20W MF 201
C1205 1UF 20% 6.3V X6S-CERM 0201
C1204 1UF 20% 6.3V X6S-CERM 0201
R1206 0 5% 1/20W MF 0201
R1208 0 5% 1/20W MF 0201
R1202 100K 5% 1/20W MF 201
R1203 127K 1% 1/20W MF 201
PLACE_NEAR=U1200.BA49:5MM
TP1200 PCH_GPP_A15
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PLT_RST_L
PM_RSMRST_L
TP1219 PCH_GPP_A13
PM_PWRBTN_L
SPIROM_USE_MLB
PM_BATLOW_L
PM_SLP_S0_L
TP1201 PCH_GPP_SLP_WLAN_L
TP1202 PCH_GPP_A11
TP1203 PCH_GPP_A12
TP1204
TP1205
TP1206
TP1207
TP1208
TP1209
TP1210
TP1211
TP1212
TP1213
TP1214
TP1215
TP1216
TP1217
TP1218
PCIE_CLK100M_SOC_N
PCIE_CLK100M_SOC_P
PCIE_CLK100M_WLAN_PCH_N
PCIE_CLK100M_WLAN_PCH_P
PCIE_CLK100M_TBT_X_N
PCIE_CLK100M_TBT_X_P
PCIE_CLK100M_TBT_T_N
PCIE_CLK100M_TBT_T_P
PCIE_CLK100M_ENET_PCH_N
PCIE_CLK100M_ENET_PCH_P
PP3V3_S5
PP1V8_S5
R1217 100K
R1248 100K
R1212 100K
R1211 100K NOSTUFF
R1213 100K
R1207 100K
R1251 100K
R1249 47K
R1250 47K
R1260 47K
R1261 47K
R1252 100K
R1253 100K
R1245 100K NOSTUFF
R1254 100K
R1230 100K
R1231 100K
R1232 100K
R1233 100K
R1237 100K NOSTUFF
R1218 100K
R1268 100K
R1267 10K
R1246 60.4 1%
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
PCH RTC/HDA/JTAG/SATA/CLK
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 12 OF 142
SHEET 12 OF 115
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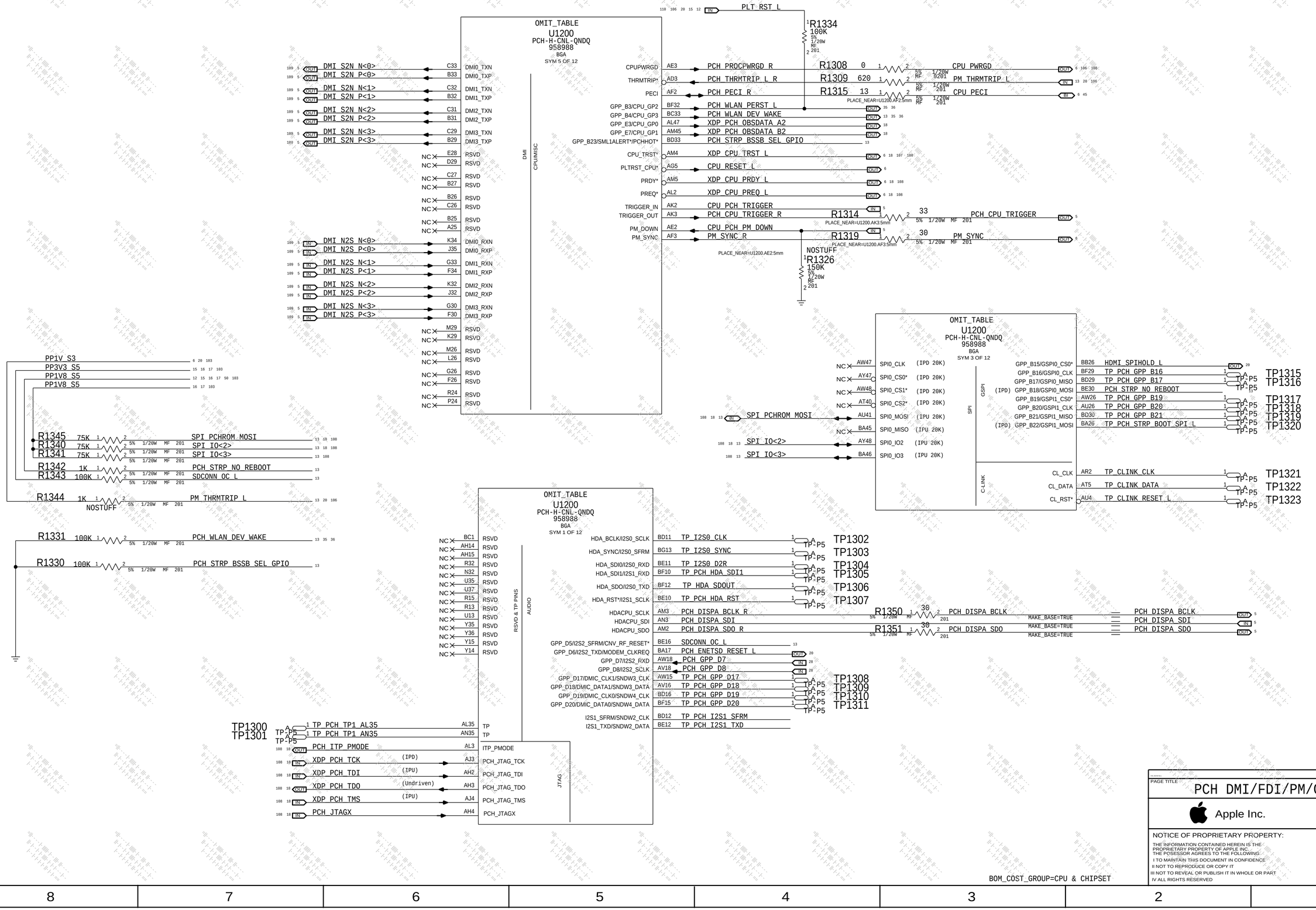
OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 5 OF 12
DMI
CPU/MISC
DMI S2N N<0>
DMI S2N P<0>
DMI S2N N<1>
DMI S2N P<1>
DMI S2N N<2>
DMI S2N P<2>
DMI S2N N<3>
DMI S2N P<3>
DMI N2S N<0>
DMI N2S P<0>
DMI N2S N<1>
DMI N2S P<1>
DMI N2S N<2>
DMI N2S P<2>
DMI N2S N<3>
DMI N2S P<3>
PLT_RST_L
R1334 100K
CPUPWRGD
THRMTRIP*
PECI
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B23/SML1ALERT*/PCHHOT*
CPU_TRST*
PLTRST_CPU*
PRDY*
PREQ*
TRIGGER_IN
TRIGGER_OUT
PM_DOWN
PM_SYNC
PCH PROCPWRGD R
PCH THRMTRIP L R
PCH PECI R
PCH WLAN PERST L
PCH WLAN DEV WAKE
XDP PCH OBSDATA A2
XDP PCH OBSDATA B2
PCH STRP BSSB SEL GPIO
XDP CPU TRST L
CPU RESET L
XDP CPU PRDY L
XDP CPU PREQ L
CPU PCH TRIGGER
PCH CPU TRIGGER R
CPU PCH PM DOWN
PM SYNC R
R1308 0
R1309 620
R1315 13
R1314 33
R1319 30
CPU PWRGD
PM THRMTRIP L
CPU PECI
PCH CPU TRIGGER
PM SYNC
NOSTUFF R1326 150K
PLACE_NEAR=U1200.AE2:5mm
PLACE_NEAR=U1200.AF2:5mm
PLACE_NEAR=U1200.AK3:5mm
PLACE_NEAR=U1200.AF3:5mm
OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 3 OF 12
SPI
GSPI
C-LINK
SPI PCHROM MOSI
SPI IO<2>
SPI IO<3>
SPI0_CLK
SPI0_CS0*
SPI0_CS1*
SPI0_CS2*
SPI0_MOSI
SPI0_MISO
SPI0_IO2
SPI0_IO3
GPP_B15/GSPI0_CS0*
GPP_B16/GSPI0_CLK
GPP_B17/GSPI0_MISO
GPP_B18/GSPI0_MOSI
GPP_B19/GSPI1_CS0*
GPP_B20/GSPI1_CLK
GPP_B21/GSPI1_MISO
GPP_B22/GSPI1_MOSI
HDMI SPIHOLD L
TP PCH GPP B16
TP PCH GPP B17
PCH STRP NO REBOOT
TP PCH GPP B19
TP PCH GPP B20
TP PCH GPP B21
TP PCH STRP BOOT SPI L
CL_CLK
CL_DATA
CL_RST*
TP CLINK CLK
TP CLINK DATA
TP CLINK RESET L
TP1315
TP1316
TP1317
TP1318
TP1319
TP1320
TP1321
TP1322
TP1323
PP1V S3
PP3V3 S5
PP1V8 S5
PP1V8 S5
R1345 75K SPI PCHROM MOSI
R1340 75K SPI IO<2>
R1341 75K SPI IO<3>
R1342 1K PCH STRP NO REBOOT
R1343 100K SDCONN OC L
R1344 1K PM THRMTRIP L
NOSTUFF
R1331 100K PCH WLAN DEV WAKE
R1330 100K PCH STRP BSSB SEL GPIO
OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 1 OF 12
RSVD & TP PINS
AUDIO
JTAG
HDA_BCLK/I2S0_SCLK
HDA_SYNC/I2S0_SFRM
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_SDO/I2S0_TXD
HDA_RST*/I2S1_SCLK
HDACPU_SCLK
HDACPU_SDI
HDACPU_SDO
GPP_D5/I2S2_SFRM/CNV_RF_RESET*
GPP_D6/I2S2_TXD/MODEM_CLKREQ
GPP_D7/I2S2_RXD
GPP_D8/I2S2_SCLK
GPP_D17/DMIC_CLK1/SNDW3_CLK
GPP_D18/DMIC_DATA1/SNDW3_DATA
GPP_D19/DMIC_CLK0/SNDW4_CLK
GPP_D20/DMIC_DATA0/SNDW4_DATA
I2S1_SFRM/SNDW2_CLK
I2S1_TXD/SNDW2_DATA
TP_I2S0_CLK
TP_I2S0_SYNC
TP_I2S0_D2R
TP_PCH_HDA_SDI1
TP_HDA_SDOUT
TP_PCH_HDA_RST
PCH_DISPA_BCLK R
PCH_DISPA_SDI
PCH_DISPA_SDO R
R1350 30
R1351 30
PCH_DISPA_BCLK
PCH_DISPA_SDI
PCH_DISPA_SDO
MAKE_BASE=TRUE
SDCONN_OC_L
PCH_ENETSD_RESET_L
PCH_GPP_D7
PCH_GPP_D8
TP_PCH_GPP_D17
TP_PCH_GPP_D18
TP_PCH_GPP_D19
TP_PCH_GPP_D20
TP1302
TP1303
TP1304
TP1305
TP1306
TP1307
TP1308
TP1309
TP1310
TP1311
TP1300
TP1301
TP_PCH_TP1_AL35
TP_PCH_TP1_AN35
PCH_ITP_PMODE
XDP_PCH_TCK (IPD)
XDP_PCH_TDI (IPU)
XDP_PCH_TDO (Undriven)
XDP_PCH_TMS (IPU)
PCH_JTAGX
ITP_PMODE
PCH_JTAG_TCK
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_JTAGX
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
PCH DMI/FDI/PM/GFX/PCI
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 13 OF 142
SHEET 13 OF 115
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CNL-H PDG indicates any USB3.1 ports can be used for DCI.

OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 7 OF 12

TP_USB3_EXT_DBG_D2R_N	D11	USB31_1_RXN	
TP_USB3_EXT_DBG_D2R_P	C11	USB31_1_RXP	
TP_USB3_EXT_DBG_R2D_C_N	F9	USB31_1_TXN	
TP_USB3_EXT_DBG_R2D_C_P	F7	USB31_1_TXP	
113 109 IN USB3_VITAMIN_D2R_N	B9	USB31_2_RXN	
113 109 IN USB3_VITAMIN_D2R_P	C9	USB31_2_RXP	
Connect to Vitamin-C Connector			
113 109 OUT USB3_VITAMIN_R2D_C_N	C3	USB31_2_TXN	
113 109 OUT USB3_VITAMIN_R2D_C_P	D4	USB31_2_TXP	
106 IN USB3_TEST_D2R_N	B10	USB31_3_RXN	
106 IN USB3_TEST_D2R_P	C10	USB31_3_RXP	
Connect to TP			
106 OUT USB3_TEST_R2D_N	F11	USB31_3_TXN	
106 OUT USB3_TEST_R2D_P	G12	USB31_3_TXP	
109 62 IN USB3_EXTA_D2R_N	K16	USB31_4_RXN	
109 62 IN USB3_EXTA_D2R_P	J15	USB31_4_RXP	
USB-A Connector A			
109 62 OUT USB3_EXTA_R2D_C_N	B14	USB31_4_TXN	
109 62 OUT USB3_EXTA_R2D_C_P	C14	USB31_4_TXP	
109 62 IN USB3_EXTB_D2R_N	J13	USB31_5_RXN	
109 62 IN USB3_EXTB_D2R_P	K13	USB31_5_RXP	
USB-A Connector B			
109 62 OUT USB3_EXTB_R2D_C_N	C15	USB31_5_TXN	
109 62 OUT USB3_EXTB_R2D_C_P	B15	USB31_5_TXP	
106 IN USB3_ENET_ADAPTOR_D2R_N	G14	USB31_6_RXN	
106 IN USB3_ENET_ADAPTOR_D2R_P	F14	USB31_6_RXP	
Connect to TP			
106 OUT USB3_ENET_ADAPTOR_R2D_N	C17	USB31_6_TXN	
106 OUT USB3_ENET_ADAPTOR_R2D_P	C16	USB31_6_TXP	

USB3 USB2

USB2N_1	J3	NC	
USB2P_1	J2	NC	
USB2N_2	N13	NC	
USB2P_2	N15	NC	
USB2N_3	K4	USB_TEST_N	BI 106
USB2P_3	K3	USB_TEST_P	BI 106
USB2N_4	M10	TP_USB_EXT_DBG_N	
USB2P_4	L9	TP_USB_EXT_DBG_P	
USB2N_5	M1	USB_DBG_XA_N	BI 28
USB2P_5	L2	USB_DBG_XA_P	BI 28
USB2N_6	K7	NC	
USB2P_6	K6	NC	
USB2N_7	L4	USB_UPC_TA_N	BI 95
USB2P_7	L3	USB_UPC_TA_P	BI 95
USB2N_8	G4	USB_EXTB_N	BI 62
USB2P_8	G5	USB_EXTB_P	BI 62
USB2N_9	M6	NC	
USB2P_9	N8	NC	
USB2N_10	H3	USB_VITAMIN_N	BI 113
USB2P_10	H2	USB_VITAMIN_P	BI 113
USB2N_11	R10	USB_UPC_TB_N	BI 96
USB2P_11	P9	USB_UPC_TB_P	BI 96
USB2N_12	G1	USB_UPC_XB_N	BI 30
USB2P_12	G2	USB_UPC_XB_P	BI 30
USB2N_13	N3	USB_ENET_ADAPTOR_N	BI 106
USB2P_13	N2	USB_ENET_ADAPTOR_P	BI 106
USB2N_14	E5	USB_EXTA_N	BI 62
USB2P_14	F6	USB_EXTA_P	BI 62

To DFU TPs
To DEBUG MUX2
To Ace TA
To ExtB USB-A
To Ace TB
To Ace XB
To DFU TPs
To ExtA USB-A

GPP_E9/USB2_OC0*	AH36	XDP_USB_EXTA_OC_L	IN 14 18 62
GPP_E10/USB2_OC1*	AL40	XDP_USB_EXTB_OC_L	IN 14 18 62
GPP_E11/USB2_OC2*	AJ44	XDP_USB_EXTC_OC_L	IN 14 18
GPP_E12/USB2_OC3*	AL41	XDP_USB_EXTD_OC_L	IN 14 18
GPP_F15/USB2_OC4*	AV47	USB_TA_OC_L	IN 14 94
GPP_F16/USB2_OC5*	AR35	USB_TB_OC_L	IN 14 94
GPP_F17/USB2_OC6*	AR37	USB_EXTG_OC_L	14
GPP_F18/USB2_OC7*	AV43	USB_EXTH_OC_L	14
USB2_COMP	F4	USB2_COMP	PLACE_NEAR=U1200.F4:10.0mm
USB2_ID	G3	USB2_ID	
USB2_VBUSSENSE	F3	USB2_VBUSSENSE	

R1410 1K 1% 1/20W MF 201
R1411 1K 1% 1/20W MF 201
R1470 113 1% 1/20W MF 201

PM_SLP_S3_L 12 26 80 92 100 106 110
PP3V3_S5 16 17 103

R1460	10K	5%	1/20W	MF	201	XDP_USB_EXTA_OC_L	14 18 62	
R1461	10K	5%	1/20W	MF	201	XDP_USB_EXTB_OC_L	14 18 62	
R1420	10K	5%	1/20W	MF	201	18 14 XDP_USB_EXTC_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTC_OC_L48
R1421	10K	5%	1/20W	MF	201	18 14 XDP_USB_EXTD_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTD_OC_L48
R1422	10K	5%	1/20W	MF	201	USB_TA_OC_L	14 94	
R1423	10K	5%	1/20W	MF	201	USB_TB_OC_L	14 94	
R1424	10K	5%	1/20W	MF	201	USB_EXTG_OC_L	14	
R1425	10K	5%	1/20W	MF	201	USB_EXTH_OC_L	14	
R1429	10K	5%	1/20W	MF	201	XDP_JTAG_ISP_TDO	14 18 94	

R1474	100K	5%	1/20W	MF	201	TBT_X_CIO_PWR_EN	14 26 28 29 30
R1471	100K	5%	1/20W	MF	201	TBT_X_USB_PWR_EN	14 26 28 29 30
R1472	100K	5%	1/20W	MF	201	TBT_T_CIO_PWR_EN	14 92 94 95 96
R1473	100K	5%	1/20W	MF	201	TBT_T_USB_PWR_EN	14 92 94 95 96
R1431	100K	5%	1/20W	MF	201	TBT_X_PLUG_EVENT_L	14 26 28
R1432	100K	5%	1/20W	MF	201	TBT_T_PLUG_EVENT_L	14 92 94
R1463	100K	5%	1/20W	MF	201	XDP_JTAG_ISP_TDI	14 18 94
R1464	100K	5%	1/20W	MF	201	BTI2SMUX_SEL_PCH	14
R1465	100K	5%	1/20W	MF	201	XDP_JTAG_ISP_TCK	14 18 94

PLACE_NEAR=U1200.A13:2mm
R1400 100 1% 1/20W MF 201

OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 8 OF 12
PCIE/SATA/USB3

NC	F20	PCIE5_RXN	
NC	G20	PCIE5_RXP	
NC	B21	PCIE5_TXN	
NC	A22	PCIE5_TXP	
NC	K21	PCIE6_RXN	
NC	J21	PCIE6_RXP	
NC	D21	PCIE6_TXN	
NC	C21	PCIE6_TXP	
NC	L24	PCIE7_RXN	
NC	J24	PCIE7_RXP	
NC	C23	PCIE7_TXN	
NC	B23	PCIE7_TXP	
NC	F24	PCIE8_RXN	
NC	G24	PCIE8_RXP	
NC	B24	PCIE8_TXN	
NC	C24	PCIE8_TXP	
NC	G36	PCIE9_RXN	
NC	F36	PCIE9_RXP	
NC	C34	PCIE9_TXN	
NC	D34	PCIE9_TXP	
NC	K37	PCIE10_RXN	
NC	J37	PCIE10_RXP	
NC	C35	PCIE10_TXN	
NC	B35	PCIE10_TXP	
NC	T43	PCIE21_RXN	
NC	R44	PCIE21_RXP	
NC	G47	PCIE21_TXN	
NC	F46	PCIE21_TXP	
NC	U40	PCIE22_RXN	
NC	U41	PCIE22_RXP	
NC	H47	PCIE22_TXN	
NC	H48	PCIE22_TXP	
NC	W43	PCIE23_RXN	
NC	W44	PCIE23_RXP	
NC	G49	PCIE23_TXN	
NC	G48	PCIE23_TXP	
NC	Y40	PCIE24_RXN	
NC	Y41	PCIE24_RXP	
NC	G46	PCIE24_TXN	
NC	G45	PCIE24_TXP	

PCIE11_RXN/SATA0A_RXN	G38	NC	
PCIE11_RXP/SATA0A_RXP	F39	NC	
PCIE11_TXN/SATA0A_TXN	B36	NC	
PCIE11_TXP/SATA0A_TXP	C36	NC	
PCIE12_RXN/SATA1A_RXN	H42	NC	
PCIE12_RXP/SATA_1A_RXP	J41	NC	
PCIE12_TXN/SATA1A_TXN	D38	NC	
PCIE12_TXP/SATA1A_TXP	E37	NC	
PCIE13_RXN/SATA0B_RXN	C45	NC	
PCIE13_RXP/SATA0B_RXP	C46	NC	
PCIE13_TXN/SATA0B_TXN	B38	NC	
PCIE13_TXP/SATA0B_TXP	C38	NC	
PCIE14_RXN/SATA1B_RXN	D46	NC	
PCIE14_RXP/SATA1B_RXP	C47	NC	
PCIE14_TXN/SATA1B_TXN	C39	NC	
PCIE14_TXP/SATA1B_TXP	D39	NC	
PCIE15_RXN/SATA2_RXN	F44	NC	
PCIE15_RXP/SATA2_RXP	E45	NC	
PCIE15_TXN/SATA2_TXN	B40	NC	
PCIE15_TXP/SATA2_TXP	C40	NC	
PCIE16_RXN/SATA3_RXN	L41	NC	
PCIE16_RXP/SATA3_RXP	M40	NC	
PCIE16_TXN/SATA3_TXN	B41	NC	
PCIE16_TXP/SATA3_TXP	C41	NC	
PCIE17_RXN/SATA4_RXN	K43	PCIE_SOC_D2R_N<0>	IN 40 109
PCIE17_RXP/SATA4_RXP	K44	PCIE_SOC_D2R_P<0>	IN 40 109
PCIE17_TXN/SATA4_TXN	A42	PCIE_SOC_R2D_C_N<0>	OUT 46 109
PCIE17_TXP/SATA4_TXP	B42	PCIE_SOC_R2D_C_P<0>	OUT 46 109
PCIE18_RXN/SATA5_RXN	P41	PCIE_SOC_D2R_N<1>	IN 40 109
PCIE18_RXP/SATA5_RXP	R40	PCIE_SOC_D2R_P<1>	IN 40 109
PCIE18_TXN/SATA5_TXN	C42	PCIE_SOC_R2D_C_N<1>	OUT 46 109
PCIE18_TXP/SATA5_TXP	D42	PCIE_SOC_R2D_C_P<1>	OUT 46 109
PCIE19_RXN/SATA6_RXN	M44	PCIE_SOC_D2R_N<2>	IN 40 109
PCIE19_RXP/SATA6_RXP	N42	PCIE_SOC_D2R_P<2>	IN 40 109
PCIE19_TXN/SATA6_TXN	C44	PCIE_SOC_R2D_C_N<2>	OUT 46 109
PCIE19_TXP/SATA6_TXP	D43	PCIE_SOC_R2D_C_P<2>	OUT 46 109
PCIE20_RXN/SATA7_RXN	R35	PCIE_SOC_D2R_N<3>	IN 40 109
PCIE20_RXP/SATA7_RXP	R37	PCIE_SOC_D2R_P<3>	IN 40 109
PCIE20_TXN/SATA7_TXN	A44	PCIE_SOC_R2D_C_N<3>	OUT 46 109
PCIE20_TXP/SATA7_TXP	B44	PCIE_SOC_R2D_C_P<3>	OUT 46 109

109 28 IN PCIE_WLANPCH_D2R_N	G17	PCIE1_RXN/USB31_7_RXN	
109 28 IN PCIE_WLANPCH_D2R_P	F16	PCIE1_RXP/USB31_7_RXP	
109 28 OUT PCIE_WLANPCH_R2D_C_N	A17	PCIE1_TXN/USB31_7_TXN	
109 28 OUT PCIE_WLANPCH_R2D_C_P	B17	PCIE1_TXP/USB31_7_TXP	
109 84 IN PCIE_ENET_PCH_D2R_N	R21	PCIE2_RXN/USB31_8_RXN	
109 84 IN PCIE_ENET_PCH_D2R_P	P21	PCIE2_RXP/USB31_8_RXP	
109 84 OUT PCIE_ENET_PCH_R2D_C_N	B18	PCIE2_TXN/USB31_8_TXN	
109 84 OUT PCIE_ENET_PCH_R2D_C_P	C18	PCIE2_TXP/USB31_8_TXP	
NC	K18	PCIE3_RXN/USB31_9_RXN	
NC	J18	PCIE3_RXP/USB31_9_RXP	
NC	B19	PCIE3_TXN/USB31_9_TXN	
NC	C19	PCIE3_TXP/USB31_9_TXP	
NC	N18	PCIE4_RXN/USB31_10_RXN	
NC	R18	PCIE4_RXP/USB31_10_RXP	
NC	D20	PCIE4_TXN/USB31_10_TXN	
NC	C20	PCIE4_TXP/USB31_10_TXP	

GPP_E4/SATA_DEVSLP0	AL48	XDP_PCH_OBSDATA_A3	BI 18
GPP_E5/SATA_DEVSLP1	AH35	XDP_PCH_OBSDATA_B0	BI 18
GPP_E6/SATA_DEVSLP2	AH40	XDP_PCH_OBSDATA_B1	BI 18
GPP_F5/SATA_DEVSLP3	AP48	TBT_X_PCI_RESET_L	OUT 20 26 28
GPP_F6/SATA_DEVSLP4	AR47	TBT_T_PCI_RESET_L	OUT 20 92 94
GPP_F7/SATA_DEVSLP5	AN46	TBT_X_CIO_PWR_EN	OUT 14 26 28 29 30
GPP_F8/SATA_DEVSLP6	AN37	TBT_X_USB_PWR_EN	OUT 14 26 28 29 30
GPP_F9/SATA_DEVSLP7	AP47	TBT_T_CIO_PWR_EN	OUT 14 92 94 95 96
GPP_E8/SATALED*	AK48	XDP_PCH_OBSDATA_B3	OUT 18

18 BI XDP_PCH_OBSFN_C0	AH41	GPP_E0/SATAXPCIE0/SATAGP0	
18 BI XDP_PCH_OBSDATA_A0	AJ43	GPP_E1/SATAXPCIE1/SATAGP1	
18 BI XDP_PCH_OBSDATA_A1	AK47	GPP_E2/SATAXPCIE2/SATAGP2	
18 BI XDP_PCH_OBSDATA_D0	AN47	GPP_F0/SATAXPCIE3/SATAGP3	
18 BI XDP_PCH_OBSDATA_D1	AM46	GPP_F1/SATAXPCIE4/SATAGP4	
94 18 14 OUT XDP_JTAG_ISP_TCK	AM43	GPP_F2/SATAXPCIE5/SATAGP5	
94 18 14 IN XDP_JTAG_ISP_TDI	AM47	GPP_F3/SATAXPCIE6/SATAGP6	
94 18 14 OUT XDP_JTAG_ISP_TDO	AM48	GPP_F4/SATAXPCIE7/SATAGP7	
96 95 94 92 14 OUT TBT_T_USB_PWR_EN	AR42	GPP_F10/SATA_SCLOCK	
28 26 14 IN TBT_X_PLUG_EVENT_L	AR48	GPP_F11/SATA_SLOAD	
94 92 14 IN TBT_T_PLUG_EVENT_L	AU46	GPP_F12/SATA_SDATAOUT1	
14 BTI2SMUX_SEL_PCH	AU47	GPP_F13/SATA_SDATAOUT0	
PCH_PCIE_RCOMPP	A13	PCIE_RCOMPP	
PCH_PCIE_RCOMPN	B12	PCIE_RCOMPN	

CNV

CNV_WR_CLKN	BD4	NC	
CNV_WR_CLKP	BE3	NC	
CNV_WT_CLKN	BC5	NC	
CNV_WT_CLKP	BB6	NC	
CNV_WR_D0N	BB3	NC	
CNV_WR_D0P	BB4	NC	
CNV_WT_D0N	BE6	NC	
CNV_WT_D0P	BD7	NC	
CNV_WR_D1N	BA3	NC	
CNV_WR_D1P	BA2	NC	
CNV_WT_D1N	BG6	NC	
CNV_WT_D1P	BF6	NC	
CNV_WT_RCOMP	BA1		

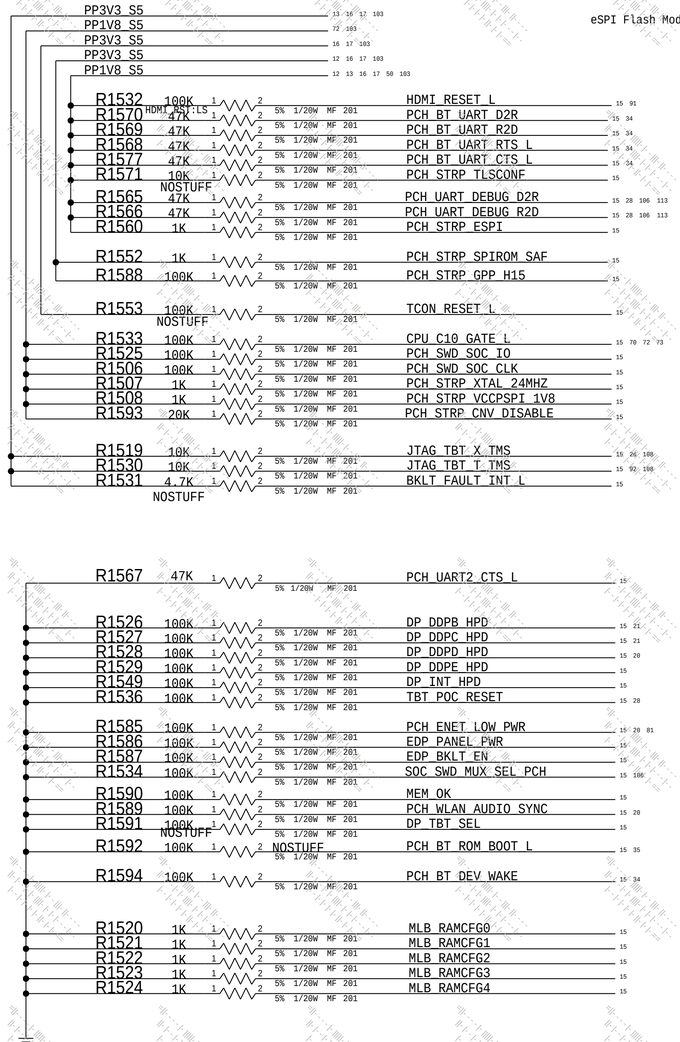
CNV_WT_RCOMP
PLACE_NEAR=U1200.BA1:2mm
NOSTUFF R1401 150 1% 1/20W MF 201

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: PCH PCI-E/USB

Apple Inc.

DRAWING NUMBER	051-02424
SIZE	D
REVISION	6.0.0
BRANCH	dvt-1
PAGE	14 OF 142
SHEET	14 OF 115

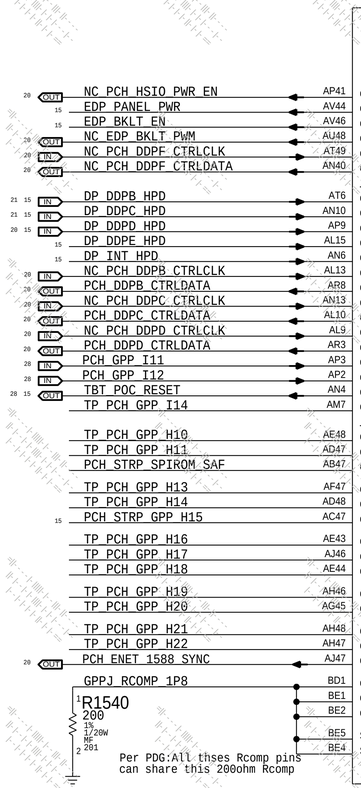


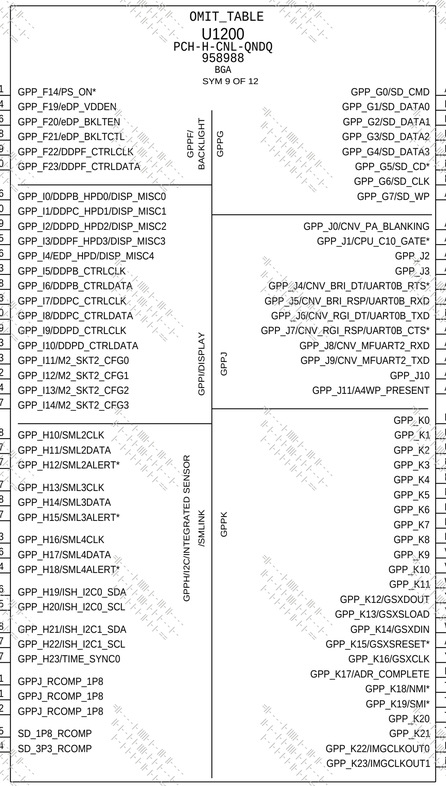
eSPI Flash Mode:0=MAF(not supported),1=SAF

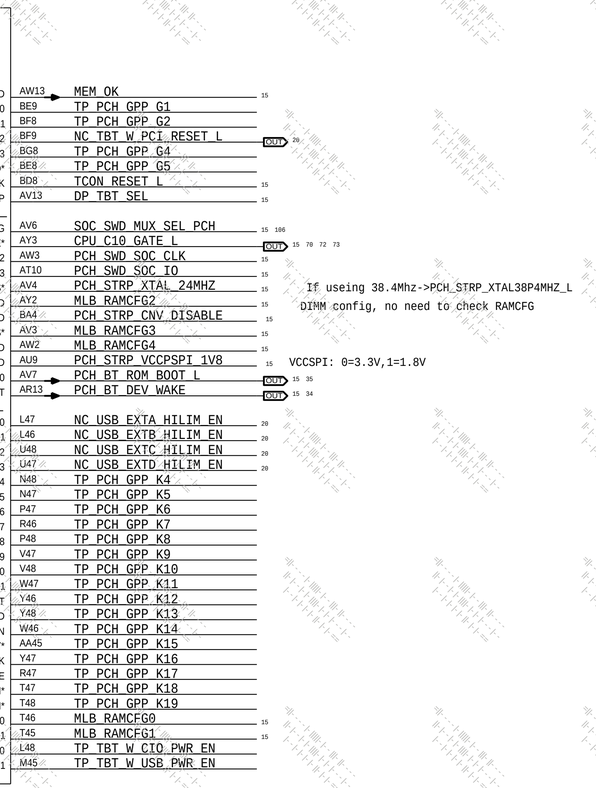
SAF System: Unused

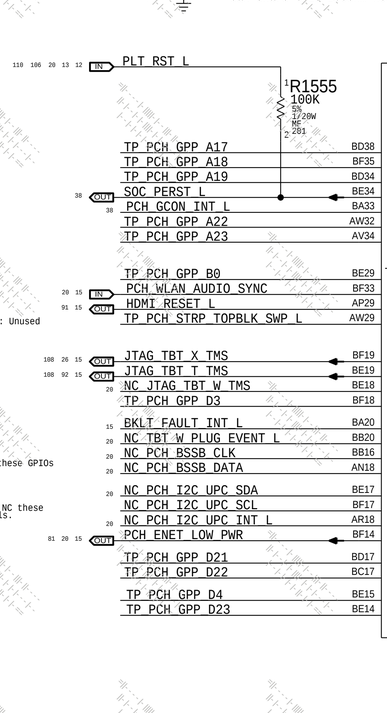
BSSB on USB-SS,NC these GPIOs

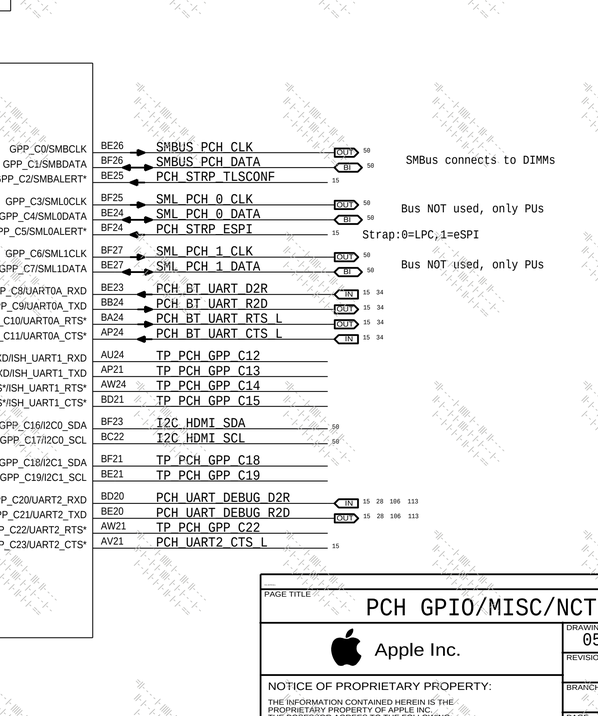
TBT_USB-C ports, NC these NO-TBT I2C signals.











SMBus connects to DIMMs

Bus NOT used, only PUs

Strap:0=LPC,1=eSPI

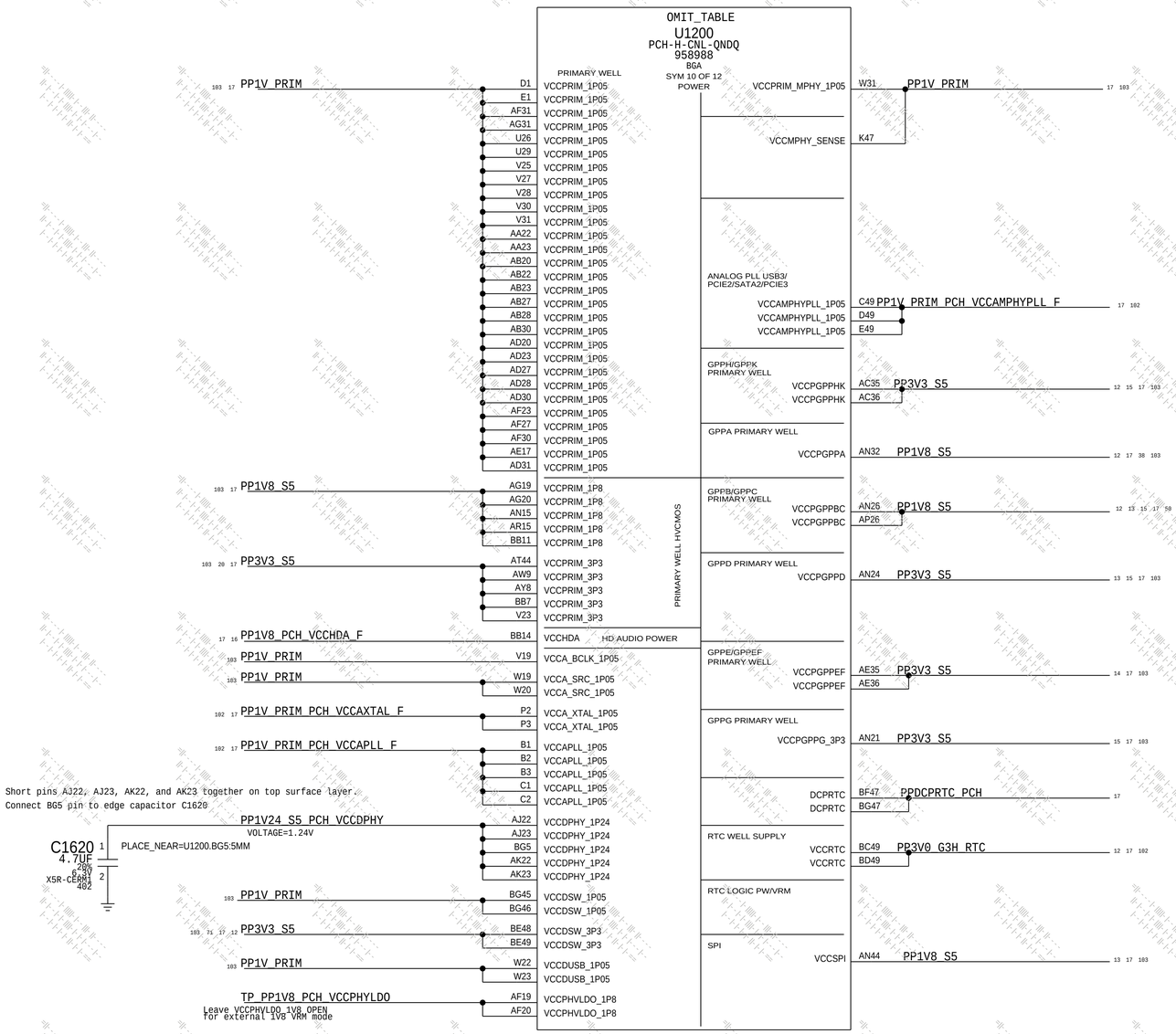
Bus NOT used, only PUs

If useing 38.4Mhz->PCH_STRP_XTAL38P4MHZ_L
DIMM config, no need to check RAMCFG

VCCSPI: 0=3.3V,1=1.8V

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	PCH GPIO/MISC/NCTF
Apple Inc.	DRAWING NUMBER 051-02424
	SIZE D
	REVISION 6.0.0
	BRANCH dvt-1
	PAGE 15 OF 142
	SHEET 15 OF 115



Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: PCH Power

Apple Inc.

DRAWING NUMBER: 051-02424

SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 16 OF 142

SHEET: 16 OF 115

1000PF CAPS ARE INTEL PLACEHOLDERS & ALL PLACENEAR NEED TO BE UPDATED

PLACE_NEAR=U1200.AF31:3MM
PP1V PRIM
C1743 1UF 10% 6.3V CERM 402
C1750 12PF 5% 50V NP0-C0G 0201
PLACE_NEAR=U1200.U26:5MM
C1730 0.1UF 10% 16V X5R-CERM 0201
C1731 0.1UF 10% 16V X5R-CERM 0201
C1732 0.1UF 10% 16V X5R-CERM 0201
C76 0.1UF 10% 16V X5R-CERM 0201
C1700 22UF 20% 6.3V X5R-CERM-1 603
C1701 1UF 10% 6.3V CERM 402

PLACE_NEAR=U1200.AA23:1.4MM
PP1V PRIM
C1751 12PF 5% 50V NP0-C0G 0201
C1736 47UF 20% 6.3V POLY-TANT 0805
PLACE_NEAR=U1200.AD31:2.1MM
C1737 1UF 20% 6.3V X6S-CERM 0201
C1734 0.1UF 10% 16V X5R-CERM 0201
C1735 0.1UF 10% 16V X5R-CERM 0201
C1738 1UF 20% 6.3V X6S-CERM 0201
PLACE_NEAR=U1200.AF31:1MM
C1702 1UF 20% 6.3V X6S-CERM 0201

PP1V PRIM
PLACE_NEAR=U1200.AF23:1MM
C1739 0.1UF 10% 16V X5R-CERM 0201
PLACE_NEAR=U1200.V25:1MM
C1703 1UF 20% 6.3V X6S-CERM 0201

PPDCPRTC_PCH
VOLTAGE=2.0V
PLACE_NEAR=U1200.BF47:3MM
C1709 0.1UF 10% 16V X5R-CERM 0201

PLACE_NEAR=U1200.BC49:1MM
PP3V0_G3H_RTC
NOSTUFF C1745 1UF 20% 6.3V X6S-CERM 0201
PLACE_NEAR=U1200.BC49:1MM
NOSTUFF C1715 0.1UF 10% 16V X5R-CERM 0201

Change 1V8_S0_PCH_VCCHDA to 1V8_PCH_VCCHDA_F
Because PCH is using 1V8_PRIM instead of 1V8_S0.
PP1V8_PCH_VCCHDA_F
PLACE_NEAR=U1200.BB14:1.2MM
PLACE_NEAR=U1200.BB14:1.2MM
C1749 0.1UF 10% 16V X5R-CERM 0201
C1748 22UF 20% 6.3V X5R-CERM-1 603
C1717 1UF 20% 6.3V X6S-CERM 0201

PP3V3_S5
PLACE_NEAR=U1200.BB7:3MM
C1744 47UF 20% 6.3V POLY-TANT 0805
C1752 12PF 5% 50V NP0-C0G 0201
C1719 1UF 20% 6.3V X6S-CERM 0201
C1720 0.1UF 10% 16V X5R-CERM 0201
PLACE_NEAR=U1200.AY8:3MM

PP3V3_S5
PLACE_NEAR=U1200.BE49:1MM
C1753 12PF 5% 50V NP0-C0G 0201
C1723 1UF 20% 6.3V X6S-CERM 0201
C1724 0.1UF 10% 16V X5R-CERM 0201
PLACE_NEAR=U1200.BE48:1MM

PP1V8_S5
PLACE_NEAR=U1200.AN44:1MM
C1757 0.1UF 10% 16V X5R-CERM 0201

PP1V8_S5
PLACE_NEAR=U1200.AG19:3MM
C1762 1UF 20% 6.3V X6S-CERM 0201

PP1V PRIM
PLACE_NEAR=U1200.AB30:1MM
C1708 1UF 20% 6.3V X6S-CERM 0201

PP1V8_S5
PLACE_NEAR=U1200.AN26:1MM
C1710 0.1UF 10% 16V X5R-CERM 0201

PP3V3_S5
PLACE_NEAR=U1200.AE35:1MM
C1713 0.1UF 10% 16V X5R-CERM 0201

PP1V8_S5
PLACE_NEAR=U1200.AN32:1MM
C1746 0.1UF 10% 16V X5R-CERM 0201

PP3V3_S5
PLACE_NEAR=U1200.AC35:1MM
C1733 0.1UF 10% 16V X5R-CERM 0201

PP3V3_S5
PLACE_NEAR=U1200.AN21:3MM
C1747 22UF 20% 6.3V X5R-CERM-1 603
PLACE_NEAR=U1200.AN21:3MM
C1714 0.1UF 10% 16V X5R-CERM 0201

PP3V3_S5
PLACE_NEAR=U1200.AN24:3MM
C1716 0.1UF 10% 16V X5R-CERM 0201

PP3V3_S5
PLACE_NEAR=U1200.BE49:3MM
C1718 1UF 20% 6.3V X6S-CERM 0201

PP3V0_G3H_RTC
PLACE_NEAR=U1200.BD49:3MM
C1721 1UF 20% 6.3V X6S-CERM 0201
PLACE_NEAR=U1200.BD49:3MM
C1722 0.1UF 10% 16V X5R-CERM 0201

RAIL SIDE
PCH SIDE

PP1V PRIM
C1754 12PF 5% 50V NP0-C0G 0201
L1700 2.2UH-20%-0.19A-0.221OHM 0603
PLACE_NEAR=U1200.C49:5MM
PLACE_NEAR=U1200.D49:3MM
PLACE_NEAR=U1200.E49:3MM
PP1V PRIM PCH VCCAMPHYPLL F
PLACE_NEAR=U1200.C49:3MM
C1704 22UF 20% 6.3V X5R-CERM 0603-1
C1740 0.1UF 10% 16V X5R-CERM 0201
C1705 1UF 20% 6.3V X6S-CERM 0201

PP1V PRIM
C1755 12PF 5% 50V NP0-C0G 0201
L1701 2.2UH-20%-0.19A-0.221OHM 0603
PLACE_NEAR=U1200.P2:1MM
PLACE_NEAR=U1200.P2:1MM
C1706 22UF 20% 6.3V X5R-CERM 0603-1
PLACE_NEAR=U1200.P2:1MM
C1741 0.1UF 10% 16V X5R-CERM 0201
C1707 1UF 20% 6.3V X6S-CERM 0201
PP1V PRIM PCH VCCAXTAL F
PLACE_NEAR=U1200.P3:1MM
PLACE_NEAR=U1200.B3:5MM

PP1V PRIM
C1756 3.0PF +/-0.1PF 50V NP0-C0G 0201
L1702 2.2UH-20%-0.19A-0.221OHM 0603
PLACE_NEAR=U1200.B1:5MM
PLACE_NEAR=U1200.B1:5MM
C1711 22UF 20% 6.3V X5R-CERM 0603-1
PLACE_NEAR=U1200.C2:5MM
C1742 0.1UF 10% 16V X5R-CERM 0201
C1712 1UF 20% 6.3V X6S-CERM 0201
PP1V PRIM PCH VCCAPLL F

Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
PCH Decoupling
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 17 OF 142
SHEET 17 OF 115

Primary / Merged (CPU/PCH) Micro2-XDP

Extra BPM Testpoints

XDP_BPM_L<0> → TP1800
XDP_BPM_L<1> → TP1801
XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
(TP-P6)

PP1V_PRIM

PULL CFG<3> LOW WHEN XDP PRESENT
PLACE_NEAR=U0500.BN28:2.54MM
XDP:YES R1801 1K 5% 1/20W MF 201 NO_XNET_CONNECTION

XDP_PRESENT_CPU

XDP_CONN J1800
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_CONN			
XDP_PIN_1			
OBSFN_A0	XDP_CPU_PREQ_L	OBSFN_C0	CPU_CFG<17>
OBSFN_A1	XDP_CPU_PRDY_L	OBSFN_C1	CPU_CFG<16>
OBSDATA_A0	CPU_CFG<0>	OBSDATA_C0	CPU_CFG<8>
OBSDATA_A1	CPU_CFG<1>	OBSDATA_C1	CPU_CFG<9>
OBSDATA_A2	CPU_CFG<2>	OBSDATA_C2	CPU_CFG<10>
OBSDATA_A3	CPU_CFG<3>	OBSDATA_C3	CPU_CFG<11>
OBSFN_B0	NC	OBSFN_D0	CPU_CFG<19>
OBSFN_B1	NC	OBSFN_D1	CPU_CFG<18>
OBSDATA_B0	CPU_CFG<4>	OBSDATA_D0	CPU_CFG<12>
OBSDATA_B1	CPU_CFG<5>	OBSDATA_D1	CPU_CFG<13>
OBSDATA_B2	CPU_CFG<6>	OBSDATA_D2	CPU_CFG<14>
OBSDATA_B3	CPU_CFG<7>	OBSDATA_D3	CPU_CFG<15>
HOOK0	XDP_PM_RSMRST_L	ITPCLK/HOOK4	ITPXDP_CLK100M_P
HOOK1	XDP_CPU_PWRBTN_L	ITPCLK#/HOOK5	ITPXDP_CLK100M_N
VCC_OBS_AB		VCC_OBS_CD	
HOOK2	NC	RESET#/HOOK6	PCH_ITP_PMODE
HOOK3		DBR#/HOOK7	XDP_DBRESET_L
SDA	NC	TDO	
SCL	NC	TRSTn	
TCK1		TDI	
TCK0		TMS	
		XDP_PRESENT#	

518S0847

XDP:YES C1804 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.42:28MM
XDP:YES C1800 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.44:28MM
XDP:YES C1801 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.43:28MM
XDP:YES C1806 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.47:28MM

PP1V8_S5 — PLACE_NEAR=J1800.48:2.54MM
XDP:YES R1804 1K 5% 1/20W MF 201

PM_RSMRST_L — R1800 1K — PLACE_NEAR=U1200.AW41:3.8MM
PM_PWRBTN_L — R1802 10 — PLACE_NEAR=U1200.BE46:3MM
SPI_PCHROM_MOSI — R1803 1K — PLACE_NEAR=U1200.AU41:3MM
XDP:YES 1/20W MF 201

XDP_PCH_TCK — R1836 0 — PLACE_NEAR=J1800.56:2.54MM
XDP_CPU_TCK
PCH_JTAGX — R1835 0 — PLACE_NEAR=J1800.58:2.3MM
XDP:YES 5% 1/20W MF 0201

XDP_PM_RSMRST_L
XDP_CPU_PWRBTN_L
SPI_MOSI_R_CONN
XDP_PCH_TCK_R

PP1V_S0SW

XDP_PCH_TDO	R1890 100	PLACE_NEAR=U1200.AH3:28MM
XDP_PCH_TDI	R1891 51	PLACE_NEAR=U1200.AH2:28MM
XDP_PCH_TMS	R1892 51	PLACE_NEAR=U1200.AJ4:28MM
XDP_CPU_TDO	R1810 100	PLACE_NEAR=U0500.BT28:28MM
XDP_CPU_TCK	R1813 51	PLACE_NEAR=U0500.BR28:28MM
XDP_PCH_TCK	R1897 51	PLACE_NEAR=U1200.AJ3:28MM
XDP_PCH_TRST_L	R1898 51	PROPER WAY TO TERMINATE?

XDP:YES 5% 1/20W MF 201
NOSTUFF

R1830 1K 5% 1/20W MF 201 — R1830 = 2.2K??? — PLACE_NEAR=U0500.EB1:2.54MM???

XDP:YES R1806 0 5% 1/20W MF 0201 — PM_SYSRST_L

ROUTE IN STAR TOPOLOGY FROM XDP CONNECTOR.

XDP_CPU_TDO	R1821 0	PLACE_NEAR=J1800.51:2.54MM
XDP_CPU_TRST_L	R1822 0	PLACE_NEAR=J1800.53:2.54MM
XDP_CPU_TDI	R1823 0	PLACE_NEAR=J1800.55:2.54MM
XDP_CPU_TMS	R1824 0	PLACE_NEAR=J1800.57:2.54MM

XDP:YES 5% 1/20W MF 0201

XDP_PCH_TDO
XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS

PP1V8_S5 — PLACE_NEAR=J1800.46:28MM
XDP:YES R1850 100K 5% 1/20W MF 201

XDP:YES C1830 0.1UF 10% 10V X5R-CERM 0201

U1830 74AUP1G07GF SOT891 (OD)
VCC GND A Y NC NC NC NC

SPI_IO2_STRAP_L — PLACE_NEAR=U1830.4:7.54MM — R1831 1.5K MF — SPI_IO<2> (STRAP TO PCH)
XDP:YES NO_XNET_CONNECTION
PLACE_NEAR=U1830.4:2.54MM — R1832 49.9 1% 1/20W MF 201 NOSTUFF
NO_XNET_CONNECTION
XDP_PRESENT_L

NEED TO CONNECT TO VCCST, *STG POWER LOGIC

PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

PCH/XDP Signals

XDP_PCH_OBSDATA_A2	TP1870
XDP_PCH_OBSDATA_A3	TP1871
XDP_PCH_OBSDATA_B0	TP1872
XDP_USB_EXTA_OC_L	TP1873
XDP_USB_EXTB_OC_L	TP1874
XDP_USB_EXTC_OC_L	TP1875
XDP_USB_EXTD_OC_L	TP1876
XDP_PCH_OBSDATA_D0	TP1877
XDP_PCH_OBSDATA_D1	TP1878
XDP_JTAG_ISP_TCK	TP1879
XDP_JTAG_ISP_TDI	TP1880
XDP_PCH_OBSFN_C0	TP1882
XDP_PCH_OBSDATA_A0	TP1883
XDP_PCH_OBSDATA_A1	TP1884
XDP_PCH_OBSDATA_B1	TP1885
XDP_PCH_OBSDATA_B2	TP1863
XDP_PCH_OBSDATA_B3	TP1887
XDP_JTAG_ISP_TDO	TP1888

(TP-P6)

Non-XDP Signals

XDP_USB_EXTA_OC_L	XDP_USB_EXTA_OC_L	MAKE_BASE=TRUE
XDP_USB_EXTB_OC_L	XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE
XDP_USB_EXTC_OC_L	XDP_USB_EXTC_OC_L	MAKE_BASE=TRUE
XDP_USB_EXTD_OC_L	XDP_USB_EXTD_OC_L	MAKE_BASE=TRUE
XDP_JTAG_ISP_TCK	XDP_JTAG_ISP_TCK	MAKE_BASE=TRUE
XDP_JTAG_ISP_TDI	XDP_JTAG_ISP_TDI	MAKE_BASE=TRUE

Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

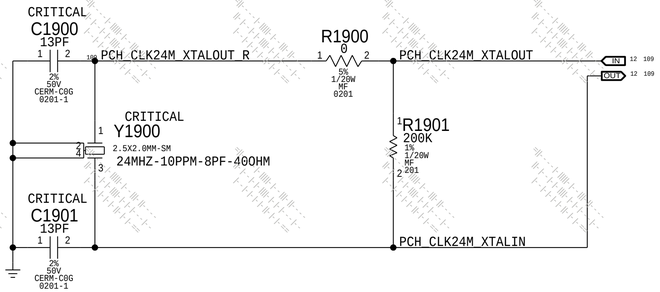
BOM_COST_GROUP=DEBUG

DESIGN: X502/MLB
LAST CHANGE: Mon Jun 15 22:04:28 2015
PAGE TITLE: CPU/PCH Merged XDP

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 18 OF 142
SHEET 18 OF 115

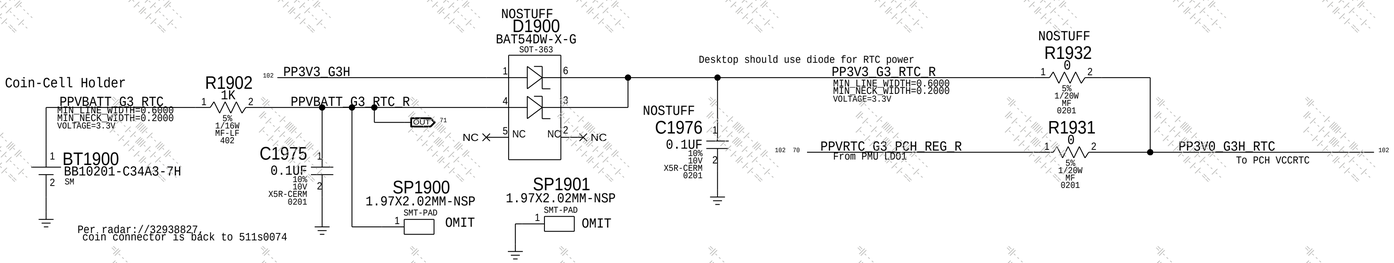
PCH 24MHz Crystal

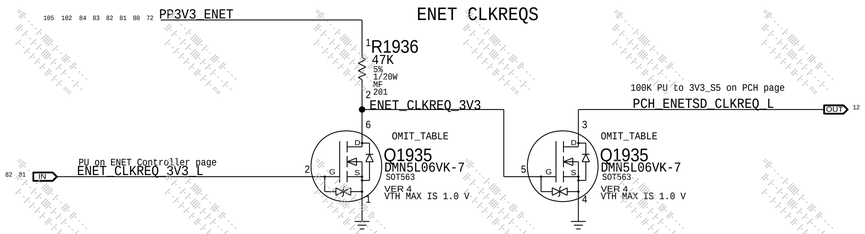


CL (load capacitance) = 8pF
Cs (trace capacitance) = 1pF (assumption)
Ci (package capacitance) = 0.5pF (assumption)
Ce = 2 * (CL - Cs - Ci) = 2 * (8 - 1 -0.5) = 13pF

PDG recommends 18pF,check in charz.

RTC Power Sources





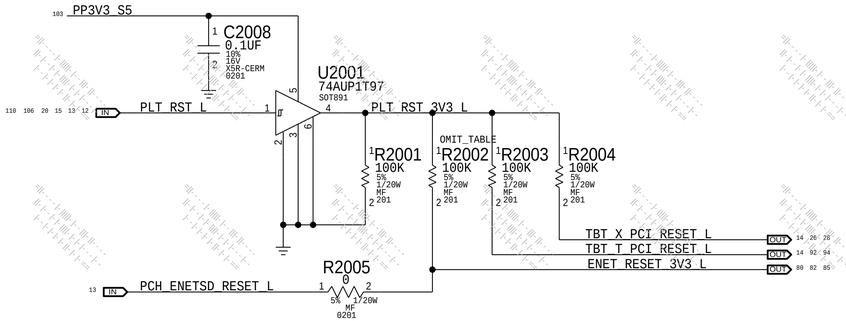
BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: Chipset Support 1

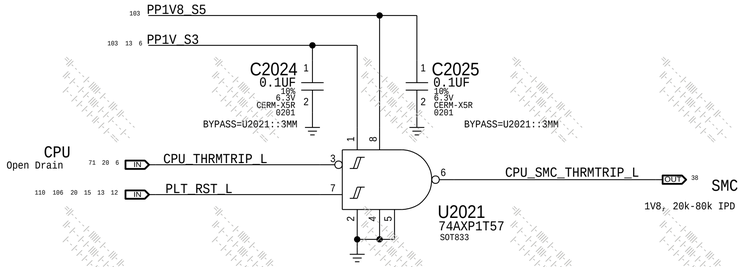
Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 19 OF 142
SHEET: 19 OF 115

Platform Reset Level Shifter

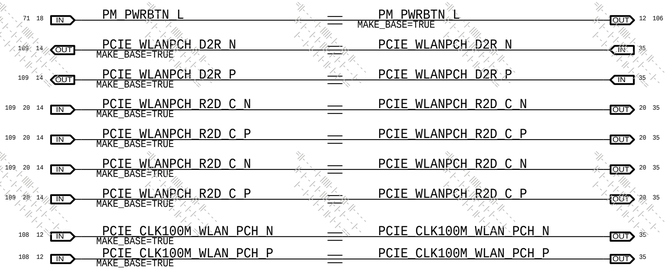


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES, 100K	R2002		ENET:10G
117S0006	1	RES, 1K	R2002		ENET:1G

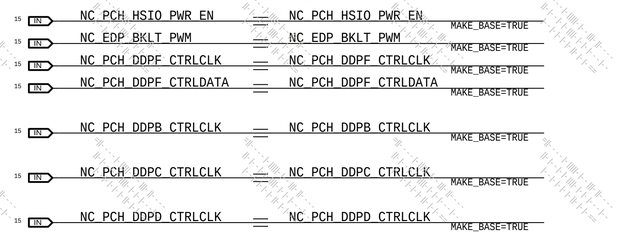


PMU response will be overridden by SMC, unless SMC and/or PCH is hung.

Misc Alias

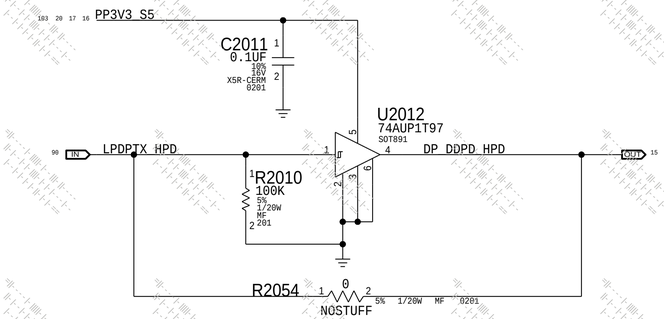


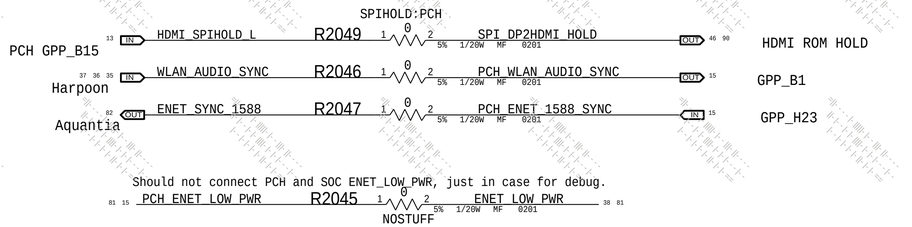
PCH NC Pins



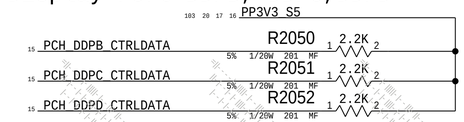
PCH THRMTRIP connection

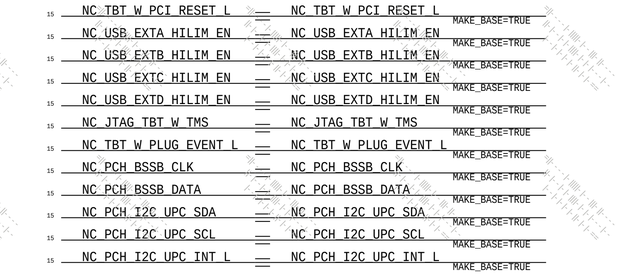
HDMI HPD





Display Port DDPB, DDPC,DDPD



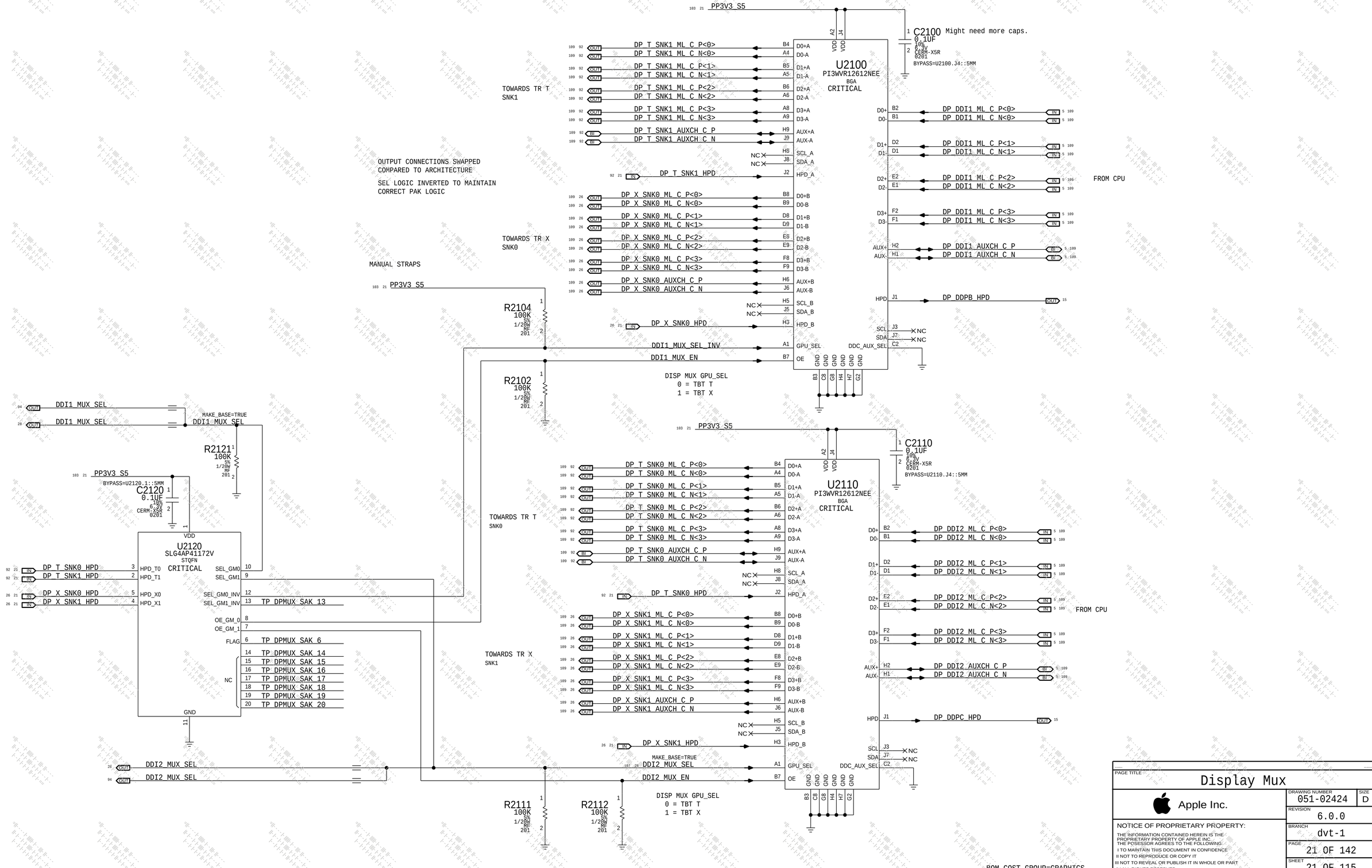


BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: Chipset Support 2

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 20 OF 142
SHEET: 20 OF 115


U2100
PI3WVR12612NEE
BGA
CRITICAL
C2100 Might need more caps.
0.1UF
BYPASS=U2100.J4::5MM
TOWARDS TR T SNK1
TOWARDS TR X SNK0
OUTPUT CONNECTIONS SWAPPED COMPARED TO ARCHITECTURE
SEL LOGIC INVERTED TO MAINTAIN CORRECT PAK LOGIC
MANUAL STRAPS
R2104 100K
R2102 100K
DISP MUX GPU_SEL
0 = TBT T
1 = TBT X
FROM CPU
U2120
SLG4AP41172V
STQFN
CRITICAL
R2121 100K
C2120 0.1UF
MAKE_BASE=TRUE
U2110
PI3WVR12612NEE
BGA
CRITICAL
C2110 0.1UF
BYPASS=U2110.J4::5MM
R2111 100K
R2112 100K
FROM CPU
PAGE TITLE
Display Mux
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 21 OF 142
SHEET 21 OF 115
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BOM_COST_GROUP=GRAPHICS

Page Notes

Power aliases required by this page:
- =PPDDRVPP_S3_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PP2V5_S3_MEM_A_SPD (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

PPDDRVTT_S0_MEM

C2350 1UF 10V 20% X5R 402-1
C2351 1UF 10V 20% X5R 402-1
C2352 1UF 10V 20% X5R 402-1
C2353 1UF 10V 20% X5R 402-1
C2354 10UF 20% 6.3V CERM-X6S 0402

PP2V5_S3_VPP

C2330 10UF 20% 6.3V CERM-X6S 0402
C2331 1UF 10% 10V X5S 402-1
BYPASS=J2300.257::2MM

DDR4 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

PP1V2_S3

C2310 1UF 20% 6.3V X6S-CERM 0201
C2311 1UF 20% 6.3V X6S-CERM 0201
C2312 1UF 20% 6.3V X6S-CERM 0201
C2313 1UF 20% 6.3V X6S-CERM 0201
C2314 1UF 20% 6.3V X6S-CERM 0201
C2315 1UF 20% 6.3V X6S-CERM 0201
C2316 1UF 20% 6.3V X6S-CERM 0201
C2317 1UF 20% 6.3V X6S-CERM 0201

C2300 10UF 20% 6.3V CERM-X6S 0402
C2301 10UF 20% 6.3V CERM-X6S 0402
C2318 10UF 20% 6.3V CERM-X6S 0402
C2319 10UF 20% 6.3V CERM-X6S 0402
C2320 10UF 20% 6.3V CERM-X6S 0402
C2321 10UF 20% 6.3V CERM-X6S 0402
C2322 10UF 20% 6.3V CERM-X6S 0402
C2323 10UF 20% 6.3V CERM-X6S 0402

CRITICAL C2324 470UF-0.006OHM 20% 2V POLY CASE-D2-SM
NOSTUFF CRITICAL C2325 470UF-0.006OHM 20% 2V POLY CASE-D2-SM

PP0V6_S3_MEM_VREFCAA

C2335 2.2UF 20% 6.3V CERM 402-LF
C2336 0.1UF 20% 10V CERM 402

J2300
DDR4-SO-DIMM-X1037
F-ANG-SM
SYM 2 OF 3

DM8*/DBI8*/NC	96	PP1V2_S3
DM7*/DBI7*/NC	241	
DM6*/DBI6*/NC	220	
DM5*/DBI5*/NC	199	
DM4*/DBI4*/NC	178	
DM3*/DBI3*/NC	75	
DM2*/DBI2*/NC	54	
DM1*/DBI1*/NC	33	
DM0*/DBI0*/NC	12	
DQS8_T	97	NC
DQS8_C	95	NC
DQS7_T	242	MEM_A_DQS_P<7>
DQS7_C	240	MEM_A_DQS_N<7>
DQS6_T	221	MEM_A_DQS_P<6>
DQS6_C	219	MEM_A_DQS_N<6>
DQS5_T	200	MEM_A_DQS_P<5>
DQS5_C	198	MEM_A_DQS_N<5>
DQS4_T	179	MEM_A_DQS_P<4>
DQS4_C	177	MEM_A_DQS_N<4>
DQS3_T	76	MEM_A_DQS_P<3>
DQS3_C	74	MEM_A_DQS_N<3>
DQS2_T	55	MEM_A_DQS_P<2>
DQS2_C	53	MEM_A_DQS_N<2>
DQS1_T	34	MEM_A_DQS_P<1>
DQS1_C	32	MEM_A_DQS_N<1>
DQS0_T	13	MEM_A_DQS_P<0>
DQS0_C	11	MEM_A_DQS_N<0>

P/N: 516S00327

J2300
DDR4-SO-DIMM-X1037
F-ANG-SM
SYM 1 OF 3

MEM_A_A<16>	152	RAS*/A16
MEM_A_A<15>	156	CAS*/A15
MEM_A_A<14>	151	WE*/A14
MEM_A_A<13>	158	A13
MEM_A_A<12>	119	A12
MEM_A_A<11>	120	A11
MEM_A_A<10>	146	A10/AP
MEM_A_A<9>	121	A9
MEM_A_A<8>	125	A8
MEM_A_A<7>	122	A7
MEM_A_A<6>	127	A6
MEM_A_A<5>	126	A5
MEM_A_A<4>	128	A4
MEM_A_A<3>	131	A3
MEM_A_A<2>	132	A2
MEM_A_A<1>	133	A1
MEM_A_A<0>	144	A0
MEM_A_BA<1>	145	BA1
MEM_A_BA<0>	150	BA0
MEM_A_CLK_P<1>	138	CK1_T/NF
MEM_A_CLK_N<1>	140	CK1_C/NF
MEM_A_CLK_P<0>	137	CK0_T
MEM_A_CLK_N<0>	139	CK0_C
NC	165	C1/CS3*/NC
NC	162	C0/CS2*/NC
MEM_A_CS_L<1>	157	CS1*/NC
MEM_A_CS_L<0>	149	CS0*
MEM_A_CKE<1>	110	CKE1/NC
MEM_A_CKE<0>	109	CKE0
MEM_A_BG<1>	113	BG1
MEM_A_BG<0>	115	BG0
MEM_A_ODT<1>	161	ODT1/NC
MEM_A_ODT<0>	155	ODT0
MEM_A_PAR	143	PARITY
NC	104	CB7/NC
NC	100	CB6/NC
NC	87	CB5/NC
NC	88	CB4/NC
NC	105	CB3/NC
NC	101	CB2/NC
NC	91	CB1/NC
NC	92	CB0/NC
MEM_RESET_L	108	RESET*
PP2V5_S3_VPP	255	VDDSPD
MEM_DIMMA_SA<2>	166	SA2
MEM_DIMMA_SA<1>	260	SA1
MEM_DIMMA_SA<0>	256	SA0
I2C_SODIMM_SDA	254	SDA
I2C_SODIMM_SCL	253	SCL
PP0V6_S3_MEM_VREFCAA	164	VREFCA
PP2V5_S3_VPP	257	VPP
	259	VPP
MEM_A_ACT_L	114	ACT*
MEM_A_ALERT_L	116	ALERT*

DQ63	246	MEM_A_DQ<63>
DQ62	245	MEM_A_DQ<62>
DQ61	233	MEM_A_DQ<56>
DQ60	232	MEM_A_DQ<60>
DQ59	250	MEM_A_DQ<59>
DQ58	249	MEM_A_DQ<58>
DQ57	236	MEM_A_DQ<57>
DQ56	237	MEM_A_DQ<61>
DQ55	225	MEM_A_DQ<53>
DQ54	224	MEM_A_DQ<55>
DQ53	212	MEM_A_DQ<50>
DQ52	211	MEM_A_DQ<52>
DQ51	229	MEM_A_DQ<49>
DQ50	228	MEM_A_DQ<51>
DQ49	215	MEM_A_DQ<54>
DQ48	216	MEM_A_DQ<48>
DQ47	204	MEM_A_DQ<43>
DQ46	203	MEM_A_DQ<42>
DQ45	190	MEM_A_DQ<40>
DQ44	191	MEM_A_DQ<45>
DQ43	208	MEM_A_DQ<46>
DQ42	207	MEM_A_DQ<47>
DQ41	194	MEM_A_DQ<44>
DQ40	195	MEM_A_DQ<41>
DQ39	182	MEM_A_DQ<39>
DQ38	183	MEM_A_DQ<38>
DQ37	169	MEM_A_DQ<37>
DQ36	170	MEM_A_DQ<36>
DQ35	186	MEM_A_DQ<35>
DQ34	187	MEM_A_DQ<34>
DQ33	173	MEM_A_DQ<33>
DQ32	174	MEM_A_DQ<32>
DQ31	80	MEM_A_DQ<31>
DQ30	79	MEM_A_DQ<30>
DQ29	67	MEM_A_DQ<29>
DQ28	66	MEM_A_DQ<28>
DQ27	84	MEM_A_DQ<27>
DQ26	83	MEM_A_DQ<26>
DQ25	71	MEM_A_DQ<25>
DQ24	70	MEM_A_DQ<24>
DQ23	59	MEM_A_DQ<23>
DQ22	58	MEM_A_DQ<22>
DQ21	45	MEM_A_DQ<17>
DQ20	46	MEM_A_DQ<16>
DQ19	63	MEM_A_DQ<19>
DQ18	62	MEM_A_DQ<18>
DQ17	49	MEM_A_DQ<20>
DQ16	50	MEM_A_DQ<21>
DQ15	37	MEM_A_DQ<14>
DQ14	38	MEM_A_DQ<15>
DQ13	25	MEM_A_DQ<9>
DQ12	24	MEM_A_DQ<8>
DQ11	42	MEM_A_DQ<13>
DQ10	41	MEM_A_DQ<12>
DQ9	29	MEM_A_DQ<10>
DQ8	28	MEM_A_DQ<11>
DQ7	17	MEM_A_DQ<7>
DQ6	16	MEM_A_DQ<2>
DQ5	3	MEM_A_DQ<5>
DQ4	4	MEM_A_DQ<4>
DQ3	21	MEM_A_DQ<3>
DQ2	20	MEM_A_DQ<6>
DQ1	7	MEM_A_DQ<1>
DQ0	8	MEM_A_DQ<0>
EVENT*/NF	134	NC

J2300
DDR4-SO-DIMM-X1037
F-ANG-SM
SYM 3 OF 3

VSS	251	VDD	163
VSS	247	VDD	159
VSS	243	VDD	153
VSS	239	VDD	147
VSS	235	VDD	141
VSS	231	VDD	135
VSS	227	VDD	129
VSS	223	VDD	123
VSS	217	VDD	117
VSS	213	VDD	111
VSS	209	VDD	112
VSS	205	VDD	118
VSS	201	VDD	124
VSS	197	VDD	130
VSS	193	VDD	136
VSS	189	VDD	142
VSS	185	VDD	148
VSS	181	VDD	154
VSS	175	VDD	160
VSS	171	VTT	258
VSS	167	IO261	261
VSS	107	IO262	262
VSS	103	IO263	263
VSS	99	IO264	264
VSS	93	IO265	265
VSS	89	IO266	266
VSS	85		
VSS	81	VSS	60
VSS	77	VSS	64
VSS	73	VSS	68
VSS	69	VSS	72
VSS	65	VSS	78
VSS	61	VSS	82
VSS	57	VSS	86
VSS	51	VSS	90
VSS	47	VSS	94
VSS	43	VSS	98
VSS	39	VSS	102
VSS	35	VSS	106
VSS	31	VSS	168
VSS	27	VSS	172
VSS	23	VSS	176
VSS	19	VSS	180
VSS	15	VSS	184
VSS	9	VSS	188
VSS	5	VSS	192
VSS	1	VSS	196
VSS	2	VSS	202
VSS	6	VSS	206
VSS	10	VSS	210
VSS	14	VSS	214
VSS	18	VSS	218
VSS	22	VSS	222
VSS	26	VSS	226
VSS	30	VSS	230
VSS	36	VSS	234
VSS	40	VSS	238
VSS	44	VSS	244
VSS	48	VSS	248
VSS	52	VSS	252
VSS	56		

PP1V2_S3
PPDDRVTT_S0_MEM

PP0V5_S3_VPP
MEM_DIMMA_SA<2>
MEM_DIMMA_SA<1>
MEM_DIMMA_SA<0>

R2340 10K 5% 1/10W MF-LF 402
R2341 10K 5% 1/10W MF-LF 402
R2342 10K 5% 1/10W MF-LF 402
C2340 2.2UF 20% 6.3V CERM 402-LF
C2341 0.1UF 20% 10V CERM 402

Memory desense caps

PP1V2_S3
C23A0 12PF 5% 25V NP0-C0G 0201
C23A1 12PF 5% 25V NP0-C0G 0201
C23A2 3.0PF +/-0.1PF 25V NP0-C0G 0201
C23A3 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP2V5_S3_VPP
C23A4 12PF 5% 25V NP0-C0G 0201
C23A5 3.0PF +/-0.1PF 25V NP0-C0G 0201

BOM_COST_GROUP=DRAM

SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE: DDR4 DIM A
Apple Inc.
DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 23 OF 142
SHEET: 23 OF 115

Page Notes

Power aliases required by this page:
- =PPDDRVPP_S3_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PP2V5_S3_MEM_B_SPD (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMM0_SCL
- =I2C_SODIMM0_SDA

BOM options provided by this page:
(NONE)

PPDDRVTT_S0_MEM
C2550 1UF 20% 6.3V CERM 402-1
C2551 1UF 20% 6.3V CERM 402-1
C2552 1UF 20% 6.3V CERM 402-1
C2553 1UF 20% 6.3V CERM 402-1
C2554 10UF 20% 6.3V CERM-X6S 0402

PP2V5_S3_VPP
C2530 10UF 20% 6.3V CERM-X6S 0402
C2531 1UF 10% 10V X5R 402-1
BYPASS=J2500.257::2MM

DDR4 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

PP1V2_S3
C2510 1UF 20% 6.3V X6S-CERM 0201
C2511 1UF 20% 6.3V X6S-CERM 0201
C2512 1UF 20% 6.3V X6S-CERM 0201
C2513 1UF 20% 6.3V X6S-CERM 0201
C2514 1UF 20% 6.3V X6S-CERM 0201
C2515 1UF 20% 6.3V X6S-CERM 0201
C2516 1UF 20% 6.3V X6S-CERM 0201
C2517 1UF 20% 6.3V X6S-CERM 0201
C2500 10UF 20% 6.3V CERM-X6S 0402
C2501 10UF 20% 6.3V CERM-X6S 0402
C2518 10UF 20% 6.3V CERM-X6S 0402
C2519 10UF 20% 6.3V CERM-X6S 0402
C2520 10UF 20% 6.3V CERM-X6S 0402
C2521 10UF 20% 6.3V CERM-X6S 0402
C2522 10UF 20% 6.3V CERM-X6S 0402
C2523 10UF 20% 6.3V CERM-X6S 0402
CRITICAL C2524 470UF-0.0060HM 20% 2V POLY CASE-D2-SM
NOSTUFF CRITICAL C2525 470UF-0.0060HM 20% 2V POLY CASE-D2-SM

PP0V6_S3_MEM_VREFCAB
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 0.1UF 20% 10V CERM 402

PP2V5_S3_VPP
MEM_DIMMB_SA<2>
MEM_DIMMB_SA<1>
MEM_DIMMB_SA<0>
R2541 10K 5% 1/16W MF-LF 402
R2540 10K 5% 1/16W MF-LF 402
R2542 10K 5% 1/16W MF-LF 402
C2540 2.2UF 20% 6.3V CERM 402-LF
C2541 0.1UF 20% 10V CERM 402

J2500
DDR4-SO-DIMM-X1037
F-ANG-SM
SYM 2 OF 3

DM8*/DBI8*/NC	96	PP1V2_S3
DM7*/DBI7*/NC	241	
DM6*/DBI6*/NC	220	
DM5*/DBI5*/NC	199	
DM4*/DBI4*/NC	178	
DM3*/DBI3*/NC	75	
DM2*/DBI2*/NC	54	
DM1*/DBI1*/NC	33	
DM0*/DBI0*/NC	12	
DQS8_T	97	NC
DQS8_C	95	NC
DQS7_T	242	MEM_B_DQS_P<7>
DQS7_C	240	MEM_B_DQS_N<7>
DQS6_T	221	MEM_B_DQS_P<6>
DQS6_C	219	MEM_B_DQS_N<6>
DQS5_T	200	MEM_B_DQS_P<5>
DQS5_C	198	MEM_B_DQS_N<5>
DQS4_T	179	MEM_B_DQS_P<4>
DQS4_C	177	MEM_B_DQS_N<4>
DQS3_T	76	MEM_B_DQS_P<3>
DQS3_C	74	MEM_B_DQS_N<3>
DQS2_T	55	MEM_B_DQS_P<2>
DQS2_C	53	MEM_B_DQS_N<2>
DQS1_T	34	MEM_B_DQS_P<1>
DQS1_C	32	MEM_B_DQS_N<1>
DQS0_T	13	MEM_B_DQS_P<0>
DQS0_C	11	MEM_B_DQS_N<0>

P/N: 998-05060

J2500
DDR4-SO-DIMM-X1037
F-ANG-SM
SYM 1 OF 3

MEM_B_A<16>	152	RAS*/A16
MEM_B_A<15>	156	CAS*/A15
MEM_B_A<14>	151	WE*/A14
MEM_B_A<13>	158	A13
MEM_B_A<12>	119	A12
MEM_B_A<11>	120	A11
MEM_B_A<10>	146	A10/AP
MEM_B_A<9>	121	A9
MEM_B_A<8>	125	A8
MEM_B_A<7>	122	A7
MEM_B_A<6>	127	A6
MEM_B_A<5>	126	A5
MEM_B_A<4>	128	A4
MEM_B_A<3>	131	A3
MEM_B_A<2>	132	A2
MEM_B_A<1>	133	A1
MEM_B_A<0>	144	A0
MEM_B_BA<1>	145	BA1
MEM_B_BA<0>	150	BA0
MEM_B_CLK_P<1>	138	CK1_T/NF
MEM_B_CLK_N<1>	140	CK1_C/NF
MEM_B_CLK_P<0>	137	CK0_T
MEM_B_CLK_N<0>	139	CK0_C
NC	165	C1/CS3*/NC
NC	162	C0/CS2*/NC
MEM_B_CS_L<1>	157	CS1*/NC
MEM_B_CS_L<0>	149	CS0*
MEM_B_CKE<1>	110	CKE1/NC
MEM_B_CKE<0>	109	CKE0
MEM_B_BG<1>	113	BG1
MEM_B_BG<0>	115	BG0
MEM_B_ODT<1>	161	ODT1/NC
MEM_B_ODT<0>	155	ODT0
MEM_B_PAR	143	PARITY
NC	104	CB7/NC
NC	100	CB6/NC
NC	87	CB5/NC
NC	88	CB4/NC
NC	105	CB3/NC
NC	101	CB2/NC
NC	91	CB1/NC
NC	92	CB0/NC
MEM_RESET_L	108	RESET*
PP2V5_S3_VPP	255	VDDSPD
MEM_DIMMB_SA<2>	166	SA2
MEM_DIMMB_SA<1>	260	SA1
MEM_DIMMB_SA<0>	256	SA0
I2C_SODIMM_SDA	254	SDA
I2C_SODIMM_SCL	253	SCL
PP0V6_S3_MEM_VREFCAB	164	VREFCA
PP2V5_S3_VPP	257	VPP
	259	VPP
MEM_B_ACT_L	114	ACT*
MEM_B_ALERT_L	116	ALERT*
EVENT*/INF	134	NC

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PP1V2_S3

J2500
DDR4-SO-DIMM-X1037
F-ANG-SM
SYM 3 OF 3

251	VSS	VDD 163
247	VSS	VDD 159
243	VSS	VDD 153
239	VSS	VDD 147
235	VSS	VDD 141
231	VSS	VDD 135
227	VSS	VDD 129
223	VSS	VDD 123
217	VSS	VDD 117
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209	VSS	VDD 112
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201	VSS	VDD 124
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193	VSS	VDD 136
189	VSS	VDD 142
185	VSS	VDD 148
181	VSS	VDD 154
175	VSS	VDD 160
171	VSS	
167	VSS	VTT 258 PPDDRVTT_S0_MEM
107	VSS	
103	VSS	IO261 261
99	VSS	IO262 262
93	VSS	IO263 263
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56	VSS	VSS 252

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PP1V2_S3
C25A0 12PF 5% 25V NP0-C0G 0201
C25A1 12PF 5% 25V NP0-C0G 0201
C25A2 3.0PF +/-0.1PF 25V NP0-C0G 0201
C25A3 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP2V5_S3_VPP
C25A4 12PF 5% 25V NP0-C0G 0201
C25A5 3.0PF +/-0.1PF 25V NP0-C0G 0201

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Apple Inc.
DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 25 OF 142
SHEET: 24 OF 115

Memory Bit/Byte Swizzle

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PAGE TITLE

DRAM: ALIASES AND BITSWAPS

Apple Inc.

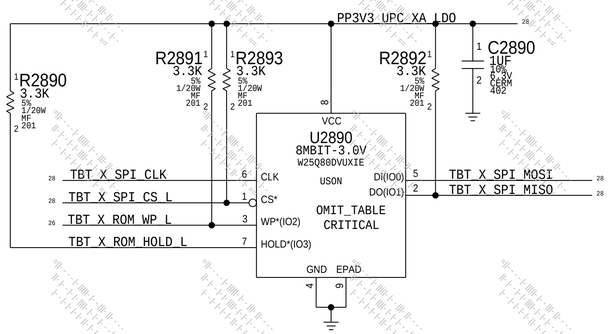
DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

BRANCH dvt-1

PAGE 27 OF 142

SHEET 25 OF 115



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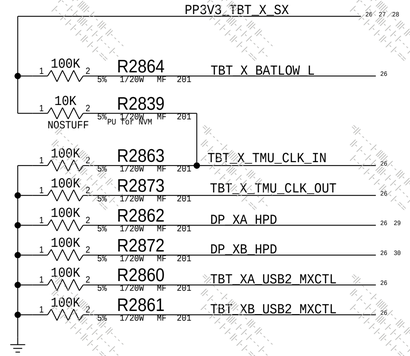
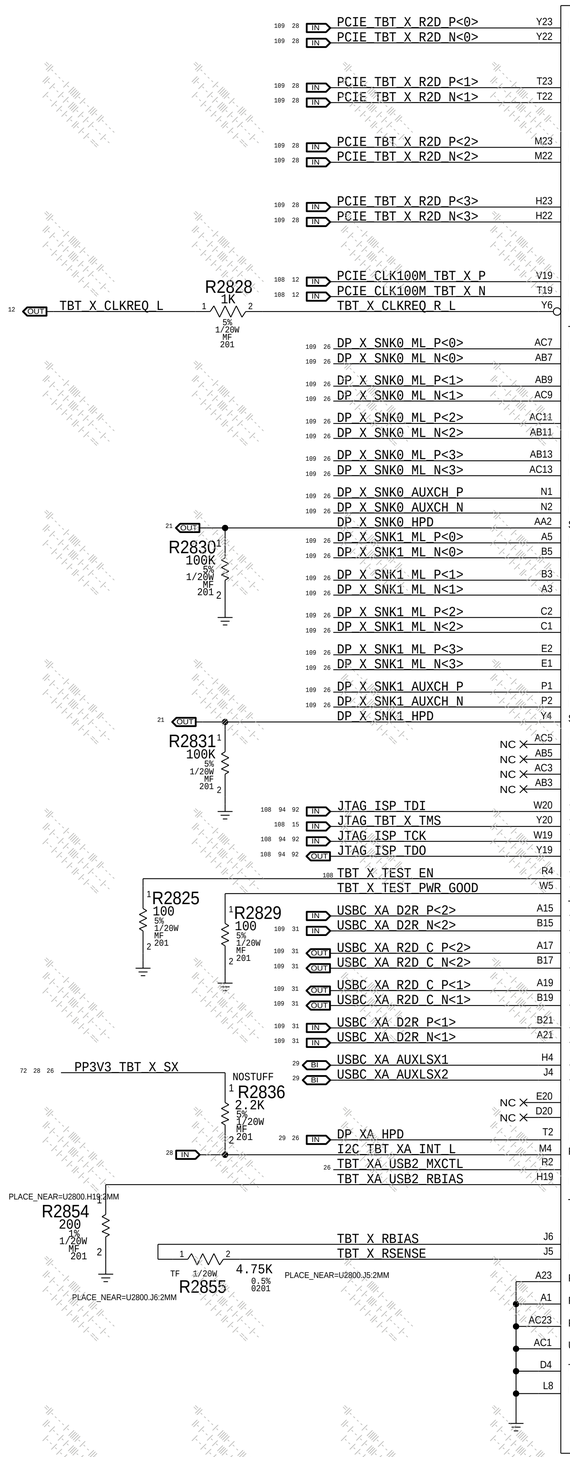
DP_X_SNK1_ML_C_N<1>	C2833 0.22UF	DP_X_SNK1_ML_N<1>	GND_VOID=TRUE
DP_X_SNK1_ML_C_P<2>	C2834 0.22UF	DP_X_SNK1_ML_P<2>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<2>	C2835 0.22UF	DP_X_SNK1_ML_N<2>	GND_VOID=TRUE
DP_X_SNK1_ML_C_P<3>	C2836 0.22UF	DP_X_SNK1_ML_P<3>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<3>	C2837 0.22UF	DP_X_SNK1_ML_N<3>	GND_VOID=TRUE
DP_X_SNK1_AUXCH_C_P	C2838 0.1UF	DP_X_SNK1_AUXCH_P	
DP_X_SNK1_AUXCH_C_N	C2839 0.1UF	DP_X_SNK1_AUXCH_N	





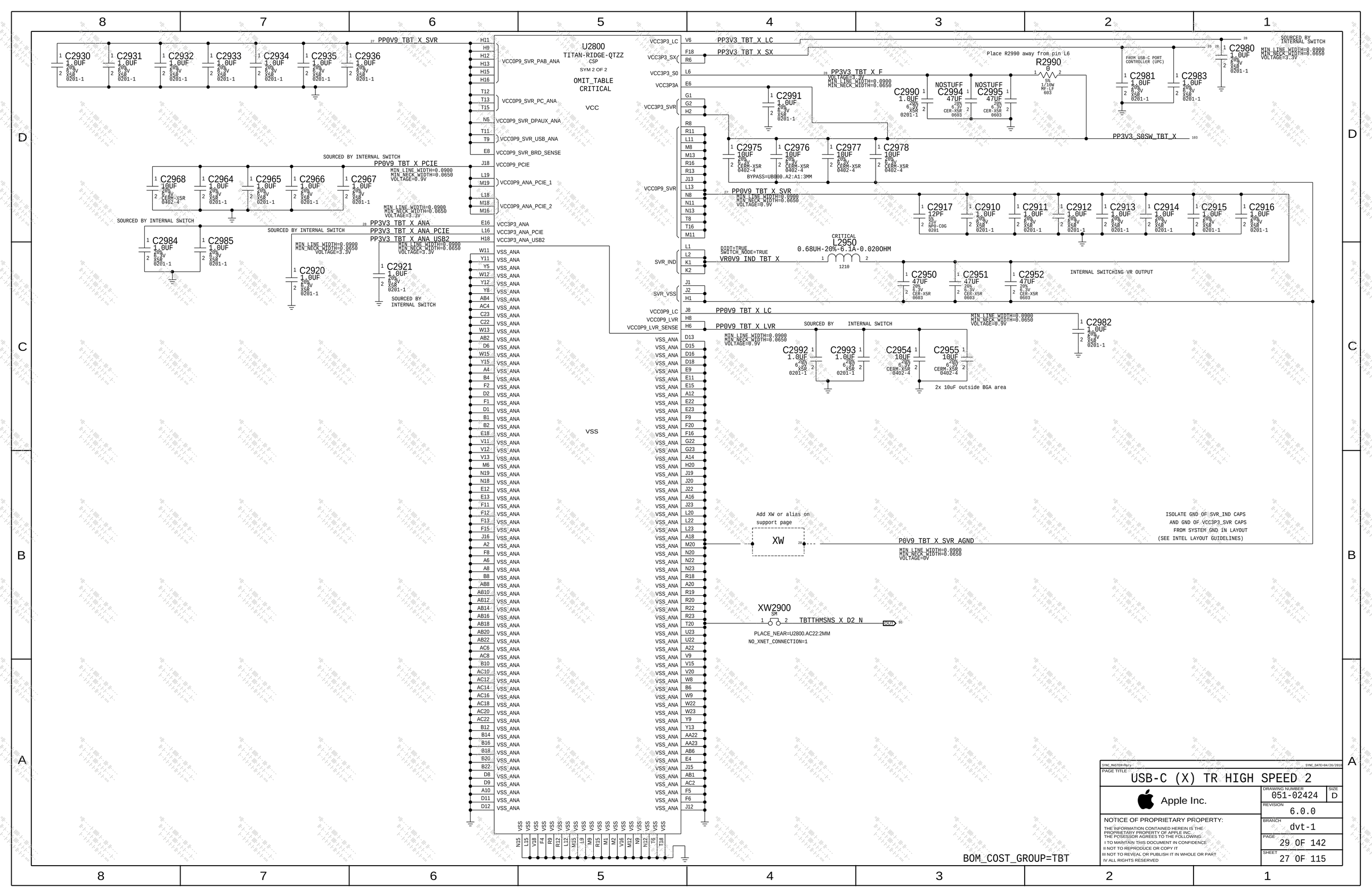
SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

USB-C (X) TR HIGH SPEED 1

Apple Inc.

DRAWING NUMBER	051-02424
SIZE	D
REVISION	6.0.0
BRANCH	dvt-1
PAGE	28 OF 142
SHEET	26 OF 115



SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: USB-C (X) TR HIGH SPEED 2

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

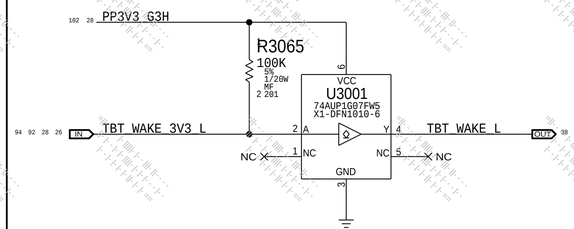
REVISION: 6.0.0

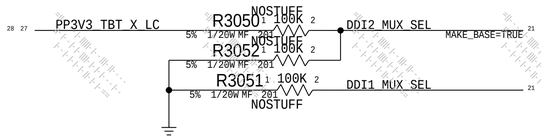
BRANCH: dvt-1

PAGE: 29 OF 142

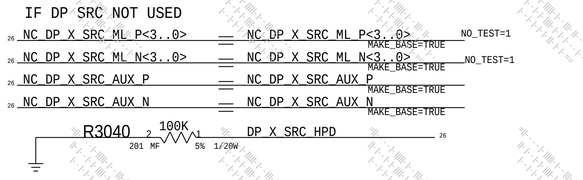
SHEET: 27 OF 115

TBT WAKE BUFFER

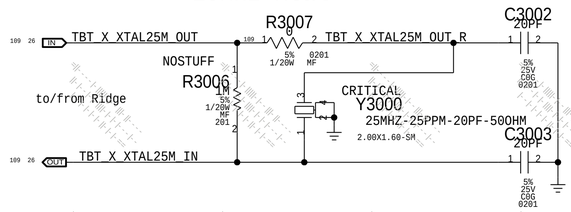




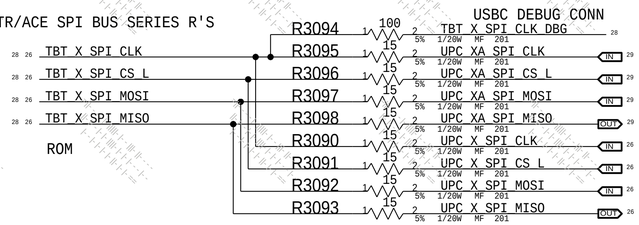
DP SRC OPTIONS



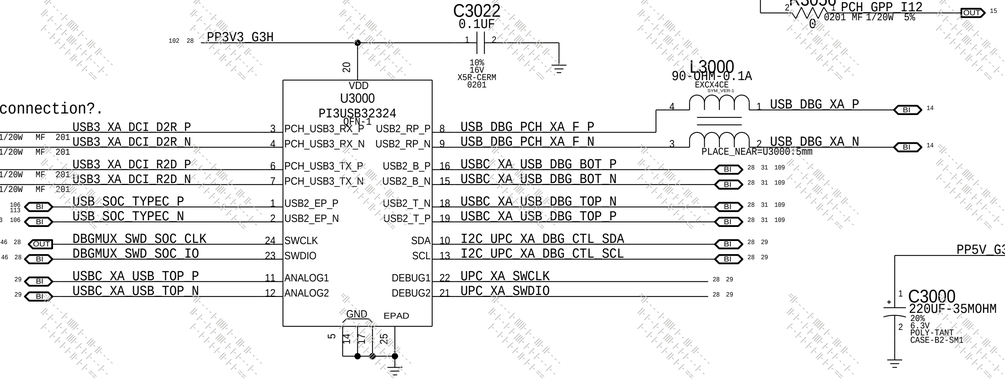
25MHz xtal



TR/ACE SPI BUS SERIES R'S

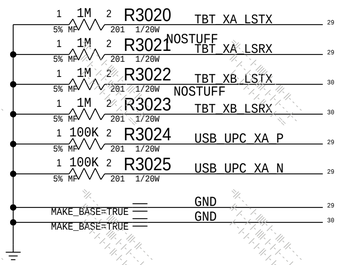


USBC DEBUG CONN



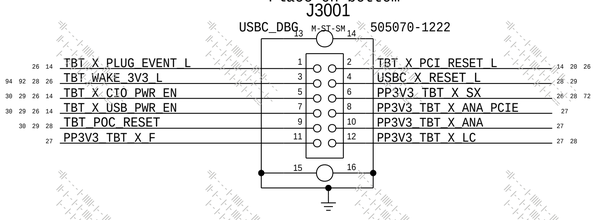
Only keep USB-A DCI connection?.

ACE Pull-Downs



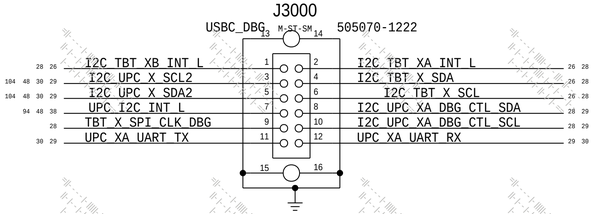
RIDGE TBT_X ARKANOID CONN

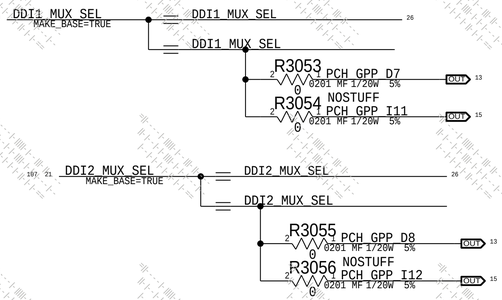
Place on bottom



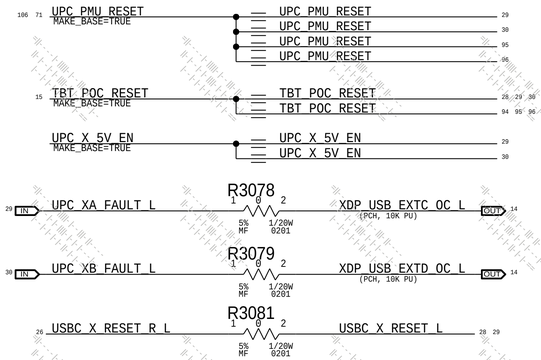
ACE ARKANOID CONN

Place on bottom

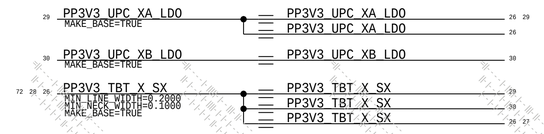




SIGNAL ALIASES

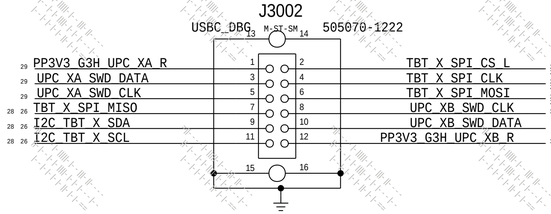


POWER ALIASES

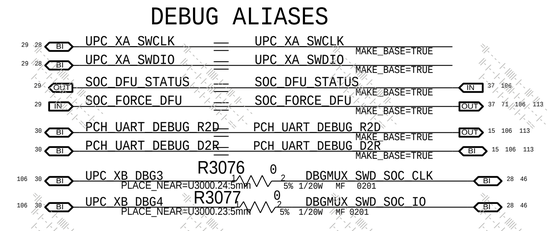


AARDVARKANOID CONN

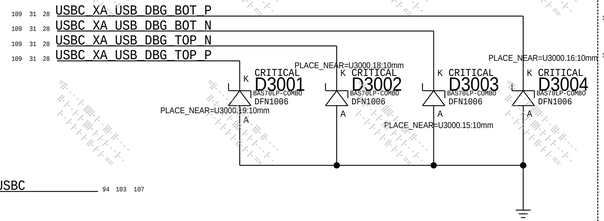
Place on TOP

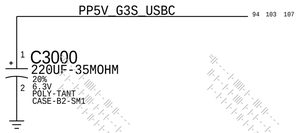


DEBUG ALIASES



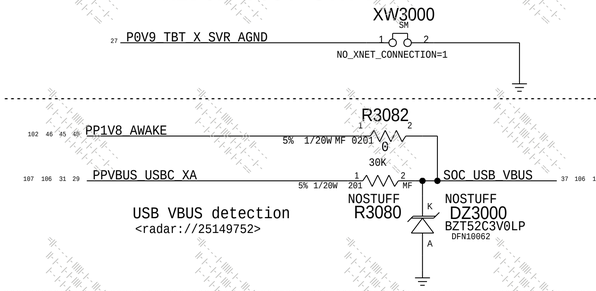
Diodes for USB2



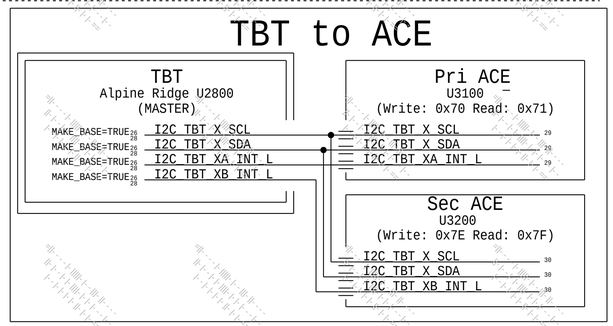


BOM_COST_GROUP=USB-C

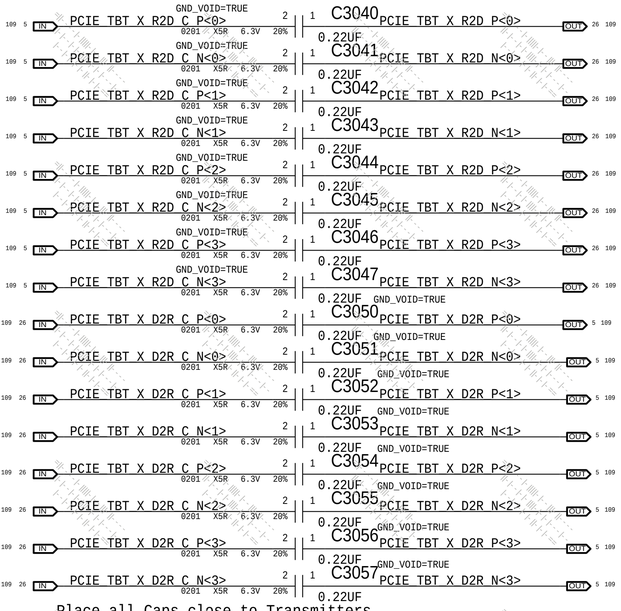
RIDGE 0.9V SVR XW



TBT to ACE



Ridge PCIE Caps



Place all Caps close to Transmitters
R2D ones close to CPU, D2R ones to TBT.

PAGE TITLE: USB-C (X) Support

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 30 OF 142
SHEET: 28 OF 115

X PRIMARY ACE USB-C PORT CONTROLLER (UPC)

J137 USBC SUPPORTS 5V @ 3A
PP12V IS FOR PROGRAMMING ACE ONLY

PPVBUS_USBC_XA
PP1V8_SLPS2R
1V8 SOURCE FOR ACE 1V8 GPIO
PP3V3_G3H
PP12V_MAIN
ACE LDO CAN DRAW UP TO 5.9 MA WHILE PROGRAMMING OTP
R3189 0 5% 1/16W MF-LF 402 PP3V3_G3H_UPC_XA_R
12V IS TO FLASH THE ACE ONLY
R3199 0 5% 1/16W MF-LF 402 PPHV_USBC_XA
VOLTAGE=12V
PP5V_G3S_USBC
VOLTAGE=3.3V

C3198 1.0UF 10% 25V X6S 0402
C3199 1UF 10% 35V X5R 0402
C3100 10UF 20% 6.3V CERM-X5R 0402-1
C3107 1.0UF 20% 6.3V X5R 0201-1
C3101 1UF 10% 35V X5R 0402
D3100 X3-WLB1608-1 SDM2U40CSP

PP3V3_UPC_XA_LDO VOLTAGE=3.3V
PP3V3_TBT_X_SX VOLTAGE=3.3V
VOUT_3V3 FOR RIDGE, OR FLOAT IF UNUSED
PP1V8_UPC_XA_LDOA VOLTAGE=1.8V
PP1V8_UPC_XA_LDOD VOLTAGE=1.8V
PP1V1_UPC_XA_LDO_BMC VOLTAGE=1.1V

C3108 10UF 20% 6.3V CERM-X5R 0402-1
C3104 2.2UF 20% 4V X5R-CERM 0201
C3105 1.0UF 20% 6.3V X5R 0201-1
C3106 0.47UF 10% 6.3V CERM-X5R 0201

PP_5V0 A11 B11 C11 D11
PP_HV A6 A7 A8 B7
PP_CABLE H10
VBUS H11 J10 J11 K11
VIN_3V3 H1
VDDIO B1
LDO_3V3 G1
VOUT_3V3 H2
LDO_1V8A K1
LDO_1V8D A2
LDO_BMC E1

CRITICAL
OMIT_TABLE
U3100
CD3215C00
PBGA
TPS65983
C0 SILICON

MRESET HIGH FORCES F11 RESET LOW
ACTIVE LOW RESET OUTPUT
TBT_POC_RESET — MRESET E11 (DIO) (3V3)
USBC_X_RESET_L — RESET* F11 (DIO) (3V3)

TP must be present on GPIO0/1 even in production
UPC_XA_DEBUGUART_TX — GPIO0 B2 (DIO)

USE GPIO1 FOR PMU STATUS
PMU_ACTIVE_READY — GPIO1 C2 (DIO) (1V8)
USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR
TBT_X_CIO_PWR_EN — GPIO2 D10 (DIO) (3V3)
USE GPIO3 FOR POWER_GATE_EN ON BANSURI DESIGNS
TBT_X_USB_PWR_EN — GPIO3 G11 (DIO) (3V3)
DP_XA_HPD — GPIO4 C10 (DIO) (3V3)
USE GPIO5 FOR PMU RESET AFTER BOOT.
UPC_PMU_RESET — GPIO5 E10 (DIO) (1V8)
UPC_X_5V_EN — GPIO6 G10 (DIO) (3V3)
SOC_DOCK_CONNECT — GPIO7 D7 (DIO) (1V8)
UPC_XA_FAULT_L — GPIO8 H6 (DIO) (3V3)

BUSPOWERZ CONTROLS BUS POWER PATH FOR PP_EXT IT MUST BE < 0.8 V
PP3V3_UPC_XA_LDO — BUSPOWERZ F10 (AI)

I2C_ADDR CONTROLS ADDR BITS 3,2,1
J135: GND I2C_ADDR ON PRIMARY ONLY
UPC_XA_I2C_ADDR — I2C_ADDR F1 (AIO)
R_OSC NEEDS NEEDS 0.1% RES
UPC_XA_R_OSC — R_OSC G2 (AIO)

CKPLUS_WAIVE=TERMSHORTED
R3102 0 5% 1/20W MF 0201
R3103 15K 0.1% 1/20W TF-LF 0201
I2C_UPC_XA_DBG_CTL_SCL — DEBUG_CTL1 E4 (DIO) (DM2)
I2C_UPC_XA_DBG_CTL_SDA — DEBUG_CTL2 D5 (DIO)

I2C BUS 1 IS TBT / ACES
I2C_TBT_X_SDA — I2C_SDA1 D1 (DIO)
I2C_TBT_X_SCL — I2C_SCL1 D2 (DIO) (3V3)
I2C_TBT_XA_INT_L — I2C_IRQ1* C1 (HIZ)

I2C BUS 2 IS SMC / ACES
I2C_UPC_X_SDA2 — I2C_SDA2 A5 (DIO)
I2C_UPC_X_SCL2 — I2C_SCL2 B5 (DIO) (1V8)
UPC_I2C_INT_L — I2C_IRQ2* B6 (HIZ)

Portable: rear connector->TBT ROM
front connector->GND
Desktop: XA_SPI -> TBT ROM
XB_SPI -> GND
UPC_XA_SPI_CLK — SPI_CLK A3 (DO)
UPC_XA_SPI_MOSI — SPI_MOSI B4 (DO)
UPC_XA_SPI_MISO — SPI_MISO A4 (DI)
UPC_XA_SPI_CS_L — SPI_SSZ B3 (DO)

UPC_XA_SWD_DATA — SWD_DATA F4 (DIO)
UPC_XA_SWD_CLK — SWD_CLK G4 (DI)

UPC_XA_UART_RX — UART_RX F2 (DI)
UPC_XA_UART_TX — UART_TX E2 (DO)

TBT_XA_LSTX — LSX_R2P L4 (DI) (NOT USED)
TBT_XA_LSRX — LSX_P2R K4 (DO)

USB_UPC_XA_P — USB_RP_P L5 (AIO) (NOT USED)
USB_UPC_XA_N — USB_RP_N K5 (AIO)

AUX PU/PD ARE INTERNAL TO TR
TP3100 TP-P5 A
TP3101 TP-P5 A
USBC_XA_AUXLSX1 — AUX_P J1 (AIO)
USBC_XA_AUXLSX2 — AUX_N J2 (AIO)

UPC_XA_SWCLK — DEBUG1 L2 (AIO)
UPC_XA_SWDIO — DEBUG2 K2 (AIO)
SOC_DFU_STATUS — DEBUG3 L3 (AIO) (1V8)
SOC_FORCE_DFU — DEBUG4 K3 (AIO)

HV FET/SENSE
DIGITAL CORE I/O AND CONTROL
TYPE-C
PORT MUX

SS H7 (AO) — UPC_XA_SS
SENSEP B10 (AI) — C3109 0.47UF 10% 6.3V CERM-X5R 0201
SENSEN A10 (AI)
HV_GATE1 B9 (AO) — NC_UPC_XA_HV_GATE1
HV_GATE2 A9 (AO) — NC_UPC_XA_HV_GATE2

C_CC1 L9 (AIO) — USBC_XA_CC1 (BI, 31 106)
C_CC2 L10 (AIO) — USBC_XA_CC2 (BI, 31 107)
C3114 220PF 10% 16V CER-X7R 0201
C3113 220PF 10% 16V CER-X7R 0201
RPD_G1 K9 (AIO)
RPD_G2 K10 (AIO)
C_USB_TP K6 (AIO) — USBC_XA_USB_TOP_P (BI, 28)
C_USB_TN L6 (AIO) — USBC_XA_USB_TOP_N (BI, 28)
C_USB_BP K7 (AIO) — NC_USBC_XA_USB_BOT_P
C_USB_BN L7 (AIO) — NC_USBC_XA_USB_BOT_N
C_SBU1 K8 (AIO) — USBC_XA_SBU1 (BI, 31 107)
C_SBU2 L8 (AIO) — USBC_XA_SBU2 (BI, 31 107)
NC L11

SOFT START RAMP RATE = 9 * ISS / CSS
ISS = 7 UA NOMIAL, 5.5 MA MIN, 8.5 MA MAX
SHORT SENSE INPUTS TO VBUS WHEN UNUSED
FLOAT HV GATE OUTPUTS WHEN UNUSED
C_CC1 AND C_CC2 PINS USED TO DELIVER POWER TO ACTIVE CIRCUITRY INSIDE A CONNECTED CABLE AND OUTPUT USB-PD DATA TO THE CABLE AND CONNECTED DEVICE
J137 HAS NO BATTERY, SO RPD CONNECT TO GND
PORT SIDE USB TOP PAIR
PORT SIDE USB BOTTOM PAIR
PORT SIDE USB SIDEBAND
PIN L11 NC OR GND TO DISSIPATE HEAT

PULL R3109 AND R3108 UP TO ACES LDO FOR 1ST RIDGE'S ACES
PULL THEM DOWN TO GND FOR 2ND RIDGE'S ACES
PP3V3_UPC_XA_LDO (26 28 29)
R3109 1M 5% 1/20W MF 201 — I2C_UPC_XA_DBG_CTL_SCL (28 29)
R3108 1M 5% 1/20W MF 201 — I2C_UPC_XA_DBG_CTL_SDA (28 29)
R3105 1M 5% 1/20W MF 201 — UPC_XA_UART_RX (28 29 30)

GND A1 D6 E5 E6 E7 F5 G5 H4 H5 G8 H8 L1 B8 D8 E8 F6 F7 F8 G6 G7 — GND (28)
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

NOTE:
DEBUG MUX IS CONNECTED TO PRIMARY ACE OF 1ST RIDGE (XA ACE)
R3752-R3755, R3790-R3792 ARE OPTIONAL

BOM_COST_GROUP=USB-C

NOT SYNCED TO OTHER PLATFORMS
SYNC_DATE=04/26/2018
Mary

PAGE TITLE: PAGE_TITLE=USB-C (X) PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 31 OF 142
SHEET 29 OF 115

X SECONDARY ACE1 USB-C PORT CONTROLLER (UPC)

NOT SYNCED TO OTHER PLATFORMS
SYNC_DATE=04/26/2018
Mary

PAGE TITLE: PAGE_TITLE=USB-C (X) PORT CONTROLLER B

Apple Inc.

DRAWING NUMBER 051-02424 | SIZE D
REVISION 6.0.0
BRANCH dvt-1

BOM_COST_GROUP=USB-C

J137 SUPPORTS 5V @ 3A

J137 HAS A QUAD-PACK USB-C CONNECTOR

PPVBUS_USBC_XA
VOLTAGE=5V
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750

NOSTUFF C3304 1UF 10% 25V X5R 402

D3300 1610 ESDA25P35-1U1M

C3300 0.01UF 10% 25V X5R-CERM 0201
C3301 0.01UF 10% 25V X5R-CERM 0201
C3302 0.01UF 10% 25V X5R-CERM 0201
C3303 0.01UF 10% 25V X5R-CERM 0201
C3310 1UF 10% 25V X5R 402

PLACE VBUS CAPS NEAR EACH VBUS PIN

C3306 0.01UF 10% 25V X5R-CERM 0201
C3307 0.01UF 10% 25V X5R-CERM 0201
C3308 0.01UF 10% 25V X5R-CERM 0201
C3309 0.01UF 10% 25V X5R-CERM 0201
C3311 3PF +/-0.1PF 25V C0G 0201
C3312 12PF 5% 50V C0G-CERM 0201

NOTE: DEBUG MUX 2 (U3000) CONNECTS TO THIS PORT

USBC_XA_D2R_P<2> → R3370 3.01 → USBC_XA_D2R_RC_P<2> → C3370 0.33UF → USBC_XA_D2R_CONN_P<2>
USBC_XA_D2R_N<2> → R3371 3.01 → USBC_XA_D2R_RC_N<2> → C3371 0.33UF → USBC_XA_D2R_CONN_N<2>
USBC_XA_SBU1
USBC_XA_USB_DBG_TOP_N
USBC_XA_USB_DBG_TOP_P
USBC_XA_CC1
USBC_XA_R2D_C_N<1> → R3372 3.01 → USBC_XA_R2D_RC_N<1> → C3372 0.22UF → USBC_XA_R2D_CONN_N<1>
USBC_XA_R2D_C_P<1> → R3373 3.01 → USBC_XA_R2D_RC_P<1> → C3373 0.22UF → USBC_XA_R2D_CONN_P<1>

J3300 CRITICAL
RCPT-USBC-QUAD-X1037
F-RT-TH
SYM 1 OF 5
CONN A

USBC_XA_D2R_CONN_P<1>
USBC_XA_D2R_CONN_N<1>
USBC_XA_R2D_CONN_N<2>
USBC_XA_R2D_CONN_P<2>

C3378 0.33UF → USBC_XA_D2R_RC_P<1> → R3378 3.01 → USBC_XA_D2R_P<1>
C3379 0.33UF → USBC_XA_D2R_RC_N<1> → R3379 3.01 → USBC_XA_D2R_N<1>
USBC_XA_SBU2
USBC_XA_USB_DBG_BOT_N
USBC_XA_USB_DBG_BOT_P
USBC_XA_CC2
C3380 0.22UF → USBC_XA_R2D_RC_N<2> → R3380 3.01 → USBC_XA_R2D_C_N<2>
C3381 0.22UF → USBC_XA_R2D_RC_P<2> → R3381 3.01 → USBC_XA_R2D_C_P<2>

DZ3300 DZ3301 DZ3304 DZ3305 SESDL2011 DSN2-THICKSTNCL
DZ3390 DZ3302 DZ3303 DZ3391 ESD8011 X3DFN2-THICKSTNCL
DZ3392 DZ3308 DZ3309 DZ3393 5V-6.2PF 0201-THICKSTNCL
DZ3306 DZ3307 DZ3310 DZ3311 SESDL2011 DSN2-THICKSTNCL

R3301 R3300 R3303 R3302 R3305 R3304 R3307 R3306 220K

PPVBUS_USBC_XB
VOLTAGE=5V
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750

NOSTUFF C3354 1UF 10% 25V X5R 402

D3370 1610 ESDA25P35-1U1M

C3350 0.01UF 10% 25V X5R-CERM 0201
C3351 0.01UF 10% 25V X5R-CERM 0201
C3352 0.01UF 10% 25V X5R-CERM 0201
C3353 0.01UF 10% 25V X5R-CERM 0201
C3360 1UF 10% 25V X5R 402

PLACE VBUS CAPS NEAR EACH VBUS PIN

C3356 0.01UF 10% 25V X5R-CERM 0201
C3357 0.01UF 10% 25V X5R-CERM 0201
C3358 0.01UF 10% 25V X5R-CERM 0201
C3359 0.01UF 10% 25V X5R-CERM 0201
C3361 3PF +/-0.1PF 25V C0G 0201
C3362 12PF 5% 50V C0G-CERM 0201

USBC_XB_D2R_P<2> → R3374 3.01 → USBC_XB_D2R_RC_P<2> → C3374 0.33UF → USBC_XB_D2R_CONN_P<2>
USBC_XB_D2R_N<2> → R3375 3.01 → USBC_XB_D2R_RC_N<2> → C3375 0.33UF → USBC_XB_D2R_CONN_N<2>
USBC_XB_SBU1
USBC_XB_USB_TOP_N
USBC_XB_USB_TOP_P
USBC_XB_CC1
USBC_XB_R2D_C_N<1> → R3376 3.01 → USBC_XB_R2D_RC_N<1> → C3376 0.22UF → USBC_XB_R2D_CONN_N<1>
USBC_XB_R2D_C_P<1> → R3377 3.01 → USBC_XB_R2D_RC_P<1> → C3377 0.22UF → USBC_XB_R2D_CONN_P<1>

J3300 CRITICAL
RCPT-USBC-QUAD-X1037
F-RT-TH
SYM 2 OF 5
CONN B

USBC_XB_D2R_CONN_P<1>
USBC_XB_D2R_CONN_N<1>
USBC_XB_R2D_CONN_N<2>
USBC_XB_R2D_CONN_P<2>

C3382 0.33UF → USBC_XB_D2R_RC_P<1> → R3382 3.01 → USBC_XB_D2R_P<1>
C3383 0.33UF → USBC_XB_D2R_RC_N<1> → R3383 3.01 → USBC_XB_D2R_N<1>
USBC_XB_SBU2
USBC_XB_USB_BOT_N
USBC_XB_USB_BOT_P
USBC_XB_CC2
C3384 0.22UF → USBC_XB_R2D_RC_N<2> → R3384 3.01 → USBC_XB_R2D_C_N<2>
C3385 0.22UF → USBC_XB_R2D_RC_P<2> → R3385 3.01 → USBC_XB_R2D_C_P<2>

DZ3320 DZ3321 DZ3324 DZ3325 SESDL2011 DSN2-THICKSTNCL
DZ3394 DZ3322 DZ3323 DZ3395 ESD8011 X3DFN2-THICKSTNCL
DZ3396 DZ3328 DZ3329 DZ3397 5V-6.2PF 0201-THICKSTNCL
DZ3326 DZ3327 DZ3330 DZ3331 SESDL2011 DSN2-THICKSTNCL

R3309 R3308 R3311 R3310 R3313 R3312 R3315 R3314 220K

BOM_COST_GROUP=USB-C

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: USB-C (X) CONNECTORS

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 33 OF 142
SHEET 31 OF 115

PLACE HOLDER

BOM_COST_GROUP=DEBUG

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

Empty

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DRAWING NUMBER 051-02424

SIZE D

REVISION 6.0.0

BRANCH dvt-1

PAGE 34 OF 142

SHEET 32 OF 115

PLACE HOLDER

BOM_COST_GROUP=DEBUG

SYNC_MASTER=PVT SYNC_DATE=04/26/2018

PAGE TITLE

Empty

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DRAWING NUMBER 051-02424

SIZE D

REVISION 6.0.0

BRANCH dvt-1

PAGE 35 OF 142

SHEET 33 OF 115

Software	I2S_SEL	UART_SEL	UART I/F
Gen1 (macOS)	0	1	UART (PCH)
Gen2	X	0	UART (SOC)

BT_DEV_WAKE option

36 35 BT_DEV_WAKE (OUT)
R3601 0 5% 1/20W MF 0201 — SOC_BT_DEV_WAKE (IN) 38
R3602 0 NOSTUFF 5% 1/20W MF 0201 — PCH_BT_DEV_WAKE (IN) 15

107 103 35 34 PP1V8_G3S
R3621 100K 5% 1/20W MF 201

MAKE_BASE=TRUE
39 (IN) UART_BT_LH_R2D = UART_BT_LH_R2D (OUT) 35 36
39 (OUT) UART_BT_LH_D2R = UART_BT_LH_D2R (IN) 35 36
MAKE_BASE=TRUE

38 34 BTUARTMUX_SEL_PCH
R3660 100K 5% 1/20W MF 201

Q3660
DMN32D1LFB4
DFN1006
108 106 45 12 (IN) PM_PCH_PWROK → G
D, S

APN376S00335
min Vgs(th)0.7V

Q3660 ensures BT does not backpower the PCH

107 103 35 34 PP1V8_G3S
R3641 0 5% 1/20W MF 0201
103 34 PP3V3_G3S_WLANBT
BYPASS=U3640::5mm
C3640 0.1UF 10% 16V X5R-CERM 0201

39 (IN) UART_BT_R2D
39 (OUT) UART_BT_D2R
15 (IN) PCH_BT_UART_R2D
15 (OUT) PCH_BT_UART_D2R
BTUARTMUX_OE_L

U3640
PI3USB102J
X2QFN
CRITICAL
VCC
GND
M+ 5, M- 4, D+ 7, D- 6, OE* 8, SEL 10
Y+ 1, Y- 2

1 UART_BT_MUX_R2D (OUT) 35 36
2 UART_BT_MUX_D2R (IN) 35 36
10 BTUARTMUX_SEL_PCH (IN) 34 38

SEL	OUTPUT
L	SOC (M)
H	PCH (D)

107 103 35 34 PP1V8_G3S
R3651 100K 5% 1/20W MF 201

103 34 PP3V3_G3S_WLANBT
BYPASS=U3650::5mm
C3650 0.1UF 10% 16V X5R-CERM 0201

39 (IN) UART_BT_R2D_RTS_L
39 (OUT) UART_BT_D2R_CTS_L
15 (IN) PCH_BT_UART_RTS_L
15 (OUT) PCH_BT_UART_CTS_L

U3650
PI3USB102J
X2QFN
CRITICAL
VCC
GND
M+ 5, M- 4, D+ 7, D- 6, OE* 8, SEL 10
Y+ 1, Y- 2

1 UART_BT_MUX_CTS_L (OUT) 35 36
2 UART_BT_MUX_RTS_L (IN) 35 36
10 BTUARTMUX_SEL_PCH 34 38

SEL	OUTPUT
L	SOC (M)
H	PCH (D)

SOC AND PCH RTS GO TO HPN CTS
SOC AND PCH CTS GO TO HPN RTS

BOM_COST_GROUP=WIRELESS

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: WIFI/BT: Support

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 36 OF 142
SHEET 34 OF 115

PP3V3_G3S_WLANBT

C3724 10UF 20% 6.3V CERM-X5R 0402-4 — PLACE_NEAR=U3730.63:2MM
C3725 10UF 20% 6.3V CERM-X5R 0402-4 — PLACE_NEAR=U3730.89:2MM
C3721 10UF 20% 6.3V CERM-X5R 0402-4 — PLACE_NEAR=U3730.74:2MM
C3722 10UF 20% 6.3V CERM-X5R 0402-4 — PLACE_NEAR=U3730.35:2MM

PP1V8_G3S

C3723 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=U3730.3:1MM

PP3V3_G3S_WLANBT

C3713 12PF 5% 25V NP0-C0G 0201 — PLACE_NEAR=U3730.89:1MM
C3714 3.0PF +/-0.1PF 25V NP0-C0G 0201 — PLACE_NEAR=U3730.89:1MM
C3715 12PF 5% 25V NP0-C0G 0201 — PLACE_NEAR=U3730.74:1MM
C3716 3.0PF +/-0.1PF 25V NP0-C0G 0201 — PLACE_NEAR=U3730.74:1MM
C3717 12PF 5% 25V NP0-C0G 0201 — PLACE_NEAR=U3730.63:1MM
C3718 3.0PF +/-0.1PF 25V NP0-C0G 0201 — PLACE_NEAR=U3730.63:1MM
C3719 12PF 5% 25V NP0-C0G 0201 — PLACE_NEAR=U3730.35:1MM
C3720 3.0PF +/-0.1PF 25V NP0-C0G 0201 — PLACE_NEAR=U3730.35:1MM
C3728 12PF 5% 25V NP0-C0G 0201 — PLACE_NEAR=U3730.74:1MM
C3727 3.0PF +/-0.1PF 25V NP0-C0G 0201 — PLACE_NEAR=U3730.74:1MM
C3726 12PF 5% 25V NP0-C0G 0201 — PLACE_NEAR=U3730.63:1MM
C3705 3.0PF +/-0.1PF 25V NP0-C0G 0201 — PLACE_NEAR=U3730.63:1MM
C3704 12PF 5% 25V NP0-C0G 0201 — PLACE_NEAR=U3730.35:1MM
C3700 3.0PF +/-0.1PF 25V NP0-C0G 0201 — PLACE_NEAR=U3730.35:1MM

OMIT_TABLE
U3730
LBEE5ZZ1HP-092
LGA
SYM 1 OF 3
CRITICAL
339S00404

29	VDDBAT_HP		
30	VDDBAT_LP		
28	VDD3P3_BT		
42	VDD3P3_PAD		
35	VDD3P3_FEM_CORE0		
89	VDD3P3_FEM_CORE1		
74	VDD3P3_FEM_CORE2		
63	VDDIO_RFSW		
2	VDDIO_PMU		
18	VDD3P3_SDIOTP		
17	VDDIO_DIG		
3			

91	2G_ANT_CORE0	109 36	50_G_0_MATCH
87	5G_ANT_CORE0	109 36	50_A_0_MATCH
76	2G_ANT_CORE1	109 36	50_G_1_MATCH
72	5G_ANT_CORE1	109 36	50_A_1_MATCH
49	2G_ANT_CORE2	109 36	50_G_2_MATCH
65	5G_ANT_CORE2	109 36	50_A_2_MATCH
44	BT_ONLY_ANT		BT_ONLY_ANT
1	WL_JTAG_SEL	108 36	WLAN_JTAG_SEL
81	WL_JTAG_TCK (GPIO2, 100K IPU VDDIO)	36	WLAN_JTAG_TCK
82	WL_JTAG_TDI (GPIO4, IPD)	35	WLAN_JTAG_TDI
83	WL_JTAG_TMS (GPIO3, 100K IPU VDDIO)	36	WLAN_JTAG_TMS
84	WL_JTAG_TRST (GPIO6, ACTIVE LOW)	108 36	WLAN_JTAG_TRST_L
85	WL_JTAG_TDO (GPIO5)	108 36	WLAN_JTAG_TDO
93	WL_UART_RX (100K IPU VDDIO)	39 36	UART_WLAN_R2D
94	WL_UART_TX (EXT PU NEEDED)	39 36	UART_WLAN_D2R
95	WL_UART_RTS (ACTIVE LOW, EXT PU NEEDED)		UART_WLAN_D2R_CTS_L
96	WL_UART_CTS (ACTIVE LOW, 100K IPU VDDIO)	39 36	UART_WLAN_R2D_RTS_L
67	WL_SPROM_MO	36 35	WLAN_SPROM_DOUT
68	WL_SPROM_MI	36 35	WLAN_SPROM_DIN
69	WL_SPROM_CLK	36 35	WLAN_SPROM_CLK
70	WL_SPROM_CS (ACTIVE HIGH)	36 35	WLAN_SPROM_CS
97	WL_GPIO_13 (MOTION CONTEXT A)		WLAN_GPIO_13
100	WL_GPIO_21 (MOTION CONTEXT B)	108 38 36	WLAN_CONTEXT_B
99	WL_GPIO_20 (WIFI TIME SYNC, EXT PD NEEDED)	37 36 20	WLAN_AUDIO_SYNC
98	WL_GPIO_17 (ACTIVE LOW SROM PRESENCE)	35	WLAN_SROM_STRAP
159	WL_PMU_TEST_O (NOTE DEFINED)		TP_WLAN_PMU_TEST
161	WL_GPIO_14 (SECI OUT)		NC_WLAN_GPIO_14
163	WL_GPIO_12 (SECI IN)	108 38 35	WLAN_CONTEXT_A
78	WL_HOST_WAKE (EXT PULL NEEDED)	38 36	WLAN_HOST_WAKE
79	WL_DEV_WAKE (IPD)	36 13	PCH_WLAN_DEV_WAKE

6	PCIE_CLK100M_WLAN_PCH_P	IN 20	PCIE_REFCLK_P
5	PCIE_CLK100M_WLAN_PCH_N	IN 20	PCIE_REFCLK_N
9	PCH_PCIE_WLAN_D2R_C_P		PCIE_TXIP
8	PCH_PCIE_WLAN_D2R_C_N		PCIE_TXIN
12	PCH_PCIE_WLAN_R2D_P		PCIE_RXIP
11	PCH_PCIE_WLAN_R2D_N		PCIE_RXIN
14	PCH_WLAN_CLKREQ_R_L	(EXT PU NEEDED)	PCIE_CLKREQ*
15	TP_AP_PCIE_WAKE_L		PCIE_WAKE*
16	PCH_WLAN_PERST_L	(EXT PU NEEDED)	PERST*
54	UART_BT_MUX_R2D	(IPU VDDIO)	BT_UART_RX
55	UART_BT_MUX_D2R	(EXT PU NEEDED)	BT_UART_TX
56	UART_BT_MUX_CTS_L	(ACTIVE LOW, IPU VDDIO)	BT_UART_CTS
57	UART_BT_MUX_RTS_L	(ACTIVE LOW, EXT PU NEEDED)	BT_UART_RTS
53	BT_ROM_BOOT_HPN_L	(40K IPD)	BT_GPIO_2/BT_SF_STRAP
60	TP_BT_JTAG_STRAP	(NOT DEFINED)	BT_JTAG_STRAP
36	BT_SPI2_CSN	(ACTIVE LOW)	BT_SF_CS
37	BT_SPI2_CLK		BT_SF_CLK
38	BT_SPI2_MISO		BT_SF_MISO
39	BT_SPI2_MOSI		BT_SF_MOSI
40	UART_BT_LH_R2D	(I2S:IPD, UART:IPU)	BT_I2S_WS
41	TP_I2S_BT_D2R	(I2S:EXT PD NEEDED, UART:NONE?)	BT_I2S_DO
123	UART_BT_LH_D2R	(I2S:IPD, UART:NONE)	BT_I2S_CLK
124	TP_I2S_BT_R2D	(I2S:IPD, UART:NONE)	BT_I2S_DI
59	TP_BT_GPIO_3	(BT TIME STAMP)	BT_GPIO_3
58	TP_BT_GPIO_4	(BT TIME SYNC)	BT_GPIO_4
		(RSVD)	
61	BT_DEV_WAKE	(IPD)	BT_DEV_WAKE
62	BT_HOST_WAKE	(EXT PULL NEEDED)	BT_HOST_WAKE

C3707 0.1UF 10% 6.3V X7R 0201 — U3730.9:2mm — PCIE_WLANPCH_D2R_P — OUT 20
C3706 0.1UF 10% 6.3V X7R 0201 — U3730.8:2mm — PCIE_WLANPCH_D2R_N — OUT 20
C3709 0.1UF 10% 6.3V X7R 0201 — PCIE_WLANPCH_R2D_C_P — IN 20
C3708 0.1UF 10% 6.3V X7R 0201 — PCIE_WLANPCH_R2D_C_N — IN 20

PP1V8_G3S
R3715 100K 5% 1/20W MF 201
R3714 100K 5% 1/20W MF 201
NOSTUFF R3700 49.9 1% 1/20W MF 201
R3701 10K 1% 1/20W MF 201

PP1V8_G3S
PP1V8_S5
R3780 10K 5% 1/20W MF 201 (PCH)
NOSTUFF R3713 10K 5% 1/20W MF 201
R3785 0 5% 1/20W MF 0201 — PCH_BT_ROM_BOOT_L — IN 15
R3786 0 5% 1/20W NOSTUFF MF 0201 (SOC) — BT_ROM_BOOT_L — IN 37

TP3701 TP TP-P5

PLACE_NEAR=U3750:2MM
R3781 0 5% 1/20W MF 0201 — BT_SPI2_CLK — BT_SPI2_CLK_R — WIFI_DBG
R3782 0 5% 1/20W MF 0201 — BT_SPI2_CSN — BT_SPI2_CSN_R — WIFI_DBG
PLACE_NEAR=U3750:2MM

PLACE_NEAR=U3750:2MM
R3783 0 5% 1/20W MF 0201 — BT_SPI2_MISO — BT_SPI2_MISO_R — WIFI_DBG
R3784 0 5% 1/20W MF 0201 — BT_SPI2_MOSI — BT_SPI2_MOSI_R — WIFI_DBG
PLACE_NEAR=U3750:2MM

BLUETOOTH SERIAL FLASH

PP1V8_G3S — PLACE_NEAR=U3750.8:2MM — PLACE_NEAR=U3750.8:4MM
R3751 100K 5% 1/20W MF 201
R3752 100K 5% 1/20W MF 201
R3753 10K 5% 1/20W MF 201
R3754 1K 5% 1/20W MF 201
C3710 0.1UF 10% 6.3V CERM-XSR 0201
C3712 10UF 20% 6.3V CERM-XSR 0402-4
U3750 2MBIT USON W25Q20EWUXIE OMIT_TABLE
VCC CLK CS* WP*(IO2) HOLD*(IO3) DI(IO0) DO(IO1) GND EPAD
BT_SPI2_CLK — BT_SPI2_MOSI — BT_SPI2_CSN — BT_SFLASH_CS_L — BT_SPI2_MISO — BT_SFLASH_WP_L — BT_SFLASH_HOLD_L

PP3V3_G3S_WLANBT — PLACE_NEAR=U3710.8:2MM
R3704 1K 5% 1/20W MF 201
C3711 0.1UF 10% 6.3V CERM-XSR 0201
U3710 CAS93C86B UDFN8 OMIT_TABLE
VCC DI CS SK PE NC DO ORG GND EPAD
WLAN_SPROM_CS — WLAN_SPROM_DOUT — WLAN_SPROM_CS_R — WLAN_SPROM_CLK — WLAN_SPROM_DIN — WIFI_SROM_ORG
BOOT_STRAPS
WLAN_SPROM_STRAP
R3702 10K 5% 1/20W MF 201
R3705 10K 5% 1/20W MF 201
R3712 10K 5% 1/20W MF 201
WLAN_SROM_STRAP:
LOW: SROM Enabled
HIGH: SROM Disabled

WLAN SERIAL EEPROM

L3701 2.2UH-1.2A 0806 DIDT=TRUE SWITCH_NODE=TRUE — P1V5_WLANBT_VLX — PP1V5_WLANBT_C — PLACE_NEAR=U3730.23:4MM — C3701 7.5UF 20% 4V 0402-THICKSTNCL — PLACE_NEAR=L3701.2:1MM — PP1V5_WLANBT — MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0650 VOLTAGE=1.5V
L3702 1UH-20%-4.1A-0.048OHM 2520-1 DIDT=TRUE SWITCH_NODE=TRUE — P1V2_WLANBT_VLX — PP1V2_WLANBT_C — PLACE_NEAR=U3730.25:4MM — C3702 7.5UF 20% 4V 0402-THICKSTNCL — PLACE_NEAR=L3702.2:1MM — PP1V2_WLANBT — MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0650 VOLTAGE=1.2V
L3703 2.2UH-1.2A 0806 DIDT=TRUE SWITCH_NODE=TRUE — PVIN_RFLDO_WLANBT_VLX — PPVIN_RFLDO_WLANBT_C — PLACE_NEAR=U3730.24:4MM — C3703 7.5UF 20% 4V 0402-THICKSTNCL — PLACE_NEAR=L3703.1:1MM — PPVIN_RFLDO_WLANBT — MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0650 VOLTAGE=1.8V
R3703 33 5% 1/20W MF 201 — PMU_CLK32K_WLANBT_R — PMU_CLK32K_WLANBT — MAKE_BASE=TRUE

BOM_COST_GROUP=WIRELESS

PAGE TITLE: WIFI/BT: MODULE 1

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 37 OF 142
SHEET: 35 OF 115

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00152	1	IND,0.9NH,1,1A,0201	L3810	CRITICAL	
131S0631	1	CAP,CER,0.3pF,0201	C3817,C3827	CRITICAL	
152S00153	1	IND,1NH,1,1A,0201	L3820	CRITICAL	
152S1222	1	IND,3NH,1,1A,0201	C3812	CRITICAL	
131S0555	1	cap,CER,1pF,0201	L3811	CRITICAL	

OMIT_TABLE
U3730
LBEE5ZZ1HP-092
LGA
SYM 2 OF 3
CRITICAL

GND
THRM_PAD

OMIT_TABLE
U3730
LBEE5ZZ1HP-092
LGA
SYM 3 OF 3
CRITICAL

THRM_PAD

R3800
1K
5%
1/20W
MF
201

PCH_WLAN_CLKREQ_R_L — PCH_WLAN_CLKREQ_L

WLAN_JTAG_TCK — WLAN_JTAG_TCK MAKE_BASE=TRUE
WLAN_JTAG_TMS — WLAN_JTAG_TMS MAKE_BASE=TRUE
WLAN_JTAG_TDI — WLAN_JTAG_TDI MAKE_BASE=TRUE

BT ARKANOID CONN

J3801
WIFI_DBG M-ST-SM 505070-1222

BT_UART_MUX_R2D	1 2	UART_BT_MUX_D2R
BT_ROM_BOOT_HPN_L	3 4	UART_BT_MUX_CTS_L
BT_DEV_WAKE	5 6	UART_BT_MUX_RTS_L
BT_HOST_WAKE	7 8	UART_BT_LH_R2D
BT_PWR_EN	9 10	UART_BT_LH_D2R
NC	11 12	NC
	15 16	

WLAN ARKANOID CONN

J3802
WIFI_DBG M-ST-SM 505070-1222

UART_WLAN_R2D	1 2	UART_WLAN_D2R
WLAN_CONTEXT_A	3 4	UART_WLAN_R2D_RTS_L
WLAN_CONTEXT_B	5 6	UART_WLAN_D2R_CTS_L
WLAN_HOST_WAKE	7 8	PCH_WLAN_CLKREQ_L
WLAN_PWR_EN	9 10	WLAN_AUDIO_SYNC
PCH_WLAN_PERST_L	11 12	PMU_CLK32K_WLANBT
	15 16	

TP3801 WLAN_JTAG_TCK
TP3802 WLAN_JTAG_TMS
TP3803 WLAN_JTAG_TDI
TP3804 WLAN_JTAG_TDO
TP3805 WLAN_JTAG_TRST_L
TP3806 WLAN_JTAG_SEL
TP3807 PCH_WLAN_DEV_WAKE
TP3808 BT_SPI2_CLK_R
TP3809 BT_SPI2_CSN_R
TP3810 BT_SPI2_MISO_R
TP3811 BT_SPI2_MOSI_R
TP3812 WLAN_SPROM_DOUT
TP3813 WLAN_SPROM_DIN
TP3814 WLAN_SPROM_CLK
TP3815 WLAN_SPROM_CS

CORE0 DIPLEXER AND MATCHING

CRITICAL
J3810
20431-001E-01
F-ST-SM
SIGNAL GND
50_0_ANT

OMIT_TABLE
C3817
0.2PF
+/-0.05PF
25V
COG-CERM
0201

OMIT_TABLE
CRITICAL
L3810
1.2NH-+/-0.05NH-1.1A-0.04OHM
0201

50_0_COM
NOSTUFF
C3816
0.2PF
+/-0.05PF
25V
COG-CERM
0201

CRITICAL
U3810
DPX205950DT-9063C2SJ
0805
COM HI LO GND
155S00449

50_A_0_DIPLEXER

OMIT_TABLE
CRITICAL
L3811
1.4NH+/-0.1NH-1.1A
0201

50_A_0_MATCH
NO STUFF
C3810
0.2PF
+/-0.05PF
25V
COG-CERM
0201

OMIT_TABLE
C3812
0.2PF
+/-0.05PF
25V
COG-CERM
0201

50_G_0_DIPLEXER
NOSTUFF
C3815
0.2PF
+/-0.05PF
25V
COG-CERM
0201

OMIT_TABLE
CRITICAL
L3814
2.5NH+/-0.1NH-0.6A
0201

50_G_0_MATCH
NOSTUFF
L3813
5.1NH-3%-0.4A
0201

CORE1 DIPLEXER AND MATCHING

CRITICAL
J3820
20431-001E-01
F-ST-SM
SIGNAL GND
50_1_ANT

OMIT_TABLE
C3827
0.2PF
+/-0.05PF
25V
COG-CERM
0201

OMIT_TABLE
CRITICAL
L3820
1.2NH-+/-0.05NH-1.1A-0.04OHM
0201

50_1_COM
NOSTUFF
C3826
0.2PF
+/-0.05PF
25V
COG-CERM
0201

CRITICAL
U3820
DPX205950DT-9163C2SJ
0805
COM HI LO GND
155S00450

50_A_1_DIPLEXER
NO STUFF
C3822
0.2PF
+/-0.05PF
25V
COG-CERM
0201

OMIT_TABLE
CRITICAL
L3821
1.2NH-+/-0.05NH-1.1A-0.04OHM
0201

50_A_1_MATCH
NO STUFF
C3820
0.2PF
+/-0.05PF
25V
COG-CERM
0201

50_G_1_DIPLEXER
NO STUFF
C3825
0.2PF
+/-0.05PF
25V
COG-CERM
0201

OMIT_TABLE
CRITICAL
L3824
2.5NH+/-0.1NH-0.6A
0201

50_G_1_MATCH
NOSTUFF
L3823
5.1NH-3%-0.4A
0201

CORE2/Aux DIPLEXER AND MATCHING

CRITICAL
J3830
20431-001E-01
F-ST-SM
SIGNAL GND
50_2_ANT

C3837
0.2PF
+/-0.05PF
25V
COG-CERM
0201
131S0431

CRITICAL
L3830
1.2NH-+/-0.05NH-1.1A-0.04OHM
0201
152S00157

50_2_COM
NOSTUFF
C3836
0.2PF
+/-0.05PF
25V
COG-CERM
0201

0805
DPX205950DT-9063C2SJ
U3830
155S00449
CRITICAL
COM HI LO GND

50_A_2_DIPLEXER
NO STUFF
C3835
0.2PF
+/-0.05PF
25V
COG-CERM
0201

OMIT_TABLE
CRITICAL
L3834
1.2NH-+/-0.05NH-1.1A-0.04OHM
0201

50_A_2_MATCH
NOSTUFF
L3833
5.1NH-3%-0.4A
0201

50_G_2_DIPLEXER
NO STUFF
C3832
0.2PF
+/-0.05PF
25V
COG-CERM
0201

OMIT_TABLE
CRITICAL
L3831
2.2NH+/-0.1NH-0.6A
0201-1

50_G_2_MATCH
NO STUFF
C3830
0.2PF
+/-0.05PF
25V
COG-CERM
0201

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	5	RES,MF,0 OHM,0.5%,0201	L3814,L3821,L3824,L3831,L3834	CRITICAL	

BOM_COST_GROUP=WIRELESS

PAGE TITLE: WIFI/BT: MODULE 2

Apple Inc.

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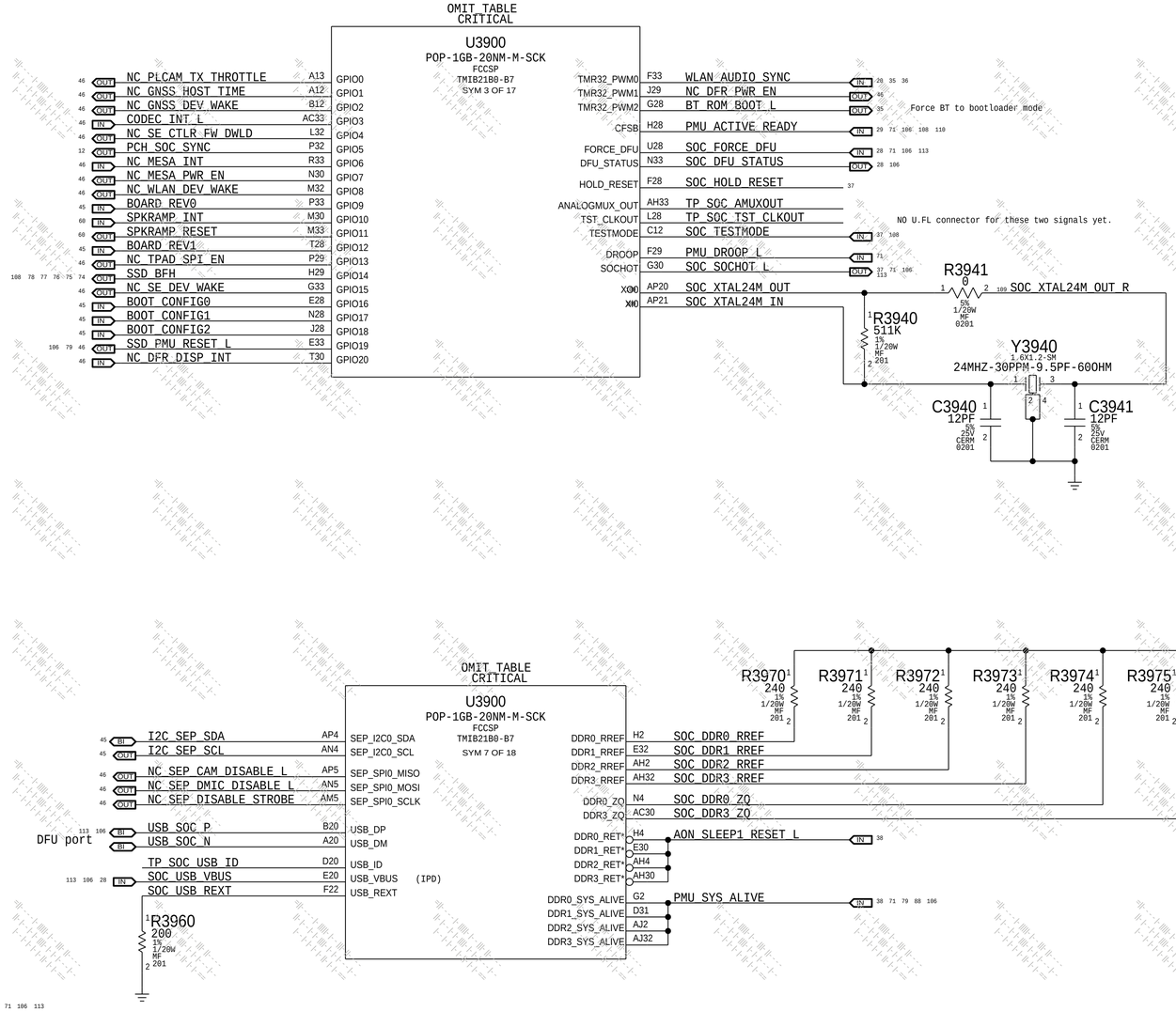
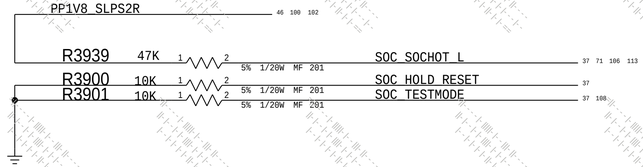
DRAWING NUMBER	051-02424
SIZE	D
REVISION	6.0.0
BRANCH	dvt-1
PAGE	38 OF 142
SHEET	36 OF 115

Note 1) IPU represents SW configured state, not HW default





BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: SoC GPIO/SEP/USB/DDR/Test

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 39 OF 142

SHEET: 37 OF 115

OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
TMI821B0-B7
SYM 6 OF 17

108 36 35	OUT	WLAN_CONTEXT_A	B5	AOP_FUNC[0]		AOP_PDM_CLK0	N6	NC_PDM_DMIC_CLK0_R
108 36 35	OUT	WLAN_CONTEXT_B	D4	AOP_FUNC[1]		AOP_PDM_CLK1	J6	NC_PDM_DMIC_CLK1_R
46	IN	NC_GYRO_INT1	G1	AOP_FUNC[2]	(IPD)	AOP_PDM_CLK2	F5	SMC_FIXTURE_MODE_L
46	IN	NC_GYRO_INT2	C5	AOP_FUNC[3]	(IPD)	AOP_PDM_CLK3	F2	NC_PLCAM_PROX_INT_L
34	OUT	BTUARTMUX_SEL_PCH	D1	AOP_FUNC[4]		AOP_PDM_CLK4	J4	NC_PLCAM_ROMEO_B2B_DETECT
15	IN	SOC_PERST_L	E4	AOP_FUNC[5]				
46	IN	NC_ALTIMETER_INT	C4	AOP_FUNC[6]	(IPD)	AOP_PDM_DATA0	F1	NC_PDM_DMIC_DATA0
46	OUT	NC_SPI_GYRO_CS_L	F4	AOP_FUNC[7]		AOP_PDM_DATA1	J1	NC_PDM_DMIC_DATA1
46	OUT	NC_SPI_ALTIMETER_CS_L	E1	AOP_FUNC[8]		AOP_SPI_MOSI	A5	NC_SPI_AOP_SENSOR_MOSI_R
						AOP_SPI_SCLK	E5	NC_SPI_AOP_SENSOR_CLK_R
48	OUT	NC_I2C_AOP_SCL	H6	AOP_I2C0_SCL				
48	BI	NC_I2C_AOP_SDA	G6	AOP_I2C0_SDA		AOP_SPI_MISO	C2	NC_SPI_AOP_SENSOR_MISO

OUT	46	
OUT	46	
IN	46	TP is needed on Dev_Supply
IN	46	
IN	46	
IN	46	
IN	46	
OUT	46	
OUT	46	
OUT	46	

OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
TMI821B0-B7
SYM 5 OF 17

46	IN	NC_DFR_TOUCH_INT_L	AG6	AON_GPIO0		JTAG_TCK	AF6	SWD_SOC_SWCLK
20	IN	CPU_SMC_THRMTRIP_L	AB6	AON_GPIO1		JTAG_TMS	AH1	SWD_SOC_SWDIO
46	IN	NC_SMC_GFX_SELF_THROTTLE	AL1	AON_GPIO2	(IPD)	JTAG_TDI	AE6	DEBUG_JTAG_SOC_TDI
46	OUT	NC_SMC_TOPBLK_SWP_L	AH5	AON_GPIO3		JTAG_TDO	AK1	DEBUG_JTAG_SOC_TDO
18	IN	XDP_PRESENT_L	AG1	AON_GPIO4		JTAG_TRST*	AH6	TP_JTAG_SOC_TRST_L
46	OUT	CODEC_RESET_L	AL4	AON_GPIO5		JTAG_SEL	Y8	SOC_JTAG_SEL
34	OUT	SOC_BT_DEV_WAKE	AK4	AON_GPIO6				(DAP=0, TAP=1)
84	IN	PCIEDN_WAKE_L	AD6	AON_GPIO7	(IPU)	DOCK_CONNECT	AJ5	SOC_DOCK_CONNECT
81 20	OUT	ENET_LOW_PWR	AM1	AON_GPIO8				
100	IN	TPAD_SPI_INT_L_ACDC_ID	AJ6	AON_GPIO9		AON_SWD0_TMS	AF2	WLAN_JTAG_TMS
46	IN	NC_SDCONN_STATE_CHANGE_L	AK5	AON_GPIO10	(IPU)	AON_SWD1_TMS	AE4	NC_MESA_MENUKEY_L
84	IN	ENET_MEDIA_SENSE	AJ1	AON_GPIO11	(IPD)	AON_SWD01_TCK	AE5	WLAN_JTAG_TCK
71	IN	PMU_INT_L	AL6	AON_GPIO12	(IPU)	WDOG	AF5	SOC_WDOG
						AON_SLEEP1_RESET*	AC6	AON_SLEEP1_RESET_L
		SPMI_CLK_R	AA6	AON_SPMI_SCLK				
		SPMI_DATA_R	AK2	AON_SPMI_SDATA				
106 71	IN	PMU_CLK32K_SOC	AK6	RT_CLK32768				
		SOC_COLD_RESET_L	AG4	COLD_RESET*				
			AF4	CFSB_AON				
108 106 71	IN	PMU_COLD_RESET_L						

IN	46 108 113	
BI	46 108 113	
IN	106 113	
IN	106 113	
IN	106	
IN	30 109	
IN	29 30 38 106	
BI	36 108	
IN	46	
OUT	36 108	
OUT	71 106	
OUT	37	

PLACE_NEAR=U3900.AA6:5MM
PLACE_NEAR=U7800.M7:5MM

71	OUT	SPMI_CLK	R4036	20	5%	1/20W	MF	201	
71	BI	SPMI_DATA	R4037	20	5%	1/20W	MF	201	

		R4039	4.7K	5%	1/20W	MF	201	

OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
TMI821B0-B7
SYM 9 OF 17

109		ESPI_IO_R<0>	R4	SMC_ESPI_IO0		SMC_GPIO0	V4	CODEC_WAKE_L
109		ESPI_IO_R<1>	R1	SMC_ESPI_IO1		SMC_GPIO1	V8	BT_HOST_WAKE
109		ESPI_IO_R<2>	T5	SMC_ESPI_IO2	(IPD)	SMC_GPIO2	V6	WLAN_HOST_WAKE
109		ESPI_IO_R<3>	T6	SMC_ESPI_IO3	(IPD)	SMC_GPIO3	U4	SMC_GFX_THROTTLE_L
113 109 12	IN	ESPI_CLK	P2	SMC_ESPI_CLK	(IPD)	SMC_GPIO4	V7	LIDINT_L_UARTHDD_D2R
113 38 12	IN	ESPI_CS_L	T4	SMC_ESPI_CS*		SMC_GPIO5	U6	PCC_EVENT
113 12	IN	ESPI_RESET_L	T2	SMC_ESPI_RESET*	(IPD)	SMC_GPIO6	V1	DP2HDMI_AOP_VDD12ON
						SMC_GPIO7	W5	PSU11VOC_WAKE_L
46 45	IN	SMC_PECI_RX	M6	SMC_PECI_IN	(IPD)	SMC_GPIO8	AC1	LIDOPEN_PSU12VPGOOD_ACDCBURST_L
45	OUT	SMC_PECI_TX	R6	SMC_PECI_OUT		SMC_GPIO9	AB2	NC_SPI_DESCRIPTOR_OVERRIDE_L
108 45	OUT	SMC_PCH_PWROK	U7	PCH_PWROK	(IPU)	SMC_GPIO10	AB1	NC_DISP_GCON_INT_L
108 45	OUT	SMC_PCH_SYS_PWROK	U8	SYS_PWROK		SMC_GPIO11	AA4	PCH_GCON_INT_L
						SMC_GPIO12	W8	PSU_P12V_EN_L
45	OUT	SMC_RSMRST_L	U1	RSMRST*	(IPU)	SMC_GPIO13	AA1	TBT_WAKE_L
108 106 45	OUT	SMC_SYSRST_L	U5	SYS_RESET*	(IPU)	SMC_GPIO14	AC2	UPC_I2C_INT_L
106 100 71 12	IN	PM_SLP_S0_L	W1	SLP_S0B		SMC_GPIO_15	K2	TP_SMC_DEBUG
63 46 45	BI	SMC_PROCHOT_L	P6	PROCHOT*				
106 88 79 71 37	IN	PMU_SYS_ALIVE	W6	SYS_ALIVE		SMC_ADC0	AE1	SMC_P12VIN_VSENSE
						SMC_ADC1	Y5	SMC_P12VIN_ISENSE
106 48	OUT	I2C_UPC_SCL	K4	SMC_I2C0_SCL		SMC_ADC2	AE2	SMC_CPU_HI_ISENSE
106 48	BI	I2C_UPC_SDA	H1	SMC_I2C0_SDA		SMC_ADC3	AB5	SMC_CPU_VCC_ISENSE
						SMC_ADC4	Y7	SMC_CPU_VCC_VSENSE
48	OUT	NC_I2C_SNS0_S0_SCL	L4	SMC_I2C1_SCL		SMC_ADC5	AD4	SMC_CPUGT_VSENSE
48	BI	NC_I2C_SNS0_S0_SDA	L5	SMC_I2C1_SDA		SMC_ADC6	AF1	SMC_CPUGT_ISENSE
						SMC_ADC7	Y6	SMC_P1V2_ISENSE
48	OUT	I2C_SNS1_S0_SCL	M4	SMC_I2C2_SCL		REFP_ADC	AC5	PP1V25_SLPS2R_SMC_AVREF
48	BI	I2C_SNS1_S0_SDA	K1	SMC_I2C2_SDA		REFM_ADC	AC4	GND_SMC_AVSS
48	OUT	I2C_DISP_SCL	L2	SMC_I2C3_SCL				
48	BI	I2C_DISP_SDA	P5	SMC_I2C3_SDA		SMC_PWM0	E2	SMC_FAN_0_PWM
106 48	OUT	I2C_PWR_SCL	L1	SMC_I2C4_SCL		SMC_TACH0	K6	SMC_FAN_0_TACH
106 48	BI	I2C_PWR_SDA	M1	SMC_I2C4_SDA		SMC_PWM1	N5	NC_SMC_FAN_1_PWM
						SMC_TACH1	L6	NC_SMC_FAN_1_TACH
48	OUT	NC_I2C_IOSNS_SCL	N1	SMC_I2C5_SCL		SMC_PWM2	K5	SMC_LED_ONEWIRE
48	BI	NC_I2C_IOSNS_SDA	N2	SMC_I2C5_SDA				
108 48	OUT	I2C_SSD_SCL	P1	SMC_I2C6_SCL	(IPU)	SMC_UART0_RXD	U2	SMC_DEBUGPRT_RX
108 48	BI	I2C_SSD_SDA	P4	SMC_I2C6_SDA		SMC_UART0_TXD	T1	SMC_DEBUGPRT_TX
						SWD_OUT0_TCK	AB4	SSD0_SWCLK_UART_R2D
						SWD_OUT0_TMS	Y1	SSD0_SWDIO_UART_D2R
						SWD_OUT1_TCK	AD1	NC_SSD1_SWCLK_UART_R2D
						SWD_OUT1_TMS	W7	NC_SSD1_SWDIO_UART_D2R

IN	46	
IN	35 36	
IN	35 36	
OUT	46	
IN	46	
BI	108	
IN	46	
IN	55	
BI	100 108	
OUT	46	
IN	46	
IN	15	
OUT	46	
IN	28	
IN	28 48 94	
IN	46	
IN	46	
IN	46	
IN	46	
IN	46	
IN	46	
IN	46	
IN	46	
IN	46	
IN	45	
IN	46	
OUT	57	
IN	57	
OUT	46	
IN	46	
BI	46	
IN	35 113	
OUT	35 113	
OUT	74 75 76 77 78 108	
BI	74 75 76 77 78 108	
OUT	46	
BI	46	

XW4089
SM
PLACE_NEAR=U3900.AC4:4MM

PLACE_NEAR=U3900.B4:5MM
PLACE_NEAR=U3900.B1:5MM
PLACE_NEAR=U3900.T5:5MM
PLACE_NEAR=U3900.T6:5MM

113 109 38 12	BI	ESPI_IO<0>	R4050	20	5%	1/20W	MF	201	
113 109 38 12	BI	ESPI_IO<1>	R4051	20	5%	1/20W	MF	201	
113 109 38 12	BI	ESPI_IO<2>	R4052	20	5%	1/20W	MF	201	
113 109 38 12	BI	ESPI_IO<3>	R4053	20	5%	1/20W	MF	201	

PP1V8_S5 — 12 16 17 103

R4046	10K	5%	1/20W	MF	201	SOC_JTAG_SEL	38 108
R4047	100K	5%	1/20W	MF	201	SOC_DOCK_CONNECT	29 30 38 106
R4054	100K	5%	1/20W	MF	201	ESPI_IO<0>	12 38 109 113
R4055	100K	5%	1/20W	MF	201	ESPI_IO<1>	12 38 109 113
R4056	100K	5%	1/20W	MF	201	ESPI_IO<2>	12 38 109 113
R4057	100K	5%	1/20W	MF	201	ESPI_IO<3>	12 38 109 113
R4059	100K	5%	1/20W	MF	201	ESPI_CS_L	12 38 113

BOM_COST_GROUP=SOC

SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE: SoC AOP/AON/SMC

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 40 OF 142
SHEET: 38 OF 115

OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
TMIB21B0-B7
SYM 4 OF 17

46 IN	GND	B24	MIPI0C_DATA0_P		ISP_I2C0_SDA	AC28	NC_I2C_FTCAM_SDA BI 49
46 IN	GND	A24	MIPI0C_DATA0_N		ISP_I2C0_SCL	AD33	NC_I2C_FTCAM_SCL OUT 49
46 IN	GND	B22	MIPI0C_DATA1_P		ISP_I2C1_SDA	AA29	NC_I2C_PLCAM_SDA BI 49
46 IN	GND	A22	MIPI0C_DATA1_N		ISP_I2C1_SCL	AD30	NC_I2C_PLCAM_SCL OUT 49
46 IN	GND	B23	MIPI0C_CLK_P		SENSOR0_CLK	AF32	NC_FTCAM_CLK12M_R OUT 46
46 IN	GND	A23	MIPI0C_CLK_N		SENSOR0_RST	AF30	NC_FTCAM_RESET_L OUT 46
					SENSOR0_ISTRB	AC29	NC_DFR_TOUCH_RESET_L OUT 46
46 IN	GND	B25	MIPI1C_DATA0_P		SENSOR1_CLK	AA28	NC_PLCAM_RX_CLK12M_R OUT 46
46 IN	GND	A25	MIPI1C_DATA0_N		SENSOR1_RST	AB30	NC_PLCAM_RX_RESET_L OUT 46
46 IN	GND	B27	MIPI1C_DATA1_P		SENSOR1_ISTRB	AA30	NC_DFR_DISP_RESET_L OUT 45
46 IN	GND	A27	MIPI1C_DATA1_N		SENSOR2_CLK	AB28	NC_PLCAM_TX_CLK12M_R OUT 46
46 IN	GND	B26	MIPI1C_CLK_P		SENSOR2_RST	AD28	NC_PLCAM_TX_RESET_L OUT 46
46 IN	GND	A26	MIPI1C_CLK_N	(IPD)	SENSOR_INT	W28	NC_PLCAM_TX_INT IN 46
46 OUT	GND	B30	MIPID_DATA0_P	(IPD)	DISP_TE	D33	NC_DFR_DISP_TE IN 46
46 OUT	GND	A30	MIPID_DATA0_N		DISP_VSYNC	L30	BOARD_REV2 IN 45
46 OUT	GND	B29	MIPID_CLK_P		CLK32K_OUT	AF29	NC_DFR_TOUCH_CLK32K_RESET_L OUT 46
46 OUT	GND	A29	MIPID_CLK_N				
	SOC_MIPI0C_REXT	F23	MIPI0C_REXT				
	SOC_MIPI1C_REXT	F25	MIPI1C_REXT				
	SOC_MIPID_REXT	F26	MIPID_REXT				

1 R4100 4.02K 1% 1/20W MF 201 2
1 R4101 4.02K 1% 1/20W MF 201 2
1 R4102 4.02K 1% 1/20W MF 201 2

OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
TMIB21B0-B7
SYM 2 OF 17

49 BI	I2C_SPKRAMP_SDA	W33	I2C0_SDA		SPI0_MISO	AN6	SPI_SOCROM_MISO IN 45
49 OUT	I2C_SPKRAMP_SCL	U30	I2C0_SCL		SPI0_MOSI	AM4	SPI_SOCROM_MOSI_R
49 BI	NC_I2C_SPKRAMP_R_SDA	AB32	I2C1_SDA		SPI0_SCLK	AN3	SPI_SOCROM_CLK_R
49 OUT	NC_I2C_SPKRAMP_R_SCL	V30	I2C1_SCL		SPI0_SSIN	AP6	SPI_SOCROM_CS_L_R
49 BI	I2C_CODEC_SDA	H30	I2C2_SDA	(IPU)	SPI1_MISO	K30	SPI_TPAD_MISO IN 45
49 OUT	I2C_CODEC_SCL	P28	I2C2_SCL		SPI1_MOSI	J30	SPI_TPAD_MOSI OUT 46
49 BI	NC_I2C_ALS_SDA	V28	I2C3_SDA		SPI1_SCLK	K33	SPI_TPAD_CLK OUT 46
49 OUT	NC_I2C_ALS_SCL	AB33	I2C3_SCL		SPI1_SSIN	R28	NC_SPI_TPAD_CS_L OUT 46
49 BI	NC_I2C_DFR_SDA	L33	I2C4_SDA		SPI2_MISO	B17	NC_SPI_MESA_MISO IN 46
49 OUT	NC_I2C_DFR_SCL	R29	I2C4_SCL		SPI2_MOSI	C17	NC_SPI_MESA_MOSI_R OUT 46
49 BI	NC_I2C_SOC_5_SDA	M29	I2C5_SDA		SPI2_SCLK	D16	NC_SPI_MESA_CLK_R OUT 46
49 OUT	NC_I2C_SOC_5_SCL	R30	I2C5_SCL		SPI2_SSIN	A17	WLAN_JTAG_TDI OUT 36 108
46 IN	NC_SPKR_ID1	J33	I2C6_SDA (IPU)		SPI3_MISO	C14	NC_SPI_DFR_MISO IN 46
46 IN	NC_SPKR_ID0	L29	I2C6_SCL (IPU)		SPI3_MOSI	D15	NC_SPI_DFR_MOSI_R OUT 46
113 IN	SOC_DEBUGPRT_RX	V32	UART0_RXD (IPU)		SPI3_SCLK	C16	NC_SPI_DFR_CLK_R OUT 46
113 OUT	SOC_DEBUGPRT_TX	U32	UART0_TXD		SPI3_SSIN	A16	NC_SPI_DFR_CS_L OUT 46
46 IN	NC_UART_SE_D2R	B15	UART1_RXD	(IPD)	I2S0_DIN	Y28	I2S_SPKRAMP_D2R_RR IN 46
46 OUT	NC_UART_SE_R2D	A15	UART1_TXD		I2S0_DOUT	AC32	I2S_SPKRAMP_R2D_R OUT 46
46 IN	NC_UART_SE_D2R_CTS_L	D13	UART1_CTS*		I2S0_BCLK	Y29	I2S_SPKRAMP_BCLK_R OUT 46
46 OUT	NC_UART_SE_R2D_RTS_L	E12	UART1_RTS*		I2S0_LRCK	AE32	I2S_SPKRAMP_LRCLK_R OUT 46
34 IN	UART_BT_D2R	F32	UART2_RXD		I2S0_MCK	AM33	NC_DFR_TOUCH_RSVD BI 46
34 OUT	UART_BT_R2D	F30	UART2_TXD	(IPD)	I2S1_DIN	C18	I2S_SPKRAMP_R_D2R IN 46
34 IN	UART_BT_D2R_CTS_L	M28	UART2_CTS*		I2S1_DOUT	E17	I2S_SPKRAMP_R_R2D_R OUT 46
34 OUT	UART_BT_R2D_RTS_L	K28	UART2_RTS*		I2S1_BCLK	D17	I2S_SPKRAMP_R_BCLK_R OUT 46
34 IN	UART_BT_LH_D2R	H32	UART3_RXD		I2S1_LRCK	B18	I2S_SPKRAMP_R_LRCLK OUT 46
34 OUT	UART_BT_LH_R2D	J32	UART3_TXD		I2S1_MCK	D18	NC_PCHROM_SW_EN OUT 46
46 IN	NC_UART_GNSS_D2R_CTS_L	H33	UART3_CTS*	(IPD)	I2S2_DIN	Y33	I2S_CODEC_D2R_RR IN 46
46 OUT	NC_UART_GNSS_R2D_RTS_L	P30	UART3_RTS*		I2S2_DOUT	AA33	I2S_CODEC_R2D_R OUT 46
36 35 IN	UART_WLAN_D2R	B14	UART4_RXD		I2S2_BCLK	AE33	I2S_CODEC_BCLK_R OUT 46
36 35 OUT	UART_WLAN_R2D	A14	UART4_TXD		I2S2_LRCK	V29	I2S_CODEC_LRCLK_R OUT 46
36 35 IN	UART_WLAN_D2R_CTS_L	C13	UART4_CTS*		I2S2_MCK	AL30	NC_I2S_CODEC_MCLK OUT 46
36 35 OUT	UART_WLAN_R2D_RTS_L	D12	UART4_RTS*	(IPD)	I2S3_DIN	R32	NC_I2S_HAWKING_D2R IN 46
					I2S3_DOUT	U33	NC_I2S_CODEC1_R2D_R OUT 46
					I2S3_BCLK	T33	NC_I2S_HAWKING_BCLK_R OUT 46
					I2S3_LRCK	U29	NC_I2S_HAWKING_LRCLK OUT 46
					I2S3_MCK	V33	NC_I2S_SPKRAMP_MCLK_R OUT 46

PLACE_NEAR=U3900.AM4:5MM
PLACE_NEAR=U3900.AN3:5MM
PLACE_NEAR=U3900.AP6:5MM

R4171 20 1 2 5% 1/20W MF 201 SPI_SOCROM_MOSI OUT 45
R4172 20 1 2 5% 1/20W MF 201 SPI_SOCROM_CLK OUT 45
R4173 20 1 2 5% 1/20W MF 201 SPI_SOCROM_CS_L OUT 45

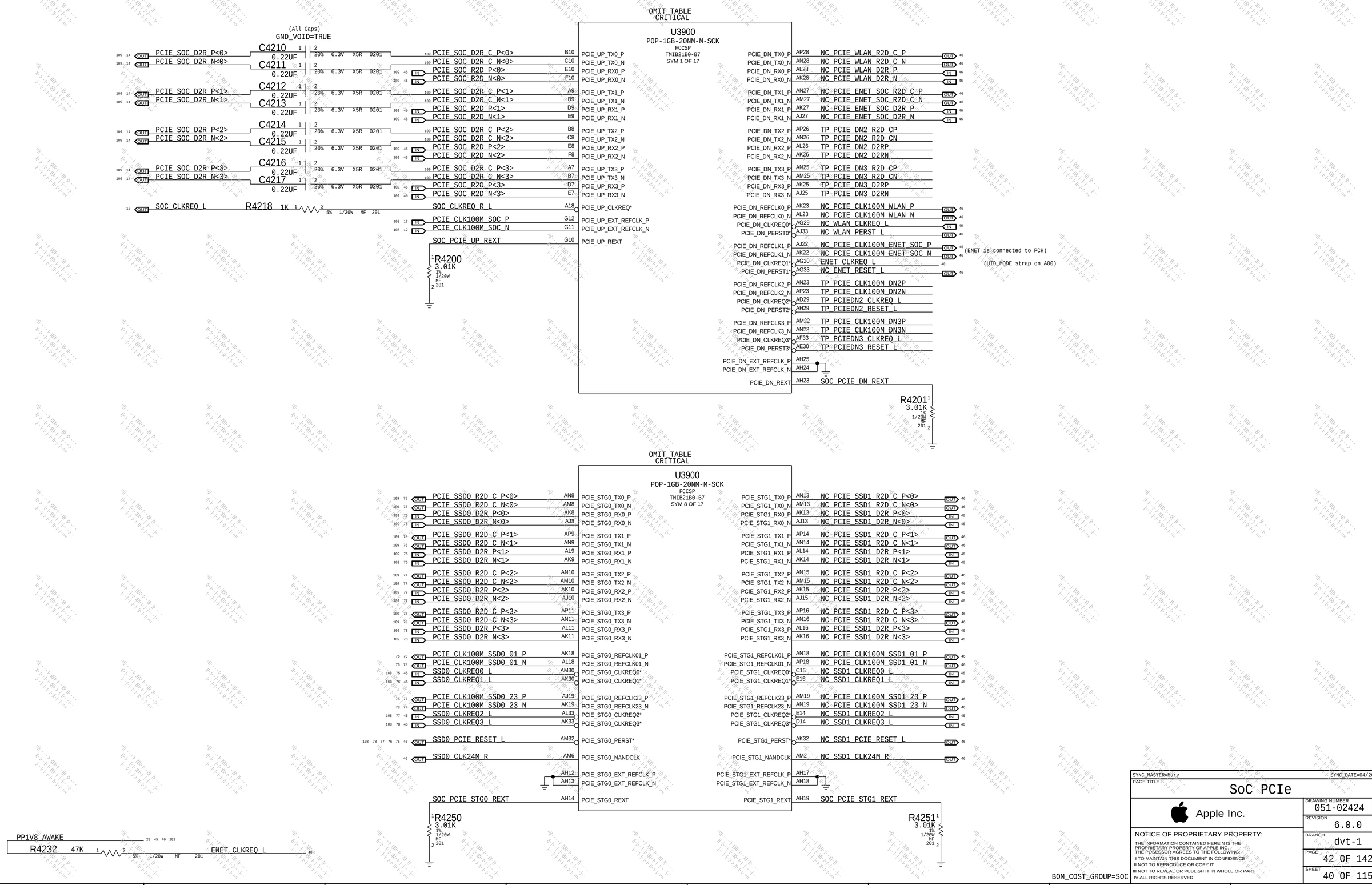
BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
SoC ISP/I2C/UART/SPI/I2S

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 41 OF 142
SHEET 39 OF 115


(All Caps)
GND_VOID=TRUE
C4210 0.22UF
C4211 0.22UF
C4212 0.22UF
C4213 0.22UF
C4214 0.22UF
C4215 0.22UF
C4216 0.22UF
C4217 0.22UF
20% 6.3V X5R 0201
PCIE SOC D2R P<0>
PCIE SOC D2R N<0>
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PCIE SOC D2R N<1>
PCIE SOC D2R P<2>
PCIE SOC D2R N<2>
PCIE SOC D2R P<3>
PCIE SOC D2R N<3>
SOC CLKREQ L
R4218 1K 5% 1/20W MF 201
PCIE SOC D2R C P<0>
PCIE SOC D2R C N<0>
PCIE SOC R2D P<0>
PCIE SOC R2D N<0>
PCIE SOC D2R C P<1>
PCIE SOC D2R C N<1>
PCIE SOC R2D P<1>
PCIE SOC R2D N<1>
PCIE SOC D2R C P<2>
PCIE SOC D2R C N<2>
PCIE SOC R2D P<2>
PCIE SOC R2D N<2>
PCIE SOC D2R C P<3>
PCIE SOC D2R C N<3>
PCIE SOC R2D P<3>
PCIE SOC R2D N<3>
SOC CLKREQ R L
PCIE CLK100M SOC P
PCIE CLK100M SOC N
SOC PCIE UP REXT
R4200 3.01K 1% 1/20W MF 201
OMIT TABLE
CRITICAL
U3900
POP-1GB-20NM-M-SCK
FCCSP
TMIB21B0-B7
SYM 1 OF 17
PCIE_UP_TX0_P B10
PCIE_UP_TX0_N C10
PCIE_UP_RX0_P E10
PCIE_UP_RX0_N F10
PCIE_UP_TX1_P A9
PCIE_UP_TX1_N B9
PCIE_UP_RX1_P D9
PCIE_UP_RX1_N E9
PCIE_UP_TX2_P B8
PCIE_UP_TX2_N C8
PCIE_UP_RX2_P E8
PCIE_UP_RX2_N F8
PCIE_UP_TX3_P A7
PCIE_UP_TX3_N B7
PCIE_UP_RX3_P D7
PCIE_UP_RX3_N E7
PCIE_UP_CLKREQ* A18
PCIE_UP_EXT_REFCLK_P G12
PCIE_UP_EXT_REFCLK_N G11
PCIE_UP_REXT G10
PCIE_DN_TX0_P AP28
PCIE_DN_TX0_N AN28
PCIE_DN_RX0_P AL28
PCIE_DN_RX0_N AK28
PCIE_DN_TX1_P AN27
PCIE_DN_TX1_N AM27
PCIE_DN_RX1_P AK27
PCIE_DN_RX1_N AJ27
PCIE_DN_TX2_P AP26
PCIE_DN_TX2_N AN26
PCIE_DN_RX2_P AL26
PCIE_DN_RX2_N AK26
PCIE_DN_TX3_P AN25
PCIE_DN_TX3_N AM25
PCIE_DN_RX3_P AK25
PCIE_DN_RX3_N AJ25
PCIE_DN_REFCLK0_P AK23
PCIE_DN_REFCLK0_N AL23
PCIE_DN_CLKREQ0* AG29
PCIE_DN_PERST0* AJ33
PCIE_DN_REFCLK1_P AJ22
PCIE_DN_REFCLK1_N AK22
PCIE_DN_CLKREQ1* AG30
PCIE_DN_PERST1* AG33
PCIE_DN_REFCLK2_P AN23
PCIE_DN_REFCLK2_N AP23
PCIE_DN_CLKREQ2* AD29
PCIE_DN_PERST2* AH29
PCIE_DN_REFCLK3_P AM22
PCIE_DN_REFCLK3_N AN22
PCIE_DN_CLKREQ3* AF33
PCIE_DN_PERST3* AE30
PCIE_DN_EXT_REFCLK_P AH25
PCIE_DN_EXT_REFCLK_N AH24
PCIE_DN_REXT AH23
NC PCIE WLAN R2D C P
NC PCIE WLAN R2D C N
NC PCIE WLAN D2R P
NC PCIE WLAN D2R N
NC PCIE ENET SOC R2D C P
NC PCIE ENET SOC R2D C N
NC PCIE ENET SOC D2R P
NC PCIE ENET SOC D2R N
TP PCIE DN2 R2D CP
TP PCIE DN2 R2D CN
TP PCIE DN2 D2RP
TP PCIE DN2 D2RN
TP PCIE DN3 R2D CP
TP PCIE DN3 R2D CN
TP PCIE DN3 D2RP
TP PCIE DN3 D2RN
NC PCIE CLK100M WLAN P
NC PCIE CLK100M WLAN N
NC WLAN CLKREQ L
NC WLAN PERST L
NC PCIE CLK100M ENET SOC P
NC PCIE CLK100M ENET SOC N
ENET CLKREQ L
NC ENET RESET L
(ENET is connected to PCH)
(UID_MODE strap on A00)
TP PCIE CLK100M DN2P
TP PCIE CLK100M DN2N
TP PCIEDN2 CLKREQ L
TP PCIEDN2 RESET L
TP PCIE CLK100M DN3P
TP PCIE CLK100M DN3N
TP PCIEDN3 CLKREQ L
TP PCIEDN3 RESET L
SOC PCIE DN REXT
R4201 3.01K 1% 1/20W MF 201
OMIT TABLE
CRITICAL
U3900
POP-1GB-20NM-M-SCK
FCCSP
TMIB21B0-B7
SYM 8 OF 17
PCIE_STG0_TX0_P AN8
PCIE_STG0_TX0_N AM8
PCIE_STG0_RX0_P AK8
PCIE_STG0_RX0_N AJ8
PCIE_STG0_TX1_P AP9
PCIE_STG0_TX1_N AN9
PCIE_STG0_RX1_P AL9
PCIE_STG0_RX1_N AK9
PCIE_STG0_TX2_P AN10
PCIE_STG0_TX2_N AM10
PCIE_STG0_RX2_P AK10
PCIE_STG0_RX2_N AJ10
PCIE_STG0_TX3_P AP11
PCIE_STG0_TX3_N AN11
PCIE_STG0_RX3_P AL11
PCIE_STG0_RX3_N AK11
PCIE_STG0_REFCLK01_P AK18
PCIE_STG0_REFCLK01_N AL18
PCIE_STG0_CLKREQ0* AM30
PCIE_STG0_CLKREQ1* AK30
PCIE_STG0_REFCLK23_P AJ19
PCIE_STG0_REFCLK23_N AK19
PCIE_STG0_CLKREQ2* AL33
PCIE_STG0_CLKREQ3* AK33
PCIE_STG0_PERST* AM32
PCIE_STG0_NANDCLK AM6
PCIE_STG0_EXT_REFCLK_P AH12
PCIE_STG0_EXT_REFCLK_N AH13
PCIE_STG0_REXT AH14
PCIE_STG1_TX0_P AN13
PCIE_STG1_TX0_N AM13
PCIE_STG1_RX0_P AK13
PCIE_STG1_RX0_N AJ13
PCIE_STG1_TX1_P AP14
PCIE_STG1_TX1_N AN14
PCIE_STG1_RX1_P AL14
PCIE_STG1_RX1_N AK14
PCIE_STG1_TX2_P AN15
PCIE_STG1_TX2_N AM15
PCIE_STG1_RX2_P AK15
PCIE_STG1_RX2_N AJ15
PCIE_STG1_TX3_P AP16
PCIE_STG1_TX3_N AN16
PCIE_STG1_RX3_P AL16
PCIE_STG1_RX3_N AK16
PCIE_STG1_REFCLK01_P AN18
PCIE_STG1_REFCLK01_N AP18
PCIE_STG1_CLKREQ0* C15
PCIE_STG1_CLKREQ1* E15
PCIE_STG1_REFCLK23_P AM19
PCIE_STG1_REFCLK23_N AN19
PCIE_STG1_CLKREQ2* E14
PCIE_STG1_CLKREQ3* D14
PCIE_STG1_PERST* AK32
PCIE_STG1_NANDCLK AM2
PCIE_STG1_EXT_REFCLK_P AH17
PCIE_STG1_EXT_REFCLK_N AH18
PCIE_STG1_REXT AH19
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PCIE SSD0 R2D C N<3>
PCIE SSD0 D2R P<3>
PCIE SSD0 D2R N<3>
PCIE CLK100M SSD0 01 P
PCIE CLK100M SSD0 01 N
SSD0 CLKREQ0 L
SSD0 CLKREQ1 L
PCIE CLK100M SSD0 23 P
PCIE CLK100M SSD0 23 N
SSD0 CLKREQ2 L
SSD0 CLKREQ3 L
SSD0 PCIE RESET L
SSD0 CLK24M R
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NC PCIE SSD1 D2R P<3>
NC PCIE SSD1 D2R N<3>
NC PCIE CLK100M SSD1 01 P
NC PCIE CLK100M SSD1 01 N
NC SSD1 CLKREQ0 L
NC SSD1 CLKREQ1 L
NC PCIE CLK100M SSD1 23 P
NC PCIE CLK100M SSD1 23 N
NC SSD1 CLKREQ2 L
NC SSD1 CLKREQ3 L
NC SSD1 PCIE RESET L
NC SSD1 CLK24M R
SOC PCIE STG0 REXT
R4250 3.01K 1% 1/20W MF 201
R4251 3.01K 1% 1/20W MF 201
PP1V8 AWAKE
R4232 47K 5% 1/20W MF 201
ENET CLKREQ L
BOM_COST_GROUP=SOC
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
SoC PCIe
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 42 OF 142
SHEET 40 OF 115
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Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3

112 105 102 PPVDDCPU_AWAKE_SOC
0.625V - 1.06V
11.6A Max

C4300 9.1UF 20% 4V CERM 0402
C4301 9.1UF 20% 4V CERM 0402
C4302 9.1UF 20% 4V CERM 0402
C4303 9.1UF 20% 4V CERM 0402
C4304 9.1UF 20% 4V CERM 0402
C4305 9.1UF 20% 4V CERM 0402
C4306 9.1UF 20% 4V CERM 0402
C4307 9.1UF 20% 4V CERM 0402
C4308 9.1UF 20% 4V CERM 0402
C4309 9.1UF 20% 4V CERM 0402
C4320 9.1UF 20% 4V CERM 0402
C4321 9.1UF 20% 4V CERM 0402
C4322 9.1UF 20% 4V CERM 0402
C4323 9.1UF 20% 4V CERM 0402
C4324 9.1UF 20% 4V CERM 0402
C4330 9.1UF 20% 4V CERM 0402
C4331 9.1UF 20% 4V CERM 0402
C4332 9.1UF 20% 4V CERM 0402
C4333 9.1UF 20% 4V CERM 0402
C4334 9.1UF 20% 4V CERM 0402

OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
TMIB21B0-B7
SYM 10 OF 17

VDD_CPU: AA12, AA14, AA16, AB11, AB13, AB15, N12, N14, N16, P11, P13, P15, R10, R12, R14, U12, U14, U16, W10, W12, W14, Y11, Y13, Y15

VDD_CPU_SRAM: AA10, N10, R16, T11, T13, T15, U10, V11, V13, V15, W16

VDD_CPU_SENSE M17
VSS_CPU_SENSE M16

C4350 9.1UF 20% 4V CERM 0402
C4351 9.1UF 20% 4V CERM 0402
C4352 9.1UF 20% 4V CERM 0402
C4353 9.1UF 20% 4V CERM 0402
C4354 9.1UF 20% 4V CERM 0402
C4357 9.1UF 20% 4V CERM 0402
C4355 9.1UF 20% 4V CERM 0402
C4356 9.1UF 20% 4V CERM 0402
C4360 9.1UF 20% 4V CERM 0402

PPVDDCPUSRAM_AWAKE 102
0.8V - 1.06V
0.9A Max

SOC_VDDCPU_SENSE 71 108
TP_SOC_VSSCPU_SENSE

112 105 102 PP0V82_SLPDDR
5.6A Max

C4370 9.1UF 20% 4V CERM 0402
C4371 9.1UF 20% 4V CERM 0402
C4372 9.1UF 20% 4V CERM 0402
C4373 9.1UF 20% 4V CERM 0402
C4380 9.1UF 20% 4V CERM 0402
C4381 9.1UF 20% 4V CERM 0402
C4385 9.1UF 20% 4V CERM 0402
C4386 9.1UF 20% 4V CERM 0402

OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
TMIB21B0-B7
SYM 11 OF 17

VDD_SOC: AC10, AC12, AC14, AC16, AC18, AC20, AC22, AC24, AD11, AD13, AD15, AD17, AD19, AD21, AD23, AD25, L10, L12, L14, L16, L18, L20, L22, L24, M11, M13, M15, M19, M21, M23, M25

VDD_SOC: R18, R20, R22, R24, T19, T21, T23, T25, W18, W20, W22, W24, Y17, Y19, Y21, Y23

VDD_SOC_SENSE Y25 TP_SOC_VDDSOC_SENSE
VSS_SENSE Y26 TP_SOC_VSSSOC_SENSE

BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
SoC Power 1

Apple Inc.

DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 43 OF 142
SHEET 41 OF 115

Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3

105 102 PP1V1_SLPDDR
0.86A Max

C4450 2.2UF 20% 4V X6S-CERM 0201
C4451 2.2UF 20% 4V X6S-CERM 0201
C4452 2.2UF 20% 4V X6S-CERM 0201
C4453 2.2UF 20% 4V X6S-CERM 0201
C4454 2.2UF 20% 4V X6S-CERM 0201
C4455 2.2UF 20% 4V X6S-CERM 0201
C4456 2.2UF 20% 4V X6S-CERM 0201
C4457 2.2UF 20% 4V X6S-CERM 0201

OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
TMIB21B0-B7
13 OF 17

C3 E3 G3 H8 J9 K8 L9 P3 R3 U3 — VDDIO11_DDR0
C33 E31 G31 H27 J26 K27 L26 P31 R31 U31 — VDDIO11_DDR1
AB3 AC9 AD3 AD8 AE3 AE9 AF8 AK3 AM3 — VDDIO11_DDR2
AA27 AB26 AB31 AC27 AD26 AD31 AE27 AE31 AK31 AM31 — VDDIO11_DDR3

VDDIO11_PLL_DDR0 H9
VDDIO11_PLL_DDR1 G26
VDDIO11_PLL_DDR2 AG8
VDDIO11_PLL_DDR3 AF26

C4460 0.22UF 20% 6.3V X6S-CERM 0201
C4461 0.22UF 20% 6.3V X6S-CERM 0201
C4462 0.22UF 20% 6.3V X6S-CERM 0201
C4463 0.22UF 20% 6.3V X6S-CERM 0201

R4460 5.1 1% 1/20W MF 0201
L4460 120-OHM-25%-0.48A-0.21DCR 0201

102 PP1V1_SLPDDR
8mA Max

PP1V1_SLPDDR_SOC_VDDIOPLLDDR_F
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.1V

VDDIO11_RET_DDR0 G4
VDDIO11_RET_DDR1 D30
VDDIO11_RET_DDR2 AJ4
VDDIO11_RET_DDR3 AJ30

C4470 2.2UF 20% 4V X6S-CERM 0201
C4471 2.2UF 20% 4V X6S-CERM 0201
C4472 2.2UF 20% 4V X6S-CERM 0201
C4473 2.2UF 20% 4V X6S-CERM 0201

PP1V1_SLPS2R
Current included in VDD2

105 102 PP0V9_SLPDDR
1.9A Max

C4400 9.1UF 20% 4V CERM 0402
C4401 9.1UF 20% 4V CERM 0402
C4402 9.1UF 20% 4V CERM 0402
C4405 9.1UF 20% 4V CERM 0402
C4406 9.1UF 20% 4V CERM 0402
C4410 9.1UF 20% 4V CERM 0402
C4411 9.1UF 20% 4V CERM 0402

U3900
POP-1GB-20NM-M-SCK
FCCSP
TMIB21B0-B7
SYM 12 OF 17

OMIT_TABLE
CRITICAL

AA18 AA20 AA22 AA24 AB17 AB19 AB21 AB23 AB25 AE10 AE12 AE14 AE16 AE18 AE20 AE22 AE24 AE26 AG9 J10 J12 J14 J16 J18 J20 J22 J24 K11 K13 K15 K17 K19 — VDD_FIXED

K21 K23 K25 N18 N20 N22 N24 P17 P19 P21 P23 P25 U18 U20 U22 U24 V19 V21 V23 V25 — VDD_FIXED

9mA Max
102 PP0V9_SLPDDR — U17 — VDD_FIXED_CPU
102 PP0V9_SLPDDR — G19 — VDD_FIXED_USB
5mA Max

102 PP0V9_SLPDDR
25mA Max
C4420 9.1UF 20% 4V CERM 0402
H20 H22 H24 — VDD_FIXED_MIPI

M9 P9 T9 V9 Y9 — VDD_LOW

102 PP0V8_SLPS2R
102mA Max
C4423 2.2UF 20% 4V X6S-CERM 0201

H10 H12 H14 — VDD_FIXED_UP_PCIE_ANA
H13 J11 J13 — VDD_FIXED_UP_PCIE_CLK

102 42 PP0V9_SLPDDR
330mA Max
C4425 9.1UF 20% 4V CERM 0402
C4426 9.1UF 20% 4V CERM 0402

VDD_FIXED_STG0_PCIE_ANA AG11 AG12 AG14
VDD_FIXED_STG0_PCIE_CLK AF11 AF13 AF15
VDD_FIXED_STG1_PCIE_ANA AG16 AG18 AG20
VDD_FIXED_STG1_PCIE_CLK AF17 AF19 AG15
VDD_FIXED_DN_PCIE_ANA AG23 AG24 AG26
VDD_FIXED_DN_PCIE_CLK AF23 AF24 AF25
VDD_FIXED_PCIE_REFBUF AE13 AE19 AE23 AF21 AG22

PP0V9_SLPDDR
330mA Max
C4430 9.1UF 20% 4V CERM 0402
C4431 9.1UF 20% 4V CERM 0402

PP0V9_SLPDDR
330mA Max
C4435 9.1UF 20% 4V CERM 0402
C4436 9.1UF 20% 4V CERM 0402

PP0V9_SLPDDR
330mA Max
C4440 9.1UF 20% 4V CERM 0402
C4441 9.1UF 20% 4V CERM 0402

C4445 9.1UF 20% 4V CERM 0402

PP0V9_SLPDDR_SOC_PCIEREFBUF
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=0.9V

R4445 0 5% 1/20W MF 0201

PP0V9_SLPDDR
45mA Max

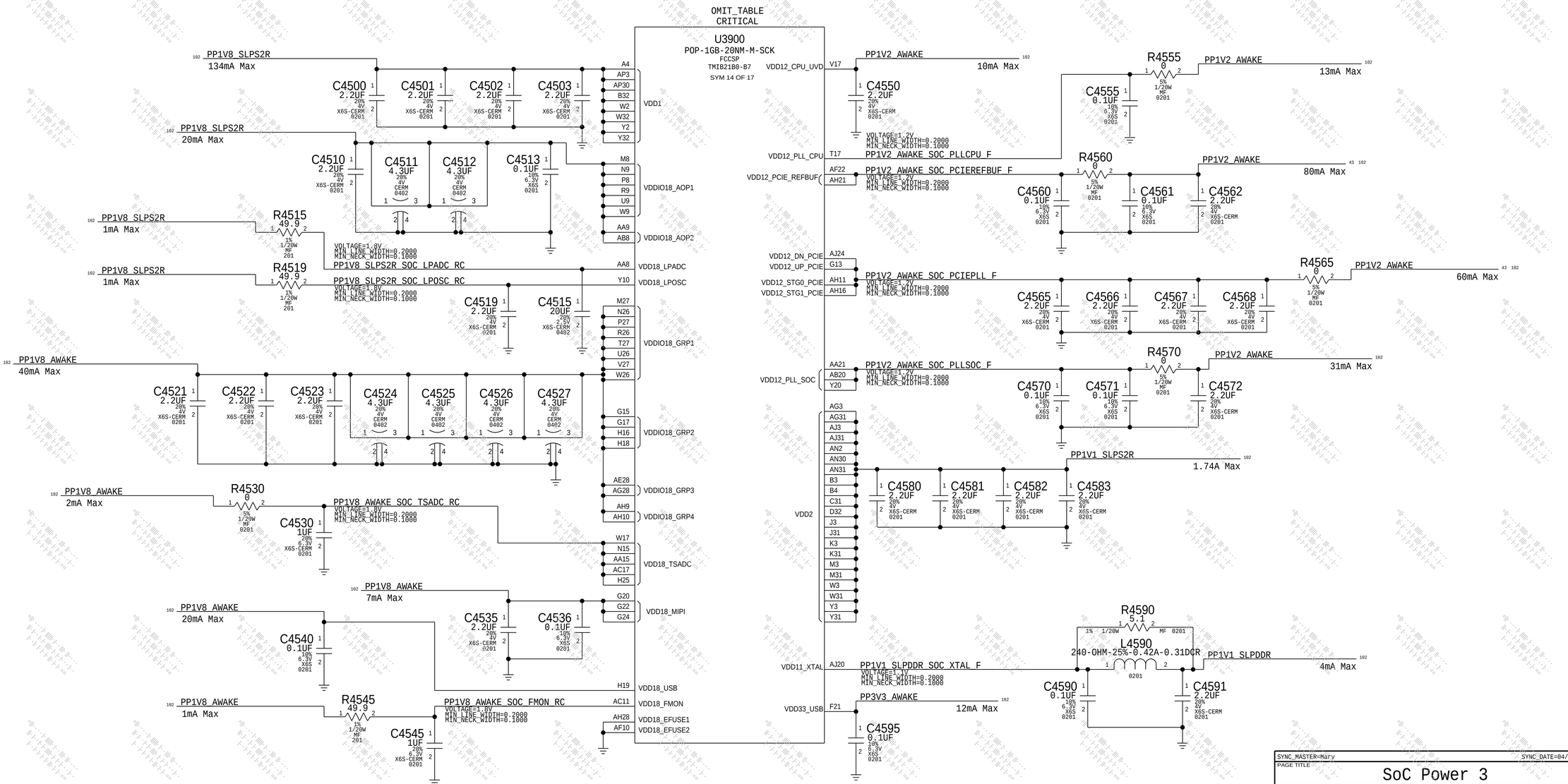
BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018
PAGE TITLE: SoC Power 2

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 44 OF 142
SHEET 42 OF 115

Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3

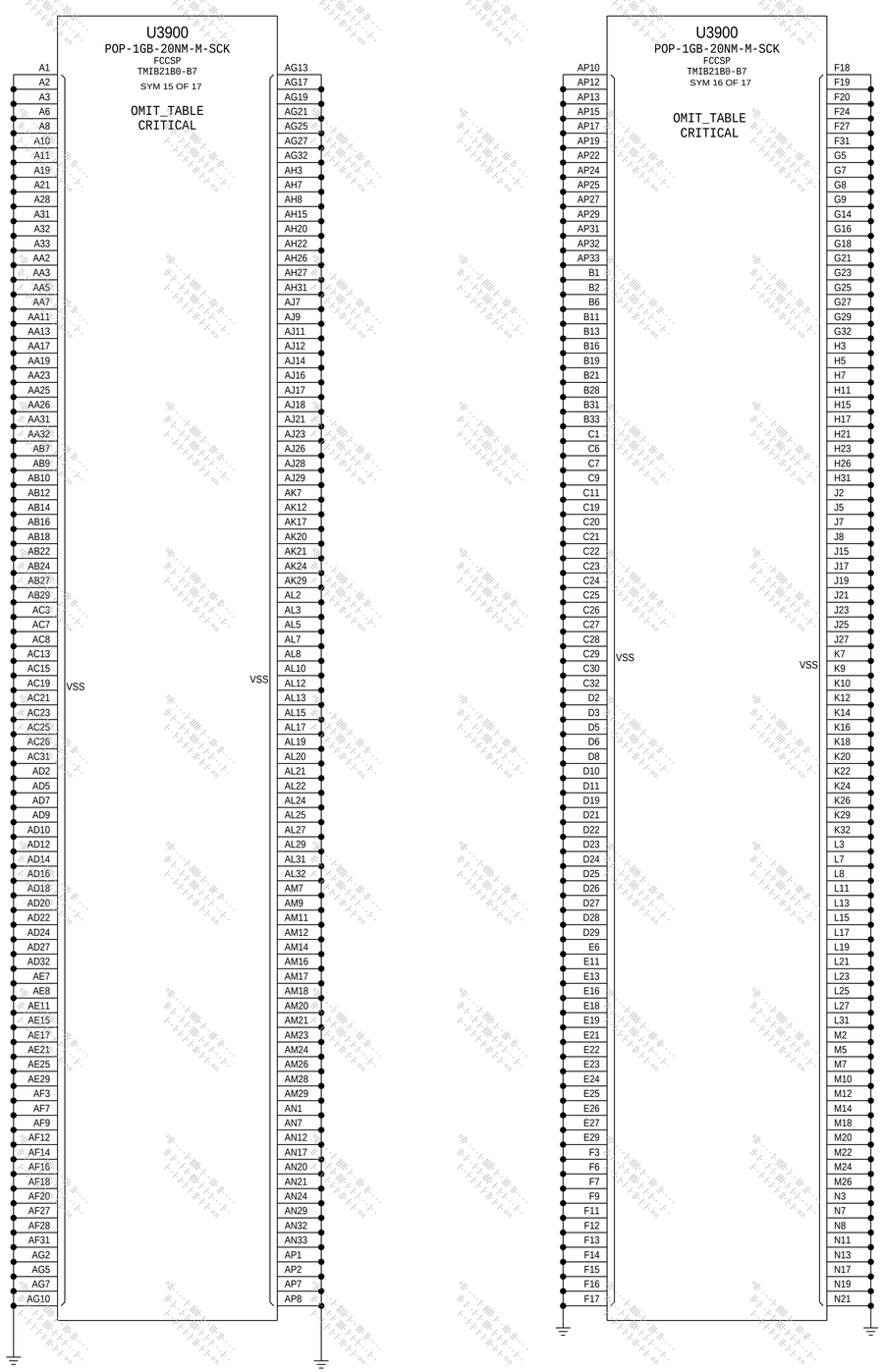


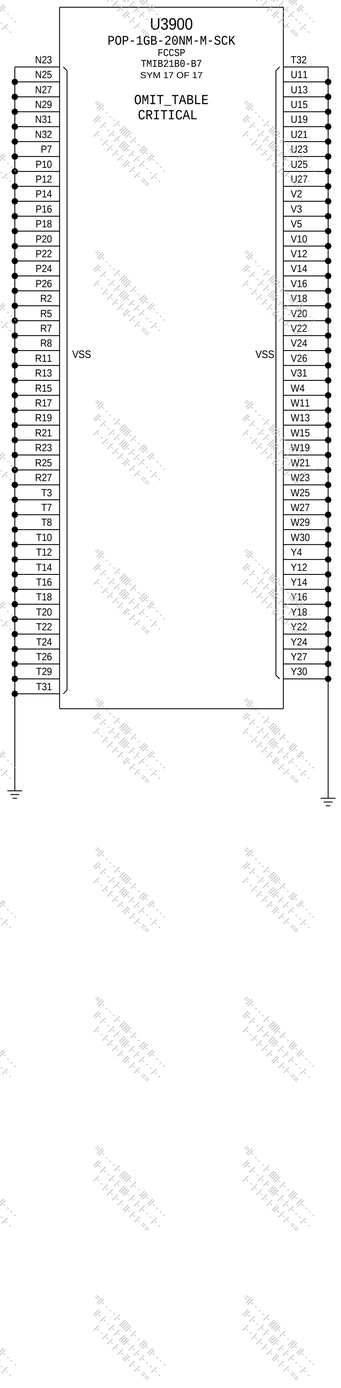
SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: SoC Power 3

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 45 OF 142
SHEET: 43 OF 115





SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

SoC Ground

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

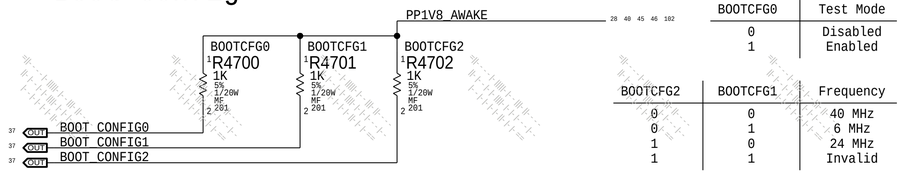
BRANCH dvt-1

PAGE 46 OF 142

SHEET 44 OF 115

BOM_COST_GROUP=SOC

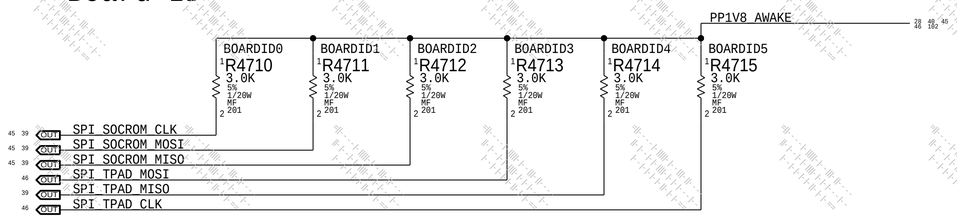
Boot Config



BOOTCFG0	Test Mode
0	Disabled
1	Enabled

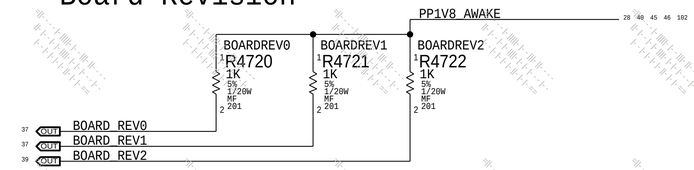
BOOTCFG2	BOOTCFG1	Frequency
0	0	40 MHz
0	1	6 MHz
1	0	24 MHz
1	1	Invalid

Board ID



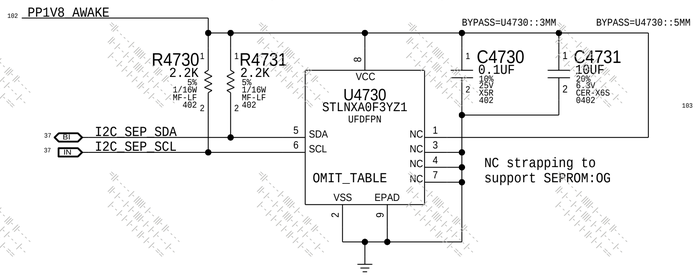
See <rdar://31977435> for project assignments

Board Revision



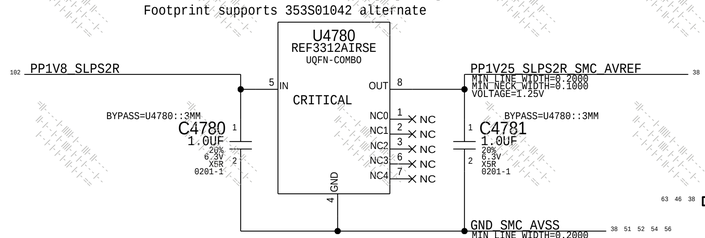
SEP EEPROM

STLNX: (Write: 0xE2, Read 0xE3)
OG: (Write: 0xA2, Read 0xA3)

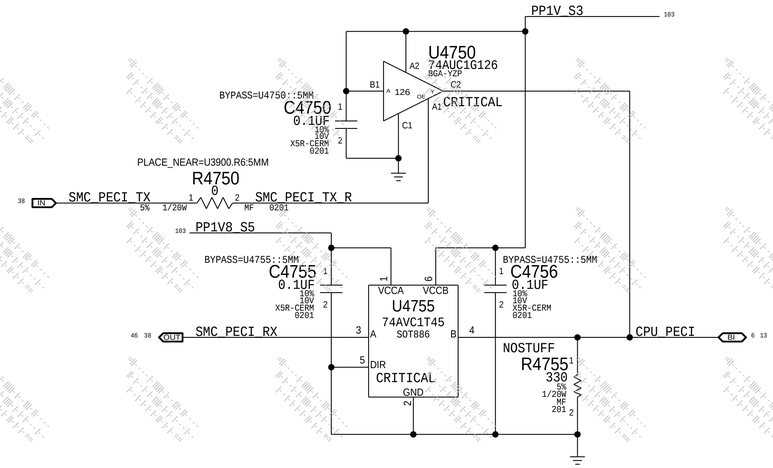


SMC AVREF Supply

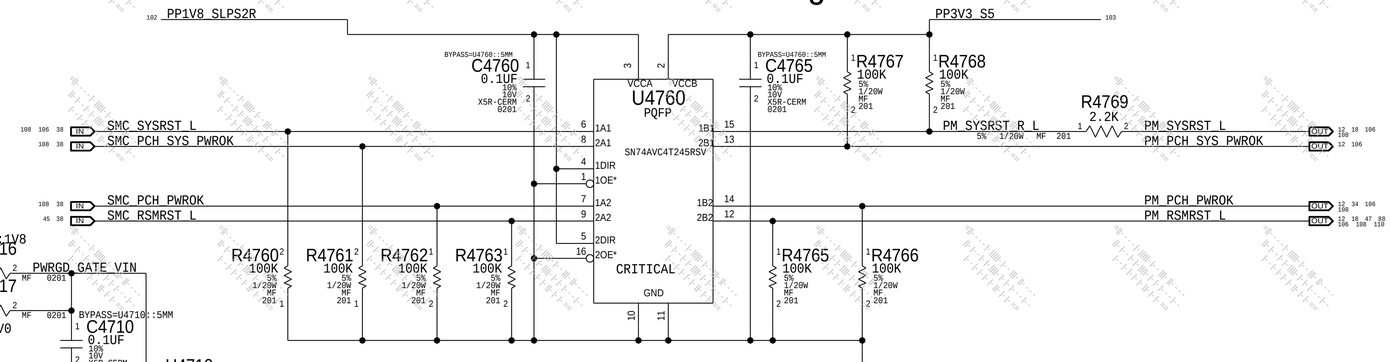
Footprint supports 353S01042 alternate



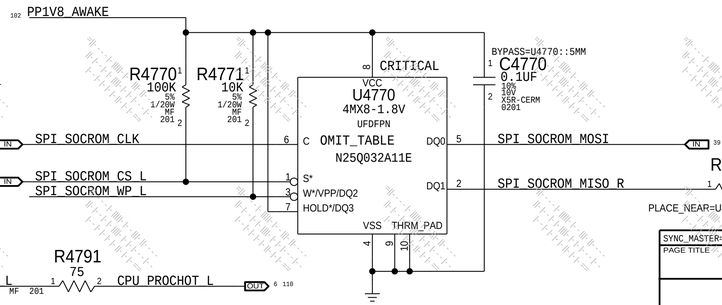
PECI Level Shifting



PCH PM Level Shifting

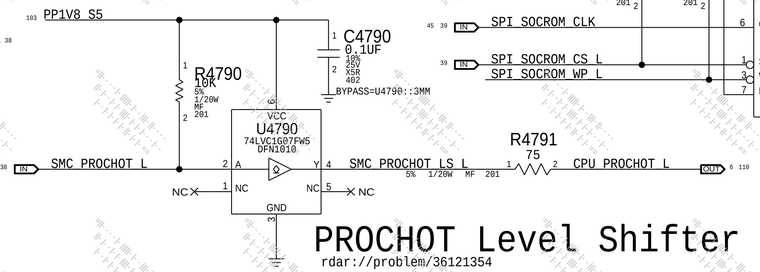


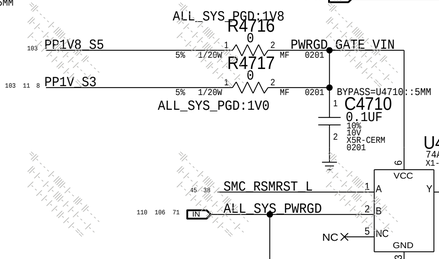
SoC ROM



PROCHOT Level Shifter

rdar://problem/36121354





SYNC_MASTER=Mary	SYNC_DATE=04/26/2018
PAGE TITLE	SoC Shared Support
Apple Inc.	DRAWING NUMBER 051-02424 · SIZE D
	REVISION 6.0.0
	BRANCH dvt-1
	PAGE 47 OF 142
	SHEET 45 OF 115

BOM_COST_GROUP=SOC

PCIe Up R2D AC Caps

(All Caps)

GND_VOID=TRUE

PCIE_SOC_R2D_C_P<0>	C4820	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_P<0>			
PCIE_SOC_R2D_C_N<0>	C4821	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_N<0>			
PCIE_SOC_R2D_C_P<1>	C4822	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_P<1>			
PCIE_SOC_R2D_C_N<1>	C4823	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_N<1>			
PCIE_SOC_R2D_C_P<2>	C4824	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_P<2>			
PCIE_SOC_R2D_C_N<2>	C4825	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_N<2>			
PCIE_SOC_R2D_C_P<3>	C4826	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_P<3>			
PCIE_SOC_R2D_C_N<3>	C4827	0.22UF	20%	6.3V	X5R	0201	PCIE_SOC_R2D_N<3>			

GPIO Source Termination

I2S_SPKRAMP_R2D_R	R4843	33	5%	1/20W	MF	201	I2S_SPKRAMP_R2D	PLACE_NEAR=U3900.AC32:5MM		
I2S_SPKRAMP_BCLK_R	R4844	33	5%	1/20W	MF	201	I2S_SPKRAMP_BCLK	PLACE_NEAR=U3900.Y20:5MM		
I2S_SPKRAMP_LRCLK_R	R4865	33	5%	1/20W	MF	201	I2S_SPKRAMP_LRCLK	PLACE_NEAR=U3900.AE32:5MM		
I2S_CODEC_R2D_R	R4847	33	5%	1/20W	MF	201	I2S_CODEC_R2D	PLACE_NEAR=U3900.AA33:5MM		
I2S_CODEC_BCLK_R	R4848	33	5%	1/20W	MF	201	I2S_CODEC_BCLK	PLACE_NEAR=U3900.AE33:5MM		
I2S_CODEC_D2R	R4863	33	5%	1/20W	MF	201	I2S_CODEC_D2R_RR	PLACE_NEAR=U3900.Y33:5MM		
I2S_CODEC_LRCLK_R	R4864	33	5%	1/20W	MF	201	I2S_CODEC_LRCLK	PLACE_NEAR=U3900.V29:5MM		
I2S_SPKRAMP_D2R	R4852	0	5%	1/20W	MF	0201	I2S_SPKRAMP_D2R_RR	PLACE_NEAR=U3900.Y28:5MM		
SPI_TPAD_MOSI							SPI_TPAD_MOSI	MAKE_BASE=TRUE		
SPI_TPAD_CLK							SPI_TPAD_CLK	MAKE_BASE=TRUE		
SSD0_CLK24M_R	R4857	20	5%	1/20W	MF	201	SSD0_CLK24M	PLACE_NEAR=U3900.AM6:5MM		

Misc Alias

CODEC_INT_L	CODEC_INT_L	MAKE_BASE=TRUE	
CODEC_WAKE_L	CODEC_WAKE_L	MAKE_BASE=TRUE	
CODEC_RESET_L	CODEC_RESET_L	MAKE_BASE=TRUE	
DP2HDMI_AOP_VDD12ON	DP2HDMI_AOP_VDD12ON	MAKE_BASE=TRUE	
SMC_LED_ONEWIRE	R4858 0 0201 1/20W 5% MF	SYS_LED	
TP_SMC_DEBUG	TP_SMC_DEBUG	MAKE_BASE=TRUE	
PSU11VOC_WAKE_L	PSU11VOC_WAKE_L	MAKE_BASE=TRUE	
SMC_GFX_THROTTLE_L	SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	
LIDINT_L_UARTHDD_D2R	LIDINT_L_UARTHDD_D2R	MAKE_BASE=TRUE	
PSU_P12V_EN_L	R4859 0 0201 1/20W 5% MF	SPI_DP2HDMI_HOLD	SPIHOLD:H9M
SWD_SOC_SWCLK	R4800 33 5% 1/20W MF 201	DBGMUX_SWD_SOC_CLK	
SWD_SOC_SWDIO	R4801 33 5% 1/20W MF 201	DBGMUX_SWD_SOC_IO	

Rdar://34600168

PP1V8_SLPS2R							
PP1V8_AWAKE							
R4883	47K	5%	1/20W	MF	201	SSD0_CLKREQ0_L	
R4884	47K	5%	1/20W	MF	201	SSD0_CLKREQ1_L	
R4887	47K	5%	1/20W	MF	201	SSD0_CLKREQ2_L	
R4888	47K	5%	1/20W	MF	201	SSD0_CLKREQ3_L	
R4885	100K	5%	1/20W	MF	201	SSD0_PCIE_RESET_L	
R4886	47K	5%	1/20W	MF	201	SSD0_CLK24M	
R4889	100K	5%	1/20W	MF	201	NC_PDM_DMIC_DATA0	NOSTUFF
R4890	100K	5%	1/20W	MF	201	NC_PDM_DMIC_DATA1	NOSTUFF
R4895	100K	5%	1/20W	MF	201	SSD_PMU_RESET_L	

R4845	100K	NOSTUFF	5%	1/20W	MF	201	I2S_SPKRAMP_R_R2D_R
R4846	100K	NOSTUFF	5%	1/20W	MF	201	I2S_SPKRAMP_R_BCLK_R
R4866	100K	NOSTUFF	5%	1/20W	MF	201	I2S_SPKRAMP_R_D2R
R4867	100K	NOSTUFF	5%	1/20W	MF	201	I2S_SPKRAMP_R_LRCLK

SMC (Fast) ADC Assignments

P12VIN_V	SMC_P12VIN_VSENSE	SMC_P12VIN_VSENSE	
P12VIN_I	SMC_P12VIN_ISENSE	SMC_P12VIN_ISENSE	
CPU_HS_I	SMC_CPU_HI_ISENSE	SMC_CPU_HI_ISENSE	
CPUCORE_I	SMC_CPU_VCC_ISENSE	SMC_CPU_VCC_ISENSE	
CPUCORE_V	SMC_CPU_VCC_VSENSE	SMC_CPU_VCC_VSENSE	
CPUGT_V	SMC_CPUGT_VSENSE	SMC_CPUGT_VSENSE	
CPUGT_I	SMC_CPUGT_ISENSE	SMC_CPUGT_ISENSE	
1V2_S3_I	SMC_P1V2_ISENSE	SMC_P1V2_ISENSE	

Calpe (Slow) ADC Assignments

PMU_VDD_I	PMU_P3V3_CAPLE_ISENSE	PMU_P3V3_CAPLE_ISENSE	
CPUSA_I	PMU_CPUSA_ISENSE	PMU_CPUSA_ISENSE	
DDR2V5_I	PMU_DDR2V5_ISENSE	PMU_DDR2V5_ISENSE	
VCCIO_I	PMU_VCCIO_ISENSE	PMU_VCCIO_ISENSE	
P5V_G3S_HS_I(12V)	PMU_P5V_G3S_HI_ISENSE	PMU_P5V_G3S_HI_ISENSE	
CPUSA_V	PMU_CPUSA_VSENSE	PMU_CPUSA_VSENSE	
USBC_5V_I	PMU_P5V_USBC_ISENSE	PMU_P5V_USBC_ISENSE	
USBA_5V_I	PMU_P5V_USBA_ISENSE	PMU_P5V_USBA_ISENSE	
TBT_3V3_I	PMU_P3V3_TBT_ISENSE	PMU_P3V3_TBT_ISENSE	
SSD0_3V3_I	PMU_P3V3_SSD0_ISENSE	PMU_P3V3_SSD0_ISENSE	
SSD0_12V_I	PMU_PBUS_SSD0_ISENSE	PMU_PBUS_SSD0_ISENSE	
P3V3_G3H_HS_I(12V)	PMU_P3V3_G3H_HI_ISENSE	PMU_P3V3_G3H_HI_ISENSE	
P3V3_G3S_WLANBT_I	PMU_P3V3_WLANBT_ISENSE	PMU_P3V3_WLANBT_ISENSE	
P3V3_ENET_I	PMU_P3V3_ENET_ISENSE	PMU_P3V3_ENET_ISENSE	
P12_ENET_I	PMU_P12V_ENET_ISENSE	PMU_P12V_ENET_ISENSE	

All: MAKE_BASE=TRUE

WLAN connects to PCH

NC_PCIE_WLAN_R2D_C_P	NC_PCIE_WLAN_R2D_C_P	MAKE_BASE=TRUE
NC_PCIE_WLAN_R2D_C_N	NC_PCIE_WLAN_R2D_C_N	MAKE_BASE=TRUE
NC_PCIE_WLAN_D2R_P	NC_PCIE_WLAN_D2R_P	MAKE_BASE=TRUE
NC_PCIE_WLAN_D2R_N	NC_PCIE_WLAN_D2R_N	MAKE_BASE=TRUE

ENET connects to PCH

NC_PCIE_ENET_SOC_R2D_C_P	NC_PCIE_ENET_SOC_R2D_C_P	MAKE_BASE=TRUE
NC_PCIE_ENET_SOC_R2D_C_N	NC_PCIE_ENET_SOC_R2D_C_N	MAKE_BASE=TRUE
NC_PCIE_ENET_SOC_D2R_P	NC_PCIE_ENET_SOC_D2R_P	MAKE_BASE=TRUE
NC_PCIE_ENET_SOC_D2R_N	NC_PCIE_ENET_SOC_D2R_N	MAKE_BASE=TRUE

NC_SPKR_ID1	NC_SPKR_ID1	
NC_SPKR_ID0	NC_SPKR_ID0	MAKE_BASE=TRUE
NC_SMC_FAN_1_PWM	NC_SMC_FAN_1_PWM	MAKE_BASE=TRUE
NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE
NC_WLAN_PERST_L	NC_WLAN_PERST_L	MAKE_BASE=TRUE
NC_WLAN_CLKREQ_L	NC_WLAN_CLKREQ_L	MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE

No MIPI

GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE
GND		MAKE_BASE=TRUE

NC_ENET_RESET_L	NC_ENET_RESET_L	
NC_UART_GNSS_D2R_CTS_L	NC_UART_GNSS_D2R_CTS_L	MAKE_BASE=TRUE
NC_UART_GNSS_R2D_RTS_L	NC_UART_GNSS_R2D_RTS_L	MAKE_BASE=TRUE
NC_UART_SE_D2R	NC_UART_SE_D2R	MAKE_BASE=TRUE
NC_UART_SE_R2D	NC_UART_SE_R2D	MAKE_BASE=TRUE
NC_UART_SE_D2R_CTS_L	NC_UART_SE_D2R_CTS_L	MAKE_BASE=TRUE
NC_UART_SE_R2D_RTS_L	NC_UART_SE_R2D_RTS_L	MAKE_BASE=TRUE
NC_PCIE_CLK100M_WLAN_P	NC_PCIE_CLK100M_WLAN_P	MAKE_BASE=TRUE
NC_PCIE_CLK100M_WLAN_N	NC_PCIE_CLK100M_WLAN_N	MAKE_BASE=TRUE
NC_PCIE_CLK100M_ENET_SOC_P	NC_PCIE_CLK100M_ENET_SOC_P	MAKE_BASE=TRUE
NC_PCIE_CLK100M_ENET_SOC_N	NC_PCIE_CLK100M_ENET_SOC_N	MAKE_BASE=TRUE
NC_PCIE_CLK100M_SSD1_01_P	NC_PCIE_CLK100M_SSD1_01_P	MAKE_BASE=TRUE
NC_PCIE_CLK100M_SSD1_01_N	NC_PCIE_CLK100M_SSD1_01_N	MAKE_BASE=TRUE
NC_PCIE_CLK100M_SSD1_23_P	NC_PCIE_CLK100M_SSD1_23_P	MAKE_BASE=TRUE
NC_PCIE_CLK100M_SSD1_23_N	NC_PCIE_CLK100M_SSD1_23_N	MAKE_BASE=TRUE
NC_SSD1_CLKREQ0_L	NC_SSD1_CLKREQ0_L	MAKE_BASE=TRUE
NC_SSD1_CLKREQ1_L	NC_SSD1_CLKREQ1_L	MAKE_BASE=TRUE
NC_SSD1_CLKREQ2_L	NC_SSD1_CLKREQ2_L	MAKE_BASE=TRUE
NC_SSD1_CLKREQ3_L	NC_SSD1_CLKREQ3_L	MAKE_BASE=TRUE
NC_SSD1_PCIE_RESET_L	NC_SSD1_PCIE_RESET_L	MAKE_BASE=TRUE
NC_SSD1_CLK24M_R	NC_SSD1_CLK24M_R	MAKE_BASE=TRUE
NC_DFR_TOUCH_RSVD	NC_DFR_TOUCH_RSVD	MAKE_BASE=TRUE

(WIFI is connected to PCH)

(ENET is connected to PCH)

No SSD on Port 1

SoC NC Pins

NC_PLCAM_TX_THROTTLE	NC_PLCAM_TX_THROTTLE	
NC_GNSS_HOST_TIME	NC_GNSS_HOST_TIME	MAKE_BASE=TRUE
NC_GNSS_DEV_WAKE	NC_GNSS_DEV_WAKE	MAKE_BASE=TRUE
NC_SE_CTLR_FW_DWLD	NC_SE_CTLR_FW_DWLD	MAKE_BASE=TRUE
NC_MESA_INT	NC_MESA_INT	MAKE_BASE=TRUE
NC_MESA_PWR_EN	NC_MESA_PWR_EN	MAKE_BASE=TRUE
NC_WLAN_DEV_WAKE	NC_WLAN_DEV_WAKE	MAKE_BASE=TRUE
NC_TPAD_SPI_EN	NC_TPAD_SPI_EN	MAKE_BASE=TRUE
NC_SE_DEV_WAKE	NC_SE_DEV_WAKE	MAKE_BASE=TRUE
NC_DFR_DISP_INT	NC_DFR_DISP_INT	MAKE_BASE=TRUE
NC_DFR_PWR_EN	NC_DFR_PWR_EN	MAKE_BASE=TRUE
NC_SEP_CAM_DISABLE_L	NC_SEP_CAM_DISABLE_L	MAKE_BASE=TRUE
NC_SEP_DMIC_DISABLE_L	NC_SEP_DMIC_DISABLE_L	MAKE_BASE=TRUE
NC_SEP_DISABLE_STROBE	NC_SEP_DISABLE_STROBE	MAKE_BASE=TRUE
NC_SPI_DESCRIPTOR_OVERRIDE_L	NC_SPI_DESCRIPTOR_OVERRIDE_L	MAKE_BASE=TRUE
NC_GYRO_INT1	NC_GYRO_INT1	MAKE_BASE=TRUE
NC_GYRO_INT2	NC_GYRO_INT2	MAKE_BASE=TRUE
NC_SPI_GYRO_CS_L	NC_SPI_GYRO_CS_L	MAKE_BASE=TRUE
NC_ALTIMETER_INT	NC_ALTIMETER_INT	MAKE_BASE=TRUE
NC_SPI_ALTIMETER_CS_L	NC_SPI_ALTIMETER_CS_L	MAKE_BASE=TRUE
NC_I2S_CODEC_MCLK	NC_I2S_CODEC_MCLK	MAKE_BASE=TRUE
NC_PDM_DMIC_CLK0_R	NC_PDM_DMIC_CLK0_R	
NC_PDM_DMIC_CLK1_R	NC_PDM_DMIC_CLK1_R	MAKE_BASE=TRUE
NC_PLCAM_PROX_INT_L	NC_PLCAM_PROX_INT_L	MAKE_BASE=TRUE
NC_PLCAM_ROMEO_B2B_DETECT	NC_PLCAM_ROMEO_B2B_DETECT	MAKE_BASE=TRUE
NC_DFR_TOUCH_INT_L	NC_DFR_TOUCH_INT_L	MAKE_BASE=TRUE
NC_SMC_GFX_SELF_THROTTLE	NC_SMC_GFX_SELF_THROTTLE	MAKE_BASE=TRUE
NC_PDM_DMIC_DATA0	NC_PDM_DMIC_DATA0	MAKE_BASE=TRUE
NC_PDM_DMIC_DATA1	NC_PDM_DMIC_DATA1	MAKE_BASE=TRUE
NC_SMC_TOPBLK_SWP_L	NC_SMC_TOPBLK_SWP_L	MAKE_BASE=TRUE
NC_SPI_AOP_SENSOR_MOSI_R	NC_SPI_AOP_SENSOR_MOSI_R	MAKE_BASE=TRUE
NC_SPI_AOP_SENSOR_CLK_R	NC_SPI_AOP_SENSOR_CLK_R	MAKE_BASE=TRUE
NC_SPI_AOP_SENSOR_MISO	NC_SPI_AOP_SENSOR_MISO	MAKE_BASE=TRUE
NC_PCIE_SSD1_R2D_C_P<0>	NC_PCIE_SSD1_R2D_C_P<0>	MAKE_BASE=TRUE
NC_PCIE_SSD1_R2D_C_N<0>	NC_PCIE_SSD1_R2D_C_N<0>	MAKE_BASE=TRUE
NC_PCIE_SSD1_R2D_C_P<1>	NC_PCIE_SSD1_R2D_C_P<1>	MAKE_BASE=TRUE
NC_PCIE_SSD1_R2D_C_N<1>	NC_PCIE_SSD1_R2D_C_N<1>	MAKE_BASE=TRUE
NC_PCIE_SSD1_R2D_C_P<2>	NC_PCIE_SSD1_R2D_C_P<2>	MAKE_BASE=TRUE
NC_PCIE_SSD1_R2D_C_N<2>	NC_PCIE_SSD1_R2D_C_N<2>	MAKE_BASE=TRUE
NC_PCIE_SSD1_R2D_C_P<3>	NC_PCIE_SSD1_R2D_C_P<3>	MAKE_BASE=TRUE
NC_PCIE_SSD1_R2D_C_N<3>	NC_PCIE_SSD1_R2D_C_N<3>	MAKE_BASE=TRUE
NC_PCIE_SSD1_D2R_P<0>	NC_PCIE_SSD1_D2R_P<0>	MAKE_BASE=TRUE
NC_PCIE_SSD1_D2R_N<0>	NC_PCIE_SSD1_D2R_N<0>	MAKE_BASE=TRUE
NC_PCIE_SSD1_D2R_P<1>	NC_PCIE_SSD1_D2R_P<1>	MAKE_BASE=TRUE
NC_PCIE_SSD1_D2R_N<1>	NC_PCIE_SSD1_D2R_N<1>	MAKE_BASE=TRUE
NC_PCIE_SSD1_D2R_P<2>	NC_PCIE_SSD1_D2R_P<2>	MAKE_BASE=TRUE
NC_PCIE_SSD1_D2R_N<2>	NC_PCIE_SSD1_D2R_N<2>	MAKE_BASE=TRUE
NC_PCIE_SSD1_D2R_P<3>	NC_PCIE_SSD1_D2R_P<3>	MAKE_BASE=TRUE
NC_PCIE_SSD1_D2R_N<3>	NC_PCIE_SSD1_D2R_N<3>	MAKE_BASE=TRUE
NC_SSD1_SWCLK_UART_R2D	NC_SSD1_SWCLK_UART_R2D	MAKE_BASE=TRUE
NC_SSD1_SWDIO_UART_D2R	NC_SSD1_SWDIO_UART_D2R	MAKE_BASE=TRUE
NC_SPI_MESA_MISO	NC_SPI_MESA_MISO	MAKE_BASE=TRUE
NC_SPI_MESA_MOSI_R	NC_SPI_MESA_MOSI_R	MAKE_BASE=TRUE
NC_SPI_MESA_CLK_R	NC_SPI_MESA_CLK_R	MAKE_BASE=TRUE
NC_SPI_DFR_MISO	NC_SPI_DFR_MISO	MAKE_BASE=TRUE
NC_SPI_DFR_MOSI_R	NC_SPI_DFR_MOSI_R	MAKE_BASE=TRUE
NC_SPI_DFR_CLK_R	NC_SPI_DFR_CLK_R	MAKE_BASE=TRUE
NC_SPI_DFR_CS_L	NC_SPI_DFR_CS_L	MAKE_BASE=TRUE
NC_SDCONN_STATE_CHANGE_L	NC_SDCONN_STATE_CHANGE_L	MAKE_BASE=TRUE
NC_DFR_TOUCH_RESET_L	NC_DFR_TOUCH_RESET_L	MAKE_BASE=TRUE
NC_DFR_TOUCH_CLK32K_RESET_L	NC_DFR_TOUCH_CLK32K_RESET_L	MAKE_BASE=TRUE
NC_DFR_DISP_TE	NC_DFR_DISP_TE	MAKE_BASE=TRUE
NC_FTCAM_CLK12M_R	NC_FTCAM_CLK12M_R	
NC_FTCAM_RESET_L	NC_FTCAM_RESET_L	MAKE_BASE=TRUE
NC_PLCAM_RX_CLK12M_R	NC_PLCAM_RX_CLK12M_R	MAKE_BASE=TRUE
NC_PLCAM_RX_RESET_L	NC_PLCAM_RX_RESET_L	MAKE_BASE=TRUE
NC_DFR_DISP_RESET_L	NC_DFR_DISP_RESET_L	MAKE_BASE=TRUE
NC_PLCAM_TX_CLK12M_R	NC_PLCAM_TX_CLK12M_R	MAKE_BASE=TRUE
NC_PLCAM_TX_RESET_L	NC_PLCAM_TX_RESET_L	MAKE_BASE=TRUE
NC_PLCAM_TX_INT	NC_PLCAM_TX_INT	MAKE_BASE=TRUE
NC_PCHROM_SW_EN	NC_PCHROM_SW_EN	MAKE_BASE=TRUE
NC_MESA_MENUKEY_L	NC_MESA_MENUKEY_L	MAKE_BASE=TRUE
NC_I2S_HAWKING_D2R	NC_I2S_HAWKING_D2R	MAKE_BASE=TRUE
NC_I2S_CODEC1_R2D_R	NC_I2S_CODEC1_R2D_R	MAKE_BASE=TRUE
NC_I2S_HAWKING_BCLK_R	NC_I2S_HAWKING_BCLK_R	MAKE_BASE=TRUE
NC_I2S_HAWKING_LRCLK	NC_I2S_HAWKING_LRCLK	MAKE_BASE=TRUE
NC_I2S_SPKRAMP_MCLK_R	NC_I2S_SPKRAMP_MCLK_R	MAKE_BASE=TRUE
NC_SPI_TPAD_CS_L	NC_SPI_TPAD_CS_L	MAKE_BASE=TRUE
NC_DISP_GCON_INT_L	NC_DISP_GCON_INT_L	MAKE_BASE=TRUE

NFC FW downlaod req

T151 Interrupt

NFC/SE device wake

No FaceTime Cam

No Digital Mic

No Altimeter

No GPU

Only for MAF

No Accelerometer

No SSD on Port 1

No GMUX GPIO

SMC_PROCHOT_L — P3MM_SM_1 — PP4800

SMC_PECI_RX — P3MM_SM_1 — PP4801

BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: SoC Project Support

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

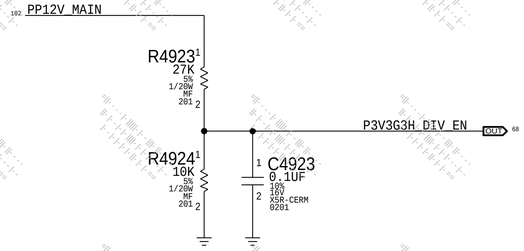
PAGE: 48 OF 142

SHEET: 46 OF 115

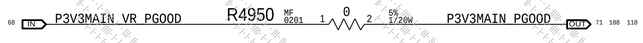
G3H

12V_G3H uses ACDC

3V3_G3H is enabled by PMIC.PVDDMAIN_EN - this is only applied for laptop Big current G3H.
On desktop,3V3_G3H should be enabled by 12V.

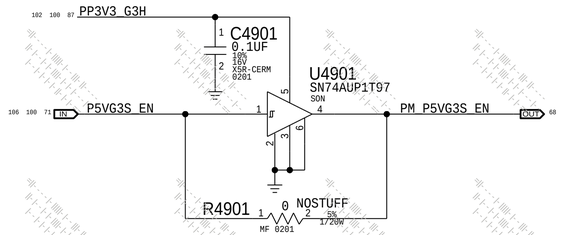


3V3_G3H_PGOOD is to PMIC.GPIO

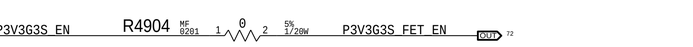


G3S - static timing by PMU

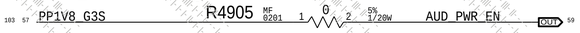
P5V_G3S is enabled by PMIC.GPIO



P3V3_G3S is enabled by PMIC.GPIO



P1V8_G3S is through BUCK3_SW4.



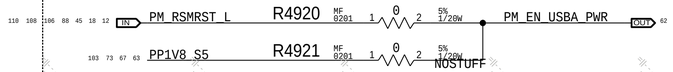
S5 - static timing by PMU

3V3_S5 uses PMU SW

1V8_S5 uses PMU SW

1V05_S5 uses PMU SW

USB-A - HW sequencing

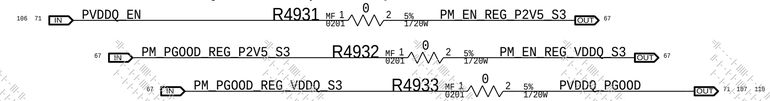


S3

1V2_S3 sequencing

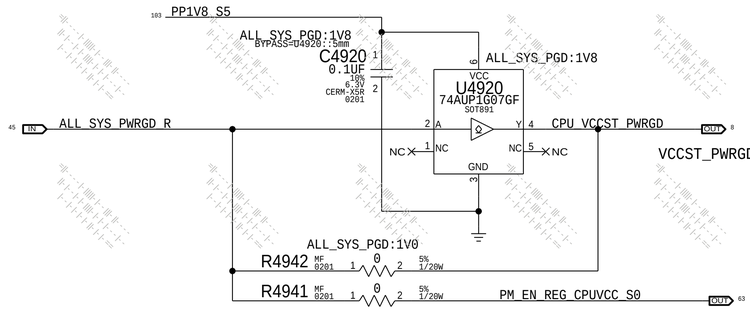
Calpe VDDQ_EN -> 2V5_VTT -> 2V5_PGOOD -> Enable 1V2 VDDQ -> VDDQ_PGDDD

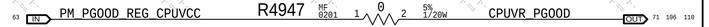
DDR4 Requirement:
VPP > VDDQ at all times
=> Ensure VPP discharges more slowly than VDDQ

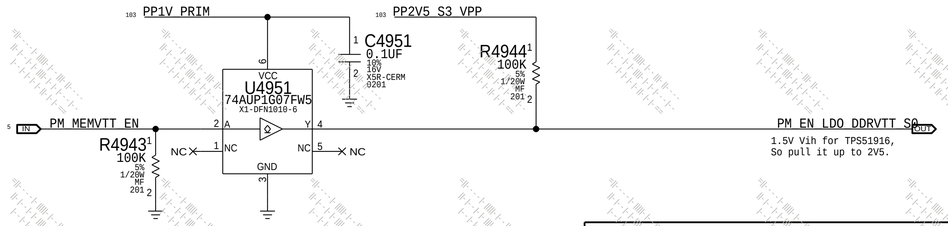


1V05_S3 uses PMU SW

S0 CPU - HW + PMU sequencing







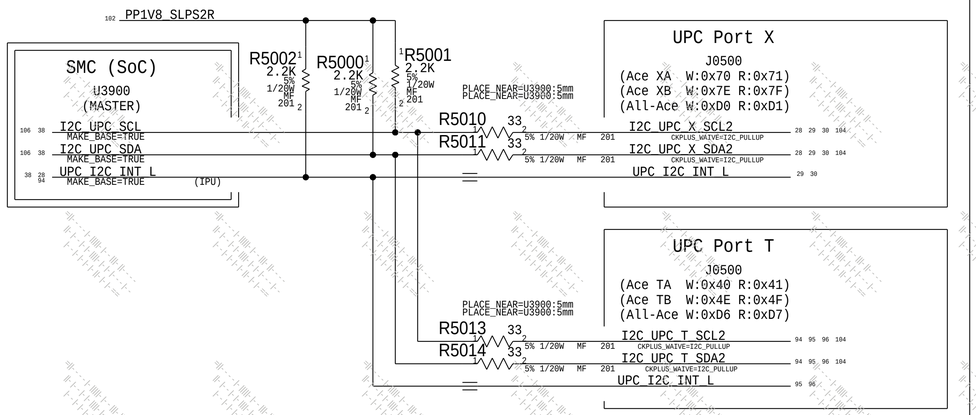
BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: Power Sequencing

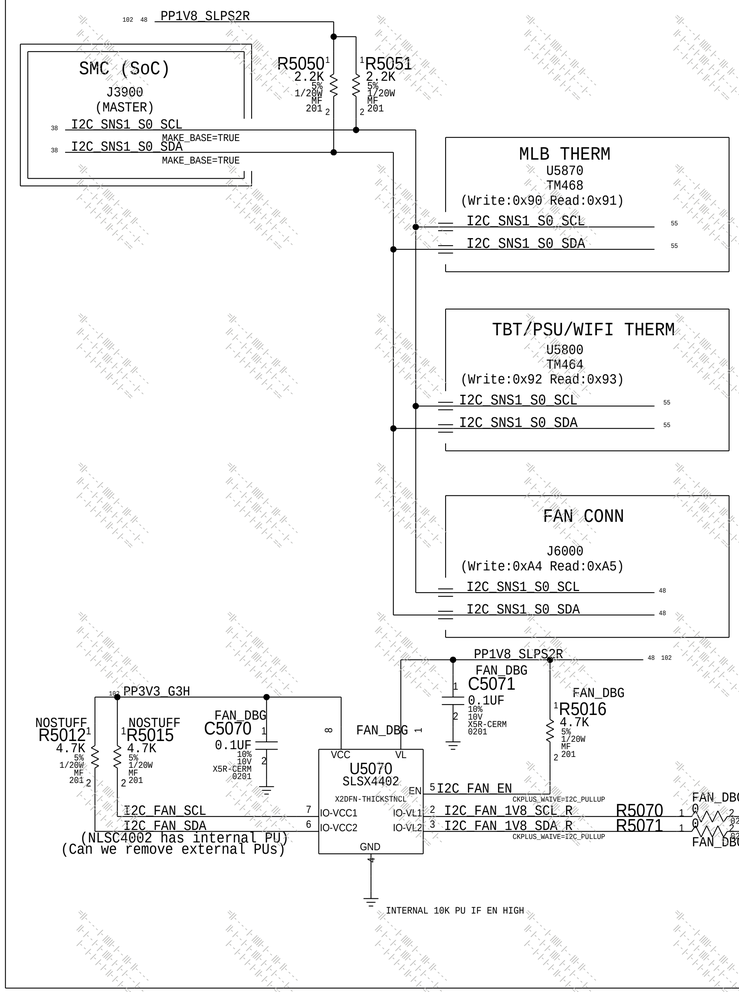
Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 49 OF 142
SHEET: 47 OF 115

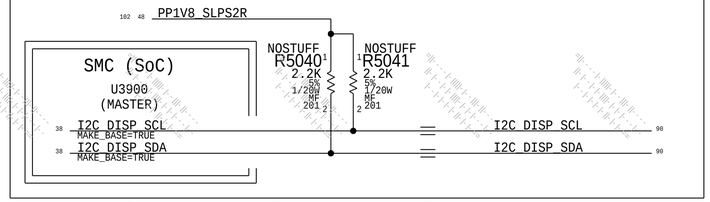
SMC I2C "0" G3H Connections



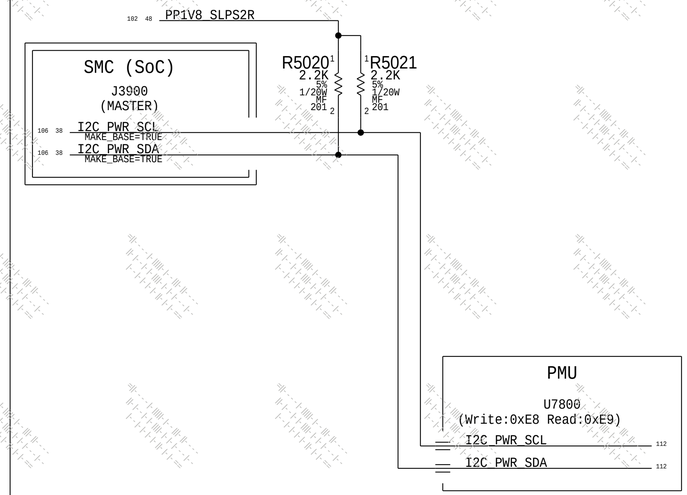
SMC I2C "2" G3H Connections



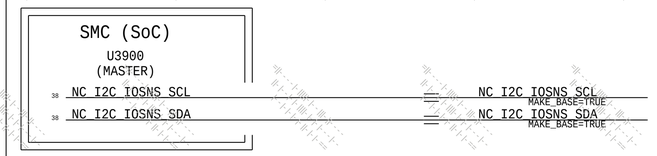
SMC I2C "3" S0 Connections



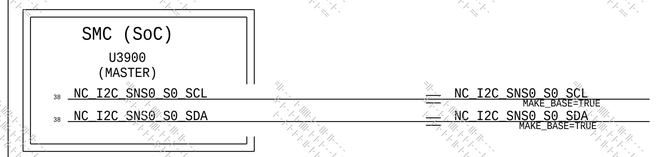
SMC I2C "4" G3H Connections



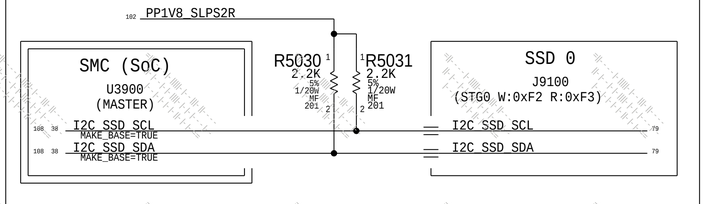
SMC I2C "5" G3S Connections



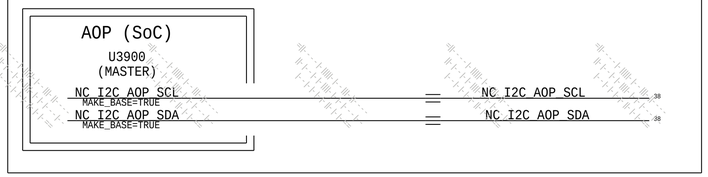
SMC I2C "1" Connections



SMC I2C "6" G3H Connections



AOP I2C G3H Connections



BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: I2C Connections 1

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

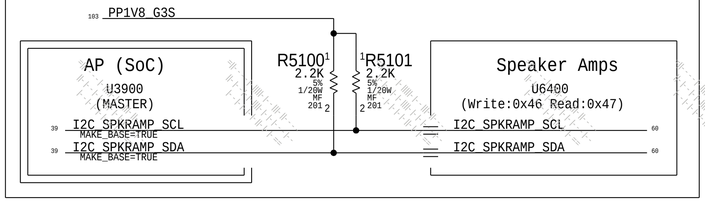
REVISION: 6.0.0

BRANCH: dvt-1

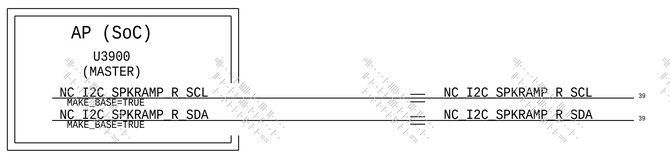
PAGE: 50 OF 142

SHEET: 48 OF 115

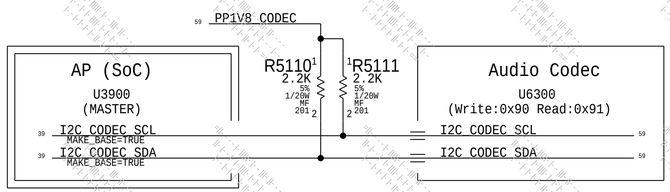
AP I2C "0" G3S Connections



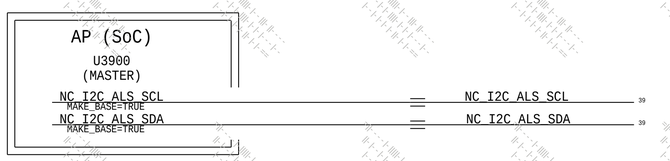
AP I2C "1" G3S Connections



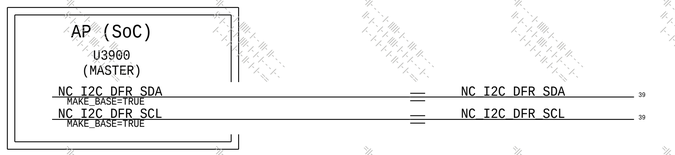
AP I2C "2" Codec Connections



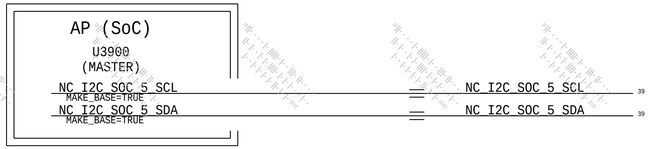
AP I2C "3" S0 Connections



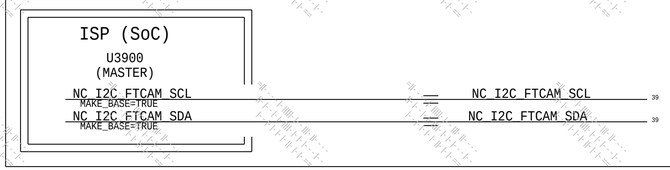
AP I2C "4" HDMI PCON G3S Connections



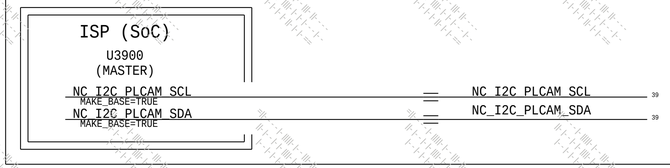
AP I2C "5" Awake Connections



ISP I2C "0" S0 Connections



ISP I2C "1" G3S Connections



BOM_COST_GROUP=SOC

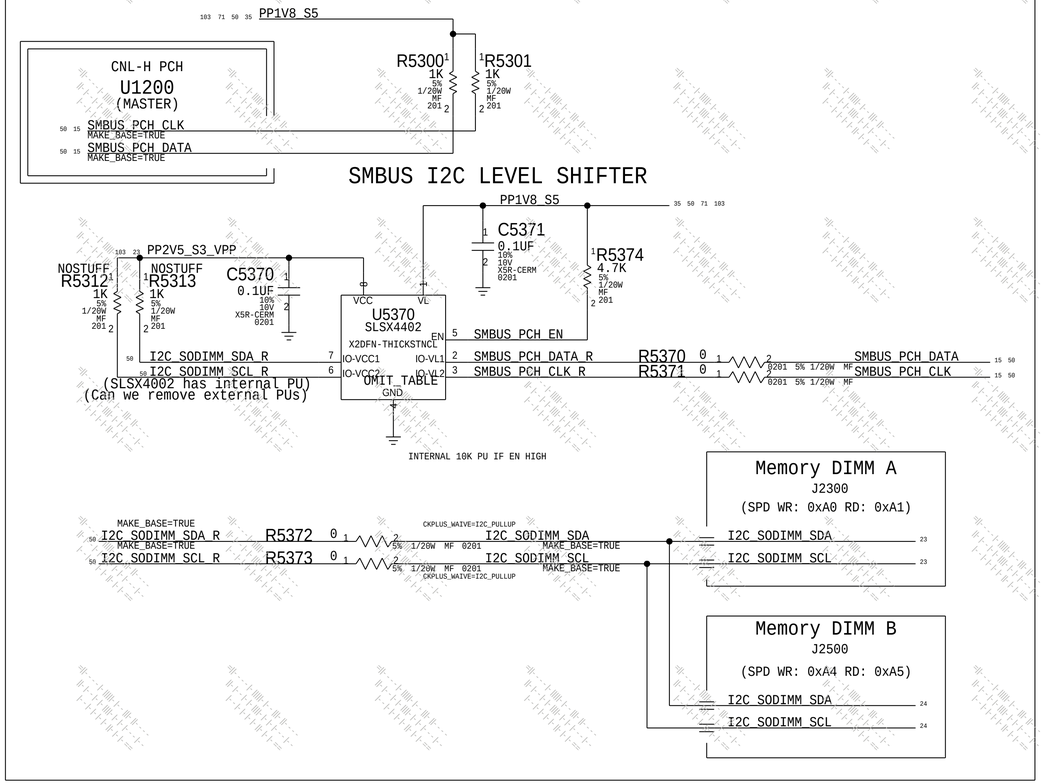
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018

PAGE TITLE
I2C Connections 2

Apple Inc.

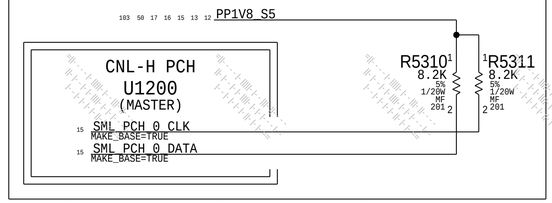
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 51 OF 142
SHEET 49 OF 115

CNL-H PCH "SMBus 0" Connections

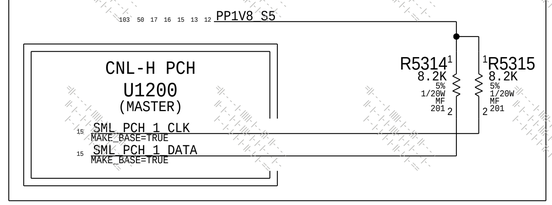


SMBUS I2C LEVEL SHIFTER

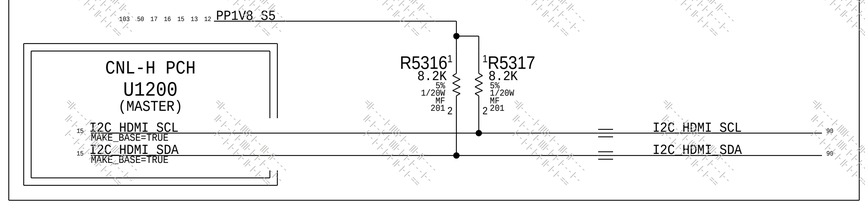
CNL-H PCH "SMLink 0"



CNL-H PCH "SMLink 1"



CNL-H PCH "I2C 0"



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
311S00179	1	IC,SLSX4402,2BIT D-LVL XLTR,1.8X1.2,DFN8	U5370	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: SMBus Connections

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 53 OF 142
SHEET: 50 OF 115

J680 SENSOR SETTINGS

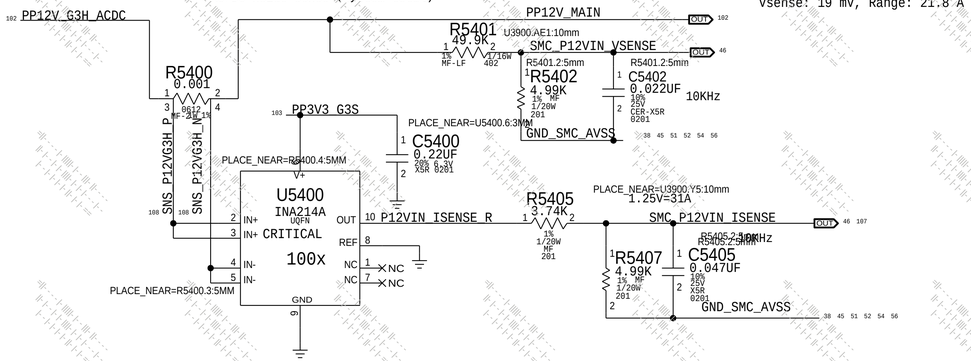
CHIP	Vref(V)	Vmax	SMC sample Freq.	ADR RC filter
H9M	1.25	1.8	10khz	0.1ms
CALPE	1.5	5	10hz	1ms
EADC	2.5	5	1-2hz(10hz)	100ms

PP12V_G3H

Current key:ID0M
Voltage key:VD0R

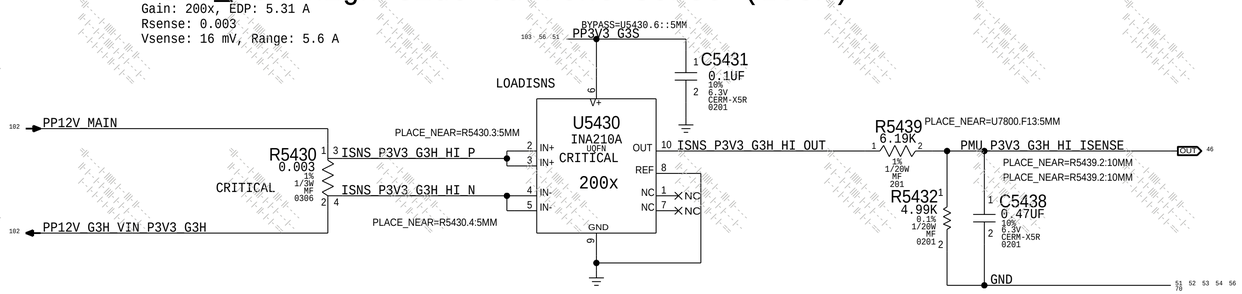
AC/DC hside sense (System total)

Gain: 100x, EDP: 18.75 A
Rsense: 0.001
Vsense: 19 mV, Range: 21.8 A



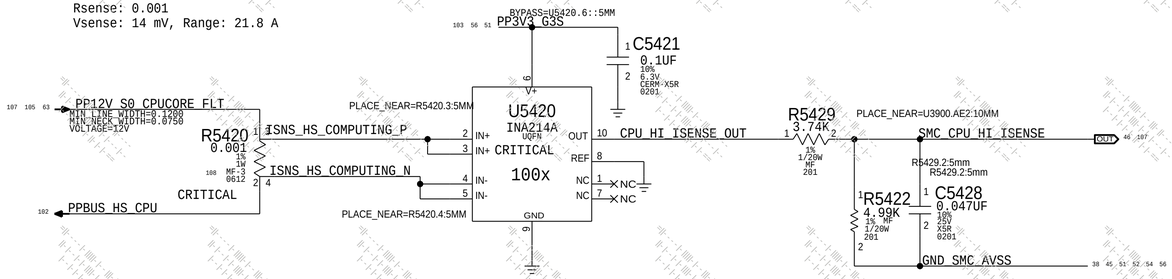
P3V3_G3H High Side Current Sense (IO3R)

Gain: 200x, EDP: 5.31 A
Rsense: 0.003
Vsense: 16 mV, Range: 5.6 A



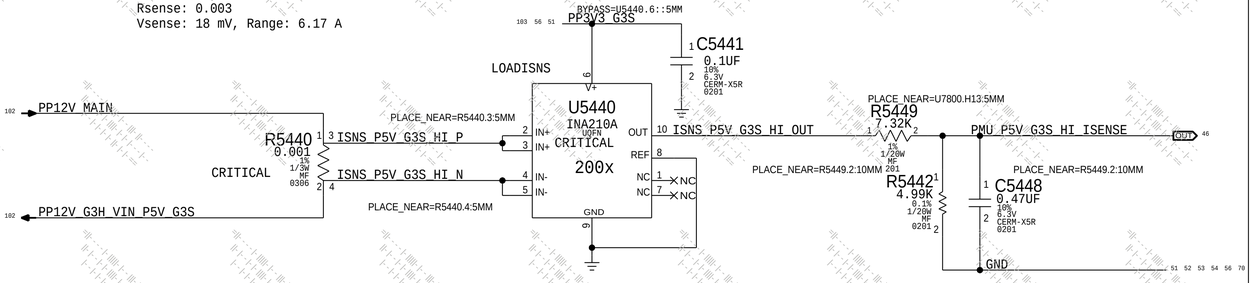
CPU High Side Currrent Sense (IC0R)

Gain: 100x, EDP: 14.41 A
Rsense: 0.001
Vsense: 14 mV, Range: 21.8 A



P5V_G3H High Side Current Sense (IO5R)

Gain: 200x, EDP: 5.89 A
Rsense: 0.003
Vsense: 18 mV, Range: 6.17 A



BOM_COST_GROUP=SENSORS

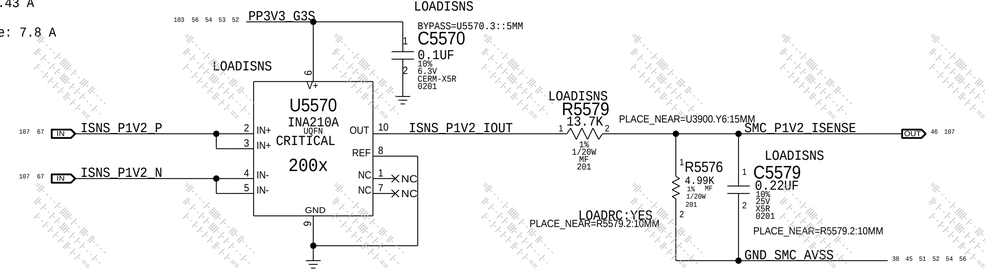
PAGE TITLE: Power Sensors High Side

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 54 OF 142
SHEET: 51 OF 115

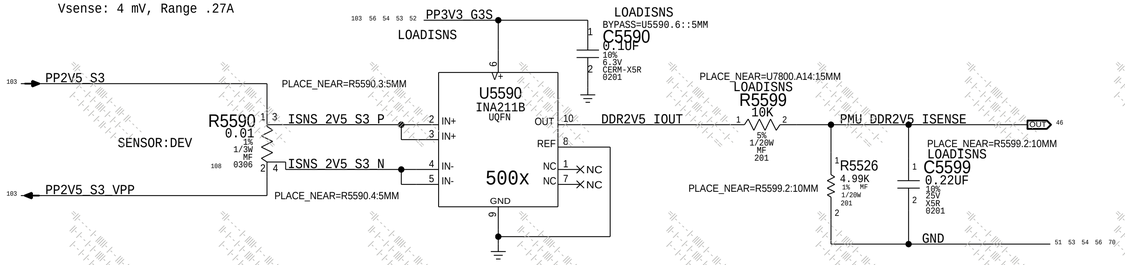
DDR4 1.2V Current Sense (IM0R)

Gain: 200x, EDP: 7.43 A
Rsense: 0.001
Vsense: 7 mV, Range: 7.8 A



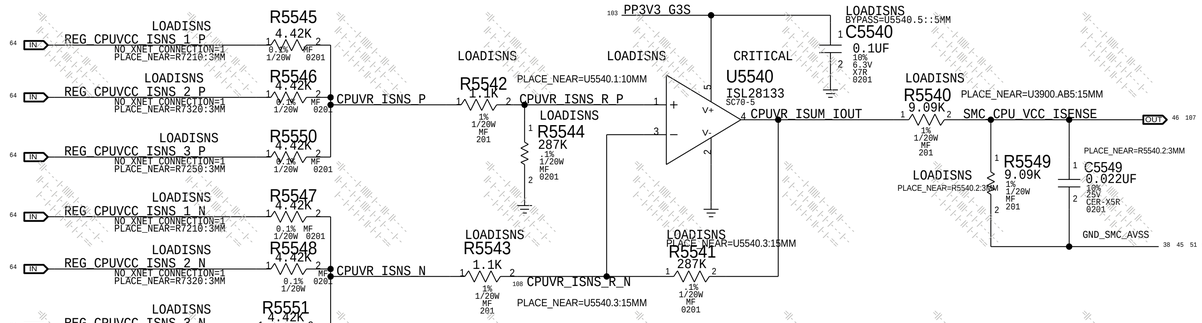
2.5V Current Sense (IM0C)

Gain: 500x, EDP: .24 A
Rsense: 0.015
Vsense: 4 mV, Range .27A



CPU Core Current Sense (ICAC)

Gain: 111.6x, EDP: 128 A
Rsense: 3x of 0.0005
Vsense:22.4 mV, Range: 134.4 A



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5576,R5519,R5549,C5539,R5529		LOADRC:NO

BOM_COST_GROUP=SENSORS

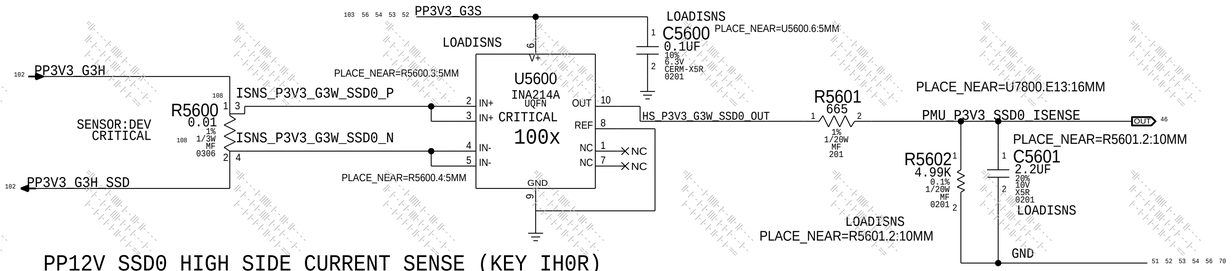
PAGE TITLE: Power Sensors Load Side

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 55 OF 142
SHEET: 52 OF 115

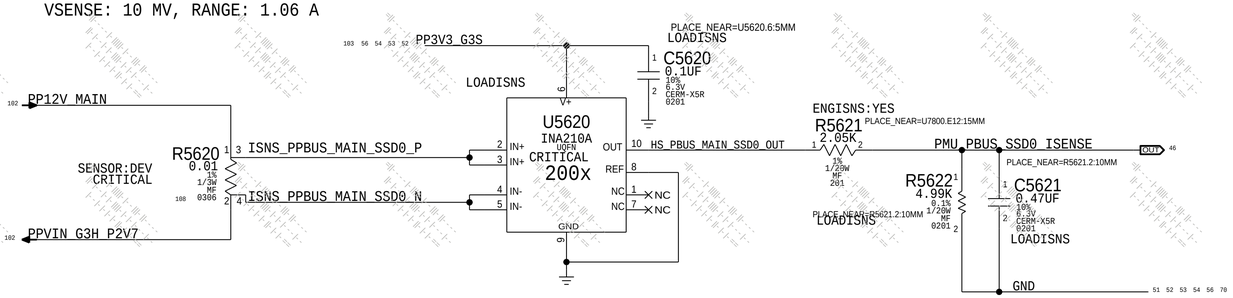
PP3V3_G3W_SSD0 HIGH SIDE CURRENT SENSE (IH0C)

GAIN: 100X, EDP: 1.6 A
RSENSE: 0.01
VSENSE: 16 MV, RANGE: 1.7 A



PP12V_SSD0 HIGH SIDE CURRENT SENSE (KEY IH0R)

GAIN: 200X, EDP: 1 A
RSENSE: 0.01
VSENSE: 10 MV, RANGE: 1.06 A



BOM_COST_GROUP=SENSORS

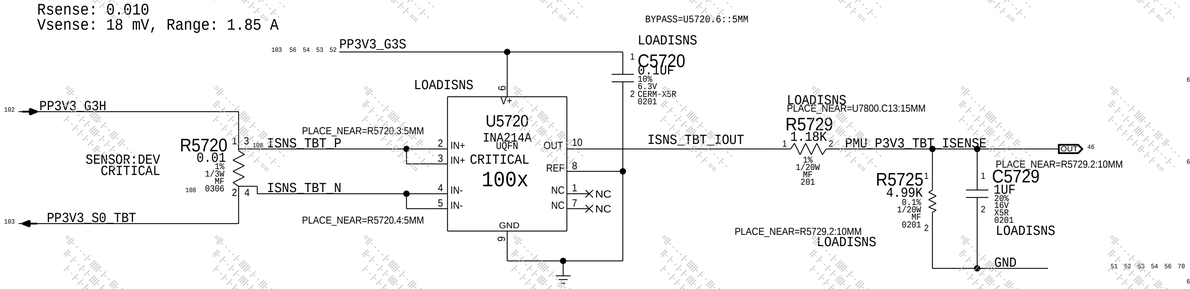
PAGE TITLE: Power Sensors Extended 1

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 56 OF 142
SHEET: 53 OF 115

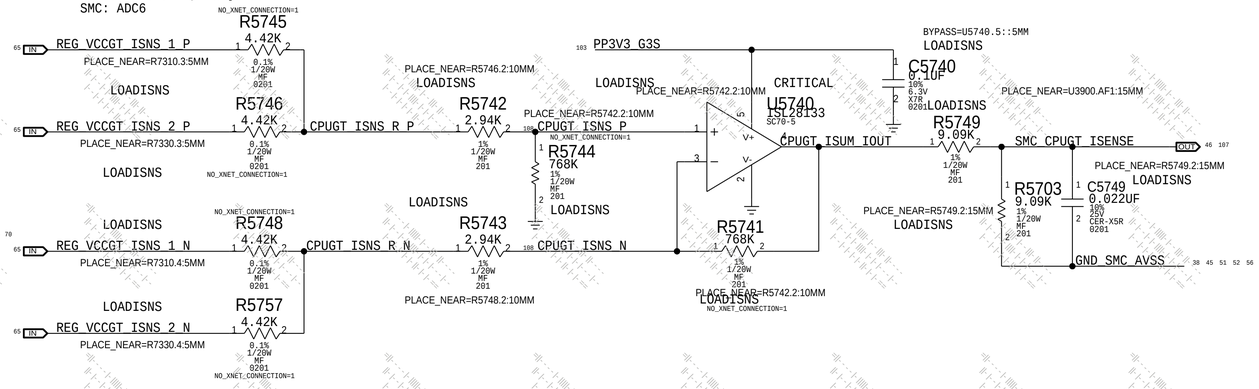
Thunderbolt TBT Current Sense (IU3C)

Gain: 100x. EDP: 1.76 A
Rsense: 0.010
Vsense: 18 mV, Range: 1.85 A



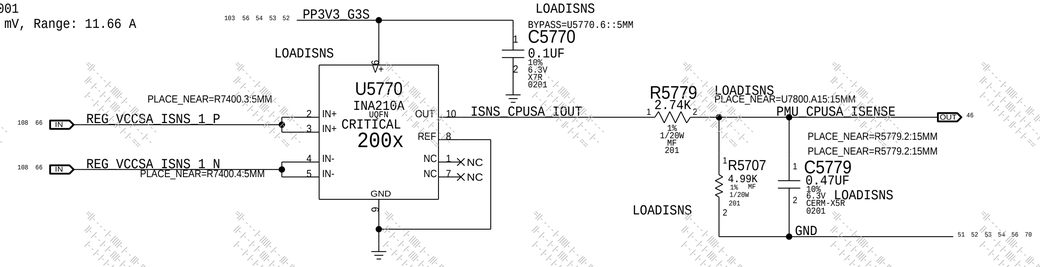
CPU GT Current Sense (ICTC)

Gain: 148.8x, EDP: 32 A
Rsense: 2x of 0.001
Vsense: 16.8 mV, Range:33.6 A
SMC: ADC6



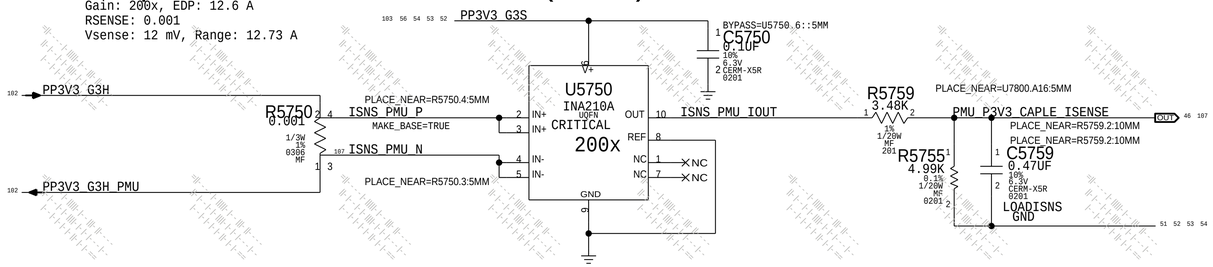
CPU SA Current Sense (ICSC)

Gain: 200x, EDP: 11.1 A
Rsense: 0.001
Vsense: 11 mV, Range: 11.66 A



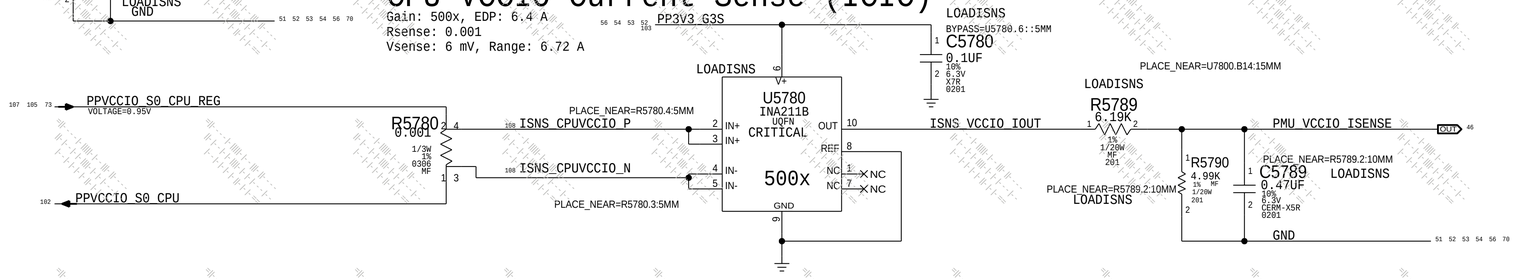
Calpe 3V3 Current Sense (ISLC)

Gain: 200x, EDP: 12.6 A
RSENSE: 0.001
Vsense: 12 mV, Range: 12.73 A



CPU VCCIO Current Sense (ICIC)

Gain: 500x, EDP: 6.4 A
Rsense: 0.001
Vsense: 6 mV, Range: 6.72 A



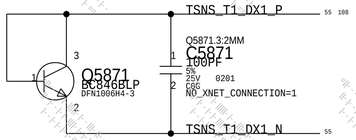
BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors Extended 2

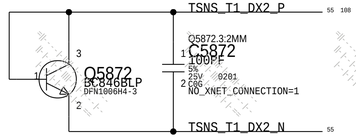
Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 57 OF 142
SHEET: 54 OF 115

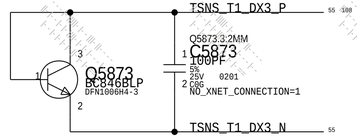
THERMAL DIODE: CPU PROX (KEY TC0P)



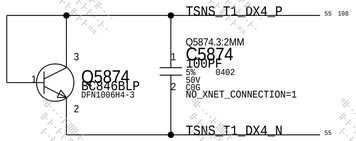
THERMAL DIODE: MEM PROX (KEY TM0P)



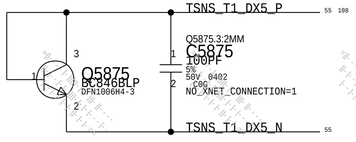
THERMAL DIODE: NAND PROX 1 (KEY TH0a)



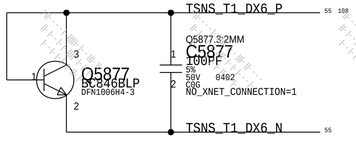
THERMAL DIODE: NAND PROX 2 (KEY TH0b)



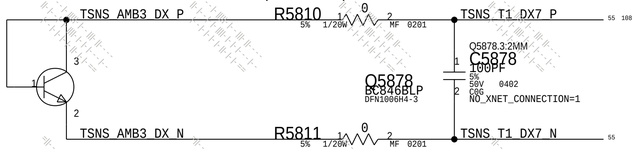
THERMAL DIODE: AMBIENT SEN 1 (KEY TaLC)



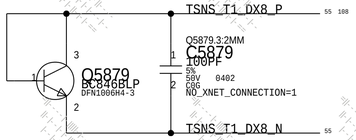
THERMAL DIODE: AMBIENT SEN 2 (KEY TaRC)



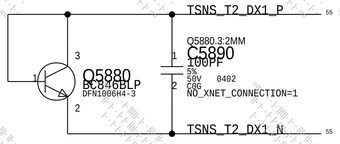
THERMAL DIODE: AMBIENT SEN 3 (KEY TCaP)



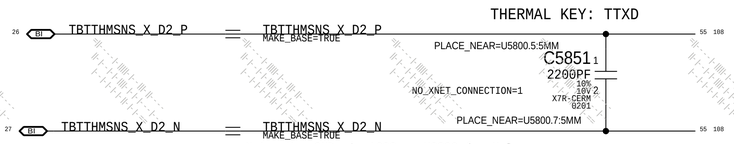
THERMAL DIODE: WIFI/BT PROX (KEY TW0P)



THERMAL DIODE: 10G/1G ETH PHY PROX (KEY TIED)

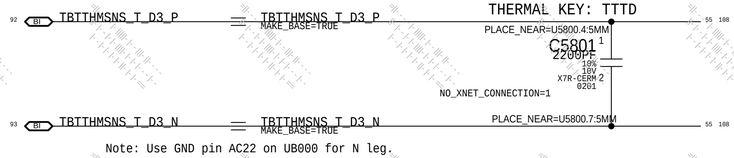


THERMAL KEY: TTXD



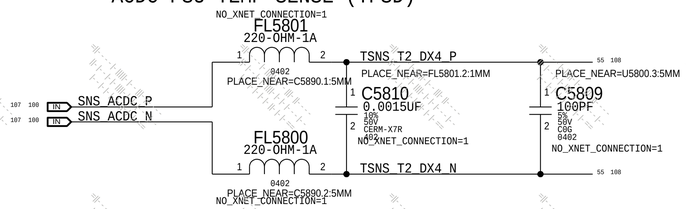
Note: Use GND pin AC22 on U2800 for N leg.

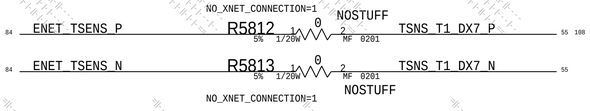
THERMAL KEY: TTTD



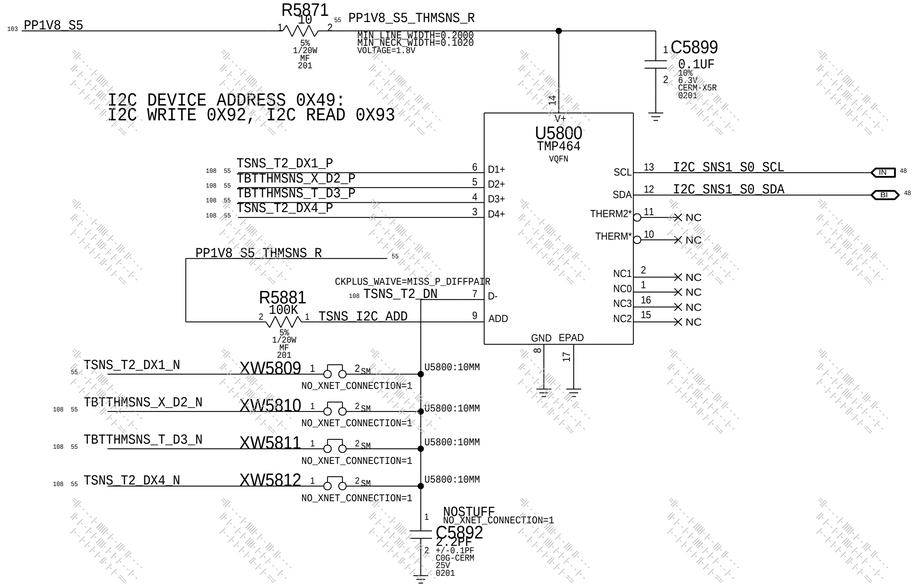
Note: Use GND pin AC22 on UB000 for N leg.

ACDC PSU TEMP SENSE (TPSD)

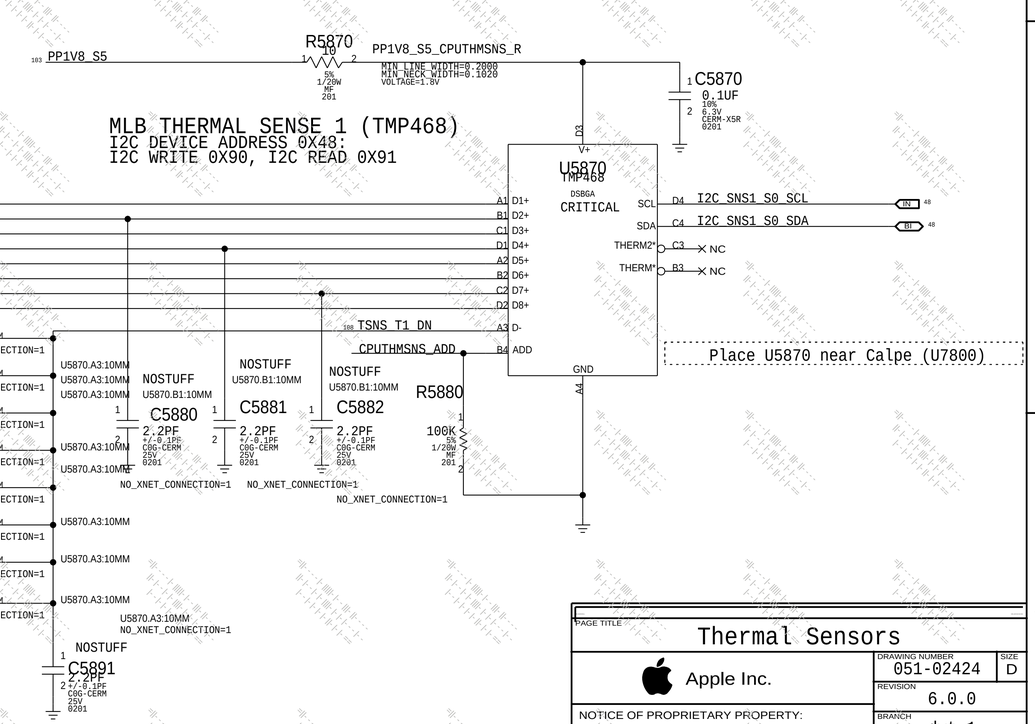




I2C DEVICE ADDRESS 0X49: I2C WRITE 0X92, I2C READ 0X93



MLB THERMAL SENSE 1 (TMP468)
I2C DEVICE ADDRESS 0X48: I2C WRITE 0X90, I2C READ 0X91



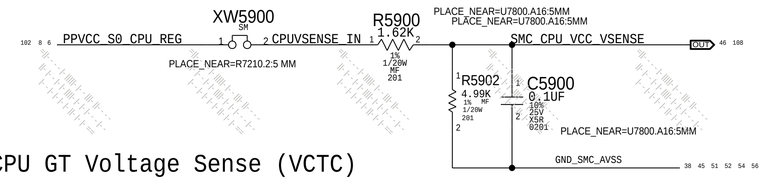
BOM_COST_GROUP=SENSORS

PAGE TITLE: Thermal Sensors

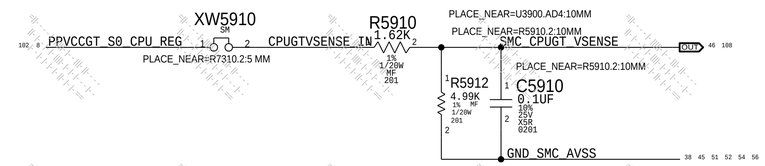
Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 58 OF 142
SHEET: 55 OF 115

CPU Core Voltage Sense (VCAC)

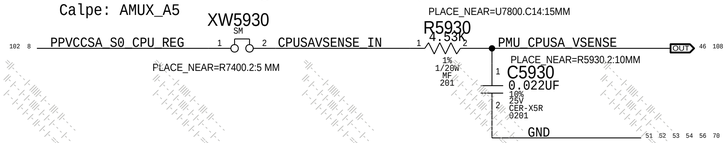


CPU GT Voltage Sense (VCTC)



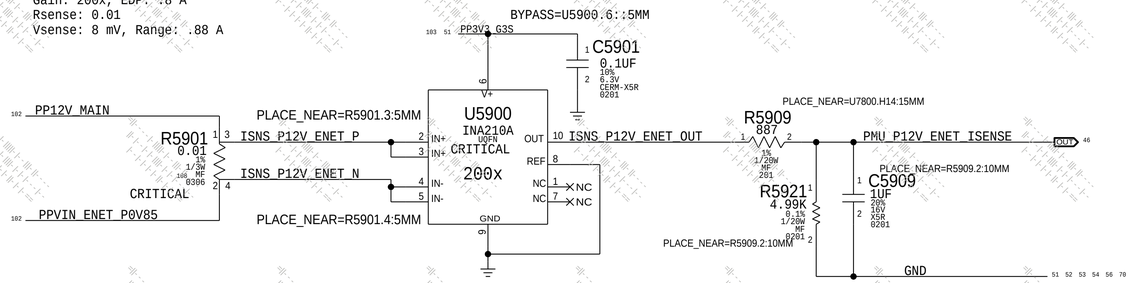
CPU SA Voltage Sense (VCSC)

Calpe: AMUX_A5



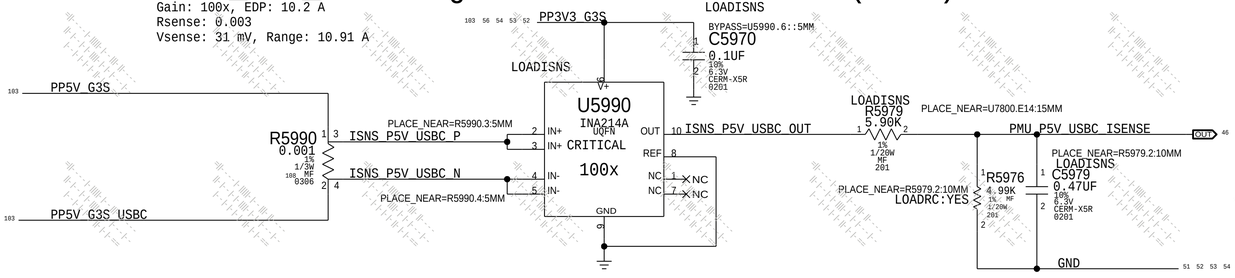
ENET 0V85 VR P12V Input Current Sense (IE2R)

Gain: 200x, EDP: .8 A
Rsense: 0.01
Vsense: 8 mV, Range: .88 A



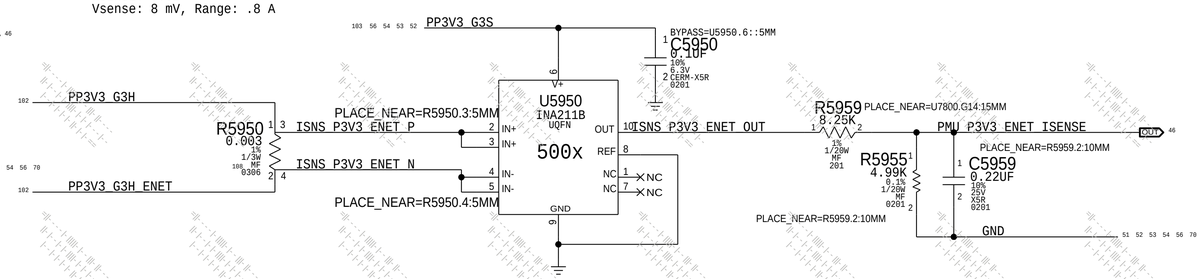
PP5V_G3S_USBC High side Current Sense (IU5C)

Gain: 100x, EDP: 10.2 A
Rsense: 0.003
Vsense: 31 mV, Range: 10.91 A



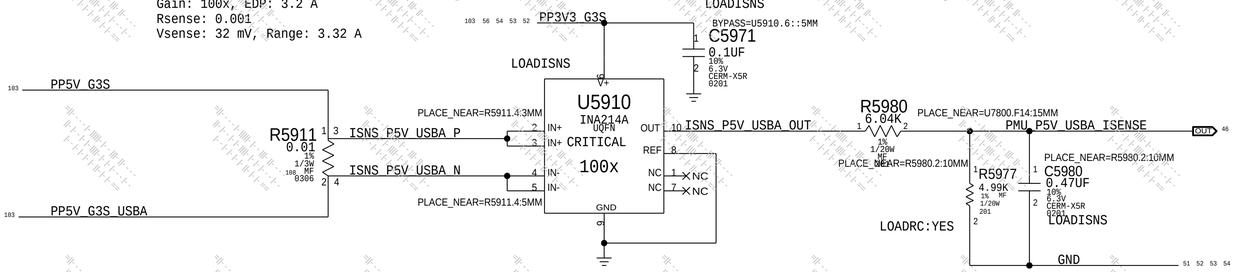
ENET 3V3 Current Sense (IE3R)

Gain: 500x, EDP: .79 A
RSENSE: 0.01
Vsense: 8 mV, Range: .8 A



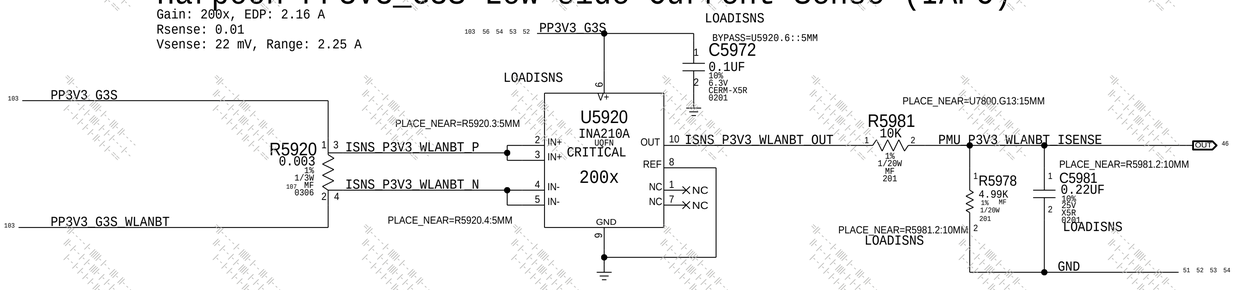
PP5V_G3S_USBA High side Current Sense (IUAC)

Gain: 100x, EDP: 3.2 A
Rsense: 0.001
Vsense: 32 mV, Range: 3.32 A



Harpoon PP3V3_G3S Low side Current Sense (IAPC)

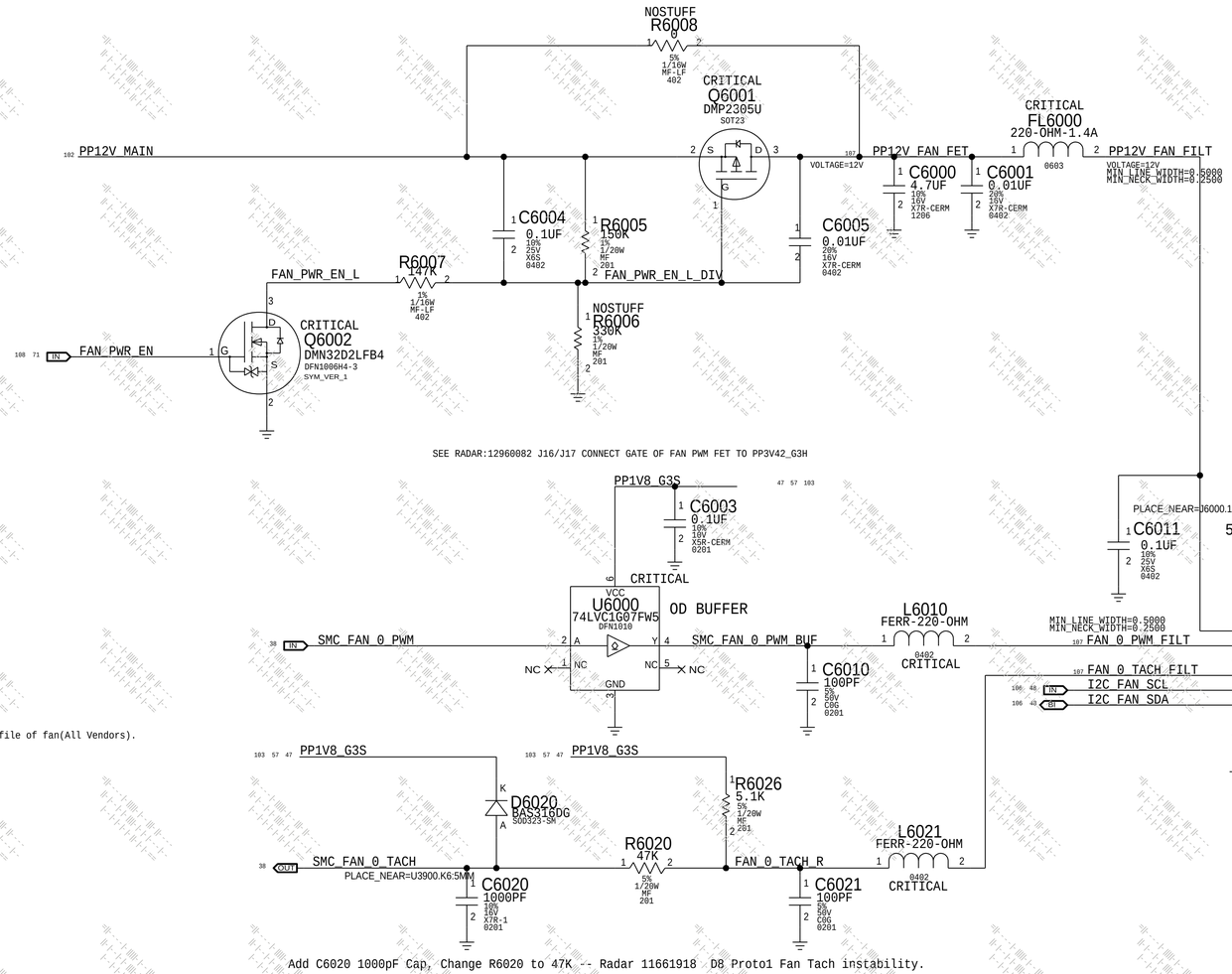
Gain: 200x, EDP: 2.16 A
Rsense: 0.01
Vsense: 22 mV, Range: 2.25 A



BOM_COST_GROUP=SENSORS

SYNC_MASTER=Mary	SYNC_DATE=04/26/2018
PAGE TITLE	More V/I Sensing
Apple Inc.	DRAWING NUMBER 051-02424 · SIZE D
	REVISION 6.0.0
	BRANCH dvt-1
	PAGE 59 OF 142
	SHEET 56 OF 115

SMC Fan 0 (System)



SEE RADAR:12960082 J16/J17 CONNECT GATE OF FAN PWM FET TO PP3V42_G3H

Note:

The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).

Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Proto1 Fan Tach instability.

BOM_COST_GROUP=FAN

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: System Fan Connector

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 60 OF 142

SHEET: 57 OF 115

BOM_COST_GROUP=DEBUG

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

SPI Debug Connector

Apple Inc.

DRAWING NUMBER 051-02424

SIZE D

REVISION 6.0.0

BRANCH dvt-1

PAGE 61 OF 142

SHEET 58 OF 115

AUDIO JACK CODEC I2C ADDRESS

AD1	AD0	ADDRESS
GND	GND	0x48 <--
GND	1.8V	0x49
1.8V	GND	0x4A
1.8V	1.8V	0x4B

PP1V8_G3S
L6362
FERR-22-OHM-1A-0.055OHM
0201
NOSTUFF
L6361
FERR-470-OHM
0201
AUD_PWR_EN
AUD_3V3_L83_LDO_EN
NOSTUFF
L6360
FERR-22-OHM-1A-0.055OHM
0201
PP3V3_G3S
PP3V3_G3S_AUDIO_LDO0
U6360
NCP160AMX180
XDFN-COMBO
NOSTUFF
GND_EPAD
IN
EN
OUT
CODEC_LDO_1V8
R6314
0
5%
1/20W
MF
0201
NOSTUFF
PP1V8_CODEC
VOLTAGE=1.8V
CRITICAL
BYPASS=U6360.1:2:5 MM
C6361
1.0UF
20%
10V
X5R-CERM
0201-1
BYPASS=U6360.4:2: MM
CRITICAL
C6360
1.0UF
20%
10V
X5R-CERM
0201-1
R6360
33K
5%
1/20W
MF
201
NOSTUFF
NOSTUFF
C6362
0.1UF
10%
25V
CER-X5R
0201
XW6300
SHORT-8L-0.25MM-SM
GND_AUDIO_CODEC

PP1V8_CODEC
MIN_LINE_WIDTH=0.0860
MIN_NECK_WIDTH=0.0720
CRITICAL
C6324
2.2UF
10%
16V
X5R-CERM
0402
BYPASS=U6300.B1:C2:5 MM
GND_AUDIO_CODEC
L6300
FERR-22-OHM-1A-0.055OHM
0201
PP1V8_G3S_AUDIO_L83_VCP
MIN_LINE_WIDTH=0.0860
MIN_NECK_WIDTH=0.0720
L6301
FERR-22-OHM-1A-0.055OHM
0201
PP1V8_G3S
PP1V8_G3S_AUDIO_L83_VL
MIN_LINE_WIDTH=0.0860
MIN_NECK_WIDTH=0.0720
BYPASS=U6300.A3:B3:5 MM
CRITICAL
C6303
0.1UF
10%
50V
X7R
603-1
L6302
FERR-22-OHM-1A-0.055OHM
0201
PP3V3_G3S
PP3V3_G3S_AUDIO_L83_VP
MIN_LINE_WIDTH=0.0860
MIN_NECK_WIDTH=0.0720
BYPASS=U6300.D7:C7:5 MM
CRITICAL
C6304
10UF
20%
6.3V
X5R-CERM
0402-7

C6302
2.2UF
10%
10V
X5R-CERM
0402
BYPASS=U6300.D6:F6:5 MM
CRITICAL
XW6301
SHORT-8L-0.25MM-SM
GND_VCP
OMIT_TABLE
C6305
4.7UF
10%
10V
X5R
0402
BYPASS=U6300.E6:F6:5 MM
L83_VCP_FILTP
MIN_LINE_WIDTH=0.0860
MIN_NECK_WIDTH=0.0720
OMIT_TABLE
C6306
4.7UF
10%
10V
X5R
0402
BYPASS=U6300.G6:F6:5 MM
L83_VCP_FILTN
MIN_LINE_WIDTH=0.0860
MIN_NECK_WIDTH=0.0720

AUD_HP_PORT_L
R6300
1K
5%
1/20W
MF
201
GND_AUDIO_CODEC
R6301
1K
5%
1/20W
MF
201
AUD_HP_PORT_R
AUD_HP_SENSE_L
AUD_HP_SENSE_R
AUD_HP_PORT_CH_GND

U6300
CS42L83
QFN
CRITICAL
APN:338S00142

6	VP	+VCP_FILT	10
39	VL	-VCP_FILT	13
47	VD_FILT	GNDCP	12
33	VA	VL_SEL	48
7	VCP	DIGLDO_PDN*	4
		INT*	2
		WAKE*	3
		RESET*	1
		SPDIF_TX	45
		SWIRE_SEL	40
		ASP_LRCK/FSYNC	43
		SWIRE_SD/ASP_SDIN	44
		ASP_SDOUT	41
		SWIRE_CLK/ASP_SCLK	42
		AD0	35
		AD1	34
		SDA	36
		SCL	37
		FLYP	8
		FLYC	9
		FLYN	11
		FILT_P	32
14	HPSENSA		
15	HPOUTA		
17	HPSENSB		
16	HPOUTB		
28	HS4		
27	HS_CLAMP2		
29	HSIN+		
24	HS3		
26	HS_CLAMP1		
30	HSIN-		
20	HS4_REF		
19	HS3_REF		
21	RING_SENSE		
18	TIP_SENSE		
22	HSBIAS_FILT		
23	HSBIAS_FILT_REF		
38	GNDL		
5	GNDD		
46	GNDHS		
25	GNDA		
31	EPAD		
49			

PP3V3_G3S
PP1V8_CODEC
NC
I2S_CODEC_LRCLK_RR
R6304
0
5%
1/20W
MF
0201
PLACE_NEAR=U6300:5 MM
I2S_CODEC_LRCLK
I2S_CODEC_R2D_RR
R6305
0
5%
1/20W
MF
0201
PLACE_NEAR=U6300:5 MM
I2S_CODEC_R2D
I2S_CODEC_D2R_R
R6306
33
5%
1/20W
MF
0201
PLACE_NEAR=U6300:5MM
I2S_CODEC_D2R
I2S_CODEC_BCLK_RR
R6307
0
5%
1/20W
MF
0201
PLACE_NEAR=U6300:5 MM
I2S_CODEC_BCLK
I2C_CODEC_SDA
I2C_CODEC_SCL
L83_FLYP
L83_FLYC
L83_FLYN
L83_FILTP
MIN_LINE_WIDTH=0.0860
MIN_NECK_WIDTH=0.0720
CRITICAL
C6310
10UF
20%
16V
X5R
0603
BYPASS=U6300.C1:C2:5 MM
CRITICAL
C6307
2.2UF
10%
10V
X5R-CERM
0402
BYPASS=U6300.E7:F7:5 MM
C6308
2.2UF
10%
10V
X5R-CERM
0402
CRITICAL
BYPASS=U6300.G7:F7:5 MM
PP1V8_G3S
R6312
47K
5%
1/20W
MF
201
R6302
47K
5%
1/20W
MF
201
R6313
47K
5%
1/20W
MF
201
CODEC_INT_L
CODEC_WAKE_L
CODEC_RESET_L

AUD_HS_MIC_P
AUD_HS_MIC_N
AUD_HP_PORT_US_GND
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1000
AUD_RING_SENSE
AUD_TIP_SENSE
L83_HSBIAS_FILT
MIN_LINE_WIDTH=0.0860
MIN_NECK_WIDTH=0.0720
CRITICAL
C6309
4.7UF
20%
6.3V
X5R
402
L83_HSBIAS_FILT_REF
MIN_LINE_WIDTH=0.0860
MIN_NECK_WIDTH=0.0720
BYPASS=U6300.F3:E3:5 MM
GND_AUDIO_CODEC
MIN_LINE_WIDTH=0.0860
MIN_NECK_WIDTH=0.0720

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0719	2	CAP,CER,4.7UF,20%,10V,X5R,0402,MURATA	C6305,C6306	CRITICAL	

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO JACK CODEC

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 63 OF 142
SHEET: 59 OF 115

1x MONO SPEAKER AMPLIFIER (TAS5770)

APN: 353S01629

PP1V8_G3S

PLACE_NEAR=U6400.D2:5 MM

PLACE_NEAR=U6400.D2:3 MM

C6402 1UF 10% 10V X5R 402-1 CRITICAL

C6403 0.1UF 10% 10V X5R 0201 CRITICAL

PLACE_NEAR=U6400.C1:5 MM

PLACE_NEAR=U6400.C1:3 MM

VOLTAGE=1.8V

SHORT-8L-0.25MM-SM XW6410

PP1V8_G3S_SPKRAMP_AVDD

C6400 1UF 10% 10V X5R 402-1 CRITICAL

C6401 0.1UF 10% 10V X5R 0201 CRITICAL

PLACE_NEAR=U6400.C4:3 MM

PLACE_NEAR=U6400.C4:10 MM

C6404 0.1UF 10% 10V X5R 0201 CRITICAL

C6405 10UF 20% 25V X5R-CERM 0603 CRITICAL

C6406 10UF 20% 25V X5R-CERM 0603 CRITICAL

C6415 10UF 20% 25V X5R-CERM 0603 CRITICAL

C6416 10UF 20% 25V X5R-CERM 0603 CRITICAL

PP12V_MAIN

R6400 47K 5% 1/20W MF 201

SPKRAMP_INT

SPKRAMP_RESET

I2C_SPKRAMP_SDA

I2C_SPKRAMP_SCL

SPKRAMP_MODE

I2S_SPKRAMP_R2D

I2S_SPKRAMP_D2R

I2S_SPKRAMP_LRCLK

I2S_SPKRAMP_BCLK

R6403 0 5% 1/20W MF 0201

R6404 33 5% 1/20W MF 201

R6402 0 5% 1/20W MF 0201

R6401 0 5% 1/20W MF 0201

PLACE_NEAR=U6400: 5MM

I2S_SPKRAMP_R2D_RR

I2S_SPKRAMP_D2R_R

I2S_SPKRAMP_LRCLK_RR

I2S_SPKRAMP_BCLK_RR

U6400 PTAS5770LB2 CSP

AVDD C1

IOVDD D2

VBAT C4 C5

GND C2

PGND A4 B4

SDZ* C3

SDA F3

SCL F4

IRQZ D4

MODE D3

SDIN F2

SDOUT E1

FSYNC E2

SBCLK F1

PDMD0 E4

PDMCK0 E3

PDMD1 E5

PDMCK1 F5

BST_P B2

OUT_P A3

OUT_P B3

VSNS_P A1

BST_N A2

OUT_N A5

OUT_N B5

VSNS_N B1

AREG D5

DREG D1

C6411 0.1UF 10% 25V X5R 0201 CRITICAL

BYPASS=U6400.B2:B3:5 MM

NO_XNET_CONNECTION=1

L6400 1800HM-3.4A 0806

PLACE_NEAR=U6400.A3:10 MM

DIDT=TRUE

XW6400 SHORT-8L-0.25MM-SM

PLACE_NEAR=J6400.1:3MM

C6412 0.1UF 10% 25V X5R 0201 CRITICAL

BYPASS=U6400.A2:A5:5 MM

NO_XNET_CONNECTION=1

L6401 1800HM-3.4A 0806

PLACE_NEAR=U6400.A5:10 MM

DIDT=TRUE

XW6401 SHORT-8L-0.25MM-SM

PLACE_NEAR=J6400.2:3MM

SPKRAMP_AREG

SPKRAMP_DREG

C6407 0.1UF 10% 25V X5R 0201

C6408 1UF 10% 16V X5R 402-1

C6409 0.1UF 10% 25V X5R 0201

C6410 1UF 10% 16V X5R 402-1 CRITICAL

PLACE_NEAR=U6400.D1:3 MM CRITICAL

PLACE_NEAR=U6400.D5:3 MM CRITICAL

PLACE_NEAR=U6400.D1:5 MM CRITICAL

PLACE_NEAR=U6400.D5:5 MM CRITICAL

MIN_LINE_WIDTH=1.5000

SPKRCONN_OUTP

SPKRCONN_OUTN

NO_STUFF

C6413 220PF 10% 25V X7R-CERM 201 CRITICAL

C6414 220PF 10% 25V X7R-CERM 201 CRITICAL

SPEAKER CABLE CONNECTOR

APN:518S0519

J6400 78171-0002 M-RT-SM

BULK CAPACITANCE

C6480 33UF 20% 16V TANT CASED12-SM CRITICAL

C6481 33UF 20% 16V TANT CASED12-SM CRITICAL

C6482 68UF 20% 16V AL CASE-D2-SM CRITICAL

C6483 68UF 20% 16V AL CASE-D2-SM CRITICAL

PP12V_MAIN

R6405 100K 5% 1/20W MF 201

R6480 0 5% 1/20W MF 0201

I2C ADDRESS: 0x31

BOM_COST_GROUP=AUDIO

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: AUDIO SKPR AMP

Apple Inc.

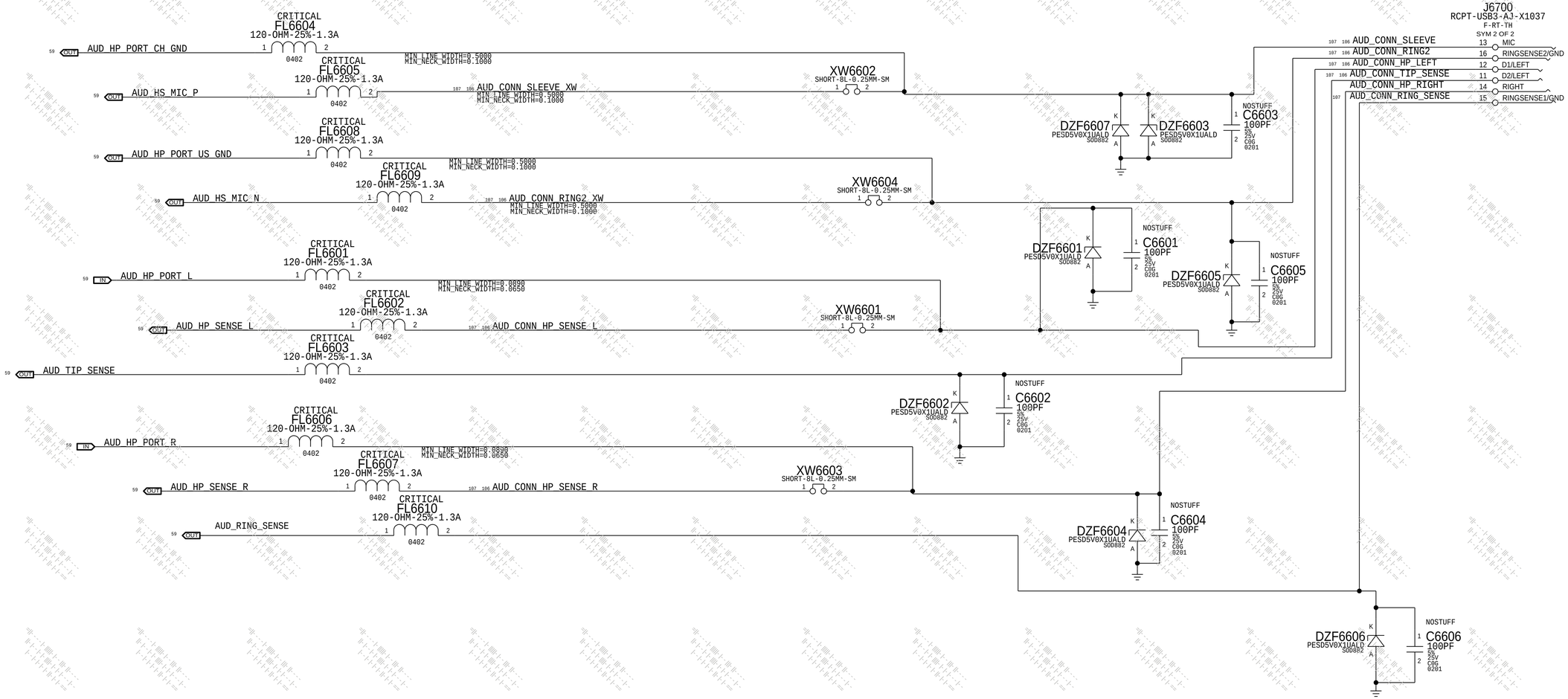
DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 64 OF 142

SHEET: 60 OF 115



BOM_COST_GROUP=AUDIO

PAGE TITLE

AUDIO JACK CONNECTOR

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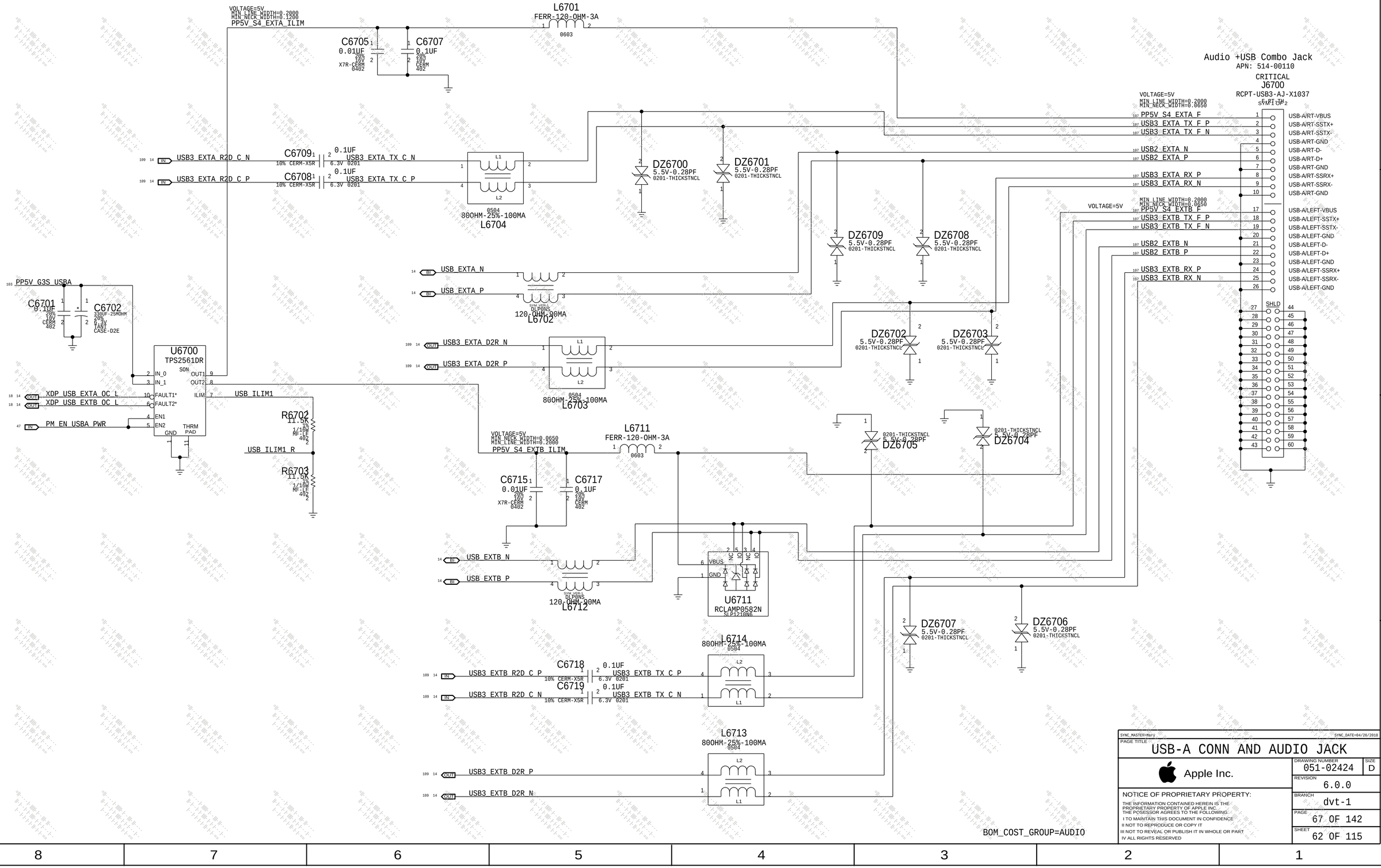
DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

BRANCH dvt-1

PAGE 66 OF 142

SHEET 61 OF 115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MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
PP5V_S4_EXTA_ILIM
L6701
FERR-120-OHM-3A
0603
C6705
0.01UF
20%
16V
X7R-CERM
0402
C6707
0.1UF
20%
10V
CERM
402
Audio +USB Combo Jack
APN: 514-00110
CRITICAL
J6700
RCPT-USB3-AJ-X1037
SHIELD
VOLTAGE=5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0650
PP5V_S4_EXTA_F
USB3_EXTA_TX_F_P
USB3_EXTA_TX_F_N
USB2_EXTA_N
USB2_EXTA_P
USB3_EXTA_RX_P
USB3_EXTA_RX_N
USB-A/RT-VBUS
USB-A/RT-SSTX+
USB-A/RT-SSTX-
USB-A/RT-GND
USB-A/RT-D-
USB-A/RT-D+
USB-A/RT-GND
USB-A/RT-SSRX+
USB-A/RT-SSRX-
USB-A/RT-GND
PP5V_S4_EXTB_F
USB3_EXTB_TX_F_P
USB3_EXTB_TX_F_N
USB2_EXTB_N
USB2_EXTB_P
USB3_EXTB_RX_P
USB3_EXTB_RX_N
USB-A/LEFT-VBUS
USB-A/LEFT-SSTX+
USB-A/LEFT-SSTX-
USB-A/LEFT-GND
USB-A/LEFT-D-
USB-A/LEFT-D+
USB-A/LEFT-GND
USB-A/LEFT-SSRX+
USB-A/LEFT-SSRX-
USB-A/LEFT-GND
SHLD
USB3_EXTA_R2D_C_N
USB3_EXTA_R2D_C_P
C6709
C6708
0.1UF
10% CERM-X5R
6.3V 0201
USB3_EXTA_TX_C_N
USB3_EXTA_TX_C_P
L6704
0504
80OHM-25%-100MA
DZ6700
DZ6701
5.5V-0.28PF
0201-THICKSTNCL
DZ6709
DZ6708
DZ6702
DZ6703
USB_EXTA_N
USB_EXTA_P
L6702
SYM_VER=1
DLP90NS
120-OHM-90MA
USB3_EXTA_D2R_N
USB3_EXTA_D2R_P
L6703
PP5V_G3S_USBA
C6701
0.1UF
20%
16V
CERM
402
C6702
330UF-25MOHM
20%
6.3V
TANT
CASE-D2E
U6700
TPS2561DR
SON
IN_0
IN_1
FAULT1*
FAULT2*
EN1
EN2
ILIM
THRM PAD
GND
OUT1
OUT2
XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L
PM_EN_USBA_PWR
USB_ILIM1
R6702
11.5K
1/10W
MF-LF
402
USB_ILIM1_R
R6703
11.5K
1/10W
MF-LF
402
VOLTAGE=5V
MIN_LINE_WIDTH=0.0650
MIN_NECK_WIDTH=0.2000
PP5V_S4_EXTB_ILIM
L6711
FERR-120-OHM-3A
0603
C6715
0.01UF
20%
16V
X7R-CERM
0402
C6717
0.1UF
20%
10V
CERM
402
DZ6705
DZ6704
0201-THICKSTNCL
5.5V-0.28PF
USB_EXTB_N
USB_EXTB_P
L6712
SYM_VER=1
DLP90NS
120-OHM-90MA
U6711
RCLAMP0582N
SLP1210N6
VBUS
GND
NC
IO
DZ6707
DZ6706
C6718
C6719
USB3_EXTB_R2D_C_P
USB3_EXTB_R2D_C_N
USB3_EXTB_TX_C_P
USB3_EXTB_TX_C_N
L6714
L6713
USB3_EXTB_D2R_P
USB3_EXTB_D2R_N
BOM_COST_GROUP=AUDIO
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
USB-A CONN AND AUDIO JACK
Apple Inc.
DRAWING NUMBER
051-02424
SIZE
D
REVISION
6.0.0
BRANCH
dvt-1
PAGE
67 OF 142
SHEET
62 OF 115
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Designed By 571391_CFL_H_PDG_Rev1p0

ISUM_C

PP1V8_S5 → R7140 10K 5% 1/20W MF 201 → PM_PGOOD_REG_CPUVCC → PM_PGOOD_REG_CPUVCC OUT 47
MAKE_BASE=TRUE

ISUMN_C (IN 66) → C7124 0.1UF 0201 10% 6.3V X7R
ISUMN_C → NOSTUFF R7131 11K 1% 1/20W MF 201 → ISUMP_C (IN 66 63)
ISUMN_C → NOSTUFF C7126 0.015UF 10% 25V X7R 402 → ISUMN_C_L_2
ISUMN_C_L_2 → NOSTUFF R7190 0 5% 1/20W MF 0201
ISUMN_C → NOSTUFF R7129 1K 1% 1/20W MF 201 → ISUMN_C_L_1
ISUMN_C_L_1 → NOSTUFF C7123 2200PF 10% 25V X7R 0201 → ISUMN_C_R
ISUMN_C_L_1 → R7127 374 1% 1/20W MF 201 → C7125 330PF 5% 25V NPO-COG 0201 → REG_VCC_U7100
ISUMN_C_R → NOSTUFF R7126 0 5% 1/20W MF 0201 → REG_VCC_U7100

ISUM_B

ISUMP_B (IN 65 63) → NOSTUFF R7106 11K 1% 1/20W MF 201 → ISUMN_B (IN 65)
ISUMN_B → NOSTUFF C7105 0.1UF 10% 6.3V X7R 0201 → ISUMN_B_L_2
ISUMN_B_L_2 → NOSTUFF R7107 0 5% 1/20W MF 0201
ISUMN_B → C7106 0.022UF 10% 6.3V X6S 0201
ISUMN_B → C7104 330PF 5% 25V NPO-COG 0201 → ISUMN_B_L_1
ISUMN_B_L_1 → R7105 348 1% 1/20W MF 201 → ISUMN_B_R
ISUMN_B_L_1 → R7108 1K 1% 1/20W MF 201 → C7103 2200PF 10% 25V CER-X7R 0201
REG_VCC_U7100 → NOSTUFF R7104 0 5% 1/20W MF 0201 → ISUMN_B_R
ISUMN_B_R → R7100 200KOHM-1% 0603-1
ISUMN_B_R → C7109 0.022UF 10% 25V X7R 0402 → ISEN1_B (65 63)
ISUMN_B_R → C7110 0.022UF 10% 25V X7R 0402 → ISEN2_B (65 63)
NTC_B_L → R7117 8.87K 1% 1/20W MF 201 → NTC_B_R → R7181 0 5% 1/20W MF 0201 → NTC_B

GT SENSE

CPU_VCCGTSENSE_P (IN 9) → R7115 10 1% 1/20W MF 201 → FB_B_L_4
FB_B_L_4 → R7114 0 5% 1/20W MF 0201 → FB_B_L_3
FB_B_L_4 → C7117 330PF 5% 25V NPO-COG 0201
FB_B_L_3 → R7112 1.87K 1% 1/20W MF 201 → FB_B (63)
FB_B_L_3 → C7113 2200PF 10% 25V CER-X7R 0201
FB_B_L_3 → R7113 510 1% 1/20W MF 201 → FB_B_L_2
FB_B (63) → R7110 1K 1% 1/20W MF 201 → FB_B_L_1
FB_B_L_1 → C7112 1000PF 5% 25V C0G-NP0 0201
FB_B_L_1 → C7199 120PF 5% 50V NPO-COG 0201
CPU_VCCGTSENSE_N (IN 9) → R7171 10 1% 1/20W MF 201 → VSSGT_SENSE_R (63)
VSSGT_SENSE_R → C7116 330PF 5% 25V NPO-COG 0201

SA SENSE

CPU_VCCSASENSE_P (IN 9) → R7125 10 1% 1/20W MF 201 → FB_C_L_4
FB_C_L_4 → R7124 0 5% 1/20W MF 0201 → FB_C_L_3
FB_C_L_4 → C7122 330PF 5% 25V NPO-COG 0201
FB_C_L_3 → R7123 3.83K 1% 1/20W MF 201 → FB_C (63)
FB_C_L_3 → C7118 1000PF 10% 16V X7R-1 0201
FB_C_L_3 → R7120 499 1% 1/20W MF 201 → FB_C_L_2
FB_C (63) → R7121 1.21K 1% 1/20W MF 201 → FB_C_L_1
FB_C_L_1 → C7120 820PF 10% 25V X7R-CERM 0201
CPU_VCCSASENSE_N (IN 9) → R7174 10 1% 1/20W MF 201 → VSSSA_SENSE_R (63)
VSSSA_SENSE_R → C7121 330PF 5% 25V NPO-COG 0201

U7100 ISL95828 TQFN CRITICAL OMIT_TABLE

PP5V_G3S (103) → R7101 1.00 1% 1/16W MF 402 → PPBUS_HS_CPU (102 73 66 65 64)
PPBUS_HS_CPU → R7102 0 5% 1/16W MF-LF 402 → REG_VCC_U7100 (63)
REG_VIN_U7100 → C7101 1UF 10% 25V X6S-CERM 0402
REG_VCC_U7100 → C7102 0.22UF 10% 16V X7R 0402-1

		41	VIN
		42	VCC
FCCM_B (OUT 65)	R7103 0 0201 MF 1/20W 5%	11	FCCM_B
PWM1_B (OUT 65)		12	PWM1_B
PWM2_B (OUT 65)		13	PWM2_B
ISUMP_B (63)		7	ISUMP_B
ISUMN_B_R (63)		8	ISUMN_B
ISEN1_B (65 63)		9	ISEN1_B
ISEN2_B (65 63)		10	ISEN2_B
COMP_B (63)		4	COMP_B
FB_B (63)		5	FB_B
VSSGT_SENSE_R (63)		6	RTN_B
REG_CPUVCC_GT_IMON		2	IMON_B
NTC_B (63)		3	NTC_B
FCCM_C (OUT 66)	R7118 0 0201 MF 1/20W 5%	34	FCCM_C
PWM_C (OUT 66)		35	PWM_C
ISUMP_C (66 63)		32	ISUMP_C
ISUMN_C_R (63)		33	ISUMN_C
COMP_C (63)		29	COMP_C
FB_C (63)		30	FB_C
VSSSA_SENSE_R (63)		31	RTN_C
REG_CPUVCC_SA_IMON		28	IMON_C
		40	PROG1
		39	PROG2
		38	PROG3
		37	PROG4
		36	PROG5
		49	THRM_PAD

C7111 220PF 5% 50V C0G 0201 → R7111 95.3K 1% 1/20W MF 201 → REG_CPUVCC_GT_IMON
C7119 39PF 5% 25V NP0-C0G 0201 → R7119 154K 1% 1/20W MF 201 → REG_CPUVCC_SA_IMON
XW7100 SM → C7127 4700PF 10% 10V X7R 201 → R7137 12.1K 1% 1/20W 201 MF
PROG1 → R7132 110K 1% 1/20W MF 201
PROG2 → R7133 215K 1% 1/20W MF 201
PROG3 → R7134 1.87K 1% 1/20W MF 201
PROG4 → R7135 165K 1% 1/20W MF 201
PROG5 → R7136 78.7K 1% 1/20W MF 201

FCCM_A	R7162 0 5% 1/20W MF 0201	24	FCCM_A_L
PWM1_A (OUT 64)		25	PWM1_A
PWM2_A (OUT 64)		26	PWM2_A
PWM3_A (OUT 64)		27	PWM3_A
ISUMP_A (63 64)		19	ISUMP_A
ISUMN_A (63)		20	ISUMN_A_L
ISEN1_A (63 64)		21	ISEN1_A
ISEN2_A (63 64)		22	ISEN2_A
ISEN3_A (63 64)		23	ISEN3_A
COMP_A (63)		16	COMP_A
FB_A (63)		17	FB_A
RTN_A		18	VSS_SENSE_R
IMON_A		14	REG_CPUVCC_IMON
NTC_A		15	NTC_A
VR_HOT		46	VR_HOT_L
VR_READY		47	PM_PGOOD_REG_CPUVCC (63)
VR_ENABLE		48	PM_EN_REG_CPUVCC_S0_R
SDA		43	SDA
ALERT*		44	ALERT
SCLK		45	SCLK
PSYS		1	PSYS

PM_EN_REG_CPUVCC_S0_R → R7148 0 5% 1/20W MF 0201 → PM_EN_REG_CPUVCC_S0 (47)
VR_HOT_L → R7147 75 1/20W 1% 201 MF → SMC_PROCHOT_L (OUT 38 45 46)
SMC_PROCHOT_L → NOSTUFF C7128 0.1UF 10% 6.3V X7R 0201
C7129 180PF 5% 50V CERM 402 → R7151 110K 1% MF 1/20W 201 → R7182 0 MF 5% 1/20W 0201 → NTC_A_L
NTC_A_L → R7150 8.87K 1% 1/20W MF 201 → NTC_A_R
I595 → R7116 200KOHM-1% 0603-1 → NTC_A_R

PLACE_NEAR=R7145.2:2.5mm
PLACE_NEAR=R7142.2:2.5mm
PLACE_NEAR=R7139.2:2.5mm
PP1V_S3 (IN 103)
PLACE_NEAR=U7100.43:2.5mm → R7138 45.3 1% 1/20W MF 201 → PP1V_S3
PLACE_NEAR=U7100.43:2.5mm → NOSTUFF R7141 100 1% 1/20W MF 201 → CPU_VIDSOUT (IN 8)
PLACE_NEAR=U7100.43:2.5mm → R7144 100 1% 1/20W MF 201 → CPU_VIDSOUT
PLACE_NEAR=U7100.44:2.5mm → R7145 10 1% 1/20W MF 201 → CPU_VIDSOUT
PLACE_NEAR=U7100.44:2.5mm → R7142 0 5% 1/20W MF 0201 → CPU_VIDALERT_L (OUT 8)
PLACE_NEAR=U7100.45:2.5mm → R7139 49.9 1% 1/20W MF 201 → CPU_VIDSCLK (IN 8)

BOM_COST_GROUP=CPU & CHIPSET

L7100 0.105UH-20%-31A-0.000320HM

PP12V_MAIN (102) → L7100 SSL0705M-SM CRITICAL → PP12V_S0_CPUCORE_FLT (51 105 107)

ISUM_A

NOSTUFF R7159 0 5% 1/20W MF 0201 → REG_VCC_U7100 (63)
ISUMN_A_L (63) → R7161 464 1% 1/20W MF 201 → ISUMN_A_R
ISUMN_A_R → R7160 1K 1% 1/20W MF 201
ISUMN_A_R → C7136 2200PF 10% 25V CER-X7R 0201
ISUMN_A_R → C7141 330PF 5% 25V NPO-COG 0201 → ISUMP_A (IN 63 64)
ISUMP_A → NOSTUFF C7140 0.1UF 10% 6.3V X7R 0201
ISUMP_A → NOSTUFF R7163 11K 1% 1/20W MF 201 → ISUMN_A (IN 64)
ISUMP_A → NOSTUFF R7164 0 5% 1/20W MF 0201
C7141 → C7137 0.022UF 10% 25V X7R 0402 → ISEN1_A (63 64)
C7141 → C7138 0.022UF 10% 25V X7R 0402 → ISEN2_A (64 63)
C7141 → C7139 0.022UF 10% 25V X7R 0402 → ISEN3_A (63 64)
ISUMN_A → C7144 0.01UF 10% 16V X7R-CERM 0201

COMP A,B,C

C7115 150PF 5% 50V CER-C0G 0201 → COMP_C (63)
COMP_C → C7114 0.0068UF 10% 25V X7R-CERM 0402 → COMP_C_L
COMP_C_L → R7122 2.7K 1% 1/20W MF 201
COMP_C → C7107 100PF 5% 25V C0G 0201 → COMP_B (63)
COMP_B → C7108 0.0082UF 10% 25V X7R 402 → COMP_B_L
COMP_B_L → R7109 4.99K 1% 1/20W MF 201
COMP_B → C7135 68PF 5% 50V C0G 0201 → COMP_A (63)
COMP_A → R7158 4.99K 1% 1/20W MF 201 → COMP_A_R
COMP_A_R → C7134 0.0082UF 10% 25V X7R 402

VCC SENSE

FB_A (63) → R7153 4.99K 1% 1/20W MF 201 → FB_A_R_3
FB_A_R_3 → R7155 0 5% 1/20W MF 0201 → FB_A_R_4
FB_A_R_4 → R7156 10 1% 1/20W MF 201 → CPU_VCCSENSE_P (IN 9)
FB_A_R_4 → C7132 330PF 5% 25V NPO-COG 0201
FB_A_R_1 → R7152 2K 1% 1/20W MF 201 → C7130 330PF 5% 25V X7R 0201
FB_A_R_2 → C7131 1500PF 10% 10V X7R 0201
FB_A_R_2 → R7154 1K 1% 1/20W MF 201
VSS_SENSE_R (63) → R7176 10 1% 1/20W MF 201 → CPU_VCCSENSE_N (IN 9)
VSS_SENSE_R → C7133 330PF 5% 25V NPO-COG 0201

PAGE TITLE: CPU & CHIPSET: CPU CORE VR

Apple Inc.

DRAWING NUMBER	051-02424
SIZE	D
REVISION	6.0.0
BRANCH	dvt-1
PAGE	71 OF 142
SHEET	63 OF 115

CPU VCC Regulator

EDC = 128A
TDC = 91A
Fsw = 583KHz

CPU VCORE Phase 1

PPBUS_HS_CPU
PP5V_G3S
FCCM_A
PWM1_A
PP5V_S0_VRD_VCIN_A1
BOOST_A_1_RC
BOOST_A_1
PHASE_A_1
SW_A_1
U7210 SIC621CD MLP-COMBO CRITICAL
R7227 MF-LF 1/16W 5% 402 VOLTAGE=5V
R7216 0 5% 1/10W MF-LF 603 DIDT=TRUE
C7216 0.22UF 10% 25V X7R 0402-1
C7228 1UF 10% 25V X6S-CERM 0402
C7211 CRITICAL 10UF 20% 16V X6S-CERM 0603
C7200 12PF 5% 25V NP0-C0G 0201
C7201 3.0PF +/-0.1PF 25V NP0-C0G 0201
C7202 12PF 5% 25V NP0-C0G 0201
C7203 3.0PF +/-0.1PF 25V NP0-C0G 0201
C7204 12PF 5% 25V NP0-C0G 0201
C7205 3.0PF +/-0.1PF 25V NP0-C0G 0201
C7206 12PF 5% 25V NP0-C0G 0201
C7207 3.0PF +/-0.1PF 25V NP0-C0G 0201
C7208 12PF 5% 25V NP0-C0G 0201
C7209 3.0PF +/-0.1PF 25V NP0-C0G 0201
C7297 CRITICAL NOSTUFF 15UF 20% 16V TANT SM
C7226 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7225 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7296 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7229 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7212 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7213 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7218 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7219 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7220 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7221 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7214 EMC CRITICAL 1UF 10% 25V X6S-CERM 0402
C7215 EMC CRITICAL 1UF 10% 25V X6S-CERM 0402
L7210 CRITICAL 0.22UH-20%-65A-0.000640HM PIME104T-SM
R7210 CRITICAL 0.0005 1% 1W MF 0612-2 VOLTAGE=1.52V
PPCPUVCC_S0_SENSE_1_1
PPVCC_S0_CPU_REG
C7217 NOSTUFF 0.001UF 10% 50V X7R-CERM 0402
R7217 NOSTUFF 2.2 5% 1/8W AE-LF 805
REG_SNUBBER_CPUVCC_1
REG_CPUVCC_ISNS_1_P
REG_CPUVCC_ISNS_1_N
R7218 3.9 1% 1/20W MF 201 NO_XNET_CONNECTION=1 ISUMN_A
R7219 1K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
R7220 100K 1% 1/20W MF 201
R7221 100K 1% 1/20W MF 201 NO_XNET_CONNECTION=1 REG_CPUVCC_ISNS_2_N
R7222 100K 1% 1/20W MF 201 NO_XNET_CONNECTION=1 REG_CPUVCC_ISNS_3_N
ISEN1_A
ISUMP_A

CPU VCORE Phase 2

PPBUS_HS_CPU
PP5V_G3S
FCCM_A
PWM2_A
PP5V_S0_VRD_VCIN_A2
BOOST_A_2_RC
BOOST_A_2
PHASE_A_2
SW_A_2
U7230 SIC621CD MLP-COMBO CRITICAL
R7247 MF-LF 1/16W 5% 402 VOLTAGE=5V
R7236 0 5% 1/10W MF-LF 603 DIDT=TRUE
C7236 0.22UF 10% 25V X7R 0402-1
C7248 1UF 10% 25V X6S-CERM 0402
C7247 CRITICAL 10UF 20% 16V X6S-CERM 0603
C7298 CRITICAL NOSTUFF 15UF 20% 16V TANT SM
C7244 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7245 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7246 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7230 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7232 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7233 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7238 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7239 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7240 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7241 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7234 EMC CRITICAL 1UF 10% 25V X6S-CERM 0402
C7231 EMC CRITICAL 1UF 10% 25V X6S-CERM 0402
L7230 CRITICAL 0.22UH-20%-65A-0.000640HM PIME104T-SM
R7230 CRITICAL 0.0005 1% 1W MF 0612-2 VOLTAGE=1.52V
PPCPUVCC_S0_SENSE_2_1
PPVCC_S0_CPU_REG
C7237 NOSTUFF 0.001UF 10% 50V X7R-CERM 0402
R7237 NOSTUFF 2.2 5% 1/8W AE-LF 805
REG_SNUBBER_CPUVCC_2
REG_CPUVCC_ISNS_2_P
REG_CPUVCC_ISNS_2_N
R7238 3.9 1% 1/20W MF 201 NO_XNET_CONNECTION=1 ISUMN_A
R7239 1K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
R7240 100K 1% 1/20W MF 201
R7241 100K 1% 1/20W MF 201 NO_XNET_CONNECTION=1 REG_CPUVCC_ISNS_1_N
R7242 100K 1% 1/20W MF 201 NO_XNET_CONNECTION=1 REG_CPUVCC_ISNS_3_N
ISEN2_A
ISUMP_A

CPU Phase 3

PPBUS_HS_CPU
PP5V_G3S
FCCM_A
PWM3_A
PP5V_S0_VRD_VCIN_A3
BOOST_A_3_RC
BOOST_A_3
PHASE_A_3
SW_A_3
U7250 SIC621CD MLP-COMBO CRITICAL
R7267 MF-LF 1/16W 5% 402 VOLTAGE=5V
R7256 0 5% 1/10W MF-LF 603 DIDT=TRUE
C7256 0.22UF 10% 25V X7R 0402-1
C7268 1UF 10% 25V X6S-CERM 0402
C7267 CRITICAL 10UF 20% 16V X6S-CERM 0603
C7299 CRITICAL NOSTUFF 15UF 20% 16V TANT SM
C7272 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7271 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7270 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7250 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7252 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7253 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7261 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7258 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7259 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7260 CRITICAL 1UF 10% 25V X6S-CERM 0402
C7254 EMC CRITICAL 1UF 10% 25V X6S-CERM 0402
C7255 EMC CRITICAL 1UF 10% 25V X6S-CERM 0402
L7250 CRITICAL 0.22UH-20%-65A-0.000640HM PIME104T-SM
R7250 CRITICAL 0.0005 1% 1W MF 0612-2 VOLTAGE=1.52V
PPCPUVCC_S0_SENSE_3_1
PPVCC_S0_CPU_REG
C7257 NOSTUFF 0.001UF 10% 50V X7R-CERM 0402
R7257 NOSTUFF 2.2 5% 1/8W AE-LF 805
REG_SNUBBER_CPUVCC_3
REG_CPUVCC_ISNS_3_P
REG_CPUVCC_ISNS_3_N
R7258 3.9 1% 1/20W MF 201 NO_XNET_CONNECTION=1 ISUMN_A
R7259 1K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
R7260 100K 1% 1/20W MF 201
R7261 100K 1% 1/20W MF 201 NO_XNET_CONNECTION=1 REG_CPUVCC_ISNS_1_N
R7262 100K 1% 1/20W MF 201 NO_XNET_CONNECTION=1 REG_CPUVCC_ISNS_2_N
ISEN3_A
ISUMP_A

BOM_COST_GROUP=CPU & CHIPSET

DRAWING: LAST_MODIFIED=Thu Jul 12 17:56:51 2018
PAGE TITLE: CPU & CHIPSET: CPU CORE VR (VCC)

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DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 72 OF 142
SHEET 64 OF 115

CPU VCCGT Regulator

EDC = 32A

TDC = 25A

Fsw = 583KHz

CPU VCCGT Phase 1

CPU VCCGT Phase 2

U7310 SIC621CD MLP-COMBO CRITICAL

U7330 SIC621CD MLP-COMBO CRITICAL

L7310 0.22UH-20%-65A-0.000640HM PIME104T-SM

L7330 0.22UH-20%-65A-0.000640HM PIME104T-SM

PPCPUVCCGT_S0_SENSE_1_1 VOLTAGE=1.52V

PPCPUVCCGT_S0_SENSE_2_1 VOLTAGE=1.52V

PPVCCGT_S0_CPU_REG

REG_SNUBBER_CPUVCCGT_1

REG SNUBBER CPUVCCGT 2

REG_VCCGT_ISNS_1_P

REG_VCCGT_ISNS_1_N

REG_VCCGT_ISNS_2_P

REG_VCCGT_ISNS_2_N

ISUMN_B

ISUMP_B

ISEN1_B

ISEN2_B

BOM_COST_GROUP=CPU & CHIPSET

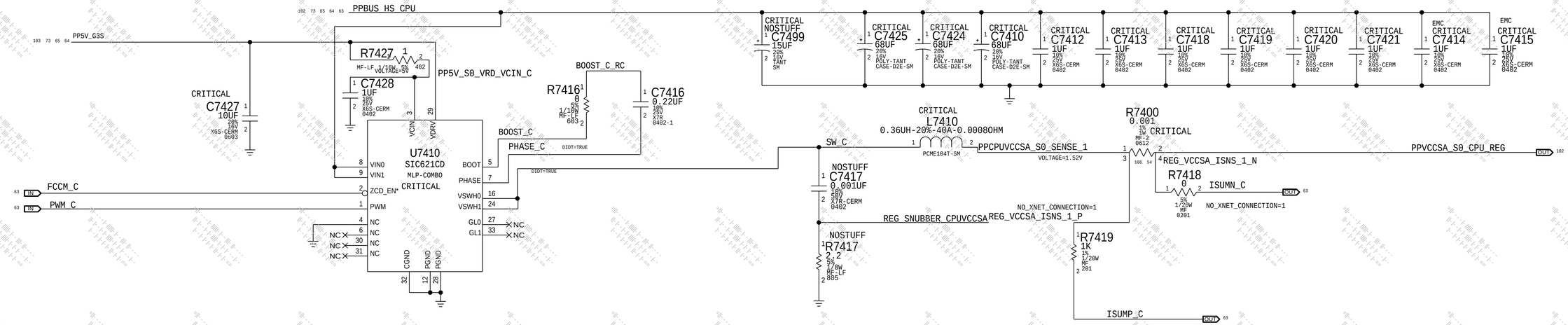
DRAWING	LAST_MODIFIED=Thu Jul 12 17:57:07 2018
PAGE TITLE	CPU & CHIPSET: CPU CORE VR (VCCGT)
Apple Inc.	DRAWING NUMBER 051-02424 SIZE D
	REVISION 6.0.0
	BRANCH dvt-1
	PAGE 73 OF 142
	SHEET 65 OF 115

CPU VCCSA Regulator

EDC = 11.1A

TDC = 10A

Fsw = 583KHz



BOM_COST_GROUP=CPU & CHIPSET

DRAWING LAST_MODIFIED=Thu Jul 12 17:57:07 2018

PAGE TITLE: CPU & CHIPSET: CPU CORE VR (VCCSA)

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

BRANCH dvt-1

PAGE 74 OF 142

SHEET 66 OF 115

VDDQ S3 REGULATOR

VDDQ = 1.2V @ 8.43A (EDC)

VTT = 0.6V @ 1A (EDC)

VPP = 2.5V @ 0.384A (EDC)

Fsw = 500KHz

Vout = 1.8 * (Rb / (Ra + Rb))

Critical:
Need copper around Q7510
to sink heat

BOM_COST_GROUP=DRAM

PAGE TITLE	CPU & CHIPSET: CPU VDDQ VR
DRAWING NUMBER	051-02424
SIZE	D
REVISION	6.0.0
BRANCH	dvt-1
PAGE	75 OF 142
SHEET	67 OF 115

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3.3V G3H Regulator

EDC = 16A

TDC = 13.6A

Fsw = 500KHz

5V G3S Regulator

EDC = 13.5A

TDC = 13.5A

Fsw = 500KHz

Vout = 0.6 * (1 + Ra / Rb)

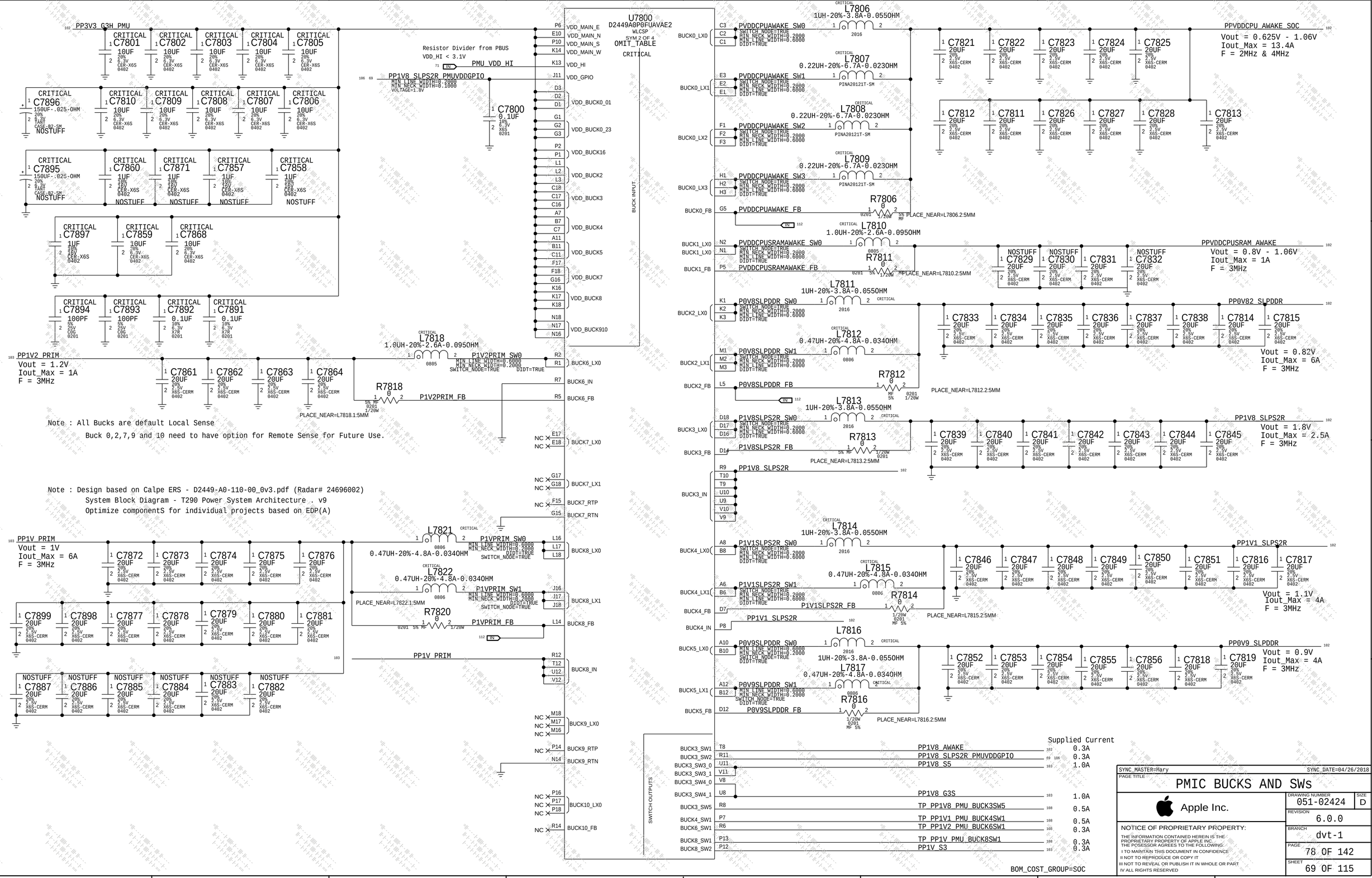
Vout = 0.6 * (1 + Ra / Rb)

Need a Divider from 12V input to enable 3V3G3H?

Enable from Calpe

PAGE TITLE	PLATFORM POWER: 3.3V G3H/5V G3S VR
Apple Inc.	DRAWING NUMBER 051-02424 SIZE D
	REVISION 6.0.0
	BRANCH dvt-1
	PAGE 76 OF 142
	SHEET 68 OF 115

BOM_COST_GROUP=PLATFORM POWER


U7800
D2449A0P0FUAVAE2
WLCSP
SYM 2 OF 4
OMIT_TABLE
CRITICAL
BUCK INPUT
VDD_MAIN_E
VDD_MAIN_N
VDD_MAIN_S
VDD_MAIN_W
VDD_HI
VDD_GPIO
VDD_BUCK0_01
VDD_BUCK0_23
VDD_BUCK16
VDD_BUCK2
VDD_BUCK3
VDD_BUCK4
VDD_BUCK5
VDD_BUCK7
VDD_BUCK8
VDD_BUCK910
PP3V3_G3H_PMU
PP1V2_PRIM
Vout = 1.2V
Iout_Max = 1A
F = 3MHz
Resistor Divider from PBUS
VDD_HI < 3.1V
PMU_VDD_HI
PP1V8_SLPS2R_PMUVDDGPIO
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.8V
C7800 0.1UF
L7818 1.0UH-20%-2.6A-0.095OHM
P1V2PRIM_SW0
R7818 0
P1V2PRIM_FB
PLACE_NEAR=L7818.1:5MM
BUCK6_LX0
BUCK6_IN
BUCK6_FB
BUCK7_LX0
BUCK7_LX1
BUCK7_RTP
BUCK7_RTN
L7821 0.47UH-20%-4.8A-0.034OHM
P1VPRIM_SW0
L7822 0.47UH-20%-4.8A-0.034OHM
P1VPRIM_SW1
R7820 0
P1VPRIM_FB
PLACE_NEAR=L7822.1:5MM
PP1V_PRIM
BUCK8_LX0
BUCK8_LX1
BUCK8_FB
BUCK8_IN
BUCK9_LX0
BUCK9_RTP
BUCK9_RTN
BUCK10_LX0
BUCK10_FB
Note : All Bucks are default Local Sense
Buck 0,2,7,9 and 10 need to have option for Remote Sense for Future Use.
Note : Design based on Calpe ERS - D2449-A0-110-00_0v3.pdf (Radar# 24696002)
System Block Diagram - T290 Power System Architecture . v9
Optimize componentS for individual projects based on EDP(A)
L7806 1UH-20%-3.8A-0.055OHM
L7807 0.22UH-20%-6.7A-0.023OHM
L7808 0.22UH-20%-6.7A-0.023OHM
L7809 0.22UH-20%-6.7A-0.023OHM
R7806 0
PLACE_NEAR=L7806.2:5MM
L7810 1.0UH-20%-2.6A-0.095OHM
R7811 0
PLACE_NEAR=L7810.2:5MM
L7811 1UH-20%-3.8A-0.055OHM
L7812 0.47UH-20%-4.8A-0.034OHM
R7812 0
PLACE_NEAR=L7812.2:5MM
L7813 1UH-20%-3.8A-0.055OHM
R7813 0
PLACE_NEAR=L7813.2:5MM
L7814 1UH-20%-3.8A-0.055OHM
L7815 0.47UH-20%-4.8A-0.034OHM
R7814 0
PLACE_NEAR=L7815.2:5MM
L7816
L7817 0.47UH-20%-4.8A-0.034OHM
R7816 0
PLACE_NEAR=L7816.2:5MM
PPVDDCPU_AWAKE_SOC
Vout = 0.625V - 1.06V
Iout_Max = 13.4A
F = 2MHz & 4MHz
PPVDDCPUSRAM_AWAKE
Vout = 0.8V - 1.06V
Iout_Max = 1A
F = 3MHz
PP0V82_SLPDDR
Vout = 0.82V
Iout_Max = 6A
F = 3MHz
PP1V8_SLPS2R
Vout = 1.8V
Iout_Max = 2.5A
F = 3MHz
PP1V1_SLPS2R
Vout = 1.1V
Iout_Max = 4A
F = 3MHz
PP0V9_SLPDDR
Vout = 0.9V
Iout_Max = 4A
F = 3MHz
SWITCH OUTPUTS
Supplied Current
PP1V8_AWAKE 0.3A
PP1V8_SLPS2R_PMUVDDGPIO 0.3A
PP1V8_S5 1.0A
PP1V8_G3S 1.0A
TP_PP1V8_PMU_BUCK3SW5 0.5A
TP_PP1V1_PMU_BUCK4SW1 0.5A
TP_PP1V2_PMU_BUCK6SW1 0.3A
TP_PP1V_PMU_BUCK8SW1 0.3A
PP1V_S3 0.3A
BOM_COST_GROUP=SOC
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
PMIC BUCKS AND SWS
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 78 OF 142
SHEET 69 OF 115
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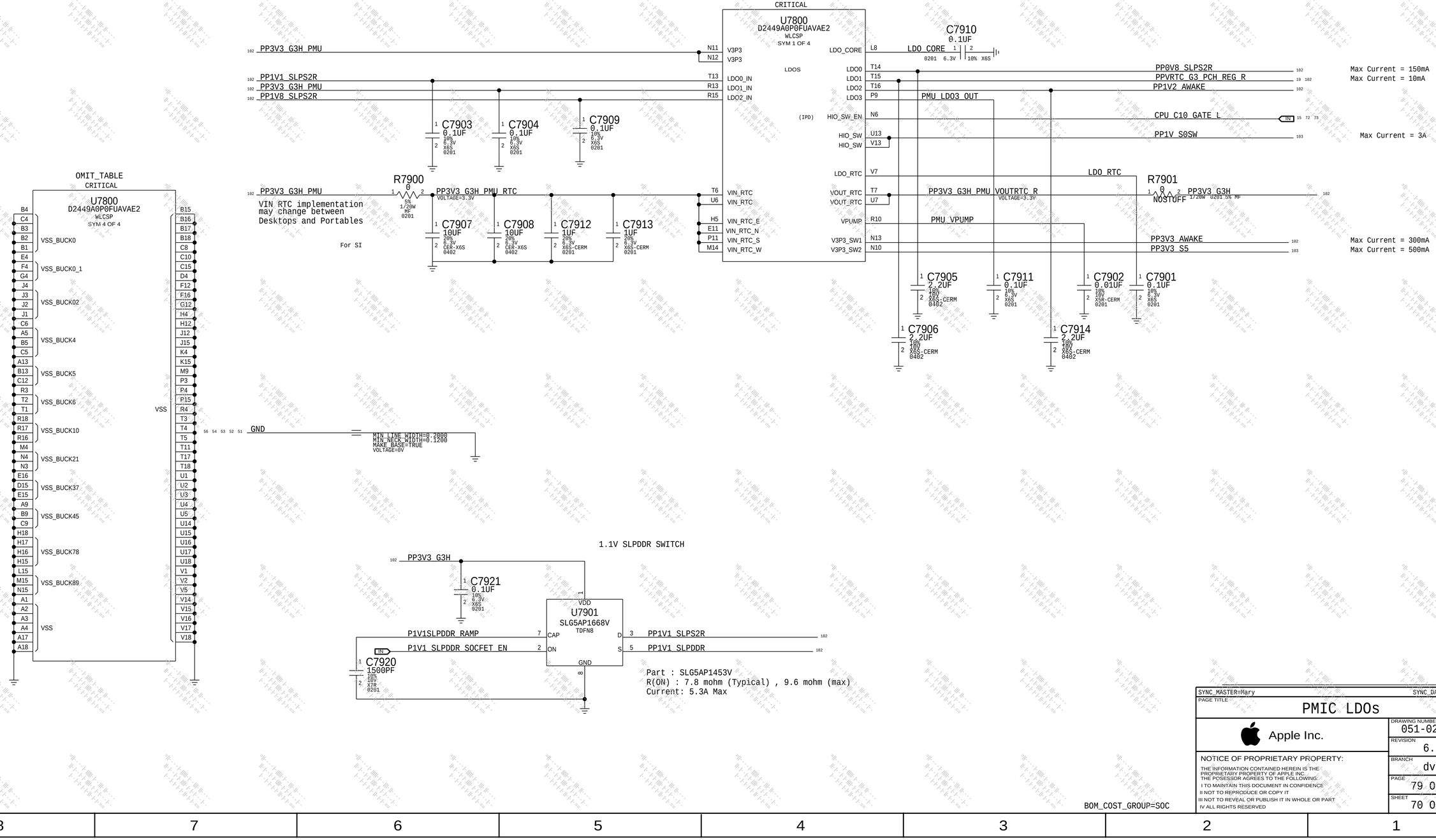
OMIT_TABLE
CRITICAL
U7800
D2449A0P0FUAVAE2
WLCSP
SYM 4 OF 4
VSS_BUCK0
VSS_BUCK0_1
VSS_BUCK02
VSS_BUCK4
VSS_BUCK5
VSS_BUCK6
VSS_BUCK10
VSS_BUCK21
VSS_BUCK37
VSS_BUCK45
VSS_BUCK78
VSS_BUCK89
VSS
VSS
GND
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
MAKE_BASE=TRUE
VOLTAGE=0V
OMIT_TABLE
CRITICAL
U7800
D2449A0P0FUAVAE2
WLCSP
SYM 1 OF 4
PP3V3_G3H_PMU
PP1V1_SLPS2R
PP3V3_G3H_PMU
PP1V8_SLPS2R
V3P3
V3P3
LDO0_IN
LDO1_IN
LDO2_IN
LDOS
C7903 0.1UF
C7904 0.1UF
C7909 0.1UF
PP3V3_G3H_PMU
R7900 0
VIN RTC implementation
may change between
Desktops and Portables
For SI
PP3V3_G3H_PMU_RTC
VOLTAGE=3.3V
C7907 10UF
C7908 10UF
C7912 1UF
C7913 1UF
VIN_RTC
VIN_RTC
VIN_RTC_E
VIN_RTC_N
VIN_RTC_S
VIN_RTC_W
LDO_CORE
LDO0
LDO1
LDO2
LDO3
HIO_SW_EN
HIO_SW
HIO_SW
LDO_RTC
VOUT_RTC
VOUT_RTC
VPUMP
V3P3_SW1
V3P3_SW2
C7910 0.1UF
LDO_CORE
PP0V8_SLPS2R
PPVRTC_G3_PCH_REG_R
PP1V2_AWAKE
PMU_LDO3_OUT
CPU_C10_GATE_L
PP1V_S0SW
LDO_RTC
R7901 0
NOSTUFF
PP3V3_G3H
PP3V3_G3H_PMU_VOUTRTC_R
VOLTAGE=3.3V
PMU_VPUMP
PP3V3_AWAKE
PP3V3_S5
C7905 2.2UF
C7906 2.2UF
C7911 0.1UF
C7914 2.2UF
C7902 0.01UF
C7901 0.1UF
Max Current = 150mA
Max Current = 10mA
Max Current = 3A
Max Current = 300mA
Max Current = 500mA
1.1V SLPDDR SWITCH
PP3V3_G3H
C7921 0.1UF
U7901
SLG5AP1668V
TDFN8
VDD
CAP
ON
GND
P1V1SLPDDR_RAMP
P1V1_SLPDDR_SOCFET_EN
PP1V1_SLPS2R
PP1V1_SLPDDR
C7920 1500PF
Part : SLG5AP1453V
R(ON) : 7.8 mohm (Typical) , 9.6 mohm (max)
Current: 5.3A Max
BOM_COST_GROUP=SOC
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
PMIC LDOs
Apple Inc.
DRAWING NUMBER
051-02424
SIZE
D
REVISION
6.0.0
BRANCH
dvt-1
PAGE
79 OF 142
SHEET
70 OF 115
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OMIT_TABLE
CRITICAL

U7800
D2449A0P0FUAVAE2
WLCSP
SYM 3 OF 4

RESET_IN1 (1V8_PU@VR)
RESET_IN2
RESET_IN3 (IPD)
RESET_IN4
RESET_IN5 (IPD)
RESET*

SYS_SLEEP*
ACTIVE_RDY
CLKOUT0_32K
CLKOUT1_32K
CLKOUT2_32K
CLKOUT3_32K
CLKOUT4_32K
SYS_ALIVE
FORCE_DFU
IRQ*
SCL
SDA
SCLK
SDATA
SYS_ACTIVE
SYS_BTN
AMUX_A0
AMUX_A1
AMUX_A2
AMUX_A3
AMUX_A4
AMUX_A5
AMUX_A6
AMUX_A7
AMUX_AY
AMUX_B0
AMUX_B1
AMUX_B2
AMUX_B3
AMUX_B4
AMUX_B5
AMUX_B6
AMUX_B7
AMUX_BY
LS_BID1 (IPU)
LS_BID2 (IPU)

RESETS
REFS
COMPARATOR
SPMI
AMUX
BUTTON
GPIO
XTAL

IREF L12 PMU_IREF
VREF K12 PMU_VREF
C8001 0.1UF 10% 6.3V X6S 0201
R8001 200K 1% 1/20W MF 201

VDROOP L7 PMU_DROOP_L OUT 37 71
VDROOP_DET M5 SOC_VDDCPU_SENSE IN 41 108
CHG_CBC_ON E9 PMU_CHGR_CBC_ON 71 No Charger support
NCHG_INT J6 PMU_CHGR_INT_L 71 No Charger support,PD or PU for INT?
CHG_POK L4 PMU_CHGR_AUX_OK 71 No Charger support
VPWR_EN D5 PMU_PVDDMAIN_EN OUT 68 106
LDO1_POK M13 PCH_RTC_RESET_L OUT 12 106
PFN E8 NC
VIN_BBAT V6 PPVBATT_G3_RTC_R VOLTAGE=3.0V 19
To be Grounded on Portables Only, RC on Coin Cell on Desktops

(IPU) BUTTON1 N7 PMU_ONOFF_L IN 71 100 106
(IPU) BUTTON2 M6 PMU_RSLOC_RST_L 71

GPIO1 D9 P3V3MAIN_PGOOD (3V3_G3H PU@VR) IN 47 108 110
GPIO2 F8 TP_P3V3G3W_EN OUT 108
GPIO3 E7 TP_P3V3G3W_PGOOD IN
GPIO4 F6 P5VG3S_EN OUT 47 71 100 106
GPIO5 F7 P5VG3S_PGOOD (1V8_G3S PU@VR) IN 47 106
GPIO6 D8 P3V3G3S_EN OUT 47 71 106
GPIO7 F9 TP_P1V8G3S_EN OUT 106
GPIO8 F10 CPUVR_PGOOD (1V8_S5 PU@VR) IN 47 106 110
GPIO9 G10 PVCCIO_EN OUT 71 73 106
GPIO10 G9 PVCCIO_PGOOD (1V8_S5 PU@VR) IN 47 108
GPIO11 G8 PVDDQ_EN OUT 47 71 106
GPIO12 G7 PVDDQ_PGOOD IN 47 107 110
GPIO13 G6 FAN_PWR_EN OUT 57 71 108
GPIO14 H8 WLAN_PWR_EN OUT 35 36 108
GPIO15 H9 BT_PWR_EN OUT 35 36 108
GPIO16 J9 TP_SE_PWR_EN 108
GPIO17 J8 TP_P3V3_S5_EN 108
(IPD) GPIO18 K9 PVCCPLLOC_EN OUT 72 108
GPIO19 K10 TP_PVCCEOPIOEDRAM_P2V7NAND_PGOOD 108
GPIO20 J10 TP_PEARL_P2V7NAND_EN 108
GPIO21 H10 TP_NAND_DISCHARGE_HDD_PWR_EN 108
GPIO22 H11 TP_NAND_RESET_L_SD_PWR_EN 108
GPIO23 G11 ENET_PWR_EN OUT 71 72 85 86 87 108
GPIO24 F11 TBT_PWR_EN OUT 71 72 108
GPIO25 D10 P1V1_SLPDDR_SOCFET_EN OUT 70 71 106

Because consolidate G3H and G3W rails on J174

106 38 OUT PMU_CLK32K_SOC
12 OUT PMU_CLK32K_PCH
R8012 33 5% 1/20W MF 201
R8011 33 5% 1/20W MF 201

106 38 IN SOC_WDOG F5
113 106 37 IN SOC_SOCHOT_L E5
106 28 IN UPC_PMU_RESET K5
20 6 IN CPU_THRMTRIP_L K6
104 IN NC_GPU_THRMTRIP N5
38 OUT PMU_COLD_RESET_L L13
100 38 12 IN PM_SLP_S0_L M12
106 71 37 110 108 29 OUT PMU_ACTIVE_READY J5

PMU_CLK32K_SOC_R H6
PMU_CLK32K_PCH_R H7
106 35 OUT PMU_CLK32K_WLANBT_R J7
NC_PMU_CLK32K_GNSS_R K7
NC_PMU_CLK32K_OUT4 K8

106 88 79 71 38 37 OUT PMU_SYS_ALIVE L11
113 106 37 28 OUT SOC_FORCE_DFU R8010 2.2K 1/20W 201 5% MF PMU_FORCE_DFU D6
Use SOC's Internal Pull Up
OUT PMU_INT_L L9
112 IN I2C_PMU_SCL M11
112 BI I2C_PMU_SDA L10

38 IN SPMI_CLK M8
38 BI SPMI_DATA M7
110 106 71 45 OUT ALL_SYS_PWRGD K11
71 20 18 OUT PM_PWRBTN_L D11

46 PMU_P3V3_CAPLE_ISENSE A16
46 PMU_CPUSA_ISENSE A15
46 PMU_DDR2V5_ISENSE A14
108 46 PMU_VCCIO_ISENSE B14
108 46 PMU_P5V_G3S_HI_ISENSE D13
108 46 PMU_CPUSA_VSENSE C14
108 46 PMU_P5V_USBC_ISENSE E14
108 46 PMU_P5V_USBA_ISENSE F14
106 TP_PMU_AMUX_AY J14
108 46 PMU_P3V3_TBT_ISENSE C13
108 46 PMU_P3V3_SSD0_ISENSE E13
108 46 PMU_PBUS_SSD0_ISENSE E12
108 46 PMU_P3V3_G3H_HI_ISENSE F13
108 46 PMU_P3V3_WLANBT_ISENSE G13
108 46 PMU_P3V3_ENET_ISENSE G14
108 46 PMU_P12V_ENET_ISENSE H14
108 TP_PMU_AMUX_B7 H13
108 TP_PMU_AMUX_BY J13

NC N9
NC M10

Caution : AMUX programmed with Gain 1 should not have inputs greater than 1.5V

R8013 0 1/20W 5% MF 0201
PMU_XTAL1_R 109
CRITICAL
Y8001 32.768KHZ-20PPM-12.5PF 1.60X1.00-SM
NOSTUFF
R8018 1M 5% 1/20W MF 201 109
C8002 18PF 5% 25V C0G-CERM 0201
C8003 18PF 5% 25V C0G-CERM 0201
C8004 0.1UF 10% 6.3V X6S 0201

PMU_XTAL1 V3
PMU_XTAL2 V4
71 110 6 IN CPU_CATERR_L L6
PMU_VDD_MAX N8
VDD_MAX
E6 VDD_OTP

PP12V_MAIN 102
R8050 1.15M 1% 1/20W TK 0201
PMU_VDD_HI OUT 69
NOSTUFF C8051 220PF 10% 25V X7R-CERM 0201
R8051 357K 1% 1/20W MF 201

PBUS	Rising Vth	Falling Vth
2S	6.059V	5.636V
3S	9.076V	8.443V
12V	9.076V	8.443V

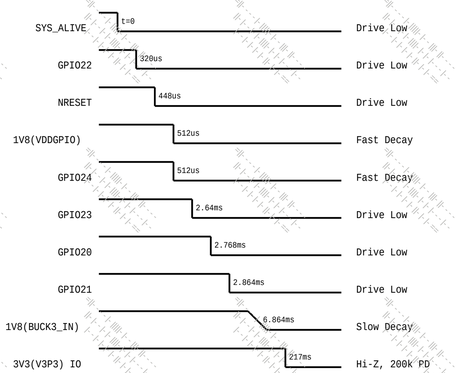
PP1V_S3 103
PP3V3_G3H_PMU 102
PP1V8_AWAKE 102
PP1V8_S5 35 50 103
PP3V3_S5 12 16 17 103
PP1V8_SLPS2R 102

R8002 10K 1/20W 201 5% MF PMU_COLD_RESET_L 38 71 106 108
R8003 10K 1/20W 201 5% MF PMU_SYS_ALIVE 37 38 71 79 88 106
R8004 0 1/20W 0201 5% MF NOSTUFF PMU_CHGR_INT_L No Charger support
R8007 10K 1/20W 201 5% MF PM_PWRBTN_L 18 20 71

R8005 10K 1/20W 201 5% MF ALL_SYS_PWRGD 45 71 106 110
R8006 10K 1/20W 201 5% MF PMU_DROOP_L 37 71
R8015 10K 1/20W 201 5% MF PMU_ONOFF_L 71 100 106
R8014 10K 1/20W 201 5% MF NOSTUFF PMU_RSLOC_RST_L 71
R8017 51 1/20W 201 5% MF CPU_CATERR_L 6 71 110
R8019 0 1/20W 0201 5% MF PMU_CHGR_CBC_ON 71 No Charger support
R8021 0 1/20W 0201 5% MF PMU_CHGR_AUX_OK 71 No Charger support
R8022 0 1/20W 0201 5% MF PMU_CHGR_INT_L 71 No Charger support

R8020 47K 1/20W 201 5% MF NOSTUFF FAN_PWR_EN 57 71 108
R8000 47K 1/20W 201 5% MF P5VG3S_EN 47 71 100 106
R8008 47K 1/20W 201 5% MF TBT_PWR_EN 71 72 108
R8009 47K 1/20W 201 5% MF P3V3G3S_EN 47 71 106
R8016 47K 1/20W 201 5% MF NOSTUFF PVCCIO_EN 71 73 106
R8023 47K 1/20W 201 5% MF PVDDQ_EN 47 71 106
R8024 47K 1/20W 201 5% MF NOSTUFF ENET_PWR_EN 71 72 85 86 87 108
R8025 47K 1/20W 201 5% MF NOSTUFF P1V1_SLPDDR_SOCFET_EN 70 71 106
R8026 47K 1/20W 201 5% MF NOSTUFF PMU_ACTIVE_READY 29 37 71 106 108 110

Power-Down Sequencing during forced shutdown
(Calpe RESET_IN, VDD_HI low, Calpe VR failure)
GPIO20-25 turn off independantly unless their domain disables first



BOM_COST_GROUP=SOC

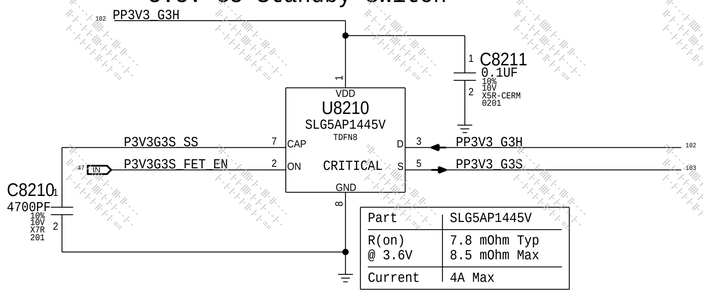
SYNC_MASTER=Mary SYNC_DATE=04/26/2018
PAGE TITLE: PMIC GPIOs Controls
Apple Inc.
DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 80 OF 142
SHEET 71 OF 115

System Power States

System State:	Shutdown (G3H)		Standby (G3S)		Standby (S4)		Sleep (S0i/S3)		Run (S0)
CPU/PCH State:	Off (RTC Only)		Off (RTC Only)		Standby		Sleep		Run
Rails / SoC State:	S2R	Awake	S2R	Awake	S2R	Awake	S2R	Awake	Awake
PP*_S2R (0.8,1.1,1.8V)	On	On	On	On	On	On	On	On	On
PP*_DDR (0.8,0.9,1.1V)	Off	On	Off	On	Off	On	Off	On	On
PP*_AWAKE (CPU,SRAM,1.2,1.8,3.3V)	Off	On	Off	On	Off	On	Off	On	On
PP3V3_G3H (VR1)	On	On	On	On	On	On	On	On	On
PP1S_G3H	On	On	On	On	On	On	On	On	On
PP3V3_G3W	Off	On	Off	On	On	On	On	On	On
PP*_G3S (1.8,3.3,5V)	Off	On	On	On	On	On	On	On	On
PP*_S5 (1.8,3.3V)	Off	Off	Off	Off	On	On	On	On	On
CPU/PCH VRs	Off	Off	Off	Off	Off/On	Off/On	Off/On	Off/On	On

* System: Shutdown Awake is a transition state only.
* SoC: SLP_DDR is a transition state only.
* CPU/PCH: S4 is only used by desktops for USB wakes.
* CPU/PCH: S5 is a transition state. May also be used for RTC wakes.

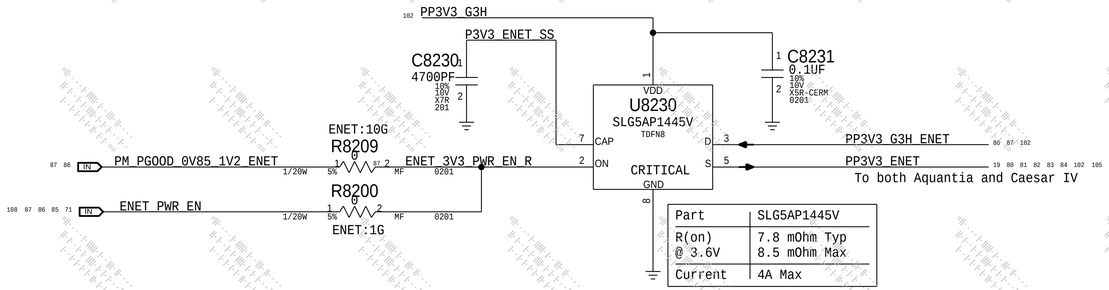
3.3V G3 Standby Switch



Part	SLG5AP1445V
R(on) @ 3.6V	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

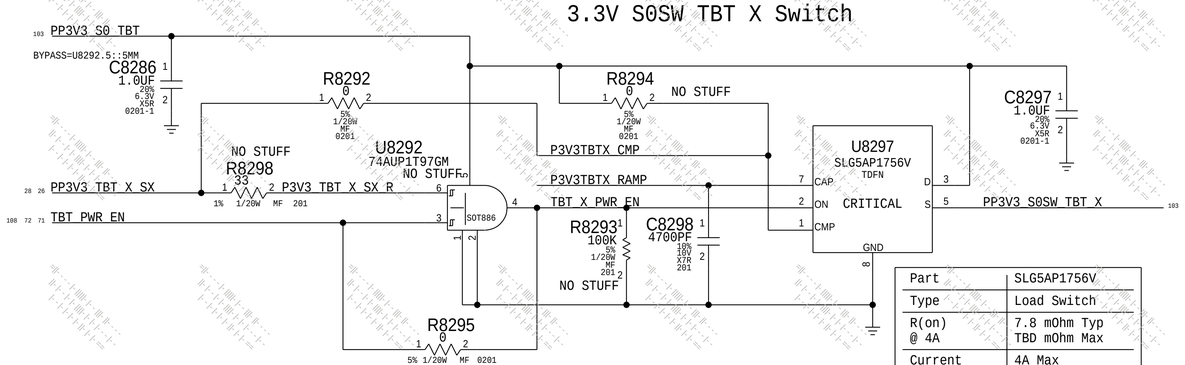
Based off rdar://30356539. 3V3_G3W can be combined into 3V3_G3H.

3.3V ENET Switch



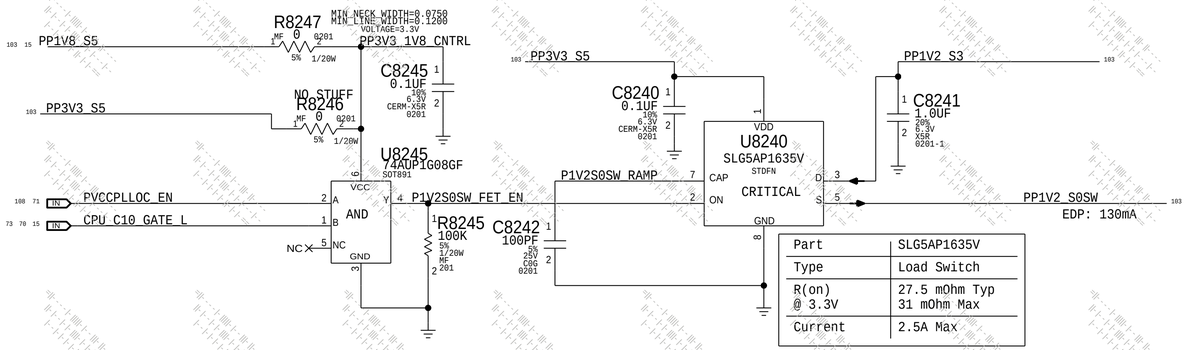
Part	SLG5AP1445V
R(on) @ 3.6V	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

3.3V S0SW TBT X Switch



Part	SLG5AP1756V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

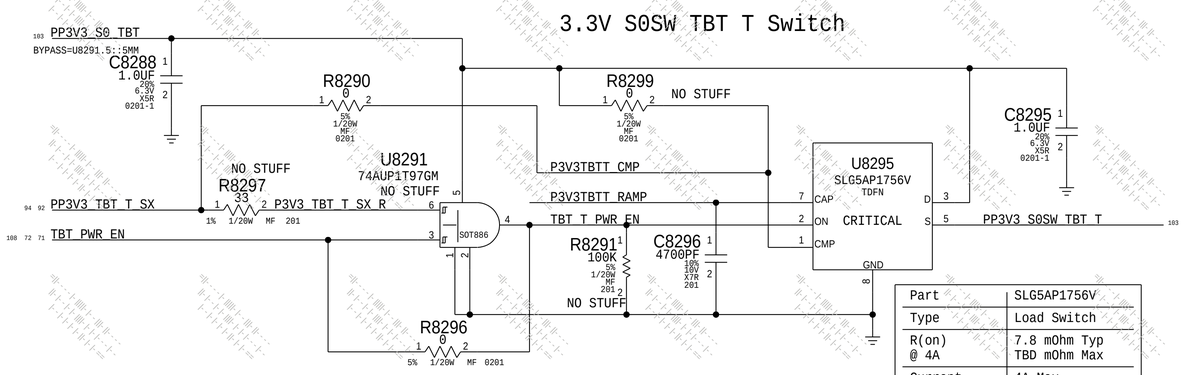
1.2V S0SW VCCPLL_OC Switch



Part	SLG5AP1635V
Type	Load Switch
R(on) @ 3.6V	27.5 mOhm Typ 31 mOhm Max
Current	2.5A Max

VCCPLL_OC has turn-on requirement of 11uS min and 240uS max from EN to 1.1V

3.3V S0SW TBT T Switch



Part	SLG5AP1756V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: 051-02424 | SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 82 OF 142
SHEET: 72 OF 115

VCCIO S0 REGULATOR

EDC = 6.4A

TDC = 6.4A

Fsw = 500KHz

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0358	2	CAP,470uF,0.0060HM,2V,D2	C8340,C8341	VR_BULKCAP:CURRENT
128S0381	2	CAP,470uF,0.00450HM,2.5V,SM	C8340,C8341	VR_BULKCAP:FUTURE

BOM_COST_GROUP=CPU & CHIPSET

DRAWING: LAST_MODIFIED=Thu Jul 12 17:57:13 2018

PAGE TITLE: CPU & CHIPSET: CPU VCCIO VR

Apple Inc.

DRAWING NUMBER: 051-02424

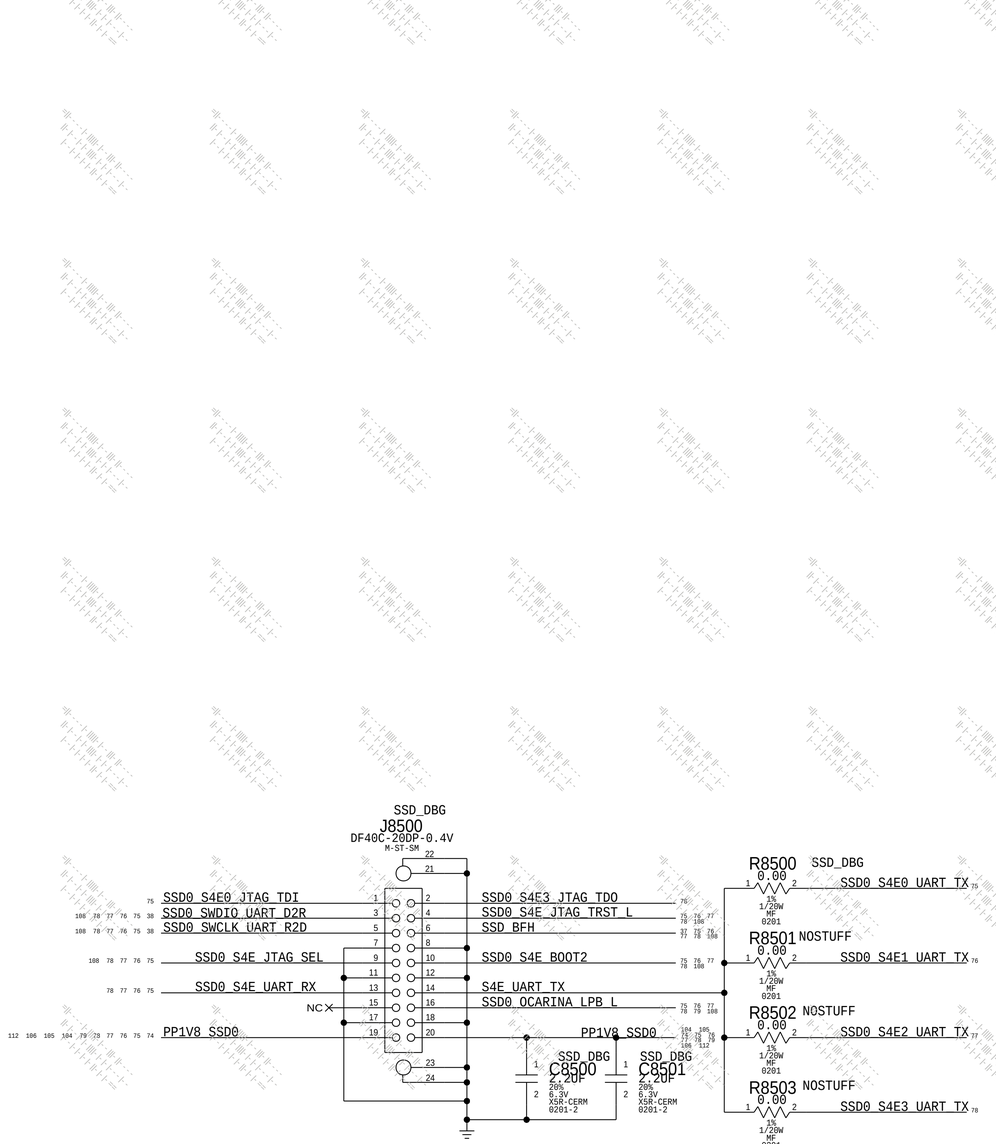
SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 83 OF 142

SHEET: 73 OF 115



BOM_COST_GROUP=DEBUG

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: SSD DEBUG AND SUPPORT

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 85 OF 142

SHEET: 74 OF 115

S4E0

PP1V8_SSD0
C8632 10UF 20% 6.3V CERM-X6S 0402
C8636 4.3UF 20% 4V CERM 0402
C8637 2.2UF 20% 6.3V X5R-CERM 0201
PP2V7_NAND_SSD0
C8648 10UF 20% 6.3V CERM-X6S 0402
C8649 2.2UF 20% 6.3V X5R-CERM 0201
C8650 2.2UF 20% 6.3V X5R-CERM 0201
PP0V9_SSD0
NC_SSD0_S4E0_VPP
U8600 KLADG4UWCA LGA OMIT_TABLE
VPP F3
VDD_PLL R4
VCC B2 L12 G4 E12 D3
VDDIO P9 T5 N2 K9 J2 E10 E2
VDD R8 P6 L6 L8 G8 G6
ANI_VREF J4
ANIO_VREF G12
AVDD18_PLL L2
PCI_VDD_2 J8
PCI_VDD_1 H8
PCI_AVDD_H J6
PCI_AVDD_CLK_2 H3
PCI_AVDD_CLK_1 H6
TP_SSD0_S4E0_ANI1_VREF
TP_SSD0_S4E0_ANI0_VREF
PP1V8_SSD0_S4E0_AVDD18_PLL
PP1V8_SSD0_S4E0_PCI_AVDD_H
PP0V9_SSD0
VOLTAGE=1.8V
VOLTAGE=1.8V
C8610 10UF 20% 6.3V CERM-X6S 0402
C8611 2.2UF 20% 6.3V X5R-CERM 0201
C8612 2.2UF 20% 6.3V X5R-CERM 0201
C8613 0.1UF 10% 16V X5R-CERM 0201
C8614 0.1UF 10% 16V X5R-CERM 0201
C8615 0.1UF 10% 16V X5R-CERM 0201
PP0V9_SSD0
XW8601 SM
PP1V8_SSD0
C8646 1.0UF 20% 10V X5R-CERM 0201-1
C8647 0.1UF 10% 16V X5R-CERM 0201
XW8600 SM
C8644 1.0UF 20% 10V X5R-CERM 0201-1
C8645 0.1UF 10% 16V X5R-CERM 0201
PLACE_NEAR=U8600.M3:3MM
R8640 100 1/20W 1% MF 201
SSD0_CLK24M_01
SSD0_CLK24M
CLK_IN M3
PCIE_REFCLK_P K11 PCIE_CLK100M_SSD0_01_P
PCIE_REFCLK_M J12 PCIE_CLK100M_SSD0_01_N
PCIE_CLKREQ_N P5 SSD0_CLKREQ0_L
PCI_RESREF H7 SSD0_S4E0_PCIE_RESREF
PCIE_RX0_P M11
PCIE_RX0_M N12
PCIE_SSD0_R2D_P<0>
PCIE_SSD0_R2D_N<0>
PCIE_TX0_P R12
PCIE_TX0_M T11
PCIE_SSD0_D2R_C_P<0>
PCIE_SSD0_D2R_C_N<0>
C8603 0.22UF 20% 10V X5R-CERM 0201
C8604 0.22UF 20% 10V X5R-CERM 0201
C8601 0.22UF 20% 10V X5R-CERM 0201
C8602 0.22UF 20% 10V X5R-CERM 0201
PCIE_SSD0_R2D_C_P<0>
PCIE_SSD0_R2D_C_N<0>
PCIE_SSD0_D2R_P<0>
PCIE_SSD0_D2R_N<0>
GND_VOID=TRUE
R8604 3.01K 1% 1/20W MF 201
RESET* L4 SSD0_OCARINA_RESET_L
TRST* G10 SSD0_S4E_JTAG_TRST_L
ZQ_C K3 SSD0_S4E0_ZQ_C
ZQ_N C10 SSD0_S4E0_ZQ_L
PLACE_NEAR=U8600.C10:2mm
R8605 300 1% 1/20W MF 201
R8606 100 1% 1/20W MF 201
R8600 100K 1% 1/20W MF 201
BOM_COST_GROUP=SSD

SSD0_OCARINA_LPB_L B3 EXT_D0/BOOT0
SSD_BFH C4 EXT_D1/BOOT1
SSD0_S4E_BOOT2 B5 EXT_D2/BOOT2/SPINAND_SCLK
SSD0_S4E0_SWD_UID0 C6 EXT_D3/SWD_UID0/SPINAND_MISO
SSD0_S4E_UART_RX B7 EXT_D4/UART_RX
SSD0_S4E0_SWD_UID1 C8 EXT_D5/SWD_UID1/SPINAND_MOSI
SSD0_S4E0_UART_TX B9 EXT_D6/UART_TX
SSD0_OCARINA_PFN B11 EXT_D7/SPF
SSD0_PCIE_RESET_L E8 EXT_NCE/PERST*
SSD0_SWDIO_UART_D2R D7 EXT_NRE/JTAG_TMS
SSD0_SWCLK_UART_R2D E6 EXT_NWE/JTAG_TCK
SSD0_S4E0_JTAG_TDO E4 EXT_RNB/JTAG_TDO
TPA8601 SSD0_S4E0_JTAG_TDI D5 EXT_CLE/JTAG_TDI
SSD0_S4E_JTAG_SEL D9 EXT_ALE/JTAG_SEL
SSD0_S4E0_DROOP_L T3 DROOP_N
SSD0_OCARINA_WP_L G2 WP_N
VSS

PP1V8_SSD0
R8602 4.7K 1% 1/20W MF 201
NOSTUFF
R8603 4.7K 1% 1/20W MF 201
SSD0_OCARINA_PFN
SSD0_S4E0_DROOP_L

SSD0_S4E_BOOT2
SSD0_S4E0_SWD_UID0
SSD0_S4E0_SWD_UID1
R8620 100K 1% 1/20W MF 201
R8608 100K 1% 1/20W MF 201
R8609 100K 1% 1/20W MF 201

SYNC_MASTER=Marv
SYNC_DATE=04/26/2018
PAGE TITLE
SSD0 S4E 0
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 86 OF 142
SHEET 75 OF 115

S4E1

U8700

KLADG4UWCA

LGA

OMIT_TABLE

SSD0_OCARINA_LPB_L	B3	EXT_D0/BOOT0
SSD_BFH	C4	EXT_D1/BOOT1
SSD0_S4E_BOOT2	B5	EXT_D2/BOOT2/SPINAND_SCLK
SSD0_S4E1_SWD_UID0	C6	EXT_D3/SWD_UID0/SPINAND_MISO
SSD0_S4E_UART_RX	B7	EXT_D4/UART_RX
SSD0_S4E1_SWD_UID1	C8	EXT_D5/SWD_UID1/SPINAND_MOSI
SSD0_S4E1_UART_TX	B9	EXT_D6/UART_TX
SSD0_OCARINA_PFN	B11	EXT_D7/SPF
SSD0_PCIE_RESET_L	E8	EXT_NCE/PERST*
SSD0_SWDIO_UART_D2R	D7	EXT_NRE/JTAG_TMS
SSD0_SWCLK_UART_R2D	E6	EXT_NWE/JTAG_TCK
SSD0_S4E1_JTAG_TDO	E4	EXT_RNB/JTAG_TDO
SSD0_S4E0_JTAG_TDO	D5	EXT_CLE/JTAG_TDI
SSD0_S4E_JTAG_SEL	D9	EXT_ALE/JTAG_SEL
SSD0_S4E1_DROOP_L	T3	DROOP_N
SSD0_OCARINA_WP_L	G2	WP_N

PP1V8_SSD0, PP0V9_SSD0, PP2V7_NAND_SSD0, PP0V9_SSD0, NC_SSD0_S4E1_VPP

VPP F3, VDD_PLL R4, VCC R2 L12 C4 E12 D9, VDDIO P9 T5 N2 K9 J2 E10 E2, VDD R8 R6 L9 L6 G8 G6, ANI_VREF J4, ANO_VREF G12, AVDD18_PLL L2, PCI_VDD_2 J8, PCI_VDD_1 H8, PCI_AVDD_H J6, PCI_AVDD_CLK_2 M9, PCI_AVDD_CLK_1 M6

TP_SSD0_S4E1_ANI1_VREF, TP_SSD0_S4E1_ANI0_VREF, PP1V8_SSD0_S4E1_AVDD18_PLL, PP1V8_SSD0_S4E1_PCI_AVDD_H, PP0V9_SSD0

VSS: U12 U10 U8 U6 U4 U2 T13 T9 T7 T1 R10 R13 P11 P7 P3 P1 N10 N4 M13 M7 M5 M1 L10 K13 K7 K5 K1 J10 H13 H11 H9 H5 H3 H1 F13 F11 F9 F7 F5 F1 D13 D11 D1 C12 C2 B13 B1 A12 A10 A8 A6 A4 A2

CLK_IN M3 SSD0_CLK24M_01

PCIE_REFCLK_P K11 PCIE_CLK100M_SSD0_01_P

PCIE_REFCLK_M J12 PCIE_CLK100M_SSD0_01_N

PCIE_CLKREQ_N P5 SSD0_CLKREQ1_L

PCI_RESREF H7 SSD0_S4E1_PCIE_RESREF

PCIE_RX0_P M11 PCIE_SSD0_R2D_P<1>

PCIE_RX0_M N11 PCIE_SSD0_R2D_N<1>

PCIE_TX0_P R12

PCIE_TX0_M T11

RESET* L4 SSD0_OCARINA_RESET_L

TRST* G10 SSD0_S4E_JTAG_TRST_L

ZQ_C K3 SSD0_S4E1_ZQ_C

ZQ_N C10 SSD0_S4E1_ZQ_L

R8704 3.01K 1% 1/20W MF 201

C8703 0.22UF 6.3V 10% 0201 X5R-CERM

C8704 0.22UF 6.3V 10% 0201 X5R-CERM

C8701 0.22UF 6.3V 10% 0201 X5R-CERM

C8702 0.22UF 6.3V 10% 0201 X5R-CERM

PCIE_SSD0_R2D_C_P<1>, PCIE_SSD0_R2D_C_N<1>, PCIE_SSD0_D2R_C_P<1>, PCIE_SSD0_D2R_C_N<1>, PCIE_SSD0_D2R_P<1>, PCIE_SSD0_D2R_N<1>

R8705 300 1% 1/20W MF 201

R8706 100 1% 1/20W MF 201

R8702 47K 1% 1/20W MF 201

R8708 100K 1% 1/20W MF 201

SSD0_S4E1_SWD_UID0, SSD0_S4E1_DROOP_L, SSD0_S4E1_SWD_UID1

R8709 100K 1% 1/20W MF 201

S4E VDD

PP0V9_SSD0

C8710 100UF 20% 6.3V CERM-X6S 0402

C8711 2.2UF 20% 6.3V X5R-CERM 0201

C8712 2.2UF 20% 6.3V X5R-CERM 0201

C8713 0.1UF 10% 6.3V X5R-CERM 0201

C8714 0.1UF 10% 6.3V X5R-CERM 0201

C8715 0.1UF 10% 6.3V X5R-CERM 0201

S4E VDDIO

PP1V8_SSD0

C8732 10UF 20% 6.3V CERM-X6S 0402

C8736 4.3UF 20% 4V CERM 0402

C8737 2.2UF 20% 6.3V X5R-CERM 0201

XW8700 SM

PP1V8_SSD0_S4E1_PCI_AVDD_H VOLTAGE=1.8V

C8744 1.0UF 20% 6.3V X5R-CERM 0201-1

C8745 0.1UF 10% 6.3V X5R-CERM 0201

XW8701 SM

PP1V8_SSD0_S4E1_AVDD18_PLL VOLTAGE=1.8V

C8746 1.0UF 20% 6.3V X5R-CERM 0201-1

C8747 0.1UF 10% 6.3V X5R-CERM 0201

VCC CAP

PP2V7_NAND_SSD0

C8748 10UF 20% 6.3V CERM-X6S 0402

C8749 2.2UF 20% 6.3V X5R-CERM 0201

C8750 2.2UF 20% 6.3V X5R-CERM 0201

BOM_COST_GROUP=SSD

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: SSD0 S4E 1

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

BRANCH dvt-1

PAGE 87 OF 142

SHEET 76 OF 115

S4E2

U8800
KLADG4UWCA
LGA
OMIT_TABLE

PP1V8_SSD0
PP0V9_SSD0
PP2V7_NAND_SSD0
PP0V9_SSD0
NC_SSD0_S4E2_VPP
TP_SSD0_S4E2_ANI1_VREF
TP_SSD0_S4E2_ANI0_VREF
PP1V8_SSD0_S4E2_AVDD18_PLL
PP1V8_SSD0_S4E2_PCI_AVDD_H
PP0V9_SSD0

VPP VDD_PLL VCC VDDIO VDD ANI1_VREF ANI0_VREF AVDD18_PLL PCI_VDD_2 PCI_VDD_1 PCI_AVDD_H PCI_AVDD_CLK_2 PCI_AVDD_CLK_1

VSS

SSD0_OCARINA_LPB_L	B3	EXT_D0/BOOT0
SSD_BFH	C4	EXT_D1/BOOT1
SSD0_S4E_BOOT2	B5	EXT_D2/BOOT2/SPINAND_SCLK
SSD0_S4E2_SWD_UID0	C6	EXT_D3/SWD_UID0/SPINAND_MISO
SSD0_S4E_UART_RX	B7	EXT_D4/UART_RX
SSD0_S4E2_SWD_UID1	C5	EXT_D5/SWD_UID1/SPINAND_MOSI
SSD0_S4E2_UART_TX	B9	EXT_D6/UART_TX
SSD0_OCARINA_PFN	B11	EXT_D7/SPF
SSD0_PCIE_RESET_L	E8	EXT_NCE/PERST*
SSD0_SWDIO_UART_D2R	D7	EXT_NRE/JTAG_TMS
SSD0_SWCLK_UART_R2D	E6	EXT_NWE/JTAG_TCK
SSD0_S4E2_JTAG_TDO	E4	EXT_RNB/JTAG_TDO
SSD0_S4E1_JTAG_TDO	D5	EXT_CLE/JTAG_TDI
SSD0_S4E_JTAG_SEL	D9	EXT_ALE/JTAG_SEL
SSD0_S4E2_DROOP_L	T3	DROOP_N
SSD0_OCARINA_WP_L	G2	WP_N

CLK_IN	M3	SSD0_CLK24M_23
PCIE_REFCLK_P	K11	PCIE_CLK100M_SSD0_23_P
PCIE_REFCLK_M	J12	PCIE_CLK100M_SSD0_23_N
PCIE_CLKREQ_N	P5	SSD0_CLKREQ2_L
PCI_RESREF	H7	SSD0_S4E2_PCIE_RESREF
PCIE_RX0_P	M11	PCIE_SSD0_R2D_P<2>
PCIE_RX0_M	N12	PCIE_SSD0_R2D_N<2>
PCIE_TX0_P	R12	PCIE_SSD0_D2R_C_P<2>
PCIE_TX0_M	T11	PCIE_SSD0_D2R_C_N<2>
RESET*	L4	SSD0_OCARINA_RESET_L
TRST*	G10	SSD0_S4E_JTAG_TRST_L
ZQ_G	K3	SSD0_S4E2_ZQ_C
ZQ_N	C10	SSD0_S4E2_ZQ_L

PLACE_NEAR=U8800.M3:3MM
R8840 100 1% 1/20W MF 201
SSD0_CLK24M
R8804 3.01K 1% 1/20W MF 201
C8803 0.22UF 10% 6.3V X5R-CERM 0201
C8804 0.22UF 10% 6.3V X5R-CERM 0201
C8801 0.22UF 10% 6.3V X5R-CERM 0201
C8802 0.22UF 10% 6.3V X5R-CERM 0201
PCIE_SSD0_R2D_C_P<2>
PCIE_SSD0_R2D_C_N<2>
PCIE_SSD0_D2R_P<2>
PCIE_SSD0_D2R_N<2>

R8802 47K 1% 1/20W MF 201
R8809 100K 1% 1/20W MF 201
R8808 100K 1% 1/20W MF 201
SSD0_S4E2_SWD_UID1
SSD0_S4E2_DROOP_L
SSD0_S4E2_SWD_UID0

R8805 300 1% 1/20W MF 201
R8806 100 1% 1/20W MF 201

S4E VDD

PP0V9_SSD0
C8810 10UF 20% 6.3V CERM-X6S 0402
C8811 2.2UF 20% 6.3V X5R-CERM 0201
C8812 2.2UF 20% 6.3V X5R-CERM 0201
C8813 0.1UF 10% 10V X5R-CERM 0201
C8814 0.1UF 10% 10V X5R-CERM 0201
C8815 0.1UF 10% 10V X5R-CERM 0201

S4E VDDIO

PP1V8_SSD0
C8832 10UF 20% 6.3V CERM-X6S 0402
C8836 4.3UF 20% 4V CERM 0402
C8837 2.2UF 20% 6.3V X5R-CERM 0201

XW8800 SM
PP1V8_SSD0_S4E2_PCI_AVDD_H VOLTAGE=1.8V
C8844 1.0UF 20% 10V X5R-CERM 0201-1
C8845 0.1UF 10% 10V X5R-CERM 0201

XW8801 SM
PP1V8_SSD0_S4E2_AVDD18_PLL VOLTAGE=1.8V
C8846 1.0UF 20% 10V X5R-CERM 0201-1
C8847 0.1UF 10% 10V X5R-CERM 0201

VCC CAP

PP2V7_NAND_SSD0
C8848 10UF 20% 6.3V CERM-X6S 0402
C8849 2.2UF 20% 6.3V X5R-CERM 0201
C8850 2.2UF 20% 6.3V X5R-CERM 0201

BOM_COST_GROUP=SSD

SYNC_MASTER=Mary SYNC_DATE=04/26/2018
PAGE TITLE: SSD0 S4E 2

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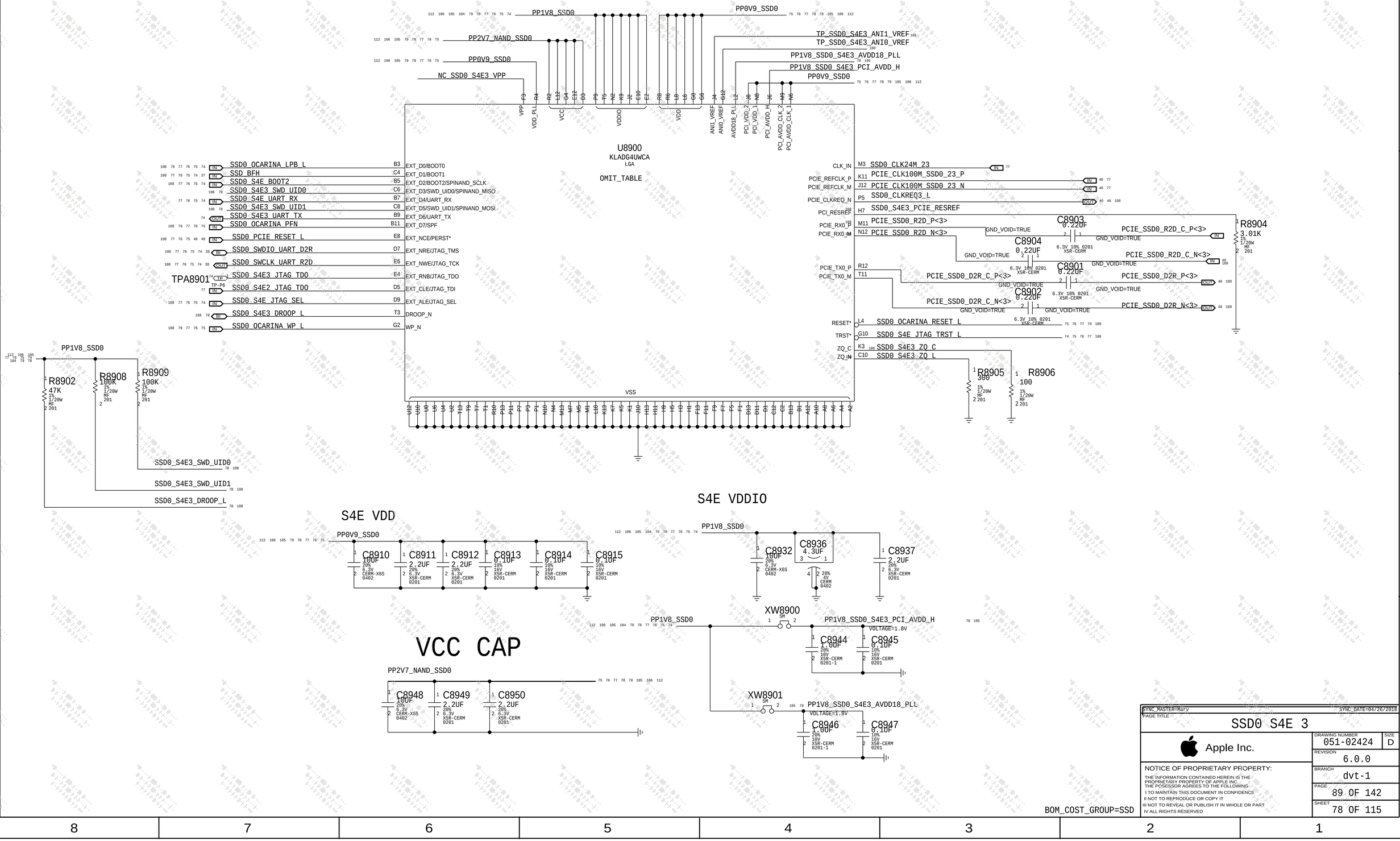
DRAWING NUMBER 051-02424 | SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 88 OF 142
SHEET 77 OF 115

S4E3



BOM_COST_GROUP=SSD

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: SSD0 S4E 3

Apple Inc.

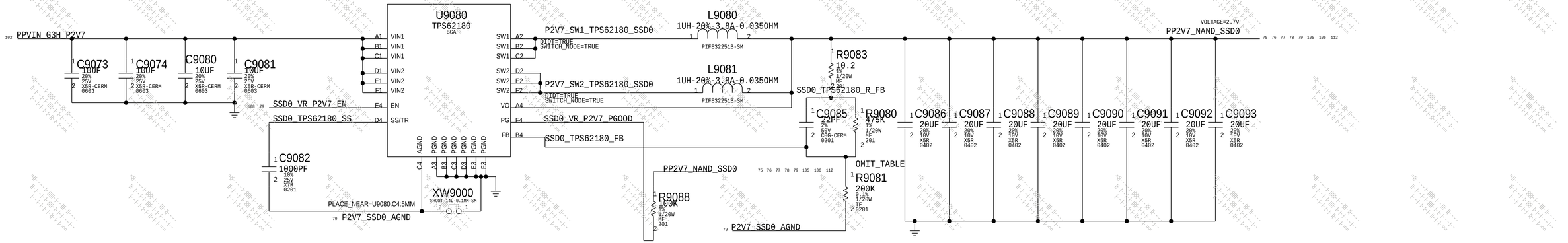
DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

BRANCH dvt-1

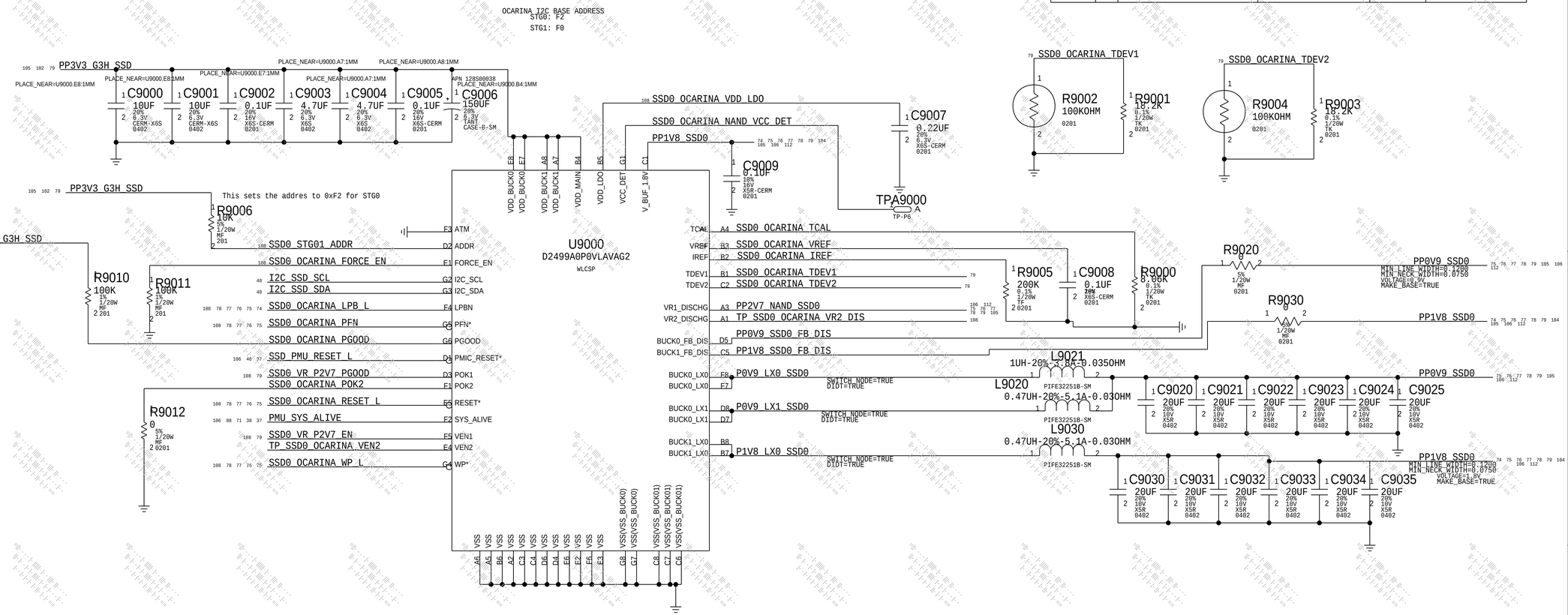
PAGE 89 OF 142

SHEET 78 OF 115



R2081:200K->2.7V, 221K->2.519V NAND VCC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0738	1	RES,THICKFILM,200KOHM,0.1%,1/20W,[illegible]	R9081	CRITICAL	SSD0_NAND_VCC:2.7V
103S00049	1	RES,THICKFILM,221KOHM,0.1%,1/20W,[illegible]	R9081	CRITICAL	SSD0_NAND_VCC:2.5V



SYNC_MASTER=Mary	SYNC_DATE=04/26/2018
PAGE TITLE	SSD0 PMIC & VR
Apple Inc.	DRAWING NUMBER 051-02424 · SIZE D
	REVISION 6.0.0
	BRANCH dvt-1
	PAGE 90 OF 142
	SHEET 79 OF 115

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BOM_COST_GROUP=SSD

BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
PP3V3R1V8_ENET_LR_OUT

ENET_SR_LX
PP1V2_ENET_INTREG
Internal 1.2V Switching Regulator pins.

PP1V2_ENET_INTREG
396mA (1000base-T, Caesar II)

ENET:1G CRITICAL L9300 FERR-600-OHM-300MA-0.85OHM 0402
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C9300 0.1UF 10% 16V X5R-CERM 0201 ENET:1G

ENET_XTALVDDH
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V

ENET:1G CRITICAL L9305 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C9305 0.1UF 10% 16V X5R-CERM 0201 ENET:1G

ENET:1G CRITICAL L9310 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
R9310 4.7K 5% 1/16W MF-LF 402 ENET:1G
C9310 0.1UF 10% 16V X5R-CERM 0201 ENET:1G
C9311 0.1UF 10% 16V X5R-CERM 0201 ENET:1G

ENET:1G R9340 4.7K 5% 1/16W MF-LF 402
ENET:1G R9341 4.7K 5% 1/16W MF-LF 402
PM_SLP_S3_L
ENET:1G R9342 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

ENET:1G C9315 4.7UF 20% 6.3V X5R-CERM 402
ENET:1G C9316 0.1UF 10% 16V X5R-CERM 0201

AVDDH BIASVDDH XTALVDDH VDDC SR_VDD SR_VDDP SR_LX SR_VFB AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC

PP1V2_ENET_PHY_AVDDL
ENET:1G L9320 FERR-600-OHM-300MA-0.85OHM 0402
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
ENET:1G C9321 0.1UF 10% 16V X5R-CERM 0201
C9320 4.7UF 20% 6.3V X5R-CERM1 402 ENET:1G

PP1V2_ENET_PHY_PCIEPLL
ENET:1G L9325 FERR-600-OHM-0.5A SM
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
ENET:1G C9326 0.1UF 10% 16V X5R-CERM 0201
C9325 4.7UF 20% 6.3V X5R-CERM1 402 ENET:1G

PP1V2_ENET_PHY_GPHYPLL
ENET:1G L9330 FERR-600-OHM-300MA-0.85OHM 0402
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 VOLTAGE=1.2V
ENET:1G C9331 0.1UF 10% 16V X5R-CERM 0201
C9330 4.7UF 20% 6.3V X5R-CERM1 402 ENET:1G

ENET:1G C9336 0.1UF 10% 16V X5R-CERM 0201
ENET:1G C9335 10UF 20% 6.3V X5R 603

QMIT_TABLE
U9300
BCM57766A1KMLG
QFN-8X8
CAESAR IV

ENET_VMAIN_PRSNT → 58 VMAIN_PRSNT (IPD-ENET)
PCIE_ENET_1G_D2R_C_N → 27 PCIE_TXD_N
PCIE_ENET_1G_D2R_C_P → 28 PCIE_TXD_P
PCIE_ENET_1G_R2D_P → 33 PCIE_RXD_P
PCIE_ENET_1G_R2D_N → 34 PCIE_RXD_N
PCIE_CLK100M_ENET_1G_P → 31 PCIE_REFCLK_P
PCIE_CLK100M_ENET_1G_N → 30 PCIE_REFCLK_N
ENET_RESET_3V3_L → 11 PERST* (IPD)
ENET_CLKREQ_3V3_L ↔ 12 CLKREQ* (OD)
PCIEDN_WAKE_ENET_L ← 3 WAKE* (OD)
ENET_1G_LOW_PWR → 4 LOW_PWR (IPD)
SMB_ENET_SCL ↔ 6 SMB_CLK
SMB_ENET_SDA ↔ 10 SMB_DATA (IPD-ENETM)
ENET_1G_SCLK → 66 SCLK_SPD1000LED*
ENET_1G_MISO ← 64 SI/EEDATA
ENET_1G_MOSI → 65 SO_LINKLED*
ENET_1G_CS_L → 63 CS*/EECLK
TP_ENET_1G_SERIAL_DO → 2 SPD100LED*/SERIAL_DO (OD)
ENET_TRAFFICLED_L → 67 TRAFFICLED*/SERIAL_DI (OD)
ENET_XTAL_IN → 18 XTALI
ENET_XTAL_OUT ← 19 XTALO
ENET_RDAC ↔ 38 RDAC
THRM_PAD 69

TRD0_P 40 ↔ ENETCONN_MDI_P<0>
TRD0_N 41 ↔ ENETCONN_MDI_N<0>
TRD1_P 44 ↔ ENETCONN_MDI_P<1>
TRD1_N 43 ↔ ENETCONN_MDI_N<1>
TRD2_P 46 ↔ ENETCONN_MDI_P<2>
TRD2_N 47 ↔ ENETCONN_MDI_N<2>
TRD3_P 50 ↔ ENETCONN_MDI_P<3>
TRD3_N 49 ↔ ENETCONN_MDI_N<3>

GPIO_0/CR_ACT_LED* (IPD) 5 NC
GPIO_1/LR_OUT 8
GPIO_2/MEDIA_SENSE 9 → ENET_1G_MEDIA_SENSE OUT 84

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT (IPx-ENET) 0 1 NC
SD_DETECT can only be used active low due to errata.
CR_CMD (IPU-ENET) 26 NC
CR_CLK 21 NC
CR_DATA0 25 NC
CR_DATA1 24 NC
CR_DATA2 23 NC
CR_DATA3 22 NC
CR_DATA4 52 NC
CR_DATA5 53 NC
CR_DATA6 54 NC
CR_DATA7 55 NC
(IPU-ENET)
MS_INS* (IPU-ENET) 59 NC
CR_LED*/CR_BUS_PWR (IPU-ENET) 60 NC
CR_WP* (IPU-ENET) 57 NC
SR_DISABLE (NO IPU OR IPD-ENET) 68

CONTROL SIGNAL TO LIGHT LED OR CONTROL SD BUS POWER.

ENET_SR_DISABLE (See note)
R9381 1K 5% 1/16W MF-LF 402 ENET:1G
ENET supports both active-levels for WP.

ENET 1.2V SR IS ENABLED IF FLOATING.

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

PP3V3R1V8_ENET_LR_OUT
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V MAKE_BASE=TRUE
ENET:1G C9380 4.7UF 20% 6.3V X5R-CERM1 402
ENET:1G C9381 0.1UF 10% 16V X5R-CERM 0201
ENET:1G C9382 0.1UF 10% 16V X5R-CERM 0201
PP3V3R1V8_ENET_LR_OUT 80

ENET:1G MEDIA_SENSE

PCIEDN_WAKE_ENET_L ← 84 (See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L TO PCIEDN_WAKE_L.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

PP3V3_ENET
ENET:1G C9390 0.1UF 10% 16V X5R-CERM 0201
U9390 AT45DB011D SOIC-8S1 OMIT_TABLE
VCC SCK CS* WP* RESET* SI SO GND
ENET_1G_SCLK ENET_1G_CS_L ENET_1G_MOSI ENET_1G_MISO
NOSTUFF R9390 4.7K 5% 1/16W MF-LF 402
ENET:1G R9397 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

ENET:1G C9340 15PF 2% 50V C0G-CERM 0402
ENET_XTAL_OUT_R
ENET:1G CRITICAL Y9340 25.000MHZ-20PPM-12PF-85C 3.2X2.5MM-SM
ENET:1G C9341 15PF 2% 50V C0G-CERM 0402
NOTE: 30 PPM crystal required
ENET:1G R9343 0 5% 1/16W MF-LF 402
ENET_XTAL_OUT
NOSTUFF R9344 1M 5% 1/16W MF-LF 402
ENET_XTAL_IN

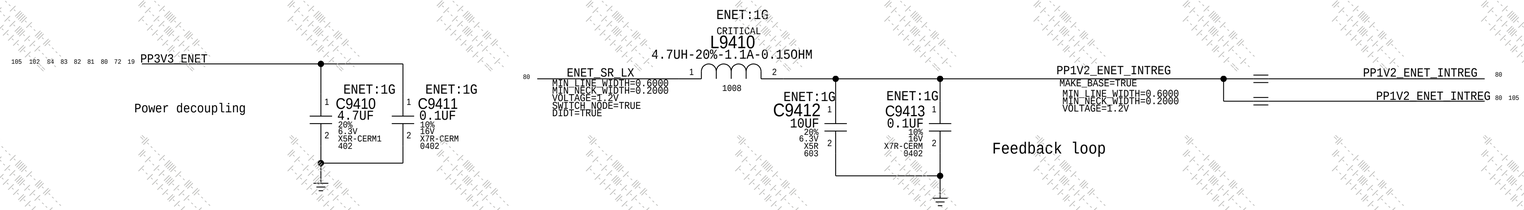
ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE
If ENET switching regulator is used, this pin should have a 1K pull-down to GND

BOM_COST_GROUP=ETHERNET

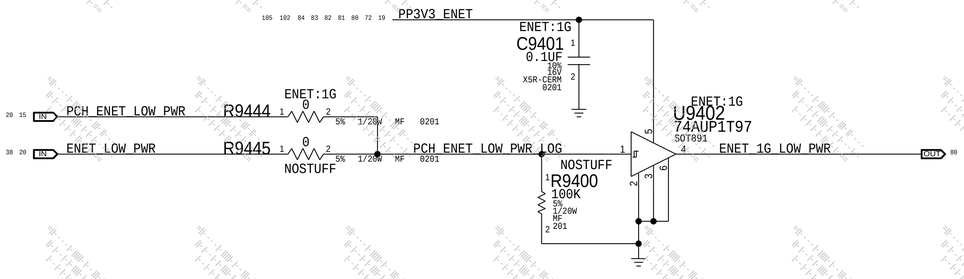
SYNC_MASTER=Mary SYNC_DATE=04/26/2018
PAGE TITLE: 1G ENET PHY (Caesar IV)
Apple Inc.
DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 93 OF 142
SHEET 80 OF 115

CAESAR IV 1.2V INT.VR CMPTS

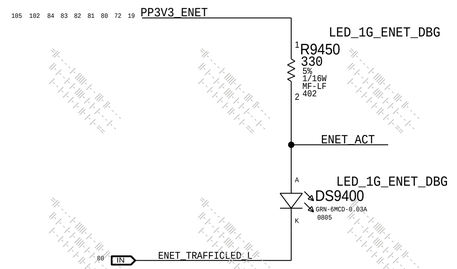


Misc Alias

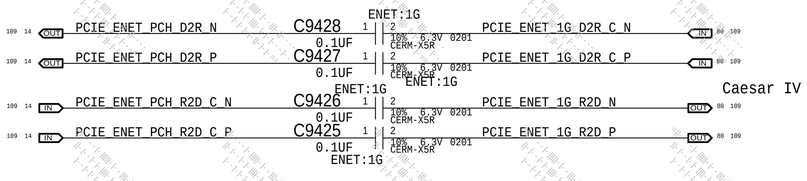
1G ENET LOW PWR



1G ETHERNET ACTIVITY LED



PCIE Connection



BOM_COST_GROUP=ETHERNET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: 1G ENET SUPPORT

Apple Inc.

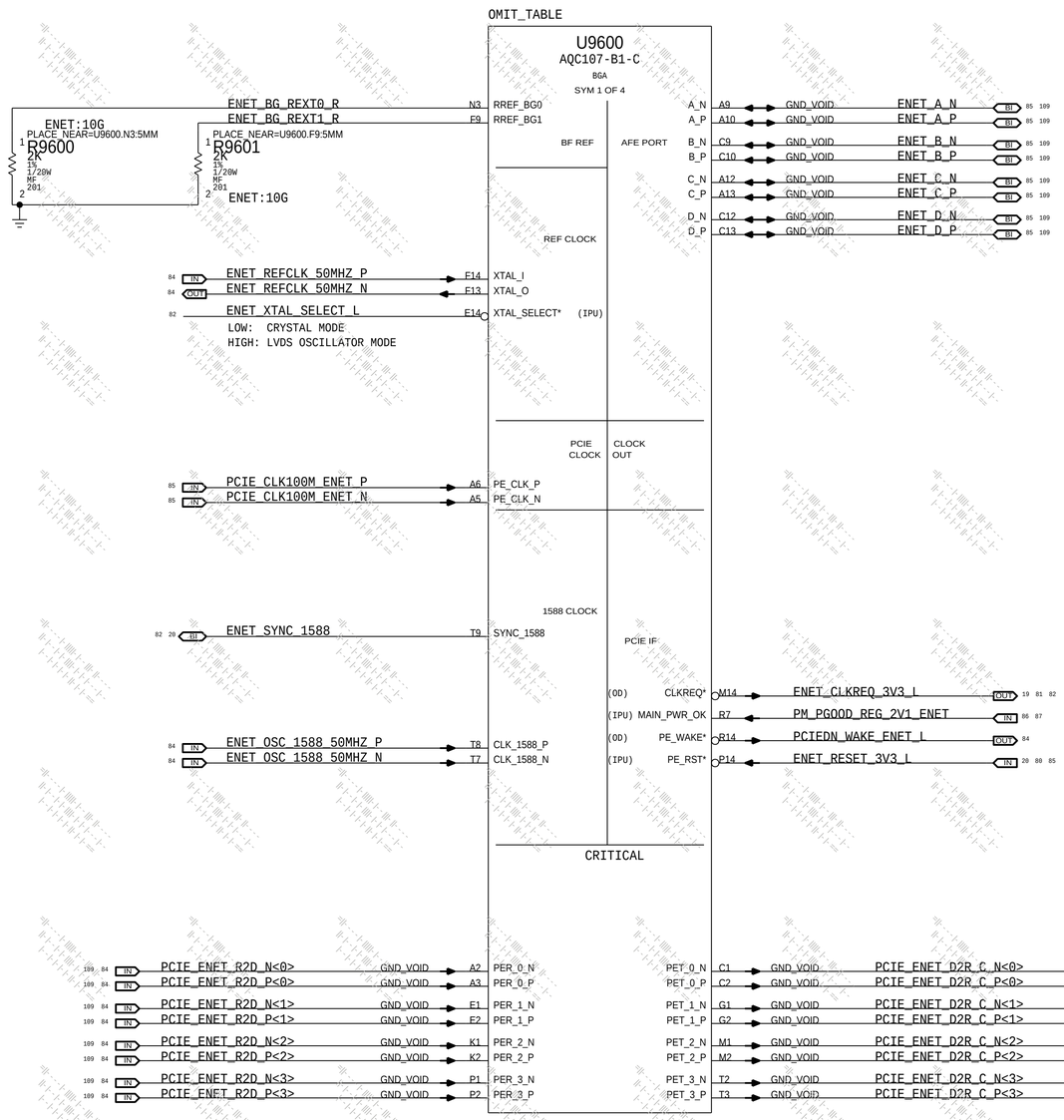
DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 94 OF 142

SHEET: 81 OF 115


OMIT_TABLE
U9600
AQC107-B1-C
BGA
SYM 1 OF 4
ENET:10G
PLACE_NEAR=U9600.N3:5MM
R9600
2K
1%
1/20W
MF
201
ENET:10G
PLACE_NEAR=U9600.F9:5MM
R9601
2K
1%
1/20W
MF
201
ENET:10G
ENET_BG_REXT0_R
ENET_BG_REXT1_R
N3 RREF_BG0
F9 RREF_BG1
BF REF
AFE PORT
A_N A9 GND_VOID ENET_A_N
A_P A10 GND_VOID ENET_A_P
B_N C9 GND_VOID ENET_B_N
B_P C10 GND_VOID ENET_B_P
C_N A12 GND_VOID ENET_C_N
C_P A13 GND_VOID ENET_C_P
D_N C12 GND_VOID ENET_D_N
D_P C13 GND_VOID ENET_D_P
REF CLOCK
ENET_REFCLK_50MHZ_P F14 XTAL_I
ENET_REFCLK_50MHZ_N F13 XTAL_O
ENET_XTAL_SELECT_L E14 XTAL_SELECT* (IPU)
LOW: CRYSTAL MODE
HIGH: LVDS OSCILLATOR MODE
PCIE CLOCK
CLOCK OUT
PCIE_CLK100M_ENET_P A6 PE_CLK_P
PCIE_CLK100M_ENET_N A5 PE_CLK_N
1588 CLOCK
ENET_SYNC_1588 T9 SYNC_1588
PCIE IF
ENET_OSC_1588_50MHZ_P T8 CLK_1588_P
ENET_OSC_1588_50MHZ_N T7 CLK_1588_N
(OD) CLKREQ* M14 ENET_CLKREQ_3V3_L
(IPU) MAIN_PWR_OK R7 PM_PGOOD_REG_2V1_ENET
(OD) PE_WAKE* R14 PCIEDN_WAKE_ENET_L
(IPU) PE_RST* P14 ENET_RESET_3V3_L
CRITICAL
PCIE_ENET_R2D_N<0> A2 PER_0_N
PCIE_ENET_R2D_P<0> A3 PER_0_P
PCIE_ENET_R2D_N<1> E1 PER_1_N
PCIE_ENET_R2D_P<1> E2 PER_1_P
PCIE_ENET_R2D_N<2> K1 PER_2_N
PCIE_ENET_R2D_P<2> K2 PER_2_P
PCIE_ENET_R2D_N<3> P1 PER_3_N
PCIE_ENET_R2D_P<3> P2 PER_3_P
PET_0_N C1 GND_VOID PCIE_ENET_D2R_C_N<0>
PET_0_P C2 GND_VOID PCIE_ENET_D2R_C_P<0>
PET_1_N G1 GND_VOID PCIE_ENET_D2R_C_N<1>
PET_1_P G2 GND_VOID PCIE_ENET_D2R_C_P<1>
PET_2_N M1 GND_VOID PCIE_ENET_D2R_C_N<2>
PET_2_P M2 GND_VOID PCIE_ENET_D2R_C_P<2>
PET_3_N T2 GND_VOID PCIE_ENET_D2R_C_N<3>
PET_3_P T3 GND_VOID PCIE_ENET_D2R_C_P<3>
OMIT_TABLE
U9600
AQC107-B1-C
BGA
SYM 2 OF 4
SLAVE SMBUS USED FOR DEBUG PORT
INTO PHY MDIO REGISTER SPACE
ENET_SLAVE_SMB_CLK T13 SLAVE_SMB_CLK
ENET_SLAVE_SMB_DAT T12 SLAVE_SMB_DAT
ENET_SMB_ALERT_L R9 SMB_ALERT*
CRITICAL
GPIO 0: CONTROL CIRCUIT FOR
ENABLING VAUX FOR WOL MODE
GPIO 1: ENABLE VOLTAGE LEVEL FOR
EFUSE PROGRAMMING
GPIO 2: WILL BE A CABLE PRESENT SIGNAL
IN UPDATED FIRMWARE
GPIO0 H13 TP_ENET_GPIO0_VAUX_EN
GPIO1 J13 ENET_GPIO1_EFUSE_EN
GPIO2 K13 ENET_MEDIA_SENSE_3V3
ENET:10G
R9625
0
5%
1/20W
MF
0201
ENET:10G
ENET_SMB_CLK
ENET_SMB_DAT
ENET_SMB_CLK_R
ENET_SMB_DAT_R
R9626
0
5%
1/20W
MF
0201
ENET:10G
T10 SMB_CLK
T11 SMB_DAT
LED 0: GREEN, ON WHEN LINK ESTABLISHED
BLINKING WHEN THERE IS ACTIVITY
LED 1: YELLOW, ON FOR 5G/2.5G/1G/100M LINK
LED 2: GREEN, ON FOR 10G LINK
LED_A0 H14 ENET_LED_A0
LED_A1 J14 ENET_LED_A1
LED_A2 K14 ENET_LED_A2
ENET_RG_K12
ENET:10G
R9622
4.99K
1%
1/20W
MF
201
K12 RG_K12
ENET:10G PLACE_NEAR=U9600.R5:10MM
ENET_10G_CS_L
R9643 0
ENET:10G PLACE_NEAR=U9600.T6:10MM
ENET_10G_SCLK
R9641 0
ENET:10G PLACE_NEAR=U9600.R6:10MM
ENET_10G_MOSI
R9642 0
ENET_10G_CS_R_L
ENET_10G_SCLK_R
ENET_10G_MOSI_R
ENET_10G_MISO
R5 CE*
T6 SCLK
R6 SOUT
T5 SIN
SDO0 R12 ENET_MEDIA_SENSE_SDO0_3V3
SDO1 R13 ENET_SDO1
TP9600
TP-P5
PP3V3_ENET
ENET:10G
R9640
4.99K
1%
1/20W
MF
201
PP3V3_ENET IS
AVAILABLE IN STANDBY
ENET_AUX_PWR
ENET:10G
C9640
0.1UF
10%
25V
X6S-CERM
0201
R8 AUX_PWR
PP1V5_LDO_ENET_EFUSE
M11 EFUSE_VDDQ
ENET_JTAG_TCK L14 TCK
ENET_JTAG_TDI P5 TDI
ENET_JTAG_TDO M13 TDO
ENET_JTAG_TMS L13 TMS
ENET_JTAG_TRST_L N13 TRST*
PULL UPS
PP3V3_ENET
R9689 4.99K ENET_CLKREQ_3V3_L
R9690 4.99K ENET:10G ENET_SMB_CLK
R9691 4.99K ENET:10G ENET_SMB_DAT
R9692 4.99K NOSTUFF ENET_SLAVE_SMB_CLK
R9693 4.99K NOSTUFF ENET_SLAVE_SMB_DAT
R9694 1K NOSTUFF ENET_JTAG_TMS
R9695 1K NOSTUFF ENET_JTAG_TDI
PP3V3_S5
R9686 4.99K NOSTUFF ENET_SYNC_1588
PULL UP / DOWNS
PP3V3_ENET
R9699 4.99K ENET:10G ENET_SMB_ALERT_L
R9698 4.99K NOSTUFF
R9612 4.99K ENET_REFCLK:OSC ENET_XTAL_SELECT_L
R9610 0 ENET_REFCLK:CRYSTAL
PULL DOWNS
R9697 1K NOSTUFF ENET_JTAG_TCK
R9688 4.99K ENET:10G ENET_JTAG_TRST_L
R9611 0 NOSTUFF ENET_SYNC_1588
R9613 10K ENET:10G ENET_GPIO1_EFUSE_EN
BOM_COST_GROUP=ETHERNET
SYNC_MASTER=MGry
SYNC_DATE=04/26/2018
PAGE TITLE
10G ETHERNET CONTROLLER 1
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 96 OF 142
SHEET 82 OF 115
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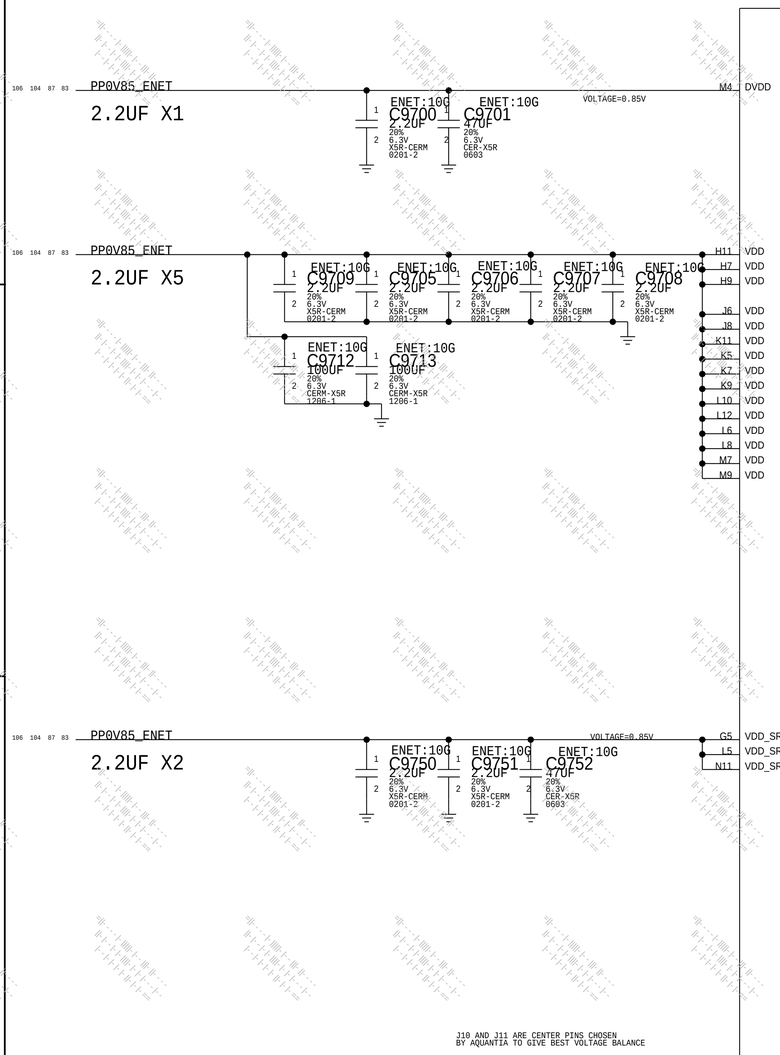
Please do NOT change the bypass caps before DCDC stability check and approval!!



PULL UPS

SYNC_MASTER=dvt SYNC_DATE=04/26/2018

PAGE TITLE: 10G ETHERNET CONTROLLER 2

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 97 OF 142
SHEET: 83 OF 115

R2D ETHERNET PCIE CAPS

PCIE_ENET_R2D_C_N<0> → C9840 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_R2D_N<0>
PCIE_ENET_R2D_C_P<0> → C9841 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_R2D_P<0>
PCIE_ENET_R2D_C_N<1> → C9842 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_R2D_N<1>
PCIE_ENET_R2D_C_P<1> → C9843 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_R2D_P<1>
PCIE_ENET_R2D_C_N<2> → C9844 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_R2D_N<2>
PCIE_ENET_R2D_C_P<2> → C9845 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_R2D_P<2>
PCIE_ENET_R2D_C_N<3> → C9846 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_R2D_N<3>
PCIE_ENET_R2D_C_P<3> → C9847 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_R2D_P<3>

D2R ETHERNET PCIE CAPS

PCIE_ENET_D2R_C_N<0> → C9850 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_D2R_N<0>
PCIE_ENET_D2R_C_P<0> → C9851 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_D2R_P<0>
PCIE_ENET_D2R_C_N<1> → C9852 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_D2R_N<1>
PCIE_ENET_D2R_C_P<1> → C9853 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_D2R_P<1>
PCIE_ENET_D2R_C_N<2> → C9854 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_D2R_N<2>
PCIE_ENET_D2R_C_P<2> → C9855 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_D2R_P<2>
PCIE_ENET_D2R_C_N<3> → C9856 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_D2R_N<3>
PCIE_ENET_D2R_C_P<3> → C9857 0.1UF 0201 X7R 6.3V 10% ENET:10G → PCIE_ENET_D2R_P<3>

1588 EXTERNAL LVDS OSCILLATOR

PP3V3_ENET → L9860 FERR-600-OHM-2A 0805 ENET:10G
PP3V3_ENET → C9860 2.2UF 20% 6.3V X5R-CERM 0201-2 ENET:10G
PP3V3_ENET → R9866 0 5% 1/16W MF-LF 402 ENET:10G
PP3V3_G3H_1588_OSC VOLTAGE=3.3V → C9861 47UF 20% 6.3V CER-X5R 0603 ENET:10G
PP3V3_G3H_1588_OSC → C9862 0.1UF 10% 6.3V X7R 0201 ENET:10G

U9860 50MHZ-50PPM-3.3V 5.00X3.20-SM ENET:10G
OSC_1588_OE → OE
NC → NC
VDD → PP3V3_G3H_1588_OSC
GND
OUT → OSC_1588_50MHZ_P → R9864 NOSTUFF 1/16W 5% MF-LF 402 → ENET_OSC_1588_50MHZ_P
OUT* → OSC_1588_50MHZ_N → R9865 NOSTUFF 1/16W 5% MF-LF 402 → ENET_OSC_1588_50MHZ_N

FLASH MEMORY

PP3V3_ENET → R9890 1K 5% 1/16W MF-LF 402 ENET:10G
PP3V3_ENET → R9891 1K 5% 1/16W MF-LF 402 ENET:10G
PP3V3_ENET → R9892 4.99K 1% 1/20W MF 201 ENET:10G
PP3V3_ENET → C9890 1.0UF 10% 25V X6S 0402 ENET:10G

U9890 32MB-85MHZ-2.3V-3.6V SOIC CRITICAL AT45DB321E OMIT_TABLE
VCC → PP3V3_ENET
ENET_10G_SCLK → SCK
ENET_10G_CS_L → CS*
ENET_10G_SPI_WP_L → WP*
ENET_10G_SPI_RST_L → RESET*
GND
SI ← ENET_10G_MOSI
SO → ENET_10G_MISO_R → R9893 0 5% 1/16W MF-LF 402 ENET:10G PLACE_NEAR=U9890.8:5MM → ENET_10G_MISO

JTAG TPS

ENET_JTAG_TRST_L → TP9820
ENET_JTAG_TDI → TP9821
ENET_JTAG_TCK → TP9822
ENET_JTAG_TMS → TP9823
ENET_JTAG_TDO → TP9824

ETHERNET ACTIVITY LEDS

PP3V3_ENET → R9830 390 5% 1/16W MF-LF 402 DEBUG_LEDS:10G → ENET0_LED → DS9830 GRN-SMCD-0.03A 0805
PP3V3_ENET → R9831 390 5% 1/16W MF-LF 402 DEBUG_LEDS:10G → ENET1_LED → DS9831 AMBER-0805NM-35-56MCD LTST-C281KFKT-5M
PP3V3_ENET → R9832 390 5% 1/16W MF-LF 402 DEBUG_LEDS:10G → ENET2_LED → DS9832 GRN-SMCD-0.03A 0805

ENET_LED_A0
ENET_LED_A1
ENET_LED_A2

AQC ON-DIE THERMAL SENSE (TIED)

ENET_TSENS_A_N → R9860 NOSTUFF 1/16W 5% MF-LF 402 NO_XNET_CONNECTION=1
ENET_TSENS_E_N → R9861 ENET:10G 0 1/16W 5% MF-LF 402 NO_XNET_CONNECTION=1 → ENET_TSENS_N
ENET_TSENS_A_P → R9862 NOSTUFF 1/16W 5% MF-LF 402 NO_XNET_CONNECTION=1
ENET_TSENS_E_P → R9863 ENET:10G 0 1/16W 5% MF-LF 402 NO_XNET_CONNECTION=1 → ENET_TSENS_P

SPARE MOSFET

NC_MEDIA_SENSE_SF_G
NC_MEDIA_SENSE_SF_S
NC_MEDIA_SENSE_SF_D
Q9880 DMN5L06VK-7 SOT563 VER 5 VTH MAX IS 1.0 V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00074	2	dual FET	Q9820,Q9835	CRITICAL	

ENET MEDIA SENSE LEVEL SHIFTER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00074	1	dual FET	Q9880	CRITICAL	ENET:1G

ENET_MEDIA_SENSE_3V3 → R9887 NOSTUFF 1/16W 5% MF-LF 402 → ENET_SENSE_FET_LS
ENET_MEDIA_SENSE_SD00_3V3 → R9888 NOSTUFF 1/16W 5% MF-LF 402
From Caesar IV: ENET_1G_MEDIA_SENSE → R9899 ENET:1G 0 1/16W 5% MF-LF 402

Q9880 DMN5L06VK-7 SOT563 VER 3 VTH MAX IS 1.0 V OMIT_TABLE
PP1V8_SLPS2R → D
ENET_SENSE_FET_LS → G
ENET_MEDIA_SENSE ← S
R9885 100K 5% 1/20W MF 201
R9886 30K 5% 1/20W MF 201

ENET WAKE LEVEL SHIFTER

PP3V3_ENET → R9820 47K 5% 1/20W MF 201
PP3V3_ENET → R9821 47K 5% 1/20W MF 201 → PCIEDN_WAKE
PP1V8_SLPS2R → R9822 NOSTUFF 47K 5% 1/20W MF 201 ENET WAKE HAS IPU → PCIEDN_WAKE_L

Q9820 DMN5L06VK-7 SOT563 VER 4 VTH MAX IS 1.0 V OMIT_TABLE
MAKE_BASE=TRUE
PCIEDN_WAKE_ENET_L → G
PCIEDN_WAKE → D
PCIEDN_WAKE_L → D
S → GND

ETHERNET SLAVE SMBUS DEBUG

ENET_SLAVE_SMB_CLK → TP9800
ENET_SLAVE_SMB_DAT → TP9801
TP9802

ETHERNET MULTI-MASTER SMBUS DEBUG

ENET_SMB_ALERT_L → TP9807
ENET_SMB_CLK → TP9805
ENET_SMB_DAT → TP9806
TP9808

LAYOUT NOTE: PLACE TPS AT 0.1MM PITCH IN STRAIGHT ROW IN SAME ORDER SHOWN HERE

50 MHZ REFCLK OSCILLATOR

PP3V3_ENET → L9880 FERR-600-OHM-2A 0805 ENET:10G
PP3V3_ENET → C9880 2.2UF 20% 6.3V X5R-CERM 0201 ENET:10G
PP3V3_G3H_ENET_REFCLK VOLTAGE=3.3V → R9889 0 5% 1/10W MF-LF 402 ENET:10G
PP3V3_G3H_ENET_REFCLK → C9881 47UF 20% 6.3V CER-X5R 0603 ENET:10G
PP3V3_G3H_ENET_REFCLK → C9882 0.1UF 10% 6.3V X7R 0201 ENET:10G

U9880 50MHZ-50PPM-3.3V 5.00X3.20-SM ENET:10G
OSC_REFCLK_OE → OE
NC → NC
VDD → PP3V3_G3H_ENET_REFCLK
GND
OUT → ENET_OSC_REFCLK_50MHZ_P
OUT* → ENET_OSC_REFCLK_50MHZ_N

USE OSCILLATOR BY DEFAULT
ENET_REFCLK:OSC
ENET_OSC_REFCLK_50MHZ_P → R9808 0 1/20W MF 0201 PLACE_NEAR=R9806.2:1MM → ENET_REFCLK_50MHZ_P
ENET_OSC_REFCLK_50MHZ_N → R9807 0 1/20W MF 0201 PLACE_NEAR=R9805.2:1MM → ENET_REFCLK_50MHZ_N
ENET_REFCLK:OSC

50 MHZ REFCLK CRYSTAL

ENET_XTALO_R → C9800 3.0PF +/-0.25PF 25V NP0-C0G 0201 ENET:10G
ENET_XTALO_R → Y9800 50MHZ-45PPM-8PF 2.0X1P6-SM ENET:10G PLACE_NEAR=U9600.F14:5.5MM APN 197S00104
ENET_XTALI → C9801 3.0PF +/-0.25PF 25V NP0-C0G 0201 ENET:10G
ENET_XTALO_R → R9800 0 5% 1/10W MF-LF 402 ENET:10G NO_XNET_CONNECTION=1
ENET_XTALO → R9801 NOSTUFF 1M 5% 1/10W MF-LF 402 NO_XNET_CONNECTION=1
ENET_REFCLK:CRYSTAL → R9805 0 1/20W 5% MF 0201 NO_XNET_CONNECTION=1
ENET_REFCLK:CRYSTAL → R9806 0 1/20W 5% MF 0201 NO_XNET_CONNECTION=1

BOM_COST_GROUP=ETHERNET

SYNC_MASTER=MGary SYNC_DATE=04/26/2018
PAGE TITLE: 10G ENET SUPPORT 1
Apple Inc.
DRAWING NUMBER: 051-02424 SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 98 OF 142
SHEET: 84 OF 115

FROM PHY

TO RJ45

RJ45
CRITICAL
J9900
RJ45-RCPT-X1037
F-RT-TH

CENTER TAP CONNECTIONS - PHY SIDE

CENTER TAP CONNECTIONS - CONNECTOR SIDE

EFUSE 1.5V VR

BOM_COST_GROUP=ETHERNET

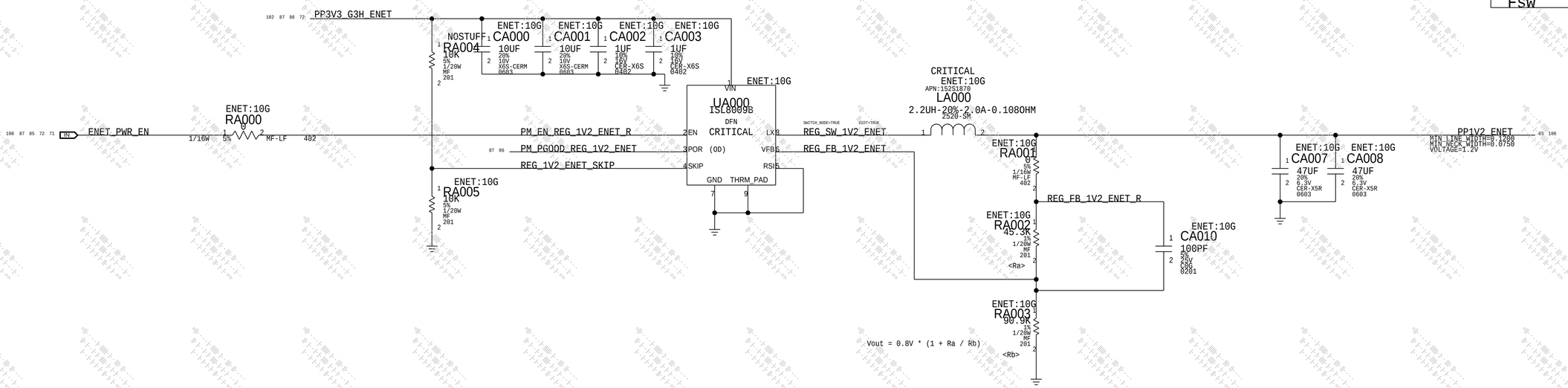
PAGE TITLE: 10G ENET SUPPORT 2

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 99 OF 142
SHEET: 85 OF 115

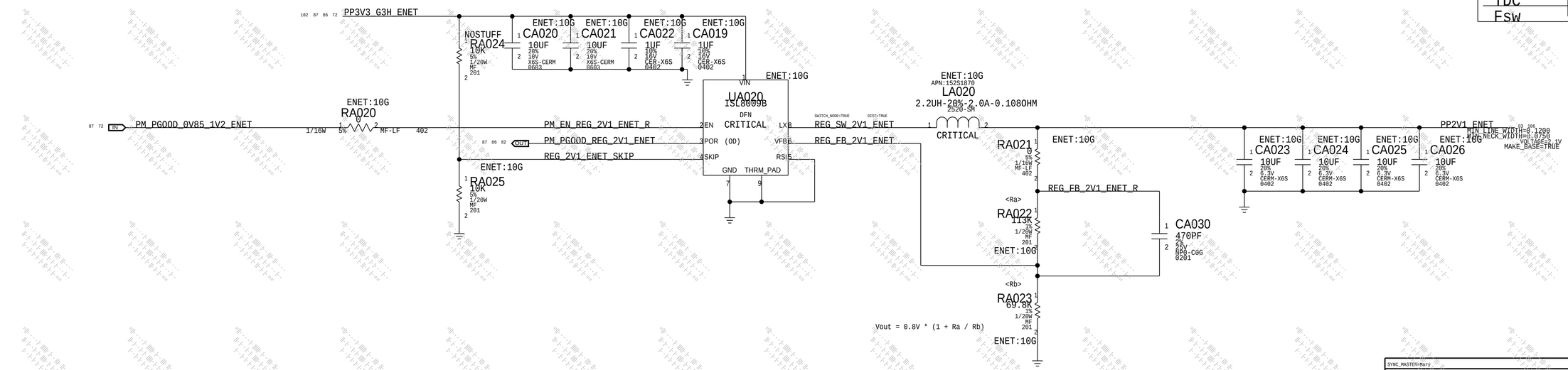
1.2V ENET REGULATOR

ENET 1V2 REGULATOR		
VOUT		1.20 V
EDC		1 A
OC	(TYP)	2.2 A
TDC		0.9 A
Fsw		1.6 MHZ



2.1V ENET REGULATOR

ENET 2V1 REGULATOR		
VOUT		2.10 V
EDC		0.5 A
OC	(TYP)	2.2 A
TDC		0.4 A
Fsw		1.6 MHZ



PP3V3_G3S 59 103 106

RA098 100K 5% 1/16W MF-LF 402 PM_PGOOD_REG_2V1_ENET 82 86 87

RA099 100K 5% 1/16W MF-LF 402 PM_PGOOD_REG_1V2_ENET 86 87

BOM_COST_GROUP=ETHERNET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: VR 10G ENET 1V2, 2V1

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

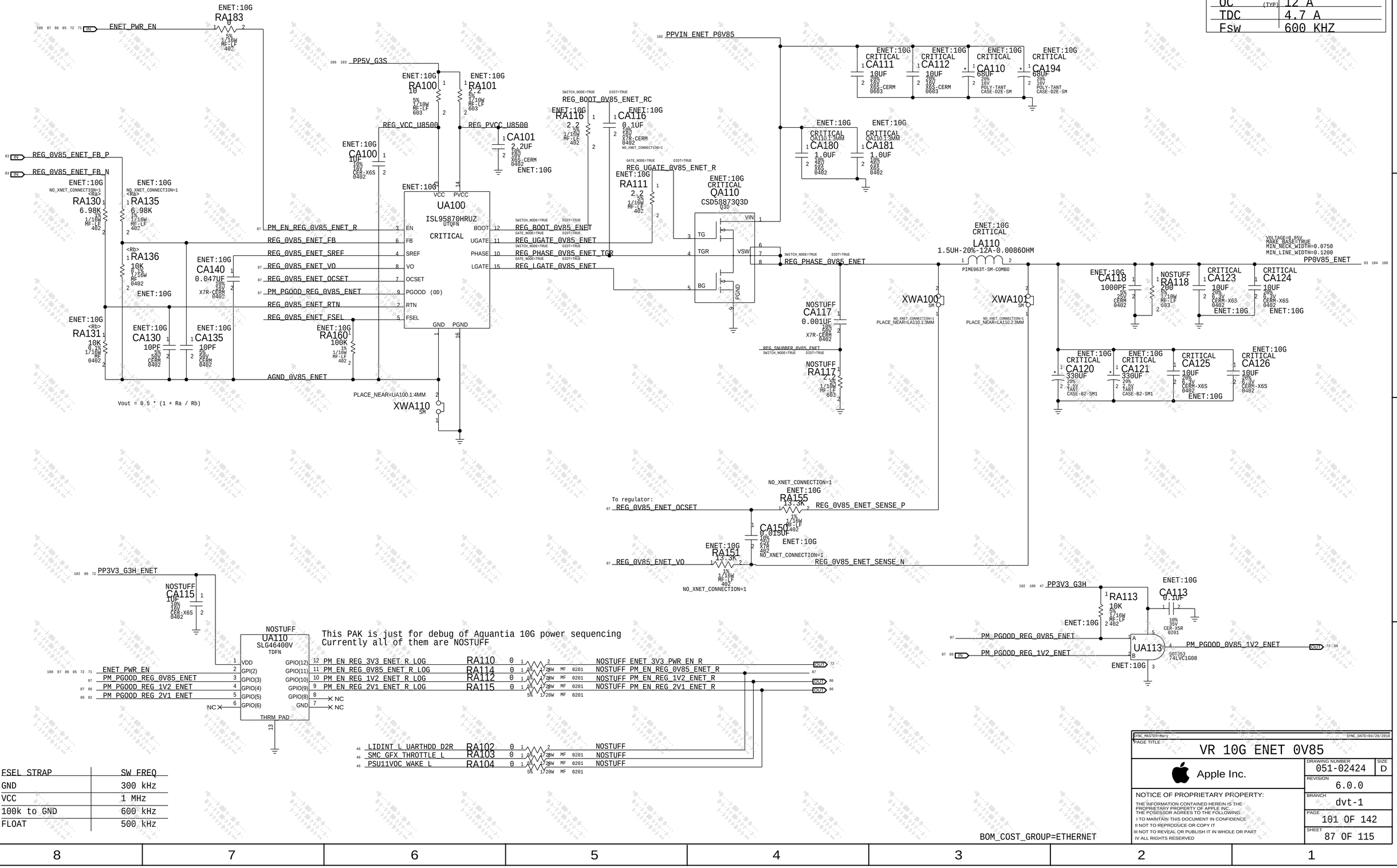
REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 100 OF 142

SHEET: 86 OF 115

ENET 0V85 REGULATOR		
VOUT		0.85 V
EDC		6.5 A
OC	(TYP)	12 A
TDC		4.7 A
Fsw		600 KHZ



FSEL STRAP	SW FREQ
GND	300 kHz
VCC	1 MHz
100k to GND	600 kHz
FLOAT	500 kHz

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: VR 10G ENET 0V85

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 101 OF 142

SHEET: 87 OF 115

HDMI CONNECTOR

THRU-HOLE

CRITICAL
JA600
HDMI-RCPT-X1037
F-RT-TH

514-00082
SHLD PINS

HDMI SPEC 1.4B (SEC 4.2.9):
HPD H:2.0 - 5.3V [SOURCE REQ]
HPD L:0.0 - 0.8V [SOURCE REQ]

HDMI SPEC 1.4B (SEC 4.2.10):
CEC H:2.50 - 3.63V
CEC L:0.00 - 0.60V
*ELEC SPECS NOT IN 2.0 SPEC YET

HDMI SPEC 1.4B (SEC 4.2.7):
+5.0V H: 5.3V [SOURCE REQ]
+5.0V L: 4.8V [SOURCE REQ]
*ELEC SPECS NOT IN 2.0 SPEC YET

(PER HDMI SPEC, SOURCE MUST SUPPLY MINIMUM 55 MA TO SINK)

(0.5A OVER-CURRENT LIMIT IMPLEMENTED)

CAPACITANCE = 0.4PF
CLAMPING VOLTAGE = 7.0V
IEC 61000-4-2 ESD: +/-30KV (AIR), +/-25KV (CONTACT)
IEC 61000-4-4 EFT: 40A (5/50NS)
IEC 61000-4-5 SURGE: 5A (8/20US)

PIN DIODE VOLTAGE DROP = 0.8V
CURRENT PER DIODE:
(3.3V - 0.8V) / 1K = 2.5MA
CURRENT THROUGH 16 DIODES = 40MA

TIME FOR VOLTAGE TO DISCHARGE
FROM 3.3V TO 0.8V
USING 0.1UF AND 10K = 1.4MS

DP2HDMI_1.5G_FILT_EN	PIN DIODE	FILTER
LOW	UNBIASED	6GBPS
HI	BIASED	1.5GBPS

REVERSE VOLTAGE PROTECTION

OVERCURRENT PROTECTION

* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.

BOM_COST_GROUP=HDMI

PAGE TITLE	HDMI CONNECTOR
Apple Inc.	DRAWING NUMBER 051-02424 · SIZE D
	REVISION 6.0.0
	BRANCH dvt-1
	PAGE 106 OF 142
	SHEET 88 OF 115

NOTE:
TERMINATION R INTEGRATED IN PCON.
NO EXT. TERMINATION NEEDED.

* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.

0.5PF CAP AND 8.2OHM RESISTORS ARE BASED ON EMPIRICAL TESTING WITH MEGACHIPS TO IMPROVE INTEROPERABILITY

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S0724	2	0.00 OHM 0201 RES	LA700,LA701	NO_CFILT
152S1073	2	8.2UH 0201 IND	LA700,LA701	CLK_FILT
118S0724	4	0.00 OHM 0201 RES	LA703,LA704,LA705,LA707	NO_DFILT
118S0724	2	0.00 OHM 0201 RES	LA709,LA710	NO_DFILT
152S2036	4	2.5UH 0201 IND	LA703,LA704,LA706,LA707	DATA_FILT
152S2036	2	2.5UH 0201 IND	LA709,LA710	DATA_FILT

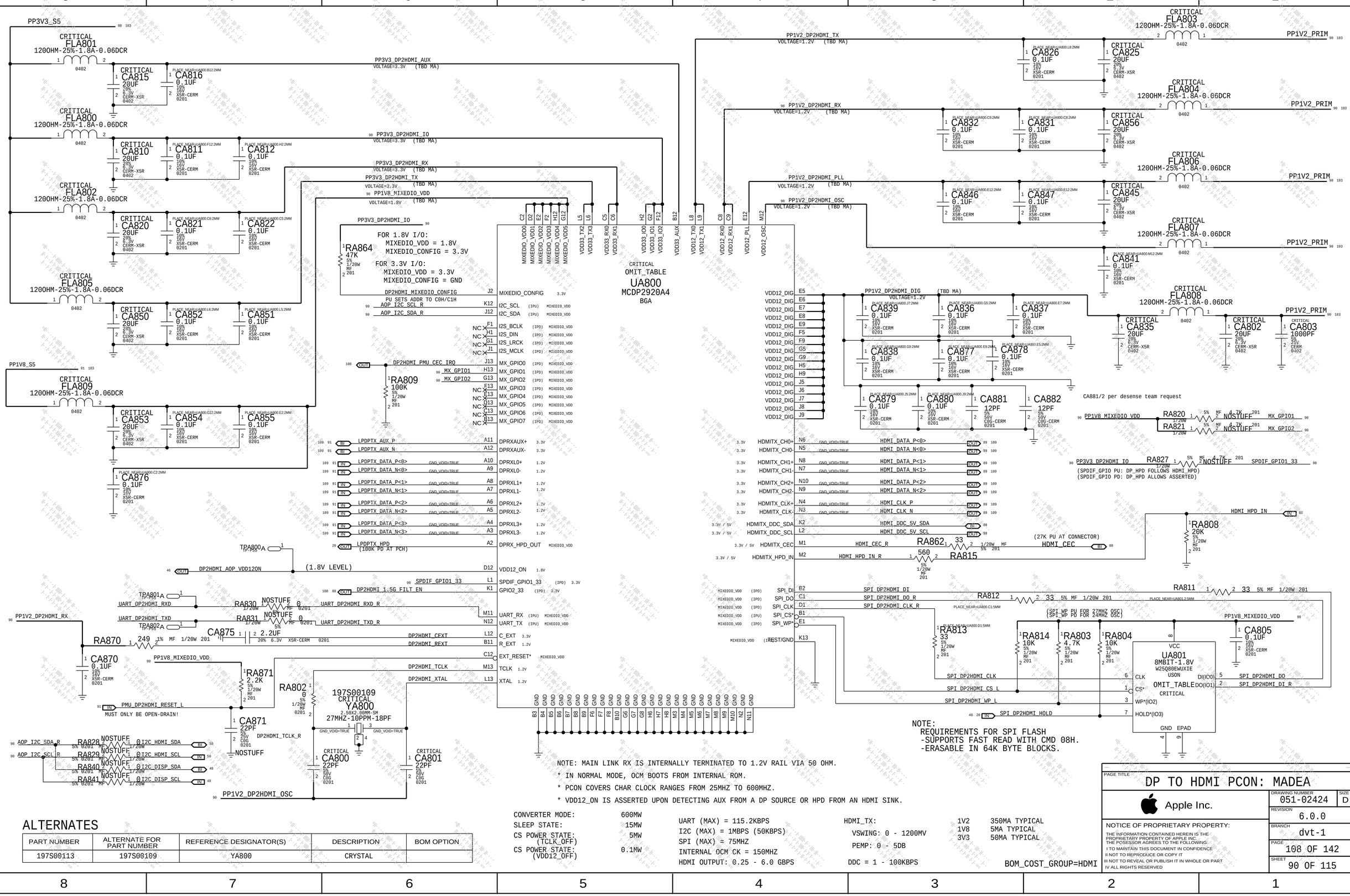
FILTER APN NUMBERS
0.2PF: 131S0431
3.0PF: 131S00093
4.0PF: 131S0597
3.0NH: 152S2045
CMCC: 155S0897
PIN DIODE: 377S00047
ESD DIODE: 377S0178

BOM_COST_GROUP=HDMI

PAGE TITLE: HDMI DESENSE FILTERS

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 107 OF 142
SHEET: 89 OF 115



ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
197S00113	197S00109	YA800	CRYSTAL	

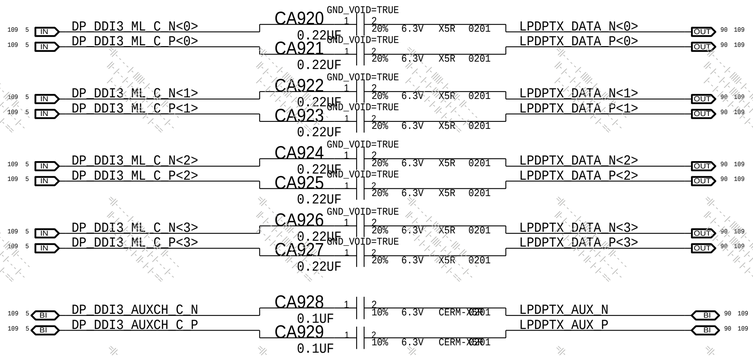
PAGE TITLE: DP TO HDMI PCON: MADEA

Apple Inc.

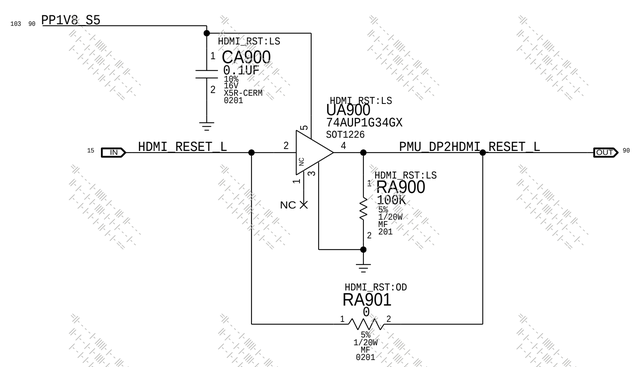
DRAWING NUMBER	051-02424
SIZE	D
REVISION	6.0.0
BRANCH	dvt-1
PAGE	108 OF 142
SHEET	90 OF 115

DDI interface AC Caps

From CPU



To HDMI



BOM_COST_GROUP=HDMI

PAGE TITLE: HDMI PROJECT SUPPORT

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 109 OF 142
SHEET: 91 OF 115

PP3V3_UPC_TA_LDO

RB090 3.3K 5% 1/20W MF 201
RB091 3.3K 5% 1/20W MF 201
RB093 3.3K 5% 1/20W MF 201
RB092 3.3K 5% 1/20W MF 201
CB090 1UF 10% 6.3V CERM 402

UB090 8MBIT-3.0V W25Q80DVUXIE USON OMIT_TABLE CRITICAL

TBT_T_SPI_CLK	CLK	DI(IO0)	TBT_T_SPI_MOSI
TBT_T_SPI_CS_L	CS*	DO(IO1)	TBT_T_SPI_MISO
TBT_T_ROM_WP_L	WP*(IO2)		
TBT_T_ROM_HOLD_L	HOLD*(IO3)		
	GND EPAD		

SNK0 AC Coupling

DP_T_SNK0_ML_C_P<0>	CB020 0.22UF	DP_T_SNK0_ML_P<0>
DP_T_SNK0_ML_C_N<0>	CB021 0.22UF	DP_T_SNK0_ML_N<0>
DP_T_SNK0_ML_C_P<1>	CB022 0.22UF	DP_T_SNK0_ML_P<1>
DP_T_SNK0_ML_C_N<1>	CB023 0.22UF	DP_T_SNK0_ML_N<1>
DP_T_SNK0_ML_C_P<2>	CB024 0.22UF	DP_T_SNK0_ML_P<2>
DP_T_SNK0_ML_C_N<2>	CB025 0.22UF	DP_T_SNK0_ML_N<2>
DP_T_SNK0_ML_C_P<3>	CB026 0.22UF	DP_T_SNK0_ML_P<3>
DP_T_SNK0_ML_C_N<3>	CB027 0.22UF	DP_T_SNK0_ML_N<3>
DP_T_SNK0_AUXCH_C_P	CB028 0.1UF	DP_T_SNK0_AUXCH_P
DP_T_SNK0_AUXCH_C_N	CB029 0.1UF	DP_T_SNK0_AUXCH_N

GND_VOID=TRUE; 20% 6.3V 0201 XSR; CERM-X5R

SNK1 AC Coupling

DP_T_SNK1_ML_C_P<0>	CB030 0.22UF	DP_T_SNK1_ML_P<0>
DP_T_SNK1_ML_C_N<0>	CB031 0.22UF	DP_T_SNK1_ML_N<0>
DP_T_SNK1_ML_C_P<1>	CB032 0.22UF	DP_T_SNK1_ML_P<1>
DP_T_SNK1_ML_C_N<1>	CB033 0.22UF	DP_T_SNK1_ML_N<1>
DP_T_SNK1_ML_C_P<2>	CB034 0.22UF	DP_T_SNK1_ML_P<2>
DP_T_SNK1_ML_C_N<2>	CB035 0.22UF	DP_T_SNK1_ML_N<2>
DP_T_SNK1_ML_C_P<3>	CB036 0.22UF	DP_T_SNK1_ML_P<3>
DP_T_SNK1_ML_C_N<3>	CB037 0.22UF	DP_T_SNK1_ML_N<3>
DP_T_SNK1_AUXCH_C_P	CB038 0.1UF	DP_T_SNK1_AUXCH_P
DP_T_SNK1_AUXCH_C_N	CB039 0.1UF	DP_T_SNK1_AUXCH_N

GND_VOID=TRUE; 20% 6.3V 0201 XSR; CERM-X5R

PP3V3_TBT_T_SX

RB064 100K	TBT_T_BATLOW_L	
RB039 10K NOSTUFF	PU TO PWR_MVM	
RB063 100K	TBT_T_TMU_CLK_IN	
RB073 100K	TBT_T_TMU_CLK_OUT	
RB062 100K	DP_TA_HPD	
RB072 100K	DP_TB_HPD	
RB060 100K	TBT_TA_USB2_MXCTL	
RB061 100K	TBT_TB_USB2_MXCTL	

5% 1/20W MF 201

UB000 TITAN-RIDGE-QTZZ CSP SYM 1 OF 2 OMIT_TABLE CRITICAL

PCIE_TBT_T_R2D_P<0>	PCIE_RX0_P	Y23	PCIE_TX0_P	V23 PCIE_TBT_T_D2R_C_P<0>
PCIE_TBT_T_R2D_N<0>	PCIE_RX0_N	Y22	PCIE_TX0_N	V22 PCIE_TBT_T_D2R_C_N<0>
PCIE_TBT_T_R2D_P<1>	PCIE_RX1_P	T23	PCIE_TX1_P	P23 PCIE_TBT_T_D2R_C_P<1>
PCIE_TBT_T_R2D_N<1>	PCIE_RX1_N	T22	PCIE_TX1_N	P22 PCIE_TBT_T_D2R_C_N<1>
PCIE_TBT_T_R2D_P<2>	PCIE_RX2_P	M23	PCIE_TX2_P	K23 PCIE_TBT_T_D2R_C_P<2>
PCIE_TBT_T_R2D_N<2>	PCIE_RX2_N	M22	PCIE_TX2_N	K22 PCIE_TBT_T_D2R_C_N<2>
PCIE_TBT_T_R2D_P<3>	PCIE_RX3_P	H23	PCIE_TX3_P	F23 PCIE_TBT_T_D2R_C_P<3>
PCIE_TBT_T_R2D_N<3>	PCIE_RX3_N	H22	PCIE_TX3_N	F22 PCIE_TBT_T_D2R_C_N<3>
PCIE_CLK100M_TBT_T_P	PCIE_REFCLK_100_IN_P	V19		
PCIE_CLK100M_TBT_T_N	PCIE_REFCLK_100_IN_N	T19		
TBT_T_CLKREQ_R_L	PCIE_CLKREQ*	Y6	PERST*	T4 TBT_T_PCI_RESET_L
			PCIE_RBIAS	N16 TBT_T_PCIE_BIAS

PCIE GEN3

RB028 1K 1% 1/20W MF 201 — TBT_T_CLKREQ_L

PLACE_NEAR=UB000.N16:2MM
RB051 3.01K 1% 1/20W MF 201

DP_T_SNK0_ML_P<0>	DPSNK1_ML0_P	AC7	DPSRC_ML0_P	AB21 NC_DP_T_SRC_ML_P<0>
DP_T_SNK0_ML_N<0>	DPSNK1_ML0_N	AB7	DPSRC_ML0_N	AC21 NC_DP_T_SRC_ML_N<0>
DP_T_SNK0_ML_P<1>	DPSNK1_ML1_P	AB9	DPSRC_ML1_P	AC19 NC_DP_T_SRC_ML_P<1>
DP_T_SNK0_ML_N<1>	DPSNK1_ML1_N	AC9	DPSRC_ML1_N	AB19 NC_DP_T_SRC_ML_N<1>
DP_T_SNK0_ML_P<2>	DPSNK1_ML2_P	AC11	DPSRC_ML2_P	AB17 NC_DP_T_SRC_ML_P<2>
DP_T_SNK0_ML_N<2>	DPSNK1_ML2_N	AB11	DPSRC_ML2_N	AC17 NC_DP_T_SRC_ML_N<2>
DP_T_SNK0_ML_P<3>	DPSNK1_ML3_P	AB13	DPSRC_ML3_P	AC15 NC_DP_T_SRC_ML_P<3>
DP_T_SNK0_ML_N<3>	DPSNK1_ML3_N	AC13	DPSRC_ML3_N	AB15 NC_DP_T_SRC_ML_N<3>
DP_T_SNK0_AUXCH_P	DPSNK1_AUX_P	N1	DPSRC_AUX_P	N4 NC_DP_T_SRC_AUX_P
DP_T_SNK0_AUXCH_N	DPSNK1_AUX_N	N2	DPSRC_AUX_N	N5 NC_DP_T_SRC_AUX_N
DP_T_SNK0_HPD	SNK1_HPD	AA2	DPSRC_HPD	R5 DP_T_SRC_HPD
DP_T_SNK1_ML_P<0>	DPSNK2_ML0_P	A5	GPIO_0	W1 DDI2_MUX_SEL
DP_T_SNK1_ML_N<0>	DPSNK2_ML0_N	B5	GPIO_1	W2 DDI1_MUX_SEL
DP_T_SNK1_ML_P<1>	DPSNK2_ML1_P	B3	EE_WP*	W4 TBT_T_ROM_WP_L
DP_T_SNK1_ML_N<1>	DPSNK2_ML1_N	A3	TMU_CLKOUT	Y1 TBT_T_TMU_CLK_OUT
DP_T_SNK1_ML_P<2>	DPSNK2_ML2_P	C2	WAKE*	Y2 TBT_WAKE_3V3_L
DP_T_SNK1_ML_N<2>	DPSNK2_ML2_N	C1	CIO_PLUG_EVENT*	AA1 TBT_T_PLUG_EVENT_L
DP_T_SNK1_ML_P<3>	DPSNK2_ML3_P	E2	TMU_CLKIN	W6 TBT_T_TMU_CLK_IN
DP_T_SNK1_ML_N<3>	DPSNK2_ML3_N	E1	I2C_SCL	V2 I2C_TBT_T_SCL
DP_T_SNK1_AUXCH_P	DPSNK2_AUX_P	P1	I2C_SDA	V1 I2C_TBT_T_SDA
DP_T_SNK1_AUXCH_N	DPSNK2_AUX_N	P2	USB_FORCE_PWR	V5 TBT_T_USB_PWR_EN
DP_T_SNK1_HPD	SNK2_HPD	Y4	FORCE_PWR	V4 TBT_T_CIO_PWR_EN
			BATLOW*	U2 TBT_T_BATLOW_L
			SLP_S3*	U1 PM_SLP_S3_L
			RTD3_PWR_EN	T5 TBT_T_RTD3_PWR_EN
			RESET*	E5 USBC_T_RESET_R_L
			XTAL_25_IN	D22 TBT_T_XTAL25M_IN
			XTAL_25_OUT	D23 TBT_T_XTAL25M_OUT
			EE_DI	Y16 UPC_T_SPI_MOSI
			EE_DO	W16 UPC_T_SPI_MISO
			EE_CS*	W18 UPC_T_SPI_CS_L
			EE_CLK	Y16 UPC_T_SPI_CLK

SINK PORT 1 / SINK PORT 2 / SOURCE PORT / LC GPIO / POC GPIO / FLASH

PU at PCH

PP3V3_UPC_TA_LDO
PP3V3_TBT_T_SX

RB034 2.2K 5% 1/20W MF 201
RB035 2.2K 5% 1/20W MF 201
RB027 100K 5% 1/20W MF 201 NOSTUFF
RB010 100K 5% 1/20W MF 201

To SPI Flash

RB030 100K 5% 1/20W MF 201 — SNK1_HPD

RB031 100K 5% 1/20W MF 201 — SNK2_HPD

	U0_SSTXP1	AC5		
	U0_SSTXN1	AB5		
	U0_SSRXP1	AC3		
	U0_SSRXN1	AB3		
JTAG_ISP_TDI	TDI	W20		
JTAG_TBT_T_TMS	TMS	Y20		
JTAG_ISP_TCK	TCK	W19		
JTAG_ISP_TDO	TDO	Y19		
TBT_T_TEST_EN	TEST_EN	R4		
TBT_T_TEST_PWR_GOOD	TEST_PWR_GOOD	W5		
USBC_TA_D2R_P<2>	ASSRXP2	A15	BSSRXp2	B7 USBC_TB_D2R_P<2>
USBC_TA_D2R_N<2>	ASSRXN2	B15	BSSRXn2	A7 USBC_TB_D2R_N<2>
USBC_TA_R2D_C_P<2>	ASSTXP2	A17	BSSTXp2	A9 USBC_TB_R2D_C_P<2>
USBC_TA_R2D_C_N<2>	ASSTXN2	B17	BSSTXn2	B9 USBC_TB_R2D_C_N<2>
USBC_TA_R2D_C_P<1>	ASSTXP1	A19	BSSTXp1	A11 USBC_TB_R2D_C_P<1>
USBC_TA_R2D_C_N<1>	ASSTXN1	B19	BSSTXn1	B11 USBC_TB_R2D_C_N<1>
USBC_TA_D2R_P<1>	ASSRXP1	B21	BSSRXp1	A13 USBC_TB_D2R_P<1>
USBC_TA_D2R_N<1>	ASSRXN1	A21	BSSRXn1	B13 USBC_TB_D2R_N<1>
USBC_TA_AUXLSX1	ASBU1	H4	BSBU1	L4 USBC_TB_AUXLSX1
USBC_TA_AUXLSX2	ASBU2	J4	BSBU2	L5 USBC_TB_AUXLSX2
	PA_USB2_D_P	E20	PB_USB2_D_P	E19 NC
	PA_USB2_D_N	D20	PB_USB2_D_N	D19 NC
DP_TA_HPD	PA_HPD	T2	PB_HPD	T1 DP_TB_HPD
I2C_TBT_TA_INT_L	PA_I2C_INT	M4	PB_I2C_INT	M5 I2C_TBT_TB_INT_L
TBT_TA_USB2_MXCTL	PA_USB2_MXCTL	R2	PB_USB2_MXCTL	R1 TBT_TB_USB2_MXCTL
TBT_TA_USB2_RBIAS	PA_USB2_RBIAS	H19	PB_USB2_RBIAS	F19 TBT_TB_USB2_RBIAS

TBT PORT A / TBT PORT B / USBSS / JTAG

PP3V3_TBT_T_SX

RB036 2.2K 5% 1/20W MF 201 NOSTUFF

RB037 2.2K 5% 1/20W MF 201 NOSTUFF

PLACE_NEAR=UB000.H19:2MM
RB054 200 1% 1/20W MF 201

PLACE_NEAR=UB000.F19:2MM
RB053 200 1% 1/20W MF 201

RB055 4.75K 0.5% 0201 TF 1/20W — PLACE_NEAR=UB000.J5:2MM

PLACE_NEAR=UB000.J6:2MM

TBT_T_RBIAS	RBIAS	J6		
TBT_T_RSENSE	RSENSE	J5		
	PA_MONDC	A23		
	PB_MONDC	A1		
	PC_MONDC	AC23		
	USB_MONDC	AC1		
	TEST_EDM	D4		
	FUSE_VQPS_64	L8		
			USB2_ATEST	B23 NC
			PCIE_ATEST	AB23 NC
			MONDC_SVR	D5
			VGA_RES	H5 NC
			ATEST_P	J9 NC
			ATEST_N	J11 NC
			THERMDA	V8 TBTTHMSNS_T_D3_P

DEBUG

USE NEAREST GND BALL (AC22) FOR THERM_D_N

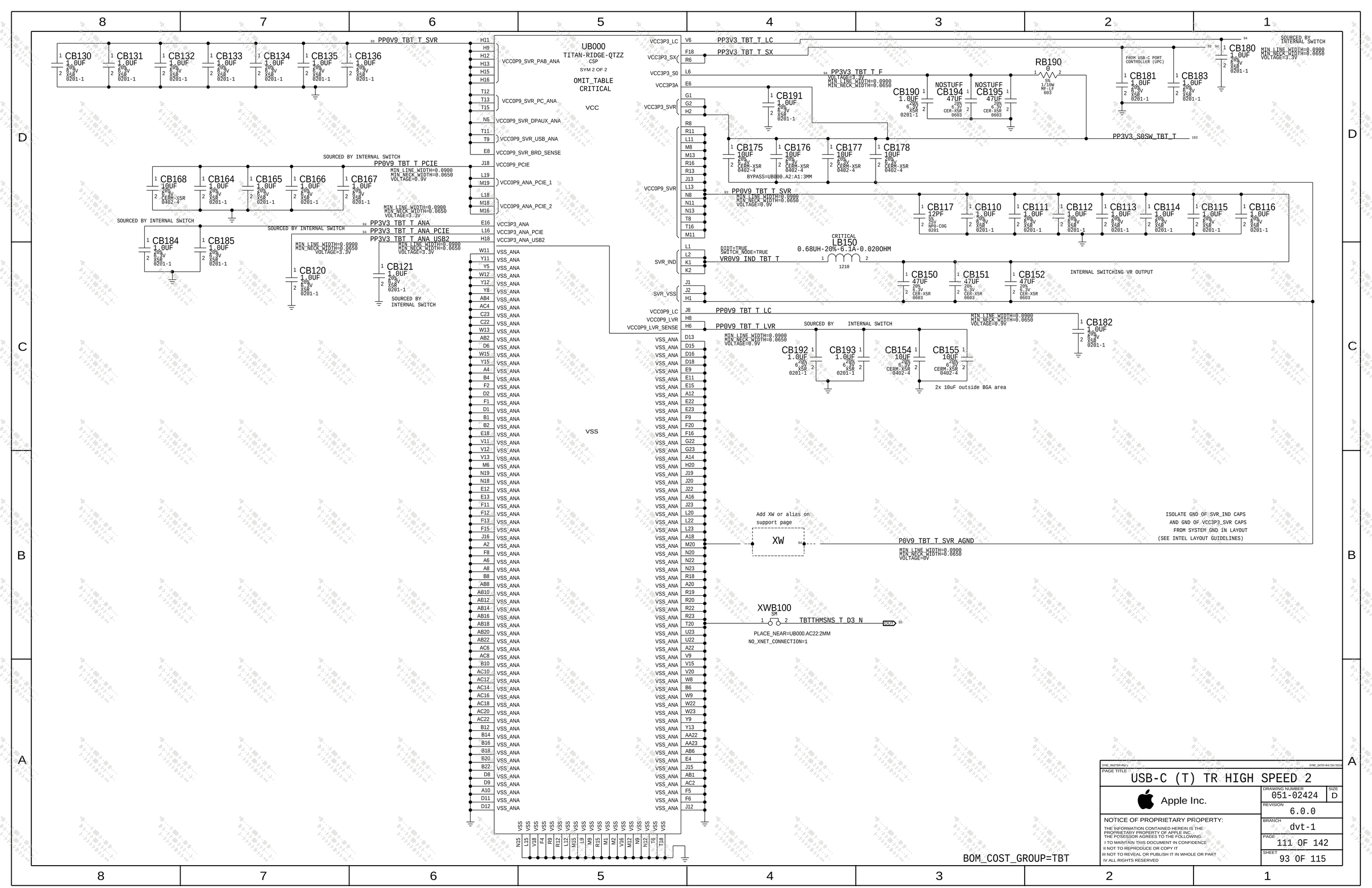
BOM_COST_GROUP=TBT

SYNC_MASTER=Mary — SYNC_DATE=04/26/2018

PAGE TITLE: USB-C (T) TR HIGH SPEED 1

Apple Inc.

DRAWING NUMBER 051-02424 — SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 110 OF 142
SHEET 92 OF 115


CB130 1.0UF 20% 6.3V X5R 0201-1
CB131 1.0UF 20% 6.3V X5R 0201-1
CB132 1.0UF 20% 6.3V X5R 0201-1
CB133 1.0UF 20% 6.3V X5R 0201-1
CB134 1.0UF 20% 6.3V X5R 0201-1
CB135 1.0UF 20% 6.3V X5R 0201-1
CB136 1.0UF 20% 6.3V X5R 0201-1
93 PP0V9_TBT_T_SVR
SOURCED BY INTERNAL SWITCH
PP0V9_TBT_T_PCIE
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0650
VOLTAGE=3.3V
VOLTAGE=0.9V
CB168 1.0UF 20% 6.3V CERM-X5R 0402-4
CB164 1.0UF 20% 6.3V X5R 0201-1
CB165 1.0UF 20% 6.3V X5R 0201-1
CB166 1.0UF 20% 6.3V X5R 0201-1
CB167 1.0UF 20% 6.3V X5R 0201-1
SOURCED BY INTERNAL SWITCH
94 PP3V3_TBT_T_ANA
94 PP3V3_TBT_T_ANA_PCIE
PP3V3_TBT_T_ANA_USB2
CB184 1.0UF 20% 6.3V X5R 0201-1
CB185 1.0UF 20% 6.3V X5R 0201-1
CB120 1.0UF 20% 6.3V X5R 0201-1
CB121 1.0UF 20% 6.3V X5R 0201-1
SOURCED BY INTERNAL SWITCH
UB000
TITAN-RIDGE-QTZZ
CSP
SYM 2 OF 2
OMIT_TABLE
CRITICAL
VCC
VSS
VCC3P3_LC
VCC3P3_SX
VCC3P3_S0
VCC3P3A
VCC3P3_SVR
VCC0P9_SVR
SVR_IND
SVR_VSS
VCC0P9_LC
VCC0P9_LVR
VCC0P9_LVR_SENSE
CB191 1.0UF 20% 6.3V X5R 0201-1
CB190 1.0UF 20% 6.3V X5R 0201-1
NOSTUFF CB194 47UF 20% 6.3V CER-X5R 0603
NOSTUFF CB195 47UF 20% 6.3V CER-X5R 0603
RB190 0 5% 1/10W MF-LF 0603
CB180 1.0UF 20% 6.3V X5R 0201-1
FROM USB-C PORT CONTROLLER (UPC)
CB181 1.0UF 20% 6.3V X5R 0201-1
CB183 1.0UF 20% 6.3V X5R 0201-1
SOURCED BY INTERNAL SWITCH
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0650
VOLTAGE=3.3V
94 PP3V3_TBT_T_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0650
PP3V3_TBT_T_LC
PP3V3_TBT_T_SX
PP3V3_S0SW_TBT_T
CB175 10UF 20% 6.3V CERM-X5R 0402-4
CB176 10UF 20% 6.3V CERM-X5R 0402-4
CB177 10UF 20% 6.3V CERM-X5R 0402-4
CB178 10UF 20% 6.3V CERM-X5R 0402-4
BYPASS=UB000.A2:A1:3MM
93 PP0V9_TBT_T_SVR
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0650
VOLTAGE=0.9V
CB117 12PF 5% 25V NP0-C0G 0201
CB110 1.0UF 20% 6.3V X5R 0201-1
CB111 1.0UF 20% 6.3V X5R 0201-1
CB112 1.0UF 20% 6.3V X5R 0201-1
CB113 1.0UF 20% 6.3V X5R 0201-1
CB114 1.0UF 20% 6.3V X5R 0201-1
CB115 1.0UF 20% 6.3V X5R 0201-1
CB116 1.0UF 20% 6.3V X5R 0201-1
DIDT=TRUE
SWITCH_NODE=TRUE
VR0V9_IND_TBT_T
CRITICAL
LB150
0.68UH-20%-6.1A-0.020OHM
1210
CB150 47UF 20% 6.3V CER-X5R 0603
CB151 47UF 20% 6.3V CER-X5R 0603
CB152 47UF 20% 6.3V CER-X5R 0603
INTERNAL SWITCHING VR OUTPUT
PP0V9_TBT_T_LC
PP0V9_TBT_T_LVR
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0650
VOLTAGE=0.9V
SOURCED BY INTERNAL SWITCH
CB192 1.0UF 20% 6.3V X5R 0201-1
CB193 1.0UF 20% 6.3V X5R 0201-1
CB154 10UF 20% 6.3V CERM-X5R 0402-4
CB155 10UF 20% 6.3V CERM-X5R 0402-4
2x 10uF outside BGA area
CB182 1.0UF 20% 6.3V X5R 0201-1
Add XW or alias on support page
XW
94
P0V9_TBT_T_SVR_AGND
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0650
VOLTAGE=0V
ISOLATE GND OF SVR_IND CAPS AND GND OF VCC3P3_SVR CAPS FROM SYSTEM GND IN LAYOUT (SEE INTEL LAYOUT GUIDELINES)
XWB100
SM
1
2
TBTTHMSNS_T_D3_N
OUT
65
PLACE_NEAR=UB000.AC22:2MM
NO_XNET_CONNECTION=1
BOM_COST_GROUP=TBT
SYNC_MASTER=Hary
SYNC_DATE=04/26/2018
PAGE TITLE
USB-C (T) TR HIGH SPEED 2
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 111 OF 142
SHEET 93 OF 115
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DP SRC OPTIONS

IF DP SRC NOT USED

92 NC_DP_T_SRC_ML_P<3..0> — NC_DP_T_SRC_ML_P<3..0> (MAKE_BASE=TRUE, NO_TEST=1)
92 NC_DP_T_SRC_ML_N<3..0> — NC_DP_T_SRC_ML_N<3..0> (MAKE_BASE=TRUE, NO_TEST=1)
92 NC_DP_T_SRC_AUX_P — NC_DP_T_SRC_AUX_P (MAKE_BASE=TRUE)
92 NC_DP_T_SRC_AUX_N — NC_DP_T_SRC_AUX_N (MAKE_BASE=TRUE)

RB240 100K 5% 1/20W MF 201
DP_T_SRC_HPD 92

RIDGE TBT_T ARKANOID CONN

Place on TOP

JB201 USBC_DBG 13 M-ST-SM 14 505070-1222

92 14 TBT_T_PLUG_EVENT_L	1	2	TBT_T_PCI_RESET_L 14 20 92
92 28 26 TBT_WAKE_3V3_L	3	4	USBC_T_RESET_L 94 95
95 94 92 14 96 TBT_T_CIO_PWR_EN	5	6	PP3V3_TBT_T_SX 72 92 94
95 94 92 14 96 TBT_T_USB_PWR_EN	7	8	PP3V3_TBT_T_ANA_PCIE 93
96 95 28 TBT_POC_RESET	9	10	PP3V3_TBT_T_ANA 93
93 PP3V3_TBT_T_F	11	12	PP3V3_TBT_T_LC 93 94
	15	16	

92 USBC_T_RESET_R_L — RB279 0 5% MF 1/20W 0201 — USBC_T_RESET_L 94 95

AARDVARKANOID CONN

Place on TOP

JB202 USBC_DBG 13 M-ST-SM 14 505070-1222

95 PP3V3_G3H_UPC_TA_R	1	2	TBT_T_SPI_CS_L 92 94
95 UPC_TA_SWD_DATA	3	4	TBT_T_SPI_CLK 92 94
95 UPC_TA_SWD_CLK	5	6	TBT_T_SPI_MOSI 92 94
94 92 TBT_T_SPI_MISO	7	8	UPC_TB_SWD_CLK 96
94 92 I2C_TBT_T_SDA	9	10	UPC_TB_SWD_DATA 96
94 92 I2C_TBT_T_SCL	11	12	PP3V3_G3H_UPC_TB_R 96
	15	16	

ACE ARKANOID CONN

Place on TOP

JB200 USBC_DBG 13 M-ST-SM 14 505070-1222

94 92 I2C_TBT_TB_INT_L	1	2	I2C_TBT_TA_INT_L 92 94
96 95 48 104 I2C_UPC_T_SCL2	3	4	I2C_TBT_T_SDA 92 94
96 95 48 104 I2C_UPC_T_SDA2	5	6	I2C_TBT_T_SCL 92 94
48 38 28 UPC_I2C_INT_L	7	8	TBT_T_CIO_PWR_EN 14 92 94 95 96
94 TBT_T_SPI_CLK_DBG	9	10	TBT_T_USB_PWR_EN 14 92 94 95 96
96 95 UPC_TA_UART_TX	11	12	UPC_TA_UART_RX 95 96
	15	16	

Pull-up and Pull-down

92 DDI2_MUX_SEL — DDI2_MUX_SEL (MAKE_BASE=TRUE) 21 94
92 DDI1_MUX_SEL — DDI1_MUX_SEL (MAKE_BASE=TRUE) 21 94

PP3V3_TBT_T_LC 93 94

RB250 100K 5% 1/20W MF 201 NOSTUFF — DDI1_MUX_SEL (MAKE_BASE=TRUE) 21 94
RB252 100K 5% 1/20W MF 201 NOSTUFF
RB251 100K 5% 1/20W MF 201 NOSTUFF — DDI2_MUX_SEL (MAKE_BASE=TRUE) 21 94

RB235 1M 201 MF 1/20W 5% — TBT_TA_LSTX 95
NOSTUFF RB236 1M 201 MF 1/20W 5% — TBT_TA_LSRX 95
RB237 1M 201 MF 1/20W 5% — TBT_TB_LSTX 96
NOSTUFF RB238 1M 201 MF 1/20W 5% — TBT_TB_LSRX 96
RB232 100K 201 MF 1/20W 5% — UPC_T_5V_EN 94

MAKE_BASE=TRUE — GND 95
MAKE_BASE=TRUE — GND 96

RIDGE 0.9V SVR XW

XWB200 SM 2 1 — P0V9_TBT_T_SVR_AGND 93
NO_XNET_CONNECTION=1

POWER ALIASES

94 92 72 PP3V3_TBT_T_SX (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, MAKE_BASE=TRUE) — PP3V3_TBT_T_SX 95 / PP3V3_TBT_T_SX 96 / PP3V3_TBT_T_SX 92 93
95 PP3V3_UPC_TA_LDO (MAKE_BASE=TRUE) — PP3V3_UPC_TA_LDO 92 95 / PP3V3_UPC_TA_LDO 92
96 PP3V3_UPC_TB_LDO (MAKE_BASE=TRUE) — PP3V3_UPC_TB_LDO 96

25MHz Xtal

92 IN TBT_T_XTAL25M_OUT — RB207 0 5% 1/20W MF 0201 — TBT_T_XTAL25M_OUT_R
NOSTUFF RB206 1M 5% 1/20W MF 201 to/from Ridge
CRITICAL YB200 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
CB202 20PF 5% 25V C0G 0201
CB203 20PF 5% 25V C0G 0201
92 OUT TBT_T_XTAL25M_IN

TBT to ACE

TBT — Alpine Ridge U2800 (MASTER)

MAKE_BASE=TRUE 92 94 I2C_TBT_T_SCL
MAKE_BASE=TRUE 92 94 I2C_TBT_T_SDA
MAKE_BASE=TRUE 92 94 I2C_TBT_TA_INT_L
MAKE_BASE=TRUE 92 94 I2C_TBT_TB_INT_L

Pri ACE — U3100 (Write: 0x70 Read: 0x71)

I2C_TBT_T_SCL 95
I2C_TBT_T_SDA 95
I2C_TBT_TA_INT_L 95

Sec ACE — U3200 (Write: 0x7E Read: 0x7F)

I2C_TBT_T_SCL 96
I2C_TBT_T_SDA 96
I2C_TBT_TB_INT_L 96

AR/ACE SPI BUS SERIES R'S

ROM
94 92 TBT_T_SPI_CLK
94 92 TBT_T_SPI_CS_L
94 92 TBT_T_SPI_MOSI
94 92 TBT_T_SPI_MISO

RB290 100 5% 1/20W MF 201 — TBT_T_SPI_CLK_DBG 94
RB280 15 5% 1/20W MF 201 — UPC_TA_SPI_CLK IN 95
RB281 15 5% 1/20W MF 201 — UPC_TA_SPI_CS_L IN 95
RB282 15 5% 1/20W MF 201 — UPC_TA_SPI_MOSI IN 95
RB283 15 5% 1/20W MF 201 — UPC_TA_SPI_MISO OUT 95
RB284 15 5% 1/20W MF 201 — UPC_T_SPI_CLK IN 92
RB285 15 5% 1/20W MF 201 — UPC_T_SPI_CS_L IN 92
RB286 15 5% 1/20W MF 201 — UPC_T_SPI_MOSI IN 92
RB287 15 5% 1/20W MF 201 — UPC_T_SPI_MISO OUT 92

Ace
TR

PP5V_G3S_USBC 28 103 107

CB200 220UF-35MOHM 20% 6.3V POLY-TANT CASE-B2-SM1

SIGNAL ALIASES

94 UPC_T_5V_EN (MAKE_BASE=TRUE) — UPC_T_5V_EN 95 / UPC_T_5V_EN 96

95 IN UPC_TA_FAULT_L — RB258 0 5% 1/20W MF 0201 — USB_TA_OC_L 14
96 IN UPC_TB_FAULT_L — RB259 0 5% 1/20W MF 0201 — USB_TB_OC_L 14
108 92 26 OUT JTAG_ISP_TDI — RB256 0 5% 1/20W MF 0201 — XDP_JTAG_ISP_TDI IN 14 18
108 92 26 OUT JTAG_ISP_TCK — RB257 0 5% 1/20W MF 0201 — XDP_JTAG_ISP_TCK IN 14 18
108 92 26 IN JTAG_ISP_TDO — RB255 0 5% 1/20W MF 0201 — XDP_JTAG_ISP_TDO OUT 14 18

TBT_X/T JTAG are connected together to PCH

Ridge PCIE Caps

R2D		D2R	
109 5 IN PCIE_TBT_T_R2D_C_P<0>	CB240 0.22UF 0201 X5R 6.3V 20% GND_VOID=TRUE	PCIE_TBT_T_D2R_C_P<0> OUT 92 109 92	IN 5 109 PCIE_TBT_T_D2R_C_P<0> CB250 0.22UF 0201 X5R 6.3V 20% GND_VOID=TRUE
109 5 IN PCIE_TBT_T_R2D_C_N<0>	CB241 0.22UF 0201 X5R 6.3V 20% GND_VOID=TRUE	PCIE_TBT_T_D2R_C_N<0> OUT 92 109 92	IN 5 109 PCIE_TBT_T_D2R_C_N<0> CB251 0.22UF 0201 X5R 6.3V 20% GND_VOID=TRUE
109 5 IN PCIE_TBT_T_R2D_C_P<1>	CB242 0.22UF 0201 X5R 6.3V 20% GND_VOID=TRUE	PCIE_TBT_T_D2R_C_P<1> OUT 92 109 92	IN 5 109 PCIE_TBT_T_D2R_C_P<1> CB252 0.22UF 0201 X5R 6.3V 20% GND_VOID=TRUE
109 5 IN PCIE_TBT_T_R2D_C_N<1>	CB243 0.22UF 0201 X5R 6.3V 20% GND_VOID=TRUE	PCIE_TBT_T_D2R_C_N<1> OUT 92 109 92	IN 5 109 PCIE_TBT_T_D2R_C_N<1> CB253 0.22UF 0201 X5R 6.3V 20% GND_VOID=TRUE
109 5 IN PCIE_TBT_T_R2D_C_P<2>	CB244 0.22UF 0201 X5R 6.3V 20% GND_VOID=TRUE	PCIE_TBT_T_D2R_C_P<2> OUT 92 109 92	IN 5 109 PCIE_TBT_T_D2R_C_P<2> CB254 0.22UF 0201 X5R 6.3V 20% GND_VOID=TRUE
109 5 IN PCIE_TBT_T_R2D_C_N<2>	CB245 0.22UF 0201 X5R 6.3V 20% GND_VOID=TRUE	PCIE_TBT_T_D2R_C_N<2> OUT 92 109 92	IN 5 109 PCIE_TBT_T_D2R_C_N<2> CB255 0.22UF 0201 X5R 6.3V 20% GND_VOID=TRUE
109 5 IN PCIE_TBT_T_R2D_C_P<3>	CB246 0.22UF 0201 X5R 6.3V 20% GND_VOID=TRUE	PCIE_TBT_T_D2R_C_P<3> OUT 92 109 92	IN 5 109 PCIE_TBT_T_D2R_C_P<3> CB256 0.22UF 0201 X5R 6.3V 20% GND_VOID=TRUE
109 5 IN PCIE_TBT_T_R2D_C_N<3>	CB247 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_D2R_C_N<3> OUT 92 109 92	IN 5 109 PCIE_TBT_T_D2R_C_N<3> CB257 0.22UF 0201 X5R 6.3V 20%

Place all Caps close to Transmitters
R2D ones close to CPU, D2R ones to TBT.

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C (T) Support

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 112 OF 142
SHEET 94 OF 115

T PRIMARY ACE USB-C PORT CONTROLLER (UPC)

J137 USBC SUPPORTS 5V @ 3A
PP12V IS FOR PROGRAMMING ACE ONLY

PPVBUS_USBC_TA
PP1V8_SLPS2R
1V8 SOURCE FOR ACE 1V8 GPIO
PP3V3_G3H
PP12V_MAIN
ACE LDO CAN DRAW UP TO 5.9 MA WHILE PROGRAMMING OTP
RB389 0 5% 1/16W MF-LF 402
RB399 0 5% 1/16W MF-LF 402
PP3V3_G3H_UPC_TA_R
12V IS TO FLASH THE ACE ONLY
VOLTAGE=3.3V
PPHV_USBC_TA
VOLTAGE=12V
PP5V_G3S_USBC
CB398 1.0UF 10% 25V X6S 0402
CB399 1UF 10% 35V X5R 0402
CB300 10UF 20% 6.3V CERM-X5R 0402-1
CB307 1.0UF 20% 6.3V X5R 0201-1
CB301 1UF 10% 35V X5R 0402
DB300 X3-WLB1608-1 SDM2U40CSP

PP3V3_UPC_TA_LDO VOLTAGE=3.3V
PP3V3_TBT_T_SX
PP1V8_UPC_TA_LDOA VOLTAGE=1.8V
PP1V8_UPC_TA_LDOD VOLTAGE=1.8V
PP1V1_UPC_TA_LDO_BMC VOLTAGE=1.1V
VOUT_3V3 FOR RIDGE, OR FLOAT IF UNUSED
CB308 10UF 20% 6.3V CERM-X5R 0402-1
CB304 2.2UF 20% 4V X5R-CERM 0201
CB305 1.0UF 20% 6.3V X5R 0201-1
CB306 0.47UF 10% 6.3V CERM-X5R 0201

PP_5V0_A11 PP_5V0_B11 PP_5V0_C11 PP_5V0_D11 PP_HV_A6 PP_HV_A7 PP_HV_A8 PP_HV_B7 PP_CABLE H10 VBUS_H11 VBUS_H10 VBUS_J11 VBUS_K11 VIN_3V3 H1 VDDIO B1 LDO_3V3 G1 VOUT_3V3 H2 LDO_1V8AK1 LDO_1V8DA2 LDO_BMC F1

CRITICAL
OMIT_TABLE
UB300
CD3215C00
PBGA
TPS65983
C0 SILICON

MRESET HIGH FORCES F11 RESET LOW
ACTIVE LOW RESET OUTPUT
TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 EVEN IN PRODUCTION
USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR
USE GPIO3 FOR POWER_GATE_EN ON BANSURI DESIGNS
USE GPIO5 FOR PMU RESET AFTER BOOT.
BUSPOWERZ CONTROLS BUS POWER PATH FOR PP_EXT_IT MUST BE < 0.8 V
I2C_ADDR CONTROLS ADDR BITS 3,2,1 J135: GND I2C_ADDR ON PRIMARY ONLY
R_OSC NEEDS NEEDS 0.1% RES
CKPLUS_WAIVE=TERMSHORTED
RB302 0 5% 1/20W MF 0201
RB303 15K 0.1% 1/20W TF-LF 0201
I2C BUS 1 IS TBT / ACES
I2C BUS 2 IS SMC / ACES
Portable: rear connector->TBT ROM, front connector->GND
Desktop: XA_SPI -> TBT ROM, XB_SPI -> GND

TBT_POC_RESET		F11	MRESET	(DIO)	(3V3)
USBC_T_RESET_L		F13	RESET*	(DIO)	(3V3)
UPC_TA_DEBUGUART_TX		B2	GPIO0	(DIO)	
UPC_TA_GPIO1		C2	GPIO1	(DIO)	(1V8)
TBT_T_CIO_PWR_EN	BI	D10	GPIO2	(DIO)	(3V3)
TBT_T_USB_PWR_EN	BI	G11	GPIO3	(DIO)	(3V3)
DP_TA_HPD	OUT	C10	GPIO4	(DIO)	(3V3)
UPC_PMU_RESET	OUT	E10	GPIO5	(DIO)	(1V8)
UPC_T_5V_EN	OUT	G10	GPIO6	(DIO)	(3V3)
UPC_TA_GPIO7		D2	GPIO7	(DIO)	(1V8)
UPC_TA_FAULT_L		H6	GPIO8	(DIO)	(3V3)
PP3V3_UPC_TA_LDO	IN	F10	BUSPOWERZ	(AI)	
UPC_TA_I2C_ADDR		F1	I2C_ADDR	(AIO)	
UPC_TA_R_OSC		G2	R_OSC	(AIO)	
I2C_UPC_TA_DBG_CTL_SCL		E4	DEBUG_CTL1	(DIO)	(DM2)
I2C_UPC_TA_DBG_CTL_SDA		D5	DEBUG_CTL2	(DIO)	
I2C_TBT_T_SDA	BI	D1	I2C_SDA1	(DIO)	
I2C_TBT_T_SCL	BI	D2	I2C_SCL1	(DIO)	(3V3)
I2C_TBT_TA_INT_L	OUT	C3	I2C_IRQ1*	(HIZ)	
I2C_UPC_T_SDA2	BI	A5	I2C_SDA2	(DIO)	
I2C_UPC_T_SCL2	BI	B5	I2C_SCL2	(DIO)	(1V8)
UPC_I2C_INT_L	OUT	B6	I2C_IRQ2*	(HIZ)	
UPC_TA_SPI_CLK	OUT	A3	SPI_CLK	(OO)	
UPC_TA_SPI_MOSI	OUT	B4	SPI_MOSI	(OO)	
UPC_TA_SPI_MISO	IN	A4	SPI_MISO	(OI)	
UPC_TA_SPI_CS_L	OUT	B3	SPI_SSZ	(OO)	
UPC_TA_SWD_DATA	BI	F4	SWD_DATA	(OIO)	
UPC_TA_SWD_CLK	IN	G4	SWD_CLK	(OI)	
UPC_TA_UART_RX	IN	F2	UART_RX	(OI)	
UPC_TA_UART_TX	OUT	E2	UART_TX	(OO)	
TBT_TA_LSTX	IN	L4	LSX_R2P	(OI)	
TBT_TA_LSRX	OUT	K4	LSX_P2R	(OO)	
USB_UPC_TA_FP		L5	USB_RP_P	(AIO)	
USB_UPC_TA_FN		K5	USB_RP_N	(AIO)	
USBC_TA_AUXLSX1	BI	J1	AUX_P	(AIO)	
USBC_TA_AUXLSX2	BI	J2	AUX_N	(AIO)	
SMC_DEBUGPRT_TX	IN	L2	DEBUG1	(AIO)	
SMC_DEBUGPRT_RX	OUT	K2	DEBUG2	(AIO)	
UPC_TA_DBG3		L3	DEBUG3	(AIO)	(1V8)
UPC_TA_DBG4		K3	DEBUG4	(AIO)	

(NOT USED)
PORT MUX
DIGITAL CORE I/O AND CONTROL
HV FET/SENSE
TYPE-C

SS	H7	UPC_TA_SS	
SENSEP	B10		
SENSEN	A10		
HV_GATE1	B9	NC_UPC_TA_HV_GATE1	
HV_GATE2	A9	NC_UPC_TA_HV_GATE2	
C_CC1	L9	USBC_TA_CC1	BI
C_CC2	L10	USBC_TA_CC2	BI
RPD_G1	K9		
RPD_G2	K10		
C_USB_TP	K6	USBC_TA_USB_TOP_P	BI
C_USB_TN	L6	USBC_TA_USB_TOP_N	BI
C_USB_BP	K7	USBC_TA_USB_BOT_P	BI
C_USB_BN	L7	USBC_TA_USB_BOT_N	BI
C_SBU1	K8	USBC_TA_SBU1	BI
C_SBU2	L8	USBC_TA_SBU2	BI
NC	L11		

CB309 0.47UF 10% 6.3V CERM-X5R 0201
CB314 220PF 10% 16V CER-X7R 0201
CB313 220PF 10% 16V CER-X7R 0201

SOFT START RAMP RATE = 9 * ISS / CSS
ISS = 7 UA NOMIAL, 5.5 MA MIN, 8.5 MA MAX
SHORT SENSE INPUTS TO VBUS WHEN UNUSED
FLOAT HV GATE OUTPUTS WHEN UNUSED
C_CC1 AND C_CC2 PINS USED TO DELIVER POWER TO ACTIVE CIRCUITRY INSIDE A CONNECTED CABLE AND OUTPUT USB-PD DATA TO THE CABLE AND CONNECTED DEVICE
J137 HAS NO BATTERY, SO RPD CONNECT TO GND
PORT SIDE USB TOP PAIR
PORT SIDE USB BOTTOM PAIR
PORT SIDE USB SIDEBAND
PIN L11 NC OR GND TO DISSIPATE HEAT

PCH USB2
USB_UPC_TA_P
USB_UPC_TA_N
LB300 90-OHM-0.1A EXCA4CE-
PLACE_NEAR=UB300.L5:5mm
PLACE_NEAR=UB300.K5:5mm
TPB300 TP-P5 A
TPB301 TP-P5 A

PULL RB309 AND RB308 UP TO ACES LDOS FOR 1ST RIDGE'S ACES
PULL THEM DOWN TO GND FOR 2ND RIDGE'S ACES
RB309 1M 5% 1/20W MF 201 I2C_UPC_TA_DBG_CTL_SCL CKPLUS_WAIVE=I2C_PULLUP
RB308 1M 5% 1/20W MF 201 I2C_UPC_TA_DBG_CTL_SDA CKPLUS_WAIVE=I2C_PULLUP
RB305 1M 5% 1/20W MF 201 UPC_TA_UART_RX
RB310 1M 5% 1/20W MF 201 UPC_TA_GPIO1
NOSTUFF

RB356 100K 5% 1/20W MF 201
RB357 100K 5% 1/20W MF 201

GND
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

NOTE:
DEBUG MUX IS CONNECTED TO PRIMARY ACE OF 1ST RIDGE (XA ACE)
R3752-R3755, R3790-R3792 ARE OPTIONAL

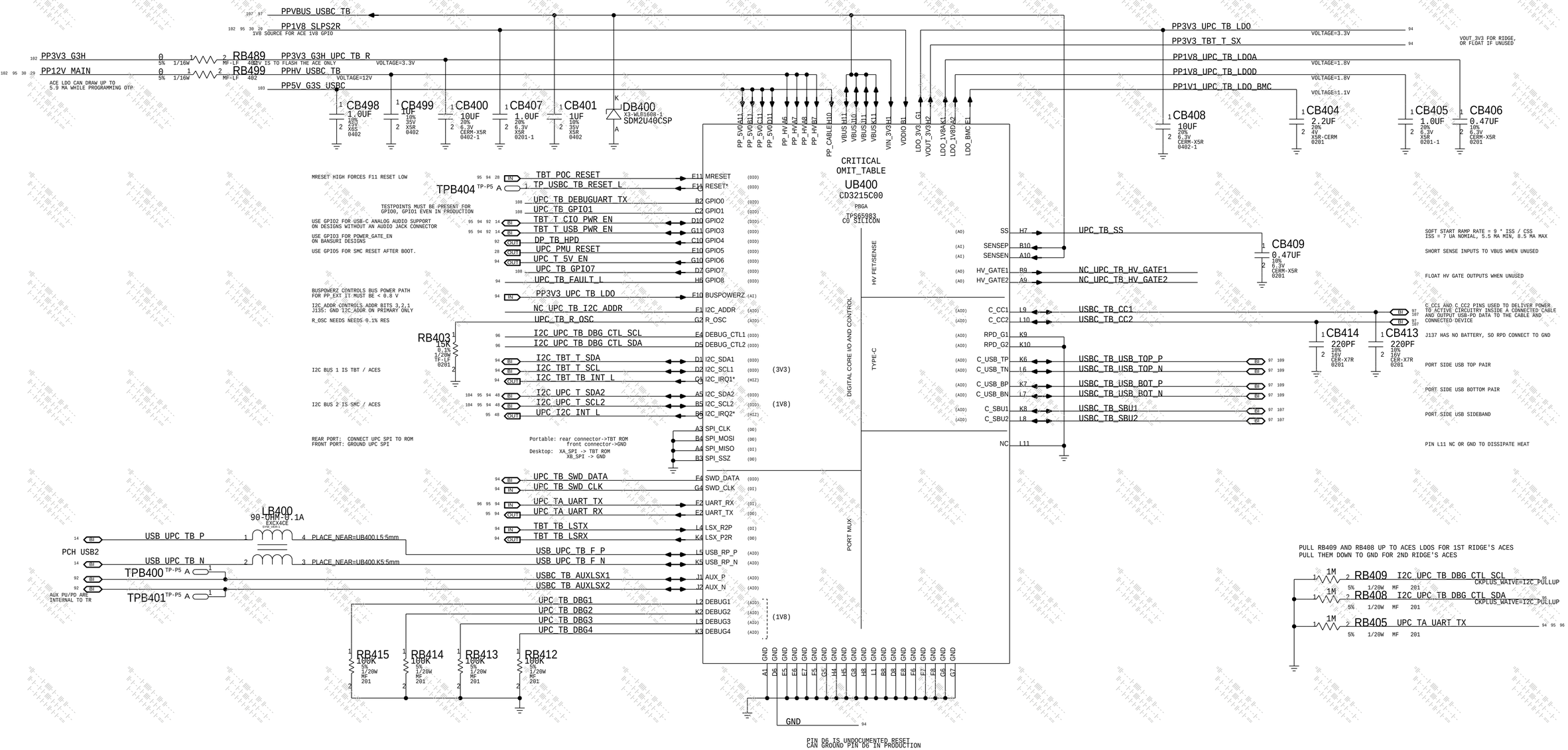
BOM_COST_GROUP=USB-C

04/26/2018 Mary
NOT SYNCED TO OTHER PLATFORMS
PAGE_TITLE=USB-C (T) PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 113 OF 142
SHEET 95 OF 115

T SECONDARY ACE USB-C PORT CONTROLLER (UPC)



NOT SYNCED TO OTHER PLATFORMS

SYNC_DATE=04/26/2018

PAGE TITLE: PAGE_TITLE=USB-C (T) PORT CONTROLLER B

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 114 OF 142

SHEET: 96 OF 115

BOM_COST_GROUP=USB-C

J137 HAS A QUAD-PACK USB-C CONNECTOR
J137 SUPPORTS 5V @ 3A

PPVBUS_USBC_TA
VOLTAGE=5V
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750

NOSTUFF CB504 1UF 10% 25V X5R 402

DZB500 1610 ESDA25P35-1U1M

CB500 0.01UF 10% 25V X5R-CERM 0201
CB501 0.01UF 10% 25V X5R-CERM 0201
CB502 0.01UF 10% 25V X5R-CERM 0201
CB503 0.01UF 10% 25V X5R-CERM 0201
CB510 1UF 10% 25V X5R 402
PLACE VBUS CAPS NEAR EACH VBUS PIN

CB506 0.01UF 10% 25V X5R-CERM 0201
CB507 0.01UF 10% 25V X5R-CERM 0201
CB508 0.01UF 10% 25V X5R-CERM 0201
CB509 0.01UF 10% 25V X5R-CERM 0201
CB511 3PF +/-0.1PF 25V C0G 0201
CB512 12PF 5% 50V C0G-CERM 0201

USBC_TA_D2R_P<2> → RB570 3.01 → USBC_TA_D2R_RC_P<2> → CB570 0.33UF → USBC_TA_D2R_CONN_P<2>
USBC_TA_D2R_N<2> → RB571 3.01 → USBC_TA_D2R_RC_N<2> → CB571 0.33UF → USBC_TA_D2R_CONN_N<2>
USBC_TA_SBU1
USBC_TA_USB_TOP_N
USBC_TA_USB_TOP_P
USBC_TA_CC1
USBC_TA_R2D_C_N<1> → RB572 3.01 → USBC_TA_R2D_RC_N<1> → CB572 0.22UF → USBC_TA_R2D_CONN_N<1>
USBC_TA_R2D_C_P<1> → RB573 3.01 → USBC_TA_R2D_RC_P<1> → CB573 0.22UF → USBC_TA_R2D_CONN_P<1>

CONN C
SYM 3 OF 5
CRITICAL
J3300
RCPT-USBC-QUAD-X1037
F-RT-TH

USBC_TA_D2R_CONN_P<1> → CB578 0.33UF → USBC_TA_D2R_RC_P<1> → RB578 3.01 → USBC_TA_D2R_P<1>
USBC_TA_D2R_CONN_N<1> → CB579 0.33UF → USBC_TA_D2R_RC_N<1> → RB579 3.01 → USBC_TA_D2R_N<1>
USBC_TA_SBU2
USBC_TA_USB_BOT_N
USBC_TA_USB_BOT_P
USBC_TA_CC2
USBC_TA_R2D_CONN_N<2> → CB580 0.22UF → USBC_TA_R2D_RC_N<2> → RB580 3.01 → USBC_TA_R2D_C_N<2>
USBC_TA_R2D_CONN_P<2> → CB581 0.22UF → USBC_TA_R2D_RC_P<2> → RB581 3.01 → USBC_TA_R2D_C_P<2>

DZB507 DZB506 DZB504 DZB505 DZB590 DZB502 DZB503 DZB591 DZB592 DZB508 DZB509 DZB593 DZB513 DZB512 DZB510 DZB511
SESDL2011 DSN2-1H1CKSTNCL
ESD9011 X3DFN2-1H1CKSTNCL
5.5V-6.2PF 0201-1H1CKSTNCL
NO_XNET_CONNECTION=1
GND_VOID

RB501 RB500 RB503 RB502 RB505 RB504 RB507 RB506
220K 201 MF 1/20W 5%

PPVBUS_USBC_TB
VOLTAGE=5V
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750

NOSTUFF CB554 1UF 10% 25V X5R 402

DZB501 1610 ESDA25P35-1U1M

CB550 0.01UF 10% 25V X5R-CERM 0201
CB551 0.01UF 10% 25V X5R-CERM 0201
CB552 0.01UF 10% 25V X5R-CERM 0201
CB553 0.01UF 10% 25V X5R-CERM 0201
CB560 1UF 10% 25V X5R 402
PLACE VBUS CAPS NEAR EACH VBUS PIN

CB556 0.01UF 10% 25V X5R-CERM 0201
CB557 0.01UF 10% 25V X5R-CERM 0201
CB558 0.01UF 10% 25V X5R-CERM 0201
CB559 0.01UF 10% 25V X5R-CERM 0201
CB561 3PF +/-0.1PF 25V C0G 0201
CB562 12PF 5% 50V C0G-CERM 0201

USBC_TB_D2R_P<2> → RB574 3.01 → USBC_TB_D2R_RC_P<2> → CB574 0.33UF → USBC_TB_D2R_CONN_P<2>
USBC_TB_D2R_N<2> → RB575 3.01 → USBC_TB_D2R_RC_N<2> → CB575 0.33UF → USBC_TB_D2R_CONN_N<2>
USBC_TB_SBU1
USBC_TB_USB_TOP_N
USBC_TB_USB_TOP_P
USBC_TB_CC1
USBC_TB_R2D_C_N<1> → RB576 3.01 → USBC_TB_R2D_RC_N<1> → CB576 0.22UF → USBC_TB_R2D_CONN_N<1>
USBC_TB_R2D_C_P<1> → RB577 3.01 → USBC_TB_R2D_RC_P<1> → CB577 0.22UF → USBC_TB_R2D_CONN_P<1>

SYM 4 OF 5
CONN D
CRITICAL
J3300
RCPT-USBC-QUAD-X1037
F-RT-TH

USBC_TB_D2R_CONN_P<1> → CB582 0.33UF → USBC_TB_D2R_RC_P<1> → RB582 3.01 → USBC_TB_D2R_P<1>
USBC_TB_D2R_CONN_N<1> → CB583 0.33UF → USBC_TB_D2R_RC_N<1> → RB583 3.01 → USBC_TB_D2R_N<1>
USBC_TB_SBU2
USBC_TB_USB_BOT_N
USBC_TB_USB_BOT_P
USBC_TB_CC2
USBC_TB_R2D_CONN_N<2> → CB584 0.22UF → USBC_TB_R2D_RC_N<2> → RB584 3.01 → USBC_TB_R2D_C_N<2>
USBC_TB_R2D_CONN_P<2> → CB585 0.22UF → USBC_TB_R2D_RC_P<2> → RB585 3.01 → USBC_TB_R2D_C_P<2>

DZB520 DZB521 DZB524 DZB525 DZB594 DZB522 DZB523 DZB595 DZB596 DZB528 DZB529 DZB597 DZB526 DZB527 DZB530 DZB531
SESDL2011 DSN2-1H1CKSTNCL
ESD9011 X3DFN2-1H1CKSTNCL
5.5V-6.2PF 0201-1H1CKSTNCL
NO_XNET_CONNECTION=1
GND_VOID

RB509 RB508 RB511 RB510 RB513 RB512 RB515 RB514
220K 201 MF 1/20W 5%

CRITICAL
J3300
RCPT-USBC-QUAD-X1037
F-RT-TH
SYM 5 OF 5
USB-C SHIELD
137–172 GND

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C (T) CONNECTORS

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 115 OF 142
SHEET: 97 OF 115

Place Holder

BOM_COST_GROUP=DEBUG

SYNC_MASTER=PVT SYNC_DATE=06/07/2016

PAGE TITLE

EMPTY

Apple Inc.

DRAWING NUMBER 051-02424

SIZE D

REVISION 6.0.0

BRANCH dvt-1

PAGE 116 OF 142

SHEET 98 OF 115

Place Holder

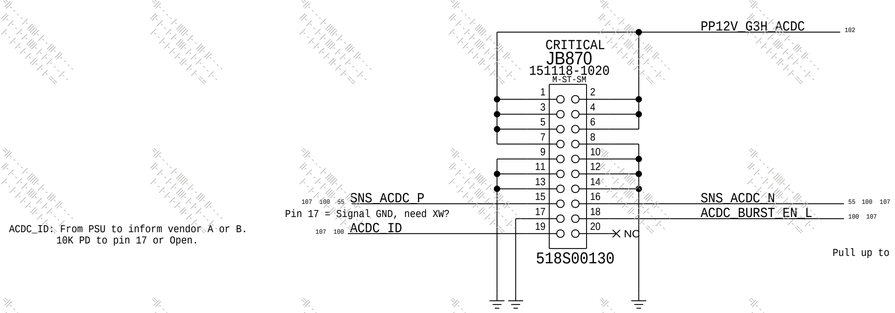
BOM_COST_GROUP=DEBUG

PAGE TITLE
Empty

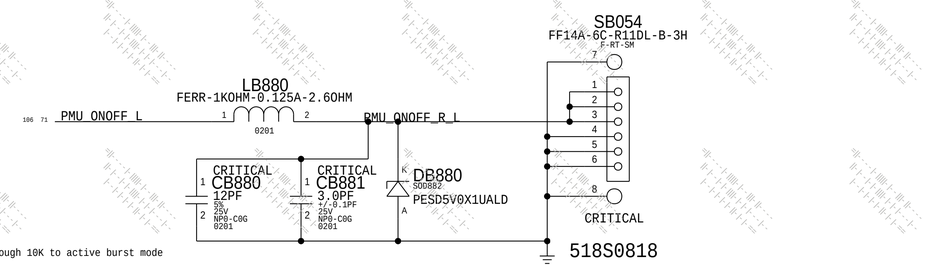
Apple Inc.

DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 117 OF 142
SHEET 99 OF 115

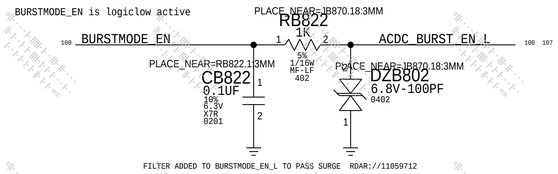
MLB Power button connector

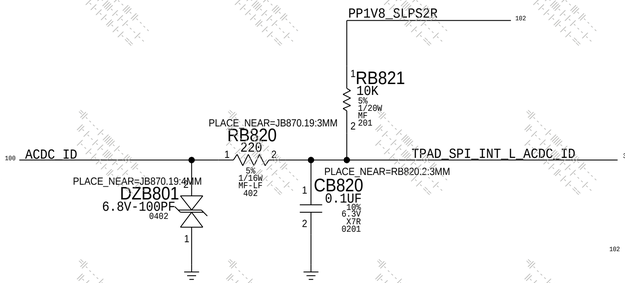


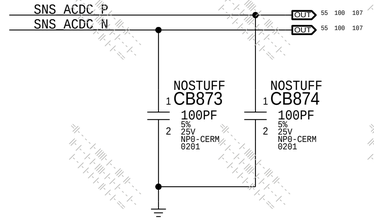
ACDC_ID: From PSU to inform vendor A or B.
10K PD to pin 17 or Open.

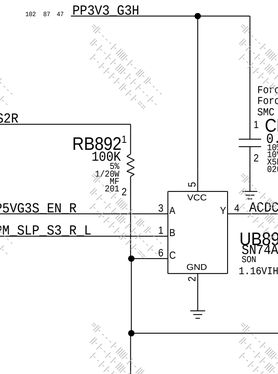


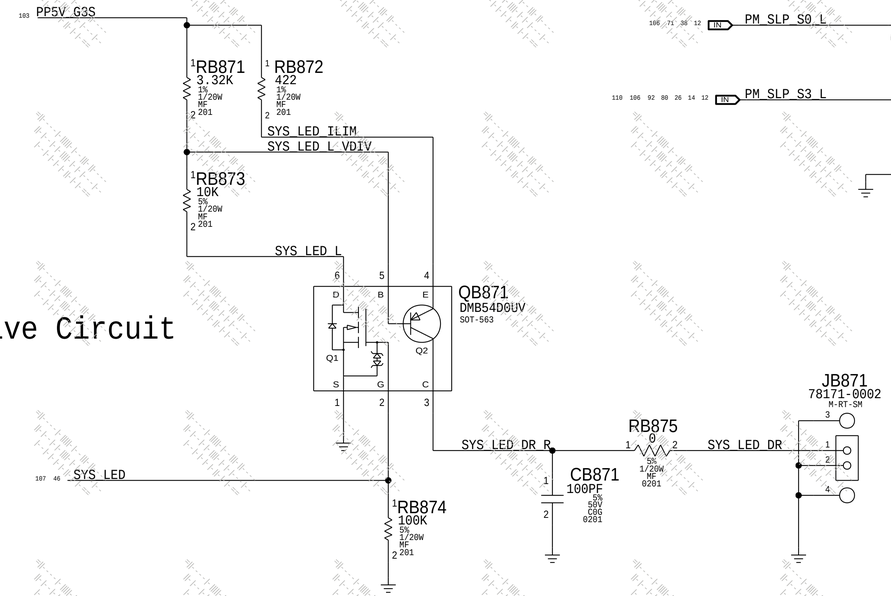
Pull up to 3.3V through 10K to active burst mode

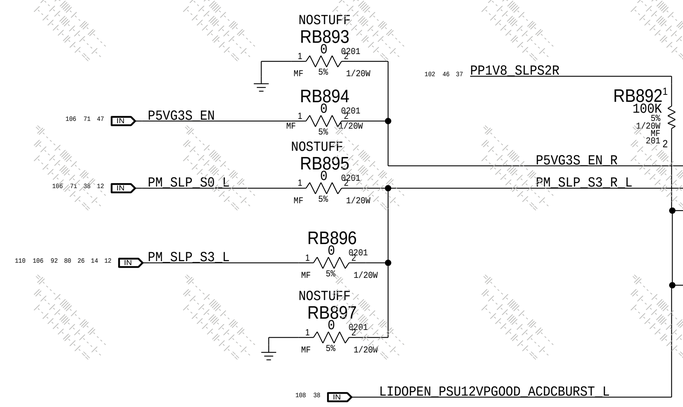












SN74AUP1T97 Logic:

C SMC_CTL	B SLP_L	A G3S_EN	Y OUT	
0	0	0	0	0-Burst mode 1- out of Burst mode
1	0	0	0	
0	1	0	1	Invalid system state
1	1	0	0	(Don't Care)
0	0	1	0	
1	0	1	1	
0	1	1	1	
1	1	1	1	

SIL LED Drive Circuit

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: POWER INPUT FROM AC/DC 1

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 118 OF 142

SHEET: 100 OF 115

12V PBUS Rails

100 PP12V_G3H_ACDC
- PP12V_G3H_ACDC — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=12V, MAKE_BASE=TRUE — 106
- PP12V_G3H_ACDC — 51
- PP12V_G3H_ACDC — 104

51 PP12V_MAIN
- PP12V_MAIN — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=12V, MAKE_BASE=TRUE — 105 106
- PP12V_MAIN — 63
- PP12V_MAIN — 56
- PP12V_MAIN — 53
- PP12V_MAIN — 71
- PP12V_MAIN — 29 30 95 96
- PP12V_MAIN — 51
- PP12V_MAIN — 51
- PP12V_MAIN — 57
- PP12V_MAIN — 47
- PP12V_MAIN — 104
- PP12V_MAIN — 60

CPU High Side Rails

51 PPBUS_HS_CPU
- PPBUS_HS_CPU — MIN_LINE_WIDTH=0.7000, MIN_NECK_WIDTH=0.0650, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PPBUS_HS_CPU — 63 64 65 66 73
- PPBUS_HS_CPU — 67
- PPBUS_HS_CPU — 104 105

3V3_G3H High Side Rails

51 PP12V_G3H_VIN_P3V3_G3H
- PP12V_G3H_VIN_P3V3_G3H — MIN_LINE_WIDTH=0.1010, MIN_NECK_WIDTH=0.0650, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PP12V_G3H_VIN_P3V3_G3H — 68
- PP12V_G3H_VIN_P3V3_G3H — 104 105

5V_G3S High Side Rails

51 PP12V_G3H_VIN_P5V_G3S
- PP12V_G3H_VIN_P5V_G3S — MIN_LINE_WIDTH=0.1010, MIN_NECK_WIDTH=0.0650, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PP12V_G3H_VIN_P5V_G3S — 68
- PP12V_G3H_VIN_P5V_G3S — 104 105

12V to NAND 2V7 VR Rails

53 PPVIN_G3H_P2V7
- PPVIN_G3H_P2V7 — MIN_LINE_WIDTH=0.0800, MIN_NECK_WIDTH=0.0720, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PPVIN_G3H_P2V7 — 79

12V to ENET VR Rails

56 PPVIN_ENET_P0V85
- PPVIN_ENET_P0V85 — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PPVIN_ENET_P0V85 — 87
- PPVIN_ENET_P0V85 — 104

3V3 G3H Rails

68 PP3V3_G3H
- PP3V3_G3H — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 105 106
- PP3V3_G3H — 54
- PP3V3_G3H — 102
- PP3V3_G3H — 54
- PP3V3_G3H — 56
- PP3V3_G3H — 72
- PP3V3_G3H — 72
- PP3V3_G3H — 102
- PP3V3_G3H — 29
- PP3V3_G3H — 30
- PP3V3_G3H — 95
- PP3V3_G3H — 96
- PP3V3_G3H — 47 87 100
- PP3V3_G3H — 53
- PP3V3_G3H — 110
- PP3V3_G3H — 28
- PP3V3_G3H — 67
- PP3V3_G3H — 19
- PP3V3_G3H — 73
- PP3V3_G3H — 70
- PP3V3_G3H — 113
- PP3V3_G3H — 70
- PP3V3_G3H — 113
- PP3V3_G3H — 48
- PP3V3_G3H — 72

3V3_G3H SSD Rail

53 PP3V3_G3H_SSD
- PP3V3_G3H_SSD — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 106
- PP3V3_G3H_SSD — 79 105
- PP3V3_G3H_SSD — 104

CPU Rails

64 PPVCC_S0_CPU_REG
- PPVCC_S0_CPU_REG — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.52V — 106
- PPVCC_S0_CPU_REG — 6 8 56
- PPVCC_S0_CPU_REG — 10
- PPVCC_S0_CPU_REG — 104 105

66 PPVCCSA_S0_CPU_REG
- PPVCCSA_S0_CPU_REG — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.52V — 106
- PPVCCSA_S0_CPU_REG — 8 56
- PPVCCSA_S0_CPU_REG — 11

65 PPVCCGT_S0_CPU_REG
- PPVCCGT_S0_CPU_REG — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.52V — 106
- PPVCCGT_S0_CPU_REG — 8 56
- PPVCCGT_S0_CPU_REG — 10
- PPVCCGT_S0_CPU_REG — 104

CPU VCCIO Rails

54 PPVCCIO_S0_CPU
- PPVCCIO_S0_CPU — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=0.95V — 106
- PPVCCIO_S0_CPU — 5 8
- PPVCCIO_S0_CPU — 11
- PPVCCIO_S0_CPU — 104 105

BUCK0 VDD SoC CPU

69 PPVDDCPU_AWAKE_SOC
- PPVDDCPU_AWAKE_SOC — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.06V — 106
- PPVDDCPU_AWAKE_SOC — 41 105 112

BUCK1 VDD SoC CPU SRAM

69 PPVDDCPUSRAM_AWAKE
- PPVDDCPUSRAM_AWAKE — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.06V — 106
- PPVDDCPUSRAM_AWAKE — 41

BUCK2 SoC VDD_SOC

69 PP0V82_SLPDDR
- PP0V82_SLPDDR — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=.82V — 106
- PP0V82_SLPDDR — 41 105 112

V3P3_SW1 USB

70 PP3V3_AWAKE
- PP3V3_AWAKE — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=3.3V — 106
- PP3V3_AWAKE — 43

PMIC LDO2 PCIE_REFBUF/PLL

70 PP1V2_AWAKE
- PP1V2_AWAKE — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.2V — 106
- PP1V2_AWAKE — 43
- PP1V2_AWAKE — 43
- PP1V2_AWAKE — 43
- PP1V2_AWAKE — 43

PMIC LDO0 - VDD_LOW

70 PP0V8_SLPS2R
- PP0V8_SLPS2R — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=0.8V, MAKE_BASE=TRUE — 106
- PP0V8_SLPS2R — 42

RTC Rails (PMIC LDO 1)

19 PP3V0_G3H_RTC
- PP3V0_G3H_RTC — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3V, MAKE_BASE=TRUE — 106
- PP3V0_G3H_RTC — 12 16 17

Calpe 3V3 VDD Rail

54 PP3V3_G3H_PMU
- PP3V3_G3H_PMU — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 107
- PP3V3_G3H_PMU — 69
- PP3V3_G3H_PMU — 70
- PP3V3_G3H_PMU — 70
- PP3V3_G3H_PMU — 71
- PP3V3_G3H_PMU — 70

3V3_G3H ENET Rail

56 PP3V3_G3H_ENET
- PP3V3_G3H_ENET — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 85 106
- PP3V3_G3H_ENET — 72 86 87

3V3 ENET Rail(Pass FET)

105 84 83 82 81 80 72 19 PP3V3_ENET
- PP3V3_ENET — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 104

BUCK3 AOP/SMC/VDD1(1V8)

69 PP1V8_SLPS2R
- PP1V8_SLPS2R — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.8V, MAKE_BASE=TRUE — 84 106
- PP1V8_SLPS2R — 43
- PP1V8_SLPS2R — 43
- PP1V8_SLPS2R — 43
- PP1V8_SLPS2R — 43
- PP1V8_SLPS2R — 113
- PP1V8_SLPS2R — 69 — Buck3_SW input, 1V8 G3S input
- PP1V8_SLPS2R — 70
- PP1V8_SLPS2R — 71
- PP1V8_SLPS2R — 48
- PP1V8_SLPS2R — 48
- PP1V8_SLPS2R — 48
- PP1V8_SLPS2R — 45
- PP1V8_SLPS2R — 45
- PP1V8_SLPS2R — 37 46 100
- PP1V8_SLPS2R — 29 30 95 96 — 1V8_SLPS2R MISC
- PP1V8_SLPS2R — 110
- PP1V8_SLPS2R — 100

BUCK3_SW1(1V8)

69 PP1V8_AWAKE
- PP1V8_AWAKE — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.8V, MAKE_BASE=TRUE — 106
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 71
- PP1V8_AWAKE — 45
- PP1V8_AWAKE — 28 40 45 46 — 1V8_AWAKE MISC
- PP1V8_AWAKE — 45
- PP1V8_AWAKE — 113
- PP1V8_AWAKE — 104

BUCK4 SDRAM VDD2 (1V1)

69 PP1V1_SLPS2R
- PP1V1_SLPS2R — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.1V, MAKE_BASE=TRUE — 106
- PP1V1_SLPS2R — 42
- PP1V1_SLPS2R — 43
- PP1V1_SLPS2R — 70 — 0V8 LDO0 input
- PP1V1_SLPS2R — 69 — Buck4_SW input
- PP1V1_SLPS2R — 70 — 1V1 SLPDDR SW input

1V1 SLPDDR SOC VDDIO DDR (SoC Transition State)

70 PP1V1_SLPDDR
Source from 1V1_SLPS2R
EN by PMIC.GPIO
- PP1V1_SLPDDR — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.1V, MAKE_BASE=TRUE — 106
- PP1V1_SLPDDR — 42 105
- PP1V1_SLPDDR — 37
- PP1V1_SLPDDR — 42
- PP1V1_SLPDDR — 43

BUCK5 VDD_FIXED

69 PP0V9_SLPDDR
- PP0V9_SLPDDR — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=0.9V, MAKE_BASE=TRUE — 106
- PP0V9_SLPDDR — 42 105
- PP0V9_SLPDDR — 42
- PP0V9_SLPDDR — 42
- PP0V9_SLPDDR — 42
- PP0V9_SLPDDR — 42

LDO1 for RTC

70 19 PPVRTC_G3_PCH_REG_R
- PPVRTC_G3_PCH_REG_R — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.0V, MAKE_BASE=TRUE

1.1V PRIM FOR XTAL

17 16 PP1V_PRIM_PCH_VCCAXTAL_F
- PP1V_PRIM_PCH_VCCAXTAL_F — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.8V, MAKE_BASE=TRUE

1.1V PRIM FOR PLL

17 16 PP1V_PRIM_PCH_VCCAPLL_F
- PP1V_PRIM_PCH_VCCAPLL_F — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.1V, MAKE_BASE=TRUE

1.1V PRIM FOR MPHY_PLL

17 16 PP1V_PRIM_PCH_VCCAMPHYPLL_F
- PP1V_PRIM_PCH_VCCAMPHYPLL_F — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1V, MAKE_BASE=TRUE

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: Power Aliases - 1

Apple Inc.

DRAWING NUMBER: 051-02424 — SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 120 OF 142
SHEET: 102 OF 115

1V S5 Rails

69 PP1V_PRIM
MIN_LINE_WIDTH=0.0700
MIN_NECK_WIDTH=0.0650
VOLTAGE=1.0V
MAKE_BASE=TRUE

PP1V_PRIM 106
PP1V_PRIM 69
PP1V_PRIM 16 17
PP1V_PRIM 16
PP1V_PRIM 16
PP1V_PRIM 16
PP1V_PRIM 16 17
PP1V_PRIM 17
PP1V_PRIM 17
PP1V_PRIM 17
PP1V_PRIM 18
PP1V_PRIM 112
PP1V_PRIM 47
PP1V_PRIM 16
PP1V_PRIM 104

These 3x rails need filter

1V S3 Rails

69 PP1V_S3
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.0V
MAKE_BASE=TRUE

PP1V_S3 106
PP1V_S3 8 11 45
PP1V_S3 8 11
PP1V_S3 71
PP1V_S3 63
PP1V_S3 6 13 20
PP1V_S3 45

1V2 S5 Rails

69 PP1V2_PRIM
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_PRIM 90

1V2 S3 Rails

67 PP1V2_S3
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S3 106 107
PP1V2_S3 23
PP1V2_S3 24
PP1V2_S3 22
PP1V2_S3 67
PP1V2_S3 12
PP1V2_S3 105
PP1V2_S3 8
PP1V2_S3 11
PP1V2_S3 72

72 PP1V2_S0SW
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S0SW 106
PP1V2_S0SW 8 11

0V6 Rails

23 22 PP0V6_S3_MEM_VREFCAA
MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0.6V
MAKE_BASE=TRUE

PP0V6_S3_MEM_VREFCAA

24 22 PP0V6_S3_MEM_VREFCAB
MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0.6V
MAKE_BASE=TRUE

PP0V6_S3_MEM_VREFCAB

2V5 VPP Rails

67 PP2V5_S3
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=2.5V
MAKE_BASE=TRUE

PP2V5_S3 107
PP2V5_S3 52

52 PP2V5_S3_VPP
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=2.5V
MAKE_BASE=TRUE

PP2V5_S3_VPP 107
PP2V5_S3_VPP 23
PP2V5_S3_VPP 24
PP2V5_S3_VPP 23 50
PP2V5_S3_VPP 24
PP2V5_S3_VPP 47

VTT Rails

67 PPDDRVTT_S0_MEM
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.2V
MAKE_BASE=TRUE

PPDDRVTT_S0_MEM 106 107
PPDDRVTT_S0_MEM 23
PPDDRVTT_S0_MEM 24

Digital Ground

GND
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=0V

1V8 G3S Rails

69 PP1V8_G3S
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_G3S 59 106
PP1V8_G3S 34 35 107
PP1V8_G3S 47 57
PP1V8_G3S 68
PP1V8_G3S 60
PP1V8_G3S 49

1V8 S5 Rails

69 PP1V8_S5
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_S5 106
PP1V8_S5 47
PP1V8_S5 12 13 15 16 17 50
PP1V8_S5 12 16 17 38
PP1V8_S5 16
PP1V8_S5 13 16 17
PP1V8_S5 18
PP1V8_S5 35 50 71
PP1V8_S5 45
PP1V8_S5 16 17
PP1V8_S5 15 72
PP1V8_S5 90 91
PP1V8_S5 55
PP1V8_S5 55
PP1V8_S5 47 63 67 73
PP1V8_S5 20
PP1V8_S5 113
PP1V8_S5 45
PP1V8_S5 45

5V G3S Rails

68 PP5V_G3S
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_G3S 87 106
PP5V_G3S 56
PP5V_G3S 56
PP5V_G3S 88
PP5V_G3S 63
PP5V_G3S 64 65 66 73
PP5V_G3S 67
PP5V_G3S 113
PP5V_G3S 104 105
PP5V_G3S 100

Modified for HDMI

USBC 5V Rails

56 PP5V_G3S_USBC
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_G3S_USBC 28 94 107
PP5V_G3S_USBC 29
PP5V_G3S_USBC 30
PP5V_G3S_USBC 95
PP5V_G3S_USBC 96
PP5V_G3S_USBC 104

USBA 5V Rails

56 PP5V_G3S_USBA
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_G3S_USBA 107
PP5V_G3S_USBA 62

3V3 G3S Rails

72 PP3V3_G3S
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3S 59 86 106
PP3V3_G3S 56
PP3V3_G3S 84
PP3V3_G3S 51
PP3V3_G3S 52
PP3V3_G3S 52 53 54 56
PP3V3_G3S 51 56

Sensor Rails

3V3 G3S Harpoon Rails

56 PP3V3_G3S_WLANBT
MIN_LINE_WIDTH=0.1010
MIN_NECK_WIDTH=0.0650
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3S_WLANBT 35 107
PP3V3_G3S_WLANBT 34

3V3 S5 Rails

70 PP3V3_S5
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3
MAKE_BASE=TRUE

PP3V3_S5 82 106
PP3V3_S5 16 17 20
PP3V3_S5 12 16 17 71
PP3V3_S5 15 16 17
PP3V3_S5 14 16 17
PP3V3_S5 13 15 16 17
PP3V3_S5 12 15 16 17
PP3V3_S5 72
PP3V3_S5 45
PP3V3_S5 72
PP3V3_S5 88 90
PP3V3_S5 20
PP3V3_S5 21
PP3V3_S5 113

GPPD is 1V8?

HDMI only 32mA?

TBT 3V3 Rails

54 PP3V3_S0_TBT
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
MAKE_BASE=TRUE
VOLTAGE=3.3V

PP3V3_S0_TBT 107
PP3V3_S0_TBT 72
PP3V3_S0_TBT 72

TBT X 3V3 Rails

72 PP3V3_S0SW_TBT_X
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
MAKE_BASE=TRUE
VOLTAGE=3.3V

PP3V3_S0SW_TBT_X 106
PP3V3_S0SW_TBT_X 27

TBT T 3V3 Rails

72 PP3V3_S0SW_TBT_T
MIN_LINE_WIDTH=0.1010
MIN_NECK_WIDTH=0.0650
MAKE_BASE=TRUE
VOLTAGE=3.3V

PP3V3_S0SW_TBT_T 93

VCCSTG From Calpe HIO_SW

70 PP1V_S0SW
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.0V
MAKE_BASE=TRUE

PP1V_S0SW 106
PP1V_S0SW 6 8 11 18

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=Mary	SYNC_DATE=04/26/2018
PAGE TITLE	Power Aliases - 2
Apple Inc.	DRAWING NUMBER 051-02424 · SIZE D
	REVISION 6.0.0
	BRANCH dvt-1
	PAGE 121 OF 142
	SHEET 103 OF 115

Misc Alias

71	NC_GPU_THRMTRIP	NC_GPU_THRMTRIP	MAKE_BASE=TRUE
48 30 29 28	I2C_UPC_X_SDA2	I2C_UPC_X_SDA2	MAKE_BASE=TRUE
48 30 29 28	I2C_UPC_X_SCL2	I2C_UPC_X_SCL2	MAKE_BASE=TRUE
96 95 94 48	I2C_UPC_T_SDA2	I2C_UPC_T_SDA2	MAKE_BASE=TRUE
96 95 94 48	I2C_UPC_T_SCL2	I2C_UPC_T_SCL2	MAKE_BASE=TRUE

TOP Side

105 104 102 PPBUS_HS_CPU
CRITICAL CC203 12PF 5% 25V NP0-C0G 0201
CRITICAL CC202 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC201 12PF 5% 25V NP0-C0G 0201
CRITICAL CC200 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC231 12PF 5% 25V NP0-C0G 0201
CRITICAL CC230 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC229 12PF 5% 25V NP0-C0G 0201
CRITICAL CC228 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC227 12PF 5% 25V NP0-C0G 0201
CRITICAL CC226 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC225 12PF 5% 25V NP0-C0G 0201
CRITICAL CC224 3.0PF +/-0.1PF 25V NP0-C0G 0201

77 78 75 74 112 106 105 79 78 PP1V8_SSD0
CRITICAL CC205 12PF 5% 25V NP0-C0G 0201
CRITICAL CC204 3.0PF +/-0.1PF 25V NP0-C0G 0201

105 104 102 PP12V_G3H_VIN_P5V_G3S
CRITICAL CC2A5 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2A4 3.0PF +/-0.1PF 25V NP0-C0G 0201

102 PP3V3_G3H_SSD
CRITICAL CC207 12PF 5% 25V NP0-C0G 0201
CRITICAL CC206 3.0PF +/-0.1PF 25V NP0-C0G 0201

106 104 87 83 PP0V85_ENET
CRITICAL CC289 12PF 5% 25V NP0-C0G 0201
CRITICAL CC288 3.0PF +/-0.1PF 25V NP0-C0G 0201

104 102 PP12V_G3H_ACDC
CRITICAL CC215 12PF 5% 25V NP0-C0G 0201
CRITICAL CC214 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC213 12PF 5% 25V NP0-C0G 0201
CRITICAL CC212 3.0PF +/-0.1PF 25V NP0-C0G 0201

104 102 PP12V_G3H_MAIN
CRITICAL CC223 12PF 5% 25V NP0-C0G 0201
CRITICAL CC222 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC221 12PF 5% 25V NP0-C0G 0201
CRITICAL CC220 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC219 12PF 5% 25V NP0-C0G 0201
CRITICAL CC218 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC217 12PF 5% 25V NP0-C0G 0201
CRITICAL CC216 3.0PF +/-0.1PF 25V NP0-C0G 0201

105 104 102 PPVCC_S0_CPU_REG
CRITICAL CC235 12PF 5% 25V NP0-C0G 0201
CRITICAL CC234 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC233 12PF 5% 25V NP0-C0G 0201
CRITICAL CC232 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC247 12PF 5% 25V NP0-C0G 0201
CRITICAL CC246 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC245 12PF 5% 25V NP0-C0G 0201
CRITICAL CC244 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC243 12PF 5% 25V NP0-C0G 0201
CRITICAL CC242 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC241 12PF 5% 25V NP0-C0G 0201
CRITICAL CC240 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC239 12PF 5% 25V NP0-C0G 0201
CRITICAL CC238 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC237 12PF 5% 25V NP0-C0G 0201
CRITICAL CC236 3.0PF +/-0.1PF 25V NP0-C0G 0201

104 102 PPVCCGT_S0_CPU_REG
CRITICAL CC262 12PF 5% 25V NP0-C0G 0201
CRITICAL CC257 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC256 12PF 5% 25V NP0-C0G 0201
CRITICAL CC255 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC254 12PF 5% 25V NP0-C0G 0201
CRITICAL CC250 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC249 12PF 5% 25V NP0-C0G 0201
CRITICAL CC248 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC263 12PF 5% 25V NP0-C0G 0201
CRITICAL CC261 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC260 12PF 5% 25V NP0-C0G 0201
CRITICAL CC259 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC258 12PF 5% 25V NP0-C0G 0201
CRITICAL CC253 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC252 12PF 5% 25V NP0-C0G 0201
CRITICAL CC251 3.0PF +/-0.1PF 25V NP0-C0G 0201

102 PP1V8_AWAKE
CRITICAL CC269 12PF 5% 25V NP0-C0G 0201
CRITICAL CC268 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC267 12PF 5% 25V NP0-C0G 0201
CRITICAL CC266 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC265 12PF 5% 25V NP0-C0G 0201
CRITICAL CC264 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC275 12PF 5% 25V NP0-C0G 0201
CRITICAL CC274 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC273 12PF 5% 25V NP0-C0G 0201
CRITICAL CC272 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC271 12PF 5% 25V NP0-C0G 0201
CRITICAL CC270 3.0PF +/-0.1PF 25V NP0-C0G 0201

102 PP3V3_ENET
CRITICAL CC281 12PF 5% 25V NP0-C0G 0201
CRITICAL CC280 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC279 12PF 5% 25V NP0-C0G 0201
CRITICAL CC278 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC277 12PF 5% 25V NP0-C0G 0201
CRITICAL CC276 3.0PF +/-0.1PF 25V NP0-C0G 0201

102 PPVIN_ENET_P0V85
CRITICAL CC287 12PF 5% 25V NP0-C0G 0201
CRITICAL CC286 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC285 12PF 5% 25V NP0-C0G 0201
CRITICAL CC284 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC283 12PF 5% 25V NP0-C0G 0201
CRITICAL CC282 3.0PF +/-0.1PF 25V NP0-C0G 0201

103 PP5V_G3S_USBC
CRITICAL CC297 12PF 5% 25V NP0-C0G 0201
CRITICAL CC296 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC295 12PF 5% 25V NP0-C0G 0201
CRITICAL CC294 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC293 12PF 5% 25V NP0-C0G 0201
CRITICAL CC292 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC291 12PF 5% 25V NP0-C0G 0201
CRITICAL CC290 3.0PF +/-0.1PF 25V NP0-C0G 0201

105 102 PP12V_G3H_VIN_P3V3_G3H
CRITICAL CC2A3 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2A2 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC2A1 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2A0 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC299 12PF 5% 25V NP0-C0G 0201
CRITICAL CC298 3.0PF +/-0.1PF 25V NP0-C0G 0201

BOTTOM Side

105 102 PPVCCIO_S0_CPU
CRITICAL CC2A7 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2A6 3.0PF +/-0.1PF 25V NP0-C0G 0201

104 102 105 PPBUS_HS_CPU
CRITICAL CC2B3 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2B2 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC2B1 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2B0 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC2A9 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2A8 3.0PF +/-0.1PF 25V NP0-C0G 0201

104 102 PPVCCGT_S0_CPU_REG
CRITICAL CC2B7 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2B6 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC2B5 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2B4 3.0PF +/-0.1PF 25V NP0-C0G 0201

104 102 105 PPVCC_S0_CPU_REG
CRITICAL CC2C3 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2C2 3.0PF +/-0.1PF 25V NP0-C0G 0203
CRITICAL CC2C1 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2C0 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC2B9 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2B8 3.0PF +/-0.1PF 25V NP0-C0G 0201

103 PP1V_PRIM
CRITICAL CC2C9 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2C8 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC2C7 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2C6 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC2C5 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2C4 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC2D3 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2D2 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CC2D1 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2D0 3.0PF +/-0.1PF 25V NP0-C0G 0201

104 102 PP12V_G3H_ACDC
CRITICAL CC2D5 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2D4 3.0PF +/-0.1PF 25V NP0-C0G 0201

104 102 PP12V_MAIN
CRITICAL CC2D7 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2D6 3.0PF +/-0.1PF 25V NP0-C0G 0201

104 87 83 106 PP0V85_ENET
CRITICAL CC2D8 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2D9 3.0PF +/-0.1PF 25V NP0-C0G 0201

105 103 PP5V_G3S
CRITICAL CC2E0 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2E1 3.0PF +/-0.1PF 25V NP0-C0G 0201

105 104 102 PP12V_G3H_VIN_P5V_G3S
CRITICAL CC2E3 12PF 5% 25V NP0-C0G 0201
CRITICAL CC2E2 3.0PF +/-0.1PF 25V NP0-C0G 0201

BOM_COST_GROUP=DESENSE

PAGE TITLE: Desense CAPs 1

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 122 OF 142
SHEET: 104 OF 115

PPVDDCPU_AWAKE_SOC
CC303 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC302 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF

PP1V1_SLPDDR
CC331 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC332 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF

PP1V8_SSD0
PLACE_NEAR=U8600.P9:3MM PLACE_NEAR=U8700.P9:3MM PLACE_NEAR=U8800.P9:3MM PLACE_NEAR=U8900.P9:3MM
PLACE_NEAR=U8600.T5:3MM PLACE_NEAR=U8700.T5:3MM PLACE_NEAR=U8800.T5:3MM PLACE_NEAR=U8900.T5:3MM
CC323 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC322 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC321 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC320 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC319 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC318 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC317 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC316 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PPVCCIO_S0_CPU_REG
CC3B7 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3B6 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC3B5 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3B4 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP0V82_SLPDDR
CC301 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC300 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF

PP0V9_SLPDDR
PLACE_NEAR=C4410:3MM
CC329 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC328 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF
PLACE_NEAR=C4411:3MM

PP2V7_NAND_SSD0
PLACE_NEAR=U8600.R2:3MM PLACE_NEAR=U8700.R2:3MM PLACE_NEAR=U8800.R2:3MM PLACE_NEAR=U8900.P2:3MM
PLACE_NEAR=U8600.G4:3MM PLACE_NEAR=U8700.G4:3MM PLACE_NEAR=U8800.G4:3MM PLACE_NEAR=U8900.G4:3MM
CC397 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC396 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC395 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC394 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC393 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC392 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC391 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC390 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP12V_G3H_VIN_P5V_G3S
CC349 12PF 5% 50V C0G-CERM 0201 NOSTUFF
CC348 3PF +/-0.1PF 100V C0G 0201 NOSTUFF
CC3A9 12PF 5% 50V C0G-CERM 0201 NOSTUFF
CC3A8 3PF +/-0.1PF 100V C0G 0201 NOSTUFF

PP1V8_SSD0_S4E0_AVDD18_PLL
PLACE_NEAR=U8600.L2:3MM
CC305 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC304 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP1V8_SSD0_S4E1_AVDD18_PLL
PLACE_NEAR=U8700.L2:3MM
CC3A5 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3A4 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP0V9_SSD0
PLACE_NEAR=U8600.R4:3MM PLACE_NEAR=U8600.R8:3MM PLACE_NEAR=U8600.J8:3MM
PLACE_NEAR=U8600.R4:5MM PLACE_NEAR=U8600.G8:3MM
CC369 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC368 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC367 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC366 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC365 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC364 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP1V2_S3
CC3D3 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC3D2 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3D1 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3D0 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP1V8_SSD0_S4E2_AVDD18_PLL
PLACE_NEAR=U8800.L2:3MM
CC307 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC306 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP1V8_SSD0_S4E3_AVDD18_PLL
PLACE_NEAR=U8900.L2:3MM
CC389 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC388 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PLACE_NEAR=U8700.R4:3MM PLACE_NEAR=U8700.R8:3MM PLACE_NEAR=U8700.J8:3MM
PLACE_NEAR=U8700.R4:5MM PLACE_NEAR=U8700.G8:3MM PLACE_NEAR=U8700.J6:3MM
CC375 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC374 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC373 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC372 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC371 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC370 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP5V_G3S
CC3C1 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3C0 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC3B9 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3B8 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP1V8_SSD0_S4E0_PCI_AVDD_H
PLACE_NEAR=U8600.J6:3MM
CC335 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC334 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP1V8_SSD0_S4E1_PCI_AVDD_H
PLACE_NEAR=U8700.J6:3MM
CC333 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC308 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PLACE_NEAR=U8800.R4:3MM PLACE_NEAR=U8800.R8:3MM PLACE_NEAR=U8800.J8:3MM
PLACE_NEAR=U8800.R4:5MM PLACE_NEAR=U8800.G8:3MM PLACE_NEAR=U8800.J6:3MM
CC3A3 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3A2 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC3A1 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3A0 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC399 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC398 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP3V3_G3H
PLACE_NEAR=L7610:3MM PLACE_NEAR=L7610:3MM
CC3C9 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3C8 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC3C7 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3C6 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC3C5 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3C4 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
PLACE_NEAR=L7610:3MM
PLACE_NEAR=L7610:3MM PLACE_NEAR=L7610:3MM PLACE_NEAR=L7610:3MM
NOSTUFF

PP1V8_SSD0_S4E2_PCI_AVDD_H
PLACE_NEAR=U8800.J6:3MM
CC347 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC346 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP1V8_SSD0_S4E3_PCI_AVDD_H
PLACE_NEAR=U8900.J6:3MM
CC345 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC344 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PLACE_NEAR=U8900.R4:3MM PLACE_NEAR=U8900.R8:3MM PLACE_NEAR=U8900.J8:3MM
PLACE_NEAR=U8900.R4:5MM PLACE_NEAR=U8900.G8:3MM PLACE_NEAR=U8900.J6:3MM
CC381 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC380 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC379 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC378 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
CC377 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC376 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP3V3_G3H_SSD
PLACE_NEAR=U9000.B4:3MM
PLACE_NEAR=U9000.B4:3MM
CC315 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC314 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP0V9_SSD0
PLACE_NEAR=C9025:3MM
CC313 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC312 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
PLACE_NEAR=C9025:3MM
NOSTUFF

PP1V8_SSD0
PLACE_NEAR=C9035:3MM
CC327 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC326 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
PLACE_NEAR=C9035:3MM
NOSTUFF

PPBUS_HS_CPU
PLACE_NEAR=R5420:3MM
CC354 12PF 5% 50V C0G-CERM 0201 NOSTUFF
CC350 3PF +/-0.1PF 100V C0G 0201 NOSTUFF
PLACE_NEAR=R5420:3MM
NOSTUFF

PPVCC_S0_CPU_REG
CC3C3 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3C2 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
NOSTUFF

PP12V_G3H_VIN_P3V3_G3H
PLACE_NEAR=R5420:3MM
CC3B3 12PF 5% 50V C0G-CERM 0201 NOSTUFF
CC3B2 3PF +/-0.1PF 100V C0G 0201 NOSTUFF
PLACE_NEAR=R5420:3MM
NOSTUFF

PP3V3_ENET
PLACE_NEAR=U9300.14:3MM
PLACE_NEAR=U9300.14:3MM
CC343 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC342 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF

ENET_XTALVDDH
PLACE_NEAR=U9300.17:3MM
PLACE_NEAR=U9300.17:3MM
CC341 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC340 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF

PPHV_USBC_XA
PLACE_NEAR=U3100:3MM
CC3E1 12PF 5% 25V C0G-CERM 0201 NOSTUFF
CC3E2 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
PLACE_NEAR=U3100:3MM
NOSTUFF

PPHV_USBC_XB
PLACE_NEAR=U3200:3MM
CC3D8 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3D7 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
PLACE_NEAR=U3200:3MM
NOSTUFF

PP3V3_ENET_PHY_BIASVDDH
PLACE_NEAR=U9300.37:3MM
PLACE_NEAR=U9300.37:3MM
CC339 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC338 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF

PP3V3_ENET_PHY_AVDDH
PLACE_NEAR=U9300.42:3MM
PLACE_NEAR=U9300.42:3MM
CC337 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC336 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF

PPHV_USBC_TA
PLACE_NEAR=UB300:3MM
CC310 12PF 5% 50V C0G-CERM 0201 NOSTUFF
CC309 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
PLACE_NEAR=UB300:3MM
NOSTUFF

PPHV_USBC_TB
PLACE_NEAR=UB400:3MM
CC3D6 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC311 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
PLACE_NEAR=UB400:3MM
NOSTUFF

PP1V2_ENET_INTREG
PLACE_NEAR=U9300.13:3MM
PLACE_NEAR=U9300.13:3MM
CC325 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC324 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP1V2_ENET_PHY_AVDDL
PLACE_NEAR=U9300.45:3MM
PLACE_NEAR=U9300.45:3MM
CC387 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC386 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP12V_MAIN
CC362 12PF 5% 25V C0G-CERM 0201 NOSTUFF
CC357 3PF +/-0.1PF 100V C0G 0201 NOSTUFF
CC356 12PF 5% 50V C0G-CERM 0201 NOSTUFF
CC355 3PF +/-0.1PF 100V C0G 0201 NOSTUFF

PPVCCIO_S0_CPU
CC3A7 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC3A6 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP1V2_ENET_PHY_PCIEPLL
PLACE_NEAR=U9300.29:3MM
PLACE_NEAR=U9300.29:3MM
CC385 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC384 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP1V2_ENET_PHY_GPHYPLL
PLACE_NEAR=U9300.36:3MM
PLACE_NEAR=U9300.36:3MM
CC383 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC382 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF

PP12V_S0_CPUCORE_FLT
CC363 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC361 3PF +/-0.1PF 100V C0G 0201 NOSTUFF
CC360 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC359 3PF +/-0.1PF 100V C0G 0201 NOSTUFF
CC358 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC353 3PF +/-0.1PF 100V C0G 0201 NOSTUFF
CC352 12PF 5% 25V NP0-C0G 0201 NOSTUFF
CC351 3PF +/-0.1PF 100V C0G 0201 NOSTUFF

BOM_COST_GROUP=DESENSE

PAGE TITLE: Desense CAPs 2

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 123 OF 142
SHEET: 105 OF 115

DFU AND FCT TESTPOINTS placed on top side of MLB, oppsite from CPU.

DFU TEST POINTS <RDAR://31619312>

Possibly useful panda signals

removed SOC_DEBUGPRT_RX/TX

TPC402	TP-P5	DEBUG_JTAG_SOC_TDO	38 113
TPC403	TP-P5	DEBUG_JTAG_SOC_TDI	38 113
TPC404	TP-P5	PP1V8_SLPS2R	84 102
TPC405	TP-P5	SOC_SOCHOT_L	37 71 113
TPC406	TP-P5	I2C_PWR_SDA	38 48
TPC407	TP-P5	I2C_UPC_SCL	38 48
TPC4E9	TP-P5	I2C_UPC_SDA	38 48
TPC4F0	TP-P5	DFUMUX_SEL	113
TPC4Z5	TP-P5	I2C_PWR_SCL	38 48
TPC401	TP-P5	USB_SOC_P	37 113
TPC431	TP-P5	USB_SOC_N	37 113
TPC440	TP-P5		
TPC439	TP-P5		
TPC4G6	TP-P5		

Other I2C TPs

Possibly useful panda signals

TPC435	TP-P5	I2C_FAN_SCL	48 57
TPC438	TP-P5	I2C_FAN_SDA	48 57

DFU NON-CUSTOMER-FACING USB PORTS

PLACE IN ACCESSIBLE BOARD AREA

SWDL

TPC408	TP-P5	USB3_TEST_D2R_N	OUT 14
TPC409	TP-P5	USB3_TEST_D2R_P	OUT 14
TPC410	TP-P5	USB3_TEST_R2D_N	IN 14
TPC411	TP-P5	USB3_TEST_R2D_P	IN 14
TPC412	TP-P5		
TPC413	TP-P5		
TPC414	TP-P5		
TPC415	TP-P5		
TPC416	TP-P5	USB_TEST_N	BI 14
TPC417	TP-P5	USB_TEST_P	BI 14
TPC418	TP-P5		

DZC400 5.5V-0.28PF 0201-THICKSTNCL
DZC401 5.5V-0.28PF 0201-THICKSTNCL
DZC402 5.5V-0.28PF 0201-THICKSTNCL
DZC403 5.5V-0.28PF 0201-THICKSTNCL
DZC408 5.5V-0.28PF 0201-THICKSTNCL
DZC409 5.5V-0.28PF 0201-THICKSTNCL

NON-CUSTOMER-FACING USB PORTS FOR ETHERNET DONGLE(Bristol OS Testing)

PLACE IN ACCESSIBLE BOARD AREA

Ethenet

TPC422	TP-P5	USB3_ENET_ADAPTOR_D2R_N	OUT 14
TPC423	TP-P5	USB3_ENET_ADAPTOR_D2R_P	OUT 14
TPC424	TP-P5	USB3_ENET_ADAPTOR_R2D_N	IN 14
TPC425	TP-P5	USB3_ENET_ADAPTOR_R2D_P	IN 14
TPC426	TP-P5		
TPC427	TP-P5		
TPC428	TP-P5		
TPC429	TP-P5		
TPC419	TP-P5	USB_ENET_ADAPTOR_N	BI 14
TPC420	TP-P5	USB_ENET_ADAPTOR_P	BI 14
TPC421	TP-P5		
TPC430	TP-P5	PP5V_G3S	87 103 106

DZC410 5.5V-0.28PF 0201-THICKSTNCL
DZC411 5.5V-0.28PF 0201-THICKSTNCL
DZC412 5.5V-0.28PF 0201-THICKSTNCL
DZC413 5.5V-0.28PF 0201-THICKSTNCL
DZC406 5.5V-0.28PF 0201-THICKSTNCL
DZC407 5.5V-0.28PF 0201-THICKSTNCL

AUDIO JACK

107 61	IN	AUD_CONN_HP_LEFT	
107 61	IN	AUD_CONN_HP_RIGHT	
107 61	IN	AUD_CONN_RING2	
107 61	IN	AUD_CONN_SLEEVE	
107 61	IN	AUD_CONN_HP_SENSE_L	
107 61	IN	AUD_CONN_HP_SENSE_R	
107 61	IN	AUD_CONN_TIP_SENSE	
107 61	IN	AUD_CONN_SLEEVE_XW	
107 61	IN	AUD_CONN_RING2_XW	
TPC4Z9	TP-P5	GND_AUDIO_CODEC	59

DEBUG MOJO

TPC451	TP-P5	PCH_UART_DEBUG_R2D	15 28 113
TPC452	TP-P5	PCH_UART_DEBUG_D2R	15 28 113
TPC453	TP-P5		

removed SMC_DEBUGPRT_RX/TX

Soc Access w/o Potassium

TPC454	TP-P5	SOC_USB_VBUS	28 37 113
TPC455	TP-P5	USB_SOC_TYPEC_P	28 113
TPC456	TP-P5	USB_SOC_TYPEC_N	28 113
TPC457	TP-P5	PMU_ACTIVE_READY	29 37 71 108 110
TPC458	TP-P5	SOC_FORCE_DFU	28 37 71 113
TPC459	TP-P5	SOC_DFU_STATUS	28 37
TPC460	TP-P5	UPC_XB_DBG3	28 30
TPC461	TP-P5	UPC_XB_DBG4	28 30
TPC462	TP-P5	SOC_DOCK_CONNECT	29 30 38
TPC463	TP-P5	SOC_SWD_MUX_SEL_PCH	15
TPC464	TP-P5		

Power Sequence,status,charging

TPC468	TP-P5	PP12V_MAIN	102 105
TPC469	TP-P5	PP1V2_S3	103 107
TPC470	TP-P5	PPVCC_S0_CPU_REG	102
TPC471	TP-P5	PP5V_G3S	87 103 106
TPC472	TP-P5	PMU_ONOFF_L	71 100
TPC4L6	TP-P5	CPU_PWRGD	6 13 108
TPC474	TP-P5	PMU_ONOFF_R_L	100 113
TPC475	TP-P5	PM_SLP_S3_L	12 14 26 80 92 106 110
TPC476	TP-P5	PM_SLP_S4_L	12
TPC477	TP-P5	PM_SLP_S5_L	12 110
TPC478	TP-P5	PM_RSMRST_L	12 18 45 47 68 108 110
TPC479	TP-P5	PPDDRVTT_S0_MEM	103 107
TPC481	TP-P5	PP1V_S3	103
TPC482	TP-P5	PM_SYSRST_L	12 18 45 108
TPC483	TP-P5	PM_PCH_SYS_PWROK	12 45
TPC484	TP-P5	PM_PCH_PWROK	12 34 45 100
TPC485	TP-P5	PLT_RST_L	12 13 15 20 110
TPC487	TP-P5	PM_SLP_S0_L	12 38 71 100
TPC488	TP-P5	SMC_FIXTURE_MODE_L	38
TPC489	TP-P5	PP1V8_G3S	59 103
TPC490	TP-P5	PP5V_G3S	87 103 106
TPC491	TP-P5	PP3V3_G3H	102 105
TPC492	TP-P5	PP3V3_G3H_SSD	102
TPC493	TP-P5	PP3V3_S0SW_TBT_X	103
TPC4B4	TP-P5	PPVDDCPU_AWAKE_SOC	102
TPC4B6	TP-P5	PVDDQ_EN	47 71
TPC4B7	TP-P5	PVCCIO_EN	71 73
TPC4B8	TP-P5	PP0V9_SLPDDR	102
TPC4B9	TP-P5	PP1V1_SLPDDR	102
TPC4C0	TP-P5	PP1V1_SLPS2R	102
TPC4C1	TP-P5	PP1V8_AWAKE	102
TPC4J1	TP-P5	SMC_SYSRST_L	38 45 108
TPC4C4	TP-P5	PP1V8_SLPS2R_PMUVDDGPIO	69
TPC4C5	TP-P5	P1V1_SLPDDR_SOCFET_EN	70 71
TPC4C6	TP-P5	PMU_CLK32K_WLANBT_R	35 71
TPC4C7	TP-P5	SOC_WDOG	38 71
TPC4C8	TP-P5	PMU_CLK32K_SOC	38 71
TPC4C9	TP-P5	PMU_SYS_ALIVE	37 38 71 79 88
TPC437	TP-P5		

BOM_COST_GROUP=DEBUG

Power Sequence,status,charging

TPC4D0	TP-P5	P5VG3S_EN	47 71 100
TPC4D1	TP-P5	PP0V8_SLPS2R	102
TPC4D2	TP-P5	PPVDDCPUSRAM_AWAKE	102
TPC4D3	TP-P5	P5VG3S_PGOOD	47 71
TPC4D4	TP-P5	CPUVR_PGOOD	47 71 110
TPC4L7	TP-P5	PPVCCGT_S0_CPU_REG	102
TPC4F3	TP-P5	PPVCCSA_S0_CPU_REG	102
TPC4L0	TP-P5	PPVCCIO_S0_CPU	102
TPC4F4	TP-P5	PP1V_S0SW	103
TPC4F5	TP-P5	PP1V2_S0SW	103
TPC4F6	TP-P5	PP1V_PRIM	103
TPC4F7	TP-P5	PP1V8_S5	103
TPC4F8	TP-P5	PP3V0_G3H_RTC	102
TPC4F9	TP-P5	ALL_SYS_PWRGD	45 71 110
TPC4G0	TP-P5	PCH_RTC_RESET_L	12 71
TPC4G1	TP-P5	PM_THRMTRIP_L	13 20
TPC4G2	TP-P5	PM_PWRBTN_L	12 20
TPC4G3	TP-P5	CPU_PROCHOT_R_L	6
TPC4G4	TP-P5	PP1V2_ENET	83 86
TPC4I2	TP-P5	PP0V85_ENET	83 87 104
TPC4G7	TP-P5	PP2V1_ENET	83 86
TPC4G8	TP-P5	PP3V3_G3H_ENET	85 102
TPC4G9	TP-P5	PP3V3_AWAKE	102
TPC4H0	TP-P5	PMU_COLD_RESET_L	38 71 108
TPC4H1	TP-P5	PP0V82_SLPDDR	102
TPC4H3	TP-P5	PMU_PVDDMAIN_EN	68 71
TPC4H4	TP-P5	UPC_PMU_RESET	28 71
TPC4H5	TP-P5	P3V3G3S_EN	47 71
TPC4H6	TP-P5	PP3V3_G3S	59 86 103
TPC4H7	TP-P5	TP_P1V8G3S_EN	71
TPC4L1	TP-P5	SSD_PMU_RESET_L	37 46 79
TPC4L2	TP-P5	PP2V7_NAND_SSD0	75 76 77 78 79 105 112
TPC4I0	TP-P5	PP3V3_S5	82 103
TPC4I1	TP-P5	PP0V9_SSD0	75 76 77 78 79 105 112
TPC4I4	TP-P5	PP1V8_SSD0	112 75 76 77 78 79 104 105
TPC4I5	TP-P5	PP1V2_AWAKE	102

Soc Access with Potassium

TPC436	TP-P5	USBC_XB_SBU1	30 31
TPC4A0	TP-P5	USBC_XB_SBU2	30 31
TPC400	TP-P5	USBC_XA_CC1	29 31
TPC4A2	TP-P5	PPVBUS_USBC_XA	28 29 31 107
TPC4A3	TP-P5		

ACDC Power Input TPs

TPC4A4	TP-P5	PP12V_G3H_ACDC	102 106
TPC4A5	TP-P5	PP12V_G3H_ACDC	102 106
TPC4A6	TP-P5	PP12V_G3H_ACDC	102 106
TPC4A7	TP-P5	PP12V_G3H_ACDC	102 106
TPC4A8	TP-P5	PP12V_G3H_ACDC	102 106
TPC4A9	TP-P5	PP12V_G3H_ACDC	102 106
TPC4B1	TP-P5		
TPC4B2	TP-P5		
TPC4B3	TP-P5		
TPC4C2	TP-P5		
TPC4D5	TP-P5		
TPC4D6	TP-P5		
TPC434	TP-P5	PP12V_G3H_ACDC	102 106
TPC432	TP-P5	PP12V_G3H_ACDC	102 106
TPC433	TP-P5	PP12V_G3H_ACDC	102 106

PAGE TITLE: DFU TEST POINTS

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 124 OF 142
SHEET: 106 OF 115

FCT TEST POINTS (TOP SIDE OF MLB)

AUDIO

TPC597	A	1	TP-P5	
TPC5A1	A	1	TP-P5	SPKRCONN_OUTP
TPC5A0	A	1	TP-P5	SPKRCONN_OUTN
TPC598	A	1	TP-P5	
TPC510	A	1	TP-P5	SPKRCONN_OUTP
TPC511	A	1	TP-P5	SPKRCONN_OUTN
TPC5A2	A	1	TP-P5	
TPC5B8	A	1	TP-P5	AUD_CONN_RING_SENSE
TPC5B7	A	1	TP-P5	AUD_CONN_RING2_XW
TPC5B6	A	1	TP-P5	AUD_CONN_TIP_SENSE
TPC5B5	A	1	TP-P5	AUD_CONN_HP_SENSE_R
TPC5A7	A	1	TP-P5	
TPC5B3	A	1	TP-P5	AUD_CONN_HP_SENSE_L
TPC5A8	A	1	TP-P5	AUD_CONN_HP_LEFT
TPC5A9	A	1	TP-P5	AUD_CONN_HP_RIGHT
TPC5B0	A	1	TP-P5	AUD_CONN_RING2
TPC5B2	A	1	TP-P5	AUD_CONN_SLEEVE
TPC5K0	A	1	TP-P5	
TPC5K1	A	1	TP-P5	AUD_CONN_SLEEVE_XW

HDMI Test Poins

TPC556	A	1	TP-P5	HDMI_CEC_CONN
TPC557	A	1	TP-P5	HDMI_RSVD
TPC561	A	1	TP-P5	HDMI_DDC_5V_CONN_SCL
TPC563	A	1	TP-P5	HDMI_DDC_5V_CONN_SDA
TPC5Y9	A	1	TP-P5	HDMI_HPD_IN_CONN
TPC592	A	1	TP-P5	PP5V0_HDMI_DDC_CONN
TPC593	A	1	TP-P5	
TPC594	A	1	TP-P5	

WIRELESS

TPC5H9	A	1	TP-P5	PP3V3_G3S_WLANBT
TPC5I0	A	1	TP-P5	PP1V8_G3S
TPC5L0	A	1	TP-P5	PPVIN_RFLDO_WLANBT
TPC5L1	A	1	TP-P5	PP1V2_WLANBT
TPC5L2	A	1	TP-P5	PP1V5_WLANBT

MEMORY

TPC5I3	A	1	TP-P5	PVDDQ_PGOOD
TPC5I4	A	1	TP-P5	PP1V2_S3
TPC5I5	A	1	TP-P5	PP2V5_S3
TPC5I6	A	1	TP-P5	PPDDRVTT_S0_MEM
TPC5I7	A	1	TP-P5	PP1V2_S3

HDMI

TPC505	A	1	TP-P5	DDI2_MUX_SEL
TPC506	A	1	TP-P5	DDI1_MUX_SEL

USB-A Test Poins

High Speed - Tear drops, NO TP

		IN		USB3_EXTA_TX_F_P
		IN		USB3_EXTA_TX_F_N
		IN		USB3_EXTA_RX_P
		IN		USB3_EXTA_RX_N
		IN		USB2_EXTA_P
		IN		USB2_EXTA_N
		IN		USB3_EXTB_TX_F_P
		IN		USB3_EXTB_TX_F_N
		IN		USB3_EXTB_RX_P
		IN		USB3_EXTB_RX_N
		IN		USB2_EXTB_P
		IN		USB2_EXTB_N
TPC595	A	1	TP-P5	PP5V_S4_EXTA_F
TPC596	A	1	TP-P5	PP5V_S4_EXTB_F
TPC599	A	1	TP-P5	
TPC5A6	A	1	TP-P5	
TPC5C5	A	1	TP-P5	PP5V_S4_EXTA_F
TPC5C6	A	1	TP-P5	PP5V_S4_EXTB_F
TPC5C7	A	1	TP-P5	
TPC5C8	A	1	TP-P5	

USBC (PLACE NEAR CONNECTOR)

TPC5G4	A	1	TP-P5	USBC_XA_SBU1
TPC5G5	A	1	TP-P5	USBC_XA_SBU2
TPC5G6	A	1	TP-P5	USBC_TA_SBU1
TPC507	A	1	TP-P5	USBC_TA_SBU2
TPC508	A	1	TP-P5	USBC_TB_SBU1
TPC509	A	1	TP-P5	USBC_TB_SBU2
TPC5G7	A	1	TP-P5	USBC_XA_CC2
TPC5G9	A	1	TP-P5	PPVBUS_USBC_XA
TPC5H0	A	1	TP-P5	PPVBUS_USBC_XA
TPC5H1	A	1	TP-P5	PPVBUS_USBC_XA
TPC5H3	A	1	TP-P5	PPVBUS_USBC_XB
TPC5H4	A	1	TP-P5	PPVBUS_USBC_XB
TPC5I8	A	1	TP-P5	PPVBUS_USBC_XB
TPC5J1	A	1	TP-P5	PPVBUS_USBC_TA
TPC5J0	A	1	TP-P5	PPVBUS_USBC_TA
TPC5J2	A	1	TP-P5	PPVBUS_USBC_TA
TPC5J4	A	1	TP-P5	PPVBUS_USBC_TB
TPC5H5	A	1	TP-P5	PPVBUS_USBC_TB
TPC5H6	A	1	TP-P5	PPVBUS_USBC_TB
TPC5H7	A	1	TP-P5	
TPC5H8	A	1	TP-P5	
TPC5M2	A	1	TP-P5	
TPC5K2	A	1	TP-P5	
TPC5K3	A	1	TP-P5	
TPC5K4	A	1	TP-P5	
TPC5J5	A	1	TP-P5	
TPC5J6	A	1	TP-P5	
TPC5N9	A	1	TP-P5	USBC_XB_CC1
TPC5N8	A	1	TP-P5	USBC_XB_CC2
TPC5O1	A	1	TP-P5	USBC_TA_CC1
TPC5O2	A	1	TP-P5	USBC_TA_CC2
TPC5O3	A	1	TP-P5	USBC_TB_CC1
TPC5O4	A	1	TP-P5	USBC_TB_CC2

FAN Test Points

TPC558	A	1	TP-P5	FAN_0_PWM_FILT
TPC559	A	1	TP-P5	FAN_0_TACH_FILT
TPC562	A	1	TP-P5	PP12V_FAN_FILT
TPC564	A	1	TP-P5	
TPC565	A	1	TP-P5	

ENET HS signals - Tear drops, NO TP

	IN		ENET_CONN_A_P
	IN		ENET_CONN_A_N
	IN		ENET_CONN_B_P
	IN		ENET_CONN_B_N
	IN		ENET_CONN_C_P
	IN		ENET_CONN_C_N
	IN		ENET_CONN_D_P
	IN		ENET_CONN_D_N

PSU Test Points

TPC501	A	1	TP-P5	SNS_ACDC_P
TPC500	A	1	TP-P5	SNS_ACDC_N
TPC503	A	1	TP-P5	ACDC_ID
TPC504	A	1	TP-P5	ACDC_BURST_EN_L
TPC502	A	1	TP-P5	SYS_LED

MISC

TPC540	A	1	TP-P5	SYS_LED_DR
TPC541	A	1	TP-P5	ISNS_P1V2_N
TPC542	A	1	TP-P5	ISNS_P1V2_P
TPC543	A	1	TP-P5	ISNS_P3V3_G3H_HI_N
TPC544	A	1	TP-P5	ISNS_P3V3_G3H_HI_P
TPC545	A	1	TP-P5	ISNS_P3V3_WLANBT_N
TPC548	A	1	TP-P5	ISNS_P3V3_WLANBT_P
TPC547	A	1	TP-P5	ISNS_P5V_G3S_HI_N
TPC546	A	1	TP-P5	ISNS_P5V_G3S_HI_P
TPC549	A	1	TP-P5	ISNS_PMU_N
TPC512	A	1	TP-P5	ISNS_PMU_P
TPC551	A	1	TP-P5	PMU_P3V3_CAPLE_ISENSE
TPC552	A	1	TP-P5	PP12V_FAN_FET
TPC513	A	1	TP-P5	PP12V_G3H_VIN_P3V3_G3H
TPC515	A	1	TP-P5	PP12V_G3H_VIN_P5V_G3S
TPC514	A	1	TP-P5	PP12V_S0_CPUCORE_FLT
TPC518	A	1	TP-P5	PP2V5_S3_VPP
TPC517	A	1	TP-P5	PP3V3_G3H_PMU
TPC516	A	1	TP-P5	PP3V3_S0_TBT
TPC519	A	1	TP-P5	PP5V_G3S_USBA
TPC523	A	1	TP-P5	PP5V_G3S_USBC
TPC522	A	1	TP-P5	PPBUS_HS_CPU
TPC520	A	1	TP-P5	PPCPUVCCSA_S0_SENSE_1
TPC521	A	1	TP-P5	PPVCCIO_S0_CPU_REG
TPC524	A	1	TP-P5	PPVDDQ_S3_REG_R
TPC527	A	1	TP-P5	PPVIN_ENET_P0V85
TPC526	A	1	TP-P5	PPVIN_G3H_P2V7
TPC525	A	1	TP-P5	SMC_CPU_HI_ISENSE
TPC528	A	1	TP-P5	SMC_CPU_VCC_ISENSE
TPC529	A	1	TP-P5	SMC_CPUGT_ISENSE
TPC530	A	1	TP-P5	SMC_P12VIN_ISENSE
TPC531	A	1	TP-P5	SMC_P1V2_ISENSE
TPC534	A	1	TP-P5	XDP_CPU_TCK
TPC533	A	1	TP-P5	XDP_CPU_TDI
TPC532	A	1	TP-P5	XDP_CPU_TDO
TPC535	A	1	TP-P5	XDP_CPU_TMS
TPC536	A	1	TP-P5	XDP_CPU_TRST_L

BOM_COST_GROUP=PCB

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: FCT TESTPOINTS

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 125 OF 142

SHEET: 107 OF 115

ICT TEST POINTS, ICT BOUNDARY SCAN TESTPOINTS

CPU XDP and PCH Test-Points

107 18 6	IN	XDP_CPU_TCK
18 13	IN	XDP_PCH_TCK
107 18 6	IN	XDP_CPU_TDI
107 18 6	IN	XDP_CPU_TDO
107 18 13 6	IN	XDP_CPU_TRST_L
107 18 6	IN	XDP_CPU_TMS
18 13	IN	XDP_PCH_TMS
18 13	IN	XDP_PCH_TDI
18 13	IN	XDP_PCH_TDO
18 13 6	IN	XDP_CPU_PREQ_L
18 13 6	IN	XDP_CPU_PRDY_L
47 45 18 12 110 106	IN	PM_RSMRST_L
106 45 34 12	IN	PM_PCH_PWROK
106 45 18 12	IN	PM_SYSRST_L
18 6	IN	CPU_CFG<3>
18 13	IN	PCH_JTAGX
18 13	BI	PCH_ITP_PMODE

H9M BOUNDARY SCAN TESTPOINTS ON FCT TESTPOINT PAGE

OTHER ICT TESTPONTS

ACE

26 15	BI	JTAG_TBT_X_TMS
94 92 26	BI	JTAG_ISP_TDI
94 92 26	BI	JTAG_ISP_TCK
94 92 26	BI	JTAG_ISP_TDO
108 26	BI	TBT_X_TEST_EN

WLAN

38 36	BI	WLAN_JTAG_TMS
38 36	BI	WLAN_JTAG_TCK
39 36	BI	WLAN_JTAG_TDI
36 35	BI	WLAN_JTAG_TDO
36 35	BI	WLAN_JTAG_TRST_L
92 15	BI	JTAG_TBT_T_TMS
38	BI	TP_JTAG_SOC_TRST_L

45 38	BI	SMC_PCH_SYS_PWROK
45 38	BI	SMC_PCH_PWROK
106 45 38	BI	SMC_SYSRST_L
106 13 6	BI	CPU_PWRGD
106 71 38	BI	PMU_COLD_RESET_L
38	BI	SOC_JTAG_SEL
37	BI	SOC_TESTMODE
36 35	BI	WLAN_JTAG_SEL
92	BI	TBT_T_TEST_EN
108 26	BI	TBT_X_TEST_EN

TP of HDMI (EE tests)

TPC646	DP2HDMI_PMU_CEC_IRQ	90
TPC641	DP2HDMI_1.5G_FILT_EN	88 90

TP of Calpe PMIC (EE tests)

TPC642	TP_PP1V8_PMU_BUCK3SW5	69
TPC643	TP_PP1V1_PMU_BUCK4SW1	69
TPC644	TP_PP1V2_PMU_BUCK6SW1	69 108
TPC645	TP_PP1V_PMU_BUCK8SW1	69 108
TPC676	SOC_VDDCPU_SENSE	41 71
TPC664	TP_P3V3G3W_EN	71
TPC665	TP_P3V3G3W_PGOOD	71
TPC667	TP_SE_PWR_EN	71
TPC668	TP_P3V3_S5_EN	71
TPC670	TP_PVCCEOPIOEDRAM_P2V7NAND_PGOOD	71
TPC671	TP_PEARL_P2V7NAND_EN	71
TPC672	TP_NAND_DISCHARGE_HDD_PWR_EN	71
TPC673	TP_NAND_RESET_L_SD_PWR_EN	71
TPC674	ENET_PWR_EN	71 72 85 86 87
TPC675	TBT_PWR_EN	71 72
TPC679	UPC_TA_GPIO7	95
TPC635	BT_PWR_EN	35 36 71
TPC669	WLAN_PWR_EN	35 36 71
TPC680	UPC_TB_GPIO7	96
TPC681	TP_PP1V2_PMU_BUCK6SW1	69 108
TPC682	TP_PP1V_PMU_BUCK8SW1	69 108
TPC677	FAN_PWR_EN	57 71
TPC683	PVCCIO_PGOOD	47 71
TPC684	P3V3MAIN_PGOOD	47 71 110
TPC636	PVCCPLLOC_EN	71 72

Test Points for Calpe breakout

TPC647	PMU_VCCIO_ISENSE	46 71 108
TPC648	PMU_VCCIO_ISENSE	46 71 108
TPC649	PMU_VCCIO_ISENSE	46 71 108
TPC650	PMU_P5V_G3S_HI_ISENSE	46 71
TPC651	PMU_CPUSA_VSENSE	46 71
TPC652	PMU_P5V_USBC_ISENSE	46 71
TPC653	PMU_P5V_USBA_ISENSE	46 71
TPC654	TP_PMU_AMUX_AY	71
TPC655	PMU_P3V3_TBT_ISENSE	46 71
TPC656	PMU_P3V3_SSD0_ISENSE	46 71
TPC657	PMU_PBUS_SSD0_ISENSE	46 71
TPC658	PMU_P3V3_G3H_HI_ISENSE	46 71
TPC659	PMU_P3V3_WLANBT_ISENSE	46 71
TPC660	PMU_P3V3_ENET_ISENSE	46 71
TPC661	PMU_P12V_ENET_ISENSE	46 71
TPC662	TP_PMU_AMUX_B7	71
TPC663	TP_PMU_AMUX_BY	71

TP of H9ML (EE tests)

TPC678	PCC_EVENT	38
TPC686	TP_SMC_DEBUG	46
TPC687	WLAN_CONTEXT_A	35 36 38
TPC688	WLAN_CONTEXT_B	35 36 38

TP of CONTEXT_A/B can be used for AOP_UART_TX/RX for debug

TPC600	LIDOPEN_PSU12VPGOOD_ACDCBURST_L	38 100
TPC6G8	SWD_SOC_SWDIO	38 46 113
TPC6G9	SWD_SOC_SWCLK	38 46 113

EE TESTS PCH

TPC631	PCIE_CLK100M_WLAN_PCH_N	12 20
TPC632	PCIE_CLK100M_WLAN_PCH_P	12 20
TPC633	PCIE_CLK100M_SOC_N	12 40
TPC634	PCIE_CLK100M_SOC_P	12 40
TPC637	PCIE_CLK100M_TBT_X_N	12 26
TPC638	PCIE_CLK100M_TBT_X_P	12 26
TPC639	PCIE_CLK100M_TBT_T_N	12 92
TPC640	PCIE_CLK100M_TBT_T_P	12 92
TPC690	SPI_PCHROM_MOSI	13 18
TPC691	TP_PCH_CLK32K_SUS	12
TPC692	SPI_IO<2>	13 18
TPC693	SPI_IO<3>	13

TP Debug ACE Nets (EE tests)

TPC622	UPC_XA_DEBUGUART_TX	29
TPC623	PMU_ACTIVE_READY	29 37 71 106 110
TPC624	UPC_XB_DEBUGUART_TX	30
TPC625	UPC_XB_GPIO1	30

Test Points for Ace XA/XB GPIO0/1, must have in production.

TPC626	UPC_TA_DEBUGUART_TX	95
TPC627	UPC_TA_GPIO1	95
TPC628	UPC_TB_DEBUGUART_TX	96
TPC629	UPC_TB_GPIO1	96

Test Points for Ace XA/XB GPIO0/1, must have in production.

SENSOR TPs

TPC694	SNS_P12VG3H_P	51
TPC695	SNS_P12VG3H_N	51
TPC6C9	ISNS_HS_COMPUTING_P	51
TPC6C8	ISNS_HS_COMPUTING_N	51
TPC6D2	CPUVR_ISNS_R_P	52
TPC6D1	CPUVR_ISNS_R_N	52
TPC6D0	ISNS_P3V3_G3W_SSD0_P	53
TPC6D3	ISNS_P3V3_G3W_SSD0_N	53
TPC6D6	ISNS_PPBUS_MAIN_SSD0_P	53
TPC6D5	ISNS_PPBUS_MAIN_SSD0_N	53
TPC6D4	ISNS_TBT_P	54
TPC6D8	ISNS_TBT_N	54
TPC6D7	ISNS_CPUVCCIO_P	54
TPC6E0	ISNS_CPUVCCIO_N	54
TPC6E1	CPUGT_ISNS_P	54
TPC6D9	CPUGT_ISNS_N	54
TPC6E4	ISNS_P5V_USBC_P	56
TPC6E3	ISNS_P5V_USBC_N	56
TPC6E2	ISNS_P5V_USBA_P	56
TPC6E6	ISNS_P5V_USBA_N	56
TPC6E5	ISNS_P3V3_ENET_P	56
TPC6E8	ISNS_P3V3_ENET_N	56
TPC6E9	ISNS_P12V_ENET_P	56
TPC6E7	ISNS_P12V_ENET_N	56
TPC6F0	PMU_CPUSA_VSENSE	46 56
TPC6F1	SMC_CPU_VCC_VSENSE	46 56
TPC6F4	SMC_CPUGT_VSENSE	46 55
TPC6F2	TSNS_T1_DX1_P	55
TPC6F3	TSNS_T1_DX2_P	55
TPC6F6	TSNS_T1_DX3_P	55
TPC6F7	TSNS_T1_DX4_P	55
TPC6F5	TSNS_T1_DX5_P	55
TPC6F9	TSNS_T1_DX6_P	55
TPC6F8	TSNS_T1_DX7_P	55
TPC6G0	TSNS_T1_DX8_P	55
TPC6G1	TSNS_T1_DN	55
TPC6G2	TSNS_T2_DX1_P	55
TPC6G4	TSNS_T2_DX4_P	55
TPC6G3	TSNS_T2_DX4_N	55
TPC6G5	TSNS_T2_DN	55
TPC6G6	TBTTHMSNS_X_D2_P	55
TPC6G7	TBTTHMSNS_X_D2_N	55
TPC6H1	REG_VCCSA_ISNS_1_P	54 66
TPC6H0	REG_VCCSA_ISNS_1_N	54 66
TPC6H3	ISNS_2V5_S3_P	52
TPC6H2	ISNS_2V5_S3_N	52
TPC6H5	TBTTHMSNS_T_D3_P	55
TPC6H4	TBTTHMSNS_T_D3_N	55

S4E

TPC619	SSD0_CLKREQ0_L	40 46 75
TPC617	SSD0_CLKREQ1_L	40 46 76
TPC616	SSD0_CLKREQ2_L	40 46 77
TPC630	SSD0_CLKREQ3_L	40 46 78
TPC614	SSD0_S4E0_DROOP_L	75
TPC618	SSD0_S4E1_DROOP_L	76
TPC611	SSD0_S4E2_DROOP_L	77
TPC612	SSD0_S4E3_DROOP_L	78
TPC685	SSD0_OCARINA_VDD_LDO	79
TPC689	SSD0_OCARINA_WP_L	75 76 77 78 79
TPC601	SSD0_VR_P2V7_EN	79
TPC602	SSD0_OCARINA_RESET_L	75 76 77 78 79
TPC603	SSD0_VR_P2V7_PGOOD	79
TPC604	SSD0_OCARINA_TCAL	79
TPC606	SSD0_OCARINA_PFN	75 76 77 78 79
TPC605	SSD0_OCARINA_FORCE_EN	79
TPC607	SSD0_OCARINA_VREF	79
TPC608	SSD0_S4E_BOOT2	74 75 76 77 78
TPC609	SSD0_S4E0_ZQ_C	75
TPC615	SSD0_S4E0_ZQ_L	75
TPC610	SSD0_S4E1_ZQ_C	76
TPC613	SSD0_S4E1_ZQ_L	76
TPC620	SSD0_S4E2_ZQ_C	77
TPC666	SSD0_S4E2_ZQ_L	77
TPC621	SSD0_S4E3_ZQ_C	78
TPC696	SSD0_S4E3_ZQ_L	78
TPC697	SSD0_S4E0_PCIE_RESREF	75
TPC698	SSD0_S4E1_PCIE_RESREF	76
TPC6A1	SSD0_S4E2_PCIE_RESREF	77
TPC6A0	SSD0_S4E3_PCIE_RESREF	78
TPC699	I2C_SSD_SCL	38 48
TPC6A2	I2C_SSD_SDA	38 48
TPC6A3	SSD_BFH	37 74 75 76 77 78
TPC6A4	SSD0_PCIE_RESET_L	40 46 75 76 77 78
TPC6A5	SSD0_STG01_ADDR	79
TPC6B0	TP_SSD0_OCARINA_VR2_DIS	79
TPC6B1	SSD0_OCARINA_LPB_L	74 75 76 77 78 79

SSD BOUNDARY SCAN Test-Points

TPC6A6	SSD0_S4E_JTAG_TRST_L	74 75 76 77 78
TPC6A9	SSD0_S4E_JTAG_SEL	74 75 76 77 78
TPC6A8	SSD0_SWDIO_UART_D2R	38 74 75 76 77 78
TPC6A7	SSD0_SWCLK_UART_R2D	38 74 75 76 77 78
TPC6B2	TP_SSD0_S4E0_ANI1_VREF	75
TPC6B3	TP_SSD0_S4E0_ANI0_VREF	75
TPC6B6	TP_SSD0_S4E1_ANI1_VREF	76
TPC6B5	TP_SSD0_S4E1_ANI0_VREF	76
TPC6B4	TP_SSD0_S4E2_ANI1_VREF	77
TPC6B7	TP_SSD0_S4E2_ANI0_VREF	77
TPC6B8	TP_SSD0_S4E3_ANI1_VREF	78
TPC6B9	TP_SSD0_S4E3_ANI0_VREF	78
TPC6C1	SSD0_S4E0_SWD_UID0	75
TPC6C0	SSD0_S4E0_SWD_UID1	75
TPC6C2	SSD0_S4E1_SWD_UID0	76
TPC6C3	SSD0_S4E1_SWD_UID1	76
TPC6C4	SSD0_S4E2_SWD_UID0	77
TPC6C6	SSD0_S4E2_SWD_UID1	77
TPC6C7	SSD0_S4E3_SWD_UID0	78
TPC6C5	SSD0_S4E3_SWD_UID1	78

BOM_COST_GROUP=PCB

PAGE TITLE: ICT, MAC-1 ,EE Testpoints

Apple Inc.

DRAWING NUMBER: 051-02424 | SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 126 OF 142
SHEET: 108 OF 115

ICT TESTPOINTS , High Speed NO_TEST

CPU

PEG

84 5	IN	PCIE_ENET_D2R_N<3..0>	NO_TEST=1
84 5	IN	PCIE_ENET_D2R_P<3..0>	NO_TEST=1
84 5	IN	PCIE_ENET_R2D_C_N<3..0>	NO_TEST=1
84 5	IN	PCIE_ENET_R2D_C_P<3..0>	NO_TEST=1
94 5	IN	PCIE_TBT_T_D2R_N<3..0>	NO_TEST=1
94 5	IN	PCIE_TBT_T_D2R_P<3..0>	NO_TEST=1
94 5	IN	PCIE_TBT_T_R2D_C_N<3..0>	NO_TEST=1
94 5	IN	PCIE_TBT_T_R2D_C_P<3..0>	NO_TEST=1
28 5	IN	PCIE_TBT_X_D2R_N<3..0>	NO_TEST=1
28 5	IN	PCIE_TBT_X_D2R_P<3..0>	NO_TEST=1
28 5	IN	PCIE_TBT_X_R2D_C_N<3..0>	NO_TEST=1
28 5	IN	PCIE_TBT_X_R2D_C_P<3..0>	NO_TEST=1

DMI

13 5	IN	DMI_S2N_N<3..0>	NO_TEST=1
13 5	IN	DMI_S2N_P<3..0>	NO_TEST=1
13 5	IN	DMI_N2S_N<3..0>	NO_TEST=1
13 5	IN	DMI_N2S_P<3..0>	NO_TEST=1

DDI

21 5	IN	DP_DDI1_ML_C_N<3..0>	NO_TEST=1
21 5	IN	DP_DDI1_ML_C_P<3..0>	NO_TEST=1
21 5	IN	DP_DDI2_ML_C_N<3..0>	NO_TEST=1
21 5	IN	DP_DDI2_ML_C_P<3..0>	NO_TEST=1
91 5	IN	DP_DDI3_ML_C_N<3..0>	NO_TEST=1
91 5	IN	DP_DDI3_ML_C_P<3..0>	NO_TEST=1
21 5	IN	DP_DDI1_AUXCH_C_N	NO_TEST=1
21 5	IN	DP_DDI1_AUXCH_C_P	NO_TEST=1
21 5	IN	DP_DDI2_AUXCH_C_N	NO_TEST=1
21 5	IN	DP_DDI2_AUXCH_C_P	NO_TEST=1
91 5	IN	DP_DDI3_AUXCH_C_N	NO_TEST=1
91 5	IN	DP_DDI3_AUXCH_C_P	NO_TEST=1

CPU CLK

12 6	IN	CPU_CLK24M_NSSC_CLK_N	NO_TEST=1
12 6	IN	CPU_CLK24M_NSSC_CLK_P	NO_TEST=1
12 6	IN	CPU_CLK100M_PCIBCLK_N	NO_TEST=1
12 6	IN	CPU_CLK100M_PCIBCLK_P	NO_TEST=1
12 6	IN	CPU_CLK100M_BCLK_N	NO_TEST=1
12 6	IN	CPU_CLK100M_BCLK_P	NO_TEST=1

DDR4 MEM

25 7	IN	MEM_A_DQ<63..0>	NO_TEST=1
25 7	IN	MEM_A_DQS_N<7..0>	NO_TEST=1
25 7	IN	MEM_A_DQS_P<7..0>	NO_TEST=1
23 7	IN	MEM_A_CLK_N<1..0>	NO_TEST=1
23 7	IN	MEM_A_CLK_P<1..0>	NO_TEST=1
23 7	IN	MEM_A_CKE<1..0>	NO_TEST=1
23 7	IN	MEM_A_CS_L<1..0>	NO_TEST=1
23 7	IN	MEM_A_ODT<1..0>	NO_TEST=1
23 7	IN	MEM_A_BA<1..0>	NO_TEST=1
23 7	IN	MEM_A_BG<1..0>	NO_TEST=1
23 7	IN	MEM_A_ACT_L	NO_TEST=1
23 7	IN	MEM_A_ALERT_L	NO_TEST=1
23 7	IN	MEM_A_PAR	NO_TEST=1
23 7	IN	MEM_A_A<16..0>	NO_TEST=1
25 7	IN	MEM_B_DQ<63..0>	NO_TEST=1
25 7	IN	MEM_B_DQS_N<7..0>	NO_TEST=1
25 7	IN	MEM_B_DQS_P<7..0>	NO_TEST=1
24 7	IN	MEM_B_CLK_N<1..0>	NO_TEST=1
24 7	IN	MEM_B_CLK_P<1..0>	NO_TEST=1
24 7	IN	MEM_B_CKE<1..0>	NO_TEST=1
24 7	IN	MEM_B_CS_L<1..0>	NO_TEST=1
24 7	IN	MEM_B_ODT<1..0>	NO_TEST=1
24 7	IN	MEM_B_BA<1..0>	NO_TEST=1
24 7	IN	MEM_B_BG<1..0>	NO_TEST=1
24 7	IN	MEM_B_ACT_L	NO_TEST=1
24 7	IN	MEM_B_PAR	NO_TEST=1
24 7	IN	MEM_B_A<16..0>	NO_TEST=1

PMIC

XTAL

71	IN	PMU_XTAL1	NO_TEST=1
71	IN	PMU_XTAL1_R	NO_TEST=1
71	IN	PMU_XTAL2	NO_TEST=1

PCH

CLK

18 12	IN	ITPXDP_CLK100M_N	NO_TEST=1
18 12	IN	ITPXDP_CLK100M_P	NO_TEST=1

USB 3.0

113 109 14	IN	USB3_VITAMIN_D2R_N	NO_TEST=1
113 109 14	IN	USB3_VITAMIN_D2R_P	NO_TEST=1
113 109 14	IN	USB3_VITAMIN_D2R_N	NO_TEST=1
113 109 14	IN	USB3_VITAMIN_D2R_P	NO_TEST=1
113 14	IN	USB3_VITAMIN_R2D_C_N	NO_TEST=1
113 14	IN	USB3_VITAMIN_R2D_C_P	NO_TEST=1
62 14	IN	USB3_EXTA_D2R_N	NO_TEST=1
62 14	IN	USB3_EXTA_D2R_P	NO_TEST=1
62 14	IN	USB3_EXTA_R2D_C_N	NO_TEST=1
62 14	IN	USB3_EXTA_R2D_C_P	NO_TEST=1
62 14	IN	USB3_EXTB_D2R_N	NO_TEST=1
62 14	IN	USB3_EXTB_D2R_P	NO_TEST=1
62 14	IN	USB3_EXTB_R2D_C_N	NO_TEST=1
62 14	IN	USB3_EXTB_R2D_C_P	NO_TEST=1

PCIE

20 14	IN	PCIE_WLANPCH_D2R_N	NO_TEST=1
20 14	IN	PCIE_WLANPCH_D2R_P	NO_TEST=1
20 14	IN	PCIE_WLANPCH_R2D_C_N	NO_TEST=1
20 14	IN	PCIE_WLANPCH_R2D_C_P	NO_TEST=1
81 14	IN	PCIE_ENET_PCH_D2R_N	NO_TEST=1
81 14	IN	PCIE_ENET_PCH_D2R_P	NO_TEST=1
81 14	IN	PCIE_ENET_PCH_R2D_C_N	NO_TEST=1
81 14	IN	PCIE_ENET_PCH_R2D_C_P	NO_TEST=1
40 14	IN	PCIE_SOC_D2R_N<3..0>	NO_TEST=1
40 14	IN	PCIE_SOC_D2R_P<3..0>	NO_TEST=1
46 14	IN	PCIE_SOC_R2D_C_N<3..0>	NO_TEST=1
46 14	IN	PCIE_SOC_R2D_C_P<3..0>	NO_TEST=1

PCIE

19	IN	PCH_CLK24M_XTALOUT_R	NO_TEST=1
19 12	IN	PCH_CLK24M_XTALIN	NO_TEST=1
19 12	IN	PCH_CLK24M_XTALOUT	NO_TEST=1

Display MUX

DP

92 21	IN	DP_T_SNK1_ML_C_N<3..0>	NO_TEST=1
92 21	IN	DP_T_SNK1_ML_C_P<3..0>	NO_TEST=1
92 21	IN	DP_T_SNK0_ML_C_N<3..0>	NO_TEST=1
92 21	IN	DP_T_SNK0_ML_C_P<3..0>	NO_TEST=1
92 21	IN	DP_T_SNK1_AUXCH_C_N	NO_TEST=1
92 21	IN	DP_T_SNK1_AUXCH_C_P	NO_TEST=1
92 21	IN	DP_T_SNK0_AUXCH_C_N	NO_TEST=1
92 21	IN	DP_T_SNK0_AUXCH_C_P	NO_TEST=1
26 21	IN	DP_X_SNK1_ML_C_N<3..0>	NO_TEST=1
26 21	IN	DP_X_SNK1_ML_C_P<3..0>	NO_TEST=1
26 21	IN	DP_X_SNK0_ML_C_N<3..0>	NO_TEST=1
26 21	IN	DP_X_SNK0_ML_C_P<3..0>	NO_TEST=1
26 21	IN	DP_X_SNK1_AUXCH_C_N	NO_TEST=1
26 21	IN	DP_X_SNK1_AUXCH_C_P	NO_TEST=1
26 21	IN	DP_X_SNK0_AUXCH_C_N	NO_TEST=1
26 21	IN	DP_X_SNK0_AUXCH_C_P	NO_TEST=1

SSD

PCIE

78 77 76 75	IN	PCIE_SSD0_D2R_C_N<3..0>	NO_TEST=1
78 77 76 75	IN	PCIE_SSD0_D2R_C_P<3..0>	NO_TEST=1
78 77 76 75	IN	PCIE_SSD0_R2D_N<3..0>	NO_TEST=1
78 77 76 75	IN	PCIE_SSD0_R2D_P<3..0>	NO_TEST=1

Titan Ridges

PCIE

28 26	IN	PCIE_TBT_X_R2D_N<3..0>	NO_TEST=1
28 26	IN	PCIE_TBT_X_R2D_P<3..0>	NO_TEST=1
28 26	IN	PCIE_TBT_X_D2R_C_N<3..0>	NO_TEST=1
28 26	IN	PCIE_TBT_X_D2R_C_P<3..0>	NO_TEST=1
94 92	IN	PCIE_TBT_T_R2D_N<3..0>	NO_TEST=1
94 92	IN	PCIE_TBT_T_R2D_P<3..0>	NO_TEST=1
94 92	IN	PCIE_TBT_T_D2R_C_N<3..0>	NO_TEST=1
94 92	IN	PCIE_TBT_T_D2R_C_P<3..0>	NO_TEST=1

DP

26	IN	DP_X_SNK0_ML_N<3..0>	NO_TEST=1
26	IN	DP_X_SNK0_ML_P<3..0>	NO_TEST=1
26	IN	DP_X_SNK0_AUXCH_N	NO_TEST=1
26	IN	DP_X_SNK0_AUXCH_P	NO_TEST=1
26	IN	DP_X_SNK1_ML_N<3..0>	NO_TEST=1
26	IN	DP_X_SNK1_ML_P<3..0>	NO_TEST=1
26	IN	DP_X_SNK1_AUXCH_N	NO_TEST=1
26	IN	DP_X_SNK1_AUXCH_P	NO_TEST=1
92	IN	DP_T_SNK0_ML_N<3..0>	NO_TEST=1
92	IN	DP_T_SNK0_ML_P<3..0>	NO_TEST=1
92	IN	DP_T_SNK0_AUXCH_N	NO_TEST=1
92	IN	DP_T_SNK0_AUXCH_P	NO_TEST=1
92	IN	DP_T_SNK1_ML_N<3..0>	NO_TEST=1
92	IN	DP_T_SNK1_ML_P<3..0>	NO_TEST=1
92	IN	DP_T_SNK1_AUXCH_N	NO_TEST=1
92	IN	DP_T_SNK1_AUXCH_P	NO_TEST=1

USB-C

31 26	IN	USBC_XA_D2R_N<2..1>	NO_TEST=1
31 26	IN	USBC_XA_D2R_P<2..1>	NO_TEST=1
31 26	IN	USBC_XA_R2D_C_N<2..1>	NO_TEST=1
31 26	IN	USBC_XA_R2D_C_P<2..1>	NO_TEST=1
31 26	IN	USBC_XB_D2R_N<2..1>	NO_TEST=1
31 26	IN	USBC_XB_D2R_P<2..1>	NO_TEST=1
31 26	IN	USBC_XB_R2D_C_N<2..1>	NO_TEST=1
31 26	IN	USBC_XB_R2D_C_P<2..1>	NO_TEST=1
97 92	IN	USBC_TA_D2R_N<2..1>	NO_TEST=1
97 92	IN	USBC_TA_D2R_P<2..1>	NO_TEST=1
97 92	IN	USBC_TA_R2D_C_N<2..1>	NO_TEST=1
97 92	IN	USBC_TA_R2D_C_P<2..1>	NO_TEST=1
97 92	IN	USBC_TB_D2R_N<2..1>	NO_TEST=1
97 92	IN	USBC_TB_D2R_P<2..1>	NO_TEST=1
97 92	IN	USBC_TB_R2D_C_N<2..1>	NO_TEST=1
97 92	IN	USBC_TB_R2D_C_P<2..1>	NO_TEST=1

XTAL

28 26	IN	TBT_X_XTAL25M_OUT	NO_TEST=1
28 26	IN	TBT_X_XTAL25M_IN	NO_TEST=1
28	IN	TBT_X_XTAL25M_OUT_R	NO_TEST=1

Madea

DP

91 90	IN	LPDPTX_DATA_N<3..0>	NO_TEST=1
91 90	IN	LPDPTX_DATA_P<3..0>	NO_TEST=1
91 90	IN	LPDPTX_AUX_N	NO_TEST=1
91 90	IN	LPDPTX_AUX_P	NO_TEST=1

HDMI

90 89	IN	HDMI_DATA_N<2..0>	NO_TEST=1
90 89	IN	HDMI_DATA_P<2..0>	NO_TEST=1
89 88	IN	HDMI_DATA_CONN_N<2..0>	NO_TEST=1
89 88	IN	HDMI_DATA_CONN_P<2..0>	NO_TEST=1
89 88	IN	HDMI_CLK_CONN_N	NO_TEST=1
89 88	IN	HDMI_CLK_CONN_P	NO_TEST=1
89	IN	HDMI_CLK_FLT_N	NO_TEST=1
89	IN	HDMI_CLK_FLT_P	NO_TEST=1
89	IN	HDMI_CLK_R_N	NO_TEST=1
89	IN	HDMI_CLK_R_P	NO_TEST=1
90 89	IN	HDMI_CLK_N	NO_TEST=1
90 89	IN	HDMI_CLK_P	NO_TEST=1

USB-C CONN

USB-C

31	IN	USBC_XA_D2R_RC_N<2..1>	NO_TEST=1
31	IN	USBC_XA_D2R_RC_P<2..1>	NO_TEST=1
31	IN	USBC_XA_R2D_RC_N<2..1>	NO_TEST=1
31	IN	USBC_XA_R2D_RC_P<2..1>	NO_TEST=1
31	IN	USBC_XA_D2R_CONN_N<2..1>	NO_TEST=1
31	IN	USBC_XA_D2R_CONN_P<2..1>	NO_TEST=1
31	IN	USBC_XA_R2D_CONN_N<2..1>	NO_TEST=1
31	IN	USBC_XA_R2D_CONN_P<2..1>	NO_TEST=1
31 28	IN	USBC_XA_USB_DBG_TOP_N	NO_TEST=1
31 28	IN	USBC_XA_USB_DBG_TOP_P	NO_TEST=1
31 28	IN	USBC_XA_USB_DBG_BOT_N	NO_TEST=1
31 28	IN	USBC_XA_USB_DBG_BOT_P	NO_TEST=1
31	IN	USBC_XB_D2R_RC_N<2..1>	NO_TEST=1
31	IN	USBC_XB_D2R_RC_P<2..1>	NO_TEST=1
31	IN	USBC_XB_R2D_RC_N<2..1>	NO_TEST=1
31	IN	USBC_XB_R2D_RC_P<2..1>	NO_TEST=1
31	IN	USBC_XB_D2R_CONN_N<2..1>	NO_TEST=1
31	IN	USBC_XB_D2R_CONN_P<2..1>	NO_TEST=1
31	IN	USBC_XB_R2D_CONN_N<2..1>	NO_TEST=1
31	IN	USBC_XB_R2D_CONN_P<2..1>	NO_TEST=1
31 30	IN	USBC_XB_USB_TOP_N	NO_TEST=1
31 30	IN	USBC_XB_USB_TOP_P	NO_TEST=1
31 30	IN	USBC_XB_USB_BOT_N	NO_TEST=1
31 30	IN	USBC_XB_USB_BOT_P	NO_TEST=1
97	IN	USBC_TA_D2R_RC_N<2..1>	NO_TEST=1
97	IN	USBC_TA_D2R_RC_P<2..1>	NO_TEST=1
97	IN	USBC_TA_R2D_RC_N<2..1>	NO_TEST=1
97	IN	USBC_TA_R2D_RC_P<2..1>	NO_TEST=1
97	IN	USBC_TA_D2R_CONN_N<2..1>	NO_TEST=1
97	IN	USBC_TA_D2R_CONN_P<2..1>	NO_TEST=1
97	IN	USBC_TA_R2D_CONN_N<2..1>	NO_TEST=1
97	IN	USBC_TA_R2D_CONN_P<2..1>	NO_TEST=1
97 95	IN	USBC_TA_USB_TOP_N	NO_TEST=1
97 95	IN	USBC_TA_USB_TOP_P	NO_TEST=1
97 95	IN	USBC_TA_USB_BOT_N	NO_TEST=1
97 95	IN	USBC_TA_USB_BOT_P	NO_TEST=1
97	IN	USBC_TB_D2R_RC_N<2..1>	NO_TEST=1
97	IN	USBC_TB_D2R_RC_P<2..1>	NO_TEST=1
97	IN	USBC_TB_R2D_RC_N<2..1>	NO_TEST=1
97	IN	USBC_TB_R2D_RC_P<2..1>	NO_TEST=1
97	IN	USBC_TB_D2R_CONN_N<2..1>	NO_TEST=1
97	IN	USBC_TB_D2R_CONN_P<2..1>	NO_TEST=1
97	IN	USBC_TB_R2D_CONN_N<2..1>	NO_TEST=1
97	IN	USBC_TB_R2D_CONN_P<2..1>	NO_TEST=1
97 96	IN	USBC_TB_USB_TOP_N	NO_TEST=1
97 96	IN	USBC_TB_USB_TOP_P	NO_TEST=1
97 96	IN	USBC_TB_USB_BOT_N	NO_TEST=1
97 96	IN	USBC_TB_USB_BOT_P	NO_TEST=1

Harpoon

ANT MATCH

36 35	IN	50_G_0_MATCH	NO_TEST=1
36 35	IN	50_A_0_MATCH	NO_TEST=1
36 35	IN	50_G_1_MATCH	NO_TEST=1
36 35	IN	50_A_1_MATCH	NO_TEST=1
36 35	IN	50_G_2_MATCH	NO_TEST=1
36 35	IN	50_A_2_MATCH	NO_TEST=1
36	IN	50_G_0_DIPLEXER	NO_TEST=1
36	IN	50_A_0_DIPLEXER	NO_TEST=1
36	IN	50_G_1_DIPLEXER	NO_TEST=1
36	IN	50_A_1_DIPLEXER	NO_TEST=1
36	IN	50_G_2_DIPLEXER	NO_TEST=1
36	IN	50_A_2_DIPLEXER	NO_TEST=1
36	IN	50_0_COM	NO_TEST=1
38	IN	50_0_ANT	NO_TEST=1
38	IN	50_1_COM	NO_TEST=1
38	IN	50_1_ANT	NO_TEST=1
36	IN	50_2_COM	NO_TEST=1
36	IN	50_2_ANT	NO_TEST=1

PCIE

35	IN	PCH_PCIE_WLAN_D2R_C_N	NO_TEST=1
35	IN	PCH_PCIE_WLAN_D2R_C_P	NO_TEST=1
35	IN	PCH_PCIE_WLAN_R2D_N	NO_TEST=1
35	IN	PCH_PCIE_WLAN_R2D_P	NO_TEST=1

BOM_COST_GROUP=PCB

H9M

PCIE

46 40	IN	PCIE_SOC_R2D_N<3..0>	NO_TEST=1
46 40	IN	PCIE_SOC_R2D_P<3..0>	NO_TEST=1
40	IN	PCIE_SOC_D2R_C_N<3..0>	NO_TEST=1
40	IN	PCIE_SOC_D2R_C_P<3..0>	NO_TEST=1

SSD PCIE

78 77 76 75 40	IN	PCIE_SSD0_D2R_N<3..0>	NO_TEST=1
78 77 76 75 40	IN	PCIE_SSD0_D2R_P<3..0>	NO_TEST=1
78 77 76 75 40	IN	PCIE_SSD0_R2D_C_N<3..0>	NO_TEST=1
78 77 76 75 40	IN	PCIE_SSD0_R2D_C_P<3..0>	NO_TEST=1

ESPI

38	IN	ESPI_IO_R<3..0>	NO_TEST=1
113 38 12	IN	ESPI_IO<3..0>	NO_TEST=1
113 38 12	IN	ESPI_CLK	NO_TEST=1
12	IN	ESPI_CLK60M_R	NO_TEST=1

XTAL

37	IN	SOC_XTAL24M_OUT	NO_TEST=1
37	IN	SOC_XTAL24M_IN	NO_TEST=1
37	IN	SOC_XTAL24M_OUT_R	NO_TEST=1

ENET

PCIE

81 80	IN	PCIE_ENET_1G_D2R_C_N	NO_TEST=1
81 80	IN	PCIE_ENET_1G_D2R_C_P	NO_TEST=1
81 80	IN	PCIE_ENET_1G_R2D_N	NO_TEST=1
81 80	IN	PCIE_ENET_1G_R2D_P	NO_TEST=1
84 82	IN	PCIE_ENET_D2R_C_P<3..0>	NO_TEST=1
84 82	IN	PCIE_ENET_D2R_C_N<3..0>	NO_TEST=1
84 82	IN	PCIE_ENET_R2D_N<3..0>	NO_TEST=1
84 82	IN	PCIE_ENET_R2D_P<3..0>	NO_TEST=1

MDI

85 80	IN	ENETCONN_MDI_N<3..0>	NO_TEST=1
85 80	IN	ENETCONN_MDI_P<3..0>	NO_TEST=1
85	IN	ENET_A_N_R	NO_TEST=1
85	IN	ENET_A_P_R	NO_TEST=1
85	IN	ENET_A_CMC_N	NO_TEST=1
85	IN	ENET_A_CMC_P	NO_TEST=1
107 85	IN	ENET_CONN_A_N	NO_TEST=1
107 85	IN	ENET_CONN_A_P	NO_TEST=1
85	IN	ENET_B_N_R	NO_TEST=1
85	IN	ENET_B_P_R	NO_TEST=1
85	IN	ENET_B_CMC_N	NO_TEST=1
85	IN	ENET_B_CMC_P	NO_TEST=1
107 85	IN	ENET_CONN_B_N	NO_TEST=1
107 85	IN	ENET_CONN_B_P	NO_TEST=1
85	IN	ENET_C_N_R	NO_TEST=1
85	IN	ENET_C_P_R	NO_TEST=1
85	IN	ENET_C_CMC_N	NO_TEST=1
85	IN	ENET_C_CMC_P	NO_TEST=1
107 85	IN	ENET_CONN_C_N	NO_TEST=1
107 85	IN	ENET_CONN_C_P	NO_TEST=1
85	IN	ENET_D_N_R	NO_TEST=1
85	IN	ENET_D_P_R	NO_TEST=1
85	IN	ENET_D_CMC_N	NO_TEST=1
85	IN	ENET_D_CMC_P	NO_TEST=1
107 85	IN	ENET_CONN_D_N	NO_TEST=1
107 85	IN	ENET_CONN_D_P	NO_TEST=1
85 82	IN	ENET_A_N	NO_TEST=1
85 82	IN	ENET_A_P	NO_TEST=1
85 82	IN	ENET_B_N	NO_TEST=1
85 82	IN	ENET_B_P	NO_TEST=1
85 82	IN	ENET_C_N	NO_TEST=1
85 82	IN	ENET_C_P	NO_TEST=1
85 82	IN	ENET_D_N	NO_TEST=1
85 82	IN	ENET_D_P	NO_TEST=1

PAGE TITLE

High speed No Testpoints

Apple Inc.

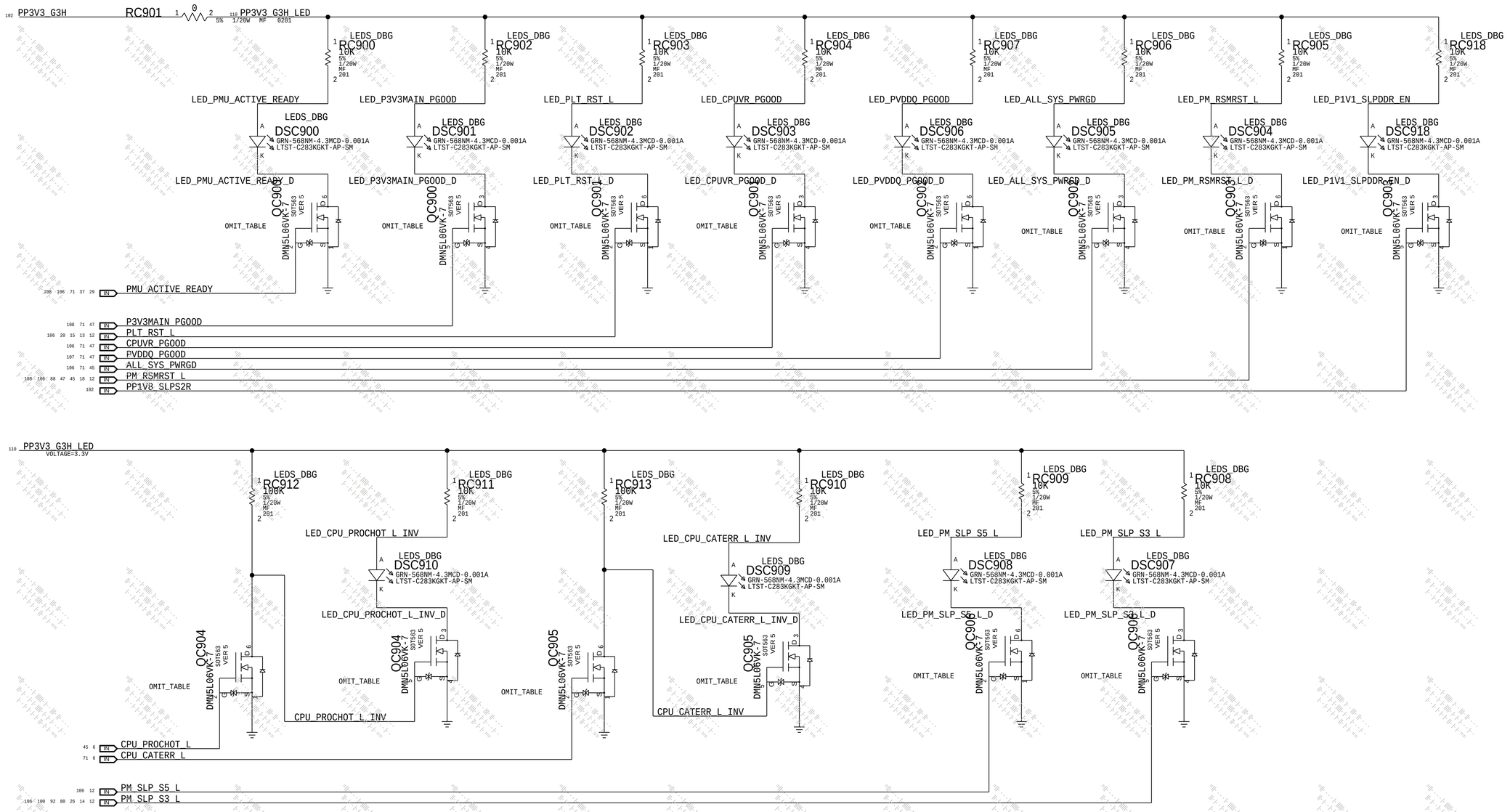
DRAWING NUMBER 051-02424 | SIZE D

REVISION 6.0.0

BRANCH dvt-1

PAGE 127 OF 142

SHEET 109 OF 115



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00074	7	dual FET	QC900,QC901,QC902,QC903,QC904,QC905,QC906	CRITICAL	LEDS_DBG

BOM_COST_GROUP=DEBUG

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

DEBUG LEDS

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

BRANCH dvt-1

PAGE 129 OF 142

SHEET 110 OF 115

BOM_COST_GROUP=PCB

PAGE TITLE

Constraints

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DRAWING NUMBER 051-02424

SIZE D

REVISION 6.0.0

BRANCH dvt-1

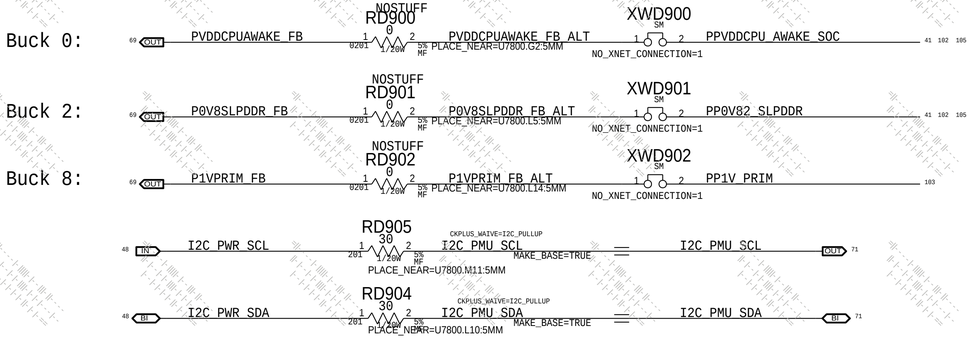
PAGE 130 OF 142

SHEET 111 OF 115

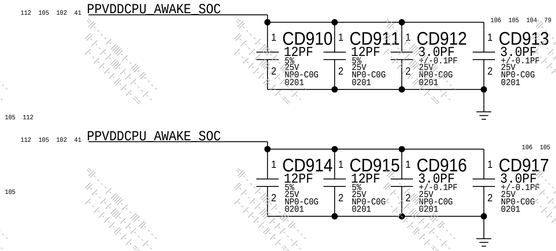
Calpe Dev Support:

Alternate Feedback:remote sense

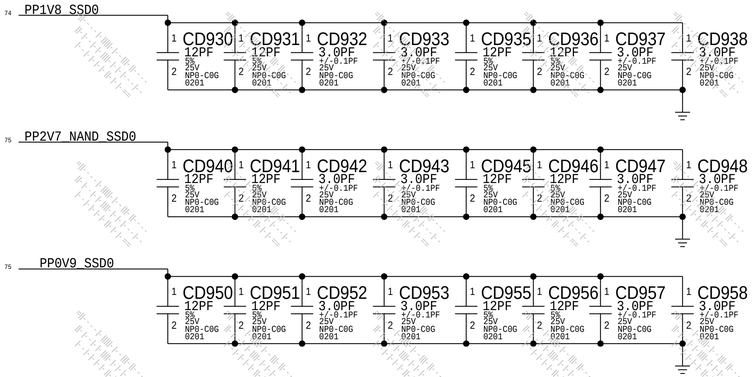
Place RD900,RD901 and RD902 to close FB pins to minimize stubs.



H9ML Desense Caps:



SSD/NAND Desense Caps:



BOM_COST_GROUP=DEBUG

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: Dev Support 1

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

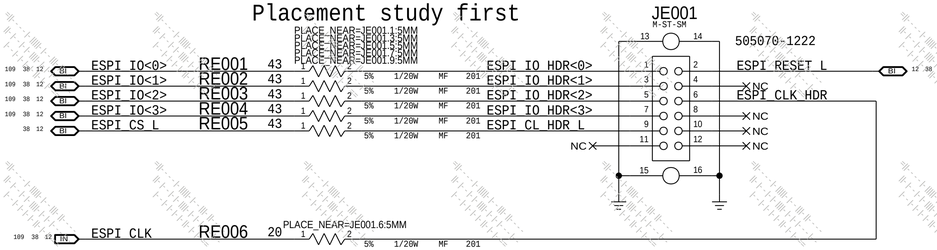
BRANCH: dvt-1

PAGE: 139 OF 142

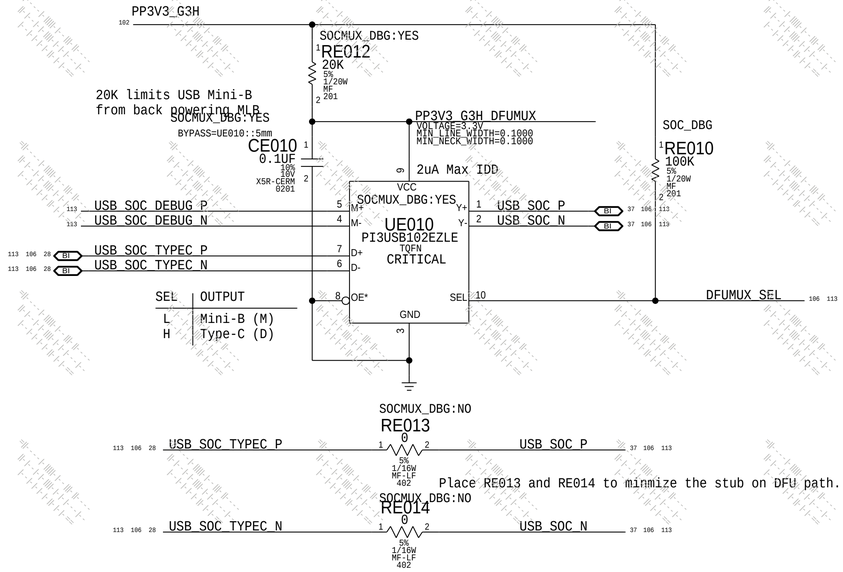
SHEET: 112 OF 115

eSPI Analyzer

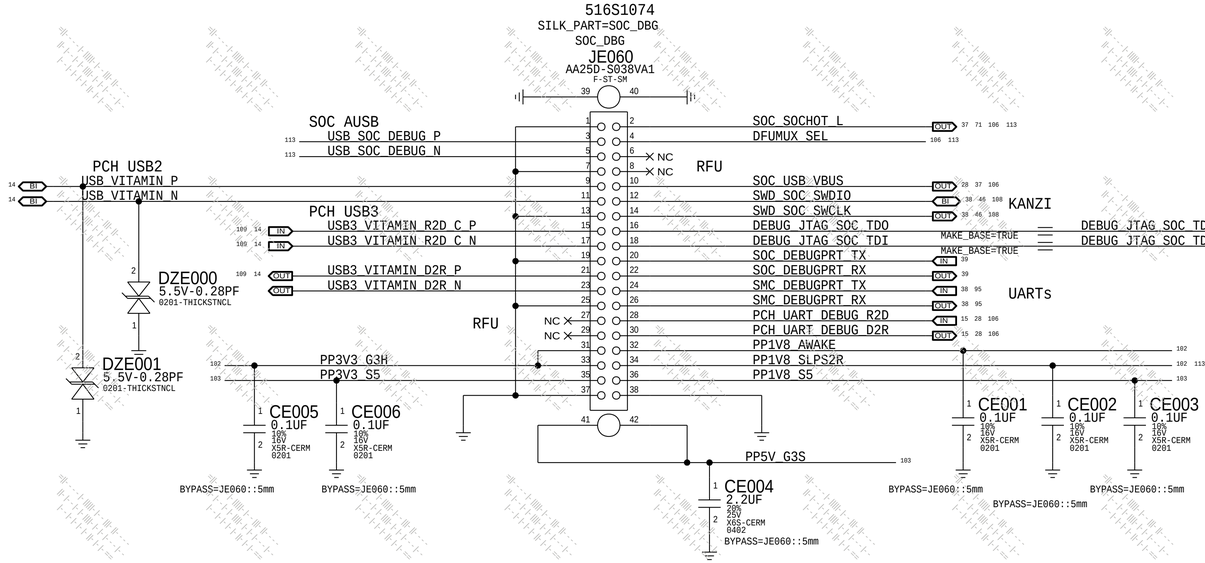
Placement study first



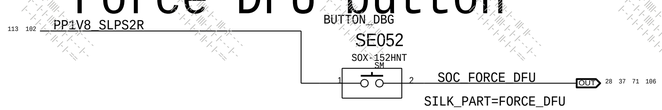
SoC USB DFU Mux



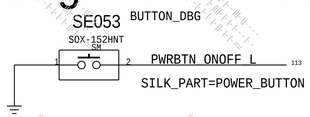
SOC DEBUG Connector



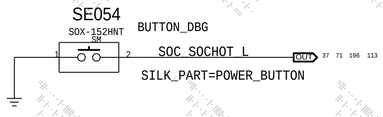
Force DFU button

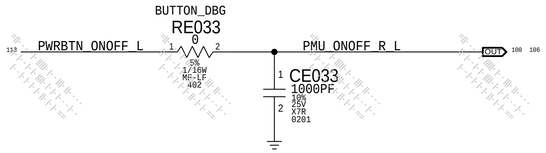


Debug Power button



PMU Reset button





BOM_COST_GROUP=DEBUG

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: Dev Support 2

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 140 OF 142

SHEET: 113 OF 115

	BOM NUMBER	BOM NAME	BOM OPTIONS	
-->	639-06831	PCBA,MLB,3.6G_4C,X1036,128G_WD,ENET_1G	COMM_BOM,CPU:3.6G,SSD:128_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
	639-06830	PCBA,MLB,3.6G_4C,X1036,128G_TB,ENET_1G	COMM_BOM,CPU:3.6G,SSD:128_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06849	PCBA,MLB,3.6G_4C,X1036,256G_WD,ENET_1G	COMM_BOM,CPU:3.6G,SSD:256_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06832	PCBA,MLB,3.6G_4C,X1036,256G_TB,ENET_1G	COMM_BOM,CPU:3.6G,SSD:256_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06833	PCBA,MLB,3.6G_4C,X1036,512G_WD,ENET_1G	COMM_BOM,CPU:3.6G,SSD:512_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06834	PCBA,MLB,3.6G_4C,X1036,512G_TB,ENET_1G	COMM_BOM,CPU:3.6G,SSD:512_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06835	PCBA,MLB,3.6G_4C,X1036,1TB_WD,ENET_1G	COMM_BOM,CPU:3.6G,SSD:1T_SD,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06836	PCBA,MLB,3.6G_4C,X1036,1TB_TB,ENET_1G	COMM_BOM,CPU:3.6G,SSD:1T_TB,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06837	PCBA,MLB,3.6G_4C,X1036,2TB_SM,ENET_1G	COMM_BOM,CPU:3.6G,SSD:2T_SM,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
3.6GHz, ENET_10G->				
	639-06838	PCBA,MLB,3.6G_4C,X1036,128G_WD,ENET_10G	COMM_BOM,CPU:3.6G,SSD:128_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-
	639-06839	PCBA,MLB,3.6G_4C,X1036,128G_TB,ENET_10G	COMM_BOM,CPU:3.6G,SSD:128_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06840	PCBA,MLB,3.6G_4C,X1036,256G_WD,ENET_10G	COMM_BOM,CPU:3.6G,SSD:256_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06841	PCBA,MLB,3.6G_4C,X1036,256G_TB,ENET_10G	COMM_BOM,CPU:3.6G,SSD:256_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06842	PCBA,MLB,3.6G_4C,X1036,512G_WD,ENET_10G	COMM_BOM,CPU:3.6G,SSD:512_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06843	PCBA,MLB,3.6G_4C,X1036,512G_TB,ENET_10G	COMM_BOM,CPU:3.6G,SSD:512_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06844	PCBA,MLB,3.6G_4C,X1036,1TB_WD,ENET_10G	COMM_BOM,CPU:3.6G,SSD:1T_SD,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06845	PCBA,MLB,3.6G_4C,X1036,1TB_TB,ENET_10G	COMM_BOM,CPU:3.6G,SSD:1T_TB,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06846	PCBA,MLB,3.6G_4C,X1036,2TB_SM,ENET_10G	COMM_BOM,CPU:3.6G,SSD:2T_SM,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-
2.8GHz, ENET_1G->				
	639-05191	PCBA,MLB,2.8G,X1036,128G_WD,ENET_1G	COMM_BOM,CPU:2.8G,SSD:128_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
	639-05383	PCBA,MLB,2.8G,X1036,128G_TB,ENET_1G	COMM_BOM,CPU:2.8G,SSD:128_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05177	PCBA,MLB,2.8G,X1036,256G_WD,ENET_1G	COMM_BOM,CPU:2.8G,SSD:256_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05385	PCBA,MLB,2.8G,X1036,256G_TB,ENET_1G	COMM_BOM,CPU:2.8G,SSD:256_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05387	PCBA,MLB,2.8G,X1036,512G_WD,ENET_1G	COMM_BOM,CPU:2.8G,SSD:512_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05391	PCBA,MLB,2.8G,X1036,512G_TB,ENET_1G	COMM_BOM,CPU:2.8G,SSD:512_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05393	PCBA,MLB,2.8G,X1036,1TB_WD,ENET_1G	COMM_BOM,CPU:2.8G,SSD:1T_SD,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05397	PCBA,2.8G,MLB,X1036,1TB_TB,ENET_1G	COMM_BOM,CPU:2.8G,SSD:1T_TB,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05959	PCBA,MLB,2.8GHz,X1036,2TB_SM,ENET_1G	COMM_BOM,CPU:2.8G,SSD:2T_SM,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
2.8GHz, ENET_10G->				
	639-05189	PCBA,MLB,2.8G,X1036,128G_WD,ENET_10G	COMM_BOM,CPU:2.8G,SSD:128_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-
	639-05384	PCBA,MLB,2.8G,X1036,128G_TB,ENET_10G	COMM_BOM,CPU:2.8G,SSD:128_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05175	PCBA,MLB,2.8G,X1036,256G_WD,ENET_10G	COMM_BOM,CPU:2.8G,SSD:256_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05386	PCBA,MLB,2.8G,X1036,256G_TB,ENET_10G	COMM_BOM,CPU:2.8G,SSD:256_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05388	PCBA,MLB,2.8G,X1036,512G_WD,ENET_10G	COMM_BOM,CPU:2.8G,SSD:512_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05392	PCBA,MLB,2.8G,X1036,512G_TB,ENET_10G	COMM_BOM,CPU:2.8G,SSD:512_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05394	PCBA,MLB,2.8G,X1036,1TB_WD,ENET_10G	COMM_BOM,CPU:2.8G,SSD:1T_SD,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05398	PCBA,2.8G,MLB,X1036,1TB_TB,ENET_10G	COMM_BOM,CPU:2.8G,SSD:1T_TB,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05958	PCBA,MLB,2.8GHz,X1036,2TB_SM,ENET_10G	COMM_BOM,CPU:2.8G,SSD:2T_SM,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-
3.0GHz, ENET_1G->				
	639-05971	PCBA,MLB,3.0GHz,X1036,256G_SD,ENET_1G	COMM_BOM,CPU:3.0G,SSD:256_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
	639-05969	PCBA,MLB,3.0GHz,X1036,256G_TB,ENET_1G	COMM_BOM,CPU:3.0G,SSD:256_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05977	PCBA,MLB,3.0GHz,X1036,512G_SD,ENET_1G	COMM_BOM,CPU:3.0G,SSD:512_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05975	PCBA,MLB,3.0GHz,X1036,512G_TB,ENET_1G	COMM_BOM,CPU:3.0G,SSD:512_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05983	PCBA,MLB,3.0GHz,X1036,1T_SD,ENET_1G	COMM_BOM,CPU:3.0G,SSD:1T_SD,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05981	PCBA,MLB,3.0GHz,X1036,1T_TB,ENET_1G	COMM_BOM,CPU:3.0G,SSD:1T_TB,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05985	PCBA,MLB,3.0GHz,X1036,2T_SM,ENET_1G	COMM_BOM,CPU:3.0G,SSD:2T_SM,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
3.0GHz, ENET_10G->				
	639-05968	PCBA,MLB,3.0GHz,X1036,256G_SD,ENET_10G	COMM_BOM,CPU:3.0G,SSD:256_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-
	639-05966	PCBA,MLB,3.0GHz,X1036,256G_TB,ENET_10G	COMM_BOM,CPU:3.0G,SSD:256_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05974	PCBA,MLB,3.0GHz,X1036,512G_SD,ENET_10G	COMM_BOM,CPU:3.0G,SSD:512_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05972	PCBA,MLB,3.0GHz,X1036,512G_TB,ENET_10G	COMM_BOM,CPU:3.0G,SSD:512_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05980	PCBA,MLB,3.0GHz,X1036,1T_SD,ENET_10G	COMM_BOM,CPU:3.0G,SSD:1T_SD,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05978	PCBA,MLB,3.0GHz,X1036,1T_TB,ENET_10G	COMM_BOM,CPU:3.0G,SSD:1T_TB,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05984	PCBA,MLB,3.0GHz,X1036,2T_SM,ENET_10G	COMM_BOM,CPU:3.0G,SSD:2T_SM,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-
3.2GHz, ENET_1G->				
	639-05997	PCBA,MLB,3.2GHz,X1036,256G_SD,ENET_1G	COMM_BOM,CPU:3.2G,SSD:256_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
	639-05995	PCBA,MLB,3.2GHz,X1036,256G_TB,ENET_1G	COMM_BOM,CPU:3.2G,SSD:256_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06003	PCBA,MLB,3.2GHz,X1036,512G_SD,ENET_1G	COMM_BOM,CPU:3.2G,SSD:512_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06001	PCBA,MLB,3.2GHz,X1036,512G_TB,ENET_1G	COMM_BOM,CPU:3.2G,SSD:512_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06009	PCBA,MLB,3.2GHz,X1036,1T_SD,ENET_1G	COMM_BOM,CPU:3.2G,SSD:1T_SD,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06007	PCBA,MLB,3.2GHz,X1036,1T_TB,ENET_1G	COMM_BOM,CPU:3.2G,SSD:1T_TB,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06011	PCBA,MLB,3.2GHz,X1036,2T_SM,ENET_1G	COMM_BOM,CPU:3.2G,SSD:2T_SM,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
3.2GHz, ENET_10G->				
	639-05994	PCBA,MLB,3.2GHz,X1036,256G_SD,ENET_10G	COMM_BOM,CPU:3.2G,SSD:256_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-
	639-05992	PCBA,MLB,3.2GHz,X1036,256G_TB,ENET_10G	COMM_BOM,CPU:3.2G,SSD:256_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06000	PCBA,MLB,3.2GHz,X1036,512G_SD,ENET_10G	COMM_BOM,CPU:3.2G,SSD:512_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05998	PCBA,MLB,3.2GHz,X1036,512G_TB,ENET_10G	COMM_BOM,CPU:3.2G,SSD:512_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06006	PCBA,MLB,3.2GHz,X1036,1T_SD,ENET_10G	COMM_BOM,CPU:3.2G,SSD:1T_SD,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06004	PCBA,MLB,3.2GHz,X1036,1T_TB,ENET_10G	COMM_BOM,CPU:3.2G,SSD:1T_TB,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06010	PCBA,MLB,3.2GHz,X1036,2T_SM,ENET_10G	COMM_BOM,CPU:3.2G,SSD:2T_SM,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-

BOM Variants

3.6GHz 4C
ENET_1G

3.6GHz 4C
ENET_10G

2.8GHz 6C
ENET_1G

2.8GHz 6C
ENET_10G

3.0GHz 6C
ENET_1G

3.0GHz 6C
ENET_10G

3.2GHz 6C
ENET_1G

3.3GHz 6C
ENET_10G

Note:SSD SD and WD are the same

BOM_COST_GROUP=PCB

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
639 BOM Configuration 1

Apple Inc.

DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 141 OF 142
SHEET 114 OF 115

X1036 BOM Groups

BOM GROUP	BOM OPTIONS
X1036_COMMON_ALL	ALTERNATE,COMMON,X1036_COMMON1,X1036_COMMON2,X1036_COMMON3,X1036_DEFAULT
X1036_DEFAULT	SSD0_NAND_VCC:2.5V,ALL_SYS_PGD:1V8,SPIHOLD:H9M,CPUPEG:X8X4X4
X1036_COMMON1	X1036_PROGRAMMABLE:ENG,X1036_MODULE_PARTS:ENG,X1036_REV:DVT
X1036_COMMON2	X1036_HDMI,X1036_ID
X1036_COMMON3	LOADISNS,VR_BULKCAP:CURRENT,SENSOR:DEV,LOADRC:YES,ENGISNS:YES,XDP:YES
X1036_ENG:NO	FAN_DBG
X1036_ENG:YES	XDP_CONN,WIFI_DBG,USBC_DBG,SOC_DBG,SSD_DBG,LEDS_DBG,SOCMUX_DBG:YES,BUTTON_DBG
X1036_PROGRAMMABLE:ENG	TBT_T_ROM:DVT,TBT_X_ROM:DVT,BT_FLASH:DVT,WLAN_EEPROM:DVT,SOC_ROM:BLANK,SEPROM:OG,HDMI_ROM:DVT
X1036_MODULE_PARTS:ENG	PCH:PRQ,TBT_TR:C1,ACE:C0,PMU:A0_C,WIFI:ES7,HDMI:A4
X1036_HDMI	CLK_FILT,DATA_FILT,HDMI_RST:OD
X1036_ENET_10G	ENET:10G,10G_ENET:B1,10G_ENET_ROM:DVT,ENET_REFCLK:OSC
X1036_ENET_1G	ENET:1G,1G_ENET:A0,1G_ENET_ROM:DVT
X1036_ID	BOARDID1,BOARDID2,BOARDID3
X1036_REV:DVT	BOARDREV2,BOARDREV1,BOARDREV0
X1036_DEVEL:DVT	X1036_ENG:YES,ALTERNATE
X1036_DEV_1G_ENET	LED_1G_ENET_DBG,ALTERNATE
X1036_DEV_10G_ENET	DEBUG_LEDS:10G,ALTERNATE

COMMON BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00130	COMMON PARTS,MLB,X1036	X1036_COMMON_ALL

DEV BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
985-00836	DEV(DEBUG)_COMMON PARTS,MLB,X1036	X1036_DEVEL:DVT
985-00853	1G ENET DEV/DEBUG PARTS,MLB,X1036	X1036_DEV_1G_ENET
985-00854	10G ENET DEV/DEBUG PARTS,MLB,X1036	X1036_DEV_10G_ENET

BOM VARIATION

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
985-00836	1	COMMON DEV/DEBUG,MLB,X1036	DEVEL	CRITICAL	DEV_BOM
685-00130	1	COMMON PARTS,MLB,X1036	COMM	CRITICAL	COMM_BOM
985-00853	1	1G ENET DEBUG,MLB,X1036	1G_DEVEL		1GDBG_BOM
985-00854	1	10G ENET DEBUG,MLB,X1036	10G_DEVEL		10GDBG_BOM

Alternatives section 2

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
128S00042	128S0329	ALL	CB200 etc rdr 37042037	
128S0311	128S0329	ALL	CB200 etc rdr 37042037	
353S00107	353S3239	ALL	U5400 erc rdr 37173893	
353S1429	353S3239	ALL	U5540 erc rdr 37175030	
107S00055	107S00090	ALL	U5540 erc rdr 37175230	
107S00056	107S00086	ALL	R5430 erc rdr 37175329	
107S0276	107S00020	ALL	R5600 erc rdr 37175569	
103S0321	103S0276	ALL	R5545 erc rdr 38515379	
138S0775	138S0860	ALL	C3198 etc rdr 38305368	
138S00049	138S0831	ALL	C8611 etc rdr 38306891	
311S00192	311S00191	ALL	U8312 etc rdr 37077481	
138S00024	138S0986	ALL	C3701/2/3 rdr 37399555	
103S00248	103S00247	ALL	R9000 rdr 38514938	
103S00250	103S00249	ALL	R9001/3 rdr 38515246	
128S0364	128S00081	ALL	C6482/3 rdr 37292870	
128S0264	128S00081	ALL	C6482/3 rdr 37292870	
377S00103	377S00138	ALL	DZB801/2 rdr 36419223	
377S0124	377S00138	ALL	DZB801/2 rdr 36419223	
138S00013	138S0772	ALL	C9921 rdr 38080947	ENET:10G
118S00093	118S00092	ALL	RA720 etc rdr 38513679	
138S0945	138S0706	ALL	C6360 etc rdr 38310616	
155S0387	155S0694	ALL	LA601 etc rdr 39358850	
155S00204	155S0731	ALL	FLA800 etc rdr 39359536	
138S00084	138S00060	ALL	C2950 etc rdr 38312295	
371S00085	371S00190	ALL	D3100 etc rdr 39225721	
138S00262	138S0806	ALL	C6000 rdr 39360099	

BOM_COST_GROUP=PCB

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: 639 BOM Configuration 2

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 142 OF 142

SHEET: 115 OF 115