MS-1681 Ver : 2.0

Calpella Platform

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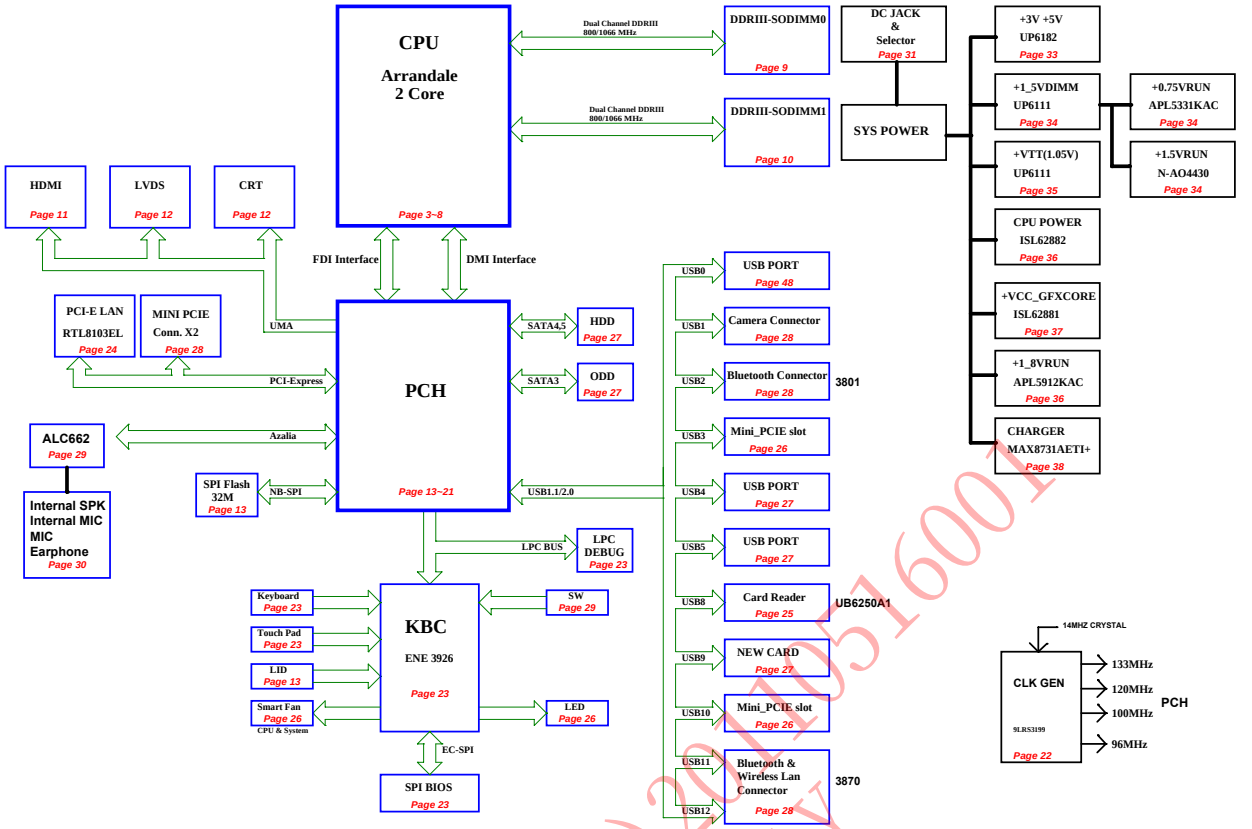

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BLOCK DIAGRAM
MS-1681

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	LAN
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	DDRIII core
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDRIII command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	Graphics core rail (Dual Core only)

Net Naming Conventions

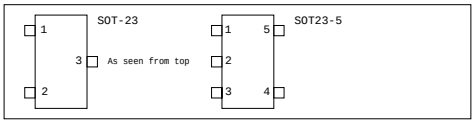
Suffix

\# = Active Low Signal

Prefix

H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

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Title: PLATFORM

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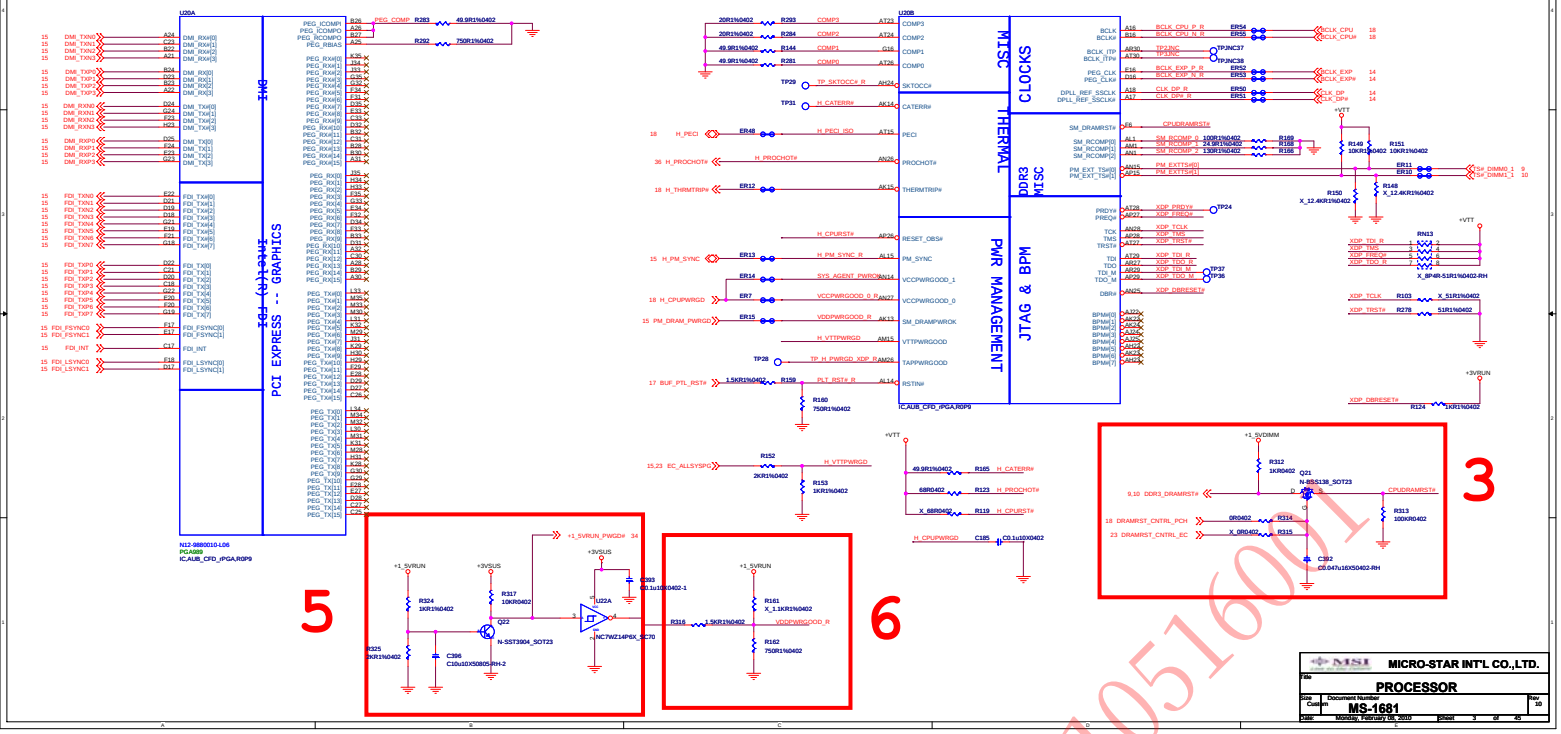
ARRANDALE PROCESSOR (CLK,MISC,JTAG)



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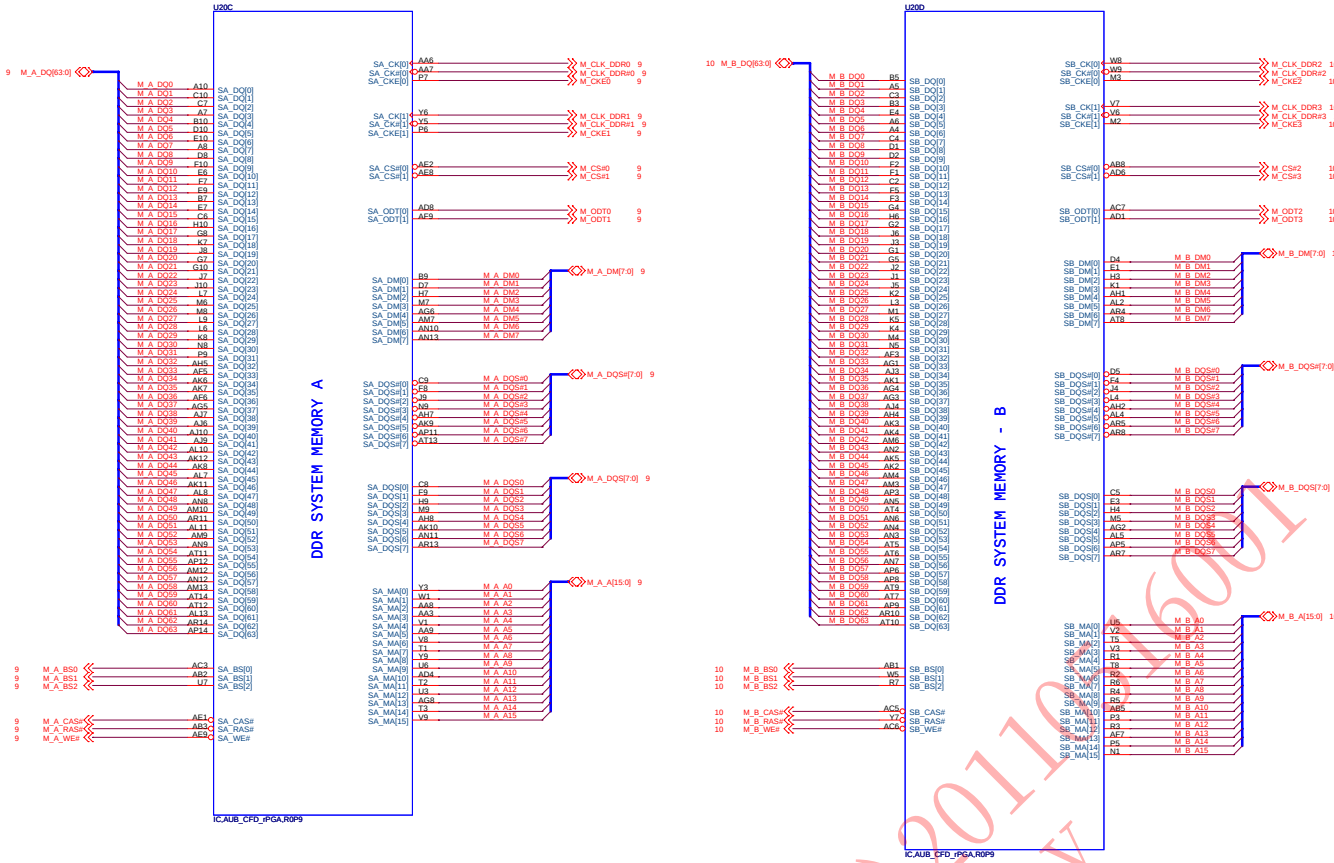
ARRANDALE PROCESSOR (DDR3)



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Title: DDR3

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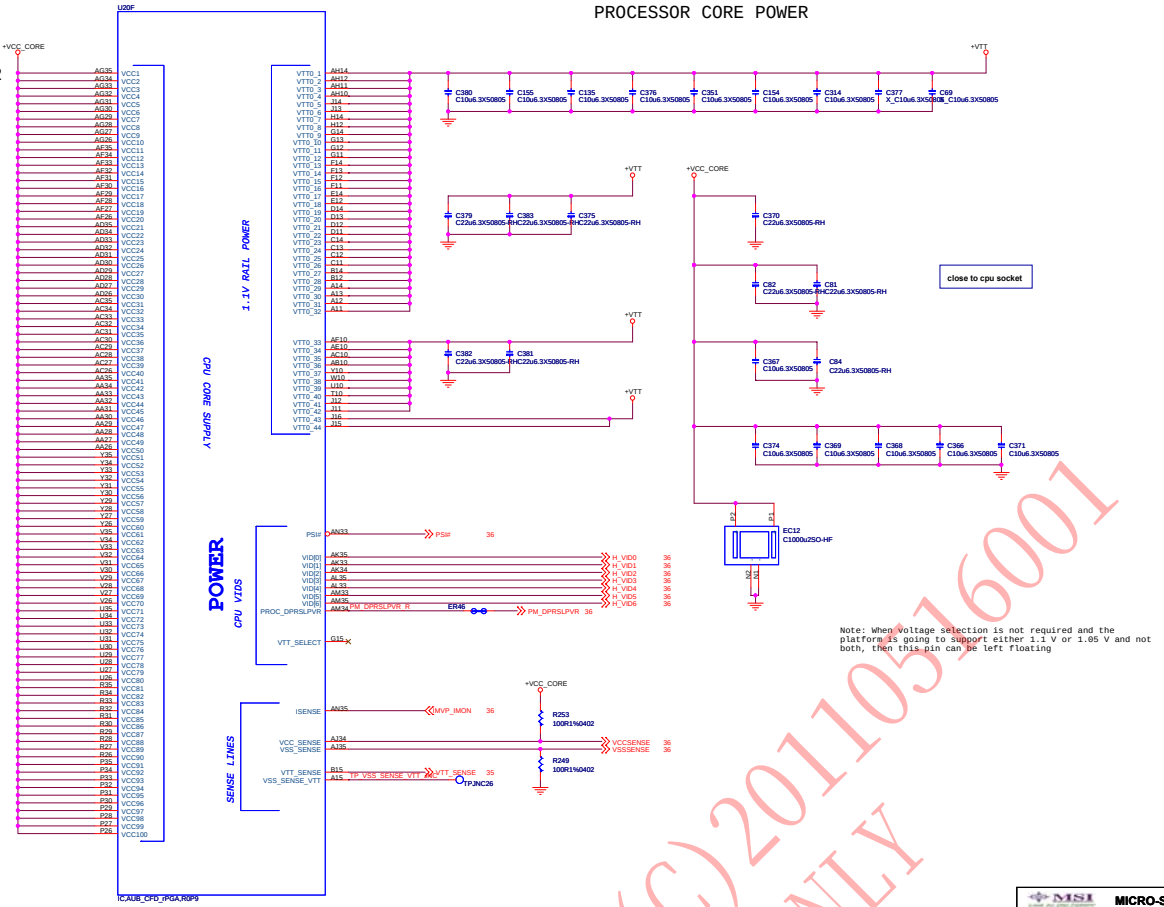
ARRANDALE PROCESSOR (POWER)

PROCESSOR CORE POWER



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Title: PROCESSOR POWER

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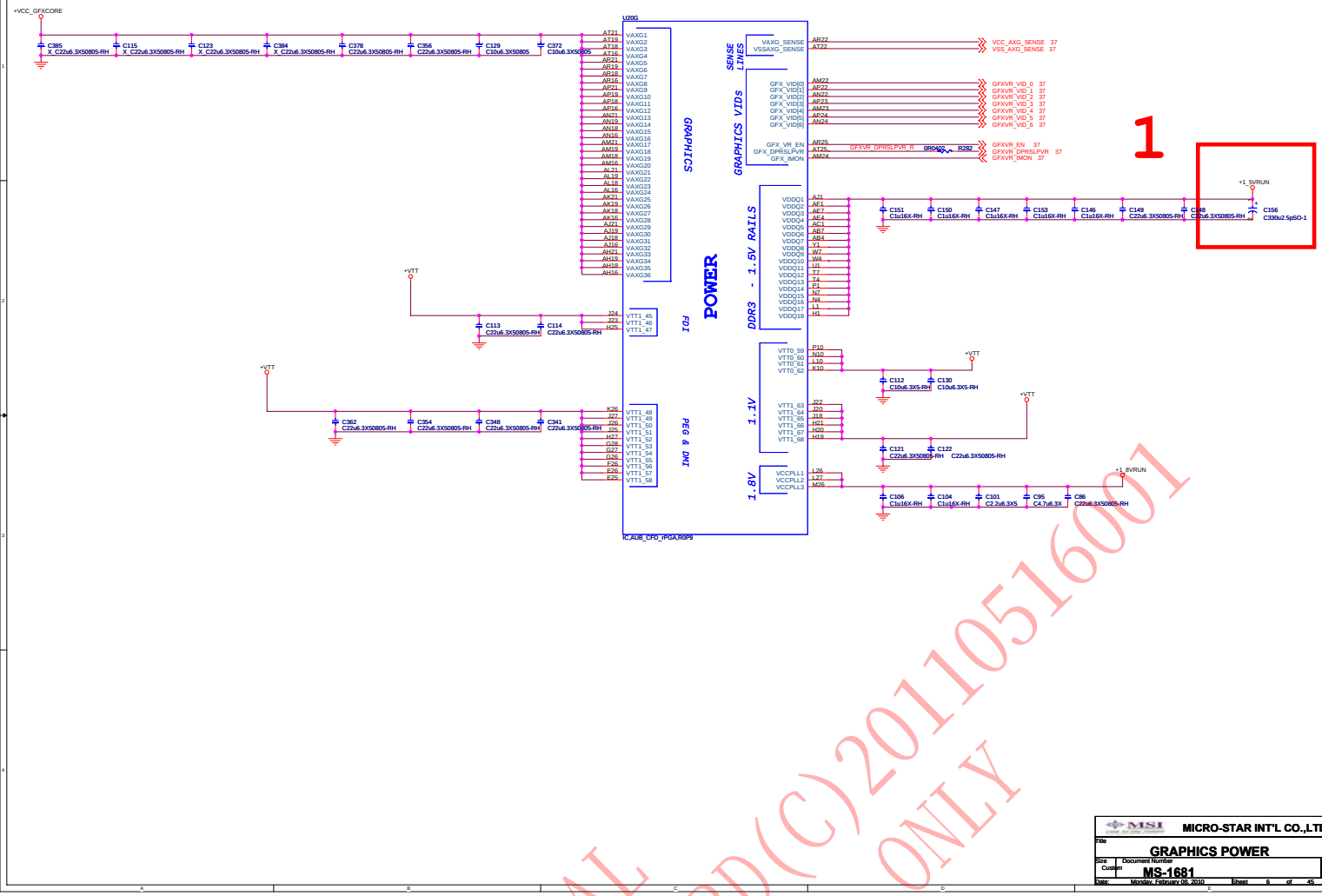
ARRANDALE PROCESSOR (GRAPHICS POWER)



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Title: GRAPHICS POWER

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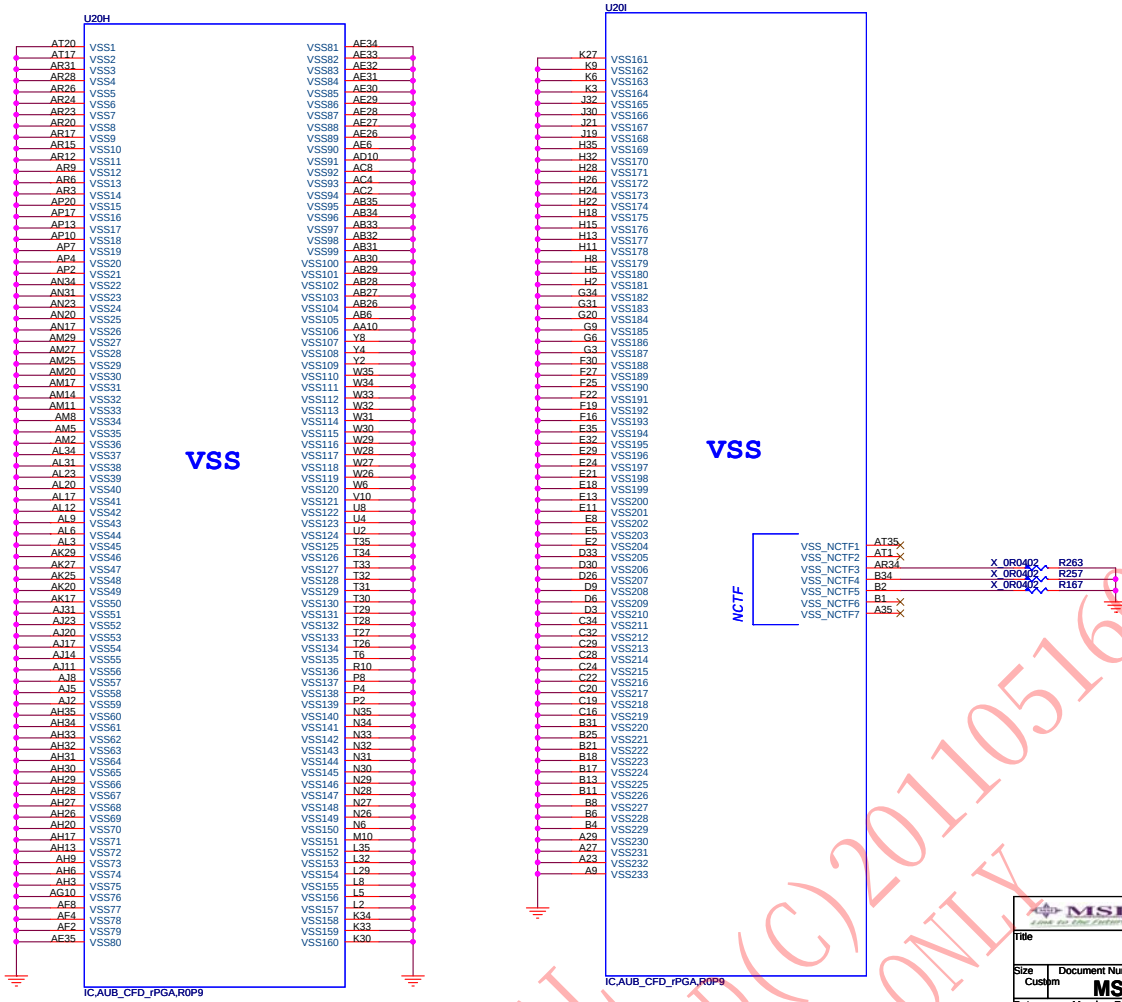
ARRANDALE PROCESSOR (GND)



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Title: PROCESSOR GND

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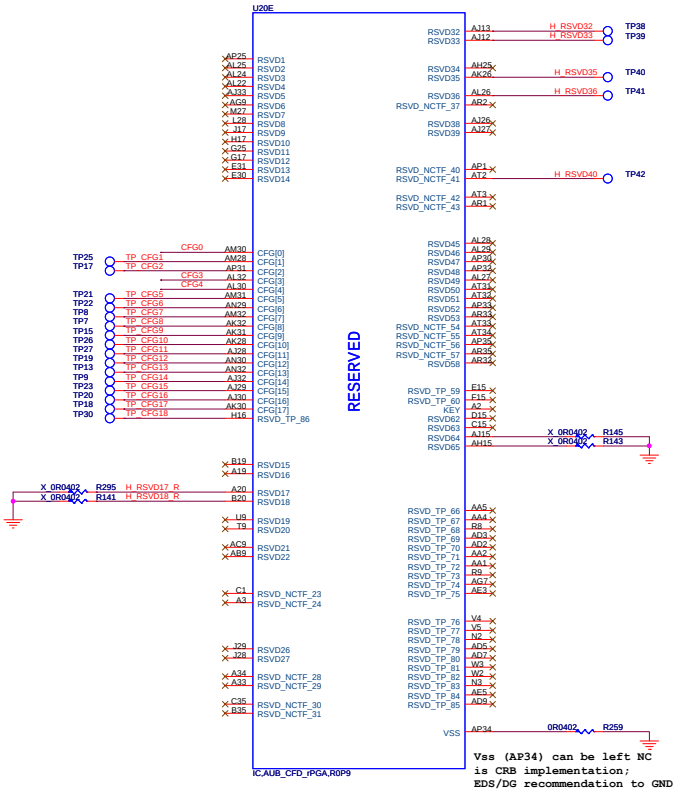
ARRANDALE PROCESSOR (RESERVED)



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG0
NO_STUFF
R97
X_3.01KR1%0402

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG3
NO_STUFF
R98
X_3.01KR1%0402

CFG[3] – PCI Express* Static Lane Numbering Reversal. Lane Reversal will be applied across all 16 Lanes.
- 1: No lane reversal
- 0: Reversal

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG4
NO_STUFF
R99
X_3.01KR1%0402

Layout Note:
Location of all CFG strap resistors needs to be close to trace to minimize stub

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Title: PROCESSOR RESERVED

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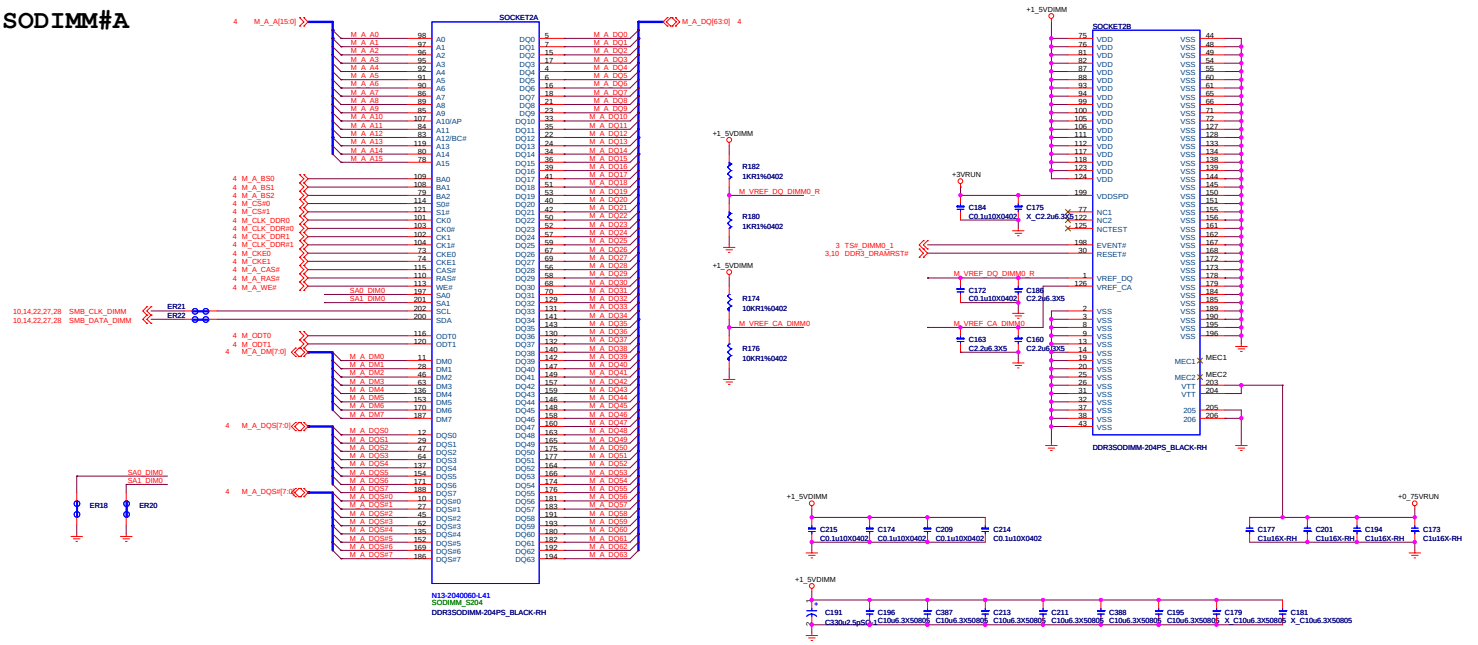
SODIMM#A



Title	DDR3 SODIMM0
Size	Custom
Document Number	MS-1681
Rev	10
Date:	Monday, February 08, 2010
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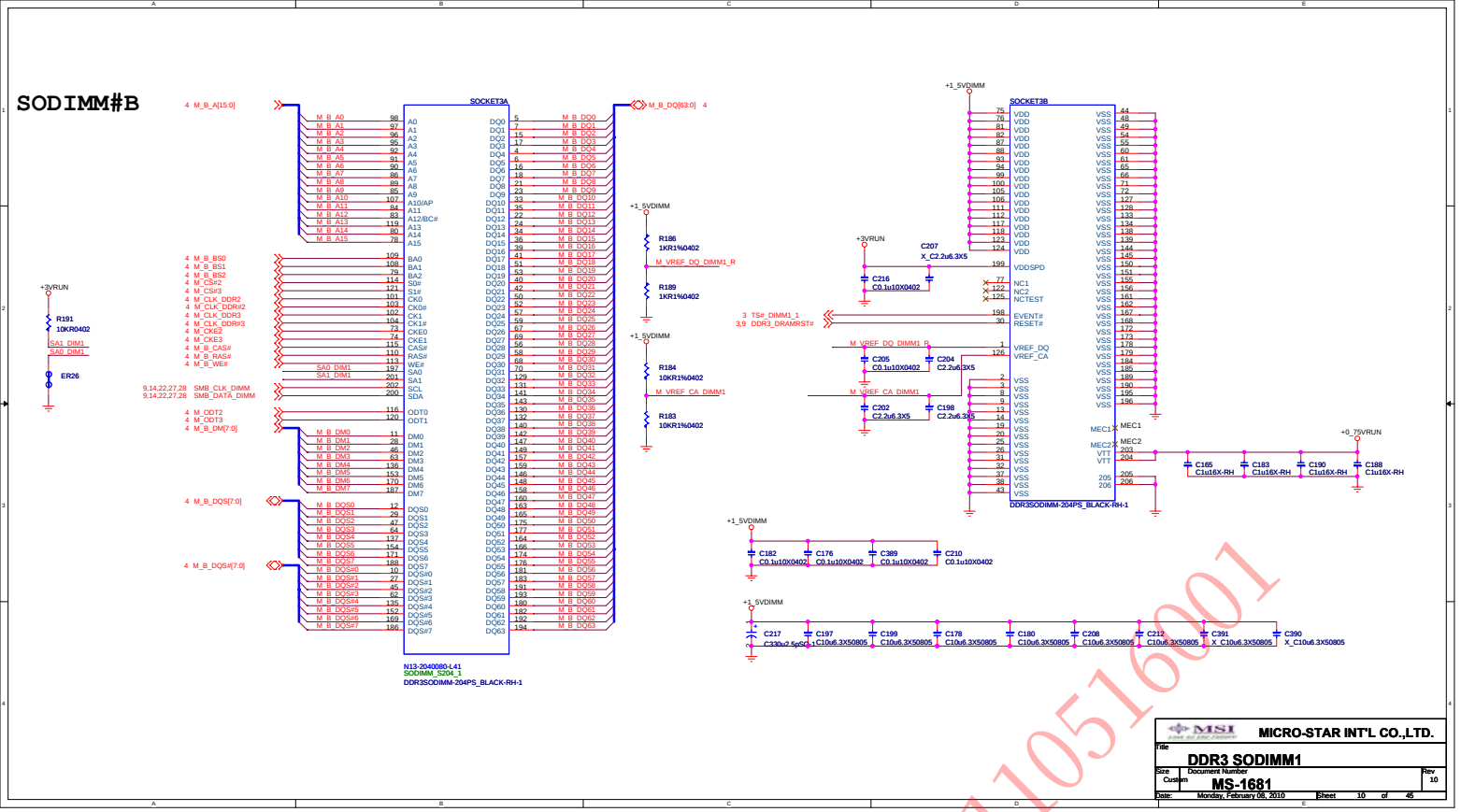

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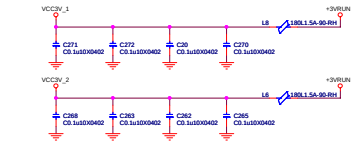
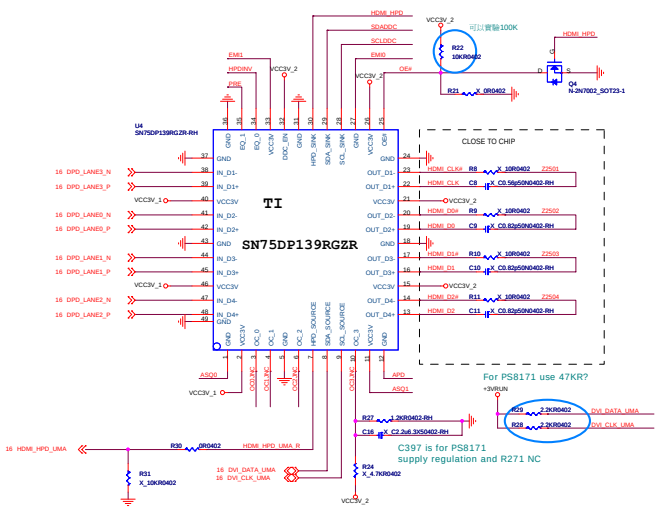
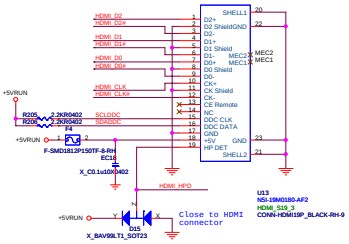
HDMI Switch



	HP_DET	OE#
UNPLUG	0	1 (HIGH Z)
PLUG	1	0 (ACTIVE)

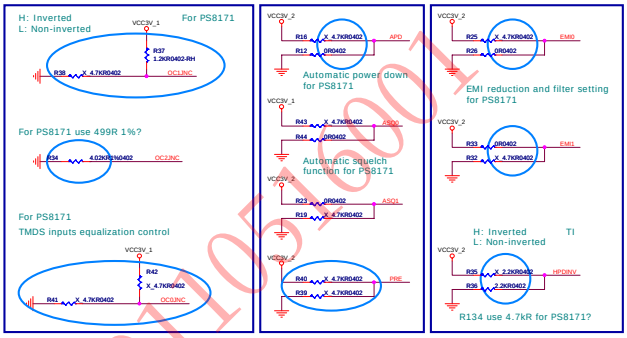


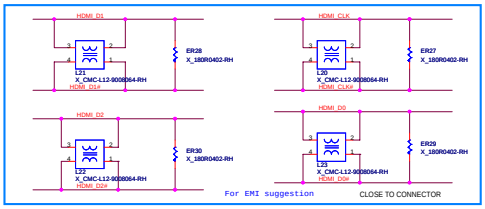
HDMI connector



SN75DP139	PS8171	Pin no.
Floating	TMDS inputs equalization control (internal pull-down~500KΩ) PEQ = LOW: Mid level EQ (Default) PEQ = HIGH: High level EQ PEQ = MID: Low level EQ	Pin 3
High	(Internal pull down~500KΩ) PIO = LOW: HPD = HPD_SINK @ 3.3V CMOS output PIO = High: HPD= HPD_SINK# (inverted HPD) @ 0.9V	Pin 4
GND VCC	[ASQ1,ASQ0] = HL: No automatic squelch (Internal pull down~500kΩ) LL: Automatic squelch enable, Level = 120mVpp, default timer LH: Automatic squelch enable, Level = 100mVpp, default timer HH: Automatic squelch enable, Level = 80mVpp, default timer ML: Automatic squelch enable, Level = 120mVpp, extended timer MH: Automatic squelch enable, Level = 100mVpp, extended timer LM: Automatic squelch enable, Level = 80mVpp, extended timer HM: Reserved MM: Reserved	Pin 1 Pin 11
4.65K to GND	499R to GND	Pin 6
GND	Automatic power down management (Internal pull up~500kΩ) APD = LOW: Automatic power down disable APD = HIGH: Automatic power down enable APD = MID: Reserved	Pin 12
1.2K to GND	2.2uF to GND	Pin 10
GND VCC	EMI reduction and filter setting. (EMI1 internal pull up~500KΩ; EMI0 internal pull down~500KΩ) [EMI1,EMI0] = HL: No EMI reduction EMI0 = HIGH: Reduced rise/fall time MID: Reduced rise/fall time, 2nd EMI1 = LOW: EMI filter setting 1 MID: Reserved	Pin 27 Pin 33
Note2	DDC Active Buffer enable and setting (internal pull-down~500KΩ) DDCBUF = LOW: No DDC active buffer, passive DDC level shifting DDCBUF = HIGH: Active DDC buffer enable, setting 1 DDCBUF = MID: Active DDC buffer enable, setting 2	Pin 34
Floating	TMDS output driver pre-emphasis level setting (internal pull down~500KΩ) PRE = LOW No pre-emphasis PRE = HIGH: Low level pre-emphasis is added PRE = MID: High level pre-emphasis is added	Pin 35

Note2: High is HPD logic inverted, Low is HPD logic non-inverted





LAB2
701-RHDM003-000

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Title: HDMI connector
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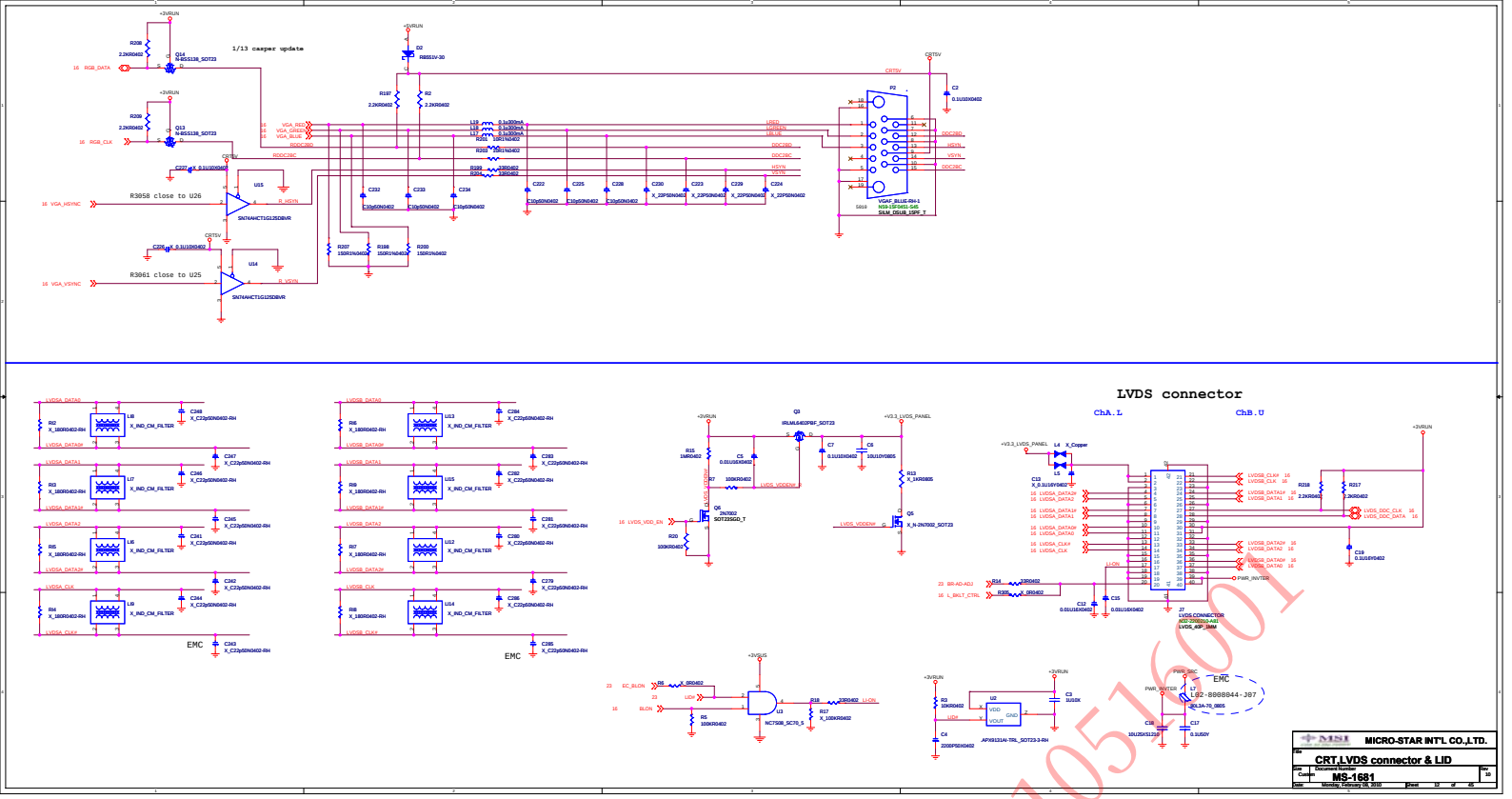

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CRT,LVDS connector & LID

MS-1681

Monday, February 08, 2010

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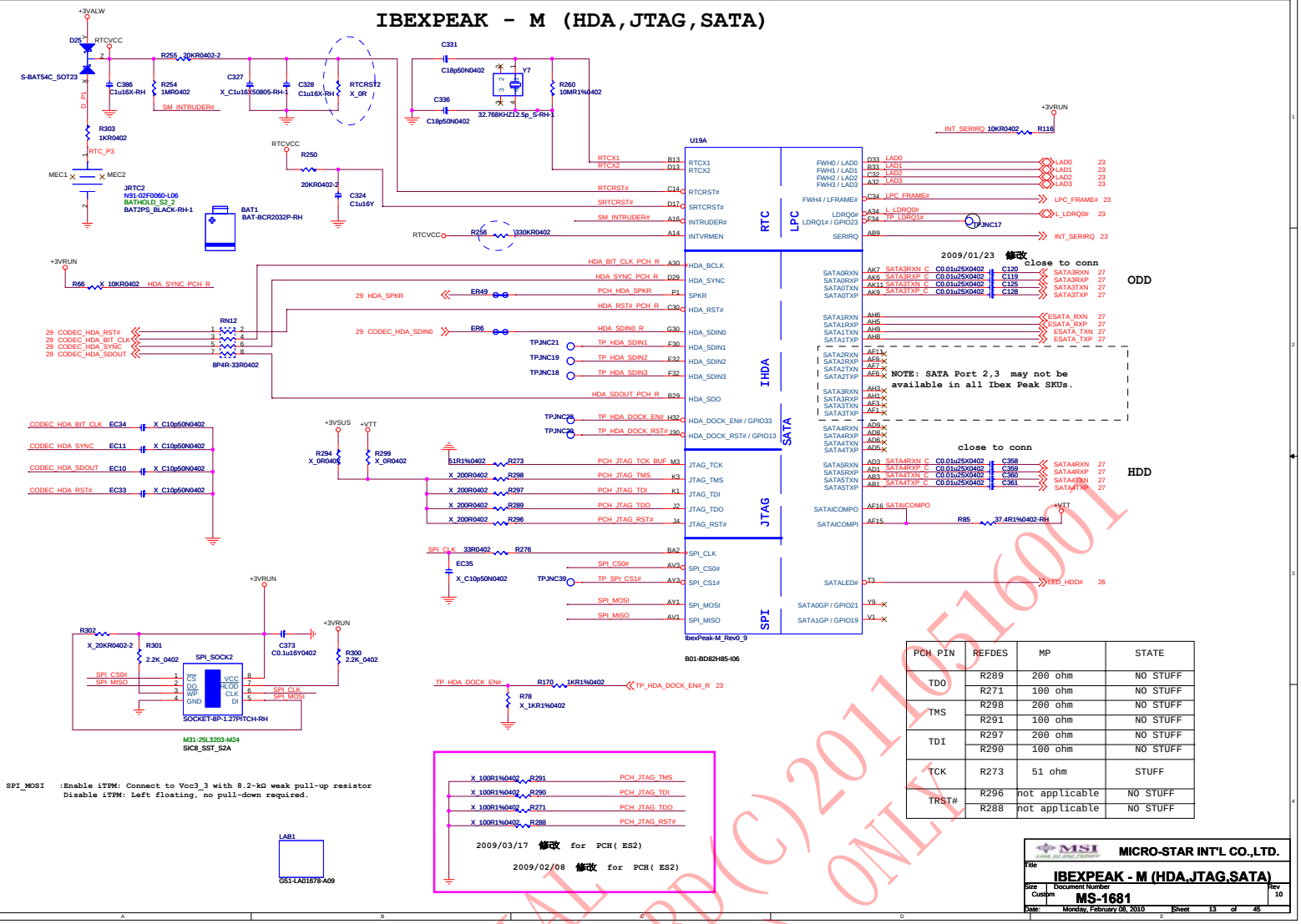
IBEXPEAK - M (HDA,JTAG,SATA)



PCH_PIN	REFDES	MP	STATE
TDO	R289	200 ohm	NO STUFF
	R271	100 ohm	NO STUFF
TMS	R298	200 ohm	NO STUFF
	R291	100 ohm	NO STUFF
TDI	R297	200 ohm	NO STUFF
	R290	100 ohm	NO STUFF
TCK	R273	51 ohm	STUFF
TRST#	R296	not applicable	NO STUFF
	R288	not applicable	NO STUFF

SPI_MOSI :Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor
Disable iTPM: Left floating, no pull-down required.

2009/03/17 修改 for PCH(ES2)

2009/02/08 修改 for PCH(ES2)

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IBEXPEAK - M (HDA,JTAG,SATA)

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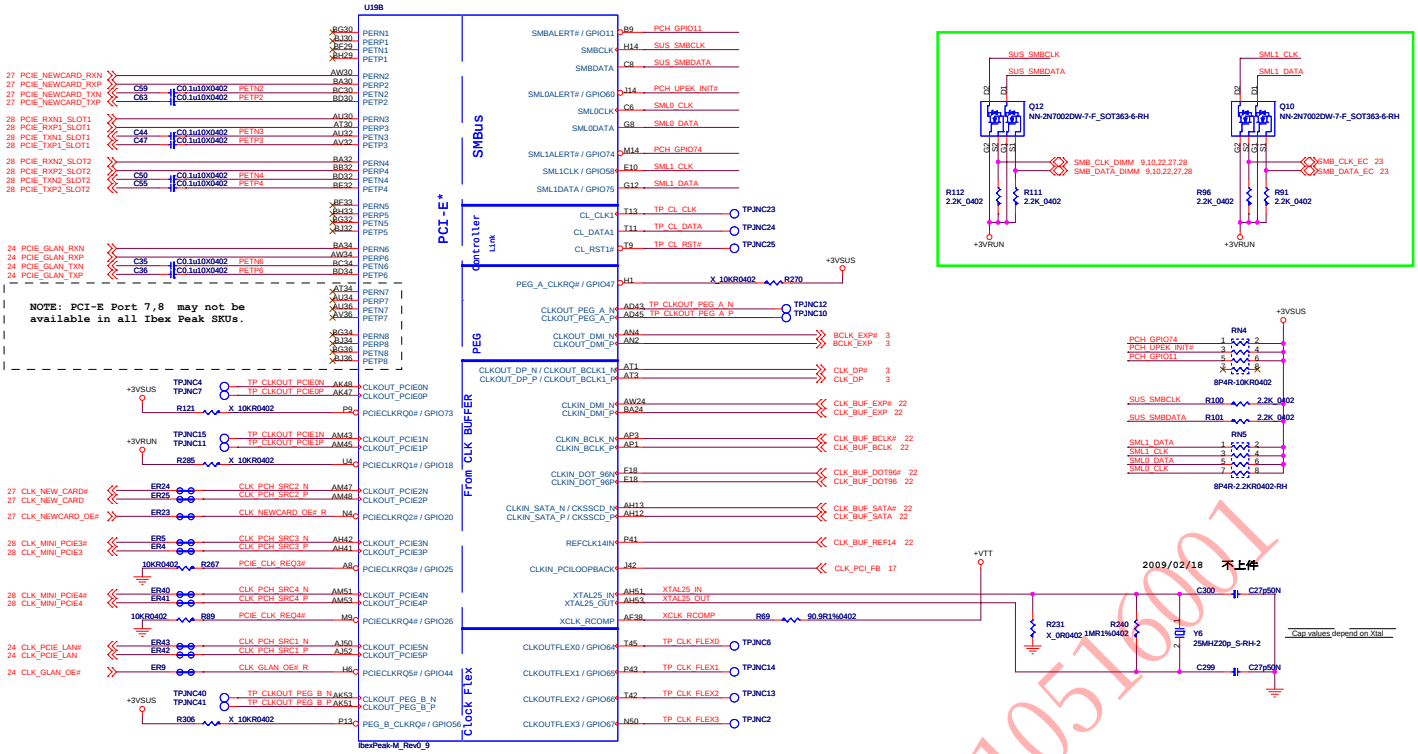
IBEXPEAK - M (PCI-E,SMBUS,CLK)



PCIECLKRQ1# / GPIO18 PCIECLKRQ1# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# PEG_B_CLKRQ#	SUS Well

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Title: IBEXPEAK - M (PCI-E,SMBUS,CLK)

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Date: Monday, February 08, 2010 | Sheet 14 of 45

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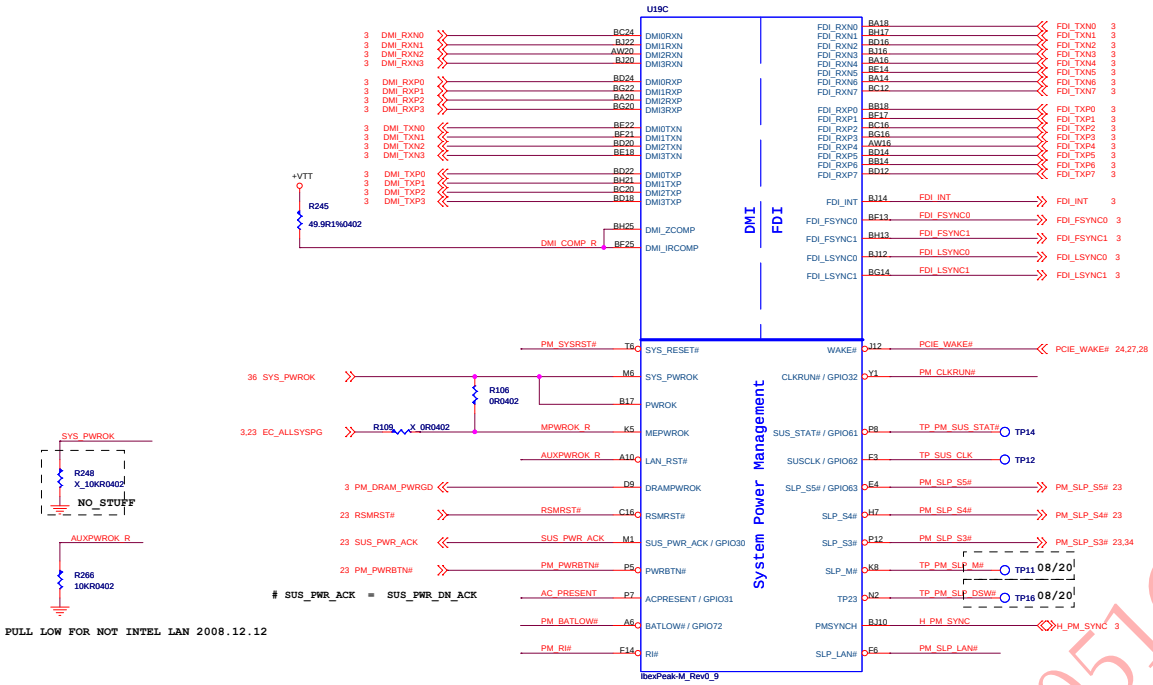
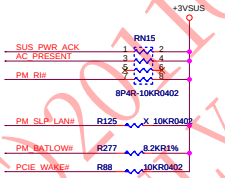
IBEXPEAK - M (DMI,FDI,GPIO)





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Title	IBEXPEAK - M (DMI,FDI,GPIO)		
Size: Custom	Document Number: MS-1681	Rev: 10	
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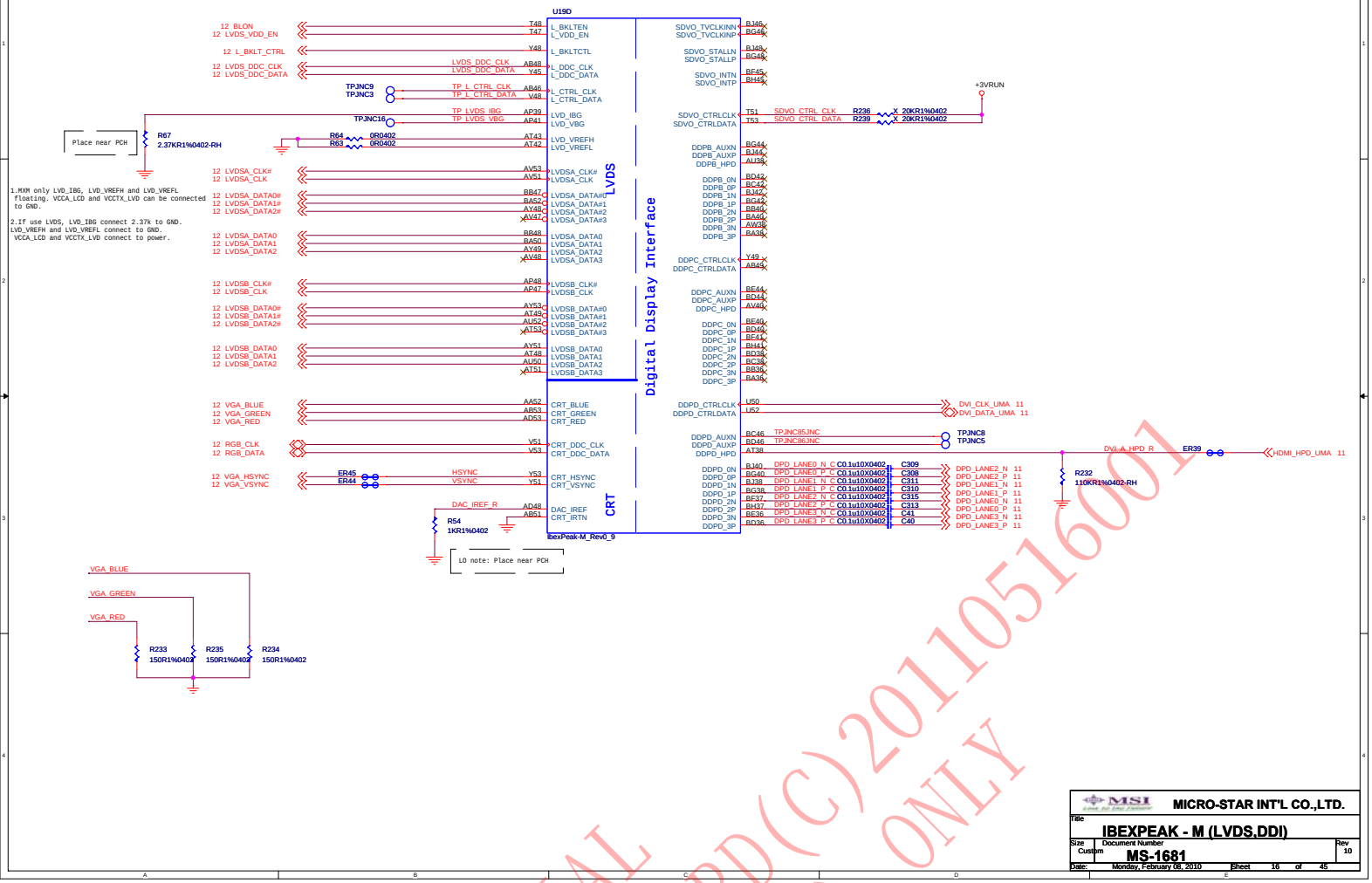
IBEXPEAK - M (LVDS,DDI)



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Title: IBEXPEAK - M (LVDS,DDI)

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IBEXPEAK - M (PCI,USB,NVRAM)

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

PCI_GNT#0
PCI_GNT#1
R58 X_1KR0402
R55 X_1KR0402
PCI_GNT#3
R49 X_1KR0402

U19E

PCI
NVRAM
USB

H40 AD0
N34 AD1
C44 AD2
A38 AD3
C36 AD4
J34 AD5
A40 AD6
D45 AD7
E36 AD8
H48 AD9
E40 AD10
C40 AD11
M48 AD12
M45 AD13
F53 AD14
M40 AD15
M43 AD16
J36 AD17
A48 AD18
E40 AD19
E42 AD20
K46 AD21
M51 AD22
J52 AD23
K51 AD24
L34 AD25
F47 AD26
J40 AD27
G46 AD28
F44 AD29
M47 AD30
H36 AD31

J50 C/BE0#
G42 C/BE1#
H47 C/BE2#
G34 C/BE3#

INT_PIRQA# G38 PIRQA#
INT_PIRQB# H51 PIRQB#
INT_PIRQC# B37 PIRQC#
INT_PIRQD# A44 PIRQD#

PCI_REQ#0 F51 REQ0#
PCI_REQ#1 A46 REQ1# / GPIO50
PCI_REQ#2 B45 REQ2# / GPIO52
PCI_REQ#3 M53 REQ3# / GPIO54

PCI_GNT#0 F48 GNT0#
PCI_GNT#1 K45 GNT1# / GPIO51
PCI_GNT#2 F36 GNT2# / GPIO53
PCI_GNT#3 H53 GNT3# / GPIO55

INT_PIRQE# B41 PIRQE# / GPIO2
INT_PIRQF# K53 PIRQF# / GPIO3
INT_PIRQG# A36 PIRQG# / GPIO4
INT_PIRQH# A48 PIRQH# / GPIO5

K6 PCIRST#

PCI_SERR# E44 SERR#
PCI_PERR# E50 PERR#

PCI_IRDY# A42 IRDY#
H44 PAR
PCI_DEVSEL# F46 DEVSEL#
PCI_FRAME# C46 FRAME#

PCI_LOCK# D49 PLOCK#

PCI_STOP# D41 STOP#
PCI_TRDY# C48 TRDY#

TP10 TP_PCI_PME# M7 PME#

PLT_RST# D5 PLTRST#

N52 CLKOUT_PCI0
P53 CLKOUT_PCI1
P46 CLKOUT_PCI2
P51 CLKOUT_PCI3
P48 CLKOUT_PCI4

IbexPeak-M_Rev0_9

NV_CE#0 AY9
NV_CE#1 BD1
NV_CE#2 AP15
NV_CE#3 BD8
NV_DQS0 AV9
NV_DQS1 BC8
NV_DQ0 / NV_IO0 AP7
NV_DQ1 / NV_IO1 AP6
NV_DQ2 / NV_IO2 AT6
NV_DQ3 / NV_IO3 AT9
NV_DQ4 / NV_IO4 BB1
NV_DQ5 / NV_IO5 AV6
NV_DQ6 / NV_IO6 BB3
NV_DQ7 / NV_IO7 BA4
NV_DQ8 / NV_IO8 BE4
NV_DQ9 / NV_IO9 BB6
NV_DQ10 / NV_IO10 BD6
NV_DQ11 / NV_IO11 BB7
NV_DQ12 / NV_IO12 BC9
NV_DQ13 / NV_IO13 BJ8
NV_DQ14 / NV_IO14 BJ6
NV_DQ15 / NV_IO15 BG6
NV_ALE BD3
NV_CLE AY6
NV_RCOMP AU2
NV_RB# AV7
NV_WR#0_RE# AY8
NV_WR#1_RE# AY5
NV_WE#_CK0 AV11
NV_WE#_CK1 BF5

NV_RCOMP
R275 X_32.4R1%0402-RH

USBP0N H18 USB_PN0
USBP0P J18 USB_PP0
USBP1N A18 USB_PN1
USBP1P C18 USB_PP1
USBP2N N20 USB_PN2
USBP2P P20 USB_PP2
USBP3N J20 USB_PN3
USBP3P L20 USB_PP3
USBP4N F20 USB_PN4
USBP4P G20 USB_PP4
USBP5N A20 USB_PN5
USBP5P C20 USB_PP5
USBP6N M22
USBP6P N22
USBP7N B21
USBP7P D21
USBP8N H22 USB_PN8
USBP8P J22 USB_PP8
USBP9N E22 USB_PN9
USBP9P F22 USB_PP9
USBP10N A22 USB_PN10
USBP10P C22 USB_PP10
USBP11N G24 USB_PN11
USBP11P H24 USB_PP11
USBP12N L24 USB_PN12
USBP12P M24 USB_PP12
USBP13N A24
USBP13P C24

USB_PN0 27
USB_PP0 27
USB_PN1 28
USB_PP1 28
USB_PN2 28
USB_PP2 28
USB_PN3 28
USB_PP3 28
USB_PN4 27
USB_PP4 27
USB_PN5 27
USB_PP5 27

NOTE: USB Port 6,7 may not be available in all Ibex Peak SKUs.

USB_PN8 25
USB_PP8 25
USB_PN9 27
USB_PP9 27
USB_PN10 28
USB_PP10 28
USB_PN11 28
USB_PP11 28
USB_PN12 28
USB_PP12 28

2009/01/23 修改

USBRBIAS# B25 USB_BIAS
USBRBIAS D25
R244 22.6R1%0402
+3VSUS

OC0# / GPIO59 N16
OC1# / GPIO40 J16
OC2# / GPIO41 F16
OC3# / GPIO42 L16
OC4# / GPIO43 E14
OC5# / GPIO9 G16
OC6# / GPIO10 F12
OC7# / GPIO14 T15

USB_OC# R84 10KR0402

14 CLK_PCI_FB
23 CLK_PCI_KBC
23 CLK_PCIF_PORTB0
CLK_PCI_FB
CLK_PCI_KBC
CLK_PCIF_PORTB0
R238 22R0402 CLKOUT_PCI1
R60 22R0402 CLKOUT_PCI2
R237 22R0402 CLKOUT_PCI3
EC32 X_C10p50N0402
EC8 X_C10p50N0402
EC31 X_C10p50N0402
EMI

+3VRUN

RN9
PCI_REQ#1
PCI_FRAME#
PCI_TRDY#
INT_PIRQH#
RN8
PCI_REQ#0
INT_PIRQB#
INT_PIRQF#
PCI_REQ#3
RN11
INT_PIRQG#
INT_PIRQC#
INT_PIRQE#
PCI_STOP#
RN3
PCI_LOCK#
PCI_PERR#
PCI_DEVSEL#
INT_PIRQA#
RN10
PCI_IRDY#
PCI_SERR#
INT_PIRQD#
PCI_REQ#2
8P4R-8.2KR0402-1

PCI_GNT#2 R68 10KR0402

PLT_RST#
R130 33R0402 LAN_RST# 24
R131 33R0402 LPC_RST# 23

+3VSUS
C107 C0.1u10X0402
U9
SG8P5X_SC70
RN6
8P4R-33R0402
NEWCARD_RST# 27
WLAN_RST# 28
TV_RST# 28
ER8
BUF_PTL_RST# 3

MICRO-STAR INT'L CO.,LTD.

Title	IBEXPEAK - M (PCI,USB,NVRAM)	
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Date: Monday, February 08, 2010	Sheet 17 of 45	

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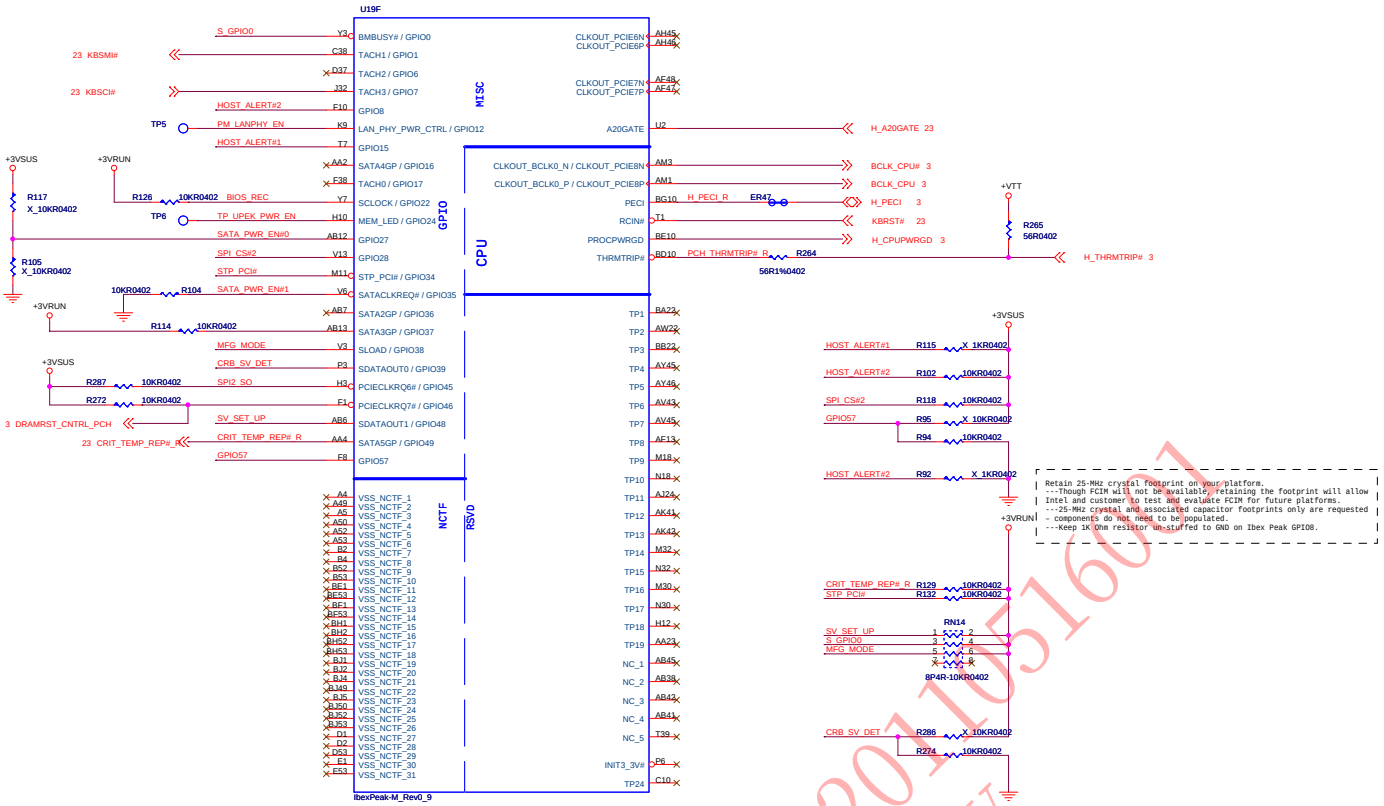
60013789 周小強 RD(C)20110516001
FOR RMA維修(劉松林) ONLY

IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)



MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK-M(GPIO,VSS_NCTF,RSVD)

Size: Custom | Document Number: MS-1681 | Rev: 10

Date: Monday, February 08, 2010 | Sheet 18 of 45

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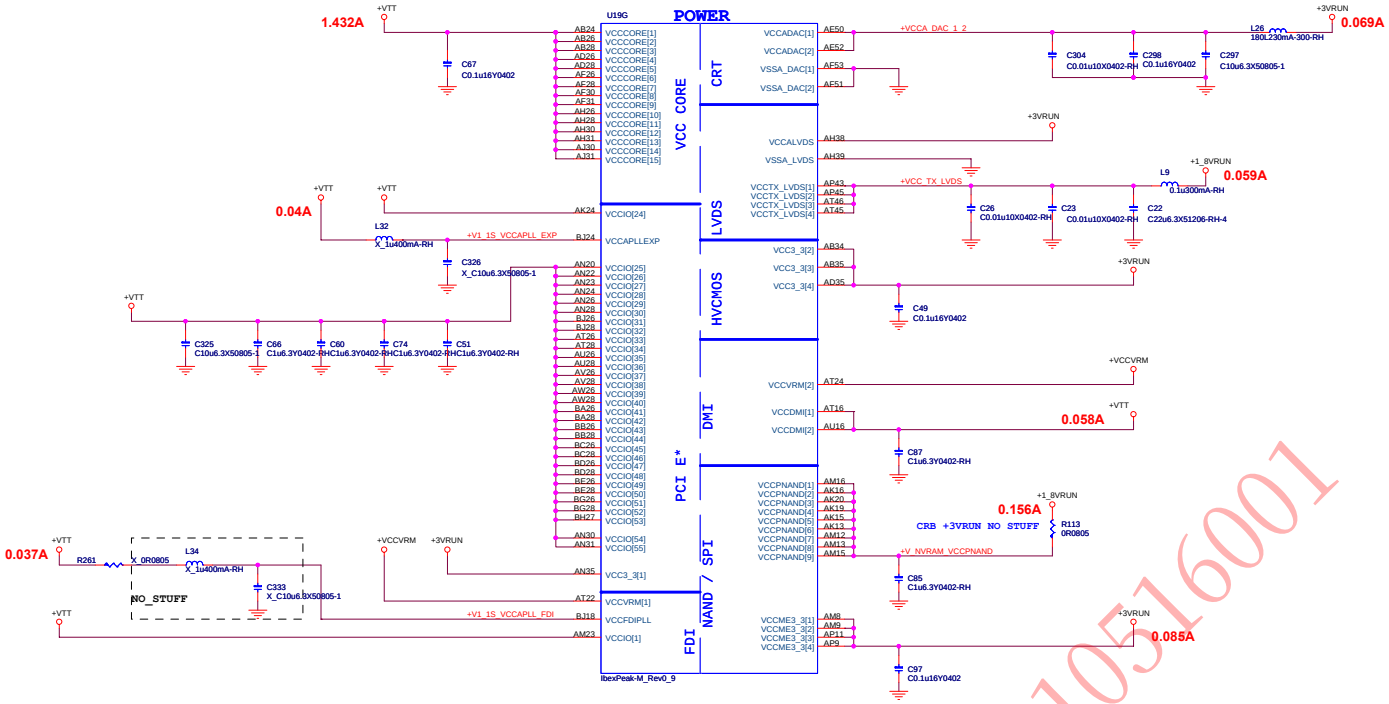
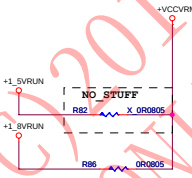
IBEXPEAK - M (POWER)



The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCACl k, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.



MICRO-STAR INT'L CO.,LTD.

Title	IBEXPEAK - M (POWER)	
Size: Custom	Document Number: MS-1681	Rev: 10
Date: Monday, February 08, 2010	Sheet 19 of 45	

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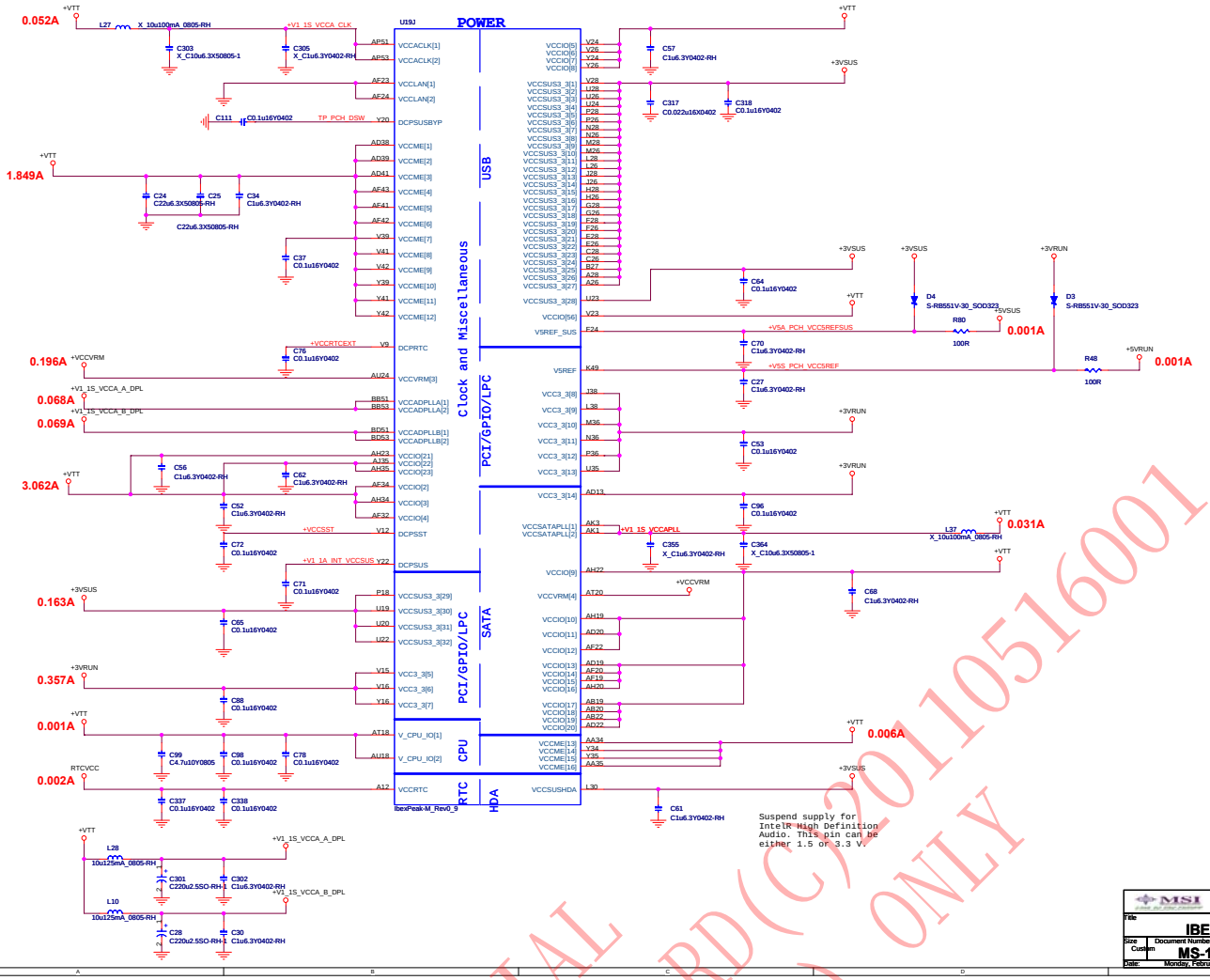
VccLAN may be grounded if Intel LAN is disabled.

IBEXPEAK - M (POWER)



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MSI	MICRO-STAR INT'L CO.,LTD.
Title	IBEXPEAK - M (POWER)
Size / Document Number	Custom / MS-1681
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Date:	Monday, February 08, 2010
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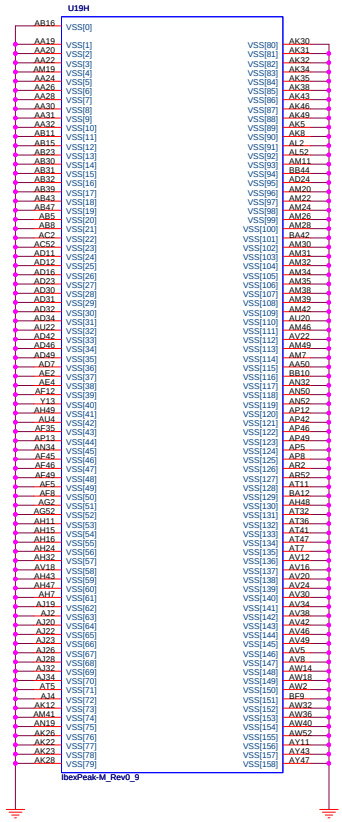
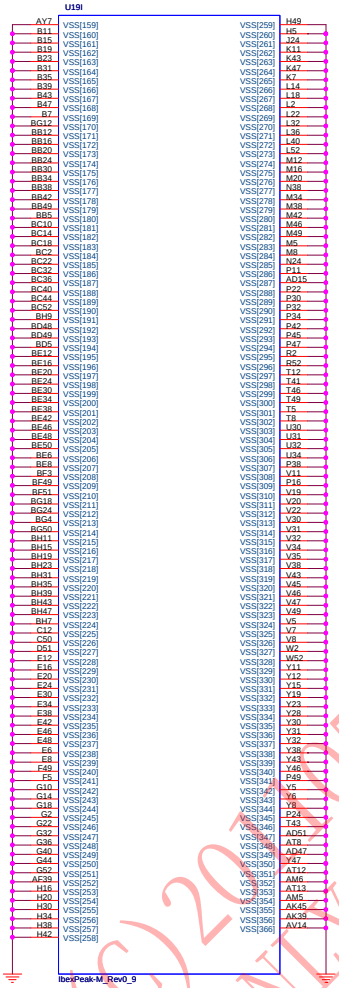
IBEXPEAK - M (GND)





MSI	MICRO-STAR INT'L CO.,LTD.
Title	IBEXPEAK - M (GND)
Size: Custom	Document Number: MS-1681
Rev	1.0
Date: Monday, February 08, 2010	Sheet 21 of 45

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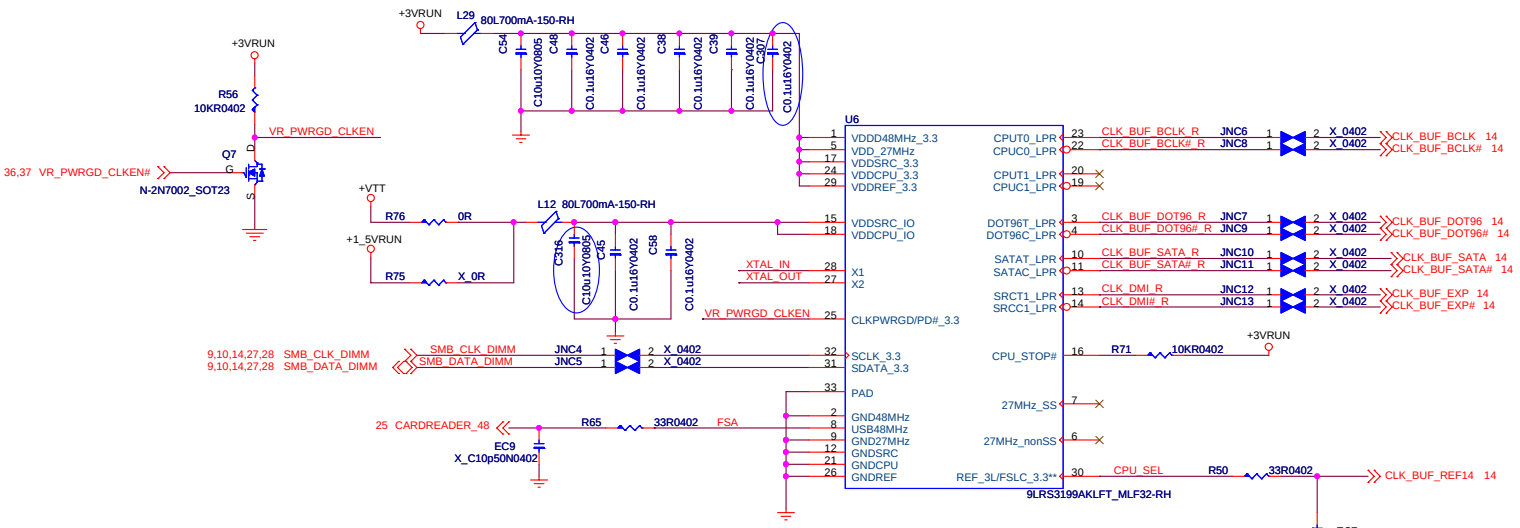
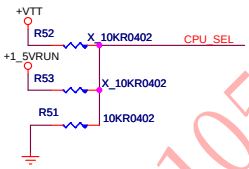


For CPU frequency select (133MHz)

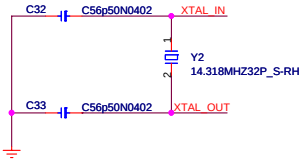


CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

Capacity select

If LC=20pf C708/C709=33pf

If LC=32pf C708/C709=56pf



Co-Lay Note:

For IDT IC9IRS3199

R598,R599,R600=10Kohm

For Silego SLG8SP587

R598,R599,R600=4.7Kohm

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MICRO-STAR INT'L CO.,LTD.

Title: Clock Generator (ICS9IRS3199)

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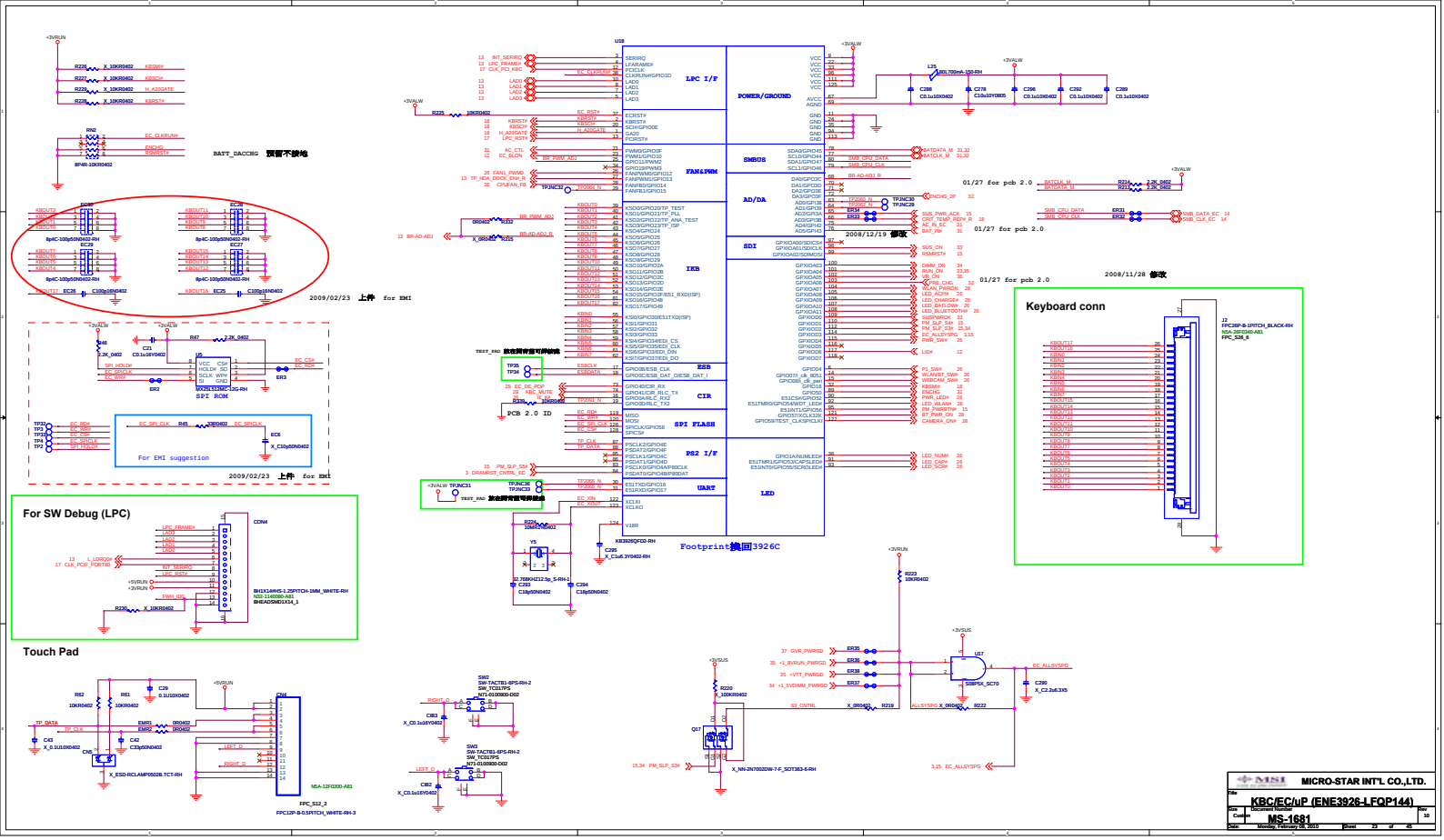

U18
LPC I/F
POWER/GROUND
SMBUS
FAN&PWM
AD/DA
SDI
IKB
ESB
SPI FLASH
PS2 I/F
CIR
UART
LED
Footprint換回3926C
BATT_DACCBG 預留不接地
2009/02/23 上件 for EMI
SPI ROM
For EMI suggestion
2009/02/23 上件 for EMI
PCB 2.0 ID
01/27 for pcb 2.0
2008/12/19 修改
2008/11/28 修改
Keyboard conn
For SW Debug (LPC)
Touch Pad
MICRO-STAR INT'L CO.,LTD.
KBC/EC/uP (ENE3926-LFQP144)
MS-1681

1. Pin 46 : RSET res. should be close to LAN chip. Don't have power trace or high frequency trace beside it.

2. The trace of each Pair(MDIX+/-) should be equal in length and better have ground under.

3. Both EGND and GND can be connect together or use 0 Ohm res. to connect them.

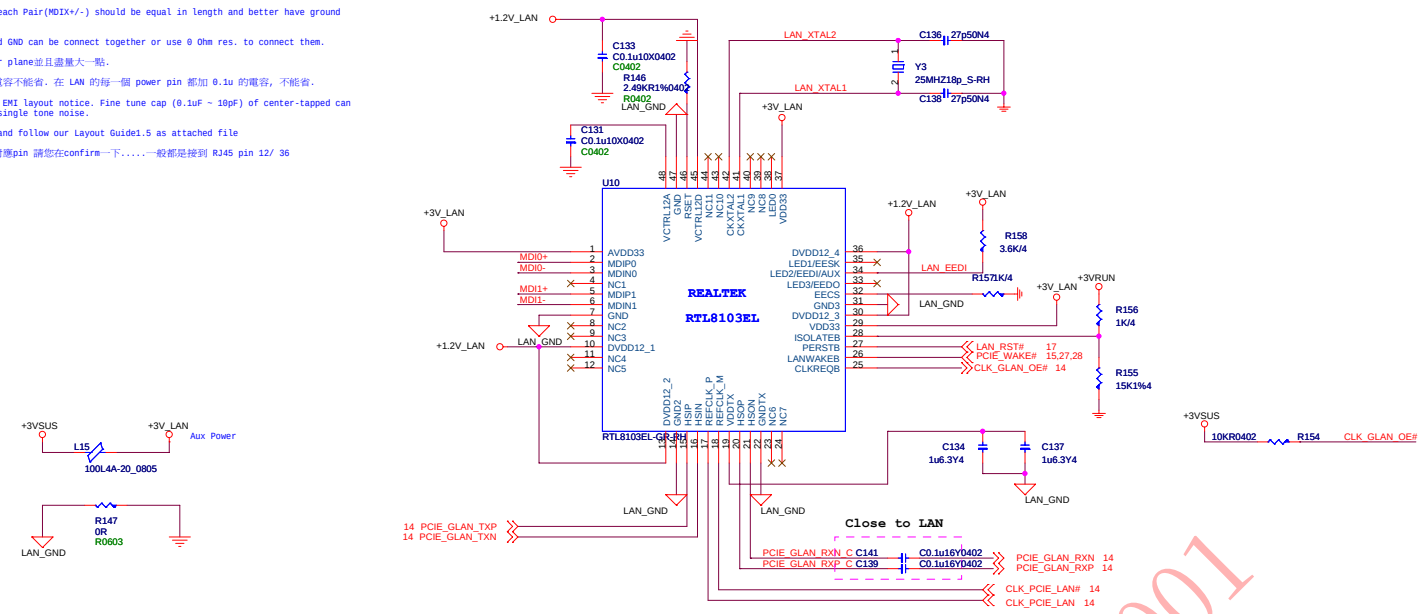
4. 1.2V請留 power plane並且盡量大一點.

5. 1.2V Bypass 電容不能省. 在 LAN 的每一個 power pin 都加 0.1u 的電容, 不能省.

6.請參考RTL8111C EMI layout notice. Fine tune cap (0.1uF ~ 10pF) of center-tapped can improve EMI for single tone noise.

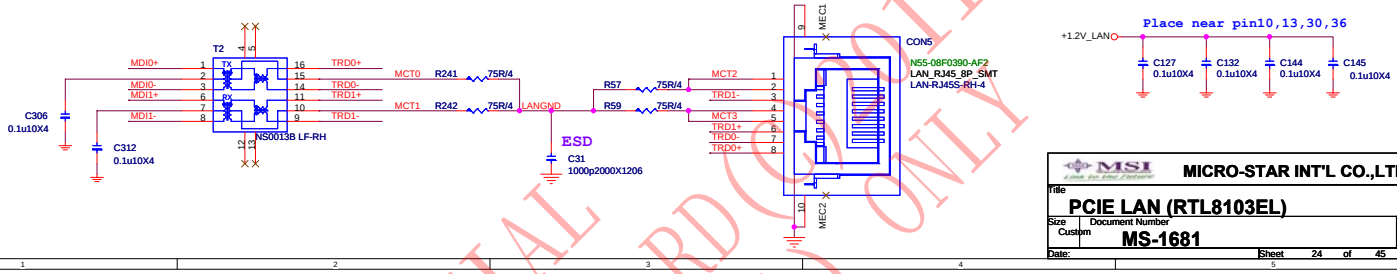
7. Please refer and follow our Layout Guide1.5 as attached file

8. RJ45 的部份,對應pin 請您在confirm一下.....一般都是接到 RJ45 pin 12/ 36



POWER Comparison

	3.3V	mW
10 M Idle/TxRx	87/172	287/568
100 M Idle/TxRx	112/165	370/545
ALDPS	60	198
D3 cold with link10M /without link	32/18	106/59.4



MICRO-STAR INT'L CO.,LTD.

Title: PCIE LAN (RTL8103EL)

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60013789 周小強 RD(02)2911051600 1
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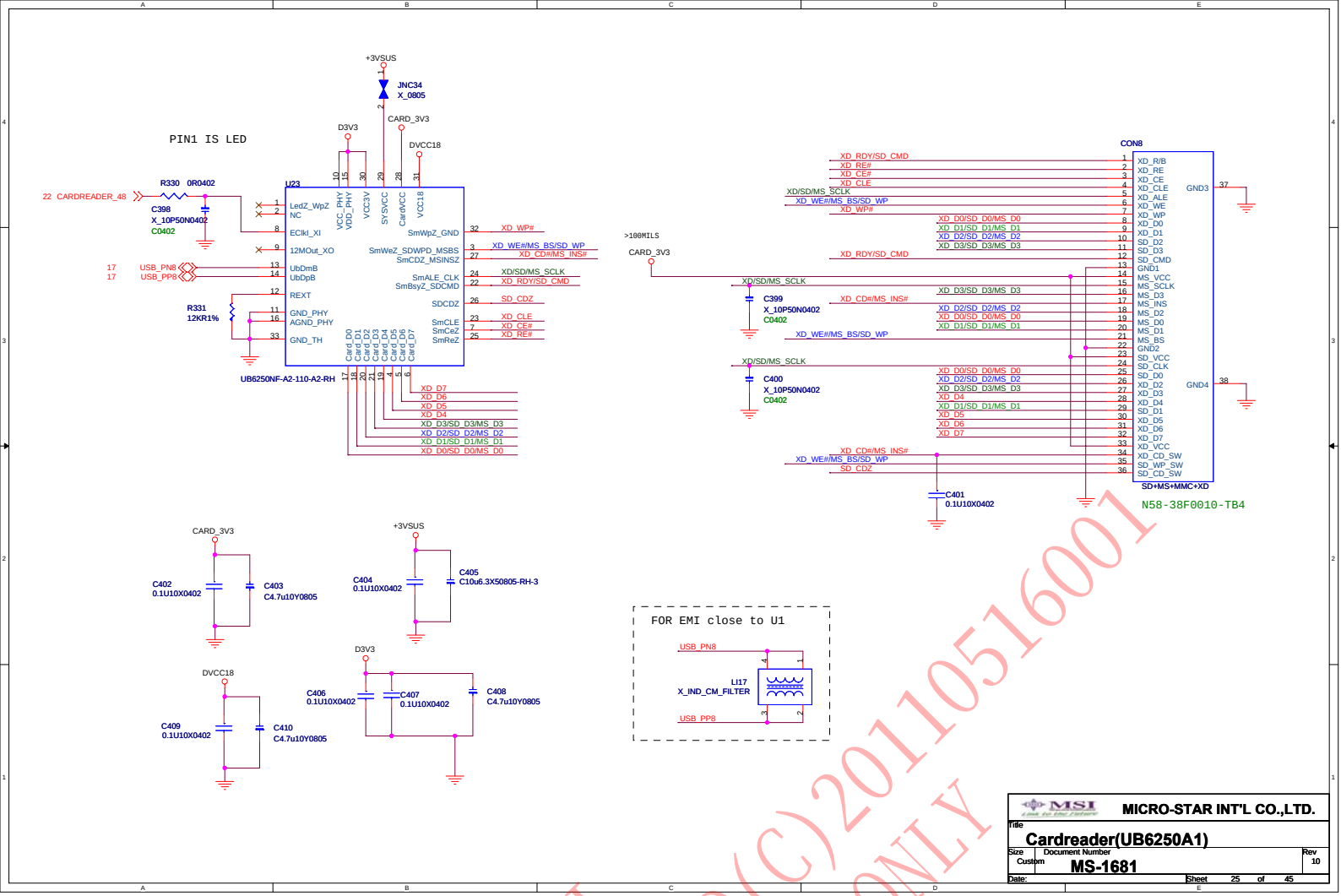

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MSI MICRO-STAR INT'L CO.,LTD.

Title: Cardreader(UB6250A1)

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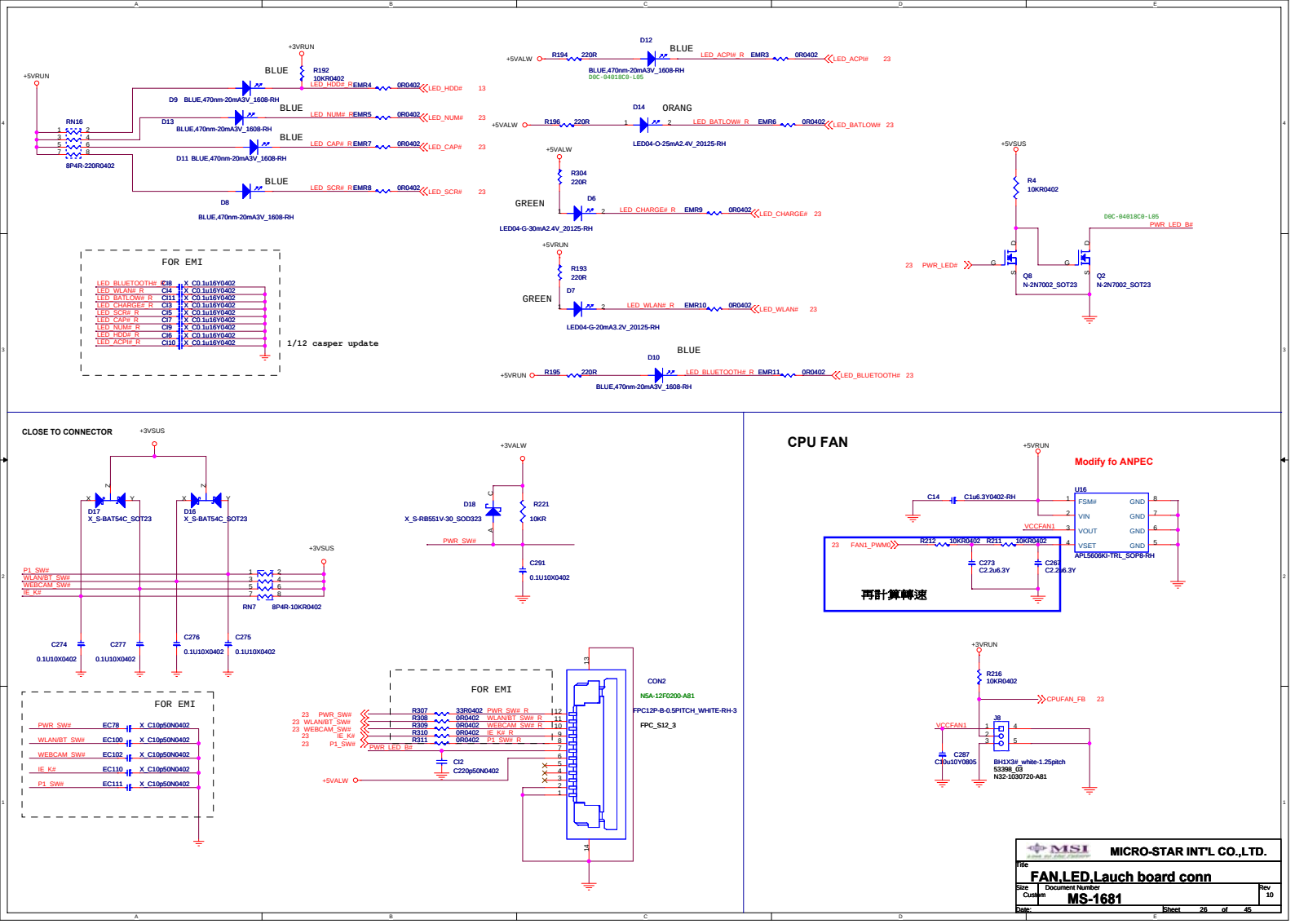

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	FAN,LED,Lauch board conn	
Size: Custom	Document Number: MS-1681	Rev: 10
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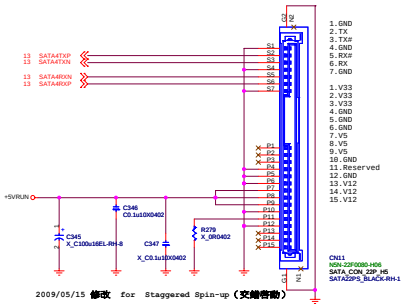
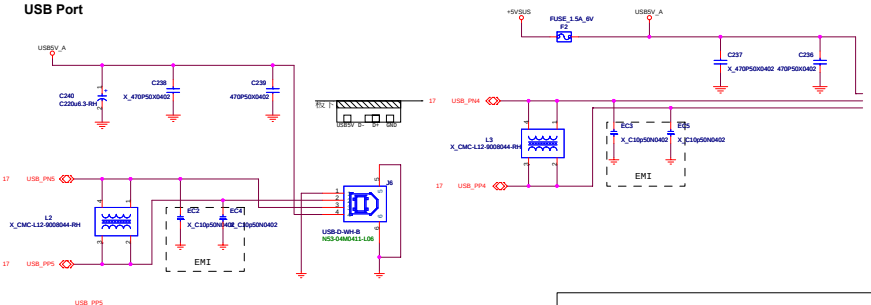
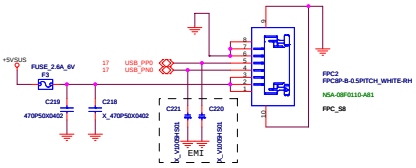
SATA HDD

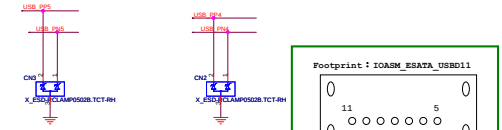


USB Port

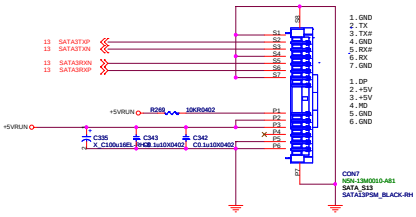


USB Port (to daughter board)

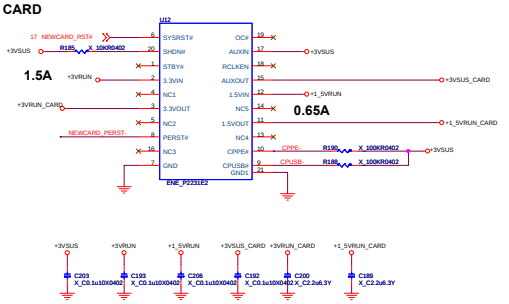


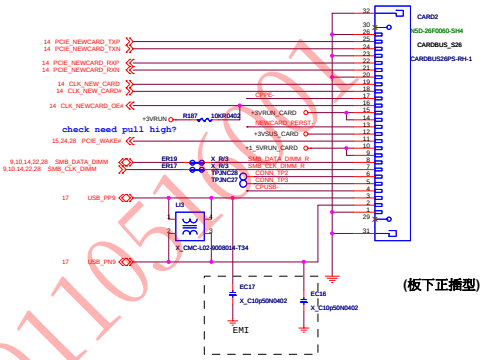


SATA ODD



NEW CARD





MICRO-STAR INT'L CO.,LTD.		
Title: HDD CDROM,USB ,NEW CARD		
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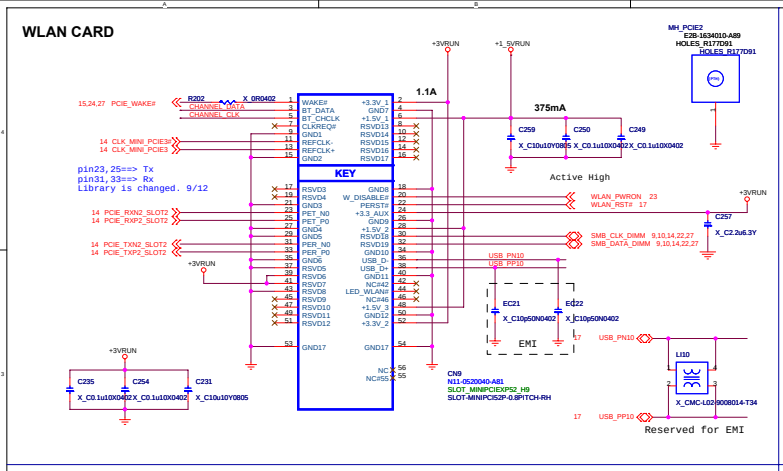

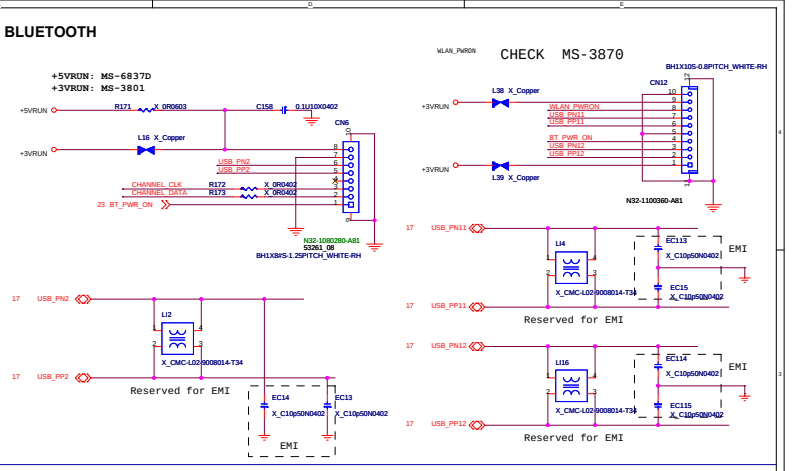

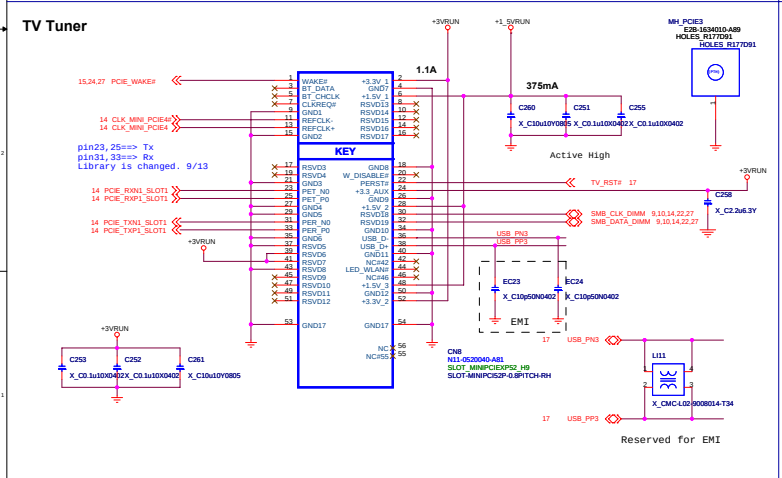

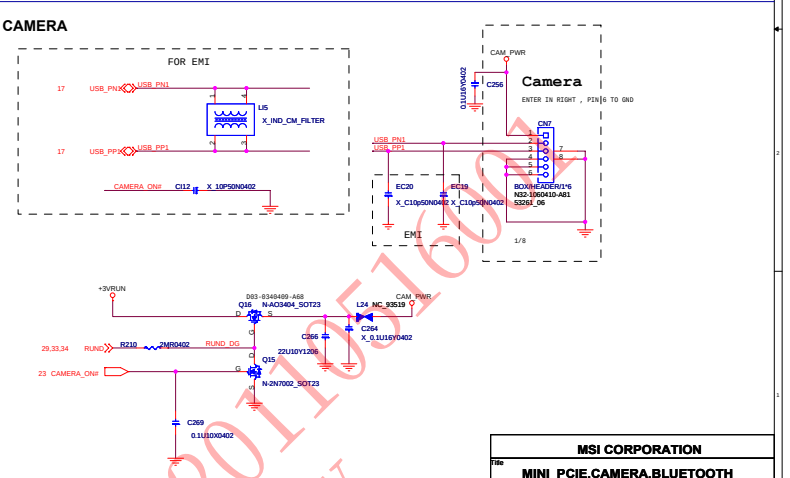

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MSI CORPORATION

Title	MINI_PCIE,CAMERA,BLUETOOTH	
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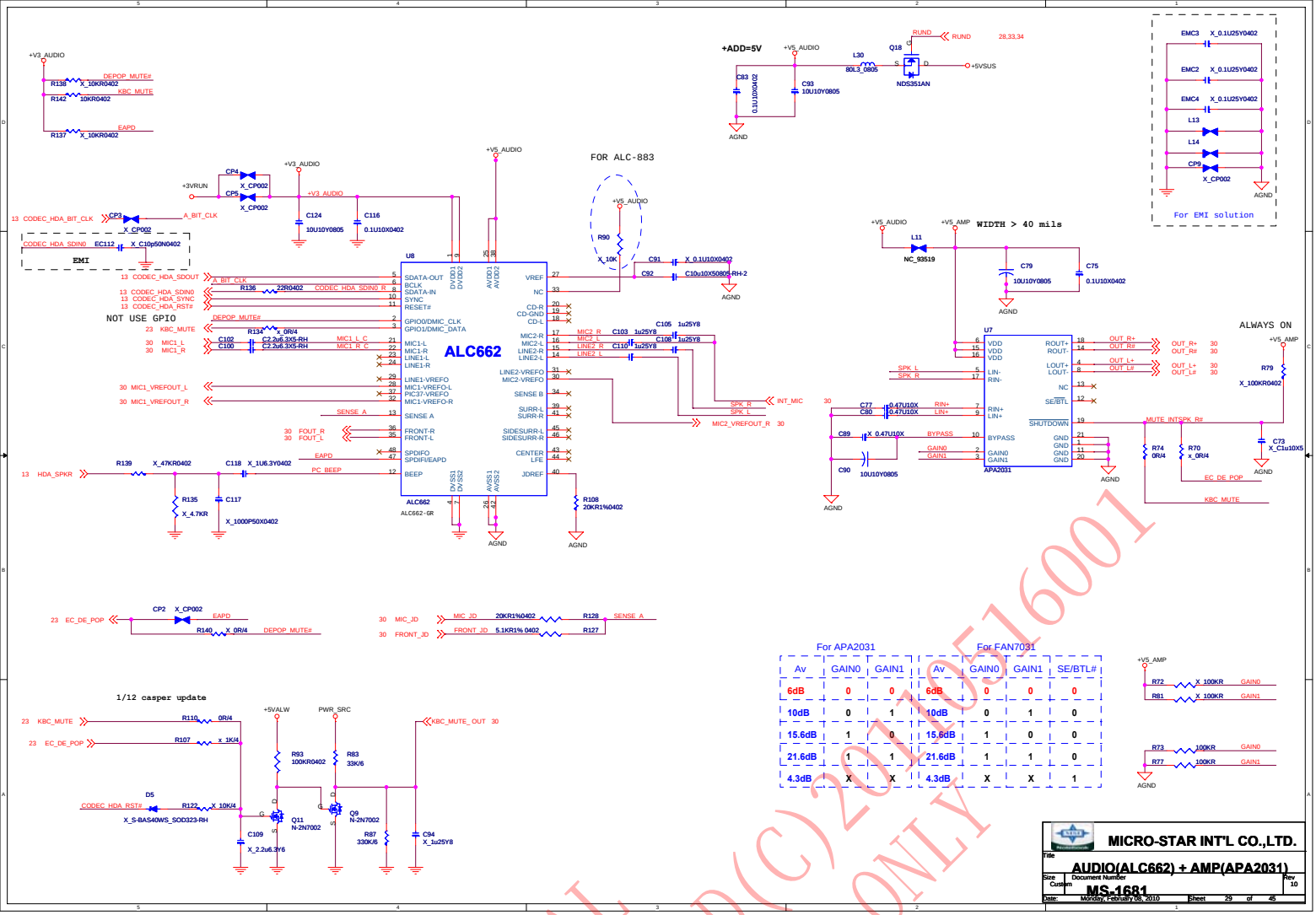

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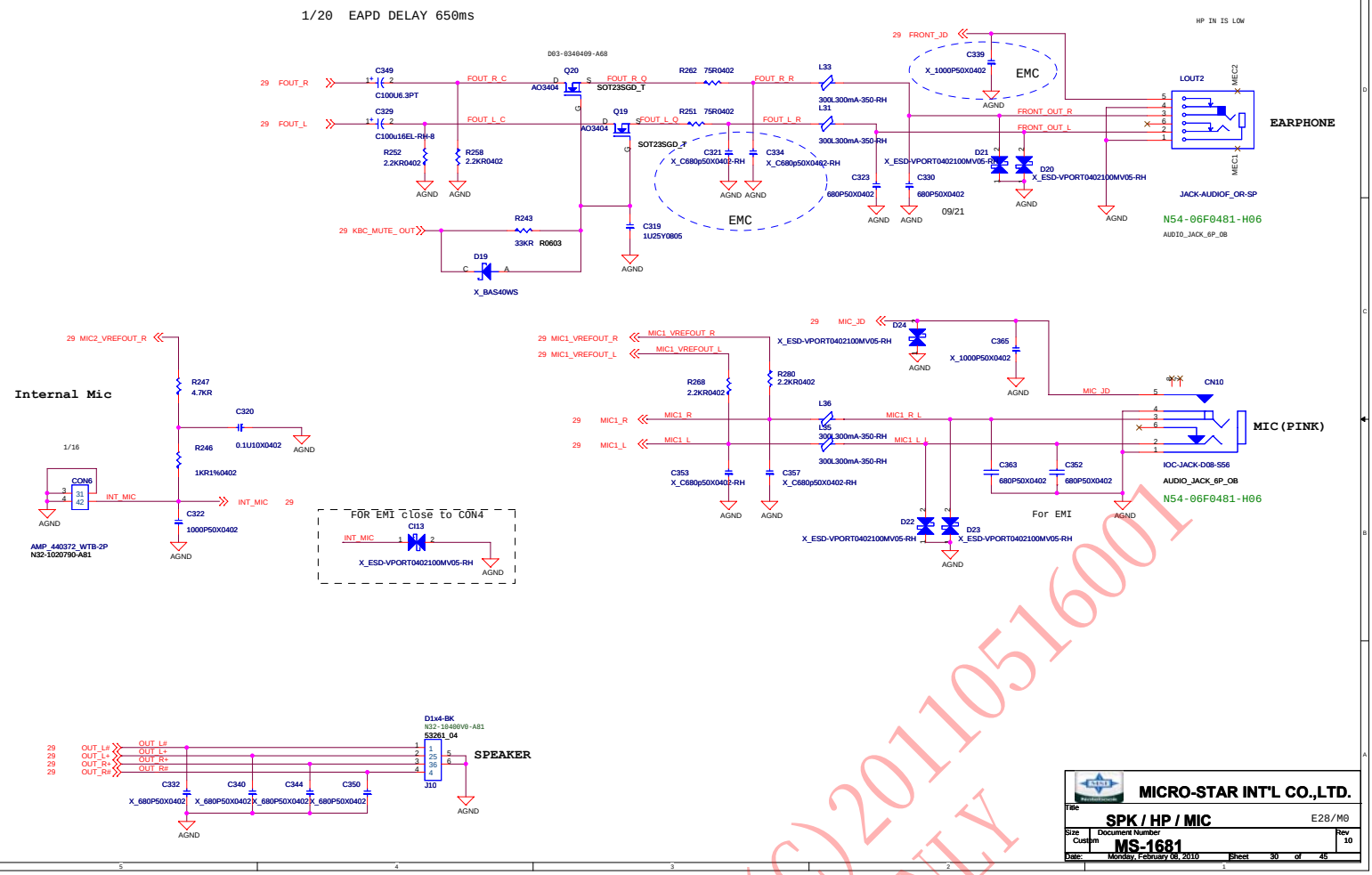
60013789 周小強 RD(C)2010051600 1
FOR RMA維修(劉松林) ONLY



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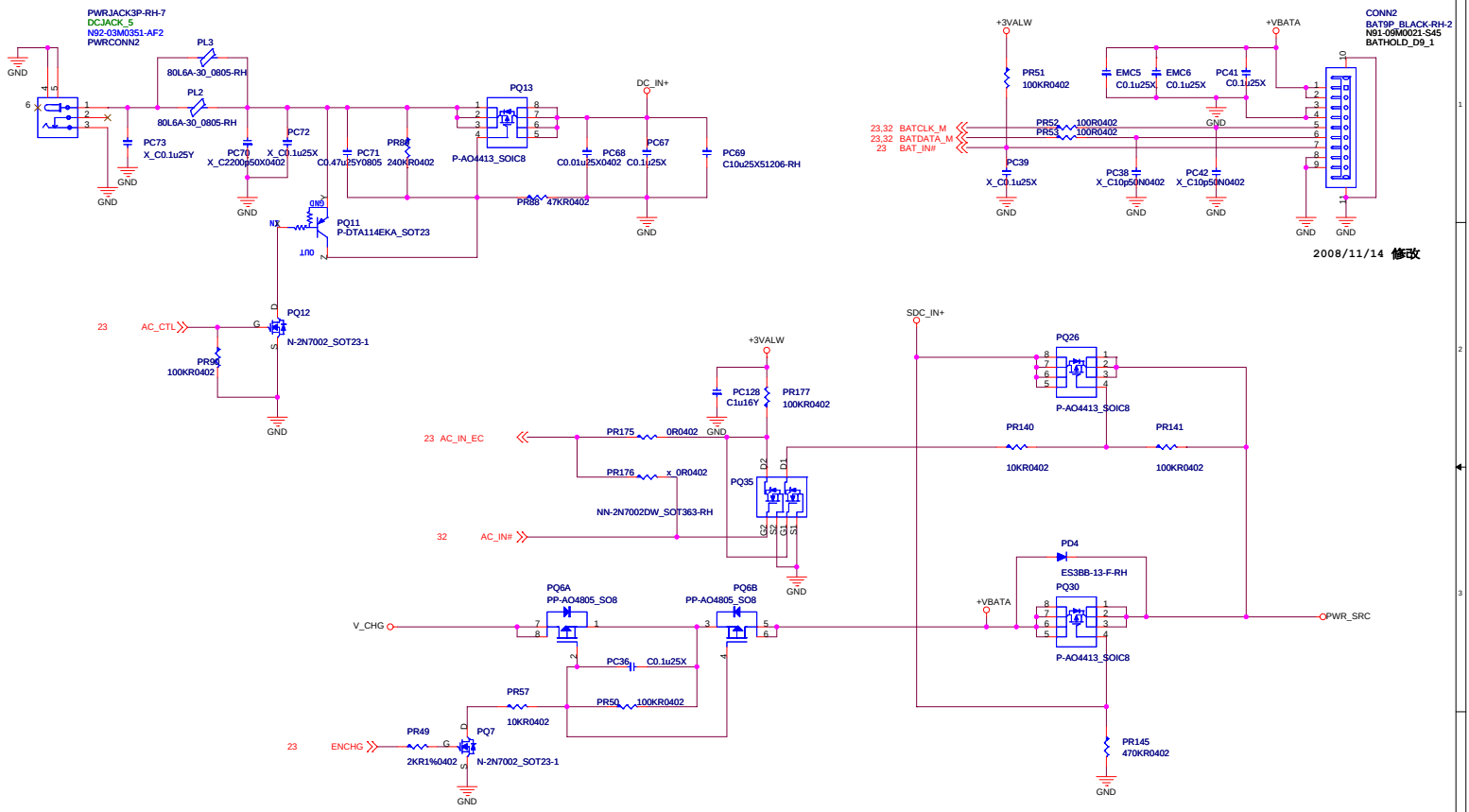

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	Battery Select	
Size: Custom	Document Number: MS-1681	Rev: 10
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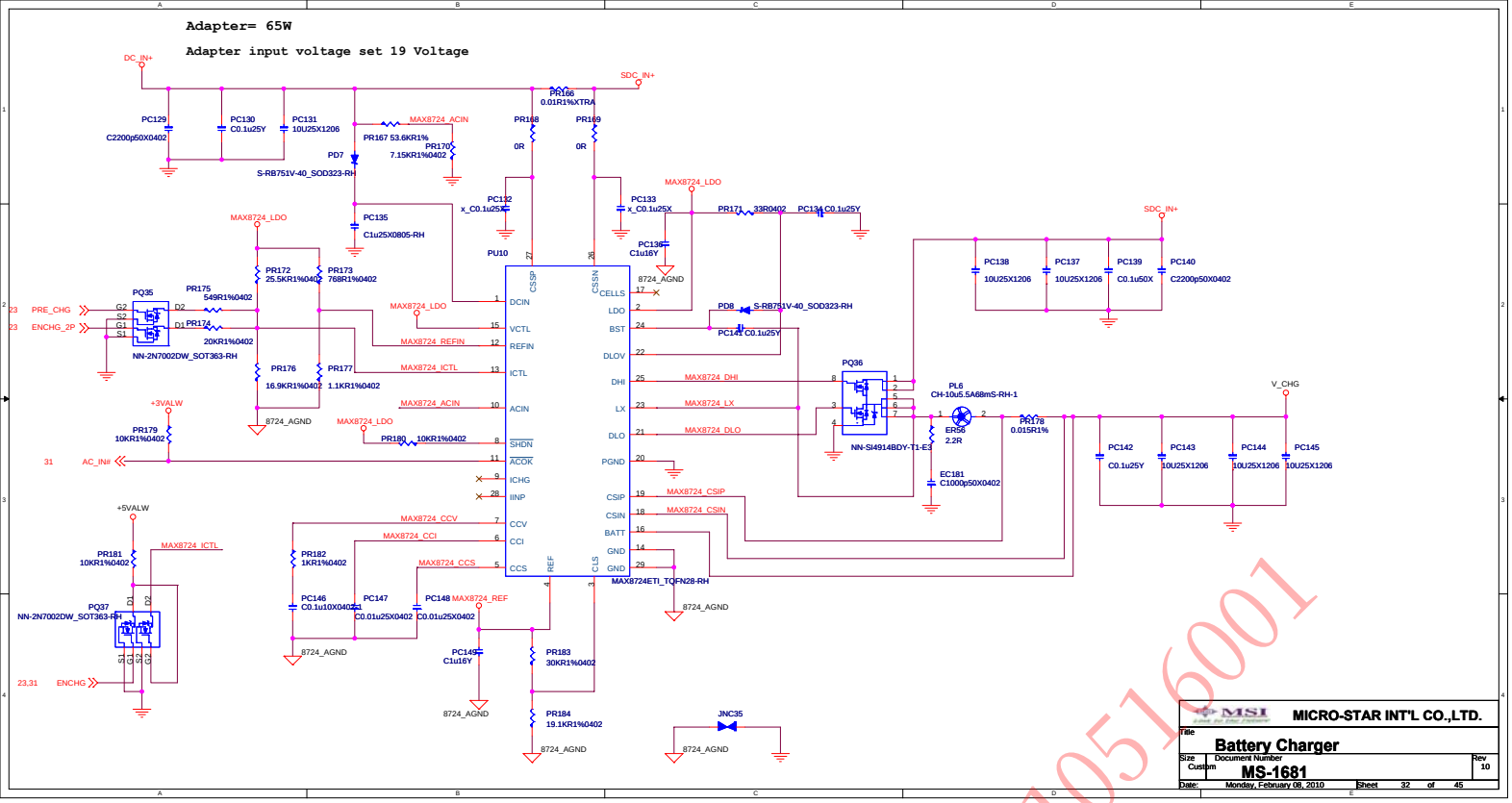

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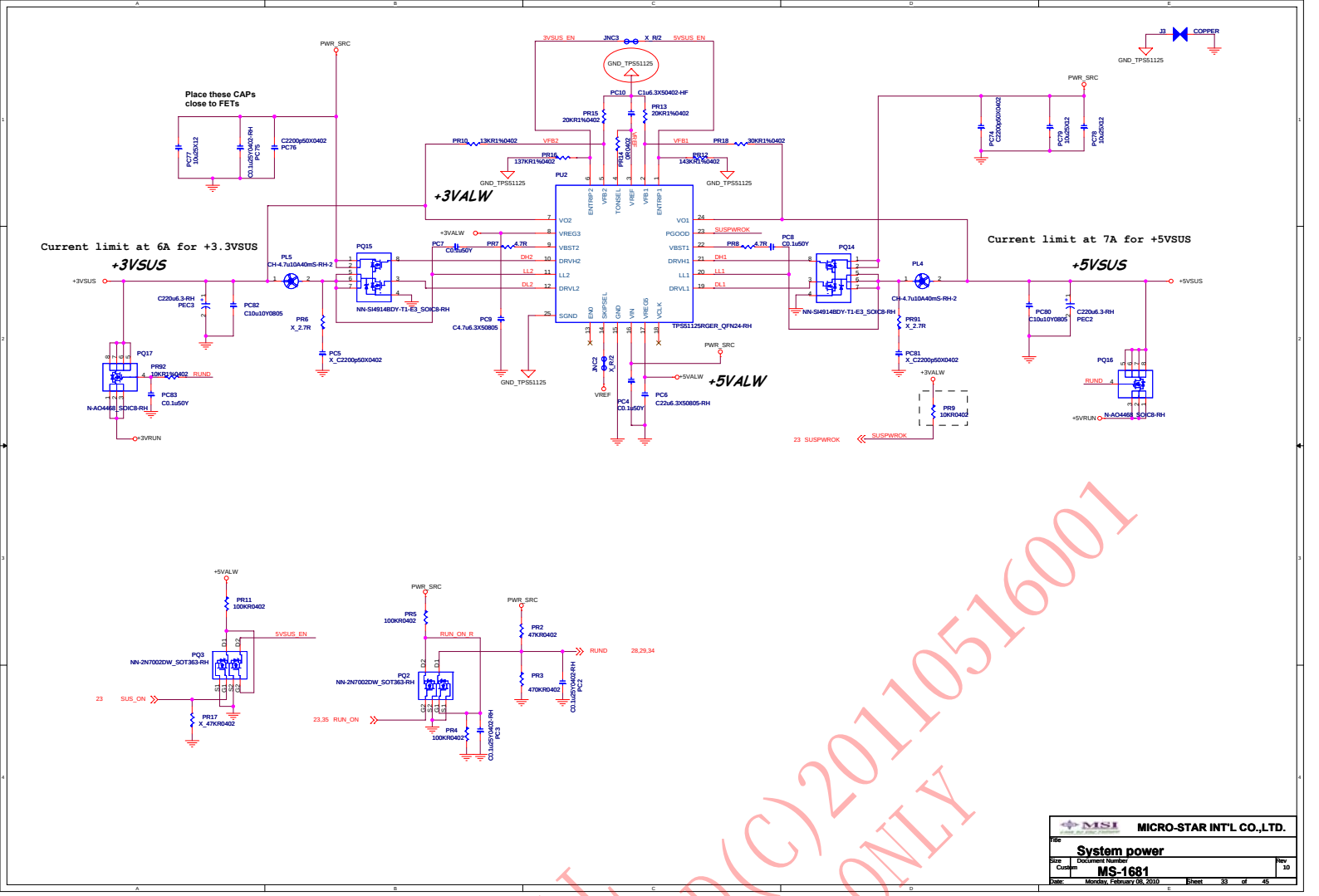
60013789 周小強 RD(C)20110516001
FOR RMA維修(劉松林) ONLY



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Title	System power
Size	Custom
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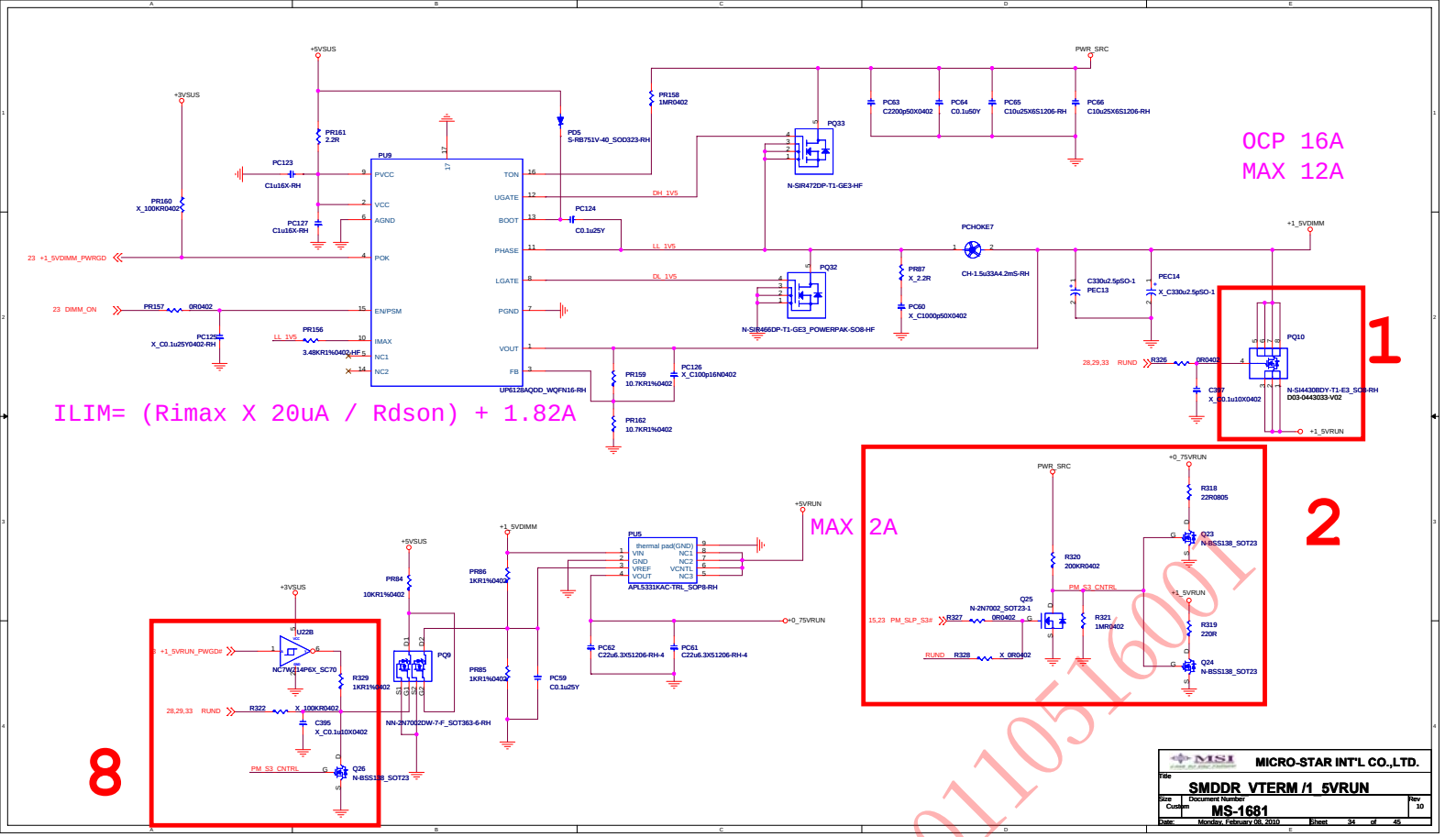

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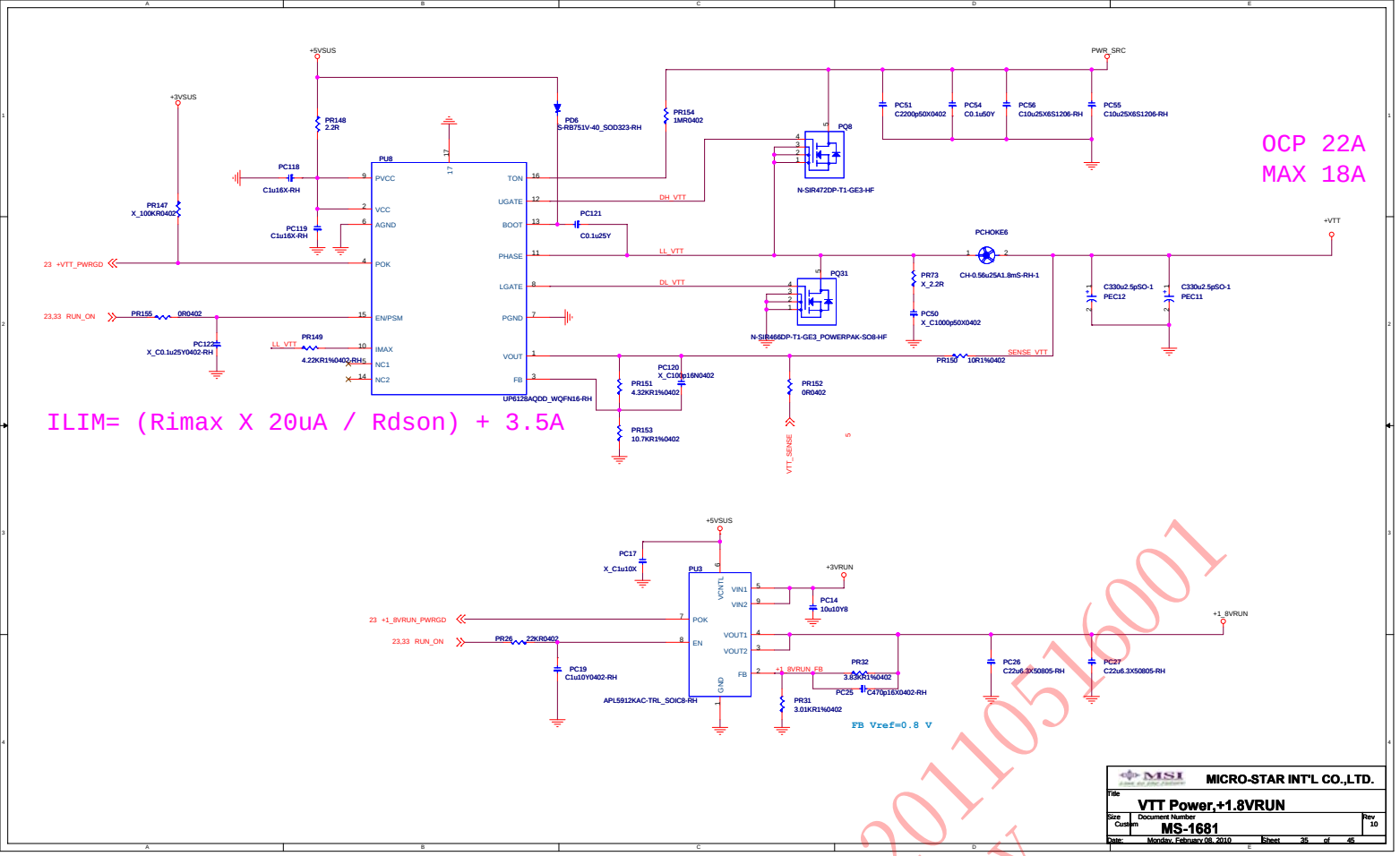
FOR RMA維修(劉松林) ONLY



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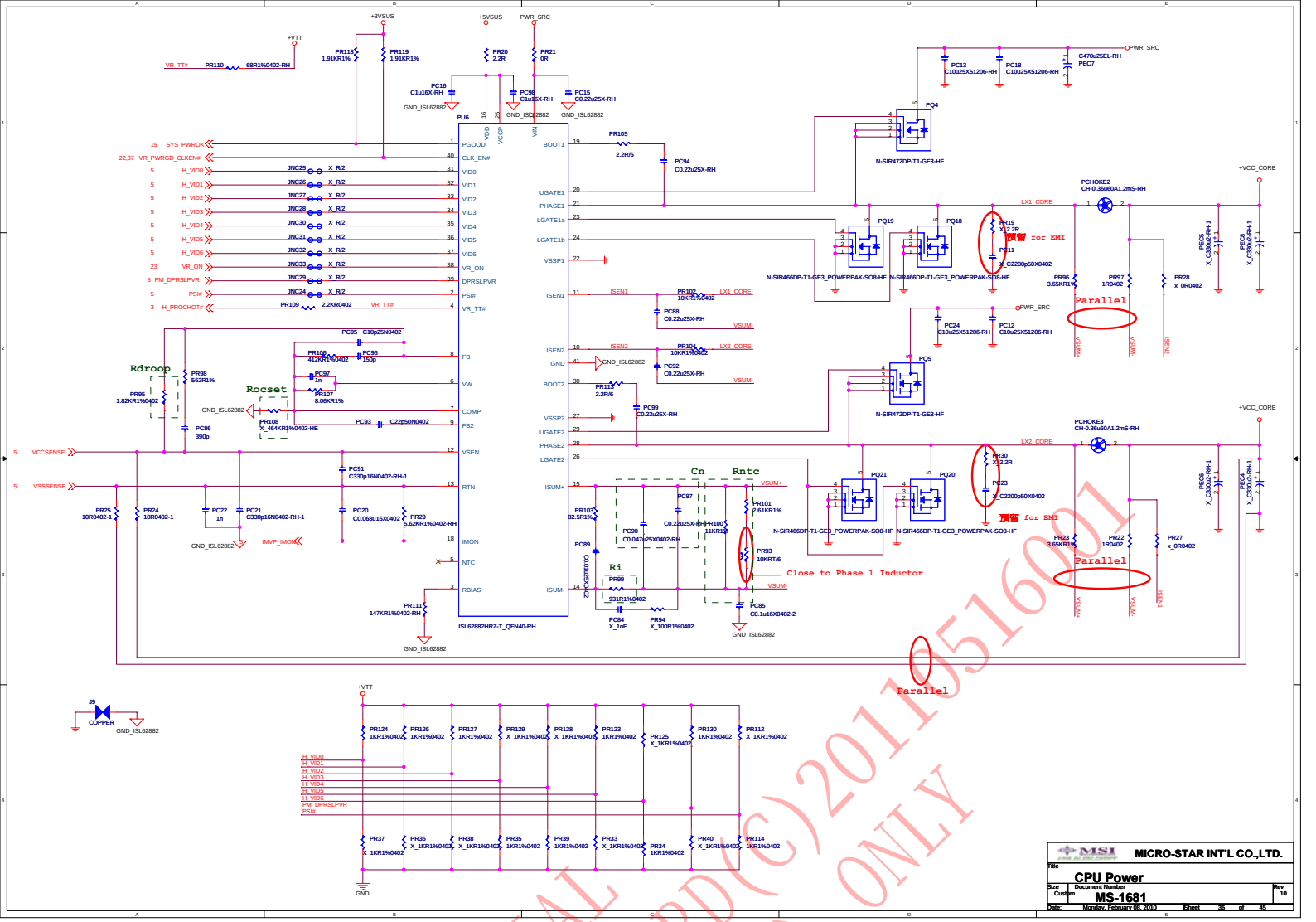
FOR RMA維修(劉松林) ONLY



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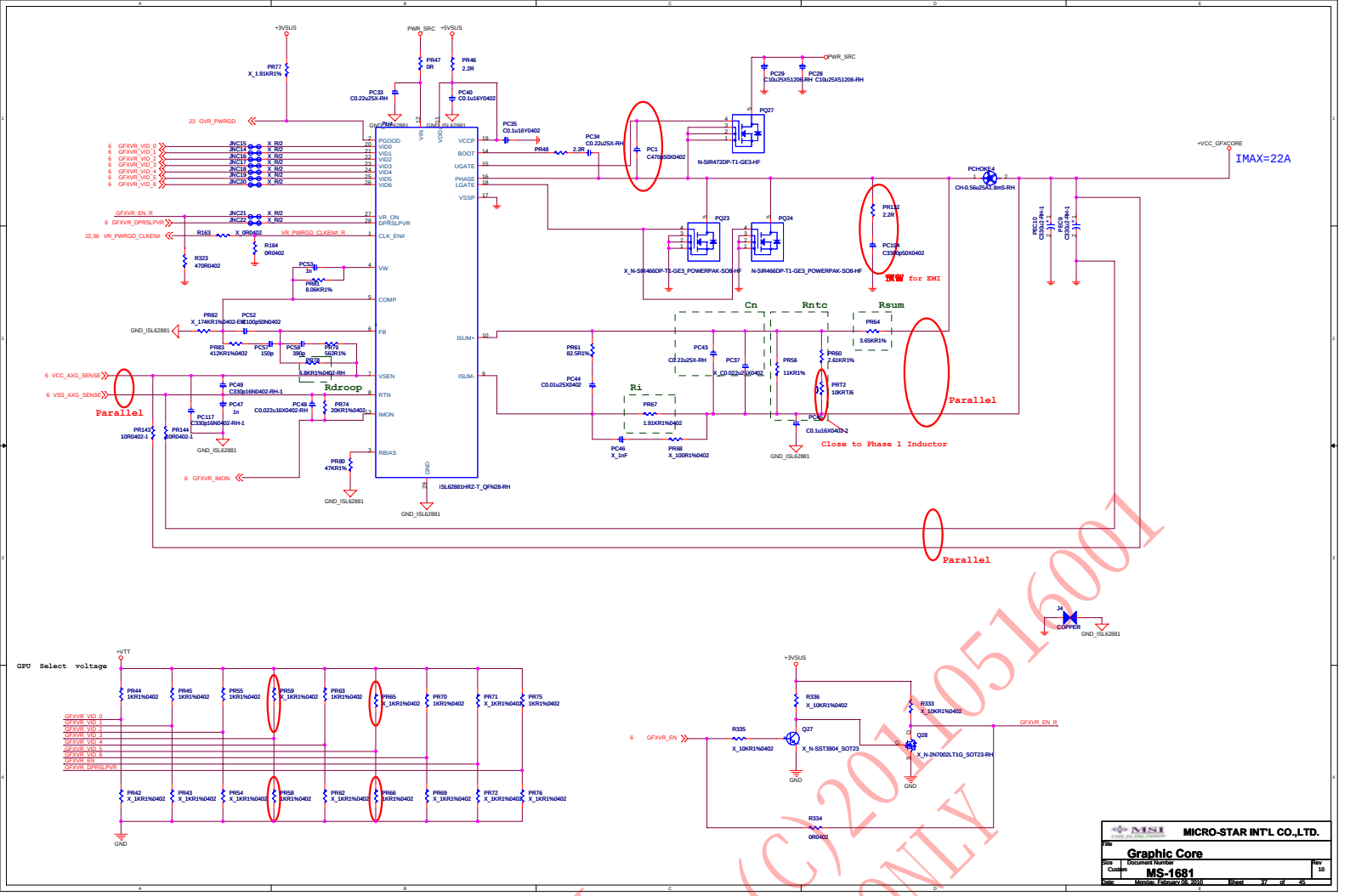
FOR RMA維修(劉松林) ONLY



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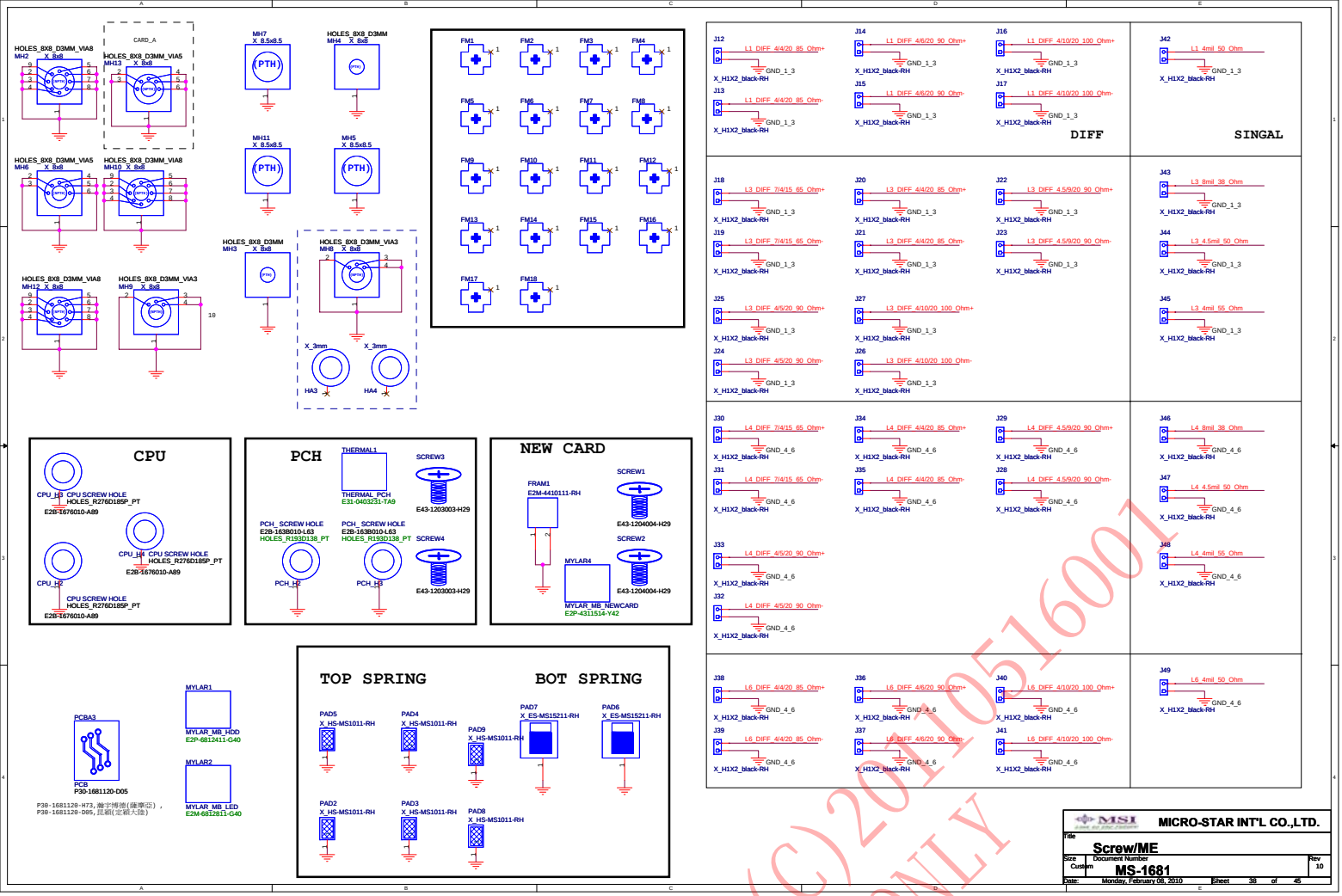
FOR RMA維修(劉松林) ONLY



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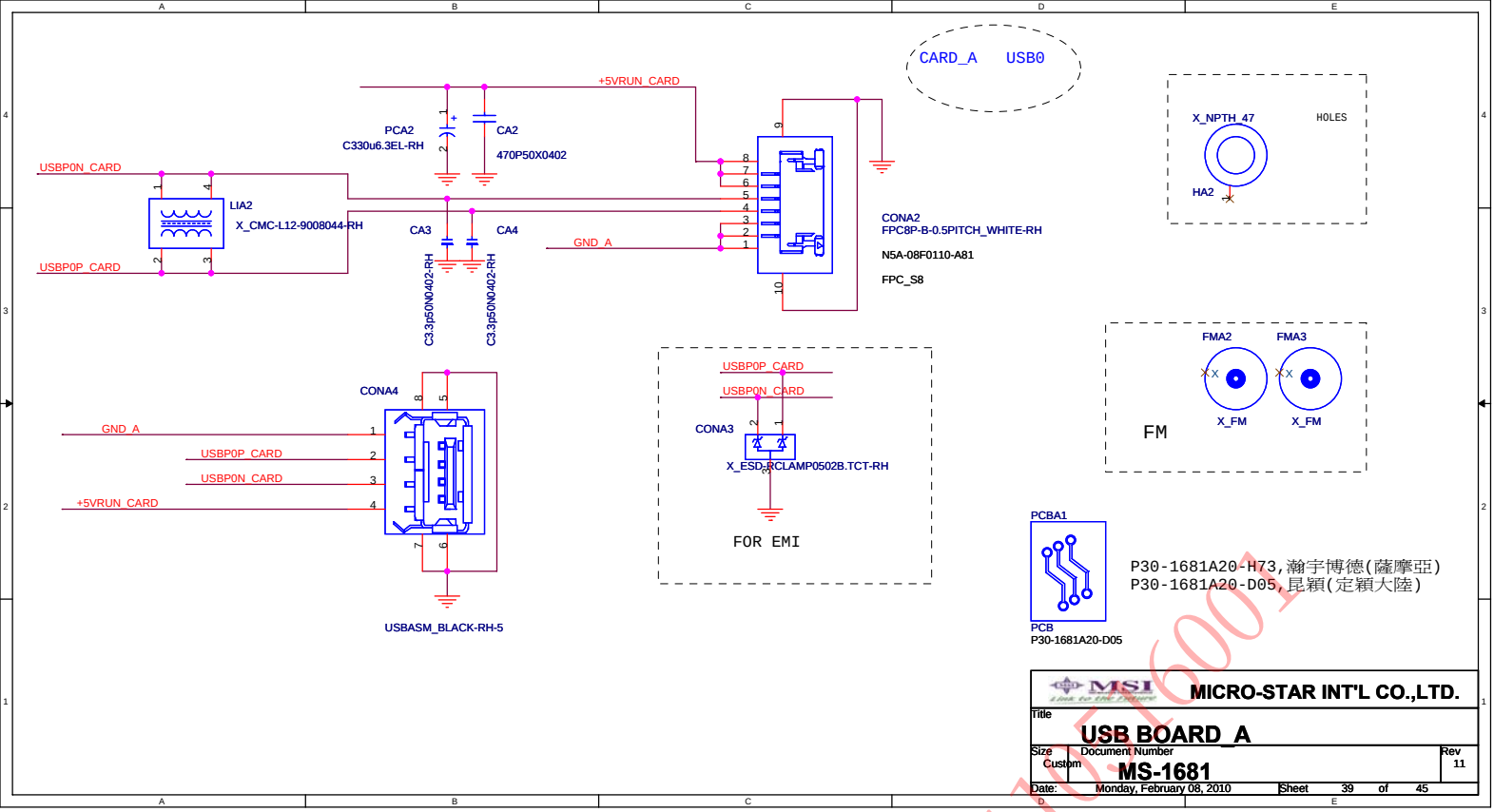

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60013789 周小強 RD(C)2010.1600
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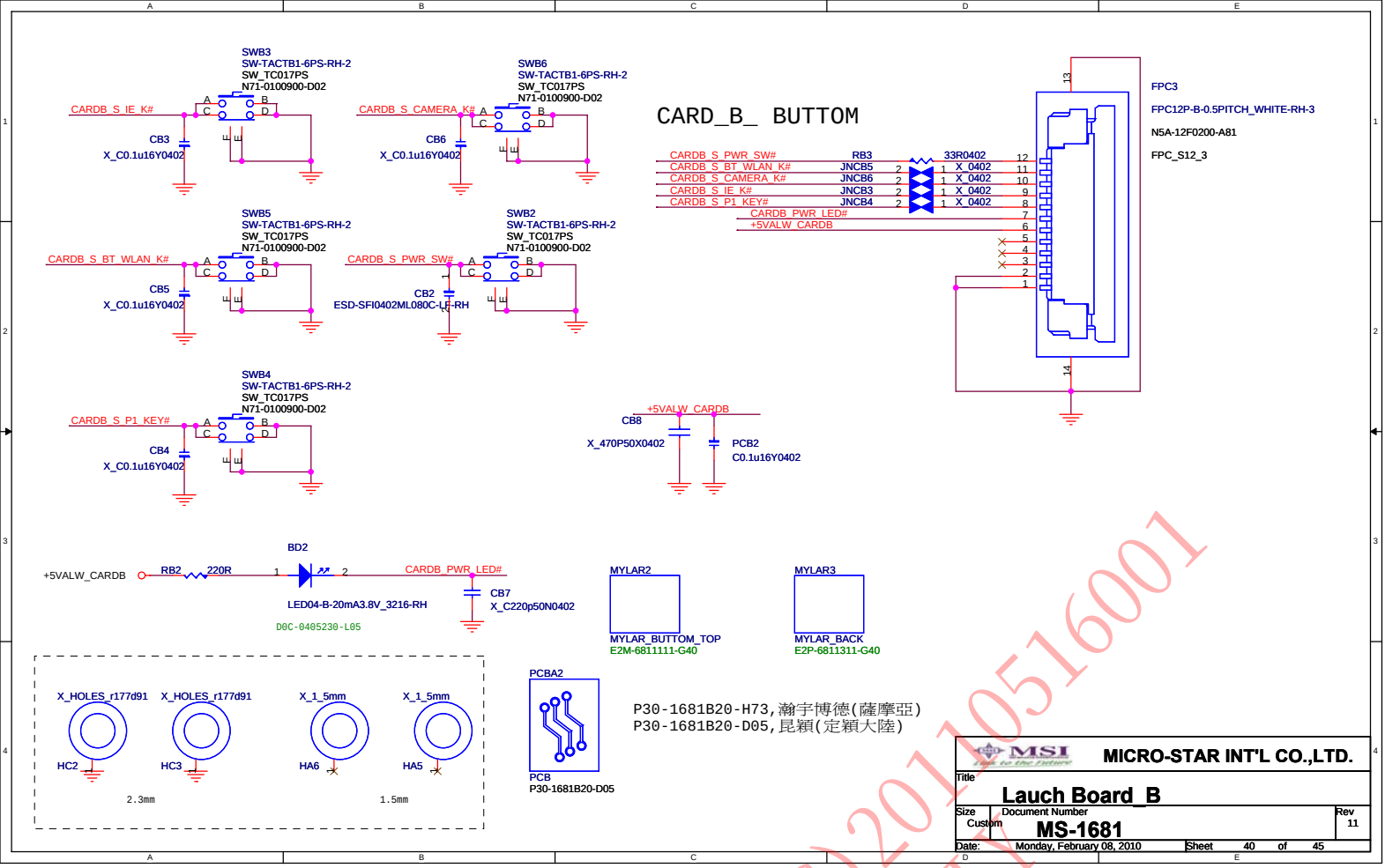

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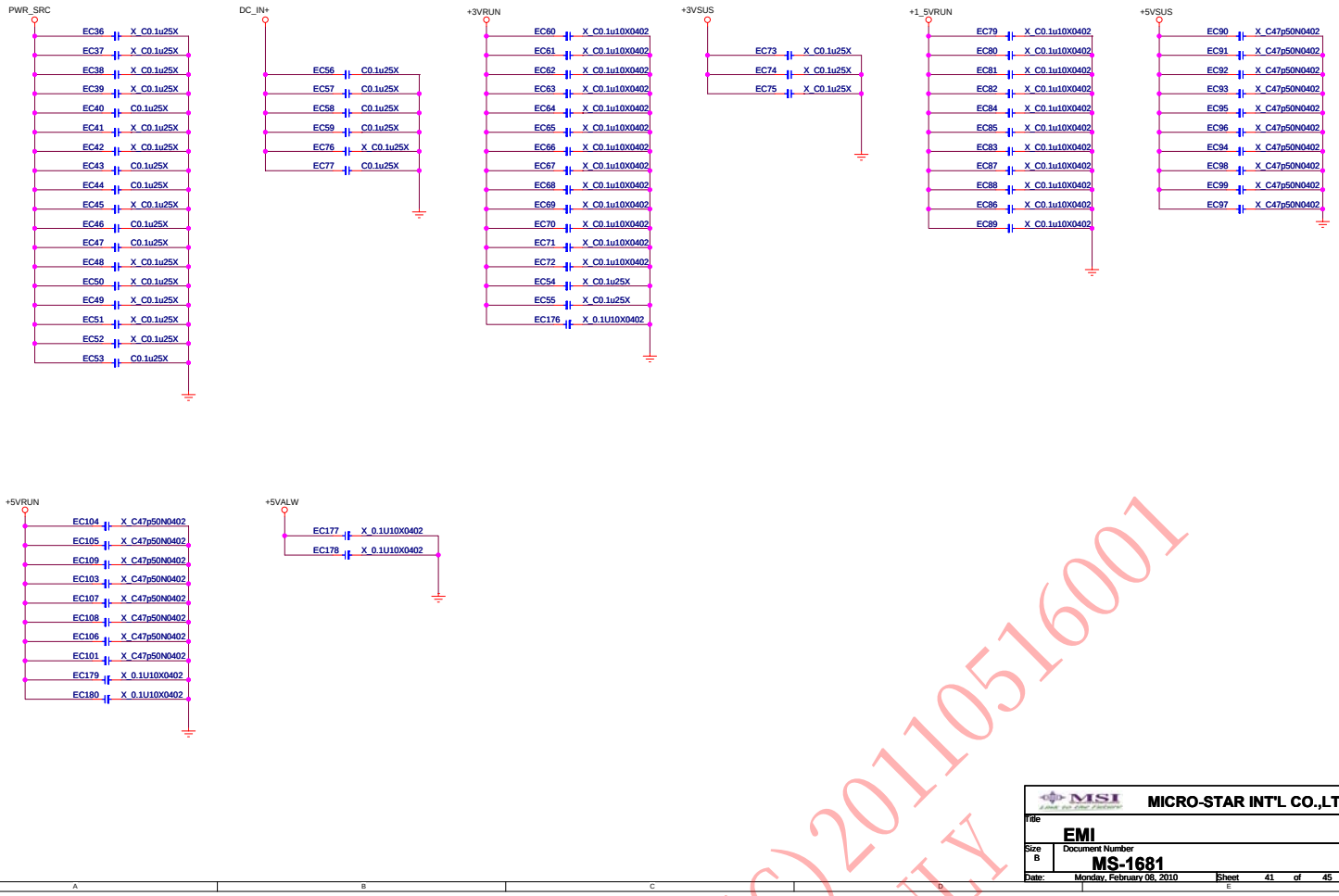

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Title: EMI

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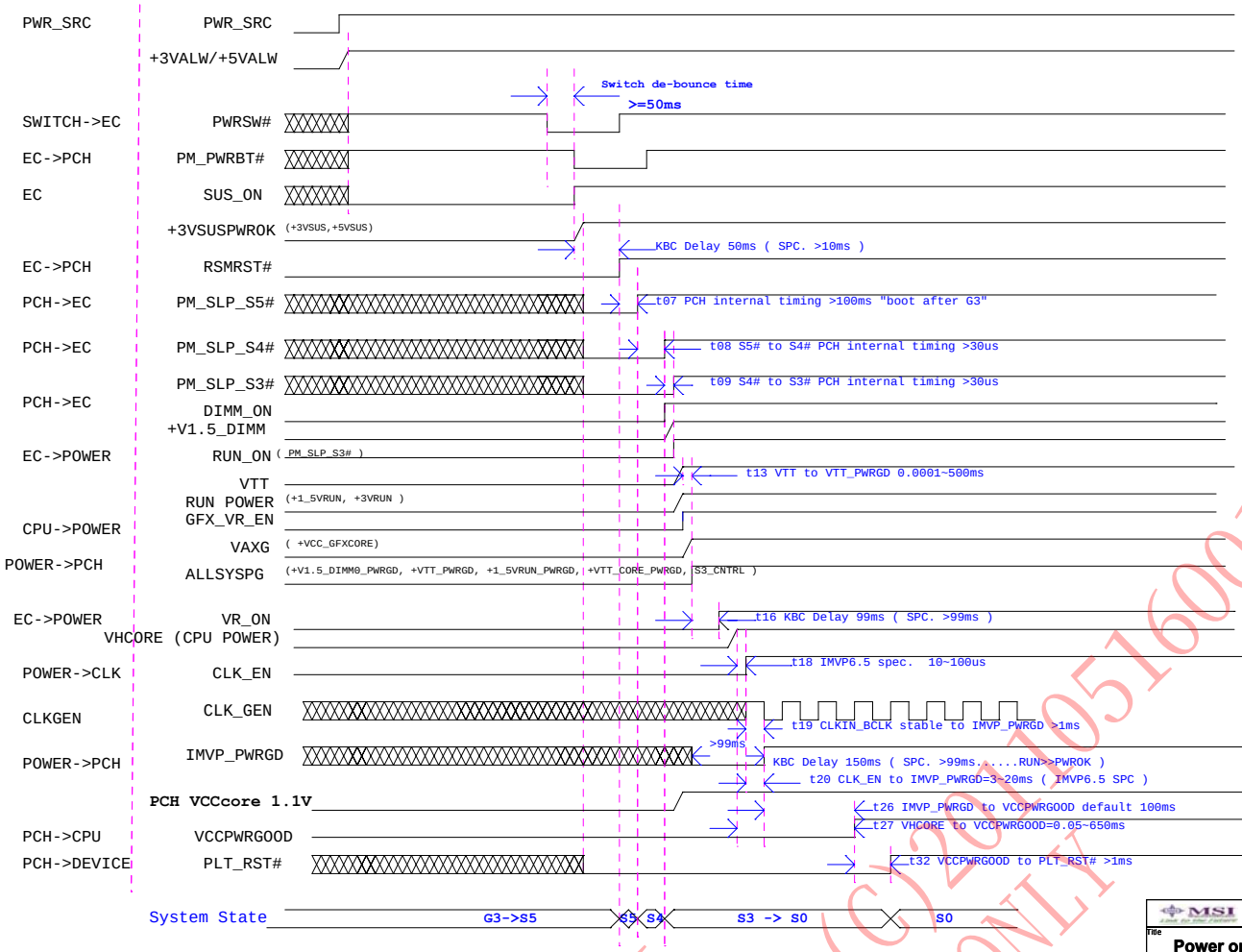
Calpella System Power on Sequence DC mode



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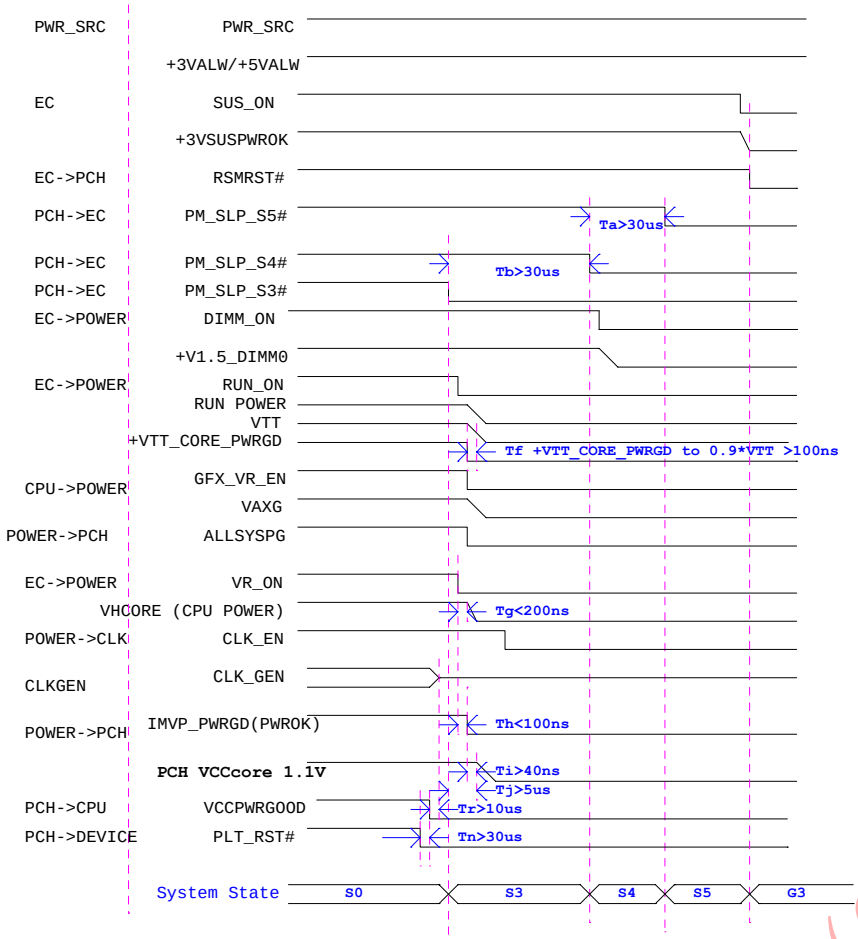
Power down Sequence DC mode S0 to G3



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Title: Power on Sequency			
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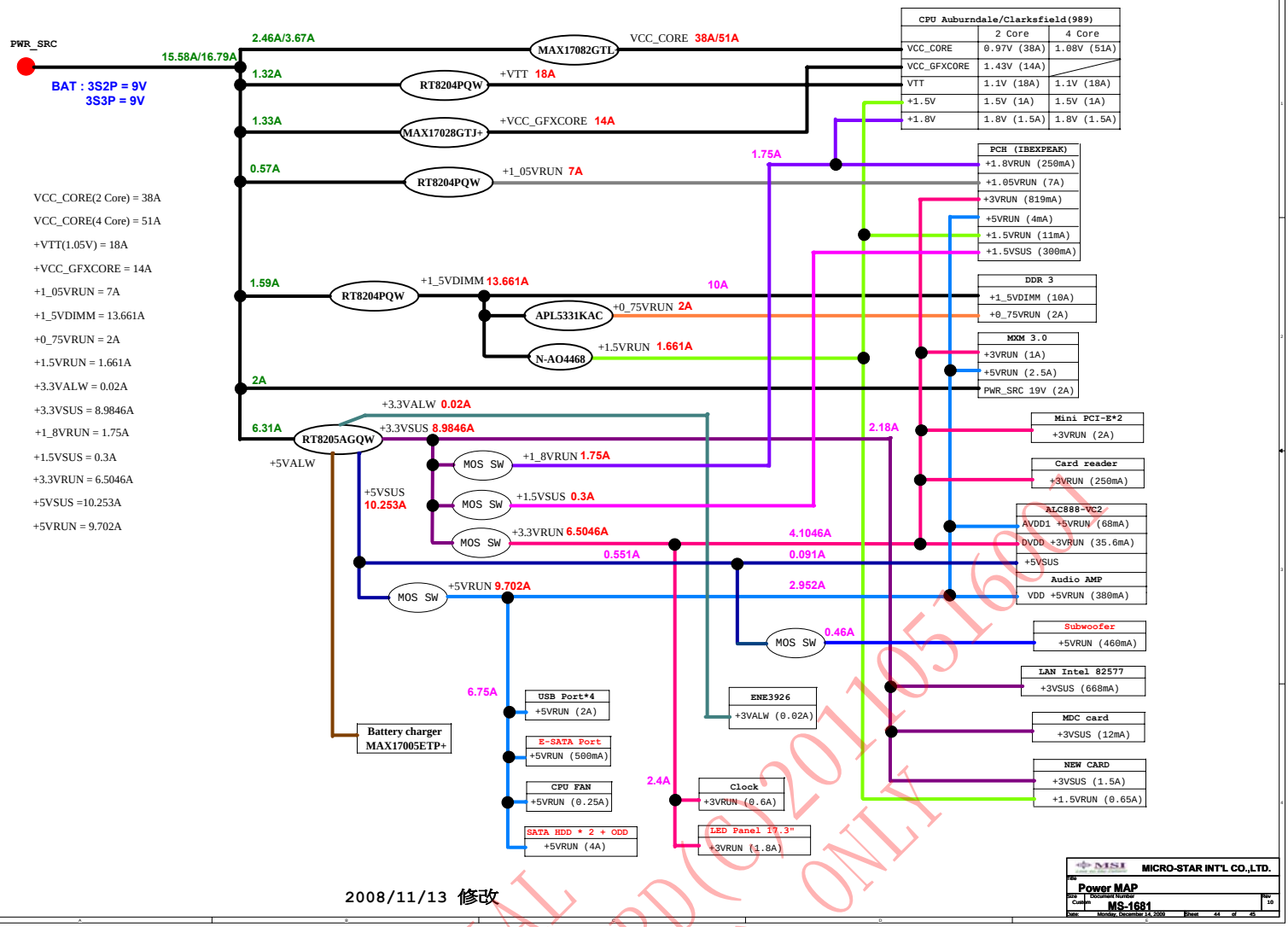

VCC_CORE(2 Core) = 38A

VCC_CORE(4 Core) = 51A

+VTT(1.05V) = 18A

+VCC_GFXCORE = 14A

+1_05VRUN = 7A

+1_5VDIMM = 13.661A

+0_75VRUN = 2A

+1.5VRUN = 1.661A

+3.3VALW = 0.02A

+3.3VSUS = 8.9846A

+1_8VRUN = 1.75A

+1.5VSUS = 0.3A

+3.3VRUN = 6.5046A

+5VSUS =10.253A

+5VRUN = 9.702A

2008/11/13 修改

MICRO-STAR INT'L CO.,LTD.

Power MAP

MS-1681

Monday, December 14, 2009

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Change Note :

0A-->0B

1.P19 stuff R113 & C85 for intel document about Braidwood

2.P23 add one PWM Pin for co-lay LED panel by EC

3.P25 Change CardReader to ENE

4.P26 Change "LED_HDD#" PU +5VRUN to +3VRUN

5.P26 Fan conn footprint change back to "53398_03"

6.P28 Add Wireless & Bluetooth combo(MS-3870)

7.P32 Change PR171 to 48.7K & PR172 to 1R0603

8.P33 Change PU2 from "UP6182AQAG" to "TPS51125" & PR18 to 30K

9.P34 Change PU9 from "UP6111AQDD" to "UP6128A" & PR156 to 3.48K & PR159 to 10.7K & PQ10 to "D03-0443033-V02"

10.P35 Change PU8 from "UP6111AQDD" to "UP6128A" & PR149 to 4.22K & remove C394

11.P36 Change PR95 to 1.82K & PR29 to 9.31K & PC90 to 47nf & PR99 to 931R & no stuff PC84 , PR94 , PEC4 , PEC5 , PEC6 , PEC8

0B-->10

1.P13 add net "TP_HDA_DOCK_EN#_R" for flash protect control.

2.P14 add wimax ac adepter schematic.

3.P23 add ENE GPIO13 for flash protect control.

4.P25 no stuff C399 & C400 for cardreader detect issus.

5.P26 change R307 from 0R to 33R for EMI.

6.P31 add 2 cap in +VBATA for EMI.

7.P34 change R329 from 0R to 1K for current limit.

8.P37 no stuff +VCC_GFXCOPE PQ23 no cost down.

9.P40 change JNCB2 to RB3 , and 33R for EMI.

10.P40 change CB2 from 0.1u to 300p for EMI.

11.P13 No stuff for MP ver PCH by R289 , R271 , R298 , R291 , R297 , R290.

10-->11

1.P37 add "PC1" & modify "PR12" & "PC104" for power shut down issue.

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