COMPAL CONFIDENTIAL

MODEL NAME : *QAL70/QAL71*
PCB NO : *LA-7741P(DAB00000810)*
BOM P/N : *4619EO31LXX*
GPIO MAP: *Rev1.1*

Dalmore 13 UMA

Ivy Bridge + Panther POINT

2012-04-11

REV : 1.0 (A00)

@ : Nopop Component
CONN@ : Connector Component

MB Type	BOM P/N	
TPM		1@
DTP		2@
SPI ON BOARD		@SPI
TAA		@TAA

CPU	CPU R1 P/N	CPU R3 P/N
SNB 2.3G (@SNB)	SA00004QX4L	SA00004QX5L
IVB 2.3G(@IVB)		
IVB 2.6G(@IVB)	SA00005JL1L	SA00005JK2L
IVB 2.8G(@IVB)	SA00005JK1L	SA00005JK2L
IVB 2.9G(@IVB)	SA00005JJ2L	SA00005JJ3L

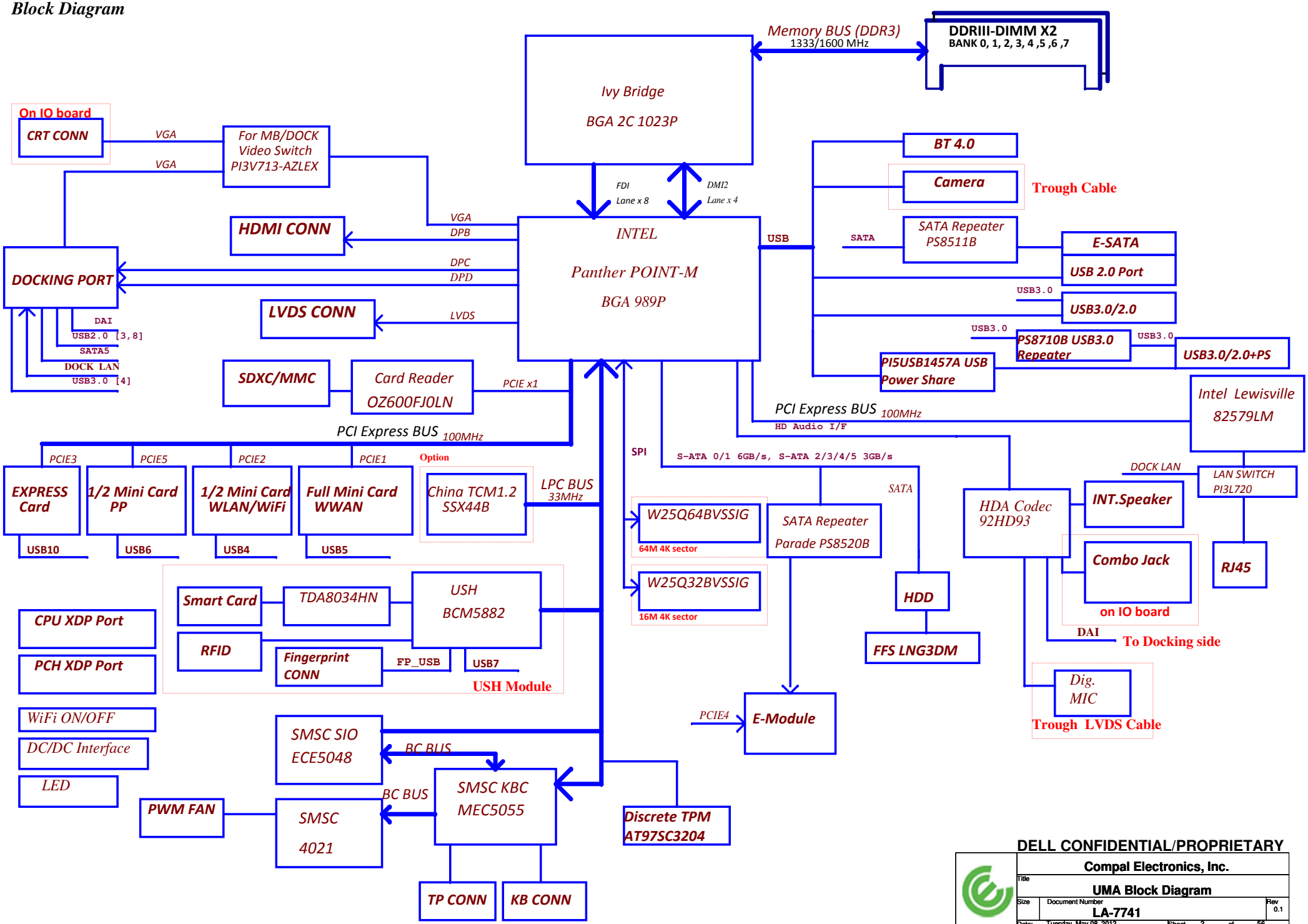
For SNB CPU: @SNB
For IVB CPU: @IVB

MB PCB

Part Number	Description
DAB00000810	PCB 0LK LA-7741P REV1 M/B

Compal Electronics, Inc.
Title: Cover Sheet
Size | Document Number: LA-7741 | Rev: 0.1
Date: Tuesday, May 08, 2012 | Sheet 1 of 56

Block Diagram



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Compal Electronics, Inc.		
Title: UMA Block Diagram		
Size	Document Number: LA-7741	Rev: 0.1
Date: Tuesday, May 08, 2012	Sheet 2 of 56	

POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane / State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and PM Table

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

	USB PORT#	DESTINATION
PCH	0	JUSB1 (Right side)
	1	JUSB2 (Rear Left side)
	2	NA
	3	MLK DOCK
	4	WLAN
	5	WWAN
	6	DOCKING
	7	USH->BIO
	8	JMINI3(PP)
	9	JESATA1 (right side)
	10	Express card
	11	Bluetooth
	12	Camera
	13	NA

USH	0	BIO
	1	NA

UMA DP/HDMI Port	Connetion
Port B	MB HDMI Conn
Port C	Dock DP port 2
Port D	Dock DP port 1

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

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Title: Index and Config.

Size | Document Number: LA-7741 | Rev: 0.1

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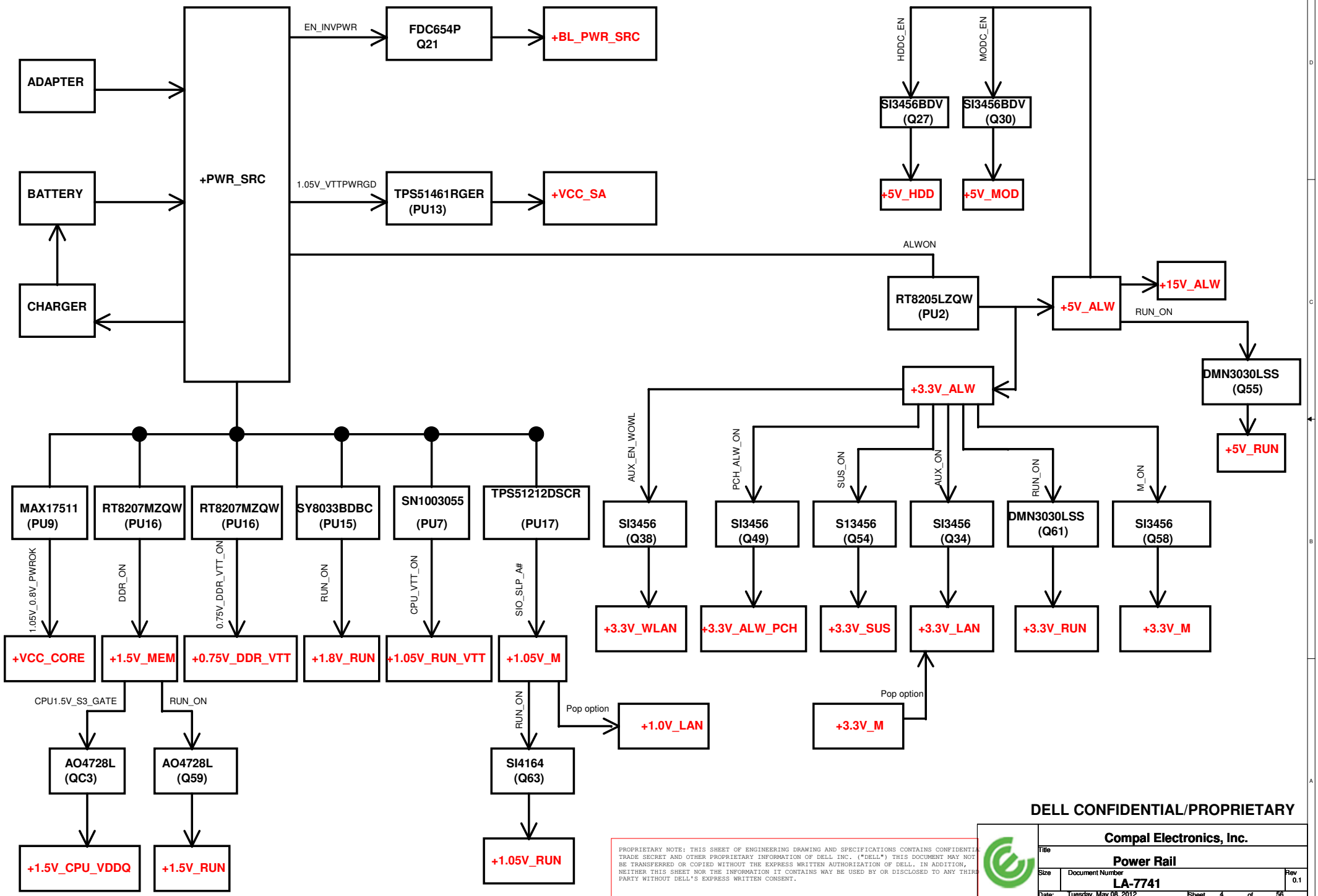

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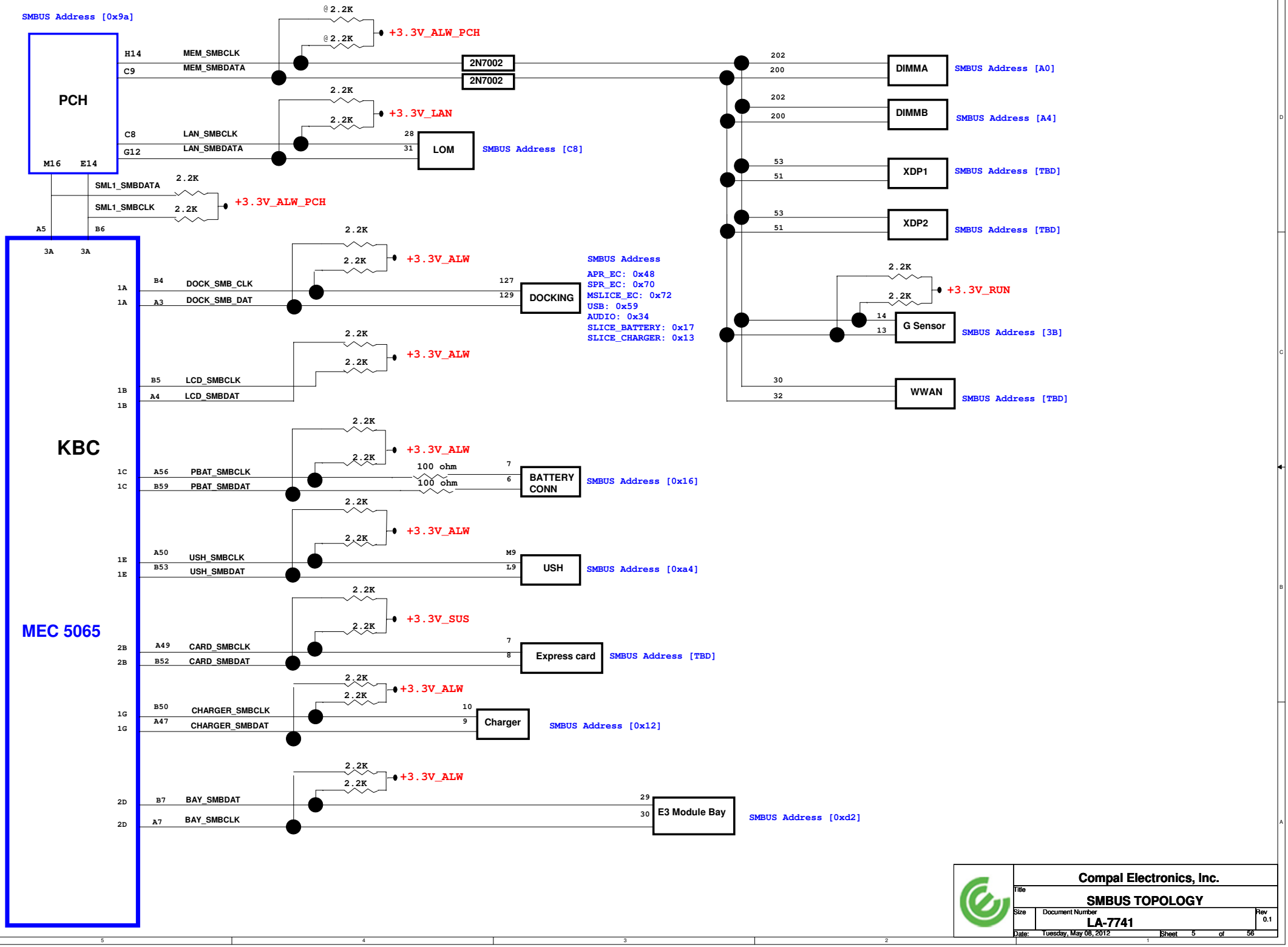
Title: Power Rail

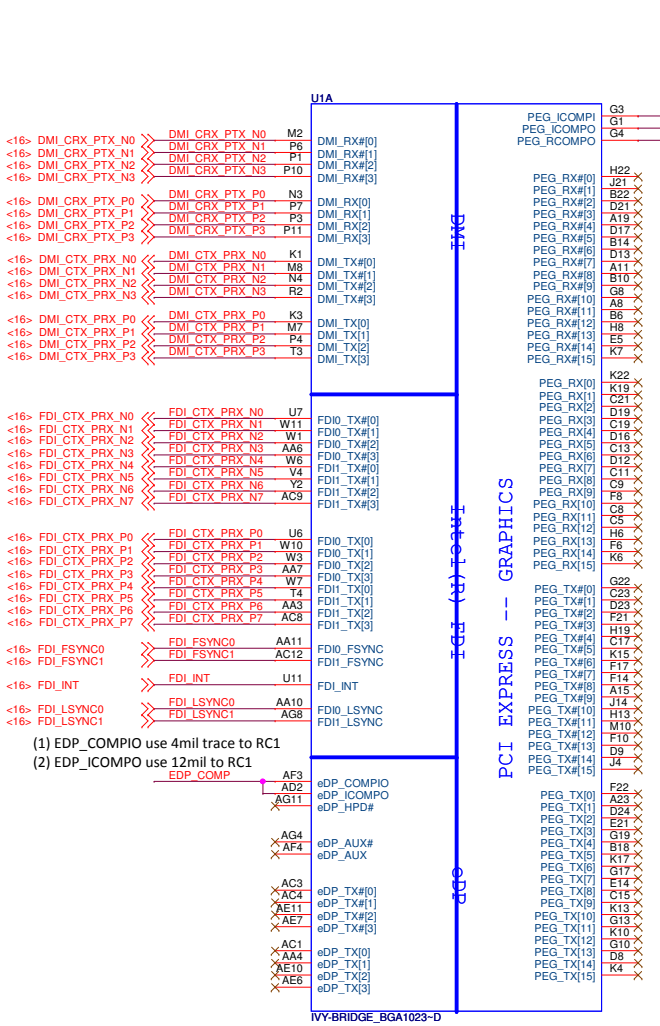
Size | Document Number: LA-7741 | Rev: 0.1

Date: Tuesday, May 08, 2012 | Sheet 4 of 56



Compal Electronics, Inc.		
Title: SMBUS TOPOLOGY		
Size	Document Number: LA-7741	Rev: 0.1
Date: Tuesday, May 08, 2012	Sheet 5 of 56	

(1)PEG_RCOMPO (G4) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC2.
(2)PEG_ICOMPO use 12mil connect to RC2



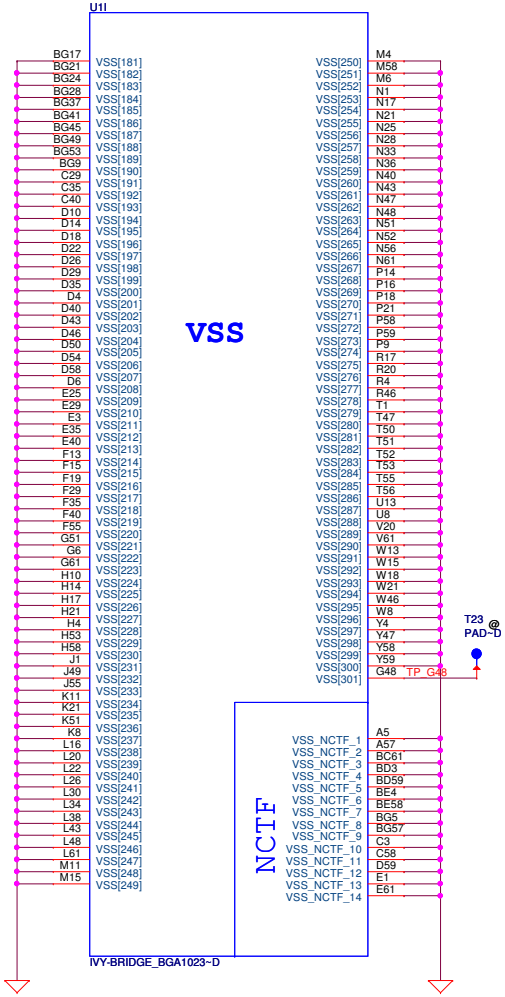
(1) EDP_COMPIO use 4mil trace to RC1
(2) EDP_ICOMPO use 12mil to RC1

+1.05V_RUN_VTT

RC2
24.9_0402_1%~D

PEG Compensation

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



eDP Compensation

+1.05V_RUN_VTT

RC1
24.9_0402_1%~D

EDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Compal Electronics, Inc.

Title: Sandy Bridge (1/6)

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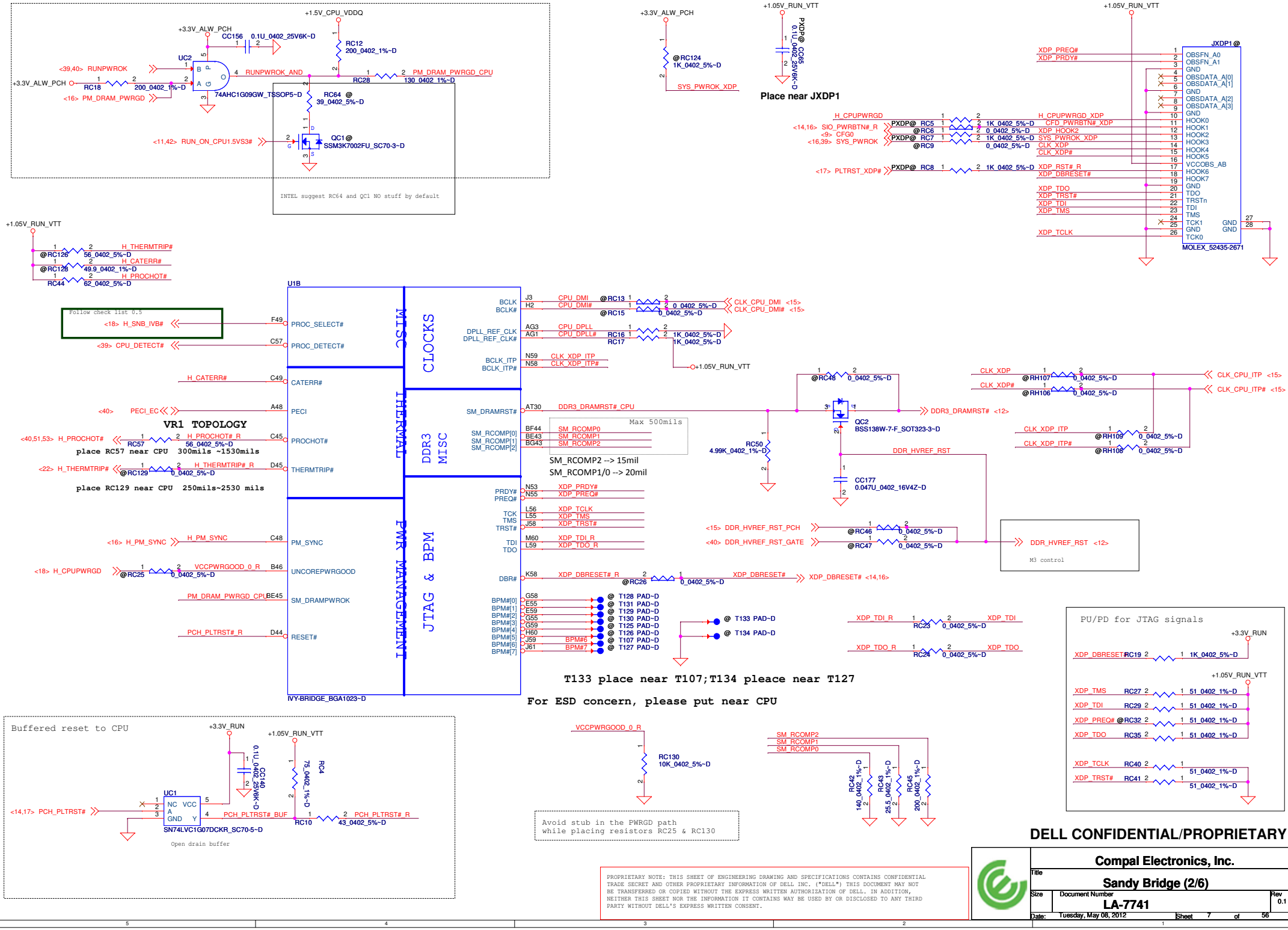
Date: Tuesday, May 08, 2012 | Sheet 6 of 56


+1.5V_CPU_VDDQ
+3.3V_ALW_PCH
CC156 0.1U_0402_25V6K~D
RC12 200_0402_1%~D
UC2
<39,40> RUNPWROK
RUNPWROK_AND
PM_DRAM_PWRGD_CPU
RC18 200_0402_1%~D
<16> PM_DRAM_PWRGD
74AHC1G09GW_TSSOP5~D
RC28 130_0402_1%~D
RC64 @ 39_0402_5%~D
<11,42> RUN_ON_CPU1.5VS3#
QC1@ SSM3K7002FU_SC70-3~D
INTEL suggest RC64 and QC1 NO stuff by default
+3.3V_ALW_PCH
@RC124 1K_0402_5%~D
SYS_PWROK_XDP
+1.05V_RUN_VTT
PXDP@ CC65 0.1U_0402_25V6K~D
Place near JXDP1
+1.05V_RUN_VTT
JXDP1@
XDP_PREQ#
XDP_PRDY#
OBSFN_A0
OBSFN_A1
OBSDATA_A[0]
OBSDATA_A[1]
OBSDATA_A[2]
OBSDATA_A[3]
H_CPUPWRGD
<14,16> SIO_PWRBTN#_R
<9> CFG0
<16,39> SYS_PWROK
PXDP@ RC5
@RC6
PXDP@ RC7
@RC9
1K_0402_5%~D
0_0402_5%~D
H_CPUPWRGD_XDP
CFD_PWRBTN#_XDP
XDP_HOOK2
SYS_PWROK_XDP
CLK_XDP
CLK_XDP#
<17> PLTRST_XDP#
PXDP@ RC8
XDP_RST#_R
XDP_DBRESET#
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
XDP_TCLK
HOOK0
HOOK1
HOOK2
HOOK3
HOOK4
HOOK5
VCCOBS_AB
HOOK6
HOOK7
TDO
TRSTn
TDI
TMS
TCK1
TCK0
GND
MOLEX_52435-2671
+1.05V_RUN_VTT
@RC126 56_0402_5%~D H_THERMTRIP#
@RC128 49.9_0402_1%~D H_CATERR#
RC44 62_0402_5%~D H_PROCHOT#
U1B
Follow check list 0.5
<18> H_SNB_IVB#
<39> CPU_DETECT#
H_CATERR#
<40> PECI_EC
VR1 TOPOLOGY
<40,51,53> H_PROCHOT#
RC57 56_0402_5%~D
H_PROCHOT#_R
place RC57 near CPU 300mils ~1530mils
<22> H_THERMTRIP#
@RC129 0_0402_5%~D
H_THERMTRIP#_R
place RC129 near CPU 250mils~2530 mils
<16> H_PM_SYNC
H_PM_SYNC
<18> H_CPUPWRGD
@RC25 0_0402_5%~D
VCCPWRGOOD_0_R
PM_DRAM_PWRGD_CPU
PCH_PLTRST#_R
F49 PROC_SELECT#
C57 PROC_DETECT#
C49 CATERR#
A48 PECI
C45 PROCHOT#
D45 THERMTRIP#
C48 PM_SYNC
B46 UNCOREPWRGOOD
BE45 SM_DRAMPWROK
D44 RESET#
MISC
CLOCKS
DDR3
MISC
JTAG & BPM
PWR MANAGEMENT
BCLK
BCLK#
J3 CPU_DMI
H2 CPU_DMI#
@RC13
@RC15
0_0402_5%~D
CLK_CPU_DMI <15>
CLK_CPU_DMI# <15>
DPLL_REF_CLK
DPLL_REF_CLK#
AG3 CPU_DPLL
AG1 CPU_DPLL#
RC16
RC17
1K_0402_5%~D
BCLK_ITP
BCLK_ITP#
N59 CLK_XDP_ITP
N58 CLK_XDP_ITP#
+1.05V_RUN_VTT
SM_DRAMRST#
AT30 DDR3_DRAMRST#_CPU
Max 500mils
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]
BF44 SM_RCOMP0
BE43 SM_RCOMP1
BG43 SM_RCOMP2
SM_RCOMP2 --> 15mil
SM_RCOMP1/0 --> 20mil
PRDY#
PREQ#
N53 XDP_PRDY#
N55 XDP_PREQ#
TCK
TMS
TRST#
L56 XDP_TCLK
L55 XDP_TMS
J58 XDP_TRST#
TDI
TDO
M60 XDP_TDI_R
L59 XDP_TDO_R
DBR#
K58 XDP_DBRESET#_R
@RC26
0_0402_5%~D
XDP_DBRESET#
XDP_DBRESET# <14,16>
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]
G58 @ T128 PAD~D
E55 @ T131 PAD~D
E59 @ T129 PAD~D
G55 @ T130 PAD~D
G59 @ T125 PAD~D
H60 @ T126 PAD~D
J59 BPM#6 @ T107 PAD~D
J61 BPM#7 @ T127 PAD~D
@ T133 PAD~D
@ T134 PAD~D
IVY-BRIDGE_BGA1023~D
@RC48 0_0402_5%~D
QC2 BSS138W-7-F_SOT323-3~D
DDR3_DRAMRST# <12>
RC50 4.99K_0402_1%~D
CC177 0.047U_0402_16V4Z~D
DDR_HVREF_RST
CLK_XDP
CLK_XDP#
@RH107 0_0402_5%~D
@RH106 0_0402_5%~D
CLK_CPU_ITP <15>
CLK_CPU_ITP# <15>
CLK_XDP_ITP
CLK_XDP_ITP#
@RH109 0_0402_5%~D
@RH108 0_0402_5%~D
<15> DDR_HVREF_RST_PCH
<40> DDR_HVREF_RST_GATE
@RC46 0_0402_5%~D
@RC47 0_0402_5%~D
DDR_HVREF_RST <12>
M3 control
T133 place near T107;T134 pleace near T127
For ESD concern, please put near CPU
XDP_TDI_R
RC23 0_0402_5%~D
XDP_TDI
XDP_TDO_R
RC24 0_0402_5%~D
XDP_TDO
PU/PD for JTAG signals
+3.3V_RUN
XDP_DBRESET#
RC19 1K_0402_5%~D
+1.05V_RUN_VTT
XDP_TMS RC27 51_0402_1%~D
XDP_TDI RC29 51_0402_1%~D
XDP_PREQ# @RC32 51_0402_1%~D
XDP_TDO RC35 51_0402_1%~D
XDP_TCLK RC40 51_0402_1%~D
XDP_TRST# RC41 51_0402_1%~D
Buffered reset to CPU
+3.3V_RUN
+1.05V_RUN_VTT
CC140 0.1U_0402_25V6K~D
RC4 75_0402_1%~D
UC1
<14,17> PCH_PLTRST#
NC VCC A GND Y
SN74LVC1G07DCKR_SC70-5~D
PCH_PLTRST#_BUF
RC10 43_0402_5%~D
PCH_PLTRST#_R
Open drain buffer
VCCPWRGOOD_0_R
RC130 10K_0402_5%~D
Avoid stub in the PWRGD path
while placing resistors RC25 & RC130
SM_RCOMP2
SM_RCOMP1
SM_RCOMP0
RC42 140_0402_1%~D
RC43 25.5_0402_1%~D
RC45 200_0402_1%~D
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Title
Sandy Bridge (2/6)
Size
Document Number
LA-7741
Rev
0.1
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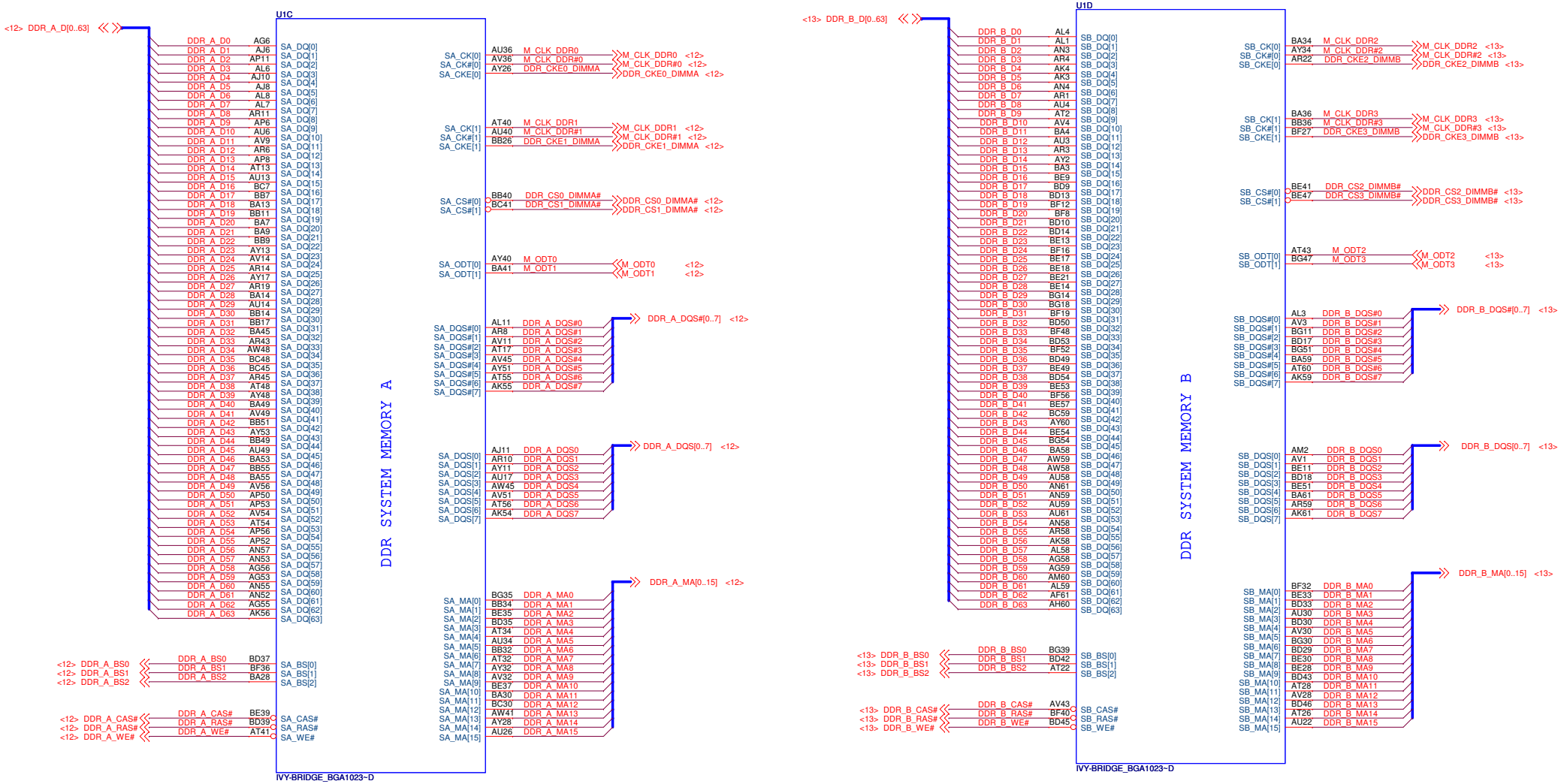

Compal Electronics, Inc.

Title: Sandy Bridge (3/6)

Size | Document Number: LA-7741 | Rev: 0.1

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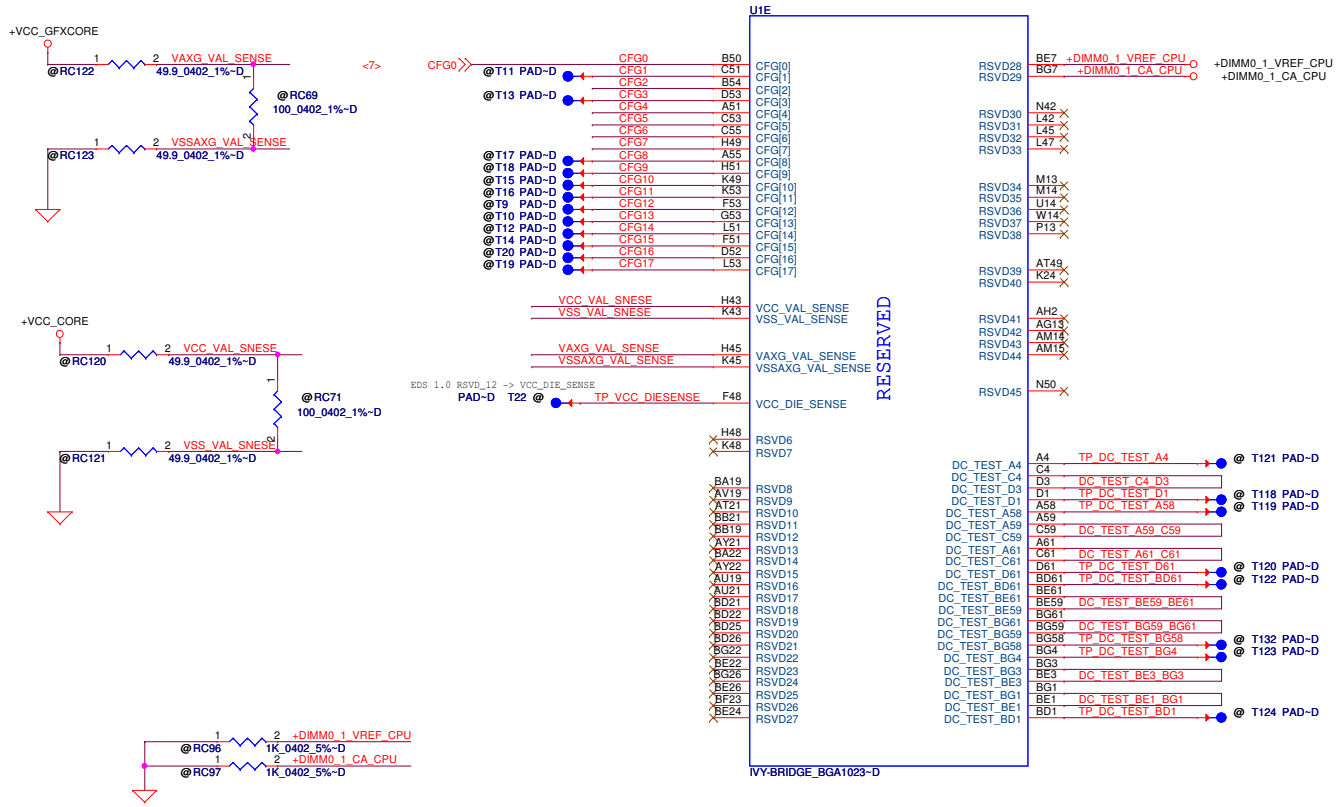
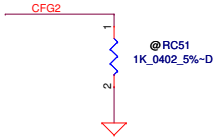
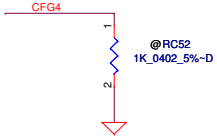


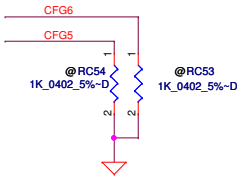
CFG Straps for Processor



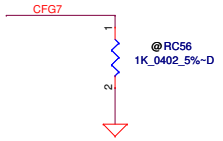
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: Sandy Bridge (4/6)

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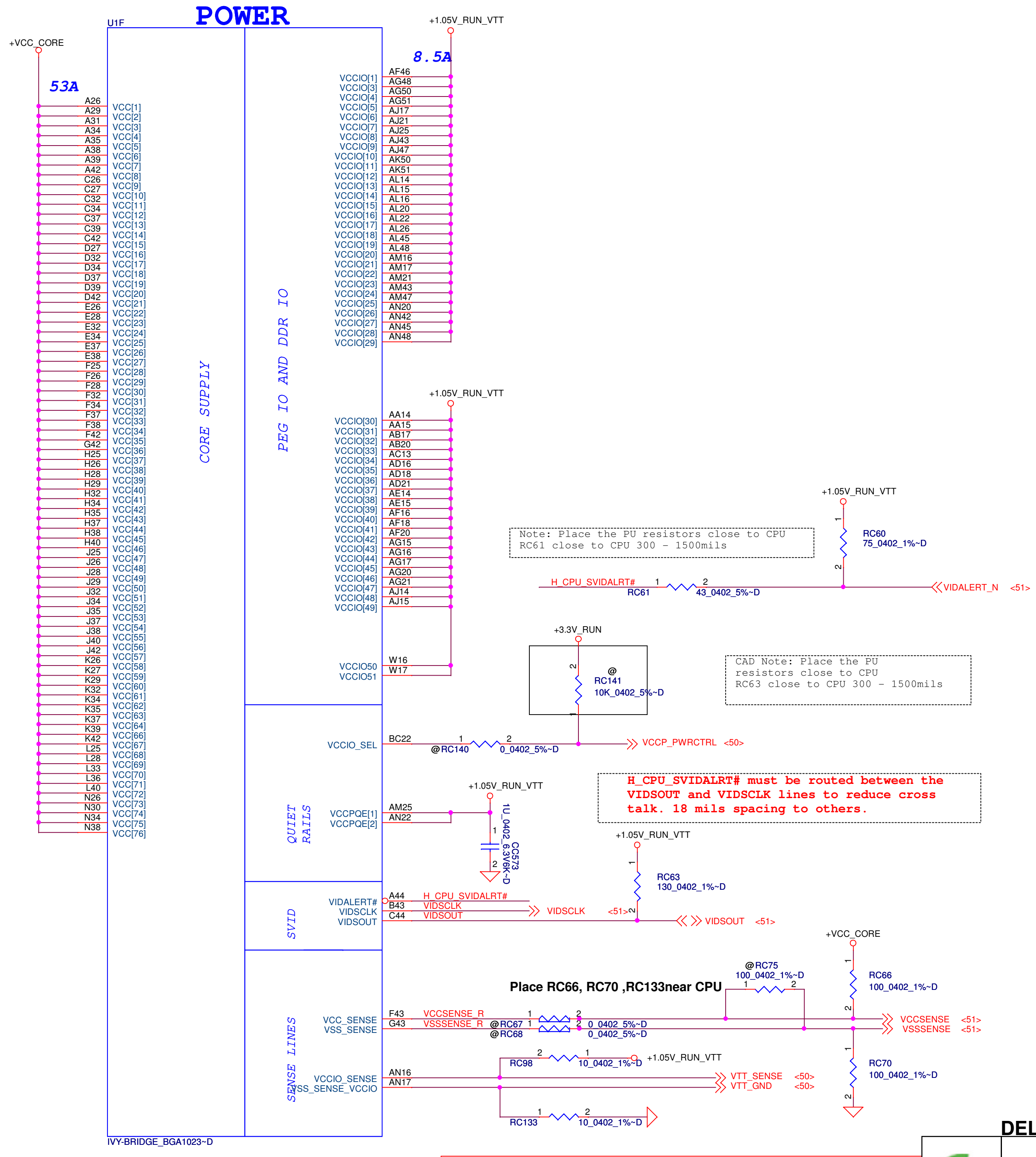
POWER



Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05/1	8.5
VAXG	0.0-1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 ★

★ Description

5A to Mem controller(+1.5V_CPU_VDDQ)
5-6A to 2 DIMMs/channel
2-5A to +1.5V_RUN & +0.75V_DDR_VTT

Compal Electronics, Inc.

Title: Sandy Bridge (5/6)

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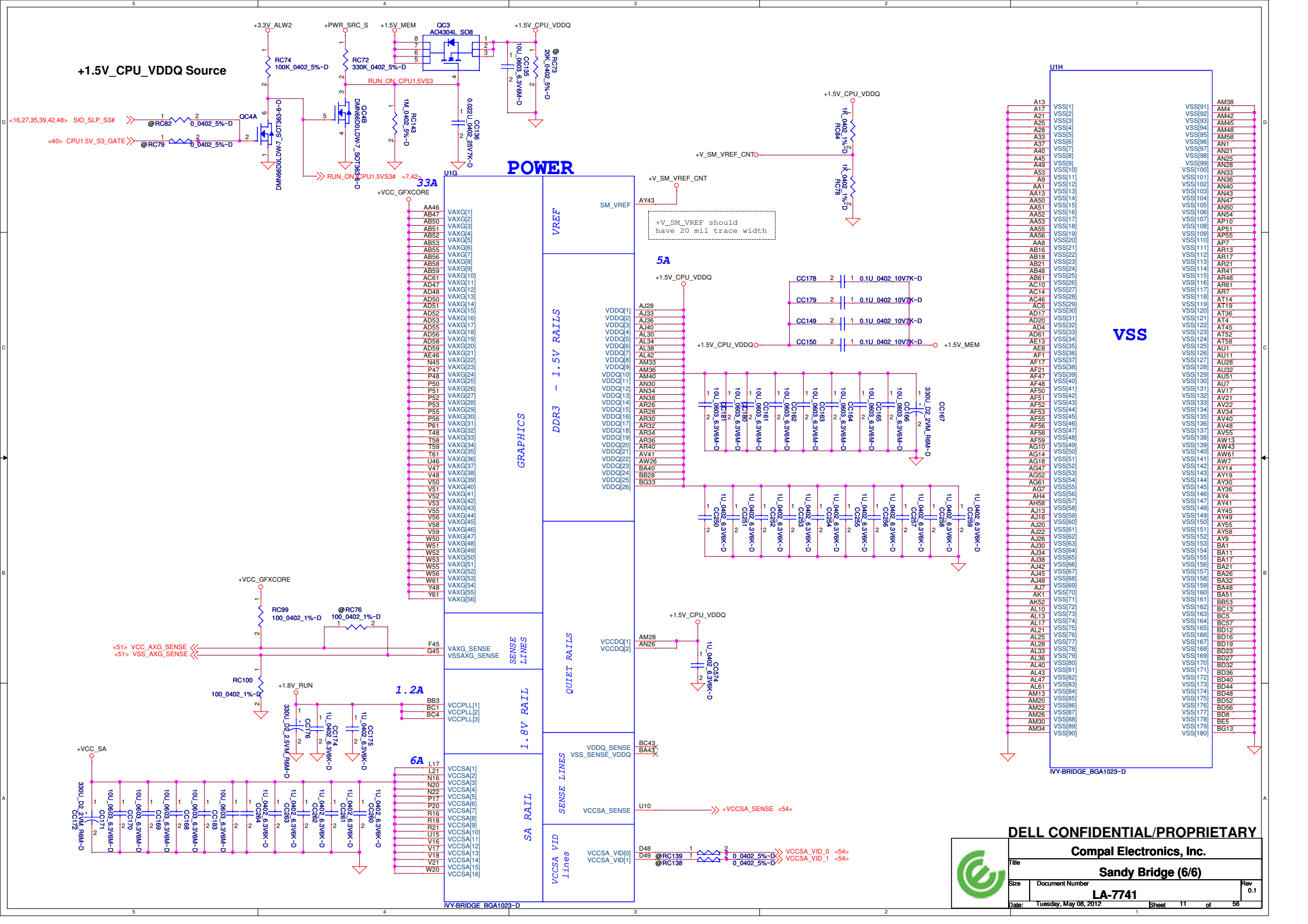
+1.5V_CPU_VDDQ Source
POWER
VSS
GRAPHICS
DDR3 - 1.5V RAILS
VREF
SENSE LINES
1.8V RAIL
QUIET RAILS
SA RAIL
VCCSA VID lines
IVY-BRIDGE_BGA1023~D
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Compal Electronics, Inc.
Sandy Bridge (6/6)
LA-7741
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JDIMM1 H=4

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMM1.203,204

M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

JDIMM1

TYCO_2-2013022-2-D

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Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size | Document Number: LA-7741 | Rev: 0.1

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2-3A to 1 DIMMs/channel

JDIMMB H=8

Populate RD4, De-Populate RD8 for Intel DDR3 VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3 VREFDQ multiple methods M3

<8> DDR_B_DQS#[0..7]
<8> DDR_B_D[0..63]
<8> DDR_B_DQS[0..7]
<8> DDR_B_MA[0..15]

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM2

Layout Note: Place near JDIMM2.203,204

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

+V_DDR_REFB_M3 — @RD8 0_0402_5%~D — +DIMM2_VREF_DQ
+V_DDR_REF — @RD4 0_0402_5%~D — +DIMM2_VREF_DQ
+DIMM2_VREF_DQ — CD23 2.2U_0402_6.3V6M; CD24 0.1U_0402_25V6K~D

JDIMM2 CONN@ TYCO_2-2013297-2~D

		+1.5V_MEM	1	VREF_DQ	VSS	2	+1.5V_MEM
			3	VSS	DQ4	4	DDR_B_D4
DDR_B_D0			5	DQ0	DQ5	6	DDR_B_D5
DDR_B_D1			7	DQ1	VSS	8	
			9	VSS	DQS0#	10	DDR_B_DQS#0
			11	DM0	DQS0	12	DDR_B_DQS0
			13	VSS	VSS	14	
DDR_B_D2			15	DQ2	DQ6	16	DDR_B_D6
DDR_B_D3			17	DQ3	DQ7	18	DDR_B_D7
			19	VSS	VSS	20	
DDR_B_D8			21	DQ8	DQ12	22	DDR_B_D12
DDR_B_D9			23	DQ9	DQ13	24	DDR_B_D13
			25	VSS	VSS	26	
DDR_B_DQS#1			27	DQS1#	DM1	28	
DDR_B_DQS1			29	DQS1	RESET#	30	DDR3_DRAMRST#_R
			31	VSS	VSS	32	DDR3_DRAMRST#_R <12>
DDR_B_D10			33	DQ10	DQ14	34	DDR_B_D14
DDR_B_D11			35	DQ11	DQ15	36	DDR_B_D15
			37	VSS	VSS	38	
DDR_B_D16			39	DQ16	DQ20	40	DDR_B_D20
DDR_B_D17			41	DQ17	DQ21	42	DDR_B_D21
			43	VSS	VSS	44	
DDR_B_DQS#2			45	DQS2#	DM2	46	
DDR_B_DQS2			47	DQS2	VSS	48	
			49	VSS	DQ22	50	DDR_B_D22
DDR_B_D18			51	DQ18	DQ23	52	DDR_B_D23
DDR_B_D19			53	DQ19	VSS	54	
			55	VSS	DQ28	56	DDR_B_D28
DDR_B_D24			57	DQ24	DQ29	58	DDR_B_D29
DDR_B_D25			59	DQ25	VSS	60	
			61	VSS	DQS3#	62	DDR_B_DQS#3
			63	DM3	DQS3	64	DDR_B_DQS3
			65	VSS	VSS	66	
DDR_B_D26			67	DQ26	DQ30	68	DDR_B_D30
DDR_B_D27			69	DQ27	DQ31	70	DDR_B_D31
			71	VSS	VSS	72	
DDR_CKE2_DIMMB	<8> DDR_CKE2_DIMMB		73	CKE0	CKE1	74	DDR_CKE3_DIMMB
			75	VDD	VDD	76	DDR_CKE3_DIMMB <8>
			77	NC	A15	78	DDR_B_MA15
DDR_B_BS2	<8> DDR_B_BS2		79	BA2	A14	80	DDR_B_MA14
			81	VDD	VDD	82	
DDR_B_MA12			83	A12/BC#	A11	84	DDR_B_MA11
DDR_B_MA9			85	A9	A7	86	DDR_B_MA7
			87	VDD	VDD	88	
DDR_B_MA8			89	A8	A6	90	DDR_B_MA6
DDR_B_MA5			91	A5	A4	92	DDR_B_MA4
			93	VDD	VDD	94	
DDR_B_MA3			95	A3	A2	96	DDR_B_MA2
DDR_B_MA1			97	A1	A0	98	DDR_B_MA0
			99	VDD	VDD	100	
M_CLK_DDR2	<8> M_CLK_DDR2		101	CK0	CK1	102	M_CLK_DDR3
M_CLK_DDR#2	<8> M_CLK_DDR#2		103	CK0#	CK1#	104	M_CLK_DDR#3 <8>
			105	VDD	VDD	106	M_CLK_DDR3 <8>
DDR_B_MA10			107	A10/AP	BA1	108	DDR_B_BS1
DDR_B_BS0	<8> DDR_B_BS0		109	BA0	RAS#	110	DDR_B_RAS#
			111	VDD	VDD	112	DDR_B_BS1 <8>
DDR_B_WE#	<8> DDR_B_WE#		113	WE#	S0#	114	DDR_CS2_DIMMB#
DDR_B_CAS#	<8> DDR_B_CAS#		115	CAS#	ODT0	116	M_ODT2
			117	VDD	VDD	118	DDR_B_RAS# <8>
DDR_B_MA13			119	A13	ODT1	120	M_ODT3
DDR_CS3_DIMMB#	<8> DDR_CS3_DIMMB#		121	S1#	NC	122	DDR_CS2_DIMMB# <8>
			123	VDD	VDD	124	M_ODT2 <8>
			125	TEST	VREF_CA	126	M_ODT3 <8>
			127	VSS	VSS	128	
DDR_B_D32			129	DQ32	DQ36	130	DDR_B_D36
DDR_B_D33			131	DQ33	DQ37	132	DDR_B_D37
			133	VSS	VSS	134	
DDR_B_DQS#4			135	DQS4#	DM4	136	
DDR_B_DQS4			137	DQS4	VSS	138	
			139	VSS	DQ38	140	DDR_B_D38
DDR_B_D34			141	DQ34	DQ39	142	DDR_B_D39
DDR_B_D35			143	DQ35	VSS	144	
			145	VSS	DQ44	146	DDR_B_D44
DDR_B_D40			147	DQ40	DQ45	148	DDR_B_D45
DDR_B_D41			149	DQ41	VSS	150	
			151	VSS	DQS5#	152	DDR_B_DQS#5
			153	DM5	DQS5	154	DDR_B_DQS5
			155	VSS	VSS	156	
DDR_B_D42			157	DQ42	DQ46	158	DDR_B_D46
DDR_B_D43			159	DQ43	DQ47	160	DDR_B_D47
			161	VSS	VSS	162	
DDR_B_D48			163	DQ48	DQ52	164	DDR_B_D52
DDR_B_D49			165	DQ49	DQ53	166	DDR_B_D53
			167	VSS	VSS	168	
DDR_B_DQS#6			169	DQS6#	DM6	170	
DDR_B_DQS6			171	DQS6	VSS	172	
			173	VSS	DQ54	174	DDR_B_D54
DDR_B_D50			175	DQ50	DQ55	176	DDR_B_D55
DDR_B_D51			177	DQ51	VSS	178	
			179	VSS	DQ60	180	DDR_B_D60
DDR_B_D56			181	DQ56	DQ61	182	DDR_B_D61
DDR_B_D57			183	DQ57	VSS	184	
			185	VSS	DQS7#	186	DDR_B_DQS#7
			187	DM7	DQS7	188	DDR_B_DQS7
			189	VSS	VSS	190	
DDR_B_D58			191	DQ58	DQ62	192	DDR_B_D62
DDR_B_D59			193	DQ59	DQ63	194	DDR_B_D63
			195	VSS	VSS	196	
			197	SA0	EVENT#	198	
		+3.3V_RUN	199	VDDSPD	SDA	200	DDR_XDP_WAN_SMBDAT <12,15,27,34>
			201	SA1	SCL	202	DDR_XDP_WAN_SMBCLK <12,15,27,34>
		+0.75V_DDR_VTT	203	VTT	VTT	204	+0.75V_DDR_VTT
			205	GND1	GND1	206	

+3.3V_RUN — RD5 10K_0402_5%~D — +3.3V_RUN
+0.75V_DDR_VTT — RD6 10K_0402_5%~D; CD43 1U_0402_25V6K~D; CD44 2.2U_0402_6.3V6M

+DIMM2_VREF_CA — CD37 2.2U_0402_6.3V6M; CD38 0.1U_0402_25V6K~D
+DIMM2_VREF_CA — @RD15 0_0402_5%~D — +V_DDR_REF

+1.5V_MEM — CD25 1U_0402_6.3V6K~D; CD26 1U_0402_6.3V6K~D; CD27 1U_0402_6.3V6K~D; CD28 1U_0402_6.3V6K~D
+1.5V_MEM — CD29 10U_0603_6.3V6M~D; CD30 10U_0603_6.3V6M~D; CD31 10U_0603_6.3V6M~D; CD32 10U_0603_6.3V6M~D; CD33 10U_0603_6.3V6M~D; CD34 10U_0603_6.3V6M~D; @CD35 10U_0603_6.3V6M~D; CD36 330U_SX_2V~D
+0.75V_DDR_VTT — CD39 1U_0402_6.3V6K~D; CD40 1U_0402_6.3V6K~D; CD41 1U_0402_6.3V6K~D; CD42 1U_0402_6.3V6K~D

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CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

PCH_AZ_SYNC is sampled at the rising edge of RSMRST# pin. So signal should be PU to the ALWAYS rail.

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs
Low - Enable External VRs

On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low

CH6 close to JXDP2

CH1 close to JXDP2

INTEL HDA_SYNC isolation circuit

CMOS place near DIMM

UH4A

BD82PPSM-ONHN-A0_BGA989~D

HDD

ODD/ E Module Bay

E-SATA

DOCK

No Reboot Strap
SPKR: Low = Default; High = No Reboot

BBS_BIT0 - BIOS BOOT STRAP BIT 0

200 MIL SO8
64Mb Flash ROM
W25Q64CVSSIG_SO8~D

200 MIL SO8
32Mb Flash ROM
W25Q32BVSSIG_SO8~D

R895 colay R940 R897 colay R942 R900 colay R941 for TAA config

RF team request

Link Done

TYCO_5-1775013-4~D

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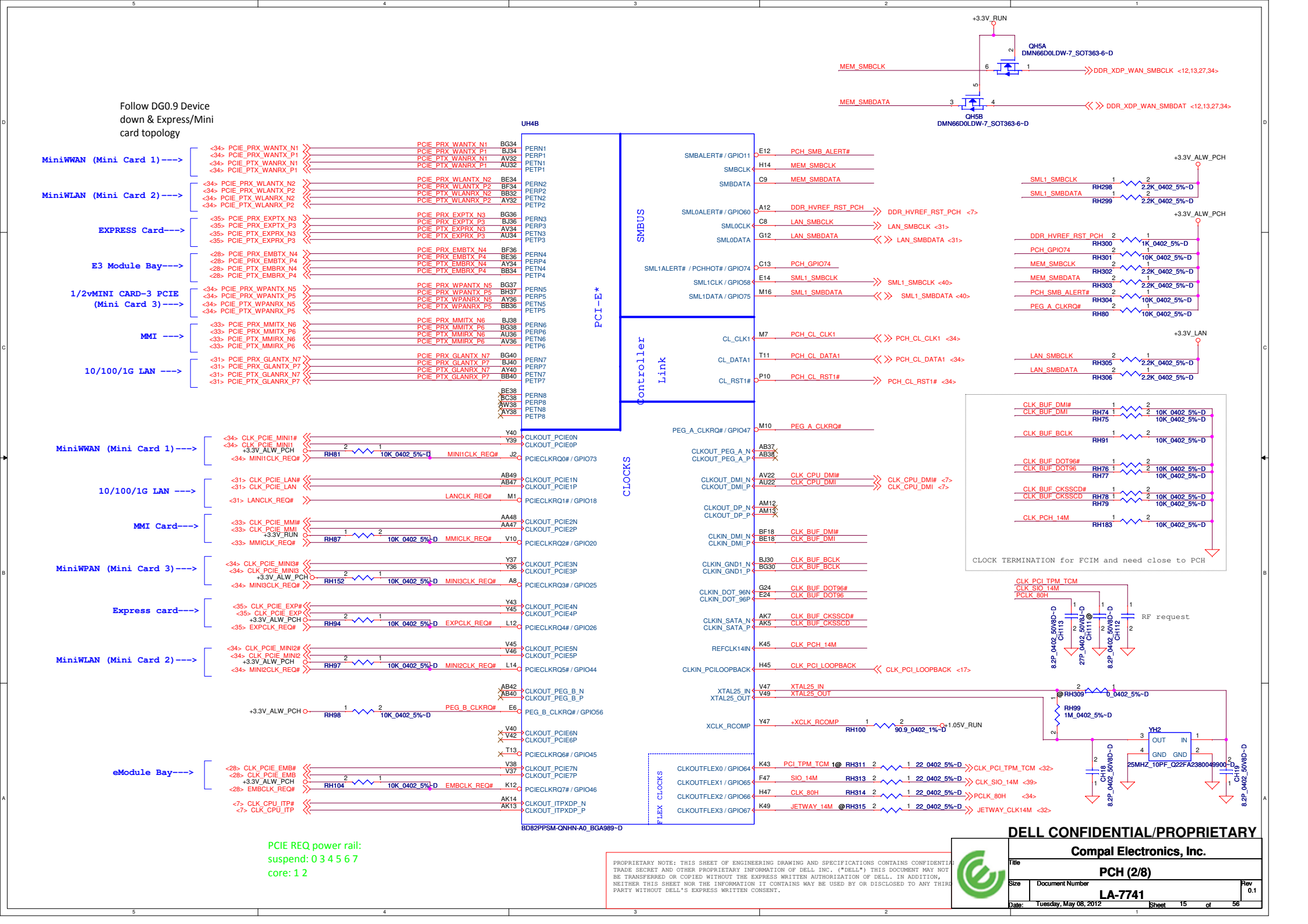

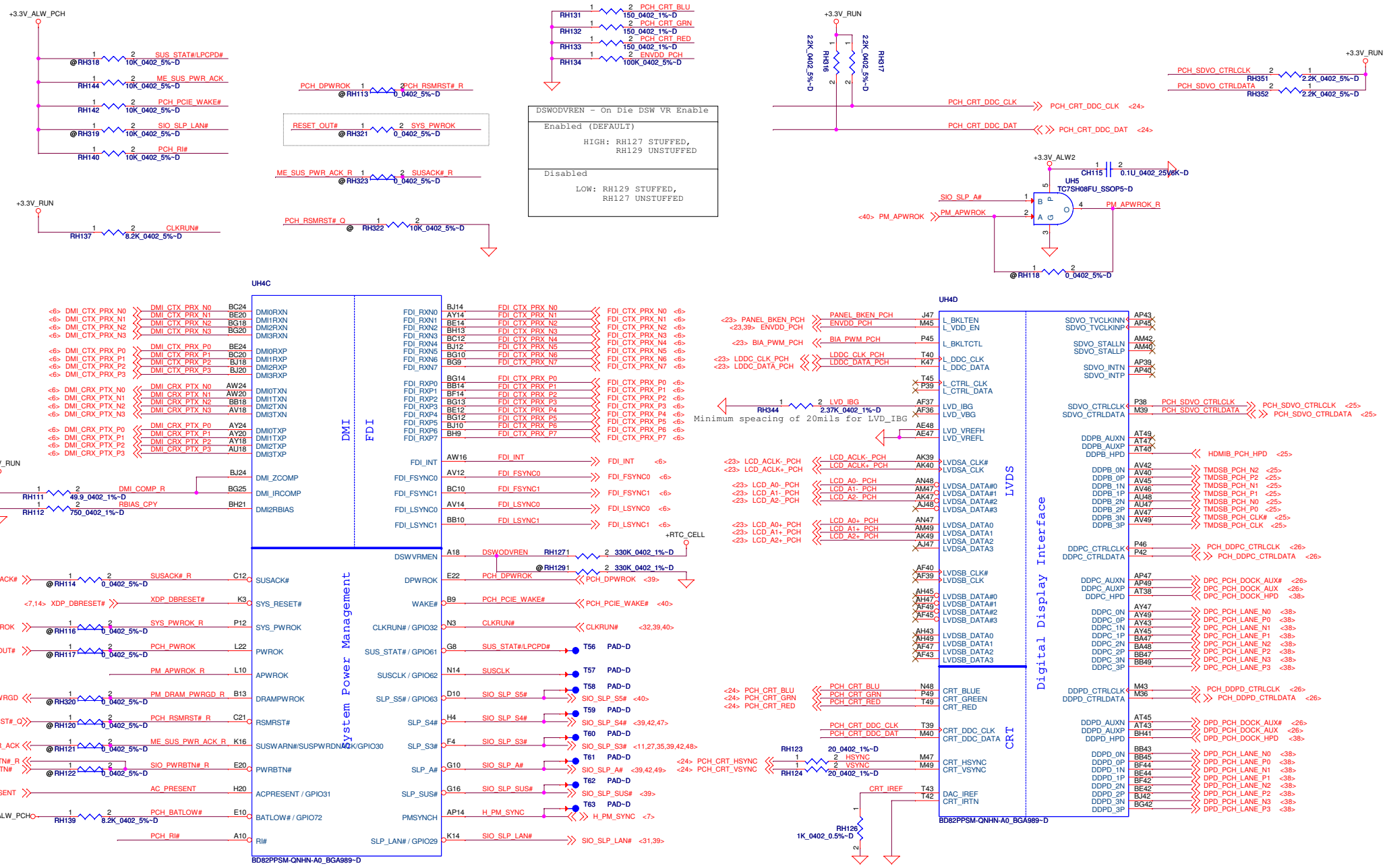

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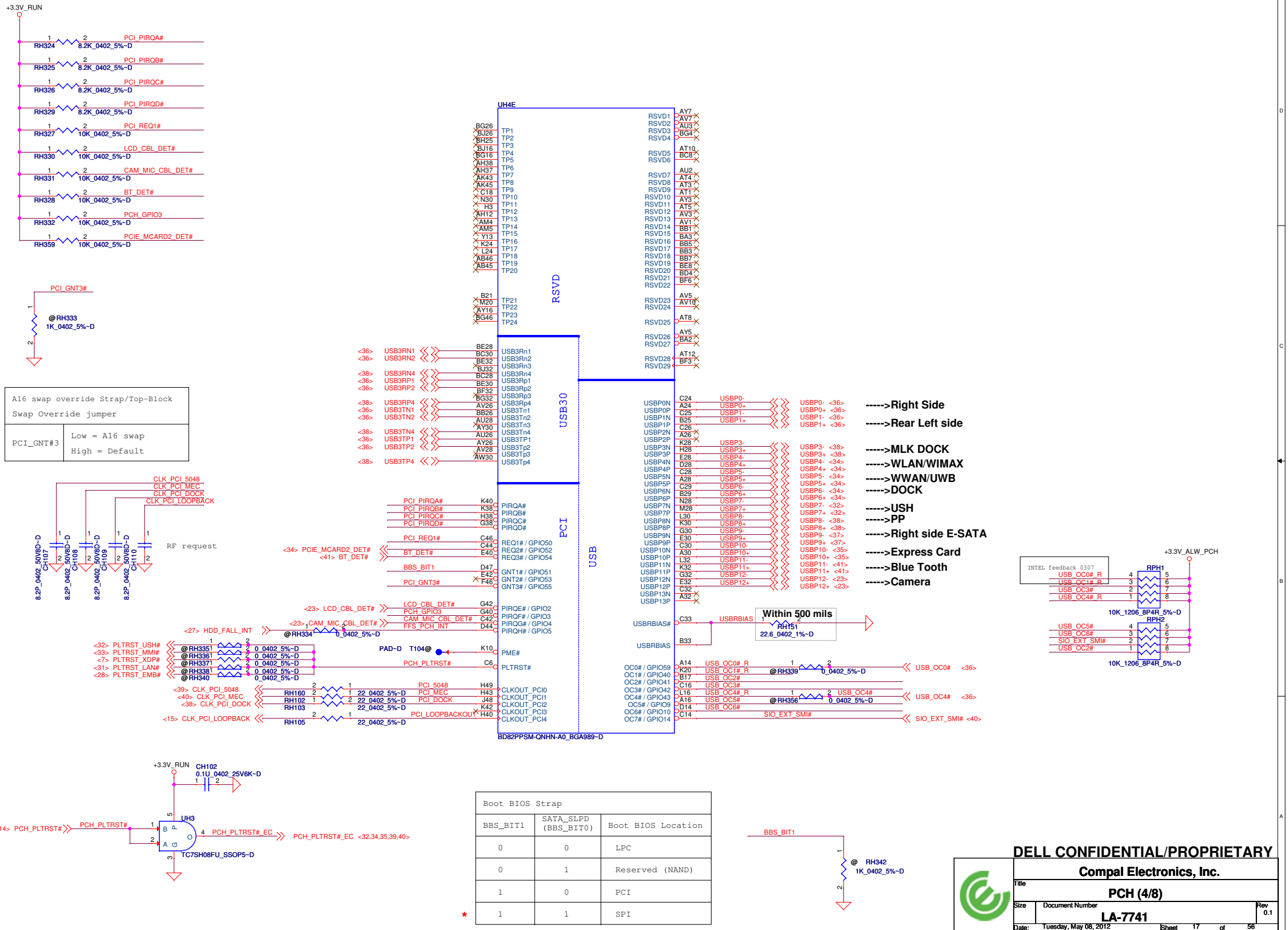
+3.3V_RUN
RH324 8.2K_0402_5%~D PCI_PIRQA#
RH325 8.2K_0402_5%~D PCI_PIRQB#
RH326 8.2K_0402_5%~D PCI_PIRQC#
RH329 8.2K_0402_5%~D PCI_PIRQD#
RH327 10K_0402_5%~D PCI_REQ1#
RH330 10K_0402_5%~D LCD_CBL_DET#
RH331 10K_0402_5%~D CAM_MIC_CBL_DET#
RH328 10K_0402_5%~D BT_DET#
RH332 10K_0402_5%~D PCH_GPIO3
RH359 10K_0402_5%~D PCIE_MCARD2_DET#
PCI_GNT3#
@RH333 1K_0402_5%~D
A16 swap override Strap/Top-Block
Swap Override jumper
PCI_GNT3# Low = A16 swap
High = Default
UH4E
RSVD
USB30
PCI
USB
BD82PPSM-QNHN-A0_BGA989~D
USB3Rn1 USB3Rn2 USB3Rn3 USB3Rn4 USB3Rp1 USB3Rp2 USB3Rp3 USB3Rp4 USB3Tn1 USB3Tn2 USB3Tn3 USB3Tn4 USB3TP1 USB3Tp2 USB3Tp3 USB3Tp4
USBP0- USBP0+ USBP1- USBP1+ USBP2- USBP2+ USBP3- USBP3+ USBP4- USBP4+ USBP5- USBP5+ USBP6- USBP6+ USBP7- USBP7+ USBP8- USBP8+ USBP9- USBP9+ USBP10- USBP10+ USBP11- USBP11+ USBP12- USBP12+
PIRQA# PIRQB# PIRQC# PIRQD#
REQ1# / GPIO50 REQ2# / GPIO52 REQ3# / GPIO54
GNT1# / GPIO51 GNT2# / GPIO53 GNT3# / GPIO55
PIRQE# / GPIO2 PIRQF# / GPIO3 PIRQG# / GPIO4 PIRQH# / GPIO5
PME# PLTRST#
OC0# / GPIO59 OC1# / GPIO40 OC2# / GPIO41 OC3# / GPIO42 OC4# / GPIO43 OC5# / GPIO9 OC6# / GPIO10 OC7# / GPIO14
CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4
USBRBIAS
----->Right Side
----->Rear Left side
----->MLK DOCK
----->WLAN/WIMAX
----->WWAN/UWB
----->DOCK
----->USH
----->PP
----->Right side E-SATA
----->Express Card
----->Blue Tooth
----->Camera
Within 500 mils
RH151 22.6_0402_1%~D
CLK_PCI_5048 CLK_PCI_MEC CLK_PCI_DOCK CLK_PCI_LOOPBACK
RF request
CH107 CH108 CH109 CH110 8.2P_0402_50V8D~D
PCI_REQ1# BT_DET# BBS_BIT1 PCI_GNT3#
LCD_CBL_DET# PCH_GPIO3 CAM_MIC_CBL_DET# FFS_PCH_INT
HDD_FALL_INT
PLTRST_USH# PLTRST_MMI# PLTRST_XDP# PLTRST_LAN# PLTRST_EMB#
@RH3351 @RH3361 @RH3371 @RH3381 @RH340 0_0402_5%~D
PAD~D T104@
PCH_PLTRST#
PCI_5048 PCI_MEC PCI_DOCK PCI_LOOPBACKOUT
RH160 RH102 RH103 RH105 22_0402_5%~D
CLK_PCI_5048 CLK_PCI_MEC CLK_PCI_DOCK CLK_PCI_LOOPBACK
@RH339 @RH356 0_0402_5%~D
USB_OC0# USB_OC1# USB_OC2# USB_OC3# USB_OC4# USB_OC5# USB_OC6#
SIO_EXT_SMI#
INTEL feedback 0307
RPH1 RPH2 10K_1206_8P4R_5%~D
+3.3V_ALW_PCH
+3.3V_RUN
CH102 0.1U_0402_25V6K~D
UH3 TC7SH08FU_SSOP5~D
<7,14> PCH_PLTRST#
PCH_PLTRST#_EC
PCH_PLTRST#_EC <32,34,35,39,40>
Boot BIOS Strap
BBS_BIT1 | SATA_SLPD (BBS_BIT0) | Boot BIOS Location
0 | 0 | LPC
0 | 1 | Reserved (NAND)
1 | 0 | PCI
1 | 1 | SPI
BBS_BIT1
@ RH342 1K_0402_5%~D
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+3.3V_ALW_PCH

RH53 4.7K_0402_5%~D

SLP_ME_CSW_DEV#

@ RH353 1K_0402_5%~D

Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

SLP_ME_CSW_DEV#	PLL ON DIE VR ENABLE
ENABLED - HIGH DEFAULT DISABLED - LOW	

+3.3V_ALW_PCH

RH177 2 1 SIO_EXT_WAKE# 10K_0402_5%~D

RH354 1 2 PCH_GPIO15 1K_0402_5%~D

RH174 2 1 PCH_GPIO36 10K_0402_5%~D

RH172 2 1 PCH_GPIO37 10K_0402_5%~D

@RH273 2 1 PCH_GPIO17 1K_0402_5%~D

@RH265 2 1 PCH_GPIO16 10K_0402_5%~D

+3.3V_ALW_PCH

RH170 2 1 KB_DET# 10K_0402_5%~D

+3.3V_RUN

@RH171 2 1 PCH_GPIO36 10K_0402_5%~D

@RH173 2 1 PCH_GPIO37 1K_0402_5%~D

RH272 1 2 PCH_GPIO16 10K_0402_5%~D

RH266 2 1 TEMP_ALERT# 10K_0402_5%~D

RH181 2 1 MEDIA_DET# 10K_0402_5%~D

RH178 1 2 PCH_GPIO7 10K_0402_5%~D

RH269 1 2 PCH_GPIO17 8.2K_0402_5%~D

RH163 1 2 IO_LOOP# 10K_0402_5%~D

UH4F

<40> SIO_EXT_SCI# — SIO_EXT_SCI# 1 @RH259 2 SIO_EXT_SCI# R 0_0402_5%~D — T7 BMBUSY# / GPIO0

<32> USH_DET# — USH_DET# — A42 TACH1 / GPIO1

<30> IO_LOOP# — IO_LOOP# — H36 TACH2 / GPIO6

PCH_GPIO7 — E38 TACH3 / GPIO7

<39> SIO_EXT_WAKE# — C10 GPIO8

<31> PM_LANPHY_ENABLE — PM_LANPHY_ENABLE — C4 LAN_PHY_PWR_CTRL / GPIO12

PCH_GPIO15 — G2 GPIO15

PCH_GPIO16 — U2 SATA4GP / GPIO16

PCH_GPIO17 — D40 TACH0 / GPIO17

<30> MEDIA_DET# — MEDIA_DET# — T5 SCLOCK / GPIO22

<34> PCIE_MCARD1_DET# — E8 GPIO24

<35> EXPRCRD_DET# — EXPRCRD_DET# — E16 GPIO27

<39> SLP_ME_CSW_DEV# — SLP_ME_CSW_DEV# — P8 GPIO28

K1 STP_PCI# / GPIO34

<34> USB_MCARD1_DET# — USB_MCARD1_DET# — K4 GPIO35

PCH_GPIO36 — V8 SATA2GP / GPIO36

PCH_GPIO37 — M5 SATA3GP / GPIO37

TPM_ID0 — N2 SLOAD / GPIO38

TPM_ID1 — M3 SDATAOUT0 / GPIO39

<27> FFS_INT2 — FFS_INT2 — V13 SDATAOUT1 / GPIO48

<39> TEMP_ALERT# — TEMP_ALERT# — V3 SATA5GP / GPIO49 / TEMP_ALERT#

<41> KB_DET# — KB_DET# — D6 GPIO57

GPIO

TACH4 / GPIO68 C40 CONTACTLESS_DET# <CONTACTLESS_DET# <32>

TACH5 / GPIO69 B41 PCH_GPIO69

TACH6 / GPIO70 C41 PCIE_MCARD3_DET# <PCIE_MCARD3_DET# <34>

TACH7 / GPIO71 A40 <USB_MCARD2_DET# <34>

A20GATE P4 SIO_A20GATE <SIO_A20GATE <40>

PECI AU16

RCIN# P5 SIO_RCIN# <SIO_RCIN# <40>

PROCPWRGD AY11 H_CPUPWRGD >H_CPUPWRGD <7>

THRMTRIP# AY10 PCH_THRMTRIP# R

INIT3_3V# T14 INIT3_3V# PAD~D T106 @

DF_TVS AY1 DF_TVS

CPU/MISC

TS_VSS1 AH8

TS_VSS2 AK11

TS_VSS3 AH10

TS_VSS4 AK10

NC_1 P37 NC_1 PAD~D T108 @

+1.05V_RUN_VTT

RH262 2 1 56_0402_5%~D

CH97 1 2 0.1U_0402_25V6K~D

+3.3V_RUN

CONTACTLESS_DET# RH256 2 1 10K_0402_5%~D

PCH_GPIO69 RH260 1 2 1.5K_0402_1%~D

+3.3V_RUN

SIO_A20GATE RH158 2 1 10K_0402_5%~D

SIO_RCIN# RH203 2 1 10K_0402_5%~D

SIO_EXT_SCI# RH263 1 2 10K_0402_5%~D

USH_DET# RH164 1 2 100K_0402_5%~D

EXPRCRD_DET# RH264 1 2 10K_0402_5%~D

VSS_NCTF_1 A4 — VSS_NCTF_1 — VSS_NCTF_1 BG2 VSS_NCTF_15

VSS_NCTF_2 A44 — VSS_NCTF_2 — VSS_NCTF_2 BG48 VSS_NCTF_16

VSS_NCTF_3 A45 — VSS_NCTF_3 — VSS_NCTF_3 BH3 VSS_NCTF_17

VSS_NCTF_4 A46 — VSS_NCTF_4 — VSS_NCTF_4 BH47 VSS_NCTF_18

VSS_NCTF_5 A5 — VSS_NCTF_5 — VSS_NCTF_5 BJ4 VSS_NCTF_19

VSS_NCTF_6 A6 — VSS_NCTF_6 — VSS_NCTF_6 BJ44 VSS_NCTF_20

VSS_NCTF_7 B3 — VSS_NCTF_7 — VSS_NCTF_7 BJ45 VSS_NCTF_21

VSS_NCTF_8 B47 — VSS_NCTF_8 — VSS_NCTF_8 BJ46 VSS_NCTF_22

VSS_NCTF_9 BD1 — VSS_NCTF_9 — VSS_NCTF_9 BJ5 VSS_NCTF_23

VSS_NCTF_10 BD49 — VSS_NCTF_10 — VSS_NCTF_10 BJ6 VSS_NCTF_24

VSS_NCTF_11 BE1 — VSS_NCTF_11 — VSS_NCTF_11 C2 VSS_NCTF_25

VSS_NCTF_12 BE49 — VSS_NCTF_12 — VSS_NCTF_12 C48 VSS_NCTF_26

VSS_NCTF_13 BF1 — VSS_NCTF_13 — VSS_NCTF_13 D1 VSS_NCTF_27

VSS_NCTF_14 BF49 — VSS_NCTF_14 — VSS_NCTF_14 D49 VSS_NCTF_28

NCTF

VSS_NCTF_15 BG2 VSS_NCTF_15

VSS_NCTF_16 BG48 VSS_NCTF_16

VSS_NCTF_17 BH3 VSS_NCTF_17

VSS_NCTF_18 BH47 VSS_NCTF_18

VSS_NCTF_19 BJ4 VSS_NCTF_19

VSS_NCTF_20 BJ44 VSS_NCTF_20

VSS_NCTF_21 BJ45 VSS_NCTF_21

VSS_NCTF_22 BJ46 VSS_NCTF_22

VSS_NCTF_23 BJ5 VSS_NCTF_23

VSS_NCTF_24 BJ6 VSS_NCTF_24

VSS_NCTF_25 C2 VSS_NCTF_25

VSS_NCTF_26 C48 VSS_NCTF_26

VSS_NCTF_27 D1 VSS_NCTF_27

VSS_NCTF_28 D49 VSS_NCTF_28

VSS_NCTF_29 E1 VSS_NCTF_29

VSS_NCTF_30 E49 VSS_NCTF_30

VSS_NCTF_31 F1 VSS_NCTF_31

VSS_NCTF_32 F49 VSS_NCTF_32

BD82PPSM-QNHN-A0_BGA989~D

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45°from the pad.

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45°from the pad.

PLACE RH150 CLOSE TO THE BRANCHING POINT (TO CPU and NVRAM CONNECTOR)

+VCCDFTERM

RH149 need to close to CPU

RH149 2.2K_0402_5%~D

<7> H_SNB_IVB# — @RH150 1 2 0_0402_5%~D — DF_TVS_R 1 RH358 2 1K_0402_5%~D — DF_TVS

DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

+3.3V_RUN

1@ RH267 10K_0402_5%~D

2@ RH270 10K_0402_5%~D

TPM_ID0

+3.3V_RUN

RH268 20K_0402_5%~D

@ RH271 2.2K_0402_5%~D

TPM_ID1

	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
USH1.0 (For SSI)	1	0
USH2.0	1	1

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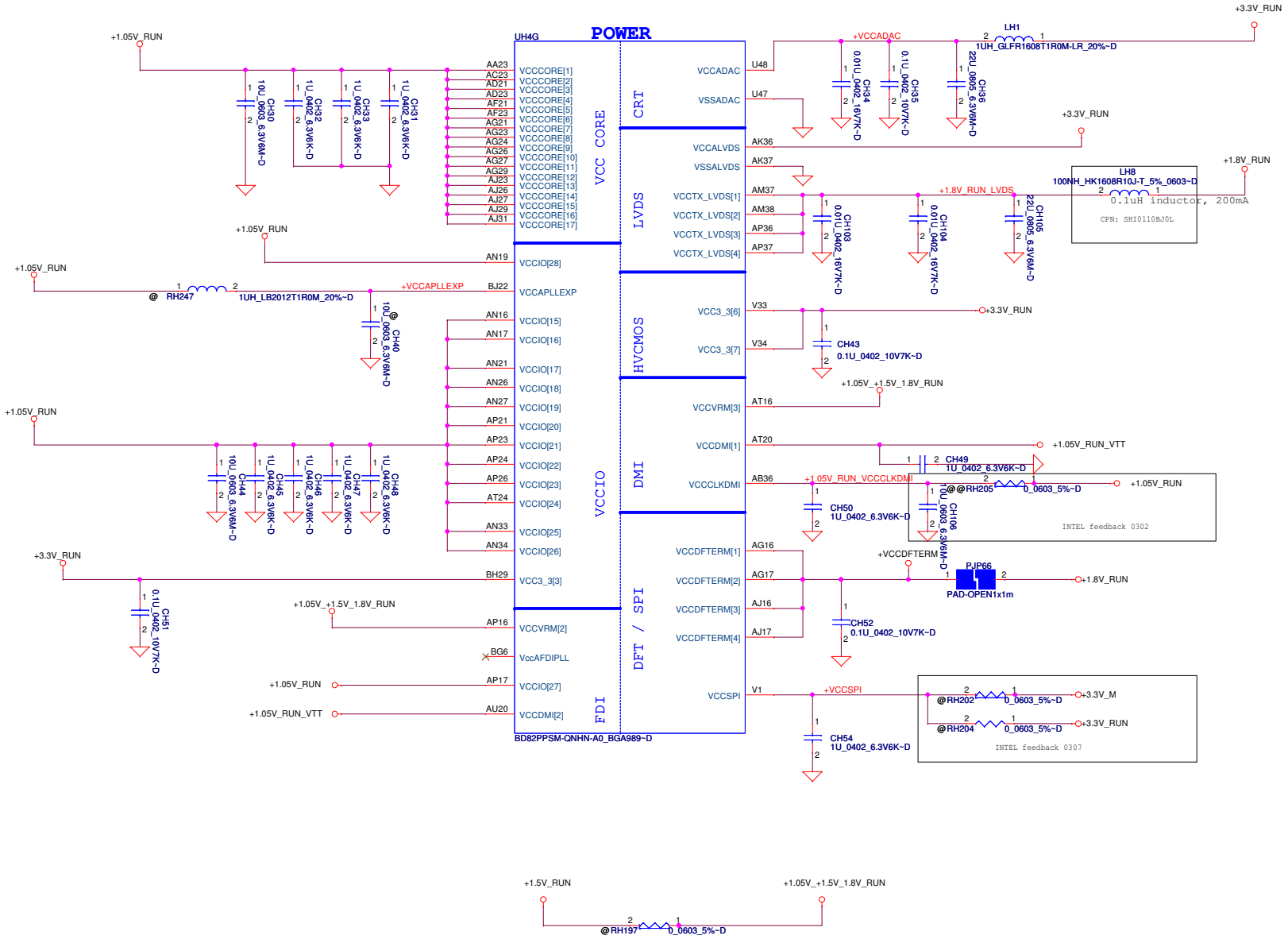


PCH Power Rail Table

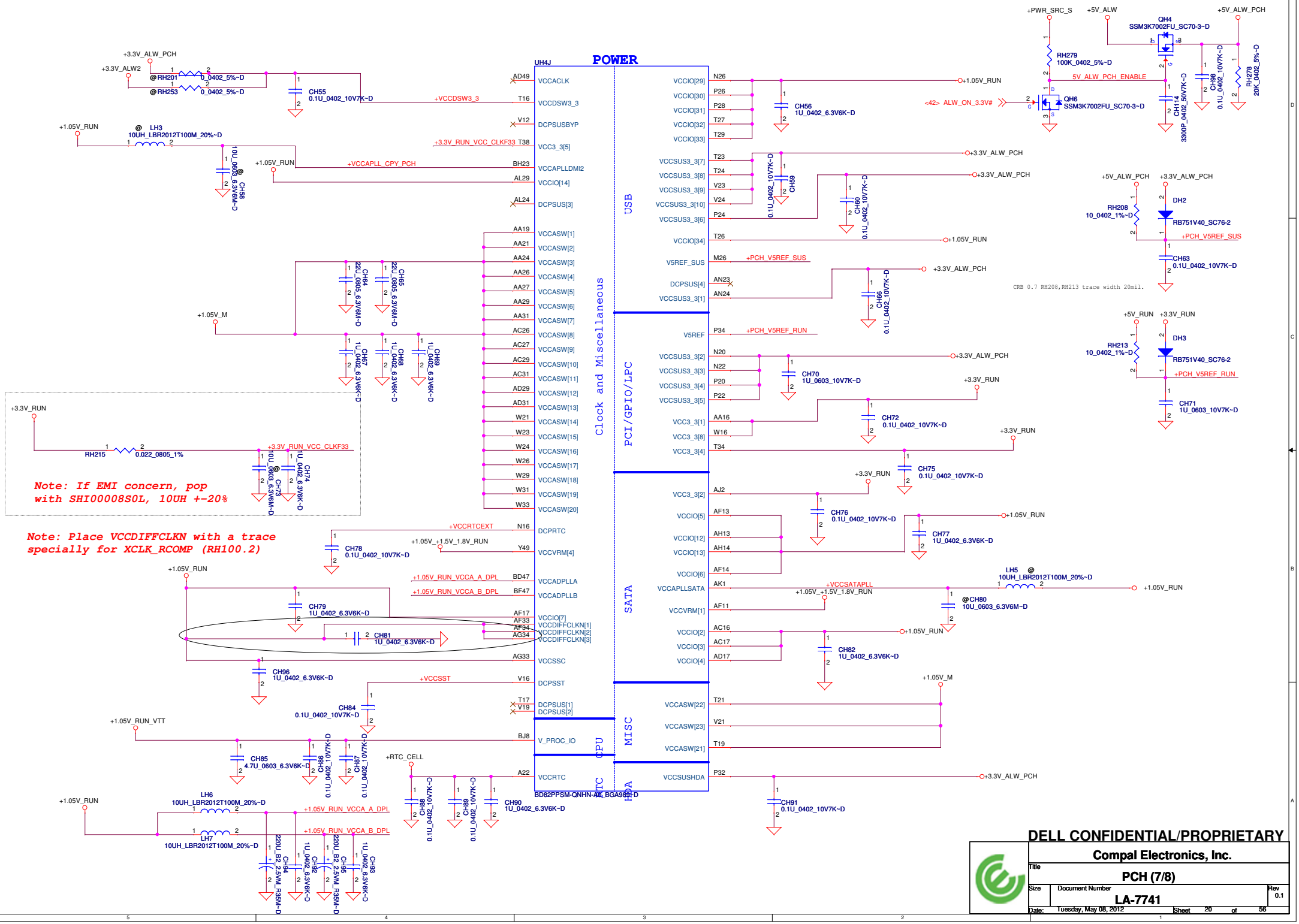
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC3	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VCCDFTERM	1.8	0.002
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Compal Electronics, Inc.

Title: PCH (6/8)

Size | Document Number: LA-7741 | Rev: 0.1

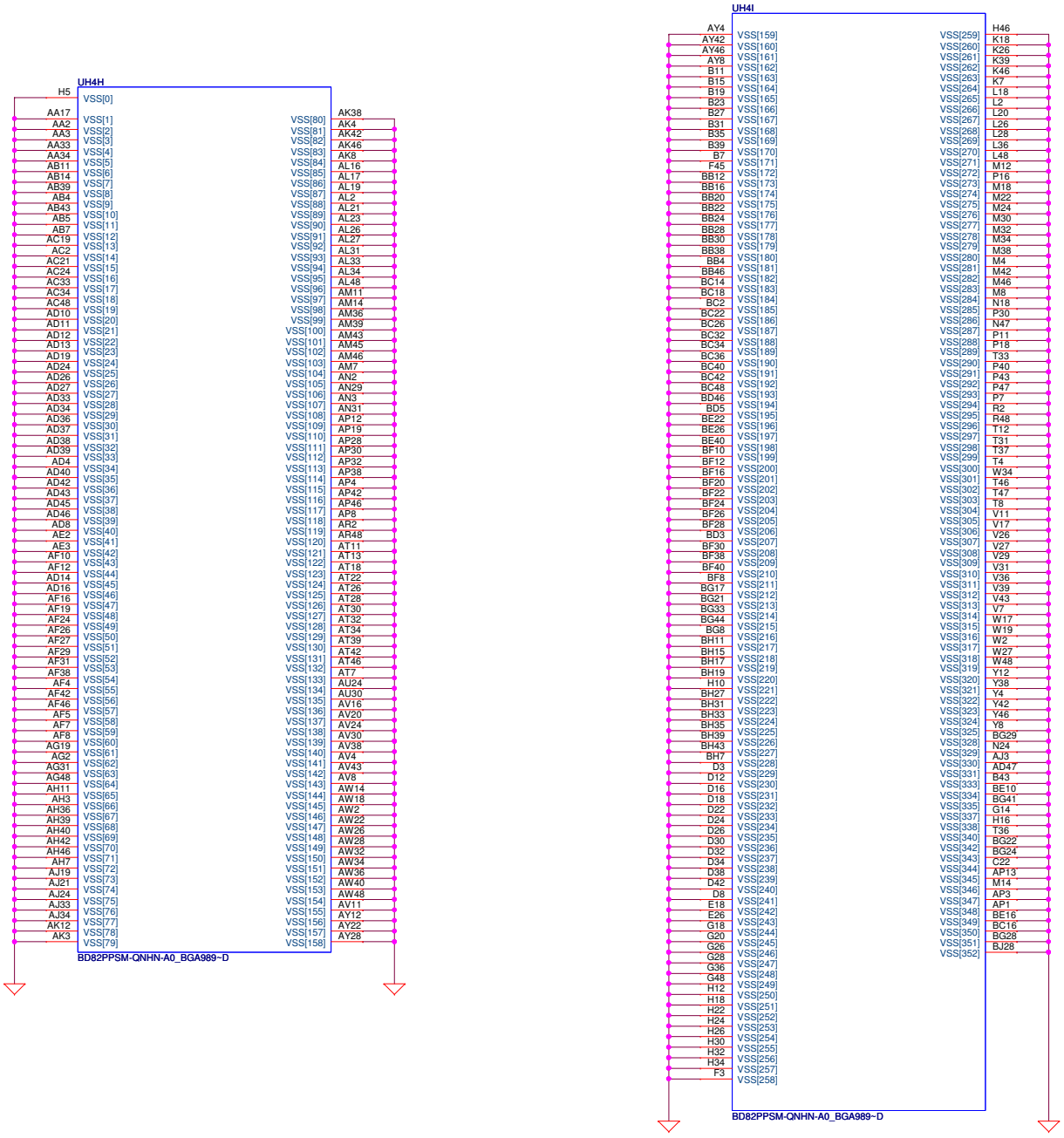
Date: Tuesday, May 08, 2012 | Sheet 19 of 56



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	PCH (7/8)	
Size	Document Number: LA-7741	Rev: 0.1
Date: Tuesday, May 08, 2012	Sheet 20 of 56	



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	PCH (8/8)	
Size	Document Number: LA-7741	Rev: 0.1
Date: Tuesday, May 08, 2012	Sheet 21 of 56	

Place under CPU
Place C266 close to the Q12 as possible

(1) DP3/DN3 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
(2) DP5/DN5 for Skin on Q13, place Q13 close to Vcore VR choke.

Link Done

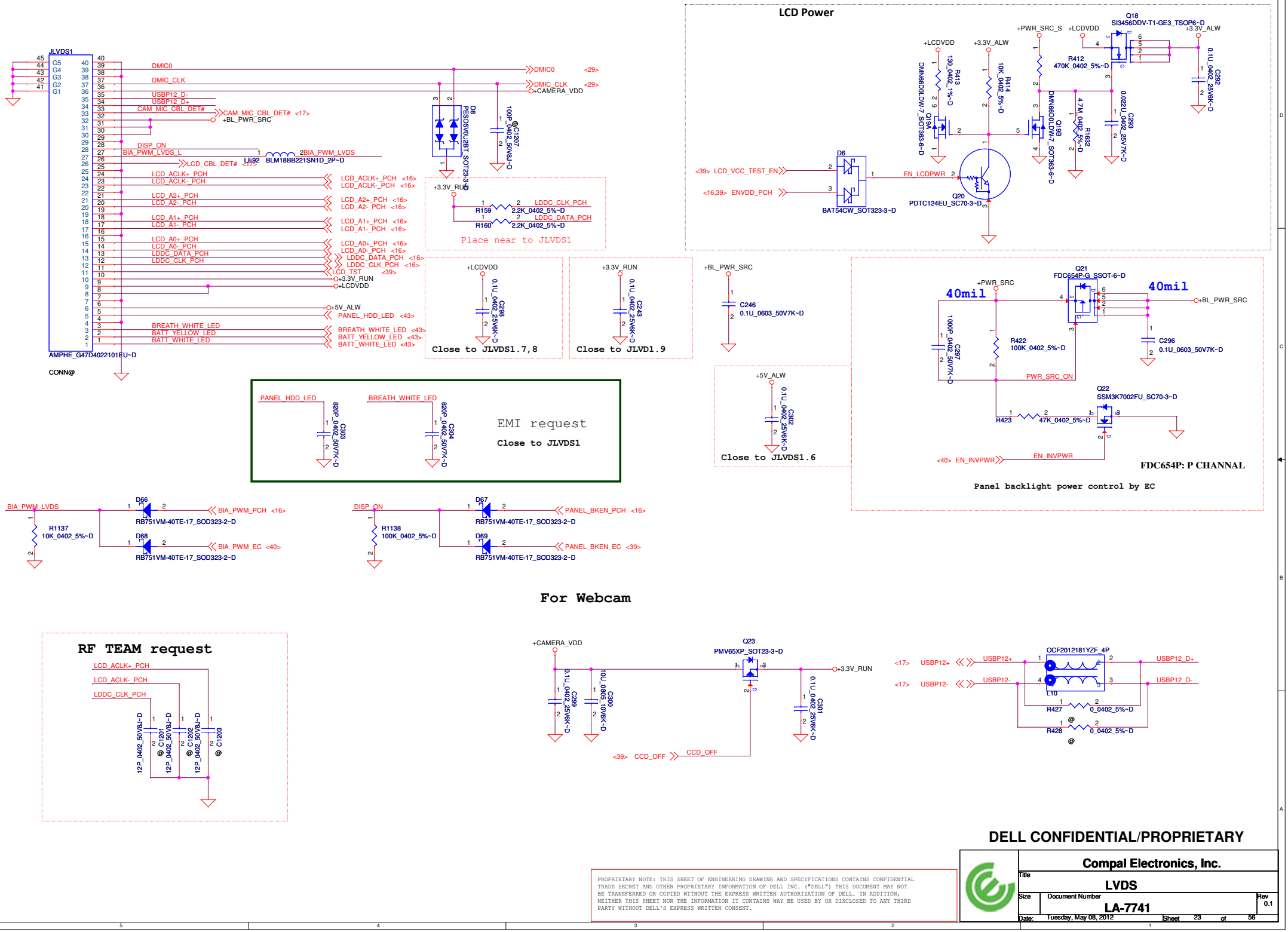
Rest=1400 Tp=94degree For SNB
Rest=1580 Tp=96degree For IVB

Compal Electronics, Inc.

Title: FAN & Thermal Sensor

Size: | Document Number: LA-7741 | Rev: 0.1

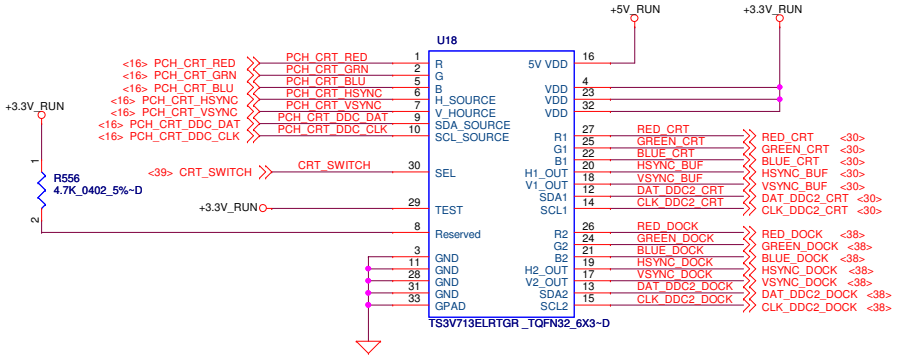
Date: Tuesday, May 08, 2012 | Sheet 22 of 56



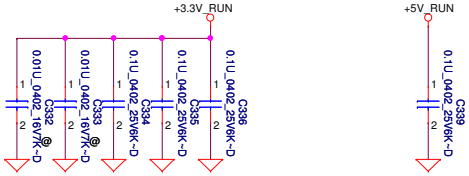
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: LVDS		
Size	Document Number: LA-7741	Rev: 0.1
Date: Tuesday, May 08, 2012	Sheet 23 of 56	

SW for MB/DOCK



SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR

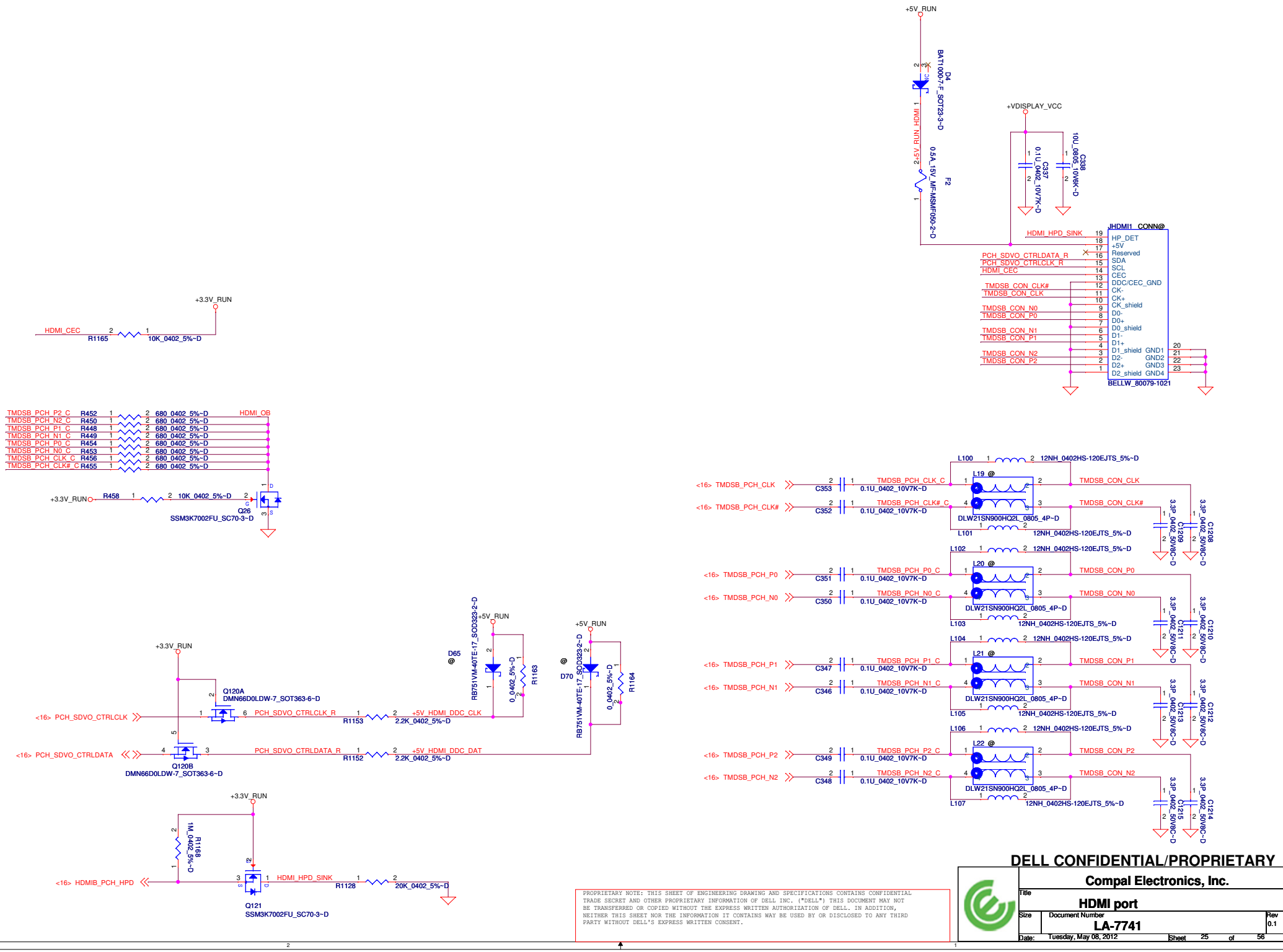


Compal Electronics, Inc.

Title: CRT/Video switch

Size | Document Number: LA-7741 | Rev: 0.1

Date: Tuesday, May 08, 2012 | Sheet 24 of 56



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Compal Electronics, Inc.

Title: HDMI port

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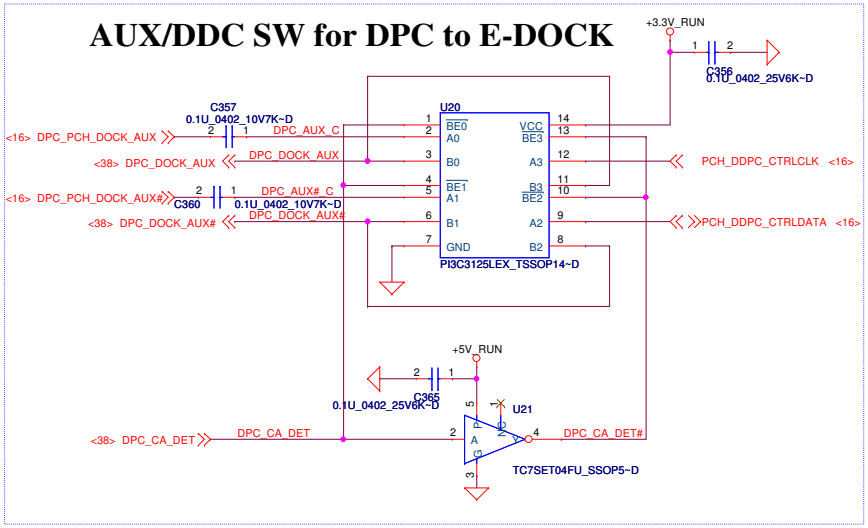
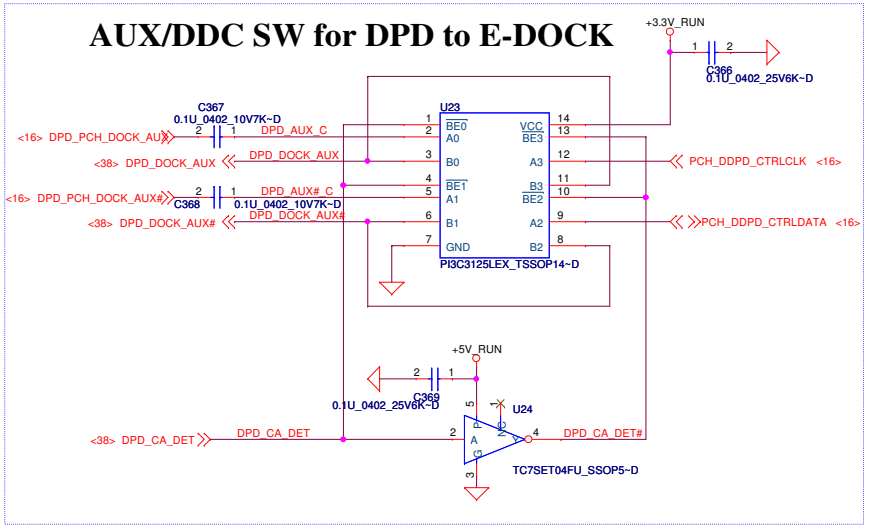
Date: Tuesday, May 08, 2012 | Sheet 25 of 56

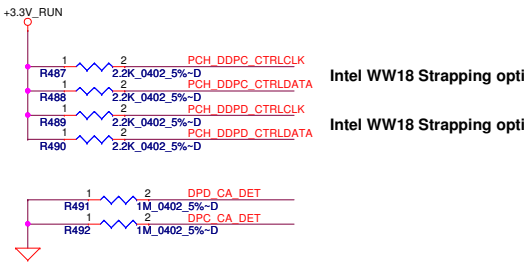
AUX/DDC SW for DPC to E-DOCK



There is a new die for PI3C3125. Sample availabe on May.

AUX/DDC SW for DPD to E-DOCK





Intel WW18 Strapping option

Intel WW18 Strapping option

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	DP125
Size	Document Number: LA-7741
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Date:	Tuesday, May 08, 2012
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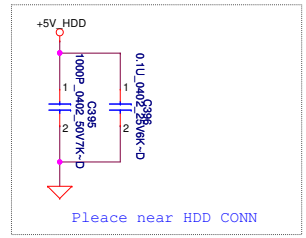
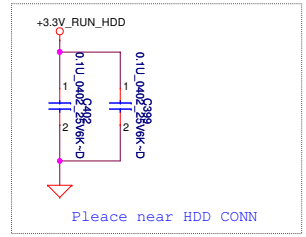
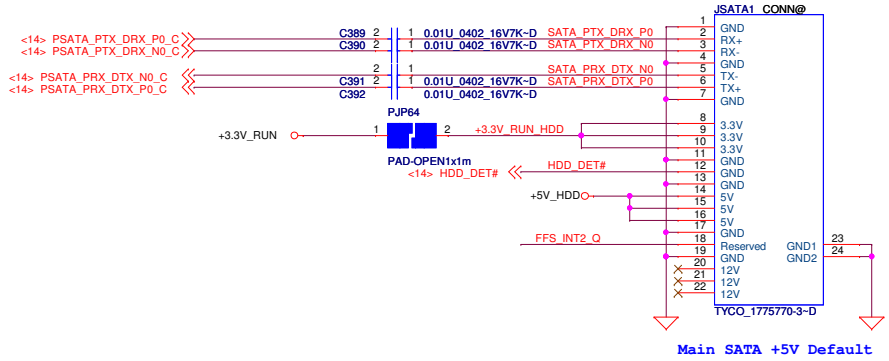


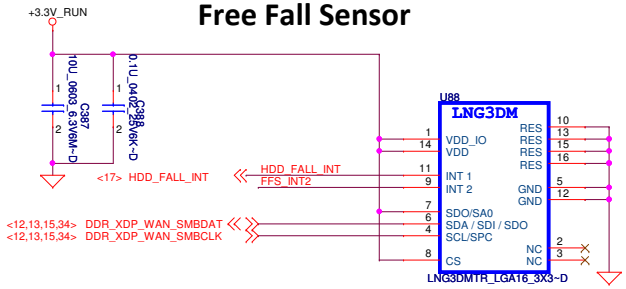


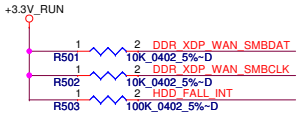
For HDD Temp.

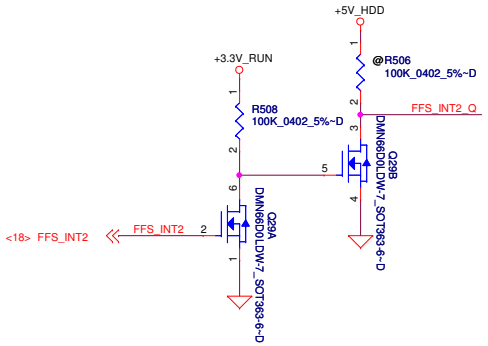


Main SATA +5V Default

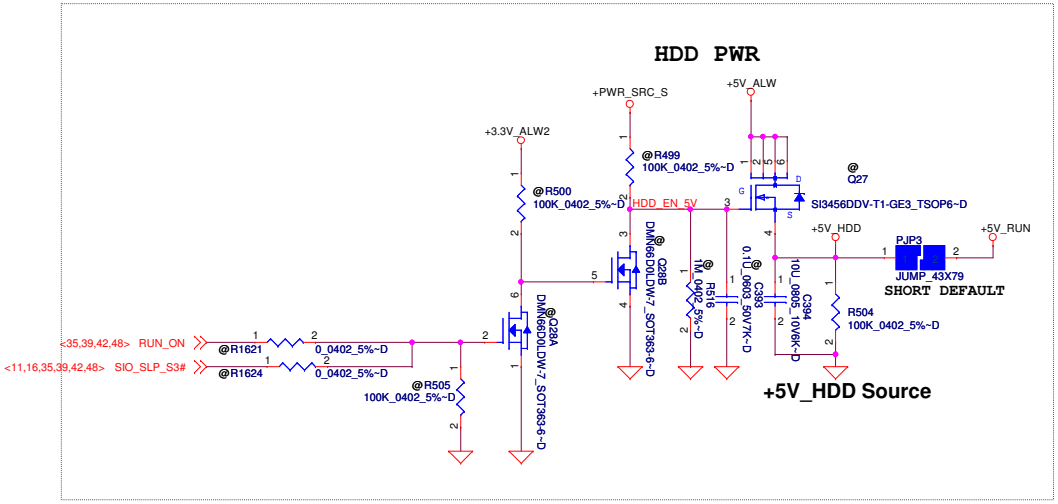
Free Fall Sensor







HDD PWR



+5V_HDD Source

DELL CONFIDENTIAL/PROPRIETARY

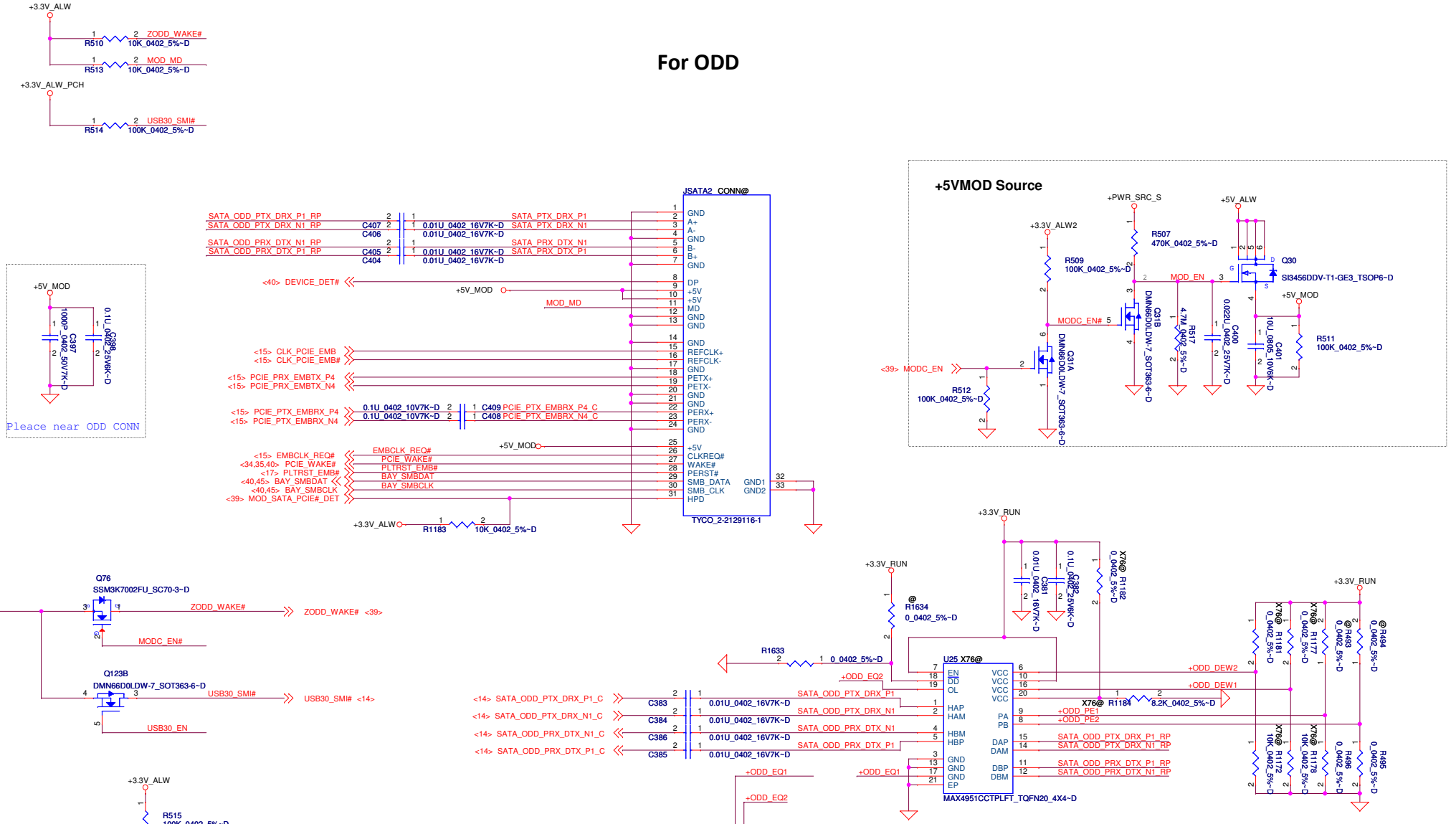
Compal Electronics, Inc.

Title: HDD CONNECTOR

Size | Document Number: LA-7741 | Rev: 0.1

Date: Tuesday, May 08, 2012 | Sheet 27 of 56

For ODD



	PIN6	PIN16	PIN9	PIN8	PIN17	PIN19	PIN20	PIN18
Parade PS8520B(Internal PD)	PH	PH	PD	PD	PD	PD	PD	PD
MAXIM MAX4951C(Internal PD)	PH	PH	PD	PD	PD	PD	VCC	PD
Pericom PI3EQX6741ST (Tri-level)	NC	NC	PD	PD	PD	PD	VCC	PH
TI SN75LVCP601 (Internally tied to Vcc/2)	PD	PD	PD	PD	PD	PD	VCC	PD

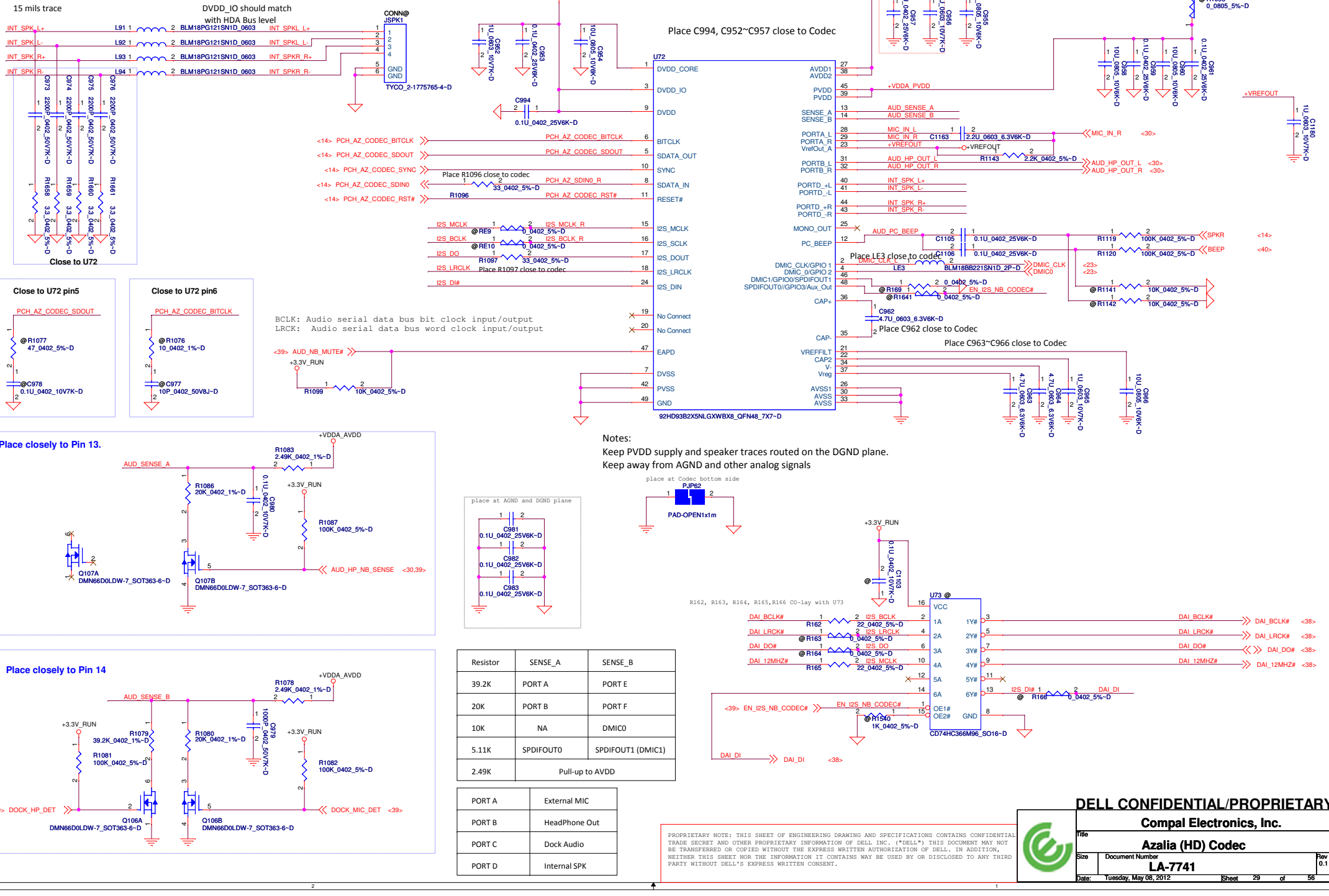
Compal Electronics, Inc.

Title: ODD CONNECTOR

Size | Document Number: LA-7741 | Rev: 0.1

Date: Tuesday, May 08, 2012 | Sheet 28 of 56

Internal Speakers Header



Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

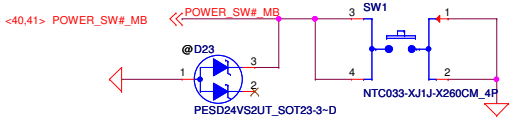
PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Dock Audio
PORT D	Internal SPK

Compal Electronics, Inc.

Title: Azalia (HD) Codec

Size: | Document Number: LA-7741 | Rev: 0.1

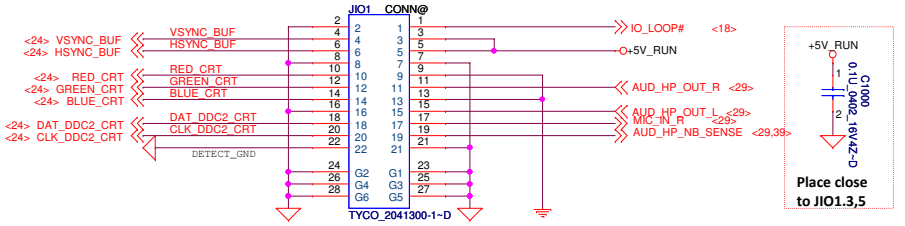
Date: Tuesday, May 08, 2012 | Sheet 29 of 56



POWER & INSTANT ON SWITCH

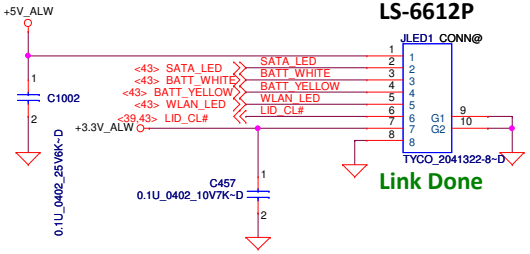
I/O board CONN.

Link Done

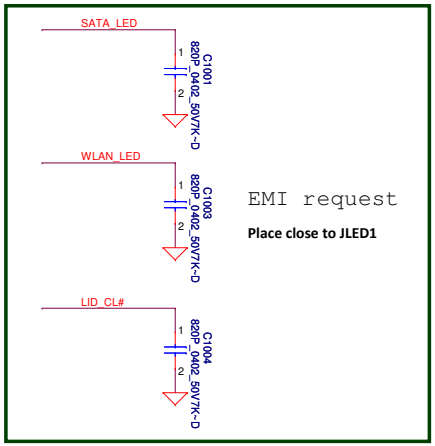


LED Board with Lid

LS-6612P



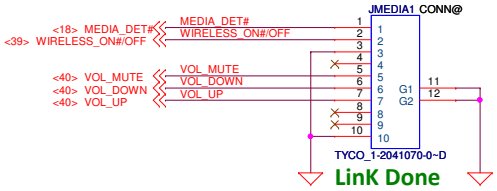
Link Done



Defult on,
WIRELESS_ON/OFF#:
LOW: ON
HIGH: OFF

Media Board

LS-6613P



LinK Done

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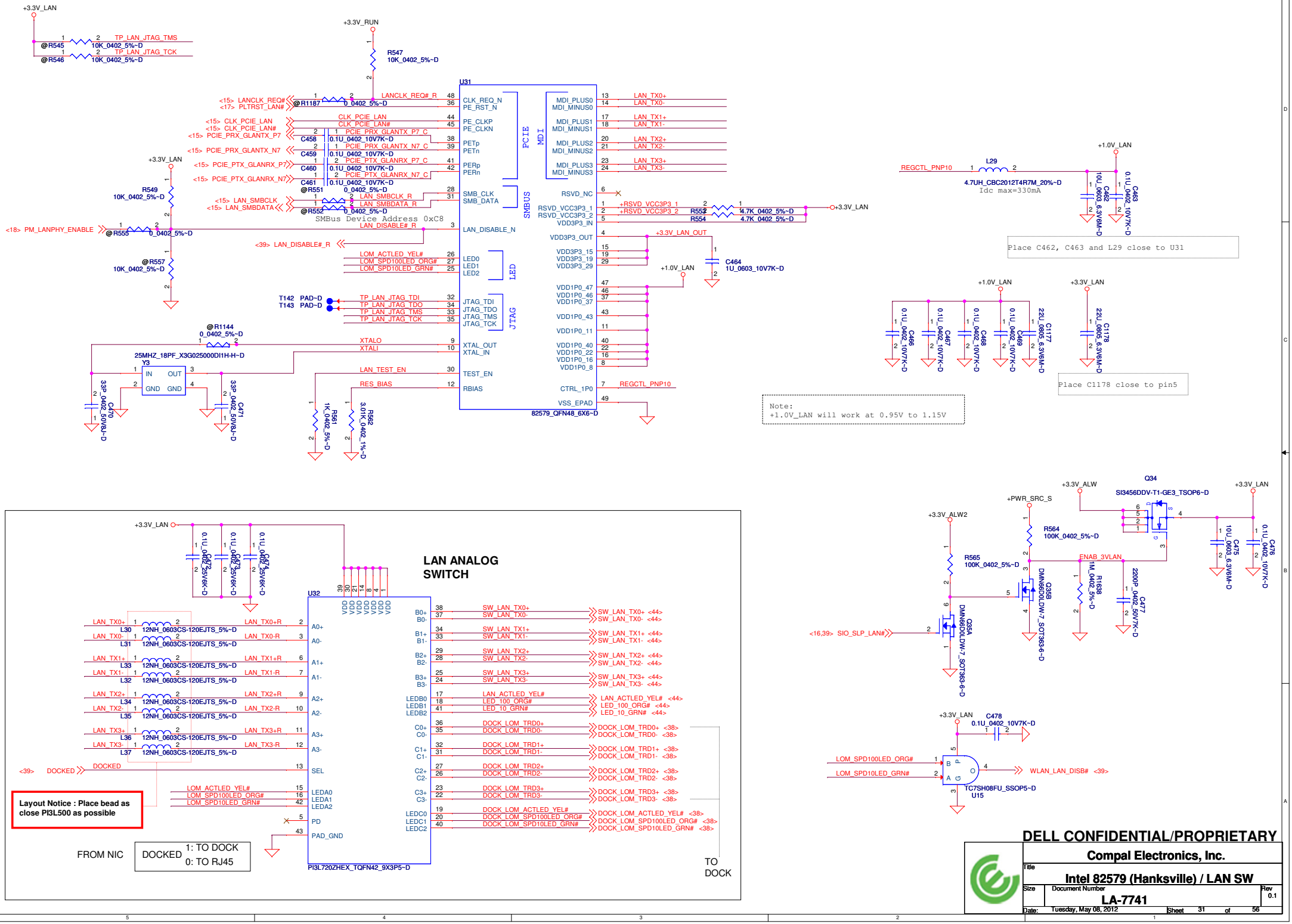
Compal Electronics, Inc.	
Title	PWR SW/Sub-board Connector
Size	Document Number: LA-7741 — Rev: 0.1
Date: Tuesday, May 08, 2012	Sheet 30 of 56


+3.3V_LAN
+3.3V_RUN
U31
82579_QFN48_6X6~D
SMBus Device Address 0xC8
Y3
25MHZ_18PF_X3G025000DI1H-H~D
Note:
+1.0V_LAN will work at 0.95V to 1.15V
Place C462, C463 and L29 close to U31
Place C1178 close to pin5
LAN ANALOG SWITCH
U32
PI3L720ZHEX_TQFN42_9X3P5~D
Layout Notice : Place bead as close PI3L500 as possible
FROM NIC
DOCKED 1: TO DOCK 0: TO RJ45
TO DOCK
Q34
SI3456DDV-T1-GE3_TSOP6~D
Q35A
Q35B
DMN66D0LDW-7_SOT363-6~D
U15
TC7SH08FU_SSOP5~D
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Intel 82579 (Hanksville) / LAN SW
LA-7741
Tuesday, May 08, 2012
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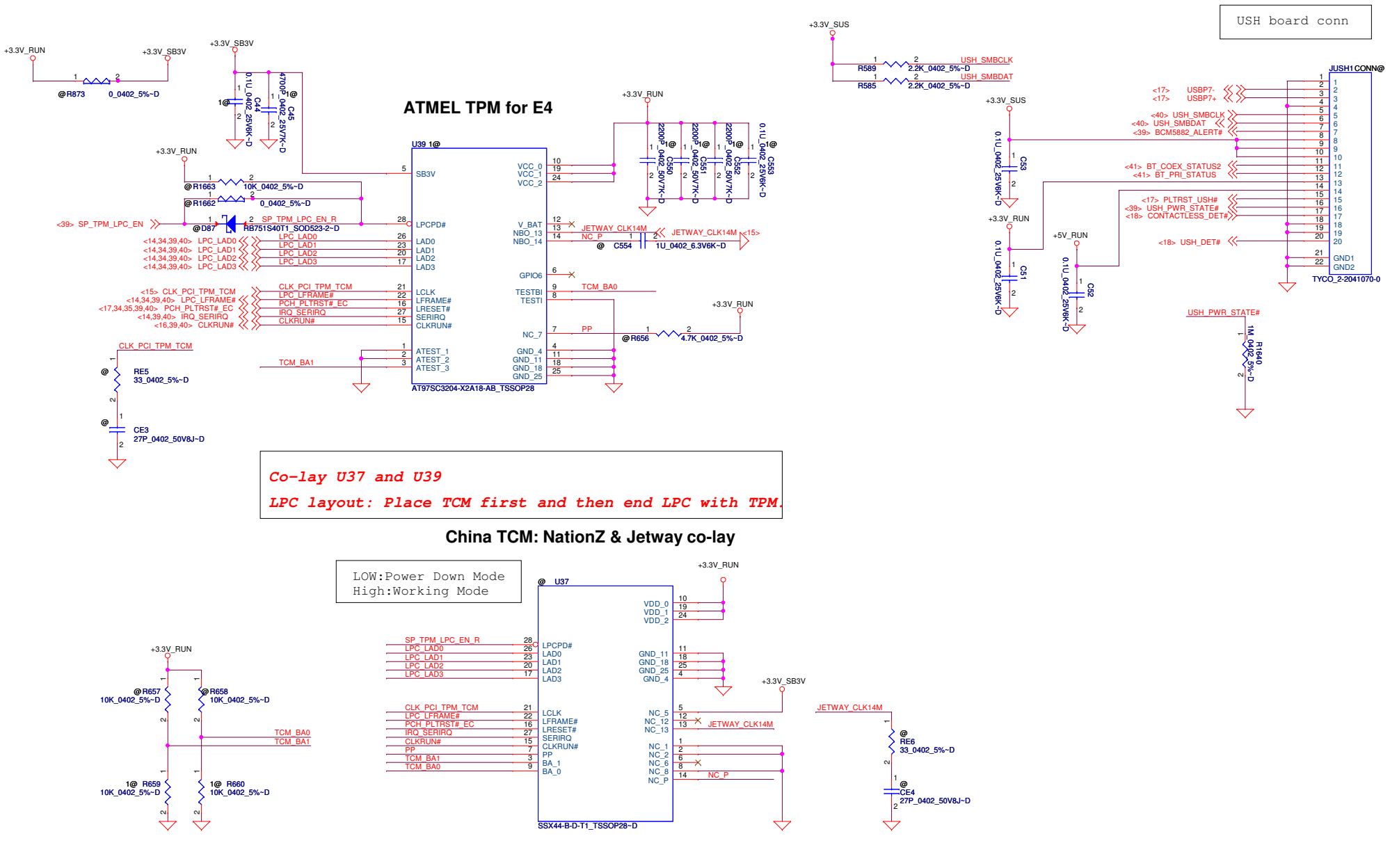

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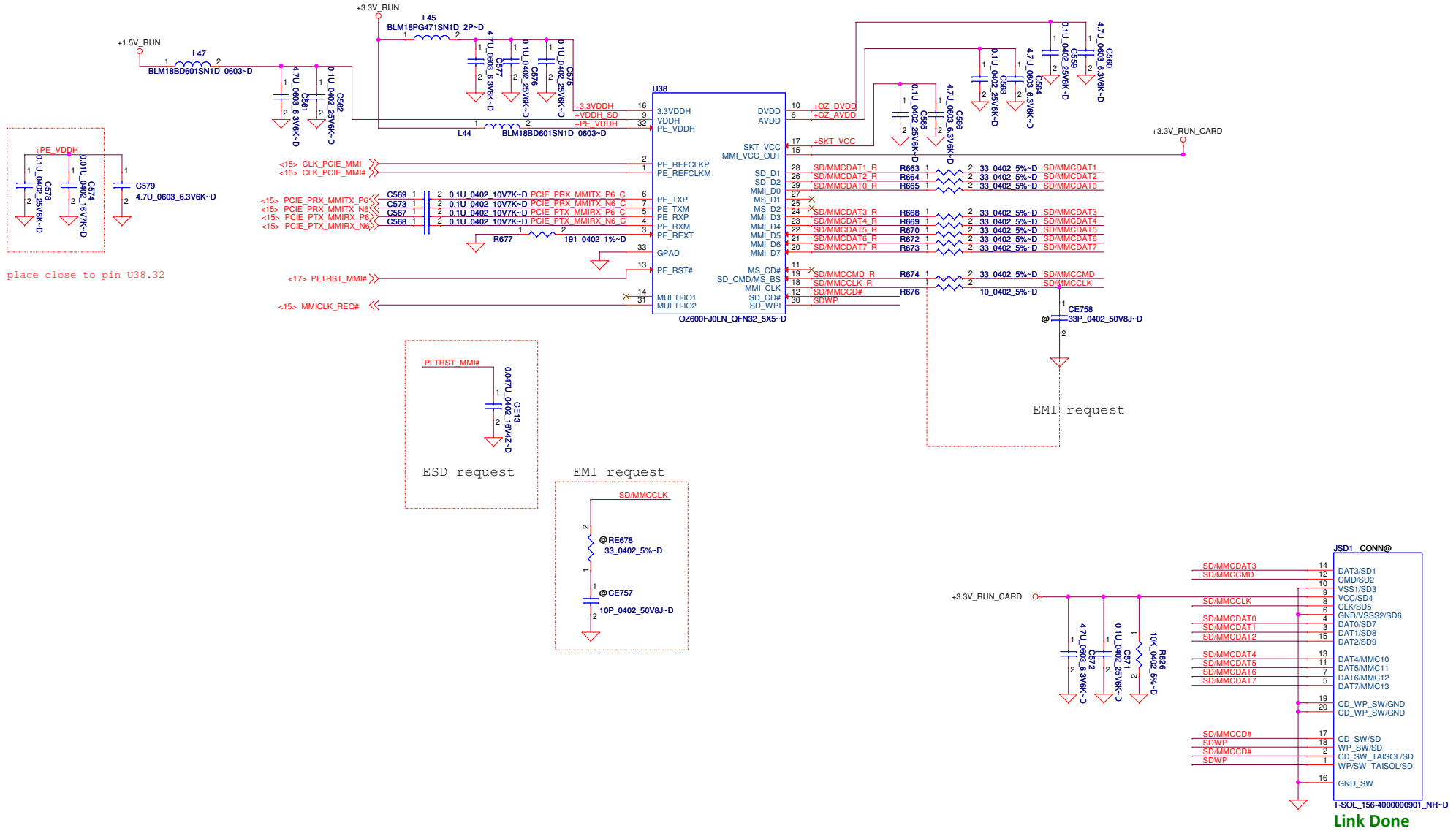
Compal Electronics, Inc.

Title: TPM/TCM

Size | Document Number: LA-7741 | Rev: 0.1

Date: Tuesday, May 08, 2012 | Sheet 32 of 56

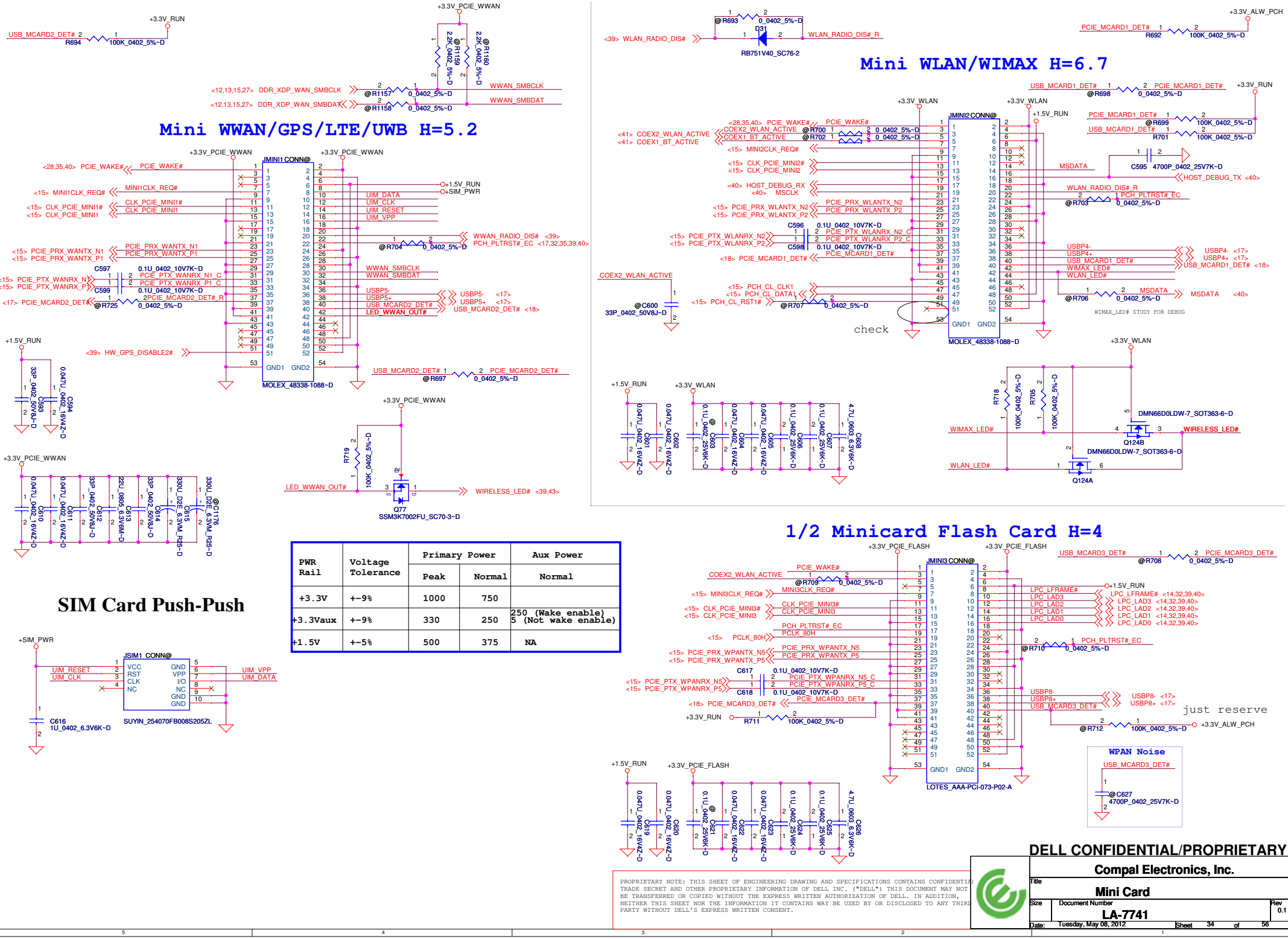


Compal Electronics, Inc.

Title: Card Reader

Size | Document Number: LA-7741 | Rev: 0.1

Date: Tuesday, May 08, 2012 | Sheet 33 of 56



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA

Compal Electronics, Inc.

Title: Mini Card

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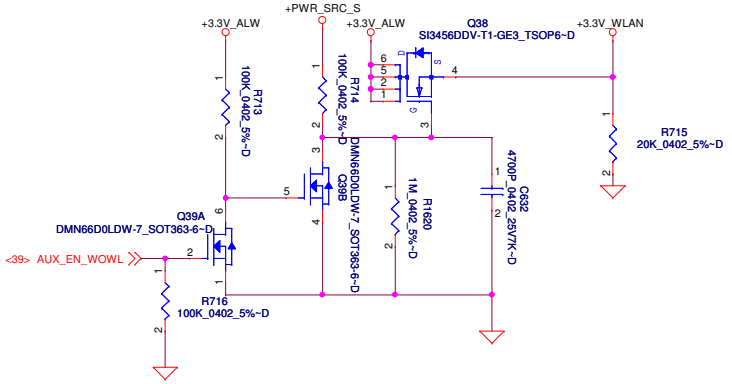
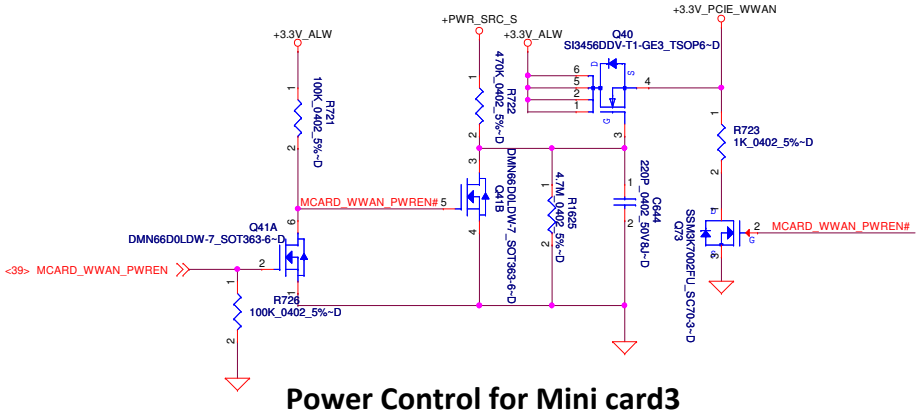
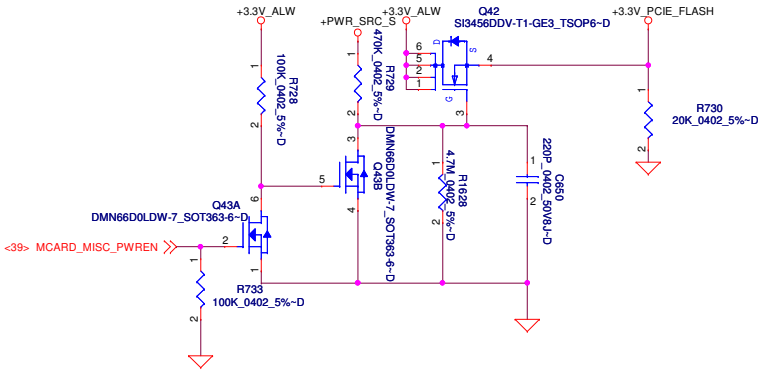
Power Control for Mini card2



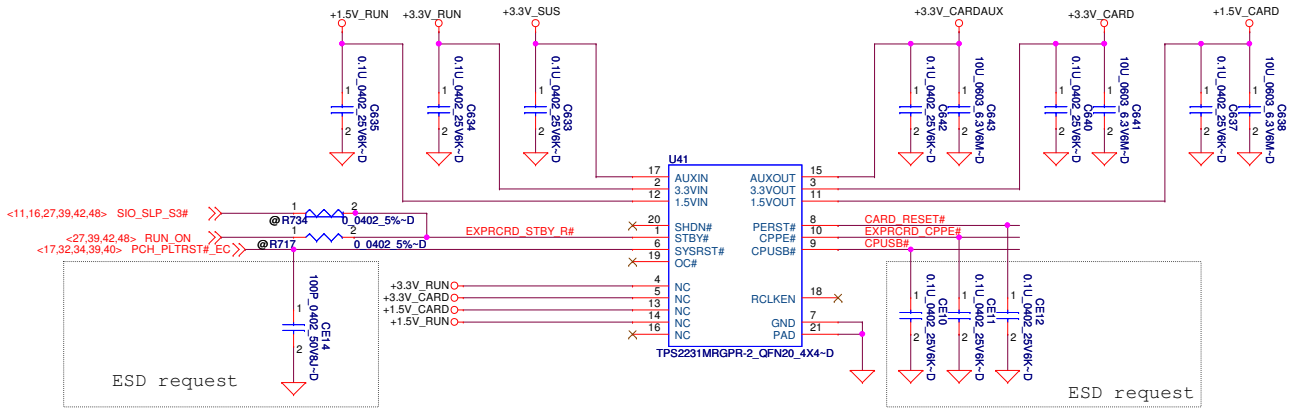
Power Control for Mini card1



Power Control for Mini card3

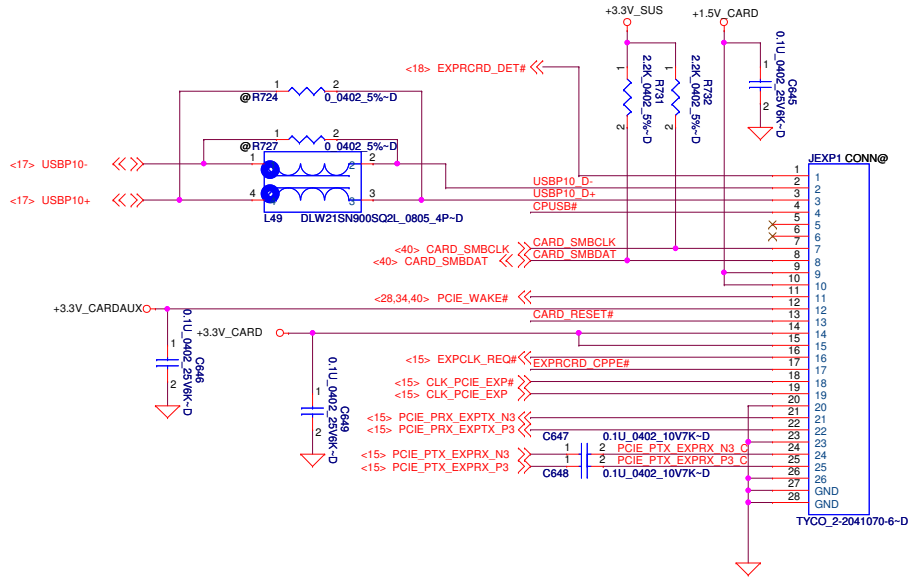


Express Card PWR S/W



Note: Add connection on pin4, pin5, pin 13 and pin14 to support GMT 2nd source part

Express Card Conn.

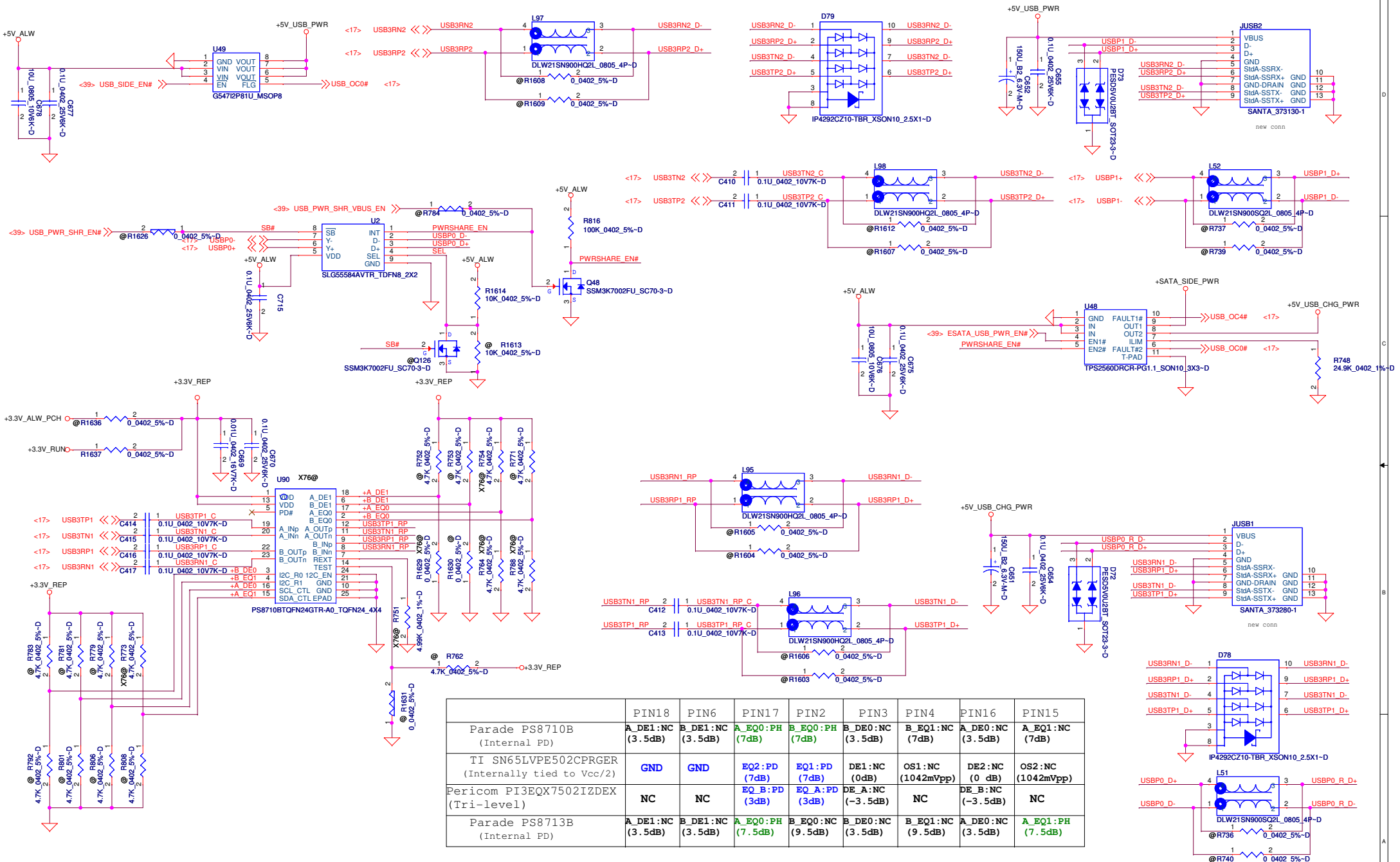


Compal Electronics, Inc.

Title: PCIE-SATA SW / PCIE PWR

Size | Document Number: LA-7741 | Rev: 0.1

Date: Tuesday, May 08, 2012 | Sheet 35 of 56



	PIN18	PIN6	PIN17	PIN2	PIN3	PIN4	PIN16	PIN15
Parade PS8710B (Internal PD)	A_DE1:NC (3.5dB)	B_DE1:NC (3.5dB)	A_EQ0:PH (7dB)	B_EQ0:PH (7dB)	B_DE0:NC (3.5dB)	B_EQ1:NC (7dB)	A_DE0:NC (3.5dB)	A_EQ1:NC (7dB)
TI SN65LVPE502CPRGER (Internally tied to Vcc/2)	GND	GND	EQ2:PD (7dB)	EQ1:PD (7dB)	DE1:NC (0dB)	OS1:NC (1042mVpp)	DE2:NC (0 dB)	OS2:NC (1042mVpp)
Pericom PI3EQX7502IZDEX (Tri-level)	NC	NC	EQ_B:PD (3dB)	EQ_A:PD (3dB)	DE_A:NC (-3.5dB)	NC	DE_B:NC (-3.5dB)	NC
Parade PS8713B (Internal PD)	A_DE1:NC (3.5dB)	B_DE1:NC (3.5dB)	A_EQ0:PH (7.5dB)	B_EQ0:NC (9.5dB)	B_DE0:NC (3.5dB)	B_EQ1:NC (9.5dB)	A_DE0:NC (3.5dB)	A_EQ1:PH (7.5dB)

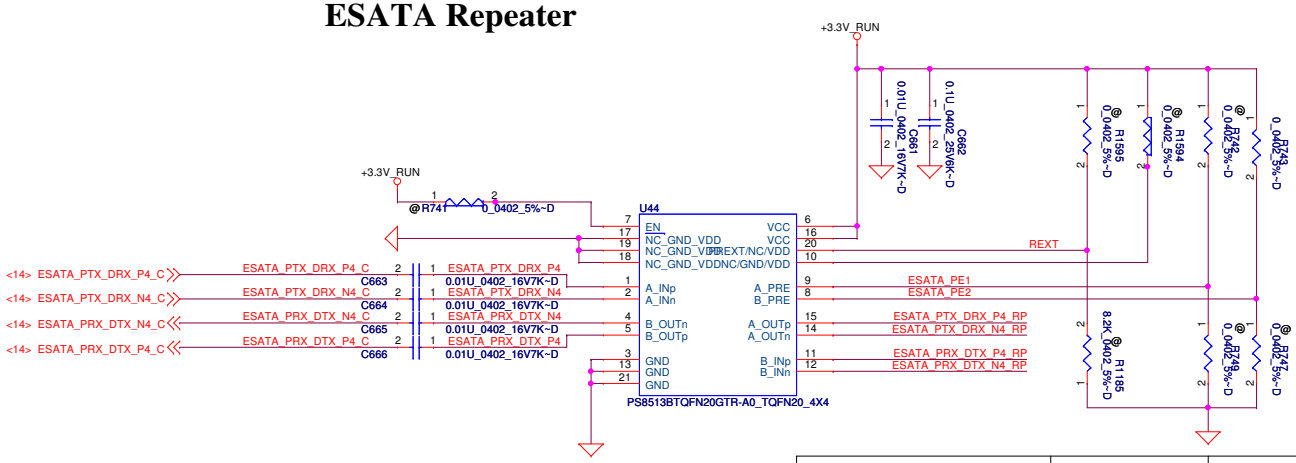
Compal Electronics, Inc.

Title: USB 3.0 x2

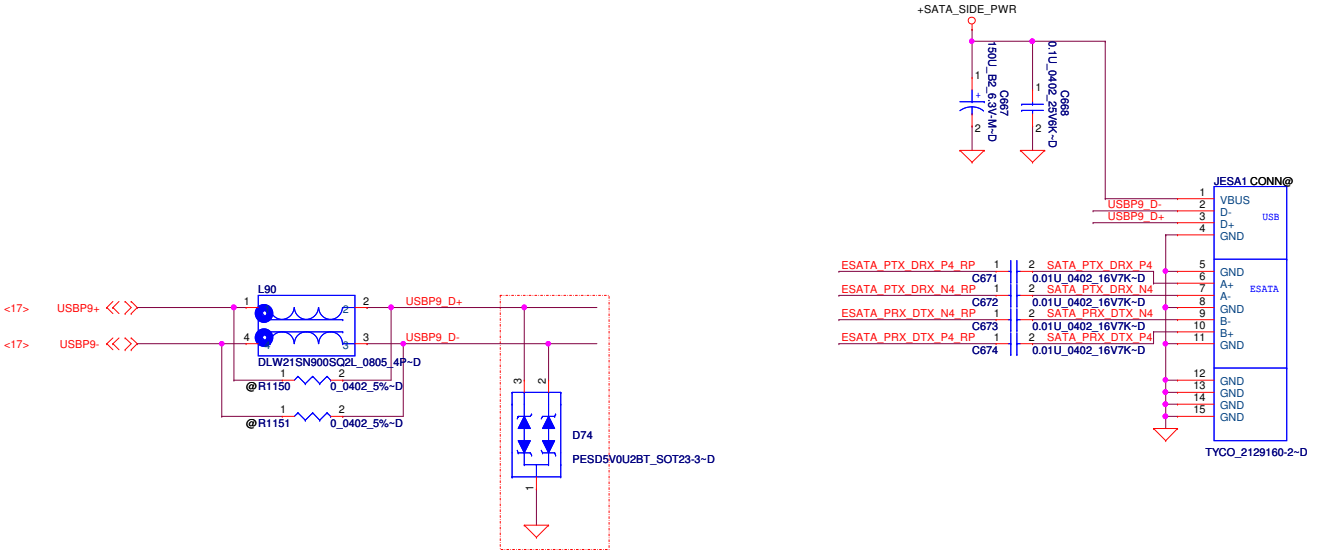
Size: | Document Number: LA-7741 | Rev: 0.1

Date: Tuesday, May 08, 2012 | Sheet 36 of 56

ESATA Repeater



	PIN8	PIN9	PIN20
Parade PS8513B (Internal PD)	**B_PRE:PH (3.5dB)**	**A_PRE:NC (0dB)**	**NC (de-pop R1595)**
MAXIM MAX4951C (Internal PD)	**B_PRE:PH (3.0dB)**	**A_PRE:NC (0dB)**	**NC (de-pop R1595)**
TI SN75LVCP412A (Internal PD)	**B_PRE:PH (2.5dB)**	**A_PRE:NC (0dB)**	**NC (de-pop R1595)**



Place D74 close to JESATA1

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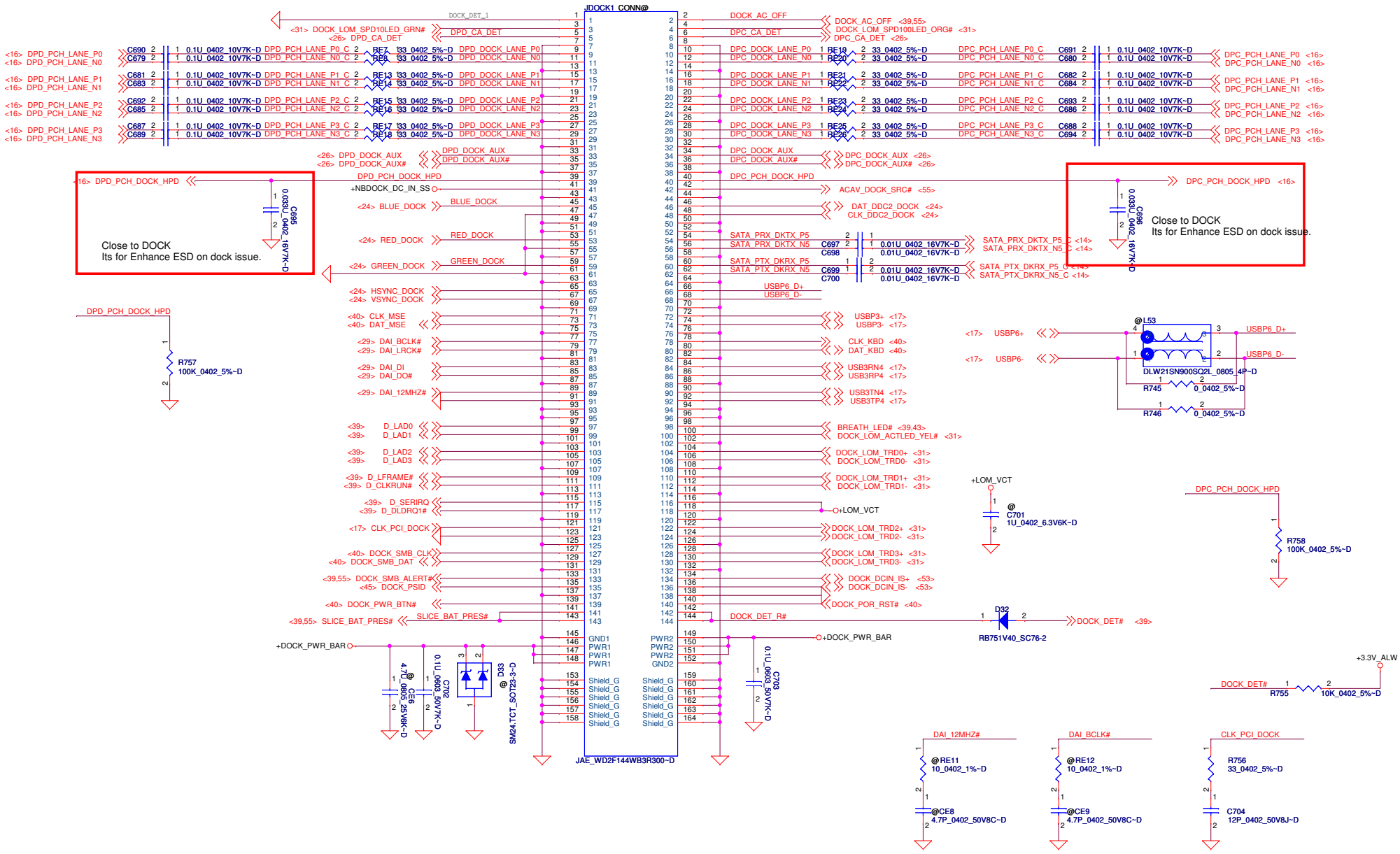
Compal Electronics, Inc.

Title: USB/ESATA/IO/MDC

Size: | Document Number: LA-7741 | Rev: 0.1

Date: Tuesday, May 08, 2012 | Sheet 37 of 56

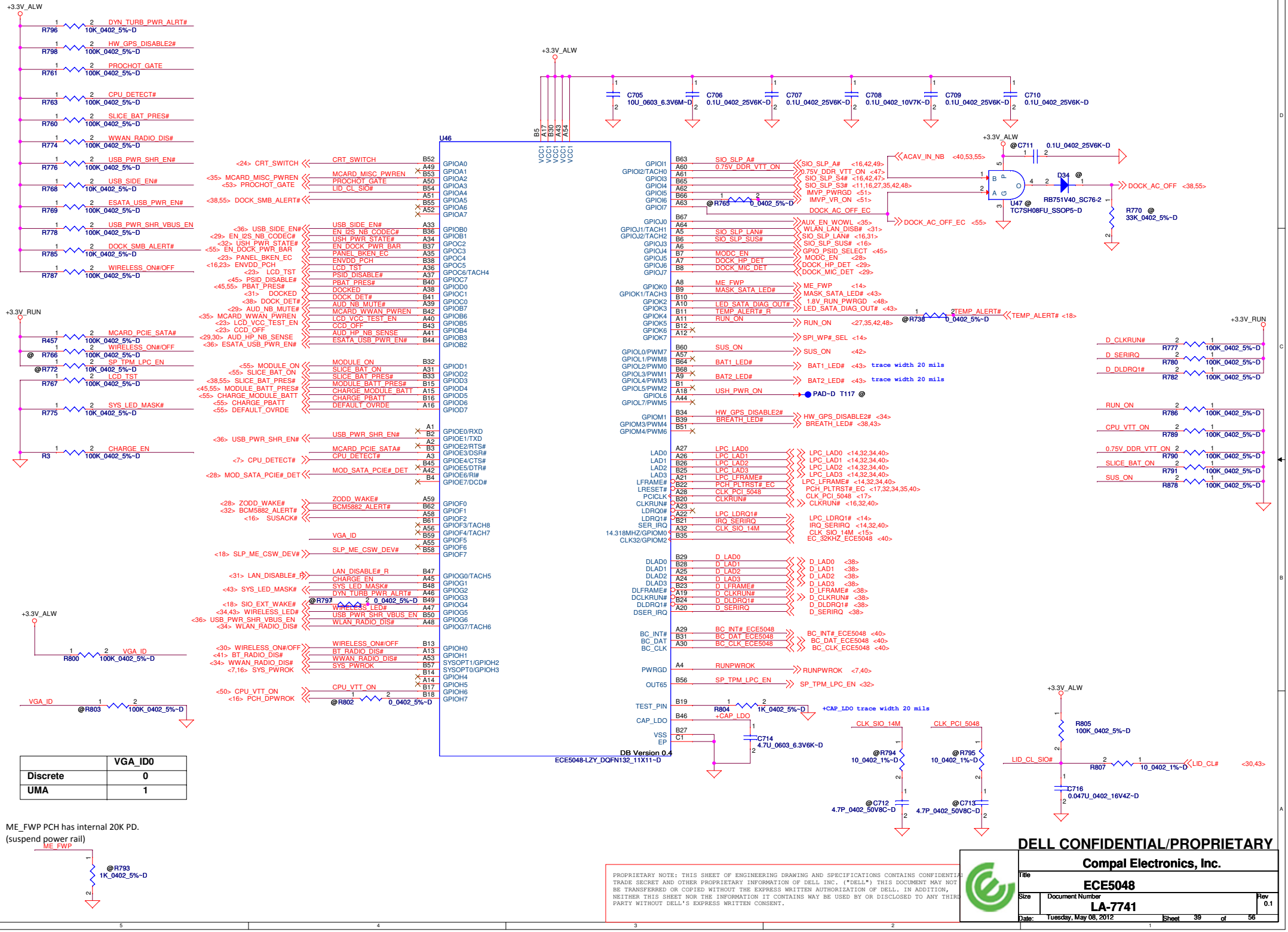


Compal Electronics, Inc.

Title: DOCKING CONN

Size: | Document Number: LA-7741 | Rev: 0.1

Date: Tuesday, May 08, 2012 | Sheet 38 of 56



	VGA_ID0
Discrete	0
UMA	1

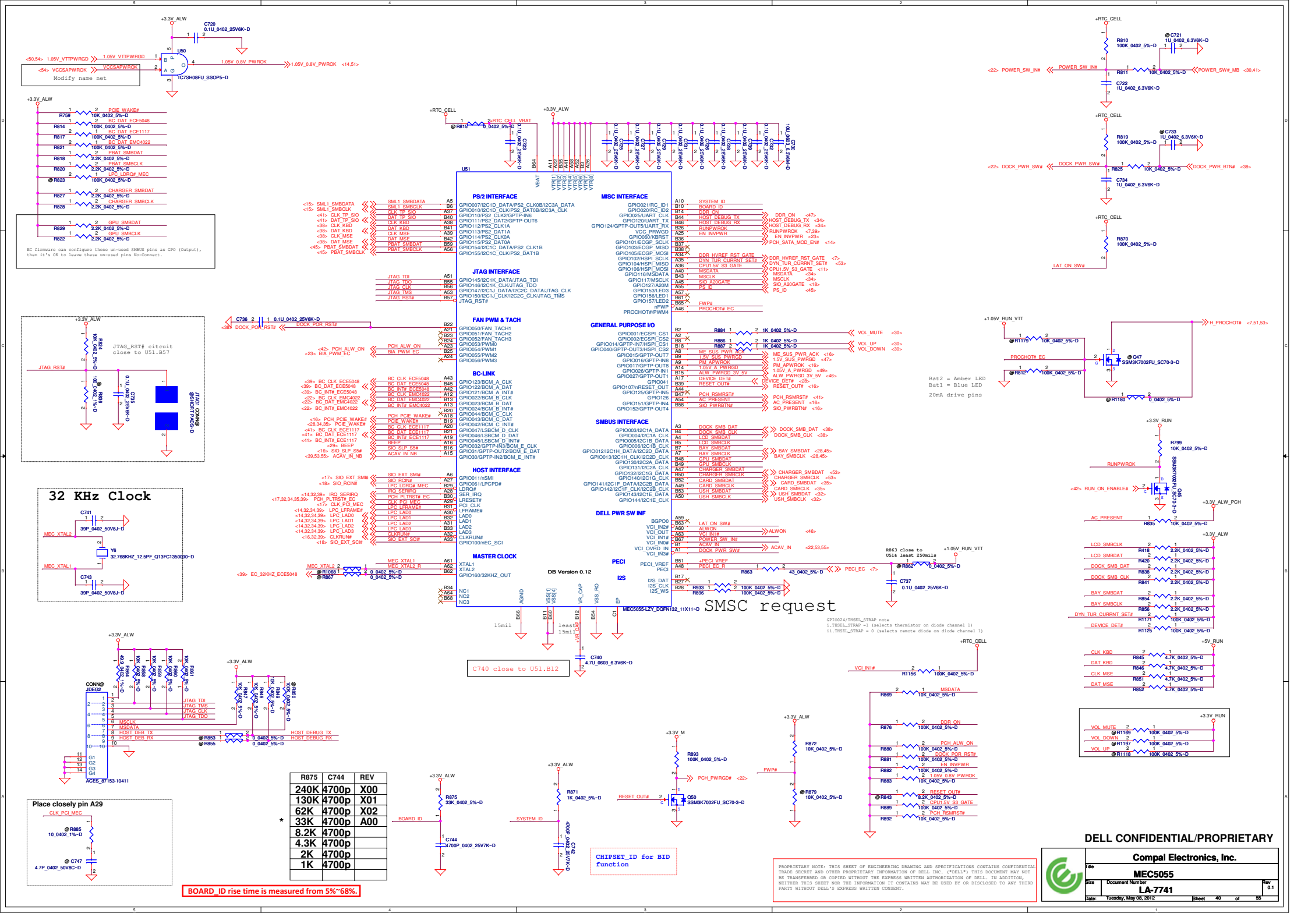
ME_FWP PCH has internal 20K PD.
(suspend power rail)

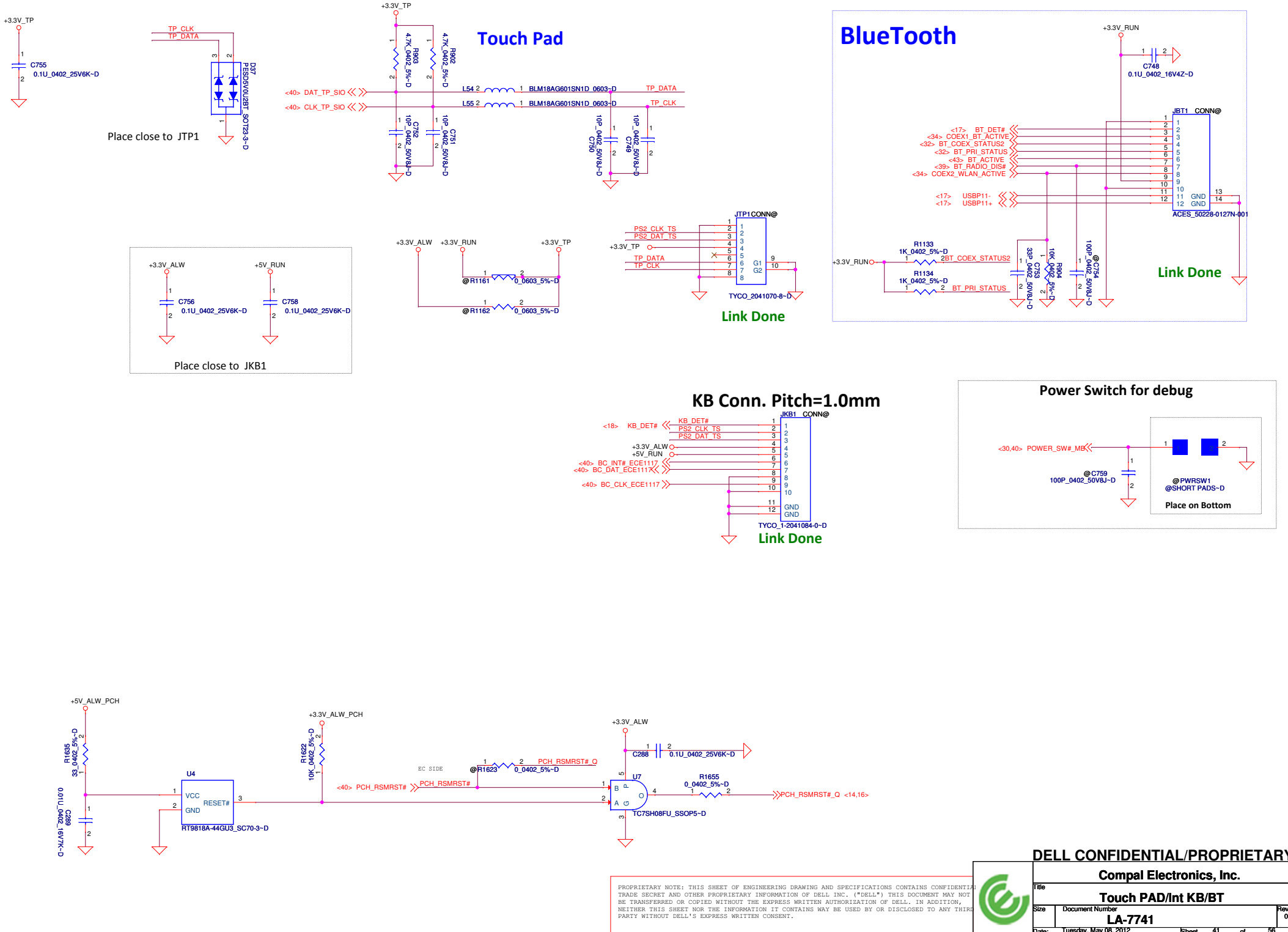
Compal Electronics, Inc.

Title: ECE5048

Size: | Document Number: LA-7741 | Rev: 0.1

Date: Tuesday, May 08, 2012 | Sheet 39 of 56


32 KHz Clock
MEC5055-LZY-DOPN132_11X11~D
DB Version 0.12
SMSC request
MASTER CLOCK
HOST INTERFACE
BC-LINK
FAN PWM & TACH
JTAG INTERFACE
PS/2 INTERFACE
MISC INTERFACE
GENERAL PURPOSE I/O
SMBUS INTERFACE
DELL PWR SW INF
PECI
I2S
Place closely pin A29
BOARD_ID rise time is measured from 5%~68%.
CHIPSET_ID for BID function
C740 close to U51.B12
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
MEC5055
LA-7741



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	Touch PAD/Int KB/BT
Size	Document Number: LA-7741
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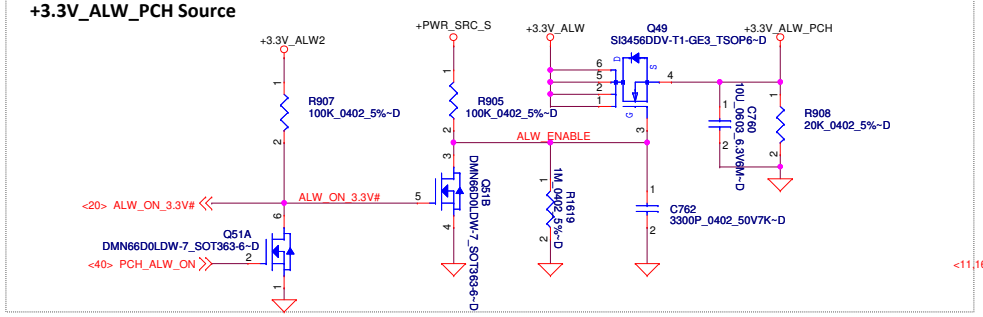
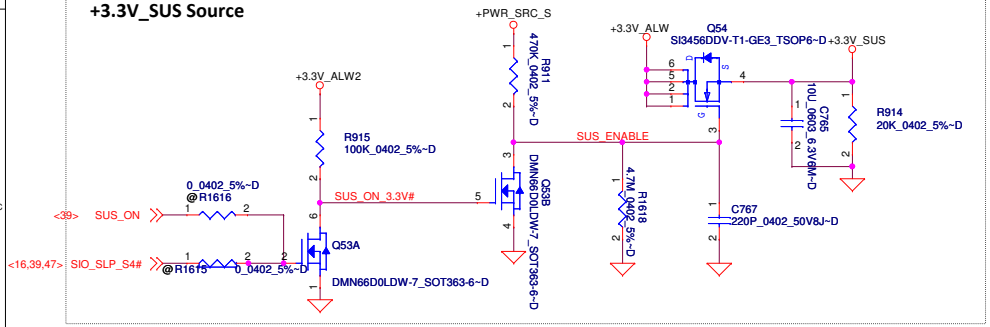
DC/DC Interface

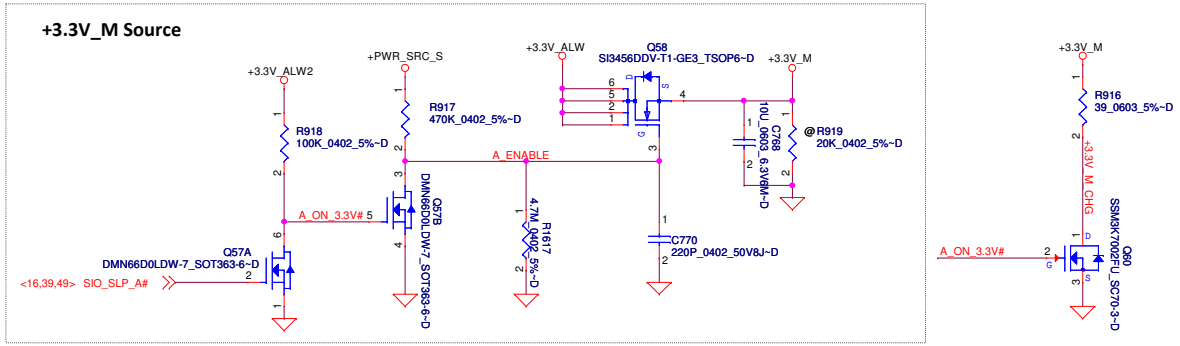
+3.3V_ALW_PCH Source



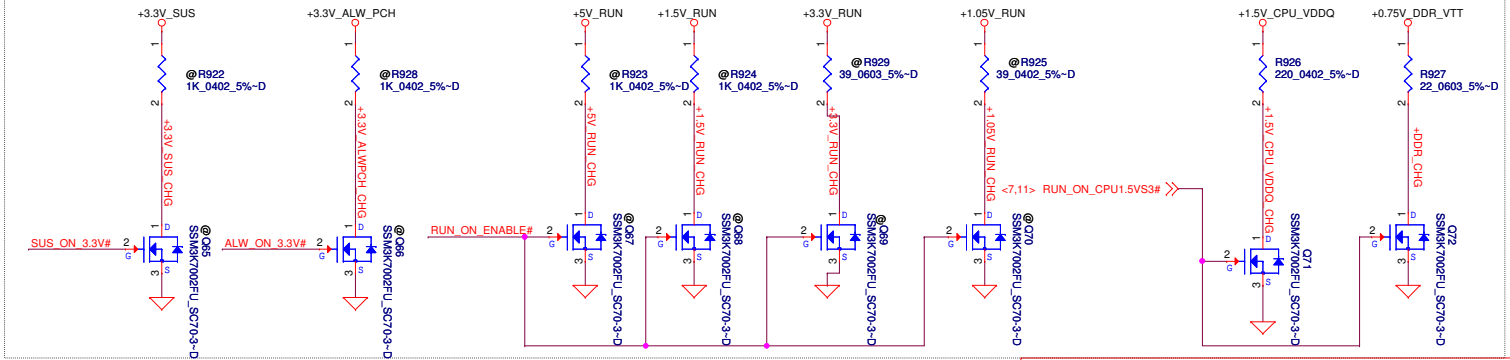
+3.3V_SUS Source



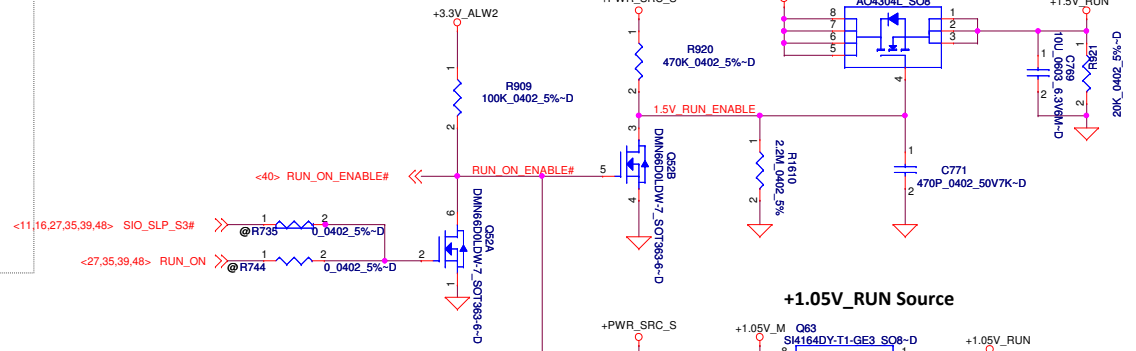
+3.3V_M Source



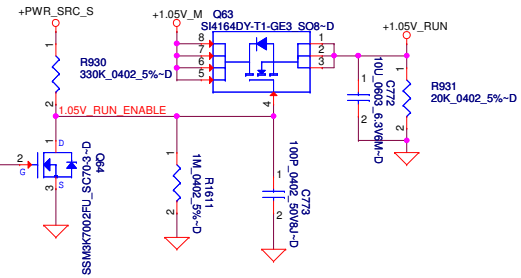
Discharg Circuit



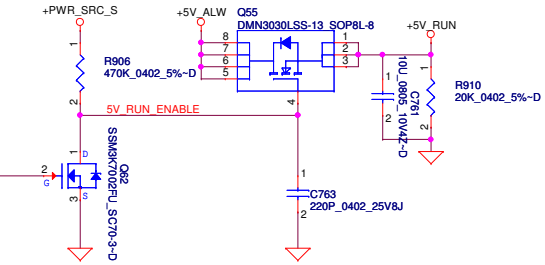
+1.5V_RUN Source



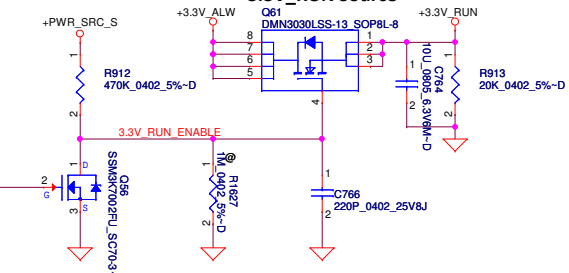
+1.05V_RUN Source



+5V_RUN Source



+3.3V_RUN Source



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Compal Electronics, Inc.	
Title	POWER CONTROL
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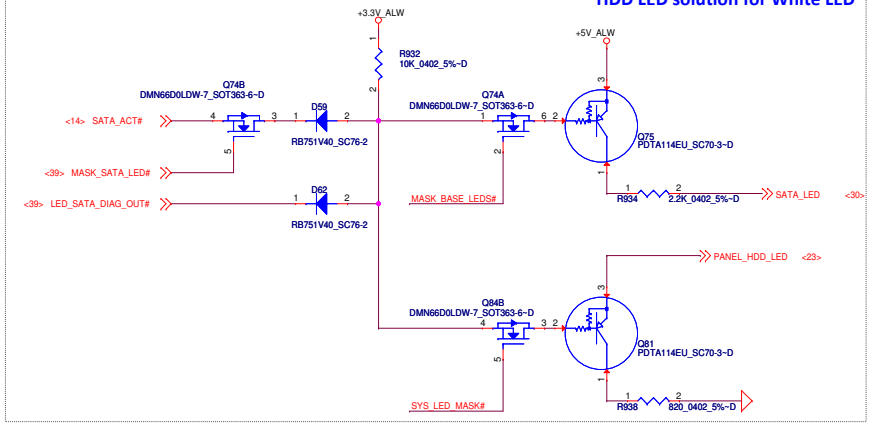
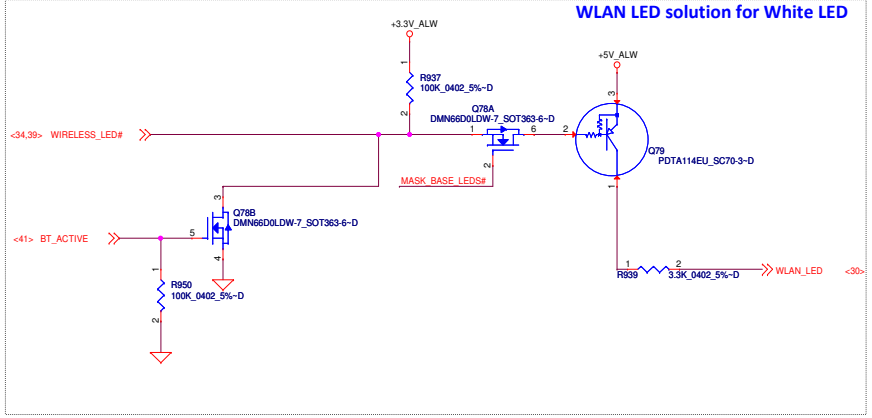
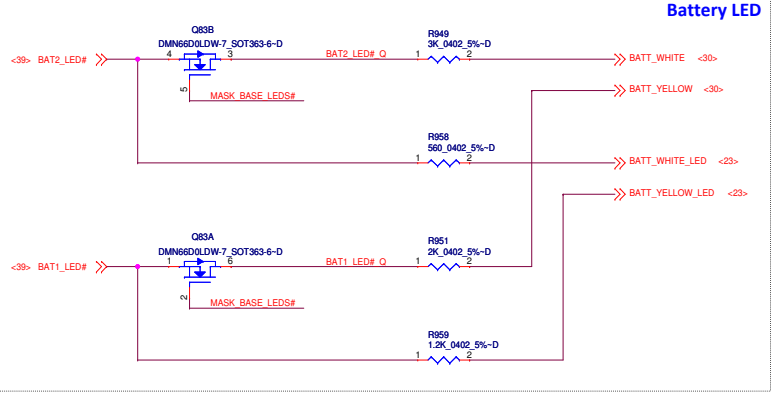
HDD LED solution for White LED



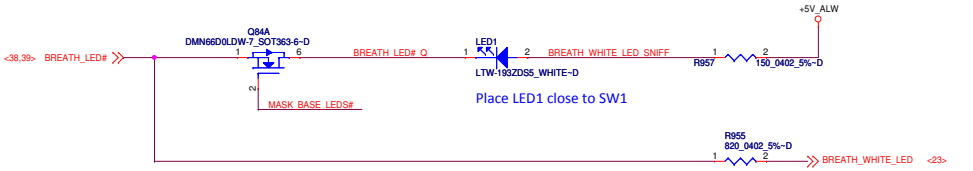
WLAN LED solution for White LED

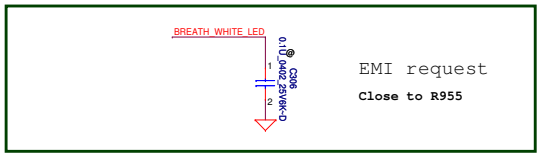


Battery LED

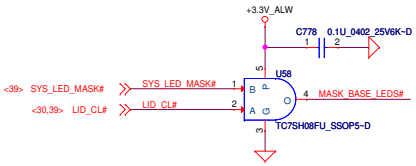


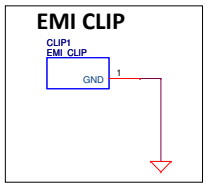
Breath LED

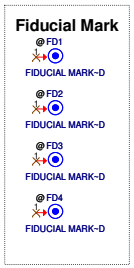


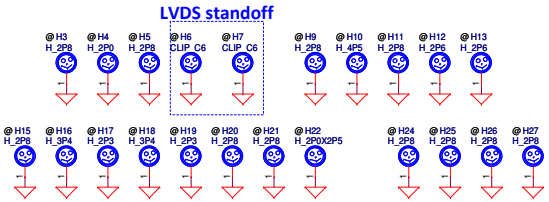


LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1









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Compal Electronics, Inc.

Title: PAD and Standoff

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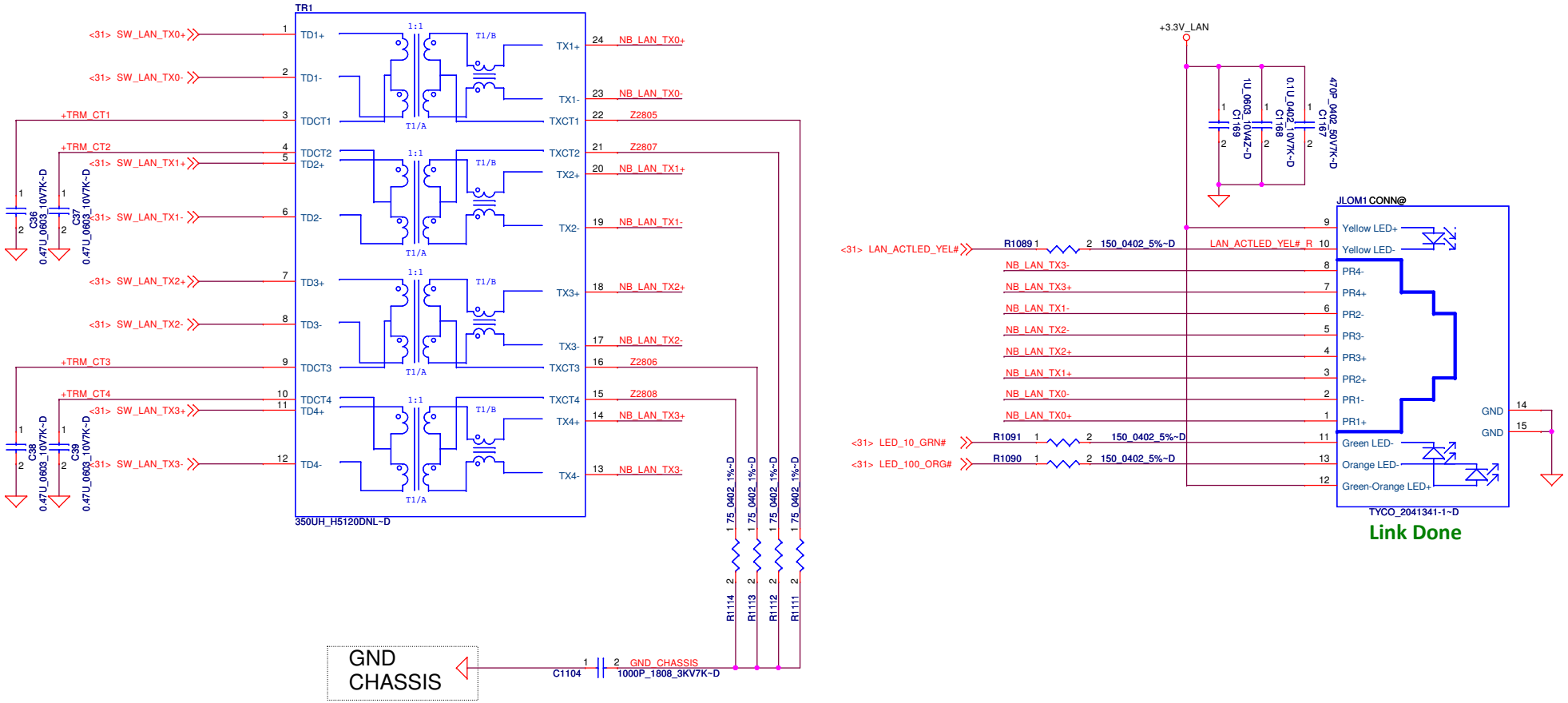

Link Done

Compal Electronics, Inc.

Title	RJ45	
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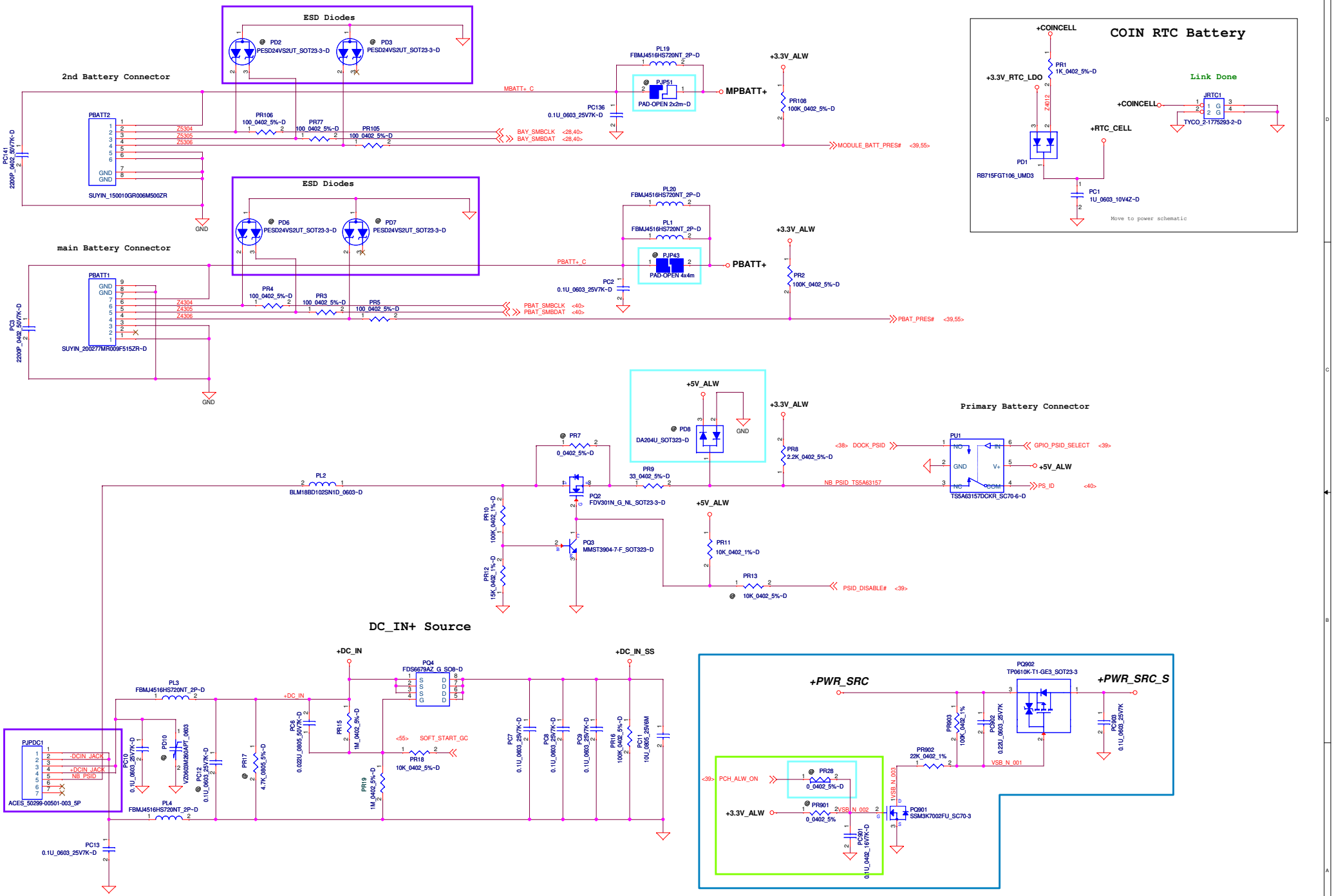

Compal Electronics, Inc.			
Title: +DCIN			
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+5V_ALWP/ +3.3V_ALWP

3.3VALWP +/- 5%
TDC=5.45A
Peak Current=7.786A
OCP min=10.122A
L/S RDS(on) 14.2m ohm(typ),17.5m ohm(max)
FSW=375KHz
Delta_Iin=1.246A
Delta_Io=3.3231A

5VALWP +/- 5%
TDC=8.41A
Peak Current=12.012A
OCP min=15.62A
L/S RDS(on) 9.7m ohm(typ),14.5m ohm(max)
FSW=300KHz
Delta_Iin=1.64A
Delta_Io=3.756A

Charlie_note :
SKIPSEL Connect to REF : DEM Mode
@DEM VFBx=2.0V

TONSEL
Frequency Selectable Input for VOUT1(+5v)/VOUT2(+3.3v) respectively.
300kHz/375kHz : Connect to REF

+PWR_SRC
PJP5 PAD-OPEN 4x4m
@ PL24 HCB2012KF-121T50_0805
+DC1_PWR_SRC
PC22 0.1U_0402_25V6
PC21 2200P_0402_50V7K
PC23 10U_0805_25V6K
@ PC24 10U_0805_25V6K
+3.3V_RTC_LDO
+3.3V_ALW2
@ PR27 0_0402_5%~D
PQ6 AON7408L_DFN8-5
PC28 10U_0805_6.3V6M~D
PR37 13.7K_0402_1%
PR43 20K_0402_1%~D
PR33 140K_0402_1%
2VREF_6182
PC36 1U_0603_16V6K
PR36 30.9K_0402_1%
PR42 20K_0402_1%~D
PR34 232K_0402_1%~D
FB_5V
FB_3V
ENTRIP2
ENTRIP1
PU2
P PAD
VO2
VREG3
BOOT2
UGATE2
PHASE2
LGATE2
TONSEL
REF
FB2
FB1
VO1
PGOOD
BOOT1
UGATE1
PHASE1
LGATE1
EN
SKIPSEL
GND
VIN
VREG5
NC
RT8205LZQW(2) WQFN 24P PWM
Typ: 175mA
PC38 0.22U_0603_25V7K~D
PR41 2.2_0603_5%
BST1_3V
BST_3V
UG_3V
LX_3V
LG_3V
PC37 0.22U_0603_25V7K~D
PR38 2.2_0603_5%
BST_5V
BST1_5V
UG_5V
LX_5V
LG_5V
+DC1_PWR_SRC
PC17 0.1U_0402_25V6
PC16 2200P_0402_50V7K
PC18 10U_0805_25V6K
@ PC20 10U_0805_25V6K
PQ5 FDS8878_G 1N SO8
PQ7 FDMS7692 1N POWER56-8
+3.3V_ALWP
PL8 2.2UH_ETQP3W2R2WFN_8.5A_20%
PC40 220U_6.3V_R17M
PR39 4.7_1206_5%
SNUB_3V
PC34 680P_0603_50V7K
PQ8 IRF8707GTRPBF_SO8
PL7 3.3UH_FDVE1040-H-3R3M=P3_11.3A_20%~D
+5V_ALWP
PR40 4.7_1206_5%
SNUB_5V
PC33 680P_0603_50V7K
PC35 220U_6.3V_R17M
+5V_ALW2
Typ: 175mA
PC26 4.7U_0805_10V6K
PC27 0.1U_0603_25V7K
+3.3V_ALW
PR20 100K_0402_1%
ALW_PWRGD_3V_5V <40>
+PWR_SRC
@ PD37 MMSZ5229BS_SOD323-2
@ PR46 499K_0402_1%~D
@ PR47 300K_0402_1%
@ PC19 1U_0603_10V6K
2VREF_6182
Max: 100uA
+DC1_PWR_SRC
PJP9 PAD-OPEN 4x4m
PJP10 PAD-OPEN 4x4m
+3.3V_ALWP
+3.3V_ALW
(5.45A,218mils ,Via NO.= 11)
PC30 0.1U_0402_25V6
PQ70B 2N7002DW-T/R7_SOT363-6~D
PQ70A 2N7002DW-T/R7_SOT363-6~D
PR150 100K_0402_1%
+5V_ALW2
PR147 2K_0402_1%~D
<40> ALWON
PR151 0_0402_5%
<22> THERM_STP#
PQ105 PDTC115EU_SOT323-3
@ PC119 1U_0603_10V6K
PJP6 PAD-OPEN 4x4m
PJP74 PAD-OPEN 4x4m
+5V_ALWP
+5V_ALW
(8.41A,336mils ,Via NO.= 17)
PC29 0.1U_0402_25V6

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.
Title: +5V/+3.3V
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+1.5V_MEN_P/ +0.75V_P

1.5Volt +/- 5%
TDC=7.18A
Peak Current=10.25A
OCP min=13.33A
L/S RDS(on) 4.2m ohm(typ),5.1m ohm(max)
FSW=253KHz for RTON=1M ohm, spec. On-Time =303.947ns
Delta_Iin=1.458A
Delta_Io=5.4728A

0.75Volt +/- 5%
TDC=0.525A
Peak Current=0.75A
OCP min=0.975A

+PWR_SRC
PJP404
PAD-OPEN 4x4m
1.5V_B+
PC412 4.7U_0805_25V6K~D
PC413 4.7U_0805_25V6K~D
PC414 0.1U_0402_25V6K~D
PC415 220P_0402_50V7K~D
PC416 0.22U_0603_16V7K~D
PR482 2.2_0603_5%~D
BOOT_1.5V
DH_1.5V
SW_1.5V
DL_1.5V
PQ67 SIR472DP-T1-GE3_POWERPAK8-5~D
PQ68 SIR466DP-T1-GE3_POWERPAK8-5
PL27 1UH 20% FDUE1040D-H-1R0M=P3_21.3A_20%~D
+1.5V_MEN_P
@ PC422 330U_SX_2V~R9M
PC423 330U_SX_2V~R9M
PR220 4.7_1206_5%
1SNUB_1.5V2
PC231 680P_0603_50V7K
+5V_ALW
+3.3V_ALW
PR484 5.1_0603_5%~D
PC424 1U_0603_10V6K~D
VDD_1.5V
PR485 100K_0402_1%~D
<40> 1.5V_SUS_PWRGD
1.5V_SUS_PWRGD
PR483 5.1K_0402_1%~D
CS_1.5V
PC419 1U_0603_10V6K~D
PU16 RT8207MZQW_WQFN20_3X3
LGATE PHASE UGATE BOOT VLDOIN VTT PAD
PGND VTTGND
CS VTTSNS
VDDP GND
VDD VTTREF
PGOOD VDDQ
TON S5 S3 FB
VLDOIN_1.5V
PJP204
PAD-OPEN1x1m
+1.5V_MEN_P
+0.75V_P
PC417 10U_0805_6.3V6M~D
PC418 10U_0805_6.3V6M~D
+V_DDR_REF
VDDQ_1.5V
Output voltage feedback input for VDDQ output
PC425 0.033U_0402_16V7~D
1.5V_B+
PR486 1M_0402_1%~D
S5_1.5V
S3_1.5V
+1.5V_MEN_P_FB
@ PR904 0_0402_5%~D
PR905 0_0402_5%~D
@ PC904 0.1U_0402_16V7K~D
+1.5V_MEN_P
FB sense trace
@ PR487 0_0402_5%~D
<40> DDR_ON
@ PR210 0_0402_5%~D
<41> SIO_SLP_S4#
@ PC426 0.1U_0402_16V7K~D
<39> 0.75V_DDR_VTT_ON
@ PR489 0_0402_5%~D

Mode	Level	+0.75V_P	+V_DDR_REF
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

PJP405 JUMP_43X118
PJP406 JUMP_43X118
+1.5V_MEN_P
+1.5V_MEM
+0.75V_P
PJP407 PAD-OPEN 3x3m
+0.75V_DDR_VTT

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Compal Electronics, Inc.
Title: +1.5V_MEN/+0.75V_DDR_VTT
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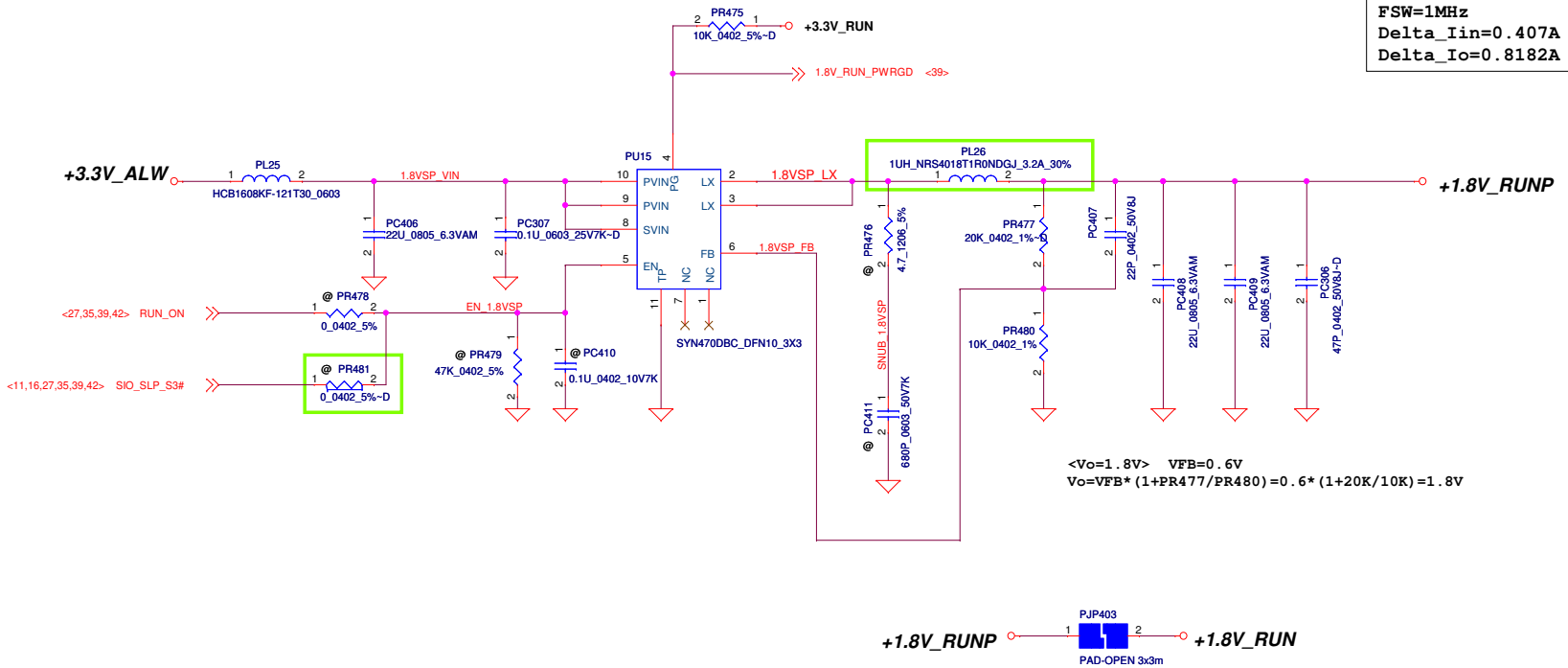
+1.8V_RUNP

1.8Volt +/-5%
TDC=0.81A
Peak Current=1.157A
OCP min=1.5A

FSW=1MHz
Delta_Iin=0.407A
Delta_Io=0.8182A



<Vo=1.8V> VFB=0.6V
Vo=VFB*(1+PR477/PR480)=0.6*(1+20K/10K)=1.8V

Compal Electronics, Inc.

Title: +1.8V_RUN

Size | Document Number: LA-7741 | Rev: 0.1

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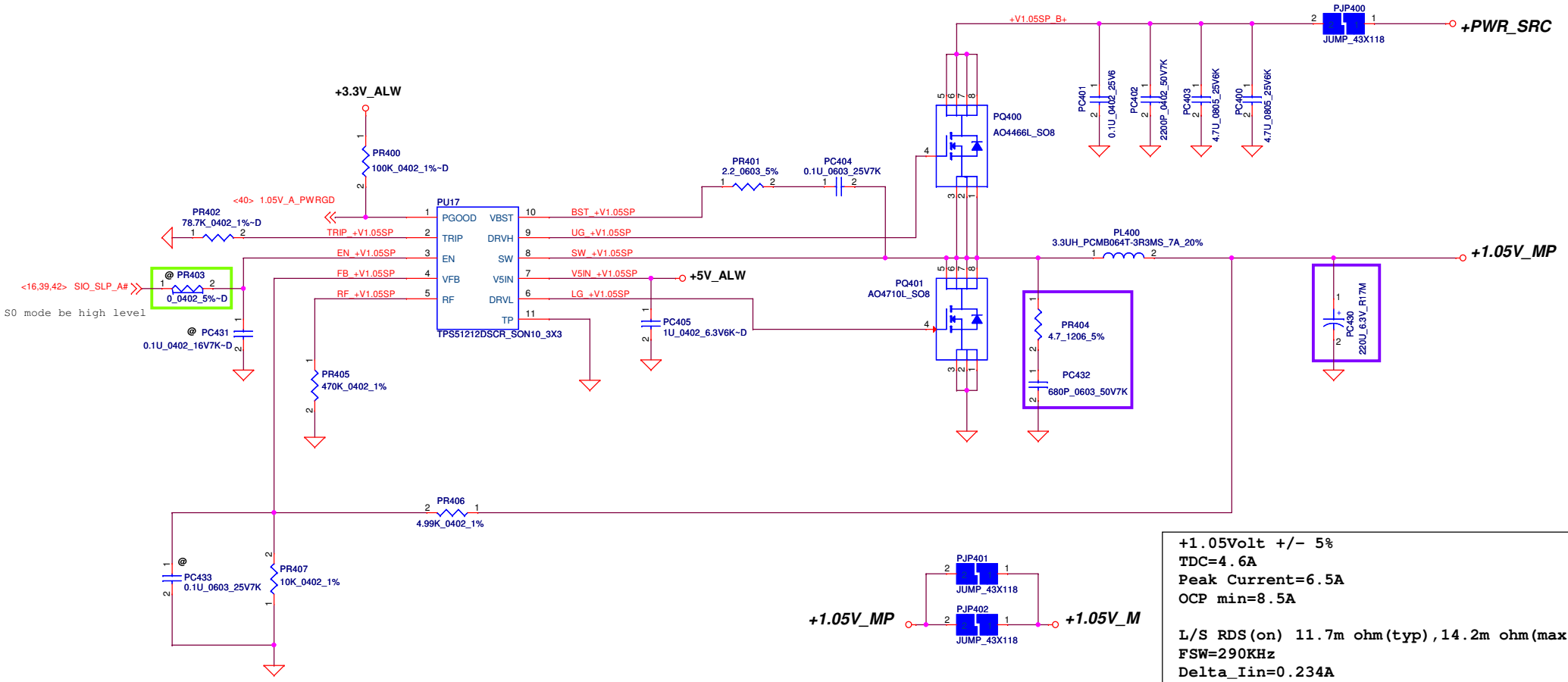
+1.05V_MP



+1.05Volt +/- 5%
TDC=4.6A
Peak Current=6.5A
OCP min=8.5A

L/S RDS(on) 11.7m ohm(typ),14.2m ohm(max)
FSW=290KHz
Delta_Iin=0.234A
Delta_Io=1.038A

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Compal Electronics, Inc.		
Title: +1.05V_M		
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+1.05VTTP

1.05Volt +/-5%
TDC=4.49A
Peak Current=6.411A
OCP min=8.334A
FSW=1MHz
Delta_Iin=0.804A
Delta_Io=1.975A

VCCP_PWRCTRL = "High" , Vo = 1.05V (SNB)
VCCP_PWRCTRL = "Low" , Vo = 1V (IVB)

Compal Electronics, Inc.

Title	ISL95870A +1.05V_RUN_VTT	
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+VCC_CORE

Charlie_note :

20110509 Maxim FAE-Allen reply:There are total 3 pcs 2.2uF capacitor for VCC(PC143), VDDA(PC160) and VDDB(PC142) pin.

Layout Note:
PC142 close to PIN15

PU9 MAX17511GTL+T_TQFN40_5X5-D

PU8 MAX17481GTA+T_TQFN8_3X3-D

PQ9, PQ11, PQ13 SIR472DP-T1-GE3_POWERPAK8-5-D

PQ10, PQ14, PQ15 SIR818DP-T1-GE3_POWERPAK8-5

PH1 10K_0402_1%_ERTJ0EG103FA-D

PH2, PH3 100K_0402_1%_TSM0B104F4251RZ-D

PL11, PL12, PL13 0.42UH_ETQP4LR42AFM_17A_20%-D

PL14 FBMA-L11-453215-121LMA90T_2

PJP27 PAD-OPEN 4x4m

PJP28 PAD-OPEN1x1m

		PQ9,PQ11,PQ13	PQ10,PQ14,PQ15
Main	X7629631L88	AON6414AL	AON6704L
2nd	X7629631L89	MDU2657RH	MDU2653RH

+VCC_CORE
TDC=37.1A
Peak Current=53A
OCP min=69A
Fsw=270KHZ

Choke DCR=1.55± 7% mΩ

Compal Electronics, Inc.

Title: Vcore

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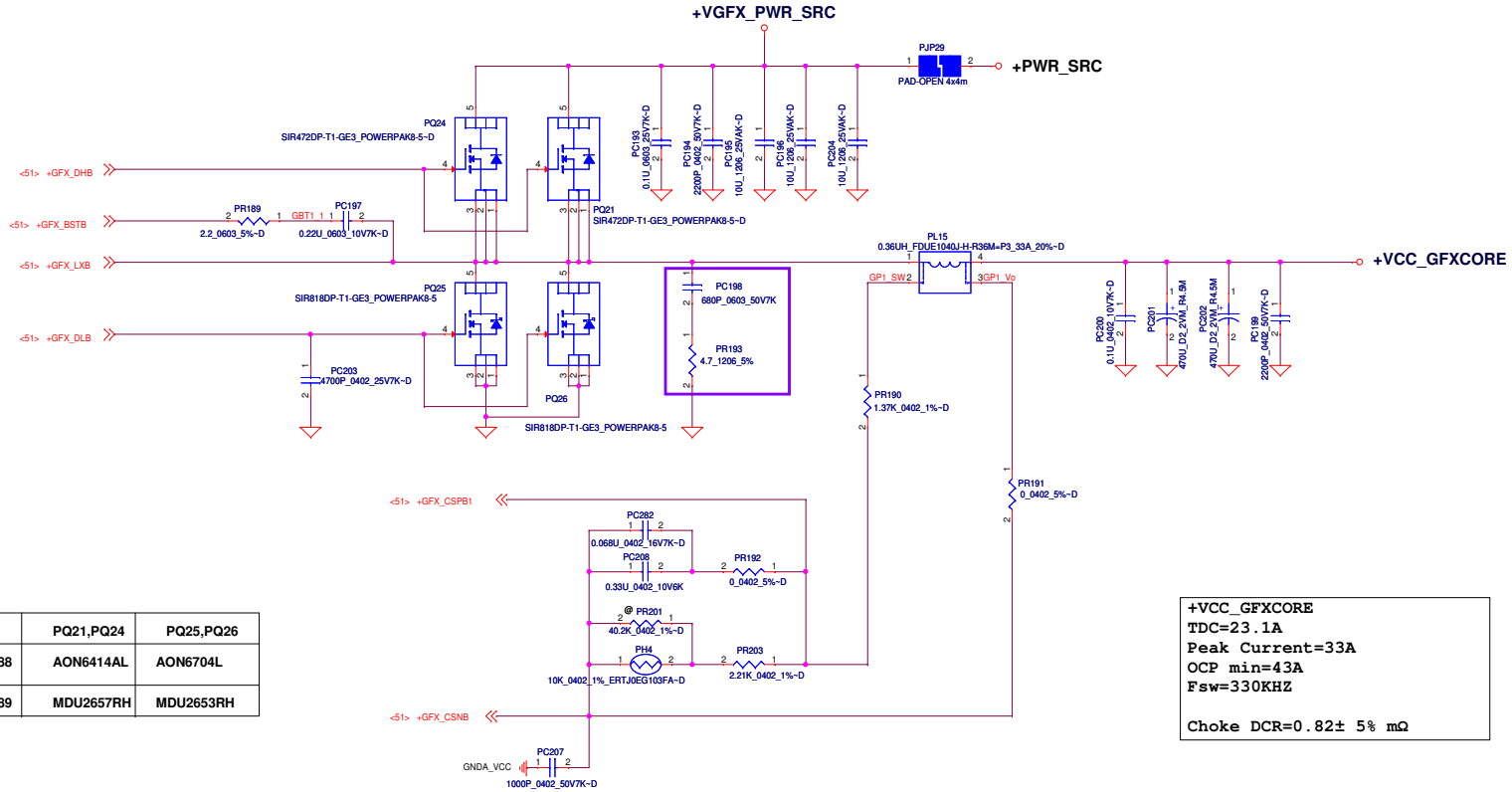
+VCC_GFXCORE



		PQ21,PQ24	PQ25,PQ26
Main	X7629631L88	AON6414AL	AON6704L
2nd	X7629631L89	MDU2657RH	MDU2653RH

```
+VCC_GFXCORE
TDC=23.1A
Peak Current=33A
OCP min=43A
Fsw=330KHZ

Choke DCR=0.82± 5% mΩ
```


Compal Electronics, Inc.

Title: ISL95870A +1.05V_RUN_VTT

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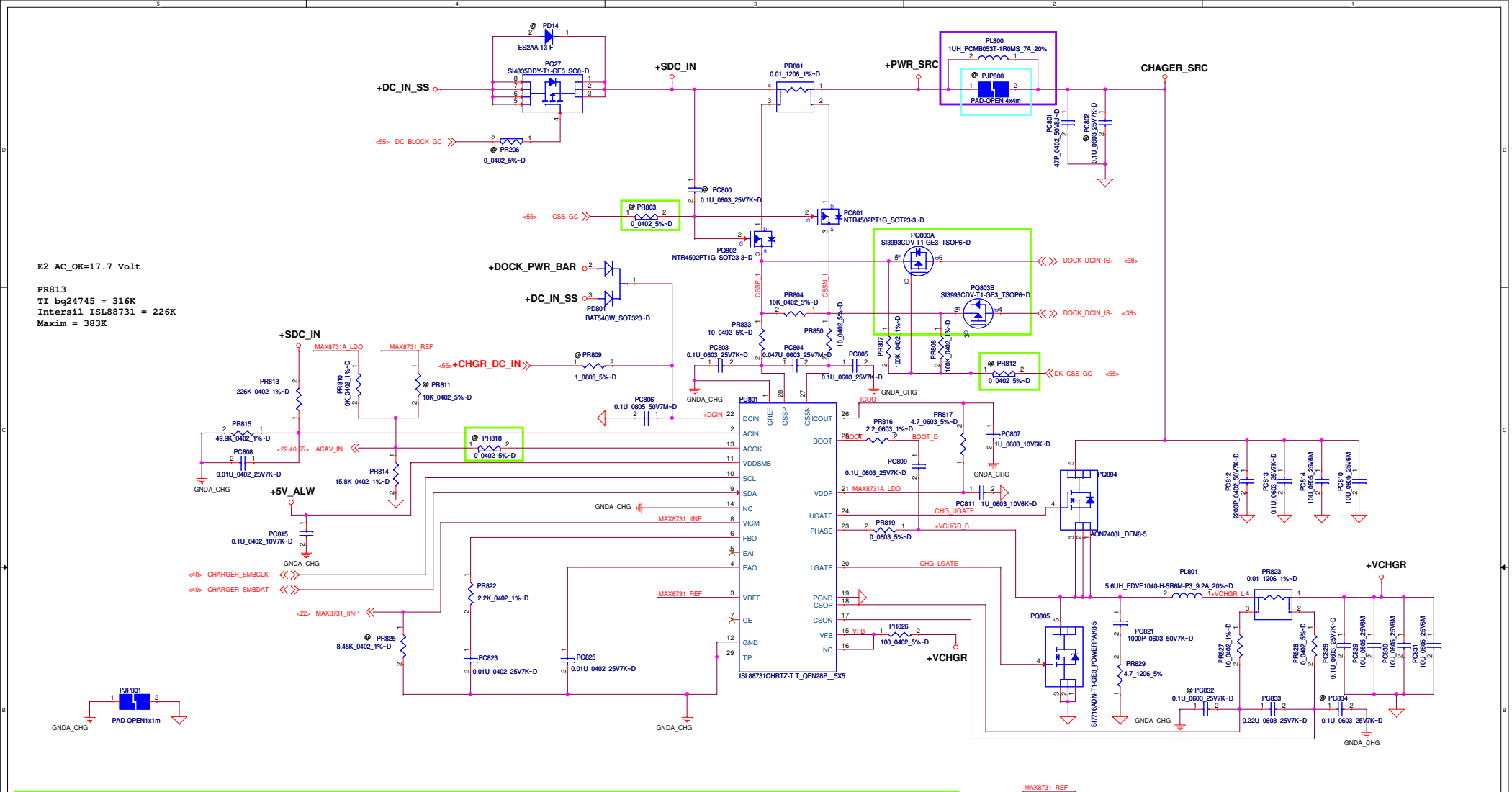
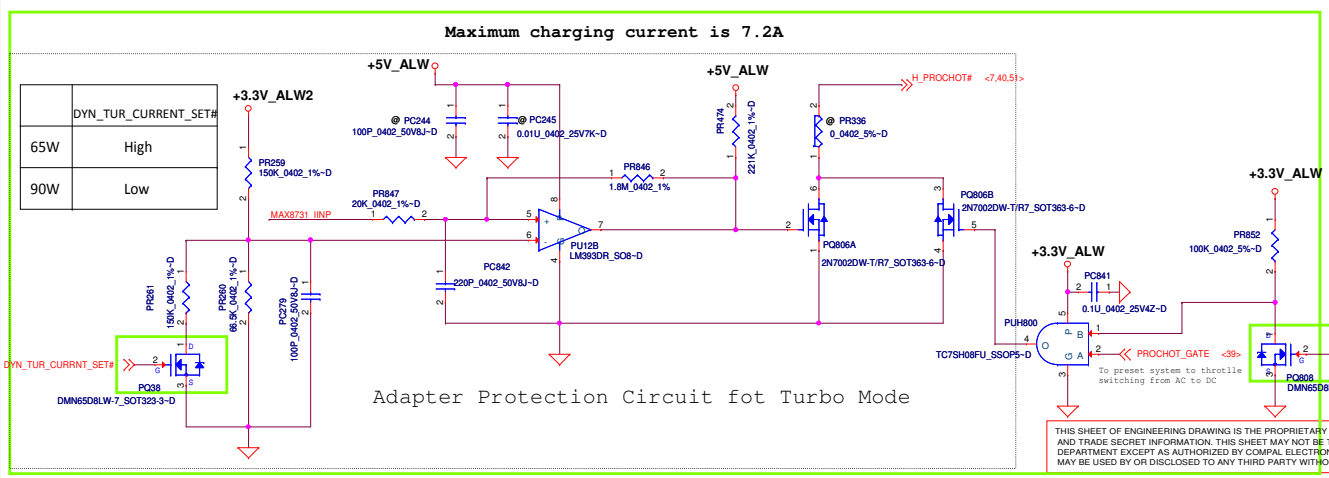
E2 AC_OK=17.7 Volt

PR813
TI bq24745 = 316K
Intersil ISL88731 = 226K
Maxim = 383K





	DYN_TUR_CURRENT_SET#
65W	High
90W	Low

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Compal Electronics, Inc.		
Title: Charger		
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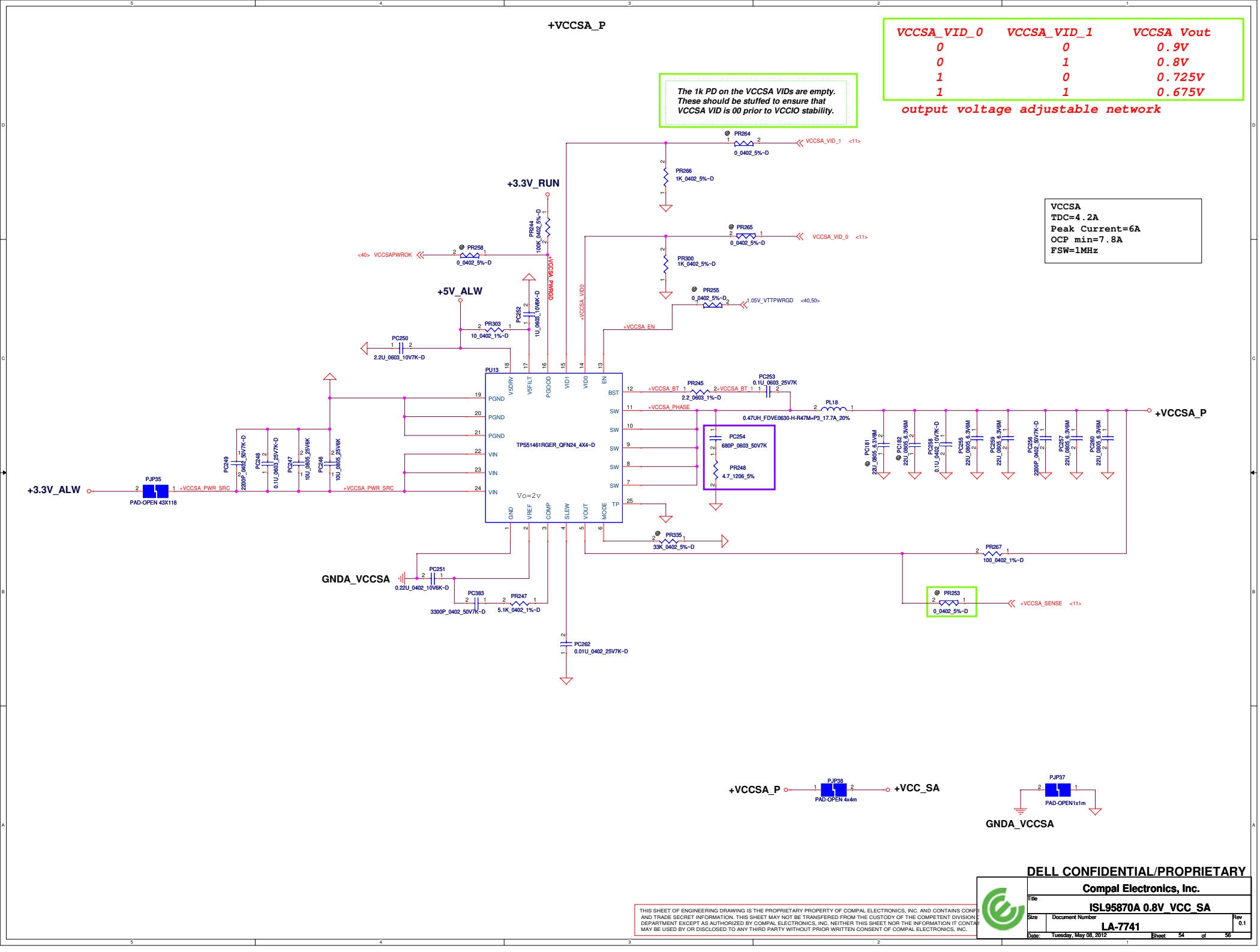

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Compal Electronics, Inc.	
Title	ISL95870A 0.8V_VCC_SA
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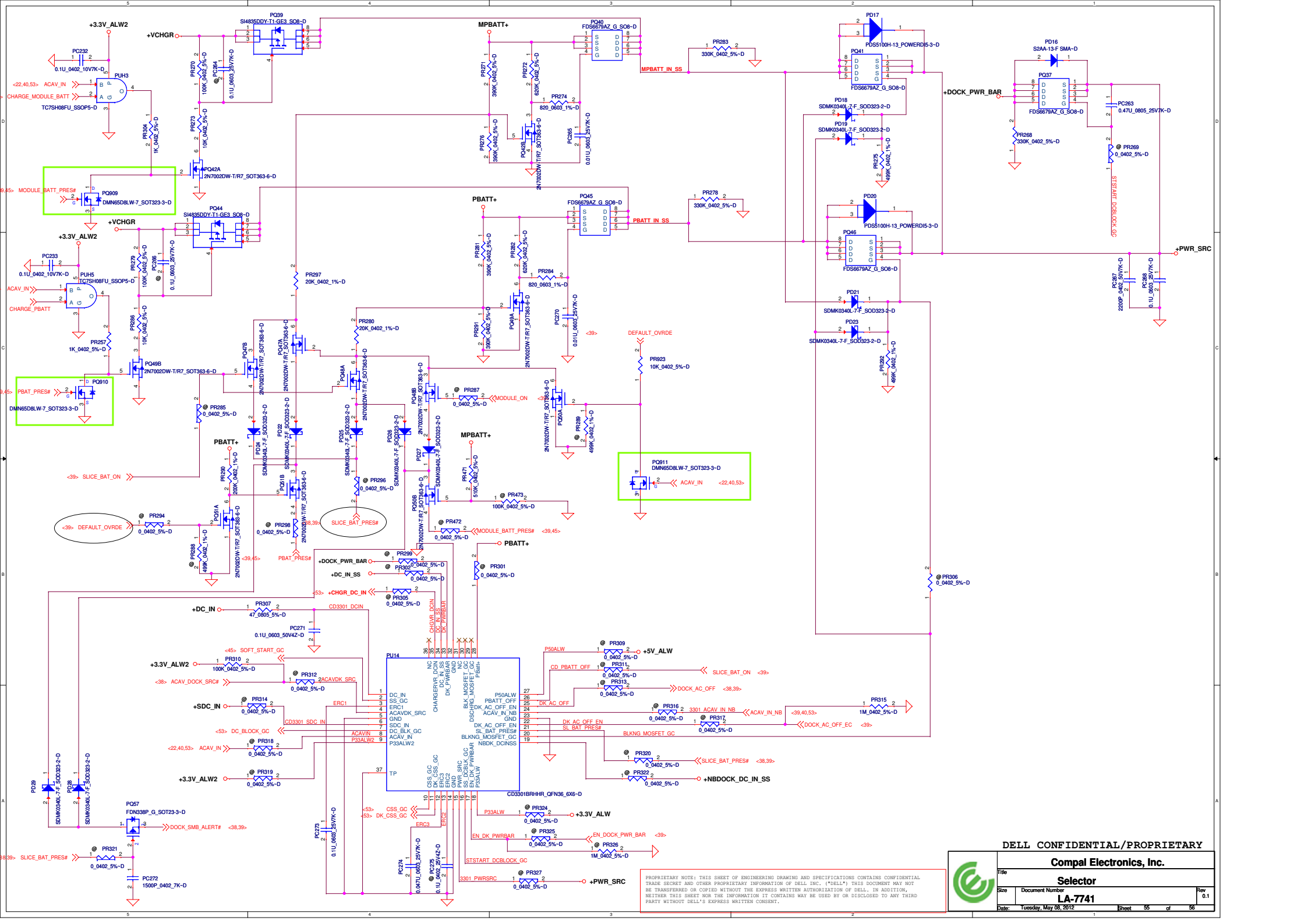

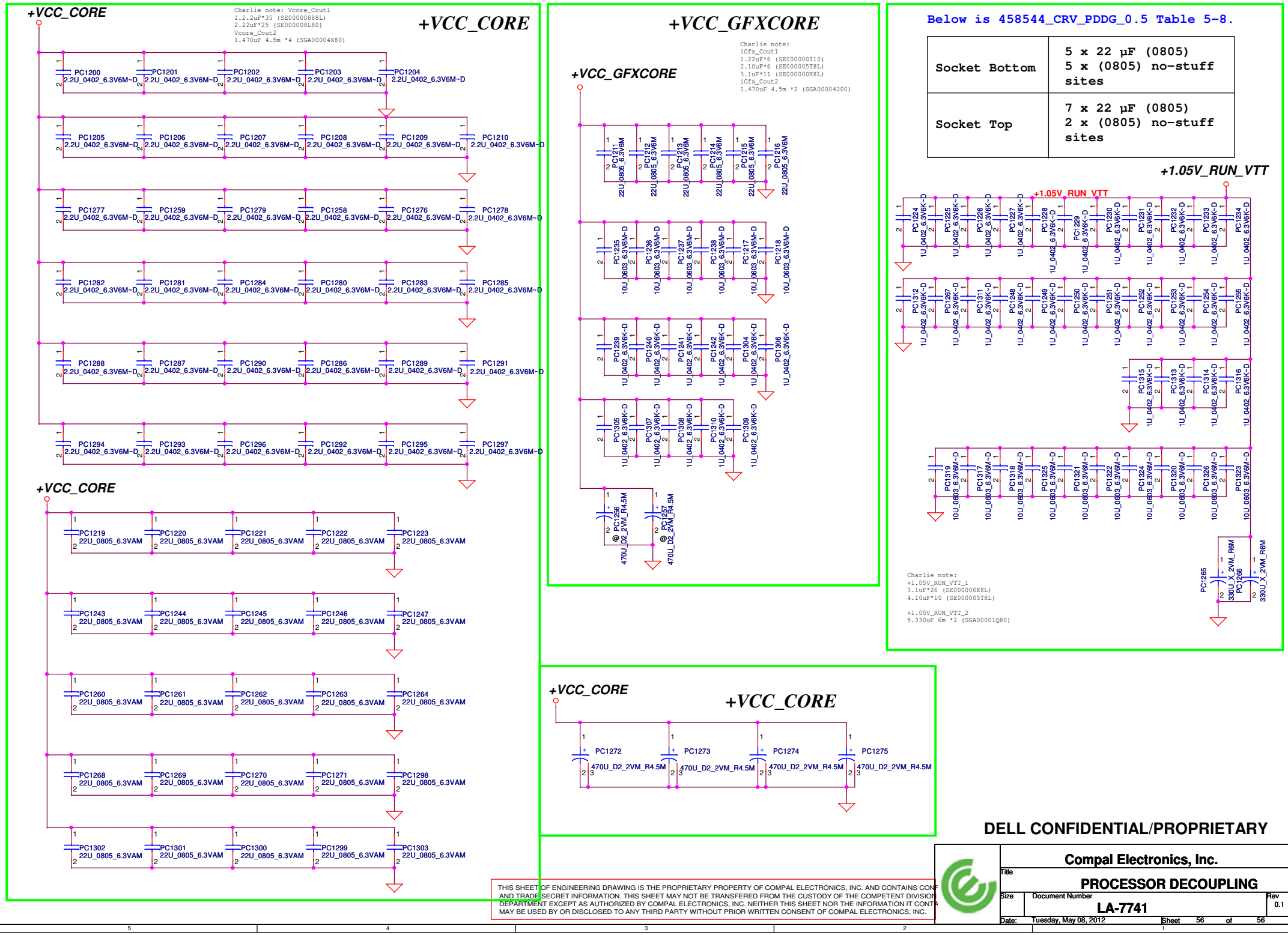

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	51	VCORE_MAX17511	2011/08/02	Maxim	CPU Load line modify	PR140 change from 9.76K_ohm(P/N :SD03497618L) to 8.66K_ohm (P/N : SD03486618L)	X01
2	51	+VCC_GFXCORE	2011/08/02	Maxim	GFX Load line modify	PR157 change from 8.45K_ohm(P/N :SD00000068L) to 7.5K_ohm (P/N : SD03475018L)	X01
3	45	DCIN	2011/08/04	DELL	ME design change	PJPDC1 change from 7pin(P/N :SP02000NQ0L) (MOLEX_87438-0743_7P) to 5pin(P/N :SP02000YD00)(ACES_50299-00501-003_5P)	X01
4	46 49	+5V_ALWP/ +3.3V_ALWP +1.05V_MP	2011/08/04	Compal	COS concern, change from D2 Polymer cap to OScon cap	+5V_ALWP/ +3.3V_ALWP portion : PC35,PC40 change from 220u_6.3V_ESR25 polymer cap(P/N: SGA00002M00) to 220u_6.3V_ESR17 OScon cap(P/N: SF000002Y00) (H=4.2) +1.05V_MP portion : PC430 change from 220u_4V_ESR15 polymer cap(P/N: SGA00000Y0L) to 220u_6.3V_ESR17 OScon cap(P/N: SF000002Y00) (H=4.2)	X01
5	47	+1.5V_MEN_P	2011/08/04	DELL	Follow VC , enable use SIO_SLP_S4#.	1. Un-pop PR487, 2. Add PR210 for net "SIO_SLP_S4#"	X01
6	46	+5V_ALWP/ +3.3V_ALWP	2011/08/05	DELL	Main and 2nd IC common setting	Un-pop PD37,PR46,PR47	X01
7	48	+1.8V_RUN	2011/08/05	Compal	follow E4-12"14"15" schematic	Add PC307 0.1U_0603_25V (P/N: SE042104K8L)	X01
8	51 53	VCORE_MAX17511 Charger	2011/08/09	Compal	EMI request	Add PL14(P/N: SM01000DJ00)(S SUPPRE_ FBMA-L11-453215-121LMA90T 1812) and un-pop PJP27 Pop PL800(P/N: SH00000NW00) (S COIL 1UH +-20% PCMB053T-1R0MS 7A)and un-pop PJP27	X01
9	45	DCIN	2011/08/17	Compal - Kuo.Richard	ESD solution	1. Pop PD2 and PD3 (P/N: SCA00000R0L) for PBATT2 2. Pop PD6 and PD7 (P/N: SCA00000R0L) for PBATT1	X01
10	46	+5V_ALWP/ +3.3V_ALWP	2011/08/17	Compal - Ling. Carol	RF solution	1. Add PC29, PC30(P/N: SE00000G88L) (S CER CAP 0.1U 25V K X5R 0402) bypass cap. at +5V_ALWP output jumper- PJP74 and +3.3V_ALWP output jumper- PJP10 2. for +5V_ALWP : Pop PR40 (P/N: SD001470B80) (S RES 1/4W 4.7 +-5% 1206), PC33 (P/N: SE025681K80) (S CER CAP 680P 50V K X7R 0603) 3. for +3.3V_ALWP : Pop PR39 (P/N: SD001470B80) (S RES 1/4W 4.7 +-5% 1206), PC34 (P/N: SE025681K80) (S CER CAP 680P 50V K X7R 0603)	X01

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11	47	+1.5V_MEN_P	2011/08/17	Compal - Ling. Carol	RF solution	for 1.5V_MEN_P: Pop PR220 (P/N: SD001470B80) (S RES 1/4W 4.7 +-5% 1206), PC231 (P/N: SE025681K80) (S CER CAP 680P 50V K X7R 0603)	X01
	49	+1.05V_MP				for +1.05V_MP: Pop PR404 (P/N: SD001470B80) (S RES 1/4W 4.7 +-5% 1206), PC432 (P/N: SE025681K80) (S CER CAP 680P 50V K X7R 0603)	
	51	+VCC_CORE				for +VCC_CORE: Pop PR117 (P/N: SD001470B80) (S RES 1/4W 4.7 +-5% 1206), PC139 (P/N: SE025681K80) (S CER CAP 680P 50V K X7R 0603) Pop PR148 (P/N: SD001470B80) (S RES 1/4W 4.7 +-5% 1206), PC159 (P/N: SE025681K80) (S CER CAP 680P 50V K X7R 0603) Pop PR173 (P/N: SD001470B80) (S RES 1/4W 4.7 +-5% 1206), PC175 (P/N: SE025681K80) (S CER CAP 680P 50V K X7R 0603)	
	52	+VCC_GFXCORE				for +VCC_GFXCORE: Pop PR193 (P/N: SD001470B80) (S RES 1/4W 4.7 +-5% 1206), PC198 (P/N: SE025681K80) (S CER CAP 680P 50V K X7R 0603)	
	54	+VCCSA_P				for +VCCSA_P: Pop PR248 (P/N: SD001470B80) (S RES 1/4W 4.7 +-5% 1206), PC254 (P/N: SE025681K80) (S CER CAP 680P 50V K X7R 0603)	
12	45	DCIN	2011/10/17	Compal	Reduce power consumption in S5.	Add net "PCH_ALW_ON" with PR28 (0 ohm) for +PWR_SRC_S enable signal. then un-pop PR901	X02
13	55	Selector	2011/11/07	Compal	Thailand flood impacted materials - Vendoe (ROHM)	Change PD18,PD19,PD21,PD22,PD23,PD24,PD25,PD26,PD27,PD28,PD29 from SCS00005T0L(S SCH DIO RB751VM-40TE-17 SOD-323) to SCS0340L01L (S SCH DIO SDMK0340L-7-F SOD-323)	X02
14	53	Charger	2011/12/06	Compal	Vendor inform material will EOL	Change PQ803A and PQ803B from SB00000CL0L (S TR NTGD4161PT1G 2P TSOP6) to SB00000E100 (S TR SI3993CDV-T1-GE3 2P TSOP6)	X02
15	53 55	Charger Selector	2011/12/06	Compal	Without ESD protected	Change PQ38,PQ808,PQ909,PQ910,PQ911 from SB57002040L (S TR 2N7002W-7-F 1N SOT323 DII) to SB00000UO00 (S TR DMN65D8LW-7 1N SOT323-3)	X02
16	45	DCIN	2011/12/06	Compal - Kuo.Richard	ESD test currently is pass	Del PD2, PD3, PD6 and PD7 (P/N: SCA00000R0L)	X02
17	48	+1.8V_RUN	2011/12/22	Compal	follow E4-12"14"15" schematic	Change PL26 from SH00000MN00 (S COIL 1UH +-20% PH041H-1R0MS 3.8A) CYNTEC to SH00000MW00 (S COIL 1UH +-30% NRS4018T1R0NDGJ 3.2A) Taiyo	X02

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18	45	DCIN	2012/02/22	Compal - YuHeng_Hsieh	ESD solution	Add @ PD8	X03

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1	42	HW	08/16/2011	COMPAL	E4 uses SIO_SLP_S4# for power control	DDR_ON and SUS_ON are replaced by SIO_SLP_S4#	X01
2	14,39	HW	08/16/2011	COMPAL	SMSC request to delete LPC_LDRQ0#	Leave LDRQ0# no connection on both of 5048 and PCH side	X01
3	22	HW	08/16/2011	COMPAL	UMA uses EMC4021 for cost concern	Change thermal sensor to EMC4021 for UMA	X01
4	42	HW	08/16/2011	COMPAL	Load SW sources output rising time mismatch and COS. cost concern	Change back to E3 +3.3V/5V_RUN discrete solution	X01
5	29	HW	08/16/2011	COMPAL	Codec is change to 92HD93	Pop R162~R166 and de-pop U73	X01
6	20,42	HW	08/16/2011	COMPAL	Vgs less than cut-in voltage in battery mode	Add control circuit for +5V_ALW_PCH	X01
7	27,28,42	HW	08/16/2011	COMPAL	Vgs of 5V MOS maybe large than max rating	Add R516, R517. Change Q55 from SB00000KQ0L to SB00000GV00	X01
8	11	HW	08/16/2011	COMPAL	Follow INTEL PDDG 0.8	De-pop RC140	X01
9	32	HW	08/16/2011	COMPAL	RESET_OUT# power sequence issue	Add R1640, 1M ohms pull down for USH_PWR_STATE# at M/B side	X01
10	40	HW	08/16/2011	COMPAL	Change board ID to X01	Change R875 to 130Kohms	X01
11	34	HW	08/16/2011	COMPAL	PCH GPIO52 need 8.2~10K pull up +3.3VS	Change R695 from 100K to 10Kohms	X01
12	23	HW	08/16/2011	COMPAL	CRT SW 2nd source TI, TS3V713 pin29 is VDD	Connect pin29 to +3.3V_RUN	X01
13	15	HW	08/16/2011	COMPAL	Follow crystal measurement report	Change C741 and C741to 39pF CH18 CH19 to 8.2pF CH2 to 18pF	X01
14	16	HW	08/16/2011	COMPAL	+1.05V_M turn off before APWROK de-assert	Add UH5 circuit for HW solution	X01
15	29	HW	08/16/2011	COMPAL	Co-lay 92HD93 with ALC290	Pop option for 92HD93/ALC290=>R1646/C1164; R1644/R1643; C965/R1642 Reserve for ALC290 only: C1204, C1205, R171, R1647, C1165, R1648 Reserve for 92HD93 only: R1645, C963	X01
16	41	HW	08/16/2011	COMPAL	Reset IC threshold voltage issue	Change U4 to RT9801A (threshold adjustable)	X01
17	26	HW	08/16/2011	COMPAL	DPX_CA_DET voltage too low through dongle	Change U21 and U24 to SA000055G0L	X01
18	17	HW	08/16/2011	COMPAL	Request from INTEL review feedback	Pop RH332 for PCH_GPIO3	X01
19	42,43	HW	08/16/2011	COMPAL	For cost saving	Change Q61 to SB00000GV00; HDD and breath LED control share Q84; Power team request Q59 change to SB00000L80L	X01
20	41	HW	08/16/2011	COMPAL	For RSMRST# debug	Reserve R1655 and pop R1623	X01
21	43	HW	08/16/2011	COMPAL	White light LED brightness is abnormal	Change R934, R938, R939, R949, R958, R957 and R955 to 2.2 Kohms	X01
22	18	HW	08/16/2011	COMPAL	Follow GPIO MAP	Add RH264 pull high for EXPRCRD_DET#	X01

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23	11	HW	08/16/2011	COMPAL	DF488976:S3 can't resume issue	Control 1.5V_VDDQ by EC. Pop RC79 and de-pop RC82	X01
24	18	HW	08/16/2011	COMPAL	Delete TCM and Non-TPM configuration	De-pop RH270 and RH271. Always pop RH267 and RH268	X01
25	23,33	HW	08/16/2011	COMPAL	EMI request to add solution	Reserve C1207 for DMIC_CLK;CE758 for SD/MMCCLK Change R676 to 22ohm	X01
26	29	HW	08/16/2011	COMPAL	EMI request to add solution	pop C981~C983 0.1uF	X01
27	36	HW	08/22/2011	COMPAL	DF499184 Right side USB3 port performance poor	Change C410~C417 from 0.01uF to 0.1uF	X01
28	15,17	HW	08/22/2011	COMPAL	RF request to add RF noise solution	Pop CH107~CH110,CH112,CH113 8.2pF	X01
29	25	HW	08/23/2011	COMPAL	DF494588:HDMI EMI fail	add C1208~C1215 3.3pF	X01
30	19	HW	08/24/2011	COMPAL	CRT ripple iisue	Change LH1 to SHI00007W0L	X01
~~31~~	~~40~~	~~HW~~	~~08/26/2011~~	~~COMPAL~~	~~SMSC review feedback~~	~~Reserve R933 R896~~	~~X01~~
32	43	HW	08/29/2011	COMPAL	Follow LED spec	Change R949, R958, R957, R955, R939, R938, R934 to 1.2K	X01
33	42	HW	08/29/2011	COMPAL	Follow 14 15	depop R1627	X01
34	25	HW	08/30/2011	COMPAL	DF494588 HDMI EMI issue	depop L19~L22 pop R451,R459 R462 R466 R468~R471 SHI0000EE0L	X01
35	25	HW	10/25/2011	COMPAL	DF494588 HDMI EMI issue	change R451,R459 R462 R466 R468~R471 to L100~L107 SHI0000ES0L 12nH	0.3(X01)
36	14	HW	10/25/2011	COMPAL	Follow crystal measurement report	change CH2 to 15pF	0.3(X01)
~~37~~	~~22~~	~~HW~~	~~10/25/2011~~	~~COMPAL~~	~~Thermal team request change OTP to 96 deg~~	~~change R406 to 1.58k~~	~~0.3(X01)~~
38		HW	11/21/2011	COMPAL	Change RC value at Gate of MOS Load SW to modify power rail soft start timing	RC72 from 100K to 330K; RC143 form 330K to 1M; CC136 form 0.1u to 0.022u R412 from 100K to 470K; R1632 form 1M to 4.7M; C293 form 0.1u to 0.022u R507 from 100K to 470K; R517 form 1M to 4.7M; C400 form 0.1u to 0.022u R722 from 100K to 470K; R1625 form 1M to 4.7M; C644 form 4700p to 220p R729 from 100K to 470K; R1628 form 1M to 4.7M; C650 form 4700p to 220p R917 from 100K to 470K; R1617 form 1M to 4.7M; C770 form 4700p to 220p R920 from 100K to 470K; R1610 form 470K to 2.2M; C771 form 4700p to 470p R930 from 100K to 330K; R1611 form 470K to 1M; C773 form 2200p to 100p R906 from 100K to 470K; C763 form 2200p to 220p R912 from 100K to 470K; C766 form 470p to 220p	0.3(X01)
39	40	HW	11/21/2011	COMPAL	SMSC review feedback	Add R933 and R896 100Kohms to GND for I2S disabled	0.3(X01)
40	29	HW	11/21/2011	COMPAL	Remove ALC290 co-lay circuit	Remove R1648, R1647, R1646, R1645, C1165, C1164, R1643, R1644, R1642, R171, C1204, C1205	0.3(X01)
41	29	HW	11/21/2011	COMPAL	15" UMA speaker no sound issue	Add snubber on speaker trace with C973~C976: 2200pF(SE074222K8L.) and R1658~R1661: 3.3ohms(0402). Change bead rated current from 200mA to 2A.	0.3(X01)

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42	33	HW	11/21/2011	COMPAL	EMI request to change SD CLK series R	R676 is changed from 33ohms to 10ohms	0.3(X01)
~~43~~	~~42~~	~~HW~~	~~11/21/2011~~	~~COMPAL~~	~~1V leakage on +3.3V_RUN during system boot~~	~~Pop Q69 and R929 discharge circuit~~	~~0.3(X01)~~
44	40	HW	11/21/2011	COMPAL	EC has internal pull up for volume signals	De-pop R1169, R1197 and R1118	0.3(X01)
45	41	HW	11/21/2011	COMPAL	Chane reset IC to RT9818A-44GU3	Update U4 symbol and add R1629 for backup of inrush prevention. Change RSMRST# pull up with 100Koms. Pop R1655 and de-pop R1623.	0.3(X01)
46	39	HW	11/21/2011	COMPAL	When suspend/resume cycles, wireless SW GPIO IRQs keeps giving	Add R787 pulling up to +3.3V_ALW for WIRELESS_ON#/OFF and de-pop R766	0.3(X01)
47	19	HW	11/21/2011	COMPAL	CRT ripple garbage display issue	Change CH36 from 10uF to 22uF	0.3(X01)
48	7~42	HW	11/21/2011	COMPAL	For cost saving	Change 0 ohm resistor to short pad	0.3(X01)
49	42	HW	11/21/2011	COMPAL	+3.3V_SUS sequence timing probelm	Change C767 to 470pF	0.3(X01)
50	32	HW	11/21/2011	COMPAL	TPM is changed to AT97SC3204-X2A18-AB	U39(TPM) is changed to SA00004WQ10(AT97SC3204-X2A18-AB) for WIN8 support	0.3(X01)
51	34	HW	11/21/2011	COMPAL	PCH GPIO52 changed to be free	De-pop R725, remove R695 and add RH359	0.3(X01)
52	11,42	HW	11/21/2011	COMPAL	AO4728L leakage issue	Change QC3 and Q59 to AO4304L (SB00000RV00)	0.3(X01)
53	32	HW	11/21/2011	COMPAL	+3.3V_RUN Giltch when AC plugin	Add D87, R1662 and R1663 (pull high to +3.3V_RUN) for HW solution backup	0.3(X01)
54	11	HW	11/21/2011	COMPAL	Change 1Kohms tolerance for cost saving	Change 1Kohms +-1% to +-5% except RC78,RC84	0.3(X01)
55	38	HW	11/21/2011	COMPAL	EMI request to add 33ohms for DP port	Add RE7,RE8,RE13~RE26 for DP portD and portC	0.3(X01)
56	22	HW	11/25/2011	COMPAL	Thermal team request change OTP to 94 deg for SNB, 96 deg for IVB	R406 =1.4K for SNB, add R1664=1.58K for IVB	0.3(X01)
57	38	HW	11/25/2011	COMPAL	EMI request to add common choke for docking USB port8	Add L53(@),R745,R746	0.3(X01)
58	34 , 38	HW	12/01/2011	COMPAL	For Dock USB Port8 EMI issue	Swap USB port6 & port8	0.3(X01)
59	23	HW	12/01/2011	COMPAL	For solve Camera USB EMI issue	Pop L10 (180ohm) ,depop R427,R428	0.3(X01)
60	7	HW	12/02/2011	COMPAL	For ESD request	Remove 0 ohm short pad at location RC129,RC25,RC23,RC24,RC26,RH106,RH107	0.3(X01)
61	35	HW	12/02/2011	COMPAL	For ESD request	Reserve CE10, CE11 and CE12 for EXP PWR SW signals, CPUSB#, EXPRCRD_CPPE# and CARD_RESET#	0.3(X01)
62	36	HW	12/02/2011	COMPAL	For cost down plan	Change USB PWR SW(U49) from TI2560 to GMT517	0.3(X01)
63	31	HW	12/02/2011	COMPAL	Change RC value at Gate of MOS Load SW to modify power rail soft start timing	R1638 from 470K to 1M	

X01

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64	36	HW	12/21/2011	COMPAL	For ESD request	D78,D79 change from SC30000250L to SC300002F0L , and pin8 connect to GND	X02
65	14~21	HW	12/21/2011	COMPAL	PCH use QS sample at ST	UH4 change to SA00005BU1L	X02
66	40	HW	12/21/2011	COMPAL	Change board ID to X02	Change R875 to 62Kohms	X02
67	43	HW	12/21/2011	COMPAL	Change current limit resistors of LED	Change R957 to 150ohms , R934 to 2.2kohm, R949 to 1.8kohm,R951 to 2Kohm,R939 to 3.3kohm,R955 to 820 ohm,R938 to 820 ohm,R958 to 560 ohm, R959 to 1.2kohm	X02
68	42	HW	12/21/2011	COMPAL	follow 14" schematic	Q55,Q61 change to SB00000GV00	X02
69	41	HW	12/28/2011	COMPAL	To prevent inrush current at reset IC input	Add R1635(33ohm) for backup of inrush prevention	X02
70	42	HW	12/28/2011	COMPAL	+3.3V_SUS sequence timing	R911 from 100K to 470K; R1618 from 1M to 4.7M; C767 from 470p to 220p	X02
71	23 ,30	HW	01/03/2012	COMPAL	For EMI request	Add C303,C304,C1001,C1003,C1004 820pF	X02
72	43	HW	01/03/2012	COMPAL	For EMI request	Add and reserve C306(@)	X02
73	43	HW	01/06/2012	COMPAL	Change current limit resistors of LED	R949 from 1.8k ohm to 3k ohm	X02
74	36	HW	02/20/2012	COMPAL	Add pop option resistor for USB3.0 repeater	Add R764,R788,R792,R801,R806,R808 location and change main source to SA000056E0L(Pericom)	A00
75	28	HW	02/20/2012	COMPAL	Parade PS8520 pin can't connect to 3.3V for avoid the leakage voltage issue.	Add R1182 for SATA repeater pop option	A00
76	40	HW	02/20/2012	COMPAL	Change board ID to A00	Change R875 to 33Kohms	A00
77	40	HW	02/20/2012	COMPAL	Change MEC5055 P/N for MP	Change U51 P/N to SA00003TZ2L	A00
78	14-21,31	HW	02/20/2012	COMPAL	Chnage PCH, LAN chip P/N for X-build	UH4 is changed to SA00005BU3L U31 is changed to SA00003SI5L	A00
79	38	HW	02/20/2012	COMPAL	System hangs after hot dock (DF531758)	Change R755 from 100Kohms to 10Kohms	A00
80	32	HW	02/20/2012	COMPAL	Add BOM config for Non-TPM	Add 1@ for TPM and 2@ for Non-TPM config	A00
81	14	HW	02/20/2012	COMPAL	De-pop resistor on PCH JTAG for power saving	De-pop RH288, RH47, RH48 and RH49	A00
82	36	HW	02/20/2012	COMPAL	Samsung cell phone can't support CDP	Change U2 to Seligo SA00004VH00, Change charging mode to SDP only in S0 ,reserve Q126(@)	A00
83	34	HW	02/20/2012	COMPAL	E4 no support WWAN SMBUS function .	Not stuff R1157 and R1158.	A00
84		HW	02/20/2012	COMPAL	For cost saving	Change 0 ohm resistor to short pad,except R1174,R1176,R1177,R1181,R1633,R495,R496,R743, R1595,R745,R746,R935,R940,R941,R942,R1163,R1164	A00
85	28	HW	03/03/2012	COMPAL	For Parade ODD repeater detect issue	Add R1814(8.2K) to PD for Parade , and reserve R1182 to PH for other repeater	A00

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86	37	HW	03/03/2012	COMPAL	Add pop option resistor for eSATA repeater	Add R1185,R749,R747	A00
87	36	HW	03/05/2012	COMPAL	System will reconnect USB 3.0 after resume from S3 issue.[BITS:DF537410].	Reserve R1636 to +3.3V_ALW_PCH, and add R1637 to +3.3V_RUN	A00
88	33	HW	03/09/2012	COMPAL	Due to ESD has an SD card lost issue	add CE13 47nF capacitor for PLTRST_MMI# on U38 side	A00
89	35	HW	03/13/2012	COMPAL	For ESD request	Pop CE10 ,CE11 ,CE12(0.1uF) ,& add CE14 (100pF)	A00
90	36	HW	04/02/2012	COMPAL	For Parade PS8713 repeater setting	Change R571 to SD03449910L (S RES 1/16W 4.99K +-1% 0402)	A00