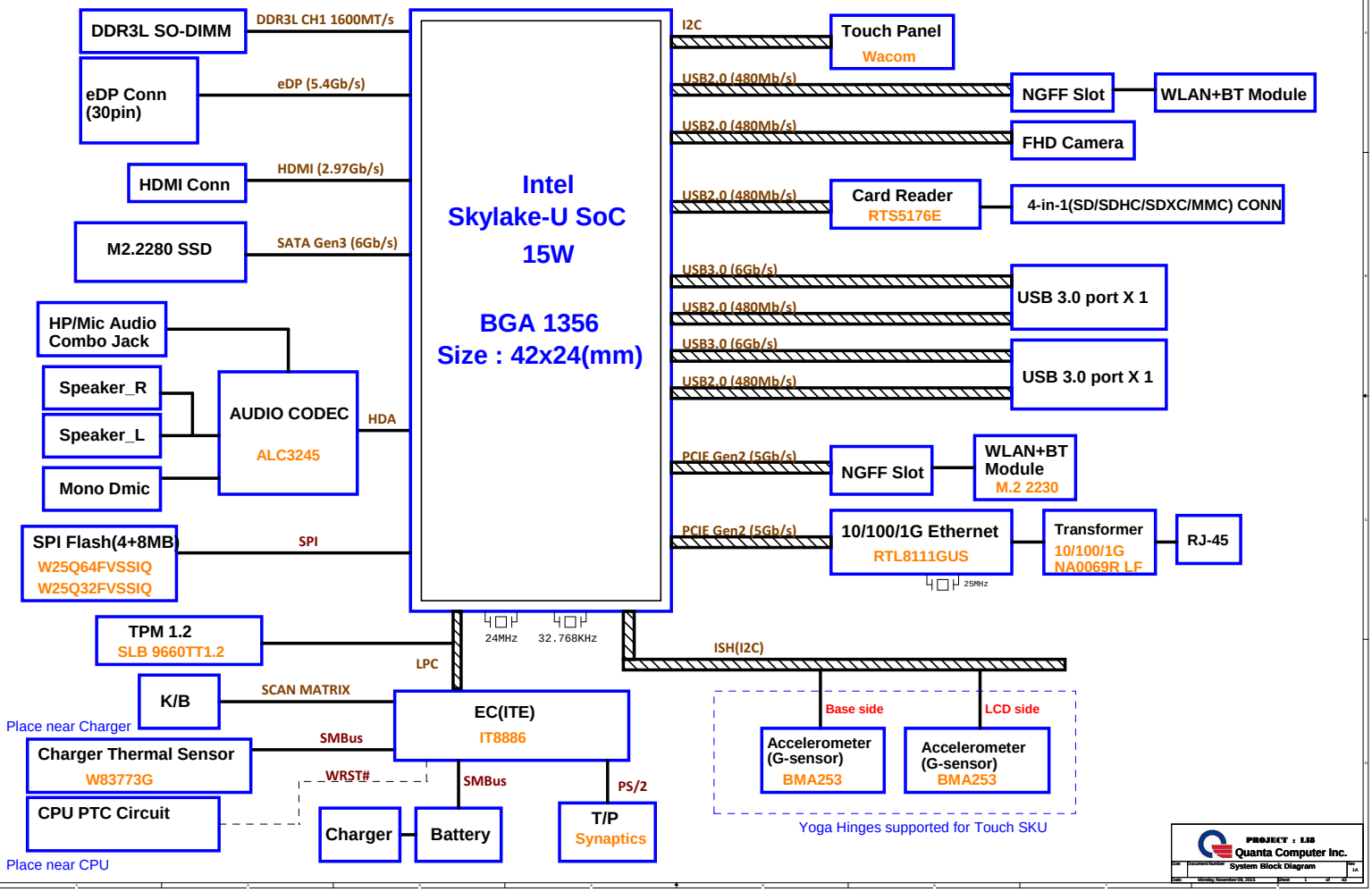
Newton Intel Skylake-U Platform UMA Block Diagram (Windows)



+3V (4,10,11,12,13,14,15,16,17,18,19,20,21,22,23,25,26,27,28,29,30,32,34,38,40)
+1.0V (4,6,16,26,40)
+VCCIO (6,16,40,43)
+VCCSTPLL (4,5,6,9,34,40)

HDMI

(19) IN_D2# → IN_D2# → E55 DDI1_TXN[0]
(19) IN_D2 → IN_D2 → F55 DDI1_TXP[0]
(19) IN_D1# → IN_D1# → E58 DDI1_TXN[1]
(19) IN_D1 → IN_D1 → F58 DDI1_TXP[1]
(19) IN_D0# → IN_D0# → F53 DDI1_TXN[2]
(19) IN_D0 → IN_D0 → G53 DDI1_TXP[2]
(19) IN_CLK# → IN_CLK# → F56 DDI1_TXN[3]
(19) IN_CLK → IN_CLK → G56 DDI1_TXP[3]

C50 DDI2_TXN[0]
D50 DDI2_TXP[0]
C52 DDI2_TXN[1]
D52 DDI2_TXP[1]
A50 DDI2_TXN[2]
B50 DDI2_TXP[2]
D51 DDI2_TXN[3]
C51 DDI2_TXP[3]

U23A SKL_ULT ? **Need apply PN**

DDI → DISPLAY SIDEBANDS

EDP_TXN[0] C47 INT_EDP_TXN0 → INT_EDP_TXN0 (18)
EDP_TXP[0] C46 INT_EDP_TXP0 → INT_EDP_TXP0 (18)
EDP_TXN[1] D46
EDP_TXP[1] C45
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP_AUXN E45 INT_EDP_AUXN → INT_EDP_AUXN (18)
EDP_AUXP F45 INT_EDP_AUXP → INT_EDP_AUXP (18)

EDP_DISP_UTIL B52 EDP_DISP_UTIL → TP35

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48
DDI2_AUXP F48
DDI3_AUXN E46
DDI3_AUXP F46

GPP_E13/DDPB_HPD0
GPP_E14/DDPC_HPD1
GPP_E15/DDPD_HPD2
GPP_E16/DDPE_HPD3
GPP_E17/EDP_HPD
L9 PCH_HDMI_HPD → PCH_HDMI_HPD (19)
L7
L6
N9
L10 EDP_HPD → EDP_HPD (18)

EDP_BKLTEN R12 PCH_LVDS_BLON → PCH_LVDS_BLON (18)
EDP_BKLTCTL R11 PCH_DPST_PWM → PCH_DPST_PWM (18)
EDP_VDDEN U13 PCH_LCDVCC_EN → PCH_LCDVCC_EN (18)

(19) HDMI_SCL → L13 GPP_E18/DDPB_CTRLCLK
(19) HDMI_SDA → L12 GPP_E19/DDPB_CTRLDATA

TP1 DDPC_CTRLDATA → N7 GPP_E20/DDPC_CTRLCLK
N8 GPP_E21/DDPC_CTRLDATA

TP2 DDPD_CTRLDATA → N11 GPP_E22/DDPD_CTRLCLK
N12 GPP_E23/DDPD_CTRLDATA

+VCCIO R71 24.9/F_4 EDP_RCOMP → E52 EDP_RCOMP

SKL_ULT
REV = 1
1 OF 20

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

+3V
R397 10K_4
EDP_HPD
R394 100K_4

U23D SKL_ULT ? **Need apply PN**

CATERR# D63
EC_PECI A64
PROCHOT# C65
THERMTRIP# C63
SKTOCC# A65

CPU MISC
BPM#[0] C55
BPM#[1] D55
BPM#[2] B54
BPM#[3] C56

GPP_E3/CPU_GP0 A6
GPP_E7/CPU_GP1 A7
GPP_B3/CPU_GP2 BA5
GPP_B4/CPU_GP3 AY5

PROC_POPIRCOMP AT16
PCH_OPIRCOMP AU16
OPCE_RCOMP H66
OPC_RCOMP H65

JTAG
PROC_TCK B61 XDP_TCK0 → XDP_TCK0 (16)
PROC_TDI D60 XDP_TDI_CPU → XDP_TDI_CPU (16)
PROC_TDO A61 XDP_TDO_CPU → XDP_TDO_CPU (16)
PROC_TMS C60 XDP_TMS_CPU → XDP_TMS_CPU (16)
PROC_TRST# B59 XDP_TRST#_CPU → XDP_TRST#_CPU (2,16)

PCH_JTAG_TCK B56 JTAG_TCK_PCH → JTAG_TCK_PCH (16)
PCH_JTAG_TDI D59 JTAG_TDI_PCH → JTAG_TDI_PCH (16)
PCH_JTAG_TDO A56 JTAG_TDO_PCH → JTAG_TDO_PCH (16)
PCH_JTAG_TMS C59 JTAG_TMS_PCH → JTAG_TMS_PCH (16)
PCH_TRST# C61 XDP_TRST#_CPU → XDP_TRST#_CPU (2,16)
JTAGX A59 JTAGX_PCH → JTAGX_PCH (16)

SKL_ULT
REV = 1
4 OF 20

(26,32,34) H_PROCHOT# → R377 499/F_4 (26) EC_PECI
TP36 CATERR#
EC_PECI
PROCHOT#
PM_THRMTRIP# (26) → PM_THRMTRIP#

(16) XDP_BPM0
(16) XDP_BPM1

TP37
(18) INT_T_SCRN# → R201 *0_4 → CPU_GP3
(14,18,23) GSEN_I2C1_INT#
TP49

R229 49.9/F_4 PROC_POPIRCOMP
R222 49.9/F_4 PCH_OPI_RCOMP
R70 49.9/F_4 EDRAM_OPIO_RCOMP
R82 49.9/F_4 EOPIO_RCOMP

+VCCSTPLL
R365 49.9/F_4 CATERR#

+1.0V
R334 *0_4S
EC-SIT2-01
R353 51_4 JTAGX_PCH
R339 51_4 JTAG_TMS_PCH
R341 51_4 JTAG_TDI_PCH
R354 51_4 JTAG_TDO_PCH
R346 51_4 JTAG_TCK_PCH

Close to Chipset

Close to EC

+VCCSTPLL
PM_THRMTRIP# R364 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL
470 OHM IS FOR I/P

PLACE NEAR CPU

+1.0V
XDP_TMS_CPU R340 51_4
XDP_TDI_CPU R344 51_4
XDP_TDO_CPU R347 51_4

+3V_DEEP_SUS
10K_4 R216 GSEN_I2C1_INT#
10K_4 R360 INT_T_SCRN#
EC-SIT-05

+VCCSTPLL
H_PROCHOT# R363 1K_4
XDP_TCK0 R358 51_4
XDP_TRST#_CPU R337 51_4

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02 – SKYLAKE 1/20(eDP/DDI)
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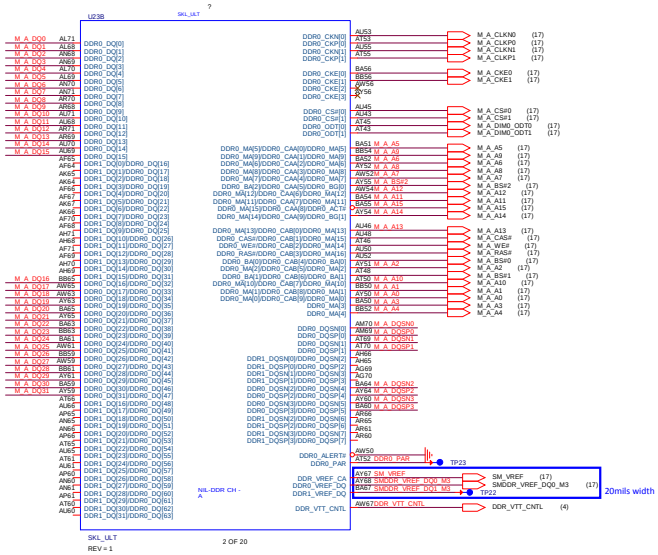
SkyLake ULT Processor (DDR3L)

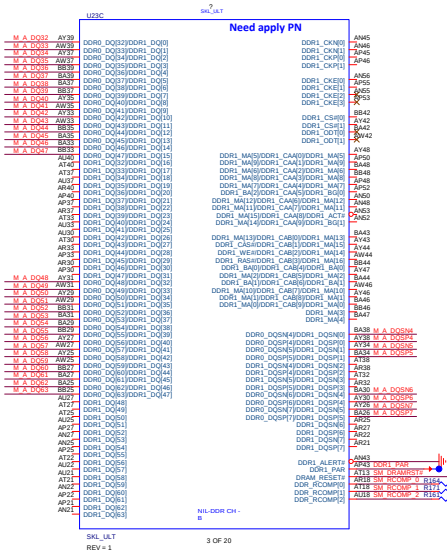
(17) M_A_DQSN[7:0]
(17) M_A_DQSP[7:0]
(17) M_A_DQ[63:0]

+1.35VSUS (6,17,38,43)

Need apply PN



Need apply PN



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Size: Document Number: 03 -- SKYLAKE 3/20(DDR3-A I/F) Rev: 1A
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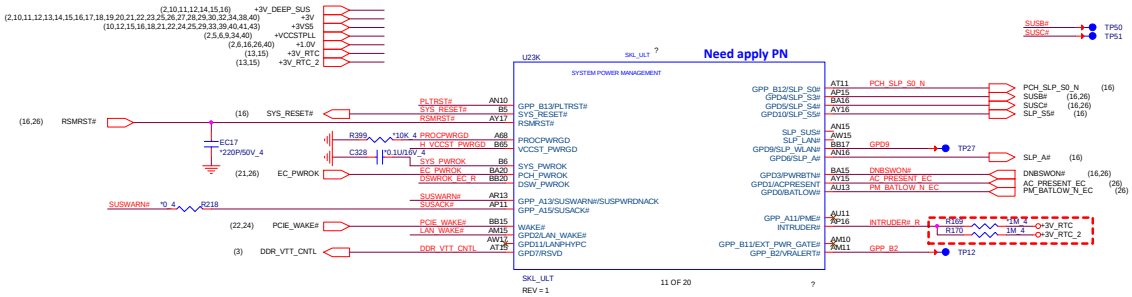
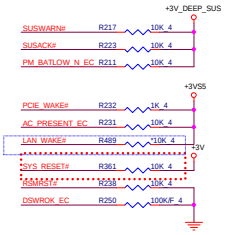
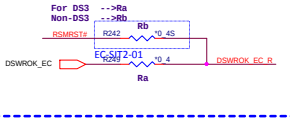


PCH Pull-high/low(CLG)



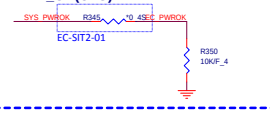
For DS3 Sequence

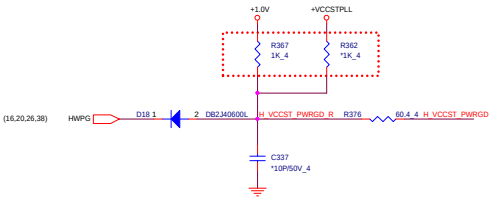


PLTRST#(CLG)

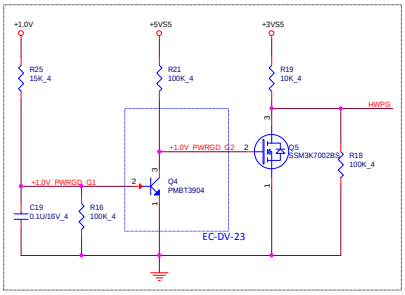
Check Q2010 Rise/Fall time less than 100ns

System PWR_OK(CLG)





Close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



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Document Number
Custom
04 -- SKYPAKE 5/20(Power Manger)
Rev
1A
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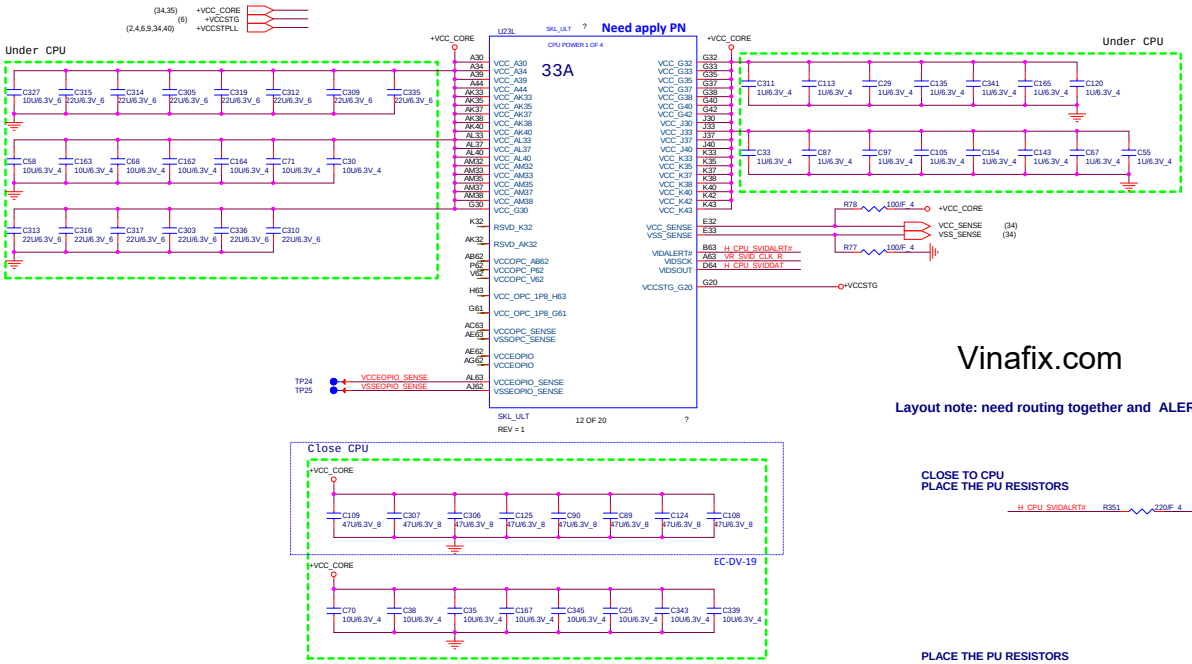
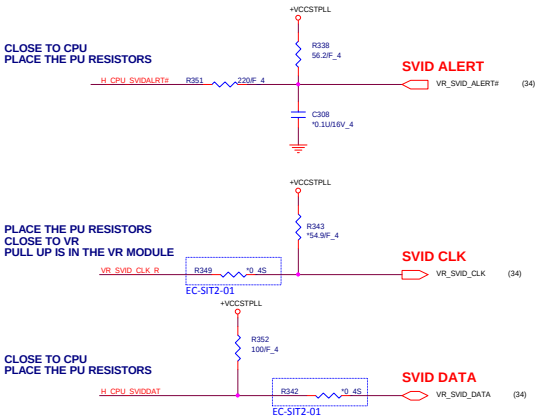


Layout note: need routing together and ALERT need between CLK and DATA.



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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Quanta Computer Inc.
Size: Document Number: 05 -- SKYPAKE 6/20 (POWER-1) Rev: 1A
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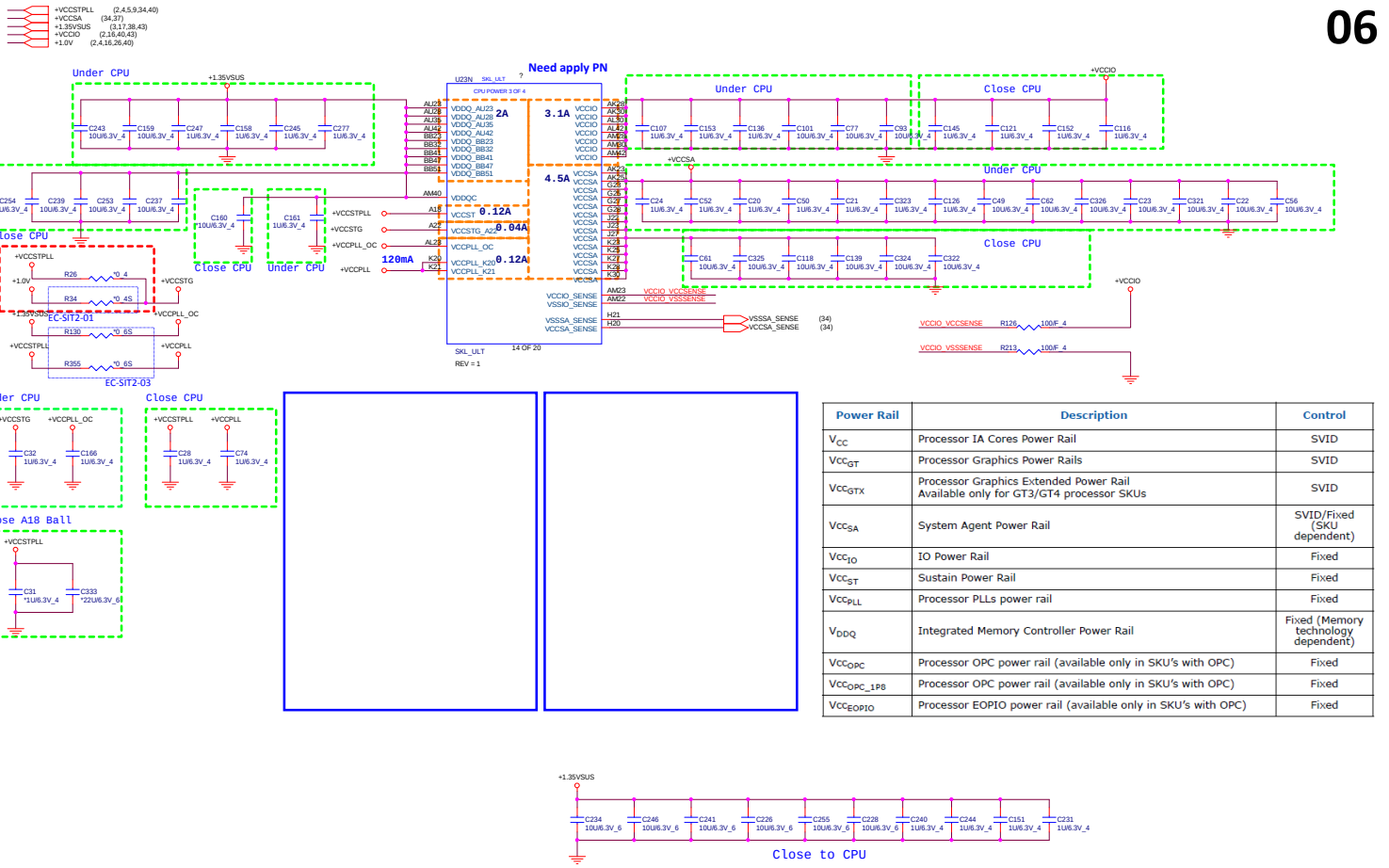

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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Size | Document Number | Custom | 06 -- SKYPAKE 7/20 (POWER-2) | Rev 1A
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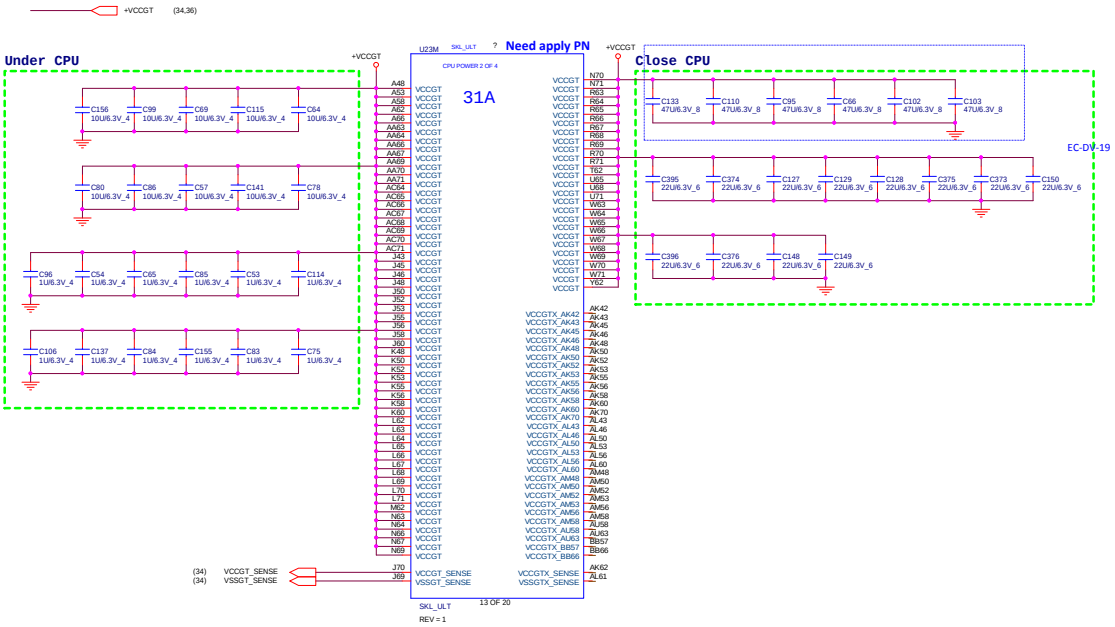

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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07 -- SKYPAKE 8/20 (POWER-3)
Rev 1A
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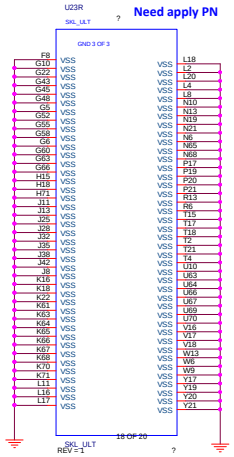

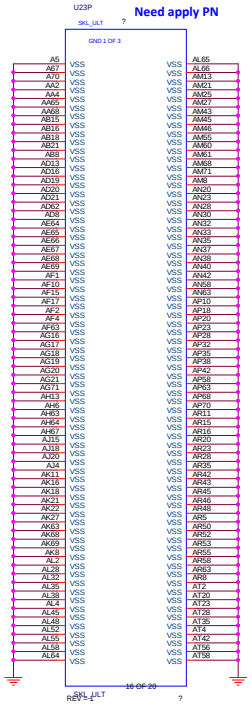

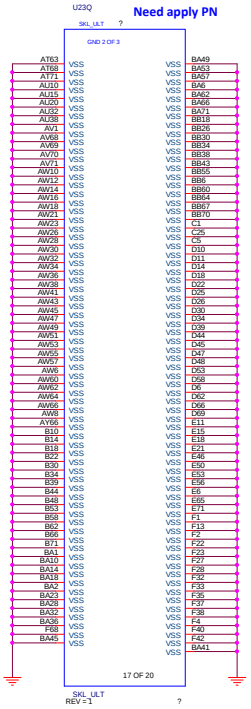

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Size	Document Number	Rev
	8 -- SKYPAKE 9/20 (GND-1)	LA

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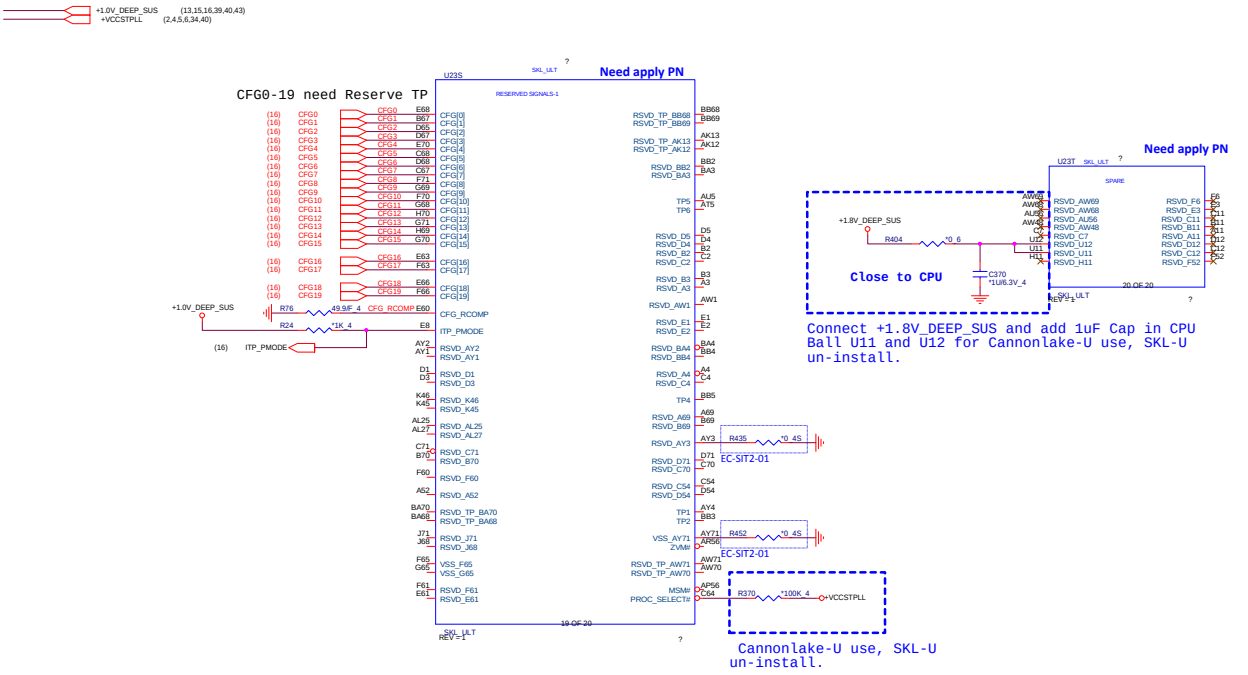

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R398 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R401 1K_4

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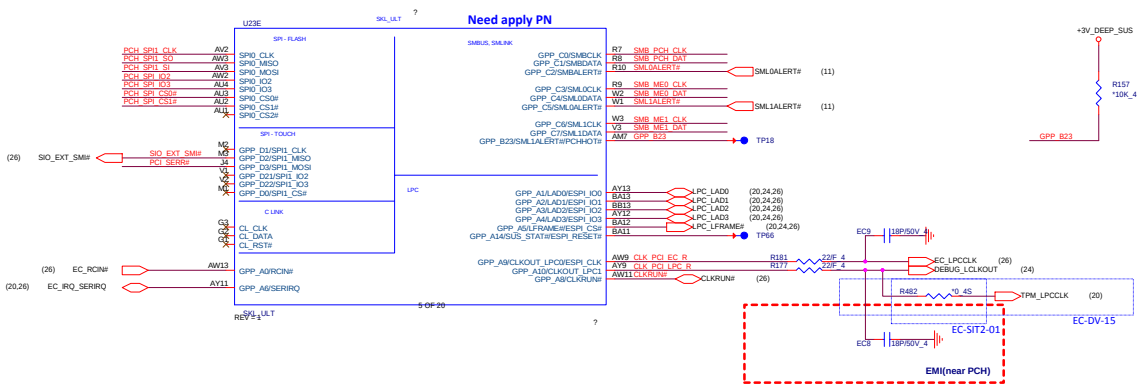
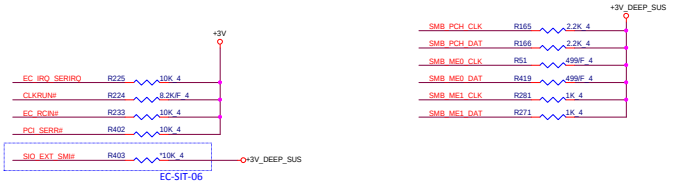
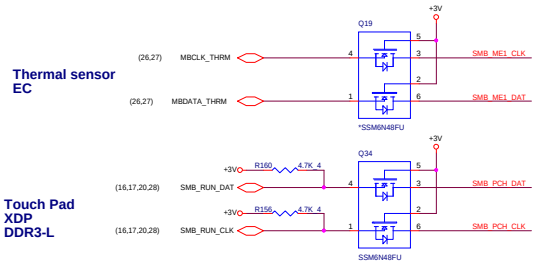
+3V_DEEP_SUS (2,4,11,12,14,15,16)
+3V (2,4,11,12,13,14,15,16,17,18,19,20,21,22,23,25,26,27,28,29,30,32,34,38,40)
+3VS5 (4,12,15,16,18,21,22,24,25,29,33,39,40,41,43)



GPIO Pull UP



SMBus/Pull-up(CLG)

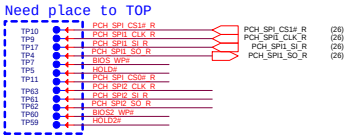


PCH SPI ROM(CLG)

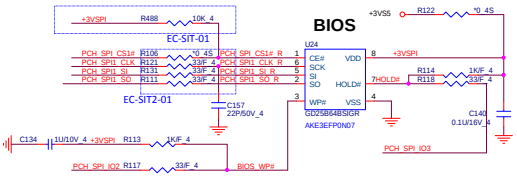
EC-DV-14

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
Socket		DFHS08FS023

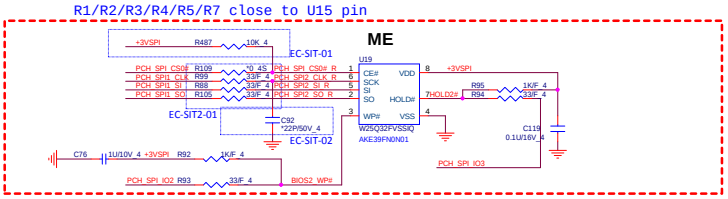
Need place to TOP



PCH SPI ROM(CLG)



R1/R2/R3/R4/R5/R7 close to U15 pin



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Size	Document Number	Rev
	10 -- SKYPAKE 14/20(SPI/LPC/SMBUS)	1A
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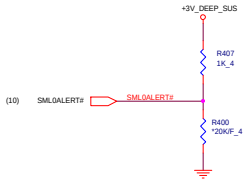
+3V_DEEP_SUS (2,4,10,12,14,15,16)
+3V (2,4,10,12,13,14,15,16,17,18,19,20,21,22,23,25,26,27,28,29,30,32,34,38,40)

Functional Strap Definitions

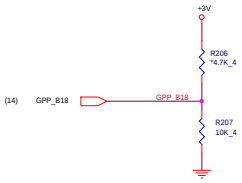
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET

TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

Flash Descriptor Security Override:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
This function is useful when running ITP/XDP.



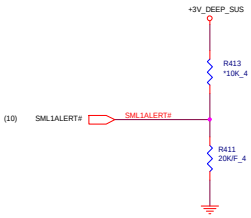
TLS Confidentiality:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO
Timer system reboot feature).
This function is useful when running ITP/XDP.

Boot BIOS Strap Bit :
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



eSPI or LPC:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

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	11 -- SKYPAKE 15/20(HDA)	1A
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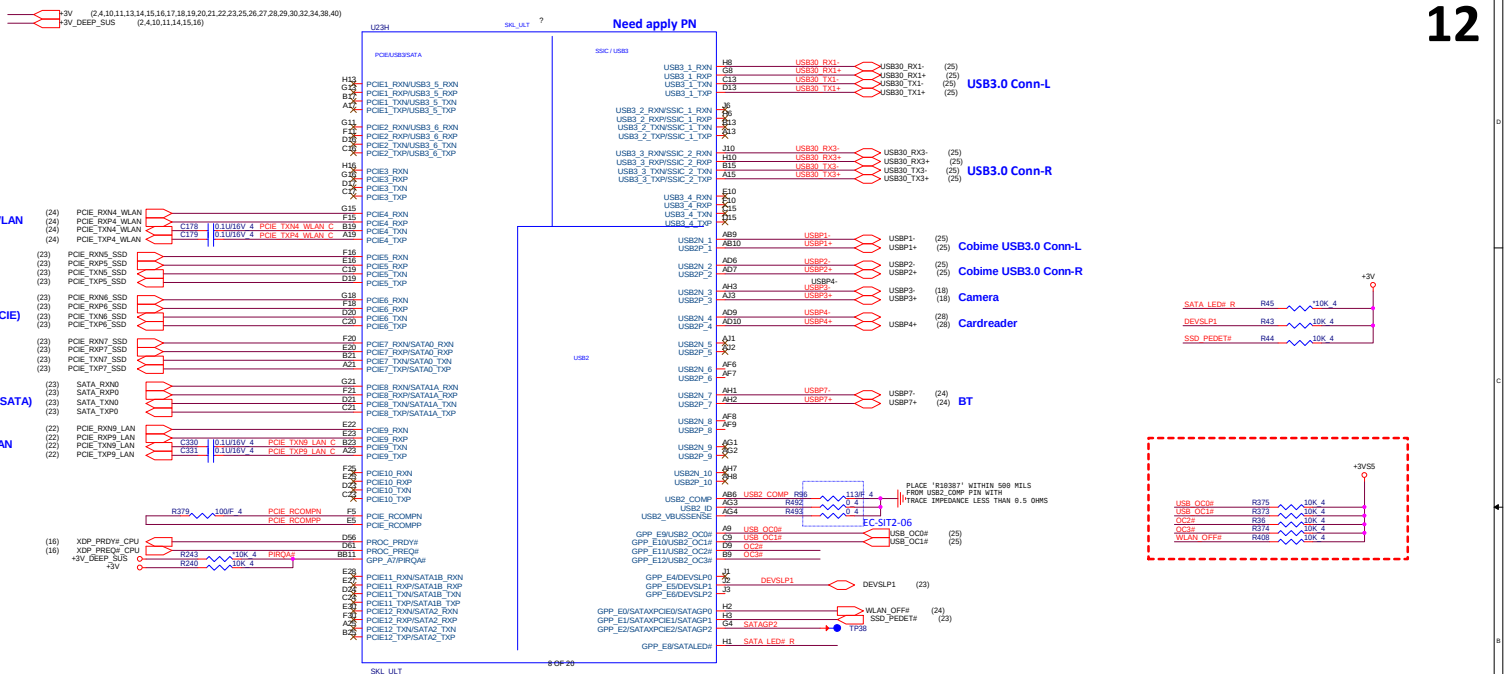


PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	Un-used	Port0	Un-used
Port2	Un-used	Port1	Un-used
Port3	Un-used	Port2	WLAN
Port4	WLAN	Port3	LAN
Port5	SSD(PCIE_3)	Port4	Un-used
Port6	SSD(PCIE_2)	Port5	Un-used
Port7	SSD(PCIE_1)		
Port8	SSD(SATA)		
Port9	LAN		
Port10	Un-used		

USB3.0 Port Mapping Table

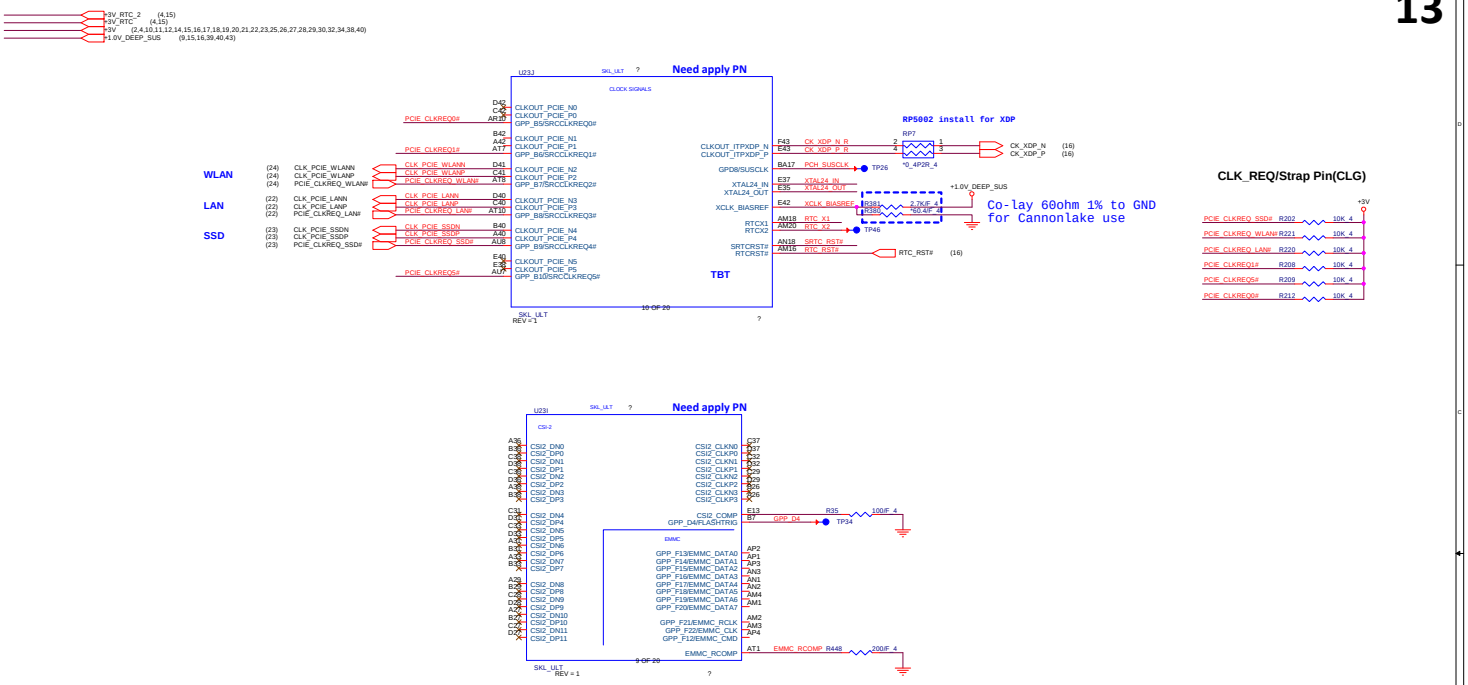
USB3.0	Function
PORT-1	USB3.0 Conn-L
PORT-2	NC
PORT-3	USB3.0 Conn-R
PORT-4	NC

USB2.0 Port Mapping Table

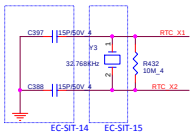
USB2.0	Function
PORT-1	Cobime USB3.0 Conn-L
PORT-2	Cobime USB3.0 Conn-R
PORT-3	Camera
PORT-4	Cardreader
PORT-5	NC
PORT-6	NC
PORT-7	BT
PORT-8	NC
PORT-9	NC
PORT-10	NC

PROJECT : LI8
Quanta Computer Inc.

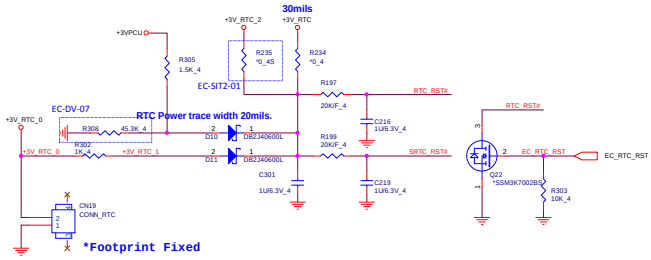
Size	Document Number	Rev
	12 -- SKYPAKE 16/20 (PCIE/USB)	1A
Date: Monday, November 09, 2015	Sheet 12 of 43	



RTC Clock 32.768KHz

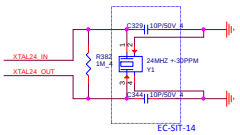


RTC Circuitry(RTC)



External Crystal and Green Clock

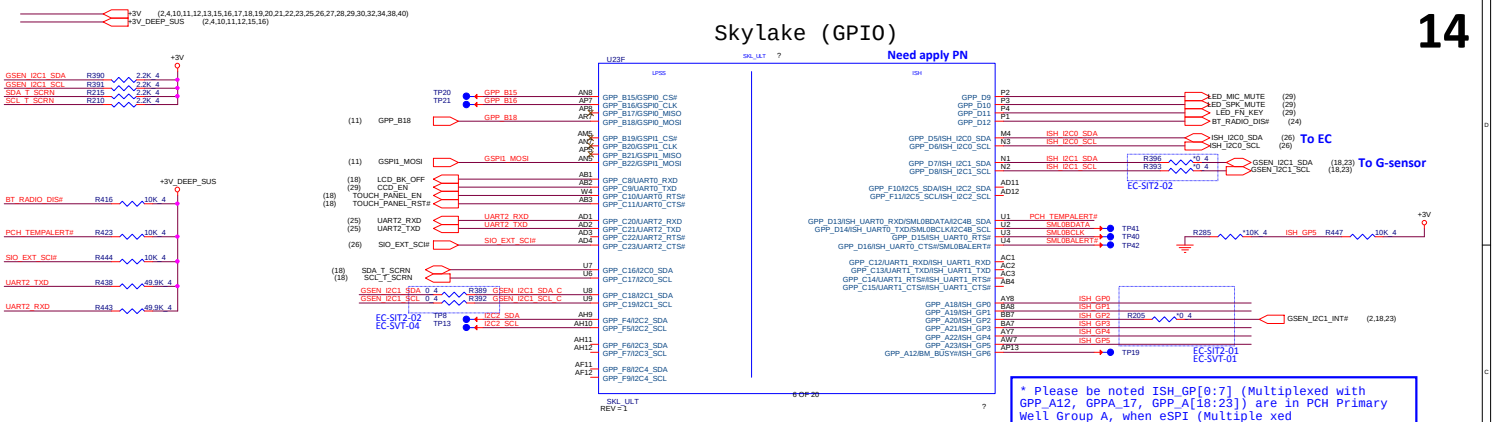
The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.



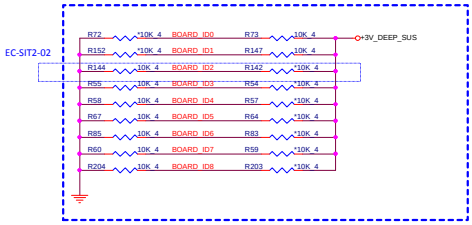
PROJECT : LI8
Quanta Computer Inc.

Size	Document Number	Rev
	13 – SKYPAKE 17/20 (CLK)	1A
Date: Monday, November 09, 2015	Sheet 13 of 43	

Skylake (GPIO)

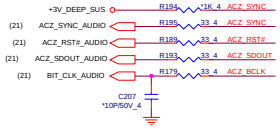


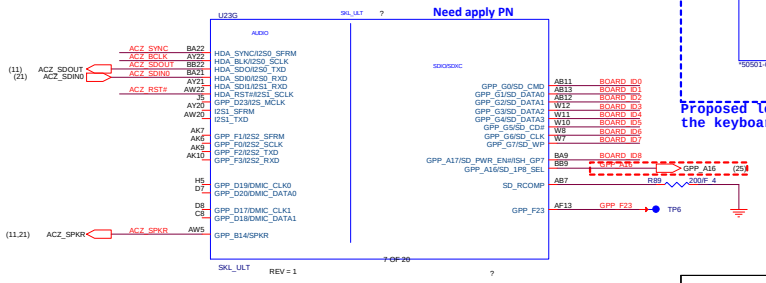
* Please be noted ISH_GP[0:7] (Multiplexed with GPP_A12, GPPA_17, GPP_A[18:23]) are in PCH Primary Well Group A, when eSPI (Multiple xed withGPP_A[0:15]) is enable, VCCPGPPA should be supplied by 1.8V. That means the signaling level of all the Primary Well Group A signals including ISH_GP[0:7] will be 1.8V.



Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
Touch SKU(ISH)	0	0	0	0	0	1
Non-Touch(ISH)	0	0	0	0	0	0
Touch SKU(I2C)	0	0	0	0	1	1
Non-Touch(I2C)	0	0	0	0	1	0
SIT2 Touch SKU(I2C)	0	0	0	1	1	1
SIT2 Non-Touch(I2C)	0	0	0	1	1	0
TBD						

HDA Bus(CLG)





Proposed location must be under the keyboard (TOP side)

PROJECT : LI8
Quanta Computer Inc.

Size	Document Number	Rev
	14 – SKYPAKE 19/20 (GPIO)	1A
Date: Monday, November 09, 2015	Sheet 14 of 43	

(2,4,10,11,12,14,16) +3V_DEEP_SUS
(9,13,16,39,40,43) +1.0V_DEEP_SUS
(9,41,43) +1.8V_DEEP_SUS
(4,13) +3V_RTC
(4,10,12,16,18,21,22,24,25,29,33,39,40,41,43) +3VS5
(4,13) +3V_RTC_2

U23O SKL_ULT CPU POWER 4 OF 4 — Need apply PN

PCH Internal VRM

C820 and C690 close to cpu less then 100 mils

+VCCPRIM — C117 1U/6.3V_4 — AB19 VCCPRIM_1P0, AB20 VCCPRIM_1P0, P18 VCCPRIM_1P0 — 2.899A
+1.0V_DEEP_SUS — C91 1U/6.3V_4 — AF18 VCCPRIM_CORE, AF19 VCCPRIM_CORE, V20 VCCPRIM_CORE, V21 VCCPRIM_CORE — 2.57A
+VCCDSW_1.0V — C385 1U/6.3V_4 — AL1 DCPDSW_1P0
+1.0V_DEEP_SUS — R405 *0_4S, C106 1U/6.3V_4 — +VCCMPHYAON_1P0 — K17 VCCMPHYAON_1P0, L1 VCCMPHYAON_1P0
+1.0V_DEEP_SUS — C15 1U/6.3V_4, C320 47U/6.3V5_8 — N15 VCCMPHYGT_1P0_N15, N16 VCCMPHYGT_1P0_N16, N17 VCCMPHYGT_1P0_N17, P15 VCCMPHYGT_1P0_P15, P16 VCCMPHYGT_1P0_P16 — 1.714A
+1.0V_DEEP_SUS — R23 *0_4S, C17 1U/6.3V_4 — +VCCAMPHYPLL_1P0 — K15 VCCAMPHYPLL_1P0, L15 VCCAMPHYPLL_1P0
+1.0V_DEEP_SUS — R74 *0_6S — +VCCAPLL_1.0V — V15 VCCAPLL_1P0 — 0.03A
+1.0V_DEEP_SUS — R98 *0_6S — +VCCPRIM — AB17 VCCPRIM_1P0_AB17, Y18 VCCPRIM_1P0_Y18
+3VS5 — R159 *0_4S — +VCCDSW_3P3 — AD17 VCCDSW_3P3_AD17, AD18 VCCDSW_3P3_AD18, AJ17 VCCDSW_3P3_AJ17 — 0.09A
C138 1U/6.3V_4, C208 1U/6.3V_4
+V3.3DX_1.5DX_ADO — AJ19 VCCHDA
+3V_DEEP_SUS — R110 *0_4S — +VCCSPI — AJ16 VCCSPI
+1.0V_DEEP_SUS — R107 *0_6S, C82 1U/6.3V_4 — +VCCSRAM_1.0V — AF20 VCCSRAM_1P0, AF21 VCCSRAM_1P0, T19 VCCSRAM_1P0, T20 VCCSRAM_1P0
+3V_DEEP_SUS — R200 *0_6S — +VCCPRIM_3.3V — AJ21 VCCPRIM_3P3_AJ21
+1.0V_DEEP_SUS — R415 *0_6S — +VCCPRIM_1.0V — AK20 VCCPRIM_1P0_AK20
+1.0V_DEEP_SUS — R22 *0_4S, C81 1U/6.3V_4 — +VCCAPLLEBB — N18 VCCAPLLEBB

EC-SIT2-03 EC-SIT2-01

SKL_ULT REV = 1

15 OF 20

VCCPGPPA AK15 +VCCPGPPA
VCCPGPPB AG15 +VCCPGPPB
VCCPGPPC Y16 +VCCPGPPC
VCCPGPPD Y15 +VCCPGPPD
VCCPGPPE T16 +VCCPGPPE
VCCPGPPF AF16 +VCCPGPPF
VCCPGPPG AD15 +VCCPGPPG
VCCPRIM_3P3_V19 V19
VCCPRIM_1P0_T1 T1 +VCCPRIM_1.0V — R120 *0_6S — +1.0V_DEEP_SUS
VCCATS_1P8 AA1 +VCCATS_1.8V — R412 *0_4S — +1.8V_DEEP_SUS
VCCRTCPRIM_3P3 AK17 +VCCRTCPRIM_3.3V — R146 *0_4S — +3V_DEEP_SUS
VCCRTC_AK19 AK19 +VCCRTC — R178 *0_4S — +3V_RTC
VCCRTC_BB14 BB14 — R174 *0_4S — +3V_RTC_2
DCPRTC BB10 DCPRTC — C203 1U/6.3V_4 — +1.8V_DEEP_SUS
VCCCLK1 A14 +VCCCLK1 — R359 *0_4S
VCCCLK2 K19 +VCCCLK2 — R27 *0_4S
VCCCLK3 L21 +VCCCLK3 — R28 *0_4S
VCCCLK4 N20 +VCCCLK4 — R30 *0_4S
VCCCLK5 L19 +VCCCLK5 — R29 *0_4S
VCCCLK6 A10 +VCCCLK6 — R372 *0_4S
GPP_B0/CORE_VID0 AN11 CORE_VID0 — TP14
GPP_B1/CORE_VID1 AN13 CORE_VID1 — TP15
C386 1U/6.3V_4 — +3V_DEEP_SUS
C342 1U/6.3V_4

20mils

EC-SIT2-01 EC-SIT2-03

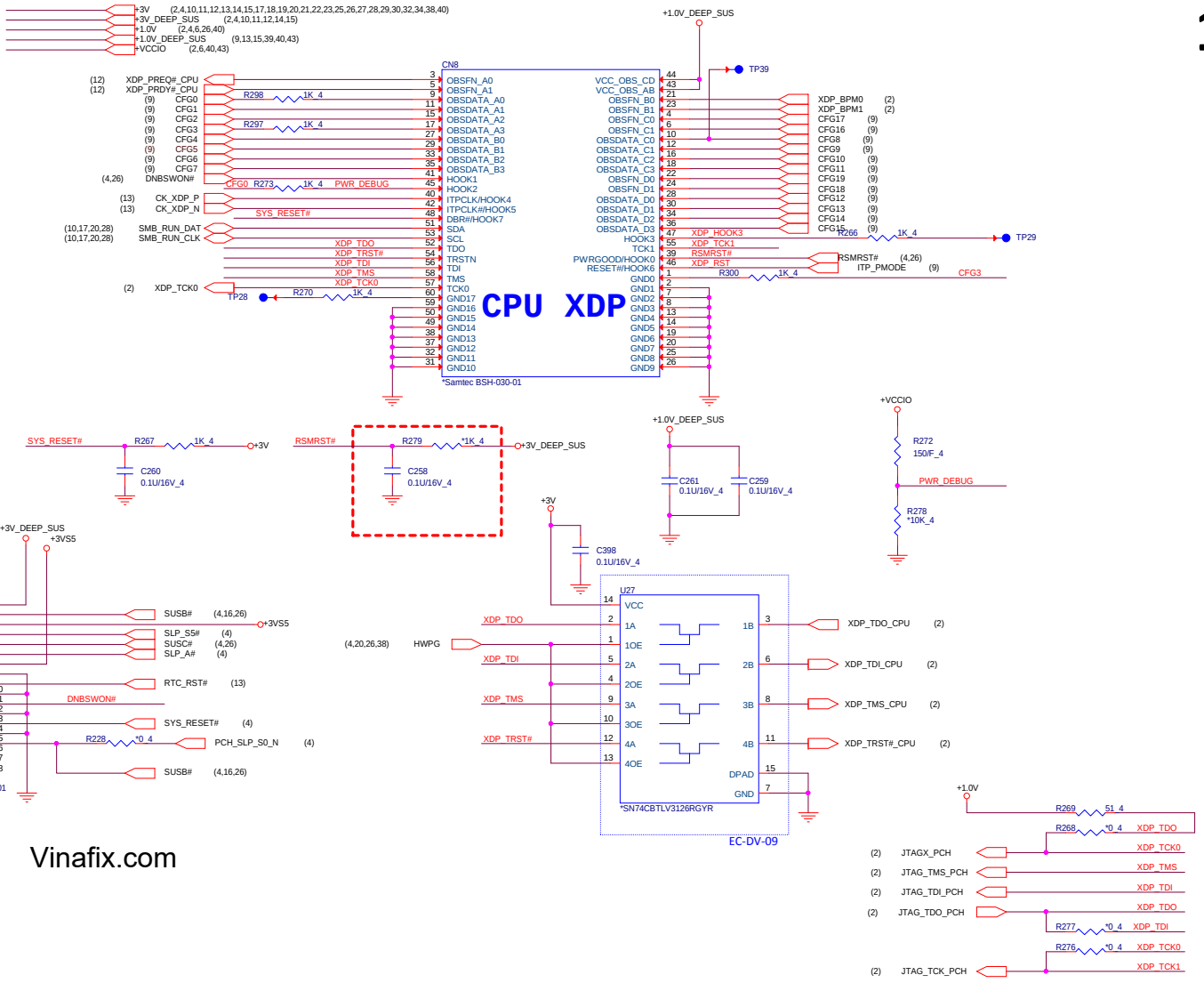
+3V_DEEP_SUS
+VCCPGPPA R139 *0_4S
+VCCPGPPB R135 *0_4S
+VCCPGPPC R87 *0_4S
+VCCPGPPD R91 *0_4S
+VCCPGPPE R84 *0_4S
+VCCPGPPG R104 *0_4S
+1.8V_DEEP_SUS
+VCCPGPPF R420 *0_6S
EC-SIT2-01 EC-SIT2-03

+V3.3DX_1.5DX_ADO — R176 *0_4S — +3V — EC-SIT2-01
+1.0V_DEEP_SUS — C16 *1U/6.3V_4, C14 *22U/6.3V_6

+3VS5 — R153 *0_6S, R158 *0_6S — +3V_DEEP_SUS — EC-SIT2-03

+VCCATS_1.8V — C380 1U/6.3V_4
+VCCRTC — C196 0.1U/16V_4, C206 1U/6.3V_4
+VCCRTCPRIM_3.3V — C174 1U/6.3V_4, C181 0.1U/16V_4
+VCCPGPPB — C168 1U/6.3V_4
+VCCPGPPC — C79 1U/6.3V_4
+VCCPGPPE — C59 1U/6.3V_4

PROJECT : LI8
Quanta Computer Inc.
Size | Document Number | Rev 1A
15 -- SKYPAKE 20/20(PCH POWER)
Date: Monday, November 09, 2015 Sheet 15 of 43



Vinafix.com

PROJECT : LI8
Quanta Computer Inc.

Size	Document Number	Rev
	16 – HSW XDP & APS	1A

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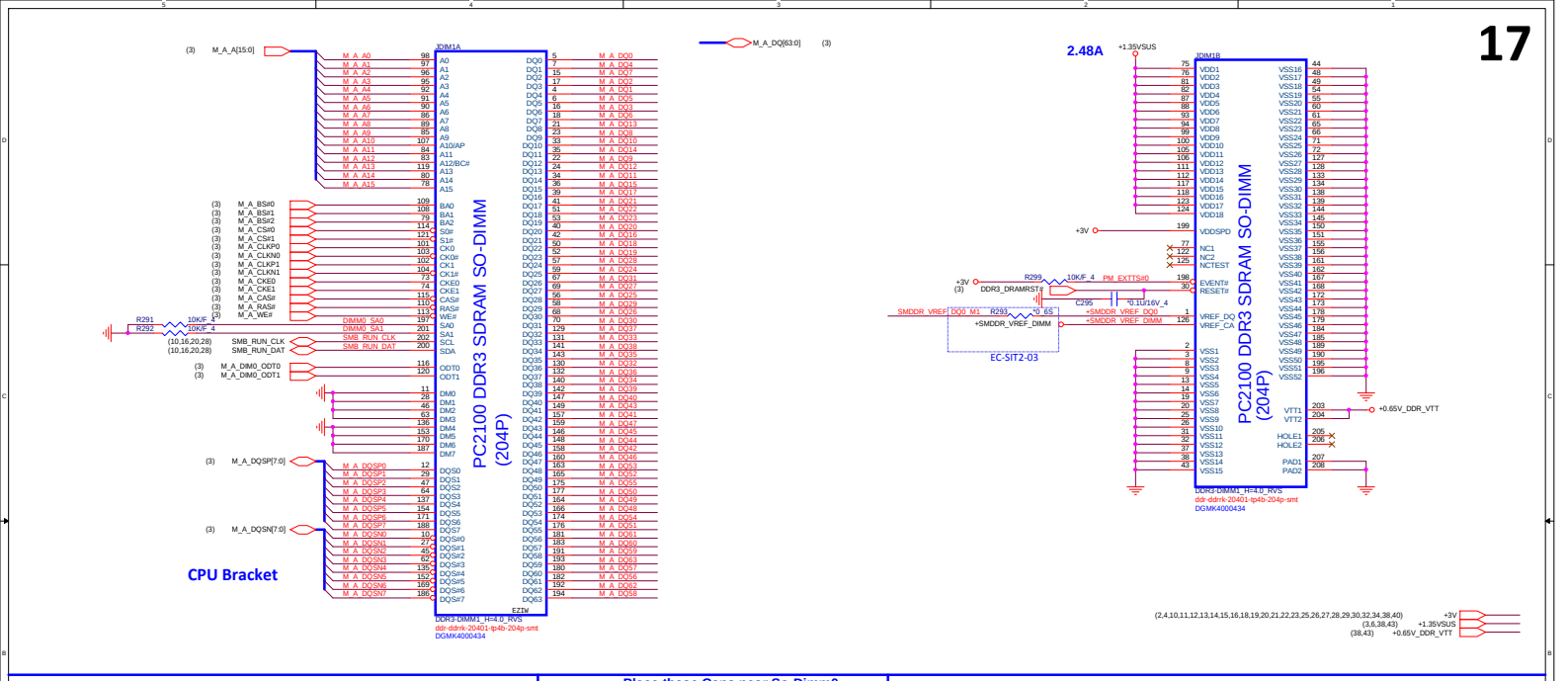
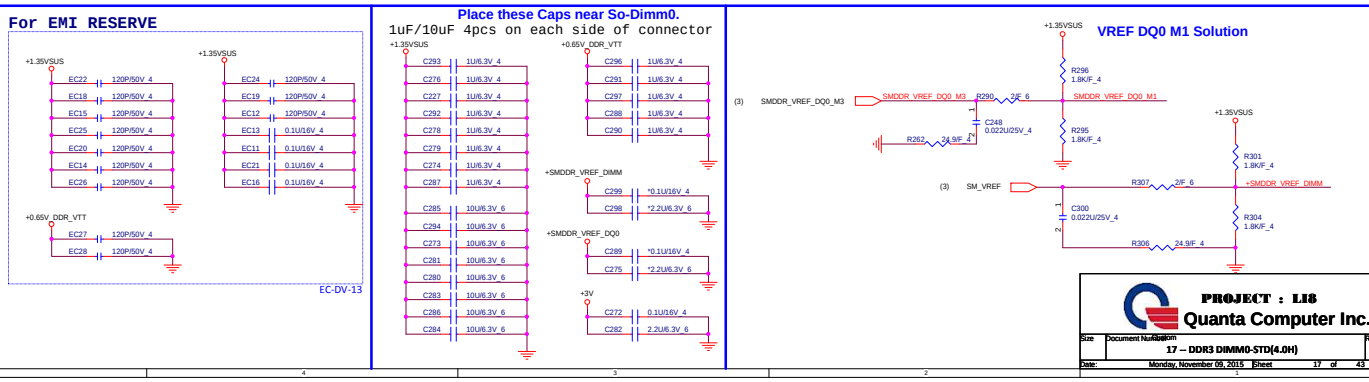
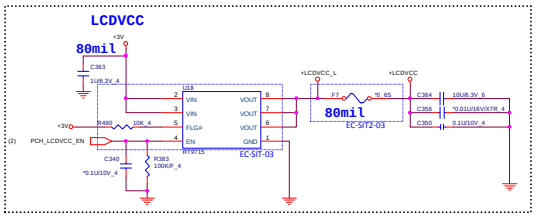
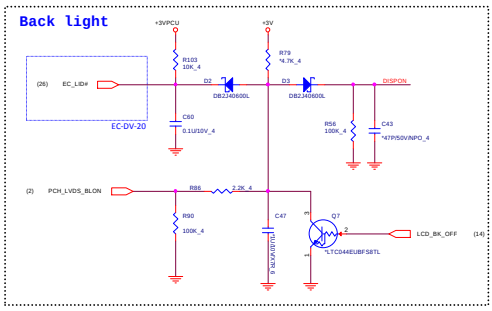

JDIM1A
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM1_H=4.0_RVS
ddr-ddrrk-20401-tp4b-204p-smt
DGMK4000434
CPU Bracket
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM1_H=4.0_RVS
ddr-ddrrk-20401-tp4b-204p-smt
DGMK4000434
2.48A
EC-SIT2-03


For EMI RESERVE
EC-DV-13
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ0 M1 Solution
PROJECT : LI8
Quanta Computer Inc.
17 -- DDR3 DIMM0-STD(4.0H)
Monday, November 09, 2015

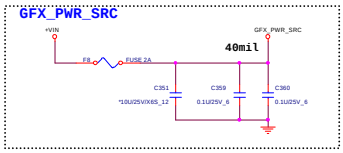
LCDVCC

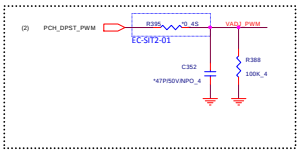


Back light

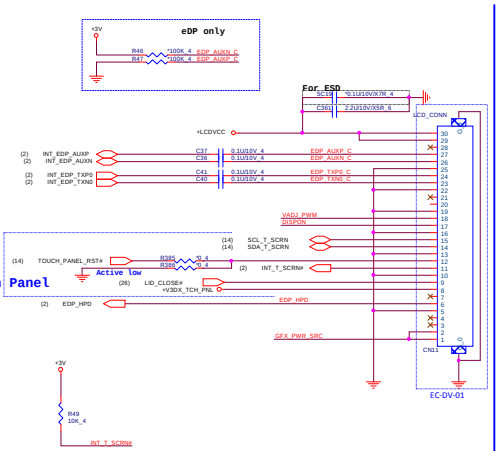


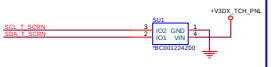
GFX_PWR_SRC



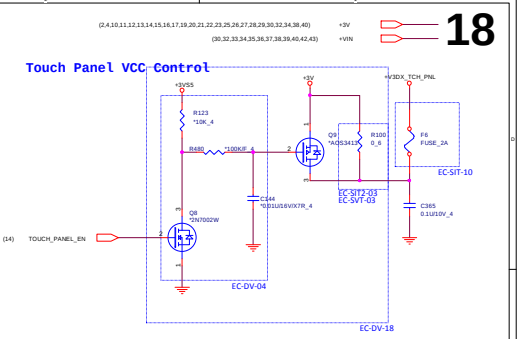


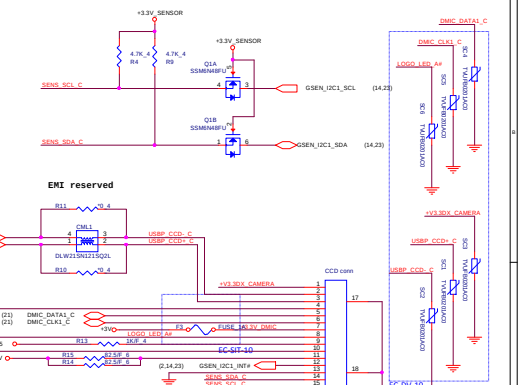
Touch Panel



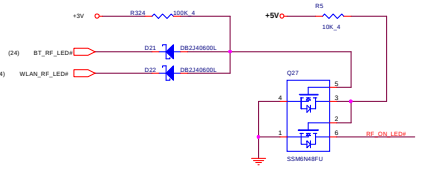


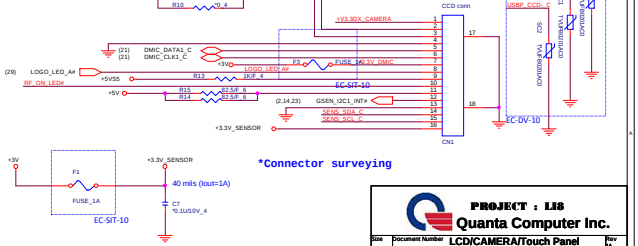
Touch Panel VCC Control



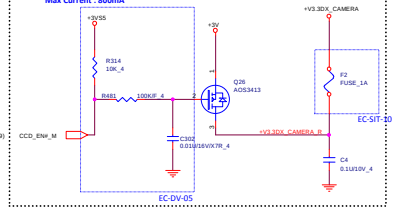


CCD+MIC+LOGO+WLAN LED CONN

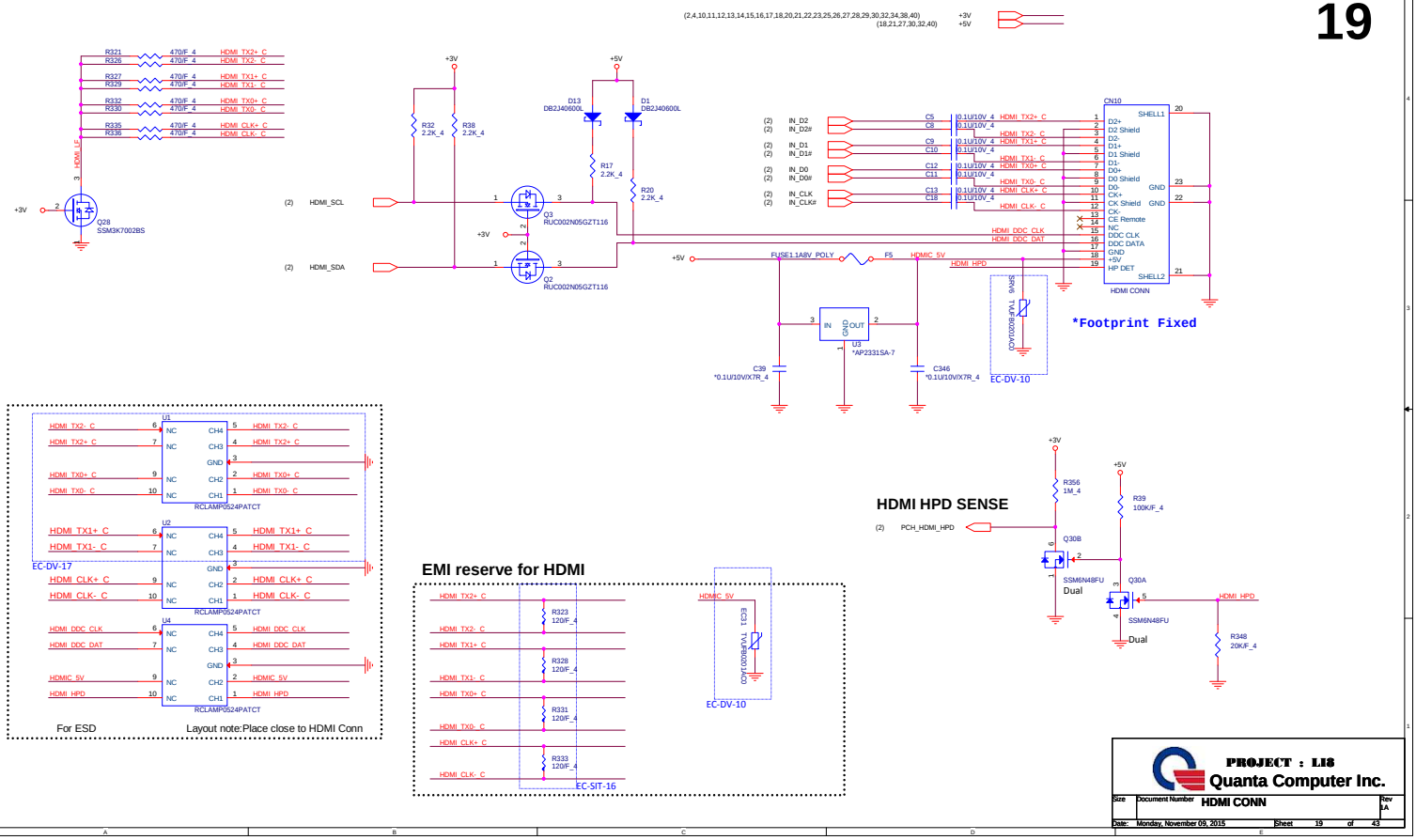




CAMERA VCC Control



*Connector surveying


(2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,25,26,27,28,29,30,32,34,38,40)
(18,21,27,30,32,40)
+3V
+5V
R321 470/F_4 HDMI_TX2+_C
R326 470/F_4 HDMI_TX2-_C
R327 470/F_4 HDMI_TX1+_C
R329 470/F_4 HDMI_TX1-_C
R332 470/F_4 HDMI_TX0+_C
R330 470/F_4 HDMI_TX0-_C
R335 470/F_4 HDMI_CLK+_C
R336 470/F_4 HDMI_CLK-_C
HDMI_LF
Q28
SSM3K7002BS
(2) HDMI_SCL
(2) HDMI_SDA
R32 2.2K_4
R38 2.2K_4
D13 DB2J40600L
D1 DB2J40600L
R17 2.2K_4
R20 2.2K_4
Q3 RUC002N05GZT116
Q2 RUC002N05GZT116
(2) IN_D2
(2) IN_D2#
(2) IN_D1
(2) IN_D1#
(2) IN_D0
(2) IN_D0#
(2) IN_CLK
(2) IN_CLK#
C5 0.1U/10V_4
C9 0.1U/10V_4
C10 0.1U/10V_4
C12 0.1U/10V_4
C11 0.1U/10V_4
C13 0.1U/10V_4
C18 0.1U/10V_4
HDMI_TX2+_C
HDMI_TX2-_C
HDMI_TX1+_C
HDMI_TX1-_C
HDMI_TX0+_C
HDMI_TX0-_C
HDMI_CLK+_C
HDMI_CLK-_C
HDMI_DDC_CLK
HDMI_DDC_DAT
CN10
SHELL1
D2+
D2 Shield
D2-
D1+
D1 Shield
D1-
D0+
D0 Shield
D0-
CK+
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
SHELL2
GND
HDMI CONN
FUSE1.1A8V_POLY
F5
HDMIC_5V
HDMI_HPD
C39 *0.1U/10V/X7R_4
U3 *AP2331SA-7
C346 *0.1U/10V/X7R_4
EC-DV-10
*Footprint Fixed
HDMI HPD SENSE
(2) PCH_HDMI_HPD
R356 1M_4
R39 100K/F_4
Q30B
Q30A
SSM6N48FU
Dual
R348 20K/F_4
U1
U2
U4
RCLAMP0524PATCT
EC-DV-17
For ESD
Layout note:Place close to HDMI Conn
EMI reserve for HDMI
R323 120/F_4
R328 120/F_4
R331 120/F_4
R333 120/F_4
EC-SIT-16
EC-DV-10
PROJECT : LI8
Quanta Computer Inc.
Size
Document Number
HDMI CONN
Rev
1A
Date: Monday, November 09, 2015
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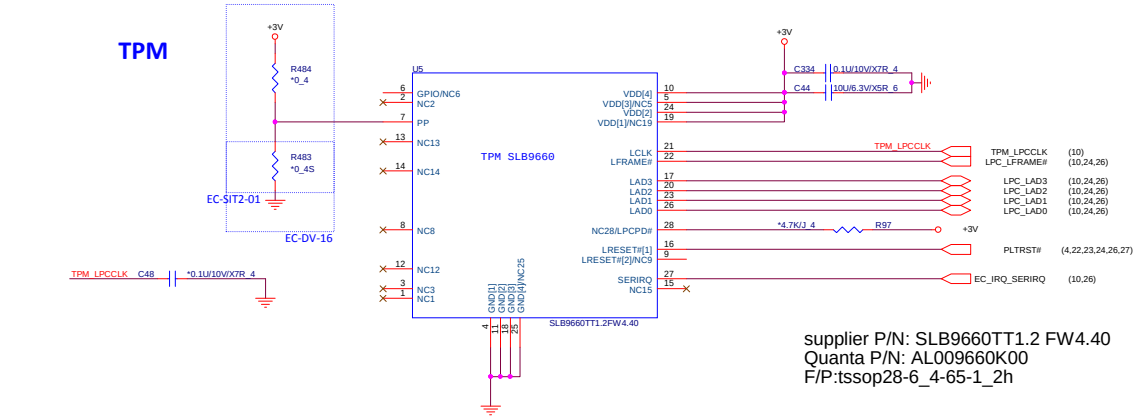
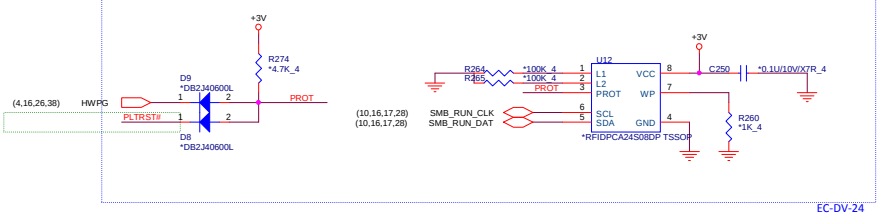
HDMI CONN

TPM



supplier P/N: SLB9660TT1.2 FW4.40
Quanta P/N: AL009660K00
F/P:tssop28-6_4-65-1_2h



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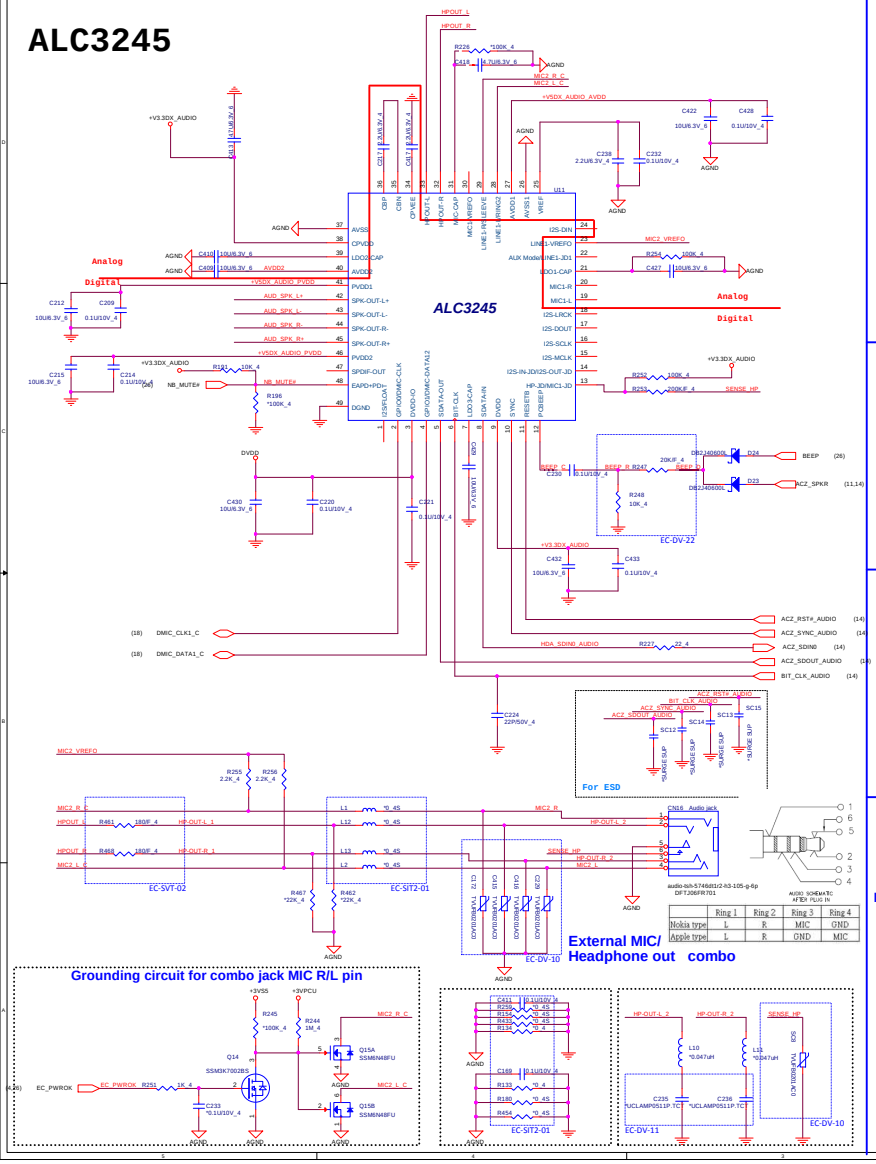
Quanta Computer Inc.

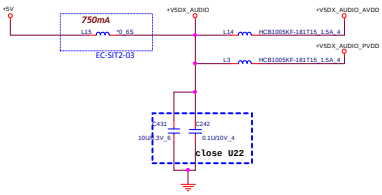
Size	Document Number	Rev
	TPM/RFID	1A
Date: Monday, November 09, 2015	Sheet 20 of 43	

ALC3245

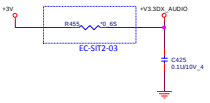


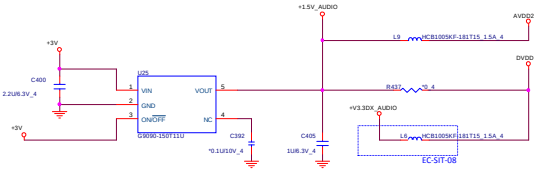
	Ring 1	Ring 2	Ring 3	Ring 4
Nokia type	L	R	MIC	GND
Apple type	L	R	GND	MIC

CODEC 5V POWER

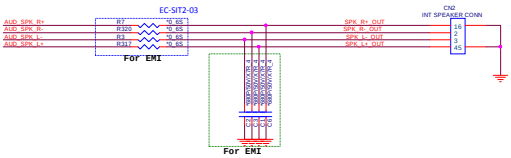


+3.3V_AUDIO_CODEC
Max Current : 419mA



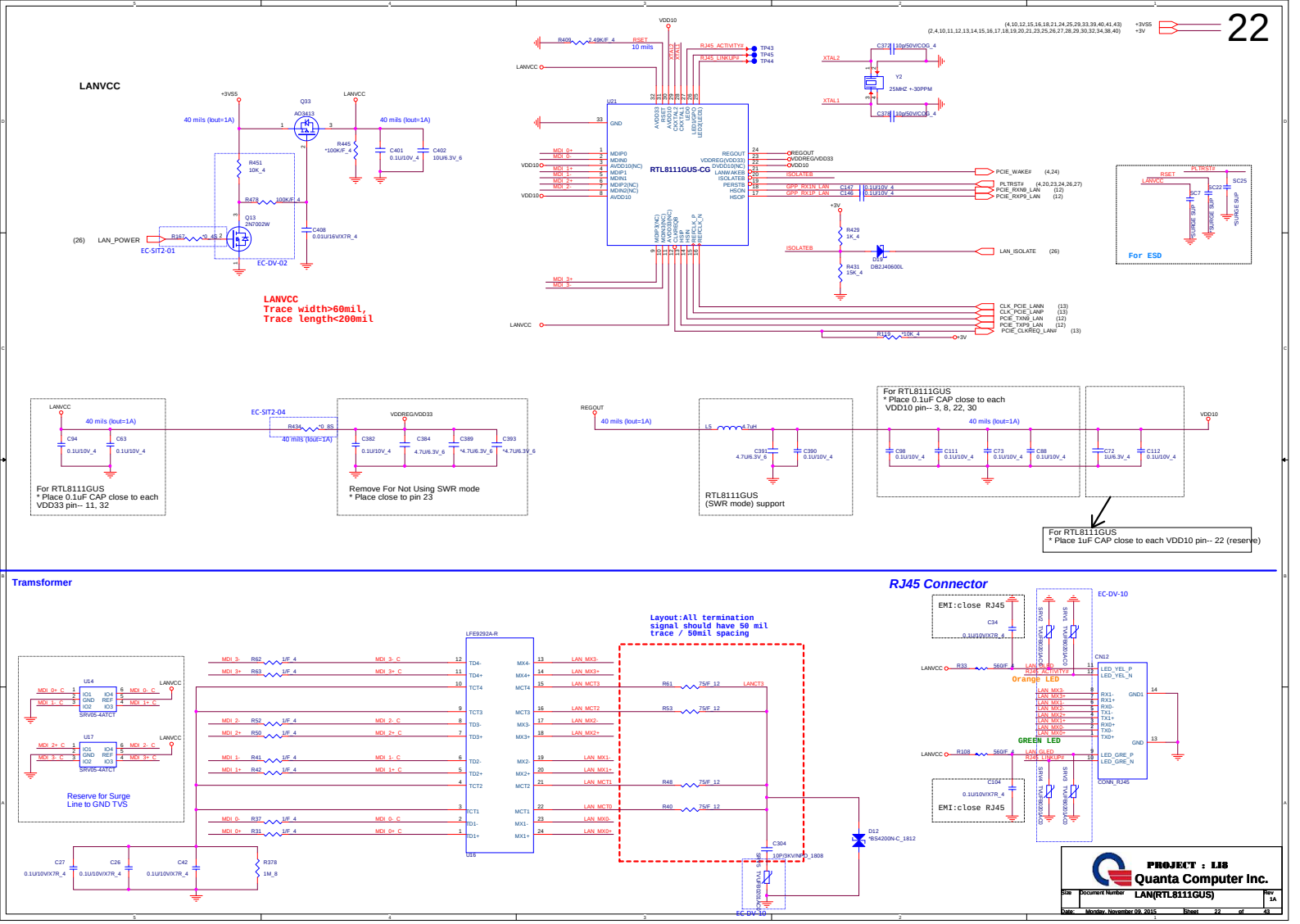


INT Speaker



Vinafix.com

PROJECT : LI8
Quanta Computer Inc.
Size: Document Number: Audio(ALC283) Rev: 1A
Date: Monday, November 09, 2015 Sheet 21 of 43



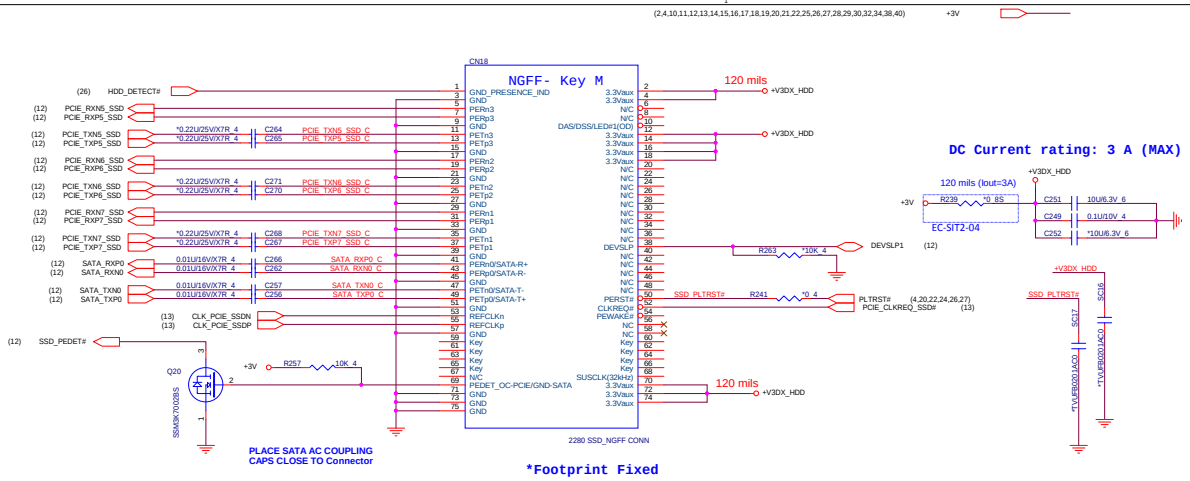
Tramsformer

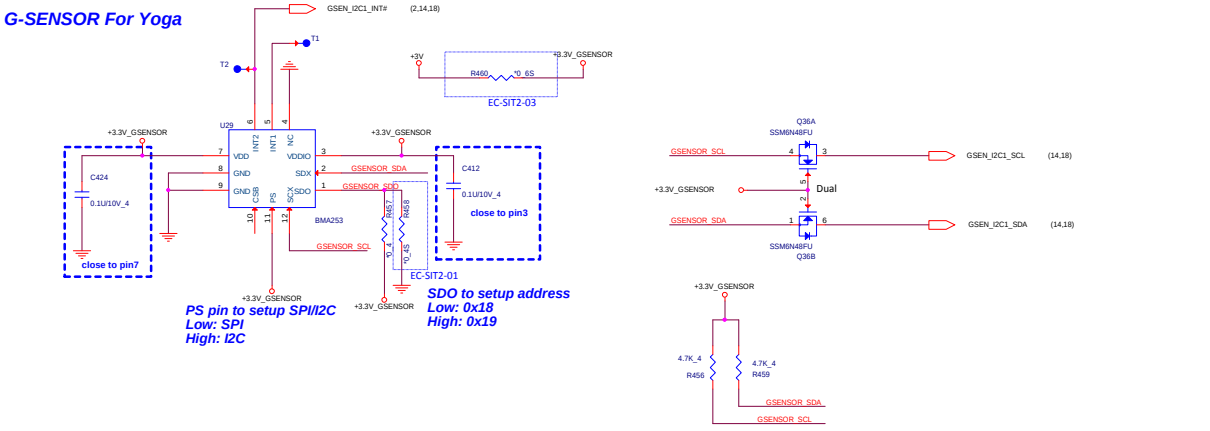
RJ45 Connector

PROJECT : LI8
Quanta Computer Inc.

Size	Document Number	Rev
	LAN(RTL8111GUS)	1A

Date: Monday, November 09, 2015 Sheet 22 of 43

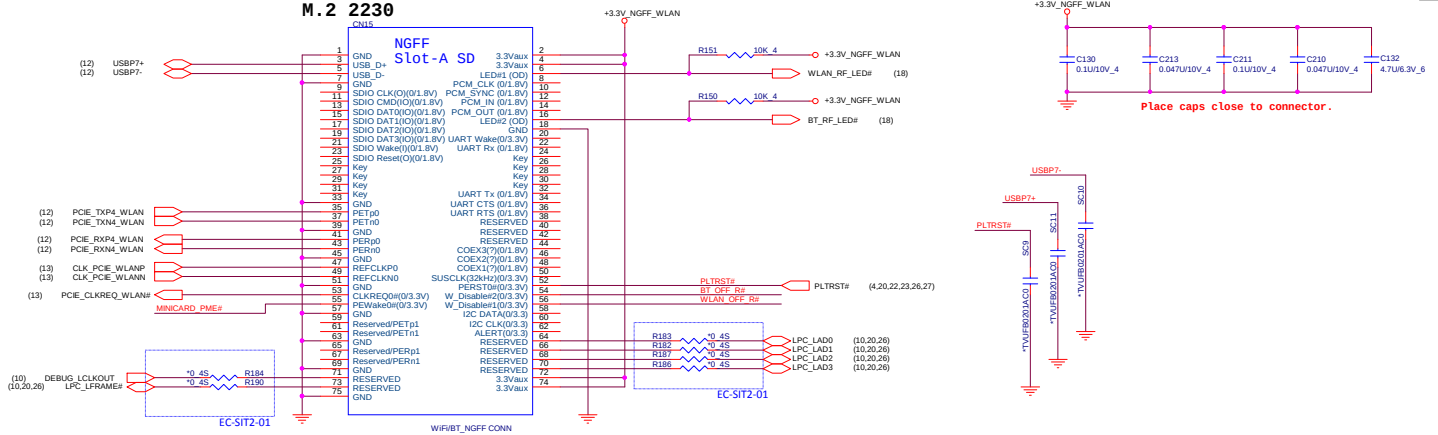




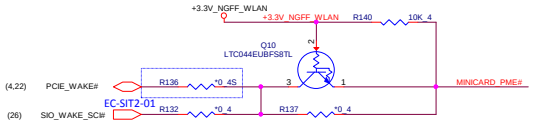
PROJECT : LI8			
Quanta Computer Inc.			
Size	Document Number	SATA/G-sensor	Rev 1A
Date: Monday, November 09, 2015	Sheet 23	of 43	

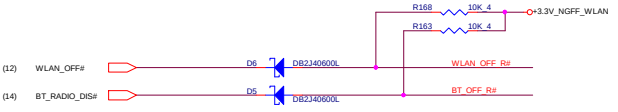
(2,4,10,11,12,13,14,15,16,17,18,19,20,21,22,23,25,26,27,28,29,30,32,34,38,40) +3V
(4,10,12,15,16,18,21,22,25,29,33,39,40,41,43) +3VS5

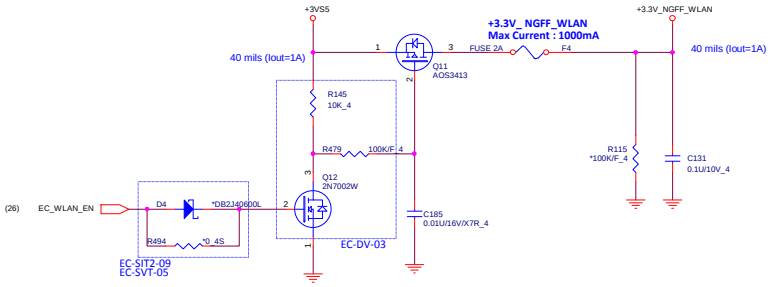
NGFF WiFi/BT connector
M.2 2230



***Footprint Fixed**





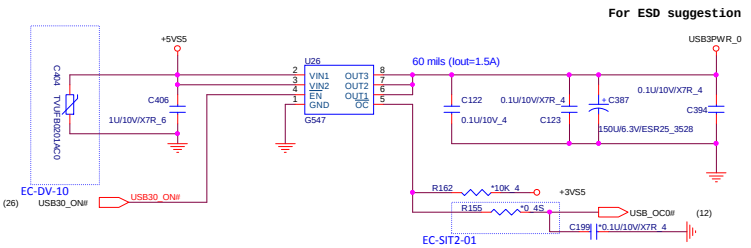


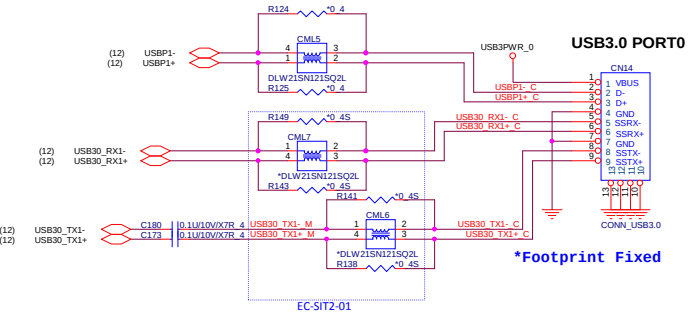
PROJECT : LI8
Quanta Computer Inc.

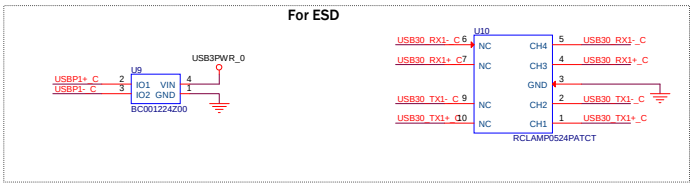
Size	Document Number	Rev
	Wifi/BT NGFF	1A

Date: Monday, November 09, 2015 Sheet 24 of 43

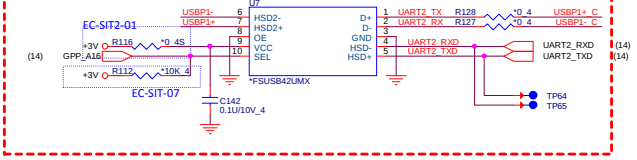
USB 3.0 Port L-side



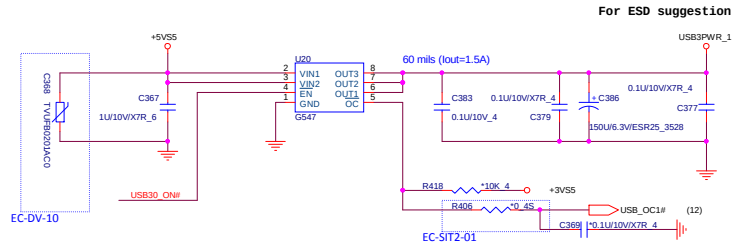


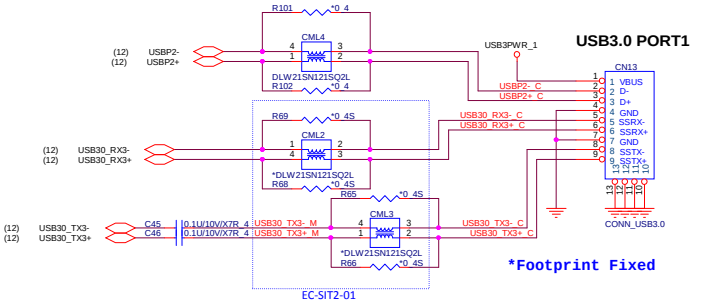


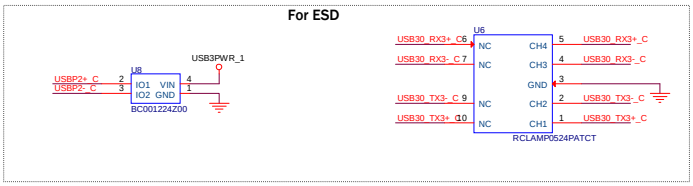
UART for DEBUG



USB 3.0 Port R-side



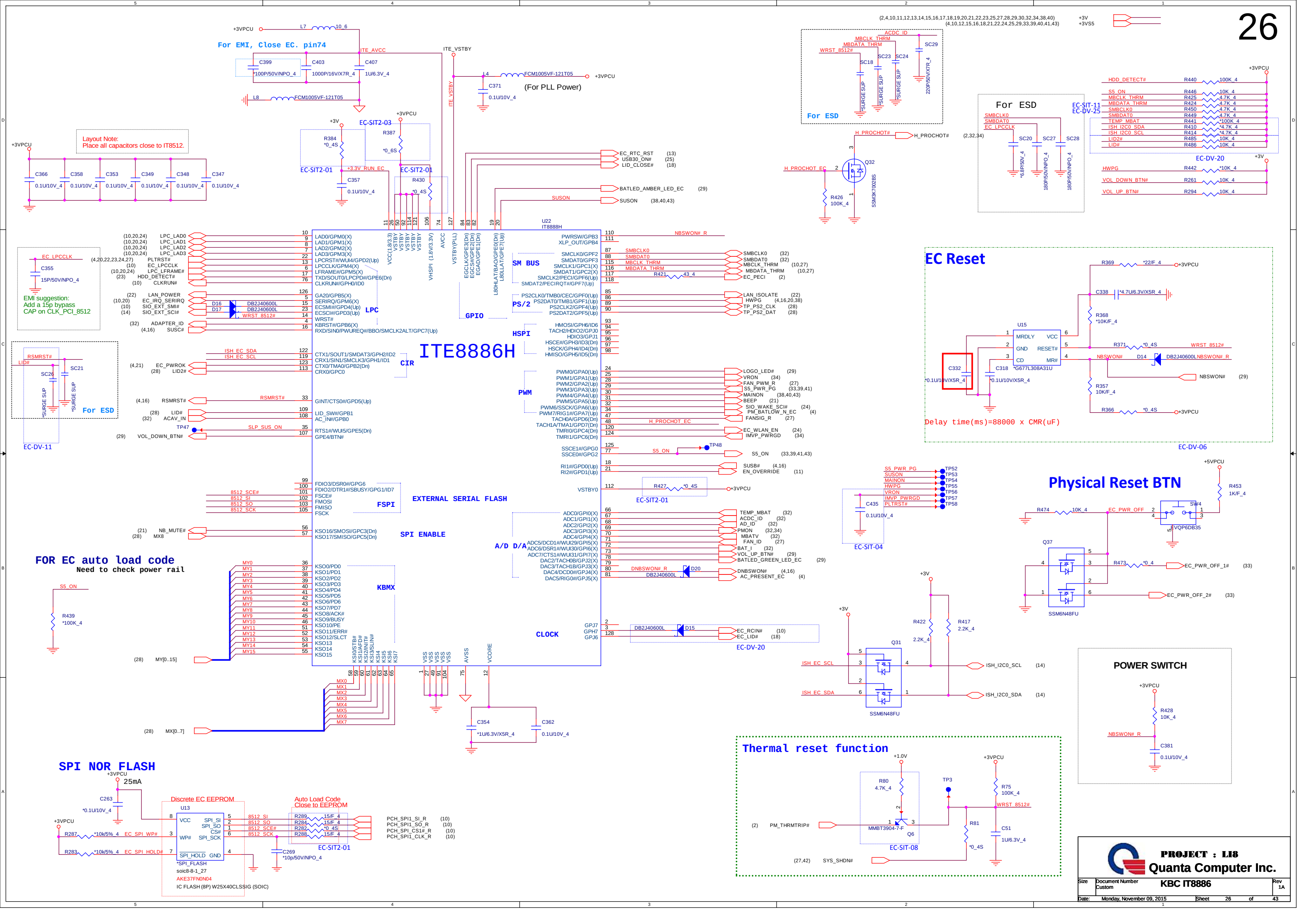




PROJECT : LI8
Quanta Computer Inc.

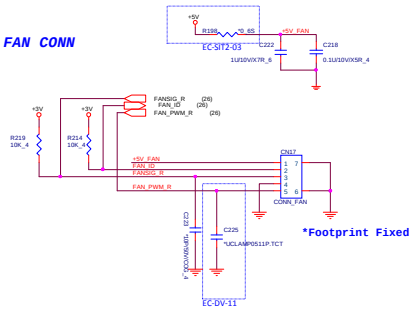
Size	Document Number	Rev
	USB2.0/USB3.0	1A

Date: Monday, November 09, 2015 Sheet 25 of 43



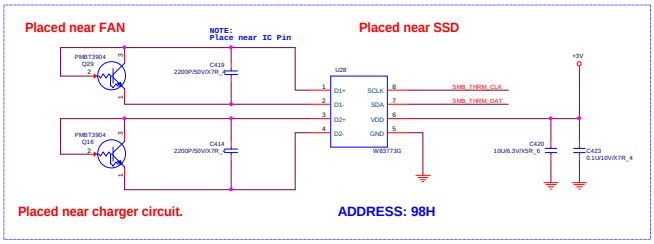
26
For EMI, Close EC. pin74
(For PLL Power)
Layout Note:
Place all capacitors close to IT8512.
For ESD
EC Reset
Delay time(ms)=88000 x CMR(uF)
Physical Reset BTN
ITE8886H
U22
IT8888H
LPC
CIR
GPIO
SM BUS
PS/2
HSPI
PWM
EXTERNAL SERIAL FLASH
FSPI
SPI ENABLE
A/D D/A
KBMX
CLOCK
EMI suggestion:
Add a 15p bypass
CAP on CLK_PCI_8512
FOR EC auto load code
Need to check power rail
SPI NOR FLASH
25mA
Discrete EC EEPROM
Auto Load Code
Close to EEPROM
IC FLASH (8P) W25X40CLSSIG (SOIC)
Thermal reset function
POWER SWITCH
PROJECT : LI8
Quanta Computer Inc.
KBC IT8886
Monday, November 09, 2015
Sheet 26 of 43

FAN CONN

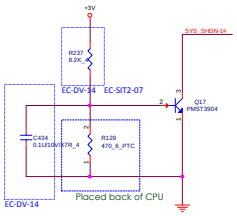


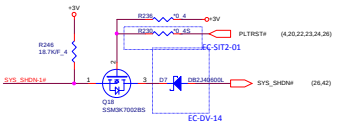
*Footprint Fixed

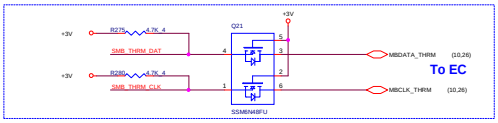
Thermal Sensor



CPU PTC circuit





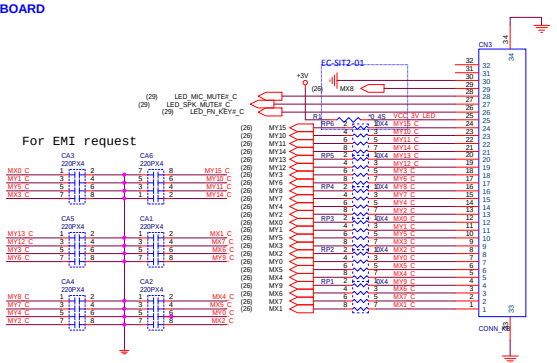


PROJECT : LI8

Quanta Computer Inc.

Size	Document Number	Rev
	FAN/Thermal	1A
Date: Monday, November 09, 2015	Sheet 27 of 43	

KEYBOARD



For EMI request

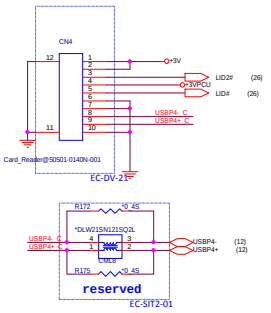
TP Control

(2,4,10,11,12,13,14,15,16,17,18,19,20,21,22,23,25,26,27,29,30,32,34,38,40)

+3V

28

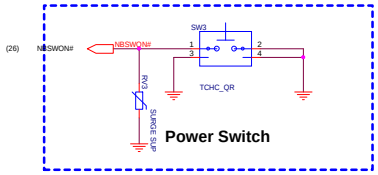
To Card Reader Board



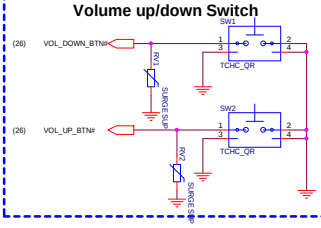
PROJECT : LI8			
Quanta Computer Inc.			
Size	Document Number	KB/TP/DB	Rev 1A
Date: Monday, November 09, 2015	Sheet 28 of 43		

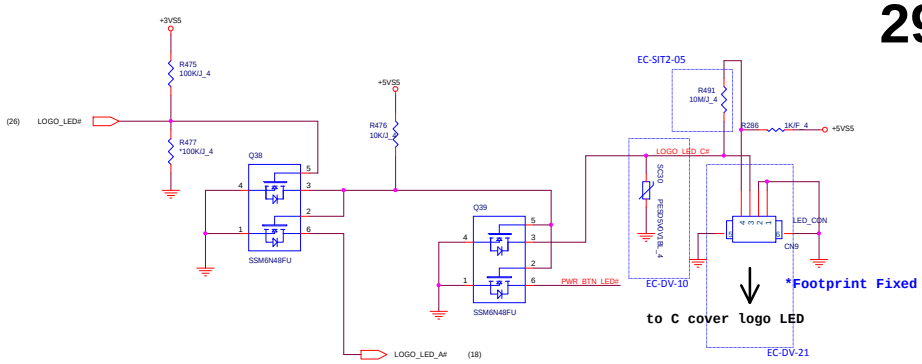
LED Driver

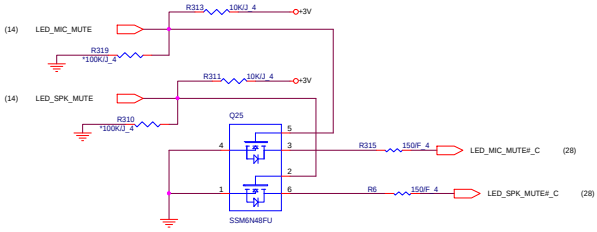
Power Switch

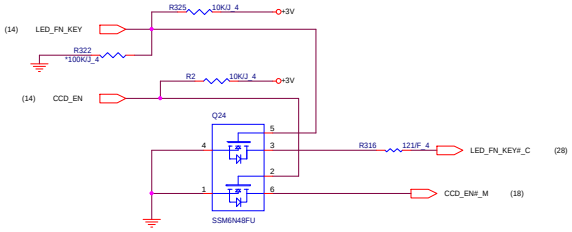


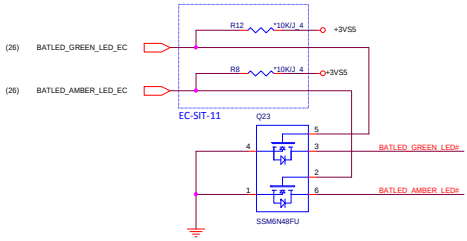
Volume up/down Switch

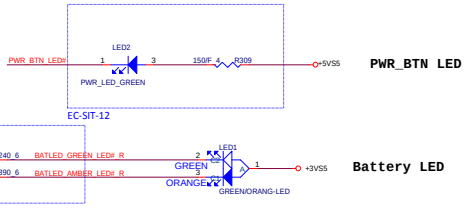




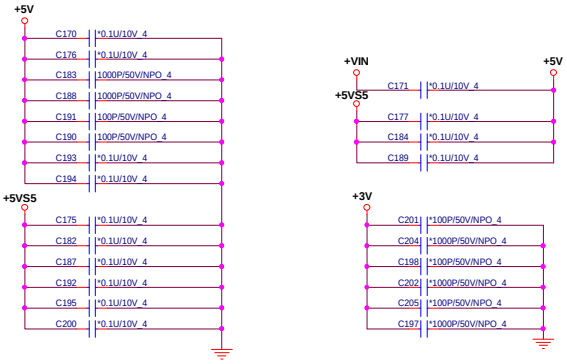








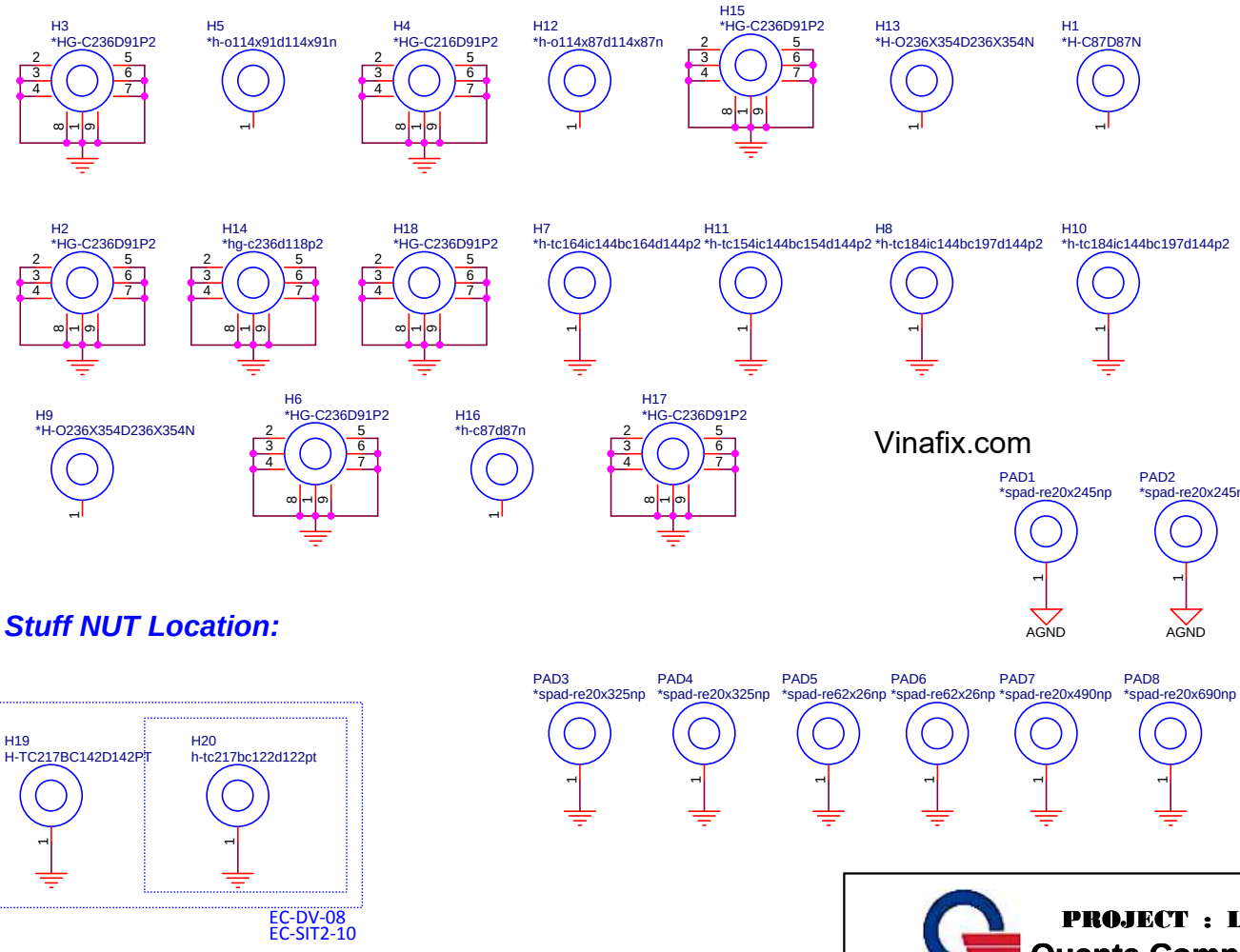
Quanta Computer Inc.	PROJECT : LI8		
Size	Document Number	POWER BUTTON	Rev
	Custom		1A
Date:	Monday, November 09, 2015	Sheet 29 of 43	



PROJECT : LI8

Quanta Computer Inc.

Size	Document Number	Rev
	All Power Good	1A
Date: Monday, November 09, 2015	Sheet 30 of 43	



Stuff NUT Location:

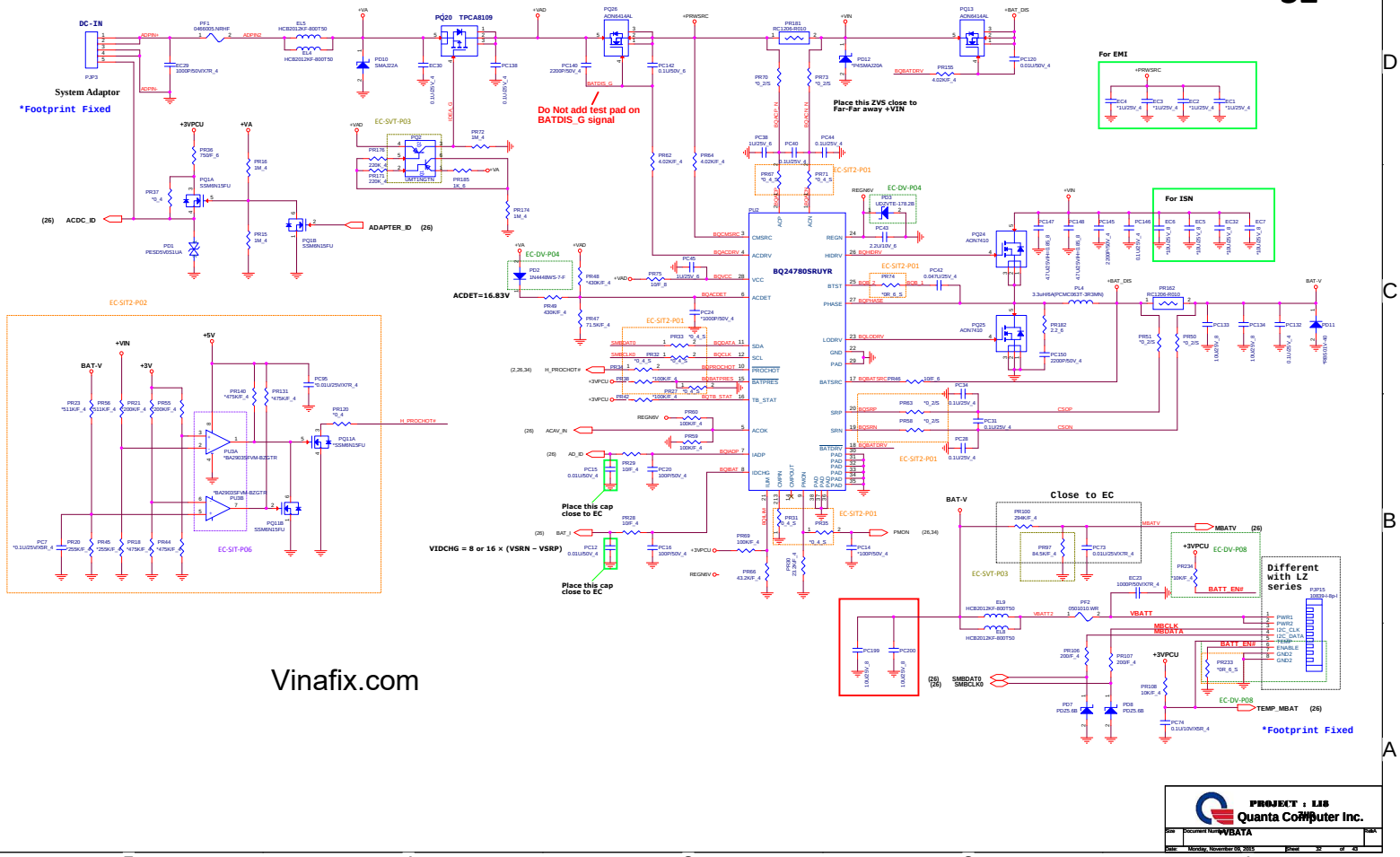
EC-DV-08
EC-SIT2-10

PROJECT : LI8

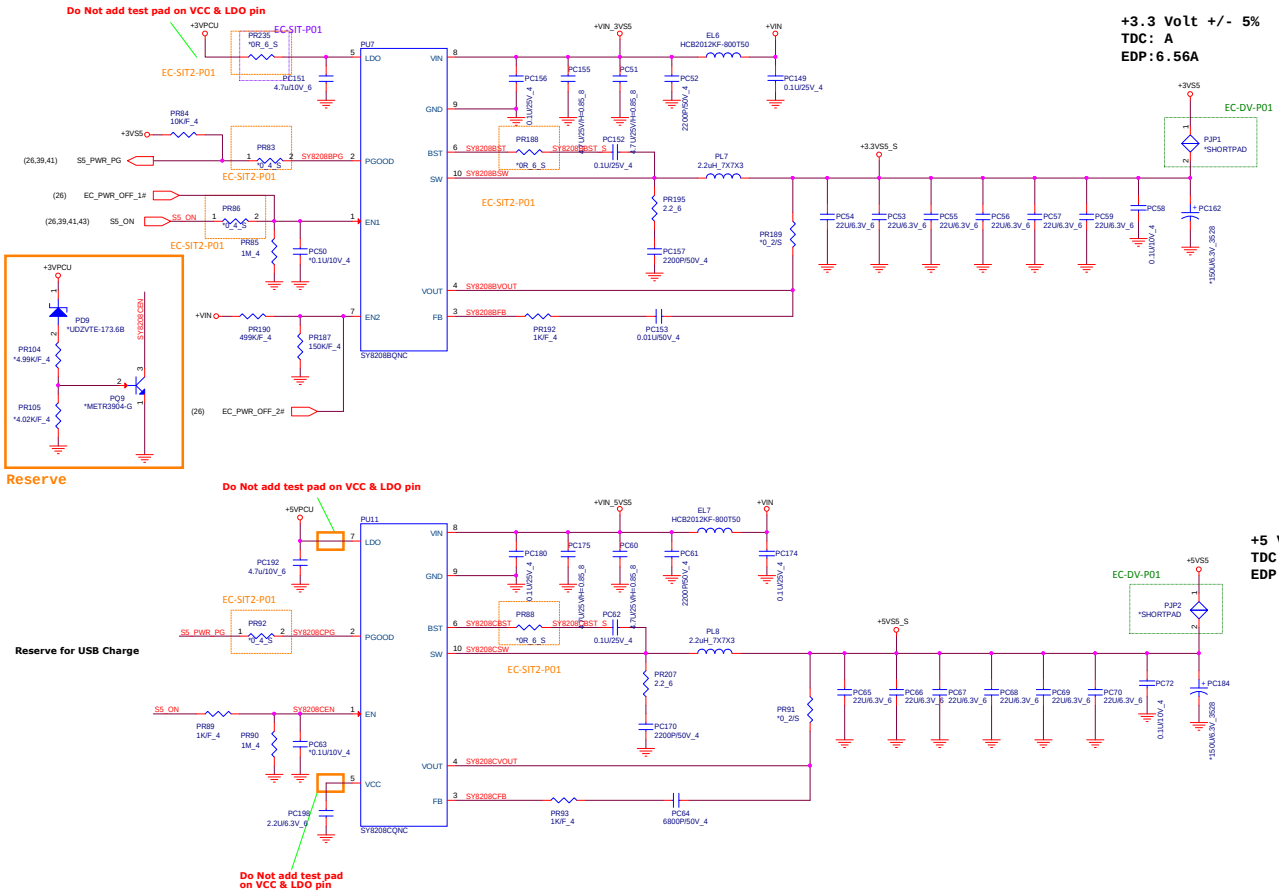
Quanta Computer Inc.

Size	Document Number	Rev
A	**Screw Hole**	1A

Date: Monday, November 09, 2015 Sheet 31 of 43



PROJECT : LI8
Quanta Computer Inc.
PBATA
Monday, November 09, 2015



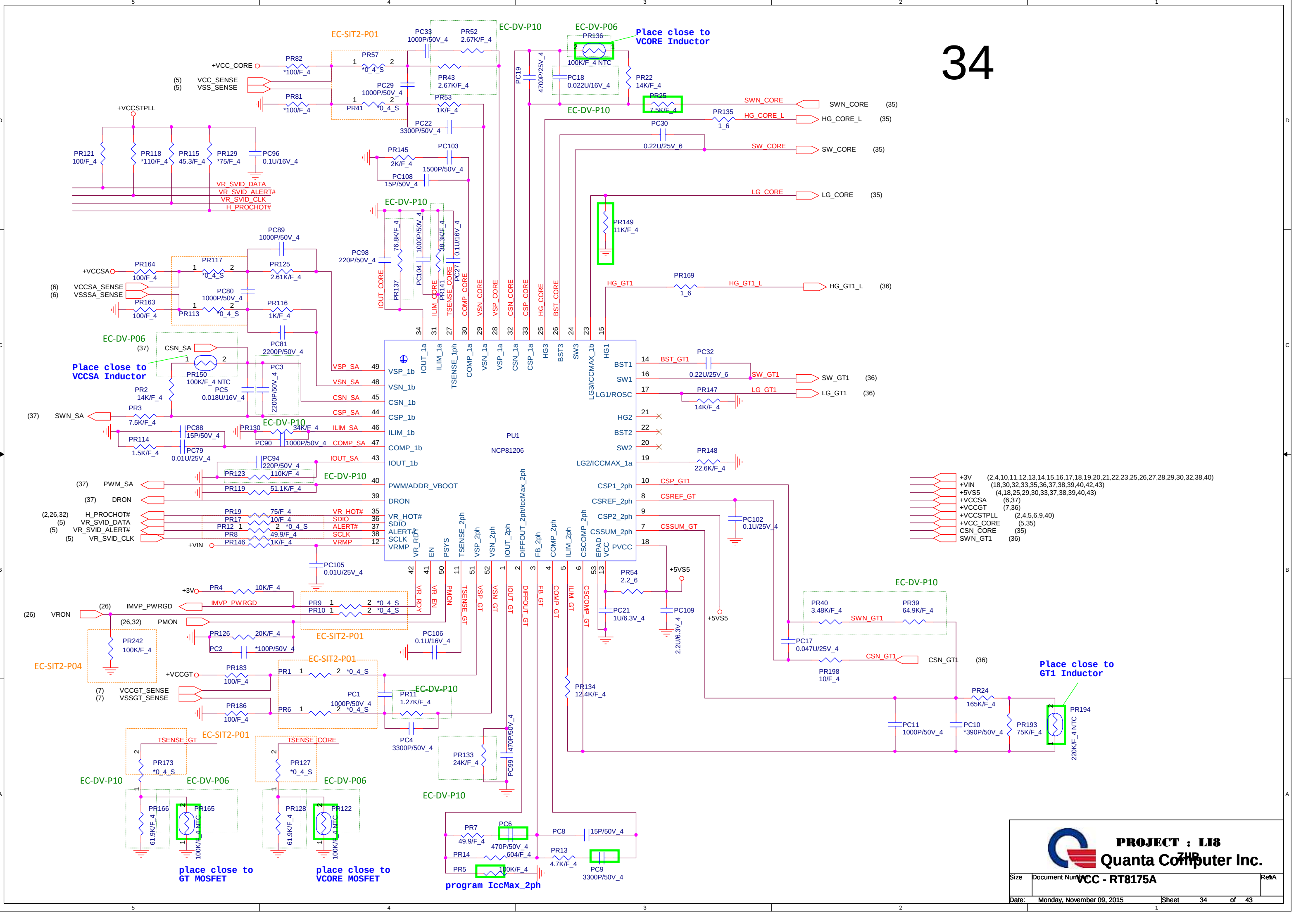
+3.3 Volt +/- 5%
TDC: A
EDP:6.56A

+5 Volt +/- 5%
TDC: A
EDP:4.6A

33

PROJECT : LIS
Quanta Computer Inc.
ZHB

Size	Document Number	Rev
	V5A_V3P3A	A
Date: Monday, November 09, 2015	Sheet 33 of 43	


Place close to VCORE Inductor
Place close to VCCSA Inductor
Place close to GT1 Inductor
place close to GT MOSFET
place close to VCORE MOSFET
program IccMax_2ph
EC-SIT2-P01
EC-DV-P10
EC-DV-P06
EC-SIT2-P04
PU1
NCP81206
+VCC_CORE
VCC_SENSE
VSS_SENSE
+VCCSTPLL
VR_SVID_DATA
VR_SVID_ALERT#
VR_SVID_CLK
H_PROCHOT#
+VCCSA
VCCSA_SENSE
VSSSA_SENSE
CSN_SA
SWN_SA
PWM_SA
DRON
+VIN
IMVP_PWRGD
VRON
PMON
+VCCGT
VCCGT_SENSE
VSSGT_SENSE
TSENSE_GT
TSENSE_CORE
SWN_CORE
HG_CORE_L
SW_CORE
LG_CORE
HG_GT1_L
SW_GT1
LG_GT1
CSN_GT1
SWN_GT1
+5VS5
+3V
VSP_1b
VSN_1b
CSN_1b
CSP_1b
ILIM_1b
COMP_1b
IOUT_1b
PWM/ADDR_VBOOT
DRON
VR_HOT#
SDIO
ALERT#
SCLK
VRMP
BST1
SW1
LG1/ROSC
HG2
BST2
SW2
LG2/ICCMAX_1a
CSP1_2ph
CSREF_2ph
CSP2_2ph
CSSUM_2ph
PVCC
+3V (2,4,10,11,12,13,14,15,16,17,18,19,20,21,22,23,25,26,27,28,29,30,32,38,40)
+VIN (18,30,32,33,35,36,37,38,39,40,42,43)
+5VS5 (4,18,25,29,30,33,37,38,39,40,43)
+VCCSA (6,37)
+VCCGT (7,36)
+VCCSTPLL (2,4,5,6,9,40)
+VCC_CORE (5,35)
CSN_CORE (35)
SWN_GT1 (36)
PROJECT : LI8
Quanta Computer Inc.
VCC - RT8175A
Size
Document Number
Rev
1A
Date: Monday, November 09, 2015
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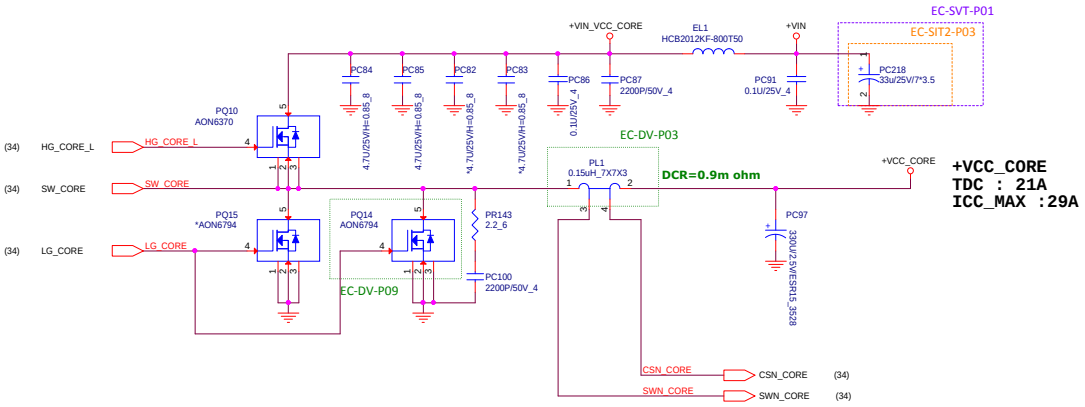

+VCC_CORE
TDC : 21A
ICC_MAX :29A

PROJECT : LI8
ZUP
Quanta Computer Inc.

Size	Document Number	Rev
	VGG - RT8175A	A

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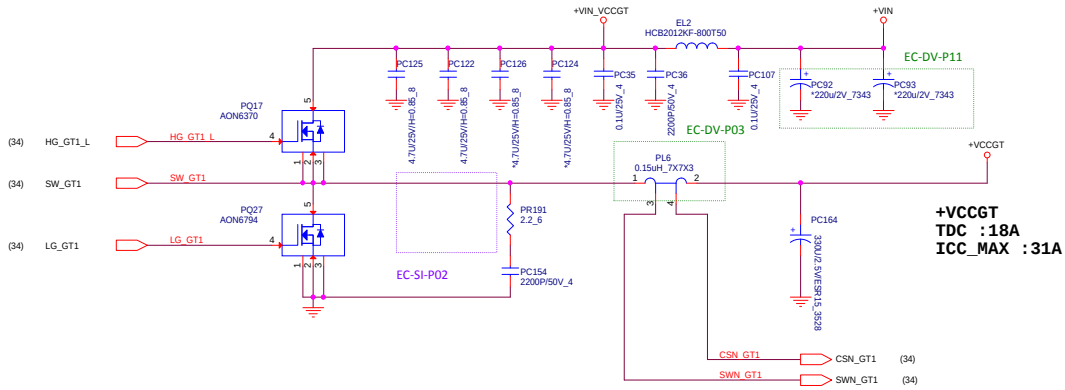
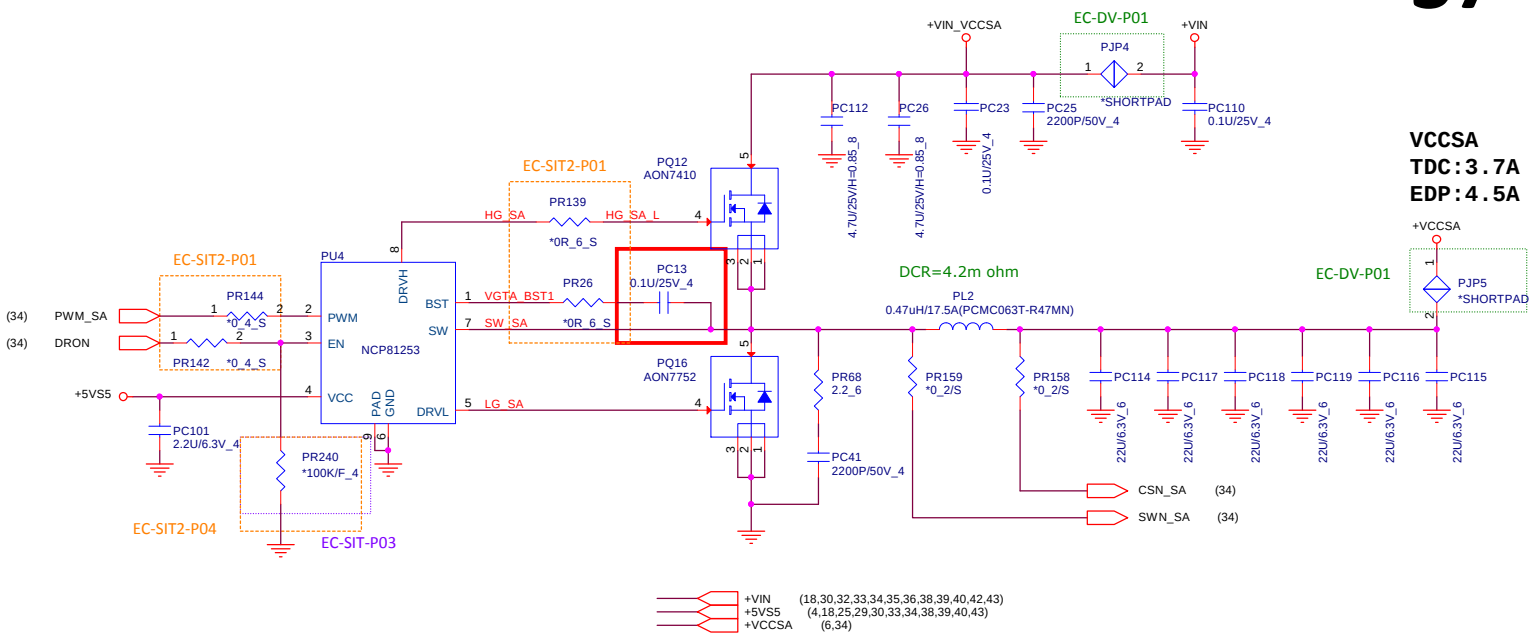

+VIN_VCCGT
EL2
HCB2012KF-800T50
+VIN
EC-DV-P11
PC125
PC122
PC126
PC124
PC35
PC36
PC107
PC92
*220u/2V_7343
PC93
*220u/2V_7343
4.7U/25V/H=0.85_8
4.7U/25V/H=0.85_8
*4.7U/25V/H=0.85_8
*4.7U/25V/H=0.85_8
0.1U/25V_4
2200P/50V_4
0.1U/25V_4
EC-DV-P03
+VCCGT
PQ17
AON6370
PQ27
AON6794
(34) HG_GT1_L
HG_GT1_L
(34) SW_GT1
SW_GT1
(34) LG_GT1
LG_GT1
PL6
0.15uH_7X7X3
PR191
2.2_6
PC154
2200P/50V_4
EC-SI-P02
PC164
330U/2.5V/ESR15_3528
+VCCGT
TDC :18A
ICC_MAX :31A
CSN_GT1
SWN_GT1
CSN_GT1 (34)
SWN_GT1 (34)

VCCSA

37



PROJECT : LI8

Quanta Computer Inc.

CustomDoc <RevCode>

Size	Document Number	Rev

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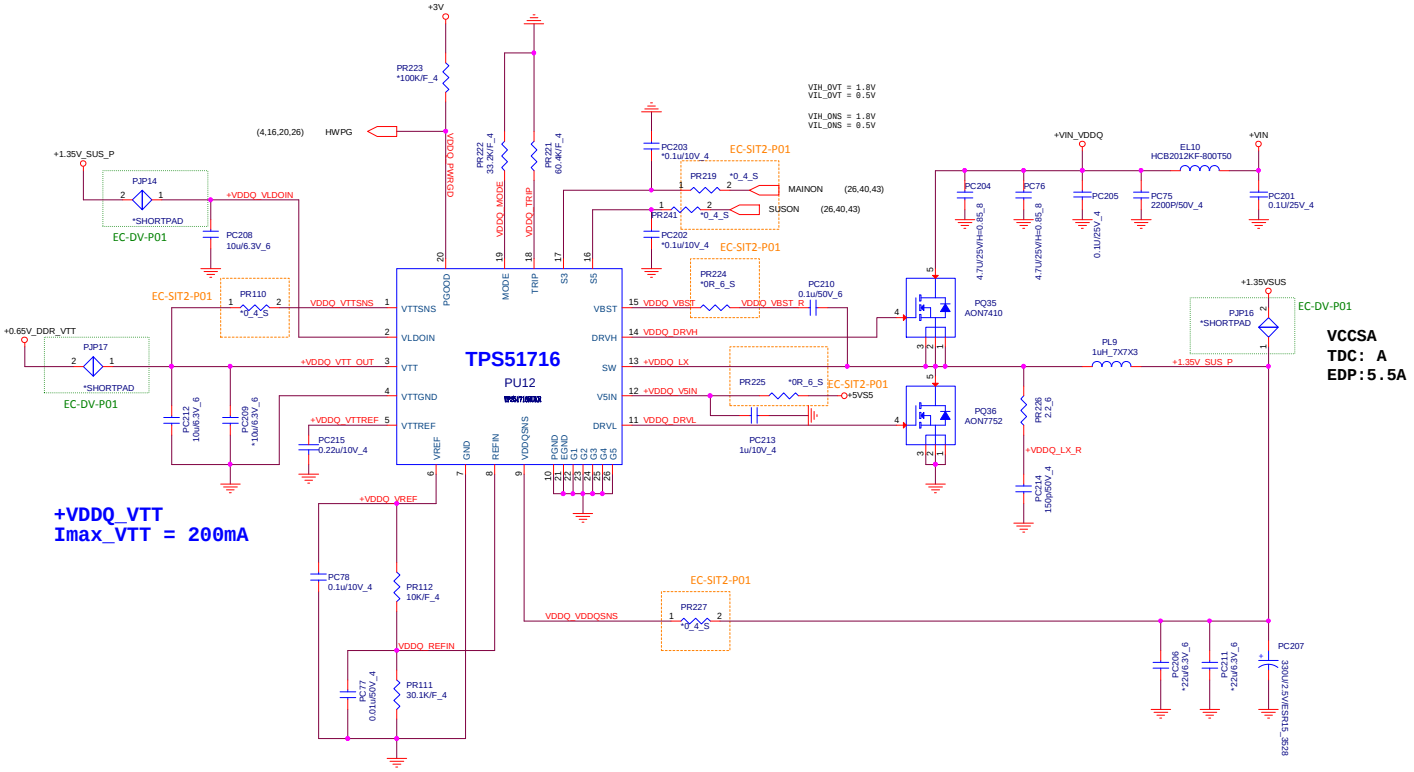
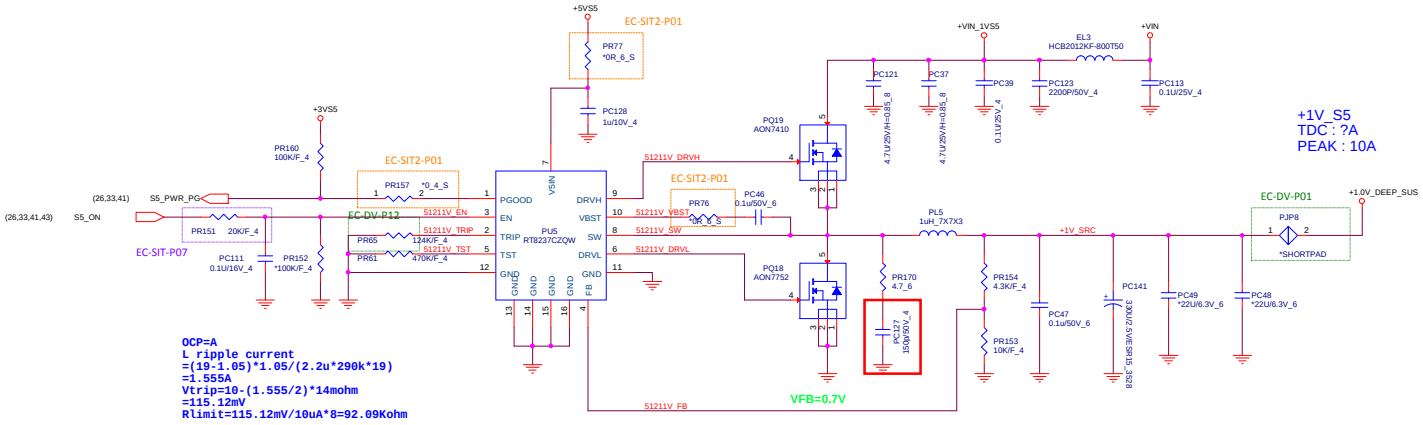
VR PAGE: +VDDQ

Fsw=500kHz



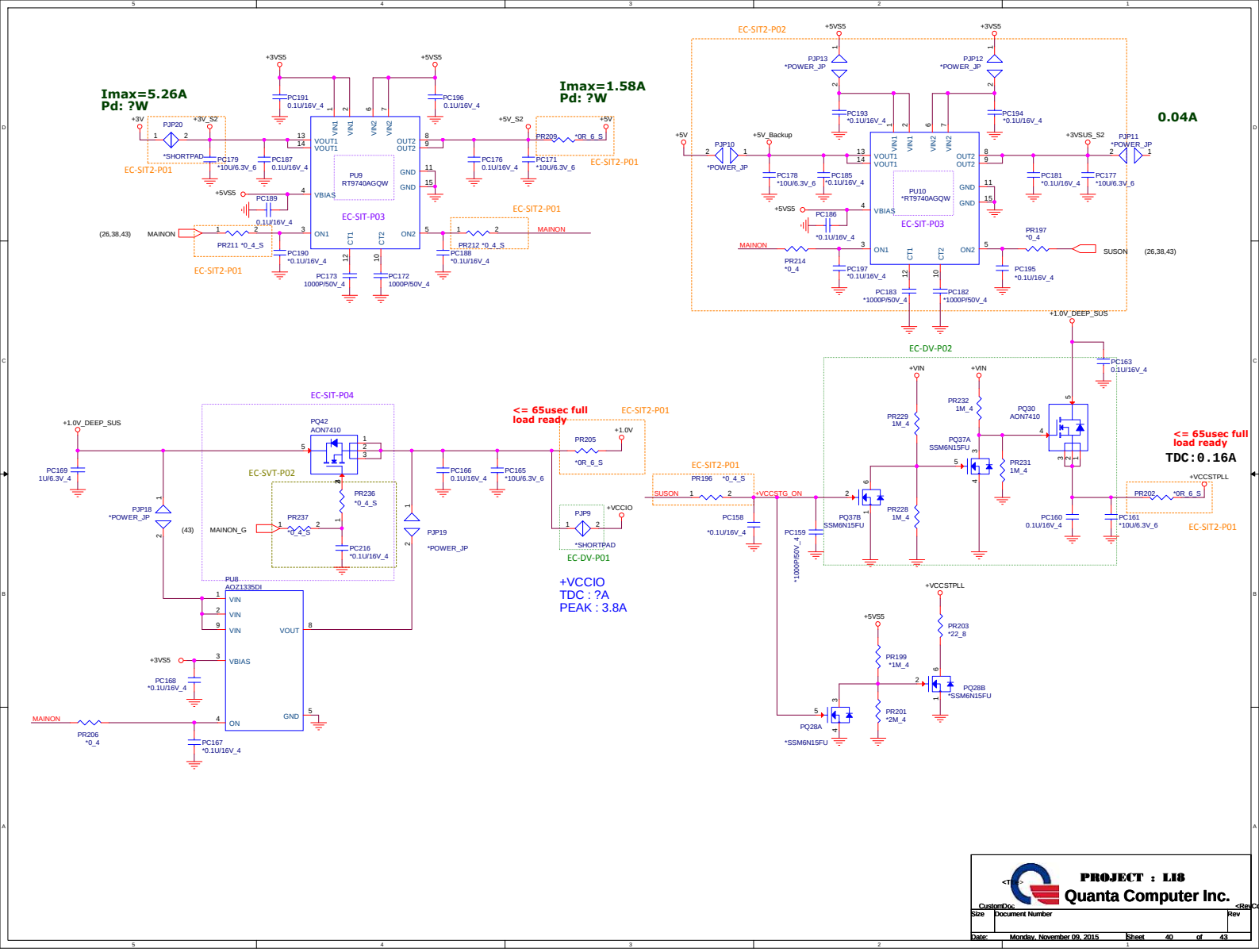
V1P0A (RT8237CZQW)



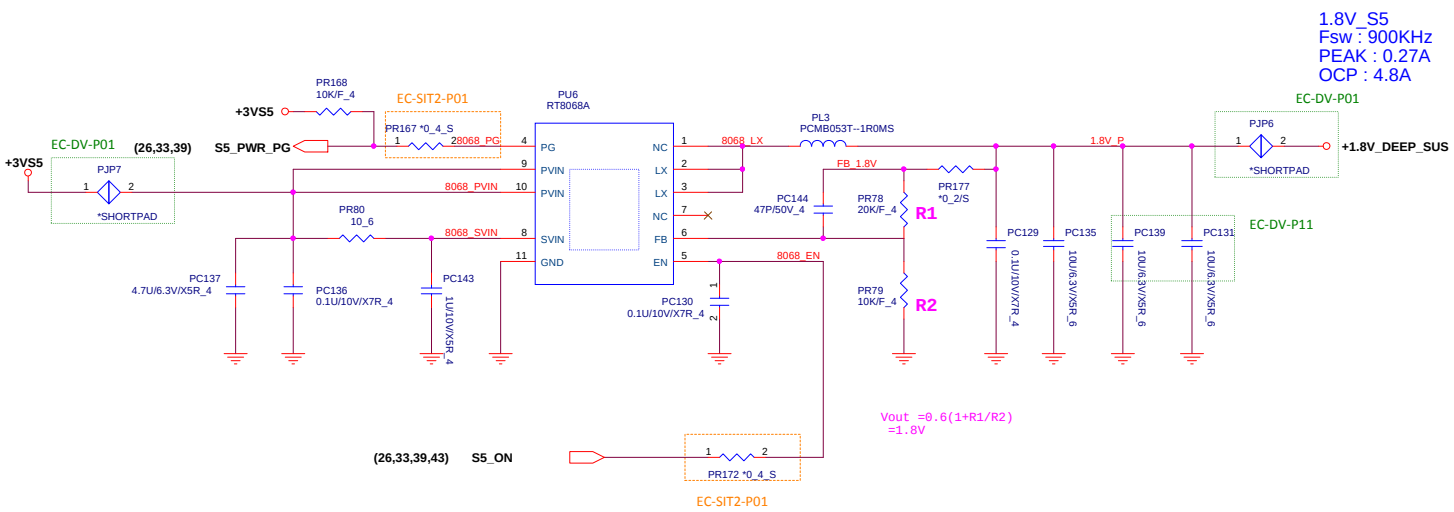
PROJECT : LI8
Quanta Computer Inc.
ZHB

Size	Document Number	MOIC_RT5041A	Rev A
Date: Monday, November 09, 2015	Sheet 39 of 43		

0109 added caps placeholder for S0 power output


Imax=5.26A
Pd: ?W
Imax=1.58A
Pd: ?W
0.04A
EC-SIT2-P02
EC-SIT2-P01
EC-SIT-P03
EC-SIT-P04
EC-SVT-P02
EC-DV-P02
EC-DV-P01
PU9 RT9740AGQW
PU10 *RT9740AGQW
PU8 AOZ1335DI
PQ42 AON7410
PQ30 AON7410
PQ37A SSM6N15FU
PQ37B SSM6N15FU
PQ28A *SSM6N15FU
PQ28B *SSM6N15FU
<= 65usec full load ready
TDC:0.16A
+VCCIO
TDC : ?A
PEAK : 3.8A
PROJECT : LI8
Quanta Computer Inc.
Monday, November 09, 2015
Sheet 40 of 43

V1P8A (RT8068A)



PROJECT : LI8			
Quanta Computer Inc.			
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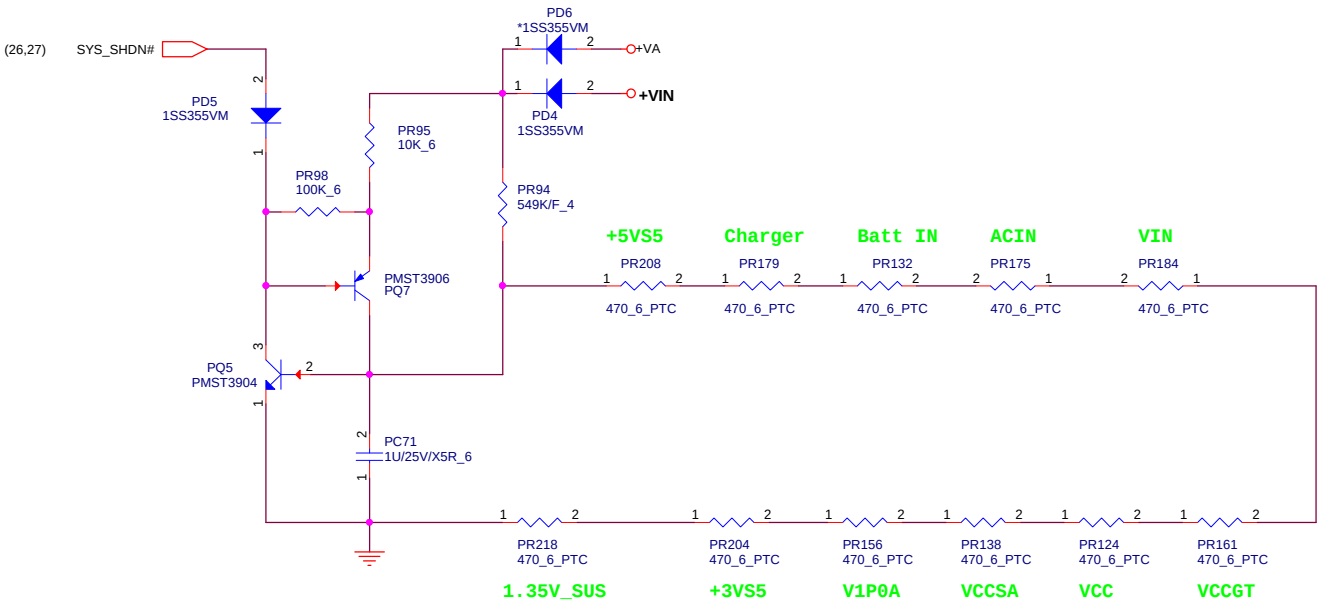

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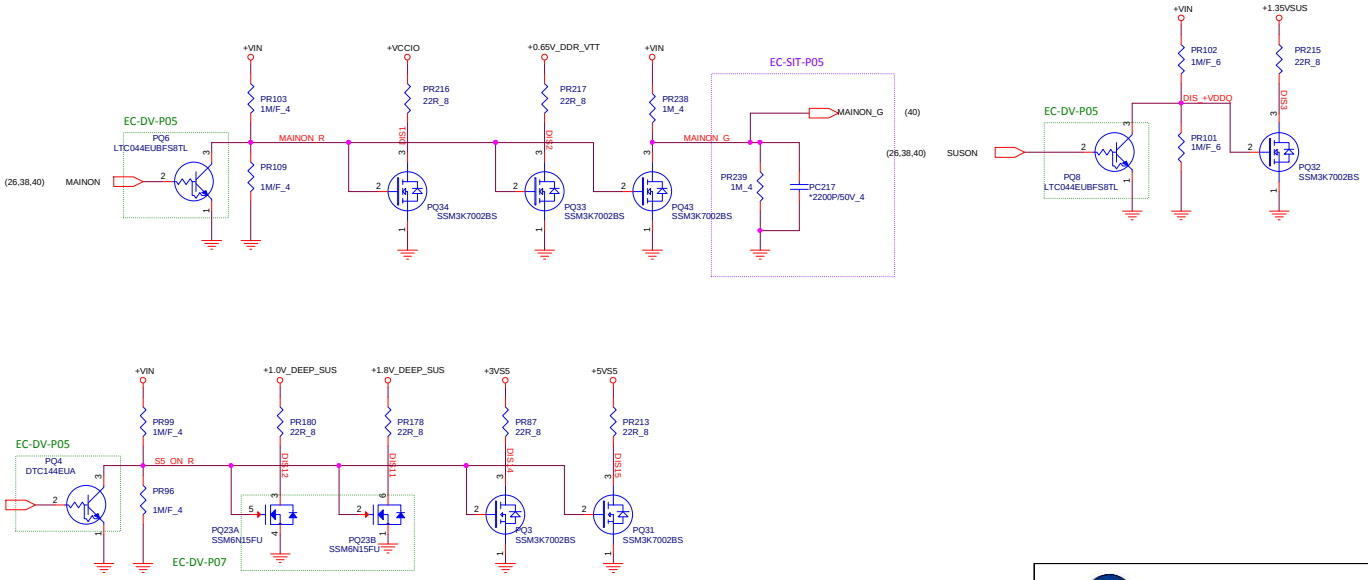

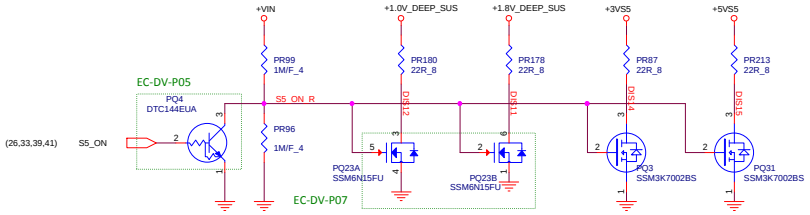

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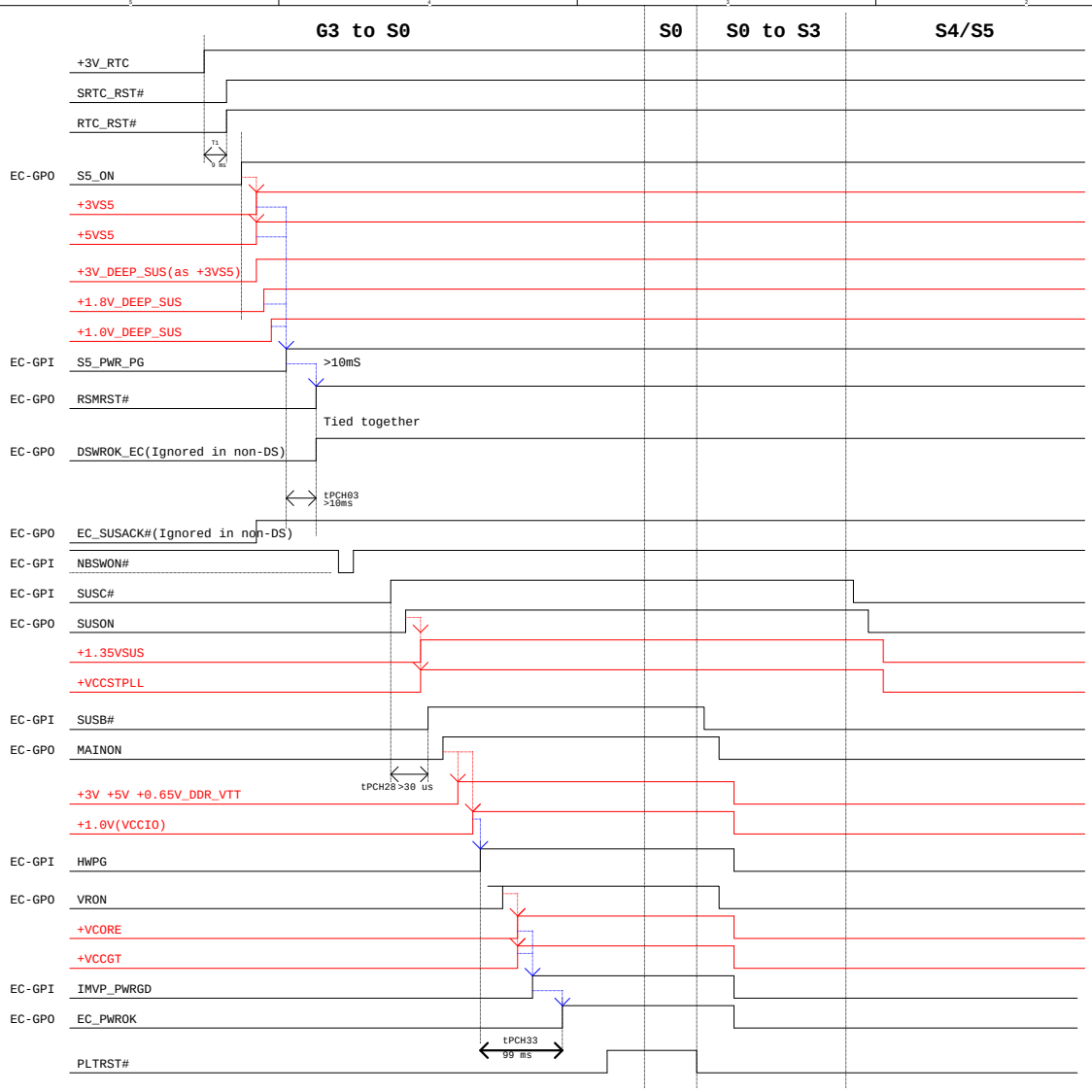

PROJECT : Y62P/Y63P
Quanta Computer Inc.

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	Intel POWER UP SEQUENCE	1A

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LI8E Schematic EC Tracking Record A to B (SDV/FVT Planar) version

EC #	Page	Description	Part Affected
EC-DV-01	18	Change LCD conn type to FPC	CN11
EC-DV-02	22	Modify the LAN power switch soft start.	Q13,R451,R478
EC-DV-03	24	Modify the WLAN power switch soft start.	Q12,R145,R479
EC-DV-04	18	Modify the Touchscreen power switch soft start.	Q8,R123,R480,C144
EC-DV-05	18	Modify the CCD power switch soft start.	R302,R314,R481,C302
EC-DV-06	26	Cancel the EC reset IC for cost saving	U15,C338,C332,R369
EC-DV-07	13	Change to popular value of resistance	R308
EC-DV-08	31	Change Nut to big one	H19,H20
EC-DV-09	16	Remove the surpluse reserved part	U27
EC-DV-10	18,19,21, 22,25,29	Change ESD solution	TOP: SRV1,SRV2,SRV3,SRV4,C172,C229,SC6,SC8,SC4,SC5,SC1,SC2,SC3 BOT: C404,C368,EC31,SRV5,C415,C416,SC30,SRV6
EC-DV-11	21,26,27	Remove the surpluse ESD part	C225,C235,C236,SC26
EC-DV-12	28	Reserve footprint for ESD	RV4,RV5,RV6,RV7
EC-DV-13	17	Stuff for EMI solution	EC22,EC18,EC15,EC25,EC20,EC14,EC26,EC24,EC19, EC12,EC13,EC11, EC21,EC16,EC27,EC28
EC-DV-14	27	Fine tune the thermistor citciuit.	C434,D7,R237
EC-DV-15	10	Modify the LPC_CLK path.	Del:R173,EC10 Add:R482
EC-DV-16	20	Add pull down RES and reserve pull up RES	R483,R484
EC-DV-17	19	Modify the HDMI ESD routing	U1,U2
EC-DV-18	18	Modify the Touchscreen power state to +3V	Q8,R123,R480,C144,Q9,R100
EC-DV-19	07,05	Change Cap height to H=0.9	C131,C110,C95,C66,C102,C103,C109,C307,C306,C125,C90,C89,C124, C108
EC-DV-20	18,26	Change backlight path pass through EC.	R485,R486
EC-DV-21	28,29	FFC connector to Koycera new type	CN5,CN4,CN9
EC-DV-22	21	Change RES value for PCBEEP issue	R247,R248
EC-DV-23	4	Change transistor source to avoid single source issue. and meet ECSL.	Q4
EC-DV-24	20	Remove RFID EEPROM due to virtual RFID implementation	U12,R260,C250,R274,D8,D9
EC-DV-25	26	Stuff ISH to EC I2C pull up resistor.	R410,R414

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EC Record A to B
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LI6J Power Schematic EC Tracking Record B to C version(SDV/FVT Planar)

EC #	Page	Description	Part Affected
EC-DV-P01	33,37,41,38,39,40	Change short pad	PJP1,PJP2,PJP4,PJP5,PJP6,PJP7,PJP8,PJP9,PJP14,PJP16,PJP17
EC-DV-P02	40	For Combustion Test	PQ37A,PQ37B,PQ30,PR228,PR229,PR231,PR232
EC-DV-P03	35,36	ME height limit change choke high degree	PL1,PL6
EC-DV-P04	32	Follow ECSL change diode vendor	PD2,PD3
EC-DV-P05	43	Follow ECSL change diode vendor	PQ4,PQ6,PQ8
EC-DV-P06	34	Follow ECSL change diode vendor	PR122,PR136,PR150,PR165
EC-DV-P07	43	Save layout space	PQ23A,PQ23B
EC-DV-P08	32	Customer request reserve	PR234
EC-DV-P09	35	CPU MOS bom change	PQ14
EC-SIT-P01	33	Add debug res	PR235
EC-SIT-P02	36	Remove MOS for placement	PQ22
EC-SIT-P03	40	Follow ECSL	PU9,PU10
EC-SIT-P04	40	Add MOS for ECSL	PQ42,PR236,PR237,PC216
EC-SIT-P05	37	Reserved debug res	PR240
EC-SIT-P06	32	Change package for placement	PU3
EC-SIT-P07	39	For sequence request	PR151
EC-SIT2-P01	32 ~ 41	Change 0 ohm to short pad	PR235,PR188,PR86,PR83,PR88,PR92,PR9,PR10,PR1,PR6,PR173,PR127 PR113,PR117,PR12,PR57,PR41,PR144,PR139,PR26,PR142,PR224,PR110 PR227,PR219,PR241,PR225,PR77,PR76,PR157,PR209,PR202,PR211 PR212,PR172,PR167,PR33,PR32,PR34,PR67,PR71,PR74,PR58,PR63,PR35 PR31,PR27,PR233,PR205 change to PJP20
EC-SIT2-P02	32,40	Remove reserve parts	PC193,PC194,PU10,PC185,PC181,PC186,PC183,PC182,PU8,PC168 PR206,PR23,PR56,PR21,PR55,PR140,PR131,PC95,PU3,PQ11,PC7,PR20 PR45,PR18,PR44
EC-SIT2-P03	35	Add Vin cap	PC218
EC-SIT2-P04	34,37	Remove PR240(100K) and add PR242(100K)	PR240,PR242

LI8E Schematic EC Tracking Record B to C (SIT Planar) version

EC #	Page	Description	Part Affected
EC-SIT-01	10	Add ME/BIOS Pull up resistor for CS# signal	R487,R488(Reserved)
EC-SIT-02	10	Remove surplus EMI capacitor.	C92
EC-SIT-03	04	Reserved pull up resistor in LAN_WAKE# on SoC.	R489(Reserved)
EC-SIT-04	26	Add capacitor in VRON to reduce to glitch	C435
EC-SIT-05	02	Remove the R360 to solve leakage issue	R360
EC-SIT-06	10	Change pull up resistor power state to 3VS5 to solve leakage issue	R403(Reserved)
EC-SIT-07	25	Remove surplus pull up resistor for leakage solving.	R112
EC-SIT-08	21	Change L6 footprint from 0603 to 0402	L6
EC-SIT-09	18	Change LCD_VCC solution for ECSL	U18,R490
EC-SIT-10	18	Change 0 ohm to fuse for combustion test	F1,F2,F3,F6
EC-SIT-11	29	Remove surplus pull up RES	R8,R12,R410,R414
EC-SIT-12	29	Remove Power LED feature	LED2,R309
EC-SIT-13	28	Add EMI solution.	RV4,RV5
EC-SIT-14	13	Fine tune crystal accuracy	C329,C344,C388,C397
EC-SIT-15	13	Change 32.768Khz source for Intel 50kohm request.	Y3
EC-SIT-16	19	Add EMI solution for HDMI.	R323,R328,R331,R333
EC-SIT-17	29	Fine fune the brightness for DC-IN LED	R312,R318

LI8E Schematic EC Tracking Record C to D (SIT-R Planar) version

EC #	Page	Description	Part Affected
EC-SIT2-01	All	Change 0 ohm to 0402 shortpad.	BOT: L1,L12,L13,R334,R342,R345,R349,R359,R372,R384,R389,R392,R395,R405,R406,R412,R427,R430,R433,R435,R452,R454,R458 TOP: L2,R1,R22,R23,R27,R28,R29,R30,R34,R65,R66,R68,R69,R84,R87,R91,R104,R106,R109,R110,R116,R122,R135,R136,R138,R139,R141,R143,R146,R149,R154,R155,R159,R167,R172,R174,R175,R176,R180,R182,R183,R184,R186,R187,R190,R205,R230,R235,R242,R259,R282,R482,R483
EC-SIT2-02	14	Change ISH path to I2C for G sensor.	R393,R396,R392,R389,R147,R152
EC-SIT2-03	All	Change 0 ohm to 0603 shortpad.	BOT: F9,L15,R317,R320,R355,R387,R415,R420,R455,R460 TOP: F7,R3,R7,R74,R98,R100,R107,R120,R130,R153,R158,R198,R200,R293
EC-SIT2-04	22	Change 0 ohm to 0805 shortpad.	BOT: R434; TOP:R239
EC-SIT2-05	29	Reserved a high reisitance res for LED broken preventation	R491
EC-SIT2-06	12	USB2_ID and USB2_VBUSSENS tied to GND for Intel design guide requirement.	R492,R493
EC-SIT2-07	27	Fine tune the thermal protection.	R237
EC-SIT2-08	26	Stuff the THRMTRIP# path for thermal protection	Q6,R80
EC-SIT2-09	24	Change the enable path for WLAN power enable.	D4,R494
EC-SIT2-10	31	Change nut for SSD.	H20

LI8E Schematic EC Tracking Record C to D (SIT-R Planar) version

EC #	Page	Description	Part Affected
EC-SVT-01	14	remove the 0 ohm(ISH to Bosch solution)	R205
EC-SVT-02	21	Change resistor value for audio fine tuning	R461,R468
EC-SVT-03	18	Change shortpad fo 0 ohm	R100
EC-SVT-04	14	Reserved 0 ohm in ISH solution path	R389,R392
EC-SVT-05	24	Change 0 ohm to shortpad	R494
EC-SVT-06	26	Reserved 0402 Cap for charger	R436

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Quanta Computer Inc.
EC Record A to B

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LI8B Power Schematic EC Tracking Record C2 to D version(SVT Planar)

EC #	Page	Description	Part Affected
EC-SVT-P01	35	Change FOOTPRINT	PC218
EC-SVT-P02	40	Change FOOTPRINT TO SHORT PAD	PR236,PR237
EC-SVT-P03	32	Change P/N FOR ECSL	PQ2
EC-SVT-P04	32	Change P/N FOR EC CHECK BATTERY VOLTAGE	PR97

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Quanta Computer Inc.
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EC Record A to B (power)
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