Project Name :GK5MPFX
Platform : CML-H+N18P-G62

M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

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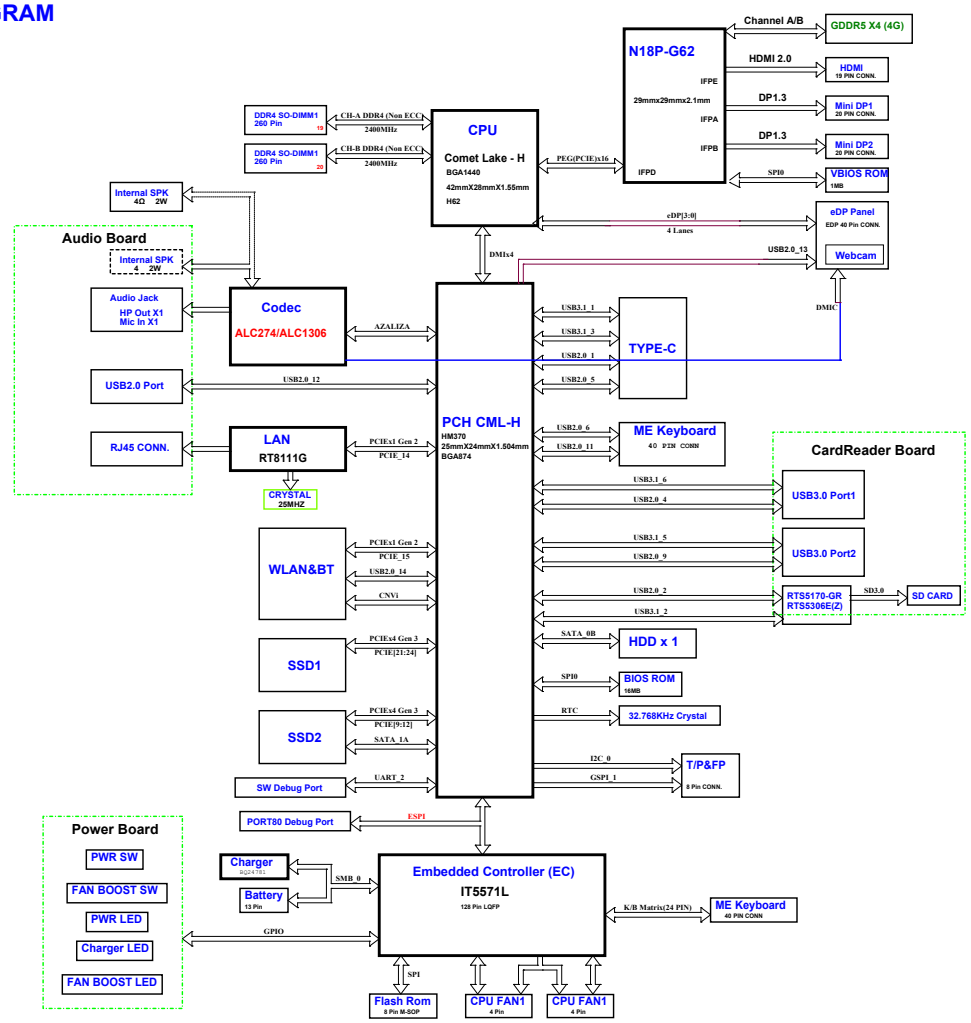
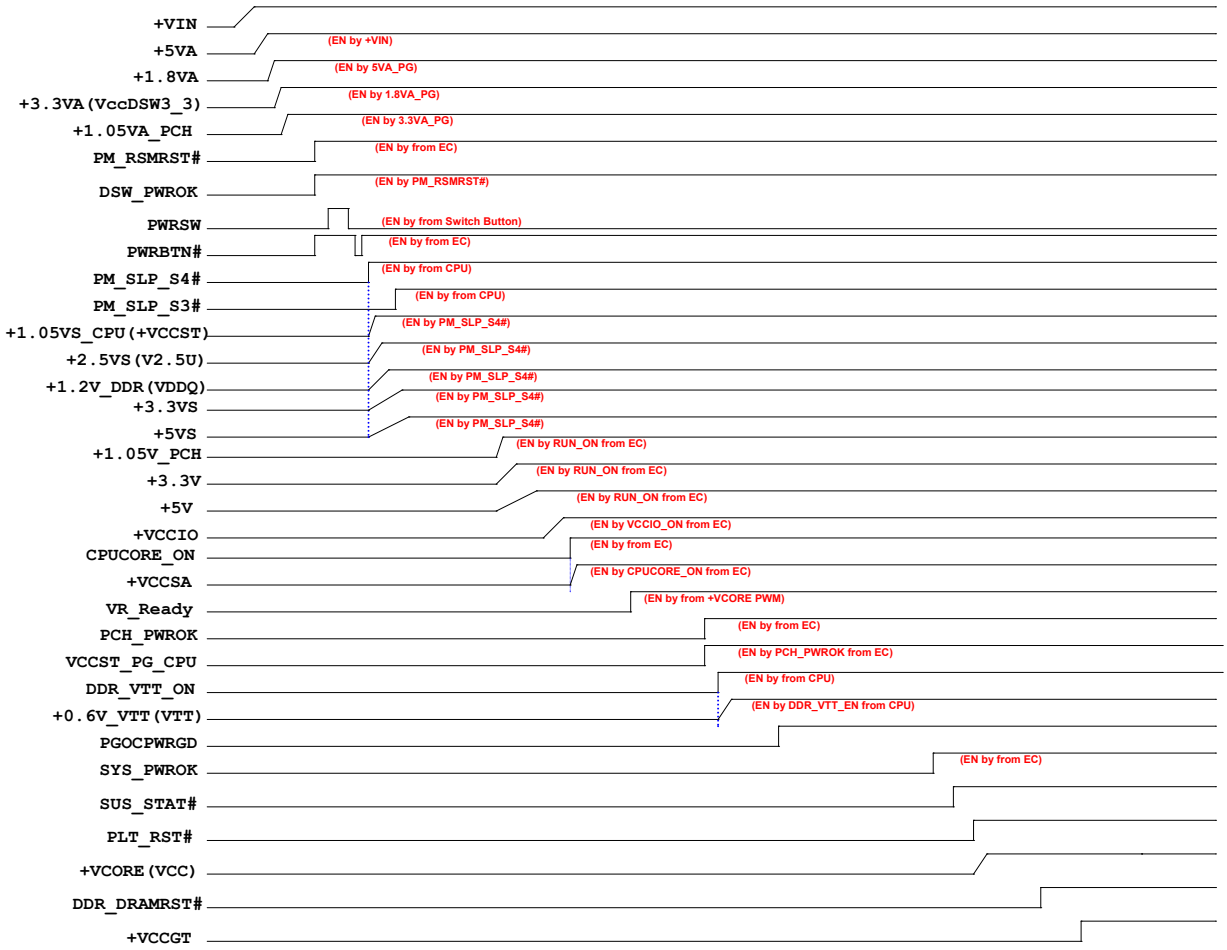
SYSTEM BLOCK DIAGRAM



SYSTEM BLOCK

GK5MPFX

POWER ON SEQUENCE



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Title: POWER SEQUENCE		
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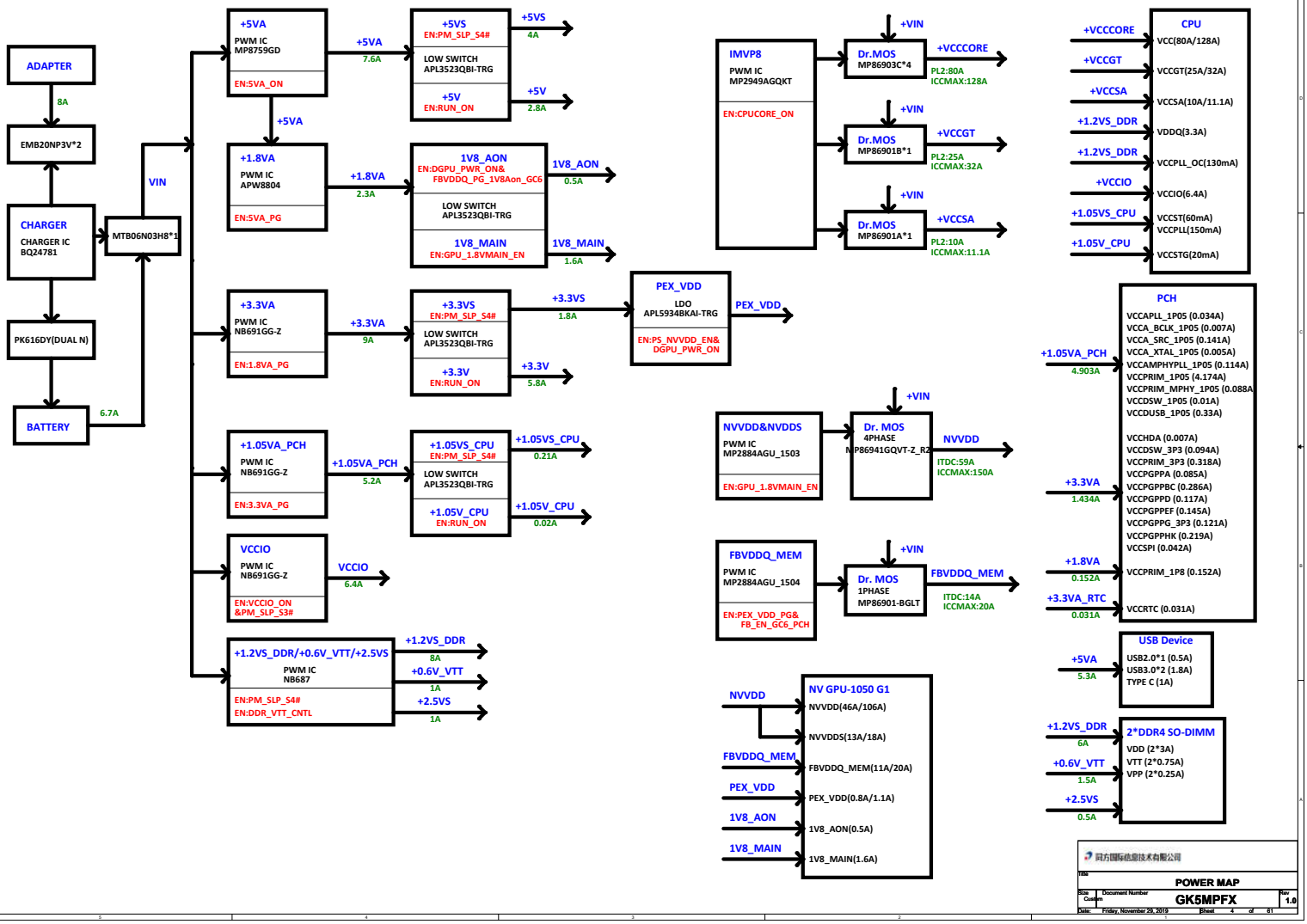
ADAPTER
8A
EMB20NP3V*2
CHARGER
CHARGER IC
BQ24781
PK616DY(DUAL N)
BATTERY
6.7A
MTB06N03H8*1
VIN
+5VA
PWM IC
MP8759GD
EN:5VA_ON
+5VA
7.6A
+5VS
EN:PM_SLP_S4#
LOW SWITCH
APL3523QBI-TRG
+5V
EN:RUN_ON
+5VS
4A
+5V
2.8A
+1.8VA
PWM IC
APW8804
EN:5VA_PG
+1.8VA
2.3A
1V8_AON
EN:DGPU_PWR_ON&
FBVDDQ_PG_1V8Aon_GC6
LOW SWITCH
APL3523QBI-TRG
1V8_MAIN
EN:GPU_1.8VMAIN_EN
1V8_AON
0.5A
1V8_MAIN
1.6A
+3.3VA
PWM IC
NB691GG-Z
EN:1.8VA_PG
+3.3VA
9A
+3.3VS
EN:PM_SLP_S4#
LOW SWITCH
APL3523QBI-TRG
+3.3V
EN:RUN_ON
+3.3VS
1.8A
+3.3V
5.8A
PEX_VDD
LDO
APL5934BKAI-TRG
EN:PS_NVVDD_EN&
DGPU_PWR_ON
PEX_VDD
+1.05VA_PCH
PWM IC
NB691GG-Z
EN:3.3VA_PG
+1.05VA_PCH
5.2A
+1.05VS_CPU
EN:PM_SLP_S4#
LOW SWITCH
APL3523QBI-TRG
+1.05V_CPU
EN:RUN_ON
+1.05VS_CPU
0.21A
+1.05V_CPU
0.02A
VCCIO
PWM IC
NB691GG-Z
EN:VCCIO_ON
&PM_SLP_S3#
VCCIO
6.4A
+1.2VS_DDR/+0.6V_VTT/+2.5VS
PWM IC
NB687
EN:PM_SLP_S4#
EN:DDR_VTT_CNTL
+1.2VS_DDR
8A
+0.6V_VTT
1A
+2.5VS
1A
IMVP8
PWM IC
MP2949AGQKT
EN:CPUCORE_ON
+VIN
Dr.MOS
MP86903C*4
+VCCCORE
PL2:80A
ICCMAX:128A
+VIN
Dr.MOS
MP86901B*1
+VCCGT
PL2:25A
ICCMAX:32A
+VIN
Dr.MOS
MP86901A*1
+VCCSA
PL2:10A
ICCMAX:11.1A
NVVDD&NVDDS
PWM IC
MP2884AGU_1503
EN:GPU_1.8VMAIN_EN
+VIN
Dr. MOS
4PHASE
MP86941GQVT-Z_R2
NVVDD
ITDC:59A
ICCMAX:150A
FBVDDQ_MEM
PWM IC
MP2884AGU_1504
EN:PEX_VDD_PG&
FB_EN_GC6_PCH
+VIN
Dr. MOS
1PHASE
MP86901-BGLT
FBVDDQ_MEM
ITDC:14A
ICCMAX:20A
NVVDD
FBVDDQ_MEM
PEX_VDD
1V8_AON
1V8_MAIN
NV GPU-1050 G1
NVVDD(46A/106A)
NVVDDS(13A/18A)
FBVDDQ_MEM(11A/20A)
PEX_VDD(0.8A/1.1A)
1V8_AON(0.5A)
1V8_MAIN(1.6A)
CPU
VCC(80A/128A)
VCCGT(25A/32A)
VCCSA(10A/11.1A)
VDDQ(3.3A)
VCCPLL_OC(130mA)
VCCIO(6.4A)
VCCST(60mA)
VCCPLL(150mA)
VCCSTG(20mA)
+VCCCORE
+VCCGT
+VCCSA
+1.2VS_DDR
+1.2VS_DDR
+VCCIO
+1.05VS_CPU
+1.05V_CPU
PCH
VCCAPLL_1P05 (0.034A)
VCCA_BCLK_1P05 (0.007A)
VCCA_SRC_1P05 (0.141A)
VCCA_XTAL_1P05 (0.005A)
VCCAMPHYPLL_1P05 (0.114A)
VCCPRIM_1P05 (4.174A)
VCCPRIM_MPHY_1P05 (0.088A)
VCCDSW_1P05 (0.01A)
VCCDUSB_1P05 (0.33A)
VCCHDA (0.007A)
VCCDSW_3P3 (0.094A)
VCCPRIM_3P3 (0.318A)
VCCPGPPA (0.085A)
VCCPGPPBC (0.286A)
VCCPGPPD (0.117A)
VCCPGPPEF (0.145A)
VCCPGPPG_3P3 (0.121A)
VCCPGPPHK (0.219A)
VCCSPI (0.042A)
VCCPRIM_1P8 (0.152A)
VCCRTC (0.031A)
+1.05VA_PCH
4.903A
+3.3VA
1.434A
+1.8VA
0.152A
+3.3VA_RTC
0.031A
USB Device
USB2.0*1 (0.5A)
USB3.0*2 (1.8A)
TYPE C (1A)
+5VA
5.3A
2*DDR4 SO-DIMM
VDD (2*3A)
VTT (2*0.75A)
VPP (2*0.25A)
+1.2VS_DDR
6A
+0.6V_VTT
1.5A
+2.5VS
0.5A
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Title
POWER MAP
Size
Custom
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GK5MPFX
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Title	CML-H DDR4		
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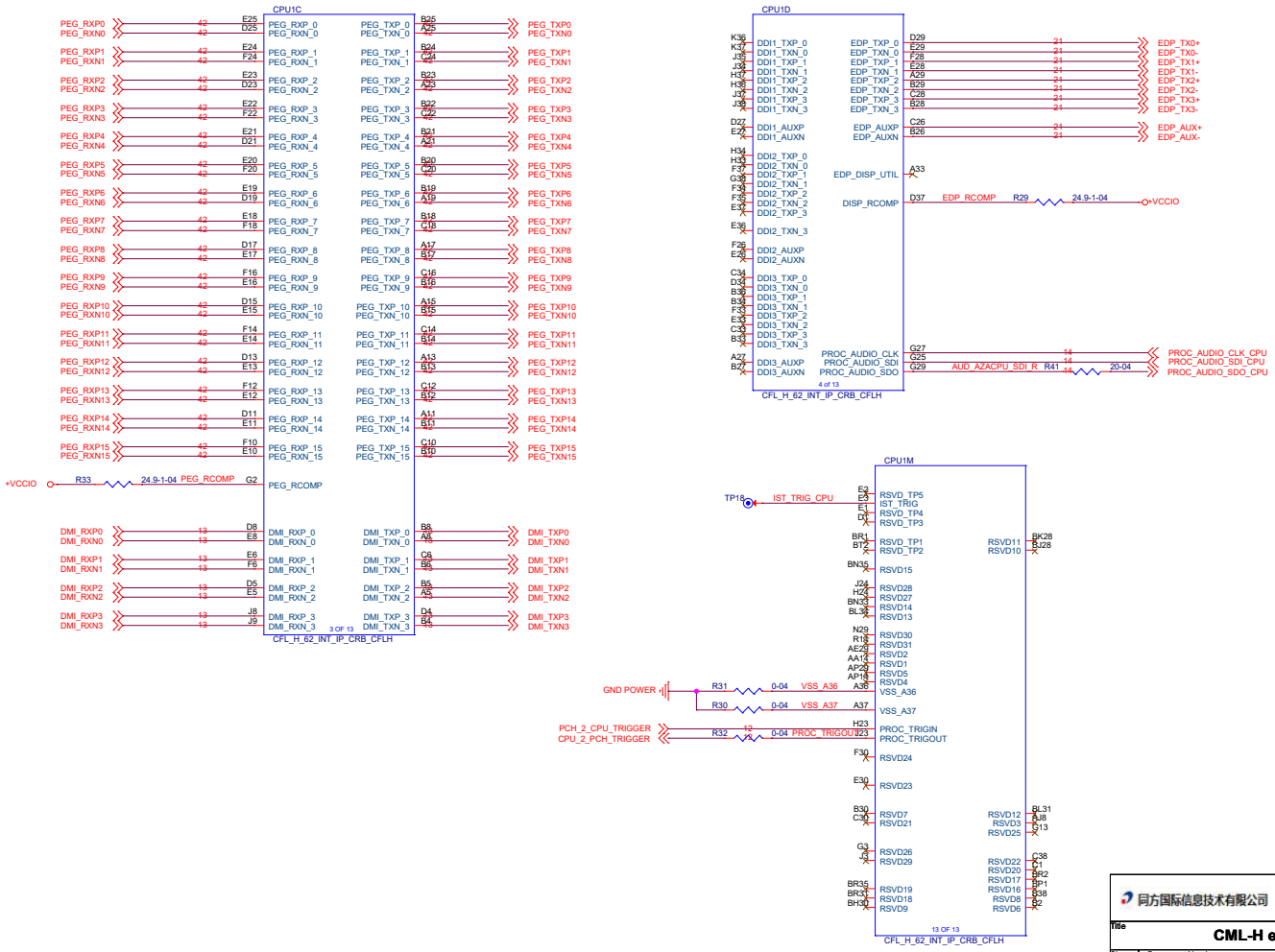

同方国际信息技术有限公司

Title	CML-H eDP/PEX/DMI/RSVD		
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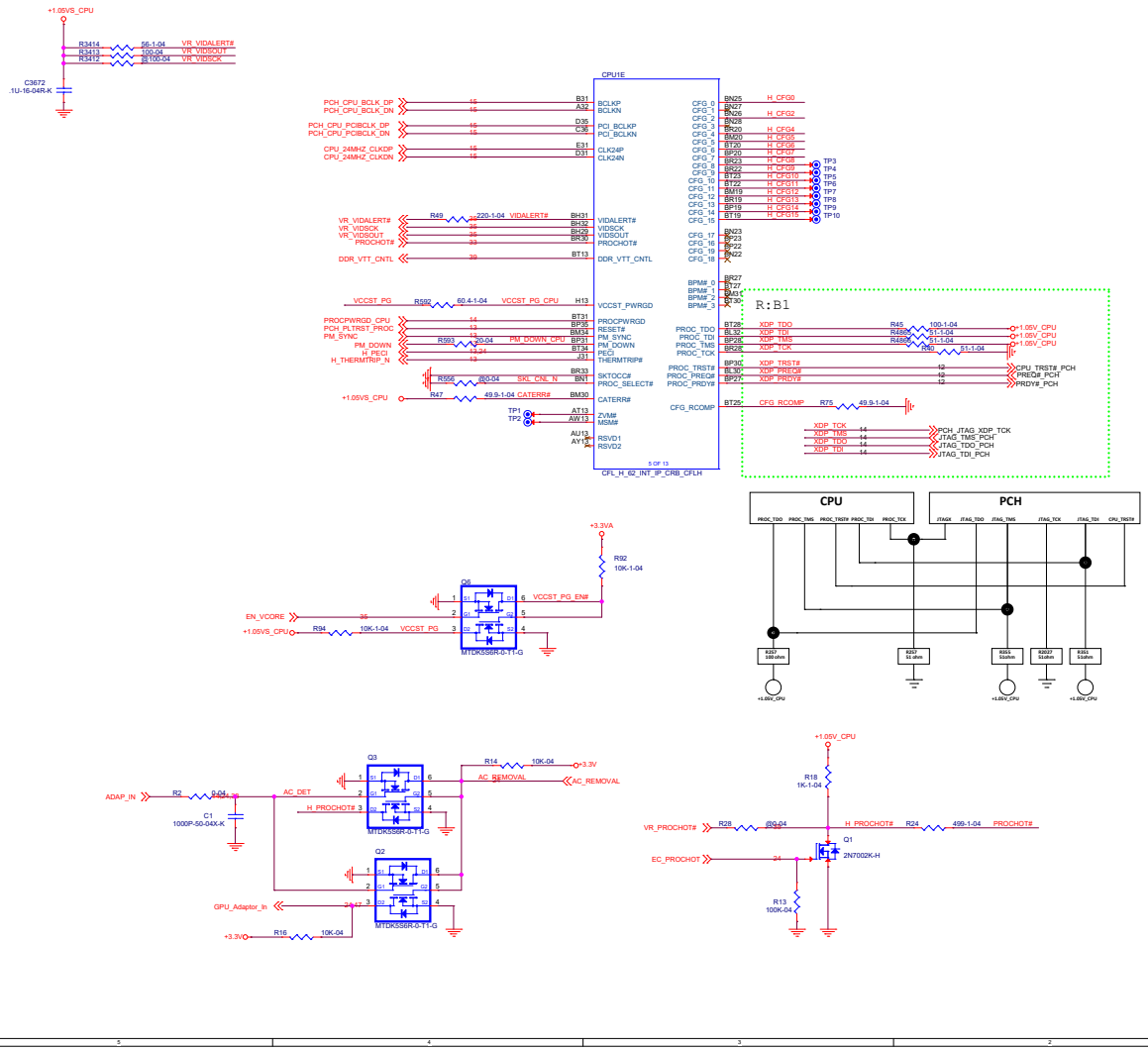

H_CFG0 (iPU)	Stall reset sequence after PCU PLL lock until de-asserted
0	Stall
1	Normal Operation No stall. (Default)

H_CFG0 R180 @1K-1-04

H_CFG2 (iPU)	PCI Express* Static x16 Lane Numbering Reversal
0	Lane numbers reversed
1	Normal operation

H_CFG2 R181 1K-1-04

H_CFG4 (iPU)	eDP Presence strap
0	Enabled
1	Disabled

H_CFG4 R172 1K-1-04

H_CFG6 (iPU)	H_CFG5 (iPU)	PCI Express* Bifurcation
0	0	1 x8, 2 x4 PCI Express
0	1	reserved
1	0	2 x8 PCI Express
1	1	1 x16 PCI Express

H_CFG5 R174 @1K-1-04
H_CFG6 R173 @1K-1-04

H_CFG7 (iPU)	PEG Training
0	PEG Wait for BIOS for training
1	PEG Train immediately following RESET# de assertion (Default)

H_CFG7 R175 @1K-1-04

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Title: CML-H MISC/CLK/JTAG/CFG

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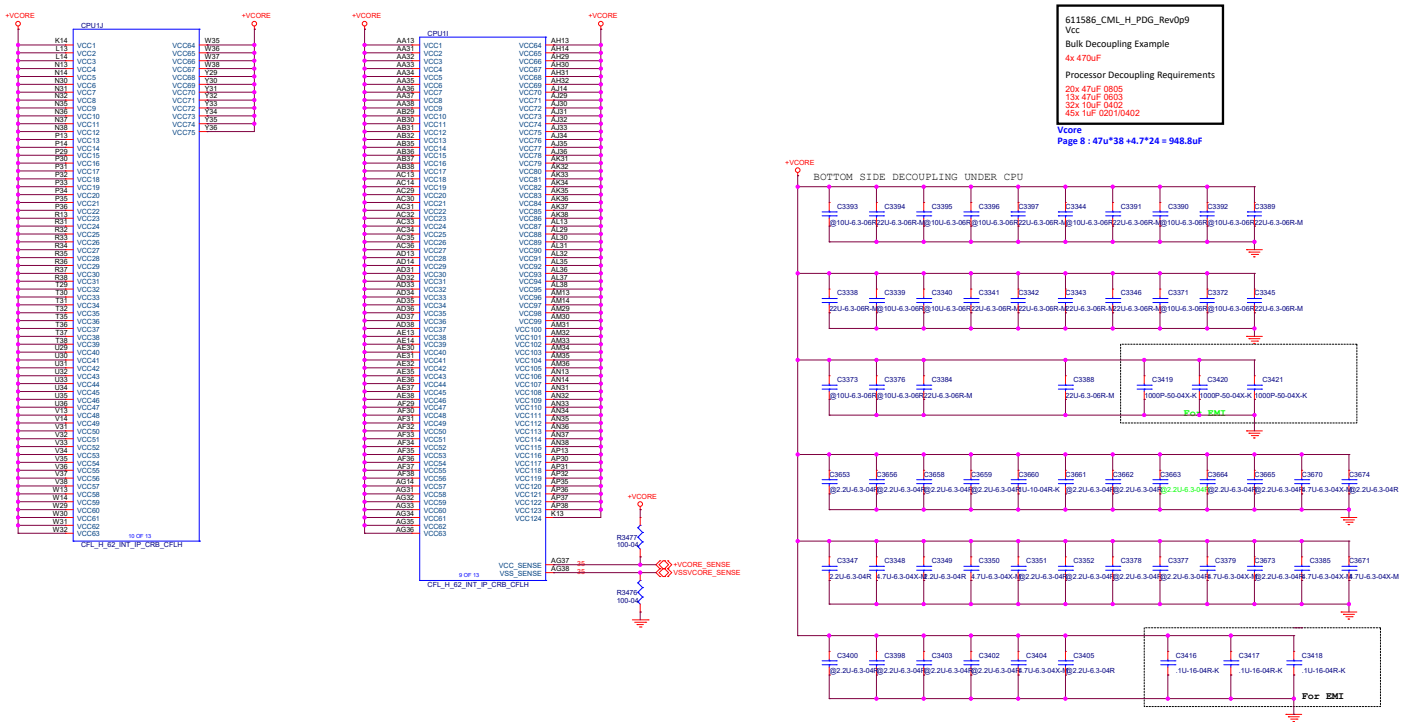

同方国际信息技术有限公司

Title: CML-H VCORE

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611586_CML_H_PDG_Rev0p9
VCCGT

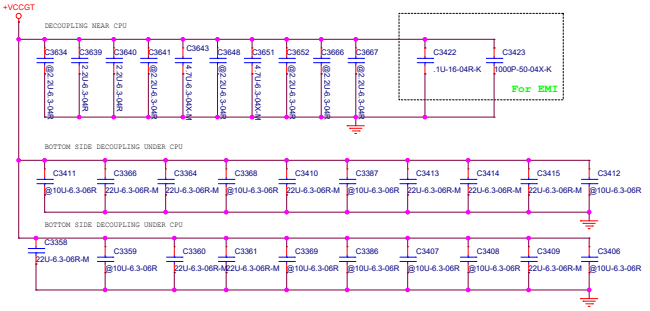
Bulk Decoupling Example

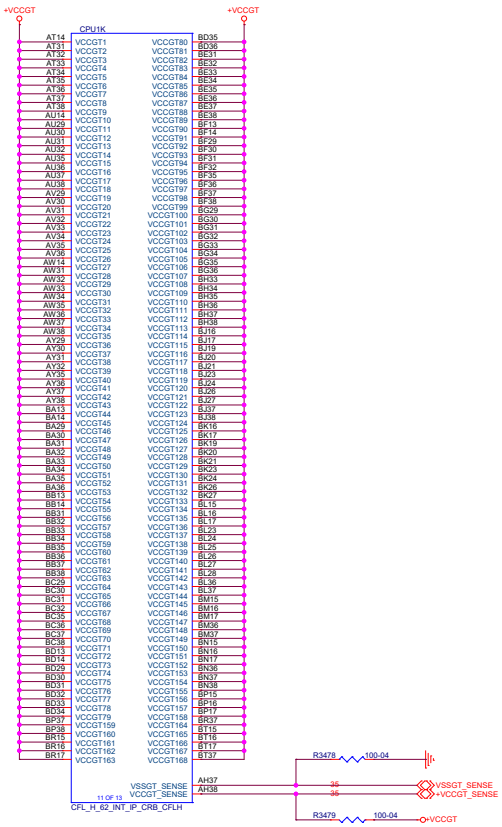
2 x 220uF

Processor Decoupling Requirements

3x 47uF 0805
7x 22uF 0603
10x 10uF 0402
12x 1uF 0201/0402

VccGT
Page 9 : 22u * 20 + 4.7u * 12 = 496.4uF





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Title	CML-H VCCGT	
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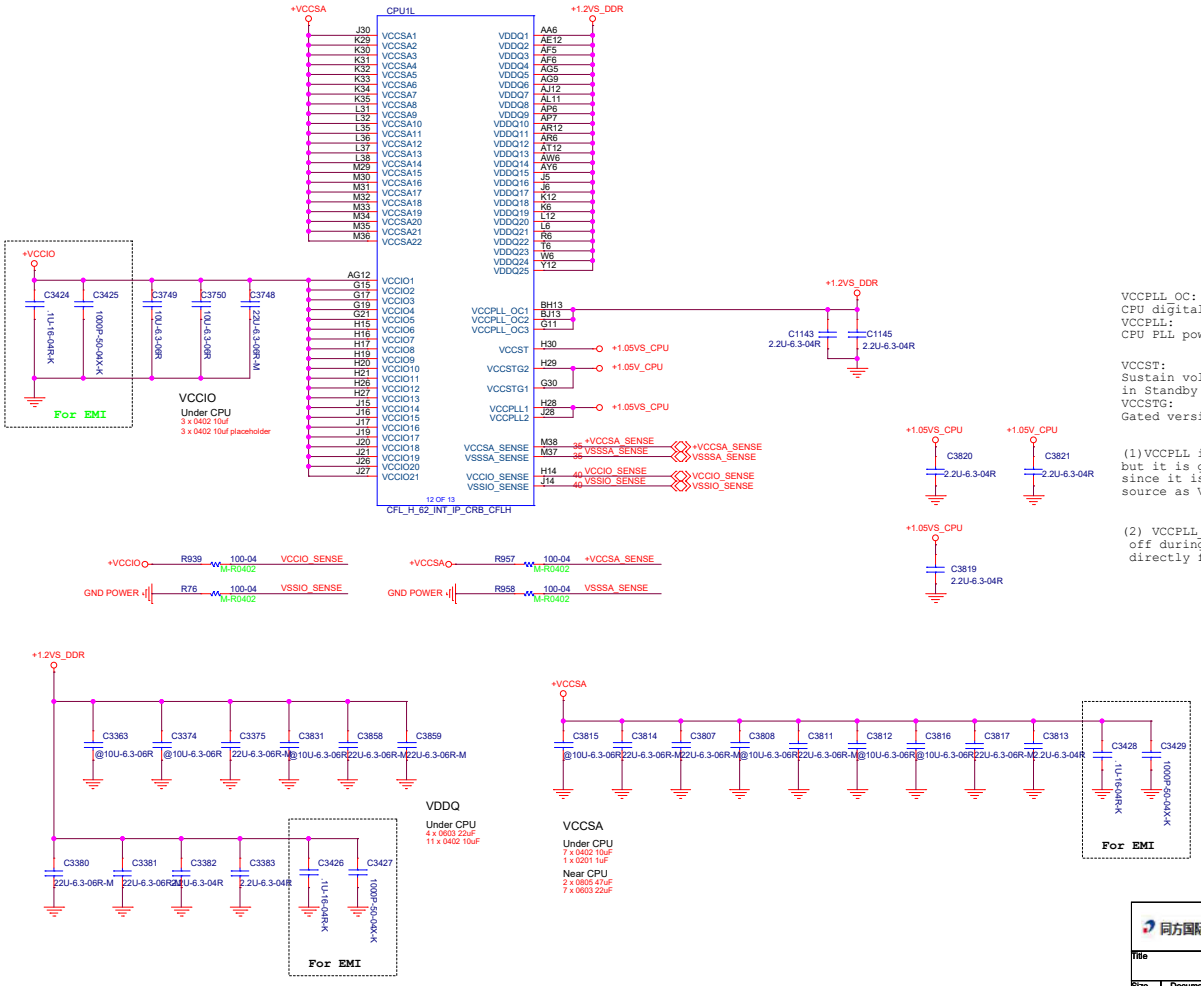

VCCPLL_OC:
CPU digital PLL power rails
VCCPLL:
CPU PLL power rails

VCCST:
Sustain voltage for processor
in Standby modes
VCCSTG:
Gated version of VCCST

(1)VCCPLL is allowed to be OFF in S3, but it is generally assumed to be ON since it is powered from the same source as VCCST.

(2) VCCPLL_OC is allowed to be turned off during S3 if it is not powered directly from VDDQ

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Title	CML-H VCCSA/VCCIO/VDDQ		
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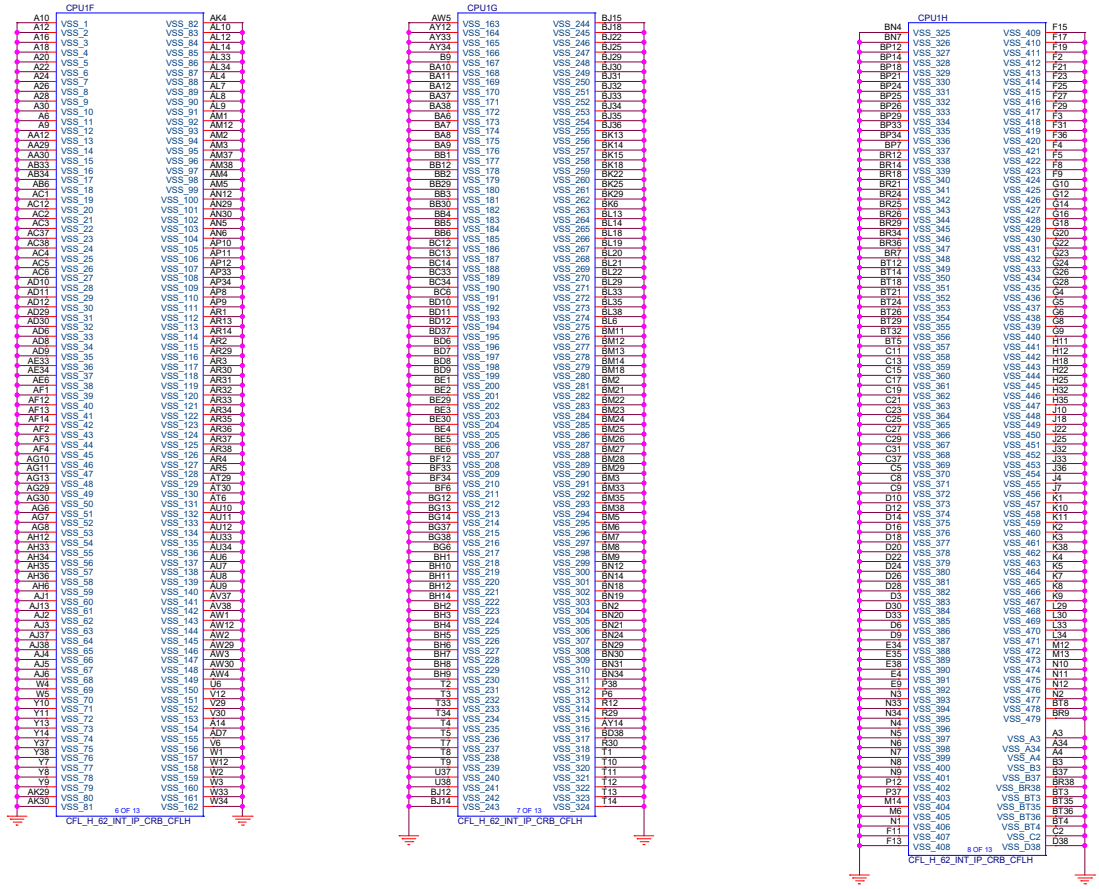

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Title: CML-H GND

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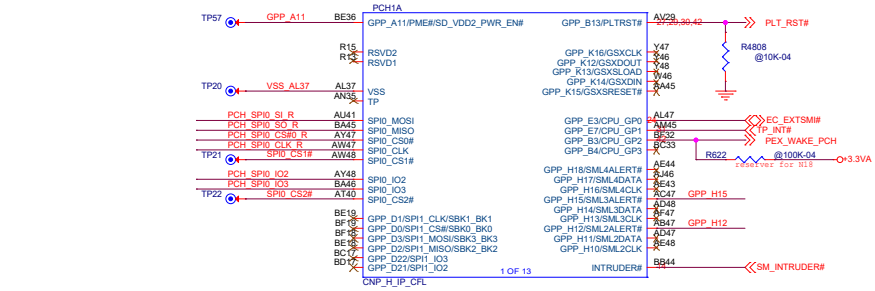
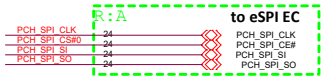
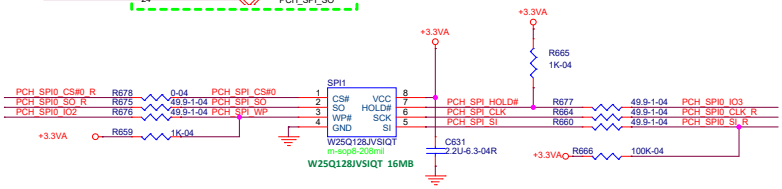


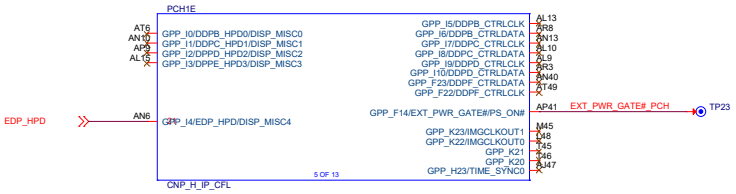
GPP_H15
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

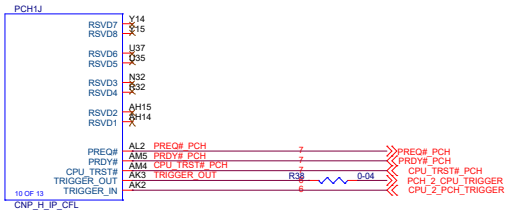
GPP_H12	eSPI Flash Sharing Mode
0	Master Attached Flash Sharing (MAFS) enabled (Default)
1	Slave Attached Flash Sharing (SAFS) enabled





SPI0_MOSI
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.





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Title	CML-H SPI/DDI CTRL/RSVD		
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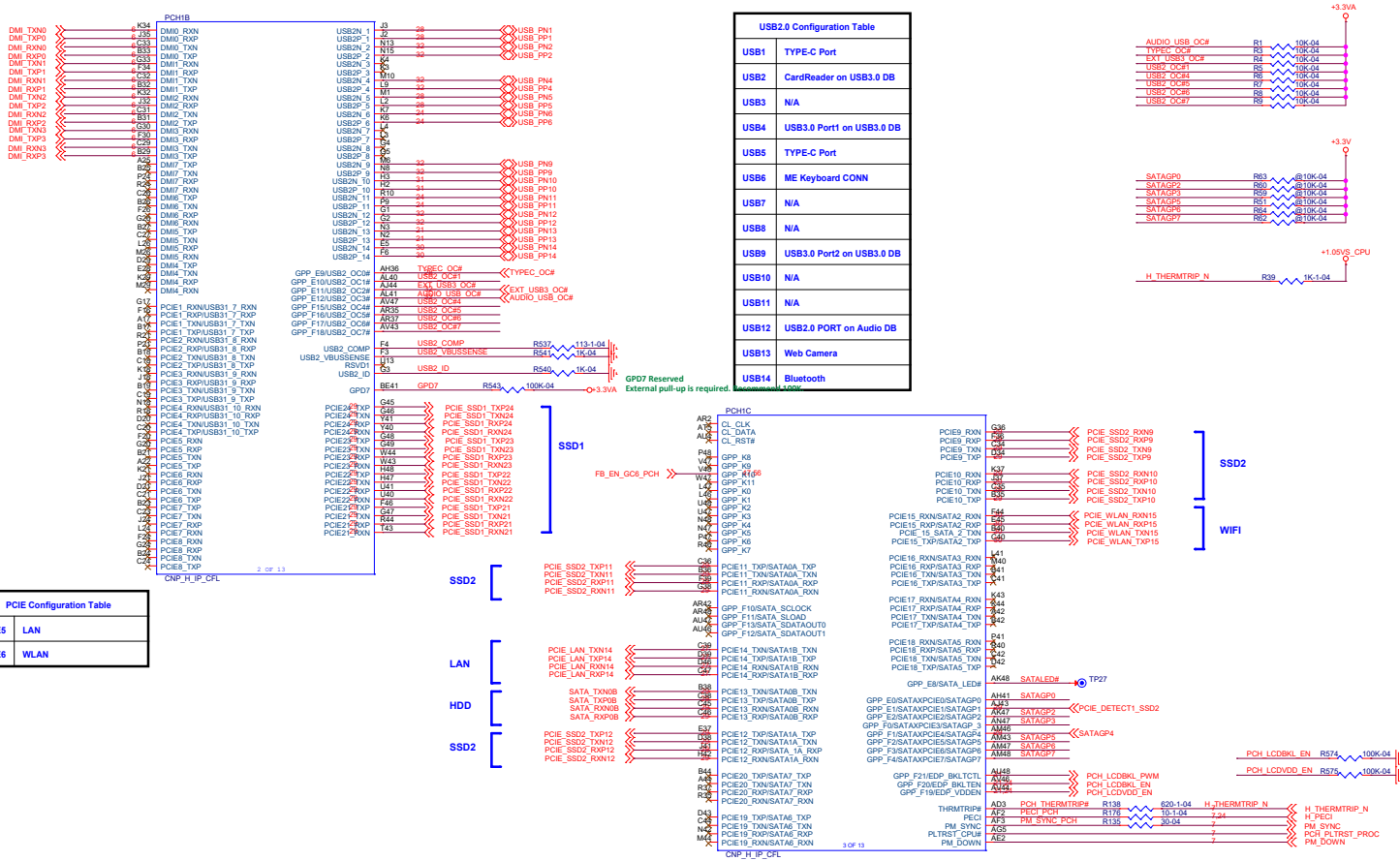

USB2.0 Configuration Table	
USB1	TYPE-C Port
USB2	CardReader on USB3.0 DB
USB3	N/A
USB4	USB3.0 Port1 on USB3.0 DB
USB5	TYPE-C Port
USB6	ME Keyboard CONN
USB7	N/A
USB8	N/A
USB9	USB3.0 Port2 on USB3.0 DB
USB10	N/A
USB11	N/A
USB12	USB2.0 PORT on Audio DB
USB13	Web Camera
USB14	Bluetooth

PCIE Configuration Table	
PCIE5	LAN
PCIE6	WLAN

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Title	CML-H DMI/PCIE/USB2/SATA		
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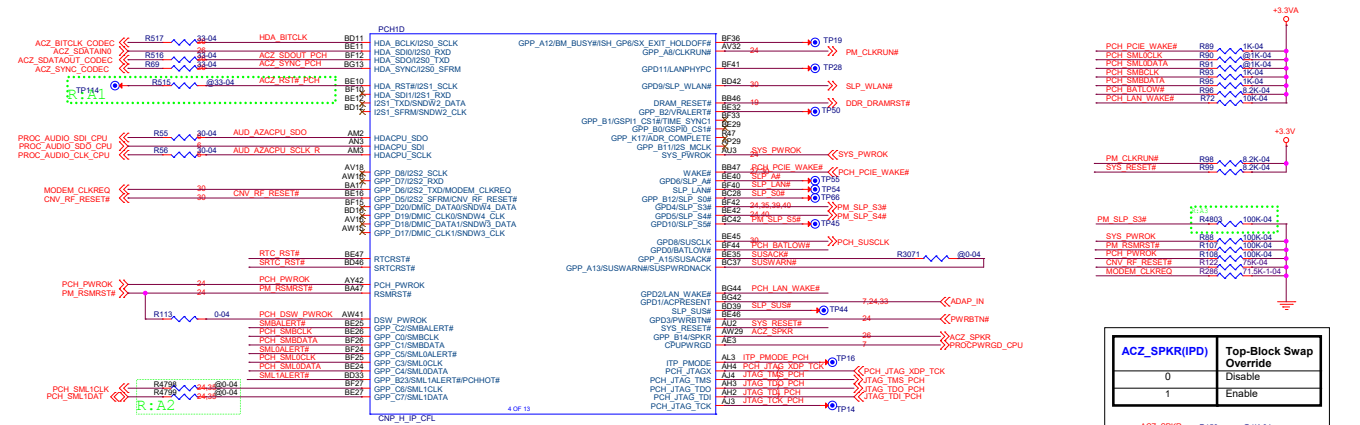

同方国际信息技术有限公司

Title	CML-H PM/HDA/SMBUS/RTC		
Size: Custom	Document Number: GK5MPFX		Rev: 1.0
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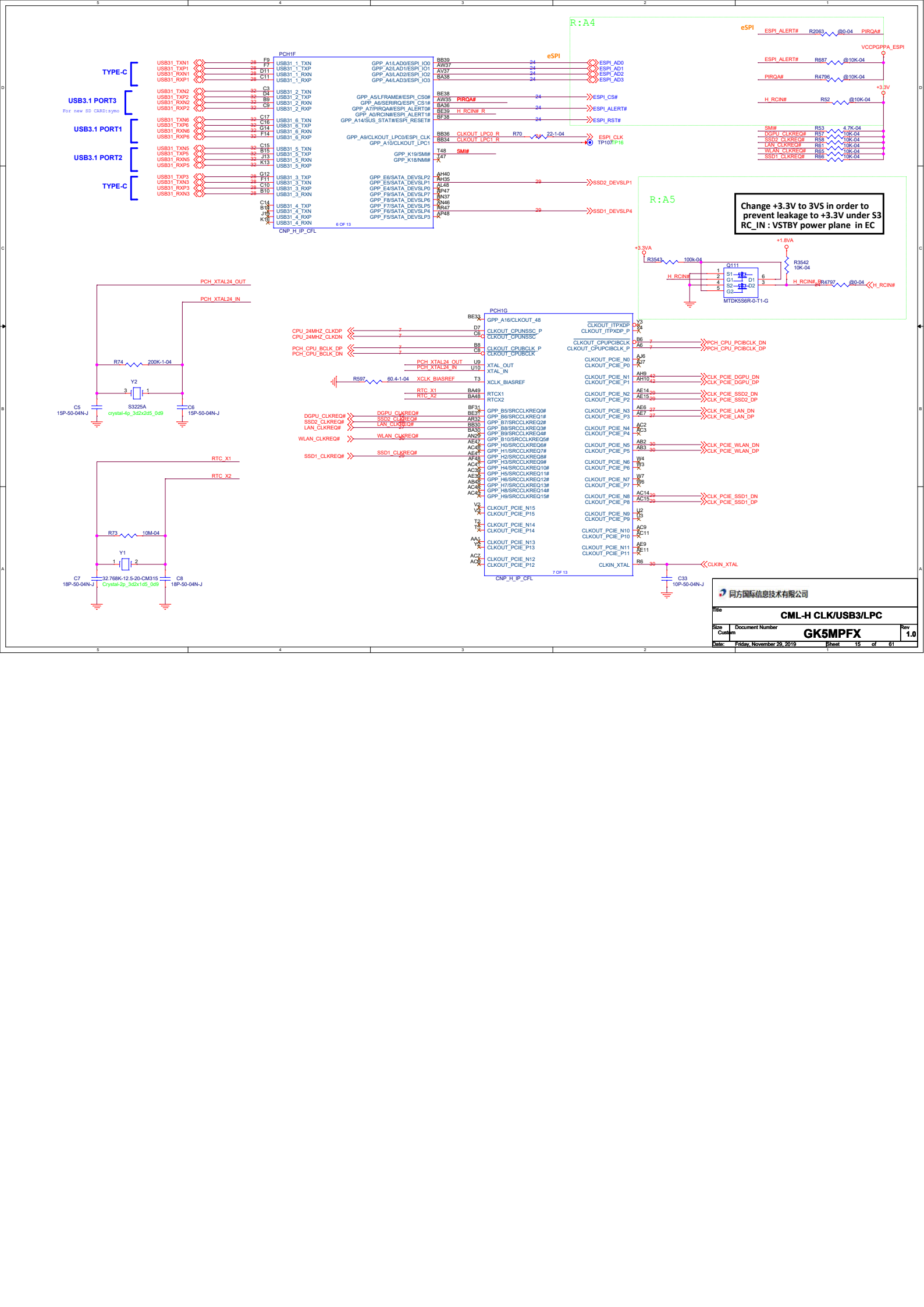
R:A4
eSPI
ESPI_ALERT#
R2063
@0-04
PIRQA#
VCCPGPPA_ESPI
ESPI_ALERT#
R687
@10K-04
PIRQA#
R4796
@10K-04
+3.3V
H_RCIN#
R52
@10K-04
SMI#
R53
4.7K-04
DGPU_CLKREQ#
R57
10K-04
SSD2_CLKREQ#
R58
10K-04
LAN_CLKREQ#
R61
10K-04
WLAN_CLKREQ#
R65
10K-04
SSD1_CLKREQ#
R66
10K-04
TYPE-C
USB3.1 PORT3
For new SD CARD:symo
USB3.1 PORT1
USB3.1 PORT2
TYPE-C
USB31_TXN1
USB31_TXP1
USB31_RXN1
USB31_RXP1
USB31_TXN2
USB31_TXP2
USB31_RXN2
USB31_RXP2
USB31_TXN6
USB31_TXP6
USB31_RXN6
USB31_RXP6
USB31_TXN5
USB31_TXP5
USB31_RXN5
USB31_RXP5
USB31_TXP3
USB31_TXN3
USB31_RXP3
USB31_RXN3
PCH1F
USB31_1_TXN
USB31_1_TXP
USB31_1_RXN
USB31_1_RXP
USB31_2_TXN
USB31_2_TXP
USB31_2_RXN
USB31_2_RXP
USB31_6_TXN
USB31_6_TXP
USB31_6_RXN
USB31_6_RXP
USB31_5_TXN
USB31_5_TXP
USB31_5_RXN
USB31_5_RXP
USB31_3_TXP
USB31_3_TXN
USB31_3_RXP
USB31_3_RXN
USB31_4_TXP
USB31_4_TXN
USB31_4_RXP
USB31_4_RXN
6 OF 13
CNP_H_IP_CFL
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A6/SERIRQ/ESPI_CS1#
GPP_A7/PIRQA#/ESPI_ALERT0#
GPP_A0/RCIN#/ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_K19/SMI#
GPP_K18/NMI#
GPP_E6/SATA_DEVSLP2
GPP_E5/SATA_DEVSLP1
GPP_E4/SATA_DEVSLP0
GPP_F9/SATA_DEVSLP7
GPP_F8/SATA_DEVSLP6
GPP_F7/SATA_DEVSLP5
GPP_F6/SATA_DEVSLP4
GPP_F5/SATA_DEVSLP3
eSPI
ESPI_AD0
ESPI_AD1
ESPI_AD2
ESPI_AD3
ESPI_CS#
ESPI_ALERT#
ESPI_RST#
PIRQA#
H_RCIN# R
CLKOUT_LPC0_R
CLKOUT_LPC1_R
R70
22-1-04
ESPI_CLK
TP107
TP16
SMI#
SSD2_DEVSLP1
SSD1_DEVSLP4
R:A5
Change +3.3V to 3VS in order to prevent leakage to +3.3V under S3
RC_IN : VSTBY power plane in EC
+3.3VA
+1.8VA
R3543
100k-04
R3542
10K-04
Q111
MTDK5S6R-0-T1-G
H_RCIN#
H_RCIN#_R
R4797
@0-04
H_RCIN#
PCH_XTAL24_OUT
PCH_XTAL24_IN
R74
200K-1-04
Y2
S3225A
crystal-4p_3d2x2d5_0d9
C5
15P-50-04N-J
C6
15P-50-04N-J
RTC_X1
RTC_X2
R73
10M-04
Y1
32.768K-12.5-20-CM315
Crystal-2p_3d2x1d5_0d9
C7
18P-50-04N-J
C8
18P-50-04N-J
PCH1G
GPP_A16/CLKOUT_48
CLKOUT_CPUNSSC_P
CLKOUT_CPUNSSC
CLKOUT_CPUBCLK_P
CLKOUT_CPUBCLK
XTAL_OUT
XTAL_IN
XCLK_BIASREF
RTCX1
RTCX2
GPP_B5/SRCCLKREQ0#
GPP_B6/SRCCLKREQ1#
GPP_B7/SRCCLKREQ2#
GPP_B8/SRCCLKREQ3#
GPP_B9/SRCCLKREQ4#
GPP_B10/SRCCLKREQ5#
GPP_H0/SRCCLKREQ6#
GPP_H1/SRCCLKREQ7#
GPP_H2/SRCCLKREQ8#
GPP_H3/SRCCLKREQ9#
GPP_H4/SRCCLKREQ10#
GPP_H5/SRCCLKREQ11#
GPP_H6/SRCCLKREQ12#
GPP_H7/SRCCLKREQ13#
GPP_H8/SRCCLKREQ14#
GPP_H9/SRCCLKREQ15#
CLKOUT_PCIE_N15
CLKOUT_PCIE_P15
CLKOUT_PCIE_N14
CLKOUT_PCIE_P14
CLKOUT_PCIE_N13
CLKOUT_PCIE_P13
CLKOUT_PCIE_N12
CLKOUT_PCIE_P12
7 OF 13
CNP_H_IP_CFL
CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
CLKOUT_CPUPCIBCLK
CLKOUT_CPUPCIBCLK_P
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
CLKOUT_PCIE_N8
CLKOUT_PCIE_P8
CLKOUT_PCIE_N9
CLKOUT_PCIE_P9
CLKOUT_PCIE_N10
CLKOUT_PCIE_P10
CLKOUT_PCIE_N11
CLKOUT_PCIE_P11
CLKIN_XTAL
CPU_24MHZ_CLKDP
CPU_24MHZ_CLKDN
PCH_CPU_BCLK_DP
PCH_CPU_BCLK_DN
R597
60.4-1-04
RTC_X1
RTC_X2
DGPU_CLKREQ#
SSD2_CLKREQ#
LAN_CLKREQ#
WLAN_CLKREQ#
SSD1_CLKREQ#
PCH_CPU_PCIBCLK_DN
PCH_CPU_PCIBCLK_DP
CLK_PCIE_DGPU_DN
CLK_PCIE_DGPU_DP
CLK_PCIE_SSD2_DN
CLK_PCIE_SSD2_DP
CLK_PCIE_LAN_DN
CLK_PCIE_LAN_DP
CLK_PCIE_WLAN_DN
CLK_PCIE_WLAN_DP
CLK_PCIE_SSD1_DN
CLK_PCIE_SSD1_DP
CLKIN_XTAL
C33
10P-50-04N-J
同方国际信息技术有限公司
Title
CML-H CLK/USB3/LPC
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61

GPP_B22/GSPI1_MOSI(IPD)	Boot BIOS Destination
0	SPI (Default)
1	LPC

+3.3V R545 @150K-04 PCH_GSPI1_SI_R

GPP_B18/GSPI0_MOSI(IPD)	No Reboot Mode with TCO Disabled
0	Disabled (Default)
1	Enable

+3.3V R546 @4.7K-04 GPP_B18

CNV_BRI_DT (IPD)	XTAL Frequency Select
0	38.4MHz XTAL frequency
1	24MHz XTAL frequency (Default)

+VCCPRIM_1P8 R610 10K-04 CNV_BRI_DT_PCH

CNV_RGI_DT	M.2 CNV Mode Select
0	Integrated CNVi enable
1	Integrated CNVi disable

CNV_RGI_DT_PCH
R617 @100K-04

+VCCPRIM_1P8 R615 20K-04 CNV_BRI_RSP
R656 20K-04 CNV_RGI_RSP

MEM_OVERCLK_EN R572 0-04 PCH_GSPI1_SI_R
OVRM_TGP_SEL R573 @0-04 GPP_B18
SMC_WAKE_SCI# 24
FBVDDQ_PG_TVBAon_GC6 55,56
Dgpu_PWR_ON 24,55
UART2_DEBUG_TXD 30
UART2_DEBUG_RXD 30
GPU_EVENT#_GC6 47
DGPU_RST# 42
TP_I2C0_SCL 31
TP_I2C0_SDA 31

PCH1K
BA26 GPP_B22/GSPI1_MOSI
BD30 GPP_B21/GSPI1_MISO
AU26 GPP_B20/GSPI1_CLK
AW26 GPP_B19/GSPI1_CS0#
BE30 GPP_B18/GSPI0_MOSI
BD29 GPP_B17/GSPI0_MISO
BF29 GPP_B16/GSPI0_CLK
BB29 GPP_B15/GSPI0_CS0#
BB24 GPP_C9/UART0_TXD
BE23 GPP_C8/UART0_RXD
AP24 GPP_C11/UART0_CTS#
BA23 GPP_C10/UART0_RTS#
BD21 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
AW24 GPP_C14/UART1_RTS#/ISH_UART1_RTS#
AP21 GPP_C13/UART1_TXD/ISH_UART1_TXD
AU23 GPP_C12/UART1_RXD/ISH_UART1_RXD
AV21 GPP_C23/UART2_CTS#
AW22 GPP_C22/UART2_RTS#
BE20 GPP_C21/UART2_TXD
BD20 GPP_C20/UART2_RXD
BE21 GPP_C19/I2C1_SCL
BF21 GPP_C18/I2C1_SDA
BC22 GPP_C17/I2C0_SCL
BF23 GPP_C16/I2C0_SDA
BE19 GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4_BK4
BE18 GPP_D23/ISH_I2C2_SCL/I2C3_SCL
GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/GSPI2_CLK
GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI
GPP_D16/ISH_UART0_CTS#/CNV_WCEN
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN
GPP_D14/ISH_UART0_TXD/I2C2_SCL
GPP_D13/ISH_UART0_RXD/I2C2_SDA
GPP_H20/ISH_I2C0_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA
GPP_A23/ISH_GP5
GPP_A22/ISH_GP4
GPP_A21/ISH_GP3
GPP_A20/ISH_GP2
GPP_A19/ISH_GP1
GPP_A18/ISH_GP0
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
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CNP_H_IP_CFL

PCH1M
AW13 GPP_G0/SD_CMD
BE5 GPP_G1/SD_D0
BF5 GPP_G2/SD_D1
BC5 GPP_G3/SD_D2
BE4 GPP_G4/SD_D3
BD5 GPP_G5/SD_CD#
AV13 GPP_G6/SD_CLK
GPP_G7/SD_WP
AP2 GPP_I11/M2_SKT2_CFG0
AF2 GPP_I12/M2_SKT2_CFG1
AN2 GPP_I13/M2_SKT2_CFG2
AM2 GPP_I14/M2_SKT2_CFG3
AV6 GPP_J0/CNV_PA_BLANKING
AY3 GPP_J1/CPU_VCCIO_PWR_GATE#
AR13 GPP_J11/A4WP_PRESENT
AV7 GPP_J10
AW3 GPP_J_2
AT10 GPP_J_3
AV4 GPP_J_4_CNV_BRI_DT_UART0_RTSB
AY2 GPP_J5/CNV_BRI_RSP/UART0_RXD
BA4 GPP_J6/CNV_RGI_DT/UART0_TXD
AV3 GPP_J7/CNV_RGI_RSP/UART0_CTS#
AW2 GPP_J8/CNV_MFUART2_RXD
AU9 GPP_J9/CNV_MFUART2_TXD
BD4 CNV_WR_CLKN
BE3 CNV_WR_CLKP
BB3 CNV_WR_D0N
BB4 CNV_WR_D0P
BA3 CNV_WR_D1N
BA2 CNV_WR_D1P
BC5 CNV_WT_CLKN
BB6 CNV_WT_CLKP
BE6 CNV_WT_D0N
BD7 CNV_WT_D0P
BC6 CNV_WT_D1N
BF6 CNV_WT_D1P
BA1 CNV_WT_RCOMP R598 150-1-04
B12 PCIE_RCOMPN
A13 PCIE_RCOMPP R596 100-1-04
BE5 SD_RCOMP_1P8 R599 200-1-04
BE4 SD_RCOMP_3P3 R600 200-1-04
BD1 GPPJ_RCOMP_1P81
BE1 GPPJ_RCOMP_1P82
BE2 GPPJ_RCOMP_1P83 GPPJ_RCOMP_1P8 R606 200-1-04
RSVD2 X35
RSVD3 X36
TP58
RSVD1 BC1
TP AL35
13 OF 13
CNP_H_IP_CFL

TP11 VCCIO_PWR_GATE#
R4875 75K-04
CNV_BRI_DT R612 33-04 CNV_BRI_DT_PCH
CNV_BRI_RSP
CNV_RGI_DT R614 33-04 CNV_RGI_DT_PCH
CNV_RGI_RSP
GPP_J9

GPP_J9	VCCPSPI Rail select
0	VCCSPI is connected to 3.3V
1	VCCSPI is connected to 1.8V

+VCCPRIM_1P8 R611 @4.7K-04 GPP_J9

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Title: CML-H CNV/UART/I2C

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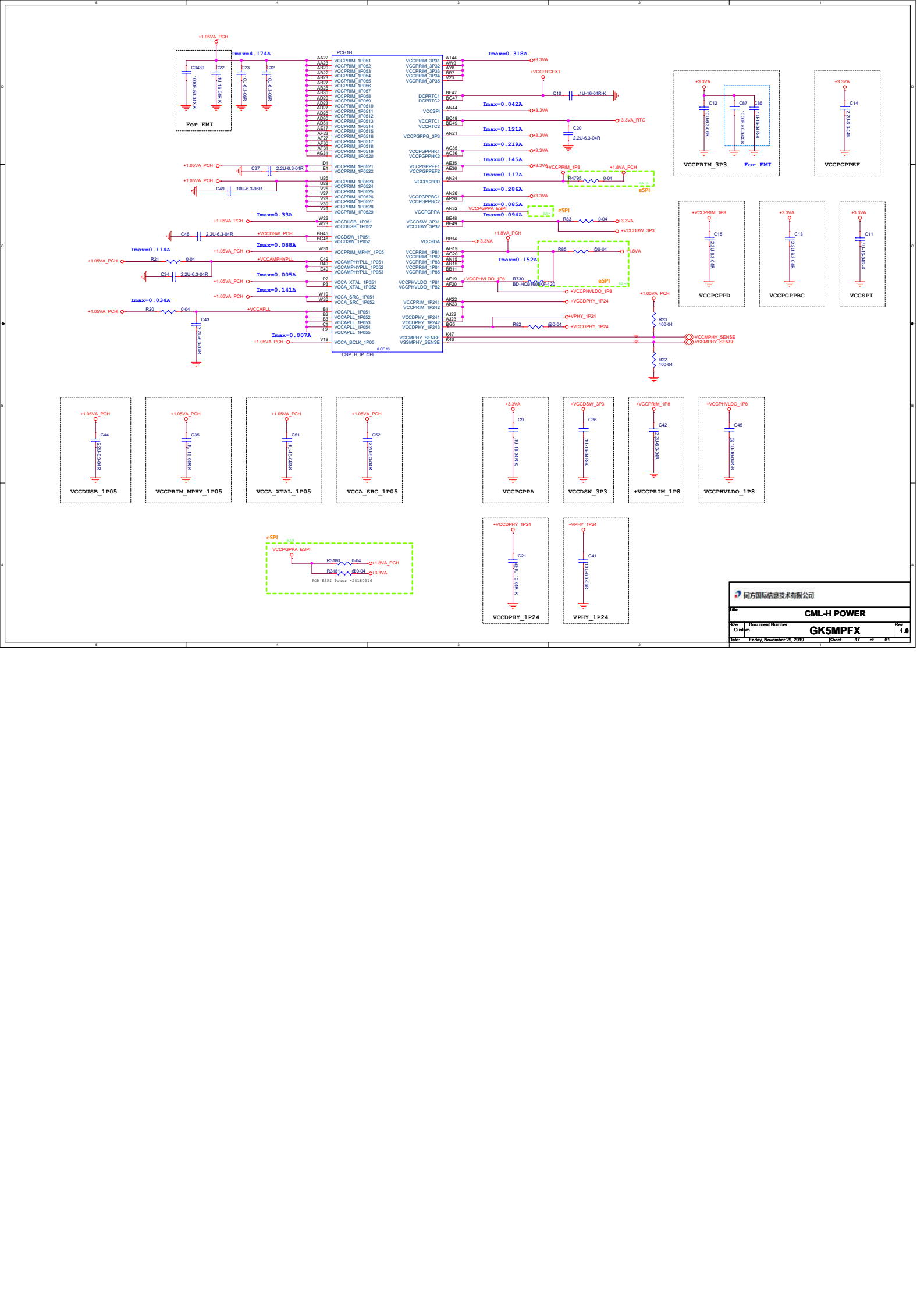
PCH1H
CNP_H_IP_CFL
8 OF 13
Imax=4.174A
Imax=0.318A
Imax=0.042A
Imax=0.121A
Imax=0.219A
Imax=0.145A
Imax=0.117A
Imax=0.286A
Imax=0.085A
Imax=0.094A
Imax=0.152A
Imax=0.33A
Imax=0.088A
Imax=0.114A
Imax=0.005A
Imax=0.141A
Imax=0.034A
Imax=0.007A
For EMI
eSPI
VCCPRIM_3P3
VCCPGPPEF
VCCPGPPD
VCCPGPPBC
VCCSPI
VCCDUSB_1P05
VCCPRIM_MPHY_1P05
VCCA_XTAL_1P05
VCCA_SRC_1P05
VCCPGPPA
VCCDSW_3P3
+VCCPRIM_1P8
VCCPHVLDO_1P8
VCCDPHY_1P24
VPHY_1P24
FOR ESPI Power -20180516
同方国际信息技术有限公司
CML-H POWER
GK5MPFX
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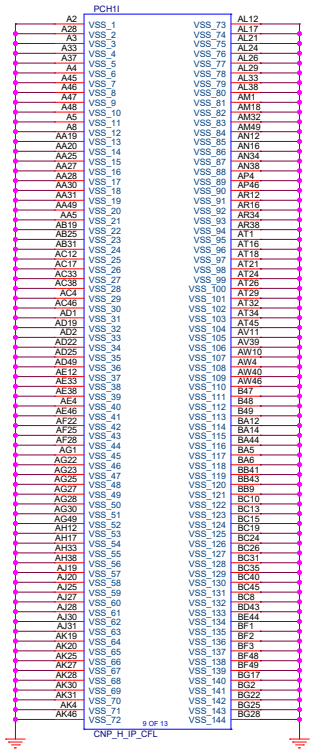

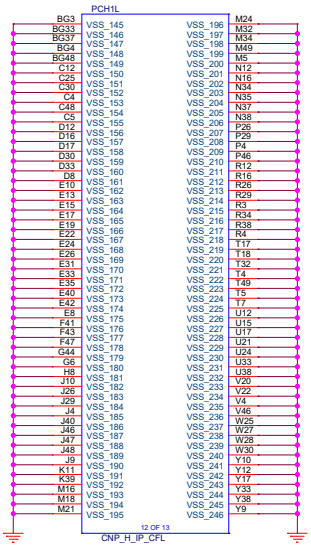

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Title	CML-H GND		
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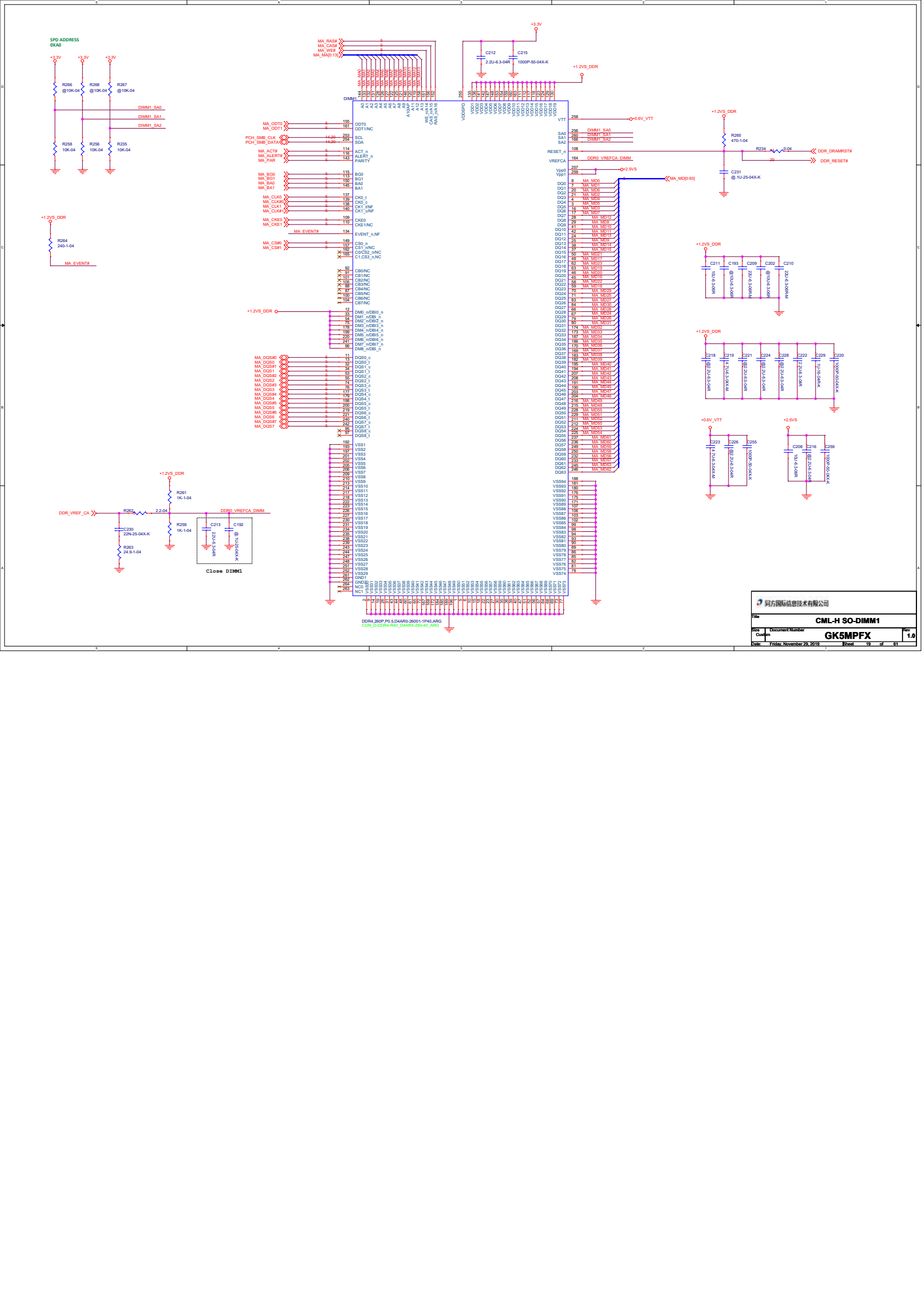
SPD ADDRESS
0XA0
DIMM1
DDR4_260P.P0.5.D4ARD-26001-1P40.ARG
CON_D-DDR4-R40_D4ARX-260-40_ARG
Close DIMM1
CML-H SO-DIMM1
GK5MPFX
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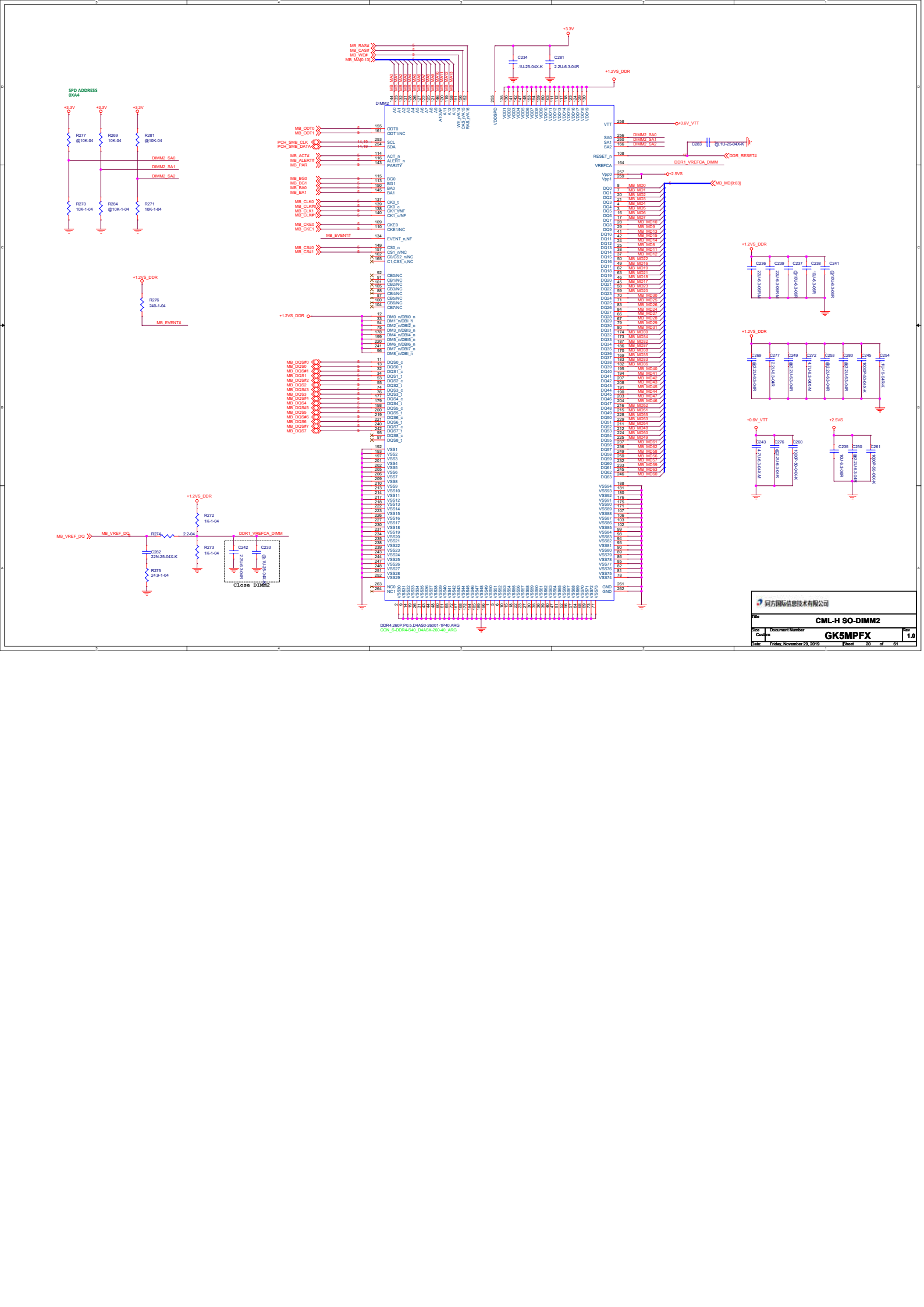
SPD ADDRESS
0XA4
DIMM2
DDR4.260P.P0.5.D4AS0-26001-1P40.ARG
CON_S-DDR4-S40_D4ASX-260-40_ARG
Close DIMM2
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CML-H SO-DIMM2
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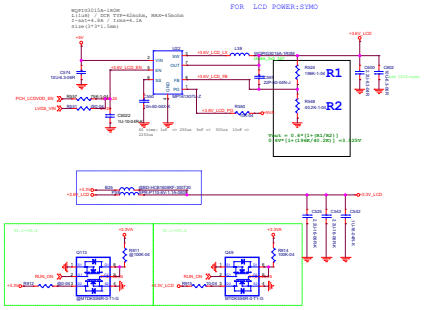
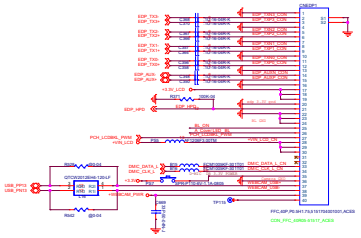
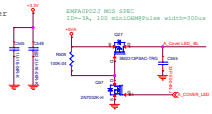
+3.6V_LCD



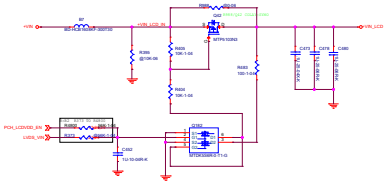


Camera power

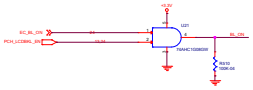
A Cover power



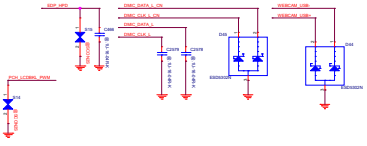
LCD BL VIN



BL_EN



ESD Discharge



	eDP Panel/CAMERA		
Size: D	Document Number: GK5MPFX		Rev: 1.0
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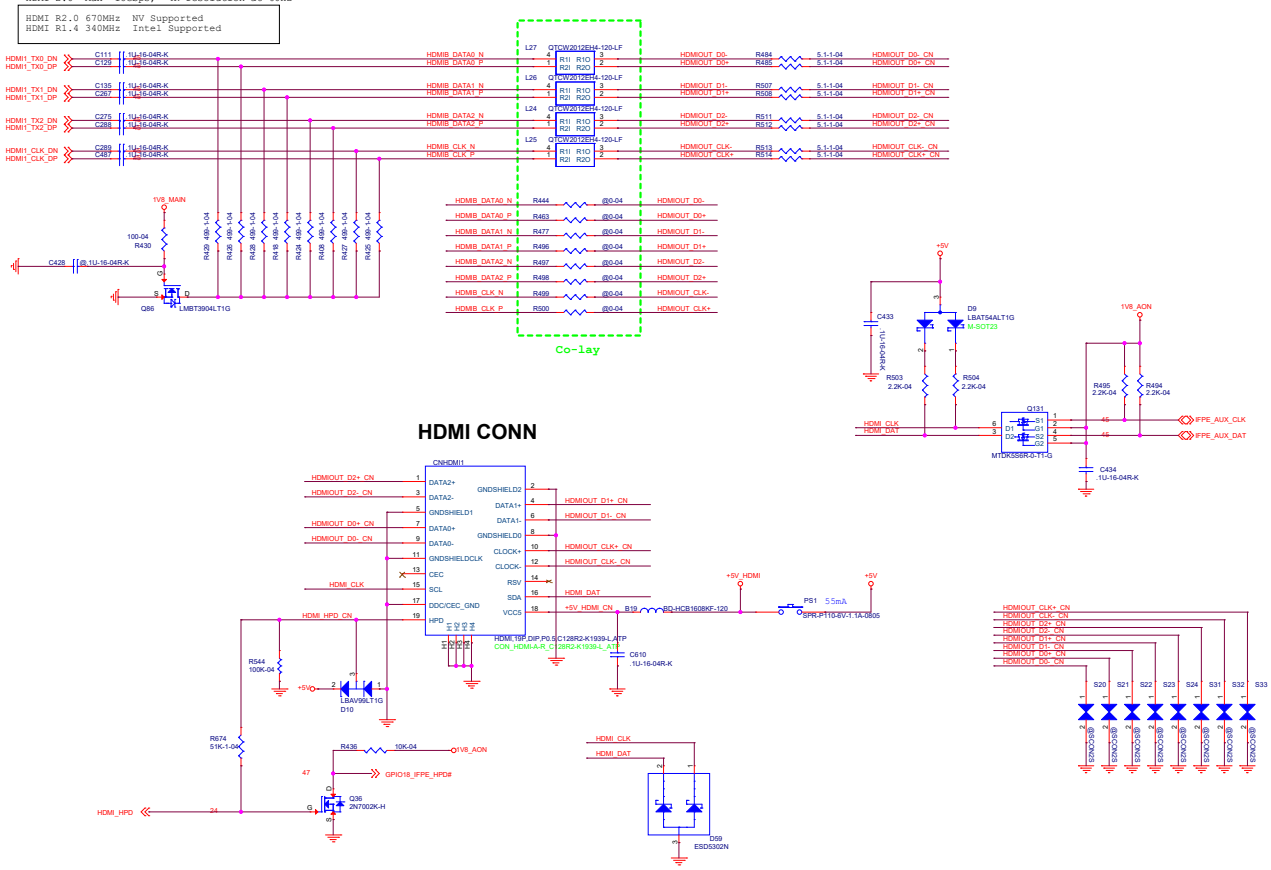
HDMI 2.0 Max =18Gbps, 4K resolution at 60HZ

HDMI R2.0 670MHz NV Supported
HDMI R1.4 340MHz Intel Supported



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Title	HDMI		
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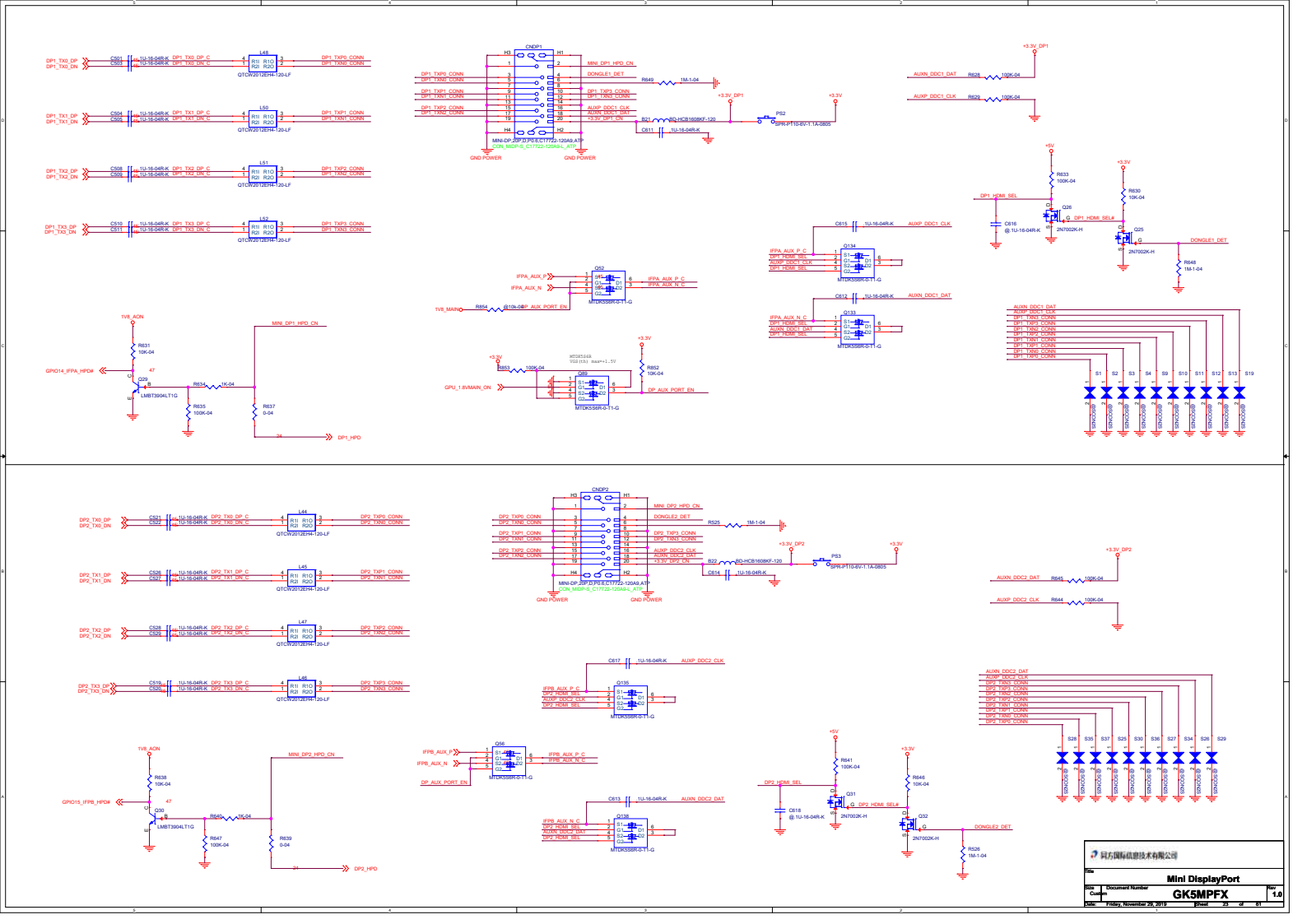
DP1_TX0_DP
DP1_TX0_DN
C521
C522
1U-16-04R-K
DP1_TX0_DP_C
DP1_TX0_DN_C
L48
QTCW2012EH4-120-LF
DP1_TXP0_CONN
DP1_TXN0_CONN
DP1_TX1_DP
DP1_TX1_DN
C504
C505
DP1_TX1_DP_C
DP1_TX1_DN_C
L50
DP1_TXP1_CONN
DP1_TXN1_CONN
DP1_TX2_DP
DP1_TX2_DN
C508
C509
DP1_TX2_DP_C
DP1_TX2_DN_C
L51
DP1_TXP2_CONN
DP1_TXN2_CONN
DP1_TX3_DP
DP1_TX3_DN
C510
C511
DP1_TX3_DP_C
DP1_TX3_DN_C
L52
DP1_TXP3_CONN
DP1_TXN3_CONN
CNDP1
H3
H1
H4
H2
MINI_DP1_HPD_CN
DONGLE1_DET
AUXP_DDC1_CLK
AUXN_DDC1_DAT
+3.3V_DP1_ON
MINI-DP-20P-D.P0.E.C17722-120A9.ATP
CON_MIDP-S_C17722-120A9-L_ATP
GND POWER
R649
1M-1-04
+3.3V_DP1
+3.3V
PS2
SPR-PT10-6V-1.1A-0805
R21
BD-HCB1608KF-120
C611
1U-16-04R-K
AUXN_DDC1_DAT
R628
100K-04
AUXP_DDC1_CLK
R629
100K-04
+3.3V_DP1
+5V
R633
100K-04
DP1_HDMI_SEL
C616
@1U-16-04R-K
Q26
2N7002K-H
DP1_HDMI_SEL#
+3.3V
R630
10K-04
Q25
2N7002K-H
DONGLE1_DET
R648
1M-1-04
C615
1U-16-04R-K
AUXP_DDC1_CLK
IFPA_AUX_P_C
DP1_HDMI_SEL
AUXP_DDC1_CLK
DP1_HDMI_SEL
Q134
MTDK3S6R-0-T1-G
C612
1U-16-04R-K
AUXN_DDC1_DAT
IFPA_AUX_N_C
DP1_HDMI_SEL
AUXN_DDC1_DAT
DP1_HDMI_SEL
Q133
MTDK3S6R-0-T1-G
AUXN_DDC1_DAT
AUXP_DDC1_CLK
DP1_TXP3_CONN
DP1_TXN3_CONN
DP1_TXP2_CONN
DP1_TXN2_CONN
DP1_TXP1_CONN
DP1_TXN1_CONN
DP1_TXP0_CONN
DP1_TXN0_CONN
S1
S2
S3
S4
S9
S10
S11
S12
S13
S19
SSN2X28
IFPA_AUX_P
IFPA_AUX_N
Q52
IFPA_AUX_P_C
IFPA_AUX_N_C
MTDK3S6R-0-T1-G
1V8_MAIN
R854
@10-0-04
DP_AUX_PORT_EN
MTDK3S6R
VGS(th) max=+1.5V
+3.3V
R853
100K-04
GPU_1.8VMAIN_ON
Q82
MTDK3S6R-0-T1-G
+3.3V
R852
10K-04
DP_AUX_PORT_EN
1V8_AON
R831
10K-04
GPIO14_IFPA_HPD#
Q29
LMBT3904LT1G
R834
1K-04
R835
100K-04
R837
0-04
MINI_DP1_HPD_CN
DP1_HPD

DP2_TX0_DP
DP2_TX0_DN
C521
C522
1U-16-04R-K
DP2_TX0_DP_C
DP2_TX0_DN_C
L44
QTCW2012EH4-120-LF
DP2_TXP0_CONN
DP2_TXN0_CONN
DP2_TX1_DP
DP2_TX1_DN
C526
C527
DP2_TX1_DP_C
DP2_TX1_DN_C
L45
DP2_TXP1_CONN
DP2_TXN1_CONN
DP2_TX2_DP
DP2_TX2_DN
C528
C529
DP2_TX2_DP_C
DP2_TX2_DN_C
L47
DP2_TXP2_CONN
DP2_TXN2_CONN
DP2_TX3_DP
DP2_TX3_DN
C519
C520
DP2_TX3_DP_C
DP2_TX3_DN_C
L46
DP2_TXP3_CONN
DP2_TXN3_CONN
CNDP2
H3
H1
H4
H2
MINI_DP2_HPD_CN
DONGLE2_DET
AUXP_DDC2_CLK
AUXN_DDC2_DAT
+3.3V_DP2_ON
MINI-DP-20P-D.P0.E.C17722-120A9.ATP
CON_MIDP-S_C17722-120A9-L_ATP
GND POWER
R525
1M-1-04
+3.3V_DP2
+3.3V
PS3
SPR-PT10-6V-1.1A-0805
R22
BD-HCB1608KF-120
C614
1U-16-04R-K
AUXN_DDC2_DAT
R645
100K-04
AUXP_DDC2_CLK
R644
100K-04
+3.3V_DP2
C617
1U-16-04R-K
AUXP_DDC2_CLK
IFPB_AUX_P_C
DP2_HDMI_SEL
AUXP_DDC2_CLK
DP2_HDMI_SEL
Q135
MTDK3S6R-0-T1-G
C613
1U-16-04R-K
AUXN_DDC2_DAT
IFPB_AUX_N_C
AUXN_DDC2_DAT
DP2_HDMI_SEL
Q138
MTDK3S6R-0-T1-G
AUXN_DDC2_DAT
AUXP_DDC2_CLK
DP2_TXP3_CONN
DP2_TXN3_CONN
DP2_TXP2_CONN
DP2_TXN2_CONN
DP2_TXP1_CONN
DP2_TXN1_CONN
DP2_TXP0_CONN
DP2_TXN0_CONN
S28
S35
S37
S25
S30
S36
S27
S34
S26
S29
SSN2X28
IFPB_AUX_P
IFPB_AUX_N
Q56
IFPB_AUX_P_C
IFPB_AUX_N_C
MTDK3S6R-0-T1-G
DP_AUX_PORT_EN
+5V
R641
100K-04
DP2_HDMI_SEL
C618
@1U-16-04R-K
Q31
2N7002K-H
DP2_HDMI_SEL#
+3.3V
R646
10K-04
Q32
2N7002K-H
DONGLE2_DET
R526
1M-1-04
1V8_AON
R838
10K-04
GPIO15_IFPB_HPD#
Q30
LMBT3904LT1G
R648
1K-04
R647
100K-04
R839
0-04
MINI_DP2_HPD_CN
DP2_HPD

昇方国际信息技术有限公司
Title
Mini DisplayPort
Size
Custom
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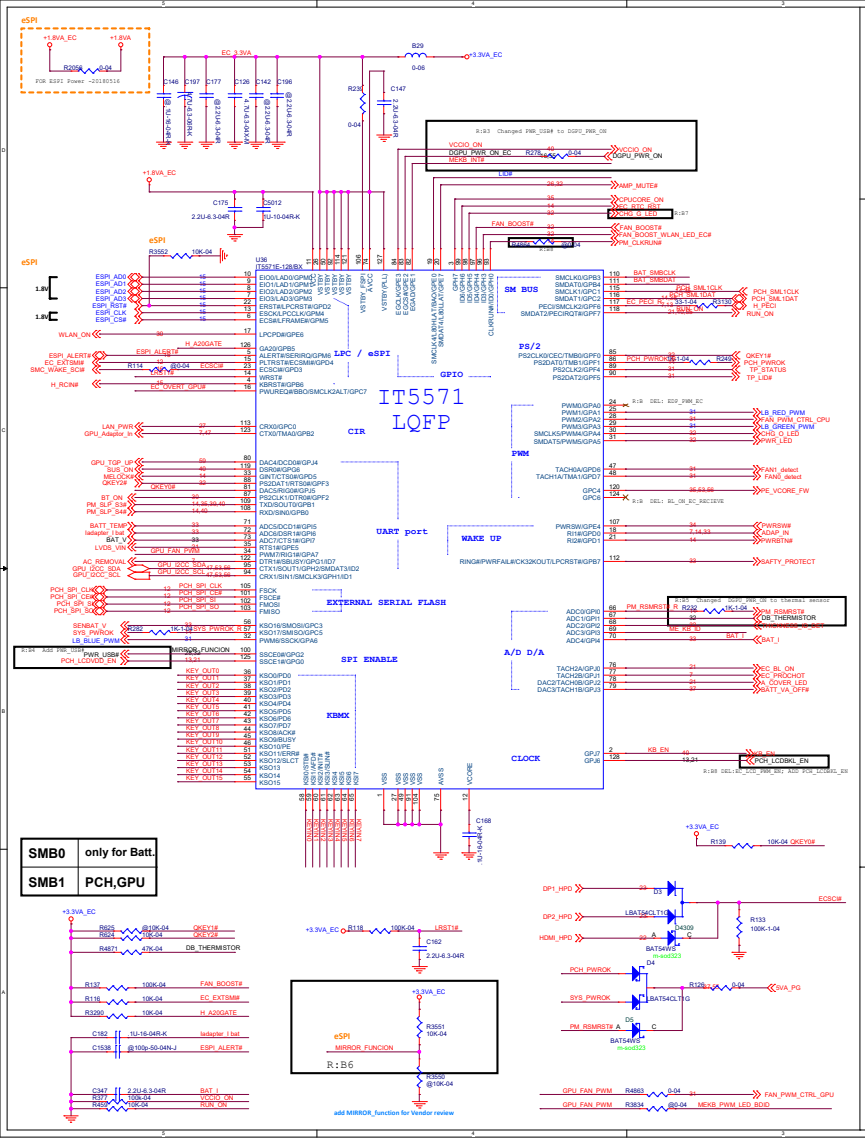

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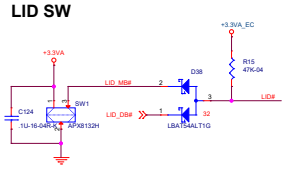
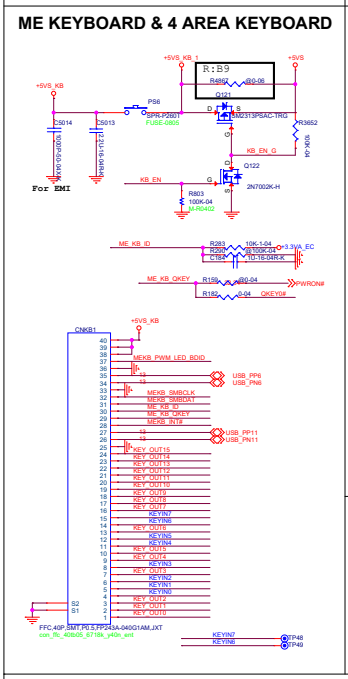
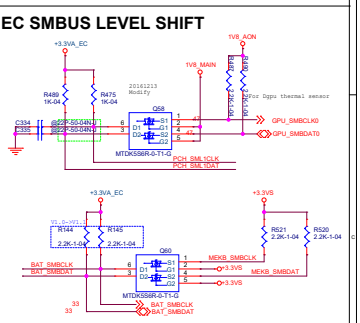


EC FLASH ROM(SPI)

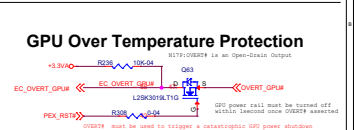
ME KEYBOARD & 4 AREA KEYBOARD



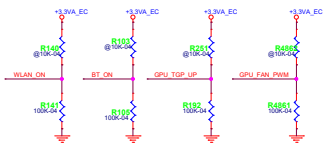
EC SMBUS LEVEL SHIFT



GPU Over Temperature Protection



Platform ID



NET / Level	WLAN_ON	BT_ON	GPU_TGP_UP	Board ID
HIGH			N18P-62	
LOW	15"	CFL-H	N18P-61	

Title	EC(IT8528E)/BIOS/KB CONN
Size / Custom	Document Number: GK5MPFX
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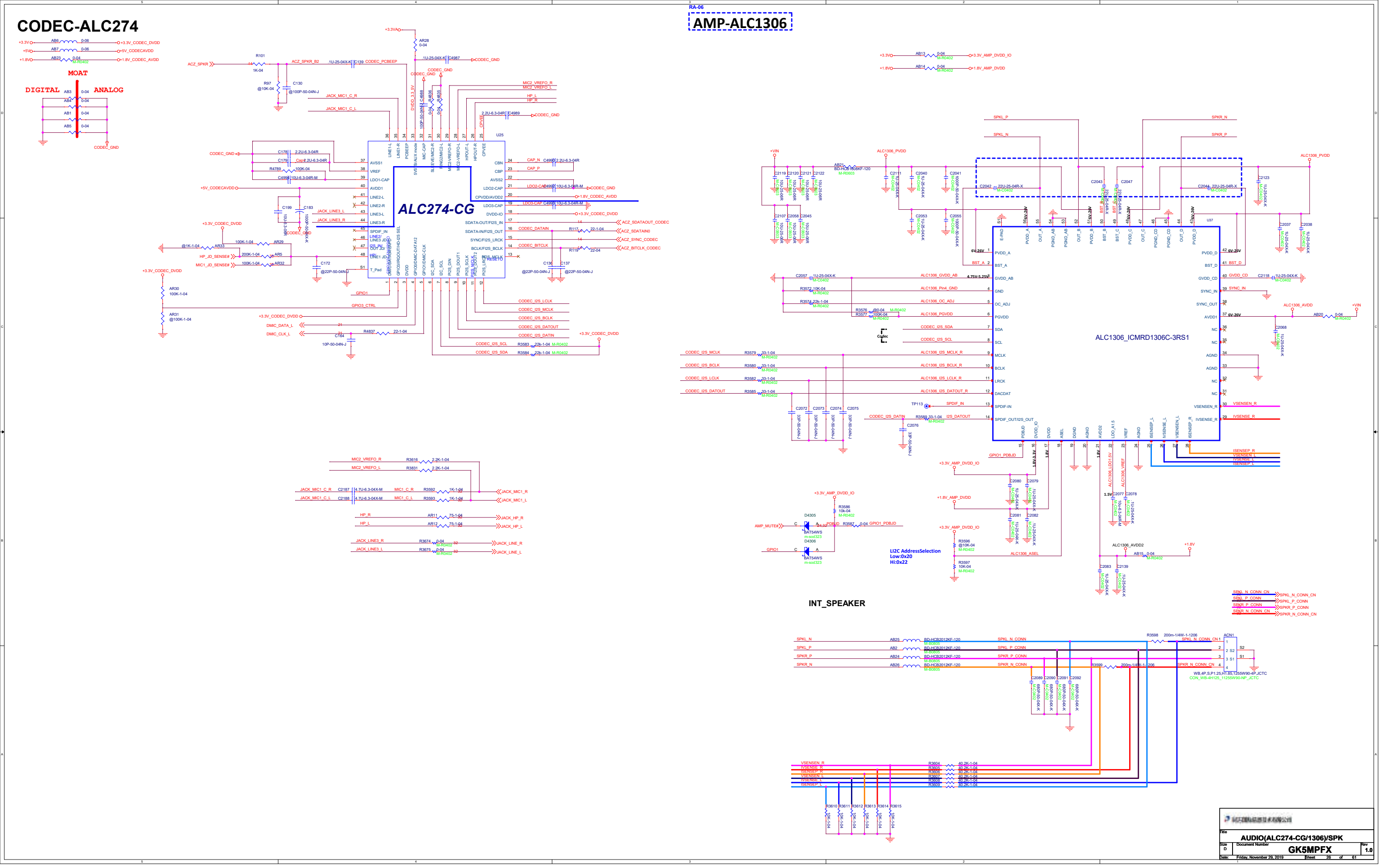
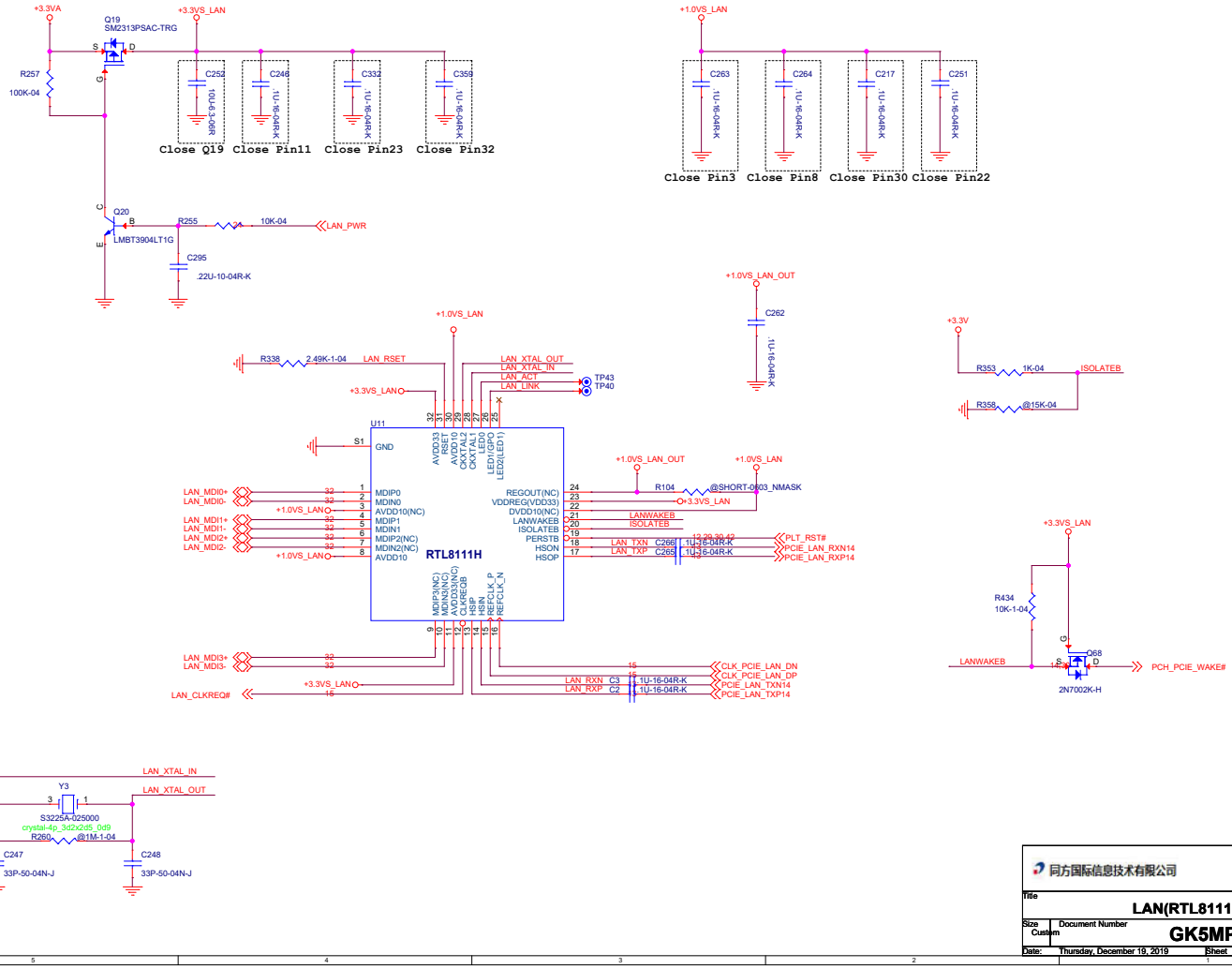
Title:	GM38PF3-10L
Size: D	Document Number: GM38PF3
Rev: 1.0	
Date: Friday, November 29, 2019	Sheet 39 of 41



CODEC-ALC274
MOAT
DIGITAL
ANALOG
ALC274-CG
RA-06
AMP-ALC1306
ALC1306_ICMRD1306C-3RS1
I2C AddressSelection
Low:0x20
Hi:0x22
INT_SPEAKER
AUDIO(ALC274-CG/1306)/SPK
GK5MPFX
1.0



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Title	LAN(RTL8111G-CG)		
Size: Custom	Document Number: GK5MPFX		Rev: 1.0
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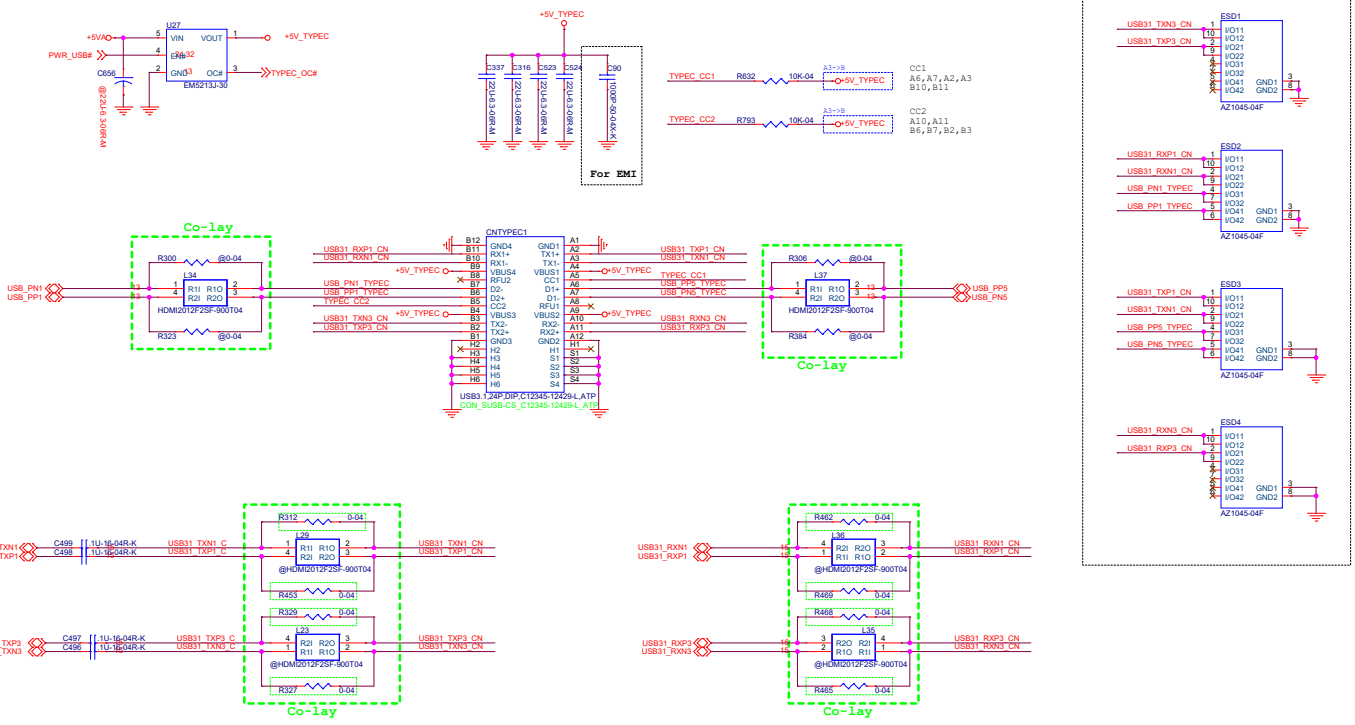
USB3.0 TYPE-C



ESD

同方国际信息技术有限公司

Title	USB3.1 TYPE-C	
Size: Custom	Document Number: GK5MPFX	Rev: 1.0
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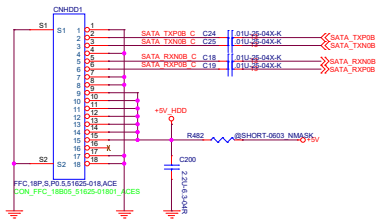
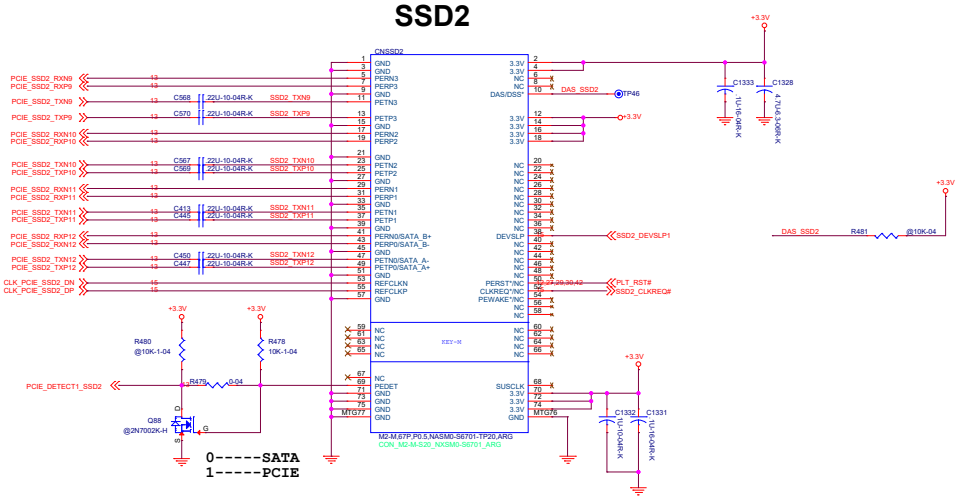
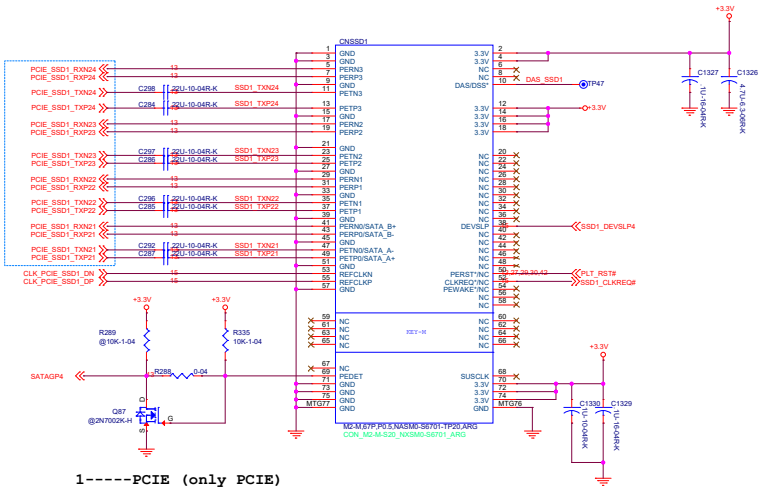
SATA-HDD



SSD2



SSD1



1-----PCIE (only PCIE)

同方国际信息技术有限公司

Title	HDD/SSD	
Size: Custom	Document Number: GK5MPFX	Rev: 1.0
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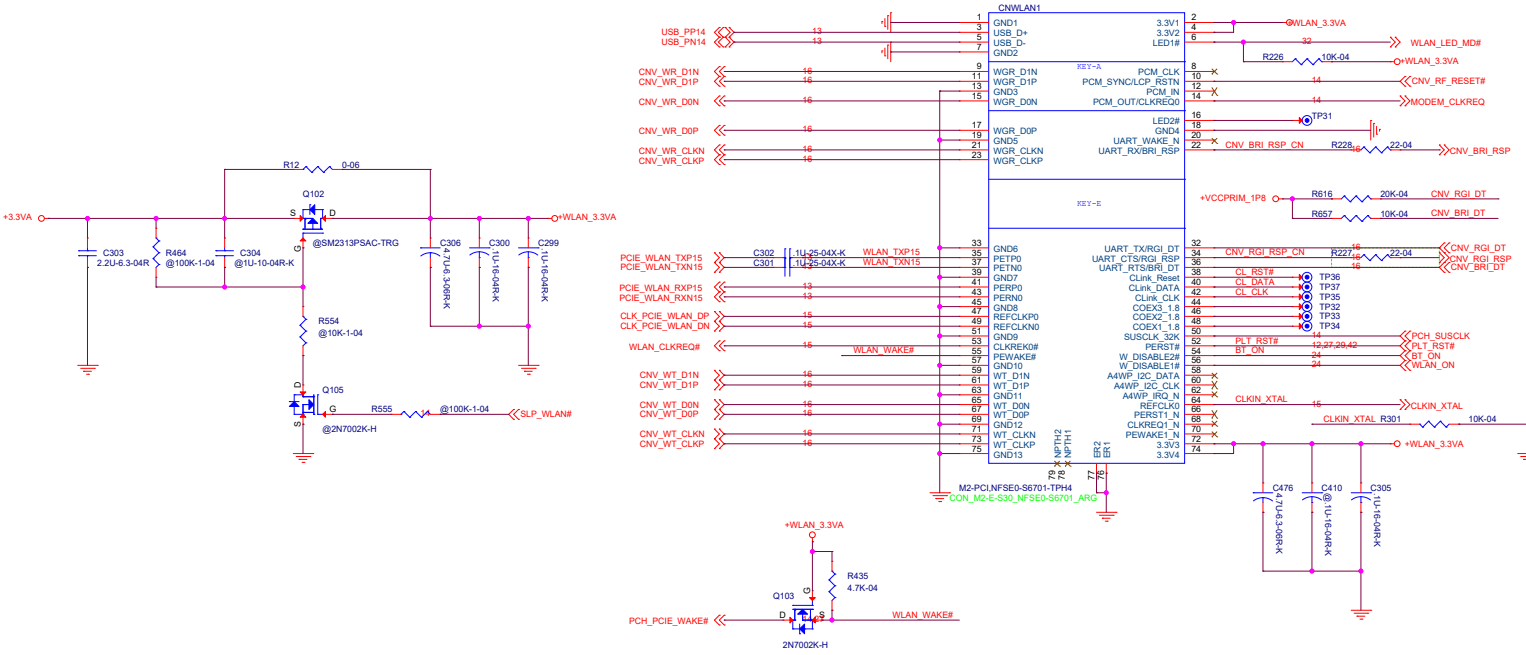
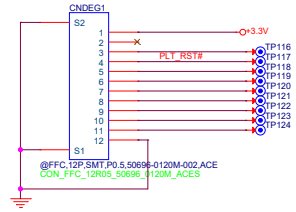
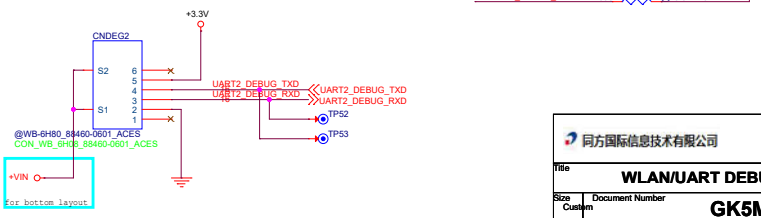
WLAN CONN



LPC debug port



UART debug port



同方国际信息技术有限公司

Title	WLAN/UART DEBUG/LPC DEBUG		
Size: Custom	Document Number: GK5MPFX		Rev: 1.0
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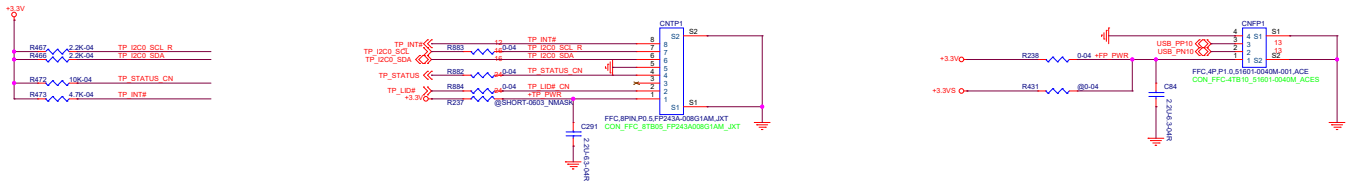
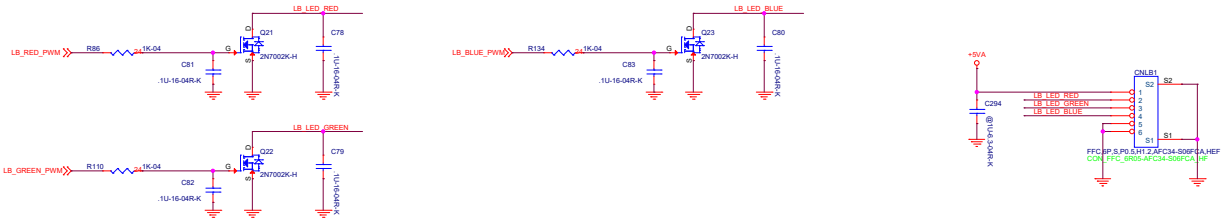
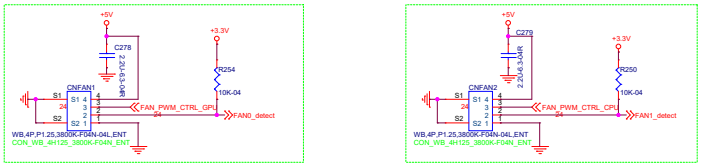
Touch Pad&Finger Print



Light bar Control



FAN CONTROLLER



同方国际信息技术有限公司

Title	TP/CP/FAN/LB		
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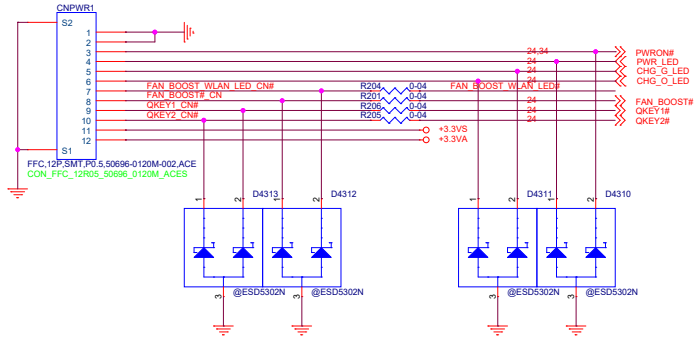
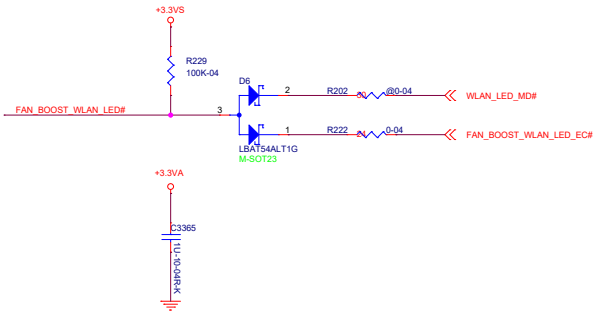
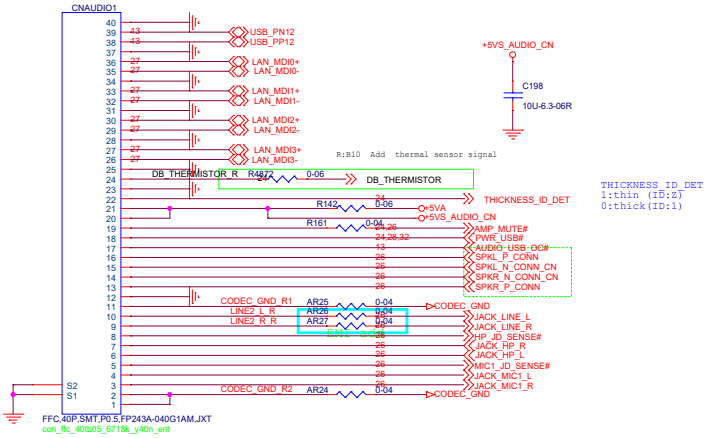
POWER DB CONN.

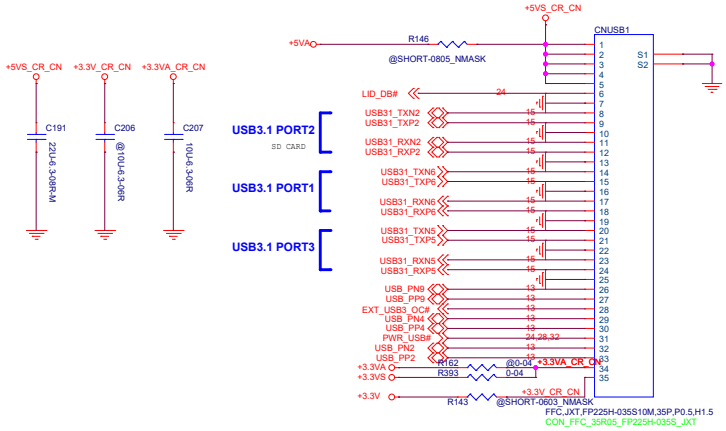




Audio&LAN DB CONN.



USB3.0 DB CONN.



同方国际信息技术有限公司

Title	PWR_DB/USB3.0 DB/Audio DB	
Size: Custom	Document Number: GK5MPFX	Rev: 1.0
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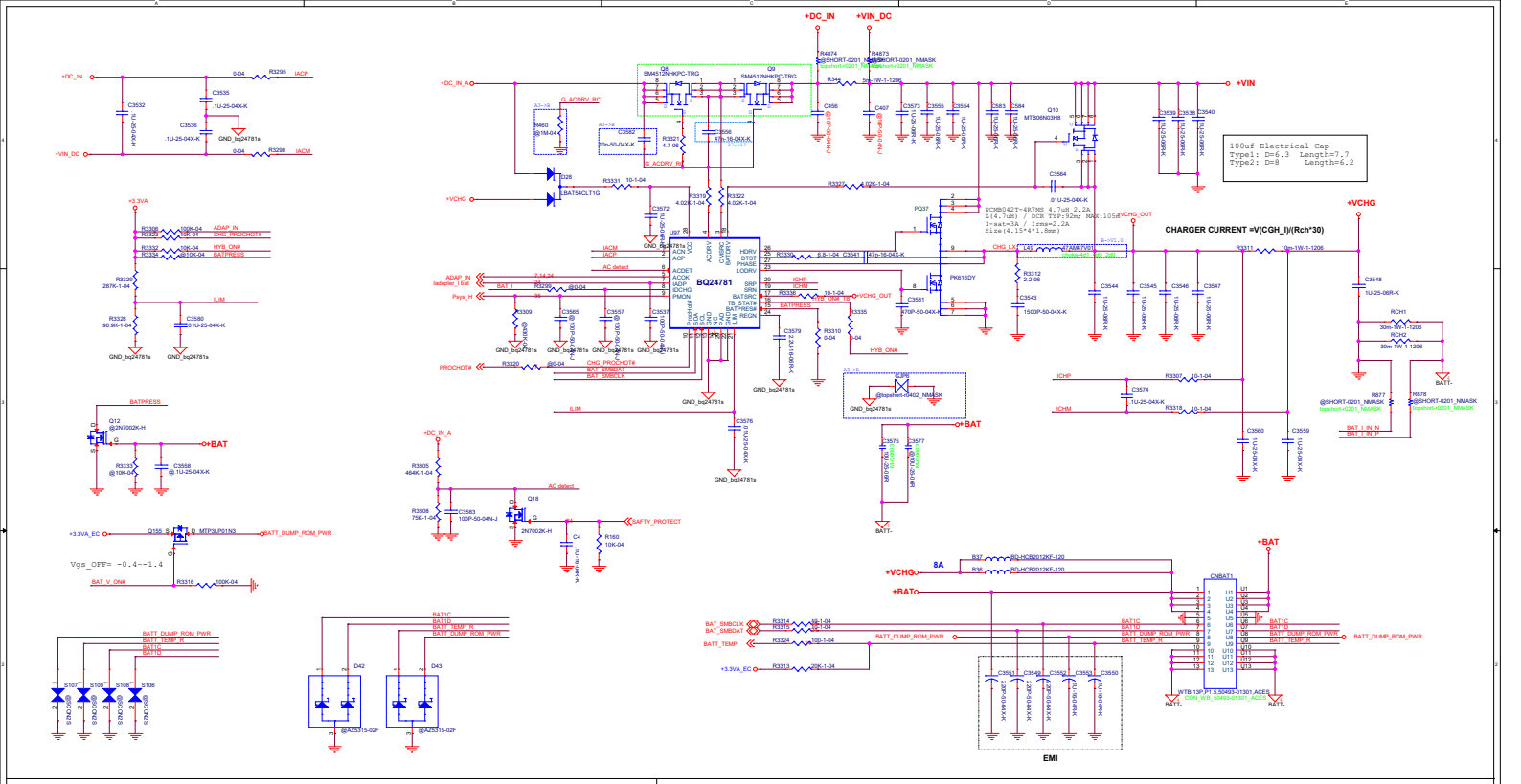
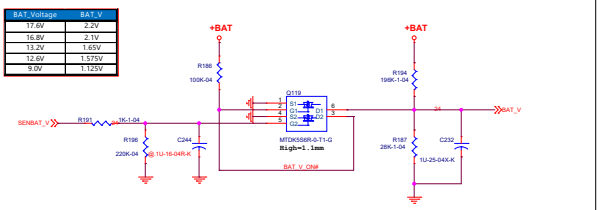
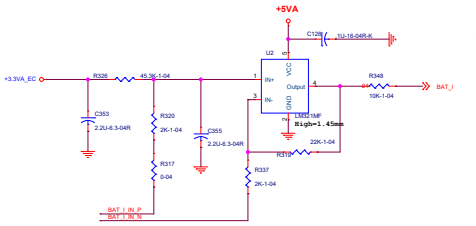


Battery Voltage Detect

BAT_Voltage	BAT_V
17.6V	2.2V
16.8V	2.1V
13.2V	1.65V
12.6V	1.575V
9.0V	1.125V



Battery Current Detect



RCH1 //RCH2 =7.5mohm

BAT_I	ICHG (0.0876V/1A)
2.0225V	4A
1.8473V	2A
1.7597V	1A
1.672V	0A
1.5844V	-1A
1.4968V	-2A
1.3216V	-4A
1.1464V	-6A
0.9712V	-8A
0.796V	-10A

RCH1 //RCH2 =15mohm

BAT_I	ICHG (0.1724V/1A)
2.3640V	4A
2.0192V	2A
1.8468V	1A
1.6744V	0A
1.5020V	-1A
1.3296V	-2A
0.9848V	-4A
0.6400V	-6A
0.2952V	-8A
0.1228V	-9A

Title	BATT IN/CHARGER(BQ24781)		
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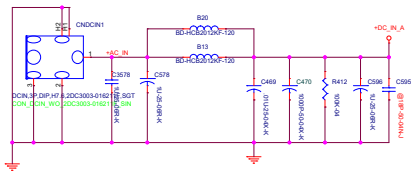
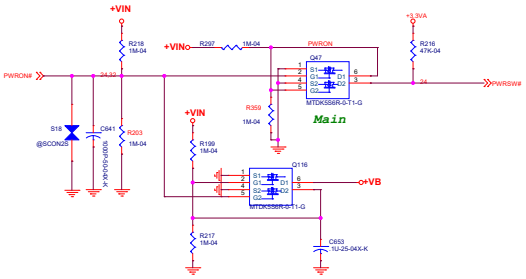
+DC_IN

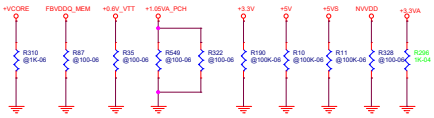


EMB20NP3V
ID=-13A TC=100 deg
Ipulse=-72A
Avalanche=-10A
9watt 1ms
15Watt 0.1ms

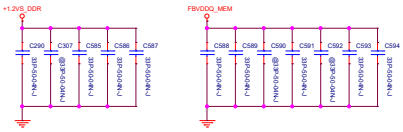
POWER SW



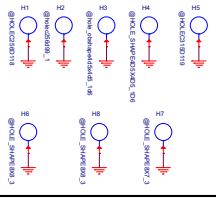
Discharge Resistor



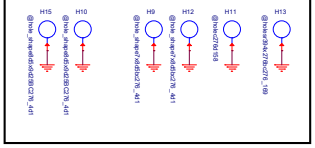
For RF



PCB HOLE



THERMAL HOLE



同方国际信息技术有限公司

Title	DC IN/PWR_SW/H-S CAP/SCREW	
Size: Custom	Document Number: GK5MPFX	Rev: 1.0
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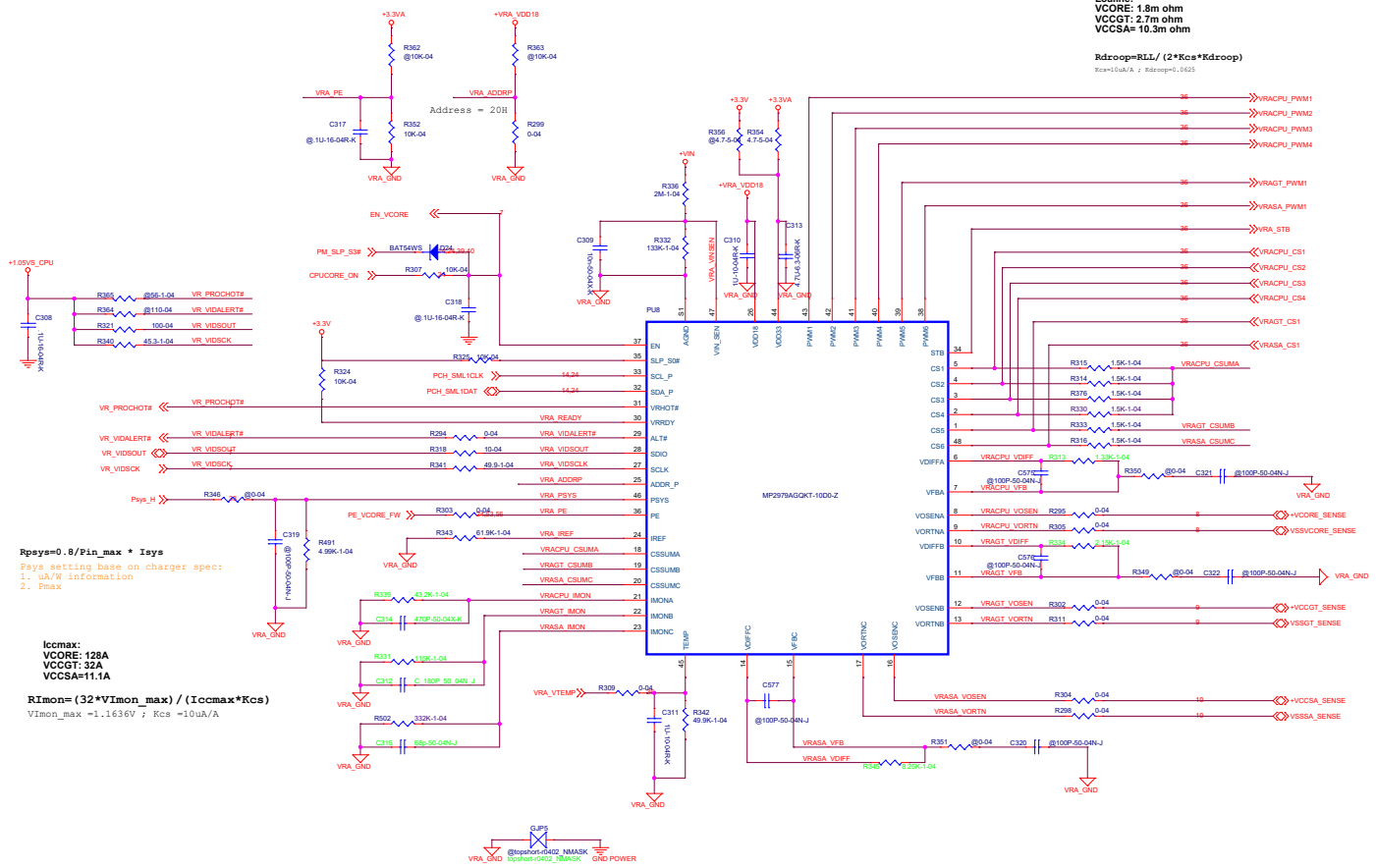
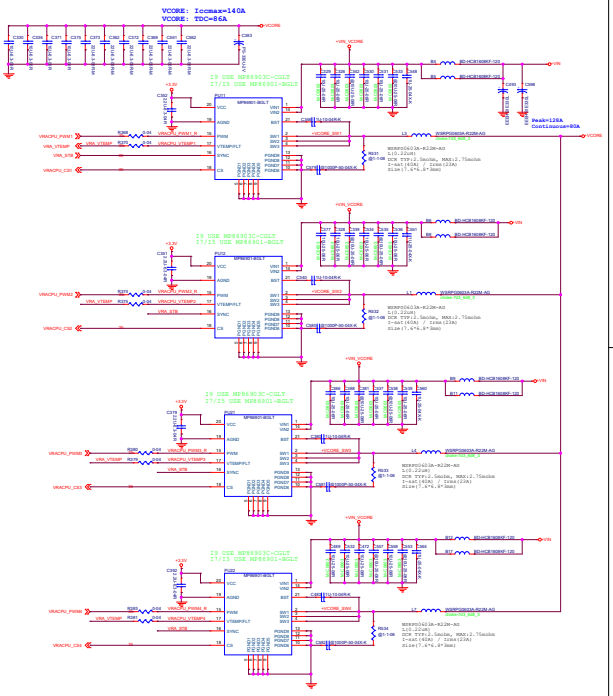


R:B9 Change value R339/C314/R331/C312/C315/R345/313/R334

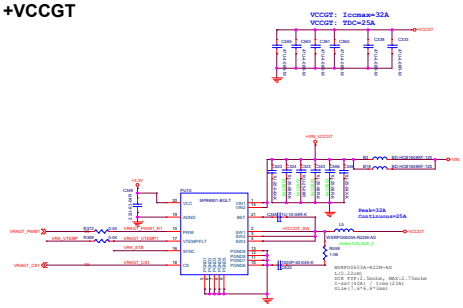
同方国际信息技术有限公司

Title	POWER VR CONTROLLER		
Size: Custom	Document Number: GK5MPFX		Rev: 1.0
Date: Thursday, December 19, 2019	Sheet 35 of 61		

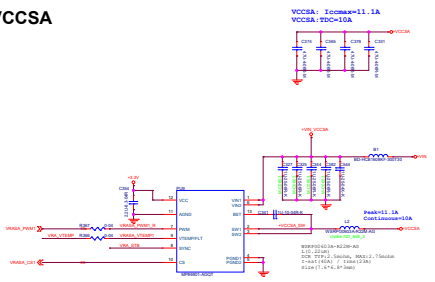
+VCORE



+VCCGT

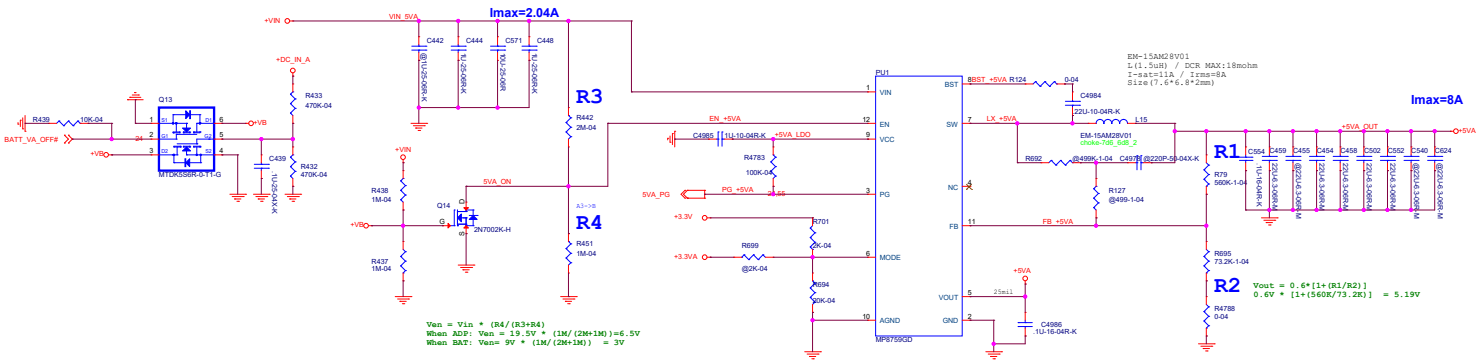


+VCCSA

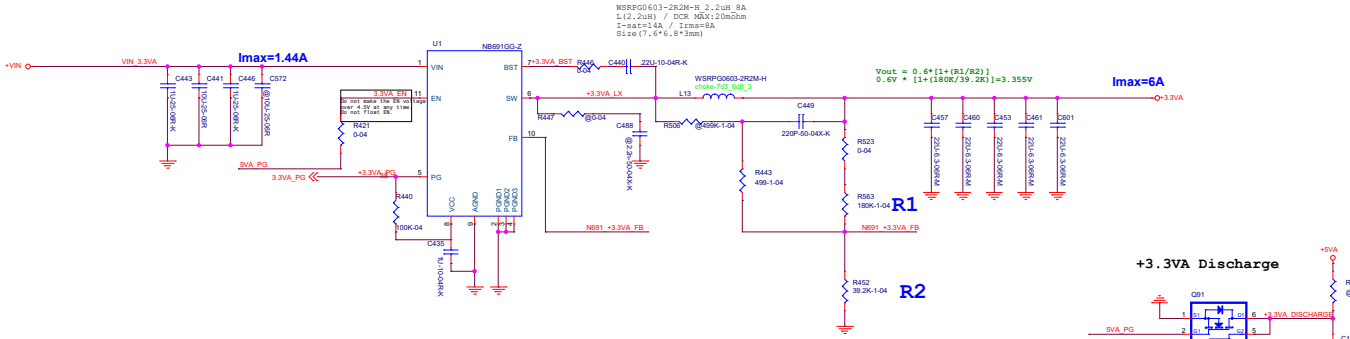


Title	POWER VCORE/VCCGT/VCCSA	
Size	Document Number	Rev
D	GK5MPFX	1.0
Date: Tuesday, November 26, 2019	Sheet 4 of 45	

+5VA



+3.3VA



同方国际信息技术有限公司			
Title	POWER +5VA/+3.3VA		
Size: Custom	Document Number: GK5MPFX		Rev: 1.0
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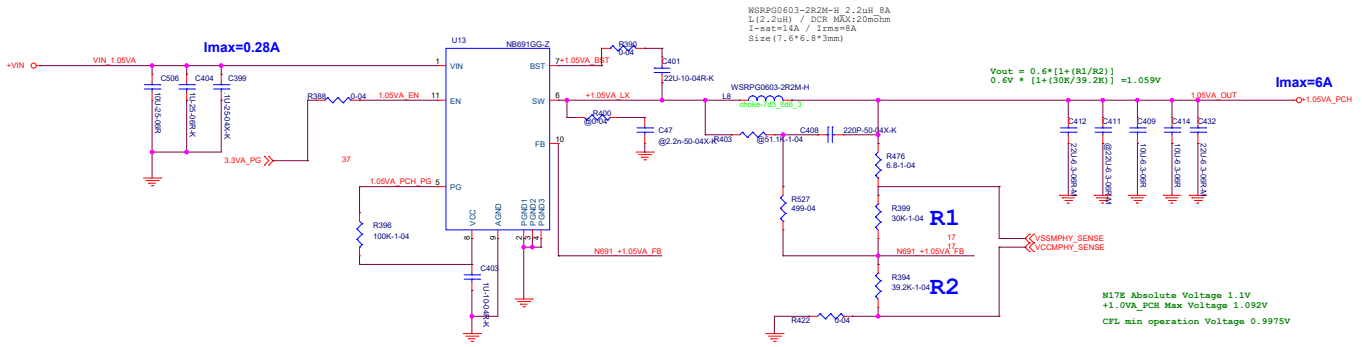
+1.05VA_PCH



同方国际信息技术有限公司

Title	POWER +1.8VA/+1.05VA_PCH		
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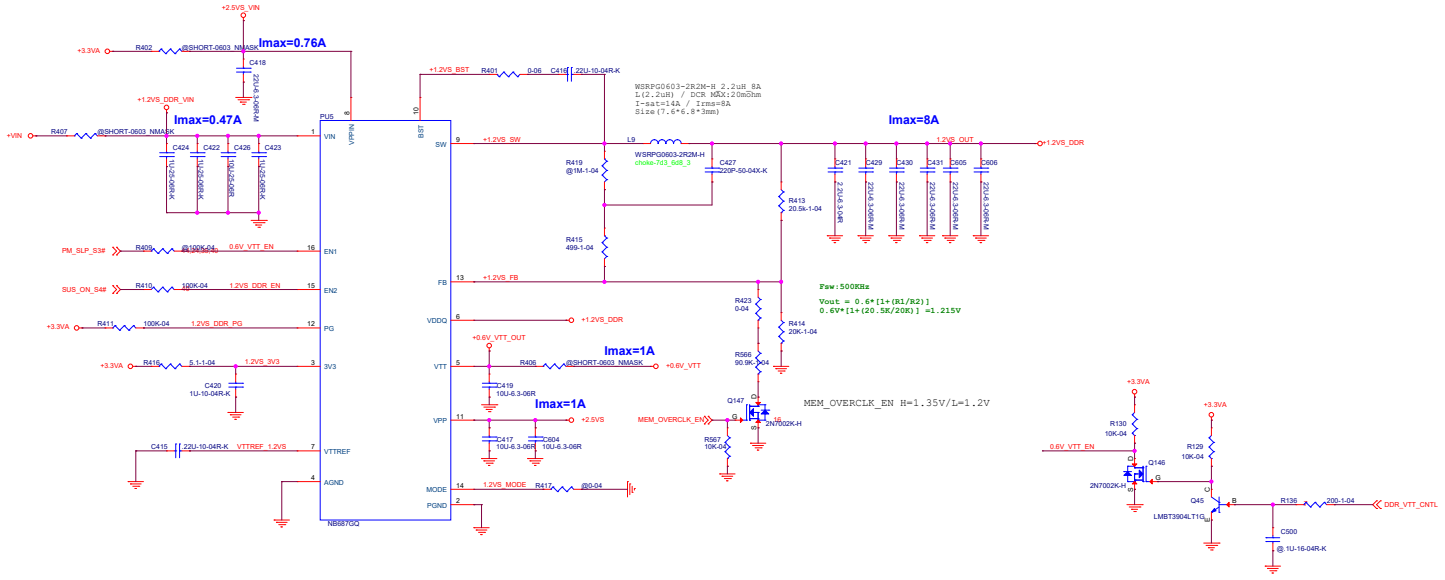
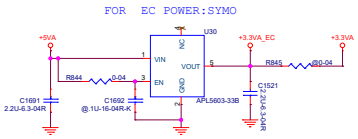
+1.2VS_DDR/+2.5VS/+0.6V_VTT



+3.3VA_EC



启方国际信息技术有限公司			
Title	POWER +1.2VS_DDR/2.5VS/VTT		
Size C	Document Number GK5MPFX		Rev 1.0
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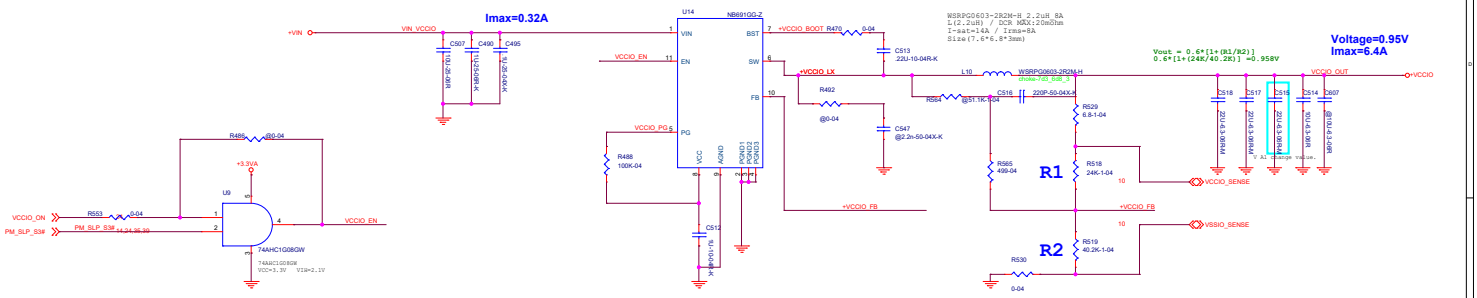
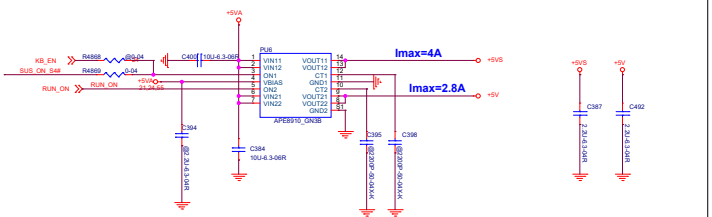
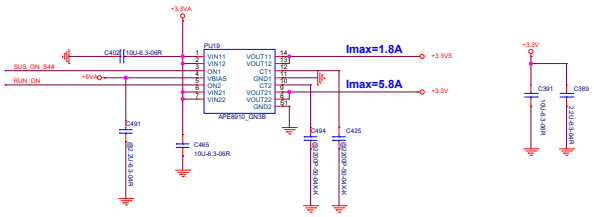
+VCCIO



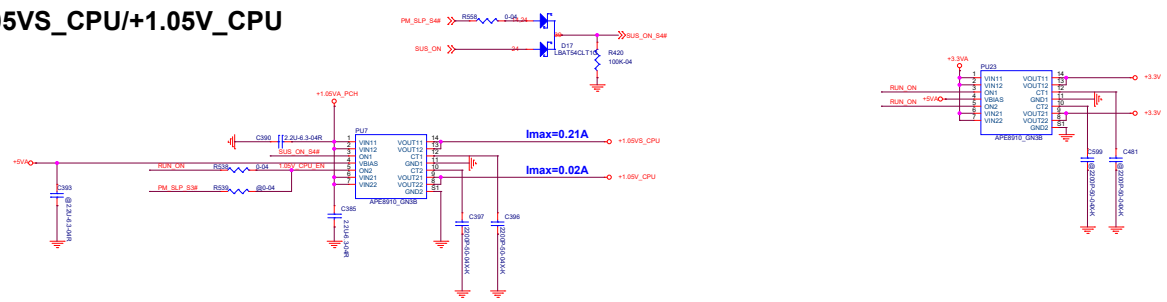
+5VS/+5V



+3.3VS/+3.3V



+1.05VS_CPU/+1.05V_CPU



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Title	POWER +VCCIO/+VS PWR/+V PWR		
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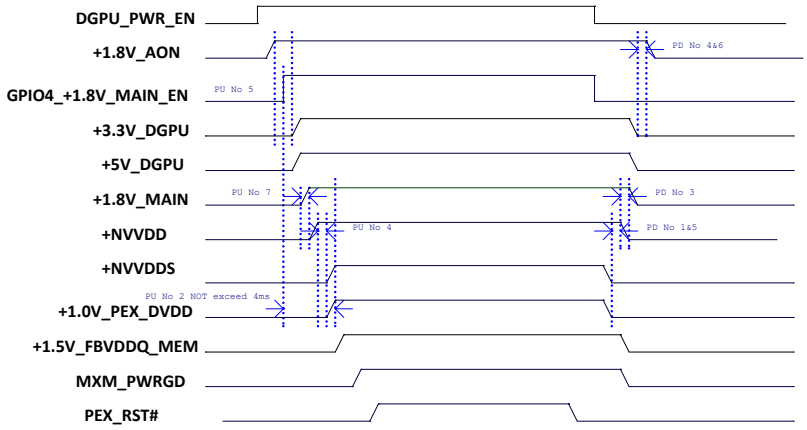
DGPU POWER SEQUENCE



POWER UP sequence is required:+1.8V_AON->+1.8V_MAIN->+NVVDD->+NVVDDS/+1.0V_PEX_DVDD->+1.5V_FBVDDQ_MEM
1.The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2.t1 From +1.8V_MAIN_EN to +1.0V_PEX_DVDD/+NVVDD_PGOOD) must NOT exceed 4ms.
3.The ramp-up overshoot should not exceed the silicon reliability limit voltage
4.Power up +NVVDD must be 90% before +1.0V+PEX_DVDD and NVVDDS can start ramp up.
5.Power up +1.8V_AON must be 90% before 3.3V ramp up.
6.All 3.3V devices that connect to the GPU must be powered after +1.8V_AON ; GPU can't have any 3.3V leakage path before +1.8V_AON present.
7.The propagation delay between +1.8V_MAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power up and power down.

POWER DOWN sequence is required
1.+NVVDDS/+1.0V_PEX_DVDD must ramp down before NVVDD.
2.All other power rails can ramp down together with NVVDD.
3.+1.8V_MAIN must power down after NVVDD power down
3.The progapation delay between +1.8VMAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power up and power down.
4.All 3.3V devices that connect to the GPU must be ramp down before +1.8V_AON; GPU can't have any 3.3V leakage path after +1.8V_AON and +1.8V_MAIN power down.
5.Power down NVVDDS and +1.0V_PEX_DVDD must be less than 10% before NVVDD can start ramp down.
6.Power down 3.3V must be less than 10% before +1.8V_AON can start ramp down.

同方国际信息技术有限公司

Title	N18P-G62 POWER SEQUENCE	
Size: Custom	Document Number: GK5MPFX	Rev: 1.0
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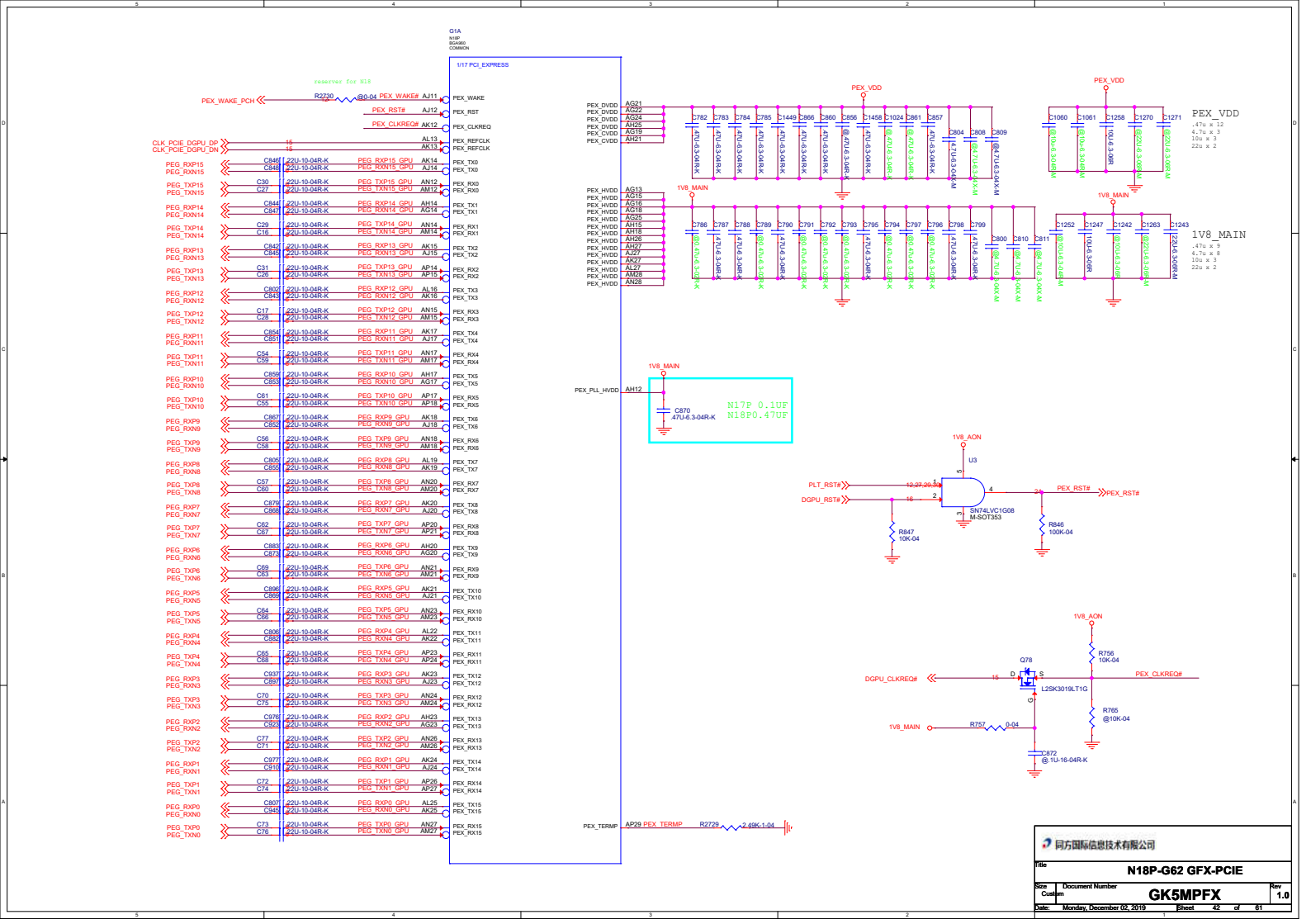
G1A
N18P
BGA680
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1/17 PCI_EXPRESS
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R2730
0-04
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PEX_RST#
PEX_CLKREQ#
CLK_PCIE_DGPU_DP
CLK_PCIE_DGPU_DN
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PEG_RXN15
PEG_TXP15
PEG_TXN15
PEG_RXP14
PEG_RXN14
PEG_TXP14
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PEG_RXN13
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PEX_DVDD
PEX_HVDD
PEX_CVDD
1V8_MAIN
PEX_PLL_HVDD
C870
.47U-6.3-04R-K
N17P 0.1UF
N18P0.47UF
PEX_TERMP
R2729
2.49K-1-04
1V8_AON
U3
SN74LVC1G08
M-SOT353
PLT_RST#
DGPU_RST#
PEX_RST#
R847
10K-04
R846
100K-04
DGPU_CLKREQ#
PEX_CLKREQ#
Q78
L2SK3019LT1G
R756
10K-04
R765
@10K-04
R757
0-04
C872
@.1U-16-04R-K
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N18P-G62 GFX-PCIE
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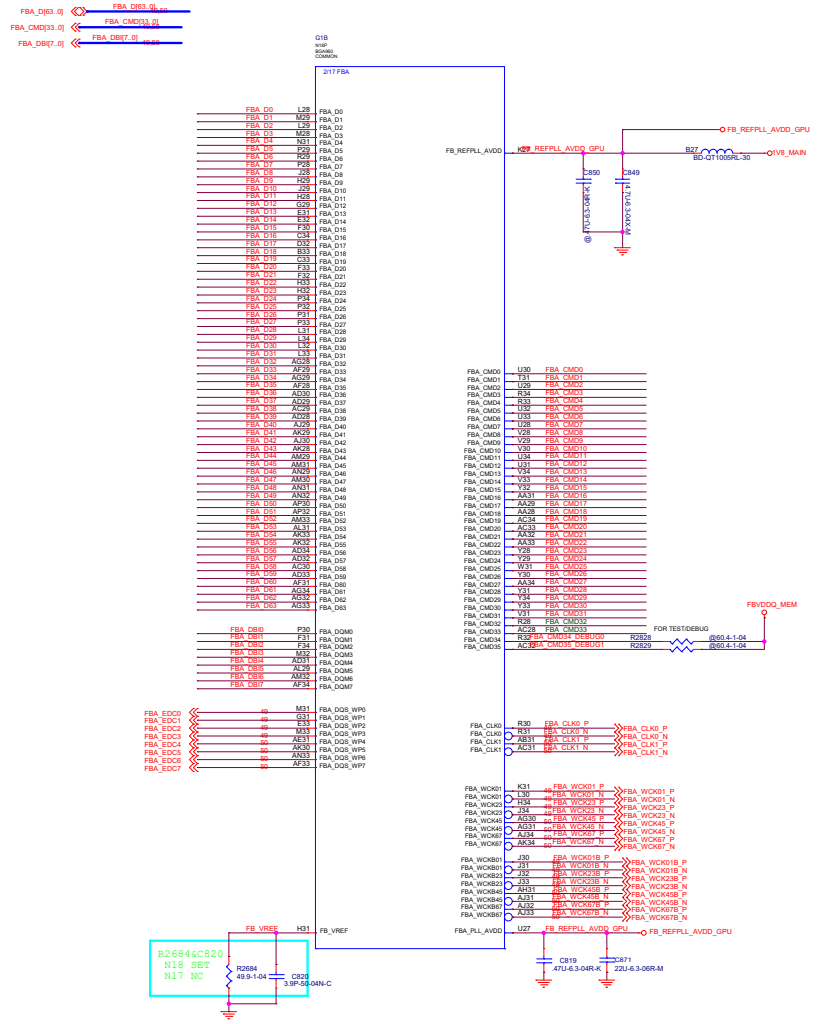
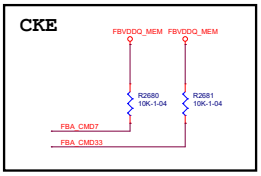
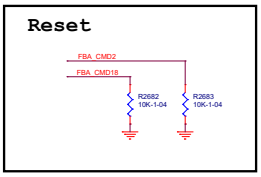


Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*





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Title	N18P-G62 FrameBuffer A		
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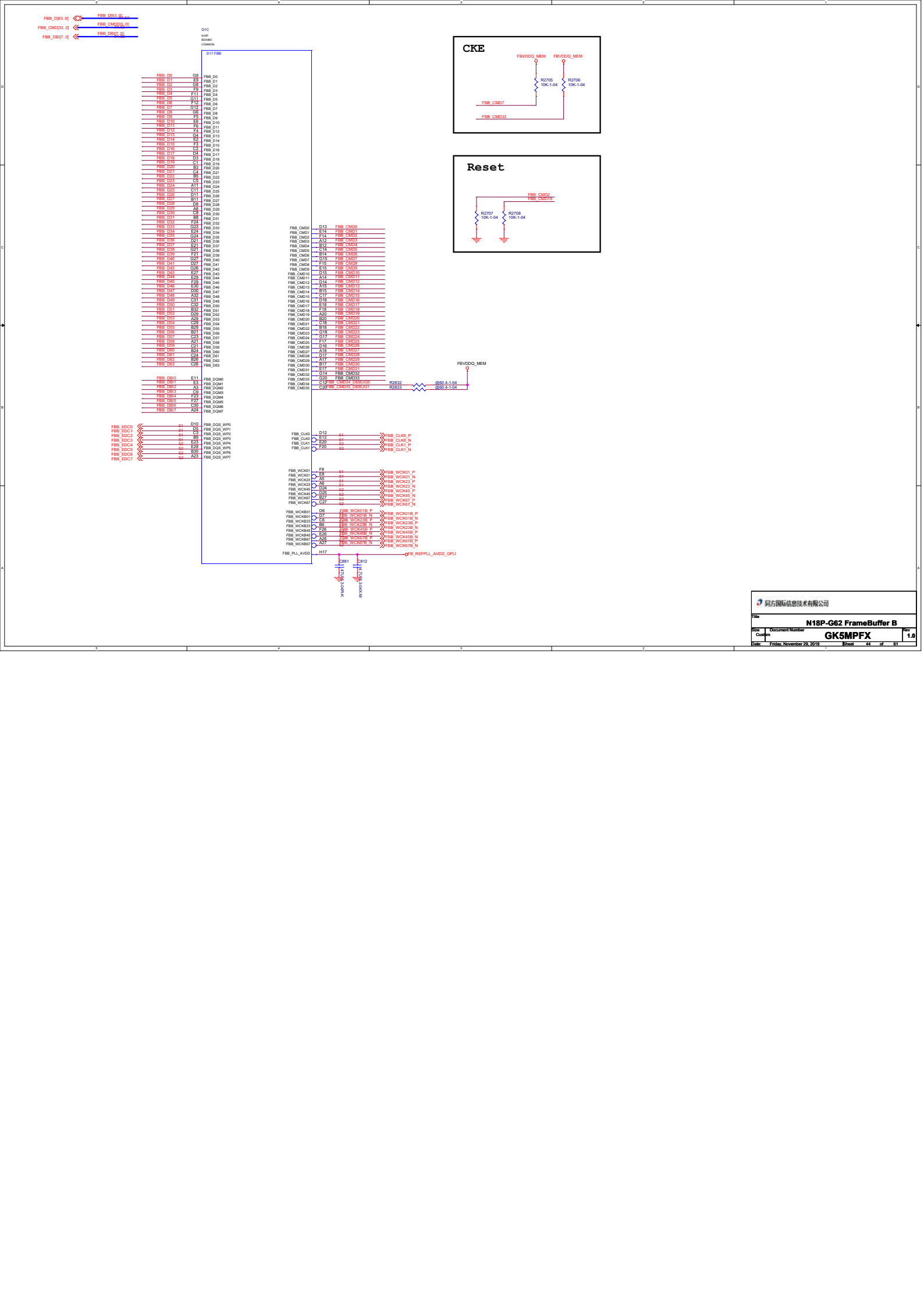
FBB_DI[63..0]
FBB_CMDI[33..0]
FBB_DBI[7..0]
G1C
N18P
BGA960
COMMON
3/17 FBB
FBB_D0 G9 FBB_D0
FBB_D1 E9 FBB_D1
FBB_D2 G8 FBB_D2
FBB_D3 F9 FBB_D3
FBB_D4 F11 FBB_D4
FBB_D5 G11 FBB_D5
FBB_D6 F12 FBB_D6
FBB_D7 G12 FBB_D7
FBB_D8 G6 FBB_D8
FBB_D9 F5 FBB_D9
FBB_D10 E6 FBB_D10
FBB_D11 F6 FBB_D11
FBB_D12 F4 FBB_D12
FBB_D13 G4 FBB_D13
FBB_D14 E2 FBB_D14
FBB_D15 F3 FBB_D15
FBB_D16 C2 FBB_D16
FBB_D17 D4 FBB_D17
FBB_D18 D3 FBB_D18
FBB_D19 C1 FBB_D19
FBB_D20 B3 FBB_D20
FBB_D21 C4 FBB_D21
FBB_D22 B5 FBB_D22
FBB_D23 C5 FBB_D23
FBB_D24 A11 FBB_D24
FBB_D25 C11 FBB_D25
FBB_D26 D11 FBB_D26
FBB_D27 B11 FBB_D27
FBB_D28 D8 FBB_D28
FBB_D29 A6 FBB_D29
FBB_D30 C8 FBB_D30
FBB_D31 B8 FBB_D31
FBB_D32 F24 FBB_D32
FBB_D33 G23 FBB_D33
FBB_D34 E24 FBB_D34
FBB_D35 G24 FBB_D35
FBB_D36 D21 FBB_D36
FBB_D37 E21 FBB_D37
FBB_D38 G21 FBB_D38
FBB_D39 F21 FBB_D39
FBB_D40 G27 FBB_D40
FBB_D41 D27 FBB_D41
FBB_D42 G26 FBB_D42
FBB_D43 E27 FBB_D43
FBB_D44 E29 FBB_D44
FBB_D45 F29 FBB_D45
FBB_D46 E30 FBB_D46
FBB_D47 D30 FBB_D47
FBB_D48 A32 FBB_D48
FBB_D49 C31 FBB_D49
FBB_D50 C32 FBB_D50
FBB_D51 B32 FBB_D51
FBB_D52 D29 FBB_D52
FBB_D53 A29 FBB_D53
FBB_D54 C29 FBB_D54
FBB_D55 B29 FBB_D55
FBB_D56 B21 FBB_D56
FBB_D57 C23 FBB_D57
FBB_D58 A21 FBB_D58
FBB_D59 C21 FBB_D59
FBB_D60 B24 FBB_D60
FBB_D61 C24 FBB_D61
FBB_D62 B26 FBB_D62
FBB_D63 C26 FBB_D63
FBB_DBI0 E11 FBB_DQM0
FBB_DBI1 E3 FBB_DQM1
FBB_DBI2 A3 FBB_DQM2
FBB_DBI3 C9 FBB_DQM3
FBB_DBI4 F23 FBB_DQM4
FBB_DBI5 F27 FBB_DQM5
FBB_DBI6 C30 FBB_DQM6
FBB_DBI7 A24 FBB_DQM7
FBB_EDC0 D10 FBB_DQS_WP0
FBB_EDC1 D5 FBB_DQS_WP1
FBB_EDC2 C3 FBB_DQS_WP2
FBB_EDC3 B9 FBB_DQS_WP3
FBB_EDC4 E23 FBB_DQS_WP4
FBB_EDC5 E28 FBB_DQS_WP5
FBB_EDC6 B30 FBB_DQS_WP6
FBB_EDC7 A23 FBB_DQS_WP7
FBB_CMD0 D13 FBB_CMD0
FBB_CMD1 E14 FBB_CMD1
FBB_CMD2 F14 FBB_CMD2
FBB_CMD3 A12 FBB_CMD3
FBB_CMD4 B12 FBB_CMD4
FBB_CMD5 C14 FBB_CMD5
FBB_CMD6 B14 FBB_CMD6
FBB_CMD7 G15 FBB_CMD7
FBB_CMD8 F15 FBB_CMD8
FBB_CMD9 E15 FBB_CMD9
FBB_CMD10 D15 FBB_CMD10
FBB_CMD11 A14 FBB_CMD11
FBB_CMD12 D14 FBB_CMD12
FBB_CMD13 A15 FBB_CMD13
FBB_CMD14 B15 FBB_CMD14
FBB_CMD15 C17 FBB_CMD15
FBB_CMD16 D18 FBB_CMD16
FBB_CMD17 E18 FBB_CMD17
FBB_CMD18 F18 FBB_CMD18
FBB_CMD19 A20 FBB_CMD19
FBB_CMD20 B20 FBB_CMD20
FBB_CMD21 C18 FBB_CMD21
FBB_CMD22 B18 FBB_CMD22
FBB_CMD23 G18 FBB_CMD23
FBB_CMD24 G17 FBB_CMD24
FBB_CMD25 F17 FBB_CMD25
FBB_CMD26 D16 FBB_CMD26
FBB_CMD27 A18 FBB_CMD27
FBB_CMD28 D17 FBB_CMD28
FBB_CMD29 A17 FBB_CMD29
FBB_CMD30 B17 FBB_CMD30
FBB_CMD31 E17 FBB_CMD31
FBB_CMD32 G14 FBB_CMD32
FBB_CMD33 G20 FBB_CMD33
FBB_CMD34 C12 FBB_CMD34_DEBUG0
FBB_CMD35 C20 FBB_CMD35_DEBUG1
R2832 @60.4-1-04
R2833 @60.4-1-04
FBVDDQ_MEM
FBB_CLK0 D12
FBB_CLK0 E12
FBB_CLK1 E20
FBB_CLK1 F20
FBB_CLK0_P
FBB_CLK0_N
FBB_CLK1_P
FBB_CLK1_N
FBB_WCK01 F8
FBB_WCK01 E8
FBB_WCK23 A5
FBB_WCK23 A6
FBB_WCK45 D24
FBB_WCK45 D25
FBB_WCK67 B27
FBB_WCK67 C27
FBB_WCK01_P
FBB_WCK01_N
FBB_WCK23_P
FBB_WCK23_N
FBB_WCK45_P
FBB_WCK45_N
FBB_WCK67_P
FBB_WCK67_N
FBB_WCKB01 D6
FBB_WCKB01 D7
FBB_WCKB23 C6
FBB_WCKB23 B6
FBB_WCKB45 F26
FBB_WCKB45 E26
FBB_WCKB67 A26
FBB_WCKB67 A27
FBB_WCK01B_P
FBB_WCK01B_N
FBB_WCK23B_P
FBB_WCK23B_N
FBB_WCK45B_P
FBB_WCK45B_N
FBB_WCK67B_P
FBB_WCK67B_N
FBB_WCK01B_P
FBB_WCK01B_N
FBB_WCK23B_P
FBB_WCK23B_N
FBB_WCK45B_P
FBB_WCK45B_N
FBB_WCK67B_P
FBB_WCK67B_N
FBB_PLL_AVDD H17
FB_REFPLL_AVDD_GPU
C881 1U/10V_X5R1K
C812 1U/10V_X5R1K
CKE
FBVDDQ_MEM
FBVDDQ_MEM
R2705 10K-1-04
R2706 10K-1-04
FBB_CMD7
FBB_CMD33
Reset
FBB_CMD2
FBB_CMD18
R2707 10K-1-04
R2708 10K-1-04
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N18P-G62 FrameBuffer B
Size Custom
Document Number GK5MPFX
Rev 1.0
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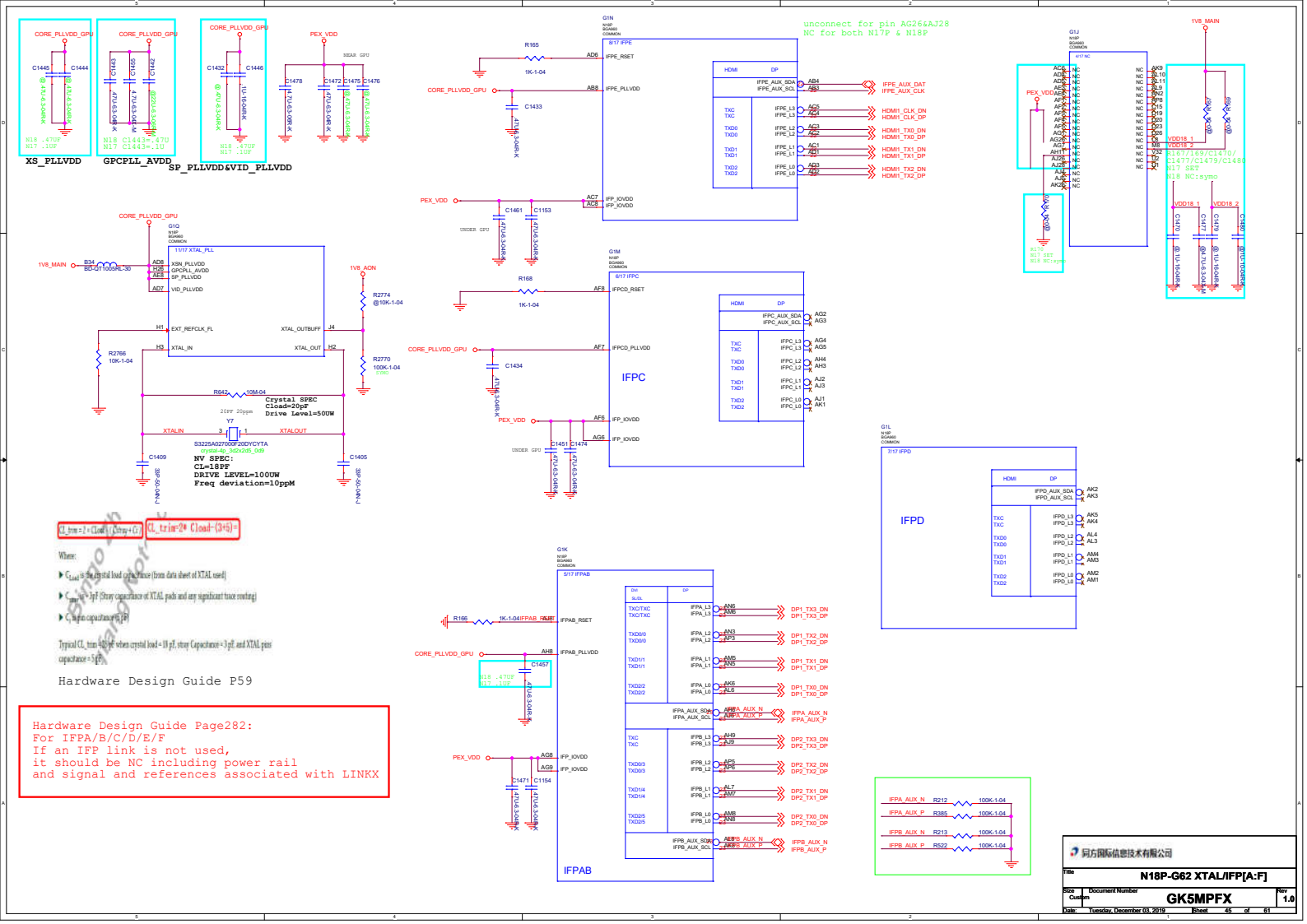
CORE_PLLVDD_GPU
C1445
C1444
XS_PLLVDD
GPCPLL_AVDD
SP_PLLVDD&VID_PLLVDD
PEX_VDD
R165
1K-1-04
IFPE_RSET
IFPE_PLLVDD
C1433
unconnect for pin AG26&AJ28
NC for both N17P & N18P
IFPE_AUX_DAT
IFPE_AUX_CLK
HDMI1_CLK_DN
HDMI1_CLK_DP
HDMI1_TX0_DN
HDMI1_TX0_DP
HDMI1_TX1_DN
HDMI1_TX1_DP
HDMI1_TX2_DN
HDMI1_TX2_DP
C1461
C1153
IFP_IOVDD
R168
IFPCD_RSET
IFPCD_PLLVDD
C1434
IFPC
C1451
C1474
1V8_MAIN
1V8_AON
R2774
@10K-1-04
R2766
10K-1-04
R2770
100K-1-04
R642
10M-04
Crystal SPEC
Cload=20pF
Drive Level=50UW
Y7
S3225A027000F20DYCYTA
NV SPEC:
CL=18PF
DRIVE LEVEL=100UW
Freq deviation=10ppm
C1409
C1405
Hardware Design Guide P59
Hardware Design Guide Page282:
For IFPA/B/C/D/E/F
If an IFP link is not used,
it should be NC including power rail
and signal and references associated with LINKX
IFPD
IFPAB
R166
IFPAB_RSET
IFPAB_PLLVDD
C1457
C1471
C1154
IFPA_AUX_N
IFPA_AUX_P
IFPB_AUX_N
IFPB_AUX_P
R212
R385
R213
R522
100K-1-04
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N18P-G62 XTAL/IFP[A:F]
GK5MPFX
Tuesday, December 03, 2019
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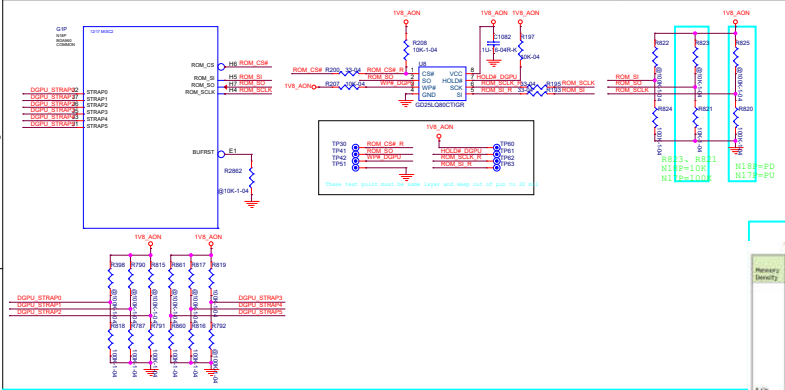

GDDR5 CFG Setting

Density	Vendor	Part Number	Strap	Strap 2	Strap 1	Strap 0
8Gb	Samsung	K4G80325FB-HC28 B-die	0X0	L	L	L
8Gb	Micron	MT51J256M32HF-70:A A-die	0X1	L	L	H
8Gb	Hynix	H5GC8H24MJR-ROC M-die	0X2	L	H	L
			0X3	L	H	H
8Gb	Micron	MT51J256M32HF-70/80-B	0X4	H	L	L
8Gb	Hynix	H5GC8H24AJR-R0C/R2C	0X5	H	L	H
4Gb	Samsung	K4G41325FE-HC28 E-die	0X7	H	H	H
4Gb	Micron	H5GC4H24AJR-ROC A-die	0X6	H	H	L
4Gb	Hynix	EDW4032BABG-70-F A-die	0X8	L	L	M

N18P STRAPS

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins (see Note)			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

Table 12.3 RAMCFG

Strap Pins (see Note)			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35 V and 1.5V[1]	Micron	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0x2	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.5V[1]	Samsung	K4G80325FC-HC25	C-die	0x0	8 Gbps	N/A	Full	Production candidate

Table 12.4 FS_OVERT* Strap Enablement

Strap Pins (see Note 1)			FS_OVERT* Function
ROM_SO (see Note 2)	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note 1: Configurations other than the two listed in Table 12.4 must be avoided, as otherwise damage to strap inputs may result.

Note 2: The ROM_SO pin should be pulled low using a 10 kΩ resistor instead of a 100 kΩ resistor.

	Voltage (V)		
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

N17P STRAPS

Table 5.3 RAMCFG

Strap Pins (see Note)			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

SOR_EXPOSED Audio Configuration Straps

Table 5.4 Display Link to SORx_EXPOSED Mapping for Down Designs

Total Display Links (DMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	Is IFPD used? (Only supports eDP.)	See This Row of Table 5.5
4	4	NO	15
4	3	YES	13
3	3	NO	14
3	2	YES	12
2	2	NO	12
2	1	YES	8
1	1	NO	8
1	0	YES	0
No other configurations are supported.			

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins (see Note 1)			Resulting SORx_EXPOSED Enablements			
	ROM_SO (see Note 2)	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

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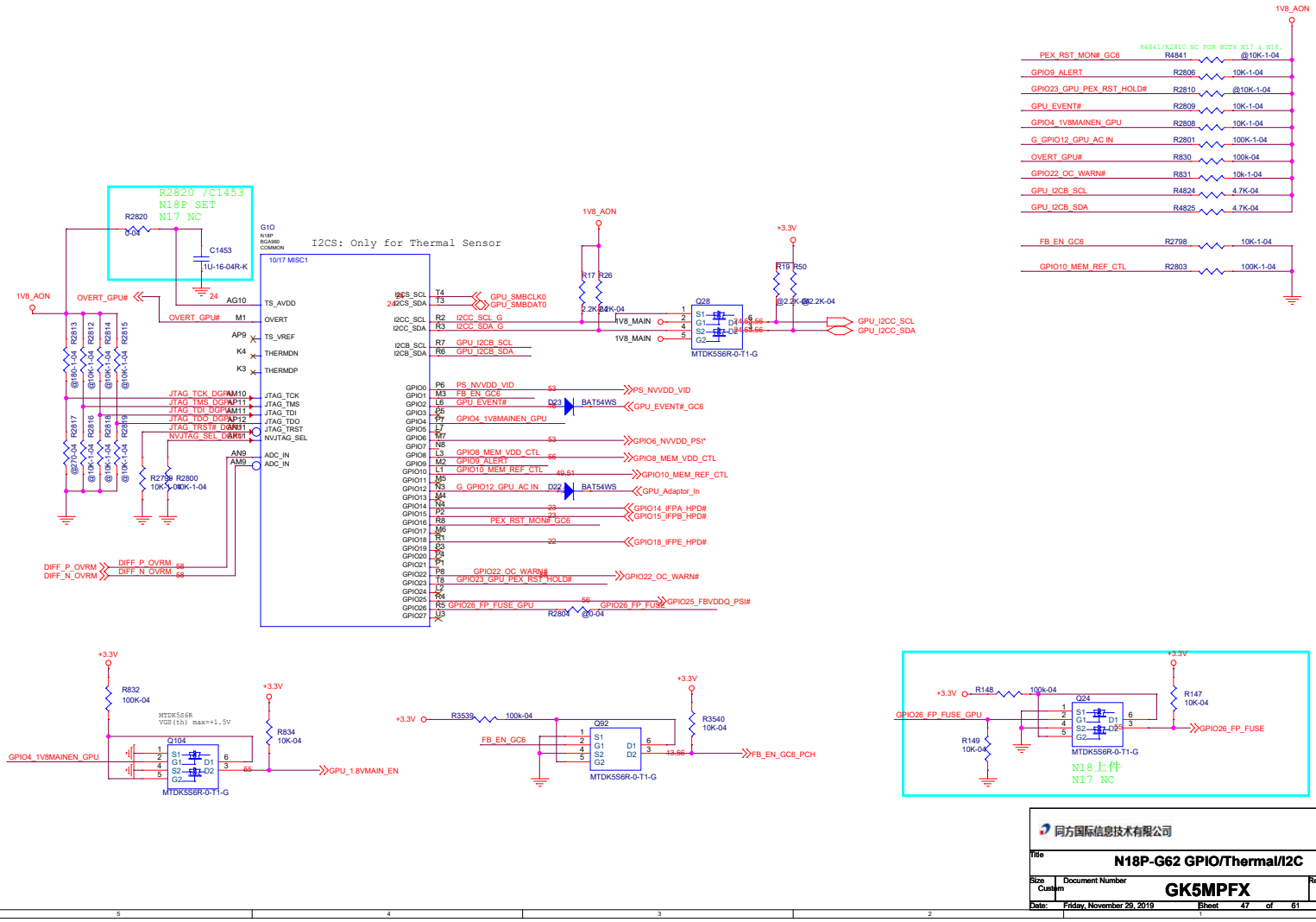
Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins (Note 1)			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

N17X HW DG(DG-07875-001_v09) Page. 78

昇东国际信息技术有限公司	
Title	N18P-G62 STRAP/Serial ROM
Size / Custom	Document Number: GK5MPFX
Rev	1.0
Date: Friday, November 29, 2019	Sheet 46 of 61


R2820 /C1453
N18P SET
N17 NC
I2CS: Only for Thermal Sensor
1V8_AON
+3.3V
R4841/R2810 NC FOR BOTH N17 & N18.
PEX_RST_MON#_GC6
GPIO9_ALERT
GPIO23_GPU_PEX_RST_HOLD#
GPU_EVENT#
GPIO4_1V8MAINEN_GPU
G_GPIO12_GPU_AC IN
OVERT_GPU#
GPIO22_OC_WARN#
GPU_I2CB_SCL
GPU_I2CB_SDA
FB_EN_GC6
GPIO10_MEM_REF_CTL
GPIO0 PS_NVVDD_VID
GPIO1 FB_EN_GC6
GPIO2 GPU_EVENT#
GPIO3 BAT54WS
GPIO4 GPIO4_1V8MAINEN_GPU
GPIO6 GPIO6_NVVDD_PSI*
GPIO8 GPIO8_MEM_VDD_CTL
GPIO9 GPIO9_ALERT
GPIO10 GPIO10_MEM_REF_CTL
GPIO12 G_GPIO12_GPU_AC IN
GPIO14 GPIO14_IFPA_HPD#
GPIO15 GPIO15_IFPB_HPD#
GPIO16 PEX_RST_MON#_GC6
GPIO18 GPIO18_IFPE_HPD#
GPIO22 GPIO22_OC_WARN#
GPIO23 GPIO23_GPU_PEX_RST_HOLD#
GPIO25 GPIO25_FBVDDQ_PSI#
GPIO26 GPIO26_FP_FUSE_GPU
GPIO26_FP_FUSE
JTAG_TCK_DGPU
JTAG_TMS_DGPU
JTAG_TDI_DGPU
JTAG_TDO_DGPU
JTAG_TRST#_DGPU
NVJTAG_SEL_DGPU
DIFF_P_OVRM
DIFF_N_OVRM
GPU_I2CC_SCL
GPU_I2CC_SDA
GPU_SMBCLK0
GPU_SMBDAT0
GPU_I2CB_SCL
GPU_I2CB_SDA
GPU_Adaptor_In
GPU_EVENT#_GC6
PS_NVVDD_VID
GPIO6_NVVDD_PSI*
GPIO8_MEM_VDD_CTL
GPIO10_MEM_REF_CTL
GPIO14_IFPA_HPD#
GPIO15_IFPB_HPD#
GPIO18_IFPE_HPD#
GPIO22_OC_WARN#
GPIO25_FBVDDQ_PSI#
GPIO26_FP_FUSE
GPU_1.8VMAIN_EN
FB_EN_GC6_PCH
N18上件
N17 NC
同方国际信息技术有限公司
N18P-G62 GPIO/Thermal/I2C
GK5MPFX
1.0
Friday, November 29, 2019
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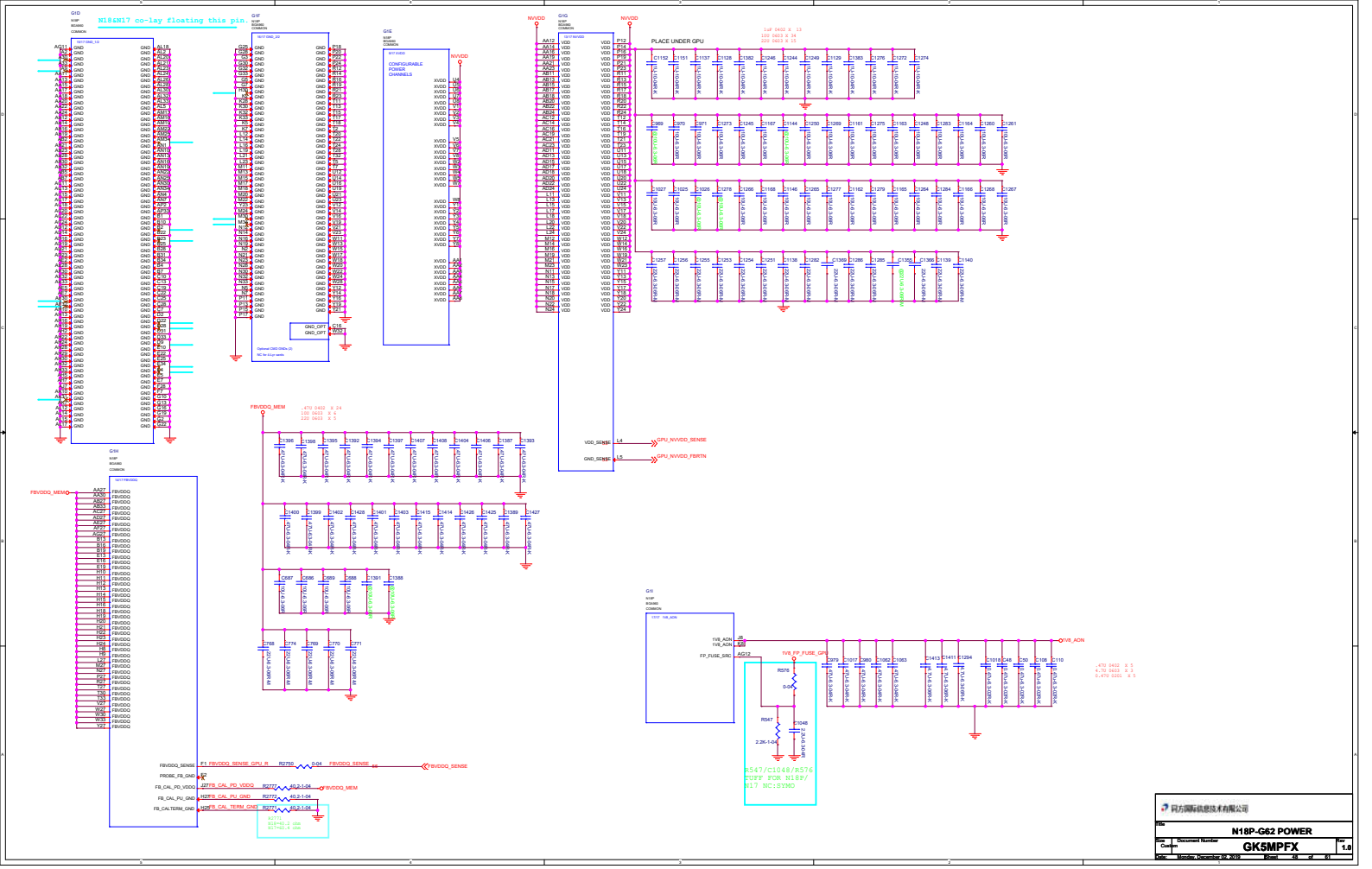
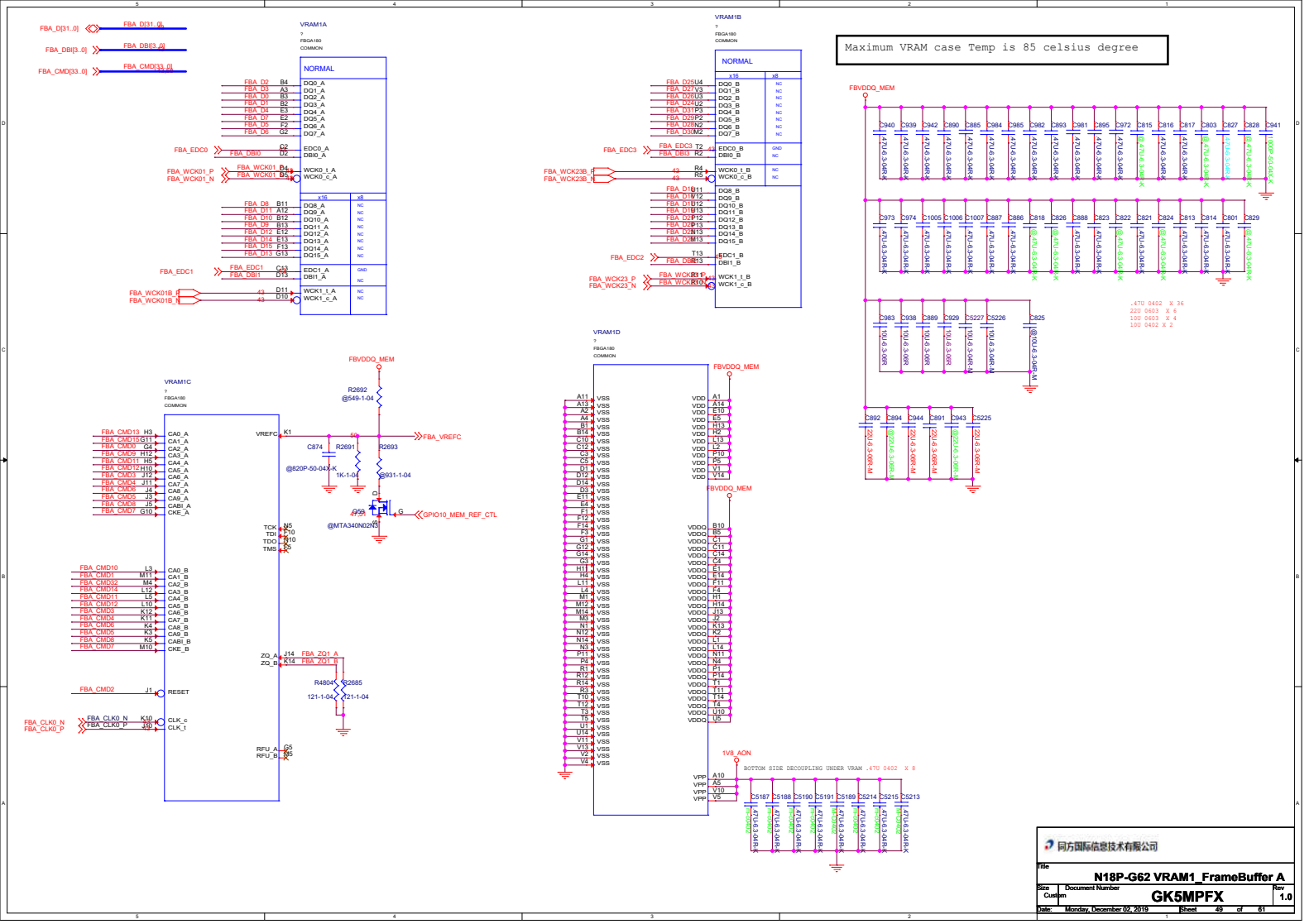
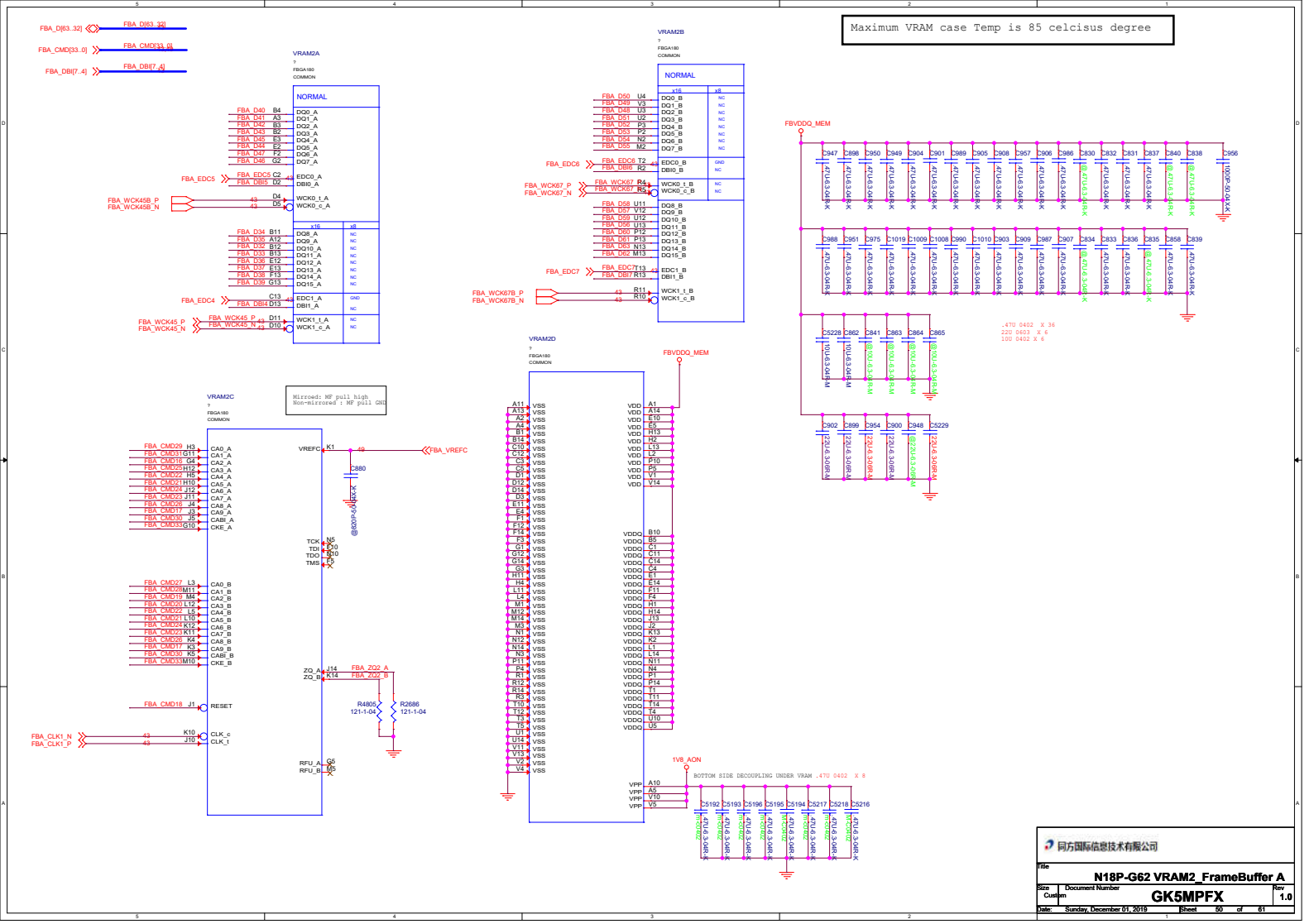
61


N18&N17 co-lay floating this pin
PLACE UNDER GPU
NVVDD
FBVDDQ_MEM
GND_OPT
VDD_SENSE
GND_SENSE
GPU_NVVDD_SENSE
GPU_NVVDD_FBRTN
TVS_ACN
FBVDDQ_SENSE
PROBE_FB_GND
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
R547/C1048/R576
TUFF FOR N18P/
N17 NC!SYMO
N18P-G62 POWER
GK5MPFX
Monday, December 02, 2019



同方国际信息技术有限公司

Title	N18P-G62 VRAM1_FrameBuffer A		
Size: Custom	Document Number: GK5MPFX		Rev: 1.0
Date: Monday, December 02, 2019	Sheet 49 of 61		


Maximum VRAM case Temp is 85 celcisus degree
VRAM2A
VRAM2B
VRAM2C
VRAM2D
NORMAL
FBVDDQ_MEM
1V8_AON
Mirrored: MF pull high
Not-mirrored : MF pull GND
BOTTOM SIDE DECOUPLING UNDER VRAM .47U 0402 X 8
.47U 0402 X 36
22U 0603 X 6
10U 0402 X 6
同方国际信息技术有限公司
N18P-G62 VRAM2_FrameBuffer A
GK5MPFX
Sunday, December 01, 2019
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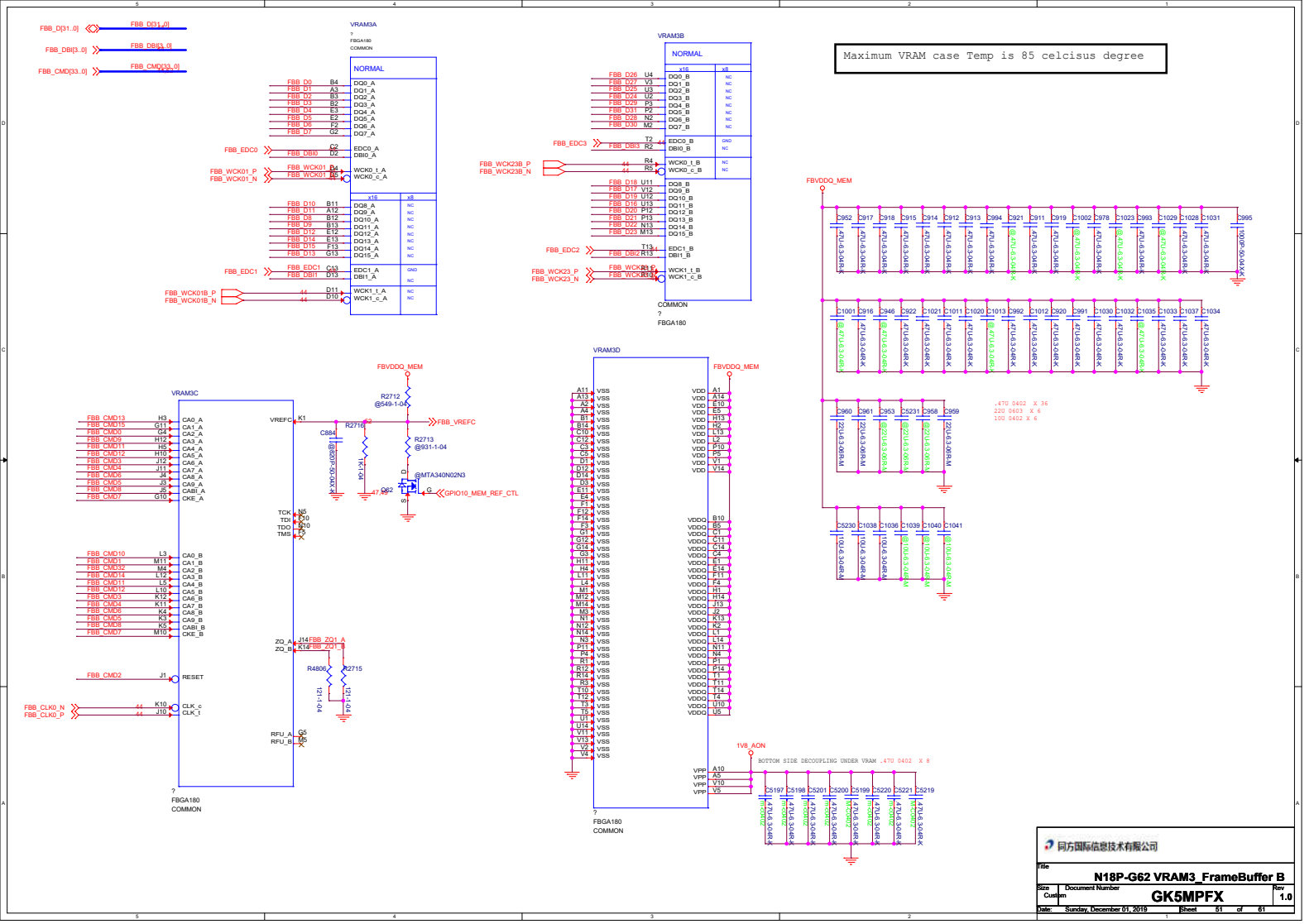
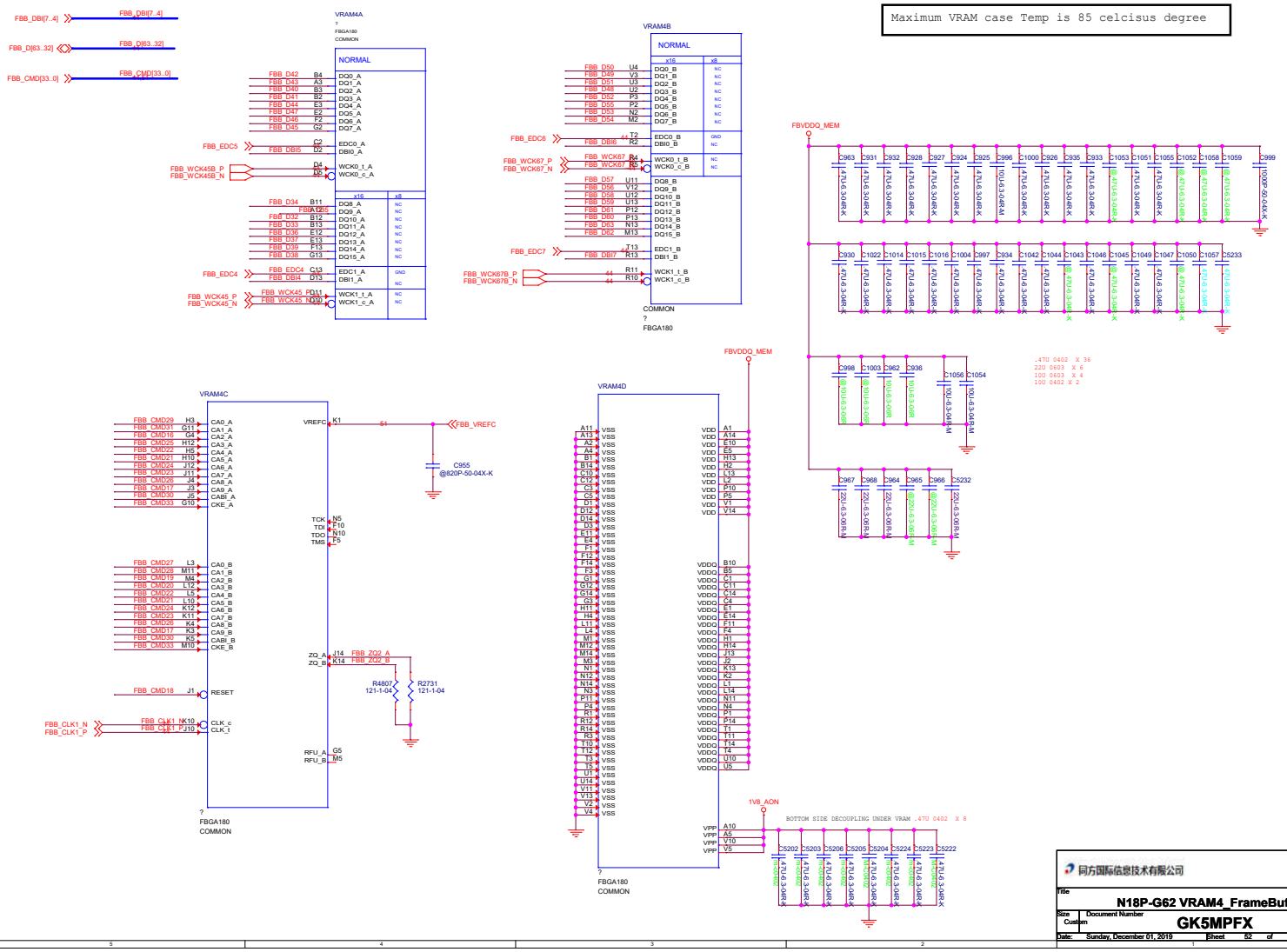
61
1.0

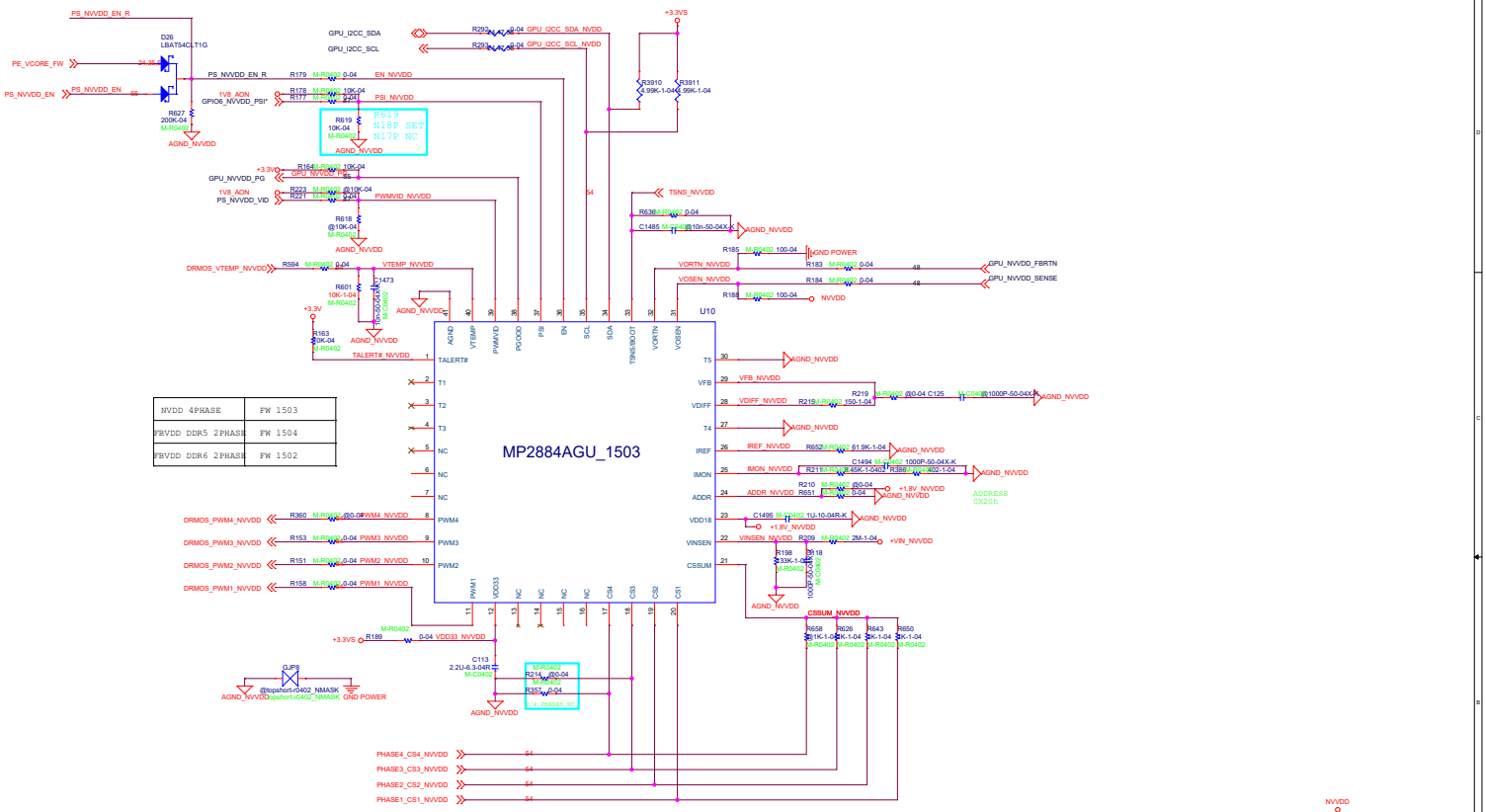

Maximum VRAM case Temp is 85 celcisus degree
VRAM3A
NORMAL
VRAM3B
NORMAL
COMMON
FBGA180
VRAM3C
VRAM3D
FBVDDQ_MEM
1V8_AON
BOTTOM SIDE DECOUPLING UNDER VRAM .47U 0402 X 8
同方国际信息技术有限公司
N18P-G62 VRAM3_FrameBuffer B
GK5MPFX
Sunday, December 01, 2019
51
61
1.0

Maximum VRAM case Temp is 85 celcisus degree



同方国际信息技术有限公司

Title	N18P-G62 VRAM4_FrameBuffer B	
Size: Custom	Document Number: GK5MPFX	Rev: 1.0
Date: Sunday, December 01, 2019	Sheet 52 of 61	



NVDD 4PHASE	FW 1503
FBVDD DDR5 2PHASE	FW 1504
FBVDD DDR6 2PHASE	FW 1502

Title	N18P-G62 NVVDD
Size	C
Document Number	GK5MPFX
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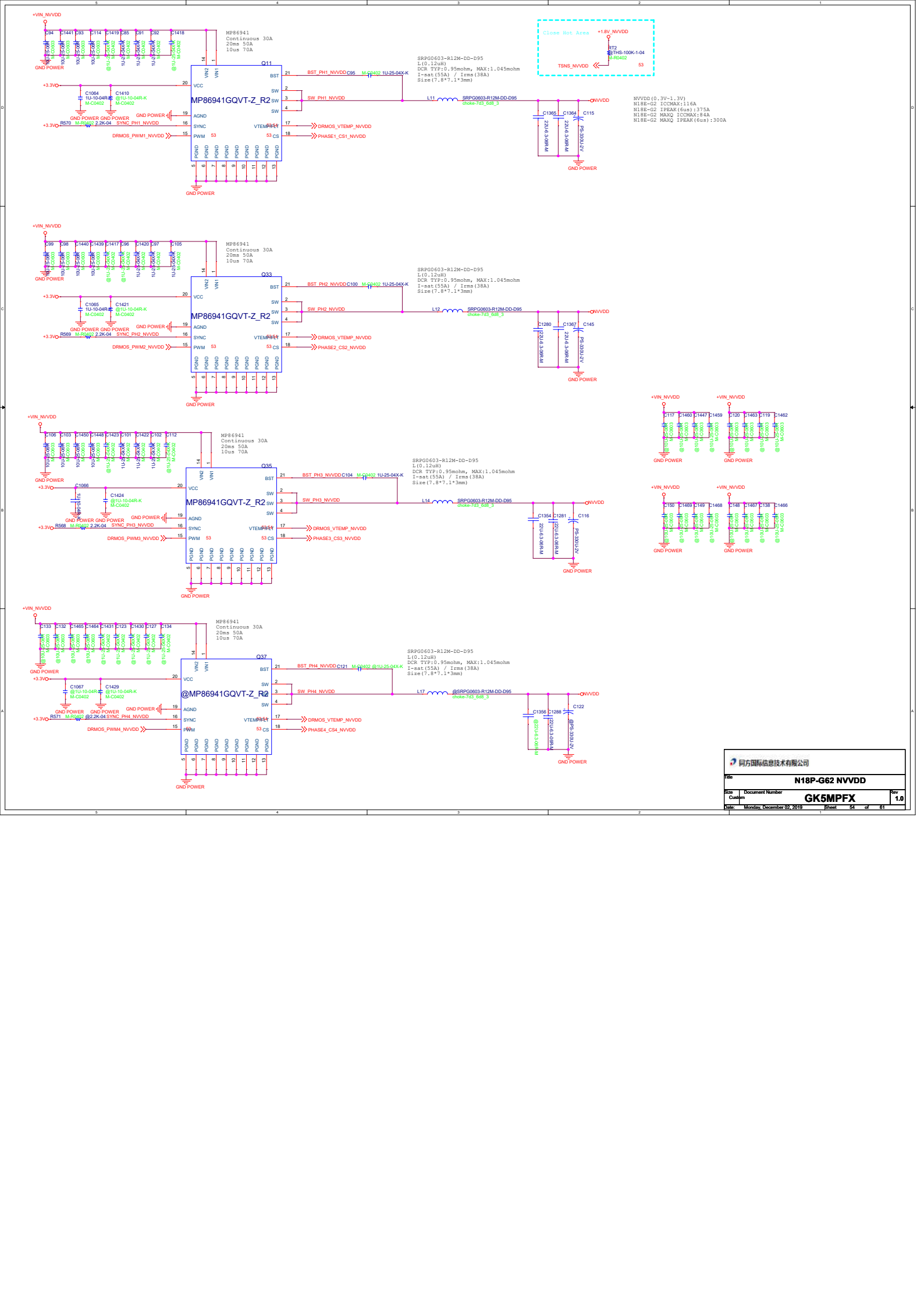
Close Hot Area
+1.8V_NVVDD
RT2
THS-100K-1-04
M-R0402
TSNS_NVVDD
53
+VIN_NVVDD
MP86941
Continuous 30A
20ms 50A
10us 70A
Q11
MP86941GQVT-Z_R2
VIN2
VIN1
VCC
AGND
SYNC
PWM
VTEMP
CS
BST
SW
PGND
BST_PH1_NVVDD
SW_PH1_NVVDD
SYNC_PH1_NVVDD
DRMOS_PWM1_NVVDD
DRMOS_VTEMP_NVVDD
PHASE1_CS1_NVVDD
SRPG0603-R12M-DD-D95
L(0.12uH)
DCR TYP:0.95mohm, MAX:1.045mohm
I-sat(55A) / Irms(38A)
Size(7.8*7.1*3mm)
L11
NVVDD
NVVDD(0.3V~1.3V)
N18E-G2 ICCMAX:116A
N18E-G2 IPEAK(6us):375A
N18E-G2 MAXQ ICCMAX:84A
N18E-G2 MAXQ IPEAK(6us):300A
Q33
BST_PH2_NVVDD
SW_PH2_NVVDD
SYNC_PH2_NVVDD
DRMOS_PWM2_NVVDD
PHASE2_CS2_NVVDD
L12
Q35
BST_PH3_NVVDD
SW_PH3_NVVDD
SYNC_PH3_NVVDD
DRMOS_PWM3_NVVDD
PHASE3_CS3_NVVDD
L14
Q37
@MP86941GQVT-Z_R2
BST_PH4_NVVDD
SW_PH4_NVVDD
SYNC_PH4_NVVDD
DRMOS_PWM4_NVVDD
PHASE4_CS4_NVVDD
L17
GND POWER
同方国际信息技术有限公司
N18P-G62 NVVDD
GK5MPFX
Rev 1.0
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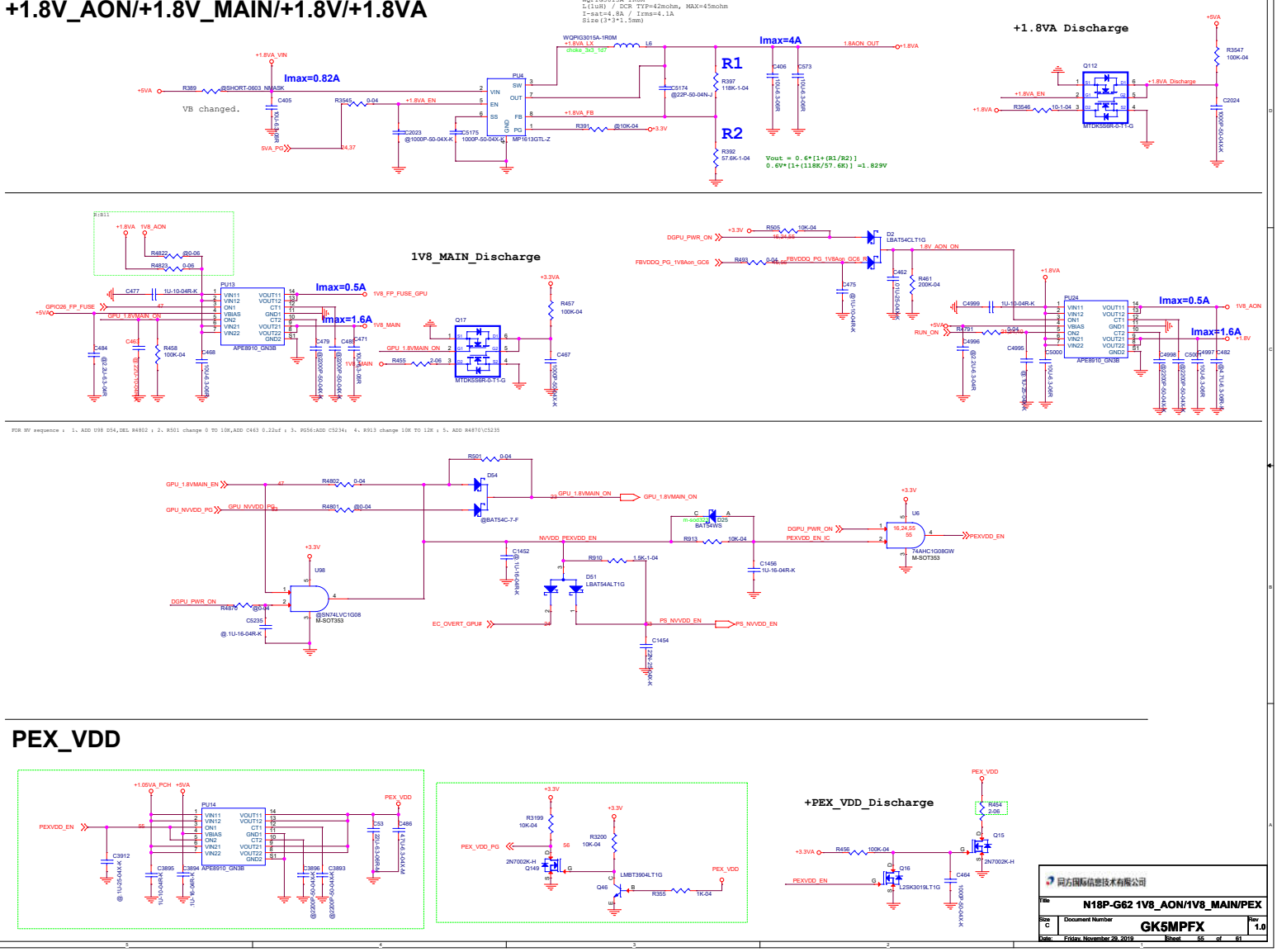
Sheet 54 of 61

+1.8V_AON/+1.8V_MAIN/+1.8V/+1.8VA

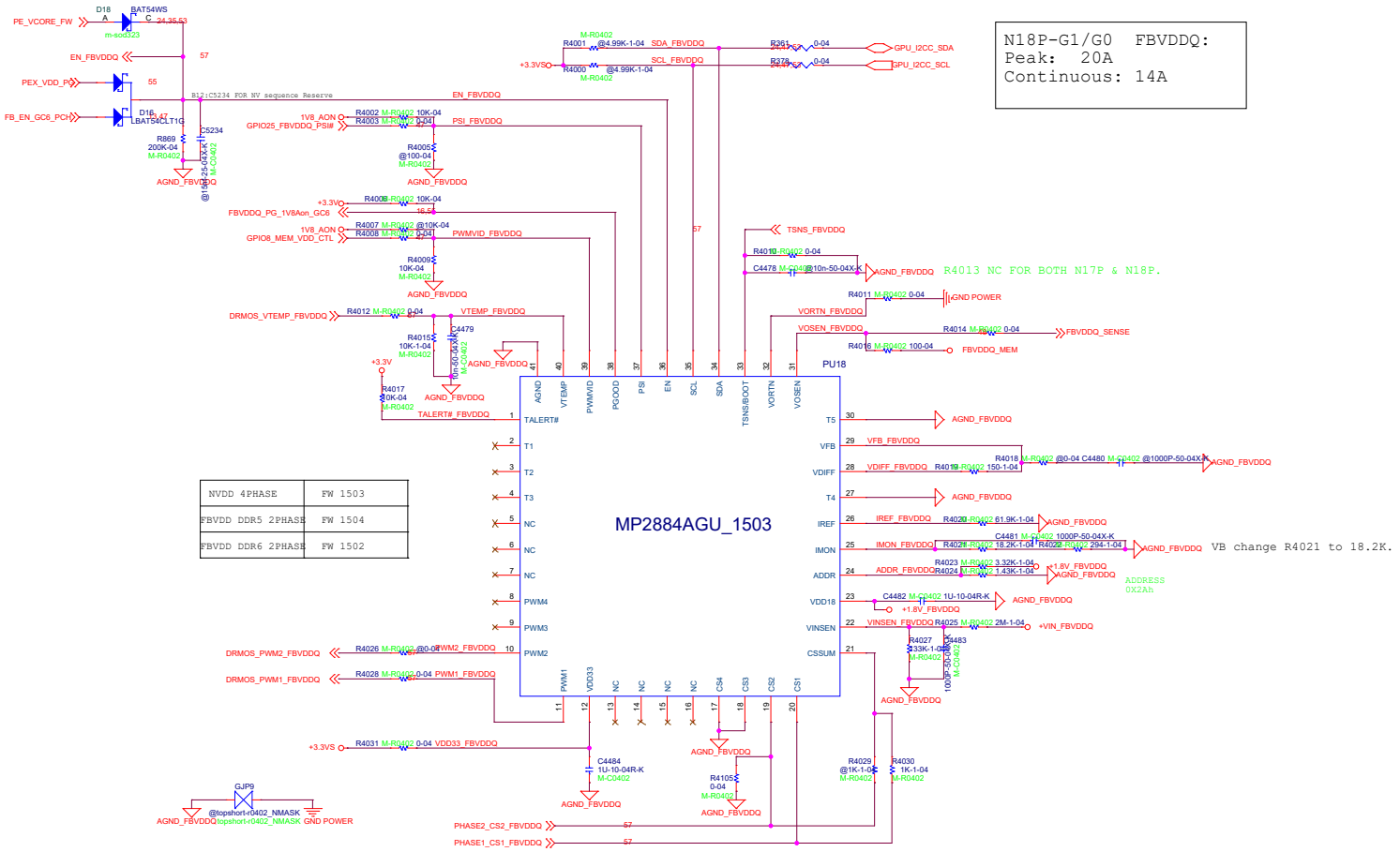


PEX_VDD

同方国际信息技术有限公司		
Title	N18P-G62 1V8_AON/1V8_MAIN/PEX	
Size C	Document Number GK5MPFX	Rev 1.0
Date: Friday, November 29, 2019	Sheet 55 of 61	

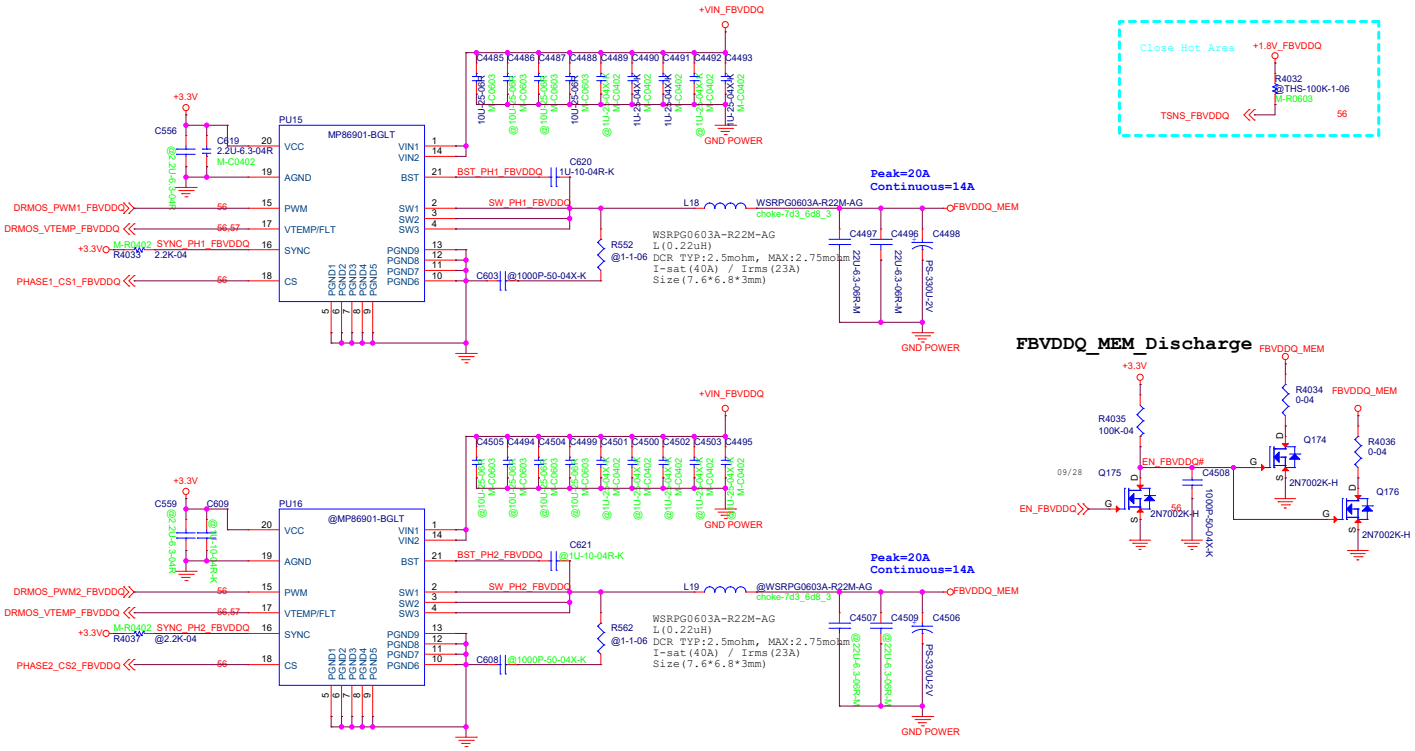
GP

FBVDDQ_MEM

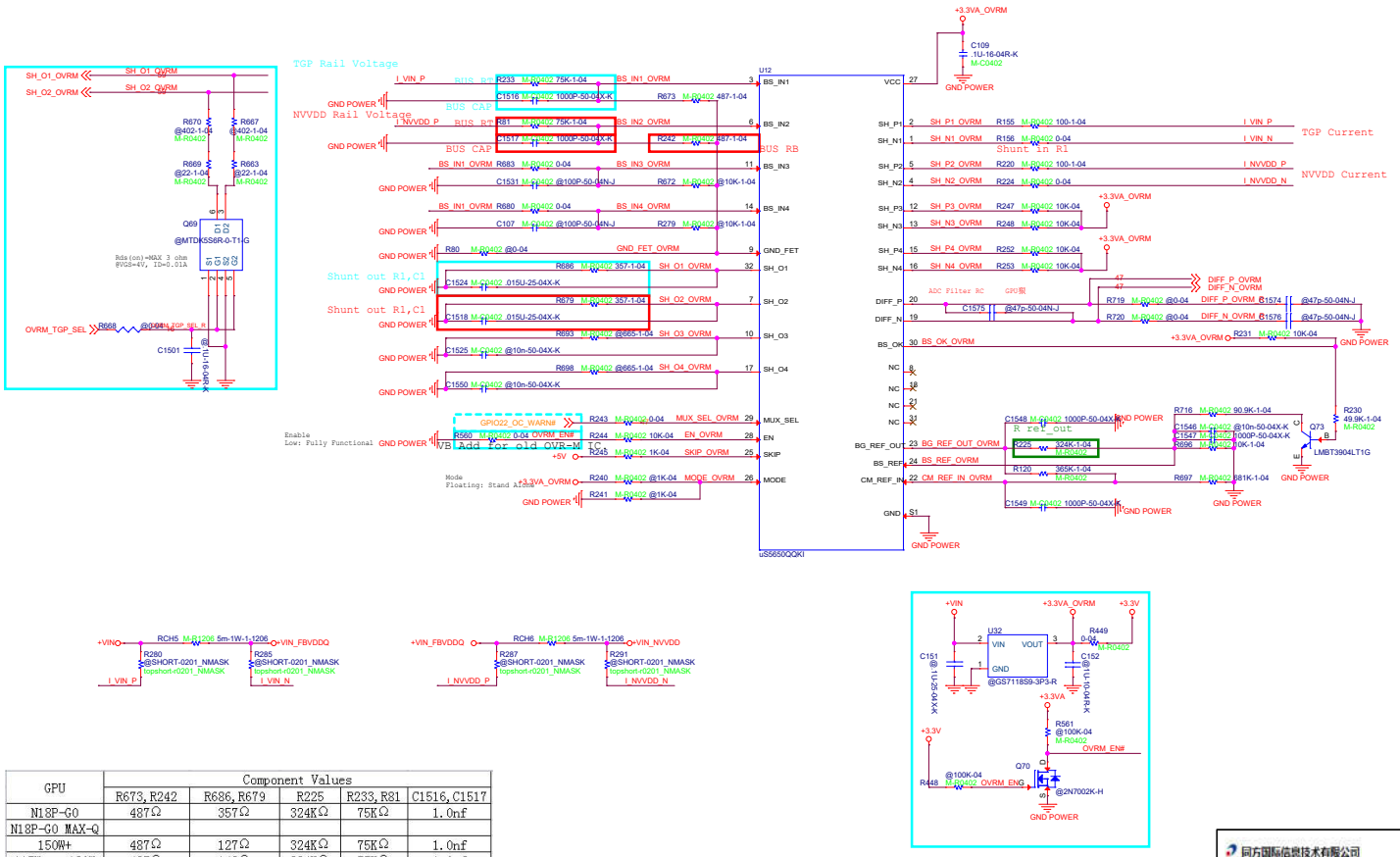


同方国际信息技术有限公司

Title	N18P-G62 FBVDDQ_MEM	
Size: Custom	Document Number: GK5MPFX	Rev: 1.0
Date: Friday, November 29, 2019	Sheet 56 of 61	



Title	N18P-G62 FBVDDQ_MEM		
Size B	Document Number GK5MPFX		Rev 1.0
Date: Monday, December 02, 2019	Sheet 57 of 61		



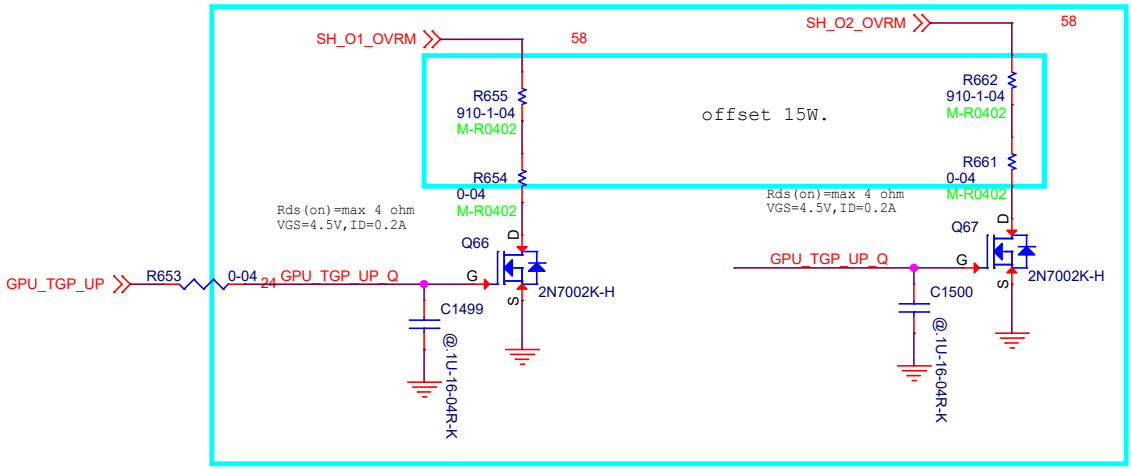
GPU	Component Values				
	R673, R242	R686, R679	R225	R233, R81	C1516, C1517
N18P-G0	487Ω	357Ω	324KΩ	75KΩ	1.0nf
N18P-G0 MAX-Q					
150W+	487Ω	127Ω	324KΩ	75KΩ	1.0nf
115W to 130W	487Ω	143Ω	324KΩ	75KΩ	1.0nf
100W to 110W	487Ω	165Ω	324KΩ	75KΩ	1.0nf
75W to 90W	487Ω	215Ω	324KΩ	75KΩ	1.0nf
70W or lower	487Ω	357Ω	324KΩ	75KΩ	1.0nf

同方国际信息技术有限公司

Title: N18P-G62 OVRM

Size: Custom | Document Number: GK5MPFX | Rev: 1.0

Date: Friday, November 29, 2019 | Sheet 58 of 61



TGP Control / TGP Watt	GPU_TGP_UP	OVRM_TGP_SEL
OVER 130W	HIGH	HIGH
100W TO 110W	HIGH	LOW
115W TO 130W (7S)	LOW	HIGH
75W TO 90W (7Z)	LOW	LOW

同方国际信息技术有限公司

Title	N18P-G62 TGP	
Size: A	Document Number: GK5MPFX	Rev: 1.0
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GK5CN5Z_A->A1 change list:
1.Erplot6 power off over 0.5W issue(close VCORE program mode)
POP R352 10K-04
R303 10K-04->0-04
EC GPC4(PIN120) connect to R303
2.Correcting PCH_PWROK,SYS_PWROK & PM_RSMRST# series resistors
R249,R282 and R232 connect to EC
POP R108 100K-04
R126 1.05VA_PCH_PG->5VA_PG
3.CNEDP1 PIN19 change to +3.3V_LCD for 4K PANEL
CNEDP1.19 from GND change to +3.3V_LCD
4.MP2949AGQKT VIN_SEN 1/16 divider network
R336 2M-1-04,R332 133K-1-04
5.PEX_VDD LDO -> Low swith for NV sequencing
PU14 APL5934BKAI-TRG(LDO)->APL3523QBI-TRG(low switch)
R454 10-06 ->2-06
6.FBVDDQ_MEM discharge circuit modify to dual path
Add Q139 2N7002K-H
7.PCH PCIE change
PCIE6(NA) -> PCIE15 WLAN
PCIE5(GbE)-> PCIE14 LAN
8.typec usb2.0 (usb 5) reverse modify
USB_PP5,USB_PN5 swap
9.ME KB ID PIN pull high resitor 1%
R283 10K-04->10K-1-04
Add C184
10.+VPHY_1P24
POP C41 10U-6.3-06R
11.+VCCPHVLDO_1P8
R25 +1.8VA->+VCCPRIM_1P8
12.GPU SMBUS to EC SMBUS reverse modify
PCH_SML1CLK & PCH_SML1DAT SWAP
13.FAN CONN change 3PIN to 4PIN
Remove U14 & U16 APL5607AKI-TRG
CNFAN1 & CNFAN2 WB,3P,SMT,P1.25,3800K-F03N-03LENT->CON_WB_4H125_3800K-F04N_ENT
14.NVVDD discharge circuit modify
MTDK5S6R-0-T1-G change to 2N7002K-H
15.EDP power sequencing
Q101 remove
add Q49 2N7002K-H,Q113 MTDK5S6R-0-T1-G change to 2N7002K-H
R373 82K-1-04->220K-1-04
C452 .47U-25-04R-K->1U-10-04R-K
16.Detect ID thickness
CNAUDIO1.22 add net THICKNESS_ID_DET
EC U5.82(GPE1) add net THICKNESS_ID_DET
17.EC detect ME KB US or UK sequecing
EC U5.104(GPG6) add net SUS_ON
ADD D17
PU5.15, PU6.3, PU7.3 and PU19.3 PM_SLP_S4#->SUS_ON_S4#
18.DCIN SAFTY_PROTECT combine to TI charger ic
Delete Q41, Q43, Q120 and other component
19.HDMI & DP hot plug add pull low resistor
change R133 100K-04 to pull low
20.+VCORE off sequencing modify
Add D24 BAT54WS
21.PEX_CLKREQ# level shift mos change
Q78 2N7002K-H->L2SK3019LT1G
22.1V8_MAIN sequencing
UNPOP C479
R455 10-06 -> 2-06
23.+5VA choke 3mm->2mm for ME
L15 WSRPG0603-2R2M-H->EM-15AM28V01
24.VCCST_PG sequencing tuning
remove U1
Q6.2 net name change to EN_VCORE
25.CNVI follow check list
R227 R228 22-1-04 -> 0-04
R612 R614 33-1-04 -> 0-04
Reserve C33
26.Mini DP & HDMI Hot plug
Remove Q28, Q33, Q35
R674 51K-1-04, R637 0-04, R639 0-04
27.Crystal tuning
C5, C6 22P-50-04N-J -> 15P-50-04N-J
C1405, C1409 18P-50-04N-J -> 33P-50-04N-J
28.PJP change to Short plane
Remove PJP2, PJP5, PJP7, PJP8, PJP10, PJP11
29.ME KB ADD ESD
Remove R139, R153,R120
Add D60~D73
30.HDMI SI tuning
Q86 L2SK3019LT1G->LMBT3904LT1G
R430 4.7K-04->100-04
31.AC VIN input add H:4mm CAP
Add C674, C597, C598 EEHSH1E330L
32.ME request NC->BAT CONN
33.DCIN CO change
34.SPK PIN SWAP WO_2DC3003-002211_SIN->CON_DCIN_WO_2DC3003-016211F_SIN
35.+5VA voltage target change to 5.142V for loss
R448 23.2K-1-04, R450 4.3K-1-04
36.SPK bead placement change for EMI request
Del R125, R252, R285, R287
37.Battery only leakage current improving
R442 220K-1-04 -> 2M-04, R451 100K-1-04 -> 1M-04
R438,R437,R218,R203,R199,R217,R297, R359 470K-04->1M-04
R194 93.1K-0.1-04->196K-1-04
R187 13.3K-0.1-0402->28K-1-04
38.RTC battery tuning
UNPOP R382
39.EMI request
UNPOP L23 , L29 , L35 , L36
POP R312, R453, R329, R327, R462, R469, R468, R465
AB11, AB12, AB8, AB9 BD-FCM1608KF-600T07->FCM1608KF-121T06
POP C1005, C1006, C988, C951, C921, C924, C1000 33P-50-04N-J

GK5CN5Z_A1->A2 change list:
1.+5V_AMP modify
Remove AB10
2.AB8, AB9, AB11, AB12 FCM1608KF-121T06 -> BD-HCB1608KF-120
3.CNSSD1 support NVMe
PCIE 17-20 -> PCIE 21-24

GK5CN5Z_A2->A3 change list:
1.CNKB1 +5VS modify
Add PU17 to seperate KB power control by EC
2.Q8 soft start modify
C3556 .1U-25-04X-K ->47n-16-04X-K
UNPOP C3582
3.+VCORE & NVVDD +VIN INPUT CAP modify for fast transient
C329,C326,... 1U-25-06R-K->10U-25-06R
C1372,C1370,... 1U-25-06R-K->10U-25-06R

GK5CN5Z_A3->B change list:
1.Q8 soft start modify
Reserving R460 for discharge
C3582 10n-50-04X-K
2.Jumper modify
GJP1,GJP2,GJP3,GJP4,GJP6,GJP7 -> TOPSHORT_20X30 ->topshort-r0402_NMASK
GJP5 topshort-r0402->topshort-r0402_NMASK
Remove PJP1,PJP6,PJP5,PJP12
3.Remove All MEKB ESD
Remove D60 - D73
4.Short +5VS to +5V_MEKB
Add R120
UNPOP PU17...
5.MEKB new PIN definition
GPA7 net name change to MEKB_PWM_LED_BDID
GPJ2 net name change to A_COVER_LED
GPI2 net name change to MEKB_INT#
6.+5VA noise reduce
R449 360K-1-04->270K-1-04
Add R474
7.NVVDD MLCC TOP & BOT reducing noise
Remove C2821
8.+5VA increase voltage for USB Droop
R448 23.2K-1-04->23.7K-1-04
9.TYPEC CC PIN power change
R632, R793 +5V->+5V_TYPEC
10.All USB port power from +5VS to +5VA
CNUSB1.5 +5VS_CR_CN
R146,U27.2,U27.3,R142 +5VS->+5VA
11.DFM check list request
POP C669 1U-10-04R-K
12.reserve internal 1.8V VRM solution
Delete R26
R610,R616,R611 +1.8VA->+VCCPRIM_1P8
13.BAT_SMB driving improving
R144,R145 4.7K-04->1K-04
14.MP2949AGQKT reserve 3.3V option
Add R356
15.R3314,R3315 100-1-04-> 10-1-04
16.CNVI CLKIN_XTAL CAP filter
C33,10P-50-04N-J

GK5CN5Z_B->V1.0 change list:
1.QKEY reserve
POP R205,R206 0-04
Add R624,R625

GK5CN5Z_V1.0->V1.1 change list:
1.CLKOUT_LPC0 noise reducing
Add C474 22P-50-04N-J
2.BAT SMBUS compatible tuning
R144 & R145 1K-04 -> 2.2K-1-04
3.+1.05VA_PCH inrease voltage
R399 3.0TK-1-04
R394 9.76K-1-04
4.Support Subwoofer
POP R161 0-04

GK5CN5Z_V1.1->V1.2 change list:
1.+3.3V add twice Low switch
Add PU23, C599, C481
2.CHG_REF CAP value change
C353,C355 1U-10-04R-K->2.2U-6.3-04R
3.BAT_I ZERO-I accuracy modify
Add R347 100K-1-04
UNPOP R326
4.Support 3.6V 144HZ PANEL
Add U18 LDO IC & related component
discharge circuit Q49 & Q113 modify
5.Remove SPI FP, Add USB FP
Remove PCH_GSPI1_CLK...
Add USB_PP10 & USB_PN10

GK5CN5Z_V1.1->V1.2 BOM change list:
1.DCIN MOS
Q8,Q9 MTB06N03H8 -> MTB2D5N03BH8-0-T6-G
2.+3.3V Dual LOW SWITCH
POP PU23 APE8910_GN3B
3.+3.3VA Voltage increase to 3.4586V
R443 56.2K-1-04 ->44.2K-1-04
R452 18K-1-04 -> 13.3K-1-04
4.ME_KB_ID pull high modify
R283 10K-1-04 ->11.8K-1-04
5.WEBCAM USB 0 ohm -> common choke
UNPOP R528,R542 0-04
POP L16 QTCW2012EH4-120-LF
C669 1U-10-04R-K->33P-50-04N-J
6.IR CAMERA POWER CAP
C555 POP 33P-50-04N-J

Title	HISTORY	
Size C	Document Number GK5MPFX	Rev 1.0
Date: Friday, November 29, 2019	Sheet 60 of 61	

Revision History

VA TO VB Date: 2019/11/25

PCB Version: B PCB P/N XXXX

No.	Modify Item	Modify Details	Schematic/Layout/BOM Change	Page
1	B1-ADD INTEL DEBUG PROC Circuit		Schematic&Layout	7
2	B2-B3 DEL DDS; Recover old GK5CP5X EDP CONNECT ; @R373, ADD R4800	@R373, ADD R4800	Schematic&BOM	12
3	B-3 Changed PWR_USB# to DGPU_PWR_ON	Layout	Schematic	24
4	B-4 Moved PWR_USB# to EC GPG2	Layout	Schematic	24
5	B-5 Changed DGPU_PWR_ON to DB_THERMISTOR DB_THERMISTOR PULL-UP	Layout &ADD R4871	Schematic&BOM	24
6	B-6 Changed PWR_USB# pull up to MIRROR_FUNCION	Layout &del R623	Schematic&BOM	24
7				24
8	B-7Changed GPH5 HYB_ON TO CHG_G_LED	Layout	Schematic	24
9	B-8 PM_CLKRUN# ADD R4864	@R4864	Schematic	24
10	B-9 +5VS_KB ADD R4867 COLAY +5VS	@R4867	Schematic	24
11	B-10 CNAUDIO1 PIN 24 Changed GND TO thermal sensor signal	Add R4872	Schematic&BOM	32
12				35
13				

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