GA-970A-D3

Revision : 1.2

GIGABYTE™

Title: COVER SHEET		
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 1 of 36	

Model Name:GA-970A-D3

Component value change history

Version: 1.2

P-Code: U98094-0

Date	Change Item		Reason
2011.03.10	0.1 9M970AD3-00-01		
2011.03.11	0.1 9M970AD3-00-01A		
2011.04.18	9M970AD3-00-02	PCB Ver 0.2	
2011.04.22	9M970AD3-00-02A	PCB Ver 0.2	
2011.05.09	9M970AD3-00-10A	PCB Ver 1.0	
2011.05.10	9M970AD3-00-10B	PCB Ver 1.01	
2011.05.18	9M970AD3-00-10C	PCB Ver 1.01	
2011.06.07	9M970AD3-00-10D	PCB Ver 1.01	
2011.06.27	9M970AD3-00-10E	PCB Ver 1.02	
2011.07.18	9M970AD3-00-11A	PCB Ver 1.1	
2011.08.17	9M970AD3-00-11B	PCB Ver 1.1	
2012.01.11	9M970AD3-00-11C	PCB Ver 1.1	
2012.01.30	9M970AD3-00-11D	PCB Ver 1.1	
2012.03.13	9M970AD3-00-12A	PCB Ver 1.2	

Circuit or PCB layout change for next version

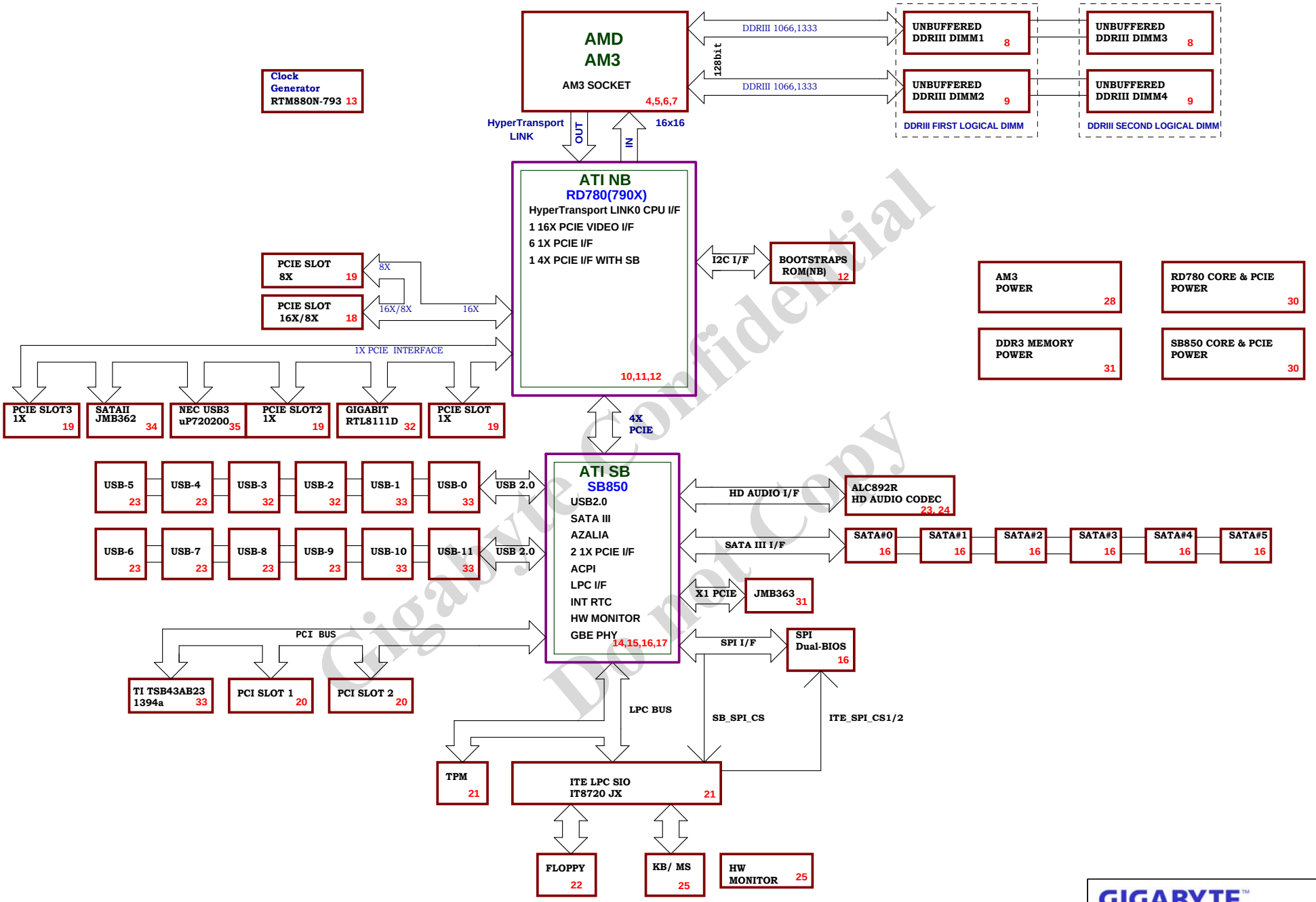
Date	Change Item	Reason
	0.1	
2011.02.22	Modify from GA-990XA-UD3	
	移除 PCIEx8, 1394, Front USB3	
	增加PCIEx1_3	
	Vcore change 4+1 power pake 6329+6609	
2011.04.18	修改CPU Vcore OCP與RC 電阻值	0.2
	修改超電壓由每格10mV改爲5mV	
2011.04.22	修改VCORE電容820uF->560uF	0.2
2011.05.09	AMD comment for validation.Erp funtion	1.0A
2011.05.10	cheang ddr dimm文字面順序1.2.3.4->4.2.3.1	1.0B
2011.05.18	修改on-off charge值	1.0C
2011.06.07	修改DDR PWR Level ripple過大issue	1.0D
2011.06.27	增加R1 R5 連接 differential clock 從 CLK GEN 到北橋.	1.0E
	MB ID SUPERI/OGP40 L不超壓H超壓	
2011.07.18	增加loadline disable function	11A
	MB ID SUPERI/OGP10	
	GP27:Disable loadline GP32:loadline 75% GP31:loadline 50%	
2011.08.17	只開放loadline Enable與Disable Function	11B
2012.01.11	LAN chip 8111E change 8111F	
2012.01.30	4+7 MOS change 6+9	11D
2012.03.13	codec 889 change 887 Remove 108db	12A

GIGABYTE™

Title: BOM & PCB HISTORY

Size: Custom | Document Number: GA-970A-D3 | Rev: 1.2

Date: Friday, March 16, 2012 | Sheet 2 of 36



GIGABYTE™

Title: BLOCK DIAGRAM

Size	Document Number	Rev
Custom	GA-970A-D3	1.2

Date: Friday, March 16, 2012 Sheet 3 of 36

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

L0_CADIN_L[0..15] → L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15] → L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15] → L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15] → L0_CADOUT_H[0..15] 10

M2CPUA
HYPERTRANSPORT

10 L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 10
10 L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 10
10 L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 10
10 L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 10
10 L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 10
10 L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 10
10 L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 10
10 L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 10
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE5	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AE4	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AH6	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AG6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AH5	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH4	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)		L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AE1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AG2	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG3	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AH1	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AG1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)		L0_CADOUT_L0	

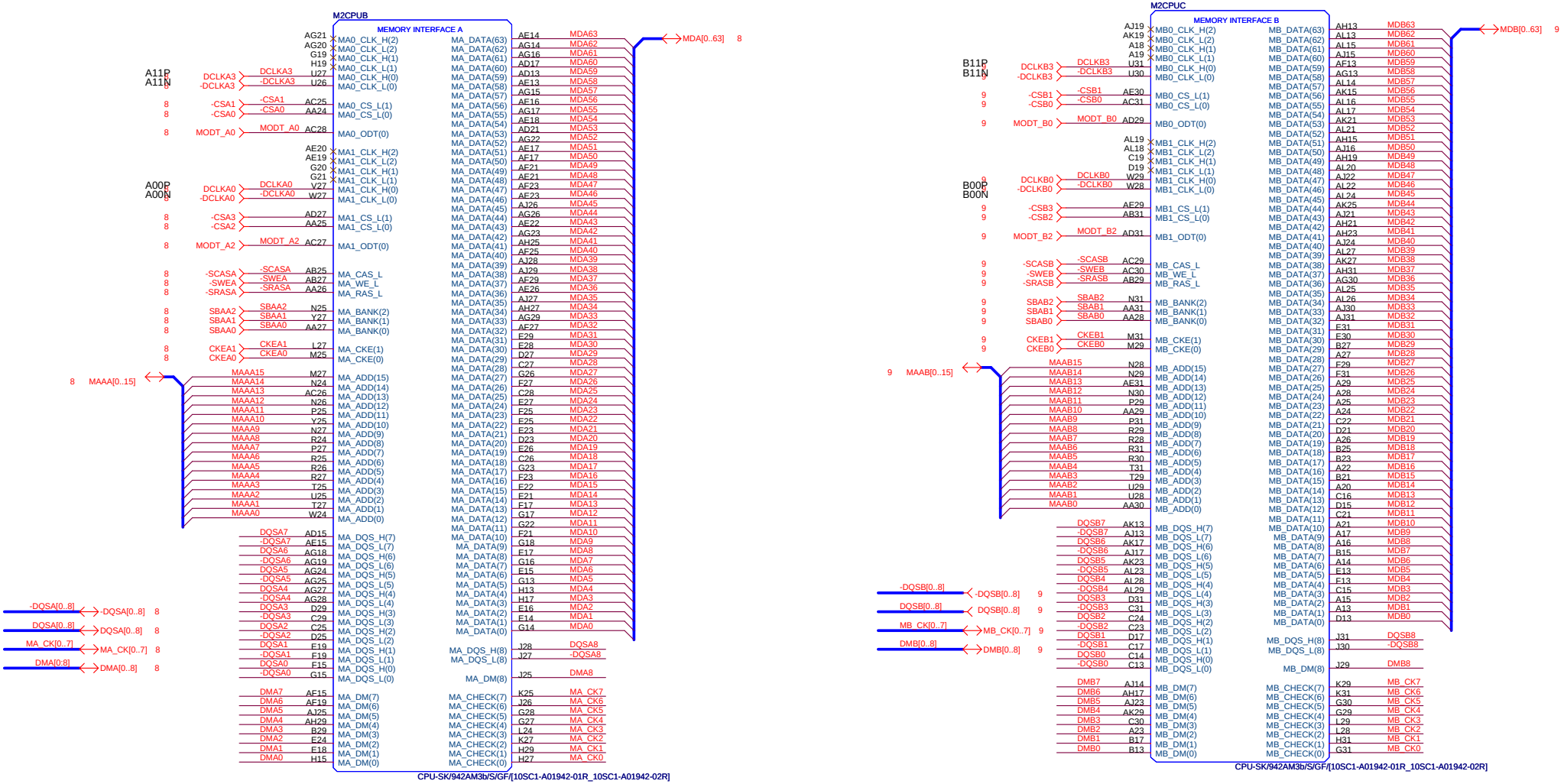
CPU-SK/942AM3b/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

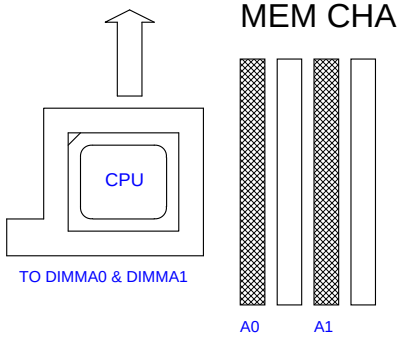
COUPON1 — COUPON1 1 — 2 COUPON/X — VCC
COUPON2 — COUPON2 1 — 2 COUPON/X

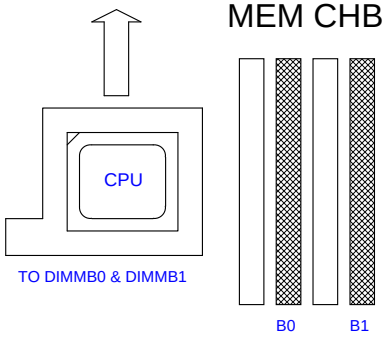
M2CPU
AM3RM/SC/BL/MB/[12KRC-04K812-31R_12KRC-04K812-32R]

GIGABYTE™

Title: CPU HYPER TRANSPORT			
Size: Custom	Document Number: GA-970A-D3		Rev: 1.2
Date: Friday, March 16, 2012	Sheet 4 of 36		

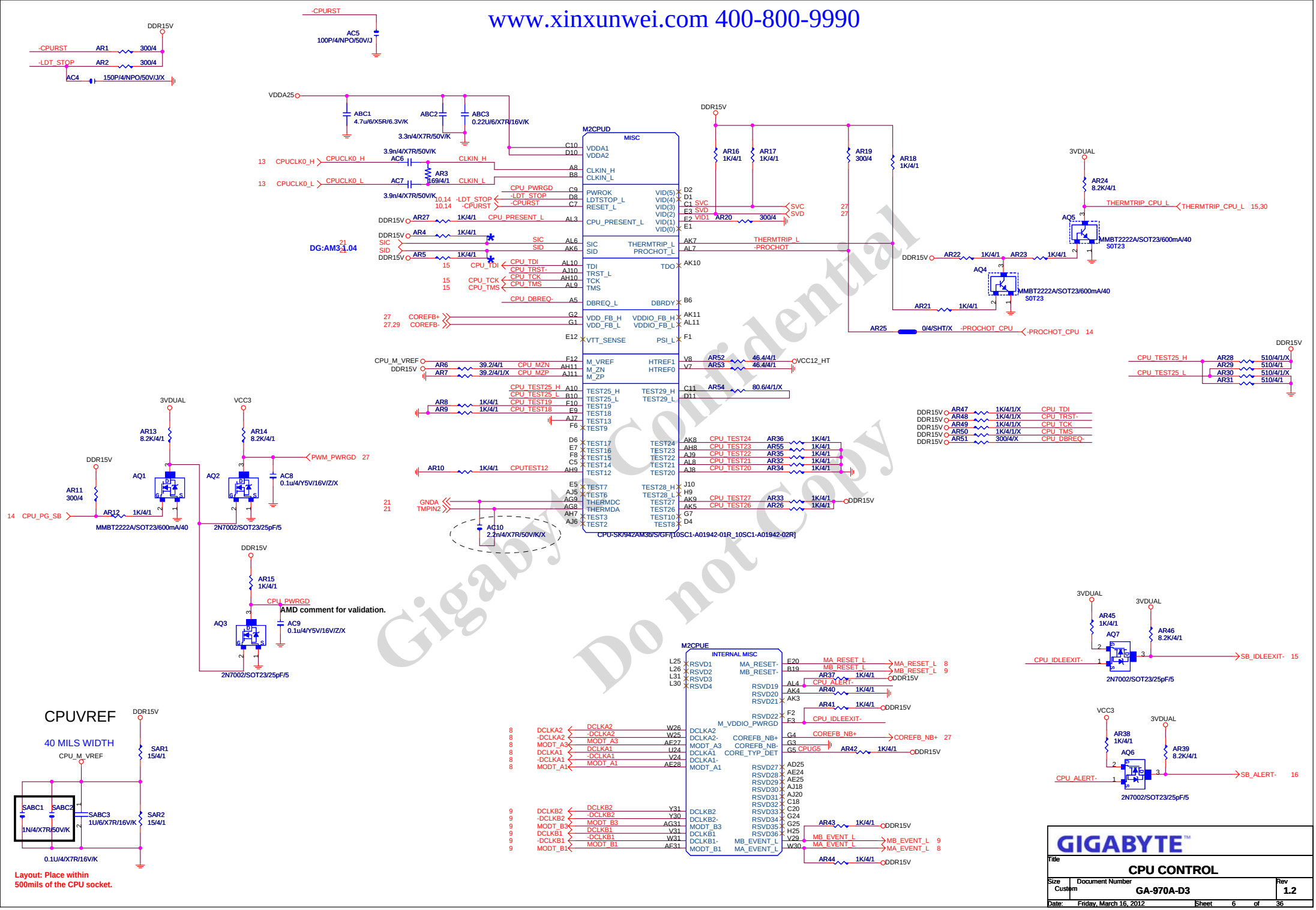






GIGABYTE™

Title	CPU DDRIII MEMORY	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 5 of 36	



GIGABYTE™

Title: CPU CONTROL

Size	Document Number	Rev
Custom	GA-970A-D3	1.2

Date: Friday, March 16, 2012 Sheet 6 of 36

VLDT_RUN is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

M2CPUF
VDD1

M2CPUG
VDD2

M2CPUH
VDD3

M2CPUI
VDDIO

AE9 Missing pins on package and socket used for mechanical keying. =>AM3

H22 Missing pins on package and socket used for mechanical keying. =>AM3

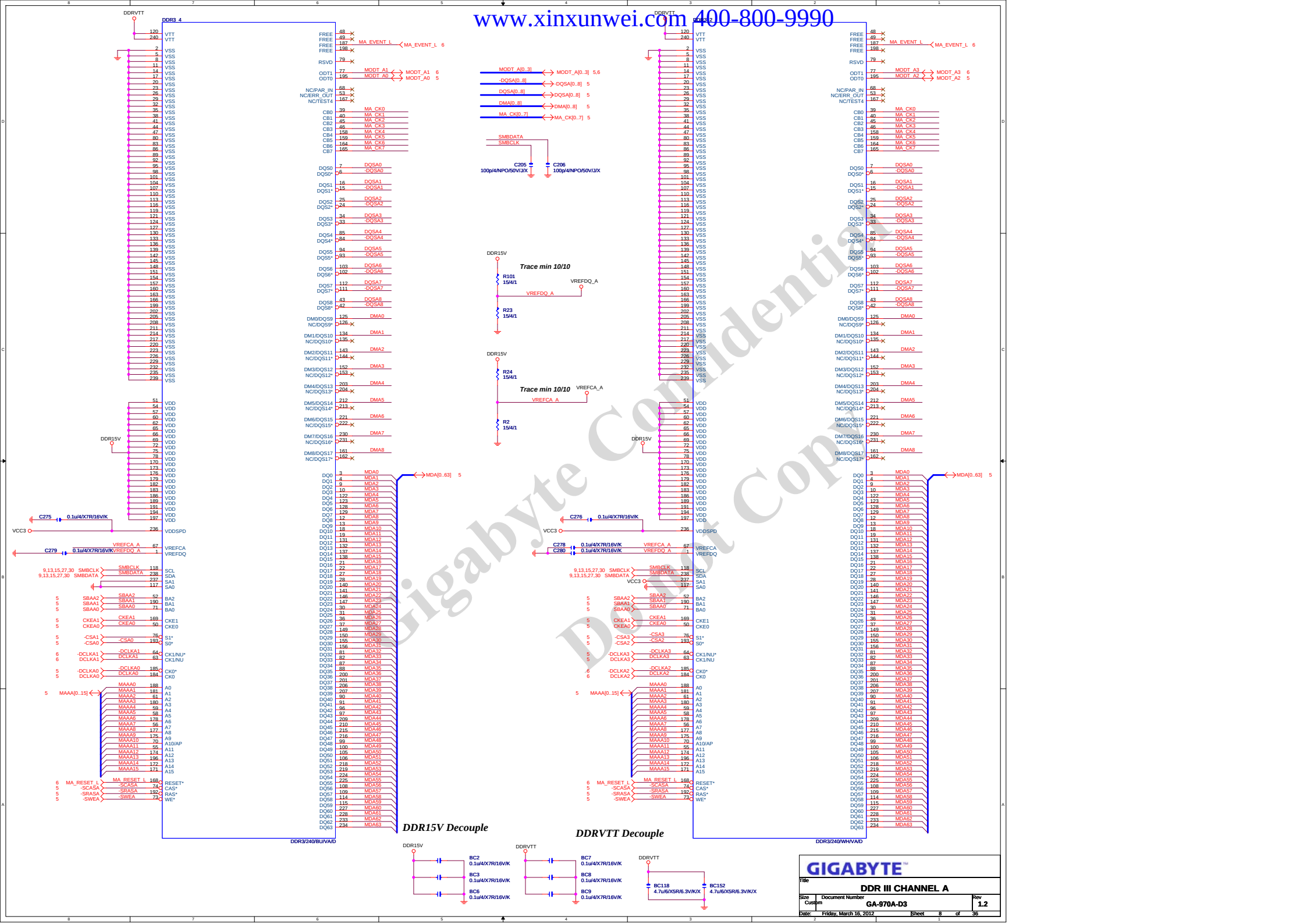
AM3 Only

BUTTOM SIDE

AMD Validation

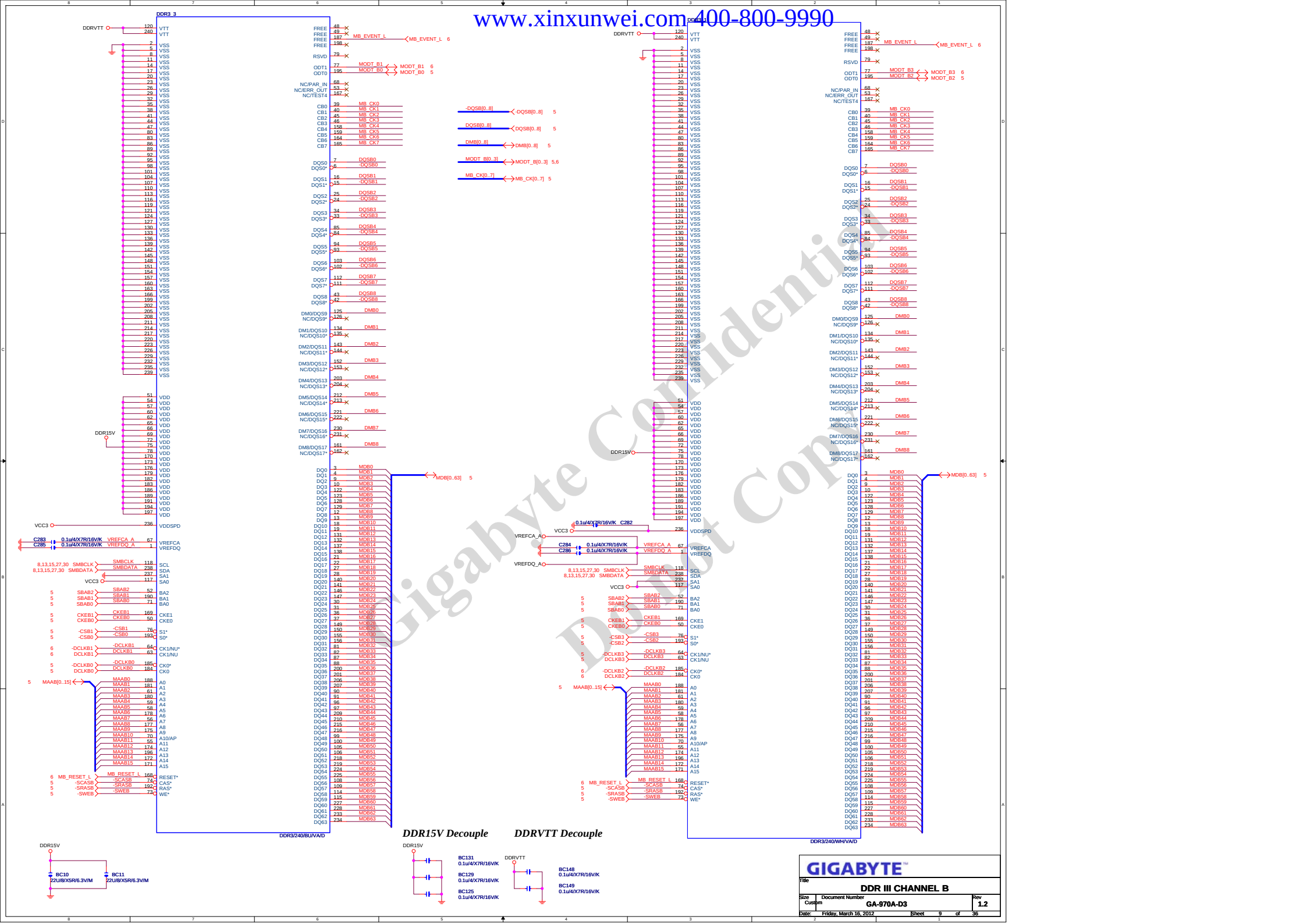
1021 EMI

GIGABYTE		
Title: CPU POWER & GND		
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 7 of 36	



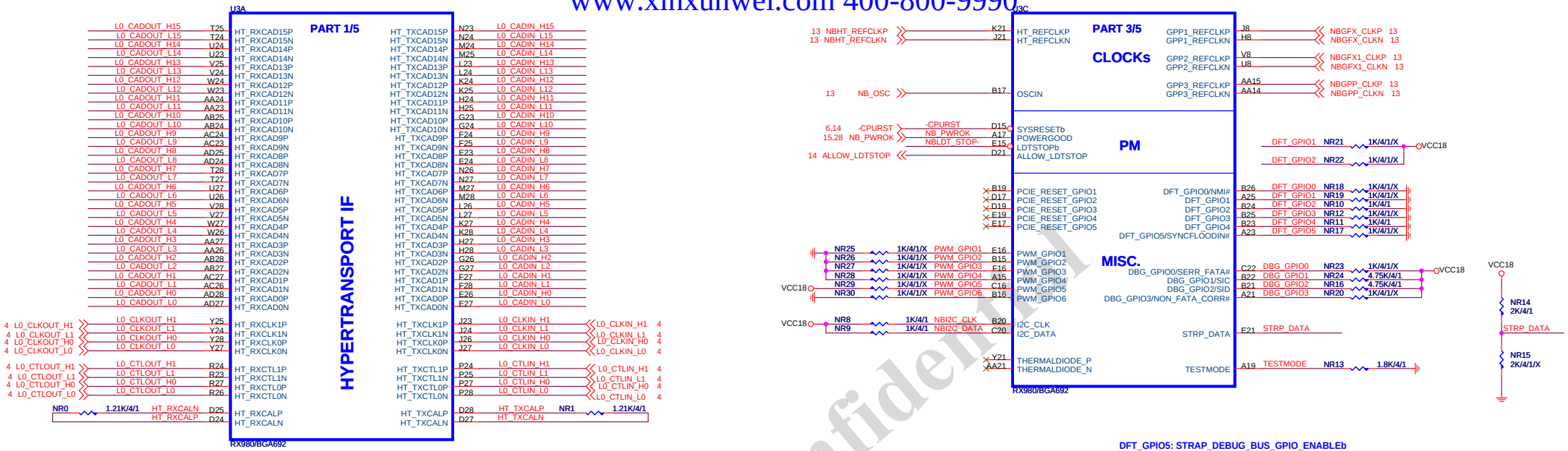
GIGABYTE

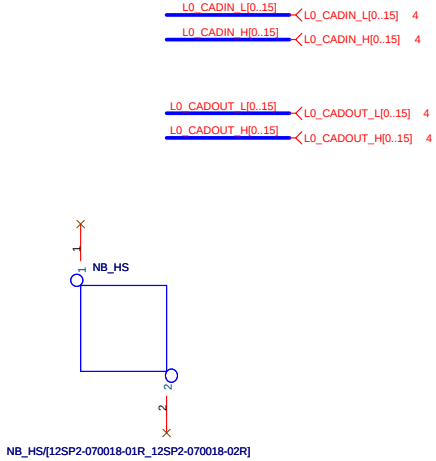
Title	DDR III CHANNEL A		
Size: Custom	Document Number: GA-970A-D3		Rev: 1.2
Date: Friday, March 16, 2012	Sheet 8 of 36		

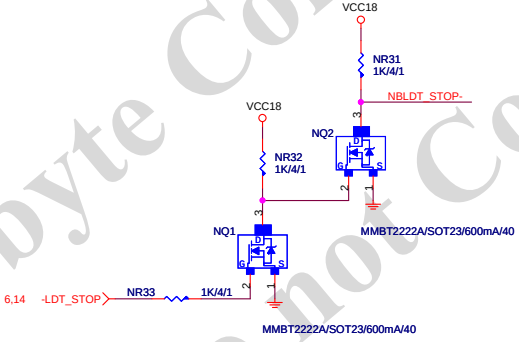


GIGABYTE

Title	DDR III CHANNEL B		
Size: Custom	Document Number: GA-970A-D3		Rev: 1.2
Date: Friday, March 16, 2012	Sheet 9 of 36		







DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101: 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

GIGABYTE™

Title	RS780 HT-LINK I/F	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 10 of 36	

U3B

PART 2/5

PCIE GPP1

EXP_A_RXP15	N6	GPP1_RX15P	GPP1_TX15P	N3	EXP_A_TXP15
EXP_A_RXN15	N5	GPP1_RX15N	GPP1_TX15N	N2	EXP_A_TXN15
EXP_A_RXP14	M5	GPP1_RX14P	GPP1_TX14P	M2	EXP_A_TXP14
EXP_A_RXN14	M4	GPP1_RX14N	GPP1_TX14N	M1	EXP_A_TXN14
EXP_A_RXP13	L6	GPP1_RX13P	GPP1_TX13P	L3	EXP_A_TXP13
EXP_A_RXN13	L5	GPP1_RX13N	GPP1_TX13N	L2	EXP_A_TXN13
EXP_A_RXP12	K5	GPP1_RX12P	GPP1_TX12P	K2	EXP_A_TXP12
EXP_A_RXN12	K4	GPP1_RX12N	GPP1_TX12N	K1	EXP_A_TXN12
EXP_A_RXP11	J6	GPP1_RX11P	GPP1_TX11P	J3	EXP_A_TXP11
EXP_A_RXN11	J5	GPP1_RX11N	GPP1_TX11N	J2	EXP_A_TXN11
EXP_A_RXP10	H5	GPP1_RX10P	GPP1_TX10P	H2	EXP_A_TXP10
EXP_A_RXN10	H4	GPP1_RX10N	GPP1_TX10N	H1	EXP_A_TXN10
EXP_A_RXP9	G6	GPP1_RX9P	GPP1_TX9P	G3	EXP_A_TXP9
EXP_A_RXN9	G5	GPP1_RX9N	GPP1_TX9N	G2	EXP_A_TXN9
EXP_A_RXP8	F5	GPP1_RX8P	GPP1_TX8P	F2	EXP_A_TXP8
EXP_A_RXN8	F4	GPP1_RX8N	GPP1_TX8N	F1	EXP_A_TXN8
EXP_A_RXP7	D2	GPP1_RX7P	GPP1_TX7P	E3	EXP_A_TXP7
EXP_A_RXN7	D1	GPP1_RX7N	GPP1_TX7N	E2	EXP_A_TXN7
EXP_A_RXP6	B5	GPP1_RX6P	GPP1_TX6P	A4	EXP_A_TXP6
EXP_A_RXN6	C5	GPP1_RX6N	GPP1_TX6N	B4	EXP_A_TXN6
EXP_A_RXP5	D6	GPP1_RX5P	GPP1_TX5P	A6	EXP_A_TXP5
EXP_A_RXN5	E6	GPP1_RX5N	GPP1_TX5N	B6	EXP_A_TXN5
EXP_A_RXP4	E7	GPP1_RX4P	GPP1_TX4P	B7	EXP_A_TXP4
EXP_A_RXN4	F7	GPP1_RX4N	GPP1_TX4N	C7	EXP_A_TXN4
EXP_A_RXP3	D8	GPP1_RX3P	GPP1_TX3P	A8	EXP_A_TXP3
EXP_A_RXN3	E8	GPP1_RX3N	GPP1_TX3N	B8	EXP_A_TXN3
EXP_A_RXP2	E9	GPP1_RX2P	GPP1_TX2P	B9	EXP_A_TXP2
EXP_A_RXN2	F9	GPP1_RX2N	GPP1_TX2N	C9	EXP_A_TXN2
EXP_A_RXP1	D10	GPP1_RX1P	GPP1_TX1P	A10	EXP_A_TXP1
EXP_A_RXN1	E10	GPP1_RX1N	GPP1_TX1N	B10	EXP_A_TXN1
EXP_A_RXP0	E11	GPP1_RX0P	GPP1_TX0P	B11	EXP_A_TXP0
EXP_A_RXN0	F11	GPP1_RX0N	GPP1_TX0N	C11	EXP_A_TXN0

PCIE GPP2

AC9		GPP2_RX15P	GPP2_TX15P	AF9	
AD9		GPP2_RX15N	GPP2_TX15N	AG9	
AD8		GPP2_RX14P	GPP2_TX14P	AG8	
AE8		GPP2_RX14N	GPP2_TX14N	AH8	
AC7		GPP2_RX13P	GPP2_TX13P	AF7	
AD7		GPP2_RX13N	GPP2_TX13N	AG7	
AD6		GPP2_RX12P	GPP2_TX12P	AG6	
AE6		GPP2_RX12N	GPP2_TX12N	AH6	
AE5		GPP2_RX11P	GPP2_TX11P	AG4	
AG5		GPP2_RX11N	GPP2_TX11N	AH4	
AF2		GPP2_RX10P	GPP2_TX10P	AE3	
AF1		GPP2_RX10N	GPP2_TX10N	AE2	
AD2		GPP2_RX9P	GPP2_TX9P	AC3	
AD1		GPP2_RX9N	GPP2_TX9N	AC2	
AB5		GPP2_RX8P	GPP2_TX8P	AB2	
AB4		GPP2_RX8N	GPP2_TX8N	AB1	
AA6		GPP2_RX7P	GPP2_TX7P	AA3	
AA5		GPP2_RX7N	GPP2_TX7N	AA2	
Y5		GPP2_RX6P	GPP2_TX6P	Y2	
Y4		GPP2_RX6N	GPP2_TX6N	Y1	
W6		GPP2_RX5P	GPP2_TX5P	W3	
W5		GPP2_RX5N	GPP2_TX5N	W2	
V5		GPP2_RX4P	GPP2_TX4P	V2	
V4		GPP2_RX4N	GPP2_TX4N	V1	
U6		GPP2_RX3P	GPP2_TX3P	U3	
U5		GPP2_RX3N	GPP2_TX3N	U2	
T5		GPP2_RX2P	GPP2_TX2P	T2	
T4		GPP2_RX2N	GPP2_TX2N	T1	
R6		GPP2_RX1P	GPP2_TX1P	R3	
R5		GPP2_RX1N	GPP2_TX1N	R2	
P5		GPP2_RX0P	GPP2_TX0P	P2	
P4		GPP2_RX0N	GPP2_TX0N	P1	

PCIE GPP3

AD11		GPP3_RX9P	GPP3_TX9P	AH10	
AC11		GPP3_RX9N	GPP3_TX9N	AG10	
AE12		GPP3_RX8P	GPP3_TX8P	AG11	
AD12		GPP3_RX8N	GPP3_TX8N	AF11	
AD13		GPP3_RX7P	GPP3_TX7P	AH12	
AC13		GPP3_RX7N	GPP3_TX7N	AG12	
AE14		GPP3_RX6P	GPP3_TX6P	AG13	
AD14		GPP3_RX6N	GPP3_TX6N	AF13	
AD15		GPP3_RX5P	GPP3_TX5P	AH14	GPP_TX5P_C NC4 0.1u/4/X7R/16V/K PCIE5_OP 19
AC15		GPP3_RX5N	GPP3_TX5N	AG14	GPP_TX5N_C NC3 0.1u/4/X7R/16V/K PCIE5_ON 19
AE16		GPP3_RX4P	GPP3_TX4P	AG15	GPP_TX4P_C NC6 0.1u/4/X7R/16V/K ML_OP 33
AD16		GPP3_RX4N	GPP3_TX4N	AF15	GPP_TX4N_C NC5 0.1u/4/X7R/16V/K ML_ON 33
AD17		GPP3_RX3P	GPP3_TX3P	AH16	
AC17		GPP3_RX3N	GPP3_TX3N	AG16	
AE18		GPP3_RX2P	GPP3_TX2P	AG17	GPP_TX2P_C NC10 0.1u/4/X7R/16V/K PCIE2_OP 19
AD18		GPP3_RX2N	GPP3_TX2N	AF17	GPP_TX2N_C NC9 0.1u/4/X7R/16V/K PCIE2_ON 19
AD19		GPP3_RX1P	GPP3_TX1P	AH18	GPP_TX1P_C NC20 0.1u/4/X7R/16V/K PCIE1_OP 19
AC19		GPP3_RX1N	GPP3_TX1N	AG18	GPP_TX1N_C NC19 0.1u/4/X7R/16V/K PCIE1_ON 19
AH20		GPP3_RX0P	GPP3_TX0P	AG19	GPP_TX0P_C NC2 0.1u/4/X7R/16V/K USB3_OP 31
AG20		GPP3_RX0N	GPP3_TX0N	AF19	GPP_TX0N_C NC1 0.1u/4/X7R/16V/K USB3_ON 31

19 PCIE5_IP — PCIE5_IP
19 PCIE5_IN — PCIE5_IN
33 ML_IP — ML_IP
33 ML_IN — ML_IN
19 PCIE2_IP — PCIE2_IP
19 PCIE2_IN — PCIE2_IN
19 PCIE1_IP — PCIE1_IP
19 PCIE1_IN — PCIE1_IN
31 USB3_IP — USB3_IP
31 USB3_IN — USB3_IN

PCI_E slot TX need CAP close to slot side

PCIE ALINK

AC21		SB_RX3P	SB_TX3P	AG22	A_TX3P_C NC11 0.1u/4/X7R/16V/K A_TX3P 14
AD21		SB_RX3N	SB_TX3N	AH22	A_TX3N_C NC12 0.1u/4/X7R/16V/K A_TX3N 14
AD22		SB_RX2P	SB_TX2P	AF21	A_TX2P_C NC14 0.1u/4/X7R/16V/K A_TX2P 14
AE22		SB_RX2N	SB_TX2N	AG21	A_TX2N_C NC13 0.1u/4/X7R/16V/K A_TX2N 14
AF25		SB_RX1P	SB_TX1P	AF23	A_TX1P_C NC15 0.1u/4/X7R/16V/K A_TX1P 14
AG25		SB_RX1N	SB_TX1N	AG23	A_TX1N_C NC16 0.1u/4/X7R/16V/K A_TX1N 14
AG26		SB_RX0P	SB_TX0P	AG24	A_TX0P_C NC18 0.1u/4/X7R/16V/K A_TX0P 14
AH26		SB_RX0N	SB_TX0N	AH24	A_TX0N_C NC17 0.1u/4/X7R/16V/K A_TX0N 14

14 A_RX3P — A_RX3P
14 A_RX3N — A_RX3N
14 A_RX2P — A_RX2P
14 A_RX2N — A_RX2N
14 A_RX1P — A_RX1P
14 A_RX1N — A_RX1N
14 A_RX0P — A_RX0P
14 A_RX0N — A_RX0N

PLACE THESE CAP CLOSE TO NB.

NB_VCC

NR2	1.27K/4/1	AE20	PCE_BCALRP
NR3	1.82K/4/1	AD20	PCE_BCALRN
NR4	1.27K/4/1	AE10	PCE_RCALRP
NR5	1.82K/4/1	AD10	PCE_RCALRN
NR6	1.27K/4/1	F14	PCE_TCALRP
NR7	1.82K/4/1	E14	PCE_TCALRN

RX980/BGA692

EXP_A_TXP[0..15] — EXP_A_TXP[0..15] 18
EXP_A_TXN[0..15] — EXP_A_TXN[0..15] 18
EXP_A_RXP[0..15] — EXP_A_RXP[0..15] 18
EXP_A_RXN[0..15] — EXP_A_RXN[0..15] 18

GIGABYTE™

Title: RS780 PCIE I/F ,Switch

Size: Custom | Document Number: GA-970A-D3 | Rev: 1.2

Date: Friday, March 16, 2012 | Sheet 11 of 36

U3E

PART 5/5

GROUND

RX980/BGA692

U3D

PART 4/5

POWER

RX980/BGA692

VDDHT=>1.1V@3.25A

VDDPCIE=>1.1V@5.5A

1.1V@8500mA

VDDHTTX=>1.2V@1A

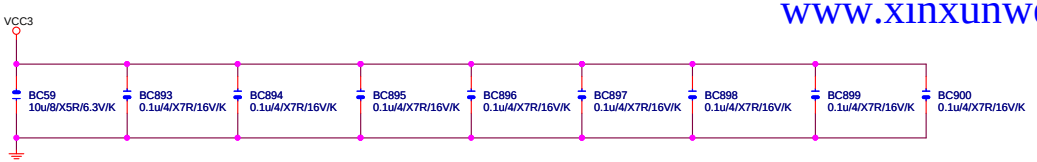
VDDA18=>1.8V@0.1A

VDDA18HTPLL=>1.8V@0.05A

VDDA18PCIE=>1.8V@2A

HT Link Stitching Caps

Title	RS780 POWER & GND
Size	Custom
Document Number	GA-970A-D3
Rev	1.2
Date:	Friday, March 16, 2012
Sheet	12 of 36



1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

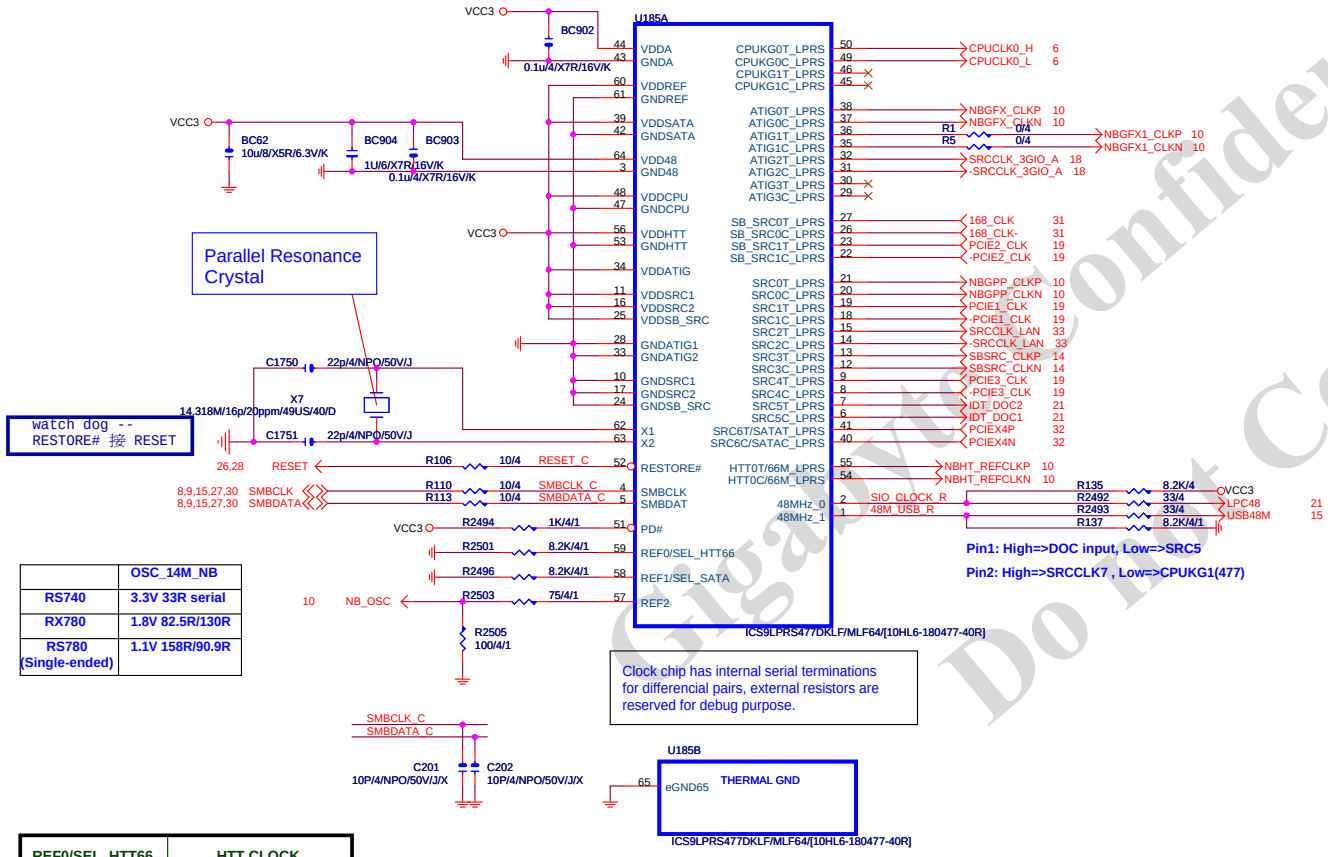
3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

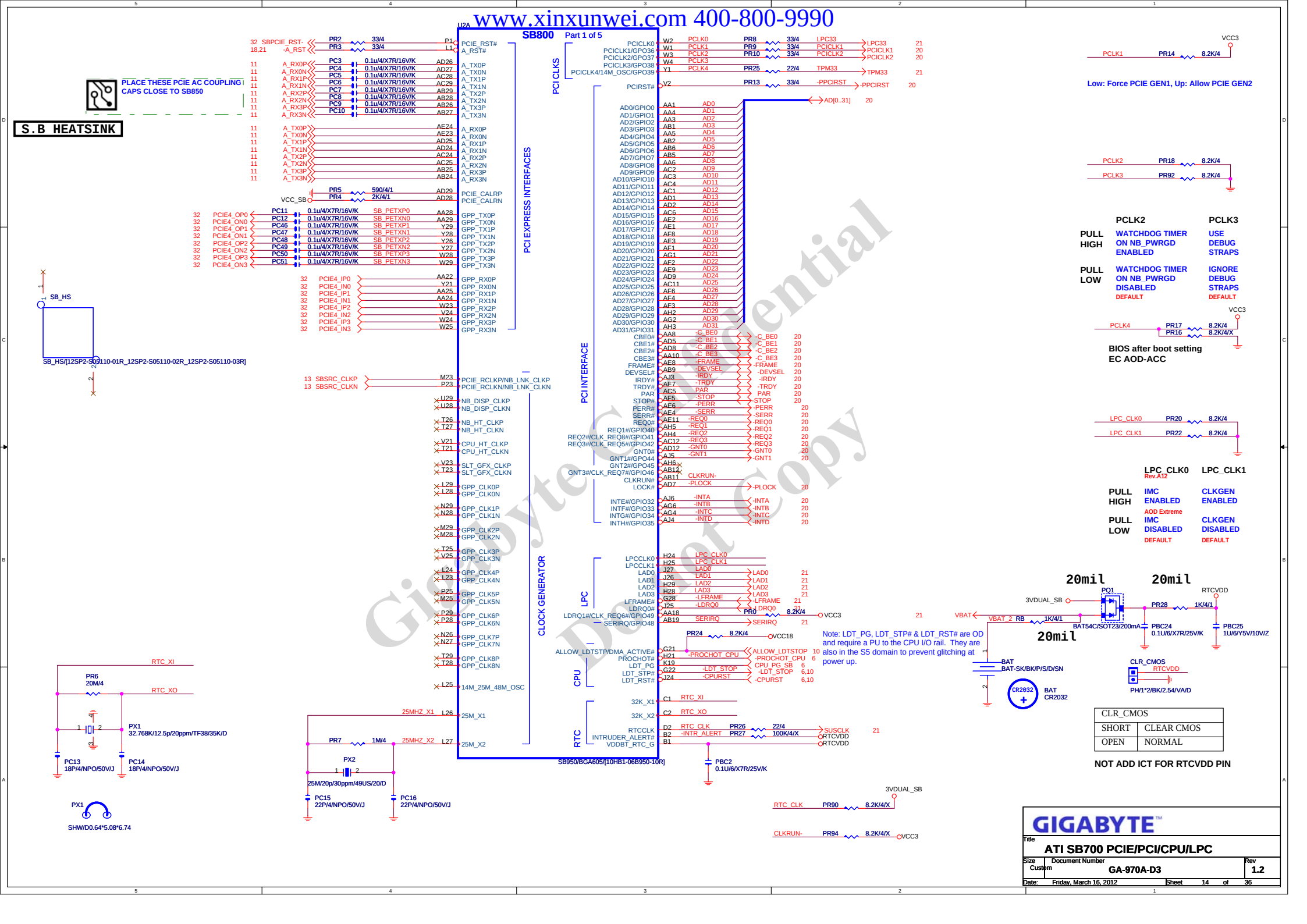
REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

GIGABYTE™

Title: RTM880N-793

Size: Custom | Document Number: GA-970A-D3 | Rev: 1.2

Date: Friday, March 16, 2012 | Sheet 13 of 36

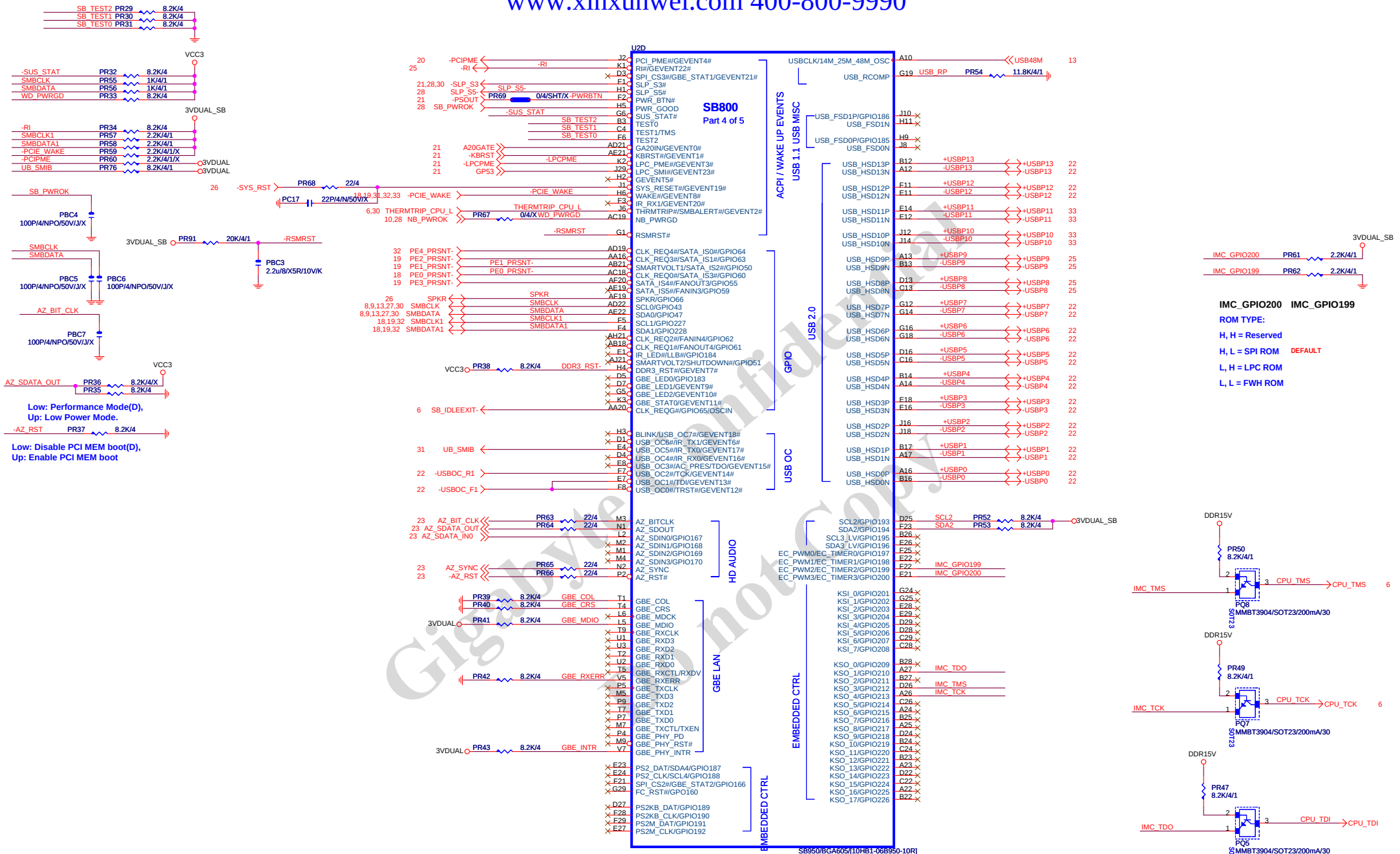


GIGABYTE™

Title: ATI SB700 PCIE/PCI/CPU/LPC

Size	Document Number	Rev
Custom	GA-970A-D3	1.2

Date: Friday, March 16, 2012 Sheet 14 of 36



GIGABYTE™

Title: ATI SB700 ACPI/USB/GPIO/AUDIO

Size	Document Number	Rev
Custom	GA-970A-D3	1.2

Date: Friday, March 16, 2012 Sheet 15 of 36

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

NOTE:
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

U2B

SB800
Part 2 of 5

SERIAL ATA

SP_TX0P_C AH9 SATA_TX0P
SP_TX0M_C AJ9 SATA_TX0N
SP_RX0M_C AJ8 SATA_RX0N
SP_RX0P_C AH8 SATA_RX0P
SP_TX1P_C AH10 SATA_TX1P
SP_TX1M_C AJ10 SATA_TX1N
SP_RX1M_C AG10 SATA_RX1N
SP_RX1P_C AE10 SATA_RX1P
SP_TX2P_C AG12 SATA_TX2P
SP_TX2M_C AE12 SATA_TX2N
SP_RX2M_C AJ12 SATA_RX2N
SP_RX2P_C AH12 SATA_RX2P
SP_TX3P_C AH14 SATA_TX3P
SP_TX3M_C AJ14 SATA_TX3N
SP_RX3M_C AG14 SATA_RX3N
SP_RX3P_C AE14 SATA_RX3P
SP_TX4P_C AG17 SATA_TX4P
SP_TX4M_C AF17 SATA_TX4N
SP_RX4M_C AJ17 SATA_RX4N
SP_RX4P_C AH17 SATA_RX4P
SP_TX5P_C AJ18 SATA_TX5P
SP_TX5M_C AH18 SATA_TX5N
SP_RX5M_C AH19 SATA_RX5N
SP_RX5P_C AJ19 SATA_RX5P

PR75 1K/4/1 SATA_CALRP AB14 SATA_CALRP
VCC_SB
PR74 931/4/1 SATA_CALRN AA14 SATA_CALRN

26 -SATA_LED -SATA_LED AD11 SATA_ACT#/GPIO67

TP5 SATA_X1 AD16 SATA_X1

TP7 SATA_X2 AC16 SATA_X2

GPIOD

FC_CLK AH28
FC_FBCLKOUT AG28
FC_FBCLKIN AF26
FC_OE#/GPIOD145 AF28
FC_AVD#/GPIOD146 AG29
FC_WE#/GPIOD148 AG26
FC_CE1#/GPIOD149 AF27
FC_CE2#/GPIOD150 AE29
FC_INT1/GPIOD144 AF29
FC_INT2/GPIOD147 AH27
FC_ADQ0/GPIOD128 AJ27
FC_ADQ1/GPIOD129 AJ26
FC_ADQ2/GPIOD130 AH25
FC_ADQ3/GPIOD131 AH24
FC_ADQ4/GPIOD132 AG23
FC_ADQ5/GPIOD133 AH23
FC_ADQ6/GPIOD134 AJ22
FC_ADQ7/GPIOD135 AG21
FC_ADQ8/GPIOD136 AF21
FC_ADQ9/GPIOD137 AH22
FC_ADQ10/GPIOD138 AJ23
FC_ADQ11/GPIOD139 AF23
FC_ADQ12/GPIOD140 AJ24
FC_ADQ13/GPIOD141 AJ25
FC_ADQ14/GPIOD142 AG25
FC_ADQ15/GPIOD143 AH26

HW MONITOR

FANOUT0/GPIO52 W5
FANOUT1/GPIO53 W6
FANOUT2/GPIO54 Y9
FANIN0/GPIO56 W7
FANIN1/GPIO57 V9
FANIN2/GPIO58 W8
TEMPIN0/GPIO171 B6
TEMPIN1/GPIO172 A6
TEMPIN2/GPIO173 A5
TEMPIN3/TALERT#/GPIO174 B5 SB_ALERT- 6
TEMP_COMM C7
VIN0/GPIO175 A3
VIN1/GPIO176 B4
VIN2/GPIO177 A4
VIN3/GPIO178 C5
VIN4/GPIO179 A7
VIN5/GPIO180 B7
VIN6/GBE_STAT3/GPIO181 B8
VIN7/GBE_LED3/GPIO182 A8

SPI ROM

SB_SPI_DI PR70 22/4 SB_SPI_DI_R J5 SPI_DI/GPIO164
SB_SPI_DO PR71 22/4 SB_SPI_DO_R E2 SPI_DO/GPIO163
SB_SPI_CLK PR72 22/4 SB_SPI_CLK_R K4 SPI_CLK/GPIO162
21 -SB_SPI_CS_ITE -SB_SPI_CS_ITE PR73 22/4 SB_SPI_CS- K9 SPI_CS1#/GPIO165
G2 ROM_RST#/GPIO161

NC1 G27
NC2 Y2

SB950/BGA605/[10HB1-06B950-10R]

PLACE SATA AC COUPLING CAPS CLOSE TO SB850

SATA3_0_1
SP_TX0P_C PC18 0.01u/4/X7R/25V/K SATA0TXPC
SP_TX0M_C PC19 0.01u/4/X7R/25V/K SATA0TXNC
SP_RX0M_C PC20 0.01u/4/X7R/25V/K SATA0RXNC
SP_RX0P_C PC21 0.01u/4/X7R/25V/K SATA0RXPC
SATA1TXPC PC30 0.01u/4/X7R/25V/K SP_TX1P_C
SATA1TXNC PC31 0.01u/4/X7R/25V/K SP_TX1M_C
SATA1RXNC PC32 0.01u/4/X7R/25V/K SP_RX1M_C
SATA1RXPC PC33 0.01u/4/X7R/25V/K SP_RX1P_C
SATA14/BU/H/OP/RA/D/2

SATA3_2_3
SP_TX2P_C PC22 0.01u/4/X7R/25V/K SATA2TXPC
SP_TX2M_C PC23 0.01u/4/X7R/25V/K SATA2TXNC
SP_RX2M_C PC24 0.01u/4/X7R/25V/K SATA2RXNC
SP_RX2P_C PC25 0.01u/4/X7R/25V/K SATA2RXPC
SATA3TXPC PC34 0.01u/4/X7R/25V/K SP_TX3P_C
SATA3TXNC PC35 0.01u/4/X7R/25V/K SP_TX3M_C
SATA3RXNC PC36 0.01u/4/X7R/25V/K SP_RX3M_C
SATA3RXPC PC37 0.01u/4/X7R/25V/K SP_RX3P_C
SATA14/BU/H/OP/RA/D/2

SATA3_4_5
SP_TX4P_C PC26 0.01u/4/X7R/25V/K SATA4TXPC
SP_TX4M_C PC27 0.01u/4/X7R/25V/K SATA4TXNC
SP_RX4M_C PC28 0.01u/4/X7R/25V/K SATA4RXNC
SP_RX4P_C PC29 0.01u/4/X7R/25V/K SATA4RXPC
SATA5TXPC PC38 0.01u/4/X7R/25V/K SP_TX5P_C
SATA5TXNC PC39 0.01u/4/X7R/25V/K SP_TX5M_C
SATA5RXNC PC40 0.01u/4/X7R/25V/K SP_RX5M_C
SATA5RXPC PC41 0.01u/4/X7R/25V/K SP_RX5P_C
SATA14/BU/H/OP/RA/D/2

VCC_SB
PBC8 1U/6/Y5V/10V/Z
PBC9 0.1u/4/Y5V/16V/Z
VCC3
PBC10 1U/6/Y5V/10V/Z
PBC11 0.1u/4/Y5V/16V/Z

VCC3
M_BIOS
21 -ITE_SPI_CS -ITE_SPI_CS 1 CS#
SB_SPI_DI 2 SO
-BIOS_WP 3 WP#
4 VSS
VDD 8 SPC23 0.1U/4/Y5V/16V/Z
HOLD# 7 -SPI_HOLD0
SCK 6 SB_SPI_CLK
SI 5 SB_SPI_DO
32M/SPI/SO8/200mil/S

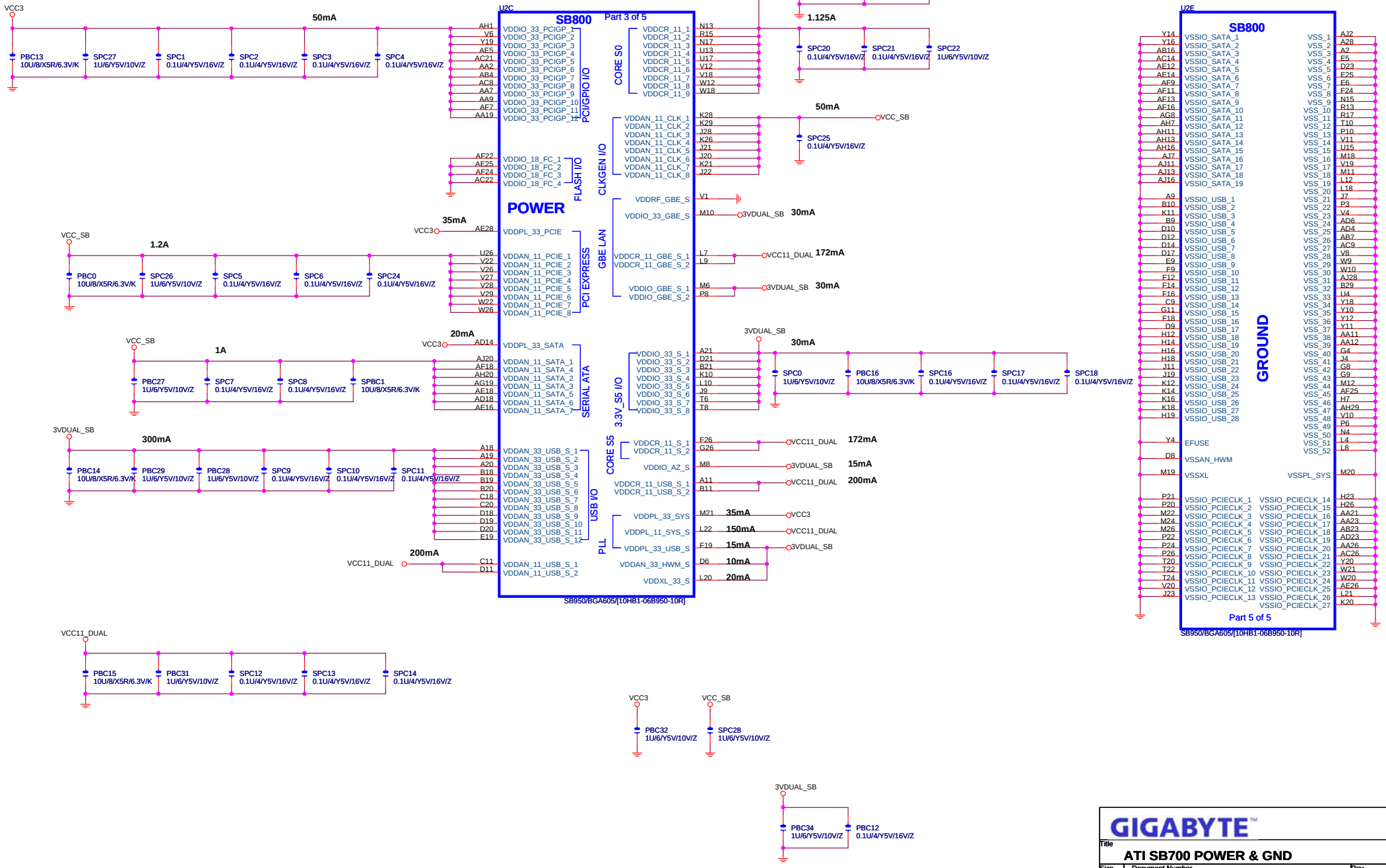
B_BIOS
21 -ITE_SPI_CS1 -ITE_SPI_CS1 1 CS#
SB_SPI_DI 2 SO
-BIOS_WP 3 WP#
4 VSS
VDD 8 VCC3
HOLD# 7 -SPI_HOLD0
SCK 6 SB_SPI_CLK
SI 5 SB_SPI_DO
32M/SPI/SO8/200mil/S

VCC3
-SPI_HOLD0 PR77 1K/4/1
-BIOS_WP PR78 1K/4/1
-ITE_SPI_CS PR79 330/4
-ITE_SPI_CS1 PR80 330/4

GIGABYTE

Title	ATI SB700 SATA/IDE/HWM/SPI	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 16 of 36	

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

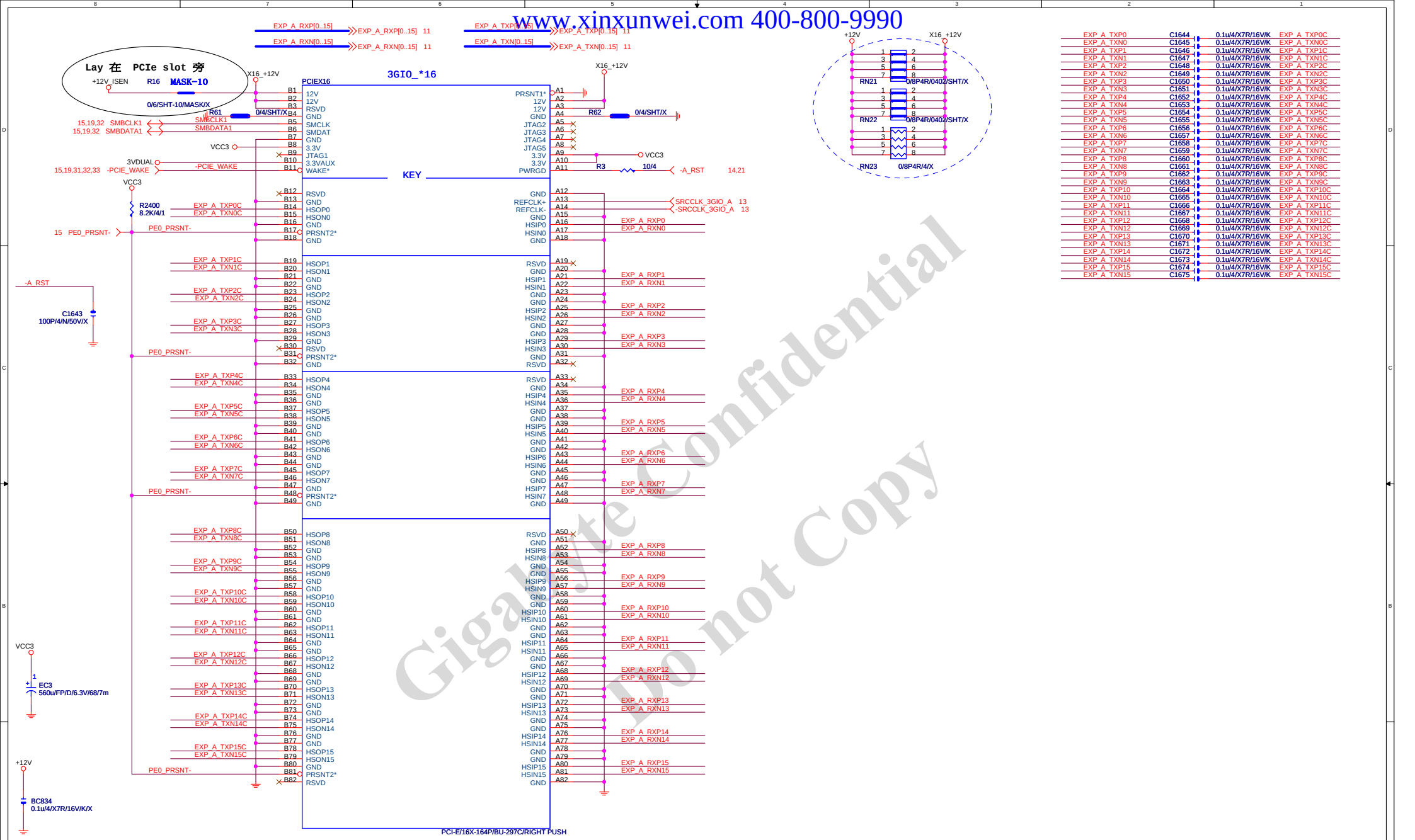


GIGABYTE™

Title: ATI SB700 POWER & GND

Size	Document Number	Rev
Custom	GA-970A-D3	1.2

Date: Friday, March 16, 2012 Sheet 17 of 36



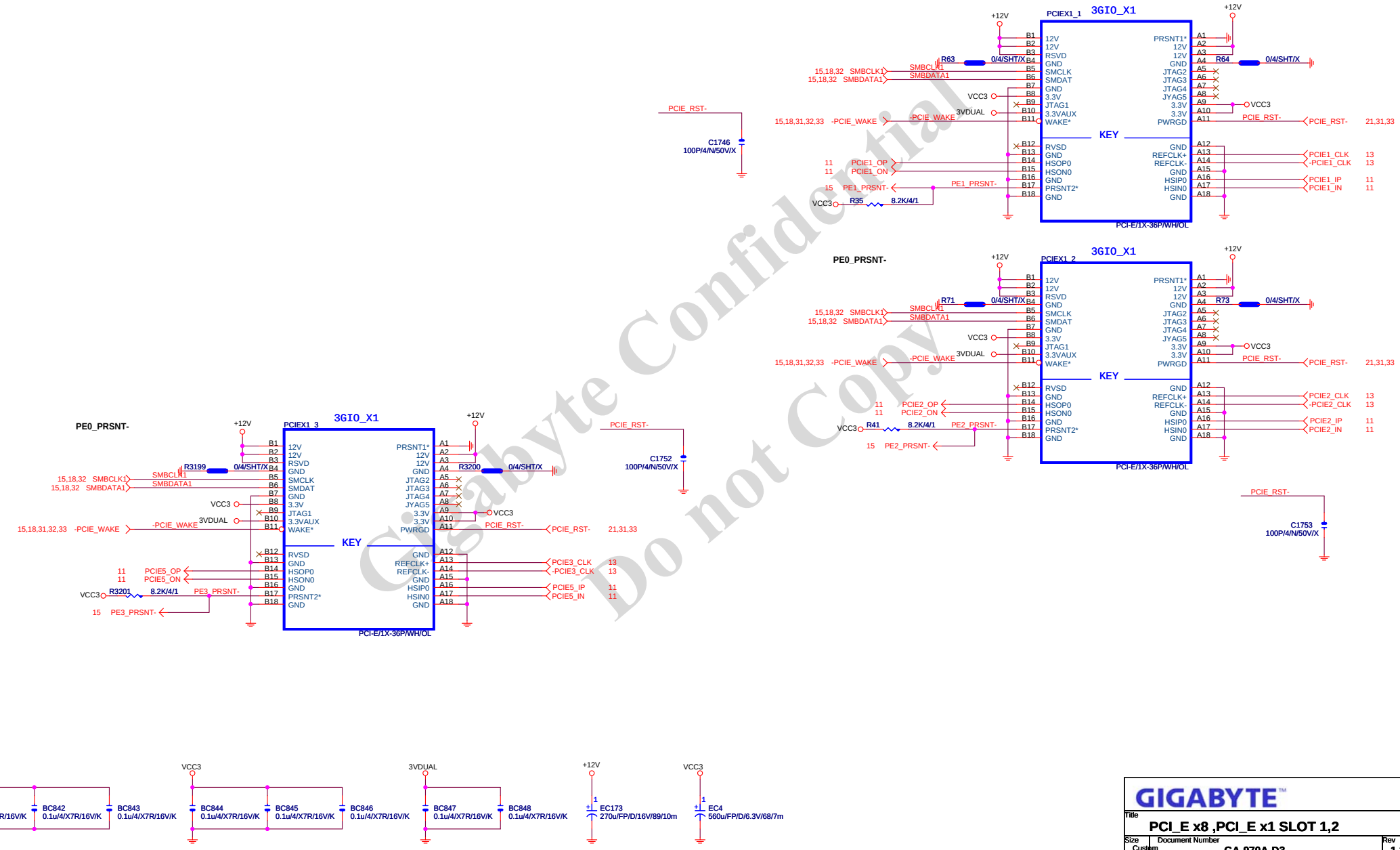
EXP_A_TXP0	C1644	0.1u/4/X7R/16V/K	EXP_A_TXP0C
EXP_A_TXN0	C1645	0.1u/4/X7R/16V/K	EXP_A_TXN0C
EXP_A_TXP1	C1646	0.1u/4/X7R/16V/K	EXP_A_TXP1C
EXP_A_TXN1	C1647	0.1u/4/X7R/16V/K	EXP_A_TXN1C
EXP_A_TXP2	C1648	0.1u/4/X7R/16V/K	EXP_A_TXP2C
EXP_A_TXN2	C1649	0.1u/4/X7R/16V/K	EXP_A_TXN2C
EXP_A_TXP3	C1650	0.1u/4/X7R/16V/K	EXP_A_TXP3C
EXP_A_TXN3	C1651	0.1u/4/X7R/16V/K	EXP_A_TXN3C
EXP_A_TXP4	C1652	0.1u/4/X7R/16V/K	EXP_A_TXP4C
EXP_A_TXN4	C1653	0.1u/4/X7R/16V/K	EXP_A_TXN4C
EXP_A_TXP5	C1654	0.1u/4/X7R/16V/K	EXP_A_TXP5C
EXP_A_TXN5	C1655	0.1u/4/X7R/16V/K	EXP_A_TXN5C
EXP_A_TXP6	C1656	0.1u/4/X7R/16V/K	EXP_A_TXP6C
EXP_A_TXN6	C1657	0.1u/4/X7R/16V/K	EXP_A_TXN6C
EXP_A_TXP7	C1658	0.1u/4/X7R/16V/K	EXP_A_TXP7C
EXP_A_TXN7	C1659	0.1u/4/X7R/16V/K	EXP_A_TXN7C
EXP_A_TXP8	C1660	0.1u/4/X7R/16V/K	EXP_A_TXP8C
EXP_A_TXN8	C1661	0.1u/4/X7R/16V/K	EXP_A_TXN8C
EXP_A_TXP9	C1662	0.1u/4/X7R/16V/K	EXP_A_TXP9C
EXP_A_TXN9	C1663	0.1u/4/X7R/16V/K	EXP_A_TXN9C
EXP_A_TXP10	C1664	0.1u/4/X7R/16V/K	EXP_A_TXP10C
EXP_A_TXN10	C1665	0.1u/4/X7R/16V/K	EXP_A_TXN10C
EXP_A_TXP11	C1666	0.1u/4/X7R/16V/K	EXP_A_TXP11C
EXP_A_TXN11	C1667	0.1u/4/X7R/16V/K	EXP_A_TXN11C
EXP_A_TXP12	C1668	0.1u/4/X7R/16V/K	EXP_A_TXP12C
EXP_A_TXN12	C1669	0.1u/4/X7R/16V/K	EXP_A_TXN12C
EXP_A_TXP13	C1670	0.1u/4/X7R/16V/K	EXP_A_TXP13C
EXP_A_TXN13	C1671	0.1u/4/X7R/16V/K	EXP_A_TXN13C
EXP_A_TXP14	C1672	0.1u/4/X7R/16V/K	EXP_A_TXP14C
EXP_A_TXN14	C1673	0.1u/4/X7R/16V/K	EXP_A_TXN14C
EXP_A_TXP15	C1674	0.1u/4/X7R/16V/K	EXP_A_TXP15C
EXP_A_TXN15	C1675	0.1u/4/X7R/16V/K	EXP_A_TXN15C

GIGABYTE™

Title: PCI EXPRESS X 16 ,X1

Size: Custom | Document Number: GA-970A-D3 | Rev: 1.2

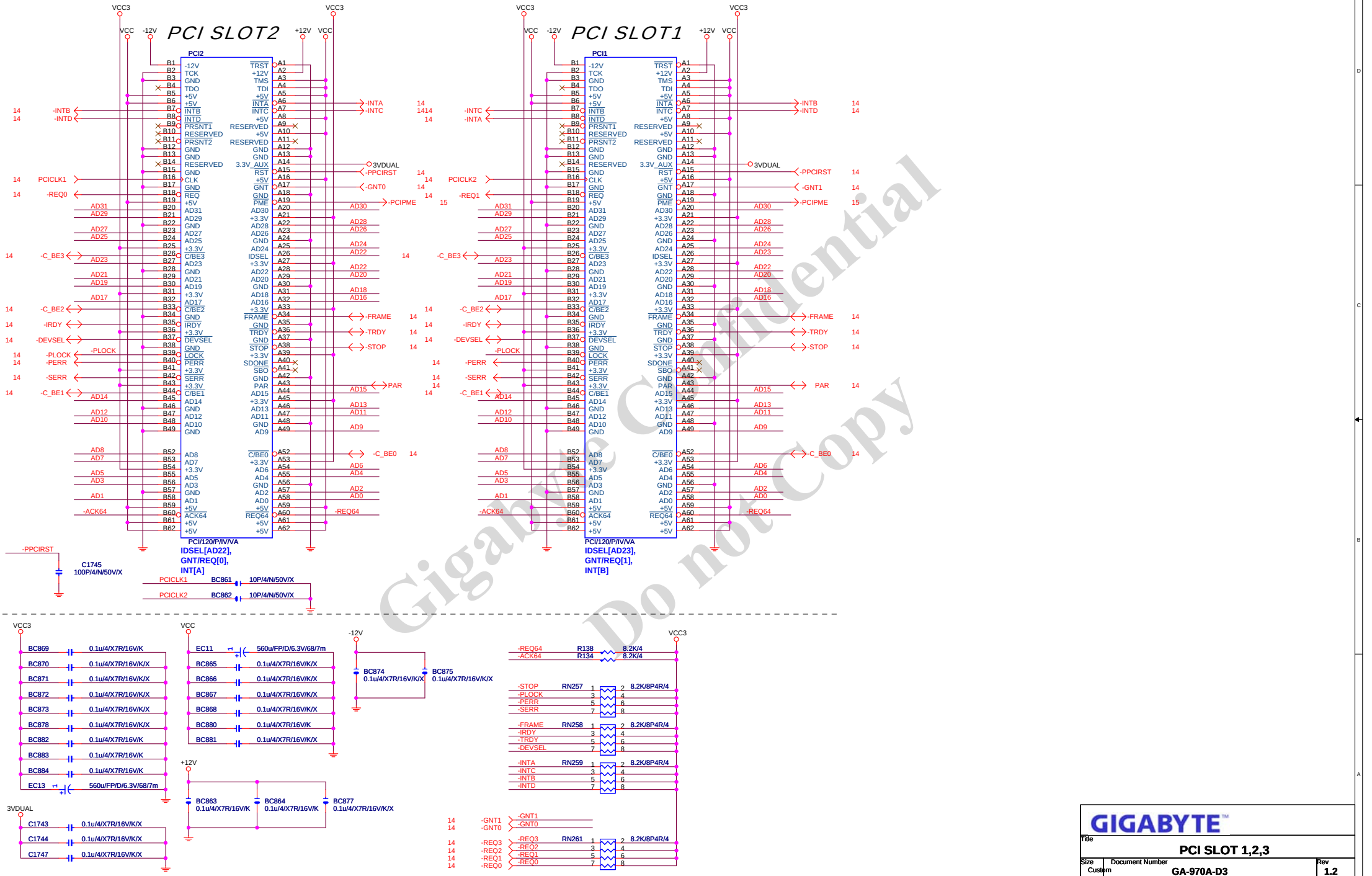
Date: Friday, March 16, 2012 | Sheet 18 of 36



GIGABYTE™

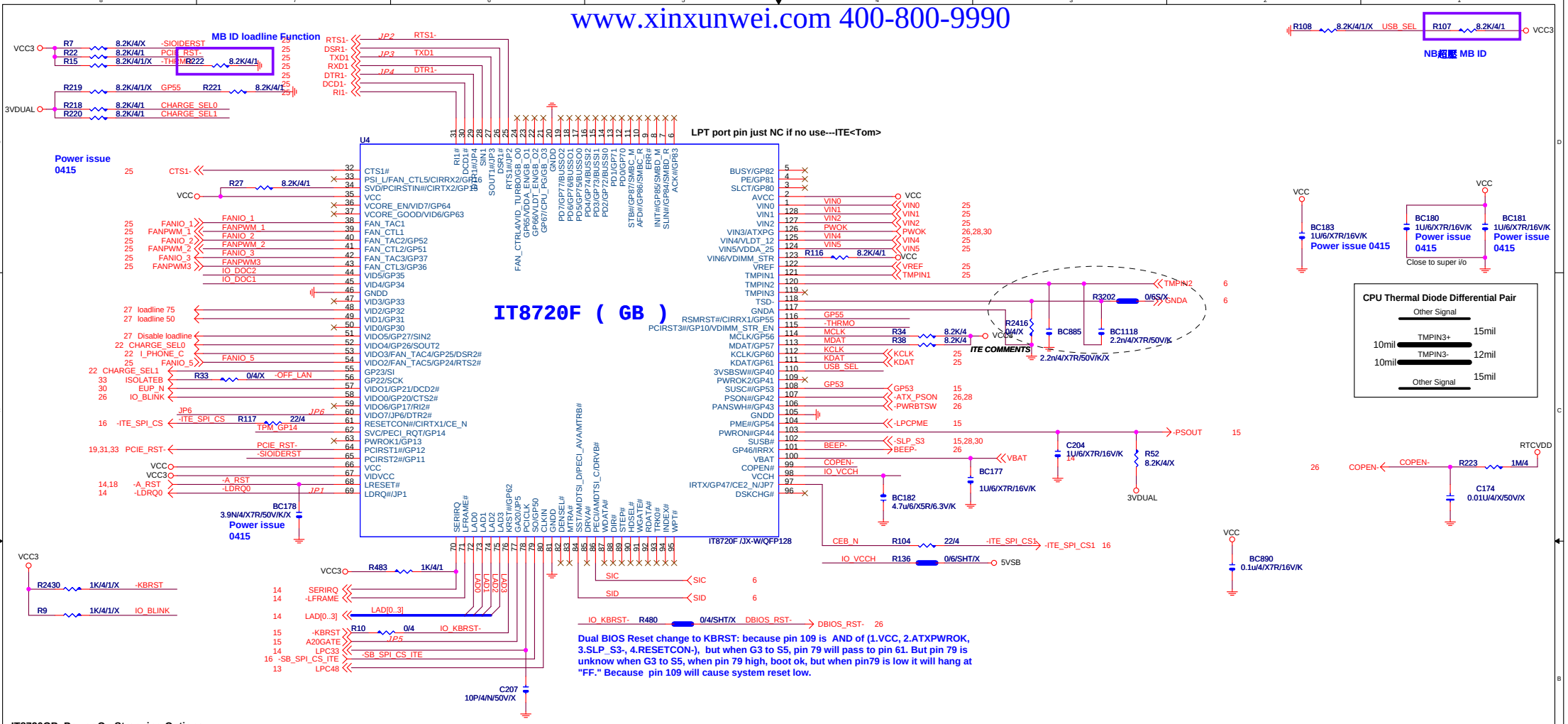
Title	PCI_E x8 ,PCI_E x1 SLOT 1,2	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 19 of 36	

PCI SLOT 1,2



GIGABYTE™

Title	PCI SLOT 1,2,3	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 20 of 36	



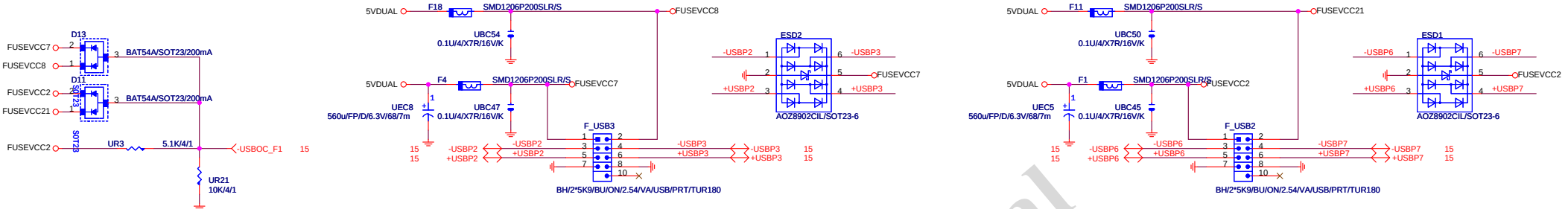
IT8720GB Power On Strapping Options

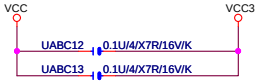
	Symbol	value	Description
JP1 Pin 69			
JP2 Pin 25	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 27	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 29	K8PWR_EN	1	K8 power sequence disabled
		0	K8 power sequence enabled
JP3 & JP5 Pin 27 & Pin 77	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5 Pin 77	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin 60	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function
JP7 Pin 97	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
		0	Disable Dual BIOS Function for GigaByte Only

GIGABYTE™

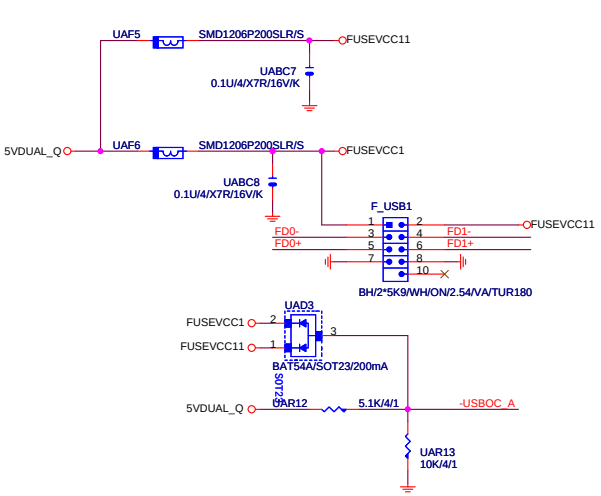
Title	ITE 8720 JX LPC IO ,Dual-BIOS ,TPM	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 21 of 36	

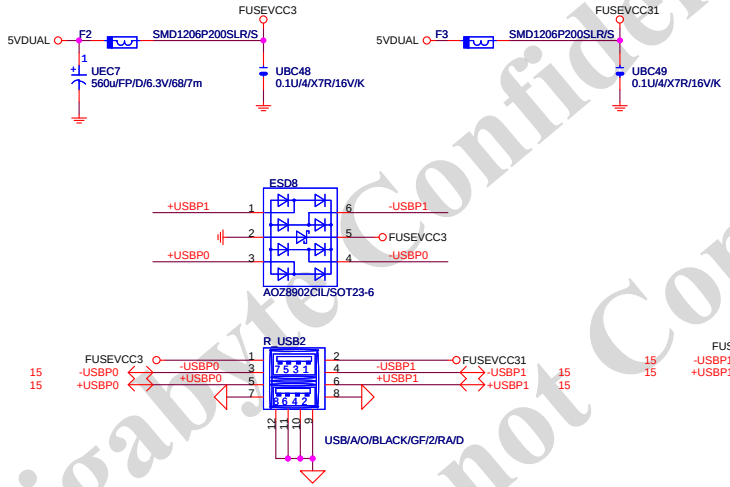
FRONT SIDE USB2



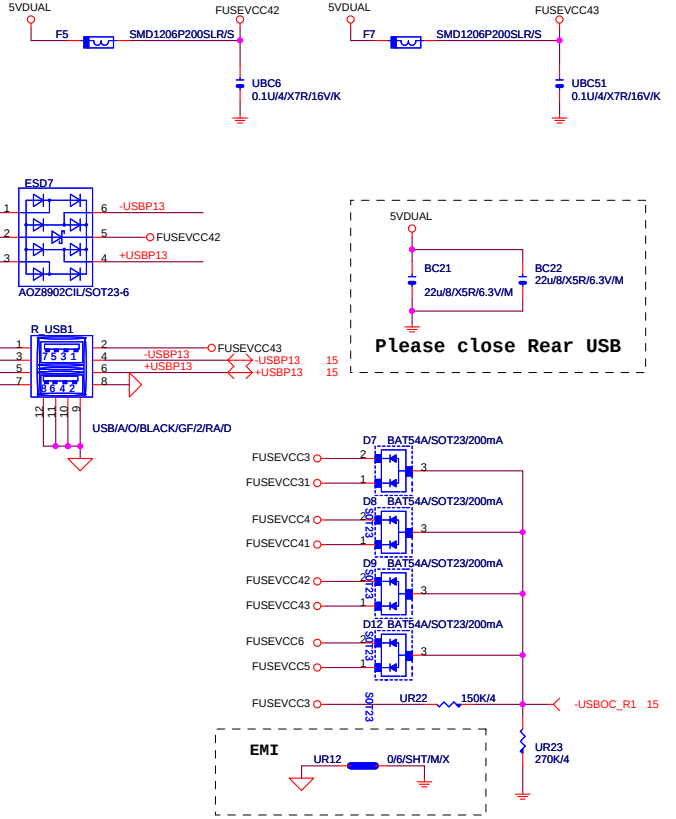


FRONT SIDE USB1





REAR USB

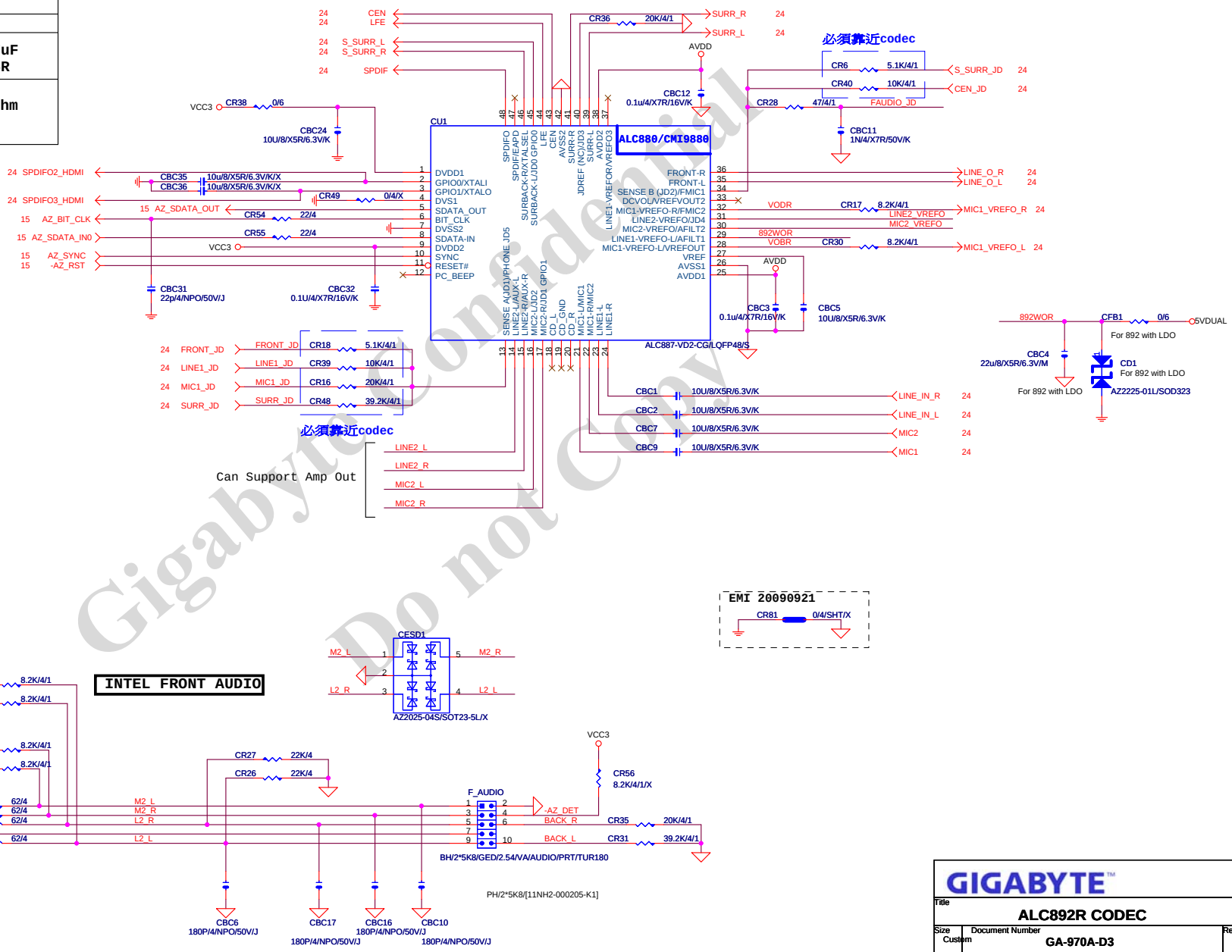


GIGABYTE™

Title	COM/LPT/F_USB/I_PWR	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 22 of 36	

AZALIA CODEC *ALC892/ALC889/ Colay*

	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm



GIGABYTE™

Title	ALC892R CODEC	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 23 of 36	

CR33 0/6/X

5VDUAL — CD4 CD4148WP/1206/300mA/X

AVDD — CBC8 22u/8/X5R/6.3V/M

CQ3 78L05/SOT89/0.1A/X

+12V — CD3 CD4148WP/1206/300mA/X

CD2 AZ2225-01L/SOD323/X

CBC21 1U/6/X7R/16V/K/X

For ESD PROTECT DIODE

SPDIF

23 SPDIFO3_HDMI — CR52 0/4/X

23 SPDIFO2_HDMI — CR53 0/4

CBC37 100p/4/NPO/50V/J

SPDIF_O — SPDIF_O PH/1*2/BK/2.54/VA/D

For HDMI SPDIF

FUSEVCC3

23 SPDIF

OPTICAL

FR/5P/BK/T/D/S(GY)

LINE OUT FRONT OUT

23 LINE_O_R — CEC2 100u/OS/D/16V/66/24m — CR7 62/4 — AJ_B5

23 LINE_O_L — CEC3 100u/OS/D/16V/66/24m — CR9 62/4 — AJ_B2

CR10 22K/4 CBC23 180P/4/NPO/50V/J CR8 22K/4 CBC26 180P/4/NPO/50V/J

LINE-IN

23 LINE_IN_R — CR5 62/4 — AJ_A5

23 LINE_IN_L — CR13 62/4 — AJ_A2

CBC18 180P/4/NPO/50V/J CBC27 180P/4/NPO/50V/J

MIC

23 MIC2 — CR29 62/4 — AJ_C5

23 MIC1 — CR32 62/4 — AJ_C2

23 MIC1_VREFO_R — CR37 0/4/SHT/X

23 MIC1_VREFO_L — CR34 0/4/SHT/X

CBC19 180P/4/NPO/50V/J CBC22 180P/4/NPO/50V/J

SURROUND

23 SURR_R — CEC5 100u/OS/D/16V/66/24m — CR46 62/4 — BJ_C5

23 SURR_L — CEC7 100u/OS/D/16V/66/24m — CR19 62/4 — BJ_C2

CR20 22K/4 CBC29 180P/4/NPO/50V/J CR45 22K/4 CBC28 180P/4/NPO/50V/J

CEN/LFE

23 LFE — CEC9 100u/OS/D/16V/66/24m — CR50 62/4 — BJ_B5

23 CEN — CEC10 100u/OS/D/16V/66/24m — CR41 62/4 — BJ_B2

CR42 22K/4 CBC25 180P/4/NPO/50V/J CR51 22K/4 CBC34 180P/4/NPO/50V/J

SURR BACK

23 S_SURR_R — CEC8 100u/OS/D/16V/66/24m — CR21 62/4 — BJ_A5

23 S_SURR_L — CEC4 100u/OS/D/16V/66/24m — CR47 62/4 — BJ_A2

CR43 22K/4 CBC33 180P/4/NPO/50V/J CR22 22K/4 CBC30 180P/4/NPO/50V/J

CESD2 AZ2025-04S/SOT23-5L/X — AJ_A2, AJ_B2, AJ_C2, AJ_C5

CESD4 AZ2025-04S/SOT23-5L/X — AJ_B5, AJ_A5, BJ_C2, BJ_A2

CESD3 AZ2025-04S/SOT23-5L/X — BJ_B5, BJ_A5, BJ_C5, BJ_B2

CESD5 AZ2025-04S/SOT23-5L/X — SPDIF, SPDIF_O

For Audio precision test

CBC38 2.2/4

USB_LAN — R_USB2 R_USB1

AUDIOB — 2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

23 LINE1_JD — LINE1_JD AJ_A5 AJ_A2 — LINE-IN

23 FRONT_JD — FRONT_JD AJ_B5 AJ_B2 — LINE-OUT

23 MIC1_JD — MIC1_JD AJ_C5 AJ_C2 — MIC-IN

BLUE LINE-IN

GREEN LINE-OUT

PINK MIC-IN

A3RJ/13P/B/[11NR6-403006-01_11NR6-403006-02]
3RJ+15F/[11NR6-403004-11]

AUDIOA — 2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

23 CEN_JD — CEN_JD BJ_B5 BJ_B2 — REAR

23 SURR_JD — SURR_JD BJ_C5 BJ_C2 — CEN

23 S_SURR_JD — S_SURR_JD BJ_A5 BJ_A2 — SIDE

Orange CEN/LFE

ALC880 - SURROUND
CMI9880 - Back SURR

Black Back side Speaker Azalia Port G

Gray Left & Right Side Speaker

CMI9880 - Side SURR

A3RJ/13P/OBG/[11NR6-403006-71]
3RJ+15F/[11NR6-403004-31]

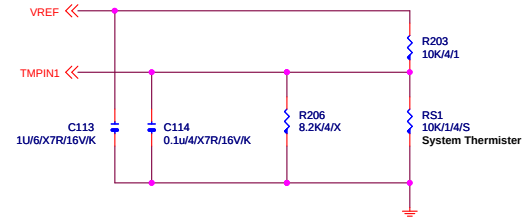
GIGABYTE™

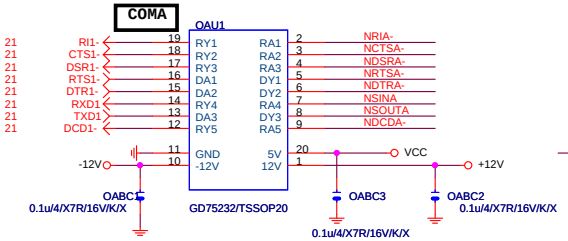
Title: AUDIO JACK

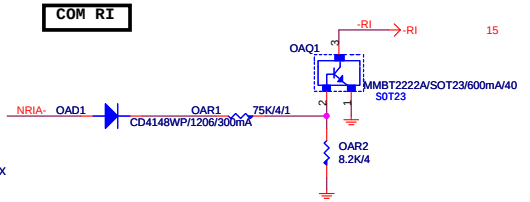
Size: Custom | Document Number: GA-970A-D3 | Rev: 1.2

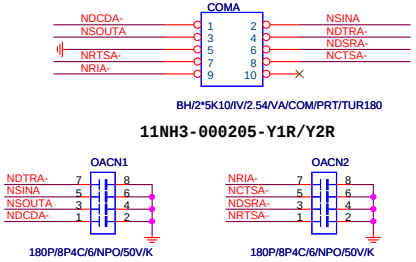
Date: Friday, March 16, 2012 | Sheet 24 of 36

Hardware Monitor circuits

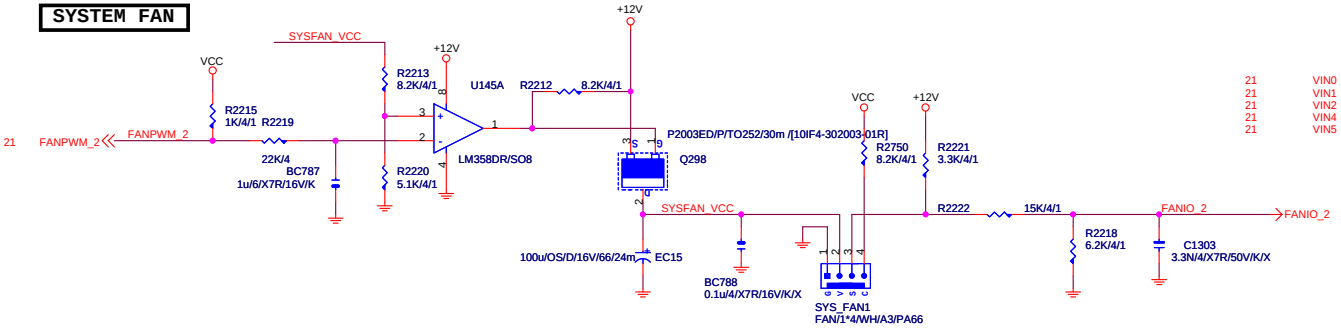


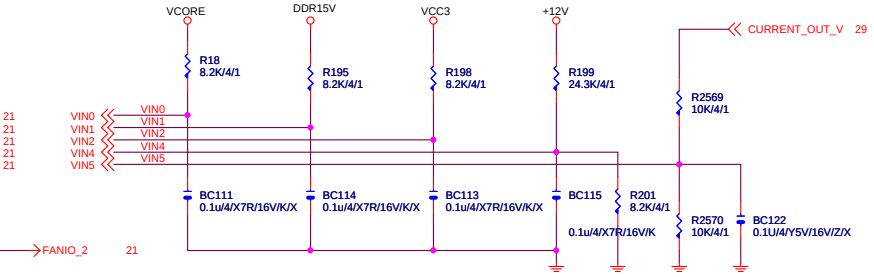




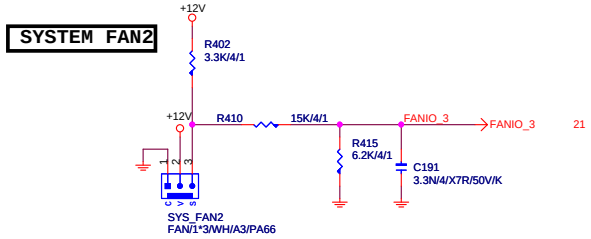


SYSTEM FAN

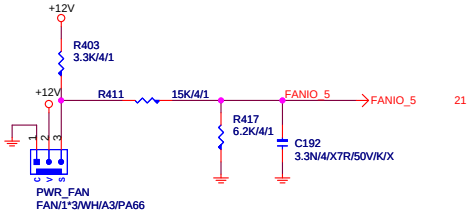




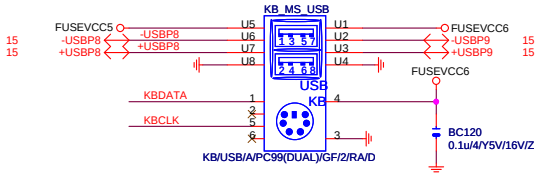
SYSTEM FAN2

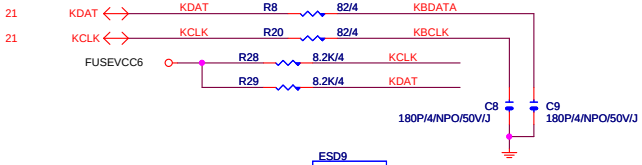


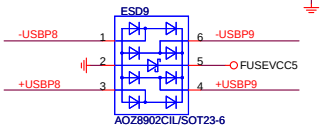
POWER FAN



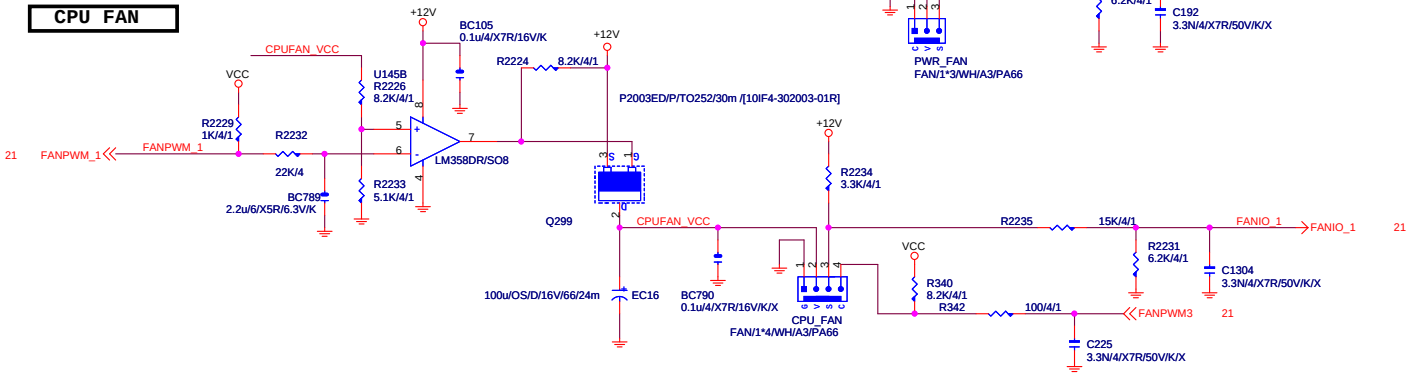
KB & USB





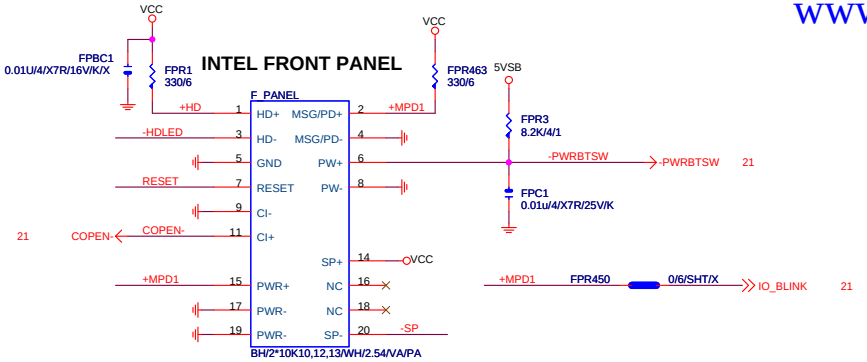


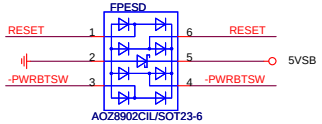
CPU FAN

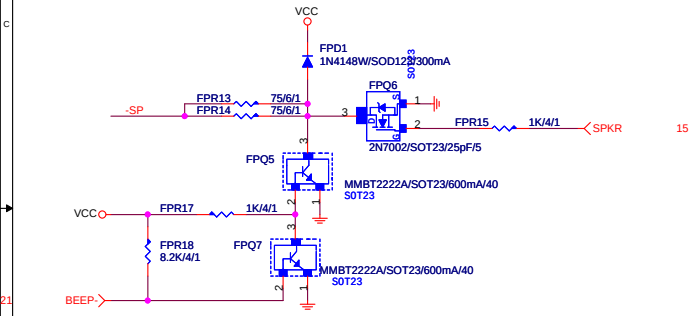


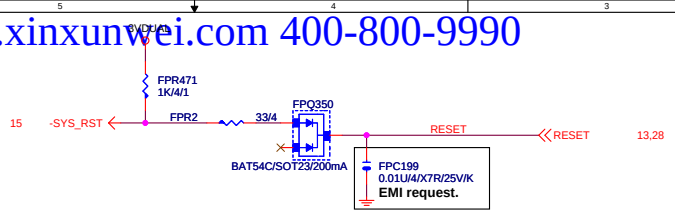
GIGABYTE			
Title: FAN/HWMO KB/MS			
Size: Custom	Document Number: GA-970A-D3		Rev: 1.2
Date: Friday, March 16, 2012		Sheet 25 of 36	

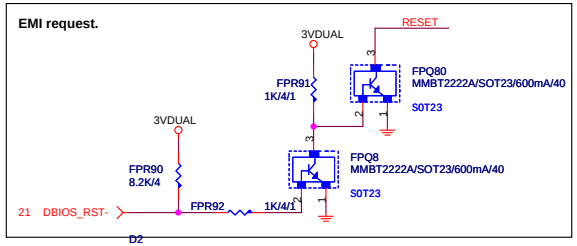
INTEL FRONT PANEL

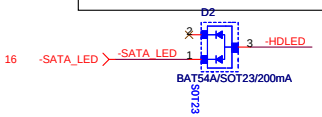


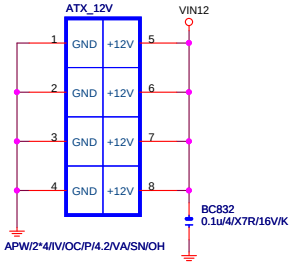


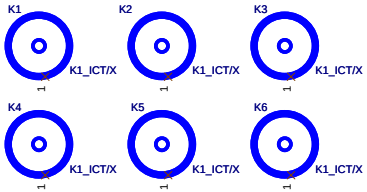


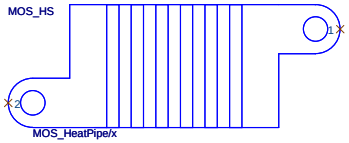


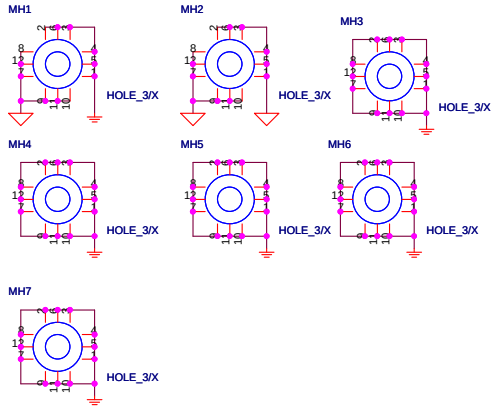




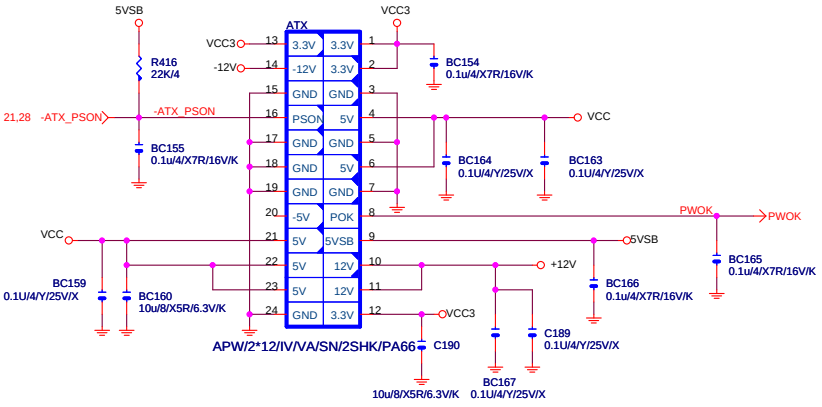


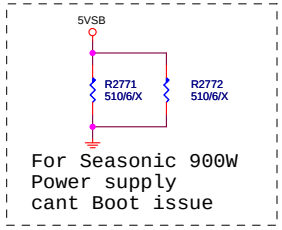




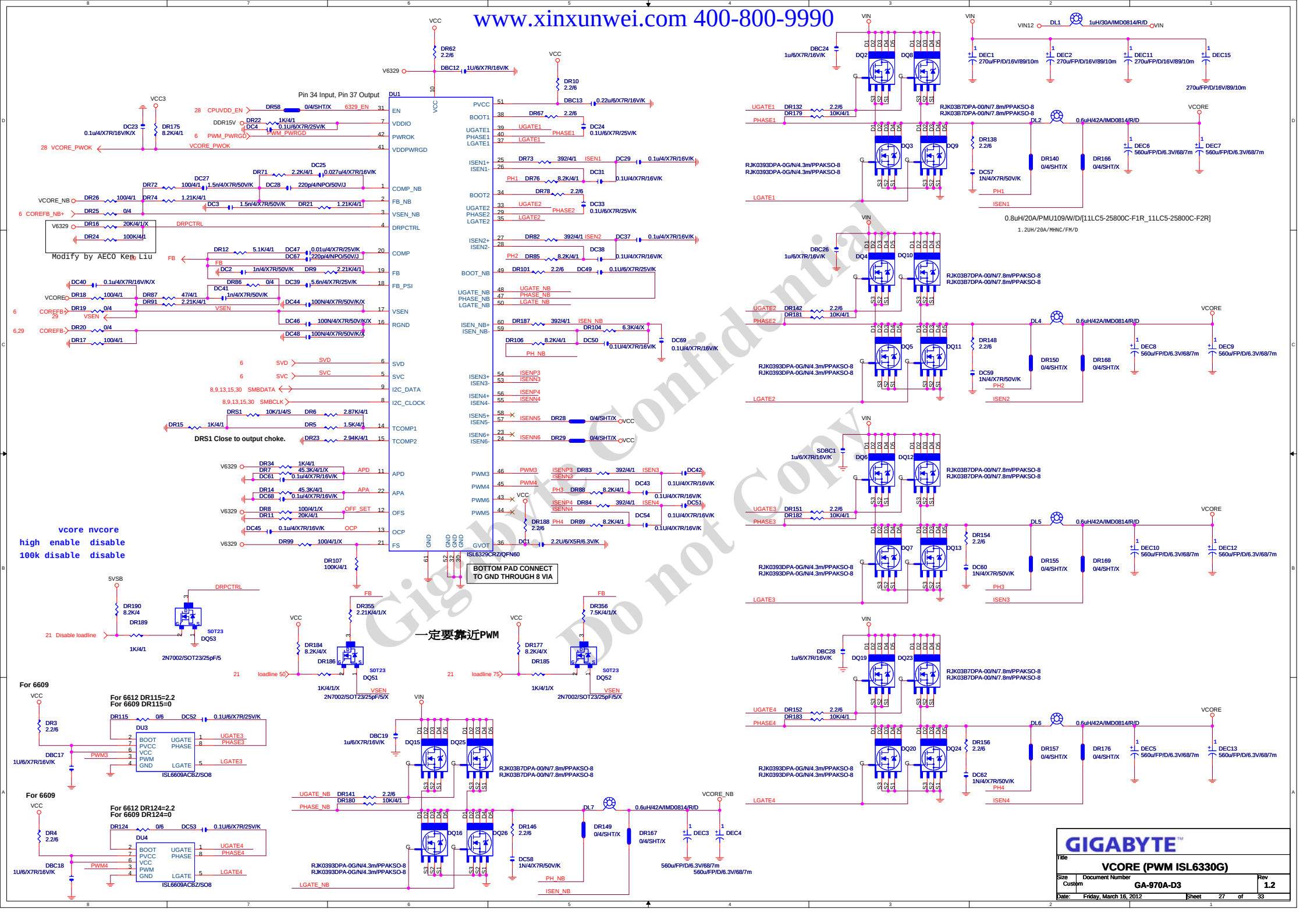


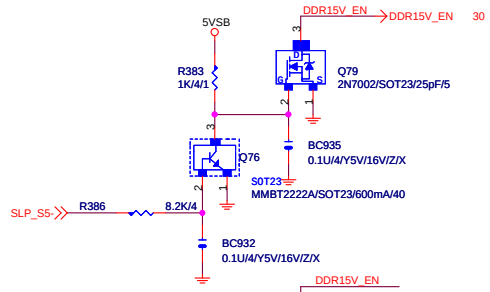
ATX POWER CONNECTOR

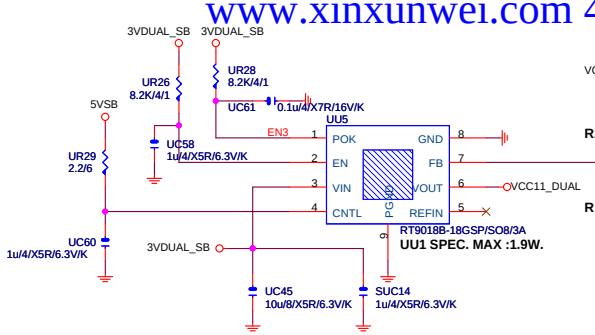


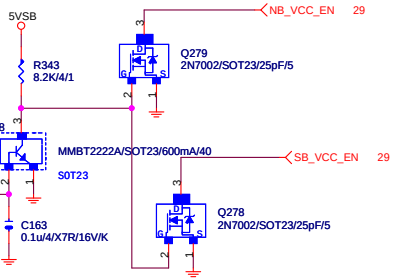


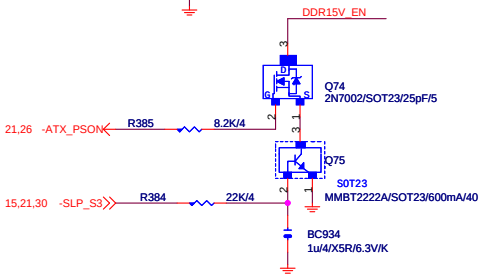
GIGABYTE			
Title: ATX, FRONT PANEL ,EC			
Size: Custom	Document Number: GA-970A-D3		Rev: 1.2
Date: Friday, March 16, 2012		Sheet 26 of 36	

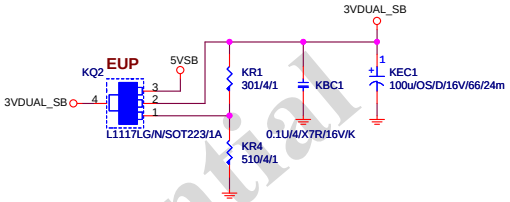


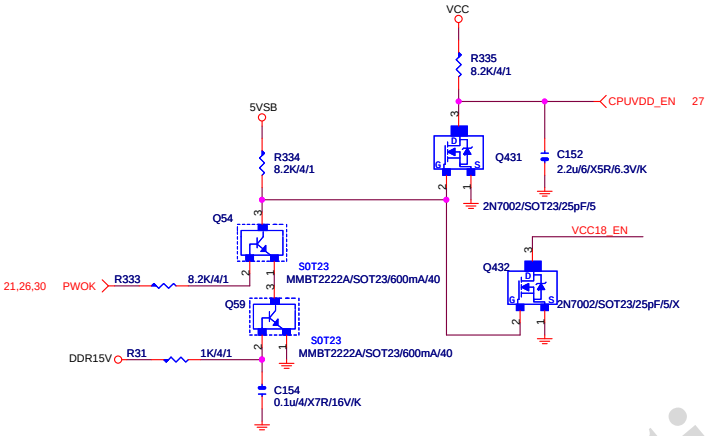




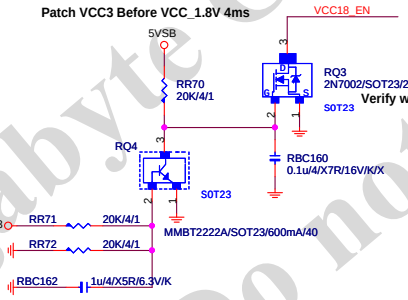


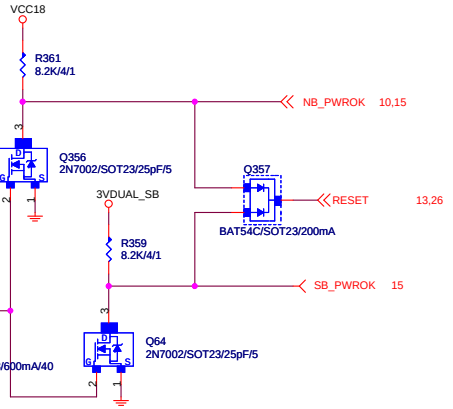




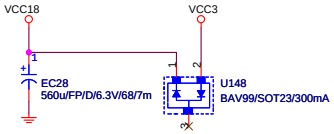


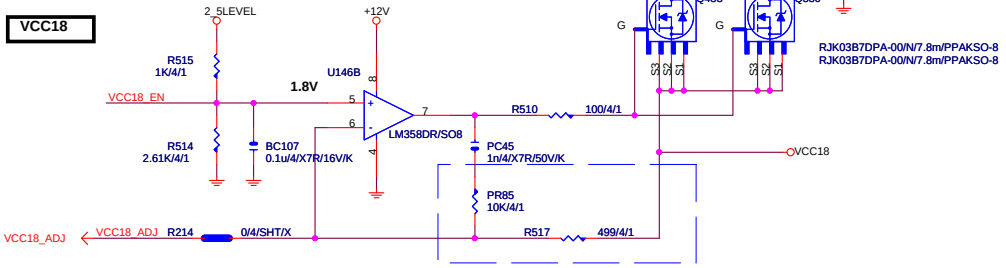
Patch VCC3 Before VCC_1.8V 4ms





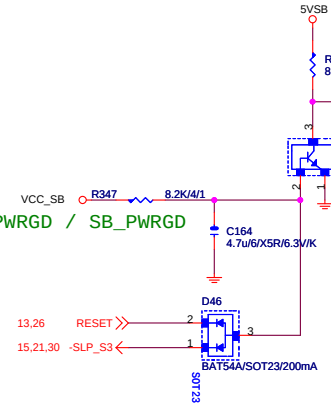
ATI for VCC3/VCC18 power ramp-up 2.1V





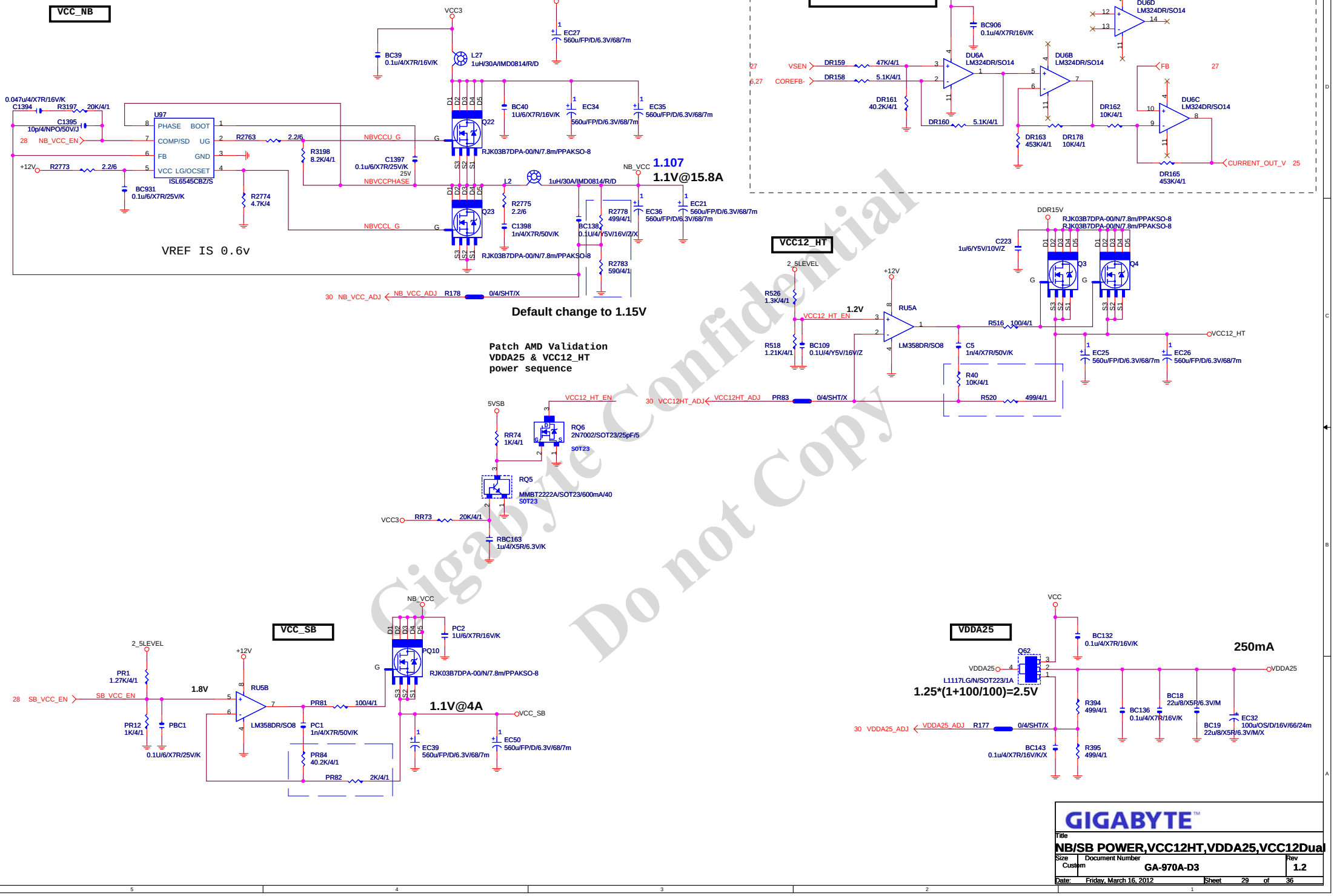
PWOK > NB_PWRGD / SB_PWRGD

(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms



GIGABYTE™

Title	POWER SEQUENCE ,VCC18 ,EUP	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 28 of 36	



GIGABYTE™

Title	NB/SB POWER,VCC12HT,VDDA25,VCC12Dual	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 29 of 36	

R2038不能上,會導致LM324 PIN1不能完全拉Lo

5VDUAL

VCC R344 8.2K/4/1 R349 12.1K/4/1 C176 1U/6/X7R/16V/K
5VSB R351 10K/4/1 R339 10K/4/1 C172 1U/6/X7R/16V/K
+12V R345 8.2K/4/1 R353 2.74K/4/1 C173 0.1U/6/X7R/25V/K
U9A U9B KA393D/SO8
R341 8.2K/4/1
R2854 1K/4/1
5VDUAL_GATE P_GATE
Q30 Q31 2SK4212/TO252/1200pF/7.8m
P2003ED/P/TO252/30m
EC31 560u/FP/D/6.3V/68/7m
EC24 100u/OS/D/16V/66/24m
Q34 2N7002/SOT23/25pF/5 SOT23
R366 1K/4/1
Q35 SOT23 MMBT2222A/SOT23/600mA/40
C180 1n/4/X7R/50V/K/X
15,21,28 -SLP_S3 R350 8.2K/4/1

EUP

D72 BAT54C/SOT23/200mA
21 EUP_N
R2855 8.2K/4/1
R2858 1K/4/1
R2856 68K/4/1
R2857 100K/4/1
Q361 3V SOT23 MMBT2222A/SOT23/600mA/40
C216 1U/6/X7R/16V/K
Q14 P_GATE BAT54A/SOT23/200mA
Q358 MMBT2907A/SOT23/-600mA/50

0x2A

BC1117 0.1u/4/X7R/16V/K
U5 NCT3933U/SOT23-8
3VDUAL R128 8.2K/4/1
VDDA25_ADJ NB_VCC_ADJ DDR_VTTREF
8,9,13,15,27 SMDATA R21 10/4 UPSDA UPSCK R25 10/4 SMBCLK

0X20 = 100% xVCC

BC1 0.1u/4/X7R/16V/K
U6 NCT3933U/SOT23-8
3VDUAL R130 1K/4/1
VCC18_ADJ VCC12HT_ADJ DDR15V_ADJ
UPSDA UPSCK

9.5V / 25A protect

9.5*(1.21K/(13.3K+1.21K))=0.792V

R529 220/6 Q96 AP431N/SOT23/150mA EC33 100u/OS/D/16V/66/24m
2_5LEVEL R513 133K/4/1 0.8V R512 63.4K/4/1 R530 13.3K/4/1 R519 1.21K/4/1 C264 1n/4/X7R/50V/K/X
+12V_ISEN
U146A LM358DR/SO8
BC106 0.1u/4/X7R/16V/K
R509 1K/4/1
R511 8.2K/4/X
THERMTRIP_CPU_L 6,15
Q92 SOT23 2N7002/SOT23/25pF/5
Q102 SOT23 2N7002/SOT23/25pF/5
R523 1K/4/1
Q101 SOT23 MMBT2222A/SOT23/600mA/40
C269 1n/4/X7R/50V/K/X
21,26,28 PWOK R506 8.2K/4/1

3VDUAL

C234 0.1u/4/X7R/16V/K
3VDUAL Q36 L1085DG/TO252/5A
R1735 100/4/1 C236 0.1u/4/X7R/16V/K EC40 560u/FP/D/6.3V/68/7m
R1737 169/4/1
1.25*(1+169/100)=3.36V

ESD5 CM1293A-04SO/S/X
SMBDATA SMBCLK 3VDUAL
VCC3 EC49 560u/FP/D/6.3V/68/7m

VREF IS 0.6V

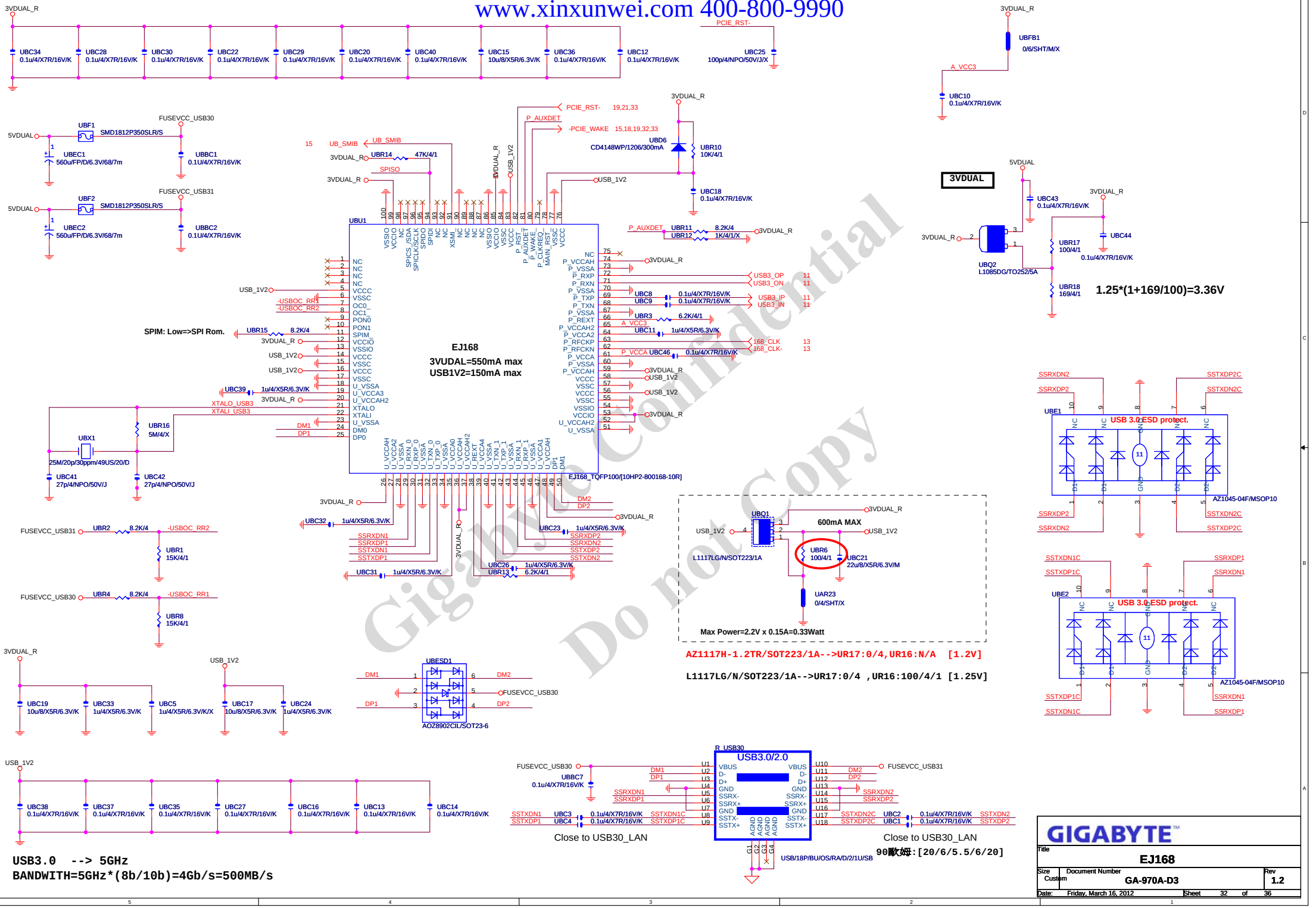
U99 ISL6545CBZ/S
PHASE BOOT COMP/SD UG FB GND VCC LG/OCSET
28 DDR15V_EN
PWM18_1 R2799 2.2/6
+12V Q394 BAT54C/SOT23/200mA R2802 2.2/6 BC933 1U/6/X7R/16V/K
0.047u/4/X7R/16V/K C1401 R2794 20K/4/1 10p/4/NPO/50V/J C1402
R2804 8.2K/4/1
R2803 8.2K/4/1 C1404 0.1u/6/X7R/25V/K 25V
DDR18V_PHASE DDR18VU_G DDR18VL_G
BC29 0.1u/4/X7R/16V/K
L3 1uH/30A/IMD0814/R/D
Q25 Q27 Q26 Q28 RJK03B7DPA-00/N/7.8m/PPAKSO-8
BC44 1U/6/X7R/16V/K EC44 560u/FP/D/6.3V/68/7m EC45 560u/FP/D/6.3V/68/7m
L4 1uH/30A/IMD0814/R/D
R2805 2.2/6 C1405 1n/4/X7R/50V/K
R2806 499/4/1 BC142 0.1U/4/Y5V/16V/Z/X WC18
R2810 330/4/1
EC46 EC47 EC48 0.01u/4/X7R/25V/K 560u/FP/D/6.3V/68/7m
DDR15V 1.507V 1.5V@20A
Default: 1.5V, from AMD
DDR15V_ADJ R213 0/4/SHT/X
0.6*(1+1.5K/1K)=1.5V

DDR15V

BC98 0.1u/4/X7R/16V/K BC102 4.7u/6/X5R/6.3V/K
U199 RT9173DPSP/3A/SO8/S
VIN VREF2 GND ENABLE VREF1 VCNTL VOUT GND BOOT_SEL
VCC R3186 1K/4/1 DDR_VTTREF R3187 1K/4/1 DDRVTT
BC100 0.1u/4/X7R/16V/K/X EC43 100u/OS/D/16V/66/24m BC99 0.1u/4/X7R/16V/K
4 VIA to GND

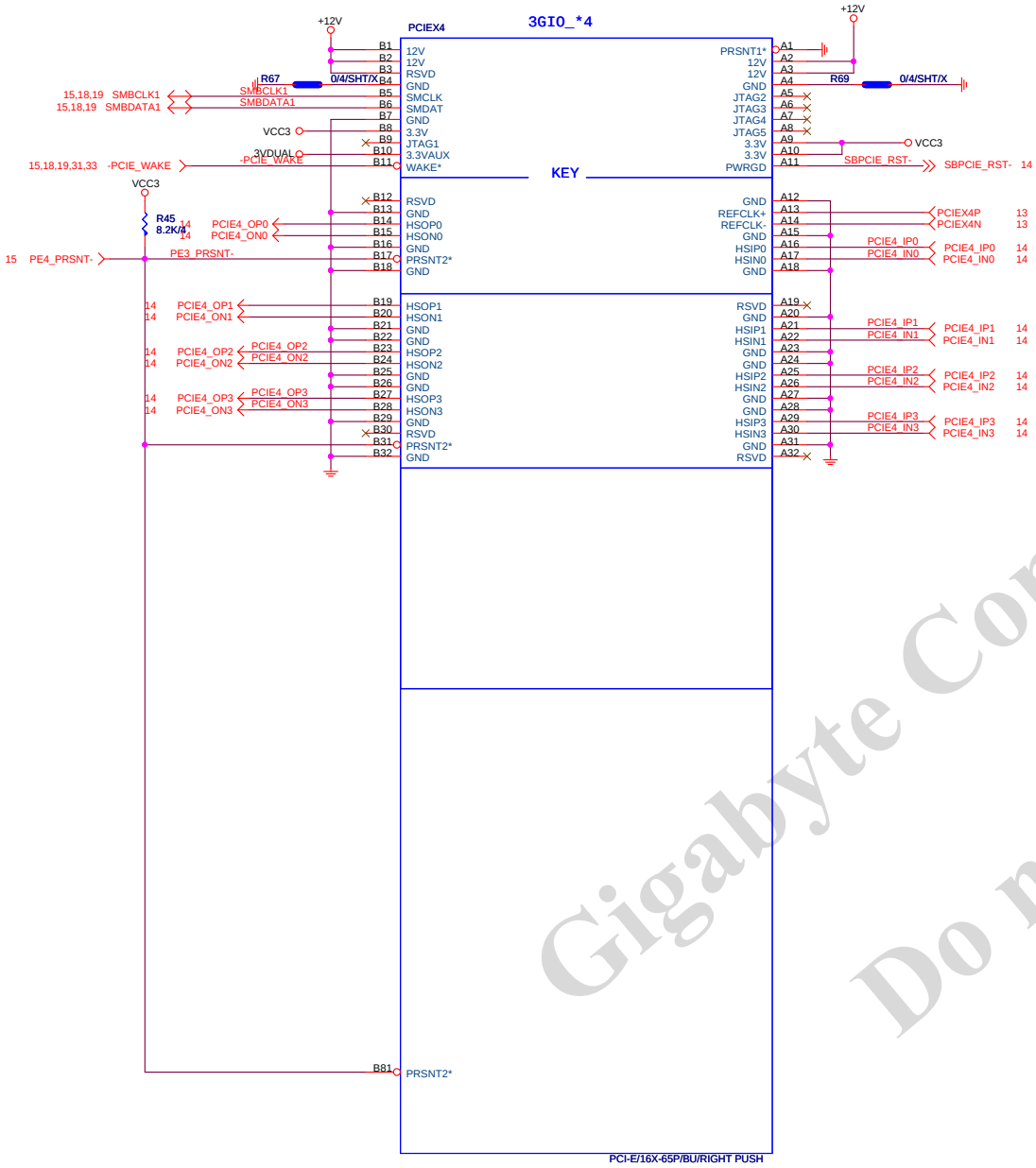
GIGABYTE™

Title	DDR POWER	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 30 of 36	



GIGABYTE™

Title	EJ168	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 32 of 36	



GIGABYTE™

Title: JMB362		
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 33 of 36	

PCIE-1G LAN

要用1% 的電阻,trace不能太長,建議在200 mil以內

LA_VDD33
LAR10 1K/4/1
LAR12 2.49K/4/1
LAU1
RTL8111F-VL-CG/QFN48

Data trace(MDI0~3)的+/-線長需等長,誤差在5mils以內,Pair跟Pair之間線長,最長跟最短data trace請勿超過800 mil

0.2版要修改

CLOSE LAN CHIP 離IC近越好200mil以內

XTALI_P
XTALO_P
LAX1 25M/20p/30ppm/49US/20/D
LAC5 27p/4/NPO/50V/J
LAC6 27p/4/NPO/50V/J

Pin34/35(VDDREG) 接到3VDUAL的trace 建議寬度大於 40mil

LAR9 1/6
LAR8 0/6/SHT/M/X
LAR7 8.2K/4
LAR6 8.2K/4
LED_LINK1000
VDD10
-PCIE_WAKE
LANWAKEB
ISOLATEB
PERSTB
PCIE_RST-
LABC4 100p/4/NPO/50V/J/X
LABC12 0.1u/4/X7R/16V/K
LABC13 4.7u/6/X5R/6.3V/K
VCC3
LAR4 1K/4/1
LAR5 15K/4/1
ISOLATEB 21
PCIE_RST- 19,21,31

LAR2 8.2K/4
LAR1 8.2K/4
3VDUAL_R
ML_OP
ML_ON
SRCCLK_LAN
-SRCCLK_LAN
ML_IP
ML_IN
LC3 0.1u/4/X7R/16V/K
LC4 0.1u/4/X7R/16V/K

USB_LAN CONNECTOR

P35-152-19W9

YELLOW
ORANGE (+,-)
GREEN (-,+)

3VDUAL_R
LAR13 150/4/1
LAFB2 0/6/SHT/M/X
LABC24 0.1u/4/Y5V/16V/Z/X
LABC22 0.01u/4/X7R/25V/K
LABC25 0.01u/4/X7R/25V/K
UP
DOWN
USB+LAN/1G/GO,Y/OS/RA/D/1

USB_LAN

RTL8101E:LR38/LC5/LR43/LC6-->O
RTL8111C:LC6-->O
RTL8102E:LC5/LC6-->O

3VDUAL_R
(CLOSE LU1)
LAEC1 560u/FP/D/6.3V/68/7m
LABC6 0.1u/4/X7R/16V/K
LABC16 0.1u/4/X7R/16V/K
LABC15 0.1u/4/X7R/16V/K
LABC5 0.1u/4/X7R/16V/K
LABC18 0.1u/4/X7R/16V/K
LABC14 0.1u/4/X7R/16V/K

VDD10
DVDD10
LABC11 0.1u/4/X7R/16V/K
LABC10 0.1u/4/X7R/16V/K
LABC9 0.1u/4/X7R/16V/K
LABC3 0.1u/4/X7R/16V/K
LABC19 0.1u/4/X7R/16V/K
LABC17 0.1u/4/X7R/16V/K
LABC8 0.1u/4/X7R/16V/K

LAL1 4.7uH/0.8A/3225/S
REGOUT
LABC20 4.7u/6/X5R/6.3V/K
LABC21 0.1u/4/X7R/16V/K
LABC1 0.1u/4/X7R/16V/K
LABC2 1u/4/X5R/6.3V/K
建議使用X5R電容

FUSEVCC4
5VDUAL
UBF3 SMD1206P200SLR/S
UEC6 560u/FP/D/6.3V/68/7m
LABC7 0.1U/4/X7R/16V/K
FUSEVCC41
UBF4 SMD1206P200SLR/S
LABC23 0.1U/4/X7R/16V/K

UBESD3
AOZ8902CIL/SOT23-6

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1

EMI
LR1 0/6/SHT/M/X

GIGABYTE

Title	REALTK RTL8111C	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.2
Date: Friday, March 16, 2012	Sheet 34 of 36	