GA-890GPA-UD3H

Revision : 3.1

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Model Name:GA-890GPA-UD3H

Version: 3.1

P-Code: U98137-0

Component value change history

Date	Change Item	Reason
2009.12.23	0.1 New BOM Release.	Modify from 9MMA79PT3-00-10K
2010.01.20	1.0A BOM Release.	Change SIO PWROK2 to -KBRST for Power-on F.F. issue
2010.01.21	1.0B BOM Release.	Change Heat-pipe ,轉 P-BOM
2010.02.06	1.0C BOM Release.	Modify NB_VCC level
2010.03.03	1.0D BOM Release.	Modify NB_VCC PWM OCP value
2010.03.16	2.0A BOM Release.	Add EC ,I_PWR function
2010.03.29	2.0B BOM Release.	Change EC SMBUS
2010.04.22	2.0C BOM Release.	Modify VCC11_DUAL power to 1.2xV for AMD SB850 USB hold-time issue
2010.05.03	2.0H BOM Release.	Change EC use SB850 ,swap DDR3 slot
2010.05.20	2.1A BOM Release.	Add CKG DOC function
2010.05.24	2.1B BOM Release.	Modify PCB silkscreen DDR3 2000+ to DDR3
2010.07.05	2.1B ECN BOM Release.	Add second source PCB (TF)祥裕
2010.08.16	2.1G BOM Release.	Change ALC892R to 892 ,Patch SPDIFIN noise issue
2010.09.09	2.1H BOM Release.	Change U2 SB850 A12 to A13
2010.09.30	2.2A BOM Release.	Change LAN RTL8111D to 8111E
2010.11.15	2.2A BOM Release.	轉 P-BOM
2010.12.06	3.0A BOM Release.	Change 16Mbit BIOS ,ALC889 ,Colay 6609+6612
2011.01.12	3.0B BOM Release.	Change U6,U7 to NCT3933 , ALC889 Line-in MLCC CBC10,CBC11 change to 22uF ,轉 P-BOM
2011.02.08	3.1A BOM Release.	Support AM3+ CPU

Circuit or PCB layout change for next version

Date	Change Item	Reason
2009.12.22	Rev0.1 Gerber-out	Modify from GA-MA790GPT-UD3H Rev1.0
2010.01.19	Rev1.0 Gerber-out	Change SIO PWROK2 to -KBRST for Power-on F.F. issue
2010.03.15	Rev2.0 Gerber-out	Add EC ,I_PWR function
2010.03.26	Rev2.01 Gerber-out	Change EC SMBUS
2010.04.30	Rev2.02 Gerber-out	Change EC use SB850 ,swap DDR3 slot
2010.05.19	Rev2.1 Gerber-out	Add CKG DOC function
2010.05.24	Rev2.11 Gerber-out	Modify PCB silkscreen DDR3 2000+ to DDR3
2010.08.13	Rev2.12 Gerber-out	Change ALC892R to 892 ,Patch SPDIFIN noise issue
2010.09.29	Rev2.2 Gerber-out	Change LAN RTL8111D to 8111E
2010.12.02	Rev3.0 Gerber-out	Change 16Mbit BIOS ,ALC889 ,Colay 6609+6612
2010.12.03	Rev3.01 Gerber-out	Change 16Mbit BIOS ,ALC889 ,Colay 6609+6612

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Title: BOM & PCB HISTORY

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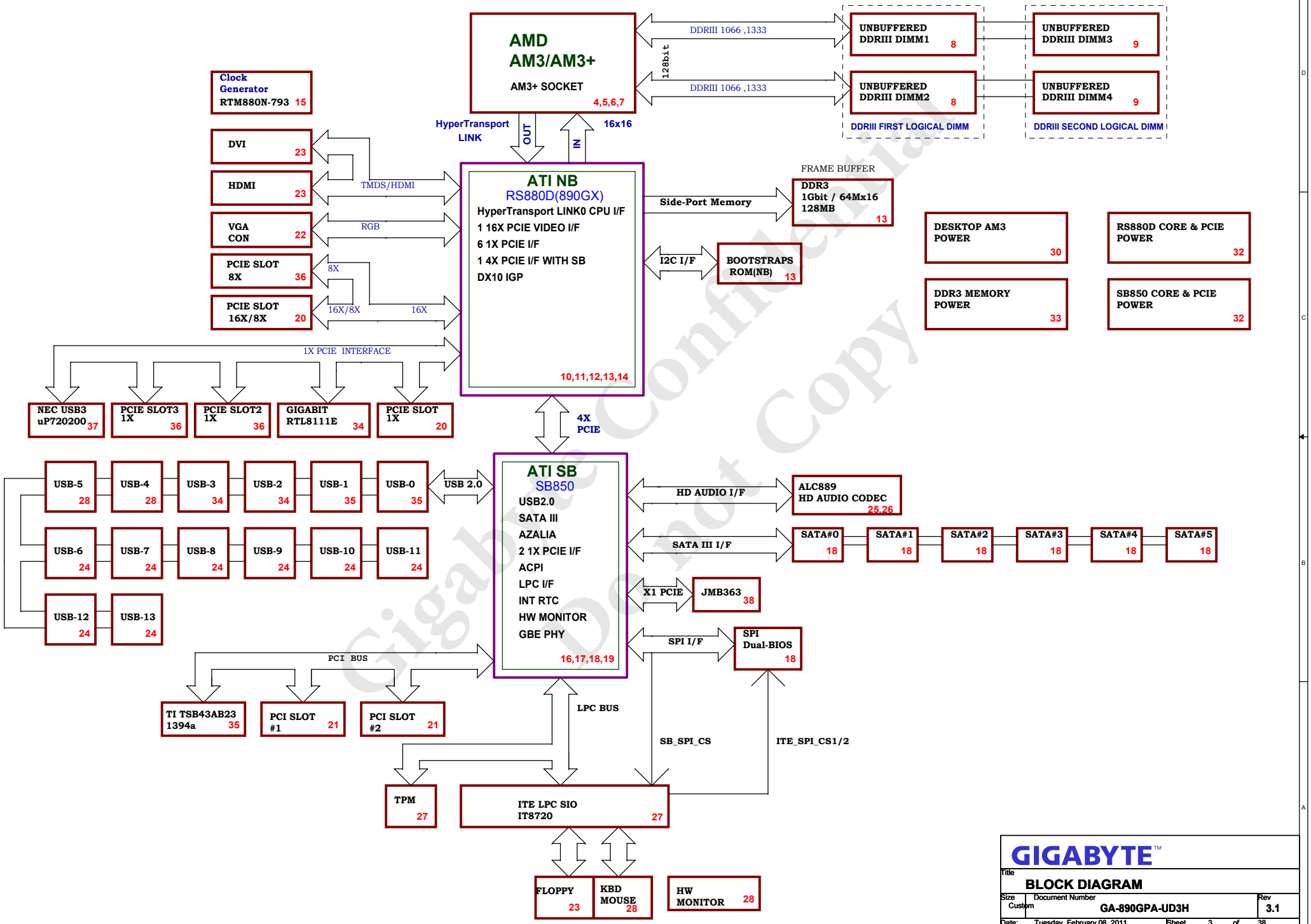
RS880 CUSTOMER DESKTOP REFERENCE DESIGN



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Title: BLOCK DIAGRAM

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L0_CADIN_L[0..15] L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15] L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] 10

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

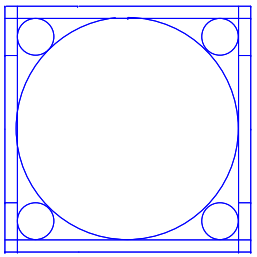
HYPERTRANSPORT

10 L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 10
10 L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 10
10 L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 10
10 L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 10
10 L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 10
10 L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 10
10 L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 10
10 L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 10
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/941AM3/S/GF/[10SC1-A01942-01R]

M2CPU

AM2RM/PP/BU/PB/[12KRC-04K812-12R]



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Title: CPU HYPER TRANSPORT

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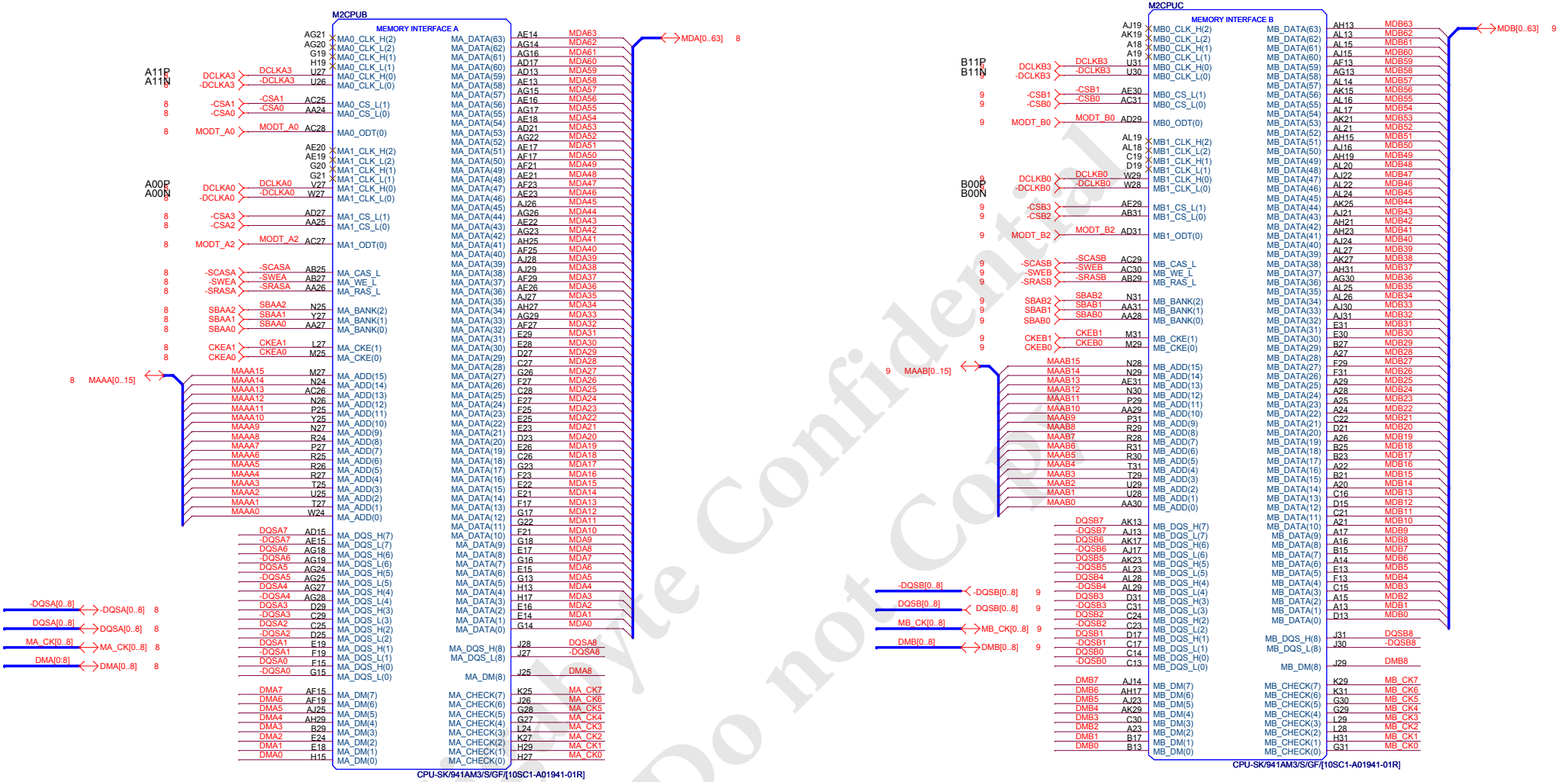

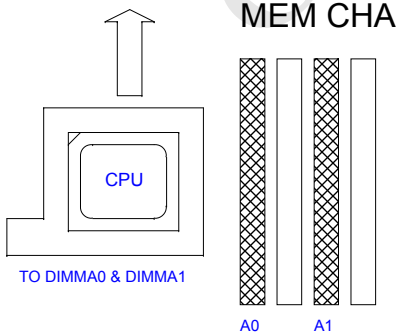

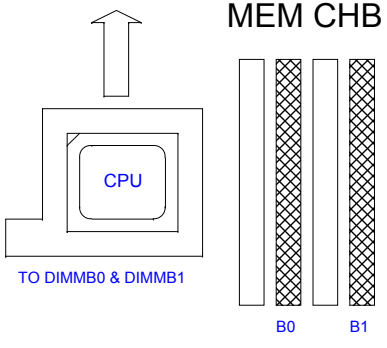

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Title: CPU DDRIII MEMORY			
Size: Custom	Document Number: GA-890GPA-UD3H		Rev: 3.1
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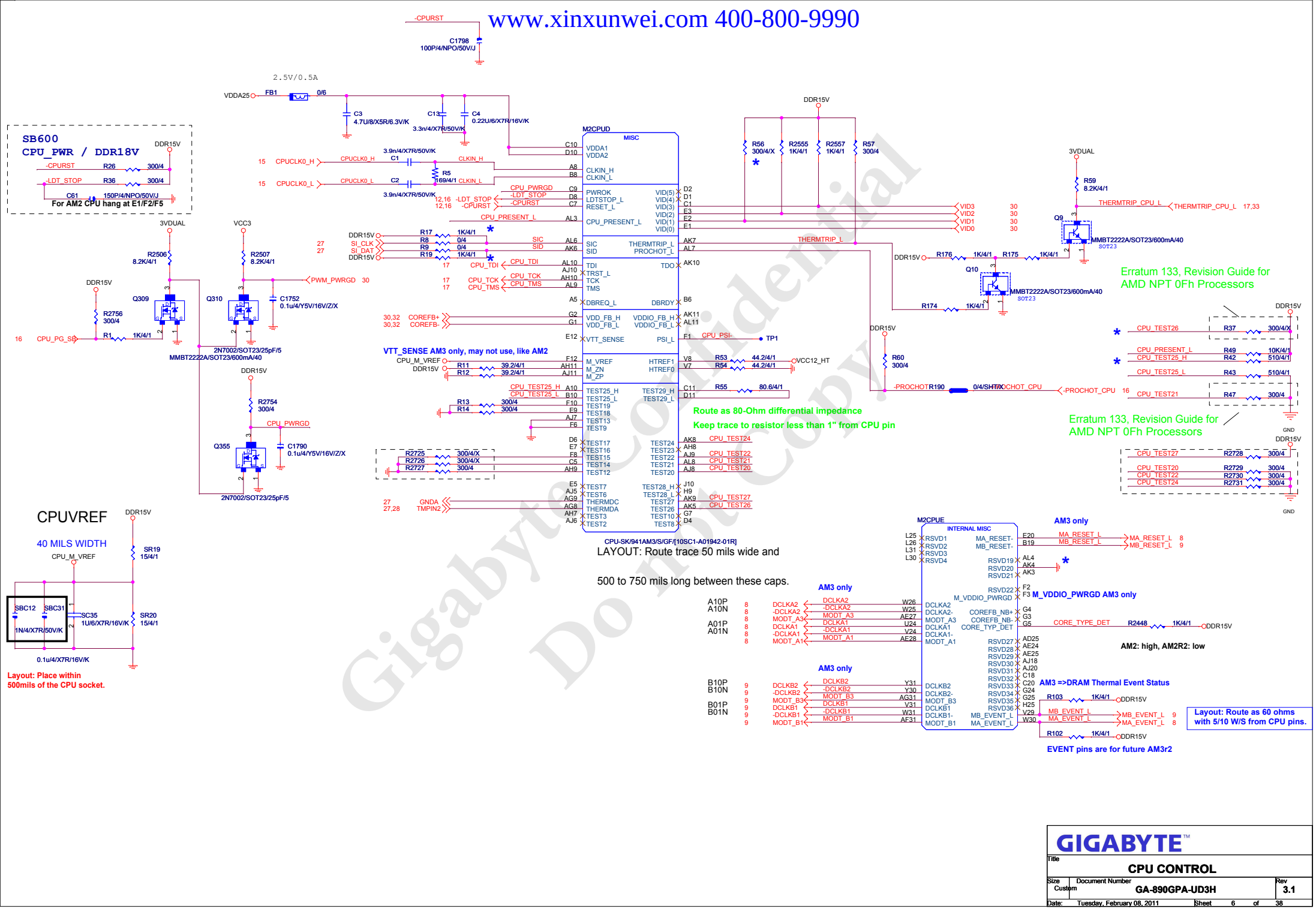
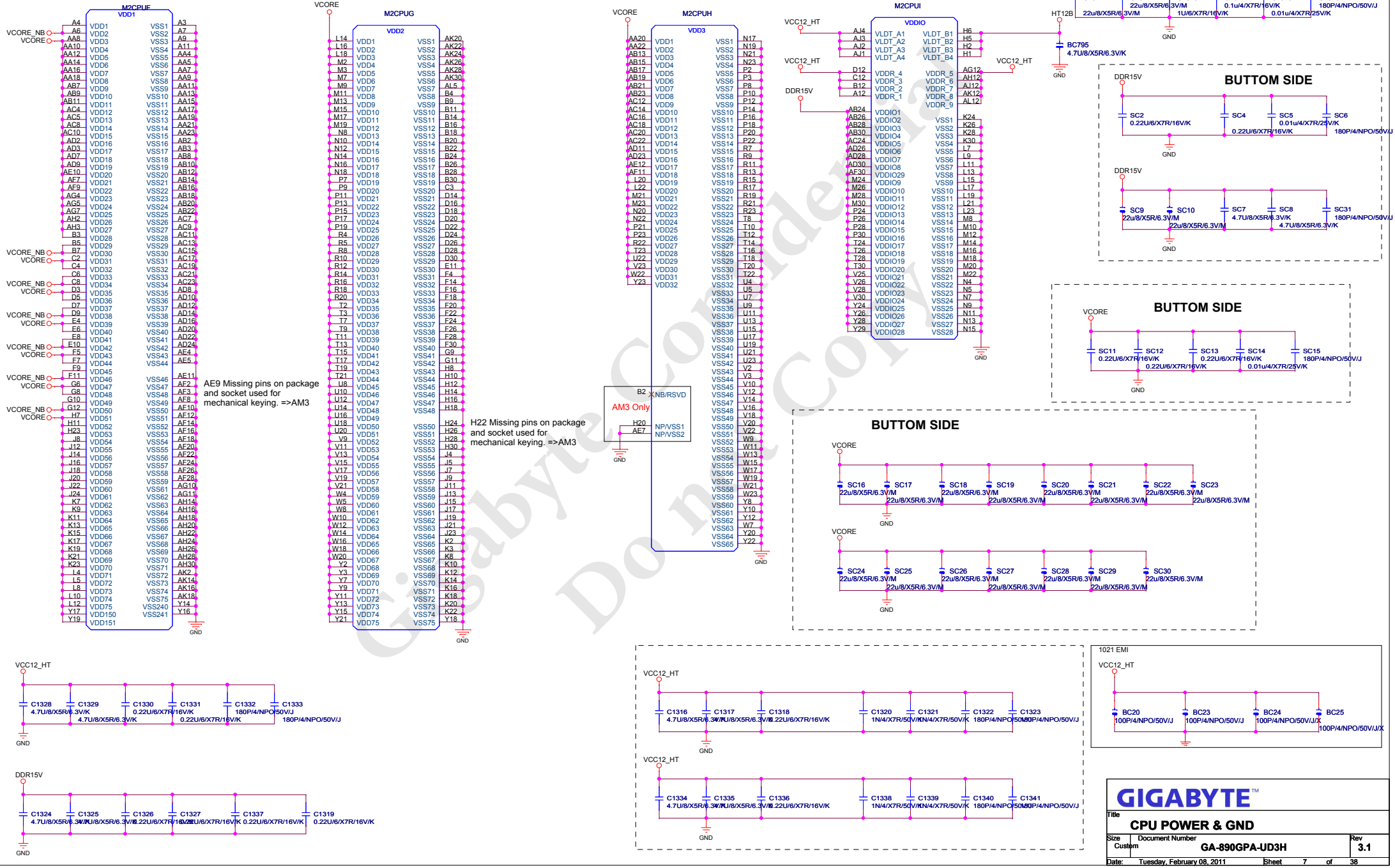


VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



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Title	CPU POWER & GND	
Size: Custom	Document Number: GA-890GPA-UD3H	Rev: 3.1
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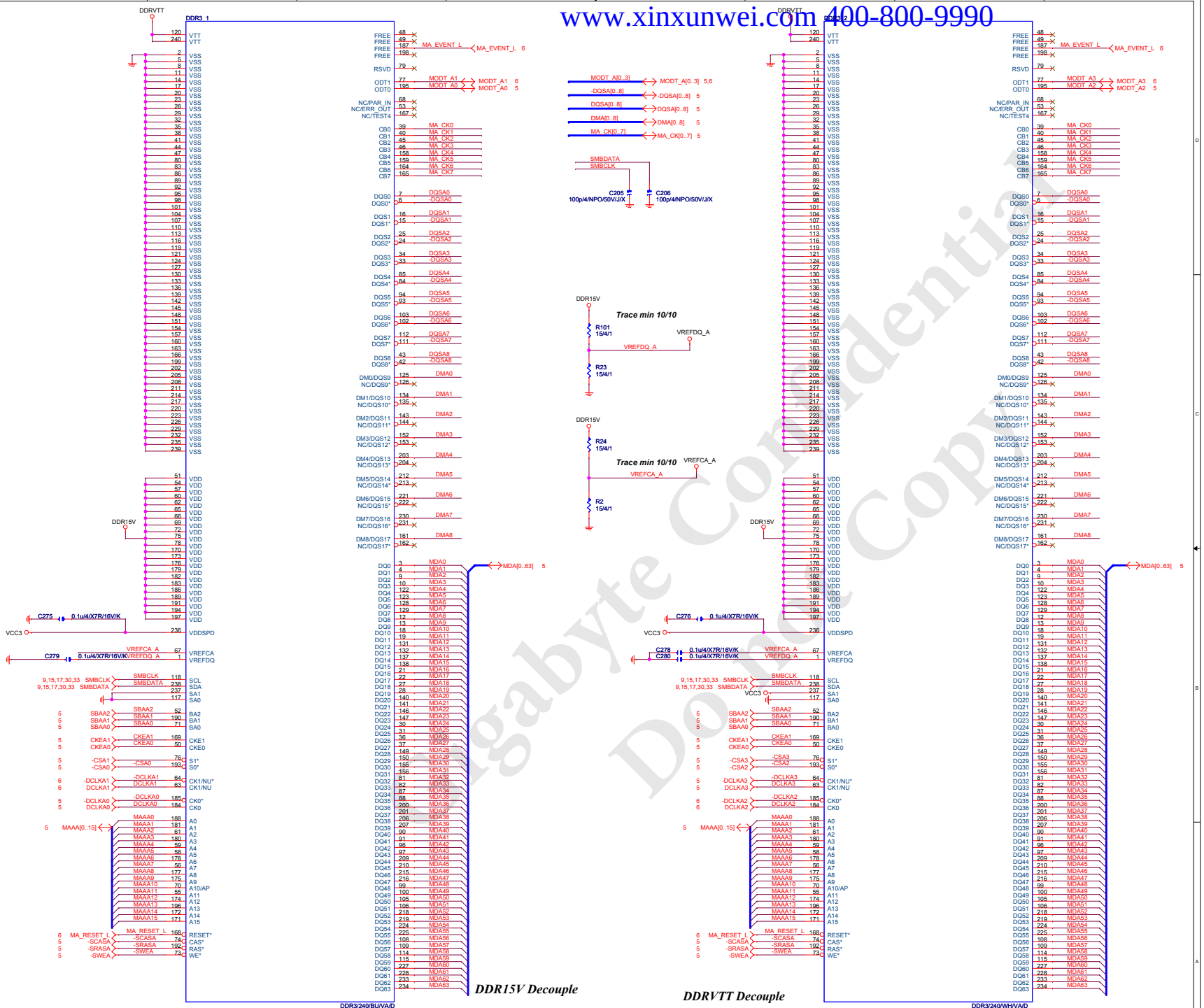

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Title	DDR III CHANNEL A	
Size: Custom	Document Number: GA-890GPA-UD3H	Rev: 3.1
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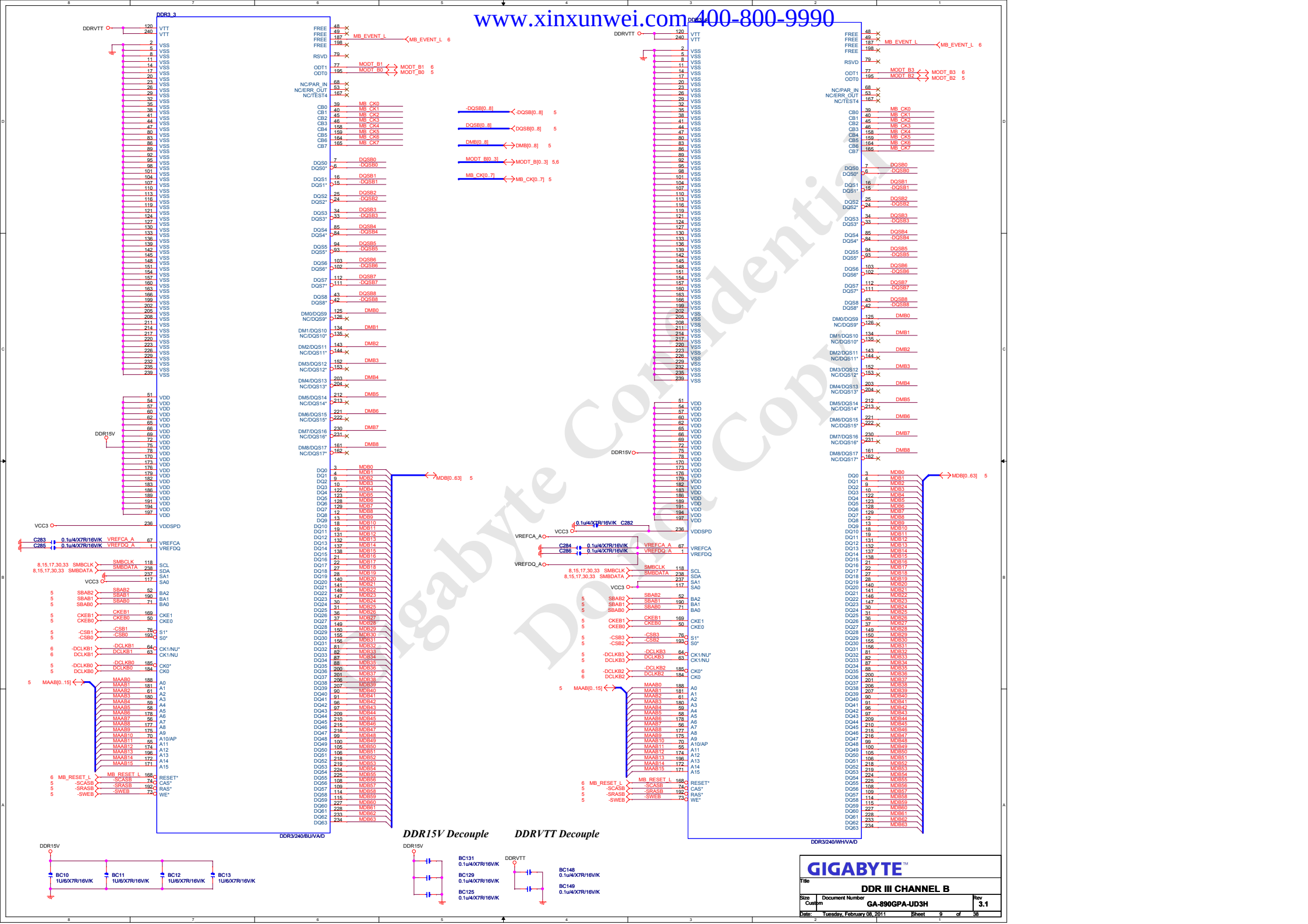

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Title	DDR III CHANNEL B		
Size: Custom	Document Number: GA-890GPA-UD3H		Rev: 3.1
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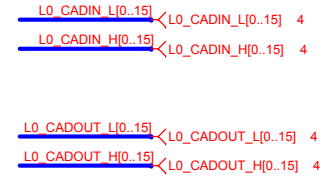

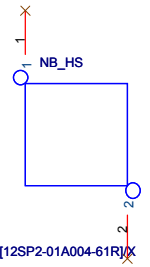

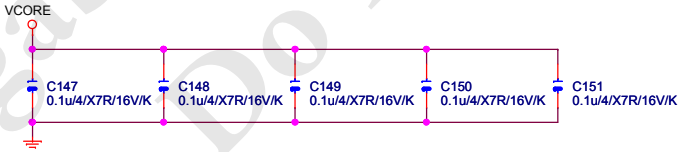

HT Link Stitching Caps

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Title: RS880 HT-LINK I/F

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Function	SEL
xI--> xOa	L (X8)
xI--> xOb	H (X16)

U3B

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

RS880D/FCBGA528/A11/[10HB1-10S880-20R]

PLACE CAP CLOSE TO CONNECTOR

U171

U172

U173

U174

ASM1440/TQFN42

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Title: RS880 PCIE I/F ,Switch

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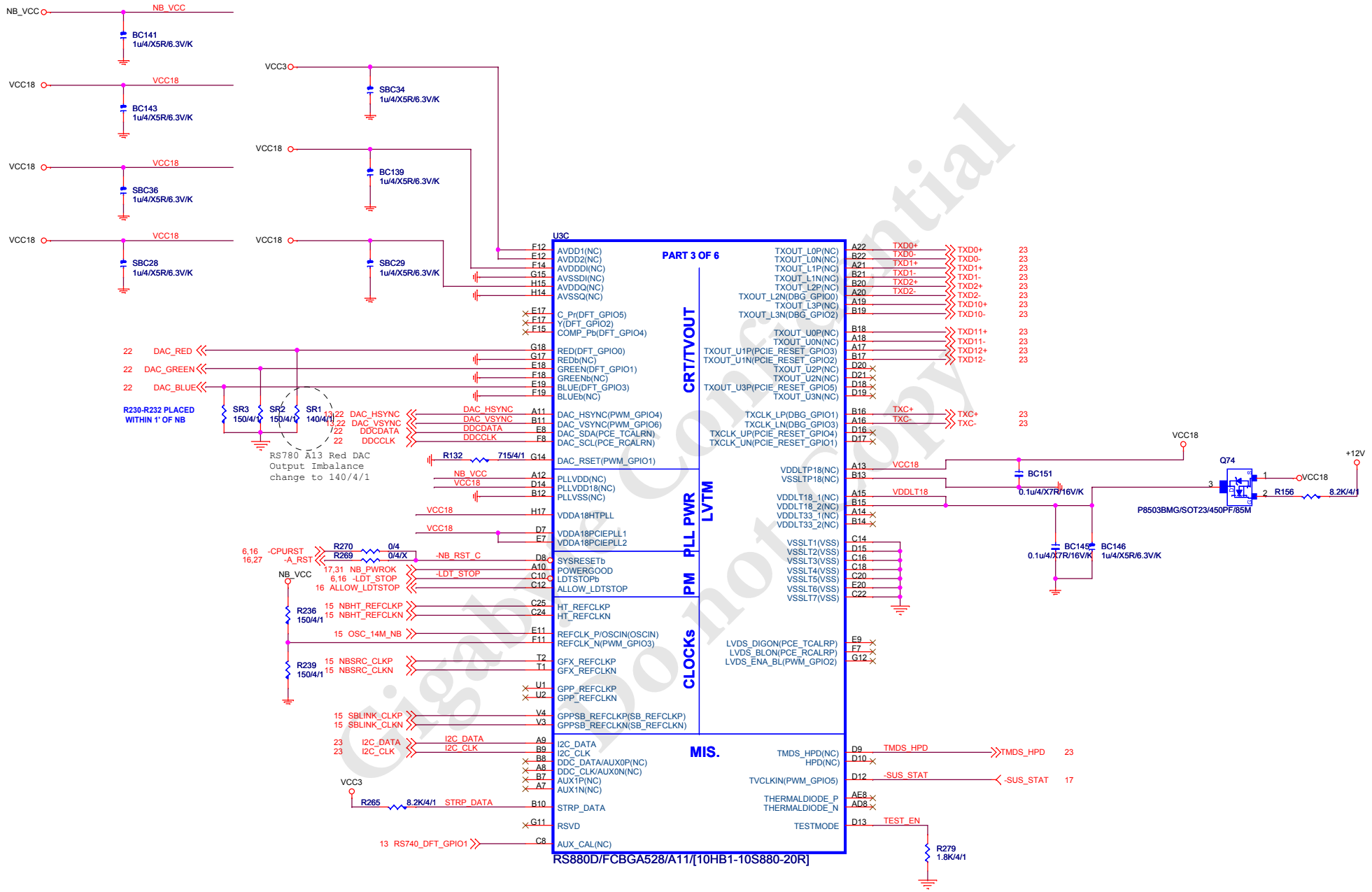

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Title: RS880 SYSTEM I/F			
Size: Custom	Document Number: GA-890GPA-UD3H		Rev: 3.1
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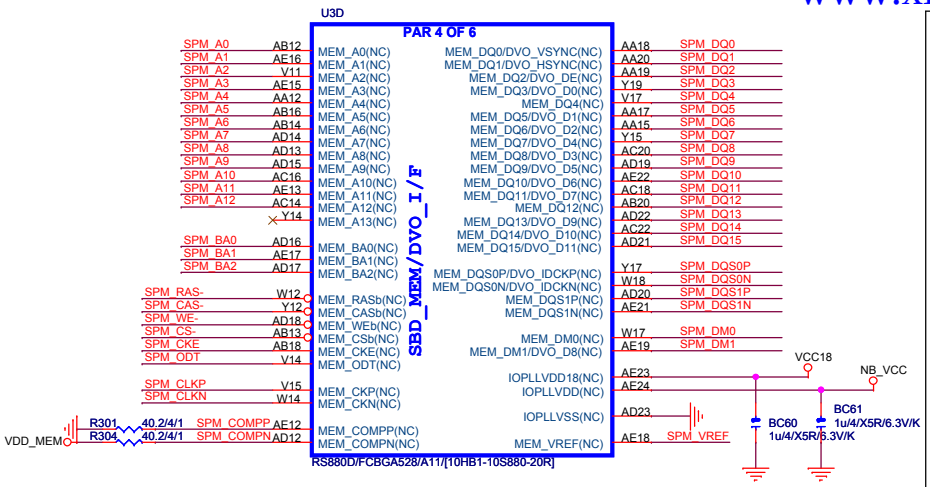

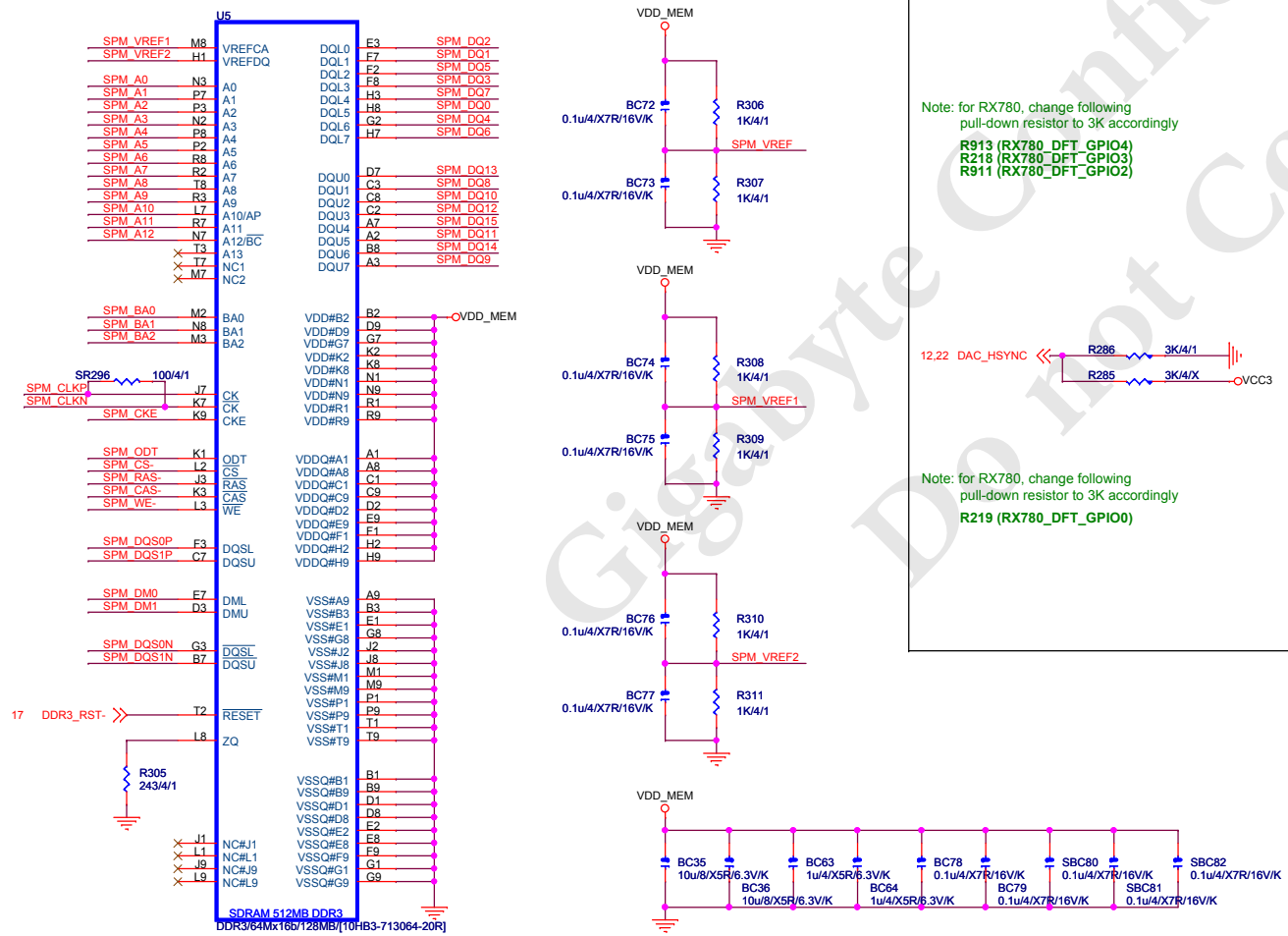

RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8

12 RS740_DFT_GPIO1 — R272 150/4/1

Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly

12,22 DAC_VSYNC — R276 3K/4/1 — VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly

R912 (RX780_DFT_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly

R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)

12,22 DAC_HSYNC — R286 3K/4/1, R285 3K/4/X — VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly

R219 (RX780_DFT_GPIO0)

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#
```

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

```
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable  (RS740/RS780); Disable(RX780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
```

RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])

```
These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E)   default
110: 4-0-0-0-0   Config A
101: 4-4-0-0-0   Config B
100: 4-2-2-0-0   Config C
011: 4-2-1-1-0   Config D
010: 4-1-1-1-1   Config E
others: register defined (default to Config E)
```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

```
111: 1-1-1-1-1-1   Mode L   default
110: 1-1-1-1-1-1   Mode L
101: 2-0-2-0-2-0   Mode C2
100: 2-0-2-0-1-1   Mode K
011: 2-0-1-1-1-1   Mode E
010: 1-1-1-1-1-1   Mode L
001: 4-0-0-0-1-1   Mode C
000: 4-0-0-0-2-0   Mode B
```

RS780: STRAP_PCIE_GPP_CFG[2:0] (configure thru register setting)

```
1-1-1-1-1-1   Mode L   default
1-1-1-1-1-1   Mode L
2-0-2-0-2-0   Mode C2
2-0-2-0-1-1   Mode K
2-0-1-1-1-1   Mode E
1-1-1-1-1-1   Mode L
4-0-0-0-1-1   Mode C
4-0-0-0-2-0   Mode B
```

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

```
Enables Side port memory
1.  Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740:  pin DFT_GPIO0
RS780:  pin HSYNC
RX780:  Not Appicable
```

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

```
Enables Test debug bus
using PCIE bus
1.  Disable (can be enabled
     thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register
                setting only
RS740: Not supported
```


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Title	RS880 STRAPS ,SPMEM	
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RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

U3F — PART 6/6 — GROUND — RS880D/FCBGA528/A11/[10HB1-10S880-20R]

Please use 1mm pad size, place all ELT test pads on bottom side only

U3E — PART 5/6 — POWER — RS880D/FCBGA528/A11/[10HB1-10S880-20R]

Title	RS880 POWER & GND
Size	Custom
Document Number	GA-890GPA-UD3H
Rev	3.1
Date:	Tuesday, February 08, 2011
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NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

VCC3 BC59 10u/8/X5R/6.3V/K BC892 1U/6/X7R/16V/K BC893 BC894 BC895 BC896 BC897 BC898 BC899 BC900 0.1u/4/X7R/16V/K

1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair

U185A

VDDA 44, GNDA 43, VDDREF 60, GNDREF 61, VDDSATA 39, GNDSATA 42, VDD48 64, GND48 3, VDDCPU 48, GNDCPU 47, VDDHTT 56, GNDHTT 53, VDDATIG 34, VDDSRC1 11, VDDSRC2 16, VDDSB_SRC 25, GNDATIG1 28, GNDATIG2 33, GNDSRC1 10, GNDSRC2 17, GNDSB_SRC 24, X1 62, X2 63, RESTORE# 52, SMBCLK 4, SMBDAT 5, PD# 51, REF0/SEL_HTT66 59, REF1/SEL_SATA 58, REF2 57

CPUKG0T_LPRS 50 → CPUCLK0_H 6
CPUKG0C_LPRS 49 → CPUCLK0_L 6
CPUKG1T_LPRS 46
CPUKG1C_LPRS 45
ATIG0T_LPRS 38
ATIG0C_LPRS 37
ATIG1T_LPRS 36 → NBSRC_CLKP 12
ATIG1C_LPRS 35 → NBSRC_CLKN 12
ATIG2T_LPRS 32 → SRCCLK_3GIO_A 20
ATIG2C_LPRS 31 → -SRCCLK_3GIO_A 20
ATIG3T_LPRS 30 → SRCCLK_3GIO_B 36
ATIG3C_LPRS 29 → -SRCCLK_3GIO_B 36
SB_SRC0T_LPRS 27 → USB3_CLK 37
SB_SRC0C_LPRS 26 → -USB3_CLK 37
SB_SRC1T_LPRS 23 → PCIE2_CLK 36
SB_SRC1C_LPRS 22 → -PCIE2_CLK 36
SRC0T_LPRS 21 → PCIE3_CLK 36
SRC0C_LPRS 20 → -PCIE3_CLK 36
SRC1T_LPRS 19 → PCIE1_CLK 20
SRC1C_LPRS 18 → -PCIE1_CLK 20
SRC2T_LPRS 15 → SRCCLK_LAN 34
SRC2C_LPRS 14 → -SRCCLK_LAN 34
SRC3T_LPRS 13 → SBSRC_CLKP 16
SRC3C_LPRS 12 → SBSRC_CLKN 16
SRC4T_LPRS 9 → SBLINK_CLKP 12
SRC4C_LPRS 8 → SBLINK_CLKN 12
SRC5T_LPRS 7 CLK_T1
SRC5C_LPRS 6 CLK_T0
SRC6T/SATAT_LPRS 41 → J363CLKP 38
SRC6C/SATAC_LPRS 40 → J363CLKN 38
HTT0T/66M_LPRS 55 → NBHT_REFCLKP 12
HTT0C/66M_LPRS 54 → NBHT_REFCLKN 12
48MHz_0 2 SIO_CLOCK_R → LPC48 27
48MHz_1 1 48M_USB_R → USB48M 17

Parallel Resonance Crystal

C1750 22p/4/NPO/50V/J
X7 14.318M/16p/20ppm/49US/40/D
C1751 22p/4/NPO/50V/J

watch dog -- RESTORE# 接 RESET

29,31 RESET → R2488 10/4

8,9,17,30,33 SMBCLK
8,9,17,30,33 SMBDATA

R2494 1K/4/1
R2501 8.2K/4/1
R2496 8.2K/4/1
R2503 158/4/1

12 OSC_14M_NB

R2505 90.9/4/1

R2492 33/4
R2493 33/4
R134 8.2K/4/1
R137 8.2K/4/1/X

Pin1: High=>DOC input, Low=>SRC5

VCC3

27 CLK_T0 → CLK_T0 R138 8.2K/4/1
27 CLK_T1 → CLK_T1 R139 8.2K/4/1

RTM880N-793/S

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

U185B

65 eGND65 THERMAL GND

RTM880N-793/S

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

GIGABYTE™

Title: ICS9LPRS477

Size: Custom | Document Number: GA-890GPA-UD3H | Rev: 3.1

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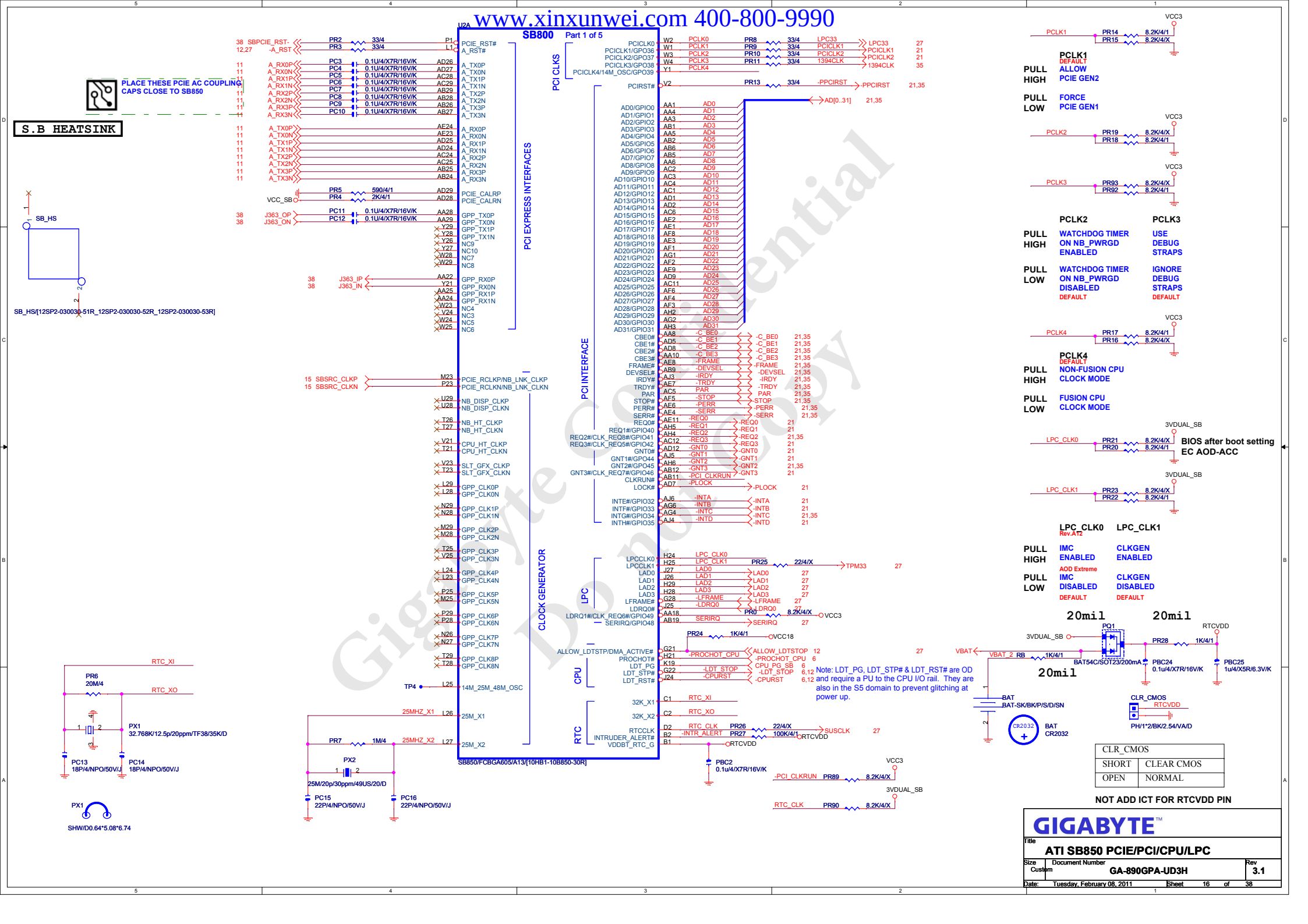


CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

GIGABYTE™

Title: ATI SB850 PCIE/PCI/CPU/LPC

Size	Document Number	Rev
Custom	GA-890GPA-UD3H	3.1

Date: Tuesday, February 08, 2011 Sheet 16 of 38

USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

either HWM inputs or PWR_GD signals can be used for power-up sequencer

IMC_GPIO200 IMC_GPIO199

ROM TYPE:

H, H = Reserved

H, L = SPI ROM DEFAULT

L, H = LPC ROM

L, L = FWH ROM

AZ_SDOUT

PULL HIGH LOW POWER MODE

PULL LOW PERFORMANCE MODE DEFAULT

Low: Disable PCI MEM boot(D),
Up: Enable PCI MEM boot

SB800 Part 4 of 5

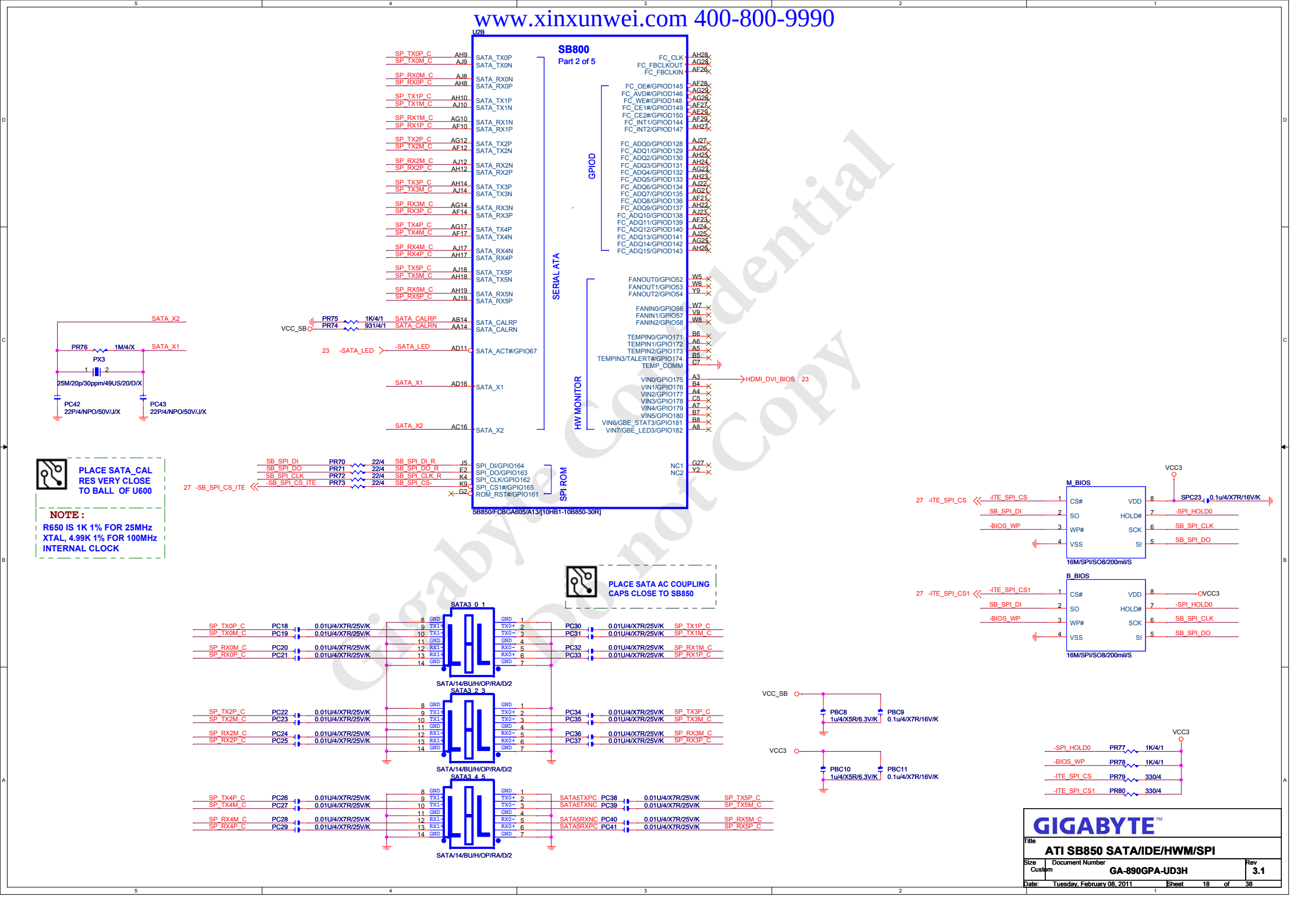
SB850/FCBGA605/A13/[10HB1-10B850-30R]

GIGABYTE™

Title: ATI SB850 ACPI/USB/GPIO/AUDIO

Size: Custom | Document Number: GA-890GPA-UD3H | Rev: 3.1

Date: Tuesday, February 08, 2011 | Sheet 17 of 38



GIGABYTE™

Title	ATI SB850 SATA/IDE/HWM/SPI	
Size: Custom	Document Number: GA-890GPA-UD3H	Rev: 3.1
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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

U2C

SB800

Part 3 of 5

POWER

SB850/FCBGA605/A13/[10HB1-10B850-30R]

U2E

SB800

GROUND

Part 5 of 5

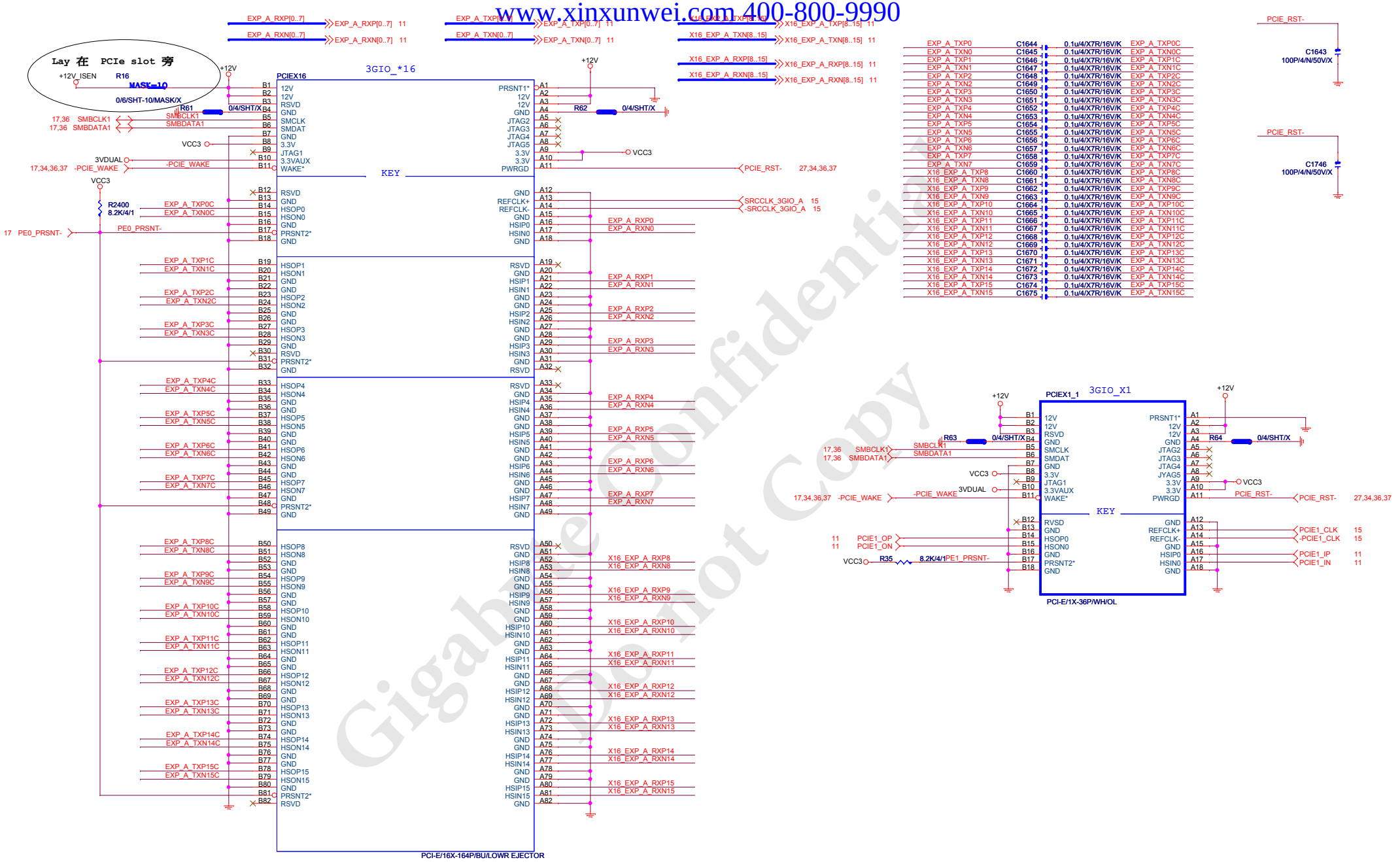
SB850/FCBGA605/A13/[10HB1-10B850-30R]

GIGABYTE™

Title: ATI SB850 POWER & GND

Size: Custom | Document Number: GA-890GPA-UD3H | Rev: 3.1

Date: Tuesday, February 08, 2011 | Sheet 19 of 38



GIGABYTE™

Title: PCI EXPRESS X 16 ,X1

Size	Document Number	Rev
Custom	GA-890GPA-UD3H	3.1

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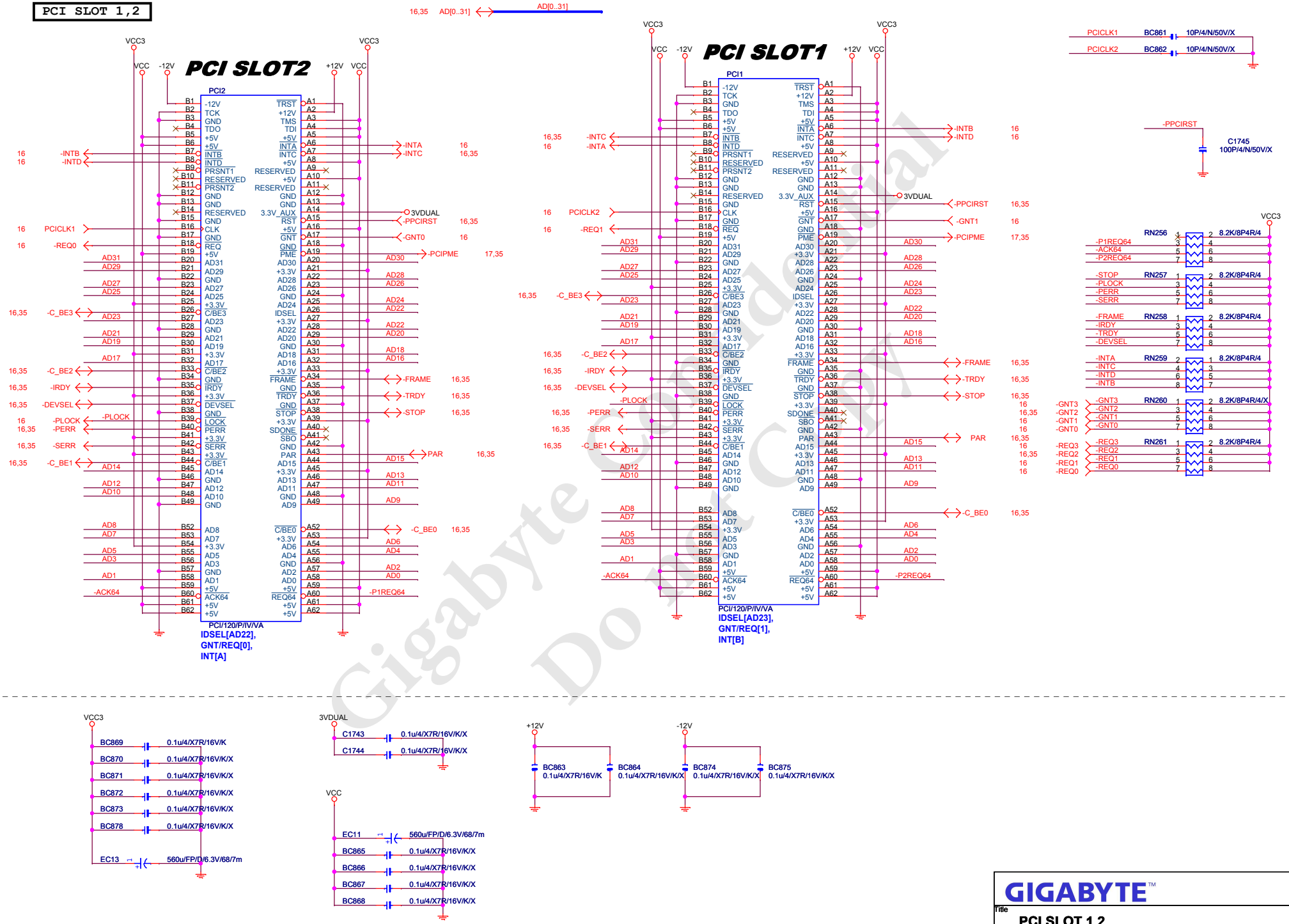
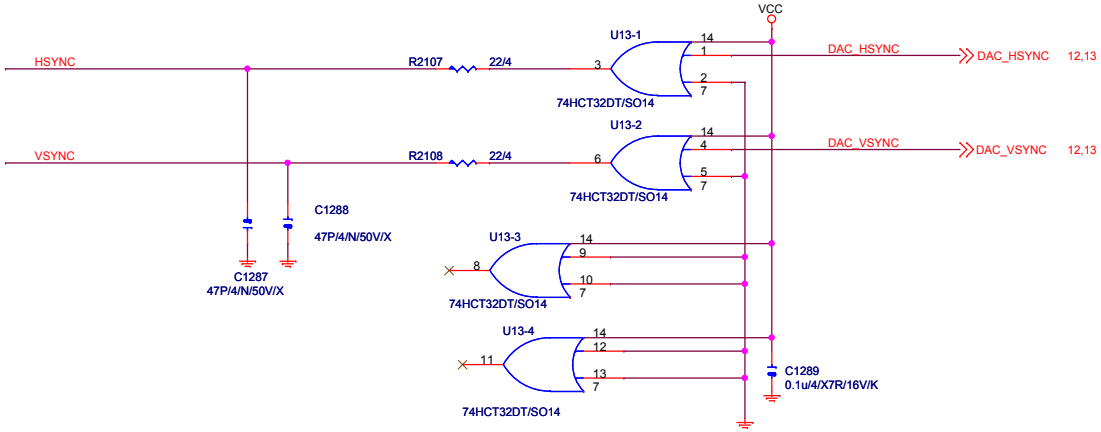
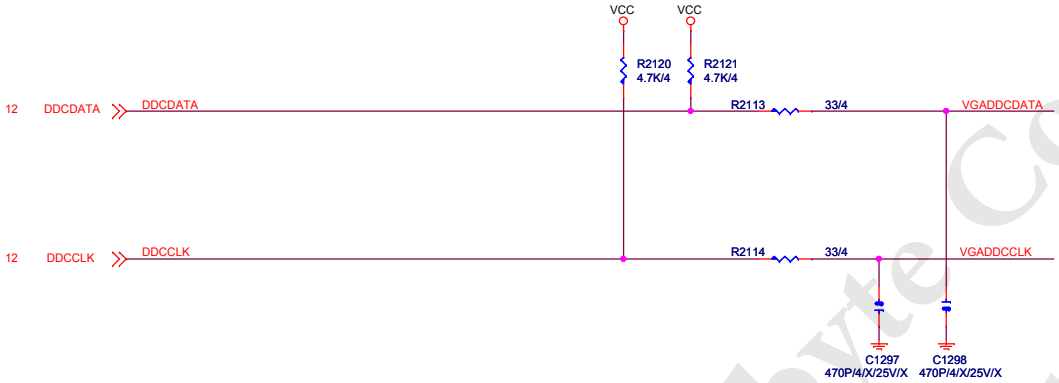
PCI SLOT 1,2

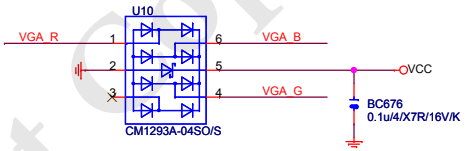


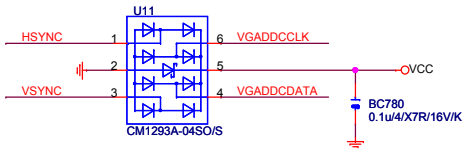
GIGABYTE™

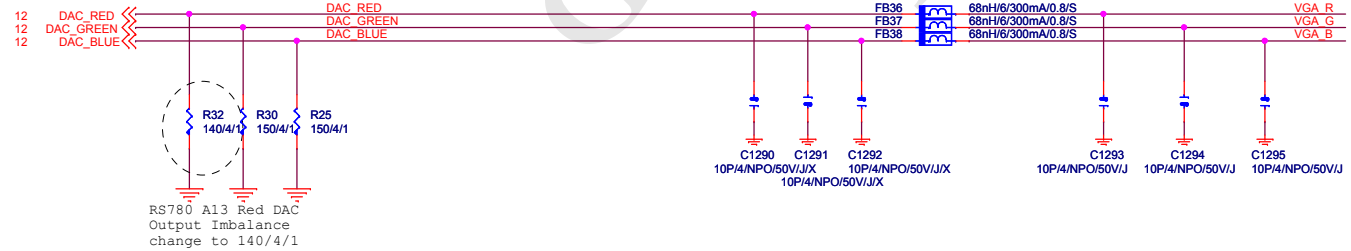
Title	PCI SLOT 1,2	
Size: Custom	Document Number: GA-890GPA-UD3H	Rev: 3.1
Date: Tuesday, February 08, 2011	Sheet 21 of 38	

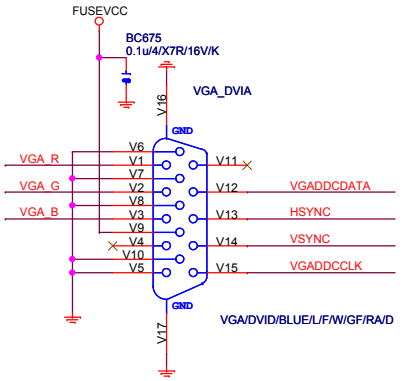






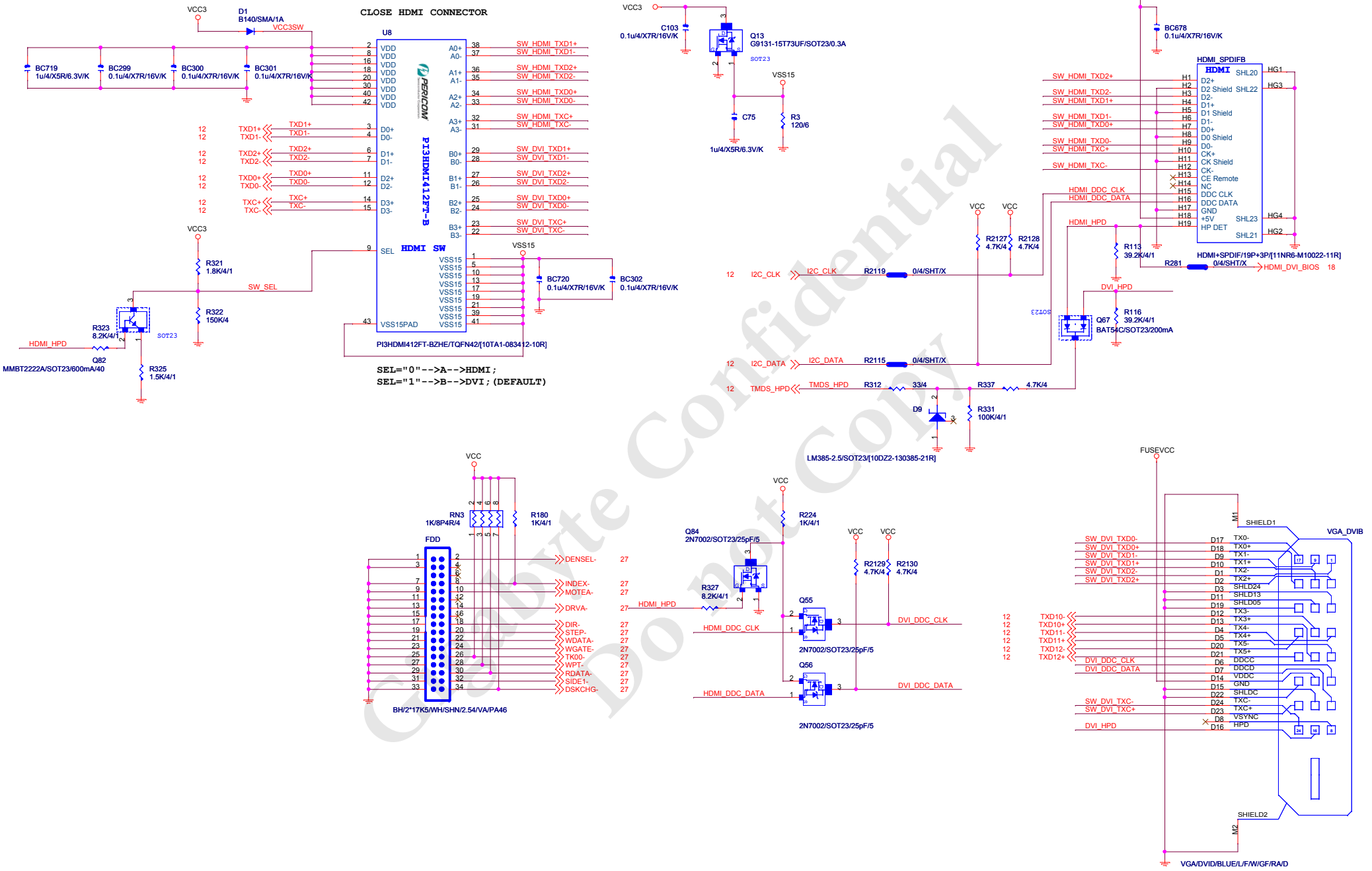






GIGABYTE™

Title: RGB		
Size: Custom	Document Number: GA-890GPA-UD3H	Rev: 3.1
Date: Tuesday, February 08, 2011	Sheet 22 of 38	



FRONT SIDE USB3

FRONT SIDE USB4

FRONT SIDE USB2

FRONT SIDE USB1

i_Phone charger circuit

DEFAULT H, STABYBY POWER

USB connector

Chipset

Title	COM/F_USB/I_PWR
Size	C
Document Number	GA-890GPA-UD3H
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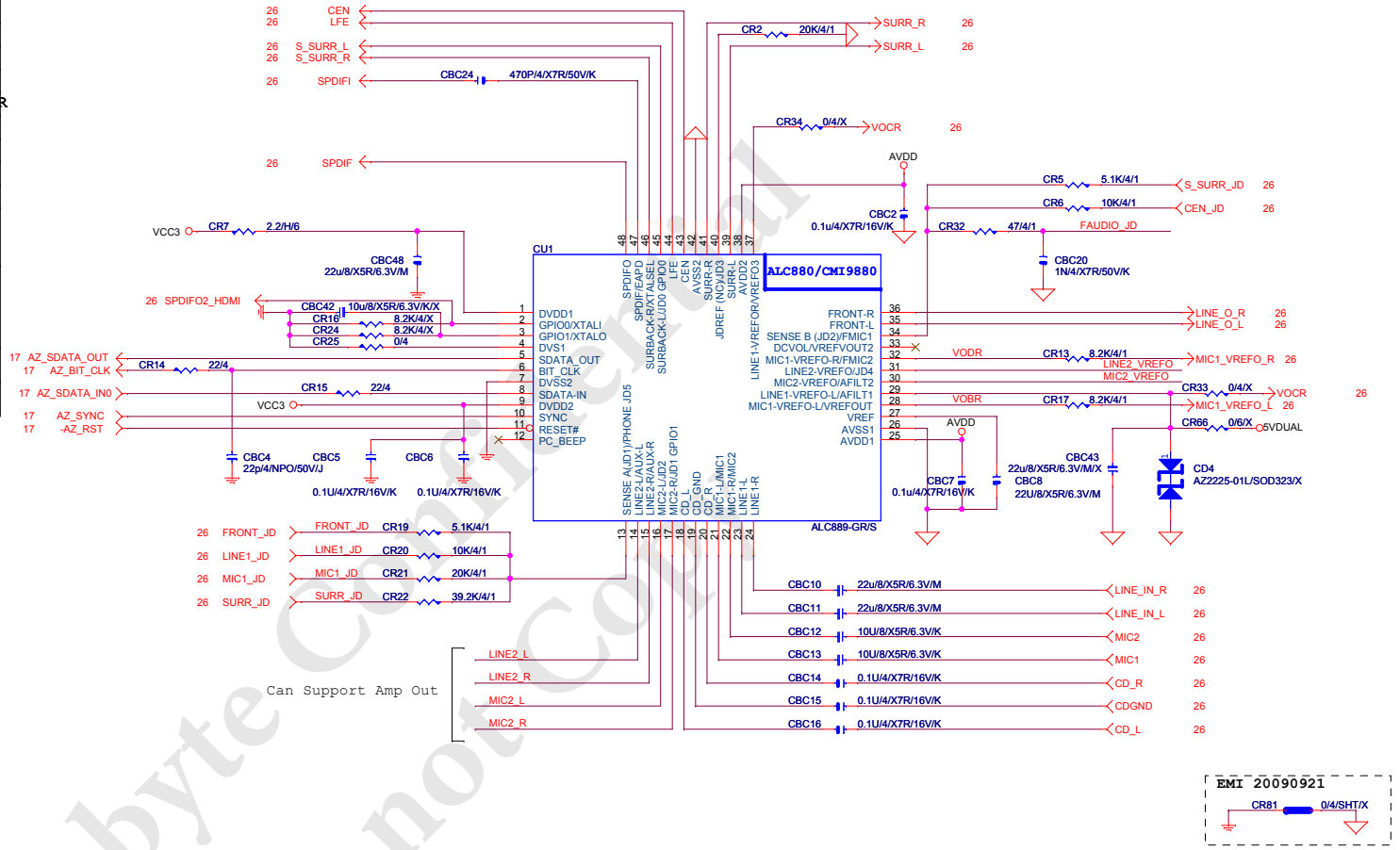
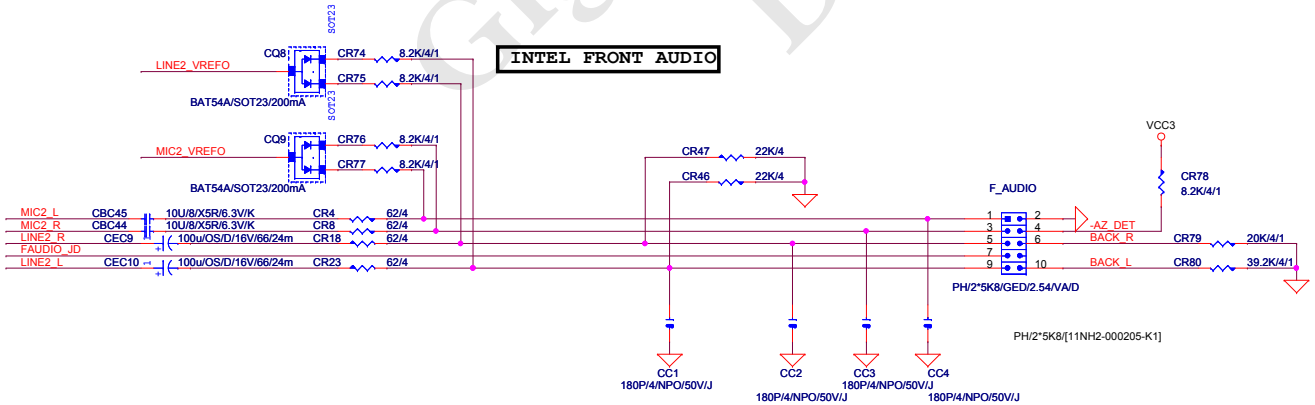
AZALIA CODEC *ALC892R/ALC889/ Colay*

	ALC892R	ALC889	ALC889A	ALC888	ALC892
CR16	X	X	O	X	X
CR24	X	X	O	X	X
CR25	X	O	O	O	X
CBC42	10uF/X5R	X	X	X	10uF/X5R
CR2	20K/1%	20K/1%	20K/0.1%	20K/1%	20K/1%
CR9	O	O	X	X	O
CR10	X	X	O	O	X
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R	4.7uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm	75 ohm	75 ohm
CR33/CD1/CD2/CD3/CQ4/ CBC25	O	O	O	O	X
CR34/CR66/CBC43/CD4	X	X	X	X	O





GIGABYTE™

Title: ALC889 CODEC

Size: Custom | Document Number: GA-890GPA-UD3H | Rev: 3.1

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CR26 0/4/SHT/X

AVDD +12V

CQ4 78L05/SOT89/0.1A

CD1 CD4148WP/1206/300mA

5VDUAL

CD2 CD4148WP/1206/300mA

CBC47 22u/8/X5R/6.3V/M

CD3 AZ2225-01L/SOD323

CBC25 1U/6/X7R/16V/K

For ESD PROTECT DIODE

SPDIF

25 SPDIF CR10 0/4/X

25 SPDIFO2_HDMI CR9 0/4

CBC34 100p/4/NPO/50V/J

For HDMI SPDIF

SPDIF_OUT

PH/1*2/BK/2.54/VA/D

25 SPDIFI VCC CR3 0/4

SPDIF_IN

CR35 75/4/1

SHR/1*3/WH/P/2.54/VA/D

FUSEVCC

25 SPDIF

S1 S2 S3 G1 G2 G3 G4

HDMI_SPDIFC

HDMI+SPDIF/19P+3P/[11NR6-M10022-11R]

CD IN

CD_IN

25 CD_L

25 CDGND

25 CD_R

SHR/1*4/BK/P/2.54/VA/D

CR51 8.2K/4/1

CR52 8.2K/4/1

CR53 8.2K/4/1

For Audio precision test

CBC19 0.01u/4/X7R/25V/K

USB_1394_ESATA

USB_LAN

AUDIOB

25 LINE1_JD LINE1_JD AJ_A5 AJ_A2

25 FRONT_JD FRONT_JD AJ_B5 AJ_B2

25 MIC1_JD MIC1_JD AJ_C5 AJ_C2

LINE-IN LINE-OUT MIC-IN

BLUE LINE-IN

GREEN LINE-OUT

PINK MIC-IN

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

A3RJ/13P/B/[11NR6-403006-01_11NR6-403006-02]

3RJ+15F/[11NR6-403004-11]

AUDIOA

25 CEN_JD CEN_JD BJ_B5 BJ_B2

25 SURR_JD SURR_JD BJ_C5 BJ_C2

25 S_SURR_JD S_SURR_JD BJ_A5 BJ_A2

REAR CEN SIDE

Orange CEN/LFE

ALC880 - SURROUND

CMI9880 - Back SURR

Black Back side Speaker Azalia Port G

Gray Left & Right Side Speaker

CMI9880 - Side SURR

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

A3RJ/13P/OBG/[11NR6-403006-71]

3RJ+15F/[11NR6-403004-31]

LINE OUT FRONT OUT

25 LINE_O_R CEC17 100u/OS/D/16V/66/24m CR59 62/4 AJ_B5

25 LINE_O_L CEC19 100u/OS/D/16V/66/24m CR60 62/4 AJ_B2

CR62 22K/4 CBC21 180P/4/NPO/50V/J CR63 22K/4 CBC22 180P/4/NPO/50V/J

LINE-IN

25 LINE_IN_R CR11 62/4 AJ_A5

25 LINE_IN_L CR12 62/4 AJ_A2

CQ1 SOT23

25 VOCR CR41 8.2K/4/1/X CR42 8.2K/4/1/X

BAT54A/SOT23/200mA/X

CBC26 180P/4/NPO/50V/J CBC27 180P/4/NPO/50V/J

Verify MIC function in LINE-in

MIC

25 MIC2 CR27 62/4 AJ_C5

25 MIC1 CR29 62/4 AJ_C2

25 MIC1_VREFO_R CR30 0/4/SHT/X

25 MIC1_VREFO_L CR31 0/4/SHT/X

CBC28 180P/4/NPO/50V/J CBC29 180P/4/NPO/50V/J

SURROUND

25 SURR_R CEC30 100u/OS/D/16V/66/24m CR43 62/4 BJ_C5

25 SURR_L CEC31 100u/OS/D/16V/66/24m CR44 62/4 BJ_C2

CR55 22K/4 CBC32 180P/4/NPO/50V/J CR56 22K/4 CBC33 180P/4/NPO/50V/J

CEN/LFE

25 LFE CEC34 10u/FP/S/10V/45/220m CR45 62/4 BJ_B5

25 CEN CEC35 10u/FP/S/10V/45/220m CR48 62/4 BJ_B2

CR57 22K/4 CBC36 180P/4/NPO/50V/J CR58 22K/4 CBC37 180P/4/NPO/50V/J

SURR BACK

25 S_SURR_R CEC38 10u/FP/S/10V/45/220m CR49 62/4 BJ_A5

25 S_SURR_L CEC39 10u/FP/S/10V/45/220m CR50 62/4 BJ_A2

CR61 22K/4 CBC40 180P/4/NPO/50V/J CR54 22K/4 CBC41 180P/4/NPO/50V/J

GIGABYTE™

Title: AUDIO JACK

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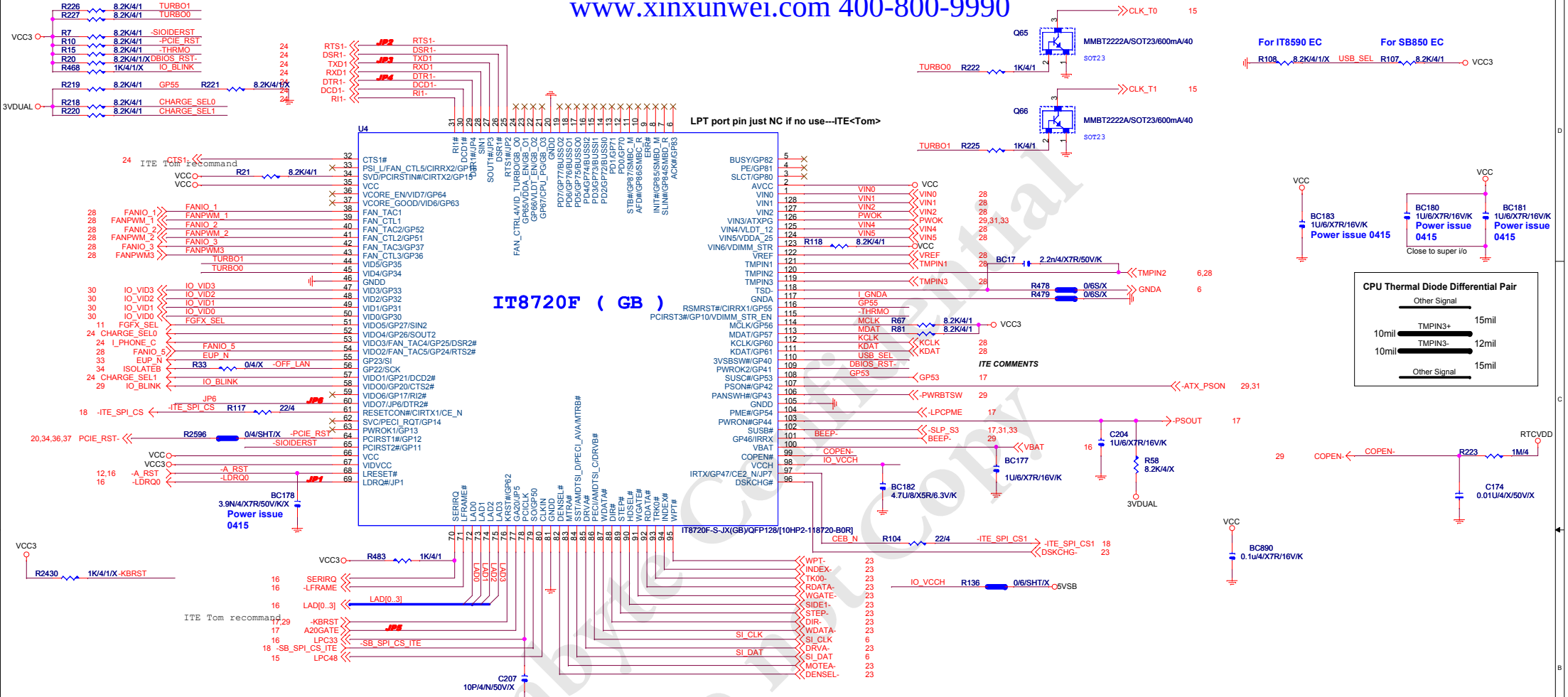

IT8720GB Power On Strapping Options

	Symbol	value	Description
JP1 Pin 69			
JP2 Pin 25	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 27	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 29	K8PWR_EN	1	K8 power sequence disabled
		0	K8 power sequence enabled
JP3 & JP5 Pin 27 & Pin 77	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5 Pin 77	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin 60	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function
JP7 Pin 97	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
		0	Disable Dual BIOS Function for GigaByte Only

Title	ITE 8720 LPC IO, TPM
Size	Custom
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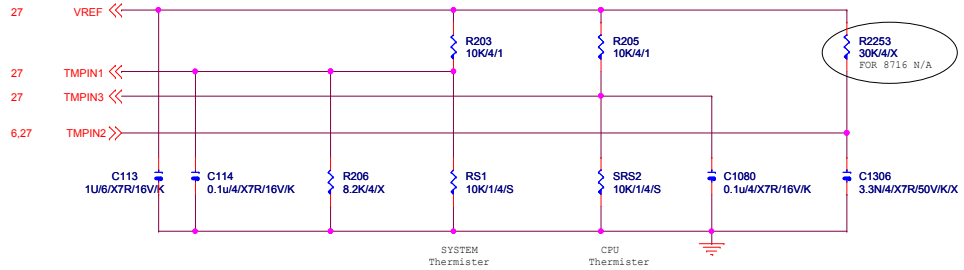
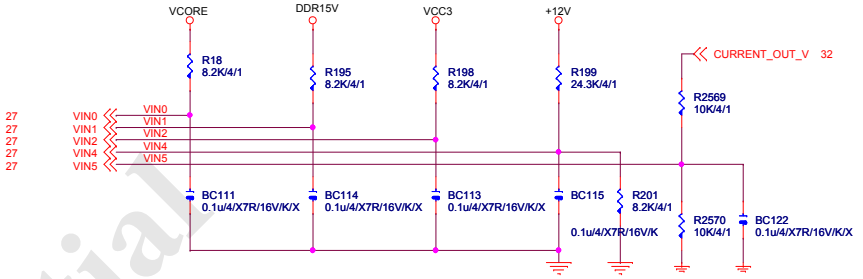
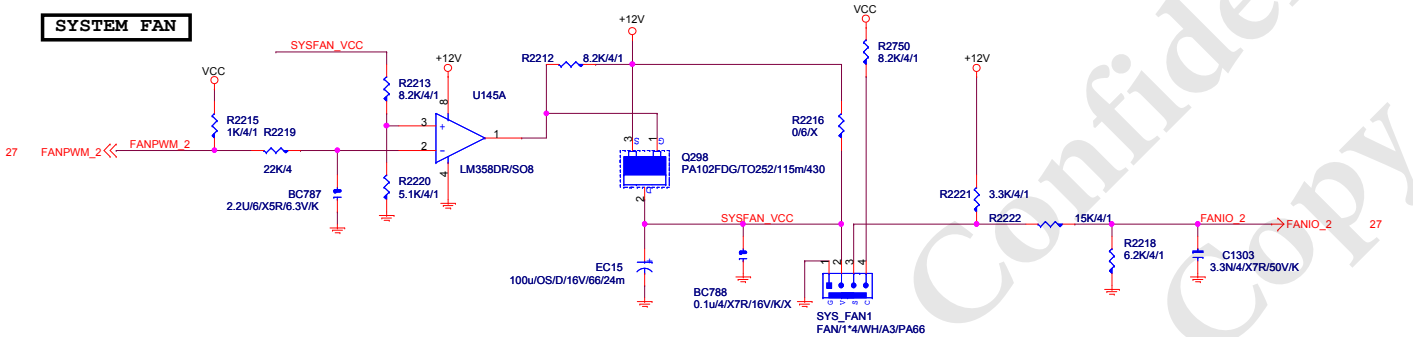
Hardware Monitor circuits

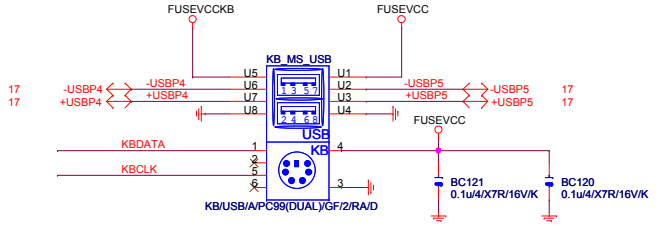


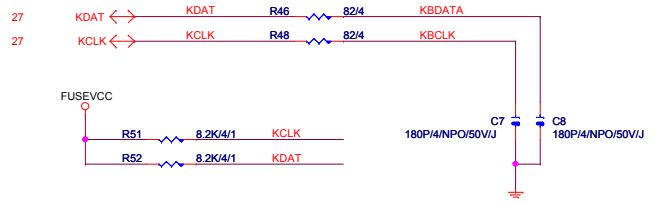


SYSTEM FAN

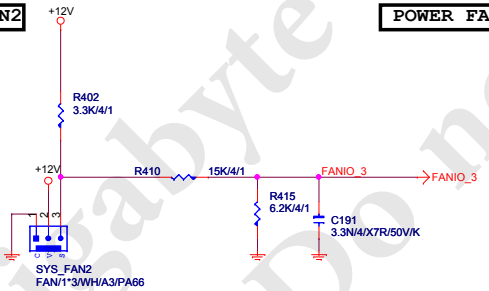


KB & USB

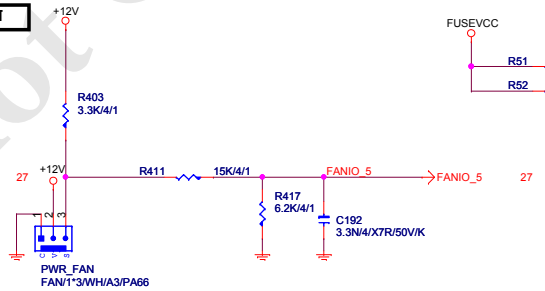


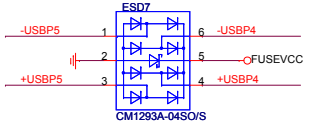


SYSTEM FAN2

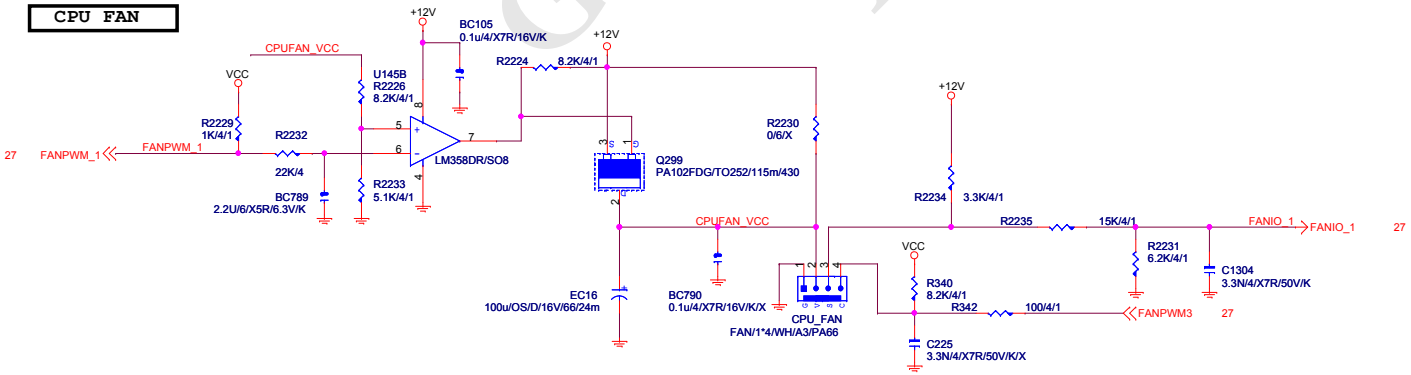


POWER FAN





CPU FAN



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Title: FAN/HWMO KB/USB

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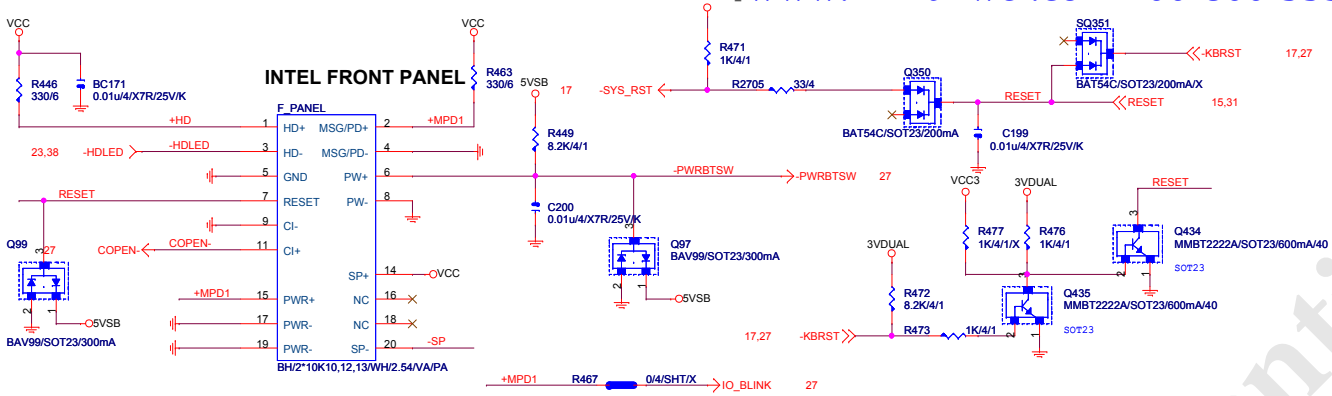
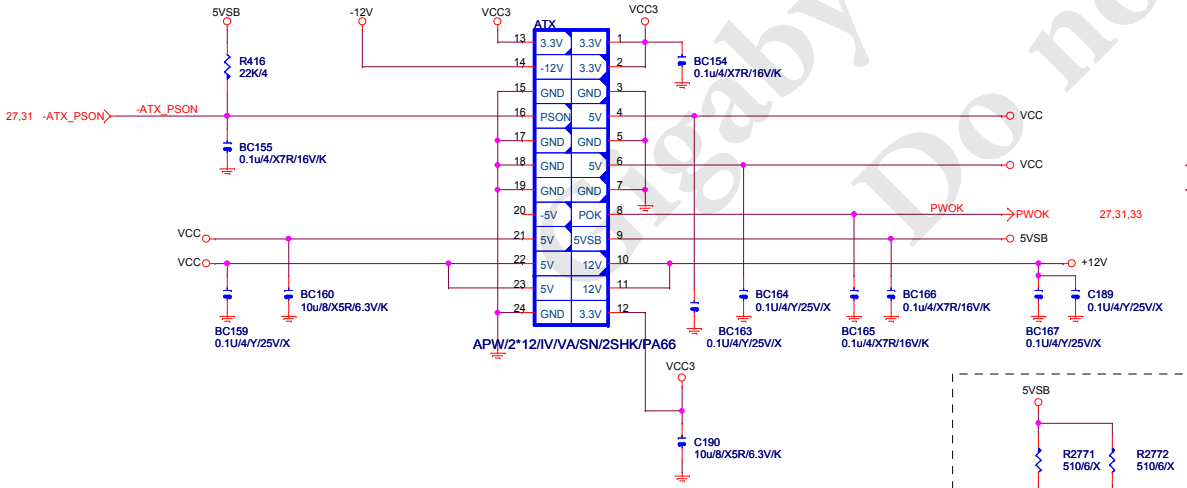
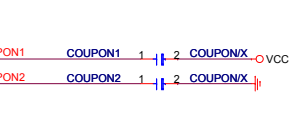
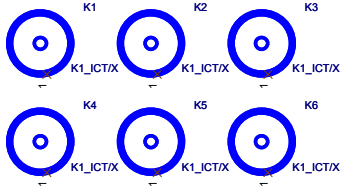
INTEL FRONT PANEL

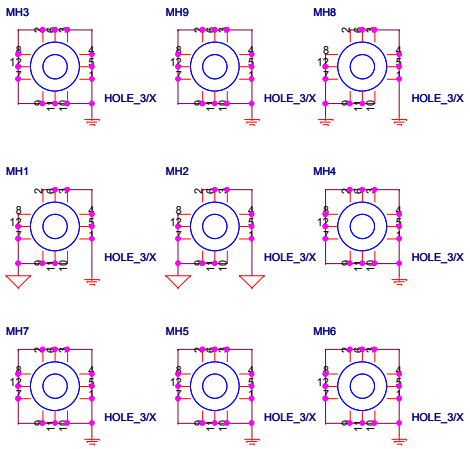


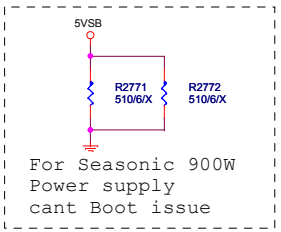
ATX POWER CONNECTOR











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Title: ATX, FRONT PANEL ,EC		
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AM2: high, AM2R2: low

ATX_12V

APW/2*4/IV/OC/P/4.2/VA/SN/OH

PWROK (SVI)
Low : "metal VID"
High : running protocol

EN rising edge :
Hi : PVI mode
Low : SVI mode

Pin 34 Input, Pin 37 Output

0.8V on

U1 ISL6324ACRA/QFN48

for 6324

for 6609

for 6609, DR67 0 ohm.

for 6609, DR78 0 ohm.

for 6609, DR101 0 ohm.

for 6609, DR115 0 ohm.

for 6609, DR124 0 ohm.

BOTTOM PAD CONNECT TO GND THROUGH 8 VIA

DRN8 1K/8P4R/4

DRN9 0/8P4R/4/SHT/X

DU3 ISL6609ACBZ/SO8

DU4 ISL6609ACBZ/SO8

DL3 DL4 DL5 DL6 0.6u/40A/IMD129/W/D

UPA2726/N/7m/PPAKSO8/[10IF9-092726-01R_10IF9-094744-01R_10IF9-074921-01R]

UPA2724/N/3.3m/PPAKSO8/[10IF9-042724-01R_10IF9-044835-01R_10IF9-034935-01R]

MOS_HS

MOS_HeatPipe/[12SP2-01A004-A1R_12SP2-01A004-A2R]

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Title: VCORE (PWM ISL6324A+6612A)

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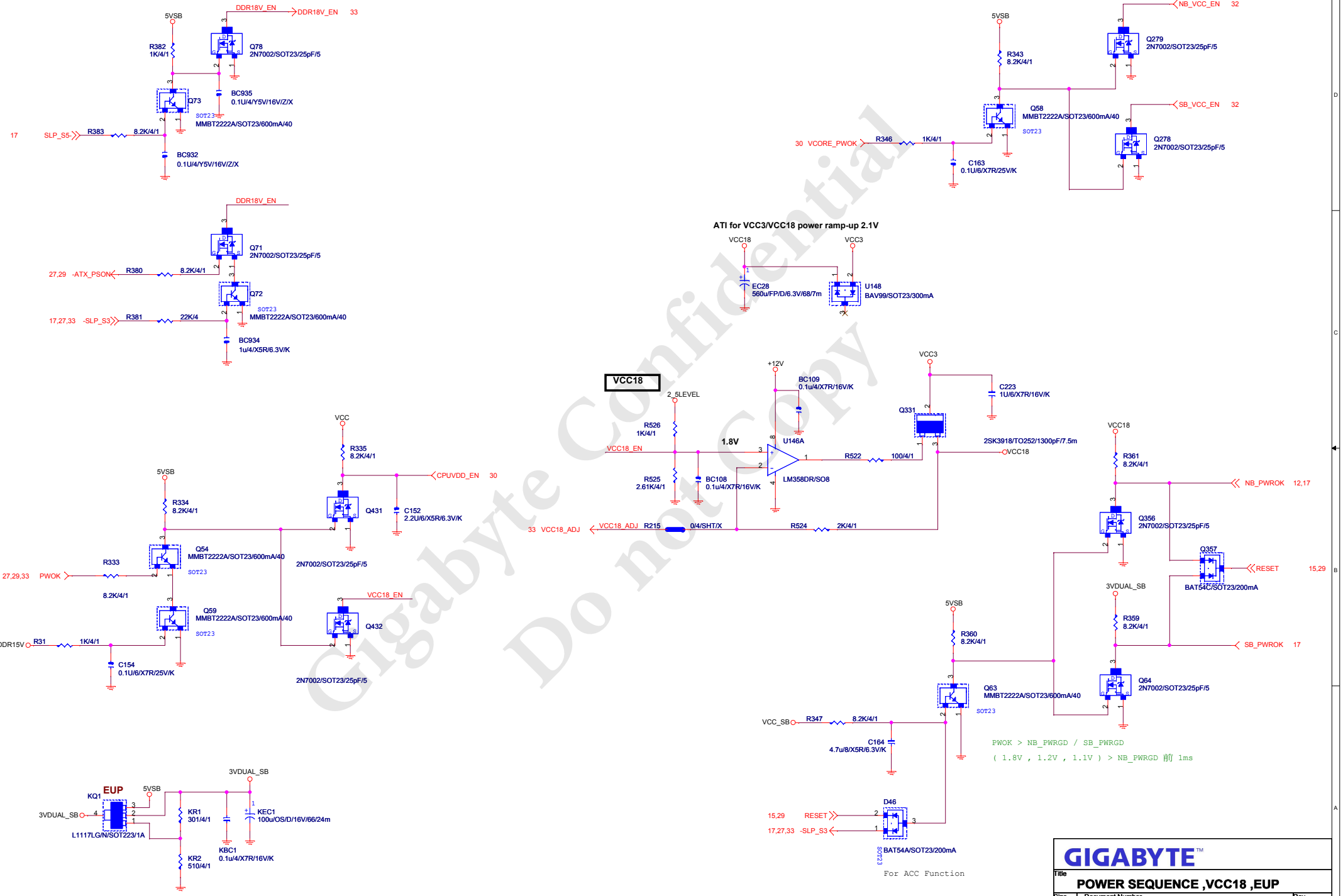

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Title	POWER SEQUENCE ,VCC18 ,EUP	
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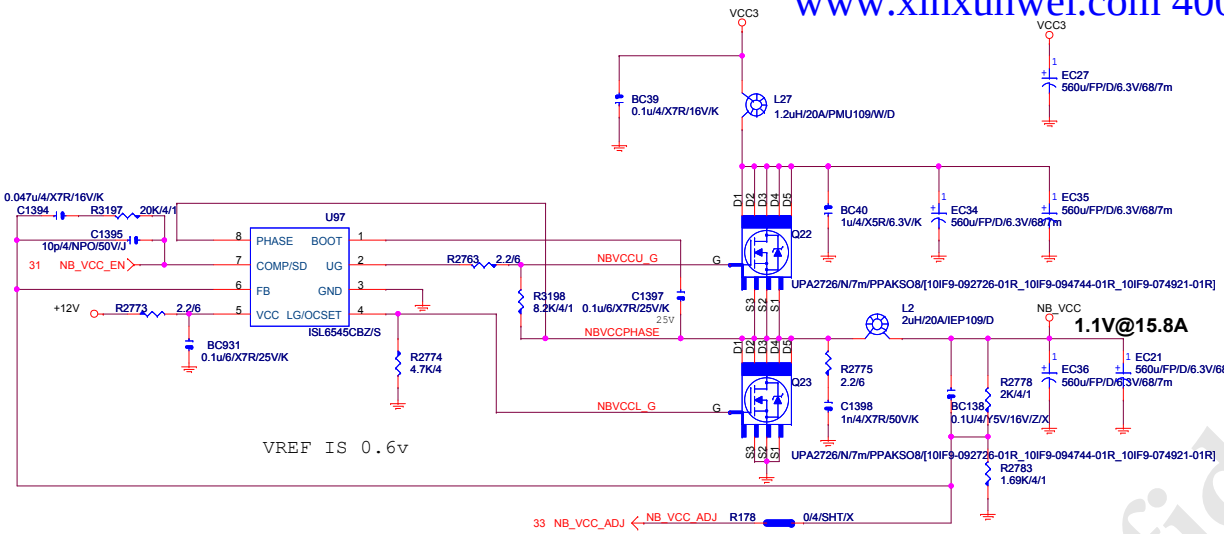
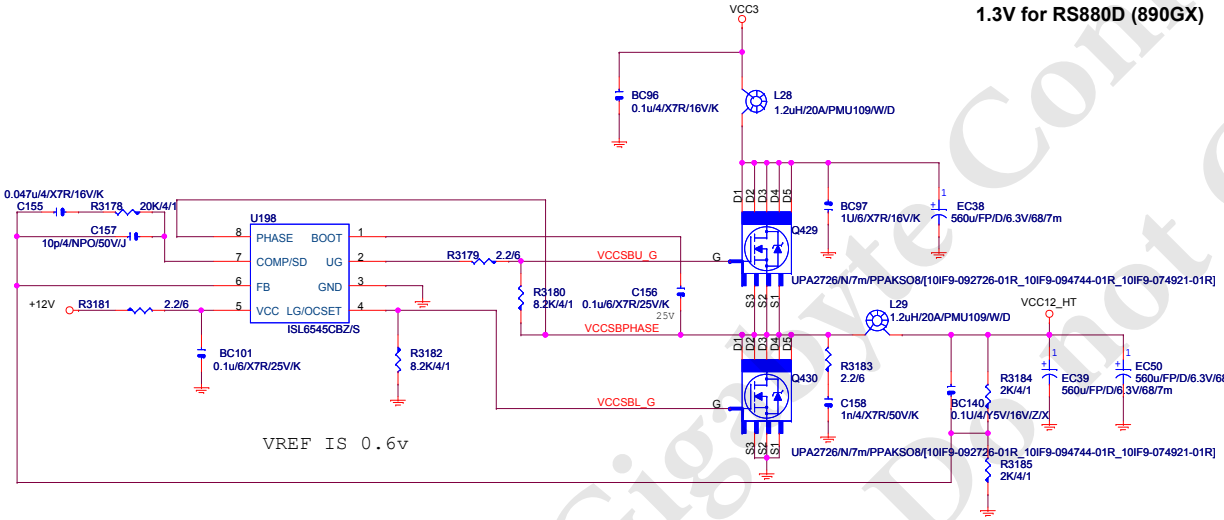
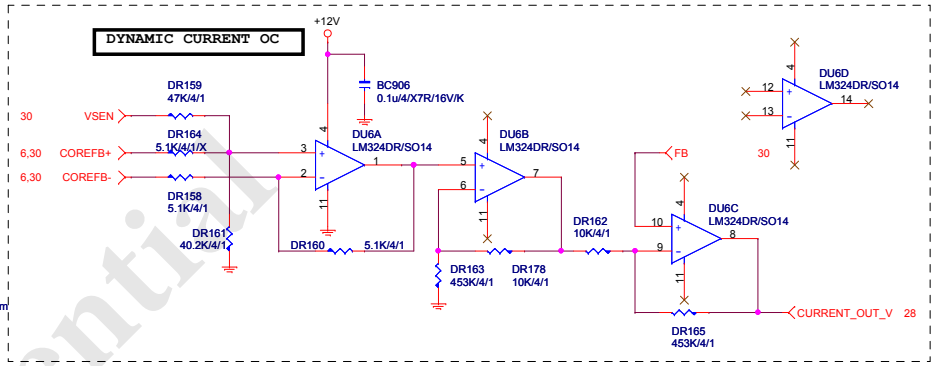


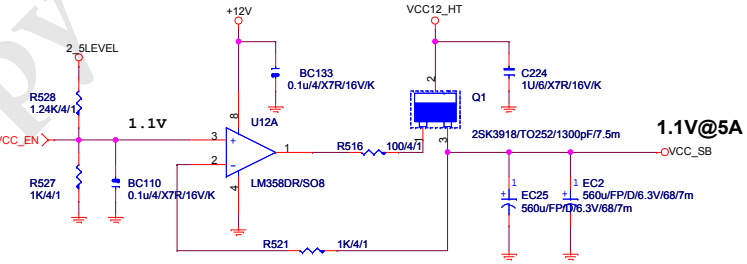
0.6*(1+2K/1.69K)=1.3V

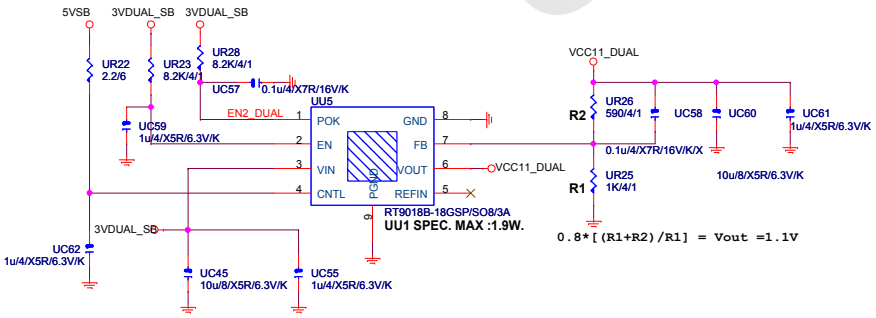
1.3V for RS880D (890GX)

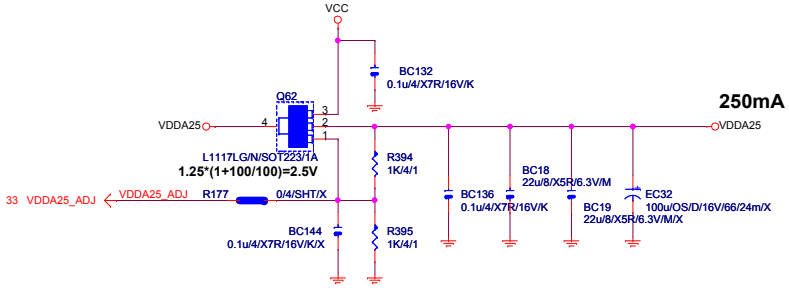


0.6*(1+2K/2K)=1.20V









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Title	NB/SB POWER,VCC12HT,VDDA25,VCC11Dual	
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R2038不能上,會導致LM324 PIN1不能完全拉Lo

5VDUAL

VCC R344 8.2K/4/1 → U9A KA393D/SO8 → R341 8.2K/4/1 → 2SK3918/TO252/1300pF/7.5m Q30 → 5VDUAL
R349 12.1K/4/1, C176 1U/6/X7R/16V/K
5VSB R351 10K/4/1, R339 10K/4/1, C172 1U/6/X7R/16V/K
+12V R345 8.2K/4/1 → U9B KA393D/SO8
R353 2.74K/4/1, C173 0.1u/6/X7R/25V/K
R2854 1K/4/1, R2853 8.2K/4/X P_GATE, Q31 P2003ED/P/TO252/30m
EC31 100u/OS/D/16V/66/24m, EC24 560u/FP/D/6.3V/68/7m
5VDUAL_GATE → R366 1K/4/1, Q35 MMBT2222A/SOT23/600mA/40, Q34 2N7002/SOT23/25pF/5, C180 1n/4/X7R/50V/K/X
17,27,31 -SLP_S3 → R350 8.2K/4/1

2_5LEVEL

R529 220/6, Q96 AP431N/SOT23/150mA, EC33 100u/OS/D/16V/66/24m
9.5V / 25A protect
9.5*(1.21K/(13.3K+1.21K))=0.792V

+12V BC106 0.1u/4/X7R/16V/K
R513 133K/4/1, 0.8V, U147A LM358DR/SO8, R509 1K/4/1
R512 63.4K/4/1, R530 13.3K/4/1, R519 1.21K/4/1, C264 1n/4/X7R/50V/K/X
+12V_ISEN
5VSB R511 8.2K/4/X, THERMTRIP_CPU_L → THERMTRIP_CPU_L 6,17
Q92 2N7002/SOT23/25pF/5
R523 1K/4/1, Q102 2N7002/SOT23/25pF/5, C269 1n/4/X7R/50V/K/X
Q101 MMBT2222A/SOT23/600mA/40, R506 8.2K/4/1
27,29,31 PWOK

VDD_MEM

2_5LEVEL, R515 1K/4/1, R514 1.8K/4/1
U146B LM358DR/SO8, 1.5V
BC107 0.1u/4/X7R/16V/K
VCC3 C217 1U/6/X7R/16V/K
Q330 2SK3918/TO252/1300pF/7.5m, R510 100/4/1, EC41 560u/FP/D/6.3V/68/7m
VCC18 R534 0/6/X, VDD_MEM R533 0/6/X
VDD_MEM_ADJ R207 0/4/SHT/X, R517 1K/4/1
1.6V for Side-Port DDR3-1333

EUP

EUP_N, D72 BAT54C/SOT23/200mA
5VSB R2855 8.2K/4/1, R2858 1K/4/1, Q14 BAT54A/SOT23/200mA P_GATE
Q358 MMBT2907A/SOT23/-600mA/50
R2856 68K/4/1, 3V, R2857 100K/4/1, C216 1U/6/X7R/16V/K, Q361 MMBT2222A/SOT23/600mA/40

3VDUAL

5VDUAL C234 0.1u/4/X7R/16V/K → 3VDUAL C236 0.1u/4/X7R/16V/K, EC40 560u/FP/D/6.3V/68/7m
Q36 L1085DG/TO252/5A
R1735 301/4/1, R1737 510/4/1
1.25*(1+510/301)=3.36V

DDR15V

BC98 0.1u/4/X7R/16V/K, BC102 4.7u/8/X5R/6.3V/K
R3186 2K/4/1, DDR_VTTREF, R3187 2K/4/1, DDRVTT
U199 W83310DG/SOP8: VIN, VREF2, GND, ENABLE, VREF1, VCNTL, VOUT, BOOT_SEL, GND
3VDUAL, BC99 0.1u/4/X7R/16V/K
EC43 560u/FP/D/6.3V/68/7m
BC100 0.1u/4/X7R/16V/K
4 VIA to GND

3VDUAL

3VDUAL R532 0/6/SHT/M/X UPI_POWER
For NCT3931 part
BC1117 0.1u/4/X7R/16V/K
U6 NCT3933U/SOT23-8: VDD, VREF1, B_SEL, VREF2, GND, VREF3, SDA, SCL
0x2A
UPI_POWER, R50 8.2K/4/1/X, R128 8.2K/4/1
VDDA25_ADJ → VDDA25_ADJ 32
NB_VCC_ADJ → NB_VCC_ADJ 32
DDR_VTTREF
8,9,15,17,30 SMBDATA, R28 10/4 UPSDA, UPSCK R29 10/4 → SMBCLK

BC1 0.1u/4/X7R/16V/K
U7 NCT3933U/SOT23-8
0X20 = 100% xVCC
UPI_POWER, R130 1K/4/1, R133 6.8K/4/1/X
VCC18_ADJ → VCC18_ADJ 31
VDD_MEM_ADJ
DDR15V_ADJ
UPSDA, UPSCK, 8,9,15,17,30 SMBCLK

ESD5 CM1293A-04SO/S/X: SMBDATA, UPI_POWER, SMBCLK

5VDUAL

BC29 0.1u/4/X7R/16V/K
L3 1.2uH/20A/PMU109/W/D UPA2726/N/7m/PPAKSO8/[10IF9-092726-01R_10IF9-094744-01R_10IF9-074921-01R]
BC44 1U/6/X7R/16V/K, EC44 560u/FP/D/6.3V/68/7m, EC45 560u/FP/D/6.3V/68/7m
Q25, Q26

0.047u/4/X7R/16V/K C1401, R2794 20K/4/1
10p/4/NPO/50V/J C1402
U99 ISL6545CBZ/S: PHASE, BOOT, COMP/SD, UG, FB, GND, VCC_LG/OCSET
31 DDR18V_EN
PWM18_1 → R2799 2.2/6 → DDR18VU_G
R2803 8.2K/4/1, C1404 0.1u/6/X7R/25V/K 25V, DDR18V_PHASE
DDR18VL_G
+12V, 5VDUAL, Q394 BAT54C/SOT23/200mA, R2802 2.2/6
BC933 0.1u/6/X7R/25V/K
R2804 12K/4/1
VREF IS 0.6V

L4 1.2uH/20A/PMU109/W/D UPA2726/N/7m/PPAKSO8/[10IF9-092726-01R_10IF9-094744-01R_10IF9-074921-01R]
DDR15V
1.5V@20A
Default: 1.5V, from AMD
R2805 2.2/6, C1405 1n/4/X7R/50V/K
BC142 0.1U/4/7.5V/16V/Z/X, R2806 2K/4/1, WC18 0.01u/4/X7R/25V/K
EC46 560u/FP/D/6.3V/68/7m, EC47 560u/FP/D/6.3V/68/7m, EC48 560u/FP/D/6.3V/68/7m
R2810 1.3K/4/1
DDR15V_ADJ R214 0/4/SHT/X
0.6*(1+1.5K/1K)=1.5V

GIGABYTE™

Title	DDR POWER	
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PCIE-1G LAN

AVDD33
LR21 8.2K/4/1
LR16 2.49K/4/1
LU1
GND
MDIP0 MDIN0 AVDD10 MDIP1 MDIN1 AVDD10(NC) MDIP2(NC) MDIN2(NC) AVDD10(NC) MDIP3(NC) MDIN3(NC) AVDD33(NC)
P_MDI0+ P_MDI0- VDD10 P_MDI1+ P_MDI1- VDD10 P_MDI2+ P_MDI2- VDD10 P_MDI3+ P_MDI3-
3VDUAL
RSET VDD10 XTALI_P XTALO_P VDD10 LED_ACT_TXRX GPIO LED_LINK100
REGOUT VDDREG VDDREG ENSWREG EEDI LED3/EEDO EECS DVDD10 LANWAKEB DVDD33 ISOLATEB PERSTB
REGOUT VDDREG_IN
LR6 0/4
LR4 8.2K/4/1
LED_LINK1000
LR5 8.2K/4/1
VDD10
-PCIE_WAKE
ISOLATEB
PCIE_RST-
RTL8111E-VB-GR/QFN48
LX1 25M/20p/30ppm/49US/20/D
LC2 27p/4/NPO/50V/J
LC1 27p/4/NPO/50V/J
VCC3
LR17 1K/4/1
LR18 15K/4/1
ISOLATEB 27
PCIE_RST- 20,27,36,37
-PCIE_WAKE 17,20,36,37
LR1 8.2K/4/1
LR3 8.2K/4/1
ML_OP ML_ON SRCCLK_LAN -SRCCLK_LAN
ML_IP ML_IN
LC3 0.1u/4/X7R/16V/K
LC4 0.1u/4/X7R/16V/K
CLOSE LAN CHIP
-PCIE_WAKE LBC34 100p/4/NPO/50V/J/X

3VDUAL
LEC7 100u/OS/D/16V/66/24m
LBC35 0.1u/4/X7R/16V/K
LBC51 0.1u/4/X7R/16V/K
LBC66 0.1u/4/X7R/16V/K
(PIN16,37,46,53,62)

AVDD33
LFB6 0/8/SHT/M/X
LBC53 0.1u/4/X7R/16V/K
LBC63 0.1u/4/X7R/16V/K
LBC64 22u/8/X5R/6.3V/M
LBC58 4.7u/6/X5R/6.3V/K
LBC65 0.1u/4/X7R/16V/K
LBC60 1u/6/X7R/16V/K

VDD10
LBC52 22u/8/X5R/6.3V/M
LBC45 0.1u/4/X7R/16V/K
LBC46 0.1u/4/X7R/16V/K
LBC47 0.1u/4/X7R/16V/K
LBC50 0.1u/4/X7R/16V/K
LBC68 0.1u/4/X7R/16V/K

VDD10
LL1 4.7uH/0.8A/3225/S
REGOUT
LBC69 1u/6/X7R/16V/K
LBC54 0.1u/4/X7R/16V/K
LBC55 0.1u/4/X7R/16V/K
LBC56 0.1u/4/X7R/16V/K
LBC59 1u/6/X7R/16V/K
(PIN8,11,14,58)
(PIN22,28)

USB_LAN

5VDUAL
F10 SMD1812P350SLR/S
FUSEVCC_USB30
LEC4 560u/FP/D/6.3V/68/7m
LBC26 0.1U/4/X7R/16V/K
F9 SMD1812P350SLR/S
FUSEVCC_USB31
LEC5 560u/FP/D/6.3V/68/7m
LBC27 0.1U/4/X7R/16V/K

SSTXDP1C SSTXDN1C SSRXDN1 SSRXDP1
UE1 USB 3.0 ESD protect. AZ1045-04F/MSOP10
SSTXDN1C SSTXDP1C SSRXDP1 SSRXDN1
SSTXDN2C SSTXDP2C SSRXDN2 SSRXDP2
UE2 USB 3.0 ESD protect. AZ1045-04F/MSOP10
SSTXDP2C SSTXDN2C SSRXDP2 SSRXDN2

ESD4
DM2 DP2 DP1 DM1 FUSEVCC_USB30
CM1293A-04SO/S

RTL8101E:LR38/LC5/LR43/LC6-->O
RTL8111C:LC6-->O
RTL8102E:LC5/LC6-->O

FOR EMI
LBC49 0.01u/4/X7R/25V/K
USB30_LAN
P_MDI0+ P_MDI0- P_MDI1+ P_MDI1- P_MDI2+ P_MDI2- P_MDI3+ P_MDI3-
LBC29 0.01u/4/X7R/25V/K
FUSEVCC_USB30
LBC25 0.1U/4/X7R/16V/K
DM1 DP1
SSRXDN1 SSRXDP1
SSTXDN1 SSTXDP1
UC26 UC24 0.1u/4/X7R/16V/K
SSTXDN1C SSTXDP1C
USB3.0
USB3+RJ45/[11NR6-702009-K1R]
Close to USB30_LAN
LED_ACT_TXRX
LED_LINK100
LED_LINK1000
LR31 150/6
LR32 150/6/X
LR30 150/6/X
3VDUAL
LFB5 0/6/SHT/M/X
LBC28 0.1u/4/Y5V/16V/Z/X
RTL8111D -->N/A
FUSEVCC_USB31
DM2 DP2
SSRXDN2 SSRXDP2
SSTXDN2C SSTXDP2C
UC20 UC22 0.1u/4/X7R/16V/K
SSTXDN2 SSTXDP2
Close to USB30_LAN
90歐姆:[20/6/5.5/6/20]

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1

GIGABYTE™
Title: REALTK RTL8111E
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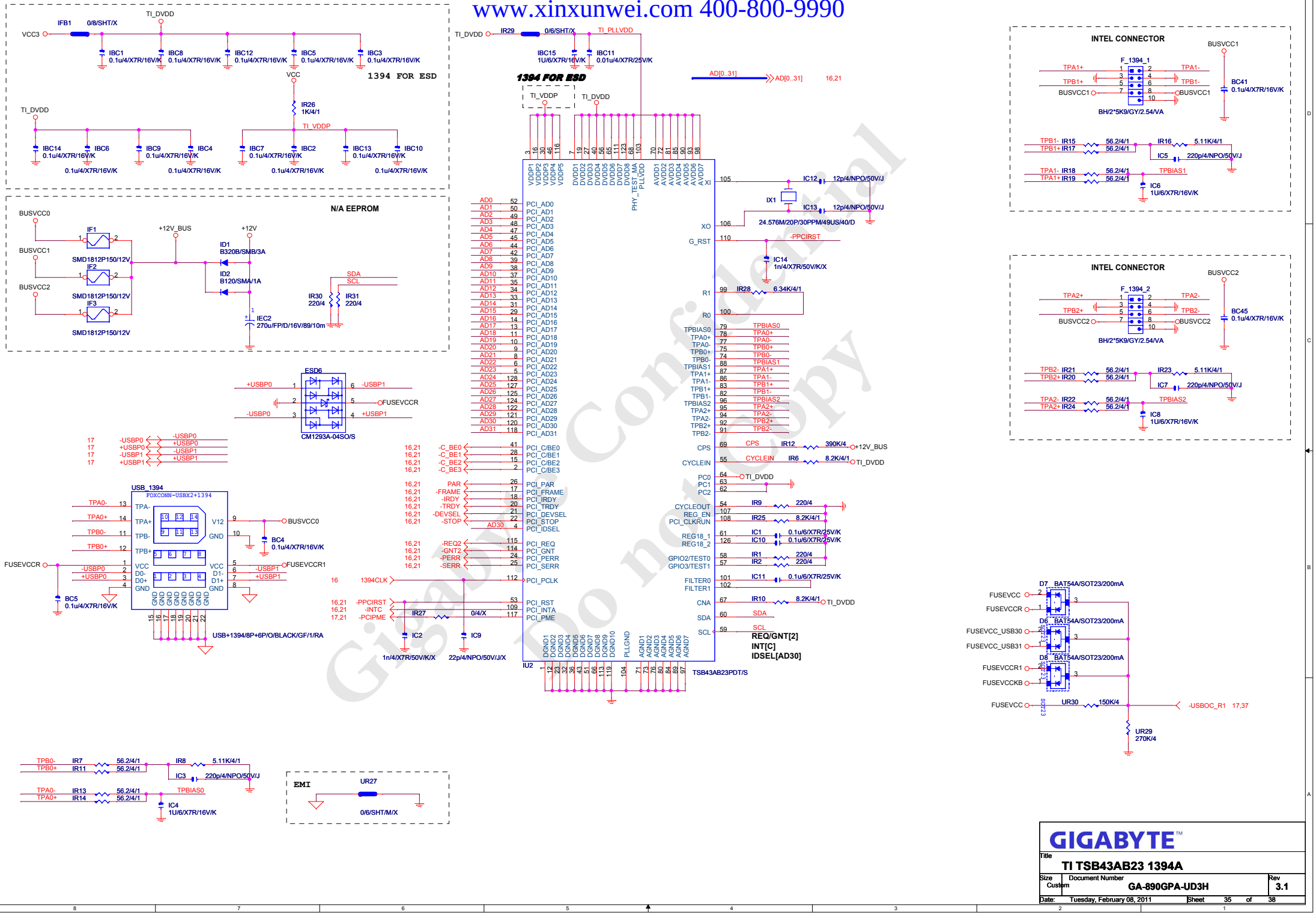

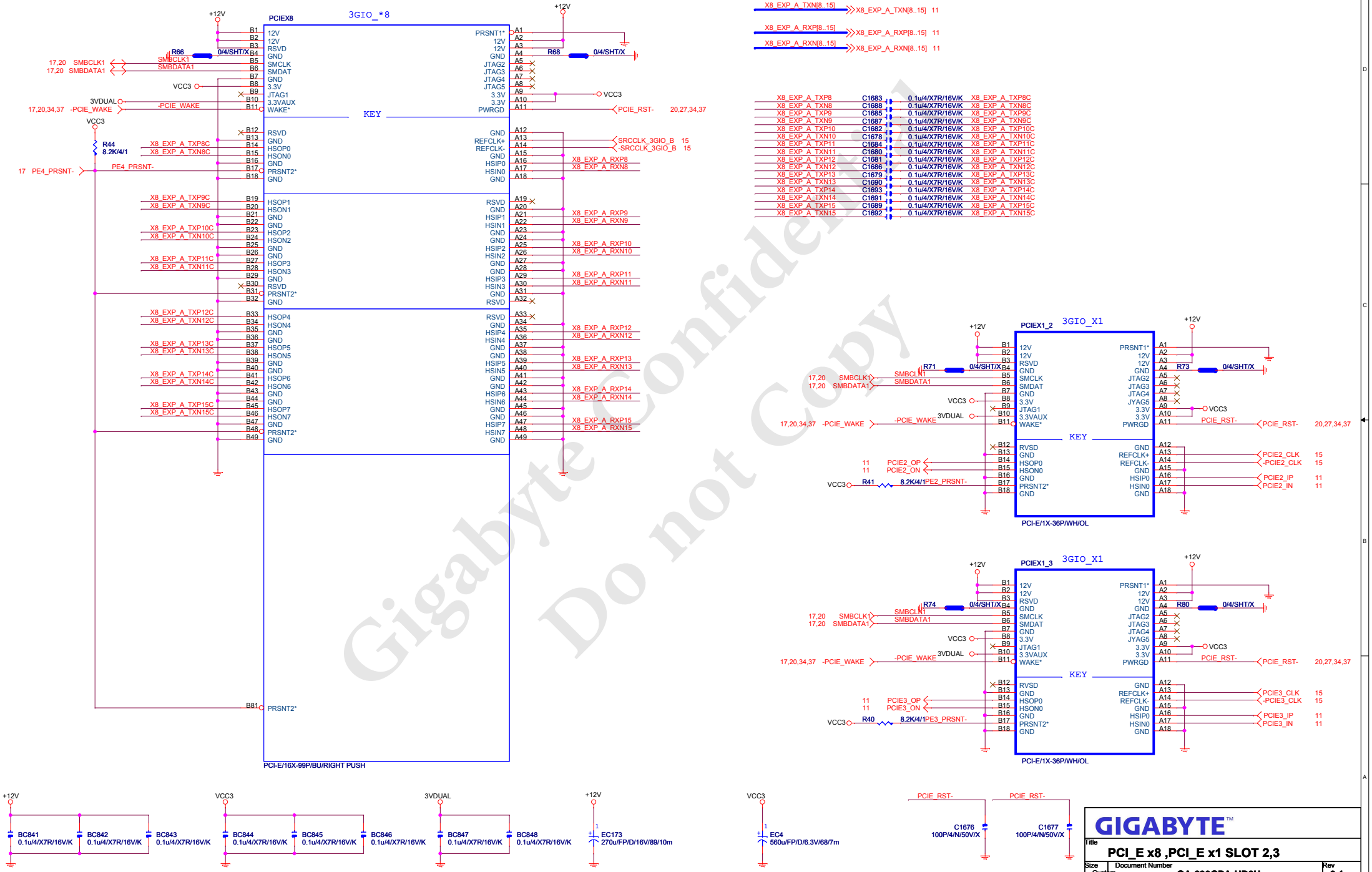

GIGABYTE		
Title	PCI_E x8 ,PCI_E x1 SLOT 2,3	
Size: Custom	Document Number: GA-890GPA-UD3H	Rev: 3.1
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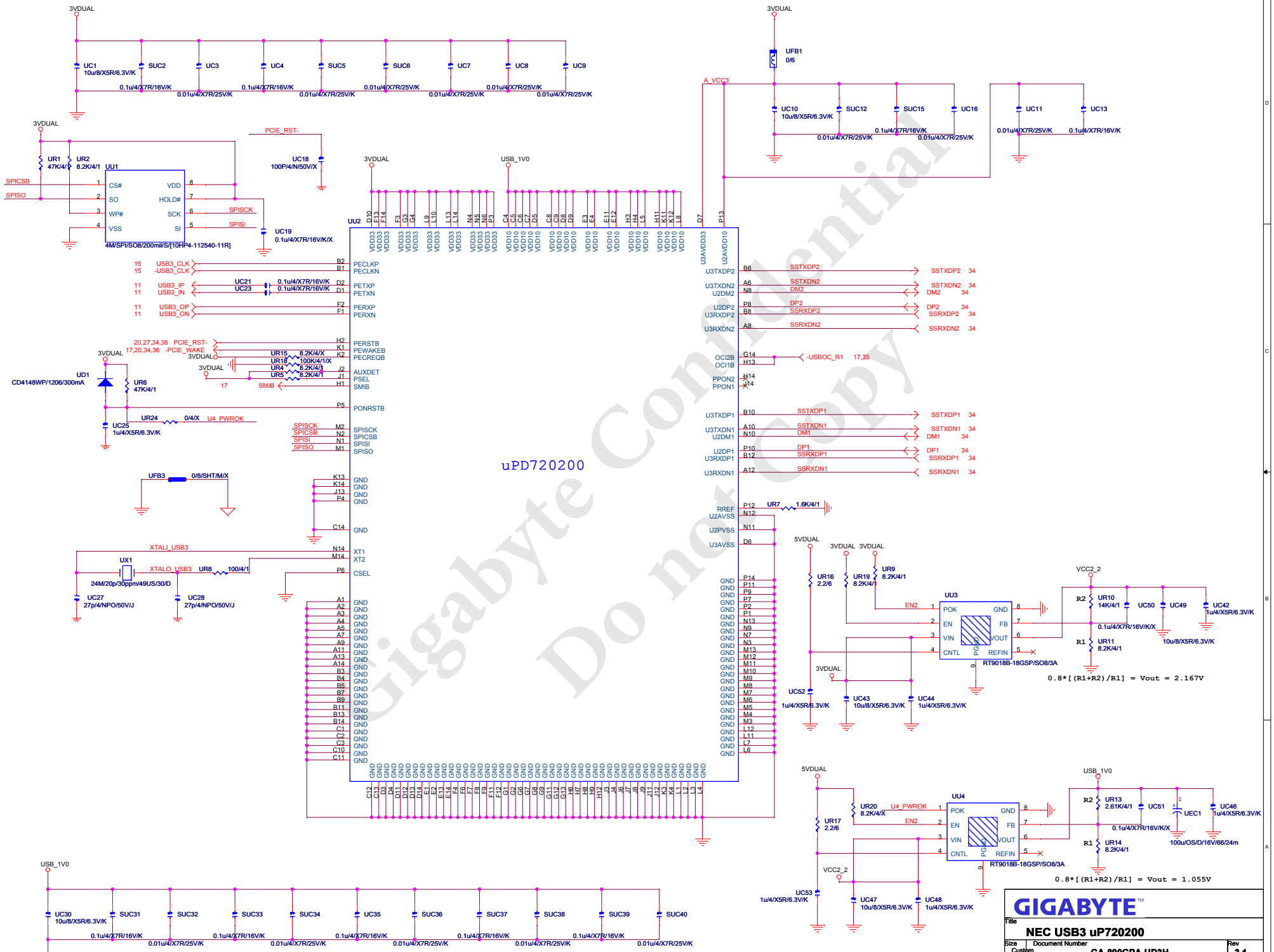

3.3V to 1.8V Voltage Regulator

VCC3 → JBC11 0.1u/4/X7R/16V/K
VCC_1.8V ← JQ1 L1085DG/TO252/5A
JR1 100/4/1
JR2 44.2/4/1
JEC1 100u/OS/D/16V/66/24m

JMB363

LQFP 100 14x14

GBB363/LQFP100/[10HP2-640363-20R]

SMBUS for test mode only.

JR3 8.2K/4/1 SMB_CLK
JR4 8.2K/4/1 SMB_DAT
SBPCIE_RST-
JC11 100P/4/NPO/50V/.J/X

close to IC

JBC3 1u/4/X5R/6.3V/K
JBC4 0.1U/4/X7R/16V/K
JBC5 1u/4/X5R/6.3V/K
JBC6 0.1U/4/X7R/16V/K
JBC7 1u/4/X5R/6.3V/K
JBC8 0.1U/4/X7R/16V/K
JBC9 2.2u/6/X5R/6.3V/K

Close to U49 pin94 and pin105

JC12 1u/4/X5R/6.3V/K
JC13 0.1U/4/X7R/16V/K
JEC2 560u/FP/D/6.3V/68/7m
JC14 0.1U/4/X7R/16V/K

Near to PIN — Check SATA eye

PCIE_REXT → JR11 8.2K/4/1
SATA_REXT1 → JR12 12K/4/1
SATA_REXT0 → JR13 12K/4/1
PCIE_REXT --> 8.06K/4/1

XTALI — JC9 33P/4/NPO/50V/J
JR9 1M/4
JX1 25M/20p/30ppm/49US/20/D
XTALO — JC10 33P/4/NPO/50V/J

JC31 0.1u/4/X7R/16V/K
JC32 0.1u/4/X7R/16V/K

J363_IP 16
J363_IN 16
J363_ON 16
J363_OP 16
J363CLKP 15
J363CLKN 15

close to IC

JC15 0.1U/4/X7R/16V/K
JC19 22u/8/X5R/6.3V/M

JBC2 10u/8/X5R/6.3V/K

Close to U49 pin110

JC20 2.2u/6/X5R/6.3V/K
JC21 0.1U/4/X7R/16V/K
JC22 0.1U/4/X7R/16V/K

Close to U49 pin99

JC23 2.2u/6/X5R/6.3V/K
JC24 0.1U/4/X7R/16V/K

CLOSE TO U49 PIN61

JC26 0.1U/4/X7R/16V/K
JC27 2.2u/6/X5R/6.3V/K

close to U49 pin56

JC28 2.2u/6/X5R/6.3V/K
JC29 0.1U/4/X7R/16V/K
JC30 1u/4/X5R/6.3V/K

VCC → JR15 1K/4/1 → PH_RESETnA
VCC3 → JR14 8.2K/4/1 → JQ2 MMBT2222A/SOT23/600mA/40 (SOT23)
RESETnA

JD1 -IDEACTP, J_LED → -HDLED → -HDLED 23,29
BAT54A/SOT23/200mA (SOT23)

IORDYA JR8 1K/4/1 → VCC3
DMARQA JR5 8.2K/4/1
INTRQA JR6 8.2K/4/1
DD7A JR7 8.2K/4/1

IDE

PH_RESETnA	1	2	
DD7A	3	4	DD8A
DD6A	5	6	DD9A
DD5A	7	8	DD10A
DD4A	9	10	DD11A
DD3A	11	12	DD12A
DD2A	13	14	DD13A
DD1A	15	16	DD14A
DD0A	17	18	DD15A
	19		(#20 key-pin)
DMARQA	21	22	
DIOWnA	23	24	
DIORnA	25	26	
IORDYA	27	28	
DMACKnA	29	30	
INTRQA	31	32	(#32 IOCS16)
DA1A	33	34	PDIAGnA
DA0A	35	36	DA2A
CS0nA	37	38	CS1nA
-IDEACTP	39	40	

BH/2*20K20/WH/SHN/2.54/VA/PA46

GSATA2_6_7
E_TXP0 JC1 0.01u/4/X7R/25V/K
E_TXN0 JC2 0.01u/4/X7R/25V/K
E_RXN0 JC3 0.01u/4/X7R/25V/K
E_RXP0 JC4 0.01u/4/X7R/25V/K
JC5 0.01u/4/X7R/25V/K E_TXP1
JC6 0.01u/4/X7R/25V/K E_TXN1
JC7 0.01u/4/X7R/25V/K E_RXN1
JC8 0.01u/4/X7R/25V/K E_RXP1
SATA/14/WH/H/OP/RA/D/2

GIGABYTE™

Title: JMB363

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