LS1511G GLK Schematics

Gemini Lake

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DY	***DUMMY, NOT ASM***
DDP/ SDP	***Memory down BOM Control***
DDR4_CTRL	***Memory down BOM Control***
MEM_IDx_x	***Memory ID for SW Team (BOM Control)***
PCB_ID	***PCB ID for SW Team (PCB version)***
SKU_ID	***SKU ID for SW Team (Model ID)***
XDP	***Debug Connector***
PSL/ Non PSL	***Support / Non Support KBC Power Switched Logic***
PTC	***positive temperature coefficient***
EMMC	***Embedded Multi Media Card***
WLAN/ CNVi	***Support WLAN type (PCIe or CNVi interface)***
SHARE NON_SHARE	***SPI ROM BOM Control***

LS1511G

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Title: ***Cover Page***

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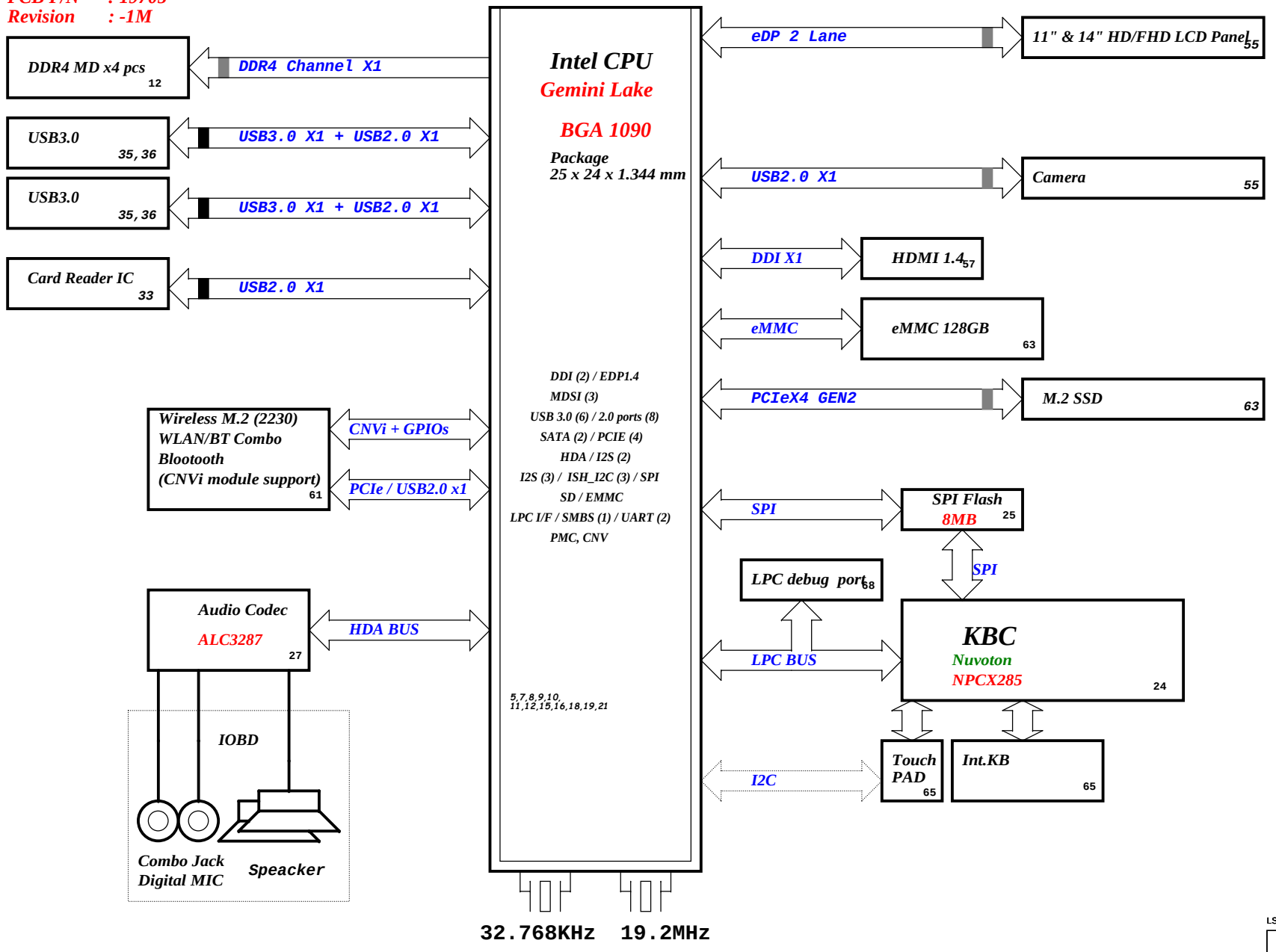
Project code :
LS1511G- 4PD0JB010001
LS1514G- 4PD0JC010001
PCB P/N : 19705
Revision : -1M

Gemini Lake Board Block Diagram

External Connector/Socket
Internal Connector/Socket

PCB Layer
L1:Top
L2:GND
L3:Signal
L4:Signal
L5:GND/VCC
L6:Bottom



CHARGER HPA02224		44
INPUTS	OUTPUTS	
19V_DCBATOUT	BT+	

SYSTEM DC/DC SY8286B/ SY8288C		45
INPUTS	OUTPUTS	
19V_DCBATOUT	5V_S5 3D3V_S5 5V_AUX_S5 3D3V_AUX_S5	

SYSTEM DC/DC BD9515NUXE2		47
INPUTS	OUTPUTS	
5V_S5	1V_CPU_VCGI	

CPU PMIC BD2671MWV		50
INPUTS	OUTPUTS	
5V_S5	1V_CPU_VNN 1D05V_S5	

CPU PMIC BD2671MWV		51
INPUTS	OUTPUTS	
5V_S5	1D2V_CPU_VDDQ_S3 1D2V_S5 1D8V_S5	
1D2V_CPU_VDDQ_S3	0D6V_VREF_S0	
3D3V_S5	2D5V_S3	

SYSTEM Load switch G2898KD1U/APE8939GN3		40
INPUTS	OUTPUTS	
5V_S5	5V_S0	
3D3V_S5	3D3V_S0	
1D8V_S5	1D8V_S0	

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Title: Block Diagram

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Title: *CPU (RSVD)*

Size	Document Number	Rev
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Title: ***CPU (RSVD)***

Size	Document Number	Rev
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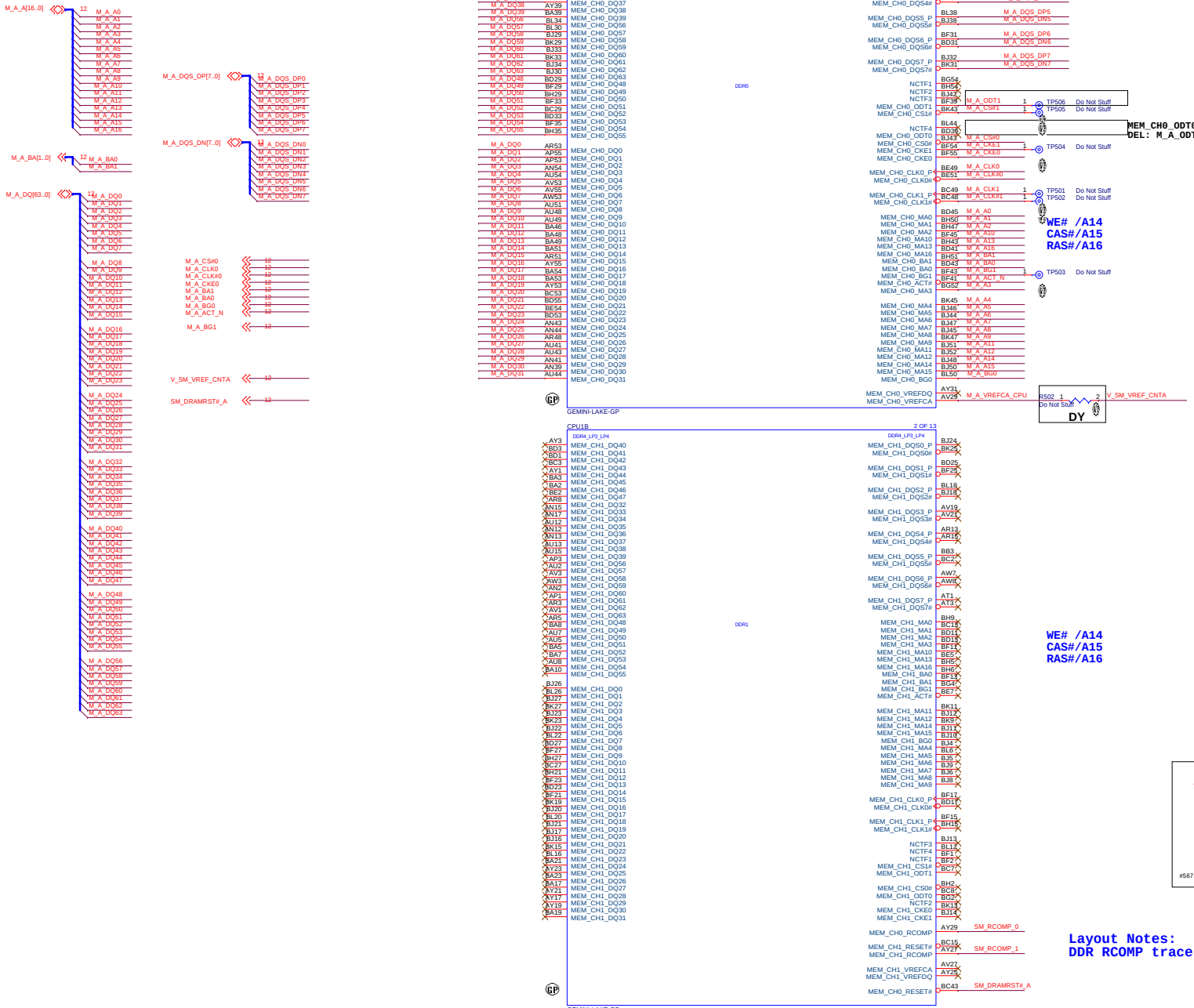
Date: Friday, December 27, 2019 Sheet 4 of 106

SSID = CPU



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Title: CPU (DDR)

Size	Document Number	Rev
A2	LS1511G	-1M

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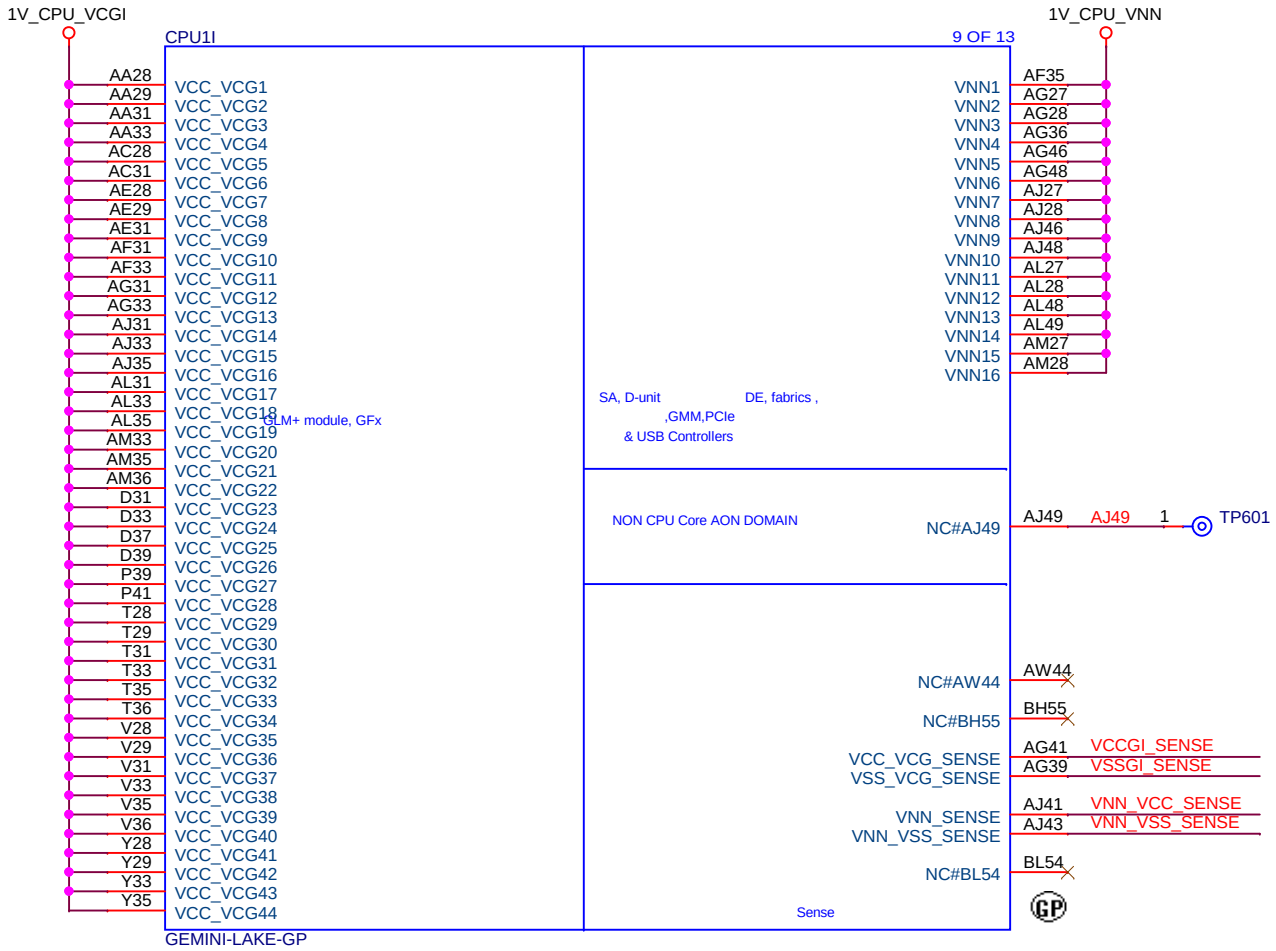
SSID = CPU PDG P54

VSSGI_SENSE <<- 47
VCCGI_SENSE <<- 47
VNN_VCC_SENSE <<- 50
VNN_VSS_SENSE <<- 50



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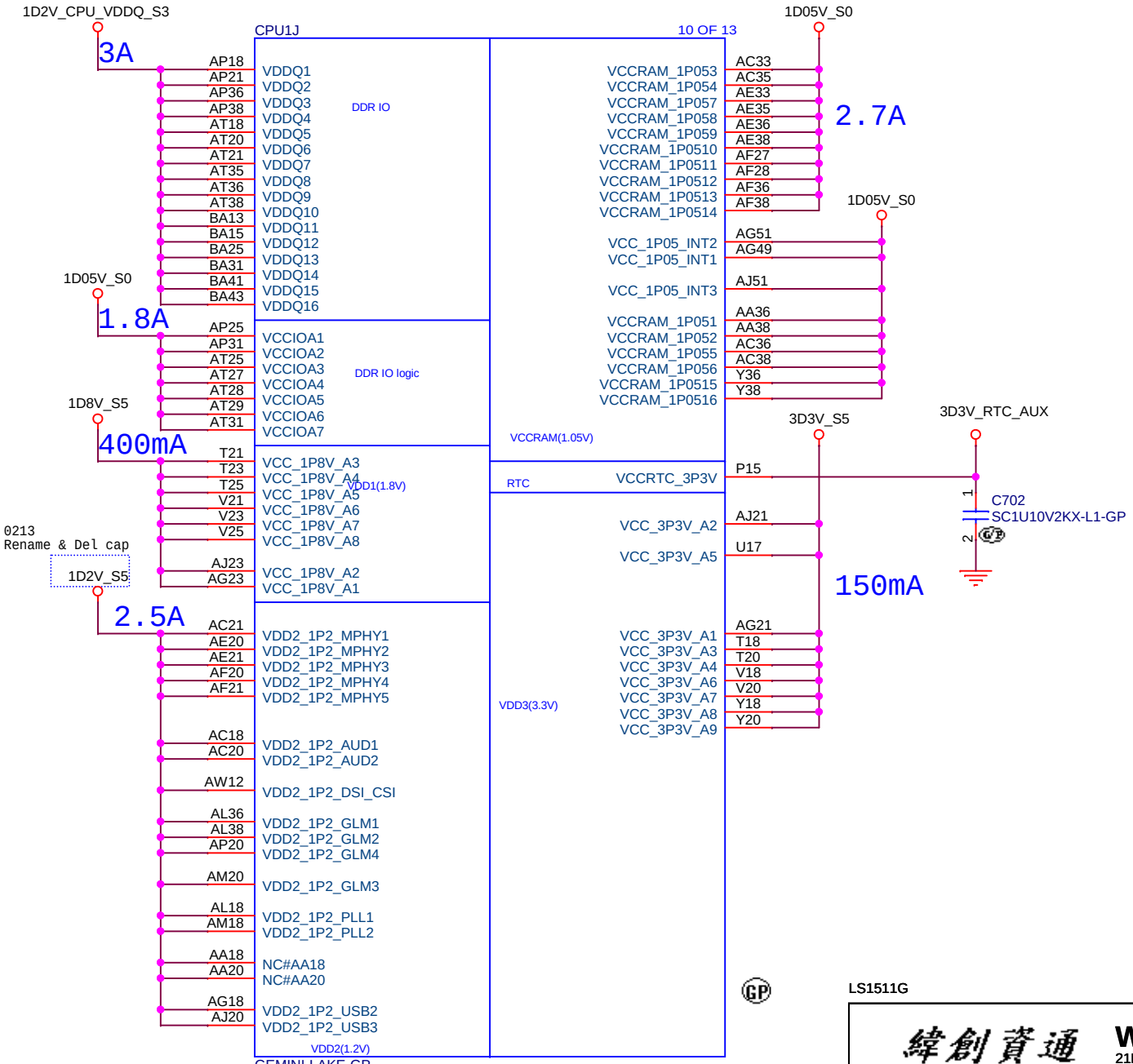
Title: ***CPU (VCCGI/VNN)***

Size	Document Number	Rev
A4	**LS1511G**	**-1M**

Date: Friday, December 27, 2019 Sheet 6 of 106

SSID = CPU



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Title: ***CPU (VDDQ/VCCIO/Others)***

Size	Document Number	Rev
A4	LS1511G	-1M

Date: Friday, December 27, 2019 Sheet 7 of 106

SSID = CPU

HDMI

HDMI_SCL_CPU 57
HDMI_SDA_CPU 57
HDMI_DDI_TX_P0 57
HDMI_DDI_TX_N0 57
HDMI_DDI_TX_P1 57
HDMI_DDI_TX_N1 57
HDMI_DDI_TX_P2 57
HDMI_DDI_TX_N2 57
HDMI_DDI_TX_P3 57
HDMI_DDI_TX_N3 57
HDMI_DET_CPU 57

EDP

eDP_TX_CPU_N0 55
eDP_TX_CPU_P0 55
eDP_TX_CPU_P1 55
eDP_TX_CPU_N1 55
eDP_AUX_CPU_N 55
eDP_AUX_CPU_P 55
eDP_BLEN_CPU 55
eDP_VDDEN_CPU 55
eDP_HPD_CPU 55
eDP_BLCTRL_CPU 55

GPIO42_FLASH_OVR 15
ME_UNLOCK 24
GPIO43_DSI_TE2 99

Check list
10K Ω ±5% Pull-up to 1.8VS3 rail

CPU1C — 3 OF 13

DDI0_TXP_0 AH1 / DDI0_TXN_0 AH3
DDI0_TXP_1 AE2 / DDI0_TXN_1 AE3
DDI0_TXP_2 AJ2 / DDI0_TXN_2 AJ3
DDI0_TXP_3 AG2 / DDI0_TXN_3 AG3
DDI0_AUXP AC12 / DDI0_AUXN AC10
HV_DDI0_HPD C39
DDI0_DDC_SCL B43 / DDI0_DDC_SDA C43
DDI0/DDI_B
3.3V (default)

DDI1_TXP_0 AA2 / DDI1_TXN_0 AA3
DDI1_TXP_1 Y3 / DDI1_TXN_1 Y1
DDI1_TXP_2 AD1 / DDI1_TXN_2 AD3
DDI1_TXP_3 AC2 / DDI1_TXN_3 AC3
DDI1_AUXP AC7 / DDI1_AUXN AC5
DDI1_DDC_SCL C42 / DDI1_DDC_SDA A42
HV_DDI1_HPD C38
DDI1/DDI_C
1.8V level
3.3V (default)

EDP_TXP_0 AE12 / EDP_TXN_0 AE13
EDP_TXP_1 AC15 / EDP_TXN_1 AC17
EDP_TXP_2 AE10 / EDP_TXN_2 AE8
EDP_TXP_3 AE5 / EDP_TXN_3 AE7
EDP_AUXP W17 / EDP_AUXN W15
HV_DDI2_HPD B39
PNL0_BKLCTL B41 / PNL0_BKLTEN C40 / PNL0_VDDEN C41
EDP_RCOMP_P AA5 / EDP_RCOMP# AA7
eDP/DDI_A
1.8V (default)
GEMINI-LAKE-GP

MDSI_A_CLKP AL2 / MDSI_A_CLKN AM3
MDSI_C_CLKP AG13 / MDSI_C_CLKN AG12
MDSI_A_DP_0 AN5 / MDSI_A_DN_0 AN7
MDSI_A_DP_1 AJ15 / MDSI_A_DN_1 AJ17
MDSI_A_DP_2 AJ7 / MDSI_A_DN_2 AJ5
MDSI_A_DP_3 AJ10 / MDSI_A_DN_3 AJ12
MDSI_C_DP_0 AG15 / MDSI_C_DN_0 AG17
MDSI_C_DP_1 AG8 / MDSI_C_DN_1 AG10
MDSI_C_DP_2 AG7 / MDSI_C_DN_2 AG5
MDSI_C_DP_3 AE15 / MDSI_C_DN_3 AE17
MDSI

MIPI_I2C_SCL R53 / MIPI_I2C_SDA R54
0214 change net name
0214 Adding R811
0216 Adding GPIO 43

GPIO_43 MDSI_C_TE
GPIO_42 MDSI_A_TE
T53 GPIO43_DSI_TE2 — 1 TP801
T55 GPIO42_FLASH_OVR
R811 1 — 2 ME_UNLOCK
0R402-DB-GP-U

MDSI_RCOMP AL5
R810 150R2F-4-L-GP
MDSI_A_TE:
If MIPI DSI is not implemented, leave them NC.

Layout Notes:
layout W/S=10/15mil, length <1000mil.

R801 100R2F-L-GP-U
#567247 #253 Table15-6
eDP signals disable guideline

Layout Notes:
Impedance 85 Ohm and space 20mil, length <400mil.

HDMI

3D3V_S0 — R809 10KR2J-L-GP
3D3V_S0 — SC_1018 — RN802 Do Not Stuff DY

HV_DDIX_HPD
It is required to enable internal 20k pull up resistor on the HV_DDI2_HPD signals by BIOS.

EDP

1D8V_S0 — R807 100KR2J-4-GP
eDP_HPD_CPU — 0222 Change PN — Q802 PJA138KA-GP — eDP_HPD_CPU_D
084.00138.0A31

HV_DDIX_HPD
It is required to enable internal 20k pull up resistor on the HV_DDI2_HPD signals by BIOS.

3D3V_S0 1D8V_S0 — RN801 SRN2K2J-1-GP
eDP_BLCTRL_CPU_B
eDP_BLCTRL_CPU — Q803 LMBT3904LT1G — eDP_BLCTRL_CPU_E
84.T3904.H11
R813 1 — 2 Do Not Stuff DY

3D3V_S0 1D8V_S0 — DY RN803 Do Not Stuff
eDP_VDDEN_CPU_B
eDP_VDDEN_CPU — Q804 Do Not Stuff — eDP_VDDEN_CPU_E
Do Not Stuff
R812 1 — 2 0R402-DB-GP-U

15.1.2.5HPD Implementation
The hot-plug detect output from eDP* sink device is a 3.3V active high signal. Since the input on the processor is a 3.3V active low signal, a logic inversion circuit is required on the motherboard. Fi gure 15-7 shows an example of this implementation.

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Title: **CPU (DDI/EDP/MDSI)**
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Title: ***CPU (RSVD)***

Size	Document Number	Rev
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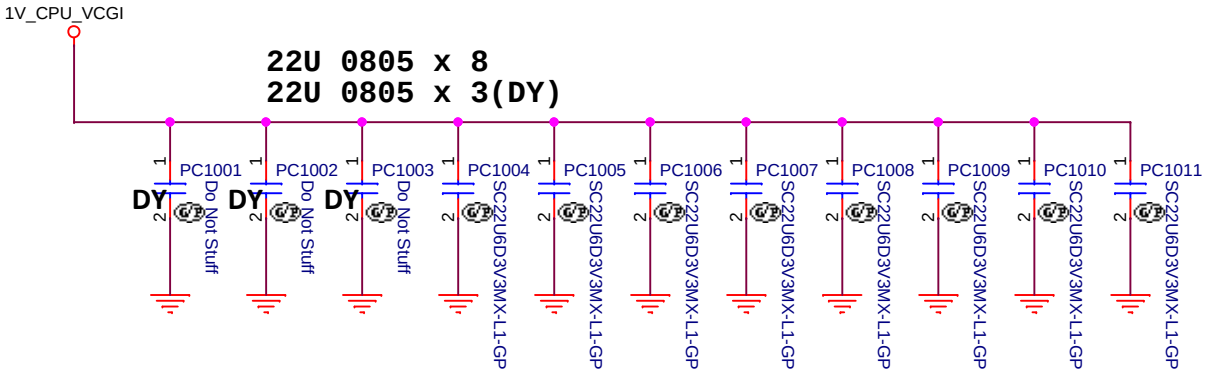
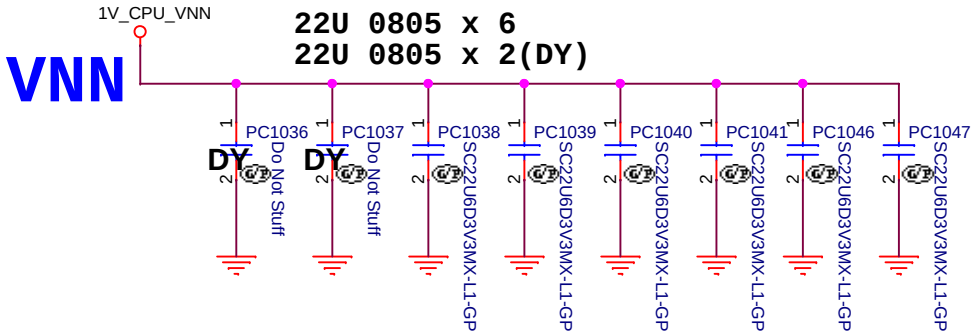
SSID = CPU

VCCGI

IccMax = 21 A



VNN



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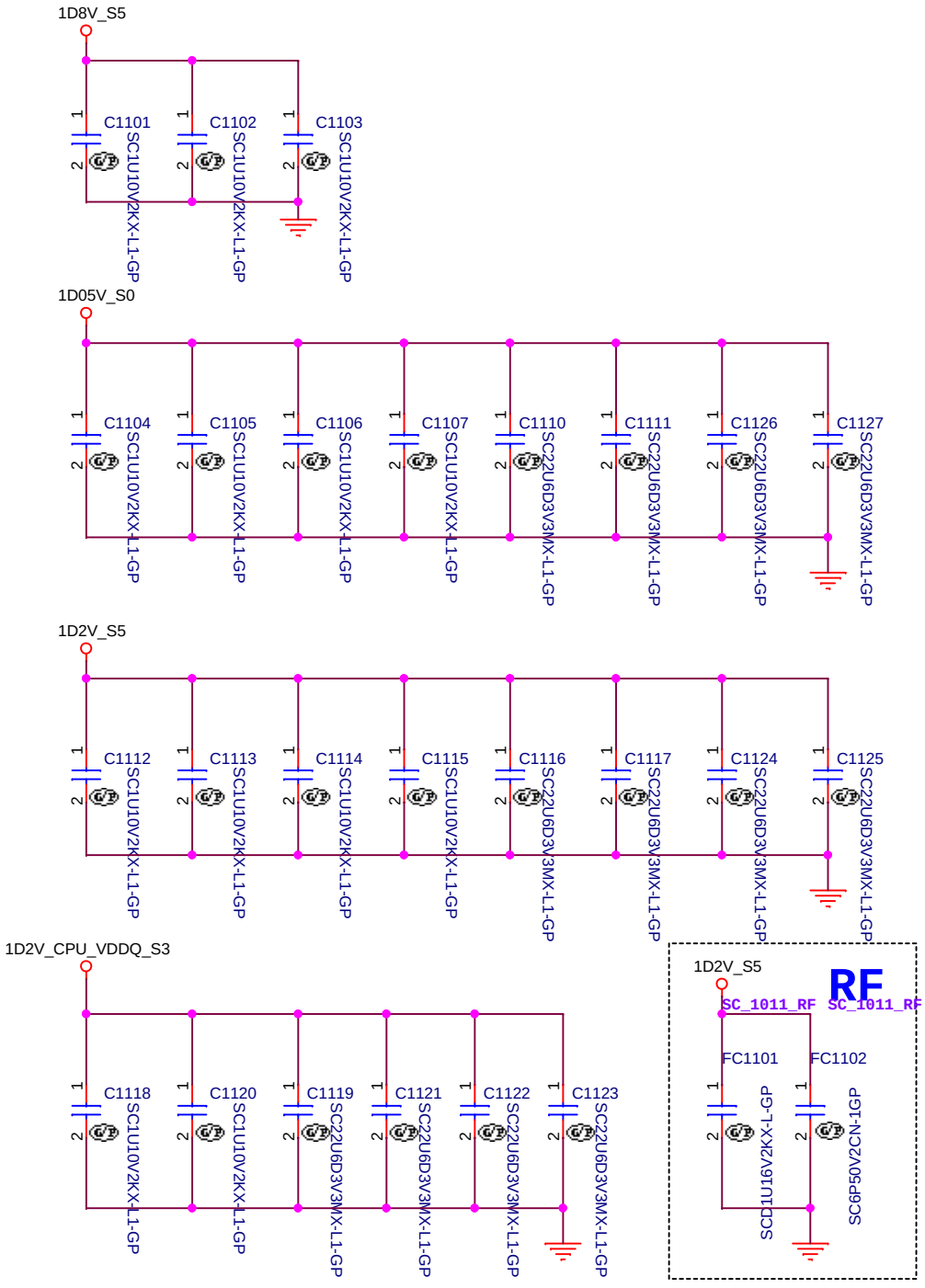
Title: CPU (Power CAP1)

Size	Document Number	Rev
A4	LS1511G	-1M

Date: Friday, December 27, 2019 Sheet 10 of 106

SSID = CPU



System Rail Name	Power Balls [GND]	Max L from Ball to nearest BSC [0402-1uF]			Max L from Ball to nearest ESC [0402 - 1uF]			Max L from Ball to nearest MLCC [0603 - 22uF *0805 - 22uF #0805 - 47uF]			Max L / R from Ball to VR Bulk [330uF_9mOhm]		
		Back Side Cap	BSC (nH)	Total (nH)	Top Side Edge Cap	ESC (nH)	Total (nH)	Top Side MLCC	MLCC (nH)	Total (nH)	Top Side Bulk	Bulk (nH)	(mΩ)
VCC_1P8V_A	V21,T25,V25,T23,V23,T21 [Y27,Y25,Y23,Y21,T27,V27,P21] AJ23,AG23[AJ25, AG25]	C417 C438 BSC_USB	1.36 0.714 1.29	0.673									
VCCIOA	AT27,AT28,AT29,AT25,AP31,AT31,AP25 [AM29,AP27,AP28,AP28,AP33,AT33,AP23,AT23,AU28,AM31]	C429 C418	0.475 0.475	0.426	C202 C203	3.72 4.10	3.6	C601 C602	5.12 4.78	4.537			
VDDQ	AP36,AT36,AP38,AT38,AT35,AT18,AP18,AP21,AT20,AT21,BA43,BA41,BA31,BA13,BA15,BA25 [AV39,AR39,AP35,AM38,AT33,AP33,AT23,AR17,AP23,AM23,AM21,AY43,AV33,BC31,AV23,AV17,AV41,AY41,BC25,AY13,AY15]	C412 C428	0.475 0.523	0.223				*C816 *C817 *C820 *C821	2.06 4.10 1.62 3.30	0.496			
VCCRAM_1P05	AC35,AE35,AE38,AE36,AF28,AF27,AF38,AF36,AC33,AE33 [AE27,AF29,AF40,AG38,AJ38,AC29,AA35,AG35,AJ36,AF25]	C424	0.712					C608	2.89				
VCCRAM_1P05_IO	AA36,AA38,Y36,Y38,AC38,AC36 [V38,W39,AF40,W41,T38,AA35]	C405	0.989					C609	3.62				
VDD2_1P24_GLM	AP20,AL38,AL36 [AM21,AR17,AJ38, AJ36]	C415	0.619		C219	1.78		C610 C611	2.10 2.09	1.978			
VDD2_1P24_AUD_ISH_PLL	AM18,AL18 [AJ18, AL17]	C435	0.791					#C823 #C824	1.88 1.88	1.75			
VDD2_1P24_USB2	AJ20,AG18 [AG20, AJ18]	C433	0.747		C217	1.723		C623	2.13				
VDD2_1P24_MPHY	AC21,AE20,AE21,AF20,AF21 [AG20,AF18,AE18,AA23,AC23,AE23,AF23,AA21]	C442	0.667		C218	1.6		C624	2.08				
VDD2_1P24_DSI_CSI	AW12[AW10]							C625	2.22				

電容位置都要在1D2V_S5 Bottom層Power周圍
(預設DY)

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Title: **CPU (Power CAP2)**

Size	Document Number	Rev
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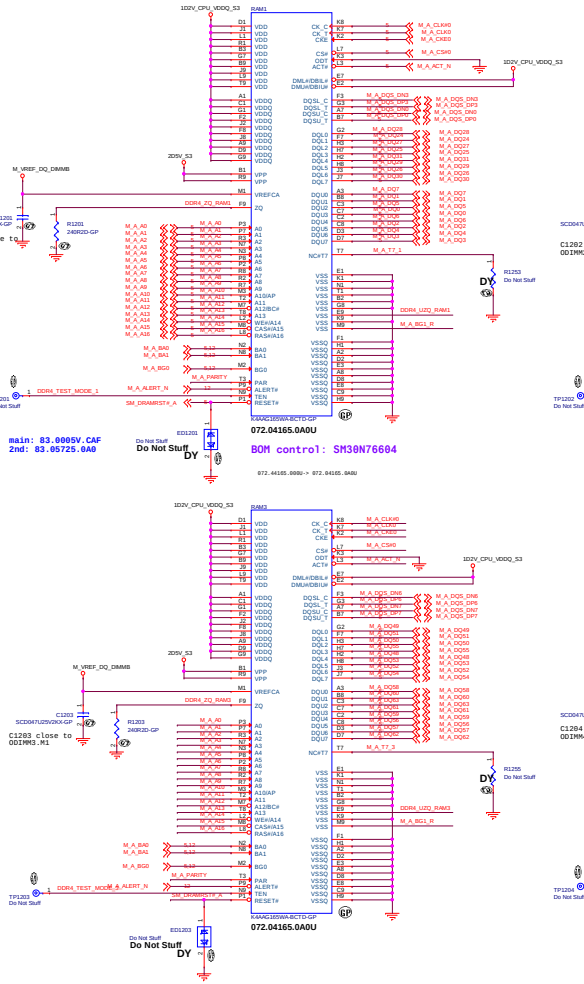
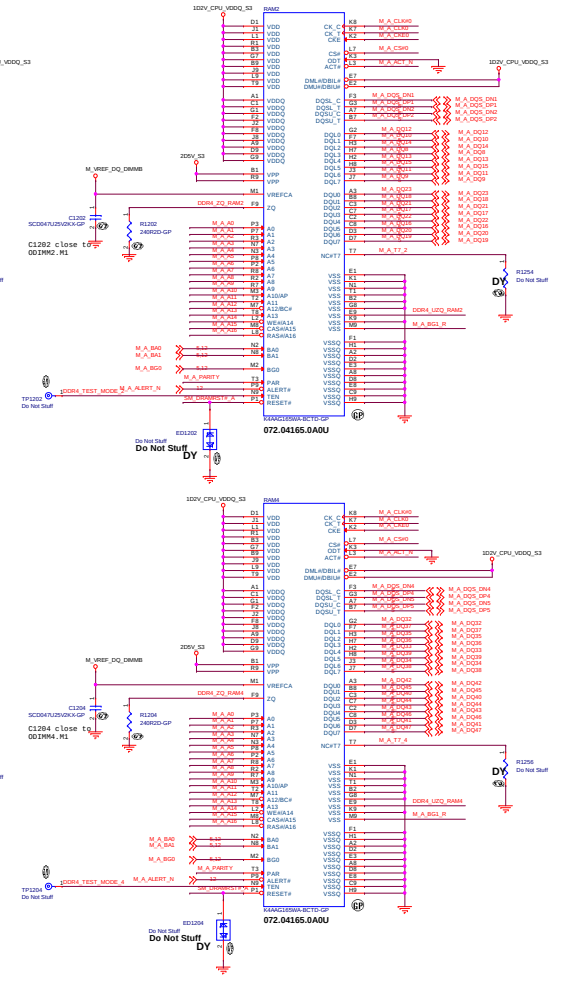
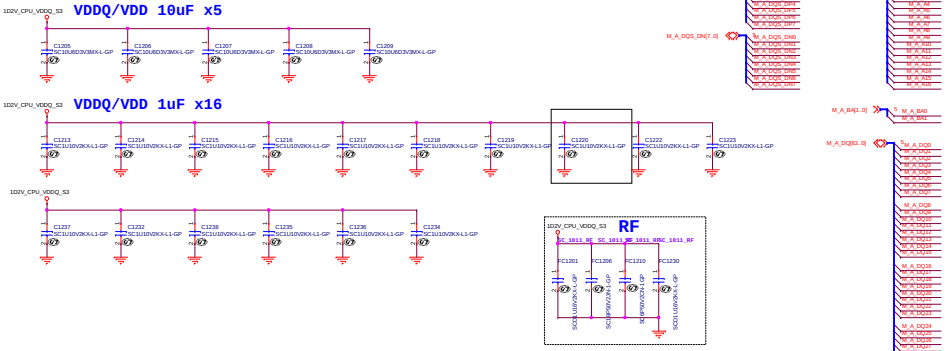
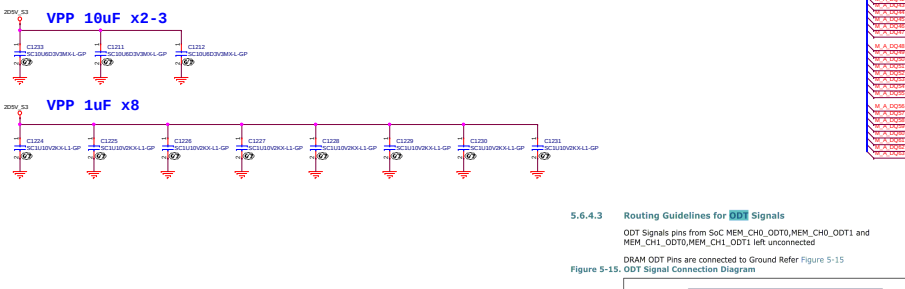
Main Func = DDR4 On Board with Single Rank

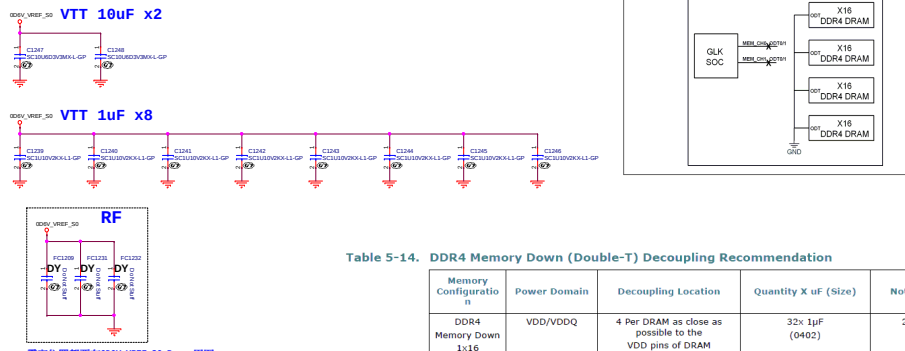




DDR4 On Board RAM Power Decouple Cap







[561280] 4.23.S KBL-U DDR4 Memory Down Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x uF (size)
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1uF (0402) (All stuffed)
		Distributed around the DRAM devices	10x 10uF (0603) (All stuffed)
	VPP	2 as near each x16 DRAM device as possible	16x 1uF (0402)
		Distributed around the DRAM devices	5x 10uF (0603)
	VTT	2 as near each x16 DRAM device as possible	16x 1uF (0402)
		Distributed around the DRAM devices	4x 10uF (0603)

5.6.4.3 Routing Guidelines for ODT Signals

ODT Signals pins from SoC MEM_CH0_ODT0,MEM_CH0_ODT1 and MEM_CH1_ODT0,MEM_CH1_ODT1 left unconnected

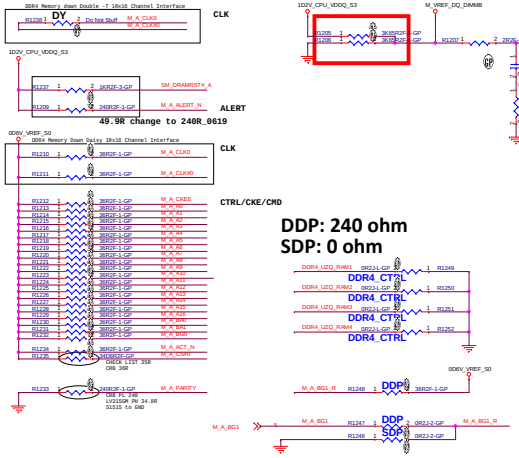
DRAM ODT Pins are connected to Ground Refer Figure 5-15

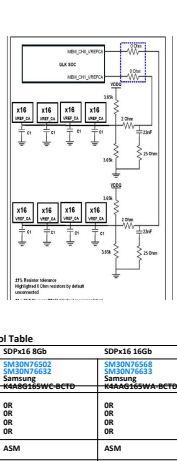
Figure 5-15. ODT Signal Connection Diagram

Table 5-14. DDR4 Memory Down (Double-T) Decoupling Recommendation

Memory Configuration	Power Domain	Decoupling Location	Quantity X uF (Size)	Notes
DDR4 Memory Down 1x16 (4 device) Each channel	VDD/VDDQ	4 Per DRAM as close as possible to the VDD pins of DRAM	32x 1µF (0402)	2
		Distribute evenly across domain, close by Drams	10x 10µF (0603)	
	Vpp	2 as near each x16 DRAM device as possible	16x 1µF (0402)	2
		Distribute evenly across domain, close by Drams	5x 10µF (0603)	2
	VTT	2 as near each x16 DRAM device as possible	16x 1µF (0402)	2
		Distribute evenly across domain, close by Drams	4x 10µF (0603)	2

Notes:
1. The decoupling solution can be taken as an reference, suggest customer to perform completed simulation and validation to verify the solution.
2. Total quantity is referring to 2 channels.
3. Decoupling for the DDR4 Memory Down will also be dependent on the DRAM memory requirements itself. Check with DRAM vendor for additional requirements or specifications.





SDP and DDP BOM Control Table

		SDPx16 8Gb	SDPx16 16Gb	SDPx16 8Gb	SDPx16 8Gb	SDPx16 16Gb	DDPx16 16Gb
		SM30N76502 SM30N76632 Samsung K4A8G165WC-BCTD	SM30N76568 SM30N76633 Samsung K4A8G165WA-BCTD	SM30N76518 SM30N76639 SK Hynix H5ANB8G6NCJR-VKC	SM30N76570 Micron MT40A512M16TB-062E	SM30N76604 Micron MT40A1G16RC-062E:B	SM30N76546 SM30N76640 SK Hynix H5ANB8G6NCJR-VKC
DDR4_CTRL	R1249 R1250 R1251 R1252	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	240R 1% 240R 1% 240R 1% 240R 1%
SDP	R1246	ASM	ASM	ASM	ASM	ASM	DY
DDP	R1247 R1248	DY DY	DY DY	DY DY	DY DY	DY DY	ASM ASM

DDPx16 16Gb SM30N76504 Samsung

DDPx16 16Gb SM30851324 Micron

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-MD_CHA)

Size: A3 | Document Number: LS1511G | Rev: -1M

Date: Friday, December 27, 2019 | Sheet 12 of 105

Blanking

LS1511G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR (DDR4-SODIMM2_CHB RSVD)***

Size	Document Number	Rev
A4	LS1511G	-1M

Date: Friday, December 27, 2019 Sheet 13 of 106

Blanking

LS1511G

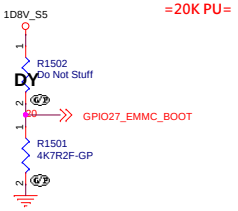
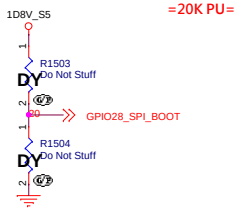
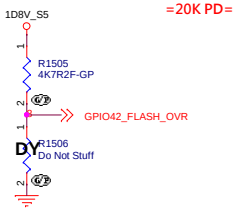
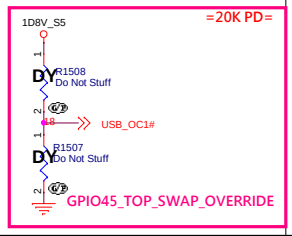
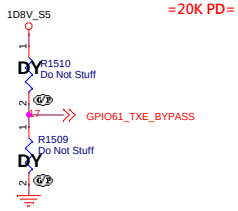
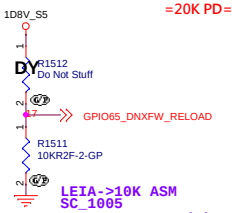
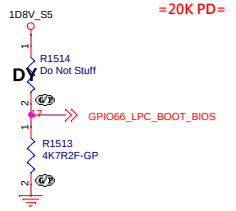
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

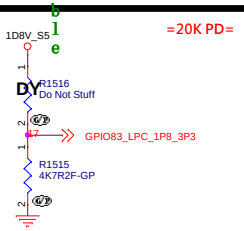
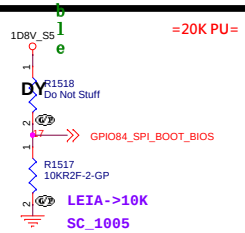
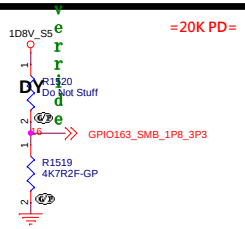
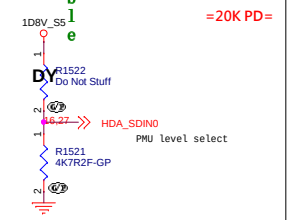
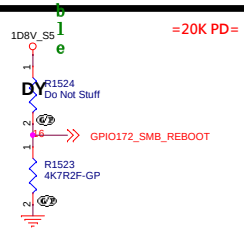
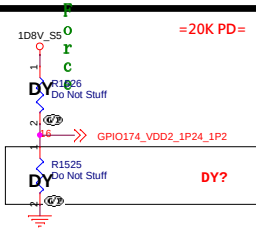
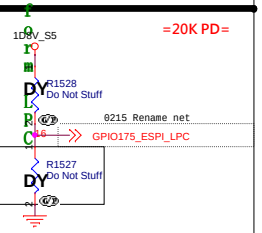
Title: *DDR (RSVD) (SODIMM3_SODIMM4)*

Size	Document Number	Rev
A4	LS1511G	-1M

Date: Friday, December 27, 2019 Sheet 14 of 106

SSID = STRAP

GPIO	GPIO_27	GPIO_28	GPIO_42	GPIO_45	GPIO_61	GPIO_65	GPIO_66
Schematic							
High	Enable =default=	Enable =default=	Override Normal	Enable =debug=	Enable	Force	Boot form LPC
Low	Disable 0213 Change setting	Disable	Normal	Disable =default=	Disable =default=	Normal =default=	Normal =default=

GPIO	GPIO_83	GPIO_84	GPIO_163	GPIO_168	GPIO_172	GPIO_174	GPIO_175
Schematic							
High	Buffer set 1.8v	Disable boot from SPI	1.8v	1.8v	Enable	1.24v	eSPI mode
Low	Buffer set 3.3v =default=	Enable =default=	3.3v =default=	3.3v =default=	Disable =default=	1.20v =default=	LPC mode =default=

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_27	GPIO_27	Allow eMMC as a boot source	20K PU	1=enable (default); 0=disable; If platform is using SPI as the boot device, then provide a pull-down for this strap to disable eMMC
GPIO_28	GPIO_28	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable ***Note:*** If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI.
GPIO_42	MDSI_A_TE	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override ***Note:*** This strap enables the platform to override security features in the SPI.
GPIO_45	USB2_OC1_N	Top swap override	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_61	SIO_UART0_TXD	Enable TXE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) ***Note:*** This strap tells TXE 3.0 to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of TXE3.0 before the first patch point this strap enabled the platform tell TXE 3.0 to bypass the ROM causing the issue and go to the patch space instead.

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_174	AVS_M_CLK_AB2	VDD2 1.24V vs. 1.20V select	20K PD	1=VDD2 is 1.24V; 0=VDD2 is 1.20V (default)
GPIO_175	AVS_M_DATA_2	eSPI vs. LPC	20K PD	1=eSPI mode; 0=LPC mode (default) Note: The default for A0 will be eSPI due to a bug on LPC.

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_65	SIO_UART2_TXD	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) ***Notes:*** 1. DnX: Download and Execute 2. This strap is a recovery strap for corrupted FW image. This strap will force TXE3.0 to execute a "Download and Execute" (DnX) flow, where it would fetch firmware from a USB stick and re-flash a USB.TXE can do it for BIOS part of FW, but if TXE FW itself is corrupted we need this strap.
GPIO_66	SIO_UART2_RTS_N	LPC boot BIOS strap	20K PD	1=boot from LPC; 0=do not boot from LPC (default) ***Note:*** The board should strap this low and do not use otherwise
GPIO_83	SIO_SPI_0_TXD	LPC 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_84	SIO_SPI_2_CLK	Allow SPI as a boot source	20K PU	1=disable 0=enable (default)
GPIO_163	AVS_I2S1_WS_SYNC	SMBus 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_164	AVS_I2S1_SDI	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_168	AVS_HDA_SDI	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_172	AVS_M_CLK_B1	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Platforms should strap this LOW. Functionality is handled by the PMC.

LS1511G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(STRAP)

Size: Custom | Document Number: LS1511G | Rev: -1M

Date: Friday, December 27, 2019 | Sheet 15 of 106

SSID = PCH

SPI ROM

SPI_MISO_ROM 25
SPI_MOSI_ROM 25
SPI_WP_ROM 25
SPI_HOLD_ROM 25
SPI_CS_CPU_N0 25
SPI_CLK_ROM 25

EMMC

EMMC_RCLK 63
EMMC_CLK 63
EMMC_D0 63
EMMC_D1 63
EMMC_D2 63
EMMC_D3 63
EMMC_D4 63
EMMC_D5 63
EMMC_D6 63
EMMC_D7 63
EMMC_CMD 63
EMMC_RST# 63

STRAP

GPIO163_SMB_1P8_3P3 15
GPIO172_SMB_REBOOT 15
GPIO174_VDD2_1P24_1P2 15
GPIO175_ESPI_LPC 15

LPC_CLK_KBC 24
LPC_CLK_DBG 68

HDA_SYNC 27
HDA_BCLK 27
HDA_SDO 27
HDA_SDIN0 15,27

CPU1G — 7 OF 13 — GEMINI-LAKE-GP

AUDIO-AVS
C26 AVS_I2S0_MCLK
B25 AVS_I2S0_BCLK
C25 AVS_I2S0_WS_SYNC
C24 AVS_I2S0_SDI GPIO_159 / Delay Vref switch
B23 AVS_I2S0_SDO

GPIO163_SMB_1P8_3P3
M23 AVS_I2S1_MCLK
L21 AVS_I2S1_BCLK
J21 AVS_I2S1_WS_SYNC GPIO_163 / SMBus 1.8v / 3,3v mode
M21 AVS_I2S1_SDI GPIO_164 / Stall boot FSM for debug
P23 AVS_I2S1_SDO

HDA_BCLK_PCH A22 AVS_HDA_BCLK
HDA_SYNC_PCH C23 AVS_HDA_WS_SYNC
HDA_SDIN0 B21 AVS_HDA_SDI GPIO_168 / PMU 1.8v 3.3v mode
HDA_SDO_PCH C22 AVS_HDA_SDO
TP1601 1 HDA_CODEC_RST# C21 AVS_HDA_RST#

GPIO172_SMB_REBOOT B19 AVS_DMIC_CLK_A1
C20 AVS_DMIC_CLK_B1 GPIO_172 / SMbus no reboot
GPIO174_VDD2_1P24_1P2 C19 AVS_DMIC_DATA_1
GPIO175_ESPI_LPC C18 AVS_DMIC_CLK_AB2 GPIO_174 / VDD2 1.24v, 1.2v mode
A18 AVS_DMIC_DATA_2 GPIO_175 / eSPI, LPC mode

eMMC
EMMC_CLK J13 EMMC_CLK
EMMC_RCLK L15 EMMC_RCLK
EMMC_D0 M19 EMMC_D0
EMMC_D1 H19 EMMC_D1
EMMC_D2 J19 EMMC_D2
EMMC_D3 P17 EMMC_D3
EMMC_D4 P19 EMMC_D4
EMMC_D5 J15 EMMC_D5
EMMC_D6 L17 EMMC_D6
EMMC_D7 M17 EMMC_D7
EMMC_CMD M13 EMMC_CMD
EMMC_RST# U44 EMMC_RST#
TP1602 1 EMMC_PWR_EN# G51 EMMC_PWR_EN#
EMMC_RCOMP L13 EMMC_RCOMP

Layout Note: W/S=10/8, length <500 mil
R1605 200R2F-L-GP 0213 Rename net. Moving Res to CPU side

SDCARD
SDCARD_CLK L29
SDCARD_D0 M29
SDCARD_D1 P29
SDCARD_D2 M27
SDCARD_D3 P27
SDCARD_CMD L27
SDCARD_CD# L25
SDCARD_LVL_WP P25
SDCARD_PWR_DWN# L23
SDCARD_RCOMP J25

1.8V / 3.3V
1.8V
1.8V / 3.3V
1.8V

intel PDG (567247 ver1.2)
Deleted SD Card Section

LPC/eSPI
LPC_CLKOUT0 C37
LPC_CLKOUT1 A38
LPC_AD0 A34
LPC_AD1 C34
LPC_AD2 B35
LPC_AD3 C35
LPC_CLKRUN# C33
LPC_FRAME# B33
LPC_SERIRQ B37

RN1601 SRN33J-5-GP-U
LPC_CLK_KBC_R 1 4 LPC_CLK_KBC
LPC_CLK_DBG_R 2 3 LPC_CLK_DBG
LPC_AD_CPU_P0
LPC_AD_CPU_P1
LPC_AD_CPU_P2
LPC_AD_CPU_P3
LPC_CLKRUN#_CPU
LPC_FRAME#_CPU
LPC_SERIRQ_CPU

0213
Rename LPC_SERIRQ PIN to LPC_SERIRQ_CPU
Rename LPC_CLKRUN# PIN to LPC_CLKRUN_CPU#

FAST_SPI
FST_SPI_CLK B29
FST_SPI_MOSI_IO0 B31
FST_SPI_MISO_IO1 C30
FST_SPI_IO2 A30
FST_SPI_IO3 C29
FST_SPI_CS0# C31
FST_SPI_CS1# C32

SPI_CLK_CPU R1604 1 0R402-DB-GP-U SPI_CLK_ROM
SPI_SI_CPU R1611 1 0R402-DB-GP-U SPI_MOSI_ROM
SPI_SO_CPU R1612 1 0R402-DB-GP-U SPI_MISO_ROM
SPI_WP_CPU R1613 1 2 0R402-DB-GP-U SPI_WP_ROM
SPI_HOLD_CPU R1614 1 2 0R402-DB-GP-U SPI_HOLD_ROM
SPI_CS_CPU_N0

LPC_SERIRQ 24 R1621 1 2 0R402-DB-GP-U LPC_SERIRQ_CPU
LPC_FRAME# 24,68 R1623 1 2 0R402-DB-GP-U LPC_FRAME#_CPU
LPC_AD0 24,68 R1622 1 2 0R402-DB-GP-U LPC_AD_CPU_P0
LPC_AD1 24,68 R1617 1 2 0R402-DB-GP-U LPC_AD_CPU_P1
LPC_AD2 24,68 R1620 1 2 0R402-DB-GP-U LPC_AD_CPU_P2
LPC_AD3 24,68 R1619 1 2 0R402-DB-GP-U LPC_AD_CPU_P3

3D3V_S0
EMMC_PWR_EN# R1630 1 2 20KR2J-L2-GP
LPC_CLKRUN#_CPU 24 LPC_CLKRUN#_CPU R1625 2 1 10KR2J-L-GP
LPC_FRAME#_CPU R1631 2 DY 1 Do Not Stuff
LPC_SERIRQ_CPU R1632 2 DY 1 Do Not Stuff

reserve pull high resistor R1631.R1632 for leakage

HDA_BCLK_PCH R1633 1 10R2J-2-GP HDA_BCLK
HDA_SYNC_PCH R1634 1 10R2J-2-GP HDA_SYNC
HDA_SDO_PCH R1635 1 10R2J-2-GP HDA_SDO

VENDOR SUGGESTION

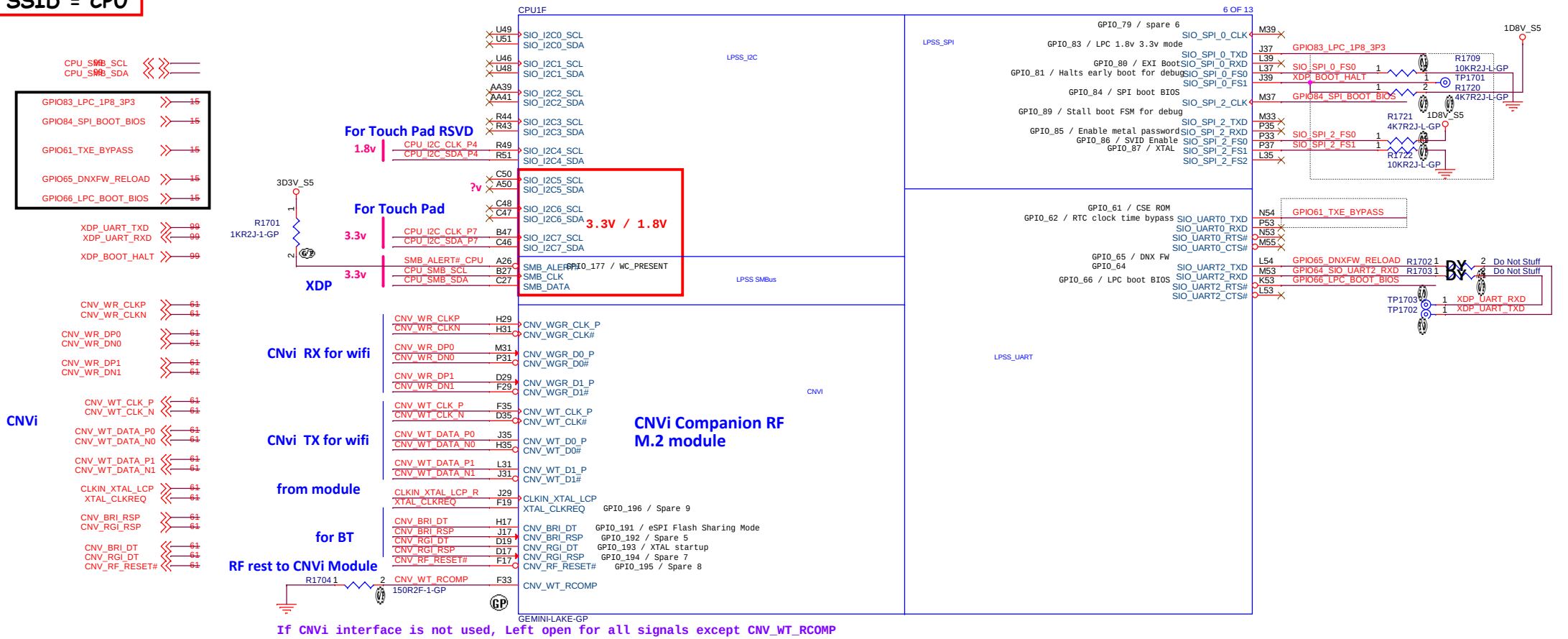
LPC_CLK_KBC
DY C1601 Do Not Stuff

LS1511G

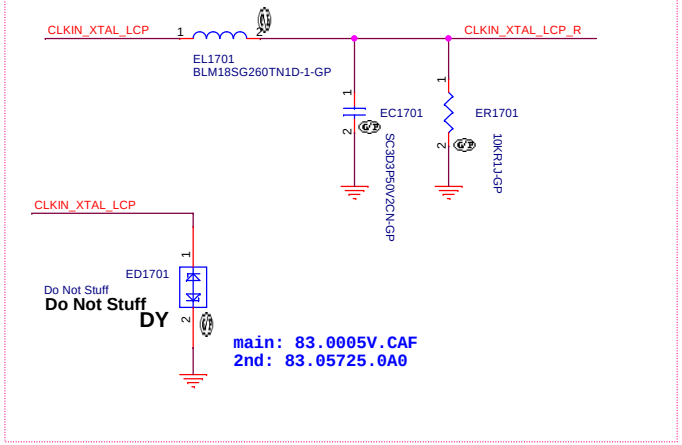
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (AVS/EMMC/SD/LPC/ESPI)
Size: A3 | Document Number: LS1511G | Rev: -1M
Date: Friday, December 27, 2019 | Sheet 16 of 106

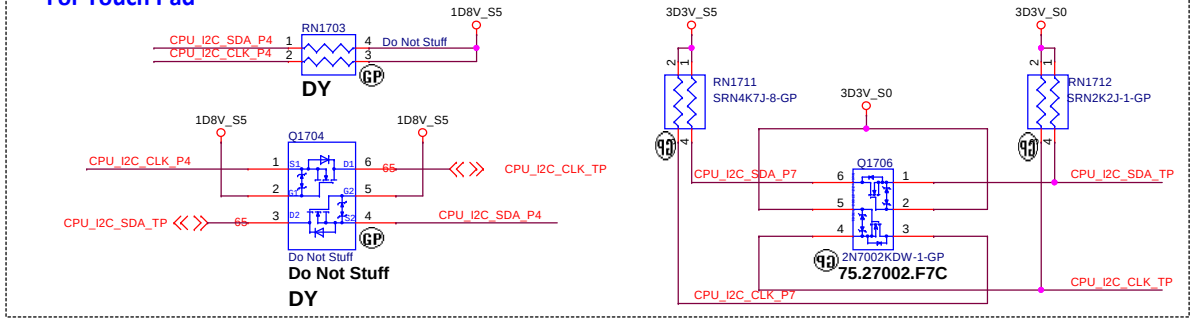
SSID = CPU

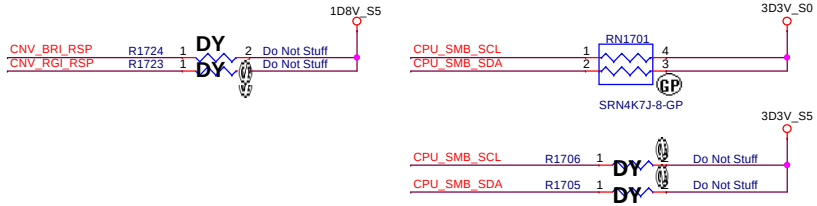


Close to CPU



For Touch Pad





LS1511G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (I2C/SMB/SPI/UART/CNVI)**

Size	Document Number	Rev
A3	LS1511G	-1M

Date: Friday, December 27, 2019 Sheet 17 of 106

SSID = PCH

USB3.0 Type A Port1

USB3.0 Type A Port2

BT

Camera S150

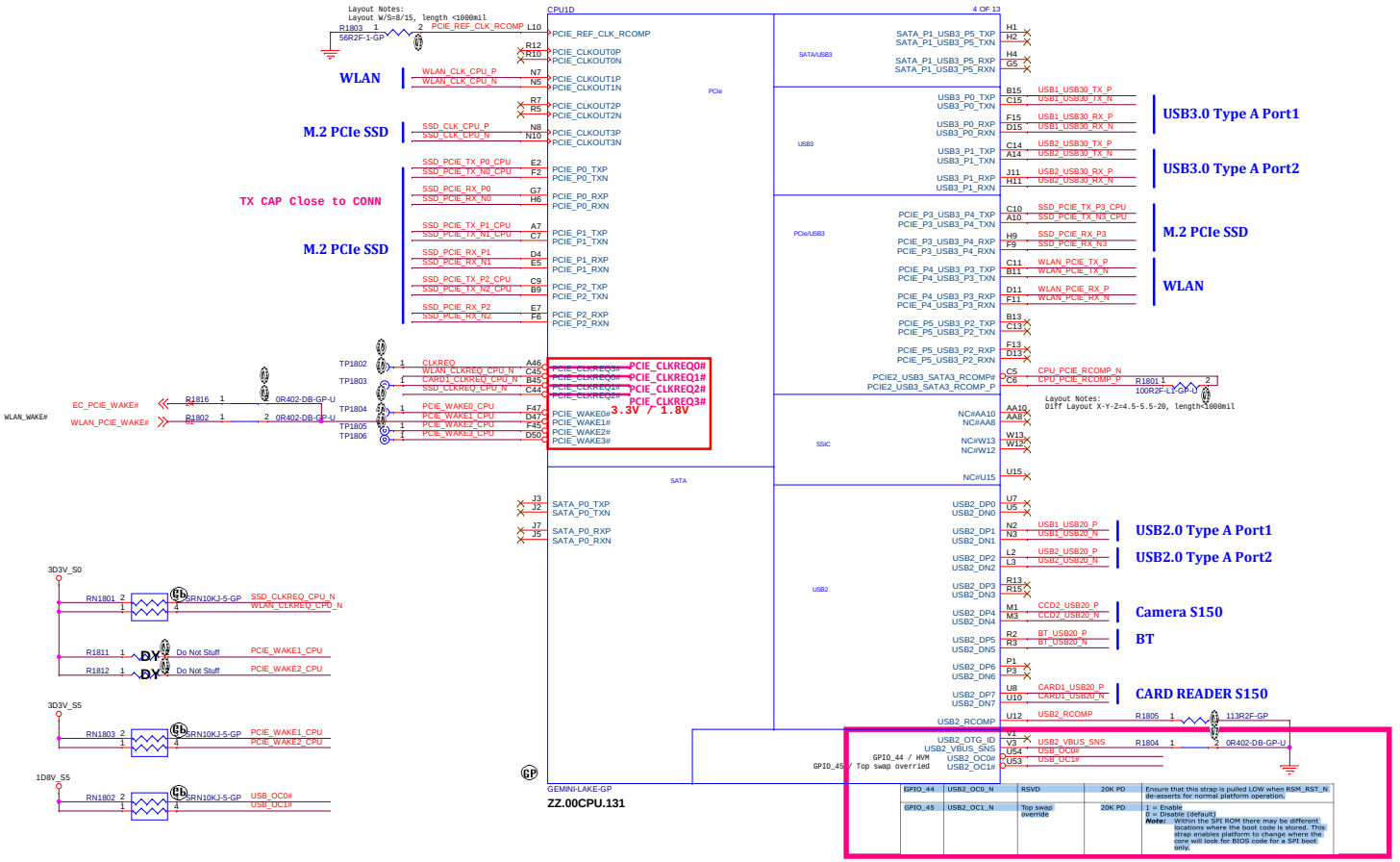
CARD READER

USB2.0 Type A Port1

USB2.0 Type A Port2

WLAN

M.2 PCIe SSD



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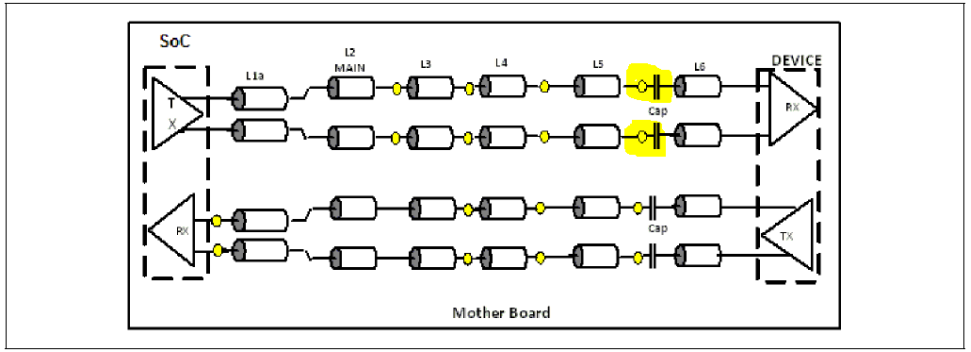
PCIE_WAKE[3:0]_N	I	V1P8/V3P3	PCIe* Wake Signals
PCIE_CLKREQ[3:0]_N	I/O	V1P8/V3P3	**PCIE Clock Request**: Used for devices that need to request one of the four output clocks. Each clock request maps to the matching clock output (for example, PCI_CLKREQ[0] maps to PCIE_CLKP/N[0]). These signals are multiplexed and may be used by other functions.

Figure 9-8. PCI Express* Device Down Topology



LS1511G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB3/USB2)

Size: A2 | Document Number: LS1511G | Rev: -1M

Date: Friday, December 27, 2019 | Sheet 18 of 106

SSID = PCH

CPU_I2C_SDA_PMIC 46
CPU_I2C_SCL_PMIC 46
PLT_RST# 24,40,61,63,68,99
PM_PWRBTN# 24,99
PM_SLP_S0# 46
PM_SLP_S3# 24,40,46
PM_SLP_S4# 24,40,46

SYS_PWROK 24
PMIC_PWRGD 40,46
RTCRST_ON 24
PMIC_THERMTRIP# 24,40,46
PROCHOT#_CPU 24,40,46
PM_SUSCLK 61

PM_RSMRST# 99

PM_RSTBTN# 99

APS debug port

TPAD14-OP-GP APS1901 1 PM_SLP_S3#
TPAD14-OP-GP APS1902 1 PM_SLP_S4#
TPAD14-OP-GP APS1903 1 RTC_RST#
TPAD14-OP-GP APS1905 1 PM_SLP_S0#

follow LS1511A AFTP1702

32kHZ for CNVi pin50

TP1901

1.8v

CPU1H

8 OF 13

PMC_I2C_SCL
PMC_I2C_SDA
PMC_SPI_CLK
PMC_SPI_FS0
PMC_SPI_FS1
PMC_SPI_FS2
PMC_SPI_RXD
PMC_SPI_TXD

PMU_PLTRST#
PMU_PWRBTN#
PMU_SLP_S0#
PMU_SLP_S3#
PMU_SLP_S4#
SUSPWRDNACK
PMU_BATLOW#
PMU_RSTBTN#
PMU_SUSCLK
SUS_STAT#

SVID0_DATA
SVID0_CLK
SVID0_ALERT_B

NC#D1
NC#D2
NC#A54
NC#C54

iCLK
RTC
PMC
PMU
Thermal
SVID
Spare
Misc

OSC_CLK_OUT_0
OSC_CLK_OUT_1
OSCIN
OSCOUT
RTC_X1
RTC_X2
VCC_RTC_EXTPAD
INTRUDER
SOC_PWROK
RSM_RST#
RTC_TEST#
RTC_RST#
THERMTRIP#
PROCHOT#
NC#AG43
NC#H53
NC#AG44
NC#H55
NC#A4
NC#BH1
SKTOCC#
NC#F37
NC#BL2
NC#BL3
NC#BL53
NC#C2
NC#C3
NC#R41

0214
Correct Net name

XTL_19D2M_X1_CPU
XTL_19D2M_X2_CPU
XTL_32K_X1_CPU
XTL_32K_X2_CPU
BVCCRTC_EXTPAD
INTRUDER
SOC_PWROK_CPU
PM_RSMRST#
RTC_TEST#
RTC_RST#
PMIC_THERMTRIP#
PROCHOT#_CPU_R

need check with SW

GEMINI-LAKE-GP

R1910 1 2 0R402-DB-GP-U PROCHOT#_CPU

3D3V_RTC_AUX

RN1905 SRN20KJ-1-GP
RTC_RST#
RTC_TEST#
C1901 SC1U10V2KX-L1-GP
C1902 SC1U10V2KX-L1-GP
G1901 GAP-OPEN

Layout Note:
place on bottom side

3D3V_S5

RN1902 SRN10KJ-5-GP PM_PWRBTN# SUS_PWRDN_ACK
R1922 100KR2J-1-GP PM_BATLOW#
RN1901 SRN10KJ-5-GP PM_RSTBTN# PM_SUS_STAT#

3D3V_RTC_AUX

R1905 330KR2J-L1-GP INTRUDER

1D8V_S5

R1901 DY Do Not Stuff PROCHOT#_CPU
R1924 DY Do Not Stuff PLT_RST#
R1912 100KR2J-1-GP PM_RSMRST#
C1905 SCD1U16V2KX-L-GP BVCCRTC_EXTPAD

32.768 kHz

XTL_32K_X1_CPU
XTL_32K_X2_CPU
R1903 10MR2J-L-GP
X1901 XTAL-32D768KHZ-88-GP
082.30003.0191
C1903 SC15P50V2JN-L-GP
C1904 SC15P50V2JN-L-GP

	C1903	C1904
EPSON 082.30003.0191	15pF	15pF
SEIKO 082.30003.0301	15pF	15pF
TXC 082.30003.0231	15pF	15pF

19.2 MHz

XTL_19D2M_X1_CPU
XTL_19D2M_X2_CPU
DEL resistor*2_-1
R1917 200KR2J-L-GP
X1902 XTAL-19D2MHZ-32-GP
082.30001.0181
C1906 SC15P50V2JN-L-GP
C1907 SC15P50V2JN-L-GP

all S0 power rail ok
(PCH_PWROK delay 1D05V_S0 between 5~100ms)
and SYS_PWROK for discrete power solution

SOC_PWROK_CPU R1920 DY Do Not Stuff SYS_PWROK
R1918 100KR2J-1-GP
R1919 0R402-DB-GP-U PMIC_PWRGD
0214
Following NBA APL

	C1906	C1907
HARMONY 082.30001.0181	15pF	15pF
TXC 082.30001.0171	15pF	15pF
HOSONIC 082.30039.0051	15pF	15pF

RTC_TEST#
RTCRST_ON
RTC_RST#
Q1901
R1904 100KR2J-4-GP
2N7002KDW-1-GP
75.27002.F7C

3D3V_S5

R1930 20KR2F-L-GP PMIC_PWRGD
R1931 DY Do Not Stuff

3D3V_AUX_S5

R1908 100KR2J-4-GP
R1902 10KR2J-L-GP
Q1902
2N7002KDW-1-GP
75.27002.F7C
3V_5V_POK#
PM_RSMRST#
3V_5V_POK_C
R1906 0R402-DB-GP-U 24 RSMRST#_KBC
R1915 0R402-DB-GP-U 40,46 3V_5V_PWRGD
R1921 DY Do Not Stuff 24,46 PMIC_RSMRST#
EC1908 Do Not Stuff DY

LS1511G

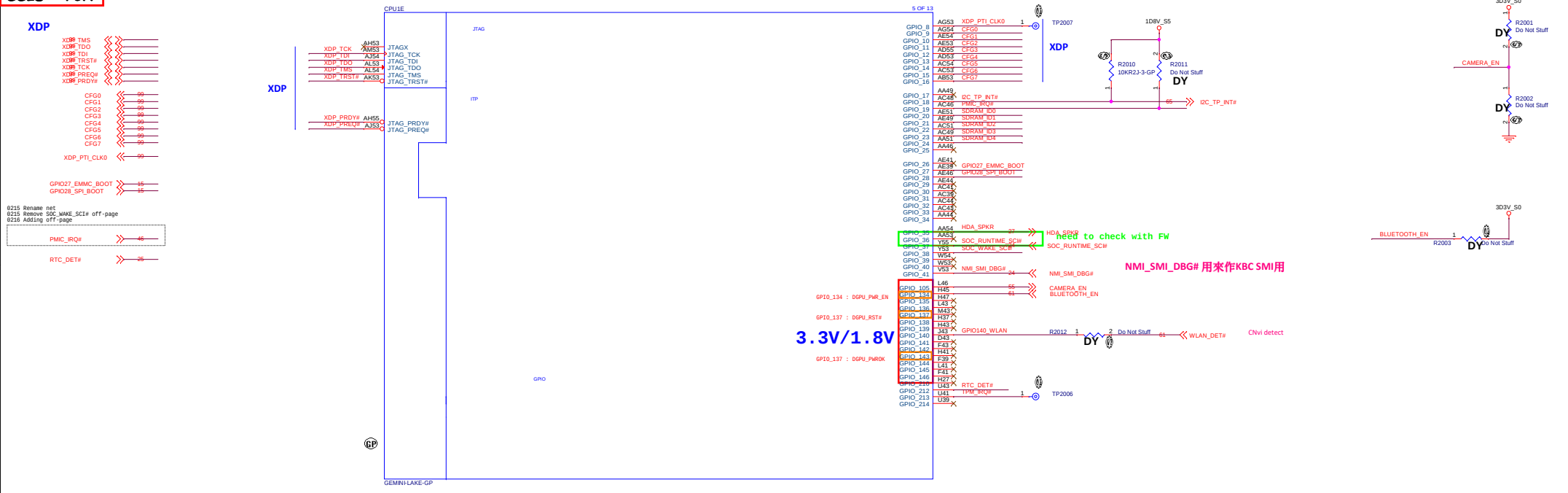
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

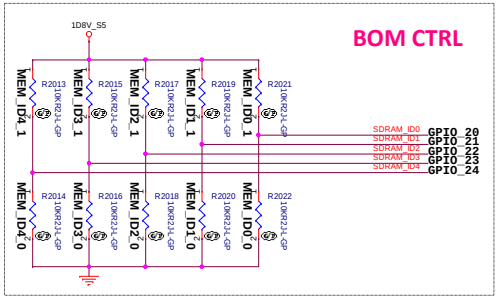
Title: CPU (PMU/PMC/SVID/RTC/MISC)

Size: A3 | Document Number: LS1511G | Rev: -1M

Date: Friday, December 27, 2019 | Sheet 19 of 106

SSID = PCH





EVT/FVT/SIT/SVT:

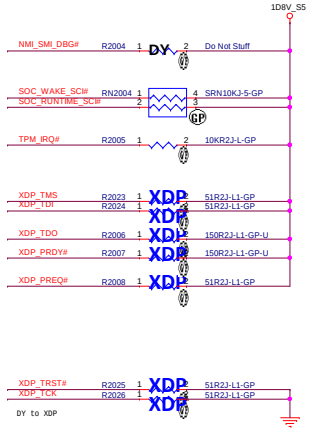
Memory Configuration	Memory Supplier	
00: 4GB 01: 8GB 10: 16GB (Reserve) 11: 8GB	00: Samsung 01: Micron 10: SK Hynix 11: (Reserve)	0: 2666 1: 3200

GPIO_23	GPIO_22	GPIO_21	GPIO_20	GPIO_24								
SDRAM_ID3	SDRAM_ID2	SDRAM_ID1	SDRAM_ID0	SDRAM_ID4	Vendor ID	Supplier	Density	Vendor PN				
0	0	0	0	0	0	SAMSUNG	4GB	K4A8G165WC-BCTD	SM30N76502	SDPx16 8Gb	2666	SKU1.6
0	1	0	0	0	1	SAMSUNG	8GB					SKU5
0	0	0	0	1	8	SAMSUNG	4GB		SM30N76632	SDPx16 8Gb	3200	
0	1	0	0	1	9	SAMSUNG	8GB					
0	0	0	1	1	4	MICRON	4GB	MT40A512M16TB-062E	SM30N76570	SDPx16 8Gb	3200	SKU2
0	1	0	1	1	5	MICRON	8GB					SKU3.7
0	0	0	1	0	6	MICRON	4GB					
0	1	0	1	0	7	MICRON	8GB					
0	0	1	0	0	2	SK HYNIX	4GB	H5AN8G6NCJR-VKC	SM30N76518	SDPx16 8Gb	2666	
0	1	1	0	0	3	SK HYNIX	8GB	H5AN8G6NCJR-VKC	SM30N76546	DDPx16 16Gb	2666	SKU4
0	0	1	0	1	10	SK HYNIX	4GB		SM30N76639	SDPx16 8Gb	3200	
0	1	1	0	1	11	SK HYNIX	8GB		SM30N76640	DDPx16 16Gb	3200	

0=L, 1=H

1	1	0	0	1	SAMSUNG	8GB		SM30N76504	DDP	3200	
1	1	0	1	1	MICRON	8GB		SM30E51324	DDP	3200	

SIT	SIT-2
SKU4.8.9	
SKU1	
SKU3.6.7	SKU10
SKU2.5.10	
	SKU1,8,9
	SKU2,3,6
	SKU4,5,7



LS1511G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (GPIO/JTAG/ITP)

Size: A2 | Document Number: LS1511G | Rev: -1M

Date: Friday, December 27, 2019 | Sheet 20 of 106

Blanking

LS1511G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (RSVD)***

Size	Document Number	Rev
A4	LS1511G	-1M

Date: Friday, December 27, 2019 Sheet 21 of 106

Blanking

LS1511G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (RSVD)*

Size	Document Number	Rev
A4	LS1511G	-1M

Date: Friday, December 27, 2019 Sheet 22 of 106

SSID = CPU

LS1511G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
Custom	LS1511G	-1M

Date: Friday, December 27, 2019 Sheet 23 of 106

SSID = KBC

Model_ID_BOM Ctrl

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
LS1511G	100.0K	10.0K 64.10025.6DL	3.0V
LS1514G	100.0K	20.0K 64.20025.1DL	2.75V
NA	100.0K	33.0K 64.33025.1DL	2.48V
NA	100.0K	47.0K 64.47025.6DL	2.24V
NA	100.0K	64.9K 64.64925.6DL	2.0V
NA	100.0K	76.8K 64.76825.6DL	1.87V
NA	100.0K	215.0K 64.21535.6DL	1.048V

SKU_ID

-1_1229

PCB VERSION

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
-1M	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

PCB_ID

SPEC: ADT PWR Detection Function V1 3

Prevent BIOS data loss solution

Nuvoton KBC PSL Power Switched Logic

1.Enter PSL mode (Entry S5 after 10sec) :
3D3V_AUX_KBC : OFF (KBC PWR supply)

2.At PSL mode (SPEC: S5<10mW)

PSL mode(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
H1	Low	OFF

PSL Wake(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Low	H1	ON

EC_GPIO47 High Active

NOVO button Fun define: one key to recover OS.

NOVO button wake KBC at PSL mode.		
KBC_NOVO_BTN#	KBC_PWRBTN_EC#	
Low	Low	

KBC_PWRBTN_EC#:Low
(1) 4sec: PWR Button shut down
(2) 8sec: KBC reset

EC GPIO PH

1.20180104
RN2403 change from 66.47236.04L 4k7 to 66.22236.04L 2k2 for SMBUS rise time and falling time fail

EC GPIO PL

R2418 ASM
R2420 DY
0607

NOTE:
Please be aware that the SPI interface trace length between PCH and EC should not exceed 650mils., The mismatch of SPI interface signals between EC and SPI flash should not exceed 500mils.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

NOTE:
PWM Signal :
1. If unused, select alternative GPIO function and enable internal pull-down.
2. Please measure and make sure that the rise time of VCC_POR is less than 10us.

1st_BATTERY / CHARGER

SB_Reserveed PD

Thermal VD

No support PECI

KBC PWR supply at PSL mode.

main: 75.05125.07D Amazing
2nd: 075.52215.007D NXP

071.00285.0C0G

R2431 close to Pin103

Wistron Corporation
2Fl, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ECIO (KBC NPCE285)
Size: A1 | Document Number: LS1511G | Rev: -1M
Date: Friday, December 21, 2007 | Sheet 24 of 105

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

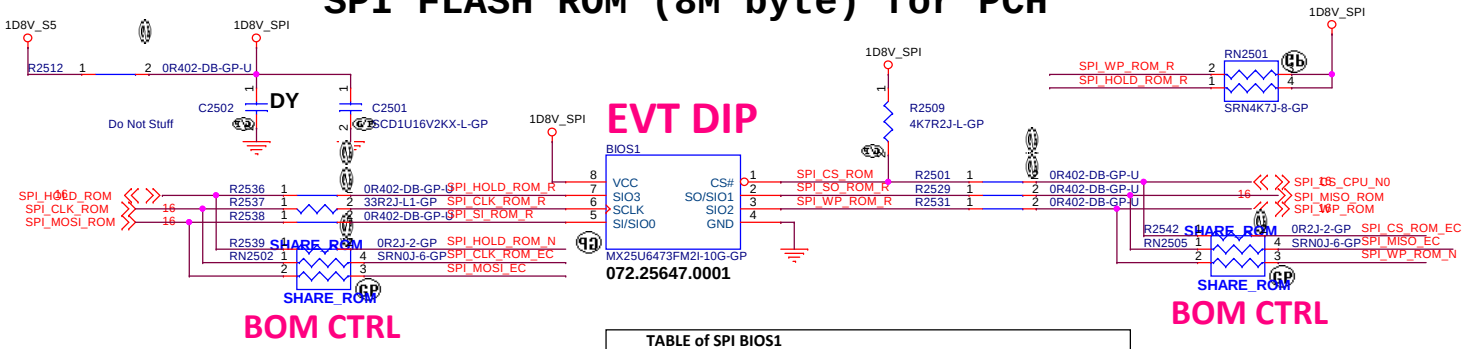
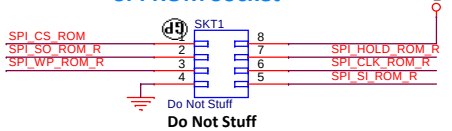


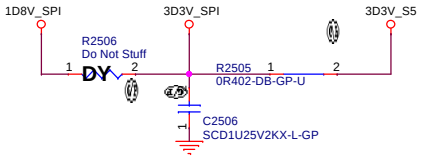
TABLE of SPI BIOS1		
VENDOR	P/N	Wistron P/N
MACRONIX	MX25U6473FM2I-10G	072.25647.0001
GIGADEVICE	GD25LB64CSIGR	072.02564.0A01

EVT ASM

Co-Layout Design on BIOS1

SPI ROM Socket





128k byte for FEROM

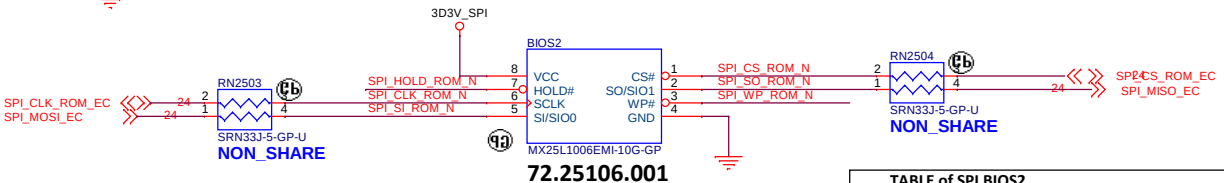
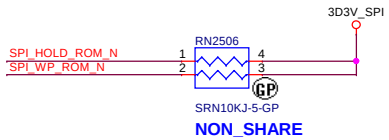


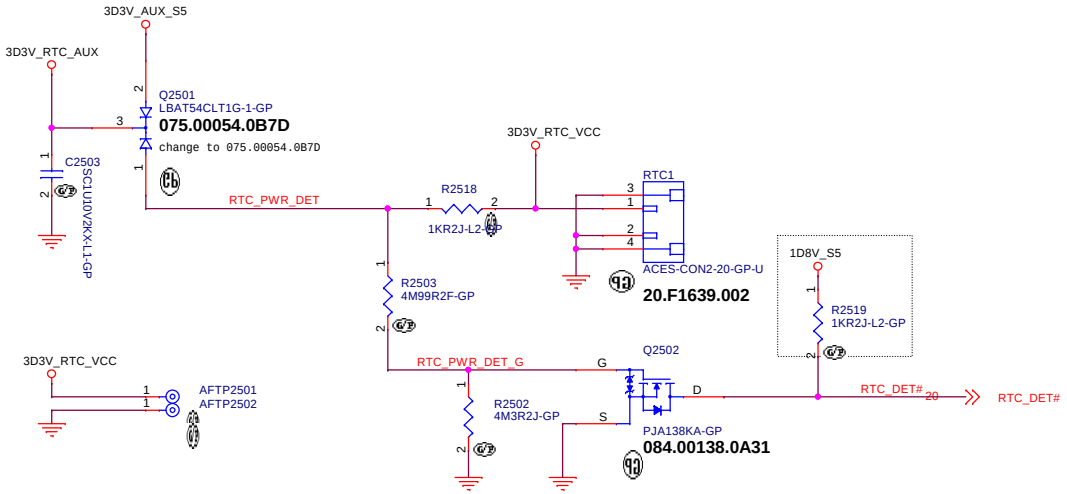
TABLE of SPI BIOS2		
VENDOR	P/N	Wistron P/N
MXIC	MX25L1006EMI-10G	72.25106.001
WINBOND	W25X10CLSNIG	72.02510.001
Giga Device	GD25D10CTIGR	072.25D10.0B0D



FEROM
EVT DIP

BIOS2 change from DY to stuff
SKT2 change to non-stuff_20190819_BCN

SSID = RBAT



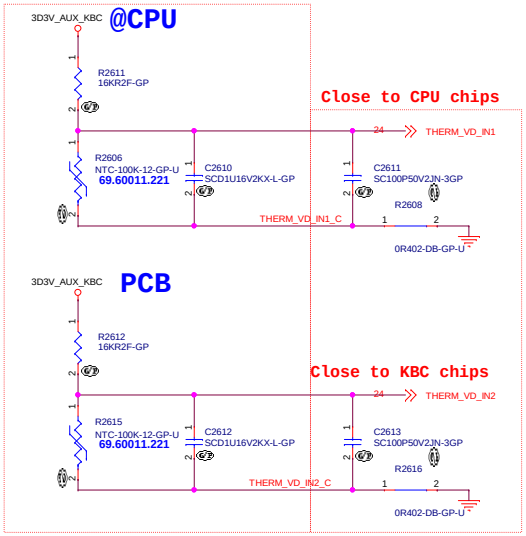
LS1511G

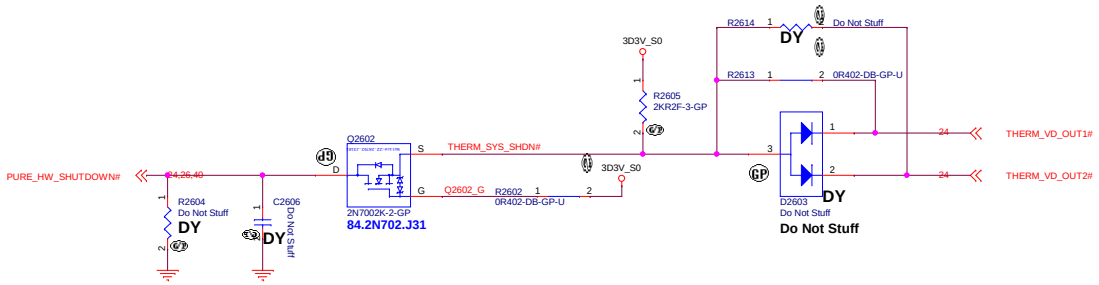
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Flash/RTC		
Size: A3	Document Number: LS1511G	Rev: -1M
Date: Friday, December 27, 2019	Sheet 25 of 106	

Main Func = Thermal Sensor

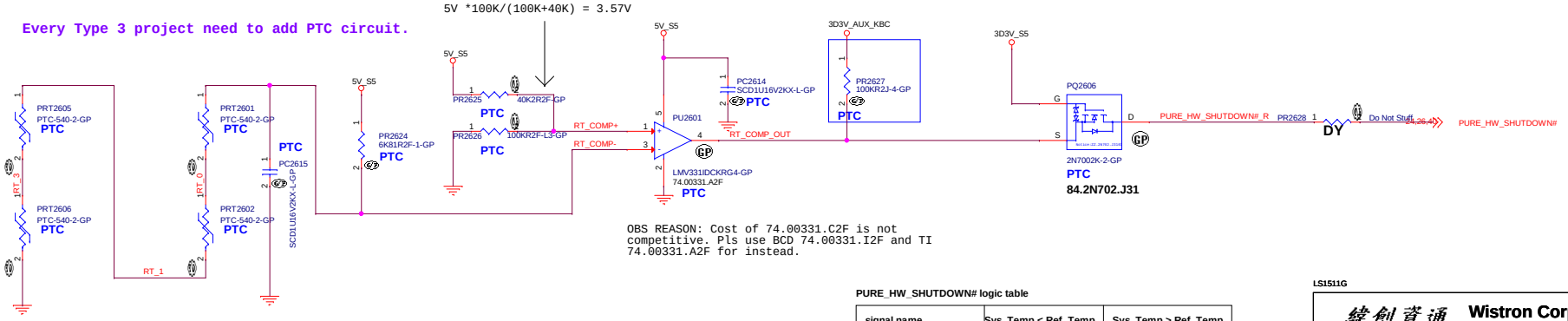
Close to Thermal sensor





PTC: BOM CTRL DY

Every Type 3 project need to add PTC circuit.



OBS REASON: Cost of 74.00331.C2F is not competitive. Pls use BCD 74.00331.I2F and TI 74.00331.A2F for instead.

PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low

LS1511G

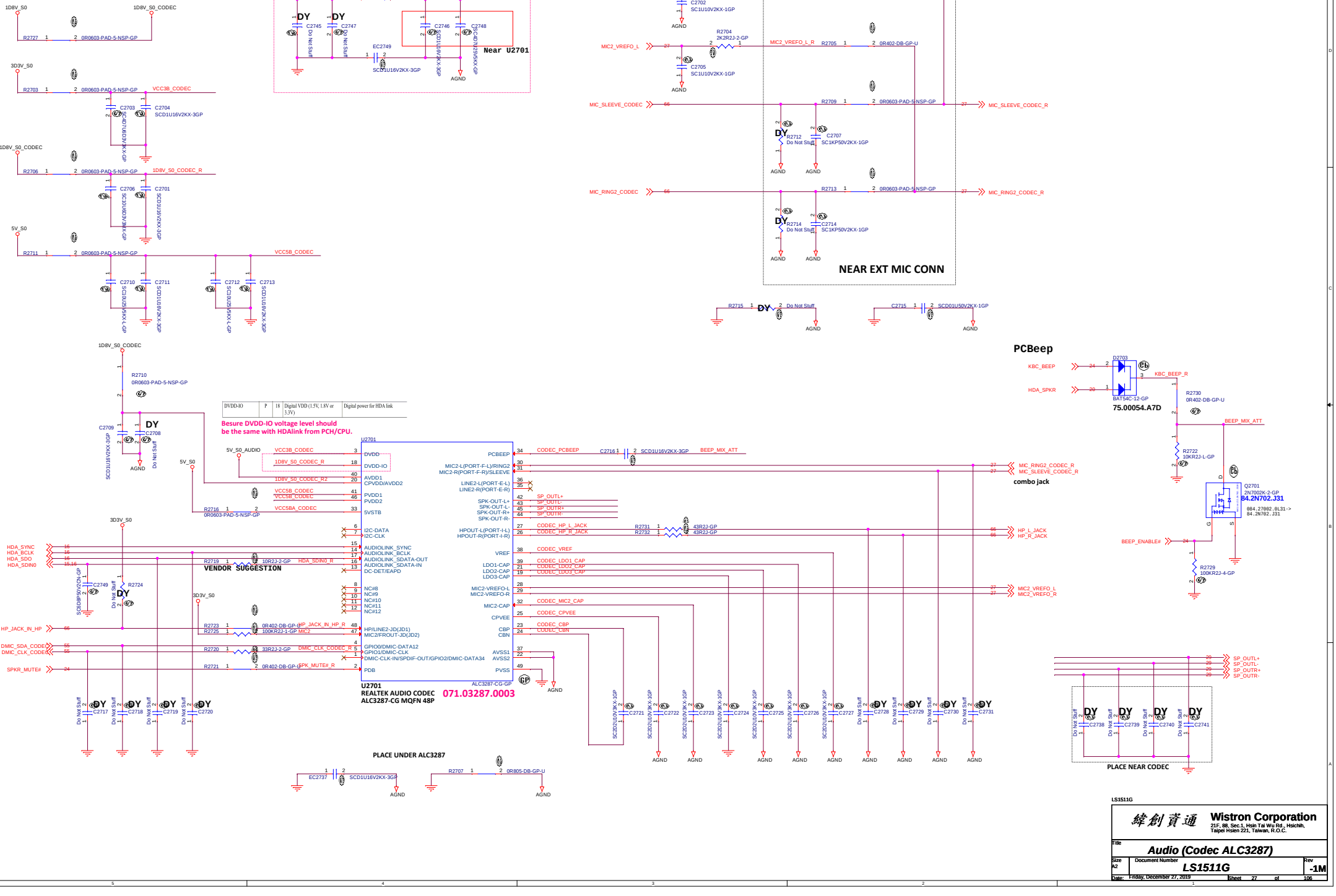
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (Thermal/Fan)

Size: Custom | Document Number: LS1511G | Rev: -1M

Date: Friday, December 27, 2019 | Sheet 26 of 106

AUDIO



LS1511G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio (Codec ALC3287)**

Size	Document Number	Rev
A2	LS1511G	-1M

Date: Friday, December 27, 2019 Sheet 27 of 106

Blanking

LS1511G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio (RSVD) (Audio AMP)***

Size	Document Number	Rev
A4	***LS1511G***	**-1M**

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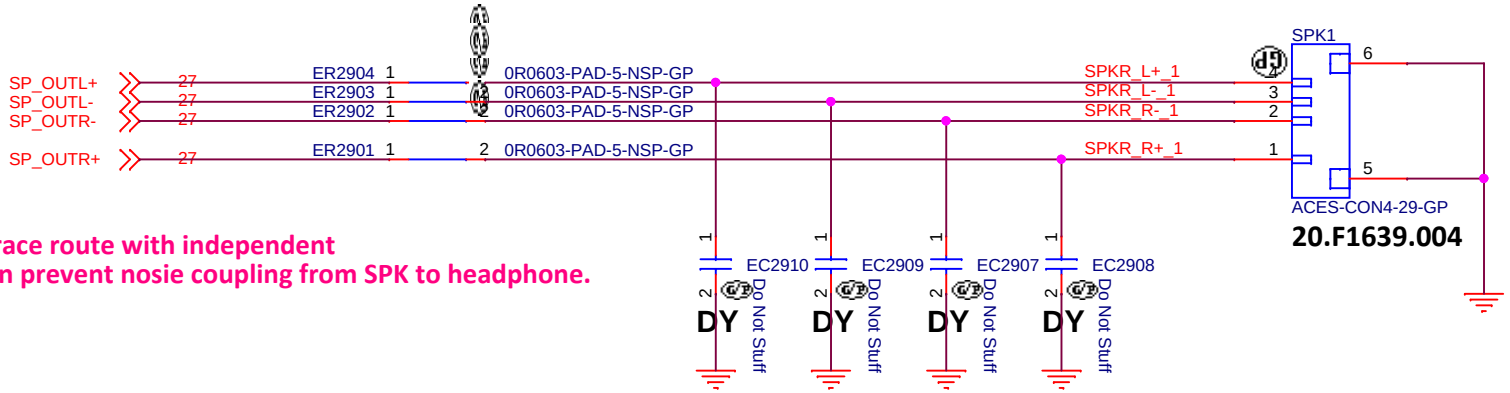
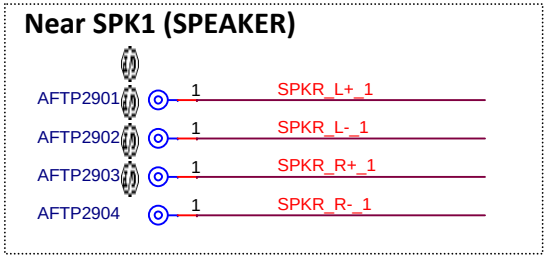
Speaker/Audio CONN



vendor,
If can, SPK trace route with independent
FPC cable can prevent nosie coupling from SPK to headphone.



Audio_Combo_Jack
IO BD

LS1511G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Audio (HP/SPK/MIC Jack)*	
Size A4	Document Number *LS1511G*	Rev -1M
Date: Friday, December 27, 2019	Sheet 29 of 106	

Blanking

LS1511G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Audio (RSVD)*		
Size: A4	Document Number: *LS1511G*	Rev: -1M
Date: Friday, December 27, 2019	Sheet 30 of 106	

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LS1511G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN (RSVD)***

Size	Document Number	Rev
A4	LS1511G	-1M

Date: Friday, December 27, 2019 Sheet 31 of 106

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LS1511G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

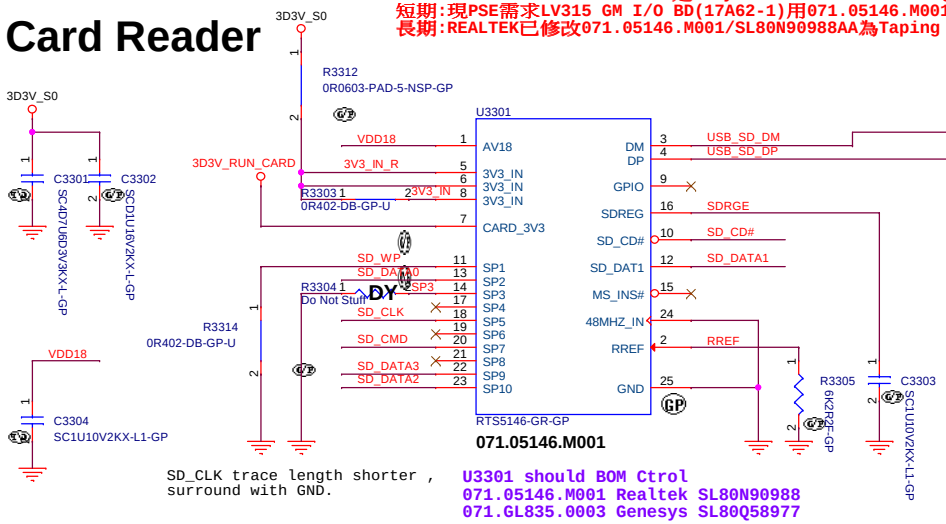
Title: ***LAN (RSVD)***

Size	Document Number	Rev
A4	LS1511G	-1M

Date: Friday, December 27, 2019 Sheet 32 of 106

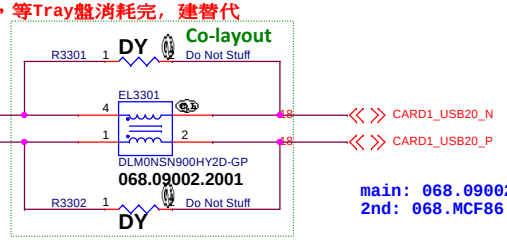
Card Reader

071.05146.M001/SL80N90988AA是Tray 071.GL835.0003/SL80Q58977AA是Taping
短期:現PSE需求LV315 GM I/O BD(17A62-1)用071.05146.M001/SL80N90988AA
長期:REALTEK已修改071.05146.M001/SL80N90988AA為Taping，等Tray盤消耗完，建替代

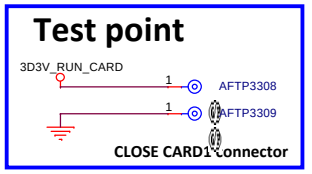


SD_CLK trace length shorter , surround with GND.

U3301 should BOM Ctrol
071.05146.M001 Realtek SL80N90988
071.GL835.0003 Genesys SL80Q58977



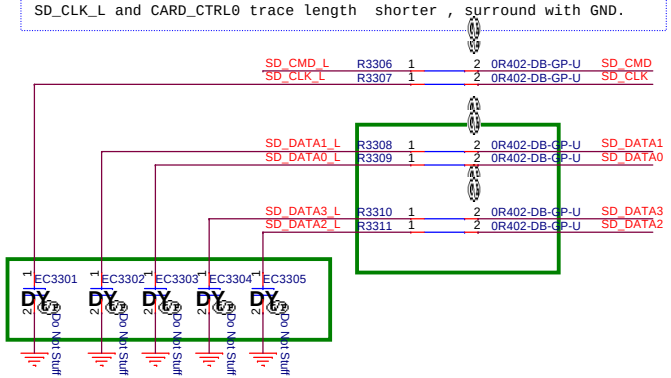
main: 068.09002.2001
2nd: 068.MCF86.2001



CARD DETECT SWITCH

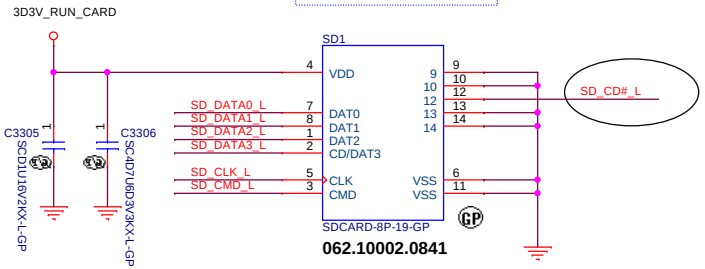
CARD (STATUS) / SWITH (CIRCUIT)	WITHOUT CARD	INSERTING CARD
DETECT SWICH	OPEN	CLOSE

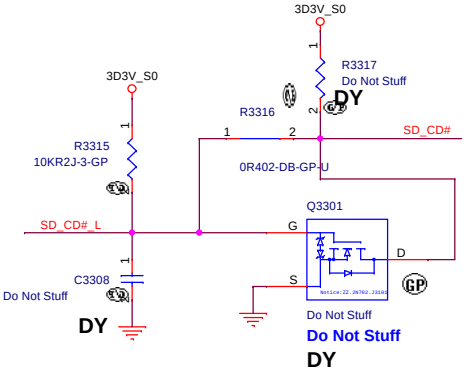
SD_CLK_L and CARD_CTRL0 trace length shorter , surround with GND.



SD_CLK_L and CARD_CTRL0 trace length shorter , surround with GND.

OPEN TYPE SD Socket





LS1511G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARDREADER (SDIO/SD Conn)

Size	Document Number	Rev
A3	LS1511G	-1M

Date: Friday, December 27, 2019 Sheet 33 of 106

Blanking

LS1511G

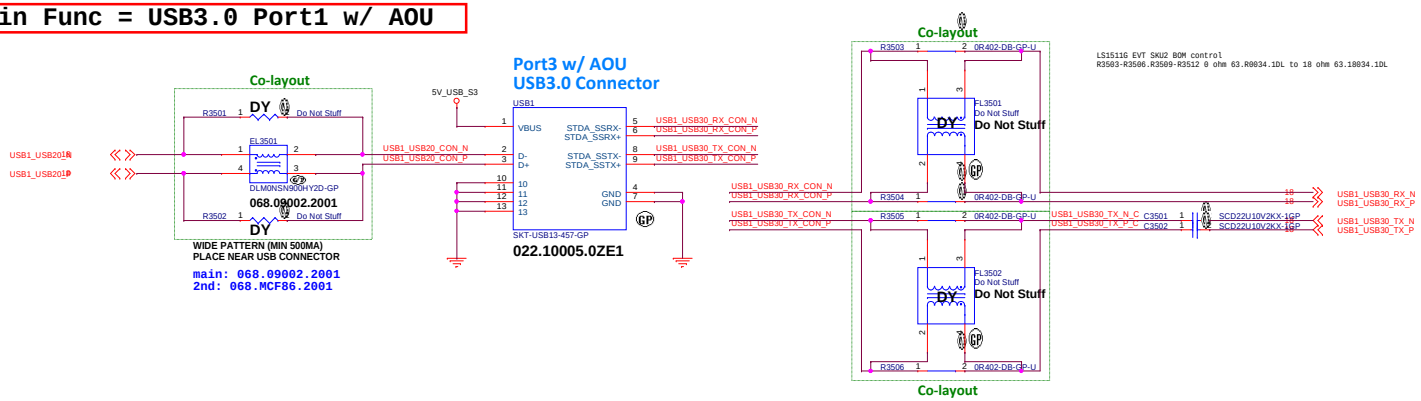
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (RSVD) (USB2.0 CONN)***

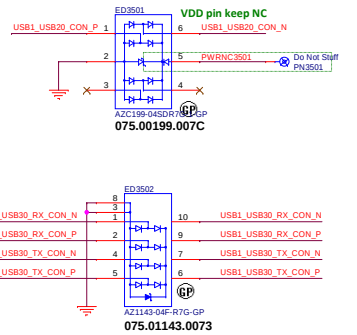
Size	Document Number	Rev
A4	LS1511G	-1M

Date: Friday, December 27, 2019 Sheet 34 of 106

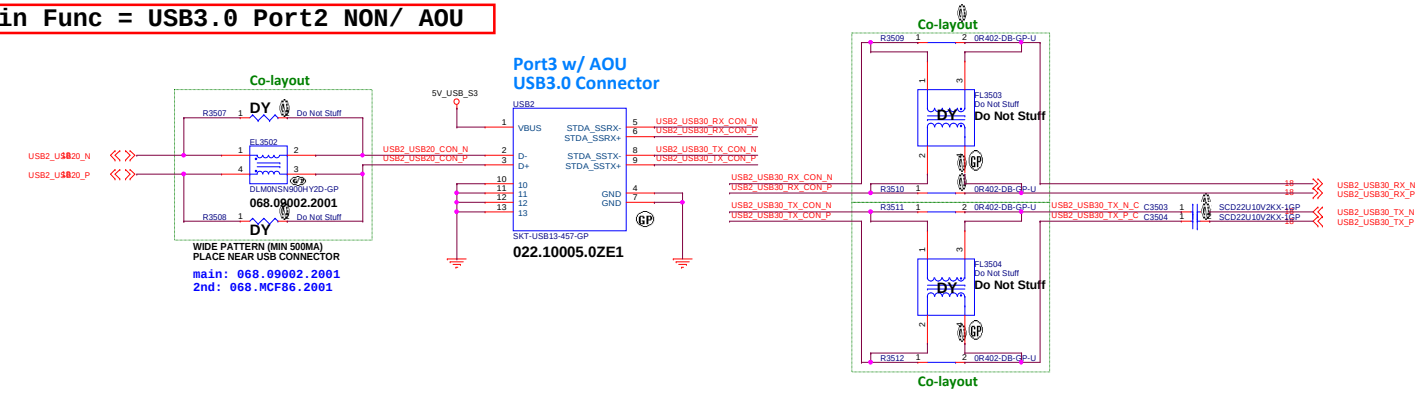
Main Func = USB3.0 Port1 w/ AOU



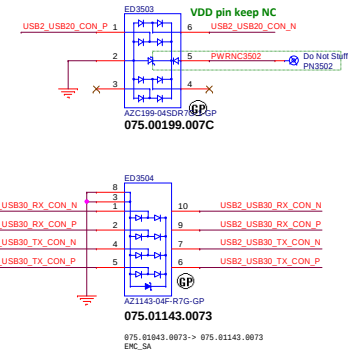
main: 075.00199.007C
2nd: 075.08105.007C



Main Func = USB3.0 Port2 NON/ AOU

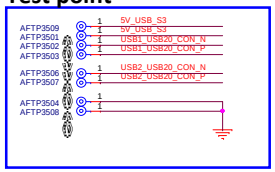


main: 075.00199.007C
2nd: 075.08105.007C



075.01043.0073-> 075.01143.0073
EMC_SA

Test point



LS1511G

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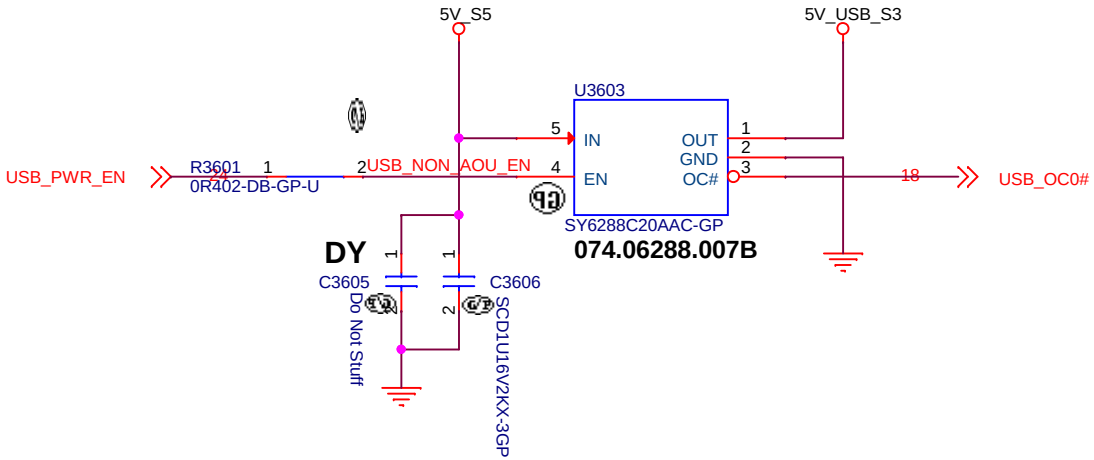
Title: USB (USB3.0 Conn)

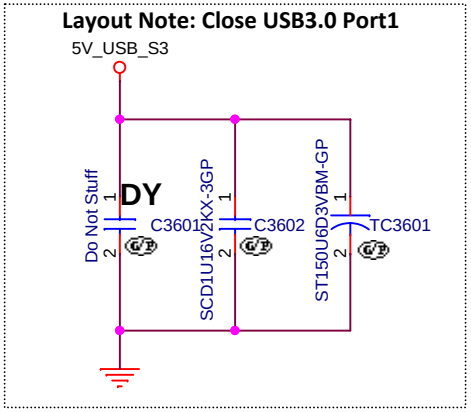
Size: A2 | Document Number: LS1511G | Rev: -1M

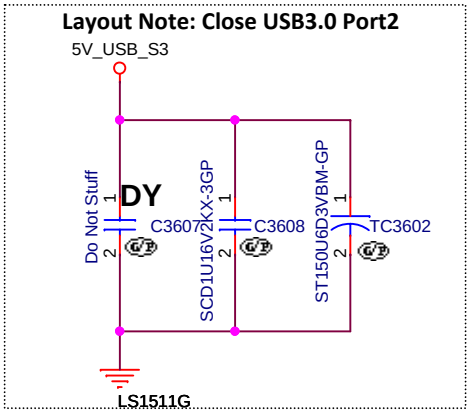
Date: Friday, December 27, 2019 | Sheet 35 of 106

Main Func = USB Charger

Port1/ 2 : USB Power







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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (USB Charger)***

Size	Document Number	Rev
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Blanking

LS1511G

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (RSVD) (PCIE to USB3.0)***

Size	Document Number	Rev
A4	LS1511G	-1M

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LS1511G

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (RSVD) (USB3.0 Redriver/USB2.0 Hub)		
Size: A4	Document Number: LS1511G	Rev: -1M
Date: Friday, December 27, 2019	Sheet 38 of 106	

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LS1511G

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Taipei Hsien 221, Taiwan, R.O.C.

Title	Sequence (RSVD)	
Size A4	Document Number LS1511G	Rev -1M
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SSID = Reset.Suspend

Power Sequence

ALL_SYS_PWRGD

PMIC_PWRGD — R4006 0R402-DB-GP-U — ALL_SYS_PWRGD

To EC

To 3V/ 5V Power IC S5 ENABLE

THERMAL TRIP PIN NEED CONNECT TO KBC

PMIC_THERMTRIP#_R — R4005 DY Do Not Stuff — PMIC_THERMTRIP#

PLT_RST# — R4001 DY Do Not Stuff — H_PWRGD_R — Q4002 Do Not Stuff

R4002 Do Not Stuff DY

PLACE CLOSE TO PCH1

0221 Change PN

3V_S5_EN — D4003 RB551V30-GP — PURE_HW_SHUTDOWN#

83.R5003.H8H

R4004 2KR2F-L1-GP — S5_ENABLE

PMIC_PWRGD 19,46

ALL_SYS_PWRGD 24

S5_ENABLE 24

PURE_HW_SHUTDOWN# 24,26

PMIC_THERMTRIP# 19,24,46

PLT_RST# 19,24,61,63,68,89

PM_SLP_S3# 19,24,46

RUN Power

5V_S0/3D3V_S0

U4001 G2898KD1U-GP 074.02898.0093

3V_5V_S0_EN — C4051 -1 1227 C4051 ASM for ESD issue

3V_SYS_OUT 3A — 5V_SYS_OUT 3.5A

Test point: AFTP4003 3D3V_S5, AFTP4001 3D3V_S0, AFTP4002 5V_S0

5V_SYS_OUT — PG4001–PG4004 GAP-CLOSE-PWR-6-GP — 5V_S0

PM_SLP_S4# — R4063 DY Do Not Stuff — PWR_5V_EN

5V_EN — R4064 0R402-DB-GP-U

3V_5V_PWRGD — R4065 0R402-DB-GP-U — PWR_5V_PG

R4066 0R402-DB-GP-U — PWR_3D3V_PG

3V_S5_EN — R4067 0R402-DB-GP-U — PWR_3D3V_EN

PWR P.45

PH on EE Side

PM_SLP_S3# — R4009 0R402-DB-GP-U — U4003 — R4010 Do Not Stuff — 3V_5V_S0_EN_R

KBC_SLP_S3# — R4061 Do Not Stuff

EC4001 SC1KP50V2KX-1GP

Do Not Stuff

1D8V_S0

1D8V_S5 — C4015 — U4002 APE8939GN3-GP 074.08939.0093 — 1D8V_S0 0.5A — C4016

R4059 0R402-DB-GP-U — 1D8V_S0_EN — R4060 Do Not Stuff — C4017

3V_SYS_OUT — PG4005–PG4007 GAP-CLOSE-PWR-6-GP — 3D3V_S0

Discharge circuit

3D3V_AUX_S5 — R4056 DY Do Not Stuff — 3D3V_S5_EN_DCG — Q4001 — 0221 Rename Net 3V_S5_EN — 3D3V_S5_DISCHG — R4048 DY Do Not Stuff — 3D3V_S5

Do Not Stuff DY

DDR3_VCCA_PWRGD

DDR3_DRAM_PWROK

APL have not DDR3_VCCA_PWRGD & COREPWROK control pin.

APL have not DRAM_PWROK control pin.

PMIC_THERMTRIP#_R — Q4004 2N7002K-2-GP 84.2N702.J31 DY — PURE_HW_SHUTDOWN#

PLT_RST#

1D8V_S5 — R4068 20KR2J-L2-GP

3D3V_S5 — R4069 20KR2J-L2-GP

Q4003 PJT138KA-GP 075.00138.0A7C

PMIC_THERMTRIP#_R — PMIC_THERMTRIP# — PMIC_THERMTRIP#_G

LS1511G

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Title: Sequence (Power Plane EN)

Size: A2 | Document Number: LS1511G | Rev: -1M

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LS1511G

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Sequence (RSVD) (DS3/S0ix)***

Size	Document Number	Rev
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Title: ***INT IO (RSVD)***

Size	Document Number	Rev
A4	**LS1511G**	**-1M**

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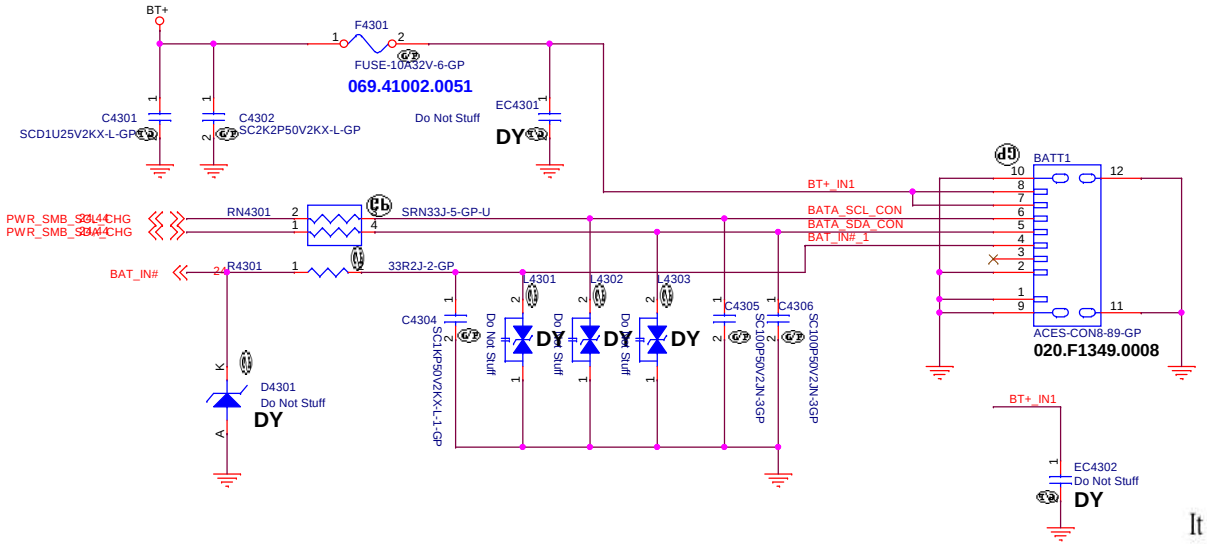
Main Func = ADT Input

1ST BATTERY CONNECTOR



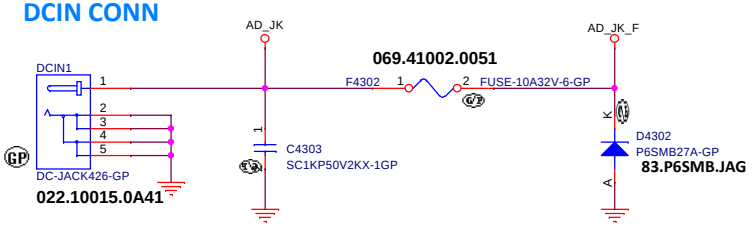
Connector Pin Alignment(Vendor：Suyin,Aces)

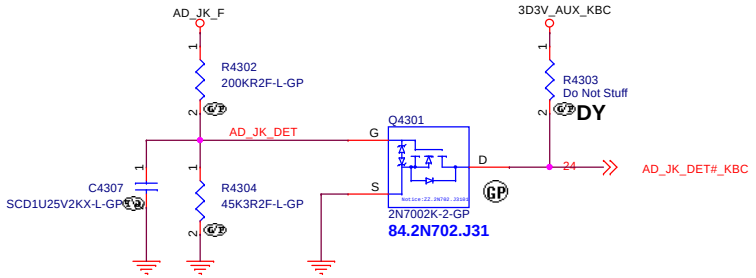
Pin#	Symbol	Comments
1	BATT+	Battery Positive Power
2	BATT+	Battery Positive Power
3	Clock	SMBus clock interface I/O pin
4	Data	SMBus data interface I/O pin
5	Detection	Connect to 10kohm resistor
6	RTC	Support RTC power or reserved
7	GND -	Common Ground Power
8	GND -	Common Ground Power

It is required to follow Lenovo common connector requirement for both battery side and system side.
Common connector drawing:

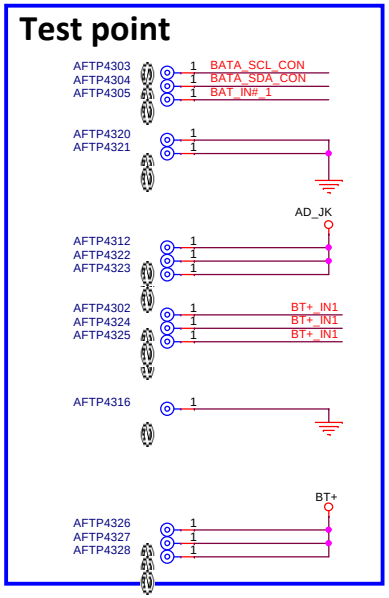
Total MLCC capacitance at DCIN connector is smaller than 1000pf to avoid LC resonance

DCIN CONN

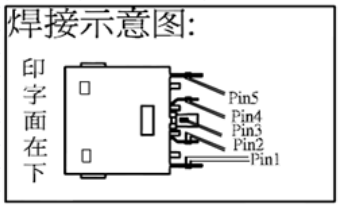




Test point



MB_Side		Cable
		Max. Current
Pin 1	AD_JK_F	UL10064AWG28# (3A)
Pin 2	AD_JK_F	UL10064AWG28# (3A)
Pin 3	AD_ID	UL10064AWG28# (3A)
Pin 4	GND	UL10064AWG26# (3.8A)
Pin 5	GND	UL10064AWG26# (3.8A)



DCBATOUT: 2~3 empty-pins between signals or other power net.
(Apply to TNB, LNB)

LS1511G

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Title: INT IO (ATX/ DC/ BATT Conn)

Size: A3 | Document Number: LS1511G | Rev: -1M

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OFFPAGE

PH on EE Side

PWR_SMB_SCL_CHG
PWR_SMB_SDA_CHG
PWR_CHG_IMON
PROCHOT#_CPU
PWR_AC_IN#
Pull high on KBC side
PWR_CHG_ON#
PWR_AD_OFF_RC

Test point

AFTP4401 PWR_AC_IN#

3D3V_AUX_KBC
R4401 Do Not Stuff DY
PWR_CHG_BM#

SSID = Charger

For Adapter IN
Confirm with EE

AD+_2 trace width > 8mil
Length < 500mil

close PU4410

Id= -10A
Qg= -22nC
Rdson=14~22mohm

084.05112.001K

Close to 第一顆MOS

Already Pull high on KBC side

74.02224.073

PC4419 is close to PU4401 PIN#4

Id= -10A
Qg= -40nC
Rdson=17.6~23mohm

SC-0906
83.R2003.A8M
83.RB530.08F
083.52030.008F

83.R2003.A8M

Cyntec, 6.5mm x 6.9mm x 3.0mm
DCR: 28m ~ 33mOhm
Idc : 5.5A , Isat : 6.5A

68.4R710.20Y

Charger Current=1.4~3.6A

84.05212.B11

84.2N702.J31

LS1511G

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Title: Power (Charger_HPA02224RGRR)
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OFFPAGE-Signal

PWR_5V_EN — 40 — PWR_5V_EN

PH on EE Side

PWR_5V_PG — 40 — PWR_5V_PG

PWR_3D3V_EN — 40 — PWR_3D3V_EN

PH on EE Side

PWR_3D3V_PG — 40 — PWR_3D3V_PG

OFFPAGE-GAP

19V_DCBATOUT — PWR_DCBATOUT_3D3V
PG4501 GAP-CLOSE-PWR-3-GP
PG4502 GAP-CLOSE-PWR-3-GP
PG4503 GAP-CLOSE-PWR-3-GP
PG4504 GAP-CLOSE-PWR-3-GP

19V_DCBATOUT — PWR_DCBATOUT_5V
PG4552 GAP-CLOSE-PWR-3-GP
PG4553 GAP-CLOSE-PWR-3-GP
PG4555 GAP-CLOSE-PWR-3-GP
PG4557 GAP-CLOSE-PWR-3-GP
PG4559 GAP-CLOSE-PWR-3-GP
PG4561 GAP-CLOSE-PWR-3-GP

3D3V_S5 — PWR_3D3V
PG4505 GAP-CLOSE-PWR-3-GP
PG4506 GAP-CLOSE-PWR-3-GP
PG4507 GAP-CLOSE-PWR-3-GP
PG4508 GAP-CLOSE-PWR-3-GP
PG4509 GAP-CLOSE-PWR-3-GP
PG4510 GAP-CLOSE-PWR-3-GP
PG4511 GAP-CLOSE-PWR-3-GP
PG4512 GAP-CLOSE-PWR-3-GP

5V_S5 — PWR_5V
PG4551 GAP-CLOSE-PWR-3-GP
PG4554 GAP-CLOSE-PWR-3-GP
PG4556 GAP-CLOSE-PWR-3-GP
PG4558 GAP-CLOSE-PWR-3-GP
PG4560 GAP-CLOSE-PWR-3-GP
PG4563 GAP-CLOSE-PWR-3-GP
PG4564 GAP-CLOSE-PWR-3-GP
PG4566 GAP-CLOSE-PWR-3-GP

3D3V_AUX_S5 — PWR_3D3V_LDO
PG4527 GAP-CLOSE-PWR-3-GP

5V_AUX_S5 — PWR_5V_LDO
PG4565 GAP-CLOSE-PWR-3-GP

IDC:6A

Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A

PWR_DCBATOUT_3D3V
PC4502 SC10U25V5KX-L-GP
PC4503 DY Do Not Stuff
PR4501 0R0603-PAD-1-GP-U
PC4506 SCD1U25V2KX-L-GP
PWR_3D3V_BOOT — PWR_3D3V_BOOT_A
PU4501 SY8286BRAC-GP
PWR_3D3V_EN, PWR_3D3V_EN2, PWR_3D3V_BOOT, PWR_3D3V_PG, PWR_3D3V_FB
PWR_3D3V_PH
PL4501 COIL-1D5UH-29-GP 68.1R510.20N
PWR_3D3V
PC4509 PC4510 PC4511 SC22U6D3V3MX-L1-GP
PC4512 DY Do Not Stuff
PWR_3D3V_LDO
PC4507 SC4D7U6D3V3KX-L-GP
PG4528 GAP-CLOSE-PWR-3-GP
PR4514 1MR2J-1-GP
PR4509 499KR2F-1-GP
19V_DCBATOUT
PR4508 499KR2F-1-GP
PC4508 DY Do Not Stuff
3D3V_AUX_S5
DY Do Not Stuff PR4505
PWR_3D3V_VOUT — Trace used 10 mil
PC4521 SC1KP50V2KX-L-1-GP
PWR_3D3V_FB2
PR4506 1KR2F-3-GP

EN rating 25V
EN Rising Threshold : 0.8V
Ilimt : 8A

Place another side , make GND plan bigger

SY8286B_074.08286.0043 for 6A IDC

SY8288B_074.08288.0A43 for 8A IDC

IDC:8A

5V_AUX_S5
PR4552 Do Not Stuff DY
Place another side , make GND plan bigger

Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A

PWR_DCBATOUT_5V
PC4554 SC10U25V5KX-L-GP
PC4555 DY Do Not Stuff
For 2cell use
PU4551 SY8288CRAC-GP
PWR_5V_PG
PWR_5V_BOOT — PWR_5V_BOOT_A
PR4554 0R0603-PAD-1-GP-U
PC4553 SCD1U25V2KX-L-GP
PWR_5V_PH
PL4551 COIL-1D5UH-29-GP 68.1R510.20N
PWR_5V
PC4556 PC4557 PC4558 PC4559 SC22U6D3V3MX-L1-GP
DY PC4560 PC4561 SC22U6D3V3MX-L1-GP
For 2cell use
PWR_5V_VOUT — Trace used 10 mil
PG4562 GAP-CLOSE-PWR-3-GP
PWR_5V_FB — PWR_5V_FB_A
PR4555 1KR2F-3-GP
PC4563 SC1KP50V2KX-L-1-GP
PWR_5V_LDO
PC4562 SC2D2U10V3KX-L-GP
PWR_5V_EN, PWR_5V_EN2
PR4556 1MR2J-1-GP
PR4557 499KR2F-1-GP
19V_DCBATOUT
PR4558 499KR2F-1-GP Do Not Stuff
PC4564 DY
PC4551 SC4D7U6D3V3KX-L-GP

Place another side , make GND plan bigger

EN rating 25V
EN Rising Threshold : 0.8V
Ilimt : 8A

LS1511G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: SY8286B_3D3V-SY8288C_5V
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OFFPAGE

CPU_I2C_SCL_PMIC — PR4609 0R0402-PAD-1-GP — PWR_CLK

CPU_I2C_SDA_PMIC — PR4615 0R0402-PAD-1-GP — PWR_DATA

3V_5V_PWRGD — PR4616 0R0402-PAD-1-GP — PWR_PMIC_EN

PM_SLP_S0# — PR4617 0R0402-PAD-1-GP — PWR_SLP_S0_B

PM_SLP_S3# — PR4618 0R0402-PAD-1-GP — PWR_SLP_S3_B

PM_SLP_S4# — PR4619 0R0402-PAD-1-GP — PWR_SLP_S4_B

PH on EE Side

PMIC_RSMRST# — PR4620 0R0402-PAD-1-GP — PWR_RSMRST_B

PMIC_PWRGD — PR4621 0R0402-PAD-1-GP — PWR_PCH_PWROK

PMIC_THERMTRIP# — PR4622 0R0402-PAD-1-GP — PWR_THERMTRIP_B

PROCHOT#_CPU — PR4623 0R0402-PAD-1-GP — PWR_PROCHOT_B

PMIC_IRQ# — PR4624 0R0402-PAD-1-GP — PWR_IRQ_B

Main Func = CPU_CORE

I2C, Other signals

19V_DCBATOUT — PG4613 GAP-CLOSE-PWR-3-GP — PC4602 SC1U25V3KX-L-GP

1D8V_S5 — PG4601 GAP-CLOSE-PWR-3-GP — PC4601 SC1U10V2KX-L1-GP

Table 4-2. Gemini Lake PMIC and SoC Signal Connections

Gemini Lake PMIC Pin	Gemini Lake SoC Pin Name	SoC Pin	SoC Pin Type	Voltage Rail
IRQ#	TBD	TBD	Input	1.8V (SoC internal)
THERMTRIP#	THERMTRIP_N	J53	Output	1.8V (SoC internal)
PROCHOT#	PROCHOT_N	J54	Input	1.8V (SoC internal)
SLP_S4#	PMU_SLP_S4_N	J49	Output	1.8V (SoC internal)
SLP_S3#	PMU_SLP_S3_N	D51	Output	1.8V (SoC internal)
SLP_S0#	PMU_SLP_S0_N	C52	Output	1.8V (SoC internal)
PCH_PWROK	SoC_PWROK	D26	Input	External PU 20K to V3P3A and PD 100K to GND
RSMRST#	RSM_RST_N	F27	Input	External PU 20K to V3P3A and PD 100K to GND
DATA	PMIC_I2C_SDA	TBD	Input/ Output	1.8V (SoC internal)
CLK	PMIC_I2C_SCL	TBD	Output	1.8V (SoC internal)

PU4601E BD2671MWV-E2-GP (5 OF 5)

PWR_VSYS	57	VSYS	VSYS_V5A_0 31 PWR_VSYS_V5A_0
PWR_VDD_1VP8A	29	VDD_V1P8A	VSYS_V5A_1 4 PWR_VSYS_V5A_1
PWR_CLK	37	CLK	VSYS_V5A_2 50 PWR_VSYS_V5A_2
PWR_DATA	36	DATA	
PWR_PMIC_EN	33	PMIC_EN	LDO15 30 PWR_PMIC_LDO1D5V
PWR_SLP_S0_B	20	SLP_S0_B	
PWR_SLP_S3_B	21	SLP_S3_B	EXTMODE 32 PWR_EXTMODE
PWR_SLP_S4_B	22	SLP_S4_B	TEST0 39 PWR_TEST0
PWR_RSMRST_B	19	RSMRST_B	
PWR_PCH_PWROK	18	PCH_PWROK	DDR_SEL0 2 PWR_EXTMODE0
PWR_THERMTRIP_B	34	THERMTRIP_B	DDR_SEL1 12 PWR_EXTMODE1
PWR_PROCHOT_B	35	PROCHOT_B	DDR_SEL2 17 PWR_EXTMODE2
PWR_IRQ_B	38	IRQ#	GND0 28, GND1 46, GND2 64, PGND 69

PR4603 20R2J-3-GP — PWR_VSYS_V5A_0_A — PG4614 GAP-CLOSE-PWR-3-GP — 5V_S5

PC4603 SC4D7U6D3V3KX-L-GP

PG4616 GAP-CLOSE-PWR-3-GP — 5V_S5

PC4604 SC4D7U6D3V3KX-L-GP

PG4615 GAP-CLOSE-PWR-3-GP — 5V_S5

PC4615 SC4D7U6D3V3KX-L-GP

PC4605 SC4D7U6D3V3KX-L-GP

PR4608 100KR2F-L3-GP

3D3V_S5

DY PR4625 Do Not Stuff

DY PR4626 Do Not Stuff

PR4625.PR4626 change from DY to stuff_20190819_BCN

DY PR4628 Do Not Stuff

DY PR4627 Do Not Stuff

DY PR4631 Do Not Stuff

PR4604 10KR2J-L-GP

PR4605 10KR2J-L-GP

DY PR4632 Do Not Stuff

DY PR4630 0R0402-PAD-1-GP

DY PR4606 Do Not Stuff

DY PR4607 Do Not Stuff

PR4633 0R0402-PAD-1-GP

Table 4-32 DDR_SEL0,1 selection on VDDQ and LDO_VPP

DDR_SEL2,1,0	DDR selection	VDDQ voltage	LDO_VPP voltage	V1P2A Voltage	VTT Voltage	Description
(L,L,L)	LPDDR3	1.200V	1.800V	1.200V	0.600V	-
(L,L,H)	DDR3L	1.350V	OFF	1.200V	0.675V	LDO_VPP unused
(L,H,L)	LPDDR4	1.100V	1.800V	1.200V	0.550V	-
(L,H,H)	DDR4	1.200V	2.500V	1.200V	0.600V	-
(H,L,L)	LPDDR3	1.200V (V1P2A boot timing)	1.800V	OFF	0.600V	V1P2A merged to VDDQ
(H,L,H)	DDR3L	1.350V	1.800V (SLP_S3_B control)	1.200V	0.675V	LDO_VPP can be used as optional LDO
(H,H,L)	LPDDR4	1.100V	1.800V	1.200V	OFF	VTT unused
(H,H,H)	DDR4	1.200V (V1P2A boot timing)	2.500V	OFF	0.600V	V1P2A merged to VDDQ

LS1511G

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (BD2671MWV_VCORE)

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PR4723 0R0402-PAD-1-GP — VCCGI_SENSE — PWR_VCCGI_FBPC

PR4724 0R0402-PAD-1-GP — VSSGI_SENSE — PWR_VCCGI_FBNB

Main Func = CPU_CORE

BUCK2[VCCGI]:1.0V_21A

19V_DCBATOUT, PWR_DCBATOUT_VCORE

PG4701 GAP-CLOSE-PWR-3-GP
PG4702 GAP-CLOSE-PWR-3-GP
PG4703 GAP-CLOSE-PWR-3-GP
PG4704 GAP-CLOSE-PWR-3-GP
PG4705 GAP-CLOSE-PWR-3-GP
PG4706 GAP-CLOSE-PWR-3-GP

DY PT4702 Do Not Stuff

5V_S5

PC4705 SC4D7U6D3V3KX-L-GP

PR4701 0R0402-PAD-1-GP

MOSFET GATE Driver

PC4711 SCD47U25V3KX-1GP

PU4701 BD9515NUXE2-GP-U
PWR_VCCGI_PVCC, PWR_VCCGI_PWM_A, PWR_VCCGI_BOOT, PWR_VCCGI_HG, PWR_VCCGI_PH, PWR_VCCGI_LG

PC4716 SC1U10V2KX-L1-GP

PR4720 0R0805-PAD-1-GP-U

DY PR4721 Do Not Stuff — PWR_VCCGI_HG_A

PU4702 FDMS3600-02-RJK0215-COLAY-GP
ZZ.00215.037
075.36354.0073
main: 075.36354.0073
2nd: 84.08S36.037

PWR_DCBATOUT_VCORE
PC4702 PC4703 PC4701 PC4704 SC10U25V5KX-L-GP

ICCMAX=21A
TDC=18A

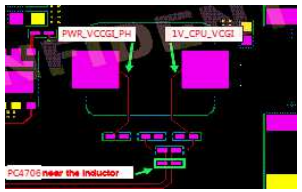
PU4601A BD2671MWV-E2-GP 1 OF 5

PR4702 0R0402-PAD-1-GP

VCCGI_PWM — PWR_VCCGI_PWM
VCCGI_DRVEN — PWR_VCCGI_DRVEN

PL4701 IND-D22UH-107-GP
Cyntec 10.3 X 11.5 X 3 mm
DCR: 1 +-5% m ohm
Idc :30A , Isat : 50A

close choke
1V_CPU_VCGI
VCCGI :1D0V_21A
PC4718 SC22U6D3V3MX-L1-GP
PT4701 SE330U2VDM-4-GP



PG4710 GAP-CLOSE-PWR-3-GP
PG4711 GAP-CLOSE-PWR-3-GP
PWR_VCCGI_CSPB
PR4707 1K1R2F-GP
PR4708 2K2R2F-GP
2PWR_VCCGI_PHA
PR4719 NTC-10K-27-GP-U
PR4709 9K1R2F-1-GP
close choke

Panasonic 7.3 * 4.3 * 1.9 mm
ESR: 9 m ohm
22uF_6.3V_0805 *8pcs
DY*2pcs

PWR_VCCGI_PH
DY PR4722 Do Not Stuff
PWR_VCCGI_SNUB
DY PC4715 Do Not Stuff

VCCGI_CSP — 51 PWR_VCCGI_CSP
PC4717 SC68P50V2JN-1GP
PR4710 0R0402-PAD-1-GP
PWR_VCCGI_CSPA
close PMIC
PC4714 SCD047U25V2KX-GP
PC4706 SCD22U10V2KX-L1-GP
close choke

VCCGI_CSN — 52 PWR_VCCGI_CSN
PR4711 820R2F-GP
PWR_VCCGI_CSNA
PC4707 Do Not Stuff
DY

close PMIC
VCCGI_VOS — 53 PWR_VCCGI_VOS
PR4716 0R0402-PAD-1-GP
PC4710 SCD047U25V2KX-GP
PR4712 4K3R3F-GP
PR4715 0R0402-PAD-1-GP
PWR_VCCGI_FBPA
PWR_VCCGI_FBPB
PG4707 GAP-CLOSE-PWR-3-GP
PWR_VCCGI_FBPC
PR4717 100R2F-L1-GP-U
1V_CPU_VCGI
PR4733 100R2F-L1-GP-U

VCCGI_FBP — 54 PWR_VCCGI_FBP
DY PC4712 Do Not Stuff
PC4713 SC1U10V2KX-L1-GP

VCCGI_FBN — 55 PWR_VCCGI_FBN
PR4713 0R0402-PAD-1-GP
PWR_VCCGI_FBNA
PG4708 GAP-CLOSE-PWR-3-GP
PWR_VCCGI_FBNB
DY PC4736 Do Not Stuff

LS1511G

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Title: POWER (BD9515/ BD2671_VCCGI)
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Title: ***Power (RSVD)***		
Size: A4	Document Number: **LS1511G**	Rev: **-1M**
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Title: ***Power (RSVD)***		
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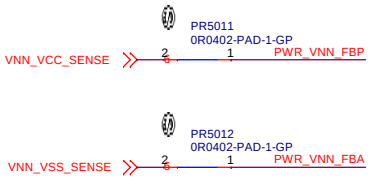
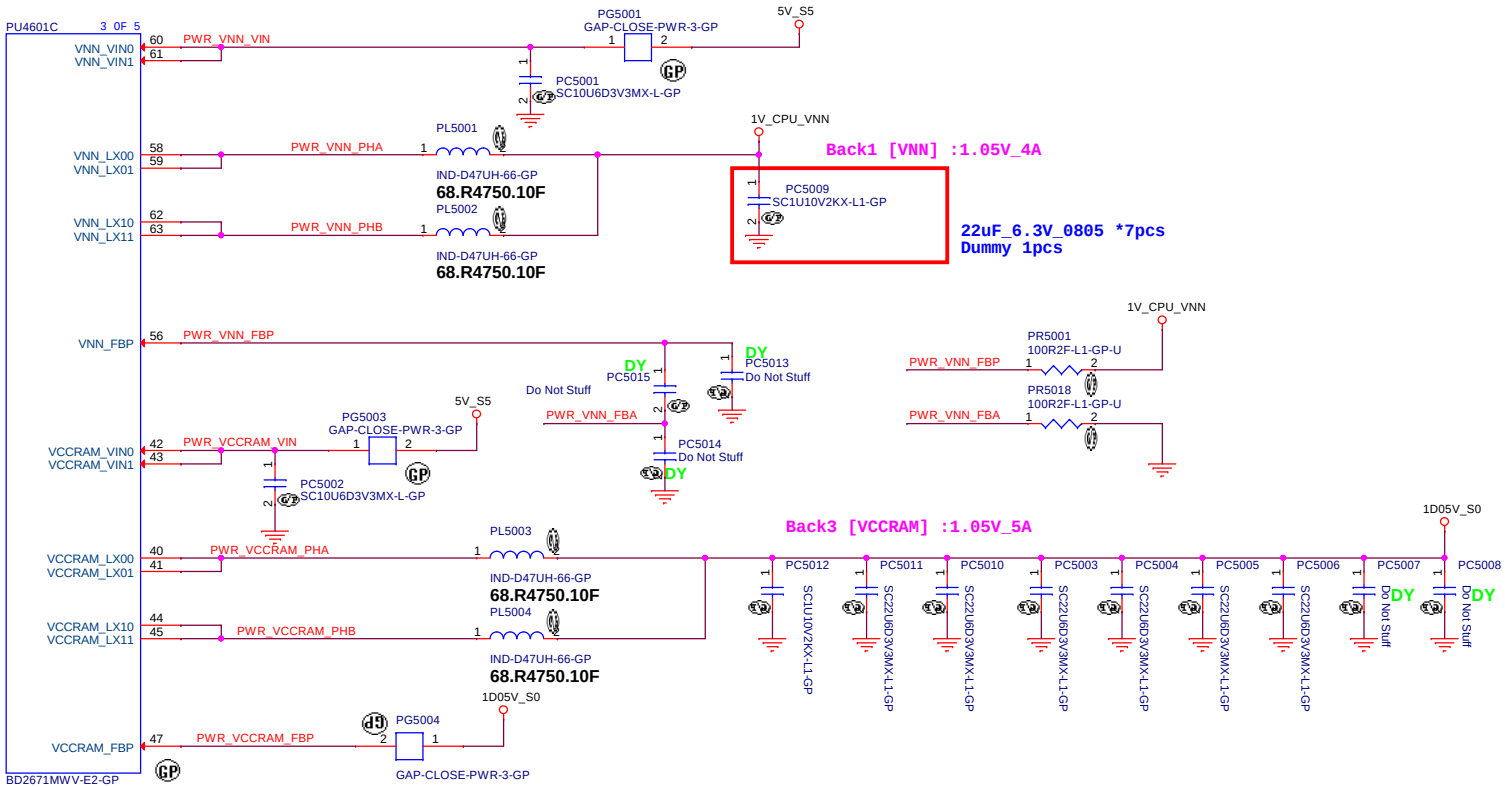


VNN[BUCK1], VCCRAM[BUCK3]



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Title: POWER (BD2671_VNN)		
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VDDQ[BUCK6], V1P2A[BUCK5]

MOSFET GATE Driver

close PMIC

close choke

close choke

Near the inductor

VDDQ :1D1V / 1D2V_7A

V1P2A[BUCK5] : 1.2V, 2.5A

1D8V_0.4A

VTT: VDDQ/2_0.6A

1D8V/2D5V_1A

Table 4-32 DDR_SEL0,1 selection on VDDQ and LDO_VPP

DDR_SEL2,1,0	DDR selection	VDDQ voltage	LDO_VPP voltage	V1P2A Voltage	VTT Voltage	Description
(L,L,L)	LPDDR3	1.200V	1.800V	1.200V	0.600V	-
(L,L,H)	DDR3L	1.350V	OFF	1.200V	0.675V	LDO_VPP unused
(L,H,L)	LPDDR4	1.100V	1.800V	1.200V	0.550V	-
(L,H,H)	DDR4	1.200V	2.500V	1.200V	0.600V	-
(H,L,L)	LPDDR3	1.200V (V1P2A boot timing)	1.800V	OFF	0.600V	V1P2A merged to VDDQ
(H,L,H)	DDR3L	1.350V	1.800V (SLP_S3_B control)	1.200V	0.675V	LDO_VPP can be used as optional LDO
(H,H,L)	LPDDR4	1.100V	1.800V	1.200V	OFF	VTT unused
(H,H,H)	DDR4	1.200V (V1P2A boot timing)	2.500V	OFF	0.600V	V1P2A merged to VDDQ

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Title: POWER (BD2671_VDDQ/VTT)

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Size: A4	Document Number: **LS1511G**	Rev: **-1M**
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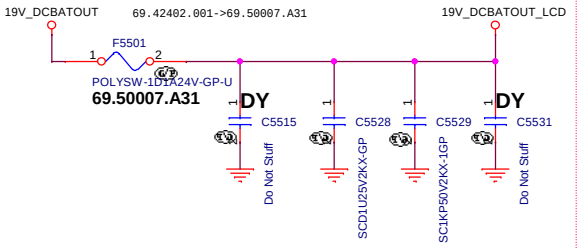
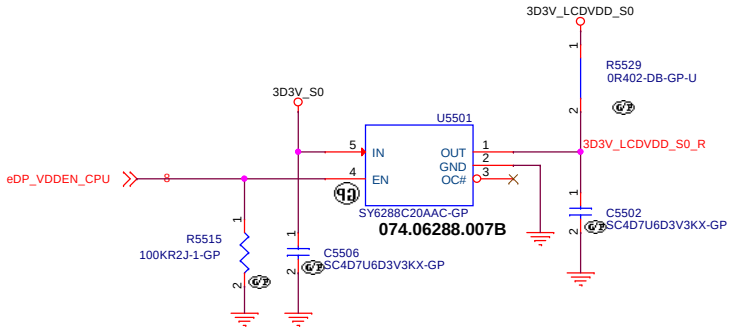
Main Func = LCD

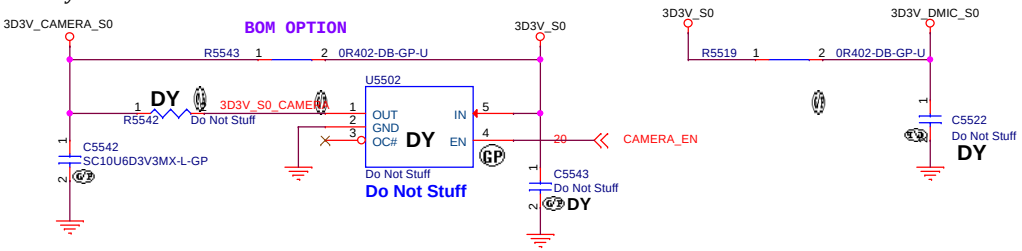
INVERTER POWER



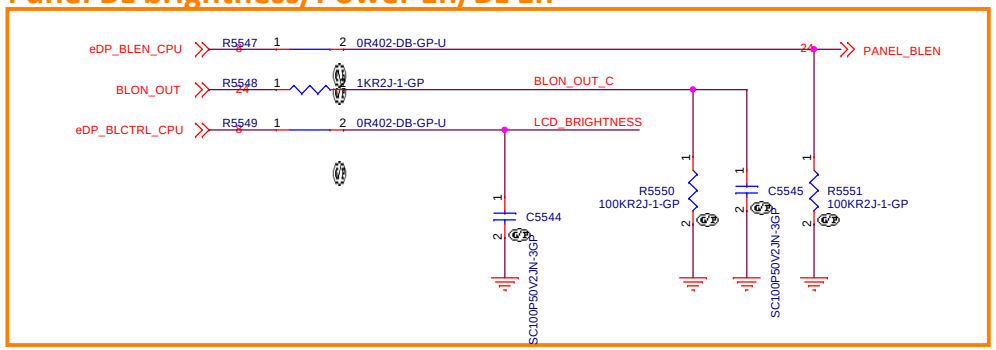


Layout 40 mil

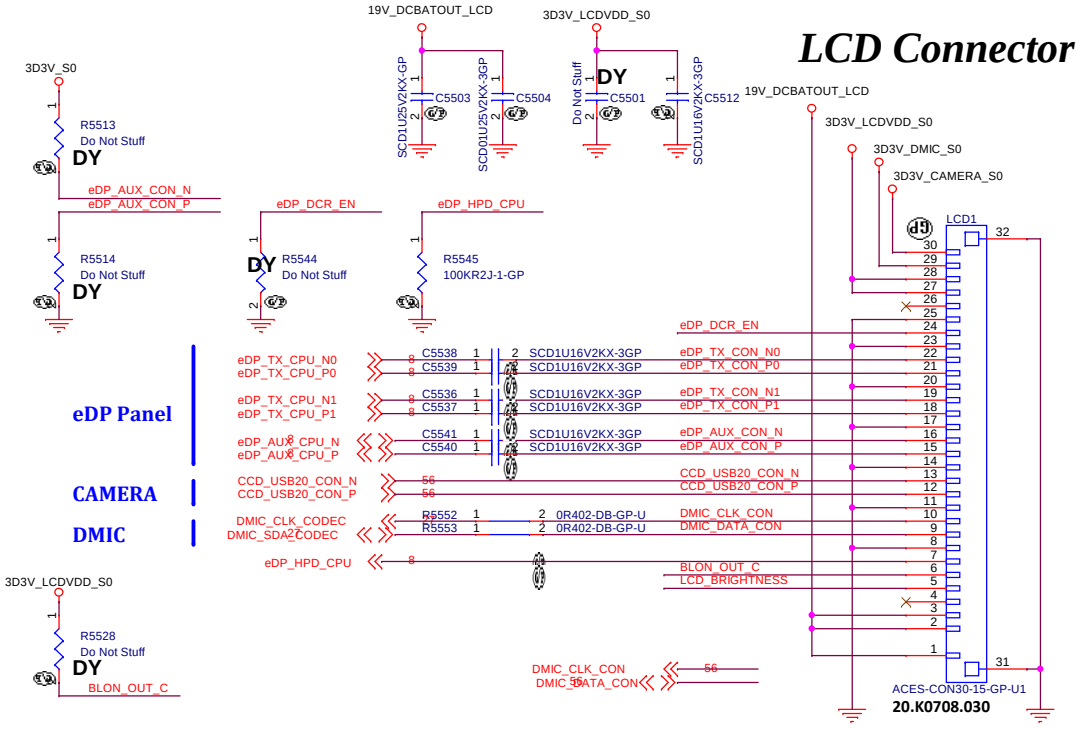
CAMERA POWER



Panel BL brightness/Power En/BL En

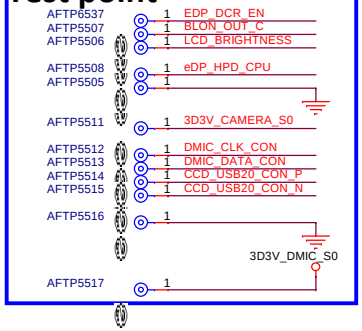


LCD Connector



1) DCBATOUT: Need 1~3 empty-pin from DCBATOUT to the signals or other power net. (Apply to TNB, LNB)

Test point



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Display (LCD/Inverter)**

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Camera S150 **TO LCD**

CCD2_USB20_P 18
CCD2_USB20_N 18
CCD_USB20_CON_N 55
CCD_USB20_CON_P 55
DMIC_CLK_CON 56
DMIC_DATA_CON 57

main: 068.09002.2001
2nd: 068.MCF8.2001

R5603 1 2 0R402-DB-GP-U
EL5601
CCD2_USB20_N 4
CCD2_USB20_P 2 1
DY
Do Not Stuff
R5604 1 2 0R402-DB-GP-U

CCD CONN

CCD_USB20_CON_N
CCD_USB20_CON_P

main: 075.00199.007C
2nd: 075.08105.007C

ED5602
1 6
2 5
3 4
PWRNC5602
Do Not Stuff FN5602
DMIC_DATA_CON
DMIC_CLK_CON
Do Not Stuff
DY
Do Not Stuff
Camera

EC5604 1 2
Do Not Stuff
DY

EC5603 1 2
Do Not Stuff
DY

LS1511G

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Display (CRT/IR Camera)***

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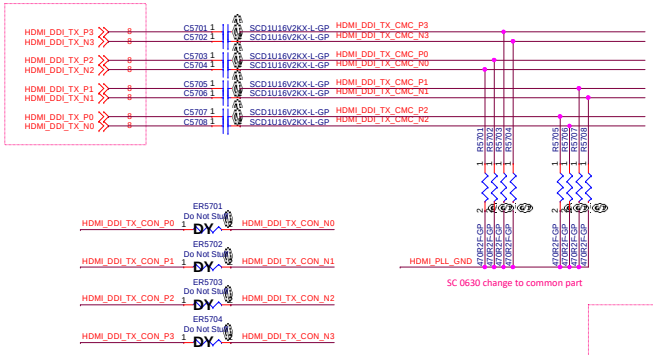
HDMI

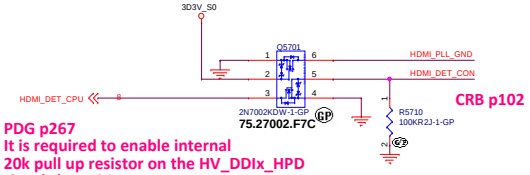
HDMI Passive Level Shifter

Close to HDMI Connector

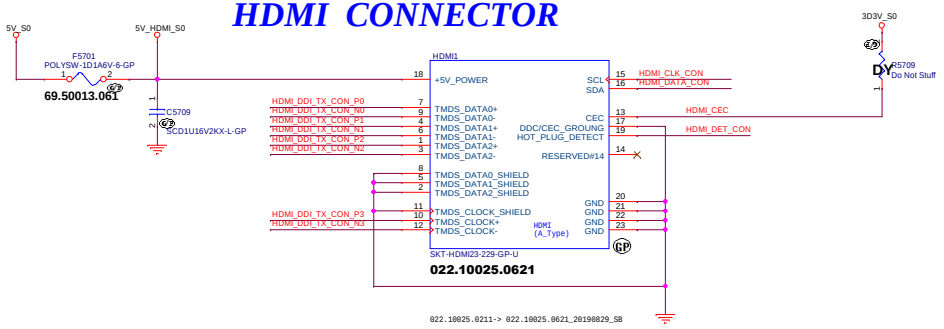


SC 0630 change to common part

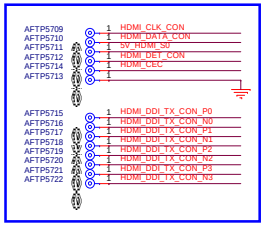
PDG p267
It is required to enable internal
20k pull up resistor on the HV_DDIx_HPD
signals by BIOS

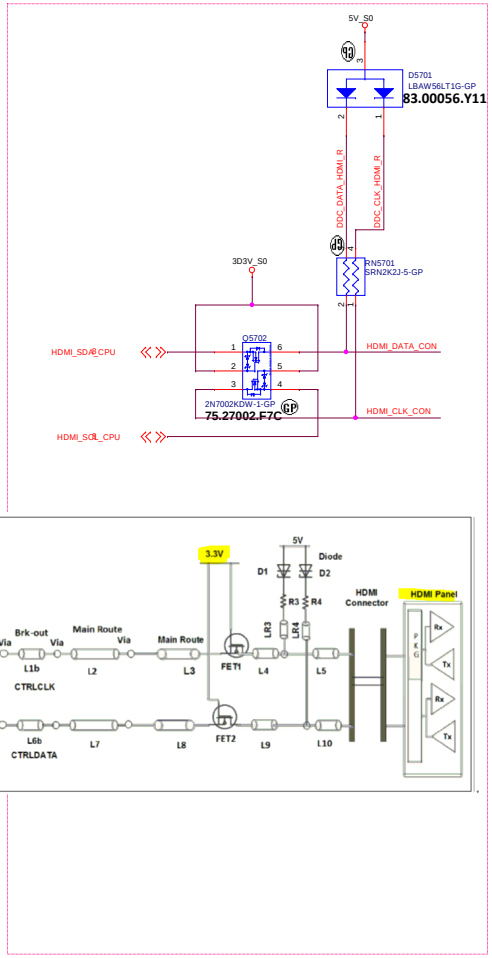


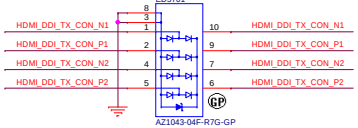
HDMI CONNECTOR



Test point







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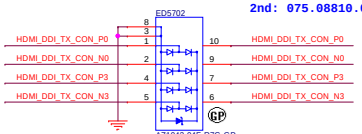
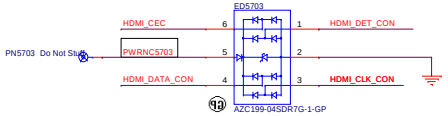
2nd: 075.08810.0A73





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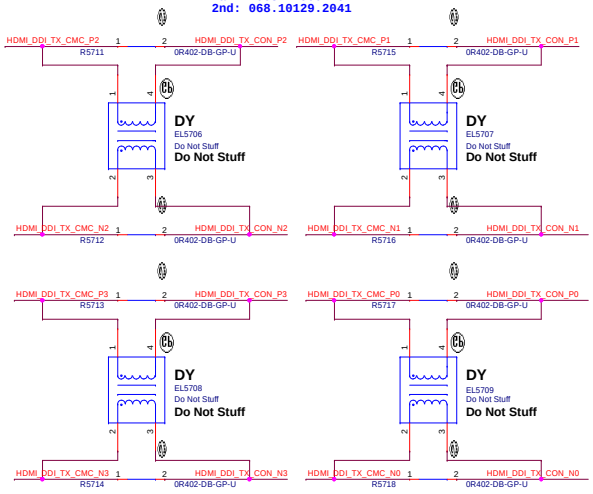
2nd: 075.08105.007C

main: 068.24900.2011
2nd: 068.10129.2041



LS1511G

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Display (HDMI Conn/Retimer)		
Size: A2	Document Number: LS1511G	Rev: -1M
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Title: ***Display (RSVD) DP / DVI***

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LS1511G

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Title: ***Display (RSVD) Backlight PWR***

Size	Document Number	Rev
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Taipei Hsien 221, Taiwan, R.O.C.

Title
INT IO (RSVD) (HDD/ODD)

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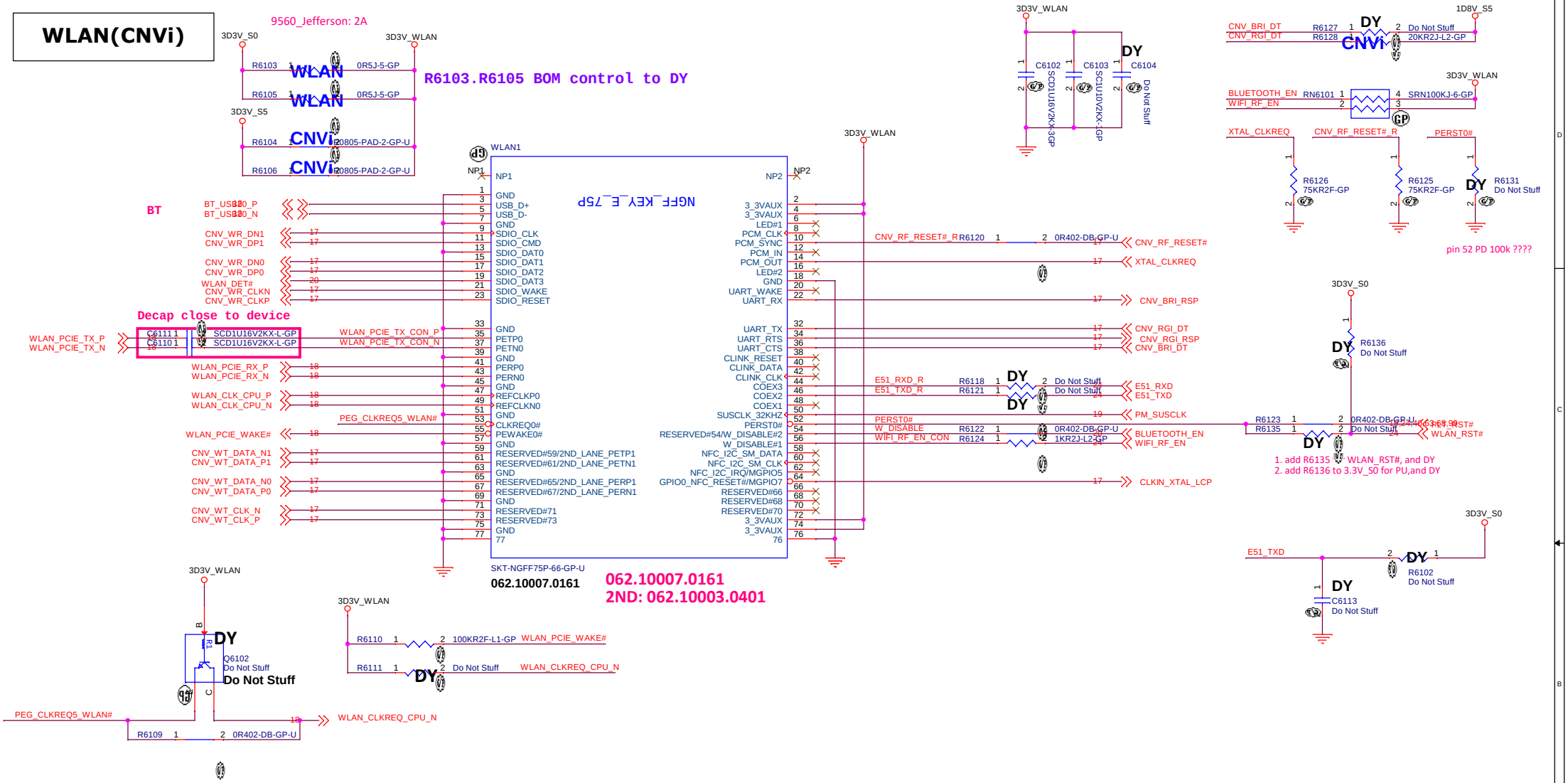
WLAN(CNVi)

9560_Jefferson: 2A

R6103.R6105 BOM control to DY



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Title: INT IO (WLAN M.2)		
Size: A3	Document Number: LS1511G	Rev: -1M
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Title	***INT IO (RSVD) WWAN***	
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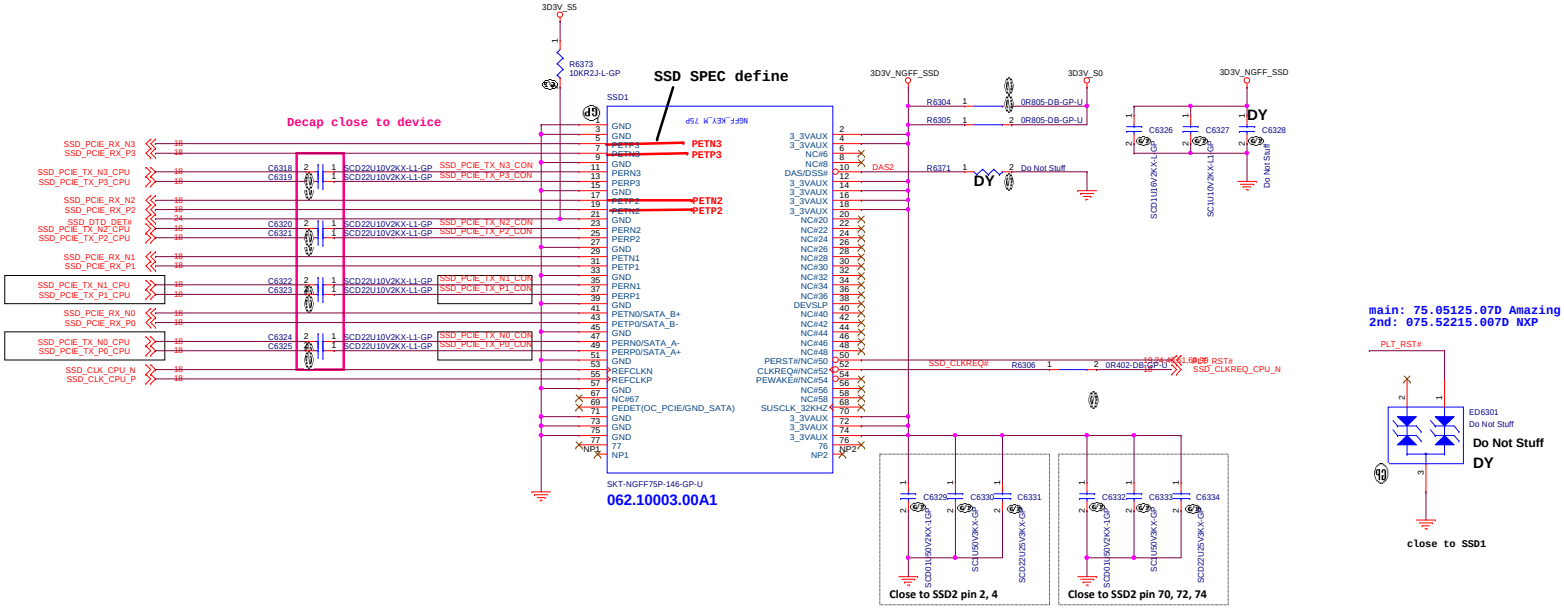
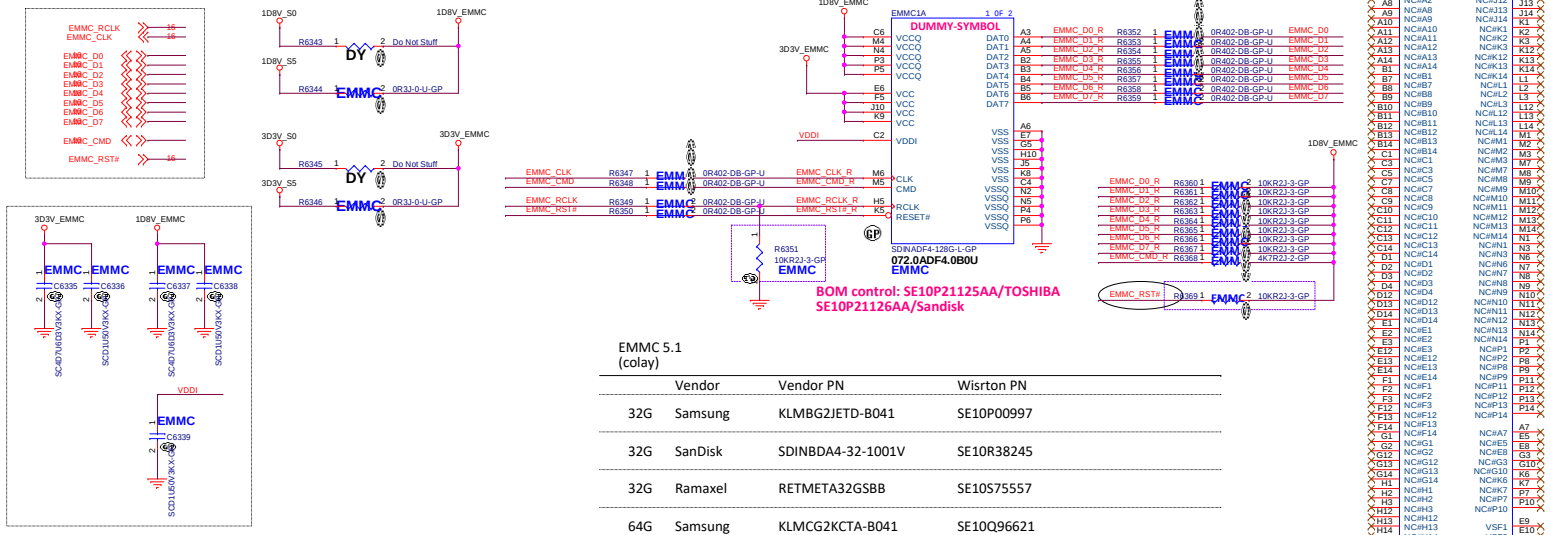
Main Func = SSD

TYPE-M NGFF CARD FOR PCIE SSD/Optane



SSID = eMMC



EMMC 5.1
(colay)

	Vendor	Vendor PN	Wisrton PN
32G	Samsung	KLMBG2JETD-B041	SE10P00997
32G	SanDisk	SDINBDA4-32-1001V	SE10R38245
32G	Ramaxel	RETMETA32GSBB	SE10S75557
64G	Samsung	KLMCG2KCTA-B041	SE10Q96621
64G	SanDisk	SDINBDA4-64-1001V	SE10R38243
64G	Ramaxel	RETMETA64GDBB	SE10S75555

LS1511G

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Title: INT IO (SSD M.2/ eMMC)

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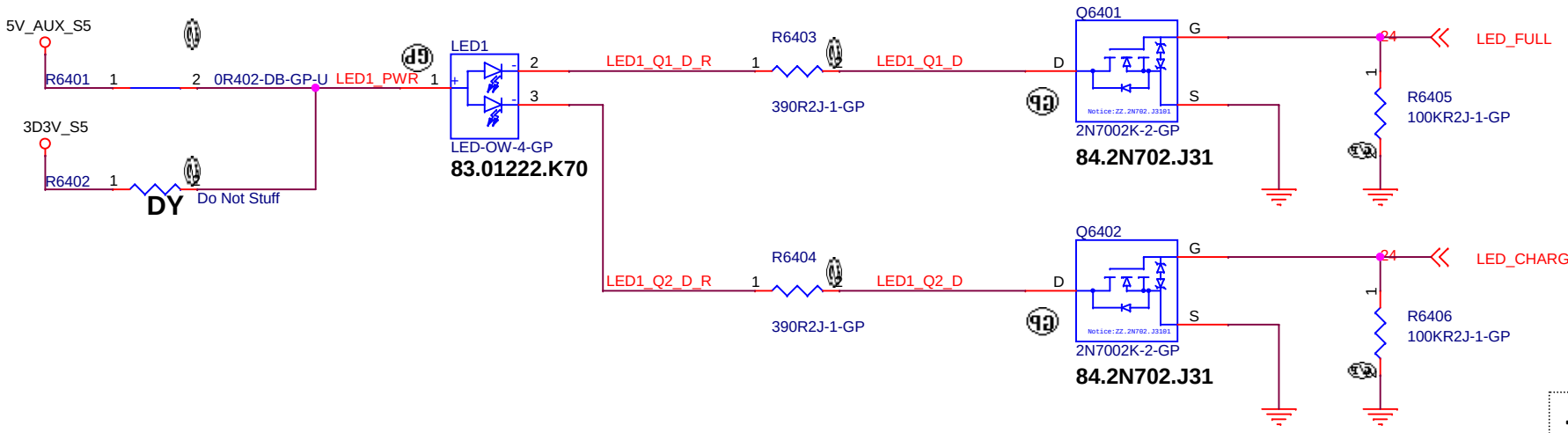
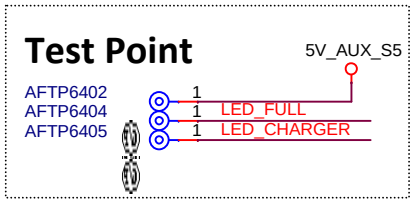
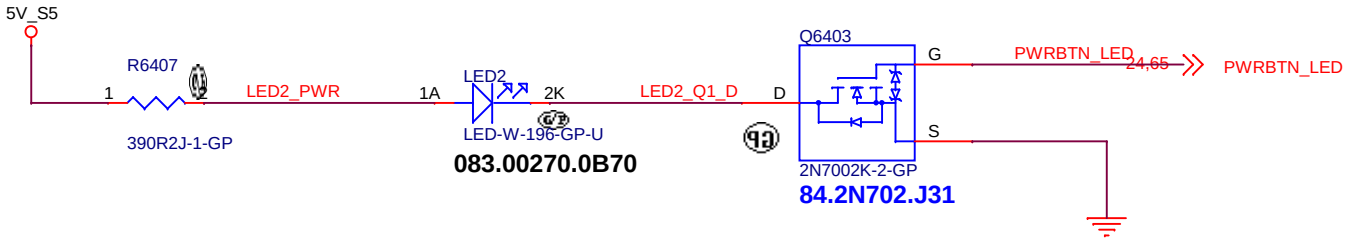
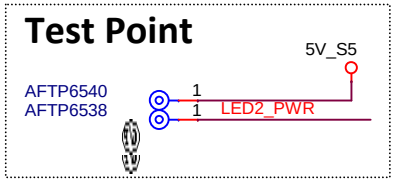
DCIN/Charger LED C350/S150



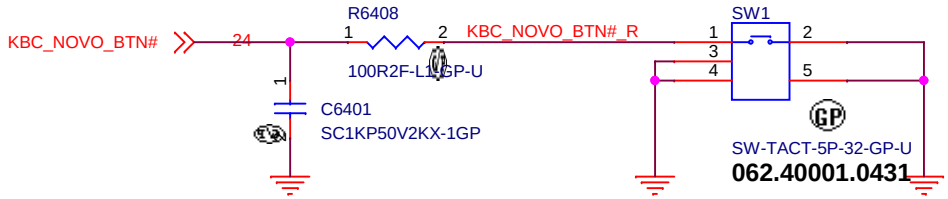


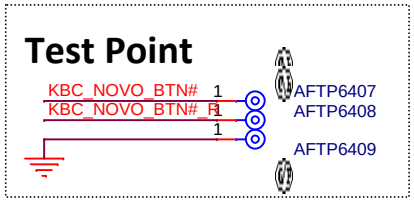
POWER BTN LED





NOVO BTN





LS1511G

緯創資通 **Wistron Corporation**
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Title: ***LED / Button / Power Button***

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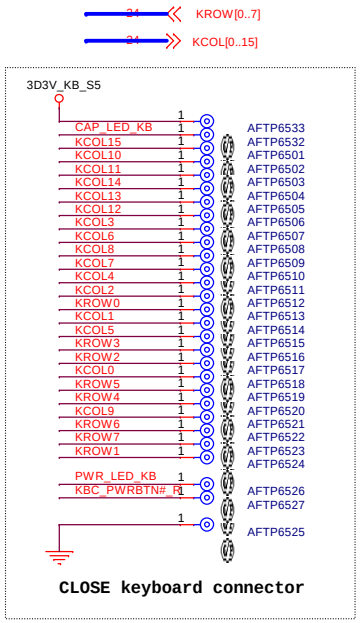
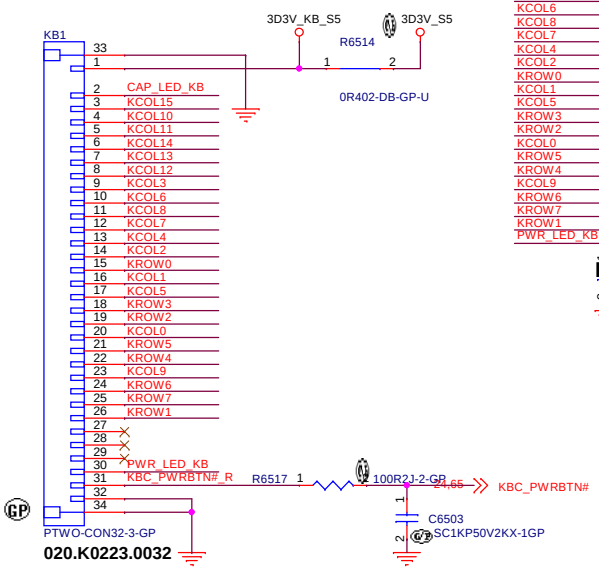
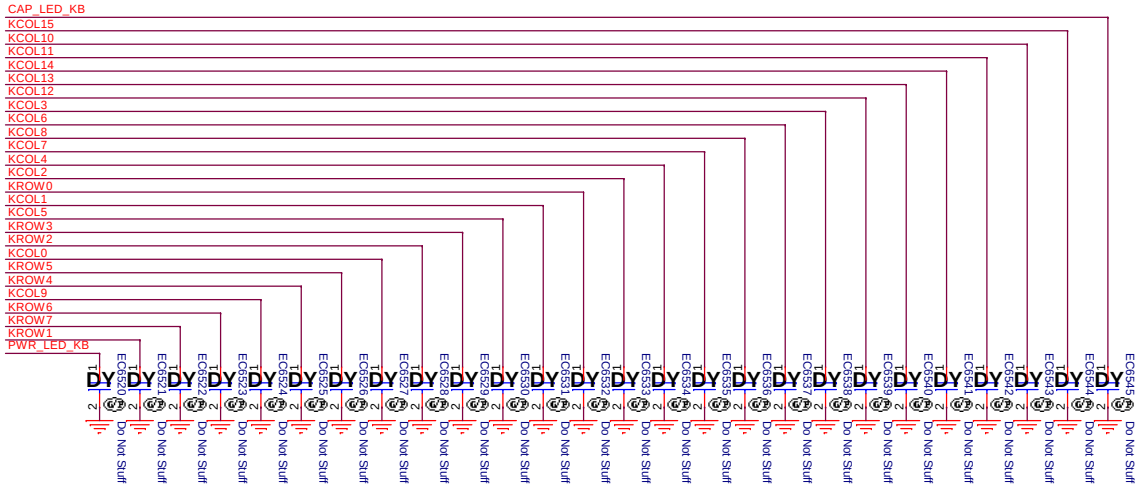
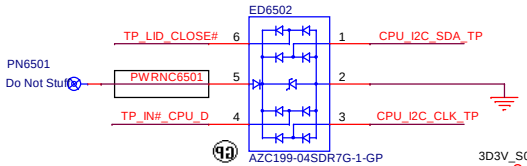
SSID = Touch.Pad

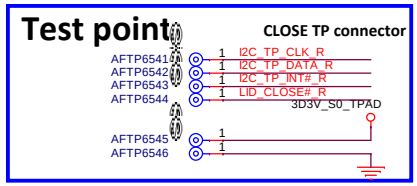


CLOSE keyboard connector



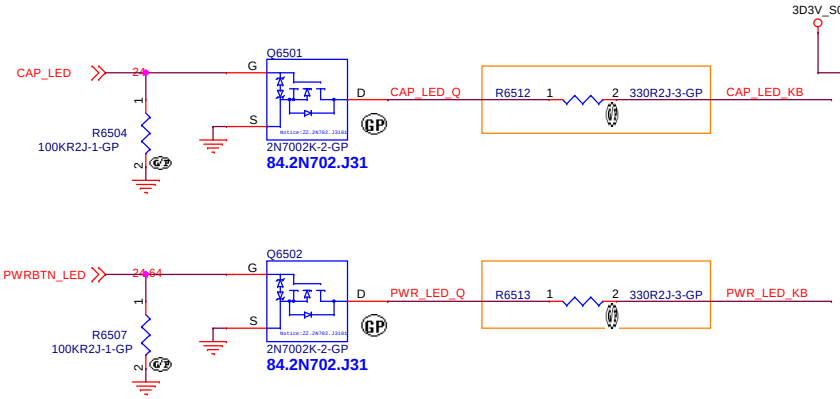


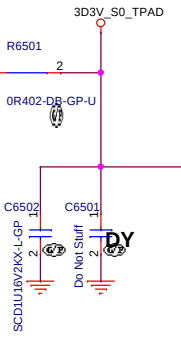




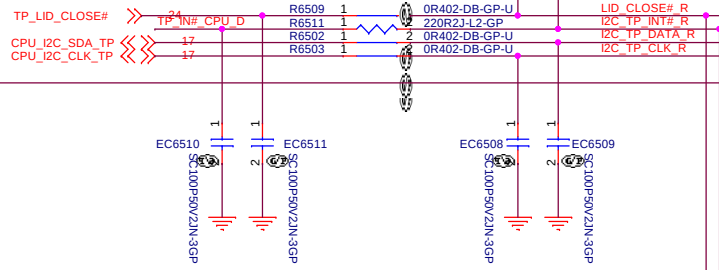
click pad

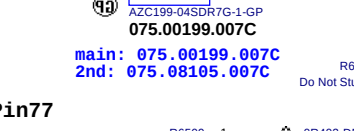
main: 075.00199.007C
2nd: 075.08105.007C



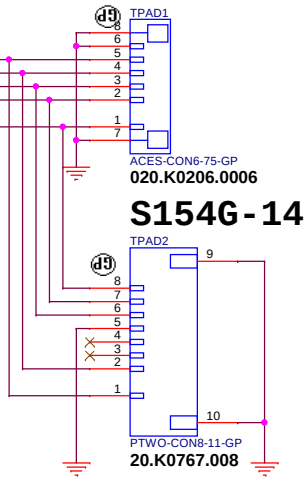


To KBC Pin77

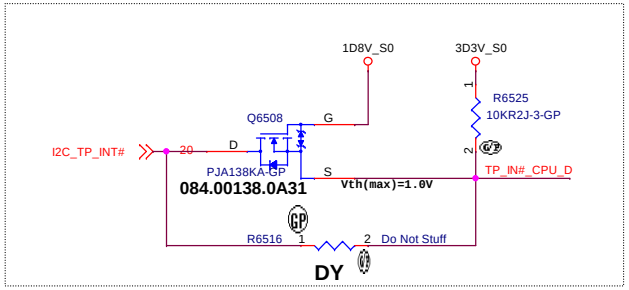


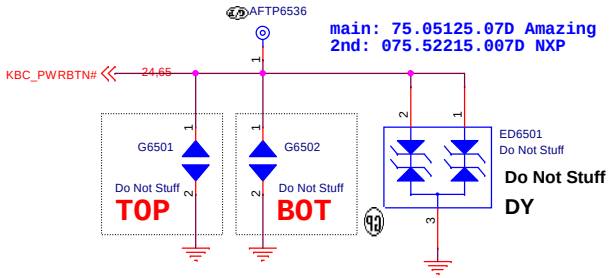


S151G-11'



S154G-14'





NEED CHECK PINDEFINE

LS1511G

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: INT IO (KB/TP)		
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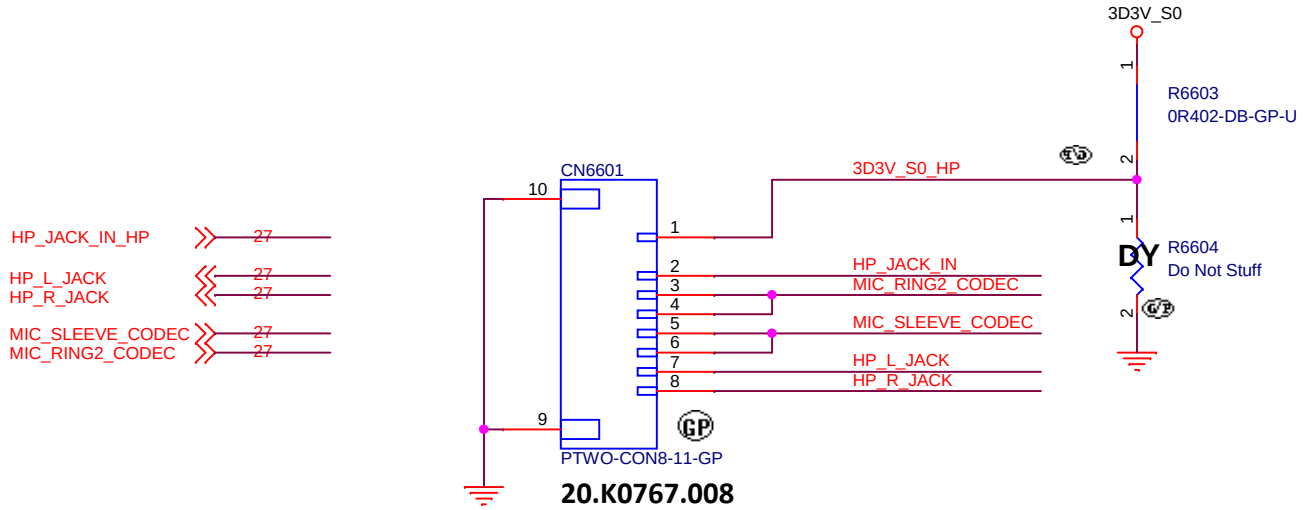
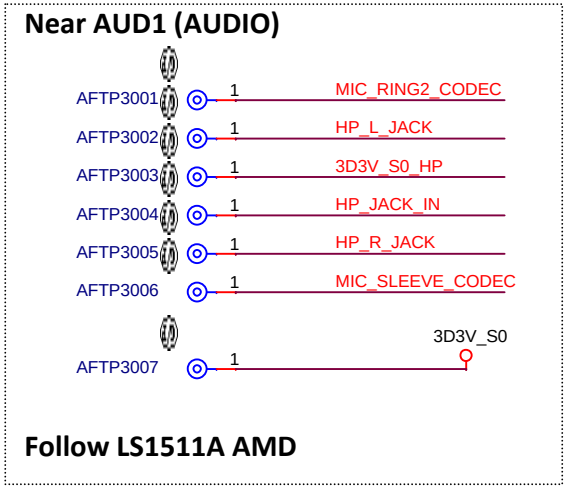
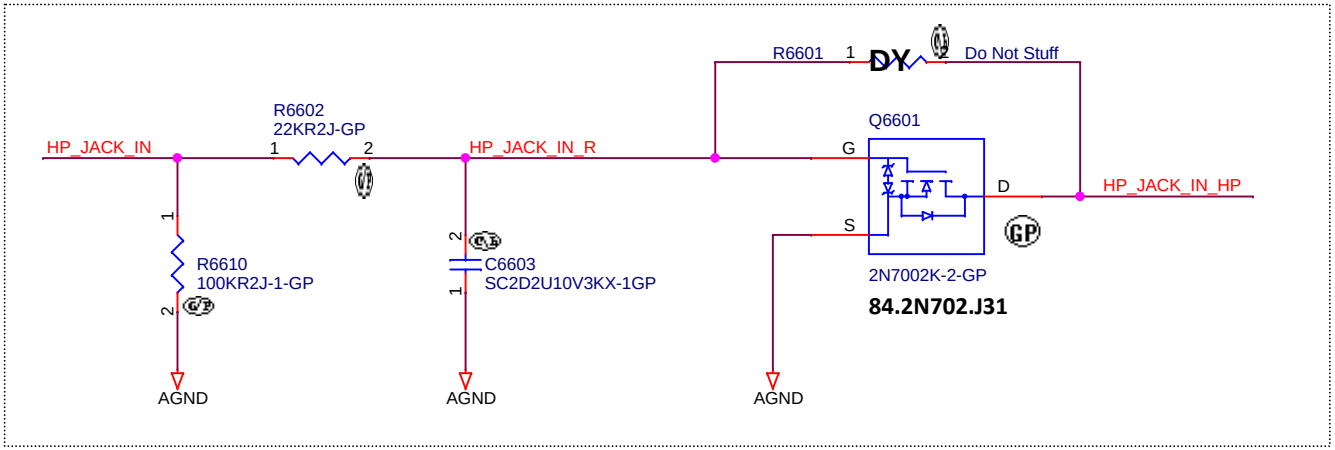




AUDIO JACK SENSE



LS1511G

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *IO Board Conn (USB/AUDIO/CR..etc)*

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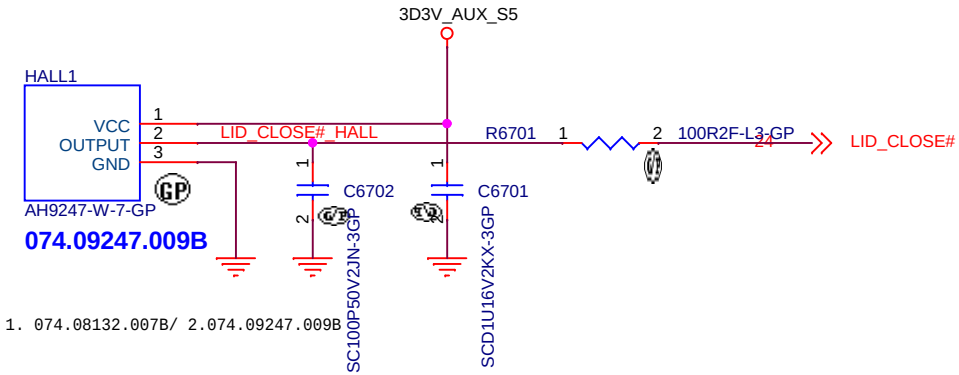
HALL SENSOR



1. 074.08132.007B/ 2.074.09247.009B

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Sensor (Hall-Sensor)*

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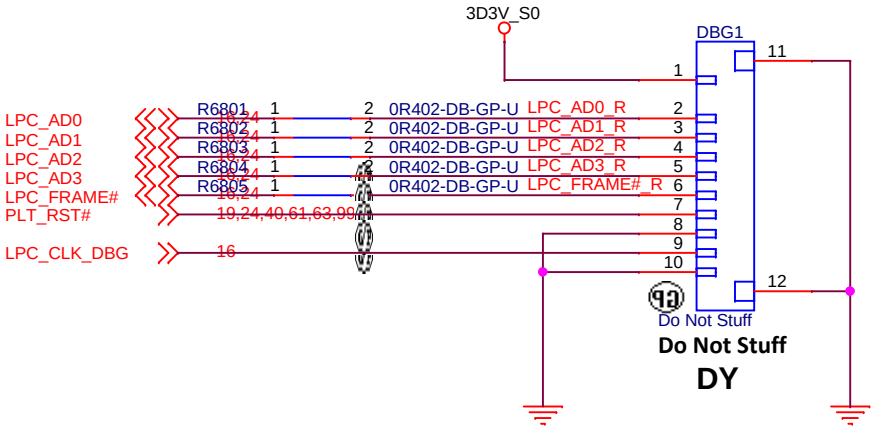
Main Func = Debug

Debug Connector



EVT: ASM
Other Stage: DY

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Title: ***Debug (LPC debug)***

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***Sensor (RSVD) (GYROSCOPE/PRESSU***

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Sensor (RSVD)***

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EXT IO (RSVD) (Thunderbolt(1/3)/Type C Re-driver)***

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

EXT IO (RSVD) (Thunderbolt(2/3)/TypeC Controller)

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EXT IO (RSVD) (Thunderbolt(3/3)/Type C Conn)***

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EXT IO ()RSVD) (TYPEC Power delivery/VBUS)***

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *EXT IO (RSVD)*

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU (RSVD) (PEG 1/5)***

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU (RSVD) (DIGITAL 2/5)*

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU (RSVD) (VRAM 3/5)*

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *GPU (RSVD) (GPIO 4/5)*		
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU (RSVD) (PWR/GND 5/5)***

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU (RSVD) (VRAM1,2 1/4)***

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU (RSVD) (VRAM3,4 2/4)*

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU (RSVD) (VRAM5,6 3/4)***

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *GPU (RSVD) (VRAM7,8 4/4)*

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU (RSVD) (Power_VGA_CORE)***

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***GPU (RSVD) (Power_others)***

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU (RSVD) (EE_Power)***

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緯創資通 **Wistron Corporation**
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Title: ***GPU (RSVD) (Discharge/Sequence)***

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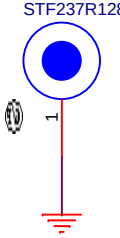
34.4YP25.001
HS1
STF237R128H34-4-GP



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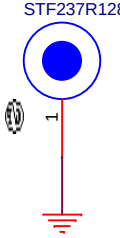
HS2
STF237R128H34-4-GP



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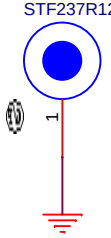
HS3
STF237R128H34-4-GP



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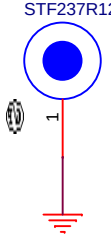
STF237R128H34-4-GP



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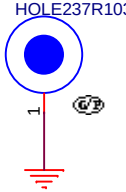
H2
HOLE237R103-GP



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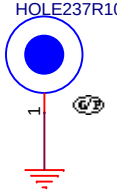
H3
HOLE237R103-GP



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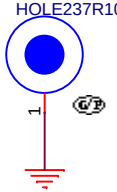
H4
HOLE237R103-GP



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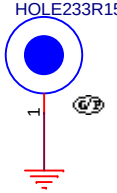
H13
HOLE233R154-GP



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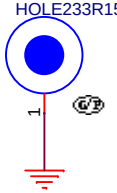
H14
HOLE233R154-GP



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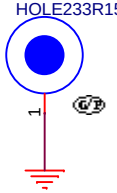
H15
HOLE233R154-GP



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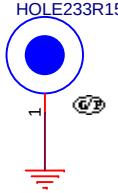
HOLE233R154-GP



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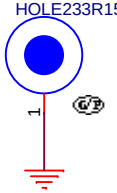
HOLE233R154-GP



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Title
UNUSED PARTS (RF/EMI Capacitors)

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *INT IO (RSVD) (NFC)*

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: INT IO (RSVD) (TPM)		
Size: A4	Document Number: LS1511G	Rev: -1M
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Title: ***INT IO (RSVD) (Finger Printer)***		
Size: A4	Document Number: **LS1511G**	Rev: **-1M**
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Title: ***EXT IO (RSVD) (Express Card/PCIE slot)***

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EXT IO (RSVD) (Smart Card/COM/PS2)***

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EXT IO (RSVD) (Docking/LPT)***

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Commercial (RSVD) (SW GFX eDP)***

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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Commercial (RSVD) (Intel LAN)***

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Commercial (RSVD) (LAN Switch)***

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DEBUG PORT

MIPI-60/XDP

CRB p159

XDP_TCK 20
XDP_TDI 20
XDP_TRST# 20
XDP_PRDY# 20
XDP_PTI_CLK0 20

CFG0 20
CFG1 20
CFG2 20
CFG3 20
CFG4 20
CFG5 20
CFG6 20
CFG7 20

PLT_RST# 19,24,40,61,63,68
PM_RSMRST# 19

XDP_UART_TXD 17
XDP_UART_RXD 17

CPU_SMB_SCL 17
CPU_SMB_SDA 17
XDP_BOOT_HALT 17
XDP_TDO 20

XDP_TMS 20
XDP_PREQ# 20

PM_RSTBTN# 19
PM_PWRBTN# 19,24

KBC_PWRBTN# 24,65
GPIO43_DSI_TE2 8

1D8V_S5
C9904 SCD1U16V2KX-L-GP
C9905 SCD1U16V2KX-L-GP
C9903 SC10U6D3V3MX-L-GP

XDP1
STC-CONN60A-GP-U1
20.F0971.060

XDP_TCK
XDP_TDI
XDP_PLT_RST#
XDP_TRST#
XDP_PRDY#
XDP_PTI_CLK0
XDP_TARGET_PRESENT_N
CFG0
CFG1
CFG2
CFG3
CFG4
CFG5
CFG6
CFG7
XDP_TMS
XDP_TDO
XDP_PM_RSTBTN#
TRST_PD
XDP_PREQ#
XDP_BOOT_HALT
BOOT_HALT_N
XDP_PM_PWRBTN#_CPU
XDP_PM_RSMRST#
XDP_I2C_SCL_LB
XDP_I2C_SDA_LB
XDP_UART_TXD
XDP_UART_RXD

0216 Del R9923

PM_RSTBTN# R9909 0R2J-L-GP XDP_PM_RSTBTN#
C9901 SCD1U16V2KX-L-GP

TRST_PD R9908 10KR2J-3-GP
R9919 4K7R2J-L-GP
R9922 1KR2J-L2-GP XDP_BOOT_HALT

PLT_RST# R9916 1KR2J-L2-GP XDP_PLT_RST#
PM_RSMRST# R9917 Do Not Stuff DY XDP_PM_RSMRST#
0220 Rename net
CPU_SMB_SDA R9914 Do Not Stuff DY XDP_I2C_SCL_LB
CPU_SMB_SCL R9918 Do Not Stuff DY XDP_I2C_SDA_LB

0216 Del R9913, R9911
0217 R9912 DY to XDP
XDP_PM_PWRBTN#_CPU R9912 0R2J-L-GP PM_PWRBTN#
C9902 SCD1U16V2KX-L-GP

1D8V_S5
0216 XDP to DY
R9910 Do Not Stuff
GPIO43_DSI_TE2 R9924 1KR2J-L2-GP XDP_TARGET_PRESENT_N
R9915 Do Not Stuff

connect to PWRBTN#
connect where?

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Title: Debug (XDP debug)

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Title: ***Table of Content***

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Title: ***Change History***

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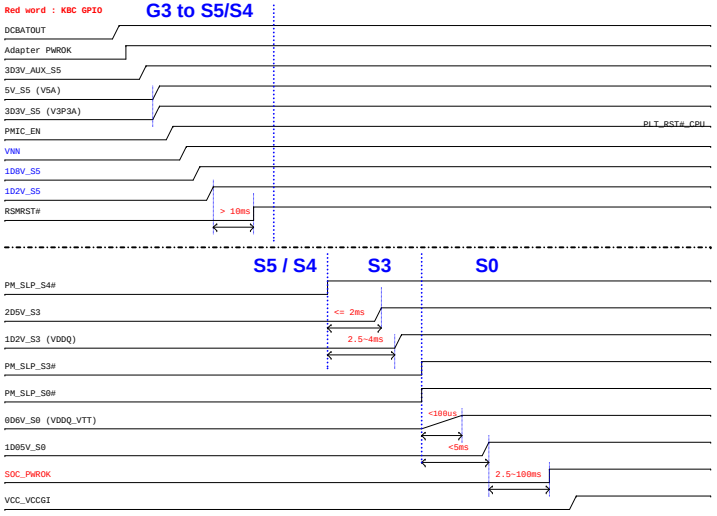
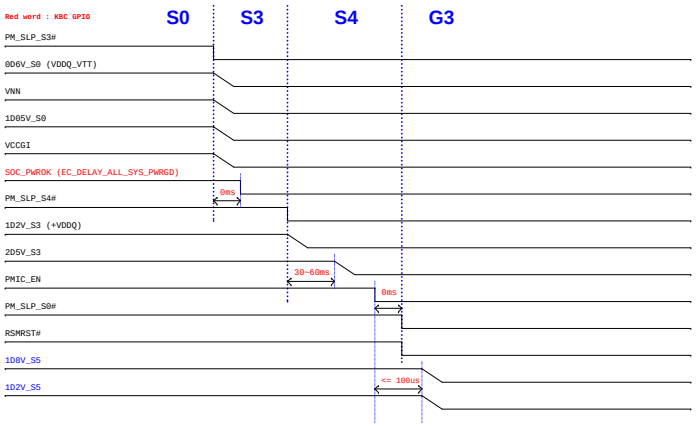
Intel-Power Up Sequence



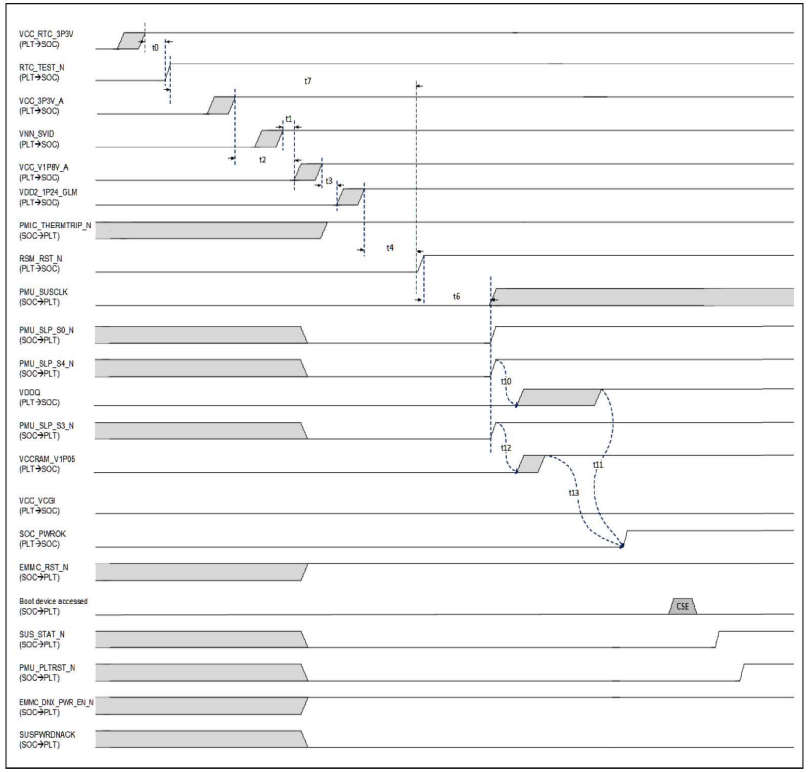
TBD

Intel-Power Down Sequence



Gemini Lake Sequence

Gemini Lake G3 Cold Boot Power-Up



PMIC Sequence

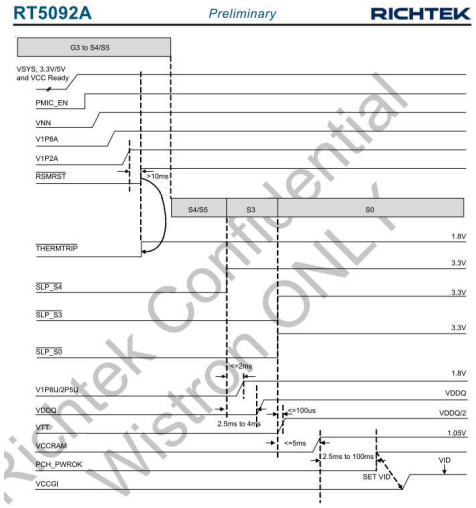


Figure 3. Power on Sequence

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Title: Power Sequence

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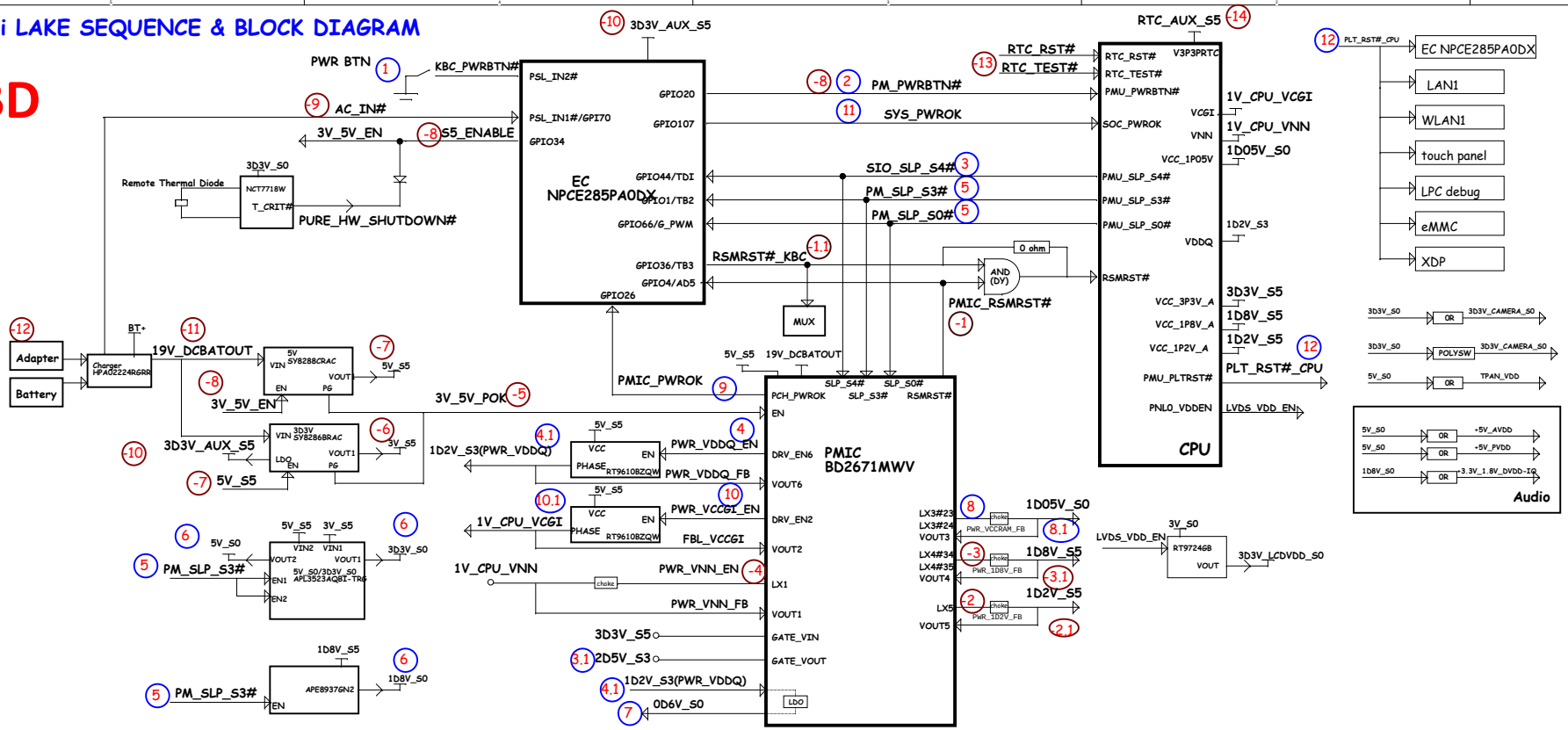
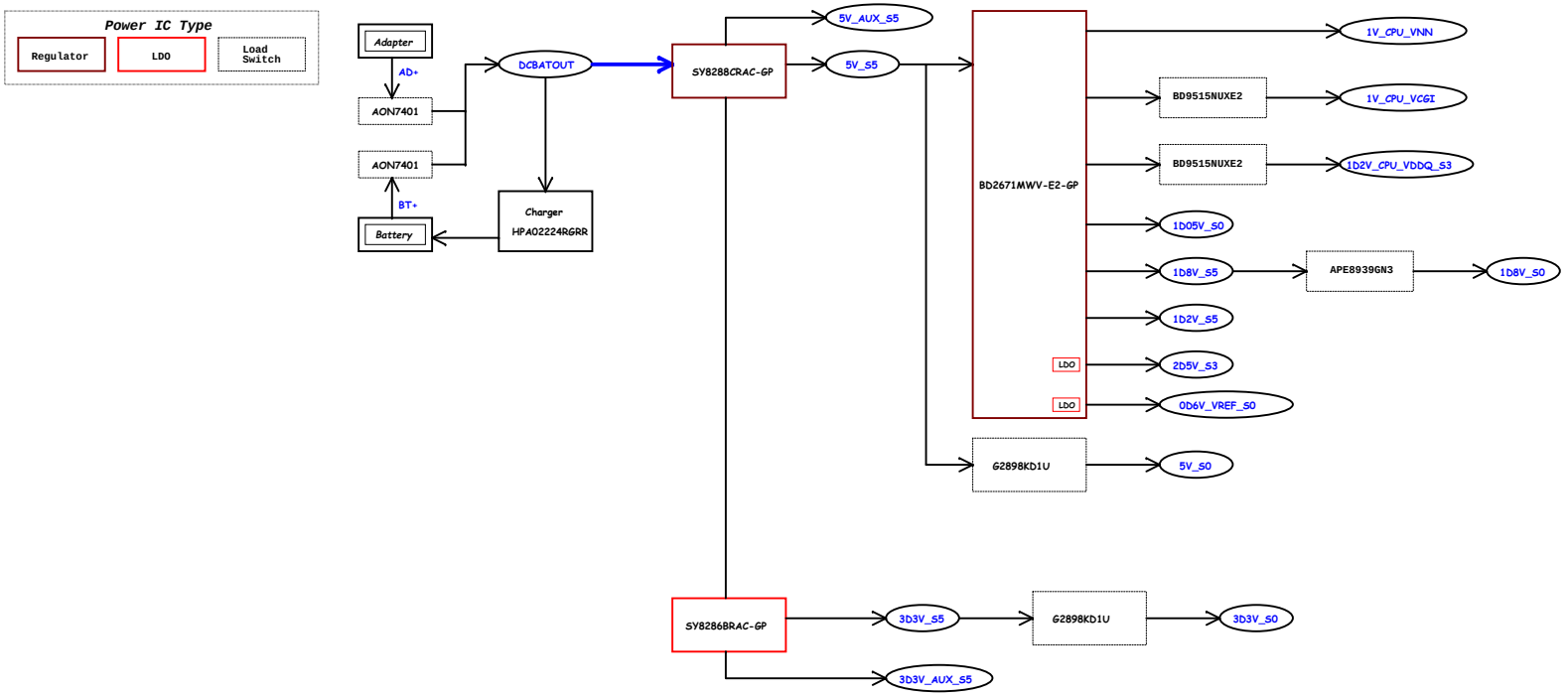
Gemini LAKE SEQUENCE & BLOCK DIAGRAM

TBD





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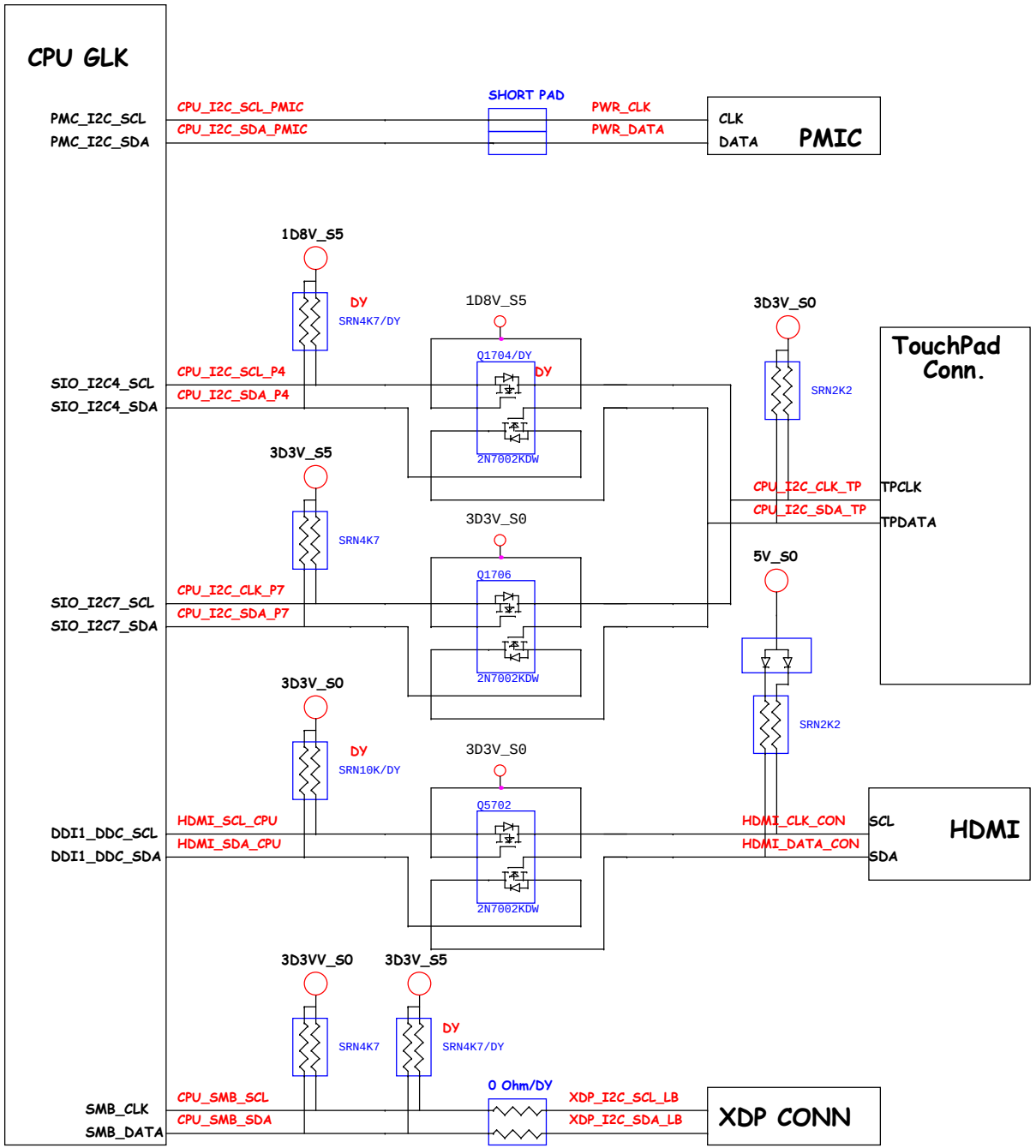
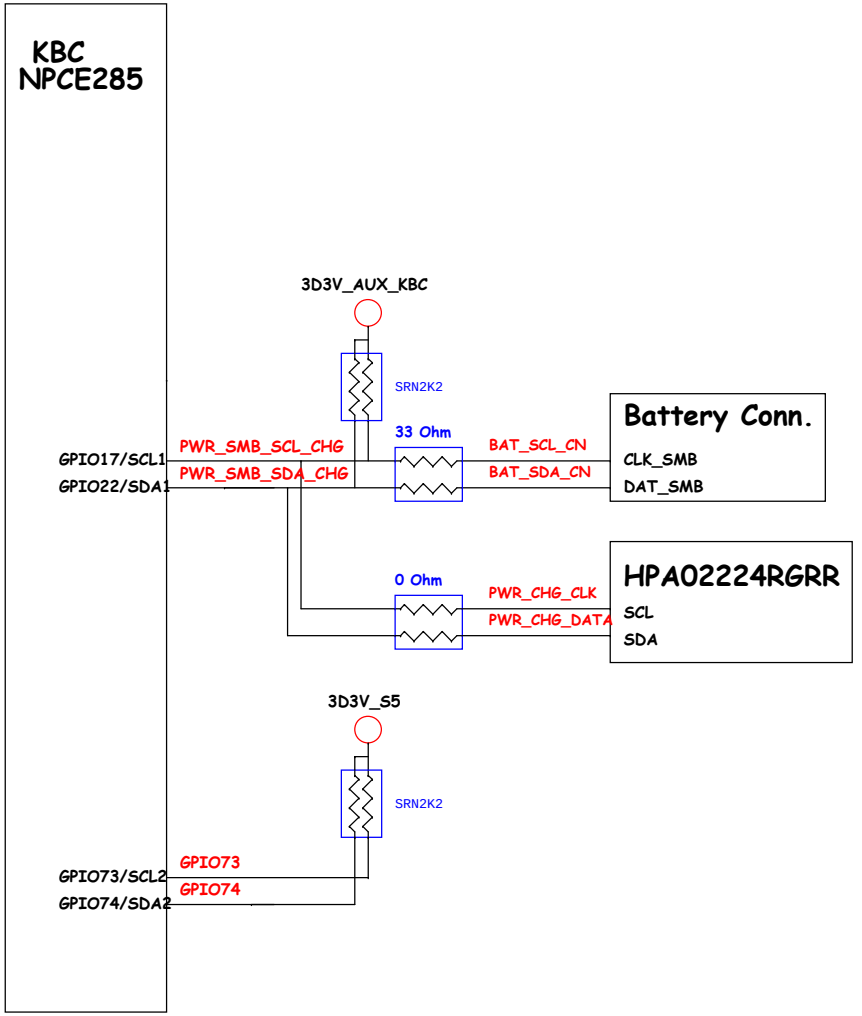
Power Block Diagram	-1M

PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: **SMBUS/I2C BLOCK DIAGRAM**

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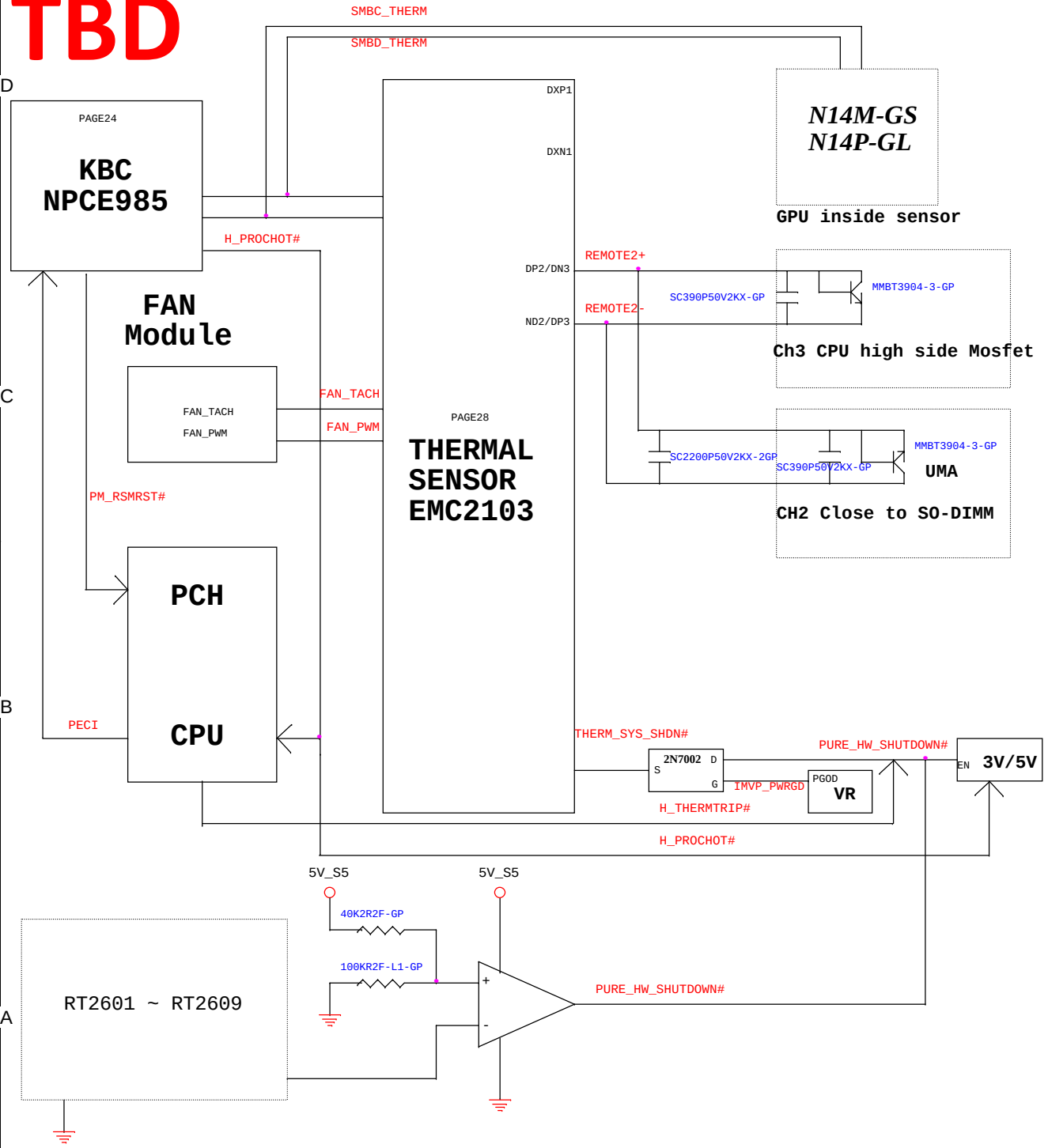
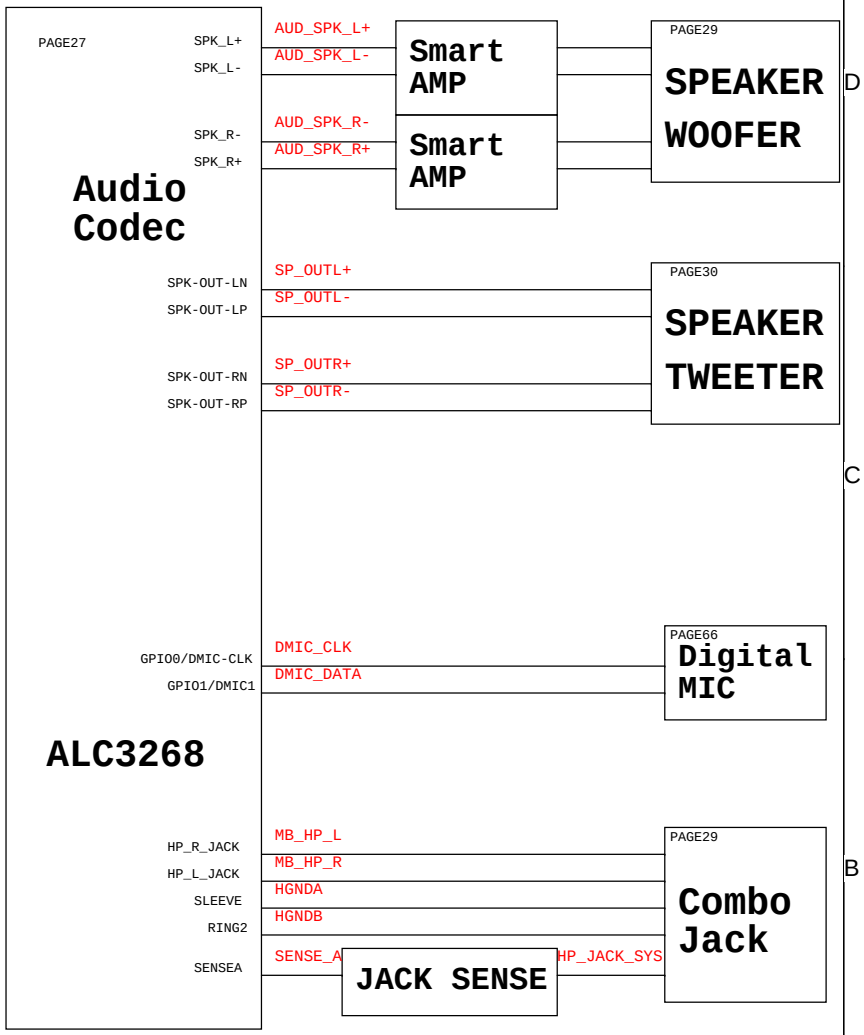
Thermal Block Diagram

TBD



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM		
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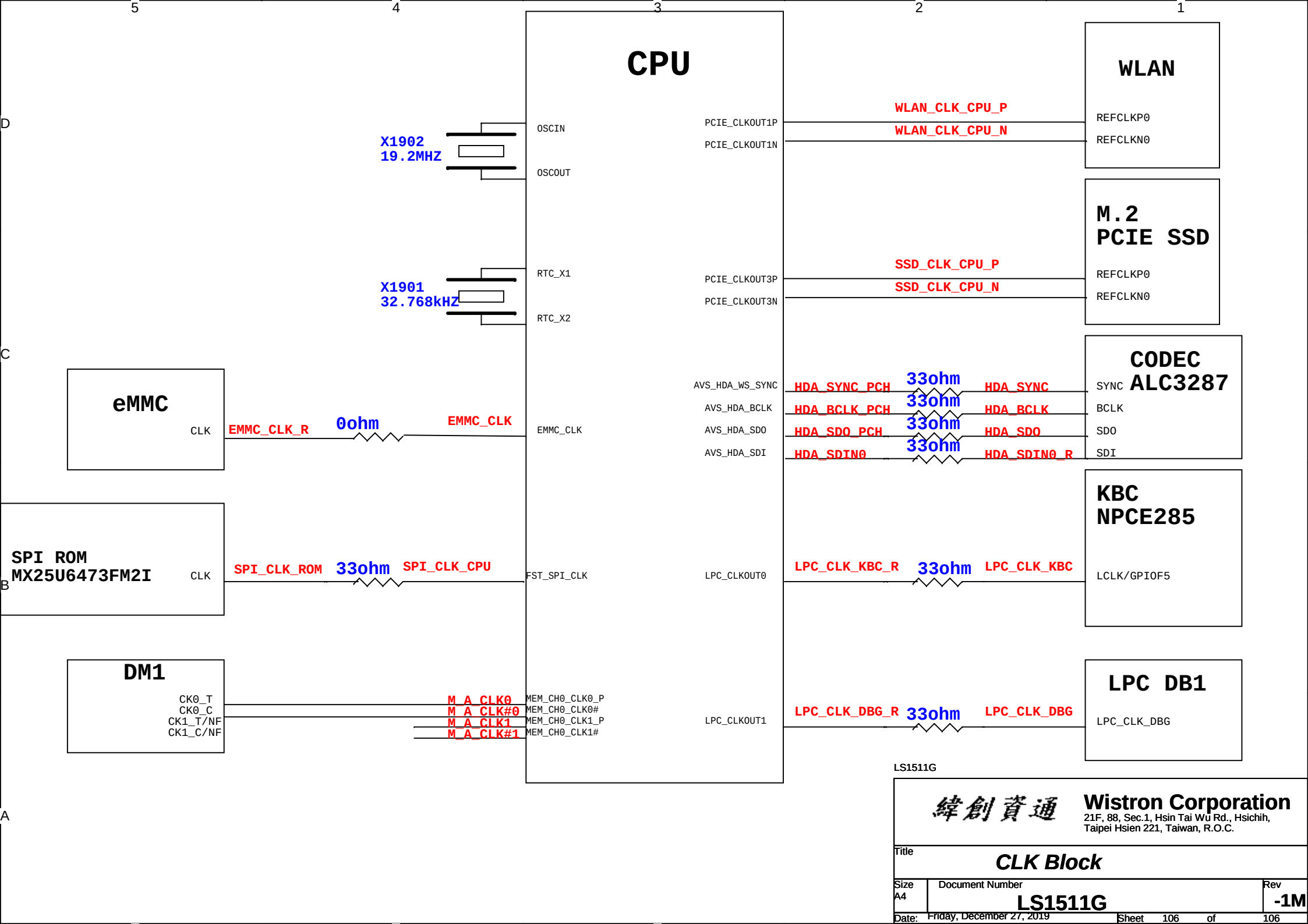

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Title	CLK Block	
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