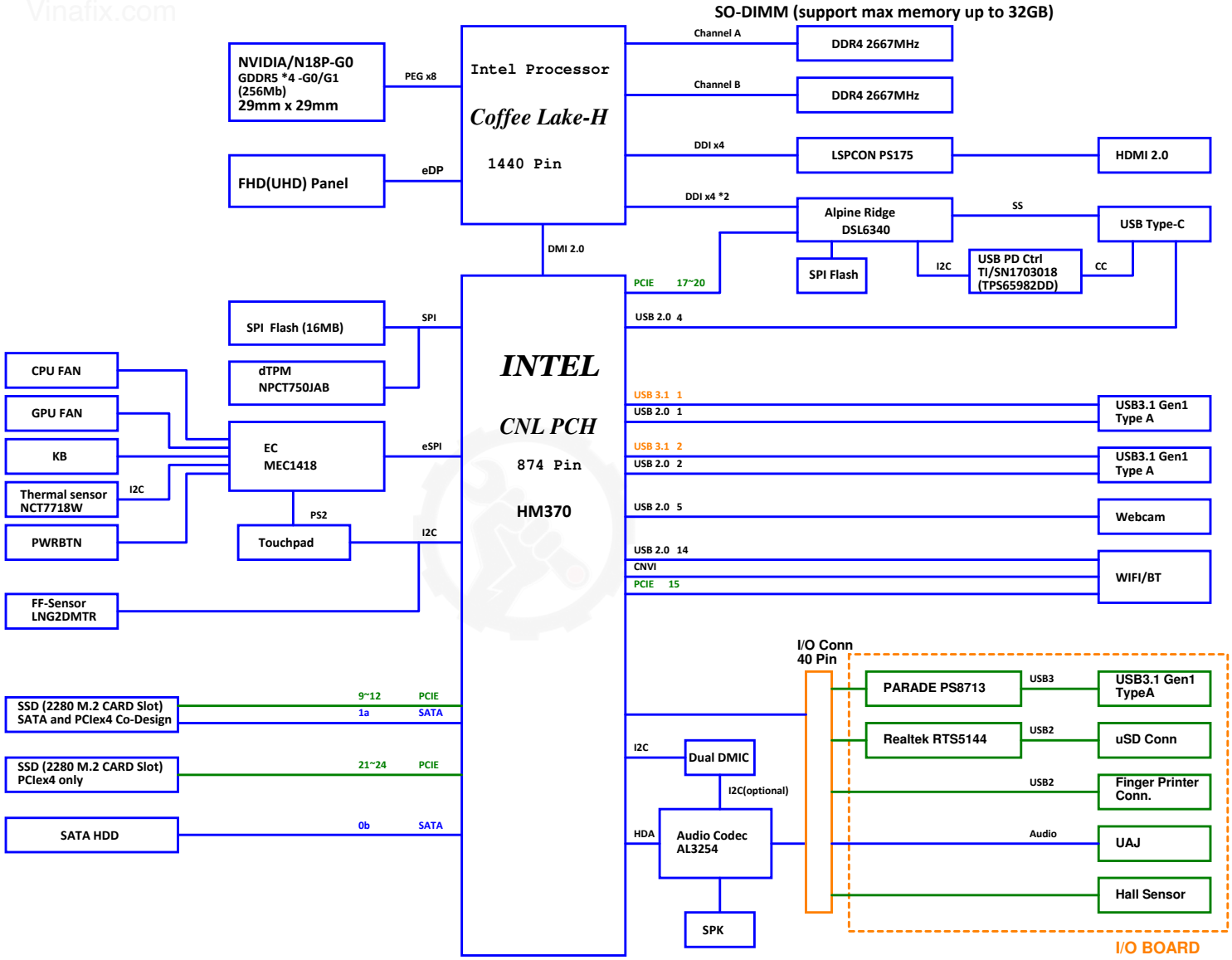
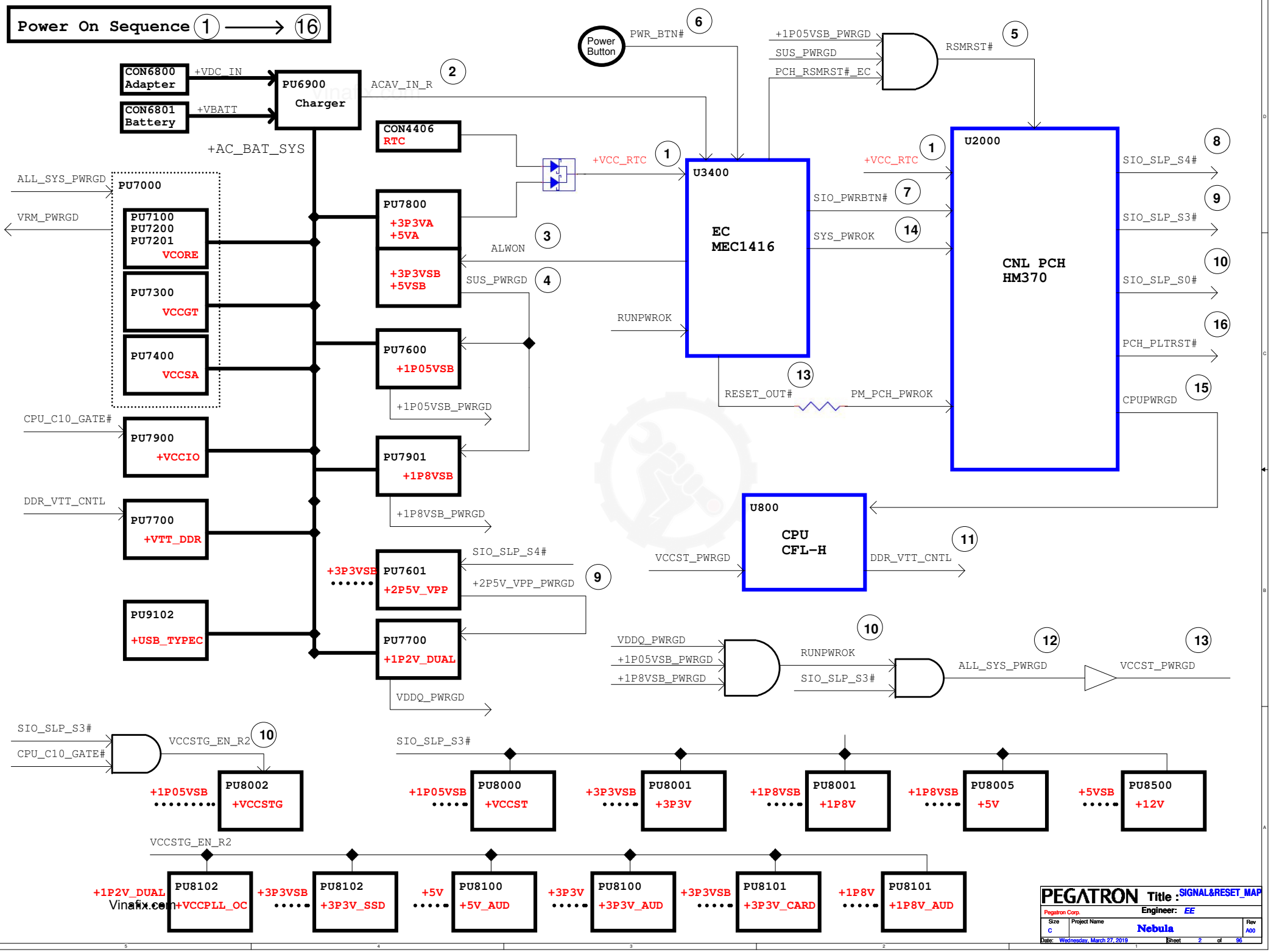
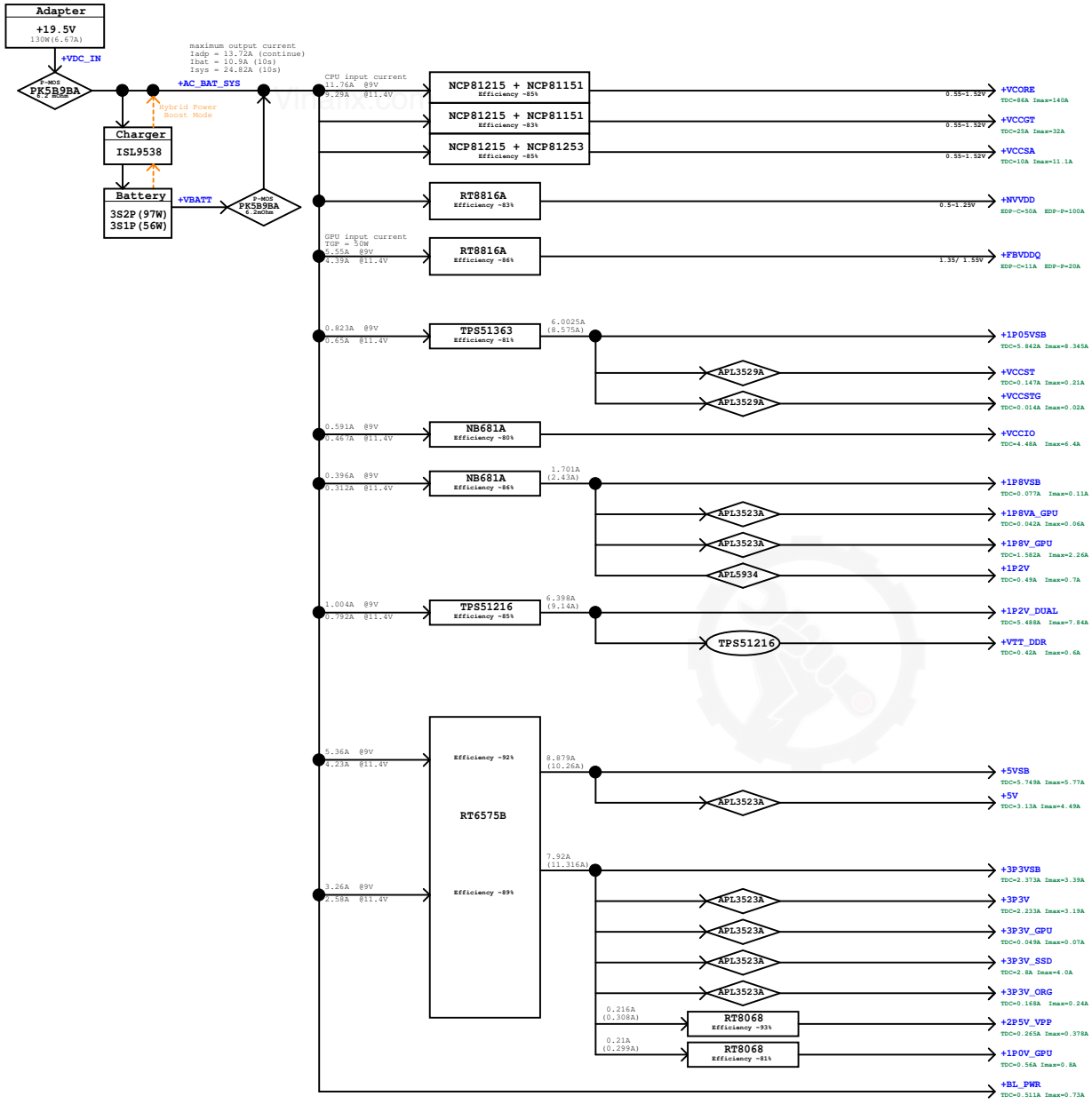
Nebula (Coffee Lake-H) Block Diagram



PEGATRON Title : BLOCK_DIAGRAM
Pegatron Corp. Engineer: EE
Size C | Project Name Nebula | Rev A00
Date: Wednesday, March 27, 2019 | Sheet 1 of 96


Power On Sequence 1 → 16
CON6800 Adapter
+VDC_IN
CON6801 Battery
+VBATT
PU6900 Charger
ACAV_IN_R
2
+AC_BAT_SYS
Power Button
PWR_BTN#
6
+1P05VSB_PWRGD
SUS_PWRGD
PCH_RSMRST#_EC
RSMRST#
5
CON4406 RTC
+VCC_RTC
1
U3400
EC MEC1416
+VCC_RTC
1
U2000
CNL PCH HM370
SIO_SLP_S4#
8
SIO_PWRBTN#
7
SIO_SLP_S3#
9
SYS_PWROK
14
SIO_SLP_S0#
10
ALL_SYS_PWRGD
PU7000
VRM_PWRGD
PU7100 PU7200 PU7201 VCORE
PU7300 VCCGT
PU7400 VCCSA
PU7800 +3P3VA +5VA
+3P3VSB +5VSB
ALWON
3
SUS_PWRGD
4
RUNPWROK
PU7600 +1P05VSB
+1P05VSB_PWRGD
PU7901 +1P8VSB
+1P8VSB_PWRGD
RESET_OUT#
13
PM_PCH_PWROK
PCH_PLTRST#
16
CPUPWRGD
15
CPU_C10_GATE#
PU7900 +VCCIO
DDR_VTT_CNTL
PU7700 +VTT_DDR
U800
CPU CFL-H
VCCST_PWRGD
DDR_VTT_CNTL
11
+3P3VSB
PU7601 +2P5V_VPP
SIO_SLP_S4#
+2P5V_VPP_PWRGD
9
PU9102 +USB_TYPEC
PU7700 +1P2V_DUAL
VDDQ_PWRGD
VDDQ_PWRGD
+1P05VSB_PWRGD
+1P8VSB_PWRGD
10
RUNPWROK
SIO_SLP_S3#
12
ALL_SYS_PWRGD
13
VCCST_PWRGD
SIO_SLP_S3#
CPU_C10_GATE#
VCCSTG_EN_R2
10
+1P05VSB
PU8002 +VCCSTG
SIO_SLP_S3#
+1P05VSB
PU8000 +VCCST
+3P3VSB
PU8001 +3P3V
+1P8VSB
PU8001 +1P8V
+1P8VSB
PU8005 +5V
+5VSB
PU8500 +12V
VCCSTG_EN_R2
+1P2V_DUAL
PU8102 +VCCPLL_OC
+3P3VSB
PU8102 +3P3V_SSD
+5V
PU8100 +5V_AUD
+3P3V
PU8100 +3P3V_AUD
+3P3VSB
PU8101 +3P3V_CARD
+1P8V
PU8101 +1P8V_AUD
Vinafix.com
PEGATRON
Title : SIGNAL&RESET_MAP
Pegatron Corp.
Engineer: EE
Size C
Project Name Nebula
Rev A00
Date: Wednesday, March 27, 2019
Sheet 2 of 96



+1P8V - (AUD 200mA)
PCH,VCCPRIM_1P8 734mA
+1P8VA_GPU to GDDR5X ~1A

+5V - AUD,PVDD1/2 3000mA
AUD,AVDD1 200mA
(HotKey 105mA)
(Ghostkey 12mA)
(KB BL 842.6mA)
VRD,VCC 50mA
=> 3.25A
+5VA - PWR_BTN 70mA
KB 70mA
ELC 150mA
1VSB,VCC 0.56mA
1P2V,VCC 0.82mA
DAC 2mA
RD,VCC 1.5mA
=> 0.3A

+3P3VA - EC 100mA
EC ROM 20mA
Audio,VDDSTB 0.0001mA
Therm sensor, VCC 1.28mA
=>0.2A

+3P3VSB - PCH,VCCDSW 94mA
PCH 2140mA
SPI 20mA
LAN 277mA
AP,Power 1240mA
AP,PD 245mA
logic 0.001mA
sensor 0.15mA
polar 12mA
USB RD 300mA
TYPE-C RD 98mA
logic 4mA
NB681,VCC 0.15mA
logic 8mA
=>4.45A

+3P3V - DDR4,VDDSPD*2 100mA
Audio,DVDDIO 5mA
Audio,DVDD 10mA
EC,VCC 100mA
CLK RD 272mA
CLK buffer 65mA
other 12mA
=> 0.6A

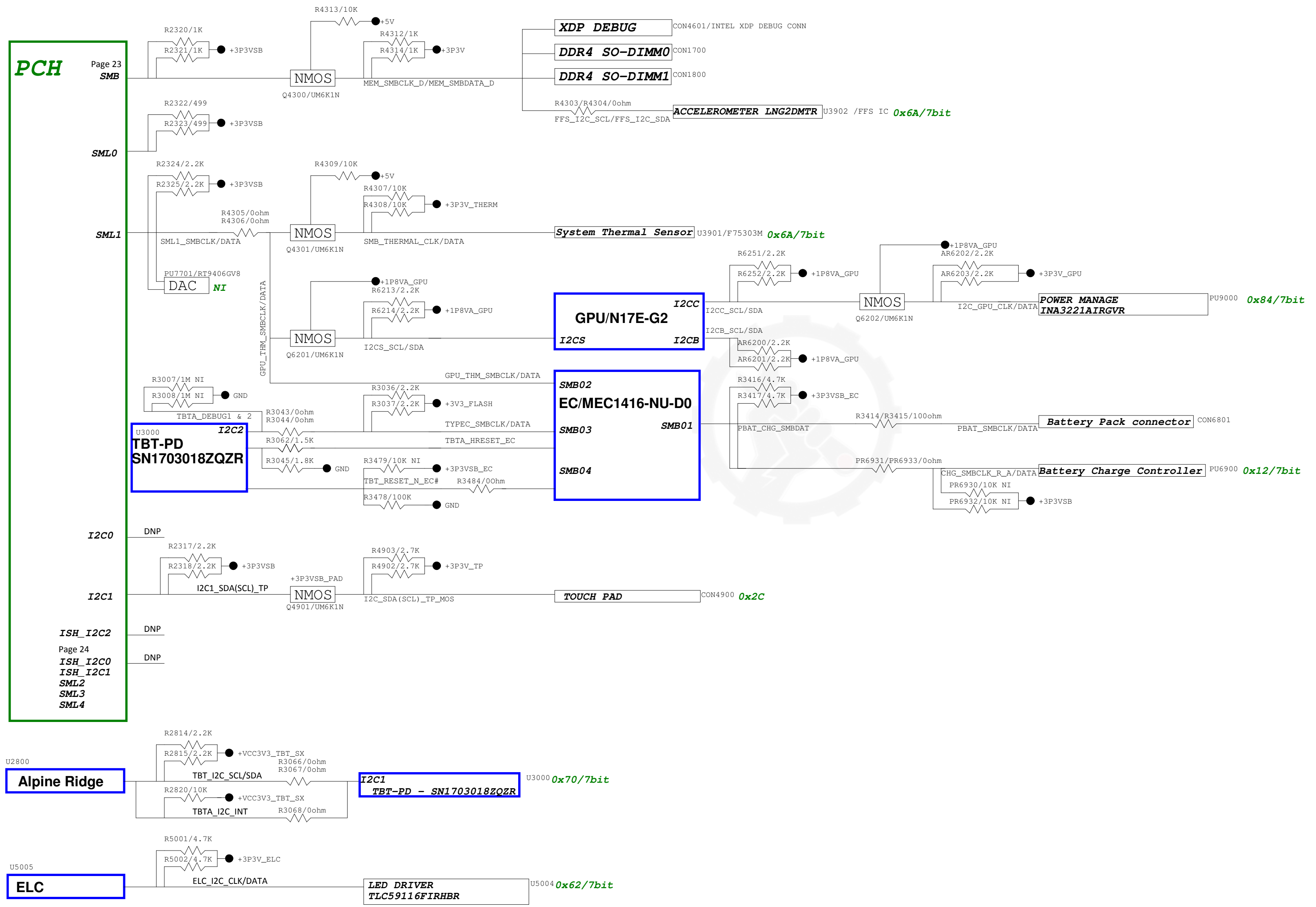
PEGATRON Title: POWER_FLOW_CHART
Pegatron Corp. Engineer: EE
Size: D | Project Name: Nebula | Rev: A00
Date: Wednesday, March 27, 2019 | Sheet 9 of 85

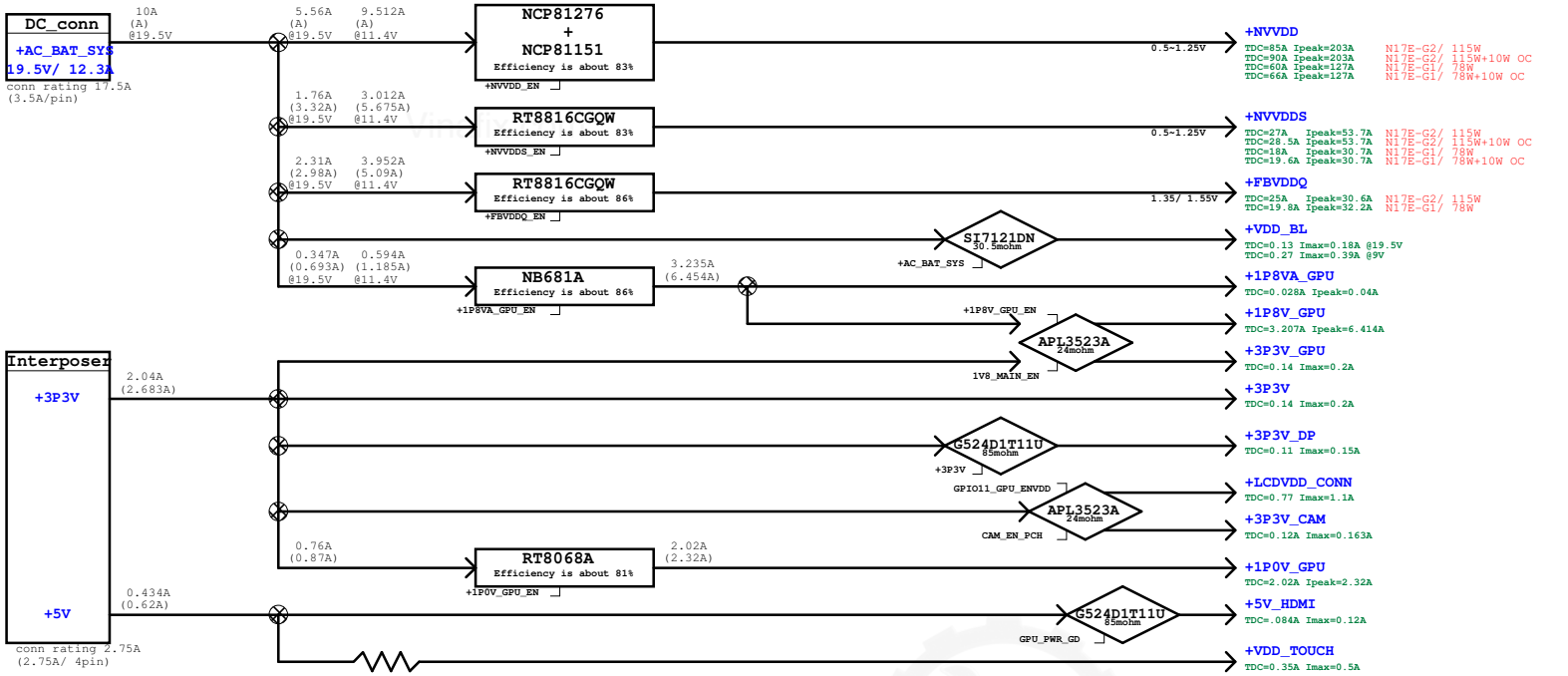
Schematics Change History

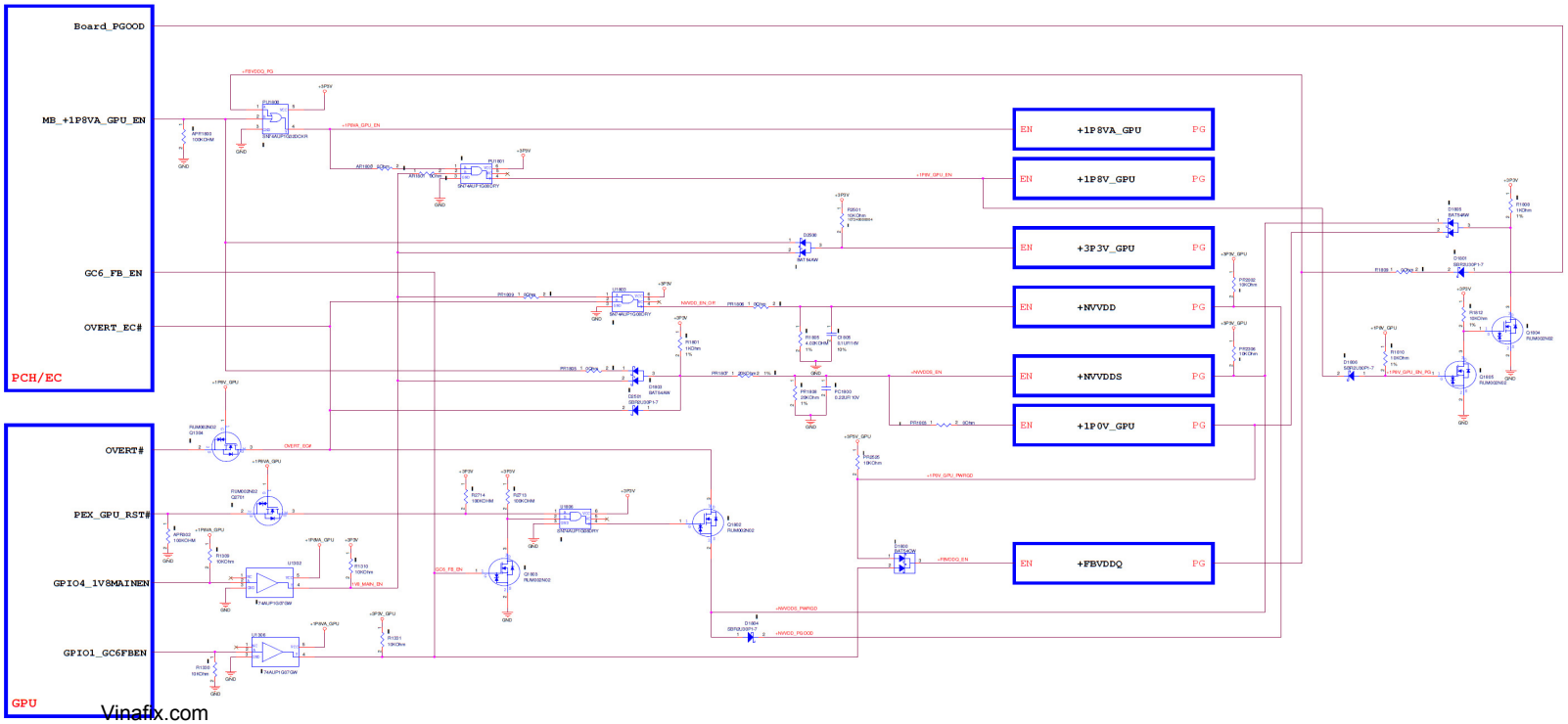
Version	Date	Description	Comments
1.00			

Vinafix.com

SMBUS & I2C Block Diagram







PEGATRON Title: GPU_Power_flow&sequence

Pegatron Corp. Engineer: EE

Size: Custom | Project Name: Nebula | Rev: A00

Date: Wednesday, March 27, 2019 Sheet 6 of 58

PEGATRON Title : POWER_SEQUENCE

Pegatron Corp. Engineer: EE

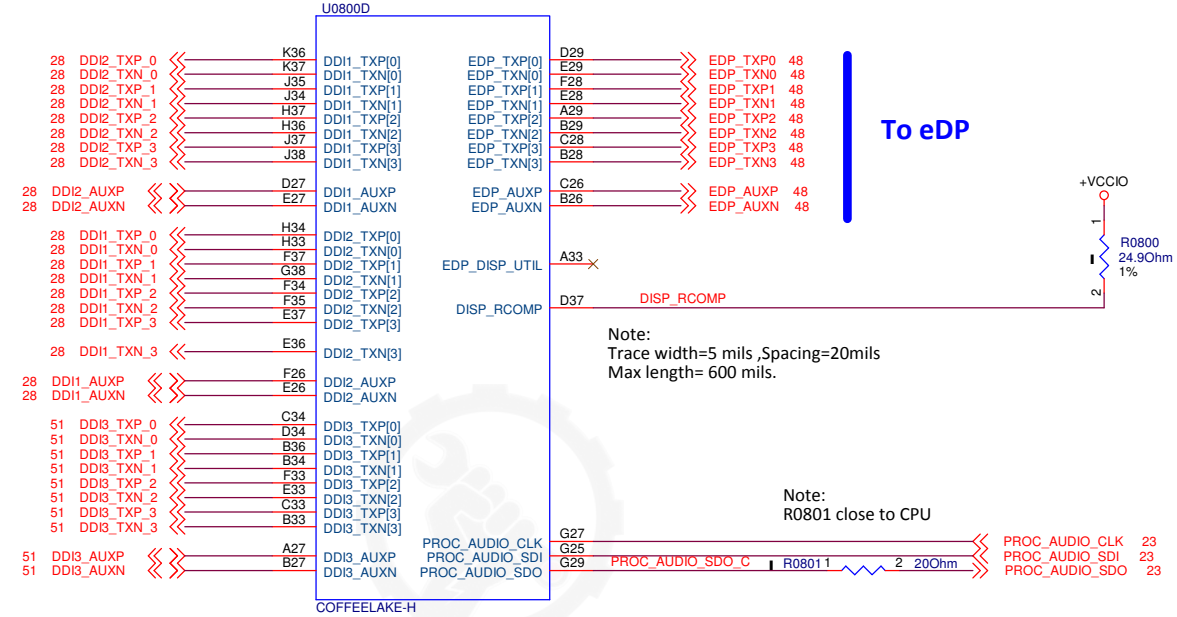
Size	Project Name	Rev
C	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 7 of 96

To Apline ridge

Swap DDI1 & DDI2
2018/06/21 Christopher_Jian

HDMI

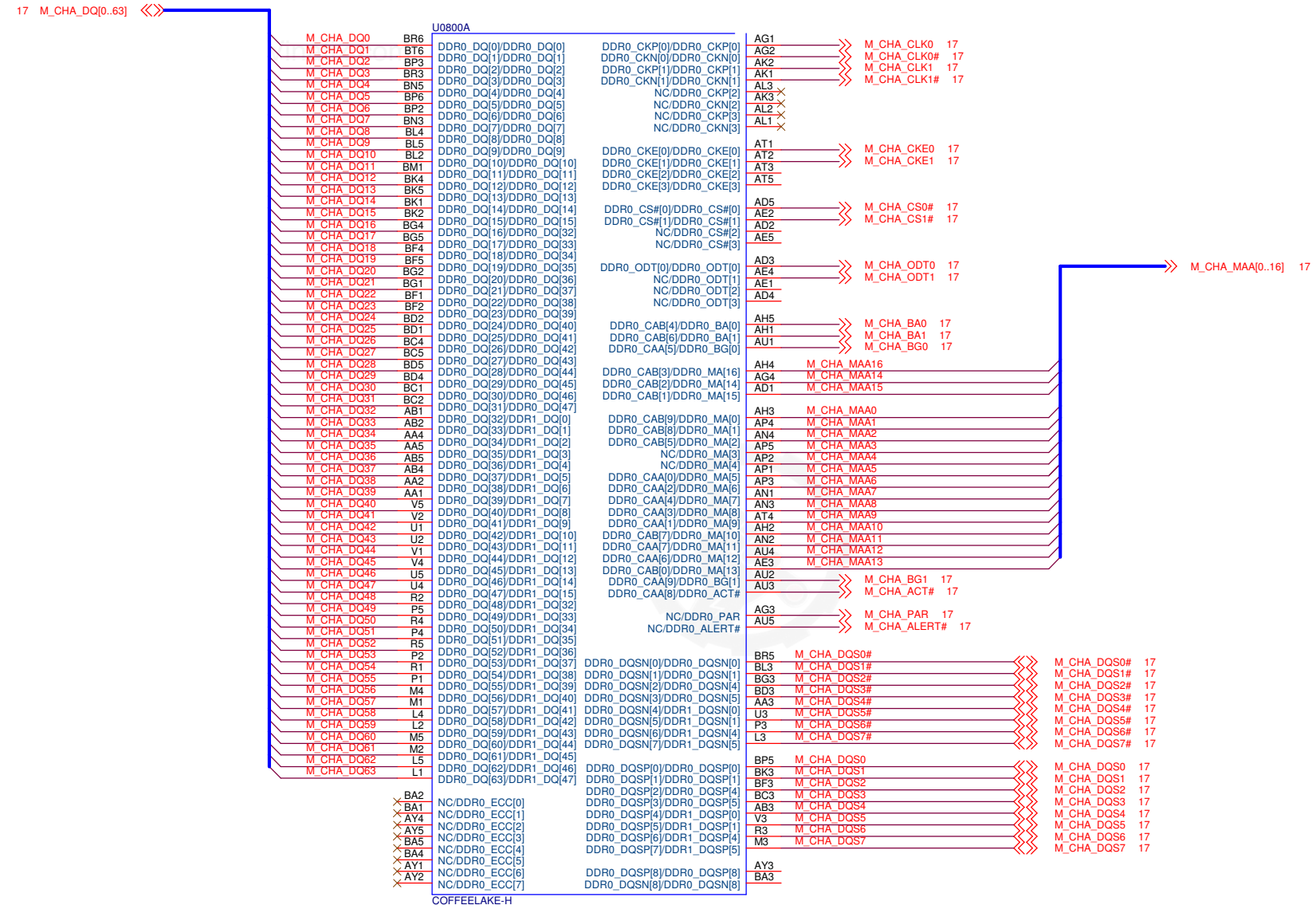


To eDP

Note:
Trace width=5 mils ,Spacing=20mils
Max length= 600 mils.

Note:
R0801 close to CPU

PEGATRON	Title : CPU_DDI/EDP	
Pegatron Corp.	Engineer: EE	
Size: B	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 8 of 96	

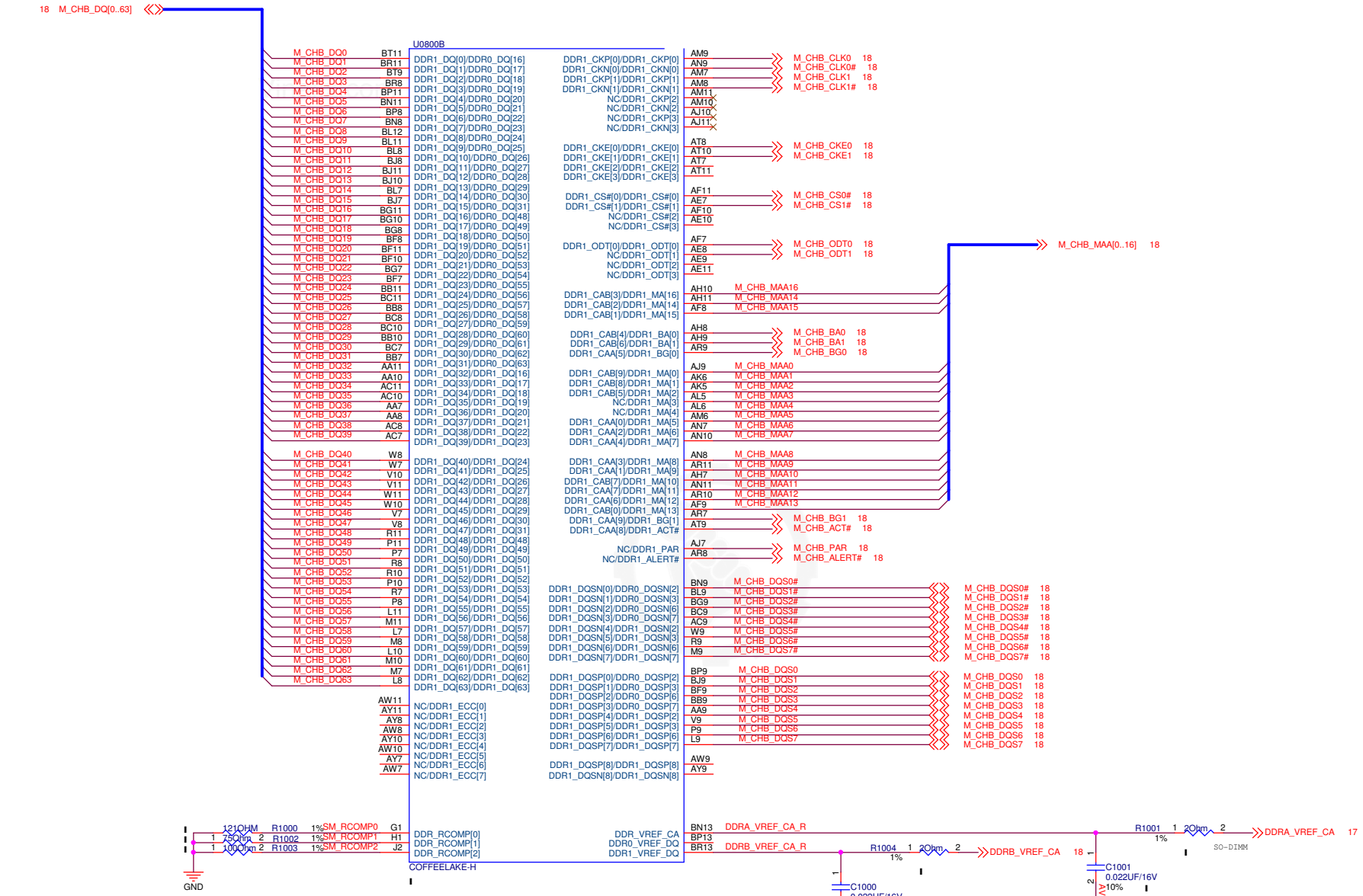


PEGATRON Title : CPU_DDR4_CHA

Pegatron Corp. Engineer: EE

Size	Project Name	Rev
B	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 9 of 96



Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω)			Min Trace Spacing (mils)				Max Length (mils)			R (Ω±1%) C(uF)	Notes
						Diff	Single Ended	Tolerance (%)	Diff	Group	Group to Group [1]/[2]	Byte [1]/[2]	Region	Breakout [1,2]	Total		
RCOMP [0]	M	MS	VSS	2	12-15					20	25/25				500	121	
RCOMP [1]	M	MS	VSS	2	12-15					20	25/25				500	75	
RCOMP [2]	M	MS	VSS	2	12-15					20	25/25				500	100	

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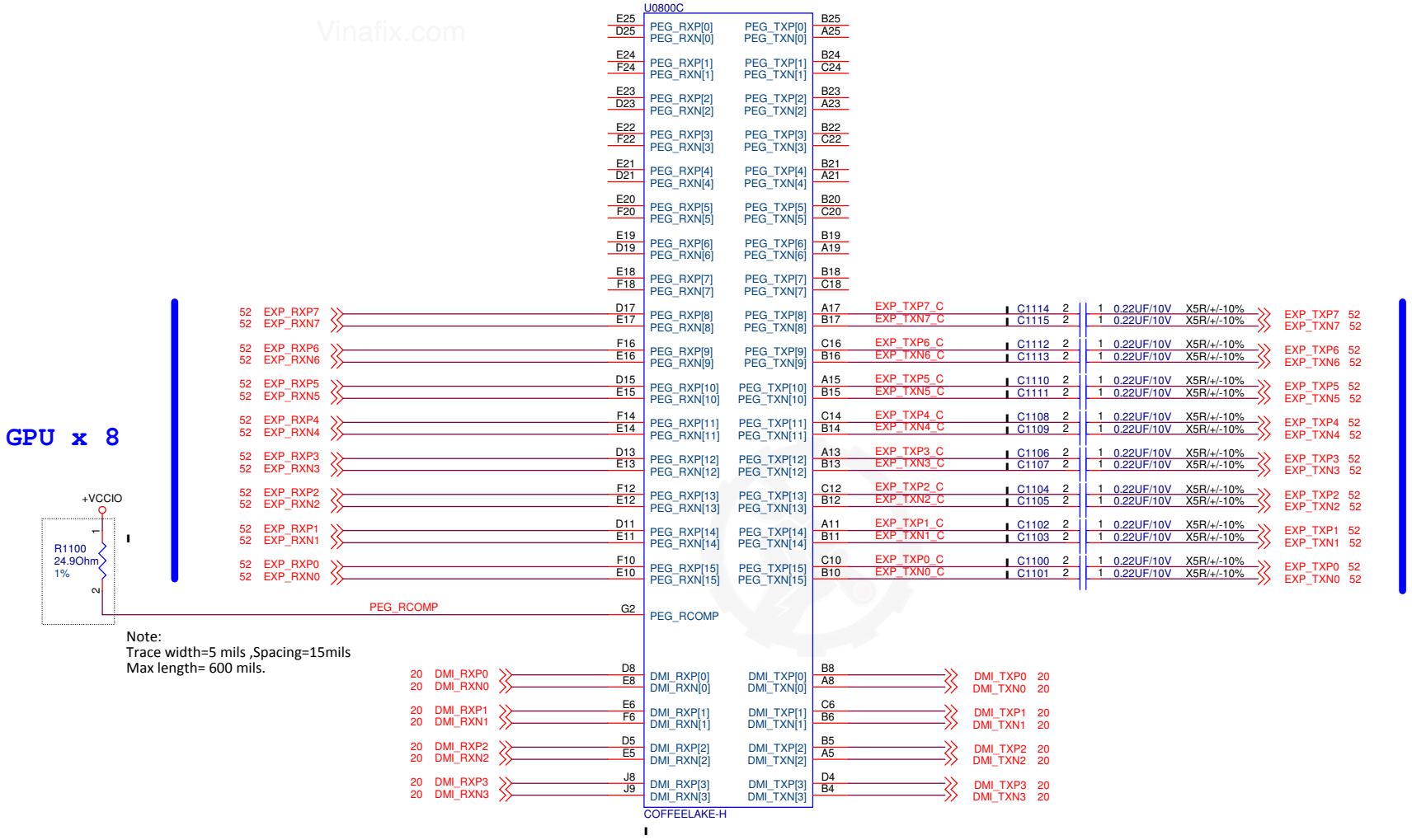
PEGATRON Title : CPU_DDR4_CHB

Pegatron Corp. Engineer: EE

Size	Project Name	Rev
Custom	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 10 of 96



Note:
Trace width=5 mils ,Spacing=15mils
Max length= 600 mils.

PEGATRON	Title : CPU_DMI/PEG		
Pegatron Corp.	Engineer: EE		
Size: B	Project Name: Nebula		Rev: A00
Date: Wednesday, March 27, 2019	Sheet 11 of 96		

Table 6-10. Processor Clocking Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BCLKP BCLKN	100 MHz Differential bus clock input to the processor	I		Diff	H and S-Processor Line
CLK24P CLK24N	24 MHz Differential bus clock input to the processor	I		Diff	
PCI_BCLKP PCI_BCLKN	100 MHz Clock for PCI Express* logic	I		Diff	

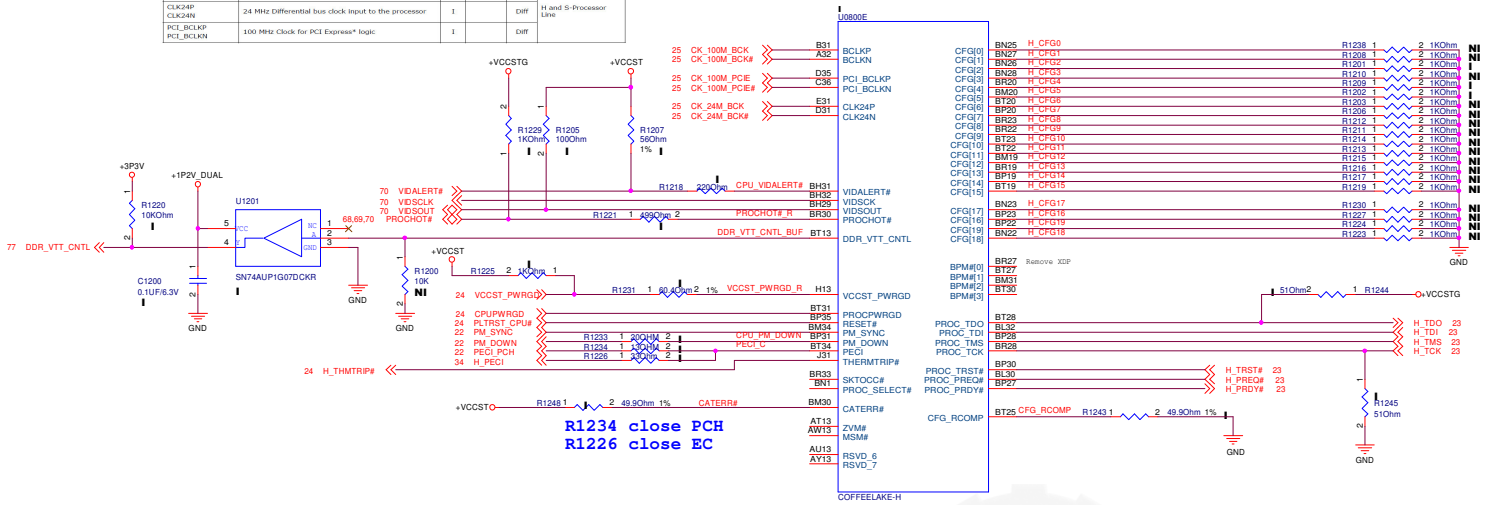


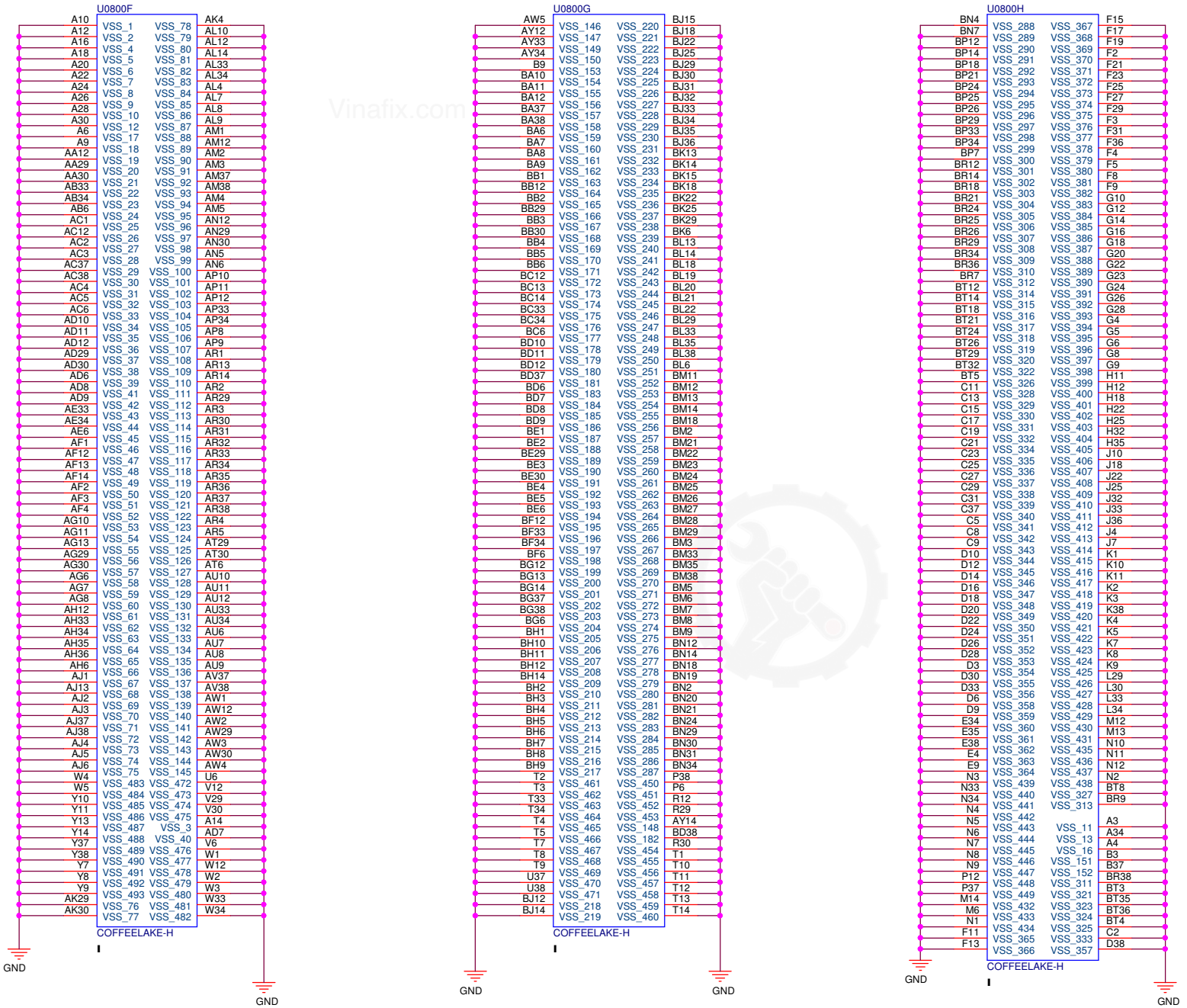
Table 51-39. Processor/PCH Strapping Checklist (Sheet 2 of 2)

Pin Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)	Default Value	✓
CFG[19:8]	Reserved configuration lands.			

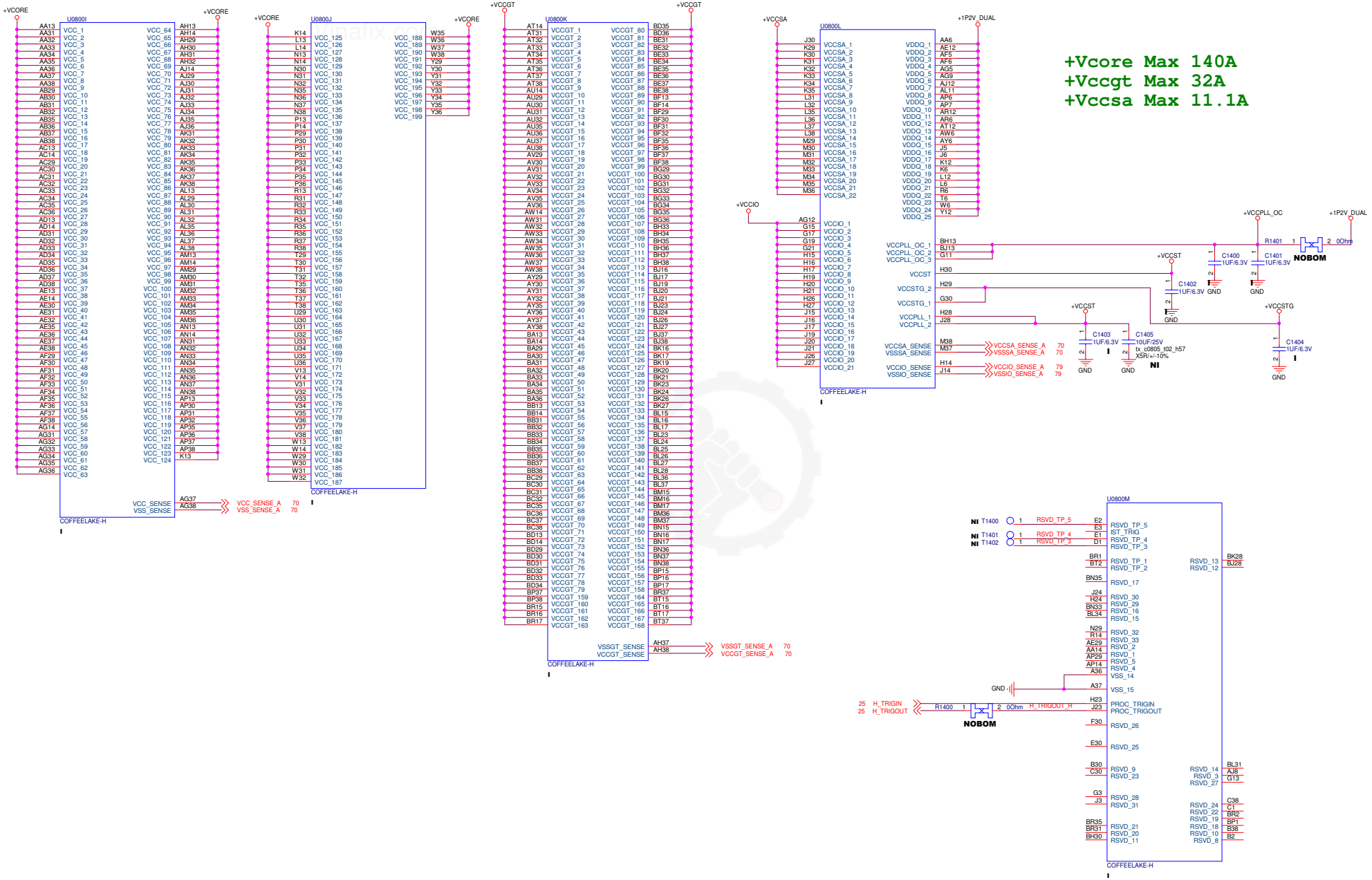
Table 6-7. Reset and Miscellaneous Signals

Signal Name	Description
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.

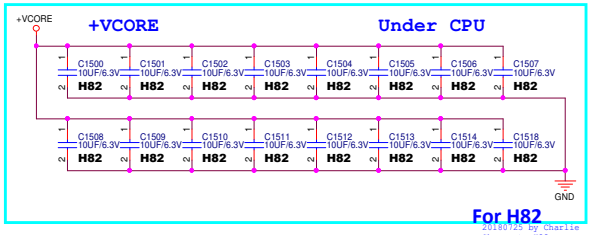
PEGATRON Title : CPU_MISC
Pegatron Corp. Engineer: EE
Size: Custom | Project Name: Nebula | Rev: A00
Date: Wednesday, March 27, 2019 | Sheet 12 of 98

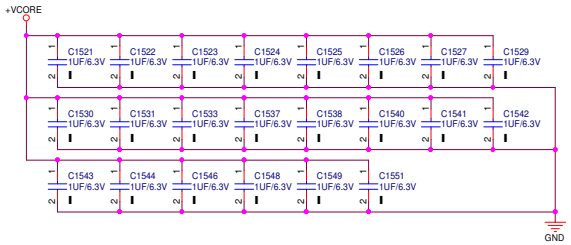


PEGATRON	Title : CPU_VSS		
Pegatron Corp.	Engineer: EE		
Size: B	Project Name: Nebula		Rev: A00
Date: Wednesday, March 27, 2019	Sheet 13 of 96		


+Vcore Max 140A
+Vccgt Max 32A
+Vccsa Max 11.1A
U0800I
U0800J
U0800K
U0800L
U0800M
COFFEELAKE-H
NOBOM
NI
Vinafix.com

+VCORE Under CPU





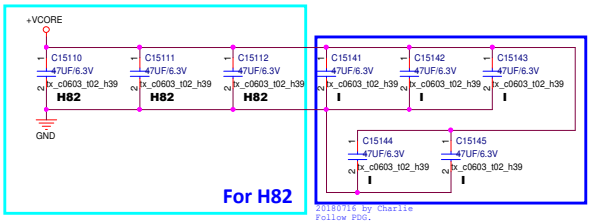
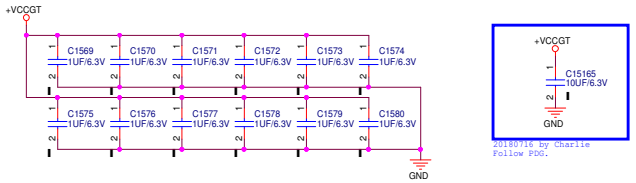


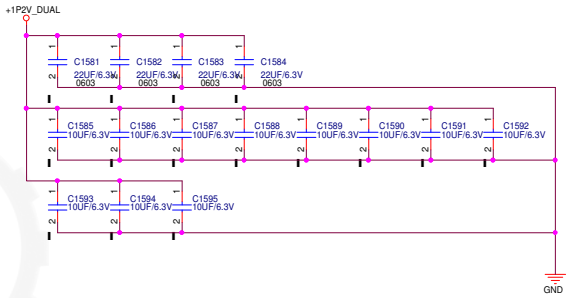
Table 50-3. Decoupling Requirements for CFL H Processor

Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
V_{CCGT}	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	
V_{CCSA}	2x 47uF 0805		
	2x 22uF 0603		
		7x 10uF 0402	
		1x 1uF 0201	
V_{DDQ}		4x 22uF 0603	
		11x 10uF 0402	
V_{CCIO}		3x 10uF 0402	
		3x 0402 (placeholder)	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.

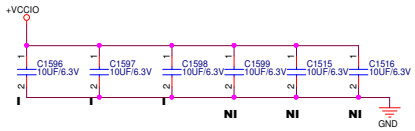
+VCCGT Under CPU



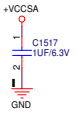
+1P2V_DUAL Under CPU



+VCCIO Under CPU



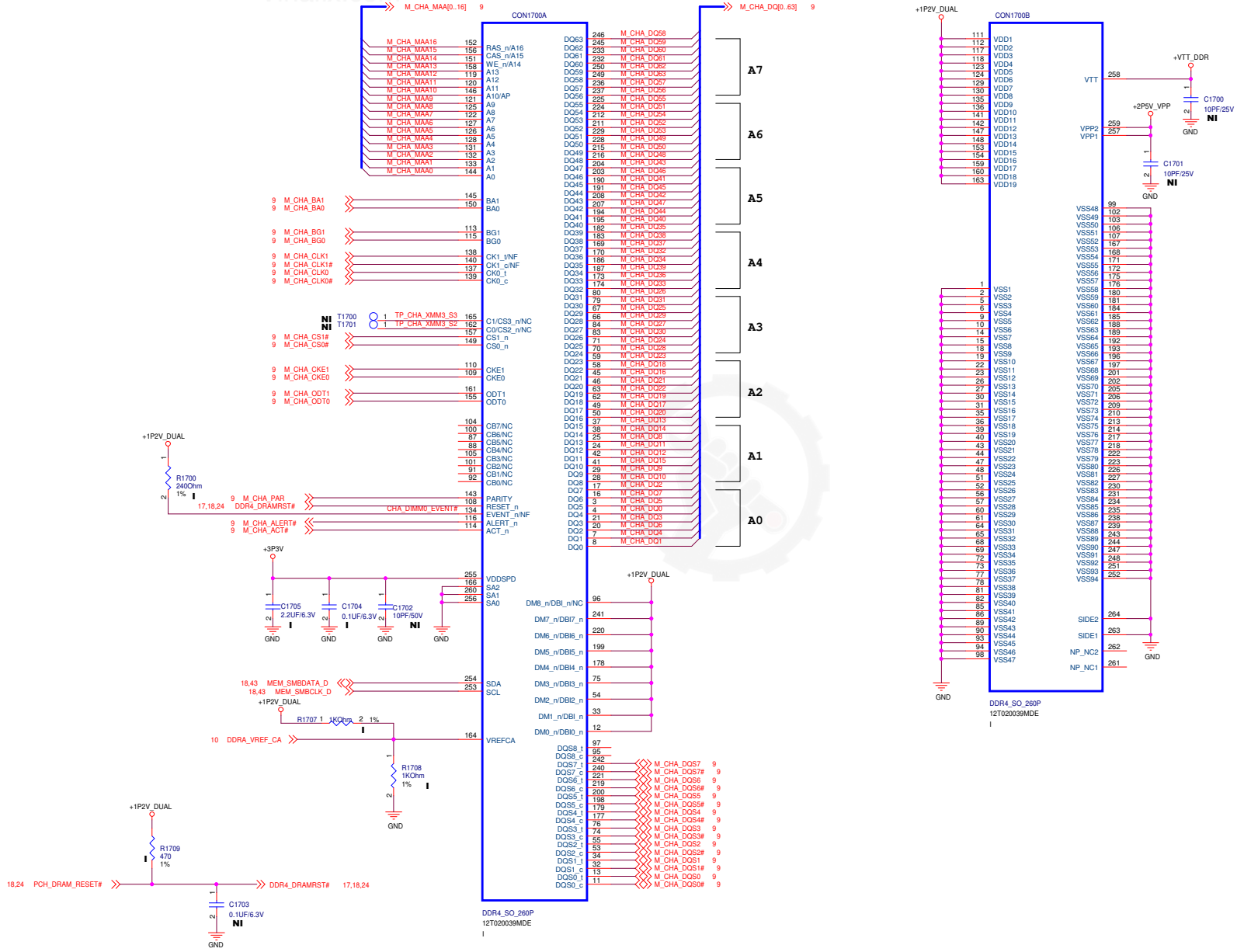
+VCCSA Under CPU



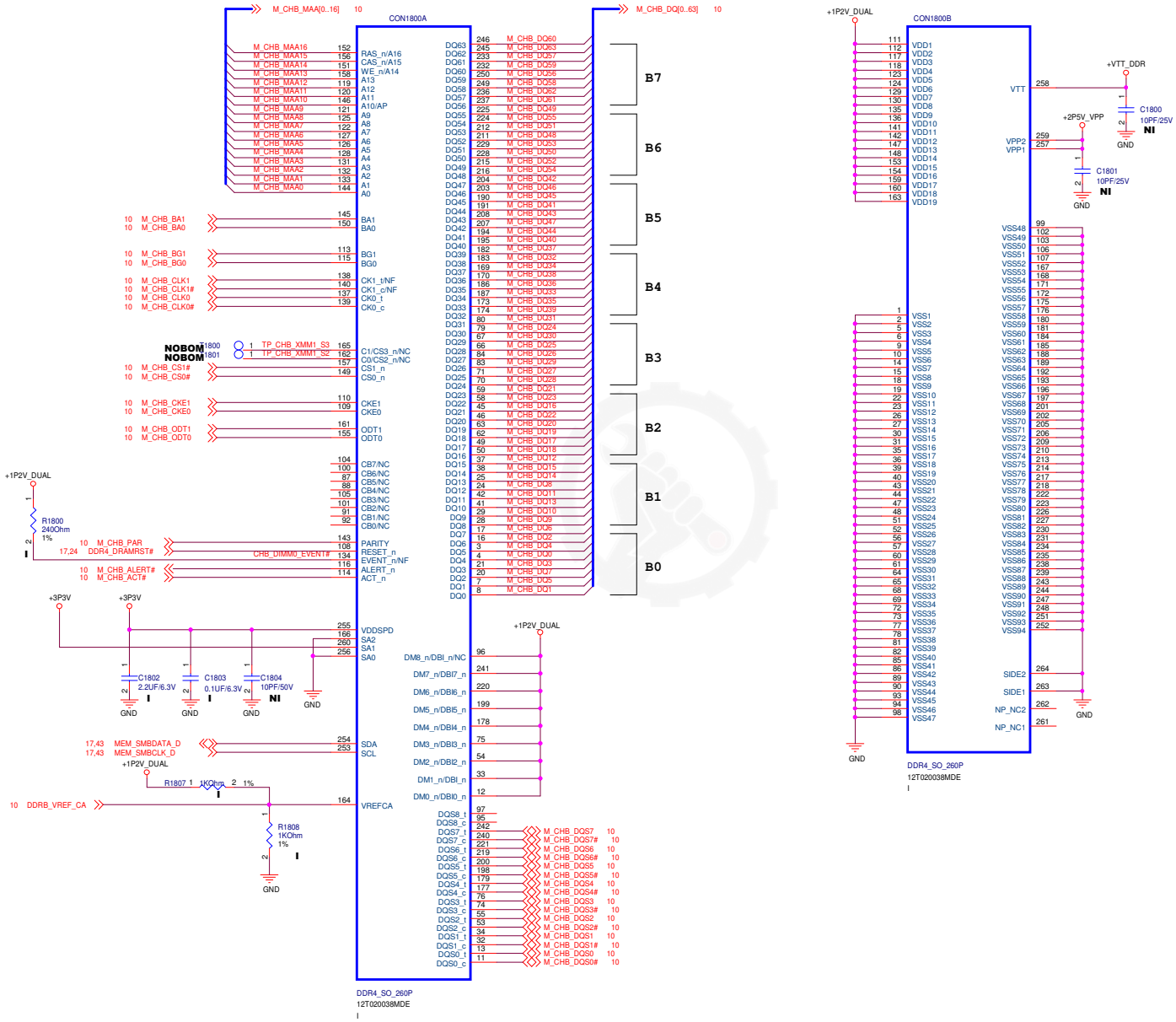
PEGATRON Title : CPU_DECOUPLING
Pegatron Corp. Engineer: EE
Size C | Project Name Nebula | Rev A00
Date: Wednesday, March 27, 2019 Sheet 15 of 96

Reserve Page

PEGATRON	Title : XXX		
Pegatron Corp.	Engineer: EE		
Size: B	Project Name: Nebula		Rev: A00
Date: Wednesday, March 27, 2019	Sheet 16 of 96		



PEGATRON	Title : DDR4_SO-DIMM0		
Pegatron Corp.	Engineer: EE		
Size: C	Project Name: Nebula		Rev: A00
Date: Wednesday, March 27, 2019	Sheet 17 of 96		

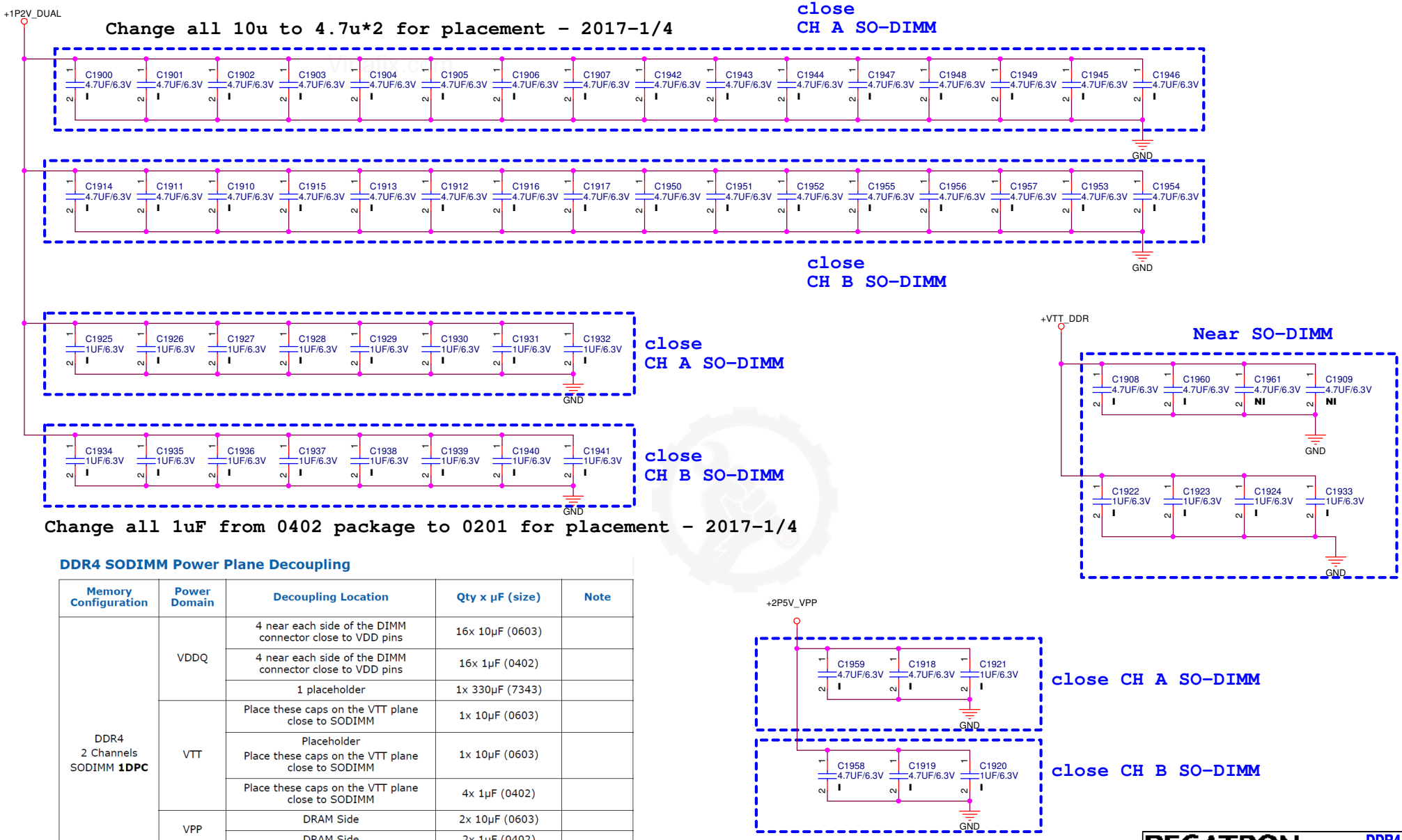


PEGATRON Title : DDR4_SO-DIMM1

Pegatron Corp. Engineer: EE

Size	Project Name	Rev
C	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 18 of 96



Change all 1uF from 0402 package to 0201 for placement - 2017-1/4

DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 2.2µF (0402)	

PEGATRON Title : DDR4_DECOUPLING

Pegatron Corp. Engineer: EE

Size	Project Name	Rev
B	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 19 of 96

U2000A

DMI

USB2.0

PCIE/USB/SATA

USB3.1

PCH-H

LEFT USB3.1(Type-A)

RIGHT USB3.1(Type-A)

RIGHT USB3.1(Type-A)

USB3.1(Type-C)

WEBCAM

Card Reader

Finger Print Reader

M.2 2230 WLAN KEY-E

IO(Type-A)

Right(Type-A)

Right(Type-A)

M.2 PCIE X4 #1

CNL PCH-H Preliminary HSIO Lane Assignments

SKU

HM370

QM370

CM246

SATA SSD4

SATA SSD3

Intel® RST for PCIe Storage port configurable as x2/x4 M.2.

Title	PCH_DMI_PCIE_USB_SATA_1-8
Engineer	EE
Pegatron Corp.	
Size	C
Project Name	Nebula
Rev	A00
Date	Wednesday, March 27, 2019
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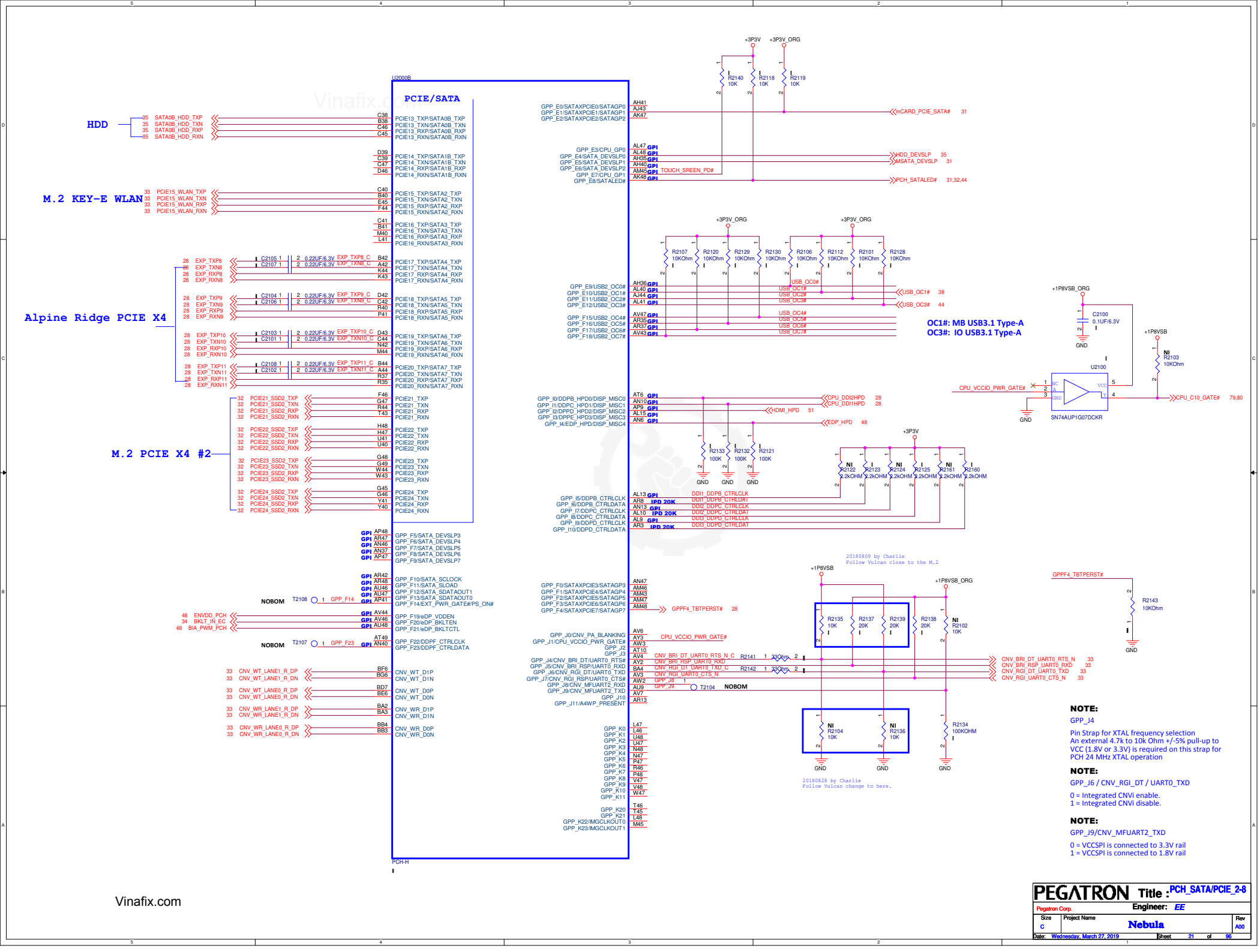


NOTE:

GPP_J4

Pin Strap for XTAL frequency selection
An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

NOTE:

GPP_J6 / CNV_RGI_DT / UART0_TXD

0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

NOTE:

GPP_J9/CNV_MFUART2_TXD

0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

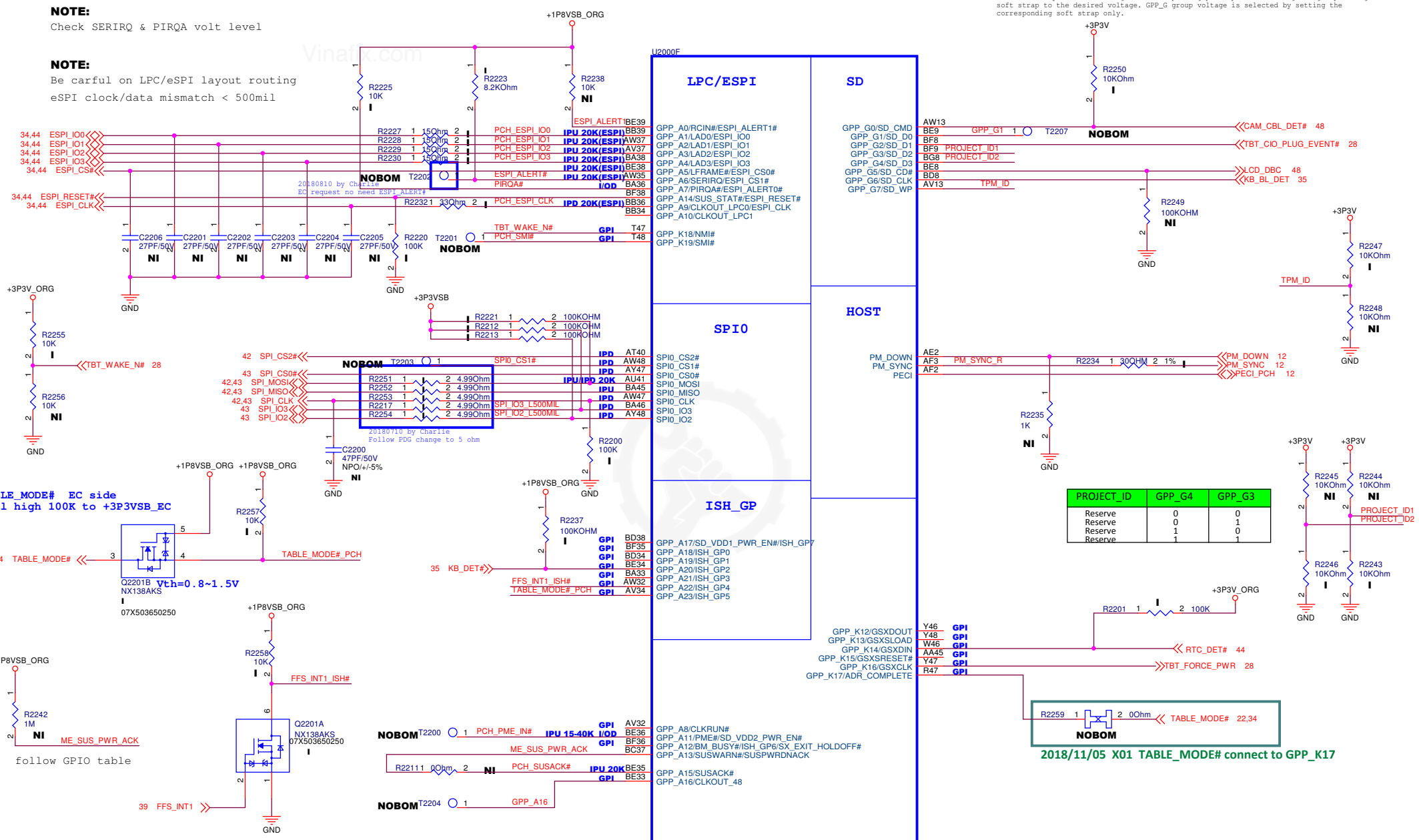
NOTE:
eSPI operates at 1.8V

NOTE:
Check SERIRQ & PIRQA volt level

NOTE:
Be carful on LPC/eSPI layout routing
eSPI clock/data mismatch < 500mil

NOTE:
Check GPP_A0 power well

NOTE: GPP_G 1.8V for GPU
GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltageselection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.

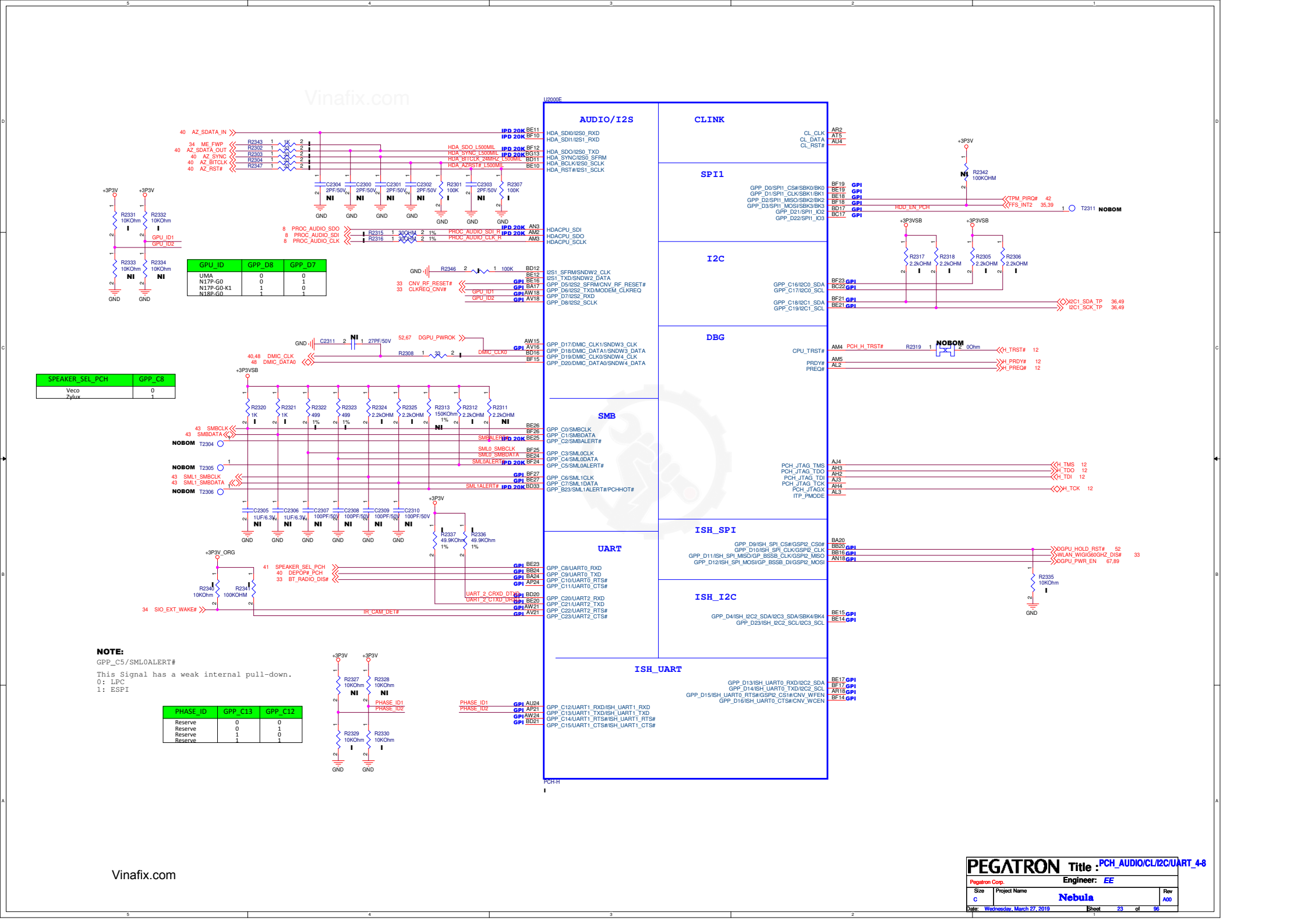


PROJECT_ID	GPP_G4	GPP_G3
Reserve	0	0
Reserve	0	1
Reserve	1	0
Reserve	1	1

2018/11/05 X01 TABLE_MODE# connect to GPP_K17

NOTE:
If Deep Sx is supported, the EC/motherboard controlling logic must change SUSACK# to match SUSWARN# once the EC/motherboard controlling logic has completed the preparations discussed in the description for the SUSWARN# pin.

PEGATRON Title : PCH_ESPI/SPI/FAN/HOST_3-8
Pegatron Corp. Engineer: EE
Size: Custom | Project Name: Nebula | Rev: A00
Date: Wednesday, March 27, 2019 Sheet 22 of 96



GPU_ID	GPP_D8	GPP_D7
UMA	0	0
N17P-G0	0	1
N17P-G0-K1	1	0
N18P-G0	1	1

SPEAKER_SEL_PCH	GPP_C8
Veco	0
Zylux	1

PHASE_ID	GPP_C13	GPP_C12
Reserve	0	0
Reserve	0	1
Reserve	1	0
Reserve	1	1

NOTE:

GPP_C5/SML0ALERT#

This Signal has a weak internal pull-down.
0: LPC
1: ESPI

PEGATRON	Title : PCH_AUDIO/CL/I2C/UART_4-8		
Pegatron Corp.	Engineer: EE		
Size: C	Project Name: Nebula		Rev: A00
Date: Wednesday, March 27, 2019	Sheet 23 of 96		

NOTE:
GPP_B22/GSPI1_MOSI

This Signal has a weak internal pull-down.
Offset 3410h:Bit 10
0: SPI
1: LPC

NOTE:
GSPI0_MOSI/GPP_B18
The signal has a weak internal pull-down.
0 = Disable "No Reboot" mode.
1 = Enable "No Reboot" mode
(PCH will disable the TCO Timer system reboot feature).

NOTE:
GPP_B14 / SPKR

0 = Disable “Top Swap” mode. (Default)
1 = Enable “Top Swap” mode.

NOTE:
GPP_H15/SML3ALERT#
External pull-up is required. Recommend 100K if pulled

NOTE:
GPP_H12/SML2ALERT#

This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.

PEGATRON	Title : PCH SML/I2C/MISC 5-8	
Pegatron Corp.	Engineer: EE	
Size: Custom	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 24 of 96	

NOTE:

CRB: 2.71Kohm

Refer to GND; NOT near switching noise; spacing 3x

Add a GND shield(Width>4 mils)

between XCLK_BIASREF and adjacent IO signals

U2000C

CLOCK

CK_100M_BCK / CK_100M_BCK#

CK_24M_BCK / CK_24M_BCK#

CK_100M_PCIE / CK_100M_PCIE#

CLKOUT_CPUBCLK_P / CLKOUT_CPUBCLK_N

CLKOUT_CPUNSSC_P / CLKOUT_CPUNSSC_N

CLKOUT_CPUPCIBCLK_P / CLKOUT_CPUPCIBCLK_N

CLKOUT_ITPXDP_P / CLKOUT_ITPXDP_N

CLKOUT_PCIE_P0 / CLKOUT_PCIE_N0

CLKOUT_PCIE_P1 / CLKOUT_PCIE_N1

CLKOUT_PCIE_P2 / CLKOUT_PCIE_N2

CLKOUT_PCIE_P3 / CLKOUT_PCIE_N3

CLKOUT_PCIE_P4 / CLKOUT_PCIE_N4

CLKOUT_PCIE_P5 / CLKOUT_PCIE_N5

CLKOUT_PCIE_P6 / CLKOUT_PCIE_N6

CLKOUT_PCIE_P7 / CLKOUT_PCIE_N7

CLKOUT_PCIE_P8 / CLKOUT_PCIE_N8

CLKOUT_PCIE_P9 / CLKOUT_PCIE_N9

CLKOUT_PCIE_P10 / CLKOUT_PCIE_N10

CLKOUT_PCIE_P11 / CLKOUT_PCIE_N11

CLKOUT_PCIE_P12 / CLKOUT_PCIE_N12

CLKOUT_PCIE_P13 / CLKOUT_PCIE_N13

CLKOUT_PCIE_P14 / CLKOUT_PCIE_N14

CLKOUT_PCIE_P15 / CLKOUT_PCIE_N15

CLK_100M_P3_WLAN_R / CLK_100M_N3_WLAN_R — R2514 / R2515 — CLK_100M_P3_WLAN / CLK_100M_N3_WLAN — M2 WLAN

CLK_100M_P5_TBT_R / CLK_100M_N5_TBT_R — R2508 / R2509 — CLK_100M_P5_TBT / CLK_100M_N5_TBT — Alpine Ridge

CLK_100M_P6_SSD1_R / CLK_100M_N6_SSD1_R — R2517 / R2518 — CLK_100M_P6_SSD1 / CLK_100M_N6_SSD1 — M2 SSD1

CLK_100M_P7_GPU_R / CLK_100M_N7_GPU_R — R2510 / R2511 — CLK_100M_P7_GPU / CLK_100M_N7_GPU — GPU

CLK_100M_P8_SSD1_R / CLK_100M_N8_SSD1_R — R2526 / R2527 — CLK_100M_P8_SSD1 / CLK_100M_N8_SSD1 — M2 SSD2

All 0Ohm resistors NOBOM

R2500 60.4Ohm 1% — XCLK_BIASREF — T3 XCLK_BIASREF

R2516 100 1% — PCIE_RCOMPP / PCIE_RCOMPN — A13 / B12 PCIE_RCOMPP / PCIE_RCOMPN

GND

NOBOM T2501 TP_PCH_RSVD_BE2 — AL35 / AN35 TP_1 / TP_2

AH15 RSVD_2; R32 RSVD_7; N32 RSVD_4; U35 RSVD_9; U37 RSVD_10; R15 RSVD_6; R13 RSVD_5; U13 RSVD_8; Y35 RSVD_13; Y36 RSVD_14; Y15 RSVD_12; Y14 RSVD_11

34,44 RTCRST_ON — R2524 100KOHM — Q2500 SSM3K36MFV

CNV_WR_CLKP / CNV_WR_CLKN — BE3 / BD4 — CNV_WR_CLK_R_DP / CNV_WR_CLK_R_DN

CNV_WT_CLKP / CNV_WT_CLKN — BB6 / BC5 — CNV_WT_CLK_R_DP / CNV_WT_CLK_R_DN

44 RTCRST# — BE47 RTCRST#

RTCX2_NO_IO — BA48 RTCX2

RTCX1_NO_IO — BA49 RTCX1

XTAL_IN / XTAL_OUT — U10 XTAL24_IN / U9 XTAL24_OUT — R2525 / R2521 NOBOM — XTAL24_IN_R / XTAL24_OUT_R

USB2_COMP — F4 — R2505 2 11.8 1% — T2502 NOBOM

RSVD_3 / RSVD_1 — BC1 / AH14

CNV_WT_RCOMP — BA1 CNV_WT_RCOMP_C — R2501 150Ohm 1%

SD_RCOMP_1P8 / SD_RCOMP_3P3 — BE5 SD_RCOMP_1P8_C / BE4 SD_RCOMP_3P3_C — R2503 200Ohm 1% / R2504 200Ohm 1%

GPPJ_RCOMP_1P8_1 / GPPJ_RCOMP_1P8_2 / GPPJ_RCOMP_1P8_3 — BD1 / BE1 GPPJ_RCOMP_1P8_C / BE2 — R2506 200Ohm 1%

R2519 10MOhm

R2520 0Ohm NOBOM

Y5_R — X2500 32.768KHZ

C2500 18PF/50V

C2501 18PF/50V

33 CLKIN_XTAL — R2523 0Ohm NOBOM — CLKIN_XTAL_C — R6 CLKIN_XTAL

R2507 10K

TRIGGER_IN / TRIGGER_OUT — AK2 / AK3

14 H_TRIGOUT / 14 H_TRIGIN — R2522 0Ohm NOBOM — H_TRIGIN_H

PCH-H

R2502 200KOhm 1%

X2501 24MHZ

C2502 10PF/50V

C2503 10PF/50V

Table 28-7. 24 MHz Crystal Specifications

Parameter	Values	Units	Max/Min Range
Frequency	24	MHz	
Frequency Tolerance	≤ 100	PPM	
Duty Cycle Variation	+/- 5	%	
Pk to Pk jitter	≤ 150	pS	Includes cycle to cycle and period
Operating Temperature	-40 to 85	°C	
Series Resistance	≤ 30	Ω	
Aging	±3	PPM	

NOTE:

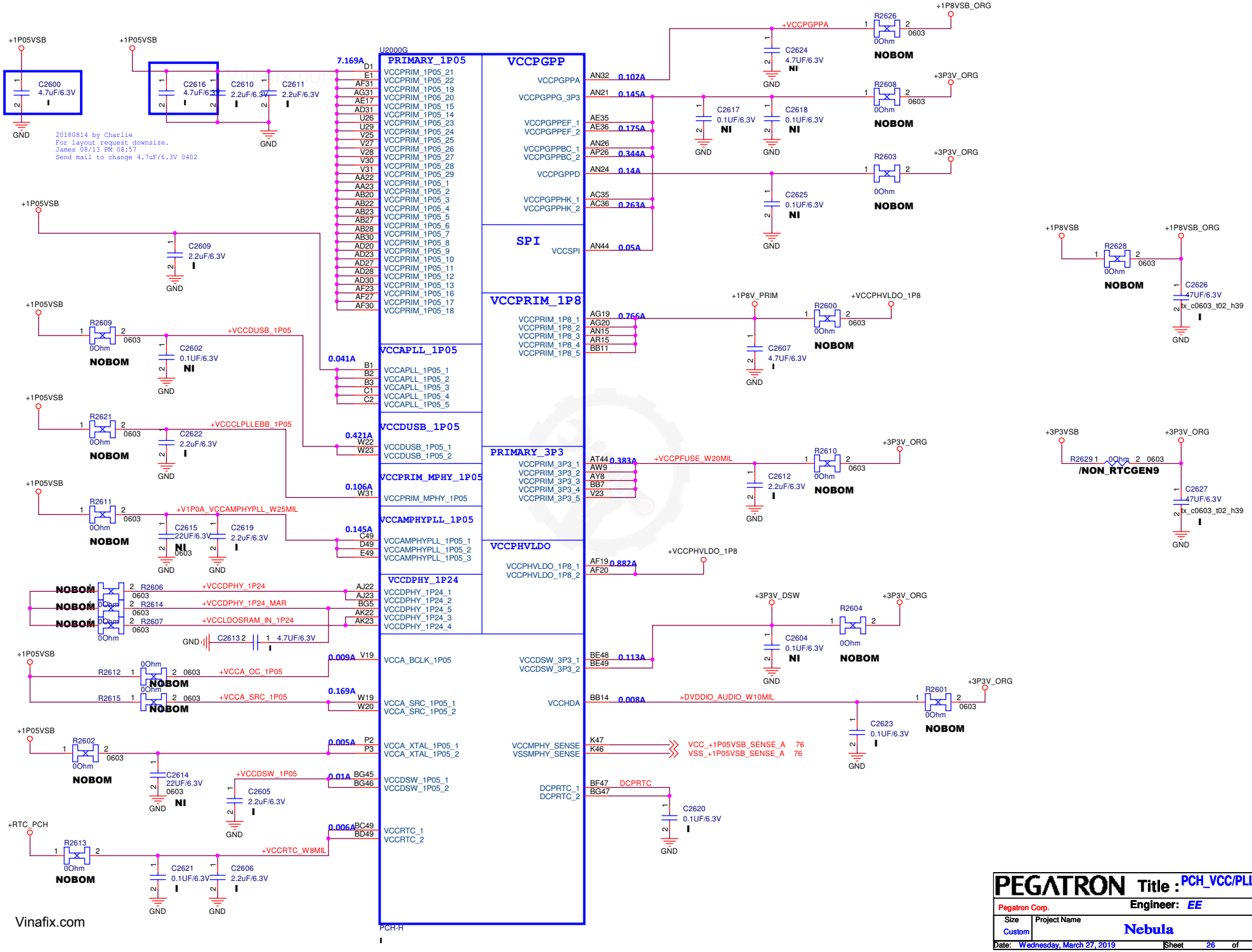
24MHz crystal : ESR 30 OHM

PEGATRON Title : PCH_CLOCK_6-8

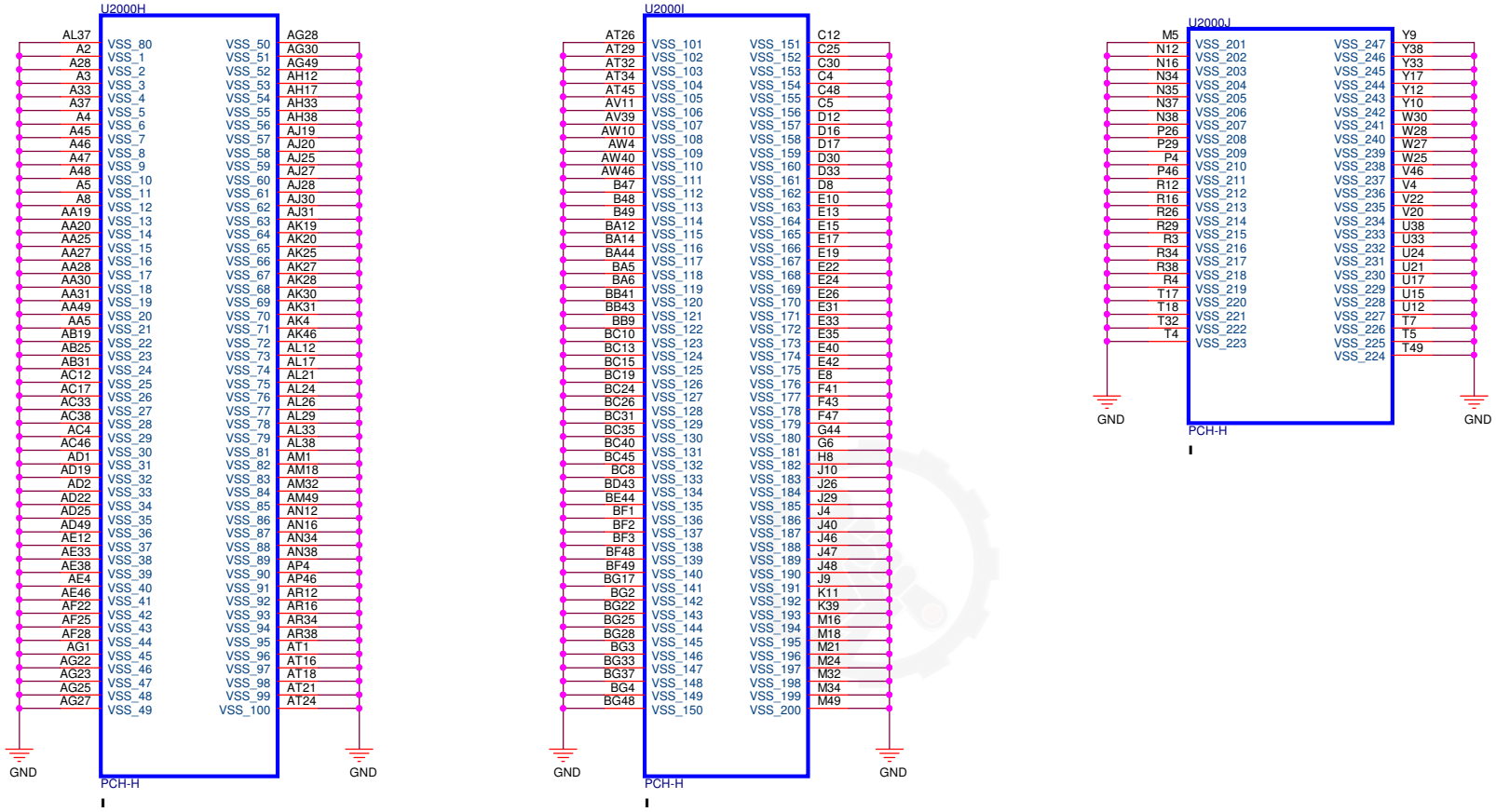
Pegatron Corp. Engineer: EE

Size	Project Name	Rev
C	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 25 of 96



PEGATRON	Title : PCH_VCC/PLL_7-8	
Pegatron Corp.	Engineer: EE	
Size: Custom	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 26 of 96	

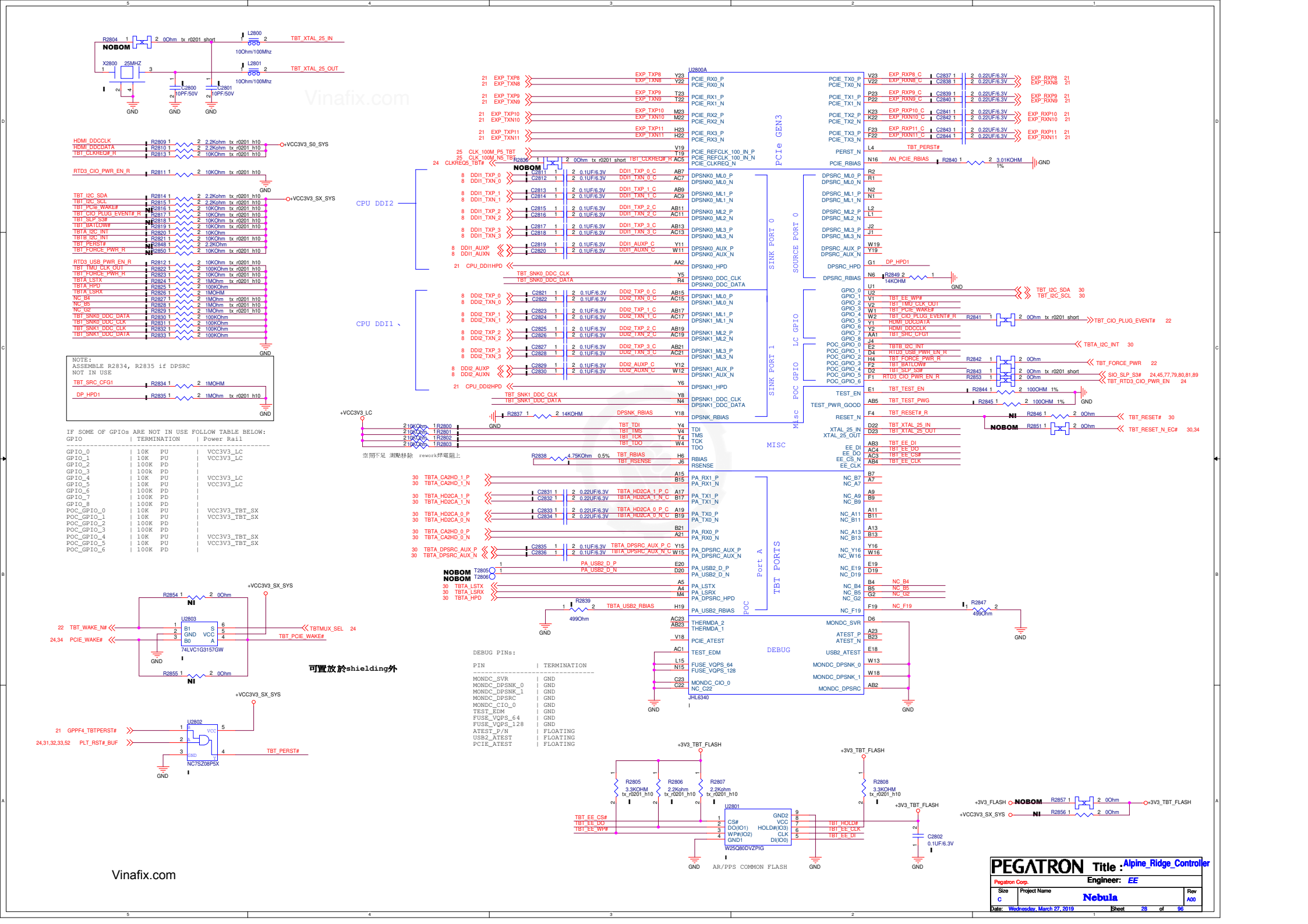


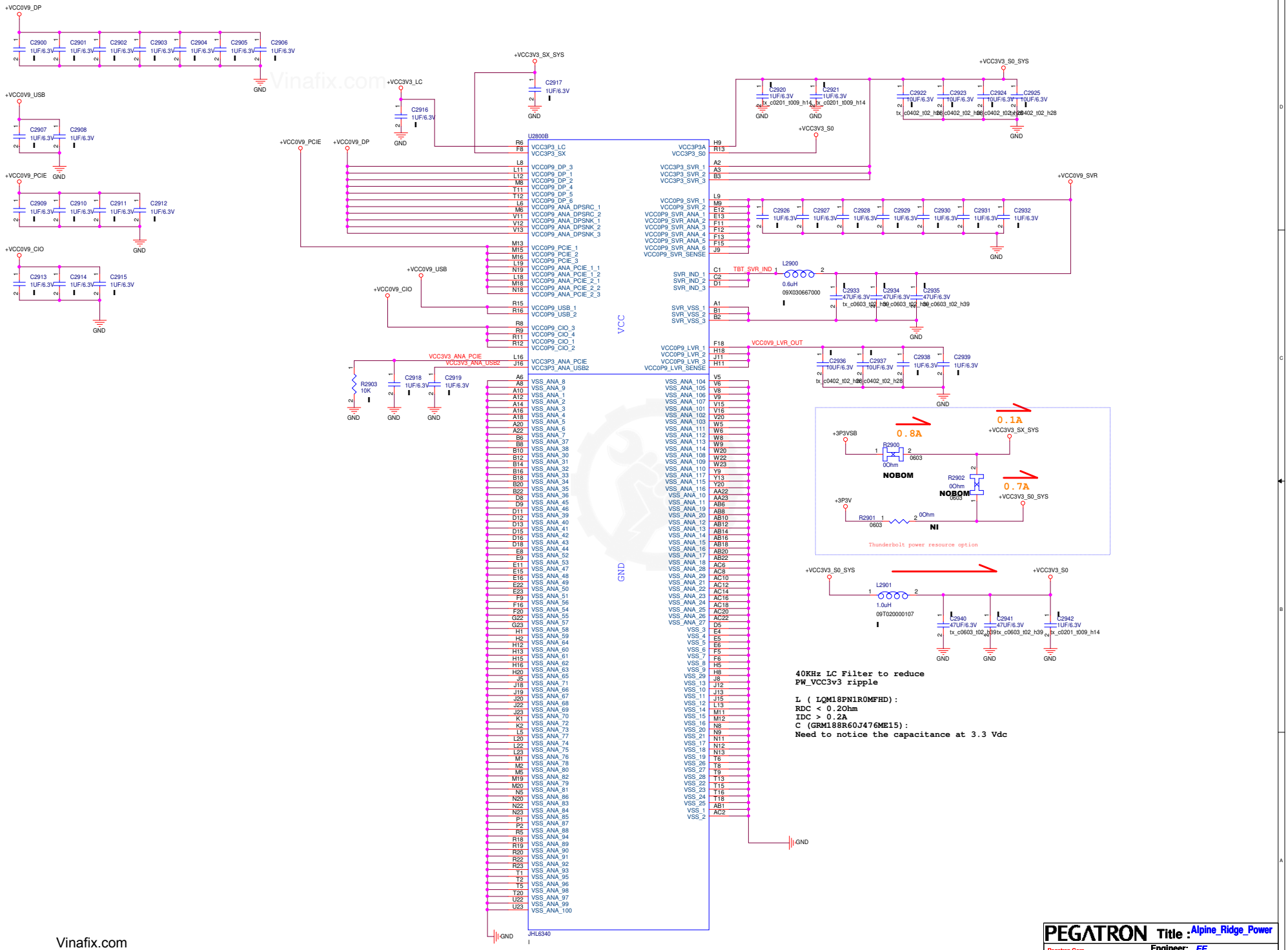
PEGATRON Title : PCH_VSS_8-8

Pegatron Corp. Engineer: EE

Size	Project Name	Rev
B	Nebula	A00

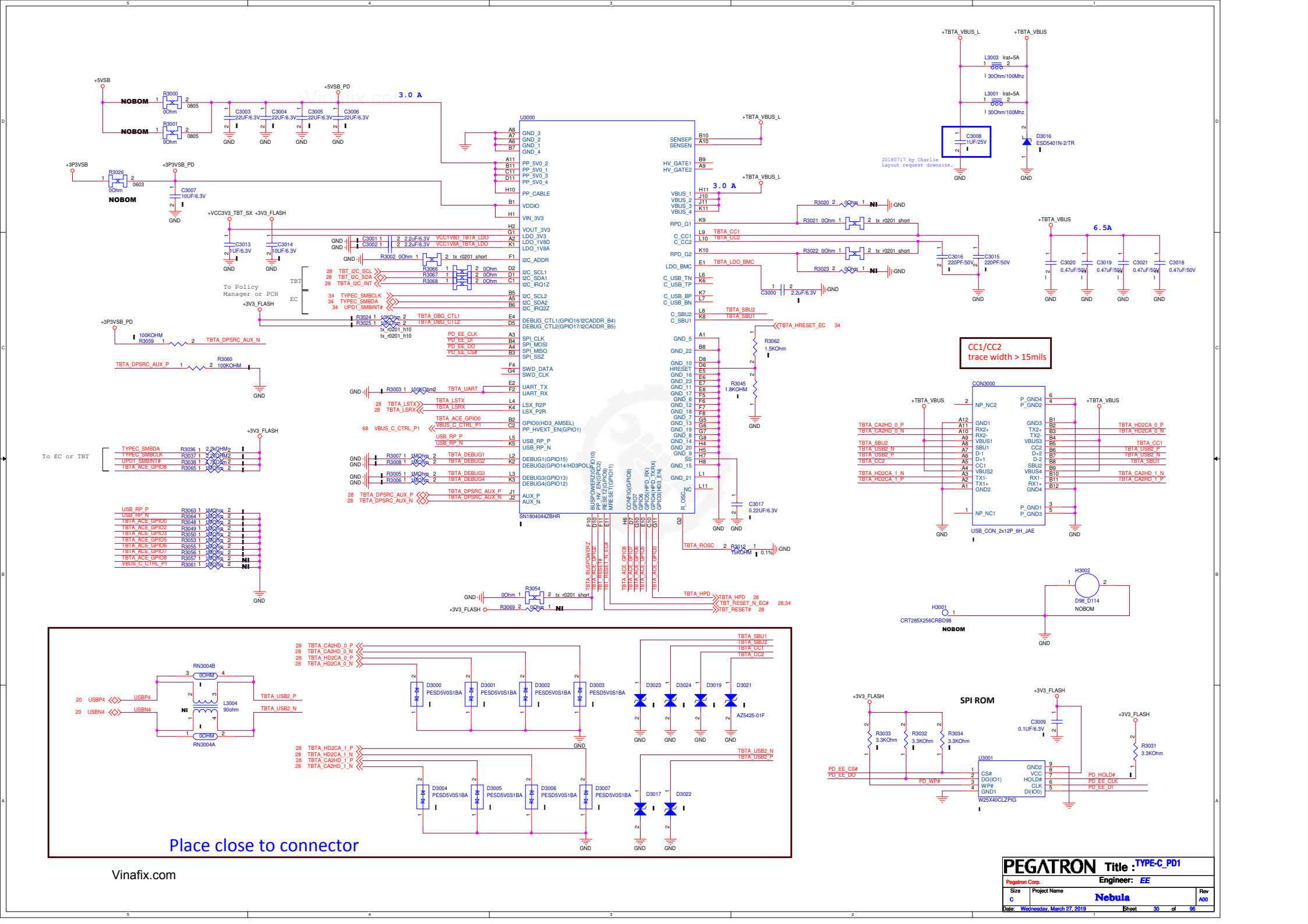
Date: Wednesday, March 27, 2019 Sheet 27 of 96


U2800A
PCIE_RX0_P
PCIE_RX0_N
PCIE_RX1_P
PCIE_RX1_N
PCIE_RX2_P
PCIE_RX2_N
PCIE_RX3_P
PCIE_RX3_N
PCIE_REFCLK_100_IN_P
PCIE_REFCLK_100_IN_N
PCIE_CLKREQ_N
PCIE_TX0_P
PCIE_TX0_N
PCIE_TX1_P
PCIE_TX1_N
PCIE_TX2_P
PCIE_TX2_N
PCIE_TX3_P
PCIE_TX3_N
PERST_N
PCIE_RBIAS
PCIe GEN3
DPSNK0_ML0_P
DPSNK0_ML0_N
DPSNK0_ML1_P
DPSNK0_ML1_N
DPSNK0_ML2_P
DPSNK0_ML2_N
DPSNK0_ML3_P
DPSNK0_ML3_N
DPSNK0_AUX_P
DPSNK0_AUX_N
DPSNK0_HPD
DPSNK0_DDC_CLK
DPSNK0_DDC_DATA
SINK PORT 0
DPSRC_ML0_P
DPSRC_ML0_N
DPSRC_ML1_P
DPSRC_ML1_N
DPSRC_ML2_P
DPSRC_ML2_N
DPSRC_ML3_P
DPSRC_ML3_N
DPSRC_AUX_P
DPSRC_AUX_N
DPSRC_HPD
DPSRC_RBIAS
SOURCE PORT 0
DPSNK1_ML0_P
DPSNK1_ML0_N
DPSNK1_ML1_P
DPSNK1_ML1_N
DPSNK1_ML2_P
DPSNK1_ML2_N
DPSNK1_ML3_P
DPSNK1_ML3_N
DPSNK1_AUX_P
DPSNK1_AUX_N
DPSNK1_HPD
DPSNK1_DDC_CLK
DPSNK1_DDC_DATA
DPSNK_RBIAS
SINK PORT 1
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
LC GPIO
POC_GPIO_0
POC_GPIO_1
POC_GPIO_2
POC_GPIO_3
POC_GPIO_4
POC_GPIO_5
POC_GPIO_6
POC GPIO
TEST_EN
TEST_PWR_GOOD
RESET_N
XTAL_25_IN
XTAL_25_OUT
EE_DI
EE_DO
EE_CS_N
EE_CLK
Misc
TDI
TMS
TCK
TDO
RBIAS
RSENSE
MISC
PA_RX1_P
PA_RX1_N
PA_TX1_P
PA_TX1_N
PA_TX0_P
PA_TX0_N
PA_RX0_P
PA_RX0_N
PA_DPSRC_AUX_P
PA_DPSRC_AUX_N
PA_USB2_D_P
PA_USB2_D_N
PA_LSTX
PA_LSRX
PA_DPSRC_HPD
PA_USB2_RBIAS
Port A
NC_B7
NC_A7
NC_A9
NC_B9
NC_A11
NC_B11
NC_A13
NC_B13
NC_Y16
NC_W16
NC_E19
NC_D19
NC_B4
NC_B5
NC_G2
NC_F19
POC
TBT PORTS
THERMDA_2
THERMDA_1
PCIE_ATEST
TEST_EDM
FUSE_VQPS_64
FUSE_VQPS_128
MONDC_CIO_0
NC_C22
MONDC_SVR
ATEST_P
ATEST_N
USB2_ATEST
MONDC_DPSNK_0
MONDC_DPSNK_1
MONDC_DPSRC
DEBUG
JHL6340
CPU DDI2
CPU DDI1
DDI1_TXP_0
DDI1_TXN_0
DDI1_TXP_1
DDI1_TXN_1
DDI1_TXP_2
DDI1_TXN_2
DDI1_TXP_3
DDI1_TXN_3
DDI1_AUXP
DDI1_AUXN
CPU_DDI1HPD
DDI2_TXP_0
DDI2_TXN_0
DDI2_TXP_1
DDI2_TXN_1
DDI2_TXP_2
DDI2_TXN_2
DDI2_TXP_3
DDI2_TXN_3
DDI2_AUXP
DDI2_AUXN
CPU_DDI2HPD
EXP_TXP8
EXP_TXN8
EXP_TXP9
EXP_TXN9
EXP_TXP10
EXP_TXN10
EXP_TXP11
EXP_TXN11
EXP_RXP8_C
EXP_RXN8_C
EXP_RXP9_C
EXP_RXN9_C
EXP_RXP10_C
EXP_RXN10_C
EXP_RXP11_C
EXP_RXN11_C
EXP_RXP8
EXP_RXN8
EXP_RXP9
EXP_RXN9
EXP_RXP10
EXP_RXN10
EXP_RXP11
EXP_RXN11
CLK_100M_P5_TBT
CLK_100M_N5_TBT
CLKREQ5_TBT#
TBT_CLKREQ#_H
TBT_PERST#
AN_PCIE_RBIAS
DP_HPD1
TBT_SNK0_DDC_CLK
TBT_SNK0_DDC_DATA
TBT_SNK1_DDC_CLK
TBT_SNK1_DDC_DATA
TBT_TDI
TBT_TMS
TBT_TCK
TBT_TDO
TBT_RBIAS
TBT_RSENSE
TBTA_CA2HD_1_P
TBTA_CA2HD_1_N
TBTA_HD2CA_1_P
TBTA_HD2CA_1_N
TBTA_HD2CA_0_P
TBTA_HD2CA_0_N
TBTA_CA2HD_0_P
TBTA_CA2HD_0_N
TBTA_DPSRC_AUX_P
TBTA_DPSRC_AUX_N
TBTA_LSTX
TBTA_LSRX
TBTA_HPD
TBT_USB2_RBIAS
TBT_I2C_SDA
TBT_I2C_SCL
TBT_EE_WP#
TBT_IMU_CLK_OUT
TBT_PCIE_WAKE#
TBT_CIO_PLUG_EVENT#_R
TBT_SLP_S3#
TBT_BATLOW#
TBT_SRC_CFG1
TBT_FORCE_PWR_R
TBT_RESET#_R
TBT_XTAL_25_IN
TBT_XTAL_25_OUT
TBT_EE_DI
TBT_EE_DO
TBT_EE_CS#
TBT_EE_CLK
TBTA_I2C_INT
TBTB_I2C_INT
RTD3_USB_PWR_EN_R
RTD3_CIO_PWR_EN_R
TBT_FORCE_PWR
SIO_SLP_S3#
TBT_RTD3_CIO_PWR_EN
TBT_CIO_PLUG_EVENT#
TBT_RESET#
TBT_RESET_N_EC#
TBT_TEST_EN
TBT_TEST_PWG
TBT_RESET#_R
TBT_SRC_CFG1
DP_HPD1
NC_B4
NC_B5
NC_G2
NC_F19
+VCC3V3_LC
+VCC3V3_S0_SYS
+VCC3V3_SX_SYS
+3V3_TBT_FLASH
GND
NOBOM
NI
空間不足 測點移除 rework焊電阻上
NOTE:
ASSEMBLE R2834, R2835 if DPSRC
NOT IN USE
IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:
GPIO | TERMINATION | Power Rail
GPIO_0 | 10K PU | VCC3V3_LC
GPIO_1 | 10K PU | VCC3V3_LC
GPIO_2 | 100K PD |
GPIO_3 | 100K PD |
GPIO_4 | 10K PU | VCC3V3_LC
GPIO_5 | 10K PU | VCC3V3_LC
GPIO_6 | 100K PD |
GPIO_7 | 100K PD |
GPIO_8 | 100K PD |
POC_GPIO_0 | 10K PU | VCC3V3_TBT_SX
POC_GPIO_1 | 10K PU | VCC3V3_TBT_SX
POC_GPIO_2 | 100K PD |
POC_GPIO_3 | 100K PD |
POC_GPIO_4 | 10K PU | VCC3V3_TBT_SX
POC_GPIO_5 | 10K PU | VCC3V3_TBT_SX
POC_GPIO_6 | 100K PD |
DEBUG PINs:
PIN | TERMINATION
MONDC_SVR | GND
MONDC_DPSNK_0 | GND
MONDC_DPSNK_1 | GND
MONDC_DPSRC | GND
MONDC_CIO_0 | GND
TEST_EDM | GND
FUSE_VQPS_64 | GND
FUSE_VQPS_128 | GND
ATEST_P/N | FLOATING
USB2_ATEST | FLOATING
PCIE_ATEST | FLOATING
R2804 NOBOM 0Ohm tx r0201 short
L2800 10Ohm/100Mhz
L2801 10Ohm/100Mhz
X2800 25MHZ
C2800 10PF/50V
C2801 10PF/50V
TBT_XTAL_25_IN
TBT_XTAL_25_OUT
HDMI_DDCCLK
HDMI_DDCDATA
TBT_CLKREQ#_R
RTD3_CIO_PWR_EN_R
TBT_I2C_SDA
TBT_I2C_SCL
TBT_PCIE_WAKE#
TBT_CIO_PLUG_EVENT#_R
TBT_SLP_S3#
TBT_BATLOW#
TBTA_I2C_INT
TBTB_I2C_INT
TBT_PERST#
TBT_FORCE_PWR_R
RTD3_USB_PWR_EN_R
TBT_IMU_CLK_OUT
TBT_FORCE_PWR_R
TBTA_LSTX
TBTA_HPD
NC_B4
NC_B5
NC_G2
TBT_SNK0_DDC_DATA
TBT_SNK0_DDC_CLK
TBT_SNK1_DDC_CLK
TBT_SNK1_DDC_DATA
TBT_SRC_CFG1
DP_HPD1
R2837 14KOHM
R2838 4.75KOhm 0.5%
R2839 499Ohm
R2847 499Ohm
R2849 14KOHM
R2840 3.01KOHM 1%
R2841 0Ohm tx r0201 short
R2842 0Ohm
R2843 0Ohm tx r0201 short
R2853 0Ohm
R2844 100OHM 1%
R2845 100OHM 1%
R2846 0Ohm
R2851 0Ohm
R2854 0Ohm
R2855 0Ohm
U2803 74LVC1G3157GW
TBTMUX_SEL
TBT_PCIE_WAKE#
U2802 NC7SZ08P5X
GPPF4_TBTPERST#
PLT_RST#_BUF
R2805 3.3KOHM tx_r0201_h10
R2806 2.2Kohm tx_r0201_h10
R2807 2.2Kohm tx_r0201_h10
R2808 3.3KOHM tx_r0201_h10
U2801 W25Q80DVZPIG
TBT_EE_CS#
TBT_EE_DO
TBT_EE_WP#
TBT_HOLD#
TBT_EE_CLK
TBT_EE_DI
C2802 0.1UF/6.3V
AR/PPS COMMON FLASH
R2857 0Ohm
R2856 0Ohm
可置放於shielding外
Vinafix.com
PEGATRON
Title : Alpine_Ridge_Controller
Engineer: EE
Pegatron Corp.
Size C
Project Name Nebula
Rev A00
Date: Wednesday, March 27, 2019
Sheet 28 of 96



Vinafix.com

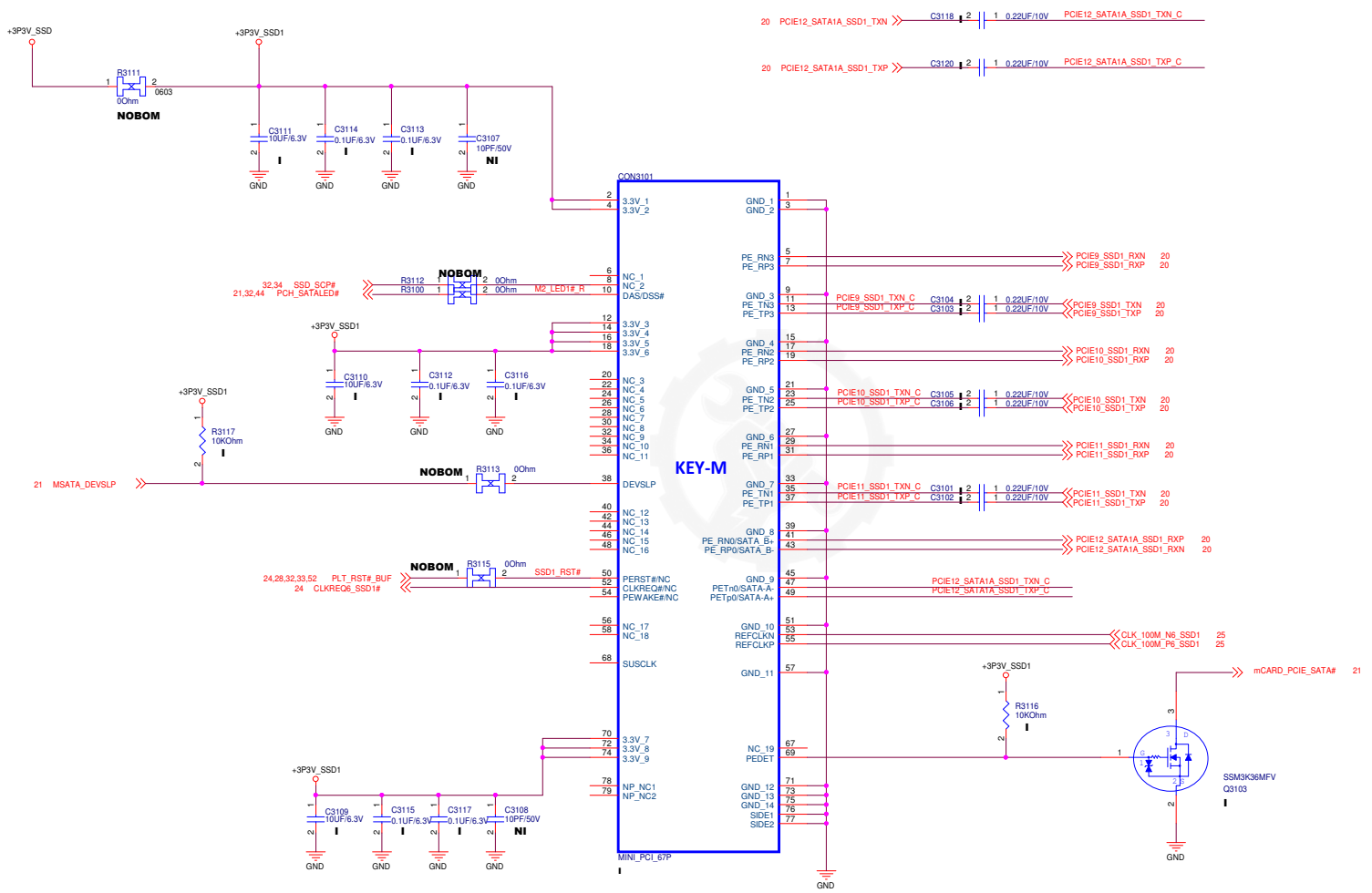
PEGATRON Corp.	Title : Alpine_Ridge_Power	
	Engineer: EE	
Size: C	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 29 of 96	



PEGATRON	Title : TYPE-C_PD1		
Pegatron Corp.	Engineer: EE		
Size: C	Project Name: Nebula		Rev: A00
Date: Wednesday, March 27, 2019	Sheet 30 of 96		

M.2 KEY-M SSD #1(SATA+PCIE X4)

PCIE/SATA SSD by BOM change 0.1uF/0.22uF



PEGATRON Corp.

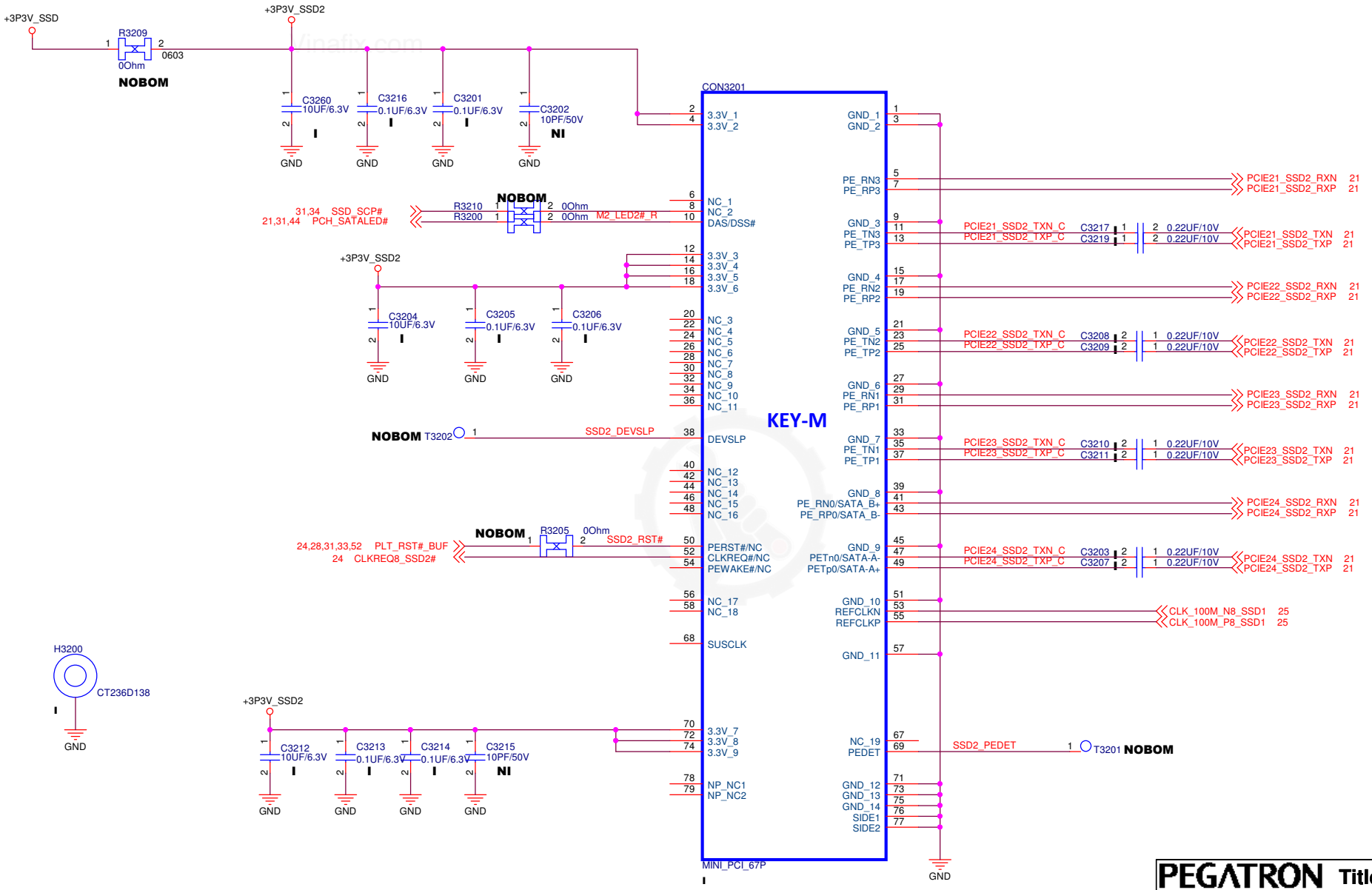
Title : M.2_PCIEX4_#1

Engineer: EE

Size	Project Name	Rev
C	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 31 of 96

M.2 KEY-M SSD #1(PCIE X4)



PEGATRON Title : M.2_PCIEX4_#2

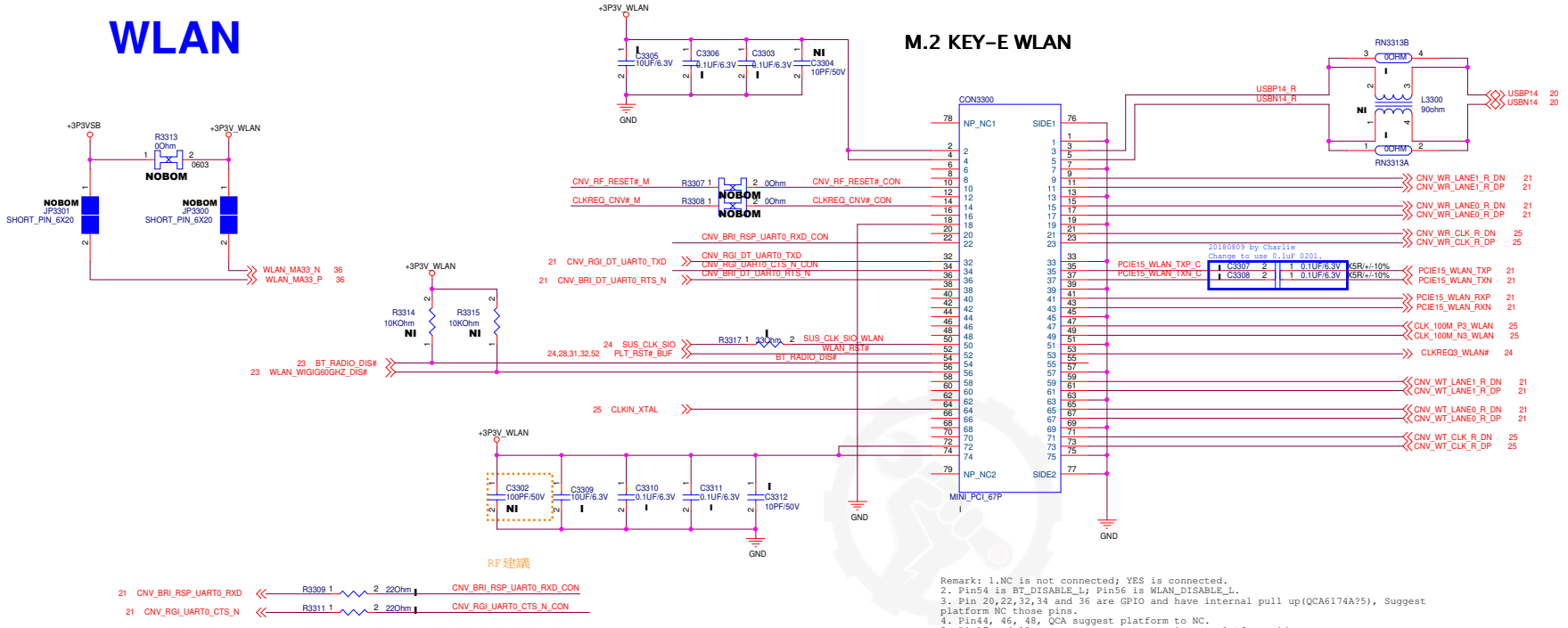
Pegatron Corp. Engineer: EE

Size	Project Name	Rev
B	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 32 of 96

WLAN

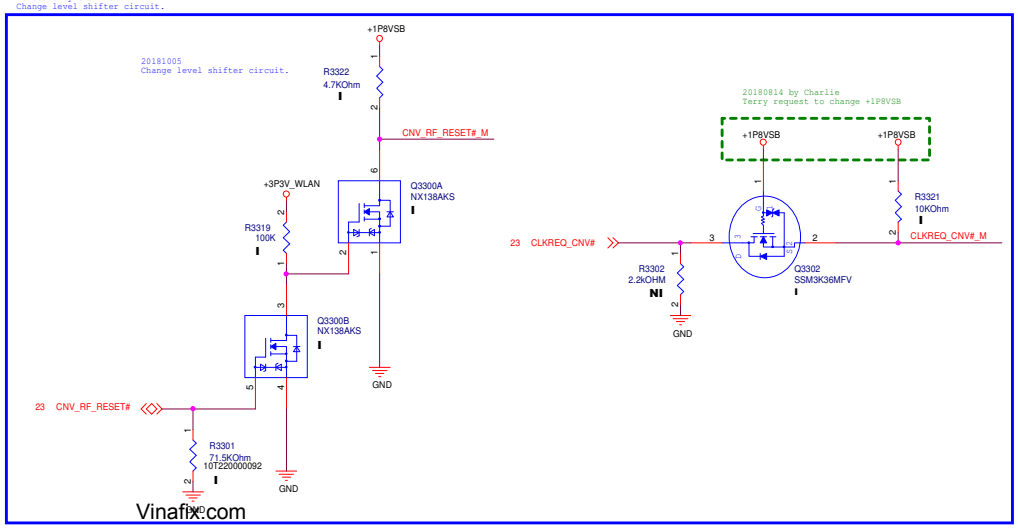
M.2 KEY-E WLAN



Remark: 1.NC is not connected; YES is connected.
2. Pin54 is BT_DISABLE_L; Pin56 is WLAN_DISABLE_L.
3. Pin 20,22,32,34 and 36 are GPIO and have internal pull up(QCA6174A?5), Suggest platform NC those pins.
4. Pin44, 46, 48, QCA suggest platform to NC.
5. Pin17 and 19 suggest reserve test point at platform side.

H3300 CT276B181D165 GND

20180809 by Charlie
Add level shifter circuit.
20180810 by Charlie
Change level shifter circuit.



PEGATRON Title : M.2_WLAN_KEY-E
Pegatron Corp. Engineer: EE
Size C | Project Name Nebula | Rev A00
Date: Wednesday, March 27, 2019 | Sheet 33 of 96

Pull Up

EC Power

eSPI Strap

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note:
If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel.
If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

Imax:12.5mA

debug test point placement together bottom side

HOST_DEBUG_TX	1	T3404	TPC26T_50	NOBOM
ICSP_CLK	1	T3406	TPC26T_50	NOBOM
ICSP_DAT	1	T3405	TPC26T_50	NOBOM
ICSP_CLR	1	T3407	TPC26T_50	NOBOM
+3P3VSB_EC	1	T3409	TPC26T_50	NOBOM

Adapter power monitor to EC ADC pin — Need very close to EC

Battery power monitor to EC ADC pin

U3400 正確料號為 0638-008K0DE
EMBEDDED CONTR. MEC1418-NU-D0

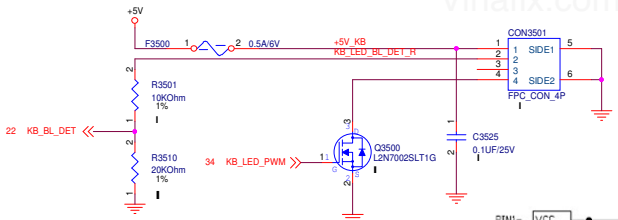
BOARD_ID(GPIO155)	PULL-LOW RES	PULL-HIGH RES	VOLTAGE
X00	100.0K	10.0K	3.000
X01	100.0K	17.8K	2.801
X02	100.0K	27.0K	2.598
X03(reserve)	100.0K	37.4K	2.402
A00	100.0K	49.9K	2.201
A01	100.0K	64.9K	2.001
A02	100.0K	82.5K	1.809
A03	100.0K	107K	1.594
Reserve	100.0K	154K	1.299
Reserve	100.0K	200K	1.100
Reserve	100.0K	TBD	0.900
Reserve	100.0K	TBD	0.700
Reserve	100.0K	TBD	0.500
Reserve	100.0K	TBD	0.300

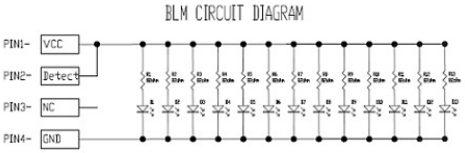
MODEL_ID(GPIO153)	PULL-LOW RES	PULL-HIGH RES	VOLTAGE
H62 + UMA	100.0K	10.0K	3.000
H82 + UMA	100.0K	17.8K	2.801
H62 + N17P-G0	100.0K	27.0K	2.598
H82 + N17P-G0	100.0K	37.4K	2.402
H62 + N17P-G0-K1	100.0K	49.9K	2.201
H82 + N17P-G0-K1	100.0K	64.9K	2.001
H62 + N18P-G0	100.0K	82.5K	1.809
H82 + N18P-G0	100.0K	107K	1.594
Reserve	100.0K	154K	1.299
Reserve	100.0K	200K	1.100
Reserve	100.0K	TBD	0.900
Reserve	100.0K	TBD	0.700
Reserve	100.0K	TBD	0.500
Reserve	100.0K	TBD	0.300

Vinafix.com

PEGATRON	Title :	EC_MEC1418	
Pegatron Corp.	Engineer:	EE	
Size: Custom	Project Name: Nebula		Rev: A00
Date: Wednesday, March 27, 2019	Sheet 34 of 98		

KB BL Conn



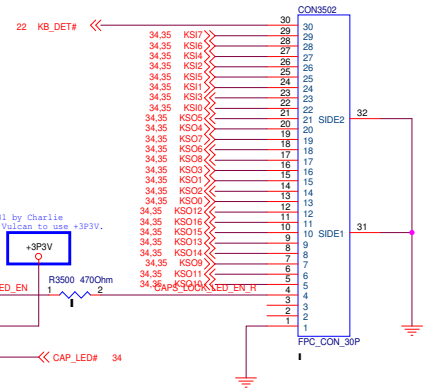


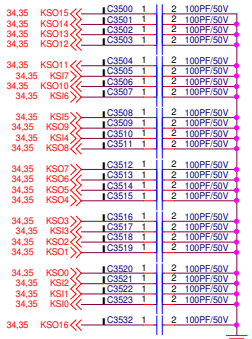
VCC : +5V
LED Vf : 2.7~3.1V

	Min(LED Vf : 3.1V)	Max(LED Vf : 2.7V)
Power consumption	271.09 mA	401.1mA

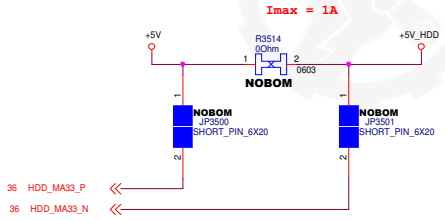
NOTES:Backlit Golden Sample , LED Bin
Luminous Intensity Bin : S4
Chromaticity Coordinates of Bin Code: A4

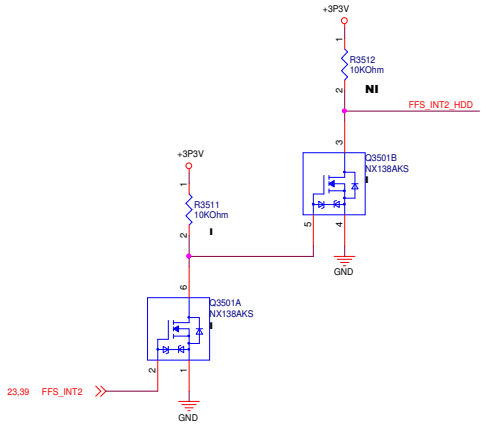
KB Conn

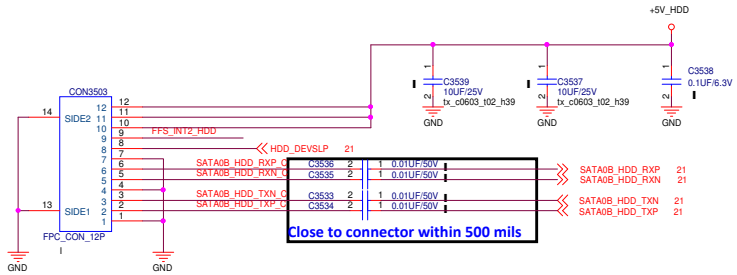




SATA HDD

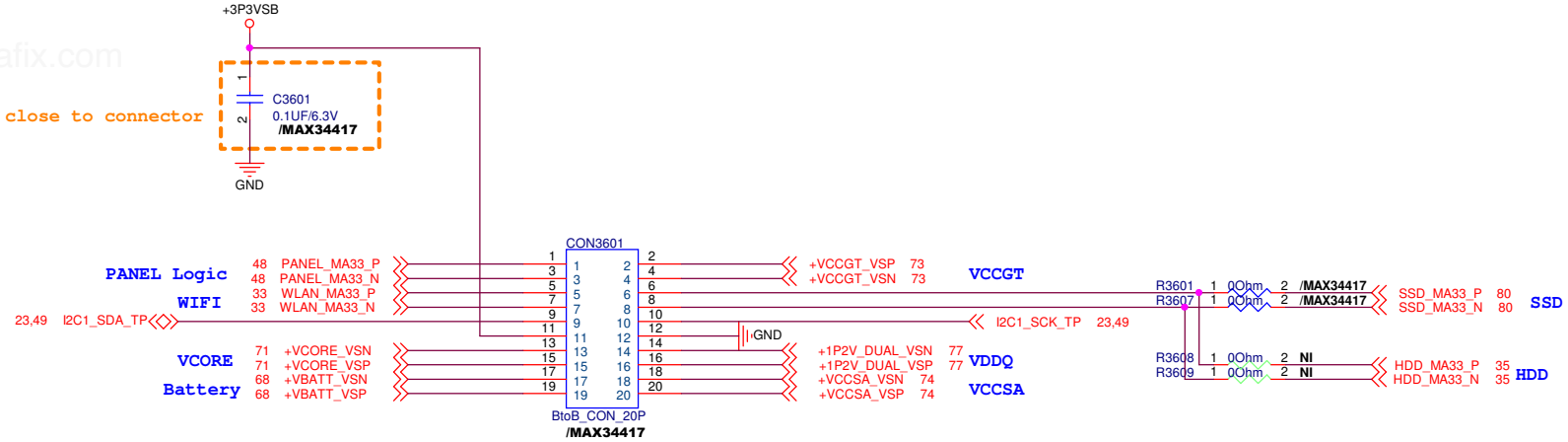






PEGATRON	Title :	SATA_HDD_KeyBoard
Pegatron Corp.	Engineer:	EE
Size: C	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 35 of 96	

POWER SENSE MAX34417



	PIN	Sense resistor
VccGT	P1+/-	PR7307 (10m ohm) PR7308 (10m ohm)
SSD	P2+/-	R4852 (10m ohm)
HDD(SATA)		R3126 (10m ohm)
WIFI	P3+/-	R3313 (10m ohm)
Panel logic	P4+/-	R3109 (10m ohm)
Battery	P5+/-	R6811 (5m ohm)
Vcore	P6+/-	PR7100 (10m ohm) PR7101 (10m ohm)
VDDQ	P7+/-	PR7700 (10m ohm)
VccSA	P8+/-	PR7407 (10m ohm)

2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19

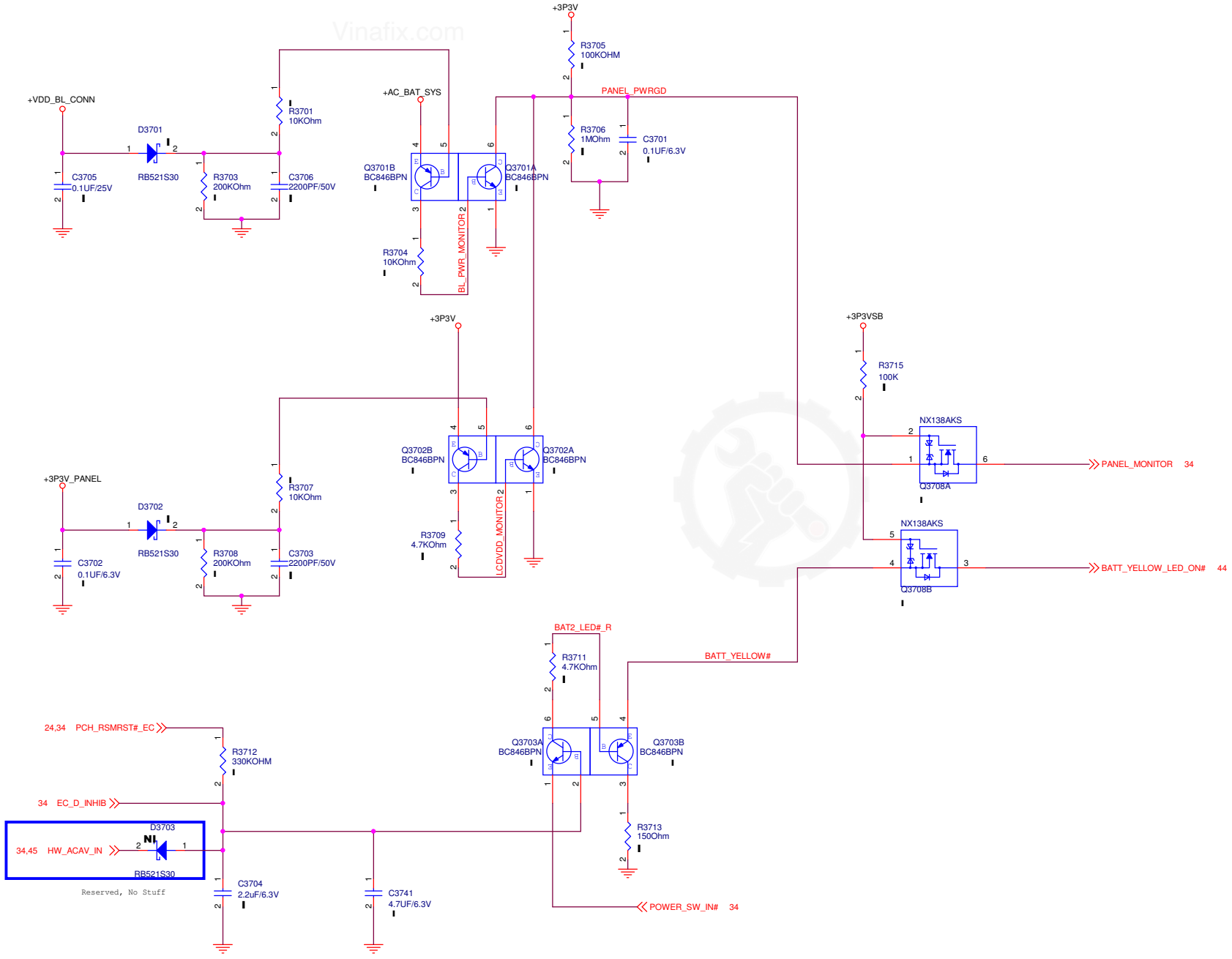
PEGATRON Title : POWER_SENSE_MAX34417

Pegatron Corp. Engineer: EE

Size	Project Name	Rev
B	Nebula	A00

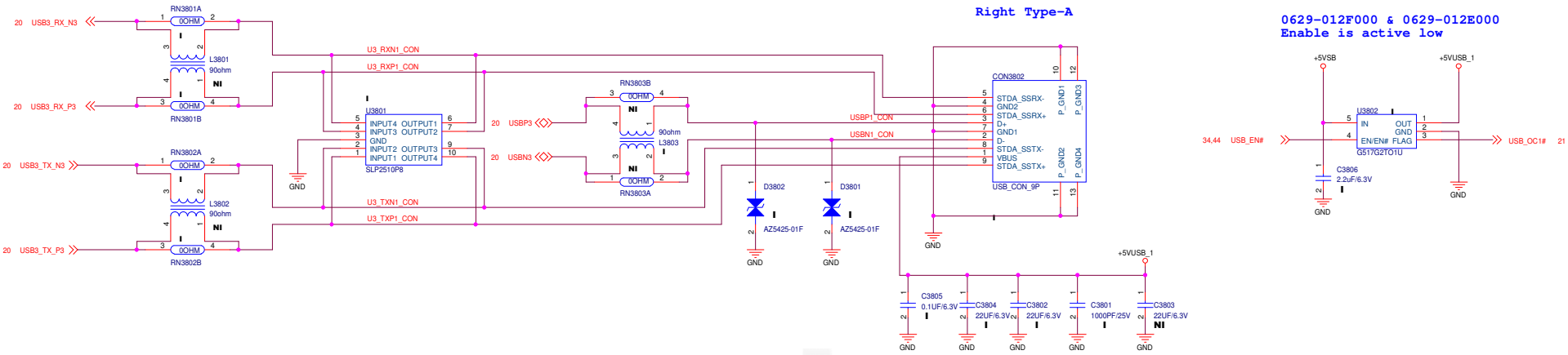
Date: Wednesday, March 27, 2019 Sheet 36 of 96

LCD BIST

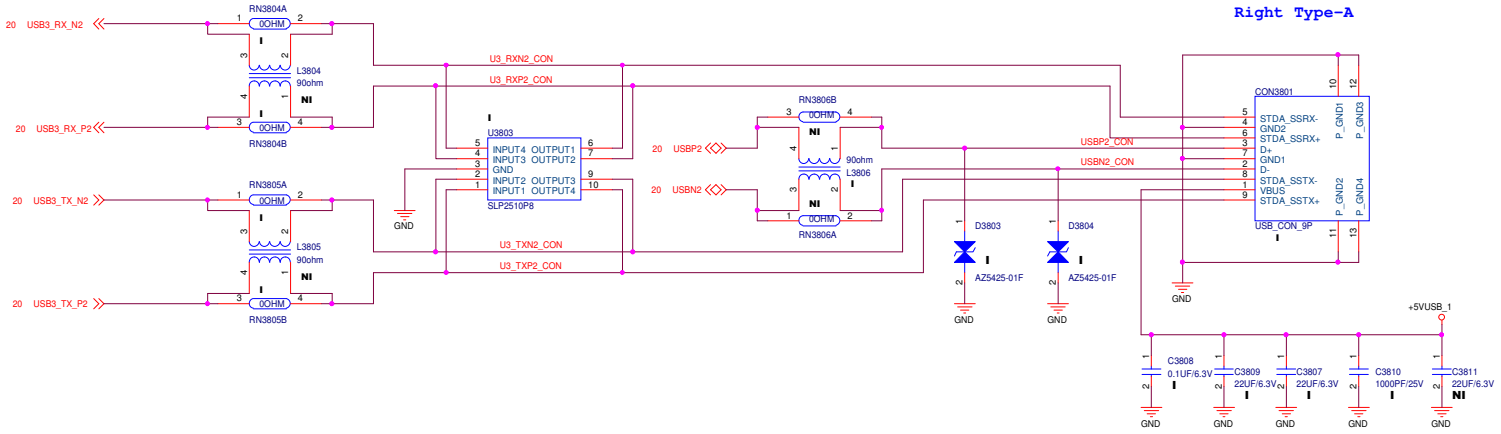


PEGATRON Pegatron Corp.	Title : LCD_BIST/MB_BIST Engineer: EE	
Size: Custom	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 37 of 96	

USB3.1 TypeA Port1 & Reapeater (Right side)

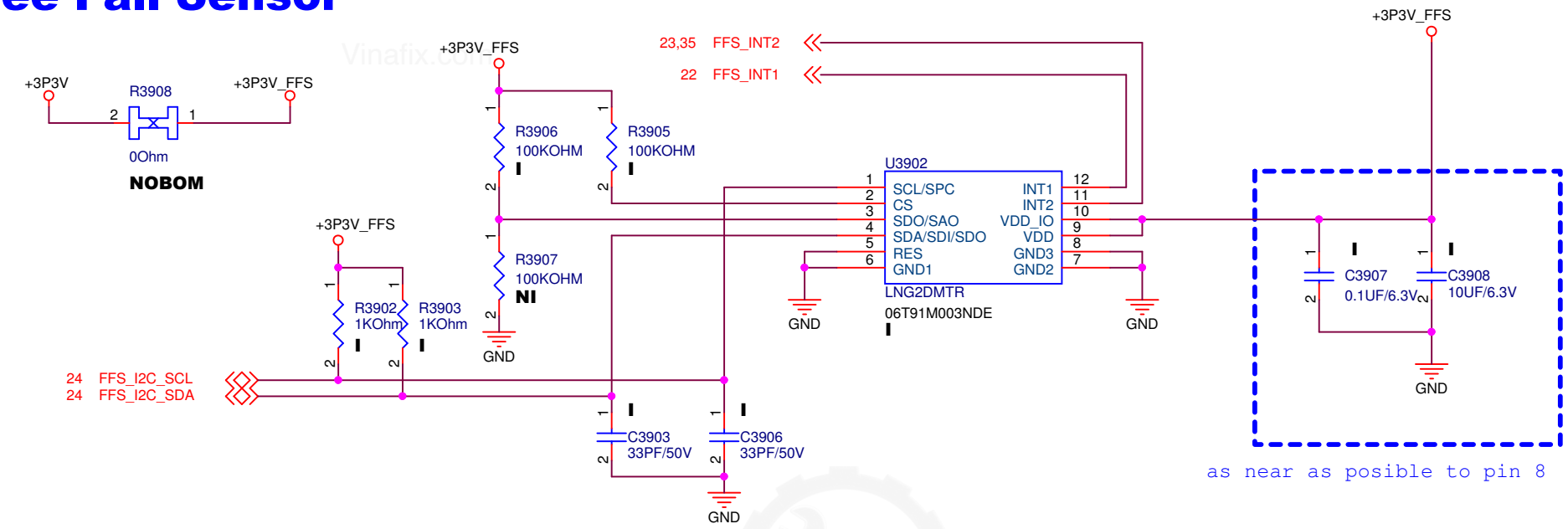


USB3.1 TypeA Port2 & Reapeater (Right side)

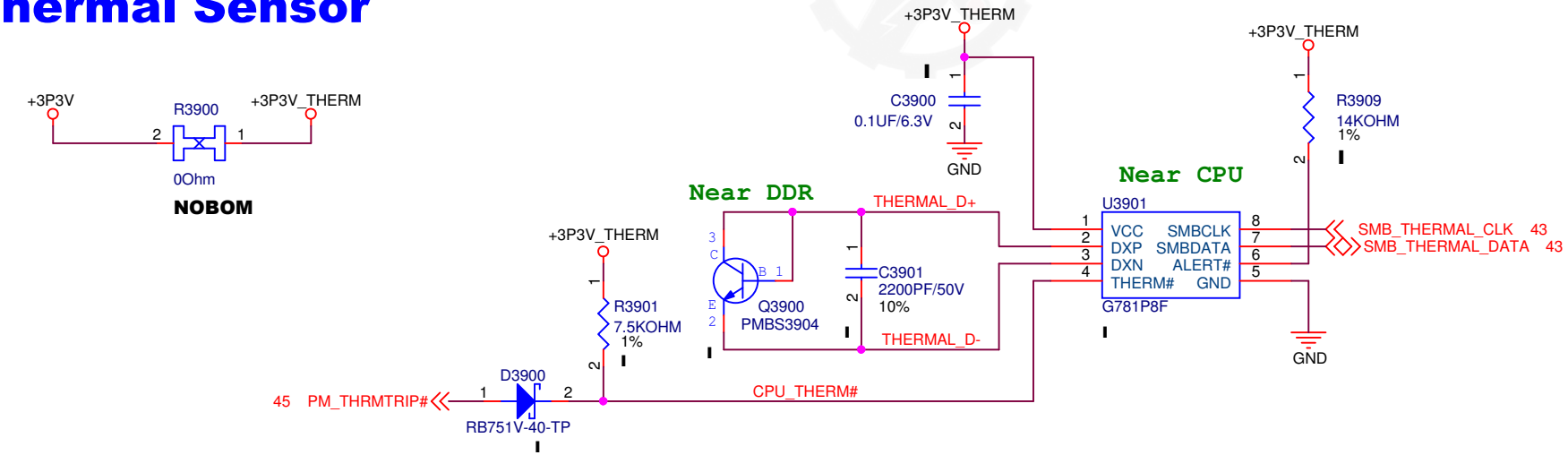


PEGATRON Corp.	Title : USB_CONN		
	Engineer: EE		
Size: C	Project Name: Nebula		Rev: A00
Date: Wednesday, March 27, 2019	Sheet 38 of 96		

Free Fall Sensor



Thermal Sensor



TEMPERATURE (℃)		T_CRIT				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

PEGATRON Title : SENSOR

Pegatron Corp. Engineer: EE

Size	Project Name	Rev
Custom	Nebula	A00

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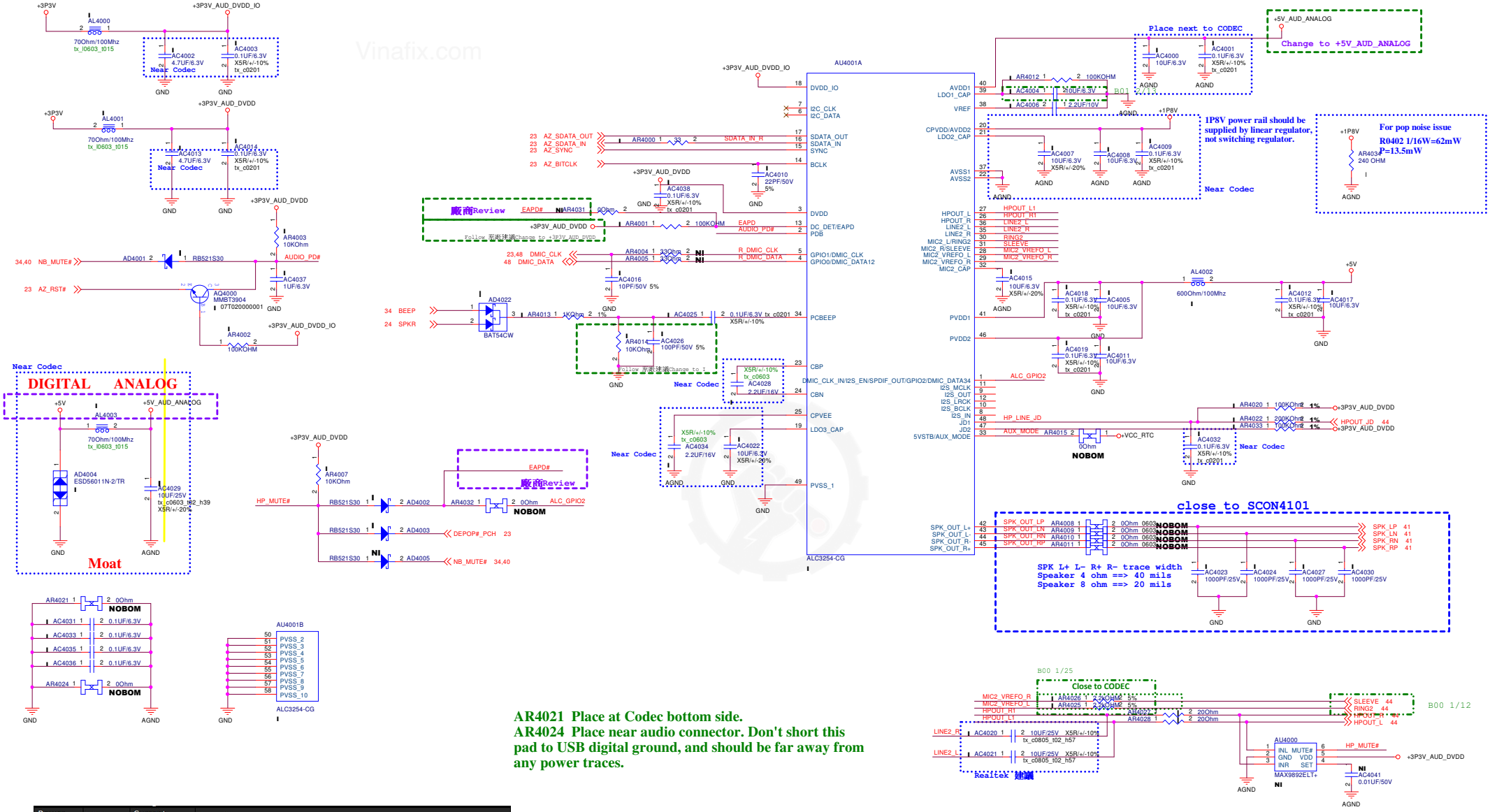
AUDIO CODEC- ALC3254-CG



AR4021 Place at Codec bottom side.
AR4024 Place near audio connector. Don't short this pad to USB digital ground, and should be far away from any power traces.

Power Rail	Voltage	Current (max)	Remark
PVDD1	5.0V	1.5A	4ohm speaker
PVDD2	5.0V	1.5A	4ohm speaker
AVDD1	5.0V	20mA	If Line2-In (PORT 1B) not in use
AVDD1	5.0V	120mA	If Line2-In (port 1B) need to support output with headphone amp.
AVDD2	1.8V	20mA	
CPVDD	1.8V	300mA/150mA/80mA	6ohm/16ohm / 32ohm headphone loading
DVDD	3.3V	10mA	
DVDD-IO	3.3 ~ 1.5V	10mA	

PEGATRON Title : AUDIO_AL3254-CG
Pegatron Corp. Engineer: EE
Size: Custom | Project Name: Nebula | Rev: A00
Date: Wednesday, March 27, 2019 | Sheet 40 of 96

GLOBAL HEADSET CONNECTOR

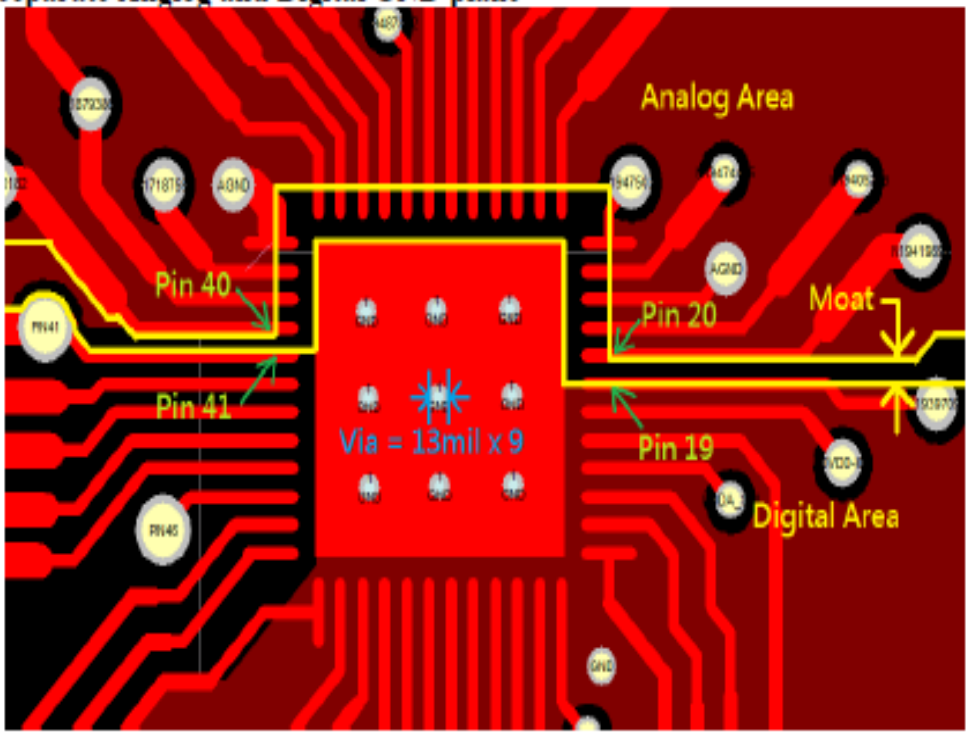
OMTP/CTIA headset, Headphone, Line-Out, Microphone input, Line input.

Below figures are 4-pole jack plugged to the combo phone jack, we could see that right figure's HP-JD pins(#5/#6) attached to HP-L(#1), that imply headset jack has to be fully plugged to make HP JD trigger. This kind of connector will significantly decrease the chance of wrong judgment. Below left figure is not the recommended phone-jack, because its HP-JD(#3/#4) attached to HP right channel.

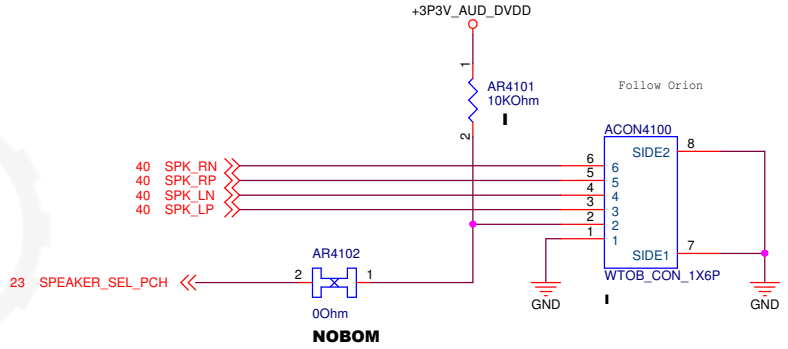
PCB trace width of Mic1-R/Mic1-L(SLEEVE/RING2) are required at least 40 mil for HP crosstalk consideration, and its length should be as short as possible.

FB1/FB2 should choose DC resistance (Rdc) < 30mOhm to get the best audio performance for HP crosstalk.

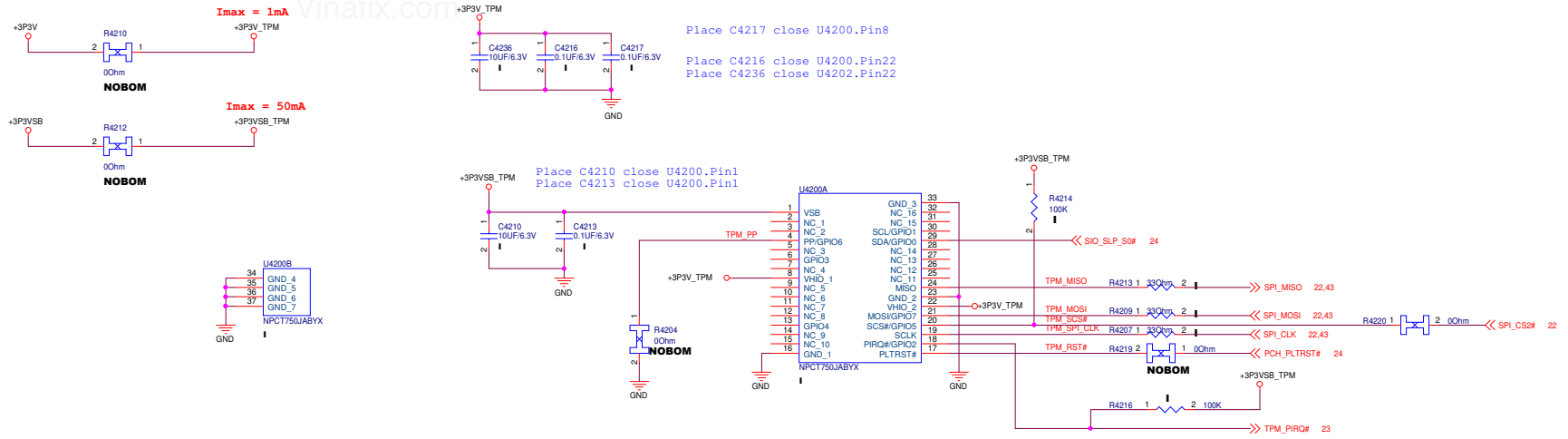
Separate Anglog and Digital GND plane



SPEAKER CONN



PEGATRON	Title : SPEAKER_CONN	
Pegatron Corp.	Engineer: EE	
Size: B	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 41 of 96	



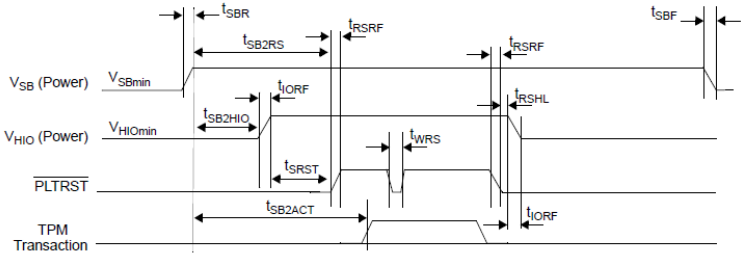
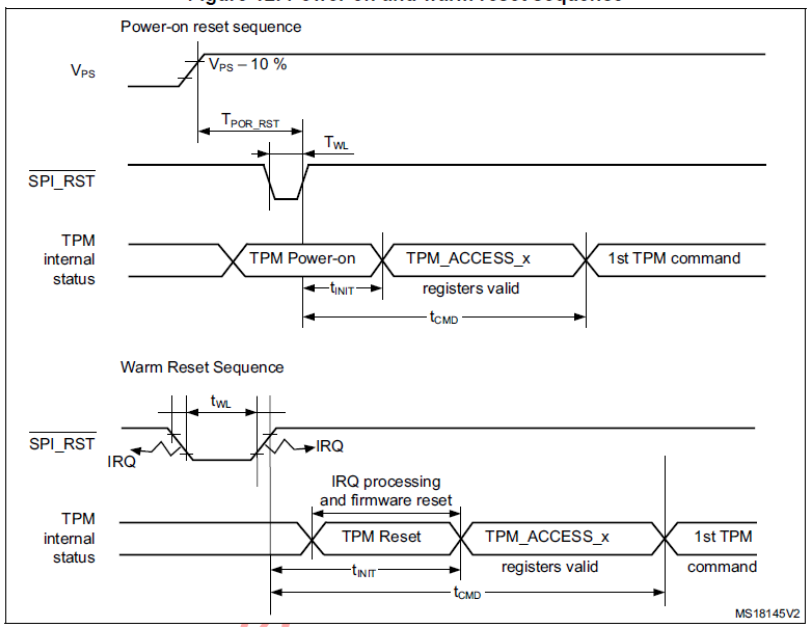


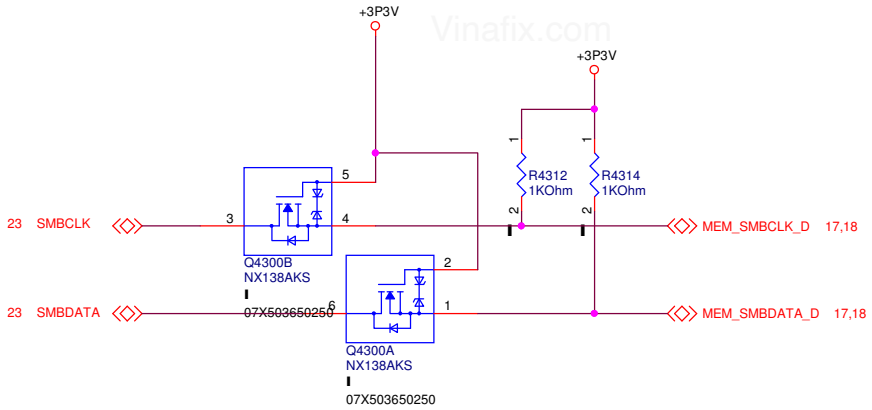
Figure 6. Power and Reset Timing Diagram

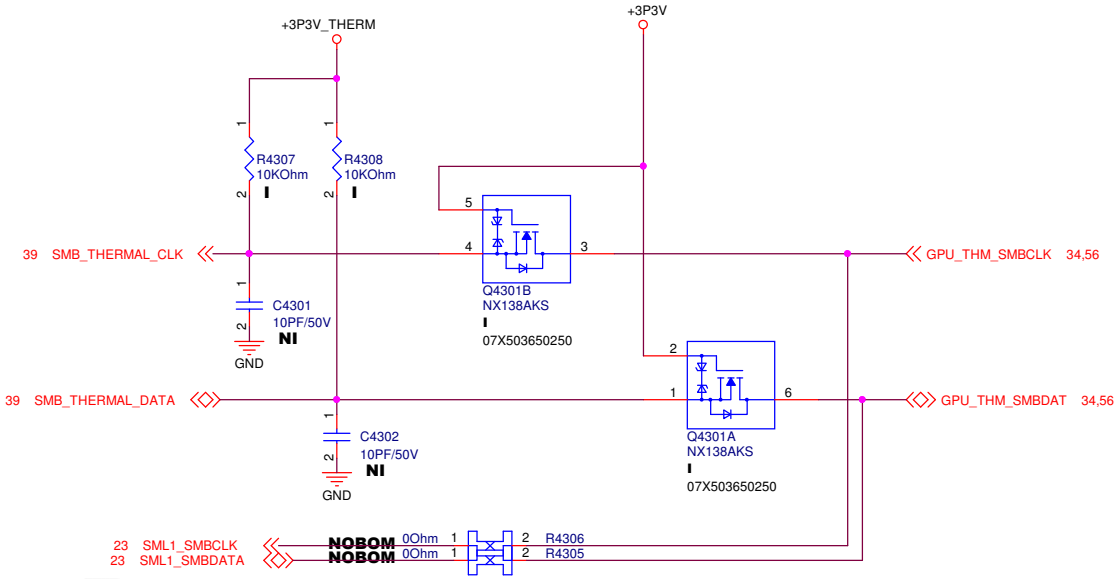
Figure 12. Power on and warm reset sequence



PEGATRON Title : TPM
Pegatron Corp. Engineer: EE
Size C | Project Name Nebula | Rev A00
Date: Wednesday, March 27, 2019 | Sheet 42 of 96

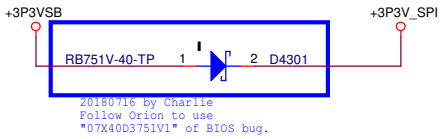
SMBUS



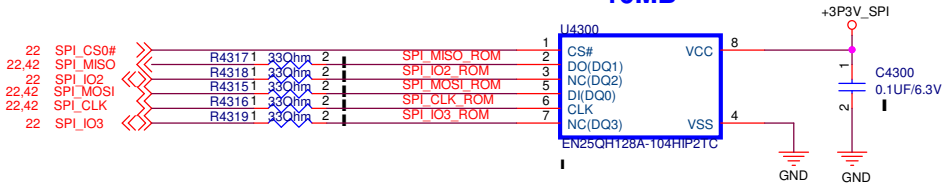


PCH side pull high +3P3VSB 1K

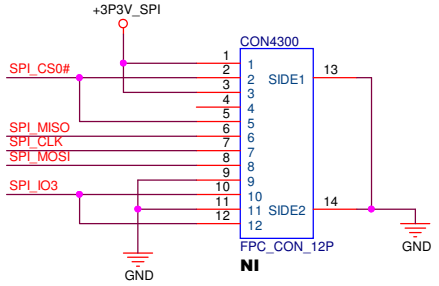
SPI ROM (Quad I/O Supported)



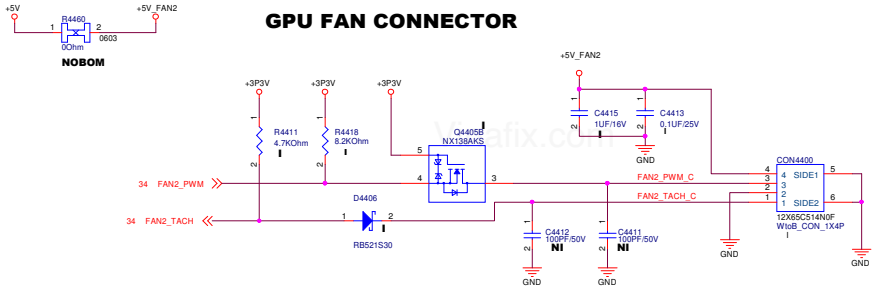
16MB

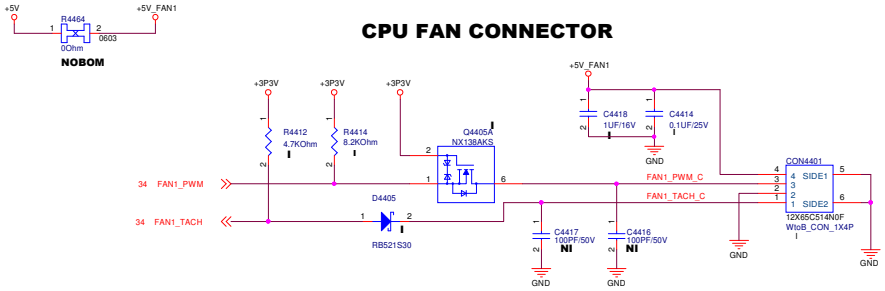


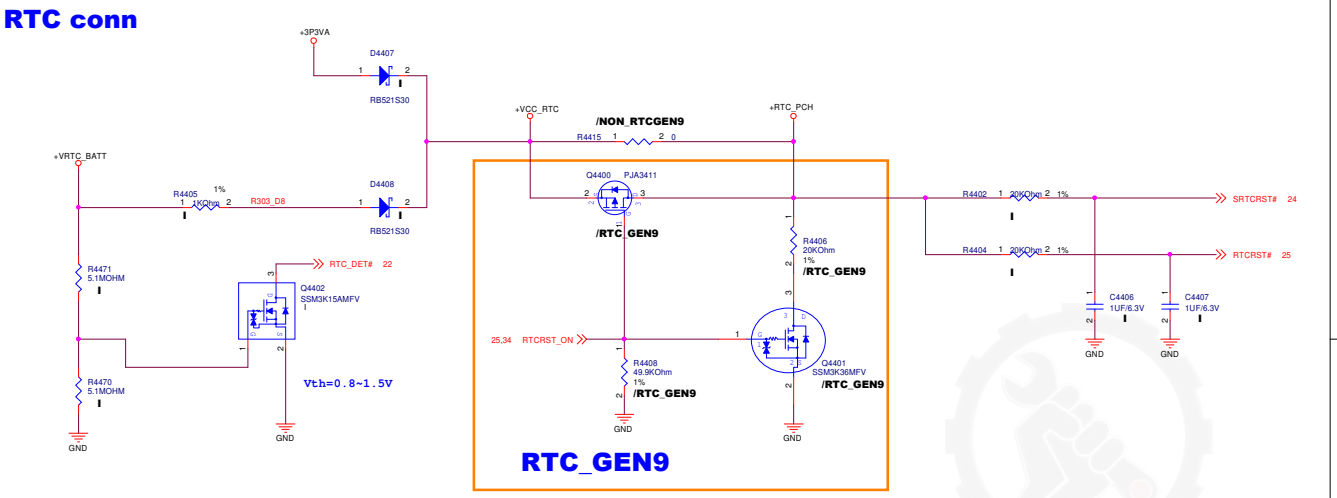
For ROM Flashing

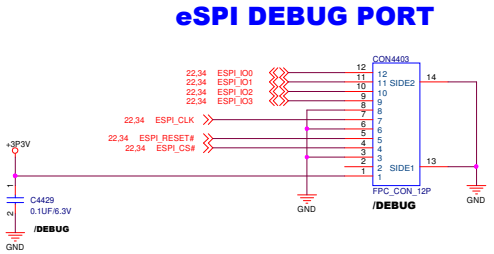


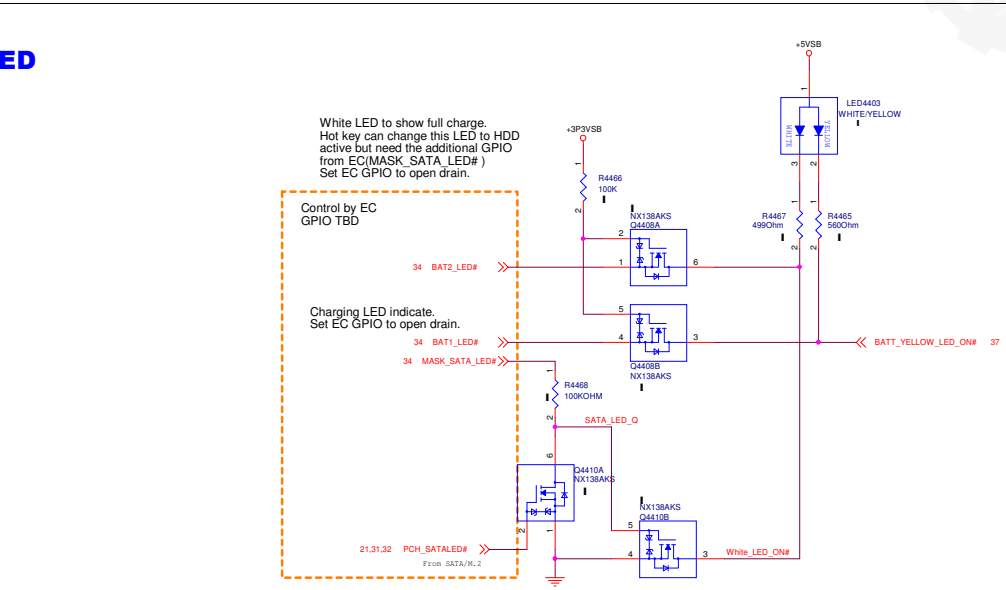
PEGATRON	Title : SM_BUS/SPI_ROM		
Pegatron Corp.	Engineer: EE		
Size: B	Project Name: Nebula		Rev: A00
Date: Wednesday, March 27, 2019	Sheet 43 of 96		

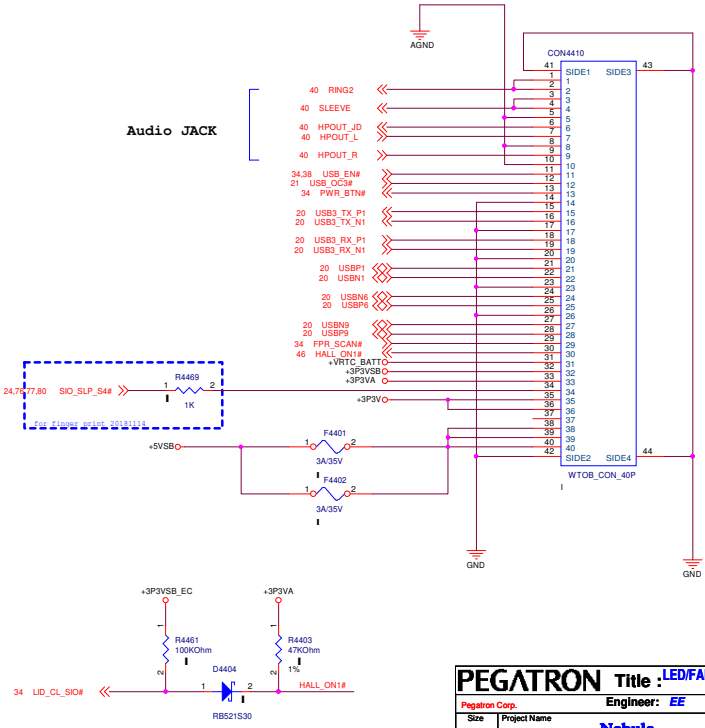












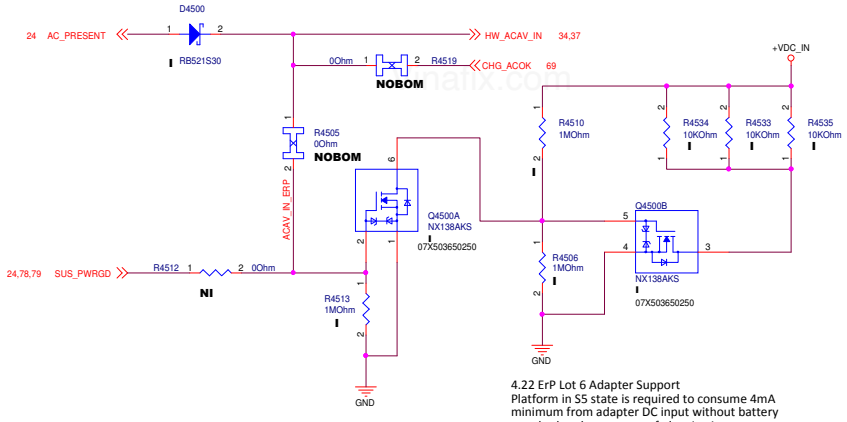
PEGATRON Title : LED/FAN/RTC/IO_CONN

Pegatron Corp. Engineer: EE

Size	Project Name	Rev
Custom	Nebula	A00

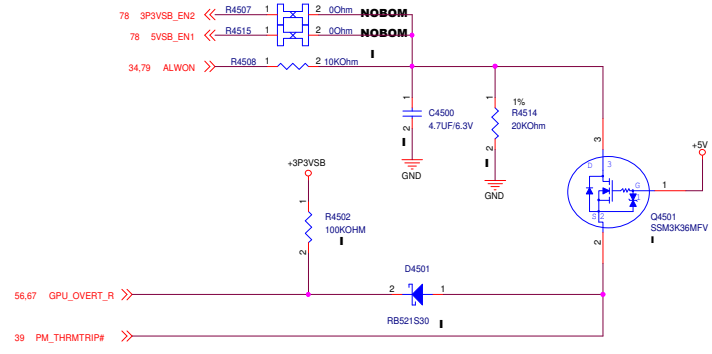
Date: Wednesday, March 27, 2019 Sheet 44 of 98

ACAV_IN Circuit

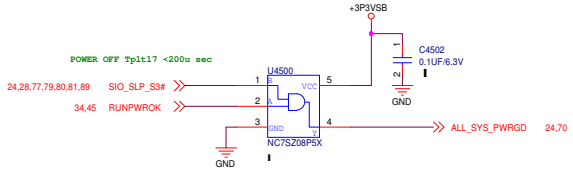


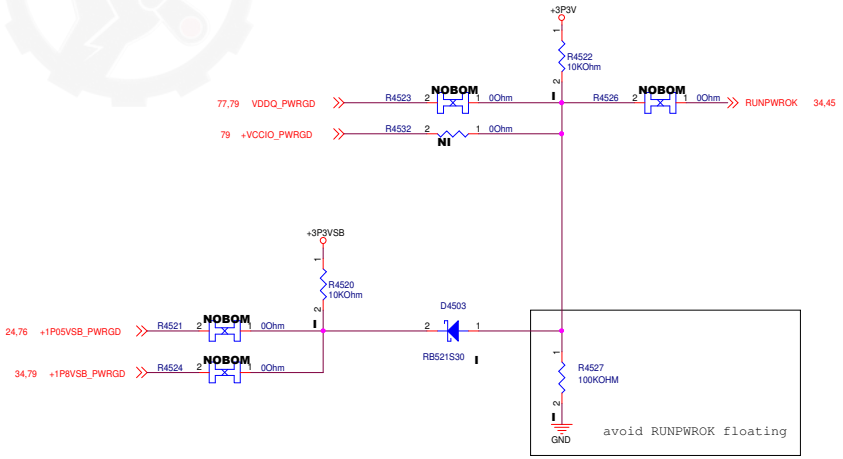
4.22 ErP Lot 6 Adapter Support
Platform in S5 state is required to consume 4mA minimum from adapter DC input without battery attached at the moment of plugging in system.

Thermal CMP Circuit



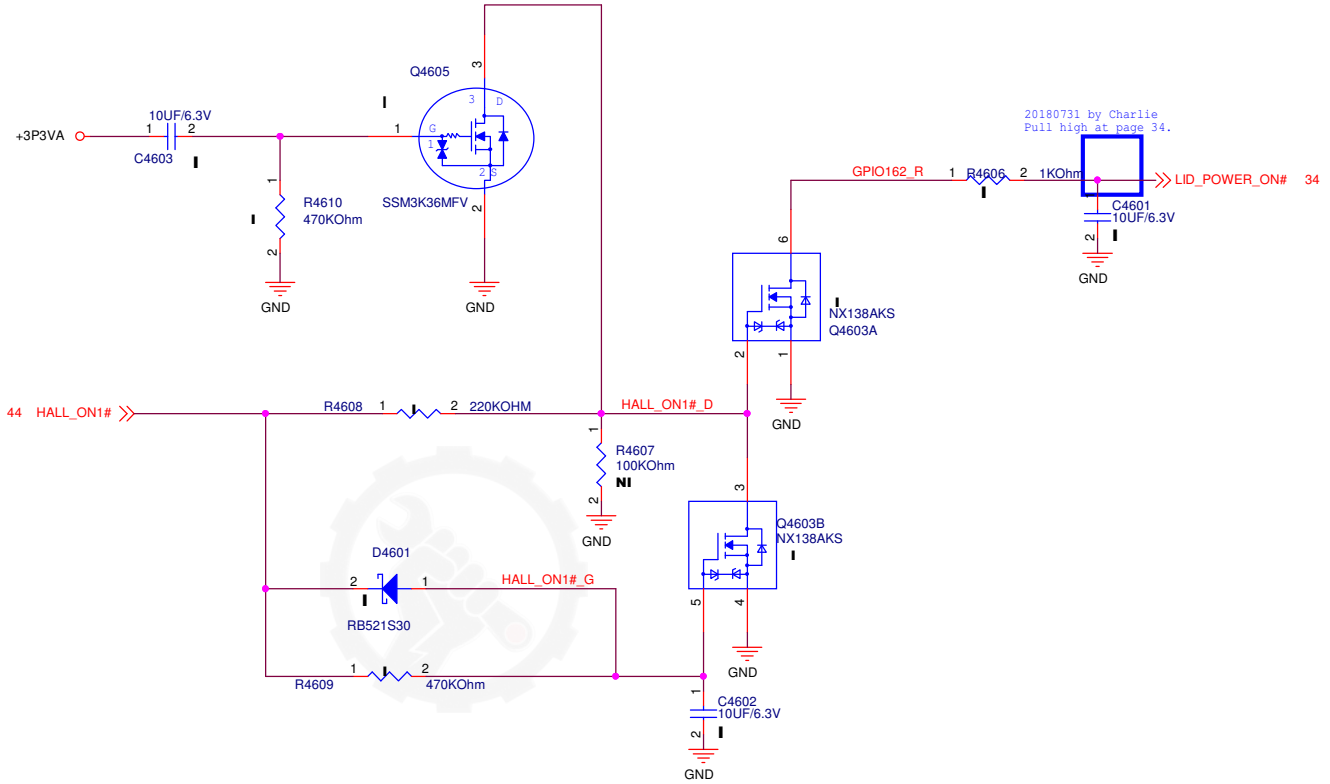
POWER GOOD DETECTER





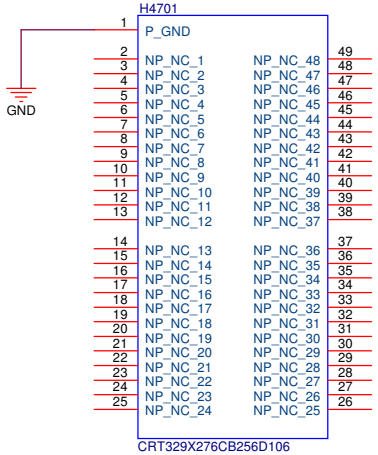
PEGATRON Title : ACAV_IN
Pegatron Corp. Engineer: EE
Size C | Project Name Nebula | Rev A00
Date: Wednesday, March 27, 2019 | Sheet 45 of 96

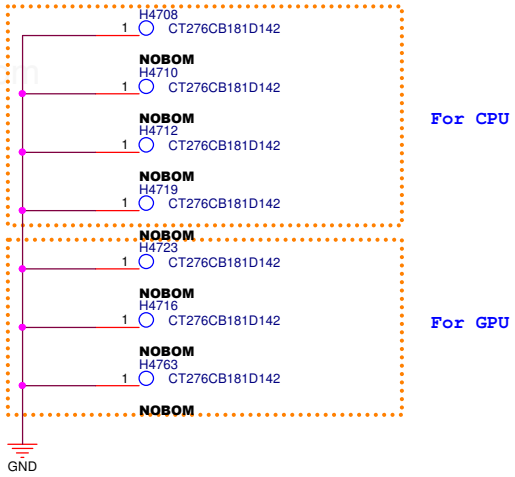
LID OPEN POWER ON

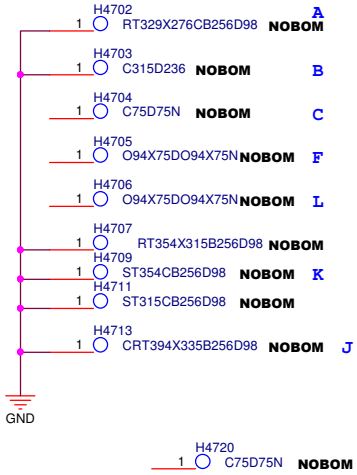


PEGATRON	Title : LID_Open_Power_ON		
Pegatron Corp.	Engineer: EE		
Size: B	Project Name: Nebula		Rev: A00
Date: Wednesday, March 27, 2019	Sheet 46 of 96		

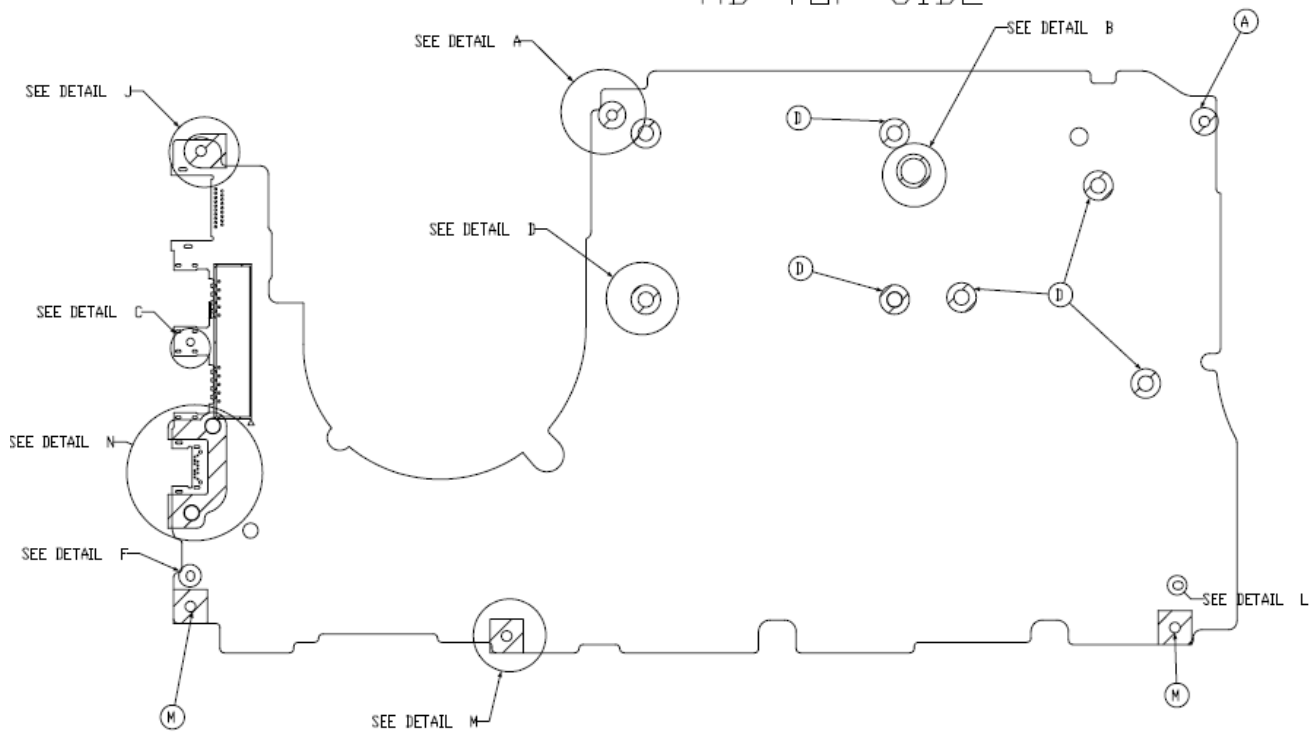
H4701 Thermal 要求修改 2018.10.25





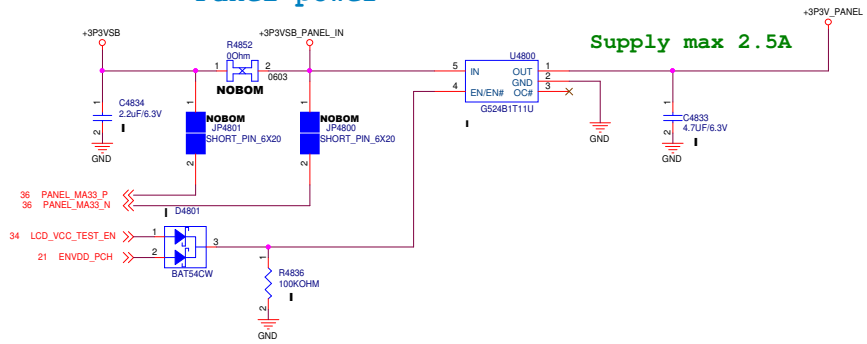


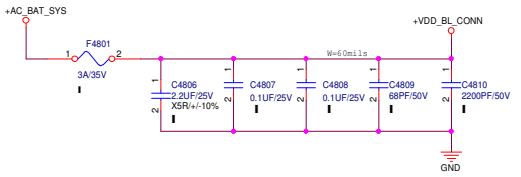
MB TOP SIDE

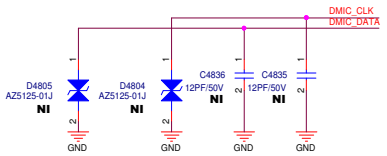


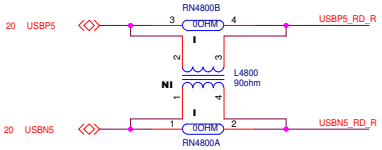
PEGATRON	Title : Label_Screw	
Pegatron Corp.	Engineer: EE	
Size: B	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 47 of 96	

Panel power

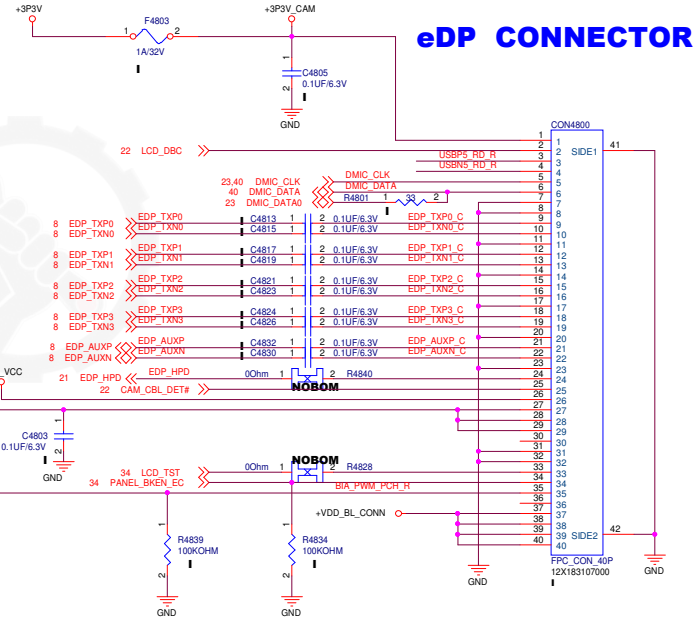








eDP CONNECTOR

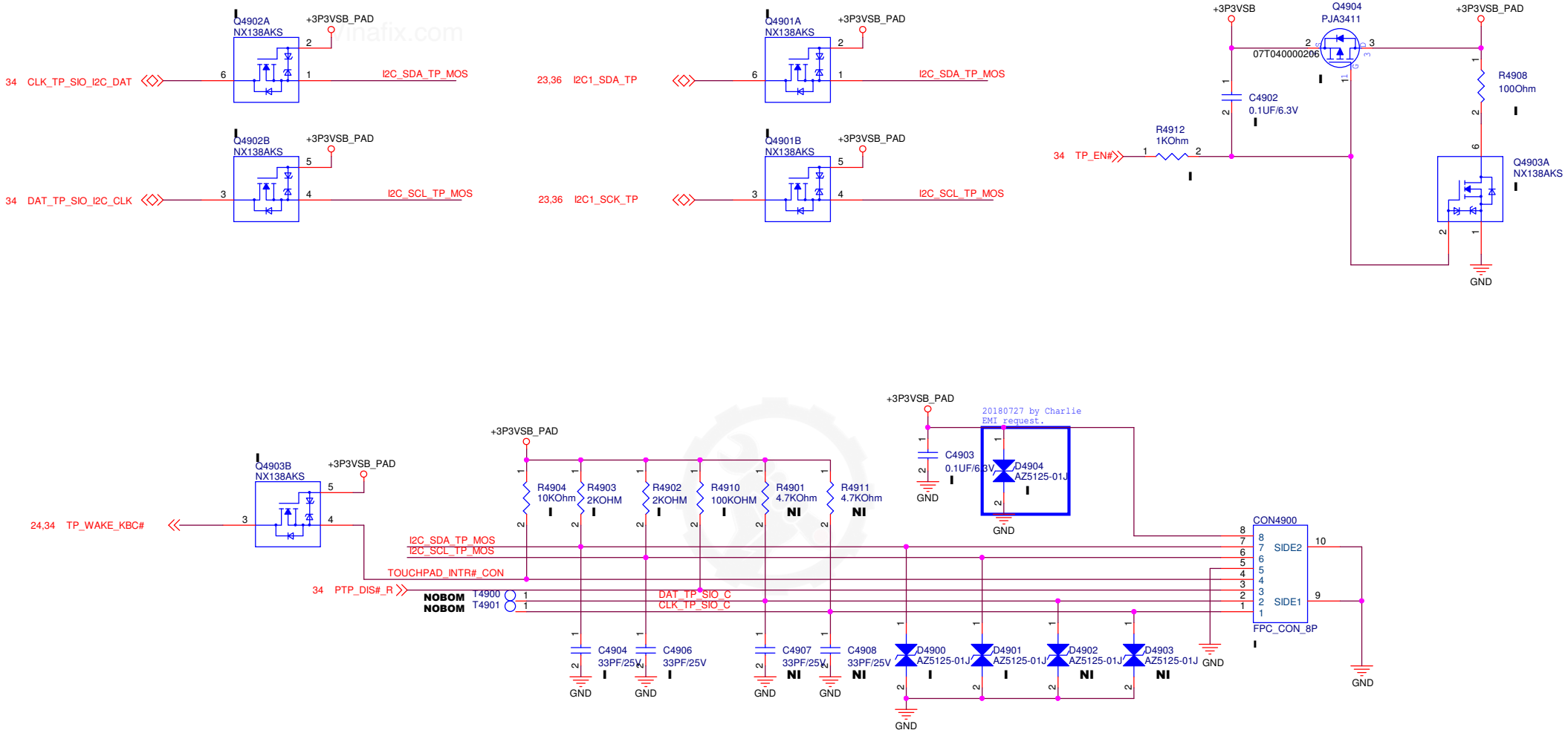


PEGATRON Title : eDP_CONN.

Pegatron Corp. Engineer: EE

Size	Project Name	Rev
C	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 48 of 96



PEGATRON Title : Click_Pad

Pegatron Corp. Engineer: EE

Size	Project Name	Rev
B	Nebula	A00

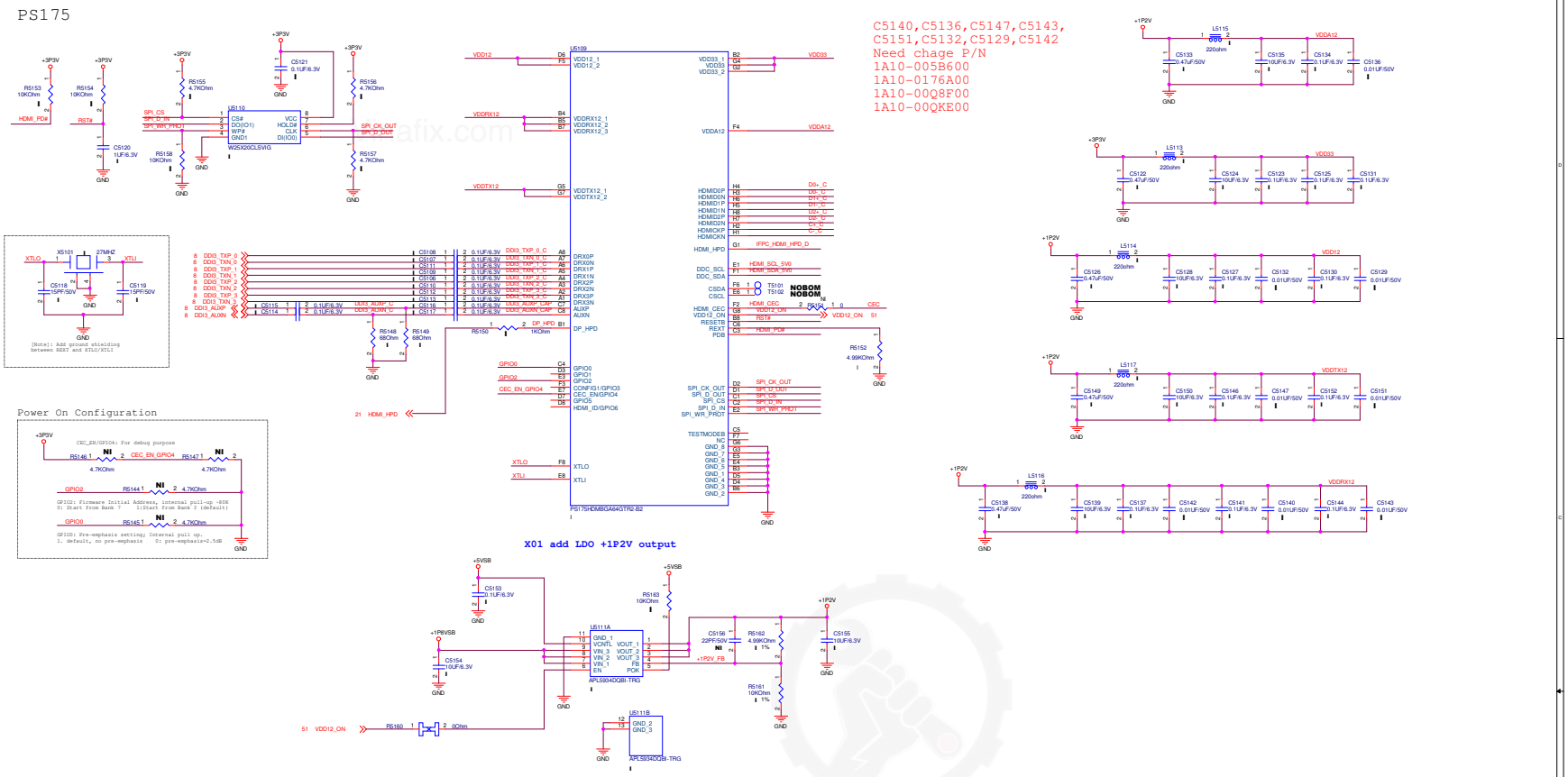
Date: Wednesday, March 27, 2019 Sheet 49 of 96

Reserve Page

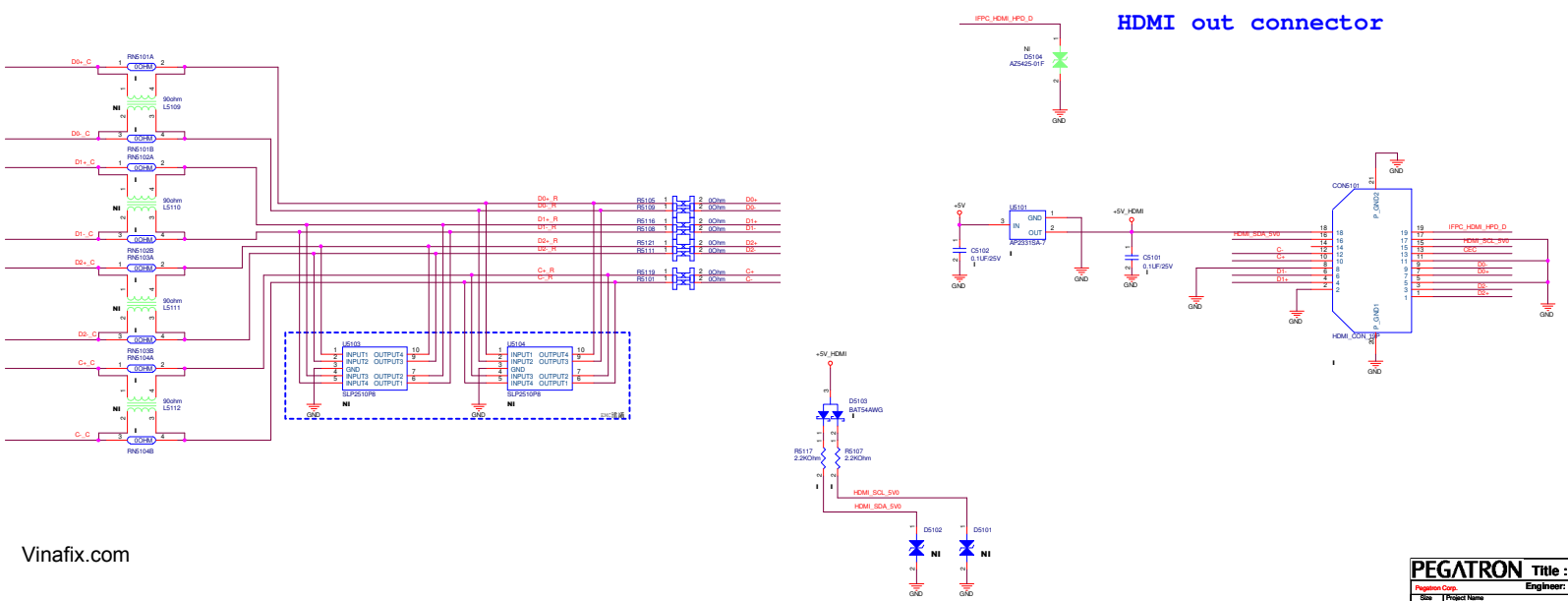
PEGATRON	Title : XXX	
Pegatron Corp.	Engineer: EE	
Size: B	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 50 of 96	

PS175

C5140,C5136,C5147,C5143,
C5151,C5132,C5129,C5142
Need chage P/N
1A10-005B600
1A10-0176A00
1A10-00Q8F00
1A10-00QKE00



HDMI



PEGATRON Title : HDMI_2.0_LSPCON
Pegatron Corp. Engineer: EE
Size: Custom | Project Name: Nebula | Rev: A00
Date: Wednesday, March 27, 2019 | Sheet 51 of 98

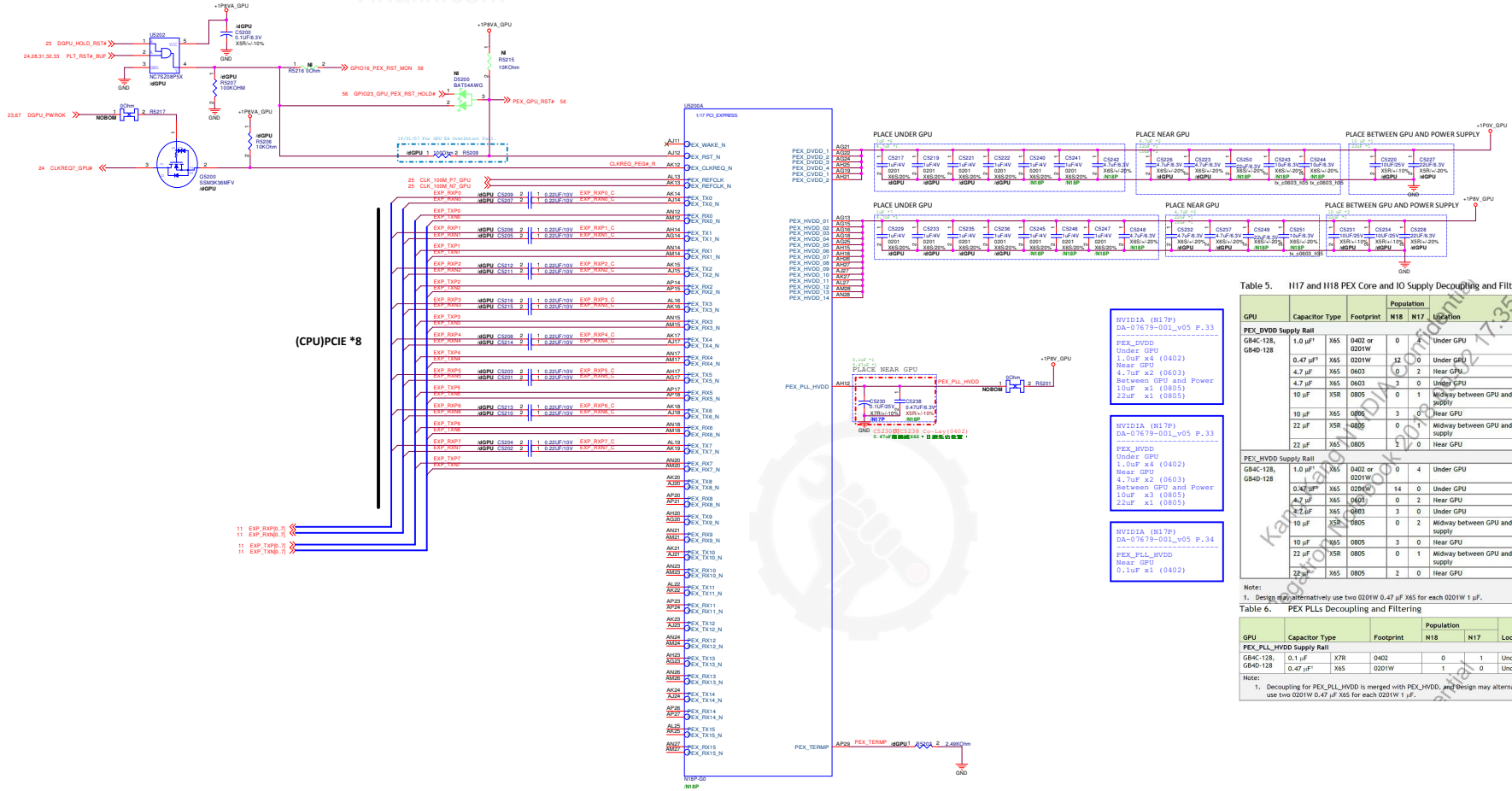


Table 5. N17 and N18 PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N18	Population N17	Location
PEX_DVDD Supply Rail					
GB4C-128, GB4D-128	1.0 µF[1]	X6S	0402 or 0201W	0	4	Under GPU
	0.47 µF[1]	X6S	0201W	12	0	Under GPU
	4.7 µF	X6S	0603	0	2	Near GPU
	4.7 µF	X6S	0603	3	0	Under GPU
	10 µF	X5R	0805	0	1	Midway between GPU and power supply
	10 µF	X6S	0805	3	0	Near GPU
	22 µF	X5R	0805	0	1	Midway between GPU and power supply
	22 µF	X6S	0805	2	0	Near GPU
PEX_HVDD Supply Rail					
GB4C-128, GB4D-128	1.0 µF[1]	X6S	0402 or 0201W	0	4	Under GPU
	0.47 µF[1]	X6S	0201W	14	0	Under GPU
	4.7 µF	X6S	0603	0	2	Near GPU
	4.7 µF	X6S	0603	3	0	Under GPU
	10 µF	X5R	0805	0	2	Midway between GPU and power supply
	10 µF	X6S	0805	3	0	Near GPU
	22 µF	X5R	0805	0	1	Midway between GPU and power supply
	22 µF	X6S	0805	2	0	Near GPU

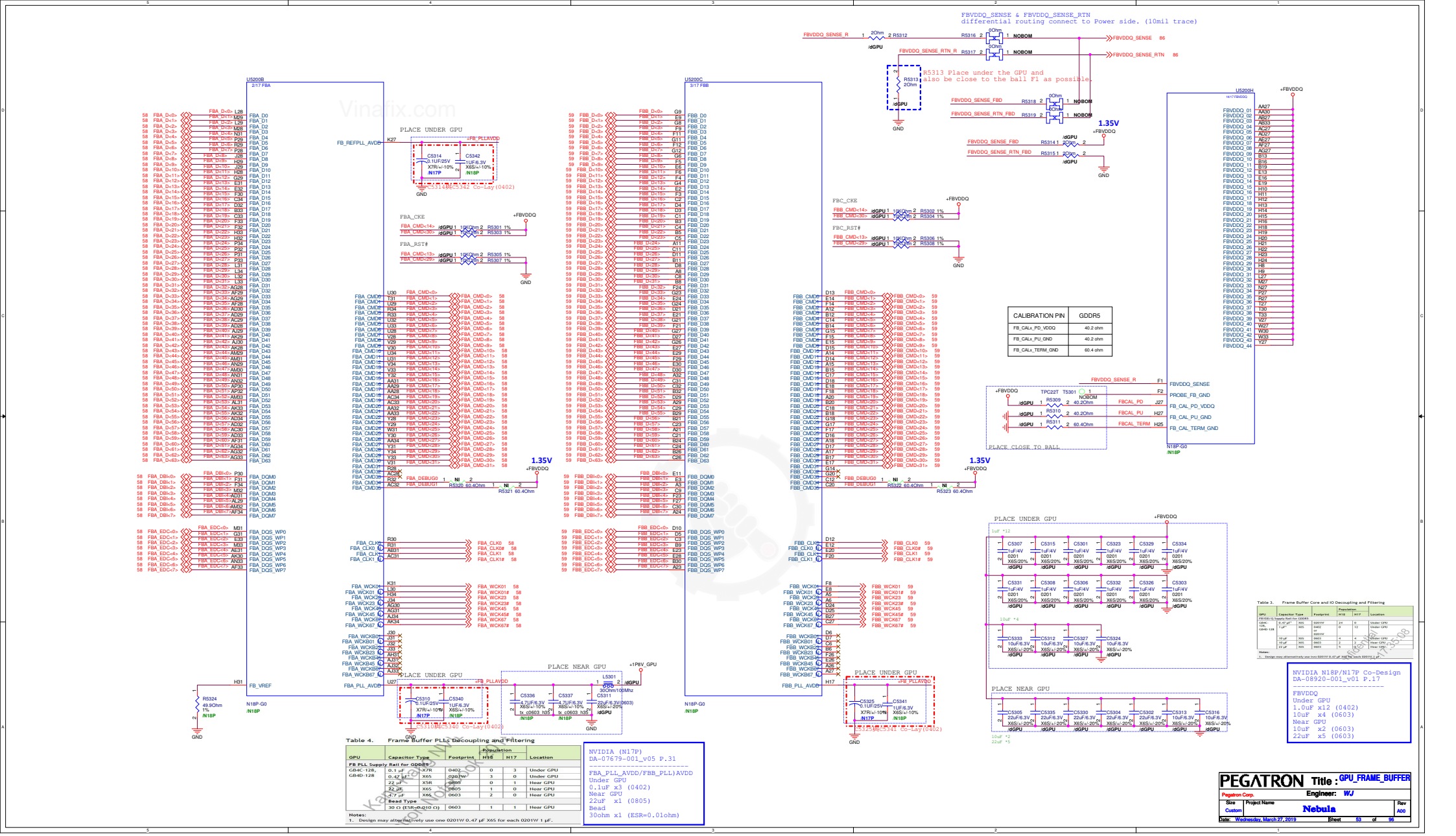
Note:
1. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

Table 6. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N18	Population N17	Location
PEX_PLL_HVDD Supply Rail					
GB4C-128, GB4D-128	0.1 µF	X7R	0402	0	1	Under GPU
	0.47 µF[1]	X6S	0201W	1	0	Under GPU

Note:
1. Decoupling for PEX_PLL_HVDD is merged with PEX_HVDD, and design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

PEGATRON Title : GPU_PCIE
Pegatron Corp. Engineer: WJ
Size: D | Project Name: Nebula | Rev: A00
Date: Wednesday, March 27, 2019 Sheet 58 of 86


FBVDDQ_SENSE & FBVDDQ_SENSE_RTN
differential routing connect to Power side. (10mil trace)
FBVDDQ_SENSE_R
FBVDDQ_SENSE_RTN_R
FBVDDQ_SENSE
FBVDDQ_SENSE_RTN
R5313 Place under the GPU and also be close to the ball F1 as possible.
FBVDDQ_SENSE_FBD
FBVDDQ_SENSE_RTN_FBD
1.35V
+FBVDDQ
GND
PLACE UNDER GPU
PLACE NEAR GPU
PLACE CLOSE TO BALL
FB_REFPLL_AVDD
+FB_PLLAVDD
FBA_CKE
FBA_RST#
FBC_CKE
FBC_RST#
CALIBRATION PIN
GDDR5
FB_CALx_PD_VDDQ
40.2 ohm
FB_CALx_PU_GND
40.2 ohm
FB_CALx_TERM_GND
60.4 ohm
FBCAL_PD
FBCAL_PU
FBCAL_TERM
PROBE_FB_GND
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
FB_VREF
+P8V_GPU
U5200B
U5200C
U5200H
N18P-G0
Table 4. Frame Buffer PLLs Decoupling and Filtering
NVIDIA (N17P)
DA-07679-001_v05 P.31
FBA_PLL_AVDD/FBB_PLL)AVDD
Under GPU
0.1uF x3 (0402)
Near GPU
22uF x1 (0805)
Bead
30ohm x1 (ESR=0.01ohm)
NVIDIA N18P/N17P Co-Design
DA-08920-001_v01 P.17
FBVDDQ
Under GPU
1.0uF x12 (0402)
10uF x4 (0603)
Near GPU
10uF x2 (0603)
22uF x5 (0603)
PEGATRON
Title : GPU_FRAME_BUFFER
Engineer: WJ
Project Name: Nebula
Rev: A00
Date: Wednesday, March 27, 2019
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NVIDIA (N17P)
DA-07679-001_v05 P.37

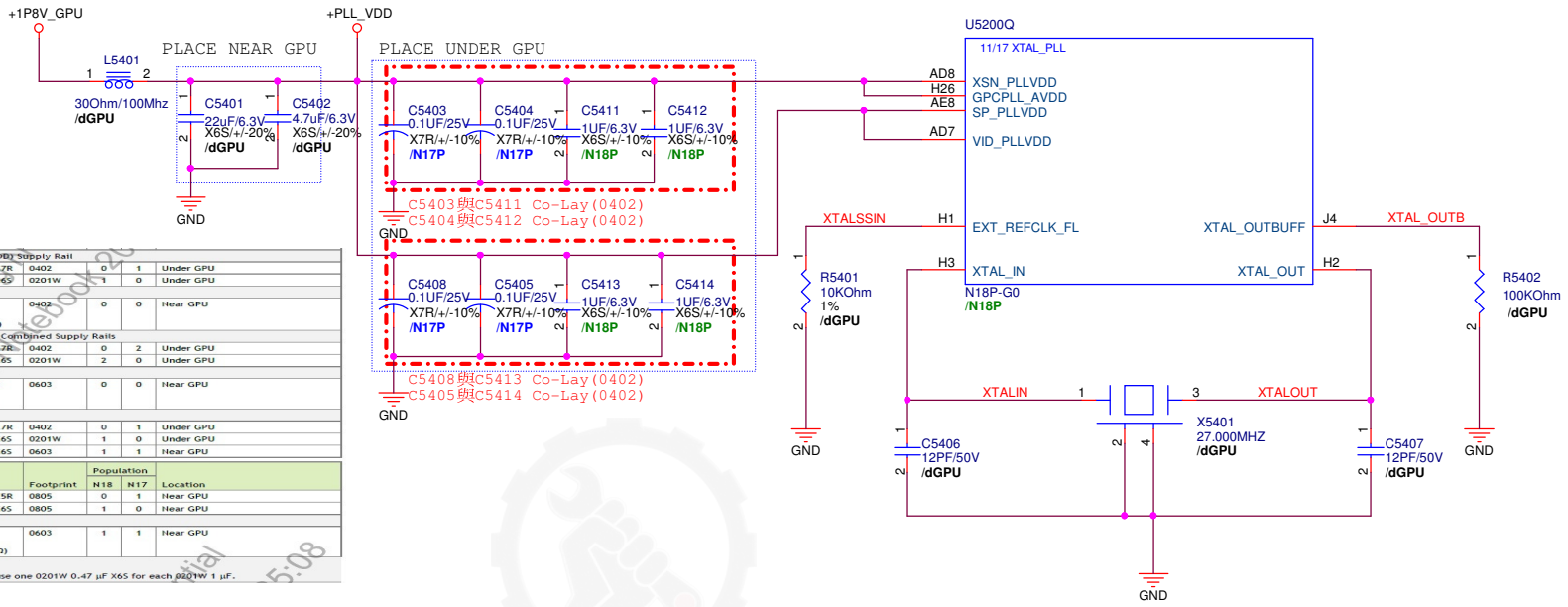
XS_PLLVDD
Under GPU (Put at GPCPLL_AVDD side)
No capacitors

NVIDIA (N17P)
DA-07679-001_v05 P.38

SP_PLLVDD/VID_PLVDD
Under GPU
0.1uF x2 (0402)

NVIDIA (N17P)
DA-07679-001_v05 P.38

GPCPLL_AVDD
Under GPU
0.1uF x1 (0402)
Near GPU
4.7uF x1 (0603)
22 uF x1 (0805)



XS_PLLVDD (N18: XSN_PLLVDD) Supply Rail						
GB4C-128 GB4D-128	0.1 µF	X7R	0402	0	1	Under GPU
	0.47 µF[1]	X6S	0201W	1	0	Under GPU
	Bead Type					
	30 Ω @ 100 MHz (ESR=0.05 Ω)		0402	0	0	Near GPU
SP_PLLVDD and VID_PLLVDD Combined Supply Rails						
GB4C-128 GB4D-128	0.1 µF	X7R	0402	0	2	Under GPU
	0.47 µF[1]	X6S	0201W	2	0	Under GPU
	Bead Type					
	300 Ω @ 100 MHz (ESR=0.2 Ω)		0603	0	0	Near GPU
GPCPLL_AVDD Supply Rail						
GB4C-128 GB4D-128	0.1 µF	X7R	0402	0	1	Under GPU
	0.47 µF[1]	X6S	0201W	1	0	Under GPU
	4.7 µF	X6S	0603	1	1	Near GPU

GPU	Type		Footprint	Population N18	Population N17	Location
	22 µF	X5R	0805	0	1	Near GPU
	22 µF	X6S	0805	1	0	Near GPU
	Bead Type					
	30 Ω @ 100 MHz (ESR=0.010 Ω)		0603	1	1	Near GPU

Note:
1. Design may alternatively use one 0201W 0.47 µF X6S for each 0201W 1 µF.

PEGATRON	Title : GPU_XTAL		
Pegatron Corp.	Engineer: WJ		
Size: B	Project Name: Nebula		Rev: A00
Date: Wednesday, March 27, 2019	Sheet 54 of 96		

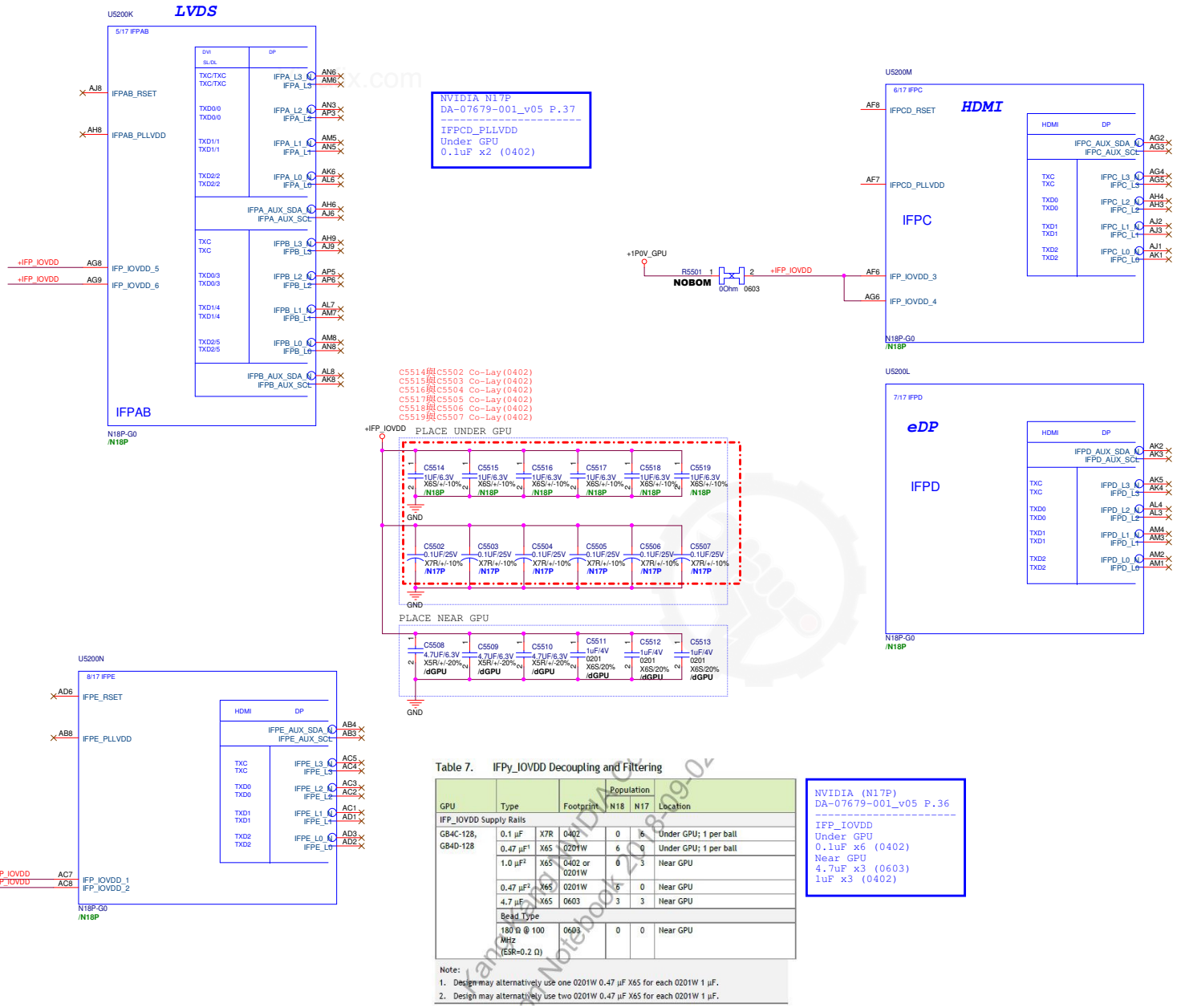

LVDS
U5200K
5/17 IFPAB
IFPAB_RSET
IFPAB_PLLVDD
IFP_IOVDD_5
IFP_IOVDD_6
IFPAB
N18P-G0
/N18P
NVIDIA N17P
DA-07679-001_v05 P.37
IFPCD_PLLVDD
Under GPU
0.1uF x2 (0402)
HDMI
U5200M
6/17 IFPC
IFPCD_RSET
IFPCD_PLLVDD
IFP_IOVDD_3
IFP_IOVDD_4
IFPC
R5501
NOBOM
0Ohm
0603
+1P0V_GPU
+IFP_IOVDD
C5514與C5502 Co-Lay(0402)
C5515與C5503 Co-Lay(0402)
C5516與C5504 Co-Lay(0402)
C5517與C5505 Co-Lay(0402)
C5518與C5506 Co-Lay(0402)
C5519與C5507 Co-Lay(0402)
PLACE UNDER GPU
C5514 C5515 C5516 C5517 C5518 C5519
1UF/6.3V X6S/+/-10% /N18P
C5502 C5503 C5504 C5505 C5506 C5507
0.1UF/25V X7R/+/-10% /N17P
GND
PLACE NEAR GPU
C5508 C5509 C5510 C5511 C5512 C5513
4.7UF/6.3V X5R/+/-20% /dGPU
1uF/4V 0201 X6S/20% /dGPU
U5200L
7/17 IFPD
eDP
IFPD
U5200N
8/17 IFPE
IFPE_RSET
IFPE_PLLVDD
IFP_IOVDD_1
IFP_IOVDD_2
Table 7. IFPy_IOVDD Decoupling and Filtering
GPU | Type | Footprint | Population N18 | Population N17 | Location
IFP_IOVDD Supply Rails
GB4C-128, GB4D-128
0.1 µF X7R 0402 0 6 Under GPU; 1 per ball
0.47 µF[1] X6S 0201W 6 0 Under GPU; 1 per ball
1.0 µF[2] X6S 0402 or 0201W 0 3 Near GPU
0.47 µF[2] X6S 0201W 6 0 Near GPU
4.7 µF X6S 0603 3 3 Near GPU
Bead Type
180 Ω @ 100 MHz (ESR=0.2 Ω) 0603 0 0 Near GPU
Note:
1. Design may alternatively use one 0201W 0.47 µF X65 for each 0201W 1 µF.
2. Design may alternatively use two 0201W 0.47 µF X65 for each 0201W 1 µF.
NVIDIA (N17P)
DA-07679-001_v05 P.36
IFP_IOVDD
Under GPU
0.1uF x6 (0402)
Near GPU
4.7uF x3 (0603)
1uF x3 (0402)
PEGATRON
Title : GPU_HDMI
Pegatron Corp.
Engineer: WJ
Size C
Project Name Nebula
Rev A00
Date: Wednesday, March 27, 2019
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Table 5.4 Display Link to SORx_EXPOSED Mapping for Down Designs

Total Display Links (HDMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	Is IFPD used? (Only supports eDP.)	See This Row of Table 5.5
3	2	YES	12
2	2	NO	12
2	1	YES	8
1	1	NO	8
1	0	YES	0
No other configurations are supported.			

Table 12.4 FS_OVERT* Strap Enablement For N18X

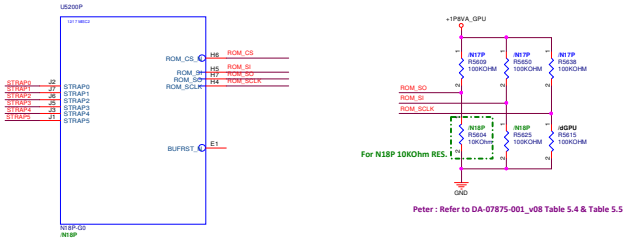
Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

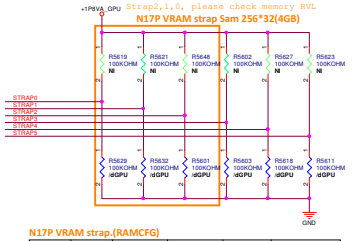
Note 1: Configurations other than the two listed in Table 12.4 must be avoided, as otherwise damage to strap inputs may result.

Note 2: The ROM_SO pin should be pulled low using a 10 kΩ resistor instead of a 100 kΩ resistor.

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
All other Strap Configurations				(Reserved)			





N17P VRAM strap.(RAMCFG)

Strap								
0	1	2	RAMCFG Num	BVL	Vendor PN	Page PN	Micron	
L	L	L	0	Sam 256*32(8Gb)	K4G80325FE-HC28	0101-01G6G0E	RS629, RS632, RS601	
L	L	L	1					
L	L	H	2					
L	L	H	3					
L	H	L	4	Mic 256*32(8Gb)	MT51J256M32HF-70:B	0101-02G0G0E	RS629, RS632, RS648	
L	H	L	5	Hyn 256*32(8Gb)	H5GC8H24AJR-R0C	0101-02G0G0E	RS603, RS632, RS648	
L	H	H	6					
L	H	H	7					
H	L	L	8					

N18P VRAM strap.(RAMCFG)

Strap							
0	1	2	RAMCFG Num	BVL	Vendor PN	Page PN	Micron
L	L	L	0				
L	L	L	1				
L	L	H	2	Mic 256*32(8Gb)	MT51J256M32HF-80:B	0101-02H1G0E	RS629, RS632, RS601
L	L	H	3	Hyn 256*32(8Gb)	H5GC8H24AJR-R2C	0101-02G0G0E	RS629, RS632, RS603
L	H	L	4				
L	H	L	5				
L	H	H	6				
L	H	H	7	Sam 256*32(8Gb)	K4G80325FC-HC25	N/A	RS629, RS632, RS648

RVL-07916-001_v16_N17x GeForce Memory RVL

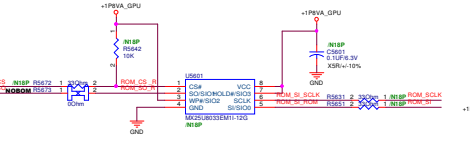
Table 3. H17P-G1/G0/G0-K1* GDDR5 Recommended Memories

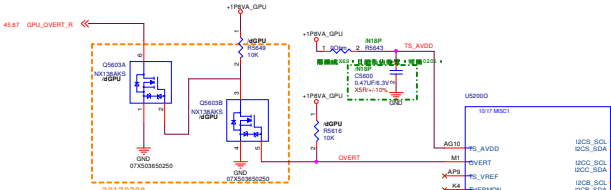
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V[2]	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[1]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[1]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[1]
			Micron	MT51J256M32HF-70:B	B-die	0x4	7 Gbps	N/A	Full	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x4	8 Gbps	N/A	N/A	Substitution allowed with waiver[1]
			Hynix	H5GC8H24AJR-R0C	A-die	0x5	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x5	8 Gbps	N/A	N/A	Substitution allowed with waiver[1]

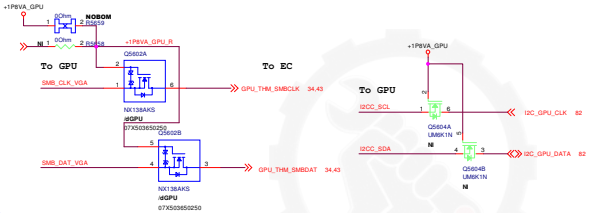
Table 4. N18P-G0 GDDR5 Recommondod Memories

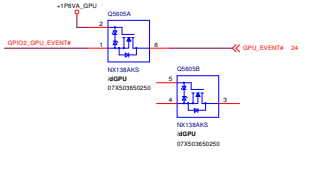
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35 V and 1.5V[1]	Micron[2]	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0x2	8 Gbps	N/A	Full	Production candidate
		TBD	Samsung[2]	K4G80325FC-HC25	C-die	0x4	8 Gbps	N/A	Full	Post production candidate

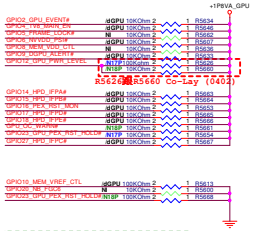
RVL-08928-001_v05_N18x GeForce Memory RVL



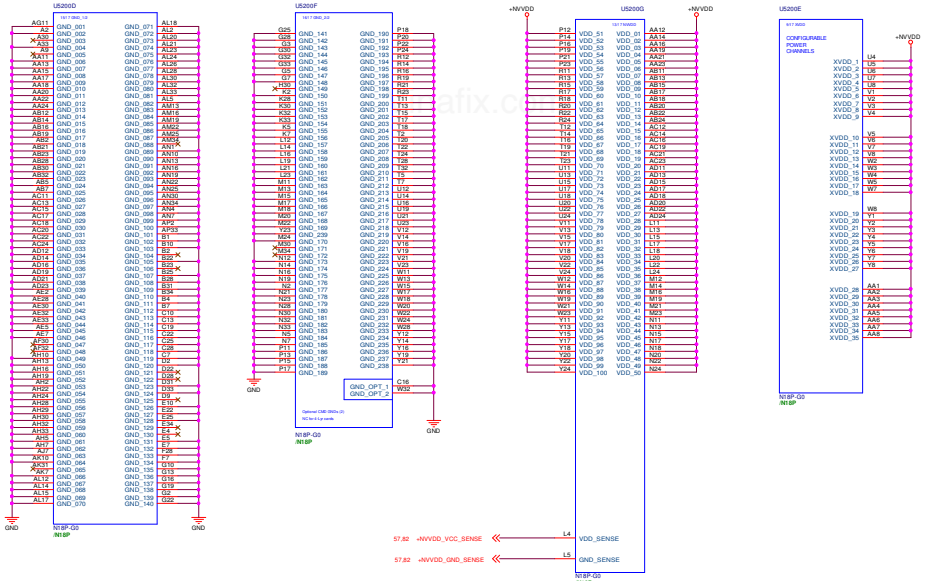








PEGATRON Title : GPU_GPIO_STRAP
Pegatron Corp. Engineer: WJ
Size: D | Project Name: Nebula | Rev: A00
Date: Wednesday, March 27, 2019 Sheet 56 of 96



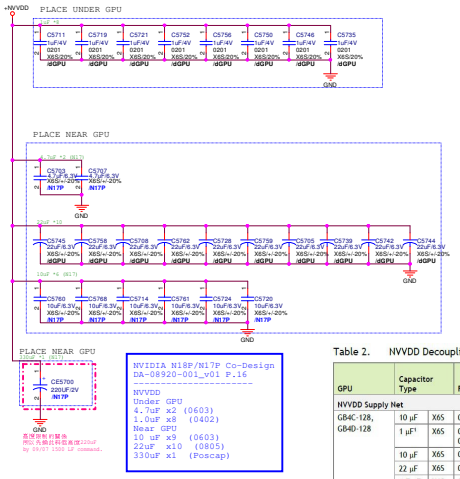


Table 2. NVVDD Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N18	Population N17	Location
NVVDD Supply Net						
GB4C-128, GB4D-128	10 µF	X6S	0603	34	21	Under GPU
	1 µF[1]	X6S	0402 or 0201W	13	13	Under GPU
	10 µF	X6S	0603	0	11	Near GPU
	22 µF	X6S	0805	15	10	Near GPU
	4.7 µF	X6S	0603	0	2	Near GPU
	330 µF	POS	7343	0	1	Near GPU

Note:
1. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

C5737 C5748 Co-Lay (0402)
C5738 C5764 Co-Lay (0402)

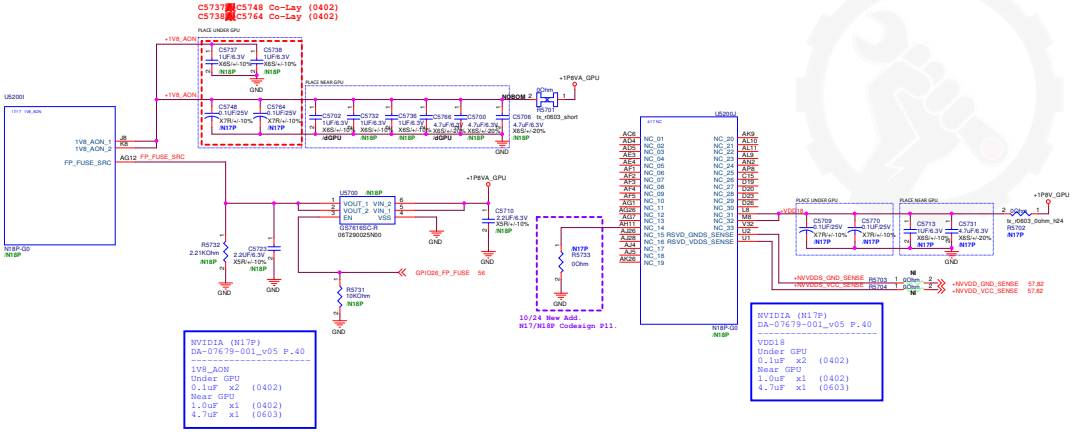
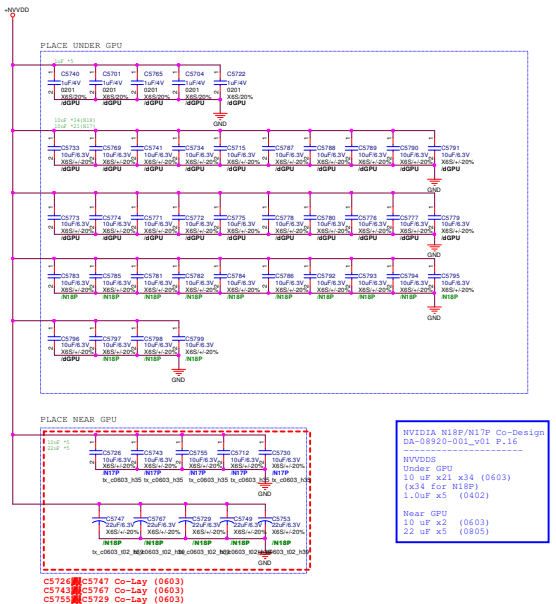


Table 9. VDD_AON and VDD_MAIN Decoupling

GPU	Capacitor Type		Footprint	Population N18	Population N17	Location
N17 VDD18 (N18 NC) Supply Rail						
GB4C-128, GB4D-128	0.1 µF	X7R	0402	N/A	2	Under GPU
	1.0 µF	X6S	0603	N/A	1	Near GPU
	4.7 µF	X6S	0603	N/A	1	Near GPU
1V8_AON Supply Rail						
GB4C-128, GB4D-128	0.1 µF	X7R	0402	0	2	Under GPU
	0.47 µF[1]	X6S	0201W	4	0	Under GPU
	1.0 µF[1]	X6S	0402 or 0201W	0	1	Near GPU
	0.47 µF[1]	X6S	0201W	6	0	Near GPU
	4.7 µF	X6S	0603	3	1	Near GPU

Note:
1. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.



C5726 C5747 Co-Lay (0603)
C5743 C5767 Co-Lay (0603)
C5755 C5729 Co-Lay (0603)
C5712 C5749 Co-Lay (0603)
C5730 C5753 Co-Lay (0603)

PEGATRON Title : GPU_Power_GND
Pegatron Corp. Engineer: WJ
Size: D | Project Name: Nebula | Rev: A00
Date: Wednesday, March 27, 2019 | Sheet 57 of 96

MEMORY : FBA Partition 31:0 (Normal)
MEMORY : FBA Partition 63:32 (Mirror)

GDDR5 Mode H Mapping

GB2B-64 GB4B-128 GB4C-128	Ch0 0..31	GB2B-64 GB4B-128 GB4C-128	Ch1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

DRAM M3 0 Normal 2 DRAM M4 7 Mirror 5

U5801A U5801B U5802A U5802B

1 3 6 4

H5GC8H24MJR-R0C /N17P /K1_NI /N17P

DRAM M3 DRAM M4

U5801C U5801D U5802C U5802D

NOBOM R5803 0Ohm NI R5801 0Ohm NOBOM R5802 0Ohm NI R5804 0Ohm

MF =1 (PU) : Mirror MF =0 (PD) : Normal

Q5801 SSM3K36MFV /dGPU

R5807 40.2Ohm /dGPU /K1_NI R5808 40.2Ohm /dGPU /K1_NI R5805 40.2Ohm /dGPU R5806 40.2Ohm /dGPU

R5809 549OHM /dGPU R5810 1.33KOHM /dGPU R5813 121Ohm /dGPU /K1_NI R5812 121Ohm /dGPU

C5808 0.01UF/50V /dGPU /K1_NI C5824 820PF/50V /dGPU /K1_NI C5848 0.01UF/50V /dGPU C5811 820PF/50V /dGPU

NVIDIA (N17P)
DG-07875-001_v08 page.160

+FBVDDQ at DRAM Side
Under GPU
1uF x10 (0402)
10uF x4 (0603)
1uF x8 (0402)
Near GPU
10uF x2 (0603)

Note : At least 2 GND vias and 2 power vias for each decoupling capacitor

Place Under DRAM M3 Place Under DRAM M3

Place Near DRAM M3

Place Under DRAM M4 Place Under DRAM M4

Place Near DRAM M4

PEGATRON Title : N17P_GDDR5_CH A
Pegatron Corp. Engineer: WJ
Size C Project Name Nebula Rev A00
Date: Wednesday, March 27, 2019 Sheet 58 of 96

Pin Swap. M1.M11 <-> M1.M13
Pin Swap. M1.M13 <-> M1.N11
Pin Swap. M1.N11 <-> M1.M11

MEMORY : FBB Partition 31:0 (Normal)
MEMORY : FBB Partition 63:32 (Mirror)

GDDR5 Mode H Mapping

GB2B-64 GB4B-128 GB4C-128	Ch0 0..31	GB2B-64 GB4B-128 GB4C-128	Ch1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

Pin Swap. M1.E11 <-> M1.F13
Pin Swap. M1.M2 <-> M1.M4

NVIDIA (N17P)
DG-07875-001_v08 page.160

+FBVDDQ at DRAM Side
Under GPU
1uF x10 (0402)
10uF x4 (0603)
1uF x8 (0402)
Near GPU
10uF x2 (0603)

Note : At least 2 GND vias and 2 power vias for each decoupling capacitor

Place Under DRAM M1
Place Under DRAM M2
Place Near DRAM M1
Place Near DRAM M2

vmafix.com

PEGATRON	Title : N17P_GDDR5_CH B
Pegatron Corp.	Engineer: WJ
Size: C	Project Name: Nebula
Rev: A00	
Date: Wednesday, March 27, 2019	Sheet 59 of 96

PEGATRON	Title : GPU_XXX	
Pegatron Corp.	Engineer: EE	
Size: B	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 60 of 96	

PEGATRON	Title : GPU_XXX	
Pegatron Corp.	Engineer: EE	
Size: B	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 61 of 96	

PEGATRON	Title : GPU_XXX	
Pegatron Corp.	Engineer: EE	
Size: B	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 62 of 96	

PEGATRON	Title : GPU_XXX	
Pegatron Corp.	Engineer: EE	
Size: B	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 63 of 96	

PEGATRON	Title : GPU_XXX	
Pegatron Corp.	Engineer: EE	
Size: B	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 64 of 96	

PEGATRON Title : GPU_XXX

Pegatron Corp. Engineer: EE

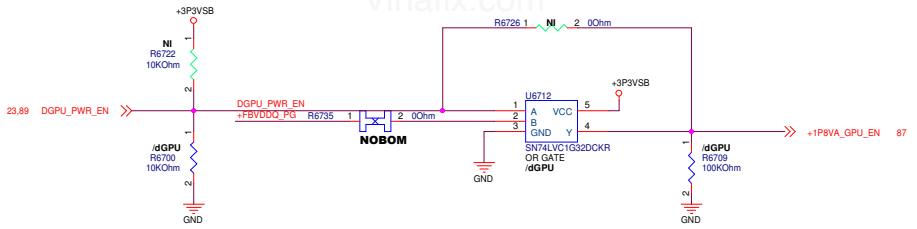
Size	Project Name	Rev
B	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 65 of 96

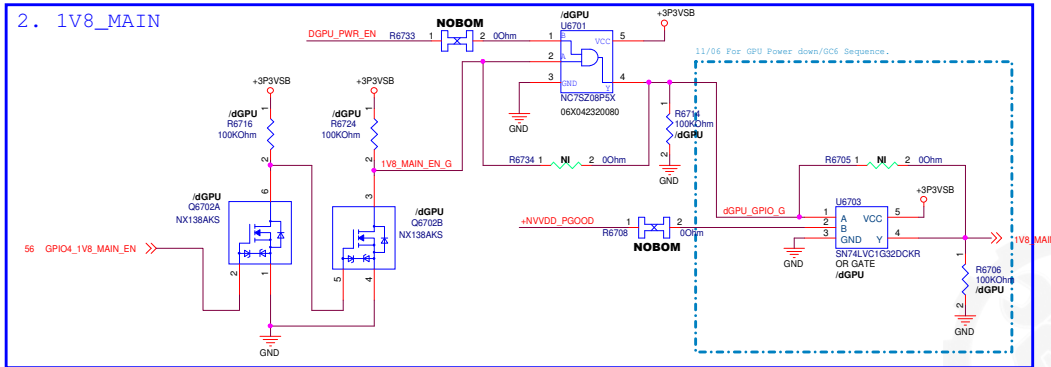
PEGATRON	Title : GPU_XXX
Pegatron Corp.	Engineer: EE
Size: B	Project Name: Nebula
Rev: A00	
Date: Wednesday, March 27, 2019	Sheet 66 of 96

GPU_POWER Sequence

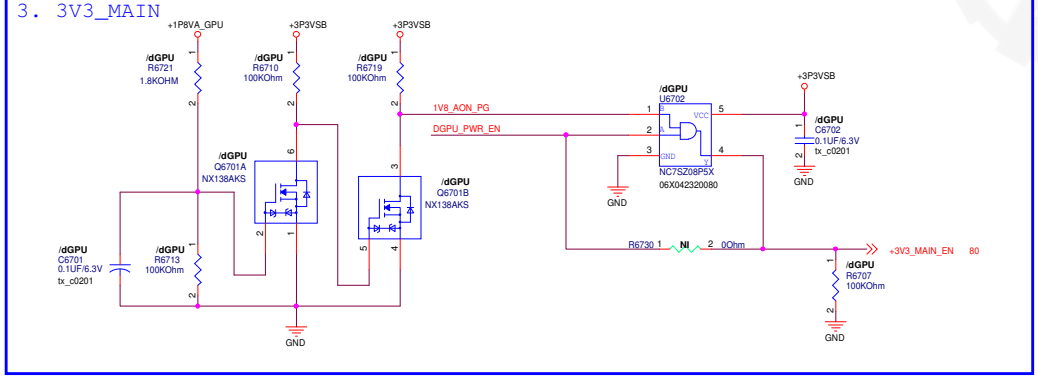
1.1V8_AON



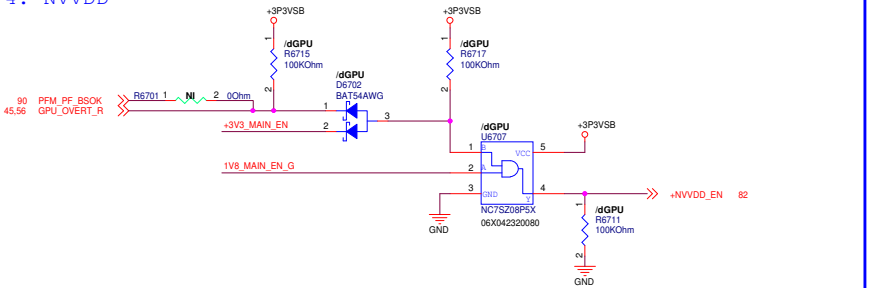
2. 1V8_MAIN



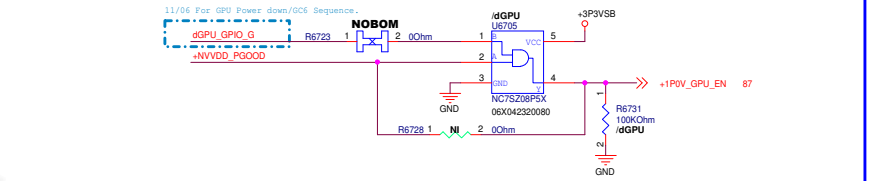
3. 3V3_MAIN



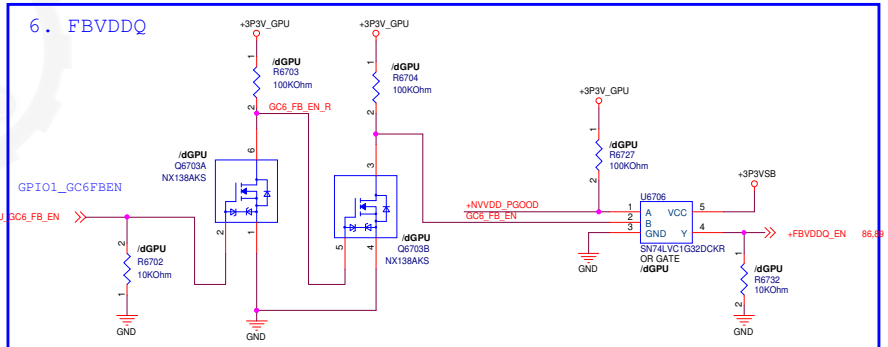
4. NVVDD



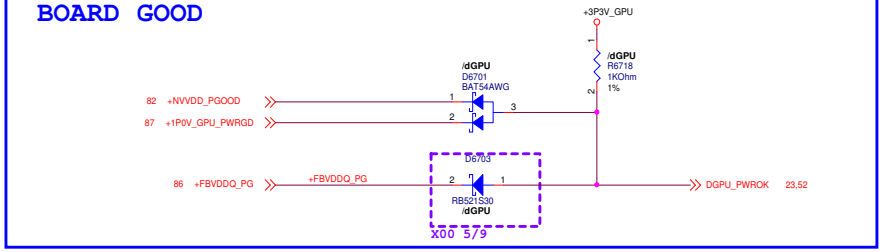
5. PEX_VDD



6. FBVDDQ



BOARD GOOD



PEGATRON Title : GPU_POWER_Sequence

Pegatron Corp. Engineer: WJ

Size	Project Name	Rev
C	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 67 of 96

DC-IN connector

N : Iin = 130W / 19.5V
= 6.667A

Modified on 7/12
EMI resolution
Follow Vulcan, remove all MLCC and TVS

Modified on 6/21
need to confirm with EE

Add 4 test point follow factory rule by 1/14

For 5X6 P-MOSFET
Rds,on = 4.1m ohm @ Vgs = 10V
Rd = 6.67^2*4.1m*1.4=255.3mW

For 3X3 N-MOSFET
Rds,on = 11.5m ohm @ Vgs = 10V
Rd = 6.67^2*11.5m*1.4=716.3mW

PSID Circuit

6/28 Change to BUS Pool

2018/11/05 X01 Change D6801 from 07T030000016 to 07X110251250 (follow Loki/Armani)

Modified on 6/19
need to confirm with EE

Battery Pack connector

2018/11/05 X01 Add for Battery damage EC issue (follow vulcan)

For 5X6 P-MOSFET
Rds,on = 4.1m ohm @ Vgs = 10V
Rd = 6.5^2*4.1m*1.4=242.5mW

For 3X3 N-MOSFET
Rds,on = 11.5m ohm @ Vgs = 10V
Rd = 6.5^2*11.5m*1.4=680mW

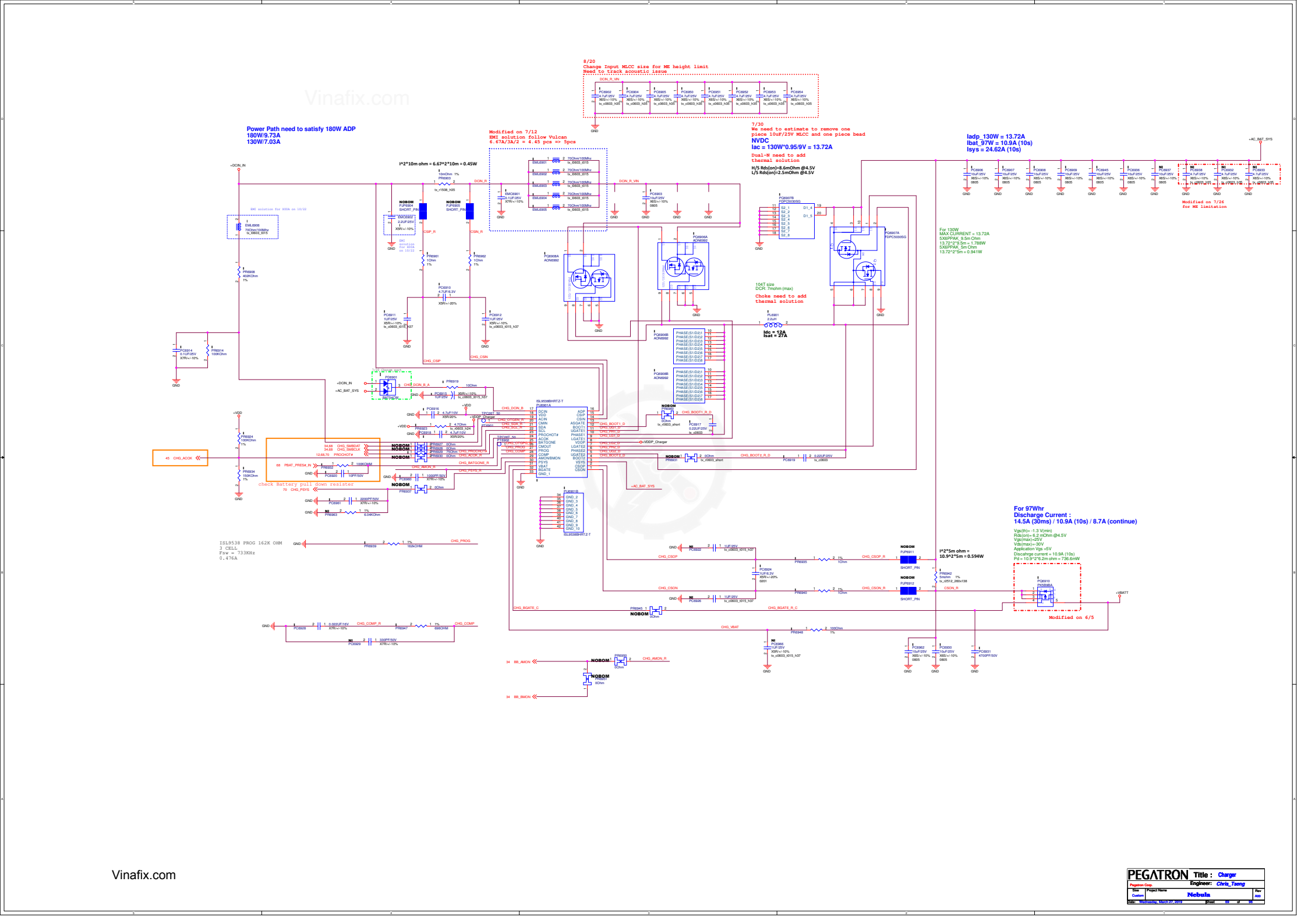
8/21 add one N-MOSFET
For single fault design

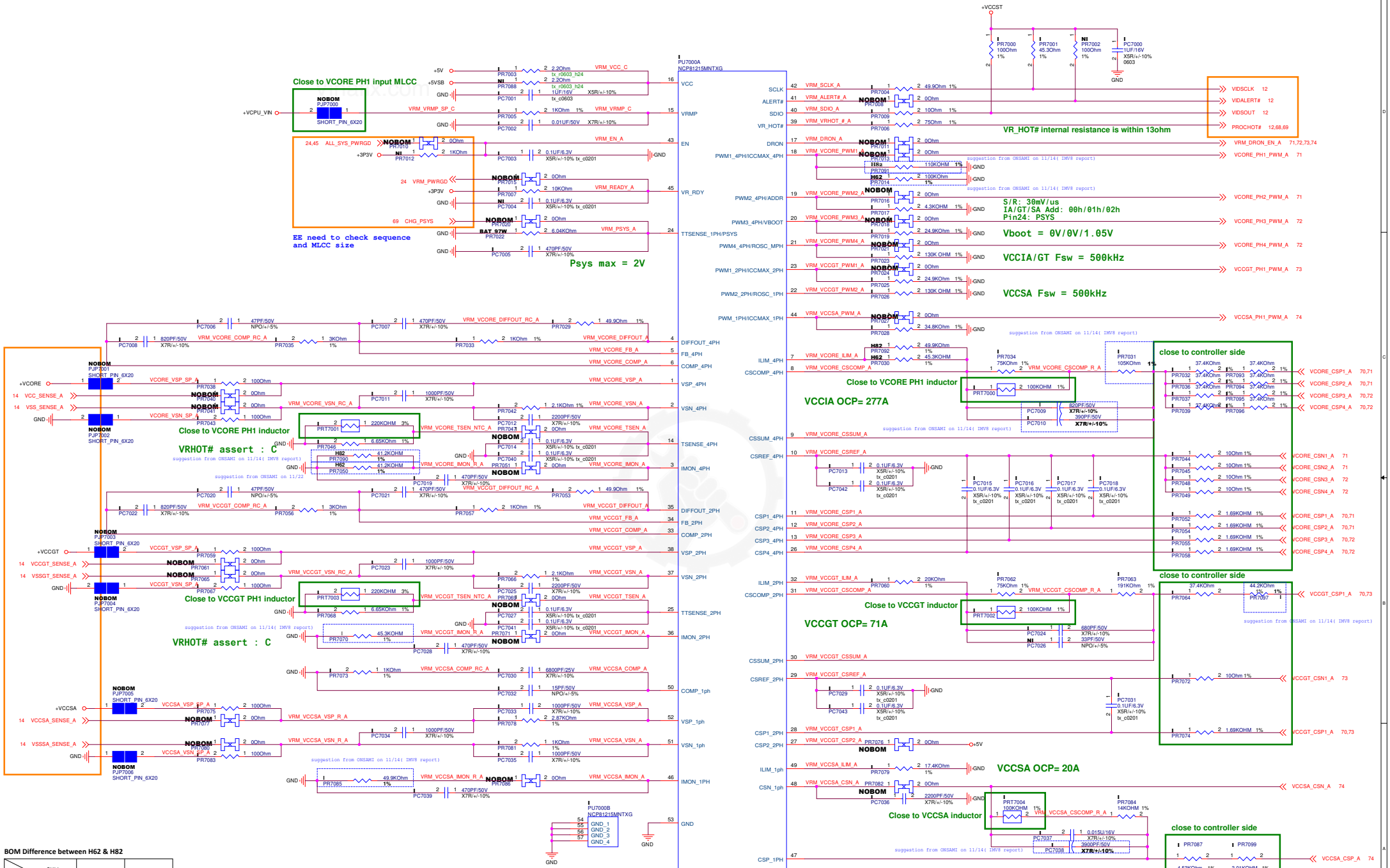
8/21 For height limit
to remove one source

Battery Protection Circuit

Adapter Protection Circuit

PEGATRON Corp.	Title : DC_IN
Size: Custom	Project Name: Nebula
Engineer: Chris_Tseng	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 68 of 96

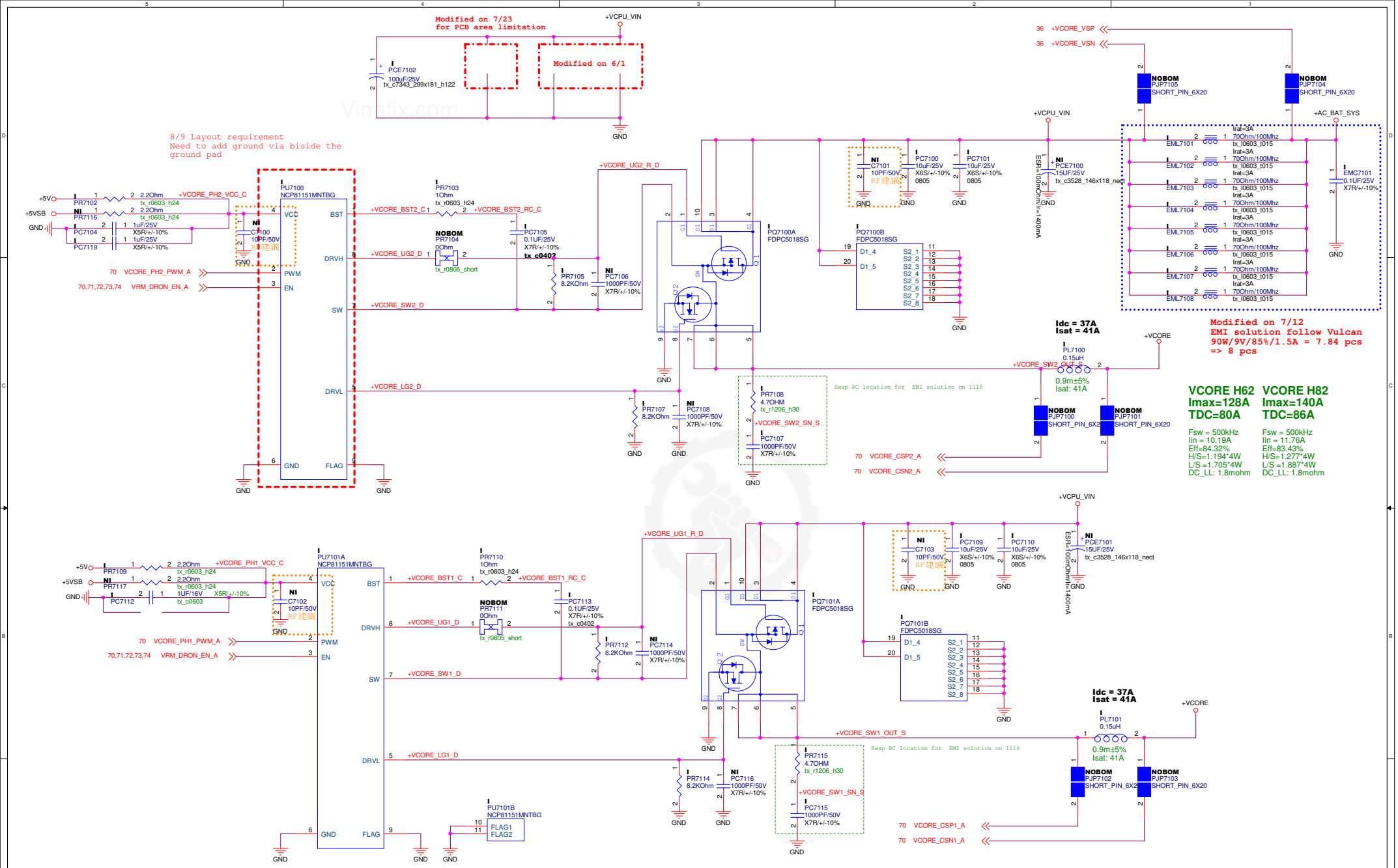

8/20
Change Input MLCC size for ME height limit
Need to track acoustic issue
Power Path need to satisfy 180W ADP
180W/9.73A
130W/7.03A
I^2*10m ohm = 6.67^2*10m = 0.45W
Modified on 7/12
EMI solution follow Vulcan
6.67A/3A/2 = 4.45 pcs => 5pcs
7/30
We need to estimate to remove one
piece 10uF/25V MLCC and one piece bead
NVDC
Iac = 130W*0.95/9V = 13.72A
Dual-N need to add
thermal solution
H/S Rds(on)=8.6mOhm @4.5V
L/S Rds(on)=2.5mOhm @4.5V
Iadp_130W = 13.72A
Ibat_97W = 10.9A (10s)
Isys = 24.62A (10s)
Modified on 7/26
for ME limitation
For 130W
MAX.CURRENT = 13.72A
5XEPPAK_9.5m Ohm
13.72^2*9.5m = 1.788W
5XEPPAK_5m Ohm
13.72^2*5m = 0.941W
104T size
DCR: 7mohm (max)
Choke need to add
thermal solution
Idc = 12A
Isat = 27A
I^2*5m ohm =
10.9^2*5m = 0.594W
For 97Whr
Discharge Current :
14.5A (30ms) / 10.9A (10s) / 8.7A (continue)
Vgs(th)= -1.3 V(min)
Rds(on)= 6.2 mOhm @4.5V
Vgs(max)=25V
Vds(max)= -30V
Application Vgs =5V
Discahrge current = 10.9A (10s)
Pd = 10.9^2*6.2m ohm = 736.6mW
Modified on 6/5
check Battery pull down resister
ISL9538 PROG 162K OHM
3 CELL
Fsw = 733KHz
0.476A
Vinafix.com
PEGATRON
Title : Charger
Engineer: Chris_Tseng
Nebula
Wednesday, March 27, 2013



BOM Difference between H62 & H82

SKU / Part Reference	H62	H82
PR7050 / PR7090	30.1KΩ	41.2KΩ
PR7014 / PR7091	100KΩ	100KΩ
PR7030 / PR7092	45.3KΩ (OCP = 252A)	45.3KΩ (OCP = 277A)

PEGATRON Title : VR CONTROLLER
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Nebula | Rev: A00
Date: Wednesday, March 27, 2019 | Sheet 70 of 96



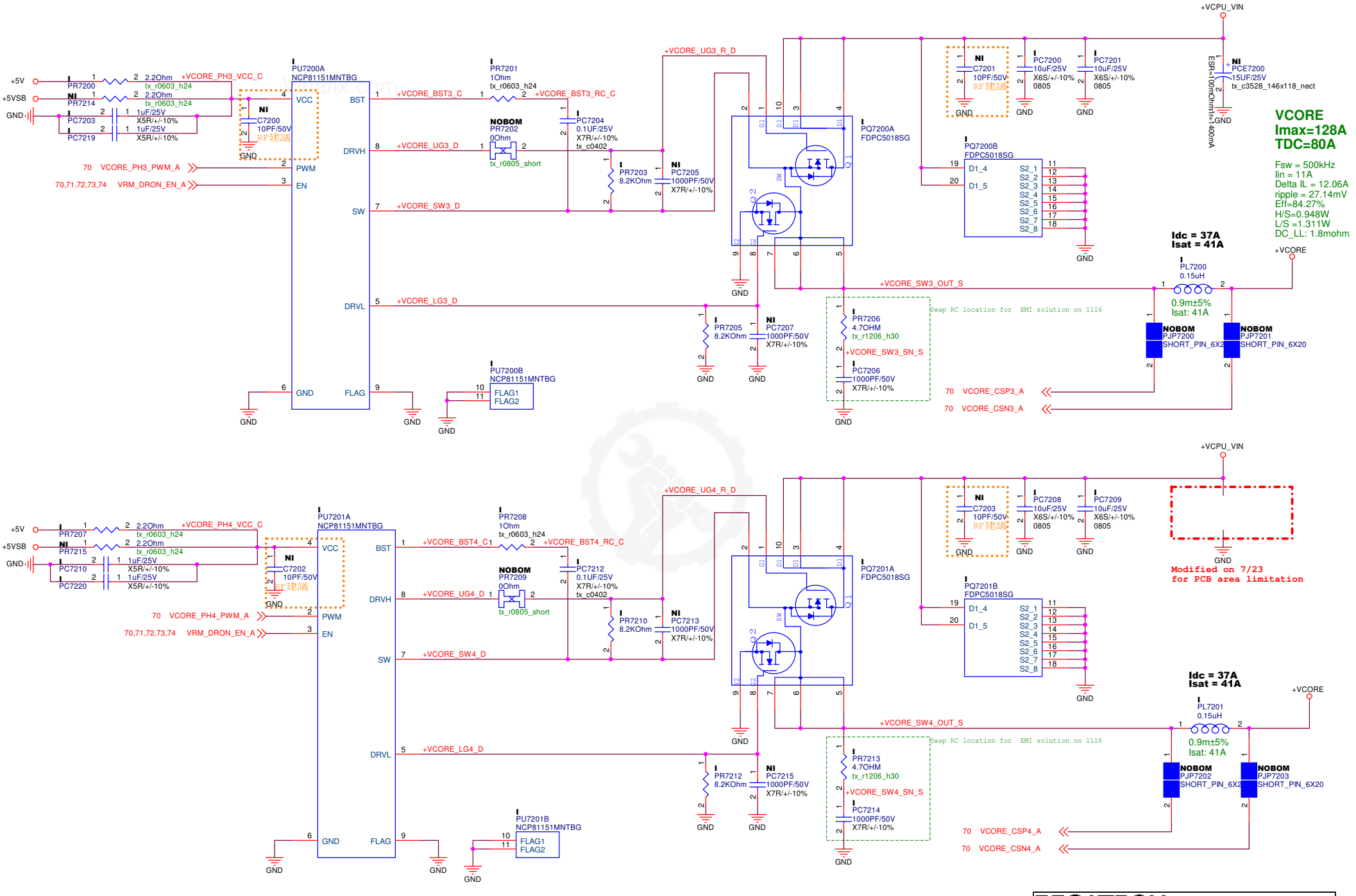
OWNER	+VCORE OC Point	Low Limit	High Limit
	167.94A -- 100% 251.91A -- 150%	78.44A	L= 0.08uH @ 80A (Per Choke)
	167.94A -- 100% 251.91A -- 150%	78.44A	L= 0.08uH @ 80A (Per Choke)

I_Low Limit = I_DVID + Io_Cout
= 26A + (30mV/uS) * 1748uF
= 78.44A

※ Controller will shut down after 50uS when 184.99A ≦ Iout < 277.49A
Controller will shut down immediately when Iout trigger 277.49A

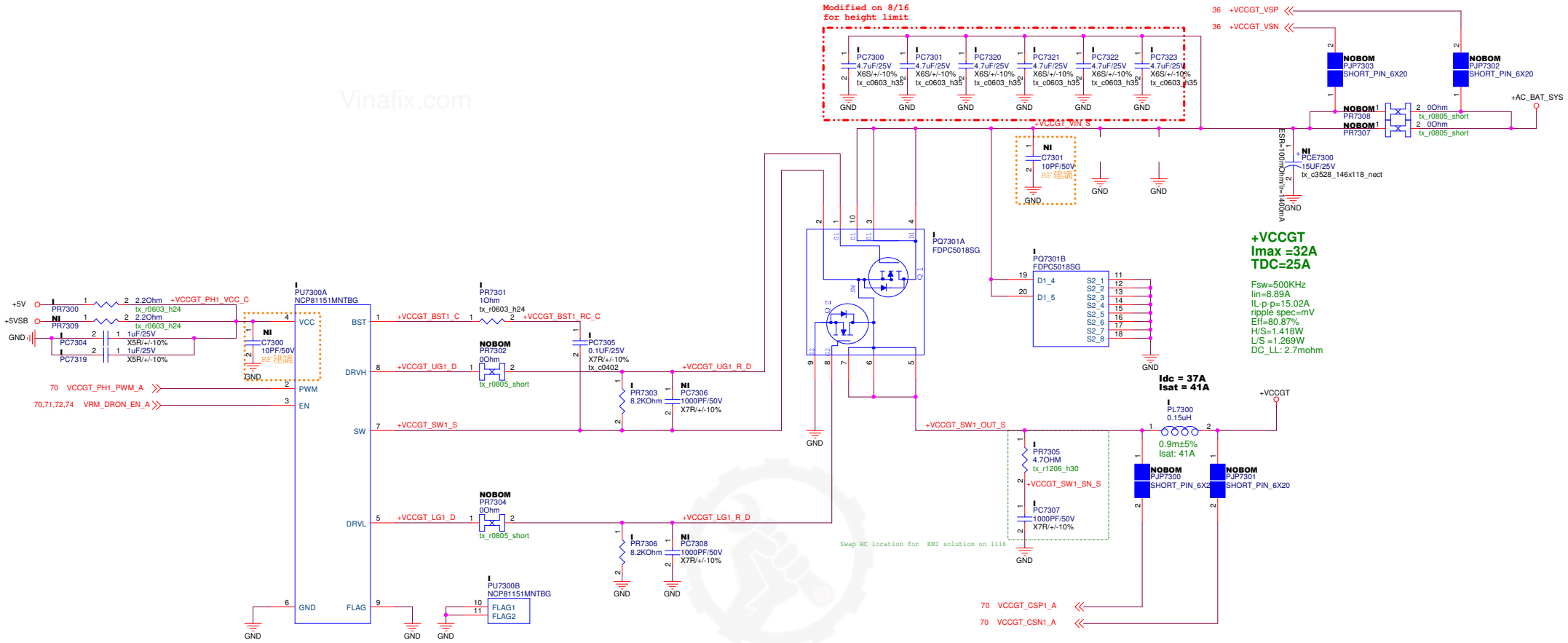
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : Vcore Driver-1
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Nebula | Rev: A00
Date: Wednesday, March 27, 2019 | Sheet 71 of 98



Vinafix.com

PEGATRON	Title : Vcore Driver-2	
Pegatron Corp.	Engineer: Chris_Tseng	
Size: Custom	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 72 of 96	



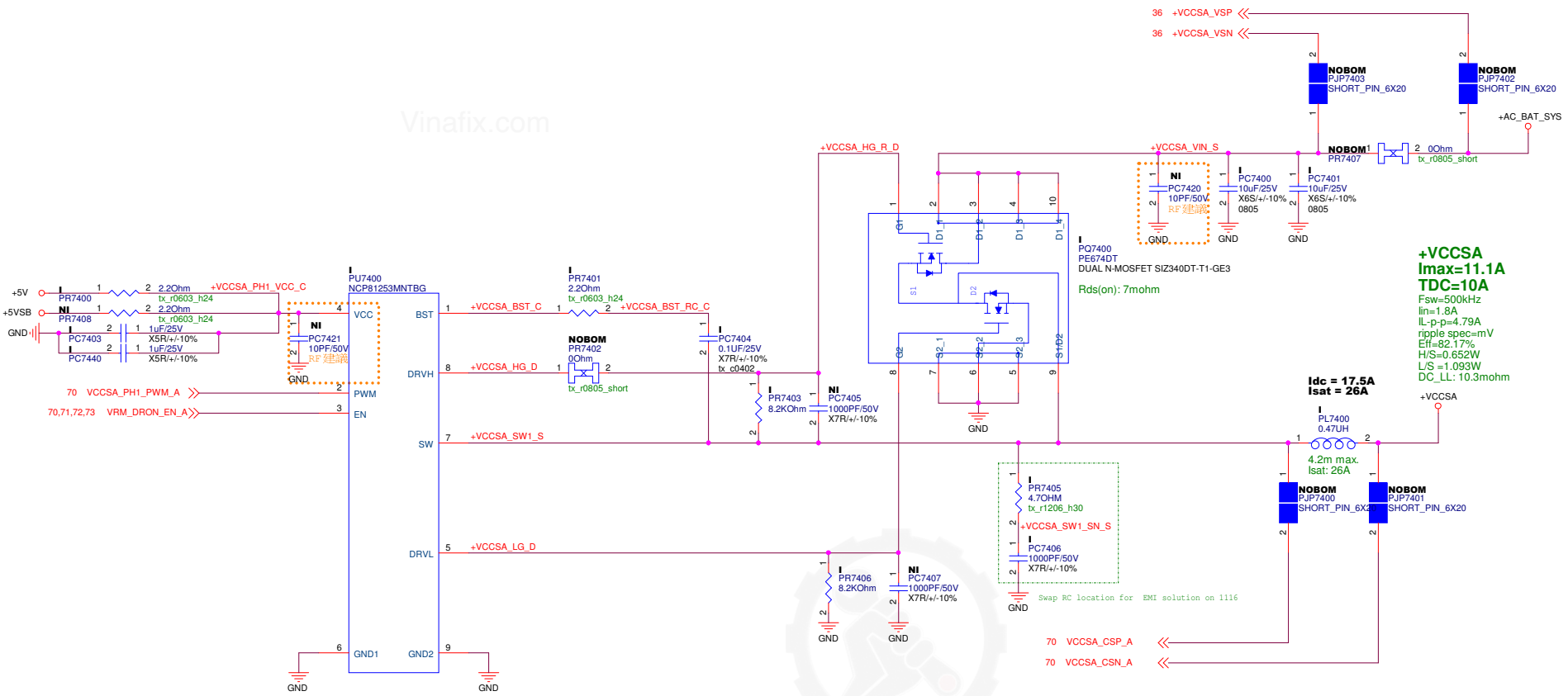
OWNER	+VCCGT OC Point	Low Limit	High Limit
	47.51A -- 100% 71.27A -- 150%	42.68A	L= 0.08uH @ 80A
	47.51A -- 100% 71.27A -- 150%	42.68A	L= 0.08uH @ 80A

I_Low Limit = I_DVID + Io_Cout
= 8A + (30mV/uS) * 1156uF
= 42.68A

※ Controller will shut down after 50uS when 47.51A ≦ Iout < 71.27A
~~Controller will shut down immediately when Iout trigger 71.27A~~

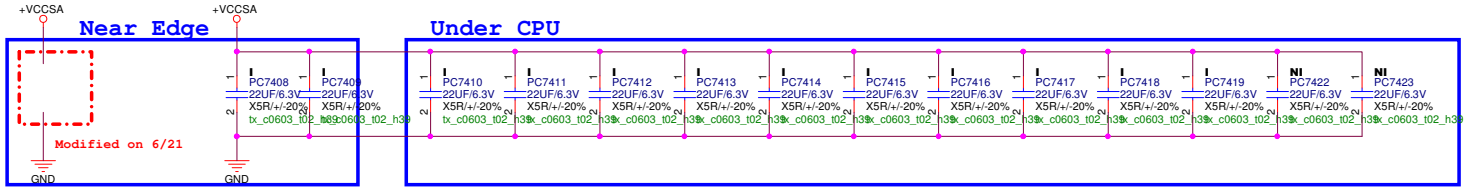
PEGATRON DT-MB RESTRICTED SECRET

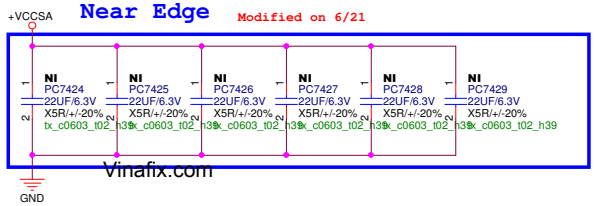
PEGATRON Title : VccGT Driver
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Nebula | Rev: A00
Date: Wednesday, March 27, 2019 | Sheet 73 of 96



OWNER	+VCCSA OC Point	Low Limit	High Limit
	18.96A @ DCR=4.2mΩ (Worst) 19.91A @ DCR=4mΩ (Typ.)	12.95A	L= 0.3uH @ 27A
	18.96A @ DCR=4.2mΩ (Worst) 19.91A @ DCR=4mΩ (Typ.)	12.95A	L= 0.3uH @ 27A

I_Low Limit = I_DVID + Io_Cout
= 5A + (30mV/uS) * 265uF
= 12.95A



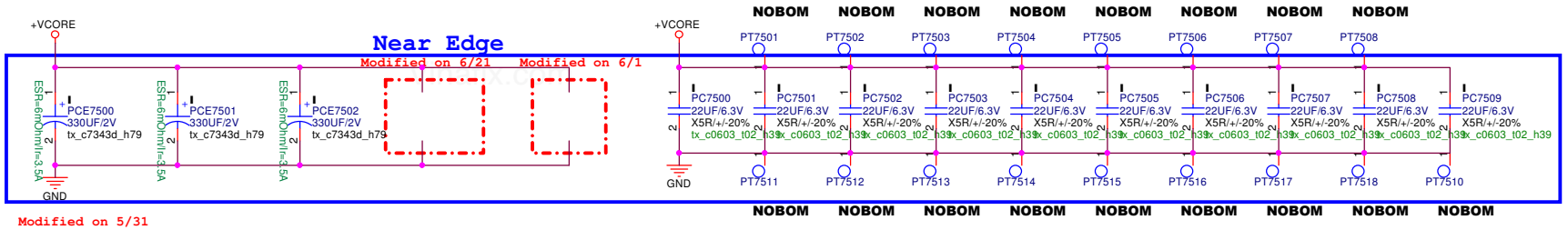


VCCSA Output CAP

22uF/6.3V * 12 (I)
22uF/6.3V * 8 (NI)

PEGATRON DT-MB RESTRICTED SECRET

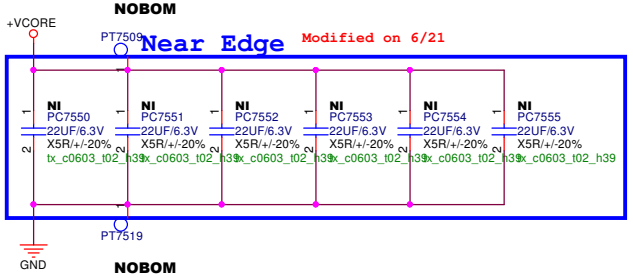
PEGATRON	Title : VccSA Driver	
Pegatron Corp.	Engineer: Chris_Tseng	
Size: Custom	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 74 of 96	

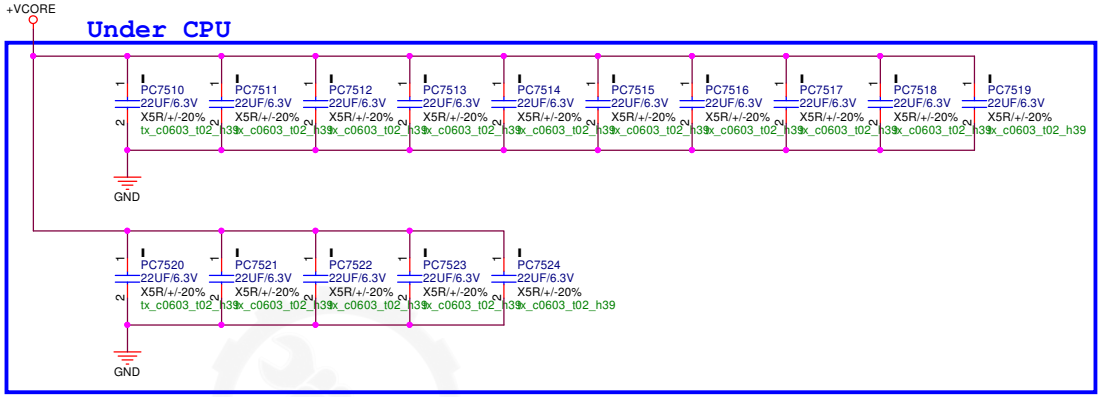


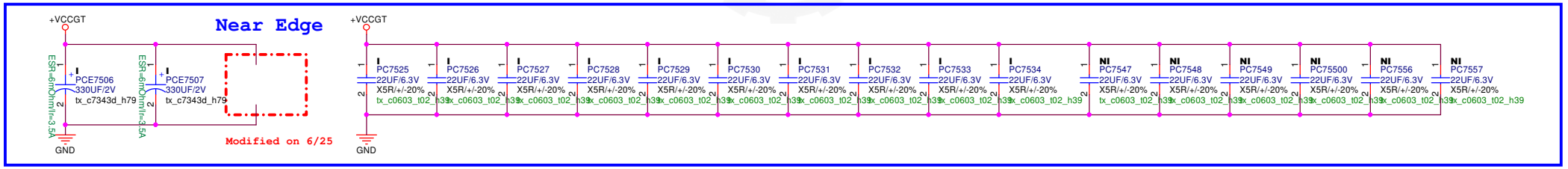
Modified on 5/31

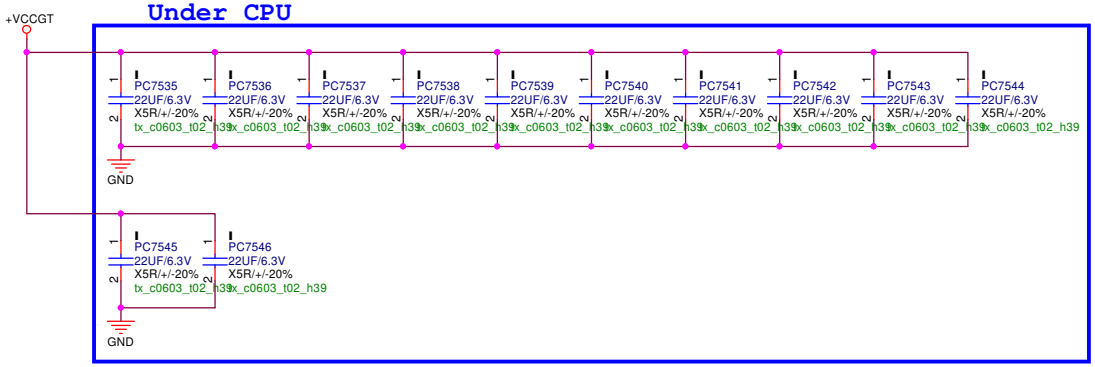
Vcore Output CAP

330uF/2V/H=2mm * 3 (I)
22uF * 25 (I)
22uF * 6 (NI)







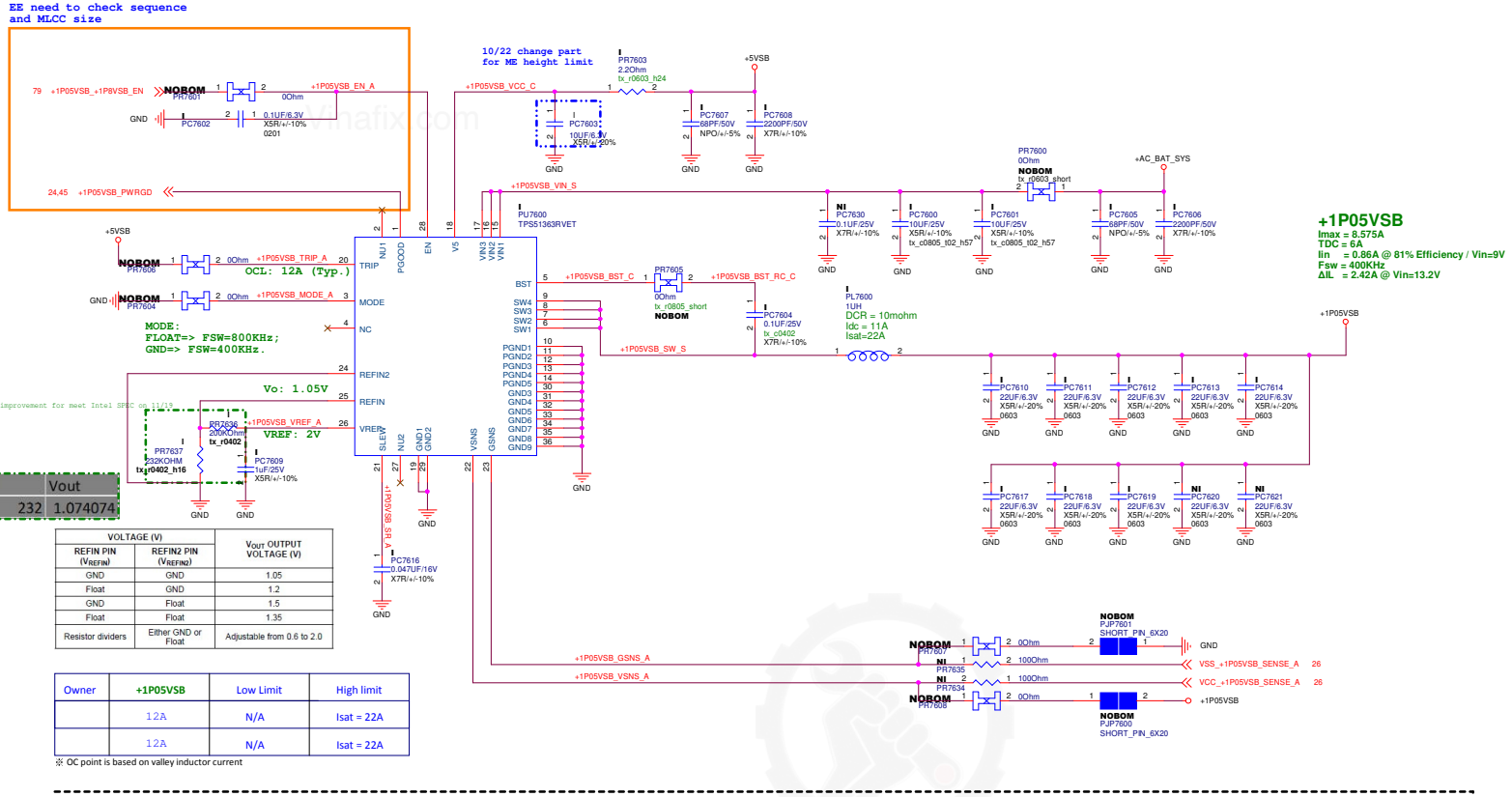


VCCGT Output CAP

330uF/2V/H=2mm * 2 (I)
22uF * 22 (I)
22uF * 6 (NI)

Vinafix.com

PEGATRON	Title :	Vcore & VccGT CAP
Pegatron Corp.	Engineer:	Chris_Tseng
Size: Custom	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 75 of 96	



Vref	R1	R2	Vout
2	200	232	1.074074

VOLTAGE (V)		
REFIN PIN (V_{REFIN})	REFIN2 PIN (V_{REFIN2})	V_{OUT} OUTPUT VOLTAGE (V)
GND	GND	1.05
Float	GND	1.2
GND	Float	1.5
Float	Float	1.35
Resistor dividers	Either GND or Float	Adjustable from 0.6 to 2.0

Owner	+1P05VSB	Low Limit	High limit
	12A	N/A	Isat = 22A
	12A	N/A	Isat = 22A

※ OC point is based on valley inductor current

Owner	+2P5V_VPP	Low Limit	High limit
	4.0A	N/A	0.66uH @ 6A
	4.0A	N/A	0.66uH @ 6A

※ OC point is based on peak inductor current

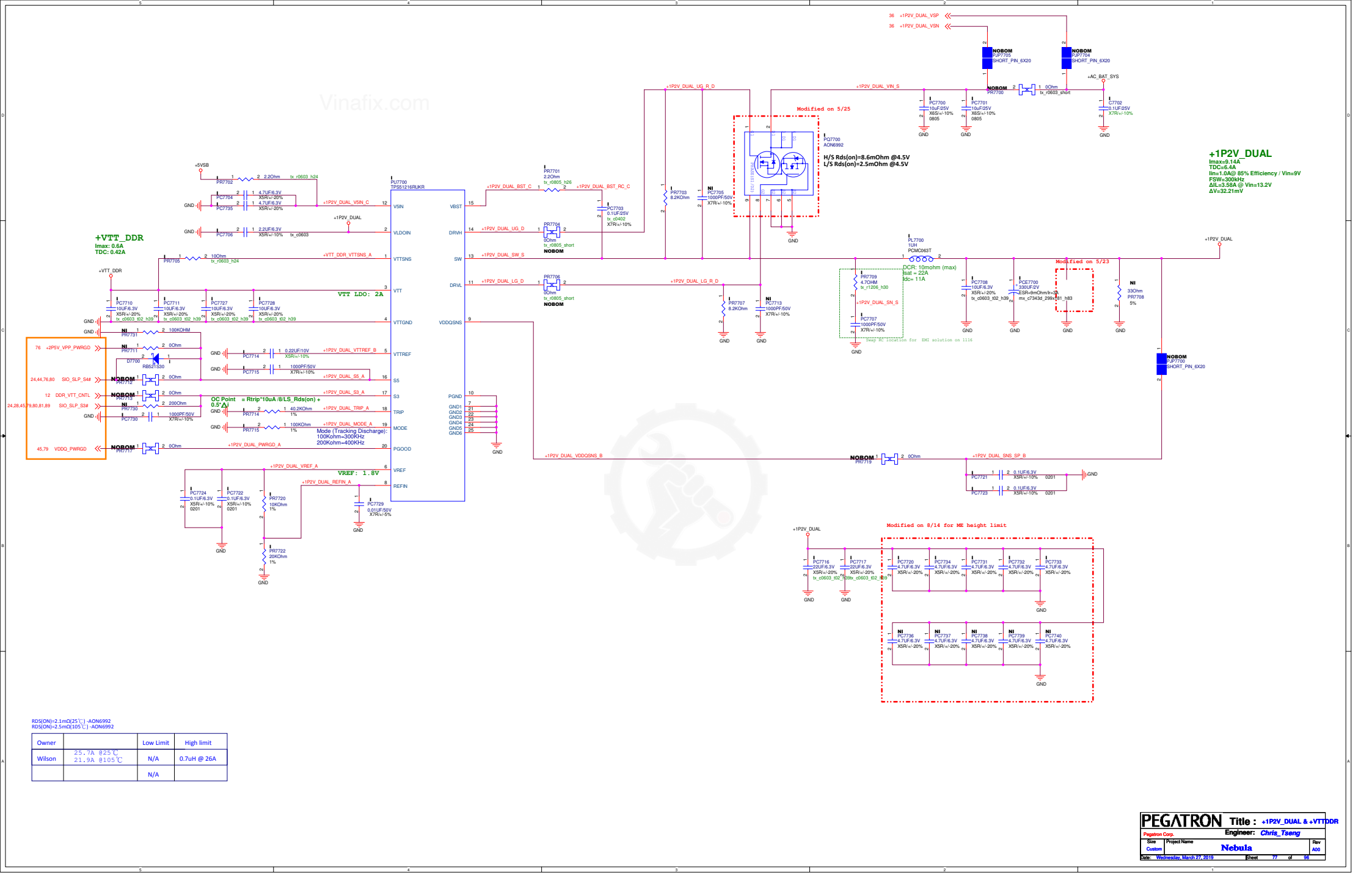
PEGATRON DT-MB RESTRICTED SECRET

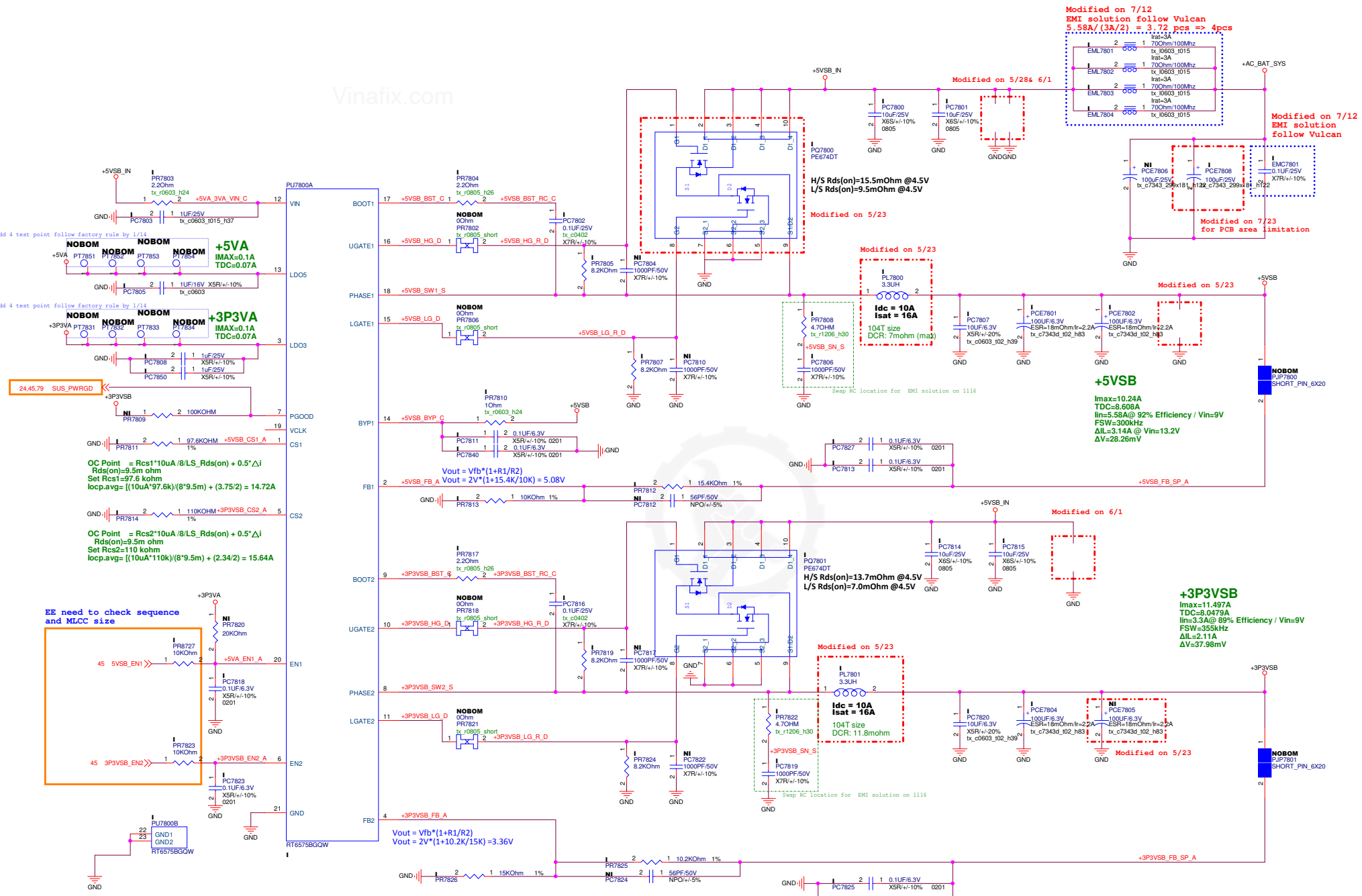
PEGATRON Title : +1P05VSB/+2P5VPP

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 76 of 98


+1P2V_DUAL
Imax=9.14A
TDC=6.4A
Iin=1.0A@ 85% Efficiency / Vin=9V
FSW=300kHz
ΔIL=3.58A @ Vin=13.2V
ΔV=32.21mV
+VTT_DDR
Imax: 0.6A
TDC: 0.42A
VTT LDO: 2A
VREF: 1.8V
H/S Rds(on)=8.6mOhm @4.5V
L/S Rds(on)=2.5mOhm @4.5V
Modified on 5/25
Modified on 5/23
Modified on 8/14 for ME height limit
DCR: 10mohm (max)
Isat = 22A
Idc= 11A
OC Point = Rtrip*10uA /8/LS_Rds(on) + 0.5*ΔI
Mode (Tracking Discharge):
100Kohm=300KHz
200Kohm=400KHz
PU7700
TPS51216RLKR
PQ7700
AON6992
PL7700
1UH
PCMC063T
+5VSB
+AC_BAT_SYS
+1P2V_DUAL_VSP
+1P2V_DUAL_VSN
+1P2V_DUAL_VIN_S
+1P2V_DUAL_UG_R_D
+1P2V_DUAL_BST_C
+1P2V_DUAL_BST_RC_C
+1P2V_DUAL_SW_S
+1P2V_DUAL_LG_D
+1P2V_DUAL_LG_R_D
+1P2V_DUAL_SN_S
+1P2V_DUAL_VDDQSNS_B
+1P2V_DUAL_SNS_SP_B
+1P2V_DUAL_VSN_C
+1P2V_DUAL_VTTREF_B
+1P2V_DUAL_S5_A
+1P2V_DUAL_S3_A
+1P2V_DUAL_TRIP_A
+1P2V_DUAL_MODE_A
+1P2V_DUAL_PWRGD_A
+1P2V_DUAL_VREF_A
+1P2V_DUAL_REFIN_A
+VTT_DDR_VTTSNS_A
+VTT_DDR
+2P5V_VPP_PWRGD
SIO_SLP_S4#
DDR_VTT_CNTL
SIO_SLP_S3#
VDDQ_PWRGD
VIN
VLDOIN
VTTSNS
VTT
VTTGND
VTTREF
S5
S3
TRIP
MODE
PGOOD
VREF
REFIN
VBST
DRVH
SW
DRVL
VDDQSNS
PGND
NOBOM
SHORT_PIN_6X20
Swap PC location for EMI solution on 1116
RDS(ON)=2.1mΩ(25℃) -AON6992
RDS(ON)=2.5mΩ(105℃) -AON6992
Owner
Low Limit
High limit
Wilson
25.7A @25℃
21.9A @105℃
N/A
0.7uH @ 26A
PEGATRON
Title : +1P2V_DUAL & +VTTDDR
Pegatron Corp.
Engineer: Chris_Tseng
Size: Custom
Project Name: Nebula
Rev: A00
Date: Wednesday, March 27, 2019
Sheet 77 of 96



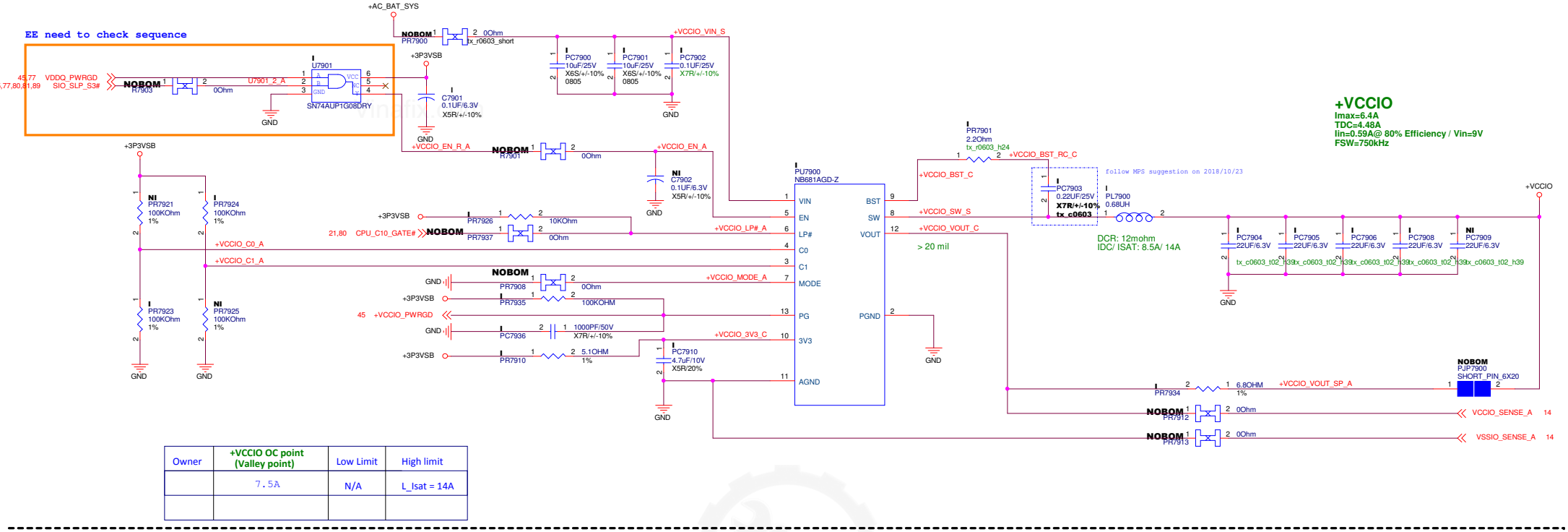
RDS(ON)=7.0mΩ(25℃) -SIZ340DT-T1-GE3
RDS(ON)=9.8mΩ(25℃) -SIZ340DT-T1-GE3

Owner	+5VSB OC point	Low Limit	High limit
Wilson	18.21A @25℃ 12.84A @105℃	N/A	0.7uH @ 26A
		N/A	

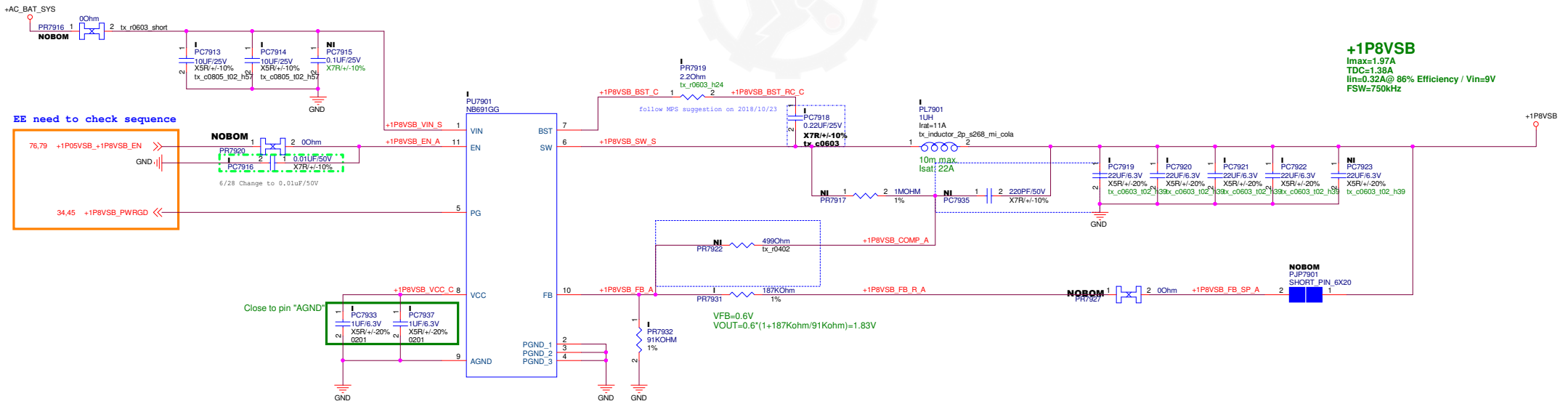
RDS(ON)=7.0mΩ(25℃) -SIZ340DT-T1-GE3
RDS(ON)=9.8mΩ(25℃) -SIZ340DT-T1-GE3

Owner	+3P3VSB OC point	Low Limit	High limit
Wilson	20.52A @25℃ 14.47A @105℃	N/A	0.7uH @ 26A
		N/A	

PEGATRON Title : +3P3VSB / +5VSB
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Nebula | Rev: A00
Date: Wednesday, March 27, 2019 Sheet 78 of 96

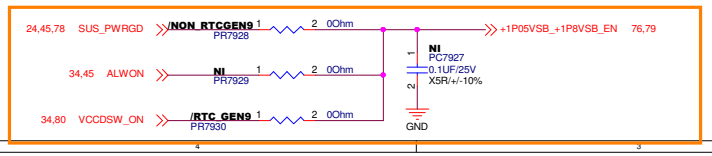


Owner	+VCCIO OC point (Valley point)	Low Limit	High limit
	7.5A	N/A	L_Isat = 14A



Owner	+VCCIO OC point (Valley point)	Low Limit	High limit
	7.5A	N/A	L_Isat = 22A
		N/A	

EE need to check sequence

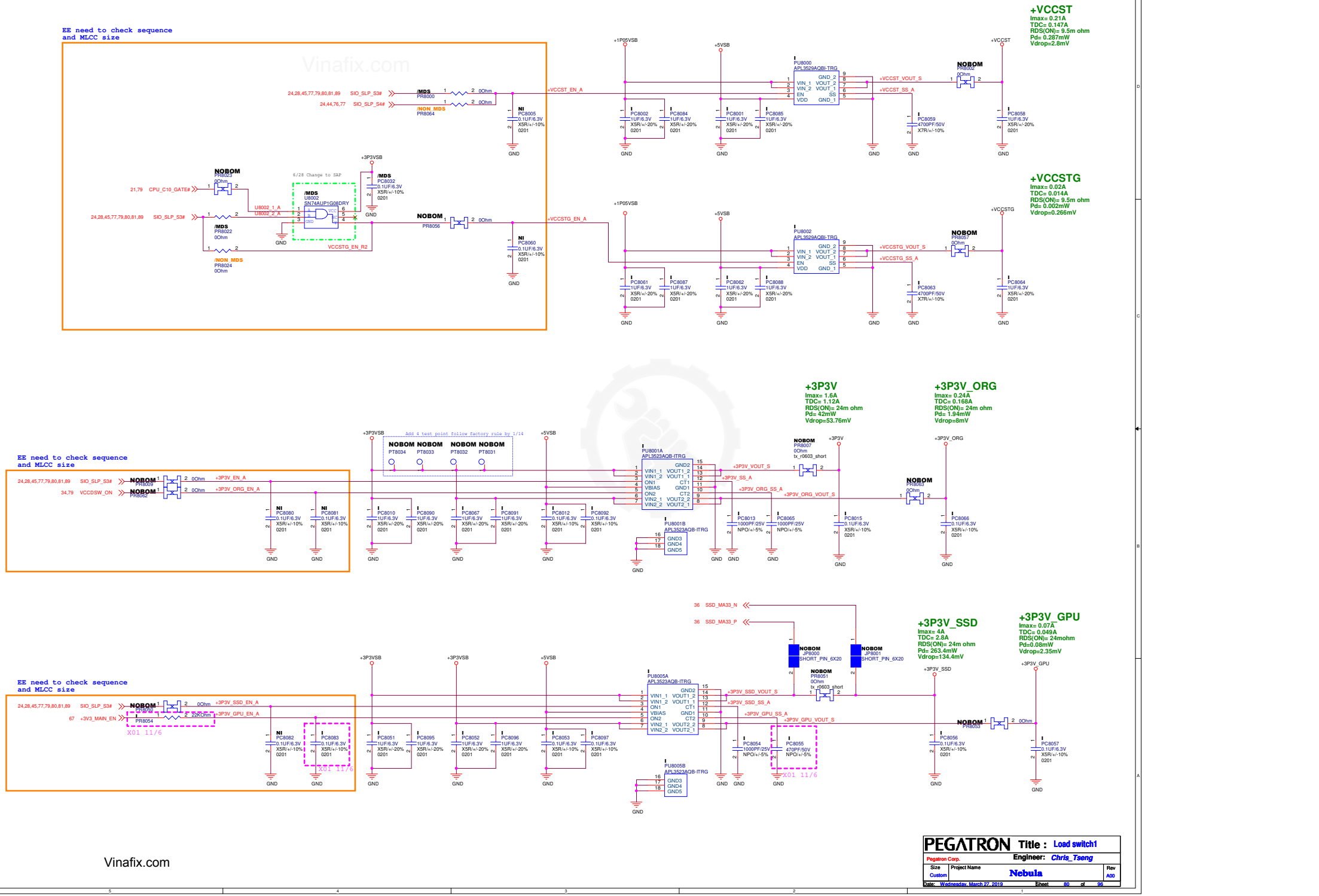


PEGATRON Title : 79.+VCCIO/ +1P8V

Pegatron Corp. Engineer: Chris_Tseng

Size	Project Name	Rev
Custom	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 79 of 96


EE need to check sequence and MLCC size
+VCCST
Imax= 0.21A
TDC= 0.147A
RDS(ON)= 9.5m ohm
Pd= 0.287mW
Vdrop=2.8mV
+VCCSTG
Imax= 0.02A
TDC= 0.014A
RDS(ON)= 9.5m ohm
Pd= 0.002mW
Vdrop=0.266mV
+3P3V
Imax= 1.6A
TDC= 1.12A
RDS(ON)= 24m ohm
Pd= 42mW
Vdrop=53.76mV
+3P3V_ORG
Imax= 0.24A
TDC= 0.168A
RDS(ON)= 24m ohm
Pd= 1.94mW
Vdrop=8mV
+3P3V_SSD
Imax= 4A
TDC= 2.8A
RDS(ON)= 24m ohm
Pd= 263.4mW
Vdrop=134.4mV
+3P3V_GPU
Imax= 0.07A
TDC= 0.049A
RDS(ON)= 24mohm
Pd=0.08mW
Vdrop=2.35mV
Vinafix.com
PEGATRON
Title : Load switch1
Engineer: Chris_Tseng
Pegatron Corp.
Size: Custom
Project Name: Nebula
Rev: A00
Date: Wednesday, March 27, 2019
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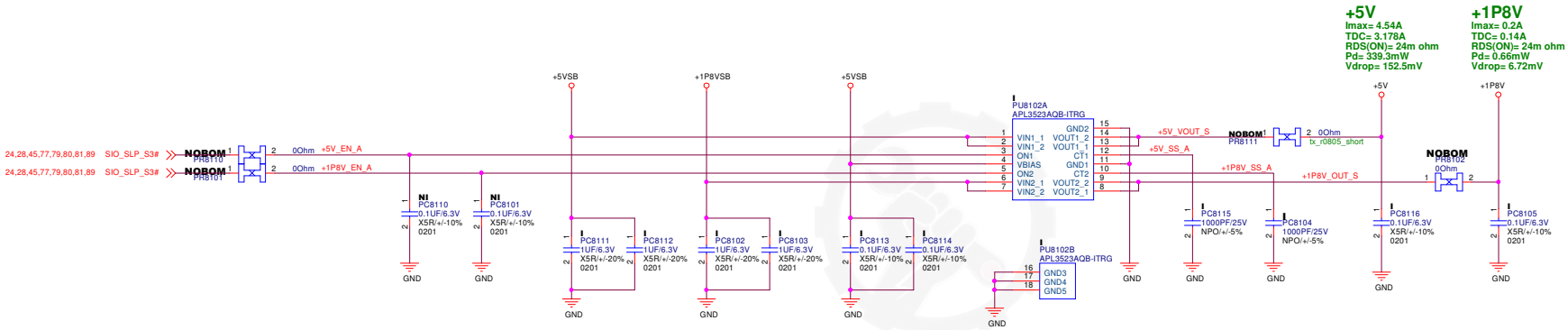
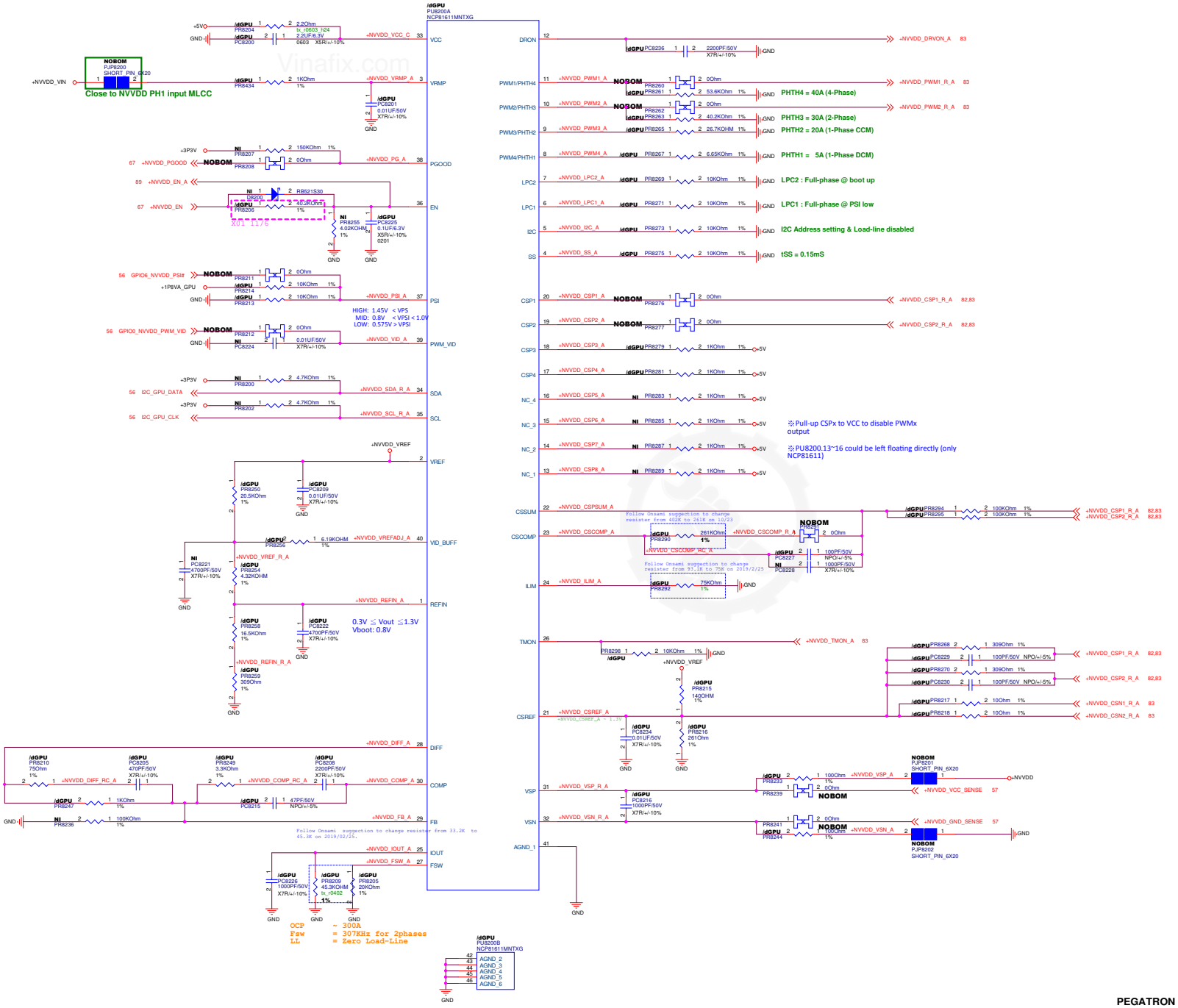


PEGATRON	Title :	Load switch2
Pegatron Corp.	Engineer:	Chris_Tseng
Size: Custom	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 81 of 96	



Vinafix.com

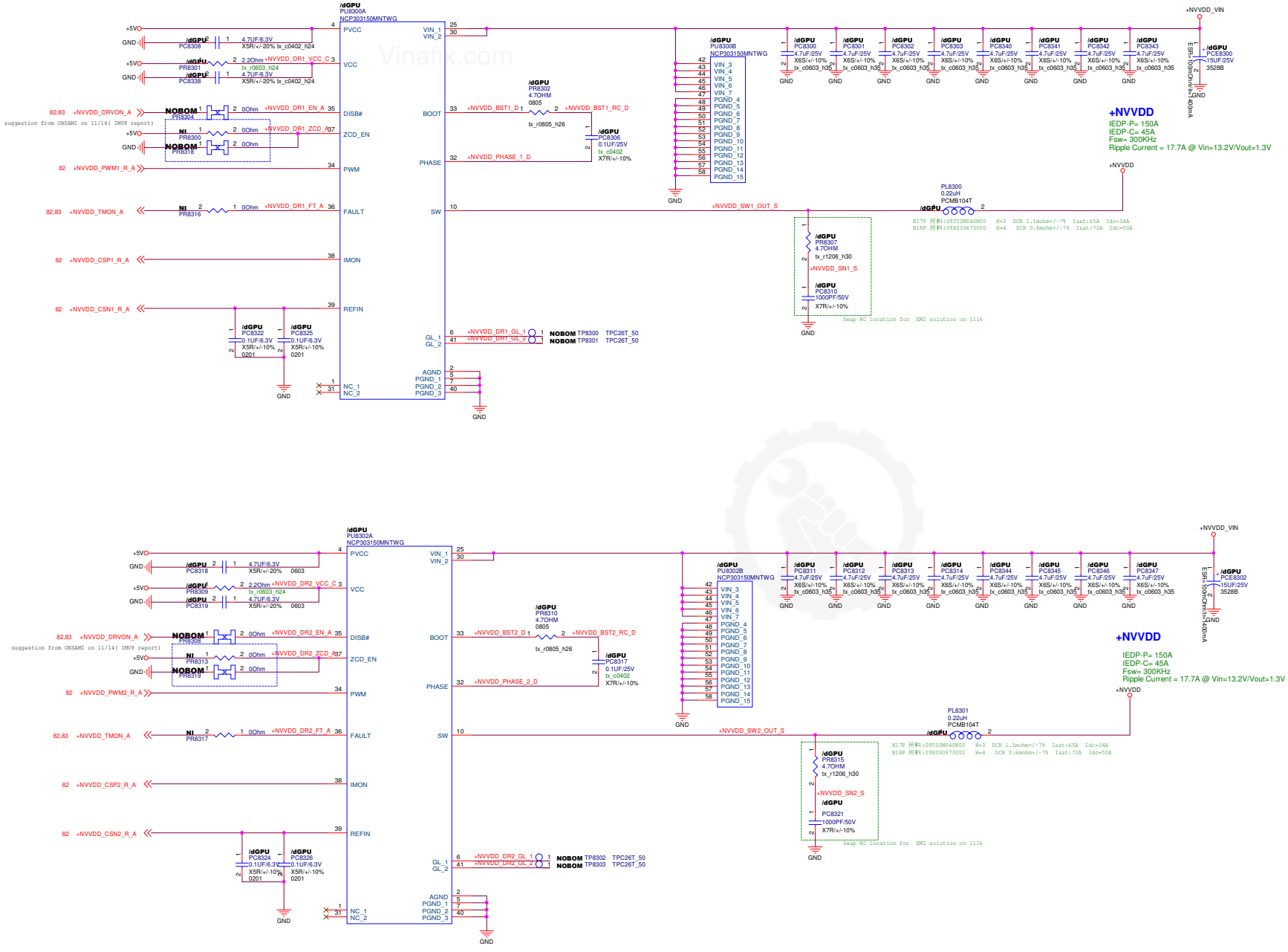
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +NVVDD Controller

Pegatron Corp. Engineer: Chris_Tseng

Size: Custom | Project Name: Nebula | Rev: A00

Date: Wednesday, March 27, 2019 | Sheet 82 of 96

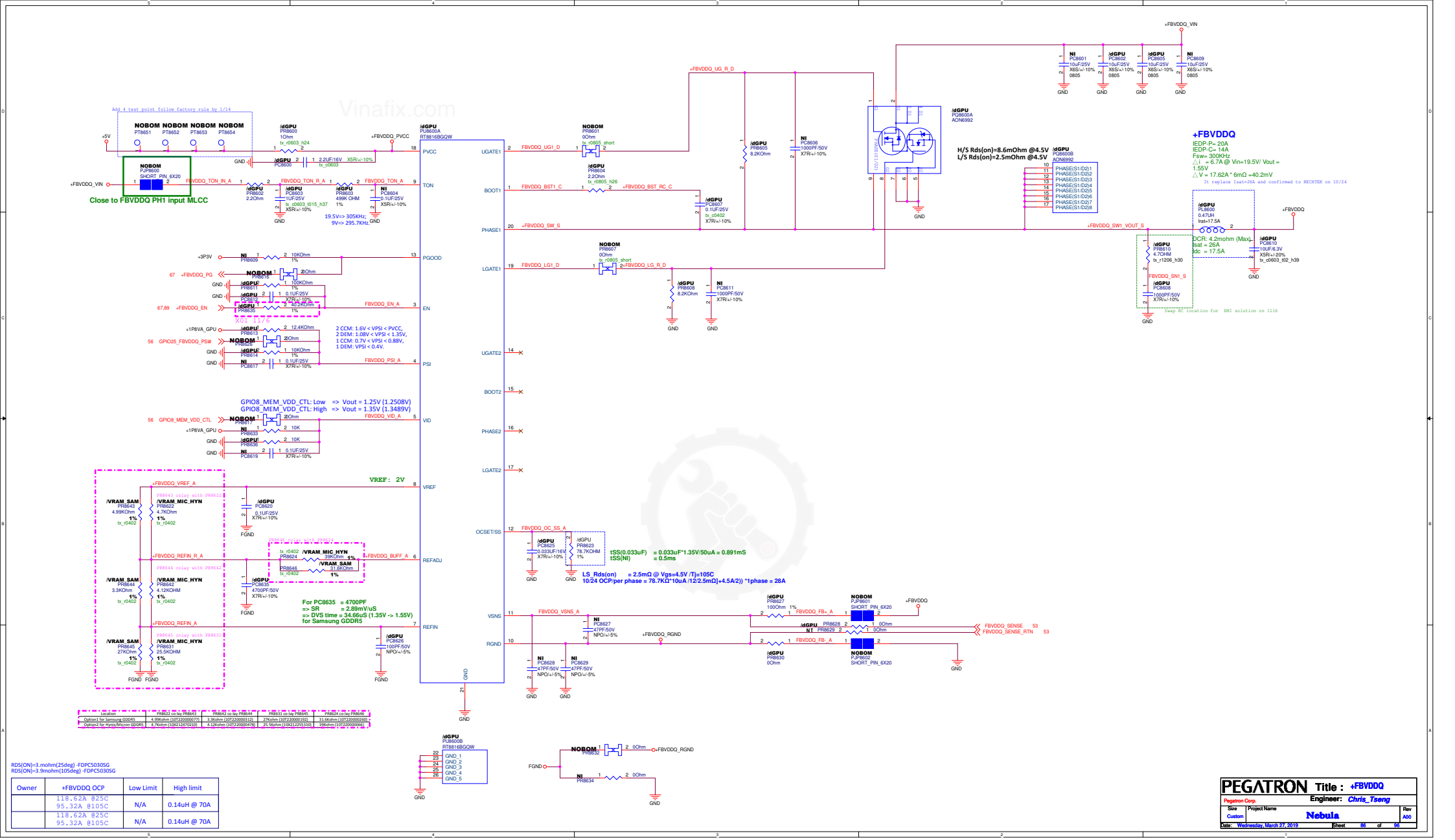


PEGATRON	Title : +NVDD Driver /Cap		
Pegatron Corp.	Engineer: Chris_Tseng		
Size: Custom	Project Name: Nebula		Rev: A00
Date: Wednesday, March 27, 2019	Sheet 83 of 96		

PEGATRON	Title : +NVVDD Driver-2	
Pegatron Corp.	Engineer: Chris_Tseng	
Size: Custom	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 84 of 98	

PEGATRON DT-MB RESTRICTED SECRET

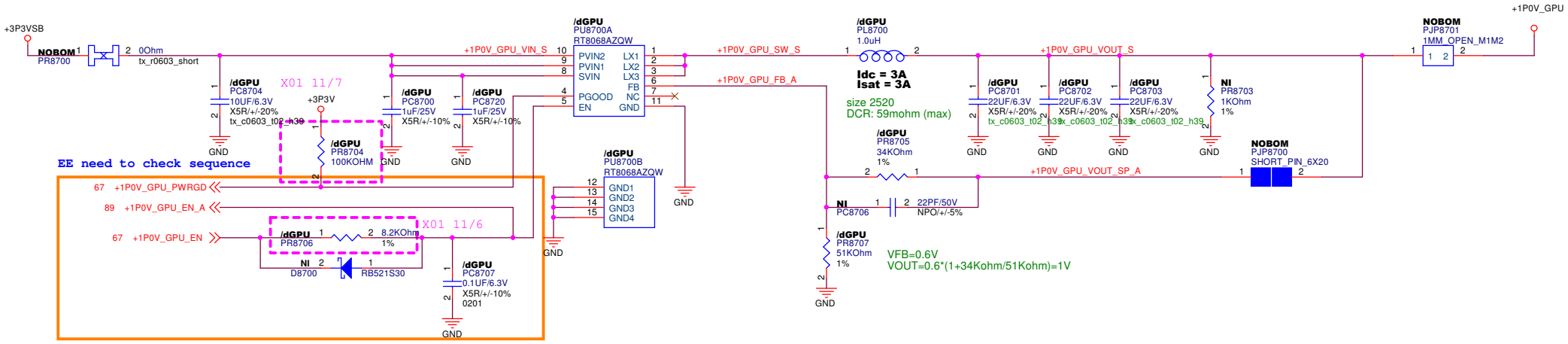
PEGATRON	Title : +NVVDD Driver-3		
Pegatron Corp.	Engineer: Chris_Tseng		
Size: C	Project Name: Nebula		Rev: A00
Date: Wednesday, March 27, 2019	Sheet 85 of 96		



Owner	+FBVDDQ OCP	Low Limit	High limit
	118.62A @25C 95.32A @105C	N/A	0.14uH @ 70A
	118.62A @25C 95.32A @105C	N/A	0.14uH @ 70A

+1P0V_GPU

Imax = 0.8A
TDC = 0.56A
Iin = 0.188A @ 90% Efficiency
Fsw = 1MHz
ΔIL = 0.697A
OCL=4A



Owner	+1P0V_GPU	Low Limit	High limit
	4.0A	N/A	0.44uH @ 6A
	4.0A	N/A	0.44uH @ 6A

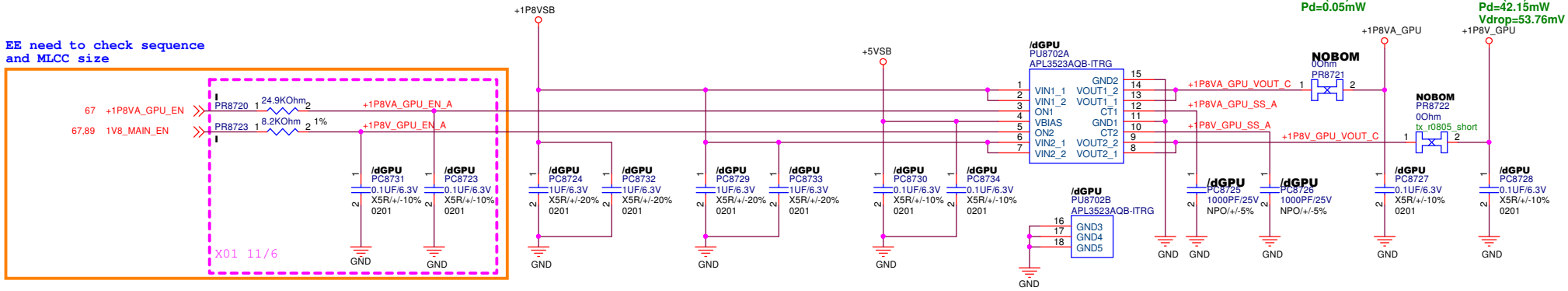
※ OC point is based on peak inductor current

+1P8VA_GPU

Imax= 0.06A
TDC= 0.042A
RDS(ON)= 24m ohm
Pd=0.05mW

+1P8V_GPU

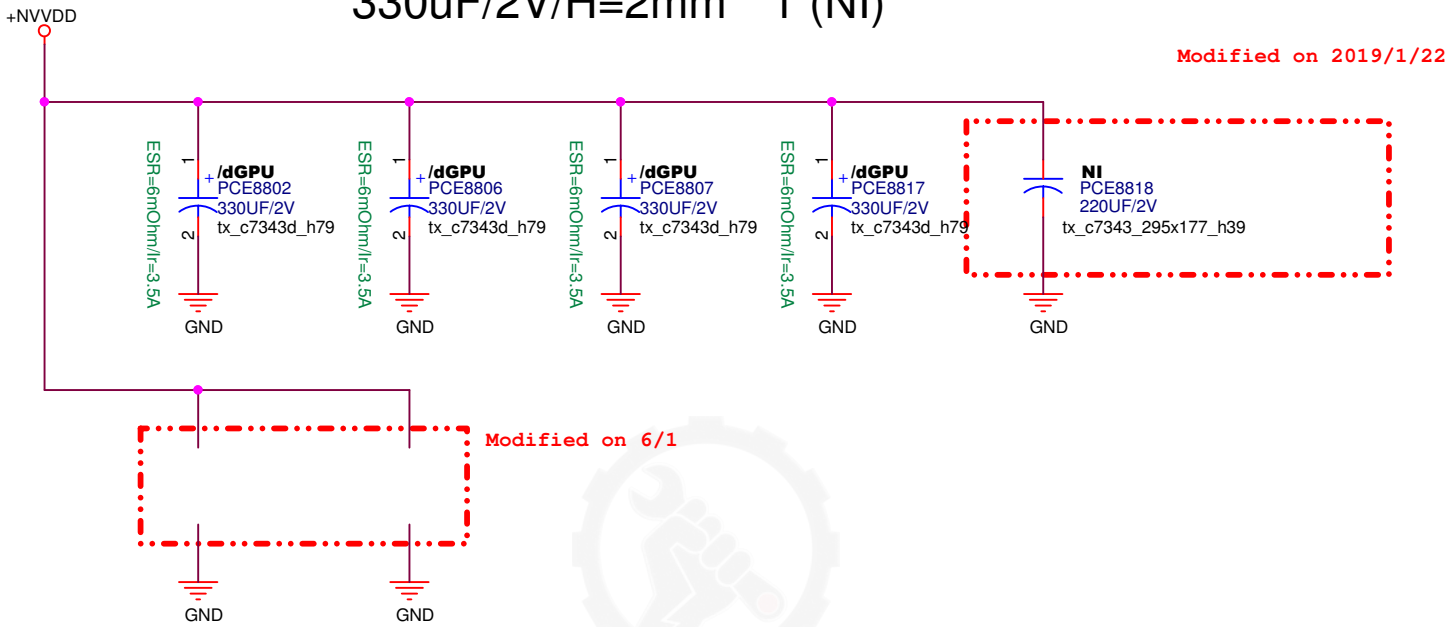
Imax= 1.6A
TDC= 1.12A
RDS(ON)= 24m ohm
Pd=42.15mV
Vdrop=53.76mV

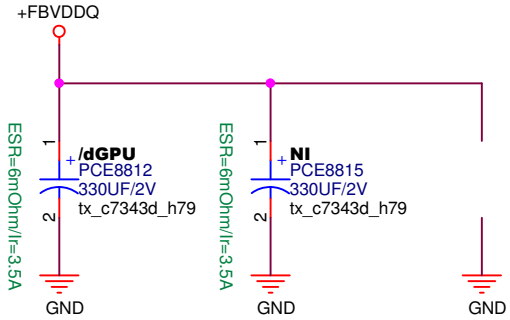


PEGATRON Title : +1P0V_GPU/+1P8V_GPU & LDO
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Nebula | Rev: A00
Date: Wednesday, March 27, 2019 Sheet 87 of 96

+NVVDD Output CAP(with +NVVDDS merged)

330uF/2V/H=2mm * 4 (I)
330uF/2V/H=2mm * 1 (NI)





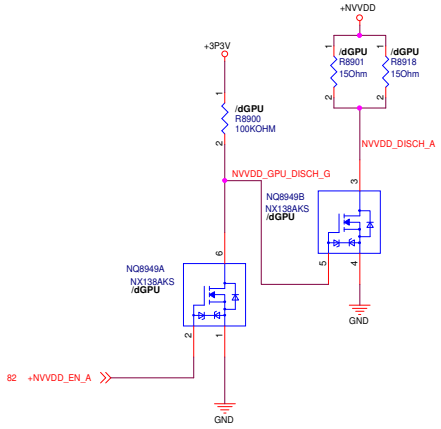
+FBVDDQ Output CAP

330uF/2V/H=2mm * 1 (I)
330uF/2V/H=2mm * 1 (NI)

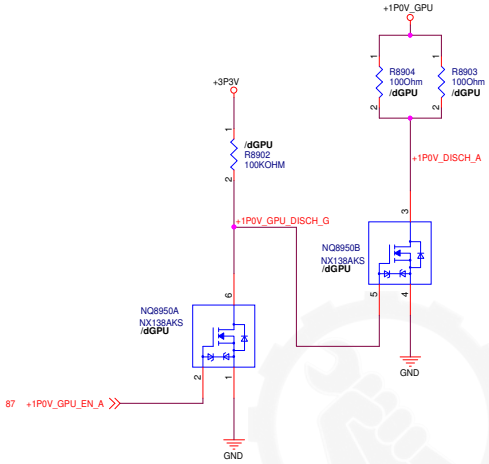
PEGATRON	Title : GPU_POWER_CAP	
Pegatron Corp.	Engineer: Chris_Tseng	
Size: Custom	Project Name: Nebula	Rev: A00
Date: Wednesday, March 27, 2019	Sheet 88 of 96	

GPU POWER DISCHARGE

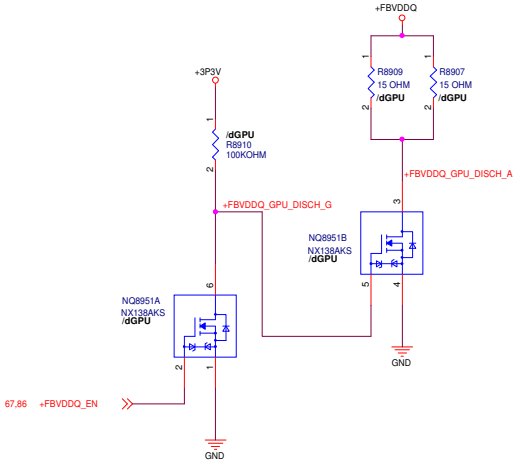
NVVDD DISCHARGE



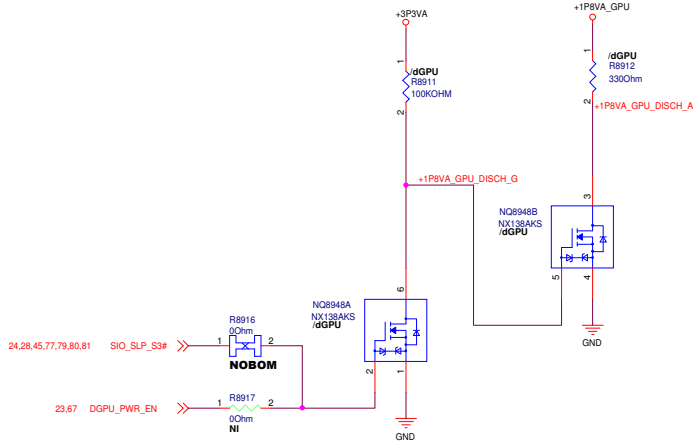
1P0V DISCHARGE



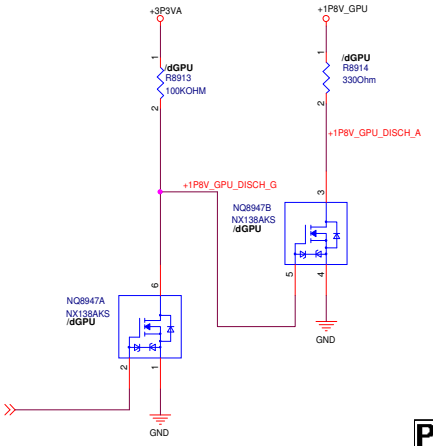
FBVDDQ DISCHARGE



1P8VA_GPU DISCHARGE



1P8V_GPU DISCHARGE



PEGATRON Title : GPU_POWER_DISCHARGE

Pegatron Corp. Engineer: WJ

Size	Project Name	Rev
C	Nebula	A00

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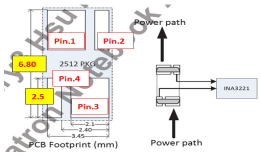


*AC_BAT_SYS (GPU power only)

Input Current: 12A @19V (1ms moving average)
Input Current: 10A @19V (5ms moving average)
Input Current : 4.21A @19V (1s movingi average)

Input Current: 25.33A @9V (1ms moving average)
Input Current: 21.11A @9V (5ms moving average)
Input Current : 8.89A @9V (1s movingi average)

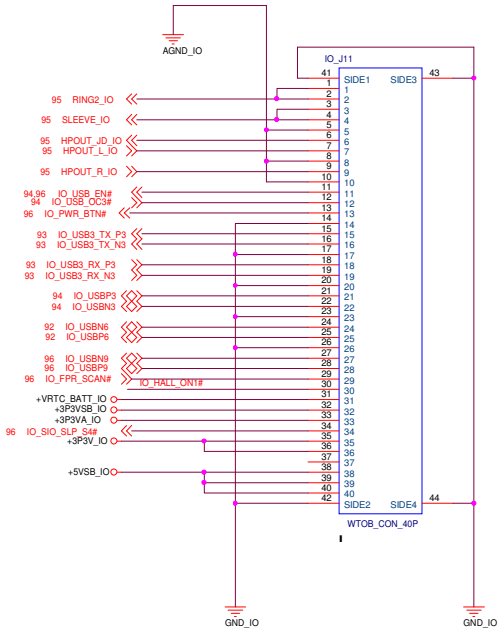
Option for PU9001

PU9001	PR9030	PR9024/PR9028	PR9023/PR9027/PR9048
0689-001W000	10T220000440	10T220000439	10T220000349
ONSAMI	243K ohm	475 ohm	649 ohm
0689-001X000	10T220418V00	10T220000281	10X221426000
UPI	324K ohm	357 ohm	487 ohm

PEGATRON Title : Power sense
Pegatron Corp. Engineer: Chris_Tseng
Size: Custom | Project Name: Nebula | Rev: A00
Date: Wednesday, March 27, 2019 | Sheet 90 of 98

A01 IO CONN & Hall Sensor

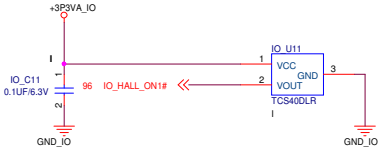
IO Connector

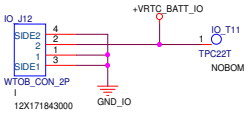


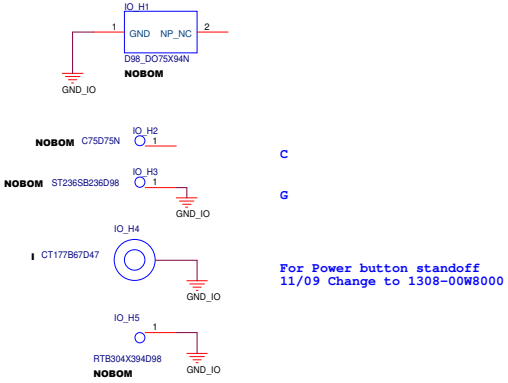
IO Connector Pin Define

1	RING2_IO	21	IO_USBP3
2	RING2_IO	22	IO_USBN3
3	SLEEVE_IO	23	GND_IO
4	SLEEVE_IO	24	IO_USBN6
5	AGND_IO	25	IO_USBP6
6	HPOUT_JD_IO	26	GND_IO
7	HPOUT_L_IO	27	IO_USBN9
8	AGND_IO	28	IO_USBP9
9	HPOUT_R_IO	29	IO_FPR_SCAN#
10	AGND_IO	30	IO_HALL_ON1#
11	IO_USB_EN#	31	+VRTC_BATT_IO
12	IO_USB_OC3#	32	+3P3VSB_IO
13	IO_PWR_BTN#	33	+3P3VA_IO
14	GND_IO	34	NC
15	IO_USB3_TX_P3	35	+3P3V_IO
16	IO_USB3_TX_N3	36	+3P3V_IO
17	GND_IO	37	NC
18	IO_USB3_RX_P3	38	+5VSB_IO
19	IO_USB3_RX_N3	39	+5VSB_IO
20	GND_IO	40	+5VSB_IO

Hall Sensor







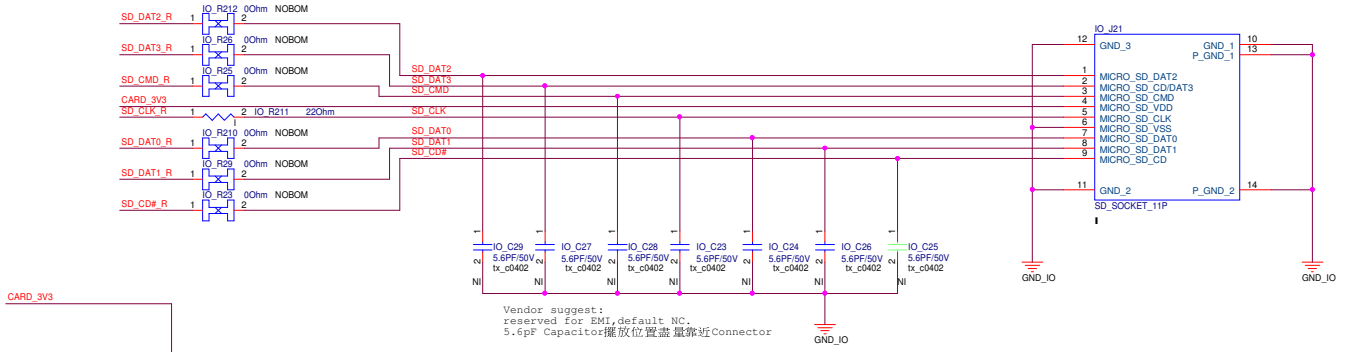
C

G

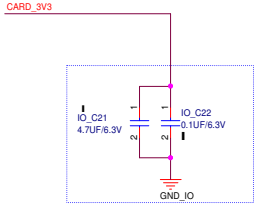
For Power button standoff
11/09 Change to 1308-00W8000

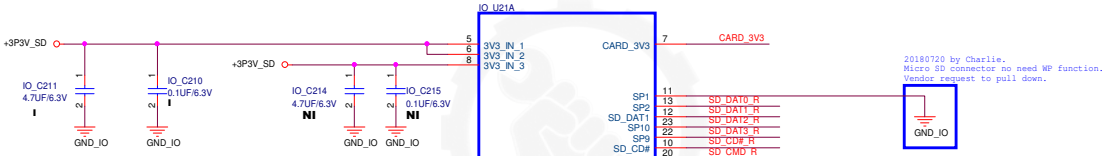
<Core Design>
PEGATRON Title : IO Conn
Pegatron Corp. Engineer: Charlie1_Chen
Size C | Project Name Nebula | Rev A00
Date: Wednesday, March 27, 2019 | Sheet 91 of 96

A02 Card_reader_RTS5144-GR

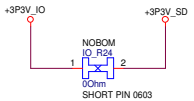


Vendor suggest:
reserved for EMI,default NC.
5.6pF Capacitor擺放位置盡量靠近Connector

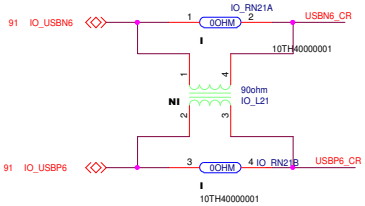




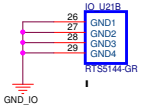
POWER



Imax: 400mA



card lock	SD_WP pin high
card unlock	SD_WP pin low



<Core Design>

PEGATRON Title : Card_reader_RTS5144GR

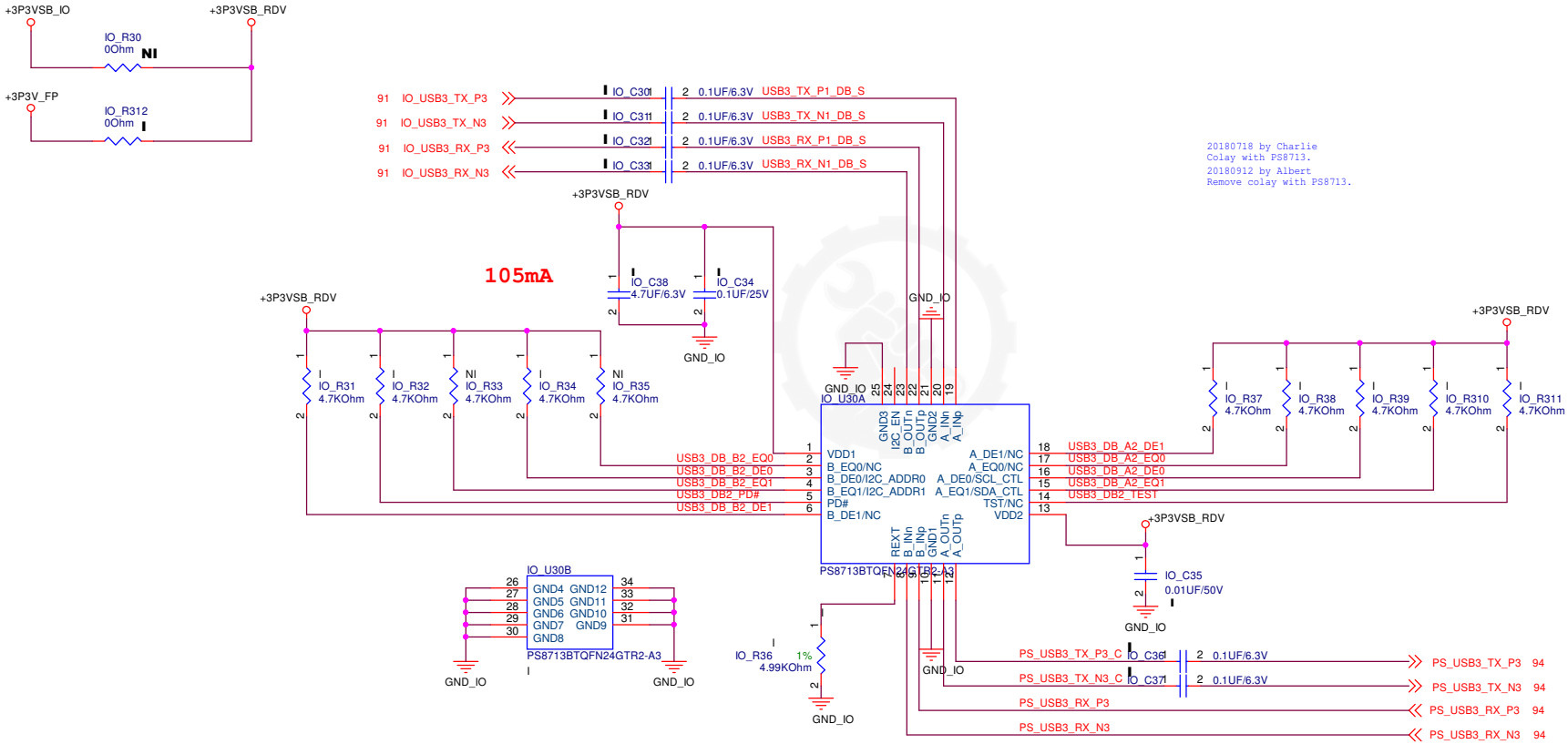
Pegatron Corp. Engineer: Albert2_Liu

Size	Project Name	Rev
C	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 92 of 96

A03 USB3.1 TypeA Port1 & Repeater (IO Board)

Imax: 105mA



<Core Design>

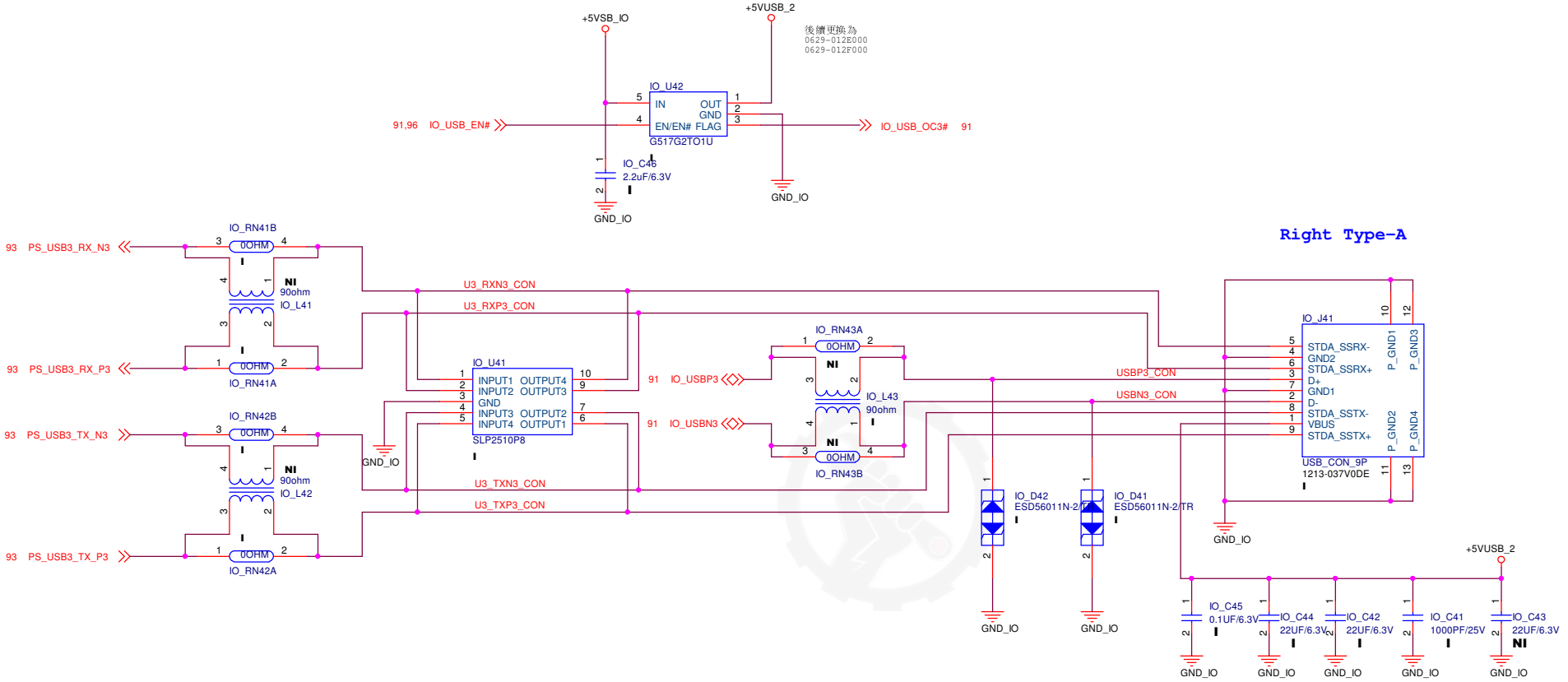
PEGATRON Title : USB TypeA Rep.

Pegatron Corp. Engineer: Albert2_Liu

Size	Project Name	Rev
A3	Nebula	A00

Date: Wednesday, March 27, 2019 Sheet 93 of 96

A04 USB3.1 TypeA Port1 & Repeater (IO Board)



<Core Design>

PEGATRON Title : USB CONN & POWER

Pegatron Corp. Engineer: Albert2_Liu

Size	Project Name	Rev
A3	Nebula	A00

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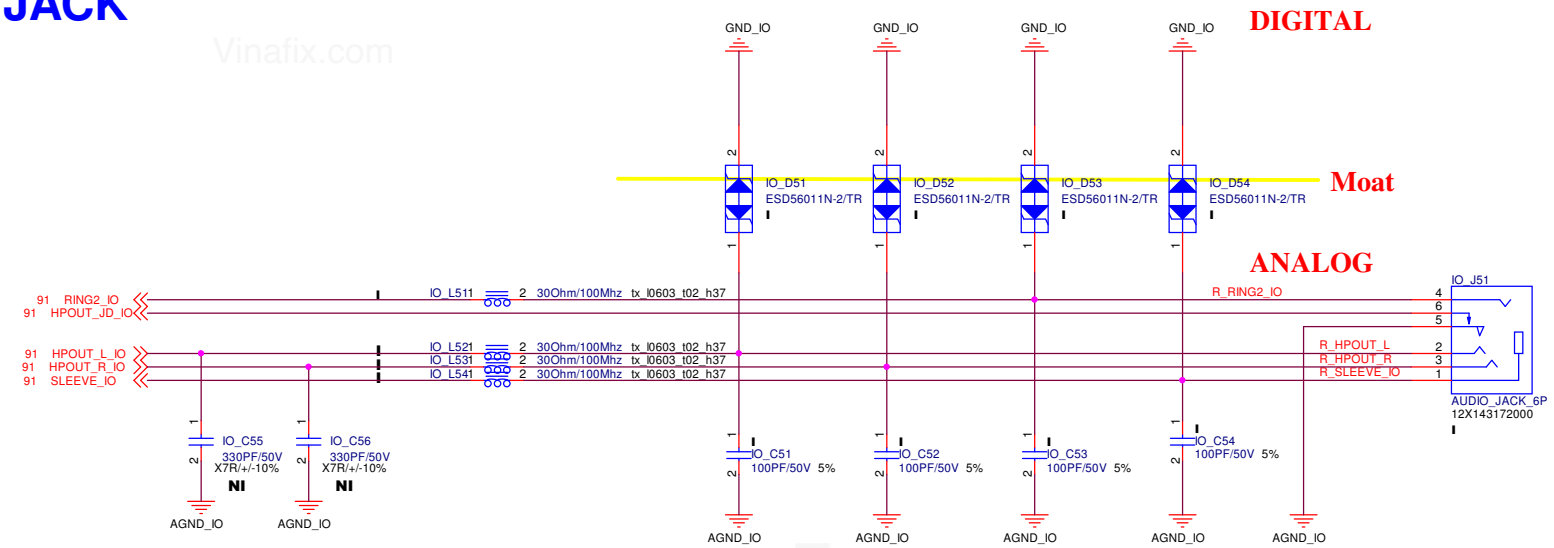
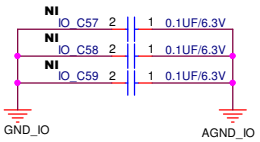
A05 AUDIO JACK





GLOBAL HEADSET CONNECTOR

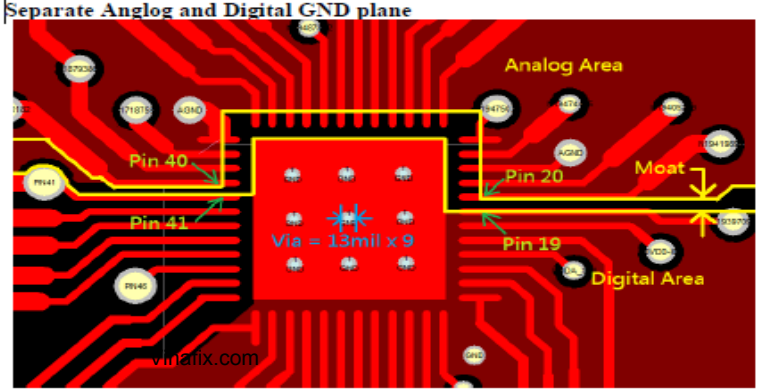
OMTP/CTIA headset, Headphone, Line-Out, Microphone input, Line input.

Below figures are 4-pole jack plugged to the combo phone jack, we could see that right figure's HP-JD pins(#5/#6) attached to HP-L(#1), that imply headset jack has to be fully plugged to make HP JD trigger. This kind of connector will significantly decrease the chance of wrong judgment. Below left figure is not the recommended phone-jack, because its HP-JD(#3/#4) attached to HP right channel.

PCB trace width of Mic1-R/Mic1-L(SLEEVE/RING2) are required at least 40 mil for HP crosstalk consideration, and its length should be as short as possible.

FB1/FB2 should choose DC resistance (Rdc) < 30mOhm to get the best audio performance for HP crosstalk.

Separate Anglog and Digital GND plane



<Core Design>

PEGATRON Title : AUDIO JACK

Pegatron Corp. Engineer: Steven_Diau

Size	Project Name	Rev
A3	Nebula	A00

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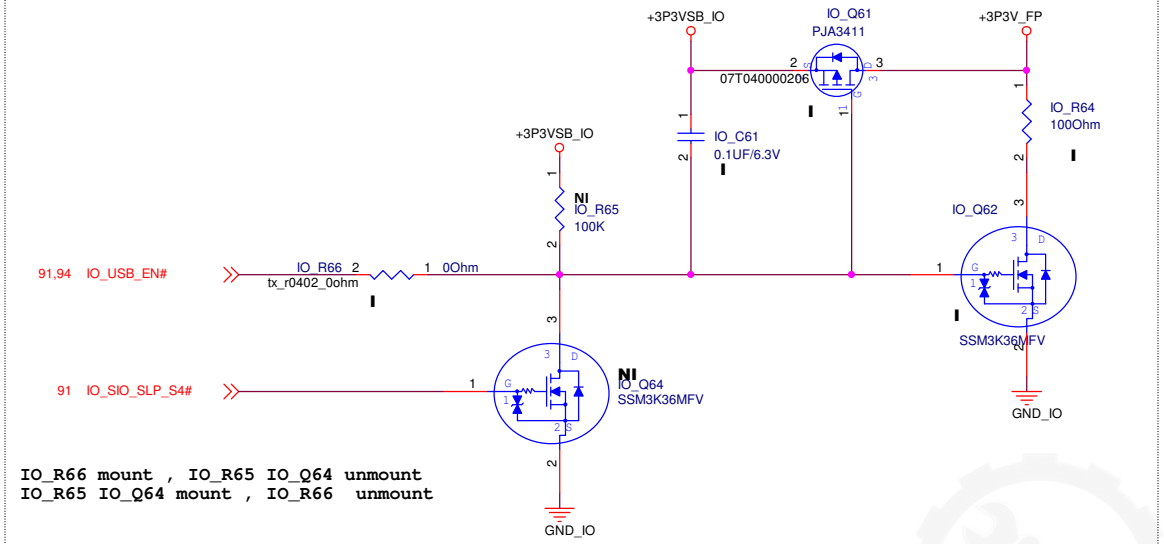
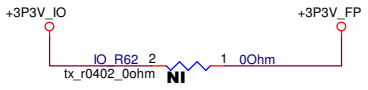
A06 Finger Print

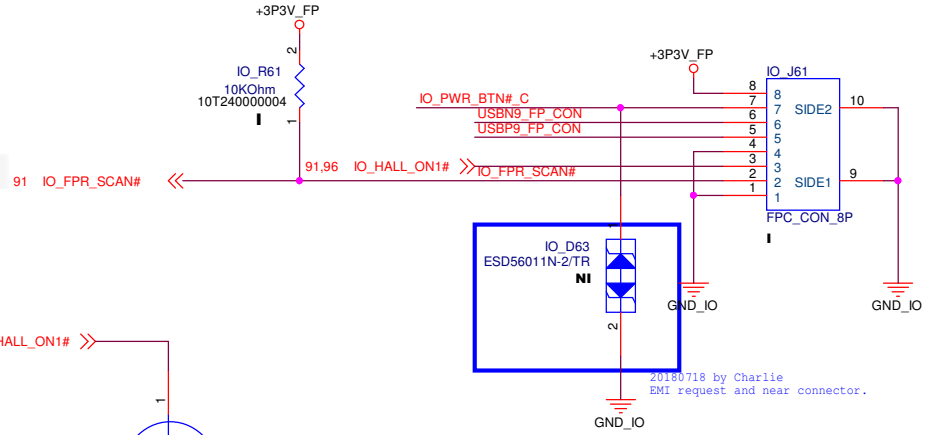
2018.11.13_By Albert2
Customer demand
-> FP S3 state keep power on(S4 no power)

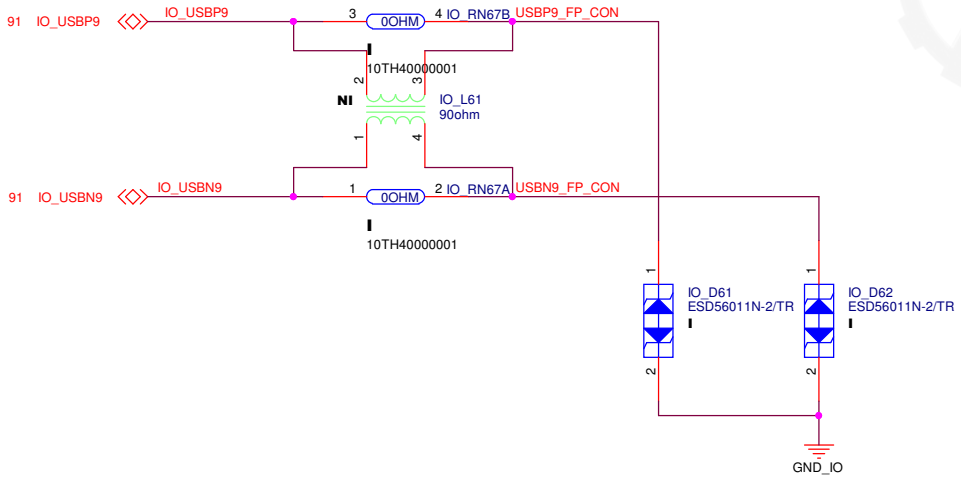


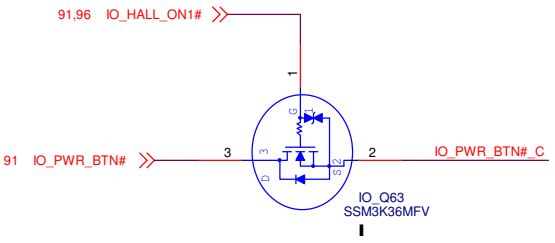
2018.11.05_By Albert2
Ref Armani design. Keep +3P3V_IO for optional



FPR CONNECTOR







<Core Design>

PEGATRON	Title : IO Conn	
Pegatron Corp.	Engineer: Albert2_Liu	
Size: B	Project Name: Nebula	Rev: A00
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