Compal Confidential

LA-H011P Schematics Document

intel Coffee Lake S with DDR4 + CNP

AIO M/B

8/21 , 2018

REV : 1.A

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title: *Cover Page*		
Size: Custom	Document Number: LA-H011P M/B	Rev: 1.0
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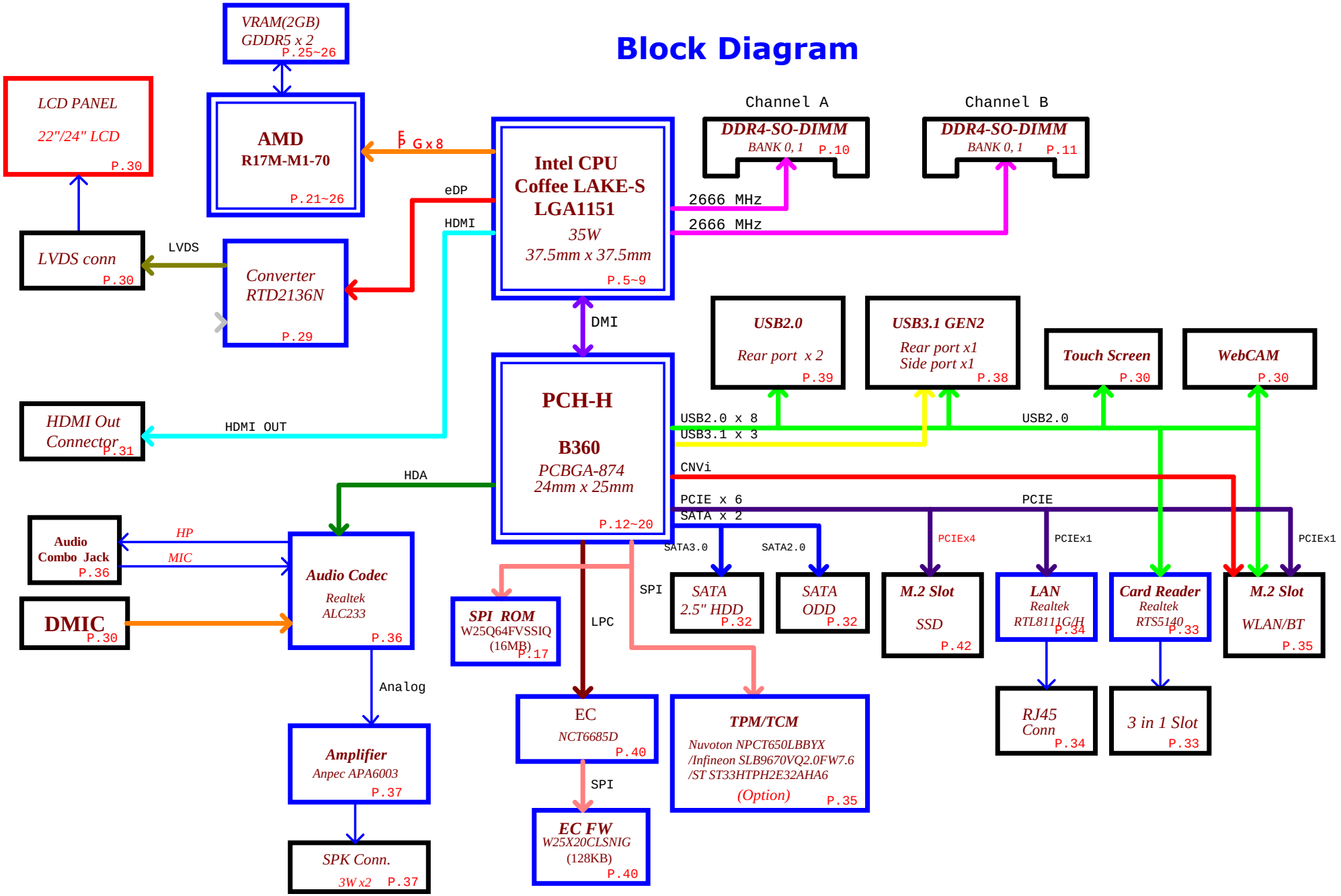
PCB Size : 163 mm x 276 mm

Block Diagram



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PCIE Port Table

No.	Port	Device
5	11	NC
6	12	LAN
7	13	WLAN
8	14	NC
21	27	SSD
22	28	SSD
23	29	SSD
24	30	SSD

SATA Port Table

No.	Port	Device
1	17	NC
2	18	NC
3	19	SSD
4	20	HDD
5	21	ODD
6	22	NC
7	23	NC
8	24	NC

USB2.0 Port Table

Port	Device	OC# Pin
1	USB 2.0 Rear IO Port 1	OC#0
2	USB 2.0 Rear IO Port 2	OC#0
3	USB 2.0/3.0 (Side IO)	OC#1
4	USB 2.0/3.0 (Rear IO)	OC#2
5	NC	NA
6	NC	NA
7	Web Camera	NA
8	Card Reader	NA
9	TOUCH	NA
14	WLAN/BT	NA

USB3.0 Port Table

No.	Port	Device
1	1	NC
2	2	USB3.0 (Side IO) GEN2
3	3	NC
4	4	USB3.0 (Rear IO) GEN2
5	5	NC
6	6	NC

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	

DDI Port Table

No.	Port	Device
1	DDI1	HDMI OUT
2	DDI2	NC
3	DDI3	NC

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+DC20V	AC or battery power rail for power circuit.	N/A	N/A	N/A
+RTCVCC_S5	RTC power	ON	ON	ON*
+3V3_DSW	3.3V DSW on power rail	ON	ON	ON*
+3VALW_S5	3.3V always on power rail	ON	ON	ON
+5VALW_S5	5V always on power rail	ON	ON	ON
+12VALW_S5	12V always on power rail	ON	ON	ON
+1.8VALW_S5	1.8V always on power rail	ON	OFF	OFF
+1.05VALW_S5	1.05V always on power rail for PCH	ON	ON	ON
+1.05V_VCCST_S3	1.0V power rail for CPU VCCST	ON	ON	OFF
+1.2V_VDDQ_S3	1.2V power rail for DDR4	ON	ON	OFF
+2.5V_S3	2.5V power rail for DDR4	ON	ON	OFF
+CPU_VCCIO_S0	0.95V power rail for CPU VCCIO	ON	OFF	OFF
+5VS_S0	5V switched power rail	ON	OFF	OFF
+3VS_S0	3.3V switched power rail	ON	OFF	OFF
+12VS_S0	12V switched power rail	ON	OFF	OFF
+1.05VS_VCCSA_S0	+1.5VS on power rail for CPU VCCSA	ON	OFF	OFF
+VCC_CORE_S0	VCC Core voltage for CPU	ON	OFF	OFF
+VCC_GT_S0	Core voltage for CPU graphic	ON	OFF	OFF
+3VS_DGPU_S0	3.3V power rail for DIS graphic	ON	OFF	OFF
+VGA_CORE_S0	VCC Core voltage for GPU	ON	OFF	OFF
+1.05VS_DGPU_S0	1.05V power rail for DIS graphic	ON	OFF	OFF
+1.35VS_VGA_S0	1.35V power rail for VRAM	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SKU ID(Project) Table

SKU (UMA&DIS)	AIO340 CFL-S WW BOM Configure Table
431AEG38L51 UMA	
431AEG38L02 Samsung 2G	
431AEG38L03 Micron 2G	
431AEG38L04 Hynix 2G	
X4EAEG38L01	

SKU (UMA&DIS)	AIO340 CFL-S PRC BOM Configure Table
431AEG38L01 UMA	
X4EAEG38L01	

BOM Structure Table

BOM Structure	BTO Item

EC SM Bus0 Address

Device	Address	HEX
Converter	1001-0100xb	94
GPU	1000-0010xb	82
PCH	1001-0000xb	90

EC SM Bus2 Address

Device	Address	HEX
LCD Backlight	0110-0010xb	62

PCH SM Bus Address

Device	Address	HEX
DDR(JDIMM1)	WRITE:0xA0	READ: 0xA1
DDR(JDIMM2)	WRITE:0xA4	READ: 0xA5

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Issued Date	2018/6/14	Deciphered Date	2019/6/14
Title	Notes List		
Size C	Document Number LA-H011P M/B		Rev 1.0
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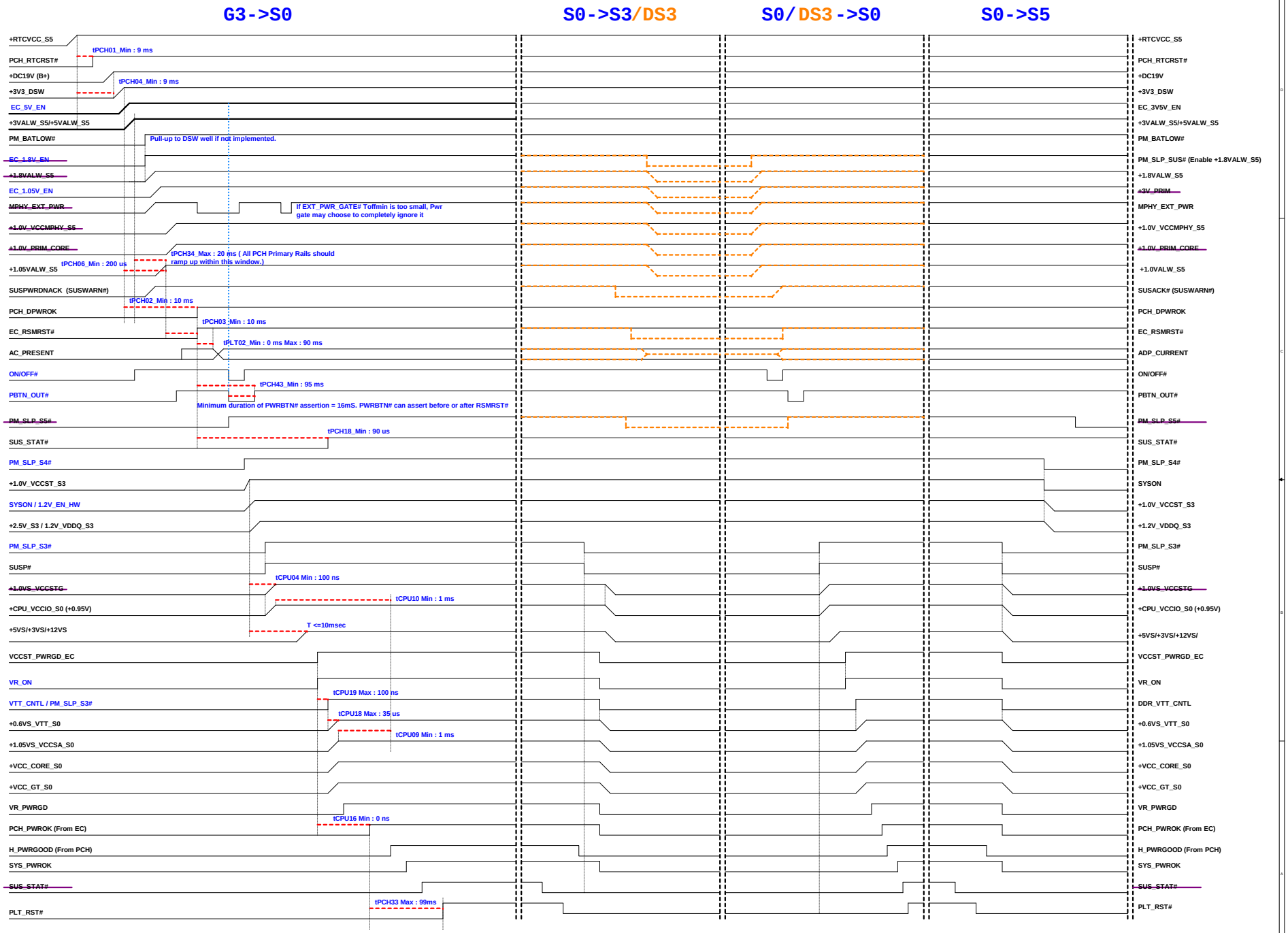
Power Sequence_SKL-S [Deep Sx Platform]



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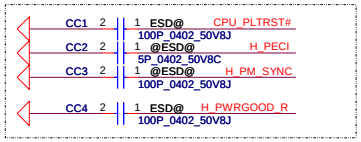
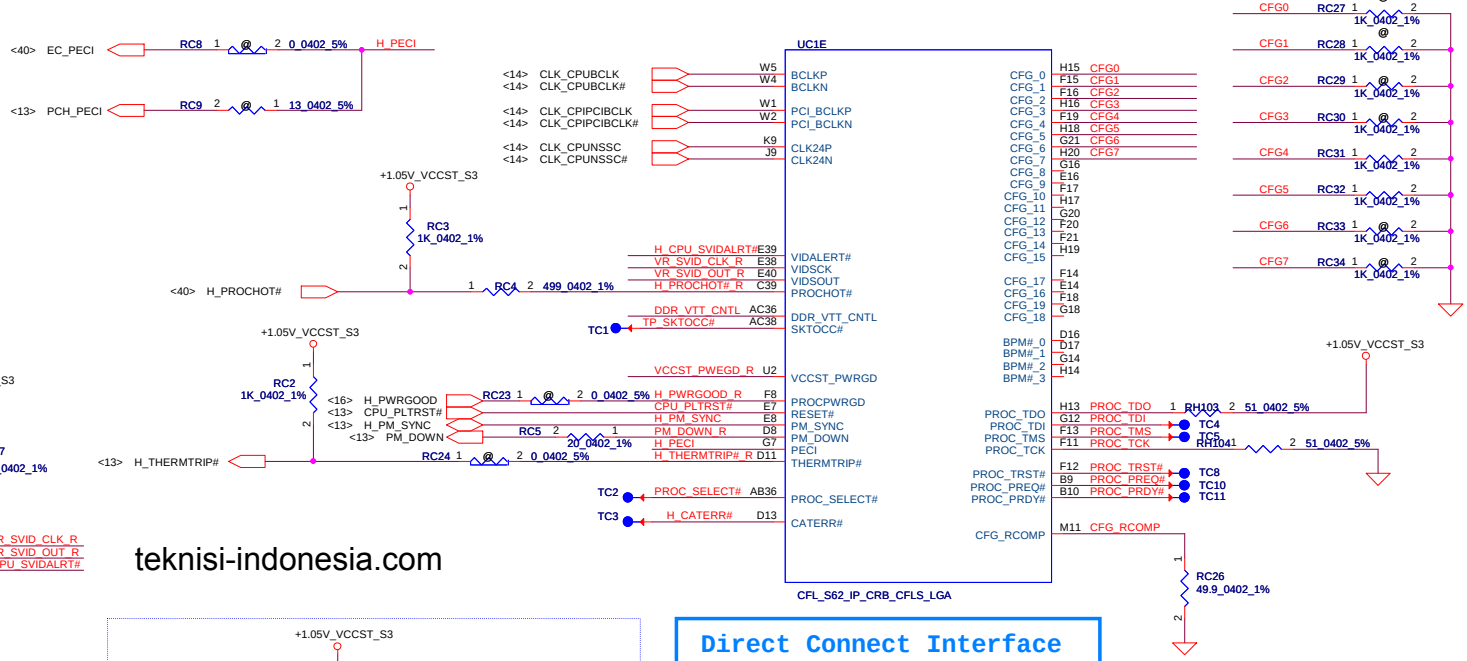
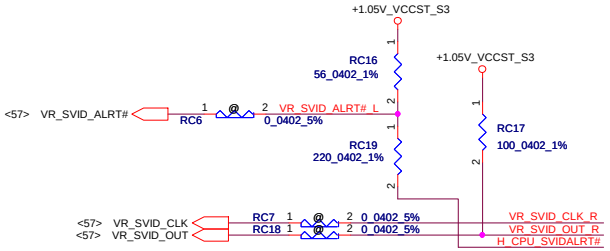
Title	PWR Sequence		
Size: Custom	Document Number: LA-H011P M/B		Rev: 1.0
Date: Tuesday, August 21, 2018	Sheet 4 of 61		



ESD request Close to CPU as possible





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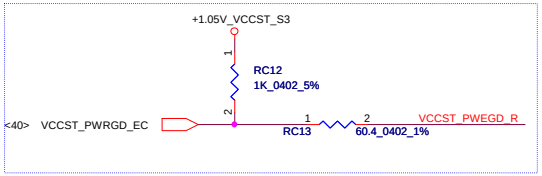
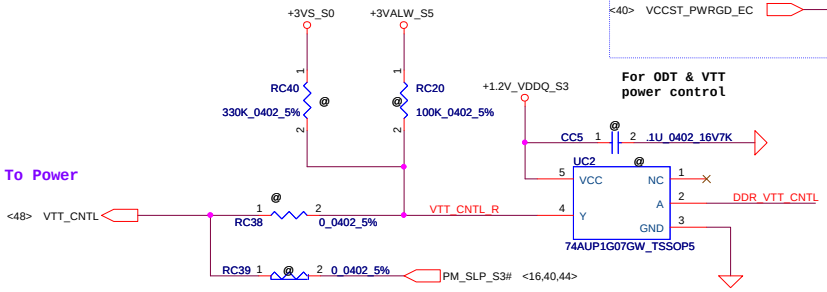
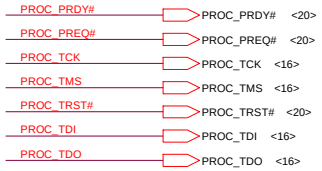


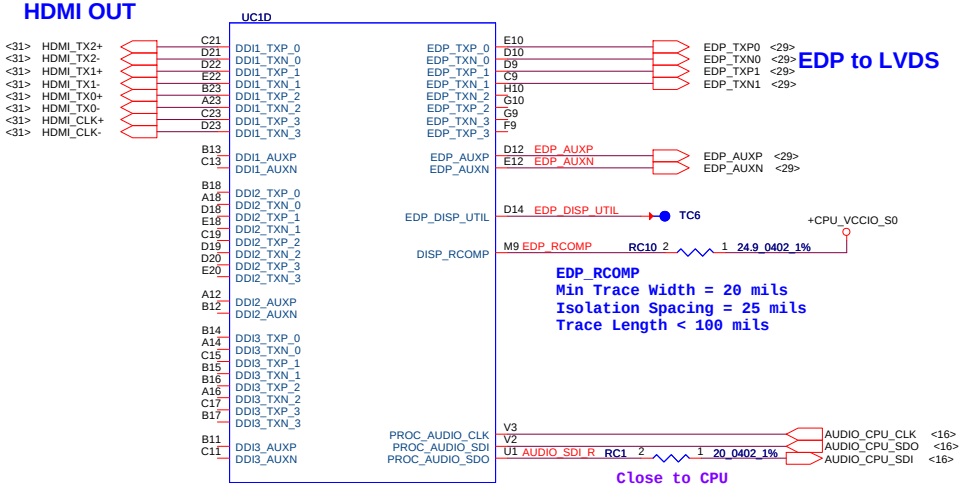
For ODT & VTT power control



Direct Connect Interface



HDMI OUT



EDP to LVDS

EDP_RCOMP
Min Trace Width = 20 mils
Isolation Spacing = 25 mils
Trace Length < 100 mils

Close to CPU

Table 7-1. Mapping of HDMI* Signals for DDI Ports

Port	Digital Display Interface Pins	CRB Digital Display Interface Signals	HDMI* Signals
Port 1	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIx_TX2_DP
	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIx_TX2_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIx_TX1_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIx_TX1_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIx_TX0_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIx_TX0_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIx_CLK_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 1	DDPB_HPD	DDI1_HPD_Q
	HDMI DDC lines for Port 1	DDPB_CTRLCLK	DDI1_CTRL_CK
		DDPB_CTRLDATA	DDI1_CTRL_DATA

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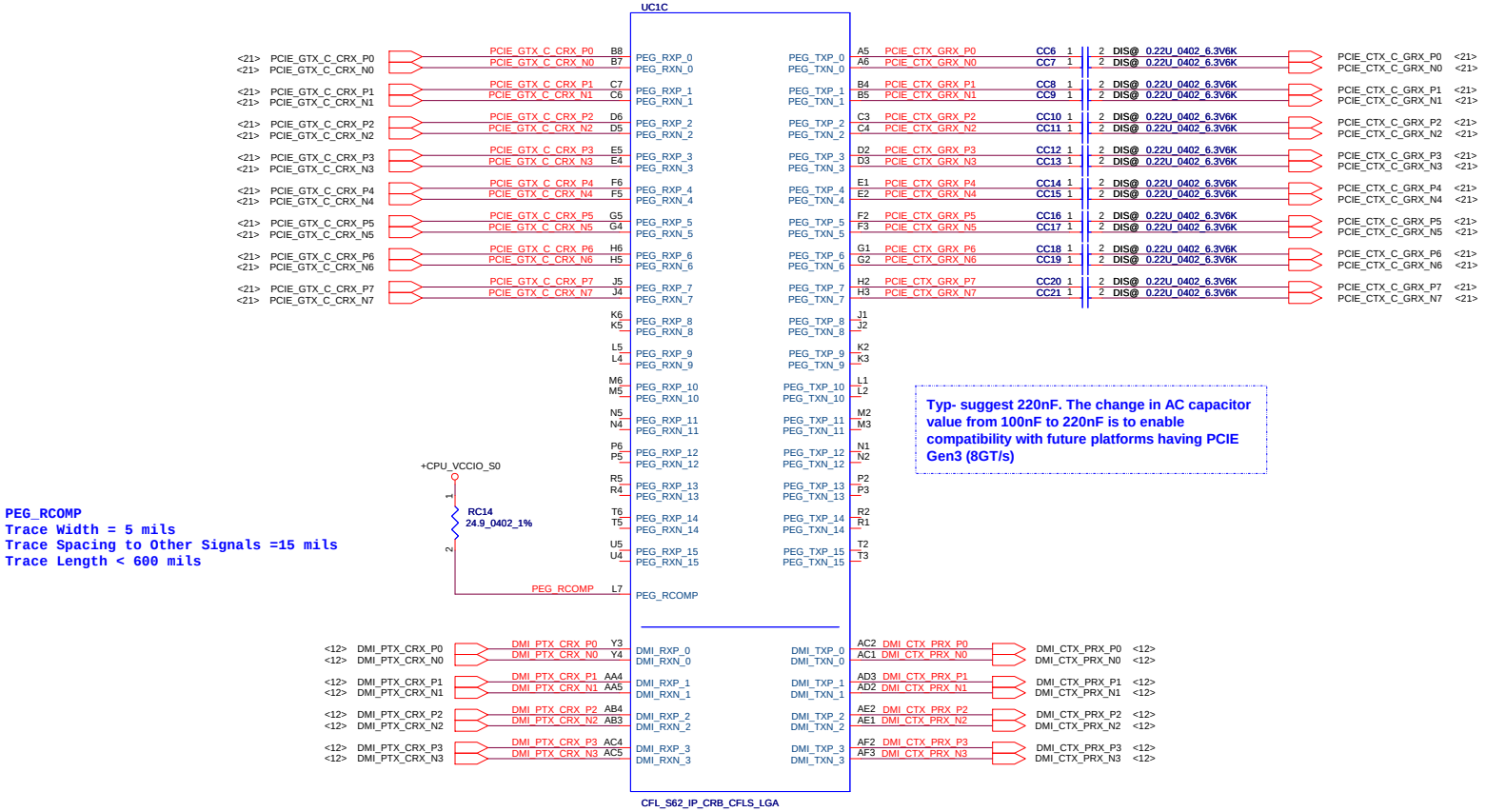

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Compal Electronics, Inc.

Title: ***Skylake DMI/PEG/FDI***

Size	Document Number	Rev
Custom	LA-H011P M/B	1.0

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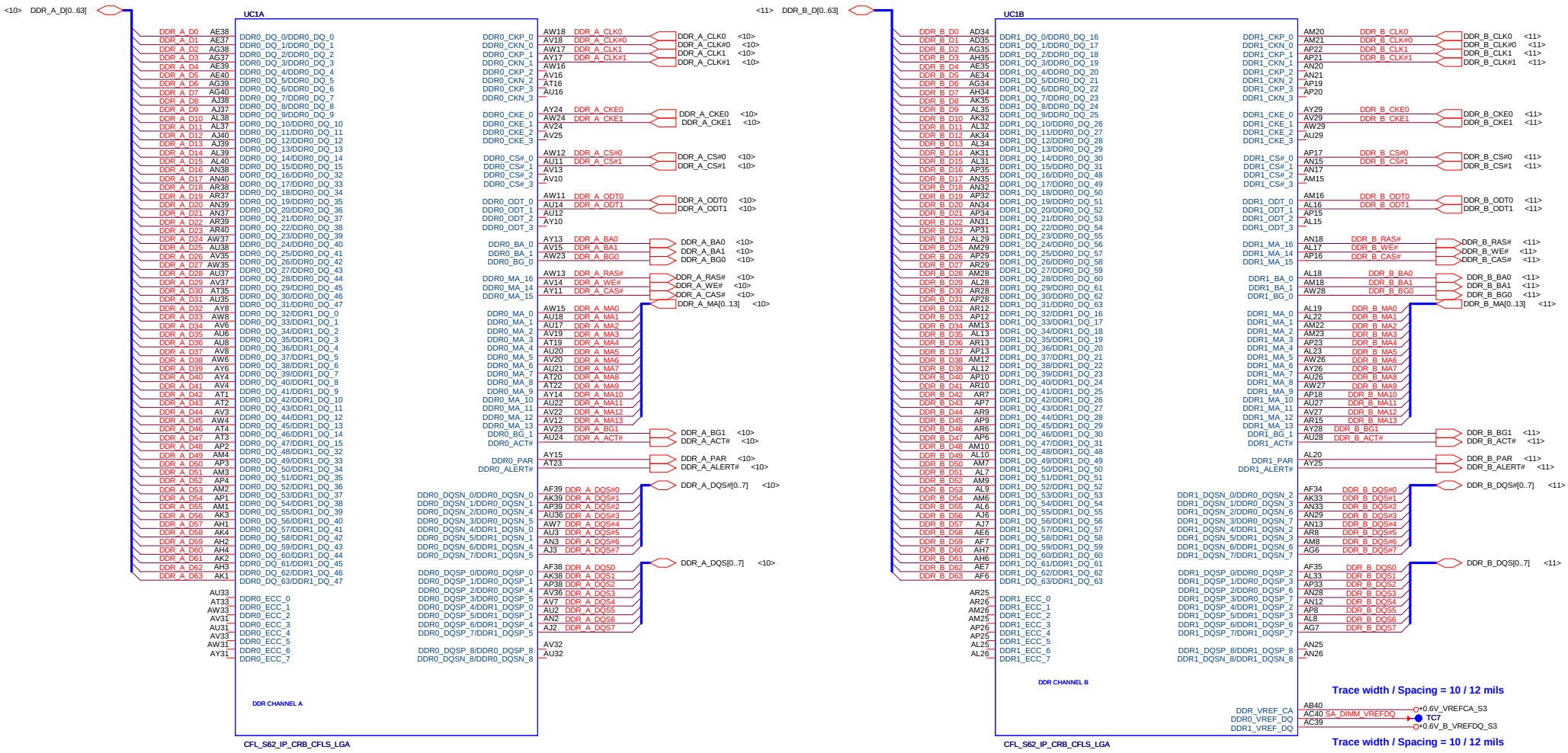

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Title: ***Skylake DDR4***

Size	Document Number	Rev
Custom	LA-H011P M/B	1.0

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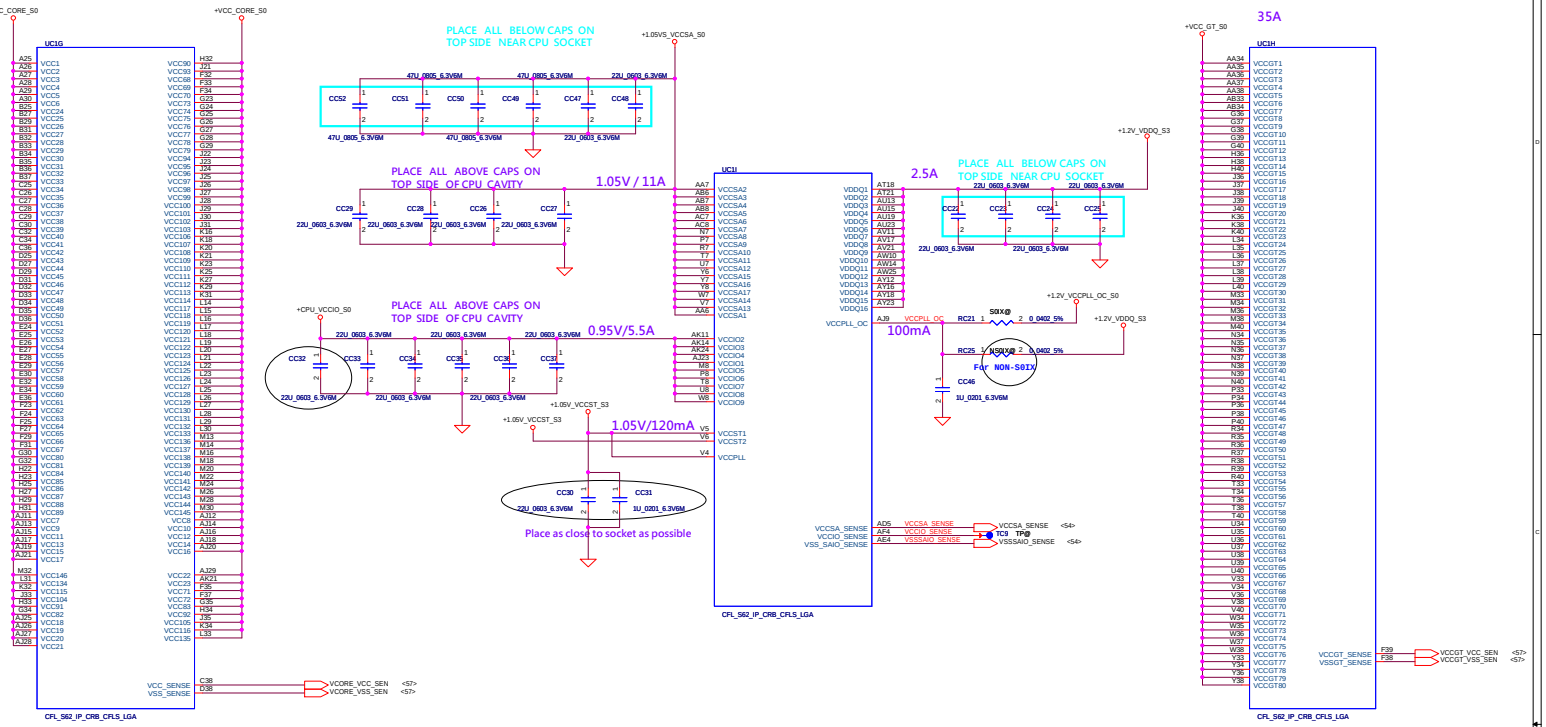

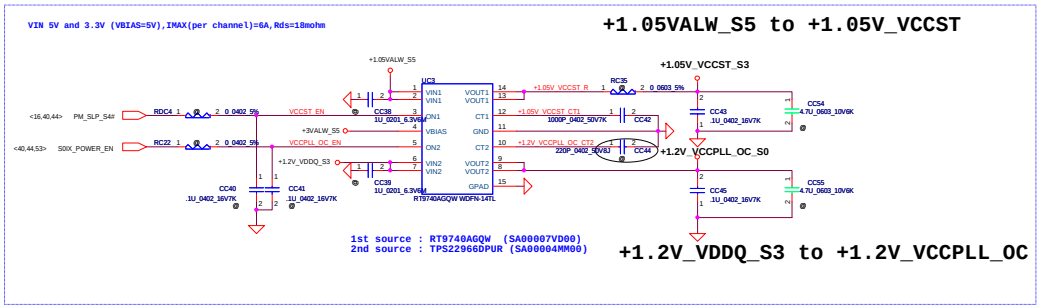

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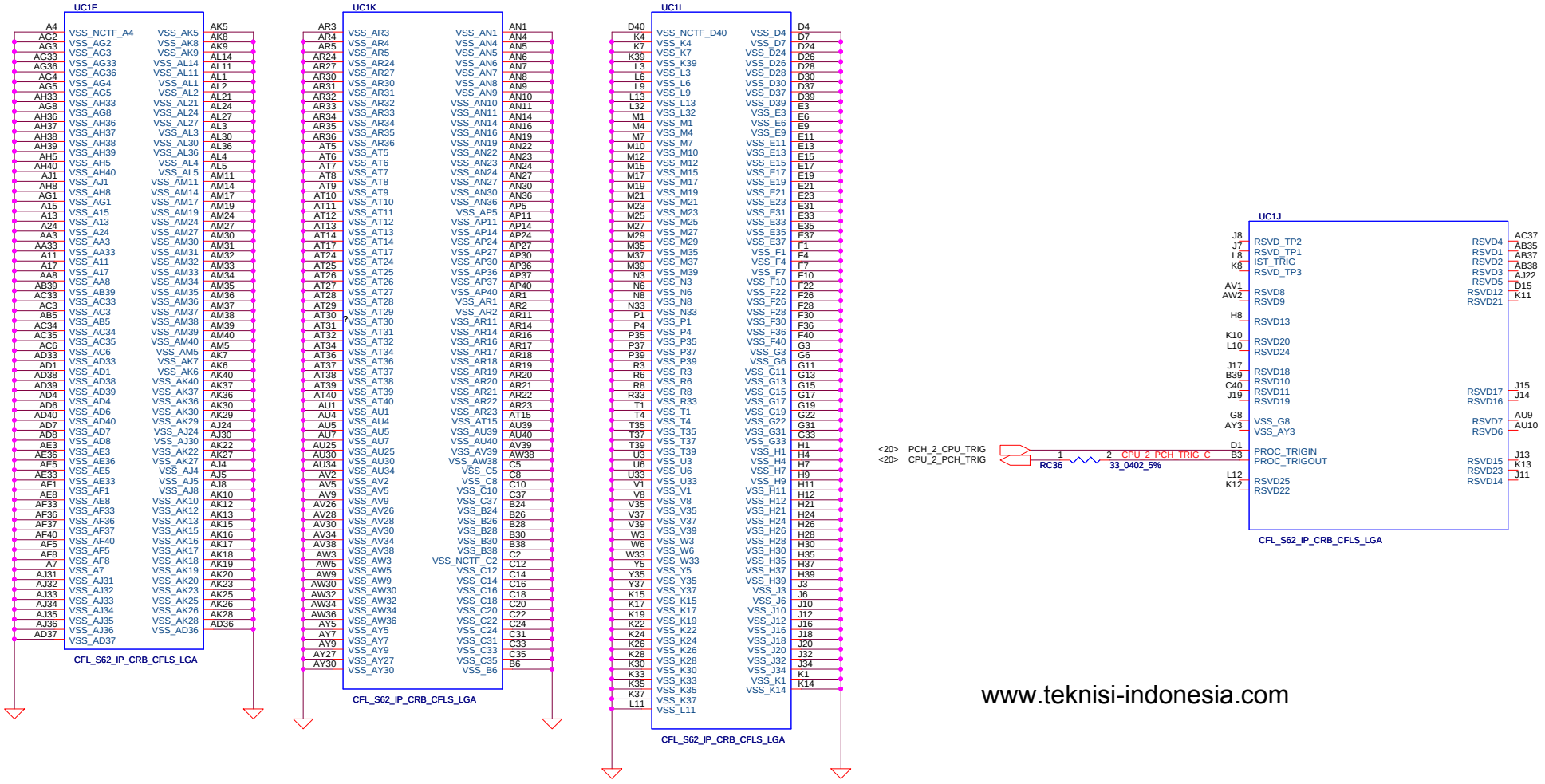
Title	Skylake POWER		
Size	Document Number		Rev
Custom	LA-H011P M/B		1.0
Date: Tuesday, August 21, 2018	Sheet 8 of 61		



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Title: ***Skylake GND/RSVD***

Size	Document Number	Rev
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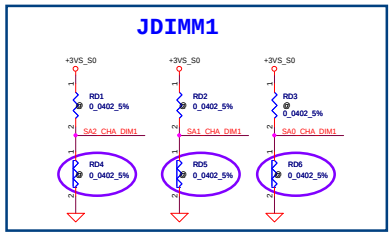
INTERLEAVE CHANNEL-A

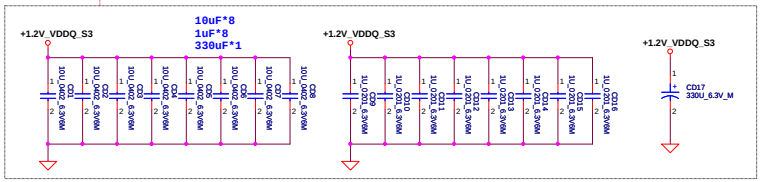
JDIMM1



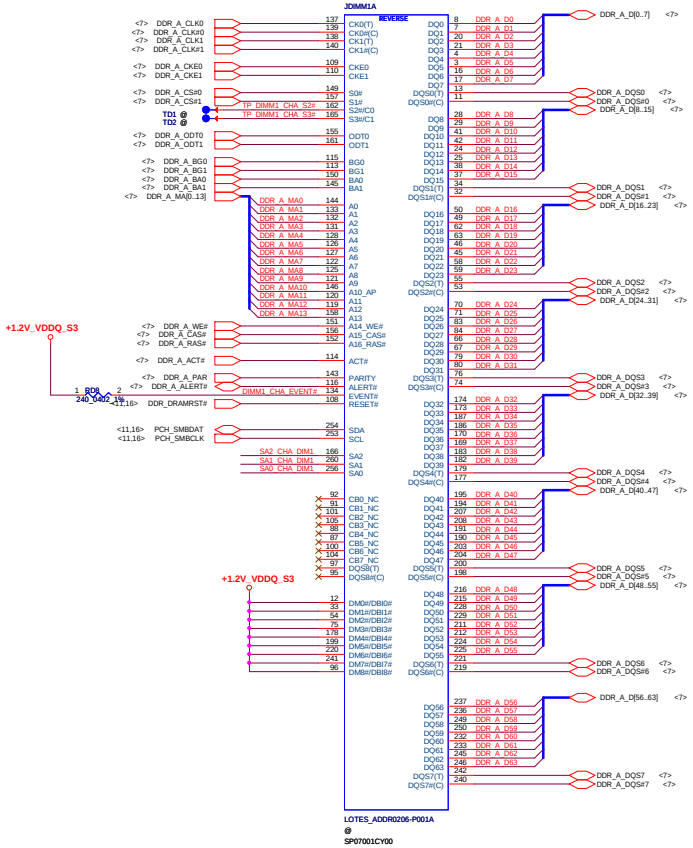
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS:0xA0
READ ADDRESS: 0xA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

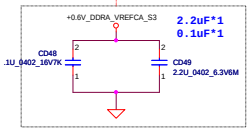
Layout Note:
Place near JDIMM1

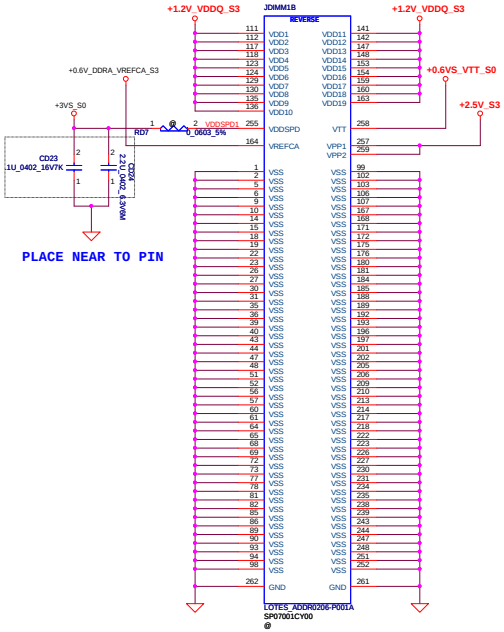


(4.0 mm) Reverse Type

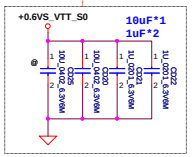


Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM1





Layout Note:
Place near JDIMM1



Layout Note:
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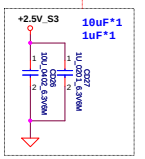

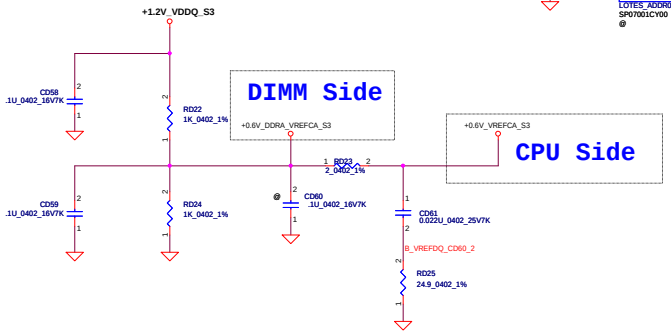

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Title: DDR4_DIMMB

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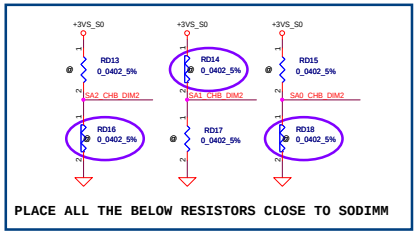
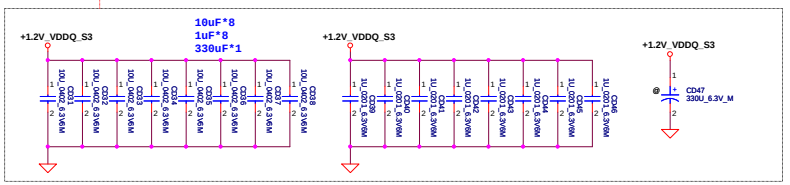
INTERLEAVE CHANNEL-B

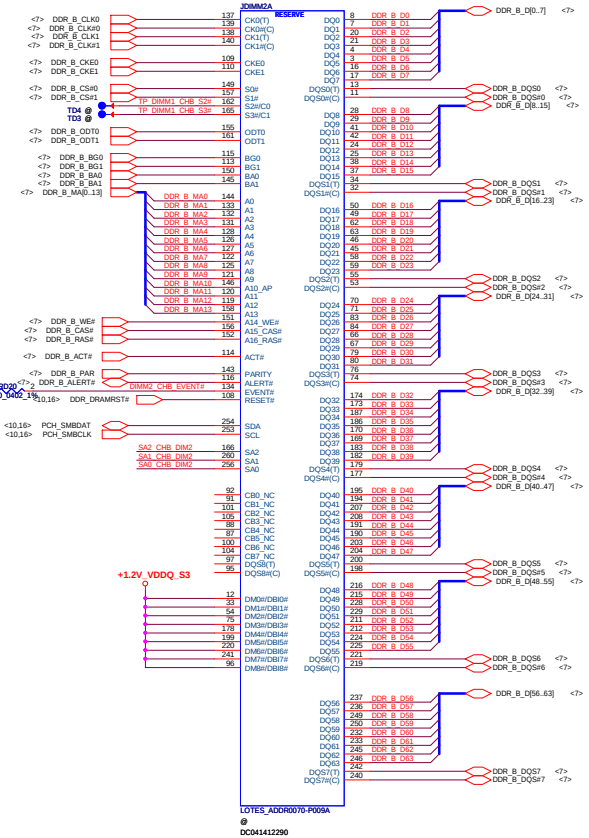
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS:0xA4
READ ADDRESS: 0xA5
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S



Layout Note:
Place near JDIMM2



(8.0 mm) Reverse Type



Layout Note:
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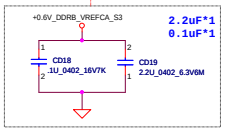
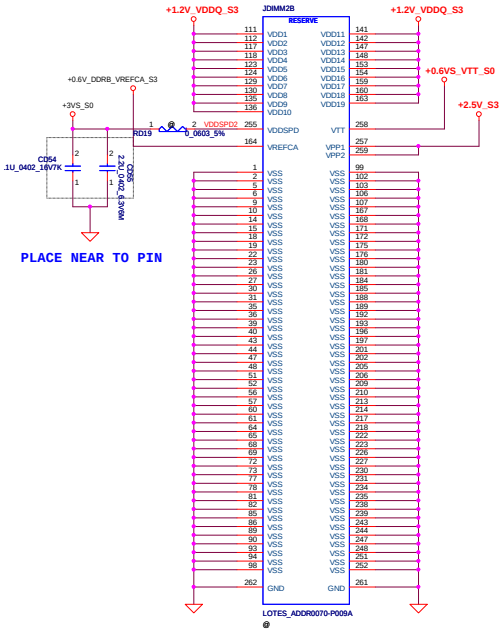
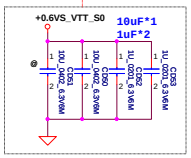
FROM THE JDIMM2



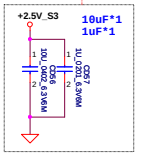


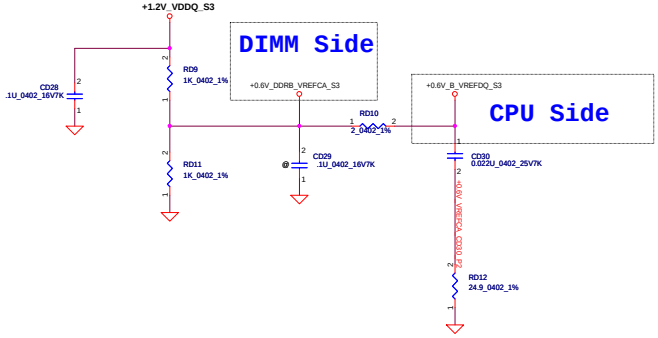
PLACE NEAR TO PIN

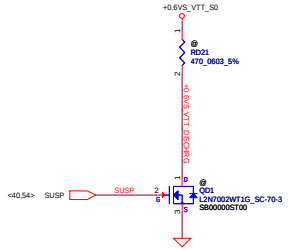
Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2







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Title: DDR4_DIMMA

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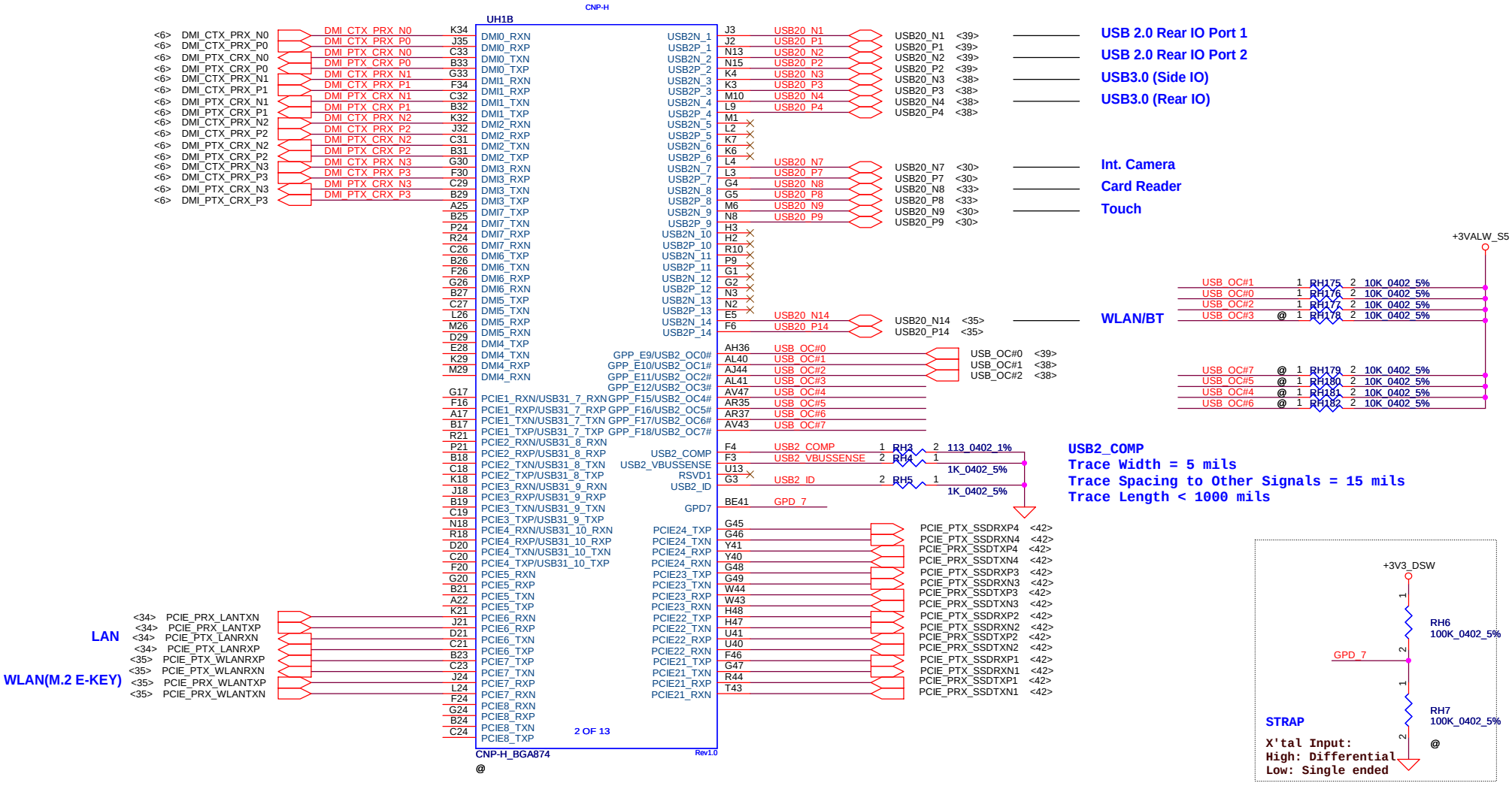

UH1

SA0000BXA10
FH82B360 SR408 B0 BGA PCH-H

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Compal Electronics, Inc.

Title: *PCH_DMI/USB2/PCIE*

Size	Document Number	Rev
B	LA-H011P M/B	1.0

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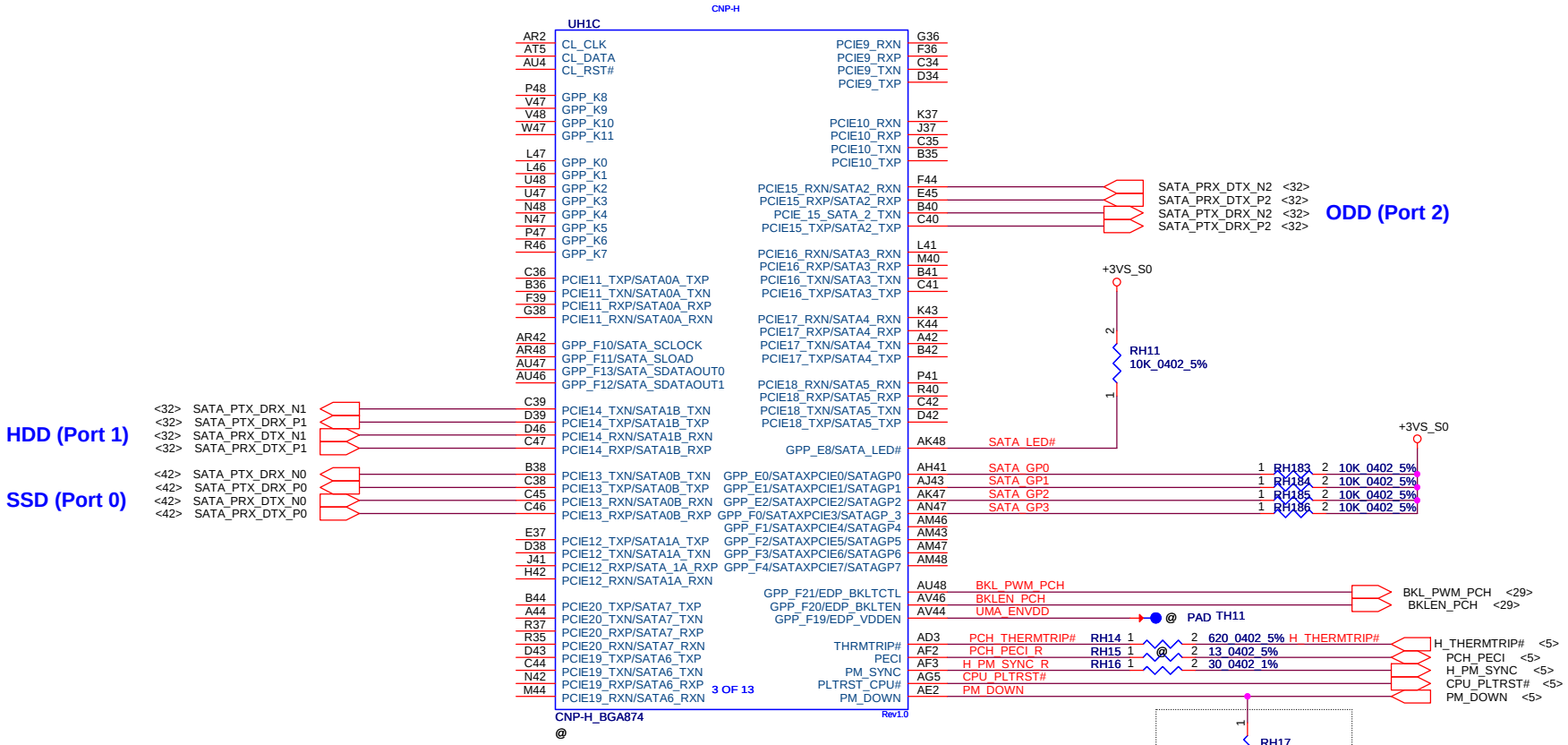

Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: ***PCH_HDA/JTAG/SATA***

Size	Document Number	Rev
B	LA-H011P M/B	1.0

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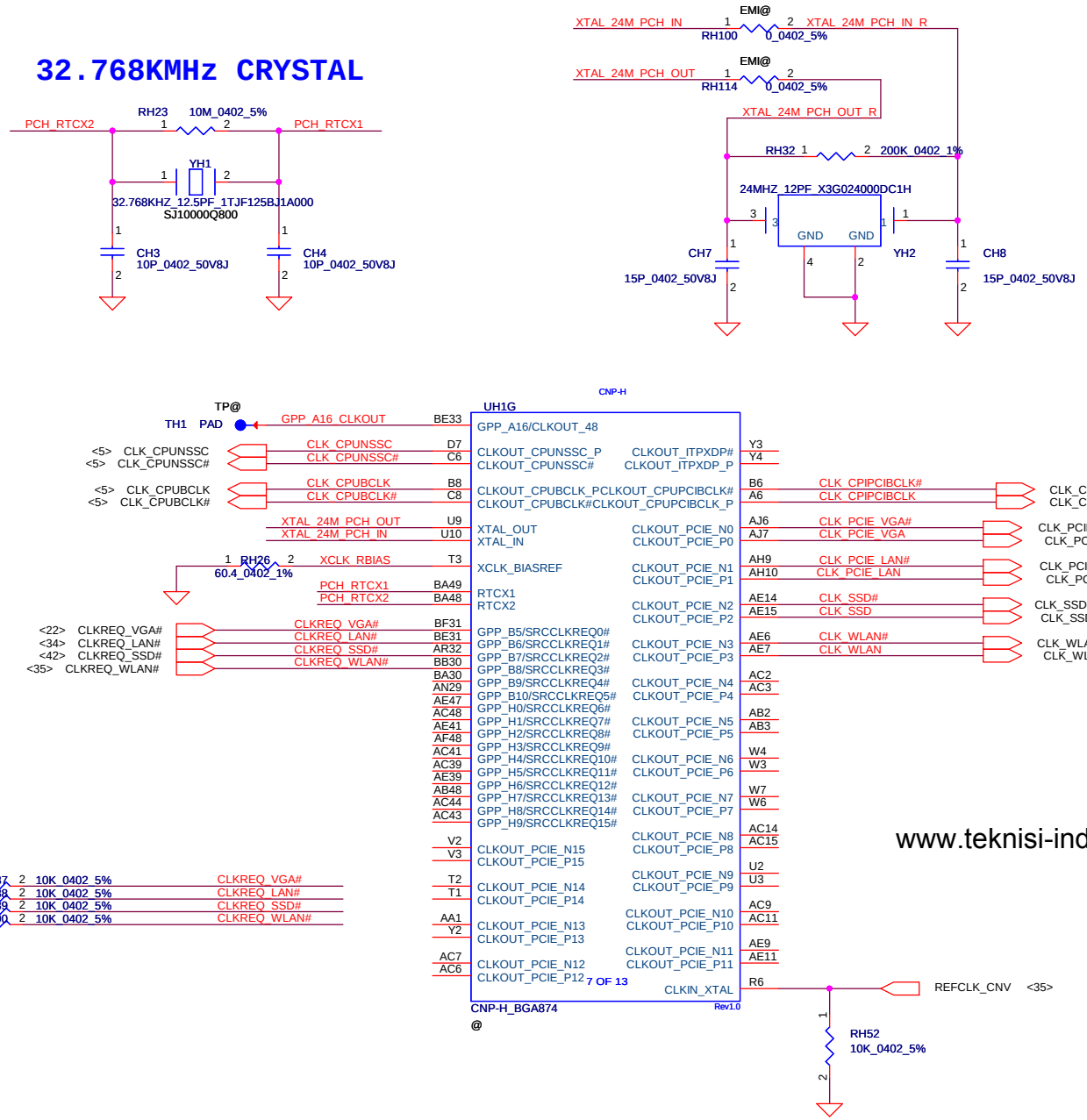

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Title	PCH_CLK\LPC\SPI\SMBUS		
Size: Custom	Document Number: LA-H011P M/B		Rev: 1.0
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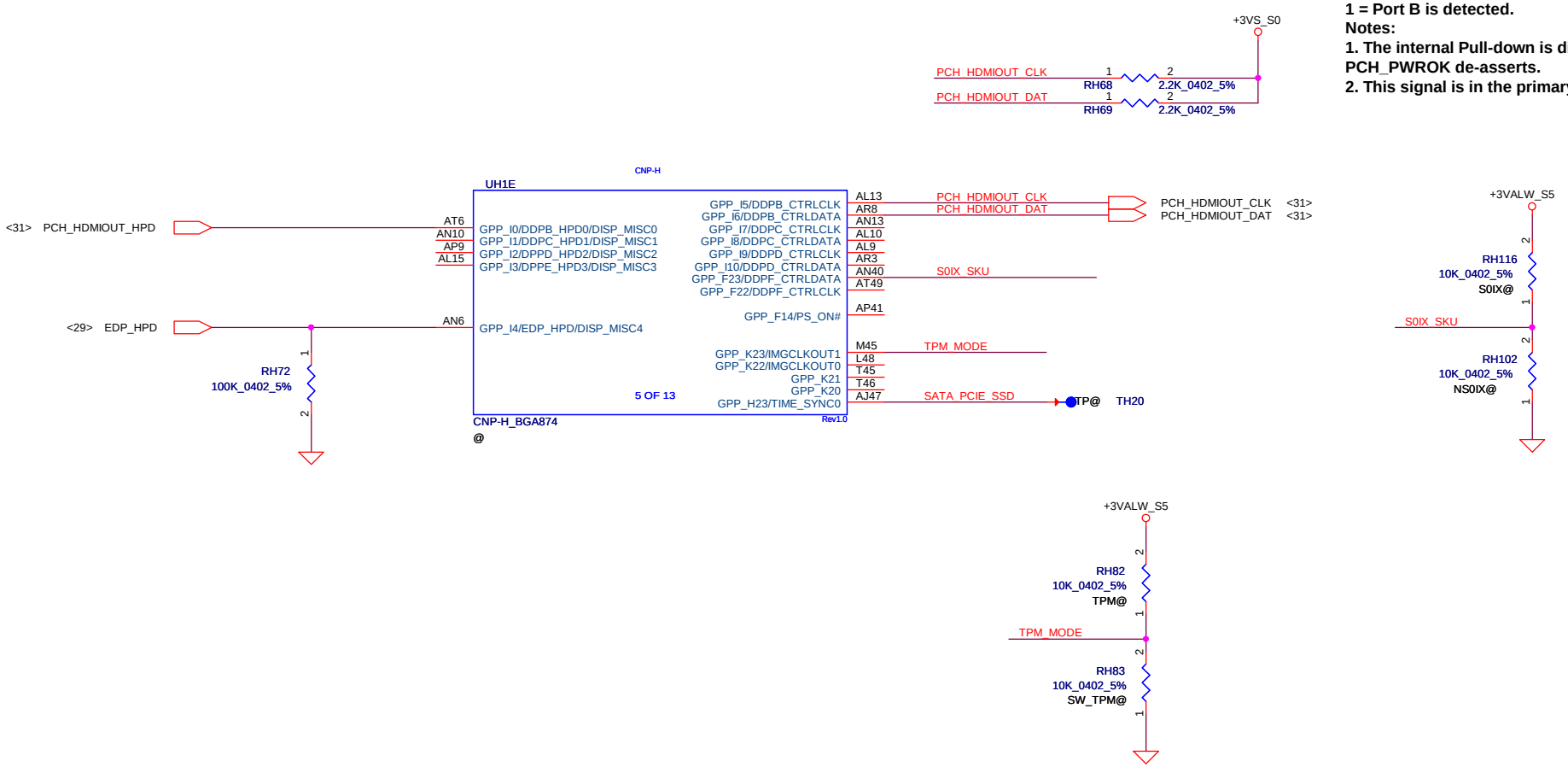
DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.
Notes:
1. The internal Pull-down is disabled after PCH_PWROK de-asserts.
2. This signal is in the primary well.



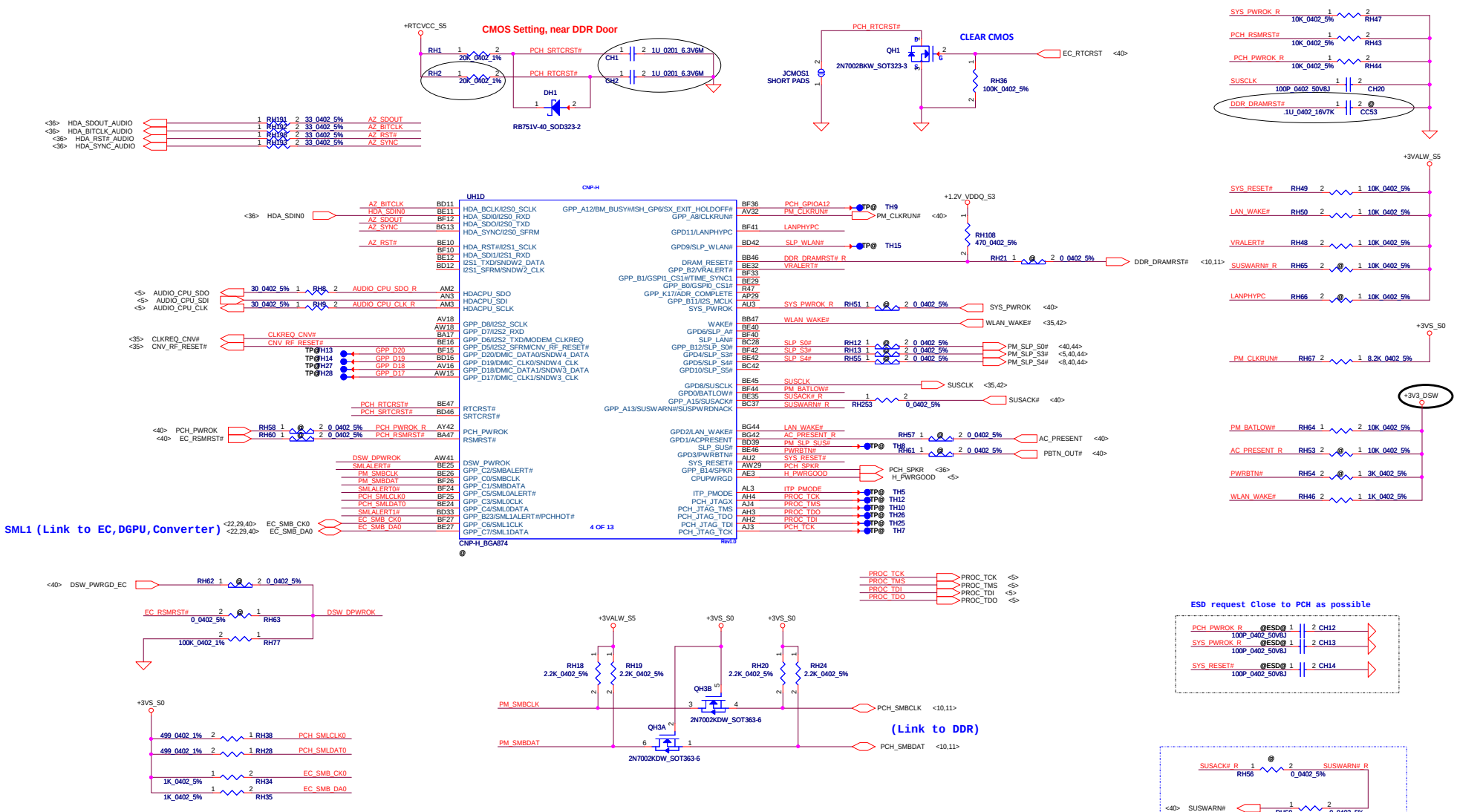
Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: ***PCH_CRT/DDC***

Size	Document Number	Rev
B	LA-H011P M/B	1.0

Date: Tuesday, August 21, 2018 Sheet 15 of 61



Functional Strap Definitions

SMLALERT#
This signal has a weak internal Pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
Notes:
1. The internal Pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Functional Strap Definitions

SMLALERT0#
This signal has a weak internal Pull-down.
0 = LPC is selected (for EC 9022).
1 = eSPI is selected (for EC 9042). (Default)
Notes:
1. The internal Pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

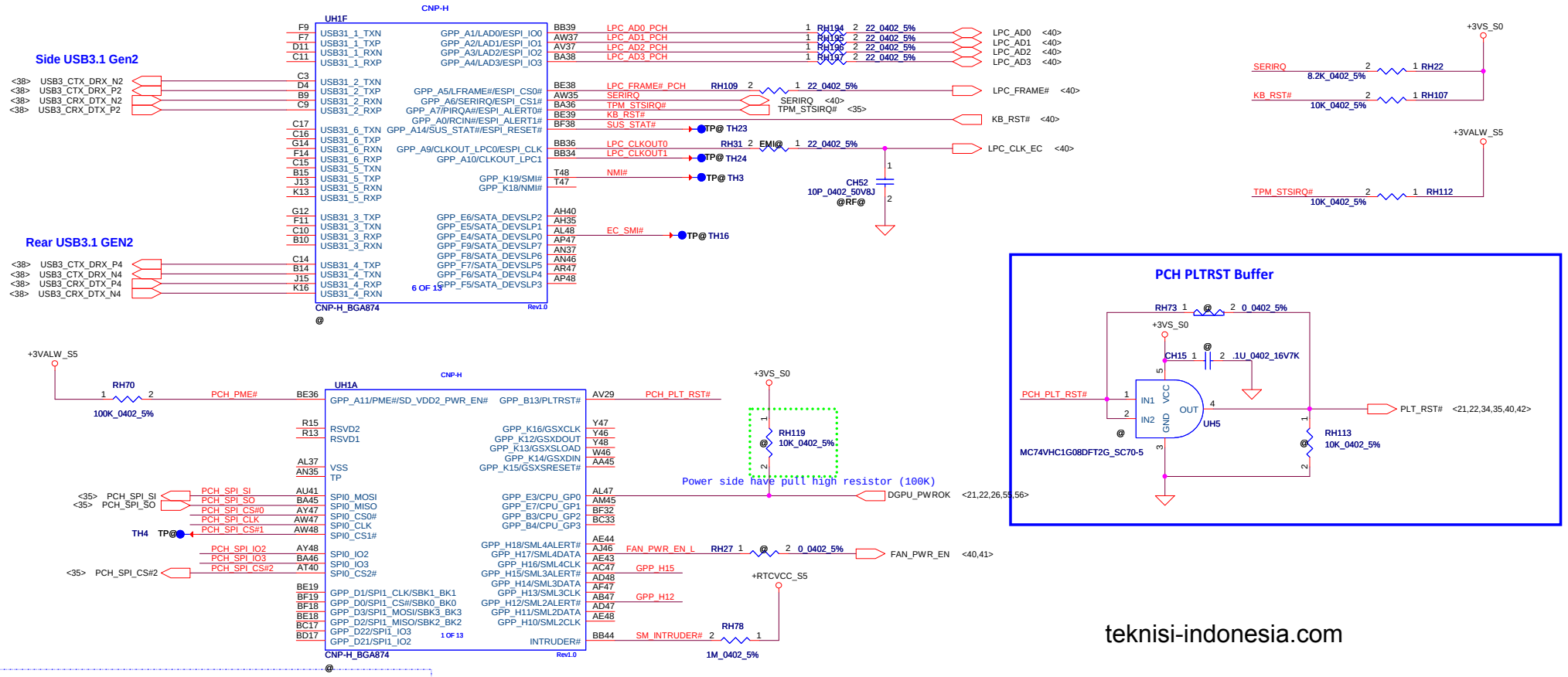
SMLALERT1#
This signal has an internal pull-down.
0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.

Vgs(max)=1.5V

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

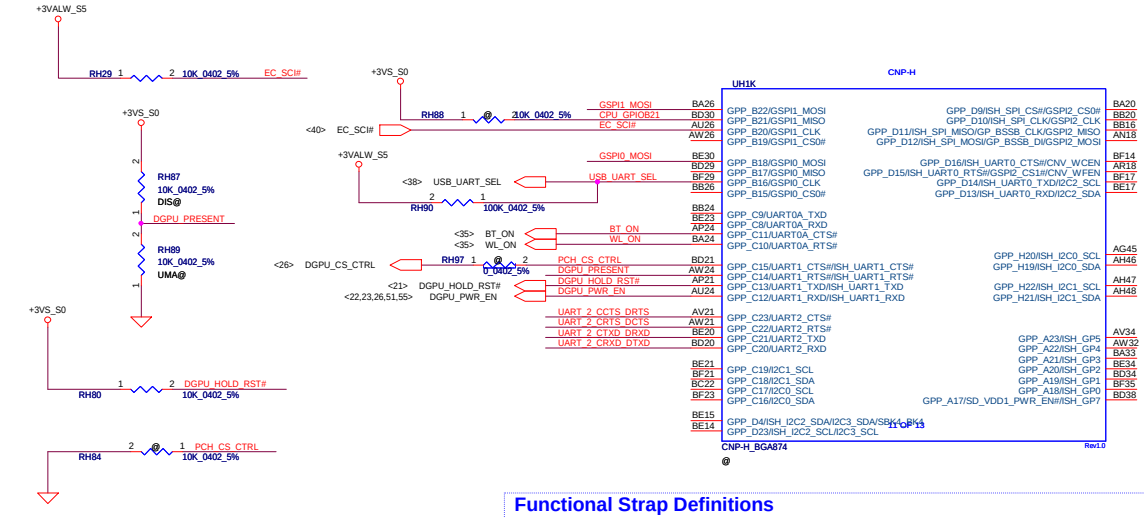
Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.
Title: PCH_HDA\SMBUS\PM
Size: C | Document Number: LA-H011P M/B | Rev: 1.0
Date: Tuesday, August 21, 2018 | Sheet 16 of 61



Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.			
Title	PCH_PCI-E/USB		
Size: Custom	Document Number: LA-H011P M/B		Rev: 1.0
Date: Tuesday, August 21, 2018	Sheet 17 of 61		



Functional Strap Definitions

GSPI0_MOSI
The signal has a weak internal Pull-down.
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
Notes:
1. The internal Pull-down is disabled after PCH_PWROK is high.
2. This signal is in the primary well.

GSPI1_MOSI
This Signal has a weak internal Pull-down.
0: SPI (Default)
1: LPC
Notes:
1. The internal Pull-down is disabled after PCH_PWROK is high.
2. This signal is in the primary well.

Strap Pin

Intel® 300 Series Chipset Preliminary HSIO Lane Assignments

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
USB 3.1 Gen 1 / Gen 2 #1	USB 3.1 Gen 1 / Gen 2 #2	USB 3.1 Gen 1 / Gen 2 #3	USB 3.1 Gen 1 / Gen 2 #4	USB 3.1 Gen 1 / Gen 2 #5	USB 3.1 Gen 1 / Gen 2 #6	USB 3.1 Gen 1 #7	USB 3.1 Gen 1 #8	USB 3.1 Gen 1 #9	USB 3.1 Gen 1 #10	PCIe 3.0 #5	PCIe 3.0 #6	PCIe 3.0 #7	PCIe 3.0 #8	PCIe 3.0 #9	PCIe 3.0 #10	PCIe 3.0 #11	PCIe 3.0 #12	PCIe 3.0 #13	PCIe 3.0 #14	PCIe 3.0 #15	PCIe 3.0 #16	PCIe 3.0 #17	PCIe 3.0 #18	PCIe 3.0 #19	PCIe 3.0 #20	PCIe 3.0 #21	PCIe 3.0 #22	PCIe 3.0 #23	PCIe 3.0 #24
						PCIe 3.0 #1	PCIe 3.0 #2	PCIe 3.0 #3	PCIe 3.0 #4	GbE (LAN)				GbE (LAN)		SATA #0[1]	SATA #1[1] GbE (LAN)	GbE (LAN)	SATA #1	SATA #2	SATA #3	SATA #4	SATA #5						
						x4				x4				x4				x4				x4				x4			
						x2		x2		x2		x2		x2			x2		x2		x2		x2			x2		x2	
						No Remapping				No Remapping				Intel® RST for PCIe Storage				No Remapping				Intel® RST for PCIe Storage				Intel® RST for PCIe Storage			

SKU

H310	USB3.1 Gen 1	USB3.1 Gen 1	USB3.1 Gen 1	USB3.1 Gen1	N/A	N/A	N/A	N/A	N/A	N/A	PCIe LAN	PCIe	PCIe	PCIe	LAN Only	N/A	PCIe	PCIe LAN	SATA LAN	SATA	SATA	SATA	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B360	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1	USB3.1 Gen 1	N/A	N/A	N/A	N/A	PCIe LAN	PCIe	PCIe	PCIe	PCIe LAN	PCIe	PCIe SATA	PCIe SATA LAN	SATA LAN	SATA	SATA	SATA	SATA	SATA	N/A	N/A	PCIe	PCIe	PCIe	PCIe

[1] SATA #0/#1 can be configured to PCIe Ports 11/12 or 13/14.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Title	PCH_UART/I2C		
Size C	Document Number LA-H011P M/B		Rev 1.0
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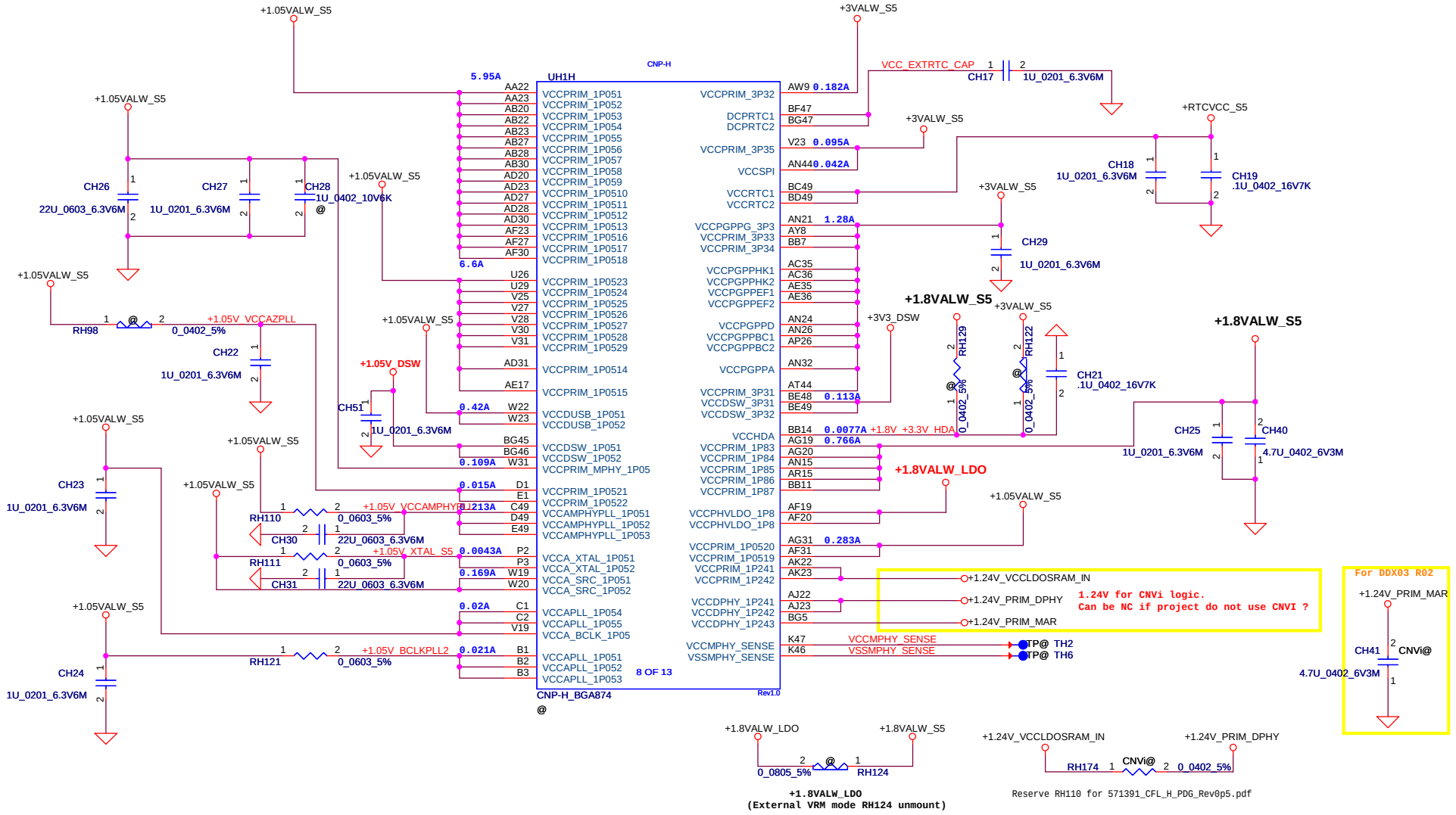
Need to confirm the decoupling and Power requirment



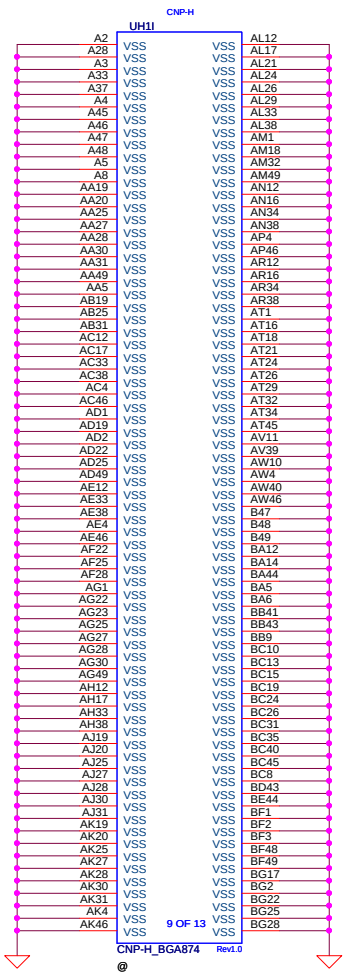
Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

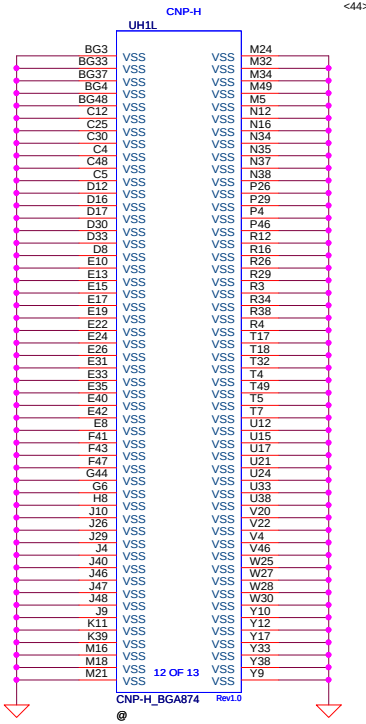
Compal Electronics, Inc.

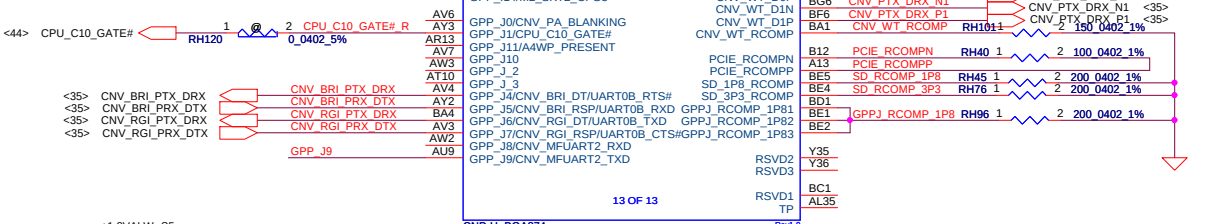
Title: ***PCH_POWER***

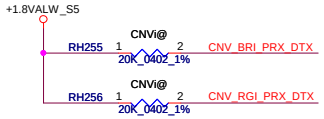
Size	Document Number	Rev
B	LA-H011P M/B	1.0

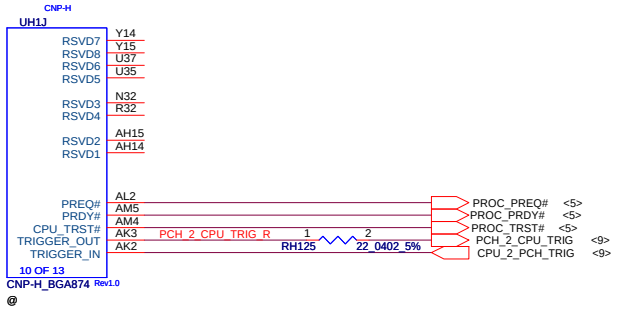
Date: Tuesday, August 21, 2018 Sheet 19 of 61











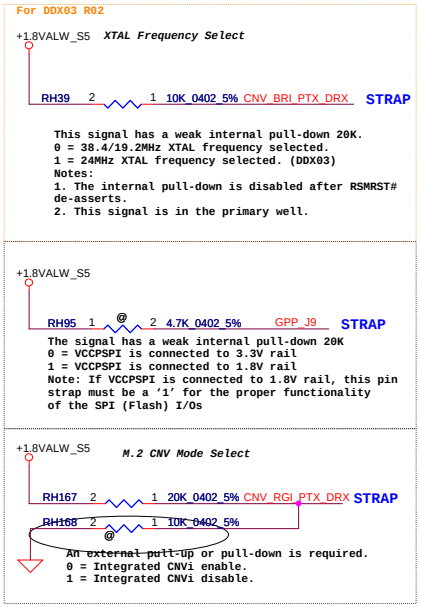


Table 18-1. GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group G (GPP_G)	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8V or 3.3V
Primary Well Group H (GPP_H) Primary Well Group K (GPP_K)	VCCPGPPHK	1.8V or 3.3V
Primary Well Group I (GPP_I)	VCCPRIM_3P3	3.3V Only
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V Only

Note: Except for GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.

Compal Electronics, Inc.			
Title: PCH_GND & CNVi			
Size: Custom	Document Number: LA-H011P M/B		Rev: 1.0
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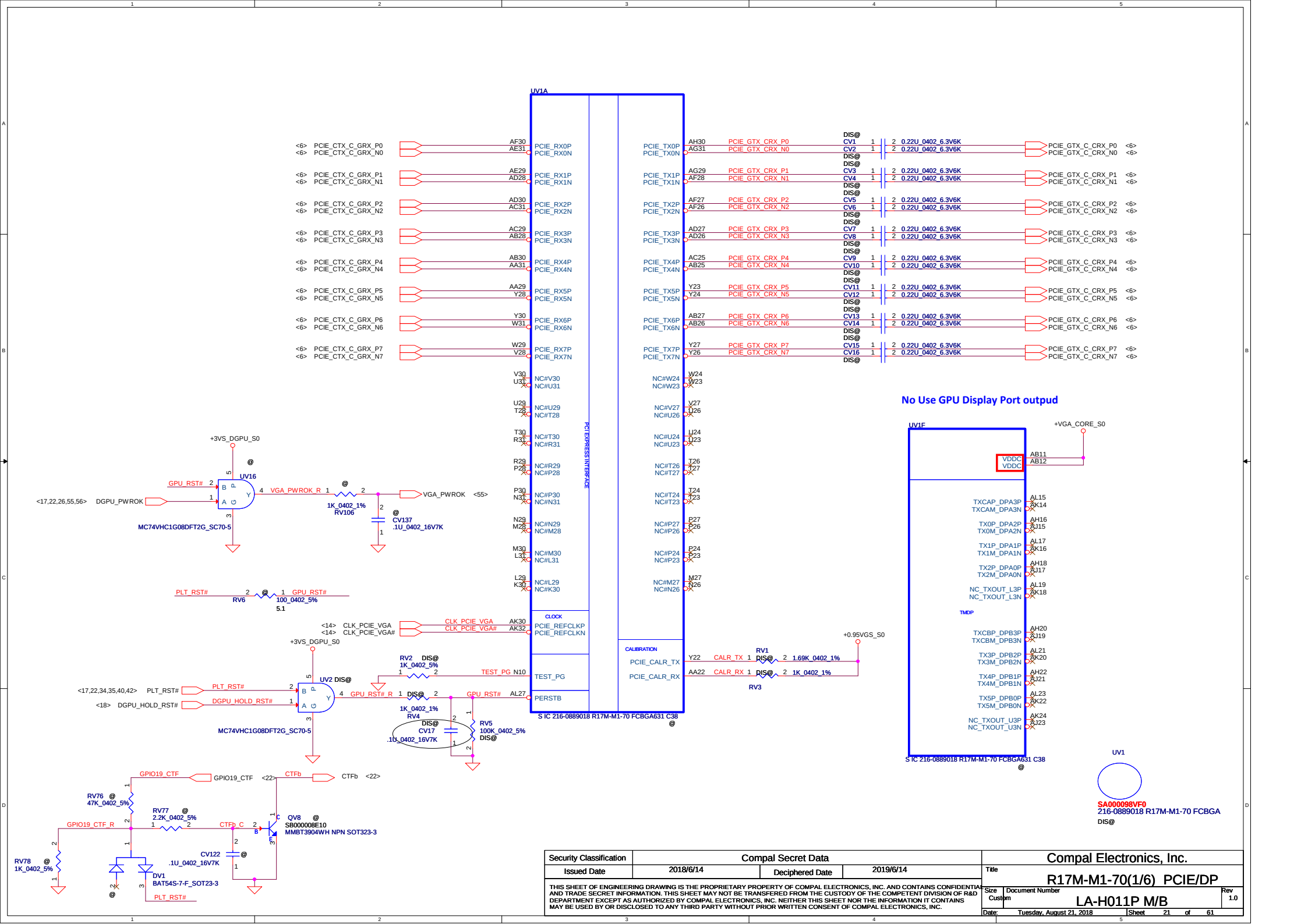


Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: R17M-M1-70(1/6) PCIE/DP

Size	Document Number	Rev
Custom	LA-H011P M/B	1.0

Date: Tuesday, August 21, 2018 Sheet 21 of 61

Meso/M16M-R16M-M2-50	Exo/R16M-M1-30
GPIO_11, 12, and 13 are added back. The following balls cease to work as GPIOs or designated functional pins, and become VDDC: • GPIO_1 • GPIO_2 • GPIO_14_HPD2 • GPIO_18_HPD3 The following ball ceases to work as a GPIO or designated functional pin, and becomes NC: • GPIO_7_BLON	The following balls cease to work as GPIOs or designated functional pins, and become NC: • GPIO_1 • GPIO_2 • GPIO_7_BLON • GPIO_11 • GPIO_12 • GPIO_13 • GPIO_14_HPD2 • GPIO_18_HPD3
"Topaz" allocates 11 more VDDC balls so that the total number of VDDC balls becomes 36. The following functional balls on earlier generations of ASICs are reassigned as the additional VDDC balls: • VARY_BL (AB11) • DIGON (AB12) • GENERCA (AB13) • GENERICC (W9) • DDC2CLK (AC11) • DDC2DATA (AC13) • HPD1 (AC14) • GPIO_1 (U10) • GPIO_2 (T10) • GPIO_18 (W10) • GPIO_14_HPD2 (Y9)	"Jet"/"Sun" has a total of 25 VDDC balls. The 11 balls listed in the "Topaz" column are NC on "Jet"/"Sun".

PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

When PS_2 bit 3=0, PS_0 bits [3:1] define the size of the Primary Memory Aperture as per table opposite

Setting Memory Aperture Size

PS_0[3] romidcfg_2	PS_0[2] romidcfg_1	PS_0[1] romidcfg_0	Memory Aperture Size
0	0	0	128 MB
0	0	1	256 MB
0	1	0	64 MB
0	1	1	Reserved
1	0	0	512 MB-Not Supported
1	0	1	1 GB-Not Supported
1	1	0	2 GB-Not Supported
1	1	1	4 GB-Not Supported

PS_1[3:1]=001
PS_1[5:4]=11

Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=11
AMD recommend 09/25

Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

0402 1% resistors are equired

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

Resistor Divider Lookup Lable

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

MLPS MEMORY ID Setting:

Board_Config[2:0]		Memory Type	Configuration	Channel Size	Vendor P/N	Compal P/N
ID	[2:0]					
0	000	Samsung gDDR5	128Mx32 2PCS	1GB	K4G41325FE-HC28	SA00009TT40
1	001	Hynix gDDR5	128Mx32 2PCS	1GB	H5GC4H24AJR-T2C	SA00008HQ00
2	010	Micron gDDR5	256Mx32 2PCS	2GB	MT51J256M32HF-70:A	SA00009TV00
3	011	Samsung gDDR5	256Mx32 2PCS	2GB	K4G80325FB-HC28	SA00009ZD10
4	100	Hynix gDDR5	256Mx32 3PCS	2GB	H5GC8H24MJR-R0C	SA00009U100

X7668038L01 : RV20 = NC , RV22 = 4.75K
X7668038L02 : RV20 = 8.45K , RV22 = 2K
X7668038L03 : RV20 = 4.53K , RV22 = 2K
X7668038L04 : RV20 = 6.98K , RV22 = 4.99K

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

10/26 Modify

EC Side pull high at page 16

Enable MLPS

ZZZ4 Hynix 2G — H1G@ — Part Number = SA00009U120
ZZZ5 Samsung 2G — S2G@ — Part Number = SA000092D20
ZZZ6 Micron 2G — M2G@ — Part Number = SA00009TV30

Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

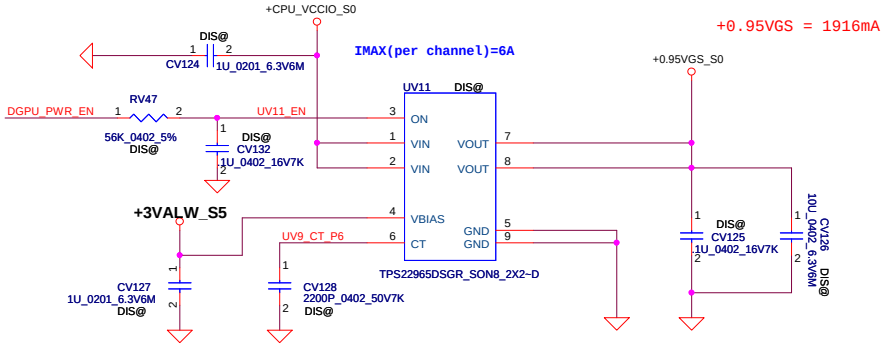
Compal Electronics, Inc.

Title: R17M-M1-70(2/6) MSIC

Size: Custom | Document Number: LA-H011P M/B | Rev: 1.0

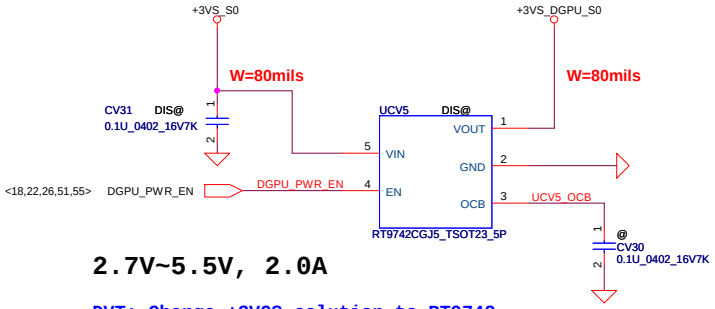
Date: Tuesday, August 21, 2018 | Sheet 22 of 61

+1.8VALW TO +1.8VGS
+0.95VALW TO +0.95VGS
Load switch



1st source : APL3526 (SA00006R100)
2nd source : TPS22965 (SA00005X500)

+3VALW to +3VGS

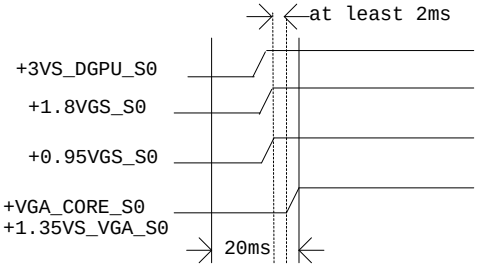


2.7V~5.5V, 2.0A

DVT: Change +3VGS solution to RT9742

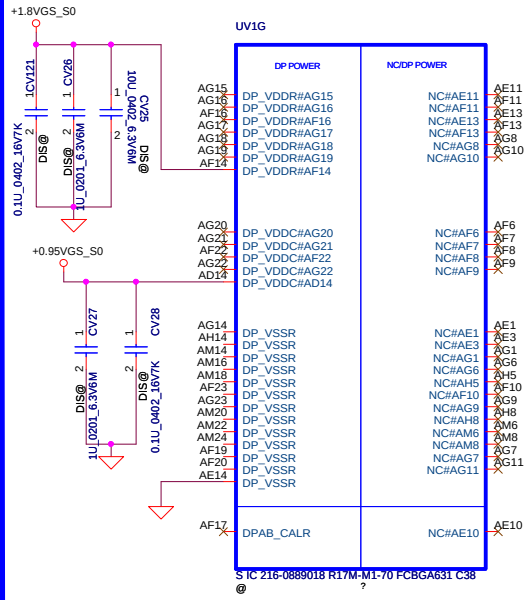
DGPU Power Sequence

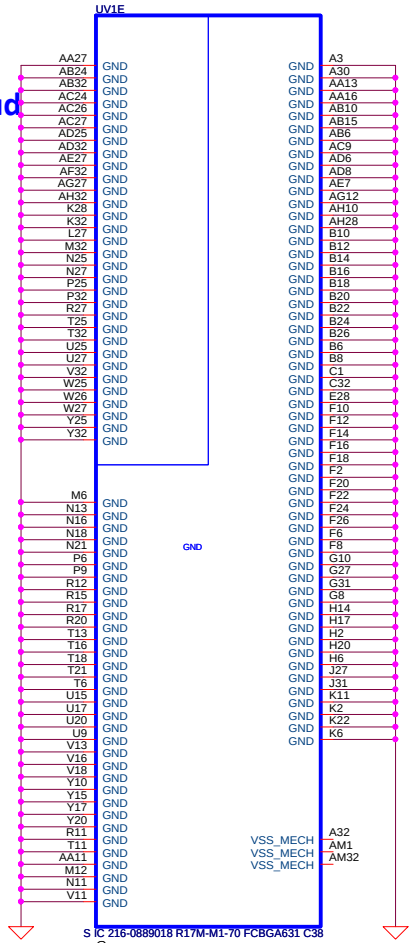
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

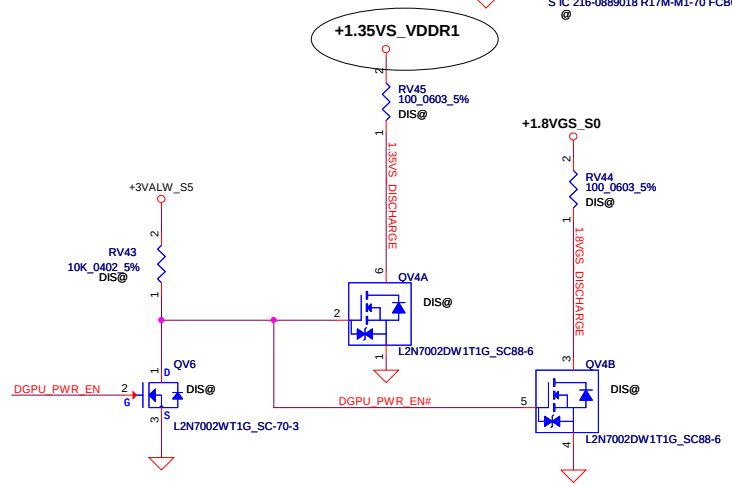


1.the 3.3-V rail ramp up first.
2.the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up

No Use GPU Display Port outpud







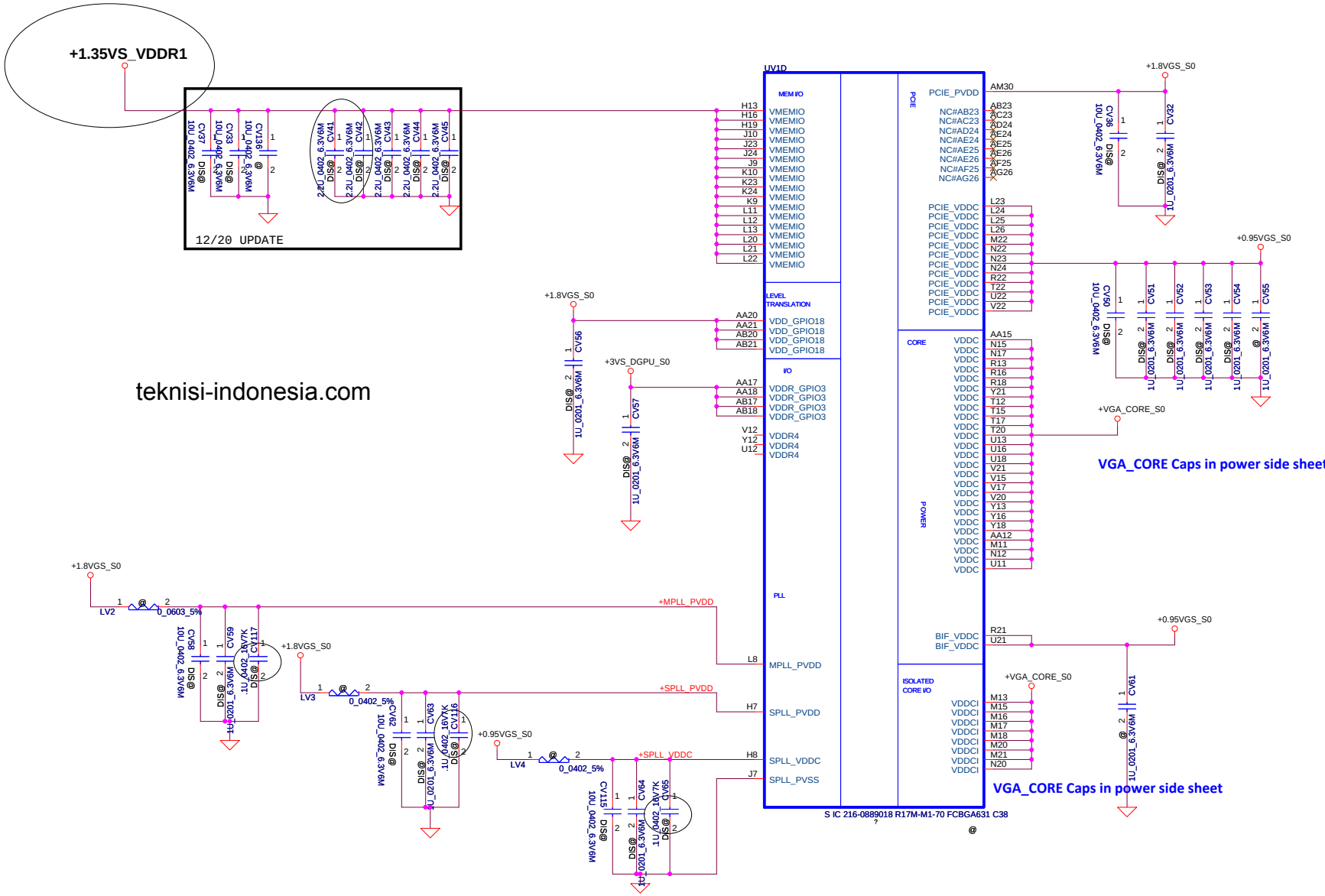
Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: R17M-M1-70 (3/6) PWR/GND

Size: Custom | Document Number: LA-H011P M/B | Rev: 1.0

Date: Tuesday, August 21, 2018 | Sheet 23 of 61



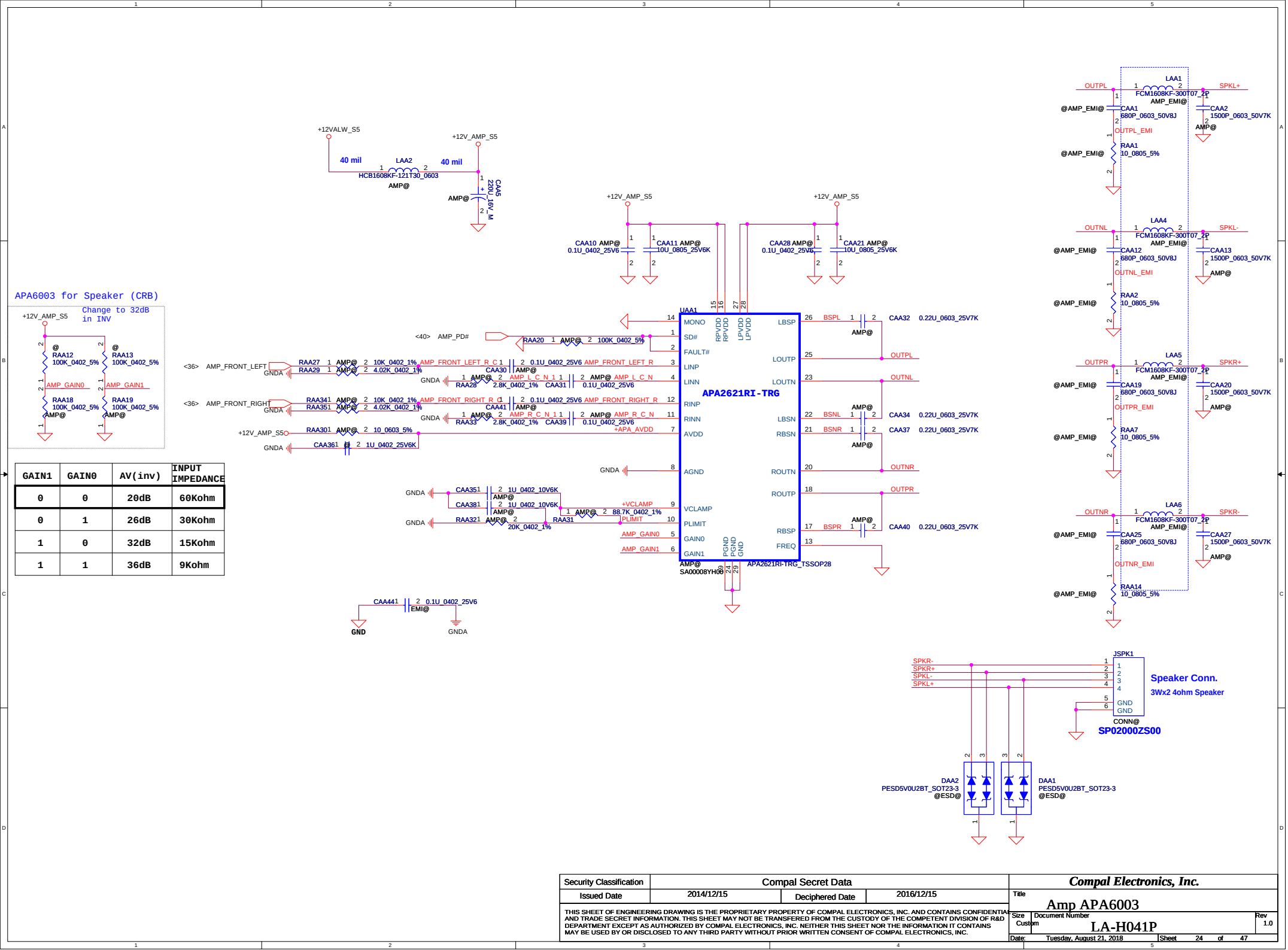
Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: R17M-M1-70(4/6) PWR

Size	Document Number	Rev
Custom	LA-H011P M/B	1.0

Date: Tuesday, August 21, 2018 | Sheet 24 of 61



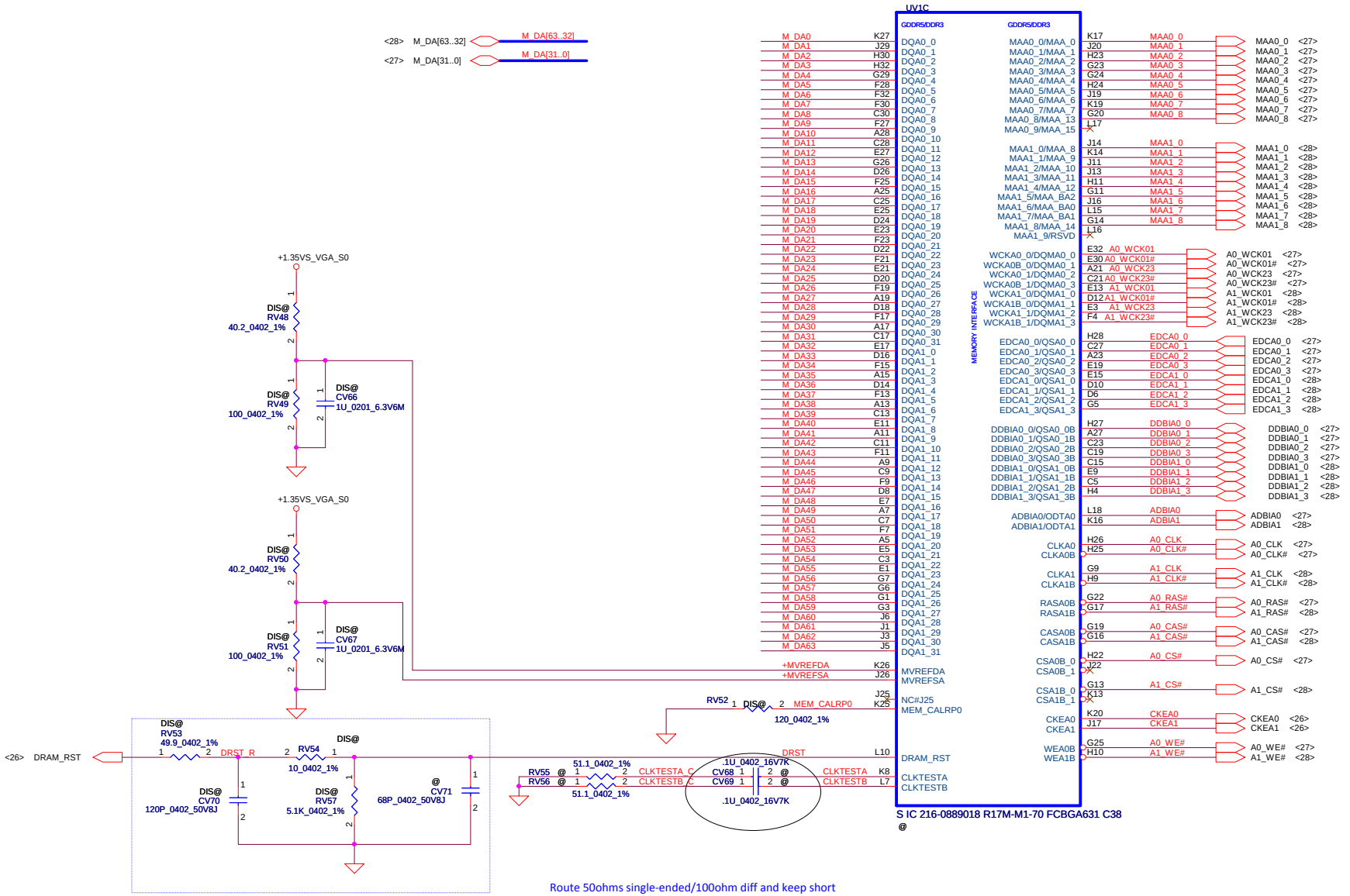
Security Classification	Compal Secret Data		
Issued Date	2014/12/15	Deciphered Date	2016/12/15

Compal Electronics, Inc.

Title: Amp APA6003

Size	Document Number	Rev
Custom	LA-H041P	1.0

Date: Tuesday, August 21, 2018 | Sheet 24 of 47



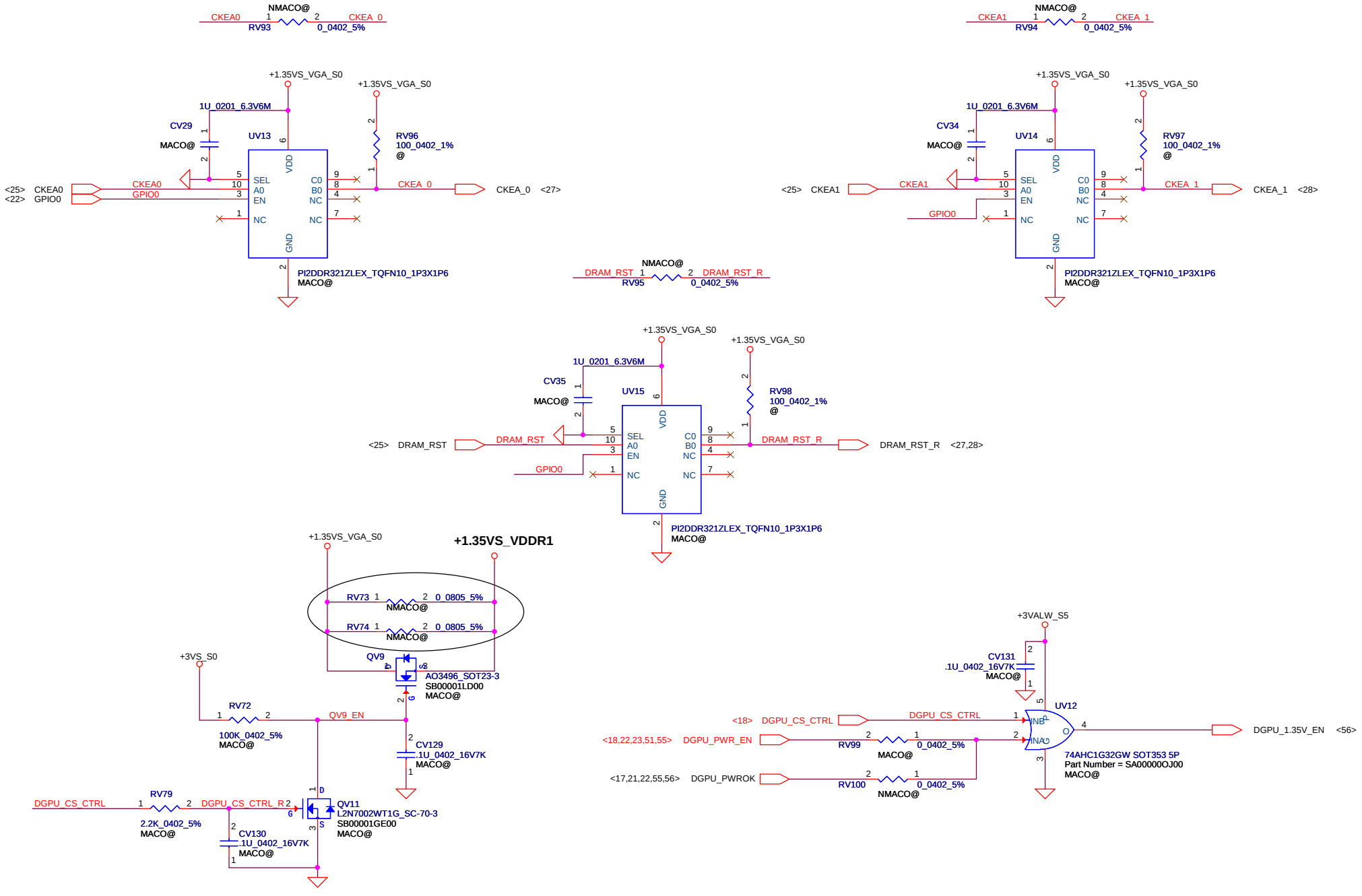
Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: R17M-M1-70(5/6) MEM

Size: Custom | Document Number: LA-H011P M/B | Rev: 1.0

Date: Tuesday, August 21, 2018 | Sheet 25 of 61



Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

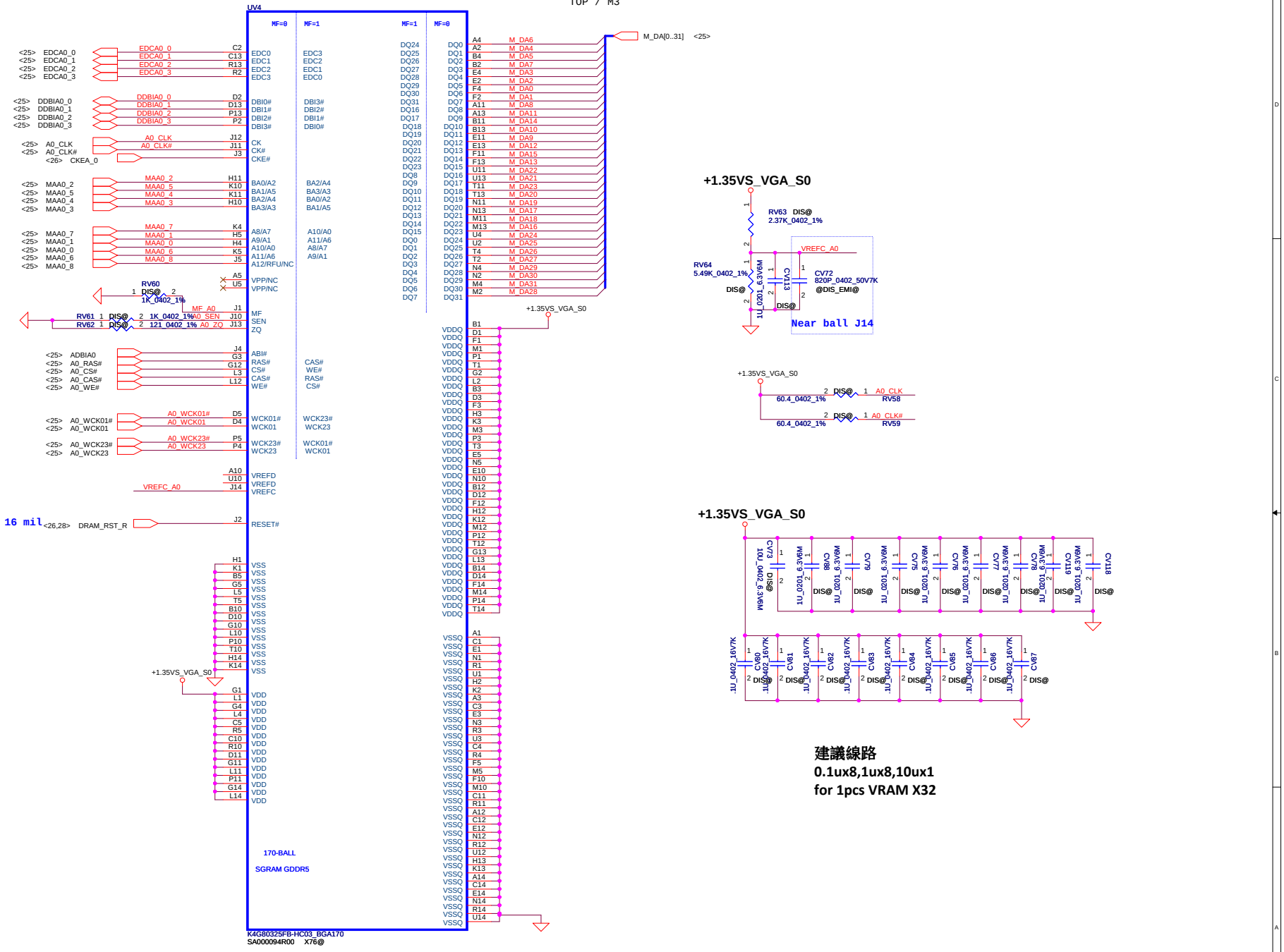
Title: R17M-M1-70(6/6)_VDDR1

Size	Document Number	Rev
Custom	LA-H011P M/B	1.0

Date: Tuesday, August 21, 2018 Sheet 26 of 61

Memory Partition A Lower -32 bits

TOP / M3



Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

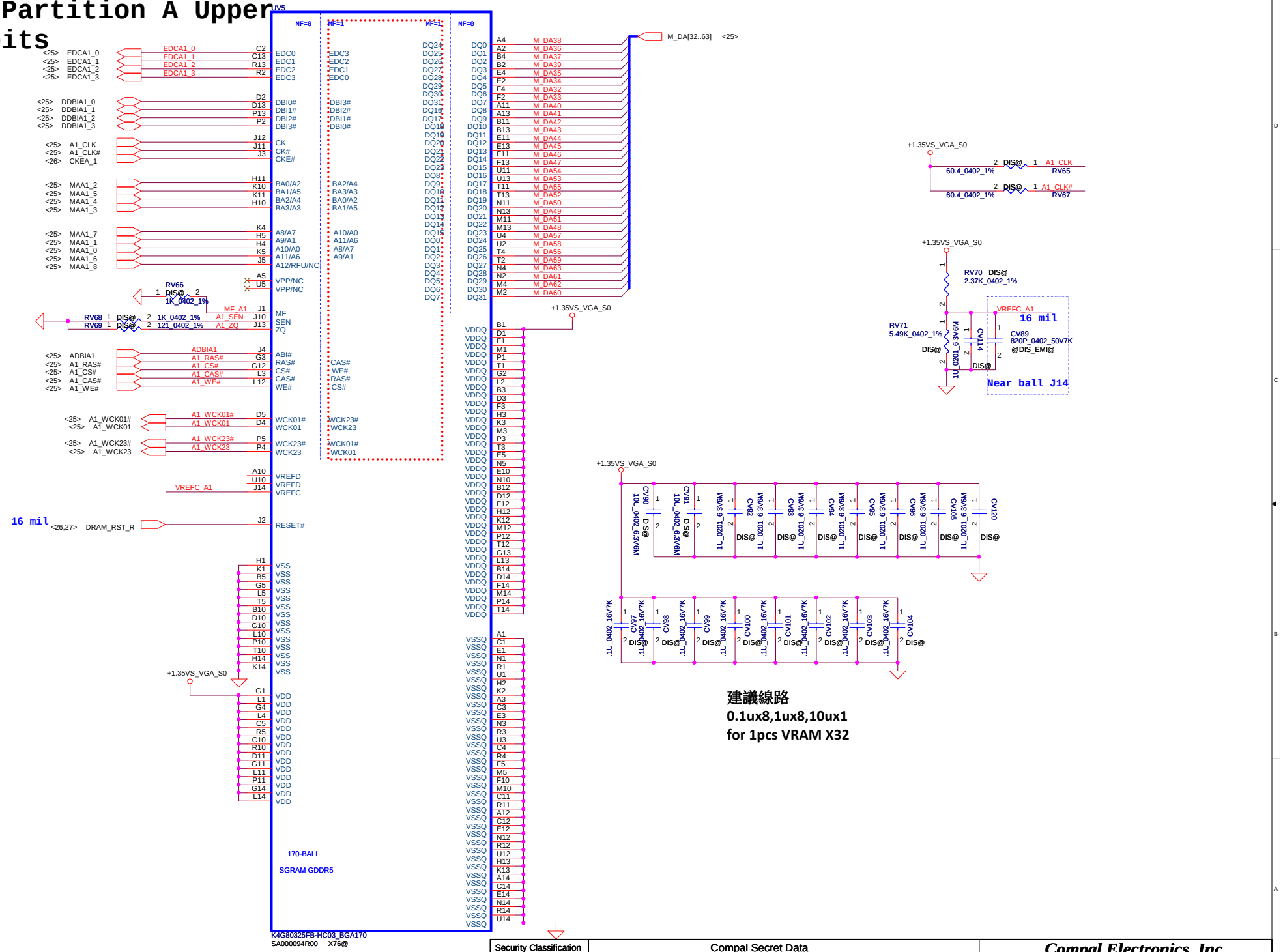
Compal Electronics, Inc.

Title: GDDR5 VRAM A Lower

Size	Document Number	Rev
	LA-H011P M/B	1.0

Date: Tuesday, August 21, 2018 Sheet 27 of 61

Memory Partition A Upper - 32 bits



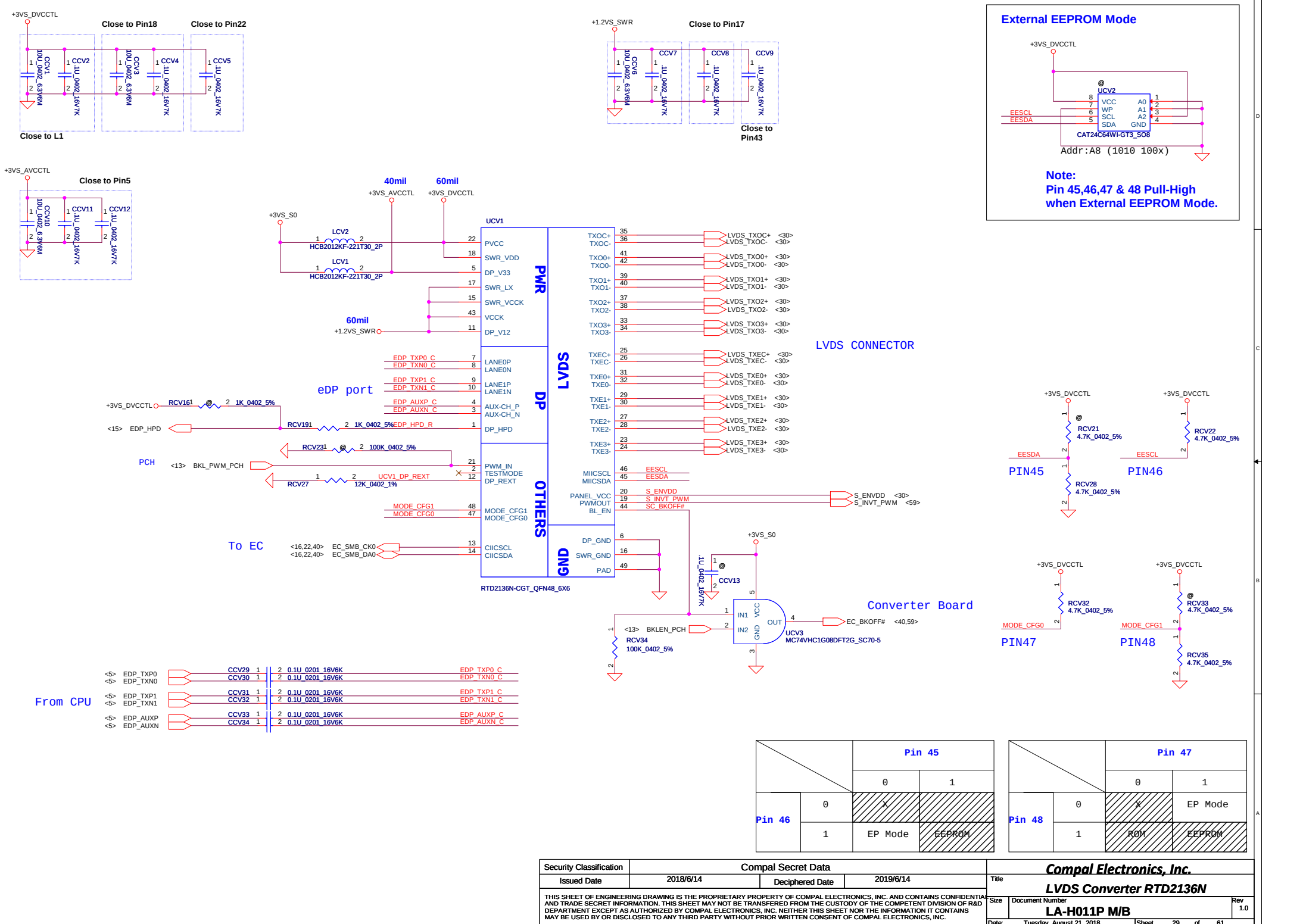
Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: GDDR5_A Upper

Size | Document Number: LA-H011P M/B | Rev: 1.0

Date: Tuesday, August 21, 2018 | Sheet 28 of 61



Security Classification	Compal Secret Data
Issued Date	2018/6/14
Deciphered Date	2019/6/14

Compal Electronics, Inc.	
Title	LVDS Converter RTD2136N
Size	Document Number: LA-H011P M/B
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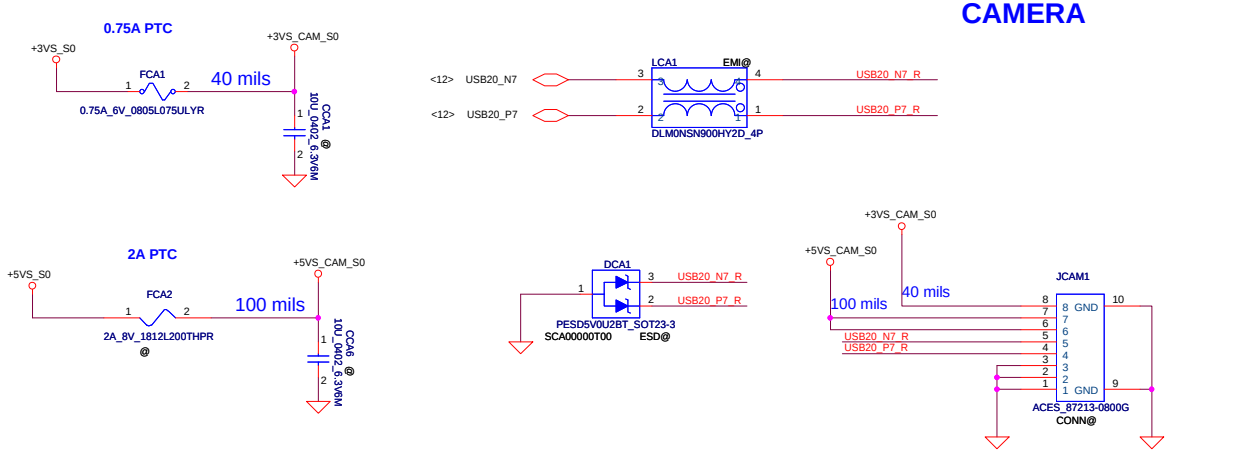

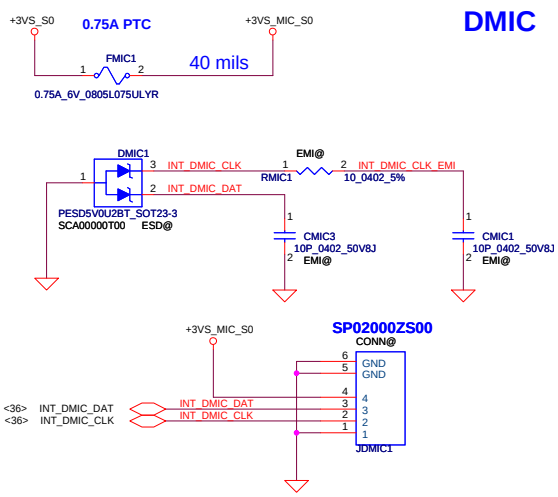

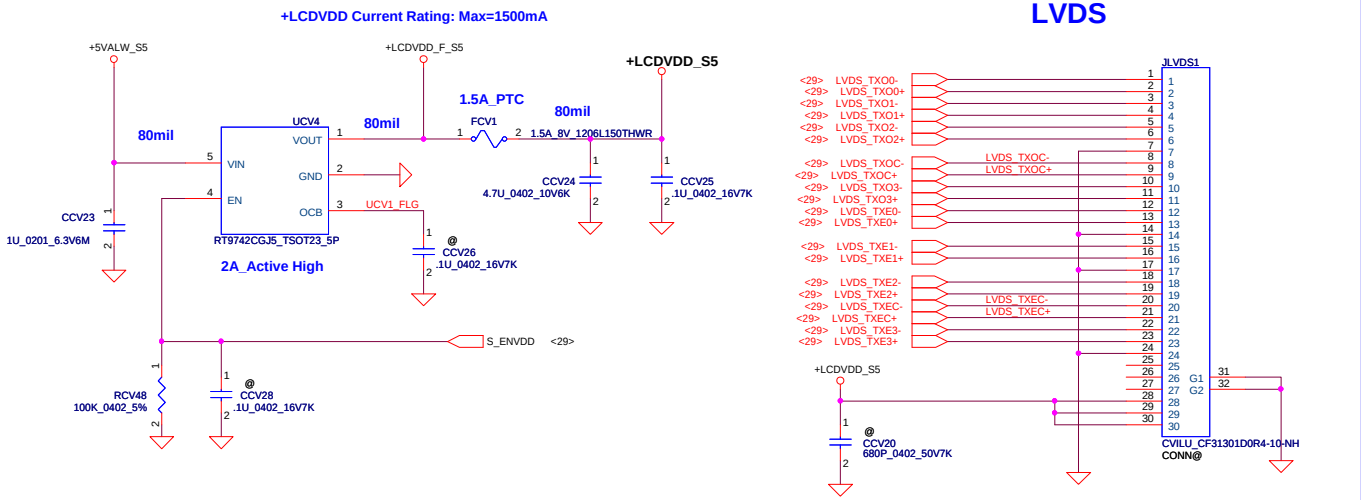

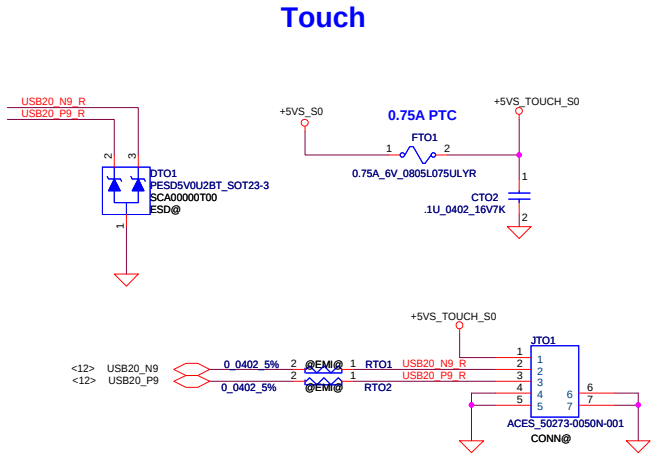

Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: *LVDS/Convertor/CAM/Touch*

Size	Document Number	Rev
Custom	LA-H011P M/B	1.0

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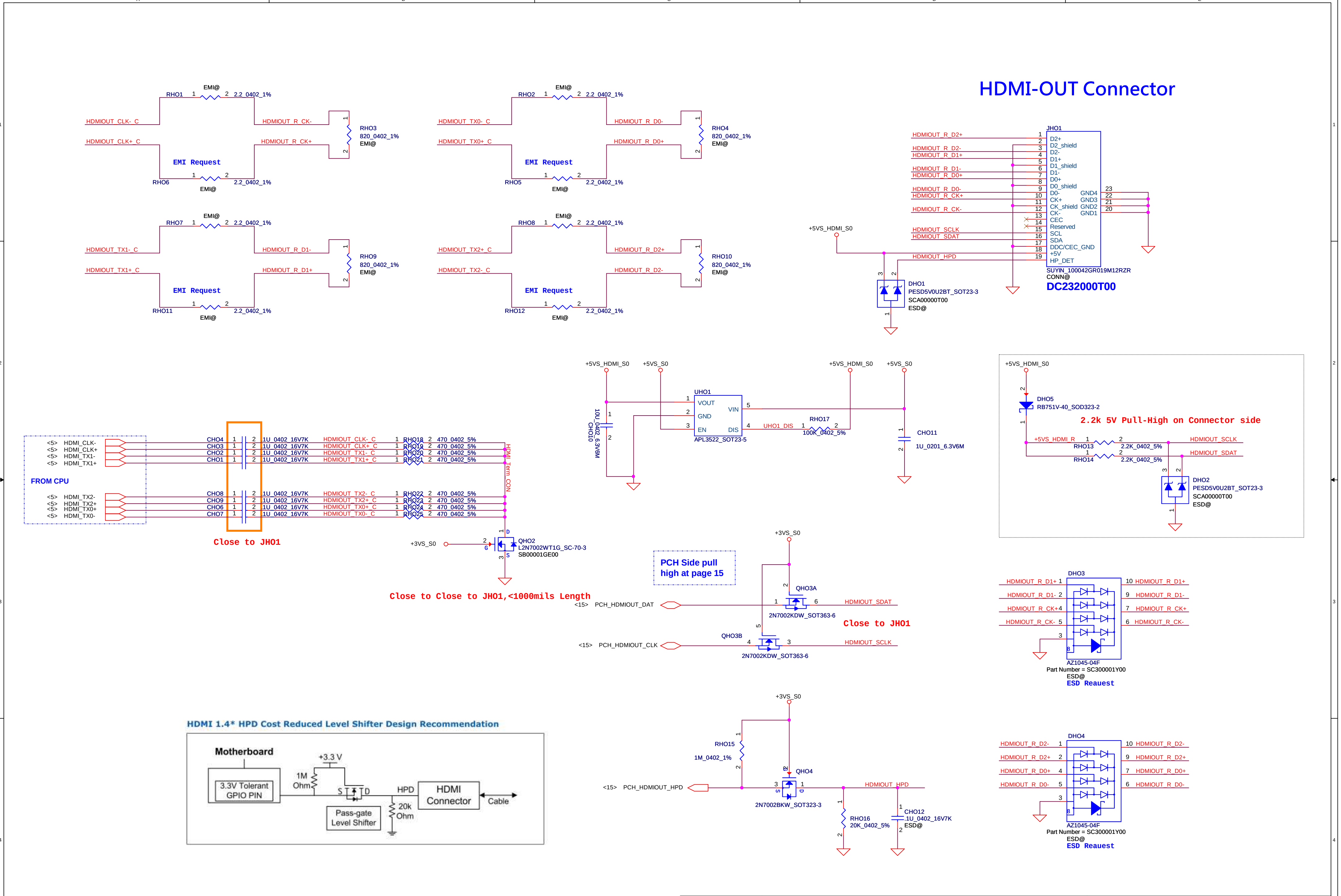
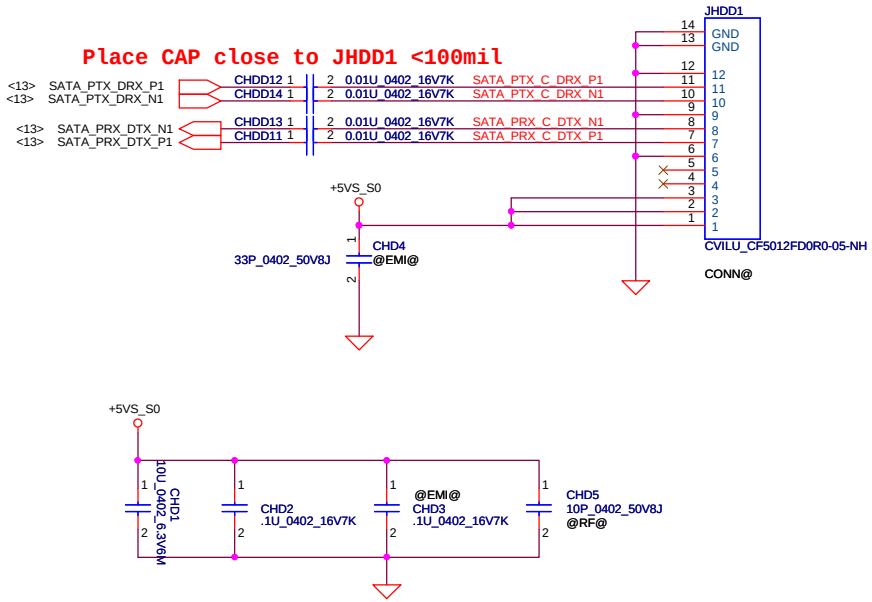


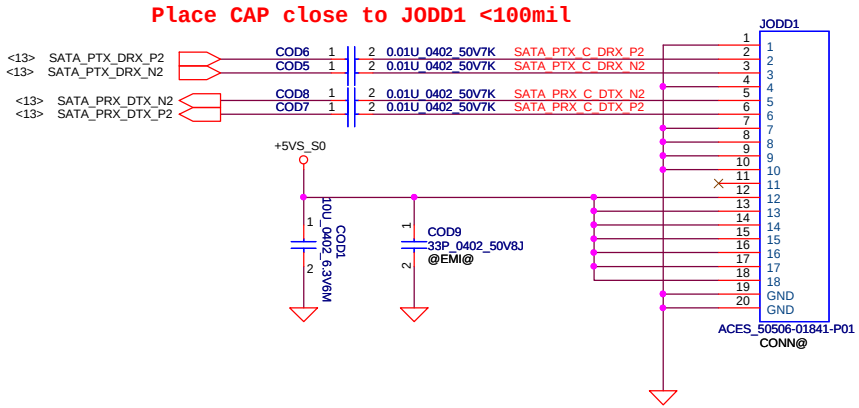
HDMI-OUT Connector
RHO1 1 EMI@ 2 2.2_0402_1%
HDMIOUT_CLK-_C
HDMIOUT_R_CK-
RHO3 820_0402_1% EMI@
HDMIOUT_CLK+_C
HDMIOUT_R_CK+
EMI Request
RHO6 1 2 2.2_0402_1% EMI@
RHO2 1 EMI@ 2 2.2_0402_1%
HDMIOUT_TX0-_C
HDMIOUT_R_D0-
RHO4 820_0402_1% EMI@
HDMIOUT_TX0+_C
HDMIOUT_R_D0+
EMI Request
RHO5 1 2 2.2_0402_1% EMI@
RHO7 1 EMI@ 2 2.2_0402_1%
HDMIOUT_TX1-_C
HDMIOUT_R_D1-
RHO9 820_0402_1% EMI@
HDMIOUT_TX1+_C
HDMIOUT_R_D1+
EMI Request
RHO11 1 2 2.2_0402_1% EMI@
RHO8 1 EMI@ 2 2.2_0402_1%
HDMIOUT_TX2+_C
HDMIOUT_R_D2+
RHO10 820_0402_1% EMI@
HDMIOUT_TX2-_C
HDMIOUT_R_D2-
EMI Request
RHO12 1 2 2.2_0402_1% EMI@
JHO1
D2+ D2_shield D2- D1+ D1_shield D1- D0+ D0_shield D0- CK+ CK_shield CK- CEC Reserved SCL SDA DDC/CEC_GND +5V HP_DET
GND4 GND3 GND2 GND1
HDMIOUT_R_D2+ HDMIOUT_R_D2- HDMIOUT_R_D1+ HDMIOUT_R_D1- HDMIOUT_R_D0+ HDMIOUT_R_D0- HDMIOUT_R_CK+ HDMIOUT_R_CK- HDMIOUT_SCLK HDMIOUT_SDAT HDMIOUT_HPD
+5VS_HDMI_S0
SUYIN_100042GR019M12RZR
CONN@
DC232000T00
DHO1 PESD5V0U2BT_SOT23-3 SCA00000T00 ESD@
FROM CPU
<5> HDMI_CLK-
<5> HDMI_CLK+
<5> HDMI_TX1-
<5> HDMI_TX1+
<5> HDMI_TX2-
<5> HDMI_TX2+
<5> HDMI_TX0+
<5> HDMI_TX0-
CHO4 CHO3 CHO2 CHO1 CHO8 CHO9 CHO6 CHO7 .1U_0402_16V7K
HDMIOUT_CLK-_C HDMIOUT_CLK+_C HDMIOUT_TX1-_C HDMIOUT_TX1+_C HDMIOUT_TX2-_C HDMIOUT_TX2+_C HDMIOUT_TX0+_C HDMIOUT_TX0-_C
RHO18 RHO19 RHO20 RHO21 RHO22 RHO23 RHO24 RHO25 470_0402_5%
HDMI_Term_CON
Close to JHO1
+3VS_S0
QHO2 L2N7002WT1G_SC-70-3 SB00001GE00
Close to Close to JHO1,<1000mils Length
+5VS_HDMI_S0 +5VS_S0
UHO1 VOUT GND EN VIN DIS APL3522_SOT23-5
CHO10 10U_0402_6.3V6M
UHO1_DIS
RHO17 100K_0402_5%
CHO11 1U_0201_6.3V6M
DHO5 RB751V-40_SOD323-2
2.2k 5V Pull-High on Connector side
+5VS_HDMI_R
RHO13 2.2K_0402_5%
RHO14 2.2K_0402_5%
HDMIOUT_SCLK HDMIOUT_SDAT
DHO2 PESD5V0U2BT_SOT23-3 SCA00000T00 ESD@
PCH Side pull high at page 15
+3VS_S0
QHO3A 2N7002KDW_SOT363-6
<15> PCH_HDMIOUT_DAT
HDMIOUT_SDAT
Close to JHO1
QHO3B 2N7002KDW_SOT363-6
<15> PCH_HDMIOUT_CLK
HDMIOUT_SCLK
DHO3
HDMIOUT_R_D1+ HDMIOUT_R_D1- HDMIOUT_R_CK+ HDMIOUT_R_CK-
AZ1045-04F
Part Number = SC300001Y00
ESD@
ESD Reauest
HDMI 1.4* HPD Cost Reduced Level Shifter Design Recommendation
Motherboard
3.3V Tolerant GPIO PIN
+3.3 V
1M Ohm
Pass-gate Level Shifter
20k Ohm
HPD
HDMI Connector
Cable
+3VS_S0
RHO15 1M_0402_1%
QHO4 2N7002BKW_SOT323-3
<15> PCH_HDMIOUT_HPD
HDMIOUT_HPD
RHO16 20K_0402_5%
CHO12 .1U_0402_16V7K ESD@
DHO4
HDMIOUT_R_D2- HDMIOUT_R_D2+ HDMIOUT_R_D0+ HDMIOUT_R_D0-
AZ1045-04F
Part Number = SC300001Y00
ESD@
ESD Reauest

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/6/14	Deciphered Date	2019/6/14	Title: HDMI IN
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size / Document Number: LA-H011P M/B / Rev 1.0
				Date: Tuesday, August 21, 2018 / Sheet 31 of 61

SATA HDD Conn.



SATA ODD Conn



Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: ***HDD***

Size	Document Number	Rev
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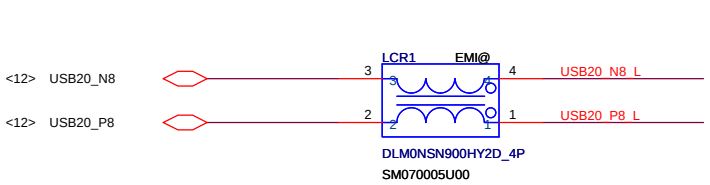
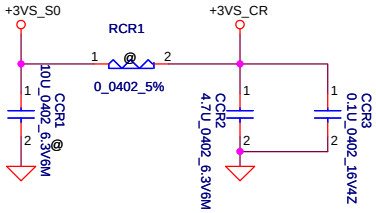
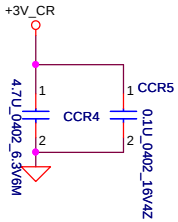
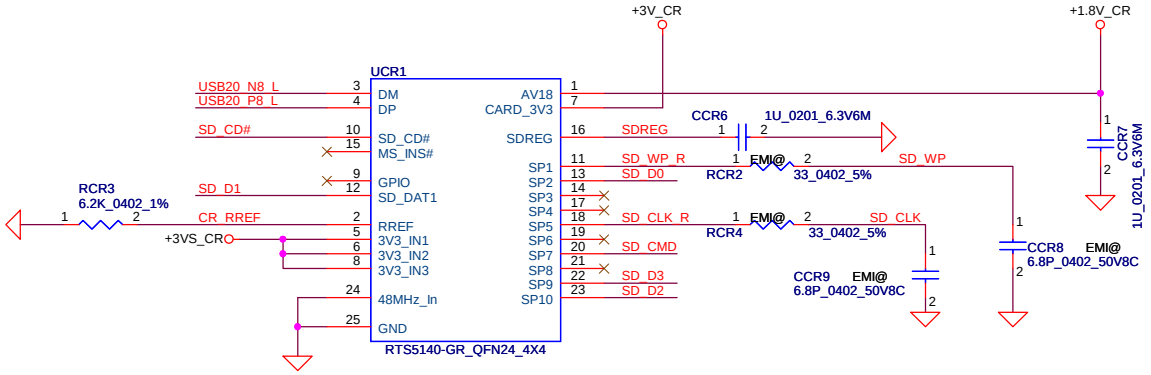
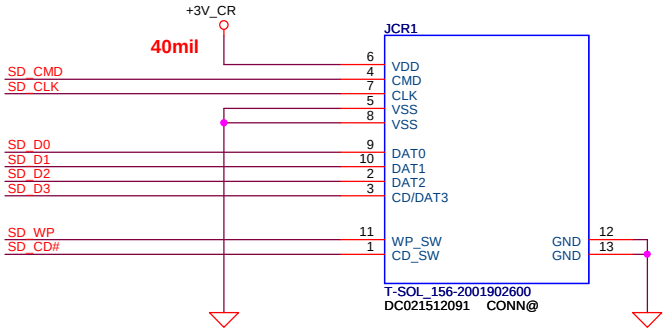






CCR4,CCR5 place close to JCR1.6





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Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: ***CardReader RTS5176***

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WOL circuit (Connect +3V_LAN to +3VALW)

+3VALW_S5 — 60mil — JUML1 @ JUMP_43X39 — 60mil — +3.3V_LAN_S5

300mA,120ohm

+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

Power (Decoupling Cap.)

40 mils — Close to Pin 11,23

+3.3V_LAN_S5
- CL1 1 2 .1U_0402_16V7K
- CL2 1 2 .1U_0402_16V7K
- @EMI@ CL5 1 2 4.7U_0402_6.3V6M
- @EMI@ CL8 1 2 4.7U_0402_6.3V6M
- CL3 1 2 .1U_0402_16V7K

Close to Pin 32

- @EMI@ CL10 1 2 .1U_0402_16V7K
- @EMI@ CL11 1 2 .1U_0402_16V7K
- @EMI@ CL21 1 2 .1U_0402_16V7K

Close to Pin 32 on TOP side

60 mils — Close to pin 3,8,30,24

+LAN_VDDREG
- CL4 1 2 .1U_0402_16V7K
- CL6 1 2 .1U_0402_16V7K
- CL7 1 2 .1U_0402_16V7K
- CL9 1 2 .1U_0402_16V7K

LED Status

WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	

always on

blinking

8111H capacitor

+3.3V_LAN_S5 — Close to pin 22

+LAN_VDDREG — +LAN_VDDREG

- @ CL12 1 2 1U_0201_6.3V6M
- CL20 1 2 .1U_0402_16V7K

CL13, CL14 need colse to UL1

CL15, CL16 need colse to UH1

UL1 (RTL8111H-CG_QFN32_4X4)

<12> PCIE_PRX_LANTXP	CL13 1 2 .1U_0402_16V7K	PCIE_PRX_C_LANTXP	17 HSOP
<12> PCIE_PRX_LANTXN	CL14 1 2 .1U_0402_16V7K	PCIE_PRX_C_LANTXN	18 HSON
<12> PCIE_PTX_LANRXP	CL15 1 2 .1U_0402_16V7K	PCIE_PTX_C_LANRXP	13 HSIP
<12> PCIE_PTX_LANRXN	CL16 1 2 .1U_0402_16V7K	PCIE_PTX_C_LANRXN	14 HSIN
<14> CLK_PCIE_LAN		CLK_PCIE_LAN	15 REFCLK_P
<14> CLK_PCIE_LAN#		CLK_PCIE_LAN#	16 REFCLK_N
		LAN_CLKREQ#_R	12 CLKREQB
<40> PCIE_WAKE#			21 LANWAKEB
		ISOLATE#	20 ISOLATEB
<17,21,22,35,40,42> PLT_RST#			19 PERSTB
+3.3V_LAN_S5	RL5 2.49K_0402_1%	UL1_RSET_P31	23 VDDREG / 31 RSET
		LAN_X2	29 CKXTAL2
		LAN_X1	28 CKXTAL1
			33 GND

AVDD10 (3, 8, 30), AVDD33 (11, 32), DVDD10 (22)

1	LAN_MIDI0+	CRL1 1 2 EMI@ 0.1U_0402_25V6	LAN_MIDI0+_C
2	LAN_MIDI0-	CRL2 1 2 EMI@ 0.1U_0402_25V6	LAN_MIDI0-_C
4	LAN_MIDI1+	CRL3 1 2 EMI@ 0.1U_0402_25V6	LAN_MIDI1+_C
5	LAN_MIDI1-	CRL4 1 2 EMI@ 0.1U_0402_25V6	LAN_MIDI1-_C
6	LAN_MIDI2+	CRL5 1 2 EMI@ 0.1U_0402_25V6	LAN_MIDI2+_C
7	LAN_MIDI2-	CRL6 1 2 EMI@ 0.1U_0402_25V6	LAN_MIDI2-_C
9	LAN_MIDI3+	CRL7 1 2 EMI@ 0.1U_0402_25V6	LAN_MIDI3+_C
10	LAN_MIDI3-	CRL8 1 2 EMI@ 0.1U_0402_25V6	LAN_MIDI3-_C

MDIP0, MDIN0, MDIP1, MDIN1, MDIP2, MDIN2, MDIP3, MDIN3

25	LAN_LED_ORG#	TP@ TL1
26	LAN_PHY_DIS#	
27	LAN_LED_YEL#	TP@ TL2

LED2, LED1/GPIO, LED0 — LAN_PHY_DIS# <40>

TP@ TL3

+LAN_VDDREG — 24 REGOUT

33 GND

+3VS_S0 — RL3 1K_0402_5% — RL6 15K_0402_5%

+3.3V_LAN_S5 — RL1 10K_0402_5%

RL5 2.49K_0402_1%

8111H LAN chip

PCH Side pull high at page 14

+3VS_S0 — +3.3V_LAN_S5 — RL8 10K_0402_5%

<14> CLKREQ_LAN# — QL1 L2N7002WT1G_SC-70-3 SB00001GE00 — LAN_CLKREQ#_R

+3.3V_LAN_S5 — RL13 @ 10K_0402_5% — LAN_PHY_DIS#

LAN_X1 — RL10 1M_0402_5% — LAN_X2

YL1 25MHZ_10PF_X3G025000DA1H-X

CL18 10P_0402_50V8J — CL19 10P_0402_50V8J

DL1 ESD@ AZC099-04S SC300001G00

LAN_MIDI0+_C	I/O2	I/O4 LAN_MIDI1-_C
GND		VDD +3.3V_LAN_S5 (RL14 0_0402_5%)
LAN_MIDI1+_C	I/O1	I/O3 LAN_MIDI0-_C

DL2 ESD@ AZC099-04S SC300001G00

LAN_MIDI2+_C	I/O2	I/O4 LAN_MIDI3-_C
GND		VDD +3.3V_LAN_S5 (RL15 0_0402_5%)
LAN_MIDI3+_C	I/O1	I/O3 LAN_MIDI2-_C

JRJ1 CONN@ SP011312232

LAN_MIDI0+_C	1	TD1+ R1
LAN_MIDI0-_C	2	TD1- R2
LAN_MIDI1+_C	3	TD2+ R3
LAN_MIDI1-_C	4	TD2- R4
JRJ1_CT_R5R6	5	CT R5
	6	CT R6
LAN_MIDI2+_C	7	TD3+ R7
LAN_MIDI2-_C	8	TD3- R8
LAN_MIDI3+_C	9	TD4+ R9
LAN_MIDI3-_C	10	TD4- R10
	11	L1
	12	L2
	13	GND
	14	GND

RL4 0_0402_5% — CL17 .1U_0402_16V7K EMI@

Yellow — RL7 510_0402_5% — LAN_LED_YEL# — LAN_LED_YEL#_R

20mils

+3.3V_LAN_S5

+3.3V_LAN_S5 — LAN_LED_YEL# — DL3 PESD5V0U2BT_SOT23-3 SCA00000T00 ESD@

RL11 1 @ 2 0_0805_5%

RL12 1 @ 2 0_0805_5%

LAN_GND

LAN_GND

Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: LAN RTL8111G/H

Size: Custom | Document Number: LA-H011P M/B | Rev: 1.0

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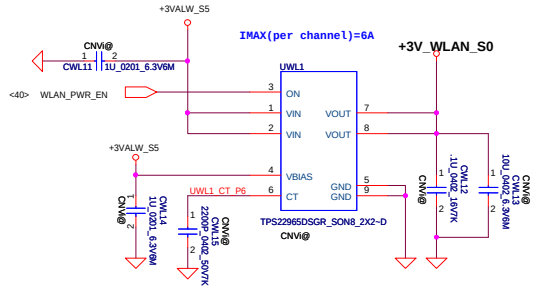
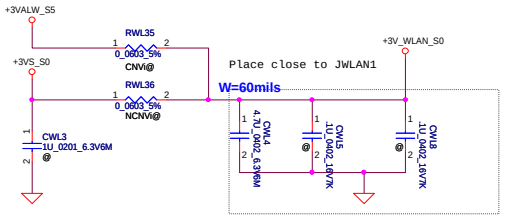
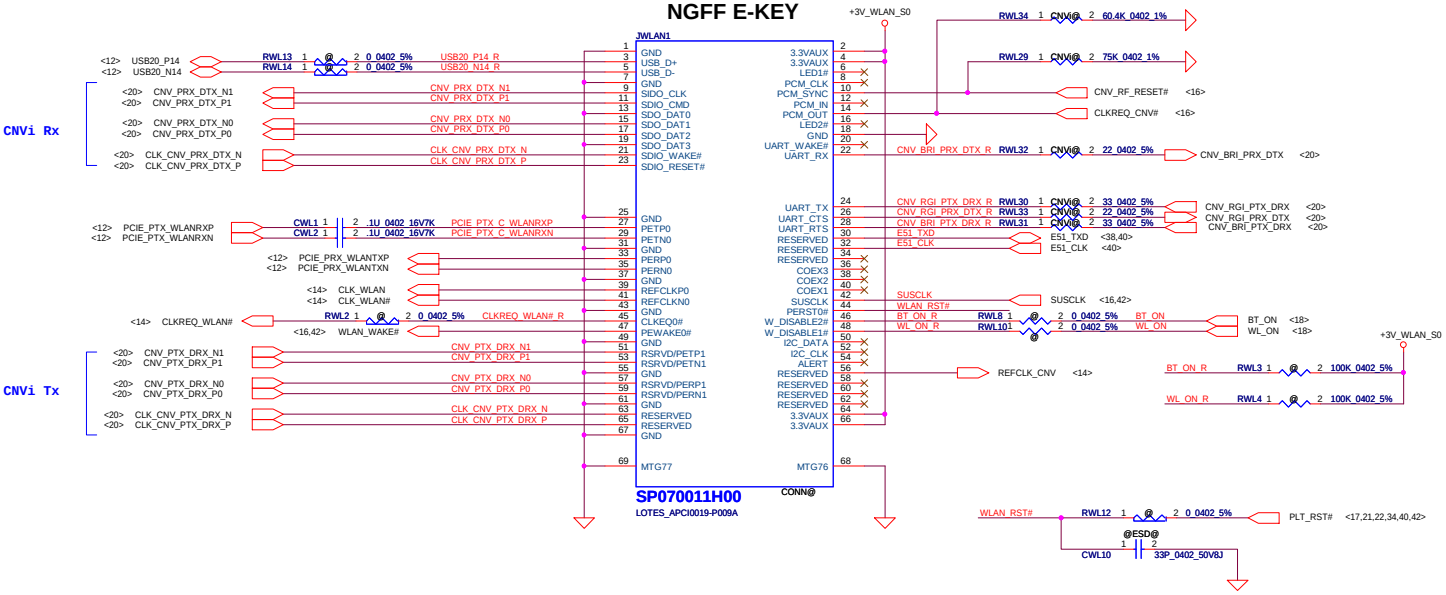
WLAN (WIFI/BT Combo)





WLAN Conn.

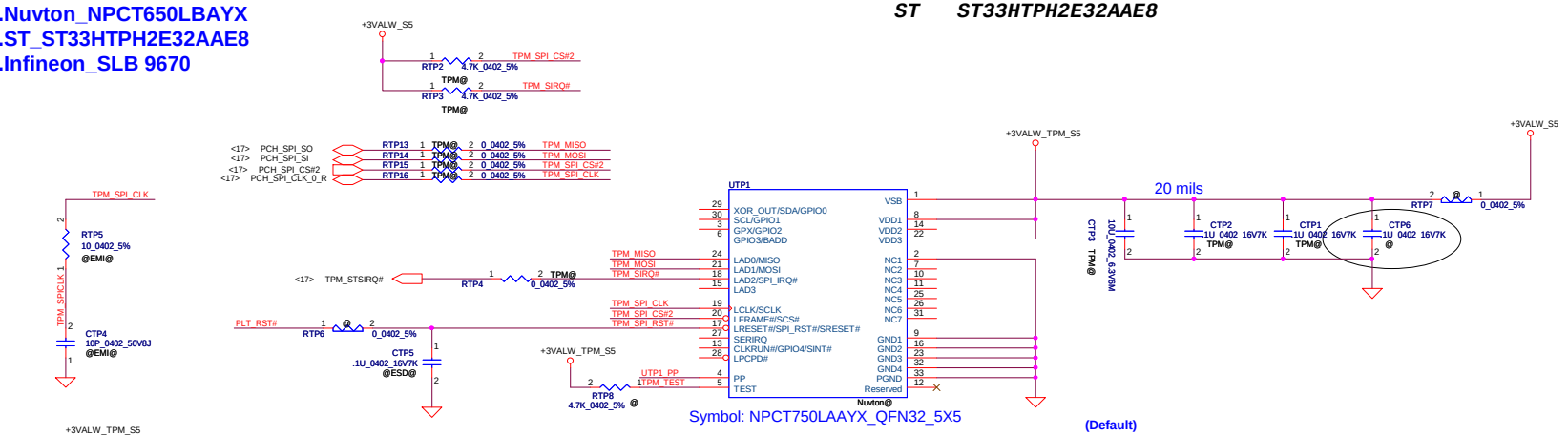
NGFF E-KEY



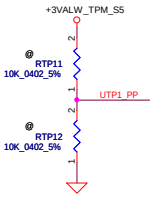
TPM 2.0 Co-lay

1.Nuvton_NPCT650LBAYX
2.ST_ST33HTPH2E32AAE8
3.Infineon_SLB 9670

NEW PART: Nuvoton NPCT650LBAYX (Default)
Infineon SLB 9670
ST ST33HTPH2E32AAE8



Symbol: NPCT750LAAYX_QFN32_5X5



TPM/TCM IC

(Default)

Pop / Un-pop For Co-lay	RTP1	RTP10	BOM Config
Nuvton_NPCT650LBAYX (SPI)	V	V	Nuvton@+TPM@
ST_ST33HTPH2E32AAE8(SPI)	X	X	ST@+TPM@
Infineon_SLB 9670(SPI)	X	X	Infineon@+TPM@

Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.			
Title	WLAN (NGFF) / TPM		
Size	Document Number		Rev
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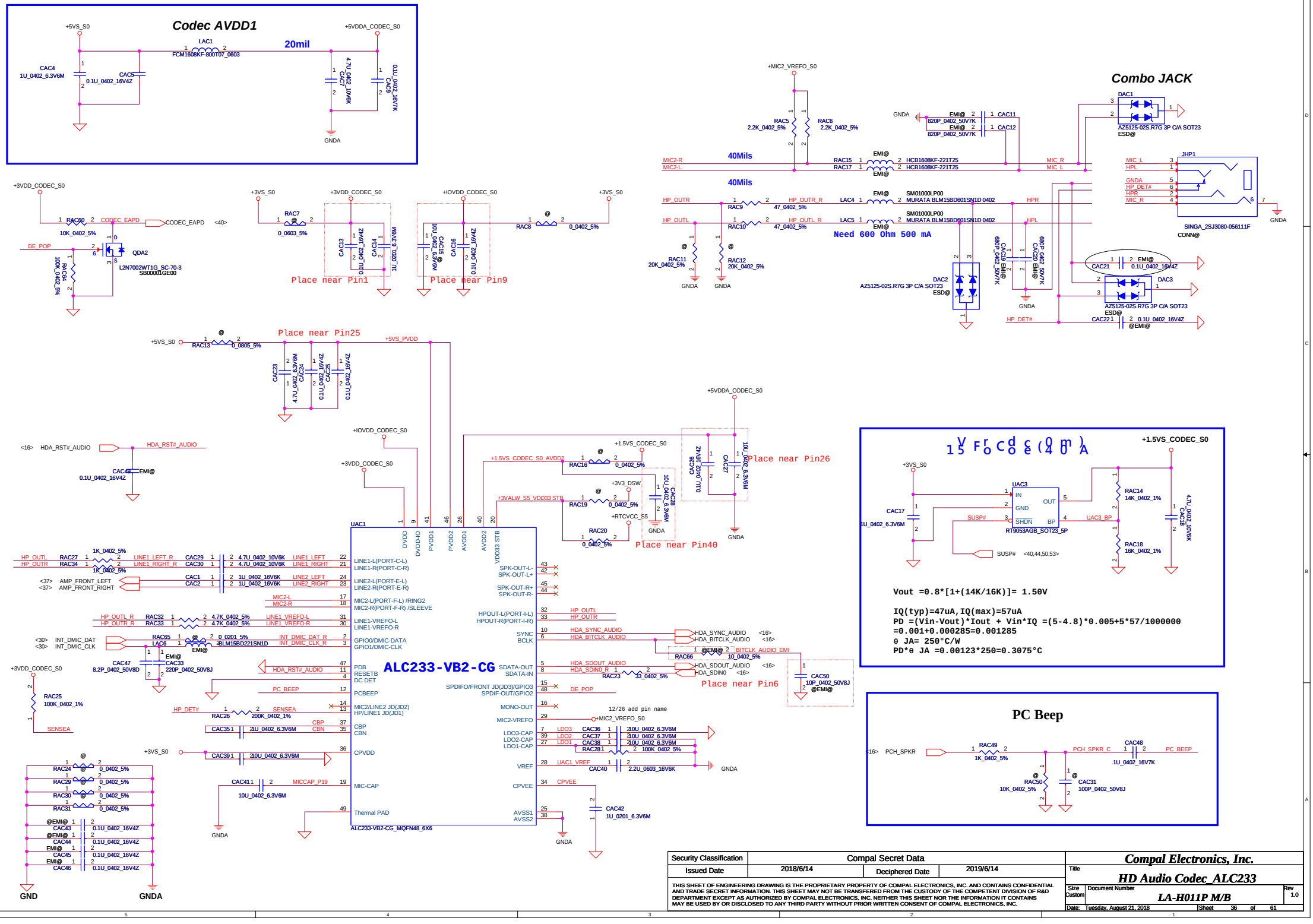

Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: **HD Audio Codec_ALC233**

Size	Document Number	Rev
Custom	LA-H011P M/B	1.0

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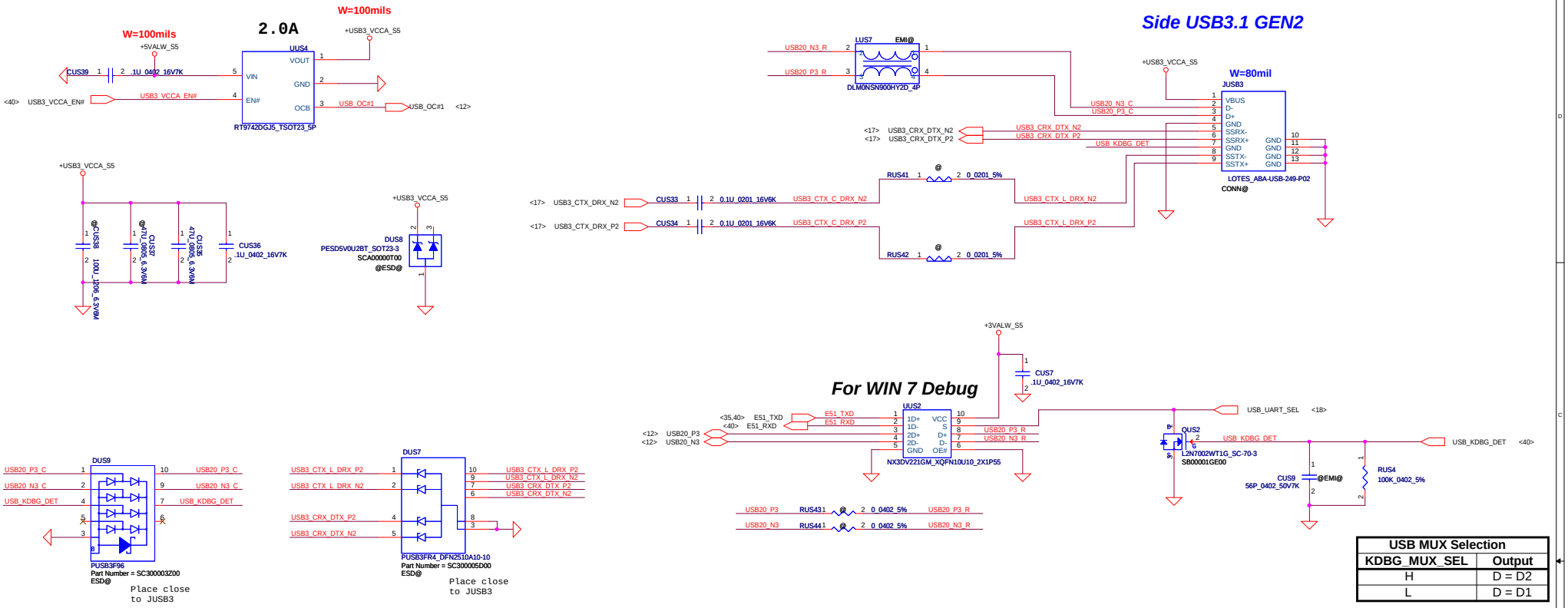

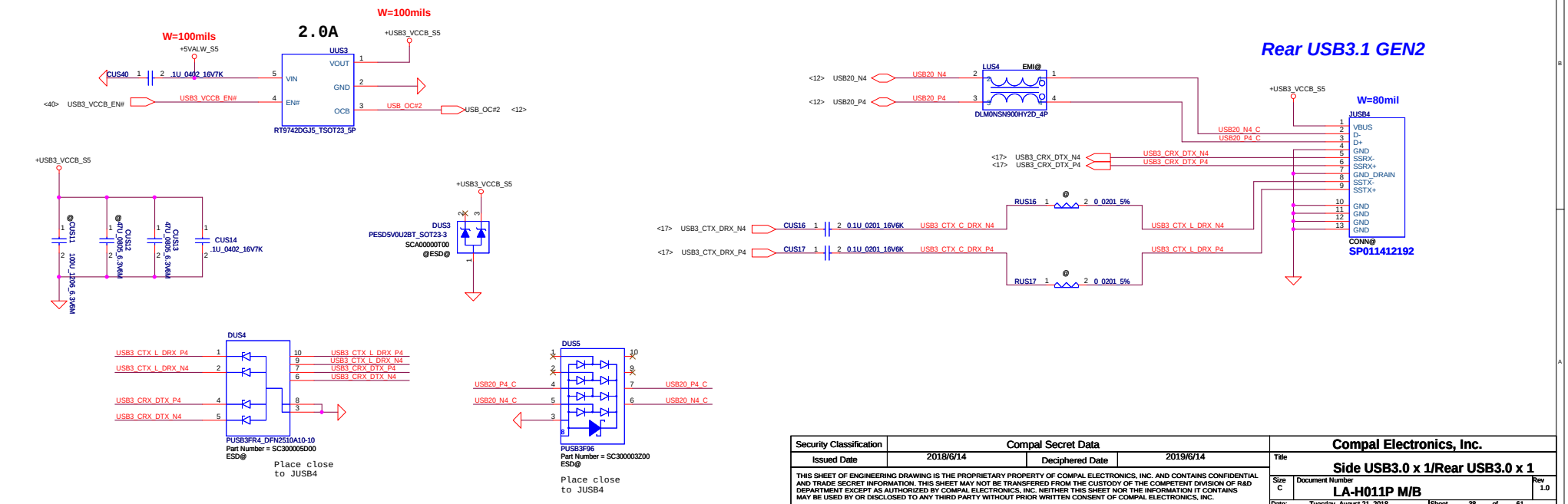

Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: Side USB3.0 x 1/Rear USB3.0 x 1

Size	Document Number	Rev
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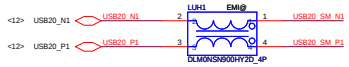
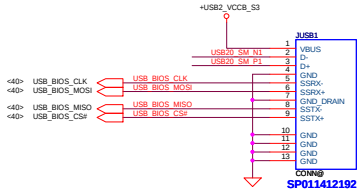
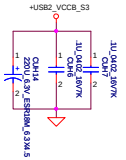
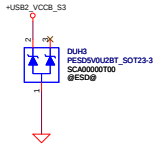
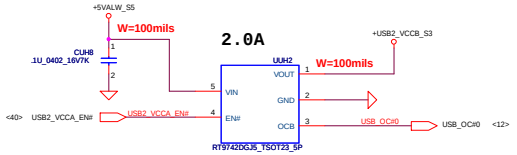
Rear USB2.0 Conn.



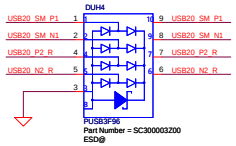




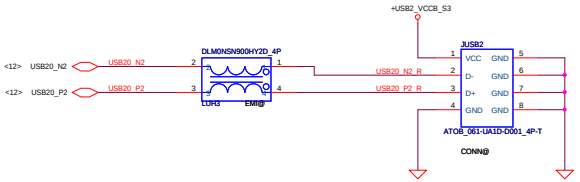


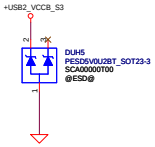


Rear USB2.0 Conn.



Place close to JUSB1 and JUSB2





Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: Rear USB2.0 x 3

Size	Document Number	Rev
Custom	LA-H011P M/B	1.0

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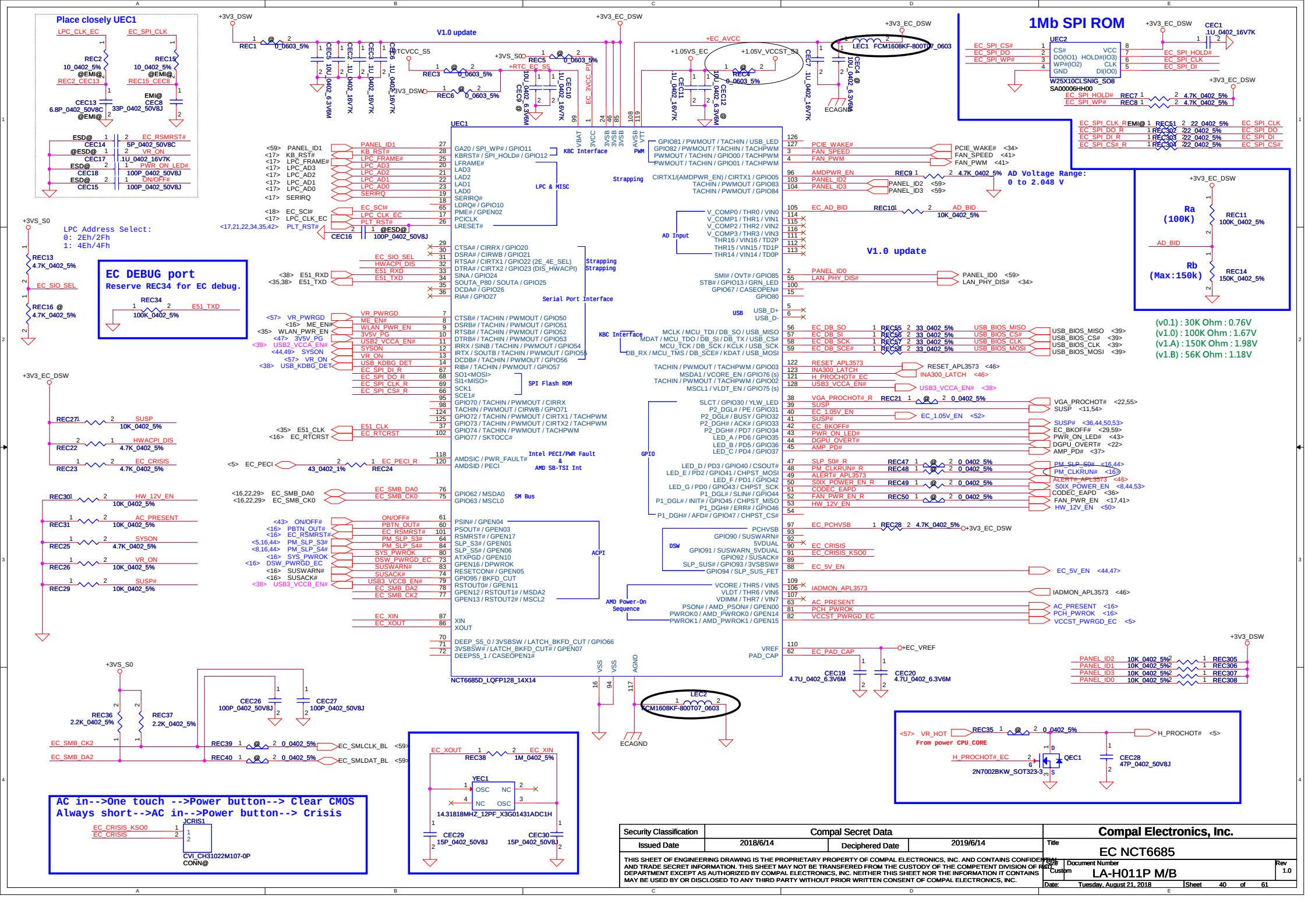


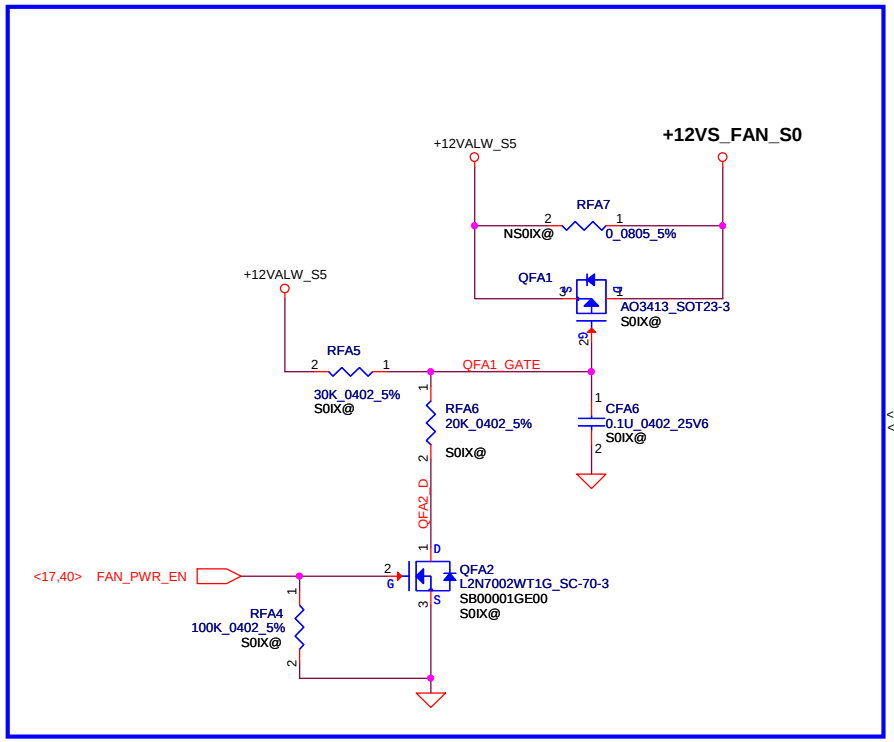
Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

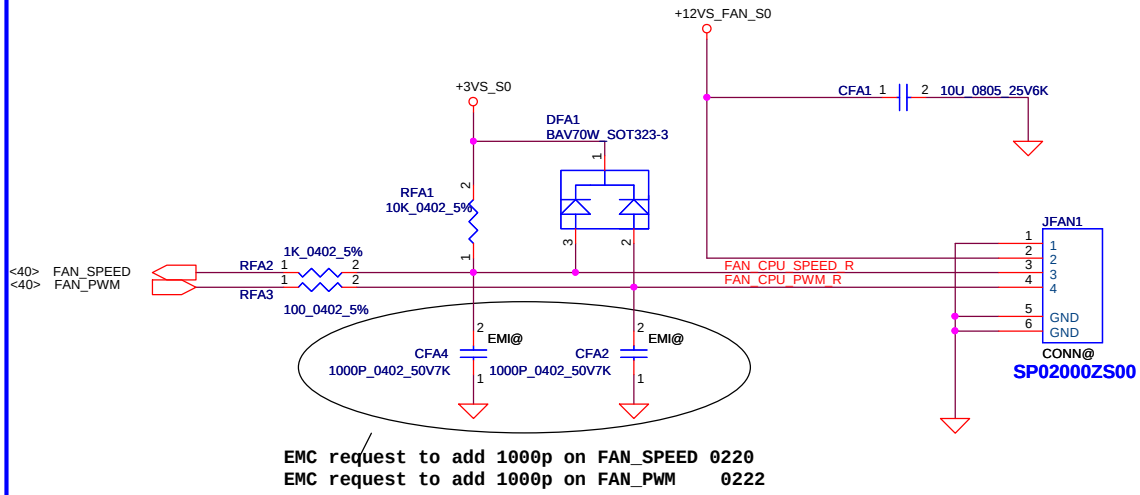
Compal Electronics, Inc.

Title: EC NCT6685

Size: Custom | Document Number: LA-H011P M/B | Rev: 1.0

Date: Tuesday, August 21, 2018 | Sheet 40 of 61





EMC request to add 1000p on FAN_SPEED 0220
EMC request to add 1000p on FAN_PWM 0222

FAN_PWM signal need keep 10 mil to other signal

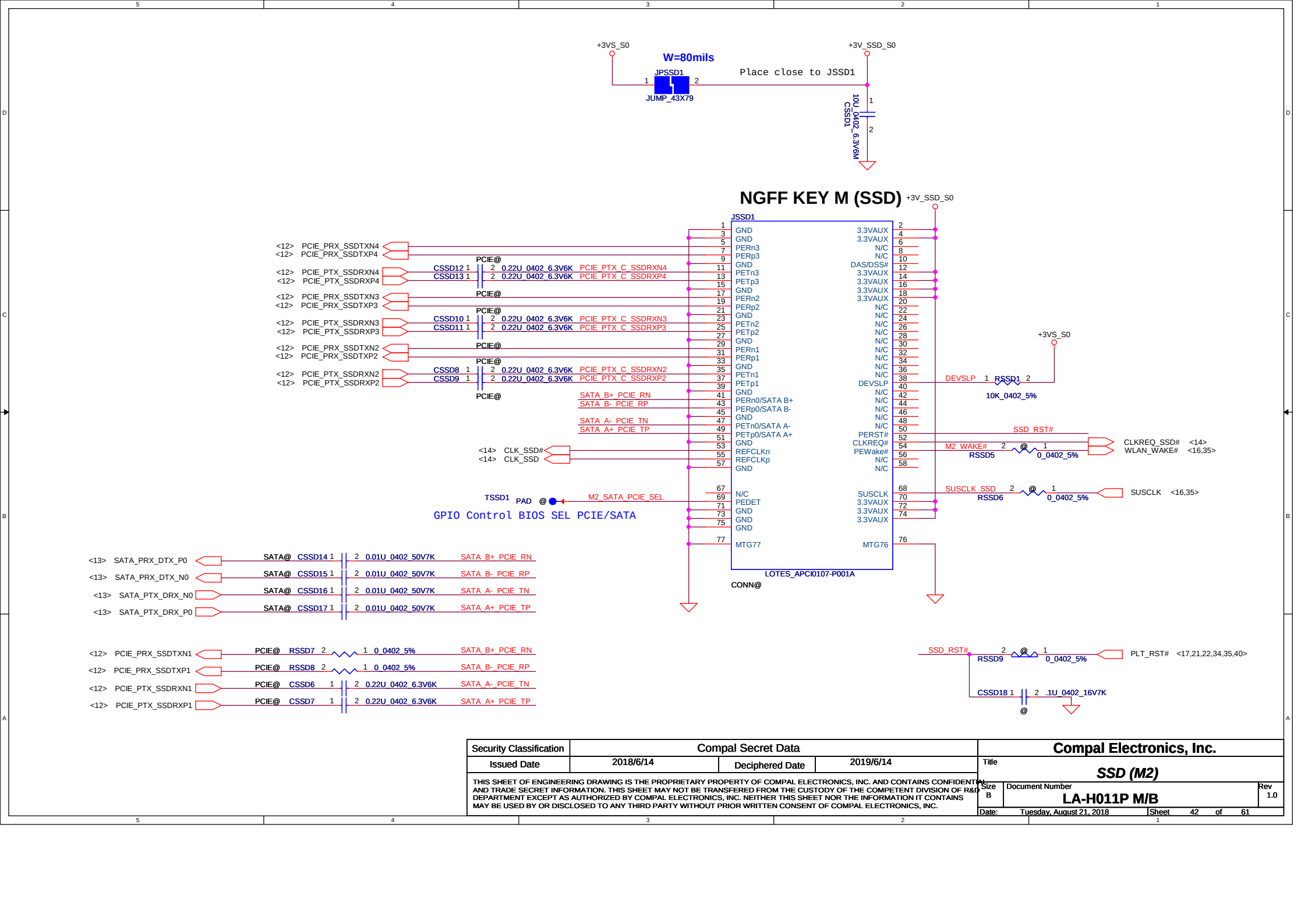
Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: **FAN/Thermal Sensor**

Size | Document Number: **LA-H011P M/B** | Rev: 1.0

Date: Tuesday, August 21, 2018 | Sheet 41 of 61



Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.

Title: ***SSD (M2)***

Size	Document Number	Rev
B	LA-H011P M/B	1.0

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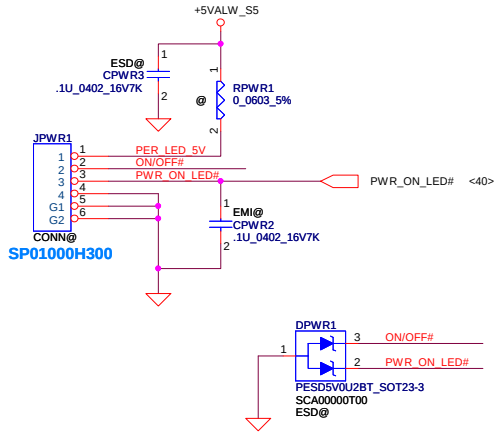
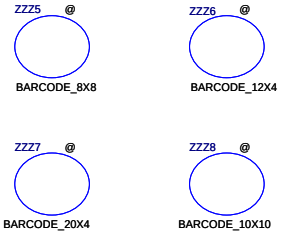
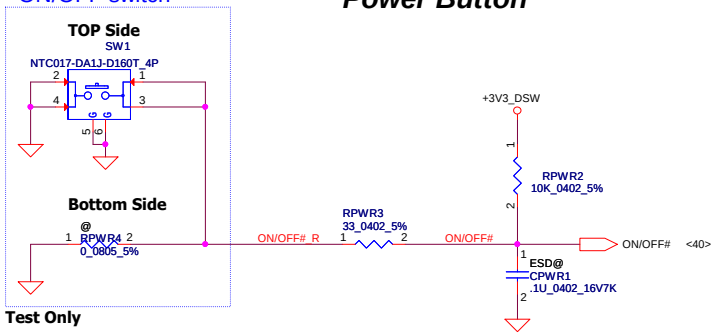


BARCODE



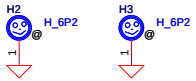
ON/OFF switch

Power Button



WIFI Hole

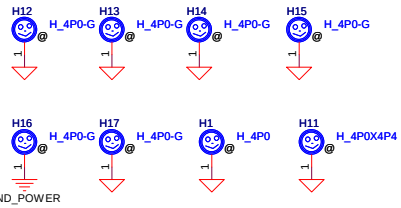
SSD Hole



Other Hole

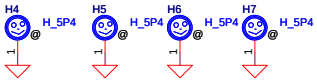
Screw Hole

4.0 mm x 6

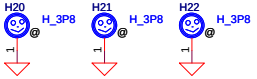


CPU Hole

5.4mm x 4

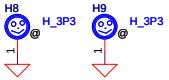


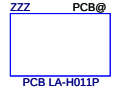
3.8 mm x 3

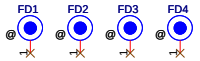


GPU Hole

3.3 mm x 2







Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

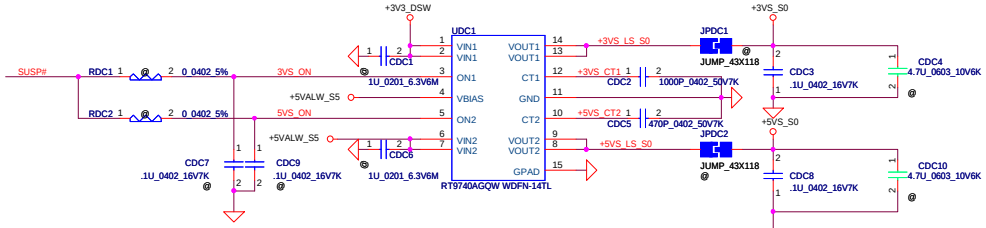
Compal Electronics, Inc.

Title: **PWR SW/LED/SCREW**

Size	Document Number	Rev
Custom	LA-H011P M/B	1.0

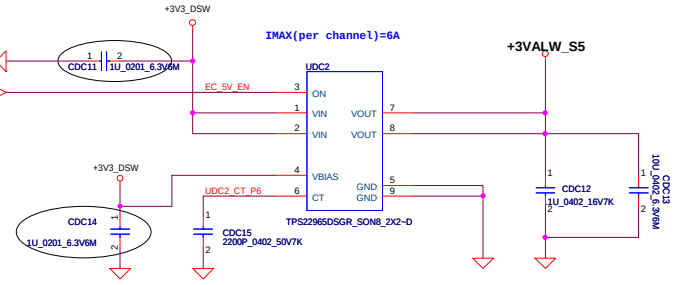
Date: Tuesday, August 21, 2018 | Sheet 43 of 61

VIN 5V and 3.3V (VBIAS=5V),IMAX(per channel)=6A,Rds=18mohm

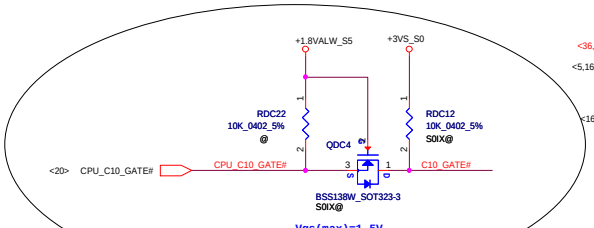


1st source : RT9740AGQW (SA00007VD00)
2nd source : TPS22966DPUR (SA00004MM00)

+3VDSW_S5 to +3VALW_S5 Transfer

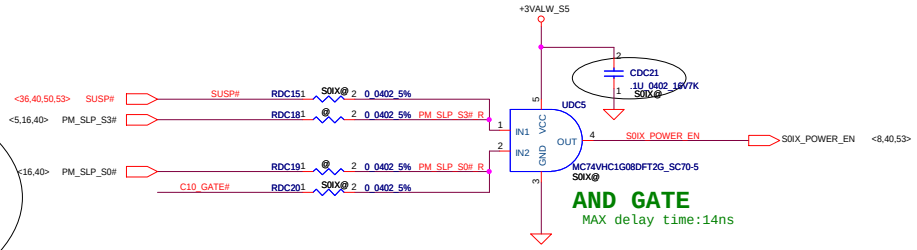


1st source : APL3526 (SA00006R100)
2nd source : TPS22965 (SA00005X50L)

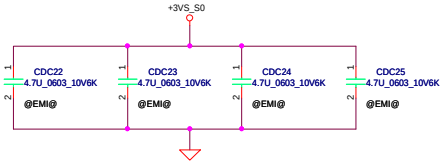


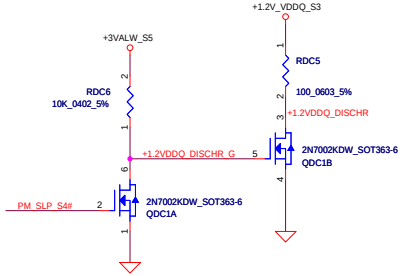
Vgs(max)=1.5V

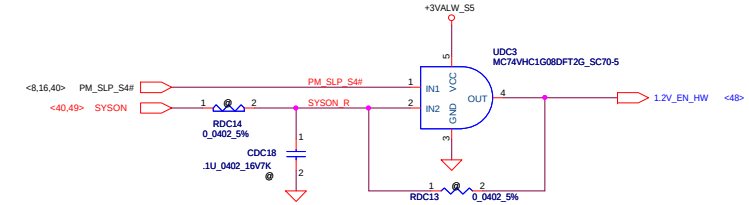
1nd source : BSS138W_PANJIT (SB00000T000)
2st source : LBSS139WT1G_LRC (SB00001GC00)



AND GATE
MAX delay time:14ns



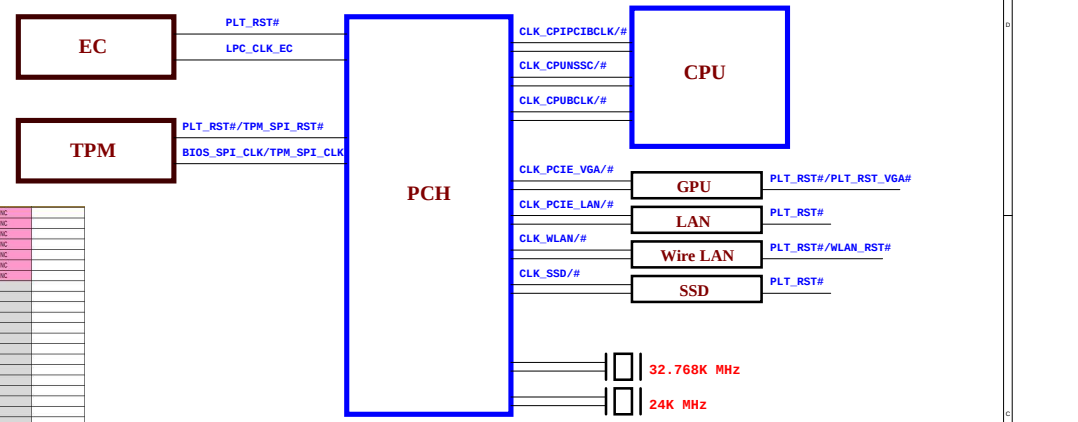




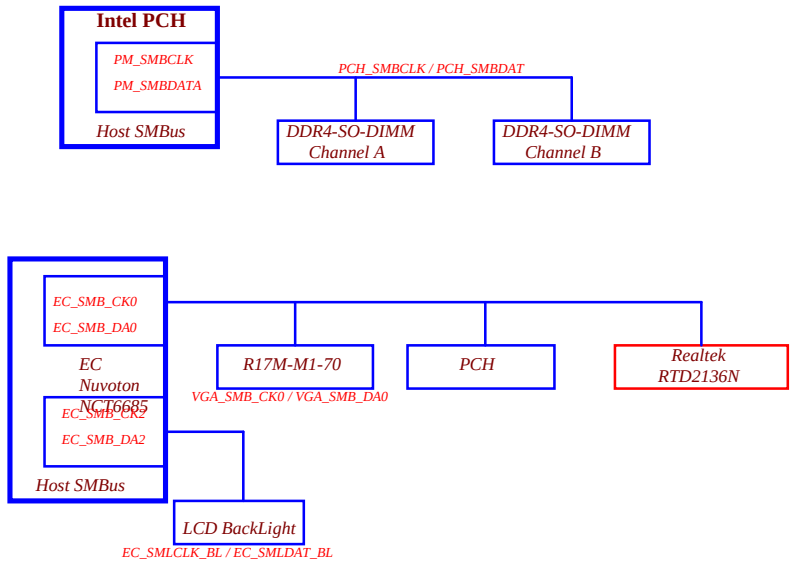
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/6/14	Deciphered Date 2019/6/14	Title: DC INTERFACE
			Size: C; Document Number: LA-H011P M/B; Rev: 1.0
			Date: Tuesday, August 21, 2018; Sheet 44 of 61

				Signal name	External PU/PD	HW Pin Requirement	Internal PU/PD Requirement	BIOS Pin Setting	Internal PU/PD Setting
GPD	BF44	GPD0/BATLOW#	none	PM_BATLOW#	PU 10K to +3V3_PCH_DSW	BATLOW#	none	Native	
	BG41	GPD1/ACPRESENT	none	AC_PRESENT_R	PU 10K to +3V3_PCH_DSW (@)	ACPRESENT	none	Native	
	BG44	GPD2/LAN_WAKE#	none	LAN_WAKE#	PU 10K to +3VALW_S5	LAN_WAKE#	none	Native	
	BE46	GPD3/PWRBTN#	none	PWRBTN#	PU 3K to +3V3_PCH_DSW	PWRBTN#	none	Native	20K PU
	BF42	GPD4/SLP_S3#	none	PM_SLP_S3#		SLP_S3#	none	Native	
	BE42	GPD5/SLP_S4#	none	PM_SLP_S4#		SLP_S4#	none	Native	
	BE40	GPD6/SLP_A#	none	NC		NC		NC	
	BE41	GPD7	none	GPD_7	HW Strap for Xtal Input H=Differential, L=Single ended PU 10K to +3VALW_S5	GPD_7	none	Native	
	BE45	GPD8/SUSCLK	none	SUSCLK	PD 100pF	SUSCLK	none	Native	
	BD42	GPD9/SLP_WLAN#	none	NC	Testpoint	NC	none	NC	
	BC42	GPD10/SLP_S5#	none	NC		NC	none	NC	
	BF41	GPD11/LANPHYPC	none	LANPHYPC	PU 10K to +3VALW_S5	LANPHYPC	none	Native	
GPP_A	BE39	GPP_A0/BC.INK/ESPI_ALERT1#	none	KB_RST#	PU 10K to +3VS_S0	GPI	none	Native	
	BB39	GPP_A1/LAD0/ESPI_IO0	none	LPC_AD0		LAD0	none	Native	
	AW37	GPP_A2/LAD1/ESPI_IO1	none	LPC_AD1		LAD1	none	Native	
	AV37	GPP_A3/LAD2/ESPI_IO2	none	LPC_AD2		LAD2	none	Native	
	BA38	GPP_A4/LAD3/ESPI_IO3	none	LPC_AD3		LAD3	none	Native	
	BE38	GPP_A5/LFRAME#/ESPI_CS0#	none	LPC_FRAME#		LFRAME#	none	Native	
	AW35	GPP_A6/SERIRQ/ESPI_CS1#	none	SERIRQ	PU 8.2K to +3VS_S0	SERIRQ	none	Native	
	BA36	GPP_A7/PIRQA#/ESPI_ALERT0#	none	LPC_PIRQA#	PU 10K to +3VALW_S5	PIRQA#	none	Native	
	AV32	GPP_A8/CLKRUN#	none	PM_CLKRUN#	PU 8.2K to +3VS_S0	CLKRUN#	none	Native	
	BB36	GPP_A9/CLKOUT_LPC0/ESPI_CLK	none	LPC_CLKOUT0		CLKOUT_LPC0	none	Native	
	BB34	GPP_A10/CLKOUT_LPC1	none	NC	Testpoint	NC		NC	
	BE36	GPP_A11/PME#/SD_VDD2_PWR_EN#	none	PCH_PME#	PU 100K to +3VALW_S5	PME#	none	Native	
	BF36	GPP_A12/BM_BUSY#/SYS_GPIO_56_EXIT_HO	none	NC	Testpoint	NC	none	NC	
	BC37	GPP_A13/SUSWARN#/SUSPWRDNACK	none	SUSWARN#_R	PU 10K to +3VALW_S5 (@)	SUSWARN#	none	Native	
	BF38	GPP_A14/SUS_STAT#/ESPI_RESET#	none	NC	Testpoint	NC	none	NC	
	BE35	GPP_A15/SUSACK#	none	SUSACK#		SUSACK#	none	Native	
	BE33	GPP_A16/CLKOUT_48	none	NC	Testpoint	NC	none	NC	
	BD38	GPP_A17/SD_VDD1_PWR_ENB/ISH_GP7	none	NC		NC	none	NC	
	BF35	GPP_A18/ISH_GP0	none	NC		NC	none	NC	
	BD34	GPP_A19/ISH_GP1	none	NC		NC	none	NC	
	BE34	GPP_A20/ISH_GP2	none	NC		NC	none	NC	
	BA33	GPP_A21/ISH_GP3	none	NC		NC	none	NC	
	AW32	GPP_A22/ISH_GP4	none	NC		NC	none	NC	
	AV36	GPP_A23/ISH_GP5	none	NC		NC	none	NC	
GPP_B	BE29	GPP_B0/GSPI0_CS1#	none	NC		NC	none	NC	
	BF33	GPP_B1/GSPI1_CS1#/TIME_SYNC1	none	NC		NC	none	NC	
	BE32	GPP_B2/VRALERT#_N	none	VRALERT#	PU 10K to +3VALW_S5	VRALERT#	none	Native	
	BF32	GPP_B3/CPU_GP2	none	NC		NC	none	NC	
	BC33	GPP_B4/CPU_GP3	none	NC		NC	none	NC	
	BF31	GPP_B5/SRCCLKREQ0#	none	CLKREQ_VGA#	PU 10K to +3VS+S0	SRCCLKREQ0#	none	Native	
	BE31	GPP_B6/SRCCLKREQ1#	none	CLKREQ_LAN#	PU 10K to +3VS+S0	SRCCLKREQ1#	none	Native	
	AB32	GPP_B7/SRCCLKREQ2#	none	CLKREQ_SSD#	PU 10K to +3VS+S0	SRCCLKREQ2#	none	Native	
	BB30	GPP_B8/SRCCLKREQ3#	none	CLKREQ_WLAN#	PU 10K to +3VS+S0	SRCCLKREQ3#	none	Native	
	BA30	GPP_B9/SRCCLKREQ4#	none	NC		NC	none	NC	
	AN29	GPP_B10/SRCCLKREQ5#	none	NC		NC	none	NC	
	AP29	GPP_B11/I2S_MCLK	none	SLP_S0#		SLP_S0#	none	Native	
	BC28	GPP_B12/SLP_S0#	none	NC		NC	none	NC	
	AV29	GPP_B13/PLTRST#	none	PCH_PLT_RST#		PLTRST#	none	Native	
	AW29	GPP_B14/SPKR	NMI SMI	PCH_SPKR	Strap for Top Swap override (Internal Pull Down)	SPKR	20K PD / L	Native	20K PD
	BB26	GPP_B15/GSPI0_CS0#	none	NC		NC	none	NC	
	BF29	GPP_B16/GSPI0_CLK	none	USB_UART_SEL	PU 100K to +3VALW_S5	GPO	none	GPO_H	
	BD29	GPP_B17/GSPI0_MISO	none	NC		NC	none	NC	
	BE30	GPP_B18/GSPI0_MOSI	none	NC	Strap for No Reboot (Internal Pull Down) H=Disable(Default), L=Enable PU 4.7K to +3VS_S0(@)	NC	20K PD / L	NC	20K PD
	AW28	GPP_B19/GSPI1_CS0#	none	NC		NC	none	NC	
	AU26	GPP_B20/GSPI1_CLK	NMI SMI	EC_SCI#	PU 10K to +3VALW_S5	GPI	none	GPI	
	BD30	GPP_B21/GSPI1_MISO	none	NC	PU 10K to +3VS_S0(@)	NC	none	NC	
	BA26	GPP_B22/GSPI1_MOSI	none	NC	Strap for BIOS Boot (Internal Pull Down) H=LPC, L=SPI(Default) PU 10K to +3VS_S0(@)	NC	20K PD / L	NC	20K PD
	BD33	GPP_B23/SMLIALERT#/PCHHOT#	NMI SMI	NC	Strap for eSPI/LPC mode selection H=eSPI(Default), L=LPC PU 4.7K to +3VALW_S5(@)	NC	20K PD / L	NC	20K PD
GPP_C	BE26	GPP_C0/SMBCLK	none	PM_SMBCLK	PU 2.2K to +3VALW_S5	SMBCLK	none	Native	
	BF26	GPP_C1/SMBDATA	none	PM_SMBDAT	PU 2.2K to +3VALW_S5	SMBDATA	none	Native	
	BE25	GPP_C2/SMBALERT#	none	NC	Strap for TLS Confidentiality (Internal Pull Down) H=Enable, L=Disable(Default)	NC	20K PD / L	NC	20K PD
	BF25	GPP_C3/SML0CLK	none	PCH_SML0CLK0	PU 499 to +3VS_S0	SML0CLK	none	Native	
	BE24	GPP_C4/SML0DATA	none	PCH_SML0DAT0	PU 499 to +3VS_S0	SML0DATA	none	Native	
	BF24	GPP_C5/SML0ALERT#	none	NC	Strap for eSPI/LPC mode selection H=eSPI(Default), L=LPC PU 4.7K to +3VALW_S5(@)	NC	20K PD / L	NC	20K PD
	BF27	GPP_C6/SML1CLK	none	EC_SMB_CK0	PU 1K to +3VS_S0	SML1CLK	none	Native	
	BE27	GPP_C7/SML1DATA	none	EC_SMB_DA0	PU 1K to +3VS_S0	SML1DATA	none	Native	
	BE23	GPP_C8/UART0A_RXD	none	NC		NC	none	NC	
	BB24	GPP_C9/UART0A_TXD	none	NC		NC	none	NC	
	BA24	GPP_C10/UART0A_RTS#	none	WL_ON	PU 10K to +3VALW_S5 (@)	NC	none	NC	
	AP24	GPP_C11/UART0A_CTS#	none	BT_ON	PU 10K to +3VALW_S5 (@)	NC	none	NC	
GPP_D	AU24	GPP_C12/UART1_RXD/ISH_UART1_RXD	none	DGPU_PWR_EN	PD 100K	NC	none	NC	
	AP21	GPP_C13/UART1_TXD/ISH_UART1_TXD	none	DGPU_HOLD_RST#	PU 10K to +3VS _S0	GPI	none	GPI	
	AW24	GPP_C14/UART1_RTS#/ISH_UART1_RTS#	none	DGPU_PRESENT	PU 10K to +3VS_S0 for DIS or PD 10K for UMA	NC	none	NC	
	BD21	GPP_C15/UART1_CTS#/ISH_UART1_CTS#	none	NC		NC	none	NC	
	BF23	GPP_C16/I2C0_SDA	none	NC		NC	none	NC	
	BC23	GPP_C17/I2C0_SCL	none	NC		NC	none	NC	
	BF21	GPP_C18/I2C1_SDA	none	NC		NC	none	NC	
	BE21	GPP_C19/I2C1_SCL	none	NC		NC	none	NC	
	BD20	GPP_C20/UART2_RXD	none	UART_2_CRXD_DTXD	PU 49.9K to +3VS_S0	UART2_RXD	none	Native	
	BE20	GPP_C21/UART2_TXD	none	UART_2_CTXD_DRXD	PU 49.9K to +3VS_S0	UART2_TXD	none	Native	
	AW21	GPP_C22/UART2_RTS#	NMI SMI	NC	PU 49.9K to +3VS_S0 @	NC	none	NC	
	AV21	GPP_C23/UART2_CTS#	NMI SMI	NC	PU 49.9K to +3VS_S0 @	NC	none	NC	
GPP_E	BF19	GPP_D0/SPI1_CS#/SBK0_BK0	NMI SMI	NC		NC	none	NC	
	BE19	GPP_D1/SPI1_CLK/SBK1_BK1	NMI SMI	NC		NC	none	NC	
	BE18	GPP_D2/SPI1_MISO/SBK2_BK2	NMI SMI	NC		NC	none	NC	
	BF18	GPP_D3/SPI1_MOSI/SBK3_BK3	NMI SMI	NC		NC	none	NC	
	BE15	GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4_BK	NMI SMI	NC		NC	none	NC	
	BE16	GPP_D5/I2S2_SFRM/CNV_RF_RESET#	none	NC		NC	none	NC	
	BA17	GPP_D6/I2S2_TXD/MODEM_CLKREQ	none	NC		NC	none	NC	
	AW18	GPP_D7/I2S2_RXD	none	NC		NC	none	NC	
	AV18	GPP_D8/I2S2_SCLK	none	NC		NC	none	NC	
	BA20	GPP_D9/ISH_SPI_CS#/GSPI2_CS0#	none	NC		NC	none	NC	
	BB20	GPP_D10/ISH_SPI_CLK/GSPI2_CLK	none	NC		NC	none	NC	
	BB16	GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GS	none	NC		NC	none	NC	
	AN18	GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI	none	NC		NC	none	NC	
	BE17	GPP_D13/ISH_UART0_RXD/I2C2_SDA	none	NC		NC	none	NC	
	BF17	GPP_D14/ISH_UART0_TXD/I2C2_SCL	none	NC		NC	none	NC	
	AR18	GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/C	none	NC		NC	none	NC	
	BF14	GPP_D16/ISH_UART0_CTS#/CNV_WCEN	none	NC		NC	none	NC	
	AW15	GPP_D17/DMIC_CLK1/SNDW3_CLK	none	NC	Testpoint	NC	none	NC	
	AV16	GPP_D18/DMIC_DATA1/SNDW3_DATA	none	NC	Testpoint	NC	none	NC	
	BD16	GPP_D19/DMIC_CLK0/SNDW4_CLK	none	NC	Testpoint	NC	none	NC	
	BF15	GPP_D20/DMIC_DATA0/SNDW4_DATA	none	NC	Testpoint	NC	none	NC	
	BD17	GPP_D21/SPI1_IO2	none	NC		NC	none	NC	
	BC17	GPP_D22/SPI1_IO3	none	NC		NC	none	NC	
	BE14	GPP_D23/ISH_I2C2_SCL/I2C3_SCL	none	NC		NC	none	NC	
GPP_F	AH41	GPP_E0/SATAXPCIE0/SATAGP0	NMI SMI	SATA_GP0	PU 10K to +3VS_S0	SATAGP0	none	Native	
	AJ43	GPP_E1/SATAXPCIE1/SATAGP1	NMI SMI	SATA_GP1	PU 10K to +3VS_S0	SATAGP1	none	Native	
	AK47	GPP_E2/SATAXPCIE2/SATAGP2	NMI SMI	SATA_GP2	PU 10K to +3VS_S0	SATAGP2	none	Native	
	AL47	GPP_E3/CPU_GP0	NMI SMI	DGPU_PWROK	PU 10K to +3VS _S0	GPO	none	GPO_H	
	AL48	GPP_E4/SATA_DEVSLP0	NMI SMI	NC		NC	none	NC	
	AH35	GPP_E5/SATA_DEVSLP1	NMI SMI	NC		NC	none	NC	
	AH40	GPP_E6/SATA_DEVSLP2	NMI SMI	NC		NC	none	NC	
	AM45	GPP_E7/CPU_GP1	NMI SMI	NC		NC	none	NC	
	AK48	GPP_E8/SATA_LED#	NMI SMI	SATA_LED#	PU 10K to +3VS_S0	SATA_LED#	none	Native	
	AH36	GPP_E9/USB2_OC0#	none	USB_OC0#	PU 10K to +3VALW_S5	USB2_OC0#	none	Native	
	AL40	GPP_E10/USB2_OC1#	none	USB_OC#1	PU 10K to +3VALW_S5	USB2_OC1#	20K PD / L	Native	20K PD
	AJ44	GPP_E11/USB2_OC2#	none	USB_OC#2	PU 10K to +3VALW_S5	USB2_OC2#	20K PD / L	Native	20K PD
	AL41	GPP_E12/USB2_OC3#	none	USB_OC#3	PU 10K to +3VALW_S5	USB2_OC3#	20K PD / L	Native	20K PD
GPP_F	AN47	GPP_F0/SATAXPCIE3/SATAGP_3	none	SATA_GP3	PU 10K to +3VS _S0	SATAGP3	none	Native	
	AM46	GPP_F1/SATAXPCIE4/SATAGP4	none	NC		NC	none	NC	
	AM43	GPP_F2/SATAXPCIE5/SATAGP5	none	NC		NC	none	NC	
	AM47	GPP_F3/SATAXPCIE6/SATAGP6	none	NC		NC	none	NC	
	AM48	GPP_F4/SATAXPCIE7/SATAGP7	none	NC		NC	none	NC	
	AP48	GPP_F5/SATA_DEVSLP3	none	NC		NC	none	NC	
	AP47	GPP_F6/SATA_DEVSLP4	none	NC		NC	none	NC	
	AN46	GPP_F7/SATA_DEVSLP5	none	NC		NC	none	NC	
	AN37	GPP_F8/SATA_DEVSLP6	none	NC		NC	none	NC	
	AP47	GPP_F9/SATA_DEVSLP7	none	NC		NC	none	NC	
	AP42	GPP_F10/SATA_SCLOCK	none	NC		NC	none	NC	
	AP48	GPP_F11/SATA_SLOAD	none	NC		NC	none	NC	
	AU46	GPP_F12/SATA_SDATAOUT1	none	NC		NC	none	NC	
	AU47	GPP_F13/SATA_SDATAOUT0	none	NC		NC	none	NC	
	AP41	GPP_F14/PS_ON#	none	NC		NC	none	NC	
	AV47	GPP_F15/USB2_OC4#	none	NC	PU 10K to +3VALW_S5(@)	NC	none	NC	
	AR35	GPP_F16/USB2_OC5#	none	NC	PU 10K to +3VALW_S5(@)	NC	none	NC	20K PD
	AR37	GPP_F17/USB2_OC6#	none	NC	PU 10K to +3VALW_S5(@)	NC	none	NC	
	AV43	GPP_F18/USB2_OC7#	none	NC	PU 10K to +3VALW_S5(@)	NC	none	NC	
	AV44	GPP_F19/EDP_VDDEN	none	NC	Testpoint	NC	none	NC	
	AV46	GPP_F20/EDP_BKLTEN	none	BKLEN_PCH		EDP_BKLTEN	none	Native	
	AU48	GPP_F21/EDP_BKLTCTL	none	BKL_PWM_PCH	PD 100K @	GPIO	none	Native	
	AN44	GPP_F22/DDPF_CTRLCLK	none	NC		GPO	none	GPO_H	
	AN40	GPP_F23/DDPF_CTRLDATA	none	NC	Testpoint	NC	none	NC	20K PD
	AW13	GPP_G0/SD_CMD	none	NC		NC	none	NC	
GPP_G	BE9	GPP_G1/SD_DATA0	none	NC		NC	none	NC	
	BF8	GPP_G2/SD_DATA1	none	NC		NC	none	NC	
	BF9	GPP_G3/SD_DATA2	none	NC		NC	none	NC	
	BG8	GPP_G4/SD_DATA3	none	NC		NC	none	NC	
	BE8	GPP_G5/SD_CD#	none	NC		NC	none	NC	
	BD8	GPP_G6/SD_CLK	none	NC		NC	none	NC	
	AV13	GPP_G7/SD_WP	none	NC		NC	none	NC	
	AE47	GPP_H0/SRCCLKREQ6#	none	NC		NC	none	NC	
	AC48	GPP_H1/SRCCLKREQ7#	none	NC		NC	none	NC	
	AE41	GPP_H2/SRCCLKREQ8#	none	NC		NC	none	NC	
	AF48	GPP_H3/SRCCLKREQ9#	none	NC		NC	none	NC	
	AC41	GPP_H4/SRCCLKREQ10#	none	NC		NC	none	NC	
	AC39	GPP_H5/SRCCLKREQ11#	none	NC		NC	none	NC	
	AE39	GPP_H6/SRCCLKREQ12#	none	NC		NC	none	NC	
	AB48	GPP_H7/SRCCLKREQ13#	none	NC		NC	none	NC	
	AC44	GPP_H8/SRCCLKREQ14#	none	NC		NC	none	NC	
	AC43	GPP_H9/SRCCLKREQ15#	none	NC		NC	none	NC	
	AF48	GPP_H10/SML2CLK	none	NC		NC	none	NC	
	AD47	GPP_H11/SML2DATA	none	NC		NC	none	NC	
GPP_H	AB47	GPP_H12/SML2ALERT#	none	NC		NC	20K PD / L	NC	20K PD
	AF47	GPP_H13/SML3CLK	none	NC		NC	none	NC	
	AD48	GPP_H14/SML3DATA	none	NC		NC	none	NC	
	AC47	GPP_H15/SML3ALERT#	none	NC		NC	none	NC	
	AE45	GPP_H16/SML4CLK	none	NC		NC	none	NC	
	AJ46	GPP_H17/SML4DATA	none	NC		NC	none	NC	
	AE44	GPP_H18/SML4ALERT#	none	FAN_PWR_EN		GPO	none	GPO_H	
	AH46	GPP_H19/ISH_I2C0_SDA	none	NC		NC	none	NC	
	AG45	GPP_H20/ISH_I2C0_SCL	none	NC		NC	none	NC	
	AH48	GPP_H21/ISH_I2C1_SDA	none	NC		NC	none	NC	
	AH47	GPP_H22/ISH_I2C1_SCL	none	NC		NC	none	NC	
	AJ47	GPP_H23/TIME_SYNC0	none	SATA_PCIE_SSD	PU 10K to +3VALW_S5 for SATA PD 10K for PCIE	GPI	none	GPI	
GPP_I	AT6	GPP_I0/DDPB_HPD0/DISP_MISC0	NMI SMI	PCH_HDMIOUT_HPD	PU 1M to +3VS _S0	DDPB_HPD0	none	Native	
	AN10	GPP_I1/DDPC_HPD1/DISP_MISC1	NMI SMI	NC		NC	none	NC	
	AP9	GPP_I2/DDPD_HPD2/DISP_MISC2	NMI SMI	NC		NC	none	NC	
	AL15	GPP_I3/DDPE_HPD3/DISP_MISC3	NMI SMI	NC		NC	none	NC	
	AN6	GPP_I4/EDP_HPD/DISP_MISC4	none	EDP_HPD	PD 100K	EDP_HPD	none	Native	
	AL13	GPP_I5/DDPB_CTRLCLK	none	PCH_HDMIOUT_CLK	PU 2.2K to +3VS_S0	DDPB_CTRLCLK	none	Native	
	AR8	GPP_I6/DDPB_CTRLDATA	none	PCH_HDMIOUT_DAT	PU 2.2K to +3VS_S0	DDPB_CTRLDATA	20K PD / L	Native	20K PD
GPP_J	AN13	GPP_J7/DDPC_CTRLCLK	none	NC		NC	none	NC	
	AL10	GPP_J8/DDPC_CTRLDATA	none	NC		NC	20K PD / L	NC	20K PD
	AL9	GPP_J9/DDPD_CTRLCLK	none	NC		NC	none	NC	
	AR3	GPP_J10/DDPD_CTRLDATA	none	NC		NC	20K PD / L	NC	20K PD
	AP3	GPP_J11/M2_SKT2_CFG0	none	NC		NC	none	NC	
	AP2	GPP_J12/M2_SKT2_CFG1	none	NC		NC	none	NC	
	AN4	GPP_J13/M2_SKT2_CFG2	none	NC		NC	none	NC	
	AM7	GPP_J14/M2_SKT2_CFG3	none	NC		NC	none	NC	
	AV6	GPP_J0/CNV_PA_BLANKING	none	NC		NC	none	NC	
	AY3	GPP_J1/CNV_C10_GATE#	none	CPU_C10_GATE#		CPU_C10_GATE#	none	Native	
	AW3	GPP_J_2	none	NC		NC	none	NC	
	AT10	GPP_J_3	none	NC		NC	none	NC	
	AV4	GPP_J4/CNV_BRI_DT/UART0B_RTS#	none	NC		NC	none	NC	20K PD
	AY2	GPP_J5/CNV_BRI_RSP/UART0B_RXD	none	NC		NC	none	NC	
	BA4	GPP_J6/CNV_RGI_DT/UART0B_TXD	none	NC		NC	none	NC	
	AV3	GPP_J7/CNV_RGI_RSP/UART0B_CTS#	none	NC		NC	none	NC	
	AW2	GPP_J8/CNV_MFUART2_RXD	none	NC		NC	none	NC	
	AU9	GPP_J9/CNV_MFUART2_TXD	none	NC		NC	none	NC	20K PD
	AV7	GPP_J10	none	NC		NC	none	NC	
	AR13	GPP_J11/A4WP_PRESENT	none	NC		NC	none	NC	
GPP_K	L47	GPP_K0	none	NC		NC	none	NC	
	L46	GPP_K1	none	NC		NC	none	NC	
	U48	GPP_K2	none	NC		NC	none	NC	
	U47	GPP_K3	none	NC		NC	none	NC	
	N48	GPP_K4	none	NC		NC	none	NC	
	N47	GPP_K5	none	NC		NC	none	NC	
	N47	GPP_K6	none	NC		NC	none	NC	
	R46	GPP_K7	none	NC		NC	none	NC	
	P48	GPP_K8	none	NC		NC	none	NC	
	V47	GPP_K9	none	NC		NC	none	NC	
	V48	GPP_K10	none	NC		NC	none	NC	
	W47	GPP_K11	none	NC		NC	none	NC	
GPP_K	Y46	GPP_K12/GSXDOUT	none	NC		NC	none	NC	
	Y48	GPP_K13/GSXSLOAD	none	NC		NC	none	NC	
	W48	GPP_K14/GSXCIN	none	NC		NC	none	NC	
	AA45	GPP_K15/GSXSRESET#	none	NC		NC	none	NC	
	Y47	GPP_K16/GSXCLK	none	NC		NC	none	NC	
	R47	GPP_K17/ADR_COMPLETE	none	NC		NC	none	NC	
	T47	GPP_K18/NMI#	none	NC		NC	none	NC	
	T48	GPP_K19/SMI#	none	NC	Testpoint	NC	none	NC	
	T46	GPP_K20	none	TPM_STS1R#		GPI	none	GPI	
	T45	GPP_K21	none	SCA_FW_FLASH	PD 10K	GPO	none	GPO_L	
	L48	GPP_K22/IMGCLKOUT0	none			GPO	none	GPO_H	
	M45	GPP_K23/IMGCLKOUT1	none	TPM_MODE	PU 10K to +3VALW_S5 for TPM or PD 10K for SW TPM	GPI	none	GPI	

System clock and Reset map



SMBUS Block Diagram



Security Classification	Compal Secret Data		
Issued Date	2018/6/14	Deciphered Date	2019/6/14

Compal Electronics, Inc.			
Title	GPIO Table & SMBUS BD		
Size	Document Number		Rev
	LA-H011P M/B		1.0
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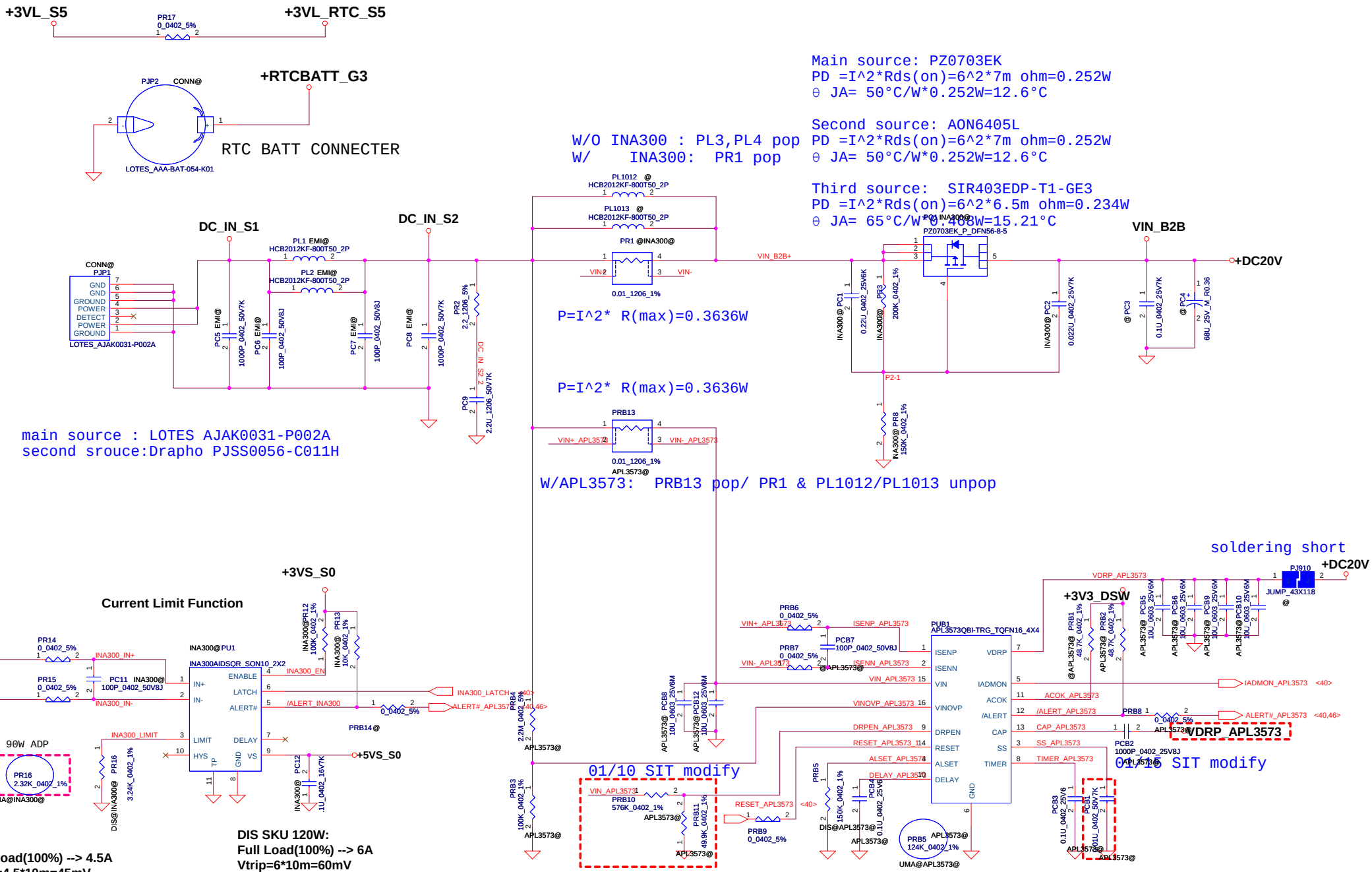

Security Classification	Compal Secret Data		
Issued Date	2013/12/18	Deciphered Date	2013/12/18

Compal Electronics, Inc.	
Title	DCIN / CONN
Size	Custom
Document Number	Rev 0.1
Date:	Tuesday, August 21, 2018
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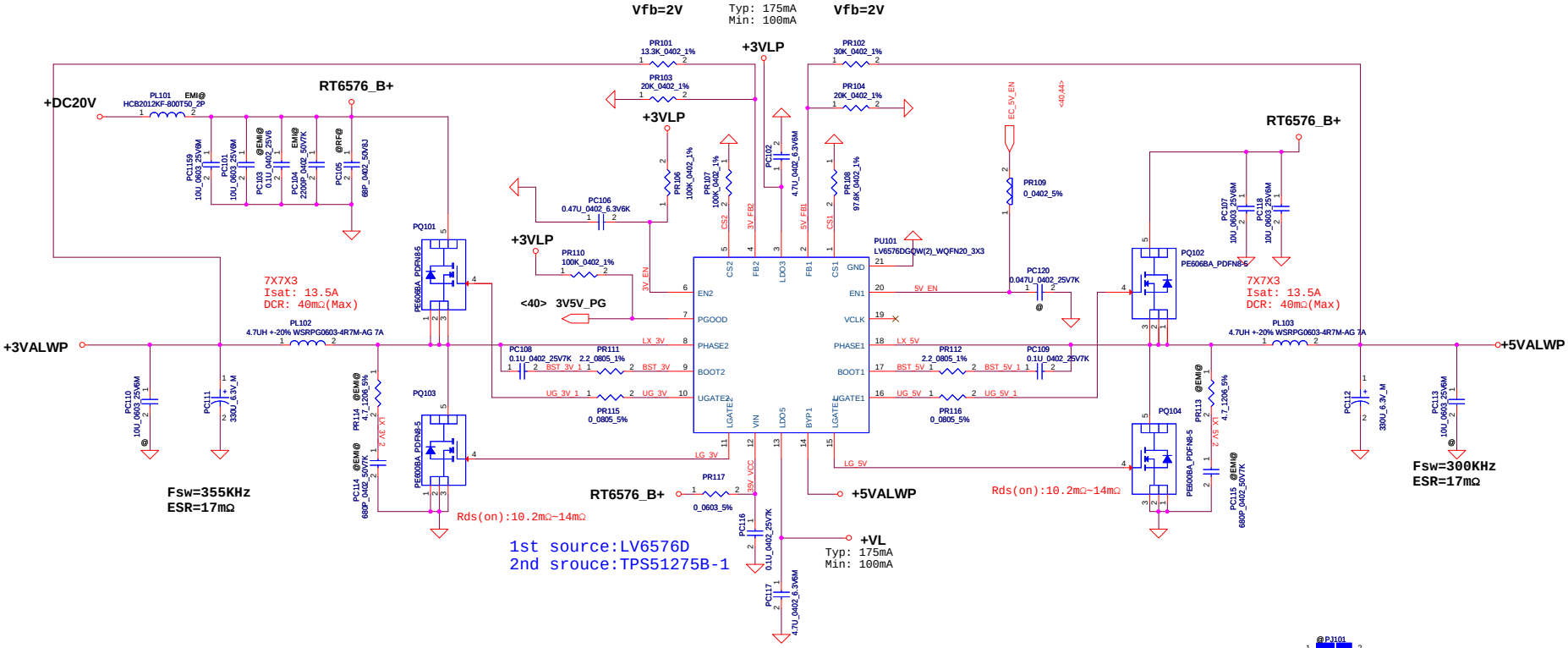
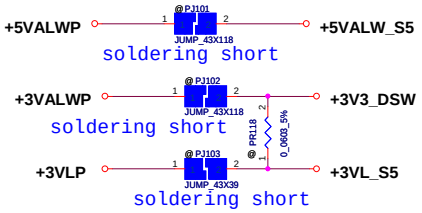




+3VALWP
Vin = 20V
Iin =3.3*7.87/0.85/20
= 1.42A

Vout = Vfb*[1+(Rt/Rb)]
= 2*[1+(13.3K/20K)]
= 3.3V

+5VALWP
Vin = 20V
Iin =5*7/0.85/20
= 2.06A

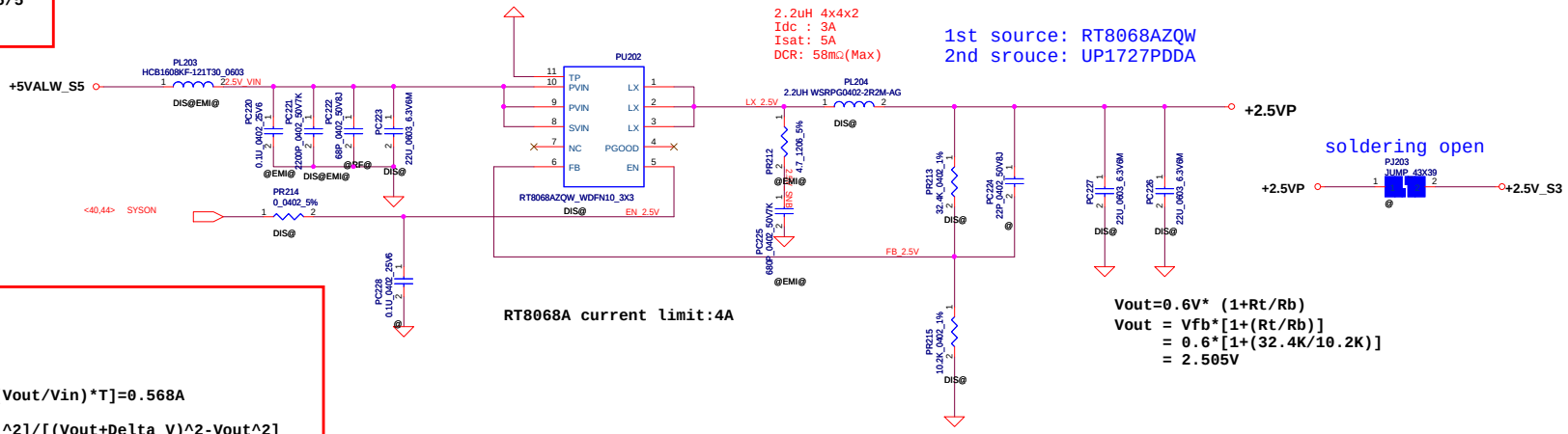
Vout = Vfb*[1+(Rt/Rb)]
= 2*[1+(30K/20K)]
=5V

+3VALWP
Imax=5.11 ; Ipeak=7.3 ;Fsw=355KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=12.03A~12.25A
Iin_ripple=1.9A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.651A
LIR=Delta IL/Ipeak=0.226
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=376.39uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.99uF

+5VALWP
Imax=4.9A,Ipeak=7A ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:10.2ohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=11.96A~12.18A
Iin_ripple=2.12A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.660A
LIR=Delta IL/Ipeak=0.38
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=180.6uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.53uF

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/08/15	Deciphered Date	2013/08/29
Title	+3VALWP / +5VALWP		
Size C	Document Number		Rev 0.1
Date: Tuesday, August 21, 2018	Sheet 48 of 60		

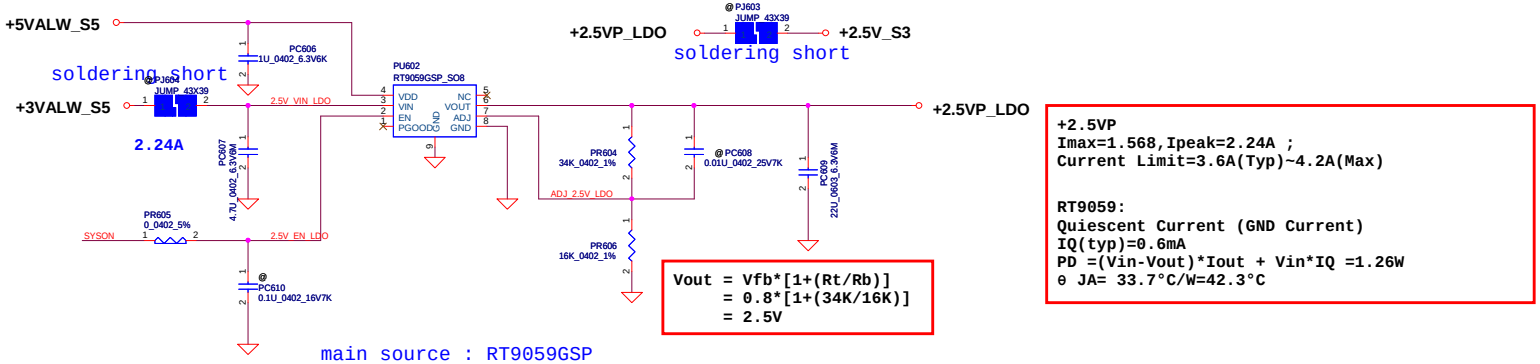
+2.5VP
Vin =5V
Iin = 2.5*2.24/0.85/5
=1.32A



+2.5VP
Ipeak=2.24A ;Fsw=1MHz
ILimit=4A
Iin_ripple=0.75A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.568A
LIR=Delta IL/Ipeak=0.25
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=11.8uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.78uF

RT8068A current limit:4A

Vout=0.6V* (1+Rt/Rb)
Vout = Vfb*[1+(Rt/Rb)]
= 0.6*[1+(32.4K/10.2K)]
= 2.505V



Vout = Vfb*[1+(Rt/Rb)]
= 0.8*[1+(34K/16K)]
= 2.5V

main source : RT9059GSP
second srouce: APL5933CKAI

+2.5VP
Imax=1.568,Ipeak=2.24A ;
Current Limit=3.6A(Typ)~4.2A(Max)

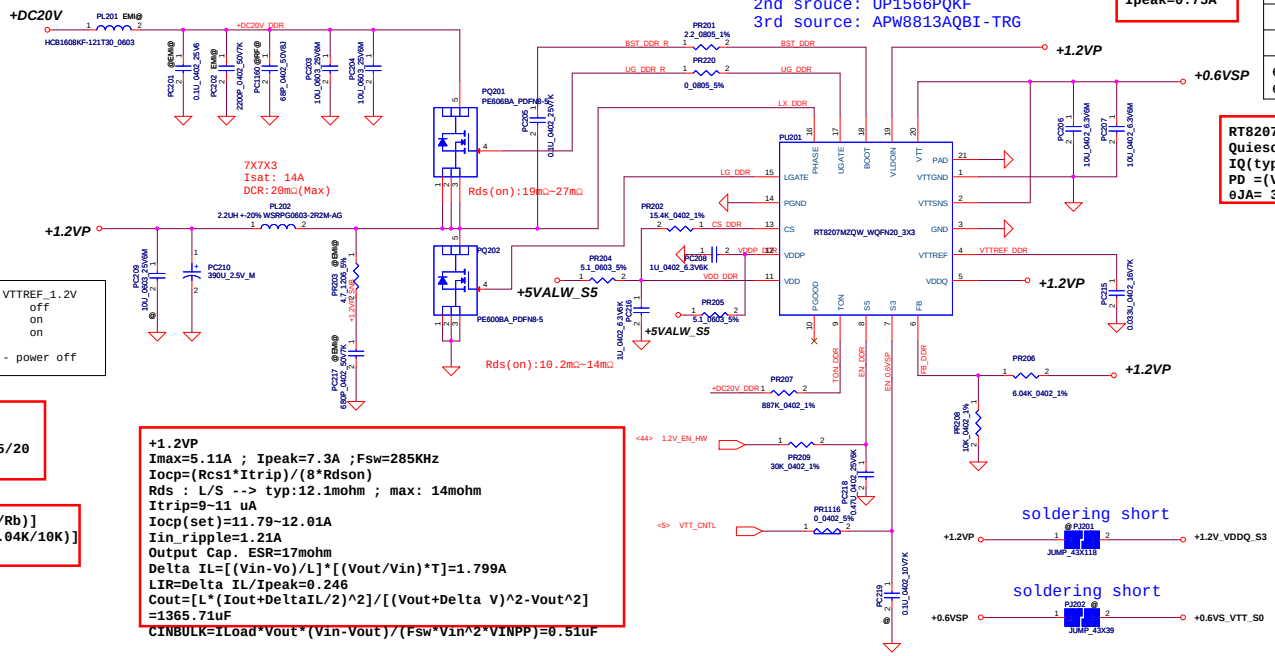
RT9059:
Quiescent Current (GND Current)
IQ(typ)=0.6mA
PD =(Vin-Vout)*Iout + Vin*IQ =1.26W
θ JA= 33.7°C/W=42.3°C

Compal Electronics, Inc.

Title: +2.5VP

Size: C | Document Number | Rev: 0.1

Date: Tuesday, August 21, 2018 | Sheet 48 of 60



Vo	0.6	
Vin	1.2	
Io	0.75	
PD	0.455	
θJA(main) θJA(2nd)	52 68	°C/W

+0.6VSP
TDC=0.53A
Ipeak=0.75A

RT8207M:
Quiescent Current (GND Current)
IQ(typ)=0.47mA,IQ(max)=1mA
PD =(Vin-Vout)*Iout + Vin*IQ =0.455W
θJA= 33.7°C/W*0.903=23.66°C

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

+1.2VP
Vin = 20V
Iin =7.3*1.2/0.85/20
= 0.51A

Vout = Vfb*[1+(Rt/Rb)]
= 0.75*[1+(6.04K/10K)]
= 1.203V

+1.2VP
Imax=5.11A ; Ipeak=7.3A ;Fsw=285KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:12.1mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=11.79~12.01A
Iin_ripple=1.21A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.799A
LIR=Delta IL/Ipeak=0.246
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1365.71uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.51uF

Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: +1.2VP/+0.6VSP/+2.5VP

Size: Custom | Document Number | Rev: 0.1

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+VPCH_1.0VP
Ipeak=4.49A,Imax=3.143A ; Iocp=10A~14A

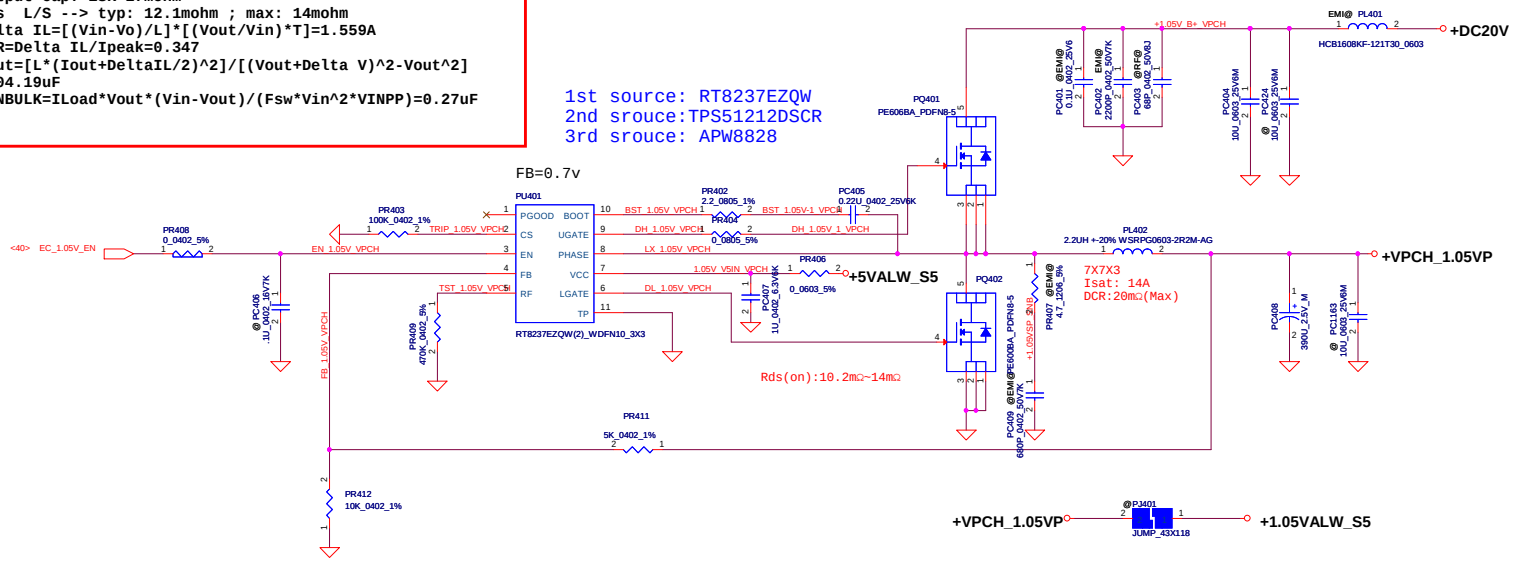
Fsw=290K
Iin_ripple= 0.75A
Output Cap. ESR=17mohm
Rds L/S --> typ: 12.1mohm ; max: 14mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.559A
LIR=Delta IL/Ipeak=0.347
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=504.19uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.27uF

Vout = Vfb*[1+(Rt/Rb)]
= 0.7*[1+(5K/10K)]
= 1.05V

+VPCH_1.0VP
Vin = 20V
Iin = 1.0*10.24/0.85/20
= 0.602A

1st source: RT8237EZQW
2nd srouce:TPS51212DSCR
3rd srouce: APW8828

FB=0.7v



Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

Compal Electronics, Inc.

Title: +VPCH_1.0VP/+12VSP

Size: Custom | Document Number | Rev: 0.1

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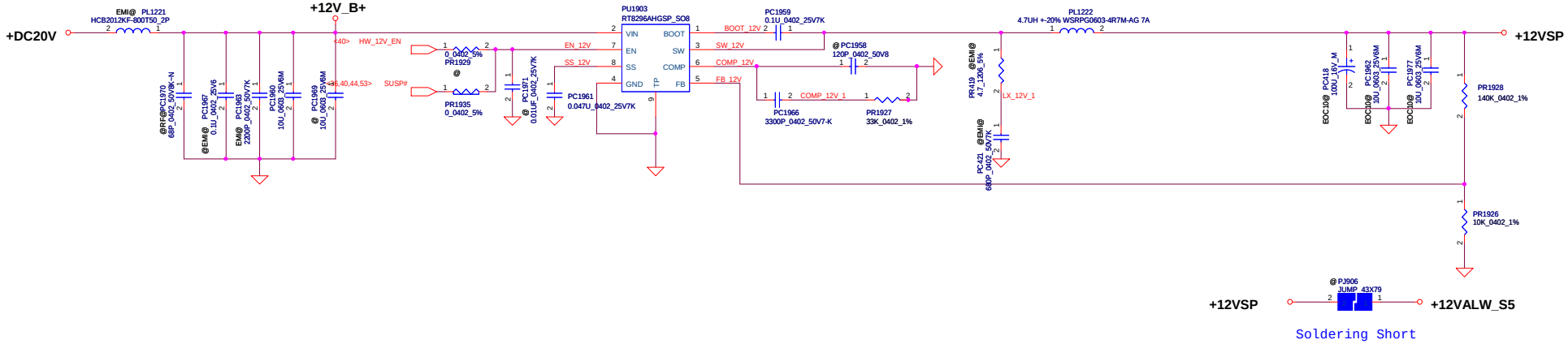
+12VSP
Vin = 20V
Iin = 12*1.83/0.85/20
= 1.29A

main source : RT8296A
second srouce:UP1735P

7X7X3
Isat: 13.5A
DCR: 40mΩ(Max)



Soldering Short

Vout = Vfb*[1+(Rt/Rb)]
= 0.8*[1+(140K/10K)]
= 12V

+12VSP
Imax=0.882A,Ipeak=1.26A ; Fsw=340KHz
Current Limit=4.1A(Min)
in_ripple=1.04A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=3.004A
LIR=Delta IL/Ipeak=0.75
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=10.24uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.27uF

Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2017/10/19

Compal Electronics, Inc.

Title: +12VSP

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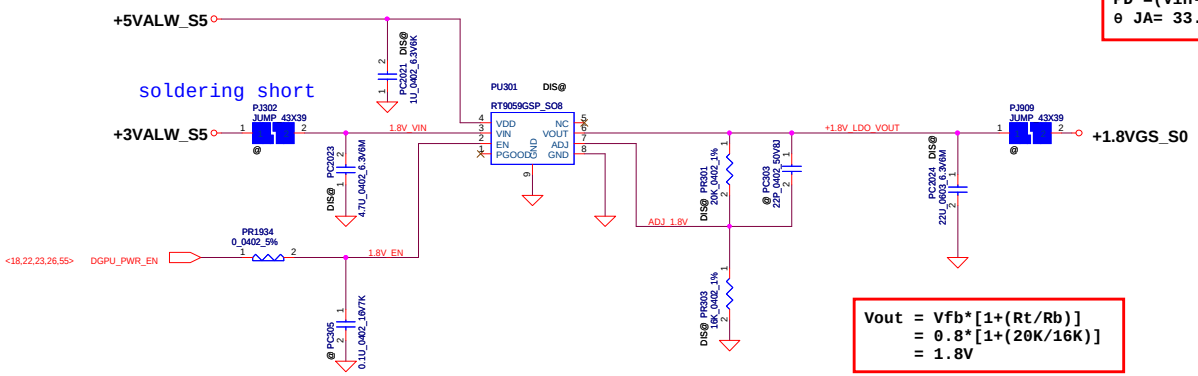



```
+1.8VALWP
Imax=0.3598, Ipeak=0.514A ;
Current Limit=3.6A(Typ)~4.2A(Max)

RT9059:
Quiescent Current (GND Current)
IQ(typ)=0.6mA
PD =(Vin-Vout)*Iout + Vin*IQ =0.542W
θ JA= 33.7°C/W=18.27°C
```

```
Vout = Vfb*[1+(Rt/Rb)]
     = 0.8*[1+(20K/16K)]
     = 1.8V
```

main source : RT9059GSP
second srouce: APL5933CKAI

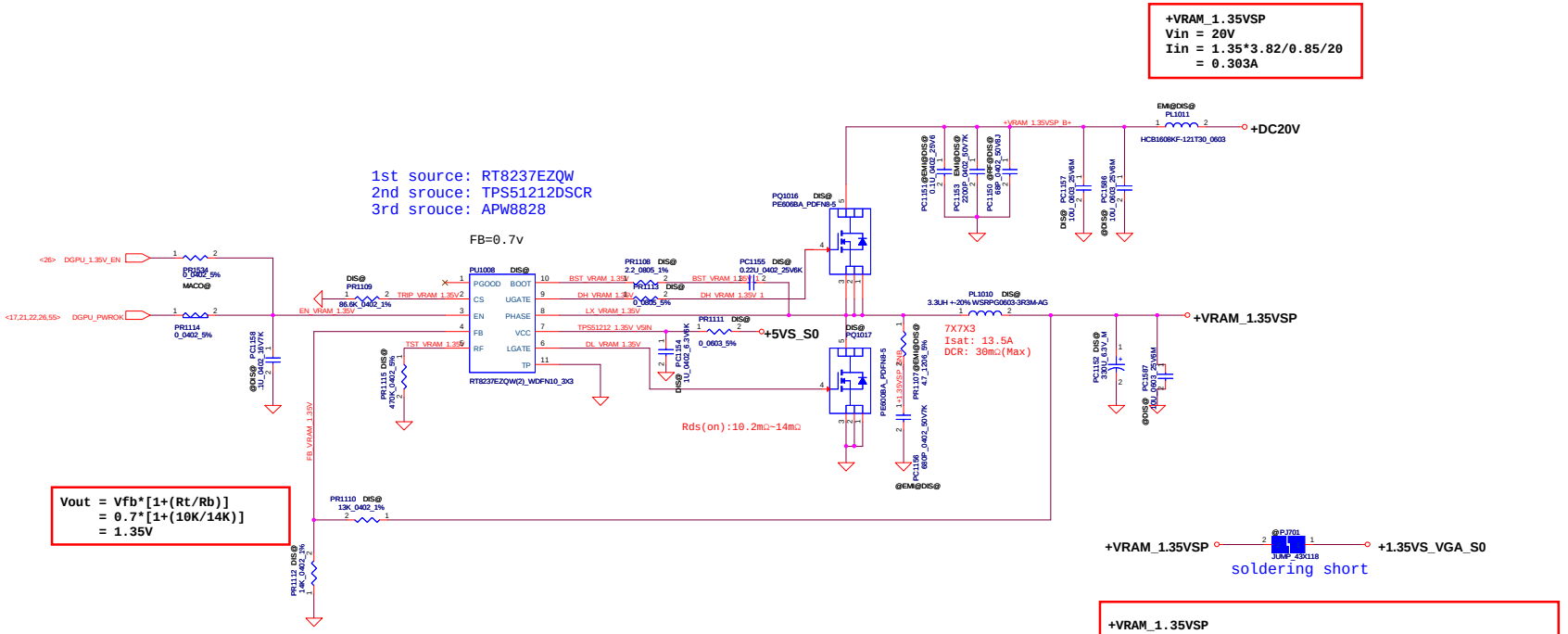
Security Classification	Compal Secret Data		
Issued Date	2014/12/26	Deciphered Date	2017/10/19

Compal Electronics, Inc.

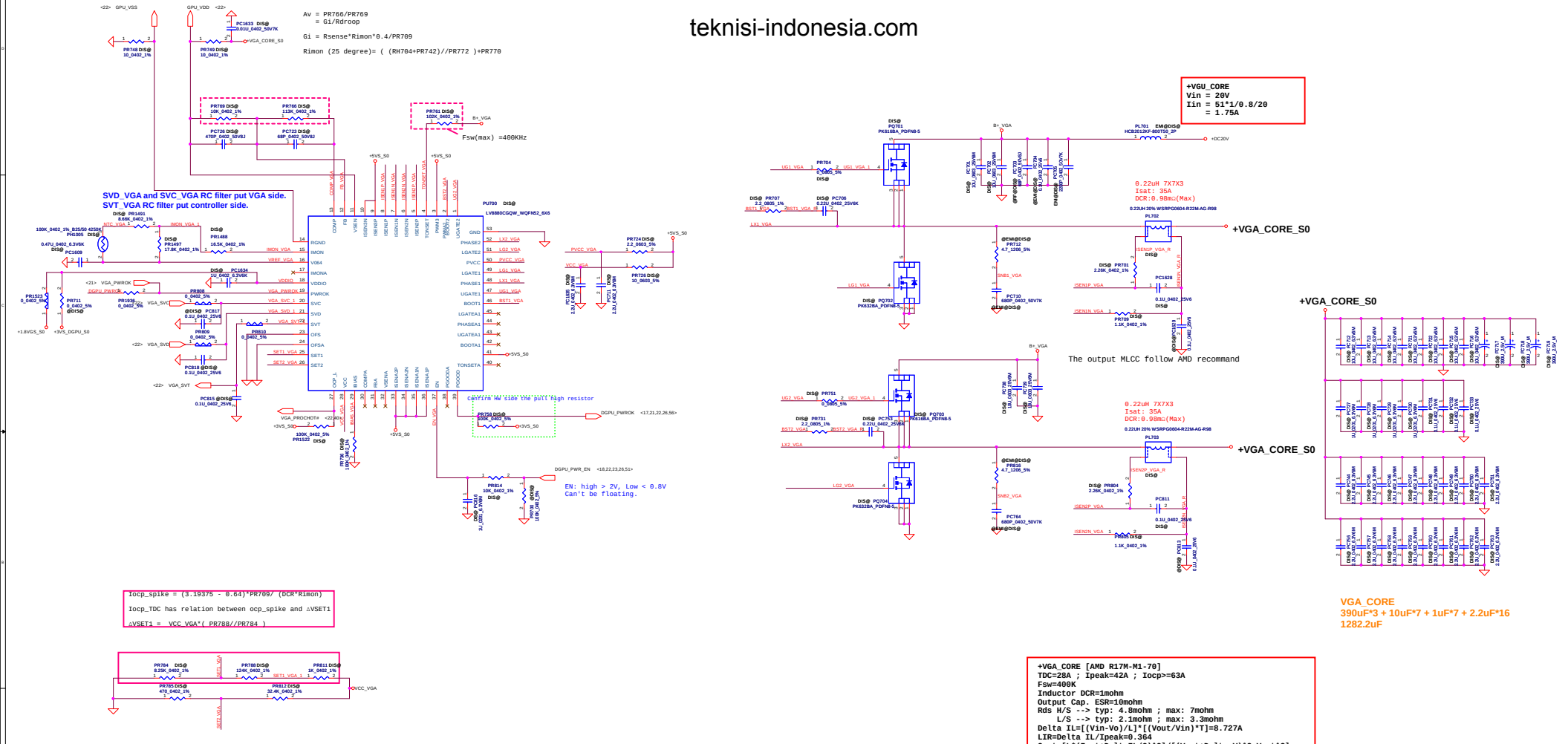
Title: *+1.8VALWP*

Size	Document Number	Rev
		0.1

Date: Tuesday, August 21, 2018 | Sheet 52 of 63

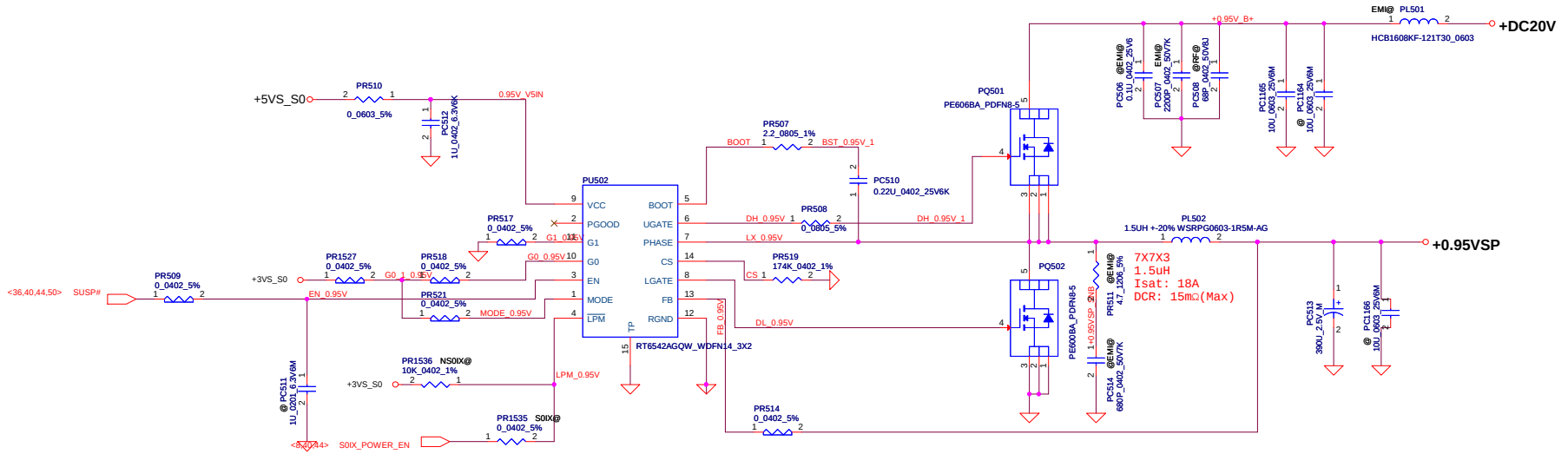


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/08/29	Deciphered Date	2013/08/29
Title	VRAM_1.35V		
Size	Document Number		Rev 0.1
Date: Tuesday, August 21, 2018	Sheet 54 of 60		



+VGA_CORE [AMD R17M-M1-70]
TDC=28A ; Ipeak=42A ; Iocp>=63A
Fsw=400K
Inductor DCR=1mohm
Output Cap. ESR=1~9mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=8.727A
LIR=Delta IL/Ipeak=0.364
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1502.1uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.81uF

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/08/29	Deciphered Date 2013/08/29	Title: VGA_CORE(RT8813)
Size	Document Number		Rev: 0.1
Date: Tuesday, August 21, 2018	Sheet 55 of 60		

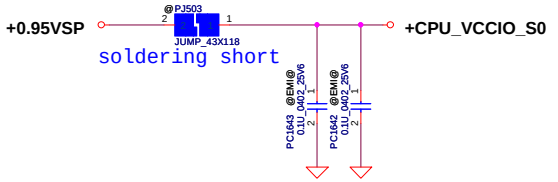


NS0IX@ for non-morden standby

```
+0.95VSP
Imax=5.845,Ipeak=8.35A ;Fsw=290KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=11.3~13.59A
Iin_ripple=1.24A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.08A
LIR=Delta IL/Ipeak=0.249
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1293.74uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.46uF
```

```
+0.95VSP
Vin = 20V
Iin =0.95*8.35/0.85/20
    = 0.466A
```

VR	LPM	G1	G0	Vout
VCCIO	1	0	1	0.95V



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2017/10/19

Title	+CPU_VCCIO_+0.95VSP		
Size Custom	Document Number		Rev 0.1
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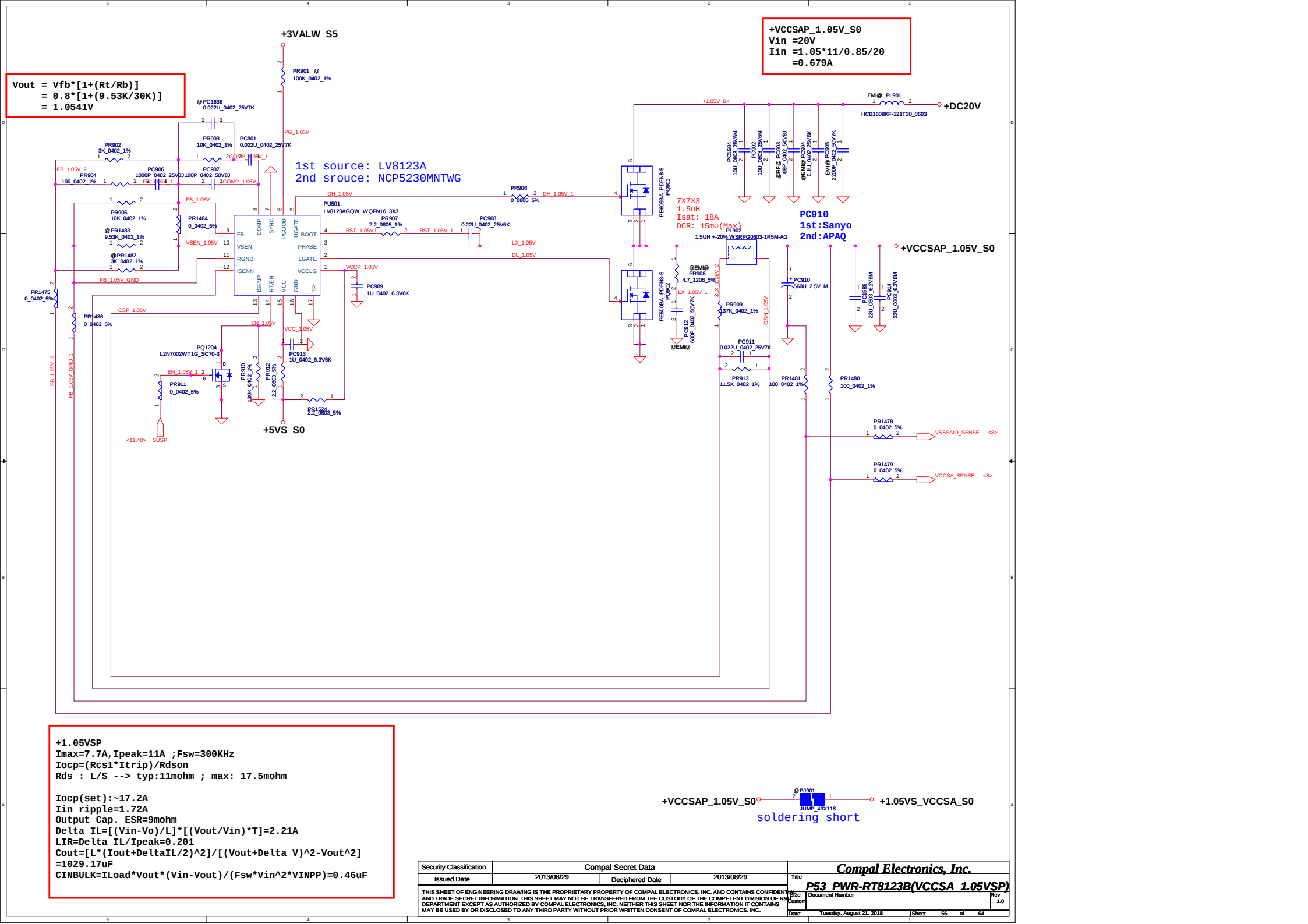


Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

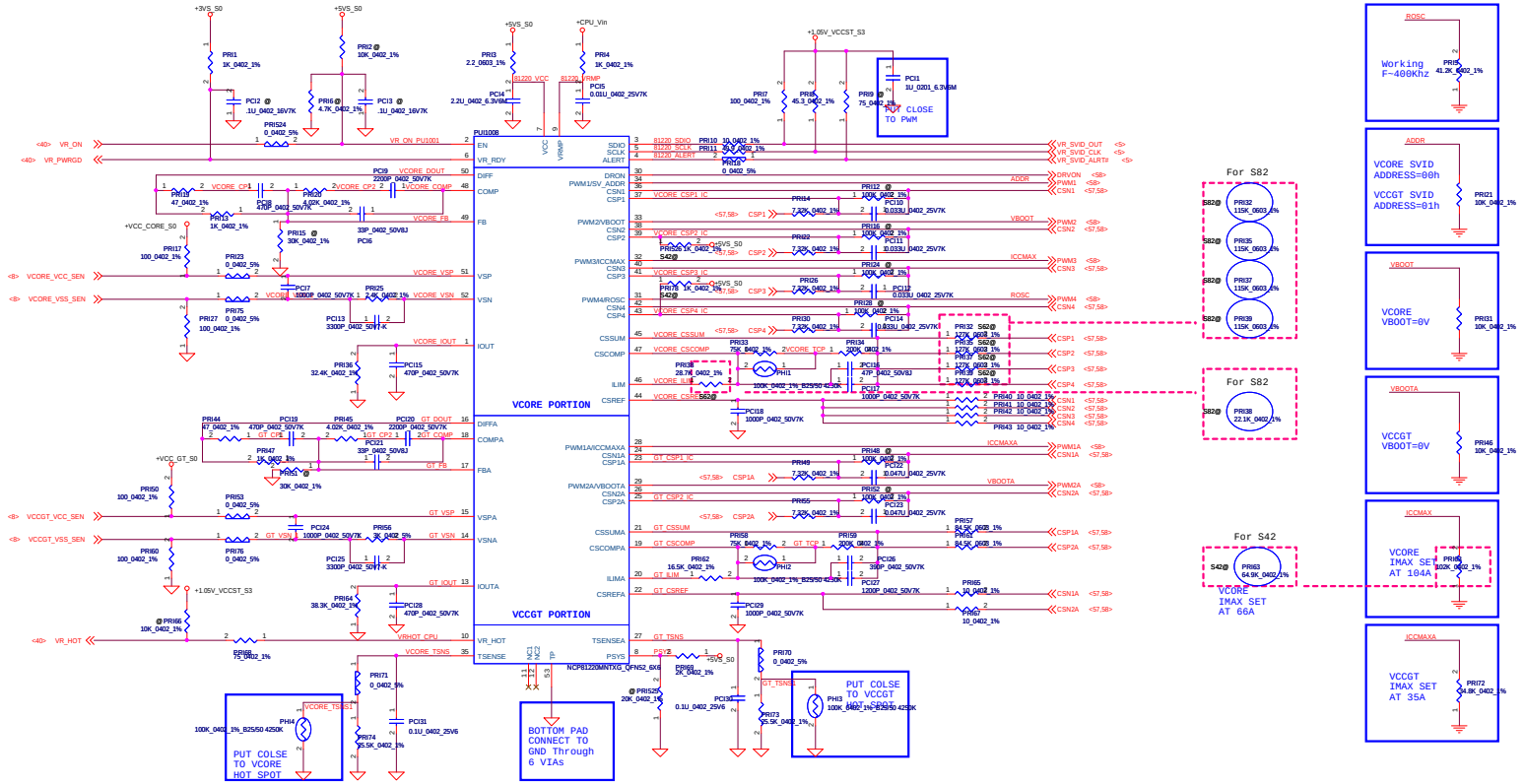
Compal Electronics, Inc.

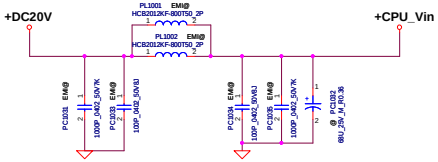
Title: P53_PWR-RT8123B(VCCSA_1.05VSP)

Size: Custom | Document Number | Rev: 1.0

Date: Tuesday, August 21, 2018 | Sheet 56 of 64

Intel Coffeelake IMVP8 POWER CFL - S-LINE 82/62/42/22 35W 4+2 PHASE





CFL-S-LINE 82/62/42/22 35W

+CPU_CORE
TDC=74A,Ipeak=104A Fsw=400K,OCP:135A ~ 176.8A
Inductor DCR=1.1mohm
Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=6.267A
LIR=Delta IL/Ipeak=0.241
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1110.03
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.03uF

+GFX_CORE
TDC=25A,Ipeak=35A Fsw=400K,OCP:45.5A ~59.5A
Inductor DCR=1.1mohm
Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=6.267A
LIR=Delta IL/Ipeak=0.358
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=577.19uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.69uF

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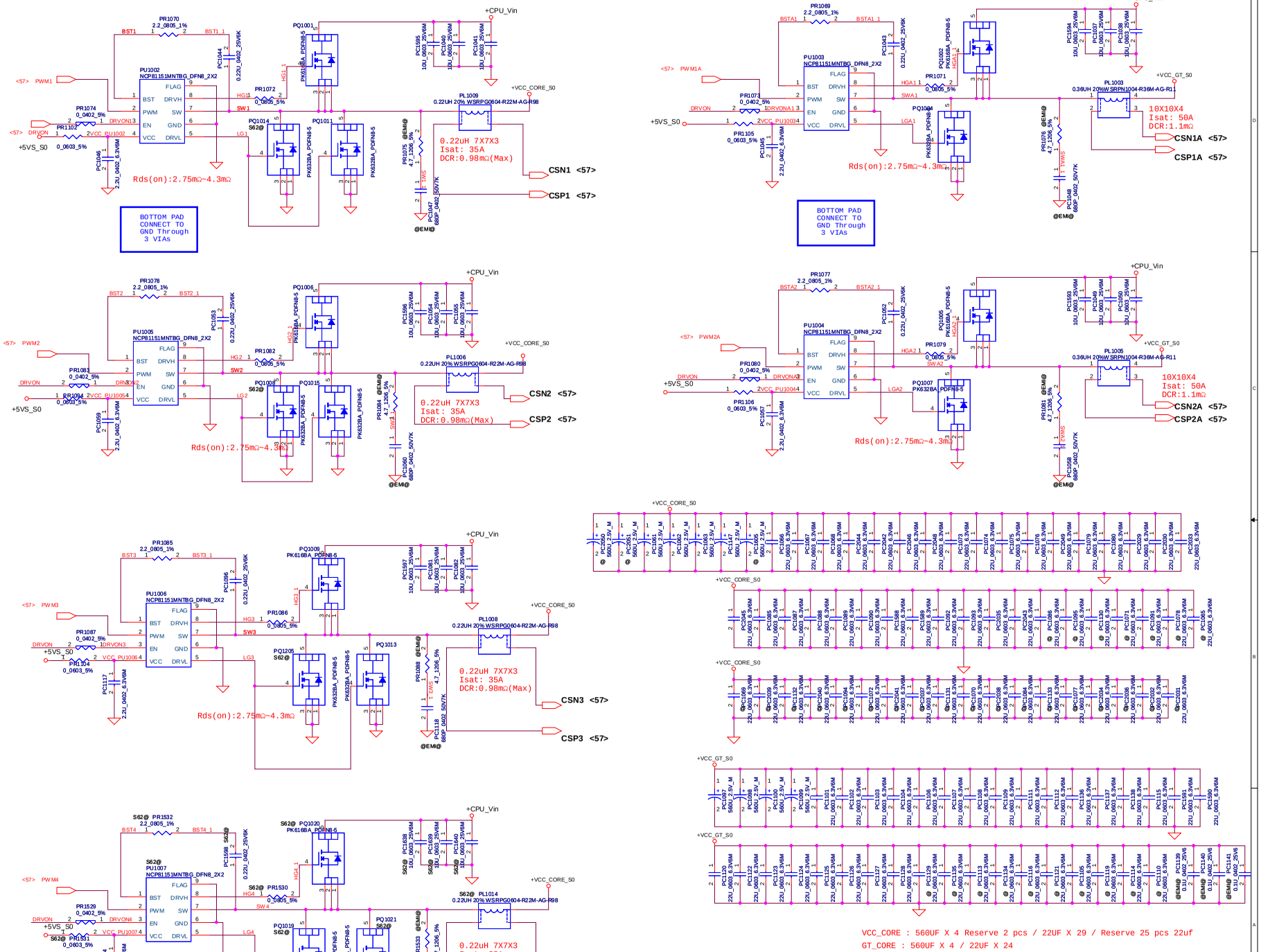
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2017/10/19

Title	CPU_CORE_1		
Size	Document Number		Rev
Custom			0.1
Date:	Tuesday, August 21, 2018	Sheet	56 of 60



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Issued Date	2010/01/25	Deciphered Date	2017/10/19

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Title: CPU_CORE_2

Size	Document Number	Rev
Custom		0.1

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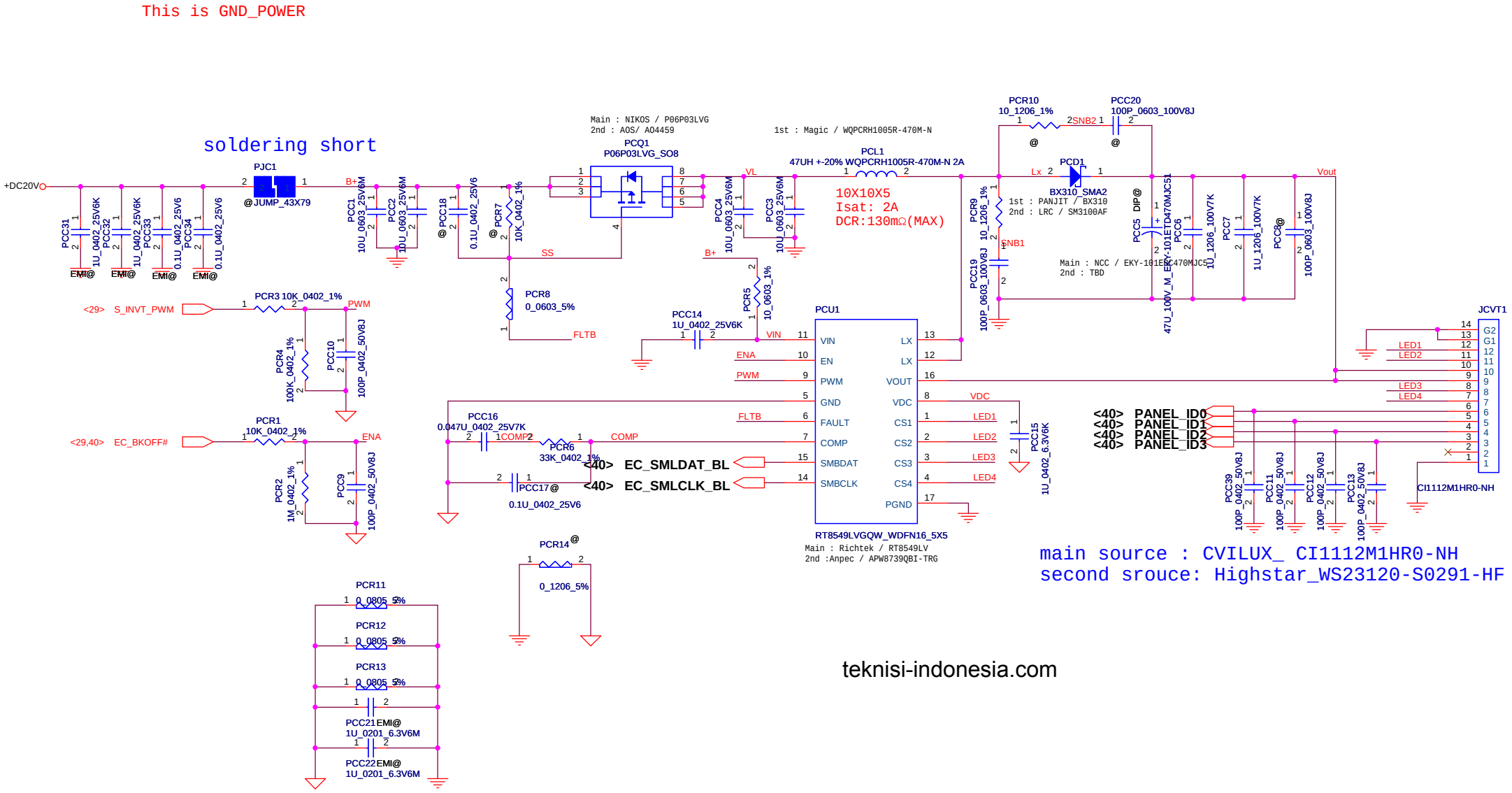
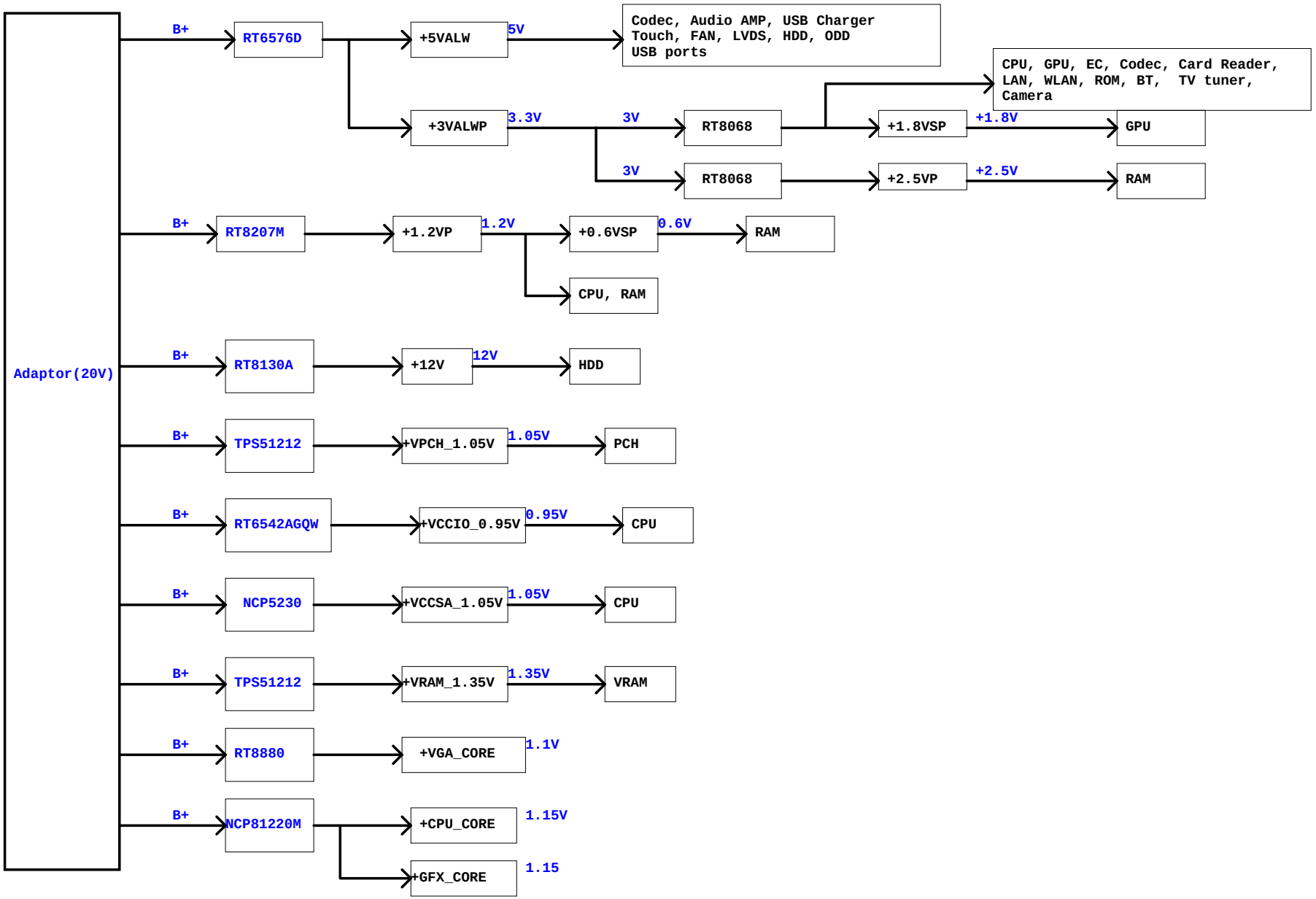


Security Classification	Compal Secret Data		
Issued Date	2015/11/25	Deciphered Date	2015/11/25

Compal Electronics, Inc.			
Title	CONVERTER/B		
Size B	Document Number	LA-D952P M/B	Rev 0.1
Date:	Sheet 58 of 60		



Security Classification	Compal Secret Data		
Issued Date	2013/12/18	Deciphered Date	2013/12/18

Compal Electronics, Inc.

Title: **Power Rail**

Size	Document Number	Rev
Custom		0.1

Date: Tuesday, August 21, 2018 Sheet 60 of 60