EA40-CX
UMA/Muxless Schematics Document
Ivy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

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Title		
Cover Page		
Size A3	Document Number EA40 CX	Rev -3
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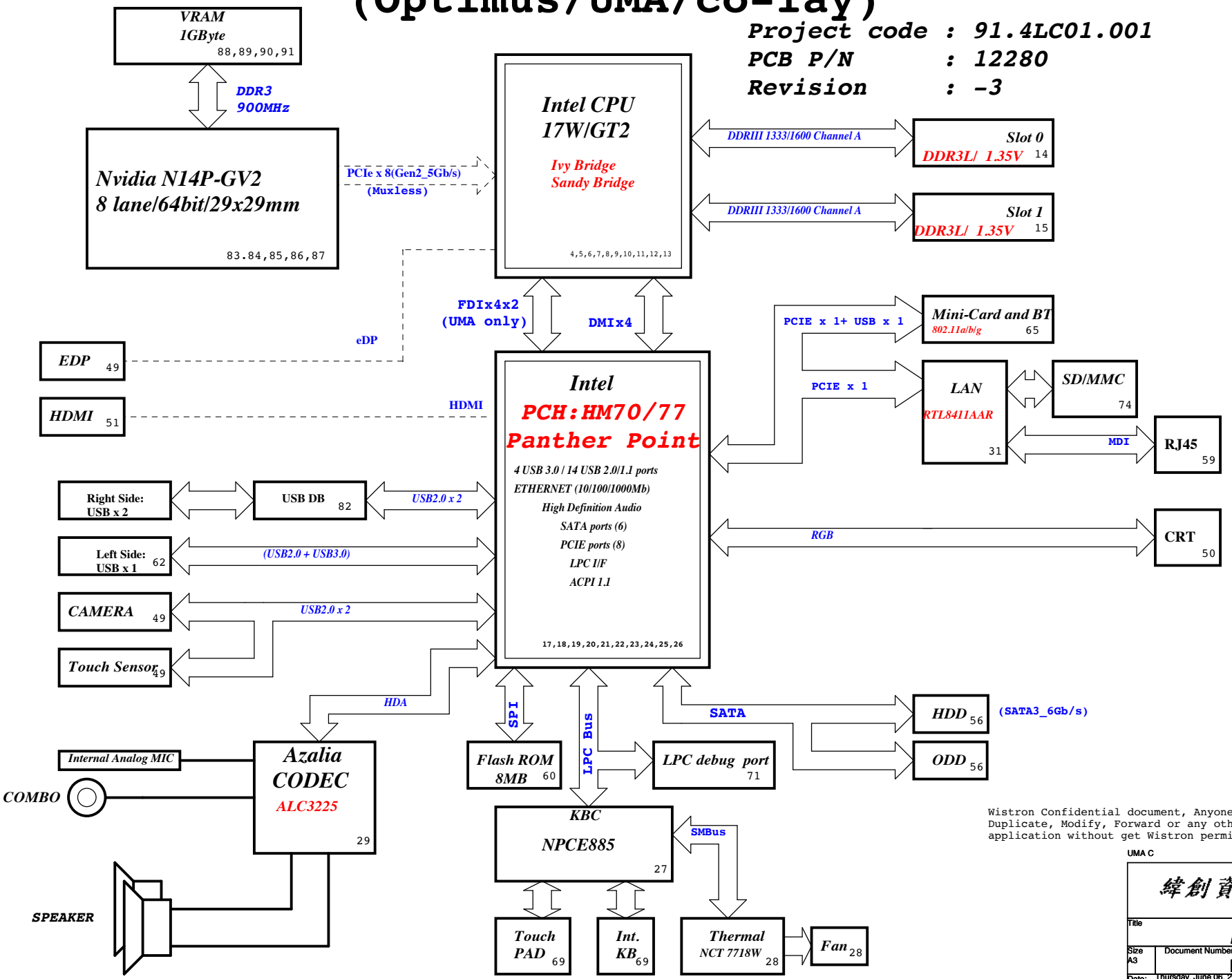
EA40_CX Block Diagram (Optimus/UMA/co-lay)

Project code : 91.4LC01.001
PCB P/N : 12280
Revision : -3



CHARGER BQ24727 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT8223MGQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

CPU DC/DC ISL95833HRTZ 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC ISL95833HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC SY8208D 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8207L 46	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0 DDR_VREF_S3

LDO RT9025-25ZSP 47	
INPUTS	OUTPUTS
3D3V_S0 3D3V_S0	1D8V_S0 1D5V_S0

LDO G978 48	
INPUTS	OUTPUTS
1D05_VTT	0D85V_S0

VGA ISL62882CHRTZ 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

SY8208D/TPS22966D 93	
INPUTS	OUTPUTS
DCBATOUT 3D3V_S0 1D05V_VTT	1D5V_VGA_S0 3D3V_VGA_S0 1D05V_VGA_S0

PCB LAYER

L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	N/A
2	N/A
3	N/A
4	ODD
5	ESATA

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address / Hex / Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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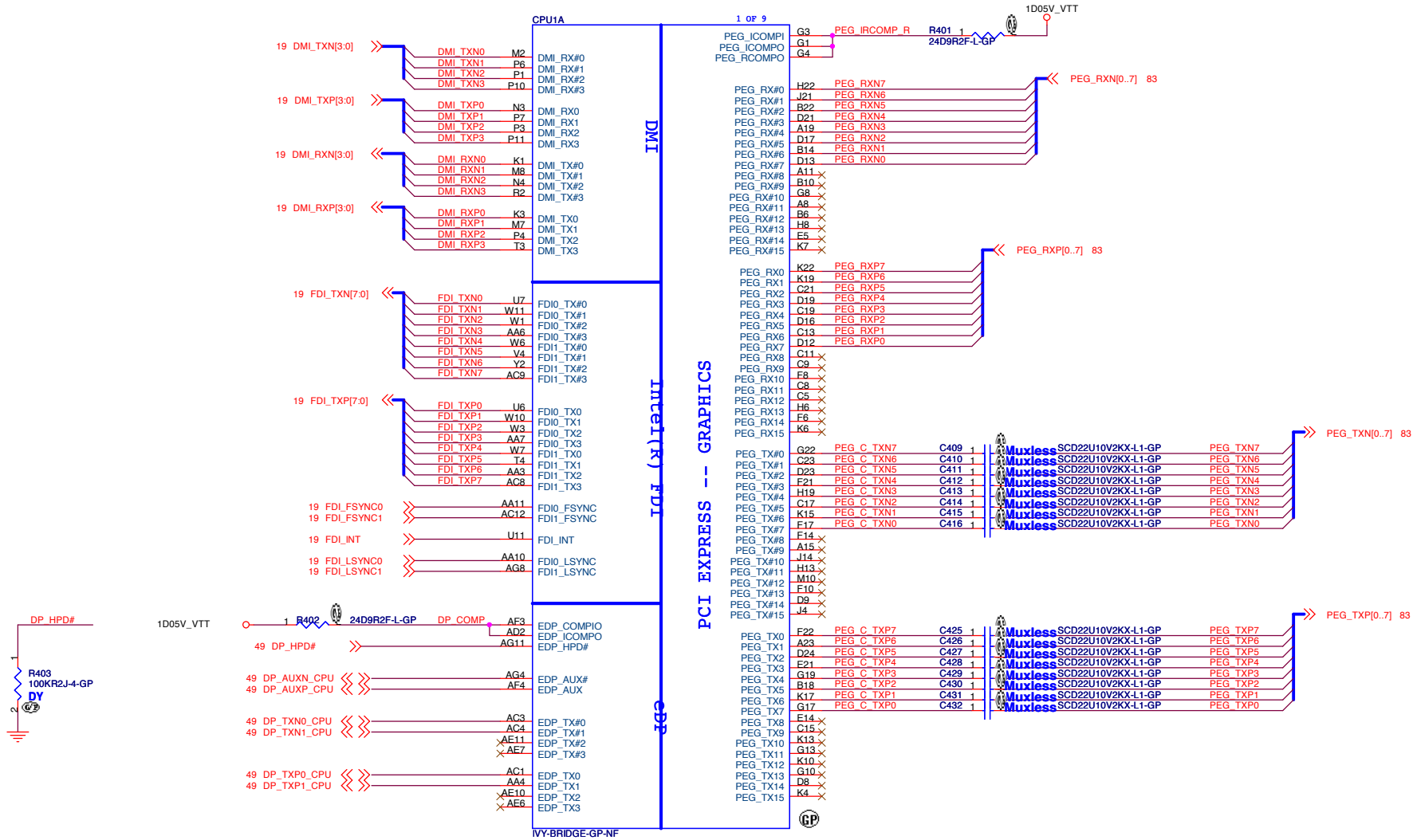
Title: Table of Content

Size: A3 | Document Number: EA40 CX | Rev: -3

Date: Thursday, June 06, 2013 | Sheet 3 of 103

SSID = CPU



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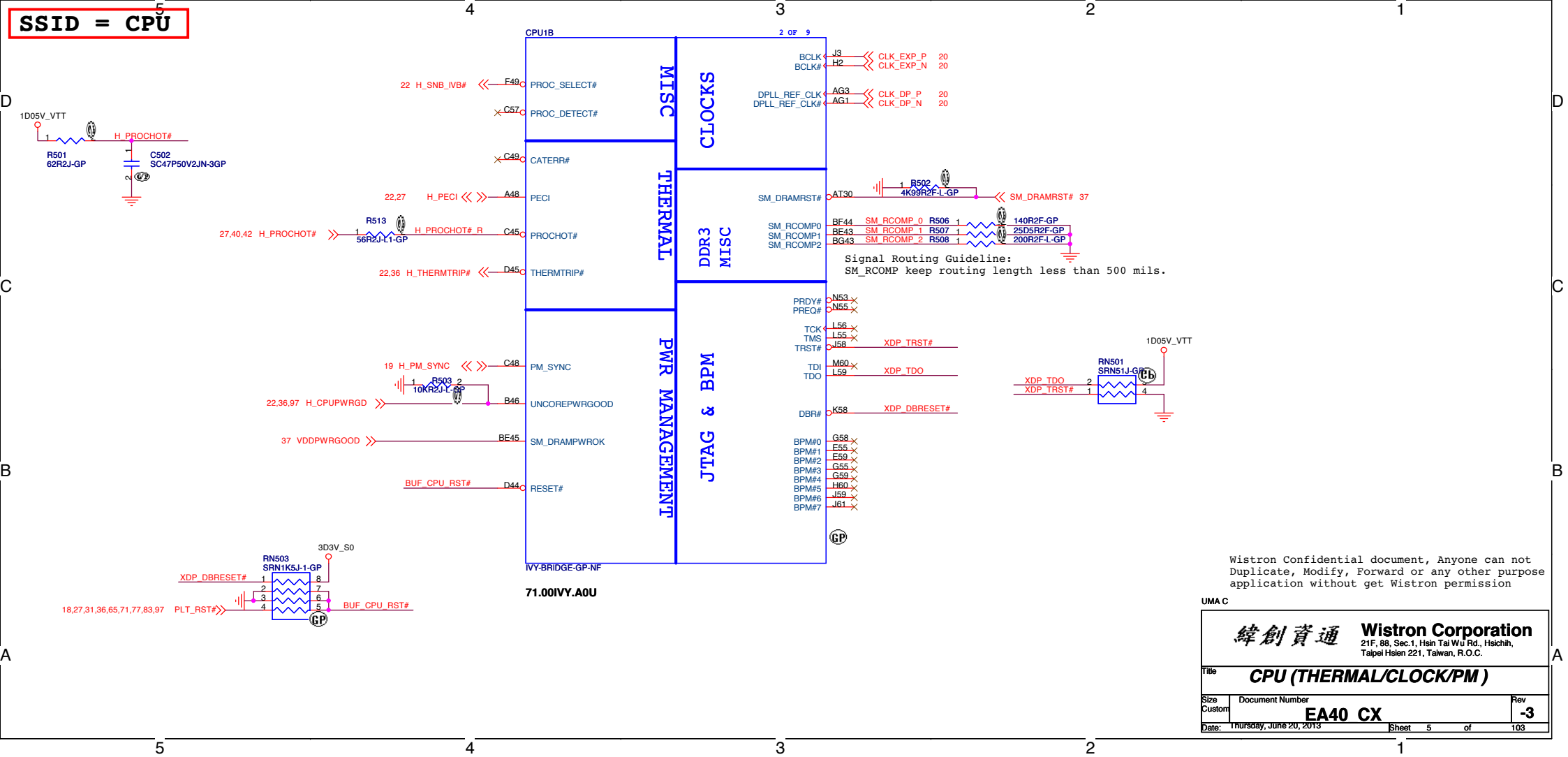
Title: **CPU (PCIE/DMI/FDI)**

Size	Document Number	Rev
A3	EA40 CX	-3

Date: Thursday, June 20, 2013 Sheet 4 of 103

SSID = CPU



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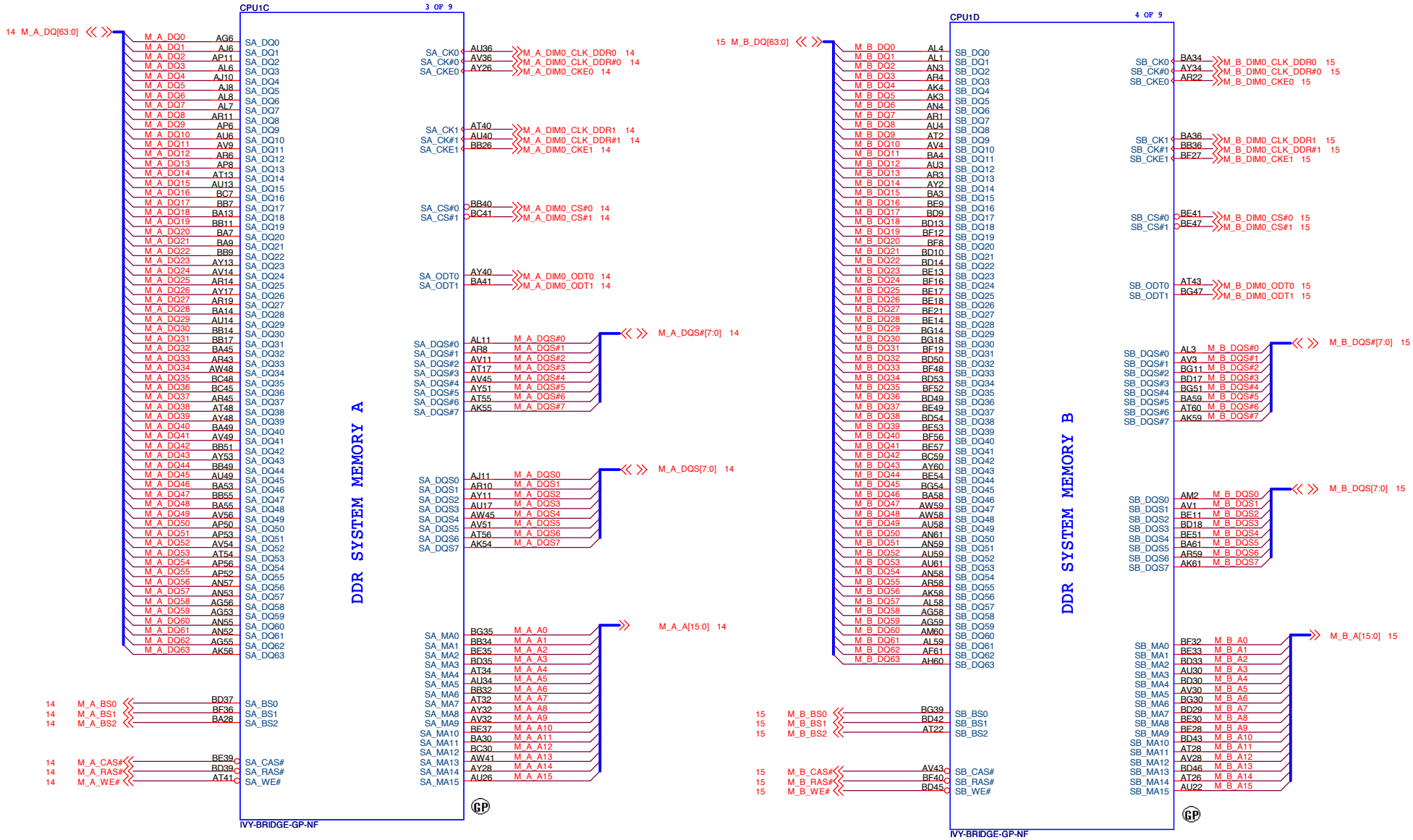
Title	CPU (THERMAL/CLOCK/PM)	
Size: Custom	Document Number: EA40 CX	Rev: -3
Date: Thursday, June 20, 2013	Sheet 5 of 103	

SSID = CPU



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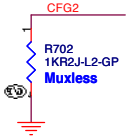
Title: CPU (DDR)

Size	Document Number	Rev
A3	EA40_CX	-3

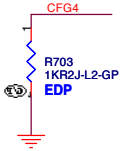
Date: Thursday, June 20, 2013 Sheet 6 of 103

SSID = CPU

PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

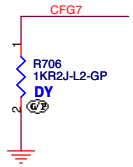


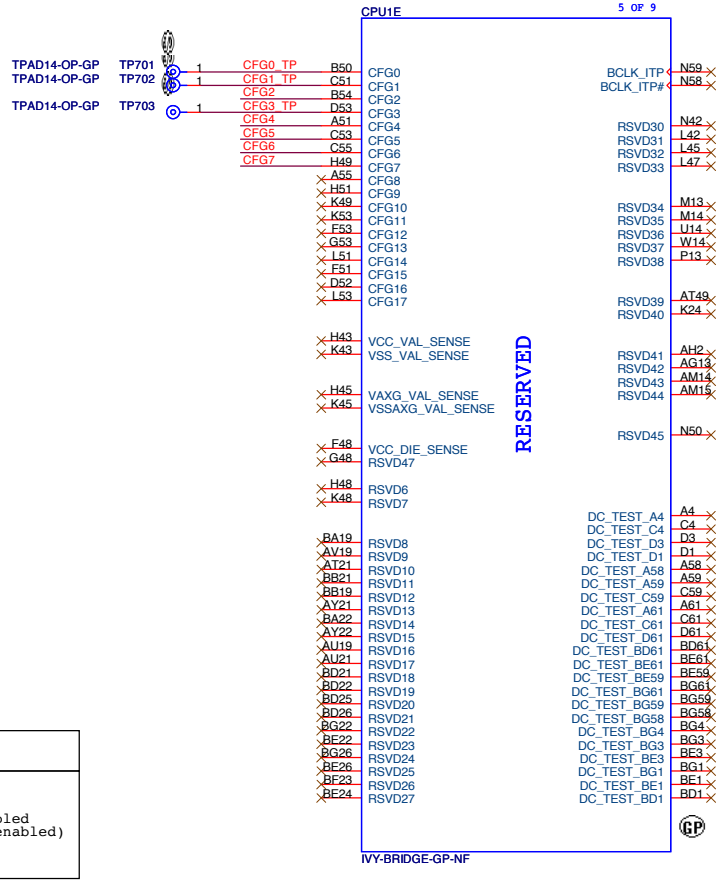
Enabl EDP function	
CFG4	1:Disable 0:Enable



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training





71.00IVY.A0U

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Title: CPU (RESERVED)

Size: A3 | Document Number: EA40_CX | Rev: -3

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SSID = CPU

POWER

ULV:17W
Iccmax:33A
ICC_TDC:25A

Iccmax:8.5A
ICC_TDC:8.5A

CPU1F

6 OF 9

CORE SUPPLY

PEG IO AND DDR IO

QUIET RAILS

SVID

SENSE LINES

IVY-BRIDGE-GP-NF

71.00IVY.A0U

SA_20111022-1

SA_20111024-3

SA_20111023-1

Place near processor

Place near processor

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Title: CPU (VCC_CORE)

Size: Custom | Document Number: EA40_CX | Rev: -3

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SSID = CPU

POWER

CPU1G — 7 OF 9

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

VCC_GFXCORE

Iccmax:18A(GT1)
ICC_TDC:12A(GT1)

SC10U6D3V3MX-L-GP C902 DY, C903 DY, C904 DY, C905 DY, C906 DY, C907 DY, C908 DY, C909 DY, C914 DY, C916 DY, C920 DY, C921 DY

SC1U6D3V2KX-L-1-GP

GRAPHICS

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54 VAXG55 VAXG56

VREF

SM_VREF — AY43 — +V_SM_VREF_CNT 37

SA_DIMM_VREFDQ — BE7 — M_VREF_DQ_DIMM0_C — M_VREF_DQ_DIMM0_C 37

SB_DIMM_VREFDQ — BG7 — M_VREF_DQ_DIMM1_C — M_VREF_DQ_DIMM1_C 37

BE7 and BG7 is NC ball in HR

RN902 SRN1KJ-7-GP DY

DDR3 - 1.5V RAILS

VDDQ1 AJ28, VDDQ2 AJ33, VDDQ3 AJ36, VDDQ4 AJ40, VDDQ5 AL30, VDDQ6 AL34, VDDQ7 AL38, VDDQ8 AL42, VDDQ9 AM33, VDDQ10 AM36, VDDQ11 AM40, VDDQ12 AN30, VDDQ13 AN34, VDDQ14 AN38, VDDQ15 AP26, VDDQ16 AP28, VDDQ17 AP30, VDDQ18 AP32, VDDQ19 AP34, VDDQ20 AP36, VDDQ21 AP40, VDDQ22 AV41, VDDQ23 AW26, VDDQ24 BA40, VDDQ25 BB28, VDDQ26 BG33

Iccmax:5A

1D35V_S0

SC10U6D3V3MX-L-GP C910, C911, C912 DY, C913 DY; SC1U6D3V2KX-L-1-GP C924 DY, C925, C918, C916, C917, C926 DY

QUIET RAILS

PROCESSOR DDR 1.5V QUIET RAIL (BGA only)
+V1.5S_VCCD_Q should be short to +V1.5S_VCCDDQ on board

VCCDQ1 AM28, VCCDQ2 AN26 — +1.5S_VCCD_Q — R909 0R0402-PAD — C923 SC1U6D3V2KX-L-1-GP

1D35V_S0

SENSE LINES

VAXG_SENSE F45, VSSAXG_SENSE G45

44 VCC_AXG_SENSE
44 VSS_AXG_SENSE

VCC_GFXCORE

R906 100R2F-L1-GP-U — R906,R907 close to CPU — R907 100R2F-L1-GP-U

VCC_AXG_SENSE
VSS_AXG_SENSE

1.8V RAIL

1D8V_S0

ICC_MAX:1.2A

C922 SC1U10V2KX-1GP

VCCPLL1 BB3, VCCPLL2 BC1, VCCPLL3 BC4

SENSE LINES

VDDQ_SENSE BC43 TP_VDDQ_SENSE — TP901 TPAD14-OP-GP
VSS_SENSE_VDDQ BA43 TP_VDDQ_VSS — TP902 TPAD14-OP-GP

SA RAIL

0D85V_S0

ICC_MAX:6A

C915 SC10U6D3V3MX-L-GP

VCCSA1 L17, VCCSA2 L21, VCCSA3 N16, VCCSA4 N20, VCCSA5 N22, VCCSA6 P17, VCCSA7 P20, VCCSA8 R16, VCCSA9 R18, VCCSA10 R21, VCCSA11 U15, VCCSA12 V16, VCCSA13 V17, VCCSA14 V18, VCCSA15 V21, VCCSA16 W20

VCCSA_SENSE U10 — VCCSA_SENSE

0D85V_S0 — R902 100R2F-L1-GP-U — R902 need be close to pin U10.

VCCSA VID lines

VCCSA_VID0 D48 — VCCSA_VID0
VCCSA_VID1 D49 — VCCSA_VID1

VCCSA_VID[0]	VCCSA_VID[1]	Selected VCCSA (XE & SV segments)	Selected VCCSA (ULV segment)
0	0	0.9 V	0.9 V
0	1	0.8 V	0.85 V
1	0	0.725 V	0.775 V
1	1	0.675 V	0.75 V

1D05V_VTT

R908 10KR2J-L-GP DY — R912 10KR2J-L-GP DY
R913 10KR2J-L-GP — R914 10KR2J-L-GP

VCCSA_VID0 — VCCSA_VID0 48
VCCSA_VID1 — VCCSA_VID1 48

IVY-BRIDGE-GP-NF

71.00IVY.A0U

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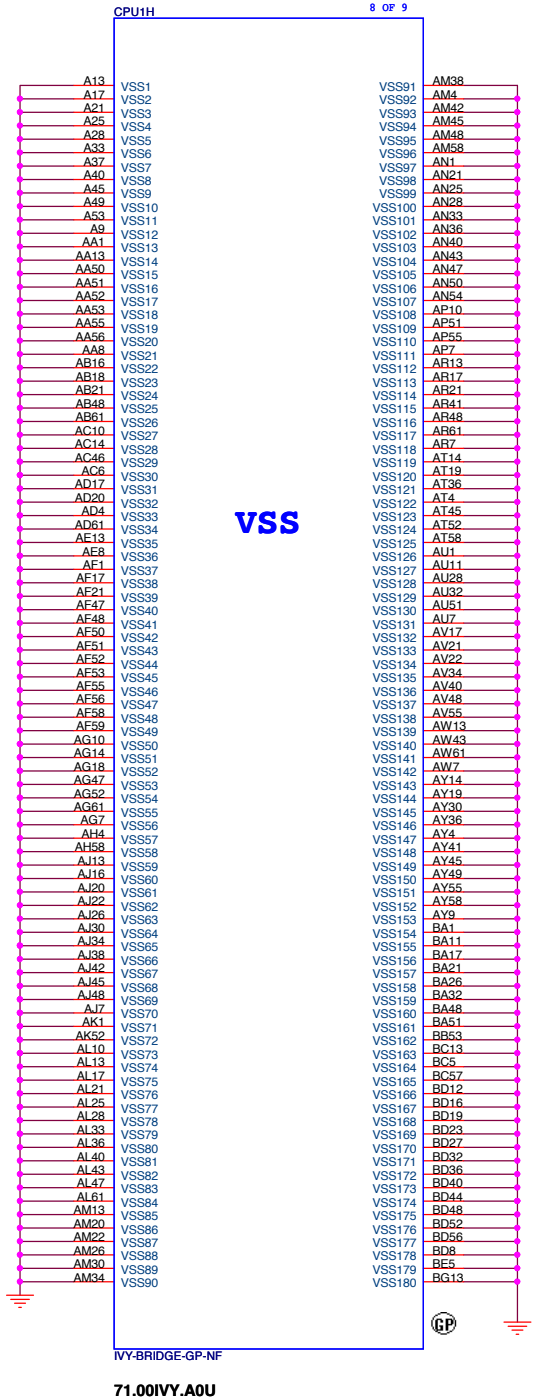
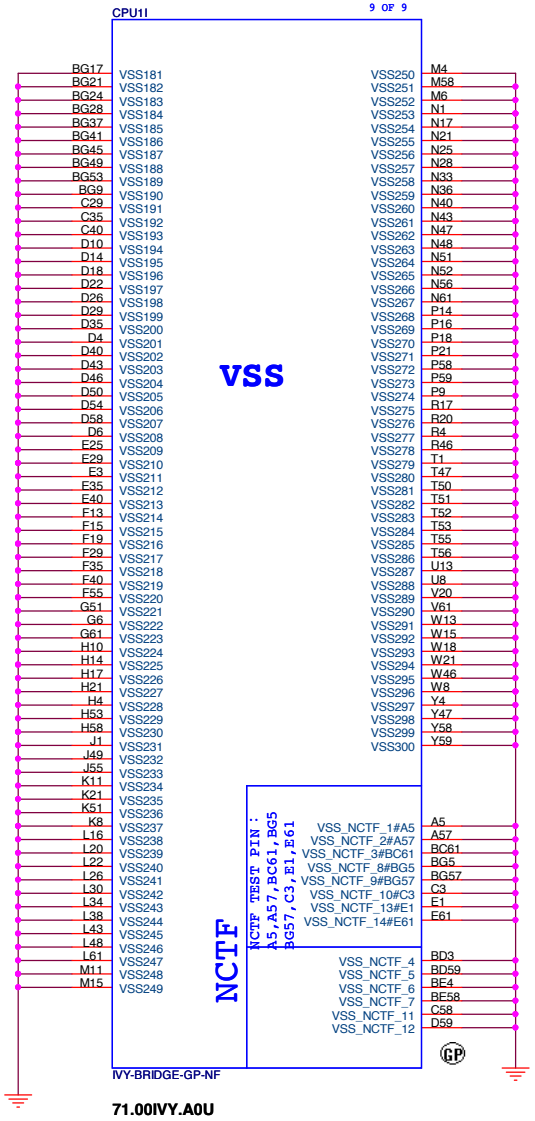
Title: CPU (VCC_GFXCORE)
Size: Custom | Document Number: EA40_CX | Rev: -3
Date: Thursday, June 20, 2013 | Sheet 9 of 103

SSID = CPU





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Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	EA40_CX	-3

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UMA C

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Title		
	XDP	
Size: A3	Document Number: **EA40_CX**	Rev: **-3**
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Title: ***Reserved***

Size	Document Number	Rev
A4	EA40_CX	-3

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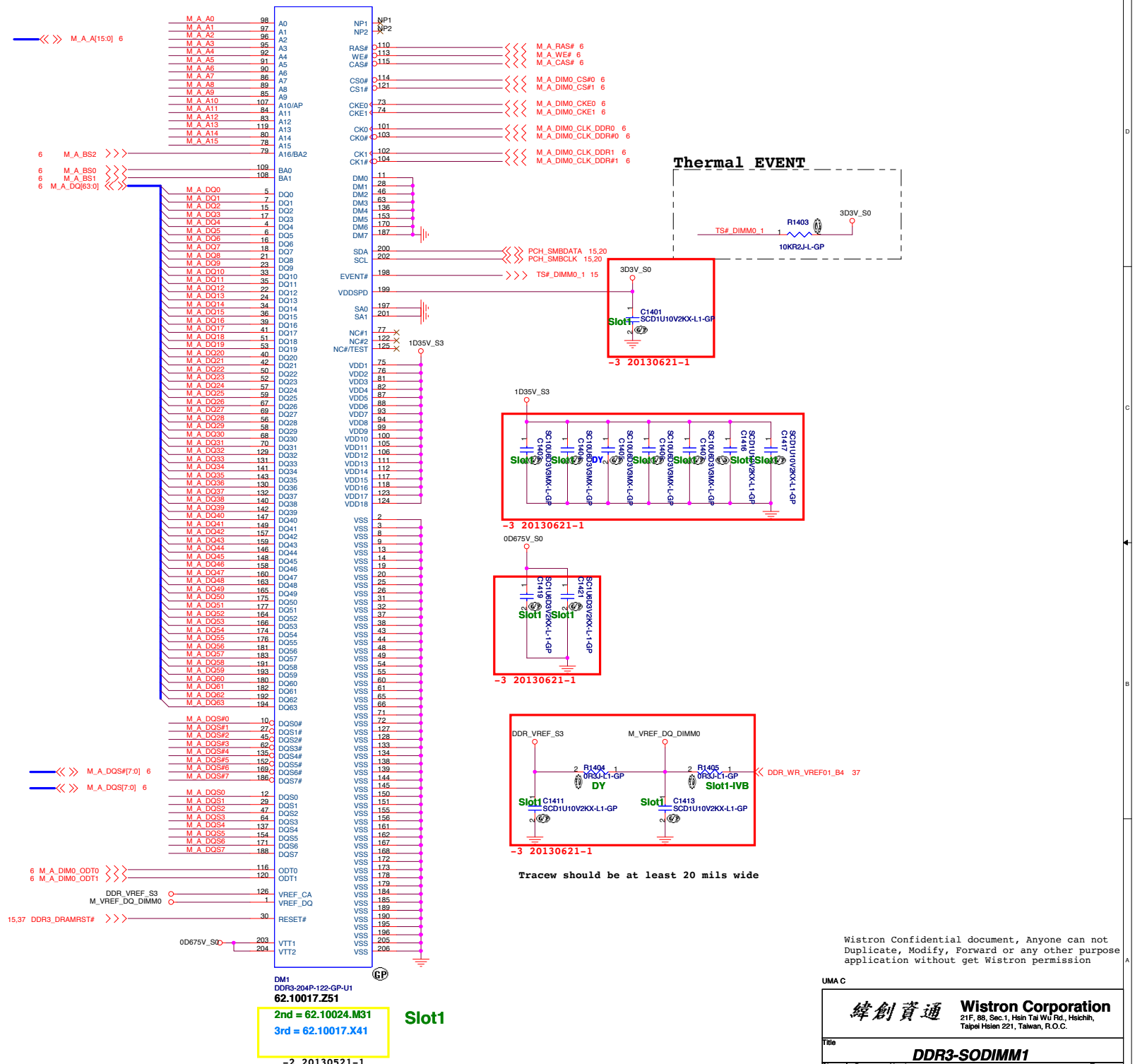
Title: ***Reserved***

Size	Document Number	Rev
A4	EA40_CX	-3

Date: Thursday, June 06, 2013 Sheet 13 of 103

SSID = MEMORY



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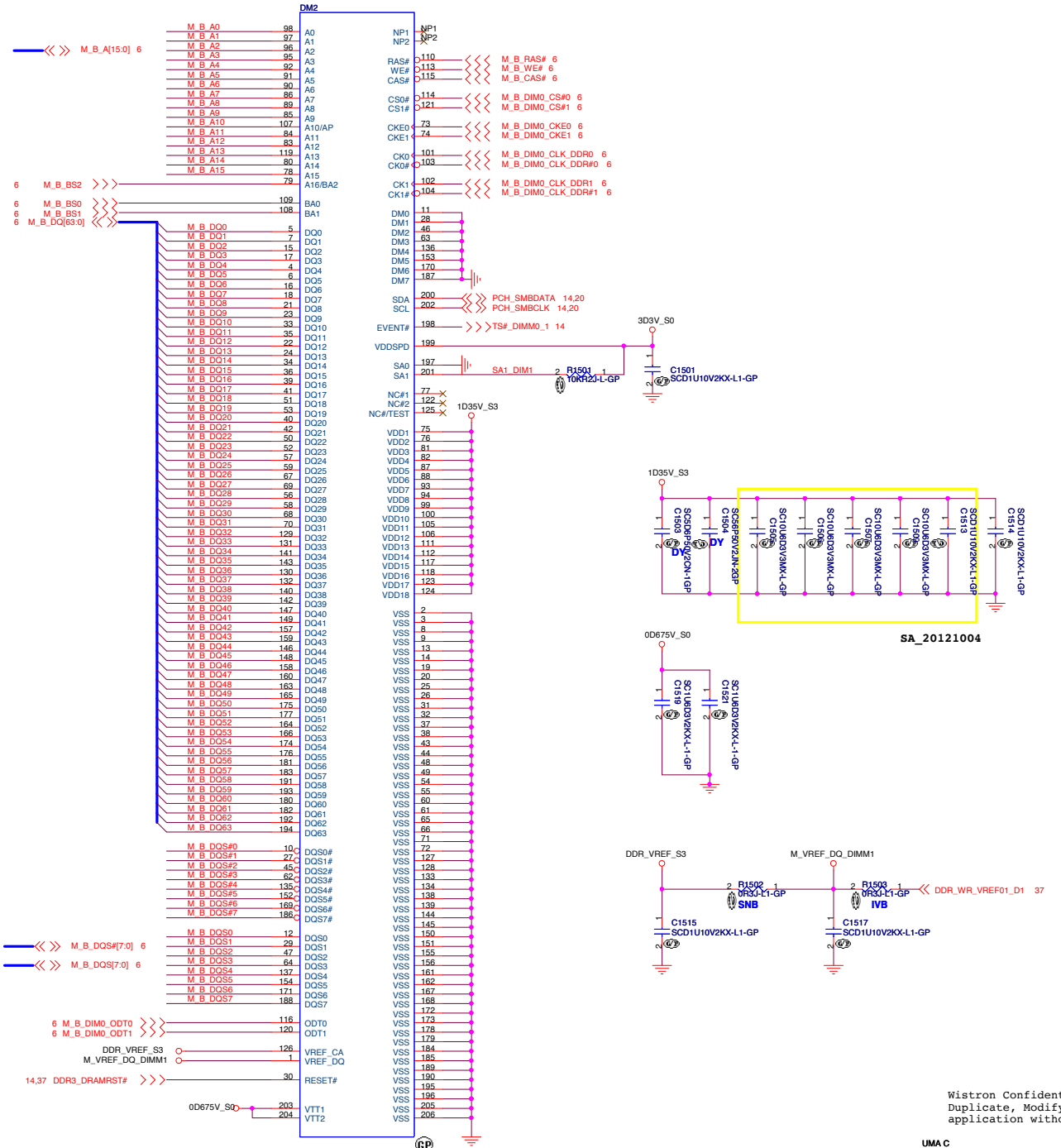
Title: DDR3-SODIMM1

Size	Document Number	Rev
Custom	EA40_CX	-1

Date: Friday, June 21, 2013 Sheet 14 of 103

SSID = MEMORY



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Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
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Date: Thursday, June 06, 2013 Sheet 15 of 103

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Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	EA40_CX	-3

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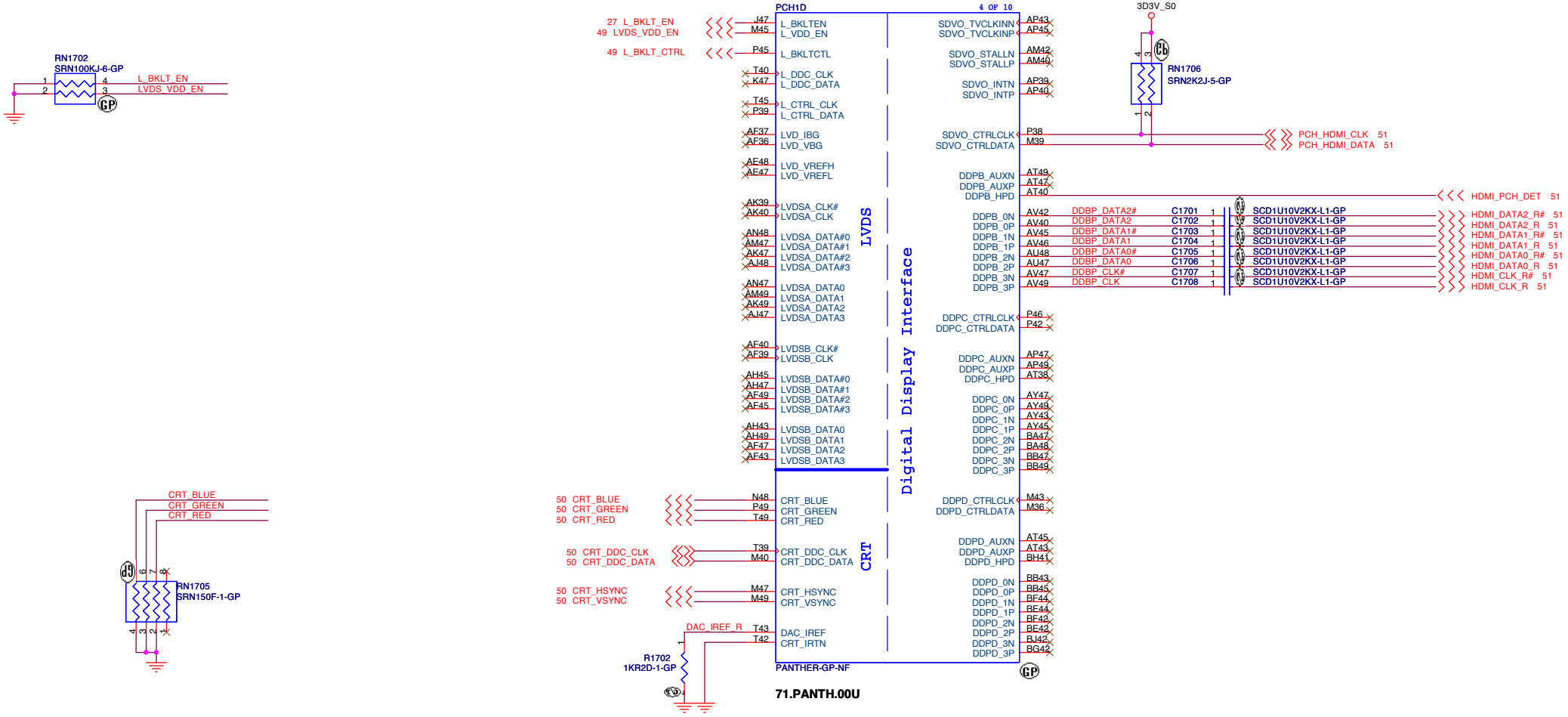

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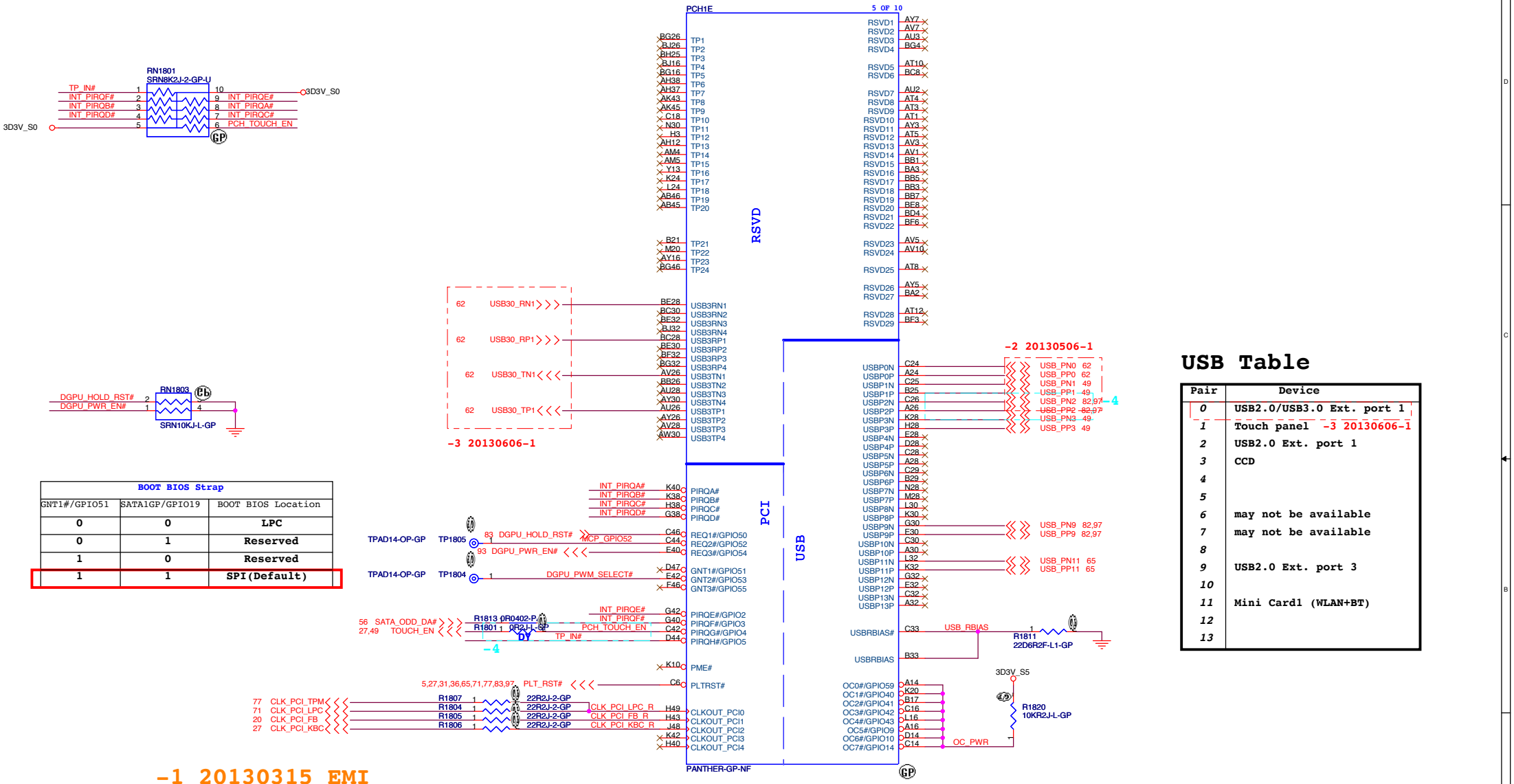
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	EA40_CX	-3

Date: Thursday, June 20, 2013 Sheet 17 of 103

SSID = PCH



USB Table

Pair	Device
0	USB2.0/USB3.0 Ext. port 1
1	Touch panel -3 20130606-1
2	USB2.0 Ext. port 1
3	CCD
4	
5	
6	may not be available
7	may not be available
8	
9	USB2.0 Ext. port 3
10	
11	Mini Card1 (WLAN+BT)
12	
13	

BOOT BIOS Strap

GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

-1_20130315_EMI

EC1804 SC10P50V2JN-L1-GP DY — CLK_PCI_KBC
EC1803 SC10P50V2JN-L1-GP DY — CLK_PCI_FB
EC1802 SC10P50V2JN-L1-GP DY — CLK_PCI_TPM
EC1801 SC33P50V2JN-3GP DY — CLK_PCI_LPC

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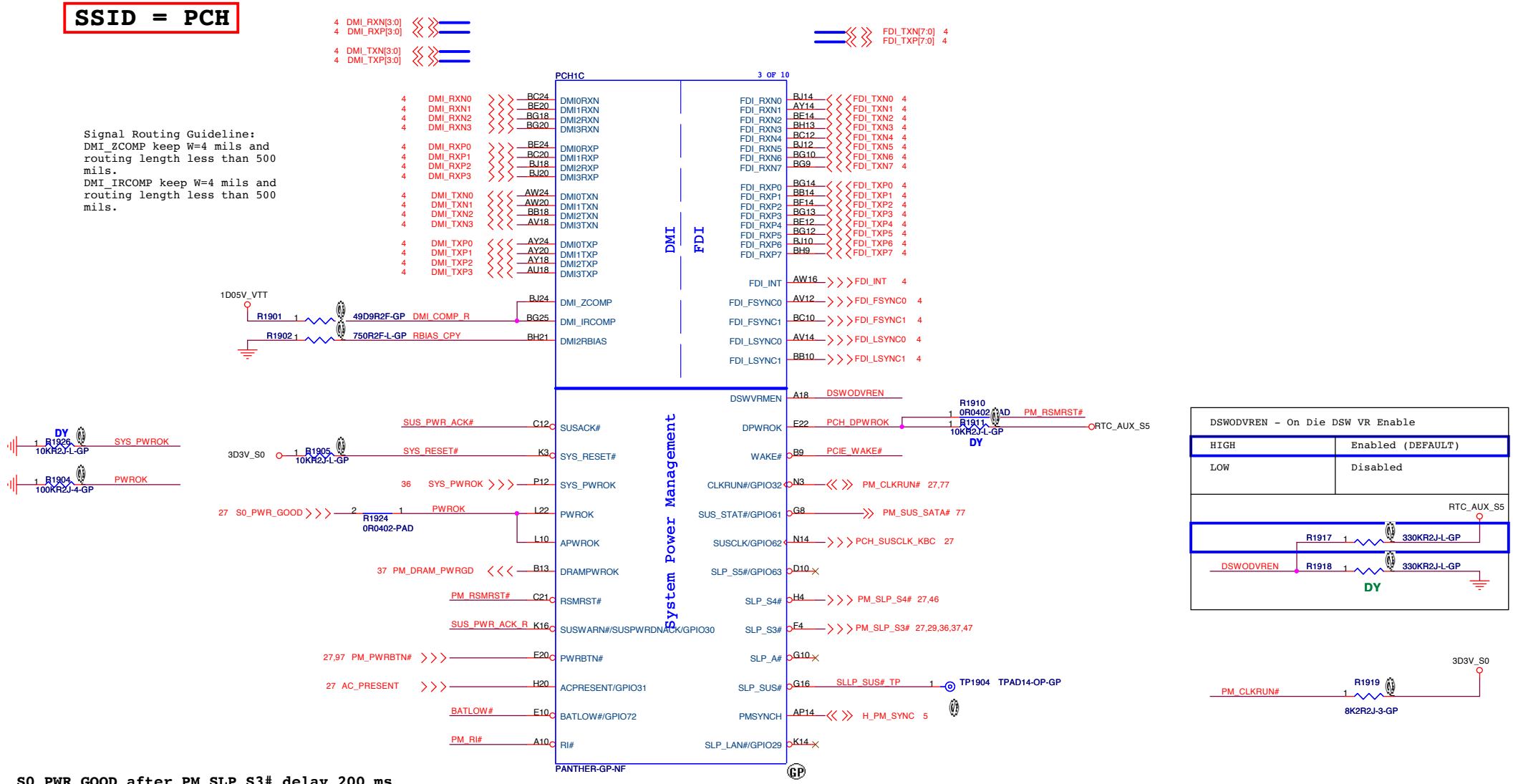
Title: PCH (PCI/USB/NVRAM)

Size: Custom | Document Number: EA40_CX | Rev: -3

Date: Friday, June 21, 2013 | Sheet 18 of 103

SSID = PCH

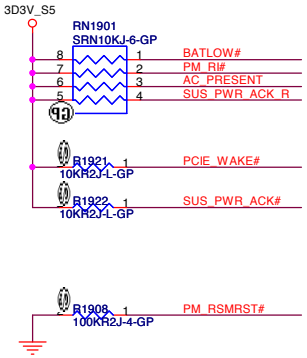
Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

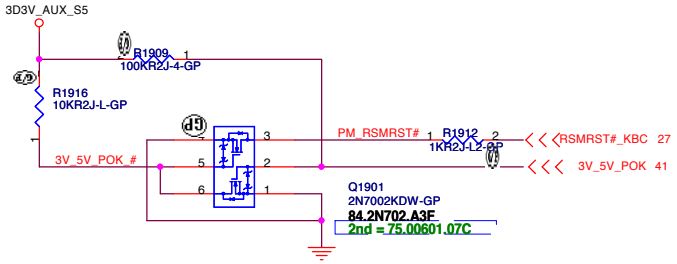


DSWODVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms





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Title: PCH (DM I/FDI/PM)

Size	Document Number	Rev
A3	EA40_CX	-3

Date: Friday, June 21, 2013 Sheet 19 of 103

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SSID = PCH

PCH1B

2 OF 10

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3 — LAN
PERN4 PERP4 PETN4 PETP4 — WLAN
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8

31 PCIE_RXN3 / 31 PCIE_RXP3 — C2011 SCD1U10V2KX-L1-GP — PCIE_TXN3_C / C2012 SCD1U10V2KX-L1-GP — PCIE_TXP3_C — 31 PCIE_TXN3 / 31 PCIE_TXP3
65 PCIE_RXN4 / 65 PCIE_RXP4 — C2005 SCD1U10V2KX-L1-GP — PCIE_TXN4_C / C2006 SCD1U10V2KX-L1-GP — PCIE_TXP4_C — 65 PCIE_TXN4 / 65 PCIE_TXP4

SMBALERT#/GPIO11 — E12 — EC_SWI# 27
SMBCLK — H14 — SMB_CLK
SMBDATA — C9 — SMB_DATA
SML0ALERT#/GPIO60 — A12 — DRAMRST_CNTRL_PCH 37
SML0CLK — C8 — SML0_CLK
SML0DATA — G12 — SML0_DATA
SML1ALERT#/PCHHOT#/GPIO74 — C13 — PCH_GPIO74
SML1CLK/GPIO58 — E14 — SML1_CLK 27,28,86
SML1DATA/GPIO75 — M16 — SML1_DATA 27,28,86

CL_CLK1 — M7
CL_DATA1 — T11
CL_RST1# — P10

3D3V_S0 — R2014 10KR2J-L-GP — PEG_A_CLKRQ#/GPIO47 — M10 — PEG_CLKREQ# 83

CLKOUT_PEG_A_N — AB37 — CLK_PCIE_VGA# 83
CLKOUT_PEG_A_P — AB38 — CLK_PCIE_VGA 83

CLKOUT_DMI_N — AV22 — CLK_EXP_N 5
CLKOUT_DMI_P — AU22 — CLK_EXP_P 5

CLKOUT_DP_N — AM12 — CLKOUT_DP_N_C — RN2017 SRN0J-6-GP — CLK_DP_N 5
CLKOUT_DP_P — AM13 — CLKOUT_DP_P_C — CLK_DP_P 5

CLKIN_DMI_N — BE18 — CLK_BUF_EXP_N
CLKIN_DMI_P — BE18 — CLK_BUF_EXP_P

CLKIN_GND1_N — BJ30 — CLK_BUF_CPYCLK_N — RN2008 SRN10KJ-L-GP
CLKIN_GND1_P — BG30 — CLK_BUF_CPYCLK_P

CLKIN_DOT_96N — G24 — CLK_BUF_DOT96_N
CLKIN_DOT_96P — F24 — CLK_BUF_DOT96_P

CLKIN_SATA_N — AK7 — CLK_BUF_CKSSCD_N
CLKIN_SATA_P — AK5 — CLK_BUF_CKSSCD_P

REFCLK14IN — K45 — CLK_BUF_REF14

CLKIN_PCILOOPBACK — H45 — CLK_PCI_FB 18

XTAL25_IN — V47 — XTAL25_IN
XTAL25_OUT — V49 — XTAL25_OUT

XCLK_RCOMP — Y47 — XCLK_RCOMP — R2007 90D9R2F-1-GP — 1D05V_VTT

CLKOUTFLEX0/GPIO64 — K43
CLKOUTFLEX1/GPIO65 — F47
CLKOUTFLEX2/GPIO66 — H47
CLKOUTFLEX3/GPIO67 — K49 — DGPU_PRSNT#

CLKOUT_PCIE0N / CLKOUT_PCIE0P — PCIE_CLK_REQ0# — J2 — PCIECLKRQ0#/GPIO73
CLKOUT_PCIE1N / CLKOUT_PCIE1P — PCIE_CLK_REQ1# — M1 — PCIECLKRQ1#/GPIO18
CLKOUT_PCIE2N / CLKOUT_PCIE2P — Lan: 31 PCIE_CLK_LAN# / 31 PCIE_CLK_LAN — 31 PCIE_CLK_LAN_REQ# — V10 — PCIECLKRQ2#/GPIO20
CLKOUT_PCIE3N / CLKOUT_PCIE3P — WLAN: 65 PCIE_CLK_WLAN# / 65 PCIE_CLK_WLAN — 65 CLK_PCIE_WLAN_REQ# — A8 — PCIECLKRQ3#/GPIO25
CLKOUT_PCIE4N / CLKOUT_PCIE4P — PCIE_CLK_REQ4# — L12 — PCIECLKRQ4#/GPIO26
CLKOUT_PCIE5N / CLKOUT_PCIE5P — PCIE_CLK_REQ5# — L14 — PCIECLKRQ5#/GPIO44
CLKOUT_PEG_B_N / CLKOUT_PEG_B_P — PEG_B_CLKRQ# — E6 — PEG_B_CLKRQ#/GPIO56
CLKOUT_PCIE6N / CLKOUT_PCIE6P — PCIE_CLK_REQ6# — T13 — PCIECLKRQ6#/GPIO45
CLKOUT_PCIE7N / CLKOUT_PCIE7P — PCIE_CLK_REQ7# — K12 — PCIECLKRQ7#/GPIO46
CLKOUT_ITPXDP_N / CLKOUT_ITPXDP_P

3D3V_S0 — RN2018 SRN10KJ-L-GP — PCIE_CLK_LAN_REQ# / PCIE_CLK_REQ1#

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

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3D3V_S5

SMB_CLK / SMB_DATA — RN2003 SRN2K2J-5-GP
SML0_DATA / SML0_CLK — RN2004 SRN2K2J-5-GP
SML1_CLK / SML1_DATA — RN2005 SRN2K2J-5-GP
PCH_GPIO74 / DRAMRST_CNTRL_PCH — RN2006 SRN10KJ-L-GP
R2009 1KR2J-L2-GP

3D3V_S0 — RN2007 SRN2K2J-5-GP

SMB_DATA — PCH_SMBDATA 14,15
Q2001 2N7002KDW-GP 84.2N702.A3F 2nd = 75.00601.07C
SMB_CLK — PCH_SMBCLK 14,15

X2001 25MHZ-18-GP
XTAL25_IN — R2006 1MR2J-L3-GP — XTAL25_OUT
C2008 SC12P50V2JN-3GP
C2007 SC15P50V2JN-L-GP
82.30020.G71
2nd = 82.30020.G61
-SB 20121113-2

3D3V_S0 — R2012 10KR2J-L-GP — DGPU_PRSNT# — UMA_DIS# 22
R2010 10KR2J-L-GP DY
R2013 10KR2J-L-GP UMA
R2011 10KR2J-L-GP Muxless
UMA_DIS#;DGPU_PRSNT#
UMA: 1 1
DIS :0 1
Muxless : 1 0
PX:0 0

3D3V_S5 — RN2001 SRN10KJ-6-GP
CLK_PCIE_WLAN_REQ#
PCIE_CLK_REQ6#
PCIE_CLK_REQ5#
PCIE_CLK_REQ4#

RN2002 SRN10KJ-6-GP
PCIE_CLK_REQ0#
PCIE_CLK_REQ7#
PEG_B_CLKRQ#
EC_SWI#

CLK_BUF_CKSSCD_P / CLK_BUF_CKSSCD_N / CLK_BUF_EXP_N / CLK_BUF_EXP_P — RN2010 SRN10KJ-6-GP
SA-20121023-1
Swap pin

CLK_BUF_DOT96_N / CLK_BUF_DOT96_P — RN2011 SRN10KJ-6-GP — SA-20121011

CLK_BUF_REF14 — R2015 10KR2J-L-GP

need very close to PCH

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Title: PCH (PCI-E/SMBUS/CLOCK/CL)
Size: Custom | Document Number: EA40_CX | Rev: -3
Date: Thursday, June 20, 2013 | Sheet 20 of 103

SSID = PCH

RTC_X1
RTC_X2
R2101 10MR2J-L-GP
X2101 XTAL-32D768KHZ-64-GP
82.30001.661
2nd = 82.30001.B21
C2101 SC6P50V2CN-1GP
C2102 SC6P50V2CN-1GP

RTC_AUX_S5
R2115 20KR2F-L-GP
R2116 20KR2F-L-GP
C2103 SC1U16V3KX-5GP
C2104 SC1U16V3KX-5GP
G2101 GAP-OPEN

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

RTC Reset

R2104 1MR2J-L3-GP
R2105 330KR2F-L-GP
SM_INTRUDER#
PCH_INTVRMEN

27 RTCRST_ON
RTC_RST#
RTC_RST# S
R2106 100KR2F-L3-GP
R2111 2KR2F-3-GP
Q2102 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031

29 HDA_CODEC_SYNC
29 HDA_CODEC_SDOUT
R2122 33R2J-L1-GP
R2123 33R2J-L1-GP
HDA_SYNC
HDA_SDOUT
DY

29 HDA_CODEC_RST#
29 HDA_CODEC_BITCLK
RN2102 SRN33J-5-GP-U
HDA_RST#
HDA_BITCLK

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

+3VS_+1.5VS_HDA_IO
R2102 1KR2J-L2-GP
HDA_SDOUT
DY

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

+3VS_+1.5VS_HDA_IO
R2103 1KR2J-L2-GP
HDA_SYNC

5V_S0
Q2101 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd =
HDA_CODEC_SYNC
HDA_SYNC_R
R2124 33R2J-L1-GP
HDA_SYNC

HDA_CODEC_BITCLK
EC2102 SC4D7P50V2CN-1GP DY
HDA_CODEC_SDOUT
EC2103 SC4D7P50V2CN-1GP DY
SPI_CS0#_R
EC2101 SC4D7P50V2CN-1GP DY

PCH1A 1 OF 10

RTC
RTC_X1 A20 RTCX1
RTC_X2 C20 RTCX2
RTC_RST# D20 RTCRST#
SRTC_RST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN

IHDA
HDA_BITCLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
29 HDA_SPKR T10 SPKR
HDA_RST# K34 HDA_RST#
29 HDA_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
27 ME_UNLOCK R2107 1KR2J-L2-GP HDA_SDOUT A36 HDA_SDO
C36 HDA_DOCK_EN#/GPIO33
N32 HDA_DOCK_RST#/GPIO13

JTAG
R2121 4K7R2J-L-GP PCH_JTAG_TCK_BUF J3 JTAG_TCK
H7 JTAG_TMS
K5 JTAG_TDI
H1 JTAG_TDO

SPI
27,60 SPI_CLK_R R2108 33R2J-L1-GP PCH_SPI_CLK T3 SPI_CLK
27,60 SPI_CS0#_R R2109 33R2J-L1-GP PCH_SPI_CS0# Y14 SPI_CS0#
T1 SPI_CS1#
27,60 SPI_SI_R R2110 33R2J-L1-GP PCH_SPI_SI V4 SPI_MOSI
27,60 SPI_SO_R U3 SPI_MISO

PANTHER-GP-NF

71.PANTH.00U

LPC
FWH0/LAD0 C38 LPC_AD0
FWH1/LAD1 A38 LPC_AD1
FWH2/LAD2 B37 LPC_AD2
FWH3/LAD3 C37 LPC_AD3
LPC_AD[0..3] 27,71,77
FWH4/LFRAME# D36 LPC_FRAME# 27,71,77
LDRQ0# E36
LDRQ1#/GPIO23 K36
SERIRQ V5 INT_SERIRQ 27,77

SATA 6G
SATA0RXN AM3 SATA_RXN0 56
SATA0RXP AM1 SATA_RXP0 56
SATA0TXN AP7 SATA_TXN0 56
SATA0TXP AP5 SATA_TXP0 56
HDD1
SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11
SATA1TXP AP10

SATA
SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7 SATA_RXN4 56
SATA4RXP Y5 SATA_RXP4 56
SATA4TXN AD3 SATA_TXN4 56
SATA4TXP AD1 SATA_TXP4 56
ODD
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATAICOMPO Y11
SATAICOMPI Y10 SATA_COMP R2112 37D4R2F-GP 1D05V_VTT
SATA3RCOMPO AB12
SATA3COMPI AB13 SATA3_COMP R2113 49D9R2F-GP 1D05V_VTT
SATA3RBIAS AH1 RBIAS_SATA3 R2114 750R2F-L-GP
SATALED# P3 SATA_LED# 68
SATA0GP/GPIO21 V14 SATA_DET#0
SATA1GP/GPIO19 P1

3D3V_S0
RN2103 SRN10KJ-6-GP
22 PSW_CLR#
SATA_LED#
INT_SERIRQ
SATA_DET#0

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

UMA C

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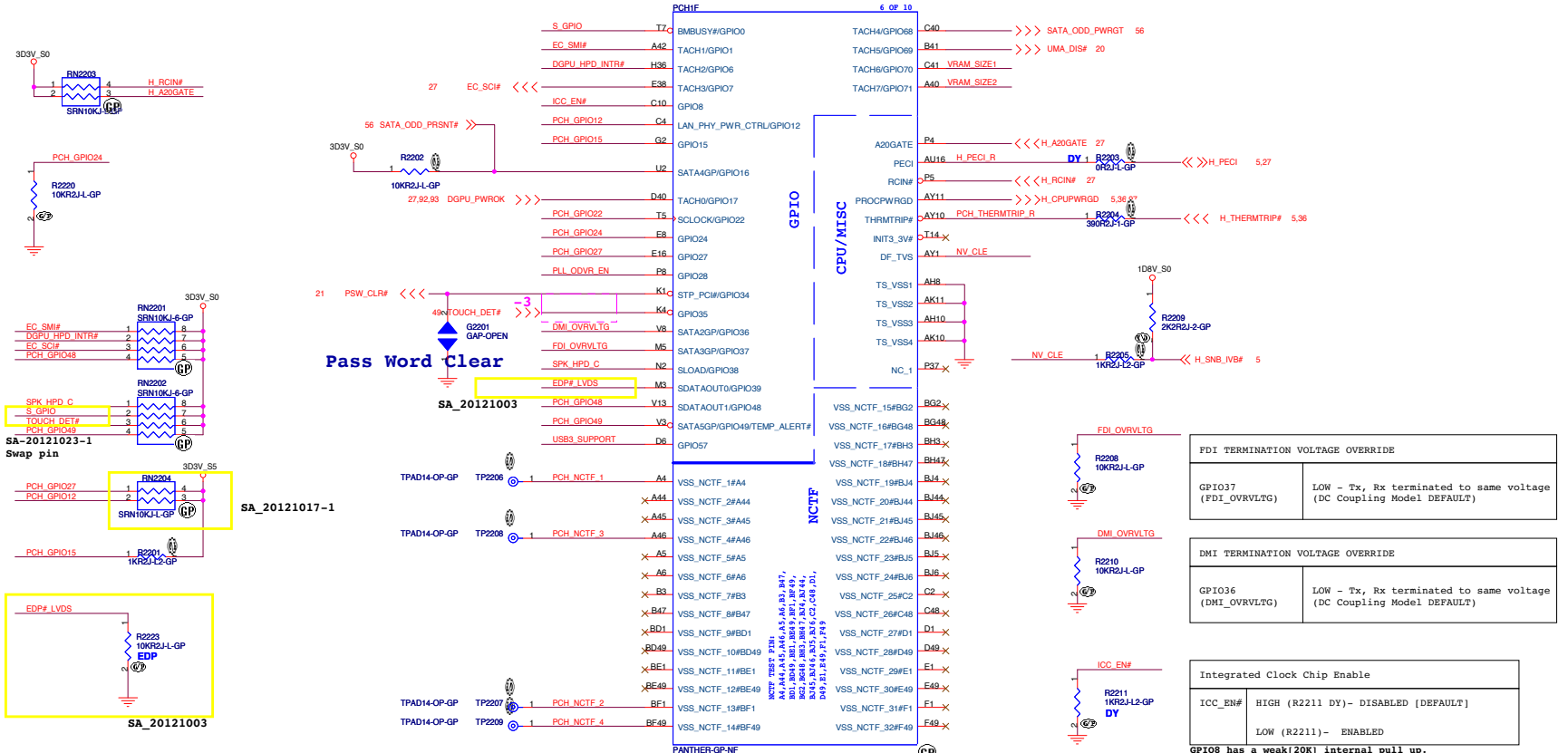
Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: Custom | Document Number: EA40_CX | Rev: -3
Date: Thursday, June 20, 2013 | Sheet 21 of 103

SSID = PCH



FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

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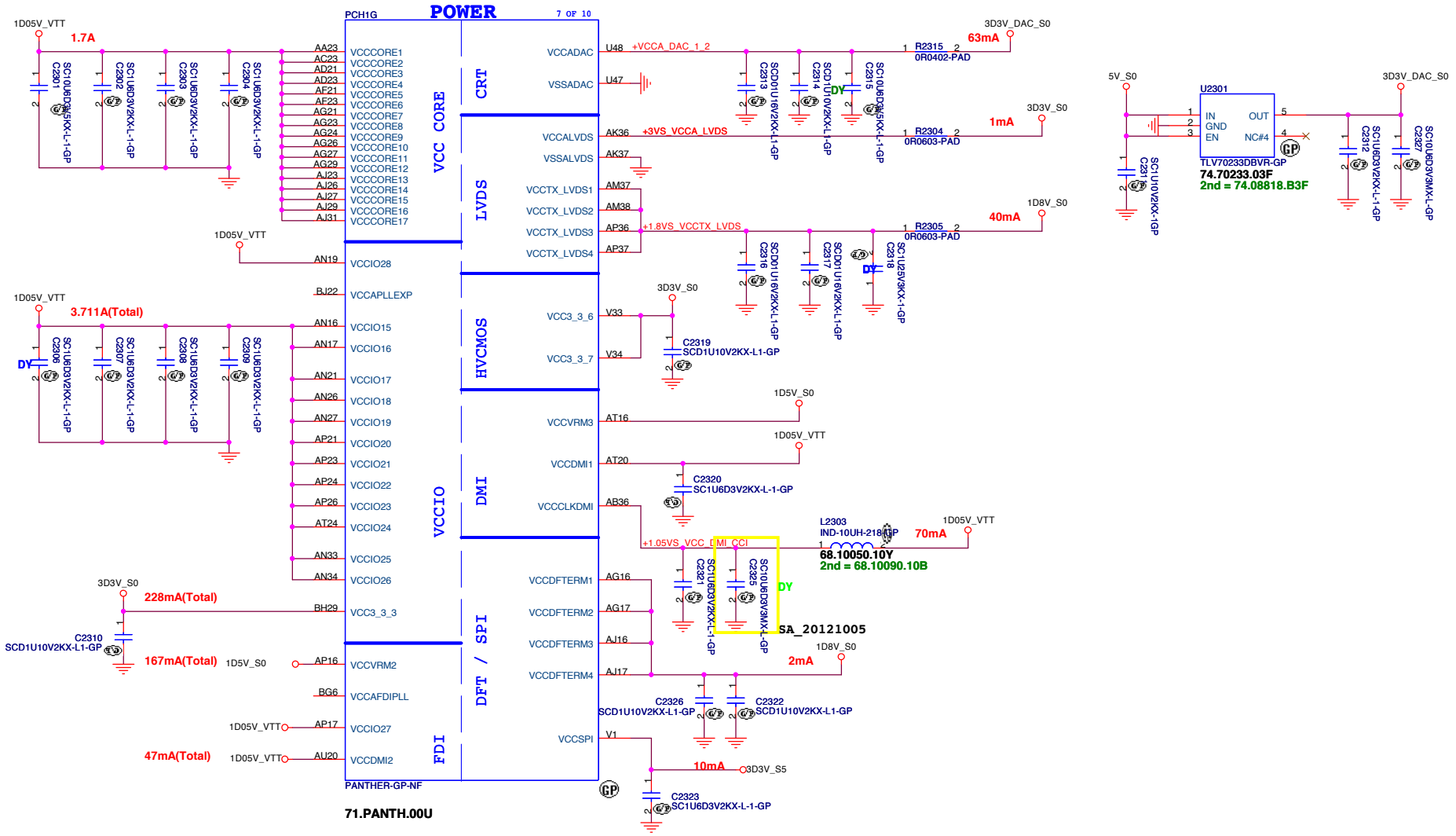
Title: PCH (GPIO/CPU)

Size: Custom | Document Number: EA40 CX | Rev: -3

Date: Thursday, June 20, 2013 | Sheet 22 of 103

SSID = PCH



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Title: PCH (POWER1)

Size: A3 | Document Number: EA40_CX | Rev: -3

Date: Friday, June 21, 2013 | Sheet 23 of 103

SSID = PCH

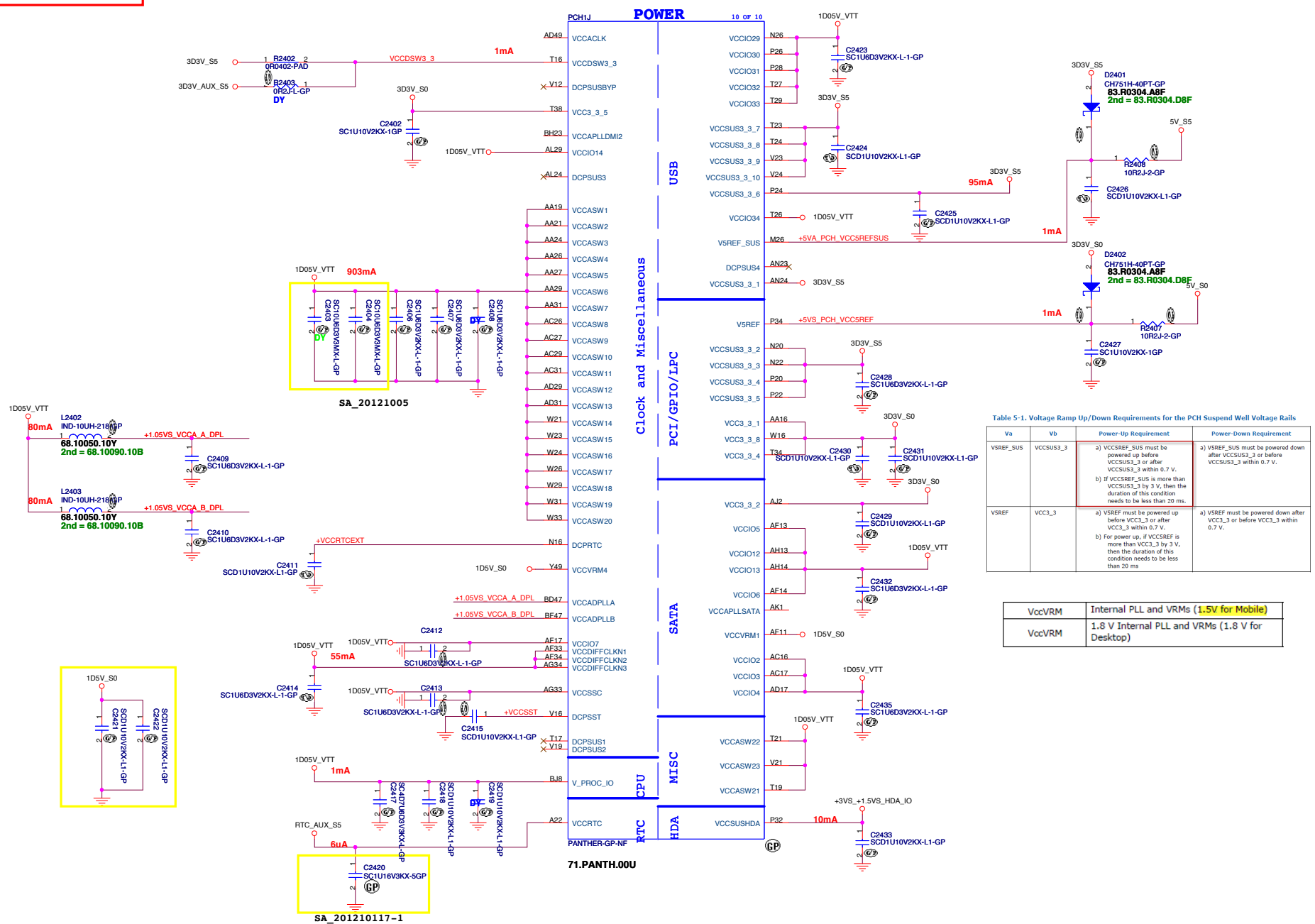

Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
VSREF_SUS	VCCSUS3_3	a) VCC5REF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V. b) If VCC5REF_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) VSREF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
VSREF	VCC3_3	a) VSREF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCC5REF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms	a) VSREF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)

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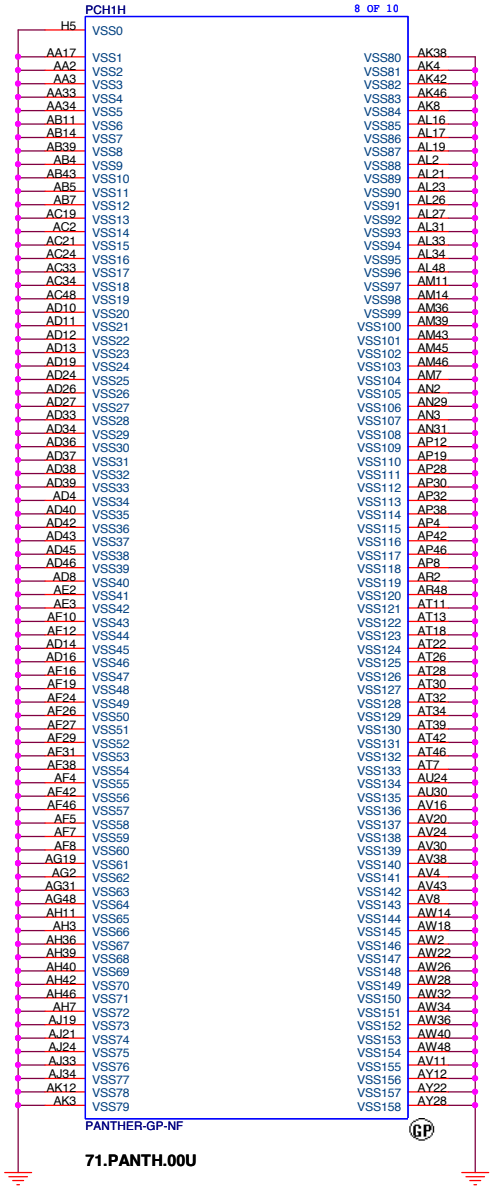
Title: PCH (POWER2)

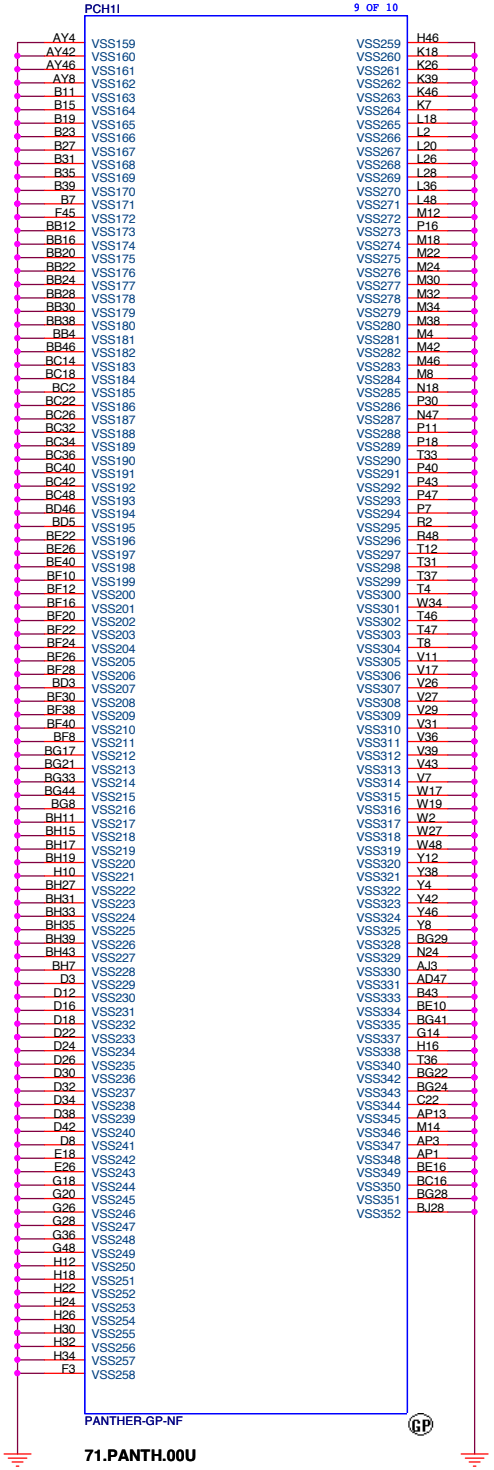
Size: Custom | Document Number: EA40_CX | Rev: -3

Date: Friday, June 21, 2013 | Sheet 24 of 103

SSID = PCH



71.PANTH.00U



71.PANTH.00U

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Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	EA40_CX	-3

Date: Thursday, June 06, 2013 Sheet 25 of 103

UMA C

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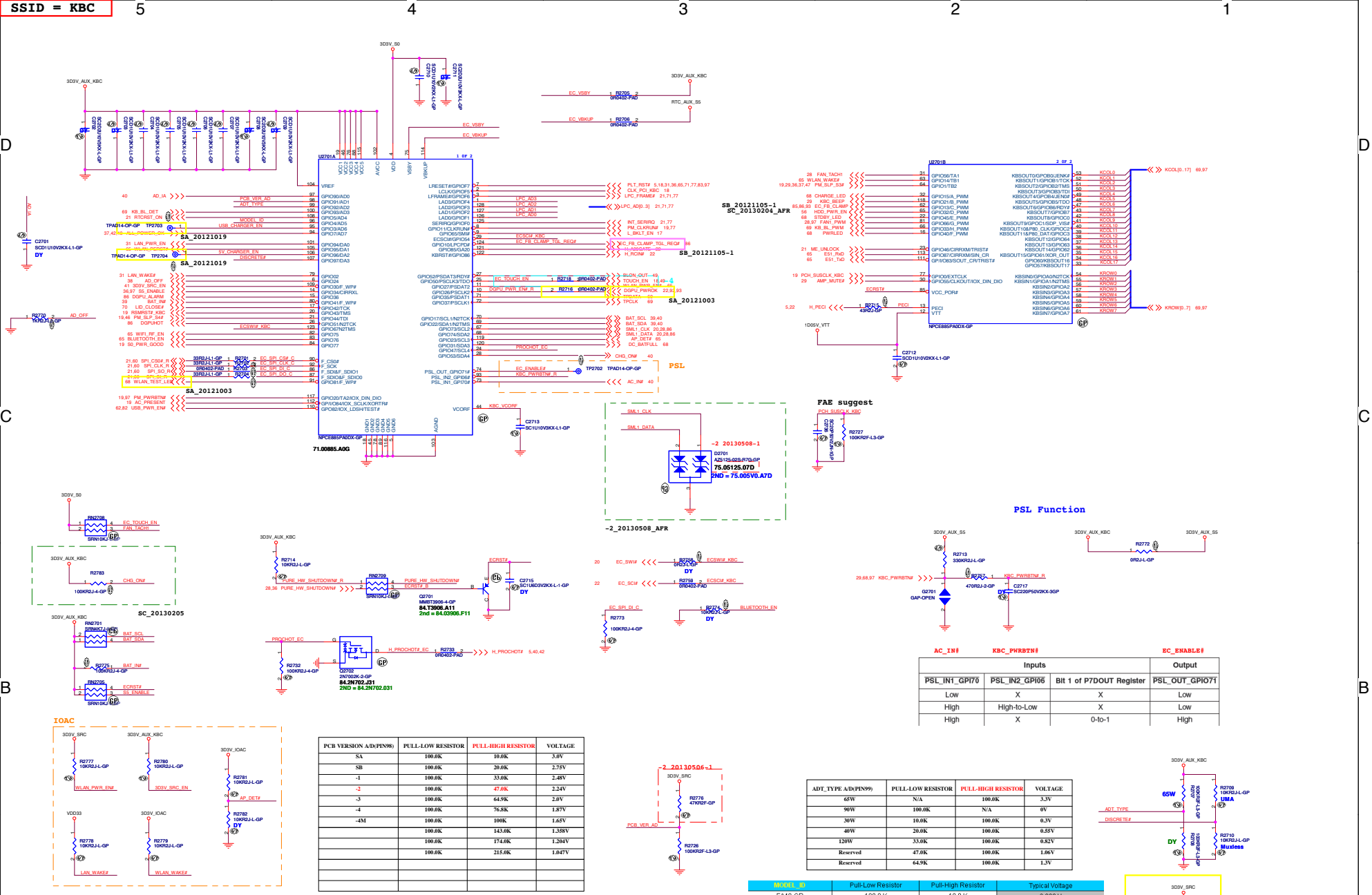
Title

Clock(colay)

Size	Document Number	Rev
A4	**EA40_CX**	-3

Date: Thursday, June 06, 2013 Sheet 26 of 103

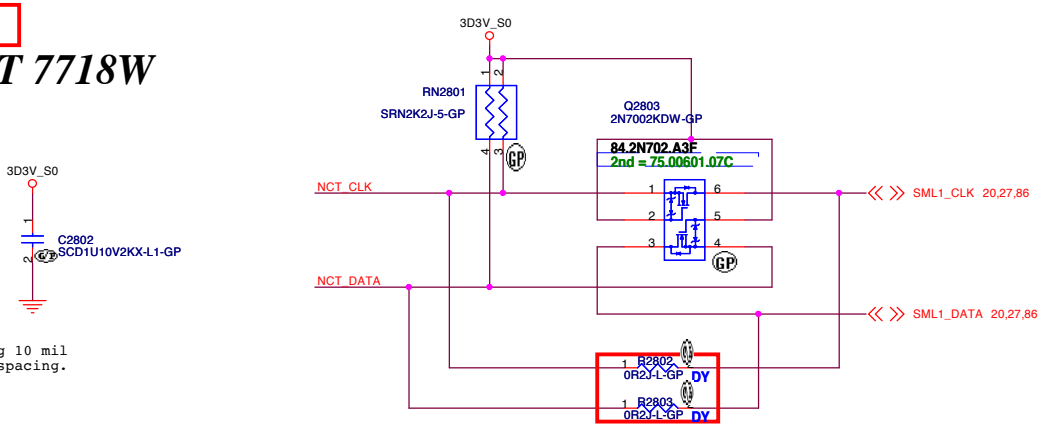
SSID = KBC



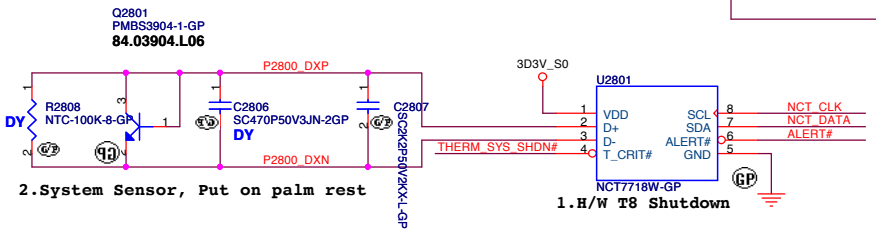
UMA C	
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	KBC NPCE885
Size / Custom	Document Number: EA40 CX
	Rev: -3
Date: Thursday, June 20, 2013	Sheet 27 of 163

SSID = Thermal

Thermal sensor NCT 7718W



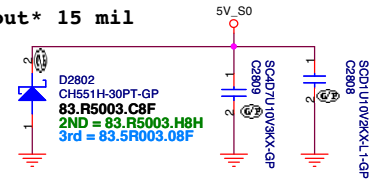
Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

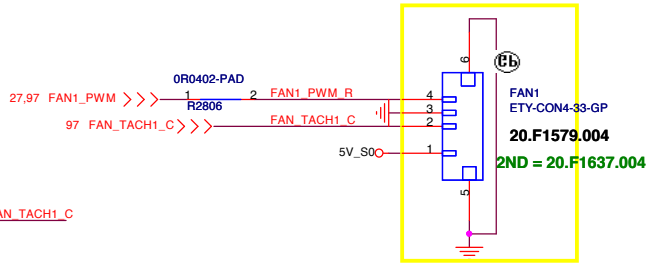


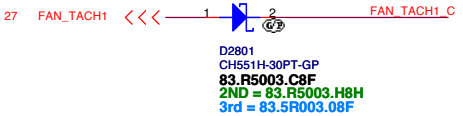
2.System Sensor, Put on palm rest

1.H/W T8 Shutdown

Layout 15 mil





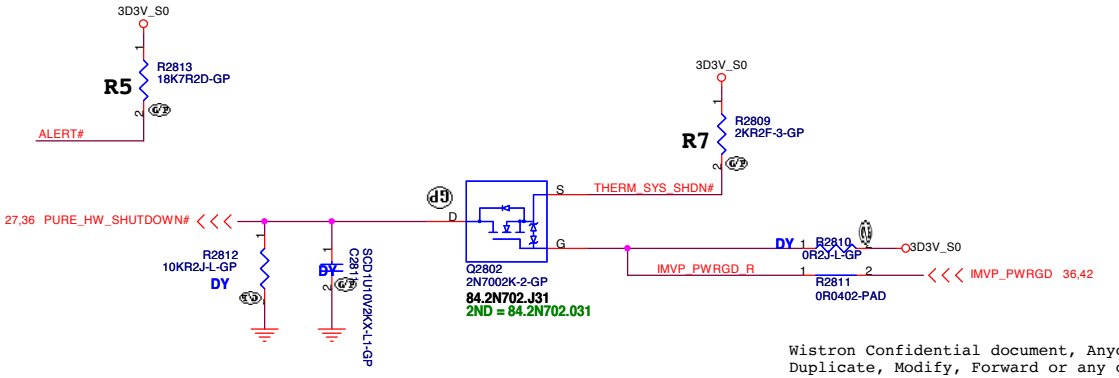


ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

SB T8=85 degree



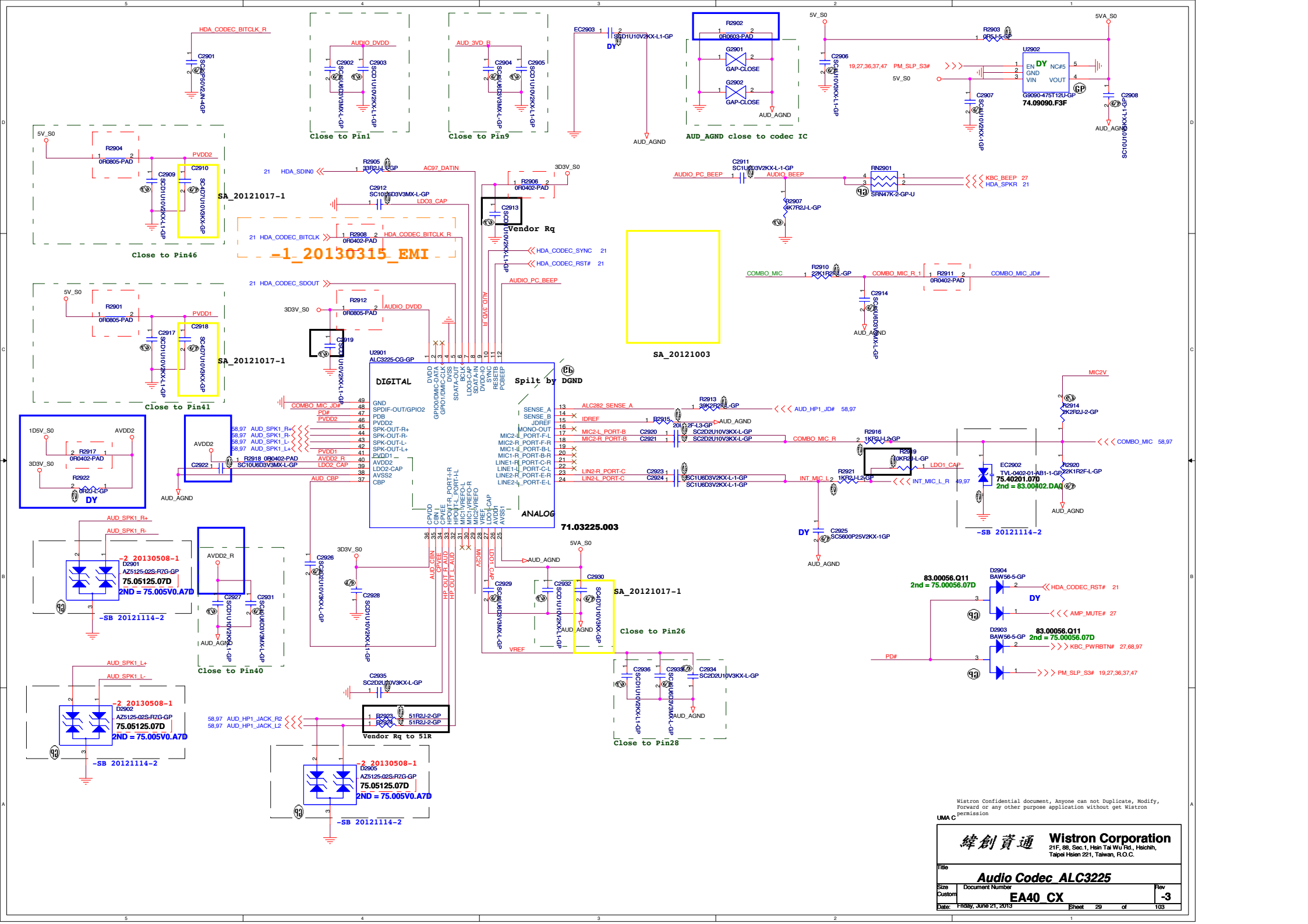
UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal NCT7718

Size: Custom | Document Number: EA40 CX | Rev: -3

Date: Thursday, June 20, 2013 | Sheet 28 of 103



UMA C

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**Audio Codec_ALC3225**
Size: Custom	Document Number: **EA40_CX** Rev: **-3**
Date: Friday, June 21, 2013	Sheet 29 of 103

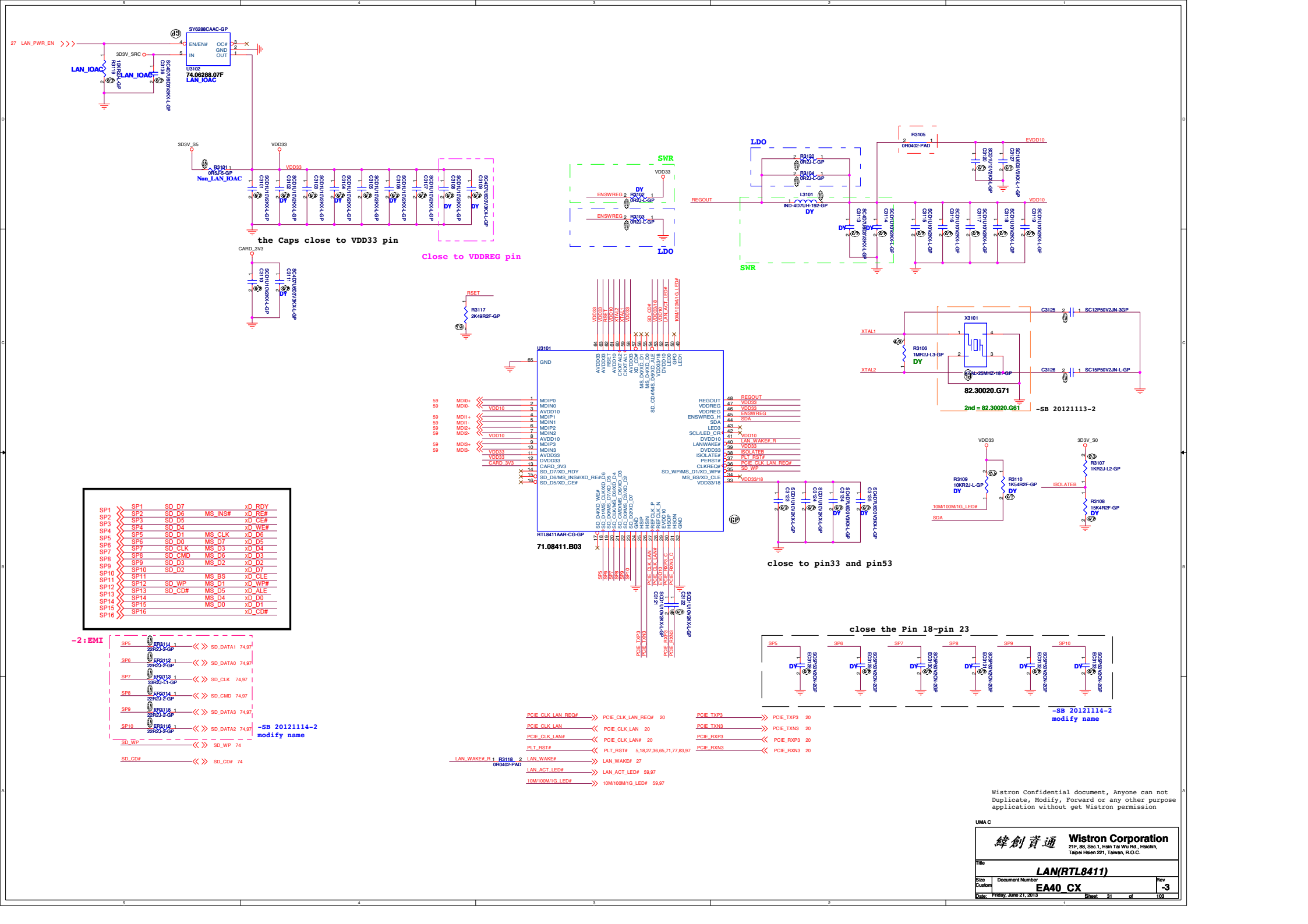
UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio AMP***

Size	Document Number	Rev
A3	EA40_CX	-3

Date: Thursday, June 06, 2013 Sheet 30 of 103


LAN_IOAC
SY6288CAAC-GP
U3102
74.06288.07F
LAN_IOAC
3D3V_S5
VDD33
Non_LAN_IOAC
the Caps close to VDD33 pin
CARD_3V3
Close to VDDREG pin
SWR
LDO
REGOUT
EVDD10
VDD10
RTL8411AAR-CG-GP
71.08411.B03
close to pin33 and pin53
X3101
82.30020.G71
2nd = 82.30020.G61
-SB 20121113-2
close the Pin 18~pin 23
-SB 20121114-2
modify name
-2:EMI
-SB 20121114-2
modify name
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LAN(RTL8411)
EA40_CX
-3
Friday, June 21, 2013
31
103

UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5159 (CARD READER)***

Size	Document Number	Rev
Custom	**EA40_CX**	**-3**
Date: Thursday, June 06, 2013	Sheet 32 of 103	

(Blanking)

UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	EA40_CX	-3

Date: Thursday, June 06, 2013 Sheet 33 of 103

(Blanking)

UMA C

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	EA40_CX	-3

Date: Thursday, June 06, 2013 Sheet 34 of 103

UMA C

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

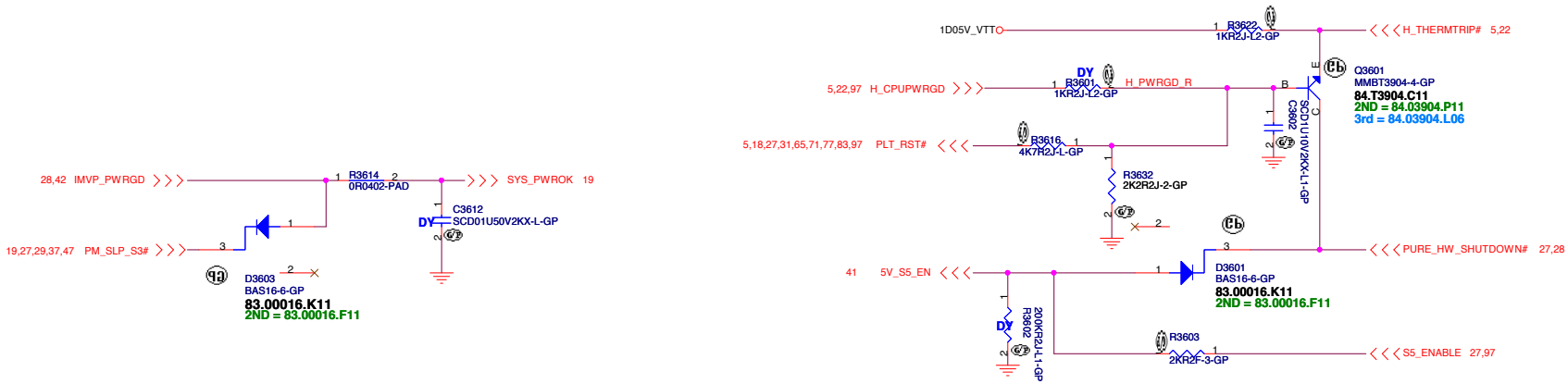
Title

USB 3.0 Controller

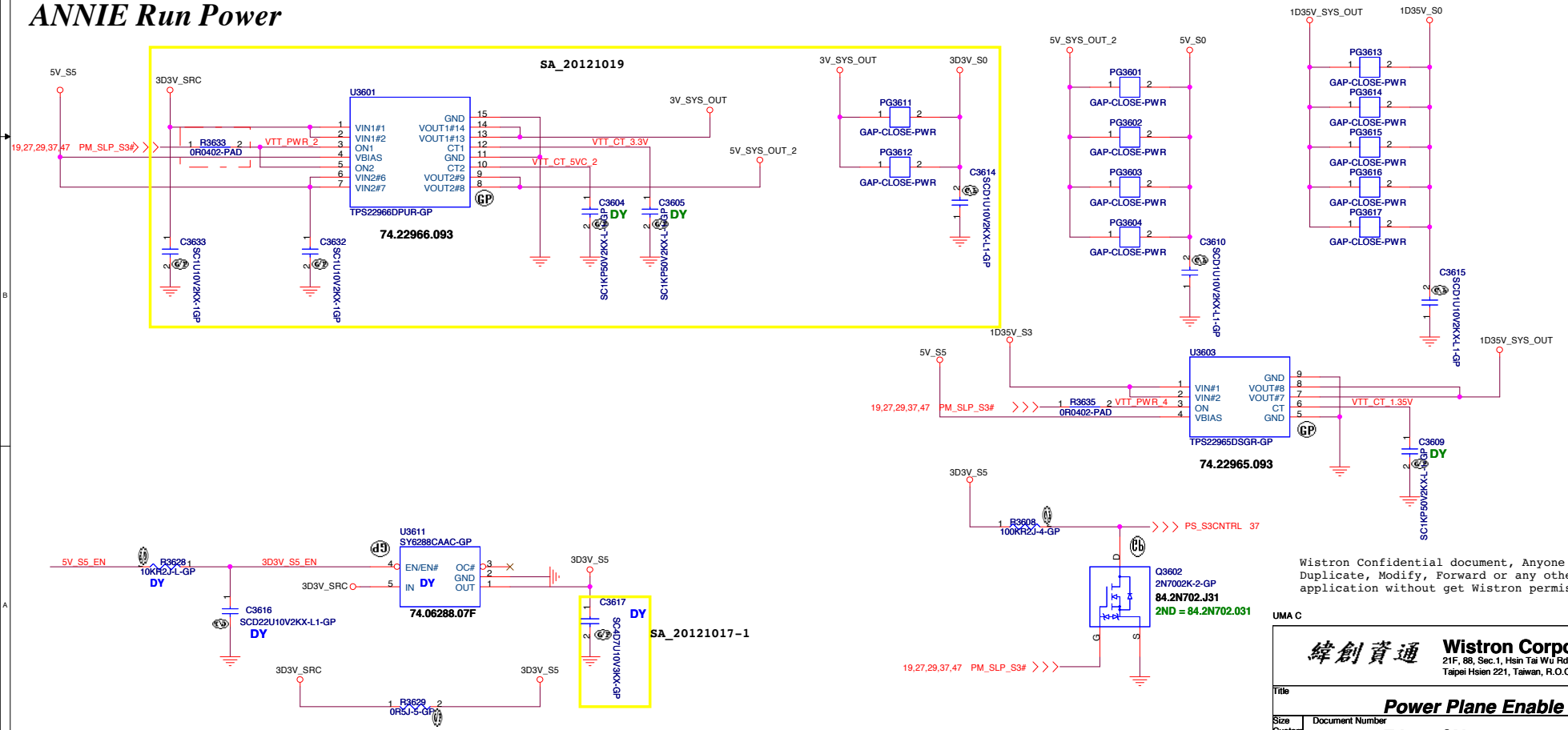
Size	Document Number	Rev
Custom	**EA40_CX**	**-3**

Date: Thursday, June 06, 2013 Sheet 35 of 103

Power Sequence



ANNIE Run Power



UMA C

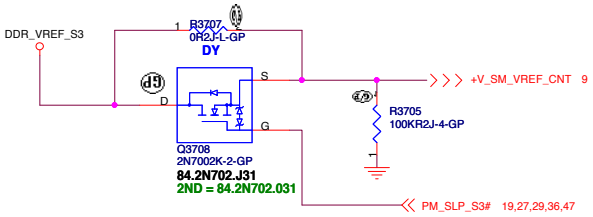
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

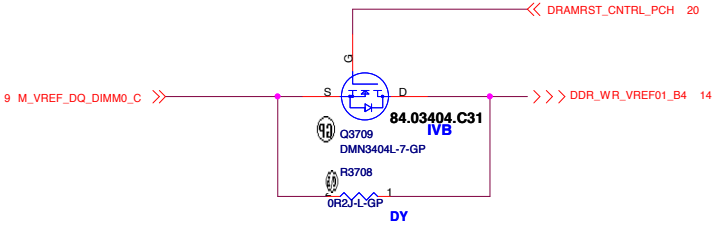
Title: **Power Plane Enable**

Size	Document Number	Rev
Custom	EA40_CX	-3

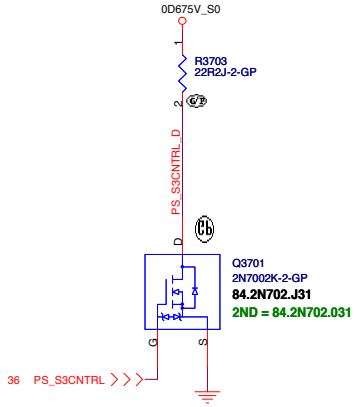
Date: Thursday, June 20, 2013 Sheet 36 of 103

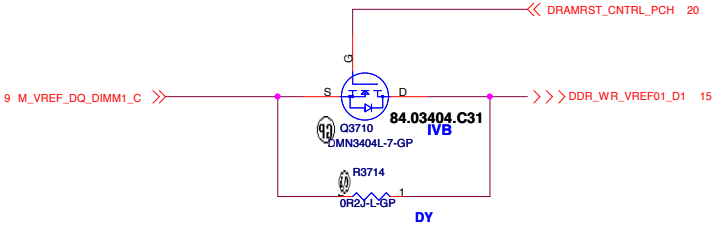
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation





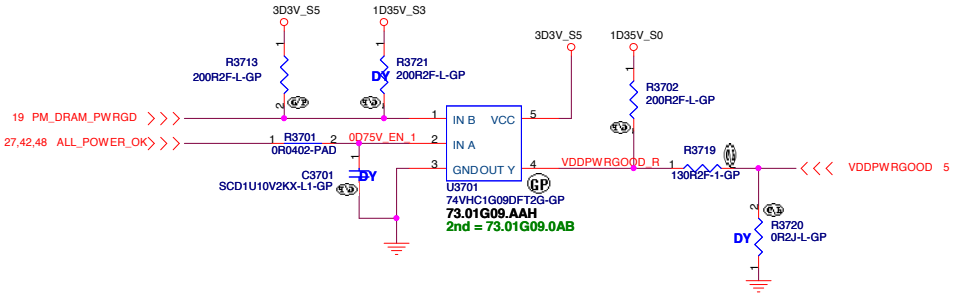
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



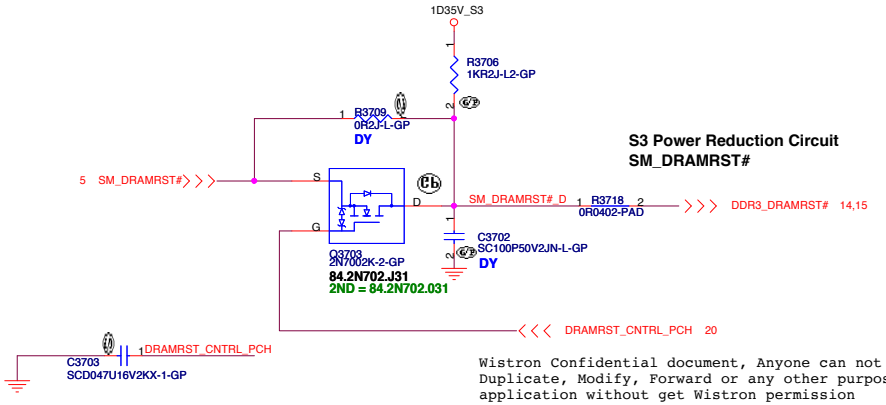


SA_20121024-3

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



S3 Power Reduction Circuit
SM_DRAMRST#

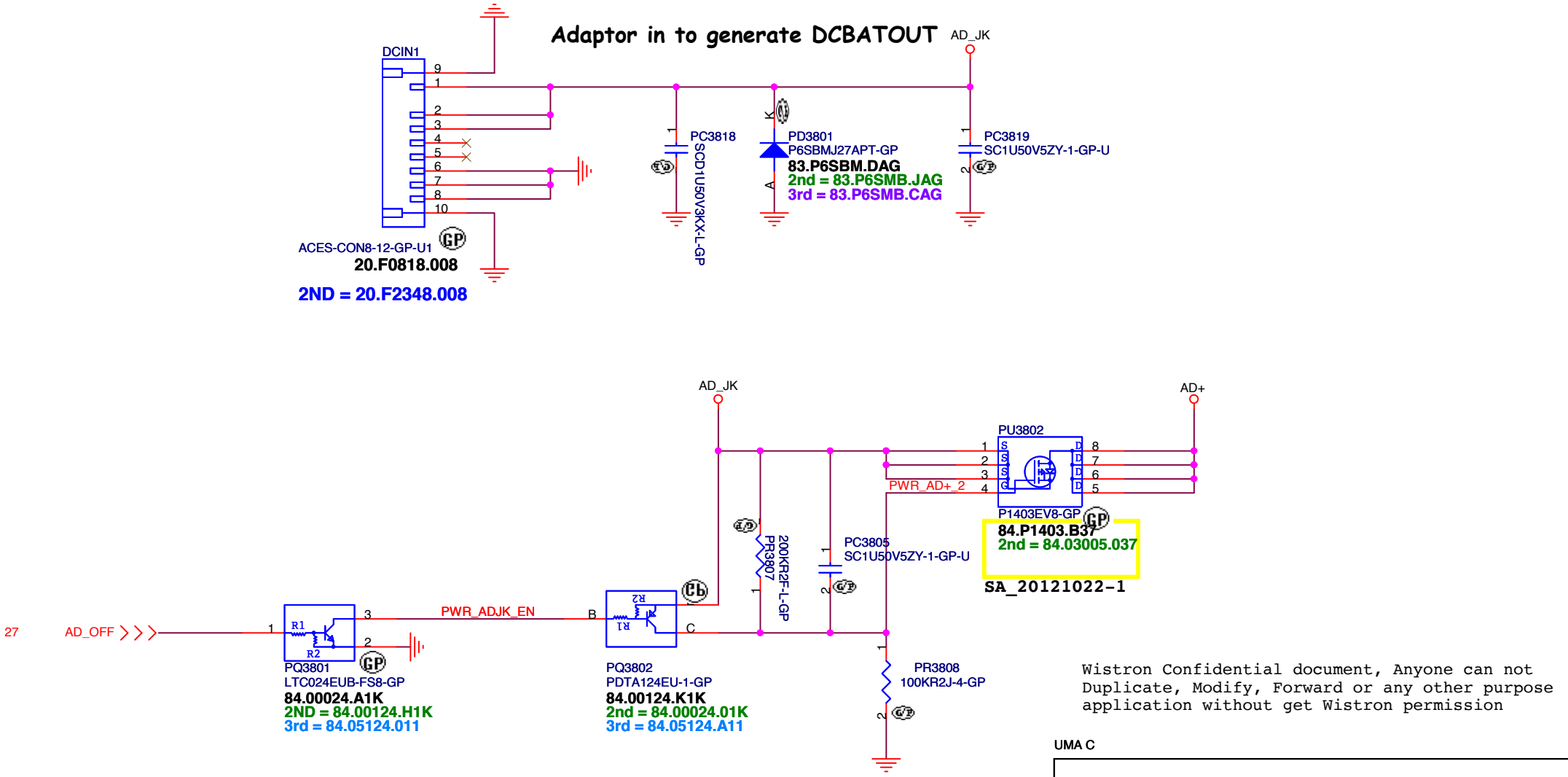
UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

Size: Custom | Document Number: EA40_CX | Rev: -3

Date: Thursday, June 20, 2013 | Sheet 37 of 103



UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN JACK**

Size	Document Number	Rev
A4	EA40 CX	-3

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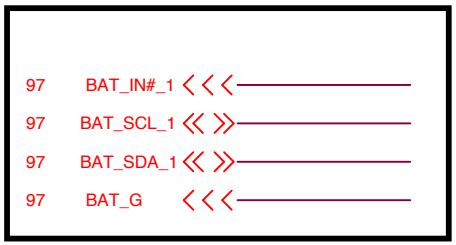
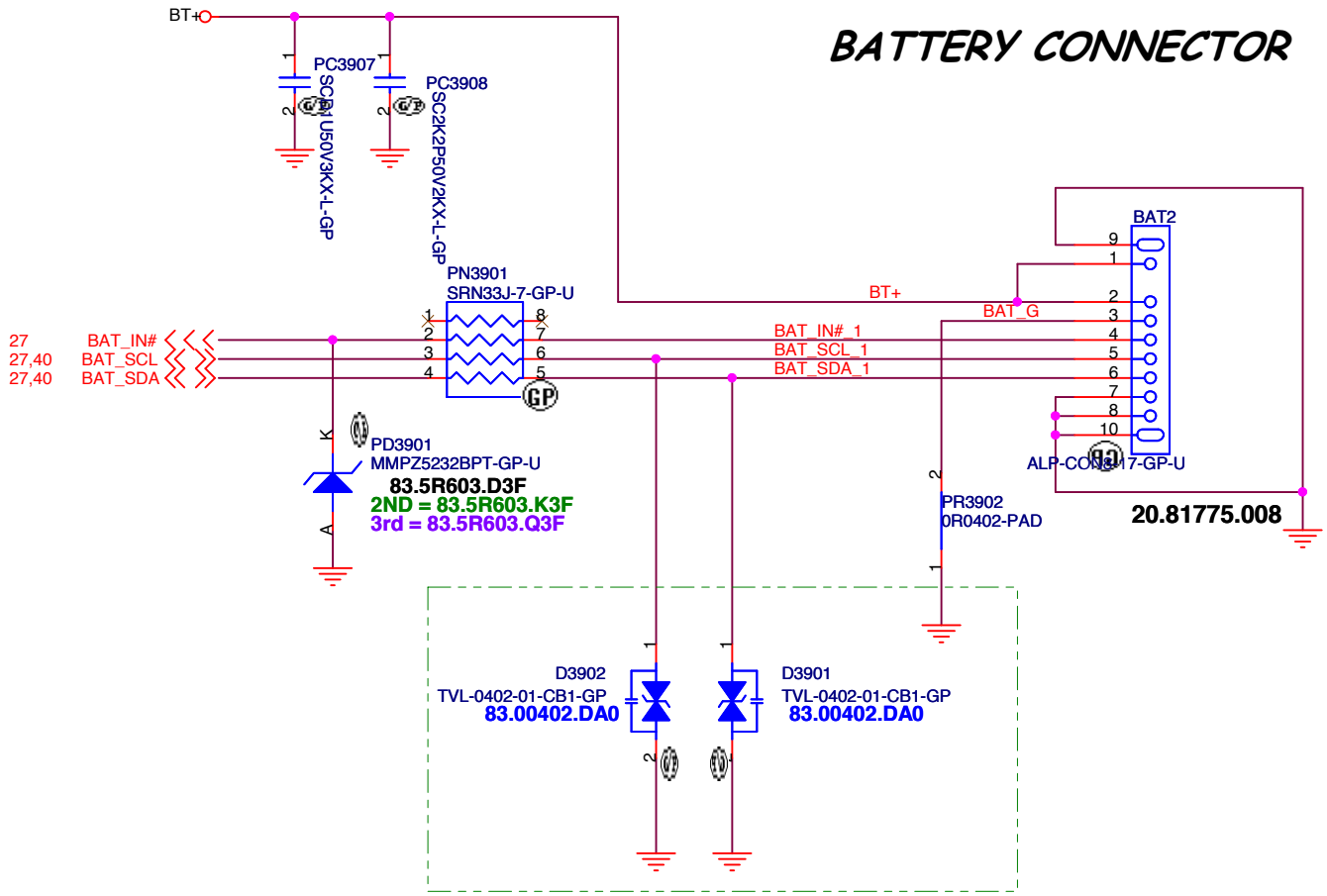
BATTERY CONNECTOR





SC_20130205_AFR

UMA C

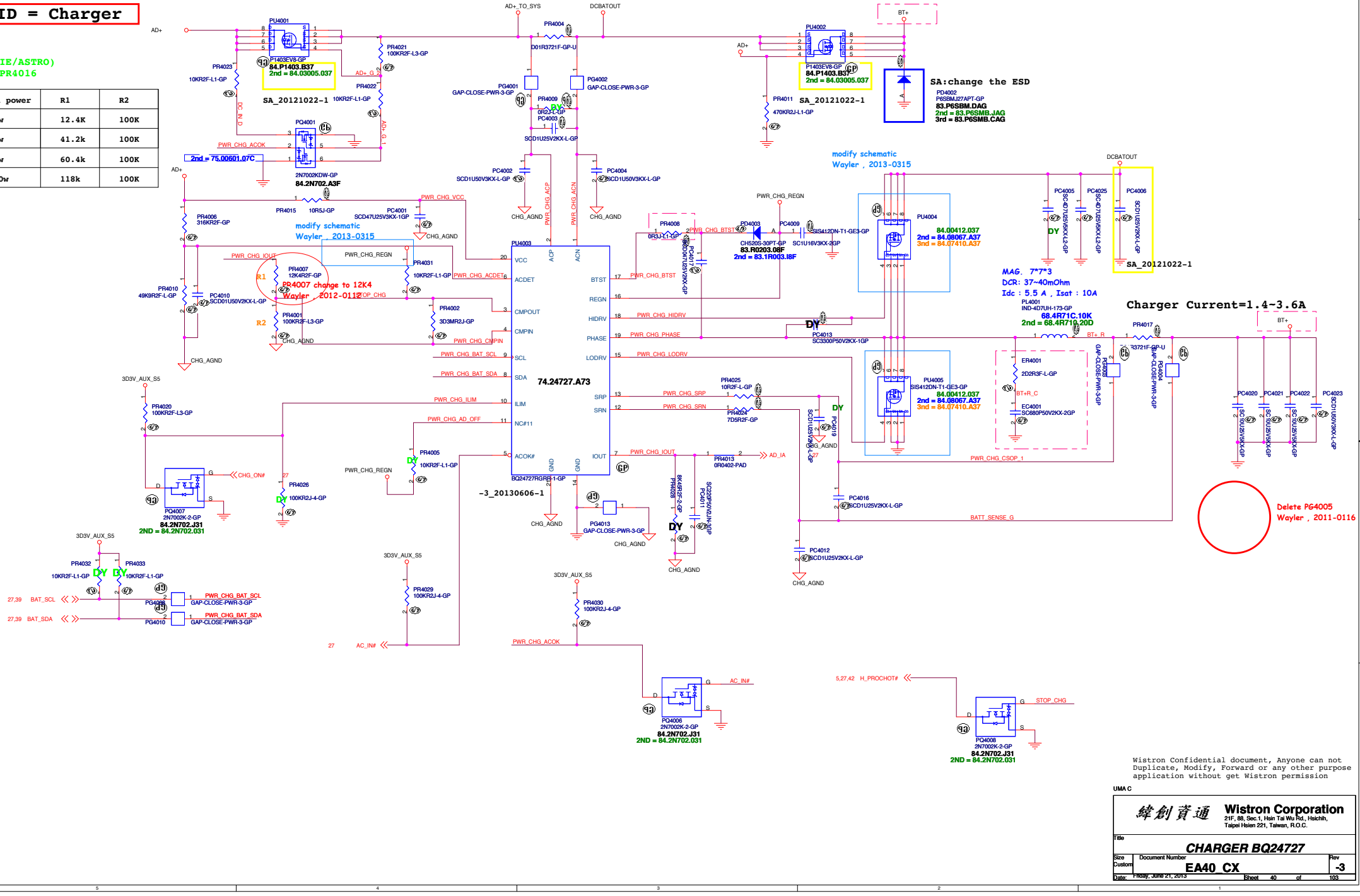
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BATT CONN		
Size A4	Document Number EA40 CX	Rev -3
Date: Thursday, June 20, 2013	Sheet 39 of 103	

SSID = Charger

A8(ANNIE/ASTRO)
PR4014,PR4016

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K



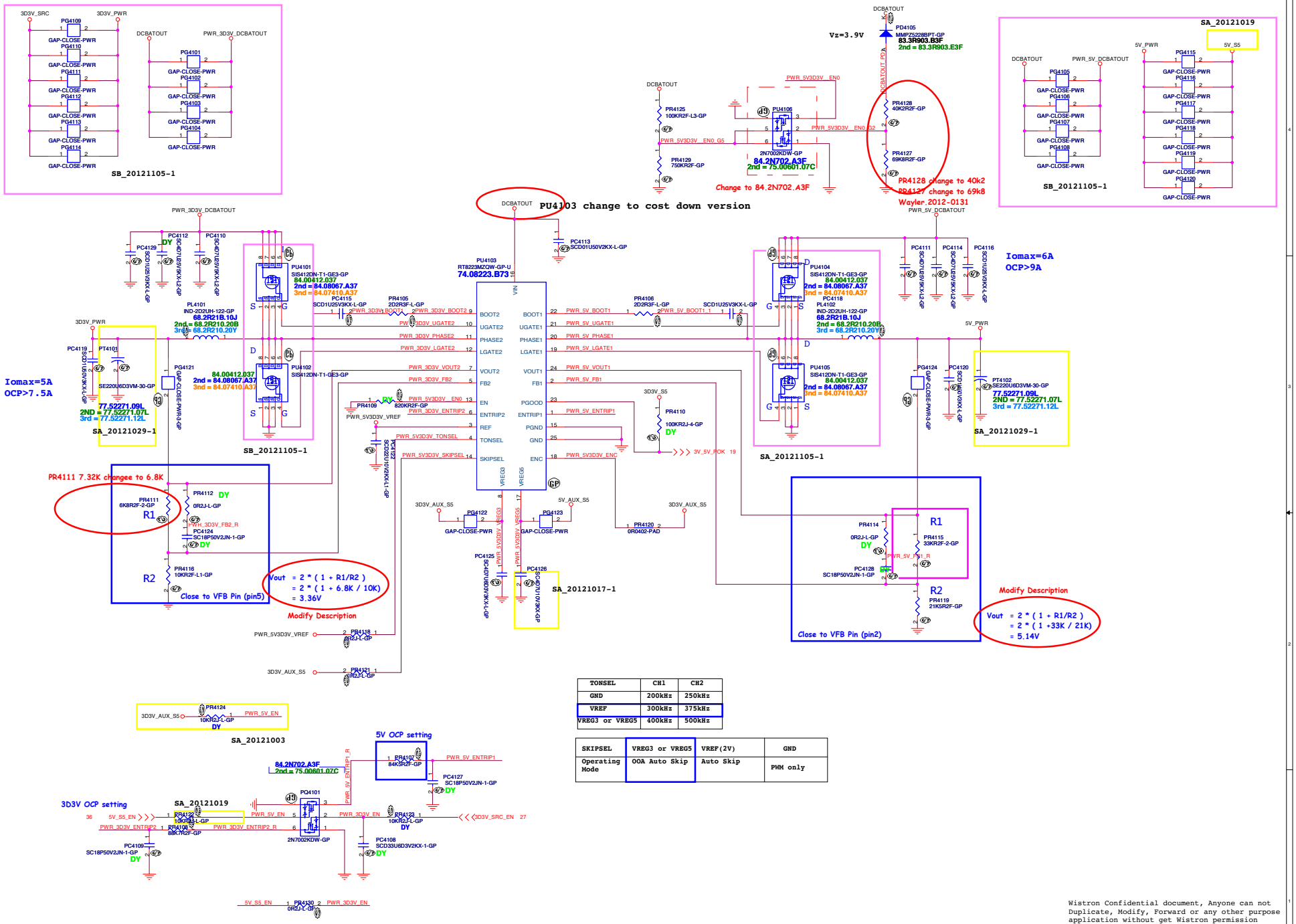
UMA C

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24727

Size: Custom | Document Number: EA40_CX | Rev: -3

Date: Friday, June 21, 2013 | Sheet 40 of 103



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

UMA C

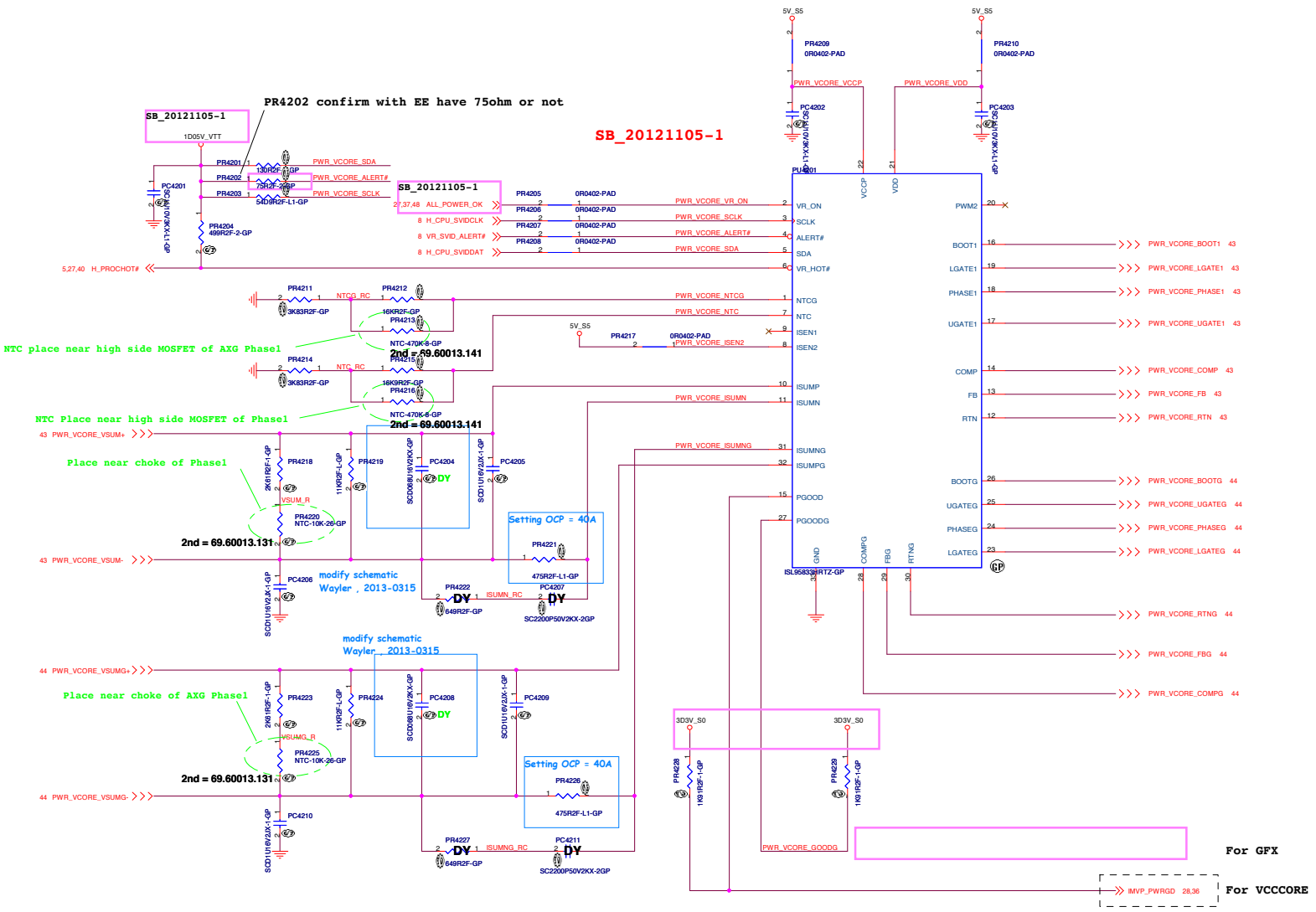
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V/3D3V(RT8223M)

Size: Custom | Document Number: EA40_CX | Rev: -3

Date: Friday, June 21, 2013 | Sheet 41 of 103

SSID = CPU.Regulator



UMA C

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95833_CPU_CORE(1/3)

Size: Custom | Document Number: EA40_CX | Rev: -3

Date: Friday, June 21, 2013 | Sheet 42 of 103

SB_20121105-1

BOM control

	Main source	2nd source
PU4301	84.03664.037 (FDMS3664S) Mount	
PU4302	84.03664.037 (FDMS3664S) DY	

BOM control

PU4301 FDMS3600-02-RJK0215-COLAY-GP
1st = 84.03664.037
2nd = 84.08107.B37
3rd = 84.00920.037

PU4303 DY FDMS3600-02-RJK0215-COLAY-GP
1st = 84.03664.037
2nd = 84.08107.B37
3rd = 84.00920.037

PWR_VCCCORE1_DCBATOUT
PC4302 SC10U25V5KX-GP
PC4303 SC10U25V5KX-GP
PC4304 SC10U25V5KX-GP
PC4305 SC10U25V5KX-GP

SA_20121019
DCBATOUT
PWR_VCCCORE1_DCBATOUT
PG4301 GAP-CLOSE-PWR
PG4304 GAP-CLOSE-PWR
PG4307 GAP-CLOSE-PWR
PG4308 GAP-CLOSE-PWR
PG4309 GAP-CLOSE-PWR
PG4310 GAP-CLOSE-PWR

42 PWR_VCORE_BOOT1
PR4301 2D2R3F-L-GP
BOOT1_RC
PC4301 SCD22U50V3ZY-1GP
42 PWR_VCORE_UGATE1
42 PWR_VCORE_PHASE1
42 PWR_VCORE_LGATE1

Pana . 10 x 10 x 4
DCR 1.1 mOhm
Isat : 24A

VCC_CORE
PL4301 L-D36UH-1-GP
68.R3610.20A
2nd = 68.R3610.20C

PG4319 GAP-CLOSE-PWR-3-GP
PG4323 GAP-CLOSE-PWR-3-GP

PT4305 SE560U2D5VM-3-GP
PT4304 SE560U2D5VM-3-GP
77.55671.01L 77.55671.01L
-3_20130621

SC_20130206

SA_20121019
PWR_VCCCORE1_DCBATOUT
DCBATOUT
PG4311 GAP-CLOSE-PWR
PG4312 GAP-CLOSE-PWR
PG4313 GAP-CLOSE-PWR
PG4314 GAP-CLOSE-PWR
PG4315 GAP-CLOSE-PWR
PG4316 GAP-CLOSE-PWR
PG4320 GAP-CLOSE-PWR
PG4321 GAP-CLOSE-PWR

42 PWR_VCORE_VSUM+
PR4302 3K65R2F-1-GP
PWR_VCORE_VSUM+_GAP
42 PWR_VCORE_VSUM-
PR4303 1R2F-GP
PWR_VCORE_VSUM-_GAP
Parallel

42 PWR_VCORE_COMP
PR4304 42K2R2F-L-GP
42 PWR_VCORE_FB

PR4305 499R2F-2-GP
PC4306 SC470P50V-2-GP
FB_RC
PC4307 SC47P50V2JN-3GP
PR4306 1K91R2F-1-GP
PR4307 267KR2F-GP
COMP_RC
PC4308 SC150P50V2JN-3GP
PR4308 2KR2F-3-GP
COMP_R
PC4309 SC680P50V2KX-2GP
modify schematic
Wayler , 2013-0315
Setting LL = 2.9m

PC4310 SC330P50V2JC-2-GP DY
PC4311 SCD01U50V2KX-L-GP
R4301 0R0402-PAD
42 PWR_VCORE_RTN

VCCSENSE 8
VSSSENSE 8
Parallel

UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95833_CPU_CORE(2/3)
Size: Custom
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Date: Friday, June 21, 2013
Sheet 43 of 103

SB_20121105-1

BOM control

	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S) Mount	
PU4402	84.03664.037 (FDMS3664S) DY	

BOM control

PU4402 FDMS3600-02-RJK0215-COLAY-GP
1st = 84.03664.037
2nd = 84.08107.B37
3rd = 84.00920.037

PWR_GFXCORE1_DCBATOUT
PC4402 SC10U25V5KX-GP
PC4403 SC10U25V5KX-GP
PC4404 SC10U25V5KX-GP
PC4405 SC10U25V5KX-GP

Iccmax=33A
IccTDC=22A
OCP>40A

Pana . 10 x 10 x 4
DCR 1.1 mOhm
Isat : 24A

42 PWR_VCORE_BOOTG
PR4309 2D2R3F-L-GP
BOOTG_RC
PC4401 SCD22U50V3ZY-1GP
42 PWR_VCORE_UGATEG
42 PWR_VCORE_PHASEG
42 PWR_VCORE_LGATEG

PL4401 L-D36UH-1-GP
68.R3610.20A
2nd = 68.R3610.20C

VCC_GFXCORE

PG4409 GAP-CLOSE-PWR-3-GP
PG4410 GAP-CLOSE-PWR-3-GP

PT4401 SE560U2D5VM-3-GP
PT4402 SE560U2D5VM-3-GP
77.55671.01L
77.55671.01L

-3_20130621

DCBATOUT
PT4403 SE68U25M4-GP
DY
79.68612.3BL

SA_20121004

DCBATOUT
PWR_GFXCORE1_DCBATOUT
PG4401 GAP-CLOSE-PWR
PG4404 GAP-CLOSE-PWR
PG4405 GAP-CLOSE-PWR
PG4406 GAP-CLOSE-PWR
PG4407 GAP-CLOSE-PWR
PG4408 GAP-CLOSE-PWR
PG4411 GAP-CLOSE-PWR

42 PWR_VCORE_VSUMG+
PR4402 3K65R2F-1-GP
PWR_VCORE_VSUMG+_GAP
42 PWR_VCORE_VSUMG-
PR4403 1R2F-GP
PWR_VCORE_VSUMG-_GAP
Parallel

42 PWR_VCORE_COMPG
PR4404 150KR2F-L-GP
42 PWR_VCORE_FBG

PR4405 499R2F-2-GP
FBG_RC
PC4406 SC470P50V-2-GP
PC4407 SC47P50V2JN-3GP
PR4406 2K55R2F-GP
PR4407 267KR2F-GP
COMPG_R2
PC4408 SC150P50V2JN-3GP
modify schematic
Wayler , 2013-0315
PR4408
COMPG_R
PC4409 SC330P50V2KX-3GP
2K74R2F-GP
Setting LL = 3.9m

AXG	Loadline	PR4064
GT1	4.6mohm	237ohm
GT2	3.9mohm	432ohm

PC4410 SC330P50V2JC-2-GP
DY
PC4411
SCD01U50V2KX-L-GP
R4401 0R0402-PAD

42 PWR_VCORE_RTNG

VCC_AXG_SENSE 9
VSS_AXG_SENSE 9
Parallel

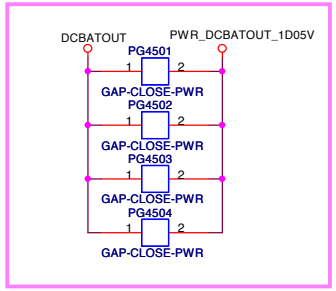
UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

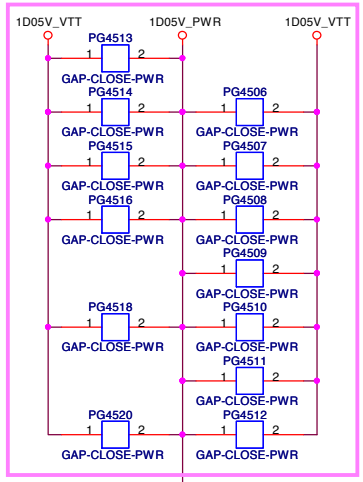
Title: ISL95833_CPU_CORE(3/3)
Size: Custom | Document Number: EA40_CX | Rev: -3
Date: Friday, June 21, 2013 | Sheet 44 of 103

SY8208D for 1D05V

SB_20121105-1



SB_20121105-1



-3 20130621-3

PWR_DCBATOUT_1D05V

OCP setting	
High	16A
Float	12A
Low	8A

PC4501 SCA7U25V5KX-L2-GP
PC4502 SCA7U25V5KX-L2-GP
PC4503 SCD1U50V2KX-L-GP
Del PC4811

Change to SY8208D SA_20121019

Freq=800KHz

PU4501
SY8208DQNC-GP-U
74.08208.K73
SB_20121105-1

PR4502 1KR2F-L-GP
3D3V_S0
37,48 1D05VTT_PWRGD
EA40-HW SB
OCP setting
PR4501 0R2J-L-GP
PR4504 0R402-PAD
46,47 RUNPWROK
SA_20121019
PC4506 SC1K5P50V2KX-L-GP

PR4503 2D2R2F-L-GP
PC4504 SCD1U25V3KX-L-GP
PWR_1D05V_BOOT
PWR_1D05V_BOOT_R
PWR_1D05V_PHASE
PWR_1D05V_VFB
PWR_1D05V_BYP
PWR_1D05V_IMAX
PWR_1D05V_EN
LDO_P5

PR4505 0R0402-PAD
3D3V_S0
modify schematic
Wayler , 2013-0315

PC4512 SC1U6D3V2KX-L-1-GP
PC4513 SC1U6D3V2KX-L-1-GP
EA40-HW SB
EA40-HW SB

Iomax = 6A
OCP >8A

CYNTEC. 5*5*3
DCR: 11~12mOhm
Idc : 8.5 A , Isat : 14A
PL4501
IND-D68UH-36-GP
68.R681A.10A
2nd = 68.R6810.20J

1D05V_PWR
PC4505 SC22U6D3V5MX-L3-GP
PC4507 SC22U6D3V5MX-L3-GP
PC4508 SC22U6D3V5MX-L3-GP
PC4509 SC22U6D3V5MX-L3-GP
DY
PC4510 SC1U50V3KX-L-GP
Del PT4803 , PT4804
Add PC4811 , PC4812 , PC4813 , PC4814

PC4511 SC220P50V2JN-3GP
R1
PR4506 75KR2F-GP
PWR_1D05V_VFB
100KR2F-L3-GP
PR4507
R2
modify schematic

Vo=0.6x(1+R1/R2)
=0.6x(1+75/100)
=1.05

UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC_1D05V(SY8208D)
Size: A3 | Document Number: EA40_CX | Rev: -3
Date: Friday, June 21, 2013 | Sheet 45 of 103

SSID = PWR.Plane.Regulator_1p2v0p6v

RT8207L for VDDQ

DCBATOUT PWR_DCBATOUT_VDDQ
PG4603 PG4606 PG4609 PG4612 GAP-CLOSE-PWR

VDDQ_PWR 1D35V_S3 VDDQ_PWR
PG4601 PG4602 PG4604 PG4605 PG4607 PG4608 PG4610 PG4611 PG4613 PG4614 PG4615 PG4616 PG4617 GAP-CLOSE-PWR

19,27 PM_SLP_S4# PR4602 0R0402-PAD PWR_VDDQ_EN
PC4603 SCD1U10V2KX-L1-GP DY

PR4601 5D1R2F-GP 5V_S5
PC4601 SC1U10V2KX-1GP
PWR_VDDQ_VCC5
OCP setting
PC4602 SC1KP50V2KX-1GP
PR4603 8K87R2F-2-GP
PWR_VDDQ_CS
PR4604 0R0603-PAD 5V_S5
PWR_VDDQ_VDDP
PC4608 SC1U10V2KX-1GP

3D3V_S5 PR4605 10KR2F-L1-GP

PU4601 RT8207MZQW-GP-U 74.08207.C73

Close to pin23
45,47 RUNPWROK
PWR_DCBATOUT_VDDQ PR4607 620KR2F-GP
PWR_VDDQ_TON PWR_VDDQ_EN PWR_VTT_EN PWR_VDDQ_VTTIN
1D35V_S3 PG4618 PG4619 GAP-CLOSE-PWR
PC4610 SC10U6D3V5MX-L1-GP
Close to pin23
DDR_VREF_PWR

PGOOD TON S5 S3 VLDOIN VTTGND VTT VTTSNS GND GND
CS VDD VDDP BOOT UGATE PHASE LGATE PGND VDDQ FB VTTREF

Iomax=1A
OCP>1.5A

PWR_VDDQ_BOOT PR4606 2D2R3F-L-GP PWR_VDDQ_PHASE_L PC4609 SCD1U25V3KX-L-GP
PWR_VDDQ_UGATE
PWR_VDDQ_PHASE
PWR_VDDQ_LGATE
PWR_VDDQ_SENSE PG4620 1D35V_S3 GAP-CLOSE-PWR
PWR_VDDQ_FB
PR4608 40K2R2F-GP PC4612 SC18P50V2JN-1-GP
R1
R2
PR4609 49K9R2F-L-GP
Vout setting
Close to PIN9
Close to output cap pin1, not inside of the output cap
Vout=0.75 x (1+R1/R2)
=0.75 x (1+40/49.9)
=1.35
PU4901 change to RT8207M
PR4610 0R0402-PAD DDR_VREF_S3
PWR_VDDQ_VTTREF
PC4613 SCD033U16V2KX-GP

+0.675VS
Iomax: 1.2A

0D675V_S0 PG4621 PG4622 GAP-CLOSE-PWR DDR_VREF_PWR
PC4614 PC4615 SC10U6D3V5MX-L1-GP DY

37 0D675V_EN PR4611 0R0402-PAD PWR_VTT_EN

PWR_DCBATOUT_VDDQ
modify schematic
Wayler , 2013-0315
PU4602 SIR172DP-T1-GE3-GP
84.00172.037
2nd = 84.08065.037
PC4604 PC4605 PC4606 SC477U25V5KX-L2-GP DY
PC4607 SCD1U25V3KX-L-GP

CYNTEC. 0.68uH 7*7*3
DCR= 5 ~ 5.5 mohm
Idc=15.5A, Isat=25A
IccMAX = 18.38A
IccTDC = 12.86A
OCP > 23.89A

PL4601 IND-D68UH-36-GP
68.R681A.10A
2nd = 68.R6810.20J
VDDQ_PWR
PC4611 SC1U16V3KX-5GP DY
PT4602 SE390U2D5VM-12-GP
77.53971.01L
2nd = 79.3971V.6AL

PU4603 SIRA12DP-T1-GE3-GP
84.SRA12.037
2nd = 84.08062.037
modify schematic
Wayler , 2013-0315

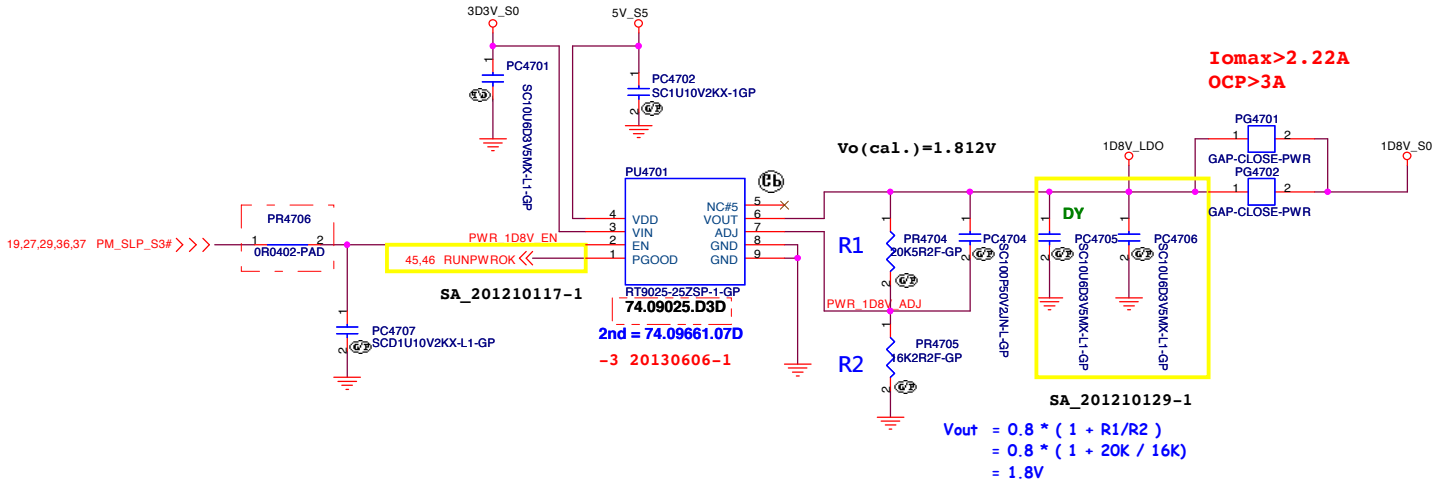
UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8207(VDDQ_VTT)	
Size: Custom	Document Number: EA40_CX	Rev: -3
Date: Thursday, June 20, 2013	Sheet 46 of 103	

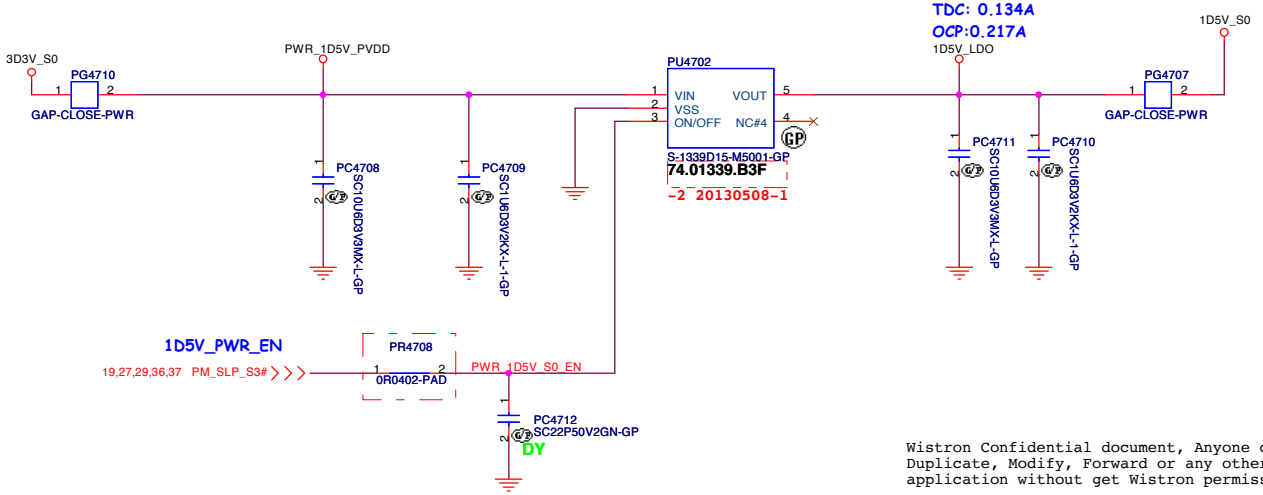
SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



S-1339D15 for 1D5V_S0

modify schematic
Wayler , 2013-0315



UMA C

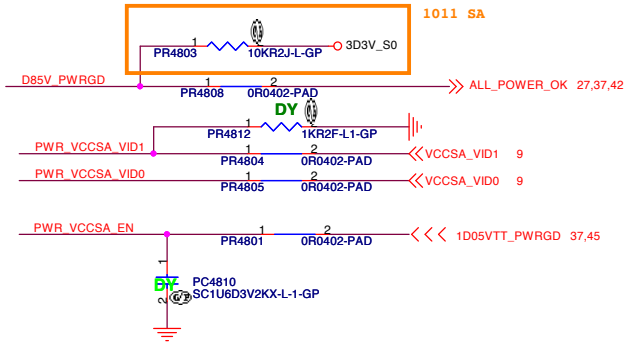
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LDO 1D8V&1D5V(RT9025)***

Size	Document Number	Rev
Custom	EA40 CX	-3

Date: Thursday, June 20, 2013 Sheet 47 of 103

LDO G978 for VCCSA



D0, D1 V_O Selection Table

D0	D1	V_O MODE=0	V_O MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

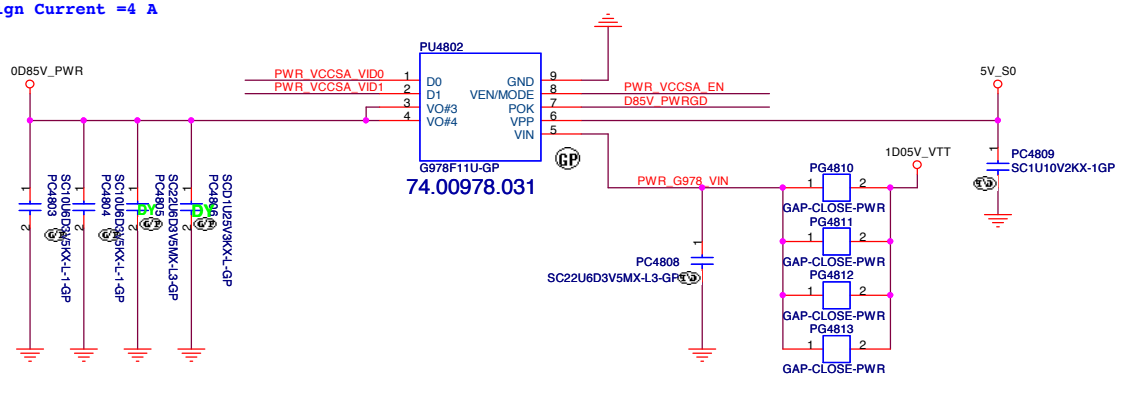
"x" means "don't care".

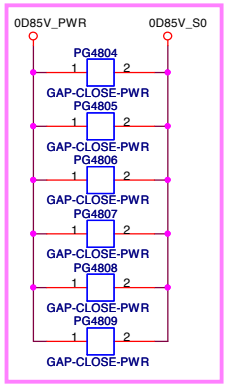
VEN/MODE Logic

VEN/MODE (VPP=5V)	EN logic
<0.6V	0
>1.0V	1

VEN/MODE (VPP=5V)	MODE logic
<2.0V	0
>2.6V	1

Design Current =4 A





UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

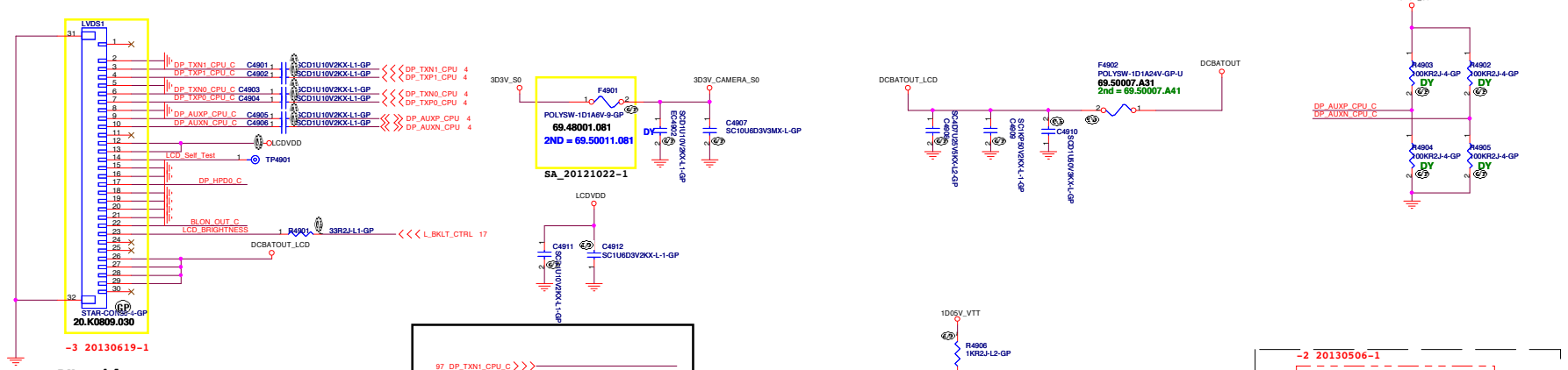
Title: VCCSA LDO G978

Size: A3 | Document Number: EA40_CX | Rev: -3

Date: Thursday, June 20, 2013 | Sheet 48 of 103

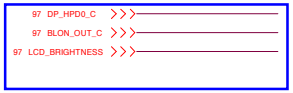
SSID = VIDEO

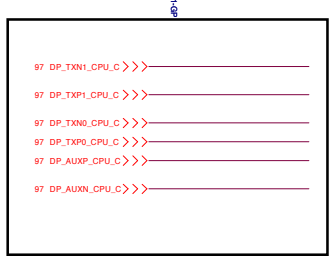
eDP Conn.

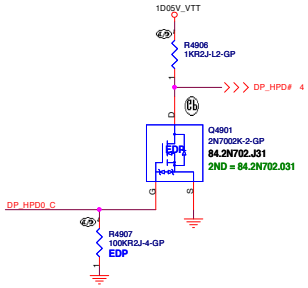


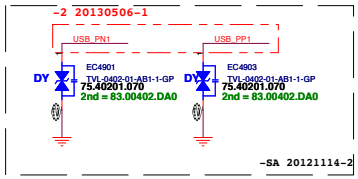
BY cable
L(pin5 GND):DMIC
H(pin5:floating):AMIC

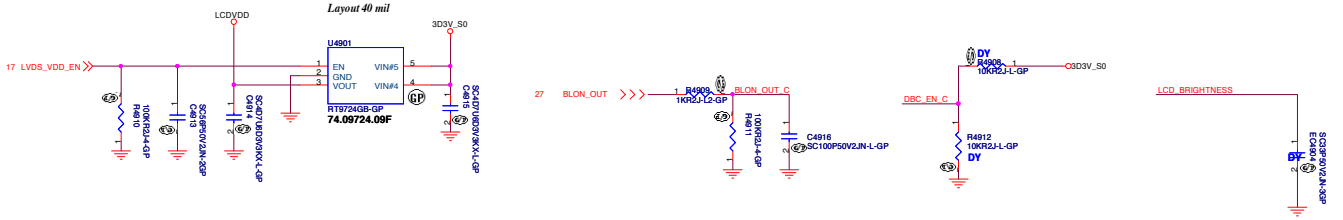
For TestPoint

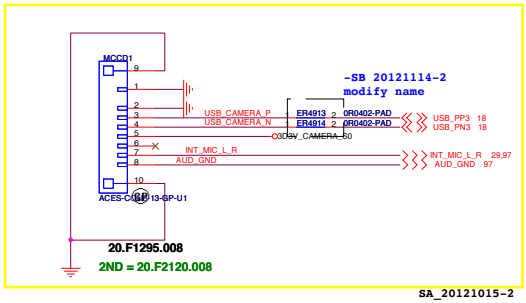


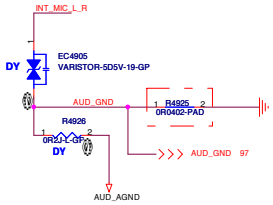




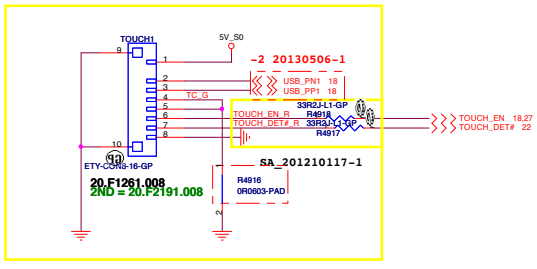








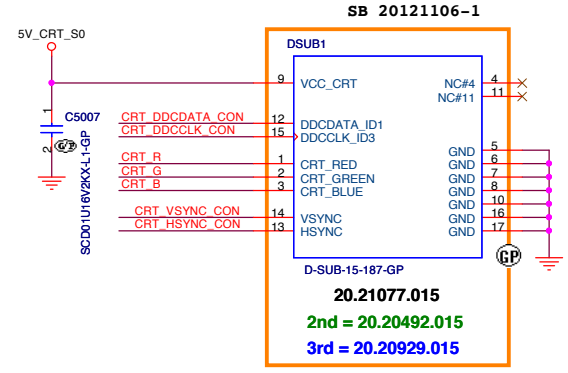
Touch Conn.

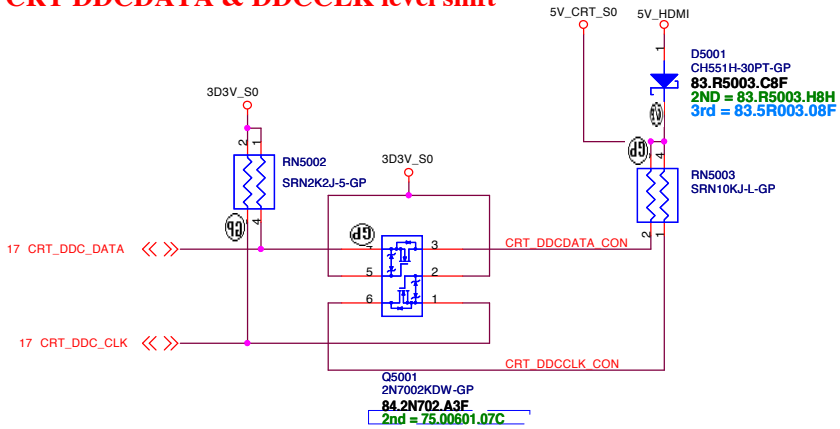


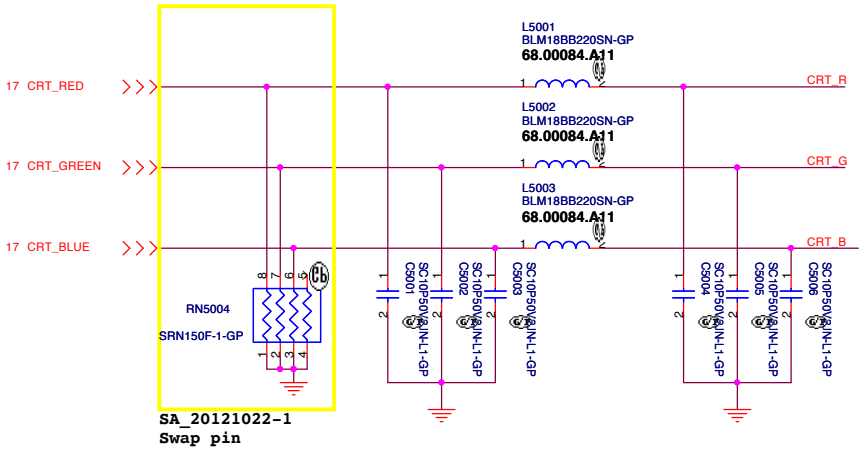
UMA C

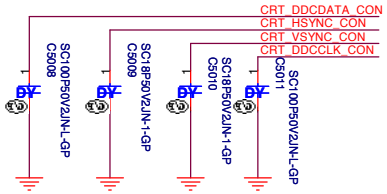
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **LCD Connector**		
Size: A2	Document Number: EA40_CX	Rev: -3
Date: Wednesday, June 19, 2013	Sheet 49 of 103	

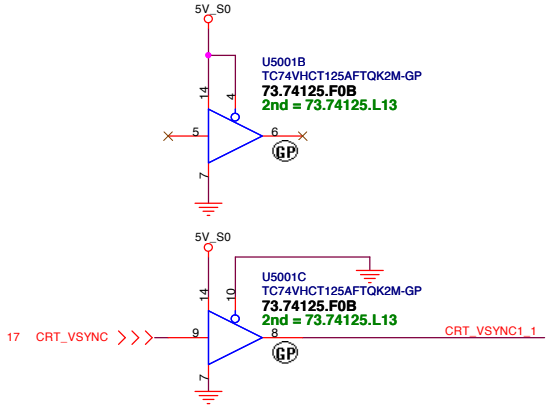
CRT DDCDATA & DDCCLK level shift

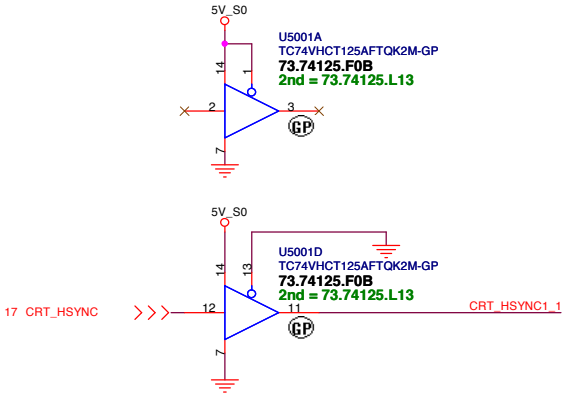


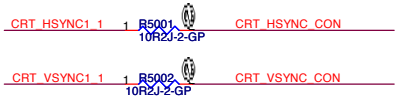












UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
A3	EA40_CX	-3

Date: Thursday, June 20, 2013 Sheet 50 of 103

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

Close to HDMI Connector

change = DIS:499 ohm
Fist = UMA Muxless:680 ohm

-1_20130315A

17 HDMI_CLK_R#
17 HDMI_CLK_R
17 HDMI_DATA0_R#
17 HDMI_DATA0_R
17 HDMI_DATA1_R#
17 HDMI_DATA1_R
17 HDMI_DATA2_R#
17 HDMI_DATA2_R

HDMI_DATA1_R#
HDMI_DATA1_R
HDMI_DATA2_R#
HDMI_DATA2_R
HDMI_CLK_R
HDMI_CLK_R#
HDMI_DATA0_R
HDMI_DATA0_R#

RN5114
SRN499F-GP

RN5115
SRN499F-GP

SA_20121022-1
Swap pin

HDMI_PLL_GND

Q5105
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031

5V_S0

HDMI1
SKT-HDMI23-91

HDMI_DATA2_R
HDMI_DATA2_R#
HDMI_DATA1_R
HDMI_DATA1_R#
HDMI_DATA0_R
HDMI_DATA0_R#
HDMI_CLK_R
HDMI_CLK_R#
DDC_CLK_HDMI
DDC_DATA_HDMI
5V_HDMI

22.10296.961
SA_20121024-2

5V_HDMI
5V_S0
F5101
POLYSW-1D1A6V-9-GP
69.48001.081
2ND = 69.50011.081
SA_20121022-1

HPD_HDMI_CON

3D3V_S0

R5111
150KR2J-L1-GP
HDMI_HPD_B

Q5102
MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.P11
3rd = 84.03904.L06

R5110
200KR2J-L1-GP

HDMI_HPD_E
R5129
0R0402-PAD
HDMI_PCH_DET 17

R5112
10KR2J-L-GP

D5103
BAW56-5-GP
83.00056.Q11
2nd = 75.00056.07D

5V_S0_D1
5V_S0_D2
5V_S0

RN5102
SRN2K2J-5-GP

Q5106
2N7002KDW-GP
84.2N702.A3F
2nd = 75.00601.07C

3D3V_S0

17 PCH_HDMI_CLK
17 PCH_HDMI_DATA

DDC_CLK_HDMI
DDC_DATA_HDMI

UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: A3 | Document Number: EA40_CX | Rev: -3

Date: Thursday, June 20, 2013 | Sheet 51 of 103

LED BACKLIGHT CONVERTER POWER

UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***eDP***	
Size A3	Document Number **EA40_CX**	Rev **-3**
Date: Thursday, June 06, 2013	Sheet 52 of 103	

(Blanking)

UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	**EA40_CX**	-3

Date: Thursday, June 06, 2013 Sheet 53 of 103

(Blanking)

UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

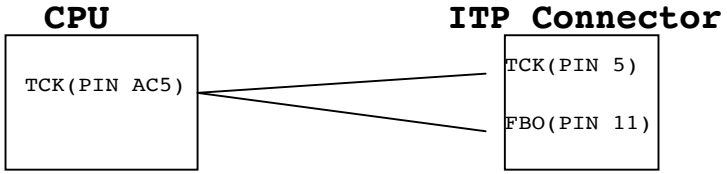
Size	Document Number	Rev
A4	EA40_CX	-3

Date: Thursday, June 06, 2013 Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



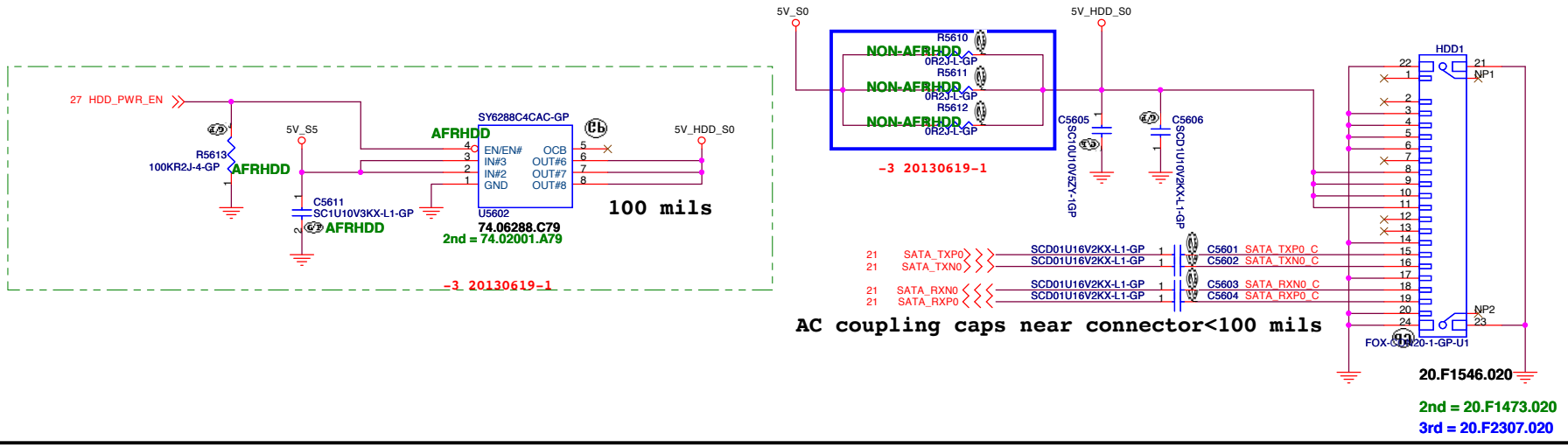
UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ITP		
Size A4	Document Number EA40 CX	Rev -3
Date: Thursday, June 06, 2013	Sheet 55 of 103	

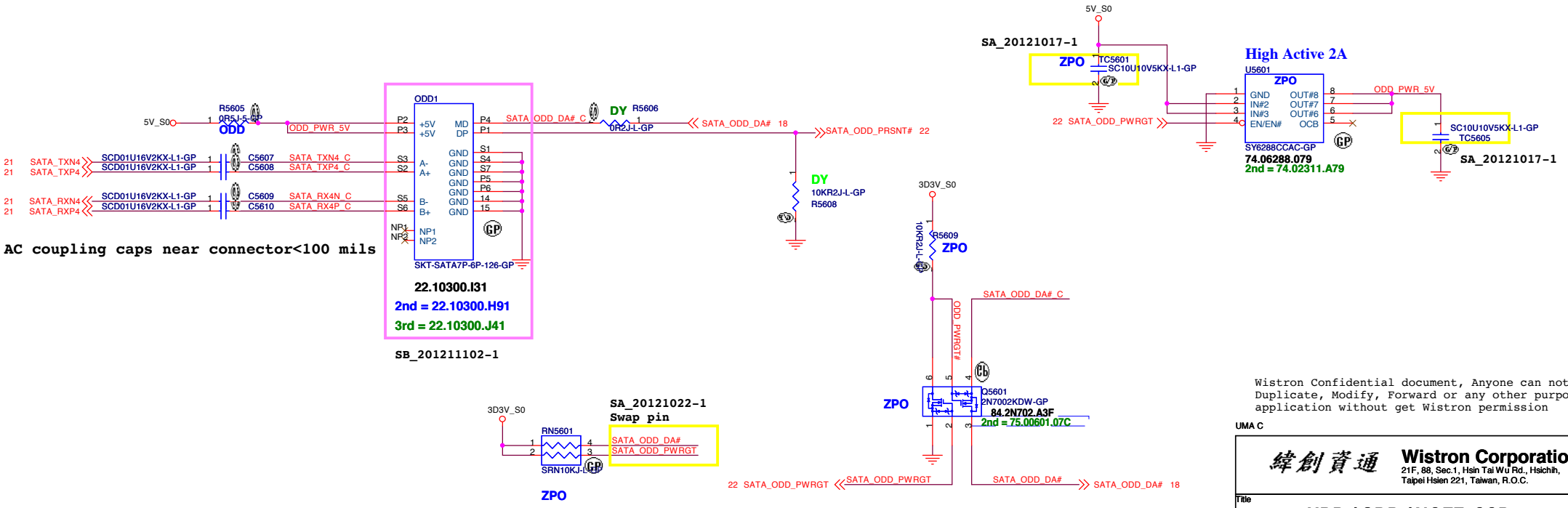
SSID = SATA

SATA HDD Connector



ODD Connector

SATA Zero Power ODD



UMA C

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD / ODD / NGFF_SSD	
Size A3	Document Number EA40 CX	Rev -3
Date: Thursday, June 20, 2013	Sheet 56 of 103	

UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

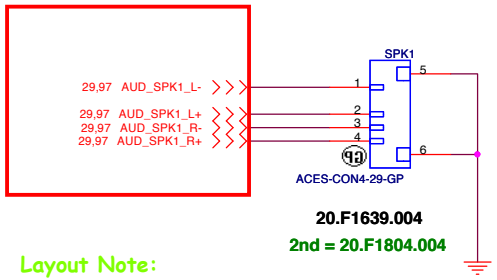
Title: ***E-SATA/USB CHARGER***

Size	Document Number	Rev
A3	EA40_CX	-3

Date: Thursday, June 06, 2013 Sheet 57 of 103

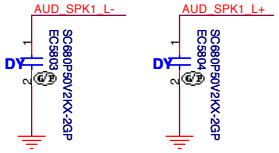
SSID = AUDIO

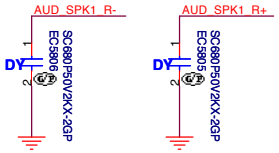
Speaker



20.F1639.004

2nd = 20.F1804.004

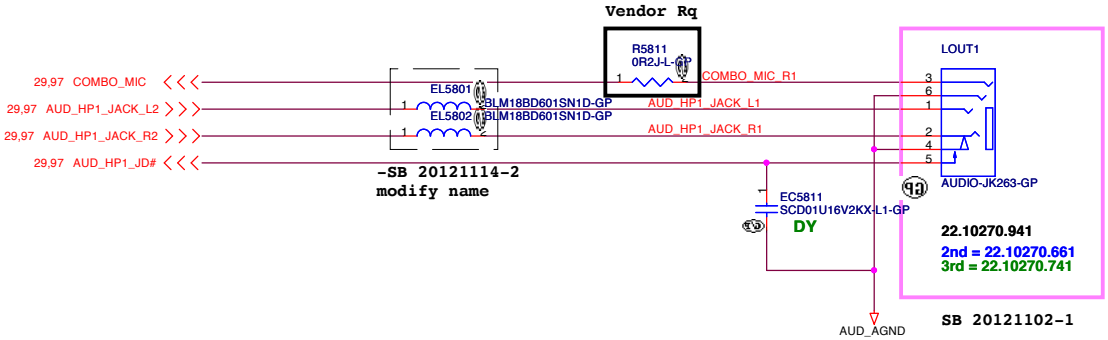




Layout Note:

Trace width=40mil

Combo Jack



-SB 20121114-2
modify name

22.10270.941

2nd = 22.10270.661

3rd = 22.10270.741

SB 20121102-1

UMA C

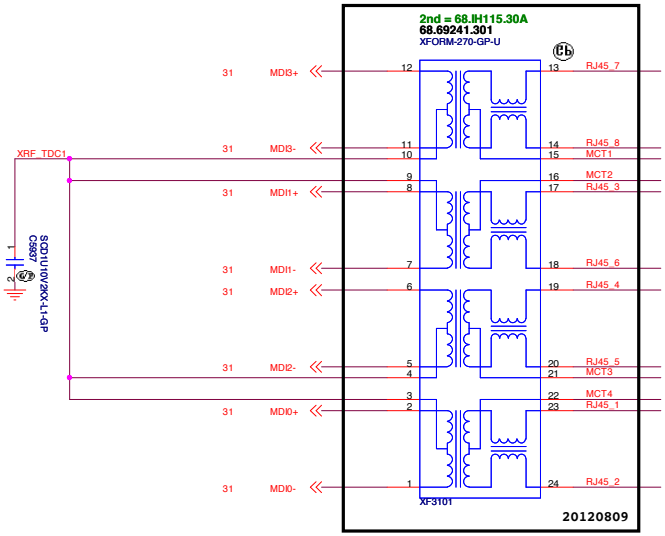
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

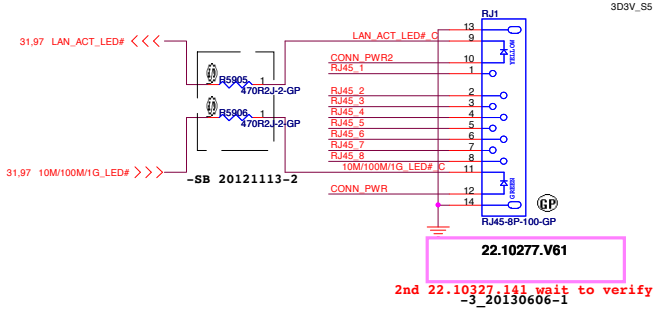
Title: Audio Jack

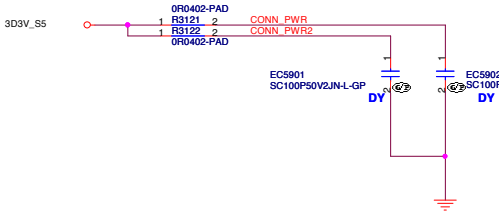
Size: A3 | Document Number: EA40 CX | Rev: -3

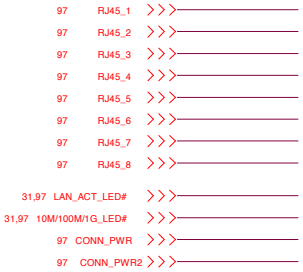
Date: Thursday, June 06, 2013 | Sheet 58 of 103

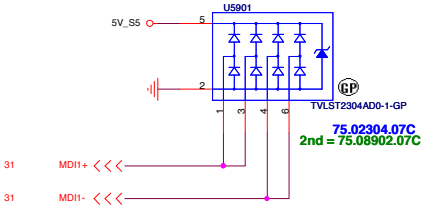
SSID = LAN

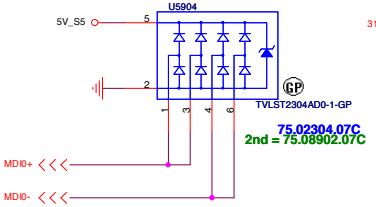


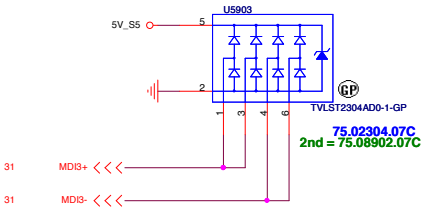


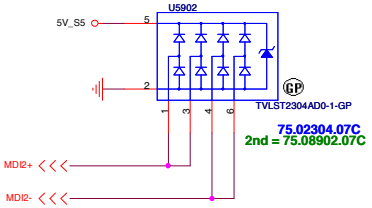


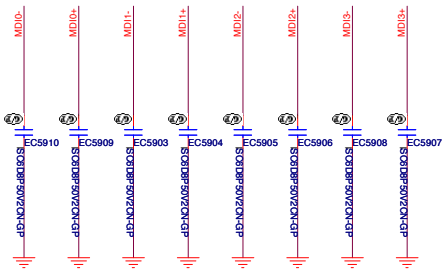


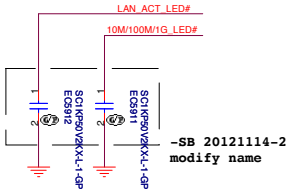


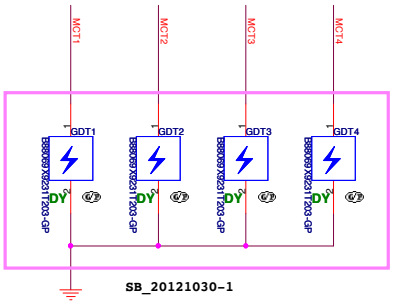


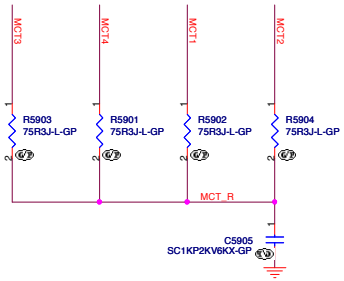












UMA C

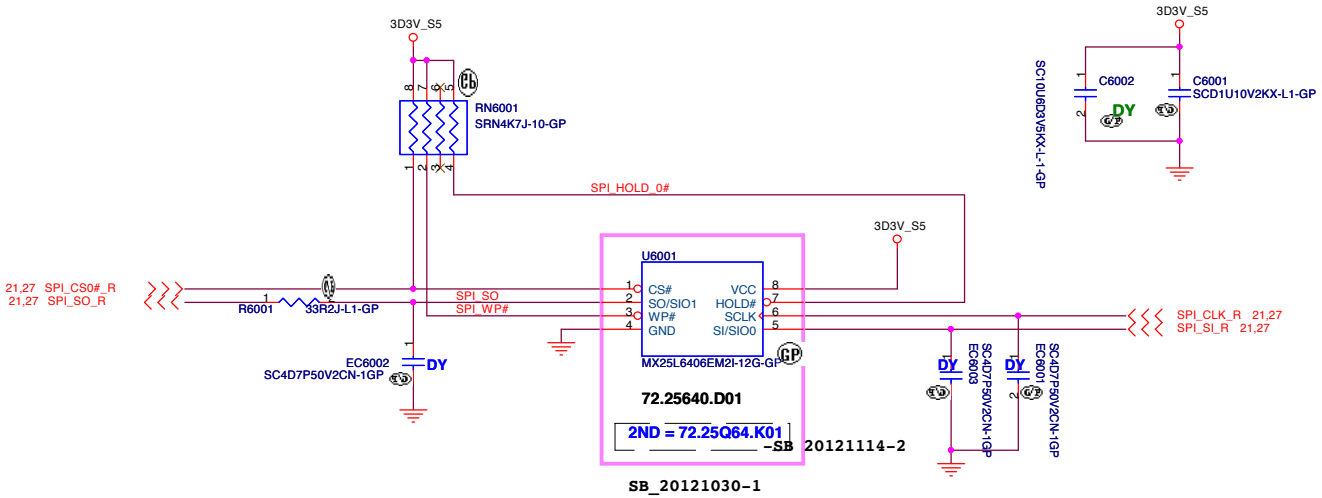
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONNECTOR**

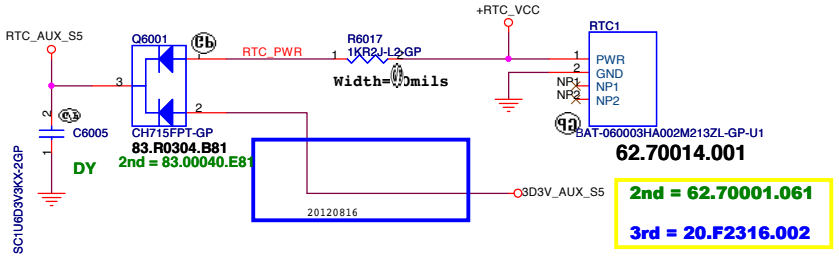
Size	Document Number	Rev
Custom	EA40_CX	-3

Date: Thursday, June 20, 2013 Sheet 59 of 103

SSID = Flash.ROM



SSID = RTC



UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Flash/RTC***

Size	Document Number	Rev
Custom	EA40 CX	-3

Date: Thursday, June 20, 2013 Sheet 60 of 103

SSID = USB

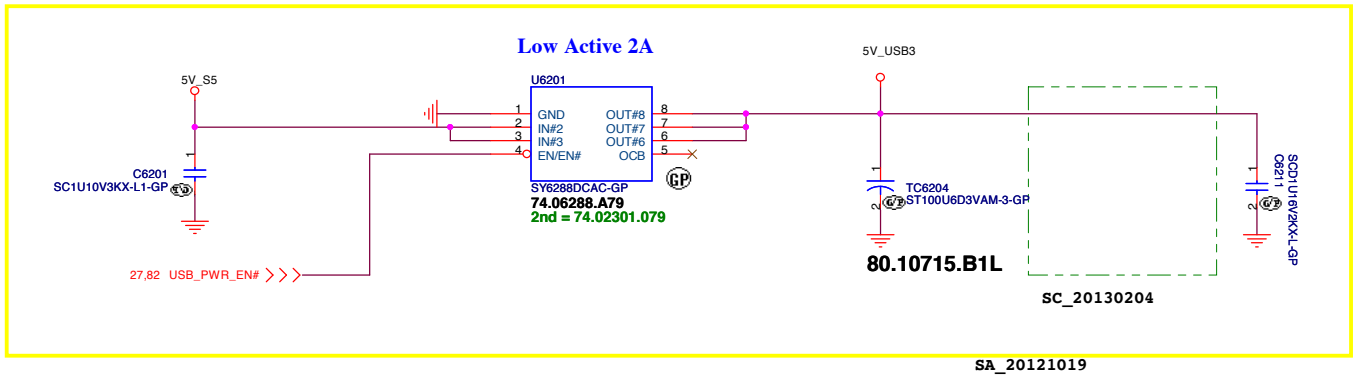
UMA C

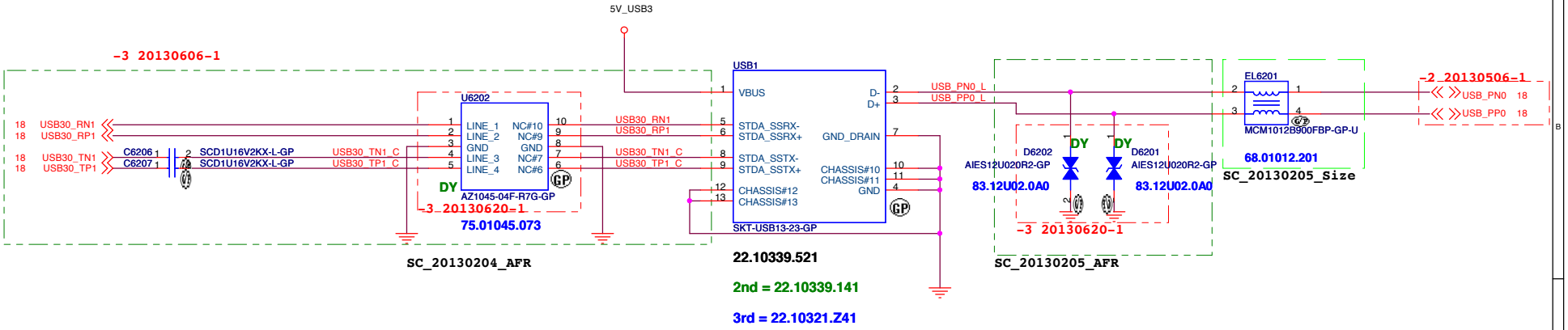
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
	USB Power SW	
Size: A3	Document Number: **EA40_CX**	Rev: **-3**
Date: Thursday, June 06, 2013	Sheet 61 of 103	

USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	





UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 3.0 Port**

Size	Document Number	Rev
A3	EA40_CX	-3

Date: Thursday, June 20, 2013 Sheet 62 of 103

SSID = User.Interface

Bluetooth Module conn.

ANNIE Bluetooth Module

UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***		
Size: A4	Document Number: **EA40_CX**	Rev: **-3**
Date: Thursday, June 06, 2013	Sheet 63 of 103	

UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

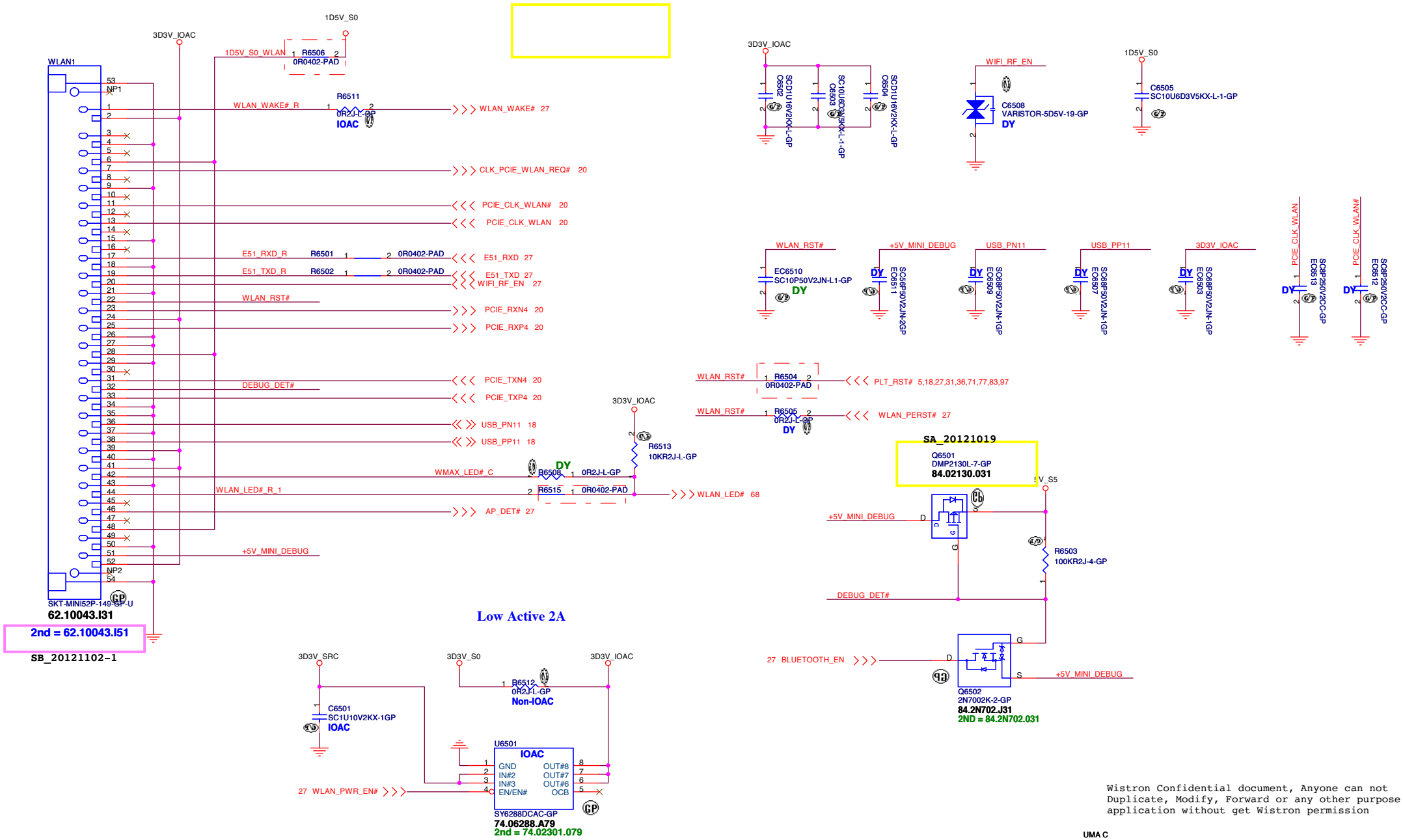
RESERVED

Size	Document Number	Rev
A4	EA40_CX	-3

Date: Thursday, June 06, 2013 Sheet 64 of 103

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/TP CONN

Size: A3 | Document Number: EA40_CX | Rev: -3

Date: Friday, June 21, 2013 | Sheet 65 of 103

SSID = Wireless

Mini Card Connector(WWAN)

UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size	Document Number	Rev
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UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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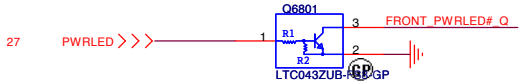
Date: Thursday, June 06, 2013 Sheet 67 of 103

SSID = User.Interface

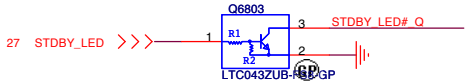
WLAN_LED

Power button LED



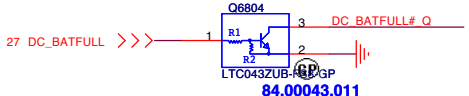
84.00043.011
2nd = 84.00143.D1K

Power STDBY_LED



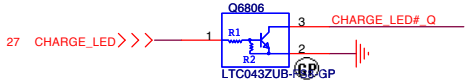
84.00043.011
2nd = 84.00143.D1K

Battery LED2(DC_BATFULL)

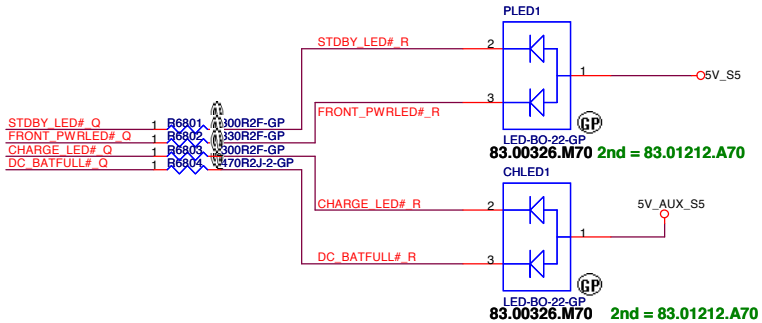


84.00043.011
2nd = 84.00143.D1K

Battery LED1(CHARGE)



84.00043.011
2nd = 84.00143.D1K



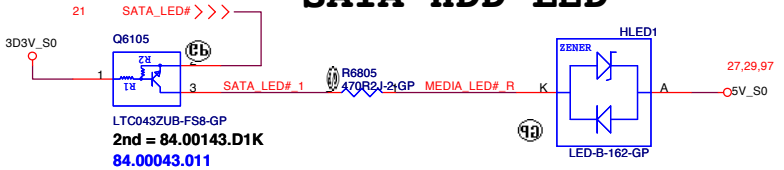
83.00326.M70 2nd = 83.01212.A70

83.00326.M70 2nd = 83.01212.A70

83.00193.N70

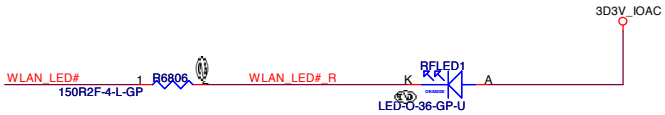
2nd = 83.19117.070

SATA HDD LED



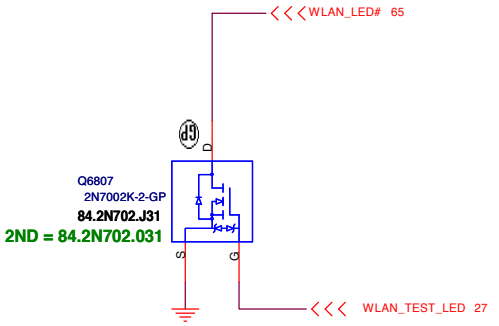
2nd = 84.00143.D1K
84.00043.011

83.00320.B70
2nd = 83.01211.070

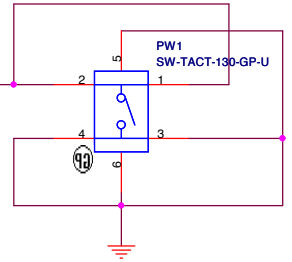


83.00270.D70

From module



for factory test



62.40009.731
2nd = 62.40089.441
3rd = 62.40009.D71

UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

Size	Document Number	Rev
Custom	EA40 CX	-3

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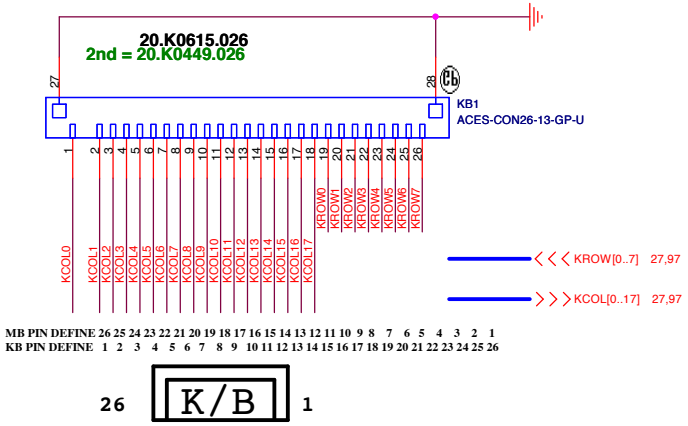
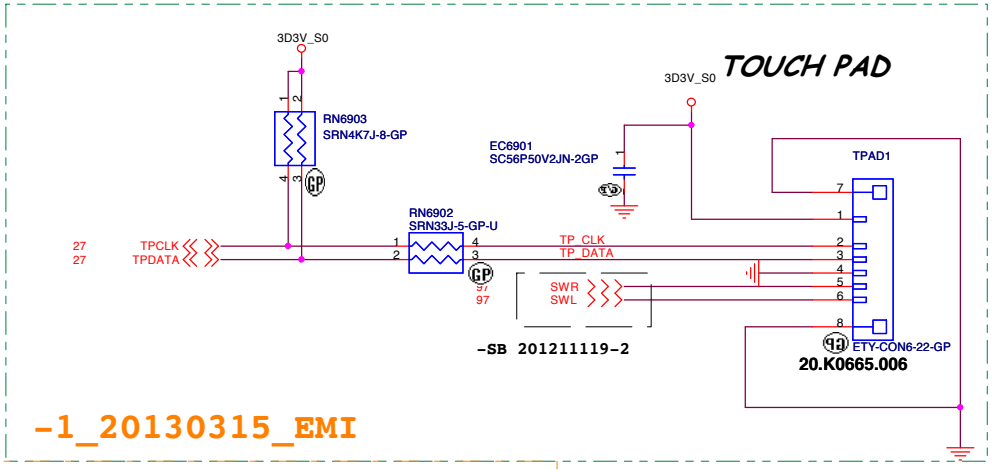
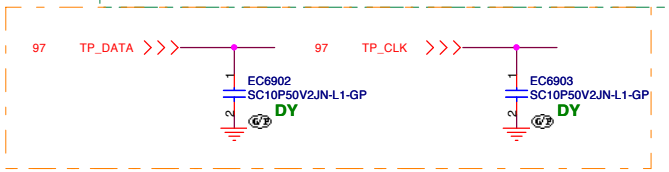
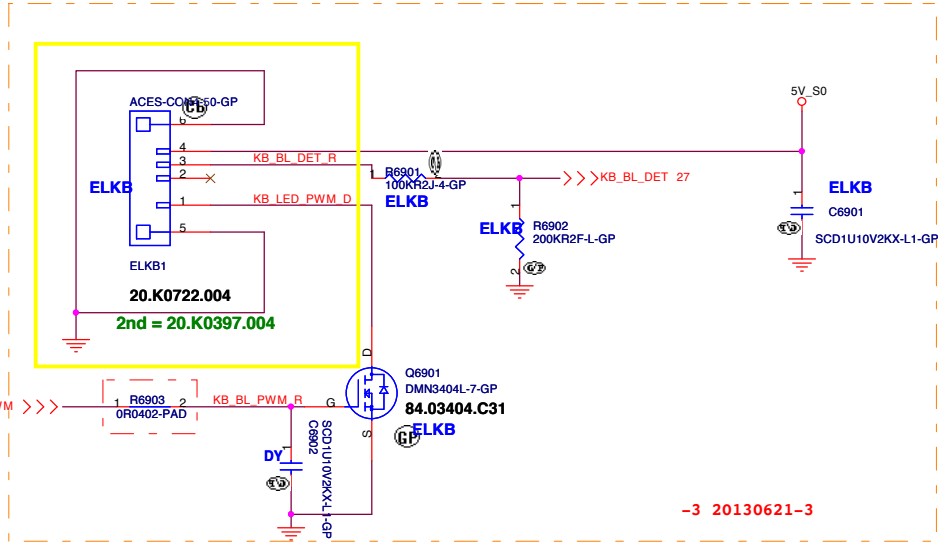
SSID = KBC

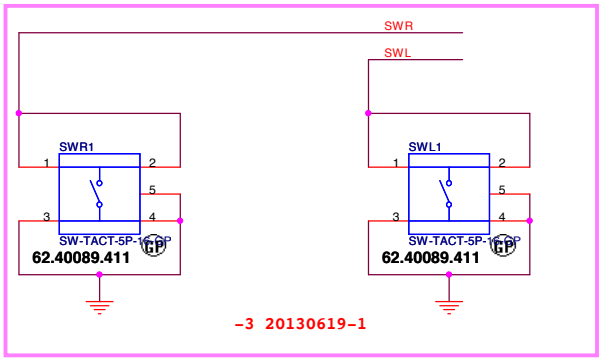
Internal KeyBoard Connector











UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Key Board/Touch Pad***

Size	Document Number	Rev
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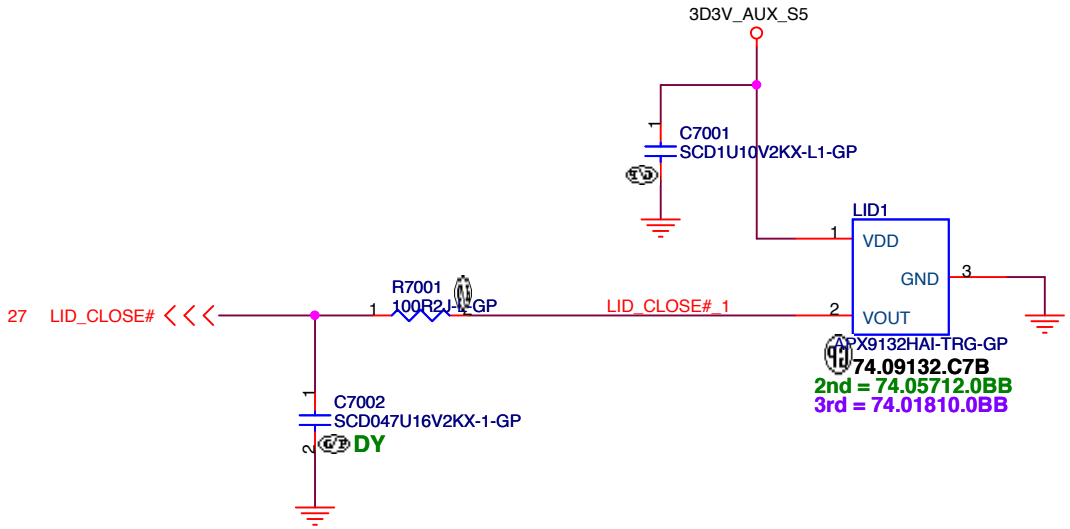

UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Hall Sensor**

Size	Document Number	Rev
A4	EA40_CX	-3

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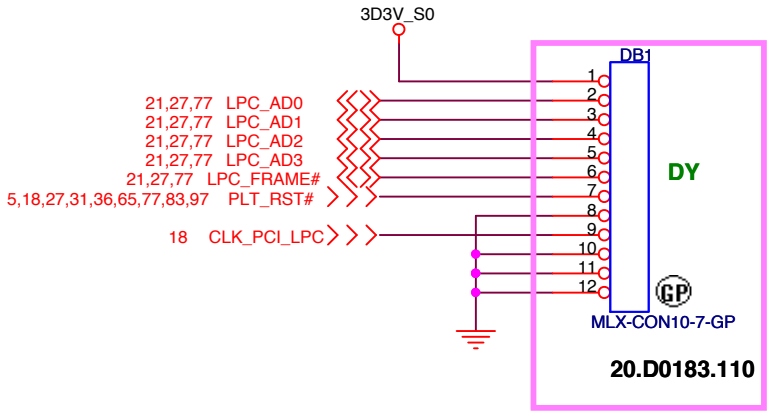

SB_20121030-1

UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	EA40_CX	-3

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UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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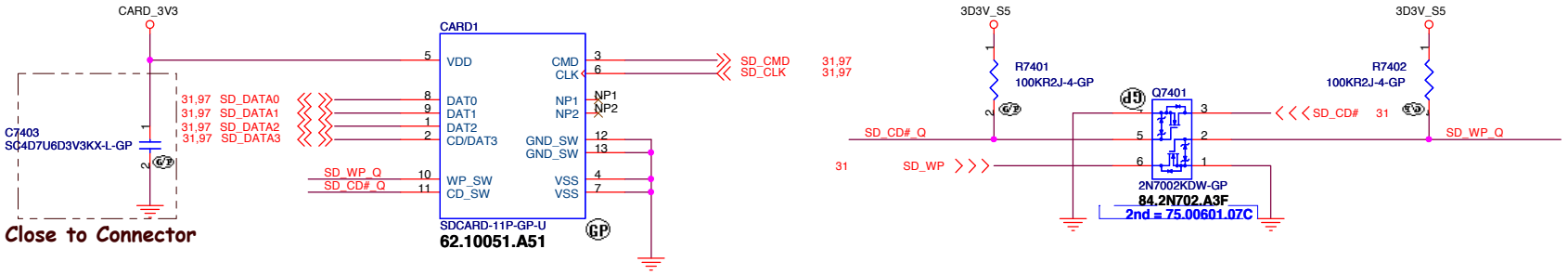
SSID = SDIO

SD/MMC Card Reader



SP1	SP1	SD_D7		xD_RDY
SP2	SP2	SD_D6	MS_INS#	xD_RE#
SP3	SP3	SD_D5		xD_CE#
SP4	SP4	SD_D4		xD_WE#
SP5	SP5	SD_D1	MS_CLK	xD_D6
SP6	SP6	SD_D0	MS_D7	xD_D5
SP7	SP7	SD_CLK	MS_D3	xD_D4
SP8	SP8	SD_CMD	MS_D6	xD_D3
SP9	SP9	SD_D3	MS_D2	xD_D2
SP10	SP10	SD_D2		xD_D7
SP11	SP11		MS_BS	xD_CLE
SP12	SP12	SD_WP	MS_D1	xD_WP#
SP13	SP13	SD_CD#	MS_D5	xD_ALE
SP14	SP14		MS_D4	xD_D0
SP15	SP15		MS_D0	xD_D1
SP16	SP16			xD_CD#

97 SD_WP_Q

97 SD_CD#_Q

UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size: Custom | Document Number: EA40_CX | Rev: -3

Date: Thursday, June 20, 2013 | Sheet 74 of 103

SSID = ExpressCard

UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
	New Card	
Size: A3	Document Number: **EA40_CX**	Rev: **-3**
Date: Thursday, June 06, 2013	Sheet 75 of 103	

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	EA40_CX	-3

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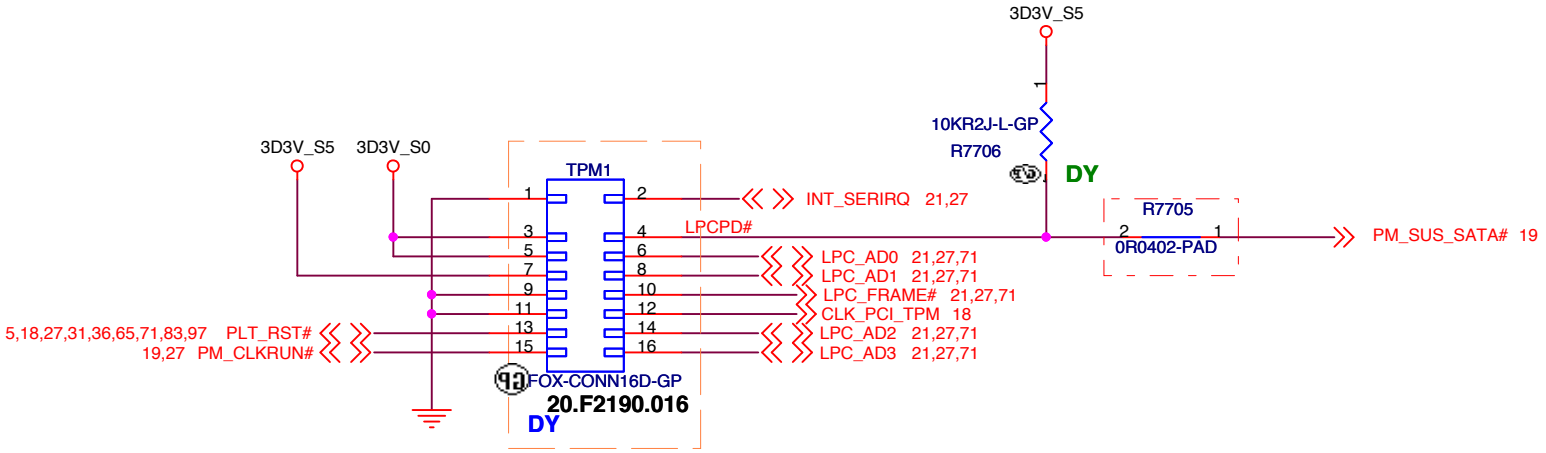

-SB 20121113-2

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPM

Size	Document Number	Rev
A4	EA40 CX	-3

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UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
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SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G- Sensor

Size	Document Number	Rev
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UMA C

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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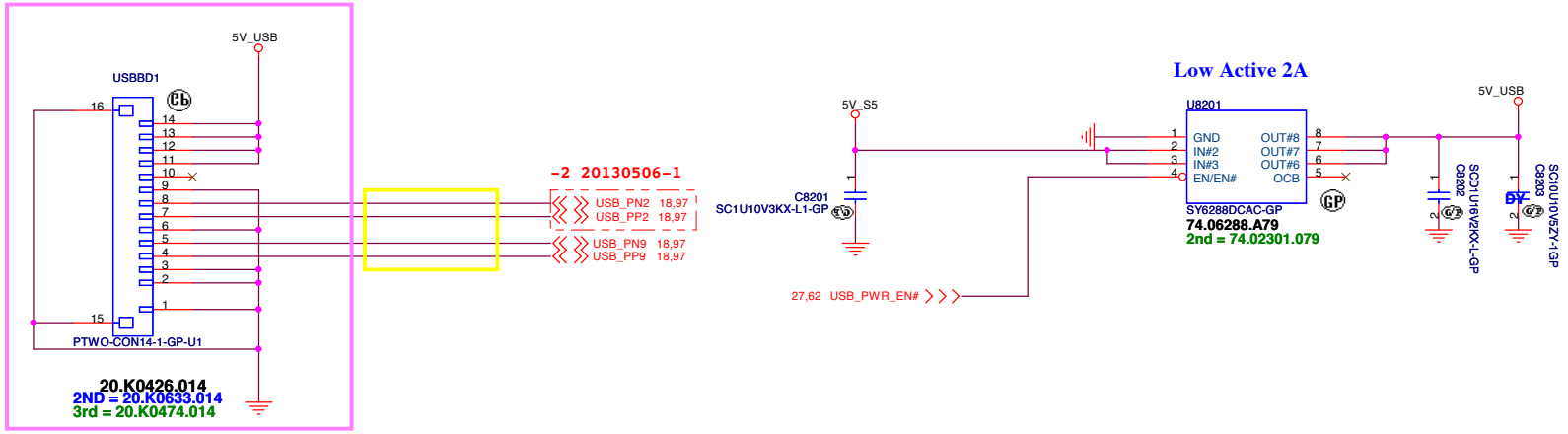

SB 20121102-1

UMA C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	EA40_CX	-3

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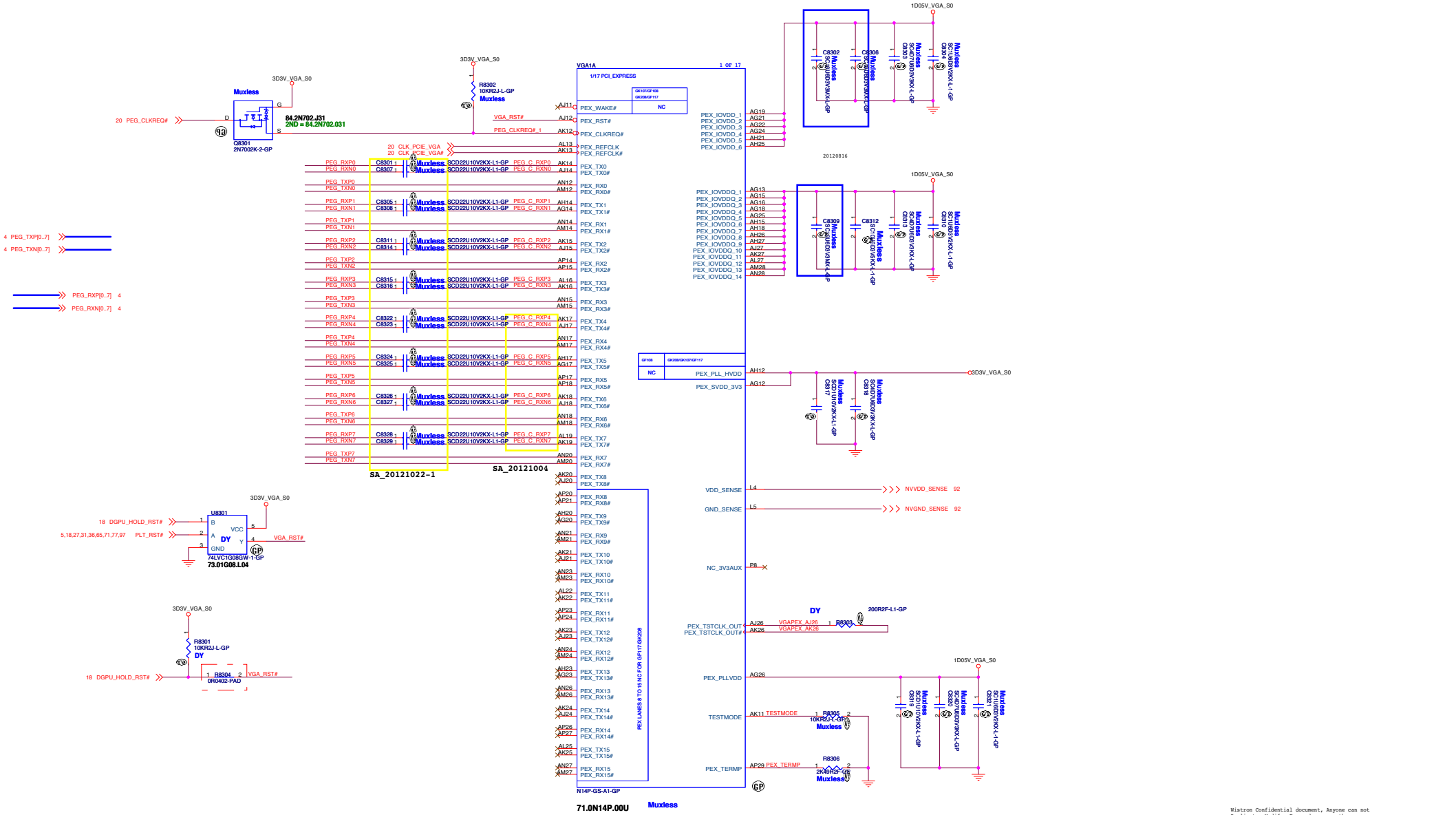

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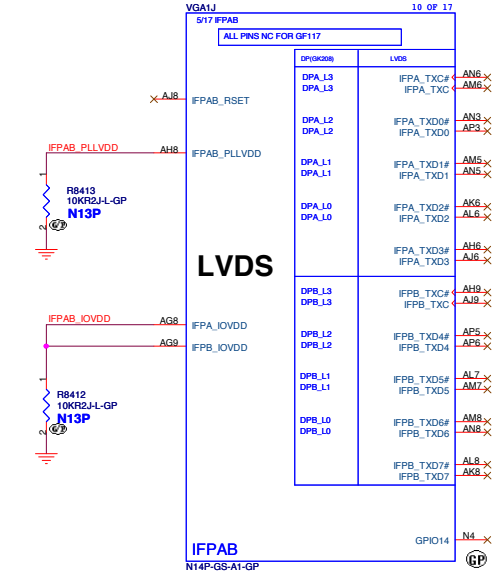
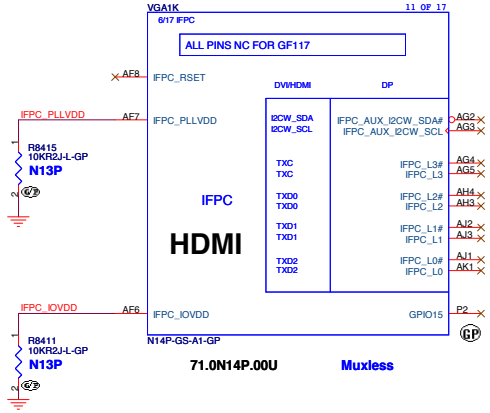
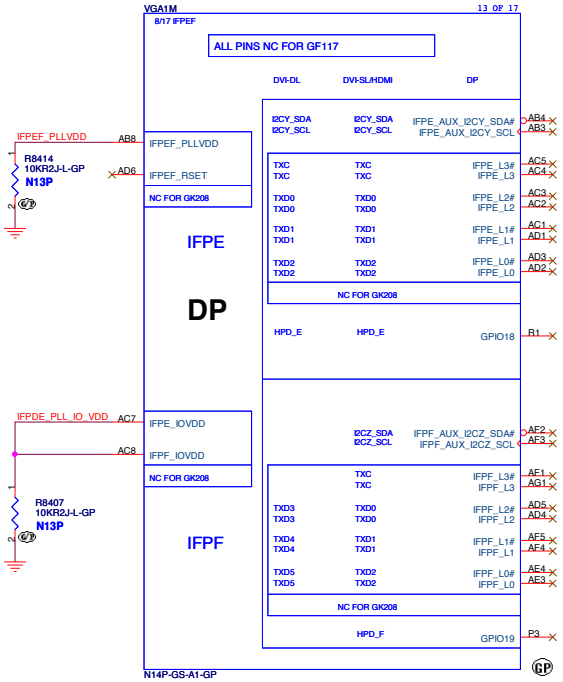
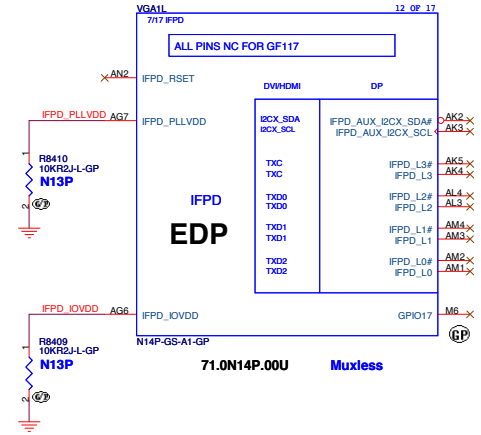
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU(PEG)***
Size: A2	Document Number: **EA40_CX** Rev: **-3**
Date: Thursday, June 20, 2013	Sheet 83 of 103









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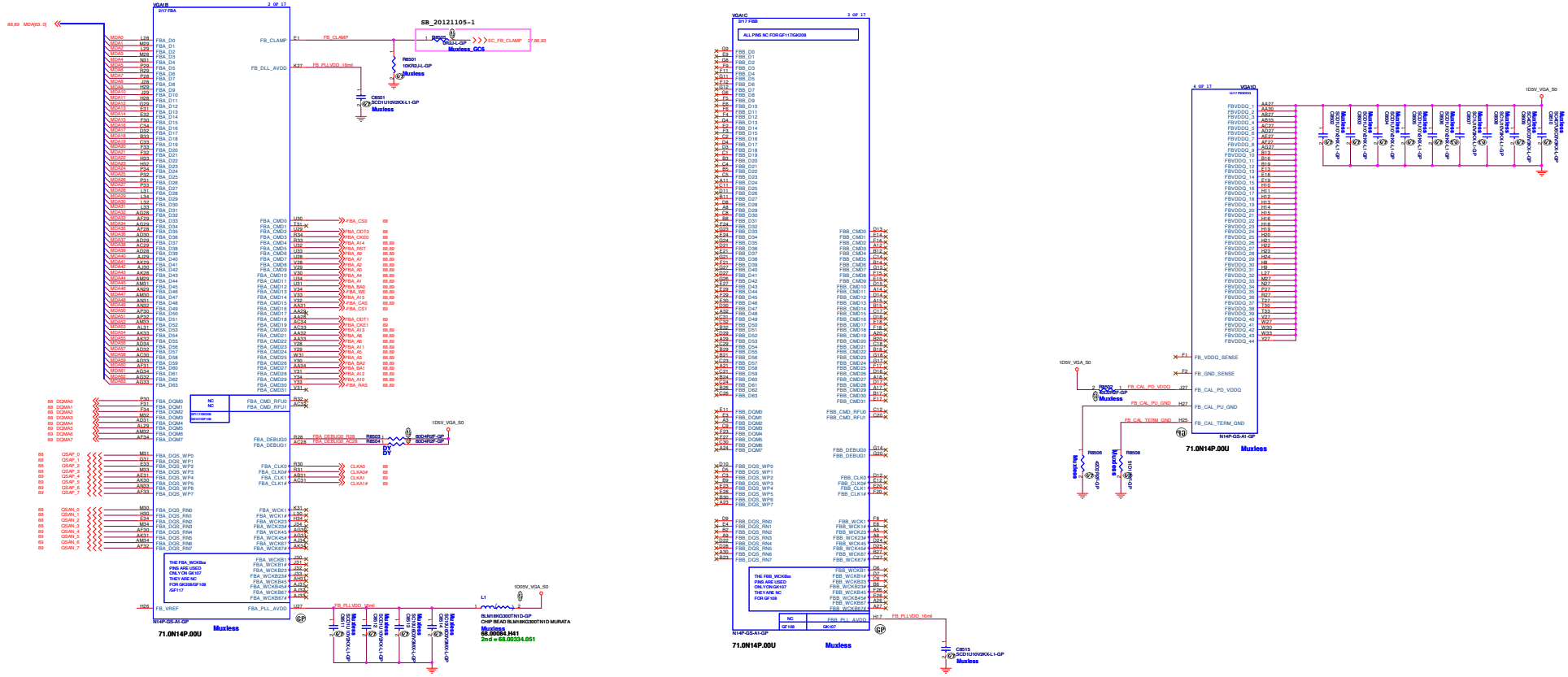
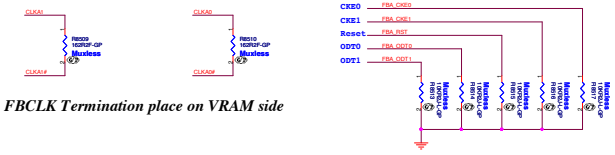
Title: GPU (DIGITALOUT)

Size	Document Number	Rev
Custom	EA40_CX	-3

Date: Thursday, June 06, 2013 Sheet 84 of 103



Group A



FBCLK Termination place on VRAM side

LIMA C

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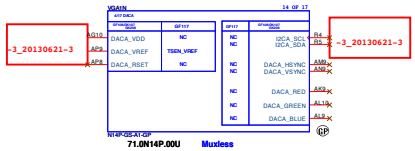
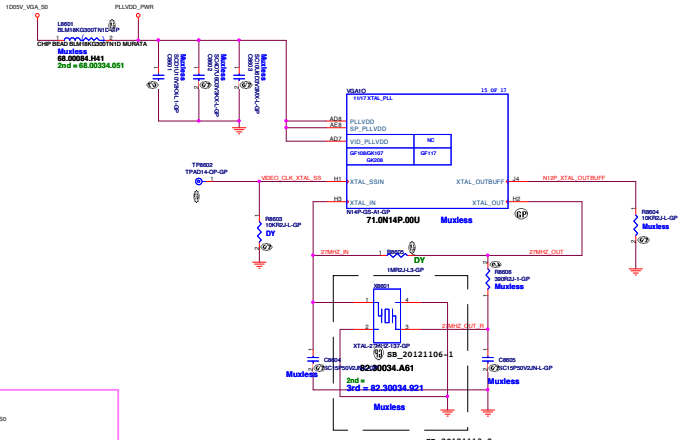
Title: **GPU (VRAM I/F)**

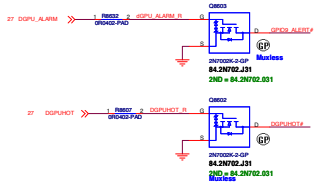
Size: A3 | Document Number: **EA40 CX** | Rev: **-3**

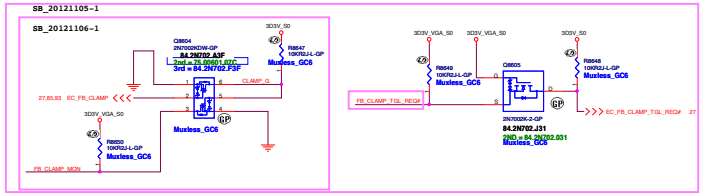
Date: Friday, June 21, 2013 | Sheet 85 of 103

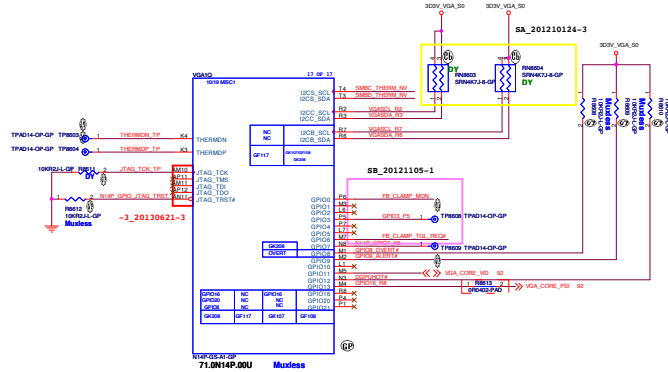


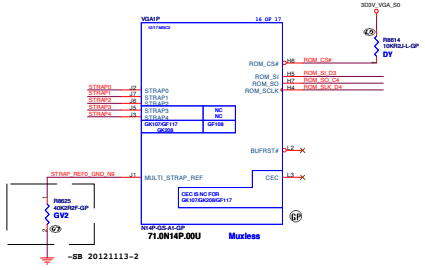


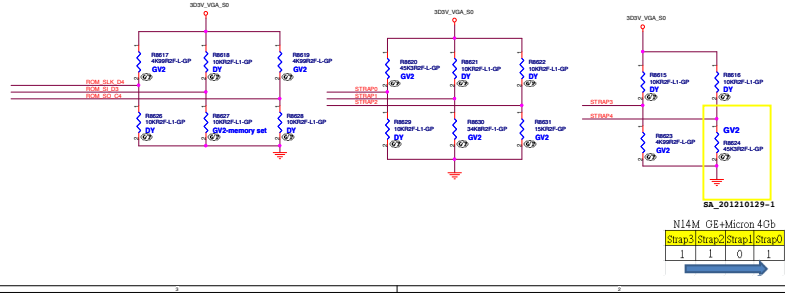
unknown function











N14M GE+Micron 4Gb

Strap3	Strap2	Strap1	Strap0
1	1	0	1

64.49915.6DL
64.10025.L0L
64.15025.6DL
64.20025.6DL
64.24925.6DL
64.30125.6DL
64.34825.6DL
64.45325.6DL

Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

4.99Kohm
10Kohm
15Kohm
20Kohm
24.9Kohm
30.1Kohm
34.8Kohm
45Kohm

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M-16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production ready
				MT41J128M16JT-107G:K	900	1150	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production ready
				K4W2G1646E-BC11	900	1204	Production ready
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	N/A	Production ready
				H5TQ2G63DFR-11C	900	N/A	Production ready
		0xC	1.5V/ 1.5V	H5TC2G63FFR-11C	1000	N/A	Production ready

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0xB	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
	Micron	0xD	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production ready
	Hynix	0x3	1.5V/ 1.5V	H5TQ4G63MFR-11C	900	N/A	Production ready
		0x4		H5TQ4G63AFR-11C		N/A	Post-Production Candidate

N14M-GE use Binary Strap. Please see the below information.

Table 122 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

N14P-GV2

Strap Pin Name	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
	1	0	0	0
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
	N	N	N	N
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
	1	0	0	1
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]
	1	1	1	1
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
	0	1	1	0
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
	0	0	0	0
STRAP 3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
	0	0	0	0
STRAP 4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V
	0	1	1	1

Support GEN3

ROM_SCLK

Strap2

N14P-GT1-A2	0x0FE4	0010	15K ohm pull-down	0100	25K ohm pull-down
N14P-GV2-B-A1	0x1292	1000	5K ohm pull-up	0010	15K ohm pull-down

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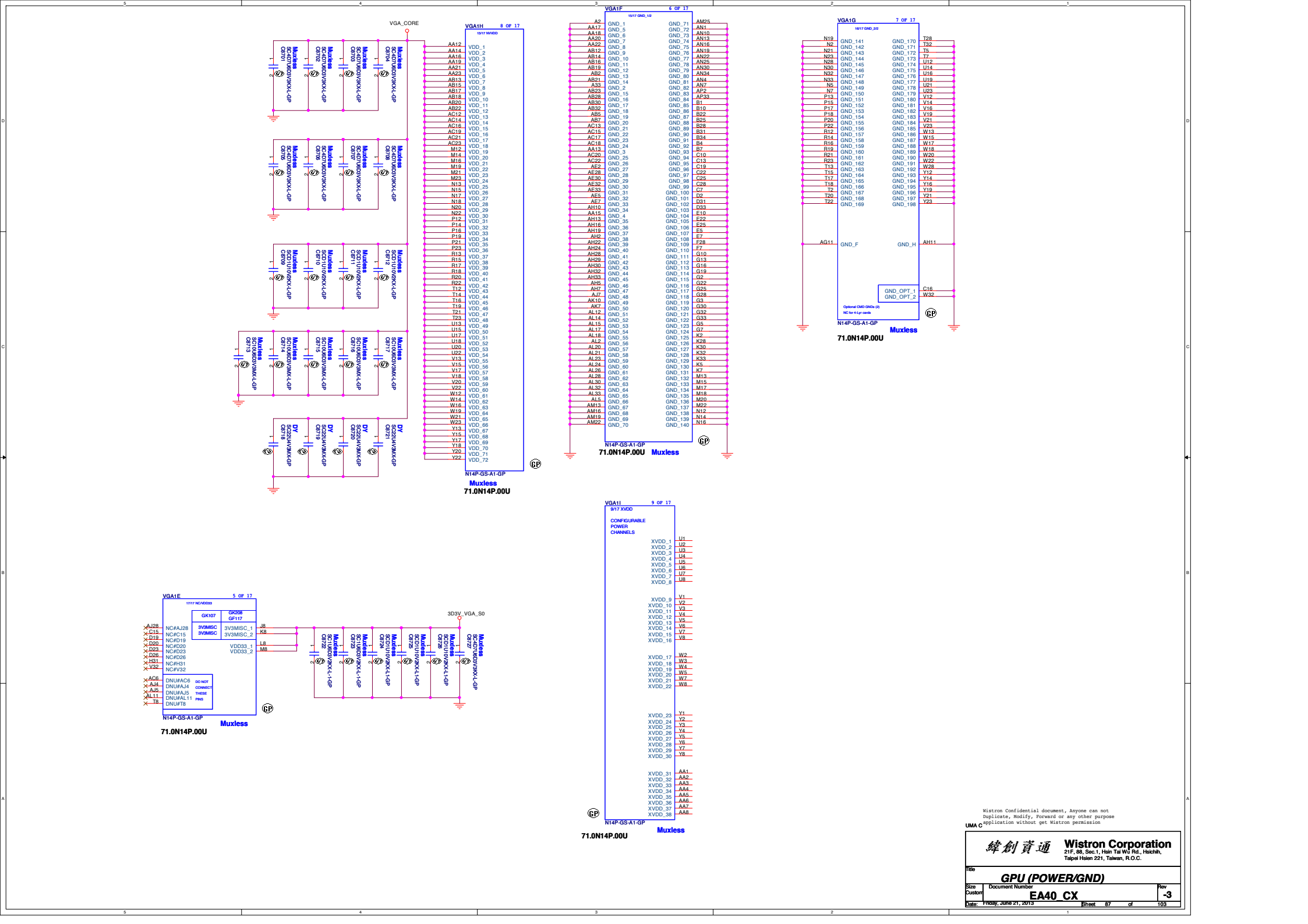
Title: GPU (GPIO/STRAP)

Size: Document Number: EA40 CX Rev: -3

Date: Friday, June 21, 2013 Sheet 86 of 126



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Title: **GPU (POWER/GND)**

Size	Document Number	Rev
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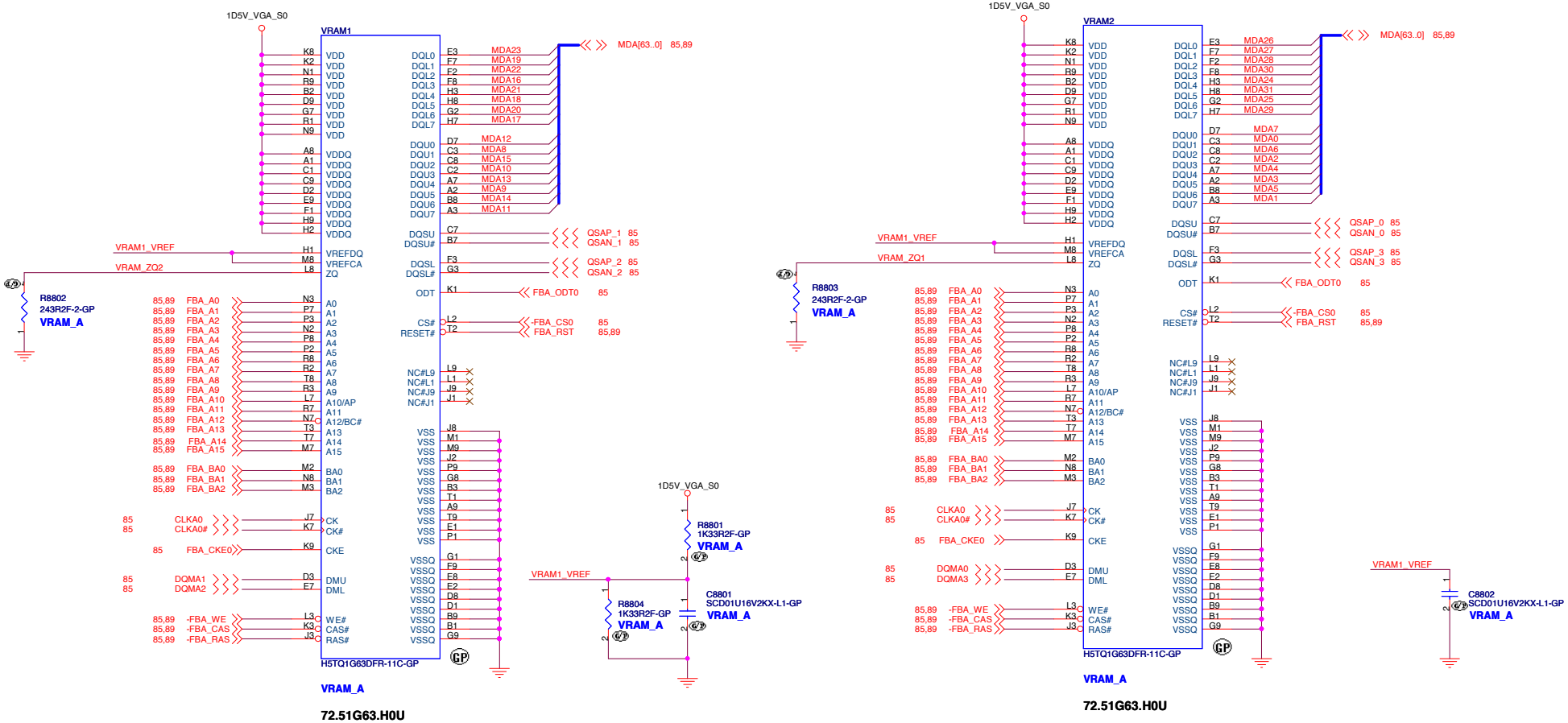
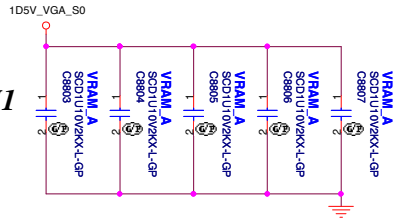
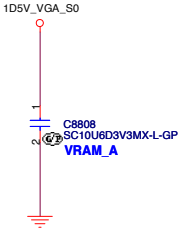
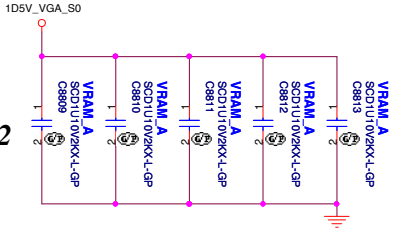


FOR VRAM1





FOR VRAM2



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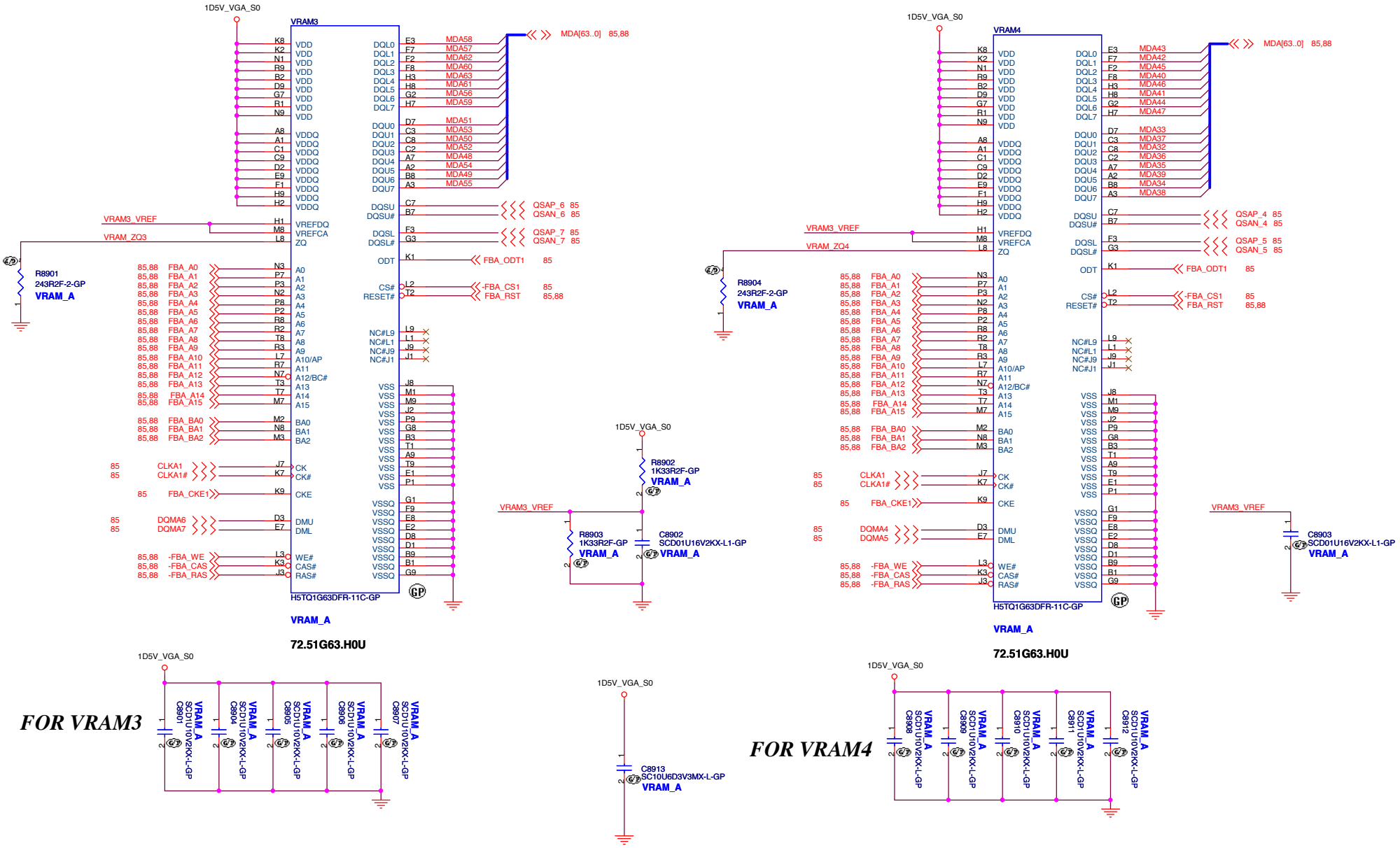
Title	***GPU-VRAM1,2 (1/4)***
Size: Custom	Document Number: **EA40_CX** Rev: **-3**
Date: Thursday, June 20, 2013	Sheet 88 of 103



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Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
Custom	EA40_CX	-3

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Title: ***GPU-VRAM5,6 (3/4)***

Size	Document Number	Rev
Custom	**EA40_CX**	**-3**

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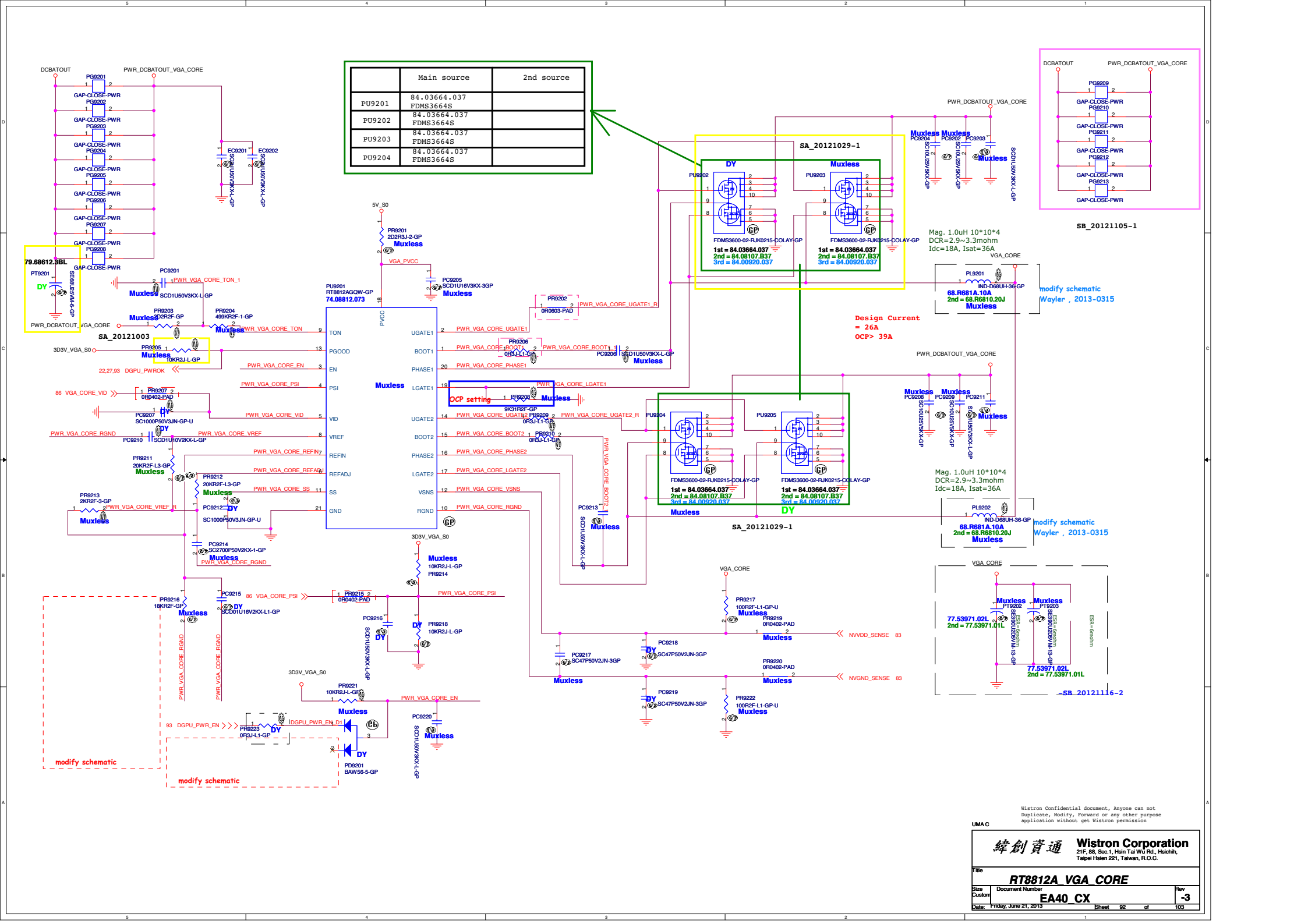
Title: ***GPU-VRAM7,8 (4/4)***

Size	Document Number	Rev
Custom	**EA40 CX**	-3

Date: Thursday, June 06, 2013 Sheet 91 of 103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PU9202
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FDMS3664S
PU9204
84.03664.037
FDMS3664S
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SA_20121003
SB_20121105-1
SB_20121116-2
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2nd = 84.08107.B37
3rd = 84.00920.037
Mag. 1.0uH 10*10*4
DCR=2.9~3.3mohm
Idc=18A, Isat=36A
68.R681A.10A
2nd = 68.R6810.20J
Muxless
DY
modify schematic
Wayler , 2013-0315
Design Current
= 26A
OCP> 39A
OCP setting
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2nd = 77.53971.01L
79.68612.3BL
DCBATOUT
PWR_DCBATOUT_VGA_CORE
VGA_CORE
5V_S0
3D3V_VGA_S0
VGA_PVCC
PVCC
TON
PGOOD
EN
PSI
VID
REFIN
REFADJ
SS
GND
UGATE1
BOOT1
PHASE1
LGATE1
UGATE2
BOOT2
PHASE2
LGATE2
VSNS
RGND
NVVDD_SENSE
NVGND_SENSE
PWR_VGA_CORE_RGND
PWR_VGA_CORE_EN
PWR_VGA_CORE_PSI
PWR_VGA_CORE_VID
PWR_VGA_CORE_VREF
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PWR_VGA_CORE_LGATE2
PWR_VGA_CORE_VSNS
DGPU_PWROK
DGPU_PWR_EN
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PWR_VGA_CORE_REFADJ
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PWR_VGA_CORE_TON_1
DGPU_PWR_EN_D1
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modify schematic
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Custom
Document Number
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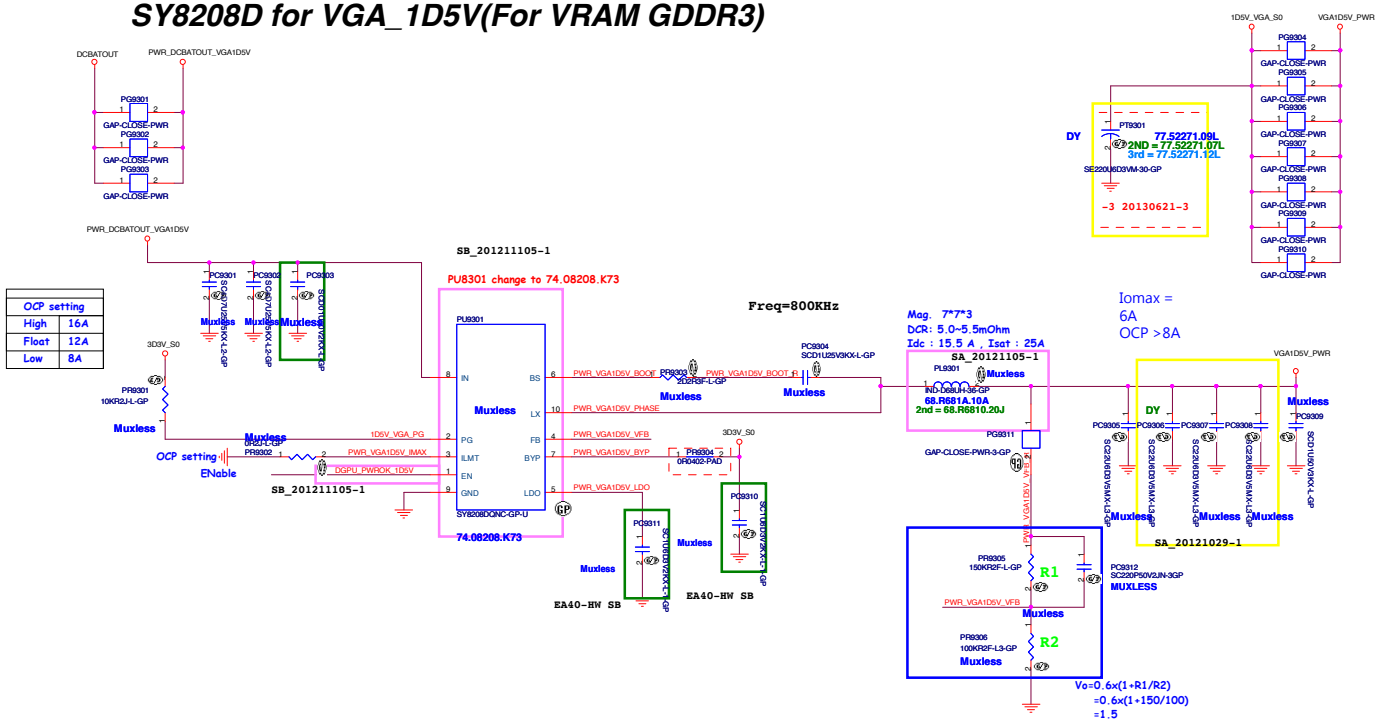
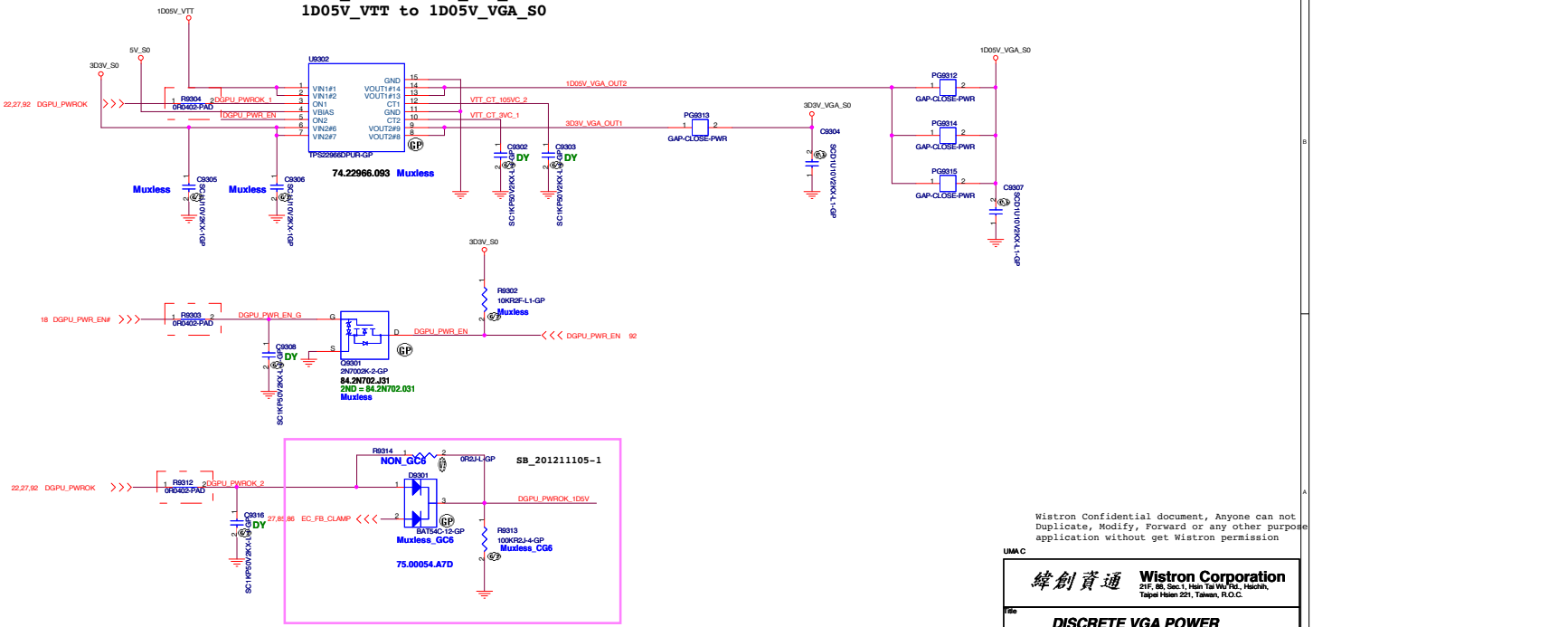
SY8208D for VGA_1D5V(For VRAM GDDR3)



3D3V_S0 to 3D3V_VGA_S0
1D05V_VTT to 1D05V_VGA_S0



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Title: DISCRETE VGA POWER

Size	Document Number	Rev
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Title

LVDS_Switch

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A4	EA40_CX	-3

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Title: ***CRT_Switch***

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SSID = SDIO

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Title: ***TOUCH PANEL***

Size	Document Number	Rev
A2	EA40_CX	-3

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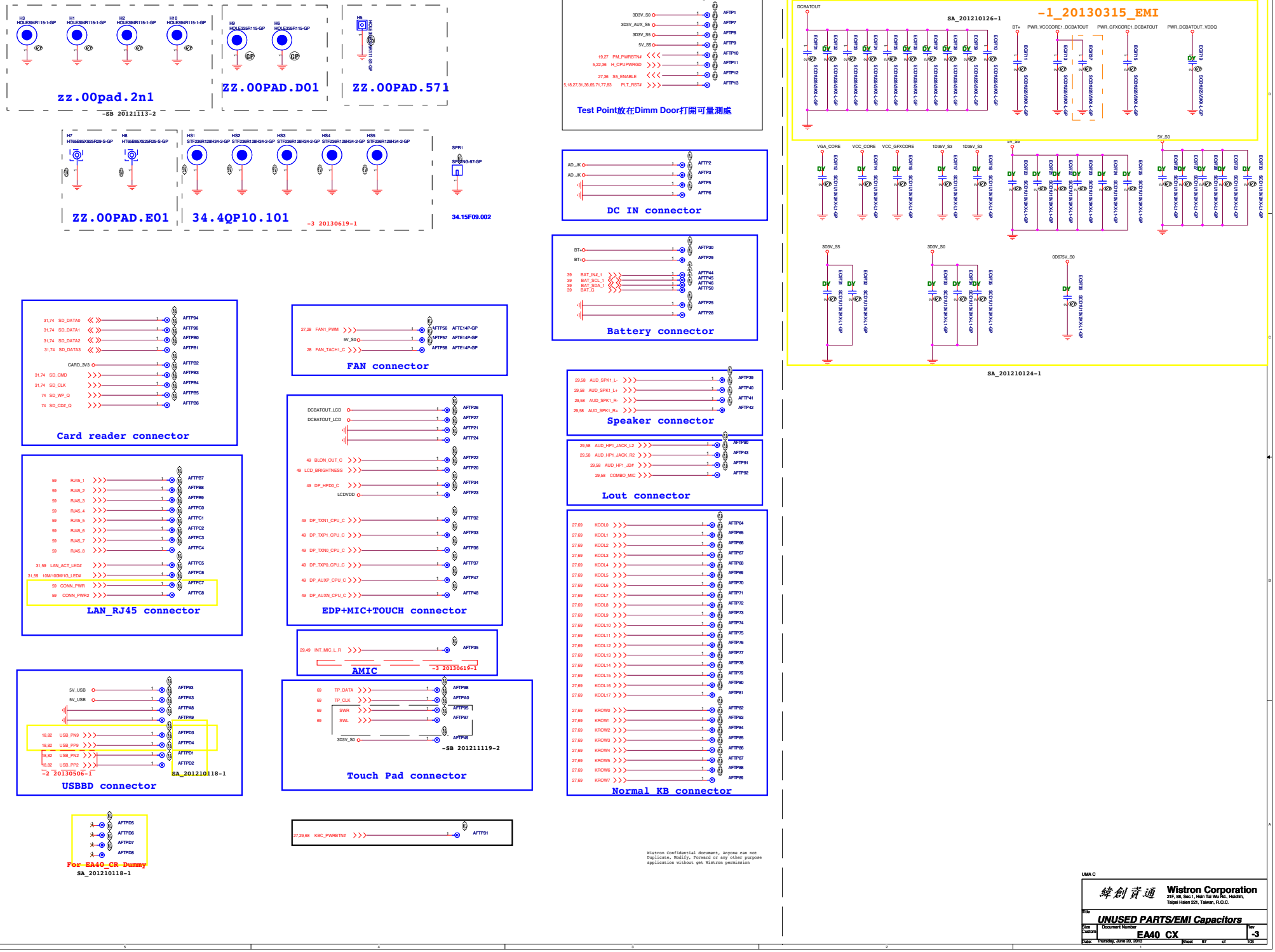
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ZZ.00PAD.D01
ZZ.00PAD.571
ZZ.00PAD.E01
34.4QP10.101
-3 20130619-1
34.15F09.002
Check test point
Test Point放在Dimm Door打開可量測處
DC IN connector
Battery connector
FAN connector
Card reader connector
LAN_RJ45 connector
EDP+MIC+TOUCH connector
Speaker connector
Lout connector
AMIC
Normal KB connector
USBBD connector
-2 20130506-1
SA_201210118-1
Touch Pad connector
-SB 201211119-2
For EA40_CR Dummy
SA_201210118-1
SA_201210126-1
-1_20130315_EMI
SA_201210124-1
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Title
UNUSED PARTS/EMI Capacitors
Size
Custom
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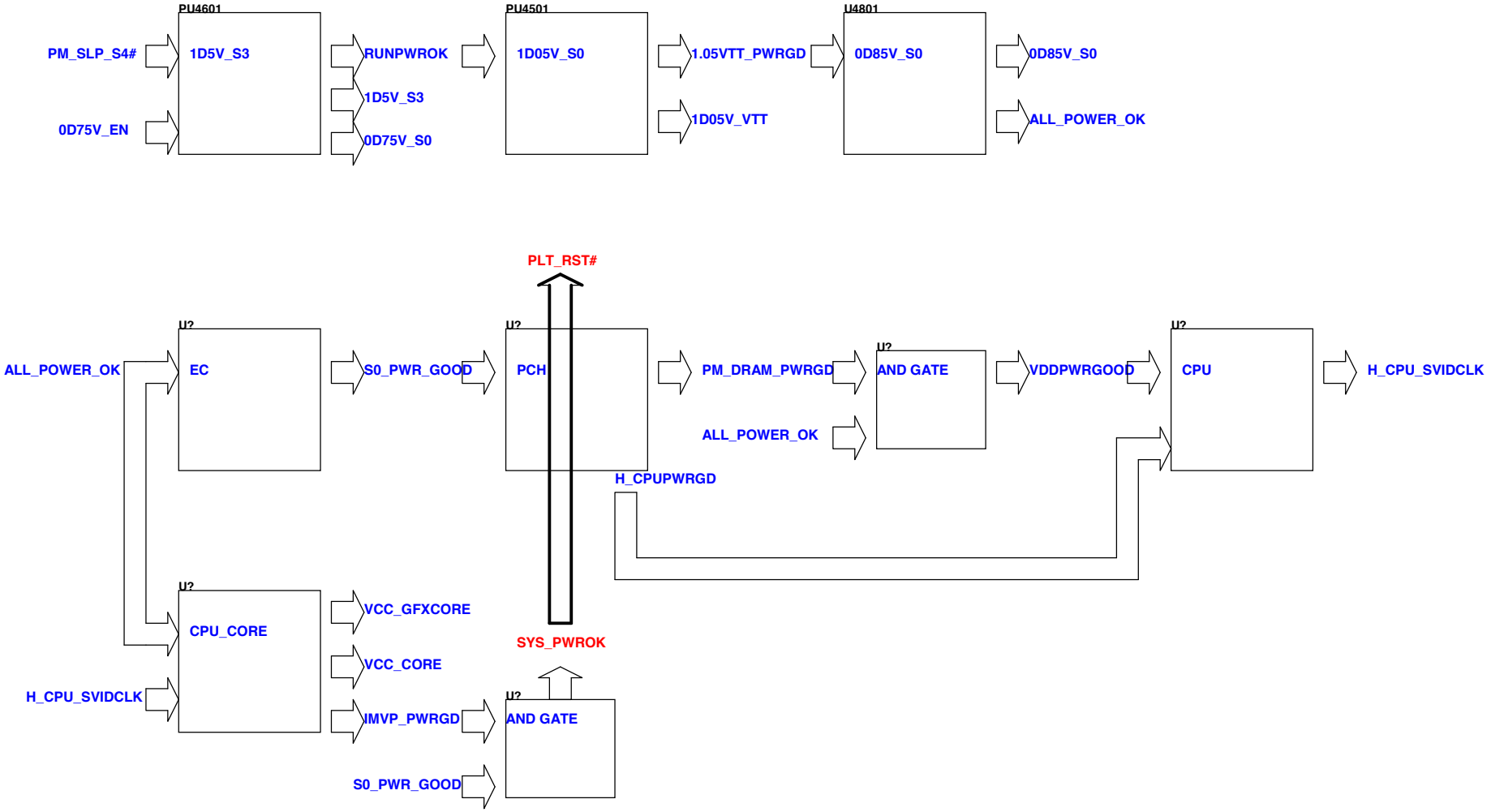
Power Sequence



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Title: Change History

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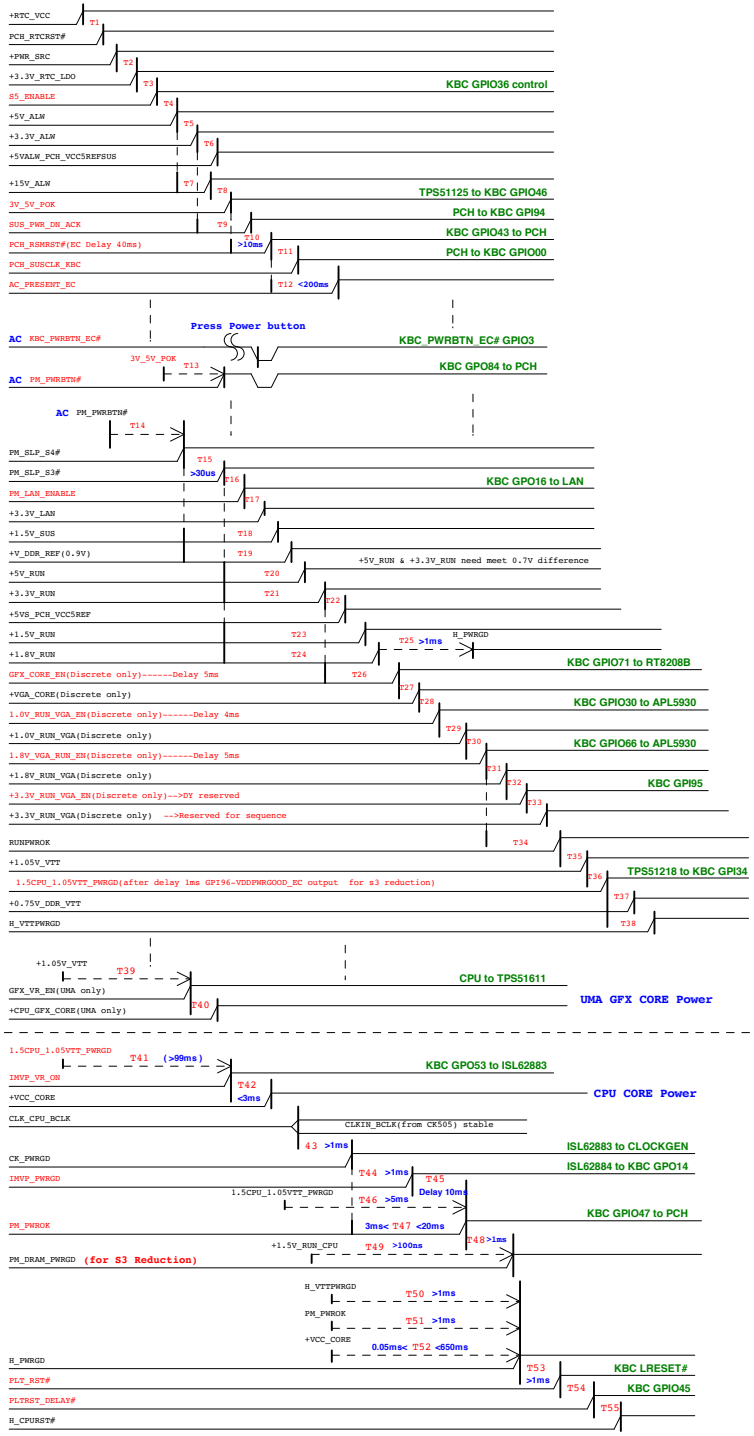
Intel-Power Up Sequence

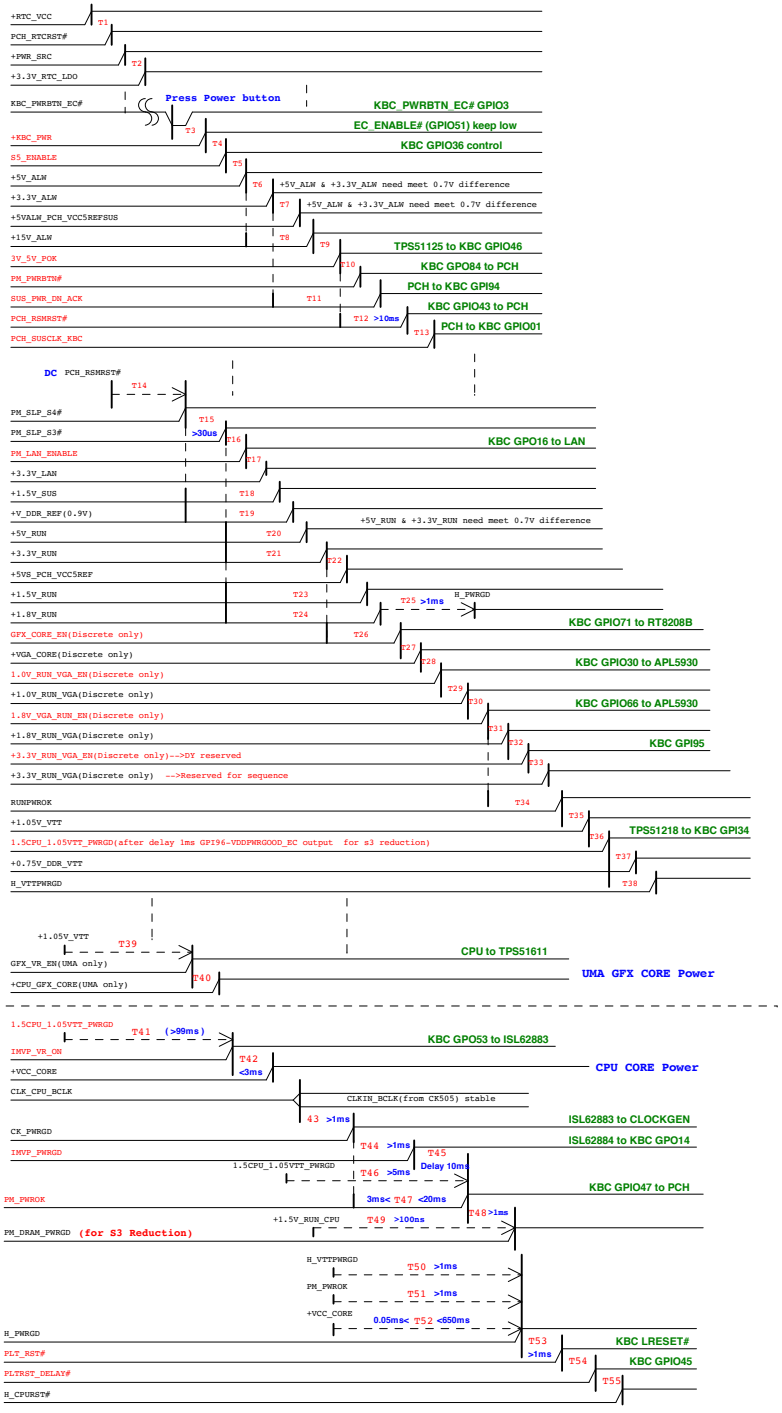
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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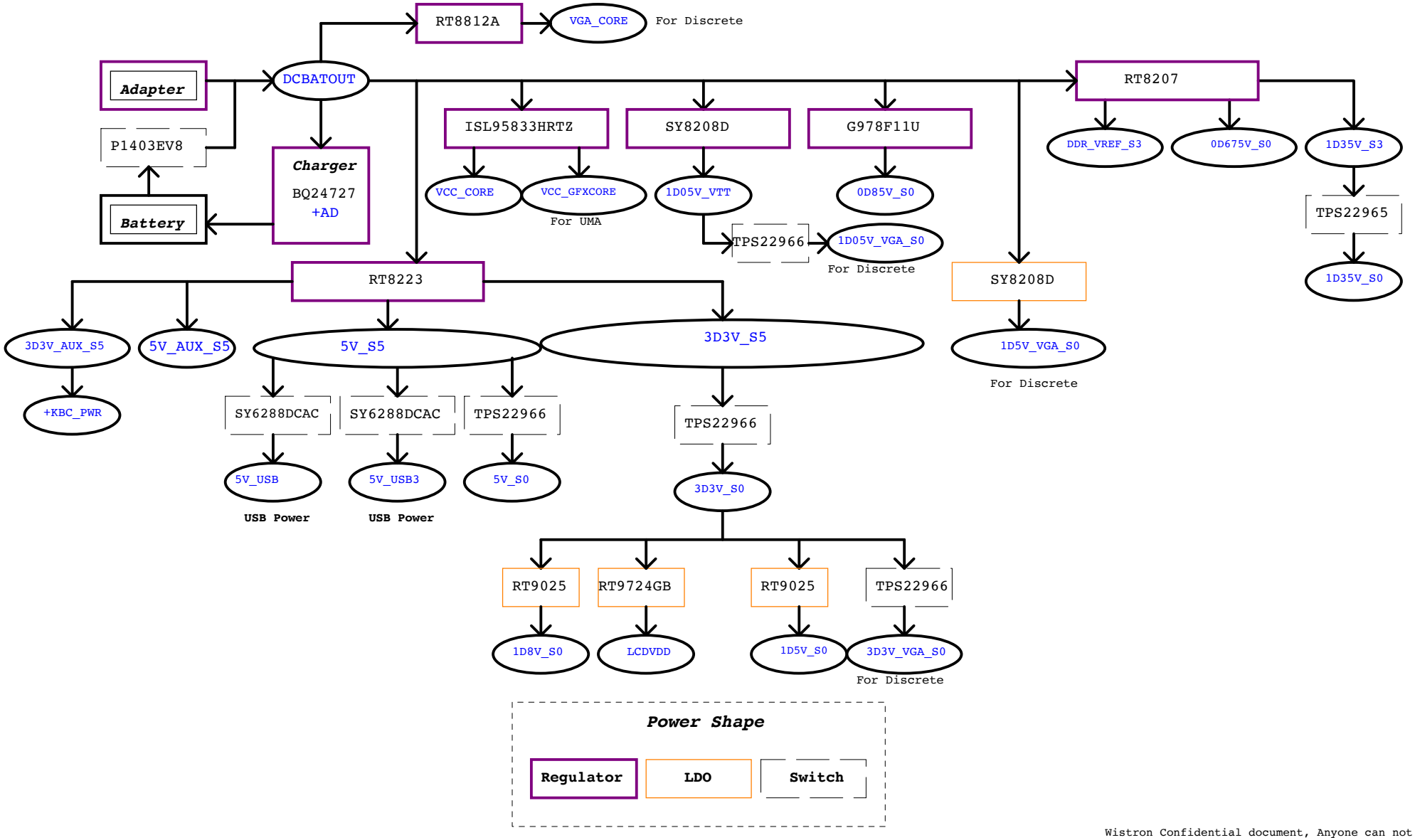
Title: Power Sequence

Size: M | Document Number: EA40_CX | Rev: -3

Date: Thursday, June 05, 2008 | Sheet 39 of 55



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Title: **Power Block Diagram**

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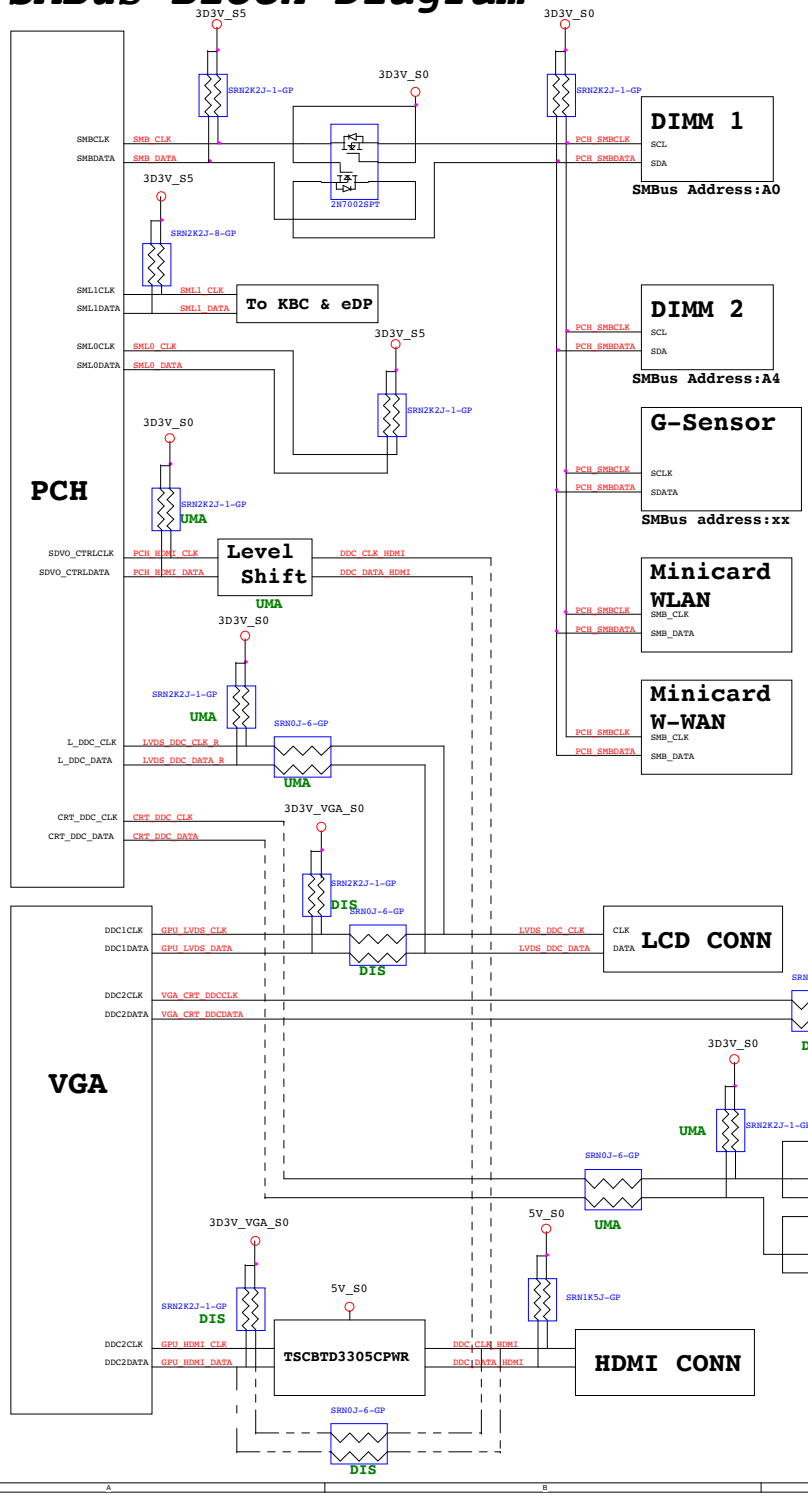
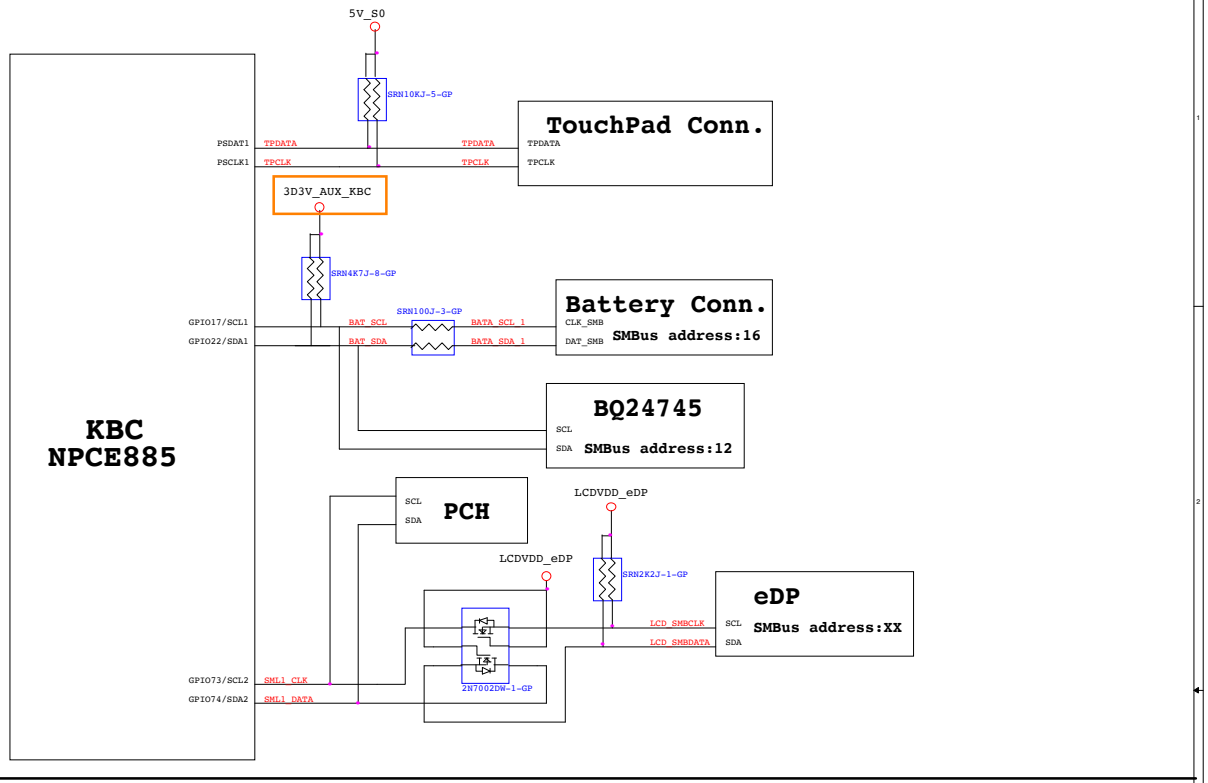
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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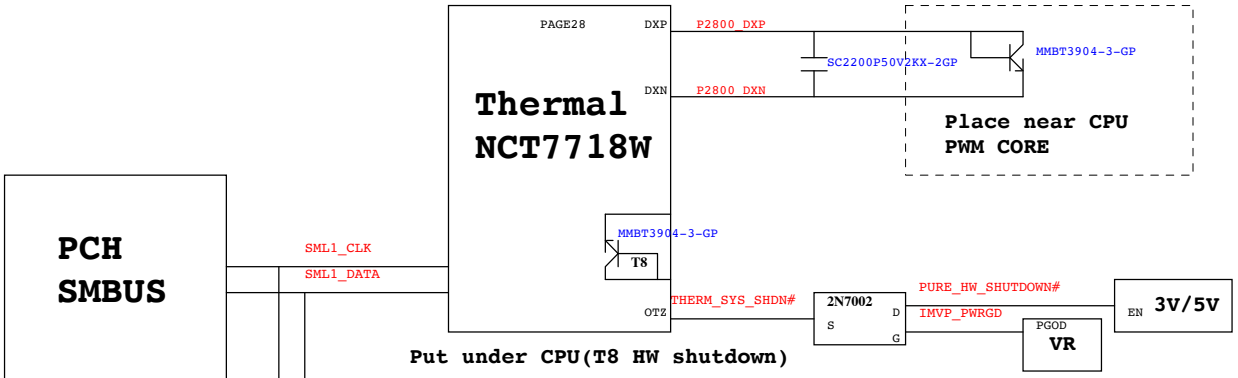
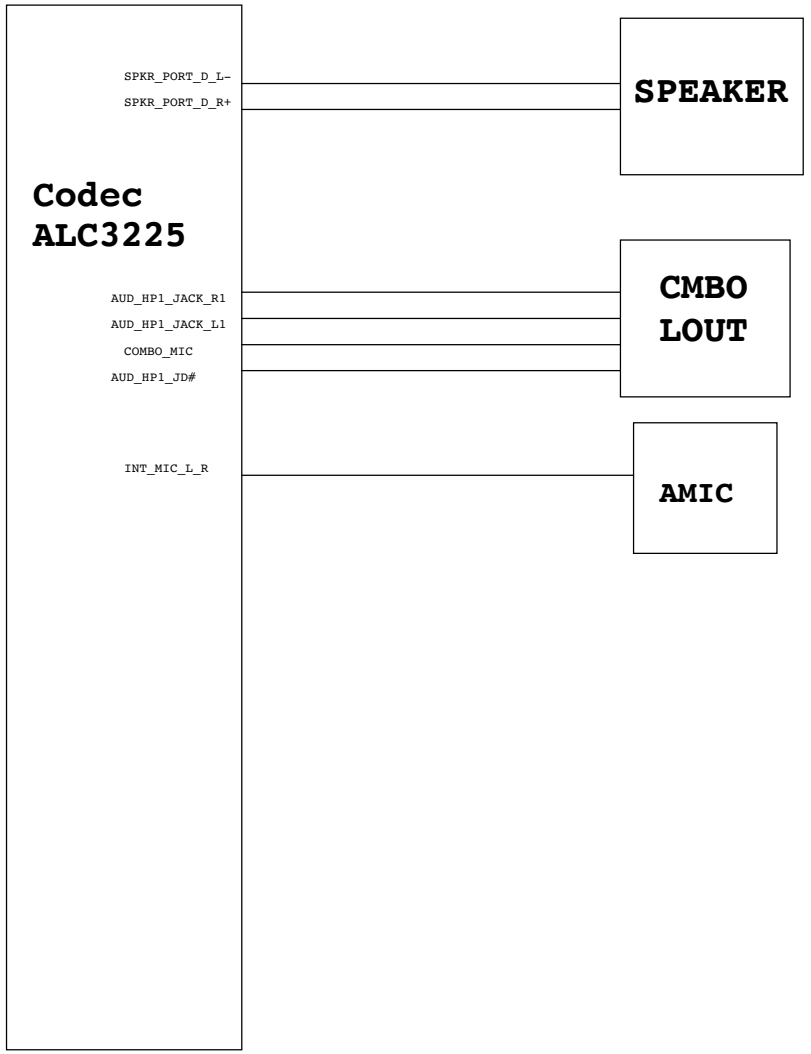
Thermal Block Diagram



Audio Block Diagram



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