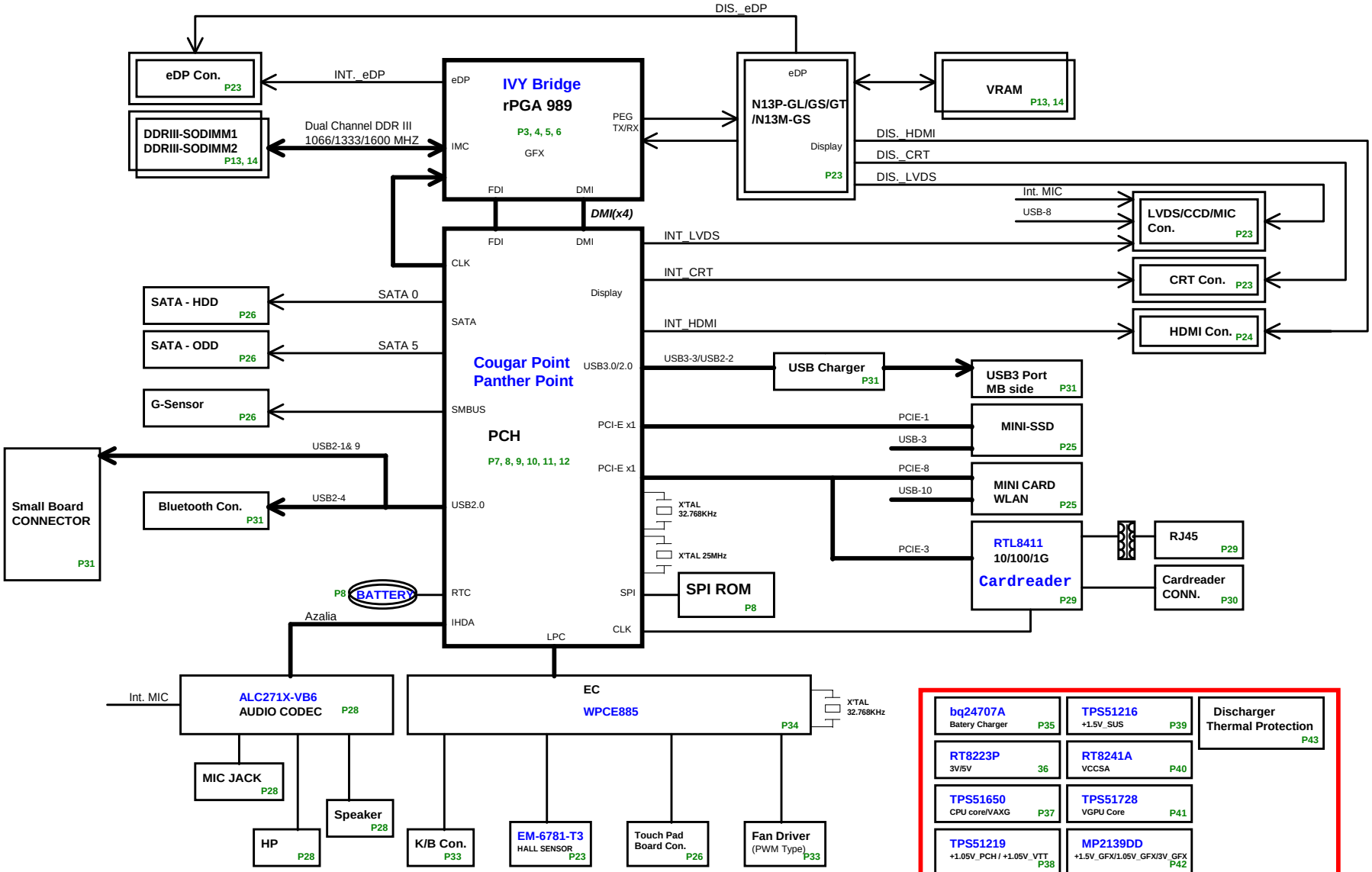
ZQT/ZQS/ZQW CRV SYSTEM BLOCK DIAGRAM



Quanta Computer Inc.

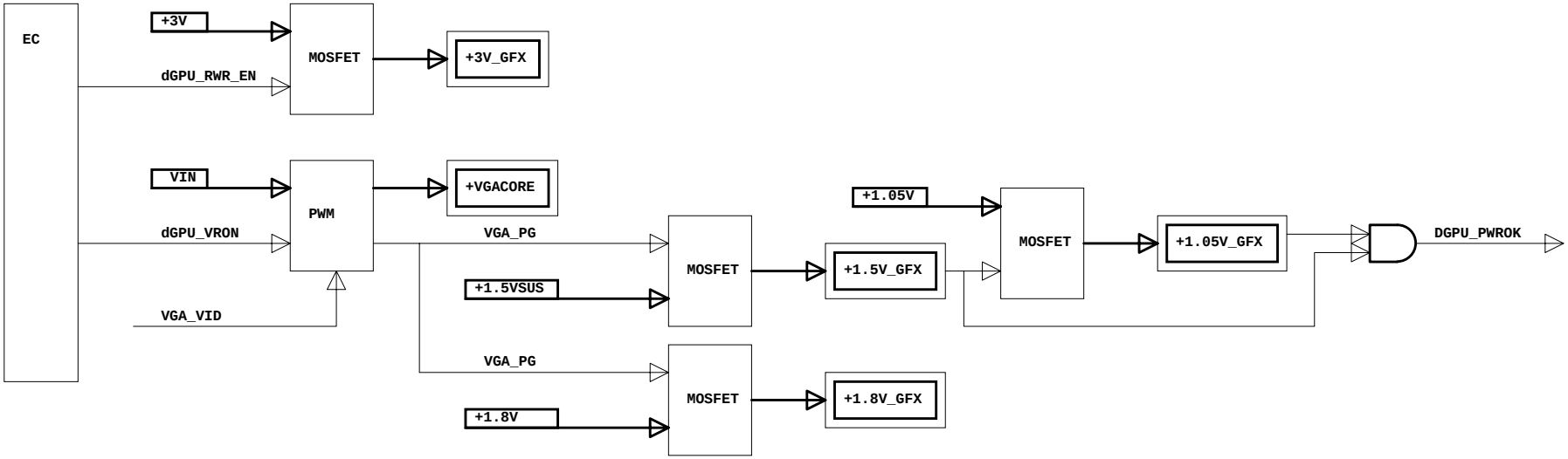
PROJECT : ZQS 45W

Block Diagram

Size | Document Number | Rev 3C

Date: Wednesday, February 08, 2012 | Sheet 1 of 46

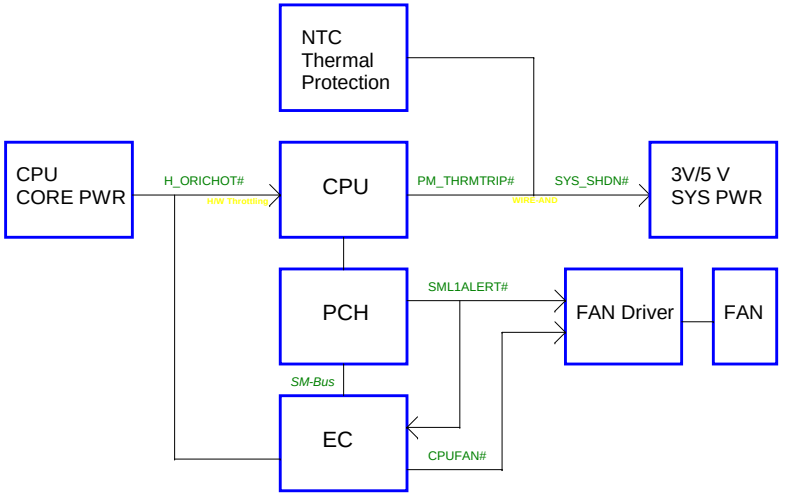
VGA power up sequence



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	VRON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER/IVY/SNB bridge VCCIO	MAINON	S0
+VCCSA	+0.9V	CPU POWER	HWPG_VTT	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
			MAINON	S0

Thermal Follow Chart



Quanta Computer Inc.

PROJECT : ZQS 45W

Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	3C

Date: Wednesday, February 08, 2012 Sheet 2 of 46

IVY Bridge Processor (DMI,PEG,FDI)

For Sandy Bridge processor only implementation:
PROC_SELECT can be left NC.

For IVY/Sandy processor compatibility:
Needs a pull-up resistor to PCH VccDFTERM rail (1.8V) through a 2.2 K±5% pull-up resistor.
Connect to the DF_TVS of PCH though a 1K±5% series resistor.

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

DIS.VGA-->EV@ + EOP@
Optimize-->IOP@ + EOP@
UMA-->IV@ + IOP@
Special-->SP@

Ivy Bridge_rPGA_2DPC_Rev0p61

HPD disable
This signal can be left as no connect if entire eDP interface is disabled.

DG 1.0 :
The recommended AC cap value is changed to 220nF for compatibility with PCIe Gen3 on future platforms.
For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.

N13P-GS--->Gen2

IVY Bridge Processor (CLK,MISC,JTAG)

iGPU wo eDP and dGPU
Connect DPLL_REF_SSCLK on Processor to GND through 1K ± 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K ± 5% resistor

Intel recommended UNCOREPWRGOOD routing on one layer

apply C5205 for nosie

CRB 1.0 : SM_RCOMP[2..0] W:20mils, S:15mils, L 500mils

	EV	UMA/OPT.
Ra	NA	0 ohm
Rb	1K	NA
Rc	1K	NA

For XDP

CRB 1.0 : change to +3V(S0)

Ivy Bridge_rPGA_2DPC_Rev0p61

FDI Disabling (Discrete Only)

C29 Reserve FDI Disabling (Discrete Only), add R665,R666,R667,R668,R669. 1/13

1/13 add

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

DP & PEG Compensation

Routed within 25 mils

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Routed within 500 mils

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

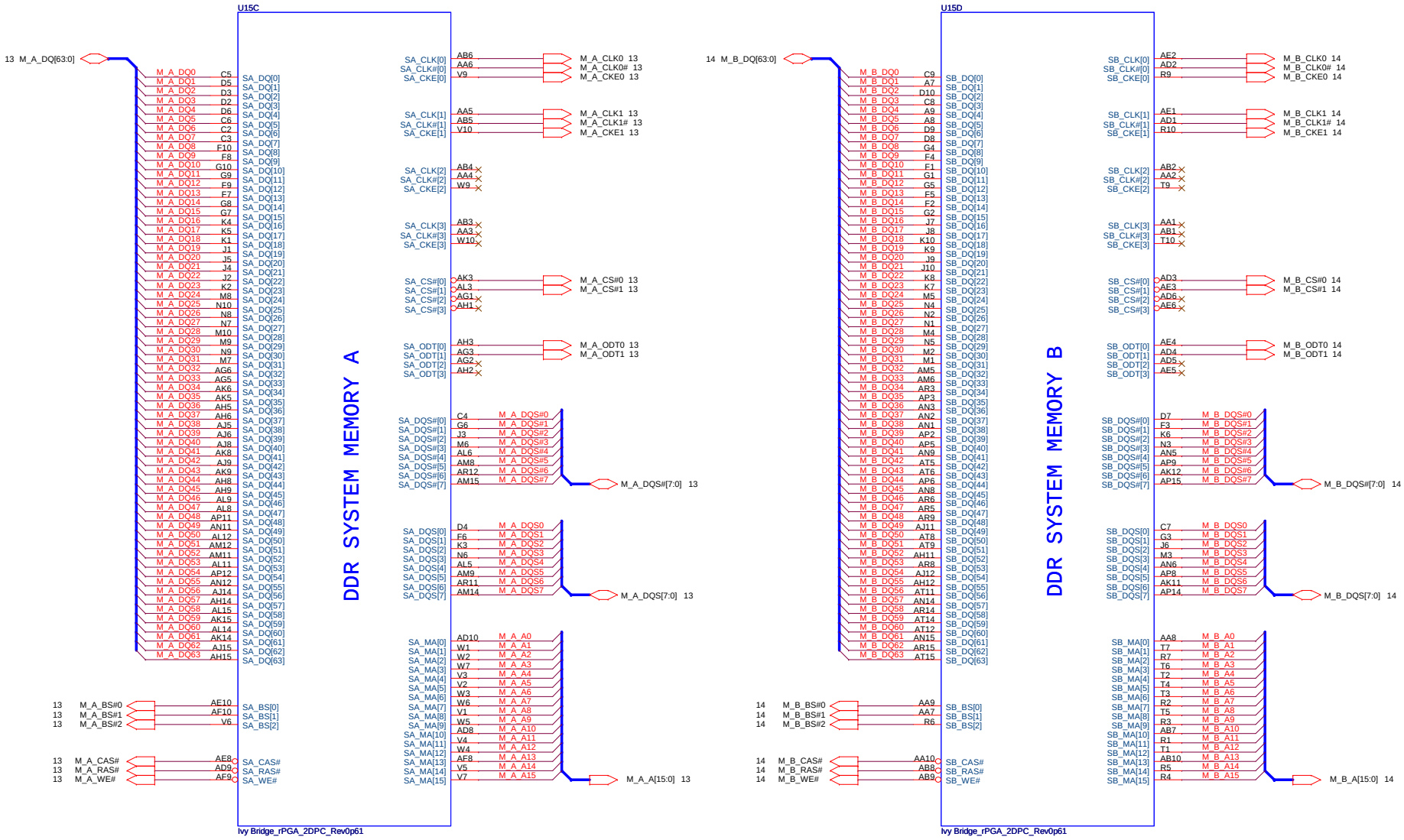
Processor pull-up(CPU)

Quanta Computer Inc.
PROJECT : ZQS 45W

Size	Document Number	Rev
	IVY Bridge 1/4	3C

Date: Wednesday, February 08, 2012 Sheet 3 of 46

IVY Bridge Processor (DDR3)



Quanta Computer Inc.	
PROJECT : ZQS 45W	
Size	Document Number: IVY Bridge 2/4 — Rev: 3C
Date: Wednesday, February 08, 2012	Sheet 4 of 46

IVY Processor (POWER)

IVY Bridge Processor (GRAPHIC POWER)

3,7,8,9,11,23,34,37,38,42,43,46 +1.05V
37,45,46 +VCC_CORE
8,11,43,46 +1.8V
37,45 +VCC_GFX

15 +1.5V_CPU
15 +VDDR_REF_CPU

40 +VCCSA

CPU Core Power
IVY 45W:TDC 52A

IVY SPEC
22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4
total : 10uF x 10 , RSVD x 1
total : 22uF x 16 , RSVD x 3
tatal : 470u x 4, RSVD x2

SNB : Spec	Cose down
470uF/4mohm x 4	330uF x2
22uF x 16	22uF x 4
10uF x 10	10uF x 20 reserved x 5

CPU VTT
IVY 45W:8.5A

SNB : Spec	Cose down
330uF/6mohm x 2	330uF x1
22uF x 12	22uF x 2
22uF x 7 (Non-stuff)	10uF x 10 reserved x 4

CPU VGT
IVY 45W:TDC 38A

Spec	Cose down
470uF/4mohm x 2	330uF x1
22uF x 12	22uF x 4
	10uF x 10

IVY SPEC
22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

U15F

POWER

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

U15G

POWER

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

1.8V RAIL

MISC

GRAPHICS

+VCC_CORE

+1.05V

+VCC_GFX

+1.8V

+1.5V_CPU

+VCCSA

IVY SPEC
22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

DIS.VGA-->EV@ + EOP@
Optimus-->IOP@ + EOP@
UMA-->IV@ + IOP@
Ssecial-->SP@

	DIS. VGA	UMA/ Optimus
Ra	0 ohm	NA

CPU VCCPL
IVY 45W:1.5A

Spec	Real
330uF/7mohm x 1	10uF x 1
10uF x 1	1uF x 2
1uF x 2	

IVY SPEC
330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

10uF (Reserved)

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
Remove PU resistor 54.9/F, stuff at IMVP7 page

SVID DATA
Remove PU resistor 130/F, stuff at IMVP7 page

SVID ALERT

Place PU resistor close to CPU

Trace Route to Power IC area.

10 mil

For M3 solution need Rb4, Rd1 W/O M3 then NC ball B4 and D1

IVY SPEC
330uF x1, 10uF_8 x6 Socket BOT edge.

Voltage selection for VCCIO:
this pin must be pulled high on the motherboard

On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V

IVY SPEC
330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

CPU SA
IVY 45W: 6A

Spec	Real
330uF/7mohm x 1	10uF x 3
10uF x 3	

CPU MCH
IVY 45W: 5A

Spec	
330uF/6mohm x 1	
10uF x 6	
Real	
10uF x 8	

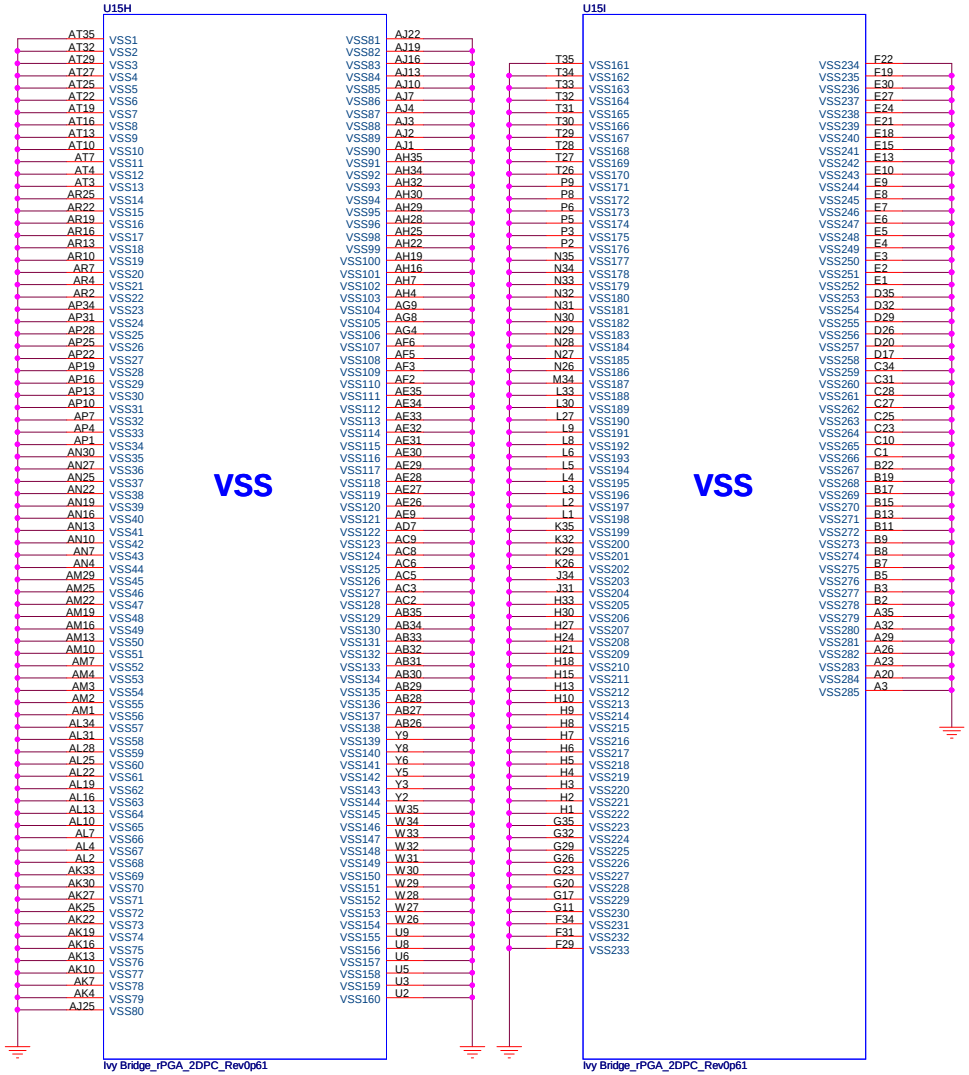
Ivy Bridge_rPGA_2DPC_Rev0p61

Quanta Computer Inc.
PROJECT : ZQS 45W

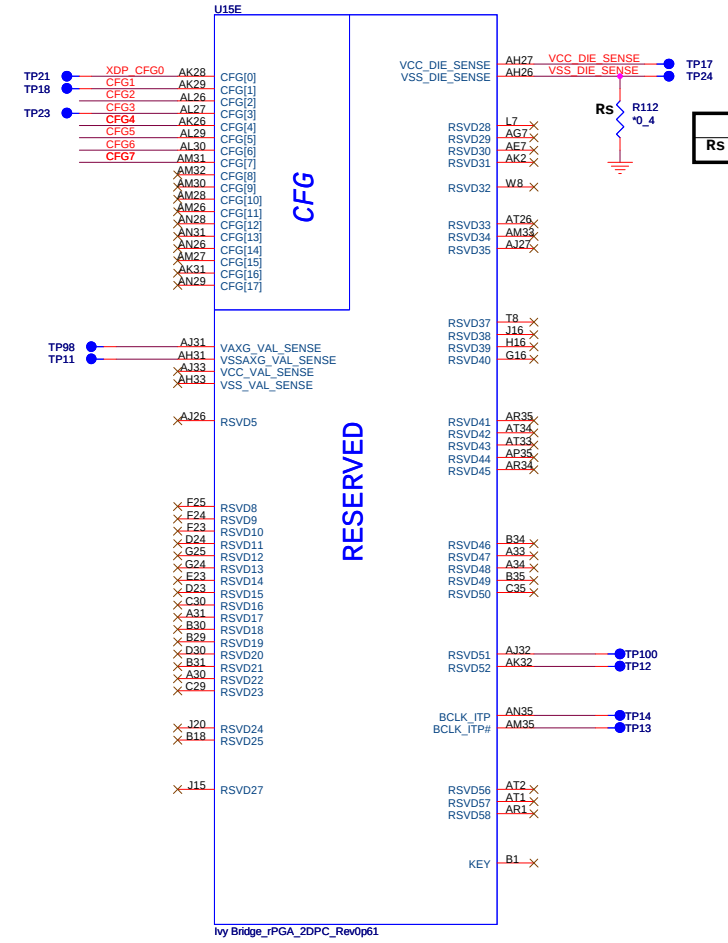
Size	Document Number	Rev
	IVY Bridge 3/4	3C

Date: Wednesday, February 08, 2012 Sheet 5 of 46

IVY Bridge Processor (GND)



IVY Bridge Processor (RESERVED, CFG)



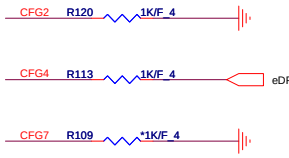
06

	For Sandy	For IVY
Rs	Stuff	NC

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	**Lane Reversed**
CFG4 (DP Presence Strap)	**Disable; No physical DP attached to eDP**	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	**PEG train immediately following xxRESETB de assertion**	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

CFG5 R110 *1K/F_4
CFG6 R108 *1K/F_4

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Quanta Computer Inc.
PROJECT : ZQS 45W

Size	Document Number	Rev
	IVY Bridge 4/4	3C

Date: Wednesday, February 08, 2012 Sheet 6 of 46

3,5,8,9,11,23,34,37,38,42,43,46 +1.05V
3,24,25,26,27,29,33,34,36,37,38,39,40,41,42,43,45,46 +3V
8,9,10,11,15,16,29,31,33,36,37,38,43,44 +3V_S5
34 DPWROK_EC

DPWROK_EC

CPT/PPT (DMI,FDI,PM)

U21C

DMI: DMI0RXN, DMI1RXN, DMI2RXN, DMI3RXN, DMI0RXP, DMI1RXP, DMI2RXP, DMI3RXP, DMI0TXN, DMI1TXN, DMI2TXN, DMI3TXN, DMI0TXP, DMI1TXP, DMI2TXP, DMI3TXP, DMI_ZCOMP, DMI_IRCOMP, DMI2RBIAS

FDI: FDI_RXN0 BJ14, FDI_RXN1 AY14, FDI_RXN2 BE14, FDI_RXN3 BH13, FDI_RXN4 BC12, FDI_RXN5 BJ12, FDI_RXN6 BG10, FDI_RXN7 BG9; FDI_RXP0 BG14, FDI_RXP1 BB14, FDI_RXP2 BF14, FDI_RXP3 BG13, FDI_RXP4 BE12, FDI_RXP5 BG12, FDI_RXP6 BJ10, FDI_RXP7 BH9; FDI_INT AW16, FDI_FSYNC0 AV12, FDI_FSYNC1 BC10, FDI_LSYNC0 AV14, FDI_LSYNC1 BB10

+1.05V R495 49.9/F_4 DMI_COMP
R499 750/F_4

System Power Management: SUS_PWR_ACK R257 *0_4 SUSACK#_R C12 SUSACK#; XDP_DBRST# K3 SYS_RESET#; SYS_PWROK P12 SYS_PWROK; PWROK L22; APWROK L10; DRAMPWROK B13; RSMRST# C21; SUSWARN#/SUSPWRDNACK/GPIO30 K16; PWRBTN# E20; ACPRESENT / GPIO31 H20; BATLOW# / GPIO72 E10; RI# A10

DSWVRMEN A18 DSWVREN 8

DPWROK F22 — 0_4 *0_4 R220 R646 PCH_RSMRST# DPWROK_EC

WAKE# B9 PCIE_WAKE# PCIE_WAKE# 29

CLKRUN# / GPIO32 N3 CLKRUN# CLKRUN# 34

SUS_STAT# / GPIO61 G8 SUS_STAT# TP129

SUSCLK / GPIO62 N14 PCH_SUSCLK TP127

SLP_S5# / GPIO63 D10 PCH_SLP_S5# TP128

SLP_S4# H4 SUSC# 34

SLP_S3# F4 SUSB# 34

SLP_A# G10 SLP_A# SLP_A# 34

SLP_SUS# G16 SLP_SUS# TP130

PMSYNCH AP14 PM_SYNC 3

SLP_LAN# / GPIO29 K14 SLP_LAN#

C607 *1u/10V_4

SYS_PWROK R559 *SHORT_4 SYS_PWROK_R

R282 *0_4 SBA

PWROK_EC R294 *SHORT_4 R609 @0_4 EC_PWROK_R

C15 Add 0Ω R609 to net EC_PWROK_R. 12/29

15 PM_DRAM_PWRGD PM_DRAM_PWRGD

34 PCH_RSMRST# PCH_RSMRST#

SUS_PWR_ACK

34 DNBSWON#

AC_PRESENT

PM_BATLOW#

PM_RI#

34,44 EC_PWROK_R EC_PWROK_R

C698 *0.1u/10V_4

C35 Reserve 0.1u capacitor C698 to EC_PWROK_R. 01/17

PANTHER POINT

Pin K47 --->LVDS Enable
--->2.2K pull-up 3.3V
Disable ---> No connect

CPT/PPT (LVDS,DDI)

U21D

LVDS: 23 INT_LVDS_BLON J47 L_BKLTEN; 23 INT_LVDS_DIGON M45 L_VDD_EN; 23 INT_LVDS_BRIGHT P45 L_BKLTCTL; 23 INT_LVDS_EDIDCLK T40 L_DDC_CLK; 23 INT_LVDS_EDIDDATA K47 L_DDC_DATA; +3V R176 2.2K_4 R168 2.2K_4 T45 L_CTRL_CLK P39 L_CTRL_DATA; R190 2.37K/F_4 TP126 AF37 LVD_IBG AF36 LVD_VBG AE48 LVD_VREFH AE47 LVD_VREFL

23 INT_TXLCLKOUT- AK39 LVDSA_CLK# 23 INT_TXLCLKOUT+ AK40 LVDSA_CLK

23 INT_TXLOUT0- AN48 LVDSA_DATA#0 23 INT_TXLOUT1- AM47 LVDSA_DATA#1 23 INT_TXLOUT2- AK47 LVDSA_DATA#2 AJ48 LVDSA_DATA#3

23 INT_TXLOUT0+ AN47 LVDSA_DATA0 23 INT_TXLOUT1+ AM49 LVDSA_DATA1 23 INT_TXLOUT2+ AK49 LVDSA_DATA2 AJ47 LVDSA_DATA3

AF40 LVDSB_CLK# AF39 LVDSB_CLK

AH45 LVDSB_DATA#0 AH47 LVDSB_DATA#1 AF49 LVDSB_DATA#2 AF45 LVDSB_DATA#3

AH43 LVDSB_DATA0 AH49 LVDSB_DATA1 AF47 LVDSB_DATA2 AF43 LVDSB_DATA3

CRT: 23 INT_CRT_BLU N48 CRT_BLUE; 23 INT_CRT_GRN P49 CRT_GREEN; 23 INT_CRT_RED T49 CRT_RED; 23 INT_CRT_DDCCLK T39 CRT_DDC_CLK; 23 INT_CRT_DDCDAT M40 CRT_DDC_DATA

INT_CRT_BLU INT_CRT_GRN INT_CRT_RED

23 INT_HSYNC R445 IOP@33_4 INT_CRT_HSYNC_R M47 CRT_HSYNC
23 INT_VSYNC R446 IOP@33_4 INT_CRT_VSYNC_R M49 CRT_VSYNC

DAC_IREF T43 DAC_IREF; T42 CRT_IRTN

R179 IOP@1K/F_4

PANTHER POINT

Digital Display Interface

SDVO_TVCLKINN AP43, SDVO_TVCLKINP AP45
SDVO_STALLN AM42, SDVO_STALLP AM43
SDVO_INTN AP39, SDVO_INTP AP40
SDVO_CTRLCLK P38, SDVO_CTRLDATA M39

DDPB_AUXN AT49, DDPB_AUXP AT47, DDPB_HPD AT40
DDPB_0N AV42, DDPB_0P AV40, DDPB_1N AV45, DDPB_1P AV46, DDPB_2N AU48, DDPB_2P AU47, DDPB_3N AV47, DDPB_3P AV49

DDPC_CTRLCLK P46, DDPC_CTRLDATA P42
DDPC_AUXN AP47, DDPC_AUXP AP49, DDPC_HPD AT38
DDPC_0N AY47, DDPC_0P AY49, DDPC_1N AY43, DDPC_1P AY45, DDPC_2N BA47, DDPC_2P BA48, DDPC_3N BB47, DDPC_3P BB49

DDPD_CTRLCLK M43, DDPD_CTRLDATA M36
DDPD_AUXN AT45, DDPD_AUXP AT43, DDPD_HPD BH41
DDPD_0N BB43, DDPD_0P BB45, DDPD_1N BF44, DDPD_1P BE44, DDPD_2N BF43, DDPD_2P BE42, DDPD_3N BJ42, DDPD_3P BG42

INT. HDMI: HDMI_DDCCLK_SW 24, HDMI_DDCDATA_SW 24, HDMI_HP 24, INT_HDMITX2N 24, INT_HDMITX2P 24, INT_HDMITX1N 24, INT_HDMITX1P 24, INT_HDMITX0N 24, INT_HDMITX0P 24, INT_HDMICLK- 24, INT_HDMICLK+ 24

DDPC_HPD_PU, DDPD_HPD_PU

Pin M39 ---> Enable
--->2.2K pull-up 3.3V

Pin P42 ---> Enable
--->2.2K pull-up 3.3V

DDPC_HPD_PU R153 *2.2K_4
DDPD_HPD_PU R158 *2.2K_4
Follow PDG DP disable guide

Pin M36 ---> Enable
--->2.2K pull-up 3.3V

C22 Change R220 from shortpad to 0Ω, reserve 0Ω R646 connect to DPWROK_EC. 01/05

The required series-resistors are:
- Direct Connect - 33 Ω
- Docking Topology - 20 Ω

R place close to PCH
R451 IOP@150/F_4 INT_CRT_BLU
R452 IOP@150/F_4 INT_CRT_GRN
R453 IOP@150/F_4 INT_CRT_RED

PCH Pull-high/low(CLG)

+3V
CLKRUN# R535 8.2K_4
XDP_DBRST# R543 4.99K/F_4
R533 *1K_4
PCH_RSMRST# R221 10K_4
SYS_PWROK R558 *10K_4

+3V_S5
PM_RI# R552 10K_4
PM_BATLOW# R286 8.2K_4
PCIE_WAKE# R530 10K_4
SLP_LAN# R260 *10K_4
SUS_PWR_ACK R251 10K_4
AC_PRESENT R219 10K_4
PM_DRAM_PWRGD R507 200/F_4
wo S3 leakage, remove R

System PWR_OK(CLG)

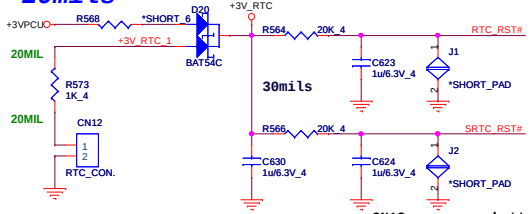
IMVP_PWRGD PU +3V
PWROK_EC PD
so AND gate output dont need PD again

+3V_S5
C651 *0.1u/10V_4
to PCH Pin12, XDP and EE debug
15 SYS_PWROK SYS_PWROK 4
U24 TC7SH08FU
2 IMVP_PWRGD 3,37
1 PWROK_EC PWROK_EC 34
R572 100K_4

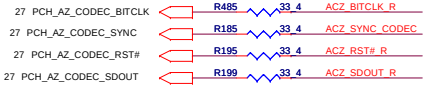
Quanta Computer Inc.
PROJECT : ZQS 45W

Size	Document Number	Rev
	Panther Point 1/6	3C
Date: Wednesday, February 08, 2012	Sheet 7 of 46	

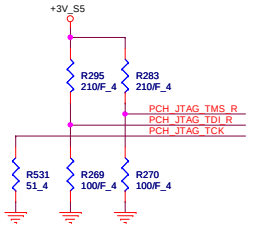
RTC Circuitry(RTC)



HDA Bus(CLG)

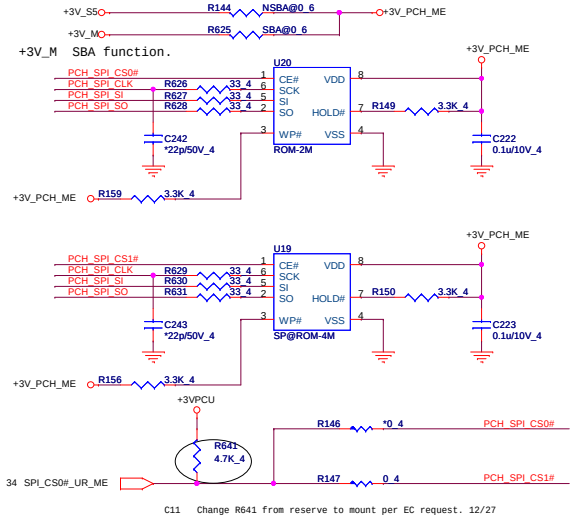


PCH JTAG Debug (CLG)



PCH Dual SPI (CLG) (Default for WIN8)

W25Q64BVSSIG / AKE3EFP0N00------>8MB
W25Q32BVSSIG / AKE391P0N00------>4MB
W25Q16BVSSIG / AKE38FP0N01----->

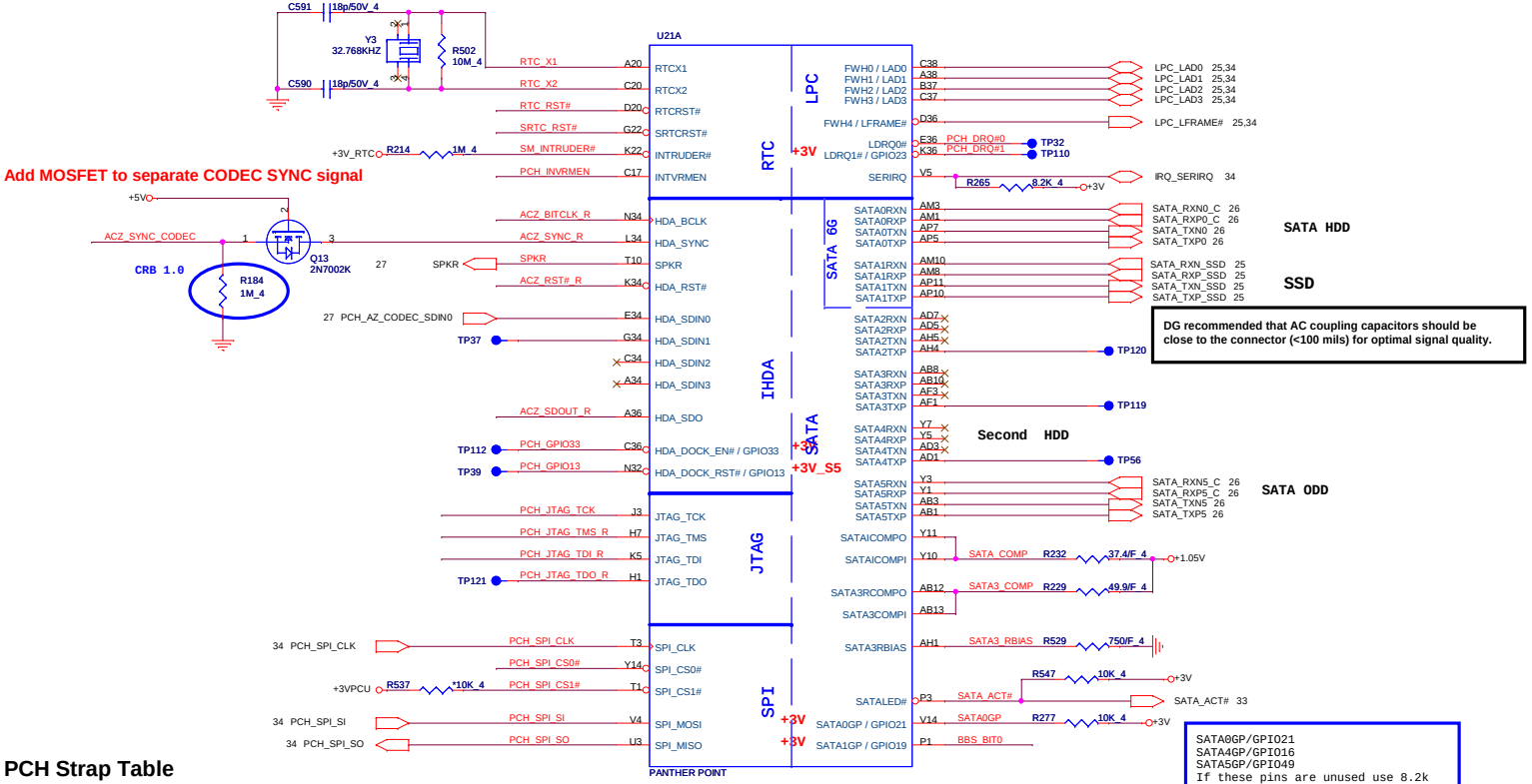


11,23,25,26,31,33,34,35,36,43,44,46 +3VPCU
11,23,24,26,27,33,36,43,46 +5V
7,9,10,11,15,16,29,31,33,36,37,38,43,44 +3V_S5

3,5,7,9,11,23,34,37,38,42,43,46 +1.05V
25,26,27,29,33,34,36,37,38,39,40,41,42,43,45,46 +3V
5,11,43,46 +1.8V

PCH2(CLG)

CPT/PPT (HDA,JTAG,SATA)

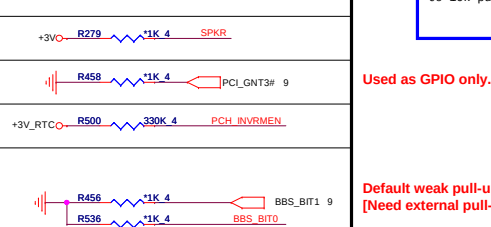


DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

SATA0GP/GPIO21
SATA4GP/GPIO16
SATA5GP/GPIO49
If these pins are unused use 8.2k to 10k pull-up to +Vcc3_3 or 8.2k to 10k pull-down to ground

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = effect (default)(weak pull-down 20K) 1 = overridden
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Disable (Default) 1 = Enable
DSWVREN	DEEP S4/S5 well On Die DSW VR Enable	DSW	High = Enable (Default) Low = Disable
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)



Used as GPIO only. at chklist 1.2

Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

ME_WR default EC setting folating

for future CPU, Sandy Bridge NC
DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhm ±5% - R8361 change to 0 or not??

Needs to be pulled High for Huron River platform. chklist 1.2

Quanta Computer Inc.
PROJECT : ZQS 45W

Size	Document Number	Rev
	Panther Point 2/6	3C

Date: Wednesday, February 08, 2012 Sheet 8 of 46

CPT/PPT (PCI,USB,NVRAM)

CPT/PPT (PCI-E,SMBUS,CLK)

TX AC cap place at connector side, AC cap to connector < 400mils

USB3.0

Port1 and port9 can be used on debug mode

XHCI for USBP0-3

EHCI1

EHCI2

Reserve for USB I/O function

USB/B-USB1-1/USB debug

MB USB

Mini-SSD

BLUETOOTH

Reserve for SIM card

USB port6Y may not be available on all PCH sku (HM55 support 12port only)

Camera

USB/B-USB1-2

MINI-CARD WLAN(MPC)

Reserve for card reader

Reserve for Touch pad

Reserve for FP

LAN

Wireless

Wireless

LAN

For XDP

For LAN

For EC

PANTHER POINT

PANTHER POINT

PLTRST#(CLG)

C38 Change U22 PLTRST# power source from +3V_S5 to +3V. 01/17

U22 TC7SH08FU

C622 0.1u/10V_4

R551 100K_4

PCI/USBOC# Pull-up(CLG)

R505 10K_10P8R

R541 10K_4

R467 10K_10P8R

	dGPU_PW_CTRL# (GPIO68) CTL : dGPU_VRON	SKU_ID1 (GPIO64)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
dGPU Only	0	0	1	GPU	Hidden	GPU boot
Switchable (Mux)				UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

dGPU_PW_CTRL#
1 = GPU power is control by H/W (pure Discrete SKU)
0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)
--->(Default)

CLK_REQ/Strap Pin(CLG)

Pull-up in N13P side

CLOCK TERMINATION for FCIM

SMBus(EC)

SMBus(PCH)

Q15 2N7002K

Q16 2N7002K

Q14 2N7002K

Q17 2N7002K

S5

S0

Quanta Computer Inc.		
PROJECT : ZQS 45W		
Size	Document Number: Panther Point 3/6	Rev: 3C
Date: Wednesday, February 08, 2012	Sheet 9 of 46	

CPT/PPT (GPIO,VSS_NCTF,RSVD)

U21F

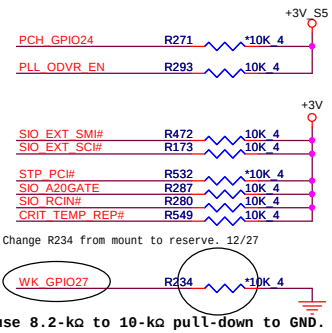
PANTHER POINT

GPIO

CPU/MISC

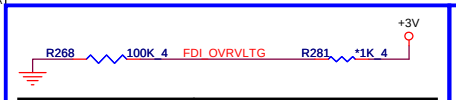
NCTF

GPIO Pull-up/Pull-down(CLG)

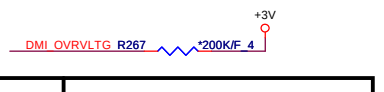


GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

SATA2GP : strap for reserved at chklist 1.2
SATA3GP : strap for reserved at chklist 1.2
NOTE: The internal pull-down is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled high when strap is sampled.

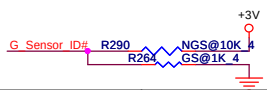


FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage



DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

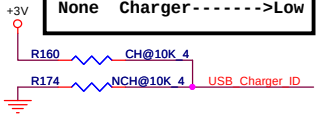
Change BIO_REC to G_Sensor_ID# 10/21
Change MB ID for G-sensor
PCH GPIO22
Pull high=no G-Sensor
Pull low=have G-Sensor



G Sensor ID	High = Disable (Default) Low = Enable

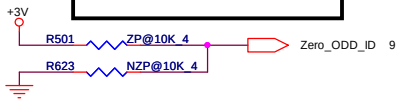
USB_Charger_ID

USB Charger------->High
None Charger------->Low



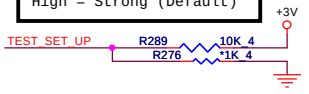
Zero ODD ID

Zero ODD------->High
None Zero ODD------->Low

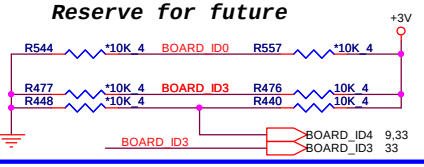


SV_SET_UP

High = Strong (Default)



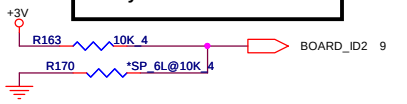
Reserve for future



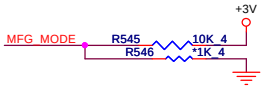
SGPIO

BOARD_ID2

8 Layer ------->High *
6 Layer ------->Low



MFG-TEST

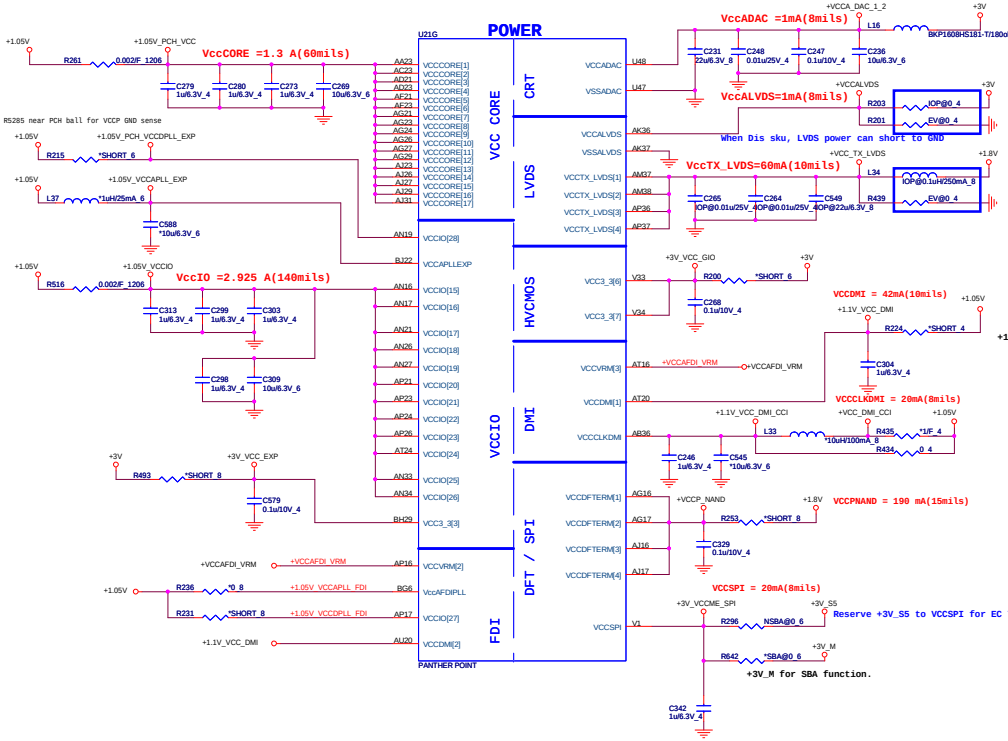


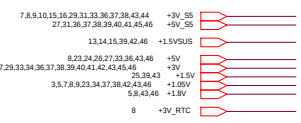
Quanta Computer Inc.
PROJECT : ZQS 45W

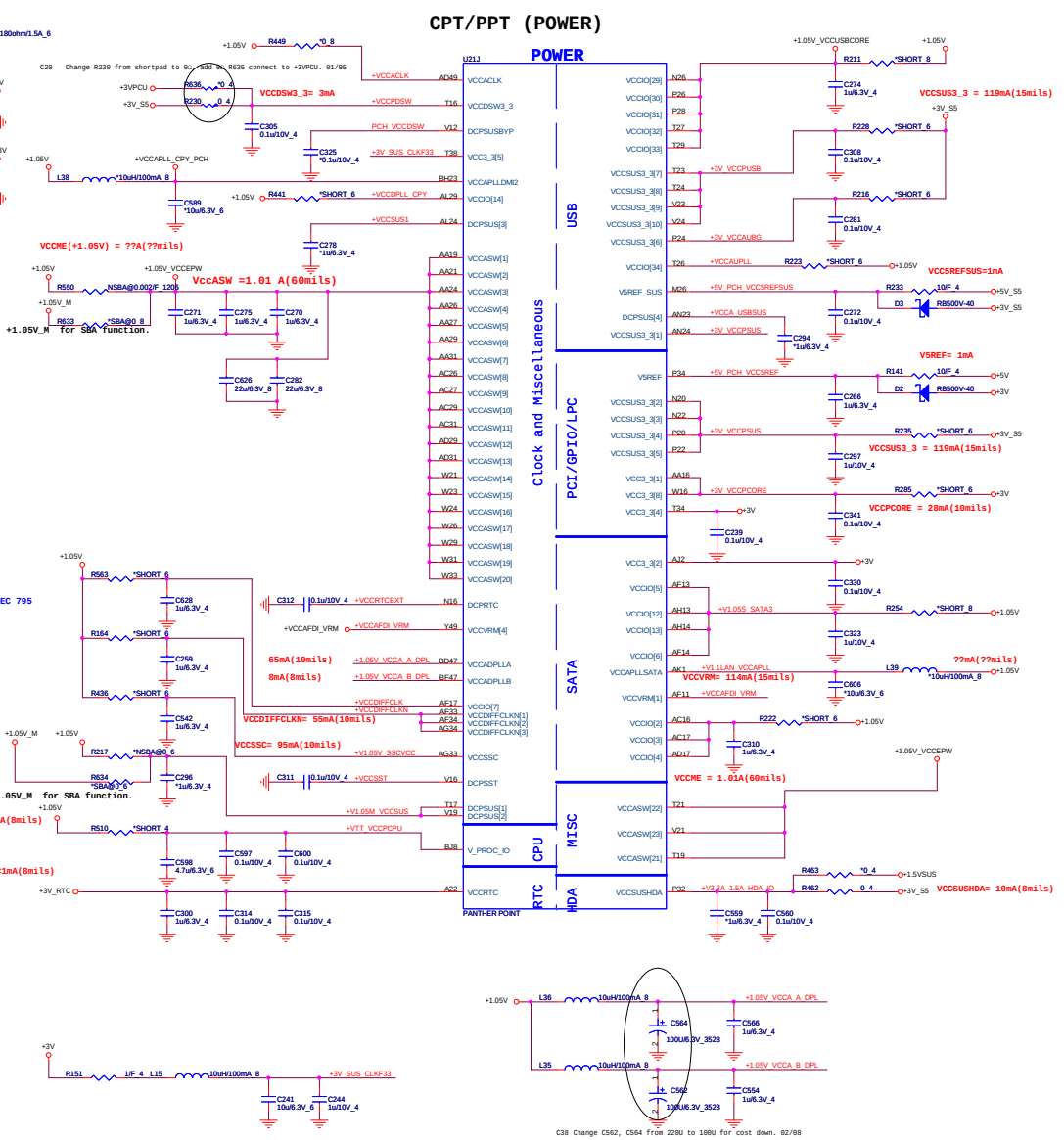
Size	Document Number	Rev
	Panther Point 4/6	3C

Date: Wednesday, February 08, 2012 Sheet 10 of 46

CPT/PPT (POWER)



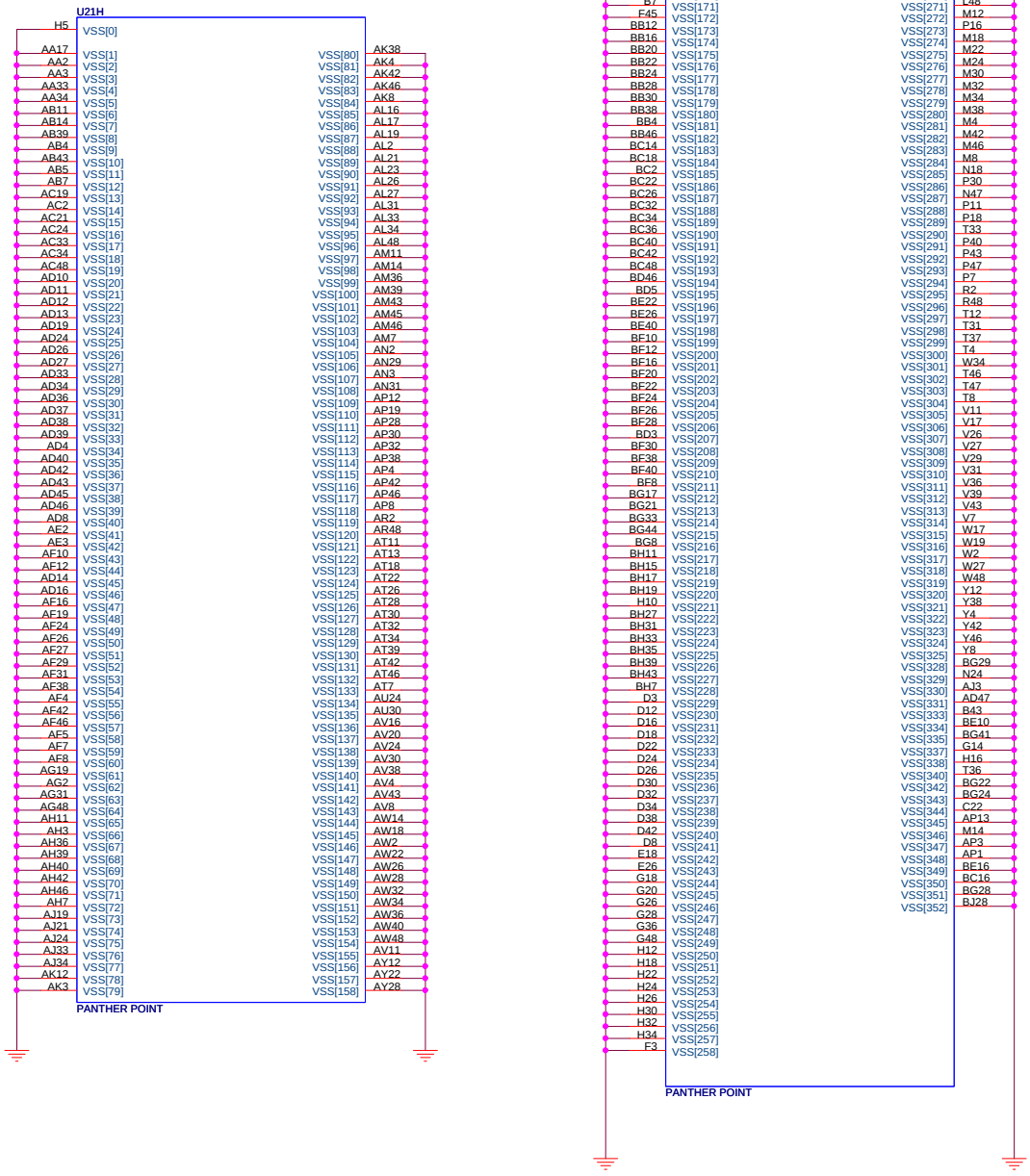




C38 Change C562, C564 from 220U to 100U for cost down. 02/08

Quanta Computer Inc.		
PROJECT : ZQS 45W		
Size	Document Number: Panther Point 5/6	Rev: 3C
Date: Wednesday, February 08, 2012	Sheet 11 of 46	

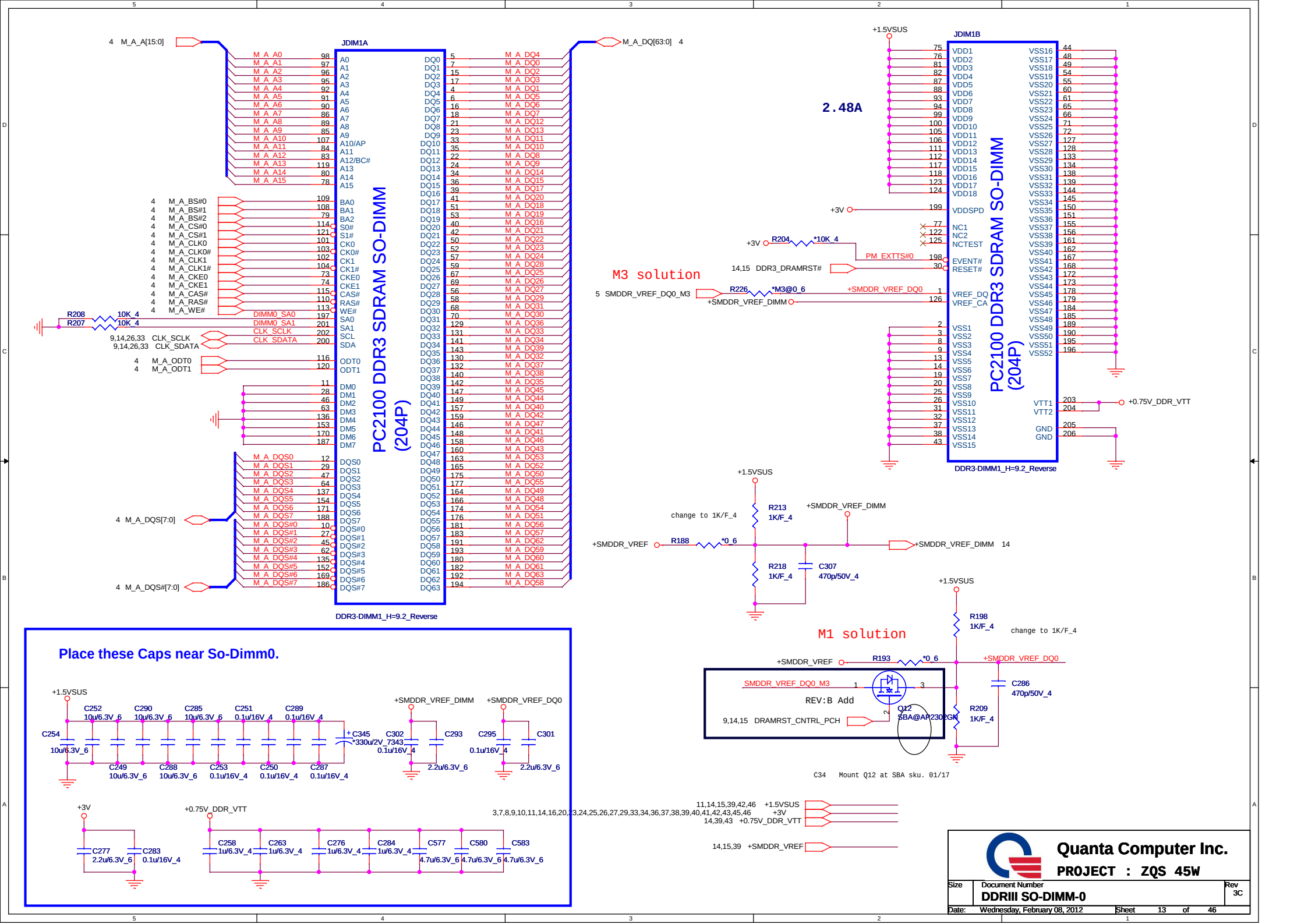
IBEX PEAK-M (GND)

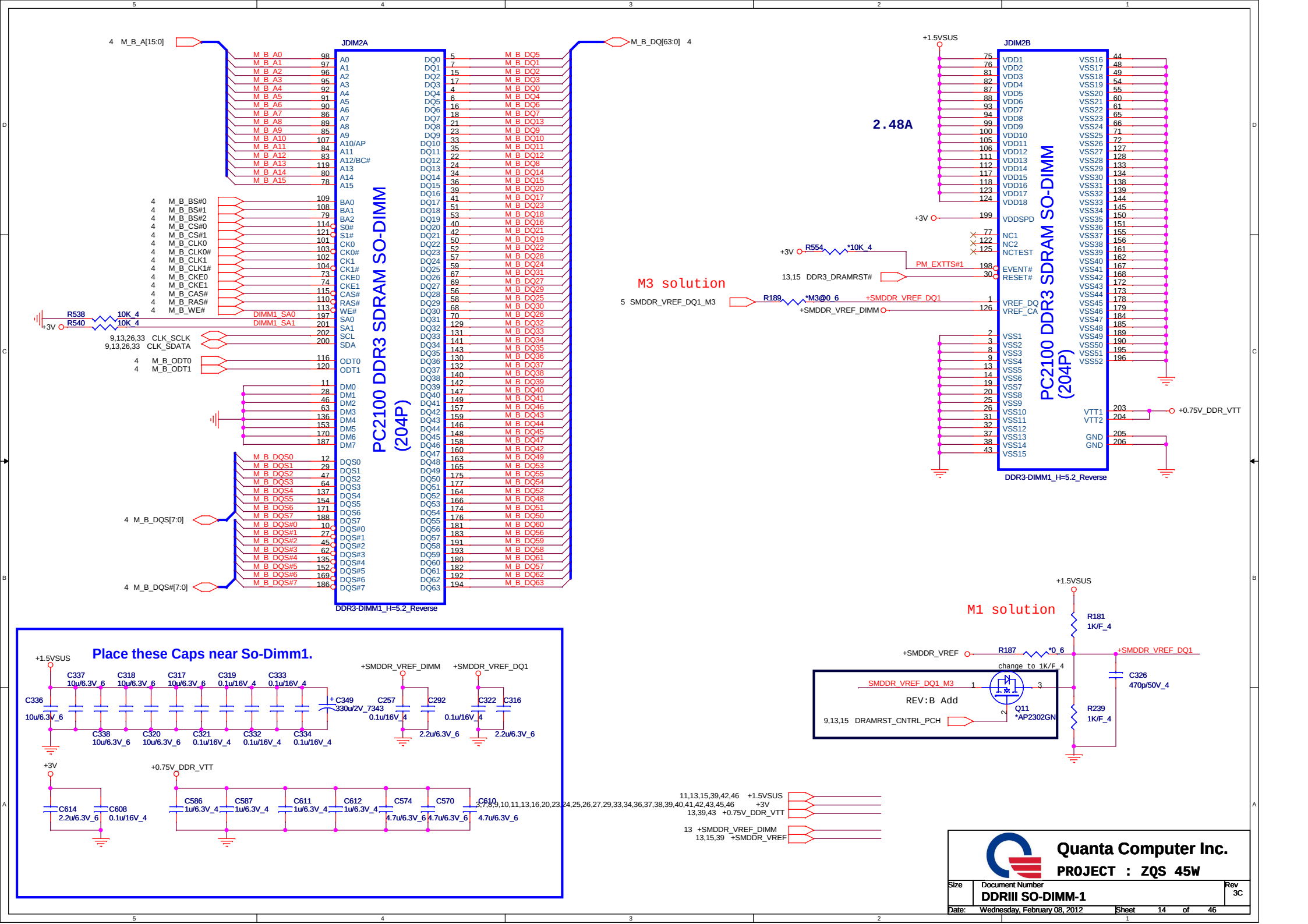


Quanta Computer Inc.

PROJECT : ZQS 45W

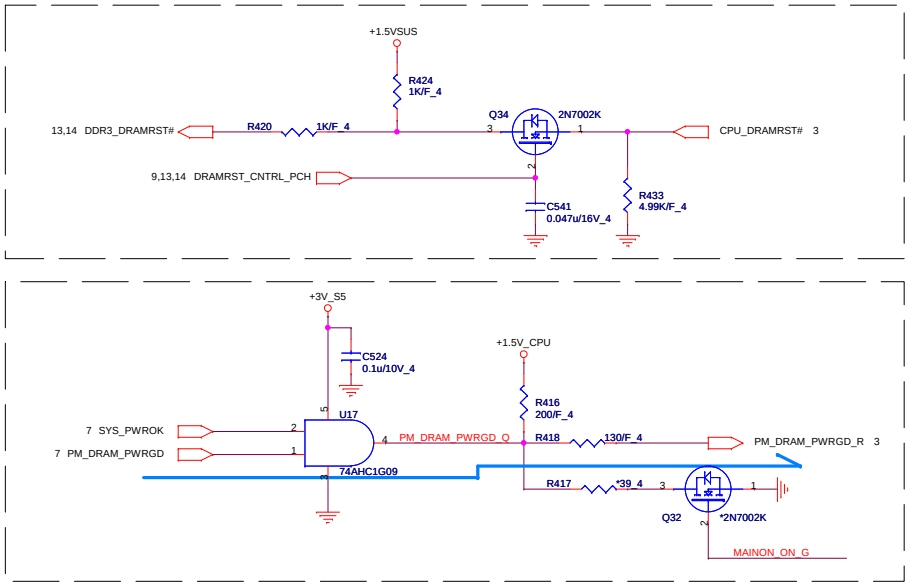
Size	Document Number	Rev
	Panther Point 6/6	3C
Date: Wednesday, February 08, 2012	Sheet 12 of 46	

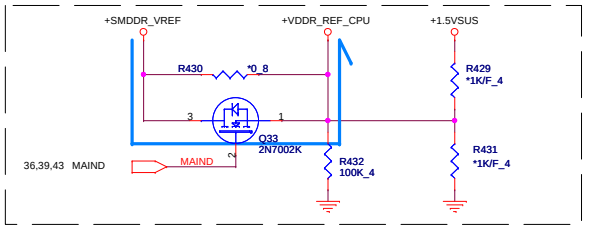

JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=9.2_Reverse
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=9.2_Reverse
2.48A
M3 solution
M1 solution
Place these Caps near So-Dimm0.
REV:B Add
C34 Mount Q12 at SBA sku. 01/17
Quanta Computer Inc.
PROJECT : ZQS 45W
DDRIII SO-DIMM-0
Wednesday, February 08, 2012


JDIM2A
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM1_H=5.2_Reverse
4 M_B_A[15:0]
M_B_DQ[63:0] 4
4 M_B_DQS[7:0]
4 M_B_DQS#[7:0]
M_B_BS#0
M_B_BS#1
M_B_BS#2
M_B_CS#0
M_B_CS#1
M_B_CLK0
M_B_CLK0#
M_B_CLK1
M_B_CLK1#
M_B_CKE0
M_B_CKE1
M_B_CAS#
M_B_RAS#
M_B_WE#
R538 10K_4
R540 10K_4
+3V
DIMM1_SA0
DIMM1_SA1
9,13,26,33 CLK_SCLK
9,13,26,33 CLK_SDATA
M_B_ODT0
M_B_ODT1
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM1_H=5.2_Reverse
+1.5VSUS
2.48A
+3V
R554 *10K_4
PM_EXTTS#1
13,15 DDR3_DRAMRST#
M3 solution
5 SMDDR_VREF_DQ1_M3
R189 *M3@0_6
+SMDDR_VREF_DQ1
+SMDDR_VREF_DIMM
+0.75V_DDR_VTT
M1 solution
R181 1K/F_4
+SMDDR_VREF
R187 *0_6
change to 1K/F_4
SMDDR_VREF_DQ1_M3
REV:B Add
9,13,15 DRAMRST_CNTRL_PCH
Q11 *AP2302GN
R239 1K/F_4
C326 470p/50V_4
Place these Caps near So-Dimm1.
C336 10u/6.3V_6
C337 10u/6.3V_6
C318 10u/6.3V_6
C317 10u/6.3V_6
C319 0.1u/16V_4
C333 0.1u/16V_4
C338 10u/6.3V_6
C320 10u/6.3V_6
C321 0.1u/16V_4
C332 0.1u/16V_4
C334 0.1u/16V_4
C349 330u/2V_7343
C257 0.1u/16V_4
C292 2.2u/6.3V_6
C322 0.1u/16V_4
C316 2.2u/6.3V_6
C614 2.2u/6.3V_6
C608 0.1u/16V_4
C586 1u/6.3V_4
C587 1u/6.3V_4
C611 1u/6.3V_4
C612 1u/6.3V_4
C574 4.7u/6.3V_6
C570 4.7u/6.3V_6
C610 4.7u/6.3V_6
11,13,15,39,42,46 +1.5VSUS
+3V
13,39,43 +0.75V_DDR_VTT
13 +SMDDR_VREF_DIMM
13,15,39 +SMDDR_VREF
Quanta Computer Inc.
PROJECT : ZQS 45W
Size
Document Number
DDRIII SO-DIMM-1
Rev 3C
Date: Wednesday, February 08, 2012
Sheet 14 of 46

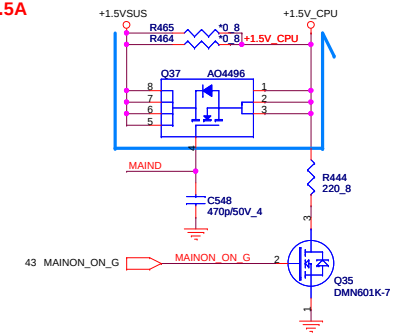
CPU XDP Connector(CPU)

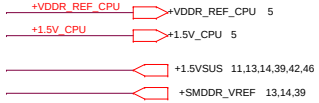
s3 leakage circuit





4.5A





Quanta Computer Inc.

PROJECT : ZQS 45W

Size	Document Number	Rev
	XDP	3C

Date: Wednesday, February 08, 2012 Sheet 15 of 46

DIS.VGA-->EV@ + EOP@
Optimize-->IOP@ + EOP@
UMA-->IV@ + IOP@
Special-->SP@

FOR DIS & Optimus

1000mA
2500mA
150mA
210mA

[PEG Interface]

U14A

EOP@N13x

N13P

N13M-GS	N13P- GL
N13P-GS	N13P- PES
Stuff--> R	Reserve--> R
Reserve -->L	Stuff--> L

Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	

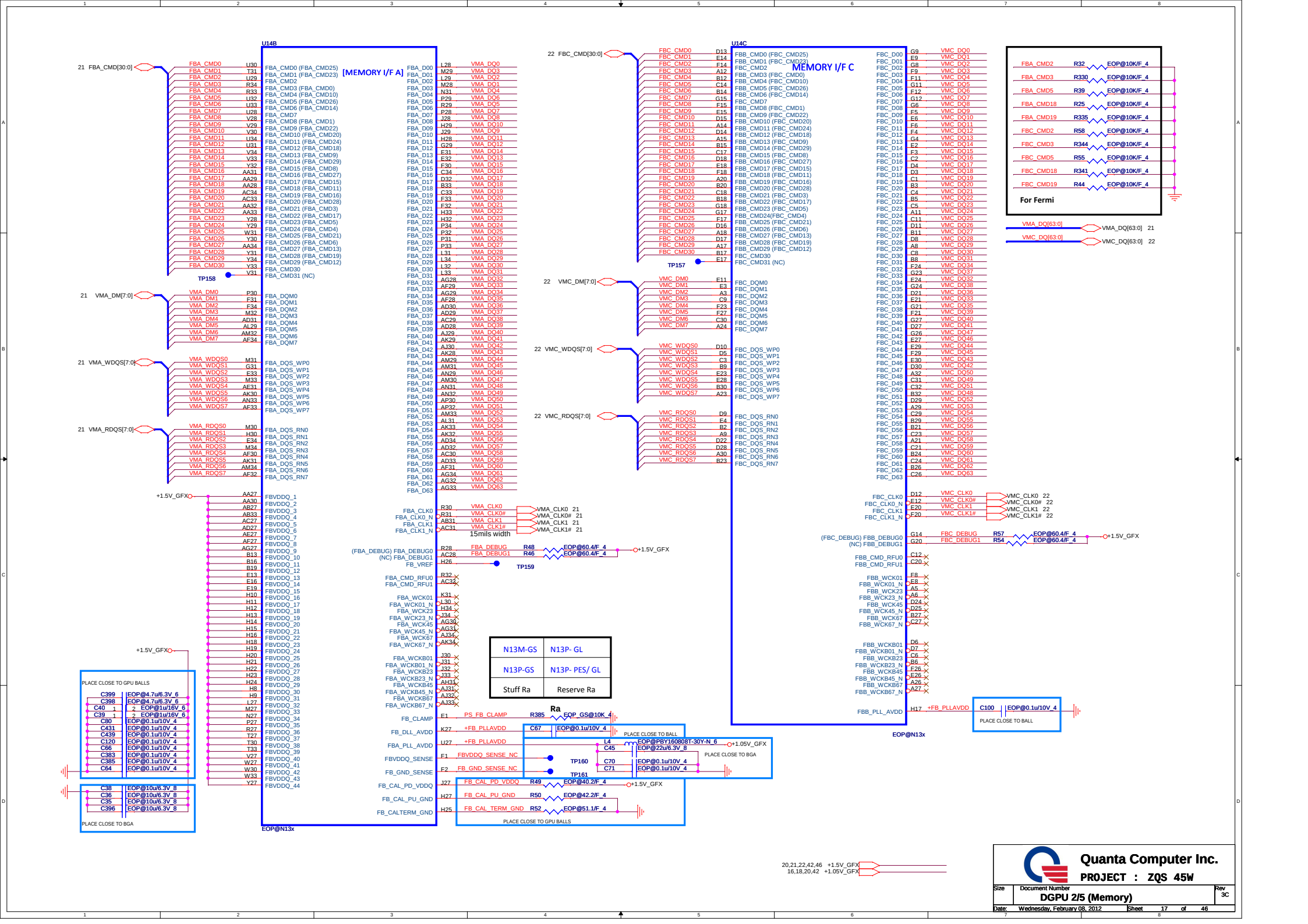
PEX_RST timing

I/O 3.3V
PEX_RST
Trise >= 1uS
Tfail <=500nS

Quanta Computer Inc.
PROJECT : ZQS 45W

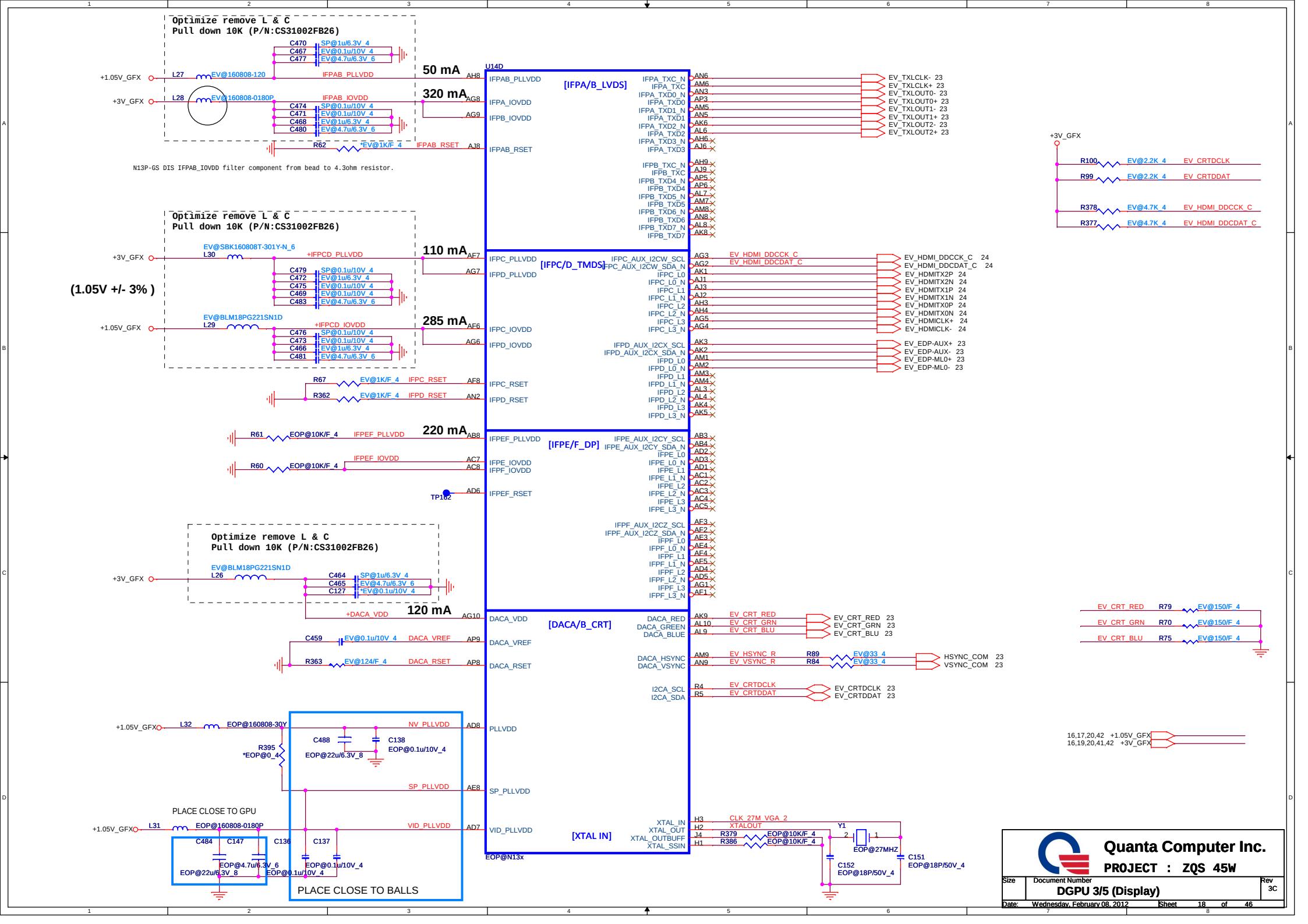
Size	Document Number	Rev
	DGPU 1/5 (PEG)	3C

Date: Wednesday, February 08, 2012 Sheet 16 of 46



20,21,22,42,46 +1.5V_GFX
16,18,20,42 +1.05V_GFX

Quanta Computer Inc.	
PROJECT : ZQS 45W	
Size	Document Number: DGPU 2/5 (Memory) — Rev: 3C
Date: Wednesday, February 08, 2012	Sheet 17 of 46


Optimize remove L & C
Pull down 10K (P/N:CS31002FB26)
50 mA
320 mA
N13P-GS DIS IFPAB_IOVDD filter component from bead to 4.3ohm resistor.
Optimize remove L & C
Pull down 10K (P/N:CS31002FB26)
(1.05V +/- 3%)
110 mA
285 mA
Optimize remove L & C
Pull down 10K (P/N:CS31002FB26)
220 mA
Optimize remove L & C
Pull down 10K (P/N:CS31002FB26)
120 mA
U14D
[IFPA/B_LVDS]
[IFPC/D_TMDS]
[IFPE/F_DP]
[DACA/B_CRT]
[XTAL IN]
PLACE CLOSE TO GPU
PLACE CLOSE TO BALLS
Quanta Computer Inc.
PROJECT : ZQS 45W
DGPU 3/5 (Display)
Wednesday, February 08, 2012
Sheet 18 of 46

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	O	GPU_VID4	GPU CORE_VDD VID4
1	O	GPU_VID3	GPU CORE_VDD VID3
2	O	LCD_BL_PWM	LCD BACKLIGHT PWM
3	O	LCD_VCC	PANEL POWER ENABLE
4	O	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	O	GPU_VID1	GPU CORE_VDD VID1
6	O	GPU_VID2	GPU CORE_VDD VID2
7	O	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	O	MEM VREF_CLT	MEMMORY VREF CONTROL
11	O	GPU_VID0	GPU CORE_VDD VID0
12	I	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	O	GPU_VID5	GPU CORE_VDD VID5
14	I	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	I	HPD_C	HOT PLUG DETECT FOR IFPC
16	O	MEM VDD	MEMMORY VDD CONTROL
17	I	HPD_D	HOT PLUG DETECT FOR IFPD
18	I	HPD_E	HOT PLUG DETECT FOR IFPE
19	I	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
34.8K---> CS33482FB22
45.3K ---> CS34532FB18

[MIOA]

[MIOB]

(Default: Hynix 2G)

ROM_SI
1G Hynix 64Mx16 -->15K PD
1G Micron 64Mx16 -->20K PD
2G Hynix 128Mx16 -->34.8K PD (B-Die)
2G Hynix 128Mx16 -->30.1K PD (D-Die)
2G Micron 128Mx16 -->45.3K PD

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10.0K	1001	0001
15.0K	1010	0010
20.0K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

QCI P/N	QCI STN B/S P/N
Hynix 64x16 900/1G P/N:	AKD5LZWTW02 / AKD5LZWTW05
Hynix 128X16 900/2G P/N:	AKD5MGWTW00 / AKD5MGWTW03
Micron 64X16 900/1G P/N:	AKD5EGSTL00 / X

C12 Change Q47 from 2N7002 to DTC144EUA, change Q47.2 from +3V_GFX to PEGX_RST#, connect GPU_TRPI# to Q47, add 0Ω R142,R237. 12/27

CRT flicker

C03 Add GPU_TRIP# to EC GPIO47, connect to NV GPI088. 12/23

R73 change from 34.8 KΩ to pull down 4.99KΩ for N13P-GS & GT STRAP1. 01/17

R382 change from 30.1 KΩ to pull down 45.3KΩ for N13P-GS & GT strap4. 01/04

N13M-GS STRAP 0-3 Define by RVL 128M*16 Hynix DDR3-> 0X6. 11/08

Strap Name	GPU Sku	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	BOM
		XCLK_417/FB[1]	FB_0_BAR_SIZE/FB[0]	SMB_ALT_ADDR	VGA_DEVICE	
ROM_SO	N13P-GL	0	0	0	1	Pull down 10K
	N13P-GS ES	1	0	0	1	Pull up 10K
	N13P-GT ES	1	0	0	1	Pull up 10K
	N13M-GS ES	0	1	0	1	Pull down 10K
		PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	
ROM_SCLK	N13P-GL	0	0	1	0	Pull down 15K
	N13P-GS ES	1	0	0	0	Pull up 4.99K
	N13P-GT ES	1	0	0	0	Pull up 4.99K
	N13M-GS ES	0	0	0	0	Pull down 10K
		RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	
ROM_SI	Hynix	X	X	X	X	
	Samsung	X	X	X	X	
	N13M-GS ES					Pull down 10K
		USER[3]	USER[2]	USER[1]	USER[0]	
STRAP0	N13P-GL	1	1	1	1	Pull up 45.3K
	N13P-GS ES	1	1	1	1	Pull up 45.3K
	N13P-GT ES	1	1	1	1	Pull up 45.3K
	N13M-GS ES	1	1	1	1	Pull down 10K
		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	
STRAP1	N13P-GL	0	1	1	1	Pull down 45.3K
	N13P-GS ES	0	0	0	0	Pull down 4.99K
	N13P-GT ES	0	0	0	0	Pull down 4.99K
	N13M-GS ES	0	1	1	0	Pull up 10K
		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	
STRAP2	N13P-GL	1	0	0	1	Pull up 10K
	N13P-GS ES2	1	0	1	1	Pull down 15K
	N13P-GT ES	1	0	1	1	Pull up 20K
	N13M-GS ES	1	0	0	1	Pull up 10K
		SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	
STRAP3	N13P-GL	0	0	0	0	Optimus Pull down 4.99K Discrete Pull down 15K
	N13P-GS ES	0	0	0	0	
	N13P-GT ES	0	0	0	0	
	N13M-GS ES	0	0	0	0	Pull down 10K
		RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	
STRAP4	N13P-GL	0	0	0	1	Pull down 10K
	N13P-GS QS	0	1	1	1	Pull down 45.3K
	N13P-GT QS	0	1	1	1	Pull down 45.3K
	N13M-GS ES	0	0	0	1	Pull down 10K

N13M-GS	N13P- GL
N13P-GS	N13P- PES
Reserve R373	Stuff R373

N13M-GS Straping table

Pin Name	Strap Mapping	Value
ROM_SCLK	SMB_ALT_ADDR	0
ROM_SI	SUB_VENDOR	0
ROM_SO	VGA_DEVICE	0
STRAP[3..0]	RAM_CFG[3..0]	0010(Hynix 64Mx16) 0110(Hynix 128Mx16)
STRAP[4]	PCIE_MAX_SPEED	0

Remark :
0 -> 10K PD
1 -> 10K PU

GFx SMBus Isolation

11/8 change for GPU temp detect

EOP@N13x

50 A

+VGACORE

U14F

[GPU VDD]

AA12	VDD_001	XVDD_001	U1
AA14	VDD_002	XVDD_002	U2
AA16	VDD_003	XVDD_003	U3
AA19	VDD_004	XVDD_004	U4
AA21	VDD_005	XVDD_005	U5
AA23	VDD_006	XVDD_006	U6
AB13	VDD_007	XVDD_007	U7
AB15	VDD_008	XVDD_008	U8
AB17	VDD_009	XVDD_009	V1
AB18	VDD_010	XVDD_010	V2
AB20	VDD_011	XVDD_011	V3
AB22	VDD_012	XVDD_012	V4
AC12	VDD_013	XVDD_013	V5
AC14	VDD_014	XVDD_014	V6
AC16	VDD_015	XVDD_015	V7
AC19	VDD_016	XVDD_016	V8
AC21	VDD_017	XVDD_017	W2
AC23	VDD_018	XVDD_018	W3
M12	VDD_019	XVDD_019	W4
M14	VDD_020	XVDD_020	W5
M16	VDD_021	XVDD_021	W7
M19	VDD_022	XVDD_022	W8
M21	VDD_023	XVDD_023	Y1
M23	VDD_024	XVDD_024	Y2
N13	VDD_025	XVDD_025	Y3
N15	VDD_026	XVDD_026	Y4
N17	VDD_027	XVDD_027	Y5
N18	VDD_028	XVDD_028	Y6
N20	VDD_029	XVDD_029	Y7
N22	VDD_030	XVDD_030	Y8
P12	VDD_031	XVDD_031	AA1
P14	VDD_032	XVDD_032	AA2
P16	VDD_033	XVDD_033	AA3
P19	VDD_034	XVDD_034	AA4
P21	VDD_035	XVDD_035	AA5
P23	VDD_036	XVDD_036	AA6
R13	VDD_037	XVDD_037	AA7
R15	VDD_038	XVDD_038	AA8
R17	VDD_039		
R18	VDD_040		
R20	VDD_041		
R22	VDD_042		
T12	VDD_043		
T14	VDD_044		
T16	VDD_045		
T19	VDD_046		
T21	VDD_047		
T23	VDD_048		
U13	VDD_049		
U15	VDD_050		
U17	VDD_051		
U18	VDD_052		
U20	VDD_053		
U22	VDD_054		
V13	VDD_055		
V15	VDD_056		
V17	VDD_057		
V18	VDD_058		
V20	VDD_059		
V22	VDD_060		
W12	VDD_061		
W14	VDD_062		
W16	VDD_063		
W19	VDD_064		
W21	VDD_065		
W23	VDD_066		
Y13	VDD_067		
Y15	VDD_068		
Y18	VDD_069		
Y17	VDD_070		
Y20	VDD_071		
Y22	VDD_072		

EOP@N13x

U14G

[GPU GND]

A2	GND_1	GND_101	D2
AA17	GND_2	GND_102	D31
AA18	GND_3	GND_103	D33
AA20	GND_4	GND_104	E10
AA22	GND_5	GND_105	E22
AB12	GND_6	GND_106	E25
AB14	GND_7	GND_107	E5
AB16	GND_8	GND_108	E7
AB19	GND_9	GND_109	F28
AB2	GND_10	GND_110	F7
AB21	GND_11	GND_111	G10
A33	GND_12	GND_112	G13
AB23	GND_13	GND_113	G16
AB28	GND_14	GND_114	G19
AB30	GND_15	GND_115	G2
AB32	GND_16	GND_116	G22
AB5	GND_17	GND_117	G25
AB7	GND_18	GND_118	G28
AC13	GND_19	GND_119	G3
AC15	GND_20	GND_120	G30
AC17	GND_21	GND_121	G32
AC18	GND_22	GND_122	G33
AA13	GND_23	GND_123	G5
AC20	GND_24	GND_124	G7
AC22	GND_25	GND_125	K2
AE2	GND_26	GND_126	K28
AE28	GND_27	GND_127	K30
AE30	GND_28	GND_128	K32
AE32	GND_29	GND_129	K33
AE33	GND_30	GND_130	K5
AE5	GND_31	GND_131	K7
AE7	GND_32	GND_132	M13
AH10	GND_33	GND_133	M15
AA15	GND_34	GND_134	M17
AH13	GND_35	GND_135	M18
AH16	GND_36	GND_136	M20
AH19	GND_37	GND_137	M22
AH2	GND_38	GND_138	N12
AH22	GND_39	GND_139	N14
AH24	GND_40	GND_140	N16
AH28	GND_41	GND_141	N19
AH29	GND_42	GND_142	N2
AH30	GND_43	GND_143	N21
AH32	GND_44	GND_144	N23
AH33	GND_45	GND_145	N28
AH5	GND_46	GND_146	N30
AH7	GND_47	GND_147	N32
AJ7	GND_48	GND_148	N33
AK10	GND_49	GND_149	N5
AK7	GND_50	GND_150	N7
AL12	GND_51	GND_151	P13
AL14	GND_52	GND_152	P15
AL15	GND_53	GND_153	P17
AL17	GND_54	GND_154	P18
AL18	GND_55	GND_155	P20
AL2	GND_56	GND_156	P22
AL20	GND_57	GND_157	R12
AL21	GND_58	GND_158	R14
AL23	GND_59	GND_159	R16
AL24	GND_60	GND_160	R19
AL26	GND_61	GND_161	R21
AL28	GND_62	GND_162	R23
AL30	GND_63	GND_163	T13
AL32	GND_64	GND_164	T15
AL33	GND_65	GND_165	T17
AL5	GND_66	GND_166	T18
AM13	GND_67	GND_167	T2
AM16	GND_68	GND_168	T20
AM19	GND_69	GND_169	T22
AM22	GND_70	GND_170	AG11
AM25	GND_71	GND_171	T28
AN1	GND_72	GND_172	T32
AN10	GND_73	GND_173	T5
AN13	GND_74	GND_174	T7
AN16	GND_75	GND_175	U12
AN19	GND_76	GND_176	U14
AN22	GND_77	GND_177	U16
AN25	GND_78	GND_178	U19
AN30	GND_79	GND_179	U21
AN34	GND_80	GND_180	U23
AN4	GND_81	GND_181	V12
AN7	GND_82	GND_182	V14
AP2	GND_83	GND_183	V16
AP33	GND_84	GND_184	V19
B1	GND_85	GND_185	V21
B10	GND_86	GND_186	V23
B22	GND_87	GND_187	W13
B25	GND_88	GND_188	W15
B28	GND_89	GND_189	W17
B31	GND_90	GND_190	W18
B34	GND_91	GND_191	W20
B4	GND_92	GND_192	W22
B7	GND_93	GND_193	W28
C10	GND_94	GND_194	Y12
C13	GND_95	GND_195	Y14
C19	GND_96	GND_196	Y16
C22	GND_97	GND_197	Y19
C25	GND_98	GND_198	Y21
C28	GND_99	GND_199	Y23
C7	GND_100	GND_200	AH11
		GND_OPT_1	C16
		GND_OPT_2	W32

EOP@N13x

PLACE UNDER GPU

+VGACORE

C85 EOP@1u/6.3V_4
C97 EOP@0.1u/10V_4
C117 EOP@0.1u/10V_4
C111 EOP@0.1u/10V_4
C128 EOP@0.1u/10V_4

C163 EOP@0.1u/10V_4
C170 EOP@0.1u/10V_4
C166 EOP@0.1u/10V_4
C162 EOP@0.1u/10V_4

+VGACORE

C89 EOP@4.7u/6.3V_6
C81 EOP@4.7u/6.3V_6
C98 EOP@4.7u/6.3V_6
C76 EOP@4.7u/6.3V_6
C123 EOP@4.7u/6.3V_6
C104 EOP@4.7u/6.3V_6
C122 EOP@4.7u/6.3V_6
C114 EOP@4.7u/6.3V_6

+VGACORE

C79 EOP@4.7u/6.3V_6
C77 EOP@4.7u/6.3V_6
C93 EOP@4.7u/6.3V_6
C99 EOP@4.7u/6.3V_6
C106 EOP@4.7u/6.3V_6
C112 EOP@4.7u/6.3V_6
C124 EOP@4.7u/6.3V_6

PLACE NEAR GPU

+VGACORE

C94 EOP@330u/2.5V_3528
C492 EOP@4.7u/25V_8
C491 EOP@4.7u/25V_8
C489 EOP@4.7u/25V_8
C490 EOP@4.7u/25V_8
C519 EOP@4.7u/25V_8
C487 EOP@22u/6.3V_8
C485 EOP@47u/6.3V_8

for meet Power down sequence for +3V_GFX

+VGACORE — D9 EOP@RB500V-40 — +3V_GFX
+1.5V_GFX — D10 EOP@RB500V-40 — +3V_GFX

+VGACORE

C508 EOP@330u/2V_7343
C497 EOP@330u/2V_7343

Power request
LSR

C31 Change DGPU_POK4 from +1.05V_GFX to +1.5V_GFX, DGPU_POK2 from +1.5V_GFX to +1.05V_GFX for possibly floating issue. 01/17

C13 Change R393 from reserve to mount. 12/27

+3V_GFX
R393 EOP@4.7K_4
+3V
R384 EOP@4.7K_4
DGPU_PWROK 10
R394 EOP@100K/F_4
Q25 EOP@DTC144EUA
C478 EOP@1000P/50V_4
DGPU_PGOK-1
+1.5V_GFX — R371 EOP@4.7K_4 — DGPU_POK4 — C463 *EOP@1000P/50V_4 — Q23 EOP@MMBT3904-7-F
+1.05V_GFX — R364 EOP@4.7K_4 — DGPU_POK2 — C461 *EOP@1000P/50V_4 — Q22 EOP@MMBT3904-7-F

41 +VGACORE
16,17,18,42 +1.05V_GFX
17,21,22,42,46 +1.5V_GFX
16,18,19,41,42 +3V_GFX
3,7,8,9,10,11,13,14,16,23,24,25,26,27,29,33,34,36,37,38,39,40,41,42,43,45,46 +3V

Quanta Computer Inc.
PROJECT : ZQS 45W

Size	Document Number	Rev
	DGPU 5/5 (Power/Ground)	3C

Date: Wednesday, February 08, 2012 Sheet 20 of 46

CHANNEL A: 256MB/512MB DDR3

17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]

VRAM2 / VRAM5 / VRAM1 / VRAM6

96-BALL SDRAM DDR3

SP_VRAM@VRAM _DDR3

Should be 240 Ohms +-1%

R29 EOP@243/F_4
R329 EOP@243/F_4
R26 EOP@243/F_4
R338 EOP@243/F_4

+1.5V_GFX

For sDDR3

VMA_CLK0 — R336 160/F_4 — VMA_CLK0#

Fermi : DDR3 Change to 160 ohm
1 : CS11602FB00 ,RES CHIP 160 1/16W +-1%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R332 EOP@1.33K/F_4
R30 EOP@1.33K/F_4
R28 EOP@1.33K/F_4
R333 EOP@1.33K/F_4

VREFC_VMA1 / VREFD_VMA1 / VREFC_VMA3 / VREFD_VMA3

R331 EOP@1.33K/F_4 — C381 EOP@0.1u/10V_4
R31 EOP@1.33K/F_4 — C26 EOP@0.1u/10V_4
R27 EOP@1.33K/F_4 — C22 EOP@0.1u/10V_4
R334 EOP@1.33K/F_4 — C386 EOP@0.1u/10V_4

17 FBA_CMD17 — FBA_CMD17 — TP1
17 FBA_CMD1 — FBA_CMD1 — TP2

For sDDR3

VMA_CLK1 — R337 160/F_4 — VMA_CLK1#

Fermi : DDR3 Change to 160 ohm
1 : CS11602FB00 ,RES CHIP 160 1/16W +-1%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

Samsung 900MHz 1G AKD5LGHT500

17,20,22,42,46 +1.5V_GFX

+1.5V_GFX
C387 EOP@1u/10V_4
C23 EOP@1u/10V_4
C384 EOP@1u/10V_4
C25 EOP@1u/10V_4

+1.5V_GFX
C393 EOP@10u/6.3V_8
C21 EOP@1u/10V_4
C388 EOP@1u/10V_4
C41 EOP@1u/10V_4
C27 EOP@1u/10V_4
C395 EOP@1u/10V_4

+1.5V_GFX
C427 EOP@10u/6.3V_8
C20 EOP@1u/10V_4
C389 EOP@1u/10V_4
C429 EOP@1u/10V_4
C42 EOP@1u/10V_4
C43 EOP@1u/10V_4
C19 EOP@1u/10V_4
C400 EOP@1u/10V_4

+1.5V_GFX
C392 EOP@10u/6.3V_8
C397 EOP@10u/6.3V_8
C391 EOP@0.1u/10V_4
C390 EOP@0.1u/10V_4
C394 EOP@0.1u/10V_4
C24 EOP@0.1u/10V_4
C379 EOP@0.1u/10V_4

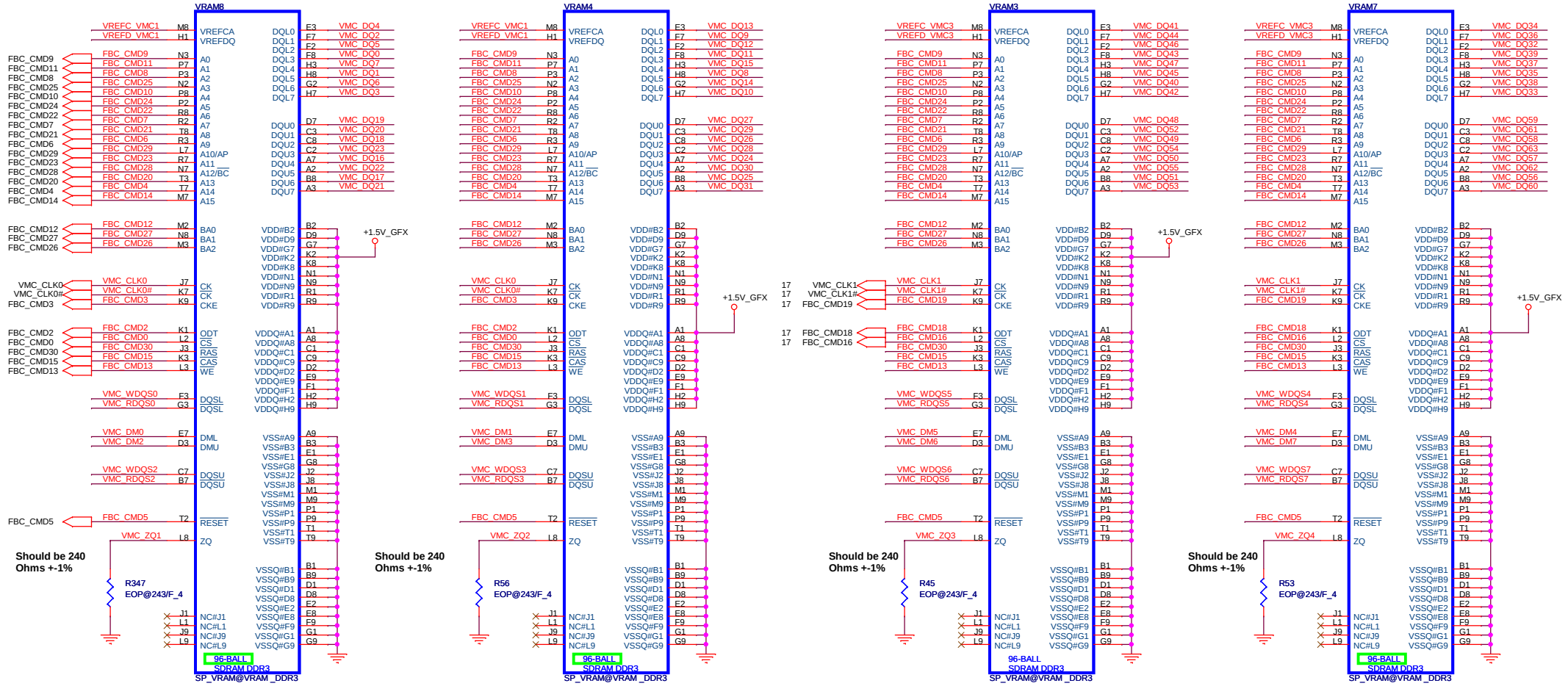
+1.5V_GFX
C17 EOP@10u/6.3V_8
C83 EOP@10u/6.3V_8
C382 EOP@0.1u/10V_4
C380 EOP@0.1u/10V_4
C88 EOP@0.1u/10V_4

Quanta Computer Inc.
PROJECT : ZQS 45W

Size	Document Number	Rev
	DGPU Memory 1/2 (DDR3)	3C
Date: Wednesday, February 08, 2012	Sheet 21 of 46	

CHANNEL B: 256MB/512MB DDR3

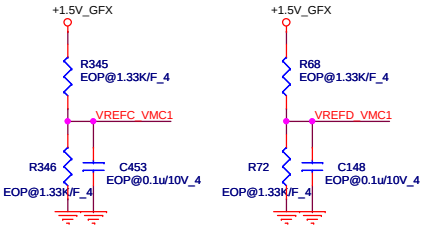
17 VMC_DQ[63..0]
17 VMC_DM[7..0]
17 VMC_WDQS[7..0]
17 VMC_RDQS[7..0]



For sDDR3

VMC_CLK0 — R350 160/F_4 — VMC_CLK0#

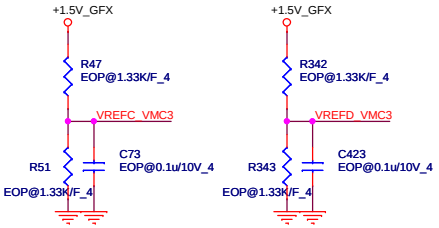
Fermi : DDR3 Change to 160 ohm
1 : CS11602FB00 ,RES CHIP 160 1/16W +-1%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

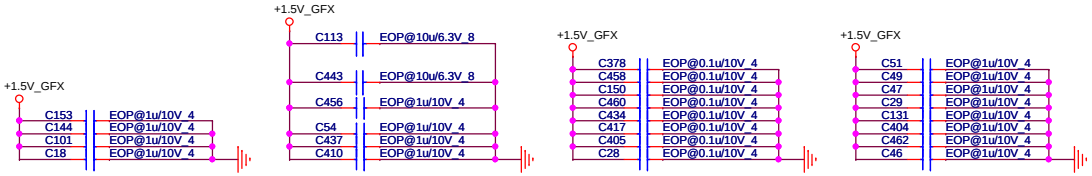


For sDDR3

VMC_CLK1 — R340 160/F_4 — VMC_CLK1#

Fermi : DDR3 Change to 160 ohm
1 : CS11602FB00 ,RES CHIP 160 1/16W +-1%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)





17 FBC_CMD17 — FBC_CMD17 — TP3
17 FBC_CMD1 — FBC_CMD1 — TP4

17,20,21,42,46 +1.5V_GFX

Samsung 900MHz 1G AKD5LGHT500

Quanta Computer Inc.
PROJECT : ZQS 45W

Size	Document Number	Rev
	DGPU Memory 2/2 (DDR3)	3C
Date: Wednesday, February 08, 2012	Sheet 22 of 46	

CRT

```
DIS.VGA-->EV@ + EOP@
Optimize-->IOP@ + EOP@
UMA-->IV@ + IOP@
Special-->SP@
```

From PCH

From EXT VGA

CM2009-02QR

LVDS & eDP

From PCH

From EXT VGA

```
Enable/Disable LVDS
Pull Up--->Enable
NC-->Disable
```

IV & Optimize-->0 ohm
EV-->10K ohm

CCD +3V-current budget 0.2A

CCD-USB

LCD Power

GS243AT11U

Lid Switch (Hall sensor)

EM-6781-T3: AL006781000
APX9132H AI-TRG: AL009132001
AH9249NTR-G1: AL009249000

Backlight Control

LID591#,EC intrnal PU

Quanta Computer Inc.	
PROJECT : ZQS 45W	
Size	Document Number: CRT/LVDS/CAMERA/LID
Rev	3C
Date: Wednesday, February 08, 2012	Sheet 23 of 46

HDMI

From PCH

7 INT_HDMITX2N
7 INT_HDMITX2P
RP13 IOP@0_4P2R
HDMITX2N_CAP
HDMITX2P_CAP
C581 0.1u/10V_4
C584 0.1u/10V_4
INT_HDMITX2N_C
INT_HDMITX2P_C

7 INT_HDMITX1N
7 INT_HDMITX1P
RP15 IOP@0_4P2R
HDMITX1N_CAP
HDMITX1P_CAP
C571 0.1u/10V_4
C573 0.1u/10V_4
INT_HDMITX1N_C
INT_HDMITX1P_C

7 INT_HDMITX0N
7 INT_HDMITX0P
RP17 IOP@0_4P2R
HDMITX0N_CAP
HDMITX0P_CAP
C575 0.1u/10V_4
C578 0.1u/10V_4
INT_HDMITX0N_C
INT_HDMITX0P_C

7 INT_HDMICLK+
7 INT_HDMICLK-
RP19 IOP@0_4P2R
HDMICLK+_CAP
HDMICLK-_CAP
C569 0.1u/10V_4
C568 0.1u/10V_4
INT_HDMICLK+_C
INT_HDMICLK-_C

DIS.VGA-->EV@ + EOP@
Optimize-->IOP@ + EOP@
UMA-->IV@ + IOP@
Special-->SP@

EV@499/F_4
P/N: CS14992FB24
UMA/Optimize-->590 Ohm
P/N: CS15902FB00

R483 SP@510_4
R486 SP@510_4
R492 SP@510_4
R491 SP@510_4
R489 SP@510_4
R487 SP@510_4
R496 SP@510_4
R494 SP@510_4

+5V R498 *0_4
+3V R624 0_4
R497 EOP@100K/F_4
Q41 2N7002E

Discrete stuff 499 Ohm
UMA/Optimize-->510 Ohm

C02 Change R483,R486,R492,R491,R498,R487,R496,R494 from 590Ω to 510Ω, and mount HDMI R194,R205,R202,R212 120Ω at optimus sku for EMI. 12/21

HDMI connector

+5V F2 SMD1206P110TFT/1.1A_1206
HDMI_5V_R D13 SSM22LLPT HDMI_5V
C557 470p/50V_4
HDMI_MB_HP R186 *SHORT_4 HP_DET_CN
R182 100K_4

CN14 HDMI CONN
SHELL1 20
D2+ INT_HDMITX2P_C
D2 Shield
D2- INT_HDMITX2N_C
D1+ INT_HDMITX1P_C
D1 Shield
D1- INT_HDMITX1N_C
D0+ INT_HDMITX0P_C
D0 Shield
D0- INT_HDMITX0N_C
CK+ INT_HDMICLK+_C
CK Shield
CK- INT_HDMICLK-_C
CE Remote
NC
DDC CLK HDMI_DDCCLK_MB
DDC DATA HDMI_DDCDATA_MB
GND
+5V
HP DET HDMI_HP_DET
SHELL2 21

From EXT VGA

18 EV_HDMITX2N
18 EV_HDMITX2P
RP14 EV@0_4P2R
HDMITX2N_CAP
HDMITX2P_CAP

18 EV_HDMITX1N
18 EV_HDMITX1P
RP16 EV@0_4P2R
HDMITX1N_CAP
HDMITX1P_CAP

18 EV_HDMITX0N
18 EV_HDMITX0P
RP18 EV@0_4P2R
HDMITX0N_CAP
HDMITX0P_CAP

18 EV_HDMICLK-
18 EV_HDMICLK+
RP20 EV@0_4P2R
HDMICLK-_CAP
HDMICLK+_CAP

HDMI-detect

+3V R180 10K_4
+3V R196 10K_4
R197 IOP@0_4 HDMI_HP 7
34 HDMI_HPD_EC#
R484 EV@0_4 EV_HDMI_HPD 19
+5V R191 *10K_4
HDMI_MB_HP
Q10 2N7002E
Q9 2N7002E

I2C

From EXT VGA

18 EV_HDMI_DDCCK_C R404 EV@0_4 HDMI_DDCCLK_COM
18 EV_HDMI_DDCDAT_C R405 EV@0_4 HDMI_DDCDATA_COM

From PCH

7 HDMI_DDCCLK_SW R455 IOP@0_4 HDMI_DDCCLK_COM
7 HDMI_DDCDATA_SW R457 IOP@0_4 HDMI_DDCDATA_COM

+3V R459 *SHORT_4
+5V D14 RB501V-40
+3V R468 IOP@2.2K_4
Q38 BSN20
R461 2.2K_4
HDMI_DDCCLK_MB

+3V R478 *SHORT_4
+5V D15 RB501V-40
+3V R473 IOP@2.2K_4
Q39 BSN20
R474 2.2K_4
HDMI_DDCDATA_MB

EMI

INT_HDMITX2P_C R212 120/F_4 INT_HDMITX2N_C
INT_HDMITX1P_C R202 120/F_4 INT_HDMITX1N_C
INT_HDMITX0P_C R205 120/F_4 INT_HDMITX0N_C
INT_HDMICLK+_C R194 120/F_4 INT_HDMICLK-_C

C02 Change R483,R486,R492,R491,R498,R487,R496,R494 from 590Ω to 510Ω, and mount HDMI R194,R205,R202,R212 120Ω at optimus sku for EMI. 12/21

3,7,8,9,10,11,13,14,16,20,23,25,26,27,29,33,34,36,37,38,39,40,41,42,43,45,46 +3V
8,11,23,26,27,33,36,43,46 +5V

Quanta Computer Inc.
PROJECT : ZQS 45W

Size	Document Number	Rev
	HDMI (PS8101)	3C
Date: Wednesday, February 08, 2012	Sheet 24 of 46	

Check LED signal. (active high or low)

MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

C37 Add Q50 connect to BT_POWERON# for WLAN ON/OFF function, pull up BT_PWRON by 10KΩ R671 to +WL_VDD, reserve 10KΩ R672 to +3V. 01/31

31,34 BT_POWERON#
Q50 DTC144EUA
R671 10K_4
R672 *10K_4
BT_PWRON
R637 *SHORT_4
Debug
TP125
CL_RST1#_WLAN
PLTRST# R314 0_4 CL_DATA1_WLAN
R315 0_4 CL_CLK1_WLAN
9 CLK_LPC_DEBUG
C26 Mount R314, R315. 01/12

CN20
MINI-CARD1

C32 Add net WLAN_OFF to connect EC(GPIO66/G_PWM) to CN20.46 (LED_WPAN#) for IOAC feature, mount 0Ω R670. 01/18
C36 Remove R308 reserved 10KΩ for LED_WLAN# pull high +3V. 01/31
C25 Change CN20 pin 30 &28 from CLK_SDATA & CLK_SCLK to SMB_PCH_CLK & SMB_PCH_DAT, reserve 0Ω R663,R664. 1/12
C07

R670 0_4
WLAN_OFF 34
LED_WLAN# 33
USBP10+ 9
USBP10- 9
WL_CLK_SDATA R664 *0_4 C25
WL_CLK_SCLK R663 *0_4
SMB_PCH_DAT 9
SMB_PCH_CLK 9
PLTRST# 9,16,29,34
RF_EN 34

9 PCIE_TX8+
9 PCIE_TX8-
9 PCIE_RX8+
9 PCIE_RX8-

9 CLK_PCH_SRC5
9 CLK_PCH_SRC5#
R305 *SHORT_4 CLK_PCH_WIFI
R306 *SHORT_4 CLK_PCH_WIFI#
9 PCIE_CLKREQ5#
PCIE_CLKREQ5#_R
DTC144EUA Q49
C27 Add Q49 connect PCIE_CLKREQ5# to CN20.7. 01/12

Debug
A_LFRAME#_R R582 *SHORT_4 LPC_LFRAME# 8,34
A_LAD3_R R581 *SHORT_4 LPC_LAD3 8,34
A_LAD2_R R578 *SHORT_4 LPC_LAD2 8,34
A_LAD1_R R577 *SHORT_4 LPC_LAD1 8,34
A_LAD0_R R576 *SHORT_4 LPC_LAD0 8,34

+WL_VDD
Q42 DTC144EUA
34 WAKE_WLAN
PCIE_WAKE#_R
C06 Change PCH_GPIO27 to WAKE_WLAN, connect to Q42 & EC GPIO96, Q42 change from reserve to mount. 12/23

+3V
R316 *0_8
+WL_VDD
C366 10u/6.3V_8
C659 0.1u/10V_4
C657 *0.1u/10V_4
C654 *0.1u/10V_4

C24 Change mini pcie power source from +3V_S5 to +3VPCU. 01/12
Q48 AO3413
+3VPCU
C708 0.33u/10V_6
R661 47K/F_4
R662 4.7K_4
34 IOAC_LANPWR#
C08 Connect EC GPIO46 IOAC_LANPWR# to WLAN, R662, add C708, R661, Q48, reserve R316. 12/23

+1.5V
+1.5V_WLAN R608 *0_6
C655 *1000p/50V_4
C658 *0.1u/10V_4
C355 *10u/6.3V_8
C07 Add R608 and reserve +1.5V to WLAN. 12/23

SSD-MINI module

+3V_SATA
R309 *SHORT_8 +3V
C635 0.1u/10V_4
C633 0.1u/10V_4
C360 10u/10V_8

CN7
MINI-CARD1
TP59
LED_OUT

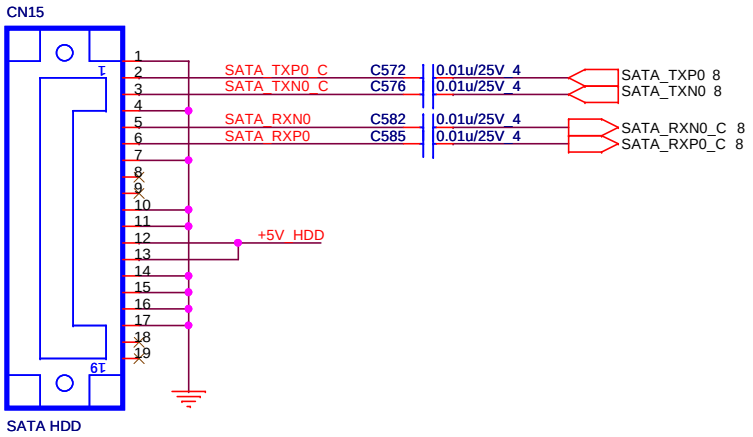
8 SATA_TXP_SSD
8 SATA_TXN_SSD
C362 0.01u/16V_4 SATA_TXP_SSD_R
C361 0.01u/16V_4 SATA_TXN_SSD_R
8 SATA_RXN_SSD
8 SATA_RXP_SSD
C359 0.01u/16V_4 SATA_RXN_SSD_R
C358 0.01u/16V_4 SATA_RXP_SSD_R
USBP3+ 9
USBP3- 9

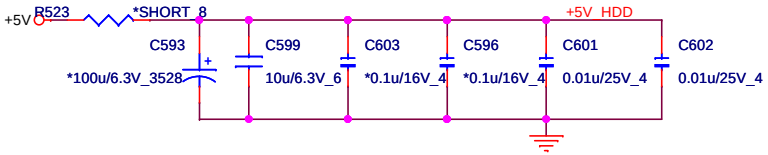
Quanta Computer Inc.
PROJECT : ZQS 45W

Size	Document Number	Rev
	MINI PCI-E / SSD	3C

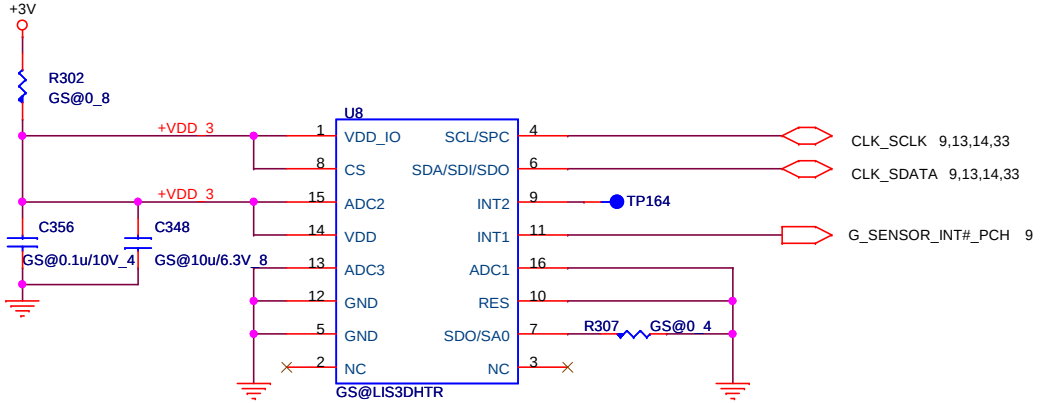
Date: Wednesday, February 08, 2012 Sheet 25 of 46

MAIN SATA HDD(HDD)



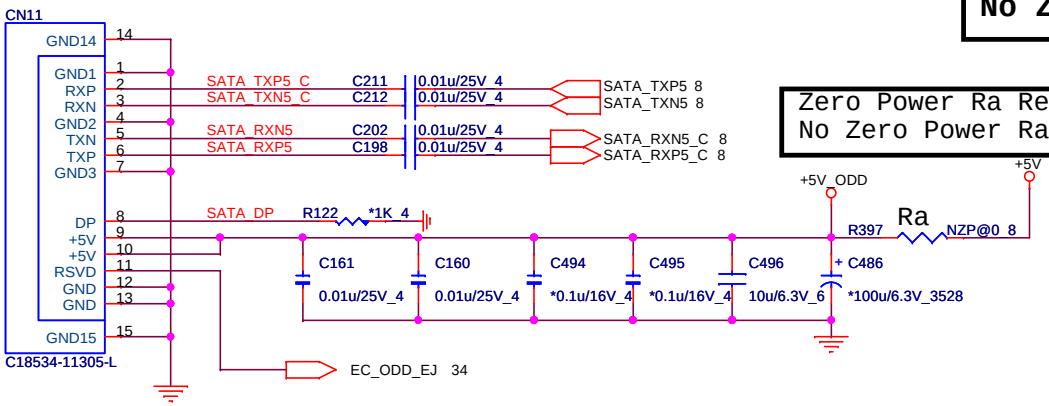


G Sensor



G-Sensor -->GS@

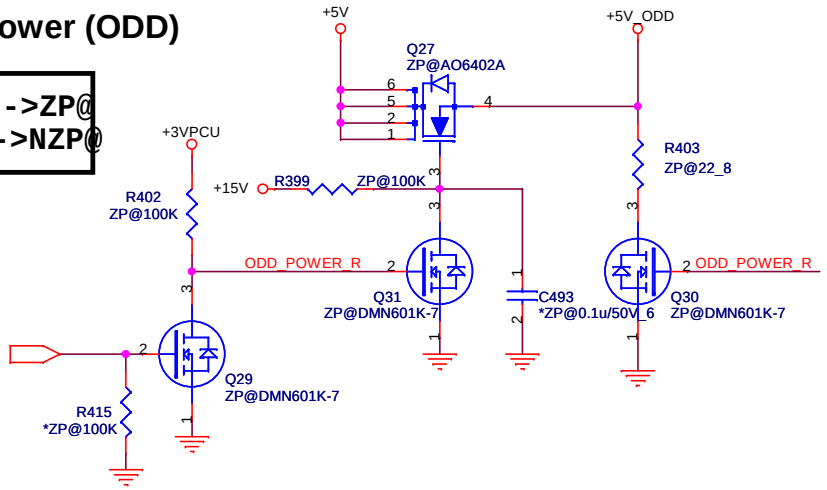
ODD (ODD)



Zero Power Ra Reserve,
No Zero Power Ra stuff

Zero Power (ODD)

Zero Power -->ZP@
No Zero Power -->NZP@

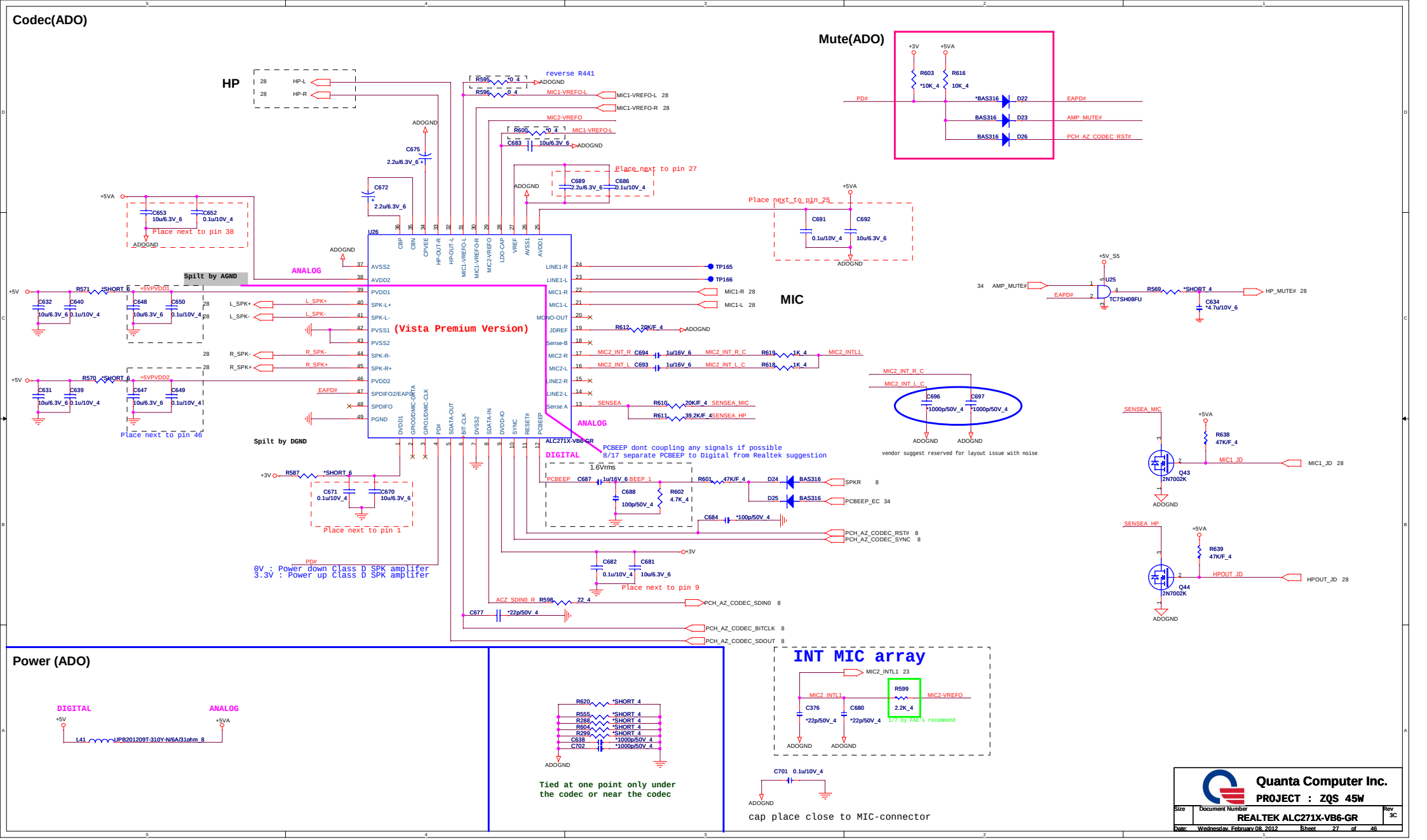


Quanta Computer Inc.

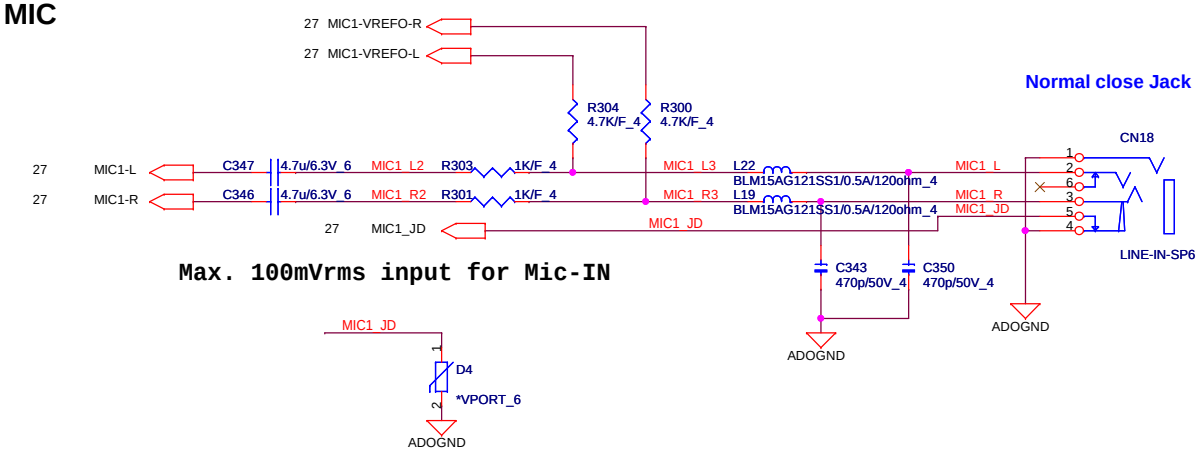
PROJECT : ZQS 45W

Size	Document Number	Rev
	SATA-HDD/ODD/G Sensor	3C
Date: Wednesday, February 08, 2012	Sheet 26 of 46	

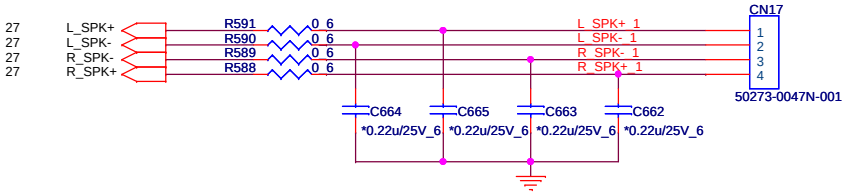
Codec(ADO)


HP
HP-L
HP-R
reverse R441
MIC1-VREFO-L
MIC1-VREFO-R
MIC2-VREFO
Place next to pin 27
Place next to pin 38
Place next to pin 25
Place next to pin 46
Place next to pin 1
Place next to pin 9
ANALOG
Spilt by AGND
Spilt by DGND
(Vista Premium Version)
U26
ALC271X-VB6-GR
MIC
DIGITAL
PCBEEP dont coupling any signals if possible
8/17 separate PCBEEP to Digital from Realtek suggestion
1.6Vrms
vendor suggest reserved for layout issue with noise
0V : Power down Class D SPK amplifier
3.3V : Power up Class D SPK amplifier
Mute(ADO)
INT MIC array
cap place close to MIC-connector
Tied at one point only under
the codec or near the codec
Power (ADO)
DIGITAL
ANALOG
L41 UPB201209T-310Y-N/6A/31ohm_8
Quanta Computer Inc.
PROJECT : ZQS 45W
REALTEK ALC271X-VB6-GR
Wednesday, February 08, 2012
Sheet 27 of 46

MIC

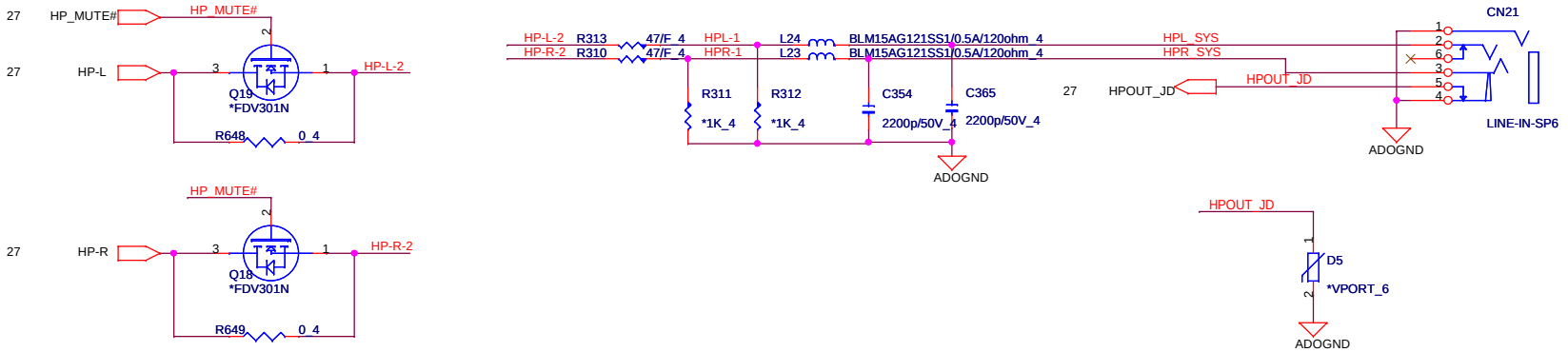


Internal Speaker



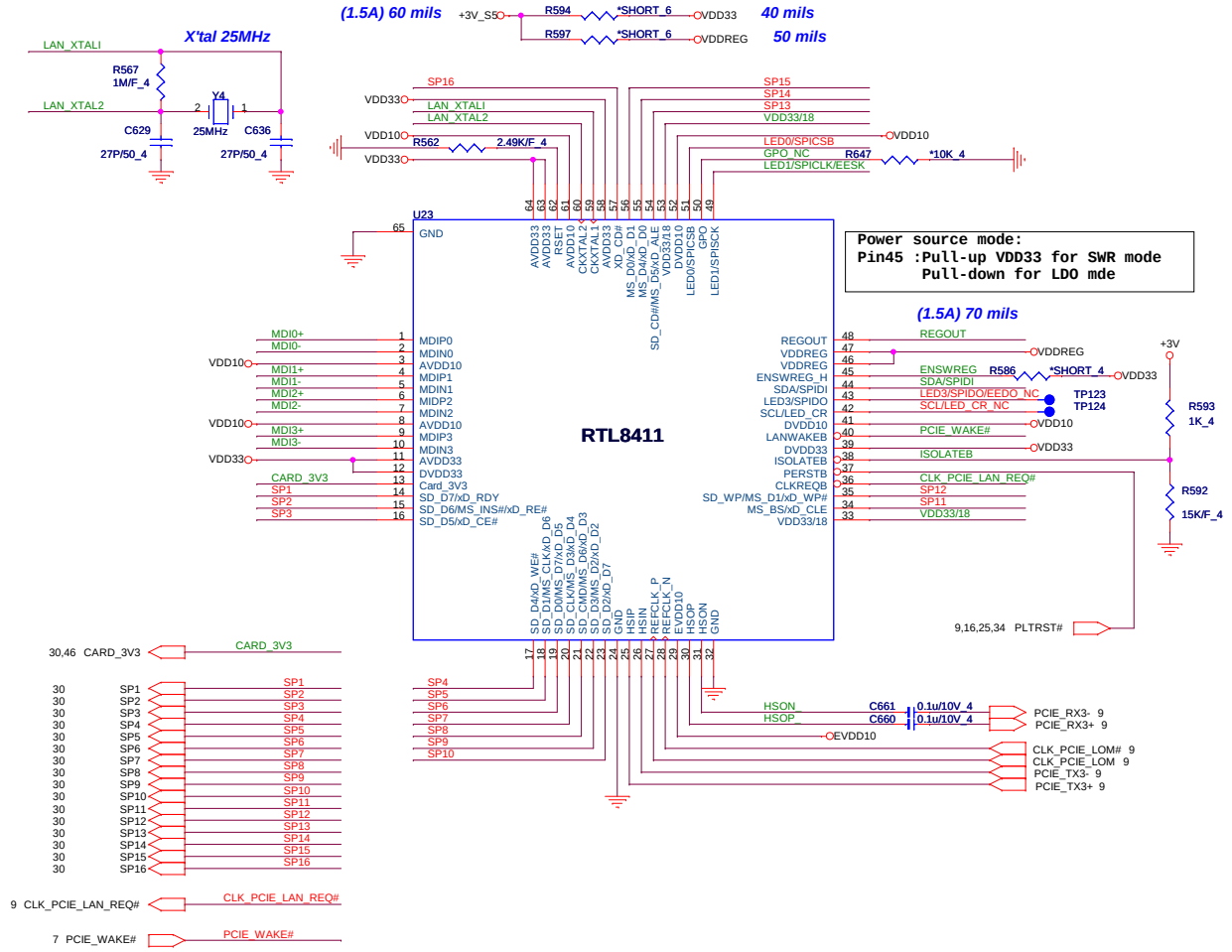
HP

Change to Normal Close circuit 11/1

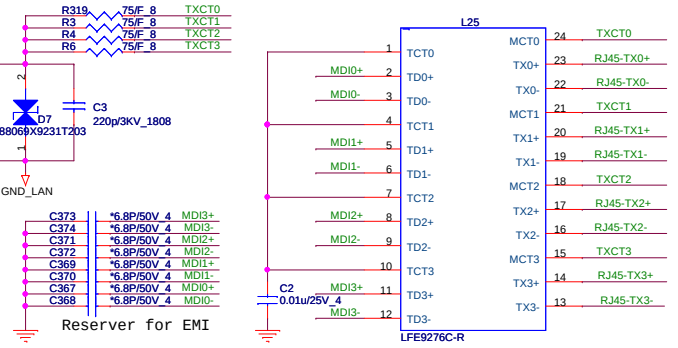


Quanta Computer Inc.		
PROJECT : ZQS 45W		
Size	Document Number: AUDIO JACK CONN	Rev: 3C
Date: Wednesday, February 08, 2012	Sheet 28 of 46	

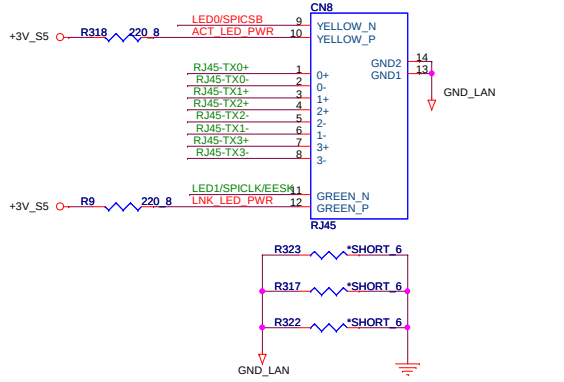
LAN/Card reader



Transformer

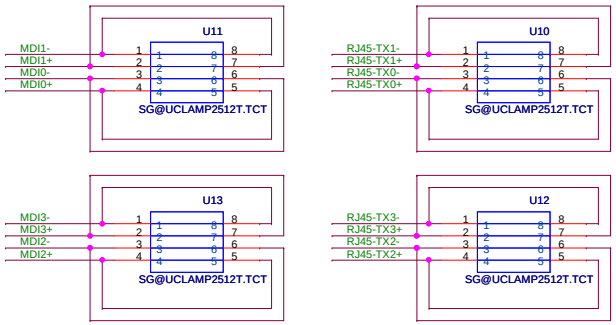


RJ45

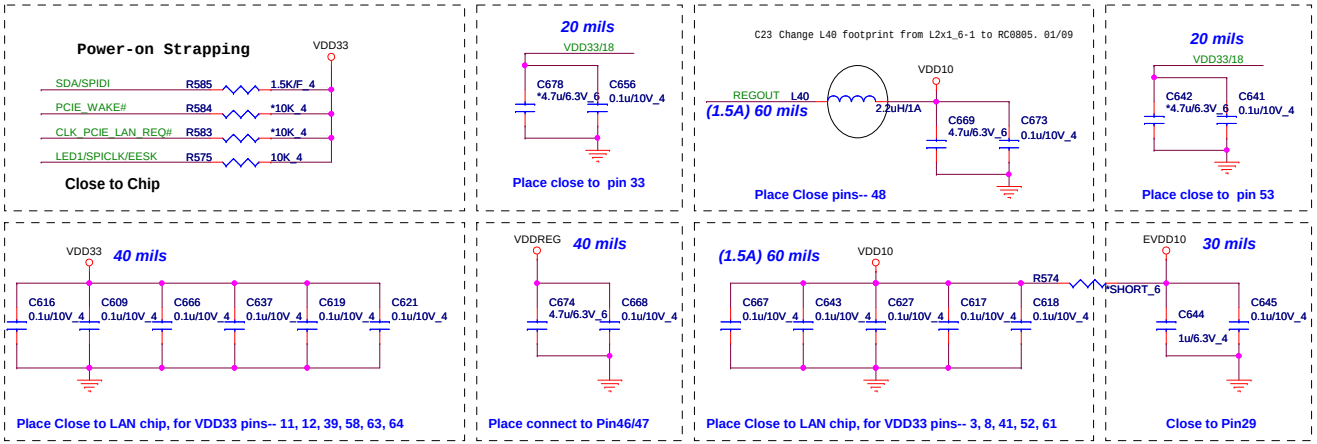


SURGE

SG@-------> Lan Surge



7,8,9,10,11,15,16,31,33,36,37,38,43,44 +3V_S5



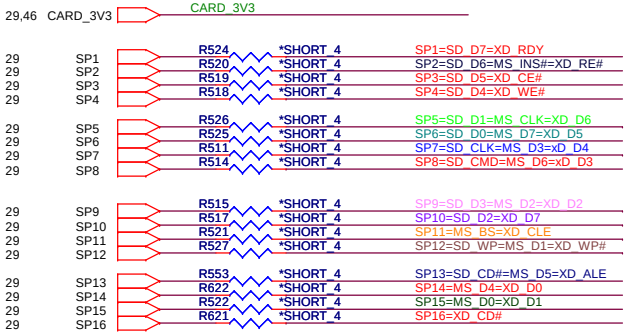
Quanta Computer Inc.			
PROJECT : ZQS 45W			
Size	Document Number		Rev
	LAN-RTL8411/CARD READER		3C
Date: Wednesday, February 08, 2012	Sheet 29	of 46	

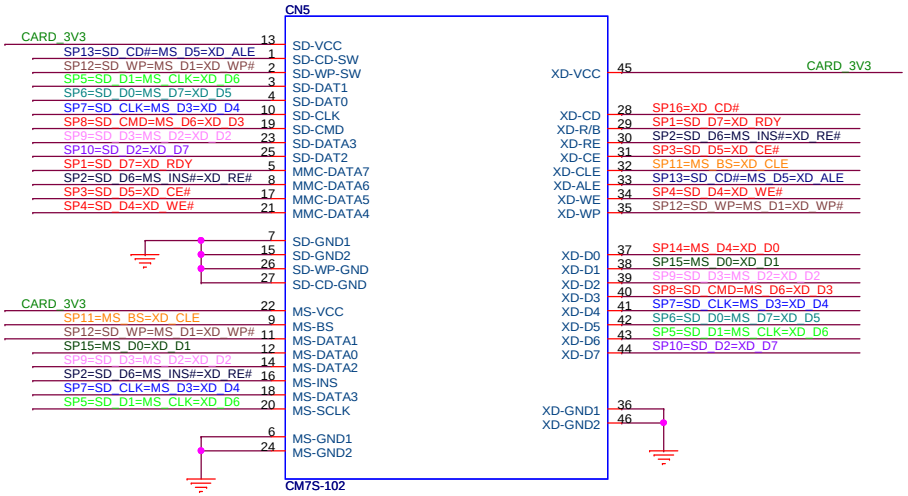
CARD READER CONNECTOR

XD,MMC 4.2/SD,MS/MSP
7 IN1 CARD READER

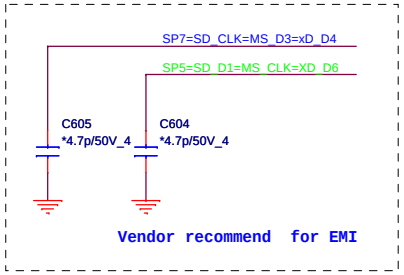
Share Pin

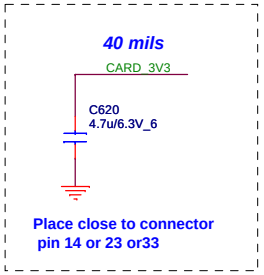
SP1	SD_D7		xD_RDY
SP2	SD_D6	MS_INS#	xD_RE#
SP3	SD_D5		xD_CE#
SP4	SD_D4		xD_WE#
SP5	SD_D1	MS_CLK	xD_D6
SP6	SD_D0	MS_D7	xD_D5
SP7	SD_CLK	MS_D3	xD_D4
SP8	SD_CMD	MS_D6	xD_D3
SP9	SD_D3	MS_D2	xD_D2
SP10	SD_D2		xD_D7
SP11		MS_BS	xD_CLE
SP12	SD_WP	MS_D1	xD_WP#
SP13	SD_CD#	MS_D5	xD_ALE
SP14		MS_D4	xD_D0
SP15		MS_D0	xD_D1
SP16			xD_CD#

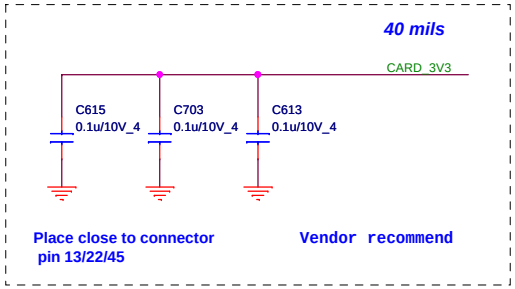




1 : DFHS44FR014
2 : DFHS44FR018





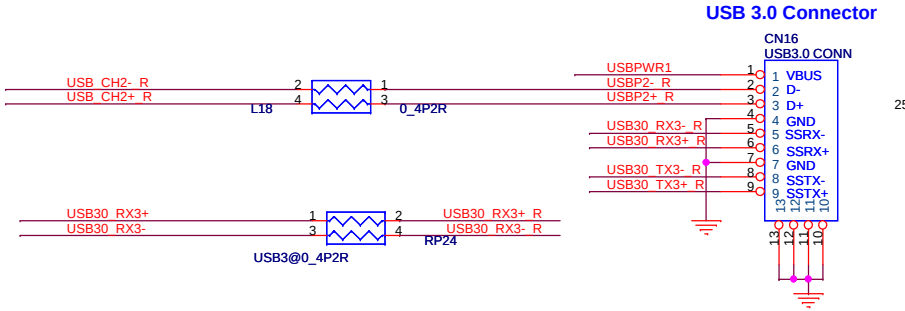


Quanta Computer Inc.

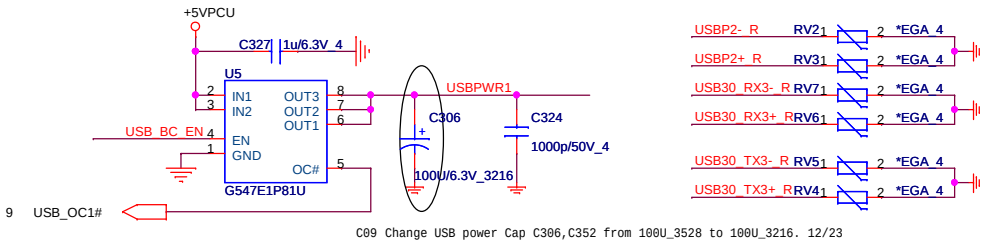
PROJECT : ZQS 45W

Size	Document Number	Rev
	CARD READER CONNECTOR	3C
Date: Wednesday, February 08, 2012	Sheet 30 of 46	

USB3.0/2.0

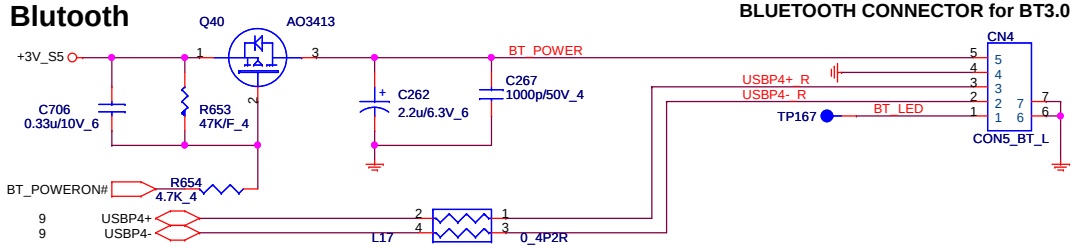


USB2.0 connector P/N: DFHS04FR487



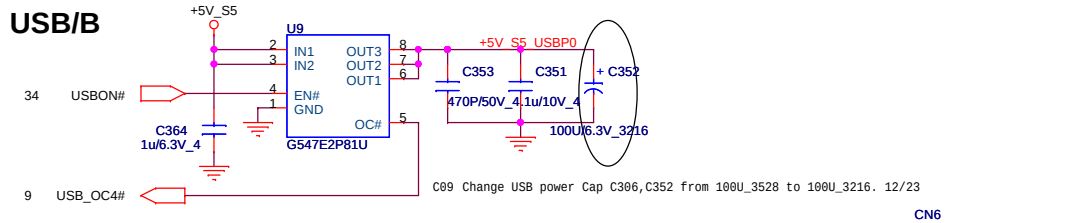
C09 Change USB power Cap C306,C352 from 100U_3528 to 100U_3216. 12/23

Blutooth

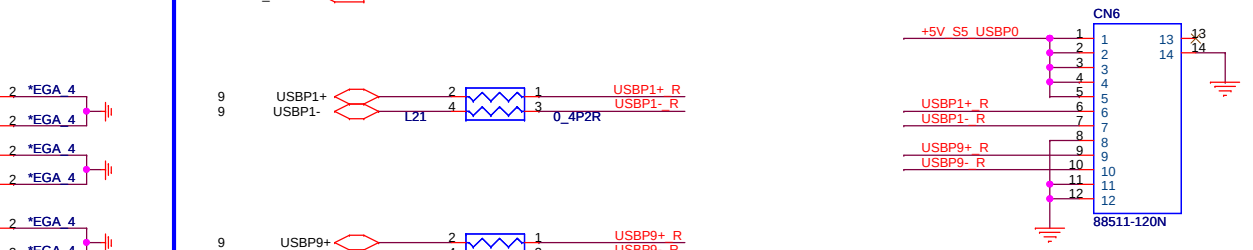


BLUETOOTH CONNECTOR for BT3.0

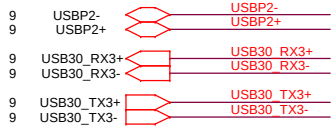
USB/B



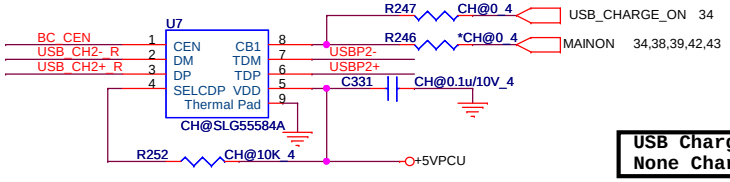
C09 Change USB power Cap C306,C352 from 100U_3528 to 100U_3216. 12/23

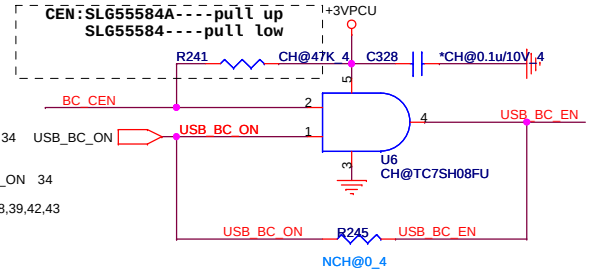


USB Charger



CB	SELCDP	Funcion
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)



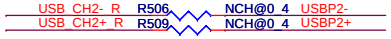


USB Charger -->CH@
None Charger--> NCH@

USB 3.0 Ra, Rb Stuff

Ra
Rb

For BA



Quanta Computer Inc.
PROJECT : ZQS 45W

Size	Document Number	Rev
	USB/ BT/CHARGER	3C
Date: Wednesday, February 08, 2012	Sheet 31 of 46	

Hole

MINI CARD NUT

HOLE7
*HG-C315D110P2

HOLE14
*HG-C315D110P2

HOLE2
*HG-C315D110P2

HOLE1
*H-C315D110P2

HOLE10
H-C217D106PT

HOLE12
*HG-C315D110P2

HOLE5
*h-c315l150d110p2

HOLE11
*ZQS-HOLE2

HOLE6
*HG-C315D110P2

HOLE13
*HG-C315D110P2

GPU NUT

HOLE17
H-C256D161PT

HOLE15
H-C256D161PT

FAN NUT

HOLE3
H-TC256BC315D161P2

HOLE16
*H-C236D165P2

HOLE19
*H-C236D165P2

HOLE18
*H-C236D165P2

C18 Change hole15, hole17 footprint to H-C256D161PT to h-c256d142pt. 12/30

PCH NUT

HOLE22
H-C224D123P2

HOLE20
H-C224D123P2

MINI PCIE

HOLE21
H-C236D65PT

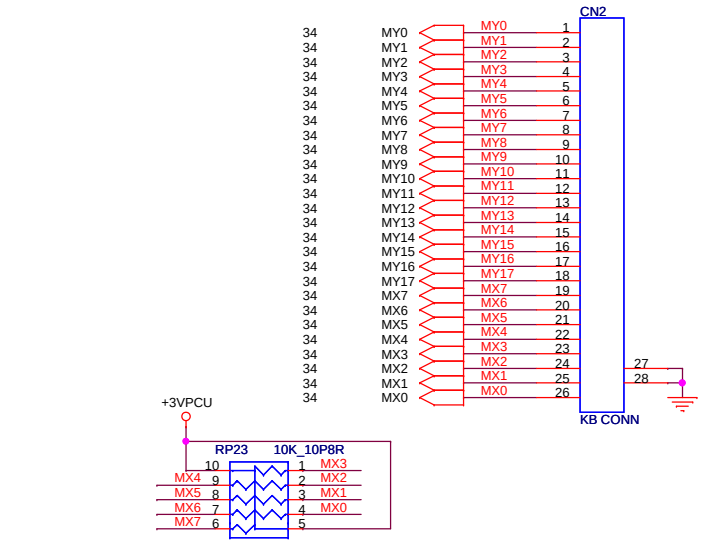
HOLE9
*H-TC433BC315D110P2

HOLE8
*ZQS-HOLE1

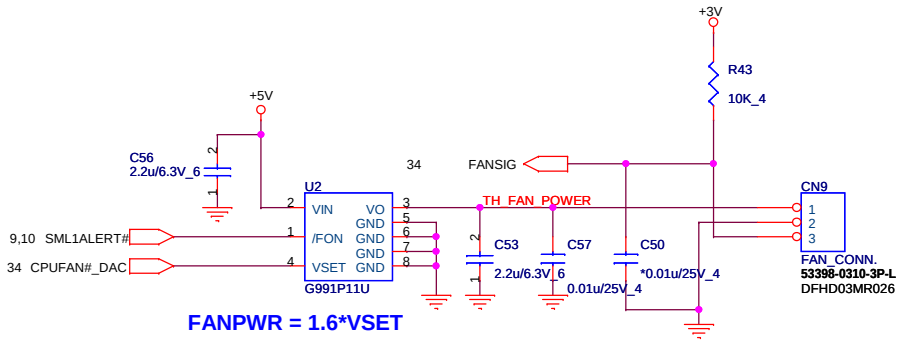
HOLE4
*O-ZQS-1

Quanta Computer Inc.		
PROJECT : ZQS 45W		
Size	Document Number: Hole	Rev: 3C
Date: Wednesday, February 08, 2012	Sheet 32 of 46	

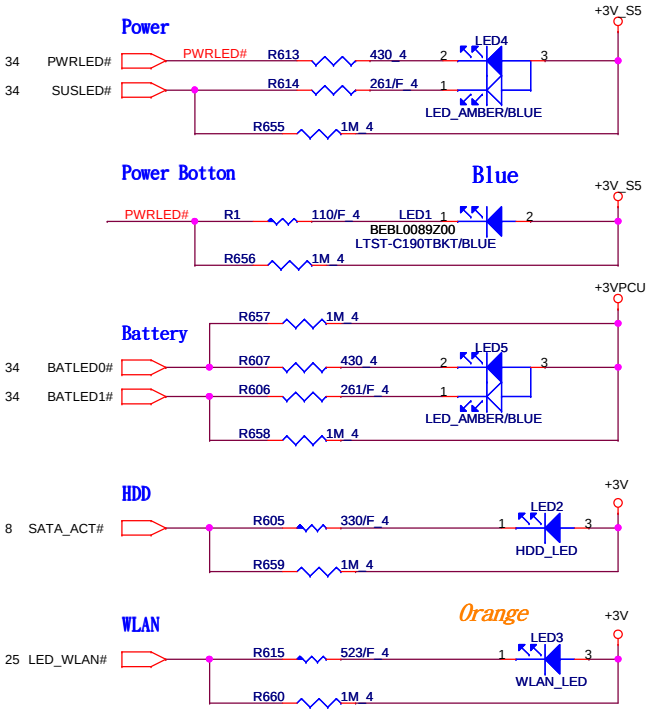
K/B



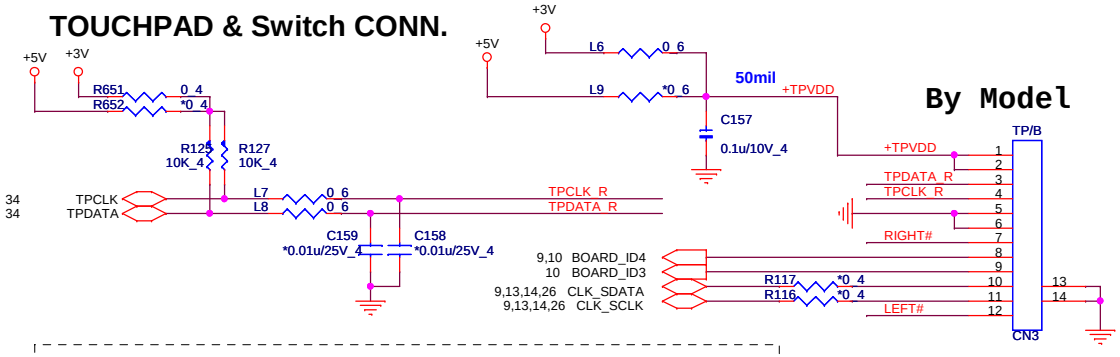
CPU FAN



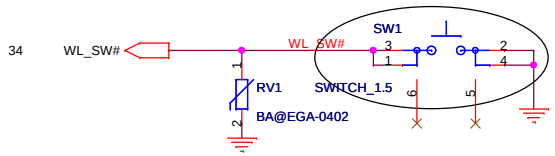
LED



TOUCHPAD & Switch CONN.



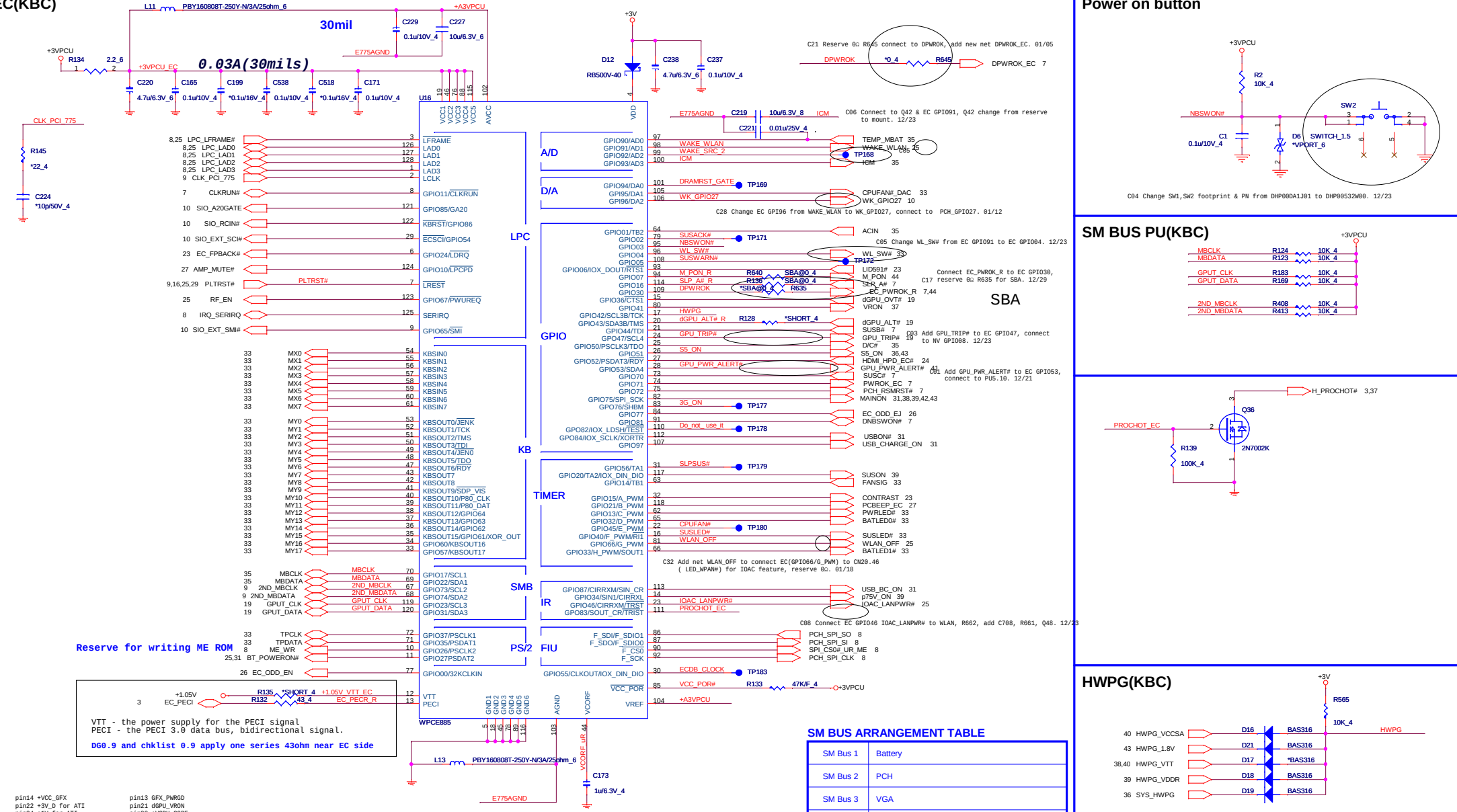
For BA WLAN function



C04 Change SW1,SW2 footprint & PN from DHP00DA1J01 to DHP00532W00. 12/23

Quanta Computer Inc.		
PROJECT : ZQS 45W		
Size	Document Number: KB/FAN/TP+FP/LED	Rev: 3C
Date: Wednesday, February 08, 2012	Sheet 33 of 46	

EC(KBC)



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA
SM Bus 4	HDMI

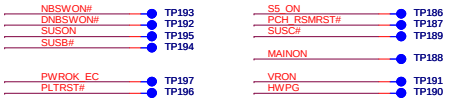
Power on button

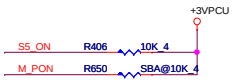
C04 Change SW1,SW2 footprint & PN from DHP00DA1J01 to DHP00532W00. 12/23

SM BUS PU(KBC)

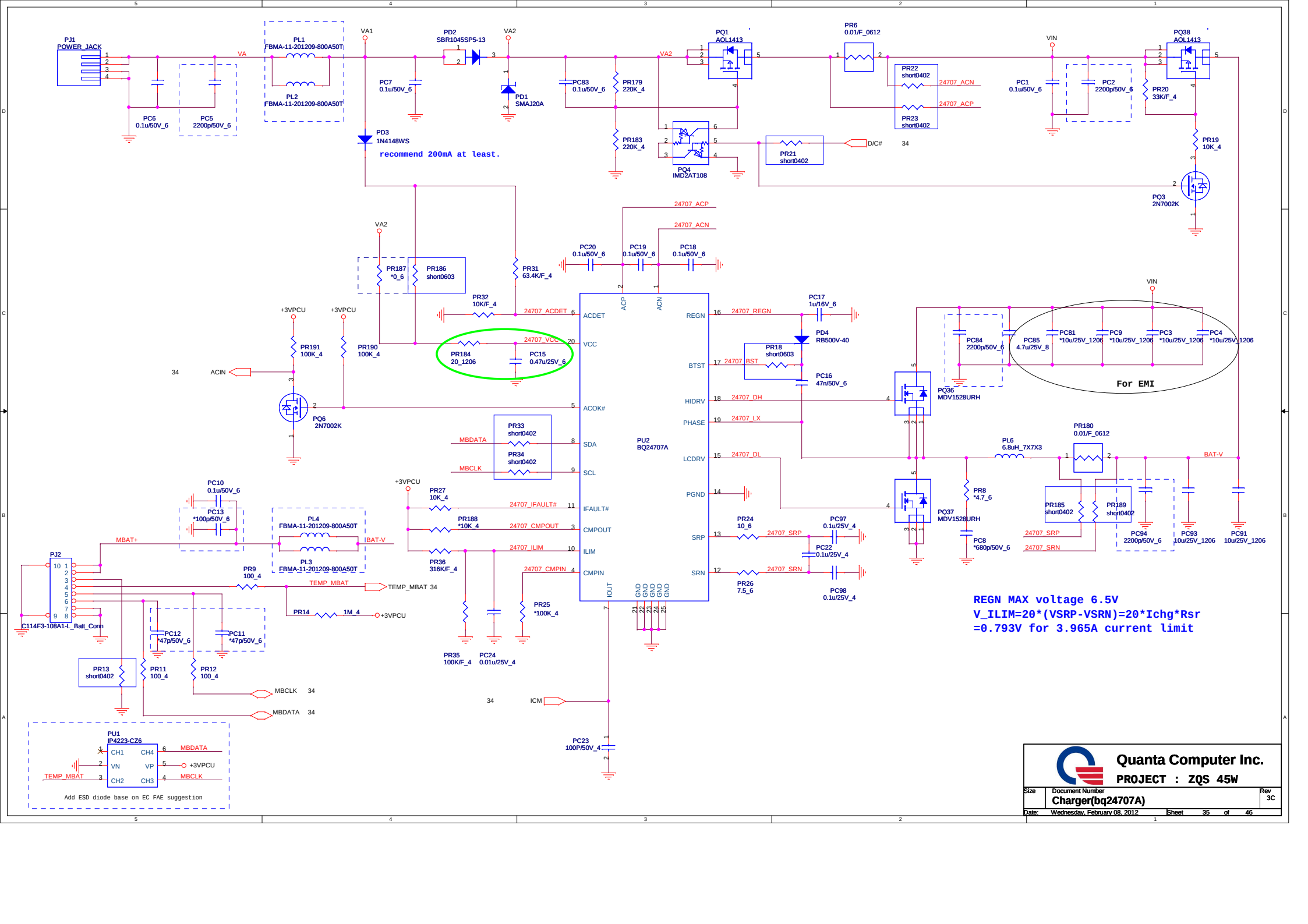
HWPG(KBC)

Power sequence





Quanta Computer Inc.			
PROJECT : ZQS 45W			
Size	Document Number		Rev
	WPCE885 & FLASH		3C
Date: Wednesday, February 08, 2012		Sheet 34 of 46	


PJ1
POWER_JACK
VA
PL1
FBMA-11-201209-800A50T
PL2
FBMA-11-201209-800A50T
VA1
PD2
SBR1045SP5-13
VA2
PD1
SMAJ20A
PC7
0.1u/50V_6
PC6
0.1u/50V_6
PC5
2200p/50V_6
PD3
1N4148WS
recommend 200mA at least.
PC83
0.1u/50V_6
PR179
220K_4
PR183
220K_4
PQ1
AOL1413
PQ4
IMD2AT108
PR6
0.01/F_0612
PR22
short0402
PR23
short0402
24707_ACN
24707_ACP
PR21
short0402
D/C#
34
VIN
PC1
0.1u/50V_6
PC2
2200p/50V_6
PQ38
AOL1413
PR20
33K/F_4
PR19
10K_4
PQ3
2N7002K
24707_ACP
24707_ACN
PC20
0.1u/50V_6
PC19
0.1u/50V_6
PC18
0.1u/50V_6
PR187
*0_6
PR186
short0603
PR31
63.4K/F_4
PR32
10K/F_4
24707_ACDET
24707_VCC
PR184
20_1206
PC15
0.47u/25V_6
PR191
100K_4
PR190
100K_4
ACIN
34
PQ6
2N7002K
+3VPCU
PU2
BQ24707A
ACDET
VCC
ACOK#
SDA
SCL
IFAULT#
CMPOUT
ILIM
CMPIN
IOUT
ACP
ACN
REGN
BTST
HIDRV
PHASE
LCDRV
PGND
SRP
SRN
GND
PC17
1u/16V_6
PD4
RB500V-40
PR18
short0603
24707_BST
PC16
47n/50V_6
24707_REGN
24707_DH
24707_LX
24707_DL
PQ36
MDV1528URH
PQ37
MDV1528URH
PC84
2200p/50V_6
PC85
4.7u/25V_8
PC81
*10u/25V_1206
PC9
*10u/25V_1206
PC3
*10u/25V_1206
PC4
*10u/25V_1206
For EMI
PR33
short0402
PR34
short0402
MBDATA
MBCLK
PC10
0.1u/50V_6
PC13
*100p/50V_6
PR27
10K_4
PR188
*10K_4
PR36
316K/F_4
24707_IFAULT#
24707_CMPOUT
24707_ILIM
24707_CMPIN
PR25
*100K_4
PR35
100K/F_4
PC24
0.01u/25V_4
PL4
FBMA-11-201209-800A50T
PL3
FBMA-11-201209-800A50T
IBAT-V
MBAT+
PJ2
C114F3-108A1-L_Batt_Conn
PR9
100_4
TEMP_MBAT
TEMP_MBAT 34
PR14
1M_4
+3VPCU
PC12
*47p/50V_6
PC11
*47p/50V_6
PR13
short0402
PR11
100_4
PR12
100_4
MBCLK 34
MBDATA 34
ICM
34
PC23
100P/50V_4
PU1
IP4223-CZ6
CH1
CH2
CH3
CH4
VN
VP
Add ESD diode base on EC FAE suggestion
PR24
10_6
PR26
7.5_6
PC97
0.1u/25V_4
PC22
0.1u/25V_4
PC98
0.1u/25V_4
PL6
6.8uH_7X7X3
PR180
0.01/F_0612
BAT-V
PR8
*4.7_6
PC8
*680p/50V_6
PR185
short0402
PR189
short0402
PC94
2200p/50V_6
PC93
10u/25V_1206
PC91
10u/25V_1206
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
Quanta Computer Inc.
PROJECT : ZQS 45W
Size
Document Number
Charger(bq24707A)
Rev
3C
Date: Wednesday, February 08, 2012
Sheet 35 of 46

MAIND → MAIND 15,39,43

SYS_SHDN# → SYS_SHDN# 3,19,43

Ven=7.23V

34 SYS_HWPG

+5VPCU
5 Volt +/- 5%
TDC : 6.63A
PEAK : 8.5A
OCP : 9A
Width : 260mil

+3VPCU
3.3 Volt +/- 5%
TDC : 7.8A
PEAK : 8.5A
OCP : 9A
Width : 220mil

PU6 RT8223P

Change 11/1

OCP:9A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=9-(2.525/2)=7.74A
Vth=7.74A*14mOhm=0.10832mV
R(Ilim)=(108.32mV*10)/10uA
~107K

OCP:9A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=9-(1.9/2)=8.05A
Vth=8.05A*14mOhm=112.7mV
R(Ilim)=(112.7mV*10)/10uA
=112.7K

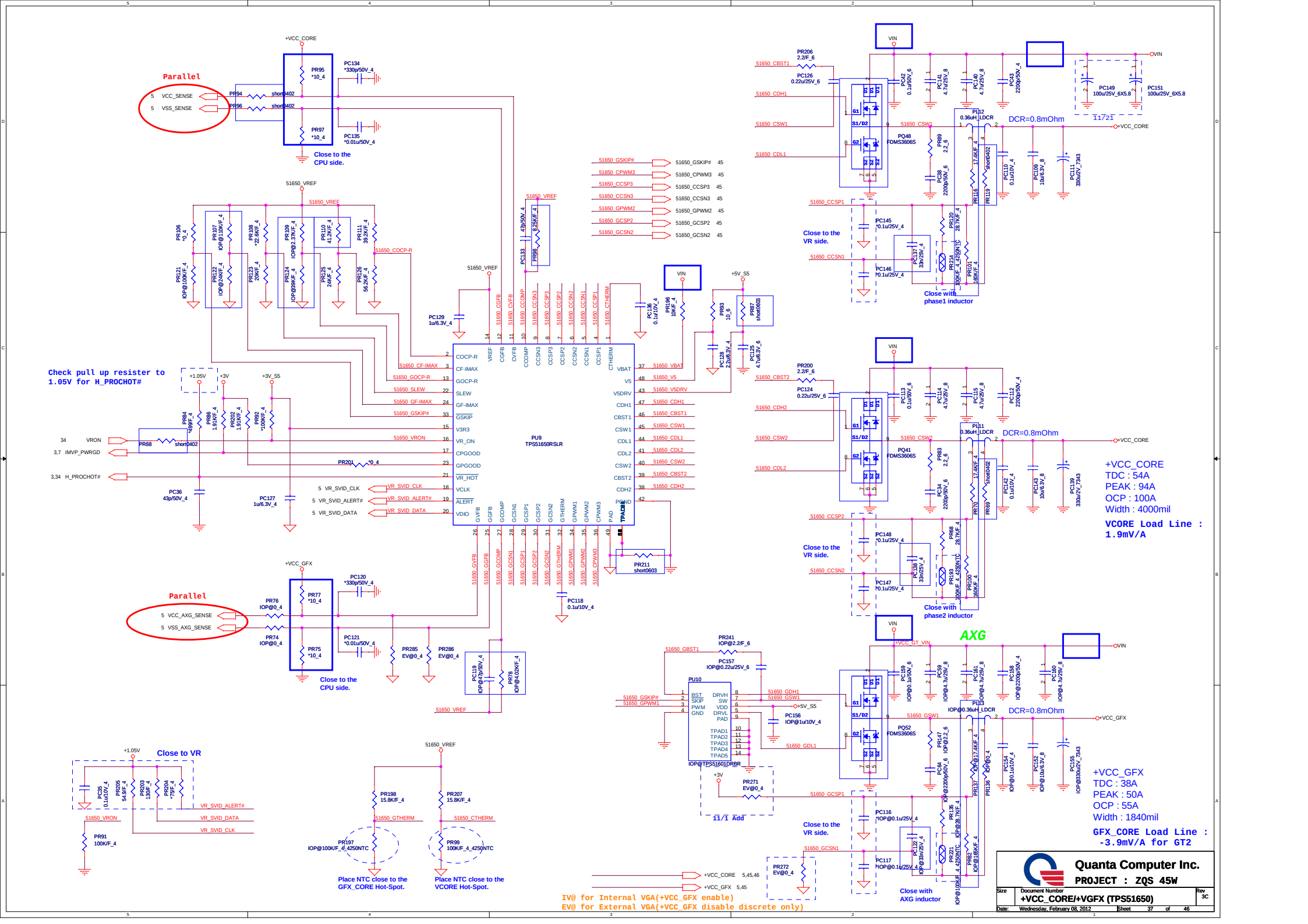
TDC : 2.63A
PEAK : 3.5A
Width : 120mil

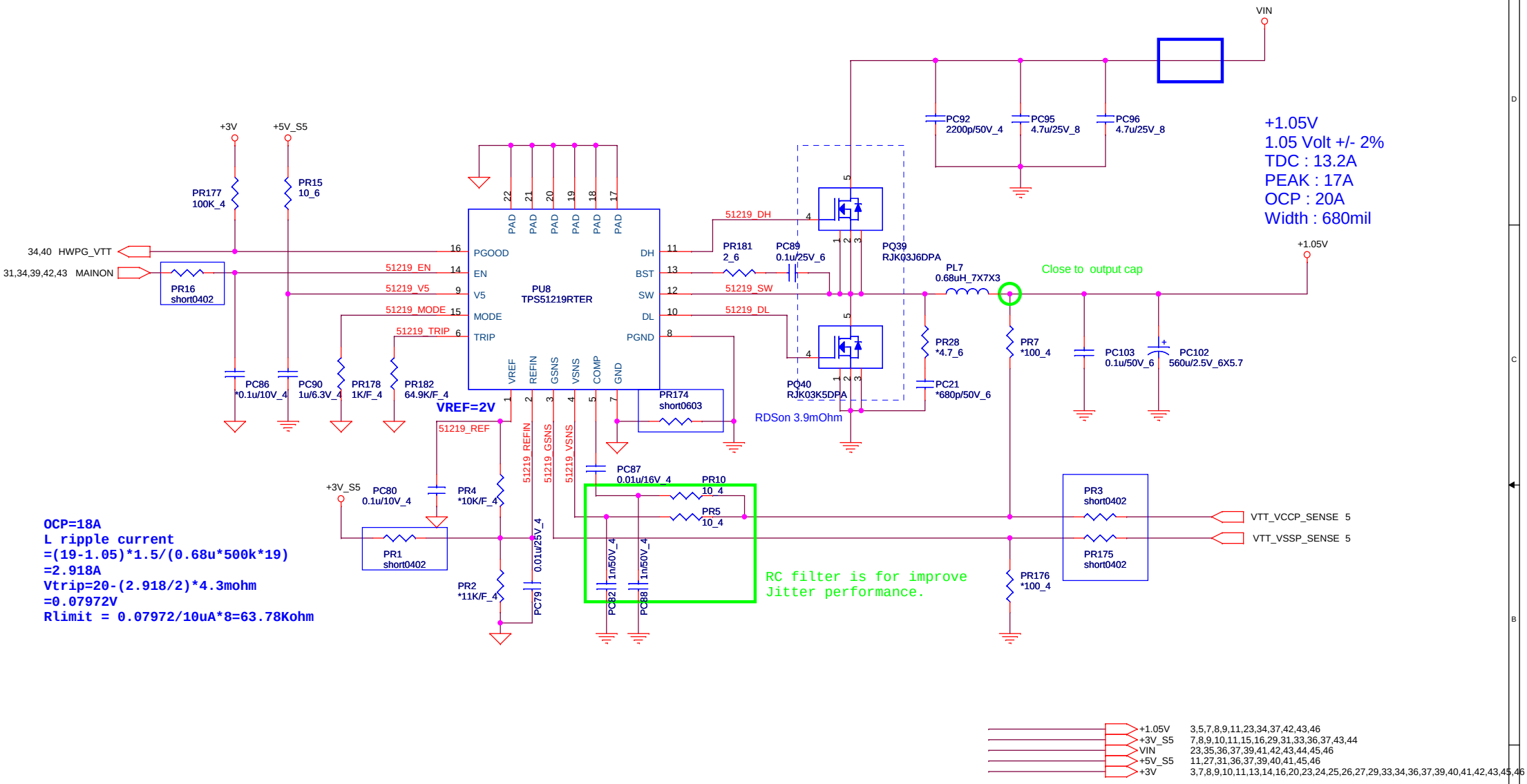
TDC : 3.45A
PEAK : 4.6A
Width : 140mil

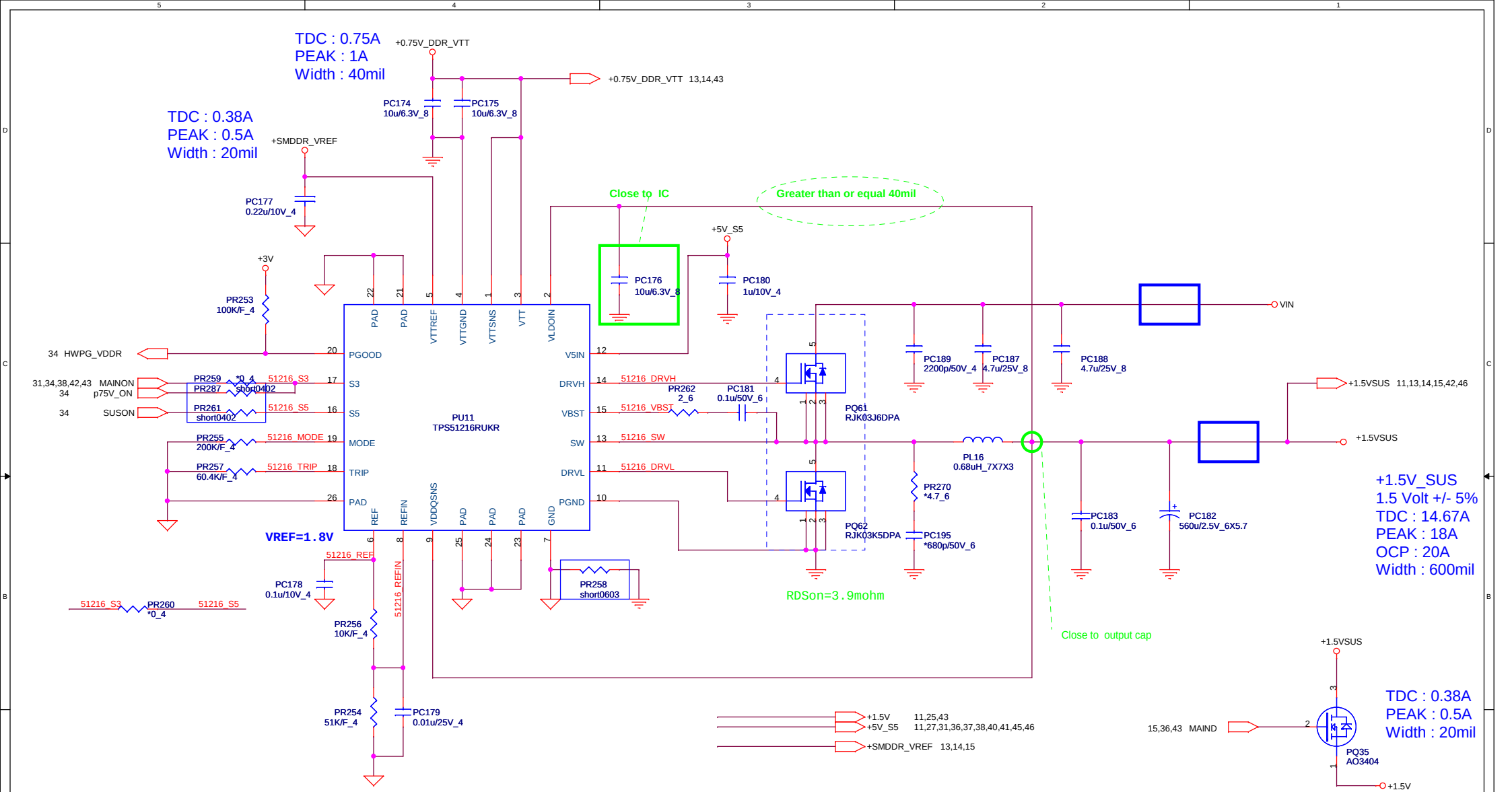
TDC : 3.2A
PEAK : 4.27A
Width : 140mil

TDC : 1.28A
PEAK : 1.7A
Width : 60mil

Quanta Computer Inc.	PROJECT : ZQS 45W	
Size	Document Number: SYSTEM 5V/3V (RT8223P)	Rev 3C
Date: Wednesday, February 08, 2012	Sheet 36 of 46	


Parallel
VCC_SENSE
VSS_SENSE
Close to the CPU side.
Check pull up resister to 1.05V for H_PROCHOT#
PU9
TPS51650RSLR
Parallel
VCC_AXG_SENSE
VSS_AXG_SENSE
Close to the CPU side.
Close to VR
PU10
IOP@TPS51601DRBR
Add
Close to the VR side.
Close with phase1 inductor
Close with phase2 inductor
Close with AXG inductor
DCR=0.8mOhm
AXG
+VCC_CORE
TDC : 54A
PEAK : 94A
OCP : 100A
Width : 4000mil
VCORE Load Line : 1.9mV/A
+VCC_GFX
TDC : 38A
PEAK : 50A
OCP : 55A
Width : 1840mil
GFX_CORE Load Line : -3.9mV/A for GT2
Place NTC close to the GFX_CORE Hot-Spot.
Place NTC close to the VCORE Hot-Spot.
IV@ for Internal VGA(+VCC_GFX enable)
EV@ for External VGA(+VCC_GFX disable discrete only)
Quanta Computer Inc.
PROJECT : ZQS 45W
+VCC_CORE/+VGFX (TPS51650)
Wednesday, February 08, 2012
37 of 46


VIN
+1.05V
1.05 Volt +/- 2%
TDC : 13.2A
PEAK : 17A
OCP : 20A
Width : 680mil
+3V
+5V_S5
PR177 100K_4
PR15 10_6
34,40 HWPG_VTT
31,34,39,42,43 MAINON
PR16 short0402
PU8 TPS51219RTER
PGOOD
EN
V5
MODE
TRIP
DH
BST
SW
DL
PGND
PAD
51219_DH
51219_EN
51219_V5
51219_MODE
51219_TRIP
51219_SW
51219_DL
PR181 2_6
PC89 0.1u/25V_6
PQ39 RJK03J6DPA
PQ40 RJK03K5DPA
PL7 0.68uH_7X7X3
Close to output cap
PC92 2200p/50V_4
PC95 4.7u/25V_8
PC96 4.7u/25V_8
PR28 *4.7_6
PC21 *680p/50V_6
PR7 *100_4
PC103 0.1u/50V_6
PC102 560u/2.5V_6X5.7
PC86 *0.1u/10V_4
PC90 1u/6.3V_4
PR178 1K/F_4
PR182 64.9K/F_4
VREF=2V
VREF
REFIN
GSNS
VSNS
COMP
GND
PR174 short0603
RDSon 3.9mOhm
51219_REF
51219_REFIN
51219_GSNS
51219_VSNS
PC87 0.01u/16V_4
PR10 10_4
PR5 10_4
PC80 0.1u/10V_4
PR4 *10K/F_4
PR1 short0402
PR2 *11K/F_4
PC79 0.01u/25V_4
PC82 1n/50V_4
PC88 1n/50V_4
PR3 short0402
PR175 short0402
PR176 *100_4
VTT_VCCP_SENSE 5
VTT_VSSP_SENSE 5
OCP=18A
L ripple current
=(19-1.05)*1.5/(0.68u*500k*19)
=2.918A
Vtrip=20-(2.918/2)*4.3mohm
=0.07972V
Rlimit = 0.07972/10uA*8=63.78Kohm
RC filter is for improve
Jitter performance.
+1.05V 3,5,7,8,9,11,23,34,37,42,43,46
+3V_S5 7,8,9,10,11,15,16,29,31,33,36,37,43,44
VIN 23,35,36,37,39,41,42,43,44,45,46
+5V_S5 11,27,31,36,37,39,40,41,45,46
+3V 3,7,8,9,10,11,13,14,16,20,23,24,25,26,27,29,33,34,36,37,39,40,41,42,43,45,46
Quanta Computer Inc.
PROJECT : ZQS 45W
Size
Document Number
+1.05V (TPS51219)
Rev 3C
Date: Wednesday, February 08, 2012
Sheet 38 of 46



OCP=20A
L ripple current
=(19-1.5)*1.5/(0.68u*400k*19)
=5.079A
Vtrip=20-(5.079/2)*4.3mohm
=0.07508V
Rlimit=0.07508/10uA*8=60.063Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZQS 45W

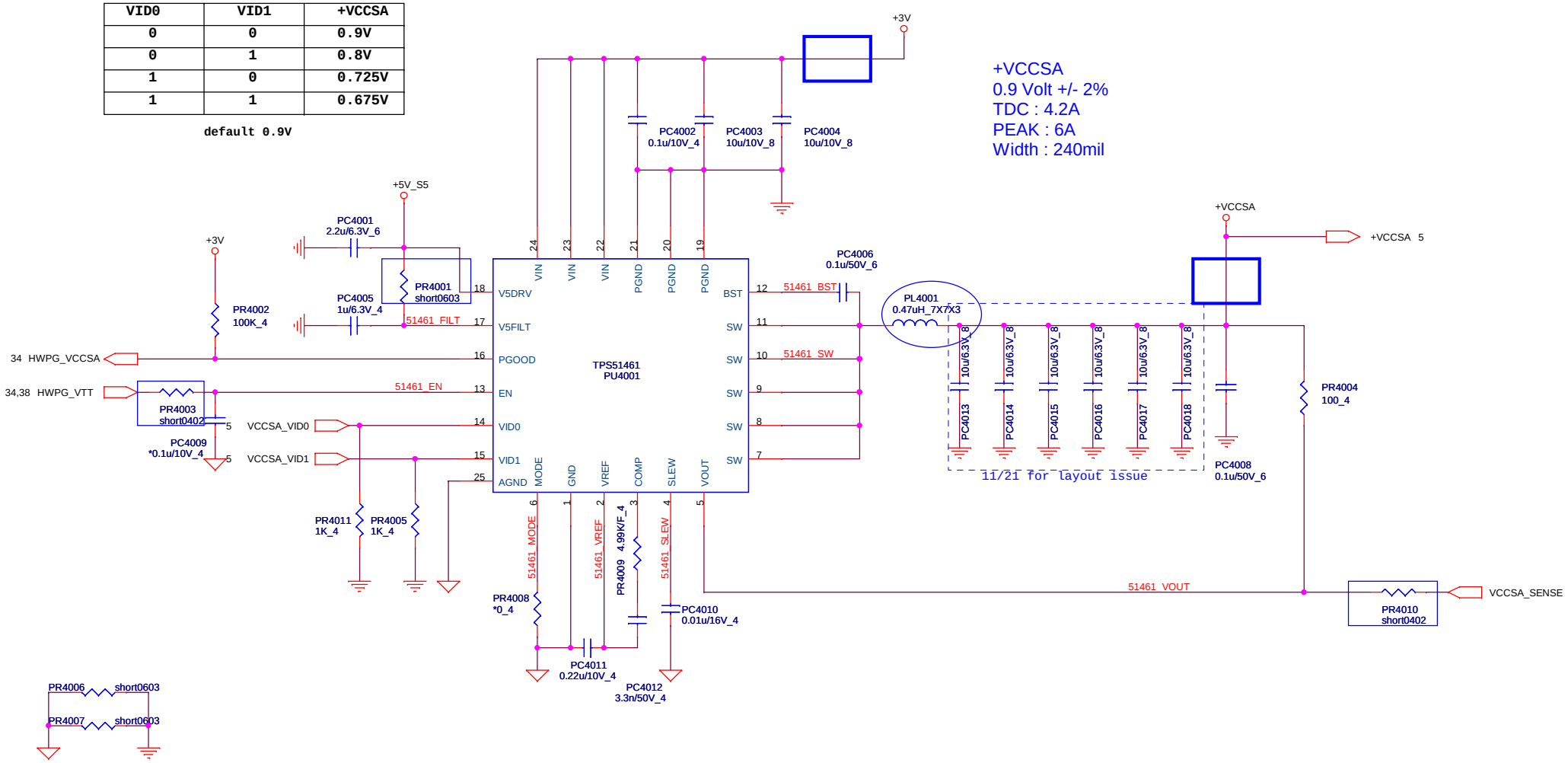
Size	Document Number	Rev
	DDR 1.5V(TPS51216)	3C

Date: Wednesday, February 08, 2012 Sheet 39 of 46

VID0	VID1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V

+VCCSA
0.9 Volt +/- 2%
TDC : 4.2A
PEAK : 6A
Width : 240mil



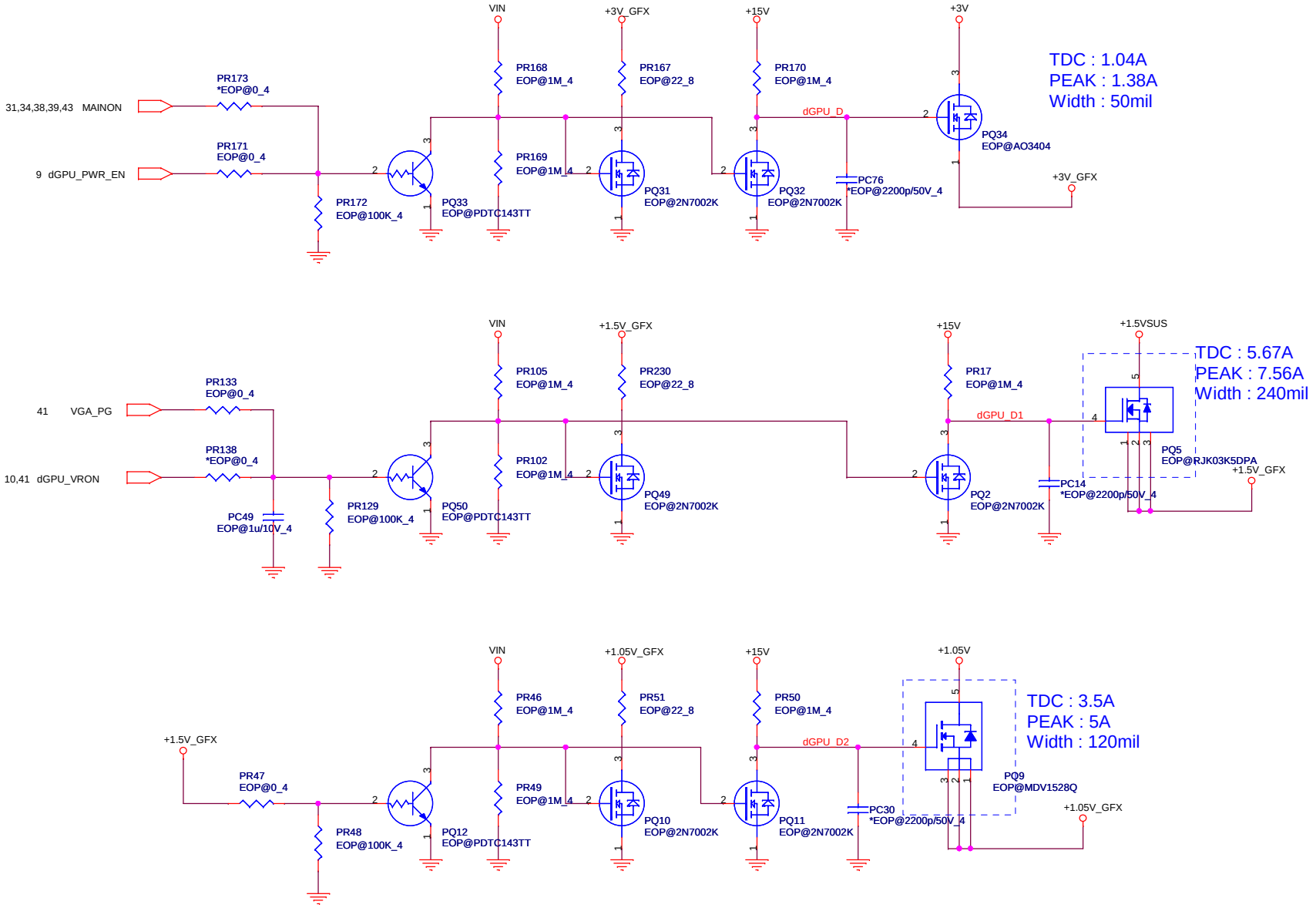
Quanta Computer Inc.		
PROJECT : ZQS 45W		
Size	Document Number: VCCSA(TPS51461)	Rev: 3C
Date: Wednesday, February 08, 2012	Sheet 40 of 46	

N13P-GL QS sample, boot up voltage set to 0.95V. VID2,3,5
N13P-GS ES sample, boot up voltage set to 0.90V. VID4,5
N13M-GS ES sample, boot up voltage set to 0.90V. VID4,5

VID							VDAC(V)
GPU SKU	6	5	4	3	2	1	0	
N13P-GL	0	1	0	1	1	0	0	0.9500
N13P/M-GS	0	1	1	0	0	0	0	0.9000

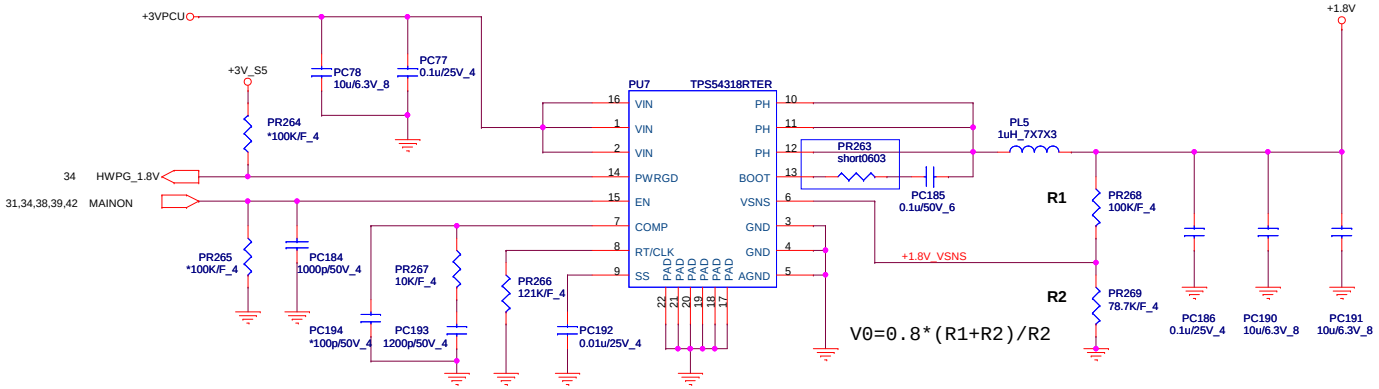
+3V_GFX
default 1.1V
PR212 EOP_VID0_H@10K/F_4 H_VID0
PR216 EOP_VID1_H@10K/F_4 H_VID1
PR220 EOP_VID2_H@10K/F_4 H_VID2
PR225 EOP_VID3_H@10K/F_4 H_VID3
PR228 EOP_VID4_H@10K/F_4 H_VID4
PR130 EOP_VID5_H@10K/F_4 H_VID5
EOP_VID5_L@10K/F_4 PR235
EOP_VID4_L@10K/F_4 PR231
EOP_VID3_L@10K/F_4 PR226
EOP_VID2_L@10K/F_4 PR222
EOP_VID1_L@10K/F_4 PR218
EOP_VID0_L@10K/F_4 PR213
+3V
PR128 *EOP@10K/F_4
PR217 EOP@100K/F_4
PR146 EOP@56_4
PR139 EOP@100K/F_4
+5V_S5
PC47 EOP@2.2u/10V_6
42 VGA_PG
19 GPU_DPRSLPVR
PR232 *EOP@100K/F_4
PR143 EOP@2.2K_4
PR224 EOP@100K/F_4
10,42 dGPU_VRON
PR223 EOP@0_4
34 GPU_PWR_ALERT#
GPU_PWR_ALERT#
C01 Add GPU_PWR_ALERT# to EC GPIO53, connect to PU5.10. 12/21
19 GPU_VID0 PR113 EOP@0_4 H_VID0
19 GPU_VID1 PR117 EOP@0_4 H_VID1
19 GPU_VID2 PR127 EOP@0_4 H_VID2
19 GPU_VID3 PR131 EOP@0_4 H_VID3
19 GPU_VID4 PR134 EOP@0_4 H_VID4
19 GPU_VID5 PR115 EOP@0_4 H_VID5
PU5 EOP@TPS51728RHAR
PGD 33
PG 34
51728_PCNT PCNT 13
SLP 12
51728_EN EN 35
THAL 10
VID0 20
VID1 19
VID2 18
VID3 17
VID4 16
VID5 15
VID6 14
51728_DROOP PC52 EOP@68p/50V_4
PC51 EOP@1200p/50V_4 PR140 EOP@8.2K/F_4
DROOP 39
51728_VREF VREF 40
51728_V5FILT +3V
PC56 EOP@0.22u/10V_6 PR233 EOP@113K/F_4
PR229 *EOP@0_4 PR114 *EOP@0_4 PR132 EOP@0_4
51728_SLEW PR227 *EOP@316K/F_4 SLEW 37
51728_TONSEL
PR145 EOP@11.8K/F_4 PR234 EOP@100K/F_4_3540NTC THRM 9
Place NTC close to the GPU Hot-Spot.
V5IN 26
DRVH2 30 51728_DRVH2
VBST2 29 51728_VBST2
LL2 28 51728_LL2
DRVL2 27 51728_DRVL2
CSP2 3 51728_CSP2
CSN2 4 51728_CSN2
DRVH1 21 51728_DRVH1
VBST1 22 51728_VBST1
LL1 23 51728_LL1
DRVL1 24 51728_DRVL1
CSP1 6 51728_CSP1
CSN1 5 51728_CSN1
PGND 25
TONSEL 36 51728_TONSEL
TRIPSEL 31 51728_TRIPSEL
OSRSEL 32 51728_OSRSEL
PR118 EOP@0_4
PR210 *EOP@0_4
PU 1
V5FILT 38 51728_V5FILT
TPAD 39
PC50 EOP@2.2u/10V_6
PR219 *EOP@0_4
PR215 EOP@0_4
+3V
PR112 *EOP@0_4
VFB 8
GFB 7
IMON 11
PwPd 41
GND 2
+VGACORE
PR238 EOP@100_4
PR144 EOP@0_4
16 GPUVCC_SENSE
16 GPUVSS_SENSE
PR142 EOP@0_4
PR239 EOP@100_4
Close to the GPU side.
51728_VFB
51728_GFB
51728_IMON
PR141 EOP@11.3K/F_4
PC54 EOP@3300p/50V_4
PR240 EOP@0_8
PC58 EOP@1n/50V_4
PC57 EOP@1n/50V_4
51728_VBST2
PR103 EOP@2.2/F_6
PC45 EOP@0.22u/25V_6
51728_DRVH2
PR208 *EOP@10K/F_4
51728_LL2
PQ43 EOP@AON6414AL
PL10 EOP@0.36uH DCR=1.1mOhm
VIN
PC41 EOP@0.1u/50V_6
PC130 EOP@4.7u/25V_8
PC39 EOP@4.7u/25V_8
PC131 EOP@2200p/50V_4
PC150 EOP@100u/25V_6X5.8
+VGACORE
51728_DRVL2
PQ25 *EOP@AON6780
PQ45 EOP@AON6780
PR85 EOP@2.2_6
PC37 EOP@2200p/50V_4
PR79 EOP@17.8K/F_4
PR71 EOP@0_4
PC107 EOP@0.1u/10V_4
PC123 EOP@10u/6.3V_8
PC104 EOP@330u/2V_7343
51728_CSP2
PC60 *EOP@0.1u/25V_4
PC55 EOP@0.022u/25V_4
51728_CSN2
PC61 *EOP@0.1u/25V_4
PR73 EOP@27.4K/F_4
PR237 EOP@200K/F_4
PR195 EOP@100K/F_4_3540NTC
Close to the VR side.
+VGPU_CORE (N13P-GS)
Countinue current:50A
Peak current:55A
OCP minimum 60A
Loadline=0mV/A
PR104 EOP@2.2/F_6
51728_VBST1
PC46 EOP@0.22u/25V_6
51728_DRVH1
PR209 *EOP@10K/F_4
51728_LL1
PQ46 EOP@AON6414AL
PL9 EOP@0.36uH DCR=1.1mOhm
VIN
PC44 EOP@0.1u/50V_6
PC48 EOP@4.7u/25V_8
PC144 EOP@4.7u/25V_8
PC132 EOP@2200p/50V_4
PC153 EOP@100u/25V_6X5.8
+VGACORE 20
+VGACORE
51728_DRVL1
PQ26 *EOP@AON6780
PQ44 EOP@AON6780
PR90 EOP@2.2_6
PC40 EOP@2200p/50V_4
PR80 EOP@17.8K/F_4
PR72 EOP@0_4
PC108 EOP@0.1u/10V_4
PC106 EOP@10u/6.3V_8
PC105 EOP@330u/2V_7343
51728_CSP1
PC63 *EOP@0.1u/25V_4
PC53 EOP@0.022u/25V_4
51728_CSN1
PC62 *EOP@0.1u/25V_4
PR81 EOP@27.4K/F_4
PR236 EOP@200K/F_4
PR199 EOP@100K/F_4_3540NTC
Close to the VR side.

Quanta Computer Inc.
PROJECT : ZQS 45W
Size
Document Number
VGPU Core (TPS51728)
Rev 3C
Date: Wednesday, February 08, 2012
Sheet 41 of 46

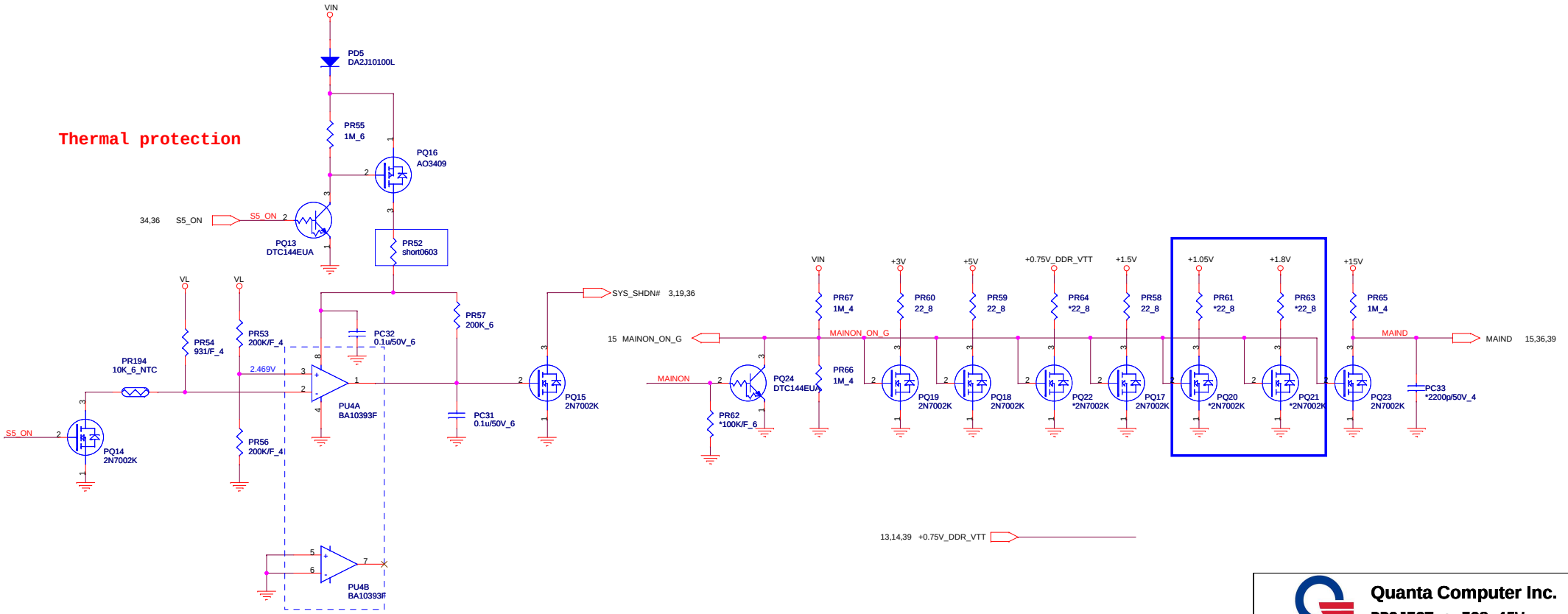


Quanta Computer Inc.		
PROJECT : ZQS 45W		
Size	Document Number: GPU_PWR	Rev: 3C
Date: Wednesday, February 08, 2012	Sheet 42 of 46	

+1.8V
1.8 Volt +/- 5%
TDC : 1.61A
PEAK : 2A
Width : 60mil

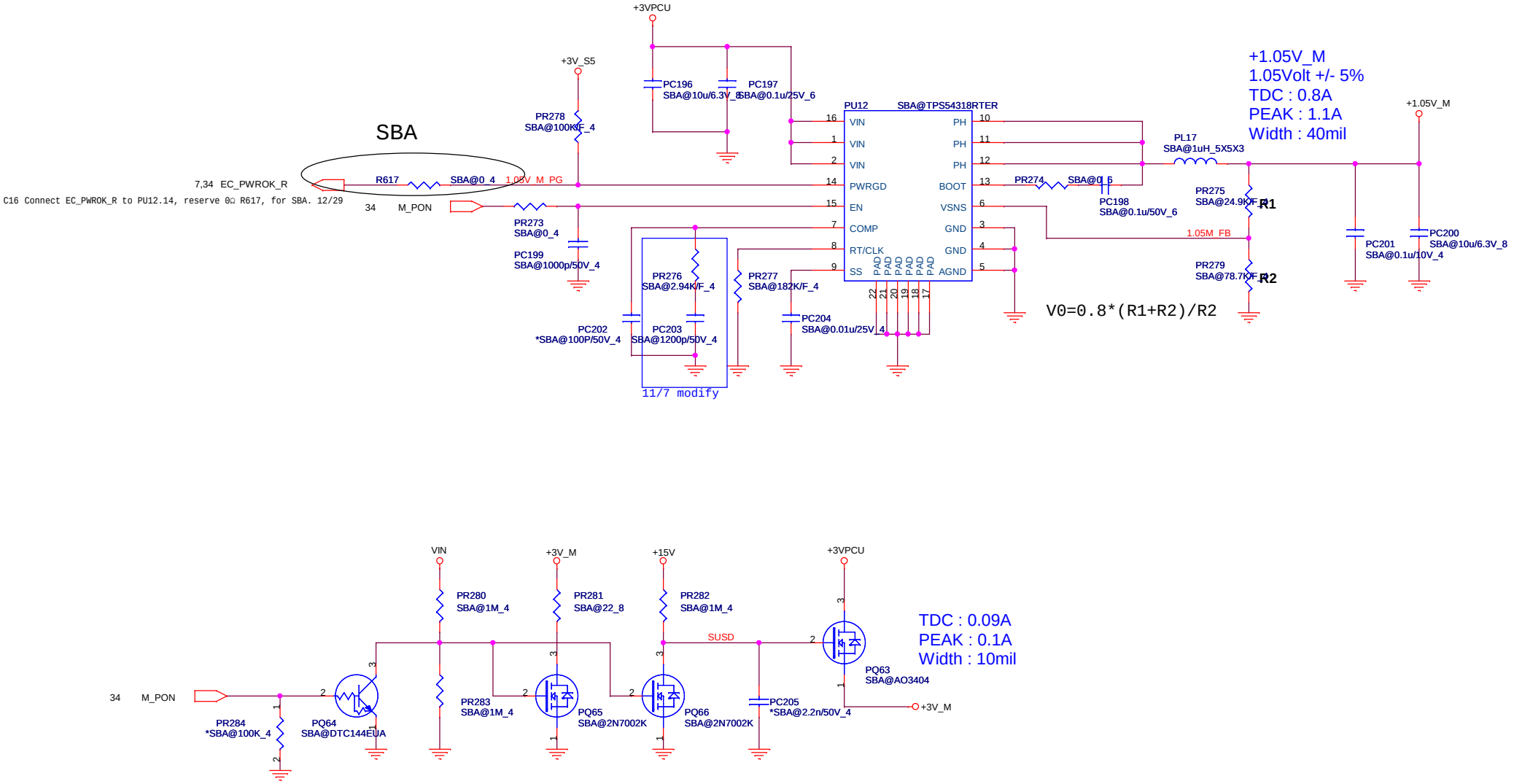


Thermal protection

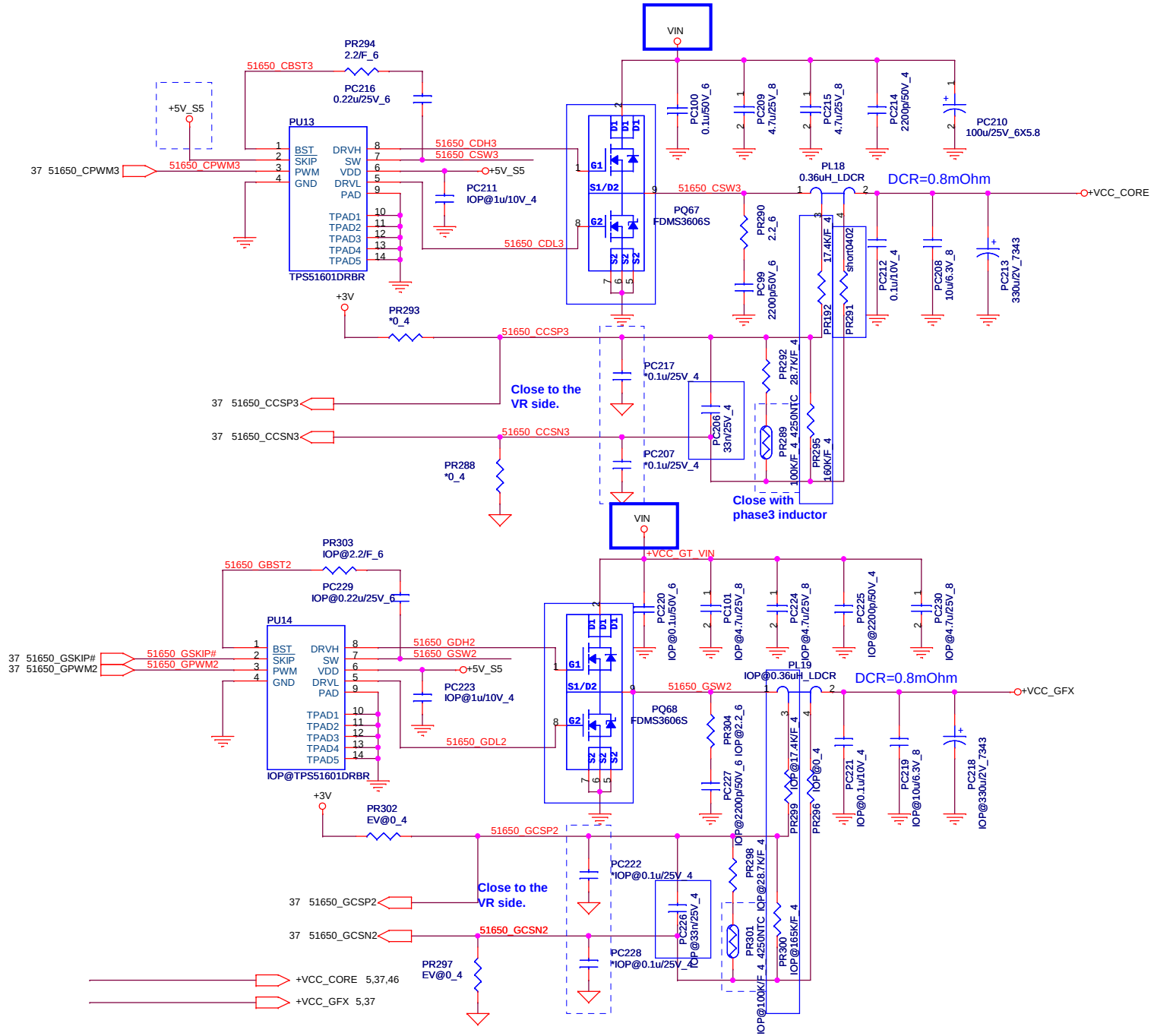


For EC control thermal protection (output 3.3V)

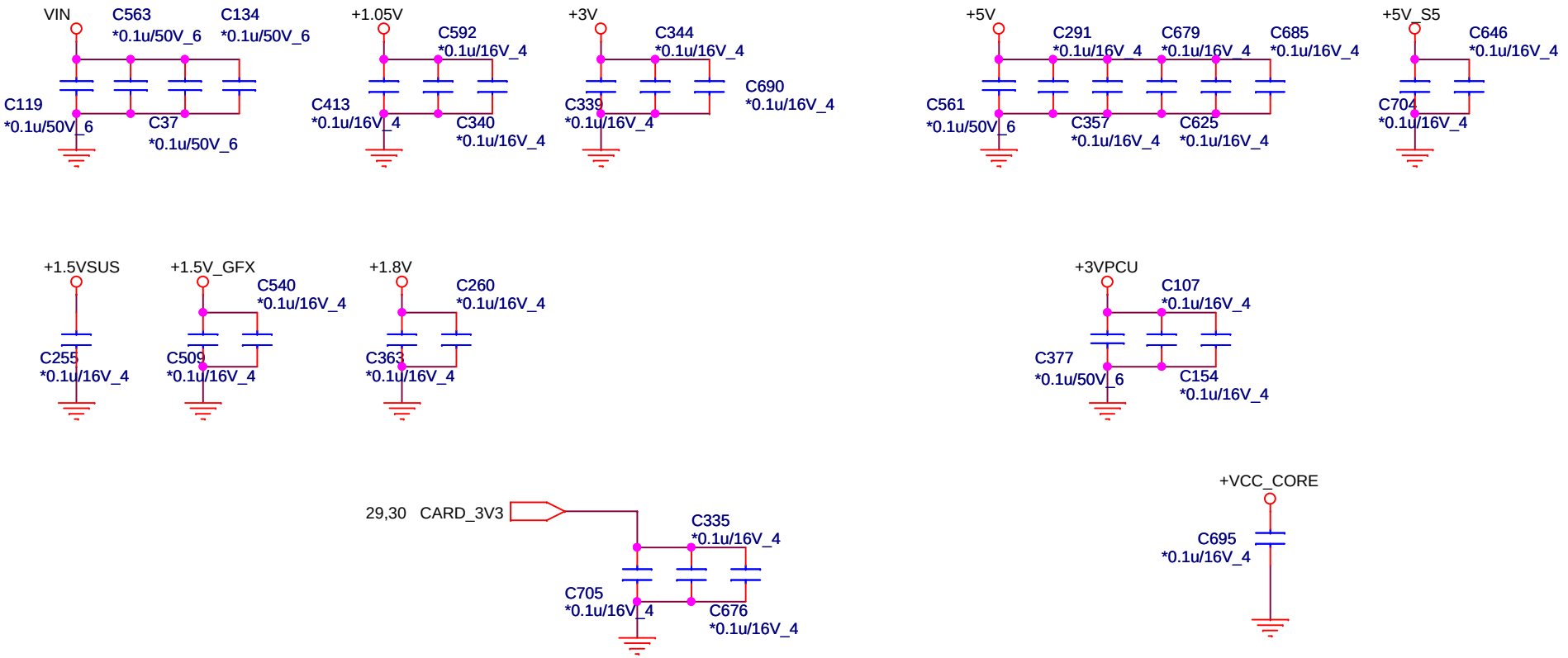
Quanta Computer Inc.		
PROJECT : ZQS 45W		
Size	Document Number: +1.8V/Discharge/Thermal	Rev 3C
Date: Wednesday, February 08, 2012	Sheet 43 of 46	



Quanta Computer Inc.		
PROJECT : ZQS 45W		
Size	Document Number: +1.05V_M/+3V_M	Rev: 3C
Date: Wednesday, February 08, 2012	Sheet 44 of 46	



Quanta Computer Inc.		
PROJECT : ZQS 45W		
Size	Document Number: +VCC_CORE/+VGFX (TPS51650)	Rev: 3C
Date: Wednesday, February 08, 2012	Sheet 45 of 46	



Quanta Computer Inc.

PROJECT : ZQS 45W

Size	Document Number	Rev
	EMI	3C
Date: Wednesday, February 08, 2012	Sheet 46 of 46	

Model

ZQS MB

REV	CHANGE LIST
C	C01 Add GPU_PWR_ALERT# to EC GPIO53, connect to PU5.10. 12/21 C02 Change R483,R486,R492,R491,R498,R487,R496,R494 from 590 Ω to 510Ω, and mount HDMI R194,R205,R202,R212 120Ω at optimus sku for EMI. 01/17 C03 Add GPU_TRIP# to EC GPIO47, connect to NV GPIO08. 12/23 C04 Change SW1,SW2 footprint & PN from DHP00DA1J01 to DHP00532W00. 12/23 C05 Change WL_SW# from EC GPIO91 to EC GPIO04. 12/23 C06 Connect to Q42 & EC GPIO91, Q42 change from reserve to mount. 12/24 C07 Add R608 and reserve +1.5V to WLAN. 12/23 C08 Connect EC GPIO46 IOAC_LANPWR# to WLAN, R662, add C708, R661, Q48, reserve R316. 12/23 C09 Change USB power Cap C306,C352 from 100U_3528 to 100U_3216. 12/23 C10 Change R328 from 47Ω to 0Ω, for hall sensor ESD & shudown issue. 12/28 C11 Change R641 from reserve to mount per EC request. 12/27 C12 Change Q47 from 2N7002 to DTC144EUA, change Q47.2 from +3V_GFX to PEGX_RST#, connect GPU_TRPI# to Q47, add 0Ω R142,R237. For GPU thermal detect. 12/27 C13 Change R393 from reserve to mount. dGPU_PWROK pull high. 12/27 C14 Change R234 from mount to reserve. WAKE_WLAN function on. 12/27 C15 Add 0Ω R609 to net EC_PWROK_R. SBA 12/29 C16 Connect EC_PWROK_R to PU12.14, reserve 0Ω R617. SBA 12/29 C17 Connect EC_PWROK_R to EC GPIO30, reserve 0Ω R635. SBA 12/29 C18 Change hole15, hole17 footprint to H-C256D161PT to h-c256d142pt. 12/30 C19 R382 change from 30.1 KΩ to pull down 45.3KΩ for N13P-GS & GT strap 4. 01/04 C20 Change R230 from shortpad to 0Ω, add 0Ω R636 connect to +3VPCU. 01/05 C21 Reserve 0Ω R645 connect to DPWROK, add new net DPWROK_EC. 01/05 C22 Change R220 from shortpad to 0Ω, reserve 0Ω R646 connect to DPWROK_EC. 01/05 C23 Change L40 footprint from L2x1_6-1 to RC0805. 01/09 C24 Change mini pcie power source from +3V_S5 to +3VPCU. 01/12 C25 Change CN20 pin 30 &28 from CLK_SDATA & CLK_SCLK to SMB_PCH_CLK & SMB_PCH_DAT, reserve 0Ω R663,R664. 1/12 C26 Mount R314, R315 for mini card debug. 01/12 C27 Add Q49 connect PCIE_CLKREQ5# to CN20.7. 01/12 C28 Change EC GPI96 from WAKE_WLAN to WK_GPIO27, connect to PCH_GPIO27. 01/12 C29 Reserve FDI Disabling (Discrete Only), add R665,R666,R667,R668,R669. 1/13 C30 Change U22 PLTRST# power source from +3V_S5 to +3V. 01/17 C31 Change DGPU_POK4 from +1.05V_GFX to +1.5V_GFX, DGPU_POK2 from +1.5V_GFX to +1.05V_GFX for possibly floating issue. 01/17 C32 Add net WLAN_OFF to connect EC(GPIO66/G_PWM) to CN20.46 (LED_WPAN#) for IOAC feature, mount 0Ω R670. 01/18 C33 R73 change from 34.8 KΩ to pull down 4.99KΩ for N13P-GS & GT STRAP1. 01/17 C34 Mount Q12 at SBA sku. 01/17 C35 Reserve 0.1u capacitor C698 to EC_PWROK_R. 01/17 C36 Remove R308 reserved 10KΩ for LED_WLAN# pull high +3V. 01/31 C37 Add Q50 connect to BT_POWERON# for WLAN ON/OFF function, pull up BT_PWRON by 10KΩ R671 to +WL_VDD, reserve 10KΩ R672 to +3V. 01/31 C38 Change C562, C564 from 220U to 100U for cost down. 02/08

Quanta Computer Inc.
PROJECT : ZQS 45W

Size: Document Number: Change list — Rev: 3C
Date: Wednesday, February 08, 2012 Sheet 47 of 47

DOC NO.					
PROJECT MODEL :	ZQS	APPROVED BY:		DATE:	2011/12/23
PART NUMBER:		DRAWING BY:		REVISON:	C