A880GM-M6 Rev:1.0

SCHEMATICS TABLE:

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REVISION HISTORY:

Rev	Date	Notes
A	2008-11-04	INITIAL RELEASE
1.0	2009-03-11	1. Change CPU Side Band Interface Connection. 2. Change CLK IC to ICS9LPRS471CS. 3. Modify CPU Vcore PWROK input level. 4. Change VCC_SB's GPIO Control Pin. 5. Modify HDMI/DVI switch and Hot-plug detection circuit. 6. Remove U10 which for the JMB362 1.8V, Direct Connect to VCC1.8. 7. Change Audio output Capacitance. 8. Change ATX12V 4 Pin to 8 Pin.
1.0	2009-06-08	1. Change the Model name to A785GM-M. 2. Add R33 for Plug only HDMI / DVI will be leakage to VCC3. 3. Change the PI3HDMI412FT-BZHES to ASM1445:(02-342-445070), Because of Leakage from the PI3HDMI412FT output differential line.
1.1	2009-09-24	Add NB_rst to LDT_RST for ACC.
1.0	2010-04-19	Change the title to A880GM-M6 V1.0.

IMPORTANT NOTES ABOUT THIS SCHEMATIC

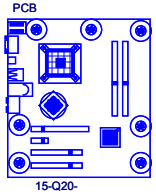
DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.

3) DESIGN NOTES in red are critical, and must be understood and followed.



PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

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Title: Cover Page

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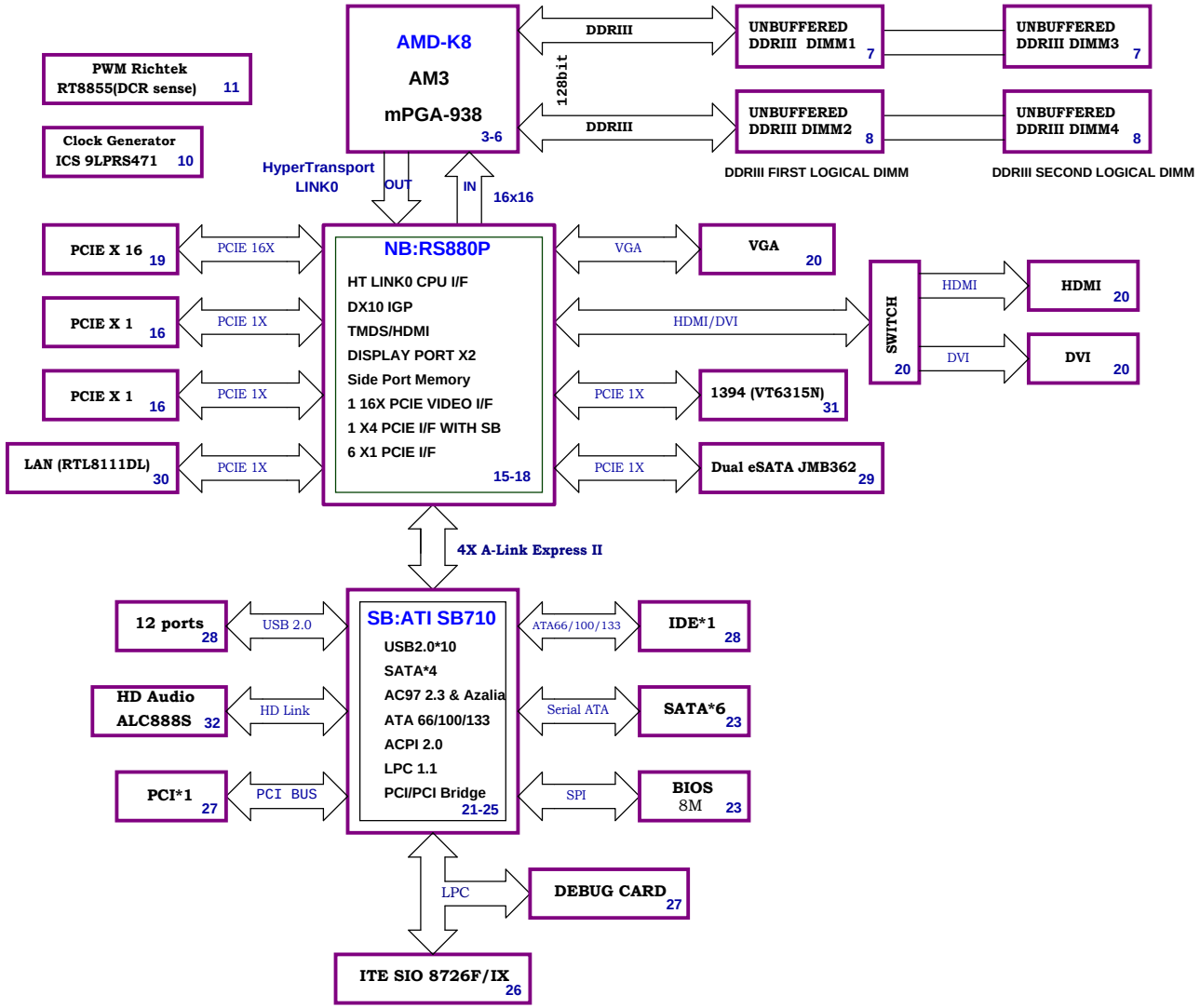

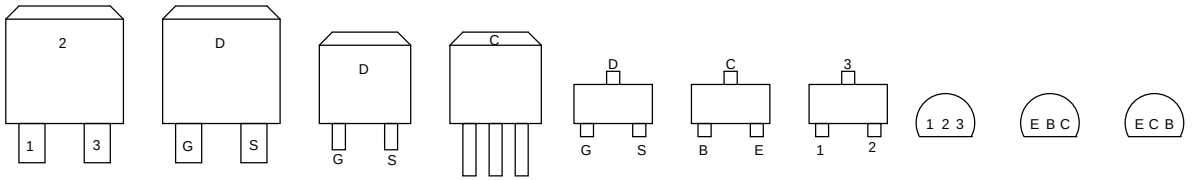

TO-263 B55QS03

TO-263 2SK3296

TO-252 20N03 TM3055TL-S 45N03 FDD6030L

TO-251 HI772(1.4W) (PNP)

SOT-23 2N7002 SI2303S SI2301S

SOT-23 2N3904 2N3906 MMBT2907A

SOT-23 BAT54C BAT54S

T0-92 LM431 78L05-D LM432

T0-92 2N2222A 2N2097A

T0-92 HSD882-D

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Title: Block Diagram		
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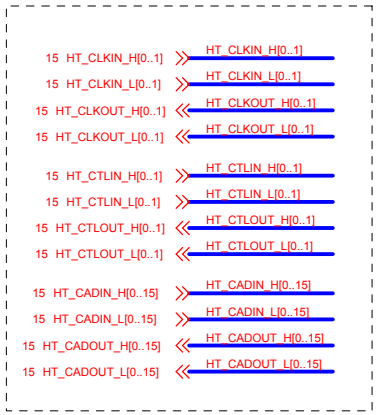
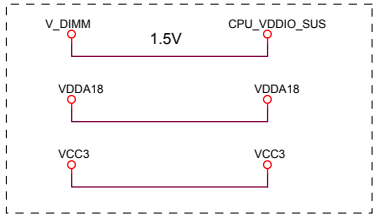
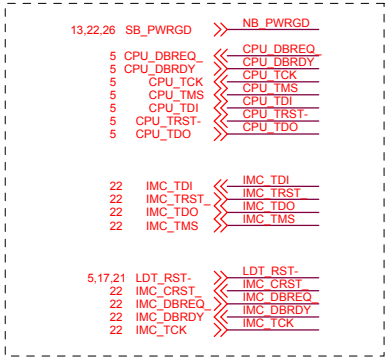
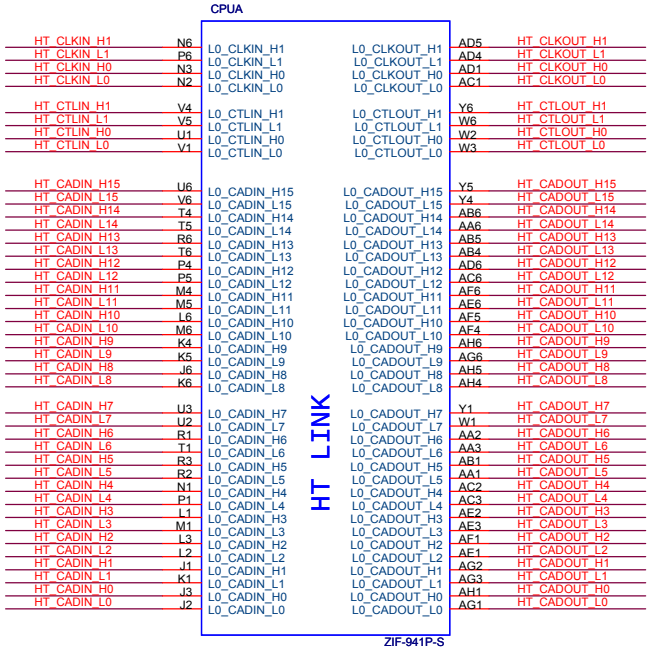
HyperTransport

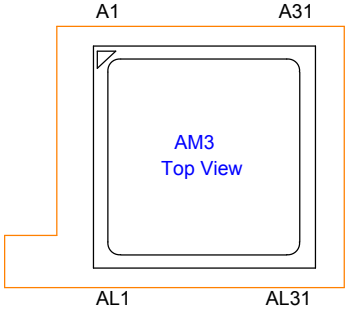


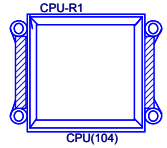






Please use 1mm pad size, place all ELT test pads on bottom side only.





Over Clocking

Elitegroup Computer Systems		
Title: CPU HT & DEBUG		
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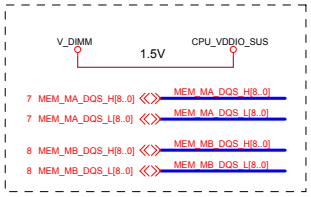
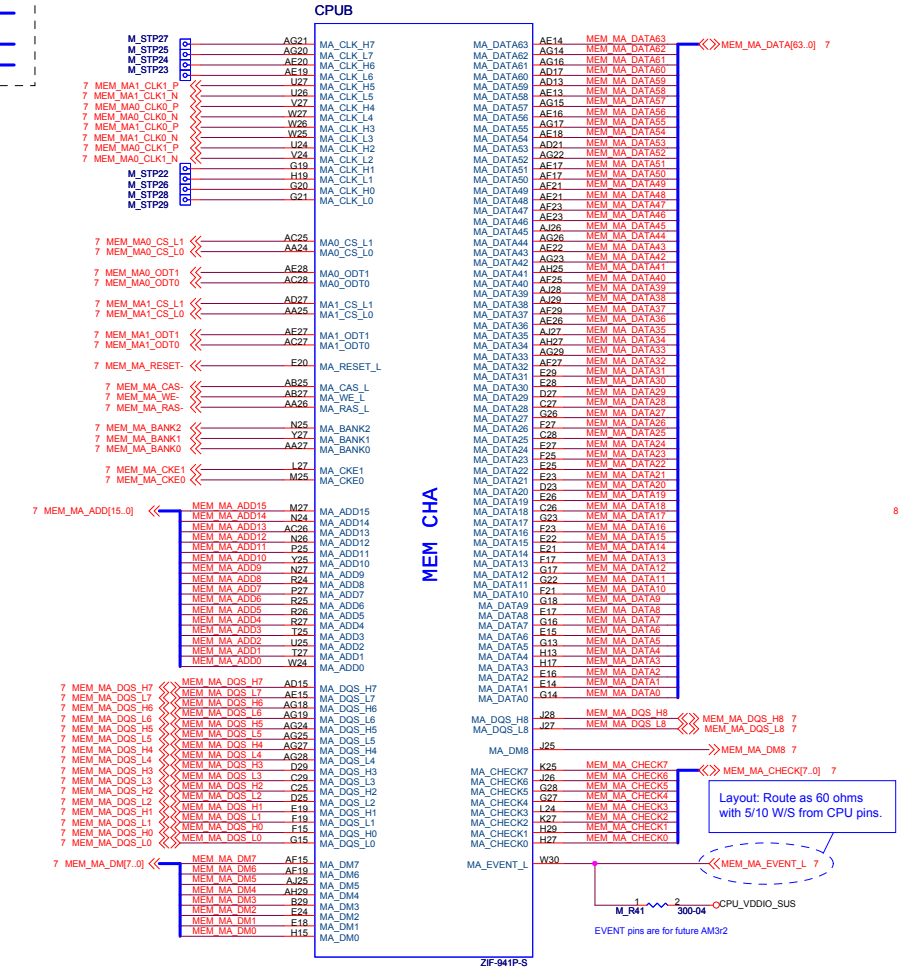
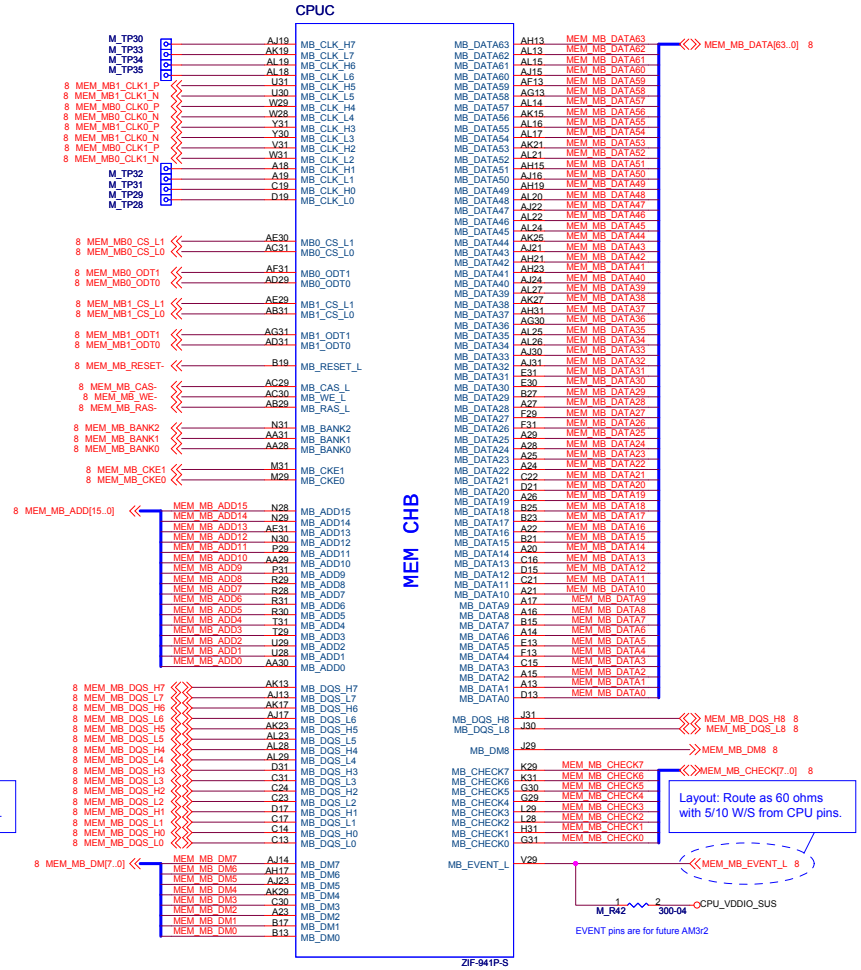
CPU Memory



DDR3 Memory Interface A

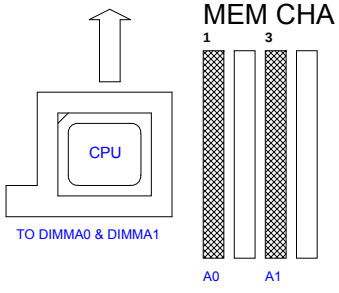


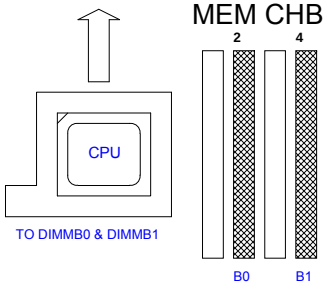
DDR3 Memory Interface B



MEMORY CLOCK TRANSLATION

DIMM	DDR2 Memory Signal	CPU Signal
DIMM A0	MEM_MA0_CLK1 MEM_MA0_CLK0	MA_CLK2 MA_CLK4
DIMM A1	MEM_MA1_CLK1 MEM_MA1_CLK0	MA_CLK5 MA_CLK3
DIMM B0	MEM_MB0_CLK1 MEM_MB0_CLK0	MB_CLK2 MB_CLK4
DIMM B1	MEM_MB1_CLK1 MEM_MB1_CLK0	MB_CLK5 MB_CLK3





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Title: AM3 CPU MEMORY

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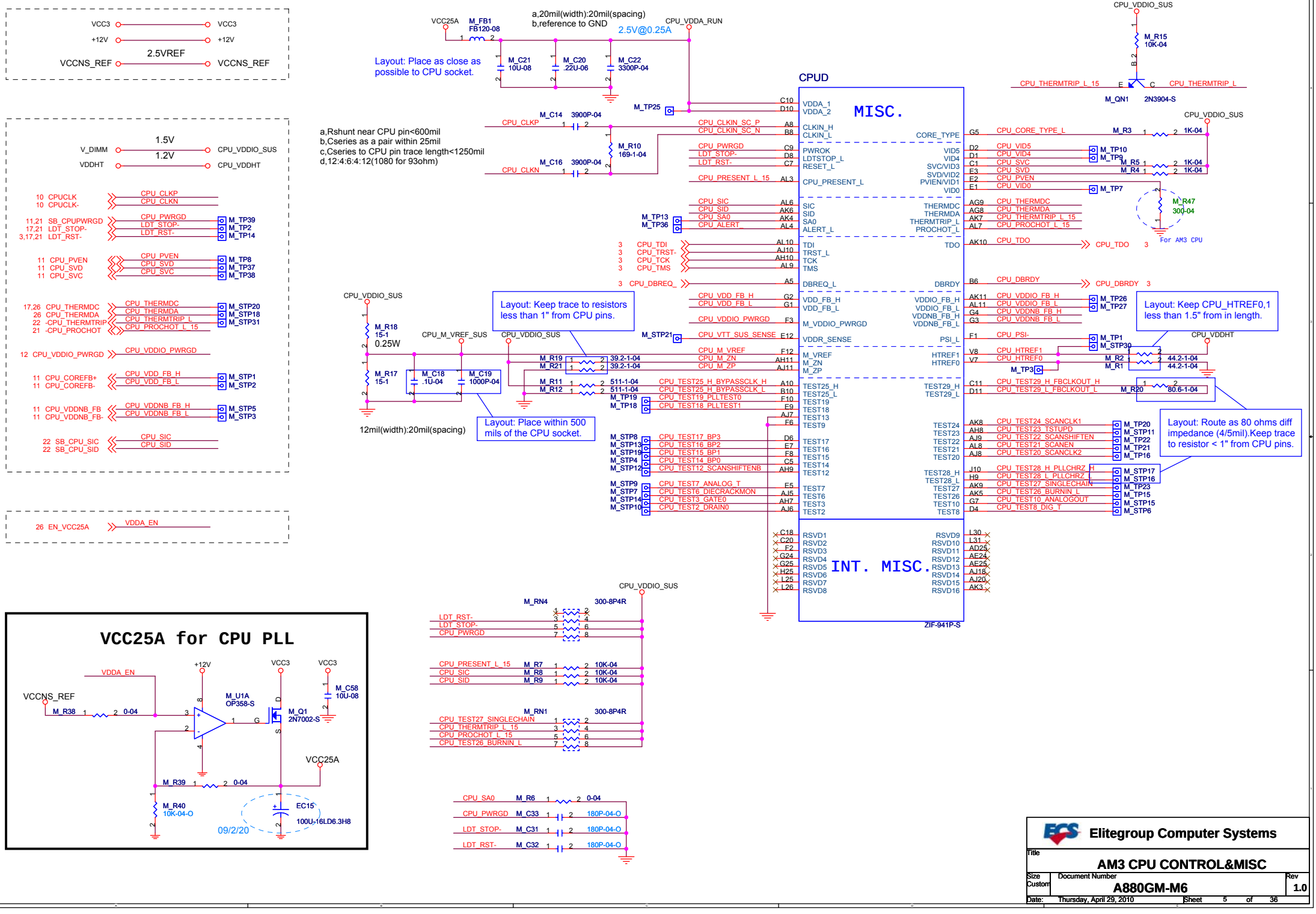
VCC3
+12V
2.5VREF
VCCNS_REF
1.5V
1.2V
V_DIMM
VDDHT
CPU_VDDIO_SUS
CPU_VDDHT
10 CPUCLK
10 CPUCLK-
CPU_CLKP
CPU_CLKN
11,21 SB_CPUPWRGD
17,21 LDT_STOP-
3,17,21 LDT_RST-
CPU_PWRGD
LDT_STOP-
LDT_RST-
M_TP39
M_TP2
M_TP14
11 CPU_PVEN
11 CPU_SVD
11 CPU_SVC
CPU_PVEN
CPU_SVD
CPU_SVC
M_TP8
M_TP37
M_TP38
17,26 CPU_THERMDC
26 CPU_THERMDA
22 -CPU_THERMTRIP
21 -CPU_PROCHOT
CPU_THERMDC
CPU_THERMDA
CPU_THERMTRIP_L
CPU_PROCHOT_L_15
M_STP20
M_STP18
M_STP31
12 CPU_VDDIO_PWRGD
CPU_VDDIO_PWRGD
11 CPU_COREFB+
11 CPU_COREFB-
CPU_VDD_FB_H
CPU_VDD_FB_L
M_STP1
M_STP2
11 CPU_VDDNB_FB
11 CPU_VDDNB_FB-
CPU_VDDNB_FB_H
CPU_VDDNB_FB_L
M_STP5
M_STP3
22 SB_CPU_SIC
22 SB_CPU_SID
CPU_SIC
CPU_SID
26 EN_VCC25A
VDDA_EN
VCC25A
M_FB1
FB120-08
a,20mil(width):20mil(spacing)
b,reference to GND
2.5V@0.25A
Layout: Place as close as possible to CPU socket.
M_C21
10U-08
M_C20
.22U-06
M_C22
3300P-04
M_TP25
a,Rshunt near CPU pin<600mil
b,Cseries as a pair within 25mil
c,Cseries to CPU pin trace length<1250mil
d,12:4:6:4:12(1080 for 93ohm)
M_C14
3900P-04
CPU_CLKP
M_R10
169-1-04
M_C16
3900P-04
CPU_CLKN
CPUD
MISC.
VDDA_1
VDDA_2
CLKIN_H
CLKIN_L
PWROK
LDTSTOP_L
RESET_L
CPU_PRESENT_L
CORE_TYPE
VID5
VID4
SVC/VID3
SVD/VID2
PVIEN/VID1
VID0
SIC
SID
SA0
ALERT_L
THERMDC
THERMDA
THERMTRIP_L
PROCHOT_L
TDI
TRST_L
TCK
TMS
TDO
DBREQ_L
DBRDY
VDD_FB_H
VDD_FB_L
M_VDDIO_PWRGD
VDDR_SENSE
VDDIO_FB_H
VDDIO_FB_L
VDDNB_FB_H
VDDNB_FB_L
PSI_L
M_VREF
M_ZN
M_ZP
HTREF1
HTREF0
TEST25_H
TEST25_L
TEST19
TEST18
TEST13
TEST9
TEST29_H
TEST29_L
TEST24
TEST23
TEST22
TEST21
TEST20
TEST17
TEST16
TEST15
TEST14
TEST12
TEST28_H
TEST28_L
TEST27
TEST26
TEST10
TEST8
TEST7
TEST6
TEST3
TEST2
INT. MISC.
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD15
RSVD16
ZIF-941P-S
CPU_CLKIN_SC_P
CPU_CLKIN_SC_N
CPU_PWRGD
LDT_STOP-
LDT_RST-
CPU_PRESENT_L_15
CPU_SIC
CPU_SID
CPU_SA0
CPU_ALERT_
3 CPU_TDI
3 CPU_TRST-
3 CPU_TCK
3 CPU_TMS
3 CPU_DBREQ_
CPU_VDD_FB_H
CPU_VDD_FB_L
CPU_VDDIO_PWRGD
CPU_VTT_SUS_SENSE
CPU_M_VREF
CPU_M_ZN
CPU_M_ZP
CPU_TEST25_H_BYPASSCLK_H
CPU_TEST25_H_BYPASSCLK_L
CPU_TEST19_PLLTEST0
CPU_TEST18_PLLTEST1
CPU_TEST17_BP3
CPU_TEST16_BP2
CPU_TEST15_BP1
CPU_TEST14_BP0
CPU_TEST12_SCANSHIFTENB
CPU_TEST7_ANALOG_T
CPU_TEST6_DIECRACKMON
CPU_TEST3_GATE0
CPU_TEST2_DRAIN0
M_TP13
M_TP36
M_STP21
M_STP8
M_STP13
M_STP19
M_STP4
M_STP12
M_STP9
M_STP7
M_STP14
M_STP10
CPU_VDDIO_SUS
M_R18
15-1
0.25W
M_R17
15-1
M_C18
.1U-04
M_C19
1000P-04
12mil(width):20mil(spacing)
CPU_M_VREF_SUS
M_R19
M_R21
39.2-1-04
M_R11
M_R12
511-1-04
M_TP19
M_TP18
Layout: Keep trace to resistors less than 1" from CPU pins.
Layout: Place within 500 mils of the CPU socket.
CPU_VDDIO_SUS
M_R15
10K-04
CPU_THERMTRIP_L_15
M_QN1
2N3904-S
CPU_THERMTRIP_L
CPU_VDDIO_SUS
G5 CPU_CORE_TYPE_L
M_R3
1K-04
D2 CPU_VID5
D1 CPU_VID4
C1 CPU_SVC
E3 CPU_SVD
E2 CPU_PVEN
E1 CPU_VID0
M_TP10
M_TP9
M_R5
M_R4
1K-04
M_TP7
AG9 CPU_THERMDC
AG8 CPU_THERMDA
AK7 CPU_THERMTRIP_L_15
AL7 CPU_PROCHOT_L_15
M_R47
300-04
For AM3 CPU
AK10 CPU_TDO
CPU_TDO 3
B6 CPU_DBRDY
CPU_DBRDY 3
AK11 CPU_VDDIO_FB_H
AL11 CPU_VDDIO_FB_L
G4 CPU_VDDNB_FB_H
G3 CPU_VDDNB_FB_L
M_TP26
M_TP27
Layout: Keep CPU_HTREF0,1 less than 1.5" from in length.
F1 CPU_PSI-
M_TP1
M_STP30
CPU_VDDHT
V8 CPU_HTREF1
V7 CPU_HTREF0
M_TP3
M_R2
M_R1
44.2-1-04
C11 CPU_TEST29_H_FBCLKOUT_H
D11 CPU_TEST29_L_FBCLKOUT_L
M_R20
80.6-1-04
Layout: Route as 80 ohms diff impedance (4/5mil).Keep trace to resistor < 1" from CPU pins.
AK8 CPU_TEST24_SCANCLK1
AH8 CPU_TEST23_TSTUPD
AJ9 CPU_TEST22_SCANSHIFTEN
AL8 CPU_TEST21_SCANEN
AJ8 CPU_TEST20_SCANCLK2
M_TP20
M_STP11
M_TP22
M_TP21
M_TP16
J10 CPU_TEST28_H_PLLCHRZ_H
H9 CPU_TEST28_L_PLLCHRZ_L
AK9 CPU_TEST27_SINGLECHAIN
AK5 CPU_TEST26_BURNIN_L
G7 CPU_TEST10_ANALOGOUT
D4 CPU_TEST8_DIG_T
M_STP17
M_STP16
M_TP23
M_TP15
M_STP15
M_STP6
CPU_VDDIO_SUS
M_RN4
300-8P4R
LDT_RST-
LDT_STOP-
CPU_PWRGD
CPU_PRESENT_L_15
CPU_SIC
CPU_SID
M_R7
M_R8
M_R9
10K-04
M_RN1
300-8P4R
CPU_TEST27_SINGLECHAIN
CPU_THERMTRIP_L_15
CPU_PROCHOT_L_15
CPU_TEST26_BURNIN_L
CPU_SA0
CPU_PWRGD
LDT_STOP-
LDT_RST-
M_R6
M_C33
M_C31
M_C32
0-04
180P-04-O
VCC25A for CPU PLL
VDDA_EN
VCCNS_REF
M_R38
0-04
+12V
VCC3
M_U1A
OP358-S
M_Q1
2N7002-S
M_C58
10U-08
VCC25A
M_R39
0-04
M_R40
10K-04-O
EC15
100U-16LD6.3H8
09/2/20
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Title
AM3 CPU CONTROL&MISC
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Custom
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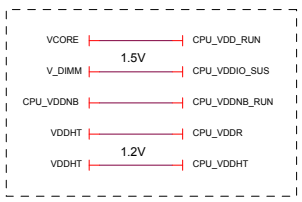
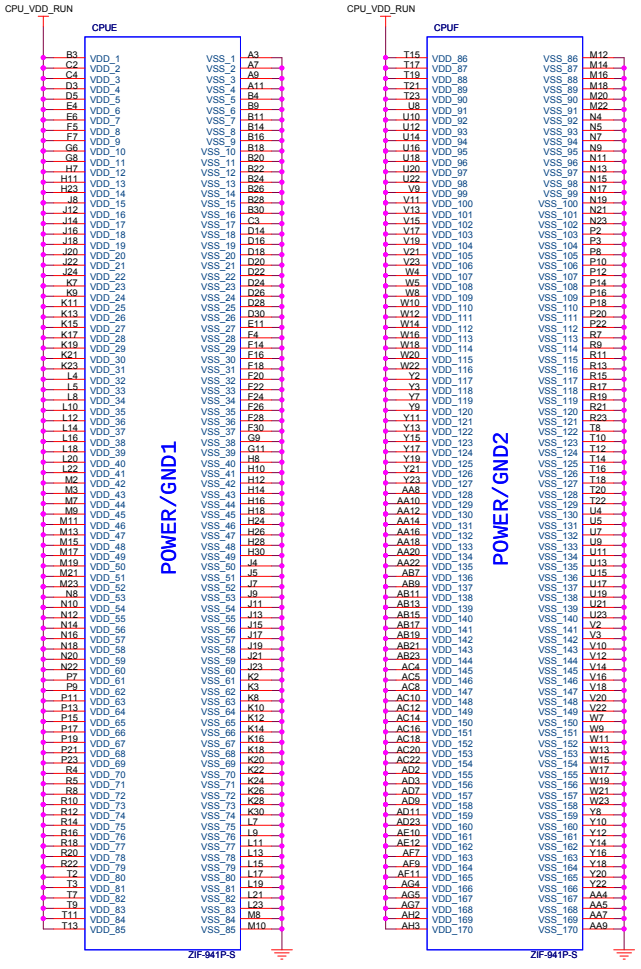
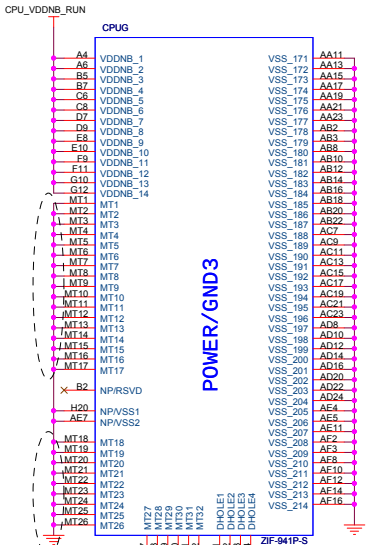
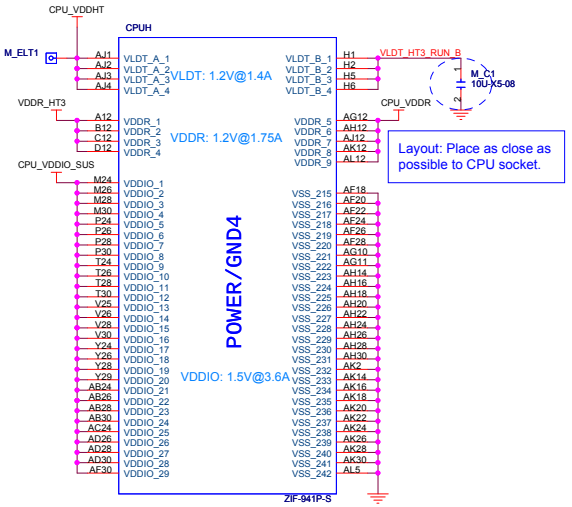
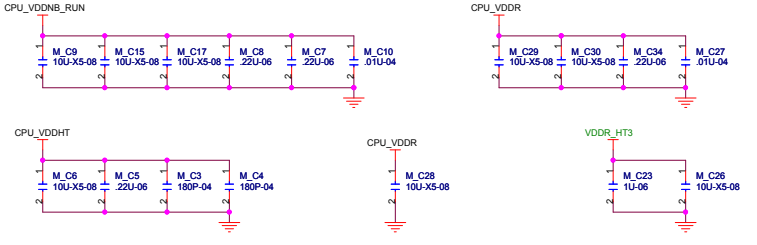
Processor Power and Ground



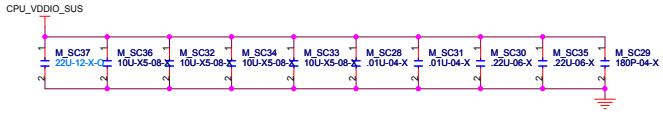


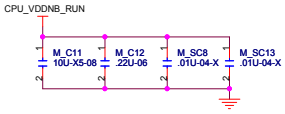


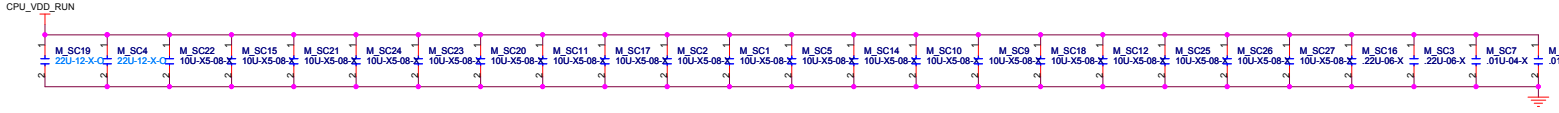


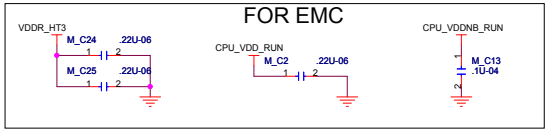


Bottom Side Decoupling









Elitegroup Computer Systems

Title: AM3 CPU PWR&GND

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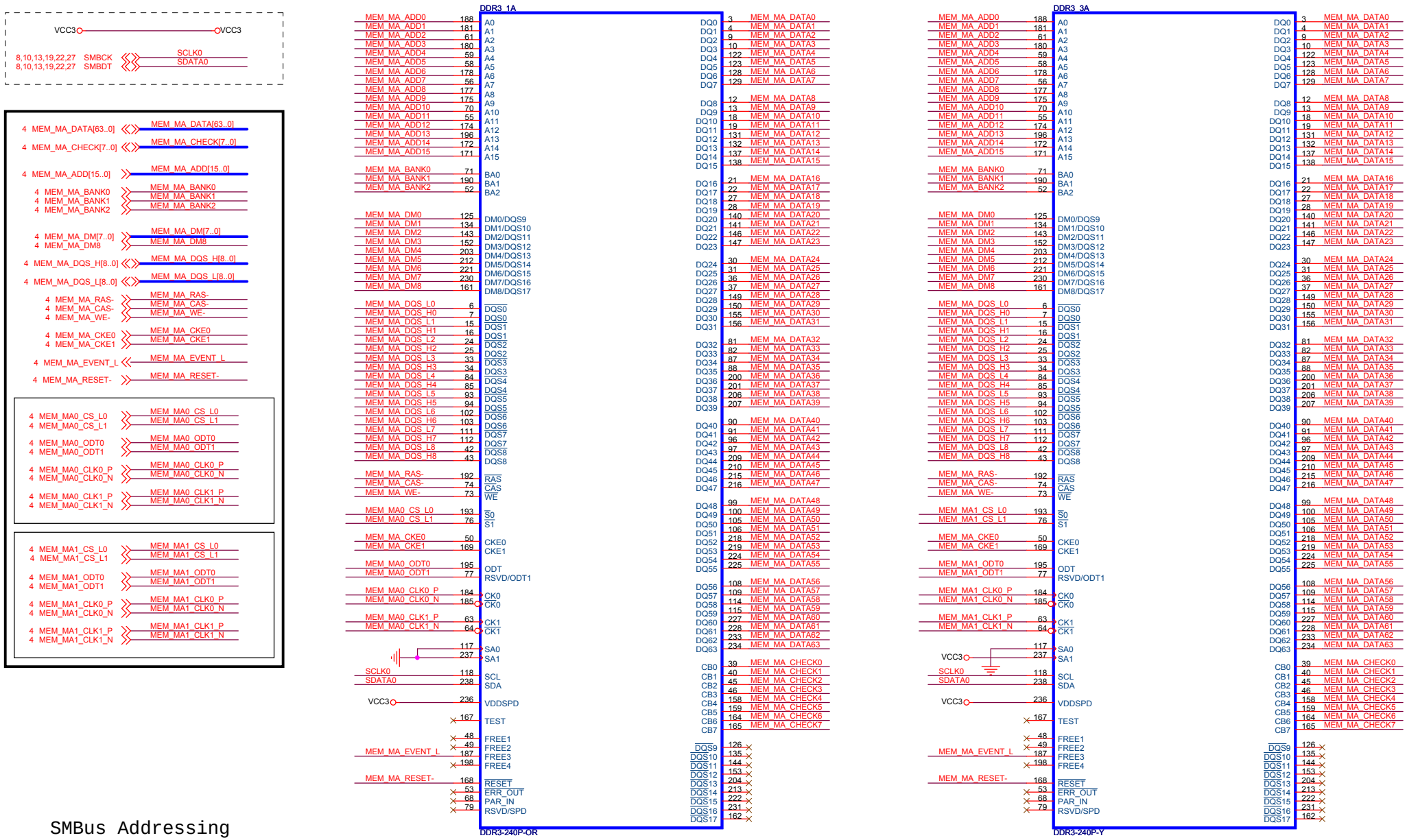

SMBus Addressing

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2
DIMMA1	A4
DIMMB1	A6

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Title: DDR3 DIMM A CH

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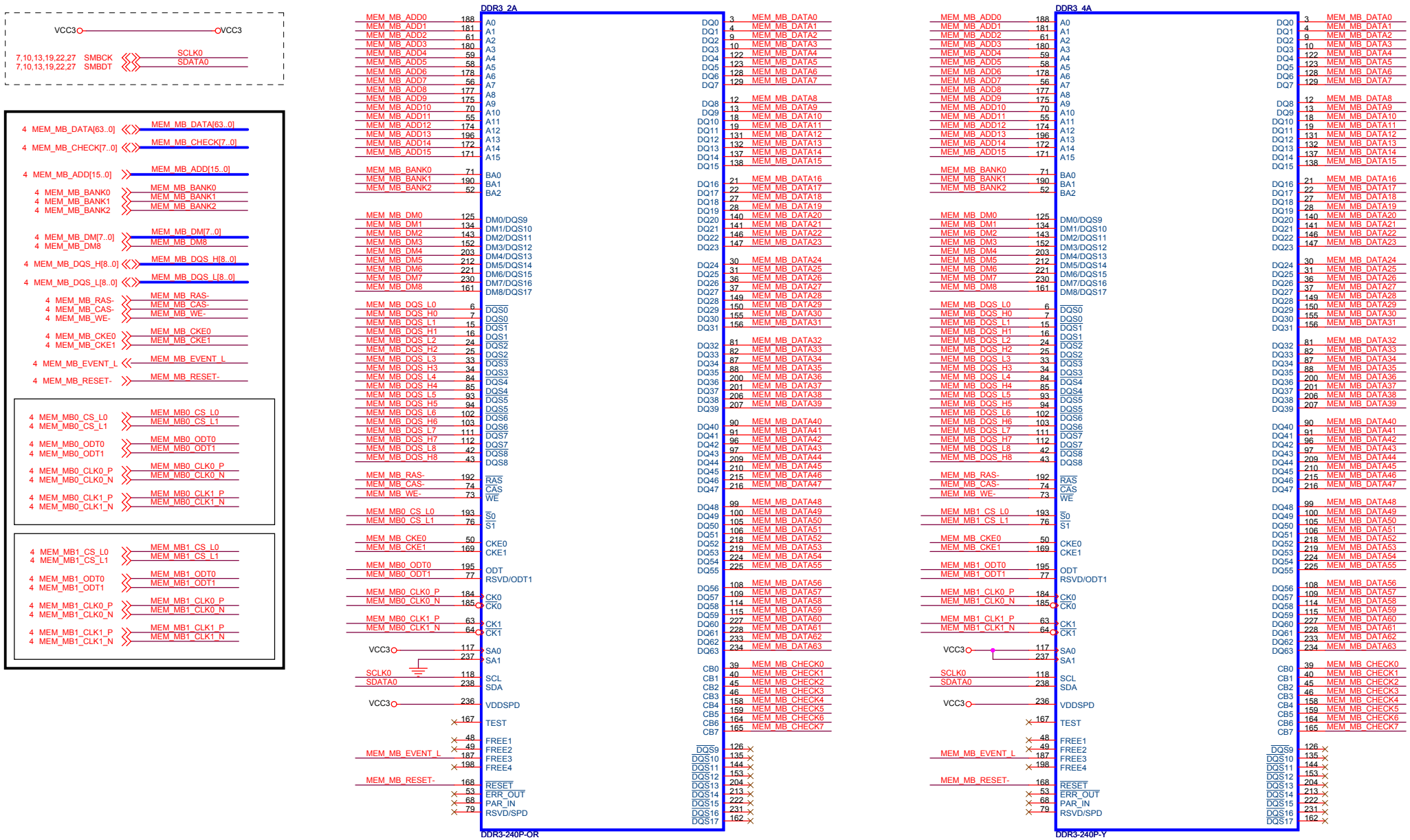

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Title: DDR3 DIMM B CH

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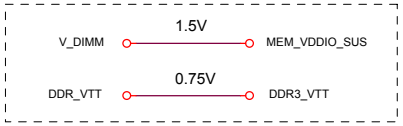
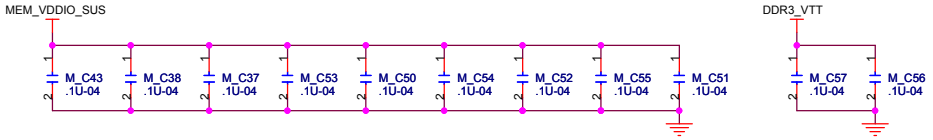
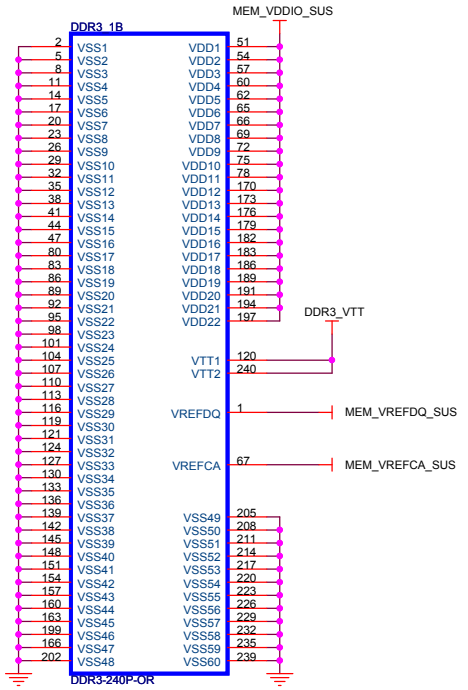
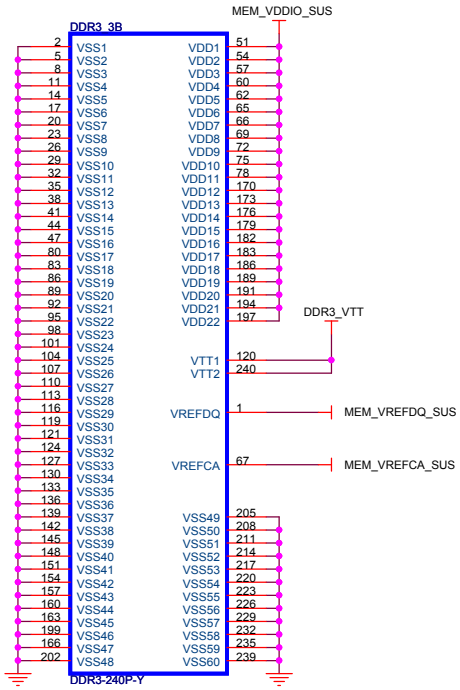
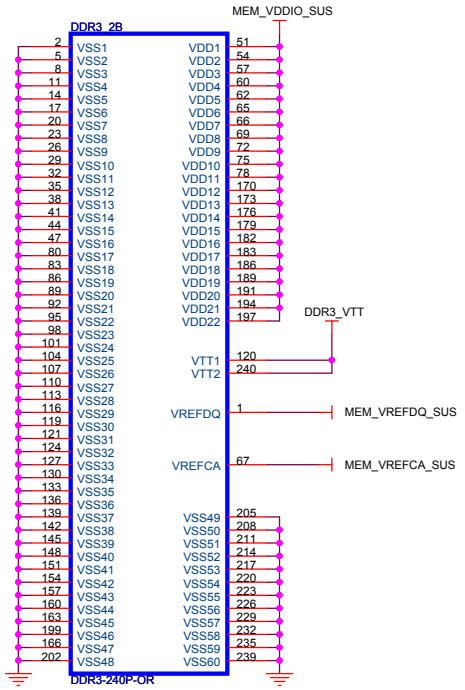


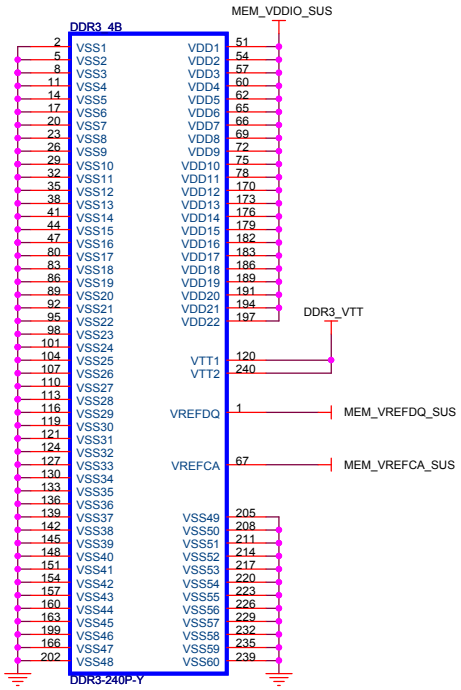
DE-COUPLING CAP FOR DIMMs



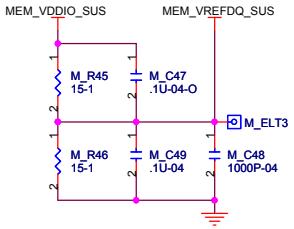






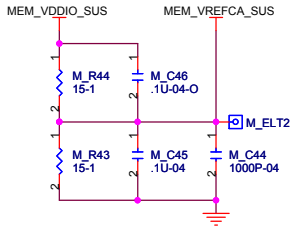


MEM_VREFDQ_SUS



Layout: Place within 500 mils of the DIMMB1 socket. 12mil(width):20mil(spacing)

MEM_VREFCA_SUS



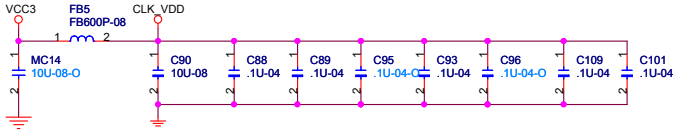
Layout: Place within 500 mils of the DIMMB1 socket. 12mil(width):20mil(spacing)

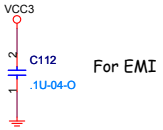
Elitegroup Computer Systems

Title: DDR3 DIMM PWR

Size: Custom | Document Number: A880GM-M6 | Rev: 1.0

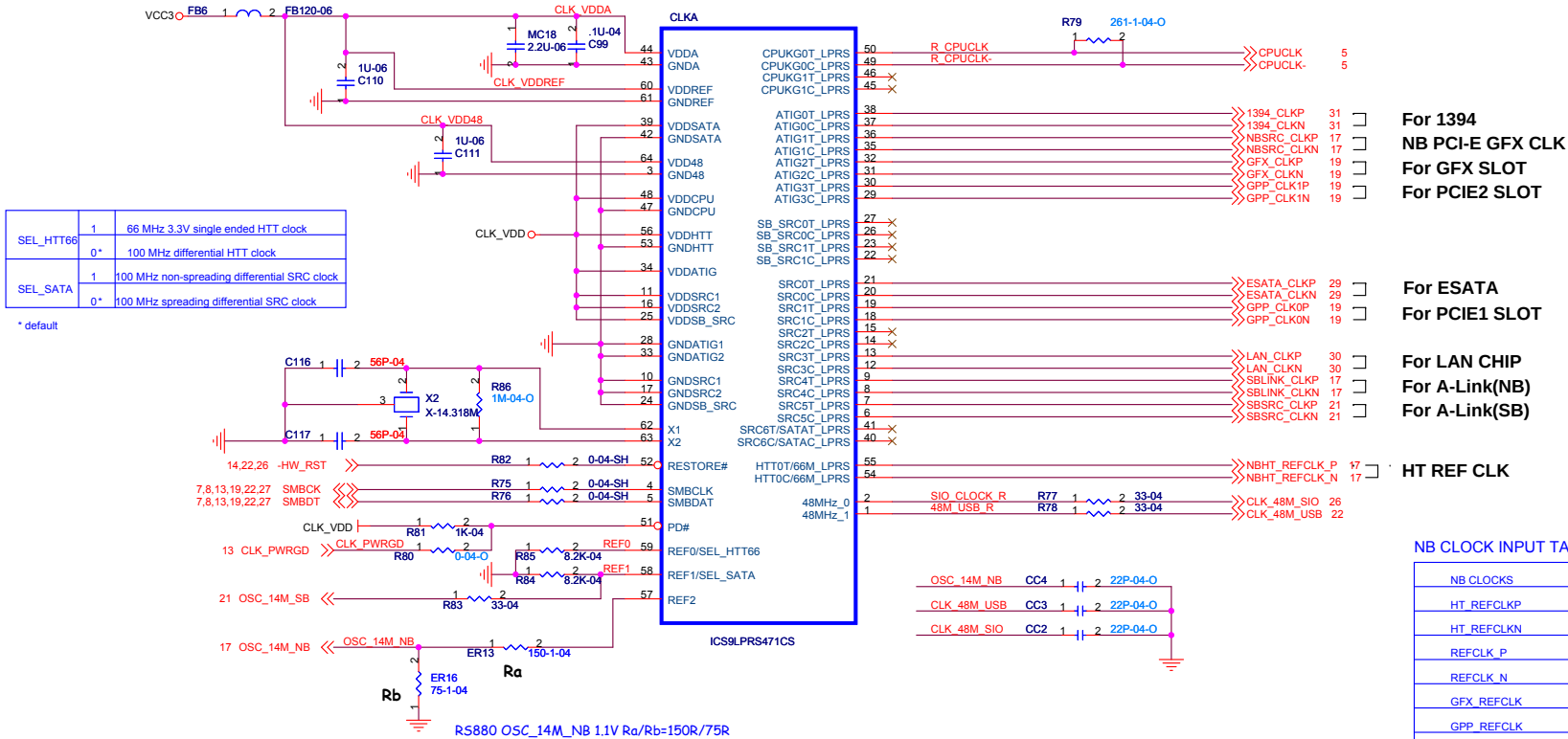
Date: Thursday, April 29, 2010 | Sheet 9 of 36





1- PLACE ALL SERIAL TERMINATION
RESISTORS CLOSE TO CLOCK GEN

2- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock

* default

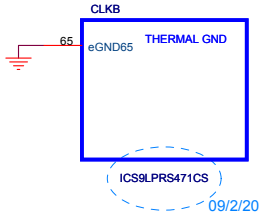
RS880 OSC_14M_NB 1.1V Ra/Rb=150R/75R

For 1394
NB PCI-E GFX CLK
For GFX SLOT
For PCIE2 SLOT

For ESATA
For PCIE1 SLOT

For LAN CHIP
For A-Link(NB)
For A-Link(SB)

HT REF CLK



NB CLOCK INPUT TABLE

NB CLOCKS	RS880
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	VREF
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

* RS880 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
Clock chip has internal serial terminations for differencial pairs

Elitegroup Computer Systems

Title: Clock Generator

Size: Custom | Document Number: A880GM-M6 | Rev: 1.0

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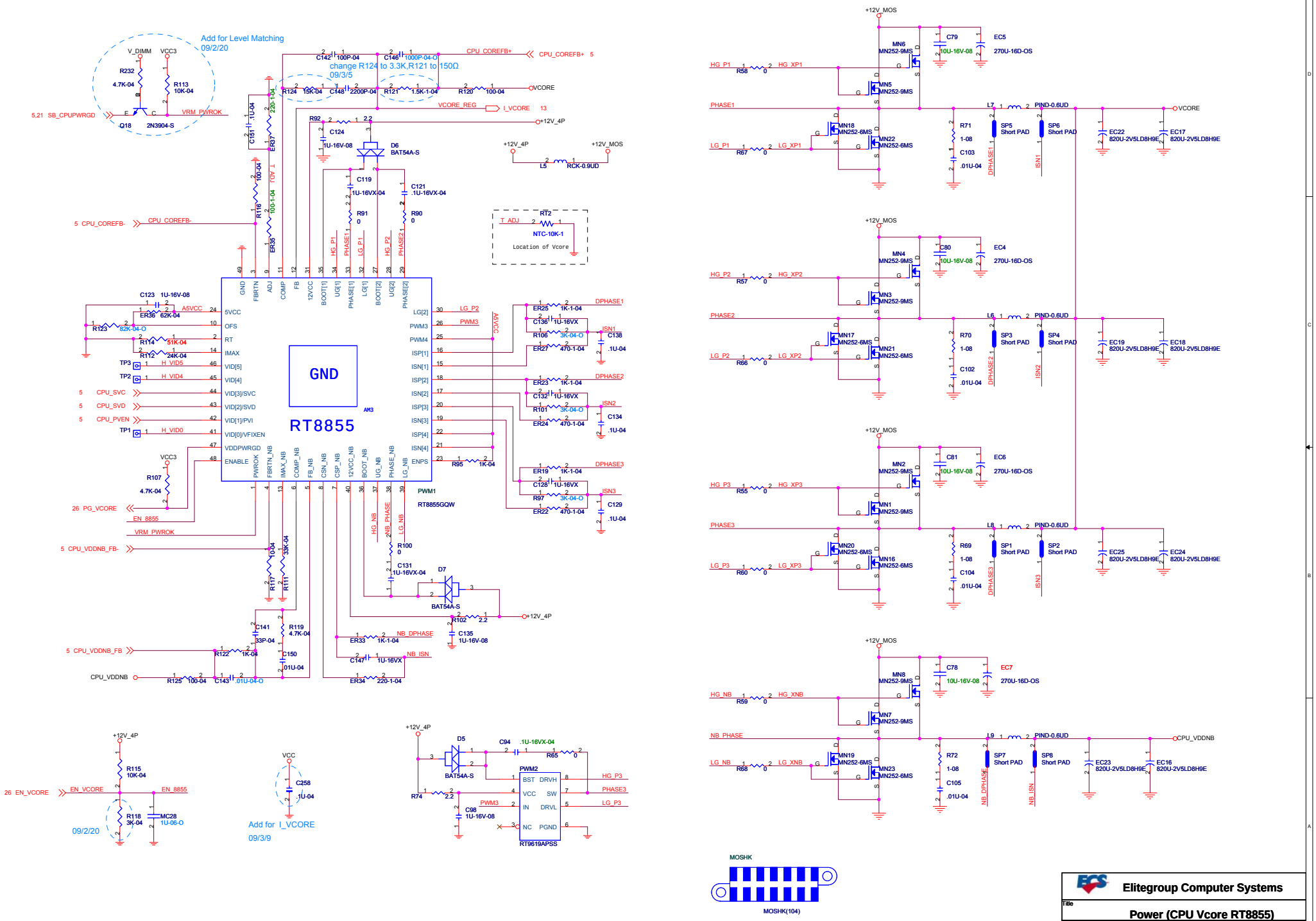
Add for Level Matching
09/2/20
change R124 to 3.3K,R121 to 150Ω
09/3/5
RT8855
RT8855GQW
PWM1
GND
AM3
Add for I_VCORE
09/3/9
09/2/20
MOSHK
MOSHK(104)
Elitegroup Computer Systems
Power (CPU Vcore RT8855)
A880GM-M6
1.0
Thursday, April 29, 2010
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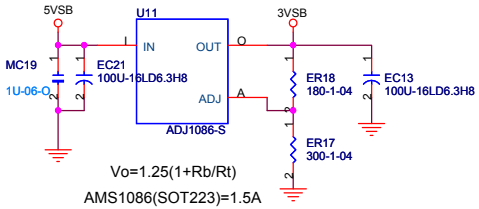
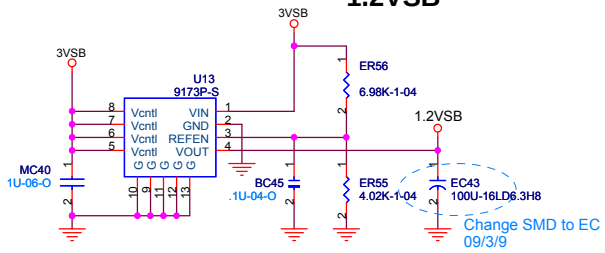
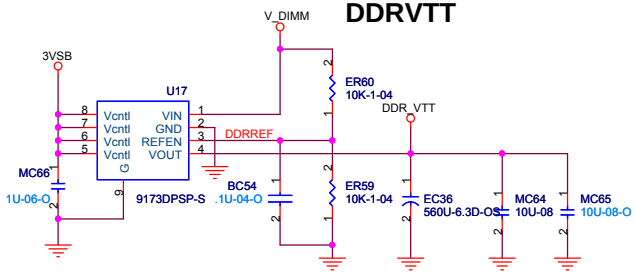
3VSB



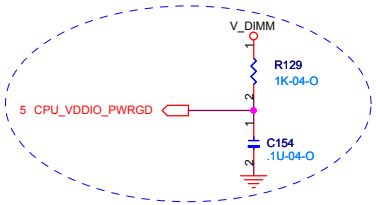
1.2VSB



DDRVTT



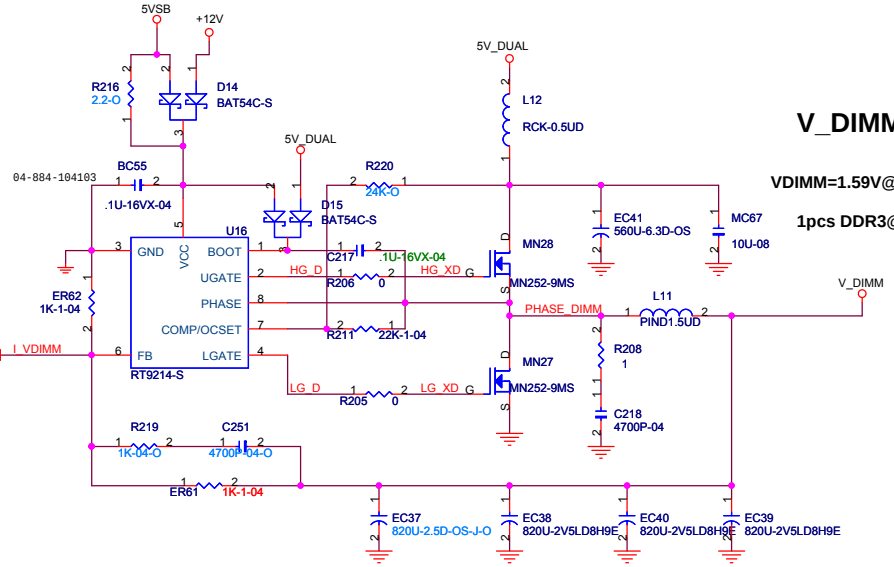
Place close to CPU



V_DIMM

VDIMM=1.59V@21A

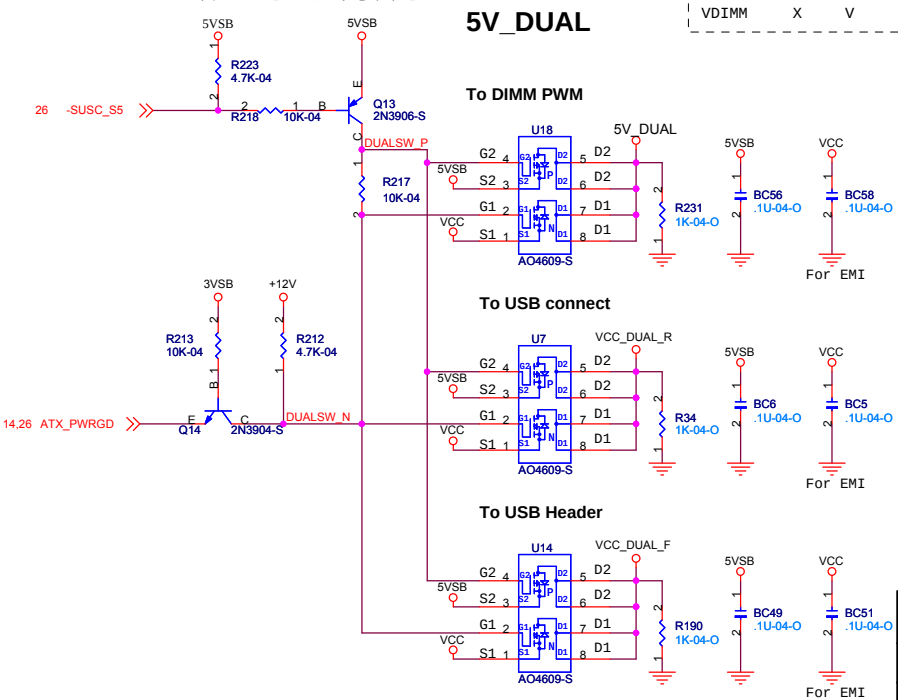
1pcs DDR3@3A



	S5	enter S0	S0	enter S3	exit S3	enter S5	S5
-SUSC_S5	0	0	1	1	1	0	0
ATX_PWRGD	0	1	1	0	1	1	0
DUALSW_P	5VSB	5VSB	12V	0	12V	5VSB	5VSB
DUALSW_N	0	12V	12V	0	12V	12V	0
5V_DUAL	X	VCC5	VCC5	5VSB	VCC5	VCC5	0
VDIMM	X	V	V	V	V	V	X

5V_DUAL

A版5VSB與Q13之間接有4.7K電阻，
導致DUAL電壓S4,S5狀態下帶電。



Elitegroup Computer Systems

Title: Power A(DC to DC)

Size: Custom | Document Number: A880GM-M6 | Rev: 1.0

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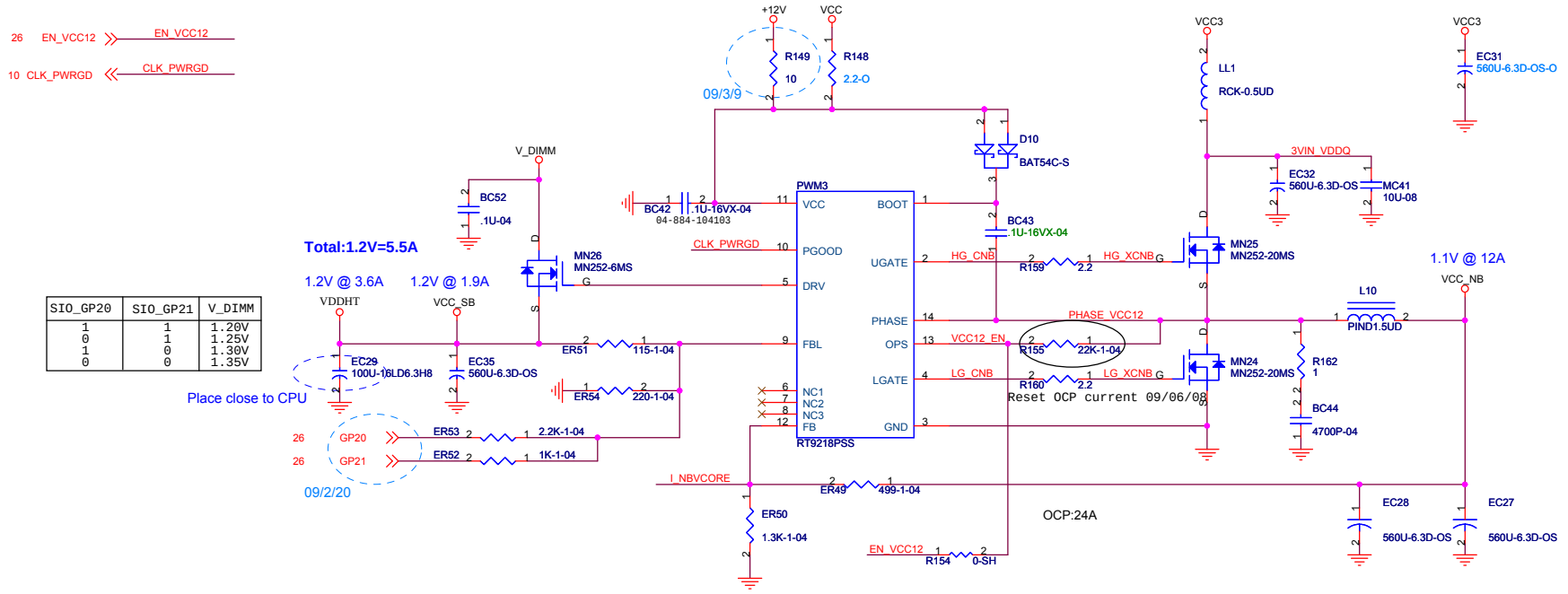
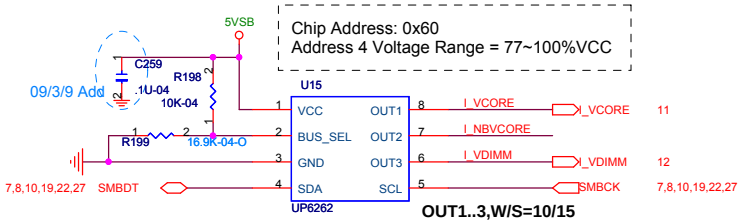
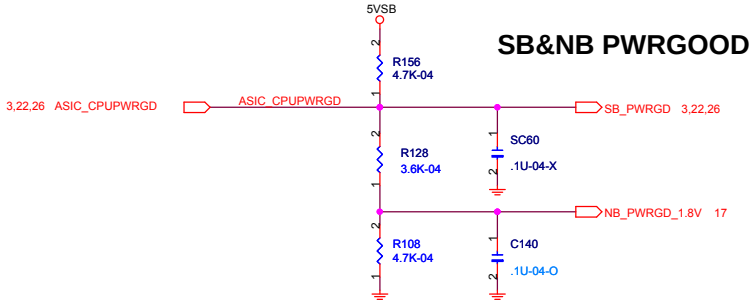
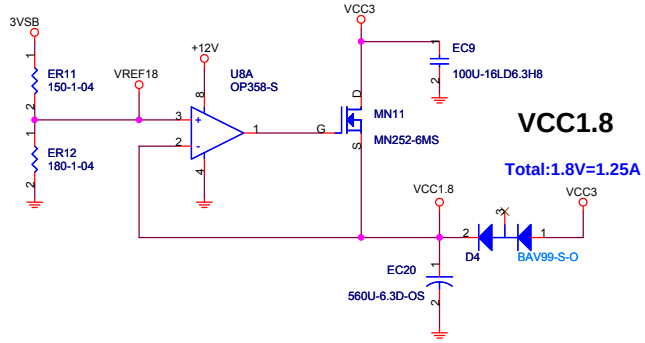


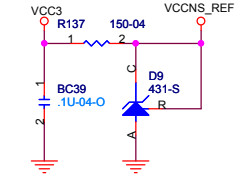
uP6262的電流輸出與ΔVout的關系如下:
選取從uP6262輸出的方向爲正,
則VCORE,VCC_NB及VDIMM的ΔVout爲:
ΔVout = -Ic * RFB;







VCC1.8



Elitegroup Computer Systems	
Title	Power B(DC to DC),PWR Sequence&good
Size: Custom	Document Number: A880GM-M6
Rev	1.0
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FRONT PANEL

External Connection

23 SATA_LED1- → SATA_LED1-
28 IDE_LED1- → IDE_LED1-
10,22,26 -HW_RST → -HW_RST
26 -PWRBTN → -PWRBTN
22 SPKR_SB → SPKR_SB
26 G_LED1 → G_LED1
26 G_LED2 → G_LED2
29 ESATA_LED- → -HDD_LED

PWR_BTN: 1 2 3 4 -PWRBTN — TACT-4P-R
RST_BTN: 1 2 3 4 -HW_RST — TACT-4P-Y

D17: SATA_LED1- 1, IDE_LED1- 2, 3 → BAT54A-S
VCC → R207 180-04 → +HDD_LED
-HDD_LED → F_PANEL 1
-HW_RST → F_PANEL 7
C207 1U-06-O
5VSB → RN18 330-8P4R
F_PANEL 2 → G_LED1X
F_PANEL 4 → G_LED2X
F_PANEL 6 → -PWRBTN
R225 100-04
C219 1U-06-O
H5X2-P10E-B

F_PANEL: +MSGLED PWR; 2 4 6 8; 1 3 5 7 9; +HDDLED RST

5VSB → R194 330-04 → STBY LED_Red_S
VCC → R200 330-04 → PWR LED_Green_S

5VSB → R215 4.7K-04 → G_LED1 → R214 1K → Q15 2N3904-S → G_LED1X
VCC → R210 4.7K-04 → G_LED2 → R209 1K → Q12 2N3904-S → G_LED2X

BUZZER SPK Colay

VCC → R168 4.7K-04
26 WT_BEEP → C197 .1U-04
22 SPKR_SB → R163 1K-04
Q11 2N3904-S
R167 100-04
VCC → BZ
C196 .1U-04-O
BUZZER-D

POWER CONNECTOR

External Connection

VCC3 → VCC3
-12V → -12V
5VSB → 5VSB
VCC → VCC
+12V → +12V
26,12,26 -ATX_PSON → -ATX_PSON
ATX_PWRGD → ATX_PWRGD

5VSB → R221 4.7K-04 → -ATX_PSON
-12V VCC VCC3 → ATX_POWER
VCC3 VCC +12V 5VSB VCC → ATX_POWER
ATX_POWER: 13 3.3V, 14 -12V, 15 GND, 16 PS_ON, 17 GND, 18 GND, 19 GND, 20 -5V, 21 +5V, 22 +5V, 23 +5V, 24 GND; 1 3.3V, 2 3.3V, 3 GND, 4 +5V, 5 GND, 6 +5V, 7 GND, 8 PWROK, 9 AUX5V, 10 +12V, 11 +12V, 12 3.3V
ATX-PW-24P2R
R222 8.2K-04 → ATX_PWRGD
C250 .1U-04-O

Change to 8pin power connector 09/2/20
+12V_4P → BC19 .1U-04
ATX12V
ATX-PW-8P2R

VCC3 → C252 .1U-04-O
+12V → C199 .1U-04-O
5VSB → C249 .1U-04-O
For EMI.
VCC → C260 .1U-04-O Placed near the L5
5VSB → C220 .1U-04-O
VCC → C248 .1U-04-O
VCC → C246 .1U-04 FOR EMI.

FAN

External Connection

+12V → +12V
VCC → VCC
26 CFAN_PWM1 → CFAN_PWM1
26 CFAN_TAC1 → CFAN_TAC1
26 SFAN_PWM2 → SFAN_PWM2
26 SFAN_TAC2 → SFAN_TAC2
26 PFAN_PWM3 → PFAN_PWM3
26 PFAN_TAC3 → PFAN_TAC3

4 3 2 1 Top View

+12V → R164 4.7K-04 → D11 1N4148-S
VCC → R136 4.7K-04
CFAN_PWM1 → R169 100-04
CFAN_TAC1 → R165 27K-04 → R166 10K-04
CPU_FAN: GPO, SENSE, +12V, GND — H4X1-P-W
EC33 100U-16LD6.3H8
C198 1U-06

VCC → R143 1K-04 09/2/20 → R142 15K-04
SFAN_PWM2
+12V → M_U1B OP358-S
R141 1K-04 → Q16 772-D (TO-251 1.4W) → R229 0-08-O
BOM:03-071-677285
R140 470-04
MC38 10U-08
R139 33K-04
R138 22K-04
+12V → R227 4.7K-04 → D18 1N4148-S
SYS_FAN: SENSE, +12V, GND — H3X1-P-W
SFAN_TAC2 → R230 27K-04 → R228 10K-04
EC42 100U-16LD6.3H8 Change 10U to 100U 09/2/20
C253 .1U-04

VCC → R46 1K-04 09/2/20 → R50 15K-04
PFAN_PWM3
+12V → U8B OP358-S
R40 1K-04 → Q8 772-D (TO-251 1.4W) → R42 0-08-O
BOM:03-071-677285
R41 470-04
MC13 10U-08
R43 33K-04
R44 22K-04
+12V → R38 4.7K-04 → D3 1N4148-S
PWR_FAN: SENSE, +12V, GND — H3X1-P-W
PFAN_TAC3 → R37 27K-04 → R36 10K-04
EC8 100U-16LD6.3H8
C83 .1U-04

H1 TH8 AUGND AUGND
H2 TH8
H3 TH8
H4 TH8
H5 TH8
H6 TH8
H7 TH8
H8 TH8

Elitegroup Computer Systems

Title: Front Panel, FAN

Size	Document Number	Rev
Custom	A880GM-M6	1.0

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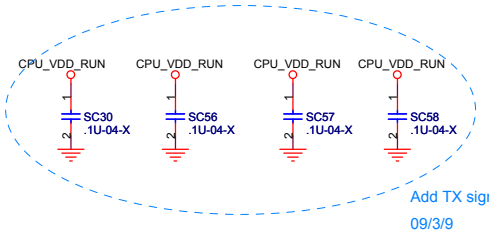
HT LINK

3 HT_CLKIN_H[0..1] — HT_CLKIN_P[0..1]
3 HT_CLKIN_L[0..1] — HT_CLKIN_N[0..1]
3 HT_CLKOUT_H[0..1] — HT_CLKOUT_P[0..1]
3 HT_CLKOUT_L[0..1] — HT_CLKOUT_N[0..1]
3 HT_CTLIN_H[0..1] — HT_CTLIN_P[0..1]
3 HT_CTLIN_L[0..1] — HT_CTLIN_N[0..1]
3 HT_CTLOUT_H[0..1] — HT_CTLOUT_P[0..1]
3 HT_CTLOUT_L[0..1] — HT_CTLOUT_N[0..1]
3 HT_CADIN_H[0..15] — HT_CADIN_P[0..15]
3 HT_CADIN_L[0..15] — HT_CADIN_N[0..15]
3 HT_CADOUT_H[0..15] — HT_CADOUT_P[0..15]
3 HT_CADOUT_L[0..15] — HT_CADOUT_N[0..15]



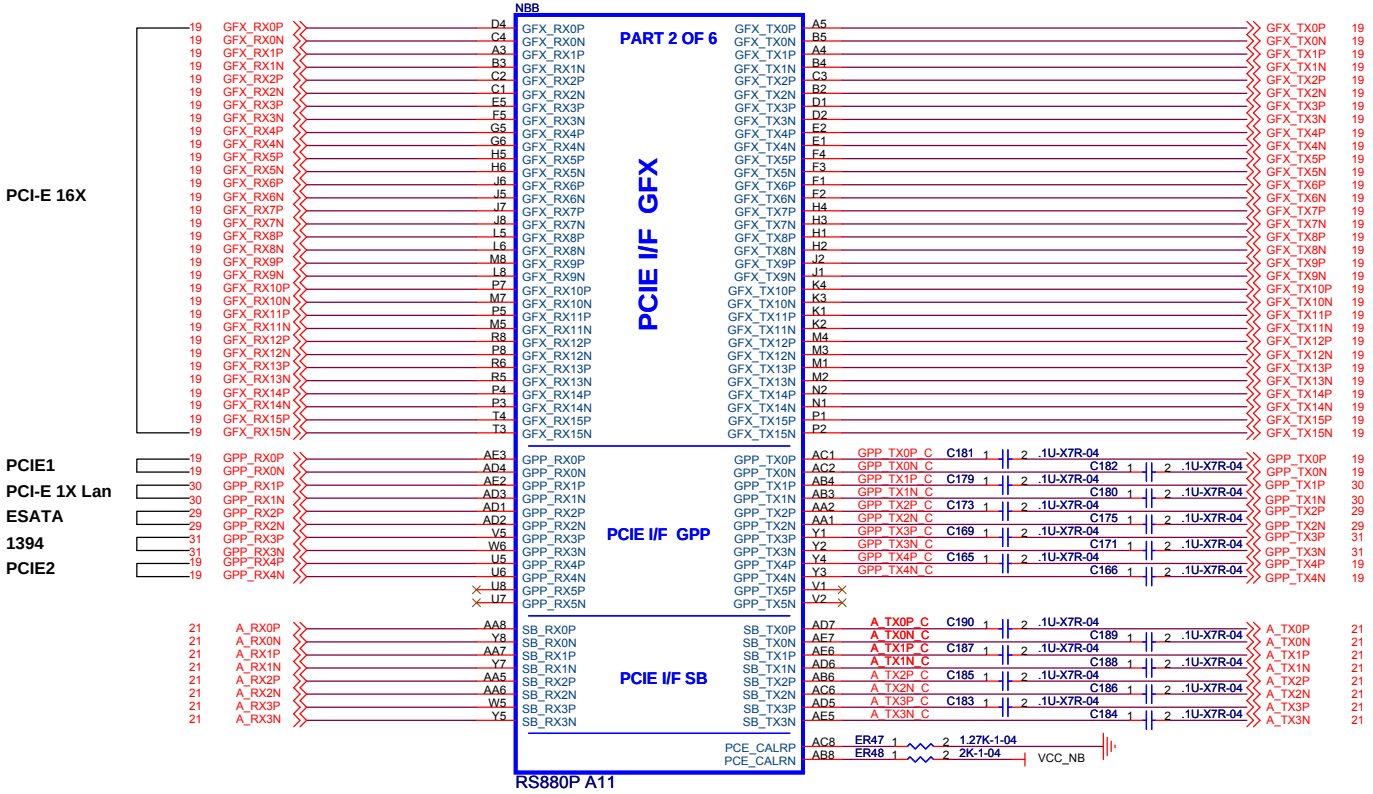
Add TX signals return path CAP
09/3/9

Elitegroup Computer system

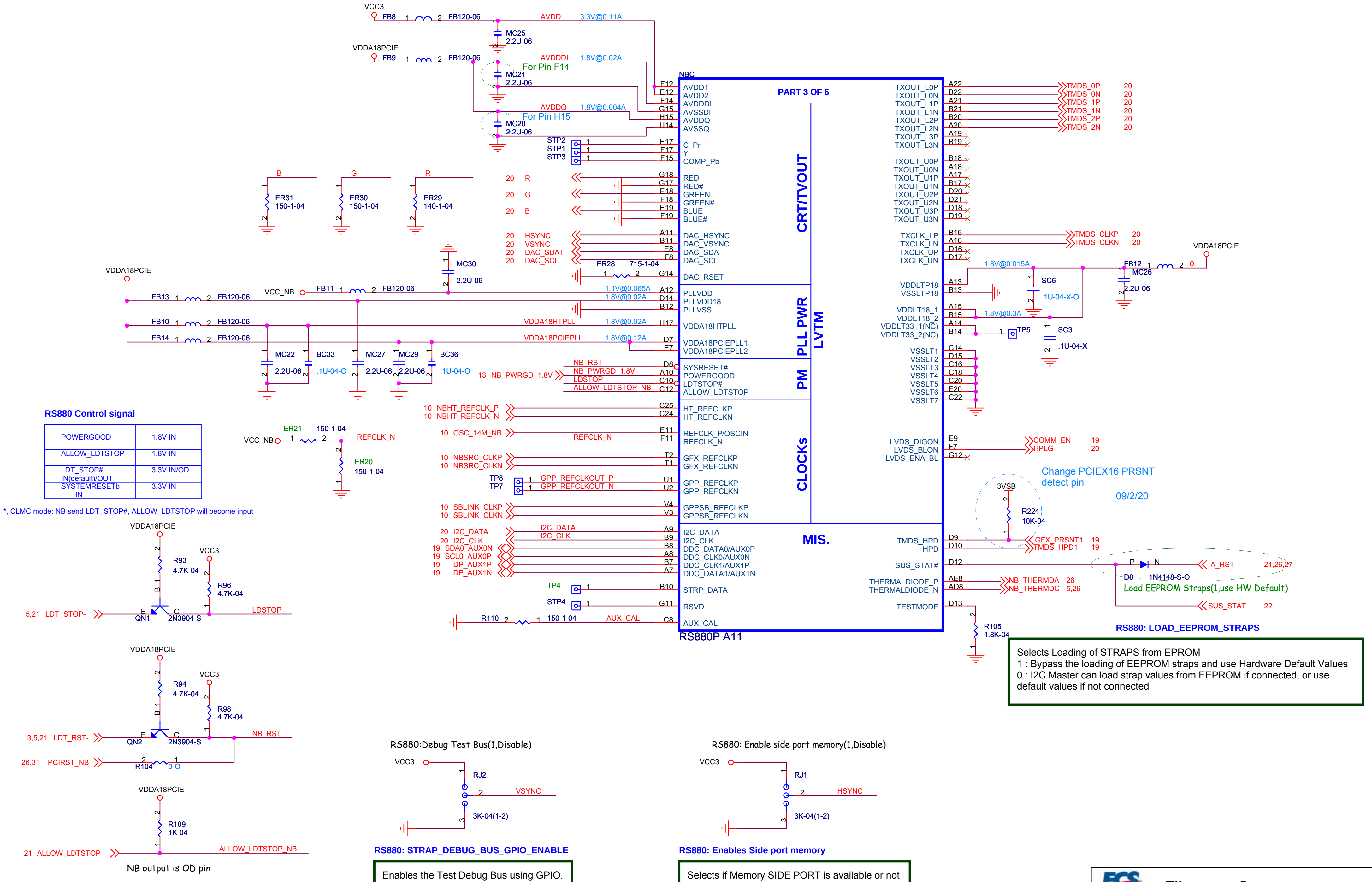
Title: NB:ATI RS880P/SB710 LINK I/F

Size: Custom | Document Number: A880GM-M6 | Rev: 1.0

Date: Thursday, April 29, 2010 | Sheet 15 of 36



Elitegroup Computer system	
Title	NB:ATI RS880P/SB710 PCI-E I/F
Size: Custom	Document Number: A880GM-M6
Rev: 1.0	
Date: Thursday, April 29, 2010	Sheet 16 of 36



NBC
PART 3 OF 6
CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKS
MIS.
RS880P A11
AVDD1
AVDD2
AVDDDI
AVSSDI
AVDDQ
AVSSQ
C_Pr
Y
COMP_Pb
RED
RED#
GREEN
GREEN#
BLUE
BLUE#
DAC_HSYNC
DAC_VSYNC
DAC_SDA
DAC_SCL
DAC_RSET
PLLVDD
PLLVDD18
PLLVSS
VDDA18HTPLL
VDDA18PCIEPLL1
VDDA18PCIEPLL2
SYSRESET#
POWERGOOD
LDTSTOP#
ALLOW_LDTSTOP
HT_REFCLKP
HT_REFCLKN
REFCLK_P/OSCIN
REFCLK_N
GFX_REFCLKP
GFX_REFCLKN
GPP_REFCLKP
GPP_REFCLKN
GPPSB_REFCLKP
GPPSB_REFCLKN
I2C_DATA
I2C_CLK
DDC_DATA0/AUX0P
DDC_CLK0/AUX0N
DDC_CLK1/AUX1P
DDC_DATA1/AUX1N
STRP_DATA
RSVD
AUX_CAL
TXOUT_L0P
TXOUT_L0N
TXOUT_L1P
TXOUT_L1N
TXOUT_L2P
TXOUT_L2N
TXOUT_L3P
TXOUT_L3N
TXOUT_U0P
TXOUT_U0N
TXOUT_U1P
TXOUT_U1N
TXOUT_U2P
TXOUT_U2N
TXOUT_U3P
TXOUT_U3N
TXCLK_LP
TXCLK_LN
TXCLK_UP
TXCLK_UN
VDDLTP18
VSSLTP18
VDDLT18_1
VDDLT18_2
VDDLT33_1(NC)
VDDLT33_2(NC)
VSSLT1
VSSLT2
VSSLT3
VSSLT4
VSSLT5
VSSLT6
VSSLT7
LVDS_DIGON
LVDS_BLON
LVDS_ENA_BL
TMDS_HPD
HPD
SUS_STAT#
THERMALDIODE_P
THERMALDIODE_N
TESTMODE
VCC3
FB8 FB120-06
AVDD 3.3V@0.11A
MC25 2.2U-06
VDDA18PCIE
FB9 FB120-06
AVDDDI 1.8V@0.02A
For Pin F14
MC21 2.2U-06
AVDDQ 1.8V@0.004A
For Pin H15
MC20 2.2U-06
STP2
STP1
STP3
ER31 150-1-04
ER30 150-1-04
ER29 140-1-04
MC30 2.2U-06
ER28 715-1-04
VCC_NB
FB11 FB120-06
1.1V@0.065A
1.8V@0.02A
FB13 FB120-06
FB10 FB120-06
FB14 FB120-06
VDDA18HTPLL 1.8V@0.02A
VDDA18PCIEPLL 1.8V@0.12A
MC22 2.2U-06
BC33 .1U-04-O
MC27 2.2U-06
MC29 2.2U-06
BC36 .1U-04-O
NB_RST
13 NB_PWRGD_1.8V
LDSTOP
ALLOW_LDTSTOP_NB
10 NBHT_REFCLK_P
10 NBHT_REFCLK_N
10 OSC_14M_NB
REFCLK_N
10 NBSRC_CLKP
10 NBSRC_CLKN
TP8
TP7
GPP_REFCLKOUT_P
GPP_REFCLKOUT_N
10 SBLINK_CLKP
10 SBLINK_CLKN
20 I2C_DATA
20 I2C_CLK
19 SDA0_AUX0N
19 SCL0_AUX0P
19 DP_AUX1P
19 DP_AUX1N
TP4
STP4
R110 150-1-04
AUX_CAL
ER21 150-1-04
ER20 150-1-04
TMDS_0P 20
TMDS_0N 20
TMDS_1P 20
TMDS_1N 20
TMDS_2P 20
TMDS_2N 20
TMDS_CLKP 20
TMDS_CLKN 20
1.8V@0.015A
FB12 0
MC26 2.2U-06
SC6 .1U-04-X-O
1.8V@0.3A
TP5
SC3 .1U-04-X
COMM_EN 19
HPLG 20
Change PCIEX16 PRSNT detect pin
09/2/20
3VSB
R224 10K-04
GFX_PRSNT1 19
TMDS_HPD1 19
D8 1N4148-S-O
-A_RST 21,26,27
Load EEPROM Straps(1,use HW Default)
NB_THERMDA 26
NB_THERMDC 5,26
SUS_STAT 22
R105 1.8K-04
QN1 2N3904-S
R93 4.7K-04
R96 4.7K-04
5,21 LDT_STOP-
LDSTOP
QN2 2N3904-S
R94 4.7K-04
R98 4.7K-04
3,5,21 LDT_RST-
NB_RST
26,31 -PCIRST_NB
R104 0-O
R109 1K-04
21 ALLOW_LDTSTOP
ALLOW_LDTSTOP_NB
NB output is OD pin
RJ2 3K-04(1-2)
VSYNC
RJ1 3K-04(1-2)
HSYNC

RS880 Control signal

POWERGOOD	1.8V IN
ALLOW_LDTSTOP	1.8V IN
LDT_STOP# IN(default)/OUT	3.3V IN/OD
SYSTEMRESETb IN	3.3V IN

*, CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input

RS880: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880:Debug Test Bus(1,Disable)

RS880: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO.
1 : Disable
0 : Enable

RS880: Enable side port memory(1,Disable)

RS880: Enables Side port memory

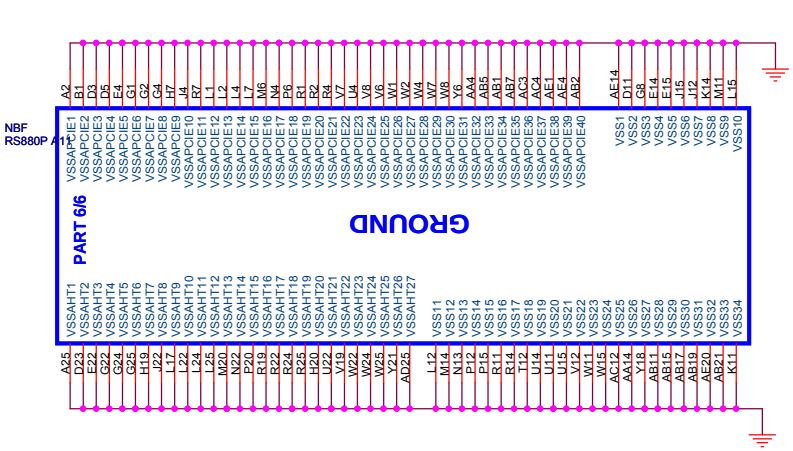
Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap:
NB_CLKCFG:CLK_TOP_SPARE_D[1]

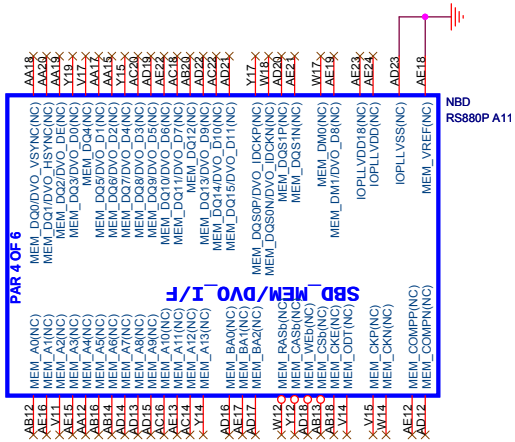
Elitegroup Computer system

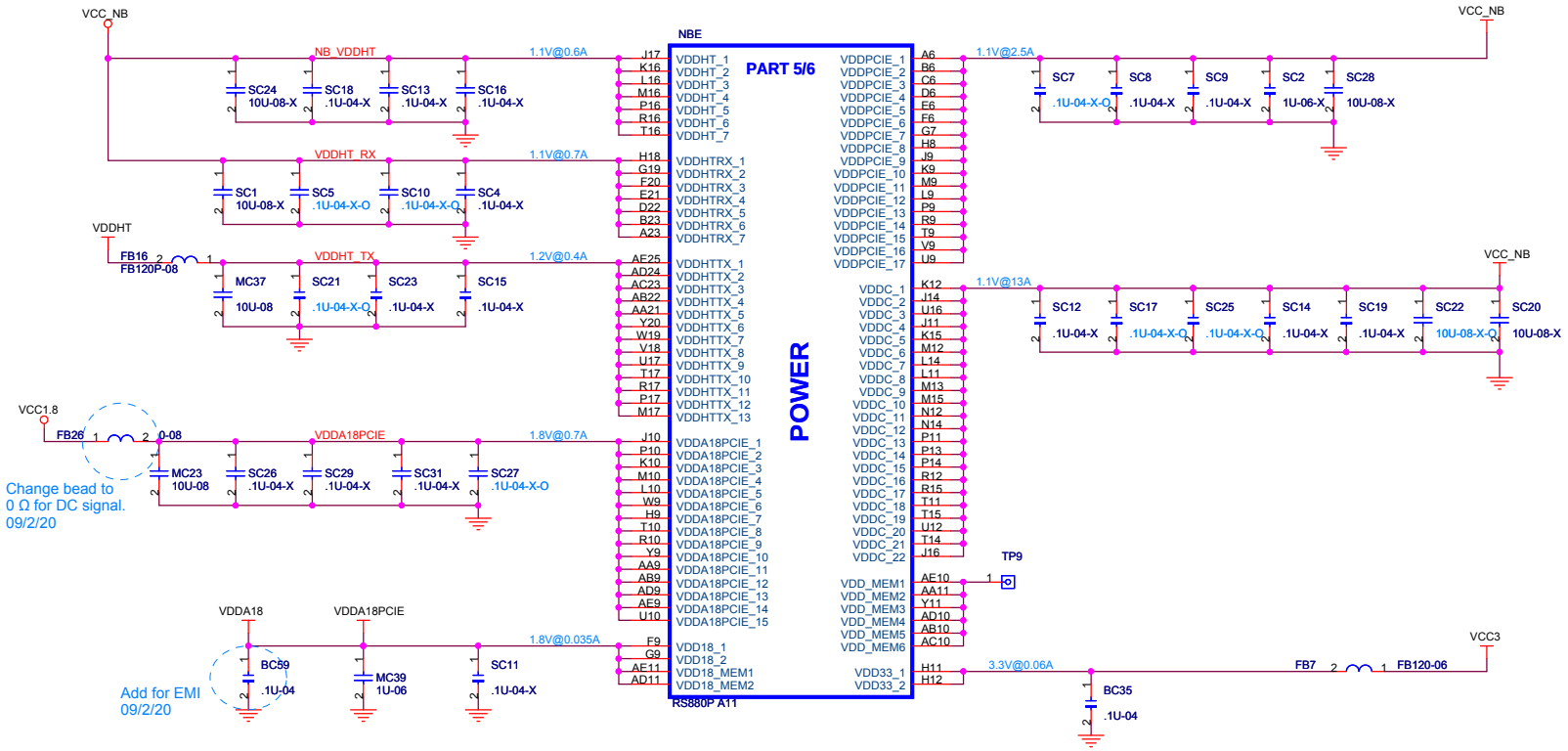
Title: NB: ATI RS880P/SB710 SYSTEM I/F

Size: Custom | Document Number: A880GM-M6 | Rev: 1.0

Date: Thursday, April 29, 2010 | Sheet 17 of 36

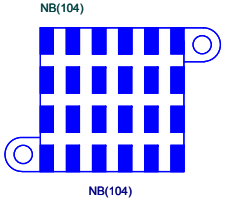






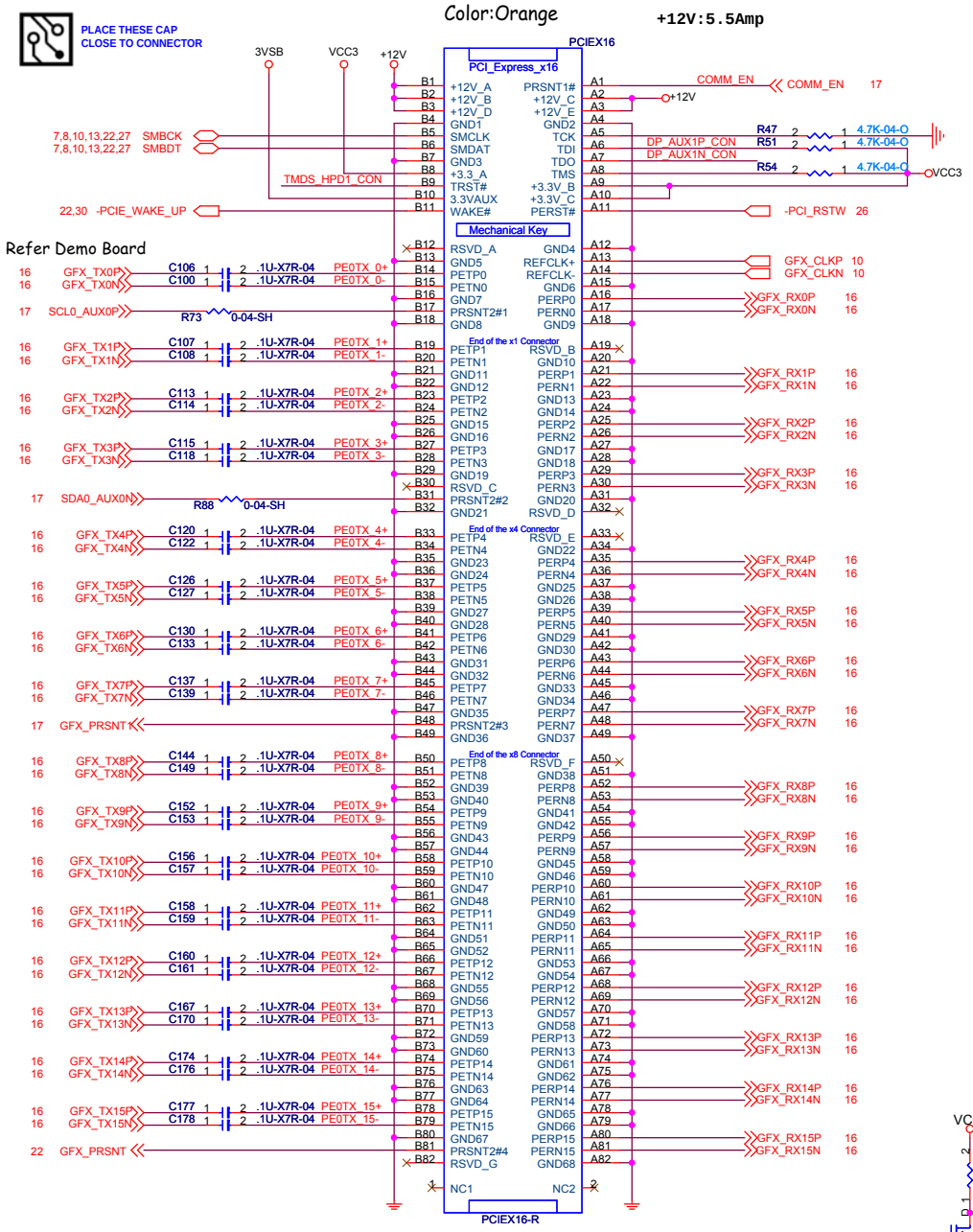
RS880 POWER TABLE

PIN NAME	RS880	VCC_NB: 1.1V	
VCC1.8V: 1.8V		VDDHT	0.6A
VDDA18PCIE	0.7A	VDDHTRX	0.7A
VDD18	0.01A	VDDPCIE	2.5A
VDD18_MEM	0.025A	VDDC	13A
PLLVDD18	0.02A	PLLVDD	0.065A
VDDA18HTPLL	0.02A	Total	16.865A
VDDA18PCIEPLL	0.12A	VCC3	
VDDLTP18	0.015A	VDD33	0.06A
VDDLT18	0.3A	AVDD	0.11A
AVDDDI	0.02A	Total	0.17A
AVDDQ	0.004A	VDDHT: 1.2V	
Total	1.234A	VDDHTTX	0.4A

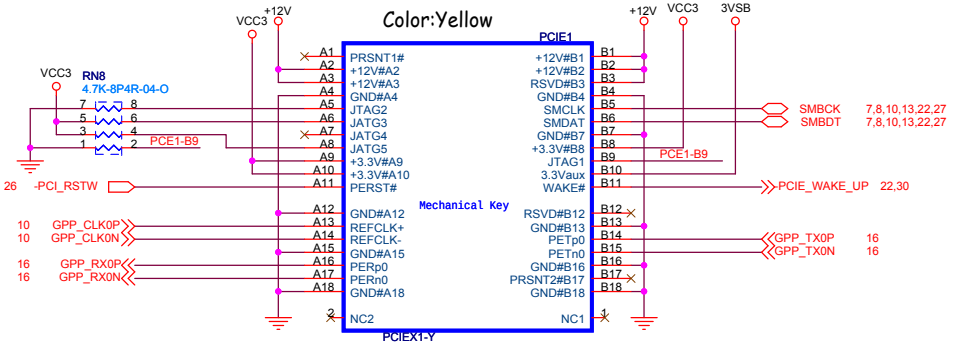


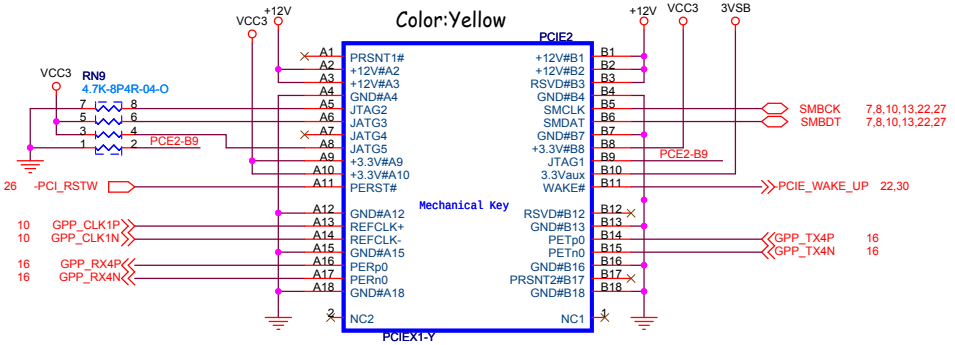
Elitegroup Computer Systems		
Title: NB RS880P/SB710 POWER		
Size: Custom	Document Number: A880GM-M6	Rev: 1.0
Date: Thursday, April 29, 2010	Sheet 18 of 36	

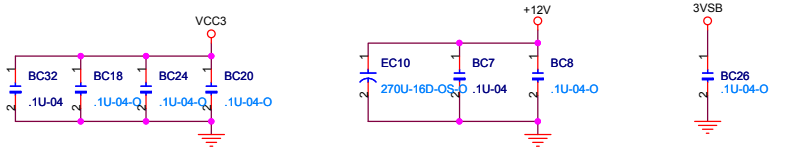
PCI_EXPRESS_x16

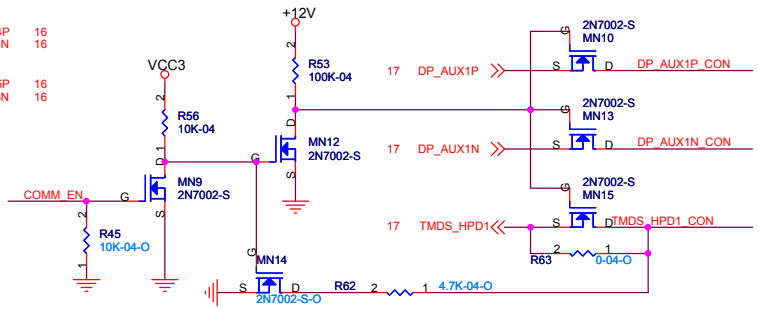


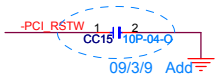
PCI_EXPRESS_x1

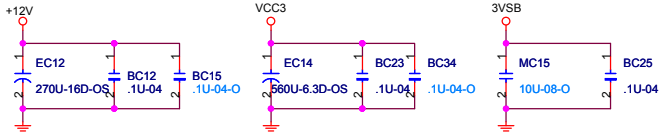






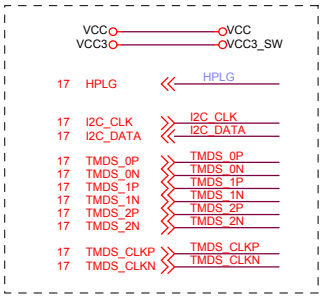


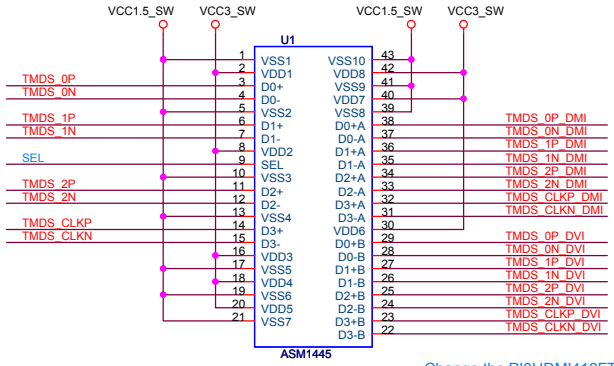




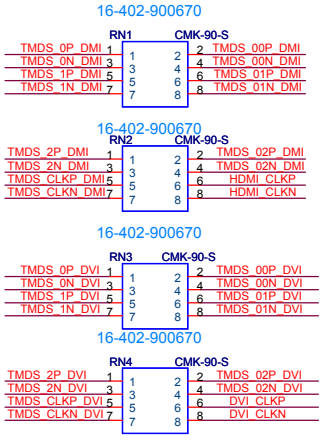
Elitegroup Computer Systems			
Title: PCI EXPRESS x16 & x1 SLOTS			
Size: Custom	Document Number: A880GM-M6		Rev: 1.0
Date: Thursday, April 29, 2010	Sheet 19 of 36		

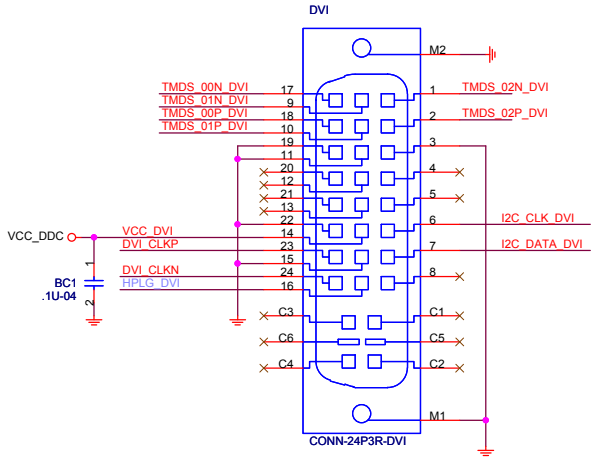
External Connection





16-402-900670



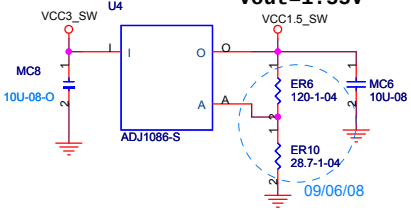


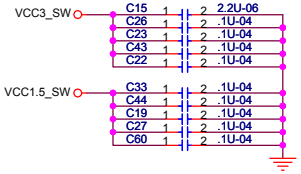
SEL	HDMI/DVI
0	HDMI
1	DVI

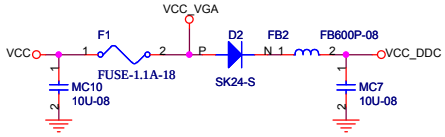
Change the PI3HDMI412FT-BZHES to ASM1445:(02-342-445070),Because of Leakage from the PI3HDMI412FT output differential line. 09/06/08

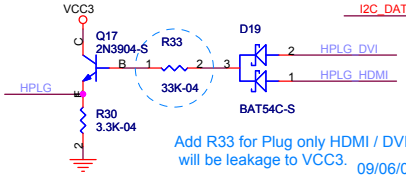
1.5V_SW

Vout=1.55V

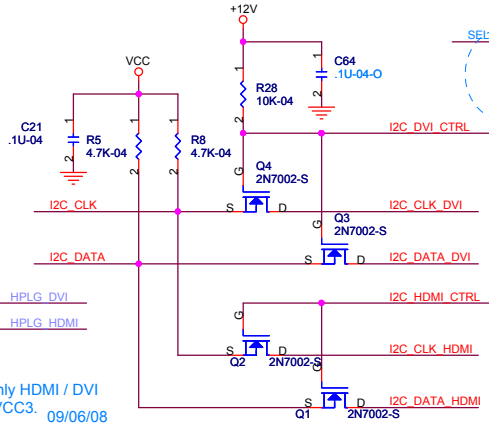




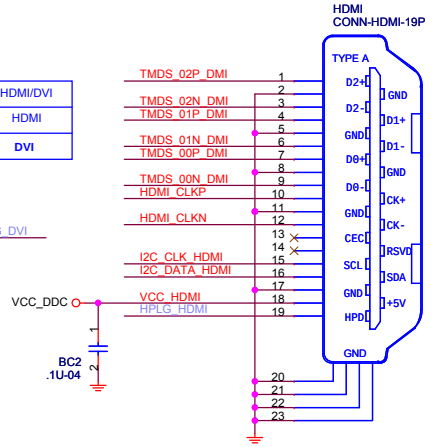




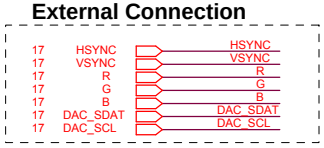
Add R33 for Plug only HDMI / DVI will be leakage to VCC3. 09/06/08

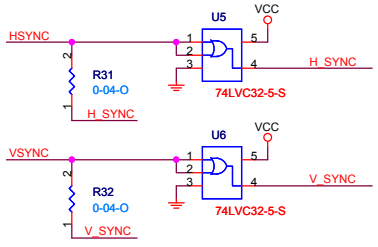


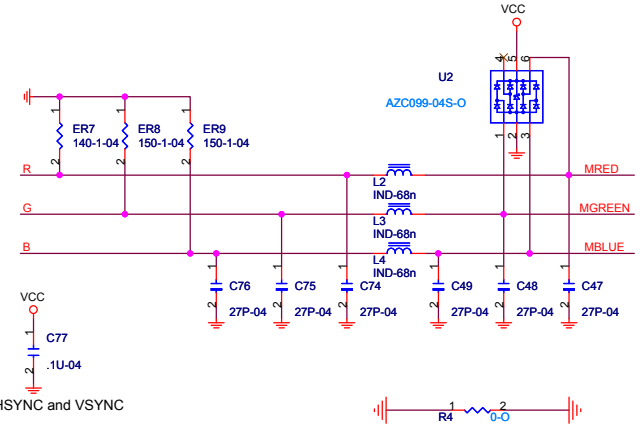
HDMI_DVI_SW	HDMI/DVI
0	HDMI
1	DVI



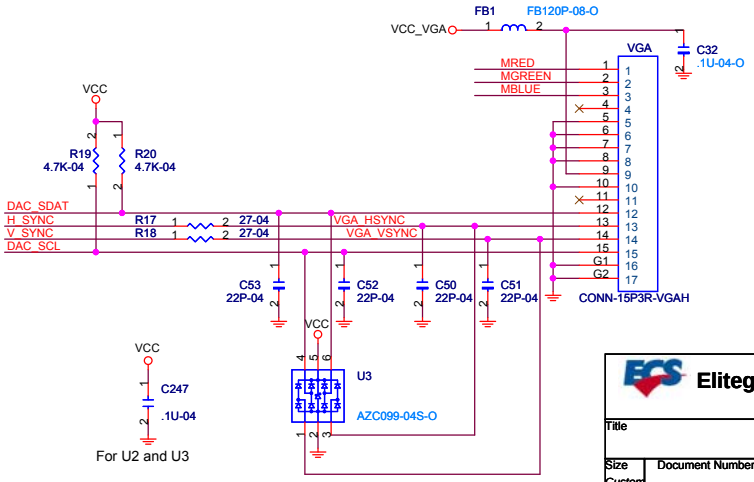
External Connection







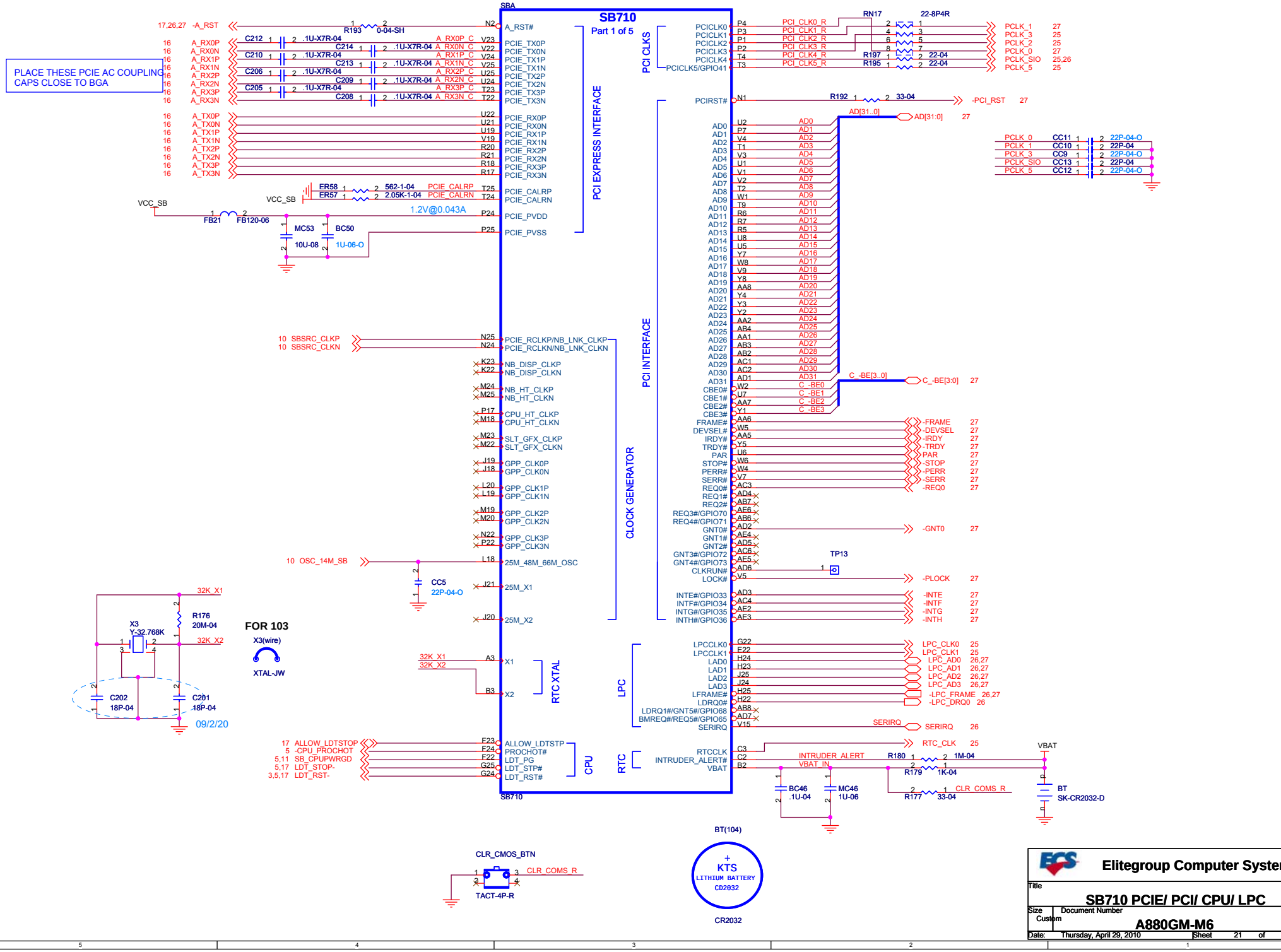
For HSYNC and VSYNC



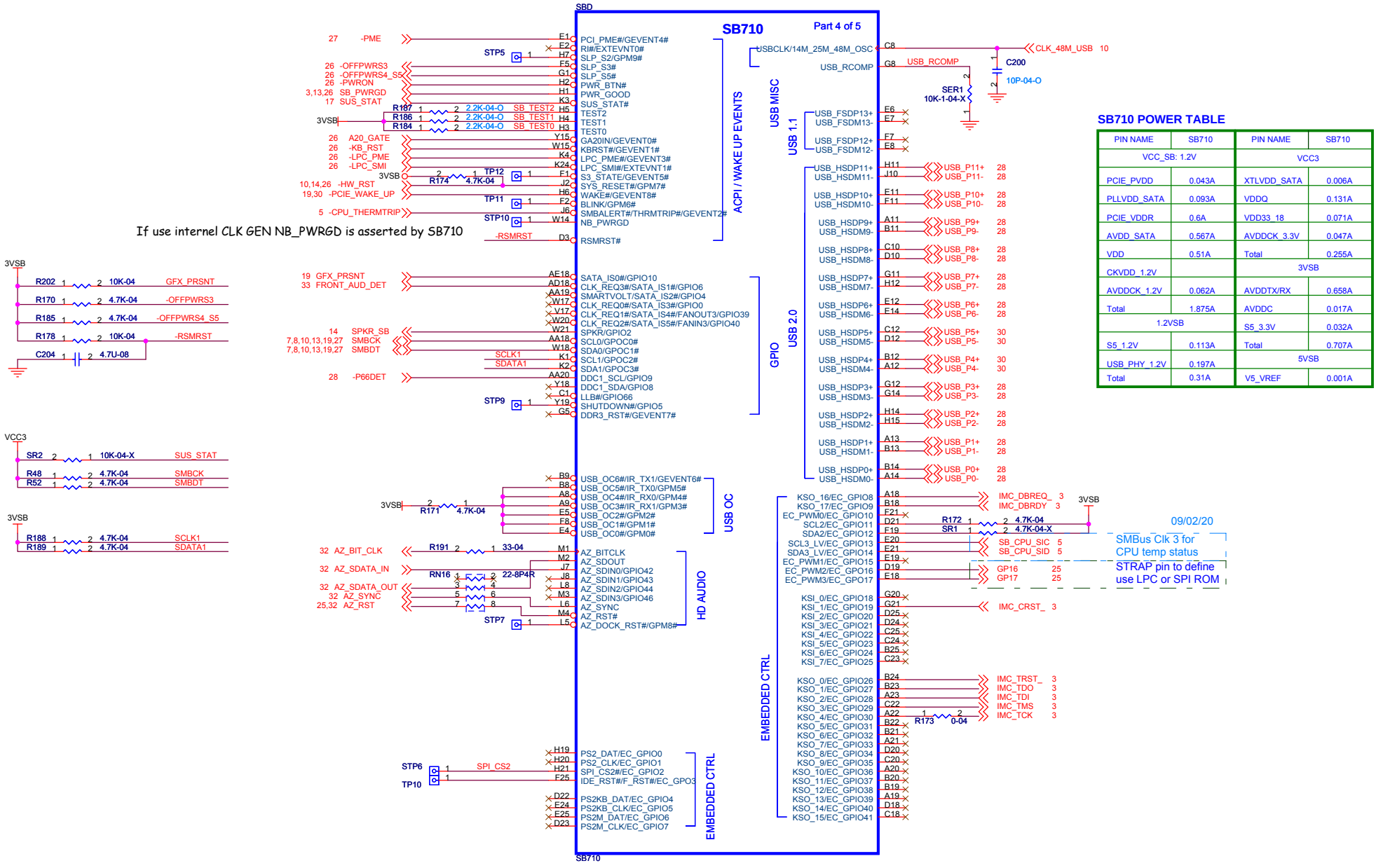
For U2 and U3

Elitegroup Computer Systems

Title	VGA,DVI,HDMI	
Size: Custom	Document Number: A880GM-M6	Rev: 1.0
Date: Monday, April 19, 2010	Sheet 20 of 36	



Elitegroup Computer Systems	
Title	SB710 PCIE/ PCI/ CPU/ LPC
Size: Custom	Document Number: A880GM-M6
Rev	1.0
Date: Thursday, April 29, 2010	Sheet 21 of 36


SB710
Part 4 of 5
If use internel CLK GEN NB_PWRGD is asserted by SB710
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
EMBEDDED CTRL
EMBEDDED CTRL
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
PS2_DAT/EC_GPIO0
PS2_CLK/EC_GPIO1
SPI_CS2#/EC_GPIO2
IDE_RST#/F_RST#/EC_GPO3
PS2KB_DAT/EC_GPIO4
PS2KB_CLK/EC_GPIO5
PS2M_DAT/EC_GPIO6
PS2M_CLK/EC_GPIO7
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSDP13+
USB_FSDM13-
USB_FSDP12+
USB_FSDM12-
USB_HSDP11+
USB_HSDM11-
USB_HSDP10+
USB_HSDM10-
USB_HSDP9+
USB_HSDM9-
USB_HSDP8+
USB_HSDM8-
USB_HSDP7+
USB_HSDM7-
USB_HSDP6+
USB_HSDM6-
USB_HSDP5+
USB_HSDM5-
USB_HSDP4+
USB_HSDM4-
USB_HSDP3+
USB_HSDM3-
USB_HSDP2+
USB_HSDM2-
USB_HSDP1+
USB_HSDM1-
USB_HSDP0+
USB_HSDM0-
KSO_16/EC_GPIO8
KSO_17/EC_GPIO9
EC_PWM0/EC_GPIO10
SCL2/EC_GPIO11
SDA2/EC_GPIO12
SCL3_LV/EC_GPIO13
SDA3_LV/EC_GPIO14
EC_PWM1/EC_GPIO15
EC_PWM2/EC_GPO16
EC_PWM3/EC_GPO17
KSI_0/EC_GPIO18
KSI_1/EC_GPIO19
KSI_2/EC_GPIO20
KSI_3/EC_GPIO21
KSI_4/EC_GPIO22
KSI_5/EC_GPIO23
KSI_6/EC_GPIO24
KSI_7/EC_GPIO25
KSO_0/EC_GPIO26
KSO_1/EC_GPIO27
KSO_2/EC_GPIO28
KSO_3/EC_GPIO29
KSO_4/EC_GPIO30
KSO_5/EC_GPIO31
KSO_6/EC_GPIO32
KSO_7/EC_GPIO33
KSO_8/EC_GPIO34
KSO_9/EC_GPIO35
KSO_10/EC_GPIO36
KSO_11/EC_GPIO37
KSO_12/EC_GPIO38
KSO_13/EC_GPIO39
KSO_14/EC_GPIO40
KSO_15/EC_GPIO41
SB710 POWER TABLE
PIN NAME | SB710 | PIN NAME | SB710
VCC_SB: 1.2V | | VCC3 |
PCIE_PVDD | 0.043A | XTLVDD_SATA | 0.006A
PLLVDD_SATA | 0.093A | VDDQ | 0.131A
PCIE_VDDR | 0.6A | VDD33_18 | 0.071A
AVDD_SATA | 0.567A | AVDDCK_3.3V | 0.047A
VDD | 0.51A | Total | 0.255A
CKVDD_1.2V | | 3VSB |
AVDDCK_1.2V | 0.062A | AVDDTX/RX | 0.658A
Total | 1.875A | AVDDC | 0.017A
1.2VSB | | S5_3.3V | 0.032A
S5_1.2V | 0.113A | Total | 0.707A
USB_PHY_1.2V | 0.197A | 5VSB |
Total | 0.31A | V5_VREF | 0.001A
09/02/20
SMBus Clk 3 for CPU temp status
STRAP pin to define use LPC or SPI ROM
Elitegroup Computer Systems
Title
SB710 APCI/ GPIO/ USB/ AUDIO
Size Custom
Document Number A880GM-M6
Rev 1.0
Date: Thursday, April 29, 2010
Sheet 22 of 36

PLACE SATA AC COUPLING CAPS CLOSE TO SB710

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB710

NOTE:
SER2 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

SB710
Part 2 of 5

SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR

SATA_CAL
SATA_X1
SATA_X2
SATA_ACT#/GPIO67
PLLVDD_SATA
XTLVDD_SATA

HWM_AGND TRACE AT LEAST 10MIL WIDE

09/06/06

SPI_DEBUG

For SPI ROM

Co-lay

AMI 8Mb ROM

SATA1/2A
SATA1/2B
SATA3/4A
SATA3/4B
SATA5/6A
SATA5/6B
SATA*2-90D-OR

Elitegroup Computer Systems	
Title	SB710 SATA / IDE / HWM / SPI
Size: Custom	Document Number: A880GM-M6
Rev	1.0
Date: Thursday, April 29, 2010	Sheet 23 of 36

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

SB710
Part 3 of 5

POWER

3.3 V power for PATA interface

FB install for SB710, DNI for SB700

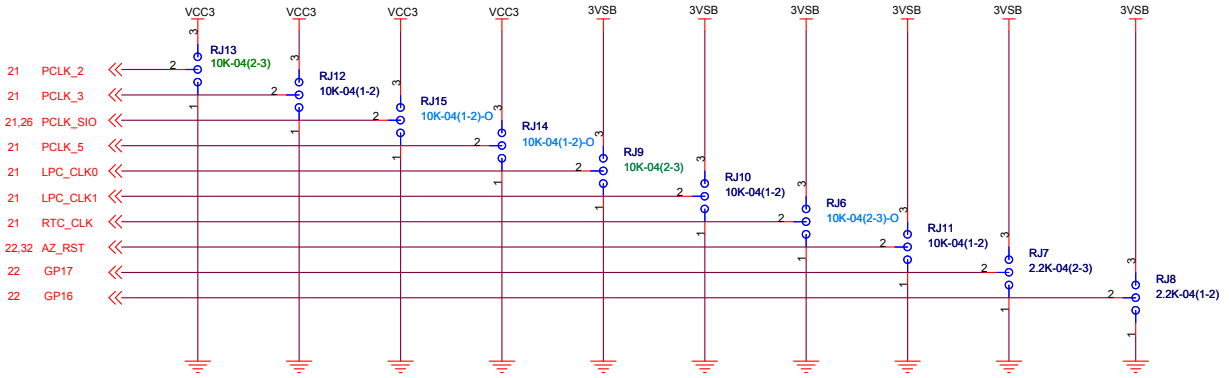
pin H18 needs dedicated via to GND

SB710
Part 5 of 5

GROUND

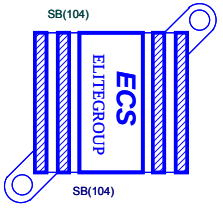
Elitegroup Computer Systems	
Title	SB710 STRAPS/ PWR/ DECOUPLING
Size: Custom	Document Number: A880GM-M6
Rev	1.0
Date: Thursday, April 29, 2010	Sheet 24 of 36

NOTE: SB710 HAS INTERNAL 10K PULL UP RESISTOR FOR RTC_CLK



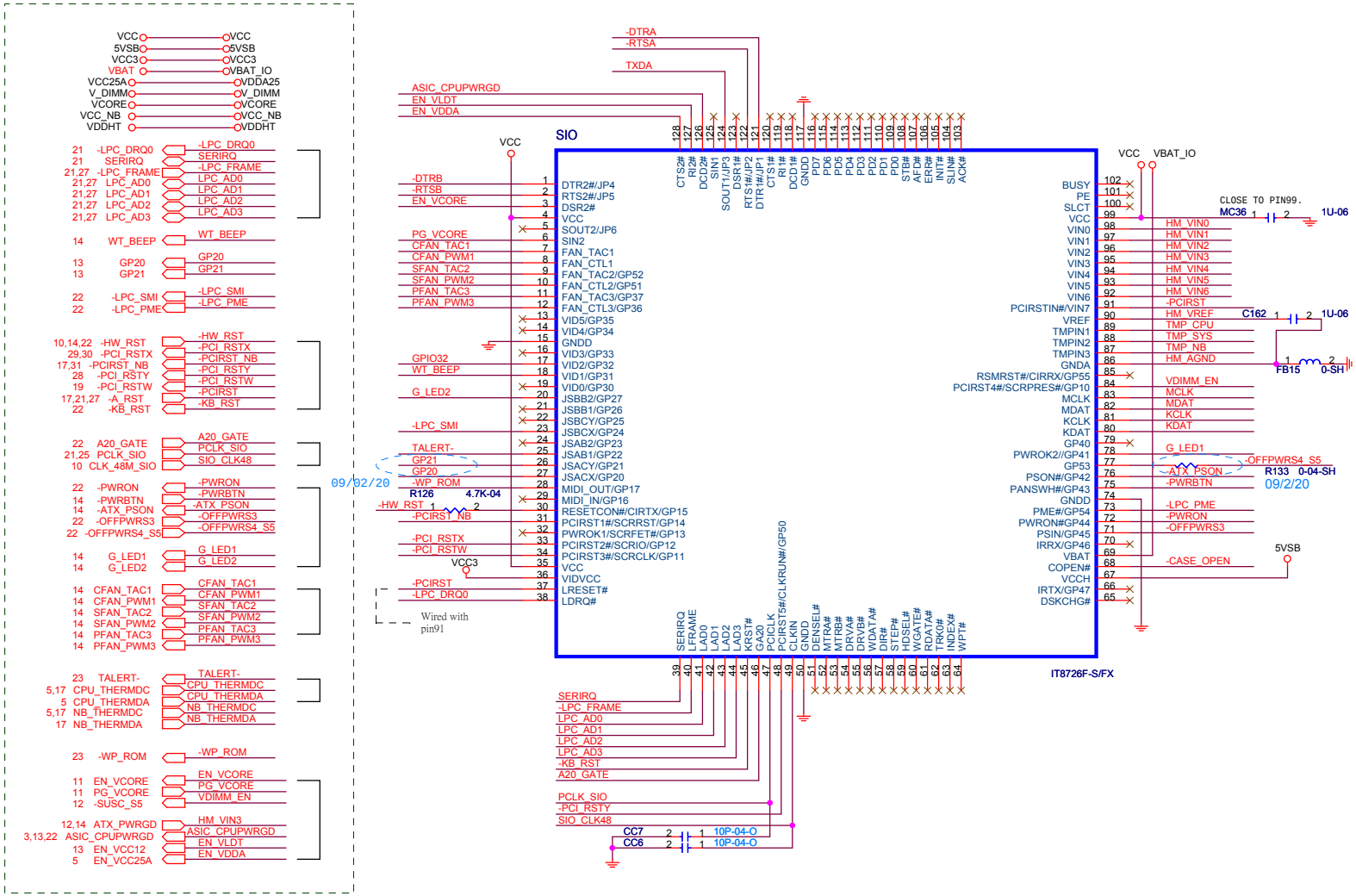
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17 GP16
PULL HIGH	Watchdog ENABLED DEFAULT	USE DEBUG STRAPS	RESERVED	RESERVED	IMC Enable DEFAULT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	PCI ROM BOOT Enable	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT L, H = LPC ROM L, L = FWH ROM
PULL LOW	Watchdog DISABLED	IGNORE DEBUG STRAPS DEFAULT			IMC Disable	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	PCI ROM BOOT Disable DEFAULT	

REQUIRED STRAPS

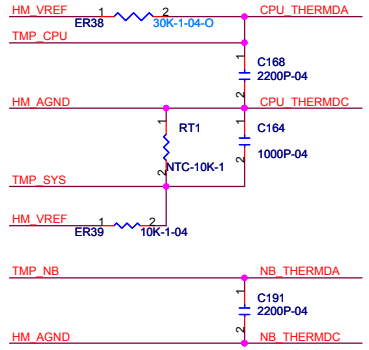


Elitegroup Computer Systems		
Title: SB710 Straps		
Size: Custom	Document Number: A880GM-M6	Rev: 1.0
Date: Thursday, April 29, 2010	Sheet 25 of 36	

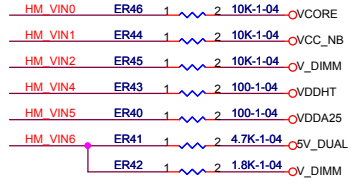
External Connection



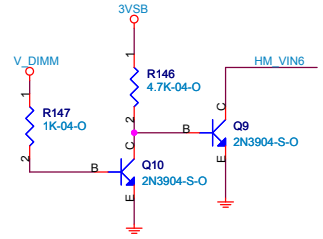
Thermal Monitor



Voltage detection



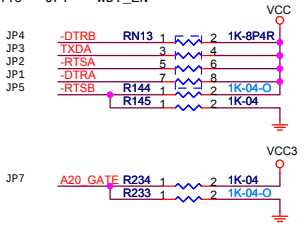
HM_VIN3 for ATX PWRGD

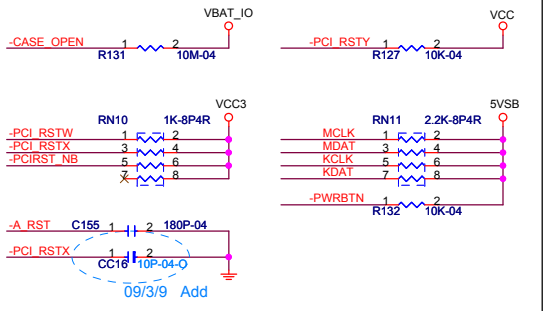


For AMD Power Sequence necessary

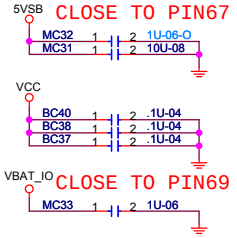
HW STRAPPING

Pin121	JP1	Flashseg1_EN	1:Disable
Pin122	JP2	SerFlh_SO_SEL	1:FLH_SO2
Pin124	JP3	CHIP_SEL	CHIP_SEL
Pin1	JP4	BUF_SEL	1:PCIRST# O.D.
Pin2/46	JP5/7	FAN_CTL_SEL	
Pin5	JP6	VID_ISEL	
Pin46	JP7	WDT_EN	

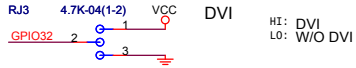




BYPASS CAP



BIOS SELECTION



Elitegroup Computer Systems			
Title: LPC SIO - ITE8726F/IX,ROM			
Size: Custom	Document Number: A880GM-M6		Rev: 1.0
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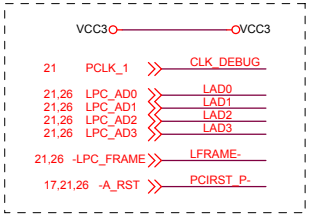
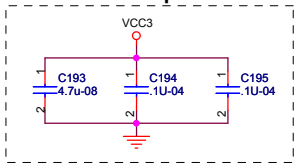
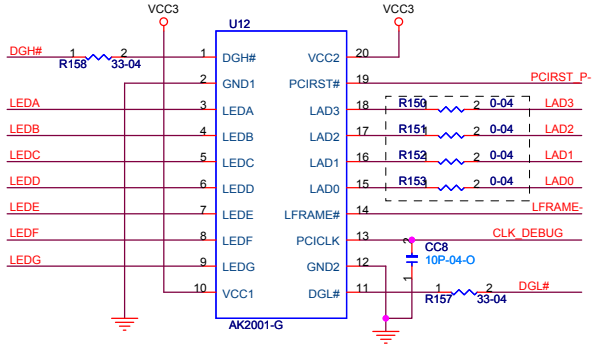
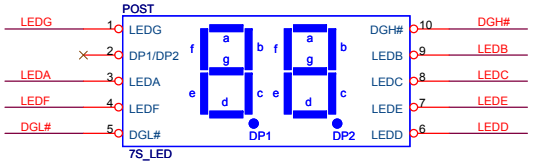
External Connection



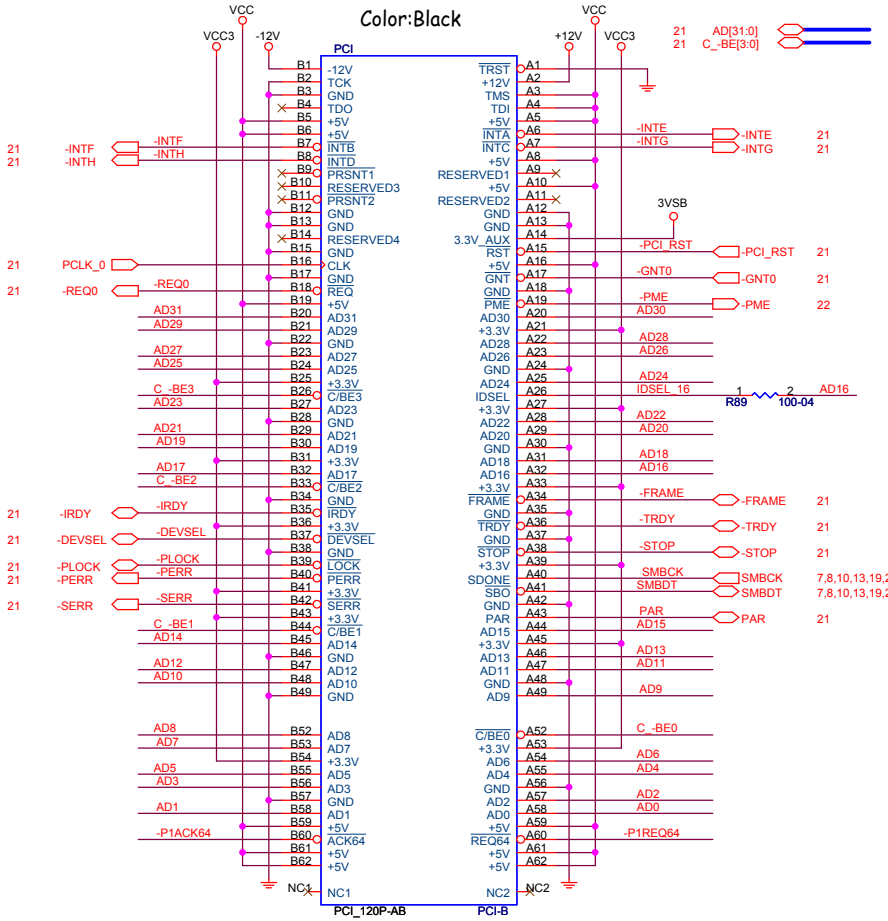
Close to U12 power Pin



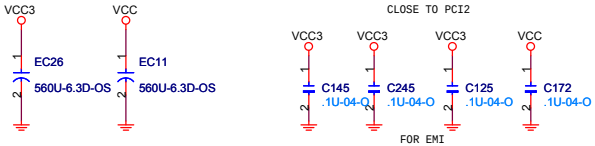


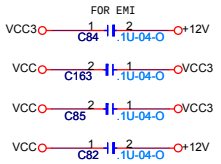


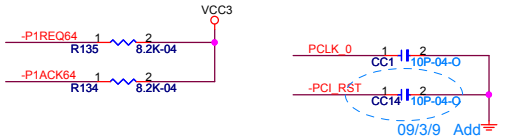
Color:Black



INT:E
IDSEL:AD16







Elitegroup Computer Systems

Title: PCI Slot, LPC DEBUG CARD

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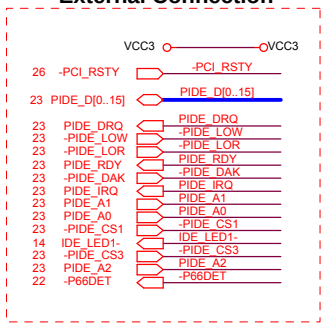
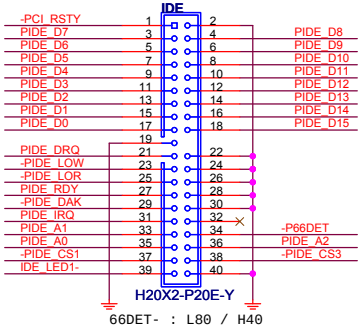
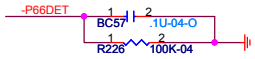
External Connection



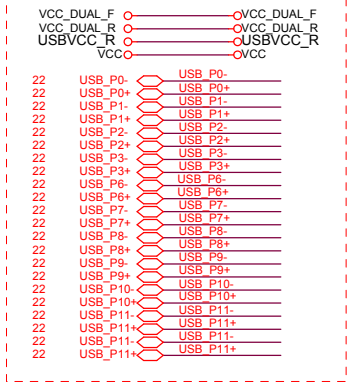


66DET- : L80 / H40



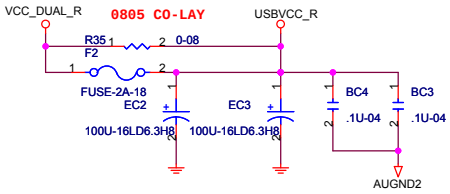
		ATi	Intel	NV	VIA	SiS
Pin 3	PDD7:	X	Pull Hi: 4.7K	Pull Hi: 4.7K	Pull Hi: 4.7K	X
Pin 21	PDDREQ	X	Pull Hi: 8.2K	Pull Lo: 5.6K	Pull Hi: 4.7K	X
Pin 27	PIORDY	X	X	Pull Lo: 10K	Pull Lo: 10K	Pull Lo: 5.6K
Pin 31	PIDE_IRQ	X	X	Pull Lo: 5.6K	Pull Lo: 5.6K	X
Pin 34	P66DET-	100K	27K	15K	10K	20K

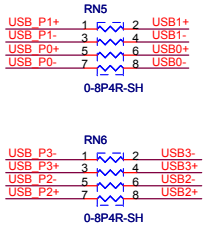
External Connection

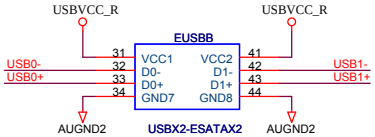


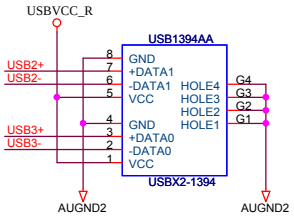
150 Mils Width

Power for Rear USB Ports

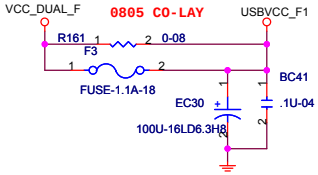


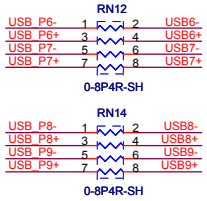


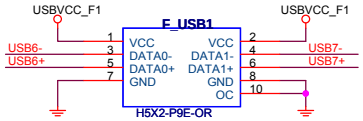


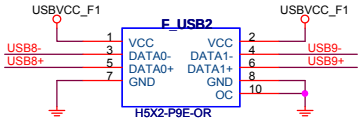


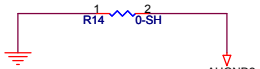
Power for Front USB Ports

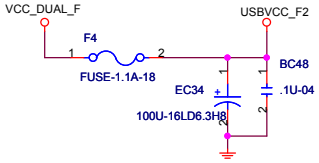


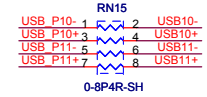


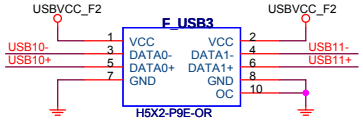












Elitegroup Computer Systems

Title: USB,IDE,VGA

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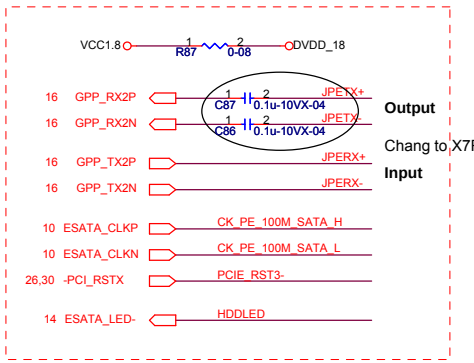
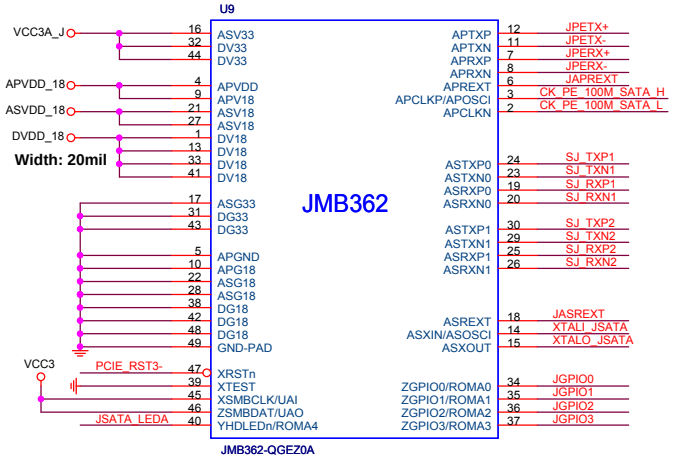
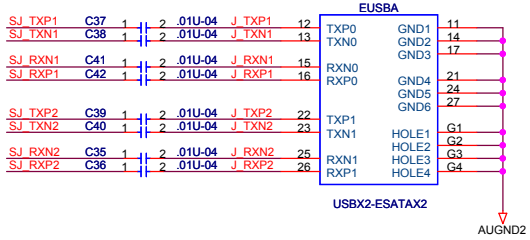
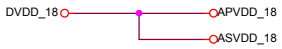
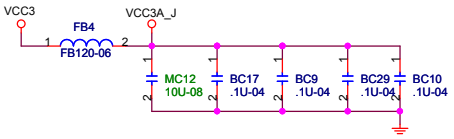
External Connection

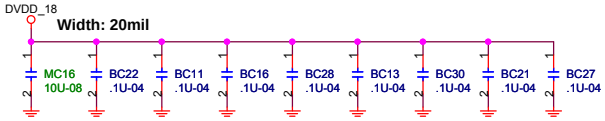


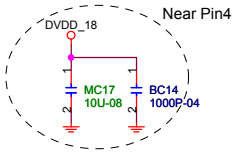


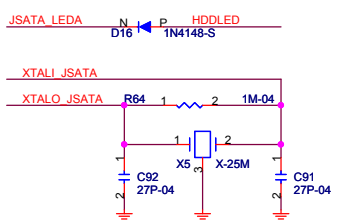


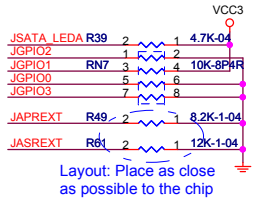












Elitegroup Computer Systems

Title	JMB362 Dual eSATA		
Size: Custom	Document Number: A880GM-M6		Rev: 1.0
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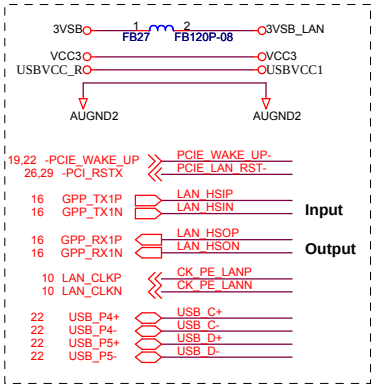
External Connection



When you found some bug, please inform
Ren(ext:665) to update circuit.

新手提醒:

LAN_HSOP/N請接到SB的PCIE RX端

LAN_HSIP/N請接到SB的PCIE TX端

LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

RTL8103EL-GR
01-278-103350

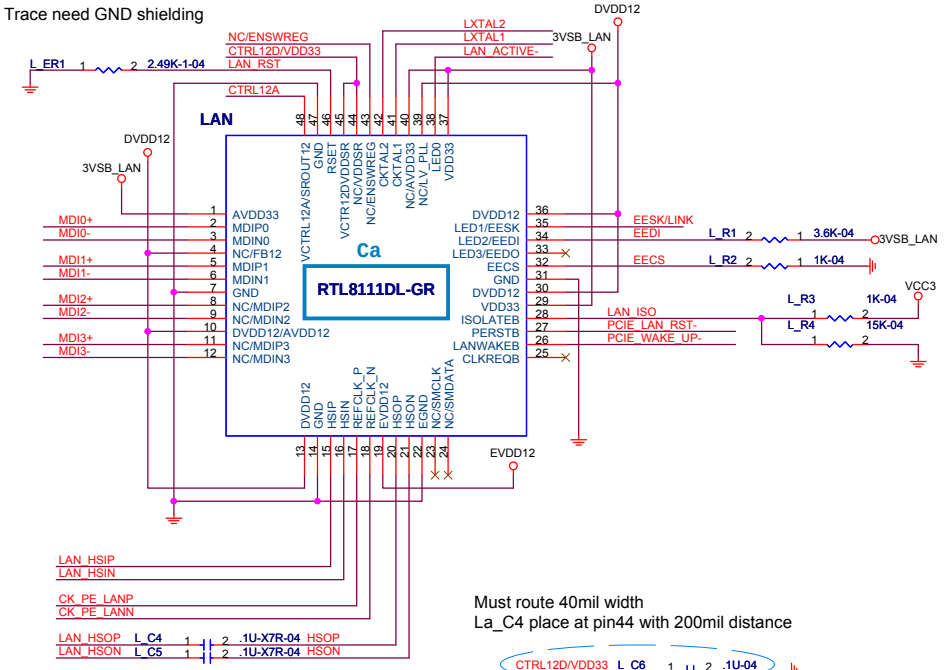
BOM Difference

	RTL8111DL-GR 1000M	RTL8103EL-GR 10/100M
Ca	RTL8111DL-GR	RTL8103EL-GR
Cb	X	V
Cc	0-04	.01U-04
Cd	X	V
Ce	V	X
Cf	USBX2-LAN-1000	USBX2-LAN-100

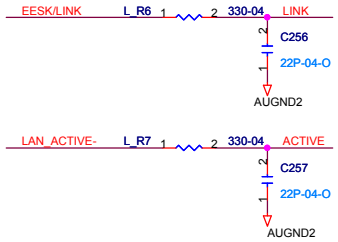
Power Difference

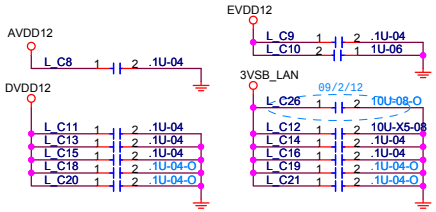
	RTL8111D	RTL8103E
AVDD33 VDD33	3.3V 3VSB供應	3.3V 3VSB供應
CTRL12A	SWitching Output	1.2V pinself 供應
DVDD12	1.2V CTRL12A供應	1.2V pinself 供應
EVDD12	1.2V CTRL12A供應	1.2V pinself 供應

RSET電阻需close to LAN
Trace need GND shielding

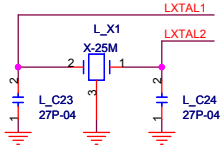


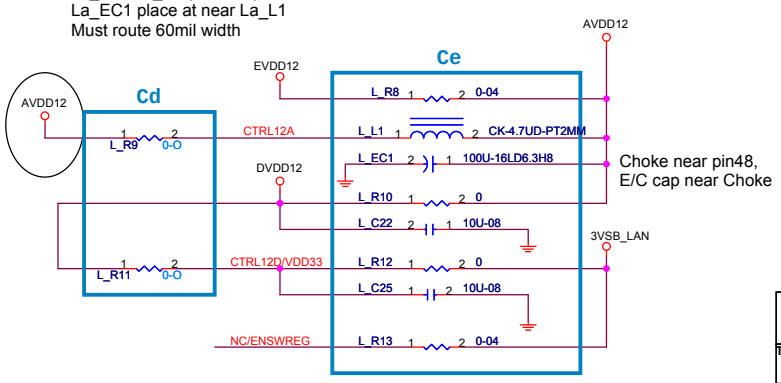
Must route 40mil width
La_C4 place at pin44 with 200mil distance



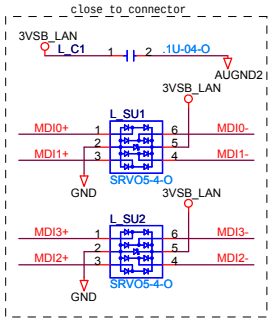


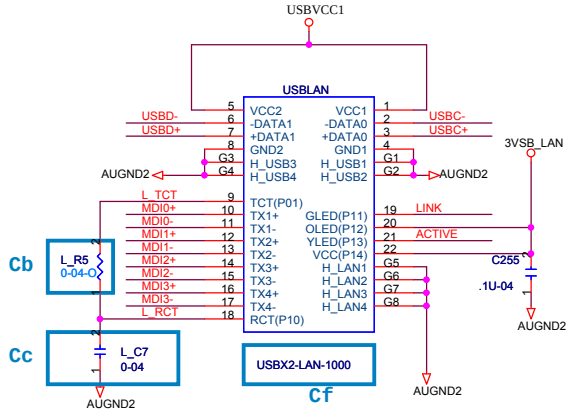
La_L1 &La_R9 place at pin48 with 200mil distance
La_EC1 place at near La_L1
Must route 60mil width





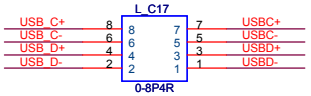
Choke near pin48,
E/C cap near Choke

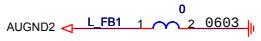




Link: Green on

Active: Yellow blinking





Elitegroup Computer Systems	
Title	PCIE LAN RTL8111DL
Size: Custom	Document Number: A880GM-M6
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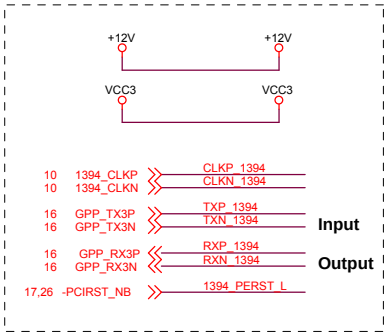
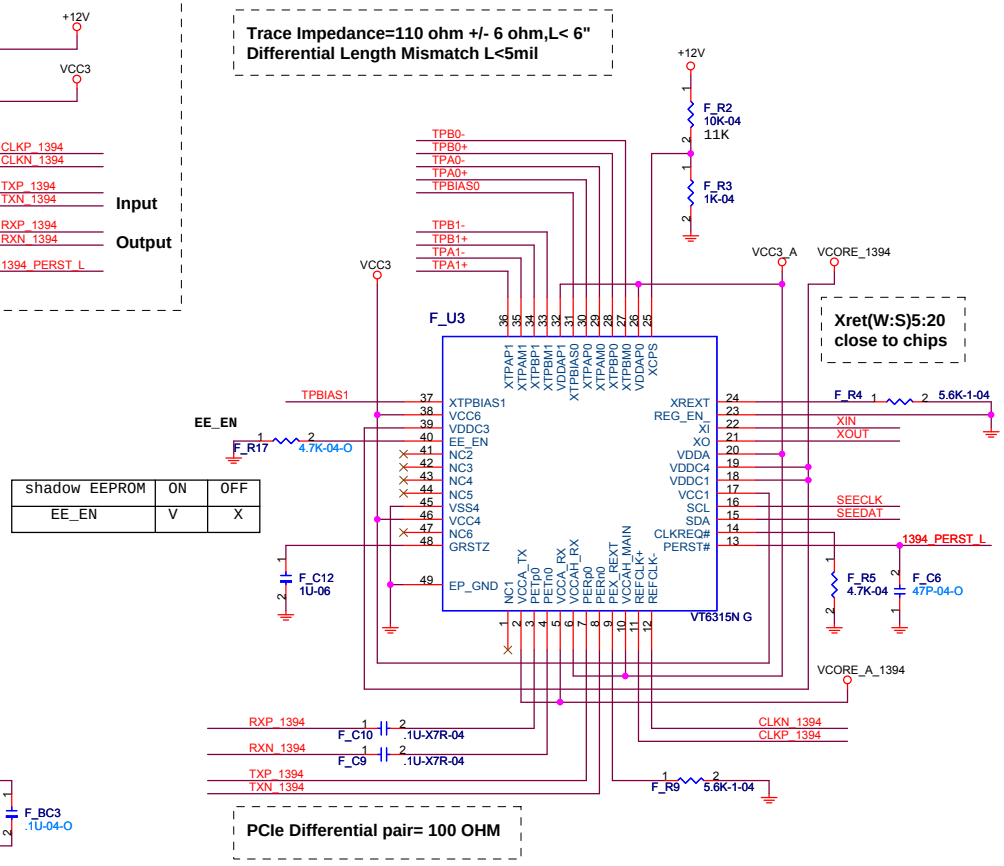
External Connection



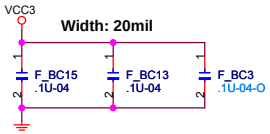
Trace Impedance=110 ohm +/- 6 ohm,L< 6"
Differential Length Mismatch L<5mil

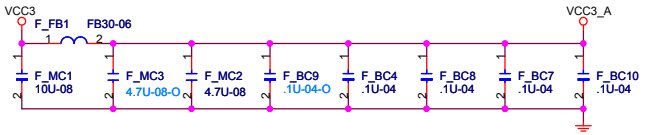


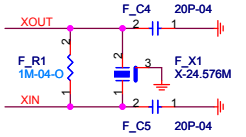
Xret(W:S)5:20
close to chips

shadow EEPROM	ON	OFF
EE_EN	V	X

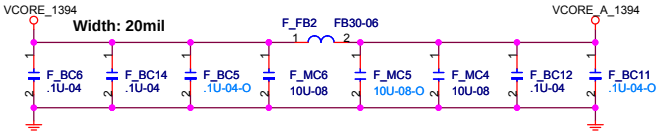
PCIe Differential pair= 100 OHM

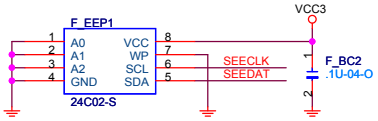




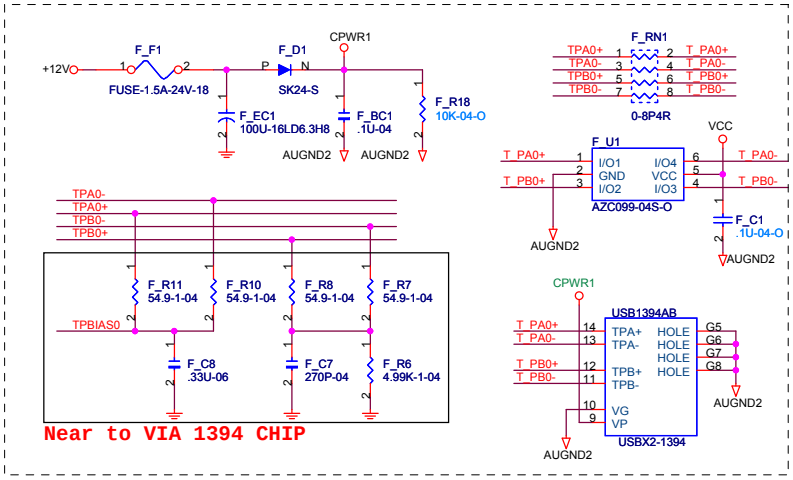


Xout,Xin (W:S)5:15mil
close to chips

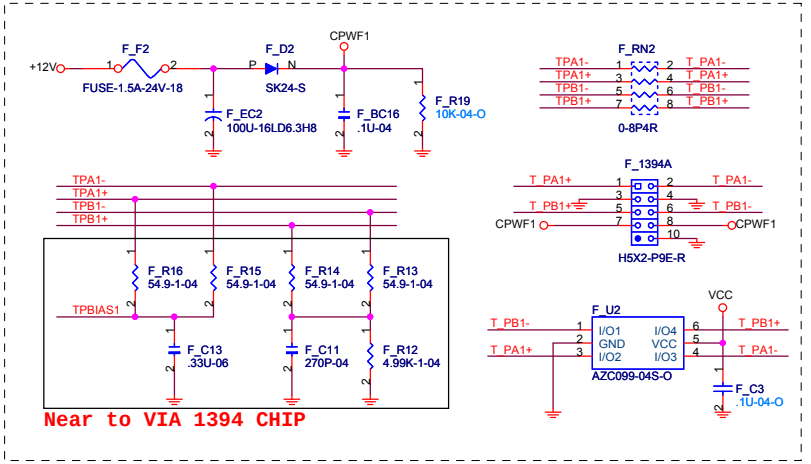




Rear I/O



Front 1394 Panel



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External Connection

5VSB — 5VSB
VCC — VCC
+12V — +12V
VCC3 — VCC3

22,25 AZ_RST — AZ_RST-
22 AZ_BIT_CLK — AZ_BIT_CLK
22 AZ_SYNC — AZ_SYNC
22 AZ_SDATA_IN — AZ_SDAIN
22 AZ_SDATA_OUT — AZ_SDOUT

AGND AUGND

22,33 FRONT_AUD_DET — FRONT_AUD_DET 22,33

For AC97 Header Judgement
GPI to South Bridge

When you found some bug, please inform Ren(ext:665) to update circuit.

AR8 0 — AUGND
AR40 0 — AUGND

Improve the background noise of MIC boost

+12V — AD3 1N4148-S — AU1 78L05-D (VIN, VOUT, GND) — MC9 10U-08 — AUGND
+5VA — AEC1 100U-16LD6.3H8 — AUGND
5VSB — AD4 BAT54C-S

09/2/20

FRONT_R — FRONT_R 33
FRONT_L — FRONT_L 33
MIC1_VREFO_R
LINE2_VREFO
MIC2_VREFO
MIC1_VREFO_L
+5VA — AEC2 100U-16LD6.3H8 — AEC3 100U-16LD6.3H8 — NetB — 10K-04-O — For ALC883 — AR7
MC3 10U-X5-08 — AUGND
+5VA — MC4 10U-08 — AC1 .1U-04 — AUGND

CODEC

LC888S-GRS

PORT-D_R, PORT-D_L, SENSE B, VrefOut-G, VrefOut-D, VrefOut-E, VrefOut-F, VrefOut-C_L, VrefOut-B_L, VREF FILT, AVSS1, AVDD1

AUGND — AC14 .1U-04 — VrefOut-A
AUGND — MC5 10U-08 +5VA — AVDD2
33 SURR_L — C6 10U-X5-08 — PORT-A_L
AUGND — AER1 20K-1-04 VOHR — VrefOut-H
33 SURR_R — C18 10U-X5-08 — PORT-A_R
AUGND — AVSS3
33 CEN — CEN — C17 10U-X5-08 — PORT-G_L
33 LFE — LEF — C16 10U-X5-08 — PORT-G_R
PORT-H_L
PORT-H_R
S/PDIF IN / EAPD
33 SPDIF_OUT — S/PDIF-OUT — AC22 100P-04

LINE1-R/PORT-C_R — C28 10U-X5-08 — LINE1_R — LINE1_R 33
LINE1-L/PORT-C_L — C29 10U-X5-08 — LINE1_L — LINE1_L 33
MIC1-R/PORT-B_R — C30 10U-X5-08 — MIC1_R — MIC1_R 33
MIC1-L/PORT-B_L — C31 10U-X5-08 — MIC1_L — MIC1_L 33
CD-R
CD-G
CD-L
MIC2-R/PORT-F_R — AEC4 100U-16LD6.3H8 — MIC2_R — MIC2_R 33
MIC2-L/PORT-F_L — AEC5 100U-16LD6.3H8 — MIC2_L — MIC2_L 33
LINE2-R/PORT-E_R — AEC6 100U-16LD6.3H8 — LINE2_R — LINE2_R 33
LINE2-L/PORT-E_L — AEC7 100U-16LD6.3H8 — LINE2_L — LINE2_L 33
SENSE A — NetA

09/2/20

09/3/10 Add

DVDD_CORE, GPIO0/SPDIFO2, GPIO1, DVSS, SDO, BCLK, DVSS, SDI, DVDD_CORE, SYNC, RESET#, PC_BEEP

AGND

GND

If have HDA link support scalable I/O, need be separated.

VCC3 — MC11 10U-08 — AC17 .1U-04
AC15 .1U-04
ATP1 — TPAZ_RST-
AZ_SYNC
AR29 22-04 — AZ_SDAIN
AZ_BIT_CLK
33 SPDIF_OUT2
AZ_SDOUT
AC16 22P-04

Verfout bias for stereo microphone.

MIC1_VREFO_R — AR6 2.2K-04 — MIC1_R
MIC1_VREFO_L — AR5 2.2K-04 — MIC1_L

AD1 BAT54A-S — LINE2_VREFO — AR2 2.2K-04 — LINE2_R; AR1 2.2K-04 — LINE2_L
AD2 BAT54A-S — MIC2_VREFO — AR4 2.2K-04 — MIC2_R; AR3 2.2K-04 — MIC2_L

Resistors Networks

Place near codec

ALC888 mount

NetA
AER6 5.1K-1-04 — FRONT_JD — FRONT_JD 33
AER5 10K-1-04 — LINE1_JD — LINE1_JD 33
AER7 20K-1-04 — MIC1_JD — MIC1_JD 33
AER8 39.2K-1-04 — SURR_JD — SURR_JD 33

NetB
AER4 10K-1-04 — CEN_JD — CEN_JD 33
AER3 20K-1-04 — MIC2_JD — MIC2_JD 33
AER2 39.2K-1-04 — LINE2_JD — LINE2_JD 33

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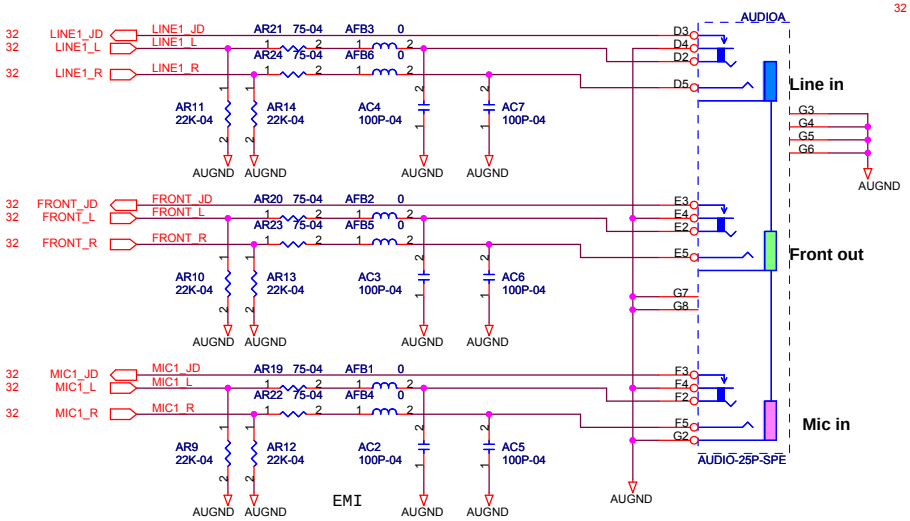
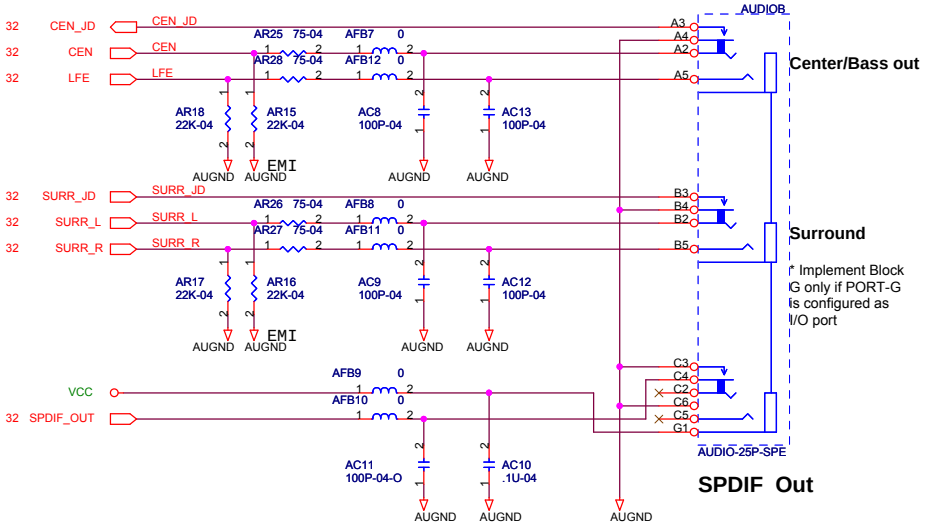
08.05.08 follow Realtek's suggusetion

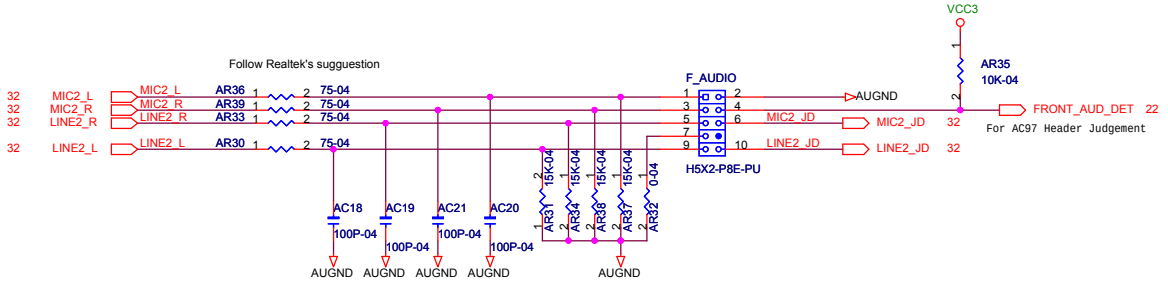
Rear Panel Onboard Analog I/O



Rear Panel (Optional Rear Audio Panel)



Follow Realtek's suggestion



SPDIF Out

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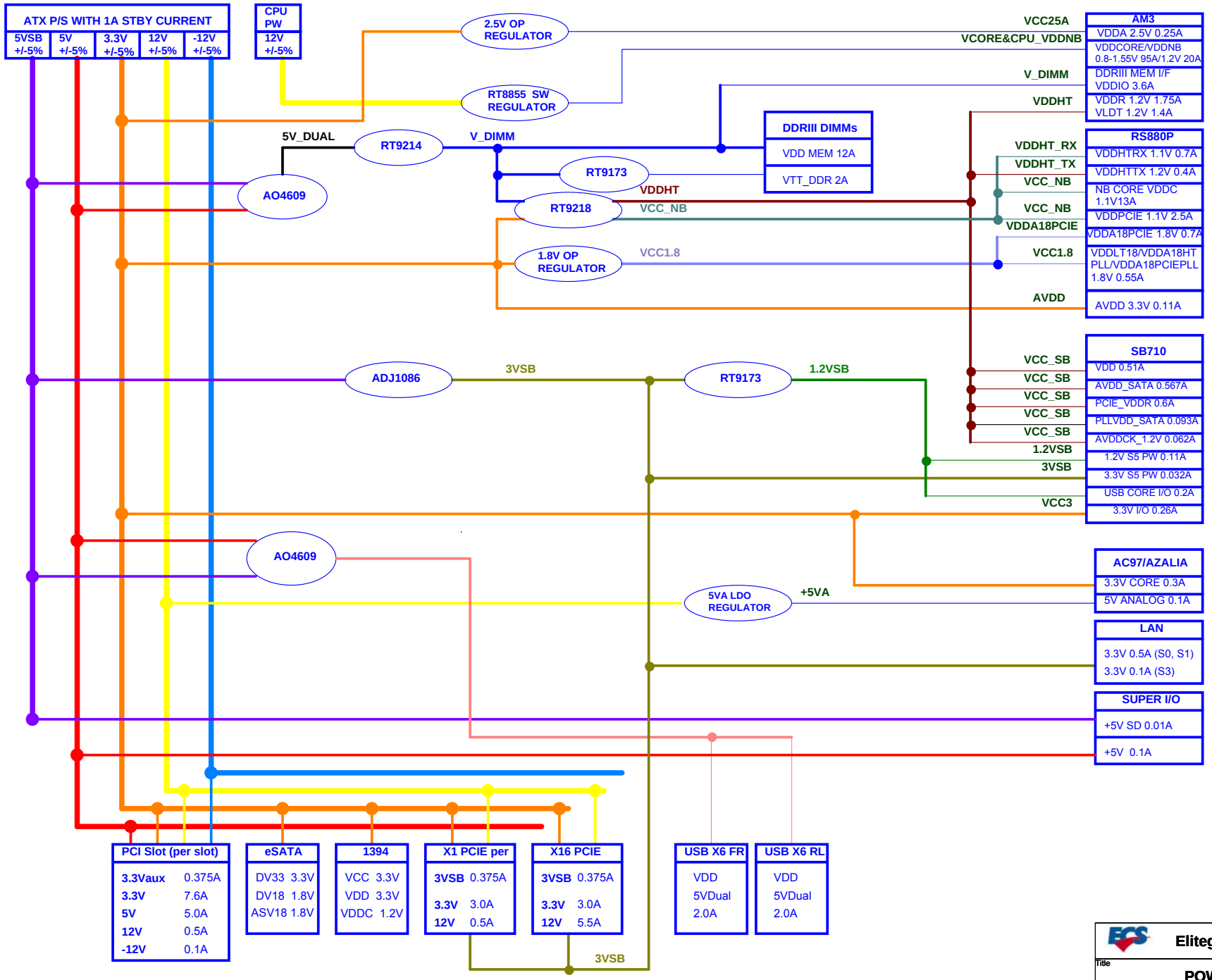

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Title: POWER DELIVERY CHART

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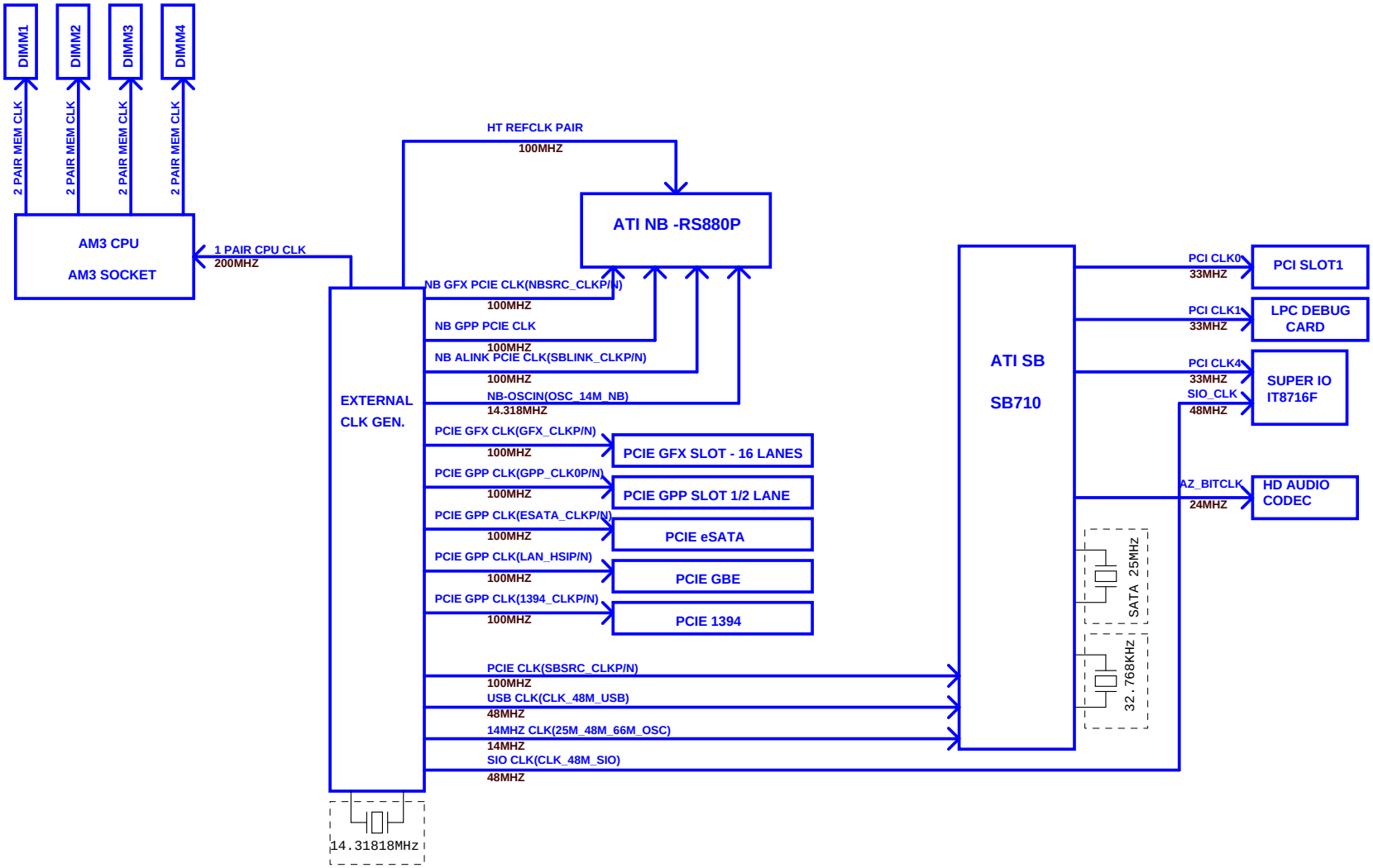

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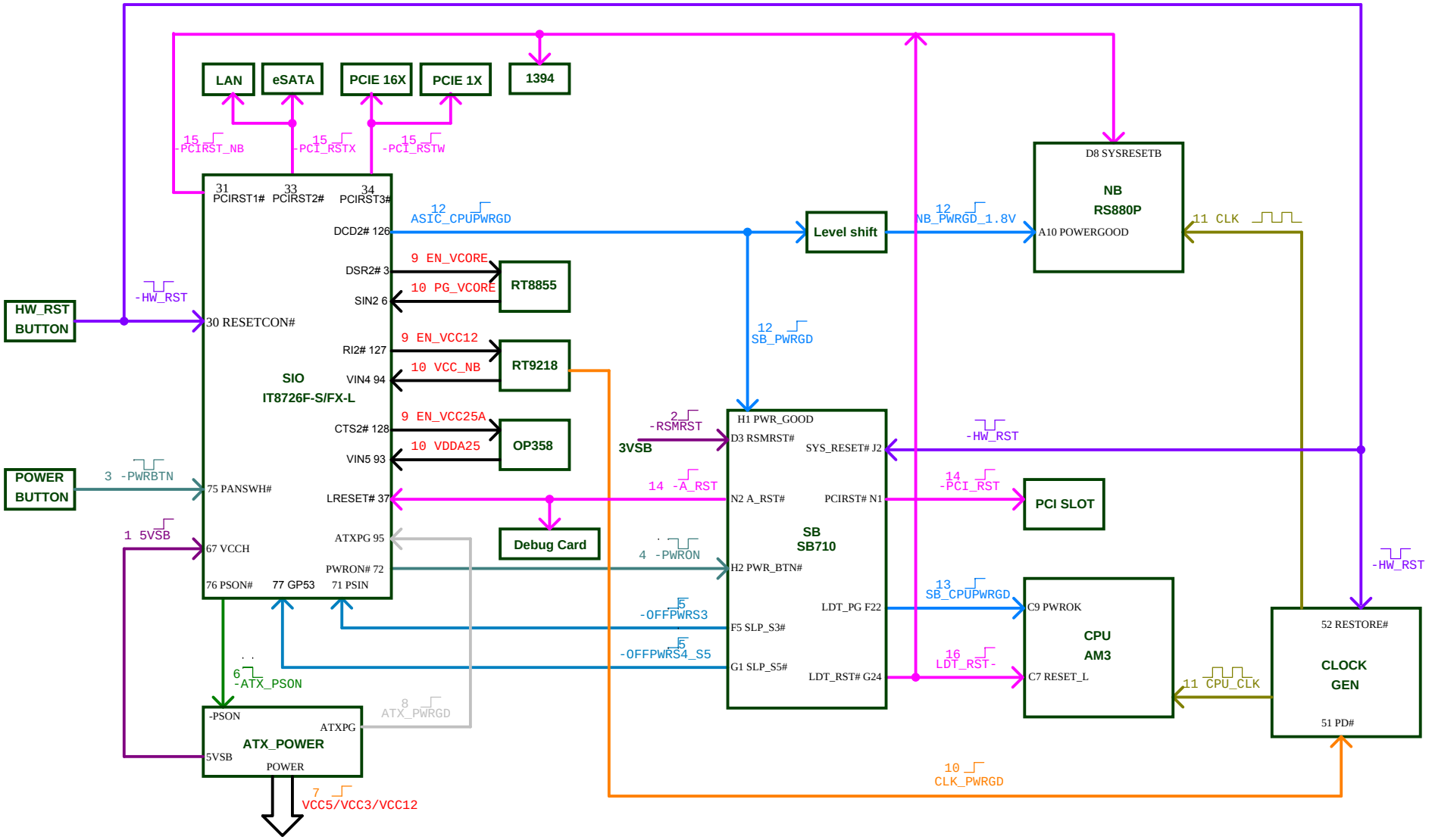
Power Sequence



Elitegroup Computer Systems		
Title: Power Sequence		
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