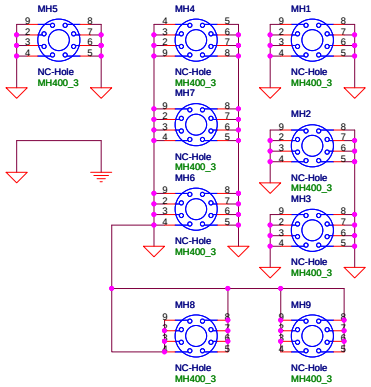
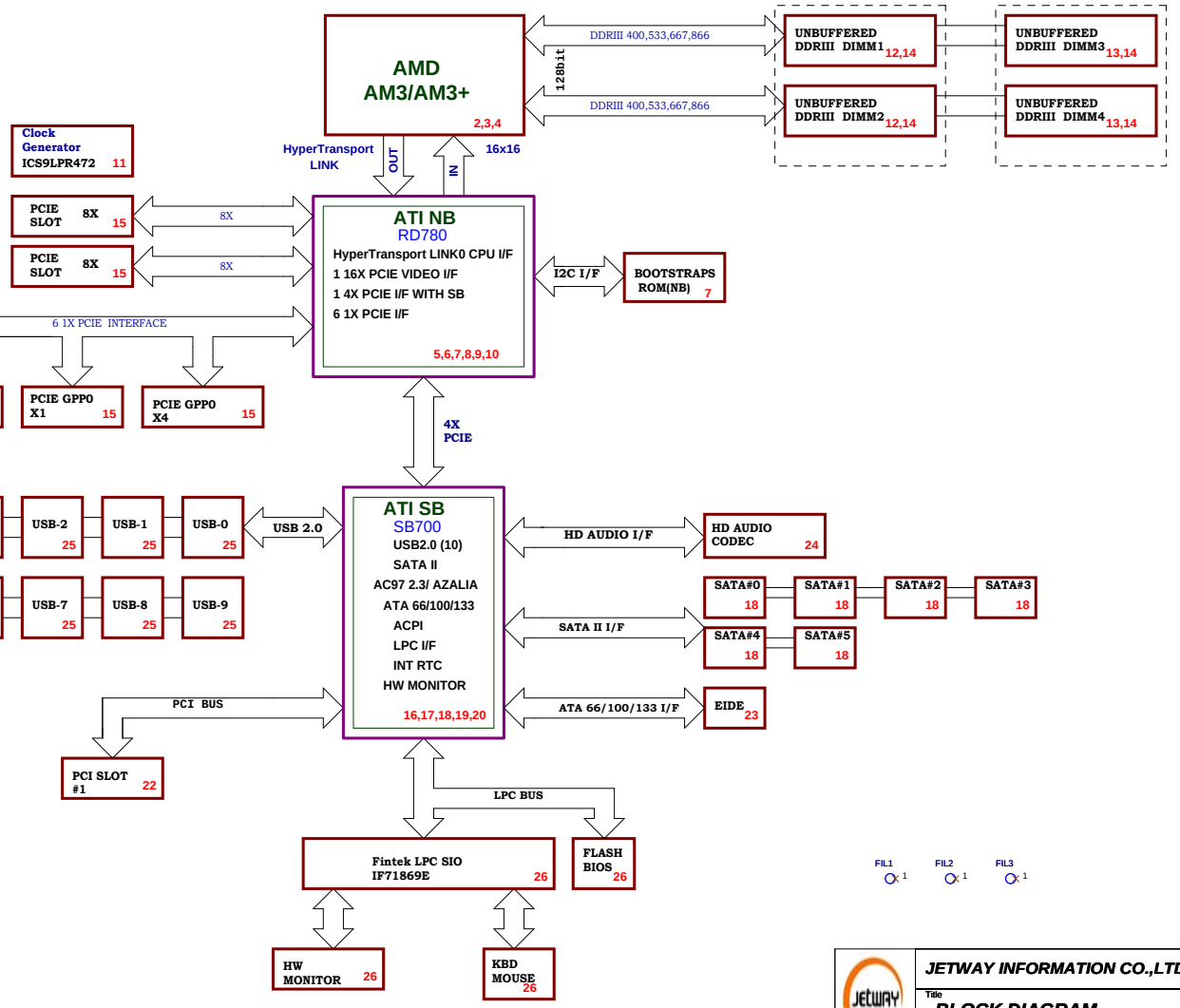
Jetway Information Co. Ltd.

RD780 CUSTOMER DESKTOP REFERENCE DESIGN





FIL1 FIL2 FIL3

JETWAY INFORMATION CO.,LTD.		
Title: BLOCK DIAGRAM		
Size: E	Document Number: HA18	Rev: 1.0
Date: Tuesday, June 21, 2011	Sheet 1 of 26	

ATHLON Control and Debug

+2.5VDDA

LAYOUT: Route 50 mils wide and 500~750 mils long

LAYOUT: Route VDDA trace approx. 50 mils wide (use 2x25 mil traces to exit ball field) and 500 mils long.

Keep trace to resistor less than 600mils from CPU pin and trace to AC caps less than 1250mils

LAYOUT: PLACE 169 OHM WITHIN 0.5INCH OF CPU

ROUTE AS DIF 5/5/5/20

LAYOUT: ROUTE 80 OHM DIFF IMPEDENCE
LAYOUT: PLACE WITHIN 0.5 INCH OF CPU

CPU_PRSNT* TERM VOLTAGE CAN BE ANY VOLTAGE

Erratum 133, Revision Guide for AMD NPT 0Fh Processors(TEST21,26)

AOD function

CPU1B <PCB Footprint> SOCKET_940_M2 SEC 2 OF 6

CPU1F <PCB Footprint> SOCKET_940_M2 SEC 6 OF 6

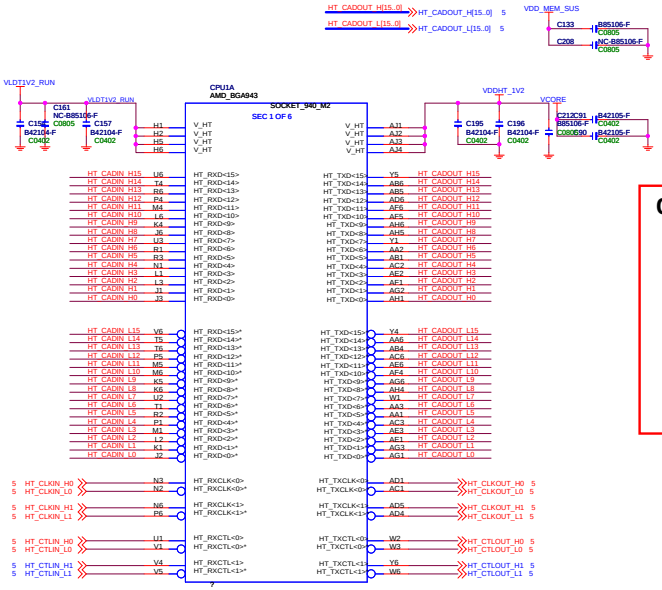
M2 Top View

Company	JETWAY INFORMATION CO.,LTD.
Title	CPU CTRL&DEBUG
Size / Document Number	HA18
Rev	1.0
Date: Tuesday, June 21, 2011	Sheet 2 of 26

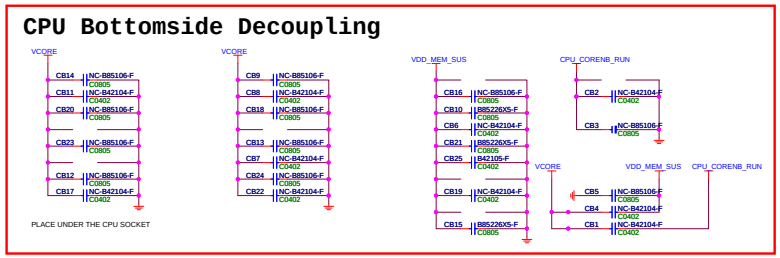
Processor Power and Ground

Processor HyperTransport Interface

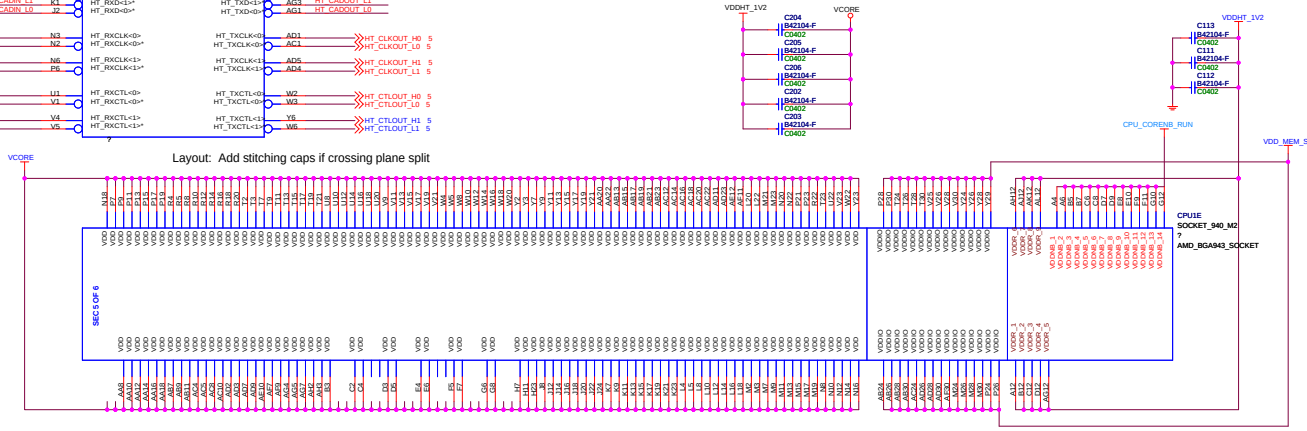
VDDLDTRUNCPU is connected to the VDD_LDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



CPU Bottomside Decoupling

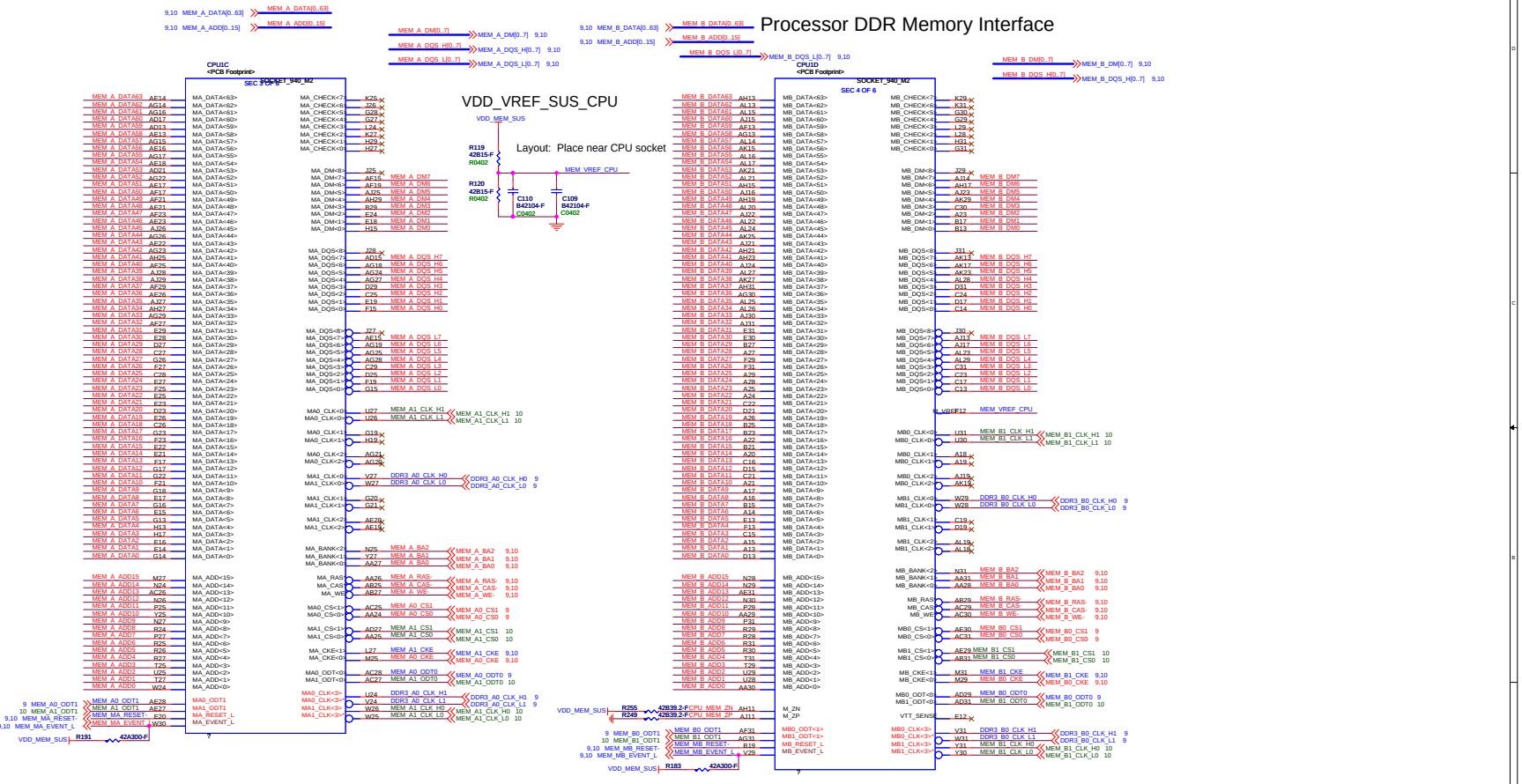


Layout: Add stitching caps if crossing plane split



JETWAY INFORMATION CO.,LTD.			
Title: CPU HT I/F & POWER			
Size: Custom	Document Number: HA18		Rev: 1.0
Date: Tuesday, June 21, 2011		Sheet 3 of 26	

Processor DDR Memory Interface



JETWAY INFORMATION CO.,LTD.			
Title: CPU DDR2MEMORY			
Size: Custom	Document Number: HA18		Rev: 1.0
Date: Tuesday, June 21, 2011		Sheet 4 of 26	

3 HT_CADIN_H[15..0] → HT_CADIN_H[15..0]

3 HT_CADIN_L[15..0] → HT_CADIN_L[15..0]

HT_CADOUT_H[15..0] → HT_CADOUT_H[15..0] 3

HT_CADOUT_L[15..0] → HT_CADOUT_L[15..0] 3

U22A

PART 1/5

HYPERTRANSPORT IF

HT_CADOUT_H15	T25	HT_RXCAD15P	HT_TXCAD15P	N23	HT_CADIN_H15
HT_CADOUT_L15	T24	HT_RXCAD15N	HT_TXCAD15N	N24	HT_CADIN_L15
HT_CADOUT_H14	U24	HT_RXCAD14P	HT_TXCAD14P	M24	HT_CADIN_H14
HT_CADOUT_L14	U23	HT_RXCAD14N	HT_TXCAD14N	M25	HT_CADIN_L14
HT_CADOUT_H13	V25	HT_RXCAD13P	HT_TXCAD13P	L23	HT_CADIN_H13
HT_CADOUT_L13	V24	HT_RXCAD13N	HT_TXCAD13N	L24	HT_CADIN_L13
HT_CADOUT_H12	W24	HT_RXCAD12P	HT_TXCAD12P	K24	HT_CADIN_H12
HT_CADOUT_L12	W23	HT_RXCAD12N	HT_TXCAD12N	K25	HT_CADIN_L12
HT_CADOUT_H11	AA24	HT_RXCAD11P	HT_TXCAD11P	H24	HT_CADIN_H11
HT_CADOUT_L11	AA23	HT_RXCAD11N	HT_TXCAD11N	H25	HT_CADIN_L11
HT_CADOUT_H10	AB25	HT_RXCAD10P	HT_TXCAD10P	G23	HT_CADIN_H10
HT_CADOUT_L10	AB24	HT_RXCAD10N	HT_TXCAD10N	G24	HT_CADIN_L10
HT_CADOUT_H9	AC24	HT_RXCAD9P	HT_TXCAD9P	F24	HT_CADIN_H9
HT_CADOUT_L9	AC23	HT_RXCAD9N	HT_TXCAD9N	F25	HT_CADIN_L9
HT_CADOUT_H8	AD25	HT_RXCAD8P	HT_TXCAD8P	E23	HT_CADIN_H8
HT_CADOUT_L8	AD24	HT_RXCAD8N	HT_TXCAD8N	E24	HT_CADIN_L8
HT_CADOUT_H7	T28	HT_RXCAD7P	HT_TXCAD7P	N26	HT_CADIN_H7
HT_CADOUT_L7	T27	HT_RXCAD7N	HT_TXCAD7N	N27	HT_CADIN_L7
HT_CADOUT_H6	U27	HT_RXCAD6P	HT_TXCAD6P	M27	HT_CADIN_H6
HT_CADOUT_L6	U26	HT_RXCAD6N	HT_TXCAD6N	M28	HT_CADIN_L6
HT_CADOUT_H5	V29	HT_RXCAD5P	HT_TXCAD5P	L26	HT_CADIN_H5
HT_CADOUT_L5	V27	HT_RXCAD5N	HT_TXCAD5N	L27	HT_CADIN_L5
HT_CADOUT_H4	W27	HT_RXCAD4P	HT_TXCAD4P	K27	HT_CADIN_H4
HT_CADOUT_L4	W26	HT_RXCAD4N	HT_TXCAD4N	K28	HT_CADIN_L4
HT_CADOUT_H3	AA27	HT_RXCAD3P	HT_TXCAD3P	H27	HT_CADIN_H3
HT_CADOUT_L3	AA26	HT_RXCAD3N	HT_TXCAD3N	H28	HT_CADIN_L3
HT_CADOUT_H2	AB28	HT_RXCAD2P	HT_TXCAD2P	G26	HT_CADIN_H2
HT_CADOUT_L2	AB27	HT_RXCAD2N	HT_TXCAD2N	G27	HT_CADIN_L2
HT_CADOUT_H1	AC27	HT_RXCAD1P	HT_TXCAD1P	F27	HT_CADIN_H1
HT_CADOUT_L1	AC26	HT_RXCAD1N	HT_TXCAD1N	F28	HT_CADIN_L1
HT_CADOUT_H0	AD28	HT_RXCAD0P	HT_TXCAD0P	E26	HT_CADIN_H0
HT_CADOUT_L0	AD27	HT_RXCAD0N	HT_TXCAD0N	E27	HT_CADIN_L0
HT_CLKOUT_H1	Y25	HT_RXCLK1P	HT_TXCLK1P	J23	HT_CLKIN_H1
HT_CLKOUT_L1	Y24	HT_RXCLK1N	HT_TXCLK1N	J24	HT_CLKIN_L1
HT_CLKOUT_H0	Y28	HT_RXCLK0P	HT_TXCLK0P	J26	HT_CLKIN_H0
HT_CLKOUT_L0	Y27	HT_RXCLK0N	HT_TXCLK0N	J27	HT_CLKIN_L0
HT_CTLOUT_H1	R24	HT_RXCTL1P	HT_TXCTL1P	P24	HT_CTLIN_H1
HT_CTLOUT_L1	R23	HT_RXCTL1N	HT_TXCTL1N	P25	HT_CTLIN_L1
HT_CTLOUT_H0	R27	HT_RXCTL0P	HT_TXCTL0P	P27	HT_CTLIN_H0
HT_CTLOUT_L0	R26	HT_RXCTL0N	HT_TXCTL0N	P28	HT_CTLIN_L0
R289 42B1 21K-F HT_RXCALP	D25	HT_RXCALP	HT_TXCALP	D28	HT_TXCALP R293 42B1 4K-F
R0402 HT_RXCALN	D24	HT_RXCALN	HT_TXCALN	D27	HT_TXCALN R0402

AMD980-F

M1 MARK X-BGA0505016-FHS1

M2 MARK X-BGA0505016-F

M3 MARK X-BGA0505016-F

M4 MARK X-BGA0505016-F

HA10-Y-F HEATSINKL405W375H150M

3 HT_CLKOUT_H0
3 HT_CLKOUT_L0
3 HT_CLKOUT_H1
3 HT_CLKOUT_L1

3 HT_CTLOUT_H0
3 HT_CTLOUT_L0
3 HT_CTLOUT_H1
3 HT_CTLOUT_L1

3 HT_CLKIN_H0
3 HT_CLKIN_L0
3 HT_CLKIN_H1
3 HT_CLKIN_L1

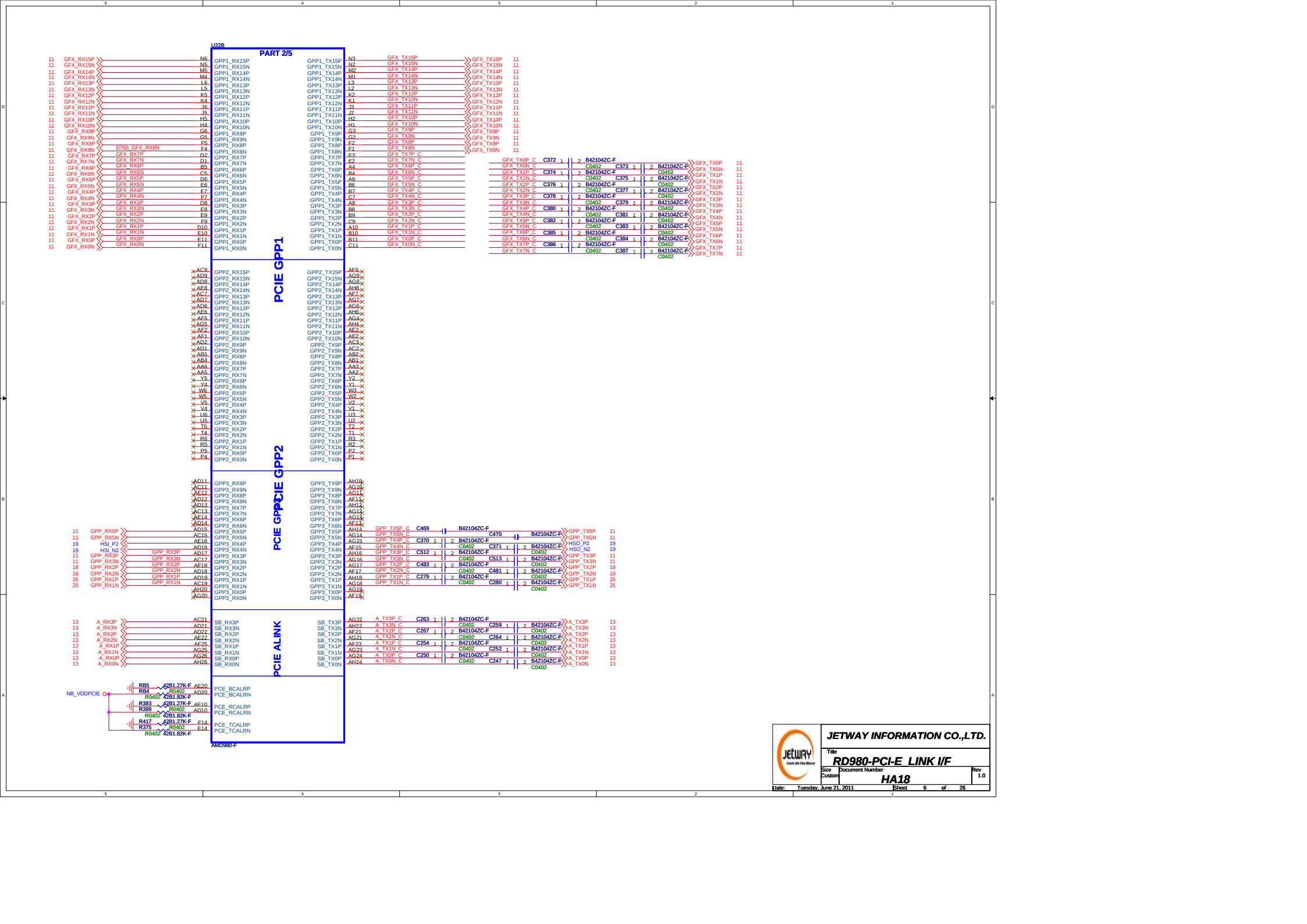
3 HT_CTLIN_H0
3 HT_CTLIN_L0
3 HT_CTLIN_H1
3 HT_CTLIN_L1

JETWAY INFORMATION CO.,LTD.

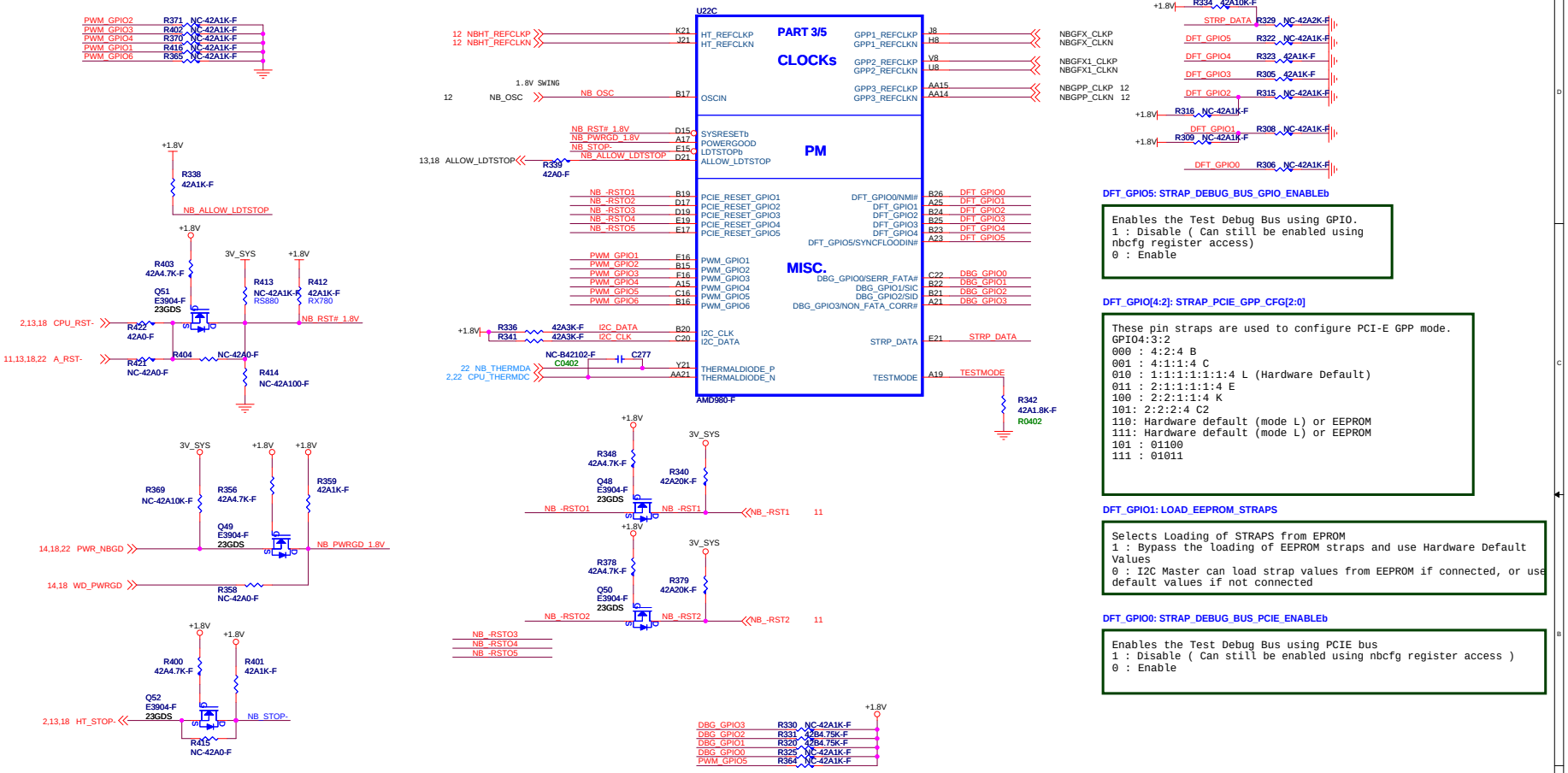
Title: RD980-HT3 LINK I/F

Size: Custom | Document Number: HA18 | Rev: 1.0

Date: Tuesday, June 21, 2011 | Sheet 5 of 26



JETWAY INFORMATION CO.,LTD.	
Title: RD980-PCI-E_LINK I/F	
Size: Custom	Document Number: HA18
Rev: 1.0	
Date: Tuesday, June 21, 2011	Sheet 6 of 26



DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

```
Enables the Test Debug Bus using GPIO.
1 : Disable ( Can still be enabled using
nbcfg register access)
0 : Enable
```

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

```
These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101: 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011
```

DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default
Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
```

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

```
Enables the Test Debug Bus using PCIE bus
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable
```

RX740/RS740/RS780 difference table (Control signal)

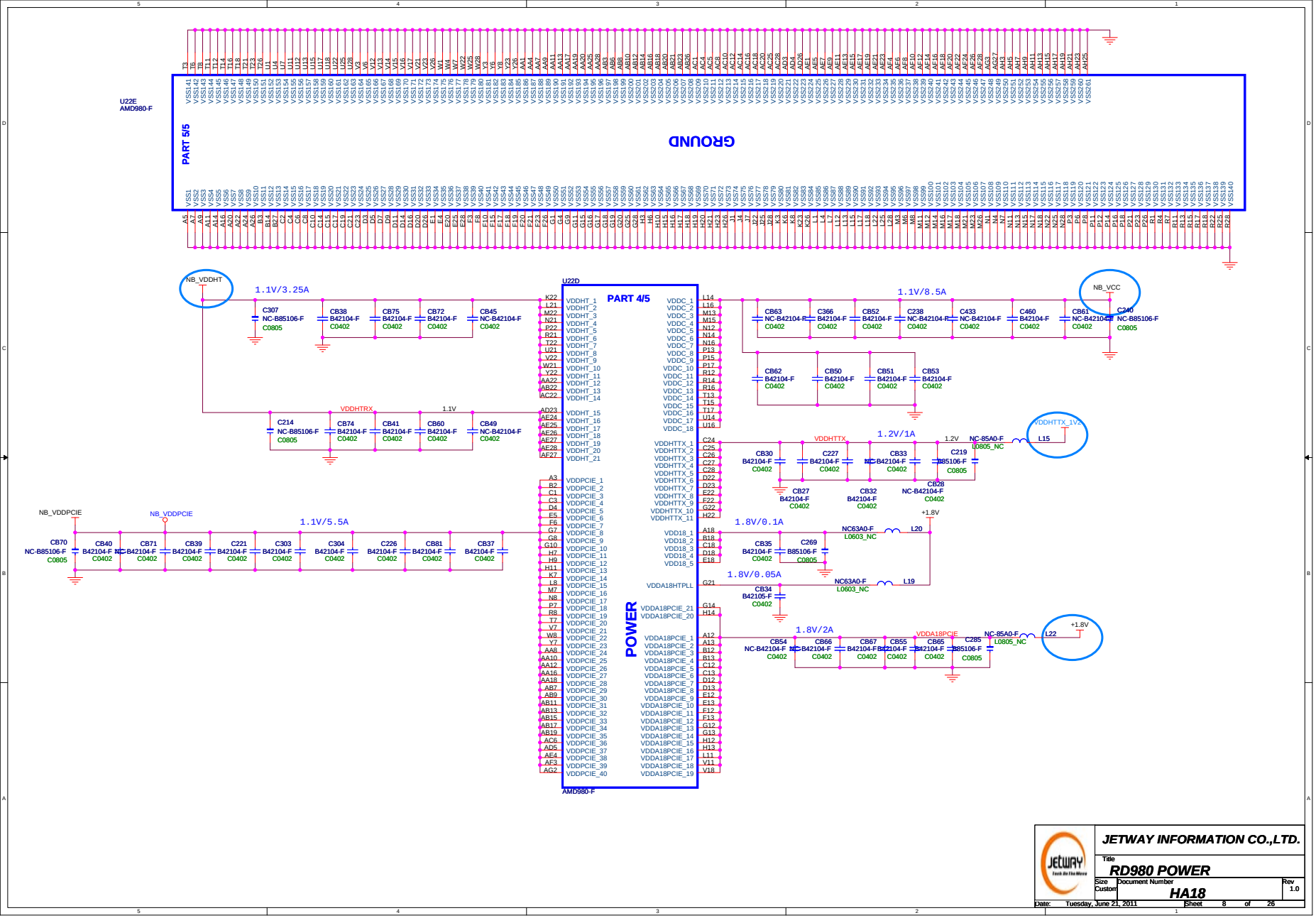
	RS740	RX780	RS780	RS880
NB_PWRGD IN	3.3V IN	1.8V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OD	OD	OD/3.3V IN	3.3V IN
LDT_STOP# IN(default)/OUT	3.3V IN	1.8V IN	3.3V IN/OD	1.8V IN
SYSTEMRESETb IN	3.3V IN	1.8V IN	3.3V IN	3.3V IN

JETWAY INFORMATION CO.,LTD.

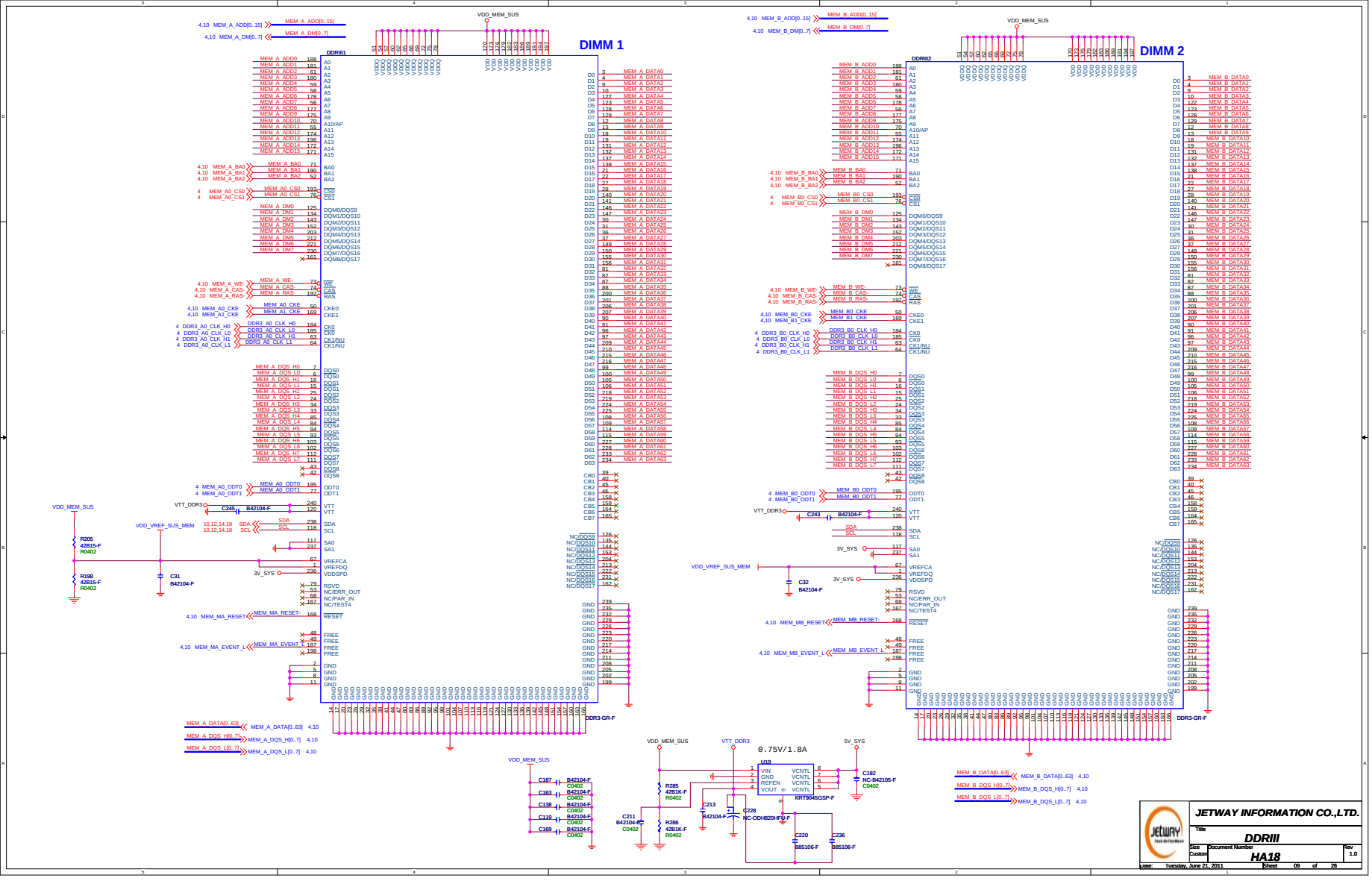
Title: RD980-SYSTEM I/F & STRAP

Size: Custom | Document Number: HA18 | Rev: 1.0

Date: Tuesday, June 21, 2011 | Sheet 7 of 26



JETWAY INFORMATION CO.,LTD.	
Title: RD980 POWER	
Size: Custom	Document Number: HA18
Rev: 1.0	
Date: Tuesday, June 21, 2011	Sheet 8 of 26


DIMM 1
DIMM 2
DDRIII1
DDRIII2
VDD_MEM_SUS
VTT_DDR3
VDD_VREF_SUS_MEM
3V_SYS
5V_SYS
0.75V/1.8A
DDR3-GR-F
KRT9045GSP-F
JETWAY INFORMATION CO.,LTD.
DDRIII
HA18
Tuesday, June 21, 2011
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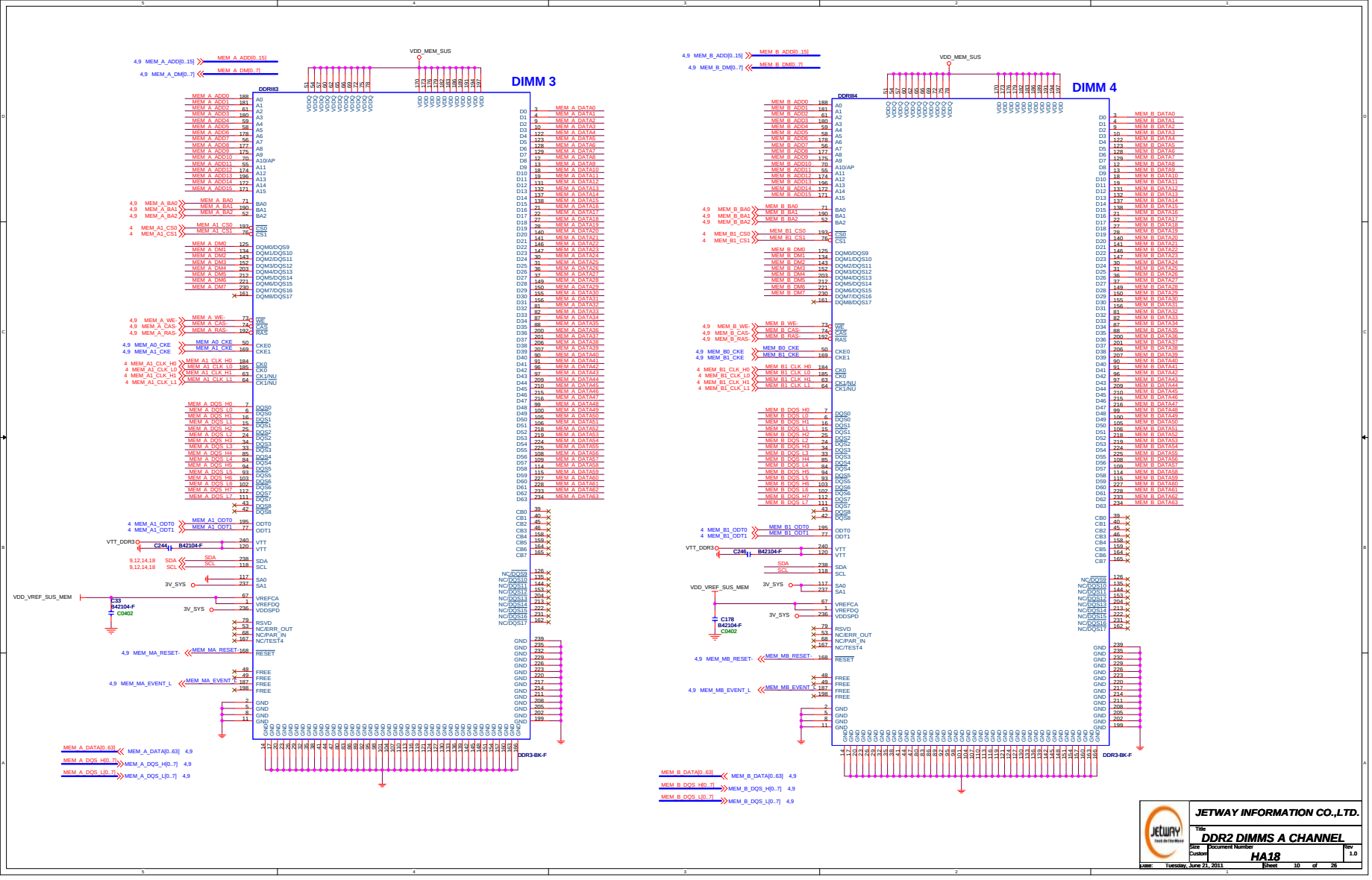

JETWAY INFORMATION CO.,LTD.

Title: DDR2 DIMMS A CHANNEL

Size: Custom | Document Number: HA18 | Rev: 1.0

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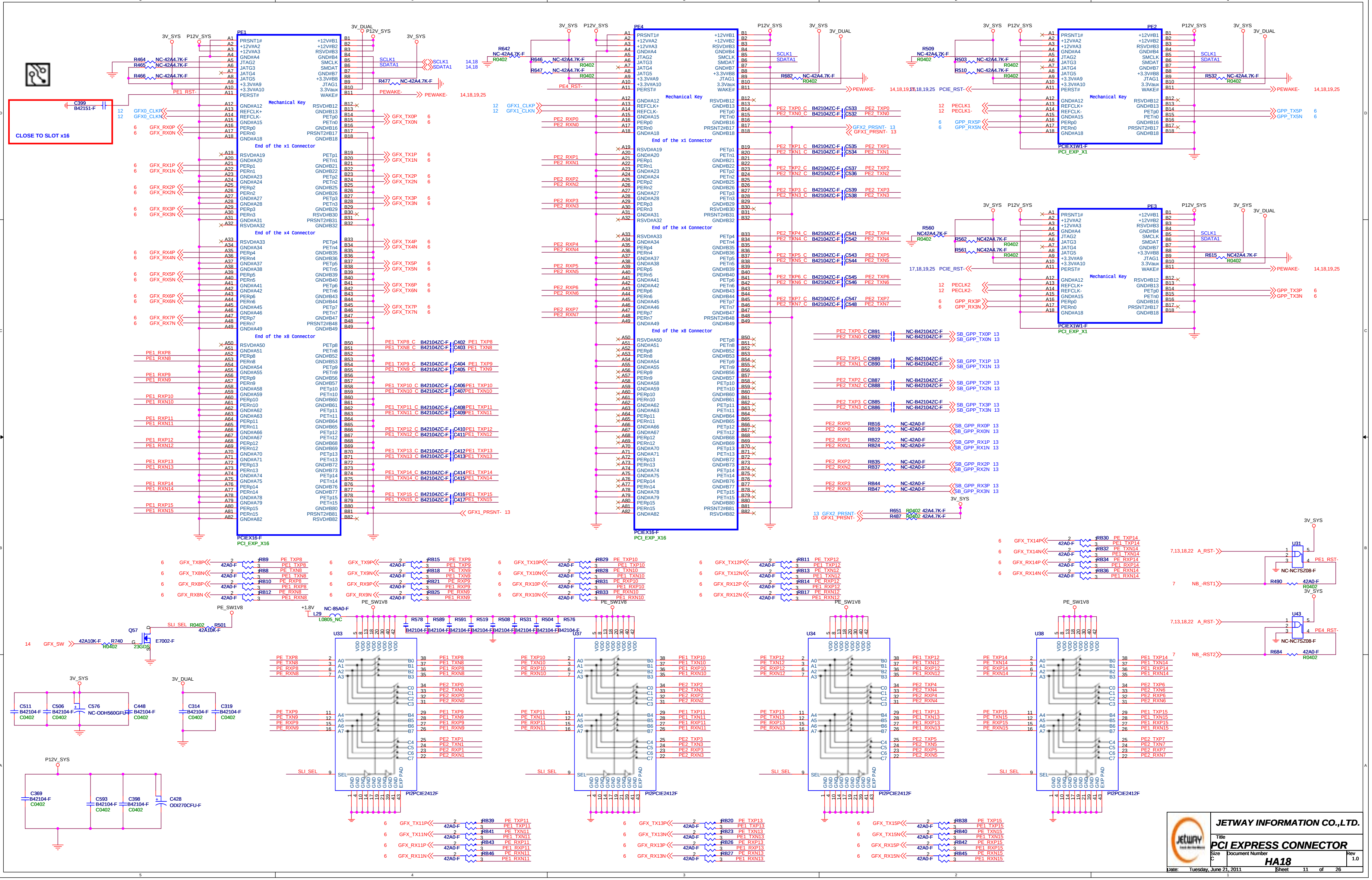
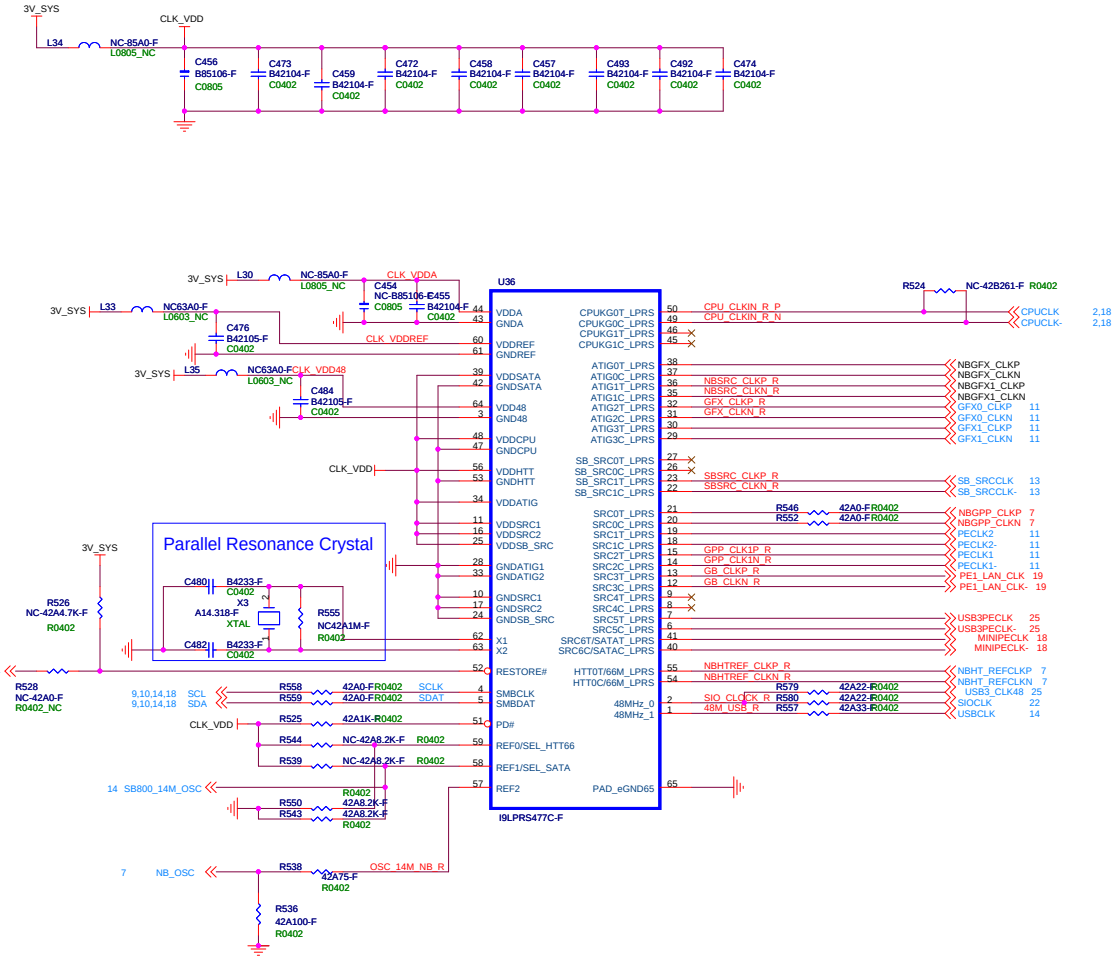
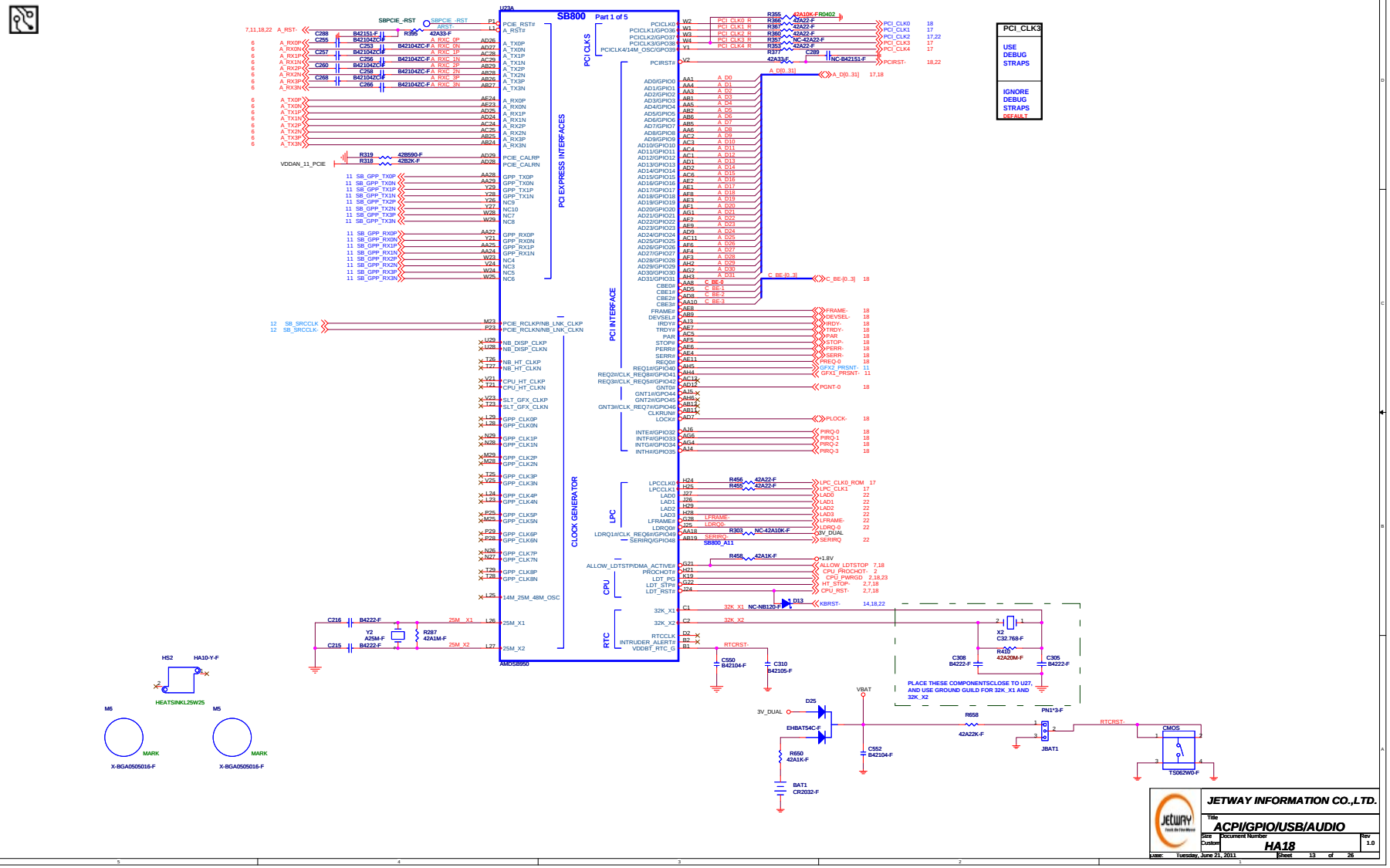
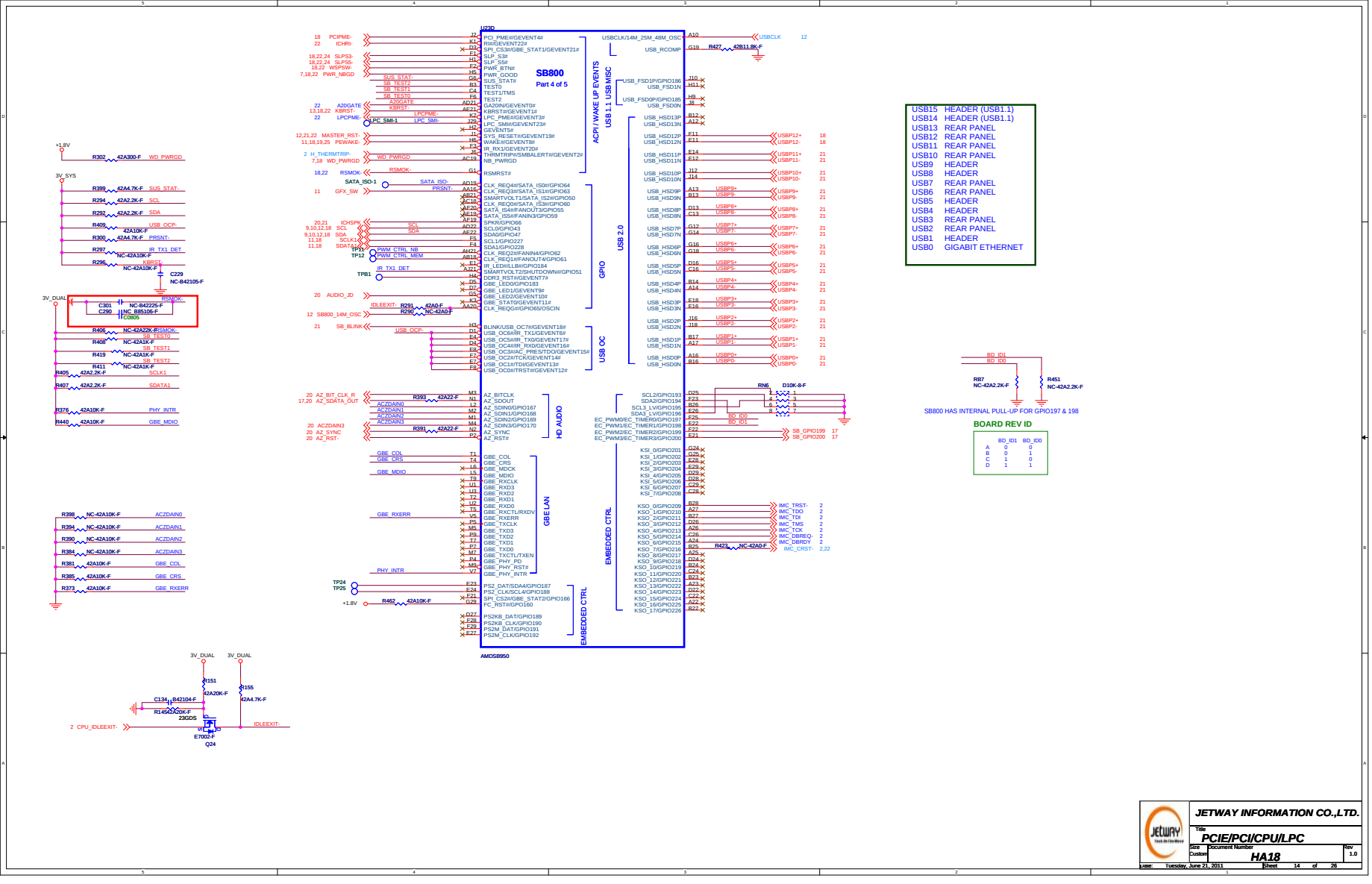

CLOSE TO SLOT x16
Mechanical Key
End of the x1 Connector
End of the x4 Connector
End of the x8 Connector
PCIEX16-F
PCI_EXP_X16
PCIE X1W1-F
PCI_EXP_X1
PI2PCIE2412F
JETWAY INFORMATION CO.,LTD.
Title
PCI EXPRESS CONNECTOR
Size
C
Document Number
HA18
Rev
1.0
Date: Tuesday, June 21, 2011
Sheet 11 of 26



JETWAY INFORMATION CO.,LTD.		
Title: RX780 EXTERNAL CLOCK GENERATOR		
Size: Custom	Document Number: HA18	Rev: 1.0
Date: Tuesday, June 21, 2011	Sheet 12 of 26	


SB800
Part 1 of 5
U23A
AMDSB950
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
PCI_CLK3
USE DEBUG STRAPS
IGNORE DEBUG STRAPS DEFAULT
PLACE THESE COMPONENTSCLOSE TO U27, AND USE GROUND GUILD FOR 32K_X1 AND 32K_X2
HEATSINKL25W25
X-BGA0505016-F
TS062WG-F
JBAT1
BAT1 CR2032-F
EHBAT54C-F
JETWAY INFORMATION CO.,LTD.
ACPI/GPIO/USB/AUDIO
HA18
Tuesday, June 21, 2011
Sheet 13 of 26


U23D
SB800
Part 4 of 5
AMDSB950
ACPI / WAKE UP EVENTS
USB1.1 USB MISC
USB 2.0
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
USB15 HEADER (USB1.1)
USB14 HEADER (USB1.1)
USB13 REAR PANEL
USB12 REAR PANEL
USB11 REAR PANEL
USB10 REAR PANEL
USB9 HEADER
USB8 HEADER
USB7 REAR PANEL
USB6 REAR PANEL
USB5 HEADER
USB4 HEADER
USB3 REAR PANEL
USB2 REAR PANEL
USB1 HEADER
USB0 GIGABIT ETHERNET
SB800 HAS INTERNAL PULL-UP FOR GPIO197 & 198
BOARD REV ID
BD_ID1 BD_ID0
A 0 0
B 0 1
C 1 0
D 1 1
JETWAY INFORMATION CO.,LTD.
PCIE/PCI/CPU/LPC
HA18
Tuesday, June 21, 2011
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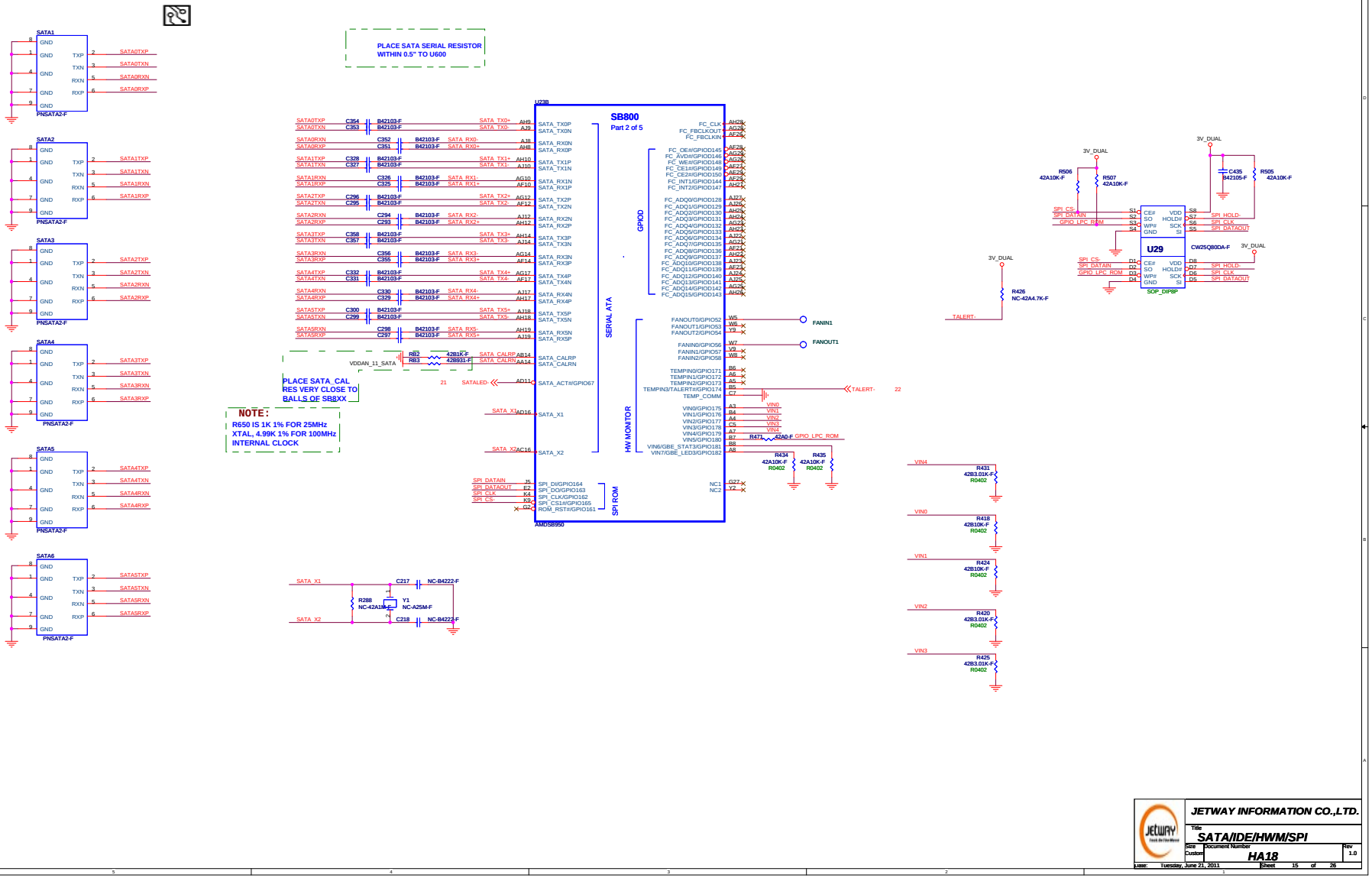

SATA1
SATA2
SATA3
SATA4
SATA5
SATA6
PNSATA2-F
PLACE SATA SERIAL RESISTOR WITHIN 0.5" TO U600
U23B
SB800
Part 2 of 5
AMDSB950
SERIAL ATA
GPIOD
HW MONITOR
SPI ROM
PLACE SATA_CAL RES VERY CLOSE TO BALLS OF SB8XX
NOTE:
R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK
FANIN1
FANOUT1
TALERT-
GPIO_LPC_ROM
3V_DUAL
U29
CW25Q80DA-F
SOP_DIP8P
JETWAY INFORMATION CO.,LTD.
SATA/IDE/HWM/SPI
HA18
Tuesday, June 21, 2011
Sheet 15 of 26

PUT ELT TEST POINTS CLOSE TO SERIES RESISTOR

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

U23C — SB800 — Part 3 of 5 — POWER

U23E — SB800 — Part 5 of 5 — GROUND

AMDSB950

TIE PIN D8 AND C7 TOGETHER THEN TO A DEDICATED GND VIA

VDDPL_33_USB_S and VDDAN-33_USB_S [12:1] can be tied together and share one ferrite bead

VDDAN_11_USB_S [2:1] and VDDCR_11_USB_S [2:1] can be tied together and share one ferrite bead

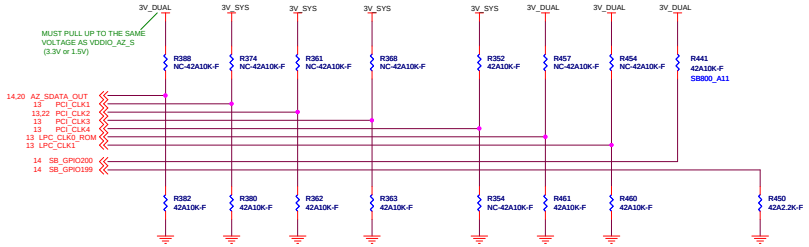
Co-Lay Capacitor 3pcs

JETWAY INFORMATION CO.,LTD.	
Title: POWER / DECOUPLING	
Size: Custom	Document Number: HA18
Rev: 1.0	
Date: Tuesday, June 21, 2011	Sheet 16 of 26

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

PLACE STRAP RESISTORS DIRECTLY ON CLK NETS (WITHOUT STUBS).

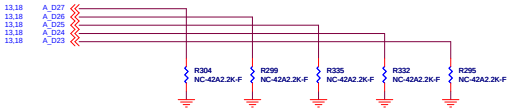
SB800 REQUIRED STRAPS



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	NON-FUSION CPU CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	FUSION CPU CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM

SB800 DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[30:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

JETWAY INFORMATION CO.,LTD.

Title: STRAPS

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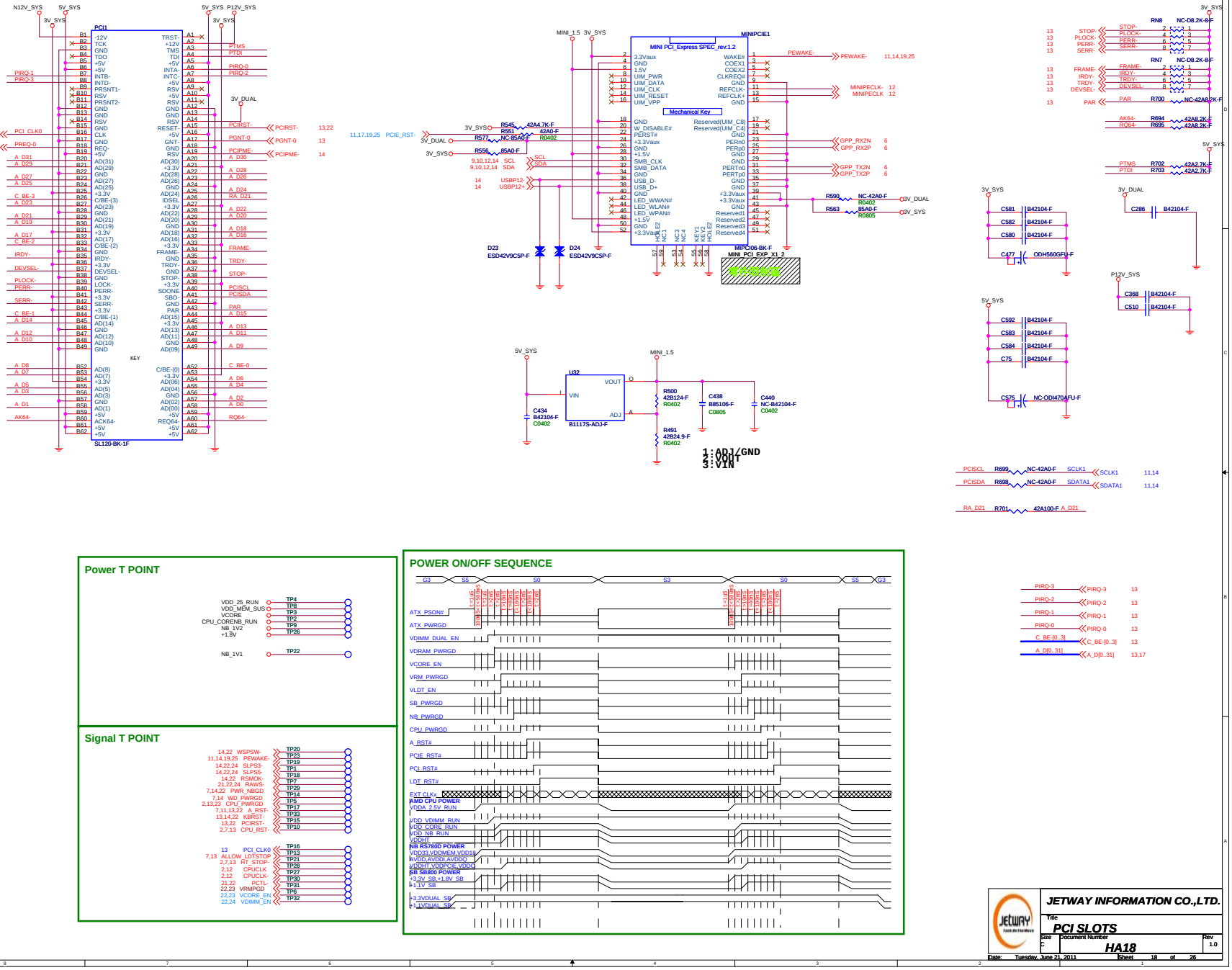
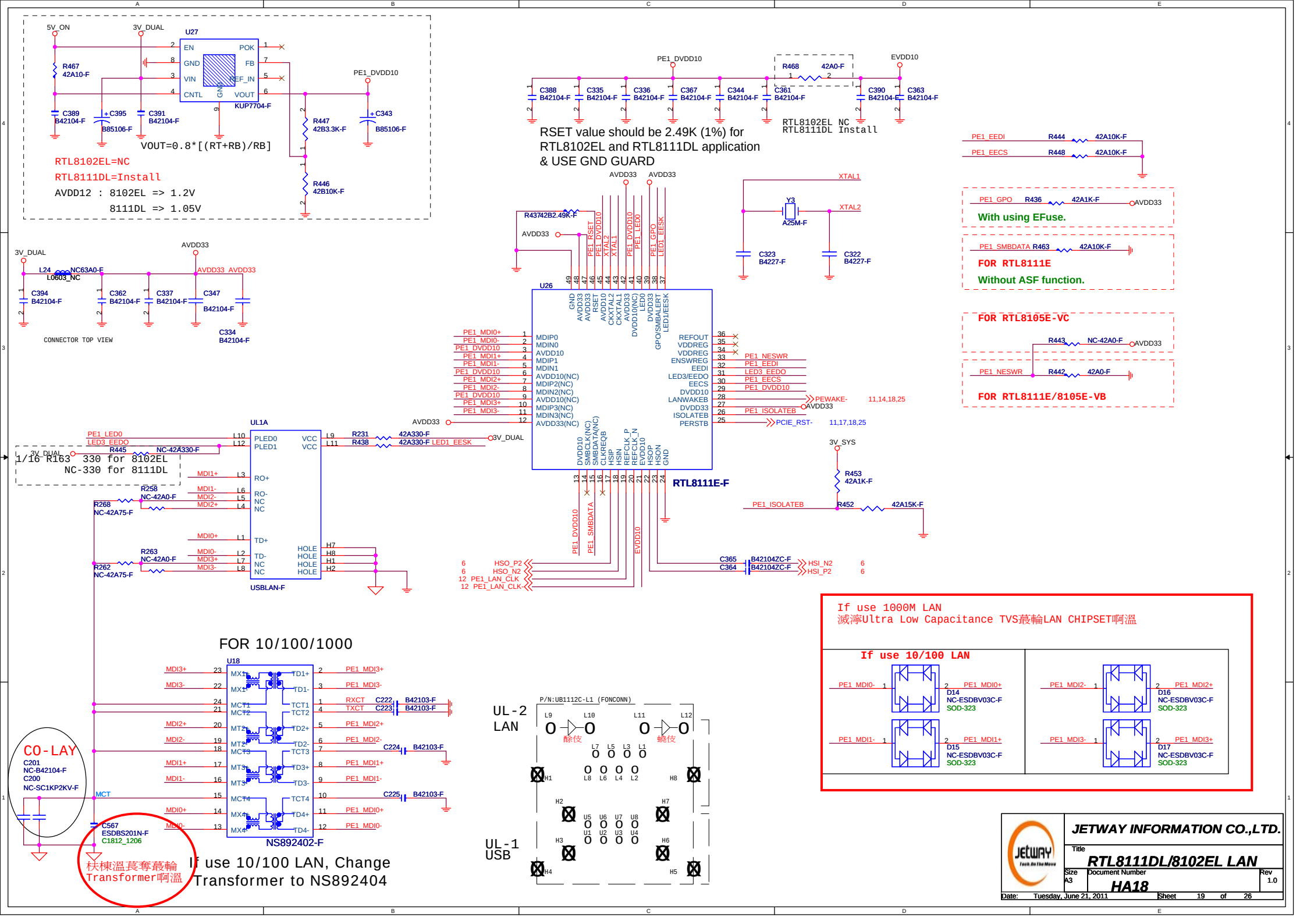

PCI1
SL120-BK-1F
MINIPCIE1
MINI PCI_Express SPEC_rev1.2
Mechanical Key
MIPCI06-BK-F
MINI PCI_EXP_X1_2
U32
B1117S-ADJ-F
1:ADJ/GND
2:VOUT
3:VIN
Power T POINT
Signal T POINT
POWER ON/OFF SEQUENCE
JETWAY INFORMATION CO.,LTD.
PCI SLOTS
HA18


5V_ON
3V_DUAL
U27
EN
GND
VIN
CNTL
POK
FB
REF_IN
VOUT
KUP7704-F
R467
42A10-F
C389
B42104-F
C395
B85106-F
C391
B42104-F
PE1_DVDD10
C343
B85106-F
R447
42B3.3K-F
R446
42B10K-F
VOUT=0.8*[(RT+RB)/RB]
RTL8102EL=NC
RTL8111DL=Install
AVDD12 : 8102EL => 1.2V
8111DL => 1.05V
PE1_DVDD10
C388 B42104-F
C335 B42104-F
C336 B42104-F
C367 B42104-F
C344 B42104-F
C361 B42104-F
R468 42A0-F
EVDD10
C390 B42104-F
C363 B42104-F
RTL8102EL NC
RTL8111DL Install
RSET value should be 2.49K (1%) for
RTL8102EL and RTL8111DL application
& USE GND GUARD
PE1_EEDI R444 42A10K-F
PE1_EECS R448 42A10K-F
PE1_GPO R436 42A1K-F AVDD33
With using EFuse.
PE1_SMBDATA R463 42A10K-F
FOR RTL8111E
Without ASF function.
FOR RTL8105E-VC
R443 NC-42A0-F AVDD33
PE1_NESWR R442 42A0-F
FOR RTL8111E/8105E-VB
3V_DUAL
AVDD33
L24 NC63A0-F
L0603_NC
C394 B42104-F
C362 B42104-F
C337 B42104-F
C347 B42104-F
C334 B42104-F
CONNECTOR TOP VIEW
R43742B2.49K-F
AVDD33
XTAL1
XTAL2
Y3
A25M-F
C323 B4227-F
C322 B4227-F
U26
RTL8111E-F
MDIP0
MDIN0
AVDD10
MDIP1
MDIN1
AVDD10(NC)
MDIP2(NC)
MDIN2(NC)
AVDD10(NC)
MDIP3(NC)
MDIN3(NC)
AVDD33(NC)
REFOUT
VDDREG
VDDREG
ENSWREG
EEDI
LED3/EEDO
EECS
DVDD10
LANWAKEB
DVDD33
ISOLATEB
PERSTB
PEWAKE-
PCIE_RST-
11,14,18,25
3V_SYS
R453 42A1K-F
R452 42A15K-F
PE1_ISOLATEB
C365 B42104ZC-F
C364 B42104ZC-F
HSI_N2
HSI_P2
HSO_P2
HSO_N2
PE1_LAN_CLK
UL1A
USBLAN-F
PLED0
PLED1
VCC
RO+
RO-
NC
TD+
TD-
HOLE
R231 42A330-F
R438 42A330-F LED1_EESK
R445 NC-42A330-F
1/16 R163 330 for 8102EL
NC-330 for 8111DL
R258 NC-42A0-F
R268 NC-42A75-F
R263 NC-42A0-F
R262 NC-42A75-F
FOR 10/100/1000
U18
NS892402-F
MX1+
MX1-
MX2+
MX2-
MX3+
MX3-
MX4+
MX4-
MCT1
MCT2
MCT3
MCT4
TD1+
TD1-
TD2+
TD2-
TD3+
TD3-
TD4+
TD4-
RXCT C222 B42103-F
TXCT C223 B42103-F
C224 B42103-F
C225 B42103-F
CO-LAY
C201
NC-B42104-F
C200
NC-SC1KP2KV-F
C567
ESDBS201N-F
C1812_1206
扶棟溫蔑奪蕞輪
Transformer啊溫
If use 10/100 LAN, Change
Transformer to NS892404
UL-2
LAN
UL-1
USB
P/N:UB1112C-L1 (FONCONN)
餘伎
蟯伎
If use 1000M LAN
滅濘Ultra Low Capacitance TVS蕞輪LAN CHIPSET啊溫
If use 10/100 LAN
D14 NC-ESDBV03C-F SOD-323
D15 NC-ESDBV03C-F SOD-323
D16 NC-ESDBV03C-F SOD-323
D17 NC-ESDBV03C-F SOD-323
JETWAY INFORMATION CO.,LTD.
Title
RTL8111DL/8102EL LAN
Size A3
Document Number HA18
Rev 1.0
Date: Tuesday, June 21, 2011
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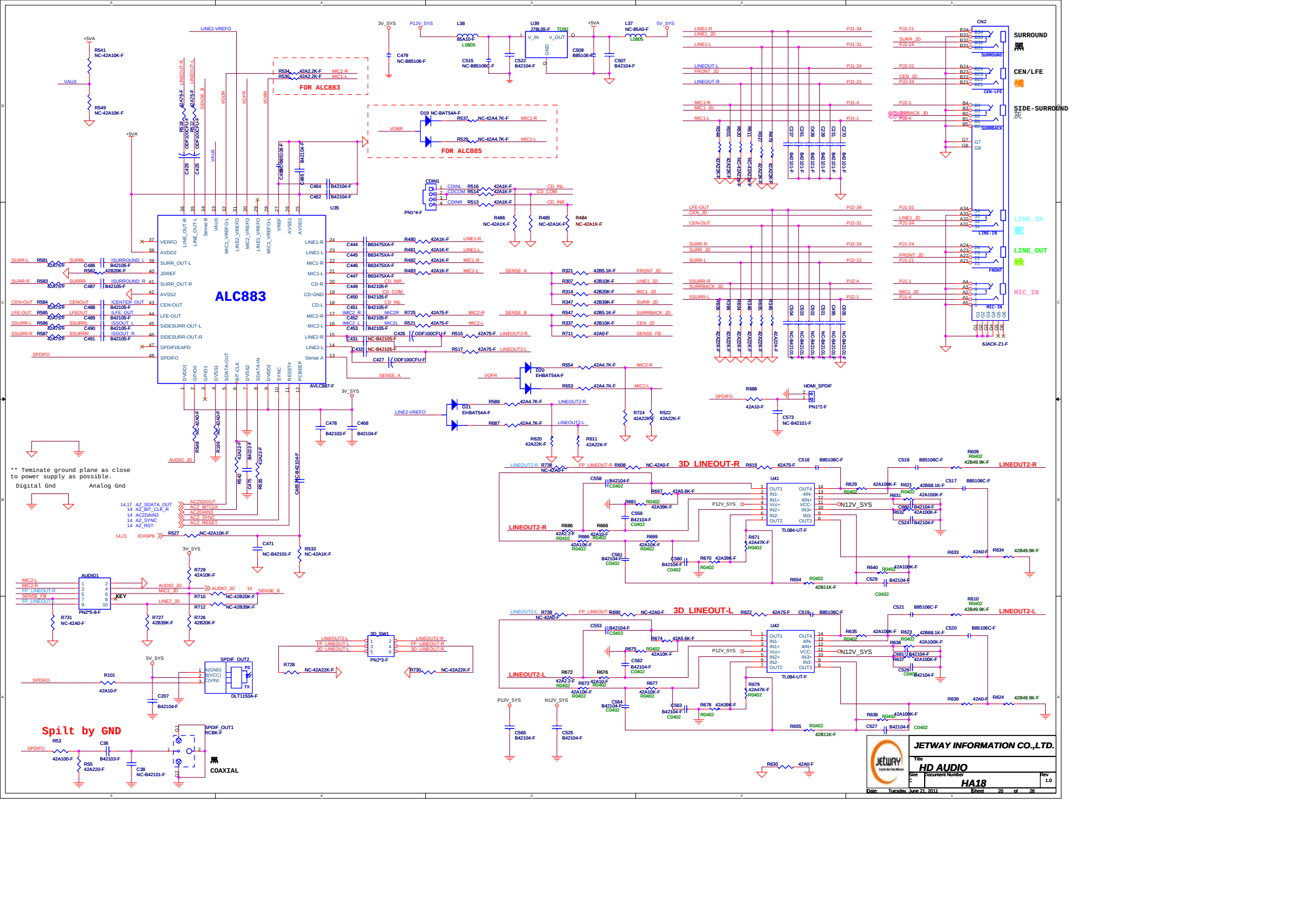
ALC883
FOR ALC883
FOR ALC885
3D_LINEOUT-R
3D_LINEOUT-L
SURROUND
CEN/LFE
SIDE-SURROUND
LINE_IN
LINE_OUT
MIC_IN
COAXIAL
Spilt by GND
** Teminate ground plane as close to power supply as possible.
Digital Gnd
Analog Gnd
JETWAY INFORMATION CO.,LTD.
HD AUDIO
HA18
Date: Tuesday, June 21, 2011
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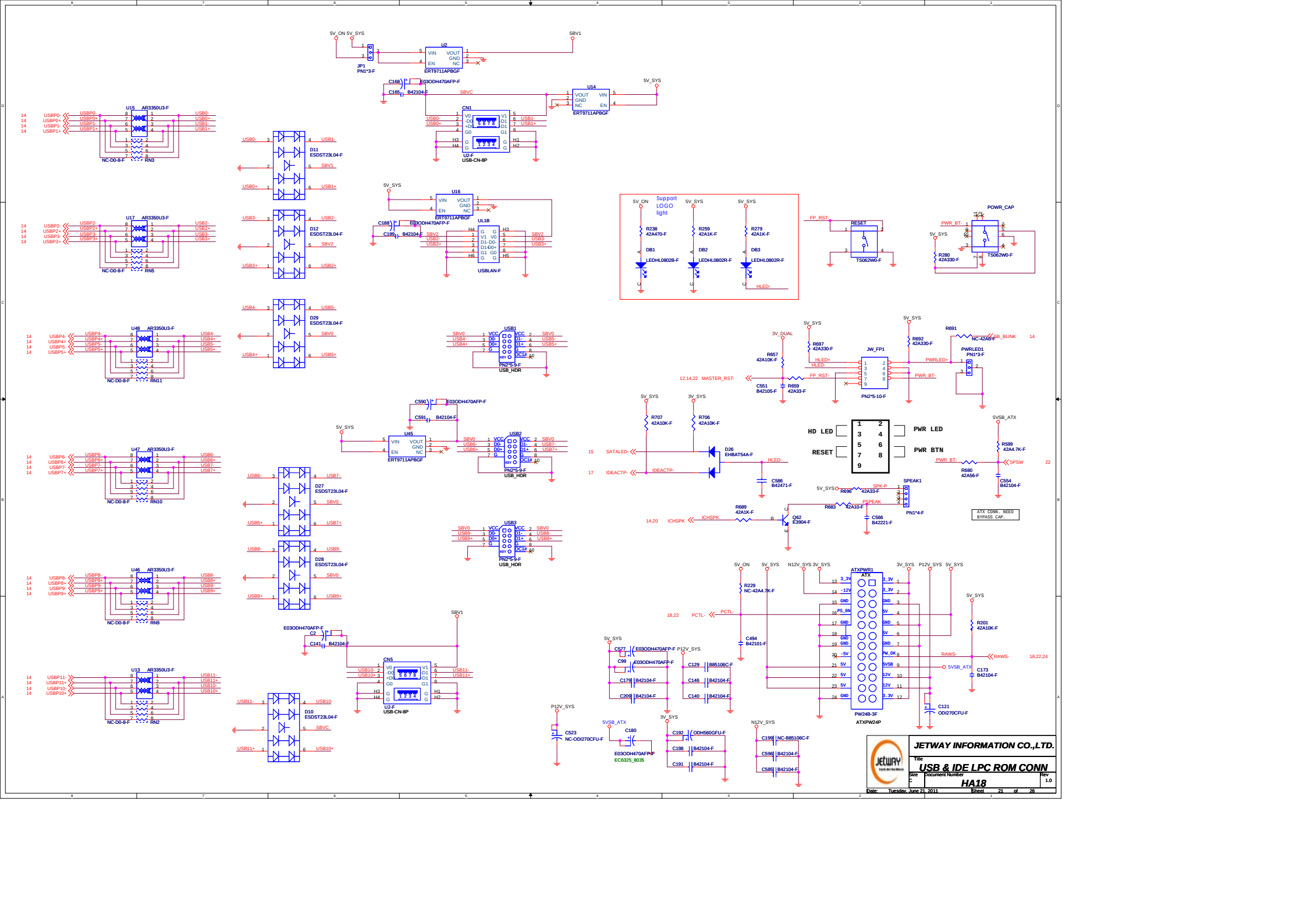
JETWAY INFORMATION CO.,LTD.
Title
USB & IDE LPC ROM CONN
Size C
Document Number HA18
Rev 1.0
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Support LOGO light
HD LED
RESET
PWR LED
PWR BTN
ATX CONN. NEED BYPASS CAP.
U15 AR3350U3-F
U17 AR3350U3-F
U48 AR3350U3-F
U47 AR3350U3-F
U46 AR3350U3-F
U13 AR3350U3-F
U2 ERT9711APBGF
U14 ERT9711APBGF
U16 ERT9711APBGF
U45 ERT9711APBGF
U1B USBLAN-F
U2-F USB-CN-8P
U2-F USB-CN-8P
USB1 USB_HDR
USB2 USB_HDR
USB3 USB_HDR
ATXPWR1 ATX
PW24B-3F ATXPW24P

POWER-ON TRIP

PIN	Function	NET Name	HI	LO
26	FANCTL3	FANCTL3	PWM FAN	LINEAR FAN
24	FANCTL2	FANCTL2	PWM FAN	LINEAR FAN
22	FANCTL1	FANCTL1	PWM FAN	LINEAR FAN
121	DTR1#	FAN40_100	FAN SPEED DUTY:40%	FAN SPEED DUTY:100%
124	SOUT1#	Config 4E/2E	4E	2E
52	TIMING/GPIO	TIMING/GPIO	TIMING	GPIO

SYSFAN 1

SYSFAN 2

CPU FAN

COM1

KB

EUP Function

JETWAY INFORMATION CO.,LTD.	
Title: LPC & H/W DOCTOR	
Size: C	Document Number: HA18
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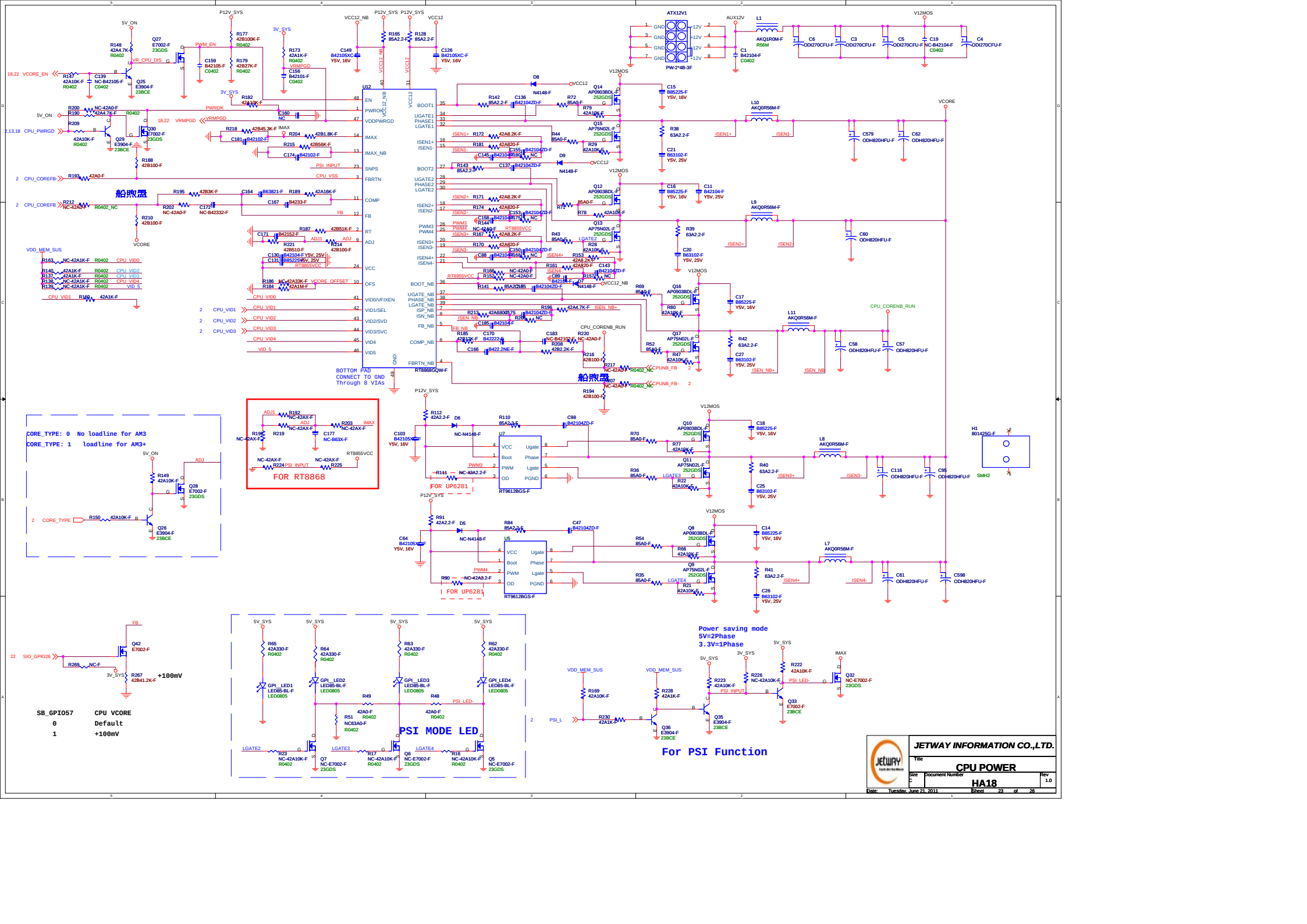
U12
RT8868GQW-F
BOTTOM PAD
CONNECT TO GND
Through 8 VIAs
FOR RT8868
FOR UP6281
FOR UP6281
U7
RT9612BGS-F
U5
RT9612BGS-F
PSI MODE LED
For PSI Function
Power saving mode
5V=2Phase
3.3V=1Phase
CORE_TYPE: 0 No loadline for AM3
CORE_TYPE: 1 loadline for AM3+
SB_GPIO57 CPU VCORE
0 Default
1 +100mV
JETWAY INFORMATION CO.,LTD.
CPU POWER
HA18
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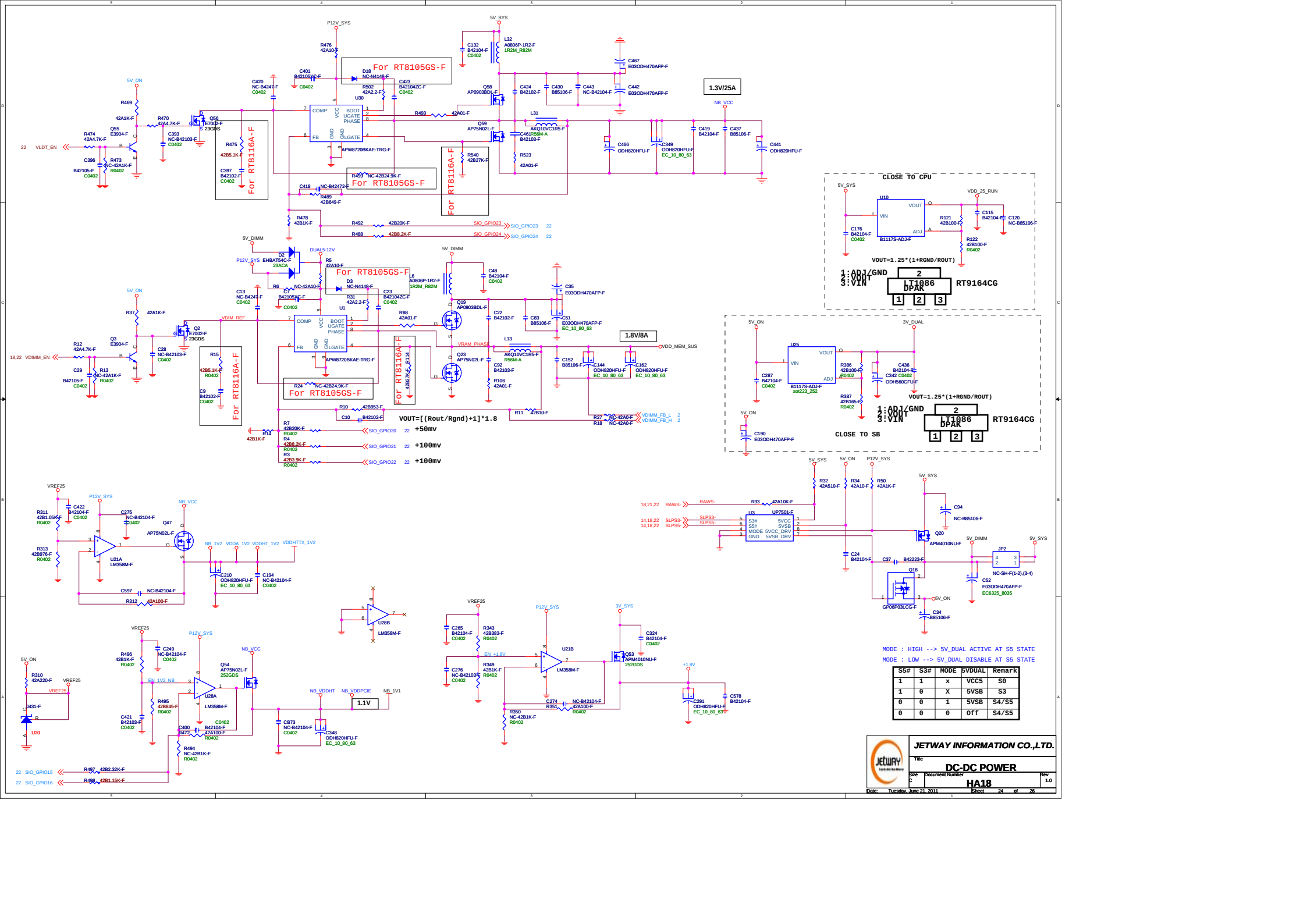
For RT8105GS-F
For RT8116A-F
For RT8116A-F
For RT8105GS-F
For RT8116A-F
For RT8105GS-F
1.3V/25A
1.8V/8A
1.1V
CLOSE TO CPU
CLOSE TO SB
VOUT=1.25*(1+RGND/ROUT)
1:ADJ/GND
2:VOUT
3:VIN
LT1086 DPAK
RT9164CG
VOUT=[(Rout/Rgnd)+1]*1.8
+50mv
+100mv
+100mv
MODE : HIGH --> 5V_DUAL ACTIVE AT S5 STATE
MODE : LOW --> 5V_DUAL DISABLE AT S5 STATE
S5# S3# MODE 5VDUAL Remark
1 1 x VCC5 S0
1 0 X 5VSB S3
0 0 1 5VSB S4/S5
0 0 0 Off S4/S5
JETWAY INFORMATION CO.,LTD.
DC-DC POWER
HA18
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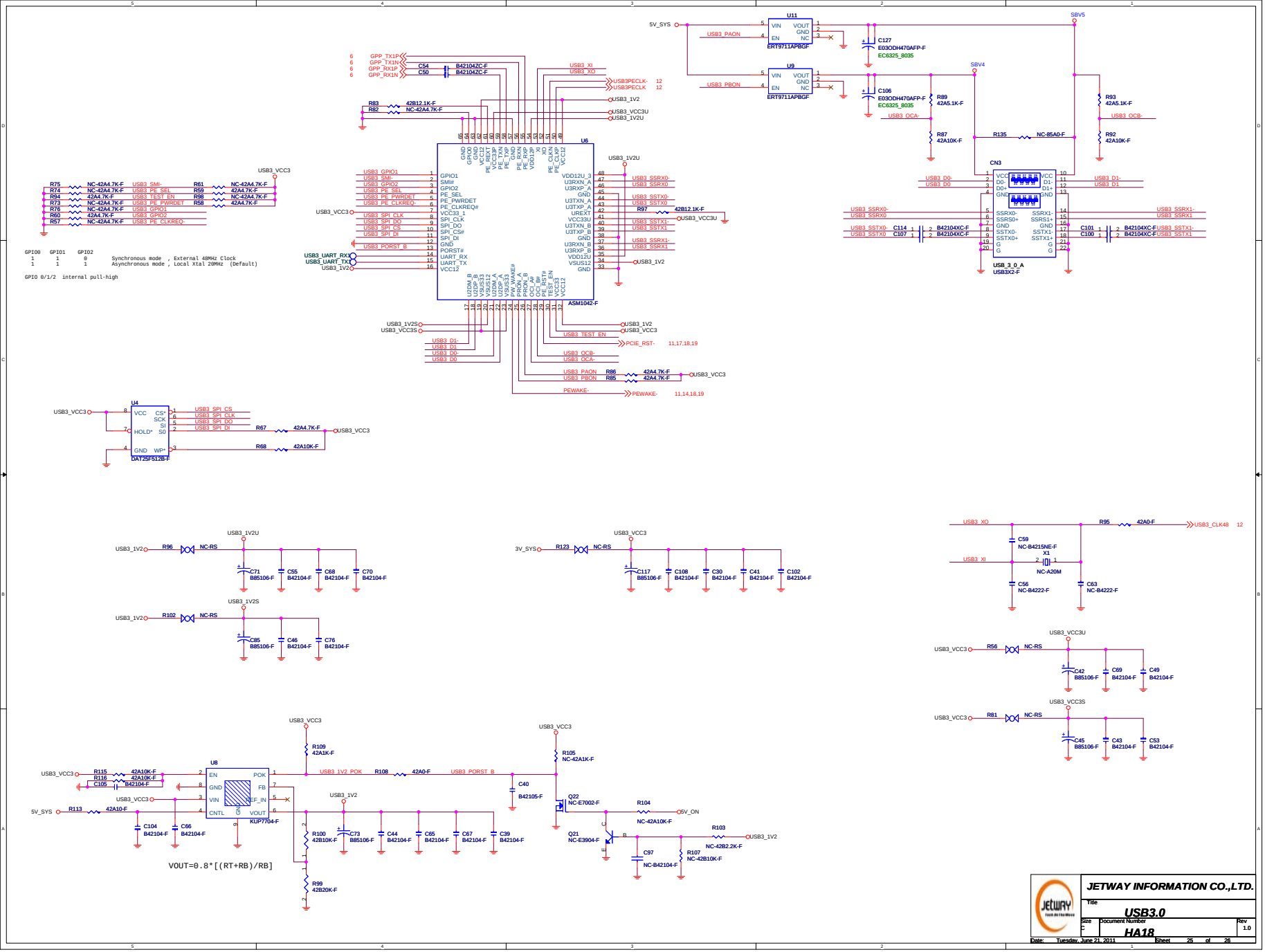
U11
ERT9711APBGF
U9
ERT9711APBGF
5V_SYS
USB3_PAON
USB3_PBON
C127
E03ODH470AFP-F
EC6325_8035
C106
E03ODH470AFP-F
EC6325_8035
SBV5
SBV4
R89
42A5.1K-F
R87
42A10K-F
R135
NC-85A0-F
R93
42A5.1K-F
R92
42A10K-F
USB3_OCA-
USB3_OCB-
CN3
USB_3_0_A
USB3X2-F
USB3_D0-
USB3_D0
USB3_D1-
USB3_D1
USB3_SSRX0-
USB3_SSRX0
USB3_SSTX0-
USB3_SSTX0
USB3_SSRX1-
USB3_SSRX1
USB3_SSTX1-
USB3_SSTX1
C114
C107
C101
C100
B42104XC-F
GPP_TX1P
GPP_TX1N
GPP_RX1P
GPP_RX1N
C54
C50
B42104ZC-F
USB3_XI
USB3_XO
USB3PECLK-
USB3PECLK
R83
R82
42B12.1K-F
NC-42A4.7K-F
USB3_1V2
USB3_VCC3U
USB3_1V2U
U6
ASM1042-F
R97
42B12.1K-F
USB3_VCC3U
USB3_GPIO1
USB3_SMI-
USB3_GPIO2
USB3_PE_SEL
USB3_PE_PWRDET
USB3_PE_CLKREQ-
USB3_SPI_CLK
USB3_SPI_DO
USB3_SPI_CS
USB3_SPI_DI
USB3_PORST_B
USB3_UART_RX3
USB3_UART_TX
USB3_1V2S
USB3_VCC3S
USB3_TEST_EN
PCIE_RST-
11,17,18,19
PEWAKE-
11,14,18,19
R86
R85
42A4.7K-F
R75
R74
R94
R73
R76
R60
R57
R61
R59
R98
R58
NC-42A4.7K-F
42A4.7K-F
GPIO0 GPIO1 GPIO2
1 1 1 Synchronous mode , External 48Mhz Clock
1 1 0 Asynchronous mode , Local Xtal 20Mhz (Default)
GPIO 0/1/2 internal pull-high
U4
DAT25F5128-F
USB3_SPI_CS
USB3_SPI_CLK
USB3_SPI_DO
USB3_SPI_DI
R67
R68
42A4.7K-F
42A10K-F
USB3_1V2U
USB3_1V2
R96
NC-RS
C71
B85106-F
C55
B42104-F
C68
B42104-F
C70
B42104-F
USB3_1V2S
R102
C95
C46
C76
3V_SYS
R123
USB3_VCC3
C117
C108
C30
C41
C102
USB3_XO
USB3_XI
R95
42A0-F
USB3_CLK48
12
C59
NC-B4215NE-F
X1
NC-A20M
C56
NC-B4222-F
C63
NC-B4222-F
USB3_VCC3U
R56
C42
C89
C49
USB3_VCC3S
R81
C45
C43
C53
U8
KUP7704-F
R115
R116
C105
R113
42A10K-F
42A10-F
C104
C66
R109
42A1K-F
USB3_1V2_POK
R108
42A0-F
USB3_PORST_B
R100
42B10K-F
C73
B85106-F
C44
C65
C67
C39
B42104-F
R99
42B20K-F
VOUT=0.8*[(RT+RB)/RB]
C40
B42105-F
R105
NC-42A1K-F
Q22
NC-E7002-F
R104
NC-42A10K-F
5V_ON
Q21
NC-E3904-F
R103
NC-42B2.2K-F
C97
NC-B42104-F
R107
NC-42B10K-F
JETWAY INFORMATION CO.,LTD.
Title
USB3.0
Size
C
Document Number
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Title: ACCESSORY

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