GA-990XA-UD3

Revision : 1.1

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Title: COVER SHEET		
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Model Name:GA-990XA-UD3

Component value change history

Version: 1.1

4 Layer, 4mil 50ohm +/- 15% L

P-Code: U98094-0

Date	Change Item	Reason
2011.03.04	0.1 New BOM Release. PCB Ver 0.1	
2011.04.12	1.0A E- BOM Release. PCB Ver 1.0	
2011.04.21	1.0B P- BOM Release. PCB Ver:1.0	R333 => 8.2K to fix backup BIOS can't show with ACBEL atx-350cn-an6fb.
		Add PR26=>22 for TPM. Change SB heatsink
2011.04.25	1.0C P- BOM Release. PCB Ver:1.01	Only remove SLI Logo
2011.04.29	1.0D P- BOM Release. PCB Ver:1.01	DDR3_4 and DDR3_1 Part NO. change
2011.06.09	1.0F MP BOM Release. PCB Ver:1.0	BC933 --> 1uF PCB Change to 1.0 w/SLI Logo
2011.07.22	11A BOM Release(DVT). PCB Ver:1.1	Add Load-Line Droop control
2011.08.15	11B P-BOM Release(SKIP PVT). PCB Ver:1.1	change Load-Line Droop 阻值 DR73,DR82,DR83,DR84 from 150 change 196 ohm

Circuit or PCB layout change for next version

Date	Change Item	Reason
2011.03.03	0.1 Gerber out	Modify from GA-890XA-UD3 2.1
2011.04.08	1.0 Gerber out	PWM GVOT ADD VCC PULL UP.
		Add Thermal Diode for AM3 CPU.
2011.04.25	1.01 Gerber out	Only remove SLI Logo
2011.07.20	1.1 Gerber out	Add CPU loadline control circuit.

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Title: BOM & PCB HISTORY

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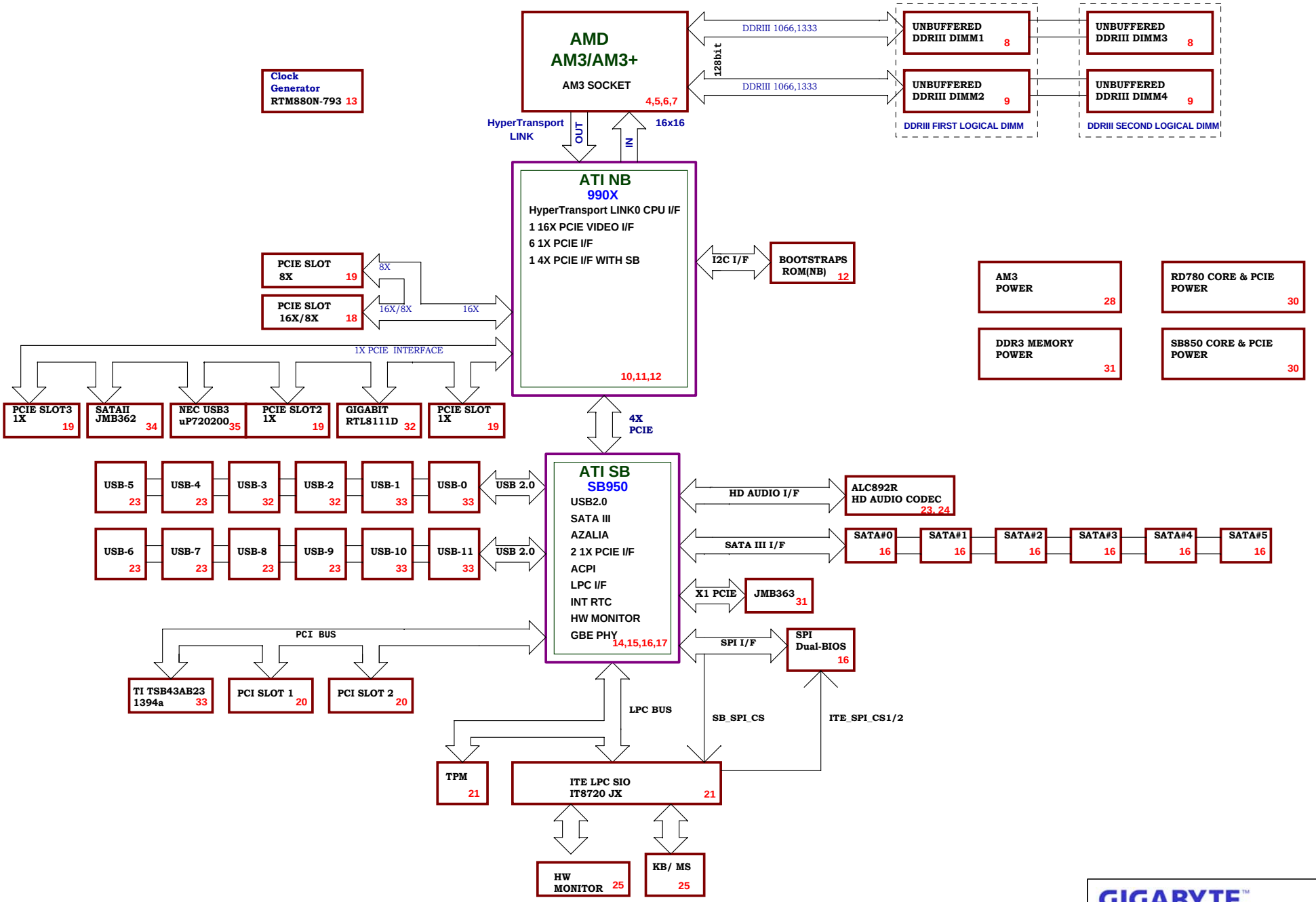

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Title: BLOCK DIAGRAM

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CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

L0_CADIN_L[0..15] L0_CADIN_L[0..15] <10>
L0_CADIN_H[0..15] L0_CADIN_H[0..15] <10>
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] <10>
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] <10>

M2CPUA
HYPERTRANSPORT

<10> L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 <10>
<10> L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 <10>
<10> L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 <10>
<10> L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 <10>
<10> L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 <10>
<10> L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 <10>
<10> L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 <10>
<10> L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 <10>
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AE5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/941AM3/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

COUPON1 COUPON1 1 2 COUPON/X VCC
COUPON2 COUPON2 1 2 COUPON/X

M2CPU
AM3RM/SC/BL/MB/[12KRC-04K812-31R]

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Title	CPU HYPER TRANSPORT		
Size: Custom	Document Number: GA-990XA-UD3		Rev: 1.1
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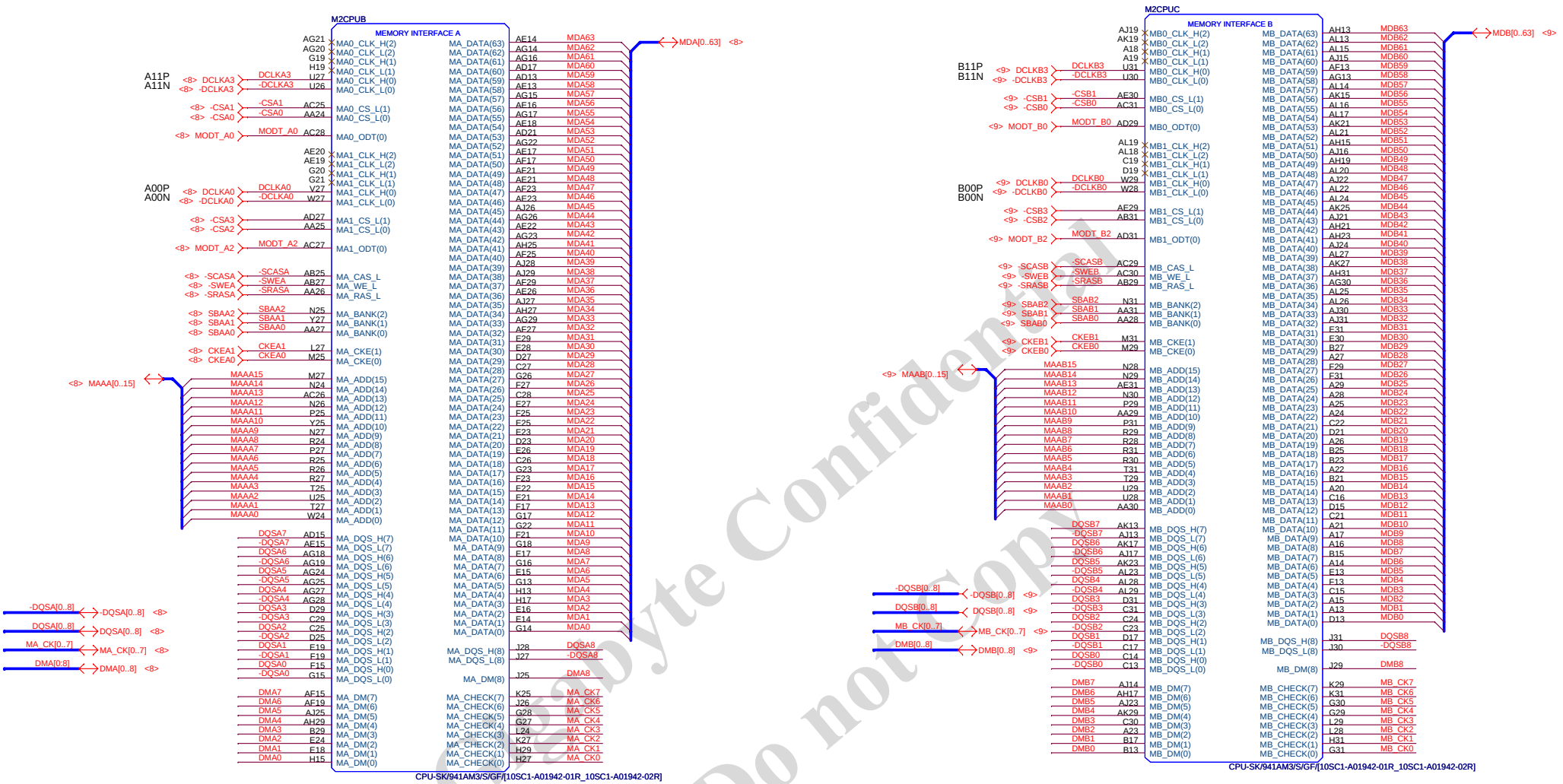

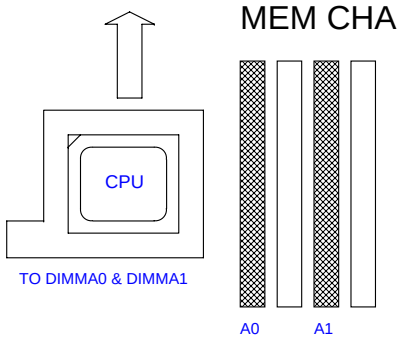

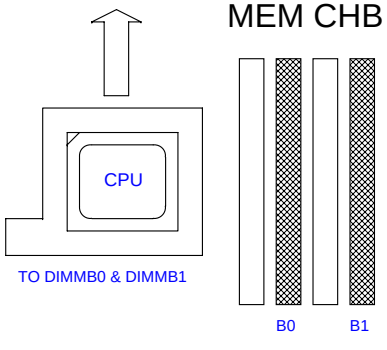

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Title	CPU DDRIII MEMORY	
Size: Custom	Document Number: GA-990XA-UD3	Rev: 1.1
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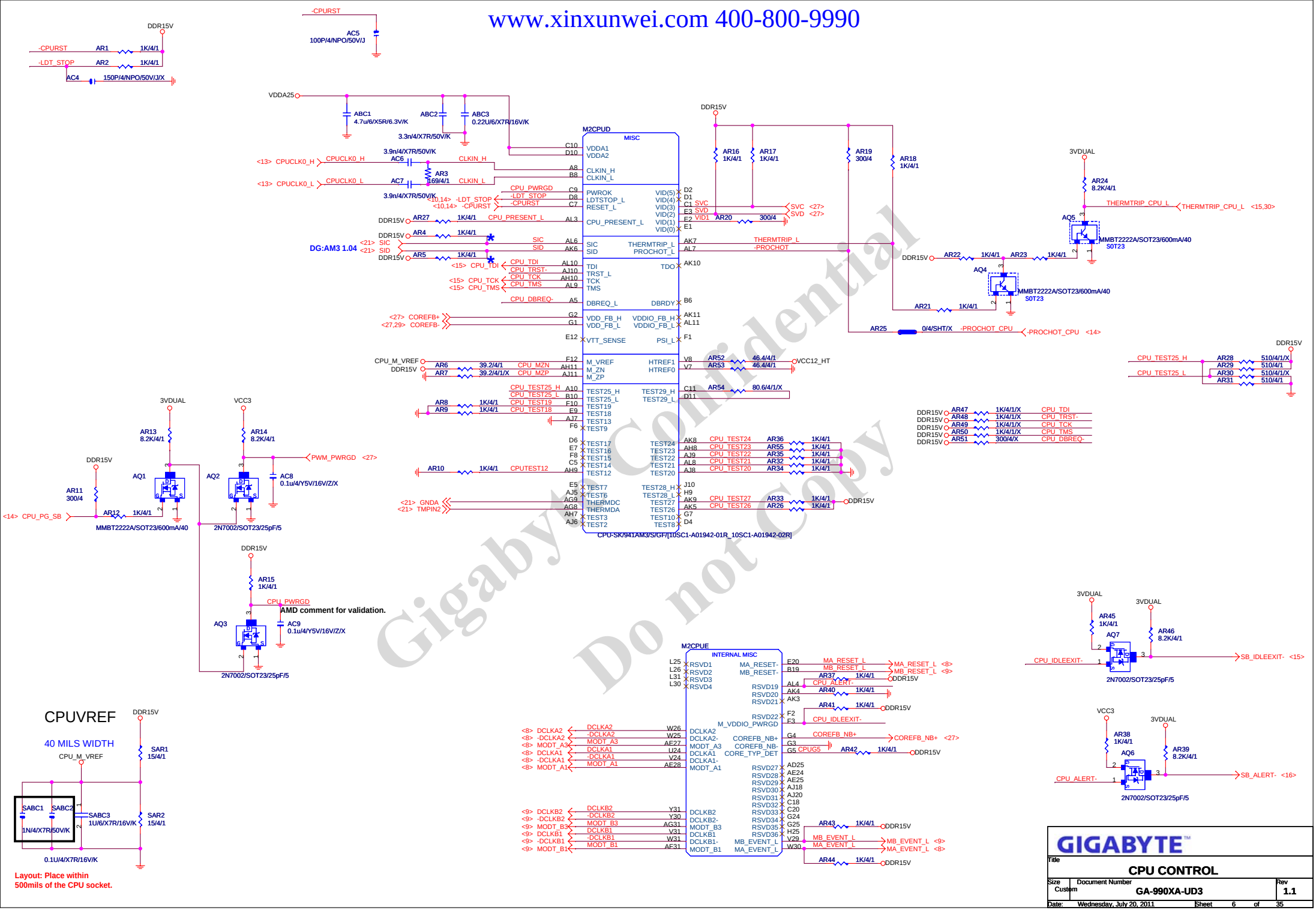
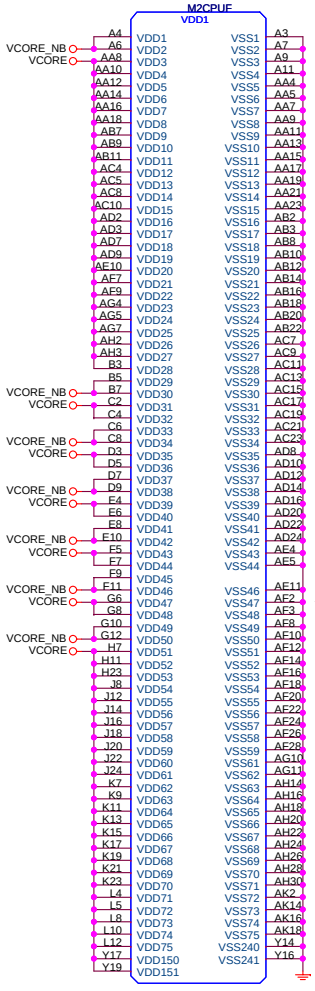
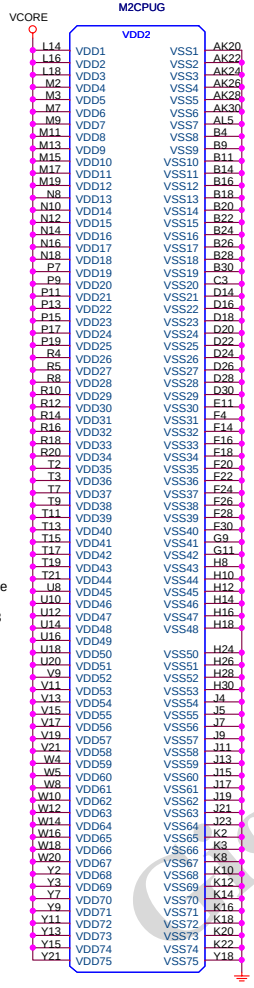
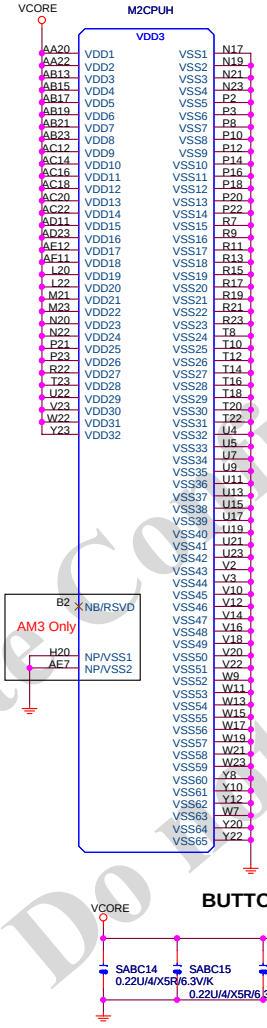
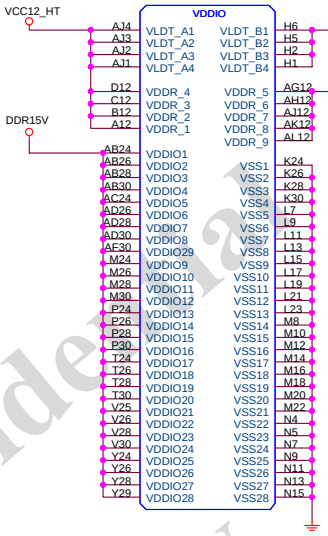


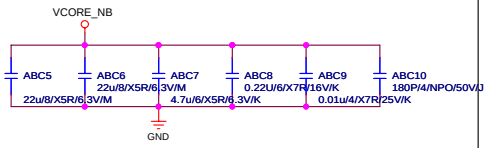
VLDT_RUN is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

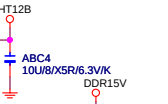


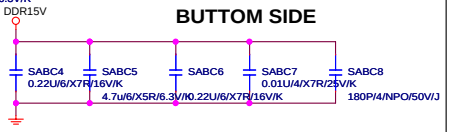


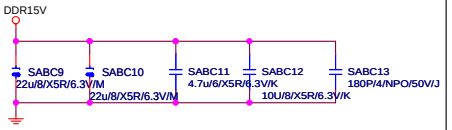


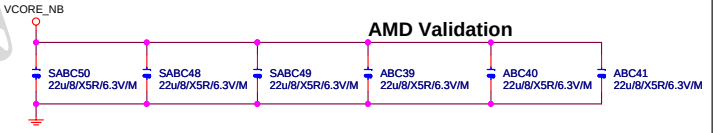


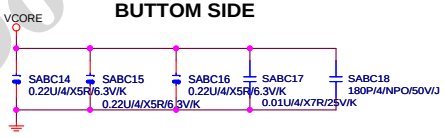


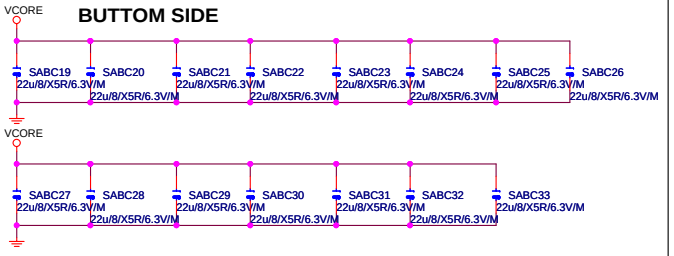


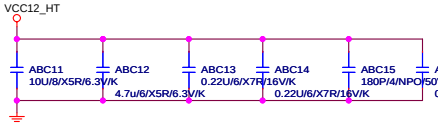


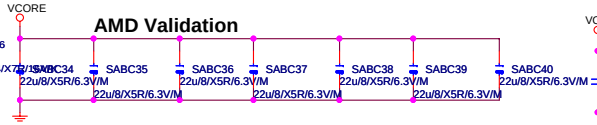


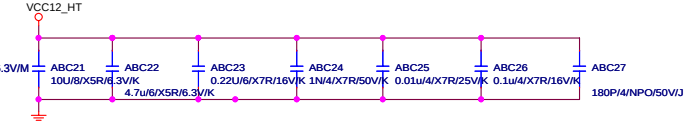


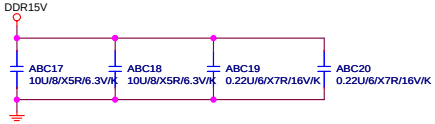


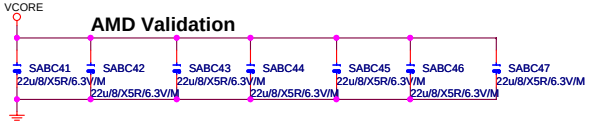


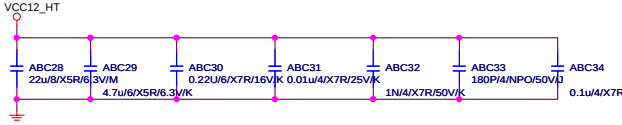


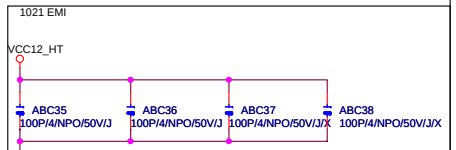












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Title: CPU POWER & GND

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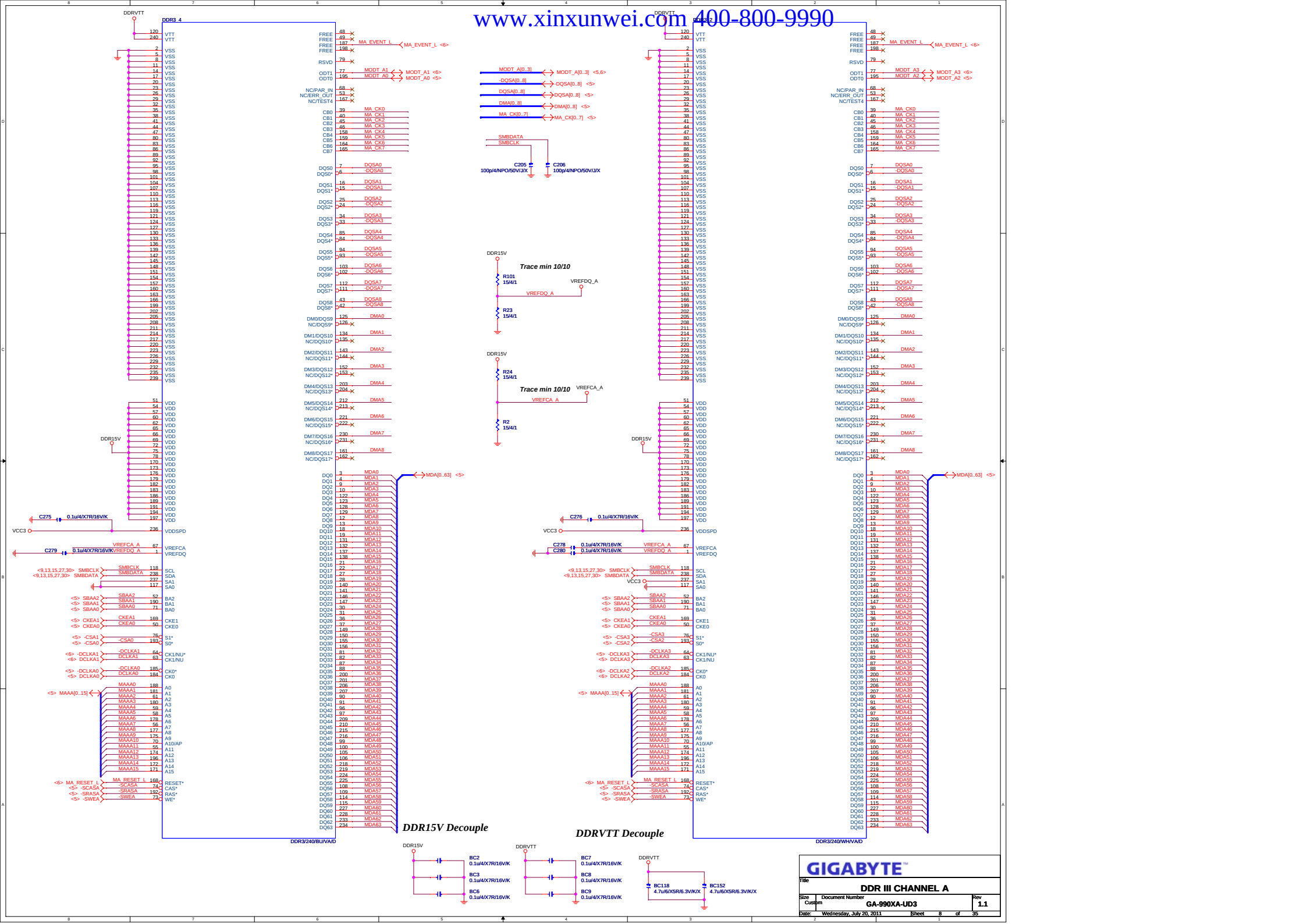

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Title	DDR III CHANNEL A	
Size: Custom	Document Number: GA-990XA-UD3	Rev: 1.1
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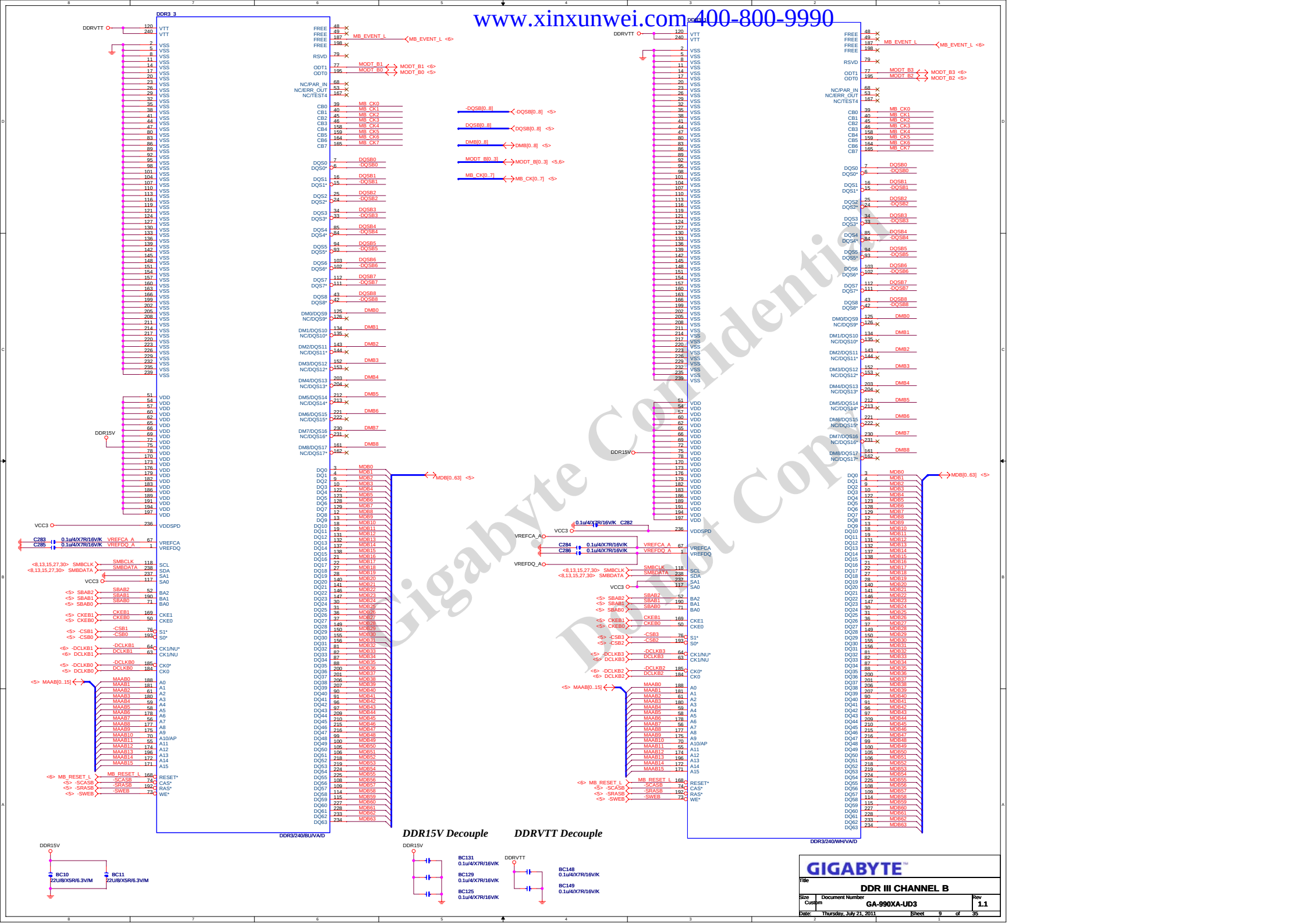

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Title: DDR III CHANNEL B

Size	Document Number	Rev
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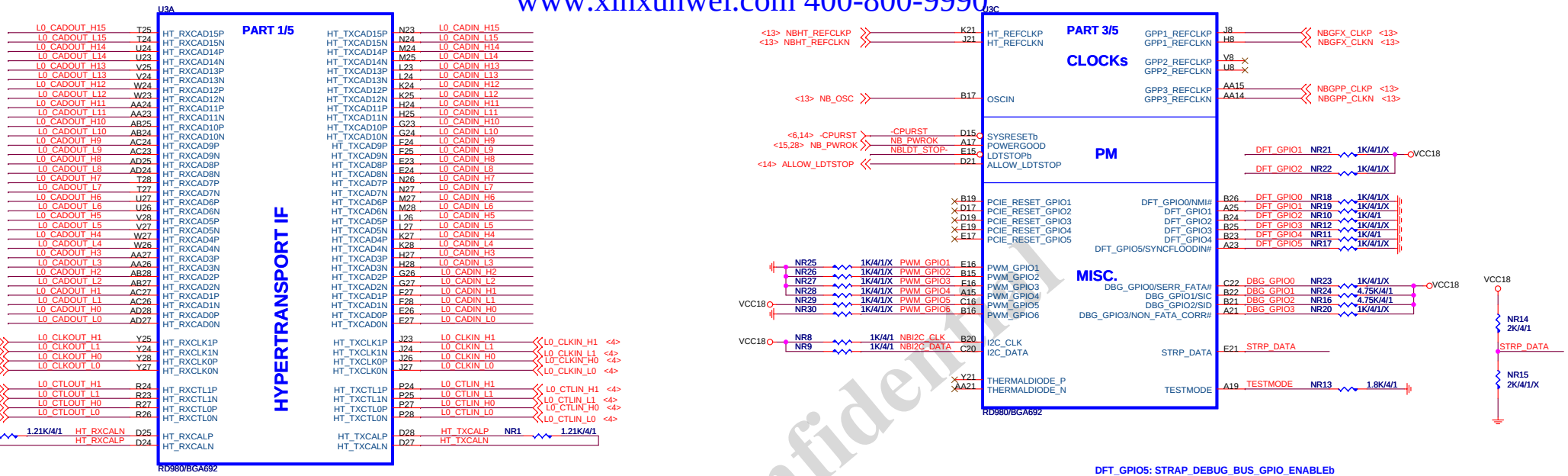

DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101: 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

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Title	RS780 HT-LINK I/F	
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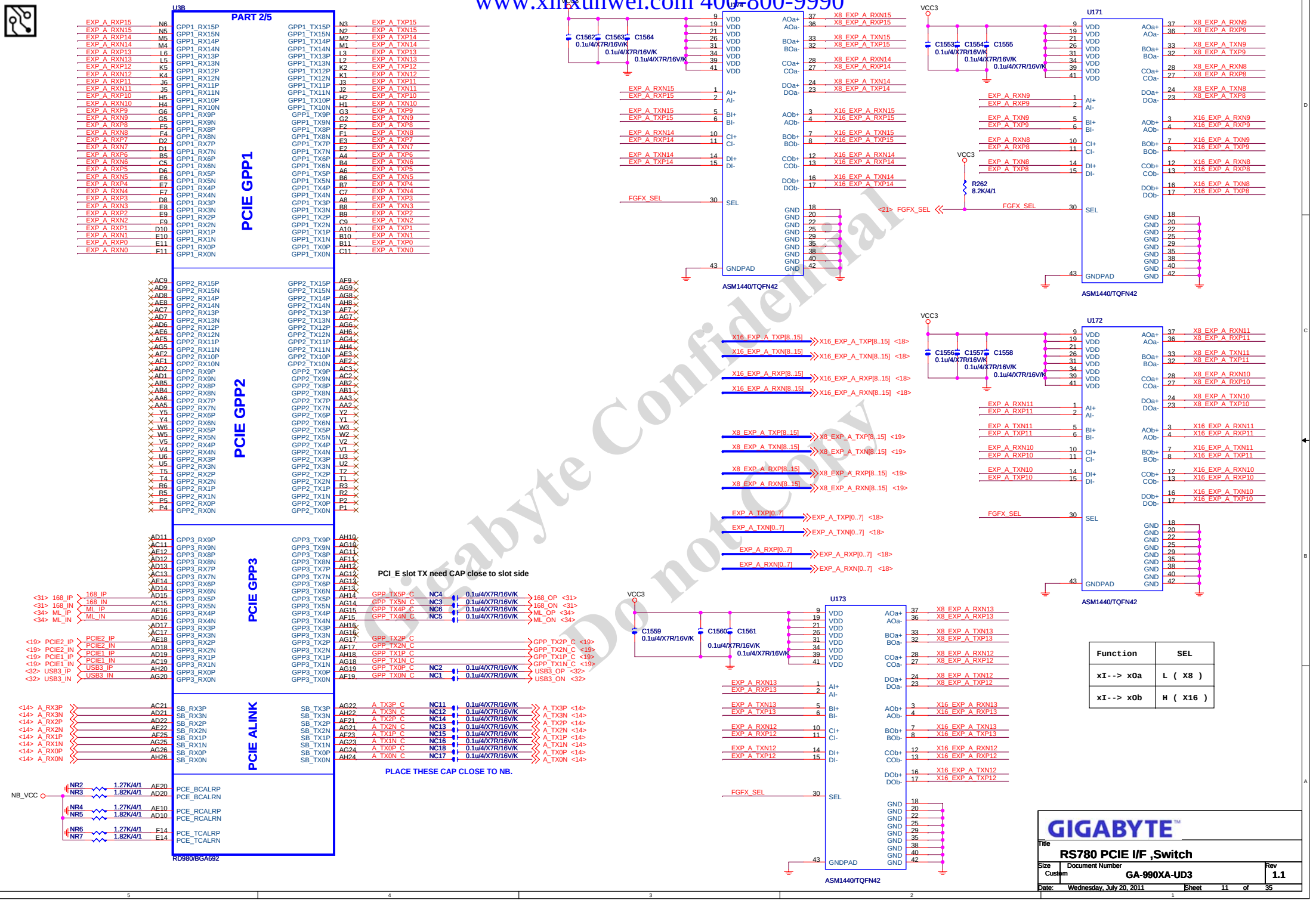


U3E

PART 5/5

GROUND

RD980/BGA692

U3D

PART 4/5

POWER

RD980/BGA692

NB_VCC

VDDHT=>1.1V@3.25A

SC42 1U/6/X7R/16V/K

C1613 0.1U/6/X7R/25V/K

C1614 10U/8/X5R/6.3V/K

VDDPCIE=>1.1V@5.5A

C1616 10U/8/X5R/6.3V/K

SC43 1U/6/X7R/16V/K

C1618 0.1U/6/X7R/25V/K

SC44 10U/8/X5R/6.3V/K

SC45 1U/6/X7R/16V/K

SBC2 1u/4/X5R/6.3V/K

C1624 0.1U/6/X7R/25V/K

SNC2 0.1U/6/X7R/25V/K

VDDA18=>1.8V@0.1A

VDDA18HTPLL=>1.8V@0.05A

VDDA18PCIE=>1.8V@2A

C1634 2.2U/6/X5R/6.3V/K

VCC18

1.1V@8500mA

SNC1 0.1U/6/X7R/25V/K

C1608 0.1U/6/X7R/25V/K

SC50 0.1U/6/X7R/25V/K

SC51 1U/6/X7R/16V/K

SC41 1U/6/X7R/16V/K

SC40 22u/8/X5R/6.3V/M

SBC3 1u/4/X5R/6.3V/K

VCC12_HT

VDDHTTX=>1.2V@1A

C1626 0.1U/6/X7R/25V/K

C1627 0.1U/6/X7R/25V/K

C1628 0.1U/6/X7R/25V/K

C1631 1U/6/X7R/16V/K

SC46 1U/6/X7R/16V/K

SC47 10U/8/X5R/6.3V/K

C1635 10U/8/X5R/6.3V/K

SBC1 1U/4/X5R/6.3V/K

C1637 0.1U/4/X7R/16V/K

SC48 22U/8/X5R/6.3V/M

SC49 1U/6/X7R/16V/K

C1640 0.1U/4/X7R/16V/K

C1641 0.1U/4/X7R/16V/K

C1642 0.1U/4/X7R/16V/K

VCORE

C147 0.1u/4/X7R/16V/K/X

C148 0.1u/4/X7R/16V/K/X

C149 0.1u/4/X7R/16V/K/X

C150 0.1u/4/X7R/16V/K/X

C151 0.1u/4/X7R/16V/K/X

HT Link Stitching Caps

SBC29 1u/4/X5R/6.3V/K

SBC36 1u/4/X5R/6.3V/K

SBC38 1u/4/X5R/6.3V/K

BC141 1u/4/X5R/6.3V/K

SBC28 1u/4/X5R/6.3V/K

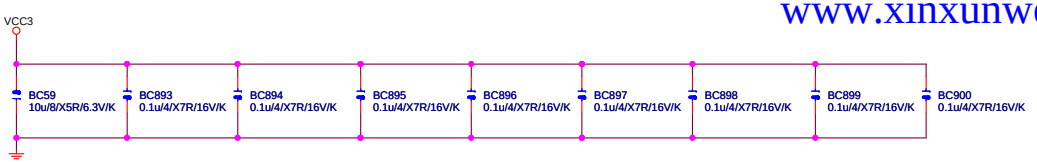
SBC37 1u/4/X5R/6.3V/K

GIGABYTE™

Title: RS780 POWER & GND

Size: Custom | Document Number: GA-990XA-UD3 | Rev: 1.1

Date: Wednesday, July 20, 2011 | Sheet 12 of 35



1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

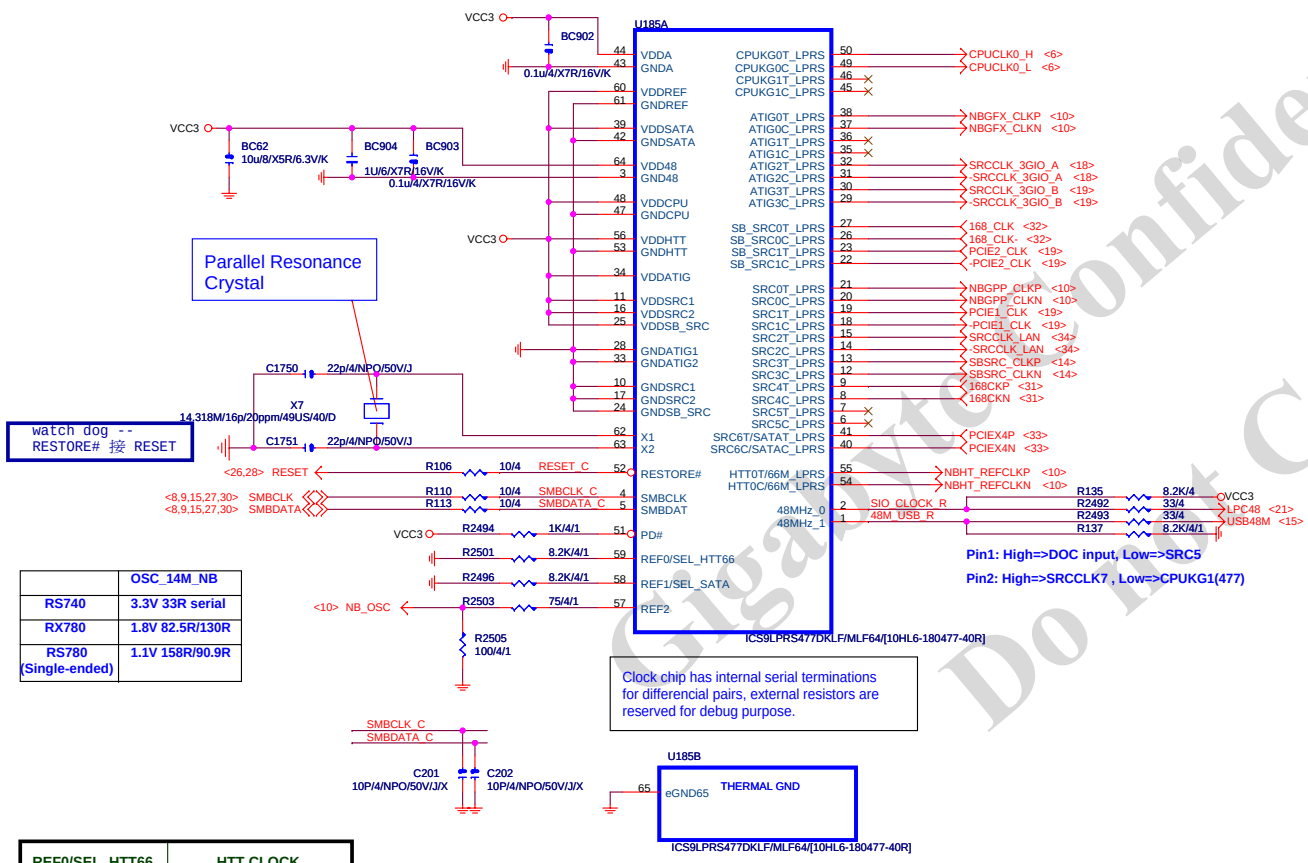
3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

GIGABYTE™

Title: RTM880N-793

Size: Custom | Document Number: GA-990XA-UD3 | Rev: 1.1

Date: Wednesday, July 20, 2011 | Sheet 13 of 35

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

S.B HEATSINK

SB_HS

SB_HS/[12SP2-S06510-11R_12SP2-S06510-12R_12SP2-S06510-13R]

PX1
SHW/D0.64*5.08*6.74

U2A
SB800 Part 1 of 5

PCI EXPRESS INTERFACES
PCIE_RST#
A_RST#
A_TX0P
A_TX0N
A_TX1P
A_TX1N
A_TX2P
A_TX2N
A_TX3P
A_TX3N
A_RX0P
A_RX0N
A_RX1P
A_RX1N
A_RX2P
A_RX2N
A_RX3P
A_RX3N
PCIE_CALRP
PCIE_CALRN
GPP_TX0P
GPP_TX0N
GPP_TX1P
GPP_TX1N
GPP_TX2P
GPP_TX2N
GPP_TX3P
GPP_TX3N
GPP_RX0P
GPP_RX0N
GPP_RX1P
GPP_RX1N
GPP_RX2P
GPP_RX2N
GPP_RX3P
GPP_RX3N

PCI CLKS
PCICLK0
PCICLK1/GPO36
PCICLK2/GPO37
PCICLK3/GPO38
PCICLK4/14M_OSC/GPO39
PCIRST#

PCI INTERFACE
AD0/GPIO0 … AD31/GPIO31
CBE0# CBE1# CBE2# CBE3#
FRAME# DEVSEL# IRDY# TRDY# PAR STOP# PERR# SERR#
REQ0# REQ1#/GPIO40 REQ2#/CLK_REQ8#/GPIO41 REQ3#/CLK_REQ5#/GPIO42
GNT0# GNT1#/GPO44 GNT2#/GPO45 GNT3#/CLK_REQ7#/GPIO46
CLKRUN# LOCK#
INTE#/GPIO32 INTF#/GPIO33 INTG#/GPIO34 INTH#/GPIO35

CLOCK GENERATOR
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
GPP_CLK4P
GPP_CLK4N
GPP_CLK5P
GPP_CLK5N
GPP_CLK6P
GPP_CLK6N
GPP_CLK7P
GPP_CLK7N
GPP_CLK8P
GPP_CLK8N
14M_25M_48M_OSC
25M_X1
25M_X2

LPC
LPCCLK0
LPCCLK1
LAD0 LAD1 LAD2 LAD3
LFRAME#
LDRQ0#
LDRQ1#/CLK_REQ6#/GPIO49
SERIRQ/GPIO48

CPU
ALLOW_LDTSTP/DMA_ACTIVE#
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#

RTC
32K_X1
32K_X2
RTCCLK
INTRUDER_ALERT#
VDDBT_RTC_G

SB950/BGA605/[10HB1-06B950-10R]

RTC_XI
RTC_XO
PR6 20M/4
PX1 32.768K/12.5p/20ppm/TF38/35K/D
PC13 18P/4/NPO/50V/J
PC14 18P/4/NPO/50V/J

25MHZ_X1
25MHZ_X2
PR7 1M/4
PX2 25M/20p/30ppm/49US/20/D
PC15 22P/4/NPO/50V/J
PC16 22P/4/NPO/50V/J

PBC2 0.1U/6/X7R/25V/K

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

Low: Force PCIE GEN1, Up: Allow PCIE GEN2

	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

BIOS after boot setting
EC AOD-ACC

	LPC_CLK0 Rev.A12	LPC_CLK1
PULL HIGH	IMC ENABLED AOD Extreme	CLKGEN ENABLED
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT

20mil 20mil 20mil

BAT54C/SOT23/200mA
BAT-SK/BK/P/S/D/SN
CR2032 BAT

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

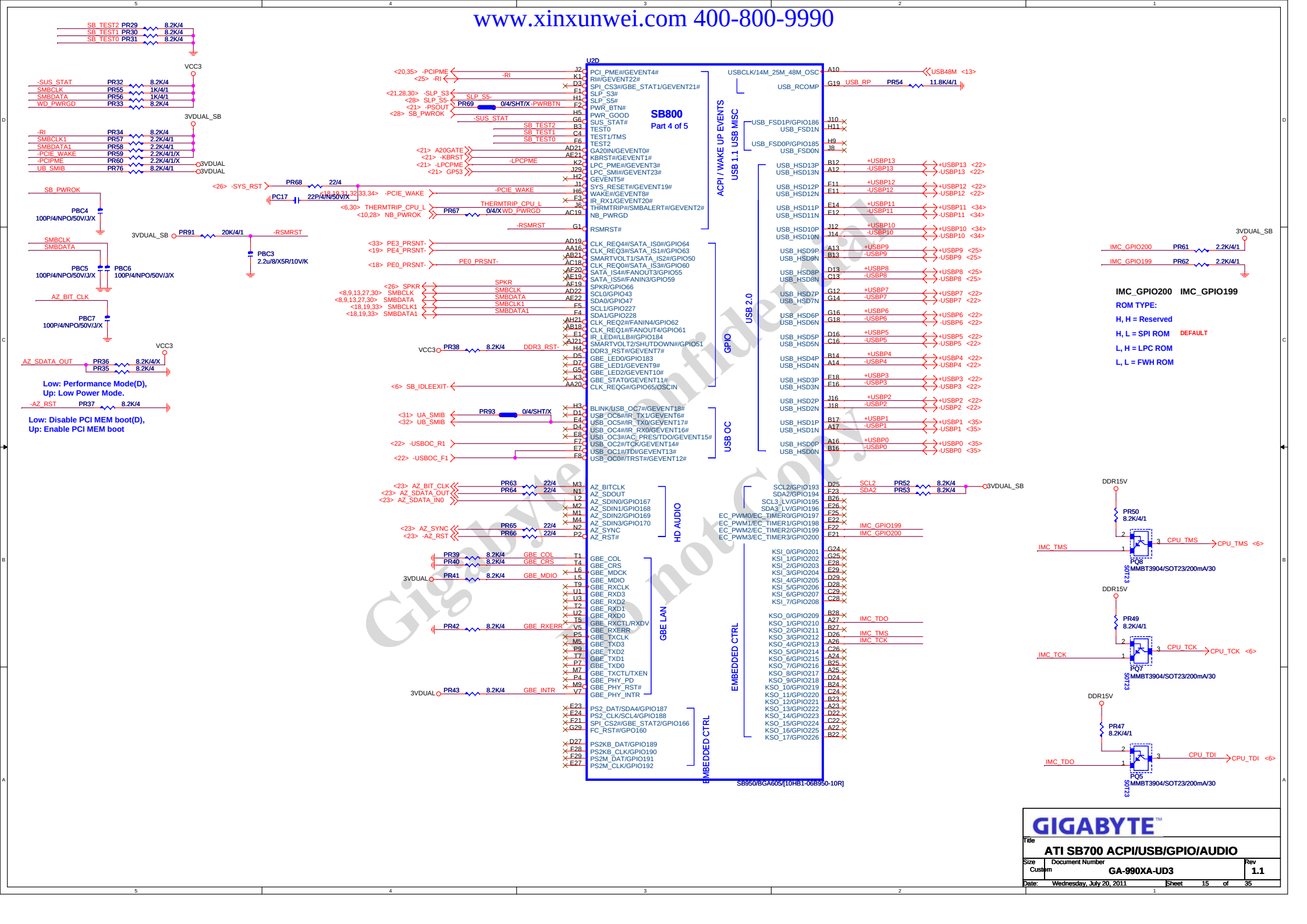
PH/1*2/BK/2.54/VA/D

GIGABYTE

Title: ATI SB700 PCIE/PCI/CPU/LPC

Size	Document Number	Rev
Custom	GA-990XA-UD3	1.1

Date: Wednesday, July 20, 2011 Sheet 14 of 35



PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

NOTE:
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

U2B

SB800
Part 2 of 5

SERIAL ATA
GPIOD
HW MONITOR
SPI ROM

SB950/BGA605/[10HB1-06B950-10R]

PLACE SATA AC COUPLING CAPS CLOSE TO SB850

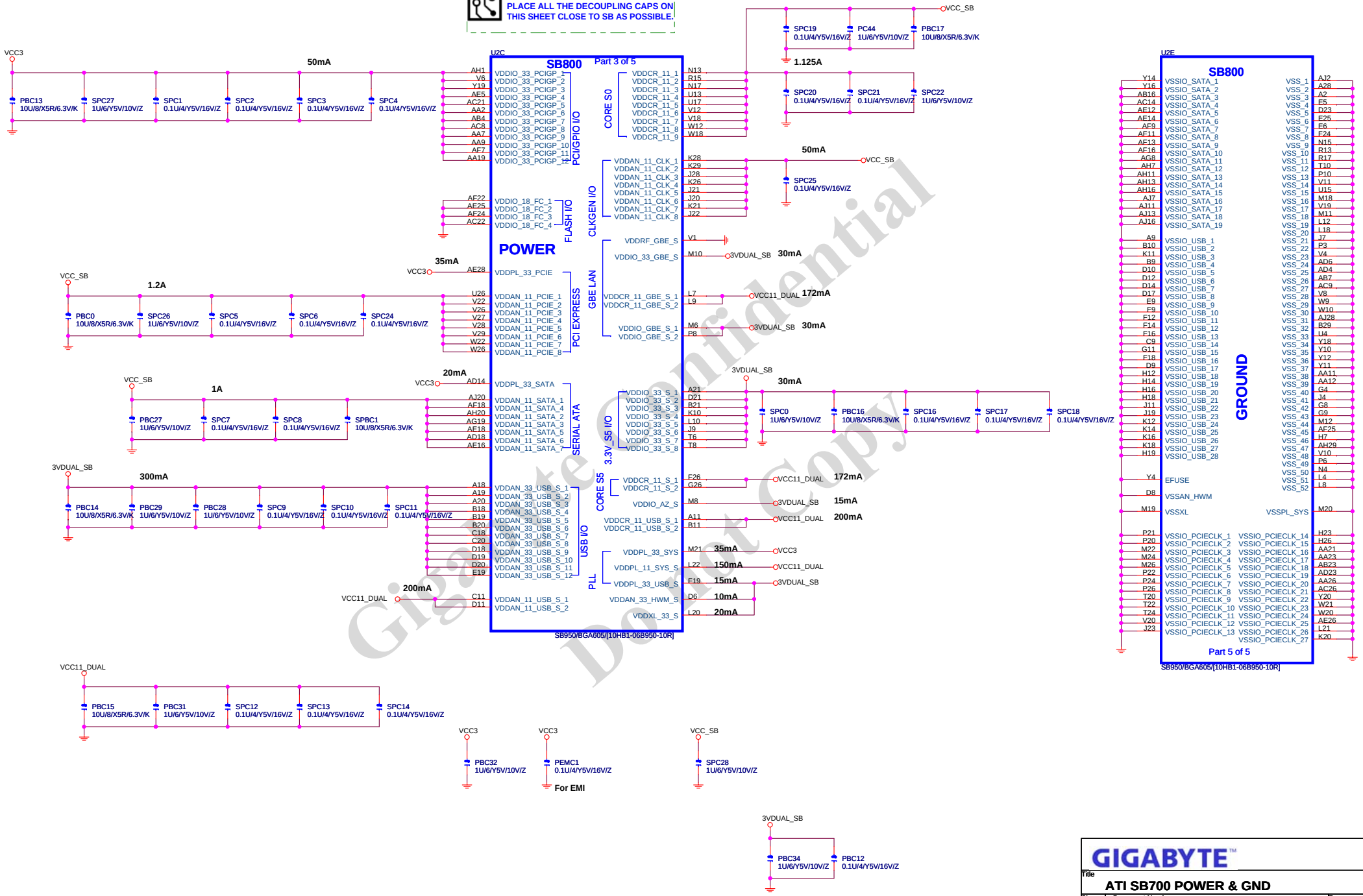
SATA3_0_1
SATA3_2_3
SATA3_4_5
SATA/14/BU/H/OP/RA/D/2

M_BIOS
B_BIOS
32M/SPI/SO8/200mil/S

GIGABYTE

Title	ATI SB700 SATA/IDE/HWM/SPI	
Size: Custom	Document Number: GA-990XA-UD3	Rev: 1.1
Date: Wednesday, July 20, 2011	Sheet 16 of 35	

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

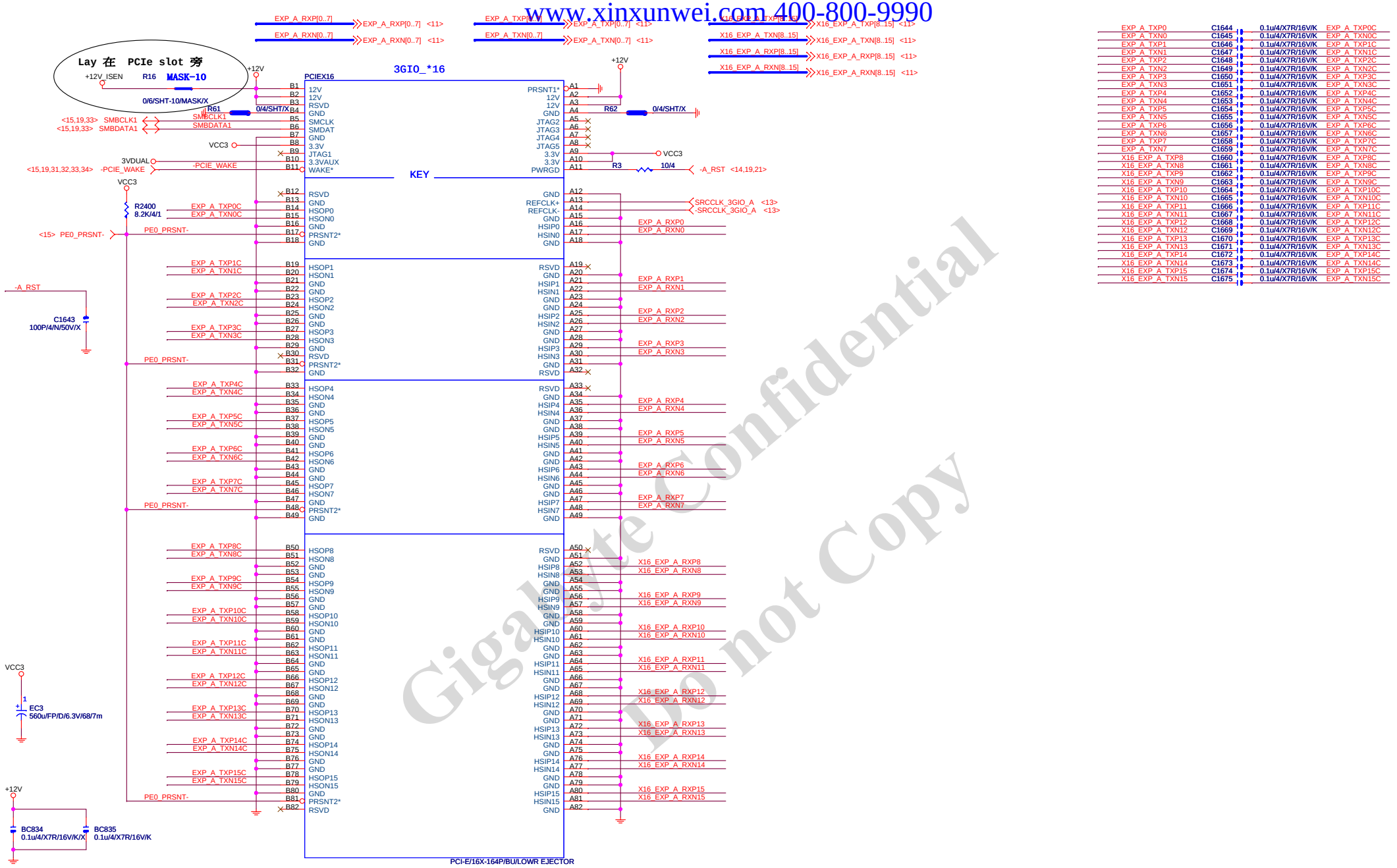


GIGABYTE™

Title: ATI SB700 POWER & GND

Size	Document Number	Rev
Custom	GA-990XA-UD3	1.1

Date: Wednesday, July 20, 2011 Sheet 17 of 35



EXP_A_TXP0	C1644	0.1u/4/X7R/16V/K EXP_A_TXP0C
EXP_A_TXN0	C1645	0.1u/4/X7R/16V/K EXP_A_TXN0C
EXP_A_TXP1	C1646	0.1u/4/X7R/16V/K EXP_A_TXP1C
EXP_A_TXN1	C1647	0.1u/4/X7R/16V/K EXP_A_TXN1C
EXP_A_TXP2	C1648	0.1u/4/X7R/16V/K EXP_A_TXP2C
EXP_A_TXN2	C1649	0.1u/4/X7R/16V/K EXP_A_TXN2C
EXP_A_TXP3	C1650	0.1u/4/X7R/16V/K EXP_A_TXP3C
EXP_A_TXN3	C1651	0.1u/4/X7R/16V/K EXP_A_TXN3C
EXP_A_TXP4	C1652	0.1u/4/X7R/16V/K EXP_A_TXP4C
EXP_A_TXN4	C1653	0.1u/4/X7R/16V/K EXP_A_TXN4C
EXP_A_TXP5	C1654	0.1u/4/X7R/16V/K EXP_A_TXP5C
EXP_A_TXN5	C1655	0.1u/4/X7R/16V/K EXP_A_TXN5C
EXP_A_TXP6	C1656	0.1u/4/X7R/16V/K EXP_A_TXP6C
EXP_A_TXN6	C1657	0.1u/4/X7R/16V/K EXP_A_TXN6C
EXP_A_TXP7	C1658	0.1u/4/X7R/16V/K EXP_A_TXP7C
EXP_A_TXN7	C1659	0.1u/4/X7R/16V/K EXP_A_TXN7C
X16_EXP_A_TXP8	C1660	0.1u/4/X7R/16V/K EXP_A_TXP8C
X16_EXP_A_TXN8	C1661	0.1u/4/X7R/16V/K EXP_A_TXN8C
X16_EXP_A_TXP9	C1662	0.1u/4/X7R/16V/K EXP_A_TXP9C
X16_EXP_A_TXN9	C1663	0.1u/4/X7R/16V/K EXP_A_TXN9C
X16_EXP_A_TXP10	C1664	0.1u/4/X7R/16V/K EXP_A_TXP10C
X16_EXP_A_TXN10	C1665	0.1u/4/X7R/16V/K EXP_A_TXN10C
X16_EXP_A_TXP11	C1666	0.1u/4/X7R/16V/K EXP_A_TXP11C
X16_EXP_A_TXN11	C1667	0.1u/4/X7R/16V/K EXP_A_TXN11C
X16_EXP_A_TXP12	C1668	0.1u/4/X7R/16V/K EXP_A_TXP12C
X16_EXP_A_TXN12	C1669	0.1u/4/X7R/16V/K EXP_A_TXN12C
X16_EXP_A_TXP13	C1670	0.1u/4/X7R/16V/K EXP_A_TXP13C
X16_EXP_A_TXN13	C1671	0.1u/4/X7R/16V/K EXP_A_TXN13C
X16_EXP_A_TXP14	C1672	0.1u/4/X7R/16V/K EXP_A_TXP14C
X16_EXP_A_TXN14	C1673	0.1u/4/X7R/16V/K EXP_A_TXN14C
X16_EXP_A_TXP15	C1674	0.1u/4/X7R/16V/K EXP_A_TXP15C
X16_EXP_A_TXN15	C1675	0.1u/4/X7R/16V/K EXP_A_TXN15C

GIGABYTE™

Title: PCI EXPRESS X 16 ,X1

Size: Custom | Document Number: GA-990XA-UD3 | Rev: 1.1

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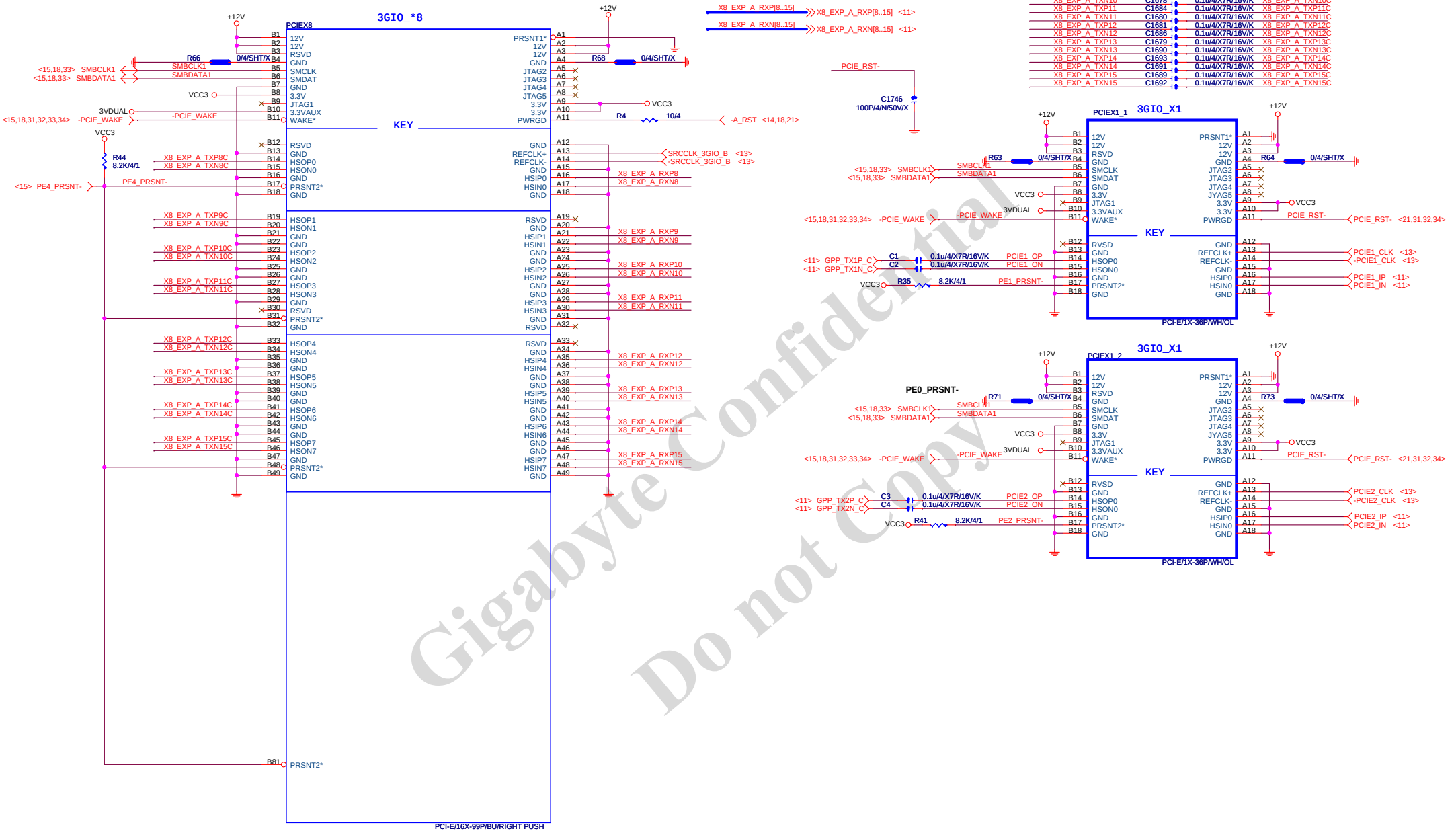


BC841	0.1u/4/X7R/16V/K	BC842	0.1u/4/X7R/16V/K
BC843	0.1u/4/X7R/16V/K	BC844	0.1u/4/X7R/16V/K
BC845	0.1u/4/X7R/16V/K	BC846	0.1u/4/X7R/16V/K
BC847	0.1u/4/X7R/16V/K	BC848	0.1u/4/X7R/16V/K
EC173	270u/FP/D/16V/89/10m	EC4	560u/FP/D/6.3V/68/7m

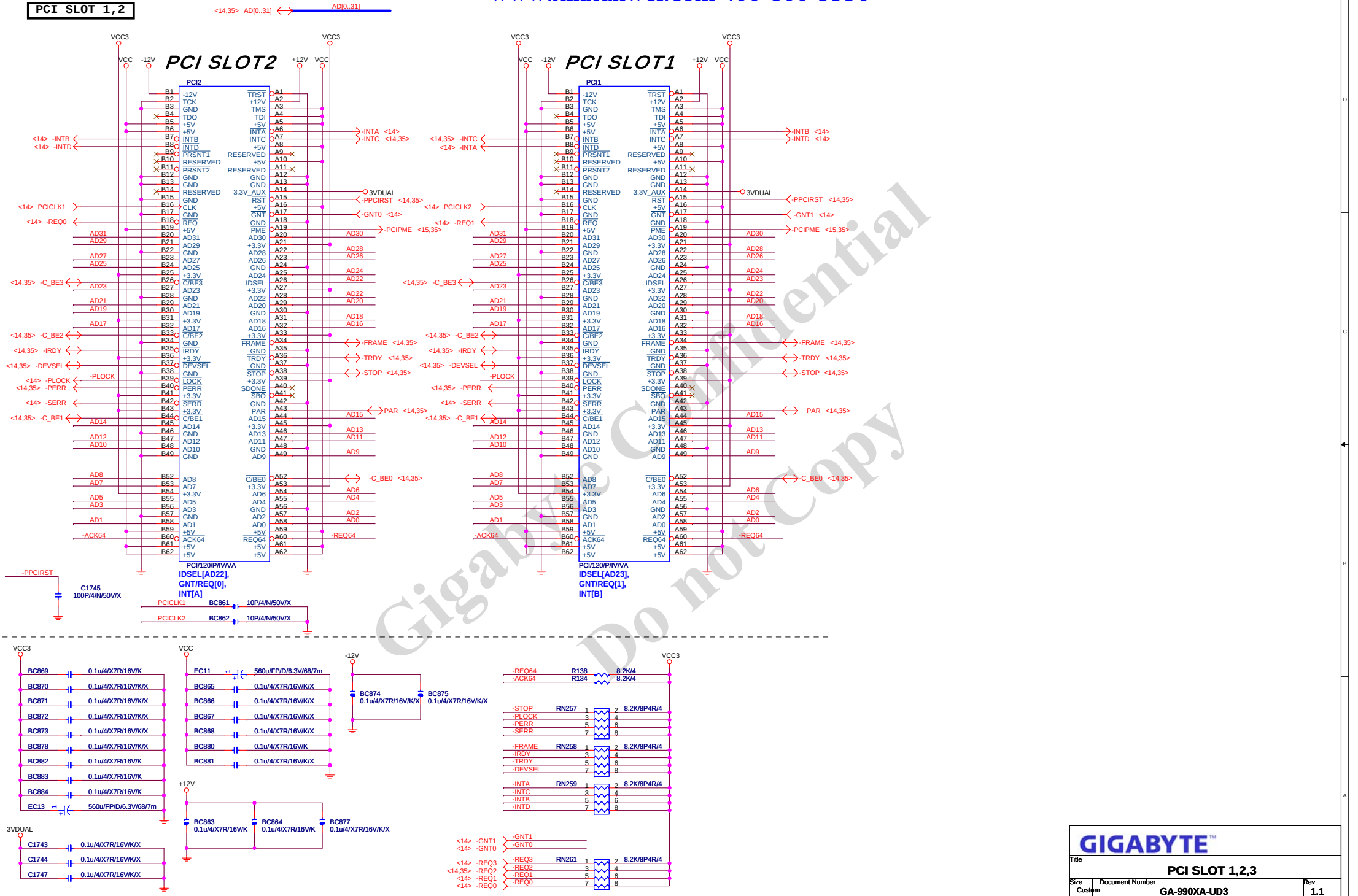
GIGABYTE

Title: PCI_E x8 ,PCI_E x1 SLOT 1,2

Size	Document Number	Rev
Custom	GA-990XA-UD3	1.1

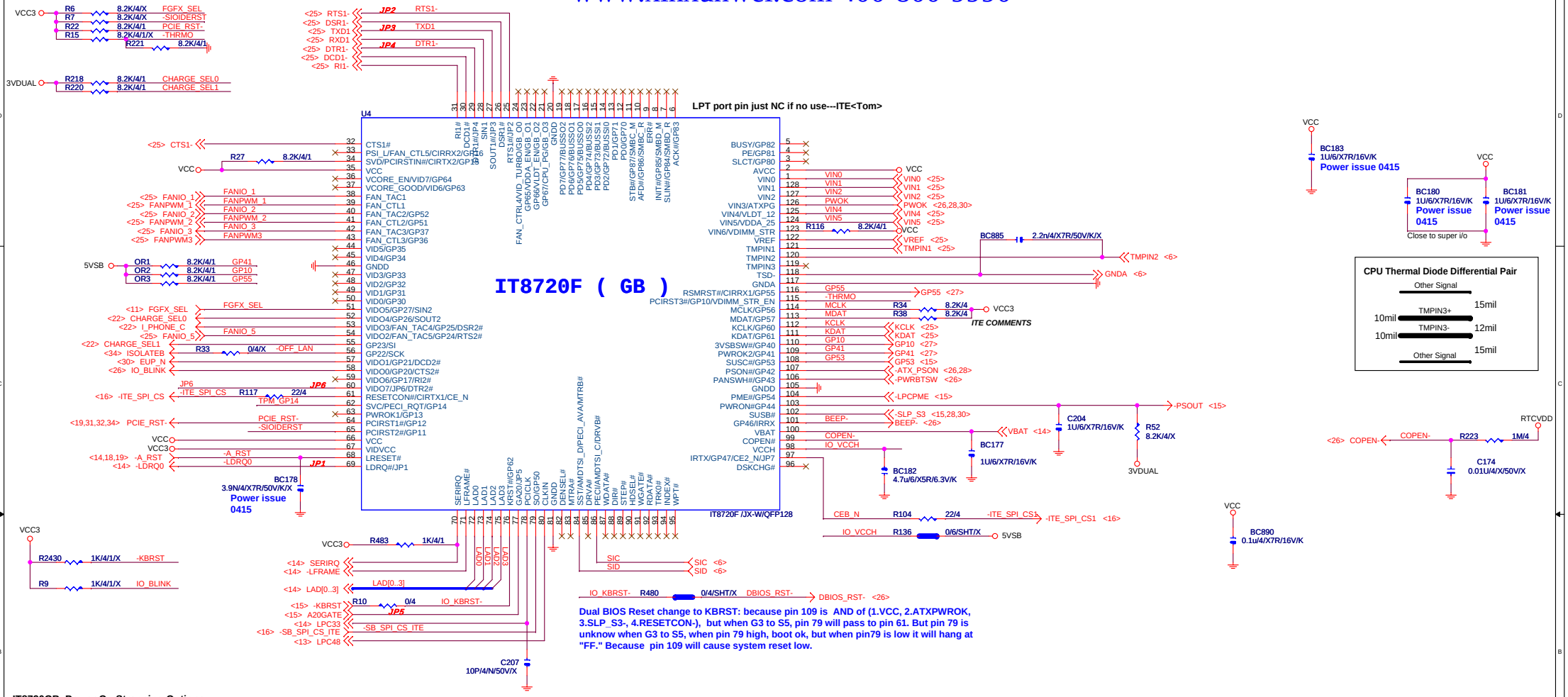
Date: Wednesday, July 20, 2011 Sheet 19 of 35

PCI SLOT 1,2



GIGABYTE™

Title	PCI SLOT 1,2,3	
Size: Custom	Document Number: GA-990XA-UD3	Rev: 1.1
Date: Wednesday, July 20, 2011	Sheet 20 of 35	



IT8720GB Power On Strapping Options

	Symbol	value	Description
JP1 Pin 69			
JP2 Pin 25	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 27	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 29	K8PWR_EN	1	K8 power sequence disabled
		0	K8 power sequence enabled
JP3 & JP5 Pin 27 & Pin 77	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5 Pin 77	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin 60	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function
JP7 Pin 97	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
		0	Disable Dual BIOS Function for GigaByte Only

GIGABYTE™

Title: ITE 8720 JX LPC IO ,Dual-BIOS ,TPM

Size	Document Number	Rev
Custom	GA-990XA-UD3	1.1

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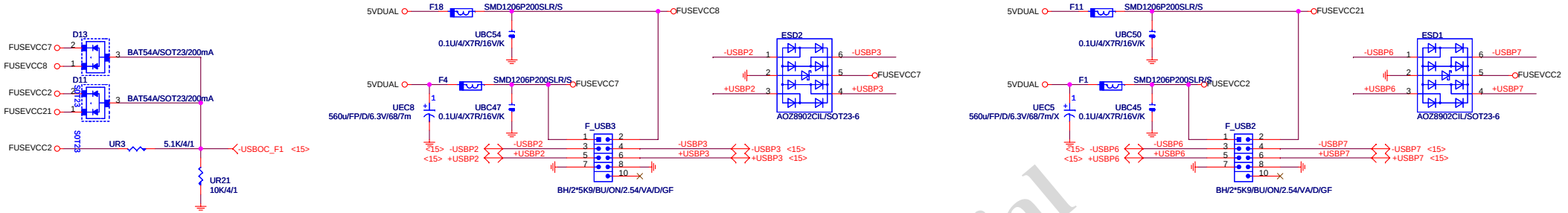
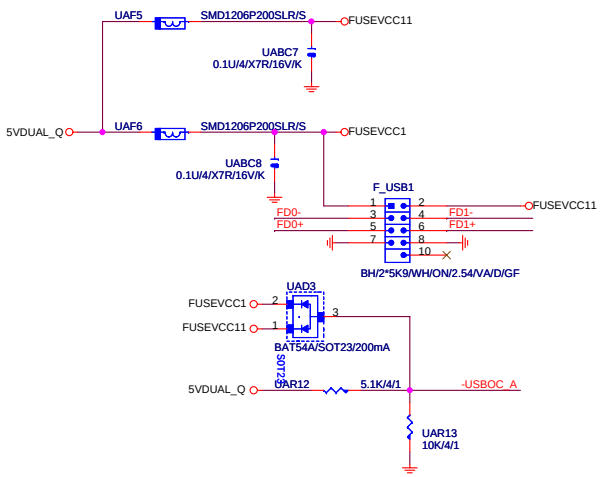
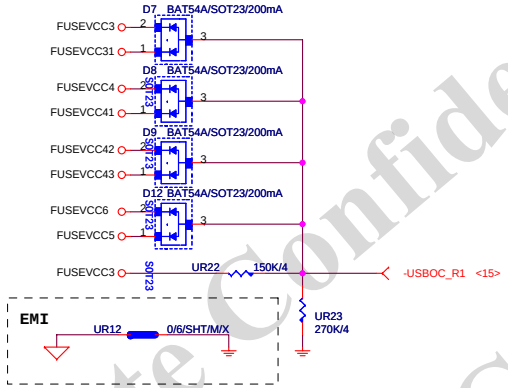
FRONT_SIDE_USB2

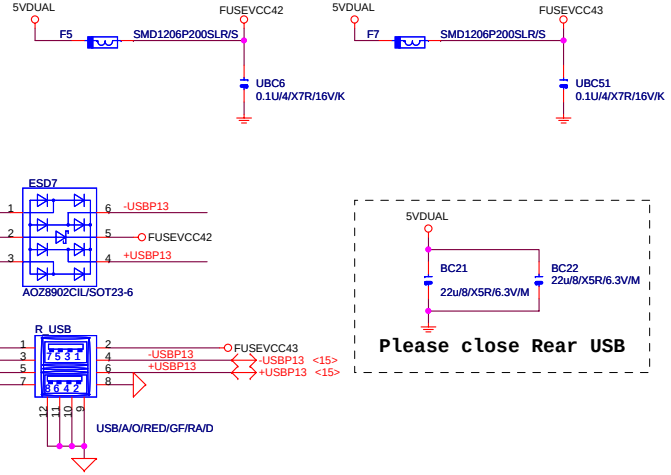


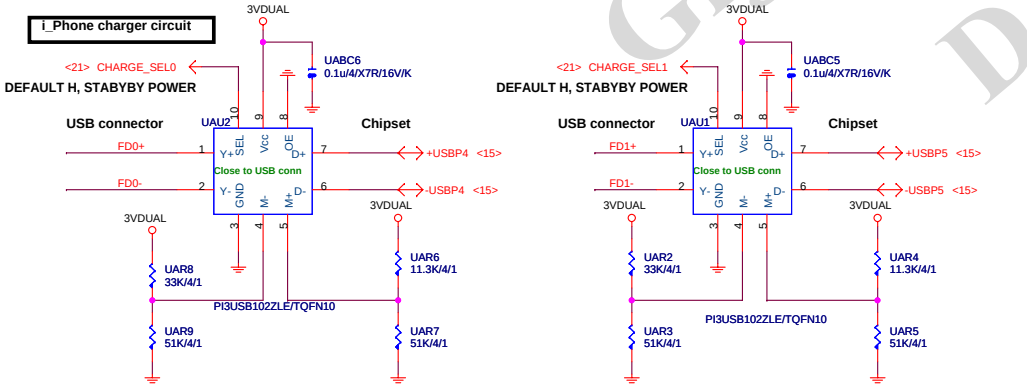
FRONT_SIDE_USB1

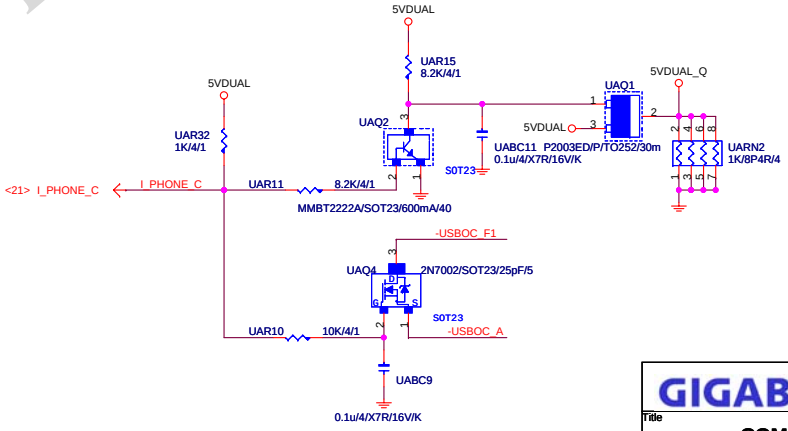




REAR_USB





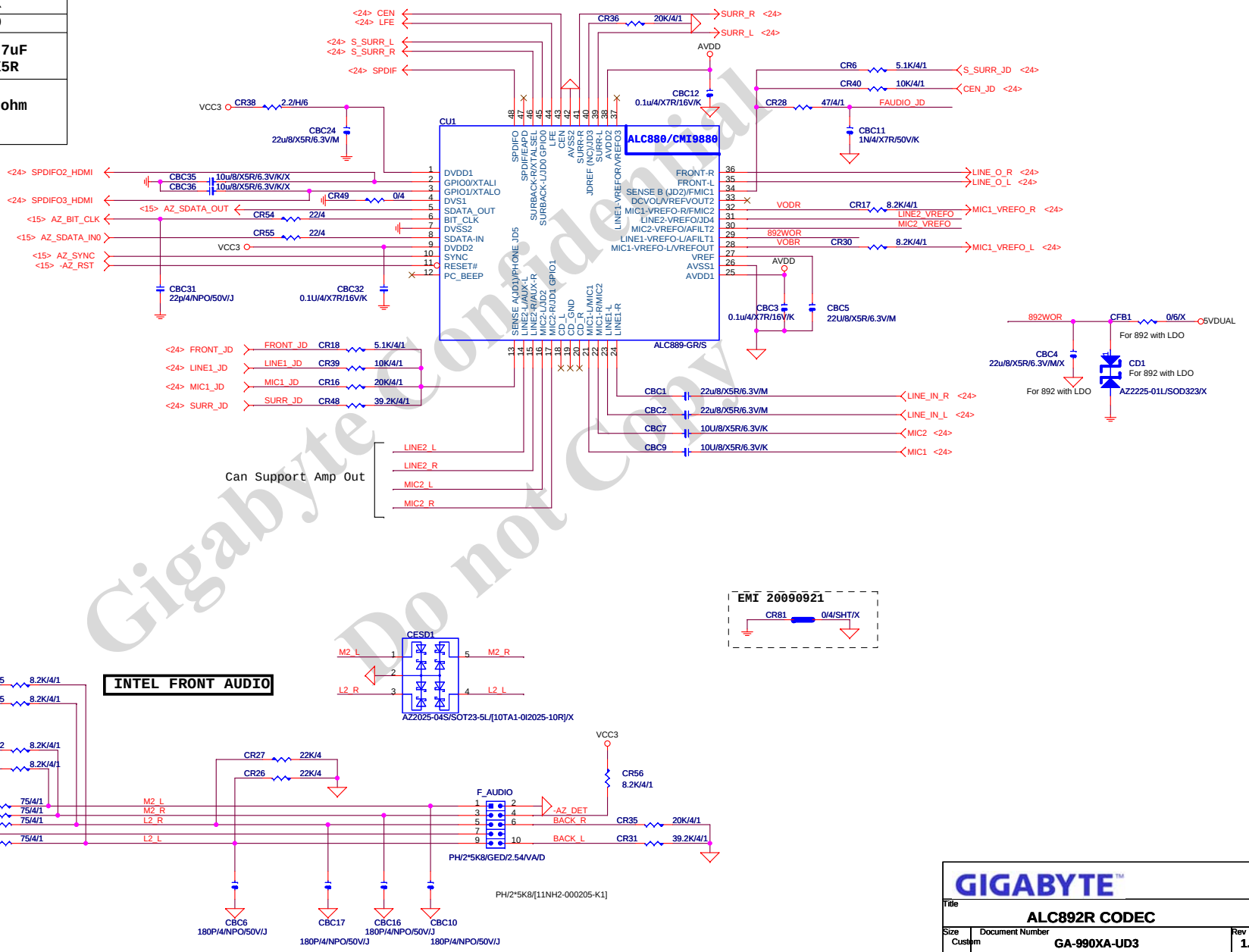


GIGABYTE™

Title	COM/LPT/F_USB/I_PWR	
Size: Custom	Document Number: GA-990XA-UD3	Rev: 1.1
Date: Wednesday, July 20, 2011	Sheet 22 of 35	

AZALIA CODEC *ALC892/ALC889/ Colay*

	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm



Title	ALC892R CODEC
Size	Custom
Document Number	GA-990XA-UD3
Rev	1.1
Date:	Wednesday, July 20, 2011
Sheet	23 of 35

CR33
0/6/SHT/X

+12V
AVDD
CQ3
CD3
CD4148WP/1206/300mA
78L05/SOT89/0.1A
5VDUAL
CD4
CD4148WP/1206/300mA
CBC8
22u/8/X5R/6.3V/M
CD2
AZ2225-01L/SOD323
CBC21
1U/6/X7R/16V/K

For ESD PROTECT DIODE

SPDIF

<23> SPDIFO3_HDMI — CR52 0/4/X
<23> SPDIFO2_HDMI — CR53 0/4
CBC37 100p/4/NPO/50V/J
SPDIF_O
SPDIF_O
PH/1*2/BK/2.54/VA/D

For HDMI SPDIF

FUSEVCC3
<23> SPDIF
SPDIF
OPTICAL
FR/5P/BK/T/D/S(GY)

CESD2
AJ_A2 — AJ_B2
AJ_C2 — AJ_C5
AZ2025-04S/SOT23-5L/[10TA1-0I2025-10R]/X

CESD3
AJ_B5 — AJ_A5
BJ_C2 — BJ_A2
AZ2025-04S/SOT23-5L/[10TA1-0I2025-10R]/X

CESD4
BJ_B5 — BJ_A5
BJ_C5 — BJ_B2
AZ2025-04S/SOT23-5L/[10TA1-0I2025-10R]/X

CESD5
SPDIF — SPDIF
SPDIF_O — SPDIF_O
AZ2025-04S/SOT23-5L/[10TA1-0I2025-10R]/X

For Audio precision test
CBC38 0.01u/4/X7R/25V/K

USB_LAN
R_USB2
R_USB1

AUDIOB
<23> LINE1_JD — LINE1_JD — AJ_A5 — AJ_A2 — A1 — GND — LINE-IN
<23> FRONT_JD — FRONT_JD — AJ_B5 — AJ_B2 — B1 — GND — LINE-OUT
<23> MIC1_JD — MIC1_JD — AJ_C5 — AJ_C2 — C1 — GND — MIC-IN

BLUE LINE-IN
GREEN LINE-OUT
PINK MIC-IN

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

AUDIOA
<23> CEN_JD — CEN_JD — BJ_B5 — BJ_B2 — D1 — GND — REAR
<23> SURR_JD — SURR_JD — BJ_C5 — BJ_C2 — E1 — GND — CEN
<23> S_SURR_JD — S_SURR_JD — BJ_A5 — BJ_A2 — F1 — GND — SIDE

Orange CEN/LFE
ALC880 - SURROUND
CMI9880 - Back SURR
Black Back Side Speaker Azalia Port G
Gray Left & Right Side Speaker
CMI9880 - Side SURR

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

A3RJ/13P/B/[11NR6-403006-01_11NR6-403006-02]
3RJ+15F/[11NR6-403004-11]

A3RJ/13P/OBG/[11NR6-403006-71]
3RJ+15F/[11NR6-403004-31]

LINE OUT FRONT OUT

<23> LINE_O_R — CEC2 100u/OS/D/16V/66/24m — CR7 62/4 — AJ_B5
<23> LINE_O_L — CEC3 100u/OS/D/16V/66/24m — CR9 62/4 — AJ_B2
CR10 22K/4 — CBC23 180P/4/NPO/50V/J — CR8 22K/4 — CBC26 180P/4/NPO/50V/J

LINE-IN

<23> LINE_IN_R — CR5 62/4 — AJ_A5
<23> LINE_IN_L — CR13 62/4 — AJ_A2
CBC18 180P/4/NPO/50V/J — CBC27 180P/4/NPO/50V/J

MIC

<23> MIC2 — CR29 62/4 — AJ_C5
<23> MIC1 — CR32 62/4 — AJ_C2
<23> MIC1_VREFO_R — CR37 0/4/SHT/X
<23> MIC1_VREFO_L — CR34 0/4/SHT/X
CBC19 180P/4/NPO/50V/J — CBC22 180P/4/NPO/50V/J

SURROUND

<23> SURR_R — CEC5 100u/OS/D/16V/66/24m — CR46 62/4 — BJ_C5
<23> SURR_L — CEC7 100u/OS/D/16V/66/24m — CR19 62/4 — BJ_C2
CR20 22K/4 — CBC29 180P/4/NPO/50V/J — CR45 22K/4 — CBC28 180P/4/NPO/50V/J

CEN/LFE

<23> LFE — CEC9 100u/OS/D/16V/66/24m — CR50 62/4 — BJ_B5
<23> CEN — CEC10 100u/OS/D/16V/66/24m — CR41 62/4 — BJ_B2
CR42 22K/4 — CBC25 180P/4/NPO/50V/J — CR51 22K/4 — CBC34 180P/4/NPO/50V/J

SURR BACK

<23> S_SURR_R — CEC8 100u/OS/D/16V/66/24m — CR21 62/4 — BJ_A5
<23> S_SURR_L — CEC4 100u/OS/D/16V/66/24m — CR47 62/4 — BJ_A2
CR43 22K/4 — CBC33 180P/4/NPO/50V/J — CR22 22K/4 — CBC30 180P/4/NPO/50V/J

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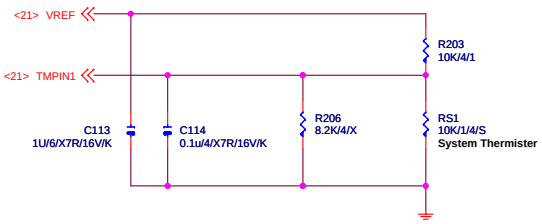
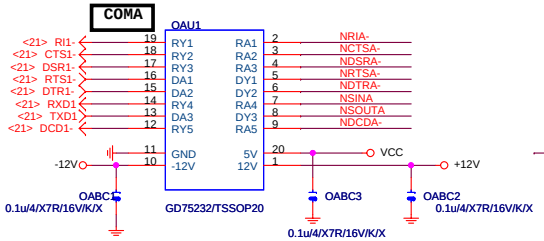
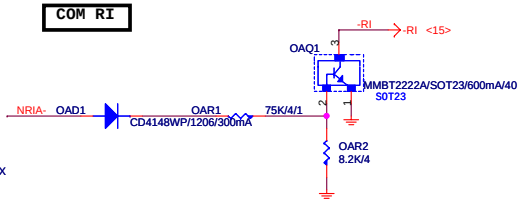
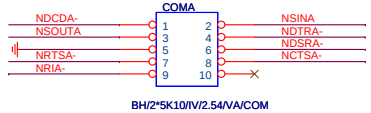
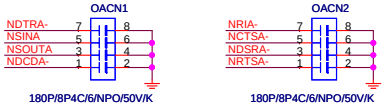
Hardware Monitor circuits



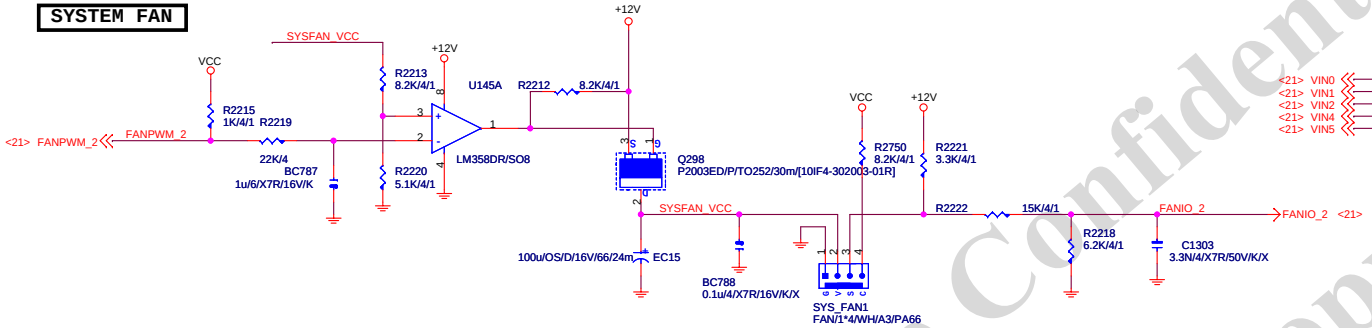


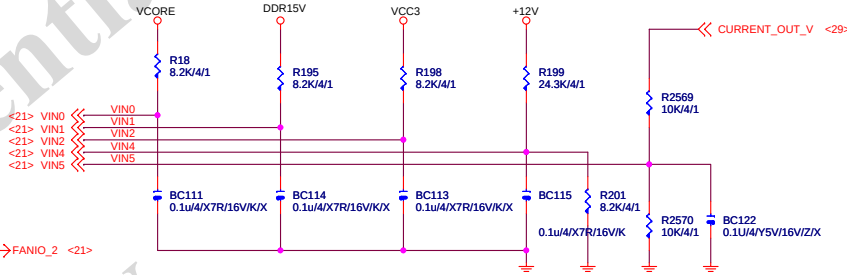




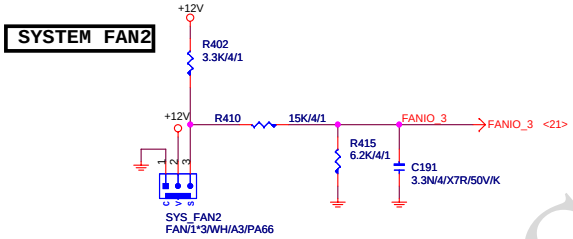


SYSTEM FAN

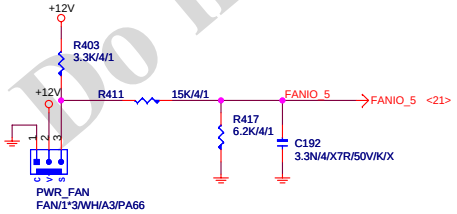




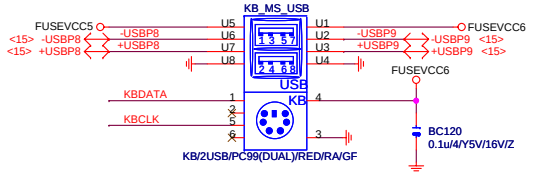
SYSTEM FAN2

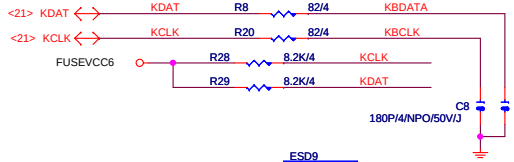


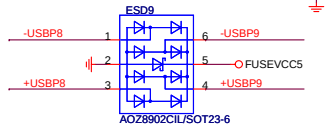
POWER FAN



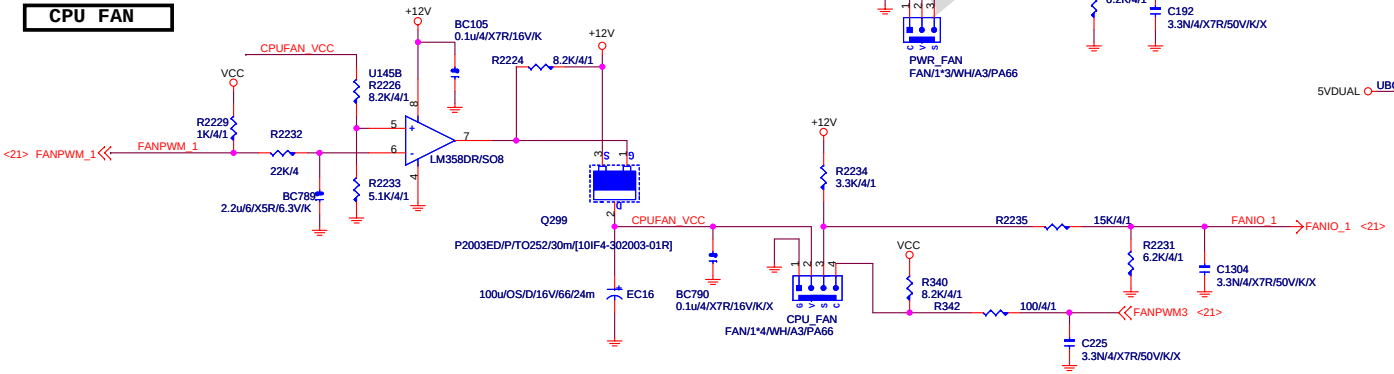
KB & USB







CPU FAN



5VDUAL UBC53 0.1U/4/X7R/16V/K

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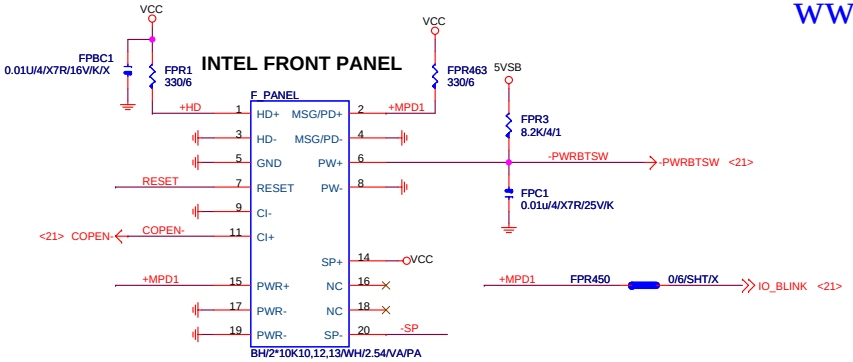
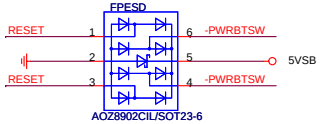
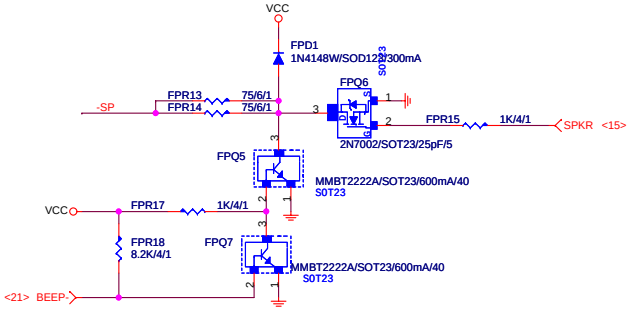
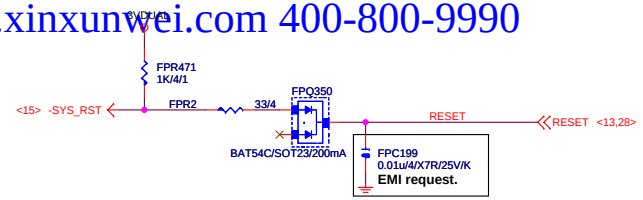
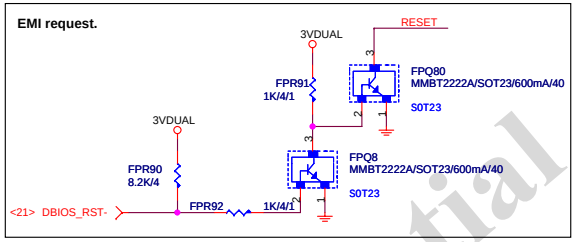
INTEL FRONT PANEL

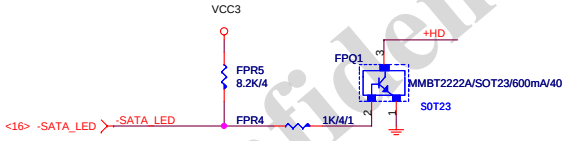


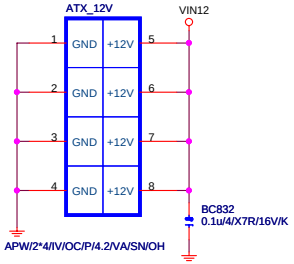


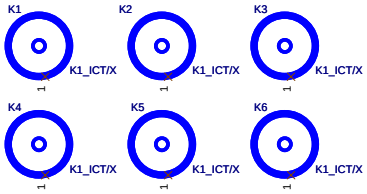


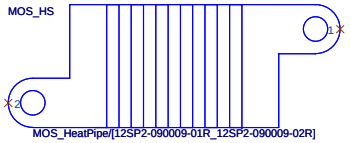




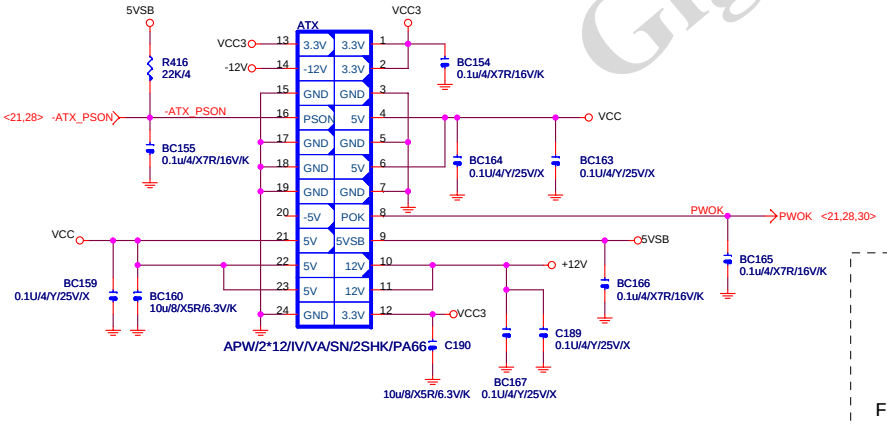


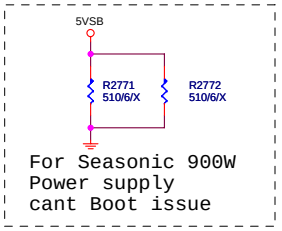


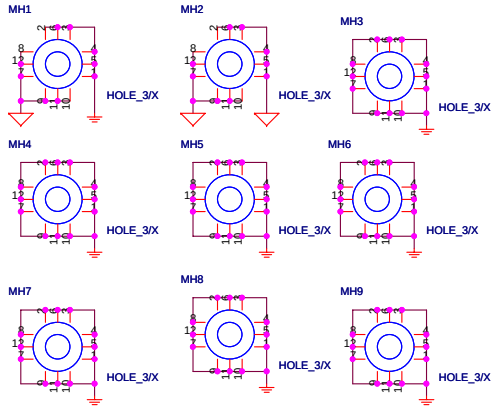




ATX POWER CONNECTOR







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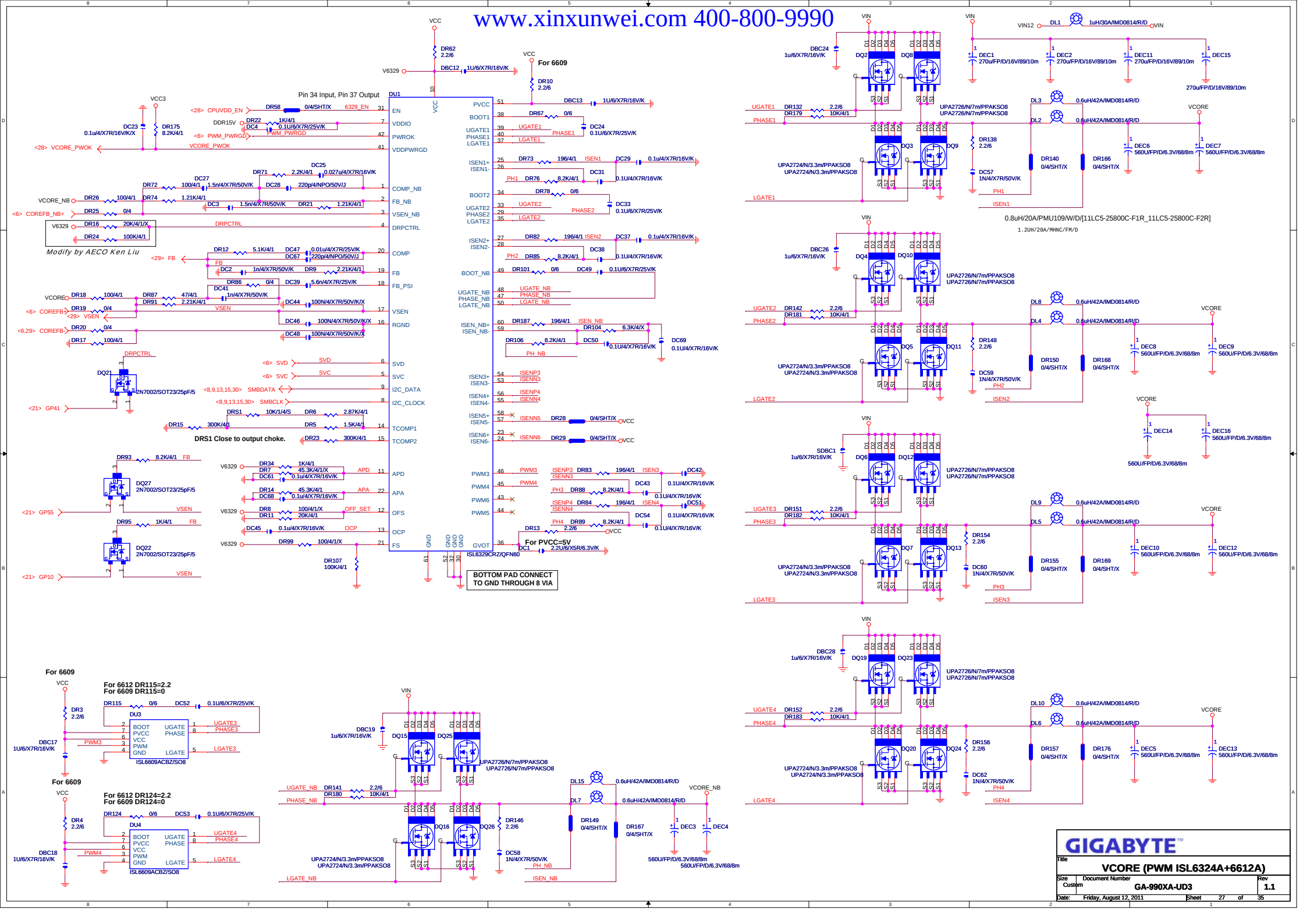
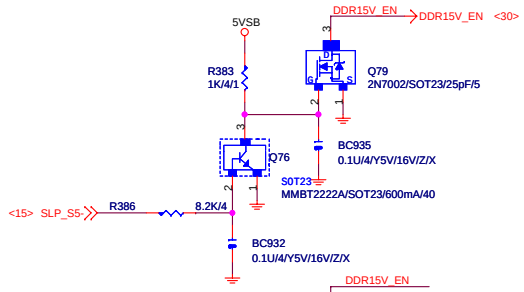
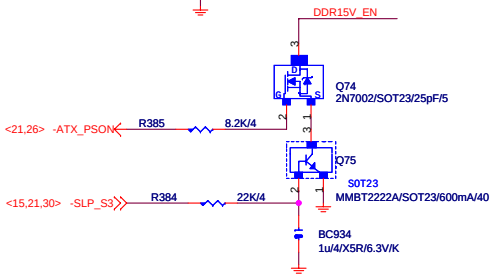
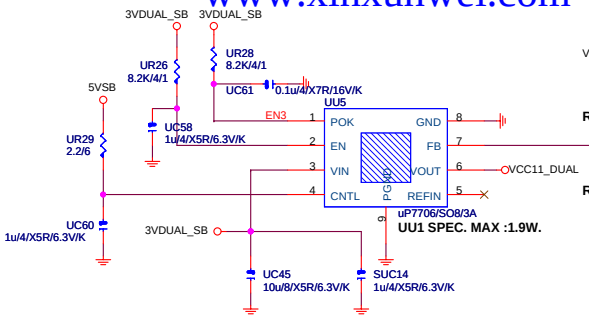
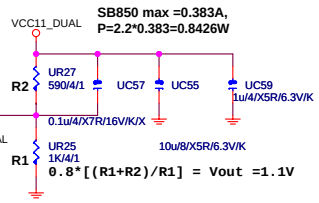
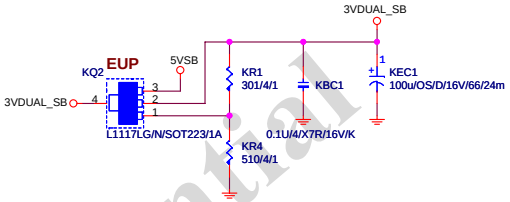


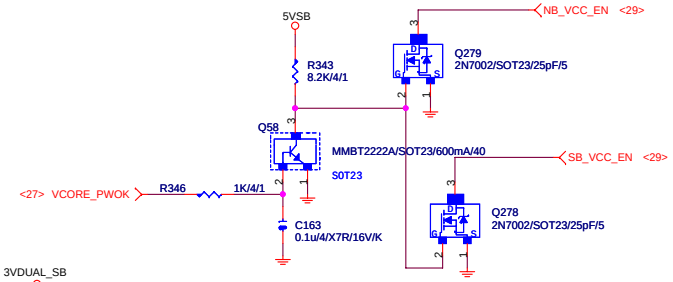


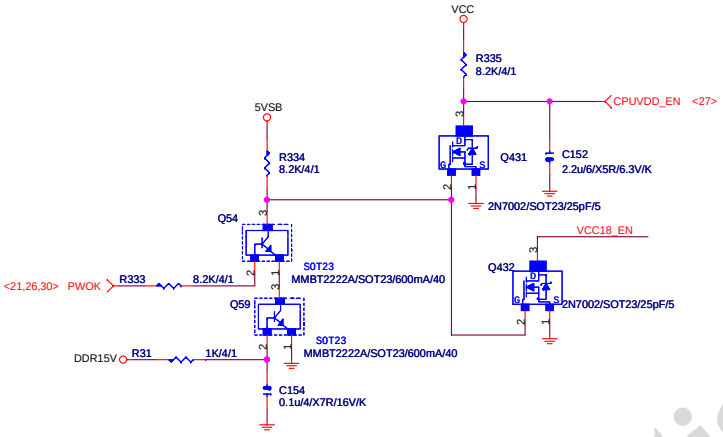




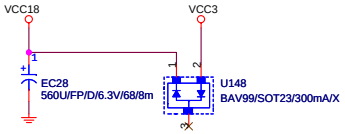


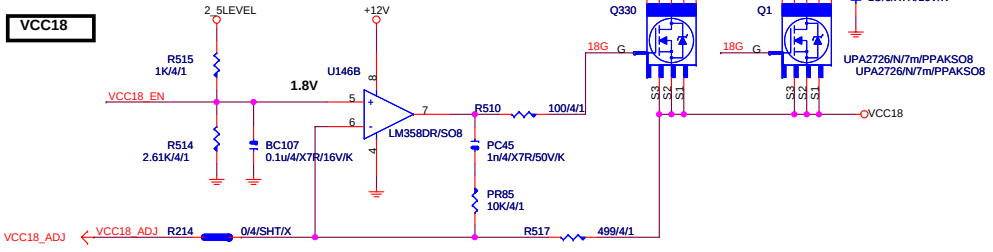


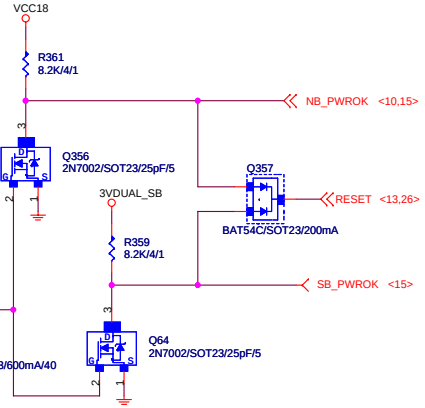


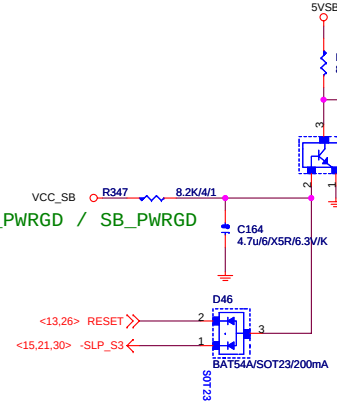


ATI for VCC3/VCC18 power ramp-up 2.1V









PWOK > NB_PWRGD / SB_PWRGD

(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms

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Title: POWER SEQUENCE ,VCC18 ,EUP

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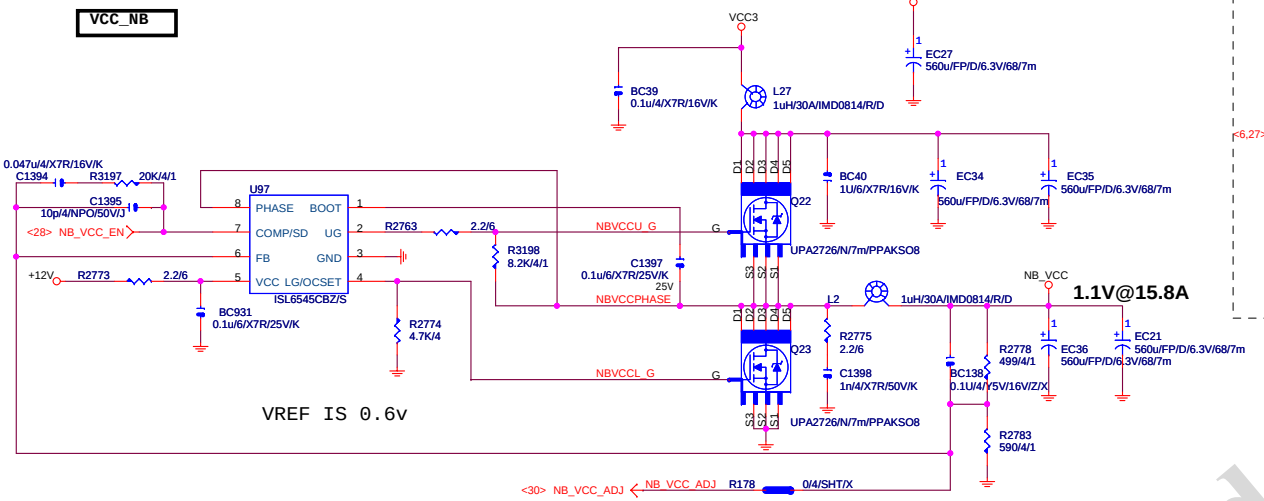
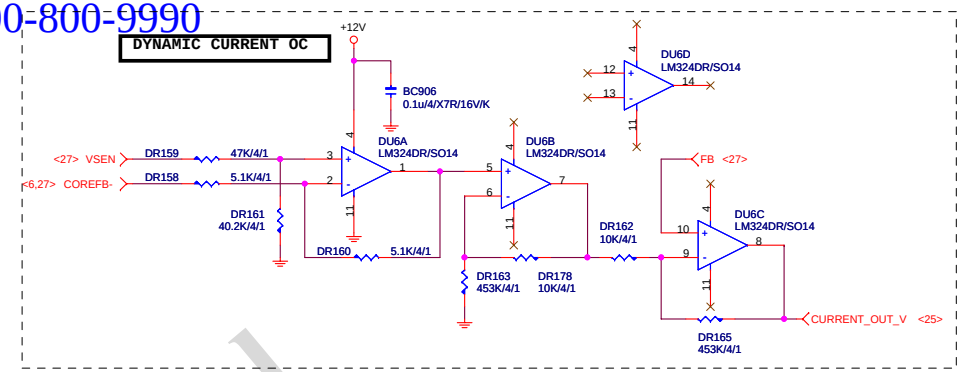
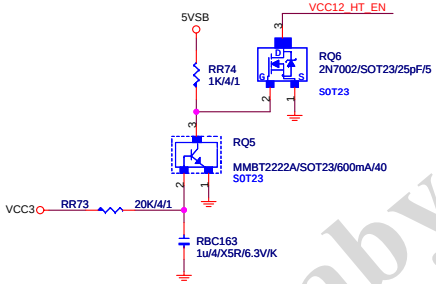
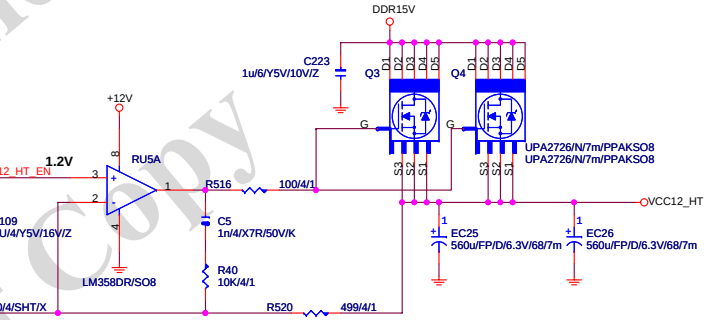


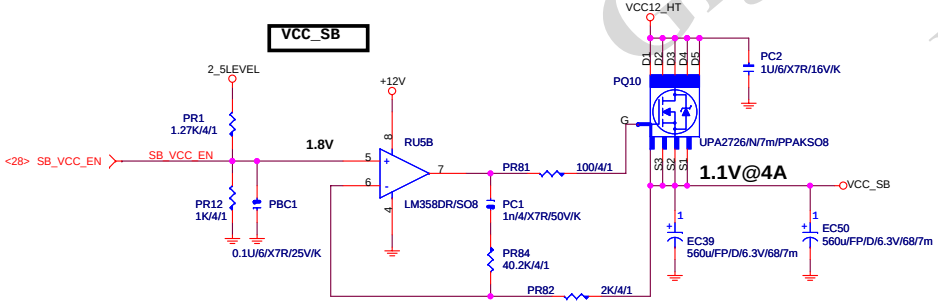


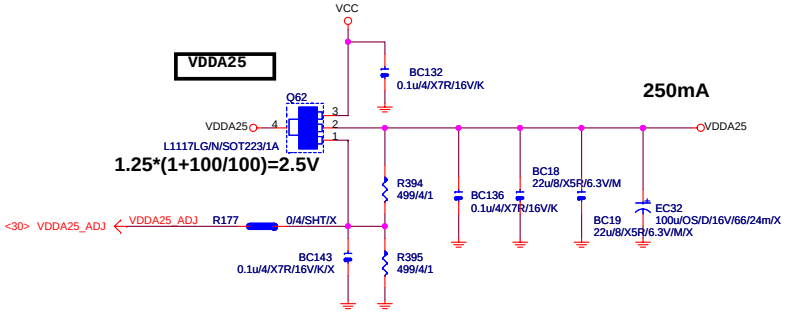
Default change to 1.15V

Patch AMD Validation
VDDA25 & VCC12_HT
power sequence









GIGABYTE™

Title	NB/SB POWER,VCC12HT,VDDA25,VCC12Dual	
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R2038不能上,會導致LM324 PIN1不能完全拉Lo

5VDUAL

9.5V / 25A protect

9.5*(1.21K/(13.3K+1.21K))=0.792V

3VDUAL

1.25*(1+169/100)=3.36V

EUP

0x2A

0X20 = 100% xVCC

1.5V@20A

Default: 1.5V, from AMD

0.6*(1+1.5K/1K)=1.5V

VREF IS 0.6V

4 VIA to GND

GIGABYTE

Title: DDR POWER

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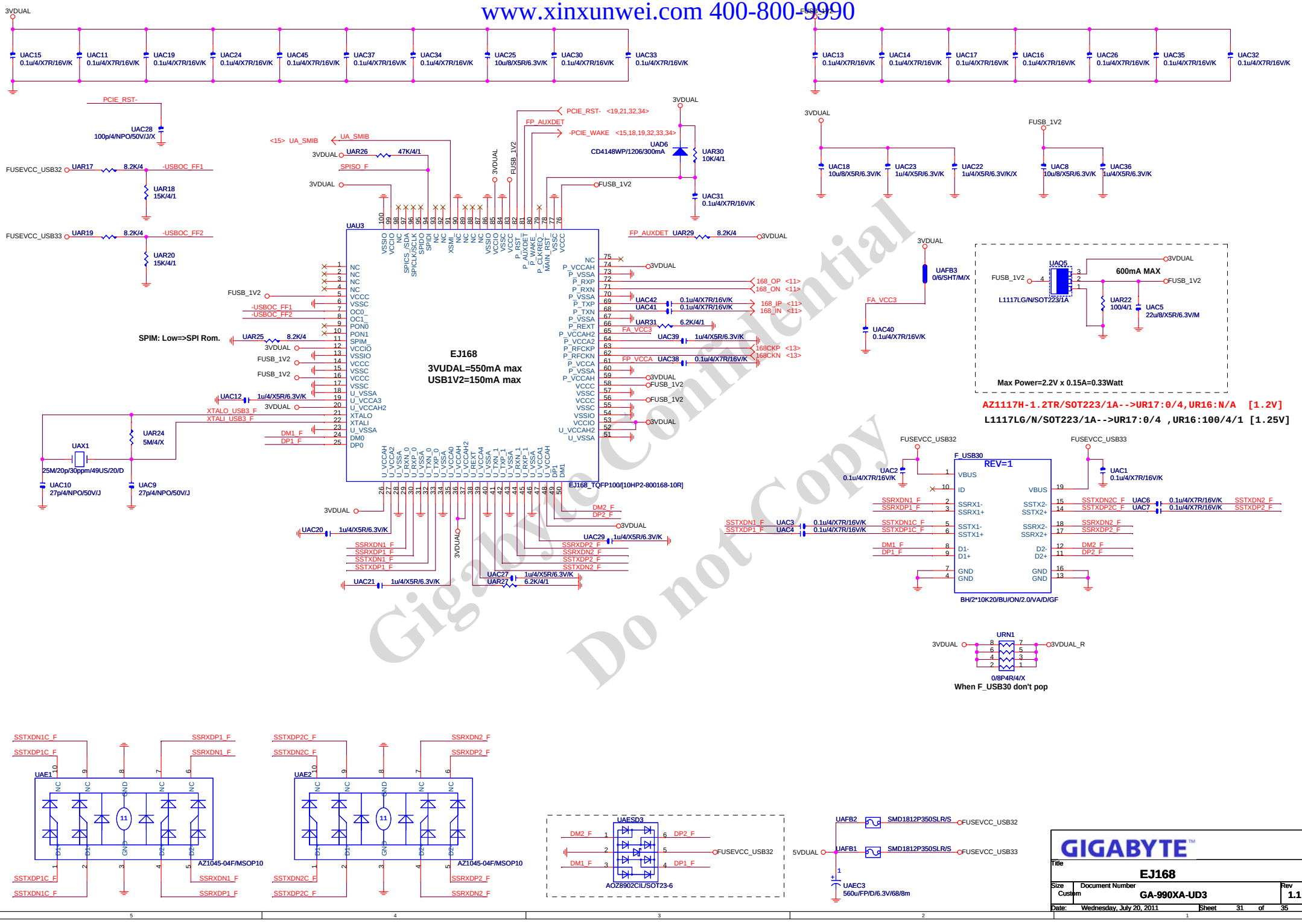

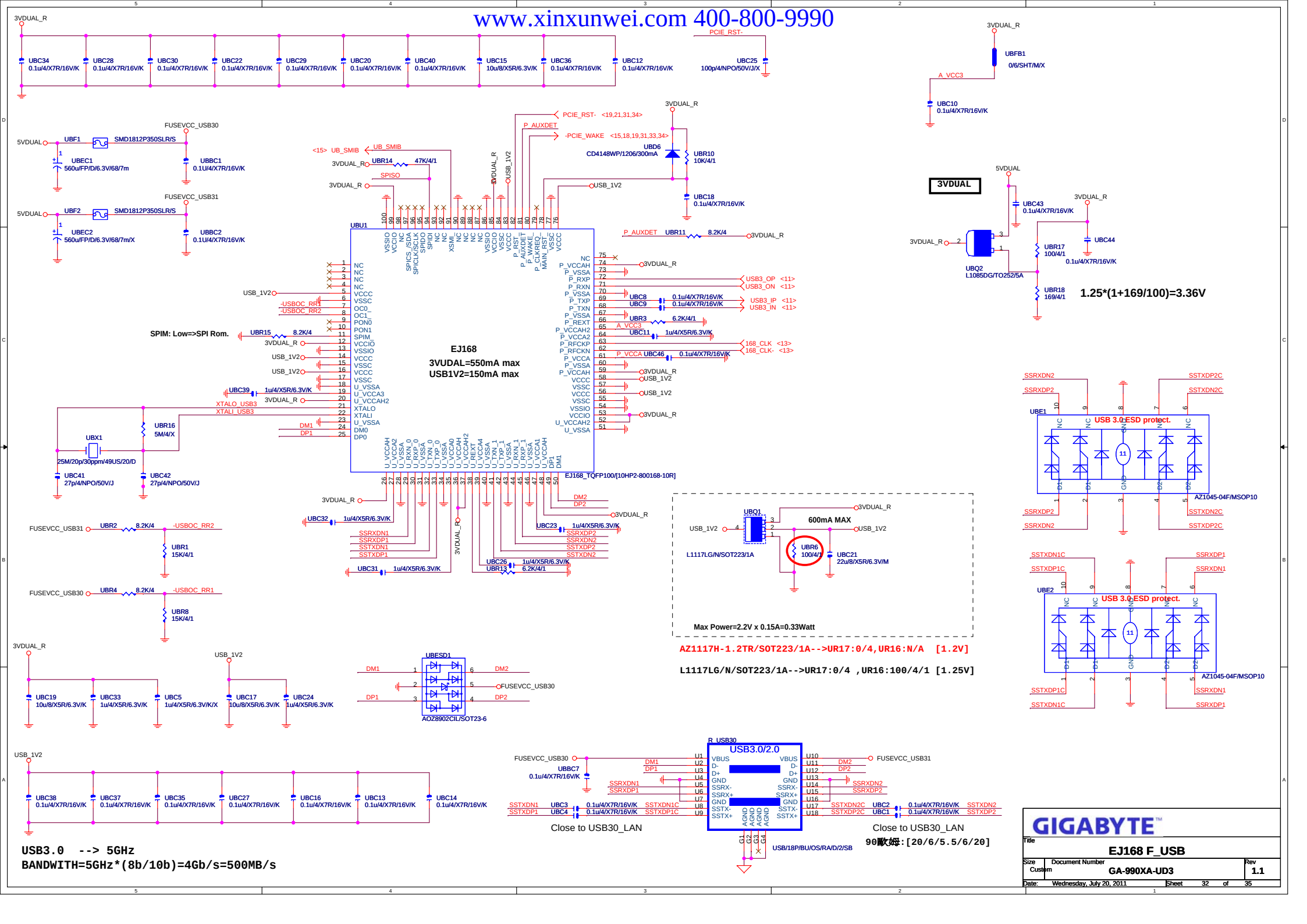

Title	EJ168 F_USB
Size	Custom
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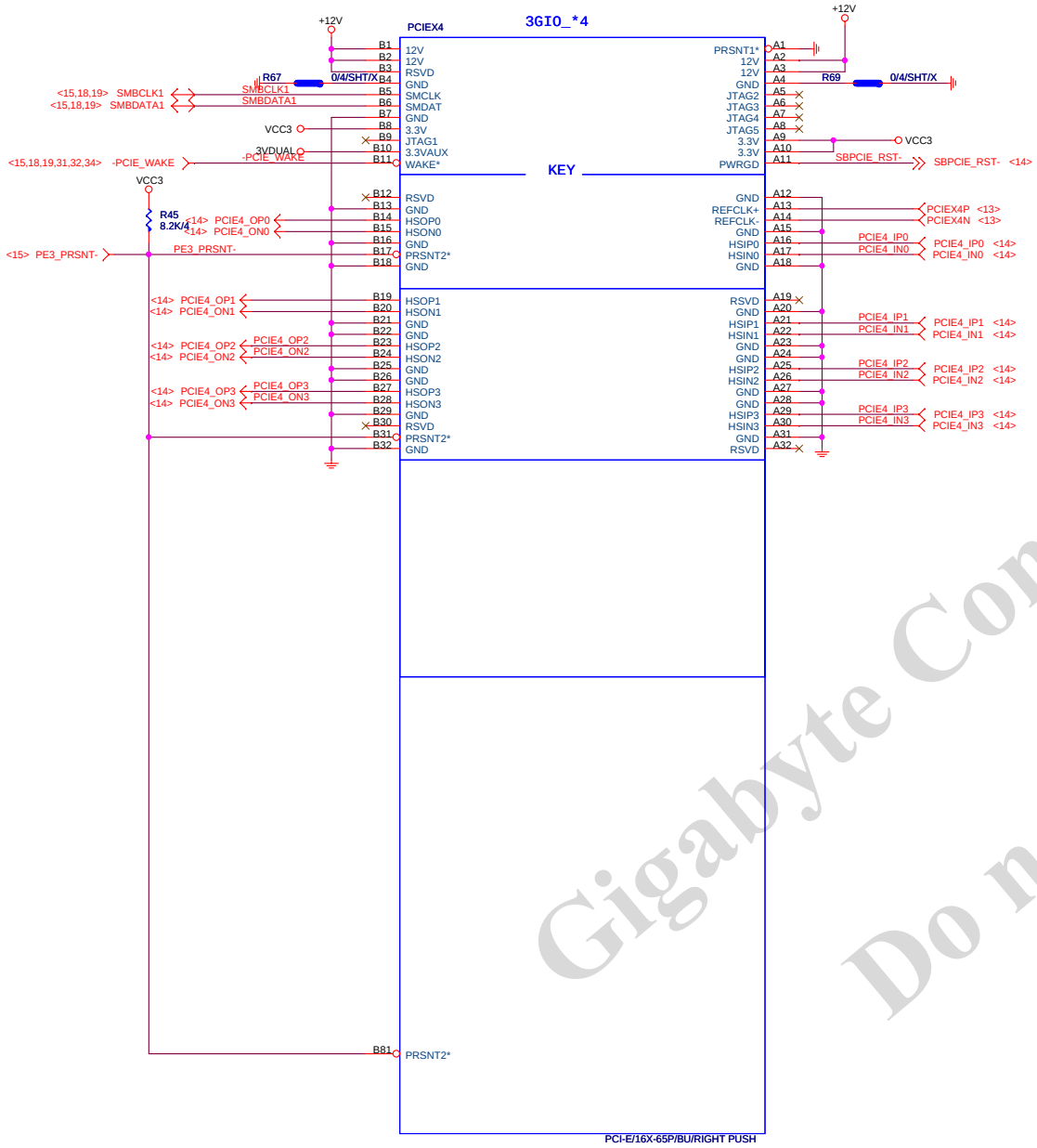

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Title: JMB362		
Size: Custom	Document Number: GA-990XA-UD3	Rev: 1.1
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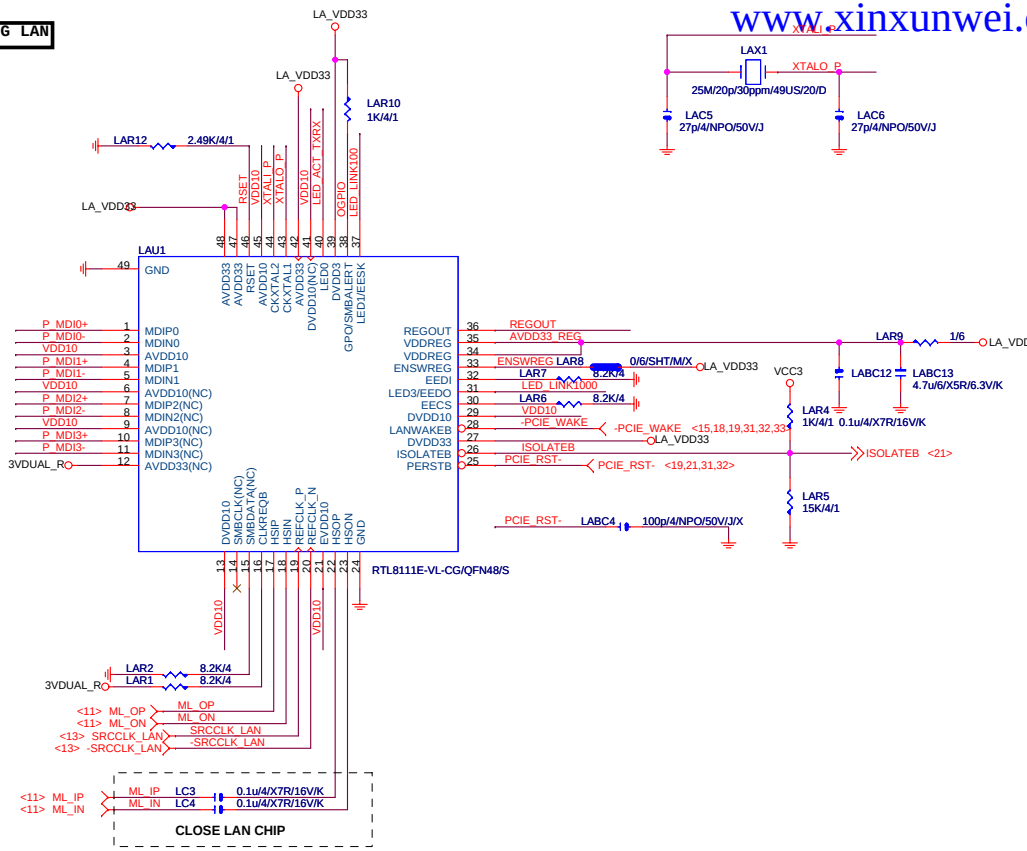
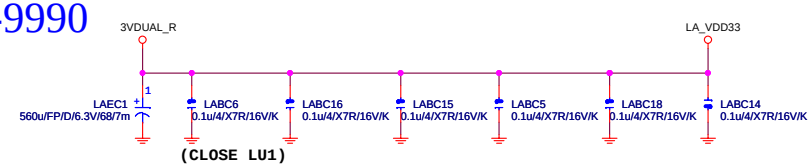
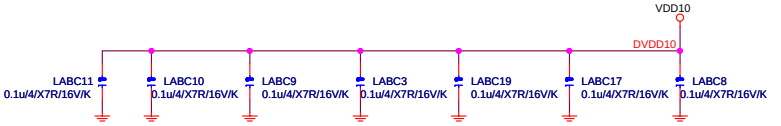
PCIE-1G LAN

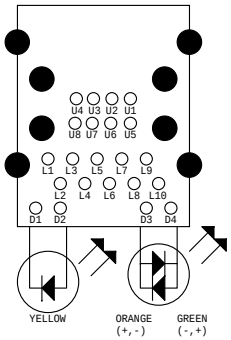


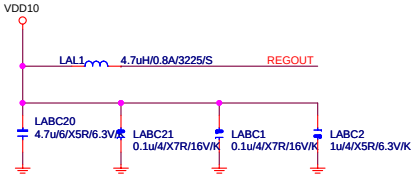




USB_LAN CONNECTOR

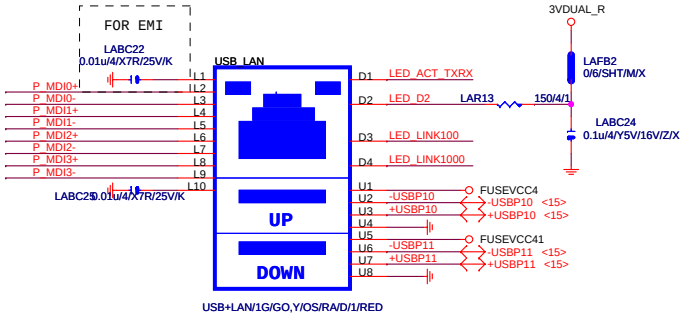
P35-152-19W9

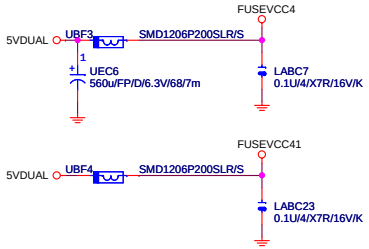


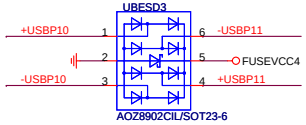


USB_LAN

RTL8101E:LR38/LC5/LR43/LC6-->O
RTL8111C:LC6-->O
RTL8102E:LC5/LC6-->O

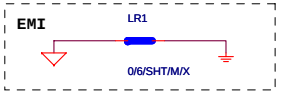






RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)

1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1



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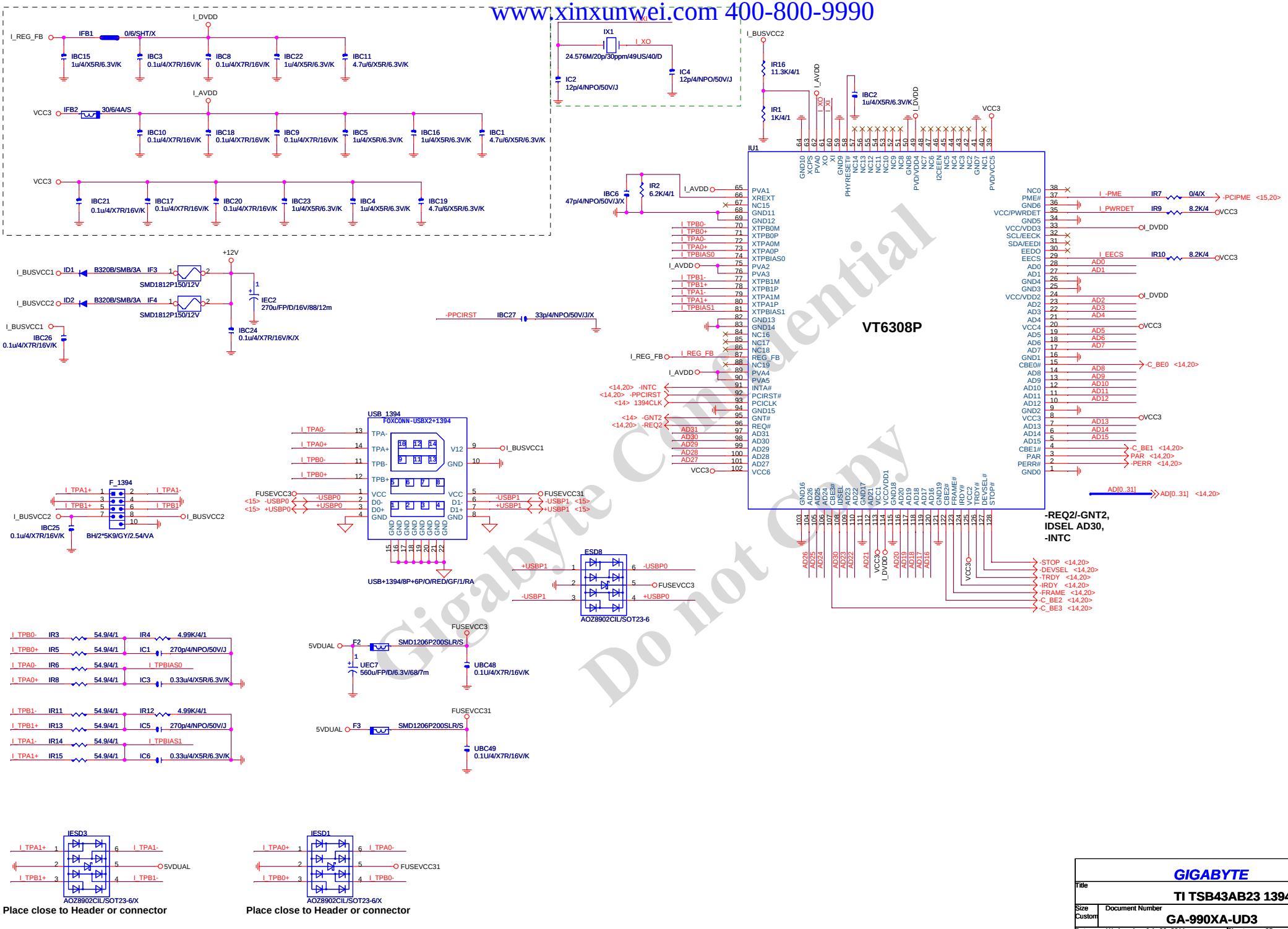

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Date: Wednesday, July 20, 2011	Sheet 35 of 35	