GA-990XA-UD3

Revision : 3.04

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Title: COVER SHEET		
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Model Name:GA-990XA-UD3

Component value change history

Version: 3.04

4 Layer, 4mil 50ohm +/- 15% L

P-Code: U98094-0

Date	Change Item	Reason
2011.03.04	0.1 New BOM Release. PCB Ver 0.1	
2011.04.12	1.0A E- BOM Release. PCB Ver 1.0	
2011.04.21	1.0B P- BOM Release. PCB Ver:1.0	R333 => 8.2K to fix backup BIOS can't show with ACBEL atx-350cn-an6fb.
		Add PR26=>22 for TPM. Change SB heatsink
2011.04.25	1.0C P- BOM Release. PCB Ver:1.01	Only remove SLI Logo
2011.04.29	1.0D P- BOM Release. PCB Ver:1.01	DDR3_4 and DDR3_1 Part NO. change
2011.06.09	1.0F MP BOM Release. PCB Ver:1.0	BC933 --> 1uF PCB Change to 1.0 w/SLI Logo
2011.07.22	11A BOM Release(DVT). PCB Ver:1.1	Add Load-Line Droop control
2011.08.15	11B P-BOM Release(SKIP PVT). PCB Ver:1.1	change Load-Line Droop 阻值 DR73,DR82,DR83,DR84 from 150 change 196 ohm
2011.09.09	12A P-BOM Release PCB Ver:1.2(註2)	change NB Chipset from 10HB1-06D980-10R to 10HB1-06D990-10R (註1) (註1) fix post code 94 at high temperature issue (註2) PCB is Ver1.1,but use leable to Ver 1.2
2011.09.14	13A P-BOM Release PCB Ver:1.3	PCB is Ver1.1, but use leable to Ver 1.3
2011.09.22	14A P-BOM Release PCB Ver:1.11	Add NBGFX1_CLKP/NBGFX1_CLKN(R1/R5)
2012.01.09	11F P-BOM Release PCB Ver:1.11	1. RTL8111E-VL change to RTL8111F-VL 2. RT9173 change RT9199
2012.04.17	11H E-BOM Release PCB Ver:1.12	Add MOS Thermal Protection circuit.
2012.05.04	11I P-BOM Release PCB Ver:1.12	change R156 from 1.5K to 2.32K
2012.08.22	30B E-BOM Release PCB Ver:3.01	change IT8728F IO; Add Patch some PSU can't boot when ERP enable.
2012.10.22	30C E-BOM Release PCB Ver:3.02	Add EC29,DEC15,C1638,C1639,C1676,EC173,C150,C151 ,OBC25,C1626,C1627,C1628,
2012.11.14	30D P-BOM Release PCB Ver:3.03	Add EC30
2012.12.19	30E P-BOM Release PCB Ver:3.03	11NR6-702009-0ER改爲11NR6-702009-96R(USB_LAN)
2013.11.01	30F P-BOM Release PCB Ver:3.03	Modify PPAKSO-8 mosfet P/N DQ9,DQ24,DQ26,DQ5,DQ7,DQ16,DQ11,DQ3,DQ13,DQ20: 10IF9-040012-10R/10IF9-040393-21R ~~/10IF9-040406-10R/10IF9-040393-01R~~ Q3,Q4,PQ10,DQ15,Q25,Q28,DQ23,Q22,Q27,DQ25,DQ10,DQ19 ,DQ2,Q26:10IF9-070428-01R/10IF9-100397-21R /10IF9-070410-00R/10IF9-100397-01R
2014.07.05	30G P-BOM Release PCB Ver:3.04	remove SATA MLCC

Circuit or PCB layout change for next version

Date	Change Item	Reason
2011.03.03	0.1 Gerber out	Modify from GA-890XA-UD3 2.1
2011.04.08	1.0 Gerber out	PWM GVOT ADD VCC PULL UP.
		Add Thermal Diode for AM3 CPU.
2011.04.25	1.01 Gerber out	Only remove SLI Logo
2011.07.20	1.1 Gerber out	Add CPU loadline control circuit.
2011.09.09		PCB is Ver1.1,but use leable to Ver 1.2
2011.09.14		PCB is Ver1.1,but use leable to Ver 1.3
2011.09.21	1.11 Gerber out	PCB Modify from 1.1 TO 1.11 Fix debug card show 94 in High temperature
2012.04.17	1.12 Gerber out	Add MOS Thermal Protection circuit.
2012.08.21	3.01 Gerber out	change IO IT8728F; Add circuit Patch some PSU can't boot when ERP enable.
2012.10.19	3.02 Gerber out	Add EC29,DEC15,C1638,C1639,C1676 for fix 3D06 restart issue
2012.11.01	3.03 Gerber out	Add EC30
2014.07.05	3.04 Gerber out	remove SATA MLCC

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Title: BOM & PCB HISTORY

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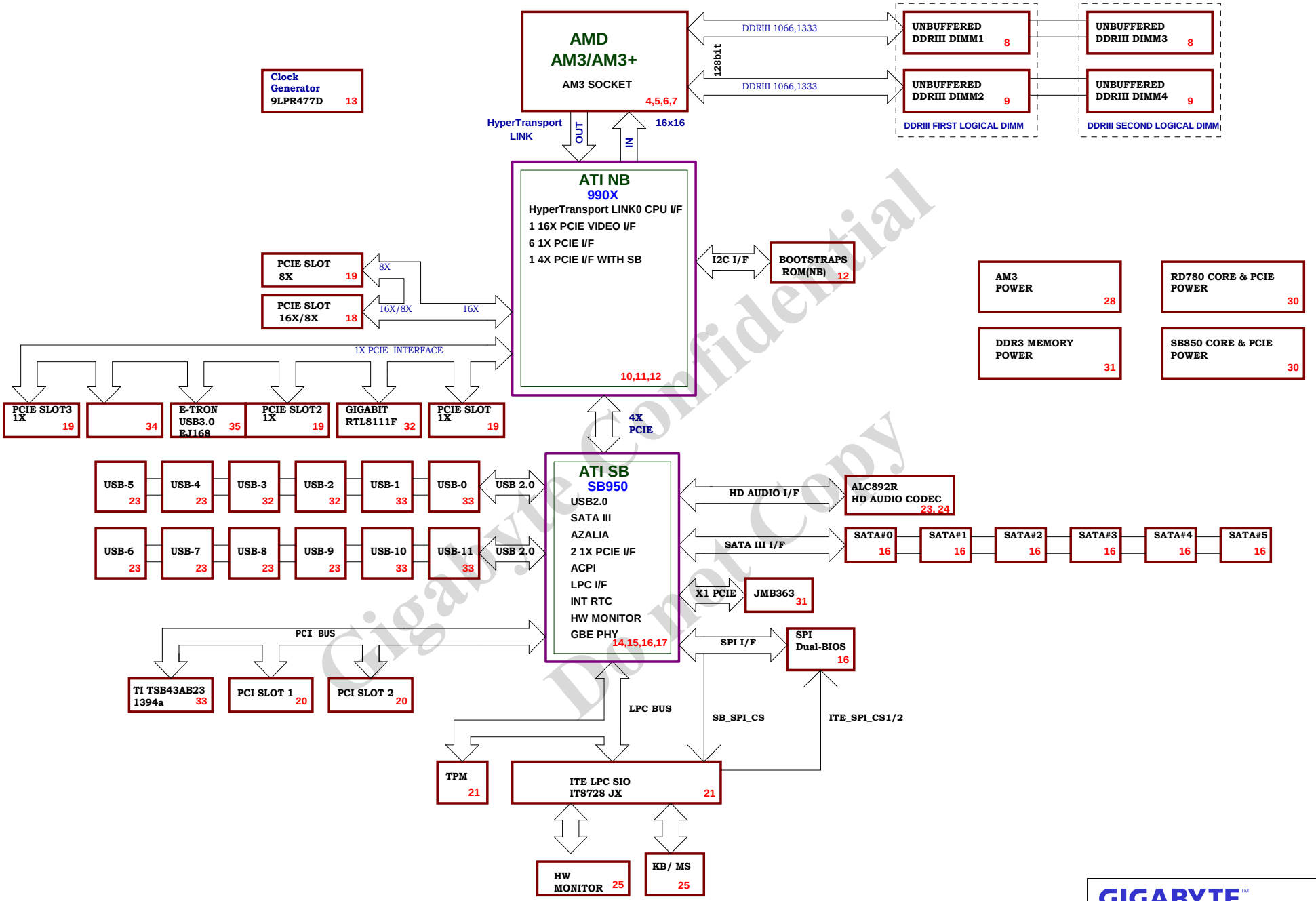

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Title: BLOCK DIAGRAM

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CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

L0_CADIN_L[0..15] L0_CADIN_L[0..15] <10>
L0_CADIN_H[0..15] L0_CADIN_H[0..15] <10>
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] <10>
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] <10>

M2CPUA
HYPERTRANSPORT

<10> L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 <10>
<10> L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 <10>
<10> L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 <10>
<10> L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 <10>
<10> L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 <10>
<10> L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 <10>
<10> L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 <10>
<10> L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 <10>
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/941AM3/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

COUPON1 COUPON1 1 2 COUPON/X VCC
COUPON2 COUPON2 1 2 COUPON/X

M2CPU
AM3RM/SC/BL/MB/[12KRC-04K812-31R]

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Title	CPU HYPER TRANSPORT		
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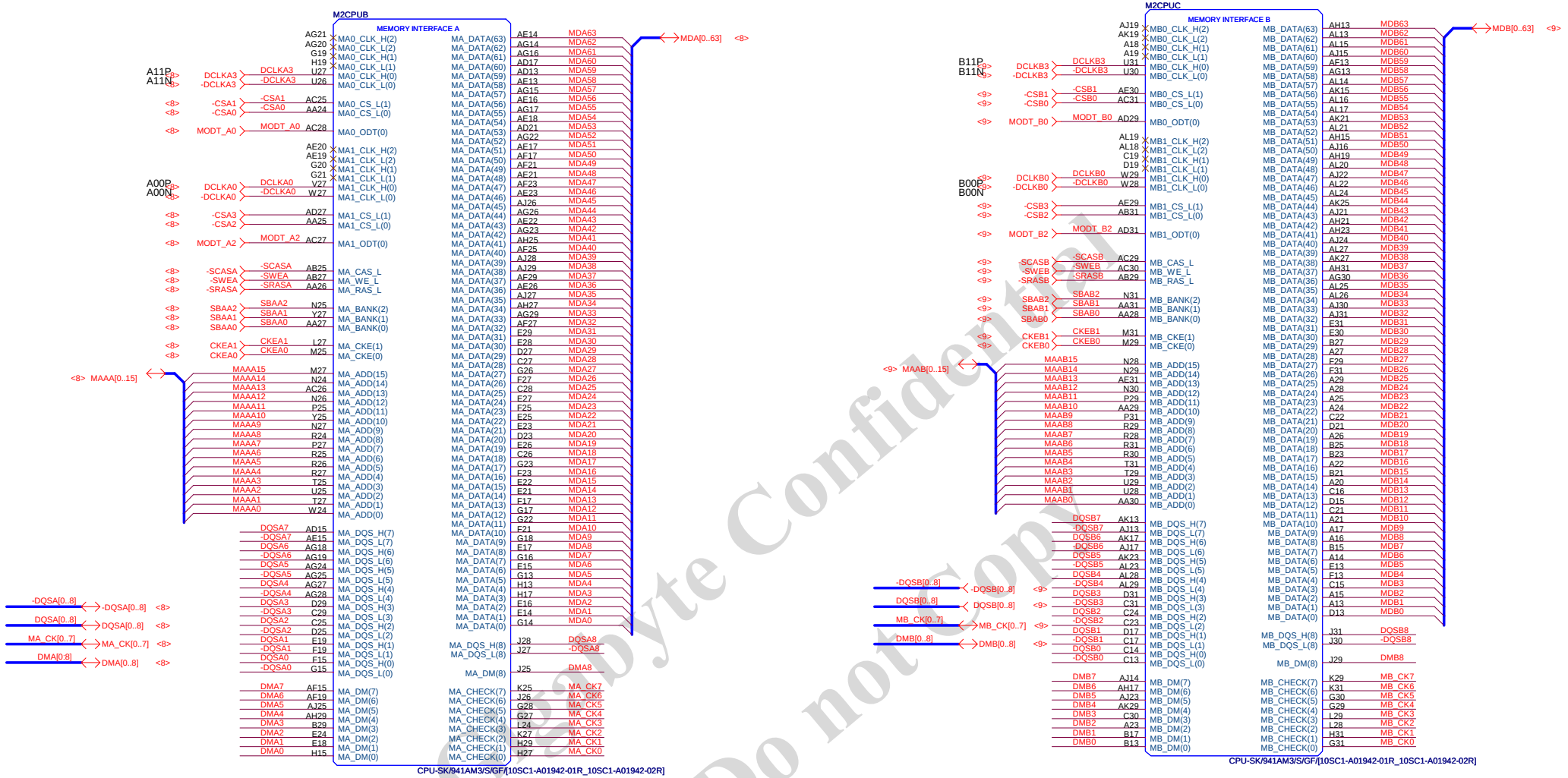

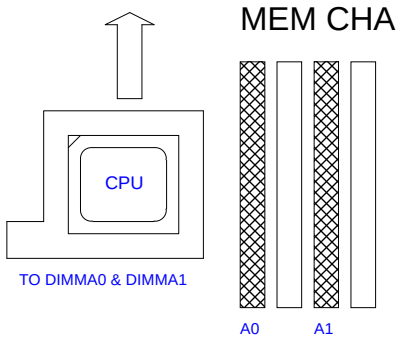

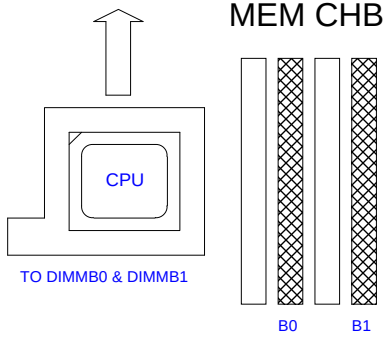

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Title	CPU DDRIII MEMORY	
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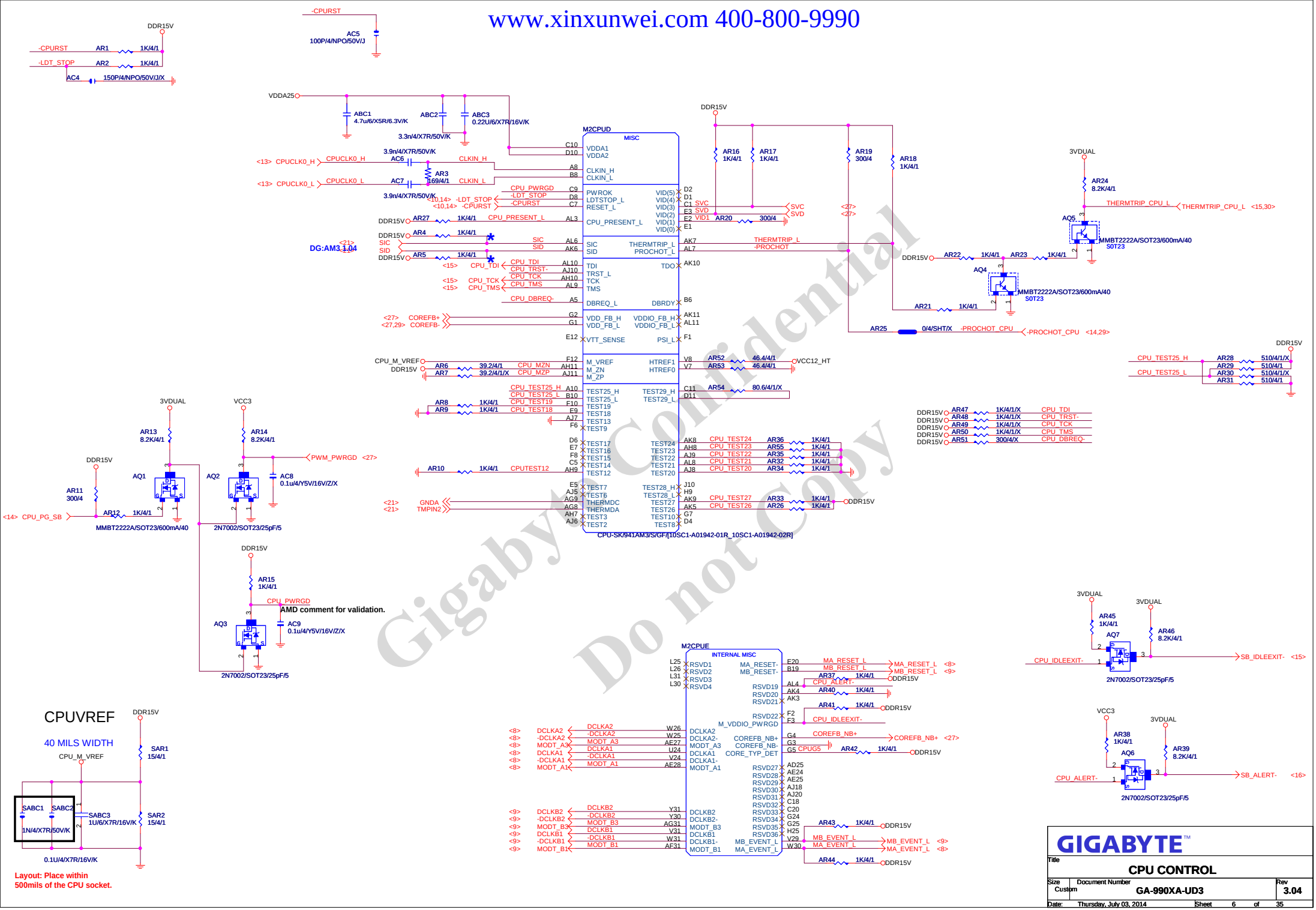

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Title	CPU CONTROL	
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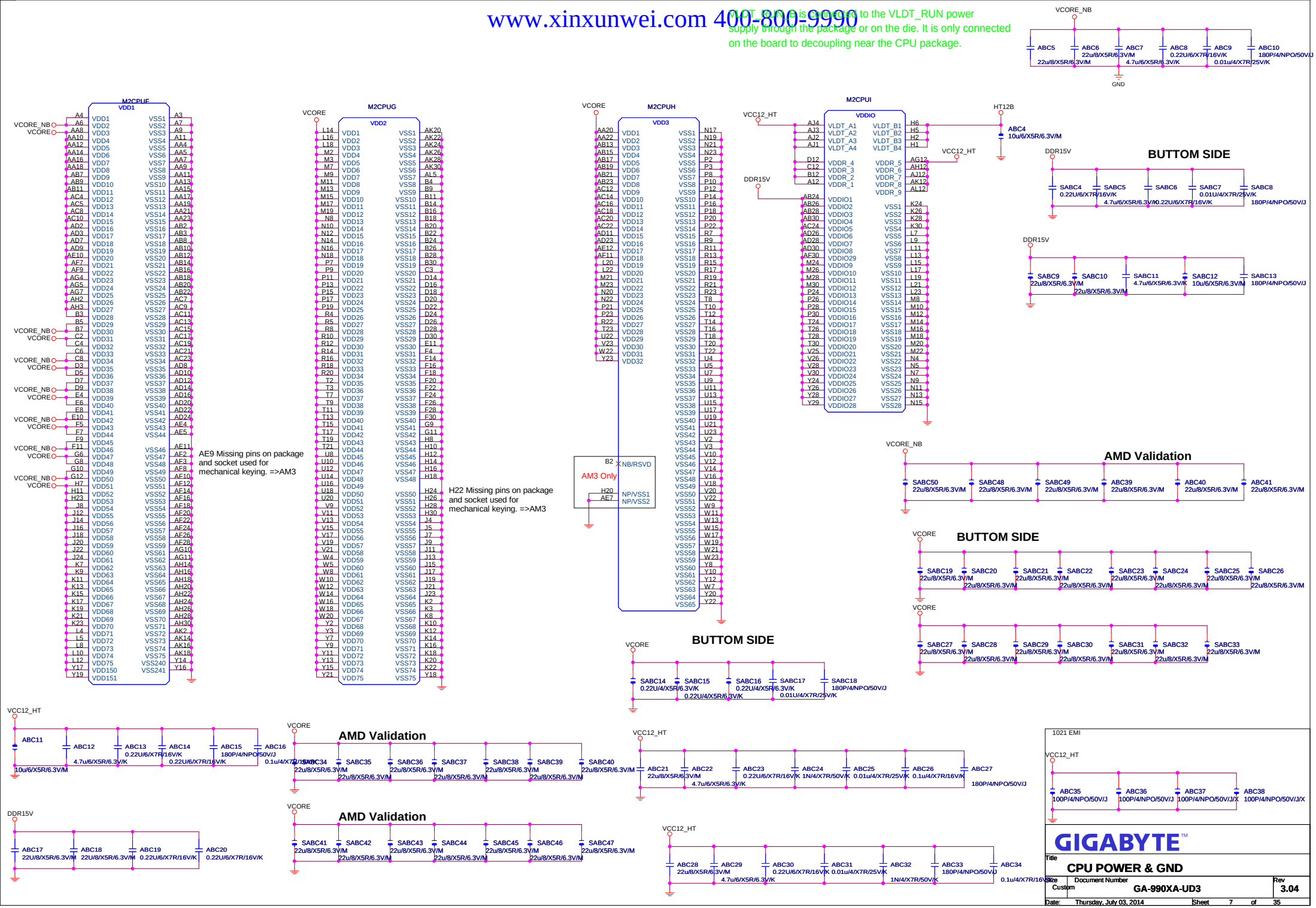
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



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Title: CPU POWER & GND

Size	Document Number	Rev
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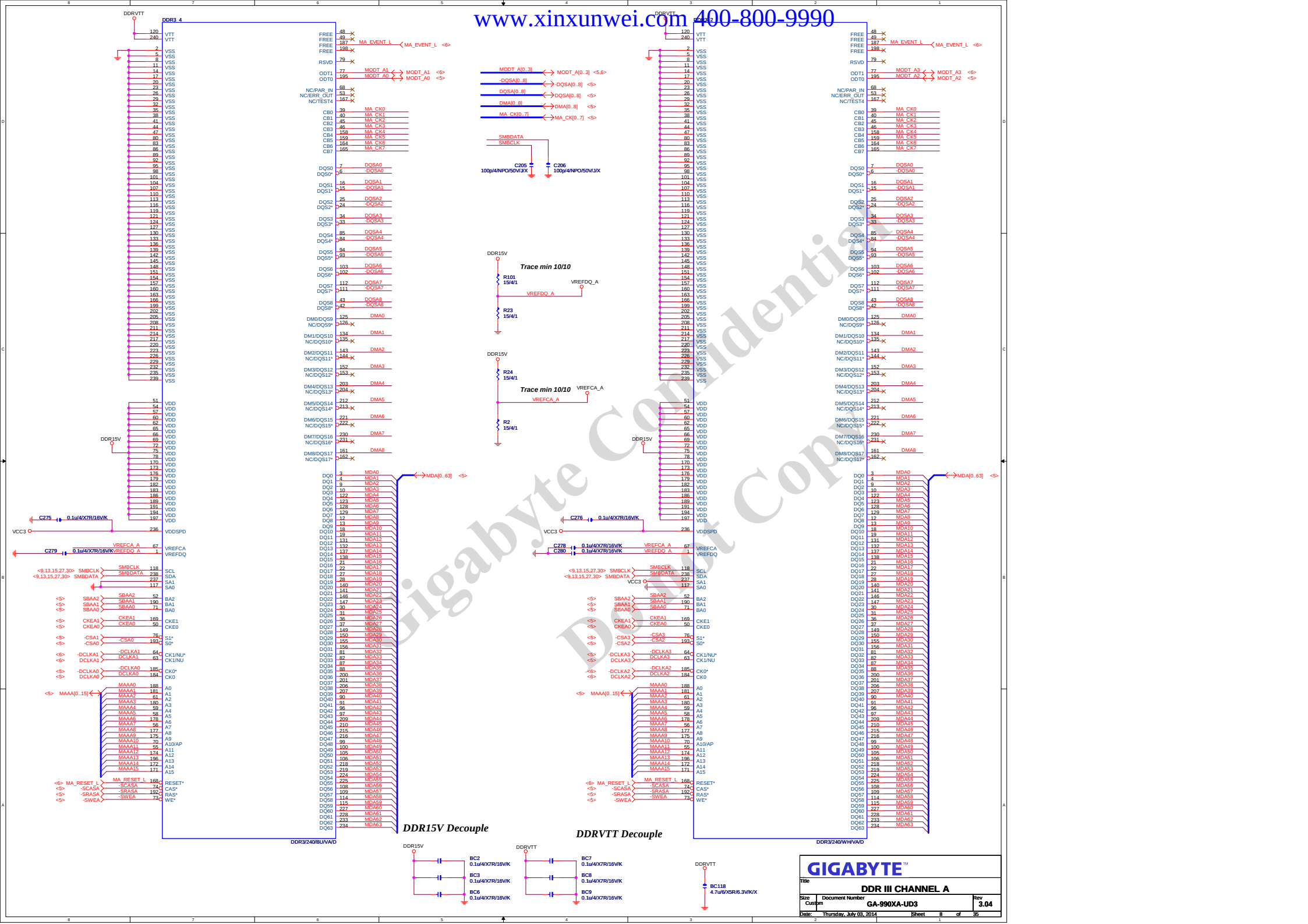

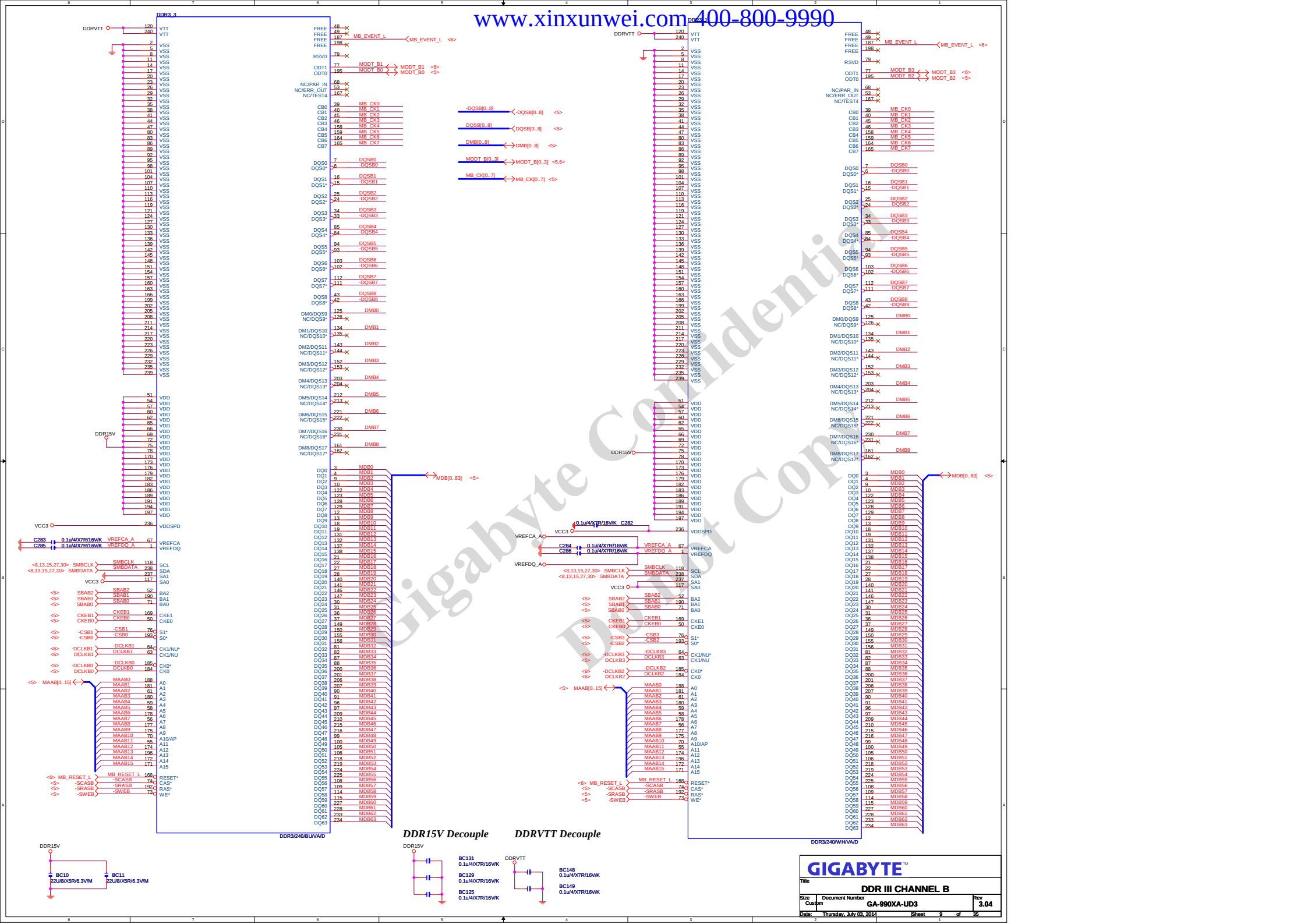

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Title	DDR III CHANNEL B	
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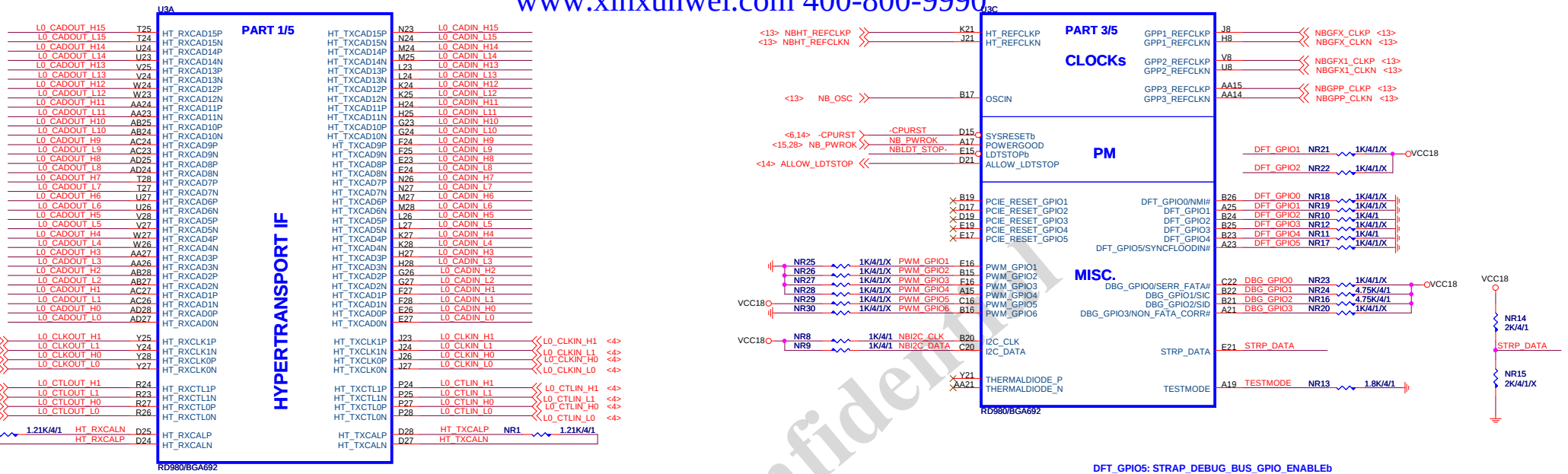

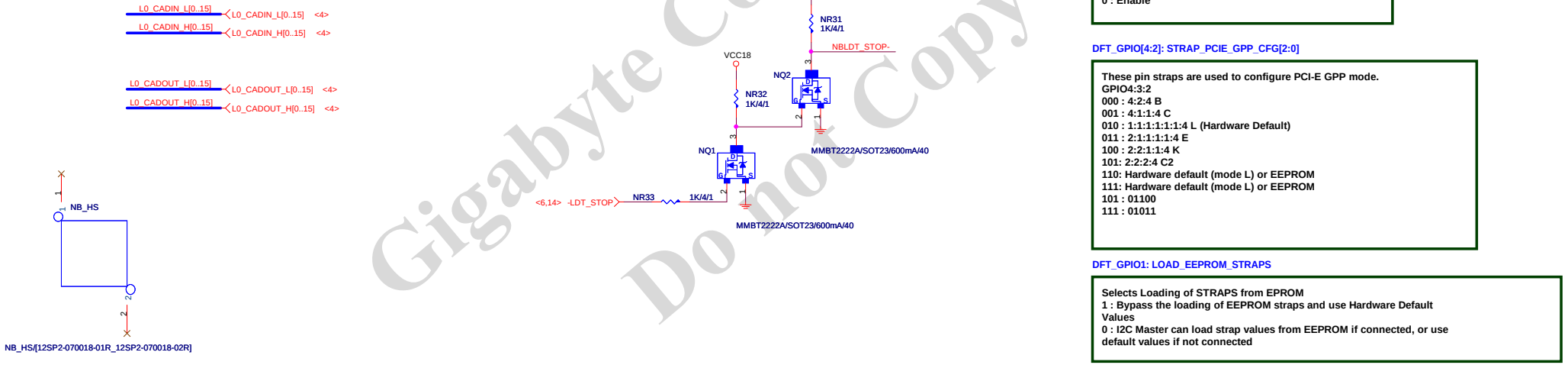

DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101: 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

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Title	RD990R HT-LINK I/F	
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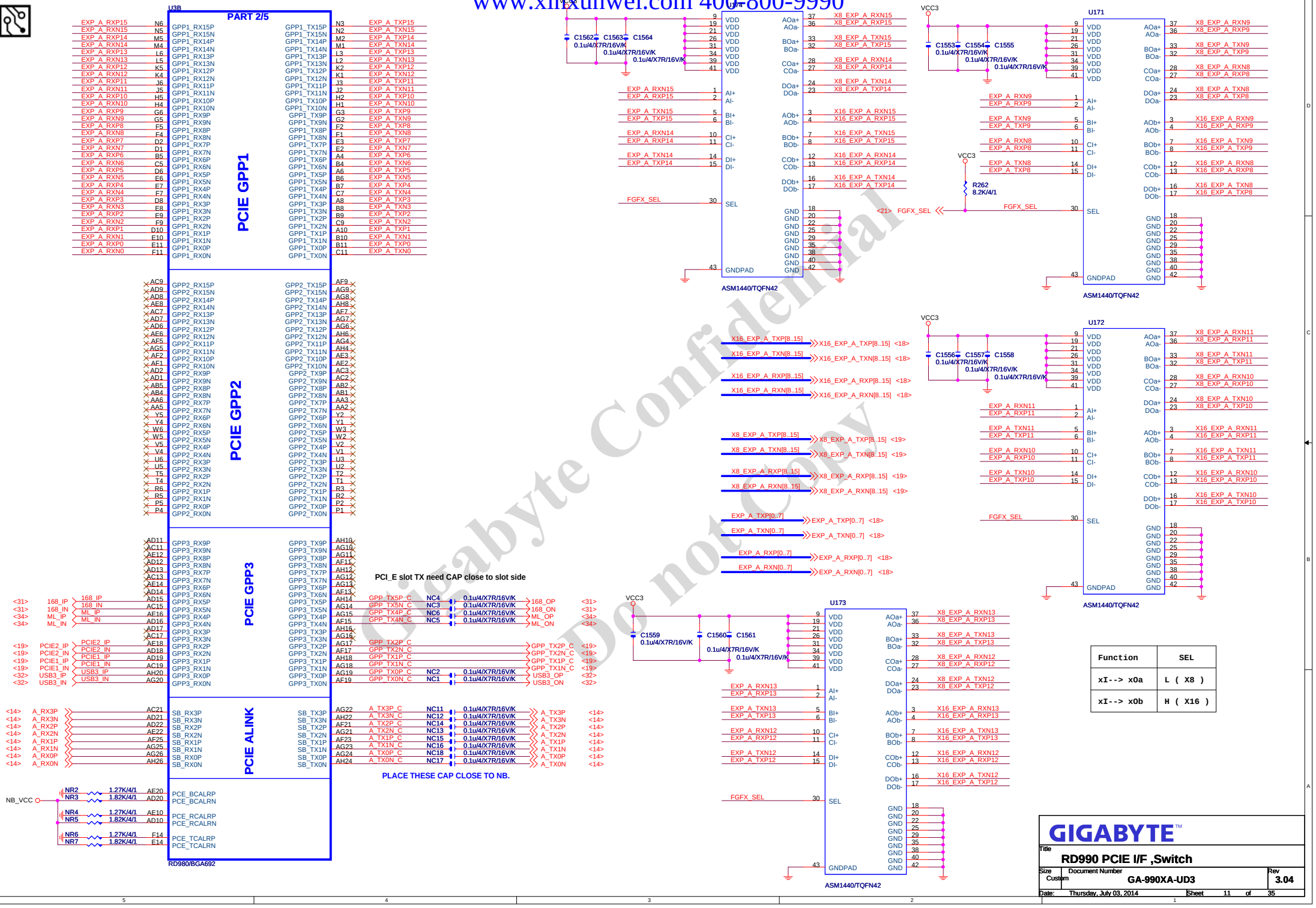

U3E

PART 5/5

GROUND

RD980/BGA692

U3D

PART 4/5

POWER

RD980/BGA692

VDDHT=>1.1V@3.25A

VDDPCIE=>1.1V@5.5A

VDDHTTX=>1.2V@1A

VDDA18=>1.8V@0.1A

VDDA18HTPLL=>1.8V@0.05A

VDDA18PCIE=>1.8V@2A

1.1V@8500mA

HT Link Stitching Caps

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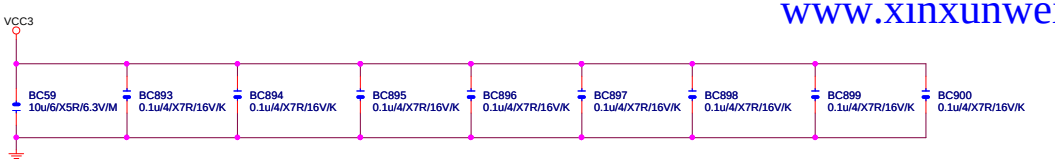


1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

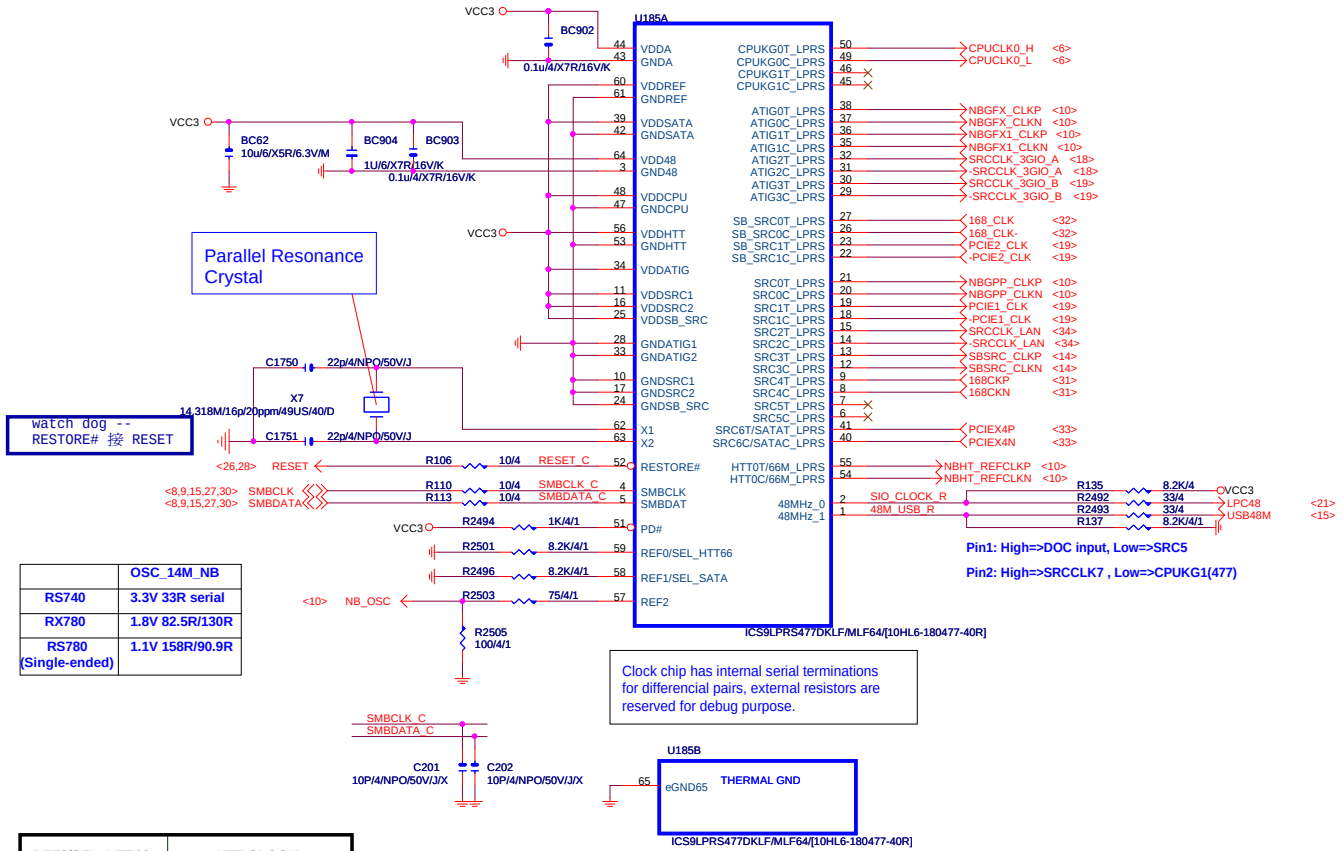
3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



Pin1: High=>DOC input, Low=>SRC5

Pin2: High=>SRCCLK7 , Low=>CPUKG1(477)

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

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Title: RTM880N-793

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PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

S.B HEATSINK

SB_HS

SB_HS/[12SP2-S06510-11R_12SP2-S06510-12R_12SP2-S06510-13R]

SB800 Part 1 of 5

PCIE_RST# / A_RST#

PCI EXPRESS INTERFACES

A_TX0P A_TX0N A_TX1P A_TX1N A_TX2P A_TX2N A_TX3P A_TX3N

A_RX0P A_RX0N A_RX1P A_RX1N A_RX2P A_RX2N A_RX3P A_RX3N

PCIE_CALRP PCIE_CALRN

GPP_TX0P GPP_TX0N GPP_TX1P GPP_TX1N GPP_TX2P GPP_TX2N GPP_TX3P GPP_TX3N

GPP_RX0P GPP_RX0N GPP_RX1P GPP_RX1N GPP_RX2P GPP_RX2N GPP_RX3P GPP_RX3N

PCIE_RCLKP/NB_LNK_CLKP

PCIE_RCLKN/NB_LNK_CLKN

NB_DISP_CLKP NB_DISP_CLKN

NB_HT_CLKP NB_HT_CLKN

CPU_HT_CLKP CPU_HT_CLKN

SLT_GFX_CLKP SLT_GFX_CLKN

GPP_CLK0P GPP_CLK0N

GPP_CLK1P GPP_CLK1N

GPP_CLK2P GPP_CLK2N

GPP_CLK3P GPP_CLK3N

GPP_CLK4P GPP_CLK4N

GPP_CLK5P GPP_CLK5N

GPP_CLK6P GPP_CLK6N

GPP_CLK7P GPP_CLK7N

GPP_CLK8P GPP_CLK8N

14M_25M_48M_OSC

25M_X1

25M_X2

SB950/BGA605/[10HB1-06B950-10R]

PCI CLKS

PCI INTERFACE

CLOCK GENERATOR

LPC

CPU

RTC

PX1 32.768K/12.5p/20ppm/TF38/35K/D

PC13 18P/4/NPO/50V/J

PC14 18P/4/NPO/50V/J

PX1 SHW/D0.64*5.08*6.74

PX2 25M/20p/30ppm/49US/20/D

PC15 22P/4/NPO/50V/J

PC16 22P/4/NPO/50V/J

PBC2 0.1u/4/X7R/16V/K

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

Low: Force PCIE GEN1, Up: Allow PCIE GEN2

	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

BIOS after boot setting
EC AOD-ACC

	LPC_CLK0 Rev.A12	LPC_CLK1
PULL HIGH	IMC ENABLED AOD Extreme	CLKGEN ENABLED
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT

20mil 20mil 20mil

BAT54C/SOT23/200mA

BAT BAT-SK/BK/P/S/D/SN

CR2032 BAT

CLR_CMOS RTCVDD PH/1*2/BK/2.54/VA/D

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

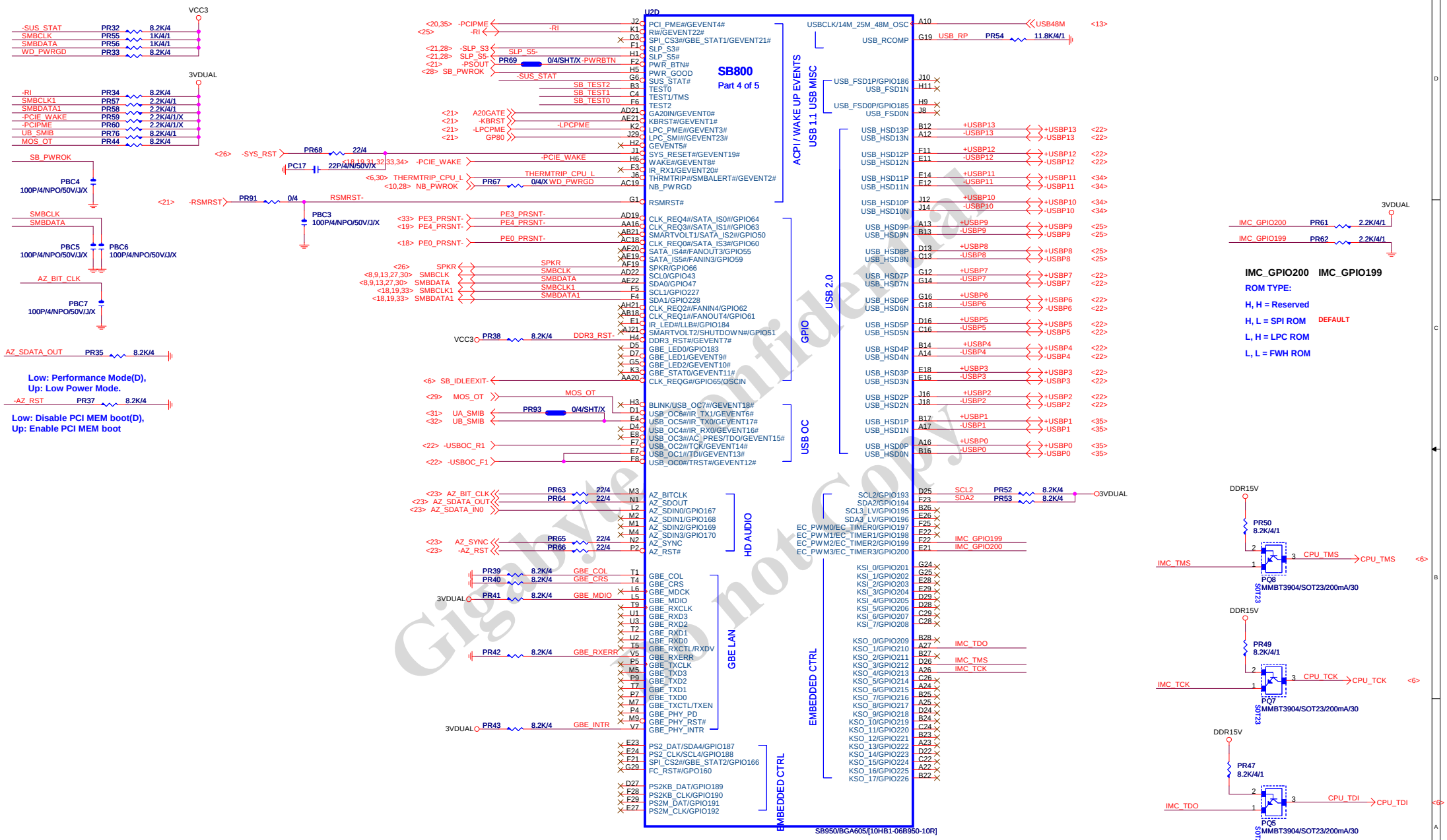
NOT ADD ICT FOR RTCVDD PIN

GIGABYTE

Title: ATI SB700 PCIE/PCI/CPU/LPC

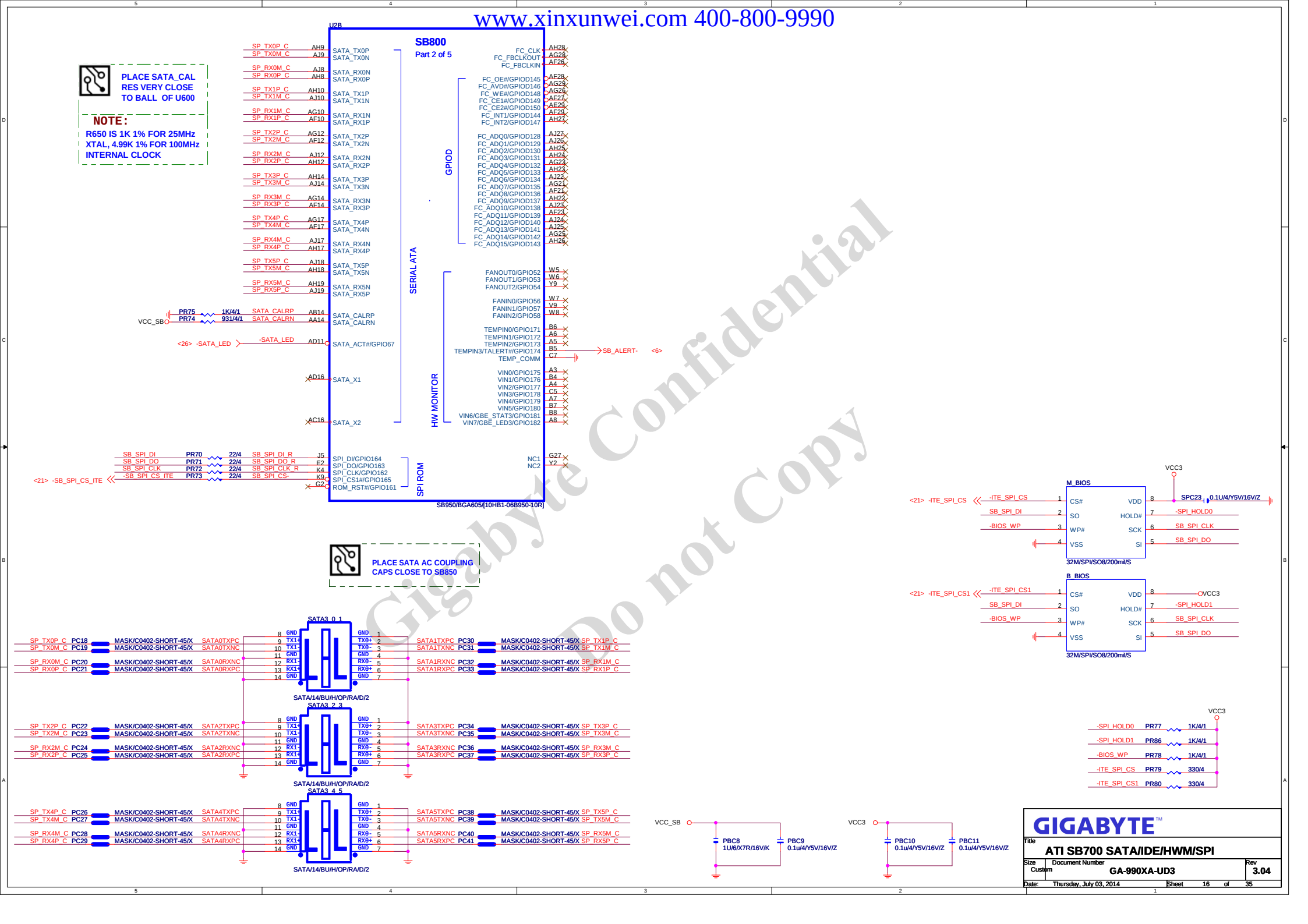
Size: Custom | Document Number: GA-990XA-UD3 | Rev: 3.04

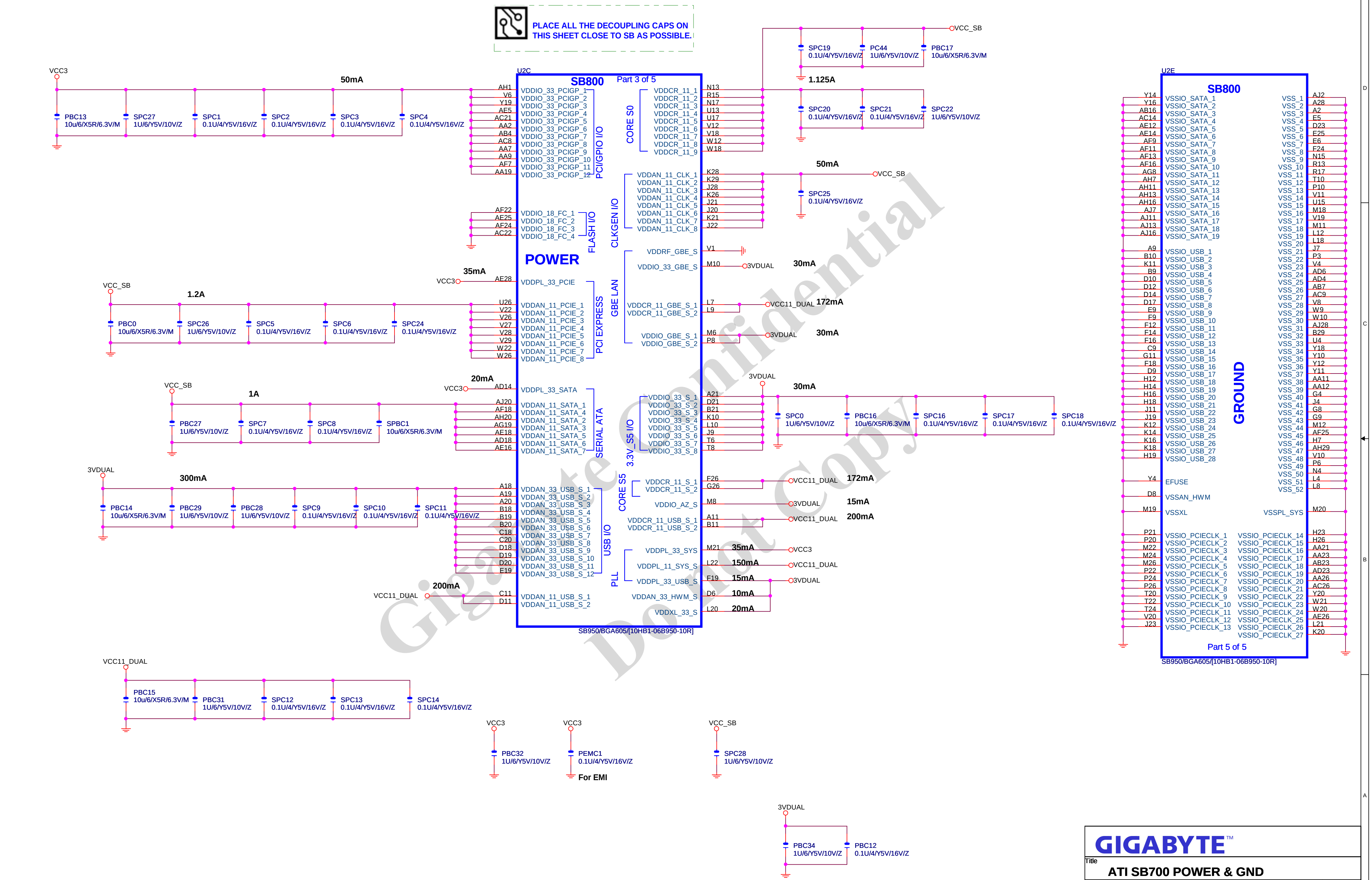
Date: Thursday, July 03, 2014 | Sheet 14 of 35



GIGABYTE™

Title	ATI SB700 ACPI/USB/GPIO/AUDIO
Size: Custom	Document Number: GA-990XA-UD3
Rev	3.04
Date: Thursday, July 03, 2014	Sheet 15 of 35

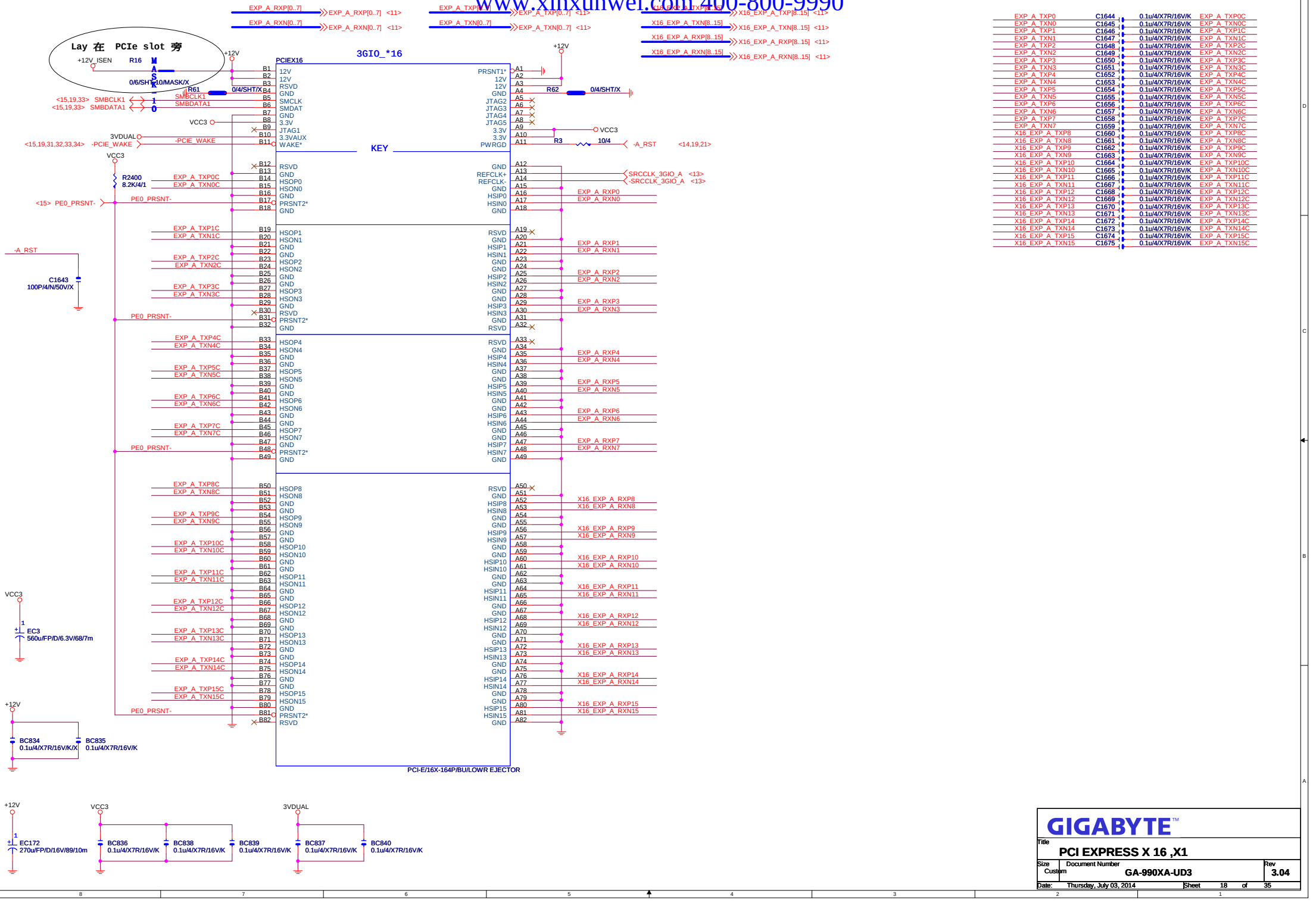




PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
U2C
SB800
Part 3 of 5
POWER
PCI/GPIO I/O
FLASH I/O
CORE S0
CLKGEN I/O
GBE LAN
PCI EXPRESS
SERIAL ATA
3.3V_S5 I/O
CORE S5
USB I/O
PLL
SB950/BGA605/[10HB1-06B950-10R]
U2E
SB800
GROUND
Part 5 of 5
SB950/BGA605/[10HB1-06B950-10R]
VCC3
50mA
PBC13 10u/6/X5R/6.3V/M
SPC27 1U/6/Y5V/10V/Z
SPC1 0.1U/4/Y5V/16V/Z
SPC2 0.1U/4/Y5V/16V/Z
SPC3 0.1U/4/Y5V/16V/Z
SPC4 0.1U/4/Y5V/16V/Z
VCC_SB
SPC19 0.1U/4/Y5V/16V/Z
PC44 1U/6/Y5V/10V/Z
PBC17 10u/6/X5R/6.3V/M
1.125A
SPC20 0.1U/4/Y5V/16V/Z
SPC21 0.1U/4/Y5V/16V/Z
SPC22 1U/6/Y5V/10V/Z
SPC25 0.1U/4/Y5V/16V/Z
35mA
1.2A
PBC0 10u/6/X5R/6.3V/M
SPC26 1U/6/Y5V/10V/Z
SPC5 0.1U/4/Y5V/16V/Z
SPC6 0.1U/4/Y5V/16V/Z
SPC24 0.1U/4/Y5V/16V/Z
VCC11_DUAL
172mA
3VDUAL
30mA
20mA
1A
PBC27 1U/6/Y5V/10V/Z
SPC7 0.1U/4/Y5V/16V/Z
SPC8 0.1U/4/Y5V/16V/Z
SPBC1 10u/6/X5R/6.3V/M
SPC0 1U/6/Y5V/10V/Z
PBC16 10u/6/X5R/6.3V/M
SPC16 0.1U/4/Y5V/16V/Z
SPC17 0.1U/4/Y5V/16V/Z
SPC18 0.1U/4/Y5V/16V/Z
300mA
PBC14 10u/6/X5R/6.3V/M
PBC29 1U/6/Y5V/10V/Z
PBC28 1U/6/Y5V/10V/Z
SPC9 0.1U/4/Y5V/16V/Z
SPC10 0.1U/4/Y5V/16V/Z
SPC11 0.1U/4/Y5V/16V/Z
15mA
200mA
150mA
10mA
PBC15 10u/6/X5R/6.3V/M
PBC31 1U/6/Y5V/10V/Z
SPC12 0.1U/4/Y5V/16V/Z
SPC13 0.1U/4/Y5V/16V/Z
SPC14 0.1U/4/Y5V/16V/Z
PBC32 1U/6/Y5V/10V/Z
PEMC1 0.1U/4/Y5V/16V/Z
For EMI
SPC28 1U/6/Y5V/10V/Z
PBC34 1U/6/Y5V/10V/Z
PBC12 0.1U/4/Y5V/16V/Z

GIGABYTE

Title	ATI SB700 POWER & GND
Size	Custom
Document Number	GA-990XA-UD3
Rev	3.04
Date:	Wednesday, August 01, 2012
Sheet	17 of 35



EXP_A_TXP0	C1644	0.1u/4/X7R/16V/K	EXP_A_TXP0C
EXP_A_TXN0	C1645	0.1u/4/X7R/16V/K	EXP_A_TXN0C
EXP_A_TXP1	C1646	0.1u/4/X7R/16V/K	EXP_A_TXP1C
EXP_A_TXN1	C1647	0.1u/4/X7R/16V/K	EXP_A_TXN1C
EXP_A_TXP2	C1648	0.1u/4/X7R/16V/K	EXP_A_TXP2C
EXP_A_TXN2	C1649	0.1u/4/X7R/16V/K	EXP_A_TXN2C
EXP_A_TXP3	C1650	0.1u/4/X7R/16V/K	EXP_A_TXP3C
EXP_A_TXN3	C1651	0.1u/4/X7R/16V/K	EXP_A_TXN3C
EXP_A_TXP4	C1652	0.1u/4/X7R/16V/K	EXP_A_TXP4C
EXP_A_TXN4	C1653	0.1u/4/X7R/16V/K	EXP_A_TXN4C
EXP_A_TXP5	C1654	0.1u/4/X7R/16V/K	EXP_A_TXP5C
EXP_A_TXN5	C1655	0.1u/4/X7R/16V/K	EXP_A_TXN5C
EXP_A_TXP6	C1656	0.1u/4/X7R/16V/K	EXP_A_TXP6C
EXP_A_TXN6	C1657	0.1u/4/X7R/16V/K	EXP_A_TXN6C
EXP_A_TXP7	C1658	0.1u/4/X7R/16V/K	EXP_A_TXP7C
EXP_A_TXN7	C1659	0.1u/4/X7R/16V/K	EXP_A_TXN7C
X16_EXP_A_TXP8	C1660	0.1u/4/X7R/16V/K	EXP_A_TXP8C
X16_EXP_A_TXN8	C1661	0.1u/4/X7R/16V/K	EXP_A_TXN8C
X16_EXP_A_TXP9	C1662	0.1u/4/X7R/16V/K	EXP_A_TXP9C
X16_EXP_A_TXN9	C1663	0.1u/4/X7R/16V/K	EXP_A_TXN9C
X16_EXP_A_TXP10	C1664	0.1u/4/X7R/16V/K	EXP_A_TXP10C
X16_EXP_A_TXN10	C1665	0.1u/4/X7R/16V/K	EXP_A_TXN10C
X16_EXP_A_TXP11	C1666	0.1u/4/X7R/16V/K	EXP_A_TXP11C
X16_EXP_A_TXN11	C1667	0.1u/4/X7R/16V/K	EXP_A_TXN11C
X16_EXP_A_TXP12	C1668	0.1u/4/X7R/16V/K	EXP_A_TXP12C
X16_EXP_A_TXN12	C1669	0.1u/4/X7R/16V/K	EXP_A_TXN12C
X16_EXP_A_TXP13	C1670	0.1u/4/X7R/16V/K	EXP_A_TXP13C
X16_EXP_A_TXN13	C1671	0.1u/4/X7R/16V/K	EXP_A_TXN13C
X16_EXP_A_TXP14	C1672	0.1u/4/X7R/16V/K	EXP_A_TXP14C
X16_EXP_A_TXN14	C1673	0.1u/4/X7R/16V/K	EXP_A_TXN14C
X16_EXP_A_TXP15	C1674	0.1u/4/X7R/16V/K	EXP_A_TXP15C
X16_EXP_A_TXN15	C1675	0.1u/4/X7R/16V/K	EXP_A_TXN15C

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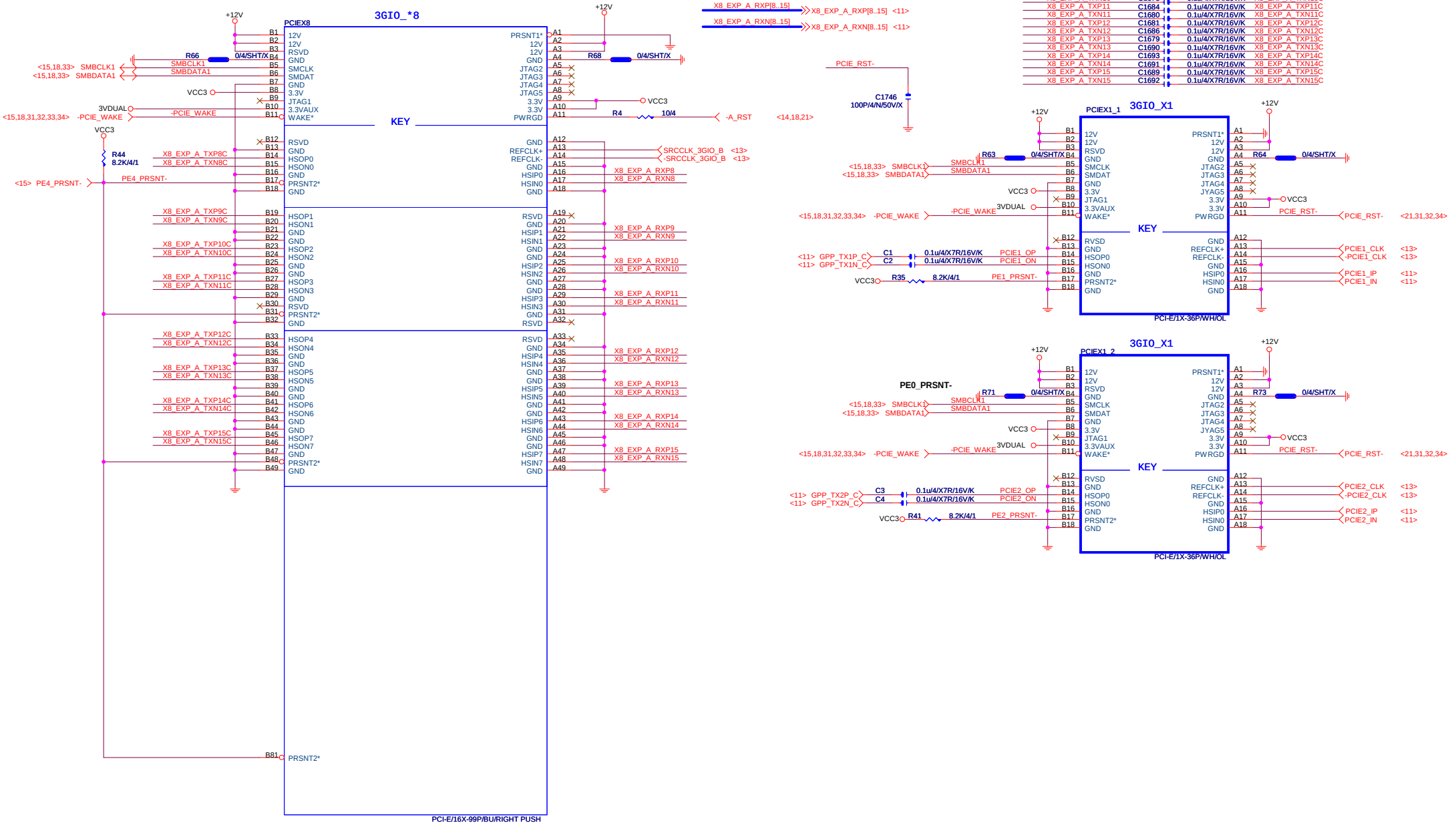
Title	PCI EXPRESS X 16 ,X1	
Size: Custom	Document Number: GA-990XA-UD3	Rev: 3.04
Date: Thursday, July 03, 2014	Sheet 18 of 35	



Title	PCI_E x8 ,PCI_E x1 SLOT 1,2
Size	Custom
Document Number	GA-990XA-UD3
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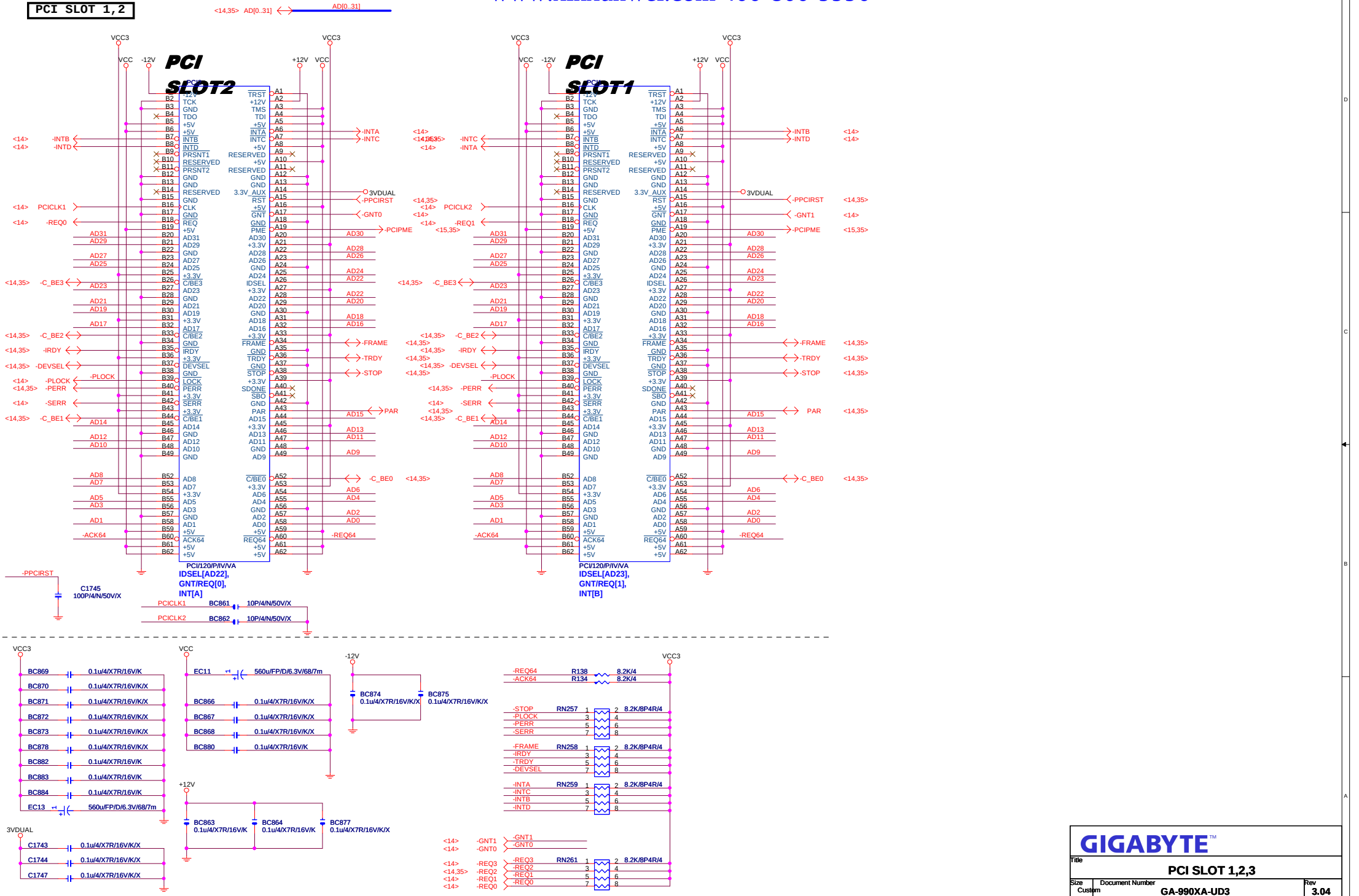
PCI SLOT 1,2



Title	PCI SLOT 1,2,3		
Size: Custom	Document Number: GA-990XA-UD3		Rev: 3.04
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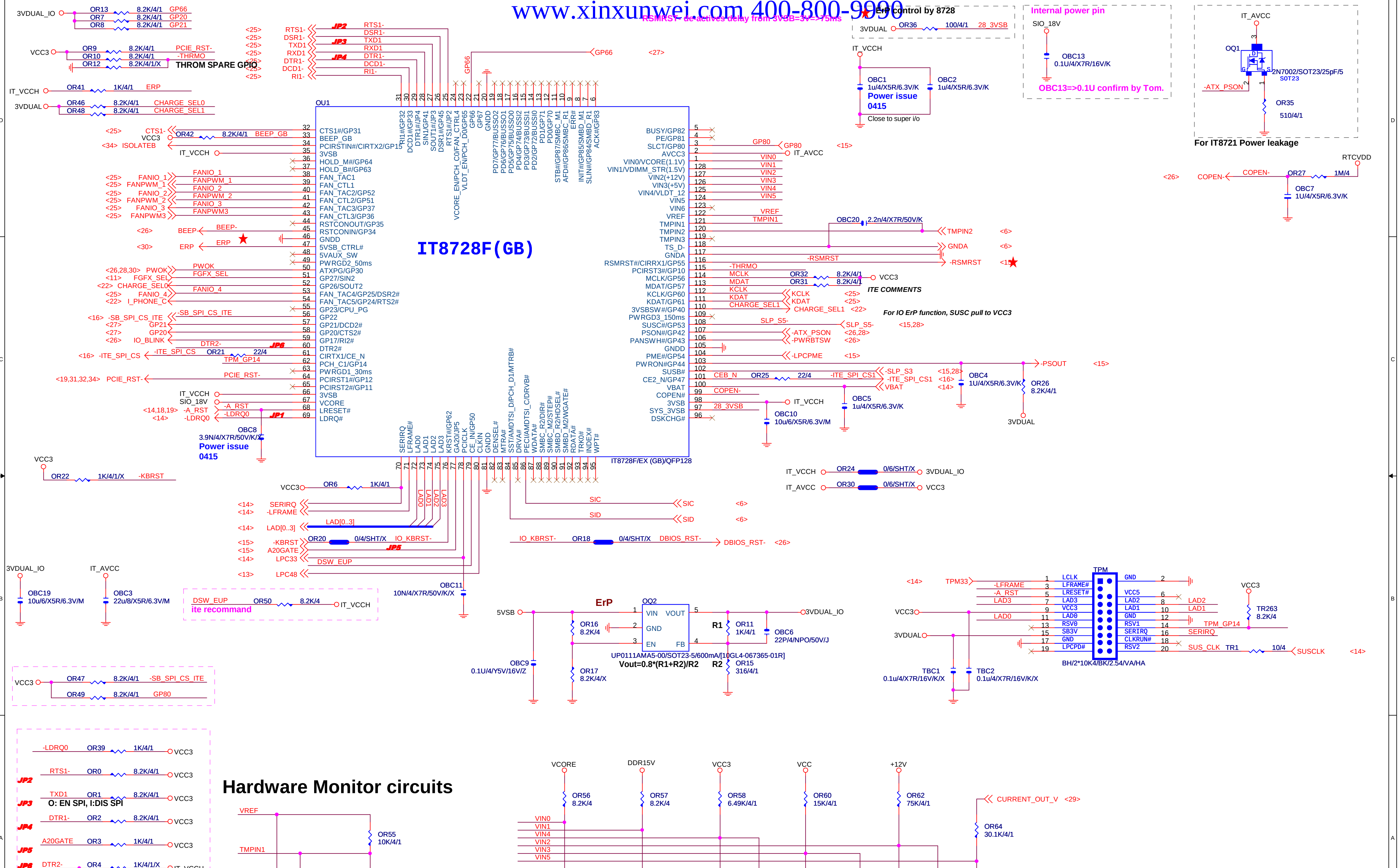
Hardware Monitor circuits


IT8728F(GB)
IT8728F/EX (GB)/QFP128
RSMRST- de-actives delay from 3VSB=3V=>75ms
ErP control by 8728
Internal power pin
OBC13=>0.1U confirm by Tom.
For IT8721 Power leakage
Power issue 0415
Close to super i/o
ITE COMMENTS
For IO ErP function, SUSC pull to VCC3
ite recommand
ErP
UP0111AMA5-00/SOT23-5/600mA/[10GL4-067365-01R]
Vout=0.8*(R1+R2)/R2
TPM
BH/2*10K4/BK/2.54/VA/HA
THROM SPARE GPIO
O: EN SPI, I:DIS SPI
DTR2- High: UV/OV by BIOS setting, Low: UV/OV by HW strap.
SYSTEM Thermister
CURRENT_OUT_V

GIGABYTE

Title: ITE 8720 JX LPC IO ,Dual-BIOS ,TPM

Size	Document Number	Rev
Custom	GA-990XA-UD3	3.04

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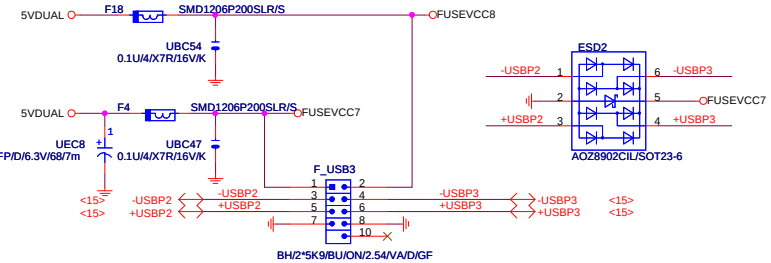
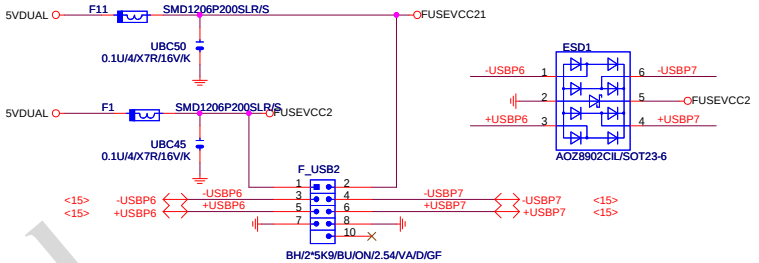
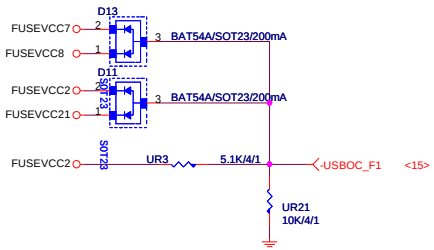
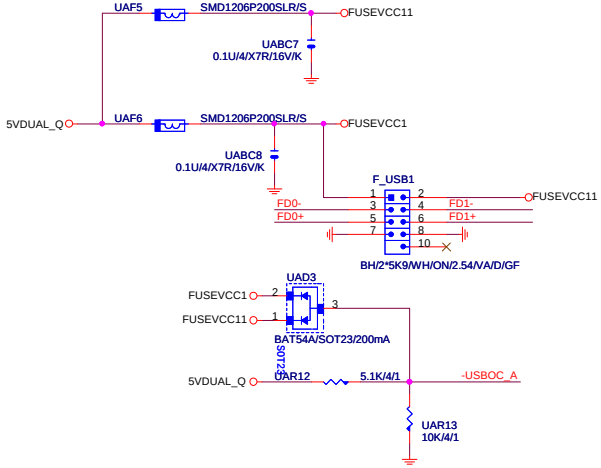
FRONT SIDE USB2

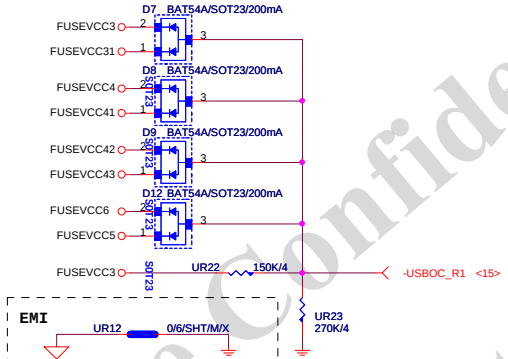




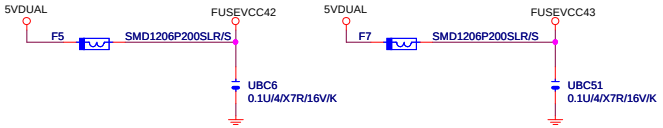


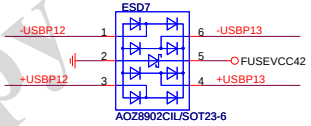
FRONT SIDE USB1

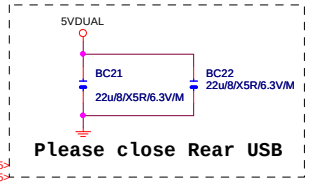


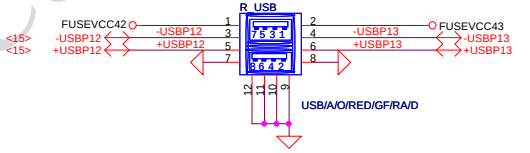


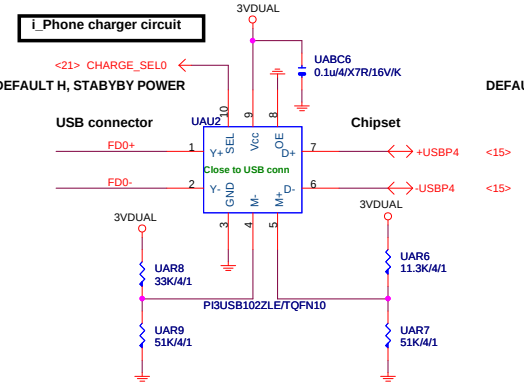
REAR USB

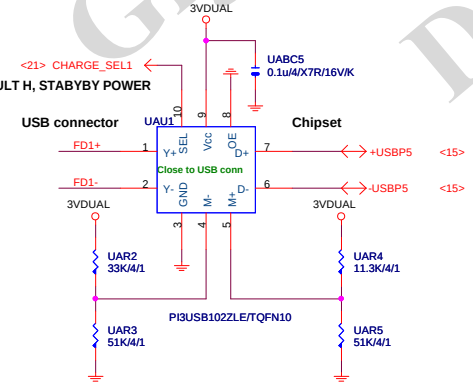


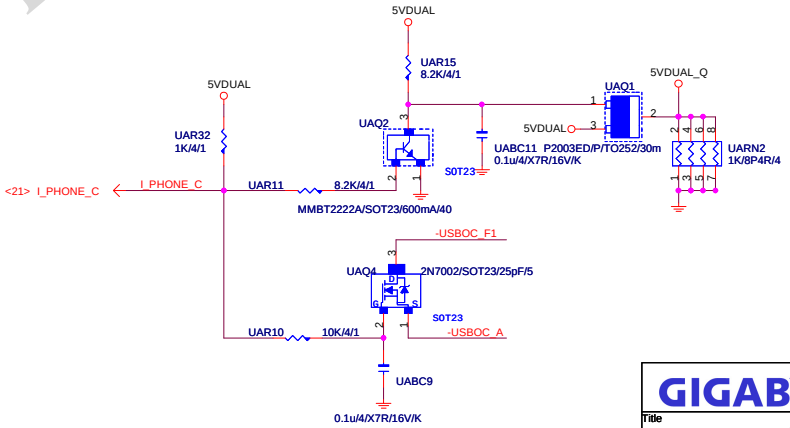












GIGABYTE™

Title	COM/LPT/F_USB/I_PWR	
Size: Custom	Document Number: GA-990XA-UD3	Rev: 3.04
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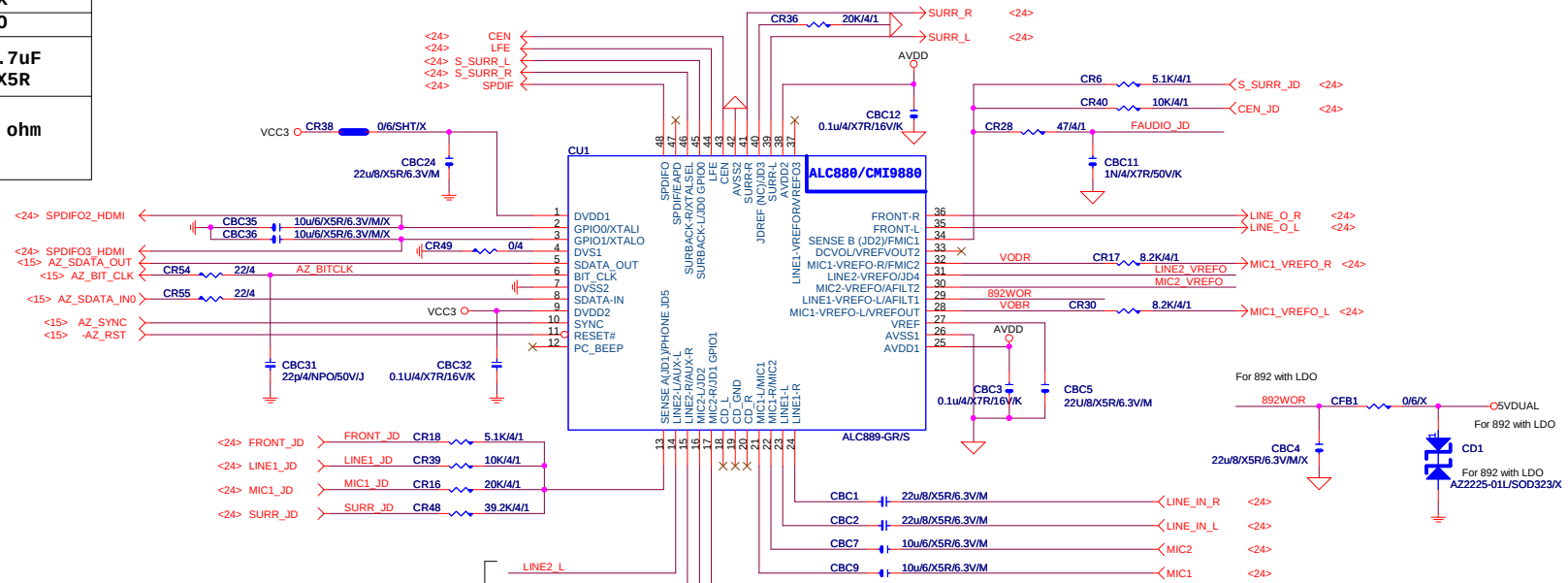
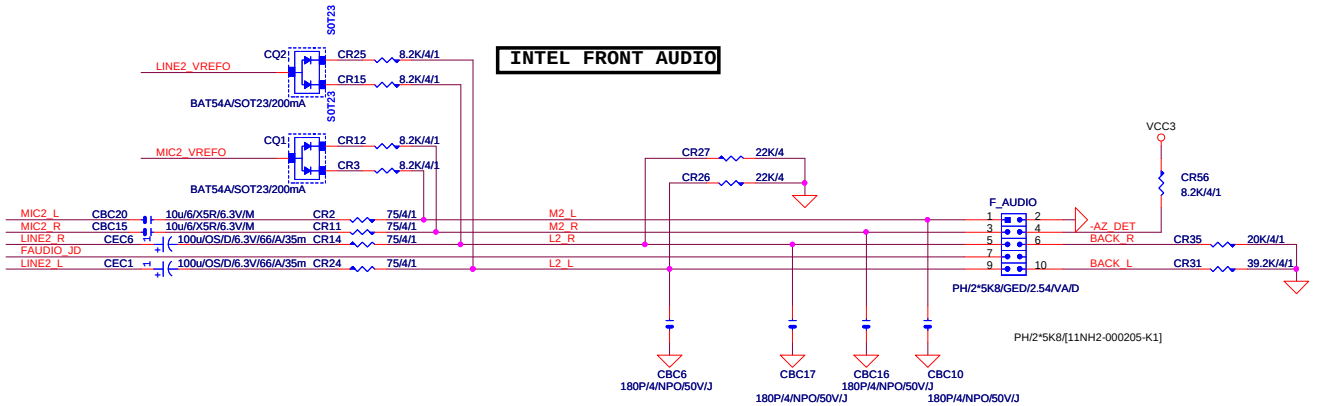
AZALIA CODEC *ALC892/ALC889/ Colay*

	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm



INTEL FRONT AUDIO



GIGABYTE™

Title	ALC892R CODEC	
Size: Custom	Document Number: GA-990XA-UD3	Rev: 3.04
Date: Thursday, July 03, 2014	Sheet 23 of 35	

CR33
0/6/SHT/X

+12V
AVDD
CQ3
CD3
CD4148WP/1206/300mA
78L05/SOT89/0.1A
5VDUAL
CD4
CD4148WP/1206/300mA
CBC8
22u/8/X5R/6.3V/M
CD2
CBC21
1U/6/X7R/16V/K
AZ2225-01L/SOD323

For ESD PROTECT DIODE

SPDIF

<23> SPDIFO3_HDMI
<23> SPDIFO2_HDMI
CR52 0/4/X
CR53 0/4
For HDMI SPDIF
CBC37
100p/4/NPO/50V/J
SPDIF_O
SPDIF_O
PH/1*2/BK/2.54/VA/D

FUSEVCC3
<23> SPDIF
SPDIF
OPTICAL
FR/5P/BK/T/D/S(GY)

LINE OUT
FRONT OUT

<23> LINE_O_R
<23> LINE_O_L
CEC2 100u/OS/D/6.3V/66/A/35m
CEC3 100u/OS/D/6.3V/66/A/35m
CR7 62/4
CR9 62/4
AJ_B5
AJ_B2
CR10 22K/4
CBC23 180P/4/NPO/50V/J
CR8 22K/4
CBC26 180P/4/NPO/50V/J

LINE-IN

<23> LINE_IN_R
<23> LINE_IN_L
CR5 62/4
CR13 62/4
AJ_A5
AJ_A2
CBC18 180P/4/NPO/50V/J
CBC27 180P/4/NPO/50V/J

MIC

<23> MIC2
<23> MIC1
<23> MIC1_VREFO_R
<23> MIC1_VREFO_L
CR29 62/4
CR32 62/4
CR37 0/4/SHT/X
CR34 0/4/SHT/X
AJ_C5
AJ_C2
CBC19 180P/4/NPO/50V/J
CBC22 180P/4/NPO/50V/J

SURROUND

<23> SURR_R
<23> SURR_L
CEC5 100u/OS/D/6.3V/66/A/35m
CEC7 100u/OS/D/6.3V/66/A/35m
CR46 62/4
CR19 62/4
BJ_C5
BJ_C2
CR20 22K/4
CBC29 180P/4/NPO/50V/J
CR45 22K/4
CBC28 180P/4/NPO/50V/J

CEN/LFE

<23> LFE
<23> CEN
CEC9 100u/OS/D/6.3V/66/A/35m
CEC10 100u/OS/D/6.3V/66/A/35m
CR50 62/4
CR41 62/4
BJ_B5
BJ_B2
CR42 22K/4
CBC25 180P/4/NPO/50V/J
CR51 22K/4
CBC34 180P/4/NPO/50V/J

SURR BACK

<23> S_SURR_R
<23> S_SURR_L
CEC8 100u/OS/D/6.3V/66/A/35m
CEC4 100u/OS/D/6.3V/66/A/35m
CR21 62/4
CR47 62/4
BJ_A5
BJ_A2
CR43 22K/4
CBC33 180P/4/NPO/50V/J
CR22 22K/4
CBC30 180P/4/NPO/50V/J

For Audio precision test
CBC38 0.01u/4/X7R/25V/K

USB_LAN
R_USB2
R_USB1

AUDIOB
<23> LINE1_JD
LINE1_JD
AJ_A5
AJ_A2
LINE-IN
<23> FRONT_JD
FRONT_JD
AJ_B5
AJ_B2
LINE-OUT
<23> MIC1_JD
MIC1_JD
AJ_C5
AJ_C2
MIC-IN
GND

BLUE
LINE-IN
GREEN
LINE-OUT
PINK
MIC-IN

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

A3RJ/13P/B/[11NR6-403006-01_11NR6-403006-02]
3RJ+15F/[11NR6-403004-11]

AUDIOA
<23> CEN_JD
CEN_JD
BJ_B5
BJ_B2
REAR
<23> SURR_JD
SURR_JD
BJ_C5
BJ_C2
CEN
<23> S_SURR_JD
S_SURR_JD
BJ_A5
BJ_A2
SIDE
GND

Orange
CEN/LFE
ALC880 - SURROUND
CMI9880 - Back SURR
Black
Back side Speaker
Azalia Port G
Gray
Left & Right Side Speaker
CMI9880 - Side SURR

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

A3RJ/13P/OBG/[11NR6-403006-71]
3RJ+15F/[11NR6-403004-31]

GIGABYTE™

Title: AUDIO JACK
Size: Custom
Document Number: GA-990XA-UD3
Rev: 3.04
Date: Thursday, July 03, 2014
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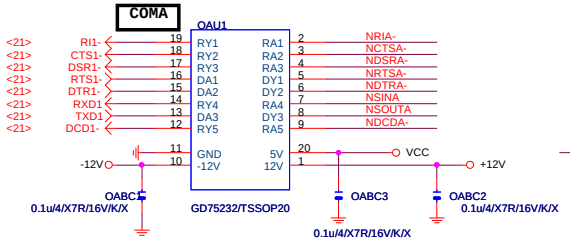
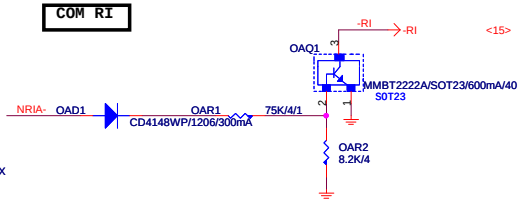
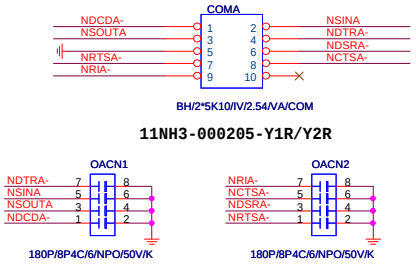
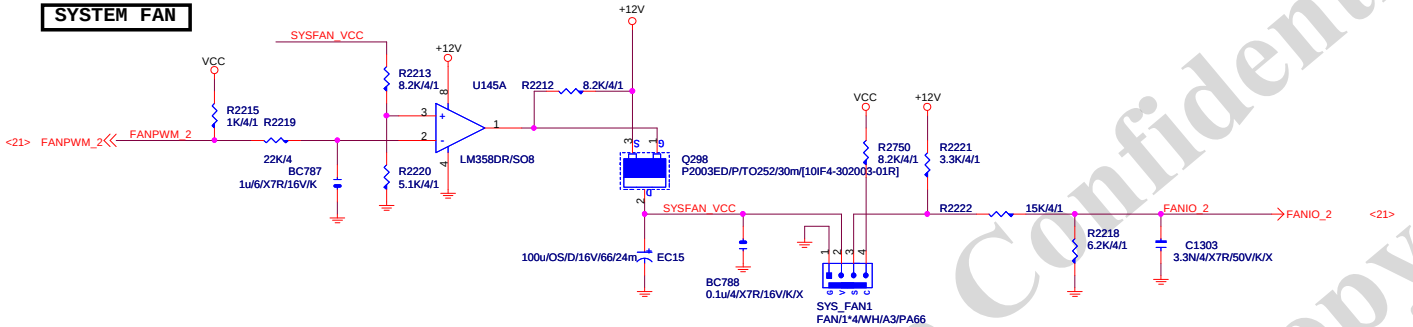


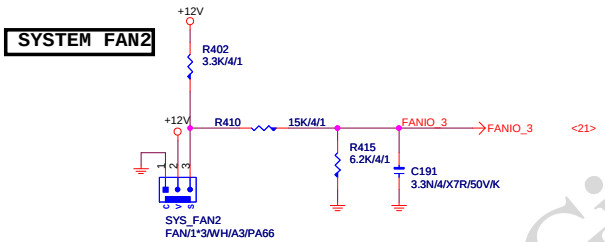




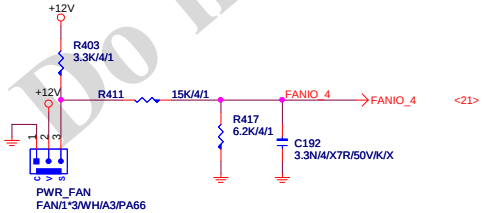
SYSTEM FAN



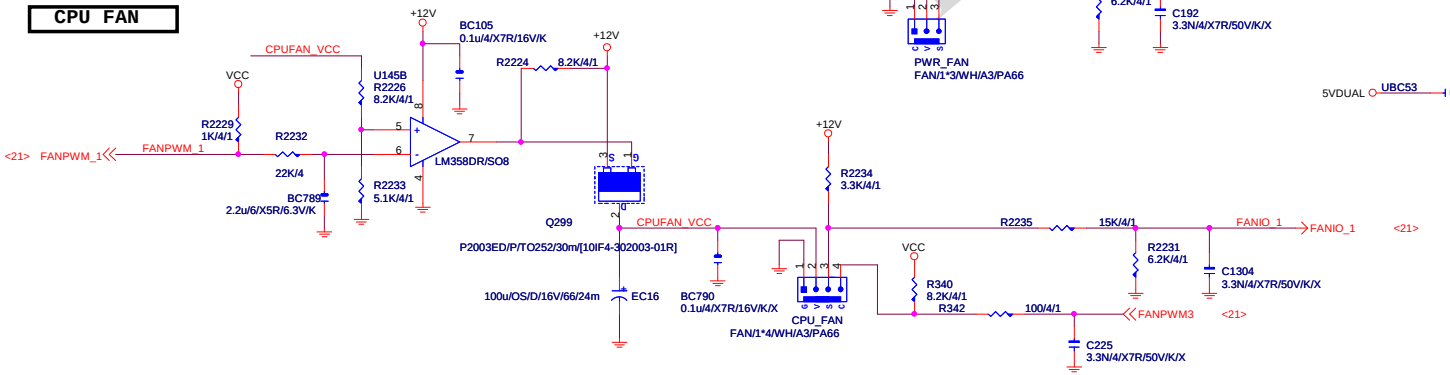
SYSTEM FAN2

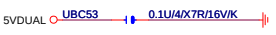


POWER FAN

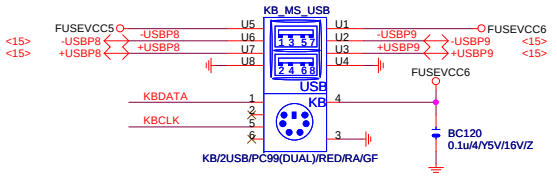


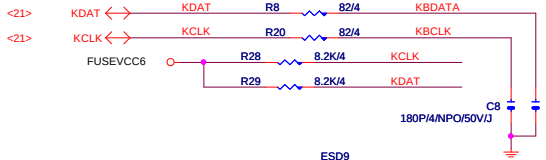
CPU FAN

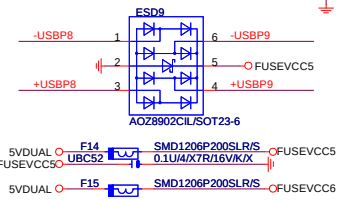




KB & USB







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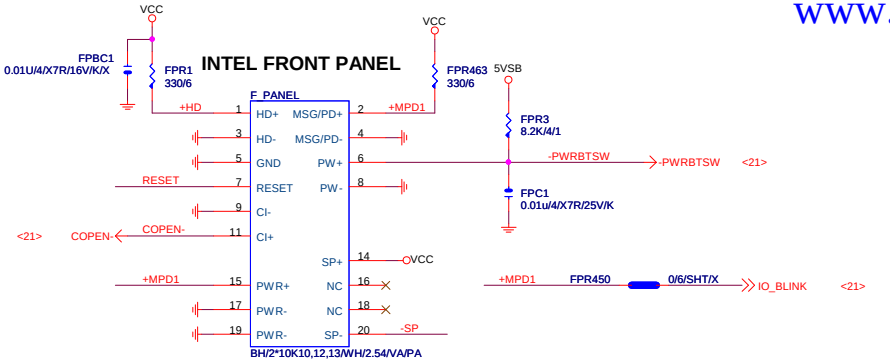

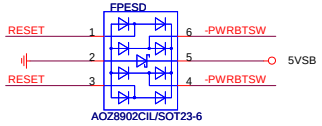

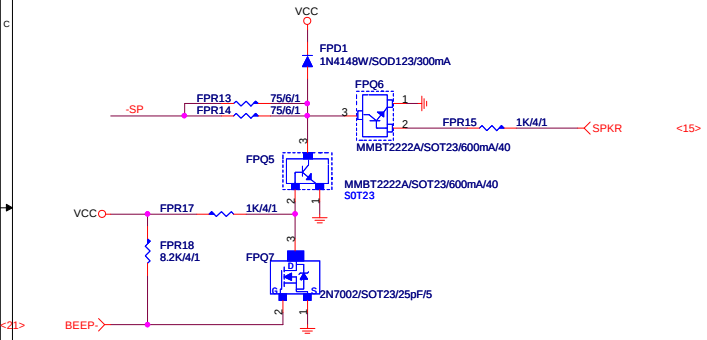

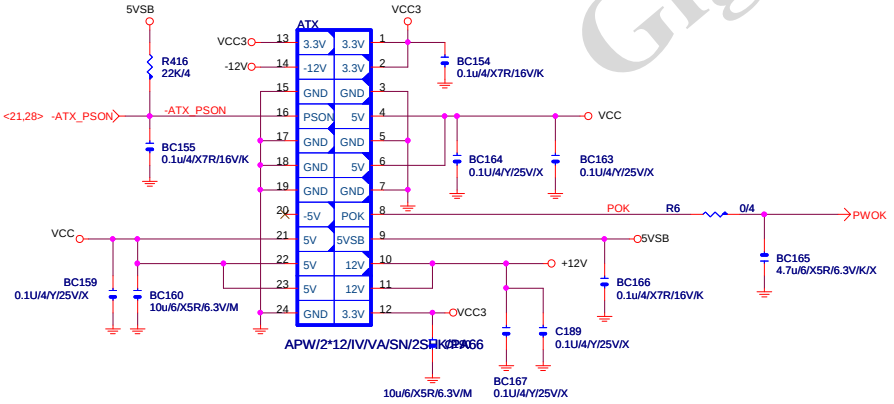

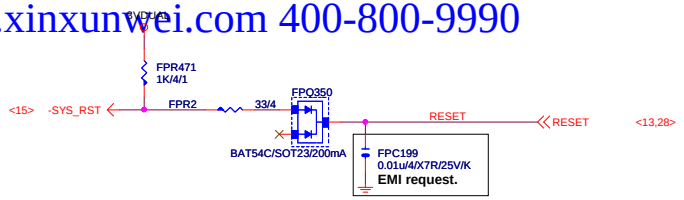

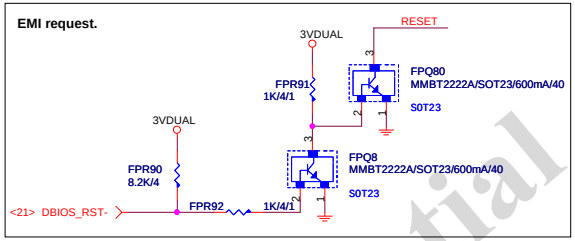

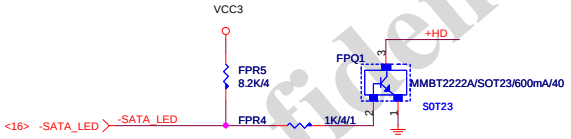

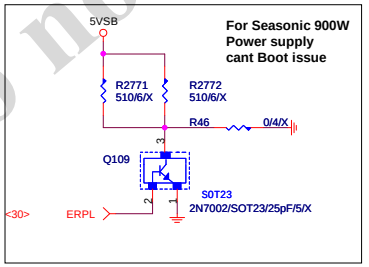

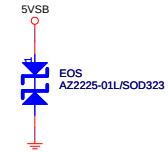

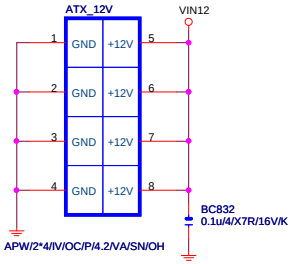

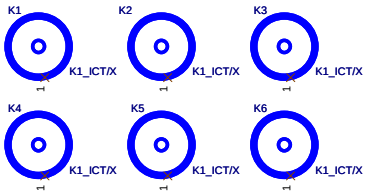

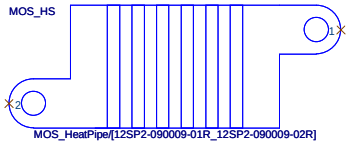

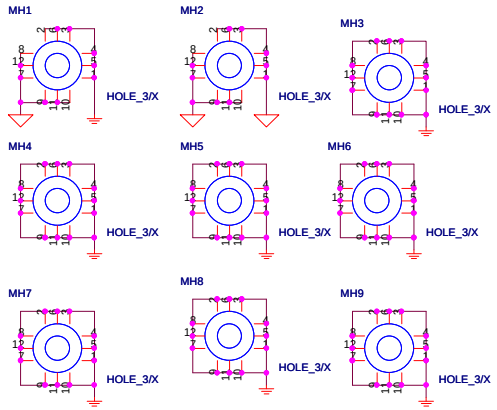

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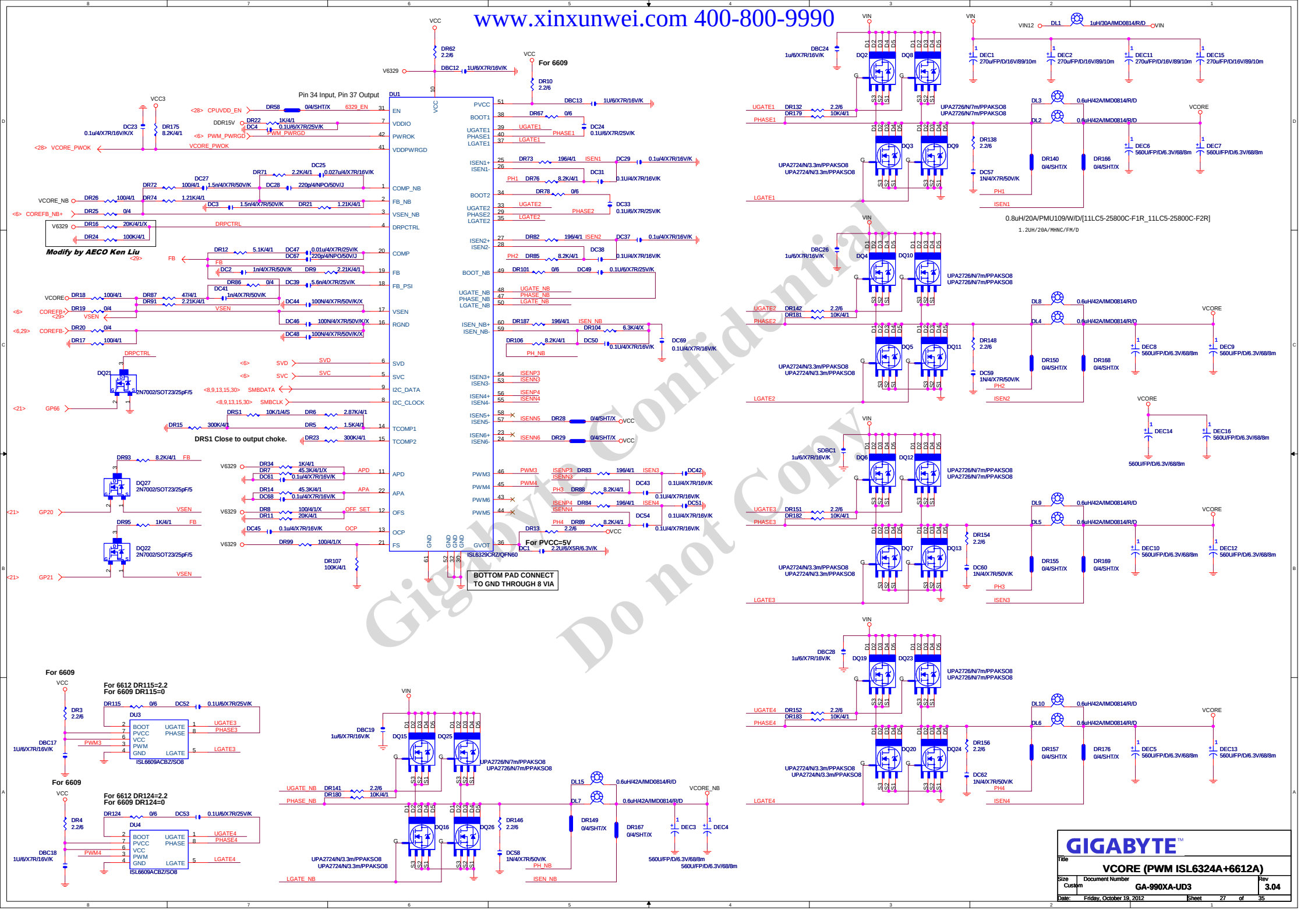
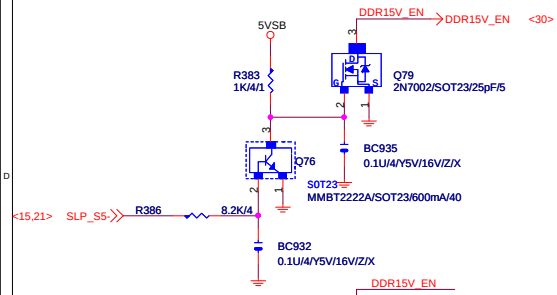
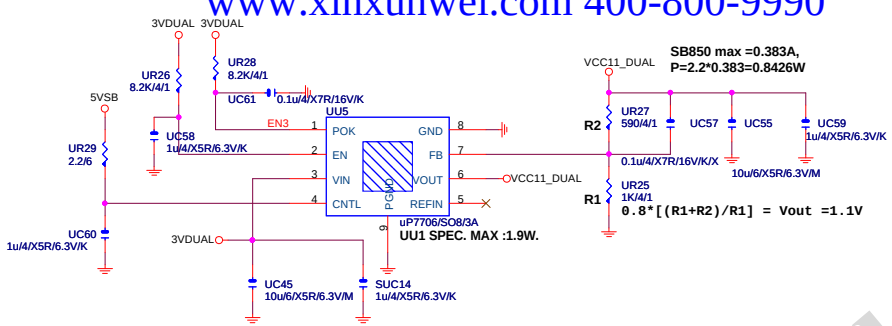
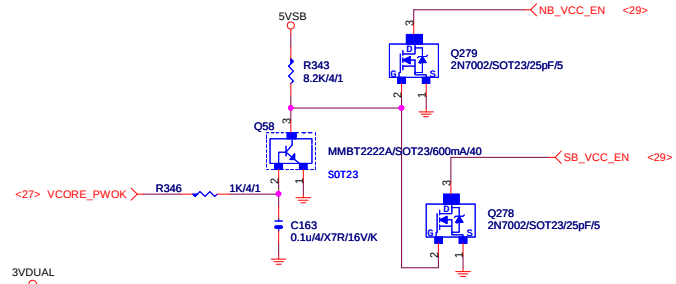
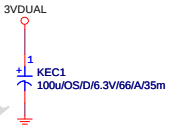
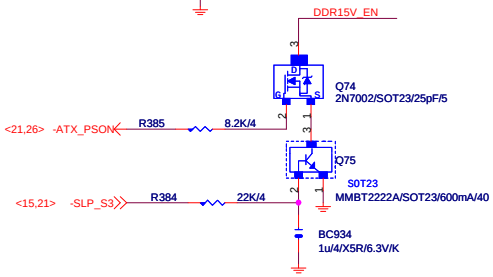


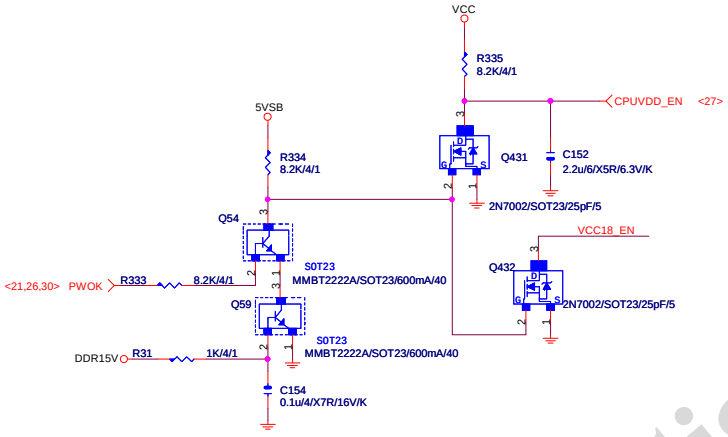




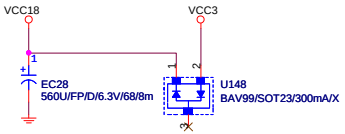


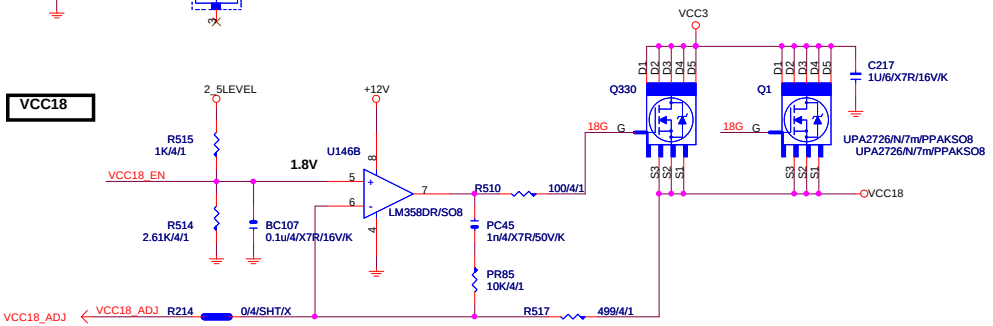


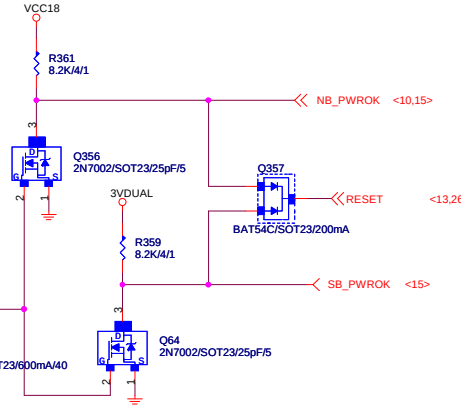


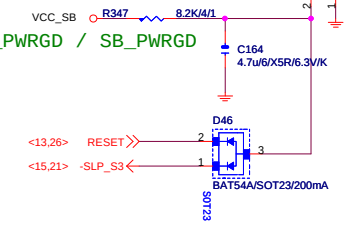


ATI for VCC3/VCC18 power ramp-up 2.1V









PWOK > NB_PWRGD / SB_PWRGD

(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms

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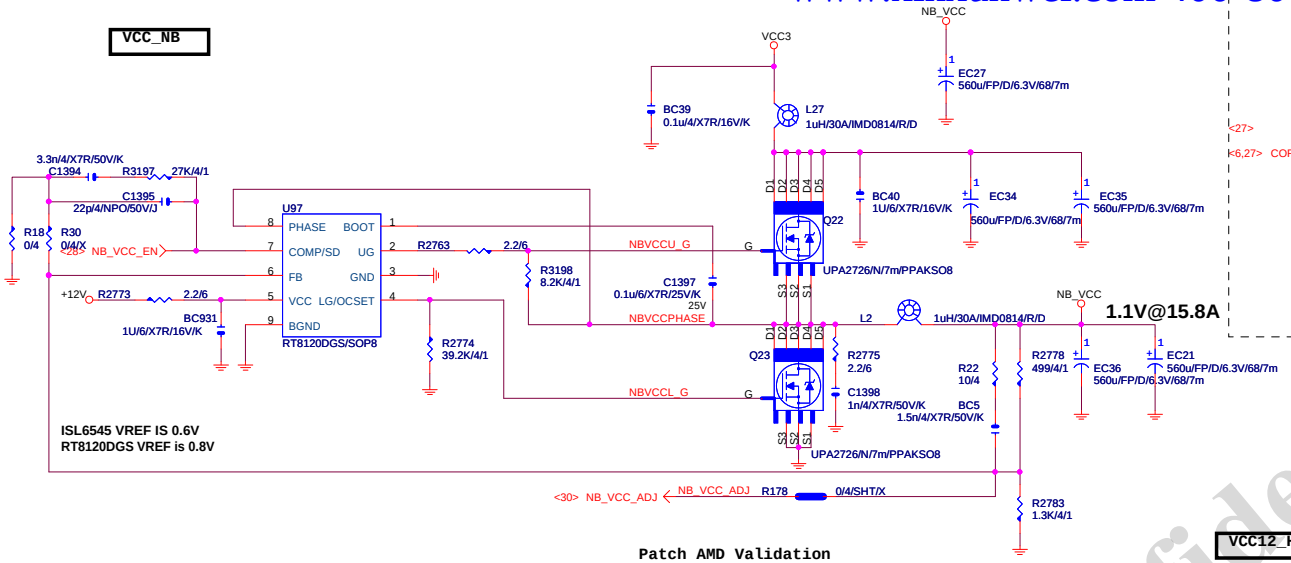
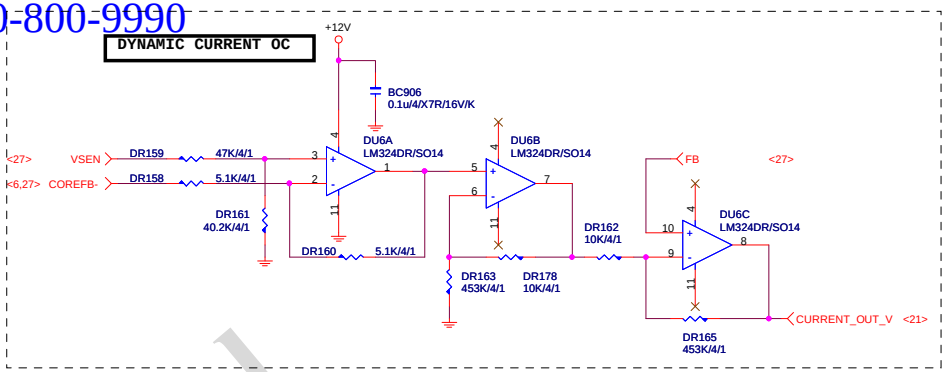
VCC_NB



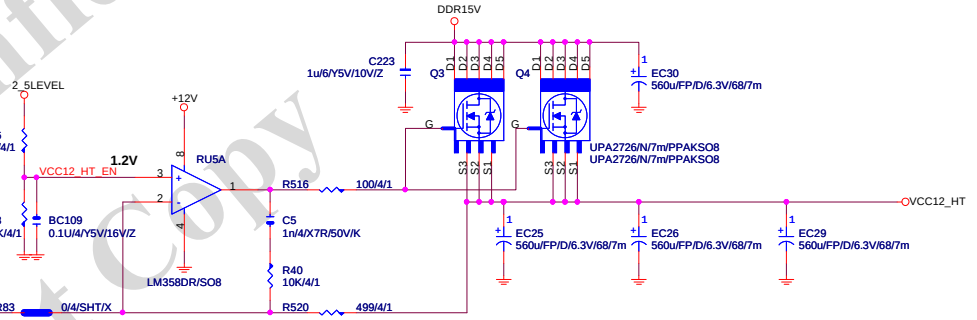
DYNAMIC CURRENT OC



Patch AMD Validation
VDDA25 & VCC12_HT
power sequence

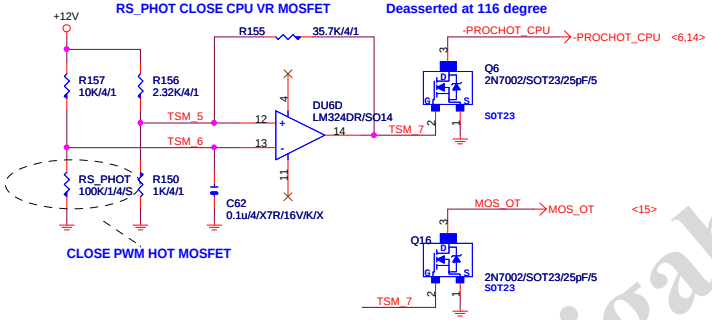
Default change to 1.15V

VCC12_HT



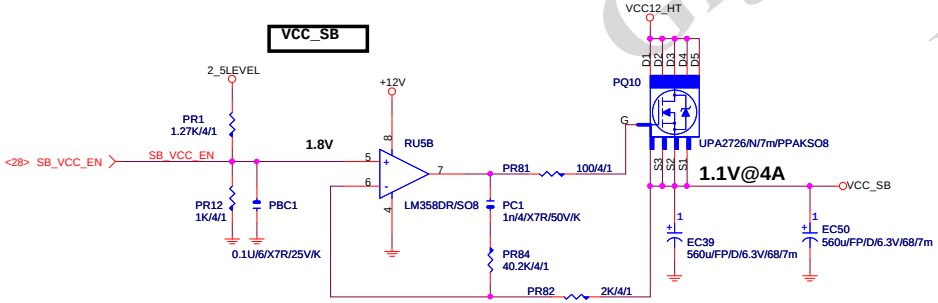
RS_PHOT CLOSE CPU VR MOSFET

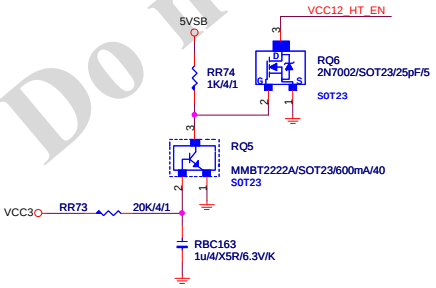
Deasserted at 116 degree



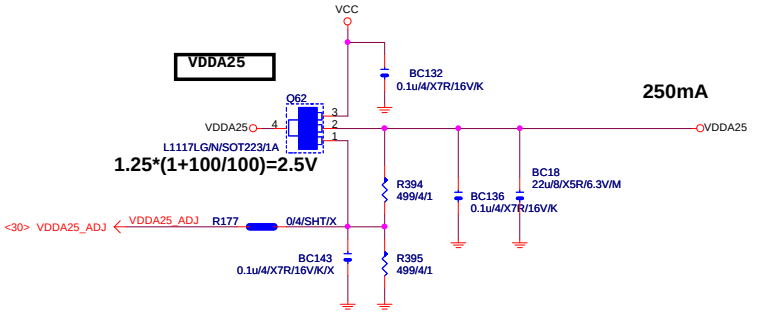
CLOSE PWM HOT MOSFET

VCC_SB





VDDA25



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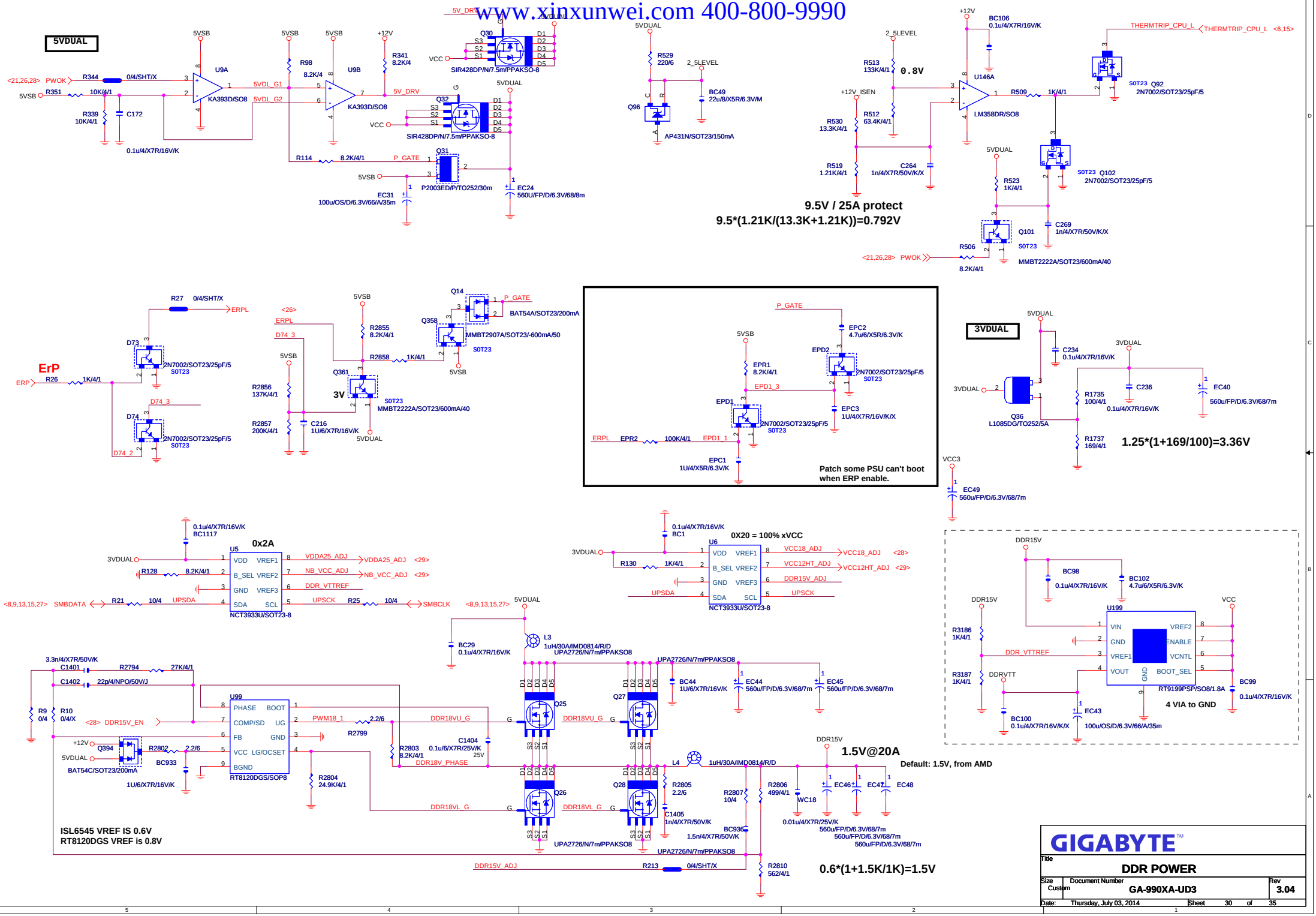

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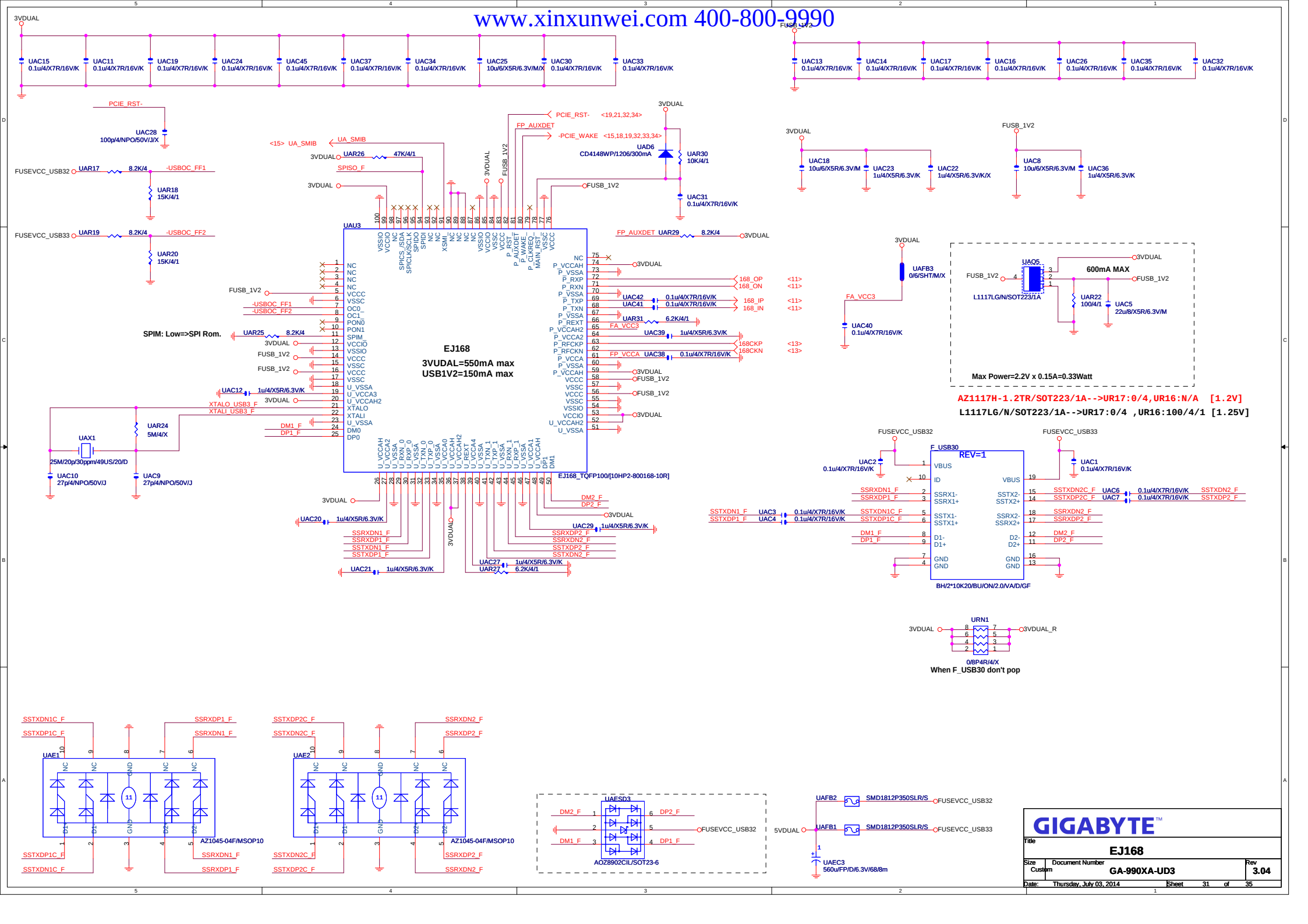

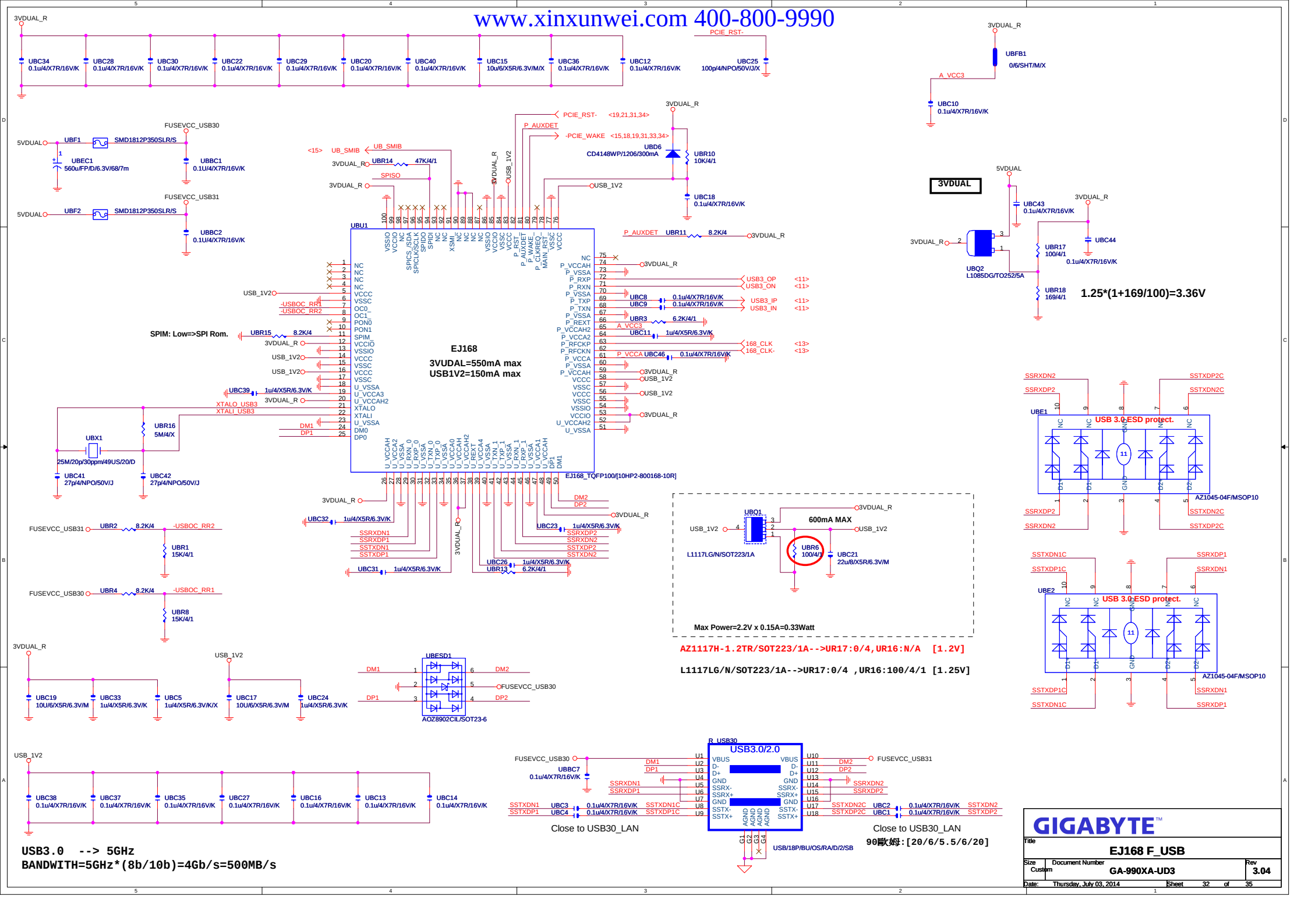

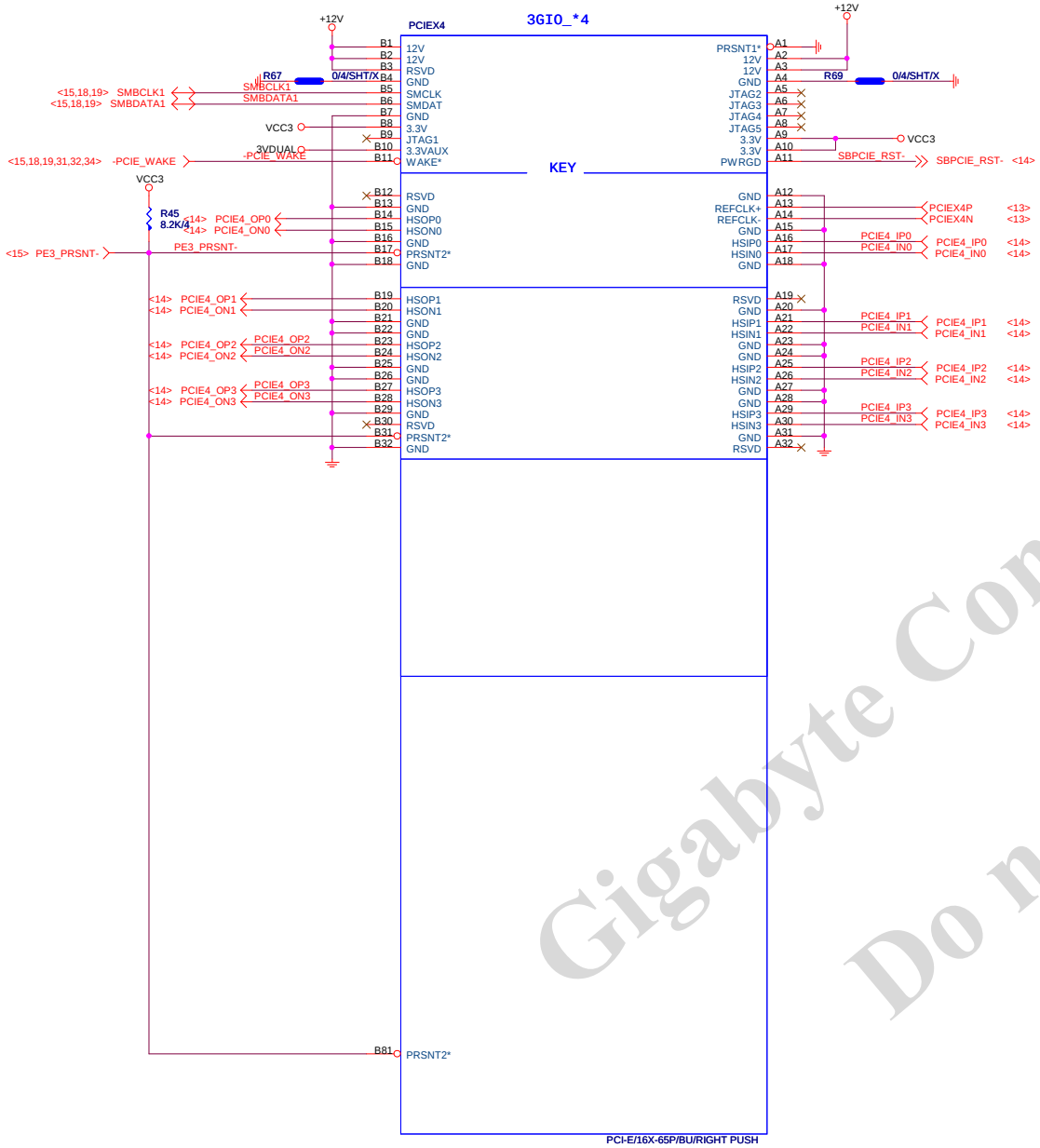

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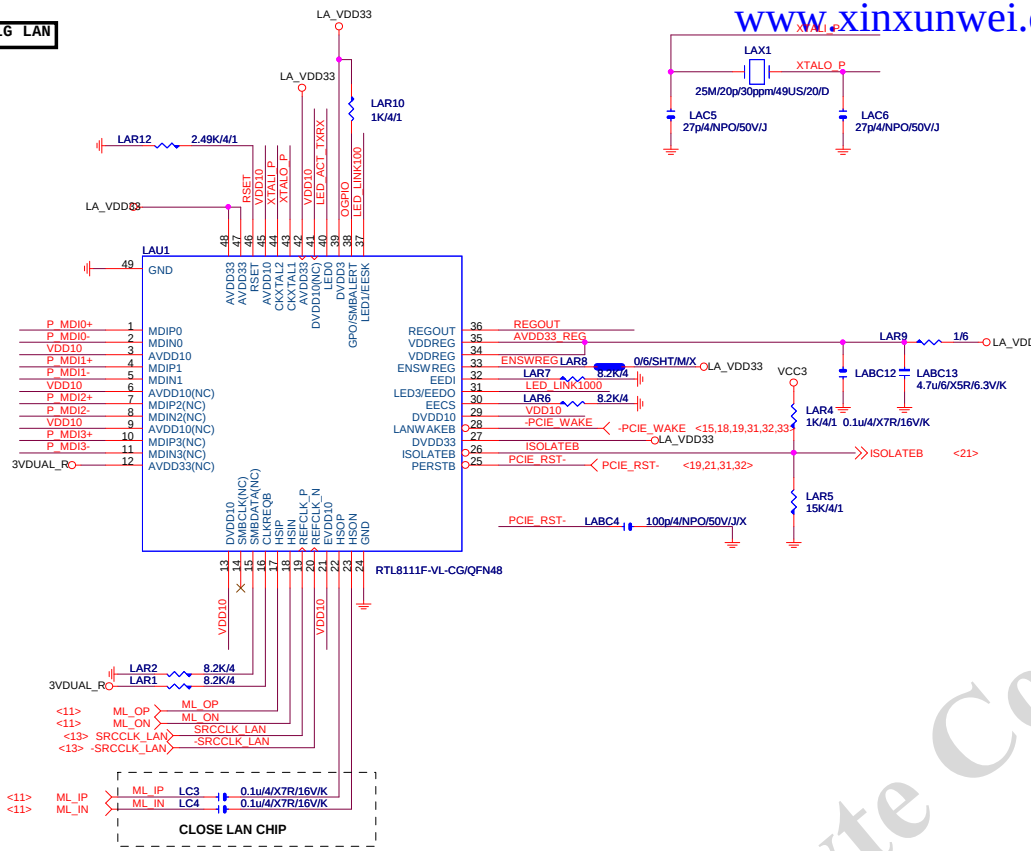
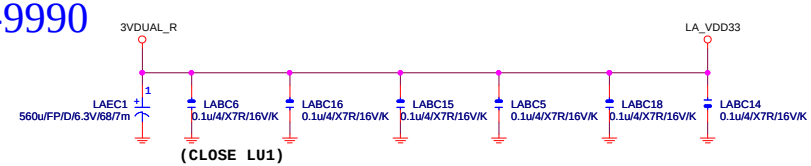
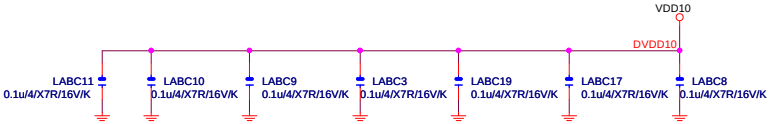
PCIE-1G LAN

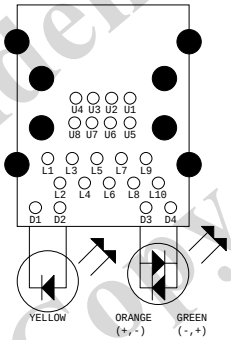


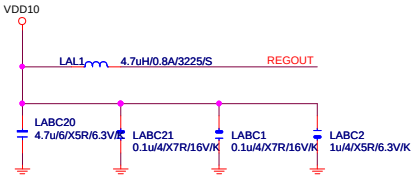




USB_LAN CONNECTOR

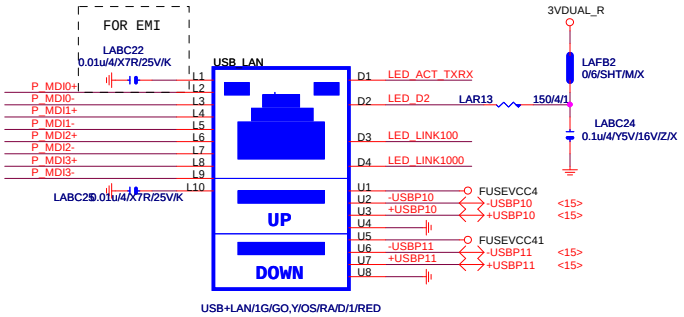
P35-152-19W9

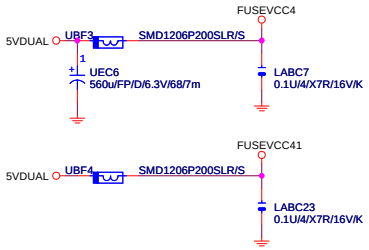


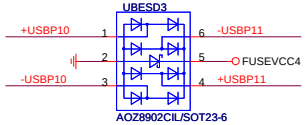


USB_LAN

RTL8101E:LR38/LC5/LR43/LC6-->0
RTL8111C:LC6-->0
RTL8102E:LC5/LC6-->0

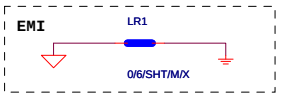






RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)

1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1



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