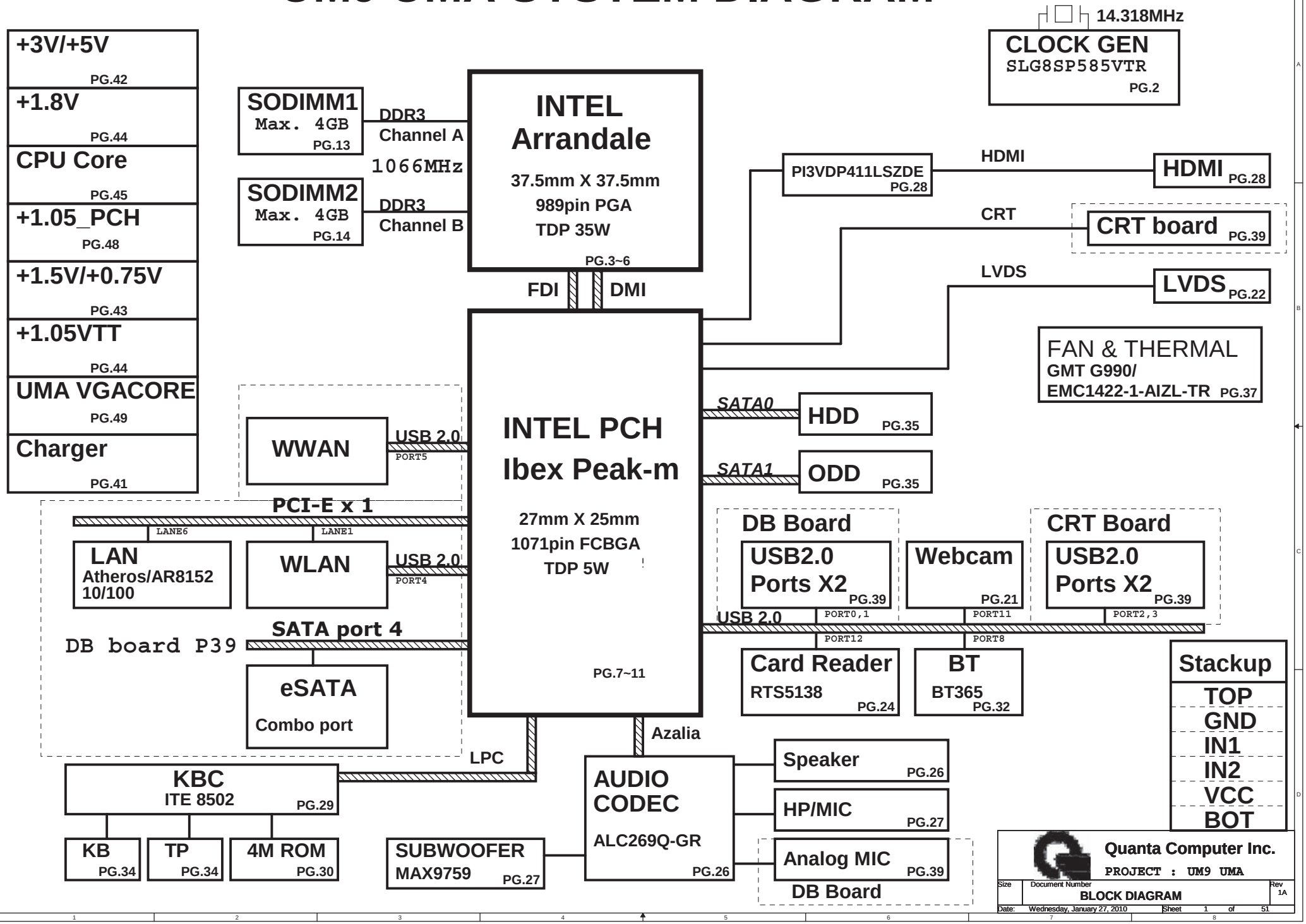
UM9 UMA SYSTEM DIAGRAM



PDC (Power Cap quantities follow UM3)

25mA

+1.05V_PCH — L10 HCB1608KF-181T15_6 — +VDDIO_CLK

C171	0.1U/ 10V
C263	0.1U/ 10V
C176	10U/6.3V_8

Place each 0.1uF cap close to pin

300mA

+3.3V_RUN — L9 HCB1608KF-181T15_6 — +VDDSE_CLK

C165	10U/6.3V_8
C168	0.1U/ 10V
C163	0.1U/ 10V
C164	0.1U/ 10V
C175	0.1U/ 10V
C174	0.1U/ 10V

Place each 0.1uF cap close to pin

U10

CK505
QFN32

+VDDSE_CLK	1	VDD_USB	
	5	VDD_LCD	
	17	VDD_SRC	
	24	VDD_CPU	
	29	VDD_REF	
+VDDIO_CLK	15	VDD_SRC_IO	
	18	VDD_CPU_IO	
	9	VSS_SATA	
	2	VSS_USB	
	8	VSS_LCD	
	12	VSS_SRC	
	21	VSS_CPU	
	26	VSS_REF	
+3.3V_RUN — R218 10K/J_4 — CK_PWRGD_R	16	CPU_STOP#	
	25	CK_PWRGD/PD#_3.3	
(8) CLK_PCH_14M — CLK_PCH_14M — C275 *10P/50V_4_NC — R222 33/J_4 CPU_SEL	30	REF_0/CPU_SEL	
XTAL_OUT	27	XOUT	
XTAL_IN	28	XIN	
(29,37) SMBDAT2	31	SDATA	
(29,37) SMBCLK2	32	SCLK	
CPU-0	23		CLK_BUF_BCLKP (8)
CPU-0#	22		CLK_BUF_BCLKN (8)
CPU-1	20		
CPU-1#	19		
DOT96T_LPR	3		CLK_BUF_DREFCLKP (8)
DOT96C_LPR	4		CLK_BUF_DREFCLKN (8)
SRC-1	13		CLK_BUF_PCIE_3GPLLP (8)
SRC-1#	14		CLK_BUF_PCIE_3GPLLN (8)
SATA	10		CLK_BUF_DREFSSCLKP (8)
SATA#	11		CLK_BUF_DREFSSCLKN (8)
27MHz_nonSS	6		
27MHz_SS	7		
GND	33		

SLG8SP585VTR

Place R8044 within 0.5" of C/G

+3.3V_RUN — R225 *10K/J_4_NC — CPU_SEL — R224 10K/J_4

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

+3.3V_RUN — R216 1K/J_4 — CK_PWRGD_R

(45) VR_PWRGD_CLKEN# — 2N7002W-7-F Q19 — R221 *100K/J_4_NC

C265 50 *100P_NC

Y4

XTAL_IN — 14.318MHZ — XTAL_OUT

C274 33P/50V_4

C272 33P/50V_4

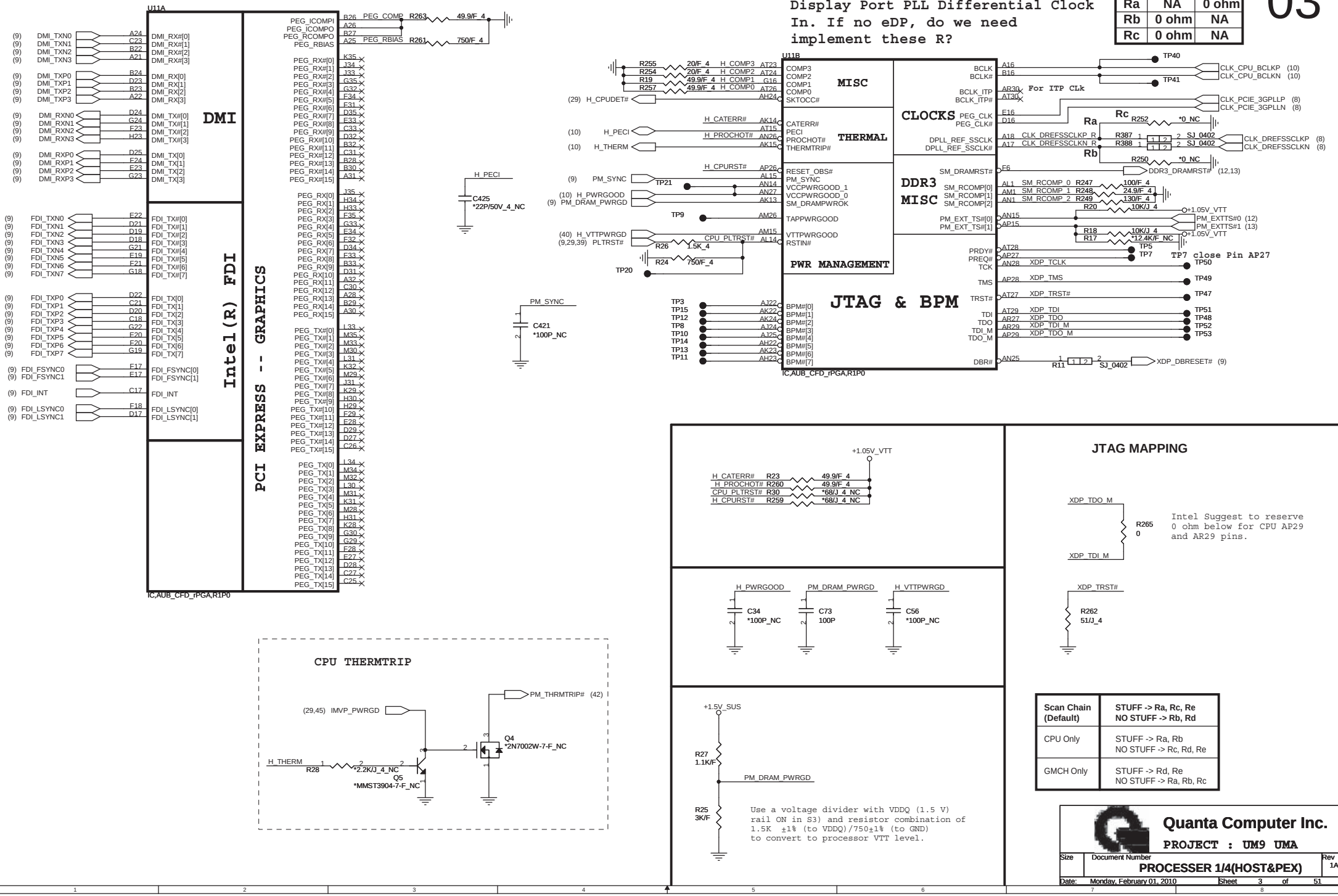
Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number: Clock Gen(ICS9LRS3197AKLFT)	Rev 1A
Date: Monday, February 01, 2010	Sheet 2 of 51	

DPLL_REF_SSCLK:Embedded Display Port PLL Differential Clock In. If no eDP, do we need implement these R?

	DIS	SG
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA



Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

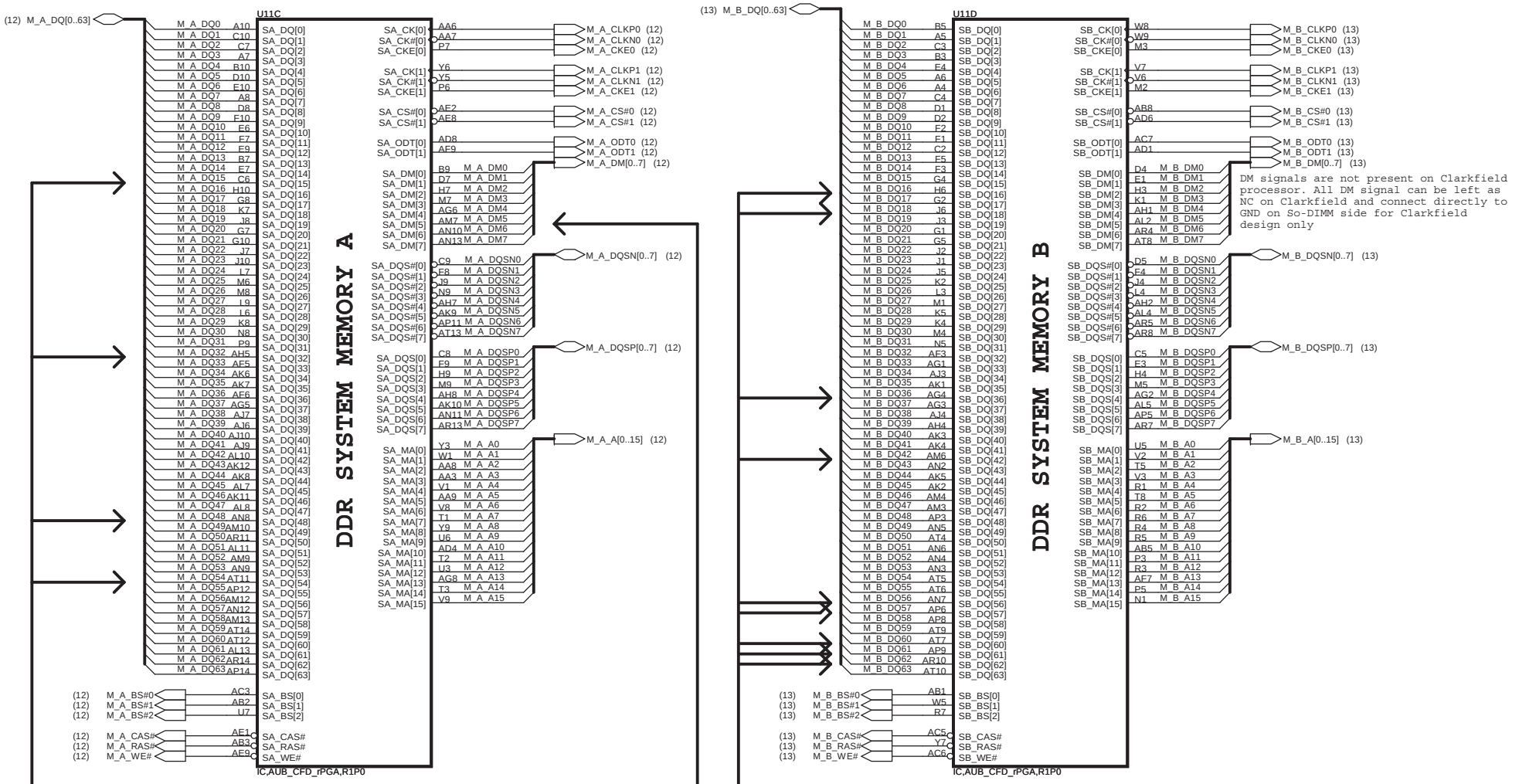
Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	PROCESSER 1/4(HOST&PEX)	1A

Date: Monday, February 01, 2010 Sheet 3 of 51

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	PROCESSER 2/4(DDR)	1A

Date: Monday, February 01, 2010 Sheet 4 of 51

18A

Name different with power

+VCC_CORE

C324 *22U/6.3V_8_NC
C334 *22U/6.3V_8_NC
C330 *22U/6.3V_8_NC
C329 *22U/6.3V_8_NC
C41 *22U/6.3V_8_NC
C40 22U/6.3V_8
C325 22U/6.3V_8
C316 22U/6.3V_8
C333 22U/6.3V_8
C54 22U/6.3V_8
C42 22U/6.3V_8
C336 22U/6.3V_8
C328 *10U/6.3V_8_NC
C32 *10U/6.3V_8_NC
C31 *10U/6.3V_8_NC
C323 *10U/6.3V_8_NC
C53 10U/6.3V_8
C39 10U/6.3V_8
C49 10U/6.3V_8
C30 10U/6.3V_8
C28 10U/6.3V_8
C339 10U/6.3V_8
C317 10U/6.3V_8
C331 10U/6.3V_8
C322 10U/6.3V_8
C55 10U/6.3V_8
C335 10U/6.3V_8
C33 10U/6.3V_8

C29 *470U_NC
C23 *470U_NC

Follow UM3

U11F

CPU CORE SUPPLY

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

IC,AUB_CFD_rPGA,R1P0

POWER

1.1V RAIL POWER

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

+1.05V_VTT

C313 10U/6.3V_8
C311 10U/6.3V_8
C319 10U/6.3V_8
C304 10U/6.3V_8
C44 *10U/6.3V_0805_NC
C315 *10U/6.3V_0805_NC
C45 *10U/6.3V_0805_NC
C62 *10U/6.3V_0805_NC
C65 *10U/6.3V_0805_NC
C309 22U/6.3V_8
C68 22U/6.3V_8
C312 *22U/6.3V_8_NC

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

AF10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

+1.05V_VTT

C64 22U/6.3V_8
C66 22U/6.3V_8

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

CPU VIDS

PSI# AN33 H_PSI# (45)

VID[0] AK35 VID0 (45)
VID[1] AK33 VID1 (45)
VID[2] AK34 VID2 (45)
VID[3] AL35 VID3 (45)
VID[4] AL33 VID4 (45)
VID[5] AM33 VID5 (45)
VID[6] AM35 VID6 (45)
PROC_DPRSLPVR AM34 DPRSLPVR (45)

VTT_SELECT G15 TP17

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

SENSE LINES

ISENSE AN35 I_MON (45)

VTT_SENSE B15 VTT_SENSE (44)
VSS_SENSE_VTT A15 TP16

R281 100/F_4 +VCC_CORE
VCC_SENSE AJ34 VCCSENSE (45)
VSS_SENSE AJ35 VSSSENSE (45)
R280 100/F_4

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

+VCC_GFX_CORE

C43 10U/6.3V_8
C50 10U/6.3V_8

C314 330U/2V_7343
C318 22U/6.3V_8
C321 22U/6.3V_8

U11G

POWER

GRAPHICS

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36

AT21 AT19 AT18 AR21 AR19 AR18 AR16 AP21 AP19 AP18 AP16 AN21 AN19 AN18 AN16 AM21 AM19 AM18 AM16 AL21 AL19 AL18 AL16 AK21 AK19 AK18 AK16 AJ21 AJ19 AJ18 AJ16 AH21 AH19 AH18 AH16

SENSE LINES

VAXG_SENSE AR22 VCC_AXG_SENSE (49)
VSSAXG_SENSE AT22 VSS_AXG_SENSE (49)

GRAPHICS VIDs

GFX_VID[0] AM22 GFXVR_VID_0 (49)
GFX_VID[1] AP22 GFXVR_VID_1 (49)
GFX_VID[2] AN22 GFXVR_VID_2 (49)
GFX_VID[3] AP23 GFXVR_VID_3 (49)
GFX_VID[4] AM23 GFXVR_VID_4 (49)
GFX_VID[5] AP24 GFXVR_VID_5 (49)
GFX_VID[6] AN24 GFXVR_VID_6 (49)

R258 4.7K/F_4

GFX_VR_EN AR25 GFXVR_EN GFXVR_EN (49)
GFX_DPRSLPVR AT25
GFX_IMON AM24 GFXVR_IMON (49)

R10 *1K/F_4_NC

2A

DDR3 - 1.5V RAILS

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18

AJ1 AF1 AE7 AE4 AC1 AB7 AB4 Y1 W7 W4 U1 T7 T4 P1 N7 N4 L1 H1

+1.5V_SUS

C71 1U/6.3V
C70 1U/6.3V
C69 1U/6.3V
C72 1U/6.3V
C75 1U/6.3V
C76 22U/6.3V_8
C74 22U/6.3V_8

C77 330U/2V_7343

FDI

+1.05V_VTT

C67 22U/6.3V_8
C52 22U/6.3V_8

VTT1_45 VTT1_46 VTT1_47

J24 J23 H25

PEG & DMI

+1.05V_VTT

C305 22U/6.3V_8
C306 22U/6.3V_8
C307 22U/6.3V_8
C63 *22U/6.3V_8_NC

VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58

K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25

1.1V

VTT0_59 VTT0_60 VTT0_61 VTT0_62 VTT1_63 VTT1_64 VTT1_65 VTT1_66 VTT1_67 VTT1_68

P10 N10 L10 K10 J22 J20 J18 H21 H20 H19

+1.05V_VTT

C310 10U/6.3V_8
C308 *10U/6.3V_0805_NC
C51 22U/6.3V_8
C320 *22U/6.3V_8_NC

1.8V

VCCPLL1 VCCPLL2 VCCPLL3

L26 L27 M26

+1.8V_RUN

C38 22U/6.3V_8
C37 4.7U/6.3V
C327 2.2U/ 6.3V
C36 1U/6.3V
C326 1U/6.3V

IC,AUB_CFD_rPGA,R1P0

VID0 R282 1K/J_4 R271 *1K/J_4_NC +1.05V_VTT
VID1 R284 1K/J_4 R273 *1K/J_4_NC
VID2 R283 1K/J_4 R272 *1K/J_4_NC
VID3 R285 1K/J_4 R274 *1K/J_4_NC
VID4 R288 1K/J_4 R277 *1K/J_4_NC
VID5 R289 1K/J_4 R279 *1K/J_4_NC
VID6 R286 1K/J_4 R275 *1K/J_4_NC
DPRSLPVR R287 1K/J_4 R276 *1K/J_4_NC
H_PSI# R270 *1K/J_4_NC R268 1K/J_4

C341 *100P_NC

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

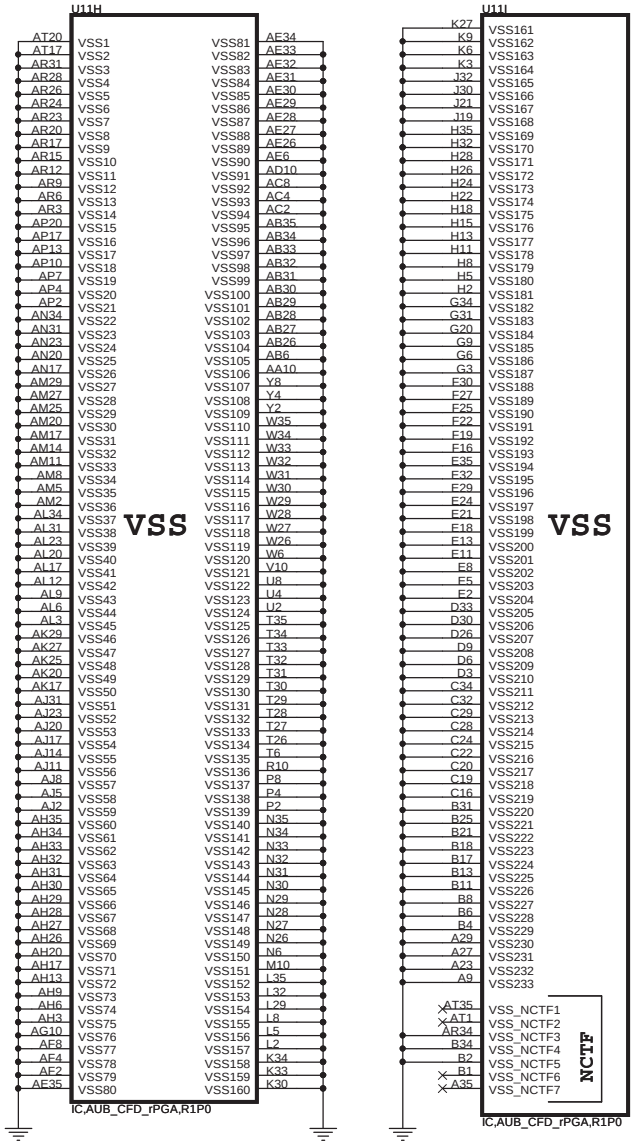
C397 close to R8361

Quanta Computer Inc.

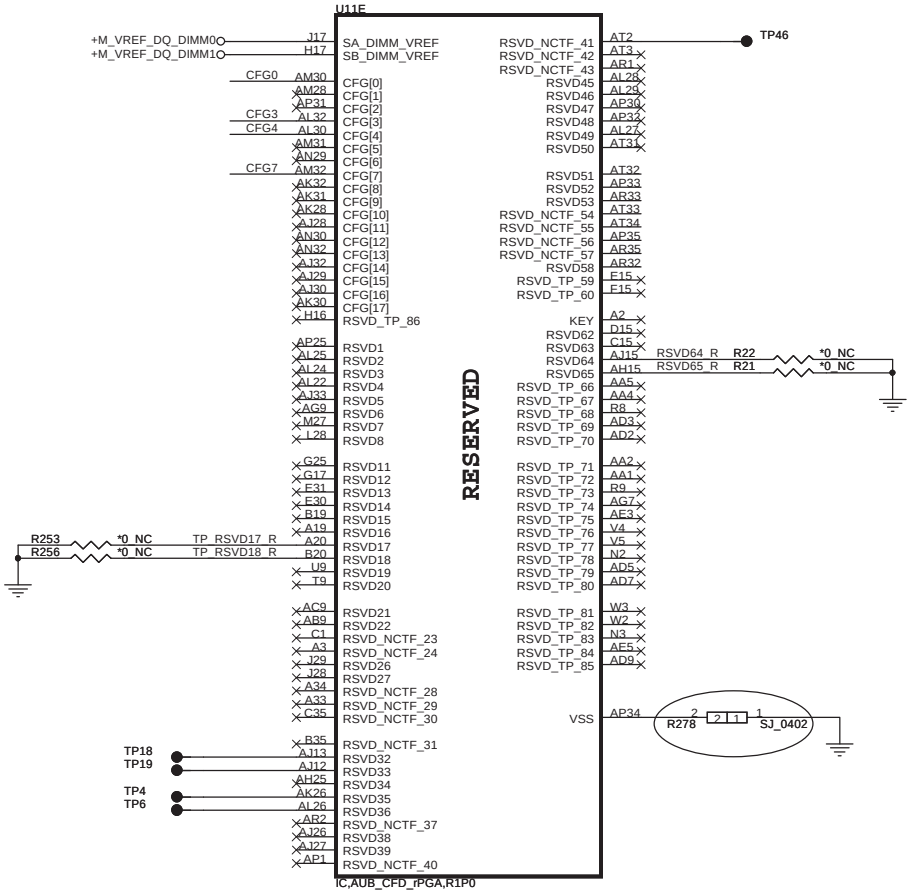
PROJECT : UM9 UMA

Size	Document Number	Rev
	PROCESSER 3/4(POWER)	1A
Date: Monday, February 01, 2010	Sheet 5 of 51	

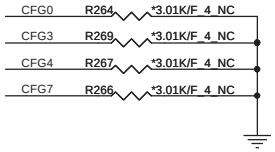
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

For Discrete only

CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

Quanta Computer Inc.
PROJECT : UM9 UMA

Size	Document Number	Rev
	PROCESSER 4/4 (GND)	1A

Date: Wednesday, January 27, 2010 Sheet 6 of 51

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U9A

Ibex-M 1 OF 10

RTC
LPC
IHDA
JTAG
SATA
SPI

HDD
ODD
ESATA

DG: Place TX cap close to connector

SATA port 2/3 are not support in HM55 .
They are only in PM 55

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

must add test point.

IbexPeak-M_Rev1_0

UMA CRT,LVDS&HDMI signals

IBEX PEAK-M (LVDS,DDI)

U9D

Ibex-M 4 OF 10

SDVO
Digital Display Interface
DISPLAY PORT B
DISPLAY PORT C
DISPLAY PORT D
LVDS--A
LVDS--B
CRT

R8337 (IREF), UMA:0.5% ,DIS:5%
Sch check list 2.0 use 5% R

IbexPeak-M_Rev1_0

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

iTPM ENABLE/DISABLE

From UM3

TPM Function	
Enable	Mount
Disable	NC (Default)

Close to VGA side

UMA:CRT 55ohm, UMA CRT display ripple issue.

Leon 11/30

For UMA HDMI Function

Q14 2N7002K-T1-E3

For AUDIO

No Reboot strap.

SPKR	Low = Default. High = No Reboot.

RTC

1mA

FM9, UM3 use 1%

Res. of TDI near PCH

JTAG_TDI, JTAG_TMS, TRST# Internal 20K PU.
JTAG_TCK Internal 20K PD

From UM3

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

NC all Res. when PCH is production stage.

Res. of RST#
PCH ES1 stage : pop
PCH ES2 stage : NC

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	1A
Date: Monday, February 01, 2010	Sheet 7 of 51	

IBEX PEAK-M (GND)

U9I

AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BG12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	N38
BB42	VSS[178]	VSS[278]	M34
BB49	VSS[179]	VSS[279]	M38
BB5	VSS[180]	VSS[280]	M42
BC10	VSS[181]	VSS[281]	M46
BC14	VSS[182]	VSS[282]	M49
BC18	VSS[183]	VSS[283]	M5
BC2	VSS[184]	VSS[284]	M8
BC22	VSS[185]	VSS[285]	N24
BC32	VSS[186]	VSS[286]	P11
BC36	VSS[187]	VSS[287]	AD15
BC40	VSS[188]	VSS[288]	P22
BC44	VSS[189]	VSS[289]	P30
BC52	VSS[190]	VSS[290]	P32
BH9	VSS[191]	VSS[291]	P34
BD48	VSS[192]	VSS[292]	P42
BD49	VSS[193]	VSS[293]	P45
BD5	VSS[194]	VSS[294]	P47
BE12	VSS[195]	VSS[295]	R2
BE16	VSS[196]	VSS[296]	R52
BE20	VSS[197]	VSS[297]	T12
BE24	VSS[198]	VSS[298]	T41
BE30	VSS[199]	VSS[299]	T46
BE34	VSS[200]	VSS[300]	T49
BE38	VSS[201]	VSS[301]	T5
BE42	VSS[202]	VSS[302]	U30
BE46	VSS[203]	VSS[303]	U31
BE48	VSS[204]	VSS[304]	U32
BE50	VSS[205]	VSS[305]	U34
BE6	VSS[206]	VSS[306]	P38
BE8	VSS[207]	VSS[307]	V11
BF3	VSS[208]	VSS[308]	P16
BF49	VSS[209]	VSS[309]	V19
BF51	VSS[210]	VSS[310]	V20
BG18	VSS[211]	VSS[311]	V22
BG24	VSS[212]	VSS[312]	V30
BG4	VSS[213]	VSS[313]	V31
BG50	VSS[214]	VSS[314]	V32
BH11	VSS[215]	VSS[315]	V34
BH15	VSS[216]	VSS[316]	V35
BH19	VSS[217]	VSS[317]	V38
BH23	VSS[218]	VSS[318]	V43
BH31	VSS[219]	VSS[319]	V45
BH35	VSS[220]	VSS[320]	V46
BH39	VSS[221]	VSS[321]	V47
BH43	VSS[222]	VSS[322]	V49
BH47	VSS[223]	VSS[323]	V5
BH7	VSS[224]	VSS[324]	V7
C12	VSS[225]	VSS[325]	V8
C50	VSS[226]	VSS[326]	W2
D51	VSS[227]	VSS[327]	W52
E12	VSS[228]	VSS[328]	Y11
E16	VSS[229]	VSS[329]	Y12
E20	VSS[230]	VSS[330]	Y15
E24	VSS[231]	VSS[331]	Y19
E30	VSS[232]	VSS[332]	Y23
E34	VSS[233]	VSS[333]	Y28
E38	VSS[234]	VSS[334]	Y30
E42	VSS[235]	VSS[335]	Y31
E46	VSS[236]	VSS[336]	Y32
E48	VSS[237]	VSS[337]	Y38
E6	VSS[238]	VSS[338]	Y43
E8	VSS[239]	VSS[339]	Y46
F49	VSS[240]	VSS[340]	P49
F5	VSS[241]	VSS[341]	Y5
G10	VSS[242]	VSS[342]	Y6
G14	VSS[243]	VSS[343]	Y8
G18	VSS[244]	VSS[344]	P24
G2	VSS[245]	VSS[345]	T43
G22	VSS[246]	VSS[346]	AD51
G32	VSS[247]	VSS[347]	AT8
G36	VSS[248]	VSS[348]	AD47
G40	VSS[249]	VSS[349]	Y47
G44	VSS[250]	VSS[350]	AT12
G52	VSS[251]	VSS[351]	AM6
AF39	VSS[252]	VSS[352]	AT13
H16	VSS[253]	VSS[353]	AM5
H20	VSS[254]	VSS[354]	AK45
H30	VSS[255]	VSS[355]	AK39
H34	VSS[256]	VSS[356]	AV14
H38	VSS[257]	VSS[366]	
H42	VSS[258]		

IbexPeak-M_Rev1_0

+3.3V_RUN

PCIE_CLK_REQ1# R208 10K
PCIE_CLK_REQ2# R199 10K

+3.3V_SUS

PCIE_CLK_REQ0# R127 10K
PCIE_CLK_REQ3# R176 10K
PCIE_CLK_REQ4# R131 10K
PCIE_CLK_REQB#_R R115 10K
PCIE_CLK_REQ5# R133 10K
PEG_CLKREQ# R180 10K

2N7002W-7-F
Q18

SMB_CLK_ME1 → SMBCLK1 (29)

+3.3V_SUS

SMB_DATA_ME1 → SMBDAT1 (29)

Q17
2N7002W-7-F

+3.3V_RUN

RP7
2.2KX2

Q15
2N7002W-7-F

(12,13,39) WLAN_SMBCLK → ICH_SMBCLK

+3.3V_RUN

Q16
2N7002W-7-F

(12,13,39) WLAN_SMBDATA → ICH_SMBDATA

IBEX PEAK-M (PCI-E,SMBUS,CLK)

U9B

Ibex-M
2 OF 10

PCI-E*

[WWAN]

[WLAN]

(39) PCIE_RXN1 → PCIE_RXN1 AW30
(39) PCIE_RXP1 → PCIE_RXP1 BA30
(39) PCIE_TXN1 → C183 0.1U/10V → PCIE_TXN1_C BC30
(39) PCIE_TXP1 → C182 0.1U/10V → PCIE_TXP1_C BD30

[LAN]

(39) PCIE_RXN6_LAN → PCIE_RXN6_LAN BA34
(39) PCIE_RXP6_LAN → PCIE_RXP6_LAN AW34
(39) PCIE_TXN6_LAN → C154 0.1U/10V → PCIE_TXN6_LAN_C BC34
(39) PCIE_TXP6_LAN → C160 0.1U/10V → PCIE_TXP6_LAN_C BD34

PCIECLKRQ0#/GPIO73 Internal 20K PU

MiniWLAN

(39) CLK_PCIE_WLANN → AM43
(39) CLK_PCIE_WLANP → AM45
(39) PCIE_CLK_REQ1# → U4

MiniWWAN

LAN

(39) CLK_PCIE_LANN → AK53
(39) CLK_PCIE_LANP → AK51
(39) PCIE_CLK_REQB#_R → PCIE_CLK_REQB#_R P13

BG30	PERN1	
BJ30	PERP1	
BF29	PETN1	
BH29	PETP1	
AU30	PERN2	
AT30	PERP2	
AU32	PETN2	
AV32	PETP2	
BA32	PERN3	
BB32	PERP3	
BD32	PETN3	
BE32	PETP3	
BF33	PERN4	
BH33	PERP4	
BG32	PETN4	
BJ32	PETP4	
BA34	PERN5	
AW34	PERP5	
BC34	PETN5	
BD34	PETP5	
AT34	PERN6	
AU34	PERP6	
AU36	PETN6	
AV36	PETP6	
BG34	PERN7	
BJ34	PERP7	
BG36	PETN7	
BJ36	PETP7	
AK48	PERN8	
AK47	PERP8	
	PETN8	
	PETP8	
	CLKOUT_PCIE0N	
	CLKOUT_PCIE0P	
AM43	CLKOUT_PCIE1N	
AM45	CLKOUT_PCIE1P	
U4	PCIECLKRQ1# / GPIO18	(+3V)
AM47	CLKOUT_PCIE2N	
AM48	CLKOUT_PCIE2P	
N4	PCIECLKRQ2# / GPIO20	(+3V)
AH42	CLKOUT_PCIE3N	
AH41	CLKOUT_PCIE3P	
A8	PCIECLKRQ3# / GPIO25	(+3V_S5)
AM51	CLKOUT_PCIE4N	
AM53	CLKOUT_PCIE4P	
M9	PCIECLKRQ4# / GPIO26	(+3V_S5)
AJ50	CLKOUT_PCIE5N	
AJ52	CLKOUT_PCIE5P	
H6	PCIECLKRQ5# / GPIO44	(+3V_S5)
AK53	CLKOUT_PEG_B_N	
AK51	CLKOUT_PEG_B_P	
P13	PEG_B_CLKRQ# / GPIO56	(+3V_S5)

IbexPeak-M_Rev1_0

PCIE_CLK_REQ0# → P9

+3.3V_SUS

SMBus

(+3V_S5)	SMBALERT# / GPIO11	B9	SMBALERT#	10K/J_4 R175
	SMBCLK	H14	ICH_SMBCLK	2.2K/J_4 R150
	SMBDATA	C8	ICH_SMBDATA	2.2K/J_4 R147
(+3V_S5)	SML0ALERT# / GPIO60	J14	SMBL0ALERT#	10K/J_4 R146
	SML0CLK	C6	SMB_CLK_ME0	2.2K/J_4 R137
	SML0DATA	G8	SMB_DATA_ME0	2.2K/J_4 R138
(+3V_S5)	SML1ALERT# / GPIO74	M14	SML1ALERT#	10K/J_4 R125
(+3V_S5)	SML1CLK / GPIO58	F10	SMB_CLK_ME1	2.2K/J_4 R154
(+3V_S5)	SML1DATA / GPIO75	G12	SMB_DATA_ME1	2.2K/J_4 R153

Controller Link

CL_CLK1 T13
CL_DATA1 T11
CL_RST1# T9

PEG

(+3V_S5) PEG_A_CLKRQ# / GPIO47 H1 PEG_CLKREQ#
CLKOUT_PEG_A_N AD43
CLKOUT_PEG_A_P AD45
CLKOUT_DMI_N AN4 → CLK_PCIE_3GPLLN (3)
CLKOUT_DMI_P AN2 → CLK_PCIE_3GPLLP (3)

From CLK BUFFER

CLKOUT_DP_N / CLKOUT_BCLK1_N AT1 → CLK_DREFSSCLKN (3)
CLKOUT_DP_P / CLKOUT_BCLK1_P AT3 → CLK_DREFSSCLKP (3)
CLKIN_DMI_N AW24 → CLK_BUF_PCIE_3GPLLN (2)
CLKIN_DMI_P BA24 → CLK_BUF_PCIE_3GPLLP (2)
CLKIN_BCLK_N AP3 → CLK_BUF_BCLKN (2)
CLKIN_BCLK_P AP1 → CLK_BUF_BCLKP (2)
CLKIN_DOT_96N F18 → CLK_BUF_DREFCLKN (2)
CLKIN_DOT_96P E18 → CLK_BUF_DREFCLKP (2)
CLKIN_SATA_N / CKSSCD_N AH13 → CLK_BUF_DREFSSCLKN (2)
CLKIN_SATA_P / CKSSCD_P AH12 → CLK_BUF_DREFSSCLKP (2)
REFCLK14IN P41 → CLK_PCH_14M (2)
CLKIN_PCILOOPBACK J42 CLK_PCI_FB → CLK_PCI_FB (9)
XTAL25_IN AH51
XTAL25_OUT AH53
XCLK_RCOMP AF38 XCLK_RCOMP R105 90.9/F_4 +1.05V_PCH

C214 *5.6P/50V_4_NC
T22
Intel recommendation
R223 *0_NC
RC0402

Clock Flex

(+3V) CLKOUTFLEX0 / GPIO64 T45 CLK_FLEX0 T19
(+3V) CLKOUTFLEX1 / GPIO65 P43 CLK_FLEX1 T20
(+3V) CLKOUTFLEX2 / GPIO66 T42 CLK_FLEX2 T17
(+3V) CLKOUTFLEX3 / GPIO67 N50 CLK_FLEX3 R192 22/J_4 → CLK_48M_CARD (25)

C244
10P/50V_4

R502 1M/F_4
XTAL25_IN — Y5 — XTAL25_OUT
C271 27P 50 NPO
25MHz
C270 27P 50 NPO
For UMA

Quanta Computer Inc.		
PROJECT : UM9 UMA		
Size	Document Number	Rev
	PCH 2/5 (PCIE, SMBUS, CK)	1A
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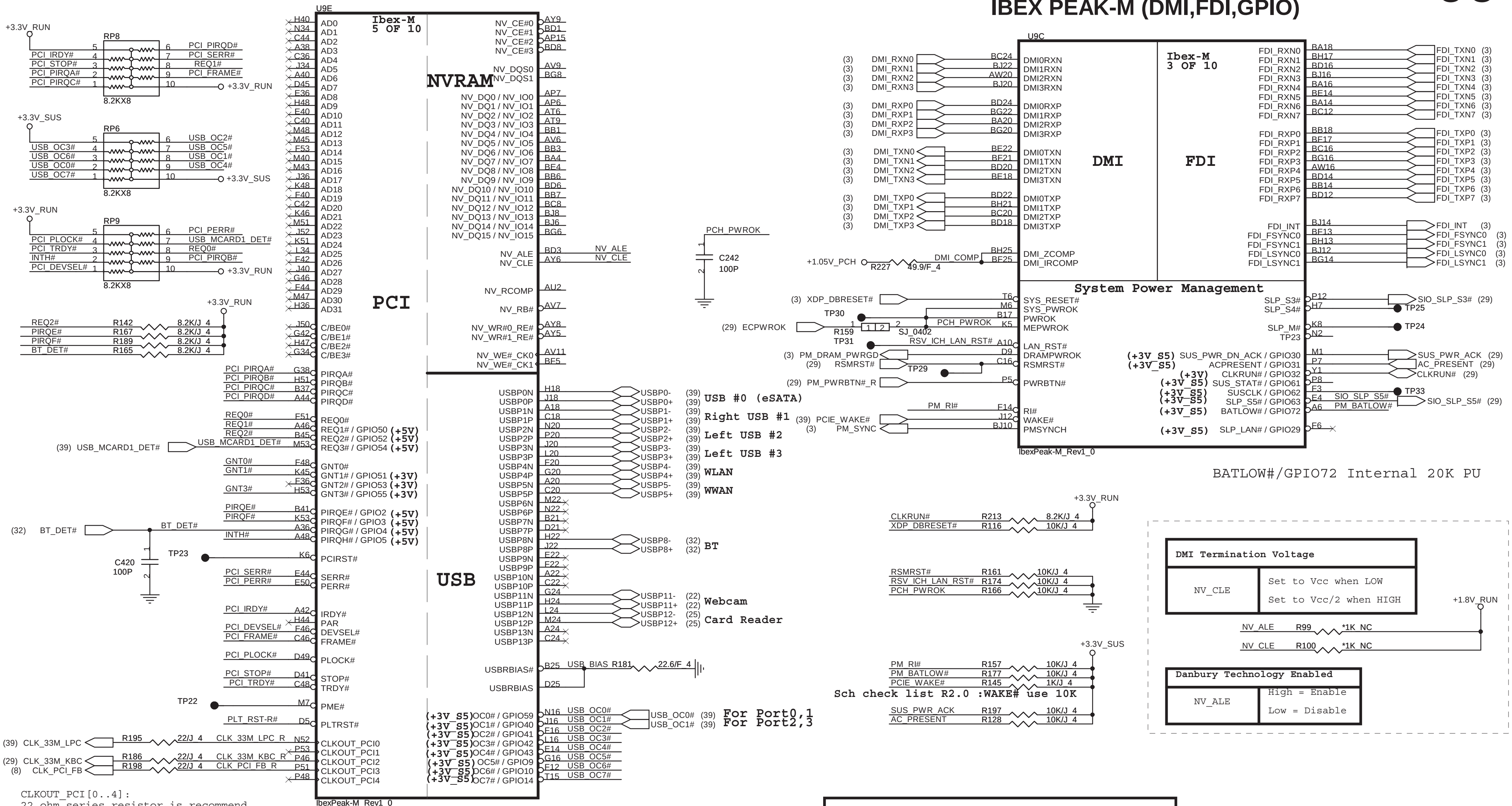
http://hobi-elektronika.net

IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)



BATLOW#/GPIO72 Internal 20K PU

CLKOUT_PCI[0..4]:
22 ohm series resistor is recommend
(single & double load) on PDG v1.1

Reserve capacitor pads for improving WWAN.

CLK_33M_KBC C243 10P/50V_4
CLK_33M_LPC C245 10P/50V_4

DMI Termination Voltage

NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Danbury Technology Enabled

NV_ALE	High = Enable Low = Disable

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Check

Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)	1A

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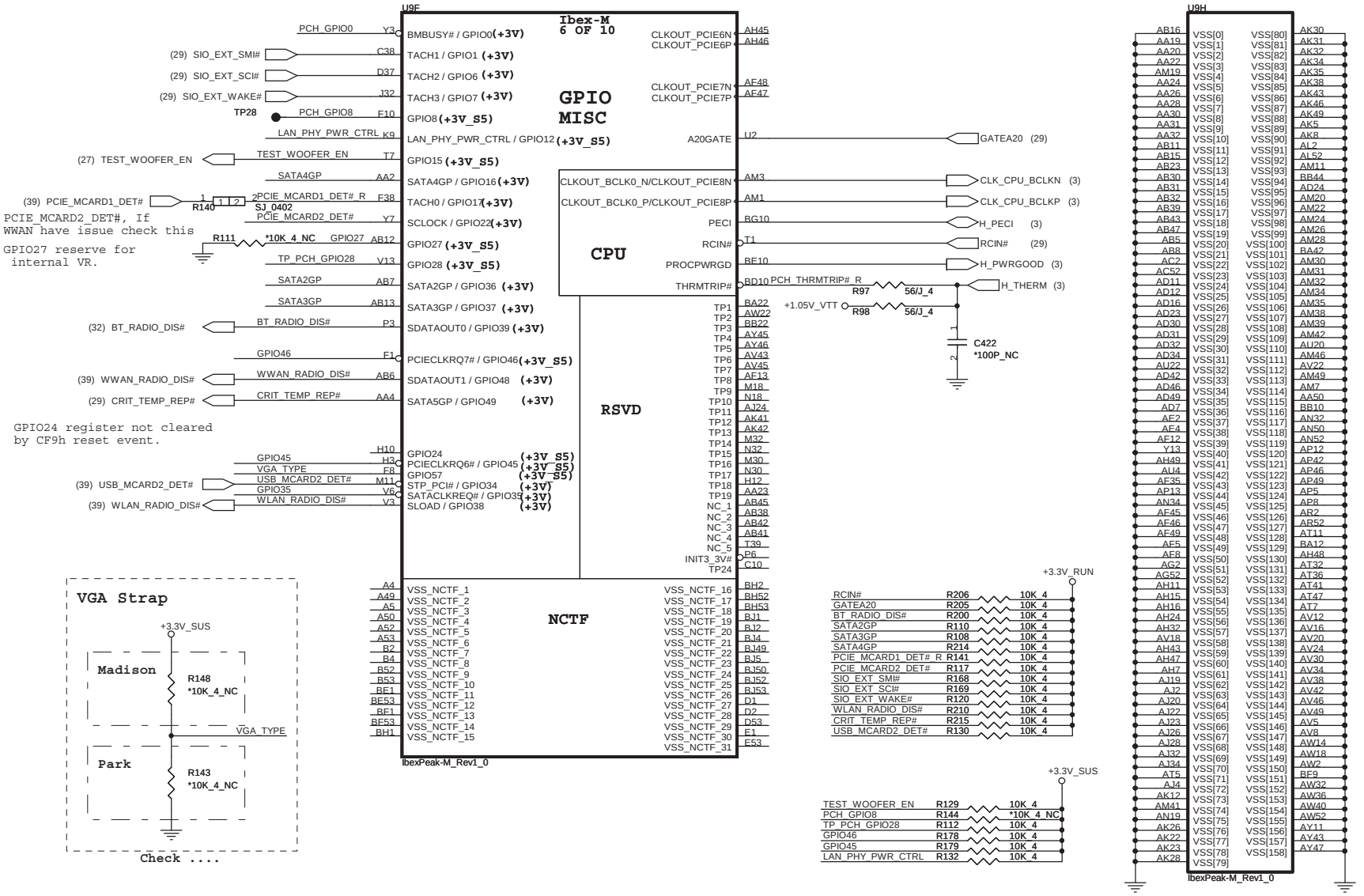
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)



R124 10K_4 GPIO35

GPIO[7,6,1,17], PCIECLKRQ6#/GPIO45, GPIO28 Internal 20K PU

+3.3V_RUN
PCH_GPIO0 R212 10K_4
WWAN_RADIO_DIS# R114 10K_4

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up (8.2~ KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

WWAN_RADIO_DIS#	1-X High = Strong (Default)

Flash Descriptor Security Override	
GPIO33	Low = Enabled High = Disabled

(7,29) PCH_MELOCK R121 *1K/J_4_NC

(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	1A
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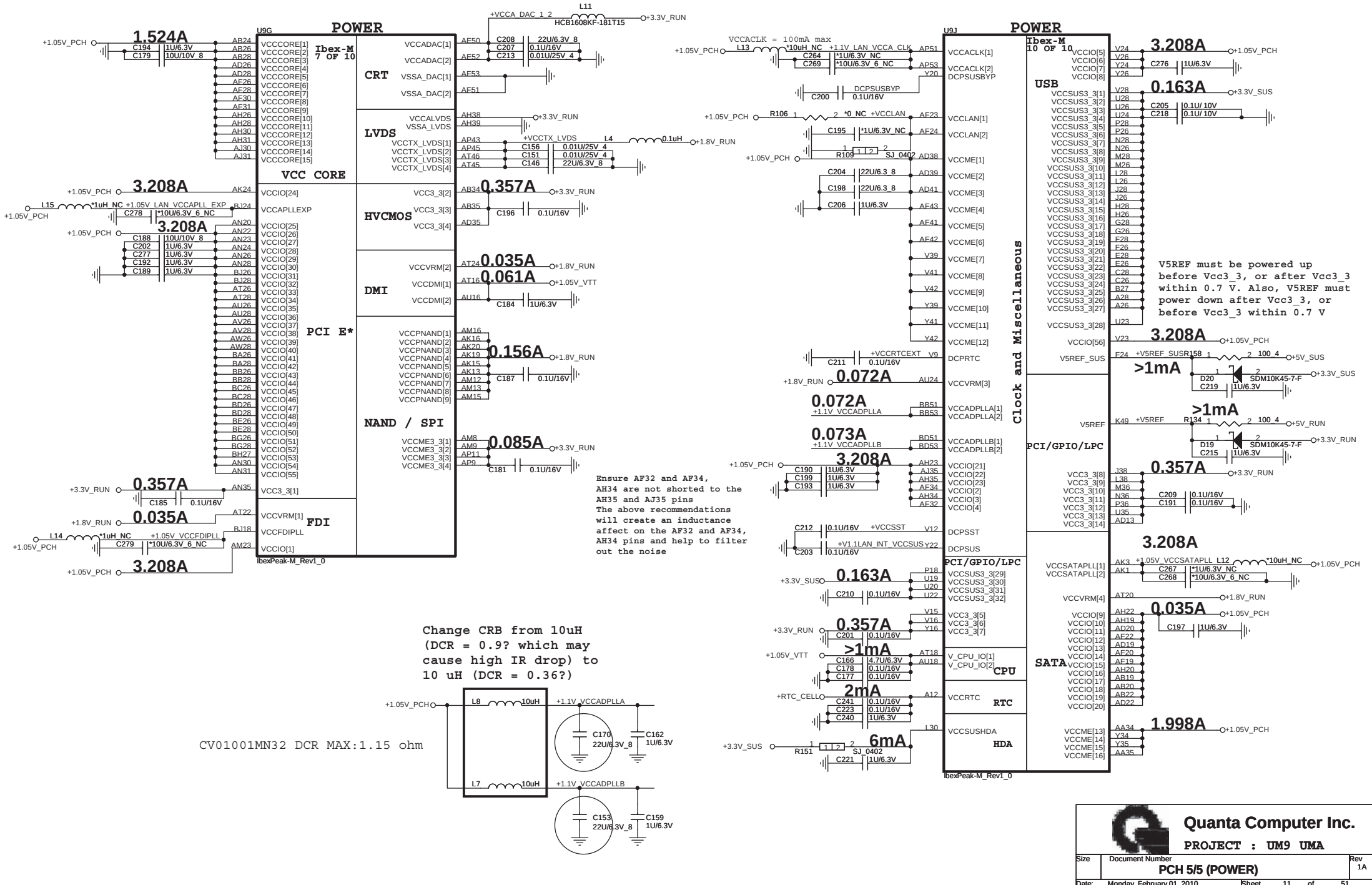
Cap quantities follow UM3

C8335 UMA:22u, DIS:10u, solve UMA CRT display ripple issue.



Quanta Computer Inc.			
PROJECT : UM9 UMA			
Size	Document Number		Rev
	PCH 5/5 (POWER)		1A
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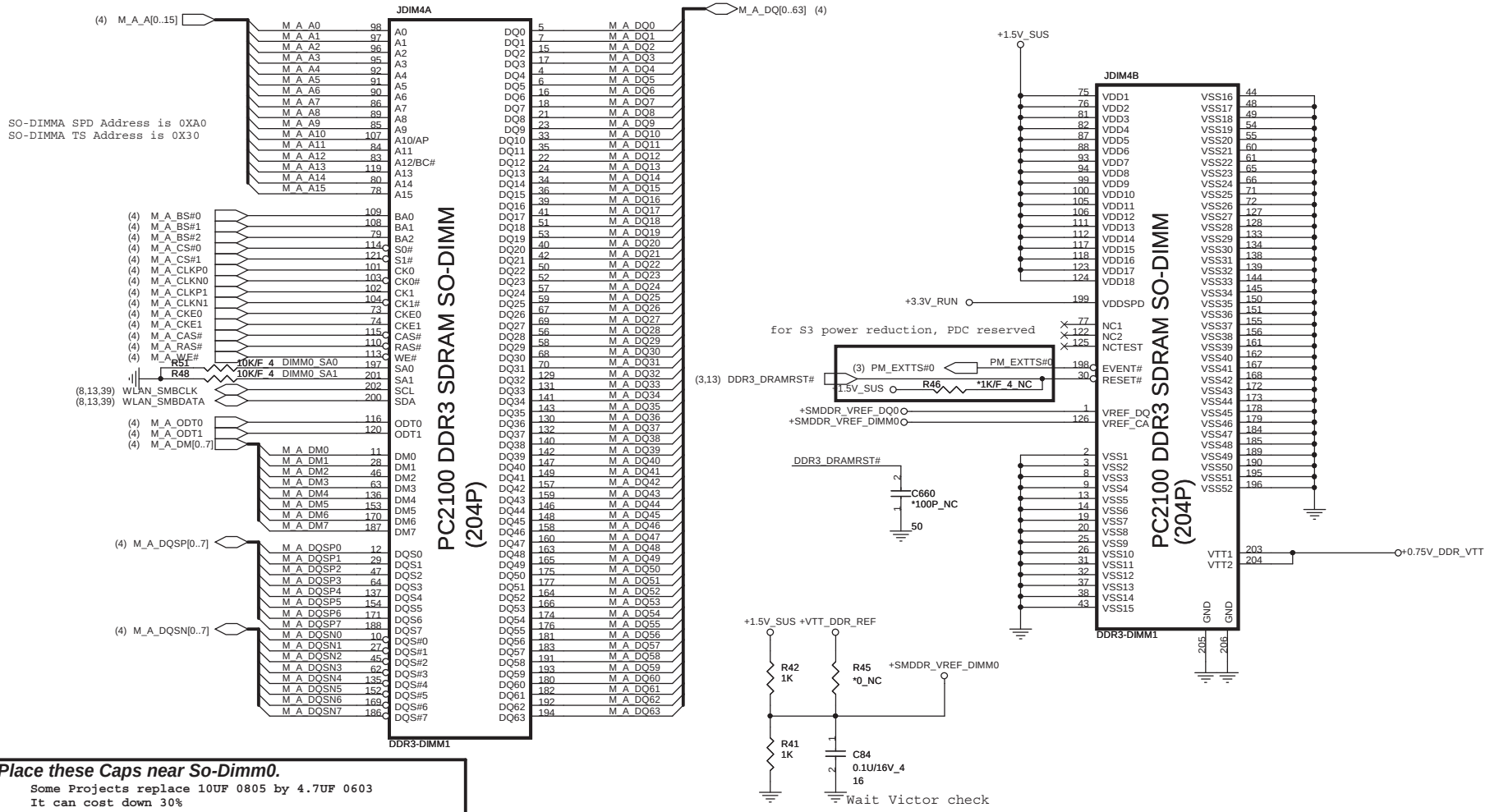
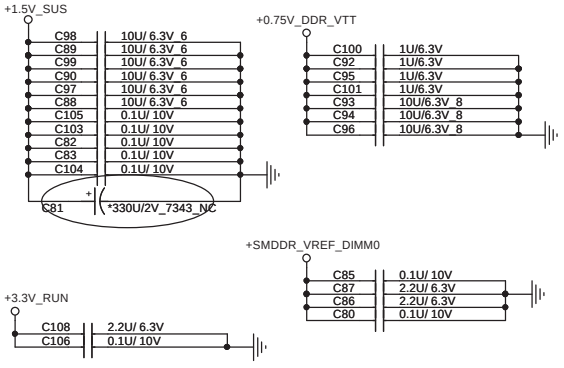
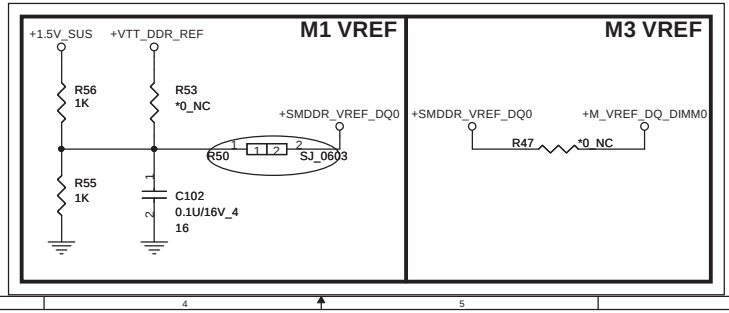


Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%





Quantities and M1/M3 follow UM3
Locations follow PDC

Quanta Computer Inc.
PROJECT : UM9 UMA

Size	Document Number	Rev
	DDR3 DIMM-0	1A
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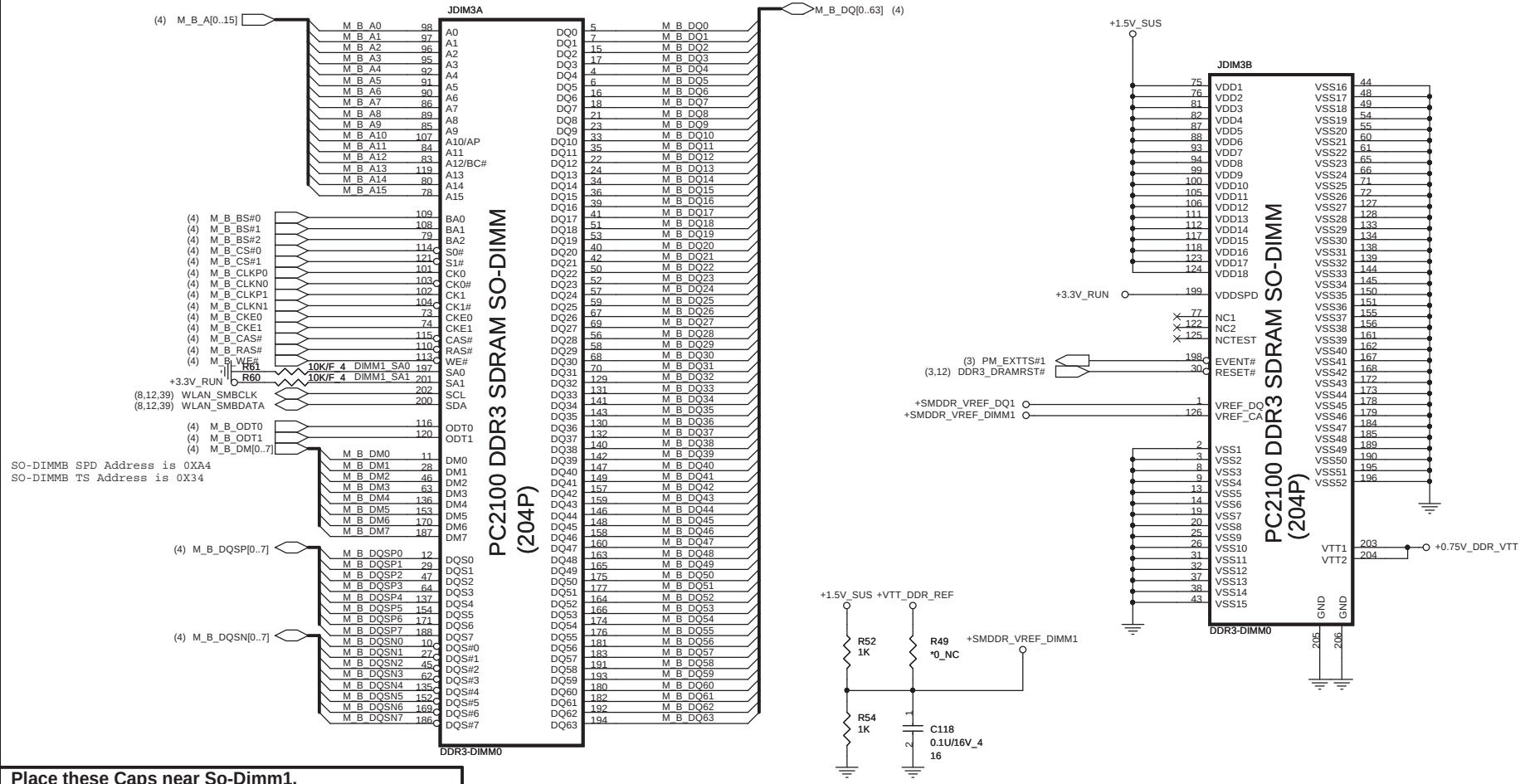
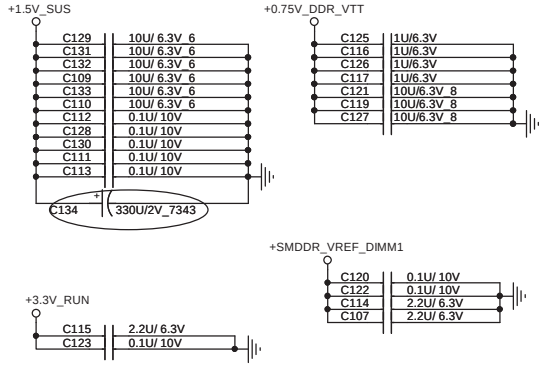
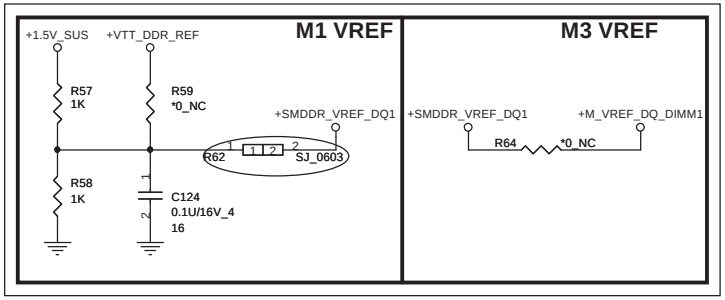


Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%





Quantities and M1/M3 follow UM3
Locations follow PDC

Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	DDR3 DIMM-1	1A

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	Blank	1A

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Quanta Computer Inc.

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	Blank	1A

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Quanta Computer Inc.

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	Blank	1A

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Quanta Computer Inc.

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	Blank	1A

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	Blank	1A

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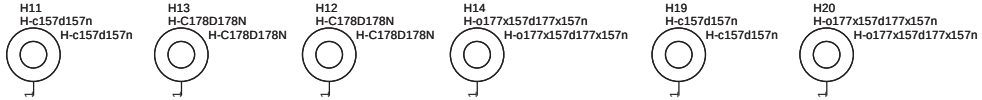
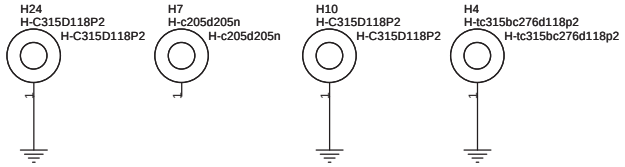
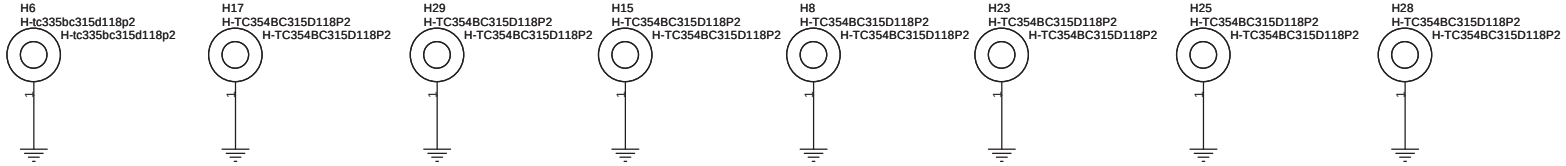
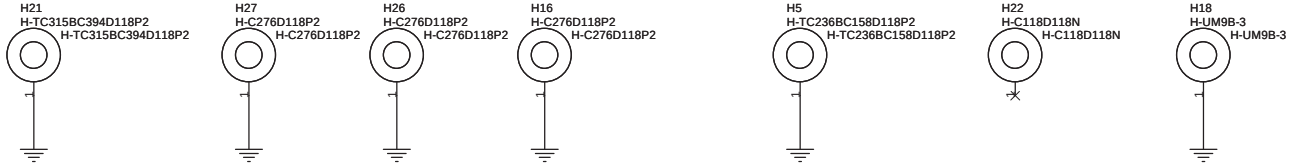
Del H1&H2



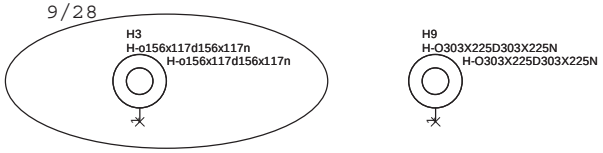




Nut



9/28



Quanta Computer Inc.
PROJECT : UM9 UMA

Size	Document Number	Rev
	SCREW PAD	1A
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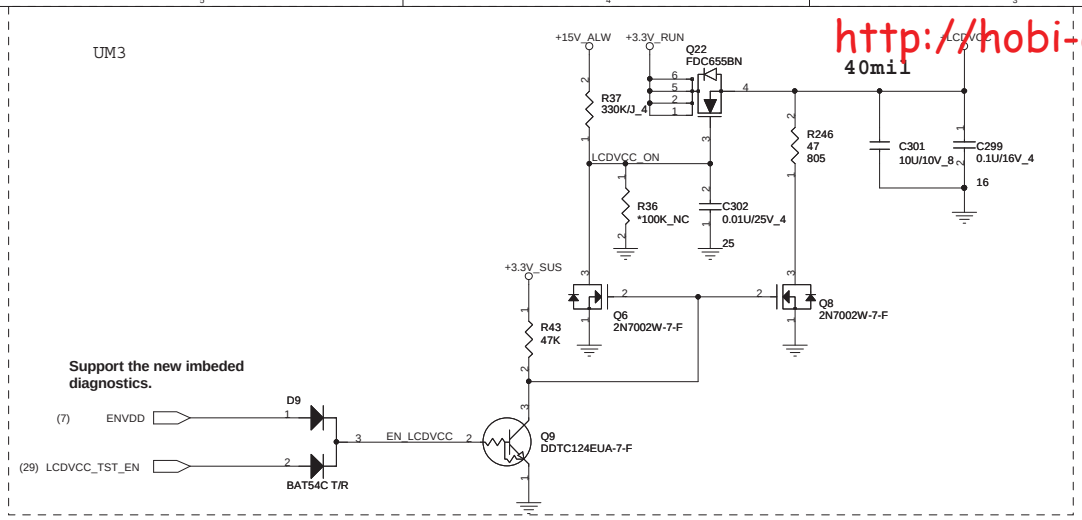

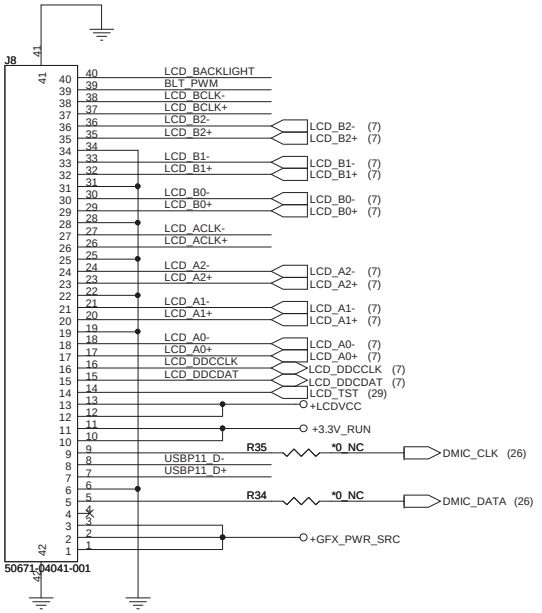

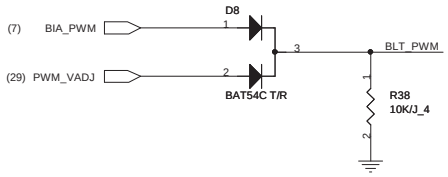

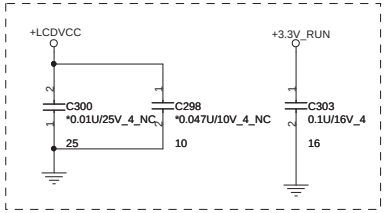

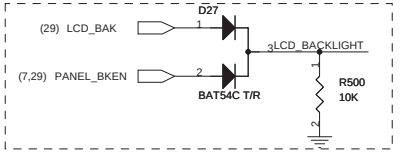

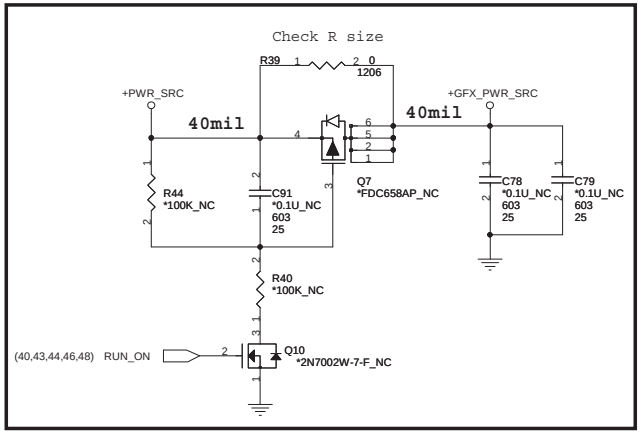

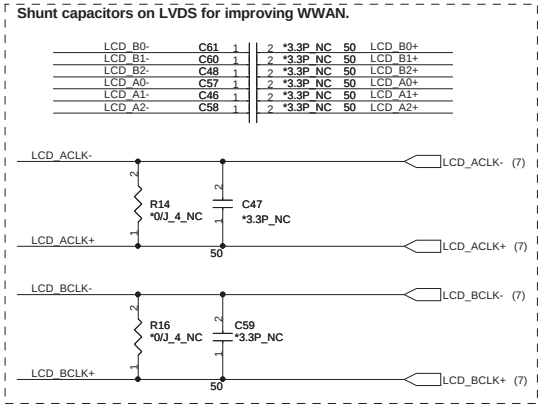

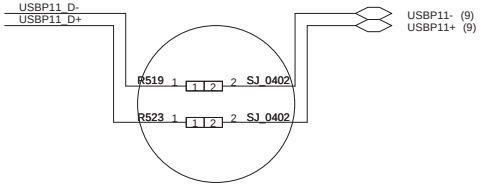

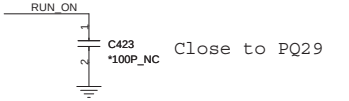

Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	LCD CONN / HDMI CONN	1A

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UM3

This page to CRT board

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	CRT CONN	1A

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To CRT BOARD

Quanta Computer Inc.

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Size	Document Number	Rev
	DB CONN/Left USB	1A

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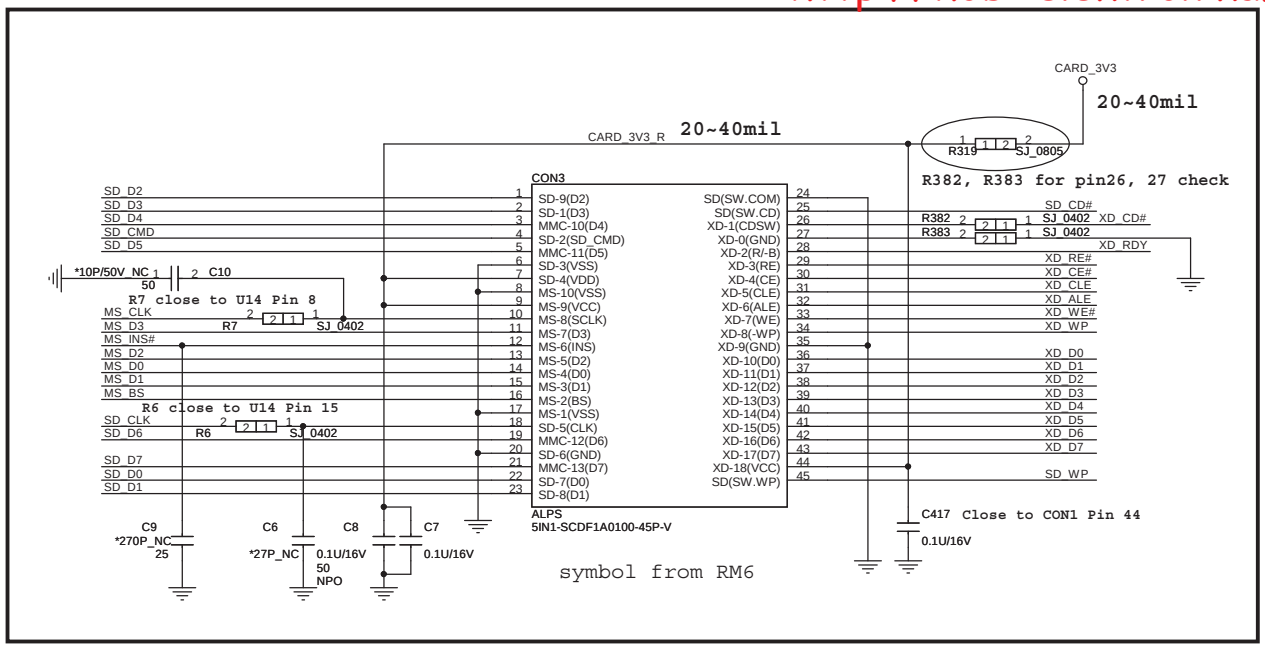
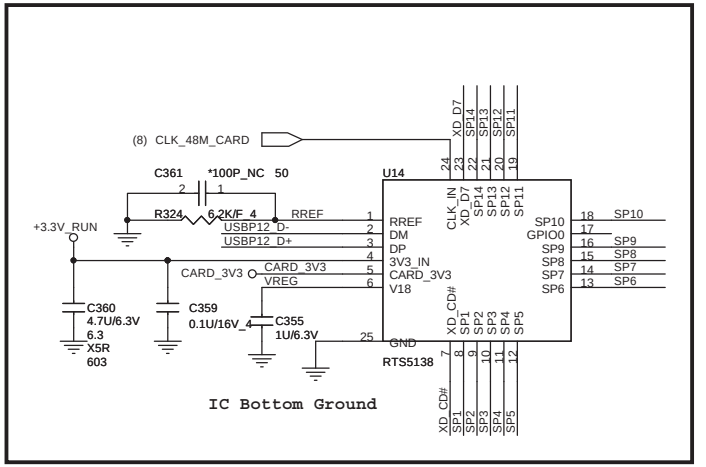
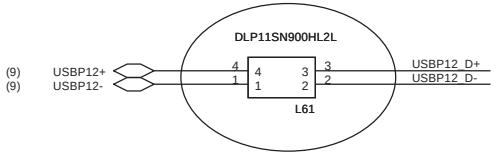




RTS5138-QFN24

SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

Share Pin



Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	Card Reader(RST5138)	1A
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UM3, symbol from PDC

***NOTE: ALC269_VB type add the LDO circuit in IC**

PIN NAME	R350	R344	R349	C398	CODEC IC
28 MIC1_VREF0-L			POP	NC	ALC269
31 CPVREF	POP	NC			VA

VA type: PIN28 作爲MIC之偏壓
PIN31接A-GND

PIN NAME	R350	R344	R349	C398	CODEC IC
28 MIC1_VREF0-L			NC	POP	ALC269
31 CPVREF	NC	POP			VB

VB type: PIN31 作爲MIC之偏壓
PIN28接CAP作爲內部LDO output 輸出濾波用

ZM1_MB_FOR_8BIT_0212-3.DSN

AVDD1, AVDD2 TYP=48mA

DVDD & DVDD-IO TYP=50mA

ALC269

Analog Plane

Digital Plane

Int. Stereo Speakers
5V / 4 Ohm / 2W

PD#=0V : Power down Class D SPK amplifer
PD#=3.3V : Power up Class D SPK amplifer
Internal pulled high.

Reserve RC for EMI

Digital GND Analog GND
Tied at one point only under the ALC269 or near the ALC269

UM3_DIS_20090824_1000_SSI_STEPHEN.DSN

Check the GND of MIC Conn. in the DB need add 0 ohm PD to A-GND

Quanta Computer Inc.
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	Azelia CODEC(ALC269)	1A
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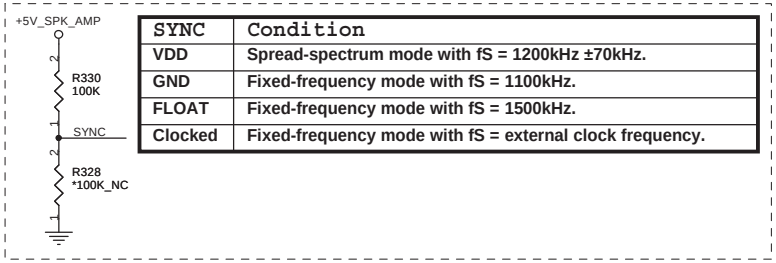
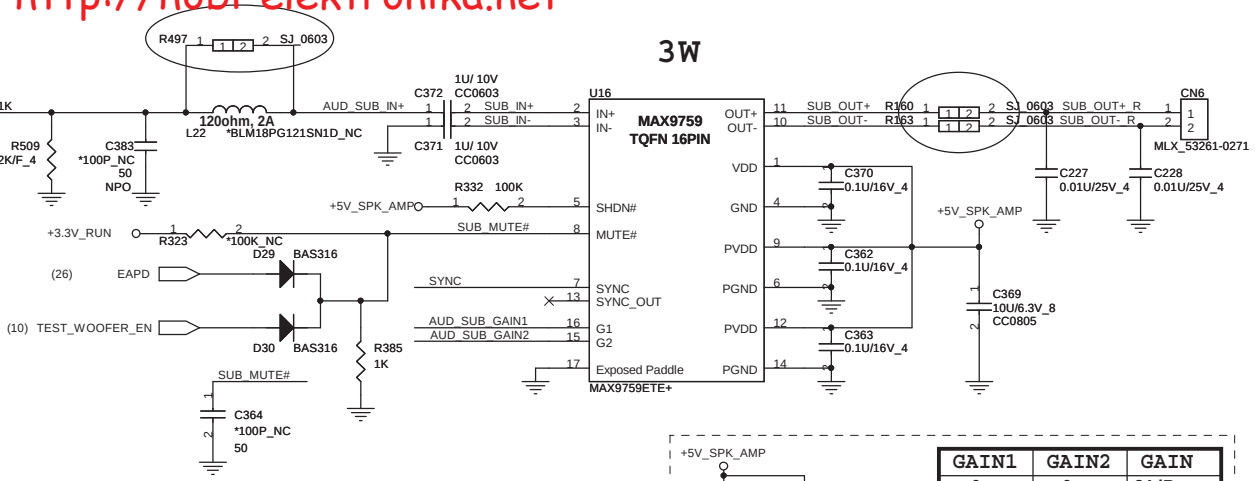
FM9

INTERNAL SUBWOOFER AMP Only for 17''

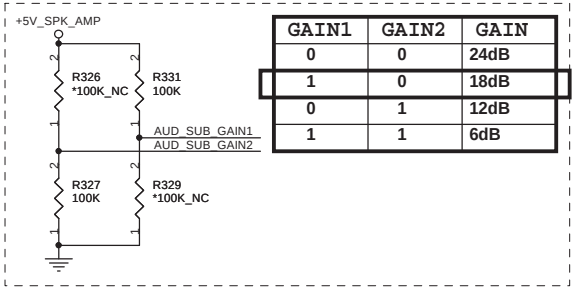
3W

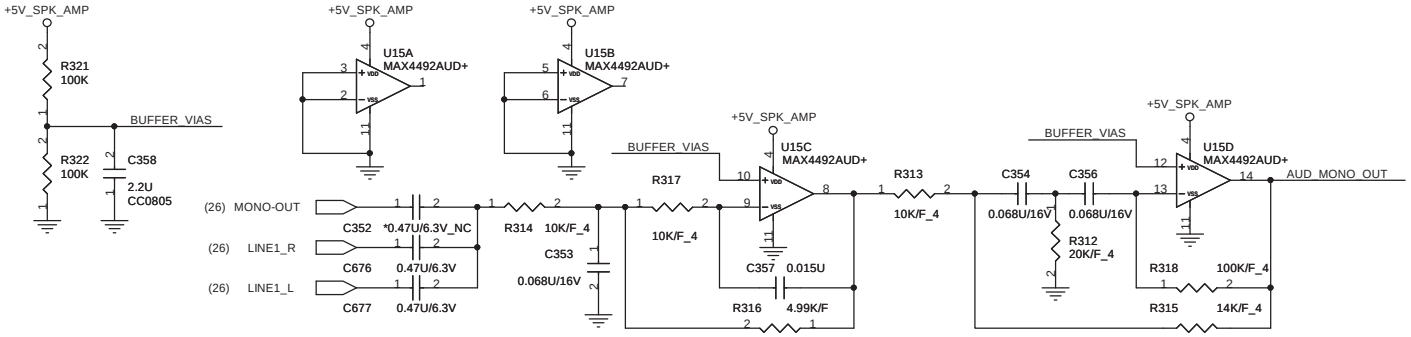
SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.

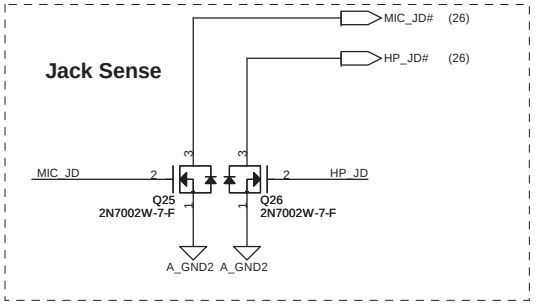


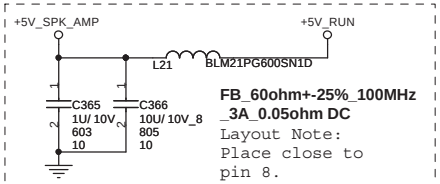


GAIN1	GAIN2	GAIN
0	0	24dB
1	0	18dB
0	1	12dB
1	1	6dB





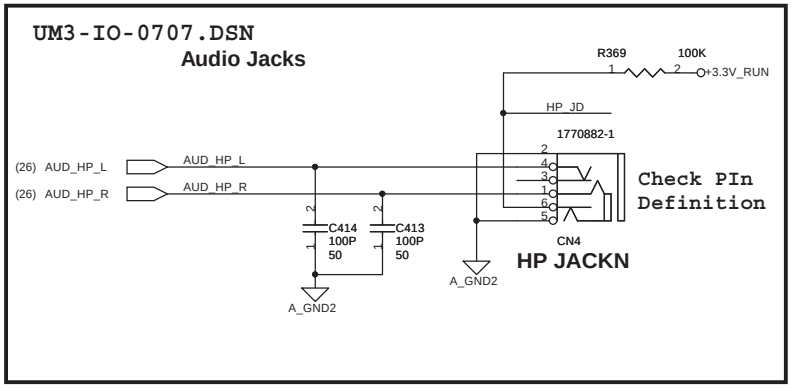


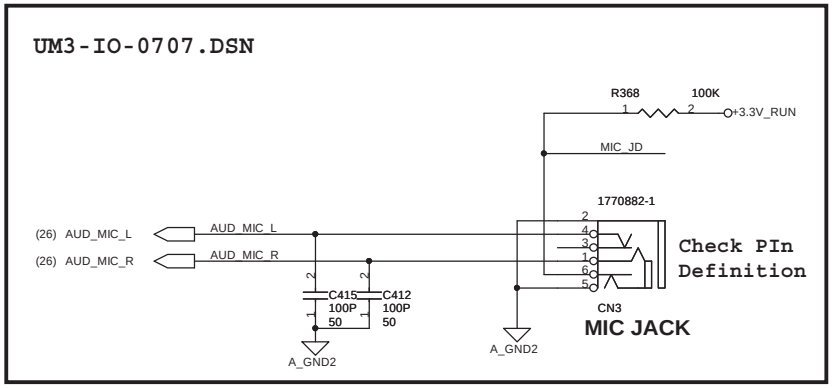


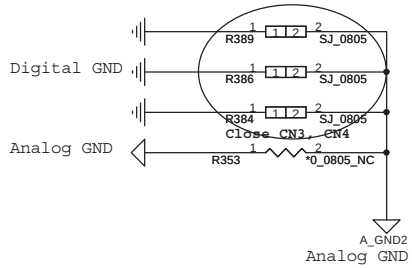
FB_60ohm+-25%_100MHz _3A_0.05ohm DC

Layout Note: Place close to pin 8.

NB_MUTE#	TEST_WOOFER_EN	AUD_SPK PD#	SUB_MUTE#
0	0	L (Disable SPK)	L (Disable Woofer)
0	1	L (Disable SPK)	H (Test Woofer)
1	0	H (Test SPK)	L (Disable Woofer)
1	1	H (Test SPK)	H (Test Woofer)







Quanta Computer Inc.

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	AUDIO CONN	1A

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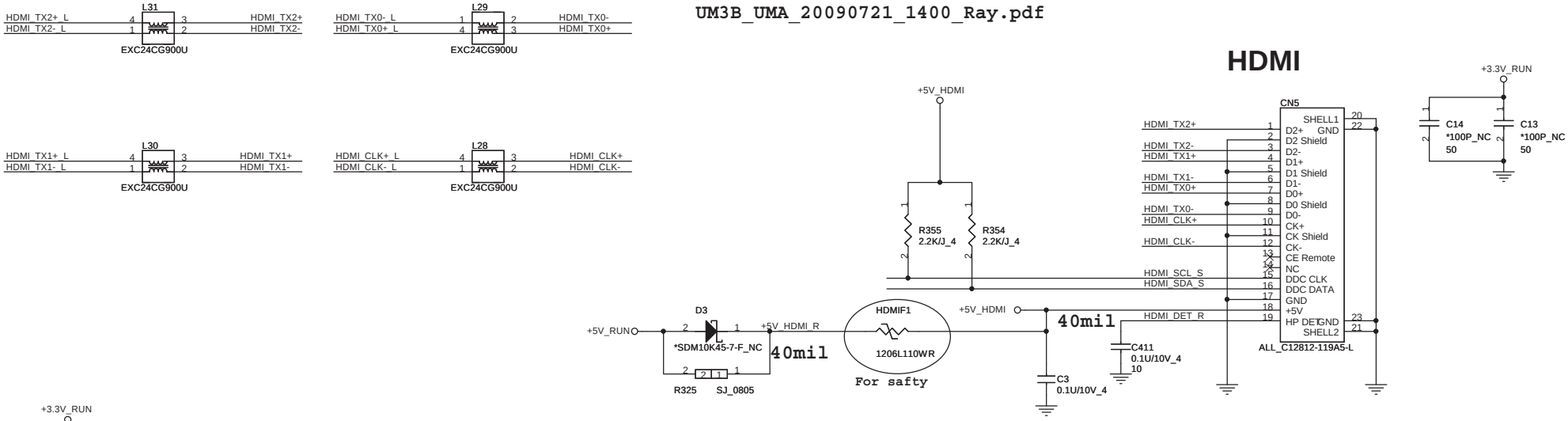
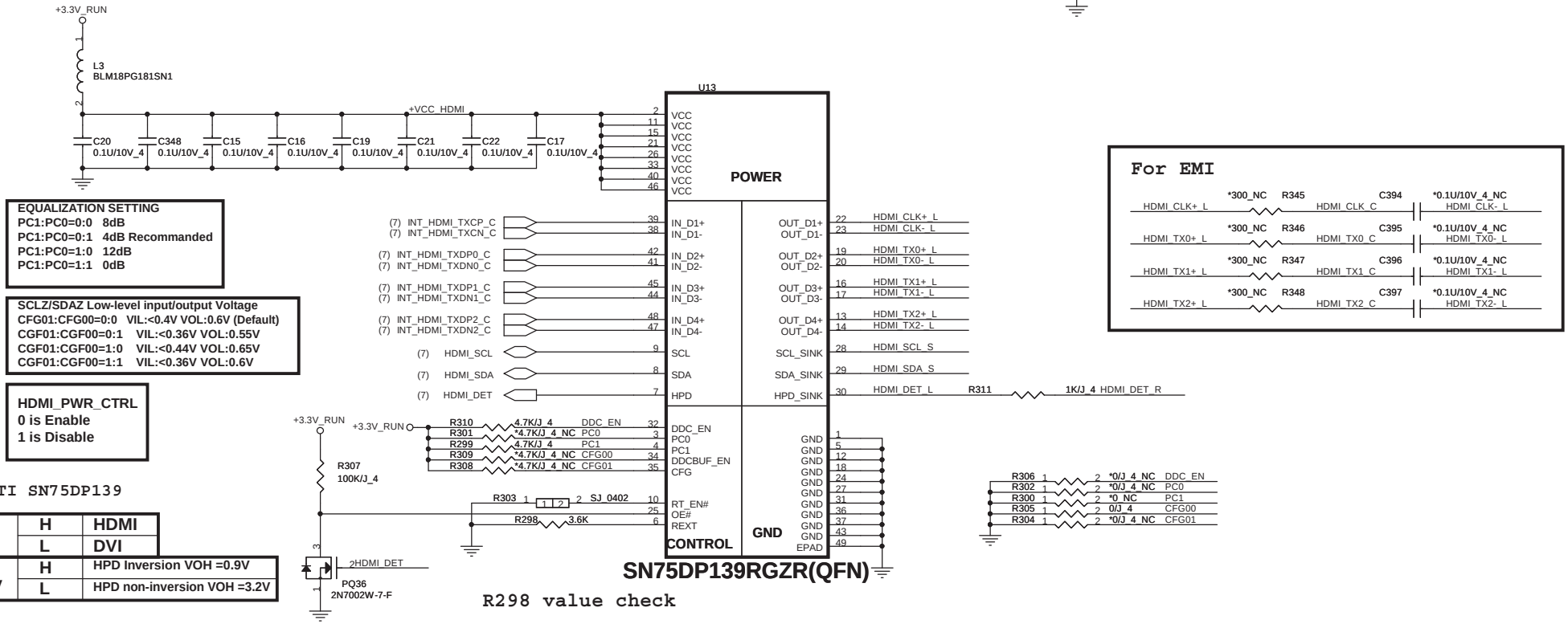
UM3B_UMA_20090721_1400_Ray.pdf

HDMI





EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)
CFG01:CGF00=0:1 VIL:<0.36V VOL:0.55V
CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V
CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V

HDMI_PWR_CTRL
0 is Enable
1 is Disable

TI SN75DP139

PIN 4 I2C_EN	H	HDMI
	L	DVI
PIN 34 HPDINV	H	HPD Inversion VOH =0.9V
	L	HPD non-inversion VOH =3.2V

R298 value check

For EMI

Quanta Computer Inc.		
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UM3

U6

ITE8502E
LQFP-128L

(34) KSO[0..17]
(34) KSI[0..7]

KSO17 57
KSO16 56
KSO15 55
KSO14 54
KSO13 53
KSO12 52
KSO11 51
KSO10 46
KSO9 45
KSO8 44
KSO7 43
KSO6 42
KSO5 41
KSO4 40
KSO3 39
KSO2 38
KSO1 37
KSO0 36

KSO17/GPC5
KSO16/GPC3
KSO15
KSO14
KSO13
KSO12/SLCT
KSO11/ERR
KSO10/PE
KSO9/BUSY
KSO8/ACK
KSO7/PD7
KSO6/PD6
KSO5/PD5
KSO4/PD4
KSO3/PD3
KSO2/PD2
KSO1/PD1
KSO0/PD0

KEYBOARD

KSI7 65
KSI6 64
KSI5 63
KSI4 62
KSI3 61
KSI2 60
KSI1 59
KSI0 58

KSI7
KSI6
KSI5
KSI4
KSI3/SLIN
KSI2/INT
KSI1/AFD
KSI0/STB

+3.3V_ALW

C281 10U/ 6.3V_6 603 6.3
C144 1U/6.3V_4
C289 0.1U/16V_4 16
C285 0.1U/16V_4 16
C280 0.1U/16V_4 16

Place these caps close to ITE8502.

+RTC_CELL
R66 SJ_0402
+VBAT1_EC
VBAT1 3
VCC 11 +3.3V_RUN
VSTBY1 26
VSTBY2 50
VSTBY3 92
VSTBY4 114
VSTBY5 121
VSTBY6 127 +3.3V_ALW
C139 0.1U/16V_4 16

ADC/DAC

ADC0/GPI0 66 HWPG
ADC1/GPI1 67 PAD T28
ADC2/GPI2 68
ADC3/GPI3 69 PAD T29
ADC4/GPI4 70 V_ID1
ADC5/GPI5 71
ADC6/GPI6 72
ADC7/GPI7 73 SIO_SLP_S5#

HWPG (37,40,45)
SUS_PWR_ACK (9)
PBAT_PRES# (47)
IINP (41)
SIO_SLP_S5# (9)

DAC0/GPJ0 76
DAC1/GPJ1 77
DAC2/GPJ2 78 USB_LEFT_EN#
DAC3/GPJ3 79
DAC4/GPJ4 80
DAC5/GPJ5 81

CRIT_TEMP_REP# (10)
SIO_EXT_WAKE# (10)
USB_LEFT_EN# (39)
FAN1_DA (37)
RSMRST# (9)
PM_PWRBTN#_R (9)

D18 SDM10K45-7-F

SMBDAT0 SMBCLK0 RP5 2.2KX2
SMBDAT1 SMBCLK1 RP4 10KX2
USB_LEFT_EN# R235 10K
SUS_ON R83 100K
IMVP_VR_ON R232 *100K_NC
SERIRQ LCD_BAK R243 R244 10K *10K_NC
SMBDAT2 SMBCLK2 RP3 10KX2

+3.3V_ALW
+3.3V_RUN

PWM

PWM0/GPA0 24
PWM1/GPA1 25 PAD T30
PWM2/GPA2 28
PWM3/GPA3 29
PWM4/GPA4 30 PAD T31
PWM5/GPA5 31 PAD T32
PWM6/GPA6 32 PAD T4
PWM7/GPA7 34 EC_BEEP (26)

BREATH_LED# (36)
FAN1_PWM (37)
PWM_VADJ (22)

TACH0/GPD6 47 FAN1_TACH (37)
TACH1/GPD7 48 PANEL_BKEN (7,22)

TMRI0/WUI2/GPC4 120 LID_SW# (34)
TMRI1/WUI3/GPC6 124 SIO_SLP_S3# (9)

R240 0
+3.3V_RUN
R239 *100K_NC
ICH_AZ_CODEC_RST0#
Q21 *2N7002W-7-F_NC
R238 *390K_NC
C288 *0.1U/10V_NC 10
Q20 *MMST3904-7-F_NC
(7,26) ACZ_RST#_AUDIO

IR/UART

PAD T33
PAD T27

RXD/GPB0 108
TXD/GPB1 109
GPC0 119
CTX0/GPB2 123
CRX1/GPH1/ID1 94
CTX1/GPH2/ID2 95 IMVP_VR_ON

H_CPUDET# (3)
IMVP_PWRGD (3,45)
RUN_ON_1 (40)
BAT1_LED (36)
IMVP_VR_ON (45)

PAD T25

LPC/FWH FLASH

PAD T21

FLFRAME/GPG2/LF 100 SUS_ON
FLRST/GPG0/TM 106
FLAD3/GPG6 104 PAD T34
PAD T7

SUS_ON (42,46)
KB_DET# (34)

FLAD2/SO 103
FLAD1/SI 102
FLAD0/SCE 101
FLCLK 105

EC_FLASH_SPI_DO (30)
EC_FLASH_SPI_DIN (30)
EC_FLASH_SPI_CS# (30)
EC_FLASH_SPI_CLK (30)

PAD T6
PAD T9
PAD T8

EGPC

EGAD/GPE1 82 ECPWROK
EGCS/GPE2 83
EGCLK/GPE3 84 PAD T26
PAD T35

ECPWROK (9)
ALW_ON (36)

GPIO

GPH3/ID3 96 BID2
GPH4/ID4 97 USB_RIGHT_EN#
GPH5/ID5 98 BID1
GPH6/ID6 99 LCD_SIZE_ID
GPG1/ID7 107 LCD_SIZE_ID2

BID2 (30)
USB_RIGHT_EN# (30,39)
BID1 (30)
LCD_SIZE_ID (30)

R65 *100K_NC +3.3V_ALW
RI1/WUI0/GPD0 18
RI2/WUI1/GPD1 21 PAD T36
WUI5/GPE5 35 SDM10K45-7-F D12
ACAV_IN (36,41)
BAT2_LED (36)

RING/PWRFAIL/LPCRST/GPB7 112 AC_PRESENT (9)
PWRSW/GPE4 125 SYS_PWR_SW# (36)
GINT/GPD5 33 LCDVCC_TST_EN (22)
PAD T5

LPC

LPCRST/WUI4/GPD2 22
LPCCLK 13
LFRAME 6
LAD0 10
LAD1 9
LAD2 8
LAD3 7

(3,9,39) PLTRST# R67 SJ_0402
(9) CLK_33M_KBC
(7,39) LFRAME#
(7,39) LAD0
(7,39) LAD1
(7,39) LAD2
(7,39) LAD3

CLKRUN/GPH0/ID0 93
SERIRQ 5
ECSMI/GPD4 15
ECSCI/GPD3 23
GA20/GPB5 126
LPCPD/WUI6/GPE6 17

(9) CLKRUN#
(7) SERIRQ
(10) SIO_EXT_SMI#
(10) SIO_EXT_SCI#
(10) GATEA20
(22) LCD_TST

SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

D11 D13 D17 SDM10K45-7-F

KBRST/GPB6 4
WRST 14
PWUREQ/GPC7 16

(10) RCIN#
T12 PAD
(22) LCD_BAK
D10 SDM10K45-7-F
WRST#
LCD_BAK

L80HLAT/GPE0 19
L80LLAT/WUI7/GPE7 20

(26) NB_MUTE#
ICH_AZ_CODEC_RST0#

SMBUS

SMCLK0/GPB3 110
SMDAT0/GPB4 111
SMCLK1/GPC1 115
SMDAT1/GPC2 116
SMCLK2/GPF6 117
SMDAT2/GPF7 118

(41,47) SMBCLK0
(41,47) SMBDAT0
(8) SMBCLK1
(8) SMBDAT1
(2,37) SMBCLK2
(2,37) SMBDAT2

PS/2

PS2CLK0/GPF0 85
PS2DAT0/GPF1 86
PS2CLK1/GPF2 87
PS2DAT1/GPF3 88
PS2CLK2/GPF4 89
PS2DAT2/GPF5 90

R507 SJ_0402
(7,10) PCH_MELOCK T11 PAD
(47) PS_ID T10 PAD
(34) CLK_TP_SIO
(34) DAT_TP_SIO

Charge and BAT
PCH
VGA, LAN, Clock Thermal IC

+3.3V_ALW
R63 100K WRST#
C137 1U/ 10V 603 10

CK32K 128
CK32KE 2
VCORE 12
VSS1 1
VSS3 27
VSS4 49
VSS5 91
VSS6 113
VSS7 122
AVCC 74
AVSS 75

ITE8502_XTAL1
ITE8502_XTAL2
ITE8502IX_JX

+3.3V_ALW
L6 BLM11A05S 603
+AVCC_EC
C147 0.1U/16V_4 16
L5 BLM11A05S 603

ITE8502E
lqfp128-16x16-4

Board ID Straps

Madison
Discrete
+3.3V_ALW

R234 *10K_NC
R78 10K
R94 *10K_NC
R88 *10K_NC
R89 10K
R91 10K
R233 *10K_NC
R79 *10K_NC
R95 10K
R86 10K
R90 *10K_NC
R92 *10K_NC

USB_RIGHT_EN#
BID1
LCD_SIZE_ID
BID2
LCD_SIZE_ID2
V_ID1

Park
UMA

VGA_TYPE
VGA_IDENTIFY

	LCD_SIZE_ID (99)	LCD_SIZE_ID2 (107)
13.3"	0	0
14"	1	0
17"	0	1

BID1	BID0 USB_RIGHT_EN#	UM9(UMA)	UM9C (Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	OT (A00)	OT (A00)
0	0	(A01)	(A01)

32KHz Clock.(Layout close to EC)

C141 18P/50V_4
W3 32.768KHZ
R496 10M/J_4
C140 18P/50V_4
ITE8502_XTAL1
ITE8502_XTAL2

CLK_33M_KBC
R241 10
C284 2.2P 50

ITE8502IX_JX
C287 0.1U/16V_4 16

Close to PU9
IMVP_VR_ON
C424 *100P_NC 50
IMVP_PWRGD
C283 *100P_NC 50

Quanta Computer Inc.
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Size	Document Number	Rev
	SIO ITE8502	1A
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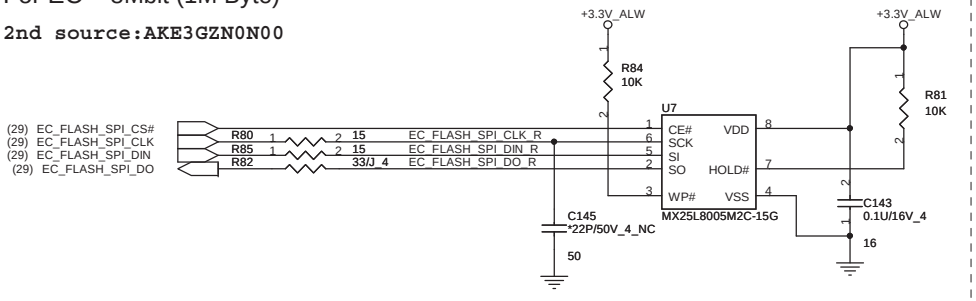
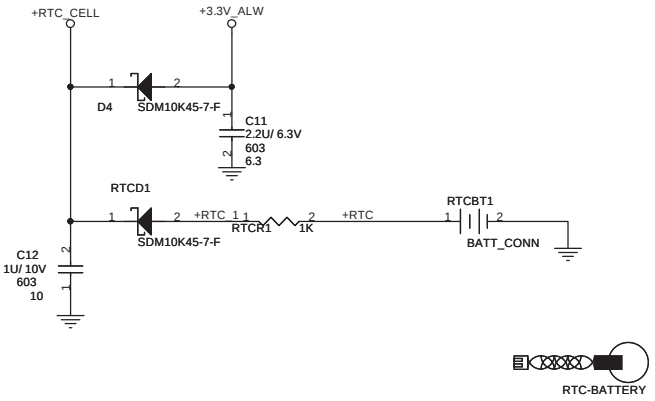
For EC 8Mbit (1M Byte)

2nd source:AKE3GZN0N00



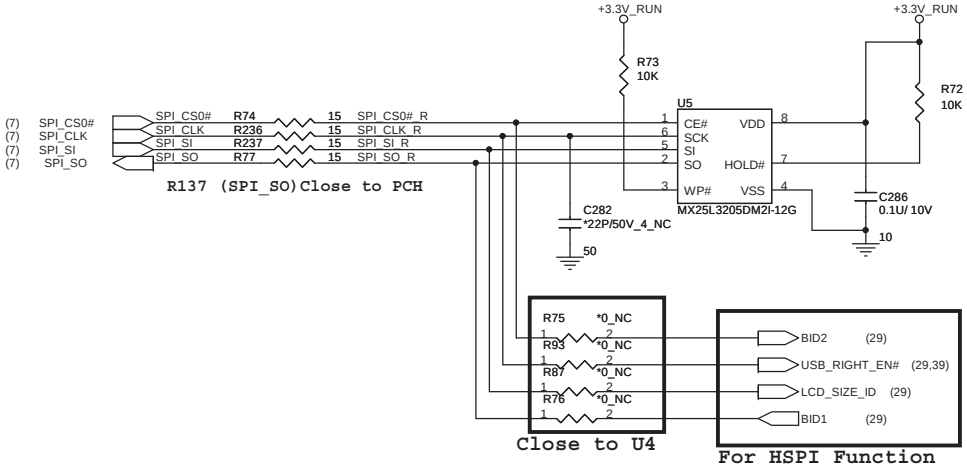
RTC BATTERY



For PCH

32Mbit (4M Byte)

2nd source:AKE39ZP0N00



Quanta Computer Inc.		
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UM3

WWAN To DB

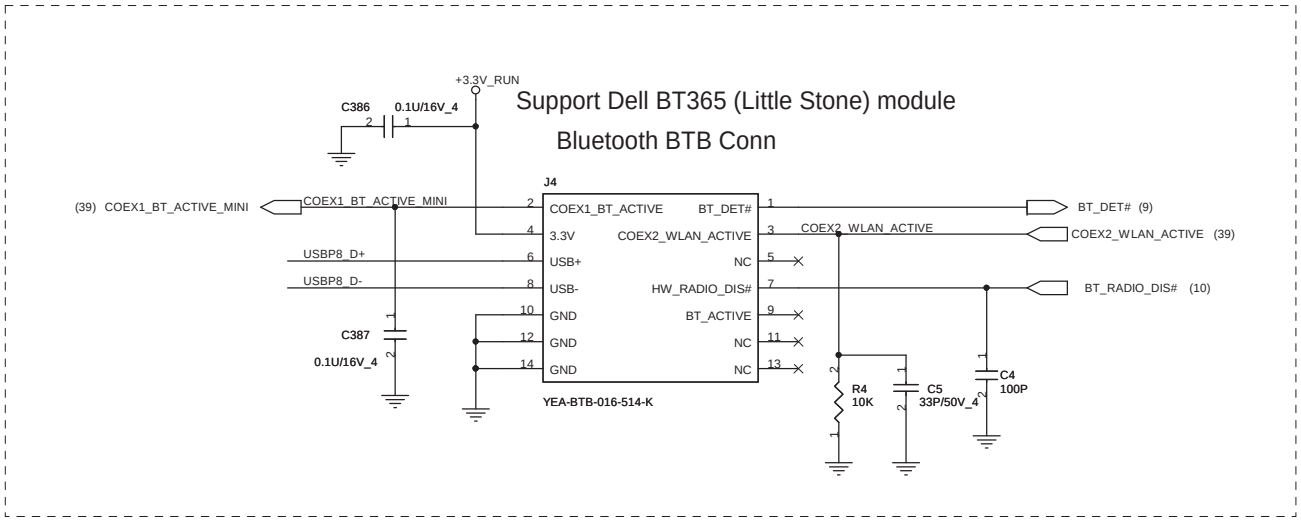
Quanta Computer Inc.

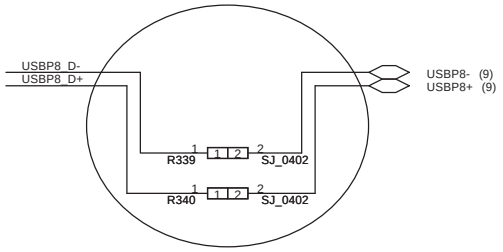
PROJECT : UM9 UMA

Size	Document Number	Rev
	MINI-Card WWAN	1A

Date: Wednesday, January 27, 2010 Sheet 31 of 51

WLAN To DB





Quanta Computer Inc.		
PROJECT : UM9 UMA		
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eSATA and USB To DB

Quanta Computer Inc.

PROJECT : UM9 UMA

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	eSATA & Right USB	1A

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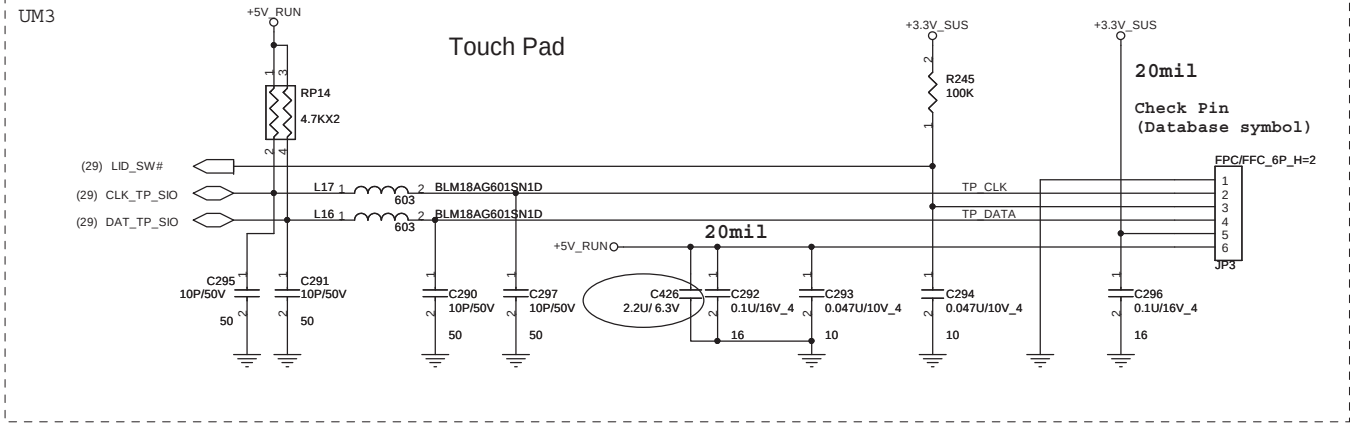
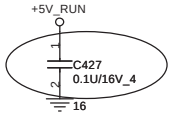
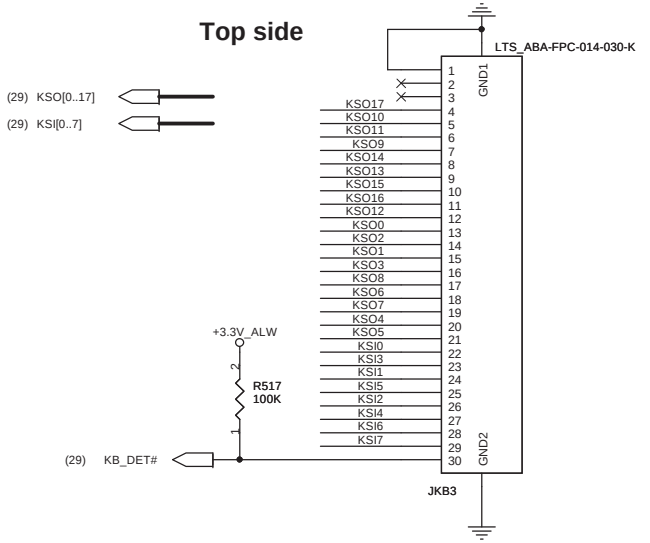
UM3 — Touch Pad

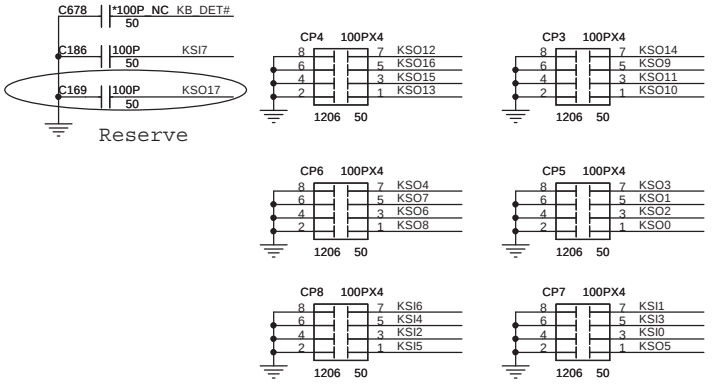




KEYBOARD CONNECTOR

Top side





100P CAPS CLOSE TO JKB3

Quanta Computer Inc.		
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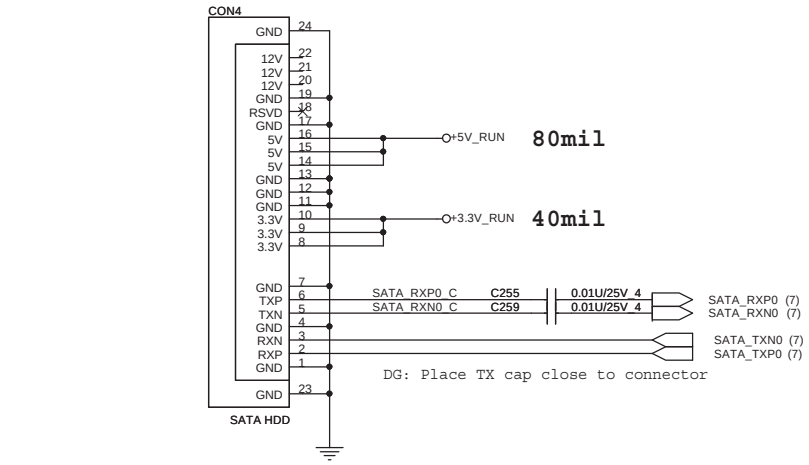
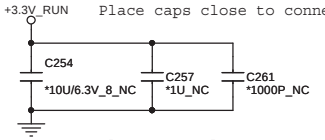
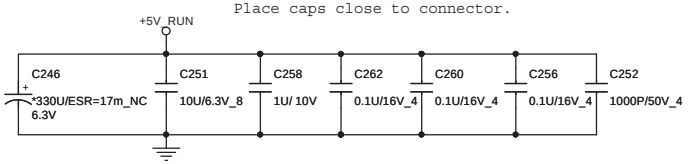
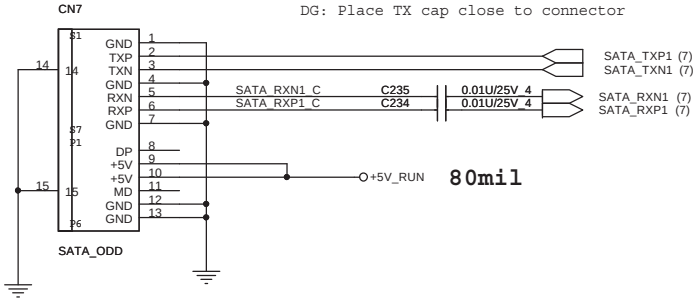
SATA Connector.

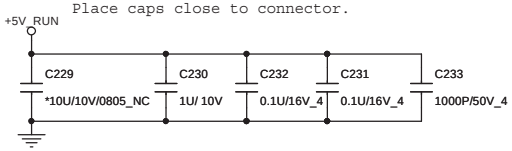






ODD Connector





Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	SATA (HDD&CD_ROM)	1A

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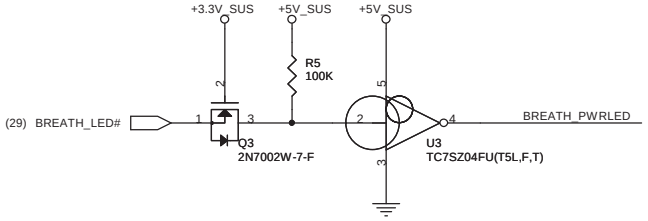
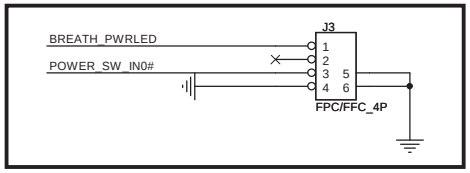
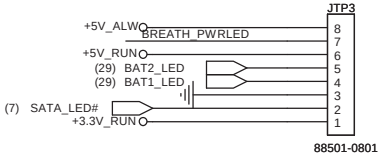
Power



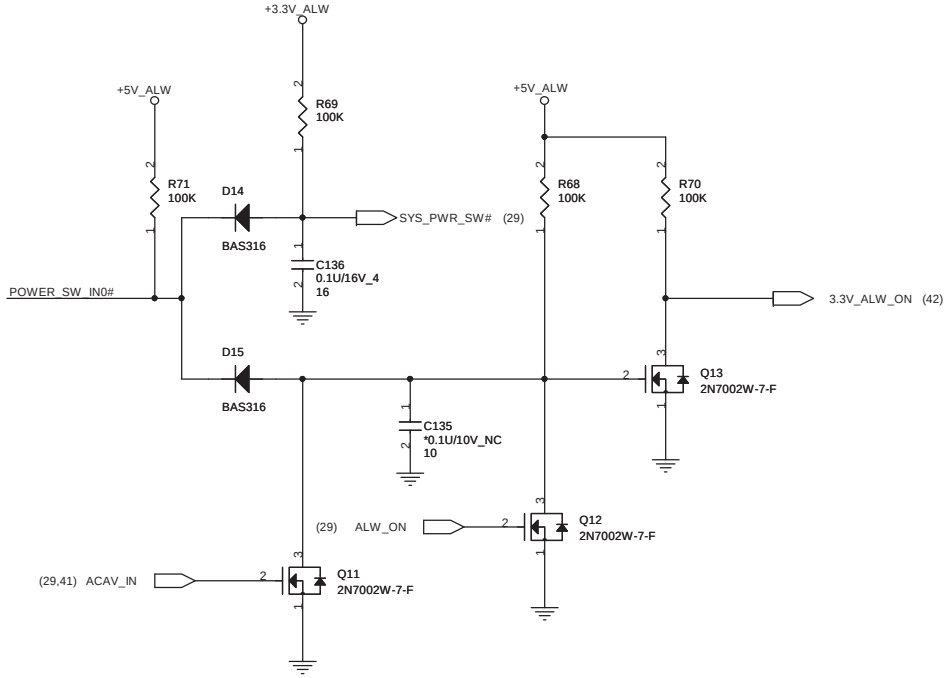
Power button Cable

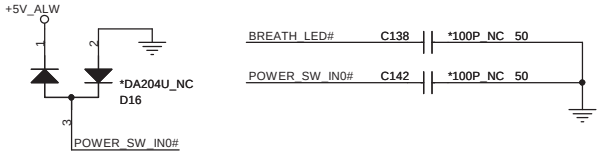


Check Connector P/N and footprint



3VALW ON POWER LOGIC





Quanta Computer Inc.		
PROJECT : UM9 UMA		
Size	Document Number: SWITCH, LED	Rev: 1A
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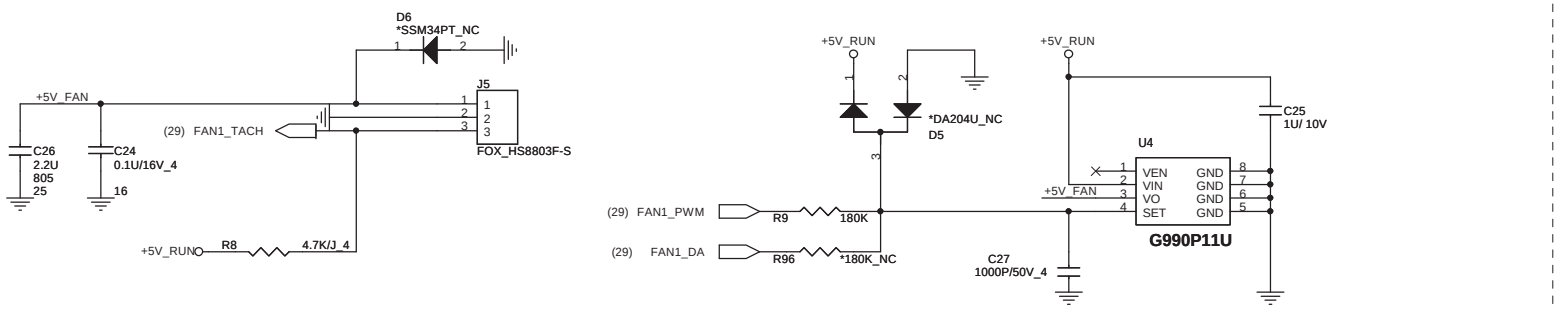
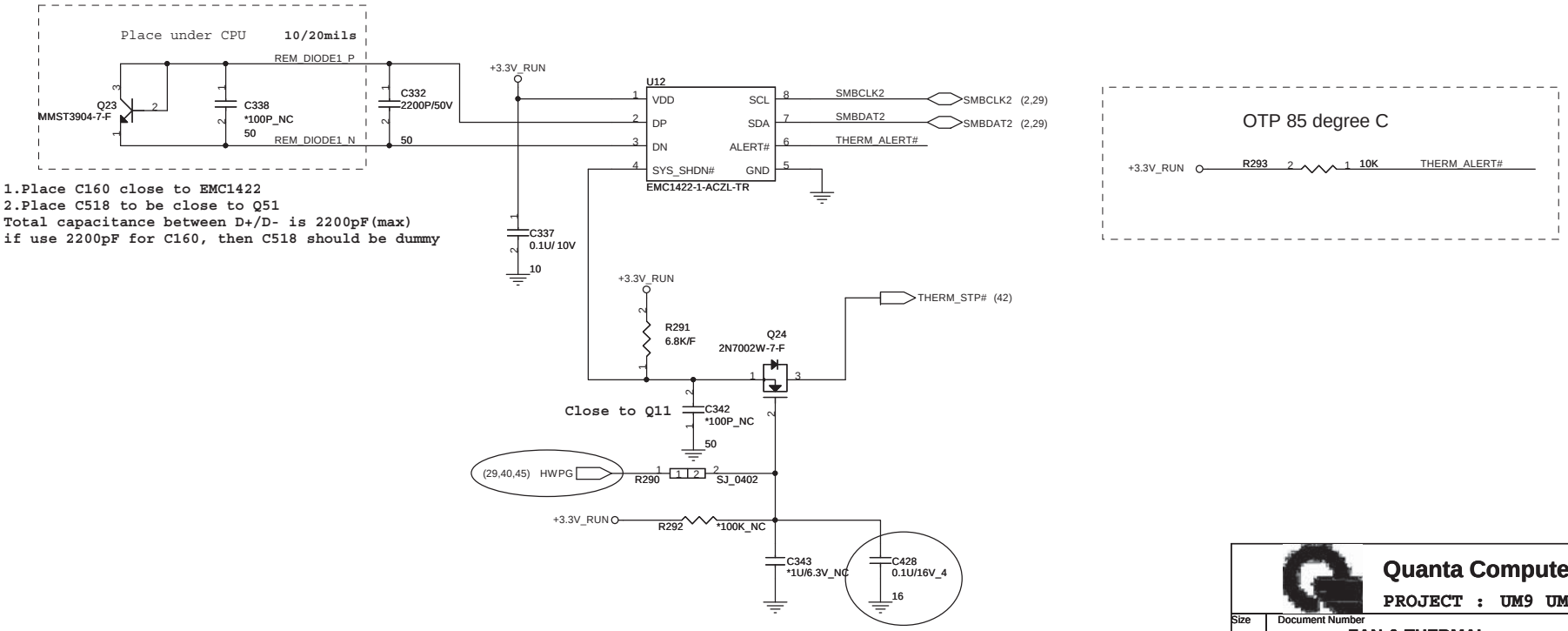
FAN CONTROL

6/23 COPY FROM RM6



UM3



Quanta Computer Inc.		
PROJECT : UM9 UMA		
Size	Document Number: FAN & THERMAL	Rev: 1A
Date: Monday, February 01, 2010	Sheet 37 of 51	

LAN To DB

Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	LAN(AR8152/RJ-45)	1A

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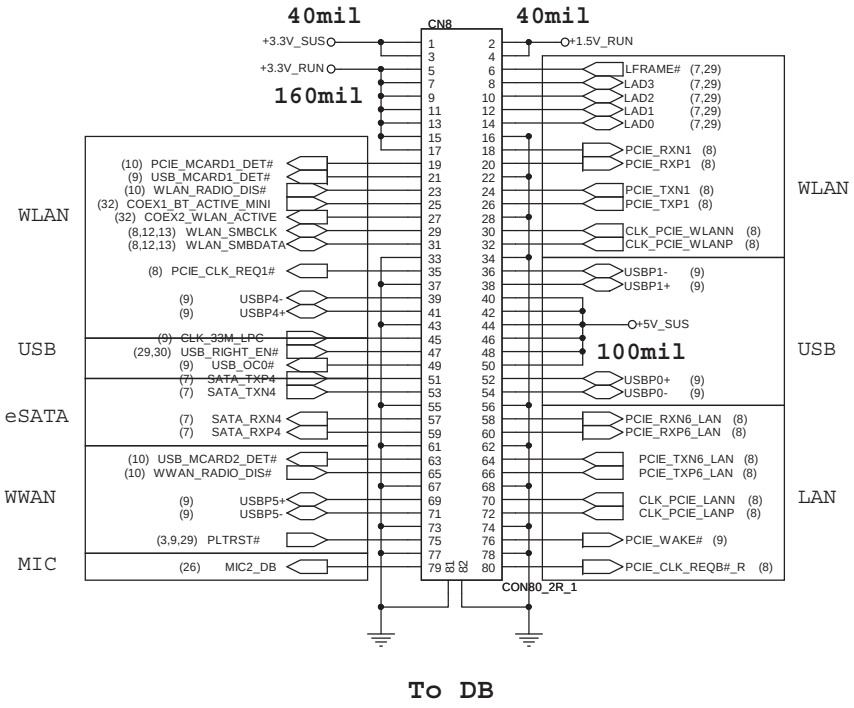
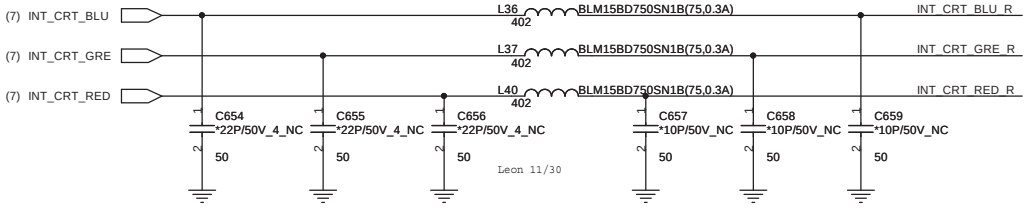
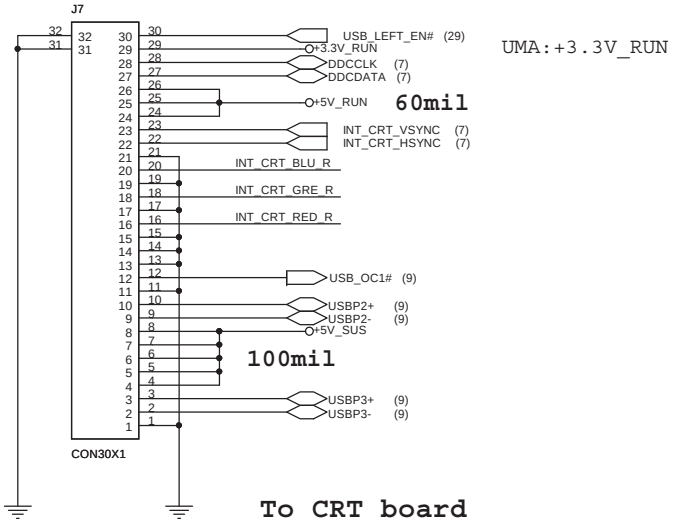


To DB

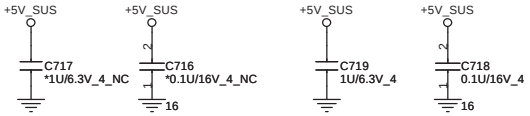


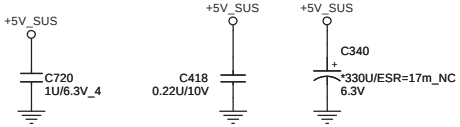
Close to PCH



UMA:+3.3V_RUN

To CRT board





Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	BTB CONN	1A
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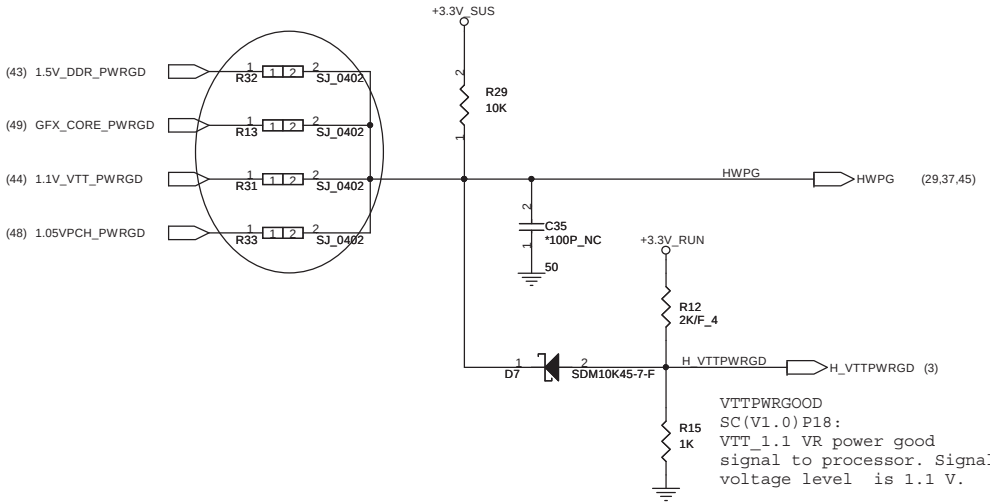
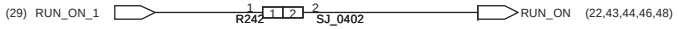
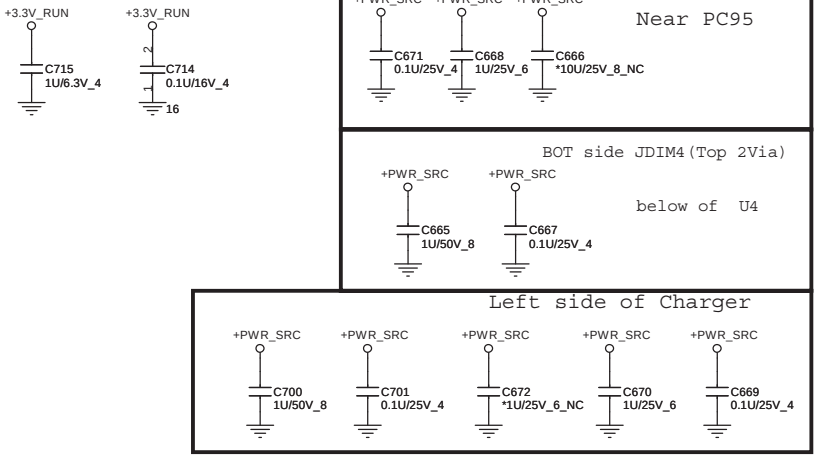
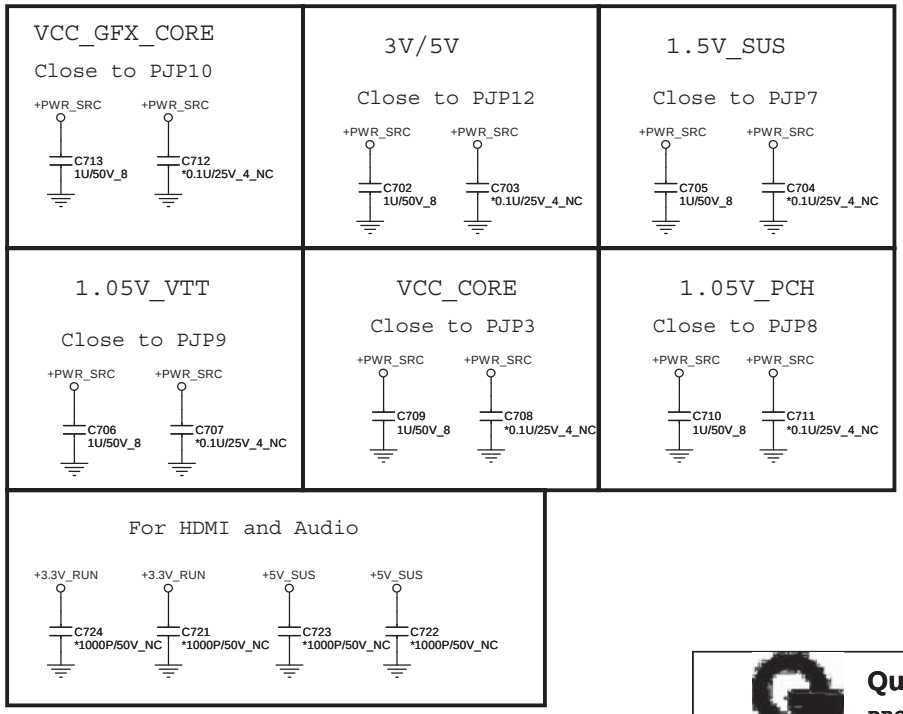
UM3





For FDI bus noise





Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	System Reset Circuit	1A
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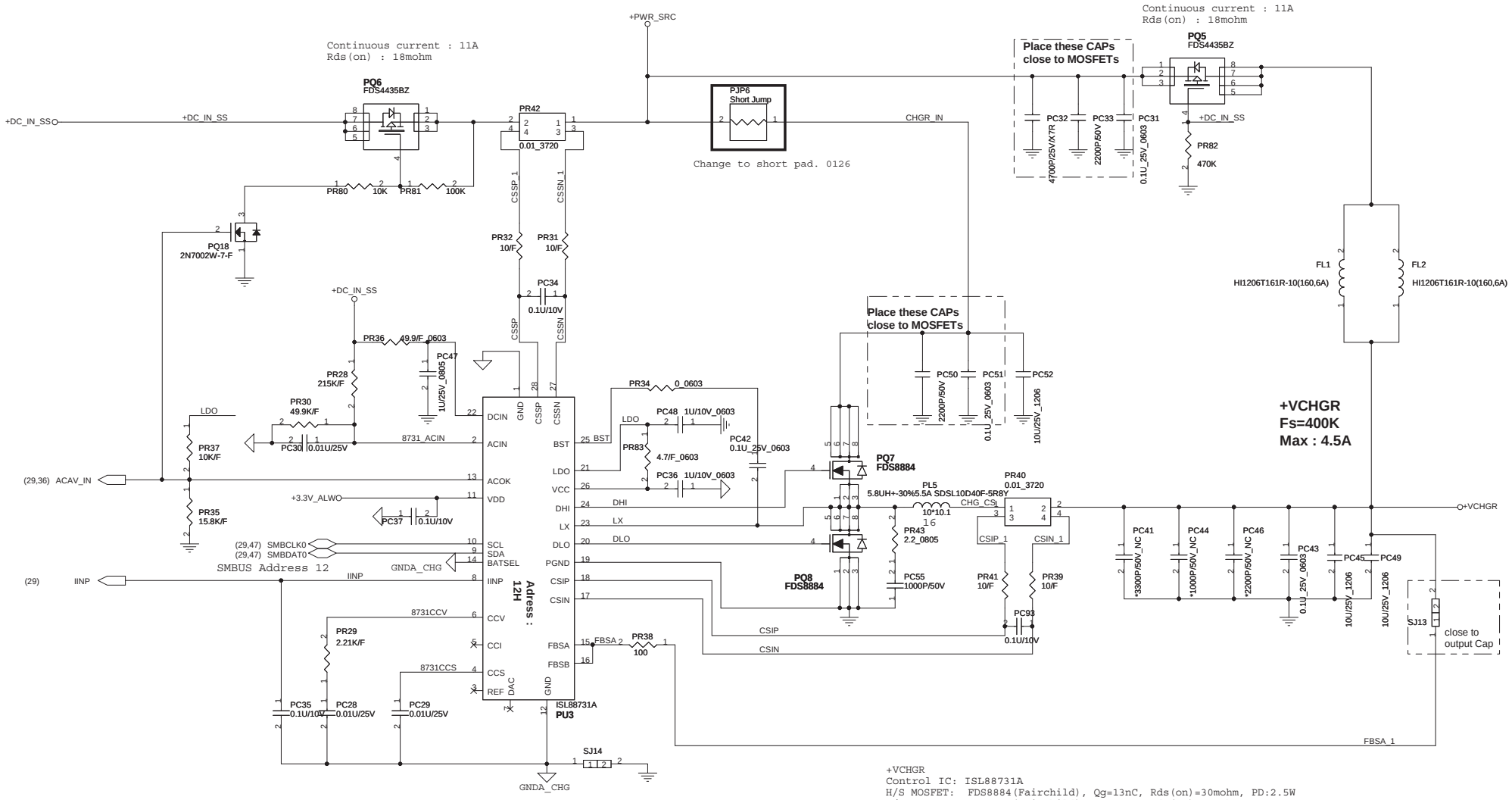
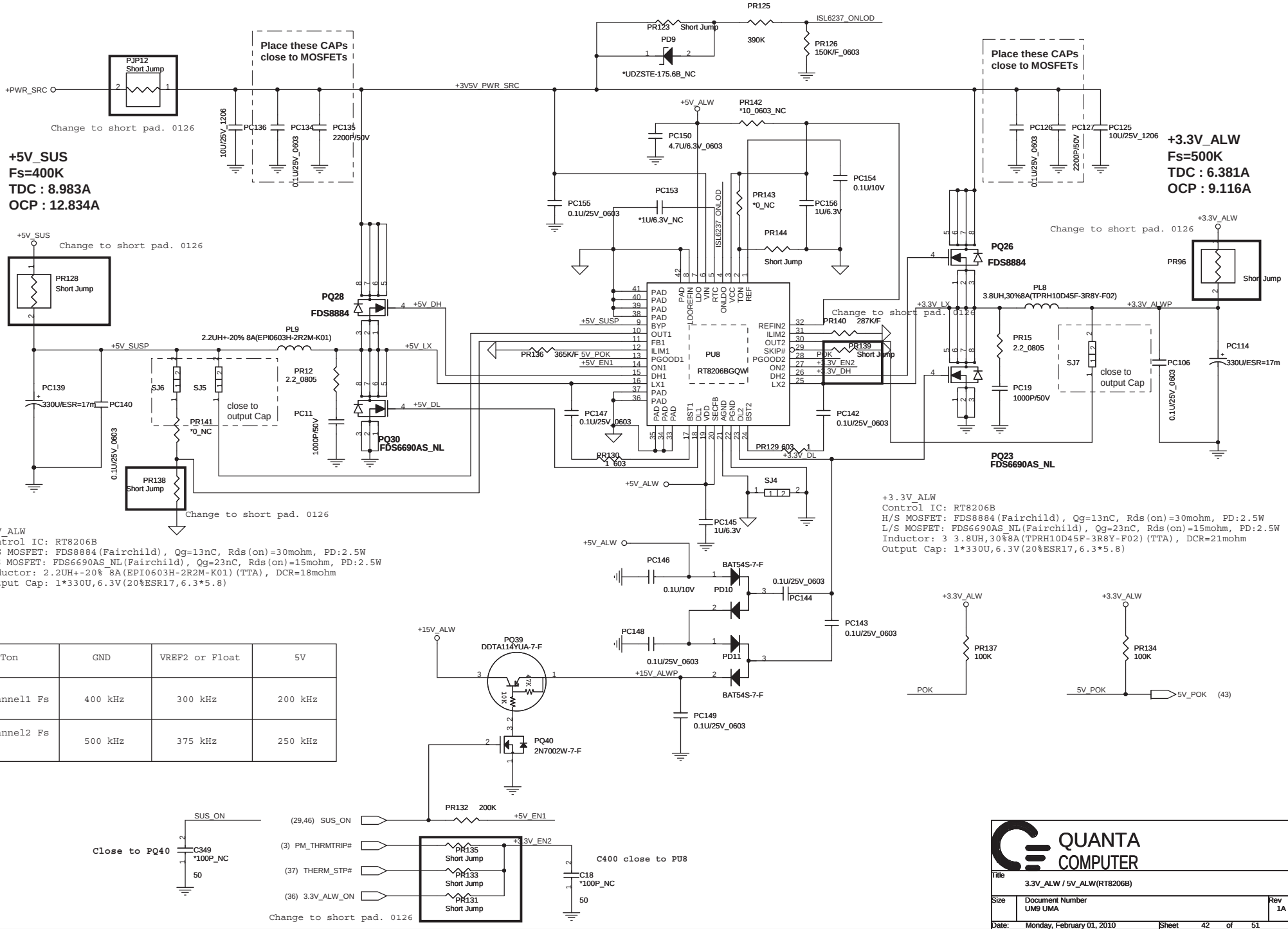
UM9-UMA-0910 OF POWER.DSN



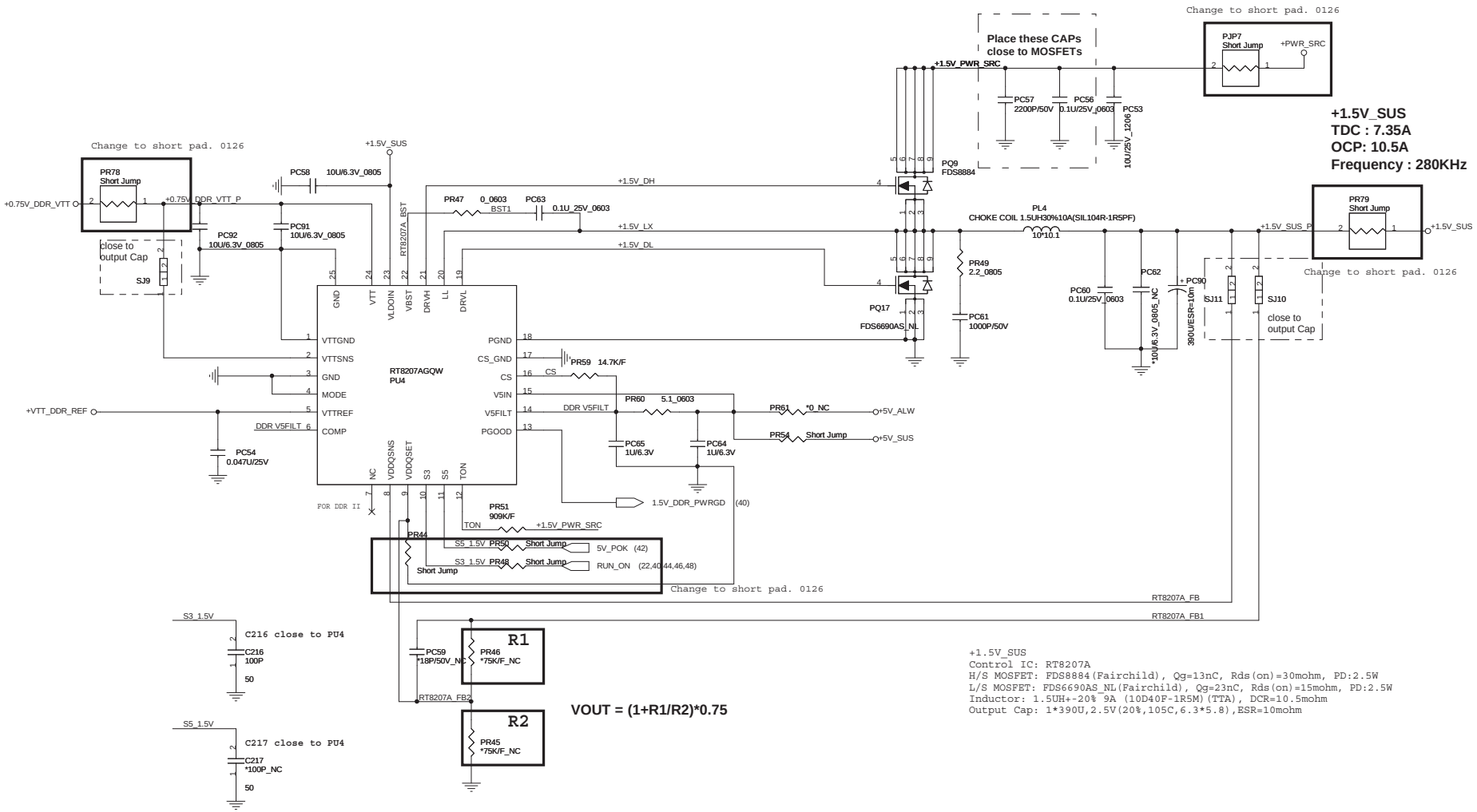
+VCHGR
Control IC: ISL88731A
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
Inductor: 5.8UH +-30% 5.5A SDSL10D40F-5R8Y(TTA), DCR=21mohm
Output Cap: 2*10U 25V(+-10%,X6S,1206)

QUANTA COMPUTER

Title	Charger (ISL88731)	
Size	Document Number UM9 UMA	Rev 2A
Date: Monday, February 01, 2010	Sheet 41 of 51	



Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz



+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
Inductor: 1.5UH+-20% 9A (10D40F-1R5M)(TTA), DCR=10.5mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

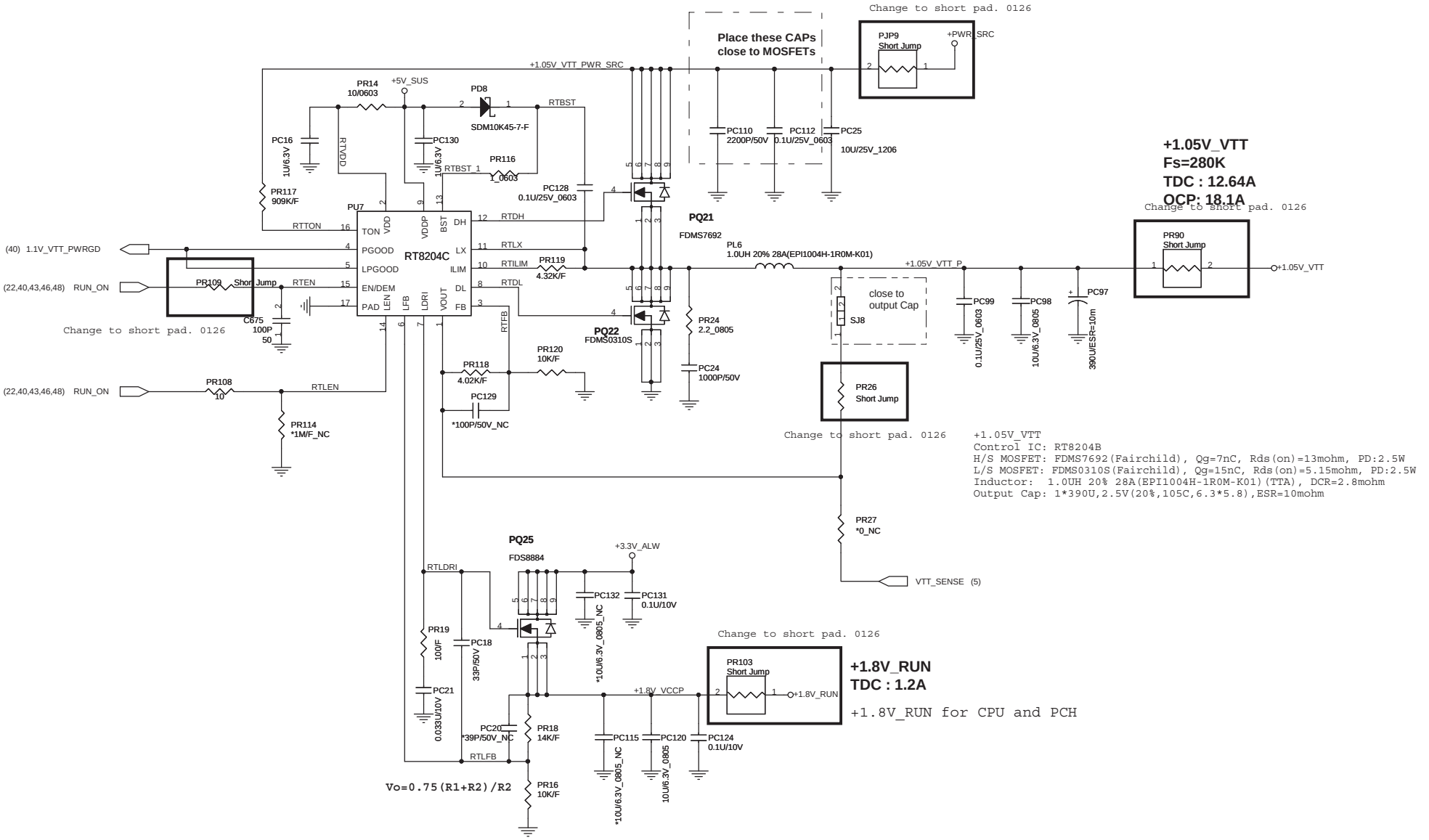
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Title	DDR3 +1.5V_SUS(RT8207AGQW)		
Size	Document Number UM9 UMA		Rev 1A
Date:	Monday, February 01, 2010	Sheet 43 of 51	



Title	+1.05V_VTT(RT8204C)	
Size	Document Number UM9 UMA	Rev 2A
Date: Monday, February 01, 2010	Sheet 44 of 51	

+VCC_CORE
Fs=300K
MAX : 48A
OCP : 64A

Change to short pad. 0126

PJP3 Short Jump

PU9 ADP3212MNR2G

PQ3 FDMS7692 · PQ4 FDMS7692 · PQ35 FDMS0310S · PQ37 FDMS0310S · PQ34 FDMS0310S · PQ38 FDMS0310S

PL11 0.36UH+-20%29.8A FDUE1040D-H-R36M=P3 · PL10 0.36UH+-20%29.8A FDUE1040D-H-R36M=P3

NOTE:
PR192 is reserved for loop gain measurement purpose.

Place close to CPU socket VCCSENSE & VSSSENSE pins

NOTE:
De-populate PR164 and PR165 when CPU is present

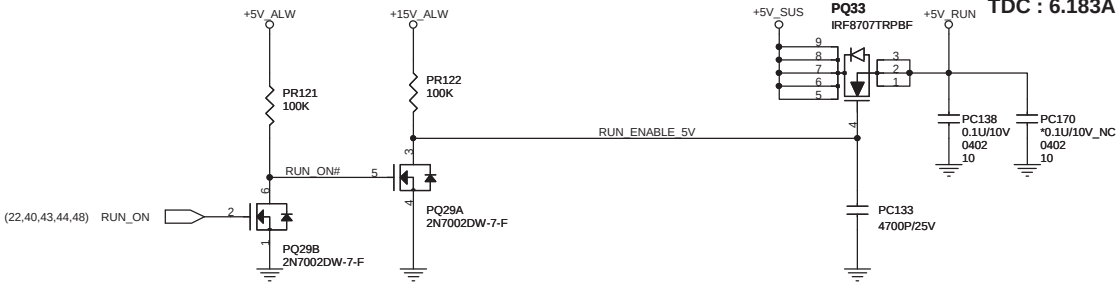
Place close to PC98

Place close to Phase1 output inductor.

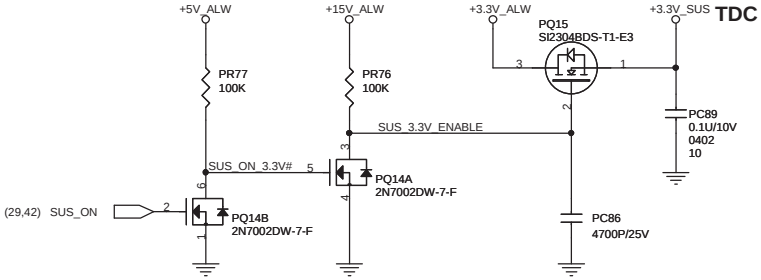
+VCC_CORE
Control IC: ADP3212
H/S MOSFET: FDMS7692(Fairchild), Qg=7nC, Rds(on)=13mohm, PD:2.5W
L/S MOSFET: FDMS0310S(Fairchild), Qg=15nC, Rds(on)=5.15mohm, PD:2.5W
Inductor: 0.36UH+-20%29.8A FDUE1040D-H-R36M=P3(Toko), DCR=0.79mohm
Output Cap: 4*330U 2V(20%,ESR=6,7343,H1.9)

Title	CPU core (ADP3212MNR2G)	
Size	Document Number UM9 UMA	Rev 1A
Date: Monday, February 01, 2010	Sheet 45 of 51	

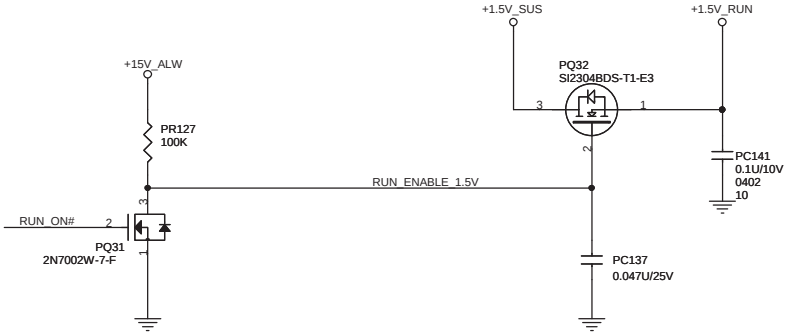
+5V_RUN
TDC : 6.183A

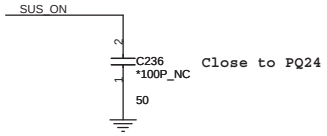


+3.3V_SUS
TDC : 0.26A

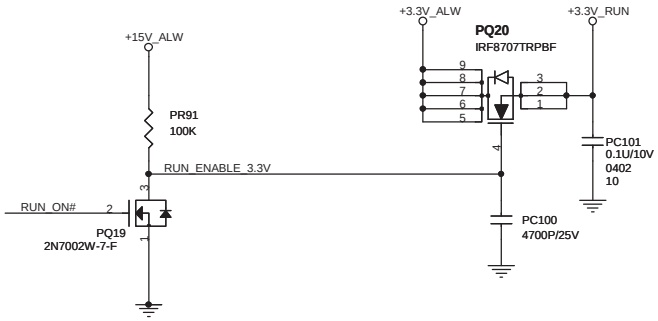


+1.5V_RUN
TDC : 0.35

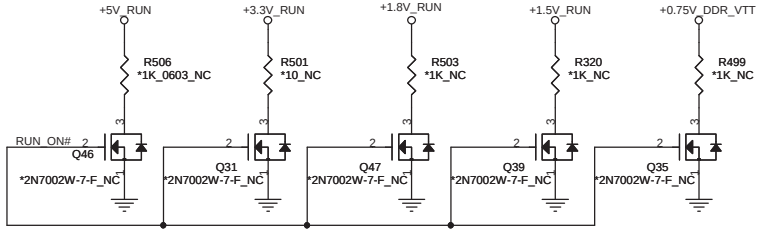


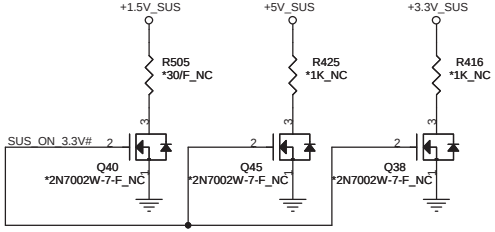


+3.3V_RUN
TDC : 4.886A



Reserve discharge path





QUANTA COMPUTER

Title	RUN / SUS POWER SW	
Size	Document Number UM9 UMA	Rev 2A
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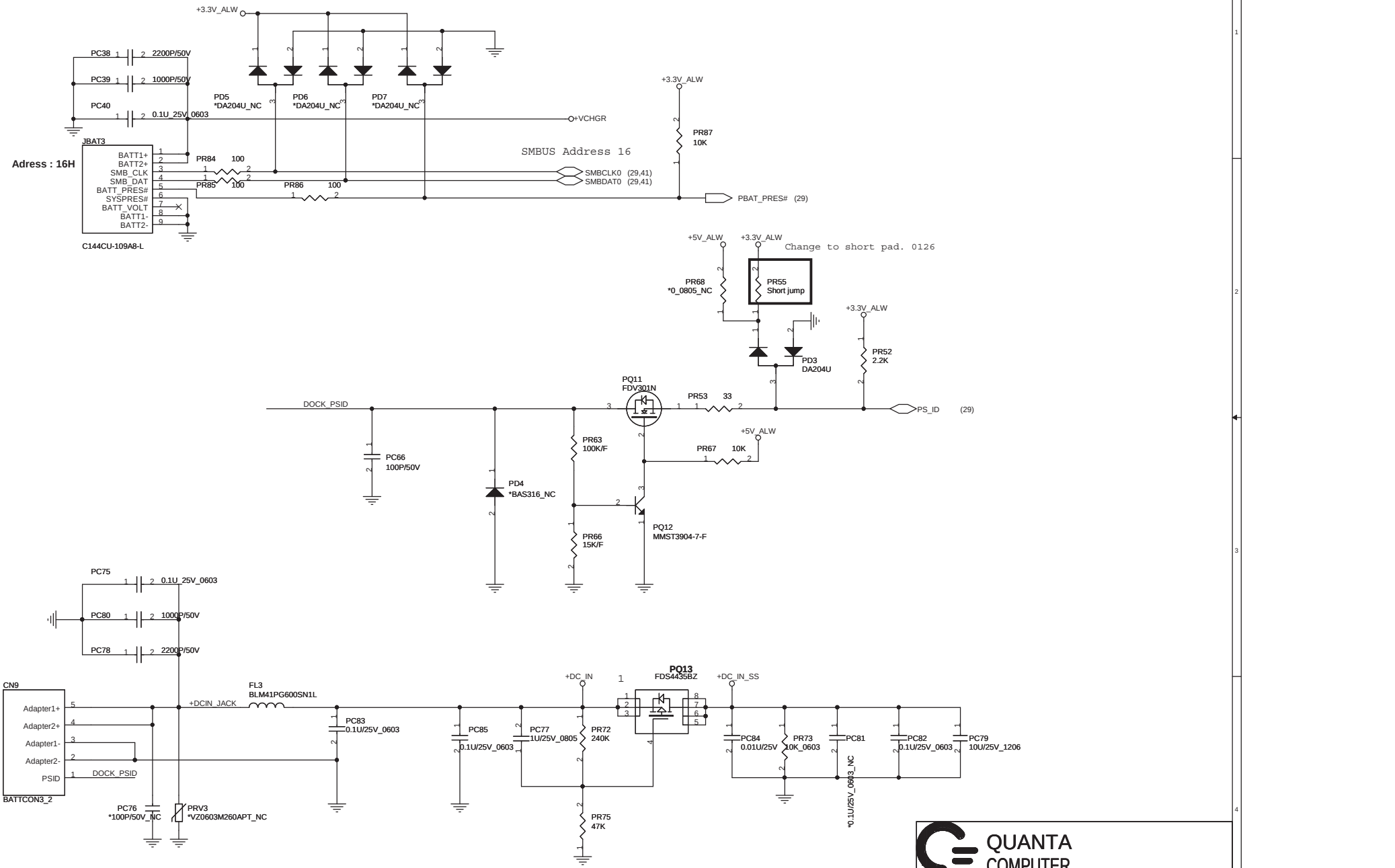
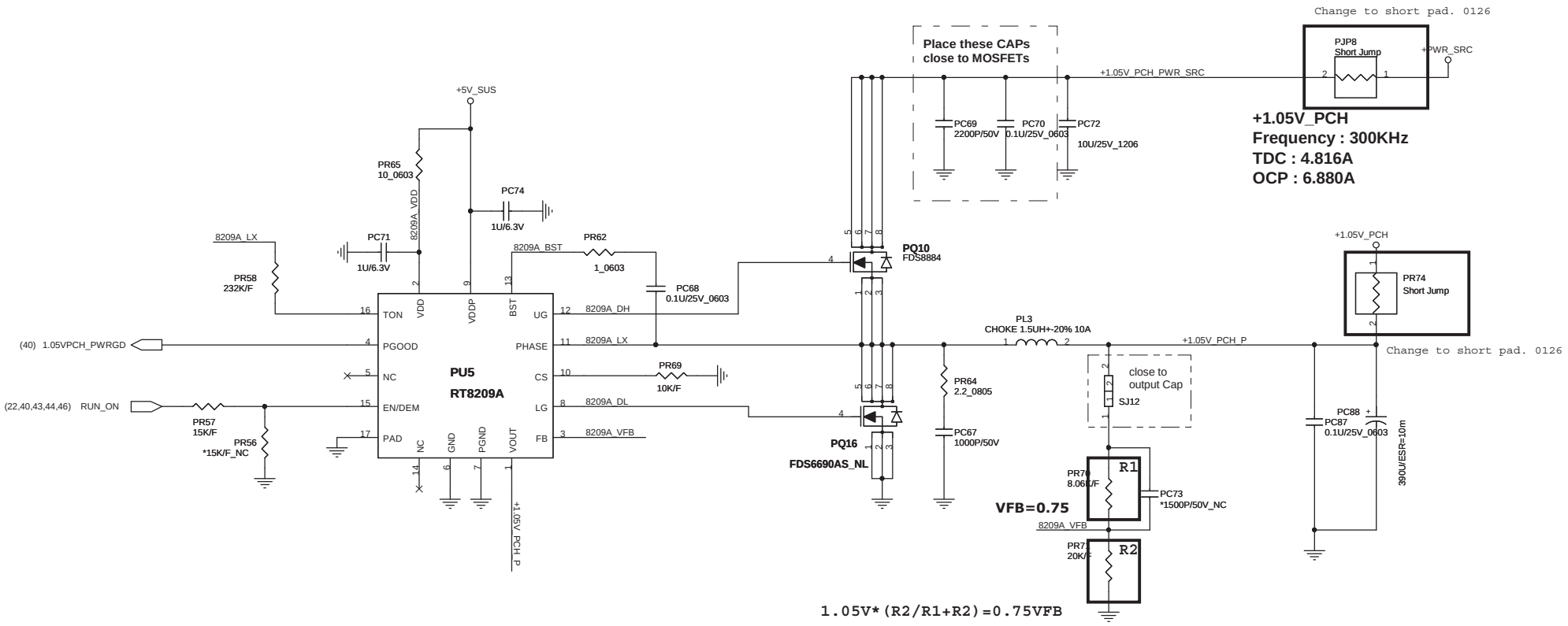


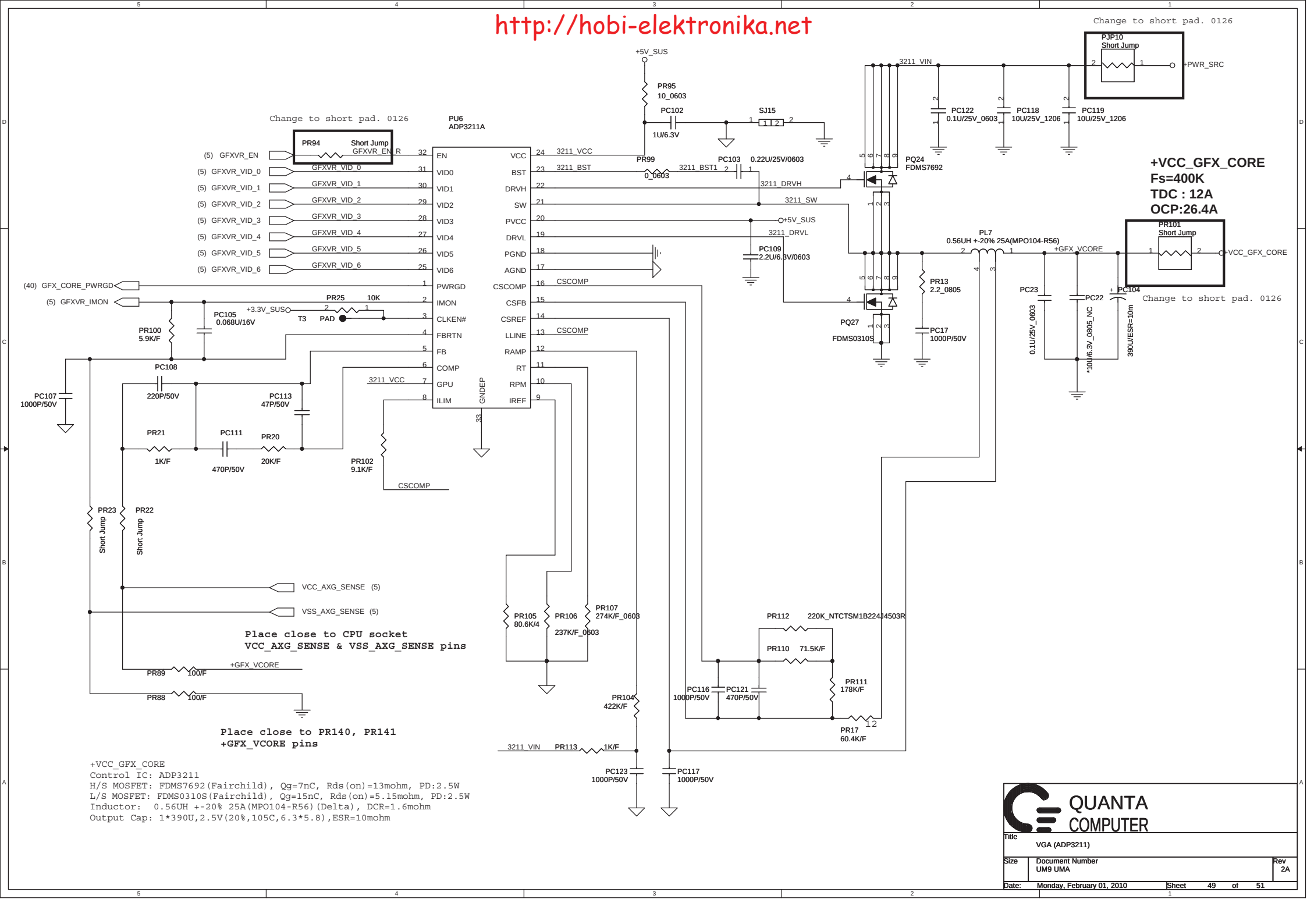
QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number UM9 UMA	Rev 2A
Date: Monday, February 01, 2010	Sheet 47 of 51	



+1.05V_PCH
Control IC: RT8209A
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
Inductor: 1.5UH+-20% 9A (10D40F-1R5M)(TTA), DCR=10.5mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm

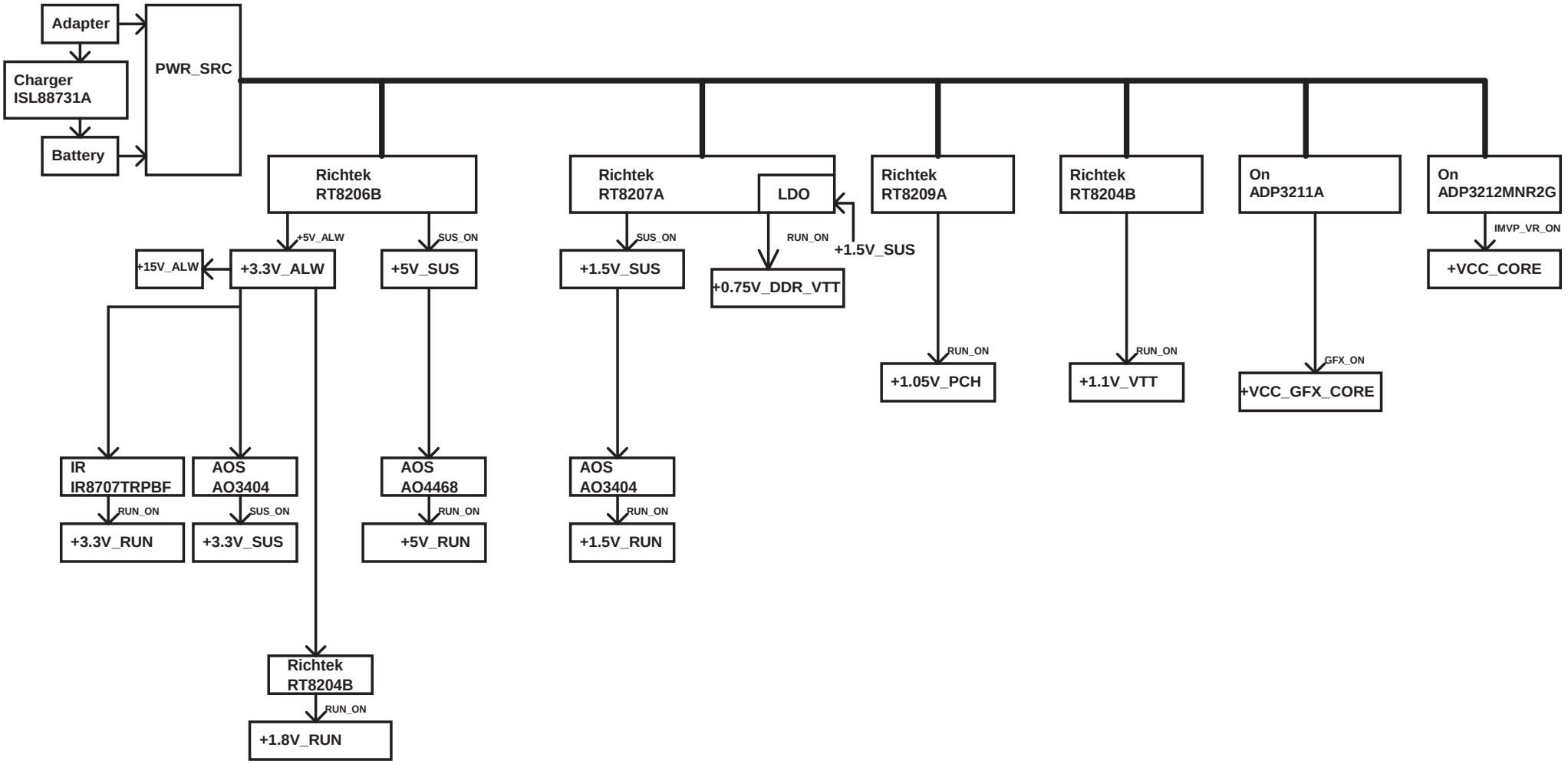
Title	+1.05V_PCH(RT8209A)	
Size	Document Number UM9 UMA	Rev 2B
Date: Monday, February 01, 2010	Sheet 48 of 51	



+VCC_GFX_CORE
Control IC: ADP3211
H/S MOSFET: FDMS7692(Fairchild), Qg=7nC, Rds(on)=13mohm, PD:2.5W
L/S MOSFET: FDMS0310S(Fairchild), Qg=15nC, Rds(on)=5.15mohm, PD:2.5W
Inductor: 0.56UH +-20% 25A(MPO104-R56)(Delta), DCR=1.6mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm

QUANTA COMPUTER

Title	VGA (ADP3211)		
Size	Document Number UM9 UMA		Rev 2A
Date: Monday, February 01, 2010		Sheet 49 of 51	



Quanta Computer Inc.

PROJECT : UM9 UMA

Size	Document Number	Rev
	Schematic Block Diagram1	1A

Date: Wednesday, January 27, 2010 Sheet 50 of 51

FM9 Power Design Block Diagram 2009/02/25

(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2) SYS_PWR_SW#
(3) 3.3V_ALW_ON, ALW_ON
(4) +3.3V_ALW, +5V_ALW, +15V_ALW
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
(7) ICH_RSMRST#
(8) SIO_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) GFX_ON
(11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
(12) RUN_ON_1(RUN_ON)
(13) +0.75V_DDR_VTT
(14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
(16) IMVP_VR_ON
(17) +VCC_CORE, IMVP_PWRGD
(18) RESET_OUT#
(19) ICH_PWRGD
(20) PM_DRAM_PWRGD
(21) CLK_CPU_BCLK(PCH to CPU)
(22) H_PWRGOOD
(23) PLTRST#(PCI_PLTRST#)

Power Jack
Adapter input
+DC_IN (1)
SI4835
+DC_IN_SS (1)
SI4835
+PWR_SRC (1)
Charger
ISL88731
Page 45
+VCHGR (1)
Battery
SI4835
+PWR_SRC (1)

+5V_VCC1 (from +5V_ALW2)
SYSTEM POWER
TPS51427A
Page 46
LDO
VR
+5V_ALW2 (1)
+3.3V_ALW (4)
+5V_ALW (4)
+3.3V_ALW_ON(From 3VALW ON POWER LOGIC) (3)
ALW_ON(For +5V_ALW and +15V_ALW turn on) (3)

(4) +5V_ALW
Diode & Cap
Page 46
+15V_ALW (4)
3V_ALW_PWRGD
5V_ALW_PWRGD

+5V_ALW
VRAM DDR3 POWER
TPS51116
Page 47
VR
LDO
+1.5V_SUS (6)
1.5V_DDR_PWRGD (6)
+0.75V_DDR_VTT (13)
(5) SUS_ON
(12) RUN_ON

+5V_ALW
PCH CORE POWER
TPS51218
Page 48
VR
+1.05V_PCH
1.05V_PWRGD (14)
(12) RUN_ON

(4) +5V_ALW
SI4800
Page 52
+5V_SUS (6)
(5) SUS_ON

(4) +3.3V_ALW
SI4800
Page 52
+3.3V_SUS (6)
(5) SUS_ON

(4) +5V_ALW
SI4800
Page 52
+5V_RUN (14)
(12) RUN_ON

(4) +3.3V_ALW
FDS8880
Page 52
+3.3V_RUN (14)
(12) RUN_ON

(14) +3.3V_RUN
SI2303
Page 17
+3.3V_DELAY (14)
(10) GFX_ON

(6) +1.5V_SUS
FDS6298
Page 52
+1.5V_RUN (14)
(12) RUN_ON

+5V_SUS
GFX CORE POWER
MAX8792ETD
Page 50
VR
+VCC_GFX_CORE
GFX_CORE_PWRGD (11)
(10) GFX_ON
(4) +5V_ALW

+5V_ALW (4)
GFX PCIE POWER
RT9018B
Page 50
VR
+1.1V_GFX_PCIE
GFX_PCIE_PWRGD (11)
(10) GFX_ON

+5V_ALW (4)
GFX POWER
RT9024PE
Page 44
VR
+1.8V_RUN_GFX
1.8V_RUN_GFX_PWRGD (14)
(12) RUN_ON

+5V_SUS
+3.3V_SUS
CPU CORE POWER
ISL6262A
TWO PHASE SOLUTION
Page 51
VR
+VCC_CORE
IMVP_PWRGD (17)
VR_PWRGD_CLKEN#
(16) IMVP_VR_ON

+5V_ALW (4)
CPU Memory Control & I/O Power
TPS51218
Page 49
VR
+1.1V_VTT
1.1V_VTT_PWRGD (14)
(12) RUN_ON

+5V_ALW (4)
CPU VCCPLL
RT9018B
Page 44
VR
+1.8V_RUN
1.8V_RUN_PWRGD (14)
(12) RUN_ON

(17) CK_PWRGD_R
CLK GEN
Page 15

Reset Circuit
Page 42
Inverter
AND Gate
Wire AND
AND Gate
(17) VR_PWRGD_CLKEN#
CK_PWRGD_R (17)
(6) 1.5V_DDR_PWRGD
(12) RUN_ON_1
RUN_ON (12)
(14) 1.1V_VTT_PWRGD
(14) 1.05V_PWRGD
(11) GFX_PCIE_PWRGD
(11) GFX_CORE_PWRGD
(14) 1.8V_RUN_PWRGD
(14) 1.8V_RUN_GFX_PWRGD
(17) IMVP_PWRGD
(18) RESET_OUT#
HWPG (15)
H_VTTPWRGD (15)
ICH_PWRGD (19)

(2) SYS_PWR_SW#
EC
IT8512
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3.3V_ALW_ON (3)
ALW_ON (3)
SUS_ON (5)
SIO_PWRBTN# (8)
ICH_RSMRST# (7)
SIO_SLP_S5# (9)
SIO_SLP_S3# (9)
(15) HWPG
RUN_ON_1 (12)
IMVP_VR_ON (16)
(17) IMVP_PWRGD
RESET_OUT# (18)

(19) ICH_PWRGD
PCH
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SIO_SLP_S4# (9)
To control DIMM VREF
PM_DRAM_PWRGD (20)
CLK_CPU_BCLK (21)
H_PWRGOOD (22)
PLTRST#(PCI_PLTRST#) (23)
(15) H_VTTPWRGD

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