Model Name : B4DBU(WIFI) / B4DBG(LTE)
File Name : LA-D301P
BOM P/N:43

ZZZ
LA-D301P
DAA000BG000
DA2@

ZZZ
LS-D303P FUN/B
DA400299000
DA2@

ZZZ
LS-D302P USB/B
DA6001HX000
DA2@

ZZZ
LS-A133P
DA600101010
DA2@

ZZZ
LS-D301P LID/B
DA400272000
DA2@

ZZZ
LS-B734P
DA6001B8010
DA2@

ZZZ
HDMI LOGO
RO0000003HM
HDMI@

ZZZ
LS-B732P
DA4001YF010
DA2@

ZZZ
DAZ PCB
DAZ1IB00100
DAZ@

Compal Confidential

B4DBU(WIFI) / B4DBG(LTE)
M/B Schematics Document

Skylake U Processor + DDR4 + Nvidia N16X

2015-12-09

Rev:1.0

UC1
S IC FJ8066201931104 SR2EU D1 2.3G ABO!
CPU_2NB0@
SA000092NB0

UC1
S IC FJ8066201930409 SR2EY D1 2.3G ABO!
CPU_2OB0@
SA000092OB0

UC1
S IC FJ8066201930408 SR2EZ D1 2.5G ABO!
CPU_2P90@
SA000092P90

UC1
S IC FJ8066201924931 QJKM D1 2.4G ABO!
CPU_2T50@
SA000092T50

UC1
S IC FJ8066201924931 SR2F0 D1 2.4G ABO!
CPU_2T80@
SA000092T80

UC1
S IC FJ8066201924950 QJKH D1 2.6G ABO!
CPU_2U70@
SA000092U70

UC1
S IC FJ8066201924950 SR2F1 D1 2.6G ABO!
CPU_2U80@
SA000092U80

Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

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Title: *Cover Page*

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Date: Thursday, December 17, 2015 Sheet 1 of 63

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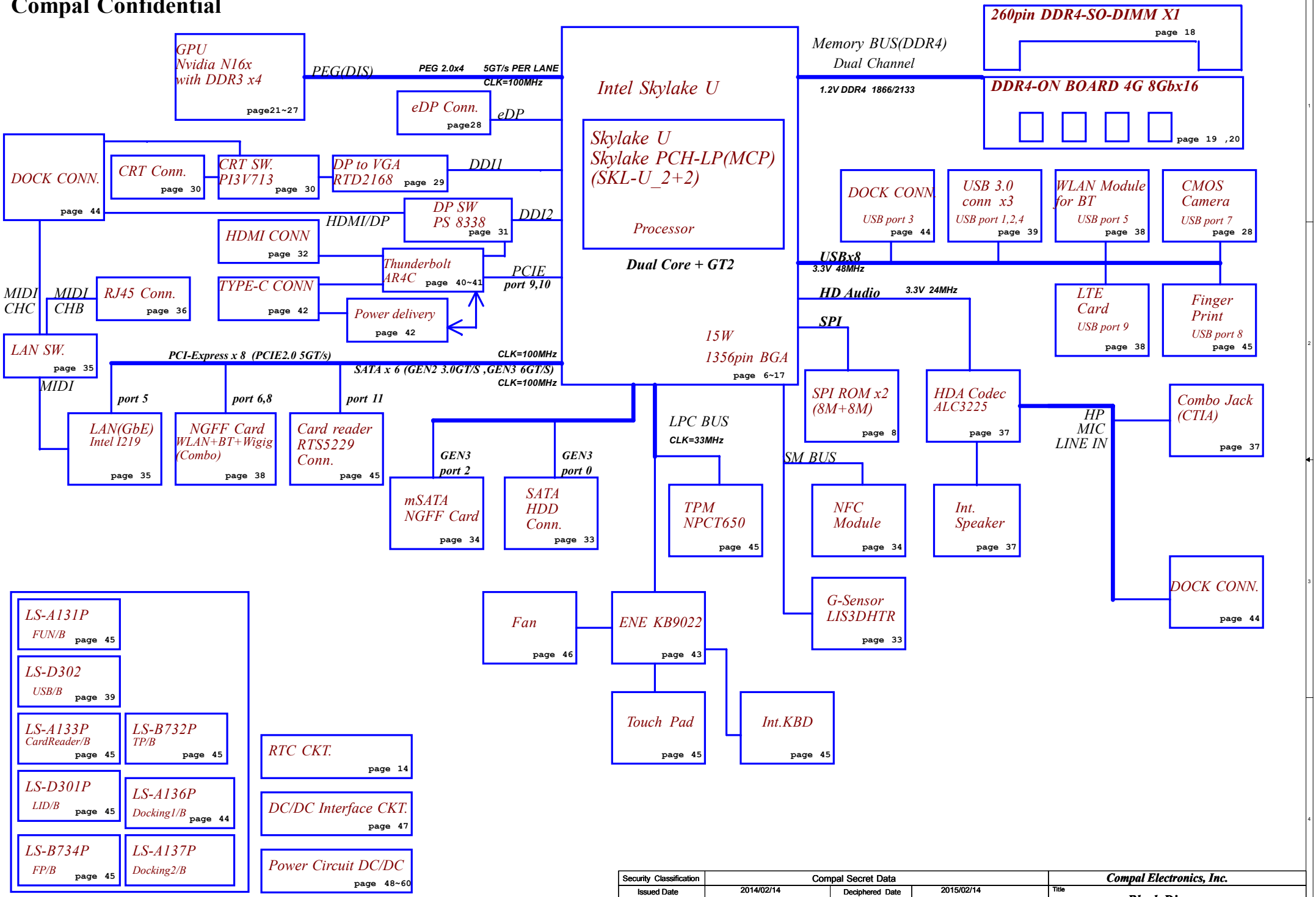

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Title: **Block Diagrams**

Size	Document Number	Rev
Custom	LA-D301P	0.1

Date: Thursday, December 17, 2015 | Sheet 2 of 63

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3
0	0	0 V	0 V	0.300 V	0x00 - 0x0B
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x0C - 0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C - 0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BOM Structure Table

BOM Option Table	
Item	BOM Structure
Unpop	@
Connector	CONN@
EMC requirement	EMC@
EMC requirement depop	@EMC@
EMI requirement	@EMC@/EMI@
Thunderbolt Funct i on	TBT@
RF requirement	@RF@/RF@
LTE Funct i on	3G@
UMA only	UMA@
VPRO Funct i on	VPRO@/NOVPRO@
VGA EMI Requirement	@VGA_EMI@/VGA_EMI@
VGA UNPOP	@VGA@
VGA RF Requirement	@RF@_VGA@
VGA Power	22@/23E@
GC6 Funct i on	GC6@/NOGC6@/NGC6
INTEL CMC	CMC@
ESPI	ESPI @

BOM Option Table	
Item	BOM Structure
dGPU	VGA@
SAMSUNG DDR4	X76SAM@
N16S-GT	SGT@
Without WiGi Funct i on	NOWG@
HDD Redriver	X76TI@/X76PAR@
GPU CG6 funct i on	VGM@
VRAM BOM Select	X76@
Single/Dual Rank	SR@/DR@ (DR@ is not been used in this project)
PD Funct i on	PD@
CPU Code	QH7Y@
CPU Code	QH7Y@

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VSDGPU	+1.05VS power rail for GPU	ON	OFF	OFF
+1.5VSDGPU	+1.5VS power rail for GPU	ON	OFF	OFF
+3VSDGPU_AON	+3VS power rail for GPU(AON rails)	ON	OFF	OFF
+3VSDGPU_MAIN	+3VS power rail for GPU GC62.0	ON	OFF	OFF
+VGA_CORE	Core power for descrete GPU	ON	OFF	OFF
+2.5V	DDR4 +2.5V Power Rail	ON	ON	OFF

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit) Write	Address(8bit) Read
I2C_0 (+3VS)	Reserved (Touch Panel)			
I2C_1 (+3VS)	TM-P2969-001 (TP)	0x2C		
	SB8787-1200 (TP-ELAN)	0x16		
SOC_SMBCLK +3VS	DIMM1	0xA0		
	DIMM2	0xA4		
	LIS3DHTR(G-Sensor)	0x30		
SOC_SML1CLK +3VS	N16S-GT (VGA)	0x9E		
	PCH-LP (SOC)	0x90		
EC_SMB_CK1 +3VLP	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		
SOC_SML0CLK +3VS	LAN	0xC8		
	NFC	0x28		

43 level BOM table

43 Level	Description	BOM Structure
431A0NBOL01	SMT MB AD301 B4DBG QJFC 2.3G UMA HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/HDMI@/NOVPRO@/PD@/TBT@/UMA@/X76PAR@/X76SAM@/RF@
431A0NBOL02	SMT MB AD301 B4DBG QJ8M 2.4G UMA HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/HDMI@/NOVPRO@/PD@/TBT@/UMA@/X76PAR@/X76SAM@/RF@
431A0NBOL03	SMT MB AD301 B4DBG QJKP 2.3G DIS HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/GC6@/HDMI@/PD@/SGT@/TBT@/VGA@/VGA_EMI@/VPRO@/X76PAR@/X76SAM@/RF@
431A0NBOL04	SMT MB AD301 B4DBG QJKK 2.5G DIS HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/GC6@/HDMI@/PD@/SGT@/TBT@/VGA@/VGA_EMI@/VPRO@/X76PAR@/X76SAM@/RF@

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Title: Notes List

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Date: Thursday, December 17, 2015 | Sheet 3 of 63

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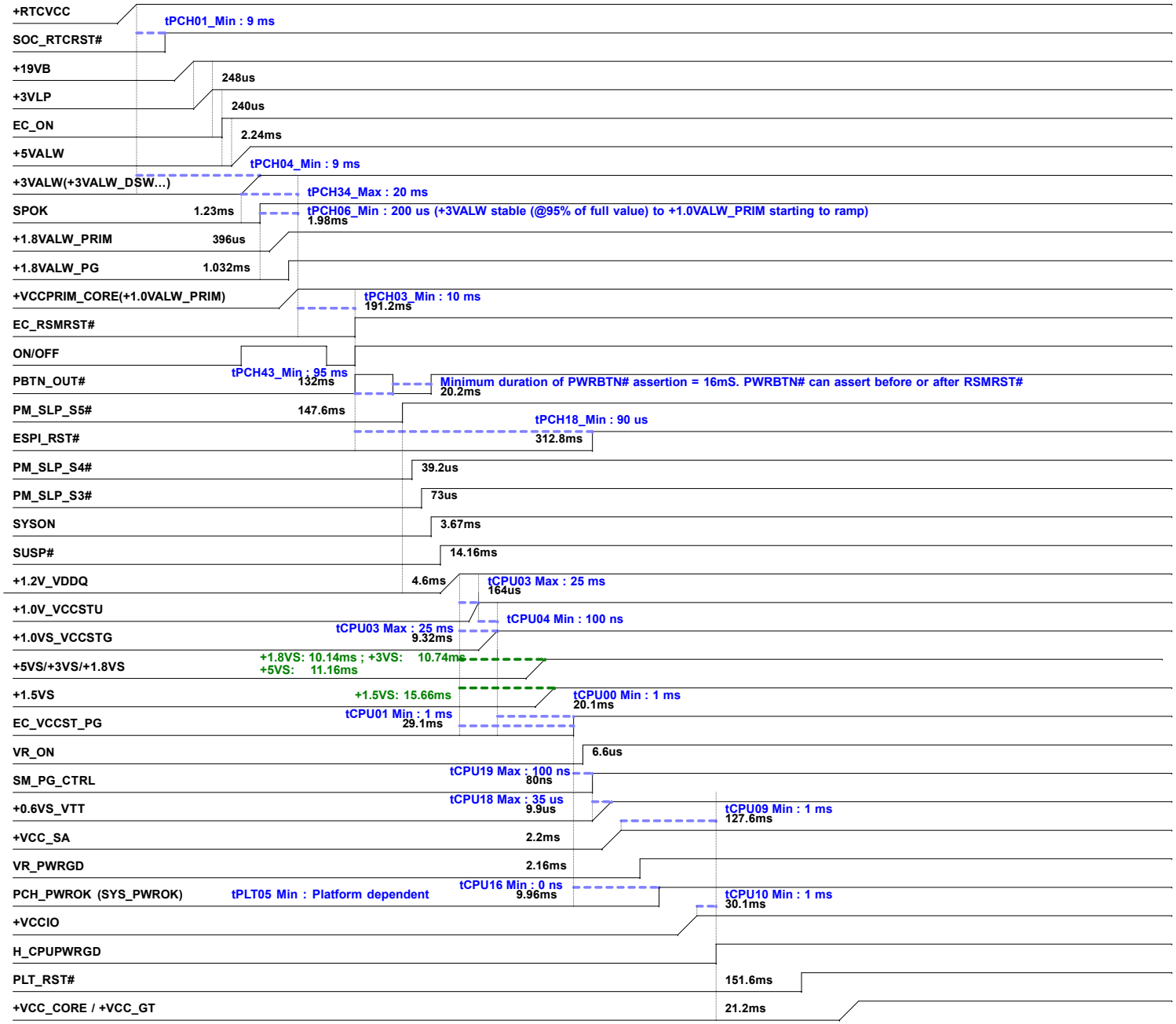
Title: Power Map

Size: Custom | Document Number: LA-D301P | Rev: 0.2

Date: Thursday, December 17, 2015 | Sheet 4 of 63

PWR Sequence_SKL-U2+2_DDR4_Value_NON CS



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Compal Electronics, Inc.

Title: **Power Sequence**

Size	Document Number	Rev
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Functional Strap Definitions

#543016 PDG0.9 P.775

DDPB_CTRLDATA/ GPP_E19 (Internal Pull Down):
DDPC_CTRLDATA/ GPP_E21 (Internal Pull Down):
DDPD_CTRLDATA/ GPP_E23 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)
Display Port B/C/D Detected
0 =Port is not detected.
1 =Port is detected.

<DP to VGA>

< PS8338 >
Docking HDMI+TBT

UC1A SKL-U Rev_0.53

DDI1_TXN[0] DDI1_TXP[0] DDI1_TXN[1] DDI1_TXP[1] DDI1_TXN[2] DDI1_TXP[2] DDI1_TXN[3] DDI1_TXP[3] DDI2_TXN[0] DDI2_TXP[0] DDI2_TXN[1] DDI2_TXP[1] DDI2_TXN[2] DDI2_TXP[2] DDI2_TXN[3] DDI2_TXP[3] DDI EDP DISPLAY SIDEBANDS

EDP_TXN[0] EDP_TXP[0] EDP_TXN[1] EDP_TXP[1] EDP_TXN[2] EDP_TXP[2] EDP_TXN[3] EDP_TXP[3] EDP_AUXN EDP_AUXP EDP_DISP_UTIL

<eDP>

DDI1_AUXN DDI1_AUXP DDI2_AUXN DDI2_AUXP DDI3_AUXN DDI3_AUXP

DP Aux (Port B for VGA)
PS8338

GPP_E18/DDPB_CTRLCLK GPP_E19/DDPB_CTRLDATA GPP_E20/DDPC_CTRLCLK GPP_E21/DDPC_CTRLDATA GPP_E22/DDPD_CTRLCLK GPP_E23/DDPD_CTRLDATA EDP_RCOMP

GPP_E13/DDPB_HPD0 GPP_E14/DDPC_HPD1 GPP_E15/DDPD_HPD2 GPP_E16/DDPE_HPD3 GPP_E17/EDP_HPD EDP_BKLTEN EDP_BKLTCTL EDP_VDDEN

1 OF 20

SKL-U_BGA1356

SOC_DP1_HPD CPU_HDMI_HPD EC_SCI# CPU_EDP_HPD ENBKL SOC_BKL_PWM SOC_ENVDD

From VGA Trans.
From DP MUX
From eDP

EC_SCI# SOC internal PU

#545659 PCH EDS 0.7 P.108
SCI capability is available on all GPIOs,
while NMI and SMI capability is available on selected GPIOs only.
Below are the PCH GPIOs that can be routed to generate SMI# or NMI:
- GPP_B14 GPP_B20 GPP_B23
- GPP_C[23:22]
- GPP_C[4:0]
- GPP_E[8:0], GPP_E[16:13]

COMPENSATION PU FOR eDP

#543016 PDG0.9 P.186
Trace width=20 mils,Spacing=25mil,Max length=100mils

#543016 PDG0.9 P.753
PH 1K to VCCST
CPU over 130 degree will output low force S0->S5

UC1D SKL-U Rev_0.53

CATERR# PECI PROCHOT# THERMTRIP# SKTOCC# CPU MISC BPM#[0] BPM#[1] BPM#[2] BPM#[3] GPP_E3/CPU_GP0 GPP_E7/CPU_GP1 GPP_B3/CPU_GP2 GPP_B4/CPU_GP3 PROC_POPIRCOMP PCH_OPIRCOMP OPCE_RCOMP OPC_RCOMP

JTAG

PROC_TCK PROC_TDI PROC_TDO PROC_TMS PROC_TRST# PCH_JTAG_TCK PCH_JTAG_TDI PCH_JTAG_TDO PCH_JTAG_TMS PCH_TRST# JTAGX

CPU_XDP_TCK0 SOC_XDP_TDI SOC_XDP_TDO SOC_XDP_TMS SOC_XDP_TRST# PCH_JTAG_TCK1 SOC_XDP_TDI SOC_XDP_TDO SOC_XDP_TMS SOC_XDP_TRST# CPU_XDP_TCK0

4 OF 20

SKL-U_BGA1356

PDG0.9 P.771
PROC_POPIRCOMP/PCH_OPIRCOMP
PD 50ohm

#544669 CRB RVP7 1.0
EDRAM_OPIO_RCOMP/EOPIO_RCOMP
PD50ohm

Reserved for ESD 2014/9/17

APS CONN

JAPS1 ACES_50506-01841-P01 CONN@

PM_SLP_S3# PM_SLP_S5# PM_SLP_S4# PM_SLP_A# SOC_RTCRST# PBTN_OUT#_R2 SYS_RESET# PM_SLP_S0# GND GND

Place to CPU side

SOC_XDP_TMS SOC_XDP_TDI SOC_XDP_TDO

CMC@ RPC2 0_0804_8P4R_5%

XDP_ITP_PMODE XDP_PRSENT_CPU XDP_HOOK6 XDP_SPI_SI XDP_SPI_IO2 XDP_HOOK3 XDP_TCK1 XDP_TCK0 XDP_PRSENT_PCH CMC@ RPC15 0_0804_8P4R_5%

CPU_XDP_TCK0 PCH_JTAG_TCK1 CFG0 EC_RSMRST# XDP_HOOK0

Follow 544924_Skylake_EDS_Vol_1_Rev_0.93

XDP CONN

JPCMC1 CMC_DEBUG_36P

OBS DATA JTAG/RC/HOOKS

DATA_0 DATA_1 DATA_2 DATA_3 DATA_4 DATA_5 DATA_6 DATA_7 DATA_CLK_1P DATA_CLK_1N DATA_8 DATA_9 DATA_10 DATA_11 DATA_12 DATA_13 DATA_14 DATA_15 DATA_CLK_2P DATA_CLK_2N

CFG0 CFG1 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7 CFG17 CFG16 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG19 CFG18

VCCOBS_AB XDP_TRST# XDP_TDI XDP_TMS XDP_TCK0 XDP_TCK1 XDP_TDO XDP_PREQ# XDP_PRDY# XDP_HOOK0 XDP_HOOK3 XDP_HOOK6 XDP_PRSENT_PCH XDP_PRSENT_CPU GND <MT> GND

INTEL_CMC_PRIMARY CONN@

PBTN_OUT# ON/OFF#

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Title: SKL-U(1/12)DDI,MSIC,XDP,EDP

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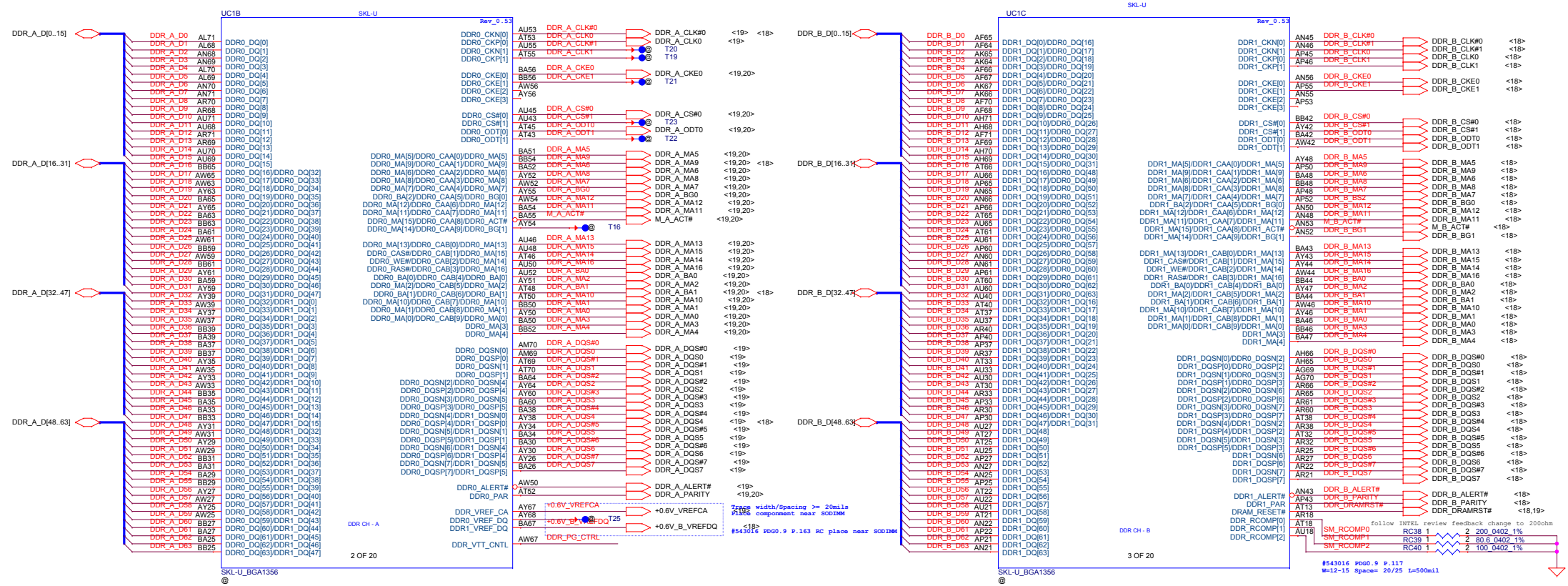
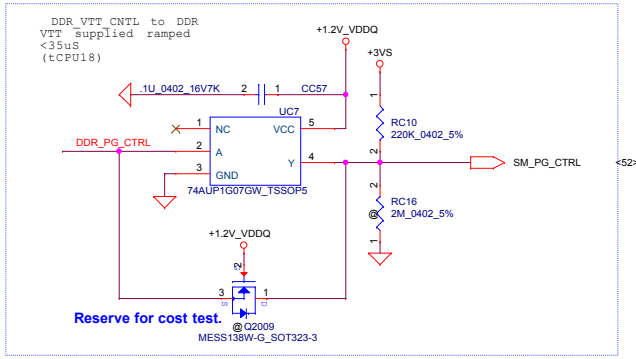
Interleaved Memory





ES Sample

UC1 CPU_QHMF_C0_2.3G QHMF@ SA00008M420

UC1 CPU_QHMG_C0_1.6G QHMG@ SA00008M320

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Title: SKL-U(2/12)DDR

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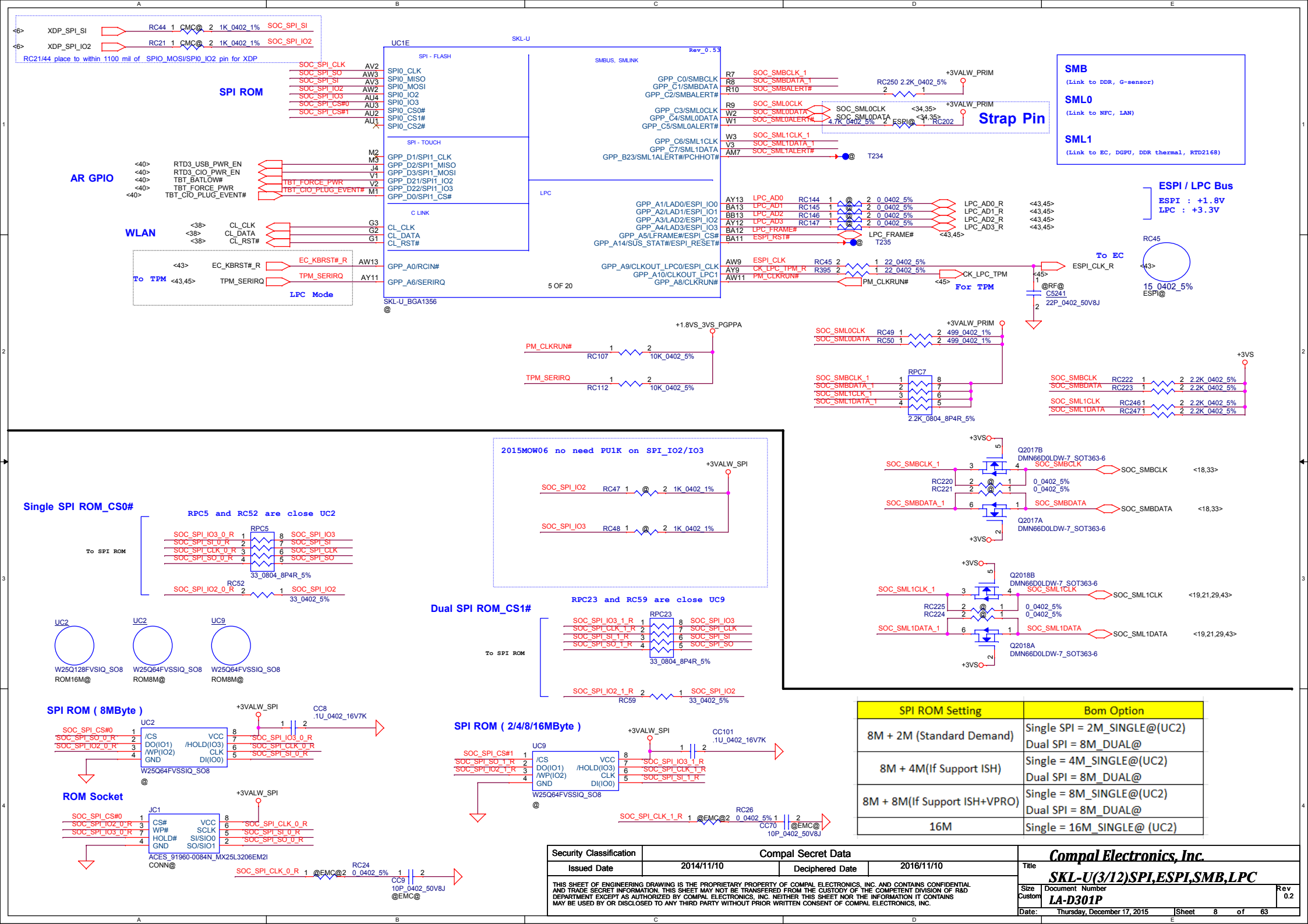

SPI ROM Setting	Bom Option
8M + 2M (Standard Demand)	Single SPI = 2M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 4M(If Support ISH)	Single = 4M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 8M(If Support ISH+VPRO)	Single = 8M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
16M	Single = 16M_SINGLE@ (UC2)

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: SKL-U(3/12)SPI,ESPI,SMB,LPC

Size	Document Number	Rev
Custom	LA-D301P	0.2

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#545659 SKL_PCH_EDS_R0.7 P.84

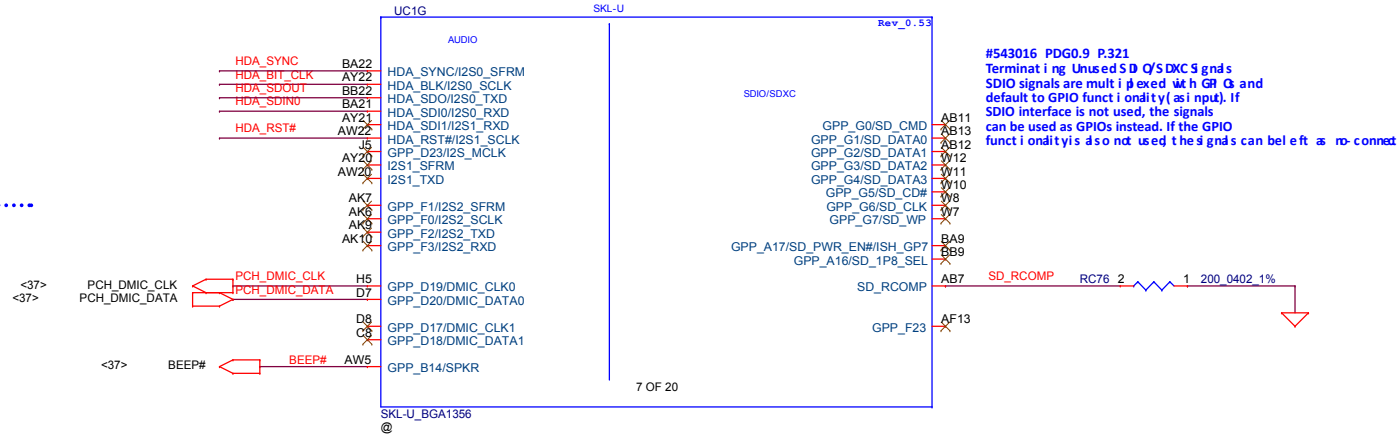
11.7.3 Intel HD Audio link capabilities

- Two SDI signals to support two external codecs.
- Drives variable frequency (6 MHz to 24 MHz) BCLK to support:
  - SDO double pumped up to 48 Mb/s
  - SDI's single pumped up to 24 Mb/s
- Provides cadence for 44.1 kHz-based sample rate output.
- Supports 1.5V, 1.8V and 3.3V modes.

Functional Strap Definitions

SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

TOP Swap Override
0 = Disable TOP Swap mode.---> AAX05 Use
1 = Enable TOP Swap Mode.



#543016 PDG0.9 P.321
Terminating Unused SDIO/SDXC Signals
SDIO signals are multiplexed with GPIOs and default to GPIO functionality(as input). If SDIO interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect

SD_RCOMP RC76 2 1 200_0402_1%

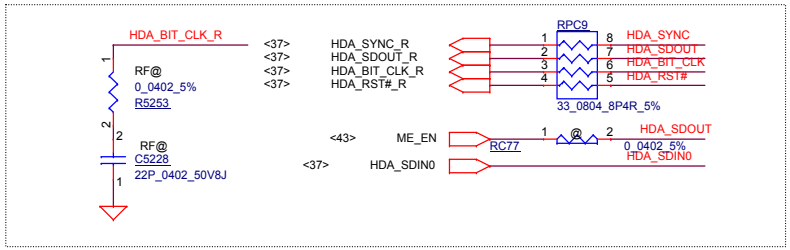
62.3.38 RCOMP Checklist

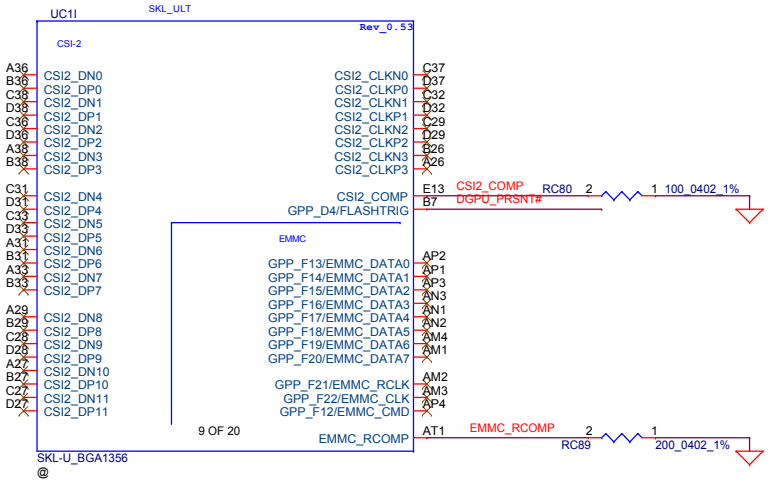
Table 62-48. RCOMP Checklist

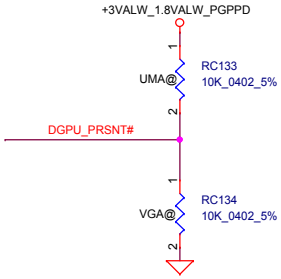
Component	Value	✓
NOA_RCOMP	49.9 ohm +/- 1% pull down termination to GND	
PEG_COMP	24.9ohm +/- 1% pull down termination to GND	
SD_RCOMP	200ohms termination to GND.	
EMMC_RCOMP	200ohms termination to GND.	
PCIE_RCOMPP/N	100 ohm +/- 1%. Differential between RCOMPP/RCOMPN	
USB2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	

SD_RCOMP	200ohms termination to GND.	
EMMC_RCOMP	200ohms termination to GND.	
PCH_POPIRCOMP	DC resistance <0.2ohm. 49.9 ohm termination resistor to GND.	
PCIE_RCOMPP/N	100 ohm +/- 1%. Differential between RCOMPP/RCOMPN	
CSI2_COMP	100 ohm +/- 1% termination resistor to GND; DC resistance <0.5ohm.	
USB2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	

HDA for AUDIO







	GPIO67 DGPU_PRSNT#
DIS,Optimus	0
UMA	1

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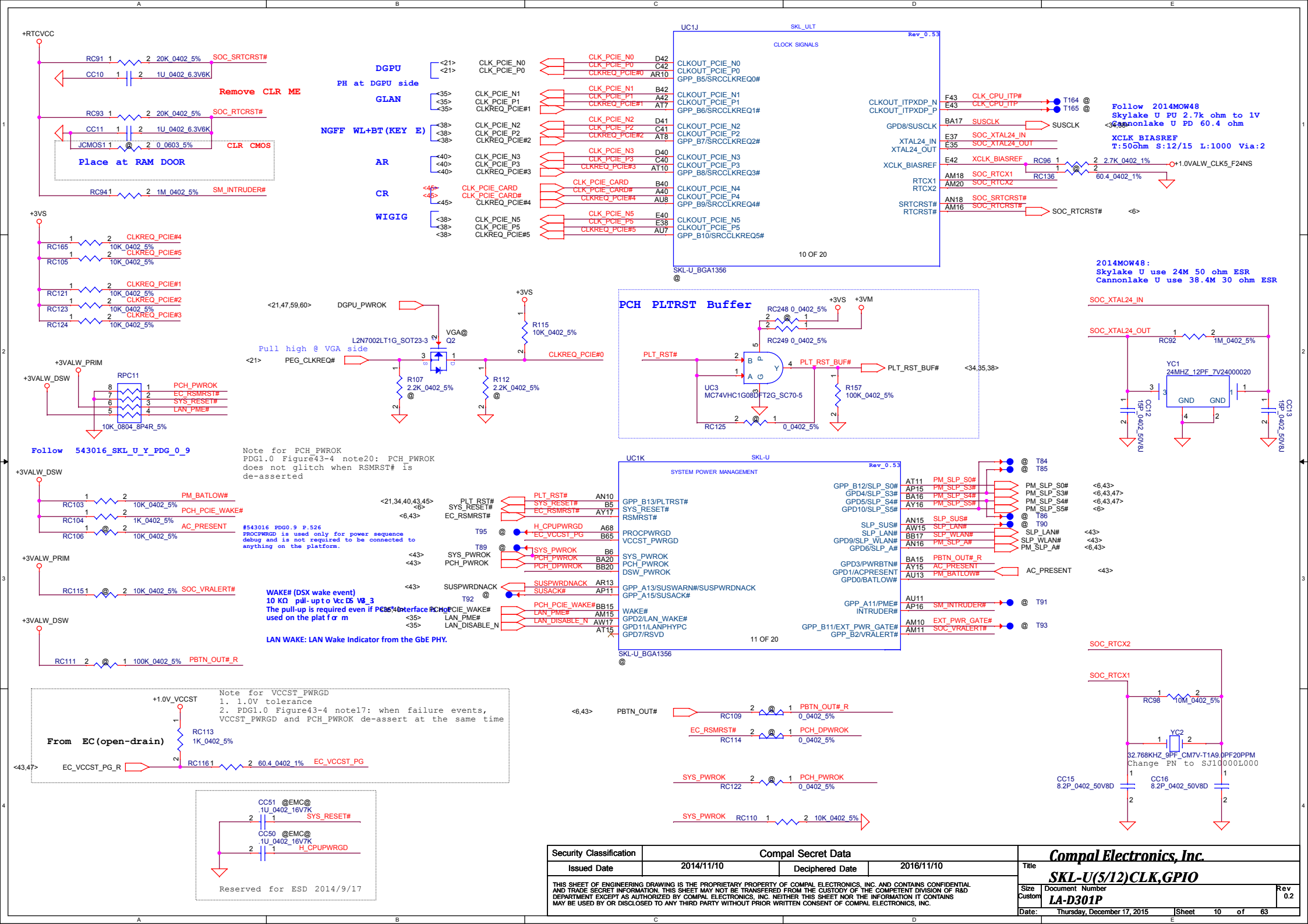
Issued Date	2014/11/10	Deciphered Date 2016/11/10

Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

Size: Custom | Document Number: LA-D301P | Rev: 0.2

Date: Thursday, December 17, 2015 | Sheet 9 of 63



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.			
Title	SKL-U(5/12)CLK,GPIO		
Size	Document Number		Rev
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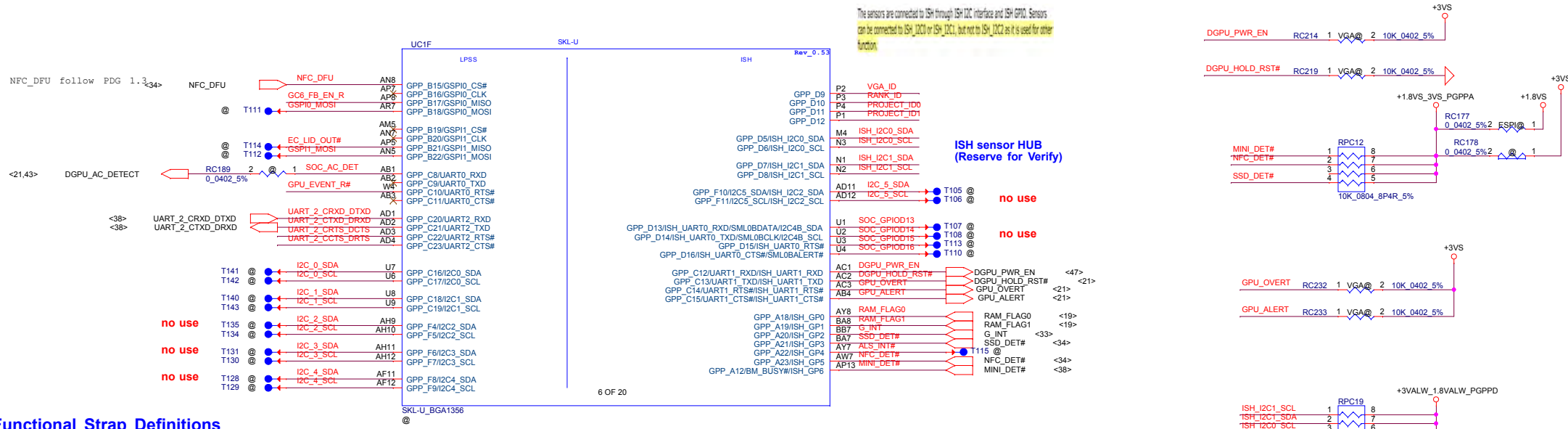
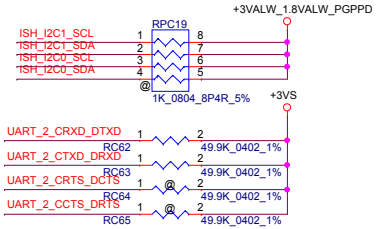
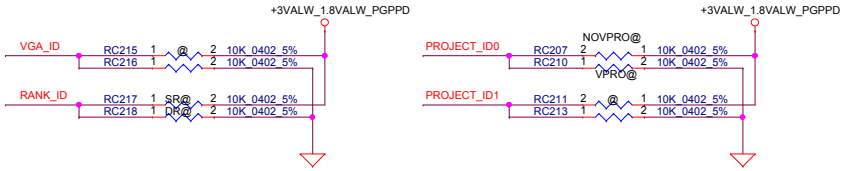
Date:	Thursday, December 17, 2015	Sheet	10 of 63

543016 SKY PDG 0.9 P.401

The sensors are connected to ISH through ISH I2C interface and ISH GPIO. Sensors can be connected to ISH_I2C0 or ISH_I2C1, but not to ISH_I2C2 as it is used for other function.







Functional Strap Definitions

SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

TOP Swap Override
*** 0 = Disable TOP Swap mode.---> AAX05 Use**
1 = Enable TOP Swap Mode.

GSPI0_MOSI /GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

*** 0 = Disable No Reboot mode. --> AAX05 Use**
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

Boot BIOS Strap Bit
*** 0 = SPI Mode --> AAX05 Use**
1 = LPC Mode

SML0ALERT# / GPP_C5 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

eSPI or LPC
*** 0 = LPC is selected for EC --> For KB9022/9032 Use**
1 = eSPI is selected for EC --> For KB9032 Only.

SMBALERT# / GPP_C2 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

TLS Confidentiality
*** 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).**
1 = Enable Intel ME Crypto (TLS) (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

VGA_ID	GPP_D9
GL	0
GM	1

RANK_ID	GPP_D10
DR	0
SR	1

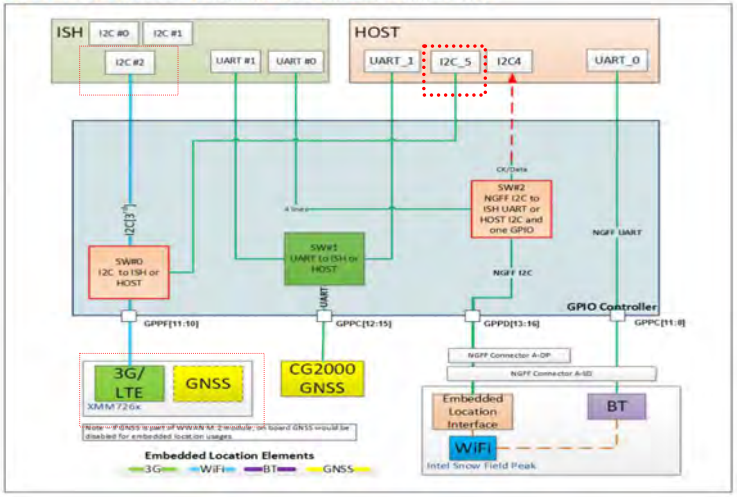
Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
*B4DBU+VPRO	0	0
B4DBU+NVPRO	0	1
Reserved	1	0
Reserved	1	1

HDA_SDO/I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Flash Descriptor Security Override
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

DDPB_CTRLDATA/ GPP_E19 (Internal Pull Down):
DDPC_CTRLDATA/ GPP_E21 (Internal Pull Down):
DDPD_CTRLDATA/ GPP_E23 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)
Display Port B/C/D Detected
0 =Port D is not detected.
1 =Port D is detected.

I2C/ISH Port(From PDG 0.9)

Figure 64-1. Embedded Location - Host and ISH Connectivity



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Compal Electronics, Inc.	
Title	SKL-U(6/12)GPIO
Size: Custom	Document Number: LA-D301P
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Date: Thursday, December 17, 2015	Sheet 11 of 63

UC1H

SKL-U

Rev_0.53

PCIE/USB3/SATA

SSIC / USB3

USB2

8 OF 20

SKL-U_BGA1356

@

DGPU

GLAN

NGFF WLAN+BT(Key E)

HDD

Wigig

Thunderbolt

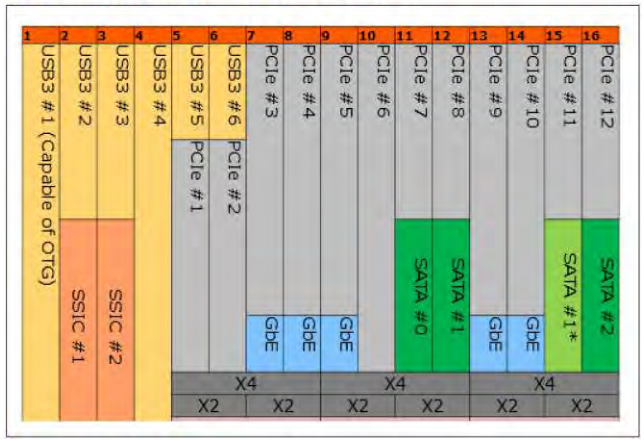
CR

SSD

#543016 P.239 PCIE_RCOMPN/PCIE_RCOMPP
BO=4 W=12 S=12 R=100ohm

Acer HSIO def i ne
3.3 Intel SKYLAKE one chip.

High Speed I/O (HSIO) Lane Multiplexing in SKL U



GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1,2,4
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	SSD
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

DEVSLP[2:0] Implementation
DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.
The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.
•When high, DEVSLP requests the SATA device to enter into the DEVSLP power state.
•When low, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

SATA General Purpose (SATAGP[2:0]) Signals
•The processor provides three SATA general purpose input signals,SATAGP[2:0] for SKL U. These signals can be configured as interlock switch inputs corresponding to a given SATA port.
•When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.
•If mechanical presence switches will not be used on the platform, SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

NFC_IRQ,RST# follow PDG 1.3

AG3,AG4 PD1K for DCI warm boot fail issue (follow PCH EDS1.2)
2015MOW10, USB2_ID connected to GND

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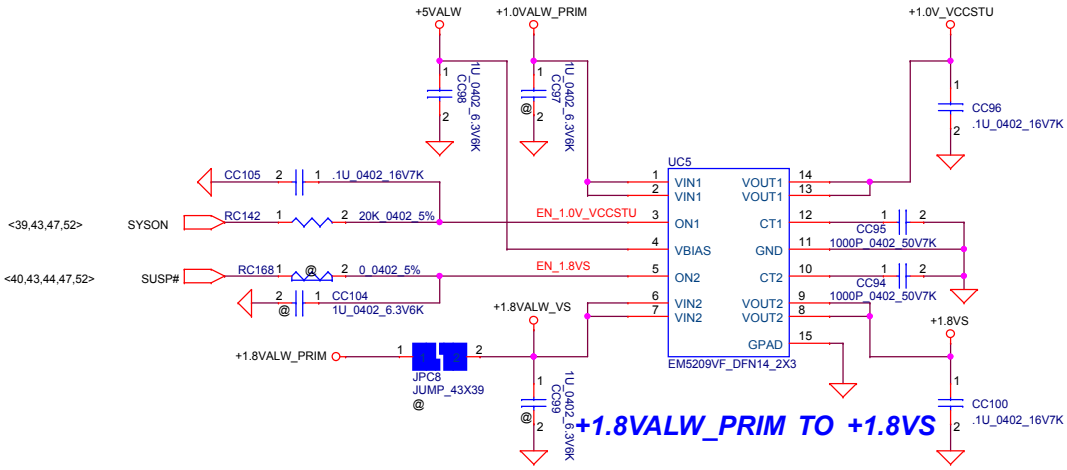
Compal Electronics, Inc.

Title: SKL-U(7/12)PCIE,USB,SATA

Size: Custom | Document Number: LA-D301P | Rev: 0.2

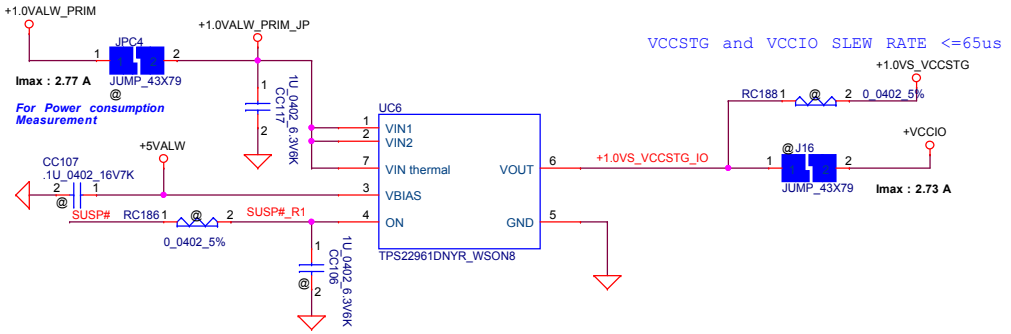
Date: Thursday, December 17, 2015 | Sheet 12 of 63

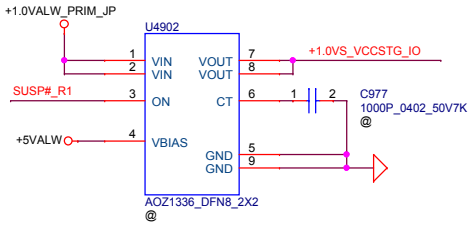
+1.0VALW_PRIM TO +1.0V_VCCSTU / +1.0VCCST

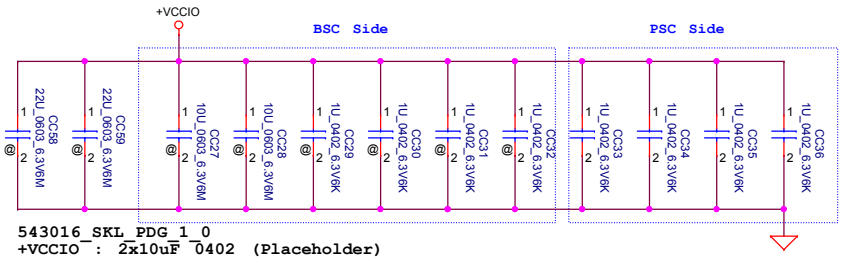


+1.8VALW_PRIM TO +1.8VS

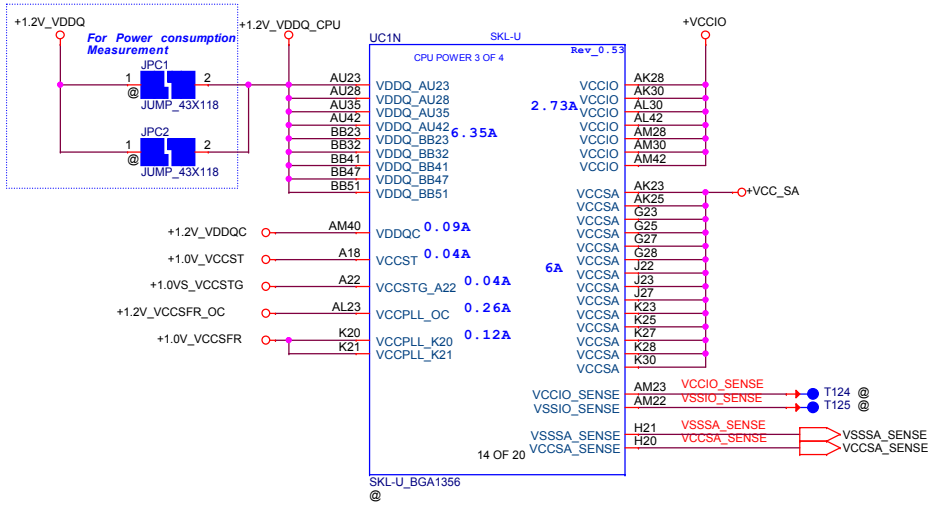
+1.0VALW_PRIM TO +1.0VS_VCCSTG

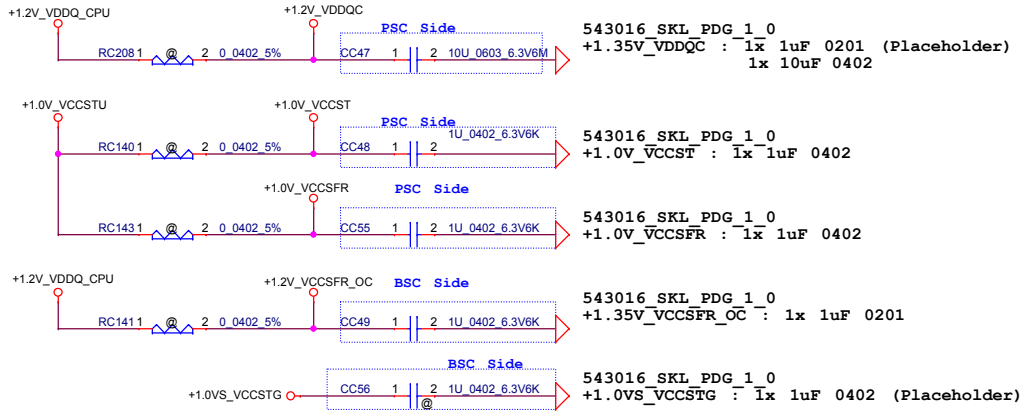






543016_SKL_PDG_1_0
+VCCIO : 2x10uF 0402 (Placeholder)
4x 1uF 0201 (Placeholder)
4x 1uF 0402





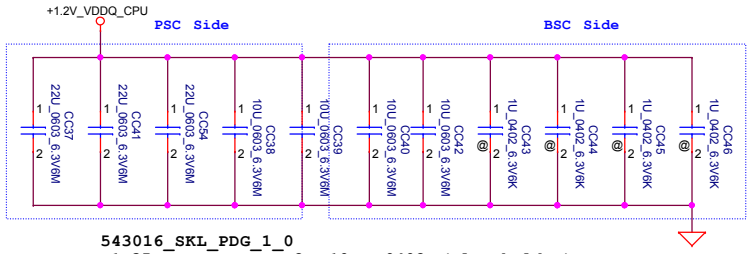
543016_SKL_PDG_1_0
+1.35V_VDDQC : 1x 1uF 0201 (Placeholder)
1x 10uF 0402

543016_SKL_PDG_1_0
+1.0V_VCCST : 1x 1uF 0402

543016_SKL_PDG_1_0
+1.0V_VCCSFR : 1x 1uF 0402

543016_SKL_PDG_1_0
+1.35V_VCCSFR_OC : 1x 1uF 0201

543016_SKL_PDG_1_0
+1.0VS_VCCSTG : 1x 1uF 0402 (Placeholder)



543016_SKL_PDG_1_0
+1.35V_VDDQ_CPU : 2x 10uF 0402 (Placeholder)
4x 1uF 0201 (Placeholder)
4x 10uF 0402
3x 22uF 0603

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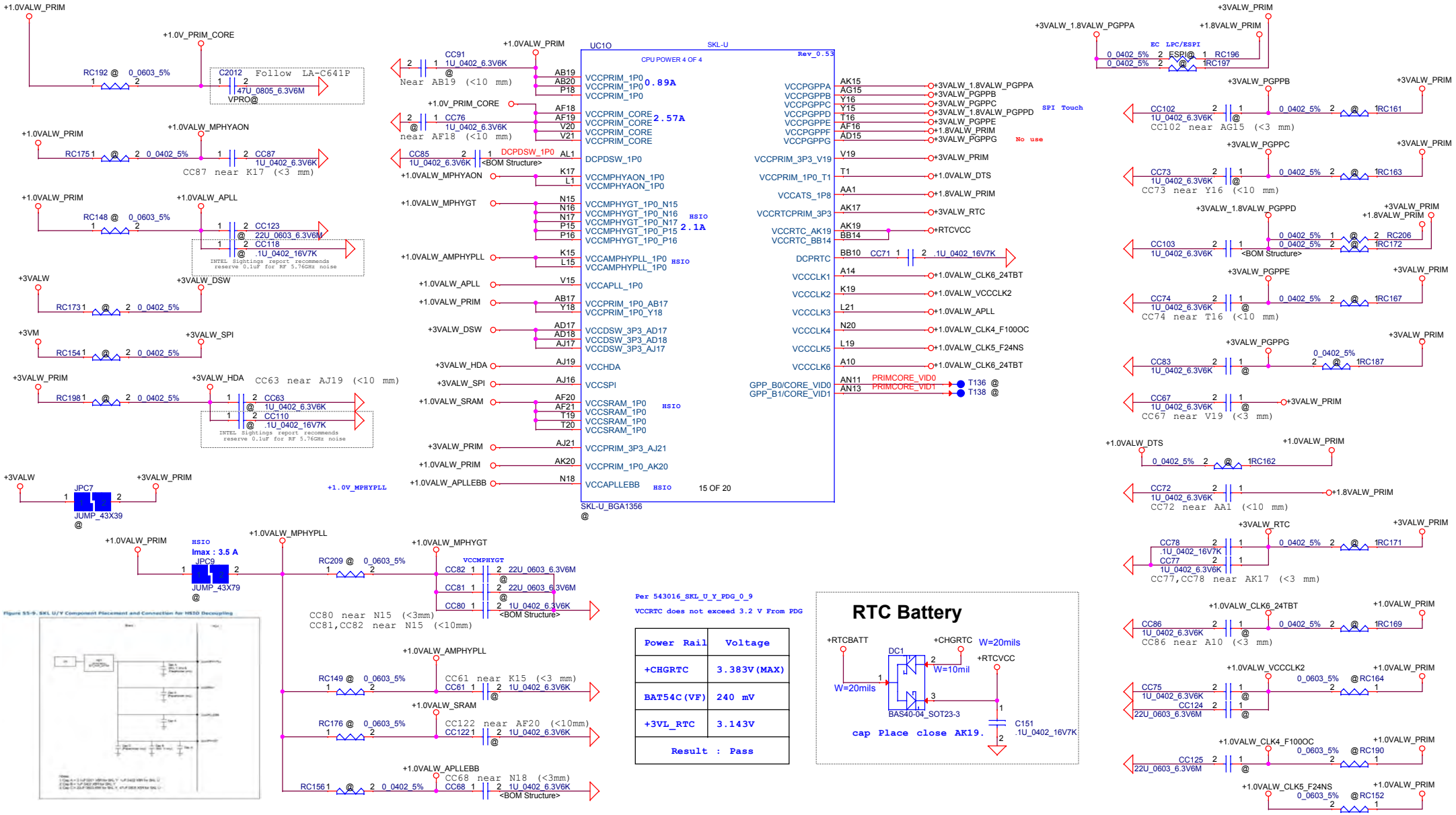
Title	Compal Electronics, Inc.		
	SKL-U(8/12)Power		
Size: Custom	Document Number: LA-D301P		Rev: 0.2
Date: Thursday, December 17, 2015	Sheet 13 of 63		



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Compal Electronics, Inc.

Title: SKL-U(9/12)Power

Size	Document Number	Rev
Custom	LA-D301P	0.2

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VCC 27A (U 15W Dual Core GT2)

#544924 Skylake EDS P.125

#544924 Skylake EDS P.125
VCCOPC 1V 2.8A
VCC_OPC_1P8 1.8V 50mA
VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

+VCC_CORE

UC1L SKL-U Rev_0.53
CPU POWER 1 OF 4

A30 VCC_A30
A34 VCC_A34
A39 VCC_A39
A44 VCC_A44
AK33 VCC_AK33
AK35 VCC_AK35
AK37 VCC_AK37
AK38 VCC_AK38
AK40 VCC_AK40
AL33 VCC_AL33
AL37 VCC_AL37
AL40 VCC_AL40
AM32 VCC_AM32
AM33 VCC_AM33
AM35 VCC_AM35
AM37 VCC_AM37
AM38 VCC_AM38
G30 VCC_G30

K32 RSVD_K32
AK32 RSVD_AK32

AB62 VCCOPC_AB62
P62 VCCOPC_P62
V62 VCCOPC_V62

H63 VCC_OPC_1P8_H63
G61 VCC_OPC_1P8_G61

AC63 VCCOPC_SENSE
AE63 VSSOPC_SENSE

AE62 VCCEOPIO
AG62 VCCEOPIO

AL63 VCCEOPIO_SENSE
AJ62 VSSEOPIO_SENSE

12 OF 20

SKL-U_BGA1356
@

T132 @ VCCOPC_SENSE
T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE
T139 @ VSSEOPIO_SENSE

+VCC_CORE

#544924 Skylake EDS P.120
VCC U(15W)-dual core GT2 27A(Typ)-33A(MAX)
0.55-1.15V

G32 VCC_G32
G33 VCC_G33
G35 VCC_G35
G37 VCC_G37
G38 VCC_G38
G40 VCC_G40
G42 VCC_G42
J30 VCC_J30
J33 VCC_J33
J37 VCC_J37
J40 VCC_J40
K33 VCC_K33
K35 VCC_K35
K37 VCC_K37
K38 VCC_K38
K40 VCC_K40
K42 VCC_K42
K43 VCC_K43

Trace Length < 25 mils

E32 VCC_SENSE → VCCSENSE <55>
E33 VSS_SENSE → VSSSENSE <55>

B63 VIDALERT# → SOC_SVID_ALERT#
A63 VIDSCK → SOC_SVID_CLK
D64 VIDSOUT → SOC_SVID_DAT
SOC_SVID_CLK <55>

G20 VCCSTG_G20 → +1.0VS_VCCSTG
+1.0VS(SUSP#)

Table 2-1. Package Sensing Recommendations

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100Ω	50Ω	<25 mils
VccGT_SENSE / VssGT_SENSE			
VccGTx_SENSE / VssGTx_SENSE			
VccSA_SENSE / VssSA_SENSE		NA	
VccIO_SENSE / VssIO_SENSE [1]			

Note: [1] Does not apply when rails are merged.

To minimize any stray noise pickup to the Vcc_SENSE/Vss_SENSE lines
- Sense traces should be referenced to a solid ground plane
- Avoid crossing over plane splits
- Maintain a 25-mil separation distance away from any other dynamic signals

VCCGT / VCCGTX(2+3e only) 40A(need confirm)

+VCC_GT

#544924 Skylake EDS P.121
VCCGT U(15W)-dual core GT2 40A(MAX)
0.55-1.15V

UC1M SKL-U Rev_0.53
CPU POWER 2 OF 4

A48 VCCGT
A53 VCCGT
A58 VCCGT
A62 VCCGT
A66 VCCGT
AA63 VCCGT
AA64 VCCGT
AA66 VCCGT
AA67 VCCGT
AA69 VCCGT
AA70 VCCGT
AA71 VCCGT
AC64 VCCGT
AC65 VCCGT
AC66 VCCGT
AC67 VCCGT
AC68 VCCGT
AC69 VCCGT
AC70 VCCGT
AC71 VCCGT
J43 VCCGT
J45 VCCGT
J46 VCCGT
J48 VCCGT
J50 VCCGT
J52 VCCGT
J53 VCCGT
J55 VCCGT
J56 VCCGT
J58 VCCGT
J60 VCCGT
K48 VCCGT
K50 VCCGT
K52 VCCGT
K53 VCCGT
K55 VCCGT
K56 VCCGT
K58 VCCGT
K60 VCCGT
L62 VCCGT
L63 VCCGT
L64 VCCGT
L65 VCCGT
L66 VCCGT
L67 VCCGT
L68 VCCGT
L69 VCCGT
L70 VCCGT
L71 VCCGT
M62 VCCGT
N63 VCCGT
N64 VCCGT
N66 VCCGT
N67 VCCGT
N69 VCCGT

J70 VCCGT_SENSE
J69 VSSGT_SENSE

N70 VCCGT
N71 VCCGT
R63 VCCGT
R64 VCCGT
R65 VCCGT
R66 VCCGT
R67 VCCGT
R68 VCCGT
R69 VCCGT
R70 VCCGT
R71 VCCGT
T62 VCCGT
U65 VCCGT
U68 VCCGT
U71 VCCGT
W63 VCCGT
W64 VCCGT
W65 VCCGT
W66 VCCGT
W67 VCCGT
W68 VCCGT
W69 VCCGT
W70 VCCGT
W71 VCCGT
Y62 VCCGT

VCCGTX_AK42 AK42
VCCGTX_AK43 AK43
VCCGTX_AK45 AK45
VCCGTX_AK46 AK46
VCCGTX_AK48 AK48
VCCGTX_AK50 AK50
VCCGTX_AK52 AK52
VCCGTX_AK53 AK53
VCCGTX_AK55 AK55
VCCGTX_AK56 AK56
VCCGTX_AK58 AK58
VCCGTX_AK60 AK60
VCCGTX_AK70 AK70
VCCGTX_AL43 AL43
VCCGTX_AL46 AL46
VCCGTX_AL50 AL50
VCCGTX_AL53 AL53
VCCGTX_AL56 AL56
VCCGTX_AL60 AL60
VCCGTX_AM48 AM48
VCCGTX_AM50 AM50
VCCGTX_AM52 AM52
VCCGTX_AM53 AM53
VCCGTX_AM56 AM56
VCCGTX_AM58 AM58
VCCGTX_AU58 AU58
VCCGTX_AU63 AU63
VCCGTX_BB57 BB57
VCCGTX_BB66 BB66

AK62 VCCGTX_SENSE
AL61 VSSGTX_SENSE

VCCGTX_SENSE
VSSGTX_SENSE

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SKL-U_BGA1356
@

For CPU2+3e SKU

T155 @
T219 @

<55> VCCGT_SENSE
<55> VSSGT_SENSE

Trace Length < 25 mils

SVID ALERT

+1.0V_VCCST
Place the PU resistors close to CPU
RC179 56_0402_5%
SOC_SVID_ALERT#
RC180 220_0402_5%
SOC_SVID_ALERT#_R <55> (To VR)

SVID DATA

+1.0V_VCCST
Place the PU resistors close to CPU
RC181 100_0402_1%
SOC_SVID_DAT
SOC_SVID_DAT <55> (To VR)

543016 PDG0.9 P.189 Need check

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	V_{CCST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDSCK							100	100	0	10	
VIDALERT#							56	Empty	220	0	

Processor Power Rails

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
V_{CCGT}	Processor Graphics Power Rails	SVID
V_{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V_{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V_{CCIO}	IO Power Rail	Fixed
V_{CCST}	Sustain Power Rail	Fixed
V_{CCPLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V_{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V_{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CCEOPIO}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: SKL-U(10/12)Power,SVID

Size	Document Number	Rev
Custom	LA-D301P	0.2

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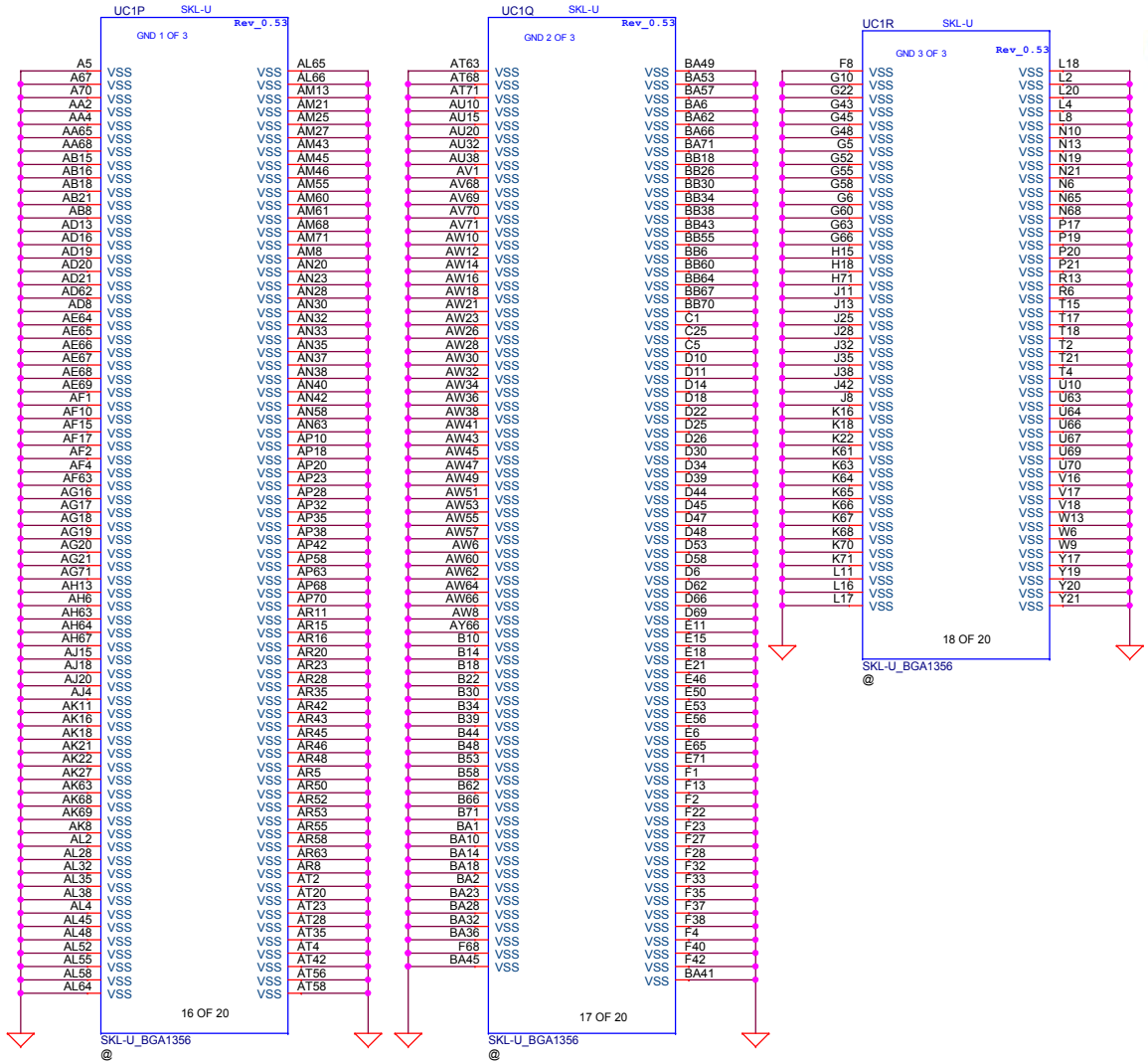
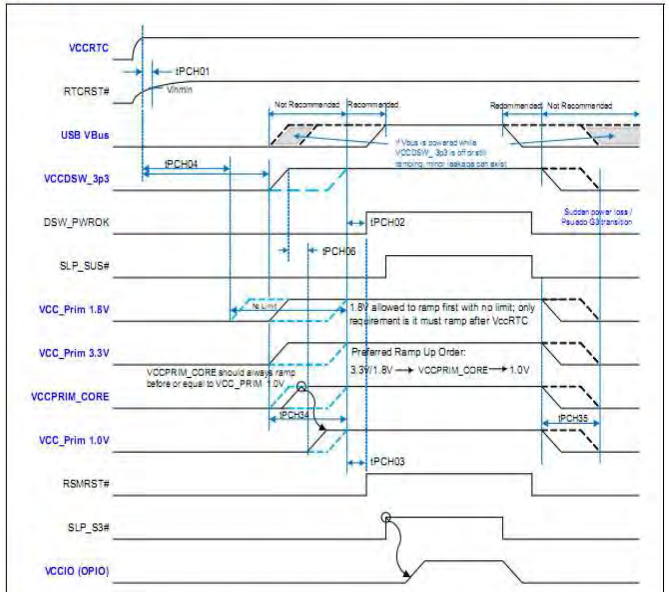


Figure 46-18.SKL-U/Y Rail-to-Rail Sequencing Requirement for Non-Deep Sx Configured System



Notes:

1. VCC_PRIM 1.8 V includes VCCPGPPF, VCCATS and may include VCCPGPPA, VCCPGPPB, VCCPGPPC, VCCPGPPD, VCCPGPPE, VCCPGPPG, VCCHDA and/or VCCSPI if the rails are 1.8 V.
2. VCC_PRIM 3.3 V includes VCCPRIM_3p3 and VCCRTCPRIM_3p3.
3. VCCPRIM_CORE is only applicable on SKL U/Y. For SKL H, the rail is merged with VCCPRIM_1p0.
4. VCC_PRIM 1.0 V may include the following rails: VCCPRIM_1p0, VCCSRAM_1p0, VCCMPHYAON_1p0, VCCMPHYGT_1p0, VCCMPHYPLL_1p0, VCCAPLL_1p0, VCCCLK1, VCCCLK2, VCCCLK3, VCCCLK4, VCCCLK5, VCCCLK6.

Security Classification	Compal Secret Data		
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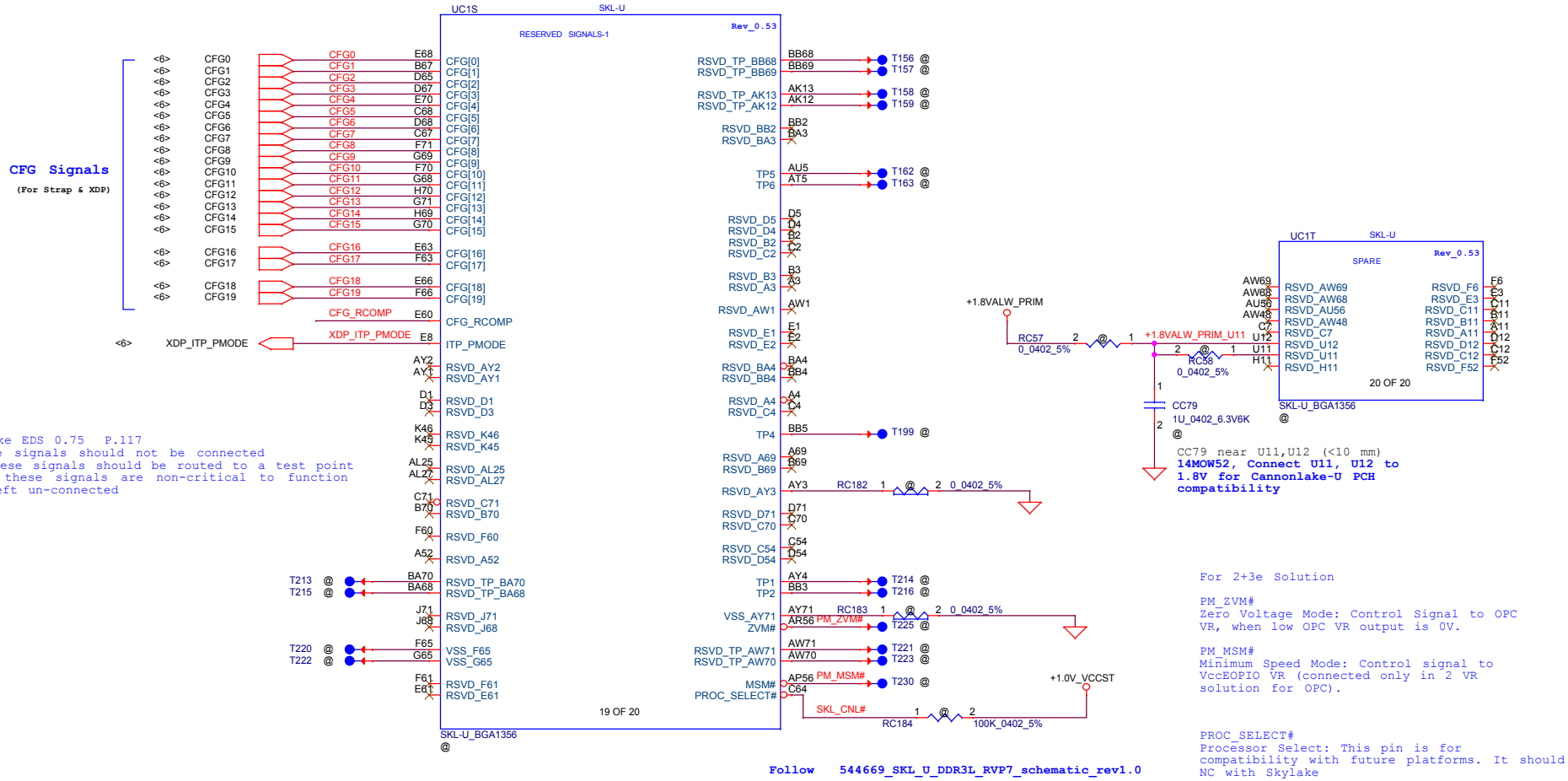
Compal Electronics, Inc.		
Title: SKL-U(11/12)GND		
Size: Custom	Document Number: LA-D301P	Rev: 0.2
Date: Thursday, December 17, 2015	Sheet 16 of 63	



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: SKL-U(12/12)RSVD

Size	Document Number	Rev
Custom	LA-D301P	0.2

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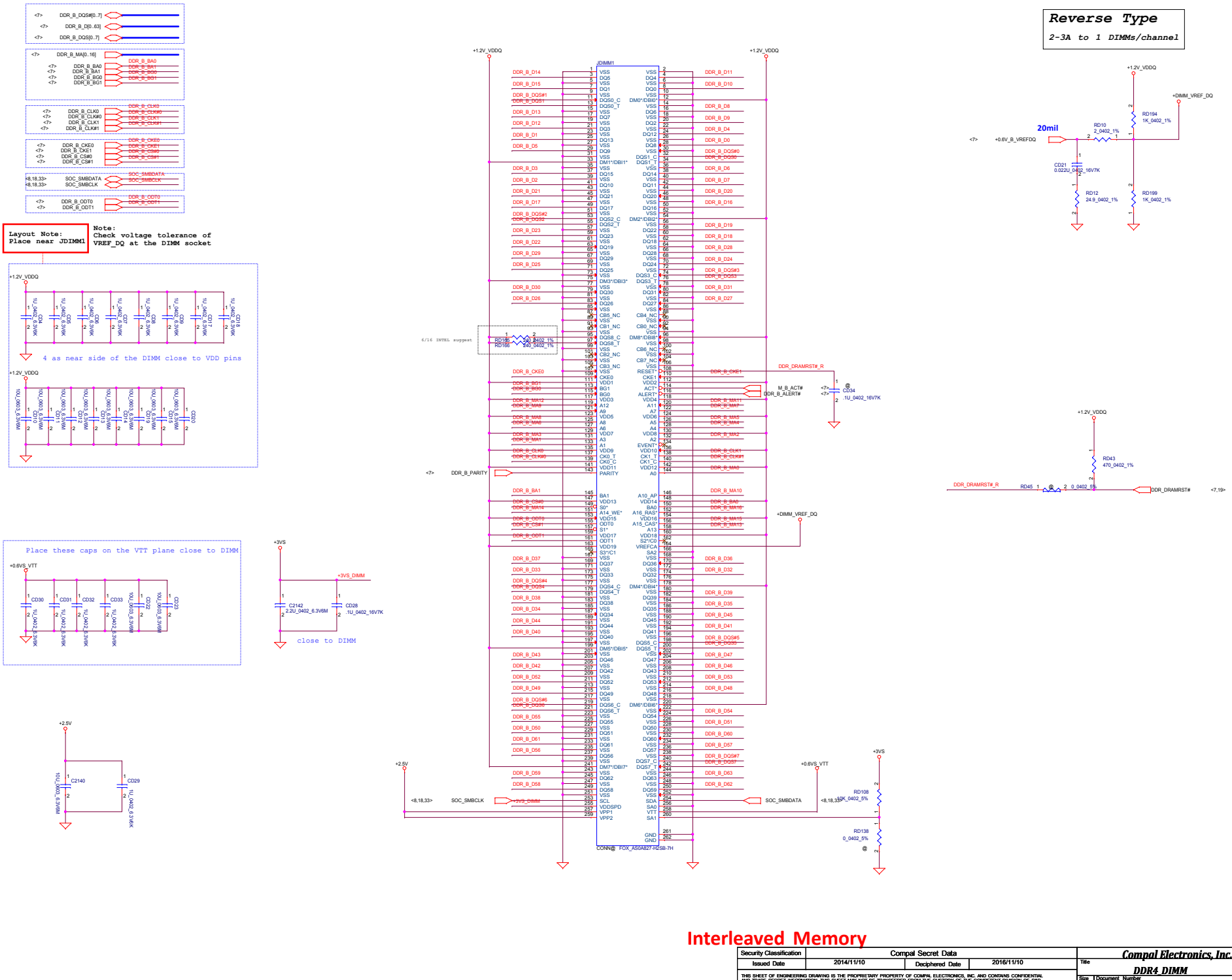
Reverse Type

2-3A to 1 DIMMs/channel



Interleaved Memory

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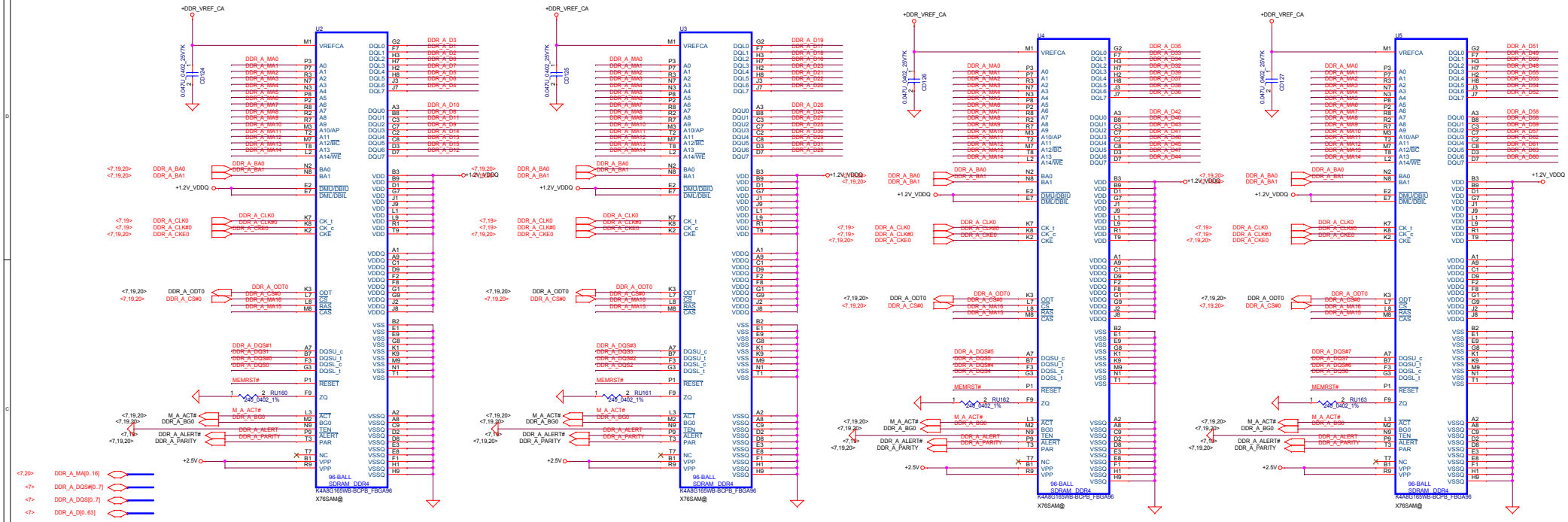
Compal Electronics, Inc.

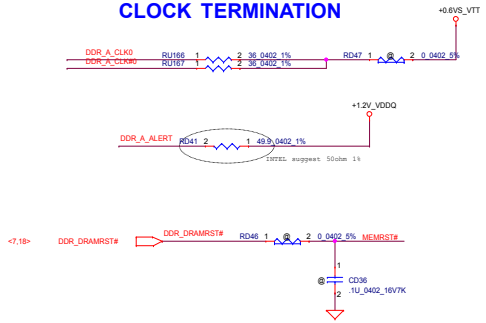
Title: DDR4 DIMM

Size: Custom | Document Number: LA-D301P | Rev: 0.2

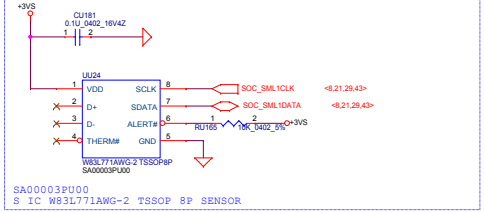
Date: Thursday, December 17, 2015 | Sheet 18 of 63

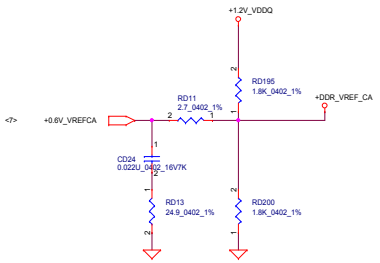


CLOCK TERMINATION



External DDR Thermal Sensor

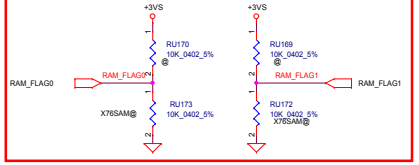




Data mapping

U2	DQ	U3	DQ	U4	DQ	U5	DQ
DQL0	D3	DQL0	D19	DQL0	D35	DQL0	D51
DQL1	D1	DQL1	D17	DQL1	D33	DQL1	D49
DQL2	D2	DQL2	D18	DQL2	D34	DQL2	D50
DQL3	D0	DQL3	D16	DQL3	D32	DQL3	D48
DQL4	D7	DQL4	D23	DQL4	D39	DQL4	D55
DQL5	D5	DQL5	D21	DQL5	D37	DQL5	D53
DQL6	D6	DQL6	D22	DQL6	D38	DQL6	D54
DQL7	D4	DQL7	D20	DQL7	D36	DQL7	D52
DQU0	D10	DQU0	D26	DQU0	D42	DQU0	D58
DQU1	D8	DQU1	D24	DQU1	D40	DQU1	D56
DQU2	D11	DQU2	D27	DQU2	D43	DQU2	D59
DQU3	D9	DQU3	D25	DQU3	D41	DQU3	D57
DQU4	D14	DQU4	D30	DQU4	D46	DQU4	D62
DQU5	D13	DQU5	D29	DQU5	D45	DQU5	D61
DQU6	D15	DQU6	D31	DQU6	D47	DQU6	D63
DQU7	D12	DQU7	D28	DQU7	D44	DQU7	D60

on board ram flag	FLAG1	FLAG0
SAM 4G SA00008Z000	0	0
	0	1
	1	0
	1	1



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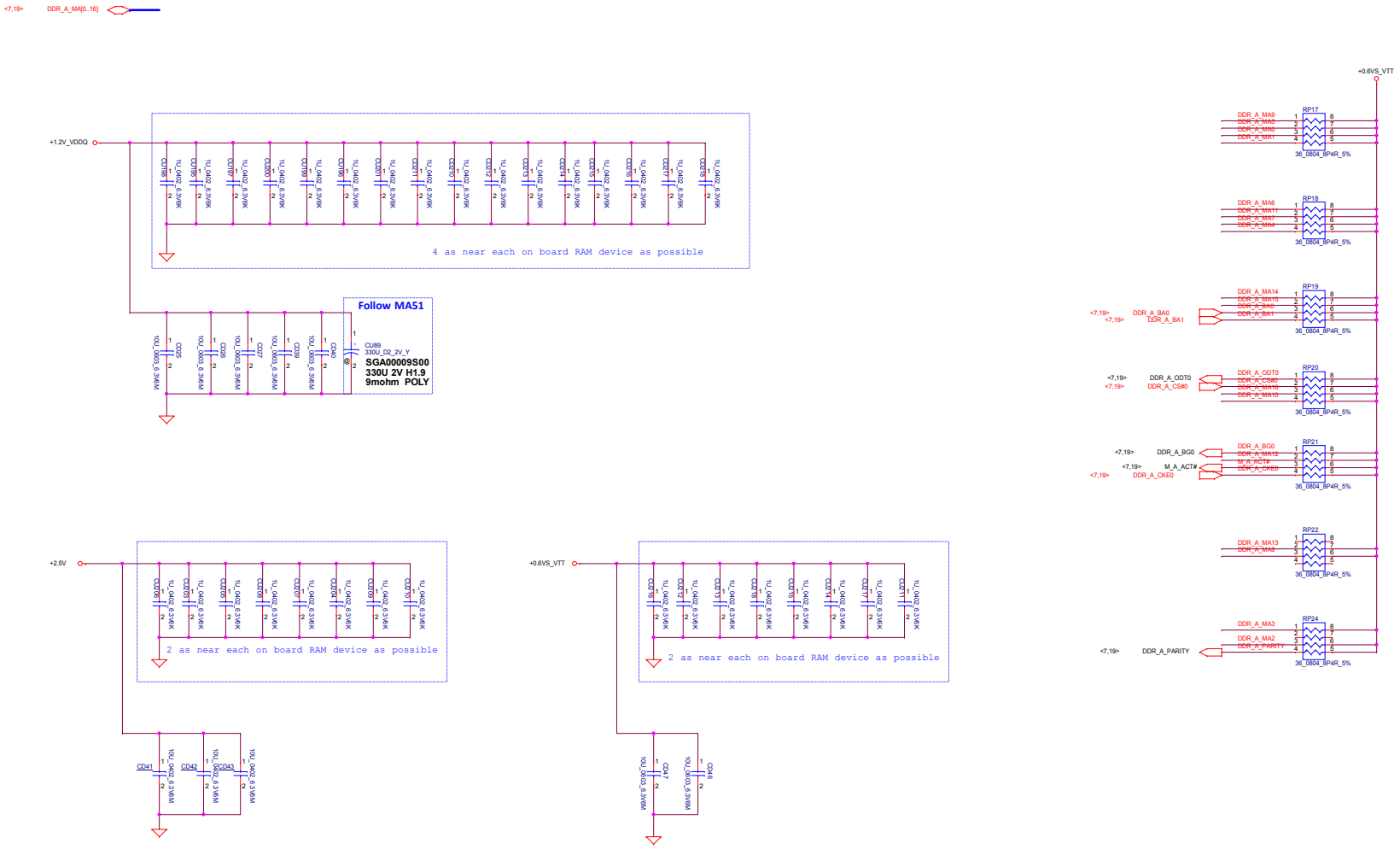
Title	DDR4 ON BOARD CHIPS		
Size: Custom	Document Number		Rev: 1A
Date: Thursday, December 17, 2015	Sheet 19 of 83		



Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

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Title	DDRIII ON BOARD CHIPS		
Size: Custom	Document Number		Rev: 1A
Date: Thursday, December 17, 2015	Sheet 20 of 63		

Note: NGC6 3VSDGPU_MAIN_EN is no function

GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		

GC6 2.0 function

SM010019400 3000ma 33ohm@100mhz DCR 0.05

38mA

PLL_VDD
0.1Ux1, 22Ux1
30ohm(ESR0.05)x1

SM01000AG00 2A 300ohm@100mhz DCR 0.1

17mA

SP_PLLVDD+VID_PLLVDD
0.1Ux2, 10Ux1,47Ux1
300ohm(ESR0.2)x1

Crystals must have a max ESR of 80 ohm

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Compal Electronics, Inc.

Title: N16X PEG 1/9

Size: Custom | Document Number: LA-D301P | Rev: 0.2

Date: Thursday, December 17, 2015 | Sheet 21 of 63

VRAM Interface

UGPU1
N16S-GT
SGT@
SA000087F10

UGPU1
N16V-GM
VGM@
SA000088R20

<26> MDA[15..0] MDA[15..0]
<26> MDA[31..16] MDA[31..16]
<27> MDA[47..32] MDA[47..32]
<27> MDA[63..48] MDA[63..48]

UGPU1B
Part 2 of 6
MEMORY INTERFACE A
GM108-ES-S-A1_FCBGA595
@

MDA	FBA_D	MDA	FBA_D
MDA0	E18	MDA32	R22
MDA1	F18	MDA33	R24
MDA2	E16	MDA34	T22
MDA3	F17	MDA35	R23
MDA4	D20	MDA36	N25
MDA5	D21	MDA37	N26
MDA6	F20	MDA38	N23
MDA7	E21	MDA39	N24
MDA8	E15	MDA40	V23
MDA9	D15	MDA41	V22
MDA10	F15	MDA42	T23
MDA11	F13	MDA43	U22
MDA12	C13	MDA44	Y24
MDA13	B13	MDA45	AA24
MDA14	E13	MDA46	Y22
MDA15	D13	MDA47	AA23
MDA16	B15	MDA48	AD27
MDA17	C16	MDA49	AB25
MDA18	A13	MDA50	AD26
MDA19	A15	MDA51	AC25
MDA20	B18	MDA52	AA27
MDA21	A18	MDA53	AA26
MDA22	A19	MDA54	W26
MDA23	C19	MDA55	Y25
MDA24	B24	MDA56	R26
MDA25	C23	MDA57	T25
MDA26	A25	MDA58	N27
MDA27	A24	MDA59	R27
MDA28	A21	MDA60	V26
MDA29	B21	MDA61	V27
MDA30	C20	MDA62	W27
MDA31	C21	MDA63	W25

FBA_CMD	CMDA	FBA_CMD	CMDA
FBA_CMD0	CMDA0	FBA_CMD16	CMDA16
FBA_CMD1	CMDA1	FBA_CMD17	CMDA17
FBA_CMD2	CMDA2	FBA_CMD18	CMDA18
FBA_CMD3	CMDA3	FBA_CMD19	CMDA19
FBA_CMD4	CMDA4	FBA_CMD20	CMDA20
FBA_CMD5	CMDA5	FBA_CMD21	CMDA21
FBA_CMD6	CMDA6	FBA_CMD22	CMDA22
FBA_CMD7	CMDA7	FBA_CMD23	CMDA23
FBA_CMD8	CMDA8	FBA_CMD24	CMDA24
FBA_CMD9	CMDA9	FBA_CMD25	CMDA25
FBA_CMD10	CMDA10	FBA_CMD26	CMDA26
FBA_CMD11	CMDA11	FBA_CMD27	CMDA27
FBA_CMD12	CMDA12	FBA_CMD28	CMDA28
FBA_CMD13	CMDA13	FBA_CMD29	CMDA29
FBA_CMD14	CMDA14	FBA_CMD30	CMDA30
FBA_CMD15	CMDA15	FBA_CMD31	CMDA31

CMDA[31..0] <26,27>

PVT modify 01/13
DQSA, DQSA# reverse

FBA_DQM0	D19	DQMA0	DQMA[3..0] <26>
FBA_DQM1	D14	DQMA1	
FBA_DQM2	C17	DQMA2	
FBA_DQM3	C22	DQMA3	
FBA_DQM4	P24	DQMA4	DQMA[7..4] <27>
FBA_DQM5	W24	DQMA5	
FBA_DQM6	AA25	DQMA6	
FBA_DQM7	U25	DQMA7	
FBA_DQS_RN0	F19	DQSA#0	DQSA#[3..0] <26>
FBA_DQS_RN1	C14	DQSA#1	
FBA_DQS_RN2	A16	DQSA#2	
FBA_DQS_RN3	A22	DQSA#3	DQSA#[7..4] <27>
FBA_DQS_RN4	P25	DQSA#4	
FBA_DQS_RN5	W22	DQSA#5	
FBA_DQS_RN6	AB27	DQSA#6	
FBA_DQS_RN7	T27	DQSA#7	
FBA_DQS_WP0	E19	DQSA0	DQSA[3..0] <26>
FBA_DQS_WP1	C15	DQSA1	
FBA_DQS_WP2	B16	DQSA2	
FBA_DQS_WP3	B22	DQSA3	DQSA[7..4] <27>
FBA_DQS_WP4	R25	DQSA4	
FBA_DQS_WP5	W23	DQSA5	
FBA_DQS_WP6	AB26	DQSA6	
FBA_DQS_WP7	T26	DQSA7	

FBA_CLK0	D24	CLKA0	<26>
FBA_CLK0_N	D25	CLKA0#	<26>
FBA_CLK1	N22	CLKA1	<27>
FBA_CLK1_N	M22	CLKA1#	<27>

FBA_WCK01	D18	FBA_WCK23	T24
FBA_WCK01_N	C18	FBA_WCK23_N	U24
FBA_WCK23	D17	FBA_WCK45	V24
FBA_WCK23_N	D16	FBA_WCK45_N	V25
FBA_WCK45	T24	FBA_WCK67	
FBA_WCK45_N	U24	FBA_WCK67_N	

FB_PLLAVDD_1	F16	FB_VREF_PROBE	D23
FB_PLLAVDD_2	P22	FB_DLLAVDD	H22
FB_CLAMP	F3	FBA_CMD34	F22
FBA_CMD35	J22		

Table 6-8. Memory ODTx, CKEx, and RST Termination

DDR3 Command Bit	Default Pull-Down
ODTx	10 kΩ
CKEx	10 kΩ
RST	10 kΩ
CS*	No Termination

ODT_L	CMDA2	R2093 1	VGA@	2	10K_0402_5%
CLK_L	CMDA3	R2094 1	VGA@	2	10K_0402_5%
RST	CMDA5	R2095 1	VGA@	2	10K_0402_5%
ODT_H	CMDA18	R2098 1	VGA@	2	10K_0402_5%
CLK_H	CMDA19	R2099 1	VGA@	2	10K_0402_5%

NV 15x DG-06803-V03

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

SM010019400 3000ma 33ohm@100mhz DCR 0.05

+1.05VSDGPU
VGA@ 2 1 L2002 CHILISIN PBY160808T-330Y-N
15+55mA
+FB_PLLAVDD
C2008 VGA@ 22U_0603_6.3V6M
C2011 VGA@ 1U_0402_16V7
C2010 VGA@ 1U_0402_16V7
C2009 VGA@ 1U_0402_16V7
Place Near GPU Place Under F16 P22 H22

T97 @ D23
1 VGA@ 2 FB_CLAMP
10K_0402_5% R2028

change to 1.35VSDGPU
+1.5VSDGPU
60.4_0402_1% 1 @ 2 R2020 FBA_CMD34
60.4_0402_1% 1 @ 2 R2022 FBA_CMD35

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: N16X VRAM 2/9

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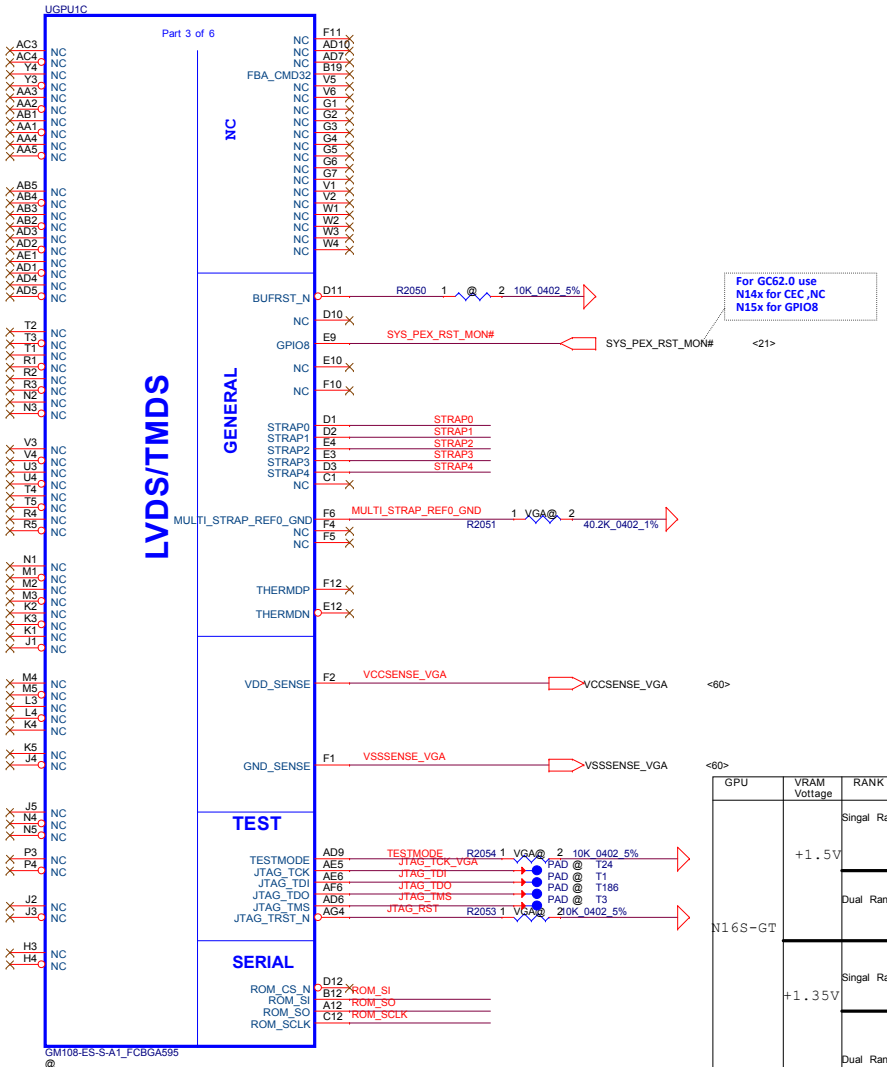
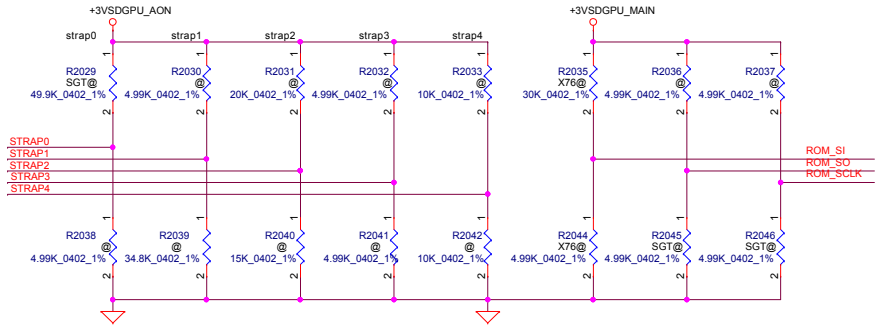


MULTI LEVEL STRAPS



N16VGM Option Component

```
STRAP0  --->  R2029 2 VGM@1 45.3K_0402_1%  SD034453280
STRAP1  --->  R2039 2 VGM@1 45.3K_0402_1%  SD034453280
STRAP2  --->  R2031 2 VGM@1 10K_0402_1%    SD034100280
STRAP3  --->  R2041 2 VGM@1 4.99K_0402_1%  SD034499180
STRAP4  --->  R2042 2 VGM@1 45.3K_0402_1%  SD034453280
ROM_SO  --->  R2036 2 VGM@1 4.99K_0402_1%  SD034499180
ROM_SCLK--->  R2037 2 VGM@1 4.99K_0402_1%  SD034499180

ROM_SI pull down 15kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x2
ROM_SI pull down 10kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x1
ROM_SI pull down 25kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x4
ROM_SI pull up 35kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0xE
ROM_SI pull up 30kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0xD
ROM_SI pull down 30kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x5
ROM_SI pull up 25kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0xC
```

N16SGT Option Component

```
ROM_SI pull down 4.99kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x0
ROM_SI pull down 10kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x1
ROM_SI pull down 15kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x2
ROM_SI pull down 20kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x3
ROM_SI pull down 25kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x4
ROM_SI pull down 30kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x5
```

For N16S-GT Multi strap table

Decive ID : 0x1347

GPU	VRAM Vottage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16S-GT	+1.5V	Singal Rank	X76629BOL07	1GHz	256Mx16x4 2GB	0x5 (SA00008DN10) Hynix H5TC4G63CFR-N0C	PU 50K	NC	NC	NC	NC	PD 30K	PD 4.99K	PD 4.99K
			X76629BOL08			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76629BOL09			0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		
		Dual Rank	X76629BOL10	1GHz	256Mx16x8 4GB	0xC (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 24.9K		
			X76629BOL11			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76629BOL12			0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		
	+1.35V	Singal Rank		900MHz	256Mx16x4 2GB	0x2 (SA00008DN10) Hynix H5TC4G63CFR-N0C						PD 15K		
						0x4 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 24.9K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		
		Dual Rank		900MHz	256Mx16x8 4GB	0xE (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 35K		
						0x4 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 24.9K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		

For N16V-GM Multi strap table

Decive ID : 0x1299

GPU	VRAM Vottage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16V-GM	+1.5V	Singal Rank	X76629BOL01	1GHz	256Mx16x4 2GB	0x9 (SA00008DN10) Hynix H5TC4G63CFR-N0C	PU 45.3K	PD45.3K	PU 10K	PD 4.99K	PD 45.3K	PU 10K	PU 4.99K	PU 4.99K
			X76629BOL02			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76629BOL03			0x4 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 24.9K		
	+1.35V	Singal Rank		900MHz	256Mx16x4 2GB	0x0 (SA00008DN10) Hynix H5TC4G63CFR-N0C						PD 5K		
						0xD (SA000077K20) Micron MT41J256M16HA-093G:E						PU 30K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		
		Dual Rank	X76629BOL04	900MHz	256Mx16x8 4GB	0xA (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 15K		
			X76629BOL05			0xD (SA000077K20) Micron MT41J256M16HA-093G:E						PU 30K		
			X76629BOL06			0xC (SA000076P20) Samsung K4W4G1646D-BC1A						PU 24.9K		

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Title: **N16X STRAPS 3/9**

Size	Document Number	Rev
Custom	LA-D301P	0.2

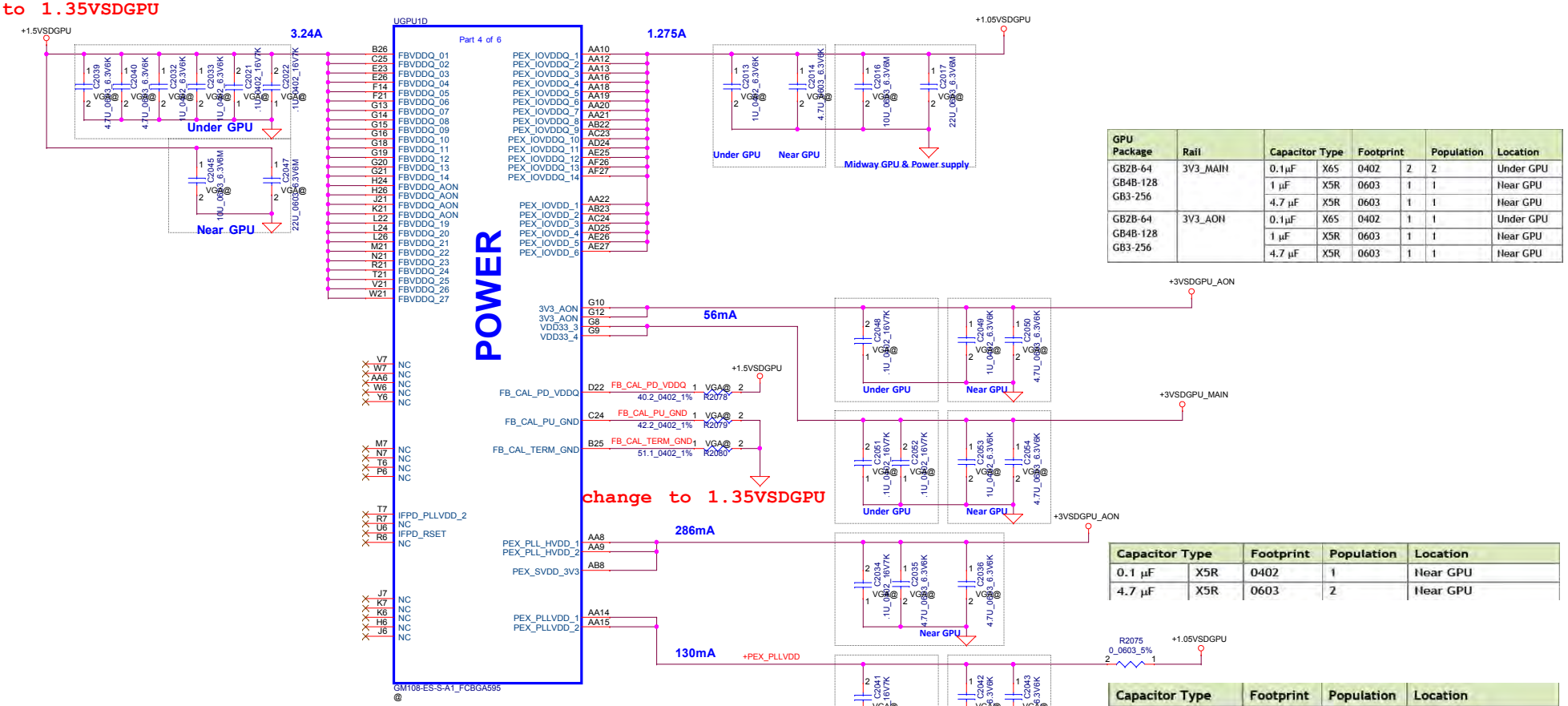
Date: Thursday, December 17, 2015 | Sheet 23 of 63

NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64 DDR3	0.1μF	X7R	0402	2	2	Under GPU
	1 μF	X7R	0603	2	2	Under GPU
	4.7 μF	X6S	0603	2	2	Under GPU
	10 μF	X5R	0805	1	1	Near GPU
	22 μF	X5R	0805	1	1	Near GPU

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 μF	X6S	0402	1	Under GPU
	4.7 μF	X6S	0603	1	Near GPU
	10 μF	X5R	0805	1	Midway between GPU and Power Supply
	22 μF	X5R	0805	1	Midway between GPU and Power Supply

change to 1.35VSDGPU



GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1μF	X6S	0402	2	2	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1μF	X6S	0402	1	1	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X5R	0402	1	Near GPU
4.7 μF	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X6S	0402	1	Under GPU
1.0 μF	X5R	0603	1	Near GPU
4.7 μF	X5R	0805	1	Near GPU

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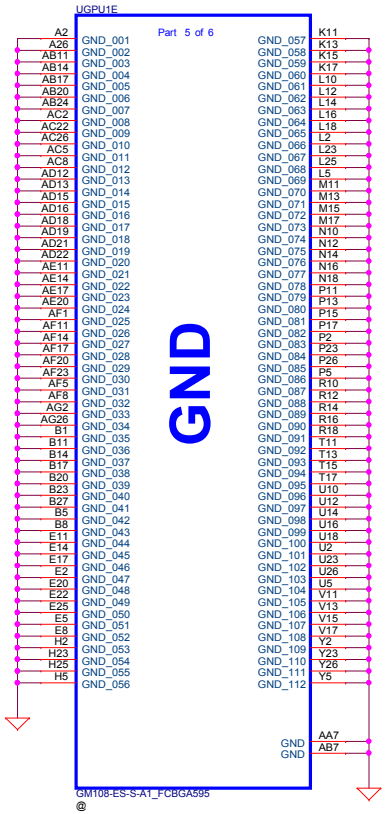

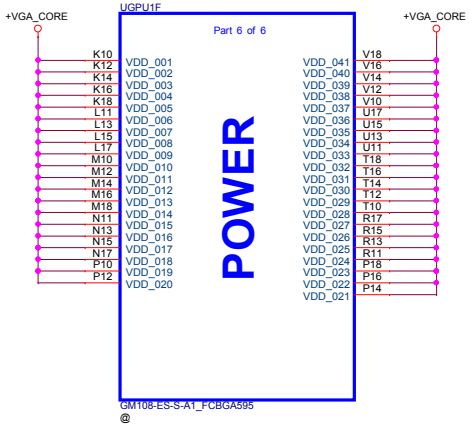

NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core — (A)	FB Total 1.5/1.35V (A)	1.05V Total 1.05V (A)
~~N15S-GM~~	~~DDR3/L~~	~~48.11~~	~~4.23~~	~~0.91~~
N15S-GT	DDR3/L	60.07	4.26	0.91

DA-06925-V05

Table 6. EDP-Peak at T_J = 102°C

Power Supply Rail	N15V-GM-S DDR3/L
(V)	(A)
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

DA07075-V01

Table 7. EDP-Peak at T_J = 102°C

Power Supply Rail	N15V-GL DDR3
(V)	(A)
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

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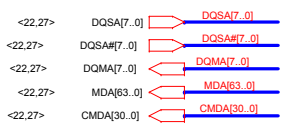
VRAM DDR3 chips

LOW BIT

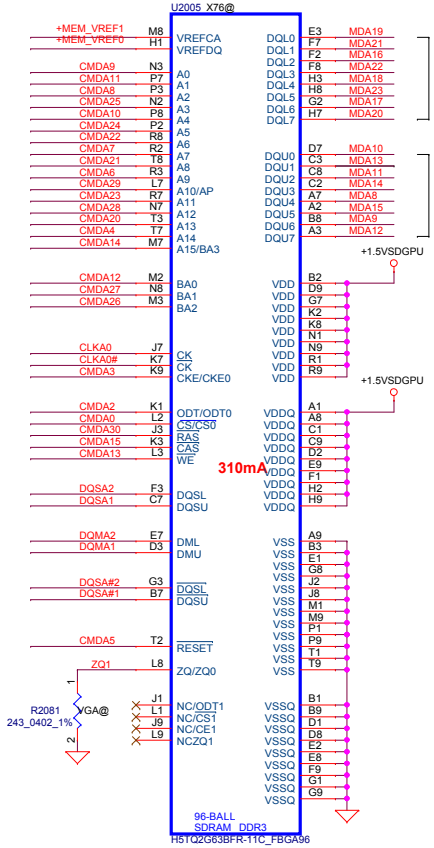


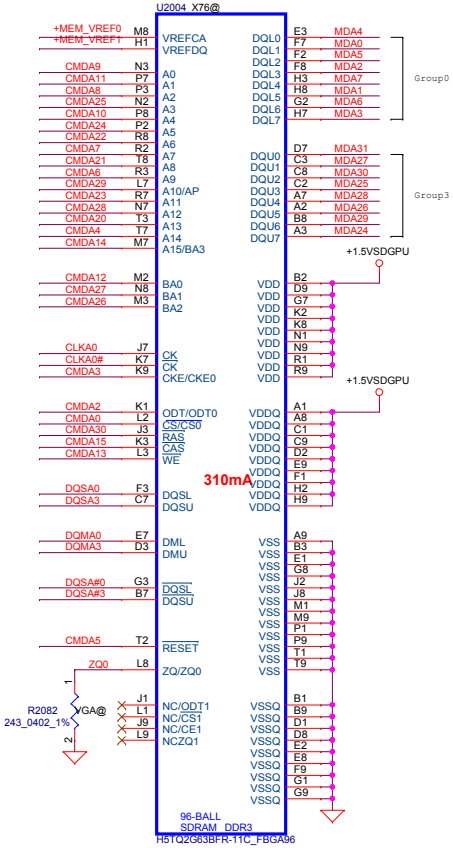
ZZZ

ALT. GROUP PARTS GT2G HYN 256M16 A4WAD
X76@VHY
X76614BOL54

ZZZ

ALT. GROUP PARTS GT2G SAM-N 256M16 A4WAD
X76@VSAM
X76614BOL58



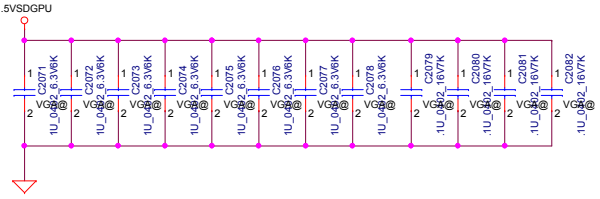


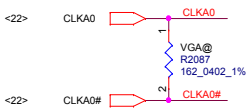
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

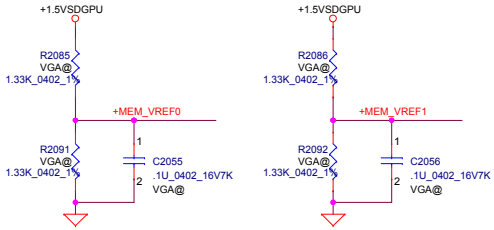
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM







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Title: N16X Upper Rank0 6/9

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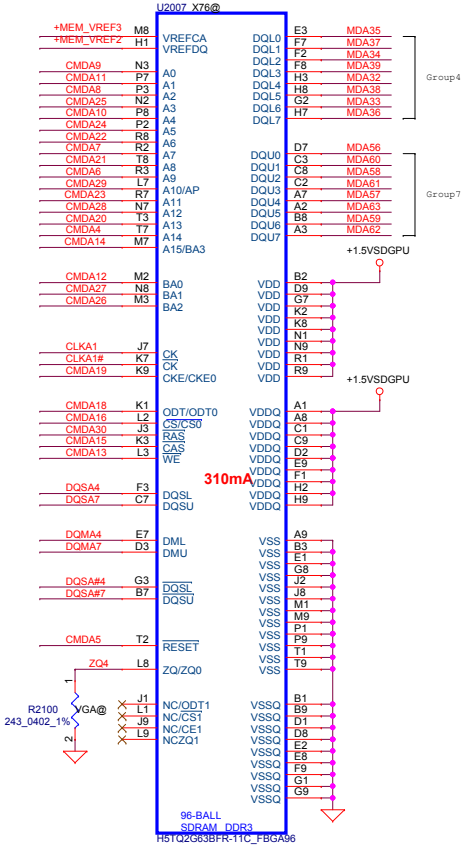
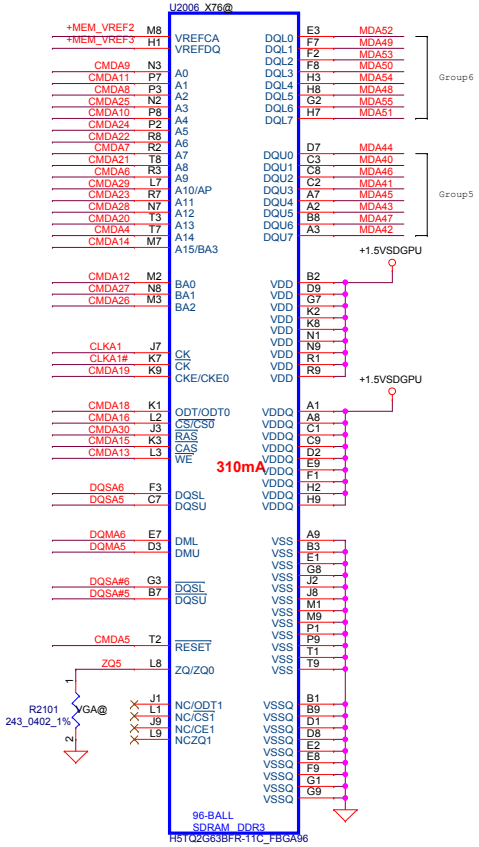
VRAM DDR3 chips

<22,26> DQSA[7..0] DQSA[7..0]
<22,26> DQSA#[7..0] DQSA#[7..0]
<22,26> DQMA[7..0] DQMA[7..0]
<22,26> MDA[63..0] MDA[63..0]
<22,26> CMDA[30..0] CMDA[30..0]

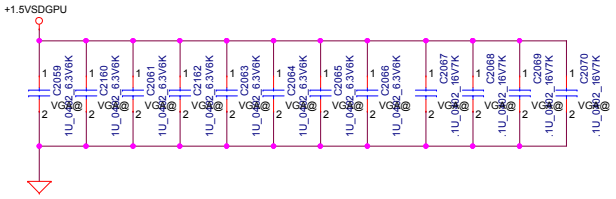
HIGH BIT

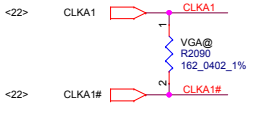


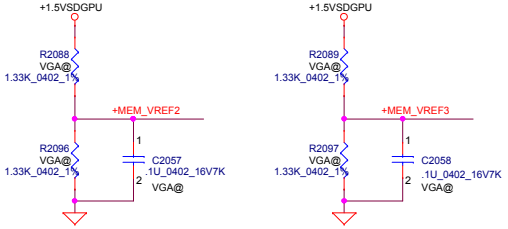


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination







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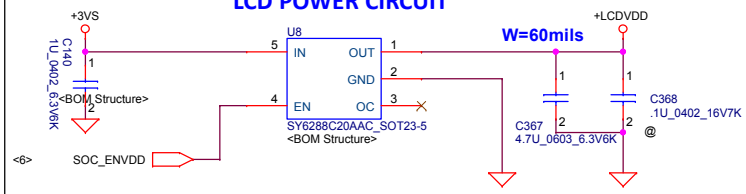
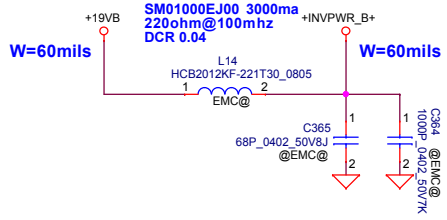
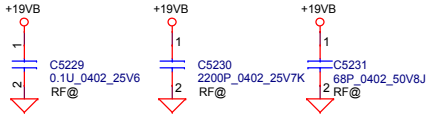
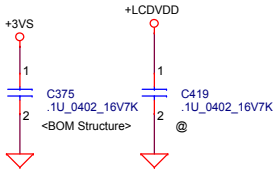
LCD POWER CIRCUIT

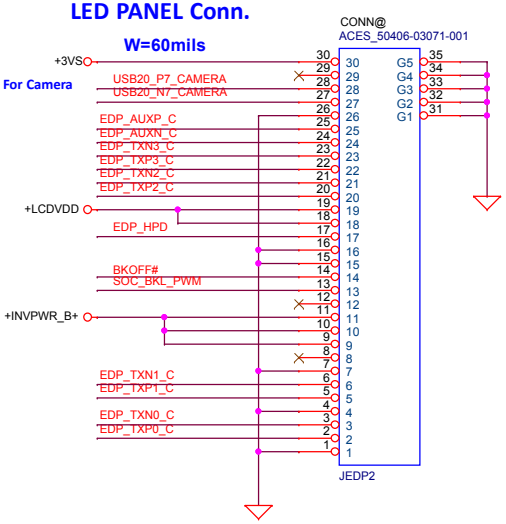


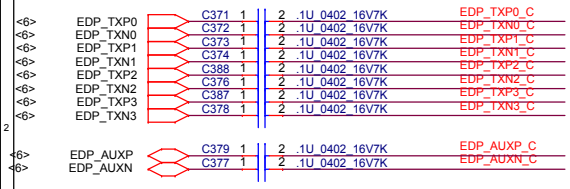


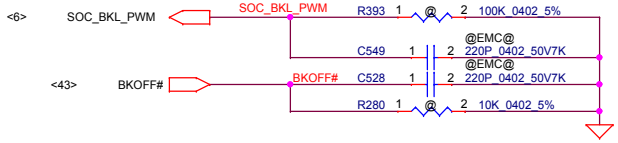


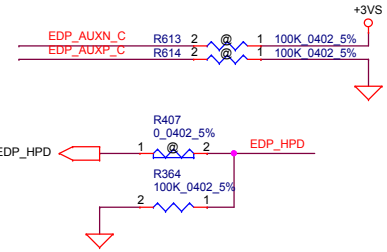


LED PANEL Conn.









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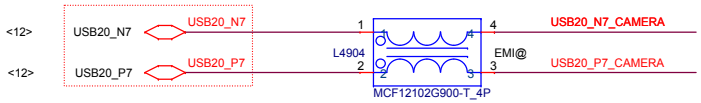
Camera



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Size	Document Number	Rev
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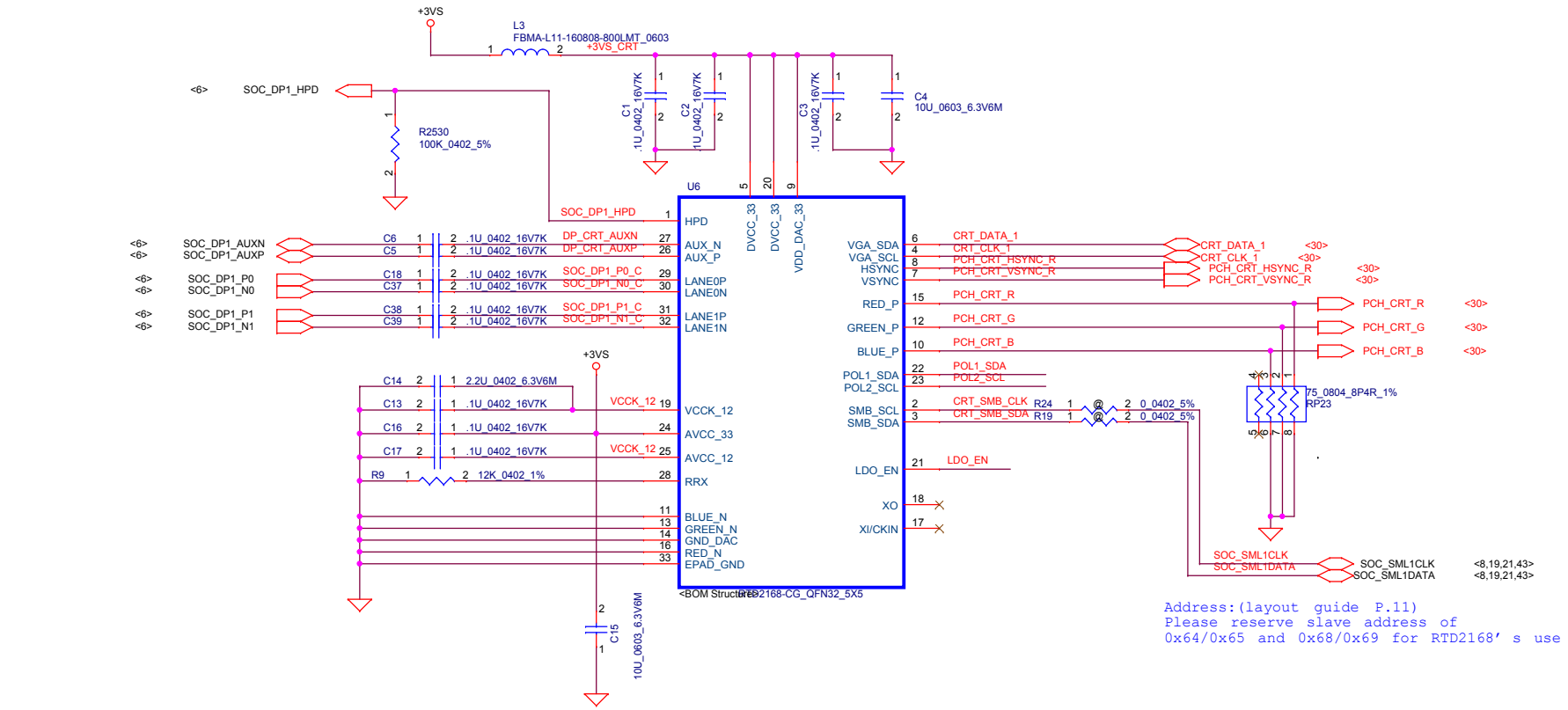
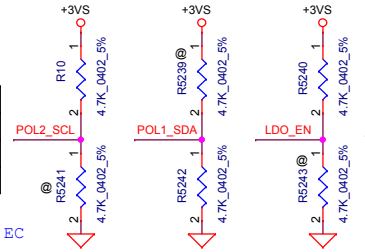


		POL_SDA	
		0	1
POL_SCL	0	X	EP
	1	*ROM	EEPROM

ROM: Internal ROM
EP: Programmed external EC
EEPROM: External ROM



LDO_EN:
*1: Internal 1.2V
0: External 1.2V

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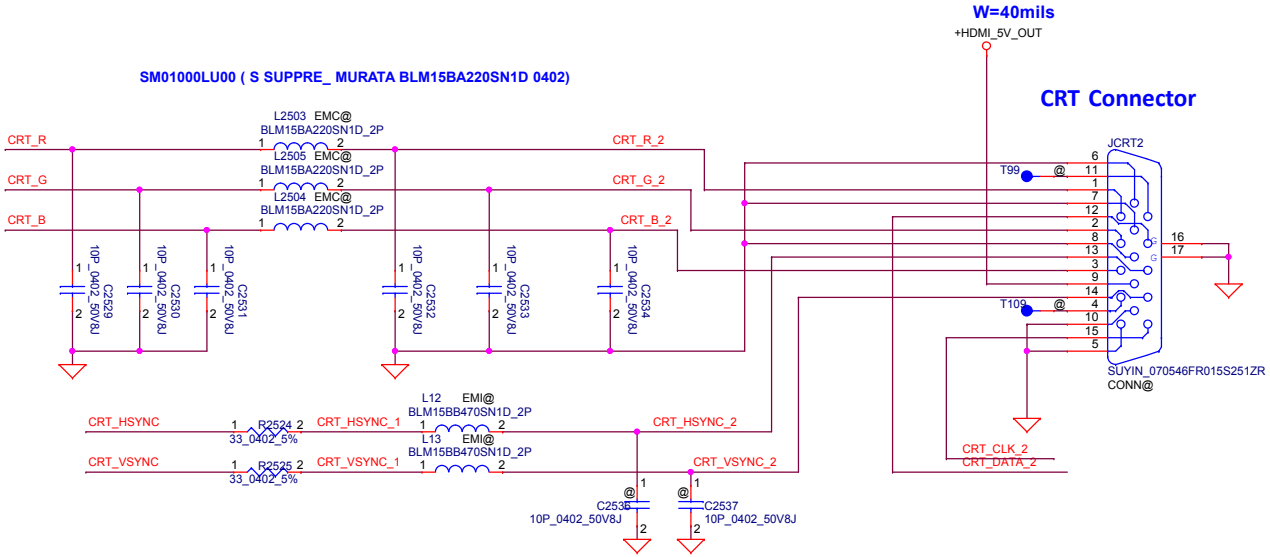
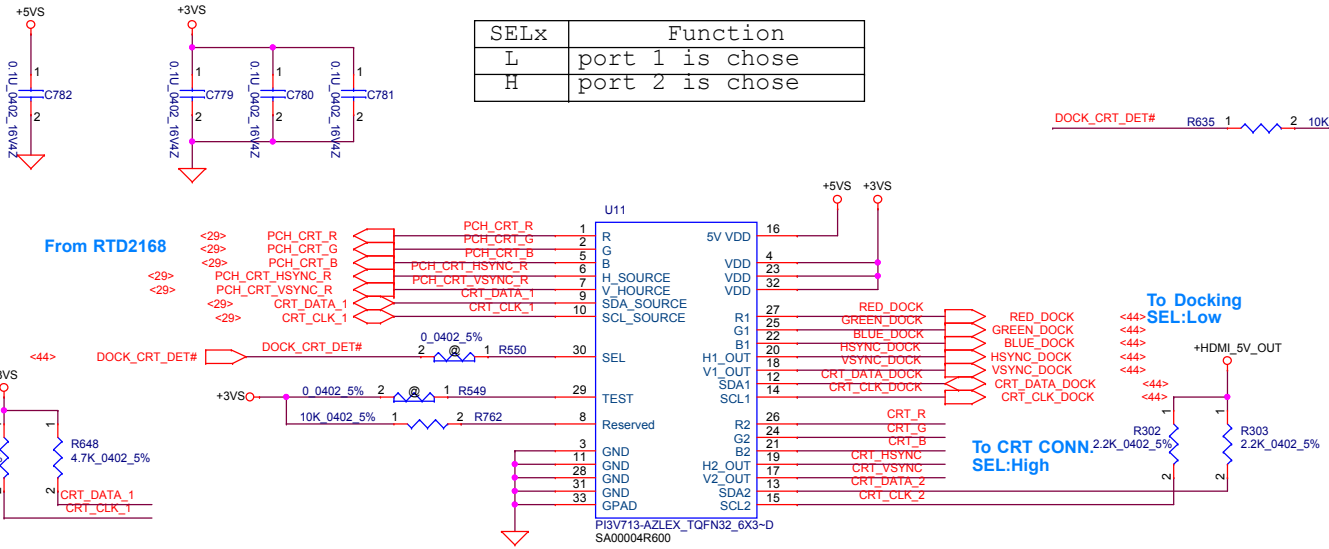
CRT conn.





SELx	Function
L	port 1 is chose
H	port 2 is chose

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Issued Date	2014/02/14	Deciphered Date	2015/02/14

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Compal Electronics, Inc.			
Title: CRT CONN.			
Size: Custom	Document Number: LA-D301P		Rev: 1A
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R183 1 2 4.7K_0201_5% DP_CFG0

Chip operational mode configuration;
Internal pull down at ~150K?, 3.3V I/O.

L: Control switching mode (default)
H: Automatic switching mode

R198 1 2 4.7K_0201_5% PI0

Automatic EQ disable;
Internal pull down at ~150K?, 3.3V IO

L: Automatic EQ enable (default)
H: Automatic EQ disable

R199 1 2 4.7K_0201_5% PI1
R203 1 2 4.7K_0201_5%

Auto test enable;
Internal pull down at ~150K?, 3.3V I/O.
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

R185 1 2 4.7K_0201_5% PC10
R186 1 2 4.7K_0201_5%
R187 1 2 4.7K_0201_5% PC20
R188 1 2 4.7K_0201_5%

AUX interception disable for Port y (y=1,2)
Internal pull down at ~150K?, 3.3V I/O.

L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mv and 0dB
M: AUX interception disable, driver output with fixed 400mv and 0dB

R189 1 2 4.7K_0201_5% PC11
R190 1 2 4.7K_0201_5%
R191 1 2 4.7K_0201_5% PC21
R194 1 2 4.7K_0201_5%

Output swing adjusment for Port y (y=1,2).
Internal pull down at ~150K?, 3.3V I/O.

L:default
H: +20%
M: -16.7%

C159 0.1U_0201_10V6K
C160 0.1U_0201_10V6K
C35 0.01U_0402_16V7K
C36 0.01U_0402_16V7K

R196 1 2 4.7K_0201_5% PEQ
R197 1 2 4.7K_0201_5%

Programmable input equalization levels; Internal pull down at ~150K?, 3.3V I/O.

L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

DP_MUX_SEL pin

Port switching control or priority configuration;
Internal pull down at ~150K?, 3.3V I/O.
L: Port1 is selected or with higher priority (default)
H: Port2 is selected or with higher priority

U23
PS8338BQFN60GTR-A0_QFN60_5X9

VDD33 (5, 21, 30, 51, 57)
GND (11, 19, 52, 61)
PAD(GND)

IN_D0p / IN_D0n — DPB_P0 / DPB_N0
IN_D1p / IN_D1n — DPB_P1 / DPB_N1
IN_D2p / IN_D2n — DPB_P2 / DPB_N2
IN_D3p / IN_D3n — DPB_P3 / DPB_N3
IN_CA_DET
IN_HPD
I2C_CTL_EN
PI1/SCL_CTL
PI0/SDA_CTL
IN_DDC_SCL — DDI2_CTRL_CK
IN_DDC_SDA — DDI2_CTRL_DATA
IN_AUXp — DPB_AUXP
IN_AUXn — DPB_AUXN
CFG0 — DP_CFG0
CFG1
PC10
PC11
PC20
PC21

OUT1_D0p / OUT1_D0n — DP_DOCK_P0 / DP_DOCK_N0
OUT1_D1p / OUT1_D1n — DP_DOCK_P1 / DP_DOCK_N1
OUT1_D2p / OUT1_D2n — DP_DOCK_P2 / DP_DOCK_N2
OUT1_D3p / OUT1_D3n — DP_DOCK_P3 / DP_DOCK_N3
to Docking

OUT2_D0p / OUT2_D0n — TBT_DP1_P0 / TBT_DP1_N0
OUT2_D1p / OUT2_D1n — TBT_DP1_P1 / TBT_DP1_N1
OUT2_D2p / OUT2_D2n — TBT_DP1_P2 / TBT_DP1_N2
OUT2_D3p / OUT2_D3n — TBT_DP1_P3 / TBT_DP1_N3
to Alpine Ridge

OUT1_AUXp_SCL / OUT1_AUXn_SDA — DP_DOCK_AUXP / DP_DOCK_AUXN
OUT2_AUXp_SCL / OUT2_AUXn_SDA — TBT_DP1_AUXP / TBT_DP1_AUXN
OUT1_CA_DET / OUT1_HPD — DP_DOCK_CAD / DP_HPD_DOCK
OUT2_CA_DET — TBT_DP1_HPD
SW
PEQ
PD
CEXT — C57 2.2U_0402_6.3V6M
REXT — R1101 4.99K_0402_0.5%

R5236 2.2K_0402_5% DDI2_CTRL_CK
R5237 2.2K_0402_5% DDI2_CTRL_DATA

<6> CPU_HDMI_HPD
R5238 100K_0402_5%
R5234 4.7K_0402_5%
R5235 0_0402_5%
DP_DOCK_SEL <44>

TBT_DP1_AUXN / DP_DOCK_AUXN — R126 100K_0201_5% / R5244 100K_0201_5%
TBT_DP1_AUXP / DP_DOCK_AUXP — R129 100K_0201_5% / R137 100K_0201_5%
OUT2_CA_DET — R106 1M_0402_5%

<6> CPU_DP2_N0 — C300 0.1U_0402_16V7K — DPB_N0
<6> CPU_DP2_P0 — C299 0.1U_0402_16V7K — DPB_P0
<6> CPU_DP2_N1 — C277 0.1U_0402_16V7K — DPB_N1
<6> CPU_DP2_P1 — C278 0.1U_0402_16V7K — DPB_P1
<6> CPU_DP2_N2 — C276 0.1U_0402_16V7K — DPB_N2
<6> CPU_DP2_P2 — C301 0.1U_0402_16V7K — DPB_P2
<6> CPU_DP2_N3 — C298 0.1U_0402_16V7K — DPB_N3
<6> CPU_DP2_P3 — C302 0.1U_0402_16V7K — DPB_P3
<6> DDI2_AUX_DN — C285 0.1U_0402_16V7K — DPB_AUXN
<6> DDI2_AUX_DP — C289 0.1U_0402_16V7K — DPB_AUXP

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Issued Date	2014/09/08	Deciphered Date	2013/10/28

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Title: P32-DP MUX

Size | Document Number: LA-D301P | Rev: 0.4(X01)

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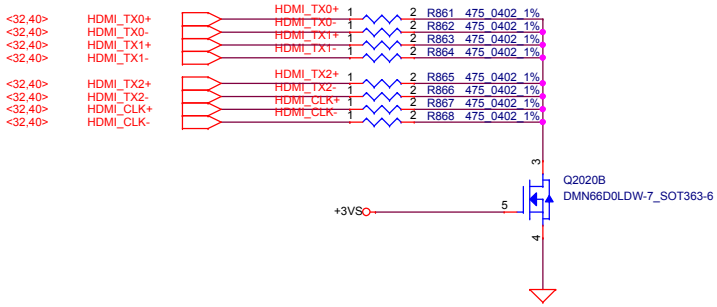
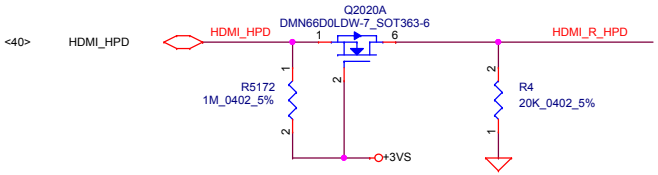
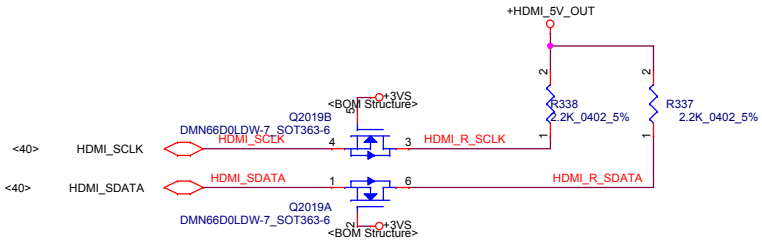
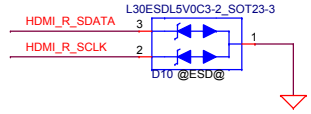
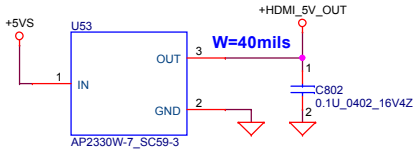
the onrigial BOM structure of R630, R631, R633, R665, R667, R668, R669, R671 is EMI@ , @ is for short pad only

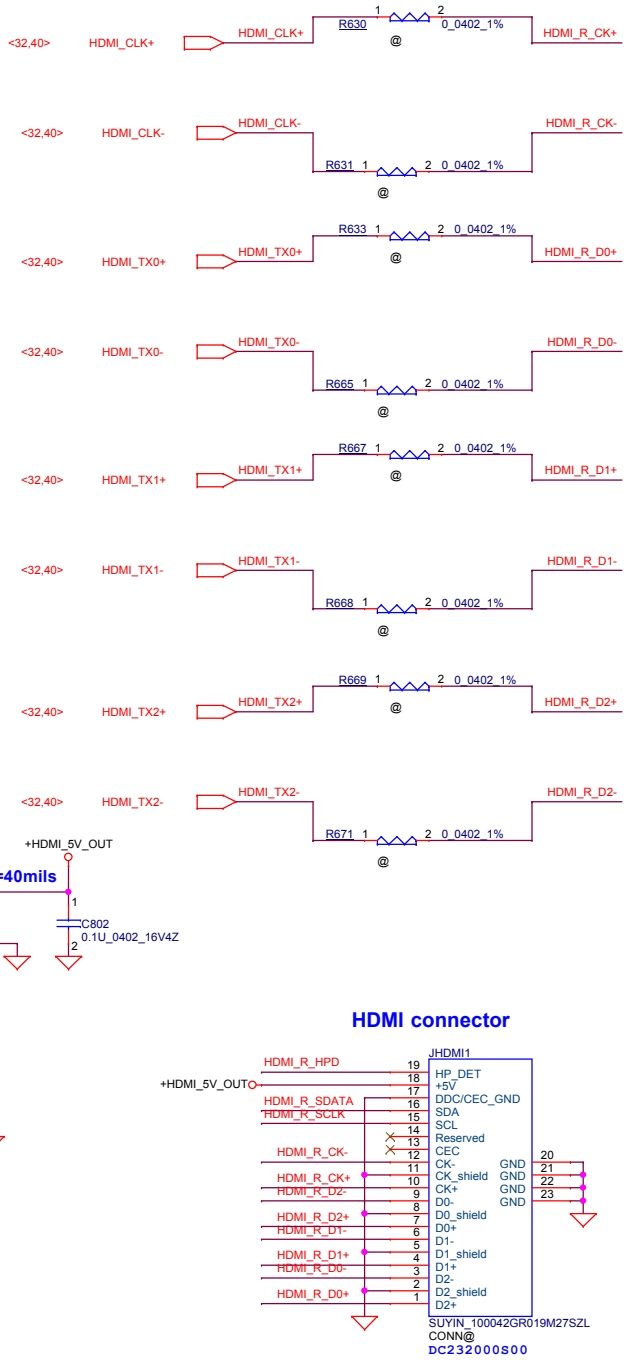












Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Title: HDMI CONN.

Size	Document Number	Rev
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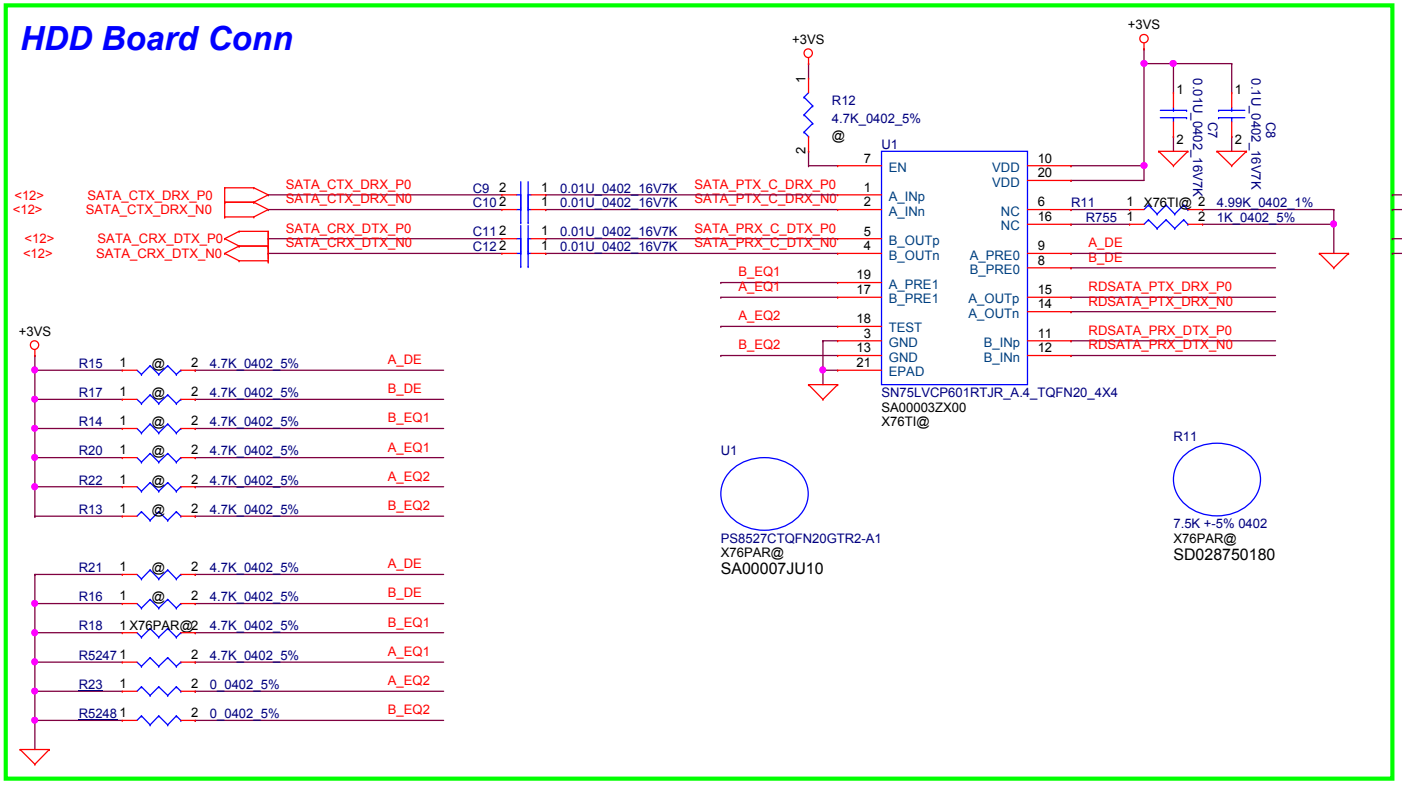
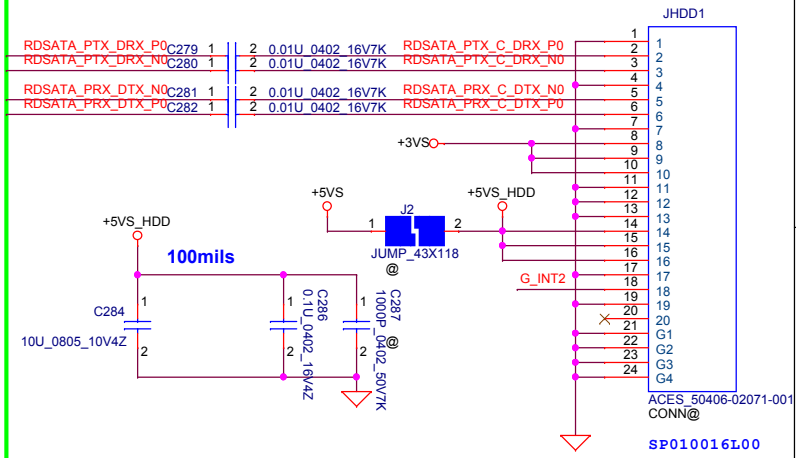
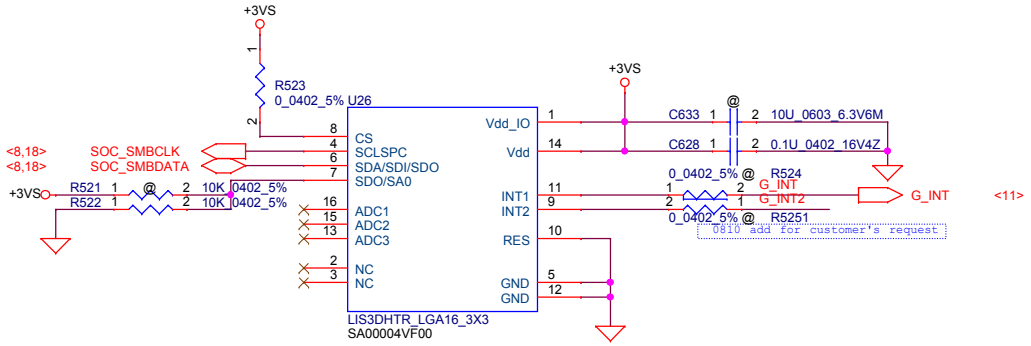
HDD Board Conn





APS G-Sensor




```
LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)
```

Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

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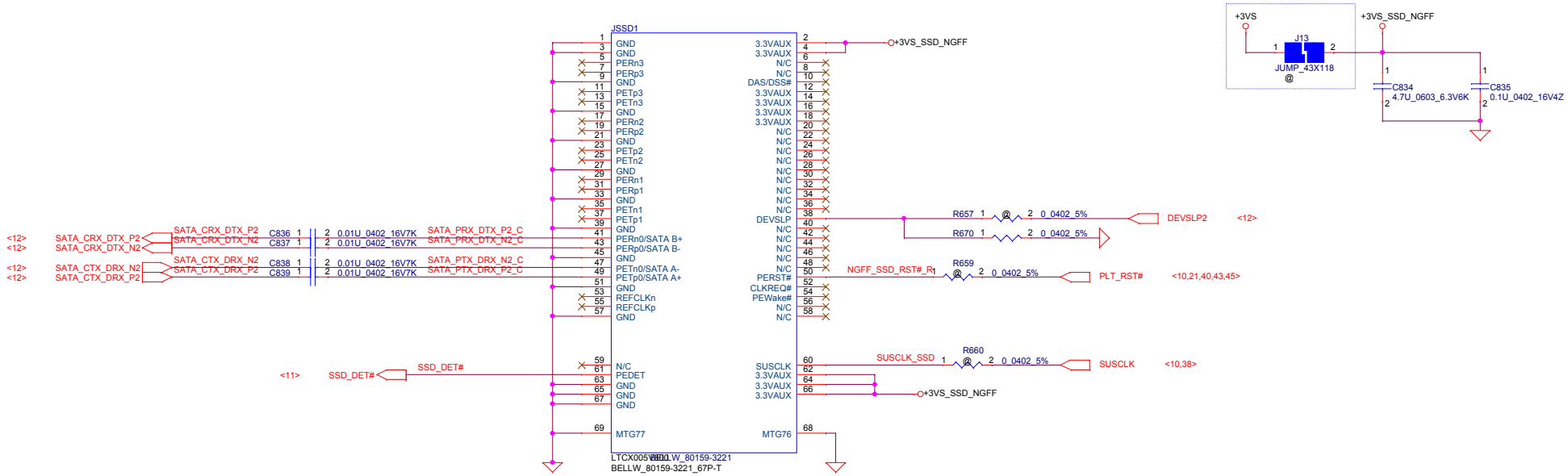
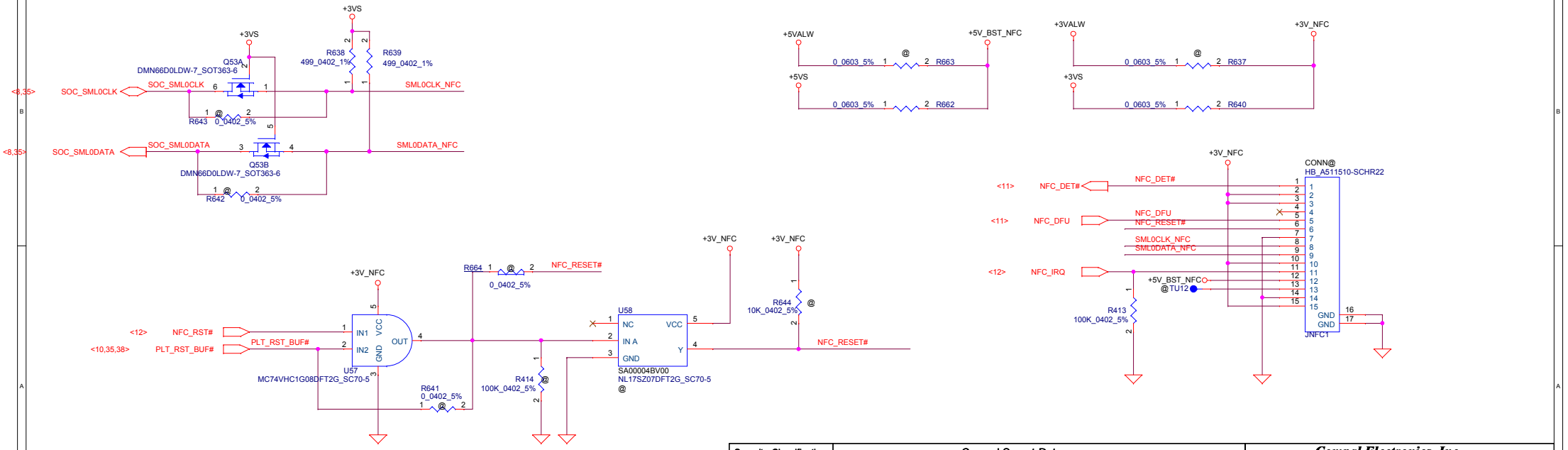
Compal Electronics, Inc.		
Title: HDD & G-Sensor		
Size: Custom	Document Number: LA-D301P	Rev: 1A
Date: Thursday, December 17, 2015	Sheet 33 of 63	





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Issued Date	2014/02/14	Deciphered Date	2015/02/14

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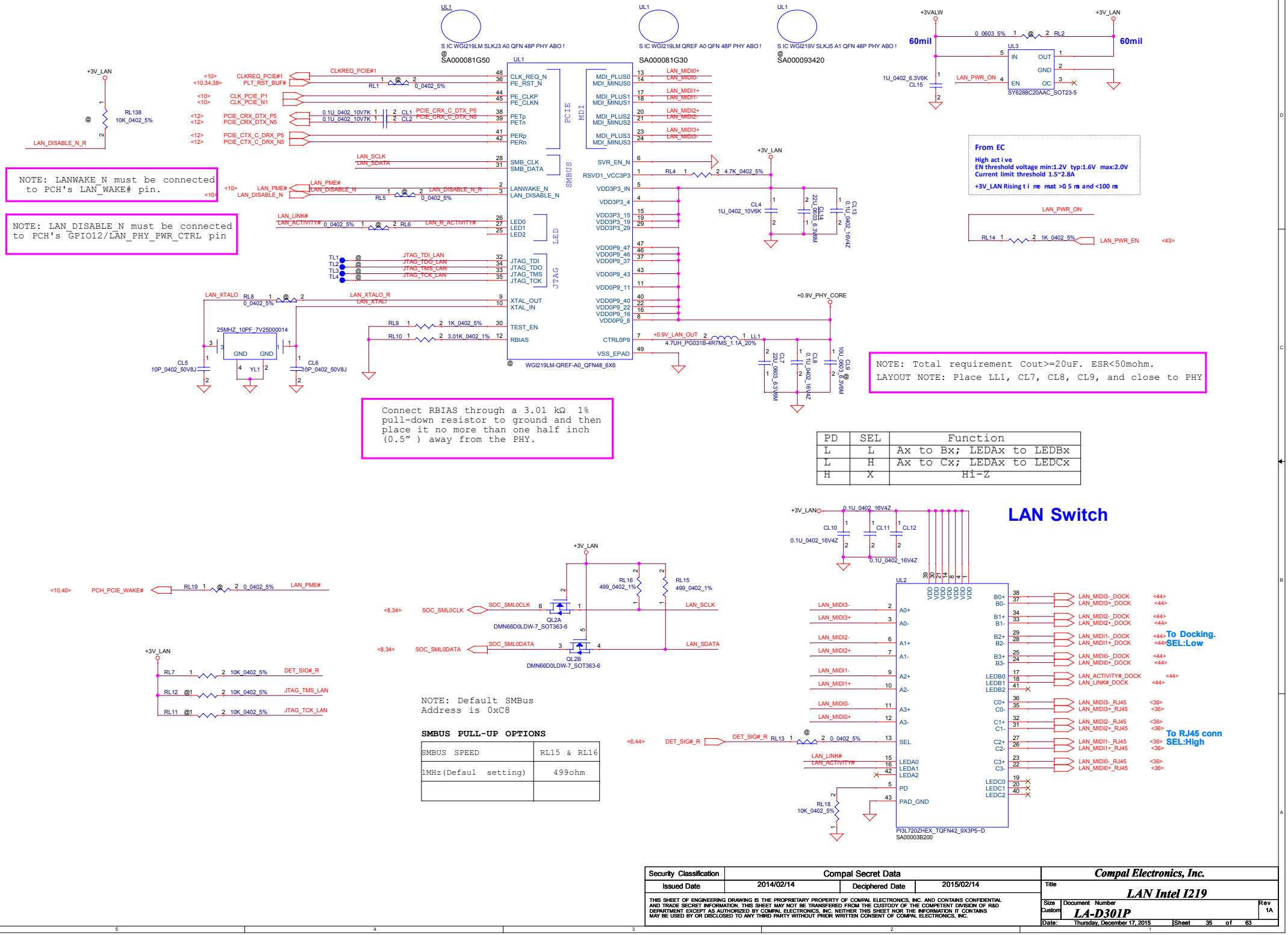
Compal Electronics, Inc.			
Title	mSATA & NFC		
Size: Custom	Document Number: LA-D301P		Rev: 1A
Date: Thursday, December 17, 2015	Sheet 34 of 63		



Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

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Title: LAN Intel I219

Size: Custom | Document Number: LA-D301P | Rev: 1A

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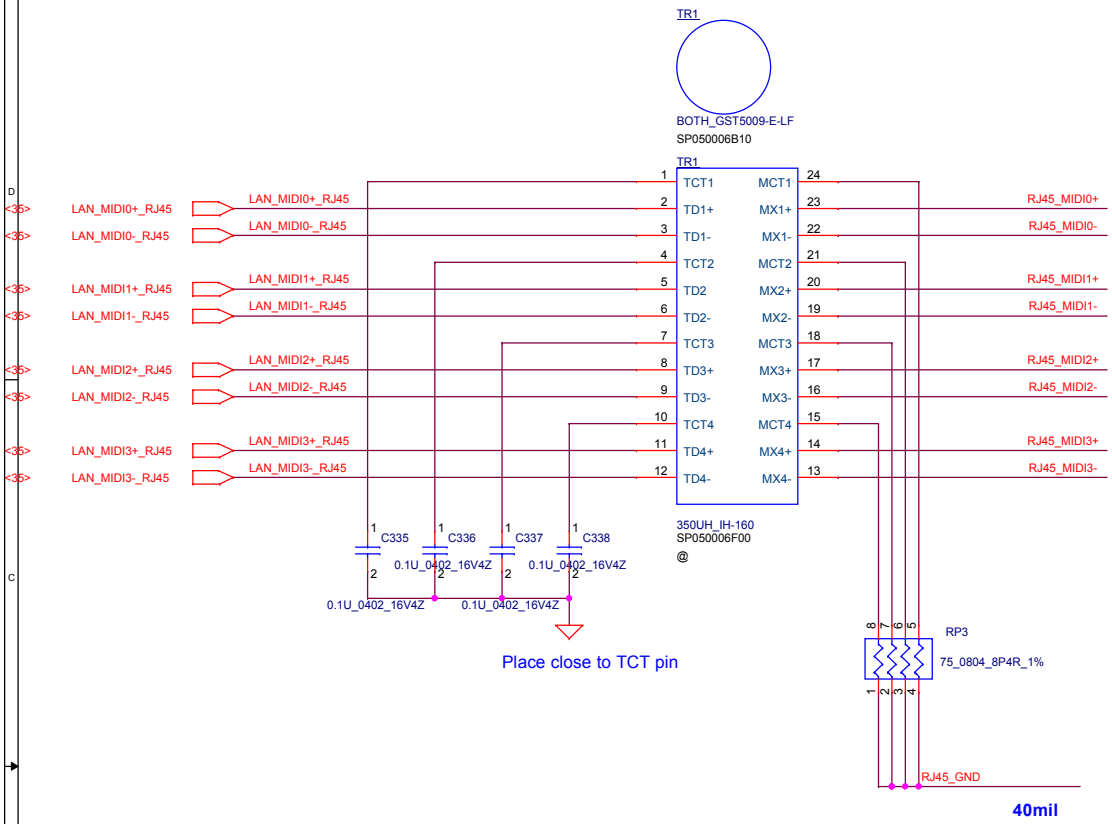
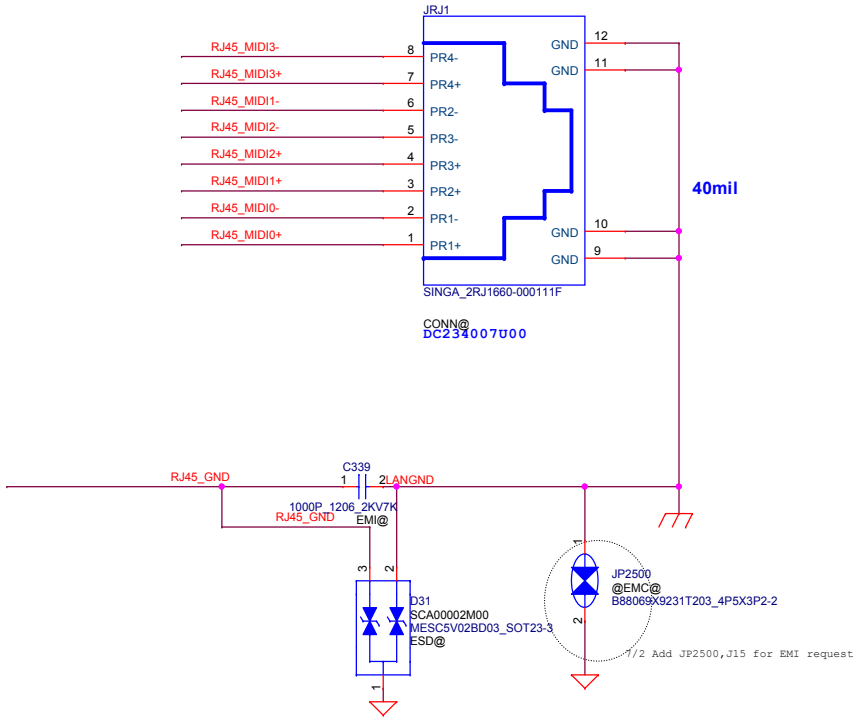
LAN Connector





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Issued Date	2014/02/14	Deciphered Date	2015/02/14

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Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size	Document Number	Rev
Custom	LA-D301P	1A

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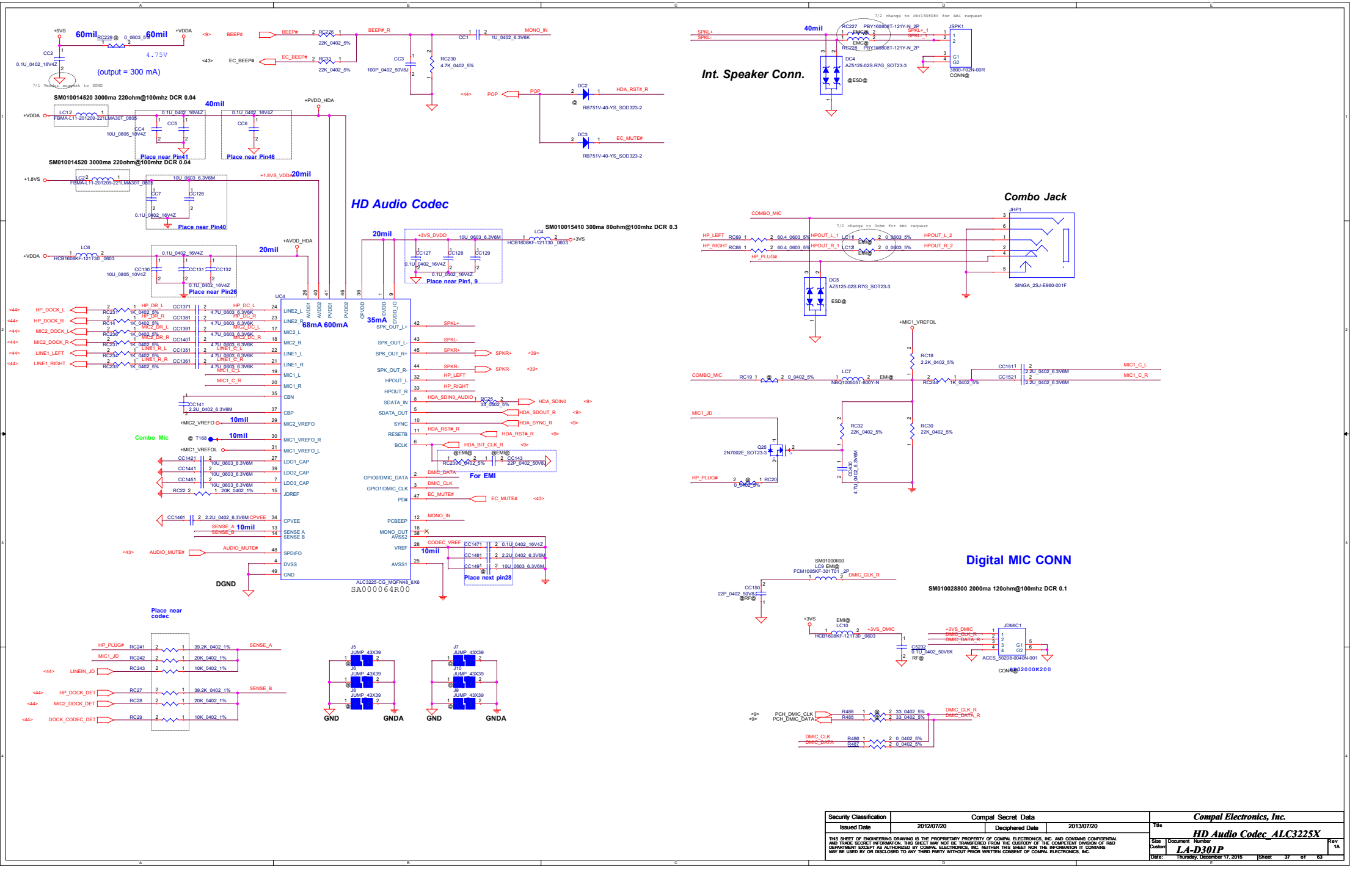

Security Classification	Compal Secret Data		
Issued Date	2012/07/20	Deciphered Date	2013/07/20

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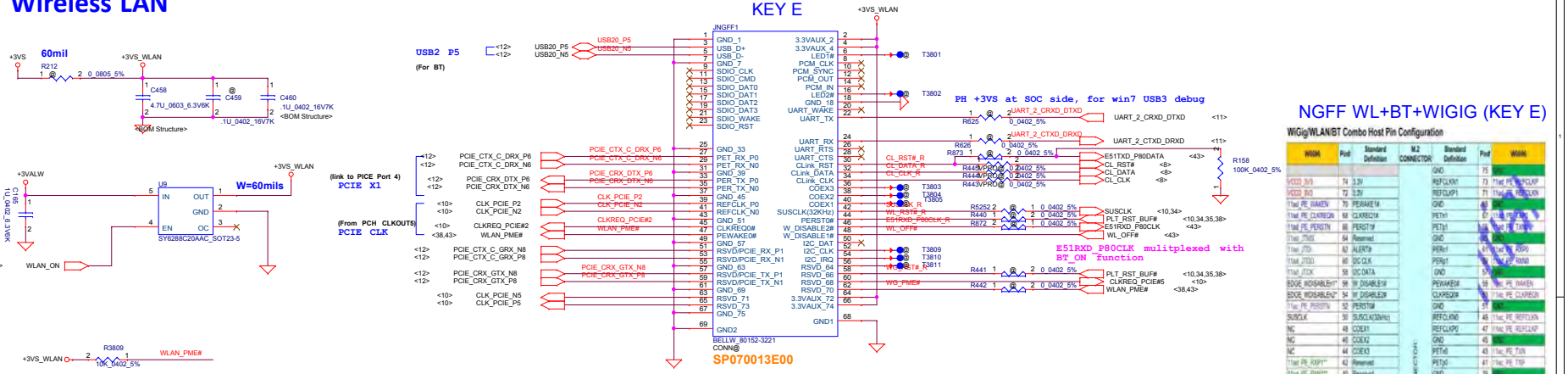
Compal Electronics, Inc.			
Title	HD Audio Codec_ALC3225X		
Size: Custom	Document Number: LA-D301P		Rev: 1A
Date: Thursday, December 17, 2015	Sheet 37 of 63		

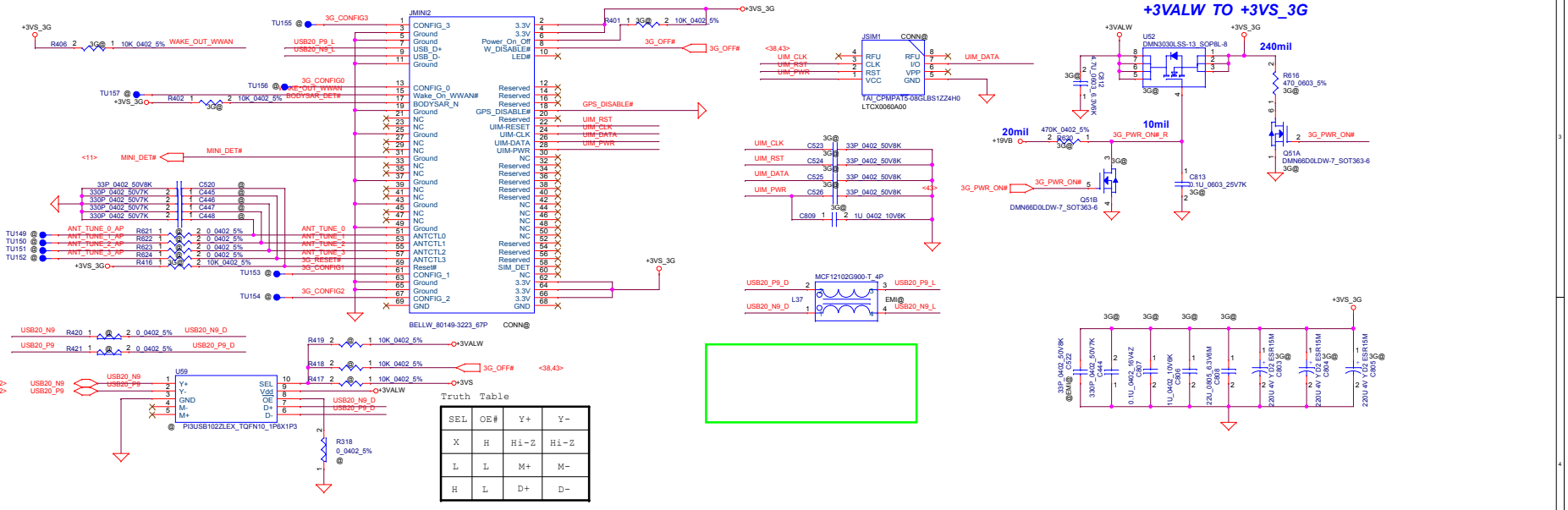
Wireless LAN



3.1.8.1.3.1.7.1. UART Wakeup

The UART power management protocol supports the following 4-wire and 5-wire interfaces:

- ~~RTS~~ UART_RXD (Input): Receive Data
- ~~CTS~~ UART_TXD (Output): Transmit Data
- UART_RTS (Input): Request to Send (Host Flow Control)
- UART_CTS (Output): Clear to Send (Device Flow Control)
- ~~Host Wake UP~~UART_Wake# (Output): Host wake-up line is optional in case the host support in band wake-up



SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

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Issued Date	2014/02/14	Deciphered Date	2015/02/14

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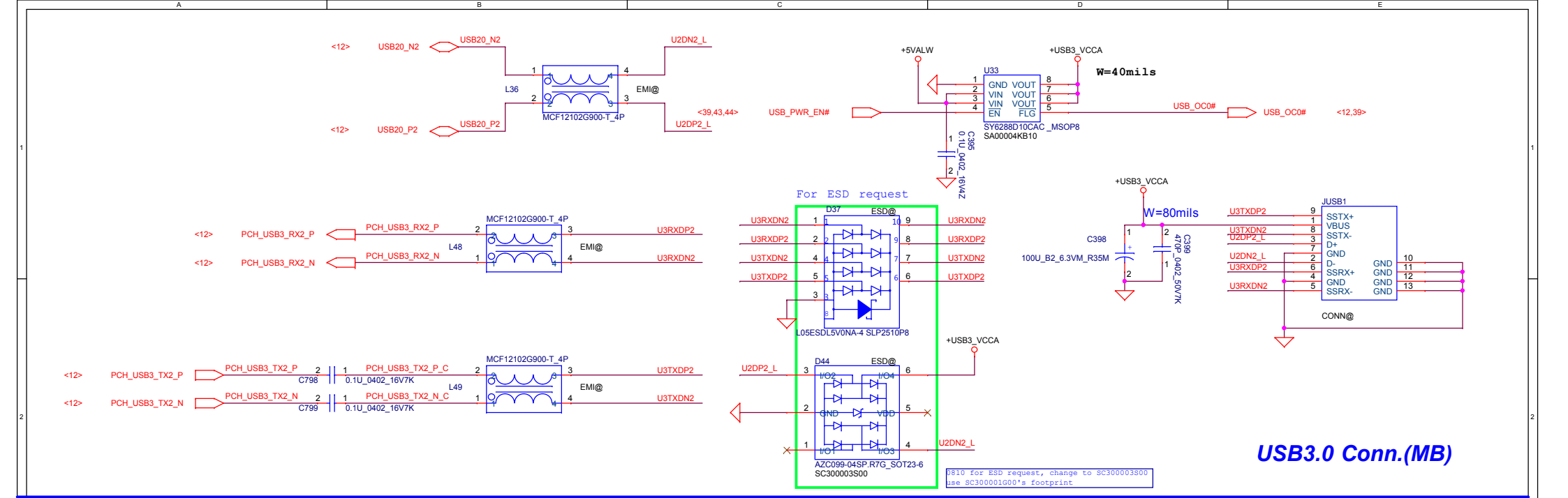
Compal Electronics, Inc.	
Title	mini Card & LTE CONN.
Size: Custom	Document Number: LA-D301P
Rev: 1A	
Date: Thursday, December 17, 2015	Sheet 38 of 63



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Issued Date	2014/02/14	Deciphered Date	2015/02/14

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Compal Electronics, Inc.

Title: USB3.0 & SSD

Size	Document Number	Rev
Custom	LA-D301P	1A

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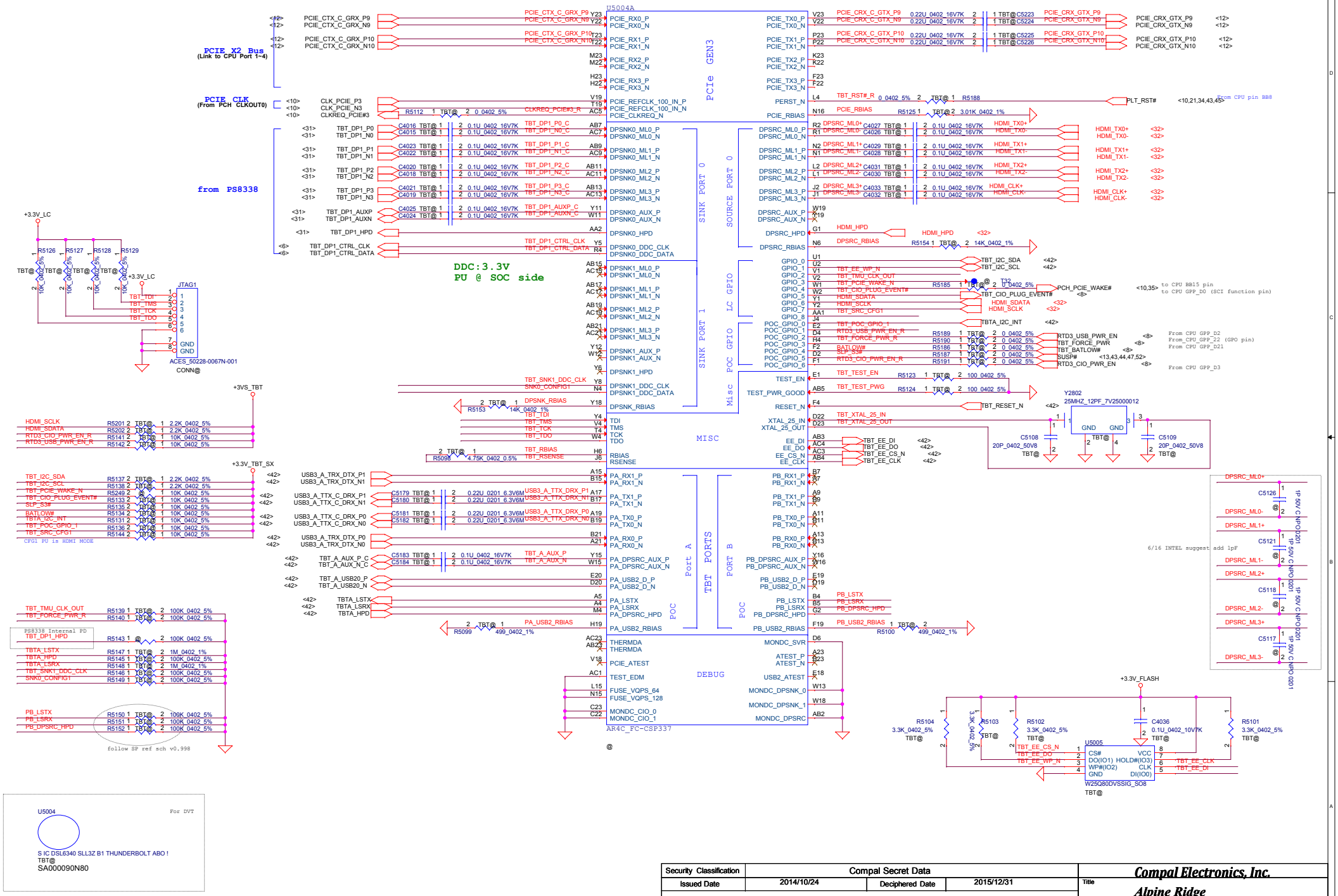

Security Classification	Compal Secret Data		
Issued Date	2014/10/24	Deciphered Date	2015/12/31

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Compal Electronics, Inc.

Title: Alpine Ridge

Size: Custom | Document Number: LA-D301P | Rev: 0.1

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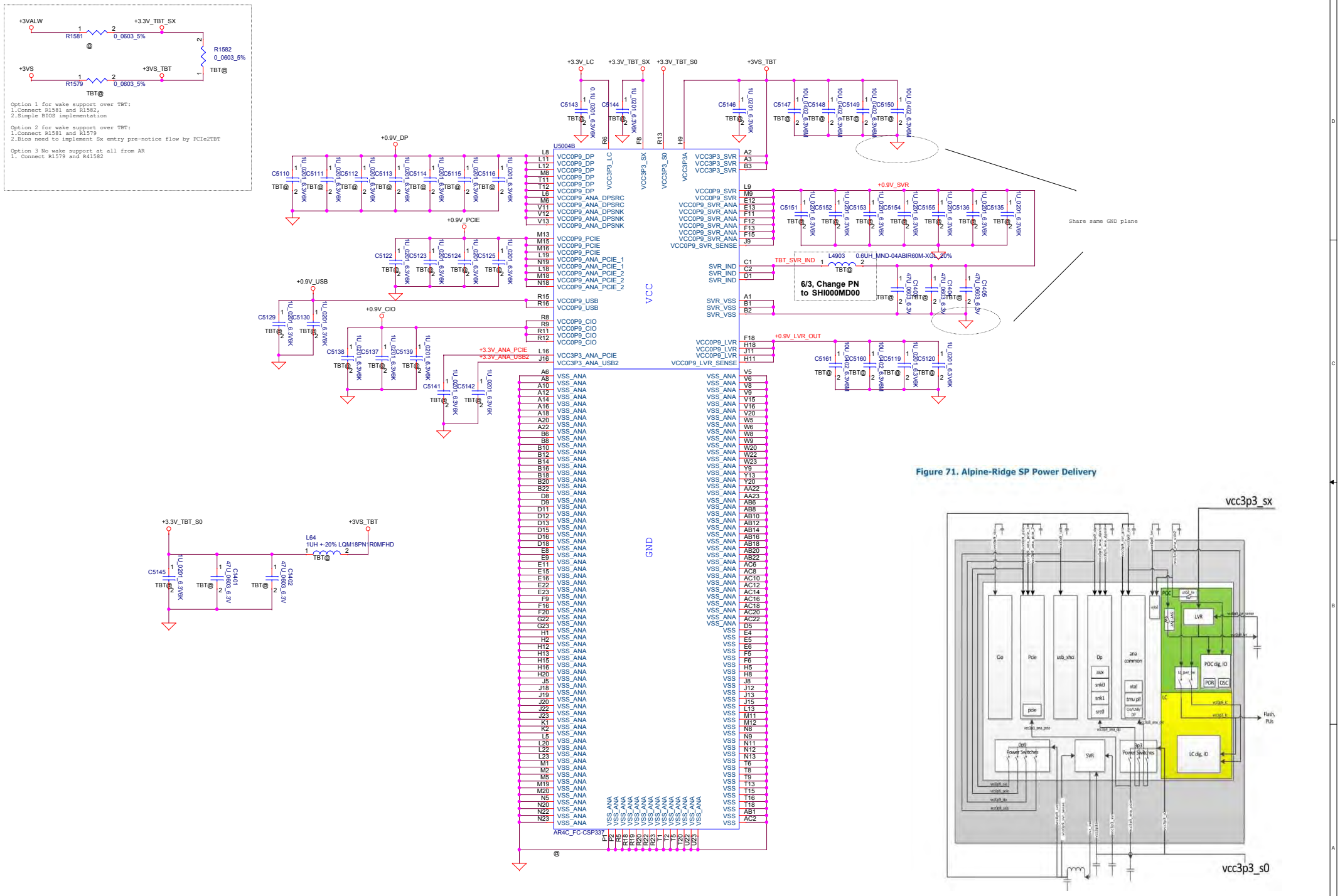

Figure 71. Alpine-Ridge SP Power Delivery

Security Classification	Compal Secret Data		
Issued Date	2014/10/24	Deciphered Date	2015/12/31

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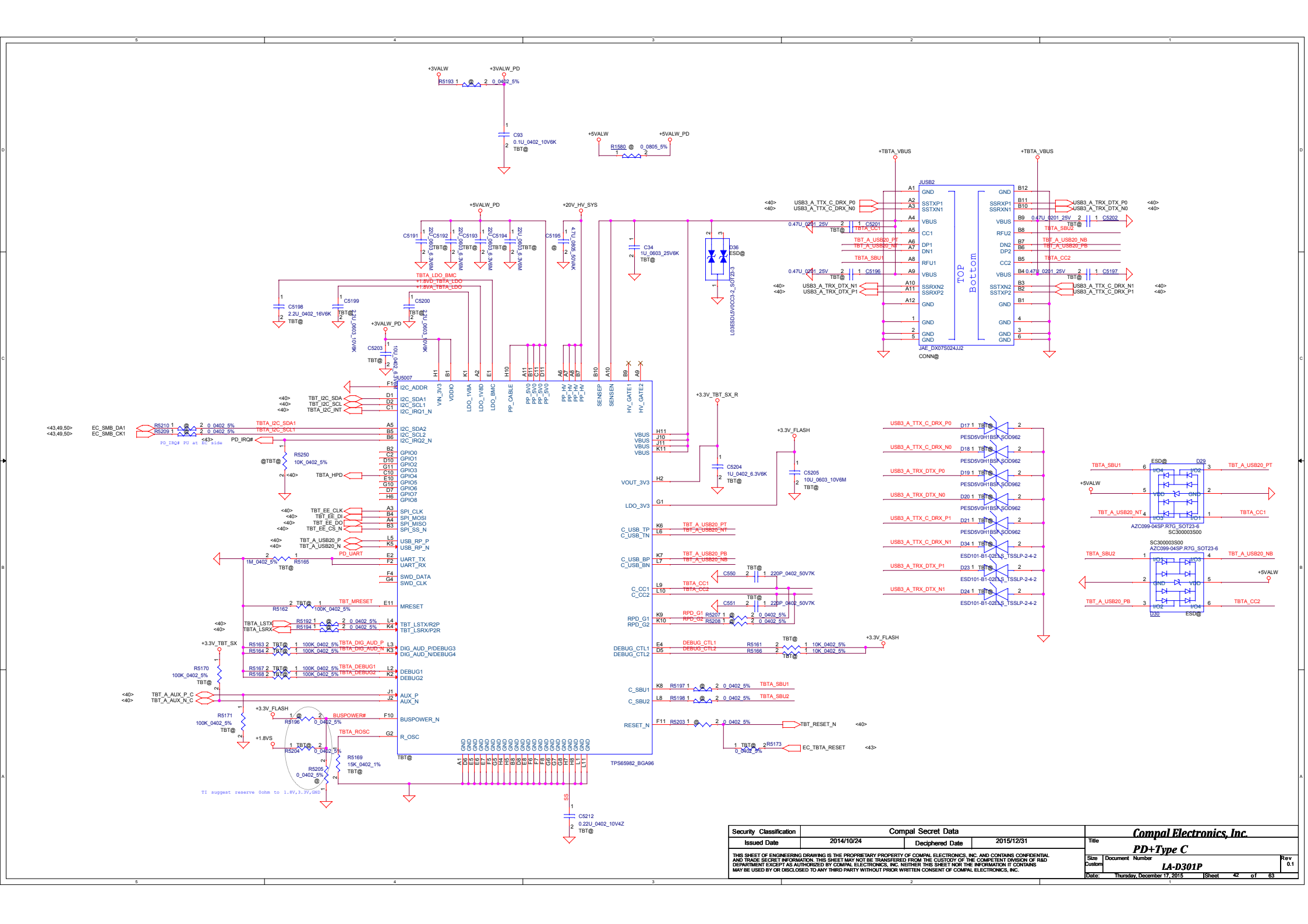
Title	Compal Electronics, Inc.		
	Alpine Ridge-POWER		
Size	Document Number		Rev
Custom	LA-D301P		0.1
Date:	Thursday, December 17, 2015	Sheet	41 of 63



Security Classification	Compal Secret Data		
Issued Date	2014/10/24	Deciphered Date	2015/12/31

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Compal Electronics, Inc.

Title: **PD+Type C**

Size	Document Number	Rev
Custom	LA-D301P	0.1

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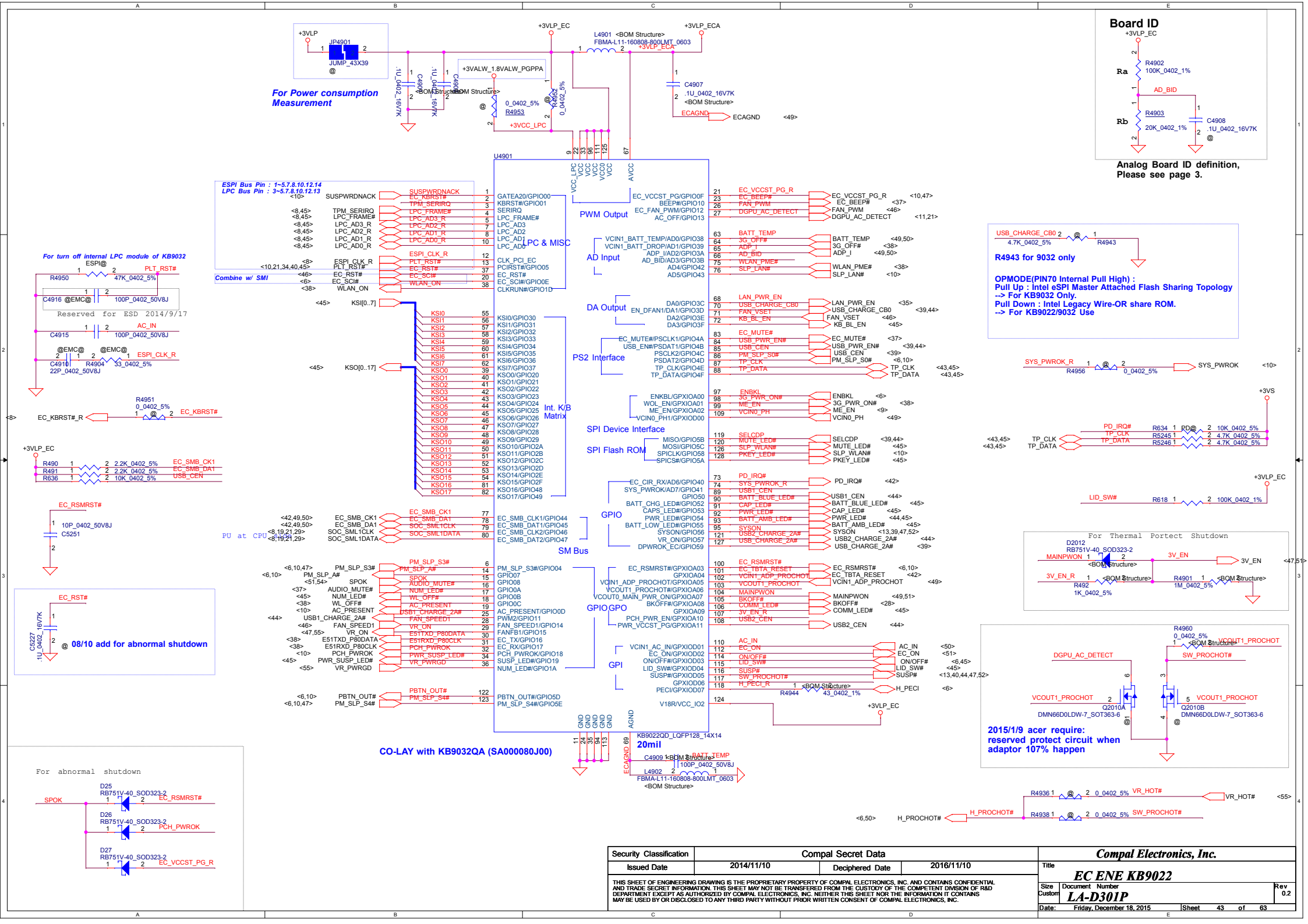
Board ID
Analog Board ID definition, Please see page 3.
For Power consumption Measurement
U4901
KB9022QD_LQFP128_14X14
20mil
CO-LAY with KB9032QA (SA000080J00)
PWM Output
AD Input
PS2 Interface
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
DA Output
Int. K/B Matrix
PC & MISC
ESPI Bus Pin : 1~5.7.8.10.12.14
LPC Bus Pin : 3~5.7.8.10.12.13
Combine w/ SMI
For turn off internal LPC module of KB9032
Reserved for ESD 2014/9/17
PU at CPU
08/10 add for abnormal shutdown
For abnormal shutdown
R4943 for 9032 only
OPMODE(PIN70 Internal Pull High) :
Pull Up : Intel eSPI Master Attached Flash Sharing Topology
--> For KB9032 Only.
Pull Down : Intel Legacy Wire-OR share ROM.
--> For KB9022/9032 Use
For Thermal Portect Shutdown
2015/1/9 acer require:
reserved protect circuit when
adaptor 107% happen
Security Classification
Compal Secret Data
Issued Date
2014/11/10
Deciphered Date
2016/11/10
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Title
EC ENE KB9022
Size
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Document Number
LA-D301P
Rev
0.2
Date:
Friday, December 18, 2015
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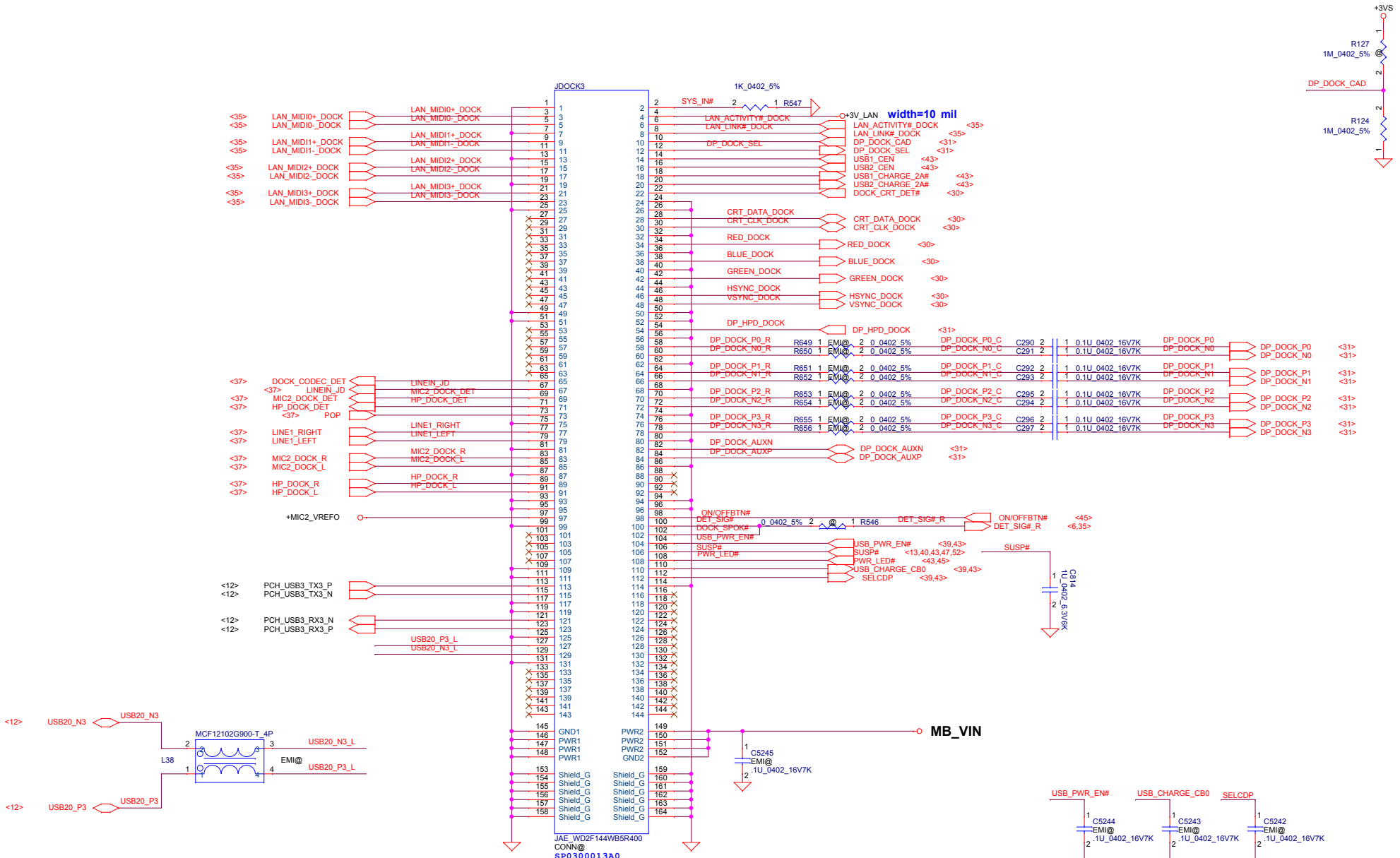
63



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Issued Date	2014/02/14	Deciphered Date	2015/02/14

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Compal Electronics, Inc.	
Title	E Series Dcok CONN.
Size: Custom	Document Number: LA-D301P
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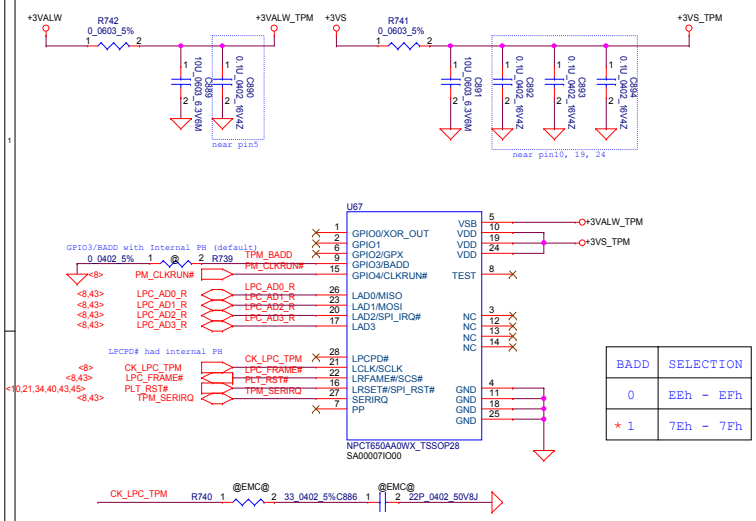
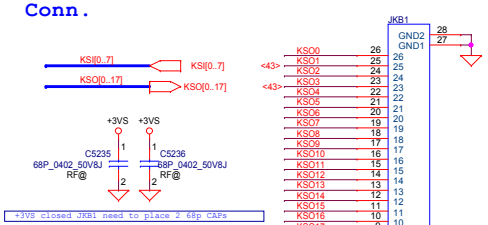
Date: Thursday, December 17, 2015	Sheet 44 of 63

TPM

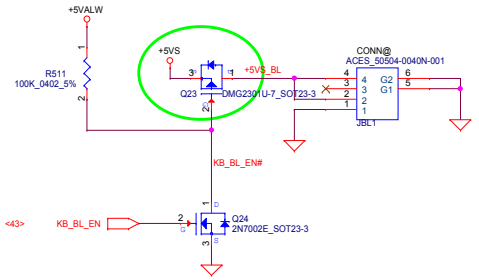


BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh

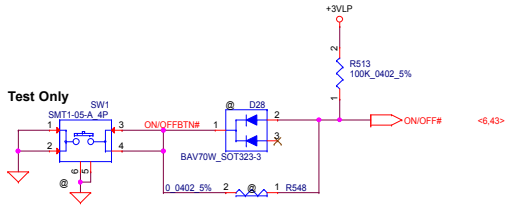
KB Conn.



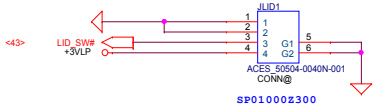
KB Backlight Conn



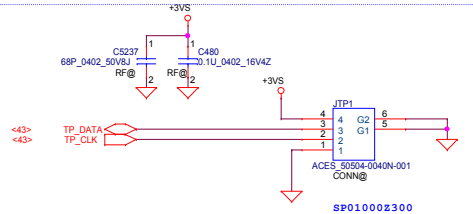
ON/OFF BTN



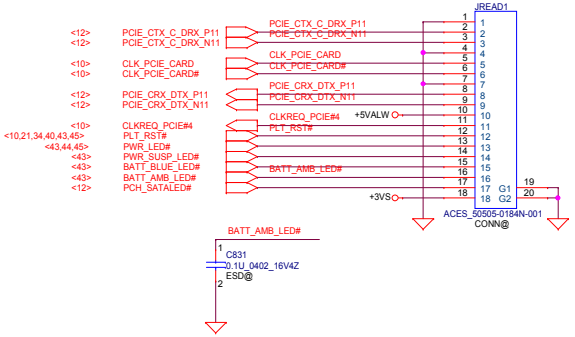
Lid Switch/B (Hall Effect Switch)



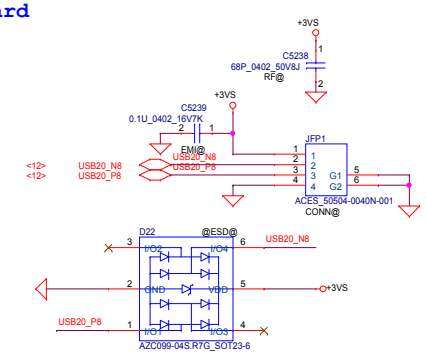
TP Conn.



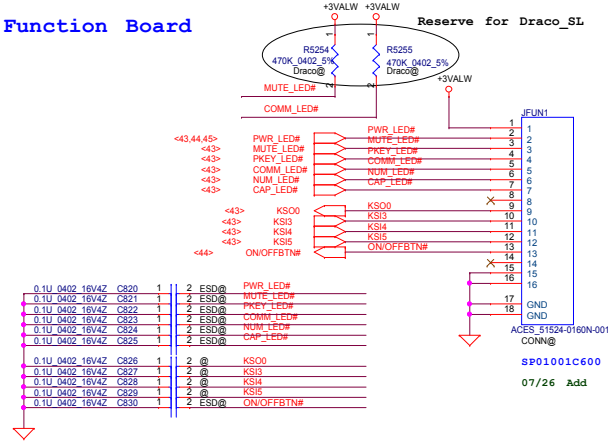
CardReader Board



FP Board



Function Board



Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

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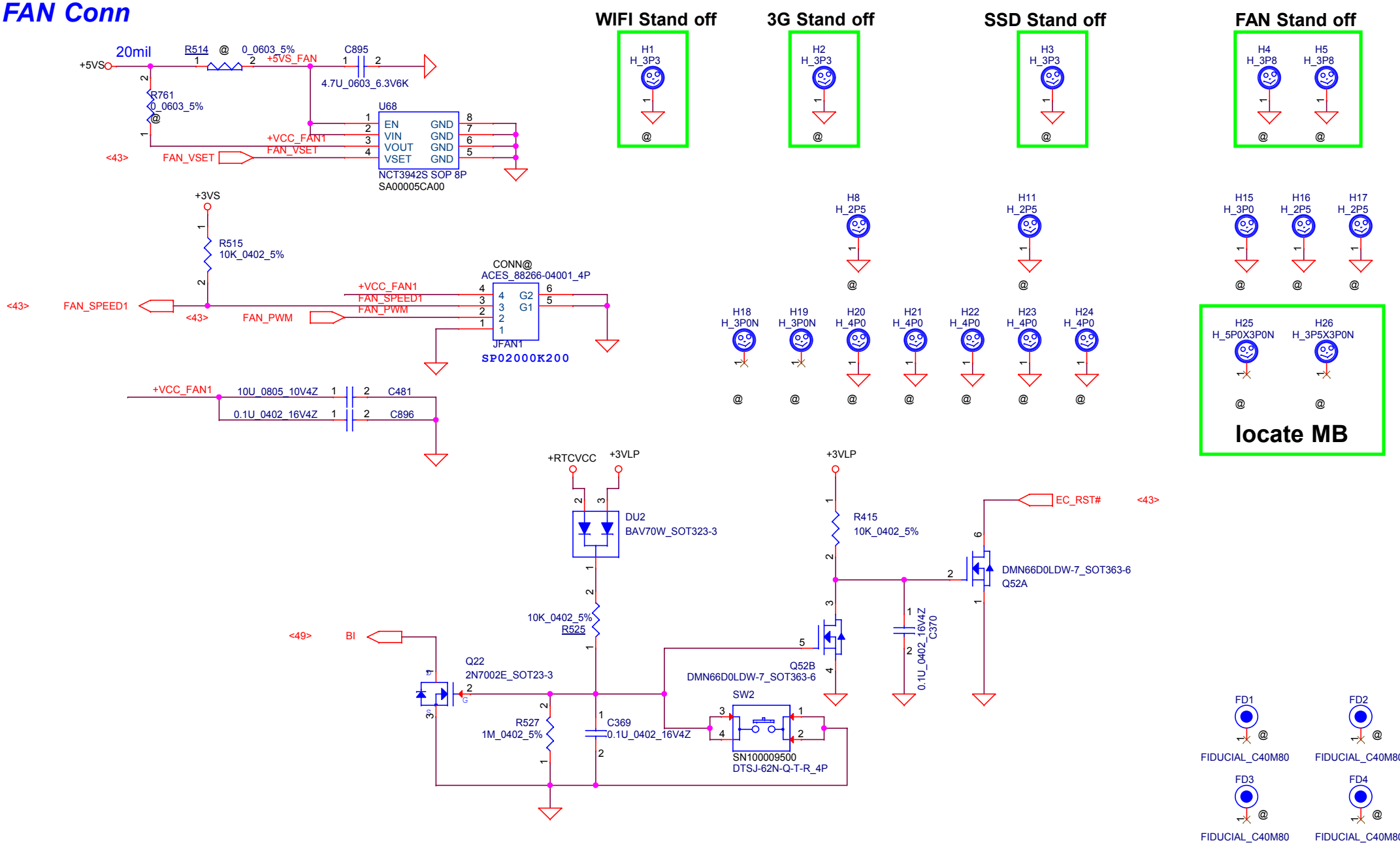
Compal Electronics, Inc.	
Title	KB/TP/LID/TPM/FUN/FP/CARD
Size: C	Document Number: LA-D301P
Rev: 1A	
Date: Thursday, December 17, 2015	Sheet 45 of 63

FAN Conn



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Issued Date	2014/02/14	Deciphered Date	2015/02/14

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Compal Electronics, Inc.			
Title: FAN & Screw			
Size: Custom	Document Number: LA-D301P		Rev: 1A
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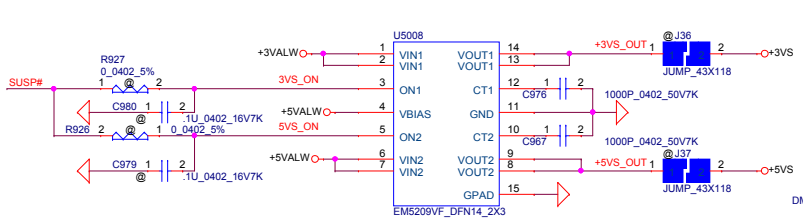
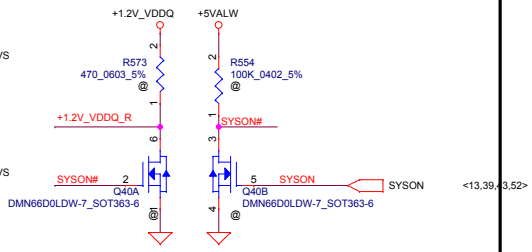
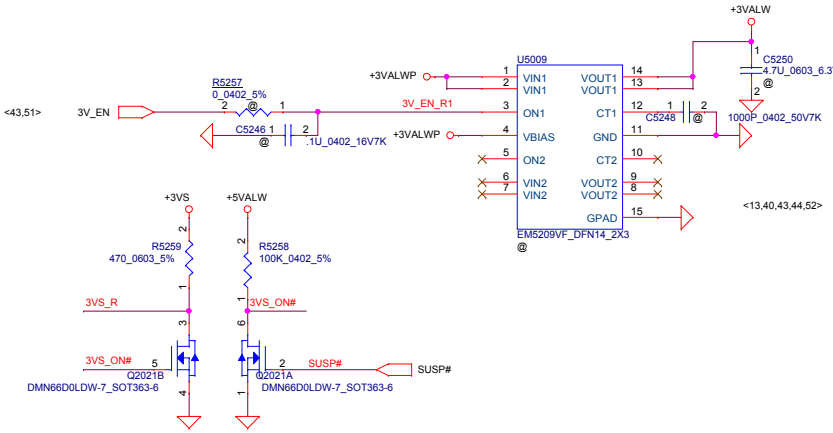
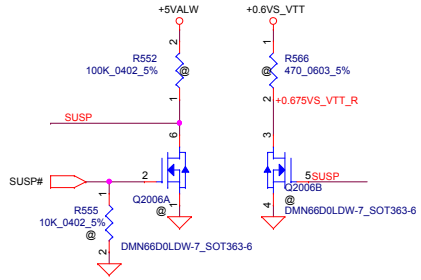
DC & VGA Interface

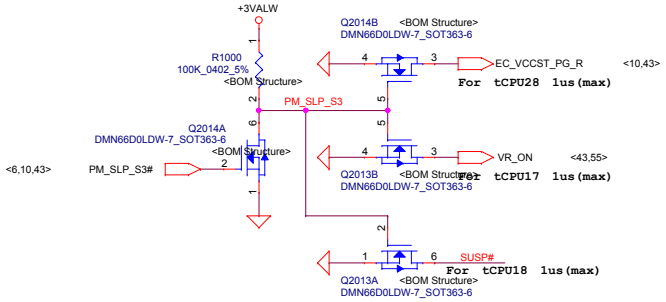


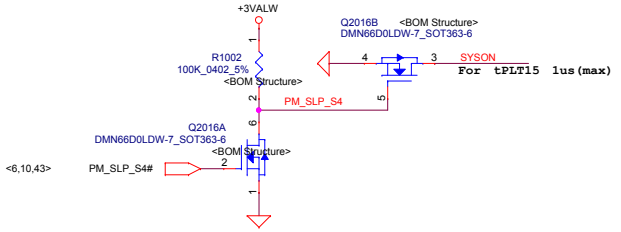




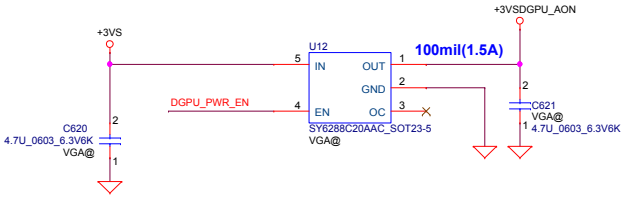


For Power Of f Sequence



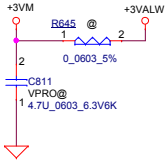


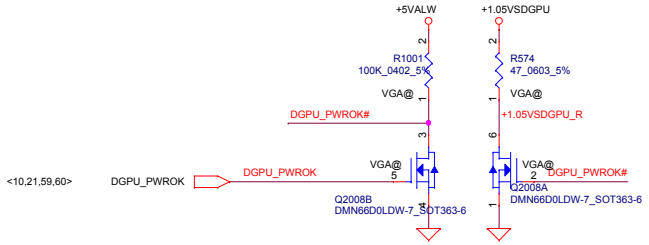
+3VS to +3VSDGPU_AON for GPU



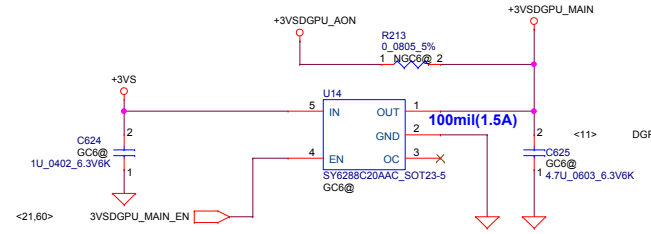
+3VALW to +3VM for Intel AMT

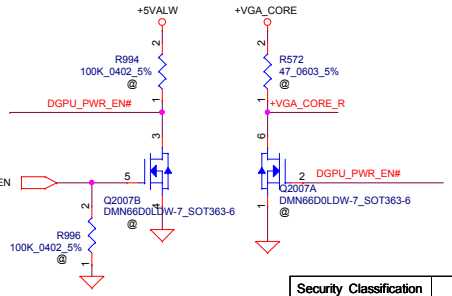
20mil(68mA)

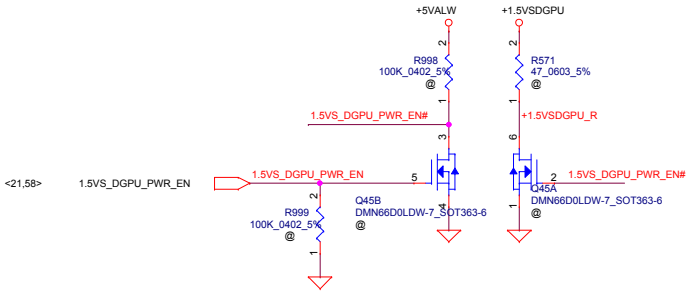




+3VS to +3VSDGPU_MAIN for GC6-2.0







3VSDGPU_MAIN_EN From GPU

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Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-D301P	0.2

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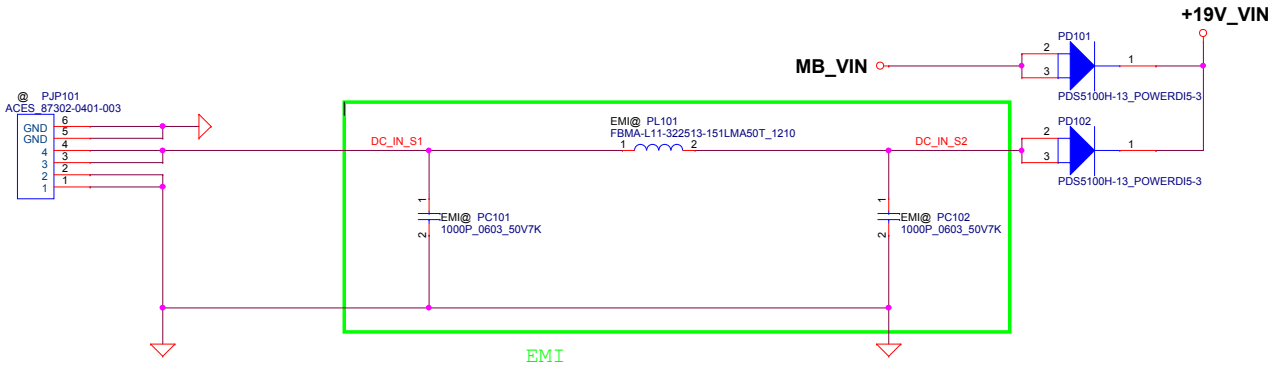
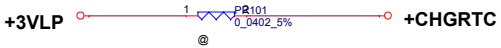
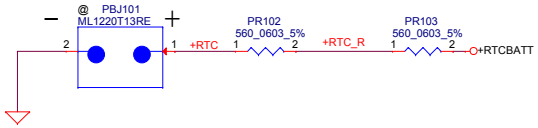
2015/7/8
PD101 and PD102 SCS00002F00 change to SCS00002M00







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Compal Electronics, Inc.

Title: **PWR DCIN / Pre-charge**

Size: Custom | Document Number: **B4DBU M/B LA-D301P** | Rev: 0.1

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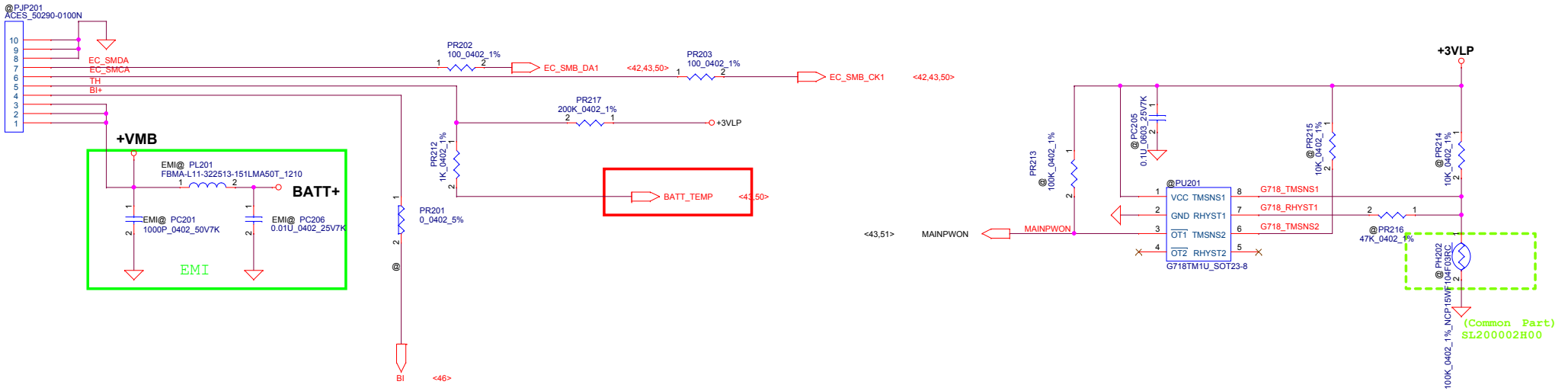
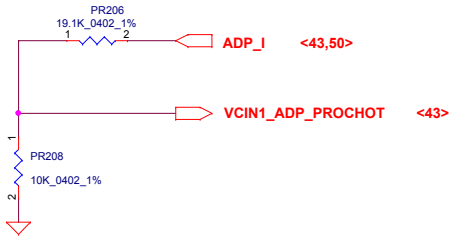


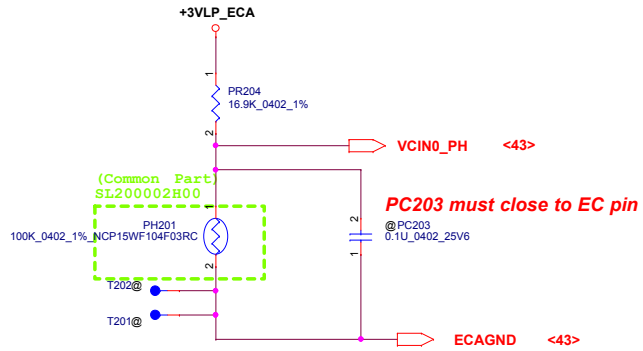
PH1 under CPU botten side :
CPU thermal protection at 92 +-3 degree C
Recovery at 56 +-3 degree C

2015/07/09 update

For KB9022 sense 20mΩ	Active	Recovery
65W PR206 19.1K ohm SD034191280	84.5W,0.61V	65W,0.47V



T202 T201 must close to PH201



PC203 must close to EC pin

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Issued Date	2014/11/10	Deciphered Date	2016/11/10

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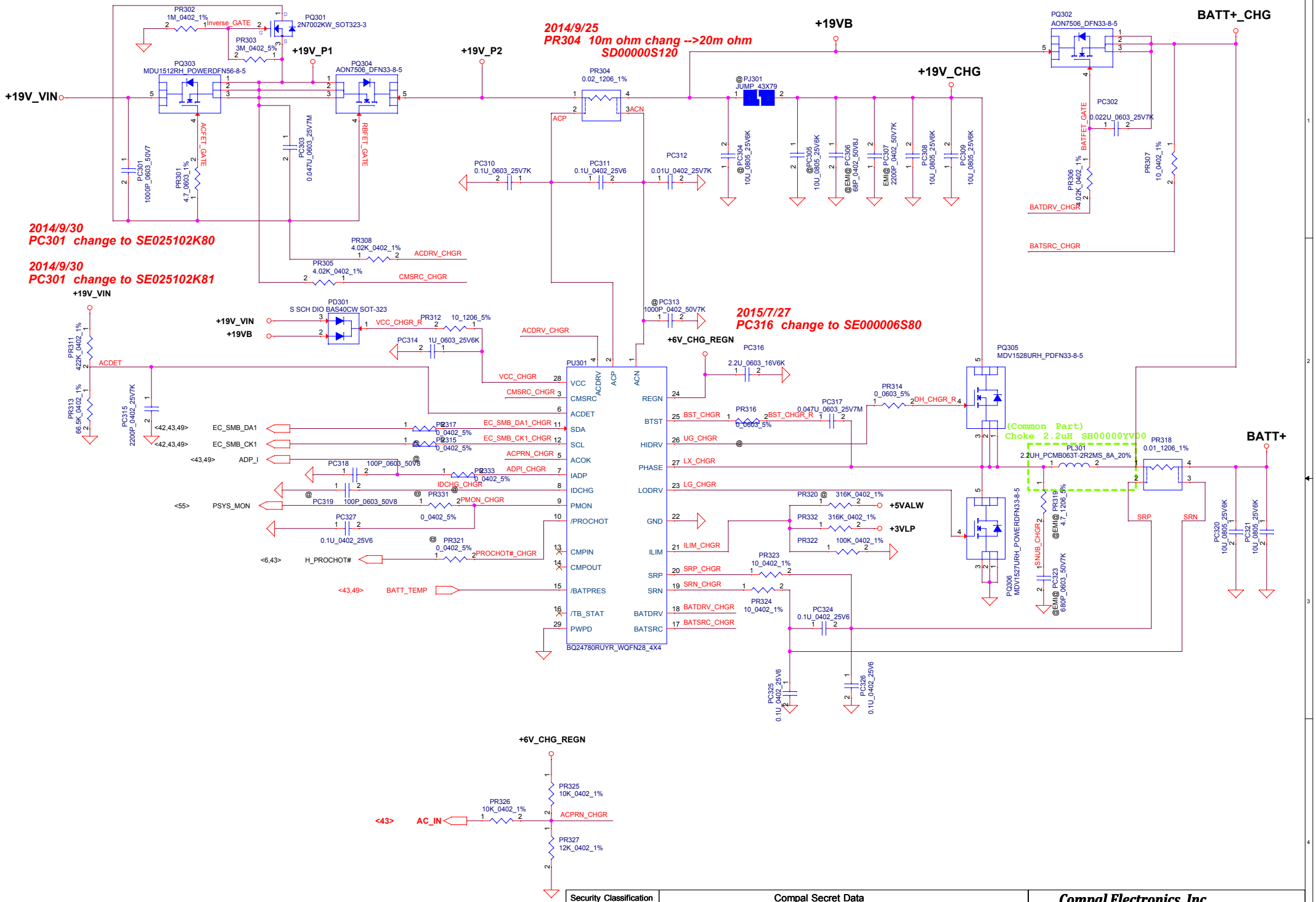
Title	PWR-BATTERY CONN/OTP		
Size: Custom	Document Number: B4DBU M/B LA-D301P		Rev: 0.1
Date: Thursday, December 17, 2015	Sheet 49 of 63		



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Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: BQ24780

Size	Document Number	Rev
Custom	B4DBU M/B LA-D301P	0.1

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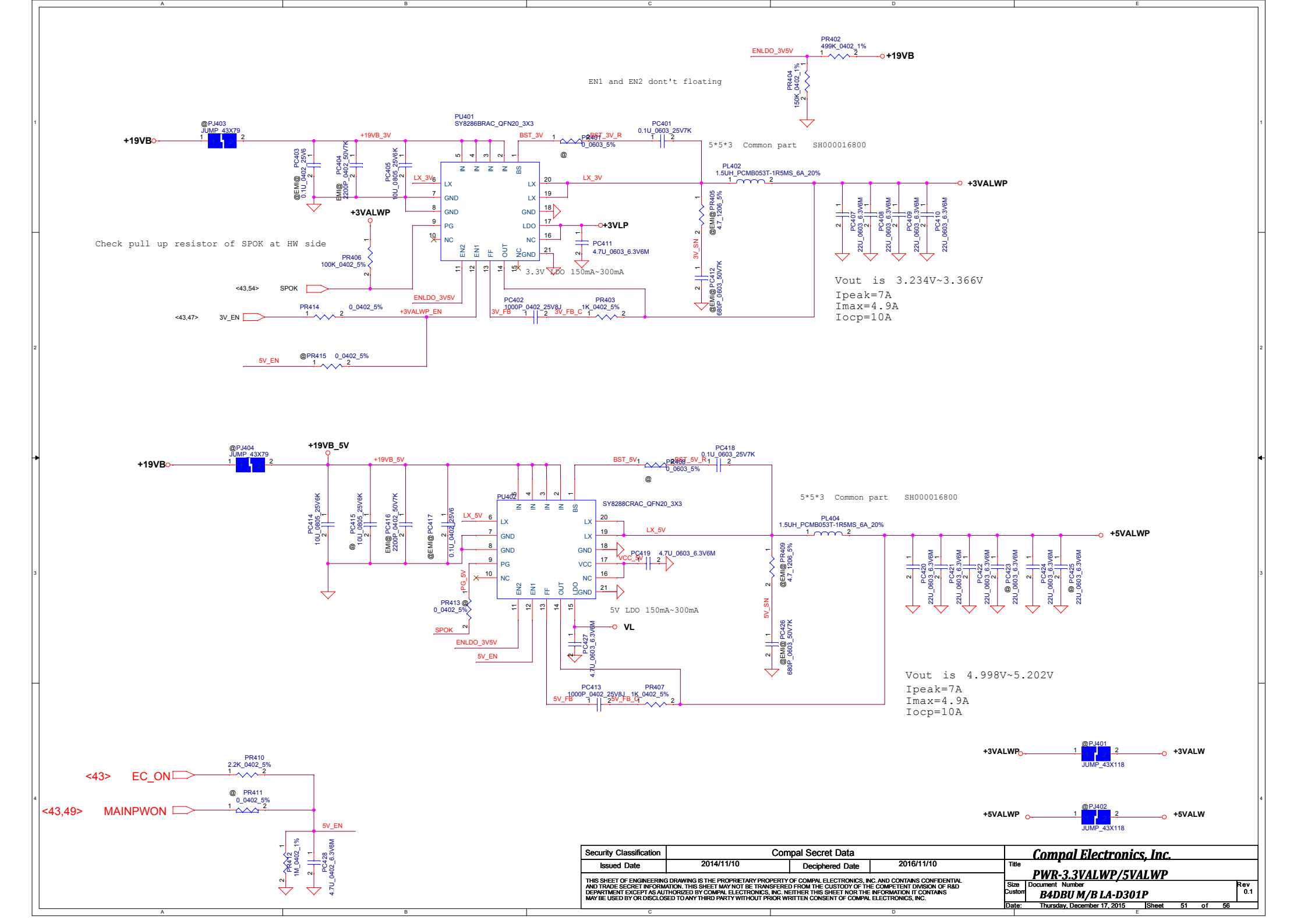

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Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: PWR-3.3VALWP/5VALWP

Size	Document Number	Rev
Custom	B4DBU M/B LA-D301P	0.1

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Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.2VP.
If you have +1.2V and +0.6V sequence question, you can change from +1.2VP to +1.2VS.

0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A

Choke 1.5uH SH000016700
Common Part 7*7*3

Update Pc510 change to Common Part SF000006S00 20141227

Change PR503 to 17.8K ohm
OCP setting 9.6A

change PQ502 form 7506 to 7716, 20150108

Vout=0.75V* (1+Rup/Rdown)
=0.75*(1+(6.19/10))
=1.2V

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 23.2mohm(Typ), 27.8mohm(Max)
Idsm: 10.1A@Ta=25C, 8.1A@Ta=70C

L/S Rds(on): 13.5mohm(Typ), 16.5mohm(Max)
Idsm: 12A@Ta=25C, 9.5A@Ta=70C

Choke: 7x7x3
Rdc=14mohm(Typ), 15mohm(Max)

Switching Frequency: 285kHz
Ipeak=8A
Iocp~9.6A
OVP: 110%~120%
VFB=0.75V, Vout=1.2V
MOSFET footprint: SIS412DN

3.8x3.8xH1.8
DCR: 20~25mohm
Idc / Isat: 3.8A

Iocp : 3.7A
FSW : 1MHz

5/29 add PC526
In order to avoid capacitor decay

Vout=0.6V* (1+Rup/Rdown)
2.504V= 0.6V*(1+36.5K/11.5K)

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Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: +1.2VP/+0.6VSP/+2.5VP

Size	Document Number	Rev
Custom	B4DBU M/B LA-D301P	0.1

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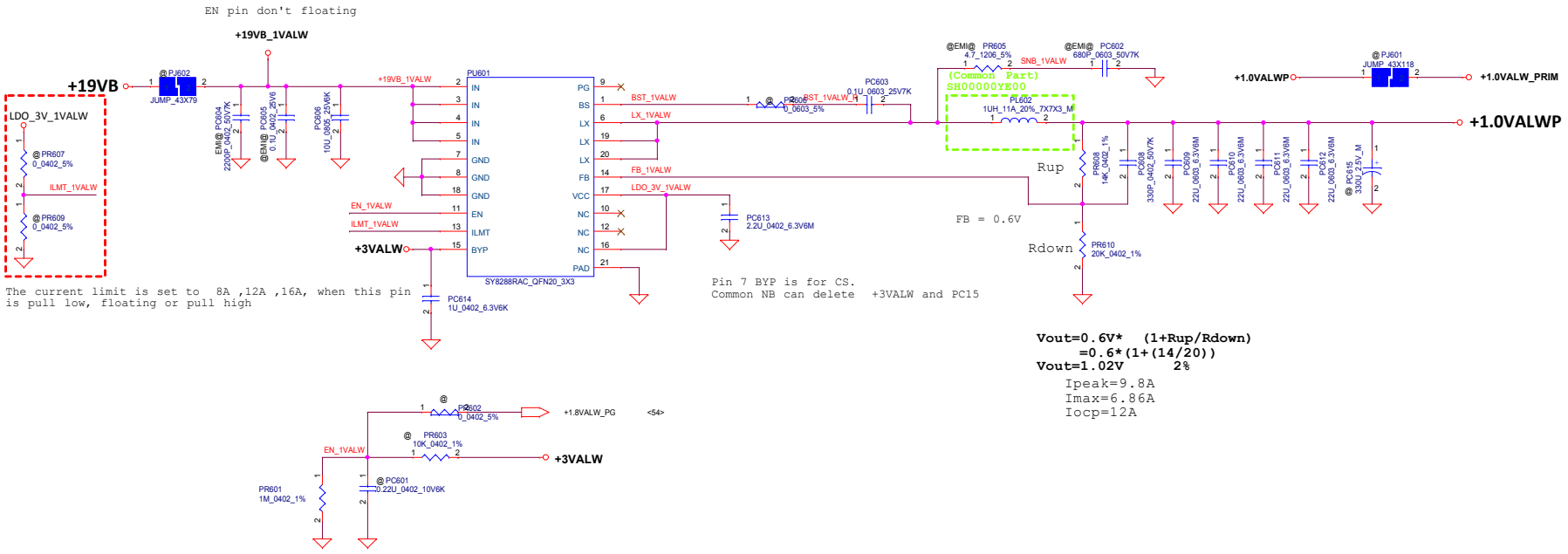

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

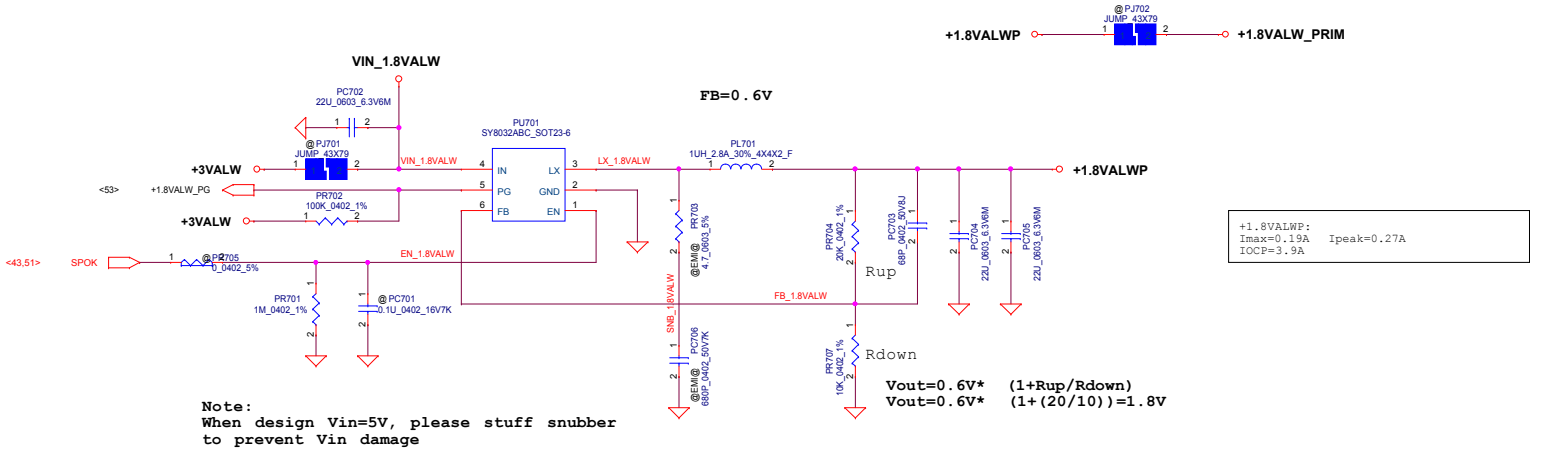
Title: +1.0VALWP

Size	Document Number	Rev
C	B4DBU M/B LA-D301P	0.1

Date: Thursday, December 17, 2015 Sheet 53 of 63

Module model information

SY8032_V2.mdd



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Compal Electronics, Inc.			
Title: SY8032			
Size: C	Document Number: B4DBU M/B LA-D301P		Rev: 0.1
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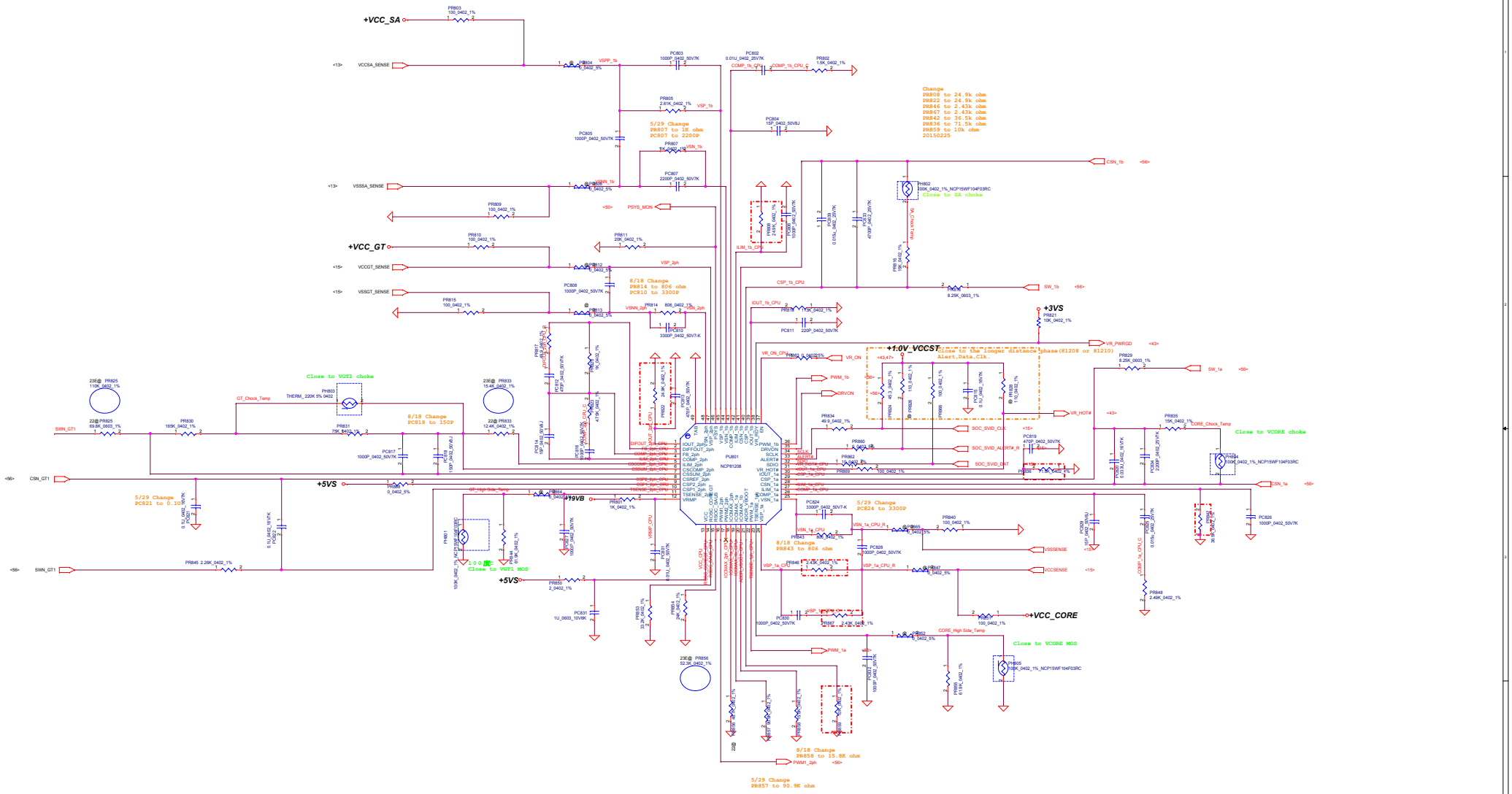
+VCC_SA
+VCC_GT
+1.0V_VCCST
+3VS
+5VS
+19VB
+VCC_CORE
Change PR808 to 24.9k ohm PR822 to 24.9k ohm PR846 to 2.43k ohm PR867 to 2.43k ohm PR842 to 36.5k ohm PR836 to 71.5k ohm PR839 to 10k ohm 20150225
5/29 Change PR807 to 1K ohm PC807 to 2200P
8/18 Change PR814 to 806 ohm PC810 to 3300P
Close to VGT1 choke
Close to VGT1 MOS
Close to SA choke
Close to VCORE choke
Close to VCORE MOS
Close to the longest distance phase(81208 or 81210) Alert,Data,Clk.
9/18 Change PC818 to 150P
5/29 Change PC821 to 0.1U
5/29 Change PC824 to 3300P
8/18 Change PR843 to 806 ohm
8/18 Change PR858 to 15.8K ohm
5/29 Change PR857 to 90.9K ohm
PU801 NCP81208
Security Classification
Issued Date 2014/11/10
Deciphered Date 2016/11/10
Compal Secret Data
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Compal Electronics, Inc.
Title IMVP8, NCP81206
Size D
Document Number B4DBU M/B LA-D301P
Rev 0.1
Date: Thursday, December 17, 2015
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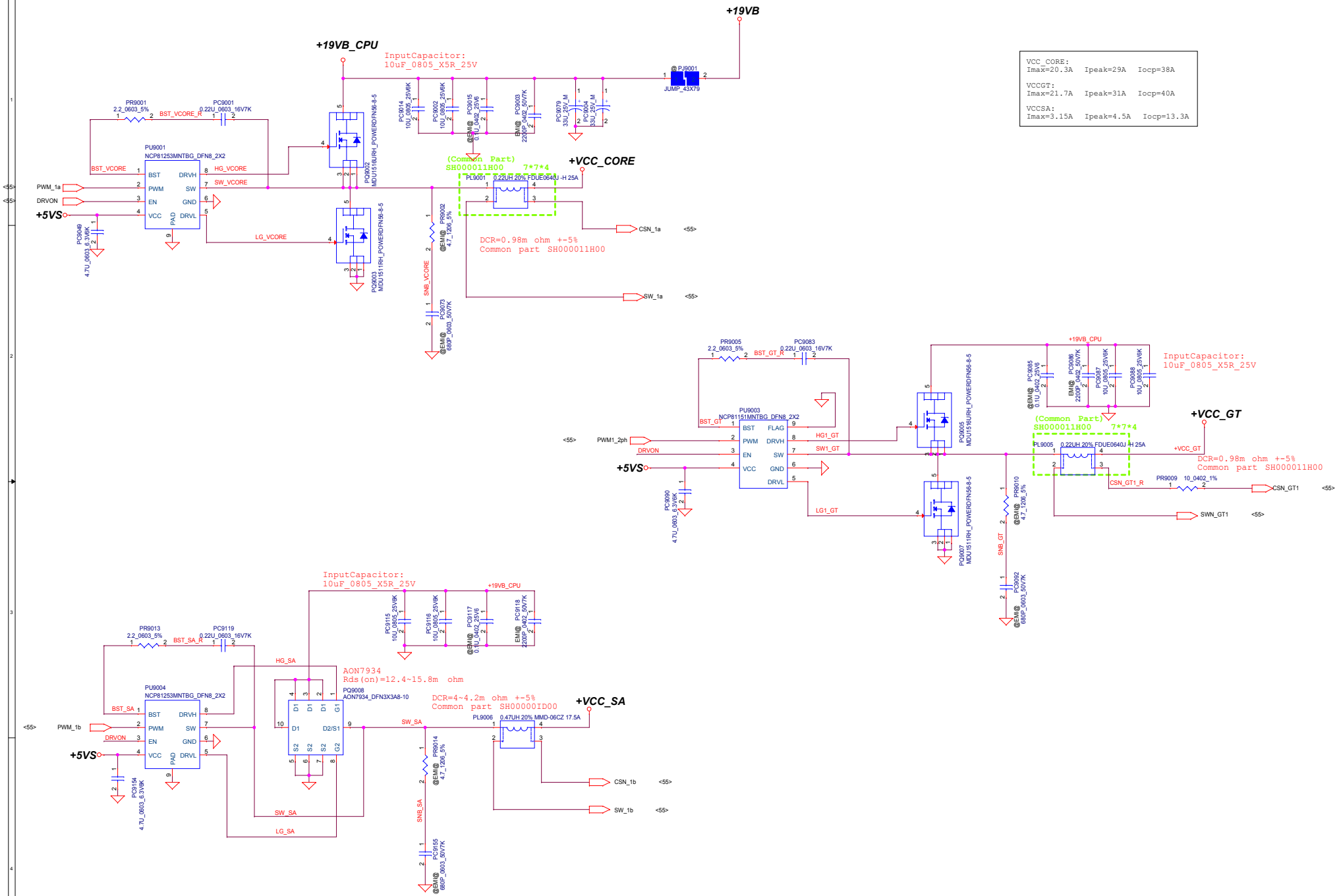

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Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
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Total VCORE Output Capacitor:
2015/07/09
22uF_0603_28PCS
1uF_0201_35PCS
UNPOP 0603_8PCS, 0201_3PCS, 330uF_R9_2PCS

+VCC_CORE

(Common Part)
SGA00009S00

20150709
D2*1 22uF_0603*30 1uF_0201*9
unpop: 22uF_0603*8 1uF_0201*11

+VCC_GT

(Common Part)
SGA00009S00

20140703
22uF_0603*6 1uF_0201*7
unpop: 22uF_0603*6

+VCC_SA

1u_0201 SE00000U200
1u_020 1 SE00000UC00.

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
C	B4DBU M/B LA-D301P	0.1

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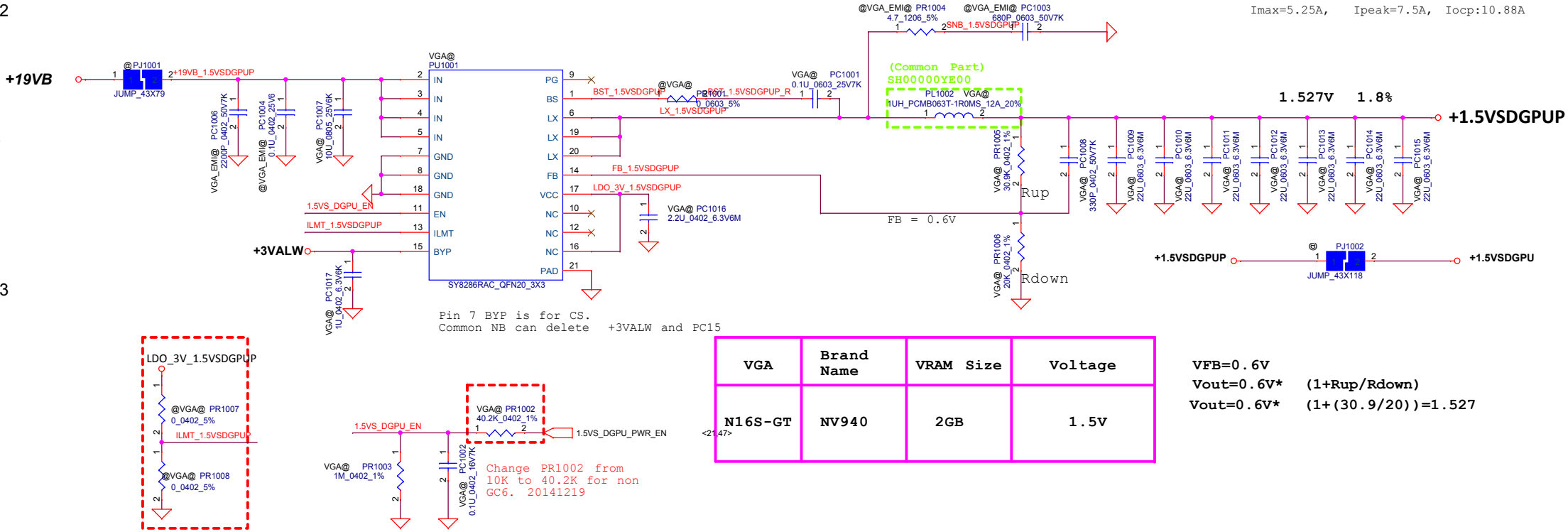

VGA	Brand Name	VRAM Size	Voltage
N16S-GT <21,47>	NV940	2GB	1.5V

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=0.6V* (1+(30.9/20))=1.527

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Compal Electronics, Inc.

Title: 1.5VSDGPUP

Size: A3 | Document Number: B4DBU M/B LA-D301P | Rev: 0.1

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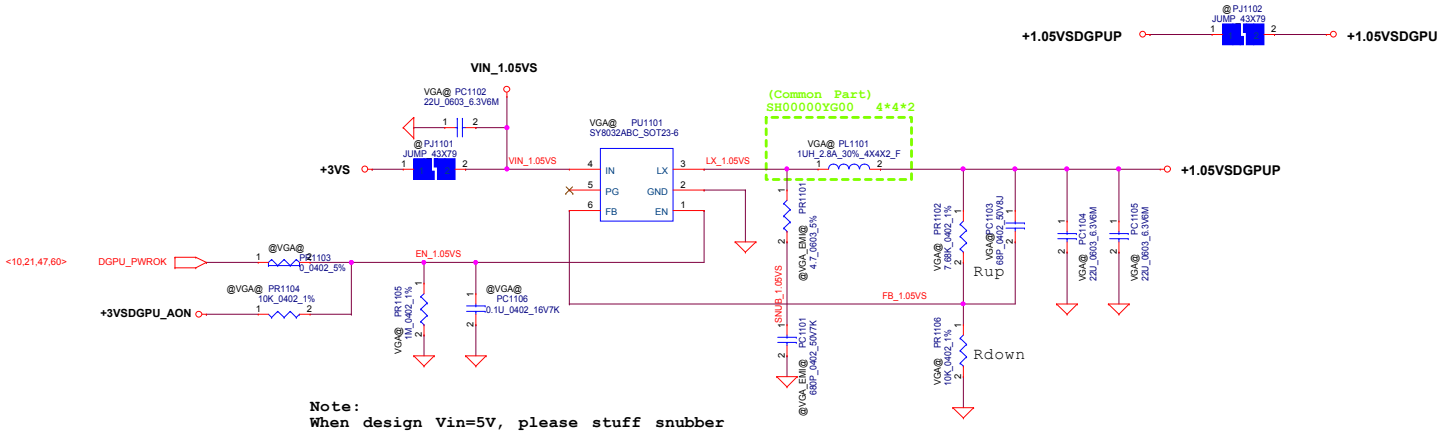
Module model information

SY8032_V2.mdd



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)
=>0.6V*(1+(7.68/10)=1.061 (1.01%)

Imax= 0.77A, Ipeak= 1.1A , Iocp=3.5A

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Issued Date	2014/11/10	Deciphered Date	2016/11/10

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Compal Electronics, Inc.

Title: SY8032

Size: C | Document Number: B4DBU M/B LA-D301P | Rev: 0.1

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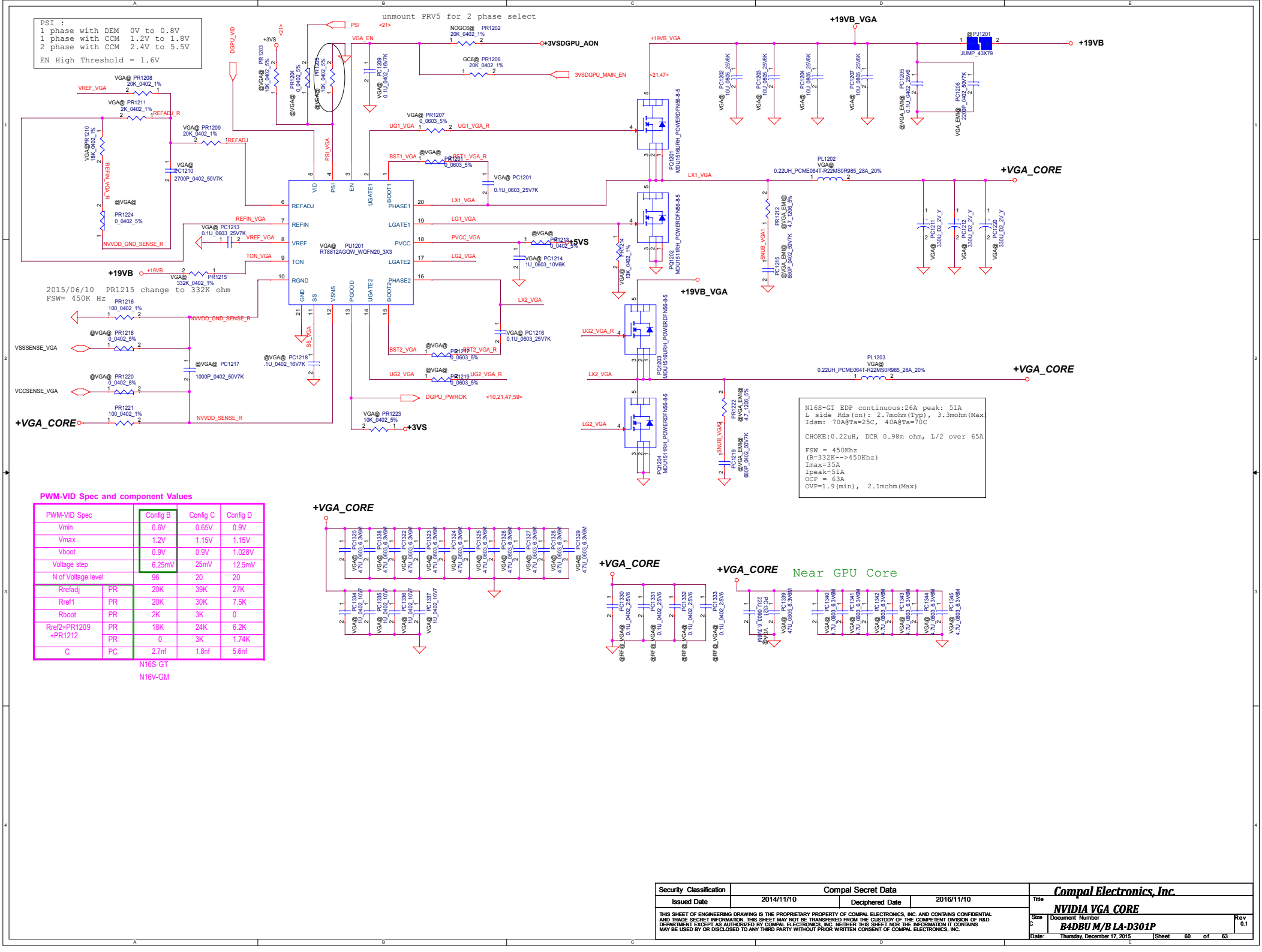

PWM-VID Spec and component Values

PWM-VID Spec		Config B	Config C	Config D
Vmin		0.6V	0.65V	0.9V
Vmax		1.2V	1.15V	1.15V
Vboot		0.9V	0.9V	1.028V
Voltage step		6.25mV	25mV	12.5mV
N of Voltage level		96	20	20
Rrefadj	PR	20K	39K	27K
Rref1	PR	20K	30K	7.5K
Rboot	PR	2K	3K	0
Rref2=PR1209 +PR1212	PR	18K	24K	6.2K
	PR	0	3K	1.74K
C	PC	2.7nf	1.8nf	5.6nf

N16S-GT
N16V-GM

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Compal Electronics, Inc.

Title: NVIDIA VGA CORE

Size	Document Number	Rev
C	B4DBU M/B LA-D301P	0.1

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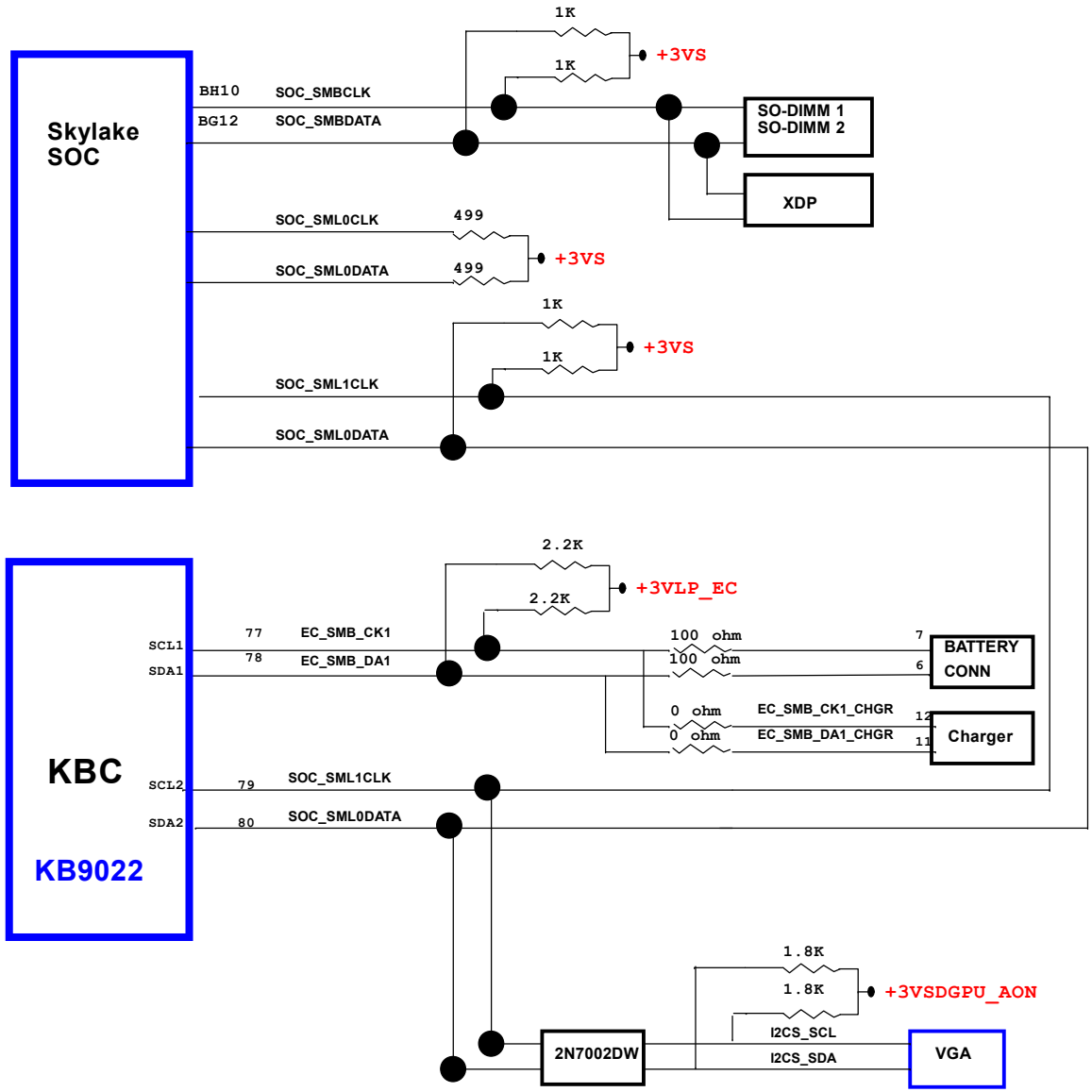

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Compal Electronics, Inc.

Title: SMBUS Routing Table

Size	Document Number	Rev
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Change.	X1 Code : SE158225K80	02	50	PC316 change to SE000006S80	8/25	DVT
02 03 04	Design Change.	ON FAE suggest to modify Parts	02	55 57	PR814 and PR843 change to 806 ohm. PR858 change to 15.8K ohm. PC810 change 3300P. PC818 change to 150P. Add PC 9008, PC9031, and PC9007.	8/25	DVT
05	Design Change.	For Type-C function	03	51	PU402 change to SA00008YM00	10/7	PVT
06 07	Design Change.	Change 0 ohm to short pad.	03		PR1001, PR101, PR1103, PR1201, PR1204, PR1213, PR1217, PR1219, PR1224, PR201, PR315, PR316, PR317, PR333, PR401, PR408, PR501, PR510, PR512, PR602, PR606 PR705, PR804, PR806, PR812, PR813, PR847, PR852, PR864, PR865 change to short pad	10/22	PVT
08							
09							
10							
11							
12							
13							
14							
14							

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EVT->DVT

0810
1. Remove RPC8
2. Change the BOM structure of CD36 and CD34 to @
3. Change UL3's part number to SA000028Y10
4. Change U67's part number to SA00007IO10
5. Add U5004's part number SA00008E710
6. Change U5007's BOM structure to TBT@
7. Change U1's part number to SA00007UJ10
8. Remove U61, C818
9. Change BOM structure of RC62 and RC63 to POP
10. Connect RC18.2 to Codec PIN 31 (for MIC function)
11. Remove RC240
12. Add C5227
13. Add R5251, R5252
14. Change D44's part number to SC300003S00
15. change BOM structure PC@ to @

0812
1. JLID1. 4 Connecto to +3VLP
2. change type C connector's part number to LTCX006Z3BL
3. remove D16

0813
1. change type C connector JUSB2's footprint from lotes_ausb0139-p001a_24 to JAE_DX07S024XJ1_24P-T

0817
1.change back TYPE C connector to SP011504212
2.change D29 and D30's part number to SC300003S00, same as D44
3.remove R630,R631,R633,R665,R667,R668,R669,R671
4.C5126,C5121,C5118,C5117 change to @ for HDMI
5.C5201,C5202,C5197,C5196 change to 0201 for TBT
6.Add C5239 0.1u on +3VS (JFP1) for EMI
7.C480,C633 change to RF@ for RF
8.ADD C5237 68P on +3VS(JTP1) for RF
9.ADD C5238 68P on +3VS(JFP1) for RF
10.ADD C5232 68P on +3VS(JDMIC) for RF
11.ADD C5229, C5230, C5231 0.1u+2200p+68p on +19VB for RF
12.ADD C5235, C5236 68P*2 on +3VS(JKB) FOR RF
13.ADD C5228, R5253 0OHM+22P (RPC9) FOR RF
14.ADD C5233 0.1u on +5VALW(JIO1) for EMI
15.ADD C5240 68P on +5VALW(JIO1) for RF
16.ADD C5241 @RF@ for RF
17.Change C5241's connection to ESPI_CLK_R
18. Change R5173's connection to EC_TBTA_RESET

0818
1. Change C5227 to @
2. Change C633 to @
3. Change C5179~C5182 package to 0201
4. Modify the connection of U26.9(G_INT2)

0819
1. Change package of R630, R631, R633, R665, R667, R668, R669, R671 to short pad
2. Add C5242, C5243, C5244, C5245 for EMI
3. Change package of U5005 to SOP8
4. R1579-->@, R1581-->POP

DVT->PVT

1008
1. C5244, C5243, C5242, C5245 change to EMI@
2. D17, D18, D19, D20, D21, D34, D23, D24 Change to SC40000AT00
3. R443, R444, R445 change to vpro@
4. R4903 change to 15K for DVT Board ID
5. R1579-->@, R1581-->POP
6. R5203-->@, R5173-->POP
7. UL3, U60 Change to SA000079400
8. SW1-->@
9. CL14 change to 0603
10. JREAD1 PIN10's connection from +3VALW to +5VALW
11. CD41, CD42, CD43 change to 0402
12 add 16M BIOS ROM on UC2

1012
1. Connect DET_SIG#_R to UCPU1 pin AY5

1015
1. Change below items to short pad :
RC238,RC245,RC55,RC56,RC12,RC130,RC131,
RC168,RC186,RC188,RC208,RC140,RC143,RC141,
RC192,RC175,RC148,RC173,RC154,RC198,RC209,
RC149,RC176,RC156,RC197,RC161,RC163,RC172,
RC167,RC187,RC162,RC171,RC169,RC164,RC190,
RC152,RD45,RD47,RD46,R550,R549,R23,R5248,
R664,RC229,RC19,RC20,R486,R487,R873,R441,
R442,R661,R5193,R1580,R5210,R5209,R5192,
R5194,R5197,R5198,R4953,R514,R645,
2. Change U5007's part number to SA00008C310

1016
1. Update power schematic 1016

1016a
1. Add R5254, R5255 for Draco_SL reserve

1018
1.Change R23, R5248, RC130, RC131, R486, R487 back to 0ohm resistor

1027
1. Change U67's part number to SA00007IO00
2. SUSCLK R5252 POP->@
3. R5250 TBT@->@TBT@
4. Add LAN Chip UL1 R3 Part Number SA000081G50
5. Replace SP050006F00 to SP050006B10

PVT->PreMP
1209
1. Change R1581 to @
2. Change R1579 to TBT@
3. Change U60 to @
4. Change UC3's to 3VM
5. BOARD ID Change to PreMP Value
6. Add RC248, RC249

1216
1. R525 changes to 10K
2. C5232 changes to 0.1U
3. PIN UC1.R10 connect to +3VALW_PRIM with 2.2K resistor
4. add U5008 for 3VALW and 3VALWP

1217
1. U5009.4 Connect to 3VLAWP
2. Add Q2021, R5258, R5259 for Discharge
3. Q2021.3 Connect to SUSP#

1218
1. Add C5251 for EC_RSMRST#

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Title: HW PIR

Size	Document Number	Rev
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