GA-MA74GMT-S2

Revision : 1.3

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Title: COVER SHEET		
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Model Name:GA-MA74GMT-S2

Component value change history

Version:1.3

P-Code: U98102-0

Date	Change Item	Reason
2009.10.23	0.1 New BOM Release.	Modify from 9MMA74G2H-00-40F
2009.10.23	0.1 New BOM Release.	Remove HDMI function
2009.11.13	1.0A BOM Release	Modify 5VDual protect schematic
2010.04.16	1.3A BOM Release	Modify Fuse F1,F2 to 3.5A for F_USB port 3倍力

Circuit or PCB layout change for next version

Date	Change Item	Reason
2009.10.22	0.1 Gerber out	Modify from GA-MA74GM-S2H 4.01 (share MA74GMT-S2H PCB)
2009.11.12	Rev1.0 Gerber-out	Modify 5VDual protect schematic
2010.04.15	Rev1.3 Gerber-out	Modify silk-screen for F_USB port 3倍力

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Title: BOM & PCB HISTORY

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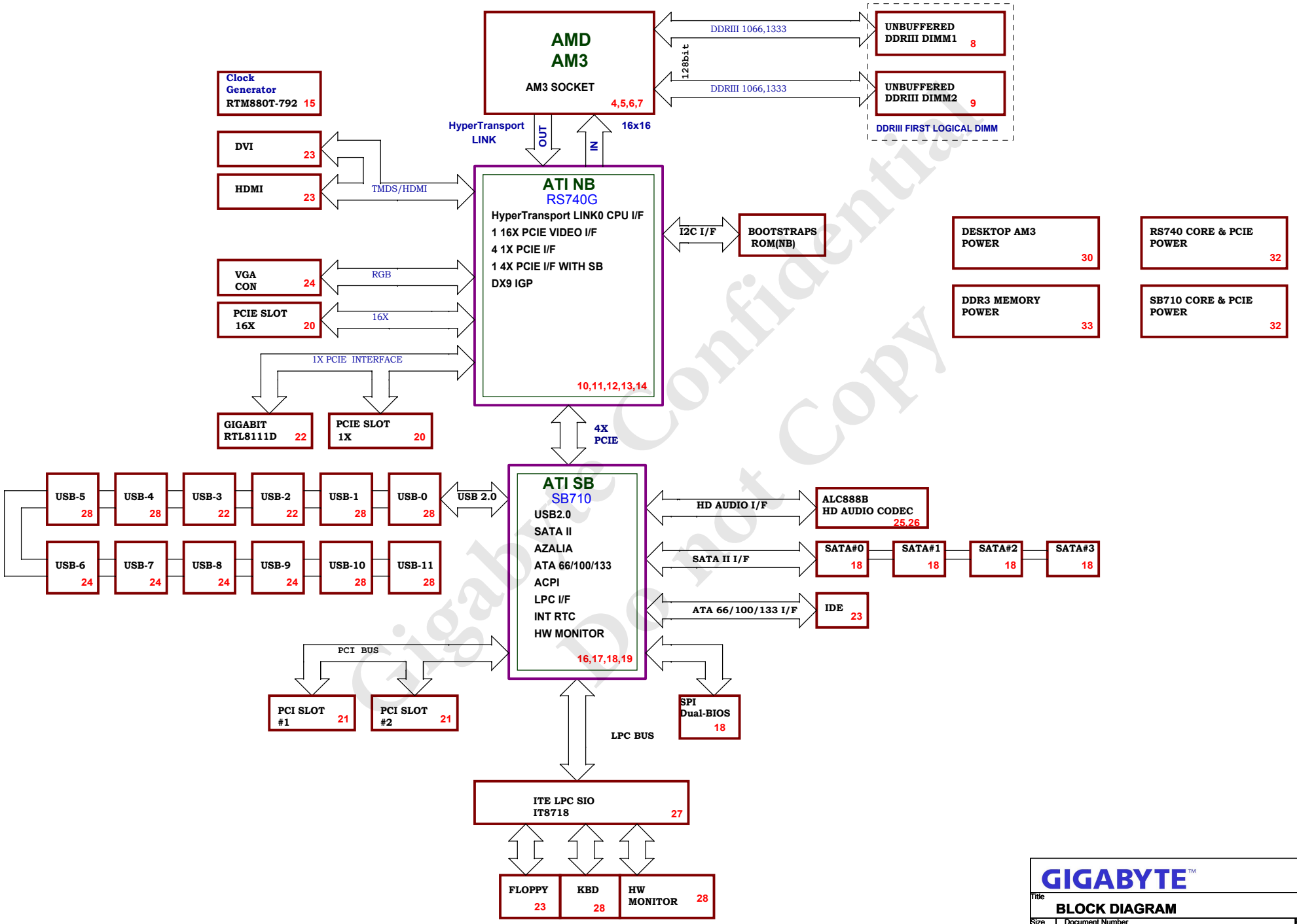
Date: Thursday, April 15, 2010 | Sheet 2 of 33

RS740 CUSTOMER DESKTOP REFERENCE DESIGN



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Title	BLOCK DIAGRAM	
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L0_CADIN_L[0..15]
L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15]
L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15]
L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15]
L0_CADOUT_H[0..15] 10

VCC_SB
GND
R4 49.9/4/1 L0_CTLIN_H1
R6 49.9/4/1 L0_CTLIN_L1

M2CPUA

HYPERTRANSPORT

10 L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 10
10 L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 10
10 L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 10
10 L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 10
10 L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 10
10 L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 10
10 L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 10
10 L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 10
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

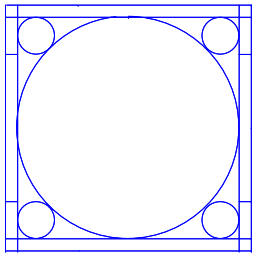
CPU-SK/941AM3/S/GF/[10SC1-A01941-01R]

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPU

AM2RM/PP/BU/PB/[12KRC-04K812-11R]



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Title	CPU HYPER TRANSPORT	
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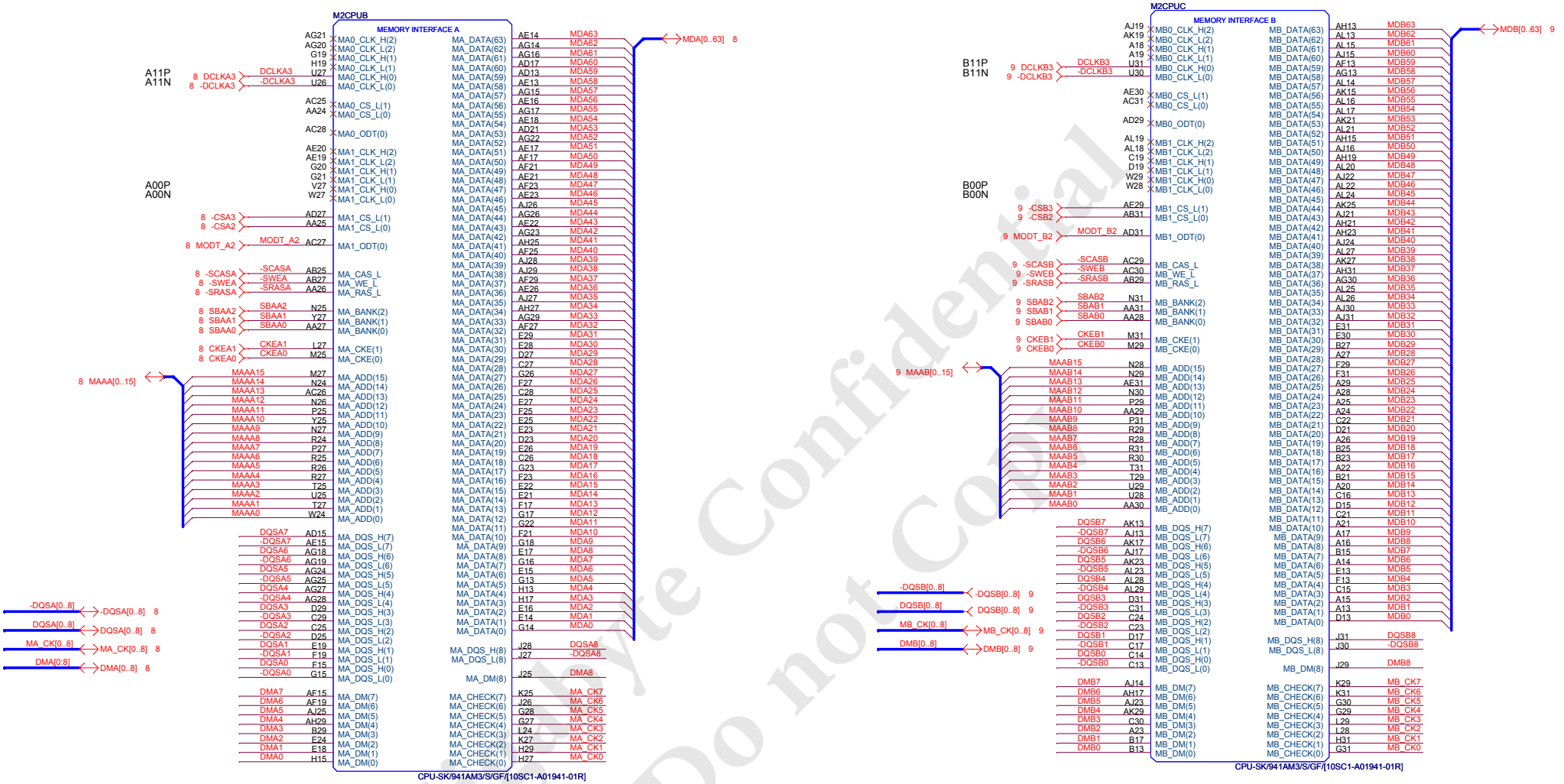

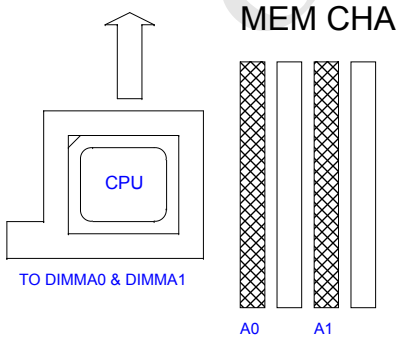

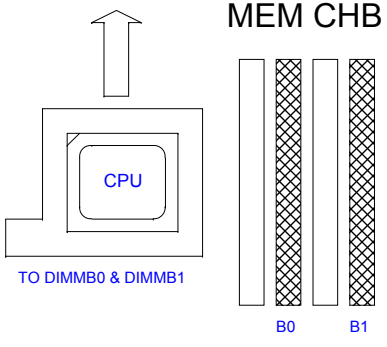

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Title: CPU DDRIII MEMORY		
Size: Custom	Document Number: GA-MA74GMT-S2	Rev: 1.3
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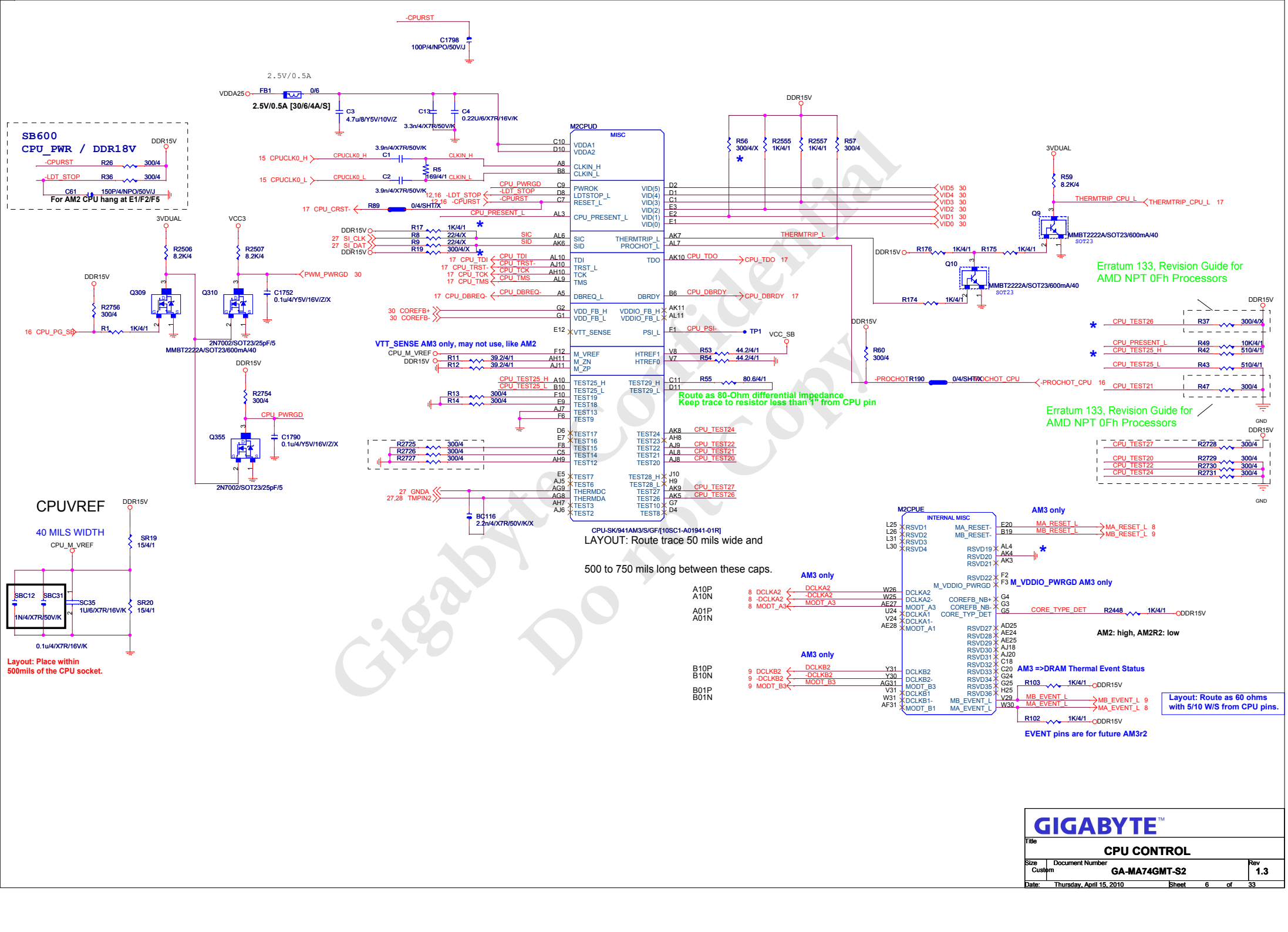

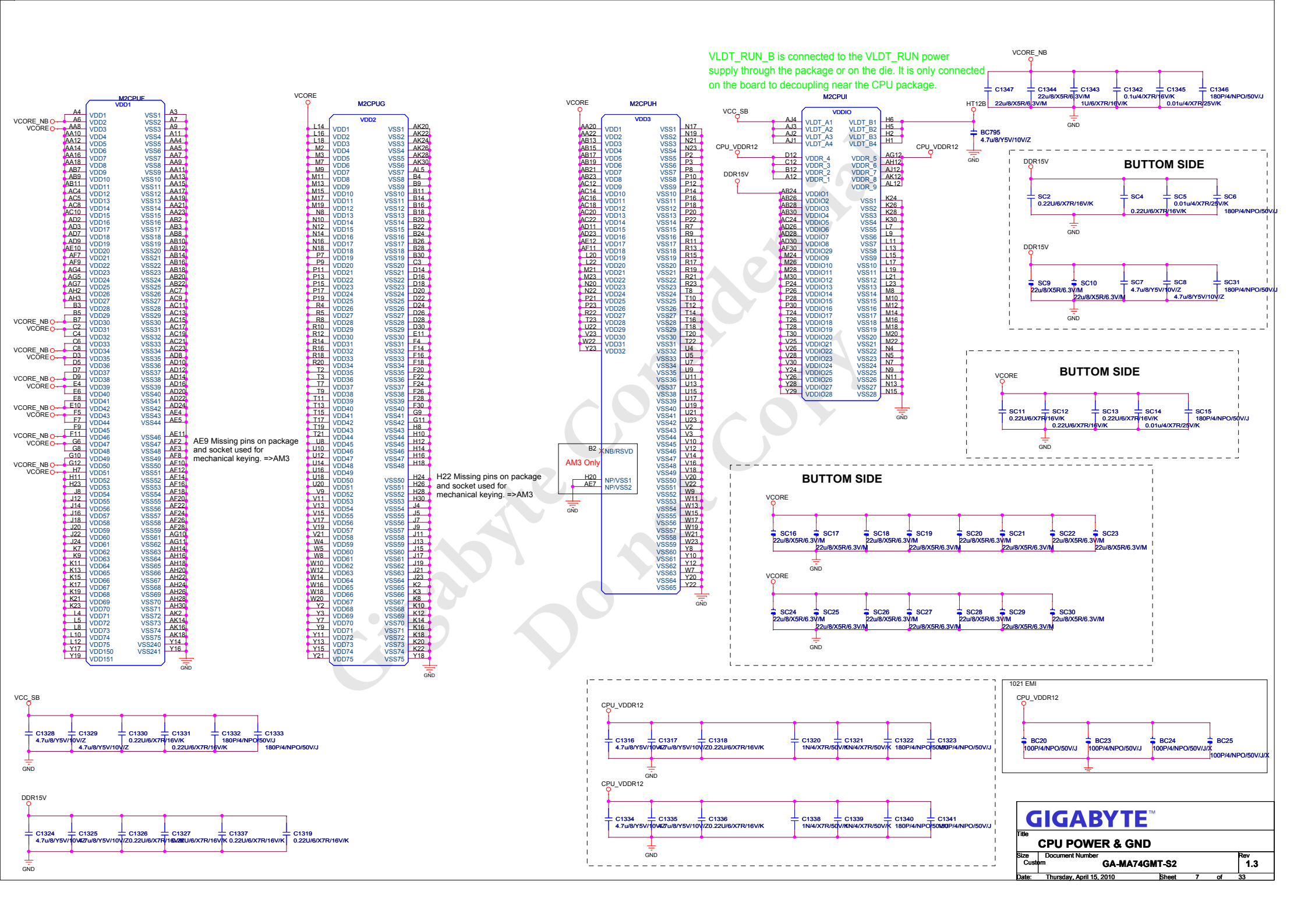
M2CPUF
VDD1
M2CPUG
VDD2
M2CPUH
VDD3
M2CPUI
VDDIO
VCORE_NB
VCORE
CPU_VDDR12
VCC_SB
DDR15V
GND
AE9 Missing pins on package and socket used for mechanical keying. =>AM3
H22 Missing pins on package and socket used for mechanical keying. =>AM3
B2 NB/RSVD
AM3 Only
H20 NP/VSS1
AE7 NP/VSS2
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.
HT12B
BC795
4.7u/8/Y5V/10V/Z
C1347
C1344
22u/8/X5R/6.3V/M
C1343
1U/6/X7R/16V/K
C1342
0.1u/4/X7R/16V/K
C1345
0.01u/4/X7R/25V/K
C1346
180P/4/NPO/50V/J
BUTTOM SIDE
SC2
0.22U/6/X7R/16V/K
SC4
SC5
0.01u/4/X7R/25V/K
SC6
0.22U/6/X7R/16V/K
SC9
22u/8/X5R/6.3V/M
SC10
SC7
4.7u/8/Y5V/10V/Z
SC8
SC31
SC11
SC12
SC13
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C1335
C1336
C1338
C1339
C1340
C1341
1021 EMI
BC20
100P/4/NPO/50V/J
BC23
BC24
BC25
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CPU POWER & GND
GA-MA74GMT-S2
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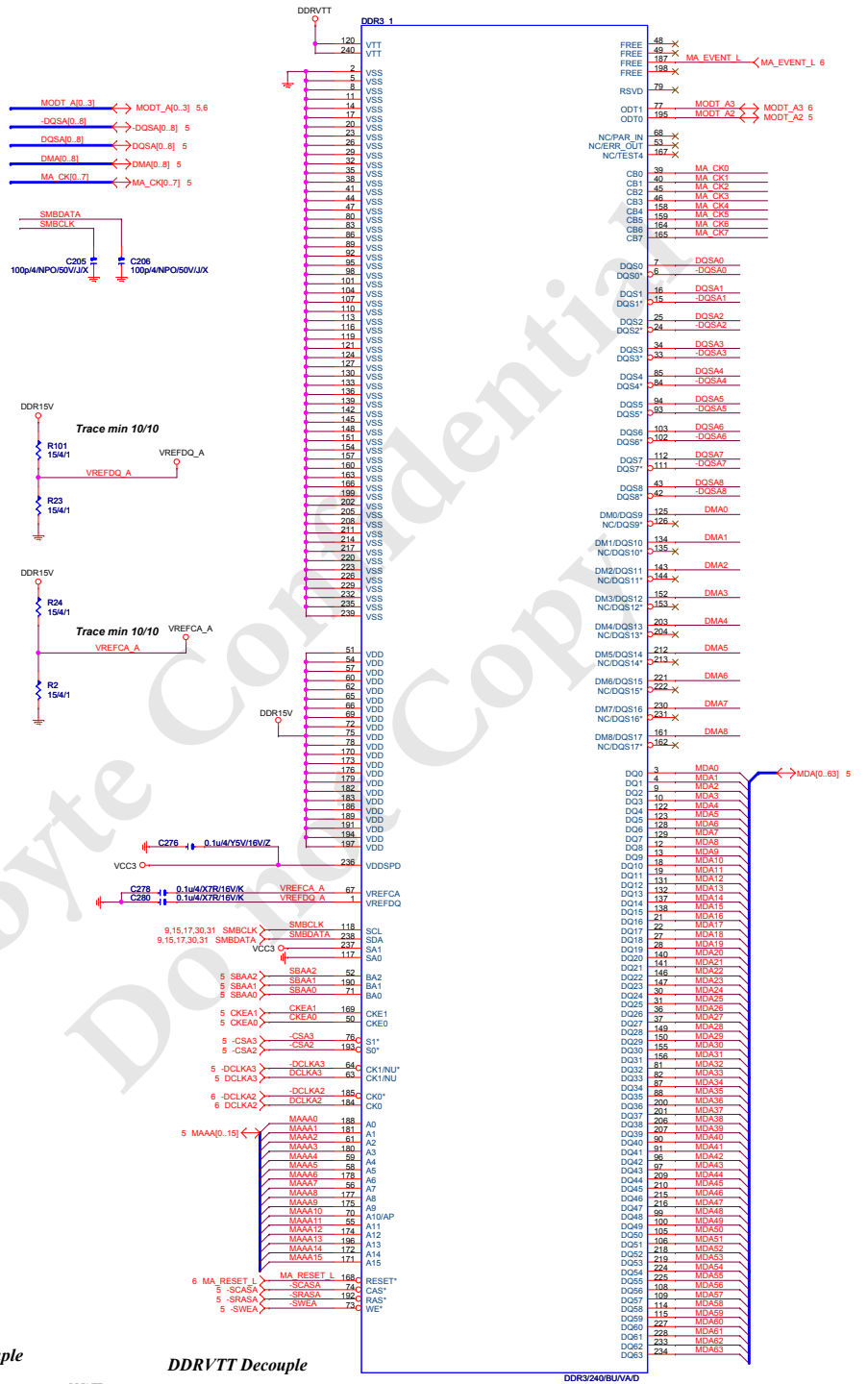
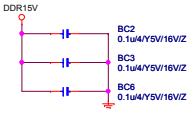
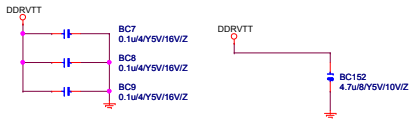
Gigabyte Confidential
Do not Copy



DDR15V Decouple



DDRVTT Decouple



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Title	DDR III CHANNEL A	
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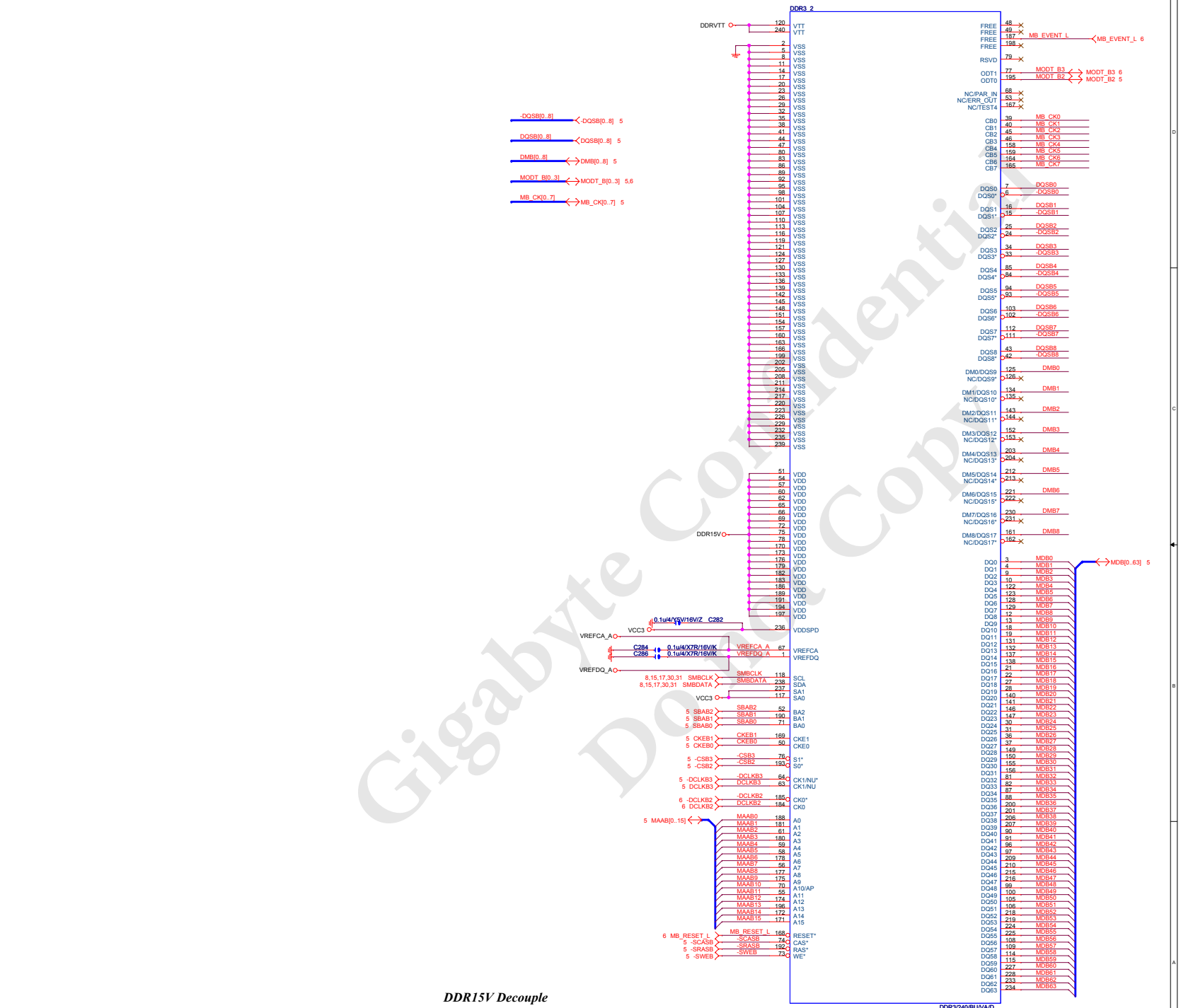
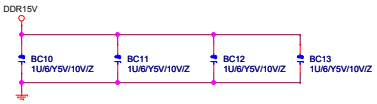
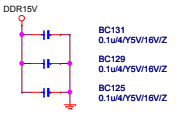


DDR15V Decouple





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Title	DDR III CHANNEL B	
Size: Custom	Document Number: GA-MA74GMT-S2	Rev: 1.3
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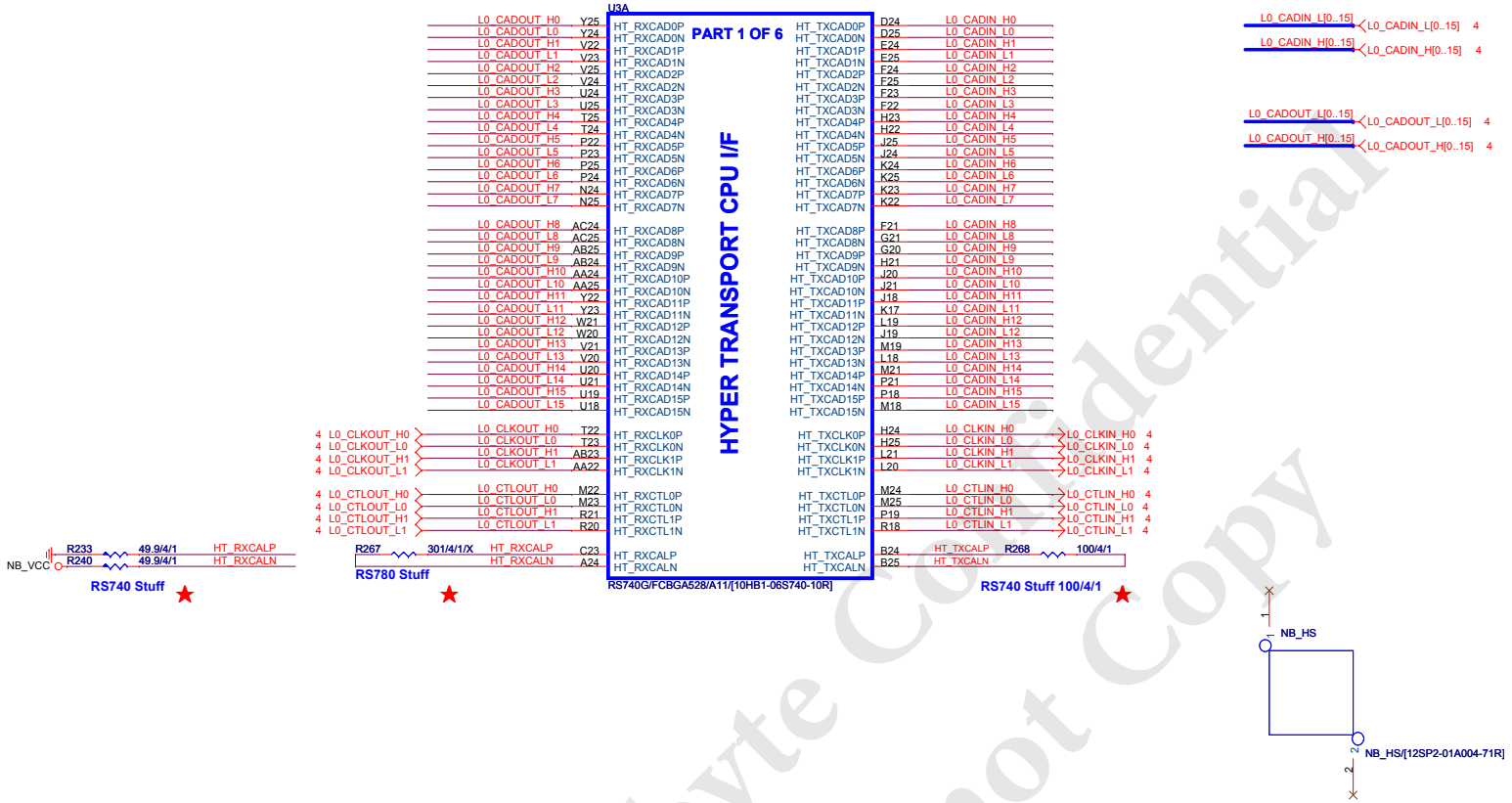

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Title: RS740 HT-LINK I/F

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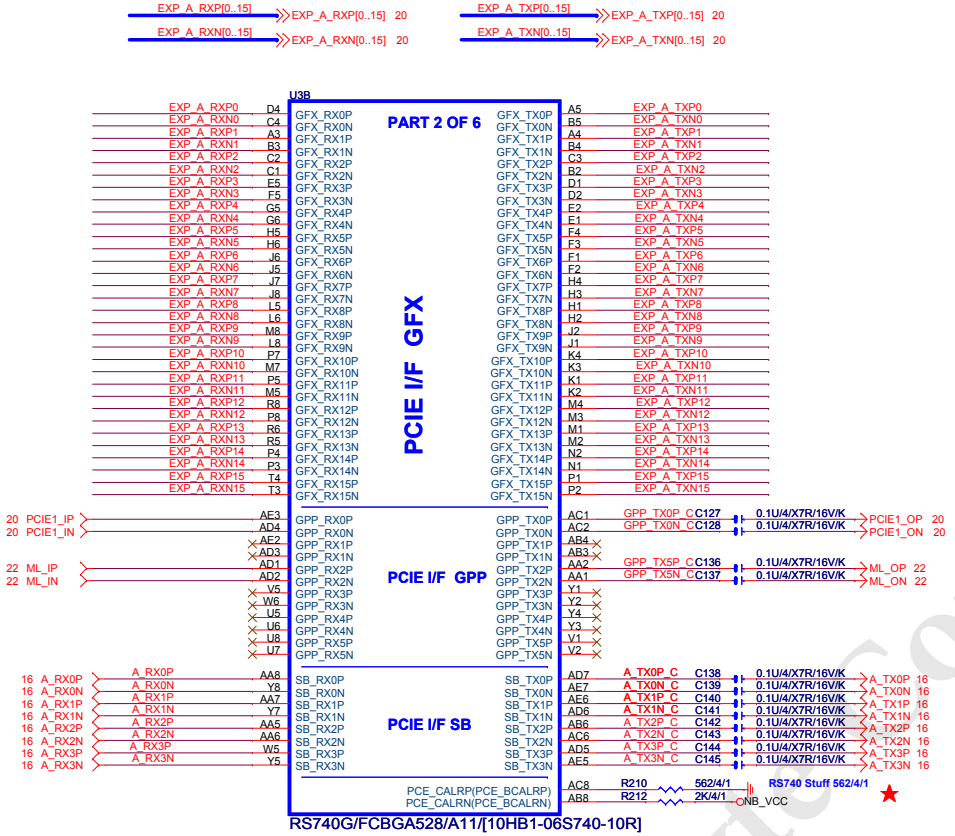

RS740G/FCBGA528/A11/[10HB1-06S740-10R]

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Title: RS740 PCIE I/F

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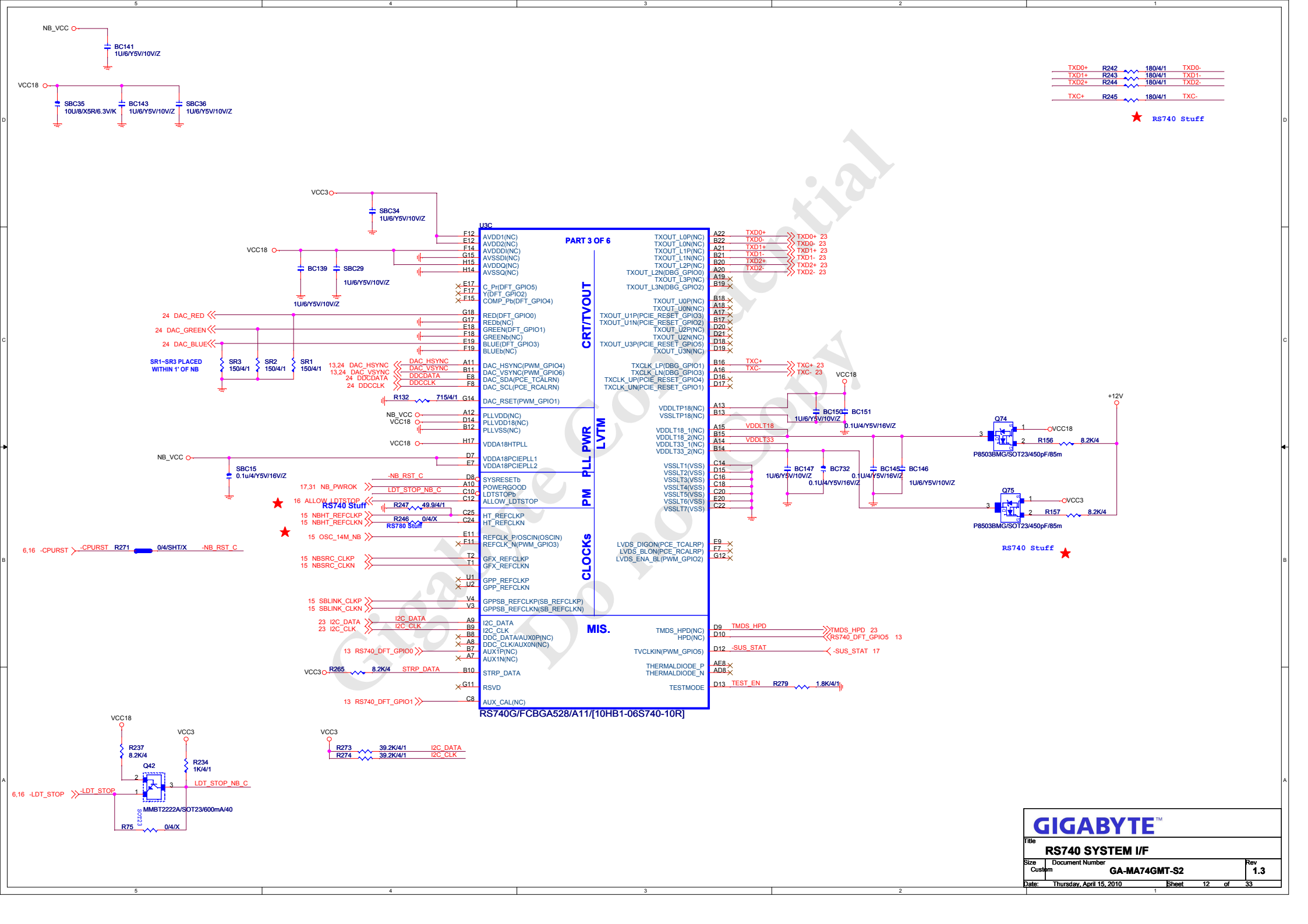

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Title: RS740 SYSTEM I/F		
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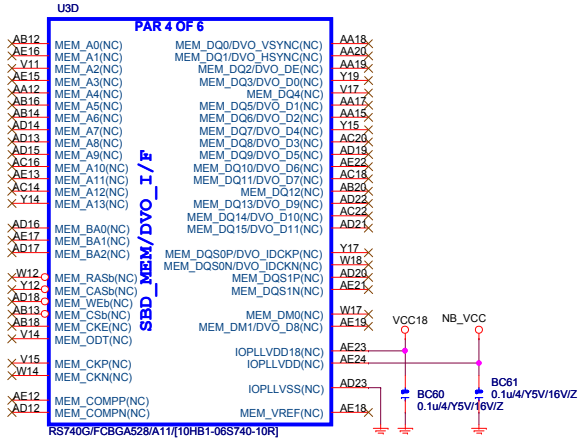
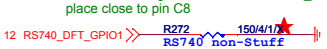
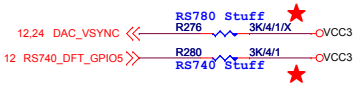


RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8



Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly



Note: for RX780, change following pull-down resistor to 3K accordingly

R912 (RX780_DFT_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly

R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)

Note: for RX780, change following pull-down resistor to 3K accordingly

R219 (RX780_DFT_GPIO0)

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#
```

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

```
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable  (RS740/RS780); Disable(RX780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
```

RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])

```
These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E)   default
110: 4-0-0-0-0   Config A
101: 4-4-0-0-0   Config B
100: 4-2-2-0-0   Config C
011: 4-2-1-1-0   Config D
010: 4-1-1-1-1   Config E
others: register defined (default to Config E)
```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

```
111: 1-1-1-1-1-1-1   Mode L   default
110: 1-1-1-1-1-1-1   Mode L
101: 2-0-2-0-2-0     Mode C2
100: 2-0-2-0-1-1     Mode K
011: 2-0-1-1-1-1     Mode E
010: 1-1-1-1-1-1     Mode L
001: 4-0-0-0-1-1     Mode C
000: 4-0-0-0-2-0     Mode B
```

RS780: STRAP_PCIE_GPP_CFG[2:0] (configure thru register setting)

```
1-1-1-1-1-1   Mode L   default
1-1-1-1-1-1   Mode L
2-0-2-0-2-0   Mode C2
2-0-2-0-1-1   Mode K
2-0-1-1-1-1   Mode E
1-1-1-1-1-1   Mode L
4-0-0-0-1-1   Mode C
4-0-0-0-2-0   Mode B
```

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

```
Enables Side port memory
1.  Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740:  pin DFT_GPIO0
RS780:  pin HSYNC
RX780:  Not Appicable
```

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

```
Enables Test debug bus
using PCIE bus
1.  Disable (can be enabled
     thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register
            setting only
RS740: Not supported
```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Title: RS740 STRAP		
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RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

U3F — PART 6/6 — GROUND

RS740G/FCBGA528/A11/[10HB1-06S740-10R]

Please use 1mm pad size, place all ELT test pads on bottom side only

U3E — PART 5/6 — POWER

RS740G/FCBGA528/A11/[10HB1-06S740-10R]

Title	RS740 POWER & GND						
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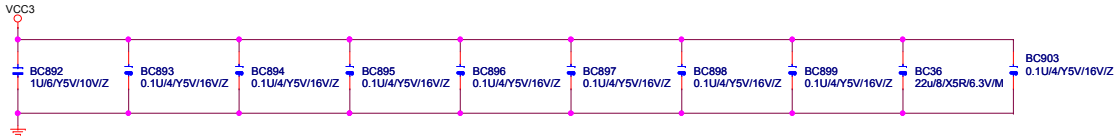


1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

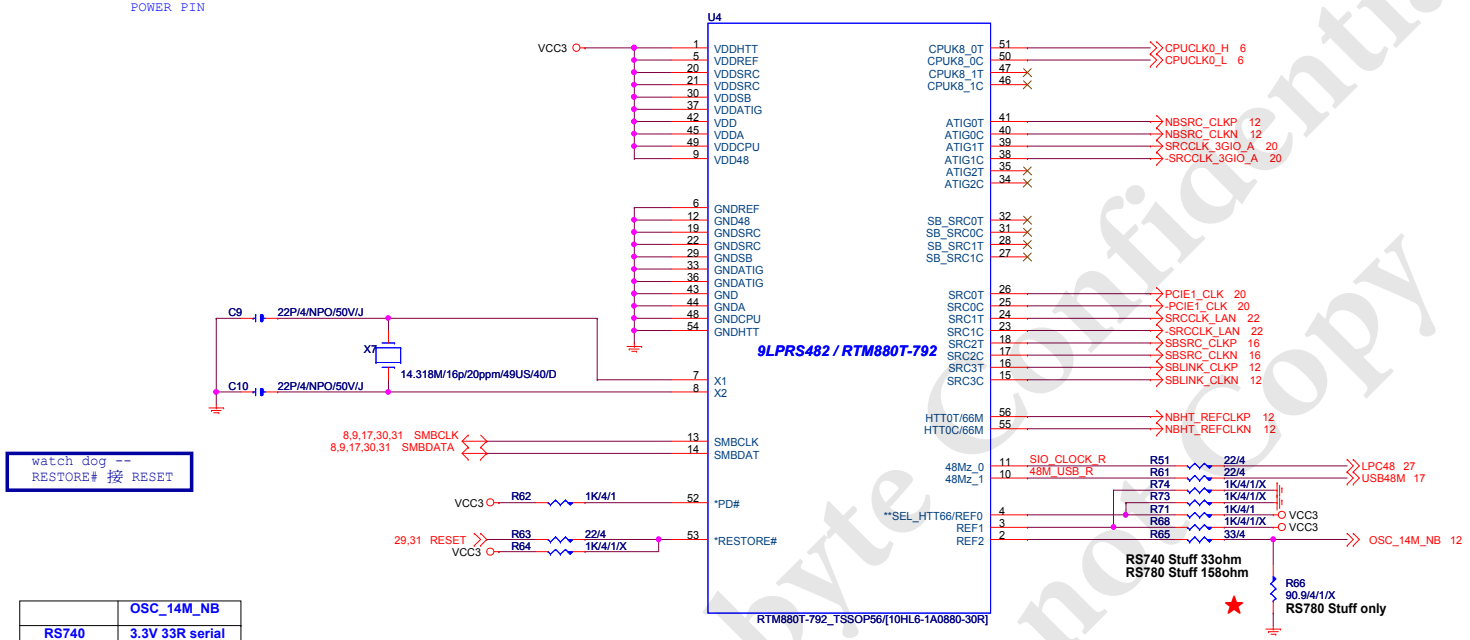
2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



watch dog --
RESTORE# 接 RESET

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

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Title: RTM880T-792

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PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

S.B HEATSINK

SB_HS

SB_HS/[12SP2-030005-42R_12SP2-030005-43R]

U2A

SB700

Part 1 of 5

A_RST#

PCIE_TX0P PCIE_TX0N PCIE_TX1P PCIE_TX1N PCIE_TX2P PCIE_TX2N PCIE_TX3P PCIE_TX3N

PCIE_RX0P PCIE_RX0N PCIE_RX1P PCIE_RX1N PCIE_RX2P PCIE_RX2N PCIE_RX3P PCIE_RX3N

PCIE_CALRP PCIE_CALRN

PCIE_PVDD PCIE_PVSS

PCIE_RCLKP/NB_LNK_CLKP PCIE_RCLKN/NB_LNK_CLKN

NB_DISP_CLKP NB_DISP_CLKN

NB_HT_CLKP NB_HT_CLKN

CPU_HT_CLKP CPU_HT_CLKN

SLT_GFX_CLKP SLT_GFX_CLKN

GPP_CLK0P GPP_CLK0N

GPP_CLK1P GPP_CLK1N

GPP_CLK2P GPP_CLK2N

GPP_CLK3P GPP_CLK3N

25M_48M_66M_OSC

25M_X1

25M_X2

PCI EXPRESS INTERFACE

PCI CLKS

PCICLK0 PCICLK1 PCICLK2 PCICLK3 PCICLK4 PCICLK5/GPIO41

PCIRST#

PCI INTERFACE

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

CBE0# CBE1# CBE2# CBE3# FRAME# DEVSEL# IRDY# TRDY# PAR STOP# PERR# SERR# REQ0# REQ1# REQ2# REQ3#/GPIO70 REQ4#/GPIO71 GNT0# GNT1# GNT2# GNT3#/GPIO72 GNT4#/GPIO73 CLKRUN# LOCK# INTE#/GPIO33 INTF#/GPIO34 INTG#/GPIO35 INTH#/GPIO36

CLOCK GENERATOR

RTC XTAL

X1 X2

LPC

LPCCLK0 LPCCLK1 LAD0 LAD1 LAD2 LAD3 LFRAME# LDRQ0# LDRQ1#/GNT5#/GPIO68 BMREQ#/REQ5#/GPIO65 SERIRQ

CPU

ALLOW_LDTSTP PROCHOT# LDT_PG LDT_STP# LDT_RST#

RTC

RTCCLK INTRUDER_ALERT# VBAT

SB710/FCBGA528/A14/[10HB1-06B710-11R]

EMI 20071107

C159 1n/4/X7R/50V/K

BC815 1U/6/Y5V/10V/Z

BC816 10U/8/X5R/6.3V/K

BC21 0.1U/4/X7R/16V/K

PCLK2 R127 8.2K/4/X R126 8.2K/4

PCLK3 R125 8.2K/4/X R124 8.2K/4

	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

LPC_CLK0 R121 8.2K/4

LPC_CLK1 R115 8.2K/4

BIOS after boot setting EC AOD-ACC

	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED AOD Extreme	CLKGEN ENABLED
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT

RTC_XI RTC_XO R166 20M/4 X4 32.768K/12.5p/20ppm/TF38/35K/D C93 18P/4/NPO/50V/J C92 18P/4/NPO/50V/J

X4 SHW/D0.64*5.08*6.74

VCC18 R169 8.2K/4

ALLOW_LDTSTOP -PROCHOT_CPU CPU_PG_SB -LDT_STOP -CPURST

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

20mil 20mil 20mil

3VDUAL Q4 BAT54C/SOT23/200mA R163 1K/4/1 RTCVDD BC783 0.1U/4/X7R/16V/K BC22 1U/6/Y5V/10V/Z

VBAT_2 RB 1K/4/1

BAT BAT-SK/BK/P/S/D/SN CR2032 BAT CR2032

CLR_CMOS RTCVDD PH/1*2/BK/2.54/VA/D

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

-PCI_CLKRUN R172 8.2K/4/X VCC3

RTC_CLK R171 8.2K/4 3VDUAL

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Title: ATI SB710 PCIE/PCI/CPU/LPC

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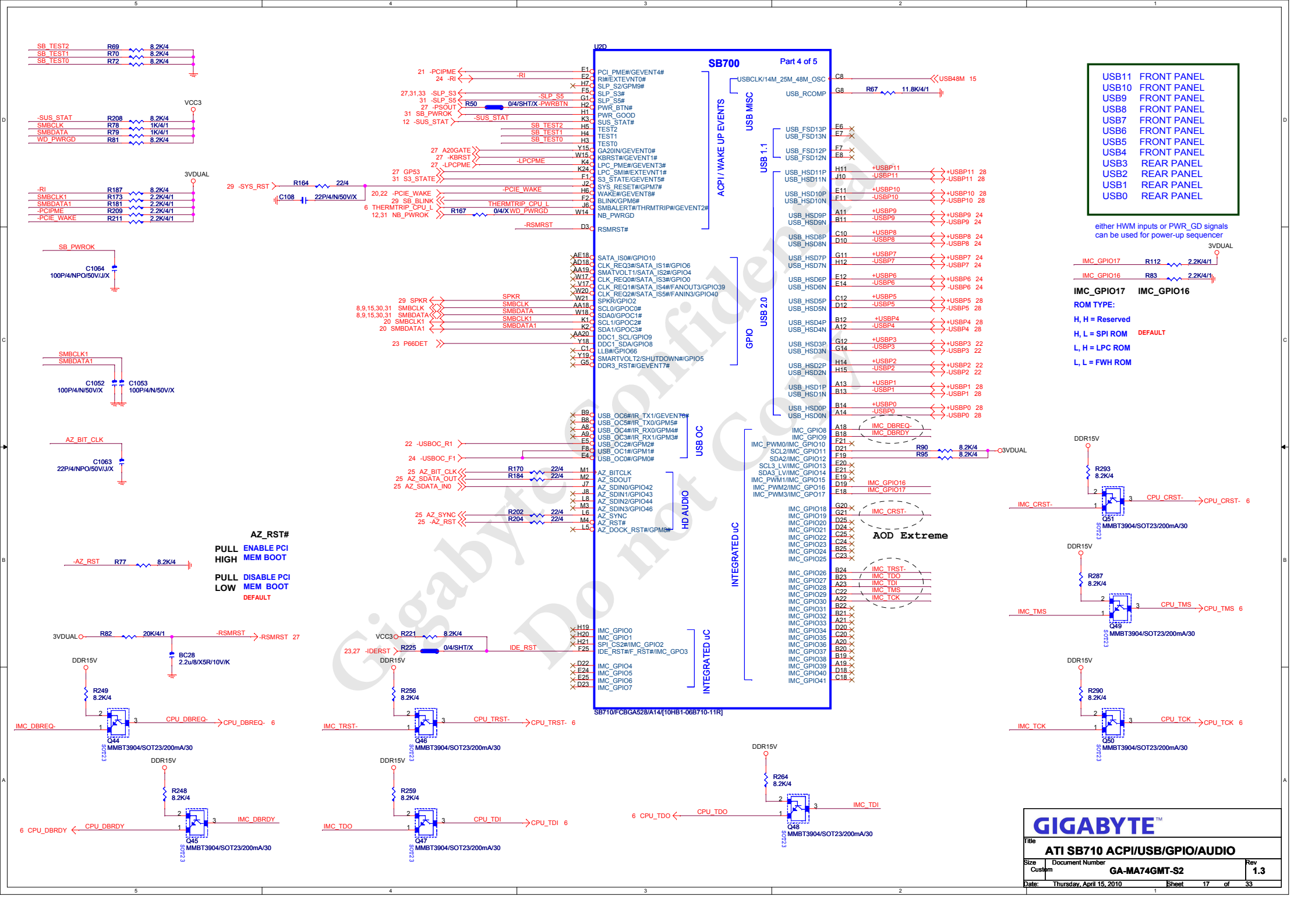
SB700
Part 4 of 5
U2D
SB710/FCBGA528/A14/[10HB1-06B710-11R]
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
INTEGRATED uC
AOD Extreme
USB11 FRONT PANEL
USB10 FRONT PANEL
USB9 FRONT PANEL
USB8 FRONT PANEL
USB7 FRONT PANEL
USB6 FRONT PANEL
USB5 FRONT PANEL
USB4 FRONT PANEL
USB3 REAR PANEL
USB2 REAR PANEL
USB1 REAR PANEL
USB0 REAR PANEL
either HWM inputs or PWR_GD signals can be used for power-up sequencer
IMC_GPIO17 IMC_GPIO16
ROM TYPE:
H, H = Reserved
H, L = SPI ROM DEFAULT
L, H = LPC ROM
L, L = FWH ROM
AZ_RST#
PULL HIGH ENABLE PCI MEM BOOT
PULL LOW DISABLE PCI MEM BOOT DEFAULT
MMBT3904/SOT23/200mA/30
Q44
Q45
Q46
Q47
Q48
Q49
Q50
Q51
GIGABYTE
ATI SB710 ACPI/USB/GPIO/AUDIO
GA-MA74GMT-S2
1.3
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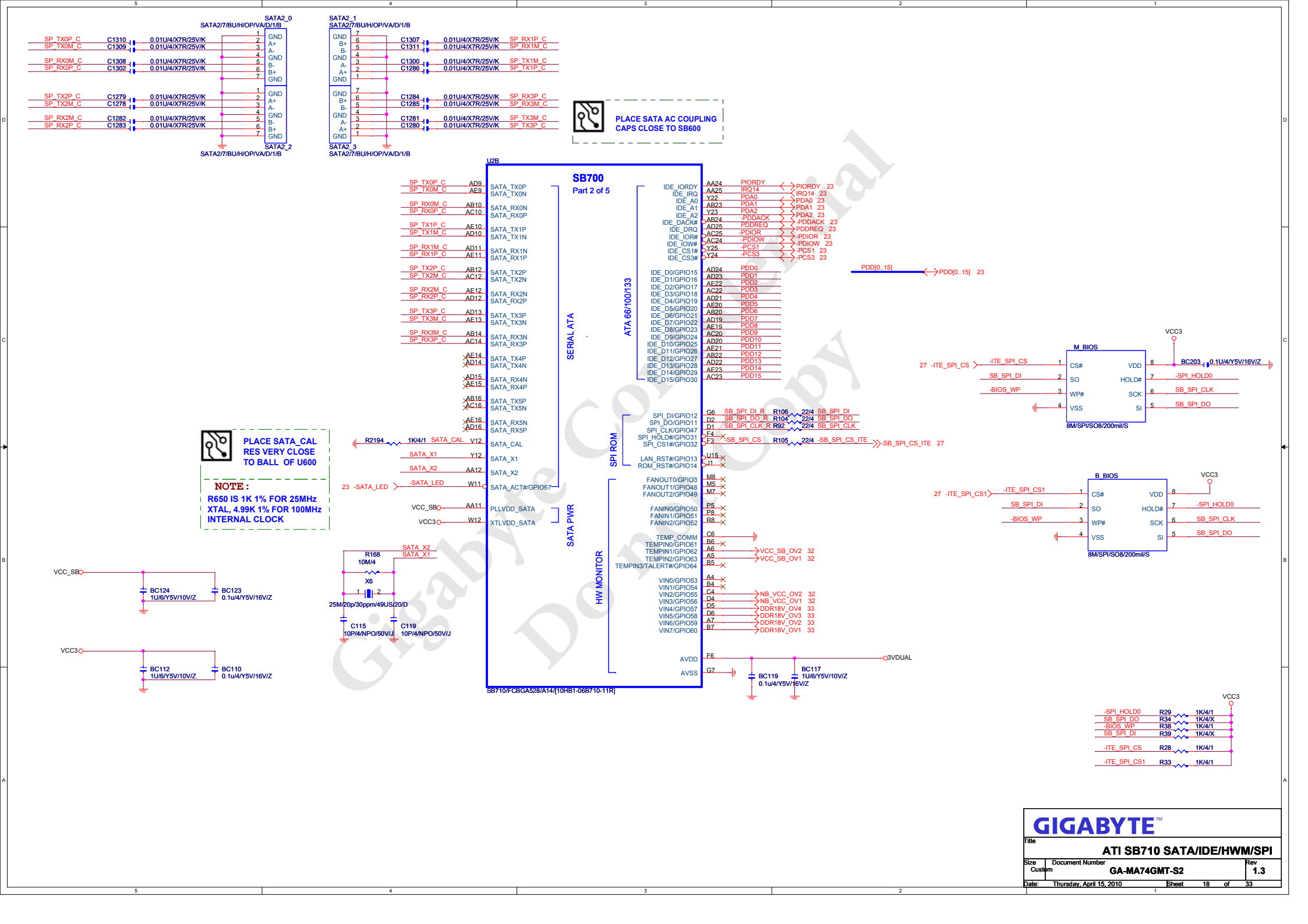
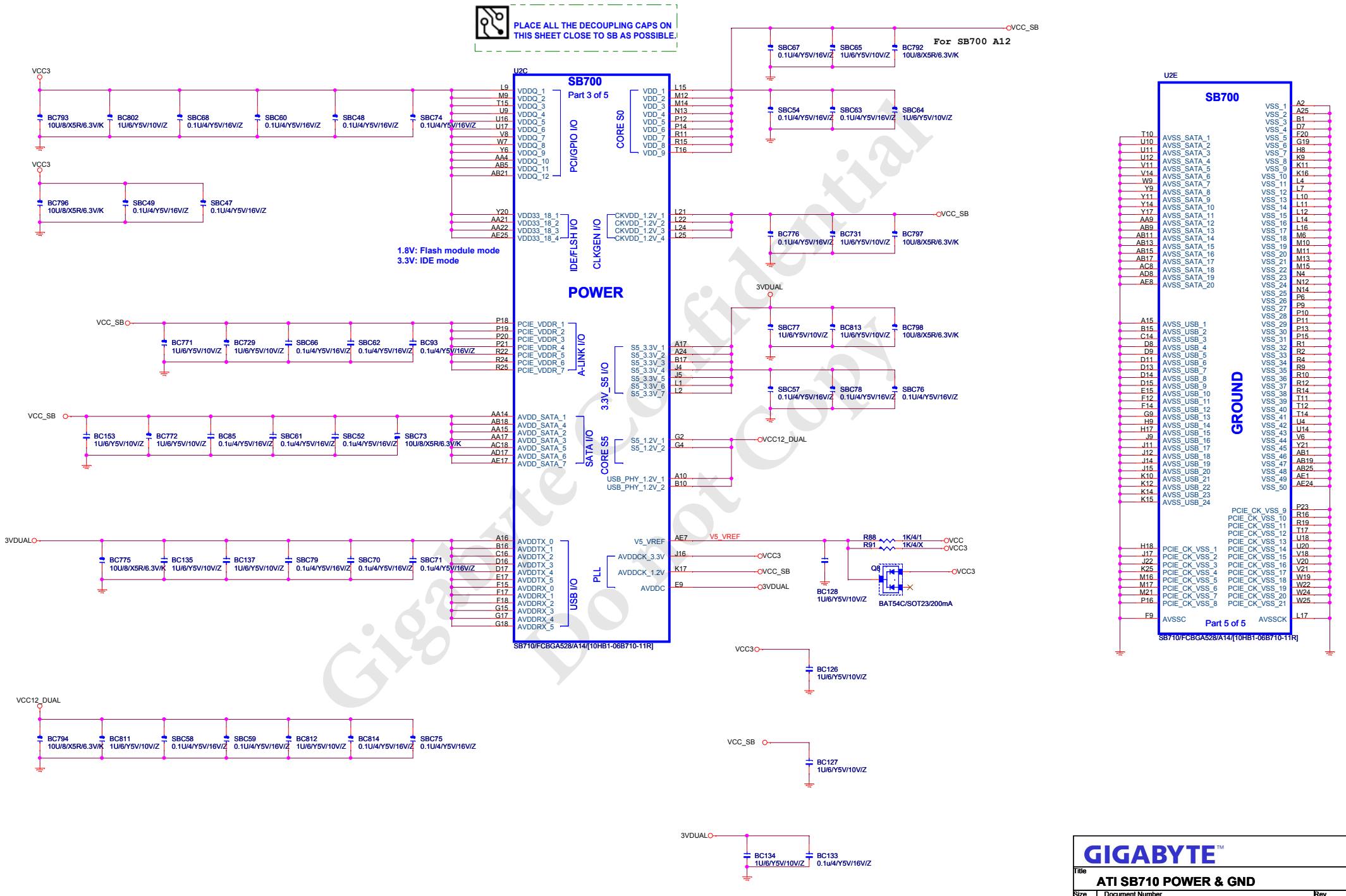
Do not Copy





Title	ATI SB710 POWER & GND
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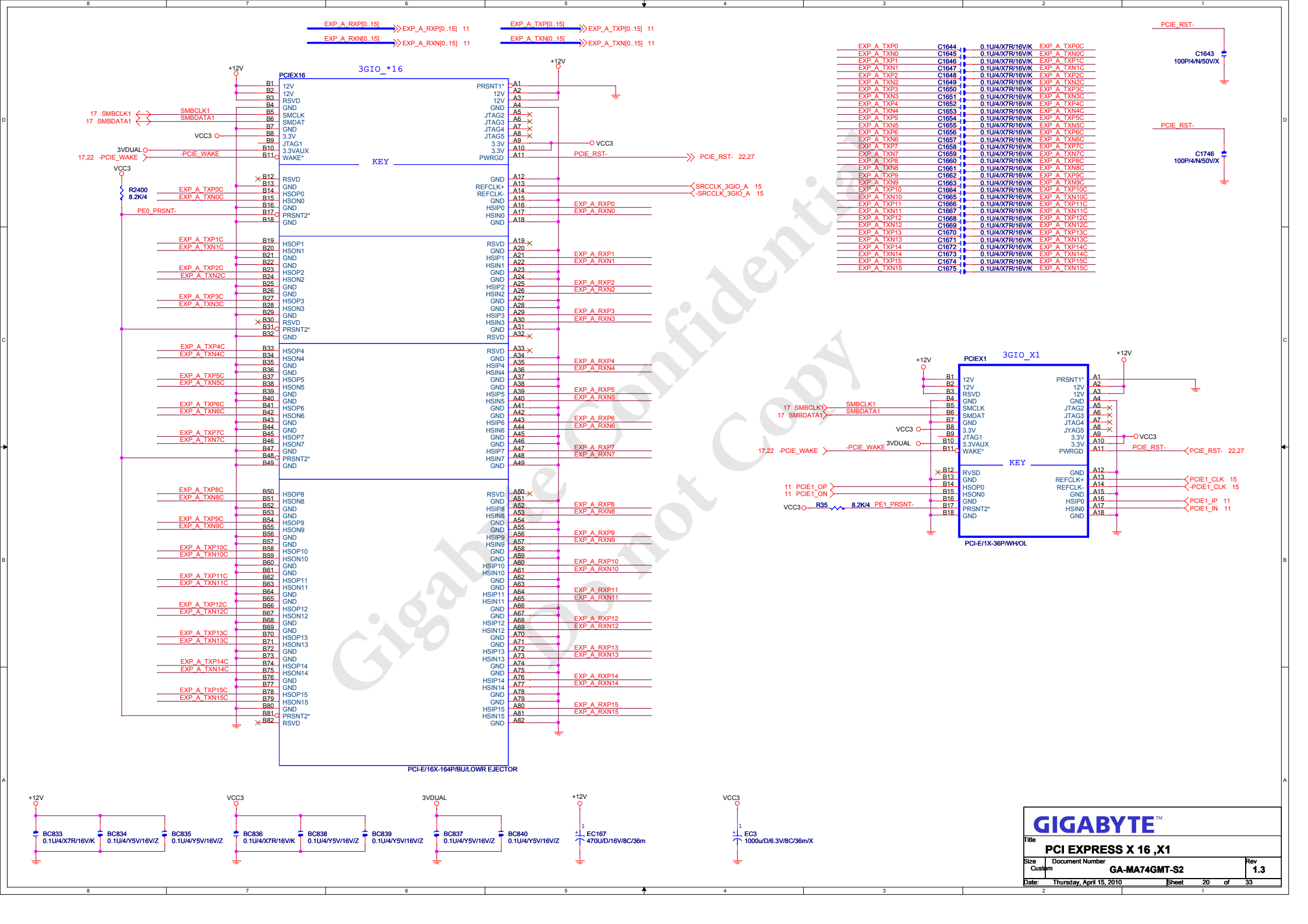

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Title: PCI EXPRESS X 16 ,X1

Size	Document Number	Rev
Custom	GA-MA74GMT-S2	1.3

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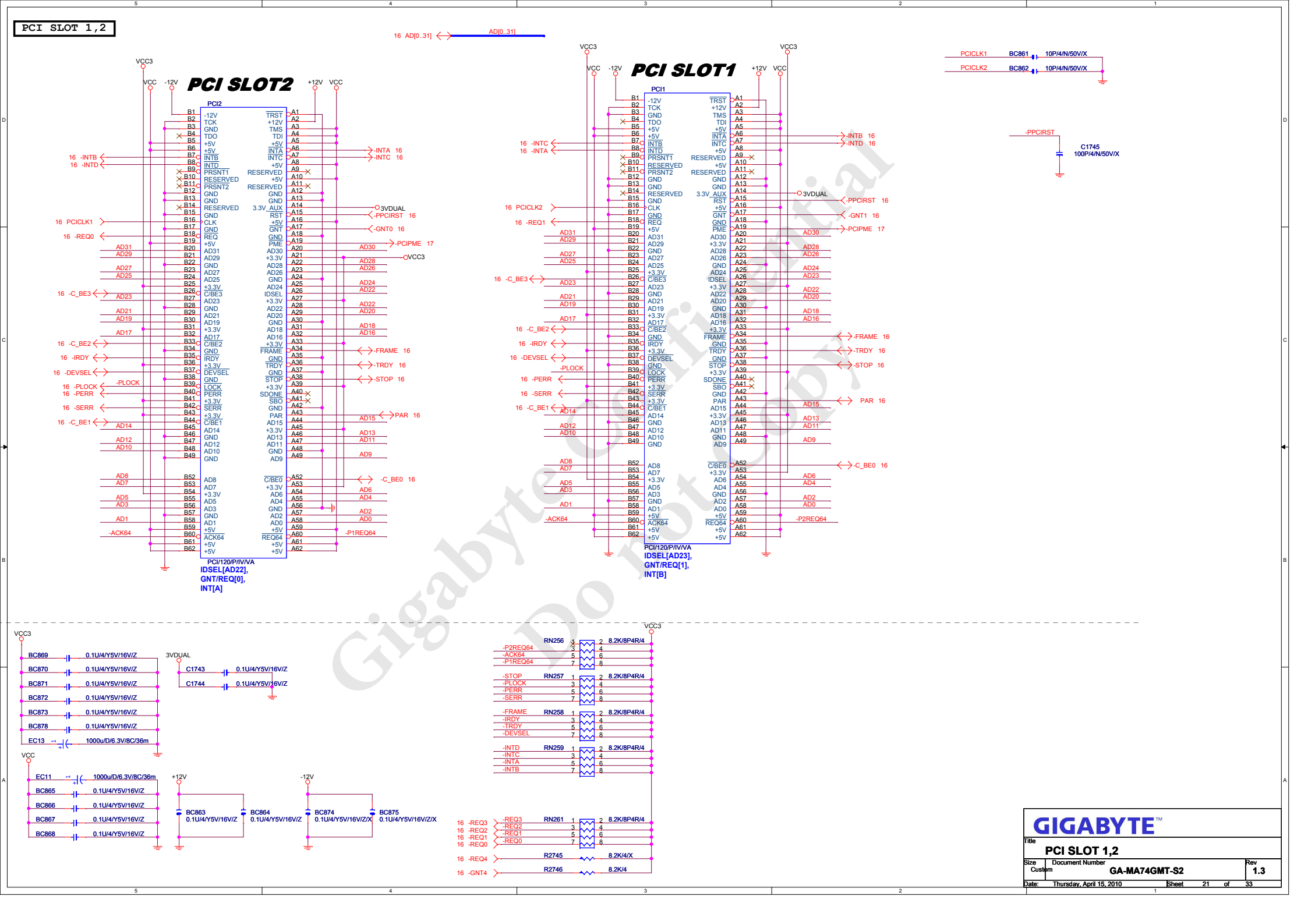
PCI SLOT 1,2



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Title	PCI SLOT 1,2	
Size: Custom	Document Number: GA-MA74GMT-S2	Rev: 1.3
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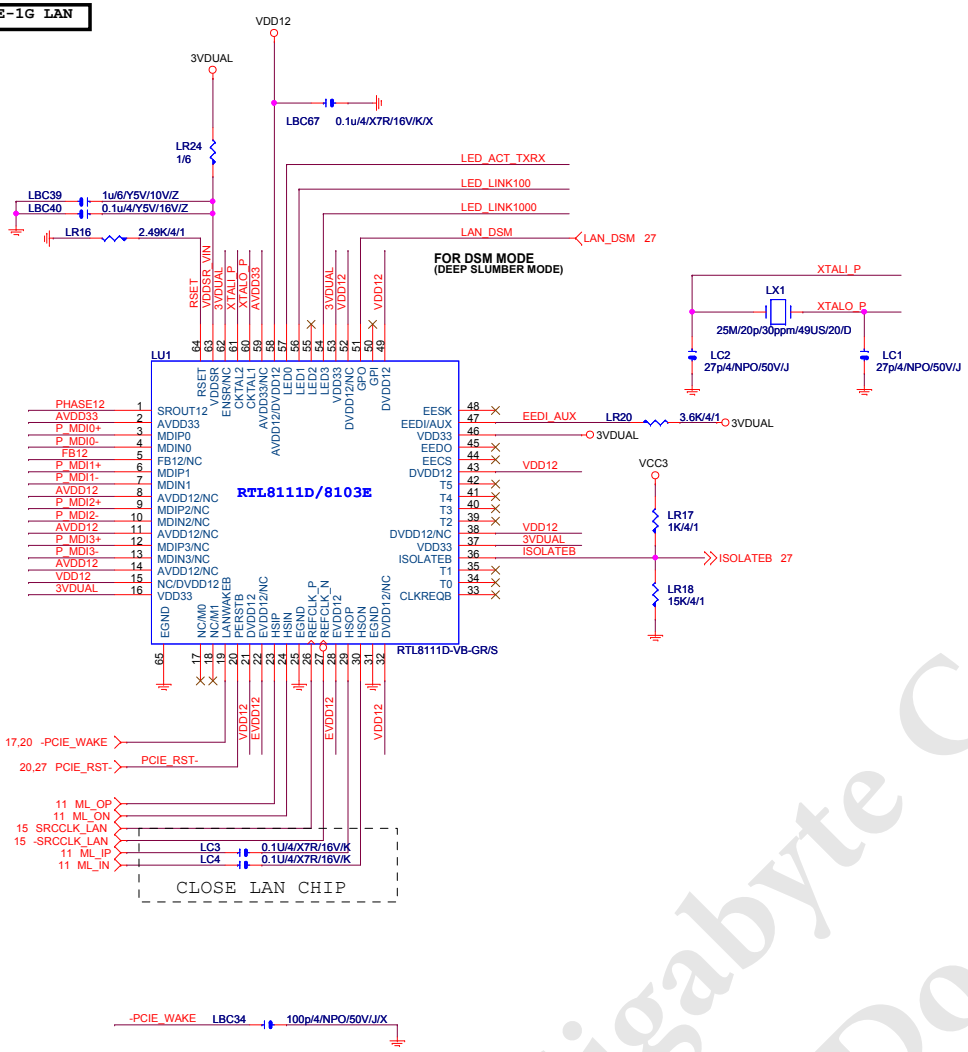
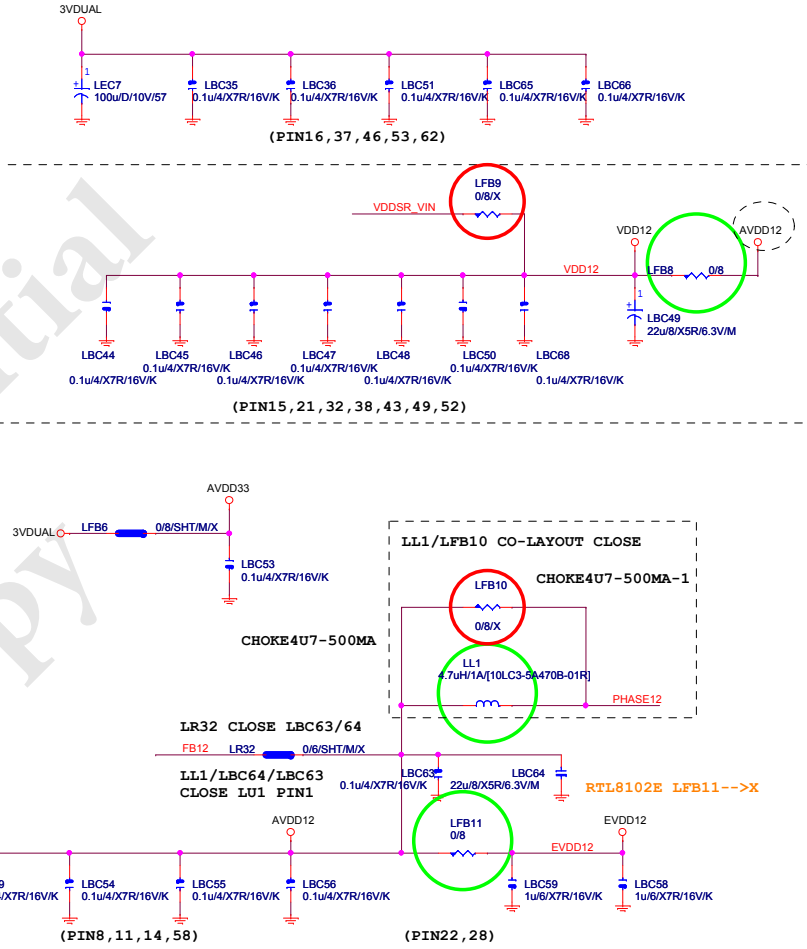
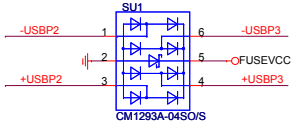
PCIE-1G LAN

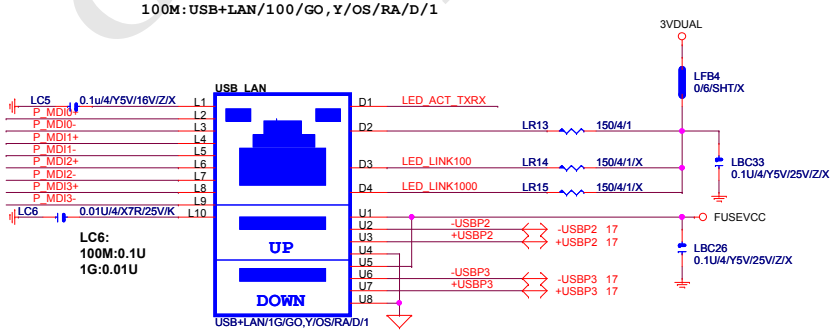




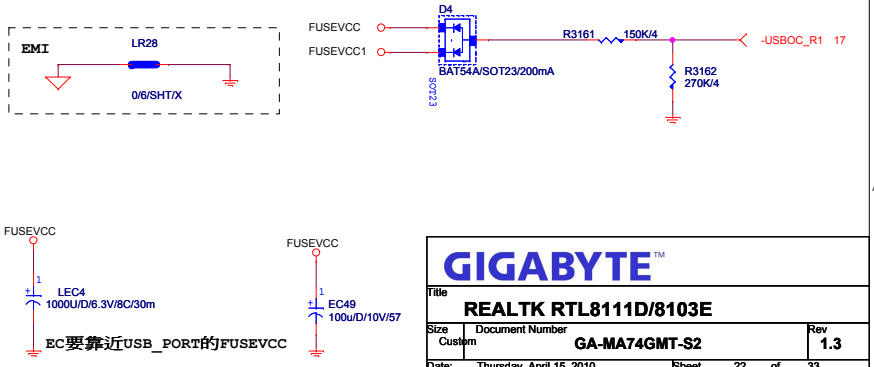
USB_LAN CONNECTOR

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1





USB_LAN



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Title	REALTK RTL8111D/8103E	
Size: Custom	Document Number: GA-MA74GMT-S2	Rev: 1.3
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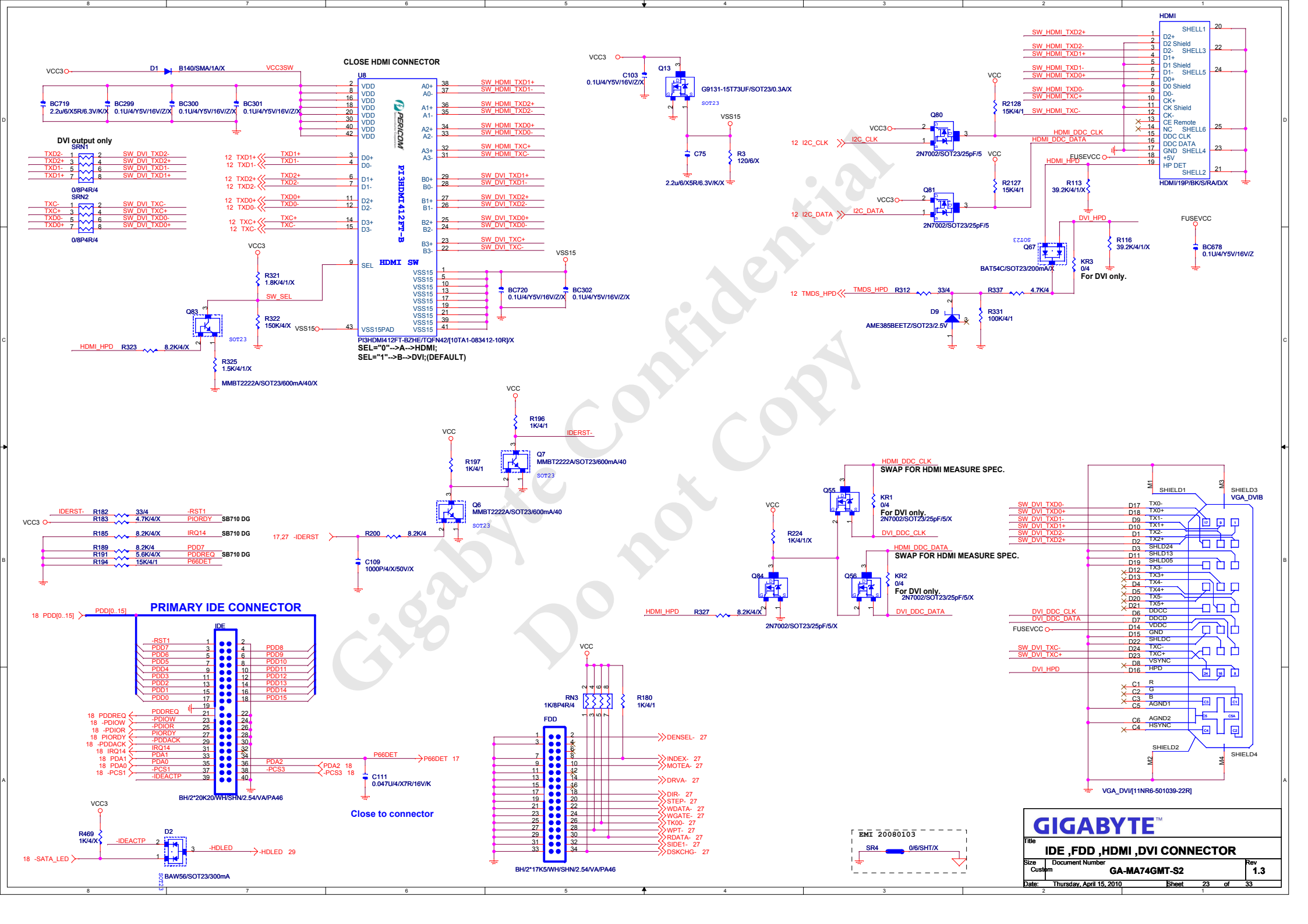

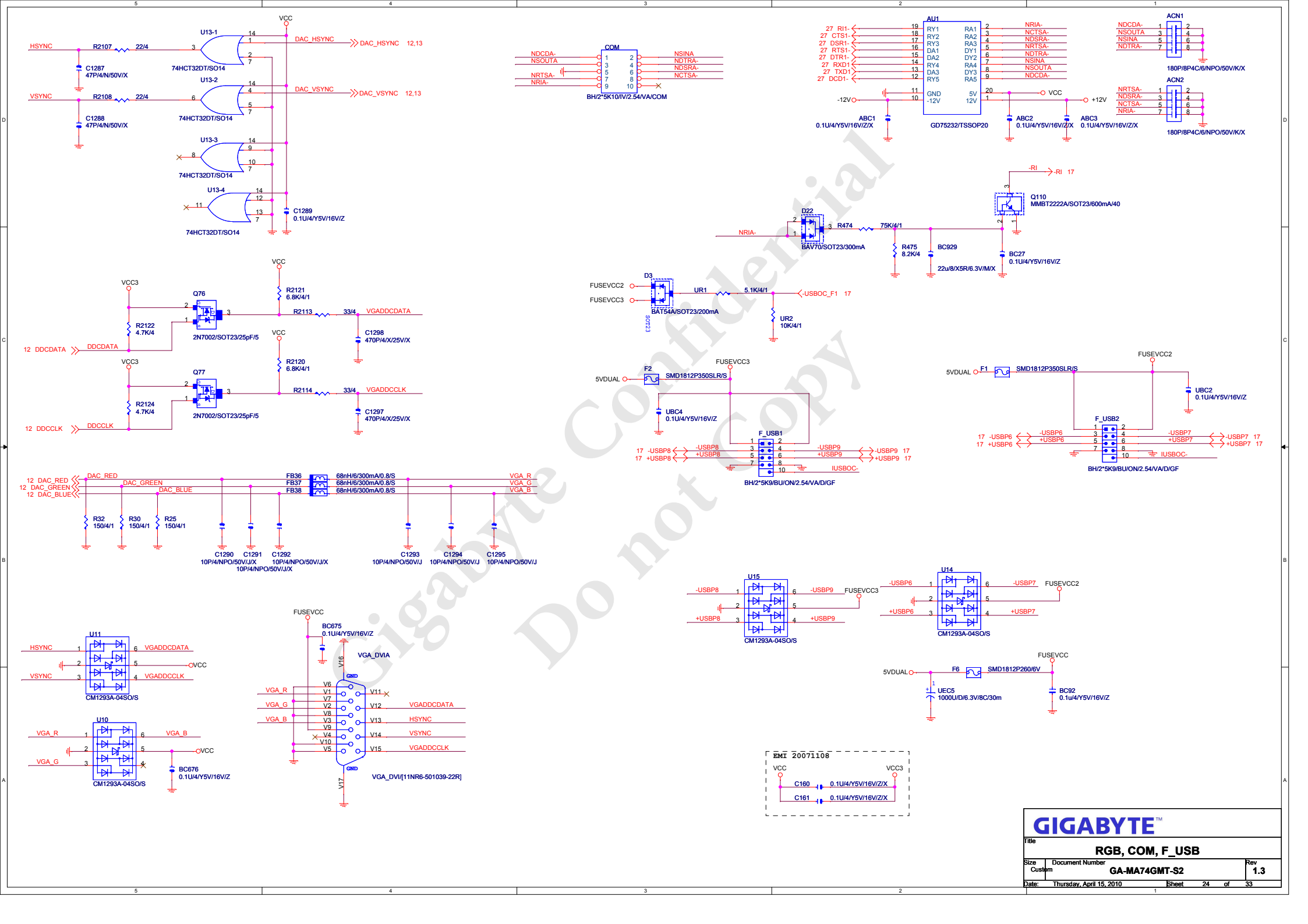

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Title	RGB, COM, F_USB	
Size: Custom	Document Number: GA-MA74GMT-S2	Rev: 1.3
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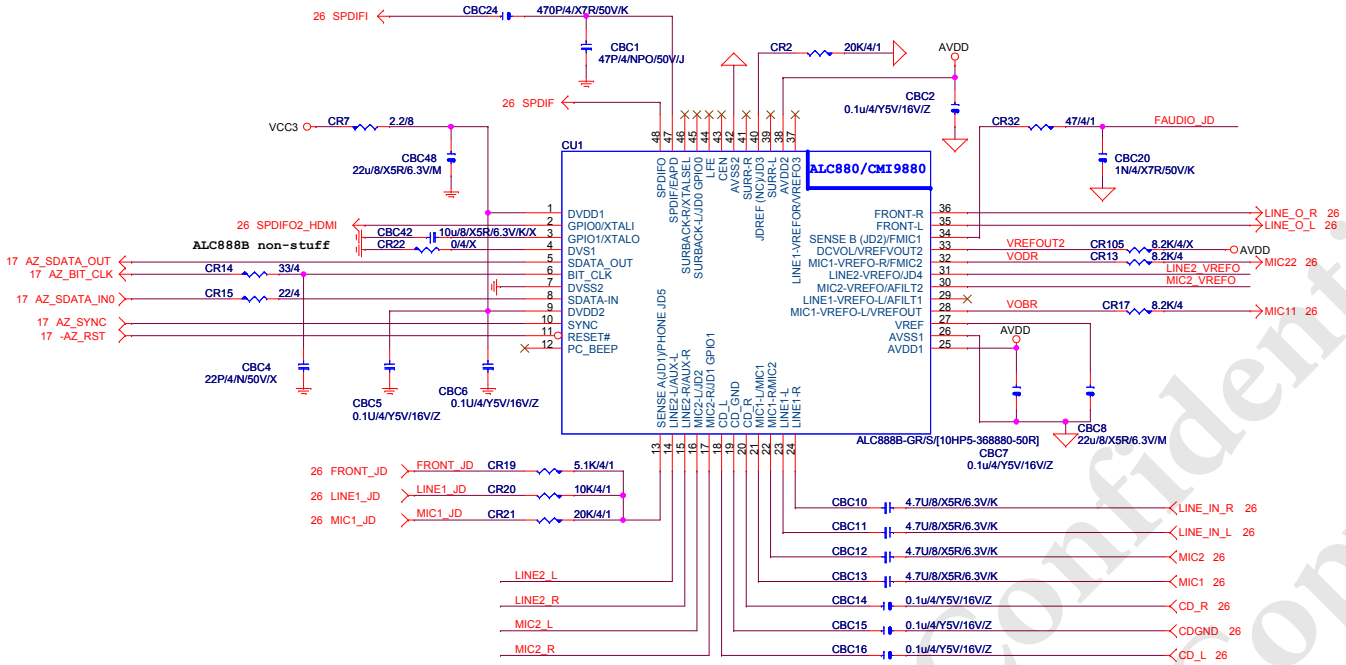

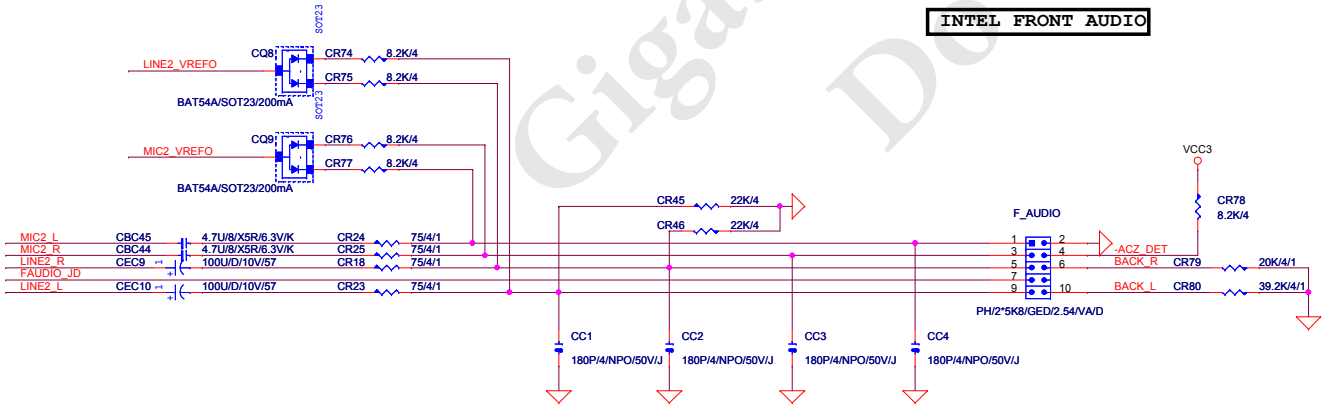

AZALIA CODEC *ALC892/ALC888B/ Colay*

	ALC892		ALC888B
CR22	X		X
CBC42	10uF/X5R		X
CR12	O		X
CR16	X		O

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Title: ALC888B CODEC

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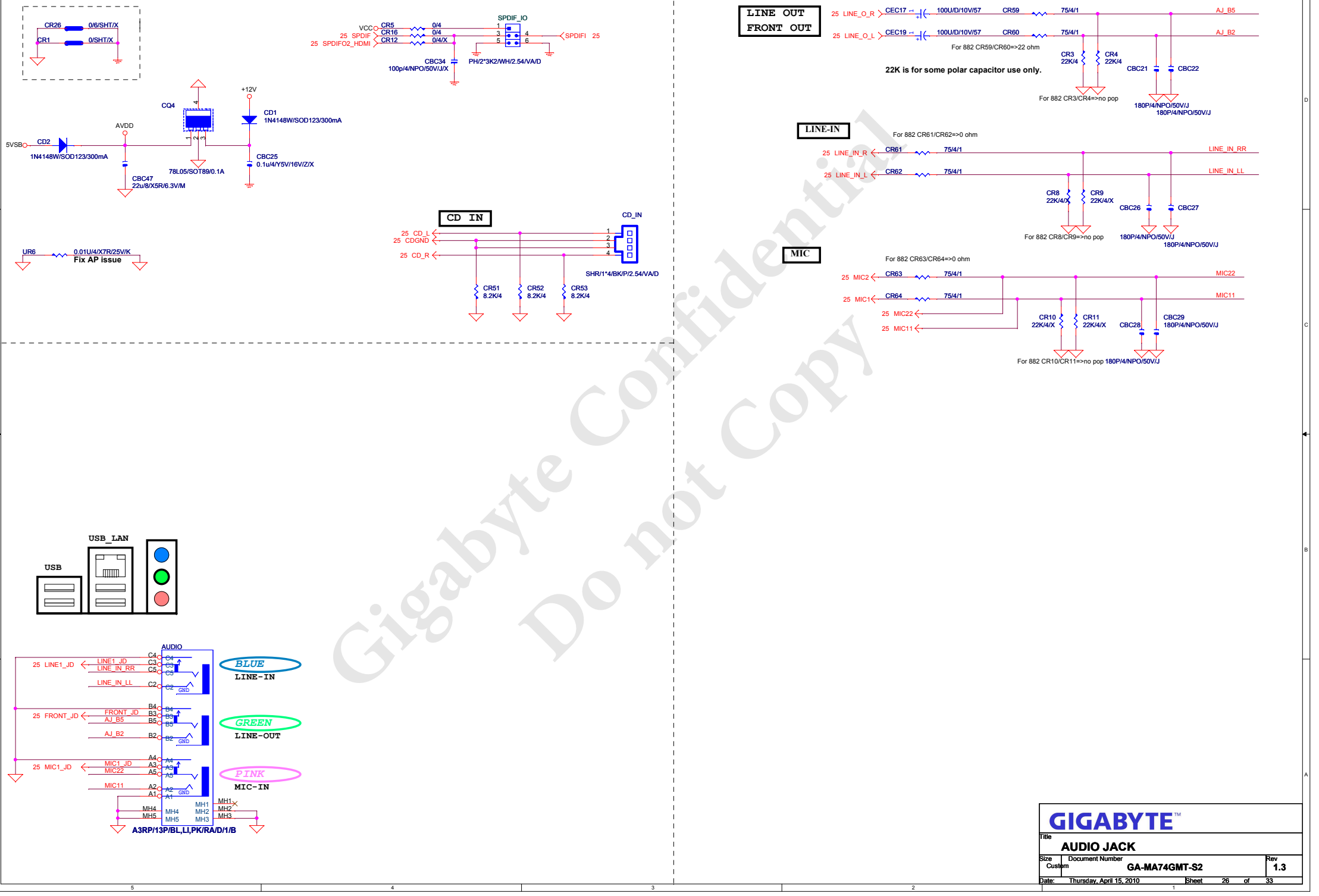

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Title: AUDIO JACK		
Size: Custom	Document Number: GA-MA74GMT-S2	Rev: 1.3
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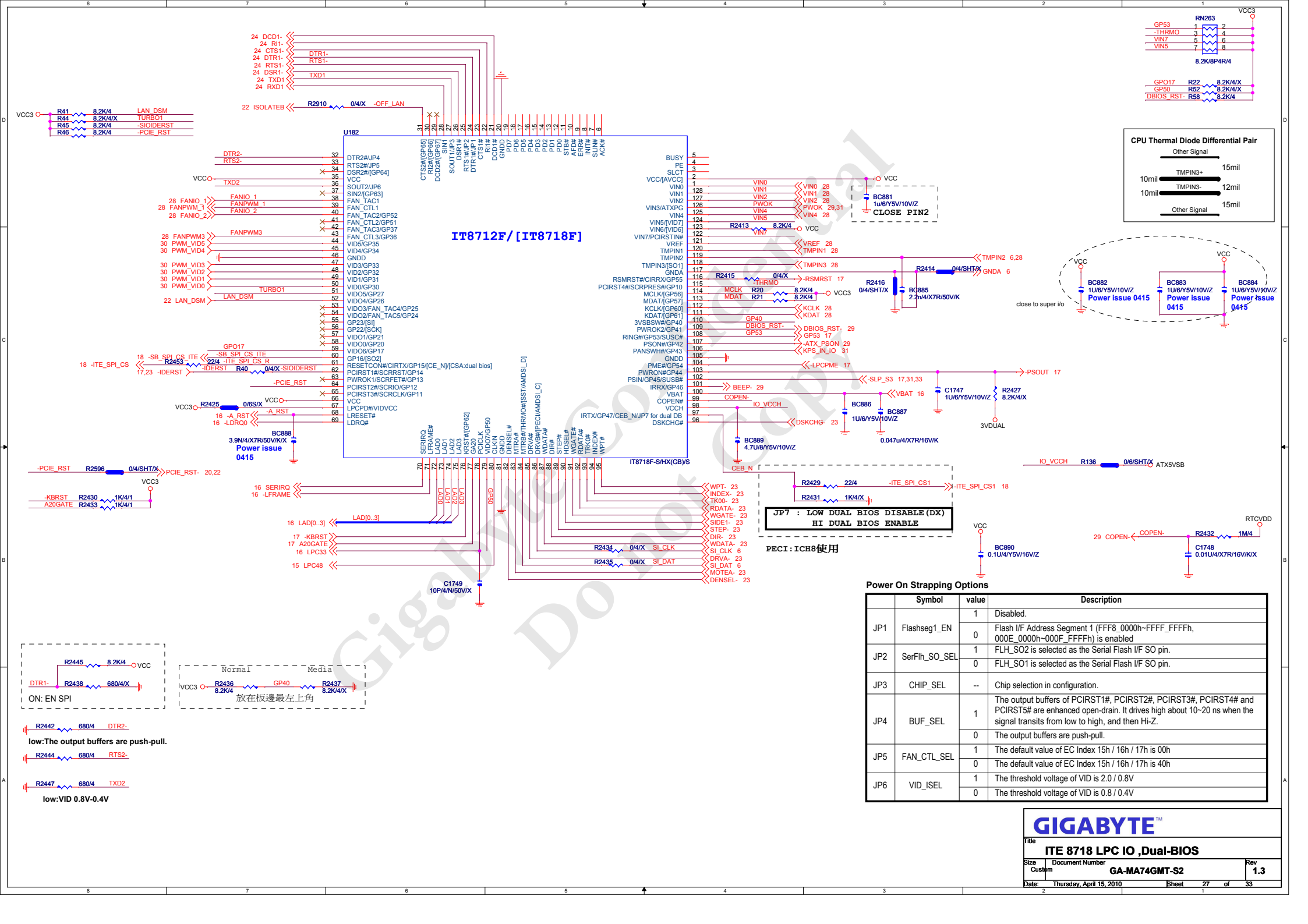

Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

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Title: ITE 8718 LPC IO ,Dual-BIOS

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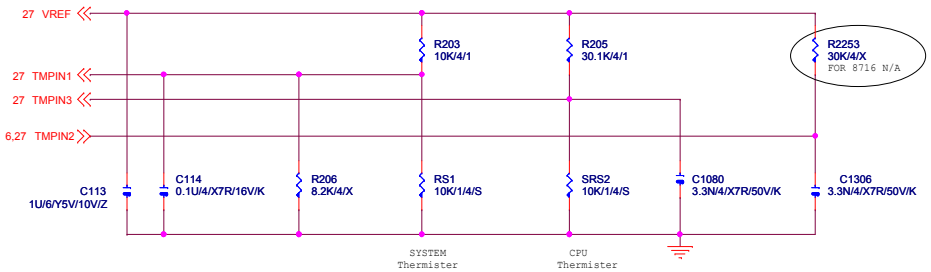
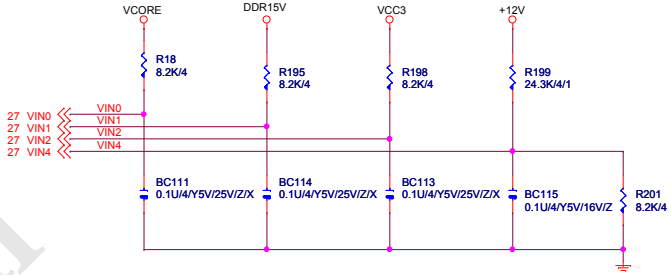
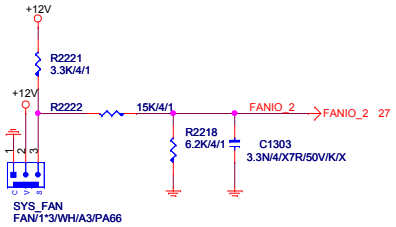
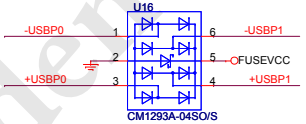
Hardware Monitor circuits



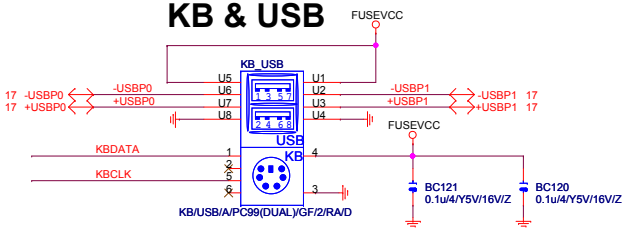


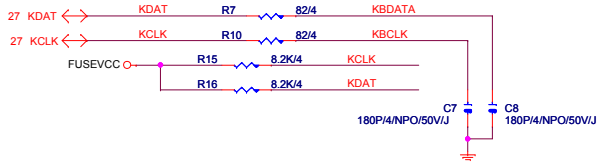
SYSTEM FAN

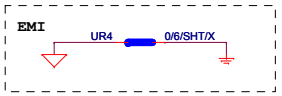


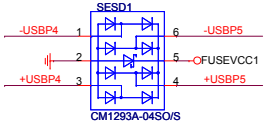


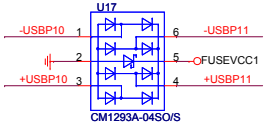
KB & USB

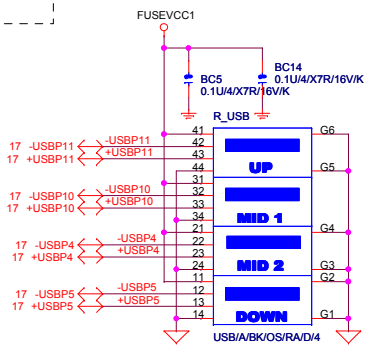




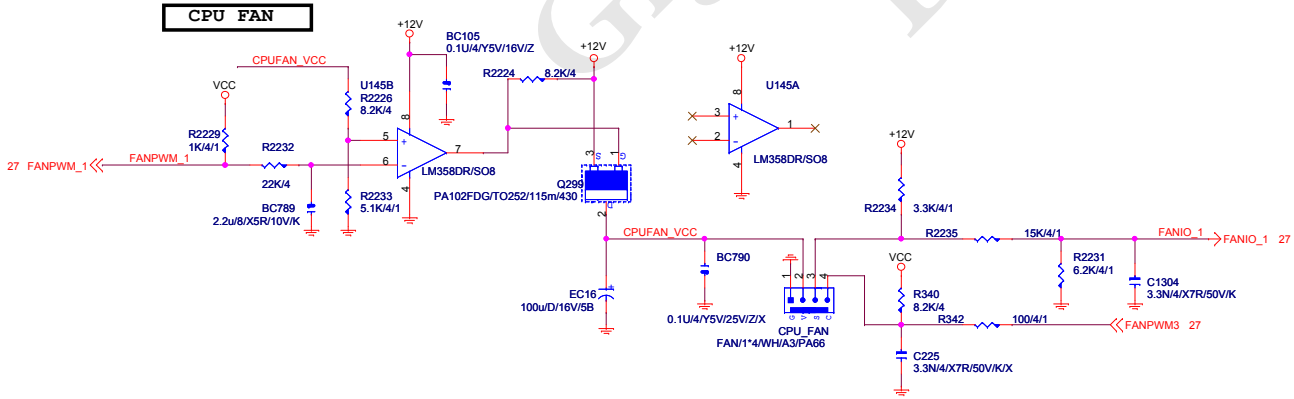








CPU FAN



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Title: FAN/HWMO ,KB/USB

Size: Custom | Document Number: GA-MA74GMT-S2 | Rev: 1.3

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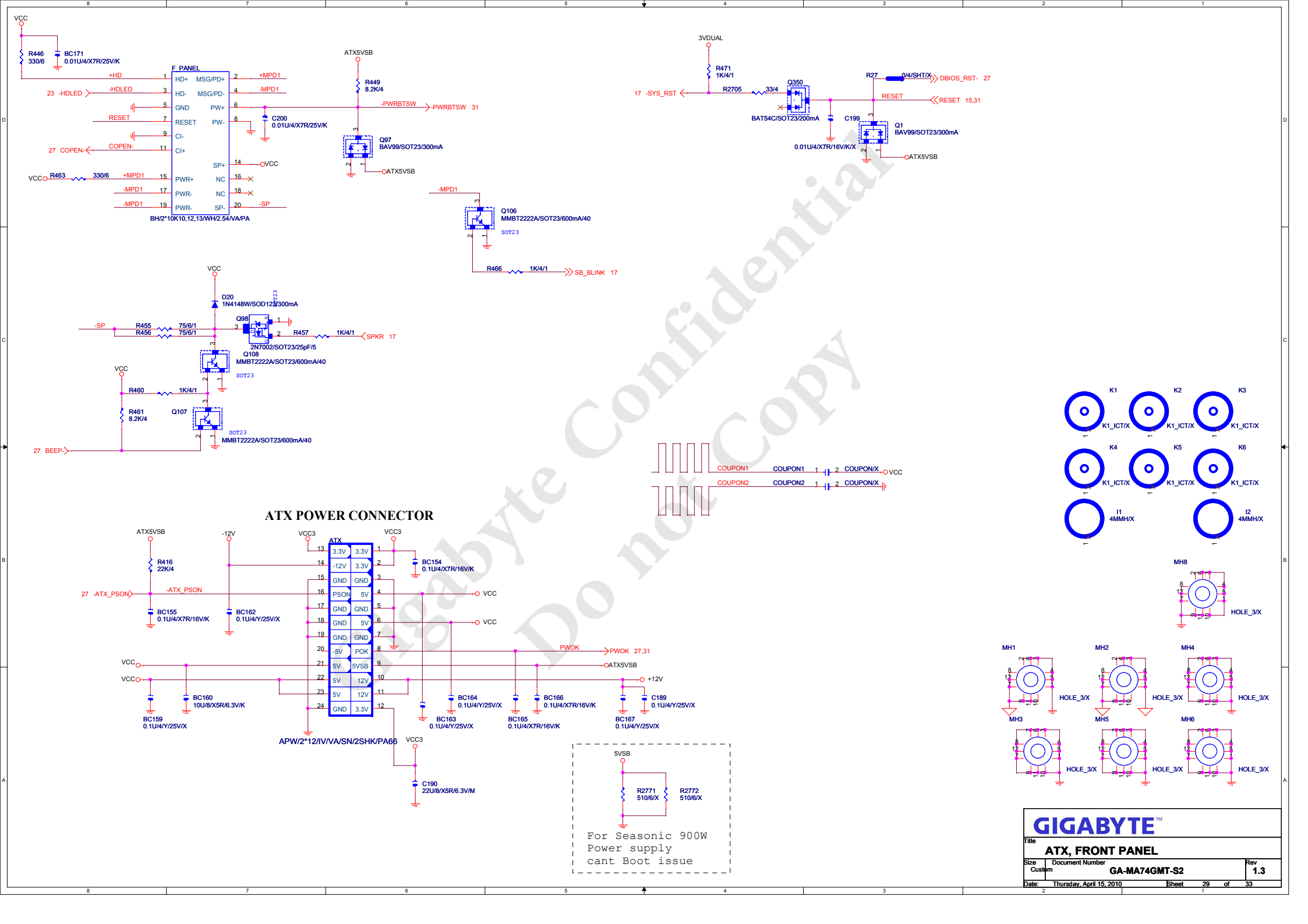
F_PANEL
BH/2*10K10,12,13/WH/2.54/VA/PA
ATX POWER CONNECTOR
APW/2*12/IV/VA/SN/2SHK/PA66
For Seasonic 900W
Power supply
cant Boot issue
GIGABYTE
ATX, FRONT PANEL
GA-MA74GMT-S2
1.3
Thursday, April 15, 2010
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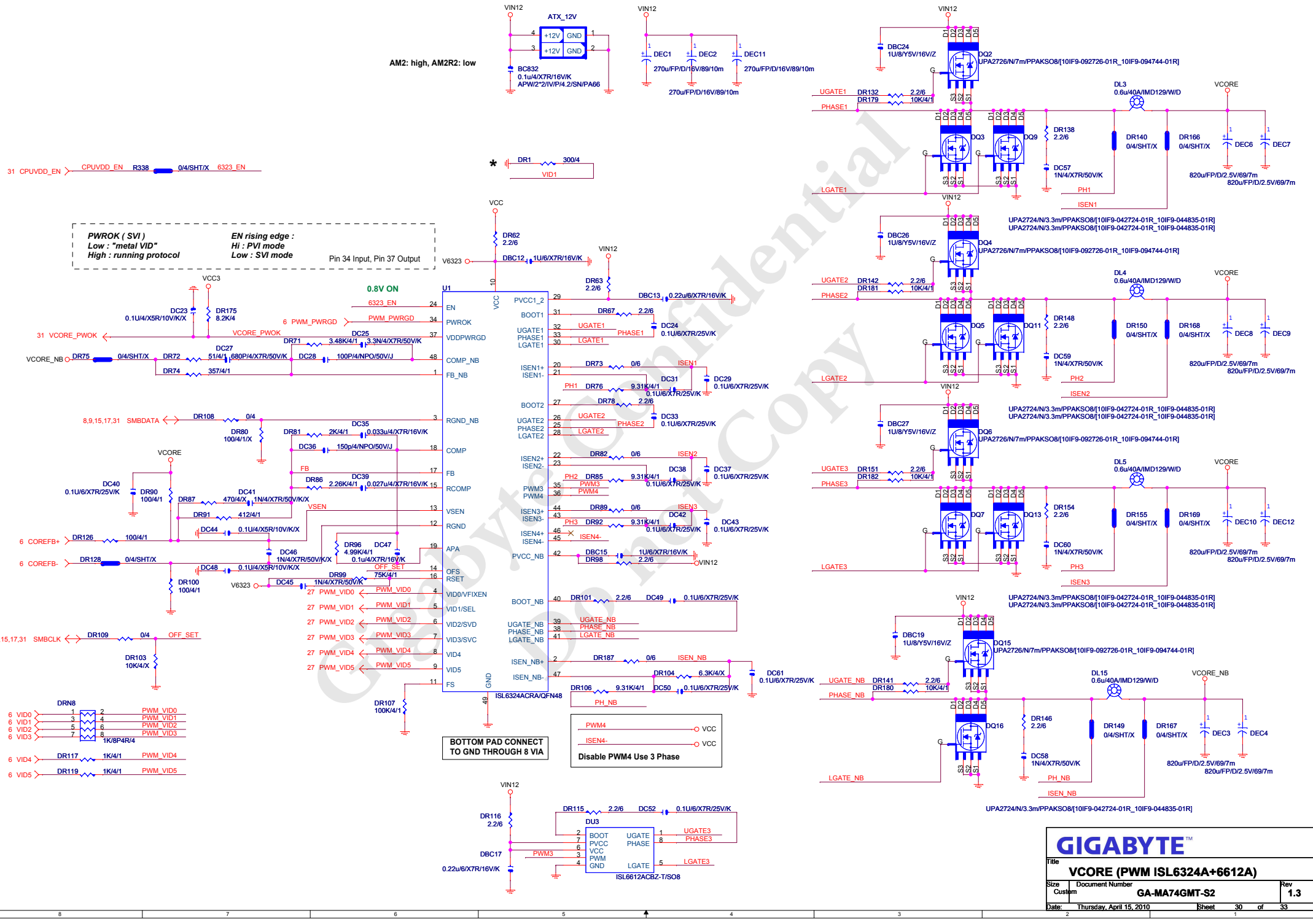

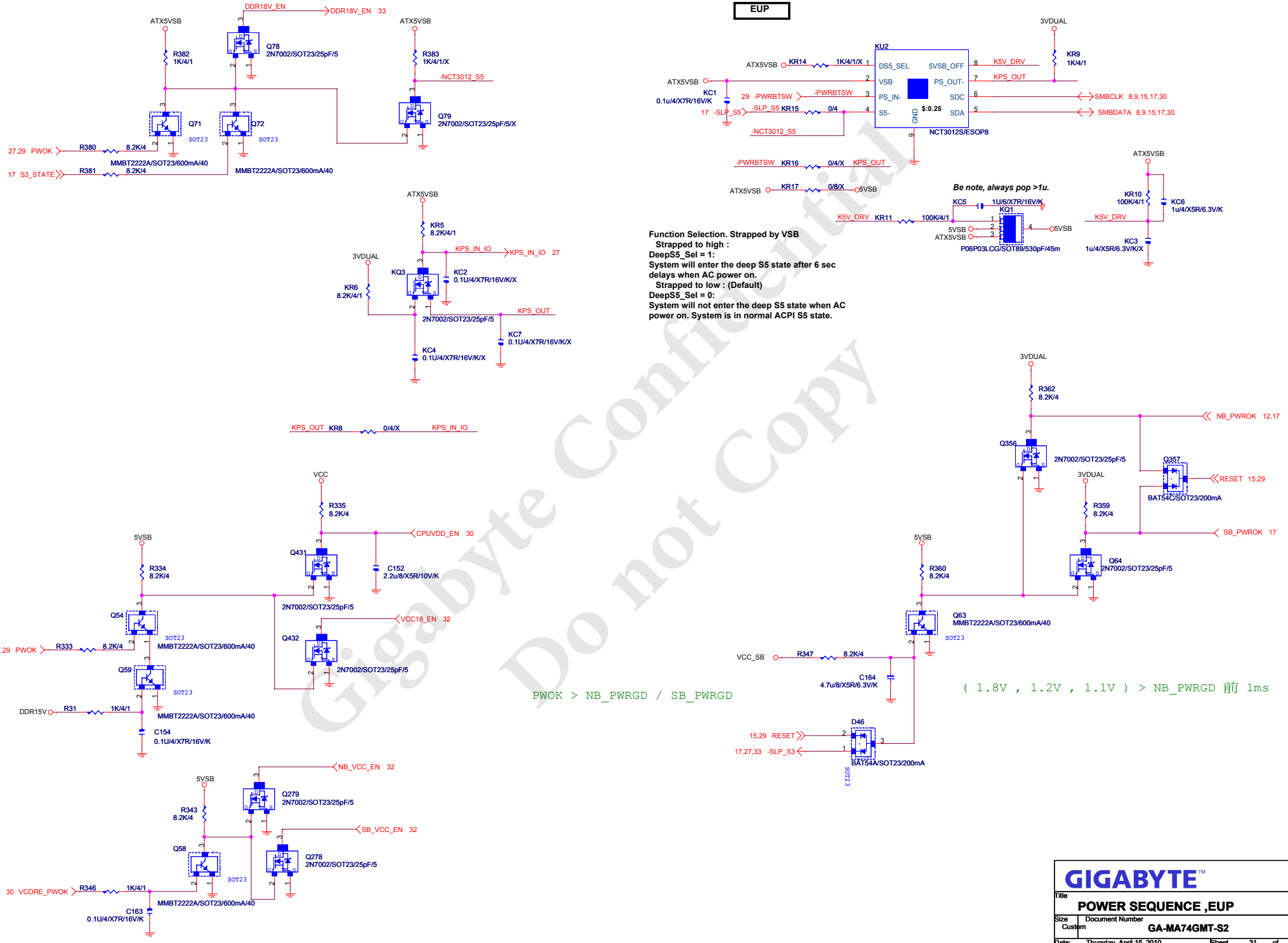

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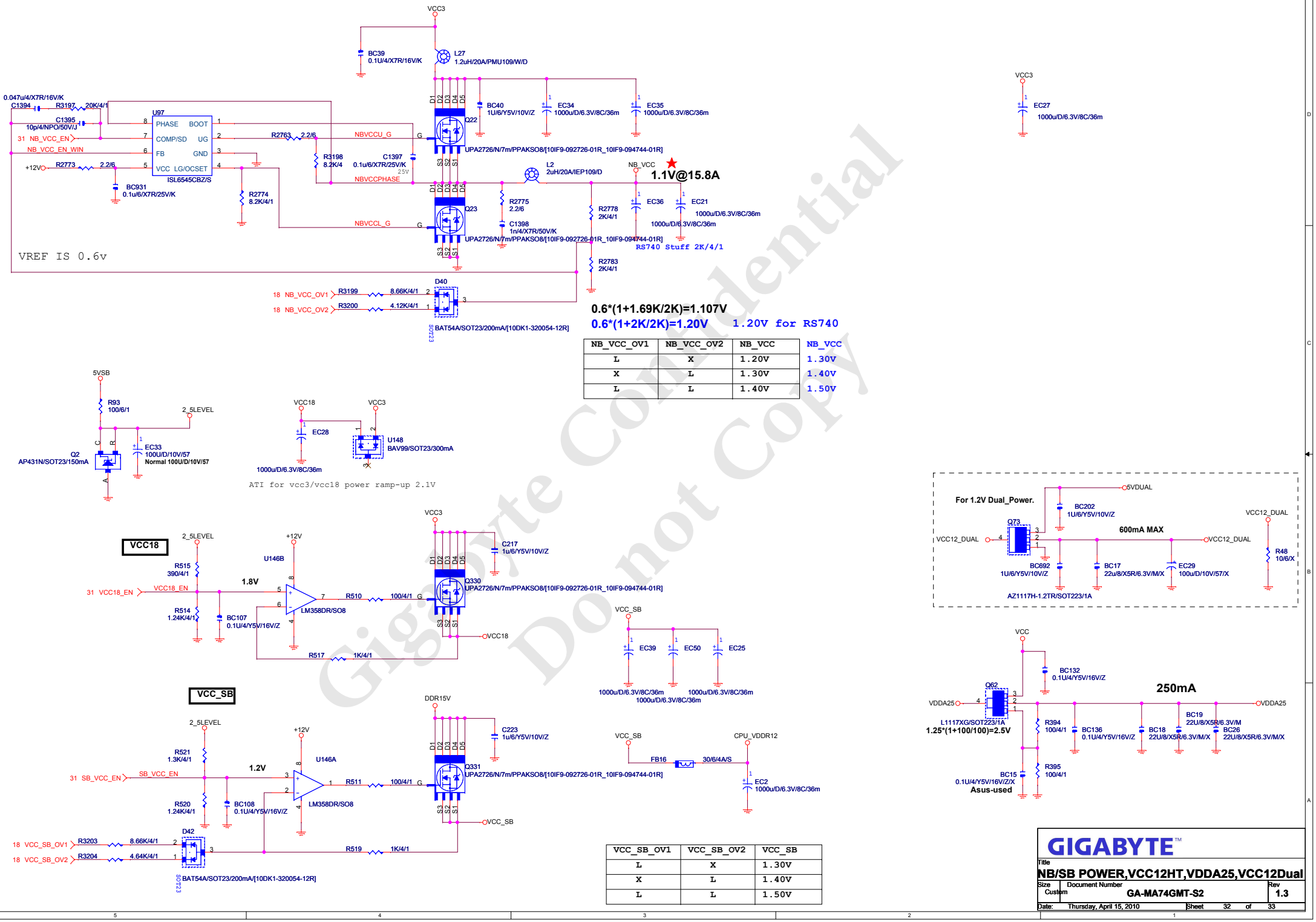

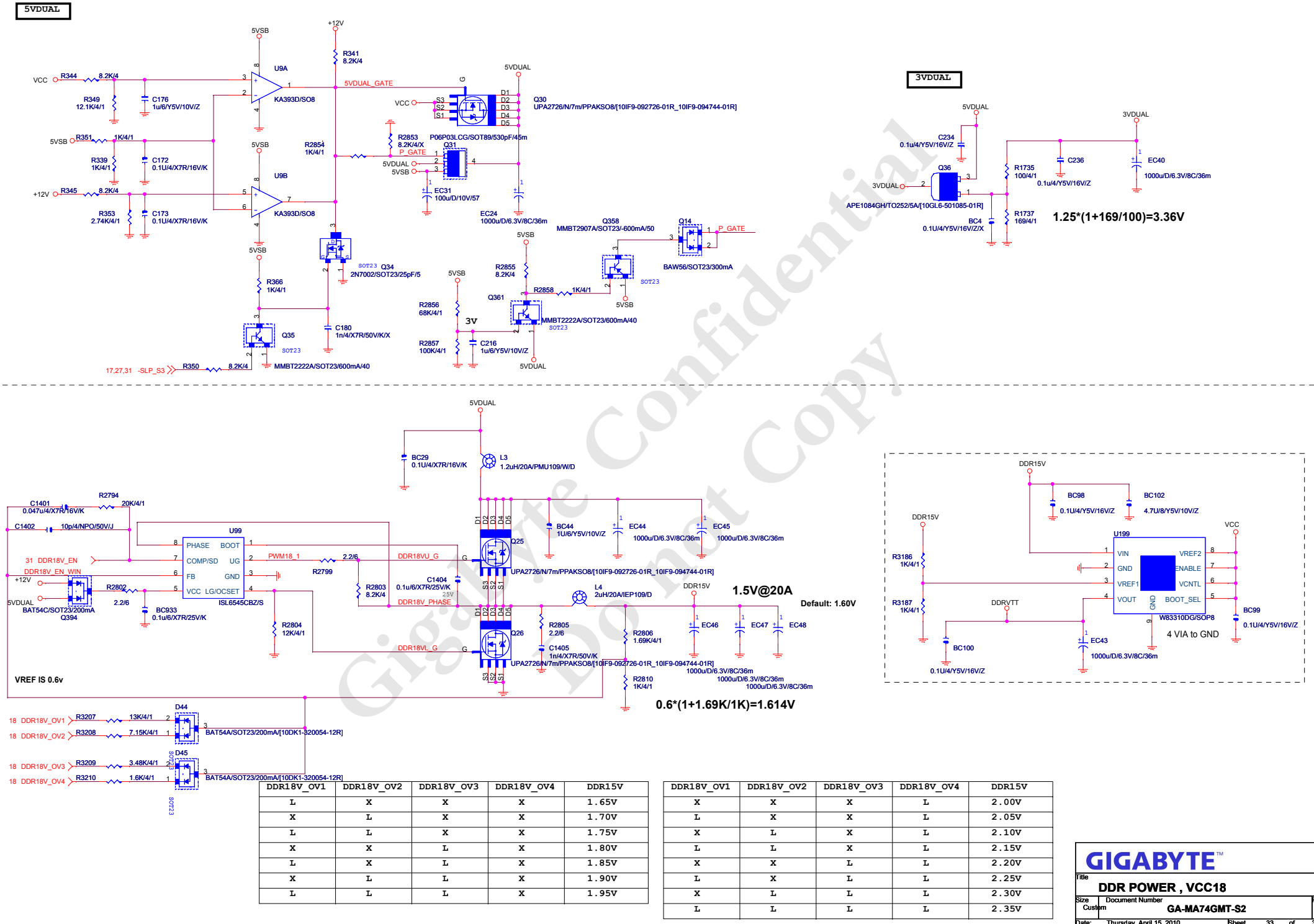

DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
L	X	X	X	1.65V
X	L	X	X	1.70V
L	L	X	X	1.75V
X	X	L	X	1.80V
L	X	L	X	1.85V
X	L	L	X	1.90V
L	L	L	X	1.95V

DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
X	X	X	L	2.00V
L	X	X	L	2.05V
X	L	X	L	2.10V
L	L	X	L	2.15V
X	X	L	L	2.20V
L	X	L	L	2.25V
X	L	L	L	2.30V
L	L	L	L	2.35V

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