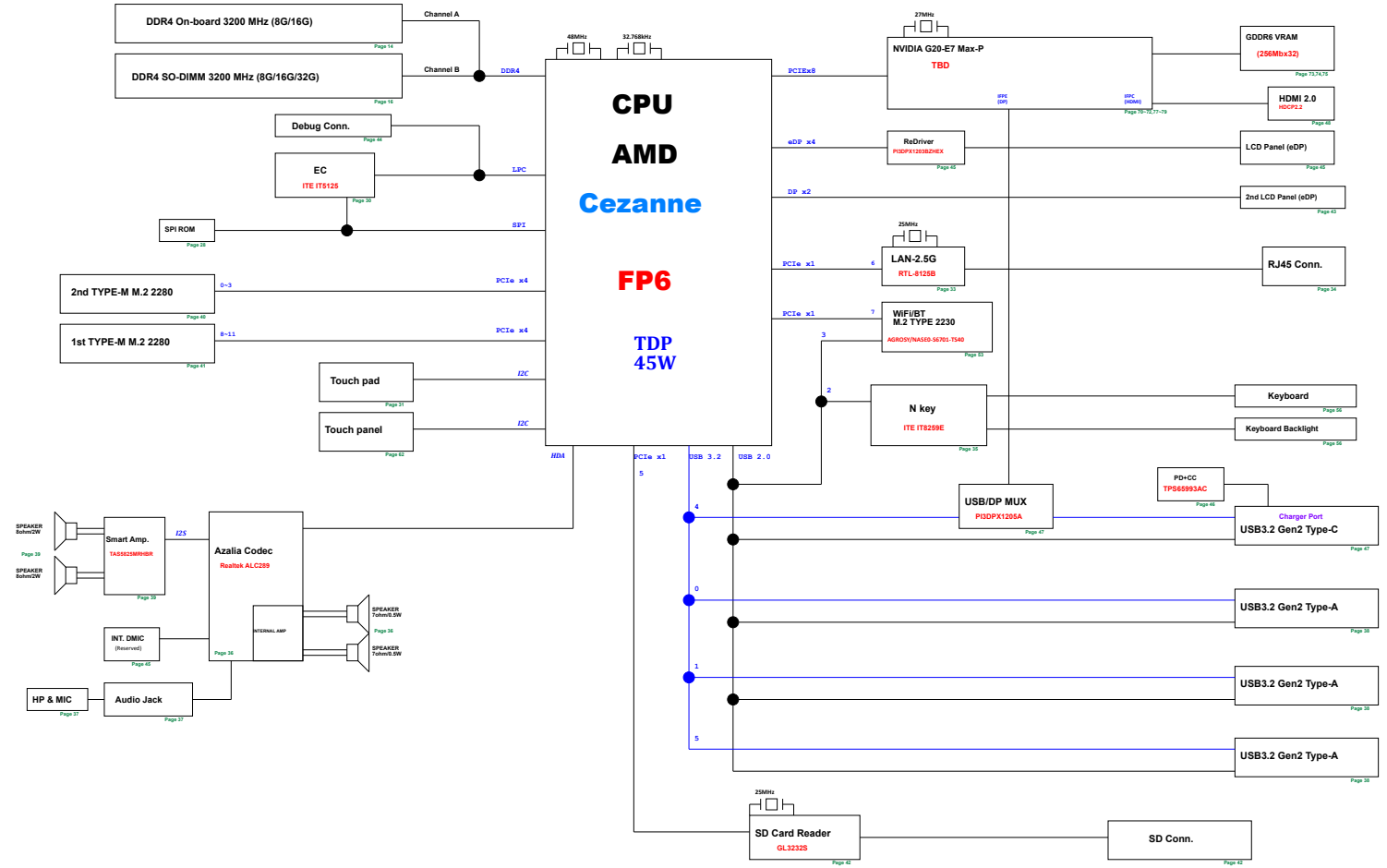
GX551Q Block Diagram



ASUS	Project Name: GX551Q	Rev: R1.0
Title: Cezanne_Block Diagram_R1.0		
Size: Custom	Dept.: KUKUNOR COMPUTER INC.	Engineer: NB1 RD2 EE2
Date: Friday, November 06, 2020	Sheet: of	

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	RCIN#	Native	RC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	GPO	(N.C)			
GPP_A12	GPI	GPO	(N.C)			
GPP_A13	SUSWANRN#	Native	ME_SusPwrDnAck		PU 10K(@)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPO	(N.C)			
GPP_A17	GPI	GPO	(N.C)			
GPP_A18	GPI	GPO	(N.C)			
GPP_A19	GPI	GPO	(N.C)			
GPP_A20	GPI	GPO	(N.C)			
GPP_A21	GPI	GPO	TBTA_MRESET(Reserved)			
GPP_A22	GPI	GPO	PCH_RTD3_CIO_PWR_EN		PU 10K	+VCC3V3_SX
GPP_A23	GPI	GPO	PCH_RTD3_USB_PWR_EN		PD 100K	

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPI	GPI	TBT_I2C_INT_PCH		PU 10K	+3VSUS
GPP_B2	GPI	GPO	(N.C)			
GPP_B3	GPI	GPO	(N.C)			
GPP_B4	GPI	GPO	(N.C)			
GPP_B5	GPI	Native	CLK_REQ0#/CLKREQ0_PEGA#		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K(@)	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#/CLKREQ2_WLAN_AC#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLK_REQ3#		PU 10K(@)	+3VSUS
GPP_B9	GPI	Native	CLK_REQ4#/CLKREQ4_GLAN#		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLK_REQ5#/CLKREQ5_TBT #		PU 10K	+3VSUS
GPP_B11	GPO	GPO	(N.C)			
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPPB14	PD		
GPP_B15	GPI	GPI	PCH_GPPB15/KB_LANG_ID0		PU 10K	+3VS
GPP_B16	GPI	GPI	PCH_GPPB16/KB_LANG_ID1		PU 10K	+3VS
GPP_B17	GPI	GPO	PCH_GPPB17/XBOX_WRST		PD 10K	
GPP_B18	GPO	Strap	PCH_GPPB18	PD		
GPP_B19	GPI	GPO	PCH_GPPB19/BT_ON_PCH		PD 10K(@)	
GPP_B20	GPI	GPO	PCH_GPPB20/GPUEVENT#_PCH		PU 10K	+3VSUS
GPP_B21	GPI	GPI	PCH_GPPB21/GC6FBEN_PCH		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPPB22	PD		
GPP_B23	GPO	Native	SML1ALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	GPI	GPP_C2_BT_UART_WAKE_N	PD	PU 4.7K	+3VSUS
GPP_C3	SML0CLK	Native	SML0_CLK (Reserved)		PU 2.2K	+3VSUS
GPP_C4	SML0DATA	Native	SML0_DAT (Reserved)		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		
GPP_C6	SML1CLK	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	SML1DATA	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPO	(N.C)			
GPP_C9	GPI	GPO	(N.C)			
GPP_C10	GPI	GPO	(N.C)			
GPP_C11	GPI	GPO	(N.C)			
GPP_C12	GPI	GPI	DIMM_SEL0			
GPP_C13	GPI	GPI	DIMM_SEL1			
GPP_C14	GPI	GPI	DIMM_SEL2			
GPP_C15	GPI	GPI	NFC_ID		PU 10K	+3VSUS
GPP_C16	GPI	Native	TBT_I2C_SDA_PCH		PU 2.2K	+3VSUS
GPP_C17	GPI	Native	TBT_I2C_SCL_PCH		PU 2.2K	+3VSUS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PU 10K	+3VS_NV
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	(N.C)			
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPO	(N.C)			
GPP_D1	GPI	GPO	(N.C)			
GPP_D2	GPI	GPO	(N.C)			
GPP_D3	GPI	GPO	(N.C)			
GPP_D4	GPI	GPO	(N.C)			
GPP_D5	GPI	Native3	PCH_GPPD5/M.2_BT_PCMFRM_CRF_RST_N		PD 75K	
GPP_D6	GPI	Native3	PCH_GPPD6/M.2_BT_PCMOUT_CLKREQ0		PD 75K(@)	
GPP_D7	GPI	GPO	PCH_GPPD7/M.2_BT_PCMIN		PD 100K(@)	
GPP_D8	GPI	GPO	PCH_GPPD8/M.2_BT_PCMCLK			
GPP_D9	GPI	GPO	(N.C)			
GPP_D10	GPI	GPO	(N.C)			
GPP_D11	GPI	GPO	(N.C)			
GPP_D12	GPI	GPO	(N.C)			
GPP_D13	GPI	GPO	(N.C)			
GPP_D14	GPI	GPO	(N.C)			
GPP_D15	GPI	GPO	(N.C)			
GPP_D16	GPI	GPO	(N.C)			
GPP_D17	GPI	GPO	(N.C)			
GPP_D18	GPI	GPO	(N.C)			
GPP_D19	GPI	GPO	(N.C)			
GPP_D20	GPI	GPO	(N.C)			
GPP_D21	GPI	GPO	(N.C)			
GPP_D22	GPI	GPO	(N.C)			
GPP_D23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	Native	SATAPCIE_DET0		PU 10K(@)	+3VS
GPP_E1	GPI	Native	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	Native	SATAPCIE_DET2		PU 10K(@)	+3VS
GPP_E3	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_E4	GPI	Native	SATA0_HDD1_DEVSLP		PU 10K(@)	+3VS
GPP_E5	GPI	Native	SATA1_NGFF3_DEVSLP		PU 10K(@)	+3VS
GPP_E6	GPI	Native	NGFF3_DEVSLP		PU 10K(@)	+3VSUS
GPP_E7	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_E8	GPI	Native	SATA_LED#		PU 10K	+3VS
GPP_E9	GPI	Native	USB_OC#0		PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1		PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2		PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3		PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	Native	SATAPCIE_DET3		PU 10K(@)	+3VS
GPP_F1	GPI	Native	SATAPCIE_DET4		PU 10K	+3VS
GPP_F2	GPI	GPO	(N.C)			
GPP_F3	GPI	GPO	(N.C)			
GPP_F4	GPI	GPO	(N.C)			
GPP_F5	GPI	GPO	(N.C)			
GPP_F6	GPI	GPO	(N.C)			
GPP_F7	GPI	GPO	(N.C)			
GPP_F8	GPI	GPO	(N.C)			
GPP_F9	GPI	GPO	(N.C)			
GPP_F10	GPI	GPO	(N.C)			
GPP_F11	GPI	GPO	(N.C)			
GPP_F12	GPI	GPO	(N.C)			
GPP_F13	GPI	GPO	(N.C)			
GPP_F14	GPI	GPO	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	GPO	(N.C)			
GPP_F20	GPI	GPO	(N.C)			
GPP_F21	GPI	GPO	(N.C)			
GPP_F22	GPI	GPO	(N.C)			
GPP_F23	GPI	GPO	PCH_GPPF23		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPO	(N.C)			
GPP_G1	GPI	GPO	(N.C)			
GPP_G2	GPI	GPO	(N.C)			
GPP_G3	GPI	GPO	(N.C)			
GPP_G4	GPI	GPO	(N.C)			
GPP_G5	GPI	GPO	(N.C)			
GPP_G6	GPI	GPO	(N.C)			
GPP_G7	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLK_REQ6#/CLKREQ6_NGFF1#		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLK_REQ7#/CLKREQ7_NGFF2#		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#/CLKREQ8_NGFF3#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K(@)	+3VSUS
GPP_H4	GPI	Native	CLK_REQ10#		PU 10K(@)	+3VSUS
GPP_H5	GPI	Native	CLK_REQ11#		PU 10K(@)	+3VSUS
GPP_H6	GPI	Native	CLK_REQ12#		PU 10K(@)	+3VSUS
GPP_H7	GPI	Native	CLK_REQ13#		PU 10K(@)	+3VSUS
GPP_H8	GPI	Native	CLK_REQ14#		PU 10K(@)	+3VSUS
GPP_H9	GPI	Native	CLK_REQ15#		PU 10K(@)	+3VSUS
GPP_H10	GPI	GPO	(N.C)			
GPP_H11	GPI	GPO	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD	PD 20K(@)	
GPP_H13	GPI	GPO	(N.C)			
GPP_H14	GPI	GPO	(N.C)			
GPP_H15	GPI	GPO	SML3ALERT#		PU 100K	+3VSUS
GPP_H16	GPI	GPI	KBID_0			
GPP_H17	GPI	GPI	KBID_1			
GPP_H18	GPI	GPI	KBID_2			
GPP_H19	GPI	GPO	(N.C)			
GPP_H20	GPI	GPO	(N.C)			
GPP_H21	GPI	GPO	(N.C)			
GPP_H22	GPI	GPO	(N.C)			
GPP_H23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	GPO	(N.C)			
GPP_I1	GPI	GPO	(N.C)			
GPP_I2	GPI	GPO	(N.C)			
GPP_I3	GPI	GPO	(N.C)			
GPP_I4	GPI	GPO	EDP_HPD		PD 100K	
GPP_I5	GPI	GPO	(N.C)			
GPP_I6	GPO	GPO	(N.C)			
GPP_I7	GPI	GPO	(N.C)			
GPP_I8	GPO	GPO	(N.C)			
GPP_I9	GPI	GPO	(N.C)			
GPP_I10	GPO	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_J0	GPI	GPO	(N.C)			
GPP_J1	CPU_VCCIO_PWR_GATE#	Native	CPU_C10_GATE#_PCH		PU 100K	+1.8VSUS
GPP_J2	GPI	GPO	(N.C)			
GPP_J3	GPI	GPO	(N.C)			
GPP_J4	CNV_BRI_DT	Native	CNV_BRI_DT		PU 4.7K	+1.8VSUS
GPP_J5	CNV_BRI_RSP	Native	CNV_BRI_RSP		PU 20K(@)	+1.8VSUS
GPP_J6	CNV_RGI_DT	Native	CNV_RGI_DT		PD 75K	
GPP_J7	CNV_RGI_RSP	Native	CNV_RGI_RSP		PU 20K(@)	+1.8VSUS
GPP_J8	GPI	GPO	(N.C)			
GPP_J9	GPO	GPO	(N.C)			
GPP_J10	GPI	GPO	(N.C)			
GPP_J11	A4WP_PRESENT	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_K0	GPI	GPO	GPIO_3_FORCE_PWR		PD 100K	
GPP_K1	GPI	GPI	PCB_ID0		PD 10K	
GPP_K2	GPI	GPI	PCB_ID1		PD 10K	
GPP_K3	GPI	GPO	GPP_K3/WLAN_BT_LED		PD 100K	
GPP_K4	GPI	GPO	GPP_K4/WLAN_LED		PD 100K	
GPP_K5	GPI	GPO	VOL_DOWN#(N.C)			
GPP_K6	GPI	GPO	VOL_UP#(N.C)			
GPP_K7	GPI	GPO	GPP_K7/TBT_HPD#		PU 10K	+3VS
GPP_K8	GPI	GPO	GPP_K8/DGPU_PWR_EN#		PU 10K(@)	+3VS
GPP_K9	GPI	GPO	WLAN_ON#		PD 100K	
GPP_K10	Reserved	GPO	GPP_K10/HDMI_HPD#		PU 10K	+3VS
GPP_K11	Reserved	GPO	GPP_K11/DP_HPD#		PU 10K	+3VS
GPP_K12	GPI	GPO	(N.C)			
GPP_K13	GPI	GPO	(N.C)			
GPP_K14	GPI	GPO	(N.C)			
GPP_K15	GPI	GPO	(N.C)			
GPP_K16	GPI	GPO	(N.C)			
GPP_K17	GPI	GPO	(N.C)			
GPP_K18	GPI	GPO	(N.C)			
GPP_K19	GPI	GPO	(N.C)			
GPP_K20	Reserved	GPO	(N.C)			
GPP_K21	Reserved	GPO	(N.C)			
GPP_K22	GPI	GPO	(N.C)			
GPP_K23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 10K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#(N.C)		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#		PD 100K	
GPD6	SLP_A#	Native	SLP_A# (N.C)			
GPD7	GPO	GPO	PCH_GPD7		PU 10K	+3VA_DSW
GPD8	SUSCLK	Native	SUS_CLK#			
GPD9	SLP_WLAN#	Native	SLP_WLAN# (N.C)			
GPD10	SLP_S5#	Native	SLP_S5# (N.C)			
GPD11	LANPHYPC	GPO	LAN_PWREN (N.C)		PU 10K(@)	+3VA_DSW

IT8225VG-128/BX GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#		
GPA2	OD	GPO	CHG_FULL_LED#		
GPA3	Alt	PWM	FAN2_PWM		
GPA4	O	GPO	EC_GPA4(N.C)		
GPA5	Alt	PWM	FAN1_PWM		
GPA6	Alt	GPO	EC_GPA6(N.C)		
GPA7	O	GPO	EC_GPA7(N.C)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	EC_GPB2(N.C)		
GPB3	Alt	GPI	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	EC_GPB5/NKey_WRST	PD 10K	
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	EC_GPC0		
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K(@)	+3VSUS
GPC4	I	GPI	EC_GPC4/PM_SUSB#	PD 100K	
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PD 100K	
GPC7	O	GPO	EC_GPC7/NKEY_PWR_EN	PD 10K(@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPO	EC_GPD0/EC_OV_DDR		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/OP_SD#		
GPD6	Alt	GPI	FAN1_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN2_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	5VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE4	O	GPO	VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE5	I	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPE6	OD	GPO	WLAN_PWR_EN	PD 100K	
GPE7	OD	GPO	THRO_CPU#	PU 10K	+3VA_DSW

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	CAP_LED#		
GPF1	O	GPO	NUM_LED#		
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_PECI	PD 10K(@)	
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2	PU 100K	+3VA_EC
GPG6	O	GPO	EC_GPG6(N.C)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK/TBT_I2C_SCL_EC	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT/TBT_I2C_SDA_EC	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_RSMRST#	PD 10K	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

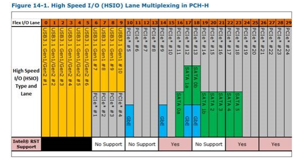
	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#	PD 100K(@)	
GPI1	I	GPI	3VSUS_PWRGD	PU 100K	+3VSUS
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP8_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD_EC	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#	PU 10K(@)	+3VSUS
GPI6	Alt	AD	A/D_MAX_POWER		
GPI7	Alt	AD	MB_MAX_POWER	PU 100K&PD 270K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPO	EC_GPJ0		
GPJ1	O	GPI	GC6FBEN_PCH	PU 10K(@)	+3VS
GPJ2	Alt	GPI	EC_GPJ2/TBTA_I2C_INT_EC		
GPJ3	O	GPO	EC_GPJ3/USB_BC1.2_OFF#		
GPJ4	Alt	GPO	EC_GPJ4/USB30_5VBUS		
GPJ5	O	GPI	EC_GPJ5/MB_DOCK_JACK_DETECT	PU 100K(@)	+3VA
GPJ6	I	GPI	NKEY_INT#	PU 10K	+3VA_DSW_NKeyPWR
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ESCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

571391_CFL_H_PDG_Rev0p71, page 230

Figure 14-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H



G703GI Source:

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	SM-Bus Address
SO-DIMM A(0)	A0h
SO-DIMM B(0)	A4h
SO-DIMM A(1)	A2h
SO-DIMM B(1)	A6h
EC Master (SMB1)	SM-Bus Address
SM-Bus Device	
GPU INT. Thermal sensor	9Eh, 9Ch
CPU Thermal Sensor	90h
TI_TAS5766M*2	98h, 9Ah
ASM1562	66h
GPU (Thermistor sense)	74h
PWR(Thermistor sense)	7Eh, 7Ch, 7Ah, 78h, 76h

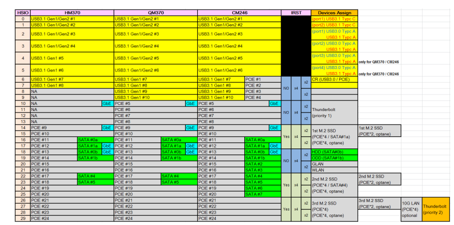
Device Identification

CPU Thermal Senser		
1st	06G023123010	NCT7717U
2nd		

GPU Thermistor		
1st	06021-00260000	APL6002A8I-TRG
2nd		

USB3.0/PCIE/SATA Setting		
1	USB3#1	
2	USB3#2	
3	USB3#3	USB Port1
4	USB3#4	
5	USB3#5	USB Port3
6	USB3#6	USB Port4
7	USB3#7	Card Reader
8	PCIE#2	
9	PCIE#3	
10	PCIE#4	
11	PCIE#5	ThunderBolt x4
12	PCIE#6	
13	PCIE#7	
14	PCIE#8	
15	PCIE#9	PCIE3.0 x 4 SSD
16	PCIE#10	
17	PCIE#11	
18	PCIE#12	
19	PCIE#13(SATA0B)	SATA HDD
20	PCIE#14(SATA1B)	
21	PCIE#15	GLAN
22	PCIE#16	WLAN_11AC
23	PCIE#17	PCIE3.0 x 4 SSD
24	PCIE#18	
25	PCIE#19	
26	PCIE#20	
27	PCIE#21	PCIE3.0 x 4 SSD
28	PCIE#22	
29	PCIE#23	
30	PCIE#24	

USB2.0 Setting		
1	USB2#1	
2	USB2#2	
3	USB2#3	USB Port1
4	USB2#4	
5	USB2#5	USB Port3
6	USB2#6	USB Port4
7	USB2#7	Card Reader
8	USB2#8	XBOX WLAN
9	USB2#9	Camera
10	USB2#10	N-Key
11	USB2#11	
12	USB2#12	Tobii IS4
13	USB2#13	TBT
14	USB2#14	BT



571182_CNL_PCH_H_EDS_Vol_1_Rev_0_7, page24

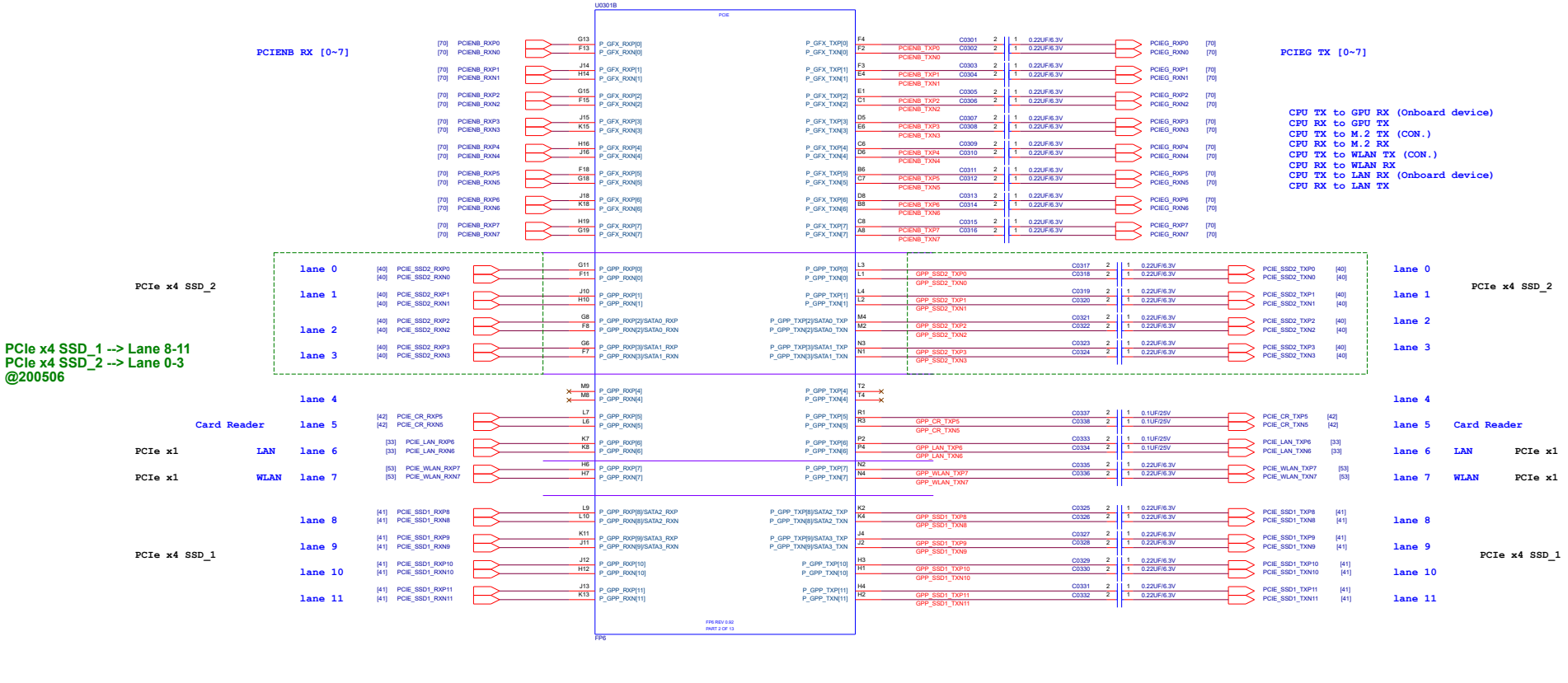
Table 1-7. PCH HSIO Detail (SKU 9-11of 11)

Flex I/O Lane	SKU		
	HM370	QM370	CM246
0	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
4	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
5	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
6	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
7	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
8	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
9	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
10	GbE	PCIe*, GbE	PCIe*, GbE
11	N/A	PCIe*	PCIe*
12	N/A	PCIe*	PCIe*
13	N/A	PCIe*	PCIe*
14	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
15	PCIe*	PCIe*	PCIe*
16	PCIe*, SATA 0A	PCIe*, SATA 0A	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B	PCIe*, SATA 1B	PCIe*, SATA 1B
20	PCIe*	PCIe*	PCIe*, SATA 2
21	PCIe*	PCIe*	PCIe*, SATA 3
22	PCIe*, SATA 4	PCIe*, SATA 4	PCIe*, SATA 4
23	PCIe*, SATA 5	PCIe*, SATA 5	PCIe*, SATA 5
24	PCIe*	PCIe*	PCIe*, SATA 6
25	PCIe*	PCIe*	PCIe*, SATA 7
26	PCIe*	PCIe*	PCIe*
27	PCIe*	PCIe*	PCIe*
28	PCIe*	PCIe*	PCIe*
29	PCIe*	PCIe*	PCIe*

PCIE/WLAN/LAN/SSD

RX Side

TX Side



Project Name	Rev
GX551Q	R1.0

Title : Ceanne_CPU_DMI,PEG,FDI,eDP,DDI_R1.0

Size: C | Dept.: ASUSTeK COMPUTER INC. | Engineer: NB1 RD2 EE1

Date: Friday, November 06, 2020 | Sheet 3 of 104

	Project Name Type-C_ALT_USB3-10G + DP + PD + Slave_Charger_TI	Rev R1.0

Title : USB3.1 TYPE-C+TI 1046A

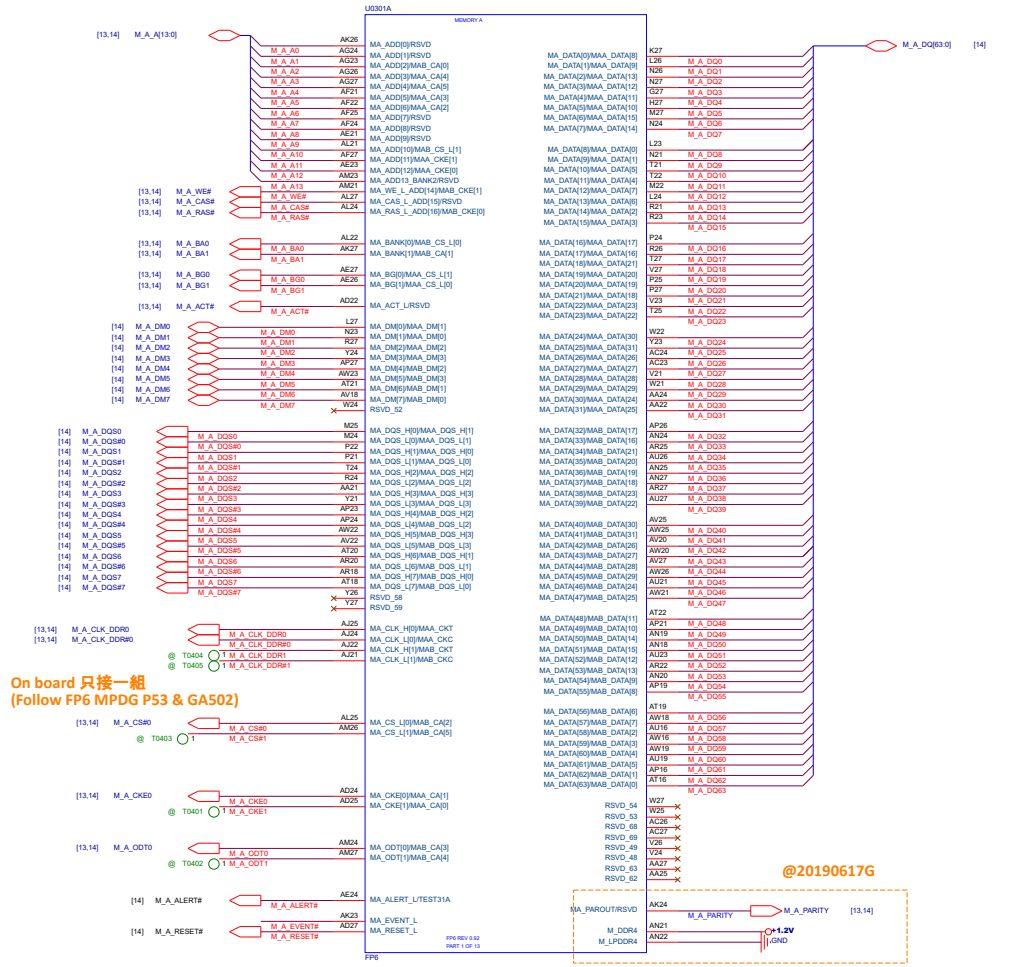
Size	Dept.:	Engineer:
D	ASUSTeK COMPUTER INC. NB1	Design IP

Date: Friday, November 06, 2020	Sheet 12	of	104

Memory Channel A

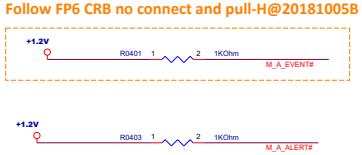
On Board DDR4

MA/B_
I/O-IOMEM-S/D VDDIO_MEM_S3 (S0_1.2)_FP6 (FDS)



On board 只接一組
(Follow FP6 MPDG P53 & GA502)

Follow FP6 CRB no connect and pull-H@20181005B

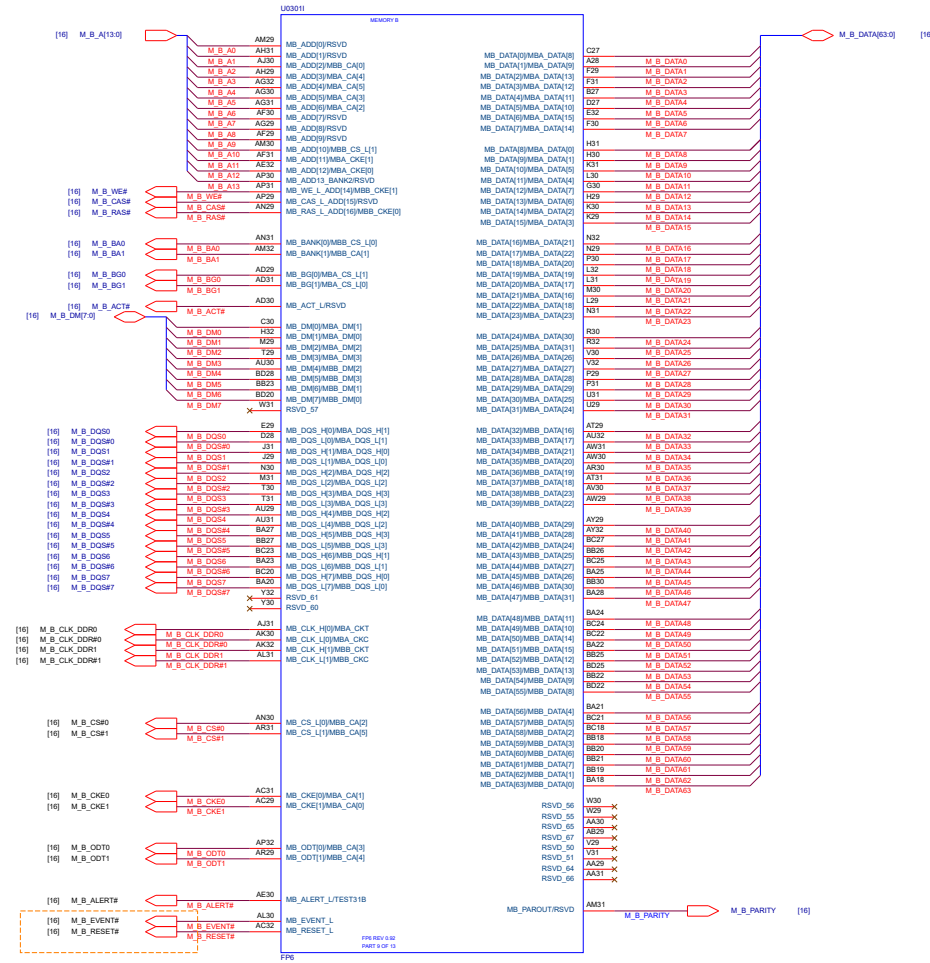


Mount by AMD review 8200612A

@20190617G

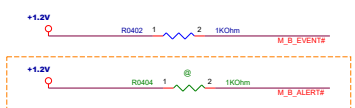
Memory Channel B

SO-DIMM DDR4



EVENT# 對接pull-H +1.2V (FP6 CRB)

RESET# only對接 (FP6 CRB)



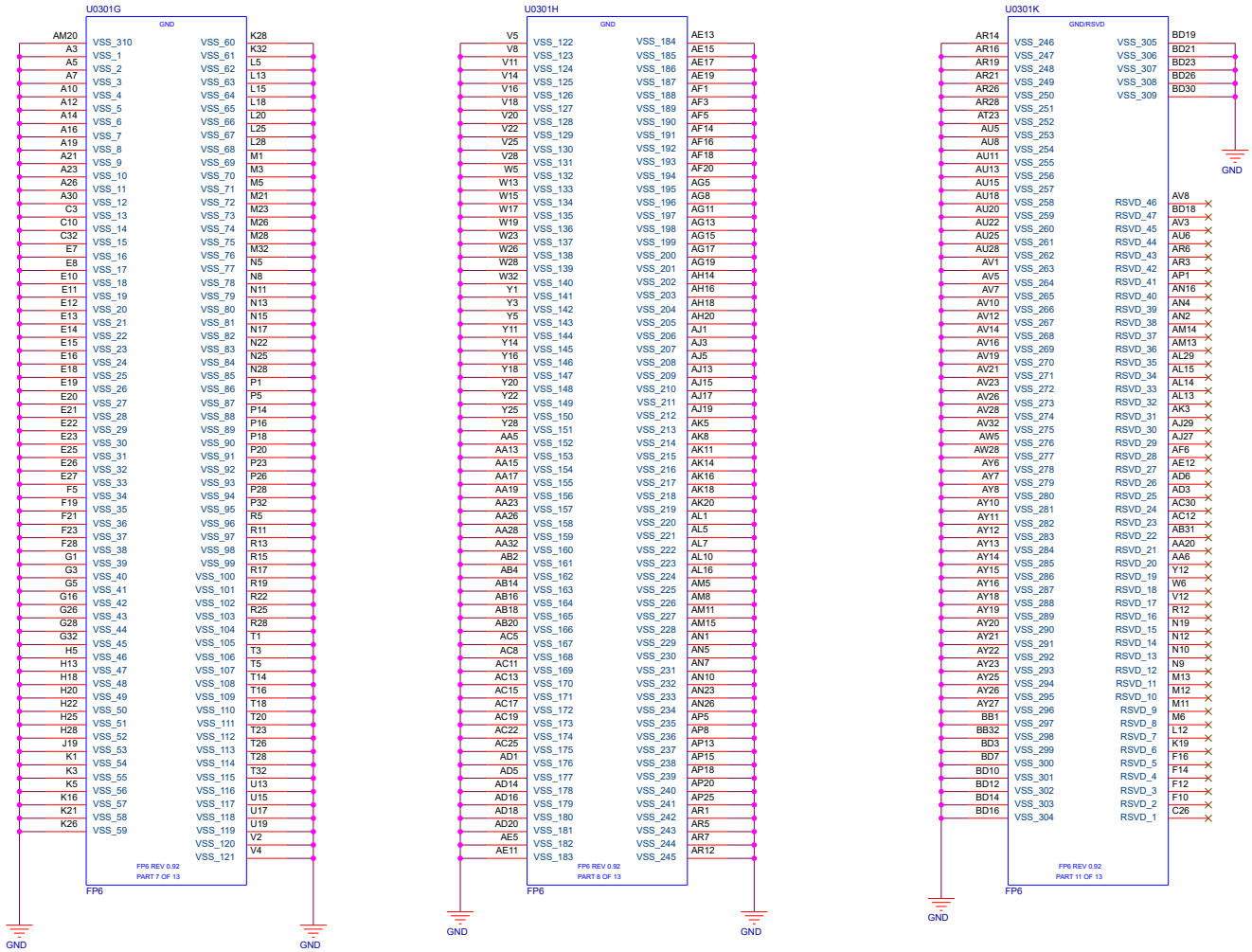
FP6 CRB預留不上

No Connect Fllow 17880D34747_FP5_Processor Motherboard Design_Guide

Main Board

ASUS	Project Name: FX505DY	Rev: R1.0
Title : AMD_CPU_DDR4		
Size: C	Dept.: ASUSTeK COMPUTER INC	Engineer: NB1 RD EE
Date: Friday, November 06, 2020	Sheet 4 of 104	

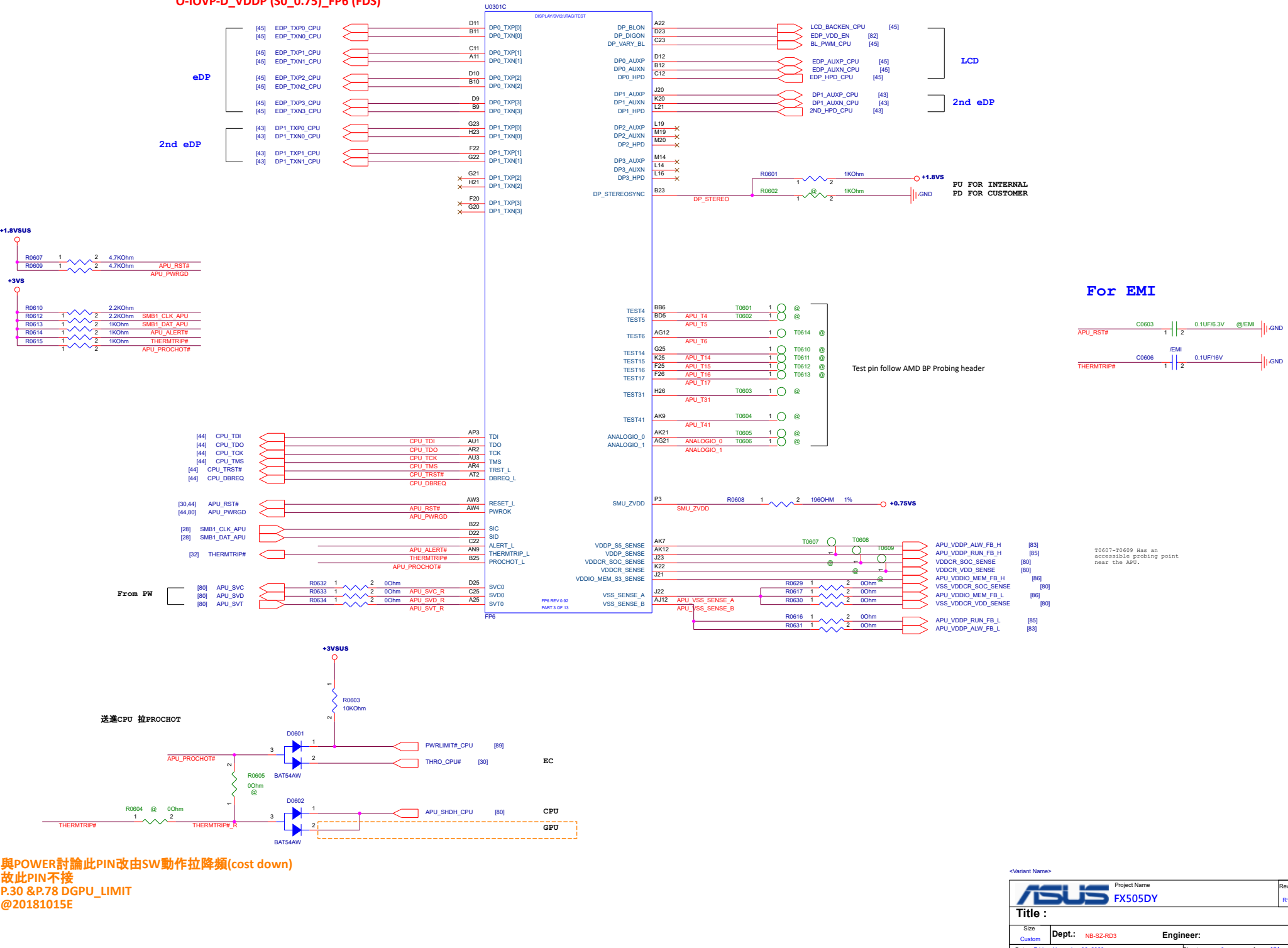
CPU_GND



Project Name: FX505DY		Rev: R1.0
Title : AMD_CPU_GND		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: RD2 EE3	
Date: Friday, November 06, 2020	Sheet 5 of 104	

Display

Display Port TX/RX
O-IOVP-D_VDDP (S0_0.75)_FP6 (FDS)



T0607-T0609 Has an accessible probing point near the APU.

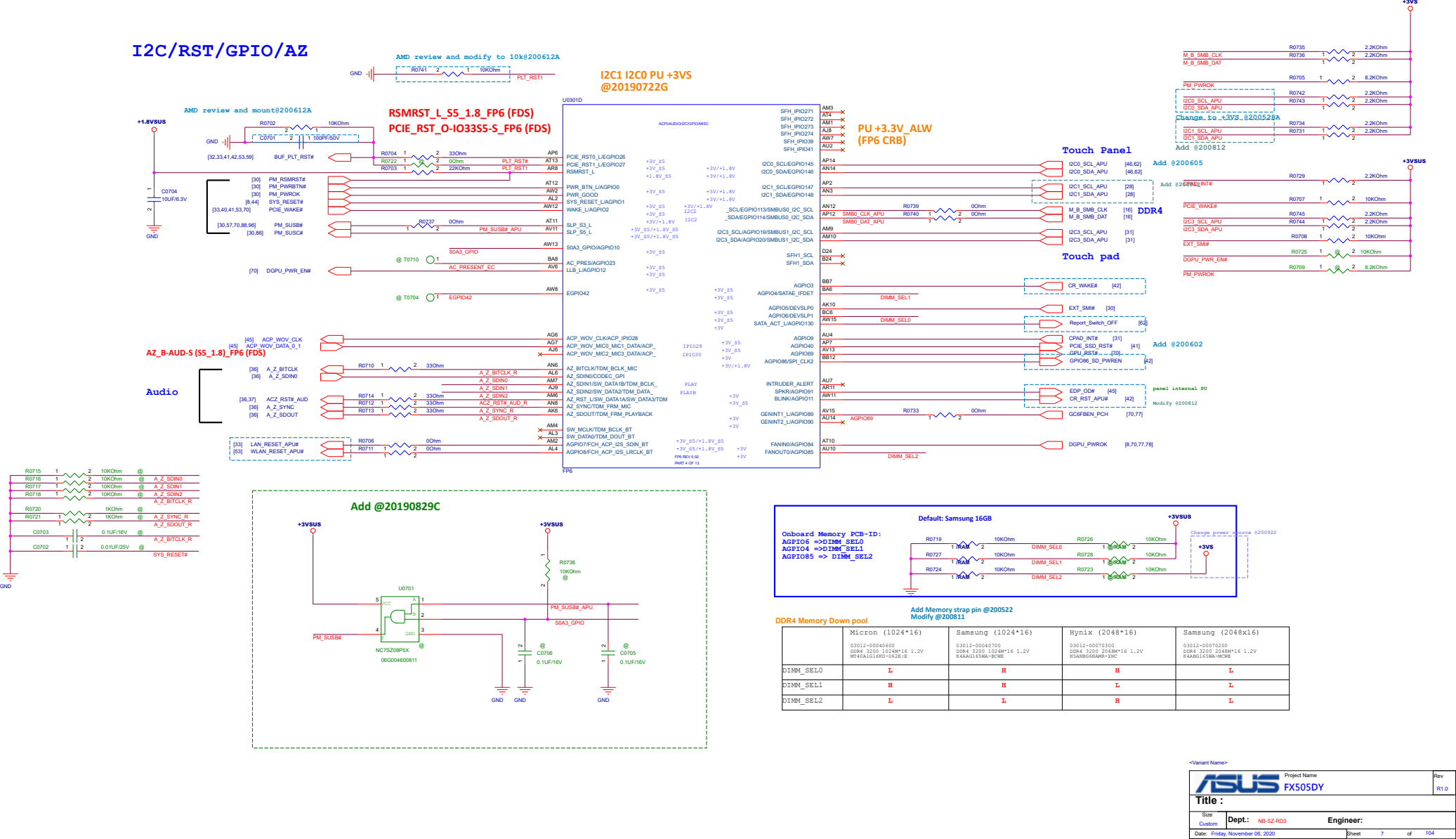
For EMI

與POWER討論此PIN改由SW動作拉降頻(cost down)
故此PIN不接
P.30 &P.78 DGPU_LIMIT
@20181015E

<Variant Name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title :		
Size: Custom	Dept.: NB-SZ-RD3	Engineer:
Date: Friday, November 06, 2020	Sheet 6 of 104	

I2C/RST/GPIO/AZ



DDR4 Memory Down pool

	Micron (1024*16) 03012-00040600 DDR4 3200 1024M*16 1.2V MT40A1G16KD-062E:E	Samsung (1024*16) 03012-00040700 DDR4 3200 1024M*16 1.2V K4AAG165WA-BCWE	Hynix (2048*16) 03012-00070300 DDR4 3200 2048M*16 1.2V H5ANBG8NAMR-XNC	Samsung (2048x16) 03012-00070200 DDR4 3200 2048M*16 1.2V K4ABG165WA-MCWE
DIMM_SEL0	L	H	H	L
DIMM_SEL1	H	H	L	L
DIMM_SEL2	L	L	H	L

<Variant Name>

Project Name: FX505DY		Rev: R1.0
Title :		
Size: Custom	Dept.: NB-SZ-RD3	Engineer:
Date: Friday, November 06, 2020	Sheet 7 of 104	

CPU CLK

DGPU CLKReq#

For Optimus

Q0801 2N7002K

CLKREQ0_GPU#

R0811 10KOhm

[7,70,77,78] DGPU_PWROK

GND

CLK_REQ
B-IO33-S (S0_3.3)_FP6 (FDS)

+3VS

R0824 R0801 R0812 R0802 R0803 R0804 10KOhm

[70] CLKREQ0_GPU#
[30] HID_DIAL_INT#
[33] CLKREQ2_LAN#
[42] CLKREQ3_CR#
[41] CLKREQ4_SSD1#
[40] CLKREQ5_SSD2#
[53] CLKREQ6_WLAN#

U0301E

CLK_REQ0_L/SATA_IS0_L/
CLK_REQ1_L/AGPIO115
CLK_REQ2_L/AGPIO116
CLK_REQ3_L/SATA_IS1_L/
CLK_REQ4_L/OSCIN/EGPIO132
CLK_REQ5_L/EGPIO120
CLK_REQ6_L/EGPIO121

SATA_2PO_L/AG
SATA_2P1_L/EG

GPU
LAN
CR
SSD1
SSD2
WLAN

[70] CLK0_PCIE_PEG_VGA
[70] CLK0_PCIE_PEG#_VGA

[33] PCIE_LAN_CLKP
[33] PCIE_LAN_CLKN
[42] PCIE_CR_CLKP
[42] PCIE_CR_CLKN
[41] PCIE_SSD1_CLKP
[41] PCIE_SSD1_CLKN
[40] PCIE_SSD2_CLKP
[40] PCIE_SSD2_CLKN
[53] PCIE_WLAN_CLKP
[53] PCIE_WLAN_CLKN

GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
GPP_CLK4P
GPP_CLK4N
GPP_CLK5P
GPP_CLK5N
GPP_CLK6P/WIFIBT_CLKP
GPP_CLK6N/WIFIBT_CLKN

PCIE CLK P/N
後端記得預留0 ohm

GPP_CLK
O-IOVP-D_VDDP (S0_0.75)_FP6 (FDS)

X48M_OSC
X48M_X1
X48M_X2

48M_X1
48M_X2

X48M_X1/X2
I-IOVPS5-S_VDDP (S5_0.75)_FP6 (FDS)

RTCCLK
O-IO18S5-S (S5_1.8)_FP6 (FDS)

R0813 R0814 0Ohm

RSVD_71
RSVD_70

RTC_CLK

C0803 C0805 15PF/50V

32K_X1
32K_X2
32K_X2_R

XT0802 32.768Khz

R0810 20MOhm

SL0805

X32K_X1
X32K_X2

X32K_X1/X2
I-RTC-S_VDDBT_RTC_G (G3_3)_FP6 (FDS)

EGPIO70
LPC_PD_L/AGPIO21
LAD0/ESPI1_DATA0/EGPIO104
LAD1/ESPI1_DATA1/EGPIO105
LAD2/ESPI1_DATA2/EGPIO106
LAD3/ESPI1_DATA3/EGPIO107
LPCCLK0/EGPIO74
LPC_CLKRUN_L/AGPIO88
LPCCLK1/EGPIO75
SERIRQ/AGPIO87
LFRAME_L/EGPIO109
LPC_RST_L/AGPIO32
AGPIO68
LPC_PME_L/AGPIO22

SPI_ROM_REQ/EGPIO67
SPI_ROM_GNT/EGPIO76
ESPI_RESET_L/KBRST_L/AGPIO129
ESPI_ALERT_L/LDRQ0_L/EGPIO108

SPI_CLK/ESPI_CLK
SPI_DI/ESPI_DATA
SPI_DO
SPI_WP_L/ESPI_DAT2
SPI_HOLD_L/ESPI_DAT3
SPI_CS1_L
SPI_CS2_L/ESPI_CS_L/AGPIO30
SPI_CS3_L/AGPIO31
SPI_TPM_CS_L/AGPIO29

EGPIO141/UART0_RXD
EGPIO143/UART0_TXD
EGPIO142/UART0_RTS_L/UART1_RXD
EGPIO140/UART0_CTS_L/UART1_TXD
AGPIO144/SHUTDOWN_L/UART0_INTR

FP6

AMD review and unmount@200612A

+3VS

INT_SERIRQ R0822 10KOhm

+3VSUS

HDMI_HPD_EN_dGPU# R0828 R0830 10KOhm
DP_HPD_event#

Add @200612

DP_HPD_event# [78]

R0829 0Ohm

EGPIO104-107_S0_1.8/3.3_FP6 (FDS)

2ND_TOUCH_REST# [62]
HDMI_HPD_EN_dGPU# [78]

R0825 R0827 0Ohm
EGPIO_70
AGPIO21

LPC

EGPIO74/75_S0_1.8/3.3_FP6 (FDS)
AGPIO88_S5_1.8/3.3
EGPIO109_S5_1.8/3.3
APGIO32_S5_1.8/3.3_FP6 (FDS)

LPC_LAD0 [30,44]
LPC_LAD1 [30,44]
LPC_LAD2 [30,44]
LPC_LAD3 [30,44]
LPC_CLK0 [30]
LPC_CLKRUN# [30]
LPC_CLK1 [44]
INT_SERIRQ [30]
LPC_FRAME# [30,44]

R0805 R0806 22Ohm /DEBUG
LPC_CLK0_R
LPC_CLK1_R
LPC_FRAME#

T0804

R0807 33Ohm
LPC_RST#
LPC_RST_L

I2C0_PD_IRQ# [46]
EXT_SCI# [30]

EXT_SCI# R0808 10KOhm +3VSUS

ESI_ALERT_L R0815 10KOhm +3VS
R0823 10KOhm +1.8VS

ANT_SW2_VC1_APU [49]
ANT_SW2_VC2_APU [49]
Add @200605

RC_IN# [30]

ESI_ALERT_L

R0816 10Ohm

ESPI_CLK

SPI

APU_SPI_CLK [30]
APU_SPI_DI [30]
APU_SPI_DO [30]
APU_SPI_WP# [30]
APU_SPI_HOLD# [30]
APU_SPI_CS1# [30]
ANT_SW1_VC1_APU [49]
ANT_SW1_VC2_APU [49]
Add @200605

LPC_RST#

C0802 150PF/50V

AMD review and mount@200612A

UART0/1_S0_3.3_FP6 (FDS)

UART0_RXD
UART0_RTS
UART0_CTS

T0801 T0802 T0805 T0806

UART0_TXD [44]

R0826 0Ohm

2ND_TOUCH_INT# [62]

Add @200602

design guide pull high

+1.8VSUS +3VSUS

R0819 R0817 10KOhm

APU_SPI_CLK

[7,44] SYS_RESET#

R0820 2KOhm
R0818 2KOhm

GND

WLAN_SUS_CLK Update

+3VSUS

C0806 0.1UF/25V

U0801

[40,41,53] SUS_CLK

MC74VHC1G04DFT2G

RTC_CLK

R0821 0Ohm

XTAL

OK

1MOhm R0809

SL0802

XT0801 48MHZ

DC

C0804 5.6PF/50V
C0801 5.6PF/50V

<Variant Name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Friday, November 06, 2020	Sheet 8 of 104	

CPU_CAP

+APU_VDDCORE_RUN

+VDDCR_VDD

7pcs 22UF /1pcs 1uF/1pcs 180pF
@20190614E

16pcs 22UF /1pcs 180pF

All BU(on bottom side under SOC)

C10101 C10100 C1099 C1098 C1097 C1001 C1002 C1003 C1004 C1005 C1006 C1007 C1008 C1009 C1010 C1011 C1012 C1013 C1014 C1015 C1016 22UF/6.3V

C1017 180PF/50V

GND

Add to follow simulation suggest @200721A

+APU_VDDSOC_RUN

+VDDCR_SOC

C1018,C1022,C1020 change to 22uF
@20190614E

All BU(on bottom side under SOC)

C1018 C1019 C1021 C1022 C1020 C1023 C1024 22UF/6.3V

C1025 1UF/6.3V

C1026 180PF/50V

GND

Follow FP6 CRB
@20190614E

C1083,C1082,C1067C1066C1065 change to unmount
@20190614E

+1.2V PI 模擬後的修改 total 5 close to CPU

+1.2V

+APU_VDDIO_SUS

9pcs 22uF /2pcs 1uF/1pcs 180pF

All BU(on bottom side under SOC)

C1083 4.7UF/6.3V

C1082 10UF/6.3V

C1067 47UF/4V

C1066 1UF/6.3V

C1065 22UF/6.3V

C1027 C1028 C1029 C1030 C1031 C1032 C1033 C1034 C1035 22UF/6.3V

C1036 C1037 1UF/6.3V

C1038 180PF/50V

0402 0402 0603

GND

+1.2V

+APU_VDDIO_SUS

ACROSS VDDIO AND VSS SPLIT

DECOUPLING BETWEEN PROCESSOR AND DIMMs

C1039 C1040 C1041 C1042 0.22UF/25V

C1043 180PF/50V

C1081 180PF/50V

4pcs 0.22uF / 2pcs 180pF

All BU(on bottom side under SOC)

GND

+APU_VDDCORE_RUN

+VDDCR_VDD

TBD

4pcs 0.22uF / 2pcs 180pF

C1044 C1045 C1046 C1047 0.22UF/25V

C1048 180PF/50V

C1049 180PF/50V

GND

DECOUPLING BETWEEN PROCESSOR AND DIMMs ACROSS VDDIO AND VSS SPLIT

+1.2V

+APU_VDDIO_SUS

RESERVED FOR DEBUG

Add @20190617E

C1087 C1088 C1089 C1090 22UF/6.3V

C1091 C1092 C1093 C1094 0.22UF/25V

C1095 0.1UF/6.3V

C1096 0.1UF/6.3V

GND

If the VSS plane is cut to create a VDDIO_MEM_S3 plane, ceramic capacitors with NP0 or C0G dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.

+VDDP change to +0.75VS
@20190704D

+VDDP_ALW

+0.75VSUS_R

1pcs 22uF / 3pcs 1uF

C1050 22UF/6.3V

C1051 C1052 C1060 1UF/6.3V

BO BU

GND

+VDDP_RUN

+0.75VS_R

2pcs 22uF / 8pcs 1uF / 1pcs 180pF

C1053 22UF/6.3V

C1054 22UF/6.3V

C1055 C1056 C1057 C1058 C1059 C1061 C1062 C1063 1UF/6.3V

C1064 180PF/50V

C1057 change to 22uF @201014A

BO BU

GND

1pcs 0.22uF / 1pcs 1uF

+VDD_18_S5 change to +1.8VSUS
@20190704D

Add @20190617D

+1.8V_ALW

+1.8VSUS_R

1pcs 22uF / 2pcs 1uF

C1084 22UF/6.3V

C1085 C1086 1UF/6.3V

BO BU

GND

+1.8V_RUN

+1.8VS_R

1pcs 22uF / 2pcs 1uF

C1068 22UF/6.3V

C1069 C1070 1UF/6.3V

BO BU

GND

+VDDBT_RTC

+3VA_RTC

C1078 0.22UF/25V

C1079 1UF/6.3V

GND

11G232210526360 (1UF/10V) change to 11G232210515320 (1UF/6.3V)
C0902
@20190705C

VDDBT_RTC_G [9,32]

JP1001 SGL_JUMP @

C1071 0.22UF/10V

C1072 1UF/6.3V

GND GND

N1,RPC22UF

AMD review @200612A

+VDD_18 change to +1.8VS
@20190704D

+3.3V_ALW

+3VSUS_R

1pcs 22uF / 2pcs 1uF

C1073 22UF/6.3V

C1074 C1075 1UF/6.3V

BO BU

GND

+3.3V_RUN

+3VS_R

1pcs 22uF / 2pcs 1uF

C1076 22UF/6.3V

C1077 C1080 1UF/6.3V

BO BU

GND

ASUS	Project Name: FX505DY	Rev: R1.0
Title :	CFL-H_CPU_PWR(1)_R1.3B	
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD EE3
Date: Friday, November 06, 2020	Sheet 10 of 104	

Project Name

Type-C_ALT_USB3-10G + DP + PD + Slave_Charger_TI

Rev

R1.0

Title : PD_TPS65993AC

Size	Dept.:	Engineer:
C	ASUSTeK COMPUTER INC.	Design IP

Date:	Sheet	of
Friday, November 06, 2020	11	104

CPU_Power

20A EDC
0.7~1.325V @ 15A TDC

96A EDC
0.3~1.400V 58A TDC

+VDDCR_SOC

+APU_VDDSOC_RUN @15A TDC @20A EDC

+VDDCR_VDD

+APU_VDDCORE_RUN @58A TDC @96A EDC

U0301F

POWER

VDDIO_MEM_S3 @ 6A
1.2±0.06

+1.2V

11G232210526360 (1UF/10V) change to 11G232210515320 (1UF/6.3V)
C0902
@20190705C

BO (Bottom side outside SOC)
BU (on bottom side under SOC)

1pcs 22uF / 1pcs 1uF

C0901 22UF/6.3V
C0902 1UF/6.3V
C0903 22UF/6.3V
BO
BU
GND

R0902 0Ohm
R0904 @ 0Ohm
+VDDIO_VPH

VDDIO_AZ_ALW @ 0.2A

VDDIO_AUDIO:
1.8±0.09

+1.8VSUS
R0906 0Ohm
VDD_33 @ 0.25A
+1.8VS_R
+VDDIO_AUDIO

VDD_33:
3.3±0.165

+3VS
R0908 0Ohm
+3VS_R
+VDD_33

VDD_18 @ 2.5A

VDD_18:
1.8±0.09

+1.8VS
SL0901
+VDD_18

VDD_18_ALW @ 1A

VDD_18_S5:
1.8±0.09

+1.8VSUS
R0909 0Ohm
+1.8VSUS_R
+VDD_18_S5

VDD_33_ALW @ 0.25A

VDD_33_S5:
3.3±0.165

+3VSUS
R0910 0Ohm
+3VSUS_R
+VDD_33_S5

VDDP_S5 @ 2A

VDDP_S5:
0.75±0.0375

+0.75VSUS
SL0902
+0.75VSUS_R
+VDDP_S5

VDDP @ 2A

VDDP:0.75±0.0375

+0.75VS
SL0903
+0.75VS_R
+VDDP

VDDBT_RTC_G:
1.425 ~ 3.465

+3VA_RTC
R0901 1KOhm
VDDBT_RTC_G

[10,32] VDDBT_RTC_G

FP6 REV 0.92
PART 6 OF 13
FP6

RTC Power

+3VA
SL0907
R0905 45.3KOhm
C0907 @10PF/50V
GND
+3VA_RTC_CTL
RTC battery

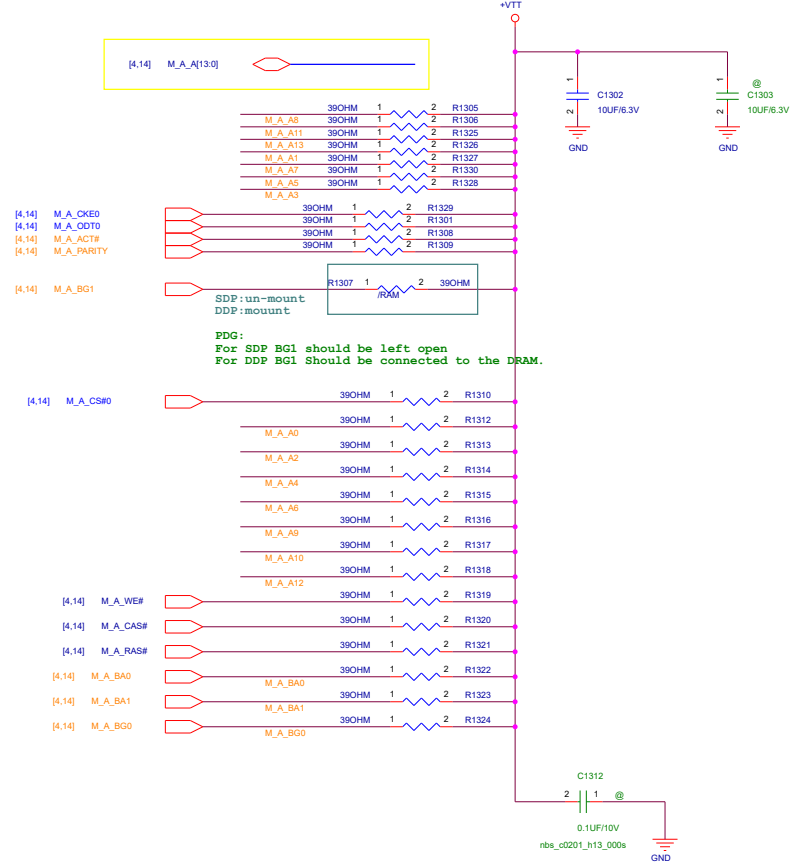
R0903 1K change to 10K (FP6 CRB)
@20190613A

+VCC_RTC
D0902
BAV70_L
+RTCBAT
R0903 10KOhm
+RTC_BAT
BAT0901
SIDE1
SIDE2
WTOB_CON_2P
12G171000002C
C0908 0.1UF/6.3V
C0906 0.1UF/6.3V @

Delete PU0901, C0903, C0904
Add SL0906
@20190613A

+3VA_RTC
SL0906
0603
+VCC_RTC

Project Name: FX505DY			Rev: R1.0
Title: CFL-H_CPU_PWR(1)_R1.3B			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD EE3	
Date: Friday, November 06, 2020	Sheet 9 of 104		



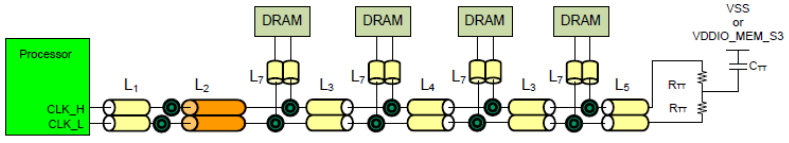
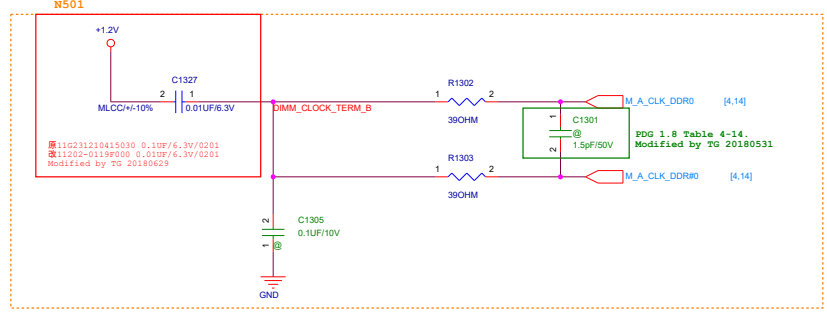


Figure 57. CLK Routing Model (DDR4 x16 DRAM Down)

The termination component values for MA_CLK are listed in Table 40.

Table 40. Component Table—DDR4 x16 CLK Termination

Ref	Value	Tolerance	Package	Comments
R_{TT}	39Ω	5%	0402	CLK termination
C_{TT}	0.1 µF	5%	0402	CLK termination to VSS or VDDIO_MEM_S3. CLK termination must match the CLK reference plane.



Clock Pull up power change from +0.6V to +1.2V (CFL PDG) 20820601

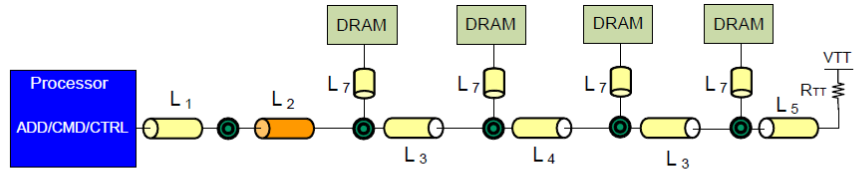


Figure 58. ADD/CMD/CTL Routing Model (DDR4 x16 DRAM Down)

The termination component values for ADD/CMD/CTL are listed in Table 42.

Table 42. Component Table—DDR4 x16 ADD/CMD/CTL Termination

Ref	Value	Tolerance	Package	Comments
R_{TT}	39Ω	5%	0402	ADD/CMD/CTL termination to VTT

<Core Design>

ASUSTeK COMPUTER INC.

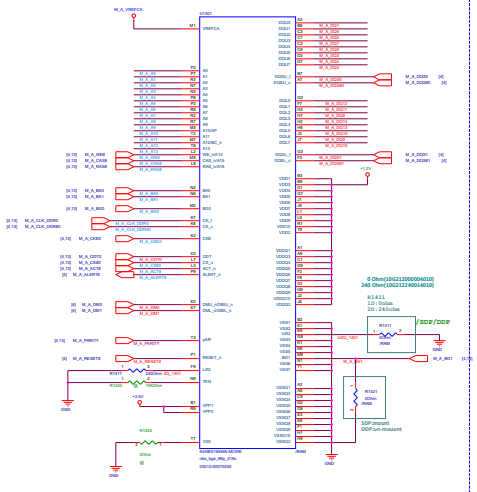
Title : DDR4_TERMINATION

Engineer: EE

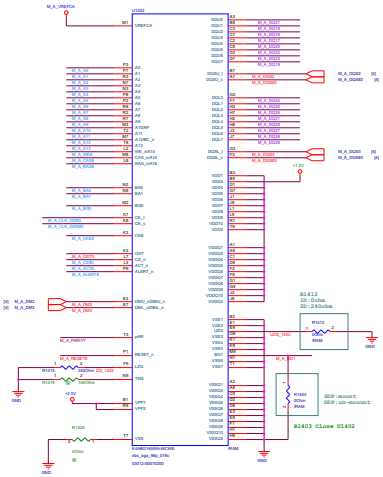
Size	Project Name	Rev
Custom	GX502GX	R1.2

Date: Friday, November 06, 2020 Sheet 13 of 104

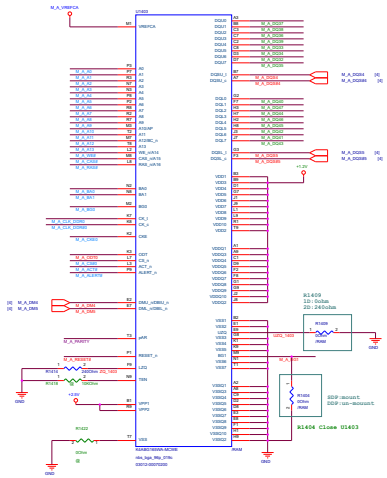
DQS0~DQS1(DQ0~DQ15)



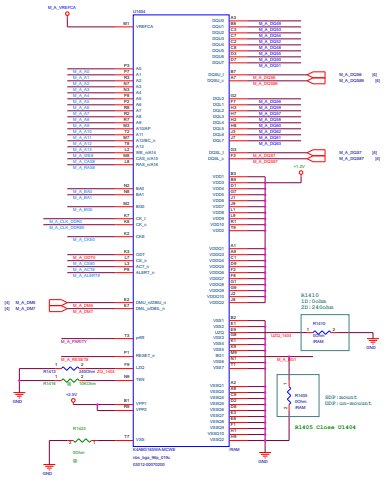
DQS2~DQS3(DQ16~DQ31)



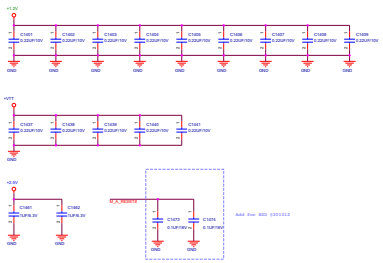
DQS4~DQS5(DQ32~DQ47)



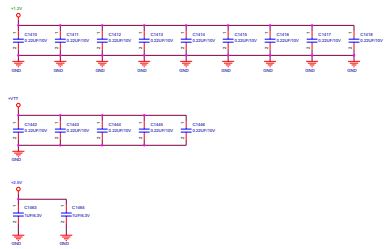
DQS6~DQS7(DQ48~DQ63)



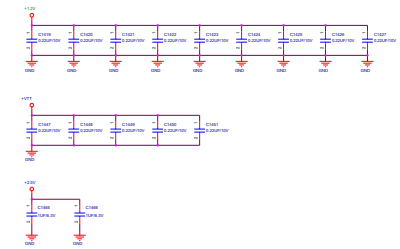
Close U1401



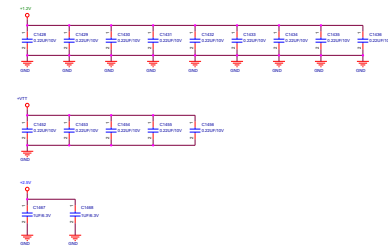
Close U1402



Close U1403



Close U1404



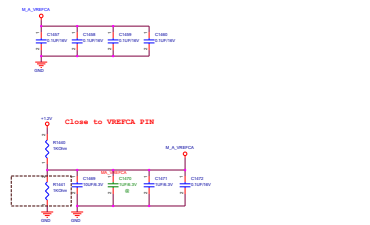
CHANNEL A and B						
MEM VREFCA	Vref Source	Connected to the center of a 50% VDDIO voltage divider network, comprised of:	2	1 k	Ω	1%
VDDIO[1]	Channel A and B Decoupling	Ceramic capacitors connected to VSS.	36	0.22	µF	0402
VTT[1]		Ceramic capacitors connected to VSS and VDDIO.	20	0.22	µF	0402
VREF_CA[1]		Ceramic capacitors connected to VDDIO.	4	0.1	µF	0402

Note: *1. Double the capacitor quantity for DRx16 configuration.*

X16 DDP

7	8	9
UDQS_c	VSSQ	VDDQ
UDQS_t	UDQ1	VDD
UDQ3	UDQ5	VSSQ
UDQ7	VSSQ	VDDQ
LDM_n/LDBI_n	VSSQ	UZQ
LDQ1	VDDQ	LZQ
VDD	VSS	VDDQ
LDQ3	LDQ5	VSSQ
LDQ7	VDDQ	VDD
CK_t	CK_c	VSS
CS_n	RAS_n/A16	VDD
A12/BC_n	CAS_n/A15	BG1
A3	BA1	TEN
A1	A5	ALERT_n
A9	A7	VPP
VSS	A13	VDD

X16 SDP



R1418 1.5K --> 1K (FP6 PR sample)
@20191119F

Title : DDR4_ON-BOARD_A1

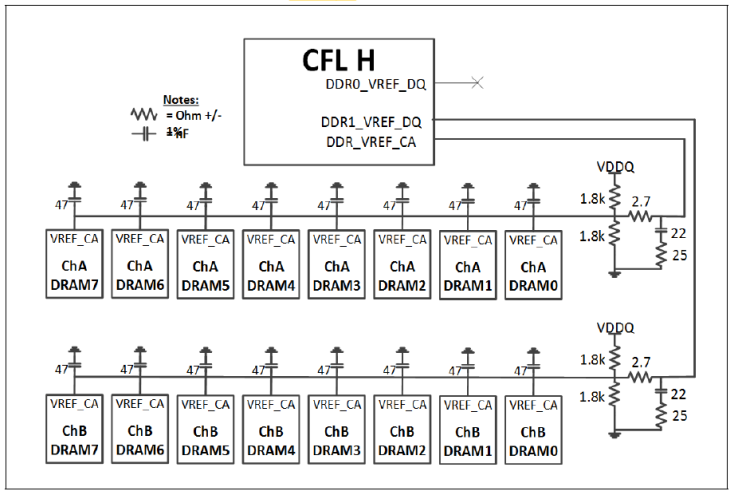
Engineer: EE

GX502GX

Title <Title>		
Size A	Document Number <Doc>	Rev R1.0
Date: Friday, November 06, 2020	Sheet 17 of 104	

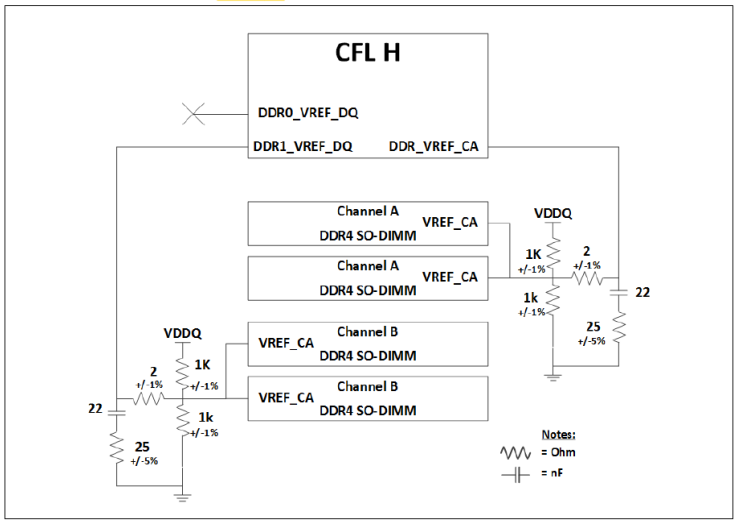
Memory Down Vref

Figure 4-24. CFL-H DDR4 x8 Memory Down V_{REF-CA} Overview



SO-DIMM1 Vref

Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview



ASUS	Project Name: GX531GX	Rev: R1.0
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, November 06, 2020	Sheet 18 of 104	

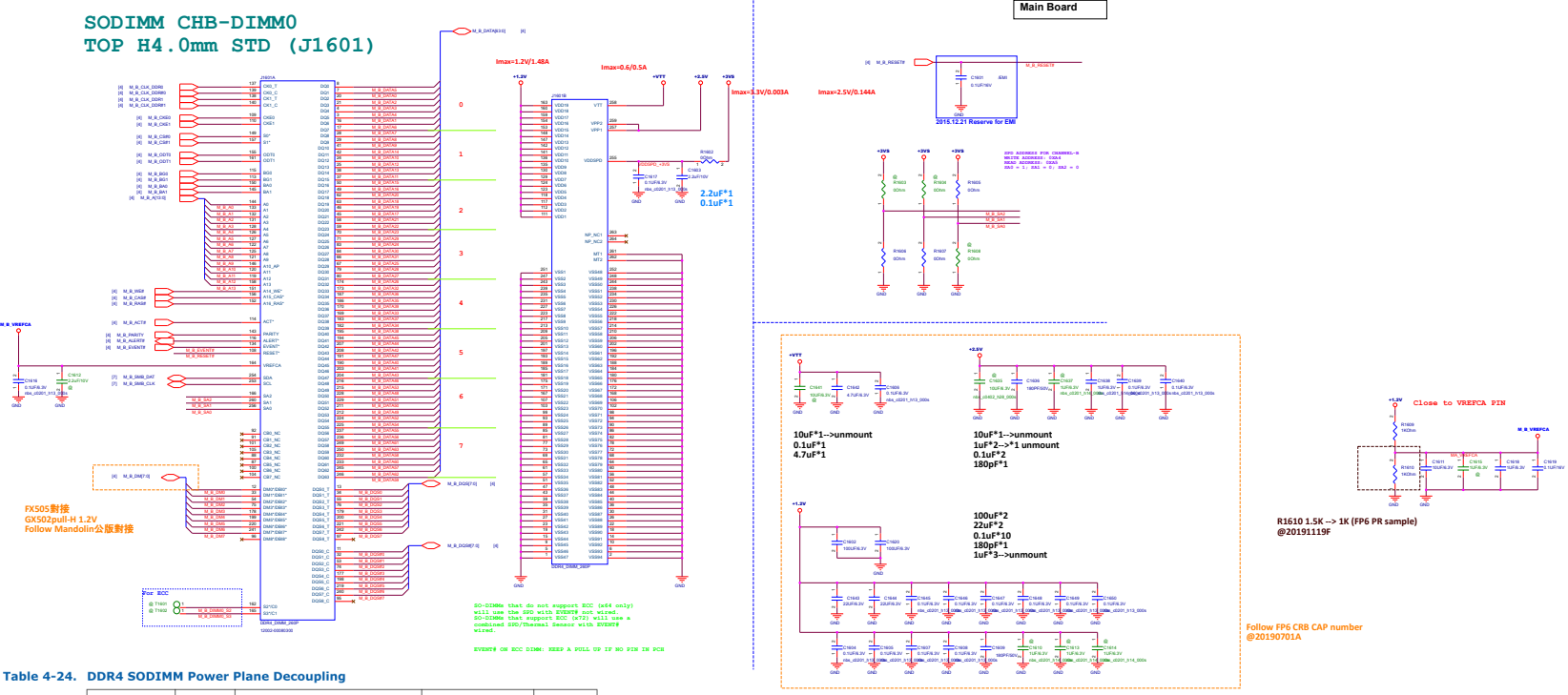


Table 4-24. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10µF (0603)	
		Placed on VTT plane close to DIMM	4x 1µF (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10µF (0603)	
		DIMM Pin side, 1 per DIMM	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0402)	

DDR4 - 2666MHz (8G)
1st : Hynix - 03A08-00051400
2nd : Samsung - 03A08-00051300
DDR4 - 2666MHz (16G)
1st : Hynix - 03A08-00061400
2nd : Samsung - 03A08-00061500

ASUS	Project Name: GA503QS	Rev: 1.0
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
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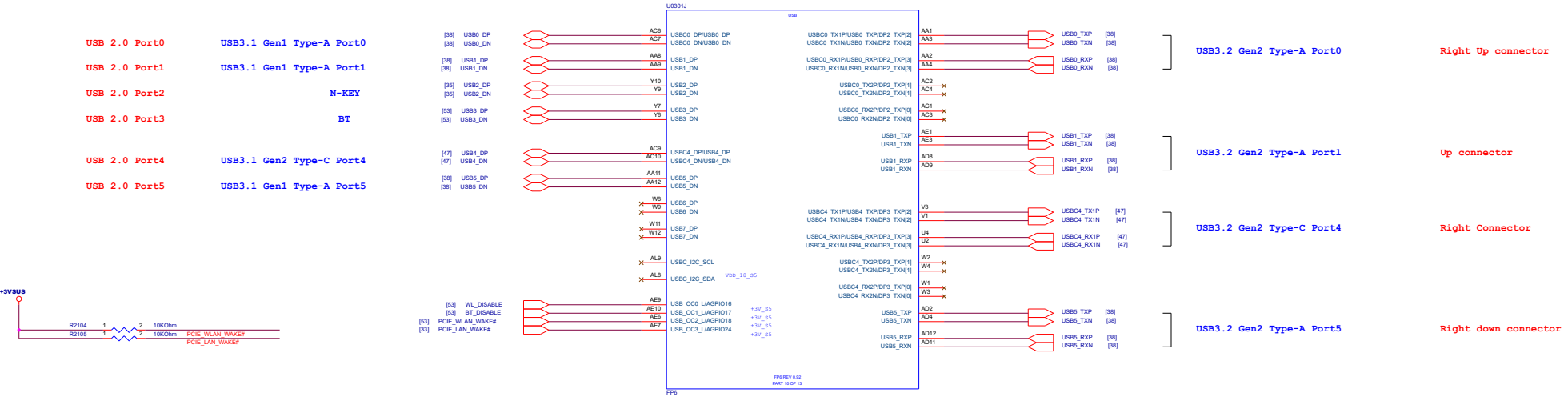
Title <Title>		
Size A	Document Number <Doc>	Rev R1.0
Date: Friday, November 06, 2020	Sheet 20 of 104	

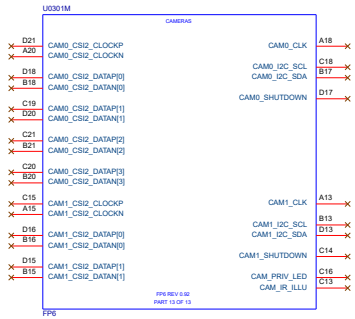
CPU_USB

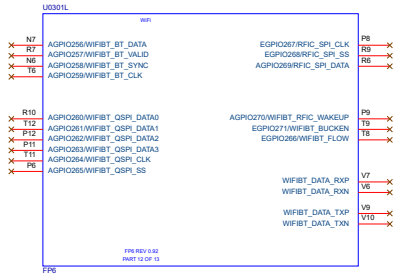
USB3.0 TX/RX
I/O-IOVPS5-D_VDDP (S5_0.75)_FP6 (FDS)



AMD Design check

AGPIO13. If unused, enable internal pull down by software.





<Variant Name>

Project Name: FX505DY		Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Friday, November 06, 2020	Sheet 21 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev R1.0
Date: Friday, November 06, 2020	Sheet 22 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev R1.0
Date: Friday, November 06, 2020	Sheet 15 of 104	

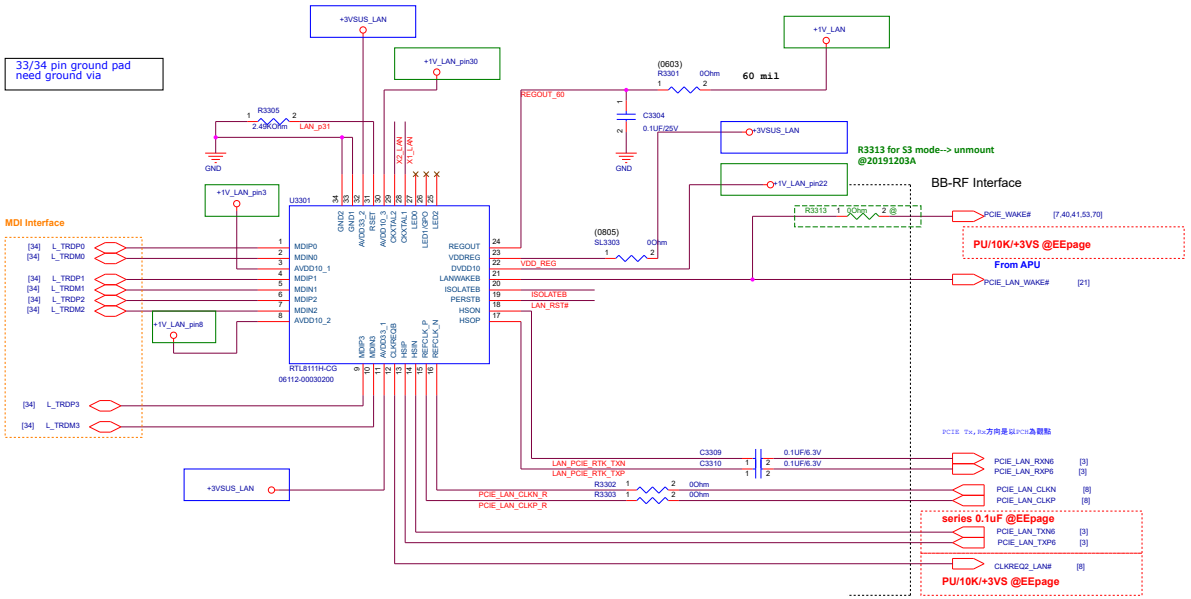
Title <Title>		
Size A	Document Number <Doc>	Rev R1.0
Date: Friday, November 06, 2020	Sheet 23 of 104	

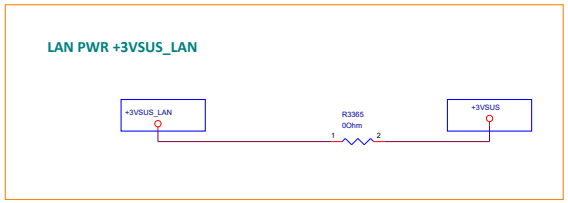
Title <Title>		
Size A	Document Number <Doc>	Rev R1.0
Date: Friday, November 06, 2020	Sheet 24 of 104	

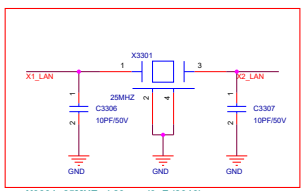
Title <Title>		
Size A	Document Number <Doc>	Rev R1.0
Date: Friday, November 06, 2020	Sheet 25 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev R1.0
Date: Friday, November 06, 2020	Sheet 26 of 104	

Main Board



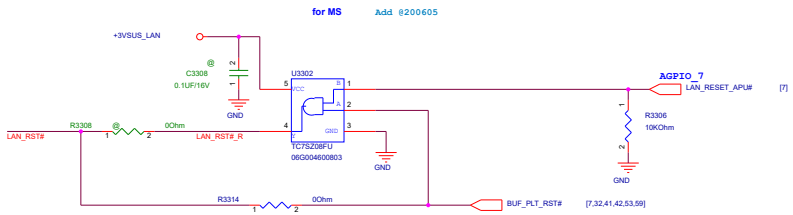


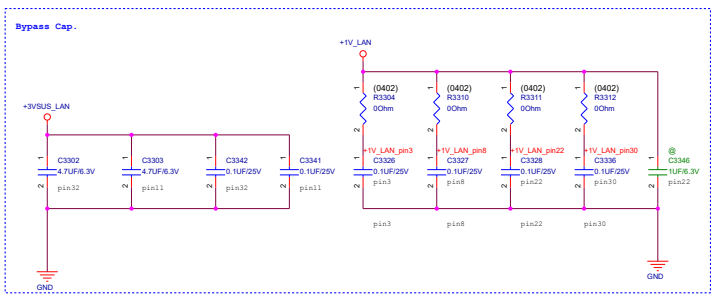


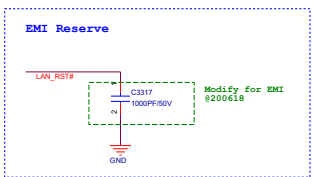
X3301: 25MHZ +/-20ppm/6pF (2016)

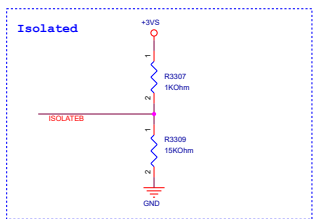
Change to 07009-00026800 20/08/11

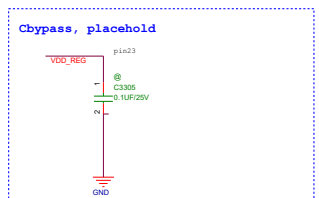
C3306, C3307 change to 10pF to follow vendor suggest @201013







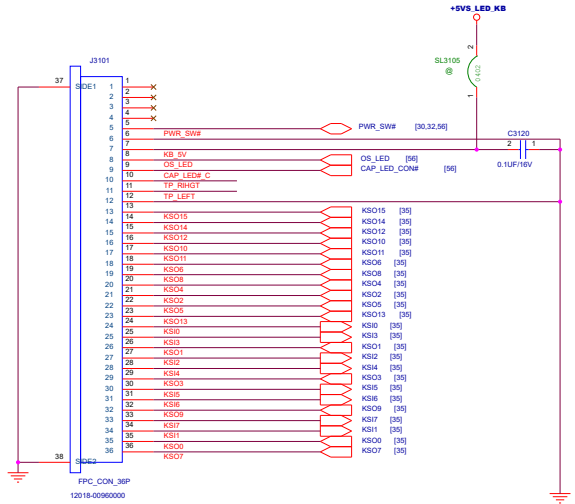




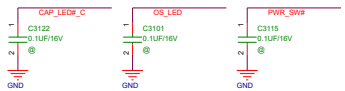
Project Name: GX551Q		Rev: R1.0
Title: LAN RTL8111GUX-CG		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Friday, November 06, 2020	Sheet 33 of 104	

Title <Title>		
Size A	Document Number <Doc>	Rev R1.0
Date: Friday, November 06, 2020	Sheet 29 of 104	

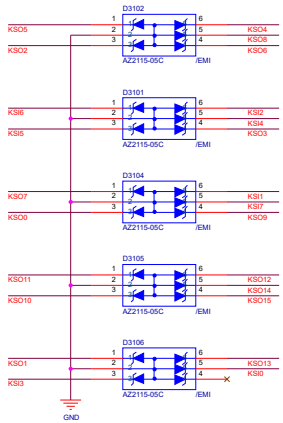
Keyboard Connector



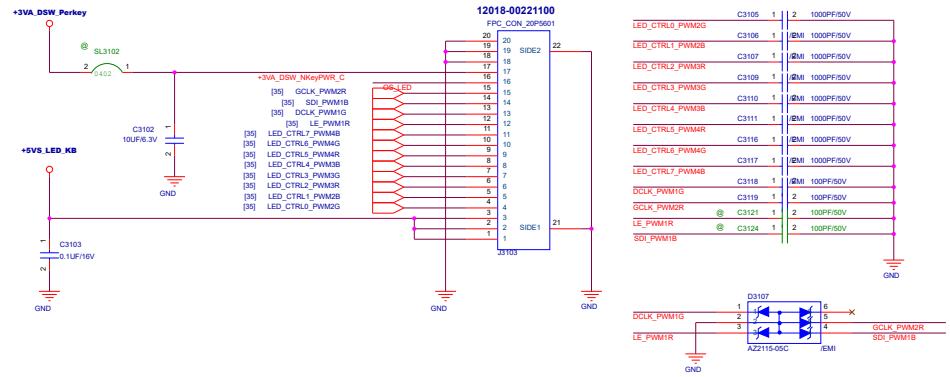
Reserved for EMI



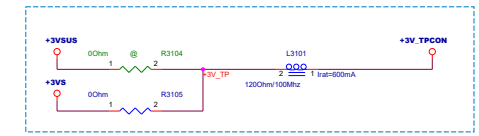
For EMI



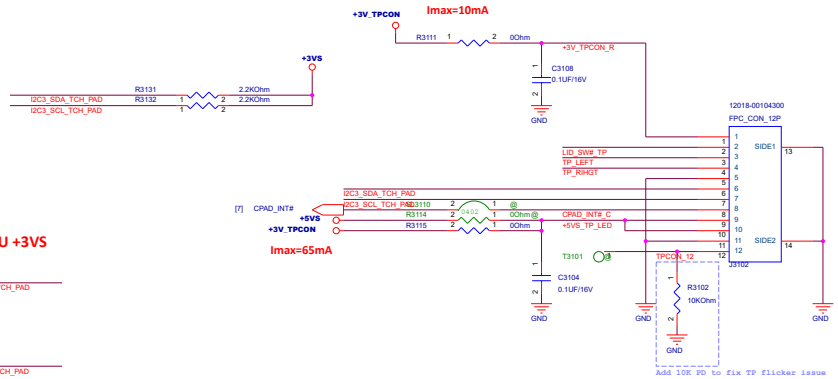
Keyboard LED



Touch Pad / Ten Keys Connector



Add +3V_TPCON option @200521A

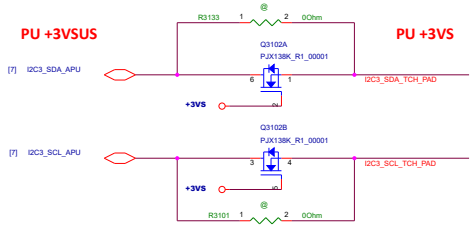


Touch Pad Pin Define

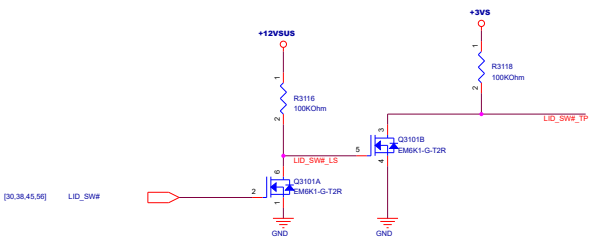
Connector type: 12 pins FFC connector, pitch is 0.5 mm.

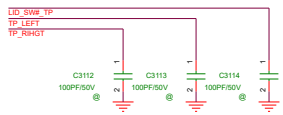
CN1 pin assignment and description

Pin#	Signal	I/O	Description
1	VDD_3.3V	Power	3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.
2	LID_CLOSE	I	Lid close/open pin. Indicates that the lid is closed or opened. Low when lid is closed. High when lid is opened.
3	SWL	I	Low active, left button signal.
4	SWR	I	Low active, right button signal.
5	GND	GND	Ground
6	SDA	I/O	I²C data. I_{DRIVE} or I_{SINK}: 8 mA max.
7	SCL	I/O	I²C clock. I_{DRIVE} or I_{SINK}: 8 mA max.
8	INT	O	Active low, indicates that the touchpad plans to send data to host
9	LED_VDD	Power	Power for LED circuit. 3.3V, driver current: TBD
10	LED_VDD	Power	Power for LED circuit. 3.3V, driver current: TBD
11	GND	GND	Ground
12	LED_CONTROL	I	To lighten the LED when high. High active

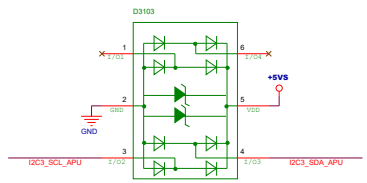


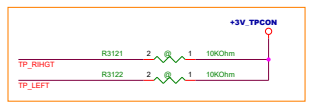
2nd: 12018-00103800





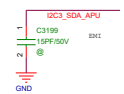
2018/01/04 for EMI Reserved

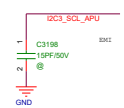


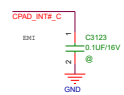


GX501GI R1.0 2017.07.25

Reserved for EMI







<Core Design>

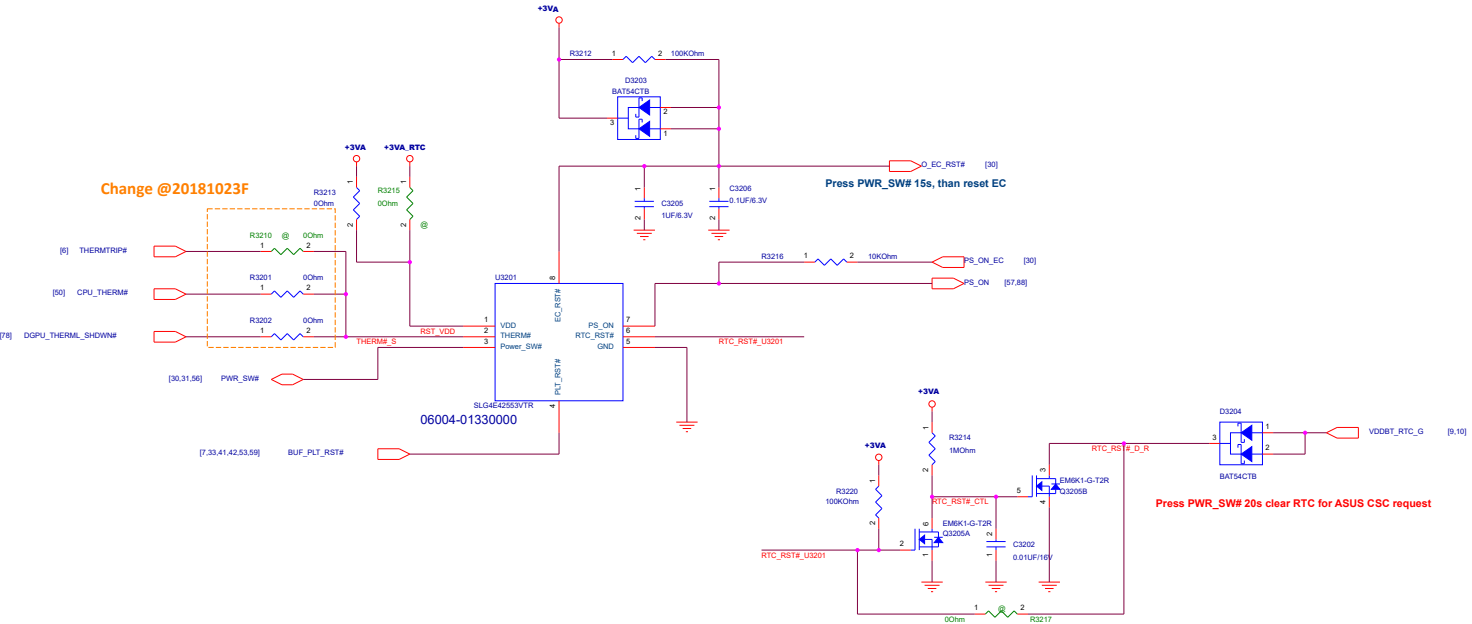
ASUSTeK COMPUTER	Title :	KBC_KB & TP
	Engineer:	EE
Size: C	Project Name: GX551Q	Rev: R1.0
Date: Friday, November 06, 2020	Sheet 31 of 103	

Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

6.6.2 Power button behavior

https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components

UX362FA R1.3 board will verify this circuit 7/E



<Variant Name>

ASUSTeK COMPUTER INC. NB4	Title : RST_Reset Circuit	
	Engineer: SZNB1	
Size: B	Project Name: FX505DY	Rev: R1.0
Date: Friday, November 06, 2020	Sheet 32 of 104	

PCIe x4 SSD_1 --> Lane 8-11
PCIe x2 SSD_2 --> Lane 0-3
@200506

2st NGFF PCIE x4

CPU PCIE

lane 3
lane 2
lane 1
lane 0

PCIE_SSD2_RXN3 / PCIE_SSD2_RXP3
PCIE_SSD2_TXN3 / PCIE_SSD2_TXP3
PCIE_SSD2_RXN2 / PCIE_SSD2_RXP2
PCIE_SSD2_TXN2 / PCIE_SSD2_TXP2
PCIE_SSD2_RXN1 / PCIE_SSD2_RXP1
PCIE_SSD2_TXN1 / PCIE_SSD2_TXP1
PCIE_SSD2_RXN0 / PCIE_SSD2_RXP0
PCIE_SSD2_TXN0 / PCIE_SSD2_TXP0
PCIE_SSD2_CLKN / PCIE_SSD2_CLKP

R4009 0Ohm
R4004 0Ohm
PCIE_SSD2_CLKN_R
PCIE_SSD2_CLKP_R

For AMD checklist @20181018H

Follow FX505DY & 公板
@20181015J

J4001

+3VS_SSD2
R4001 10KOhm
DAS_DSS_LED2#
SATA2_DEVSLP_C
NGFF_PERST#
NGFF2_PEWAKE#
NGFF2_NC1
NGFF2_NC2
NGFF2_SUSCLK

C4002 6PF/25V
C4003 10UF/6.3V
C4004 10UF/6.3V
C4005 10UF/6.3V
C4006 10UF/6.3V
C4007 10UF/6.3V
C4011 0.1UF/6.3V
C4012 0.1UF/6.3V
C4013 0.1UF/6.3V
C4014 0.1UF/6.3V
C4015 0.1UF/6.3V

Add C4009, C4008
@20191009B

C4009 22UF/6.3V
C4008 22UF/6.3V

NGFF_PERST# [41]

CLKREQ5_SSD2# [8]
PCIE_WAKE#_ [7,33,41,53,70]

Q4001 2N7002K

CLKREQ3_SSD2# --> CLKREQ5_SSD2#
@20190624A

R4012 0Ohm
SUS_CLK [8,41,53]

Add @20181013C

MINI_PCI_TAB_REMOVE
12003-00079400

J4001_NGFF M-KEY PCIEx4 Connector H=5.0mm

1st Source: P/N:12003-00162500 ARGOSY/NASM0-S6701-TS50

EMI

NGFF_PERST#
D4001
AZ5825-01F.R7GR

change to 07024-01020000
@200515

NGFF1 Device Sleep

SATA2_DEVSLP_C
R4014 0Ohm
/Enable Devslp

Add @20181219B (EMI request)

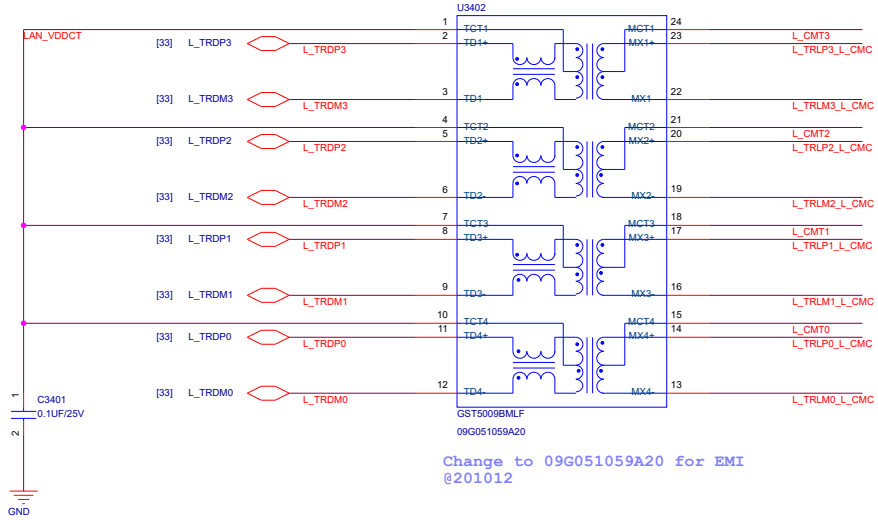
C4017 /EMI 0.1UF/16V
C4016 /EMI 0.1UF/16V
PCIE_WAKE#

[41] DAS_DSS_LED1#
DAS_DSS_LED1#
DAS_DSS_LED2#
R4030 @PCIE 0Ohm
D4006 BAT54AW
R4022 @PCIE 0Ohm
R4060 10KOhm
DAS_DSS_LED# [56]

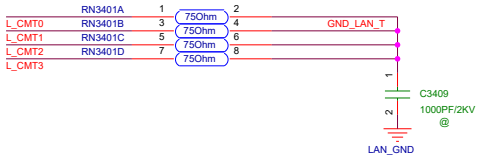
Remove MUX @20181102C

H4002 CT236CB176D146
13020-01379900

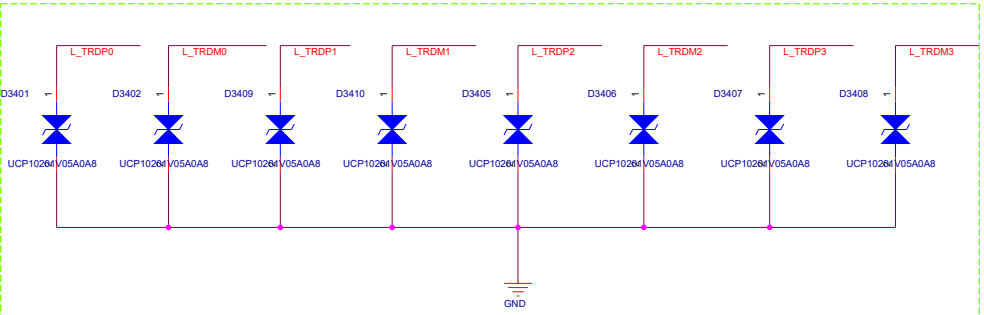
Project Name: GX502GX			Rev: R1.0
Title: NGFF_SSD_PCIE_CON			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1	
Date: Friday, November 06, 2020	Sheet 40 of 104		



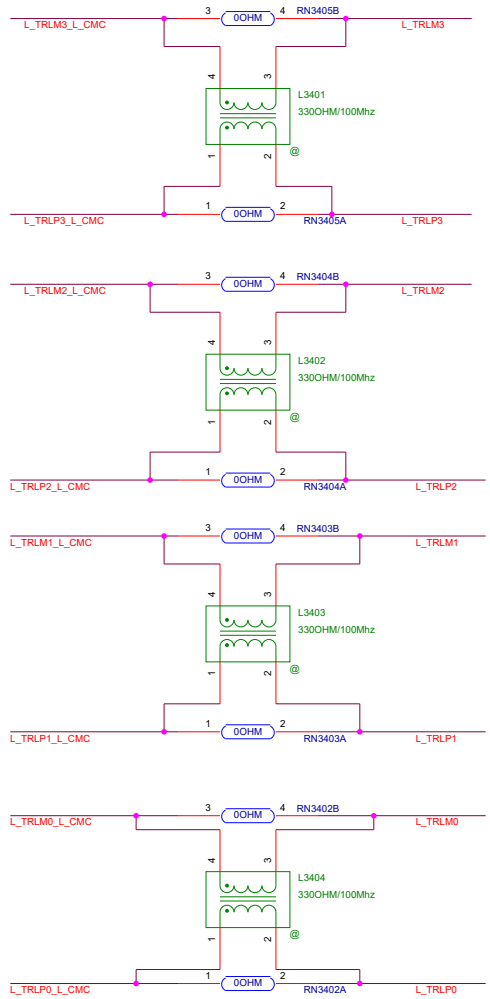
Change to 09G051059A20 for EMI
@201012

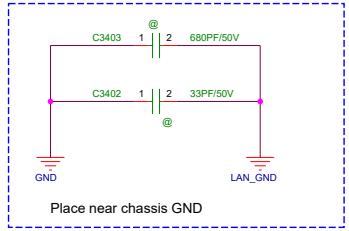


ESD diode change to discrete @0619



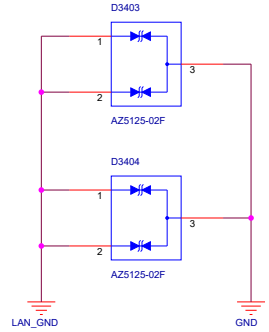
Main Board



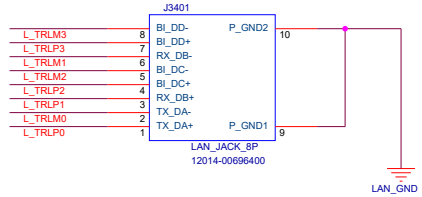


Place near chassis GND

C3402 Change to 33pF mount
@200618
C3402 change to 11204-00747000
@200805



LAN Connector

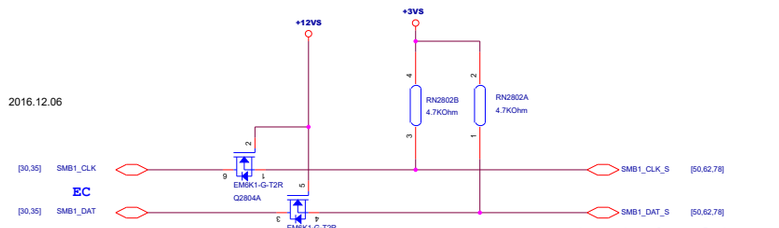


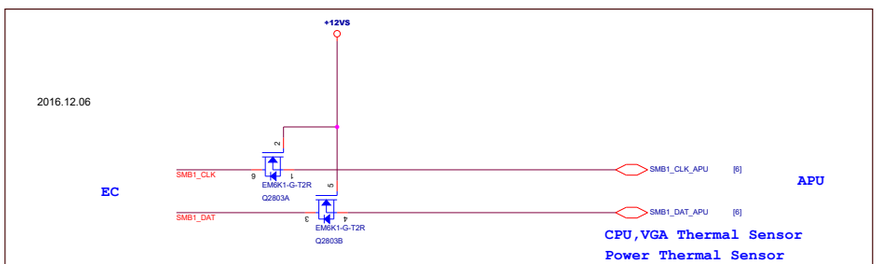
ASUS	Project Name: GU502DU		Rev: 1.0
Title : LAN_RJ45_CON			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1	
Date: Friday, November 06, 2020	Sheet 34 of 104		

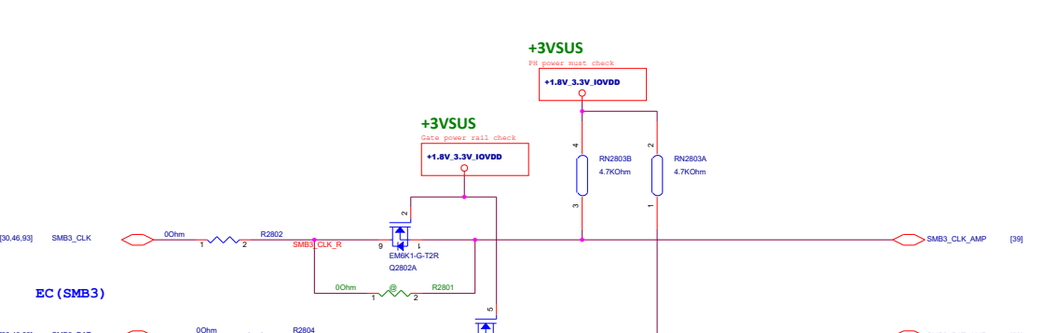
<Variant Name>

Title <Title>		
Size B	Document Number GA401	Rev R1.0
Date: Friday, November 06, 2020	Sheet 27 of 104	

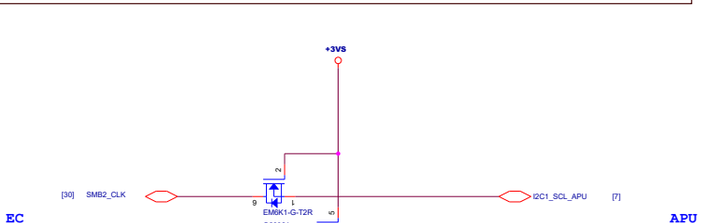
Avoid SIC, SID leakage
@20191119D





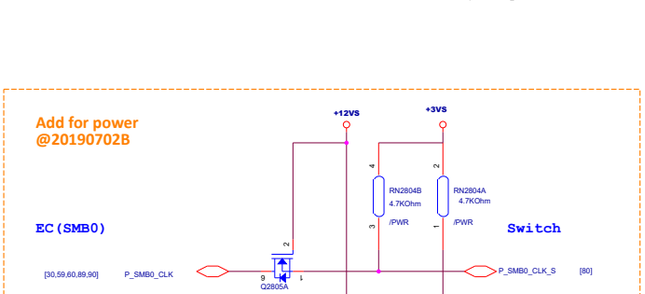


GX501VI R1,1 for smart amp



ASUS Dial @200812

Add for power
@20190702B



RN2804, Q2805 --> mount
@20191016A

NKEY_預留0 OHM對接

EC_PU +3VA

	Isolation		GPU sensor
EC (SMB1)		+3VS	VRAM sensor
			CPU sensor
			HDMI_預留

APU I2C3_PU +3VSUS

DDR4 SO-DIMM_對接

EC (SMB3)

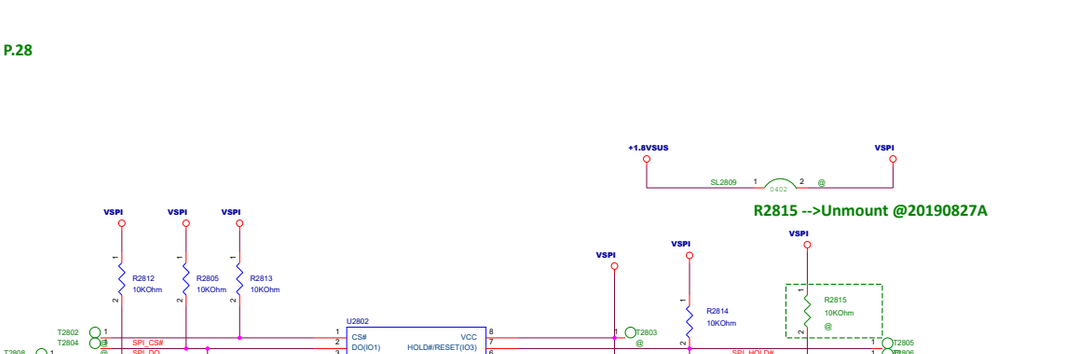
Type-C PD

Slave charger

	Isolation		
EC (SMB3)		+3VSUS	Audio AMP
M_B_SMB_DAT		SMB3_CLK_AMP	

SPI ROM change to P.28
@20190731C

SPI ROM

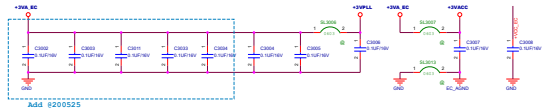


Change to 05006-00096200
@200622
Change to 05006-00096500 for RMC support
@200709
Change to 05006-00096700 for 1.8V solution
@200721

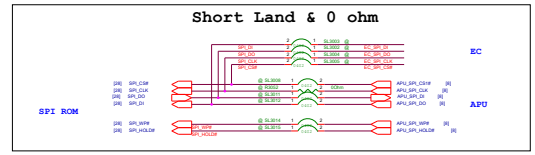
Project Name: GX531GX			Rev: R1.0
Title: PCH-SPI ROM,OTH			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, November 06, 2020	Sheet 28 of 104		

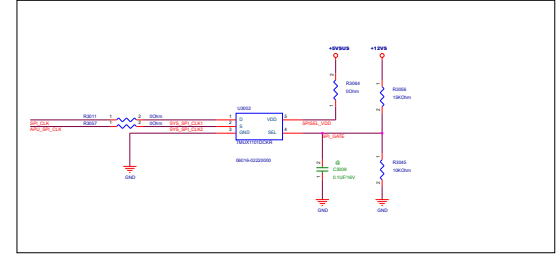
EC Chip - IT8225

EC Power



SPI_CLK 10k change to 10 OHM @20181029G





VCC => +3VS system power ; LPC
VSTBY=>+3VA_EC ;Power supply of EC power

+3VACC==+3VA_EC
+3VAPLL==+3VA_EC_0906

Add @20181219B (EMI request)

C3015 0.1UF --> 0.01UF @20191115A

C3016 0.1UF --> 100PF @20191115A

Change to ITS125VG-192/CX
@200528A

R3018 & R3022 unmount (shipping mode OD test)
@20200427

Del 1.8V_ON_EC NET, 0910

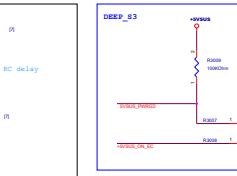
Add R3069 (EC HW Strap Pin)
@20191115A

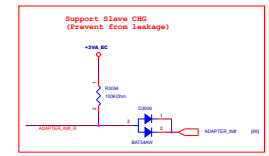
Table 1. TMUX1101 Truth table

SEL	SWITCH STATE
0	OFF (HI-Z)
1	ON

Table 2. TMUX1102 Truth table

SEL	SWITCH STATE
0	ON
1	OFF (HI-Z)





Project Name	FX505YD
Rev	R1.0
Title :	EC
Dept.:	Engineer:
Date: Friday, November 06, 2020	Sheet 30 of 104

*** POWER

** [P.36] +12VS_AUDIO — +12VS_AUDIO

** [P.30] +3VA_EC — +3VA_EC

** [P.36] +1V8_AUD_DVDD_IO — +1V8_AUD_DVDD_IO

*** SINGAL

** Line to Codec [36]

[36] LINE1_R
[36] LINE1_L
LINE1_R
LINE1_L

** Headset from Codec [36]

[36] HPOUT_R
[36] HPOUT_L
HPOUT_R
HPOUT_L

[36] MIC2_VREFO_L — MIC2_VREFO_L
[36] MIC2_L_RING2 — MIC2_L_RING2
[36] MIC2_R_SLEEVE — MIC2_R_SLEEVE
[36] MIC2_VREFO_R — MIC2_VREFO_R

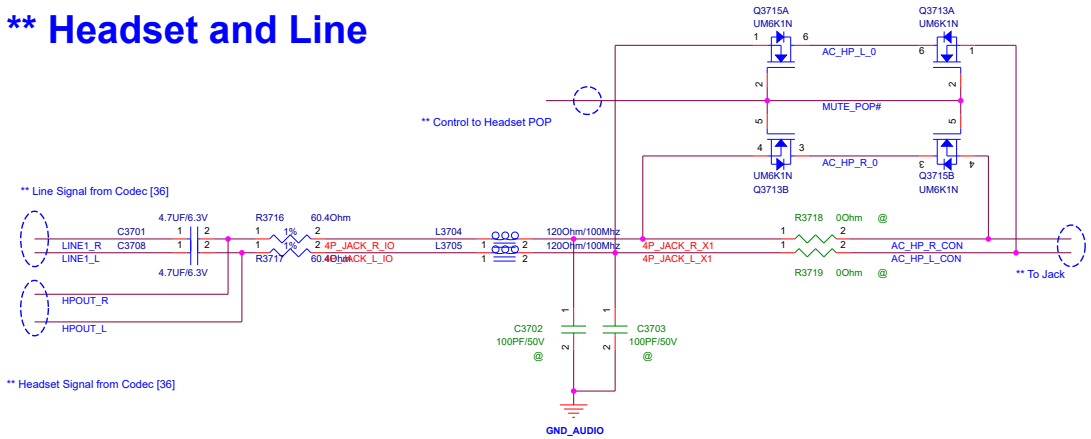
** Control Pin from Codec [36]

[36] EAPD# — EAPD#
[36] TOU_CON_L — TOU_CON_L

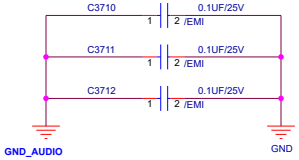
** Control Pin from APU [7]

[7,36] ACZ_RST#_AUD — ACZ_RST#_AUD

** Headset and Line

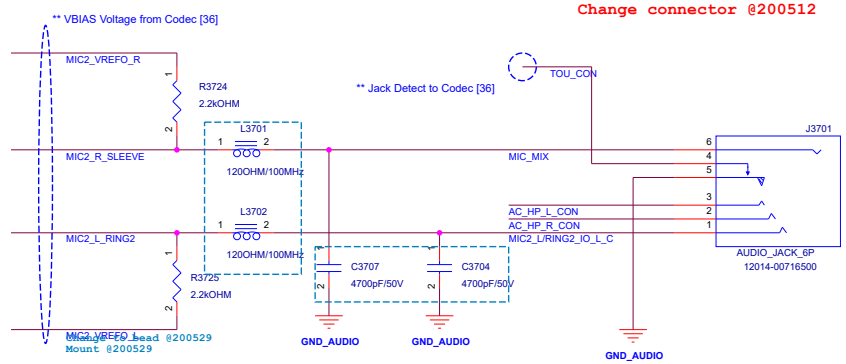


** A_GND / GND

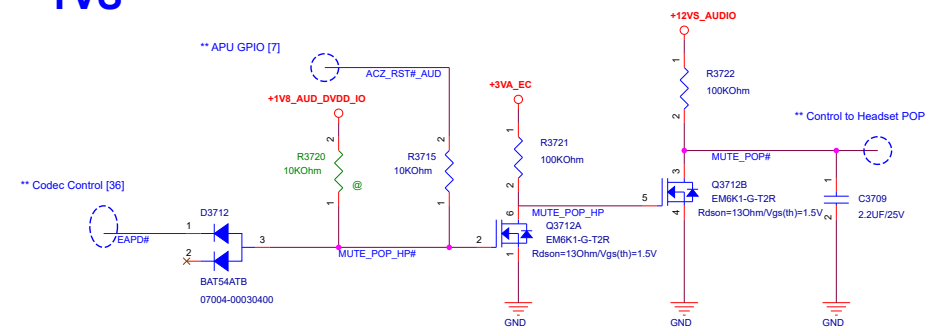


** Jack and MIC

Change connector @200512



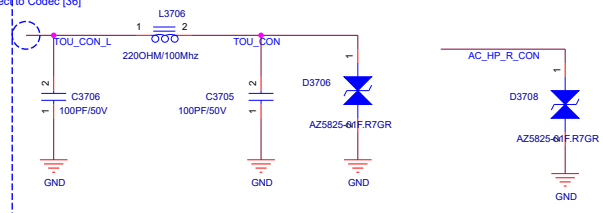
** TVS



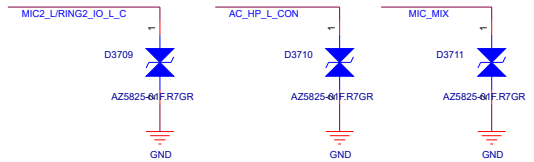
** TVS

HP & MIC Connector

HP ESD Protect



EXTERNAL MICROPHONE



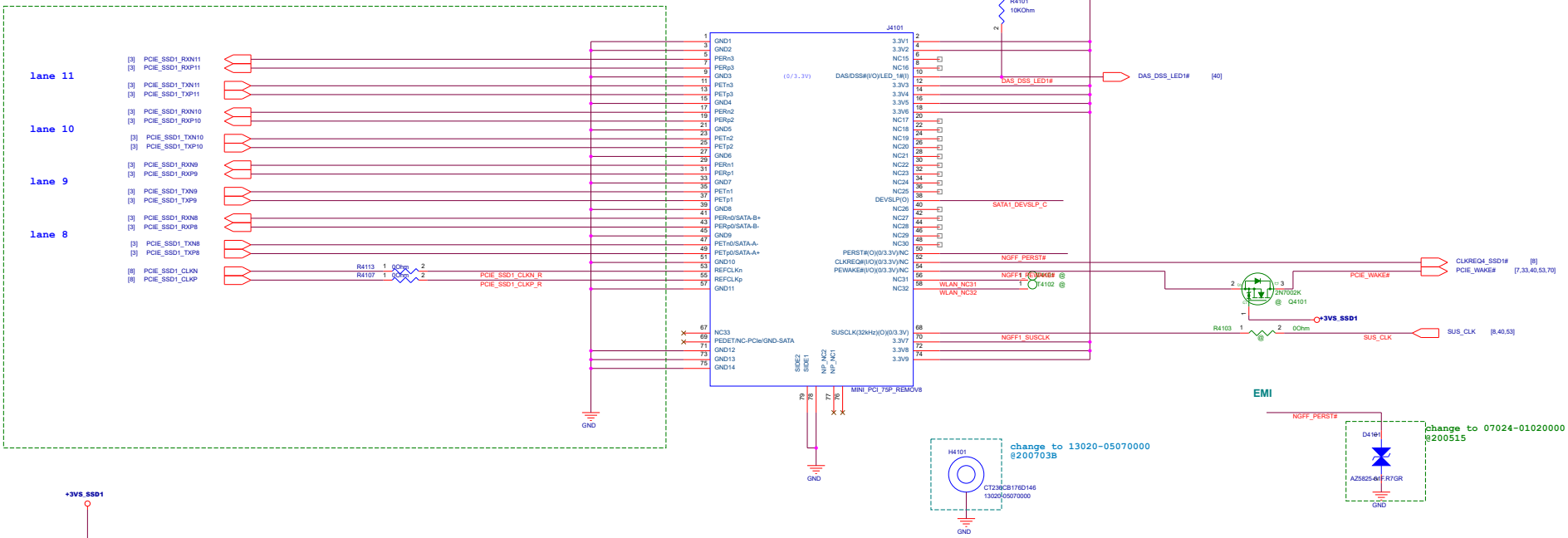
Change to 07024-01152200 for EMI @200522

ASUS	Project Name: GX531GX	Rev: R1.0
Title :	AUDIO ALC3236-CG/VB2 Jack	
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer:
Date: Friday, November 06, 2020	Sheet 37 of 104	

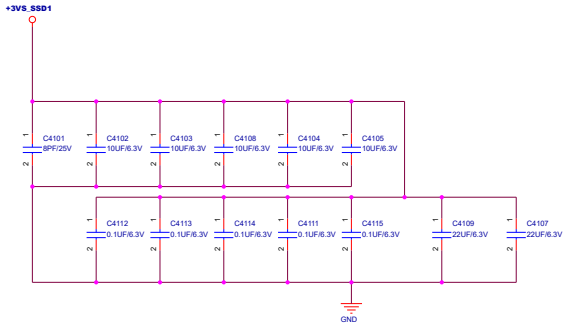
< KEY-M NGFF_SSD >

PCIe x4 SSD_1 --> Lane 8-11
PCIe x2 SSD_2 --> Lane 0-3
@200505

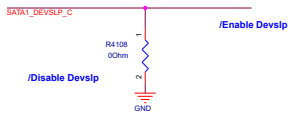
1nd NGFF PCIE x4



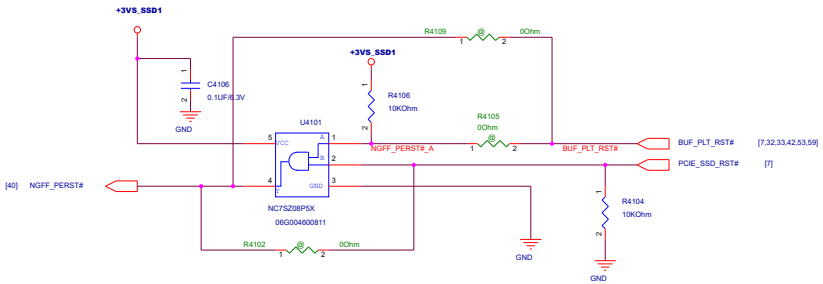
EMI



HW_Control NGFF Device Sleep



Close to Device connector



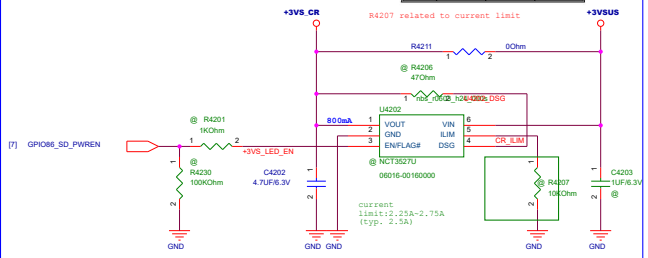
Power_3.3V

for RTD3
for layout placement

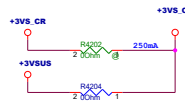
UHS-II consuption
+3VS_CR : 238.4mA(IC)+800mA(Card)=1.1A

Current Limit vs. R_{ILIM} Values

R_{ILIM} (Ω)	Min. Current Limit (mA)	Typ. Current Limit (mA)	Max. Current Limit (mA)
6.98k	2700	3000	3300
7.68k	2430	2700	2970
8.25k	2250	2500	2750
9.53k	1980	2200	2420
10.5k	1800	2000	2200
11.5k	1620	1800	1980
14.3k	1350	1500	1650
17.4k	1080	1200	1320
21k	900	1000	1100



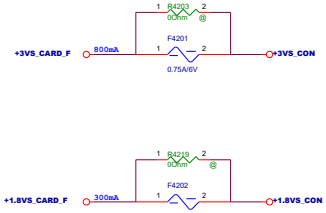
Power_3.3V



RTD3	Support	No Support
R4202	Unmount	Mount
R4204	Mount	Unmount

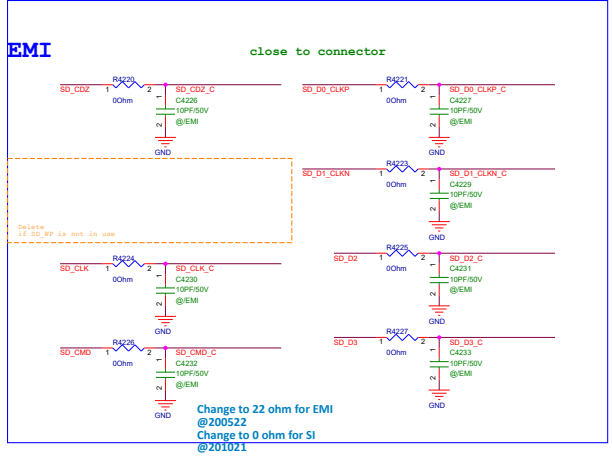
Power_1.2V

Safety

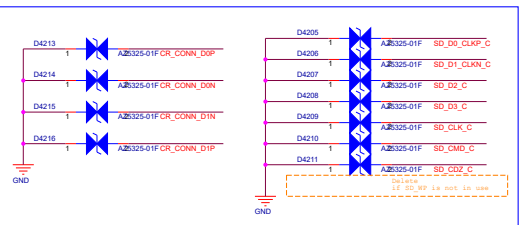


EMI

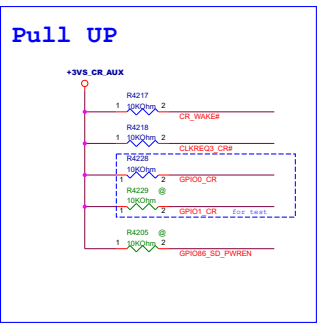
close to connector



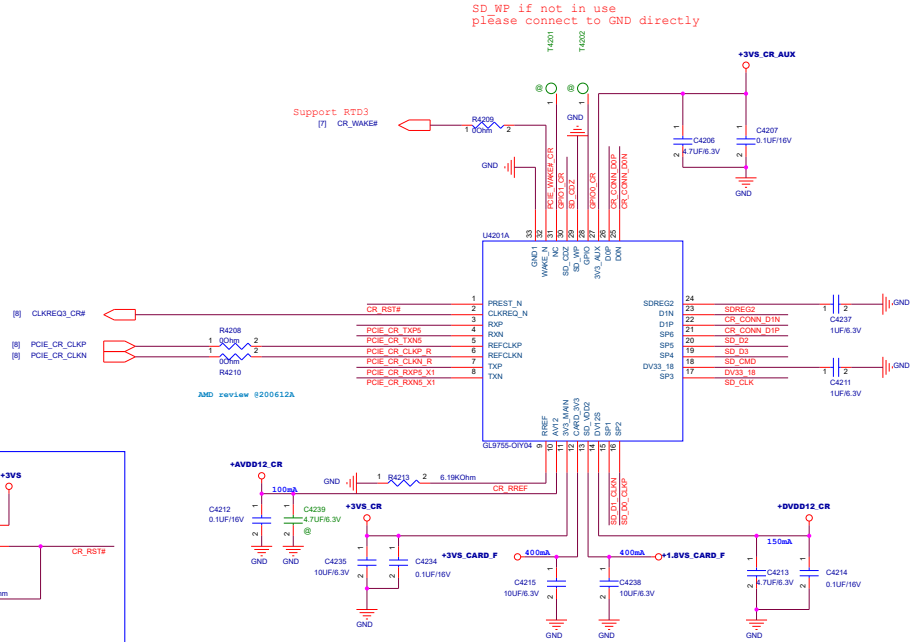
ESD



Pull UP

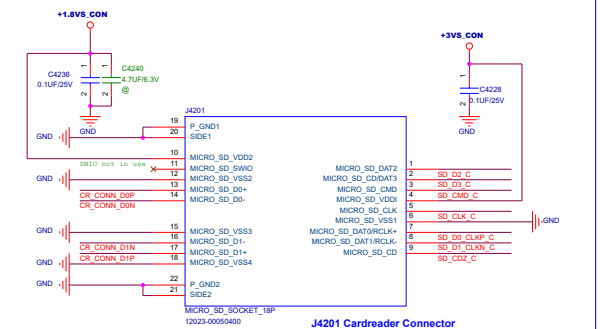


SD_WP if not in use
please connect to GND directly



Micro SD Connector

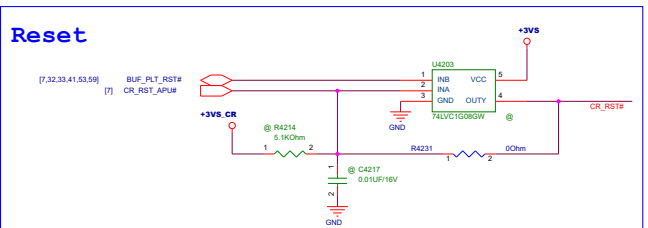
UHS-II:
Differential Impedance is 100ohm.
Differential pair mismatch < 5mil
Ground gap > 20mil.



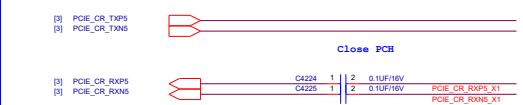
J4201 Cardreader Connector

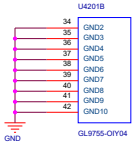
GX551 P/N:12023-00050400 TAISOL/158-2000902612(Default)

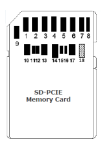
Reset



PCIE







PCIe/NVMe Interface is assigned to pads on the second row as well as sharing some of the pads in the first row.

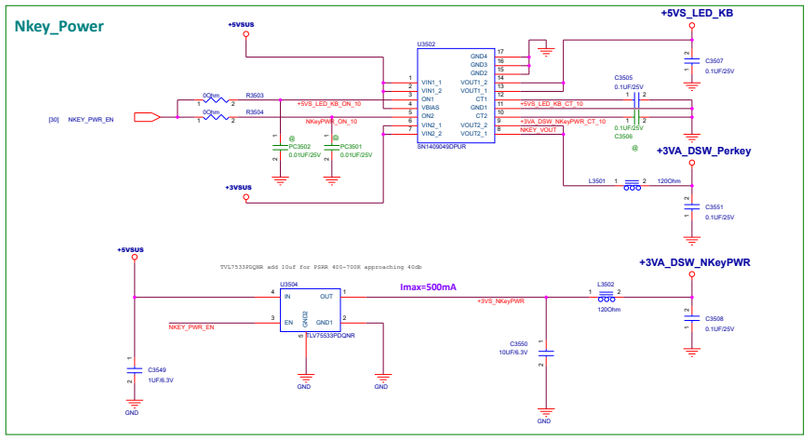
Pin #	Name	Type	Description
1	PERST#	Input signal (active low)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
4	VDD1	Supply voltage	2.7V to 3.6V
7	REFCLK+	Differential Signaling; Input	Clock Input
8	REFCLK-	Differential Signaling; Input	Clock Input
9	CLKREQ#	I/O (active low, open drain)	Reference clock request signal. Also used by L1 PM substates
10	VSS3	Ground	
11	PCIe TX+	Differential Signaling	Card Input
12	PCIe TX-	Differential Signaling	Card Input
13	VSS4	Ground	
14	VDD2	Supply Voltage 2	1.70V to 1.95V
15	PCIe RX-	Differential Signaling	Card Output
16	PCIe RX+	Differential Signaling	Card Output
17	VSS5	Ground	
18*	VDD3	Supply Voltage 3	1.14v to 1.30v

(*) reserved for future optional VDD3 power

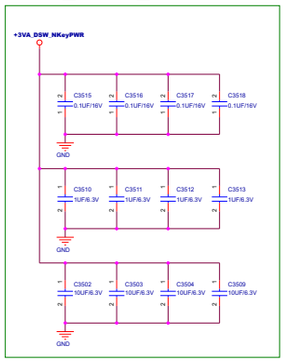
ASUS	Project Name	GX550L	Rev R1.3
Title :	CR_GL9755		
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: TG_Wei	
Date: Friday, November 06, 2020	Sheet 42 of 103		

N_KEY_IT8299E

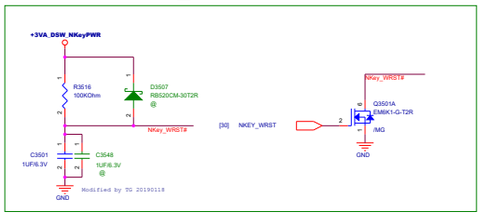
Nkey_Power



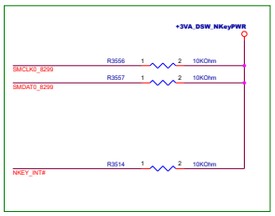
Nkey_Power_Cap



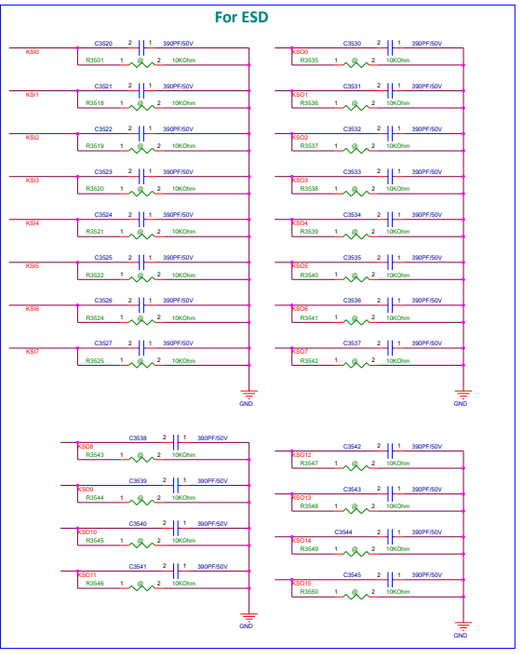
For EC Reset N_key



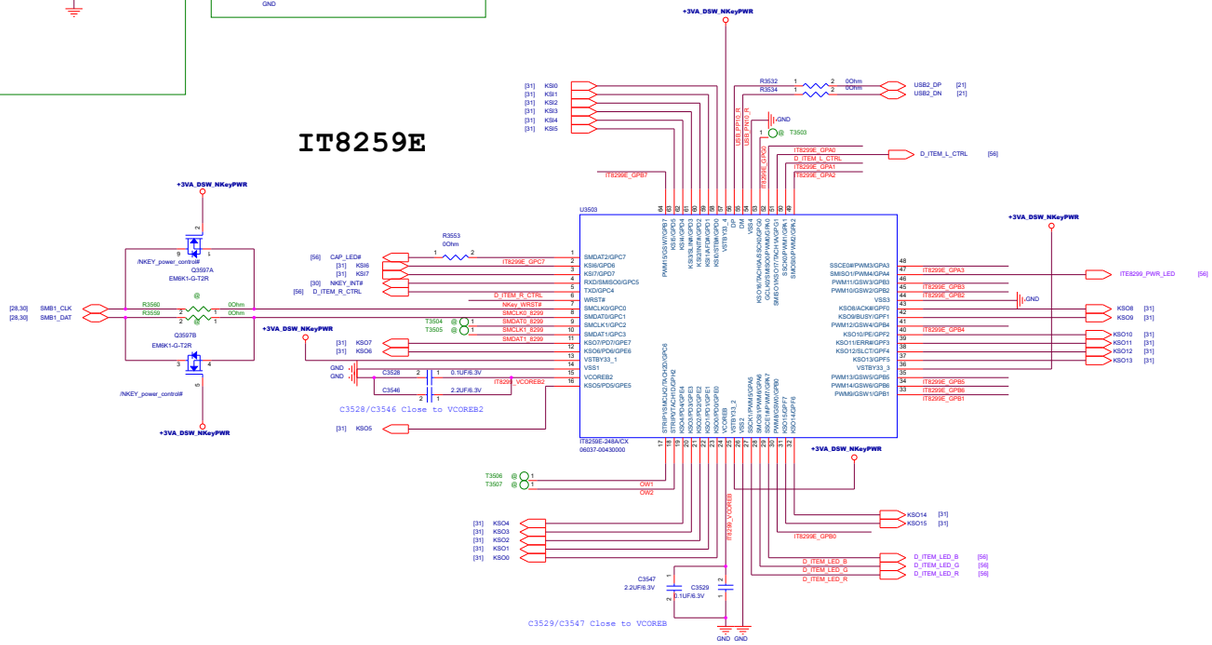
Pull up



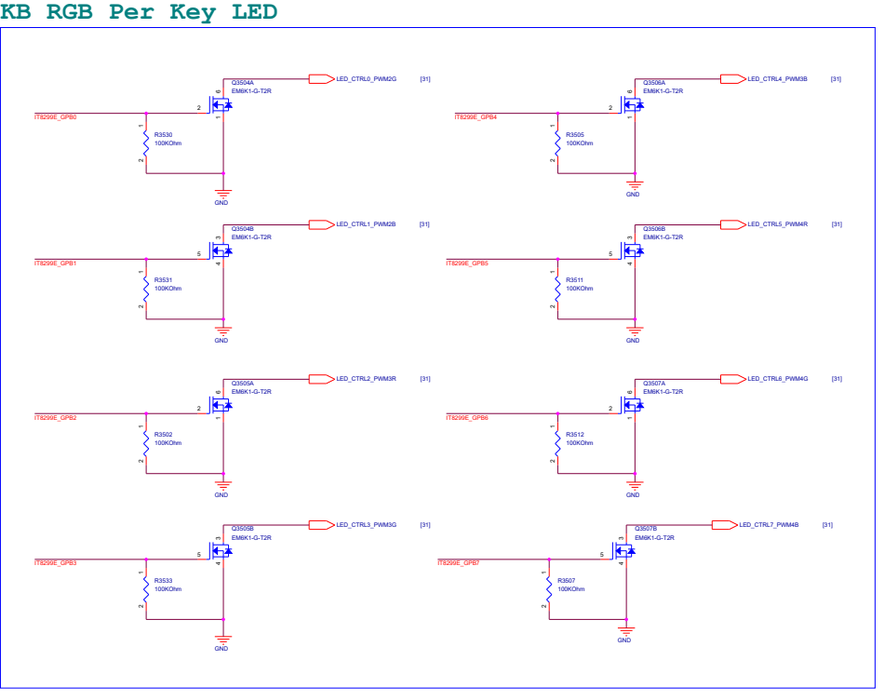
For ESD



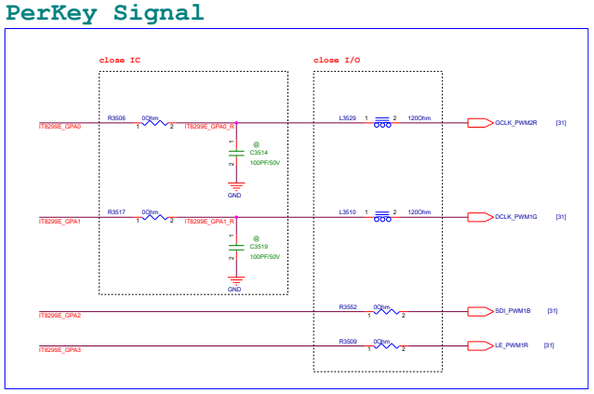
IT8259E



KB RGB Per Key LED



PerKey Signal



<Core Design>

ASUSTeK COMPUTER	Title :	LAN_*****
	Engineer:	EE
Size: Custom	Project Name: GX550LXS	Rev: R1.0
Date: Friday, November 06, 2020	Sheet 35 of 103	

*** POWER

** [R88] +3VS — +3VS
** [R87] +3VSUS — +3VSUS
** [R87] +1.8VS — +1.8VS
** [R84] +1.8VSUS — +1.8VSUS
** [R88] +5VS — +5VS
** [R87] +5VSUS — +5VSUS
** [R87] +12VS — +12VS

*** SINGAL

** PCH Control

[7] A_Z_BITCLK — A_Z_BITCLK
[7] A_Z_SYNC — A_Z_SYNC
[7] A_Z_SDIN0 — A_Z_SDIN0
[7] A_Z_SDOUT — A_Z_SDOUT

** EC Control

[30] AMP_SLEEP# — AMP_SLEEP#
[30] OP_SD# — OP_SD#

** Jack Control

[37] EAPD# — EAPD#
[37] TOU_CON_L — TOU_CON_L

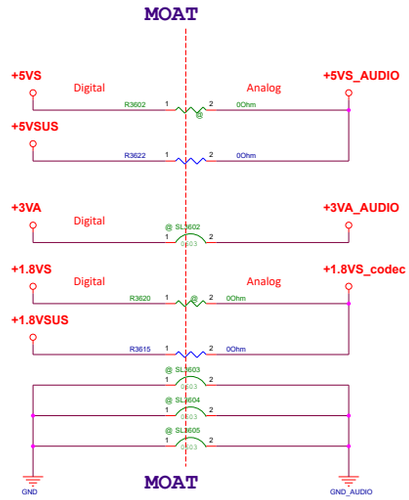
*** To EXT. Amp.

[39] I2S_Codec_SDIN — I2S_Codec_SDIN
[39] I2S_Codec_SDOUT — I2S_Codec_SDOUT
[39] I2S_BCLK — I2S_BCLK
[39] I2S_LRCLK — I2S_LRCLK

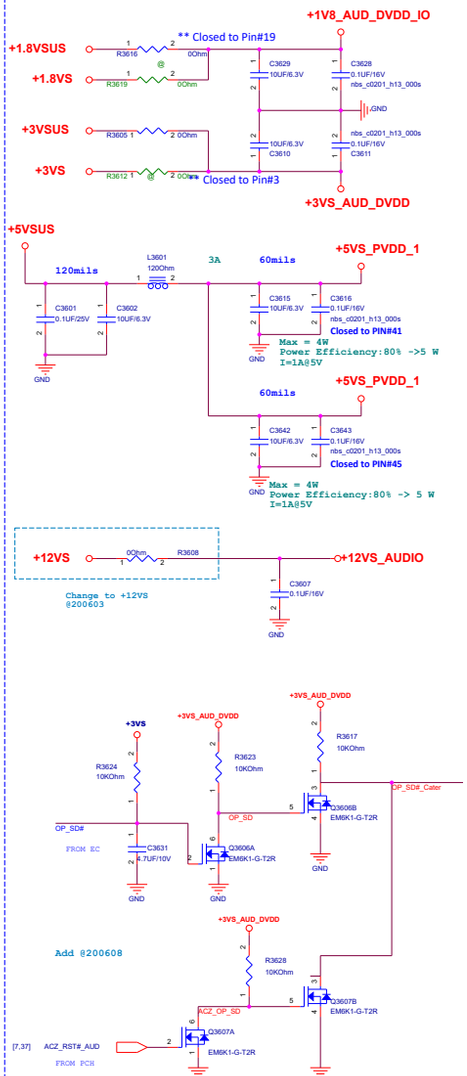
*** Headset Connection

[37] LINE1_R — LINE1_R
[37] LINE1_L — LINE1_L
[37] MIC2_R_SLEEVE — MIC2_R_SLEEVE
[37] MIC2_L_RING2 — MIC2_L_RING2
[37] MIC2_VREFO_R — MIC2_VREFO_R
[37] MIC2_VREFO_L — MIC2_VREFO_L
[37] HPOUT_L — HPOUT_L
[37] HPOUT_R — HPOUT_R

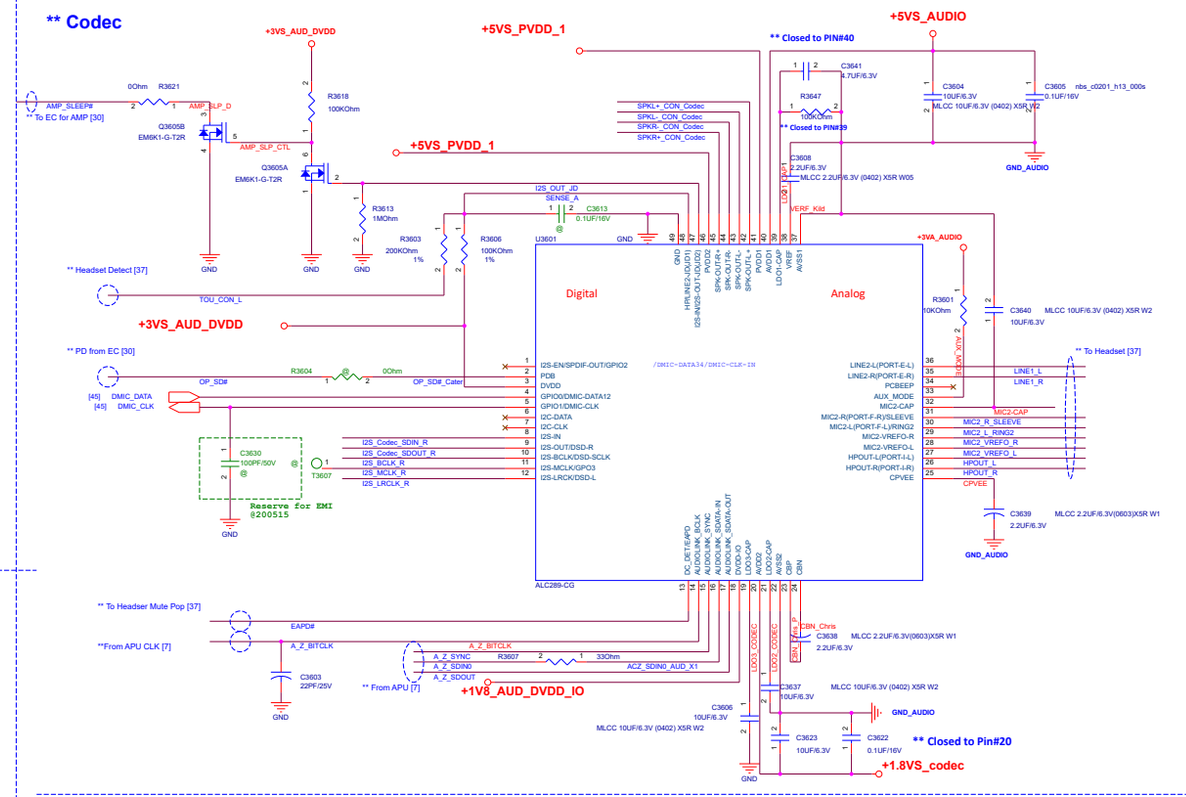
** PWR DISTRIBUTION (ANALOG)



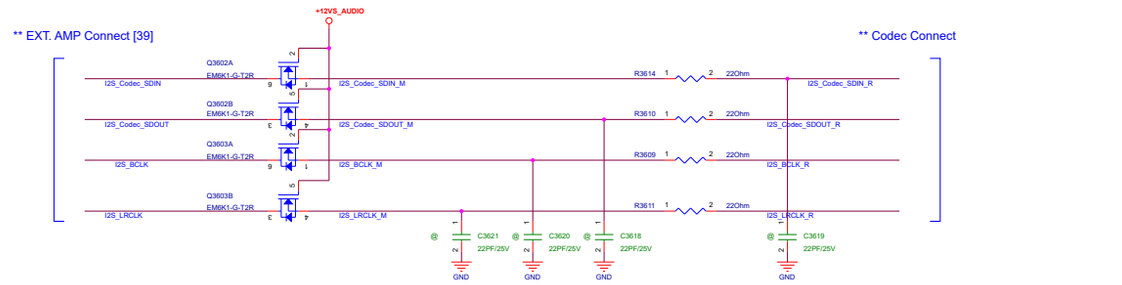
** PWR DISTRIBUTION (DIGITAL)



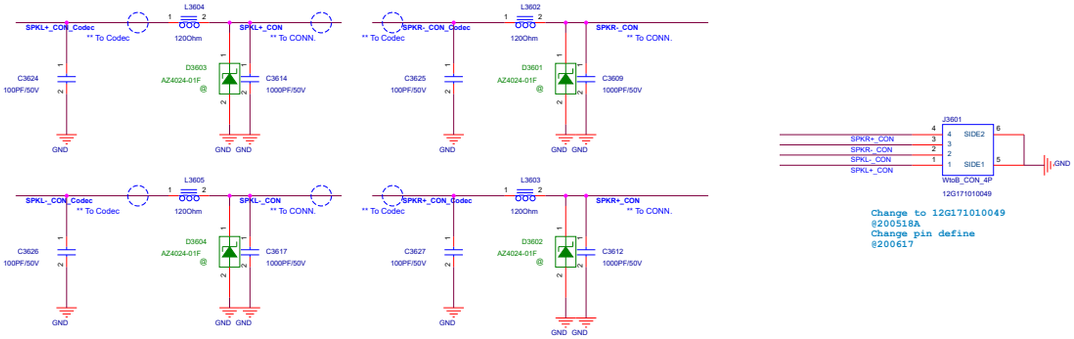
** Codec



** EXT. AMP Connection



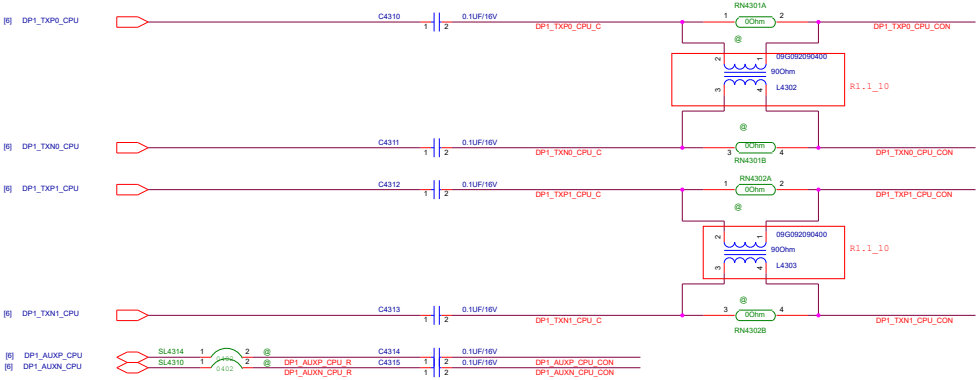
** Tweeter AMP CONN.

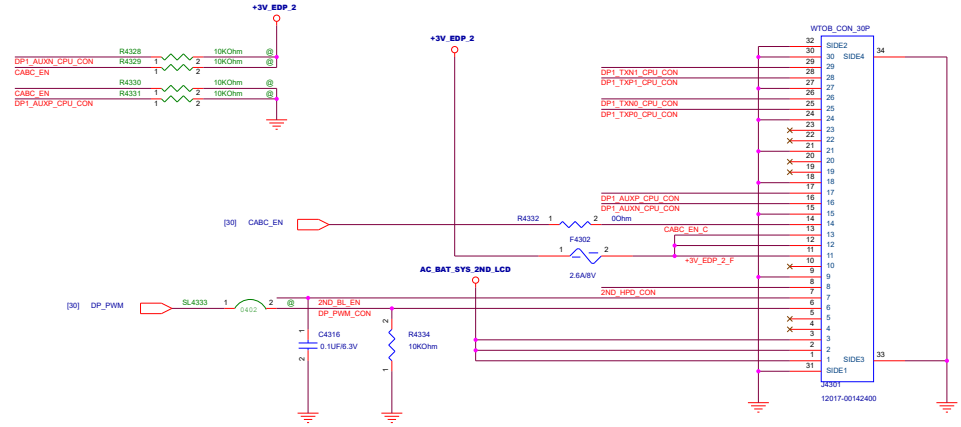


<Core Design>

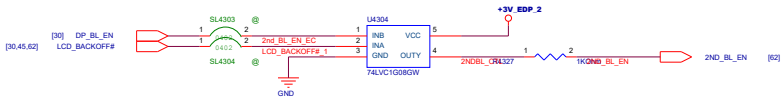
ASUS	Project Name: ALC285+SMARTAMP	Rev: R1.3
Title : AUD-ALC285		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1
Date: Friday, November 06, 2020	Sheet 36 of 104	

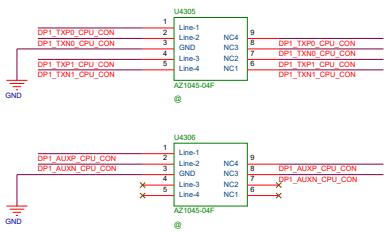
Second Display





For ESD





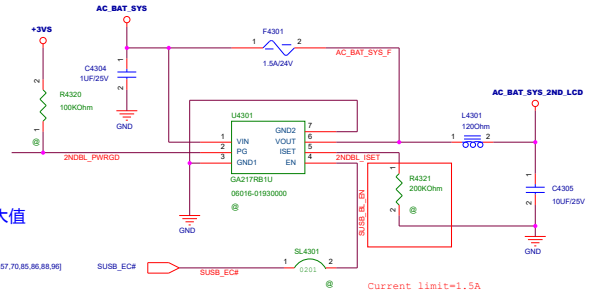
LCD Power switch

DP_3

Power Switch IC Protection Circuit

180423 Holton
Add Power Switch circuit with GA217 06016-01930000

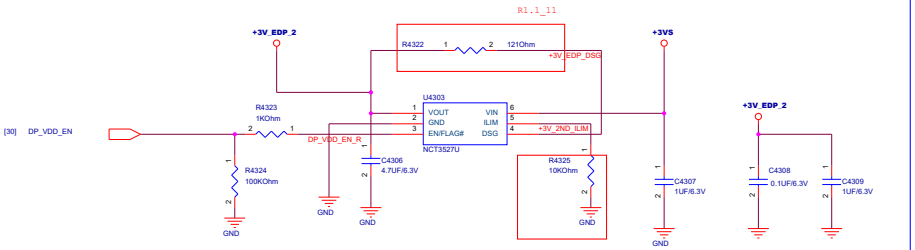
Mark Copy UX461FN 1129



LCDBL_PWRGD:
H: OK
L: NG

※R_iset (R4541)的阻值決定Panel工作電流最大值
R_iset(Kohm)=300/I-limit(A)

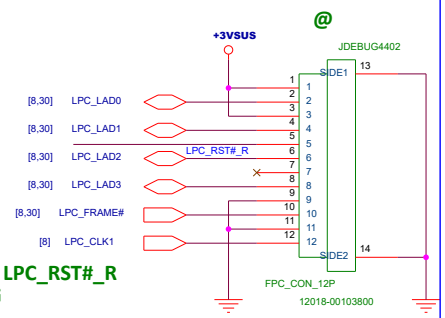
LCD Power switch



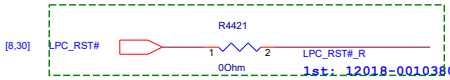
Project Name: GX550LXS			Rev: R1.0
Title: CB_CON			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, November 06, 2020	Sheet 43 of 104		

LPC Debug Port

2017/11/10



Add R4421 & LPC_RST#_R @20190909G

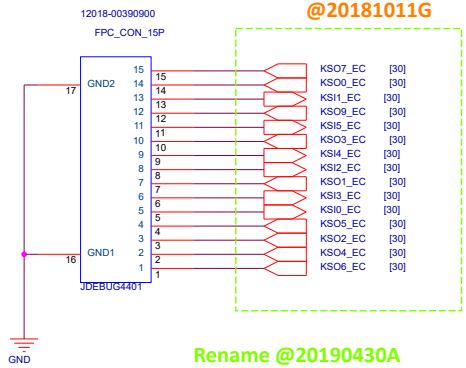


1st: 12018-00103800
2nd :12018-00103300

Flash BIOS

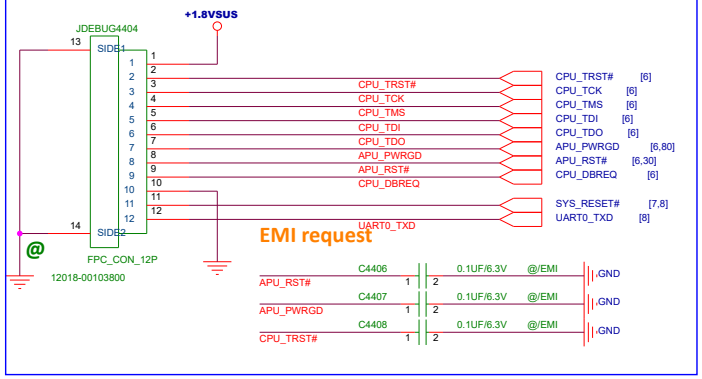
2017/11/10

Rename @20181011G



Rename @20190430A

HDT + UART Debug

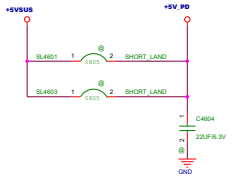


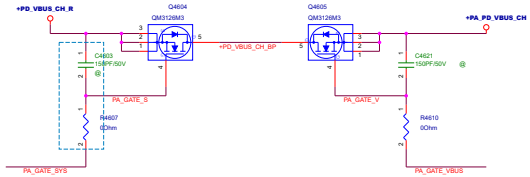
EMI request

<Core Design>

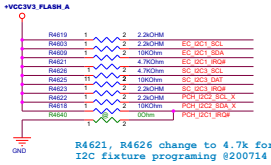
ASUSTeK COMPUTER	Title : DEBUG_LPC	
	Engineer: EE	
Size: B	Project Name: GX502GX	Rev: R1.0
Date: Friday, November 06, 2020	Sheet 44 of 104	

Imax=1port+1CC=3.6A



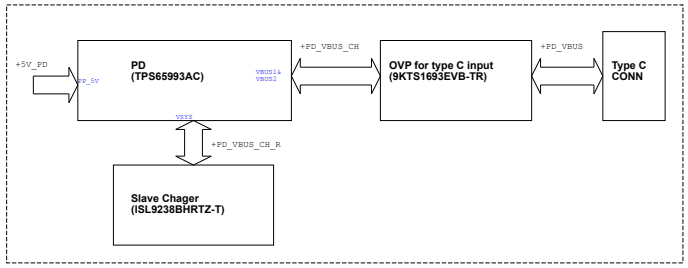


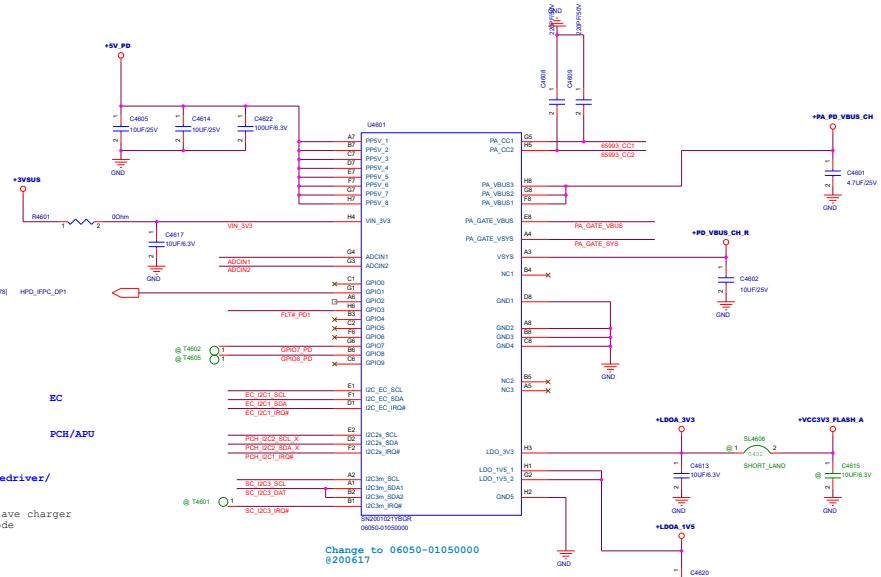
Add R4607, R4610, C4503
@200525



R4621, R4626 change to 4.7k for
I2C fixture programing @200714

Power Flow Chart





EC

PCH/APU

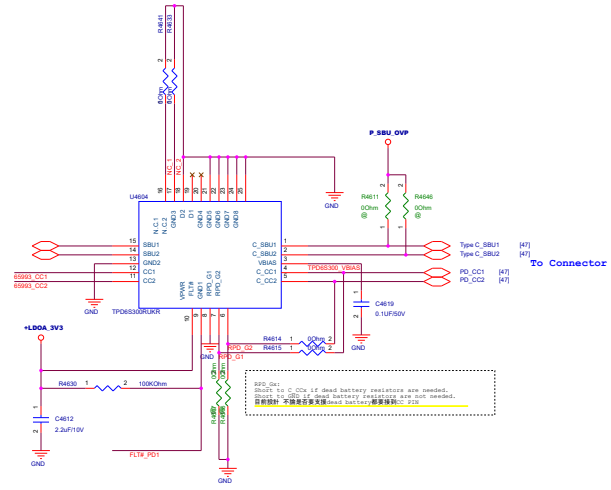
I2C ROM/MUX Redriver/
Slave Charger

Connect to I2C ROM & Slave charger
Reserved for MUX I2C mode

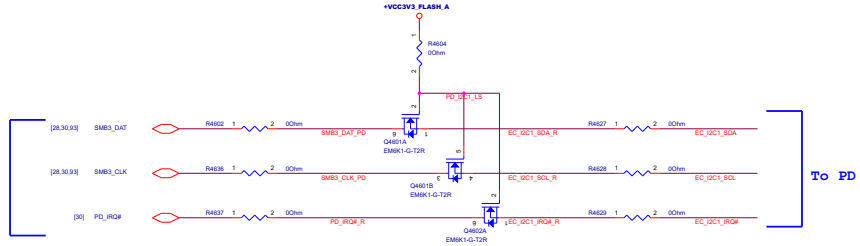
Change to 06050-01050000
@200617

From 1205A

From PD



To PD

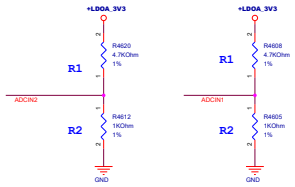


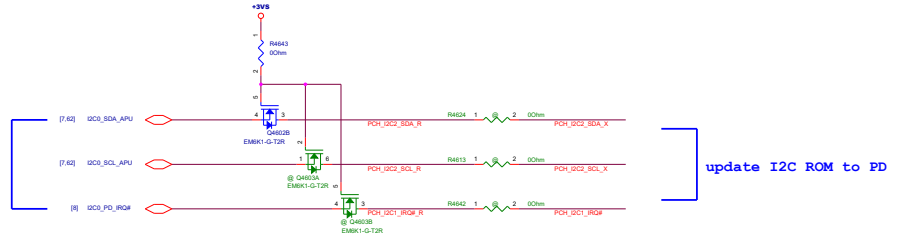
EC & Slave Charger

Supported Slave Charger

	W/O I2C ROM	W/ I2C ROM
R4620	4.7K ohm	umount
R4612	1K ohm	1K ohm
R4608	4.7K ohm	umount
R4605	1K ohm	1K ohm

I2C Default Slave Address -> 0x42

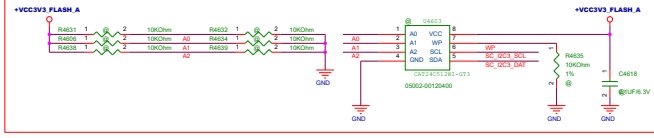




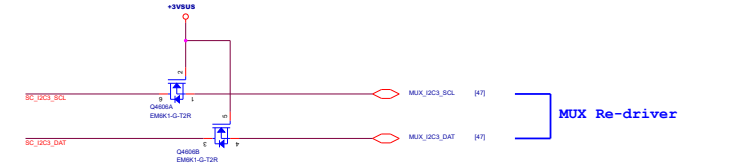
update I2C ROM to PD

Updaye FW from PCH/APU

I2C ROM

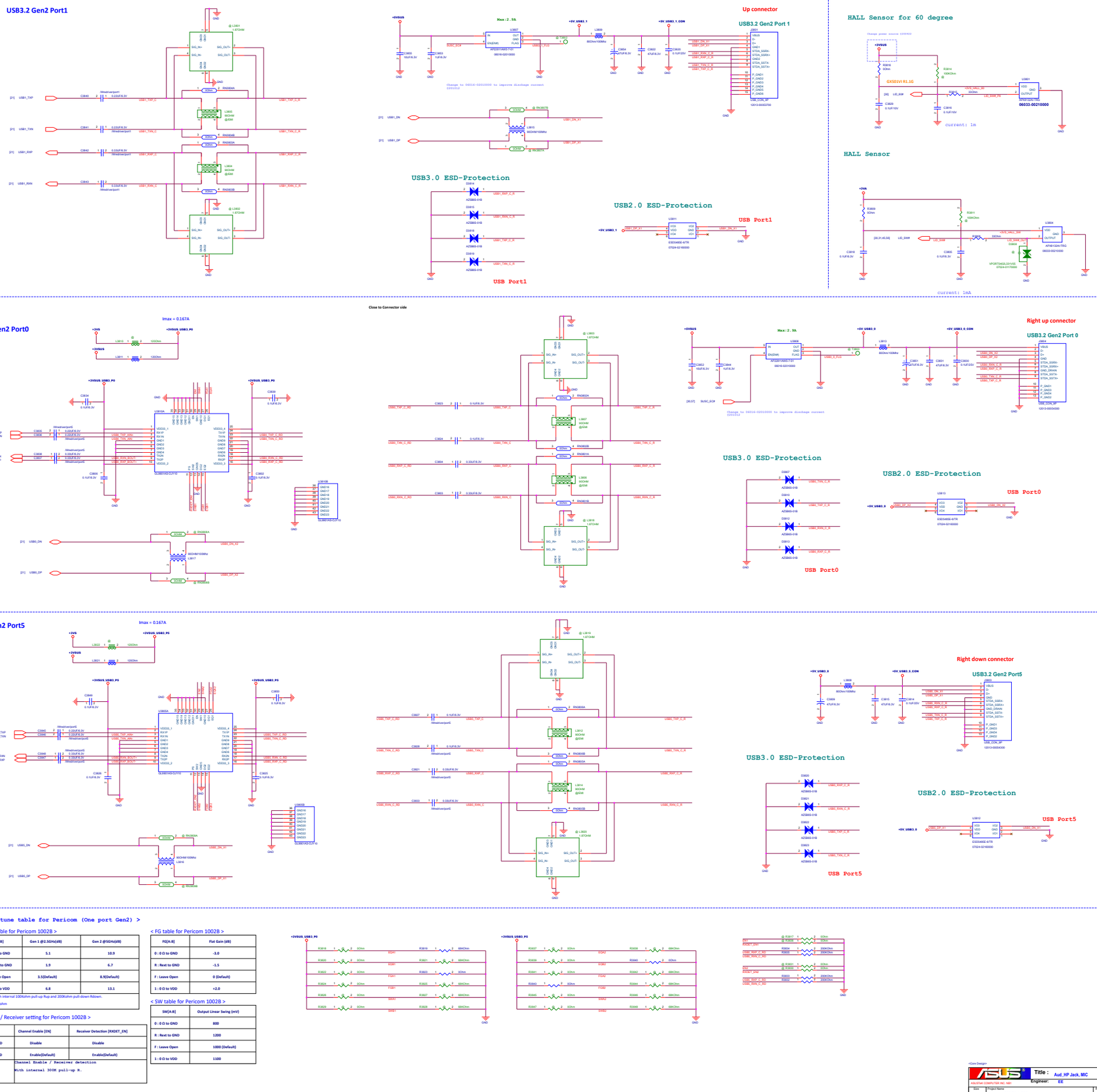


PD I2C ROM



MUX Re-driver

ASUS	Project Name: Type-C_ALT_USB3-10G + DP + PD + Slave_Charger_TI		Rev: R1.0
Title :	PD_TPS65993AC		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Design IP	
Date: Friday, November 06, 2020	Sheet: 46 of 104		



< Fine tune table for Pericom (One port Gen2) >

< EQ table for Pericom 1002B >

EQ[A:B]	Gen 1 @2.5GHz(dB)	Gen 2 @5GHz(dB)
0 : 0 Ω to GND	5.1	10.9
R : Rext to GND	1.9	6.7
F : Leave Open	3.5(Default)	8.9(Default)
1 : 0 Ω to VDD	6.8	13.1

Note : With internal 100kohm pull-up Rup and 200Kohm pull-down Rdown.
Rext = 68Kohm

< FG table for Pericom 1002B >

FG[A:B]	Flat Gain (dB)
0 : 0 Ω to GND	-3.0
R : Rext to GND	-1.5
F : Leave Open	0 (Default)
1 : 0 Ω to VDD	+2.0

< SW table for Pericom 1002B >

SW[A:B]	Output Linear Swing (mV)
0 : 0 Ω to GND	800
R : Rext to GND	1200
F : Leave Open	1000 (Default)
1 : 0 Ω to VDD	1100

< Channel / Receiver setting for Pericom 1002B >

Setting	Channel Enable [EN]	Receiver Detection [RXDET_EN]
0 : 0 Ω to GND	Disable	Disable
1 : 0 Ω to VDD	Enable(Default)	Enable(Default)
Note	Channel Enable / Receiver detection With internal 300K pull-up R.	

SPK Power

AC_BAT_SYS
+PVDD_AMP
R3901 1 2 0Ohm
R3931 1 2 0Ohm
+ CE3901 15UF/25V
GND

IO Power

+1.8VSUS
+3VSUS
0926 Modify
R3907 1 2 @ 0Ohm
R3921 1 2 0Ohm
5mA
+1.8V_3.3V_IOVDD
C3907 1UF/6.3V
GND

INTERNAL SPK1 Conn.

SPK L+ L- R+ R- trace width
Speaker 8 ohm
Max = 1.5W / Channel
I = 0.43 A

(Smart AMP MAX 2A/Channel) ==> 60mils

J3901
WTOB_CON_6P
12017-00011400
ADR_AMP
H_SPKL-_CON
H_SPKL+_CON
H_SPKR-_CON
H_SPKR+_CON
SIDE1
SIDE2
GND

Add to follow design IP @200612A
Change to 11020-00084000 (H=2.1mm) @201006A

+PVDD_AMP
C3903 22UF/25V
C3904 22UF/25V
C3905 0.1UF/50V
GND

+1.8V_3.3V_IOVDD
C3911 4.7UF/10V
C3910 0.1UF/16V
GND

C3947 0.22UF/25V
C3944 0.22UF/25V
H_SPKL- / H_SPKL-
BST_AN_AMP
BST_BN_AMP
H_SPKR- / H_SPKR-

C3938 0.22UF/25V
H_SPKL+ / H_SPKL+
BST_AP_AMP
C3946 0.22UF/25V
H_SPKR+ / H_SPKR+
BST_BP_AMP

C3939 1UF/16V
R3913 1KOhm
VR_DIG_AMP
ADR_AMP

U3905A
BST_A+
OUT_A+
PVDD1
PVDD2
DGND
DVDD
VR_DIG
ADR
GND1
PGND4
PGND3
OUT_A-
BST_A-
BST_B-
OUT_B-
PGND2
PGND1
BST_B+
OUT_B+
PVDD4
PVDD3
AGND
AVDD
GVDD
PDN#
GPIO0
GPIO1
GPIO2
LRCLK
SCLK
SDIN
SDA
SCL
TAS5825MRHBR

C3942 1UF/16V
C3943 1UF/16V
AVDD_AMP
GVDD_AMP

+PVDD_AMP
C3945 0.1UF/50V
C3914 22UF/25V
C3912 22UF/25V
GND

+1.8V_3.3V_IOVDD
R3930 10KOhm
R3902 0Ohm
REST_AMP# [30]
AMP_PDN#
C3948 0.1UF/16V
GND

U3905B
TAS5825MRHBR
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14

0926 Change for additional 13 VIA

Add REST_AMP#@20190430A

+1.8V_3.3V_IOVDD
R3924 @ 10KOhm AMP_GPIO0
R3925 @ 10KOhm AMP_GPIO2

[36] I2S_Codec_SDIN
[36] I2S_LRCLK
[36] I2S_BCLK
[36] I2S_Codec_SDOUT
I2S_Codec_SDIN
I2S_LRCLK
I2S_BCLK
I2S_Codec_SDOUT
SMB3_CLK_AMP [28]
SMB3_DAT_AMP [28]

I2C Address Table

	ADR_AMP(SPK)	Address 8bit
Main(N.C.)	Open	0x9A
Second	Short	0x98

SPK Output

L3901 30Ohm/100Mhz
H_SPKL- / H_SPKL-_CON
D3903 AZ4024-01F
C3915 1000PF/50V

L3902 30Ohm/100Mhz
H_SPKR- / H_SPKR-_CON
D3904 AZ4024-01F
C3919 1000PF/50V

L3903 30Ohm/100Mhz
H_SPKL+ / H_SPKL+_CON
D3905 AZ4024-01F
C3917 1000PF/50V

L3904 30Ohm/100Mhz
H_SPKR+ / H_SPKR+_CON
D3906 AZ4024-01F
C3921 1000PF/50V

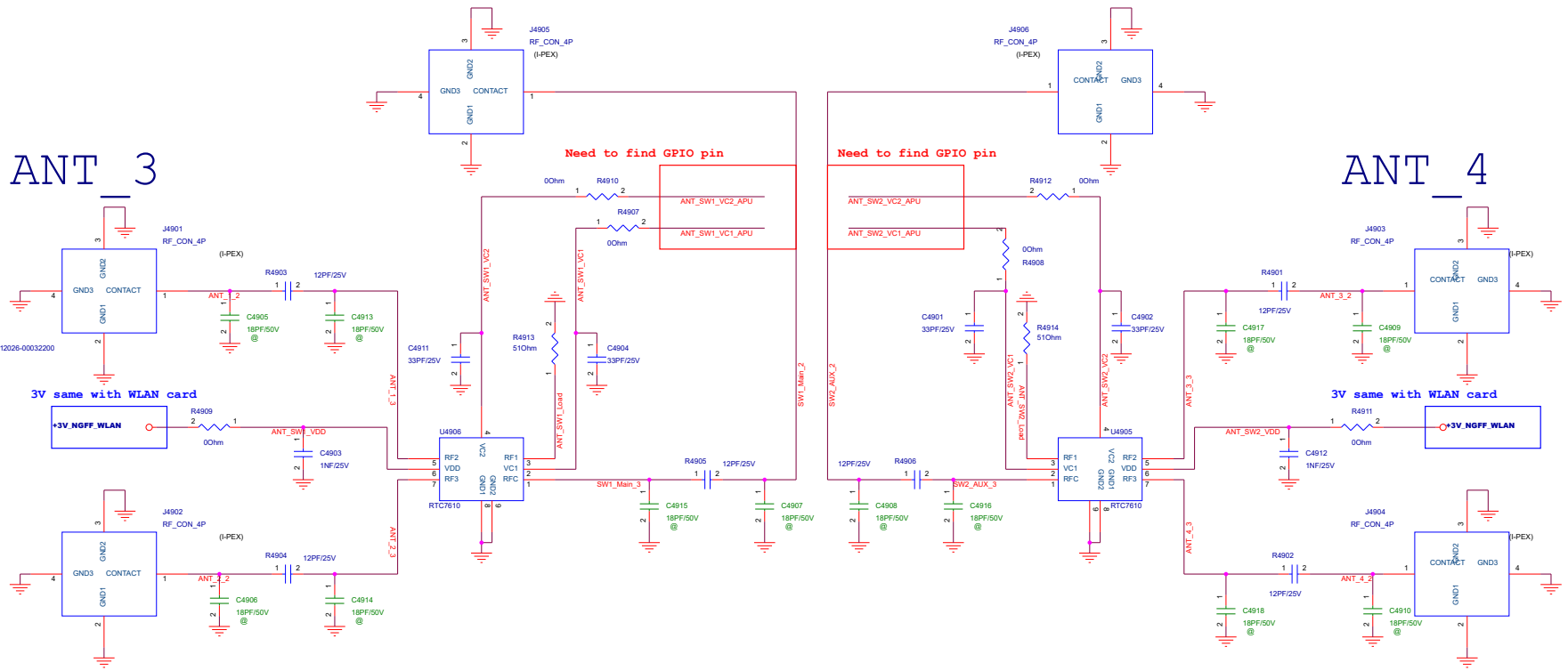
GND

ASUS	Project Name: GX531GX	Rev: R1.0
Title : AUD_INT SPK		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Friday, November 06, 2020	Sheet 39 of 104	

[8] ANT_SW1_VC2_APU
[8] ANT_SW1_VC1_APU
[8] ANT_SW2_VC2_APU
[8] ANT_SW2_VC1_APU

Module_AUX

Module_MAIN



U4906 RTC7610			
ANT	Port	VC1 GPP_B2	VC2 GPP_A19
50 Ω	RF1	1	0
ANT_3	RF2	X	1
ANT_4	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

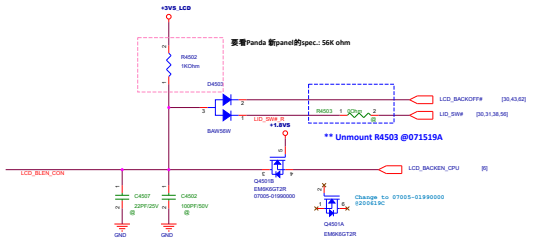
U4905 RTC7610			
ANT	Port	VC1 GPP_B0	VC2 GPP_A18
50 Ω	RF1	1	0
ANT_1	RF2	X	1
ANT_2	RF3	0	0

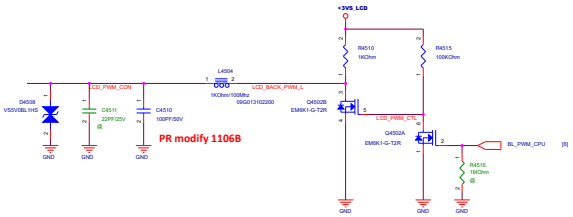
X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

<Core Design>

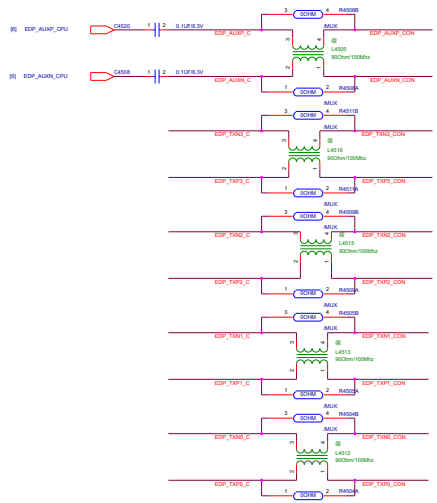
ASUS	Project Name: GX701	Rev: 1.0
Title : ANT		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, November 06, 2020	Sheet 49 of 103	

Controll Signal (LCD/BL)



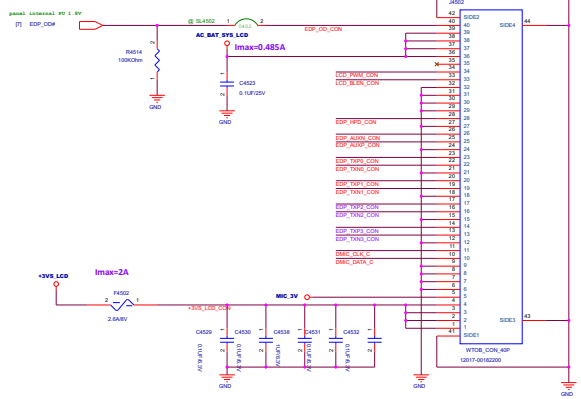


eDP from CPU



For EMI

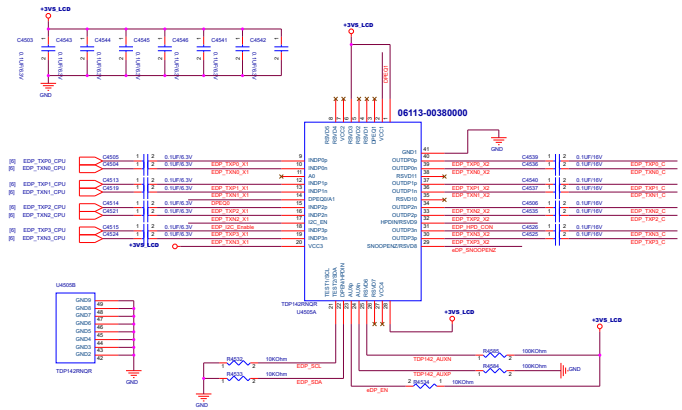
Normal : L (OD Enable)
Active : H (OD disable)



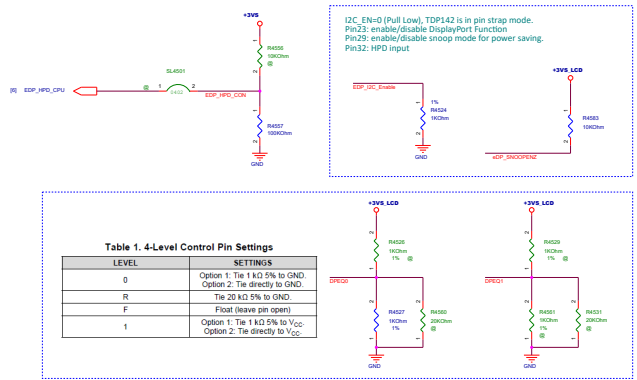
eDP Panel Conn.

1st : 12017-00182200

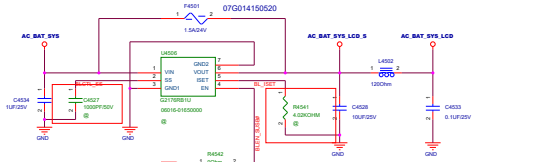
** EDP1.4 Re-driver



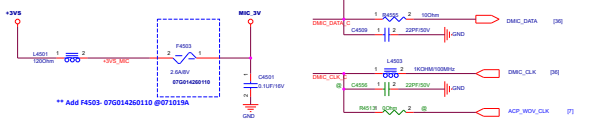
** eDP_HPD (CPU)



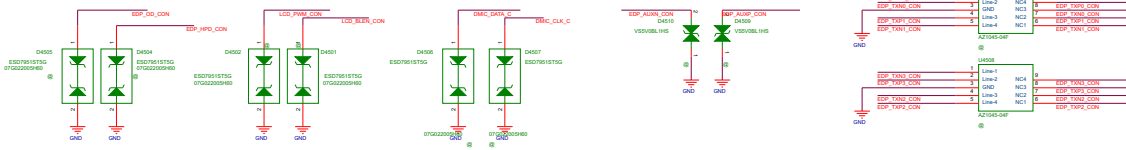
** Panel BL Power



** MIC PWR

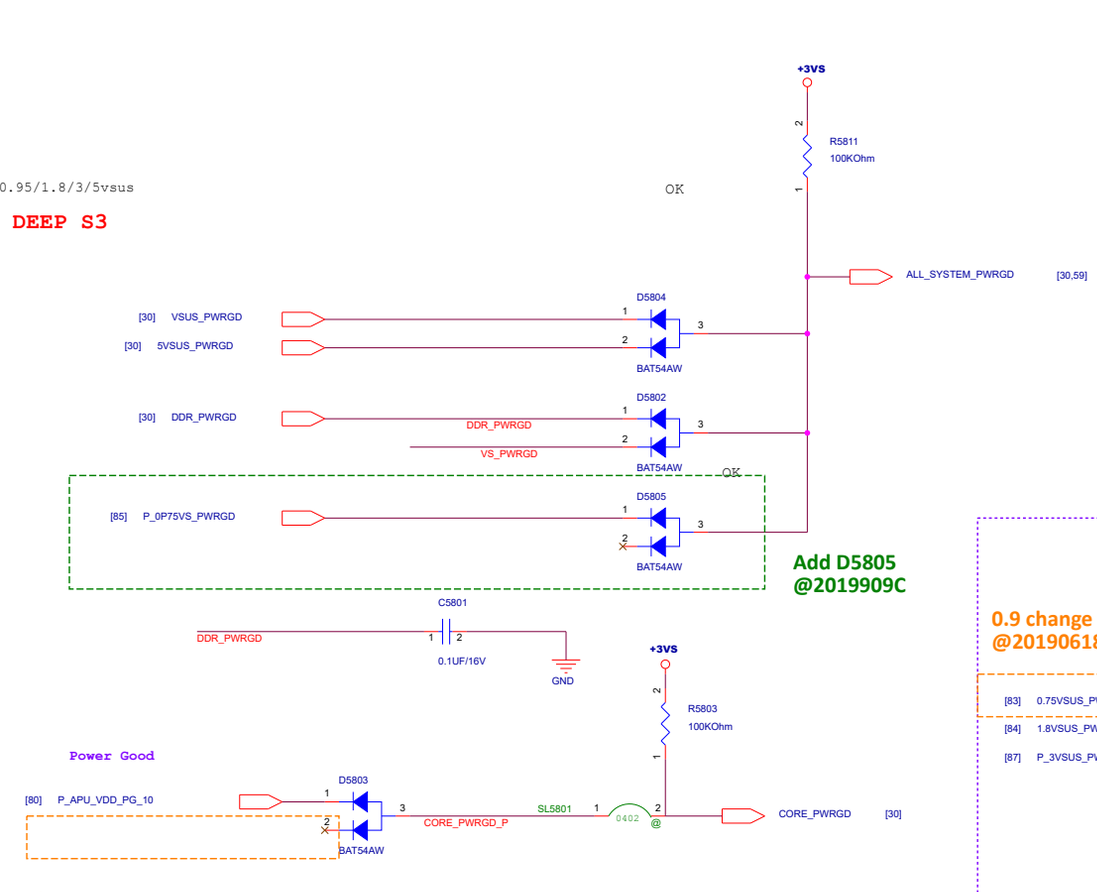


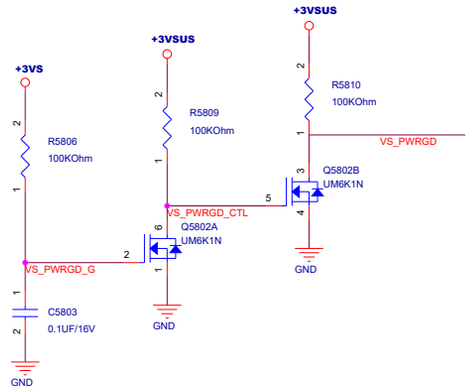
** For ESD

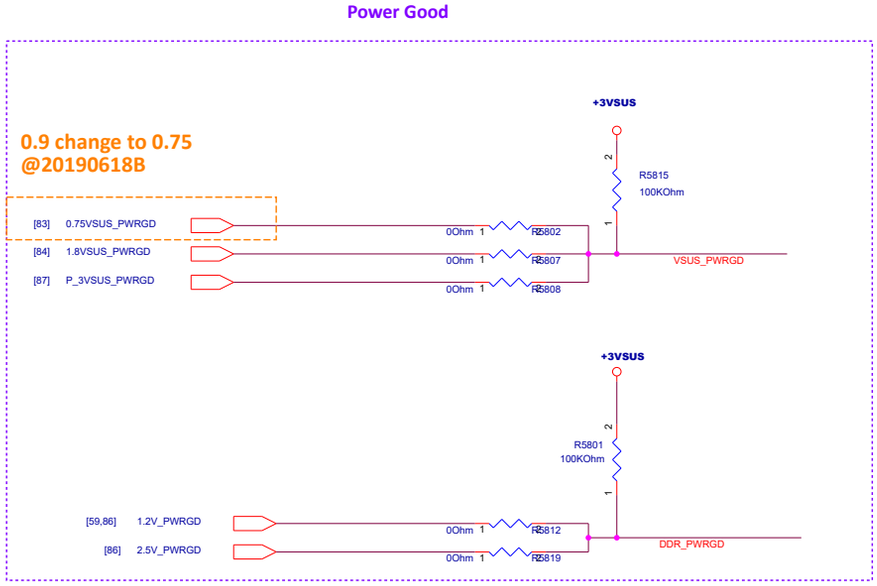


Title :	CRT_eDP
Engineer:	EE
Size: Custom	Project Name: GA401
Rev: 1.0	
Date: Friday, November 06, 2020	Sheet 45 of 104

POWER GOOD DETECTER







Remove AMD GPU PWRGD
@20181009K

ASUS	Project Name: FX505DY	Rev: R1.0
Title : POWER GOOD DETECTER		
Size: Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: RD2 EE3	
Date: Friday, November 06, 2020	Sheet 58 of 104	

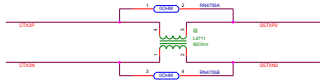
Title : USB Charger

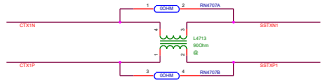
Engineer: EE

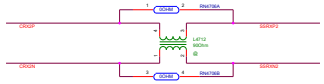
Size	Project Name	Rev
A1	GX502GX	R1.0

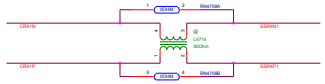
Friday, November 08, 2019 | Sheet 53 of 59

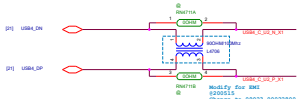
USB EMI-Protection

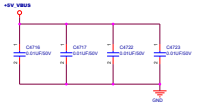


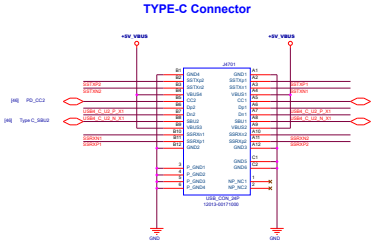


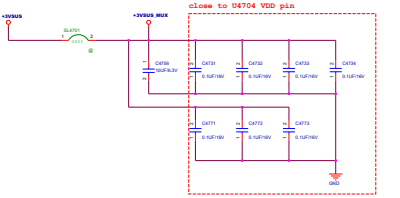


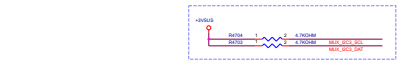


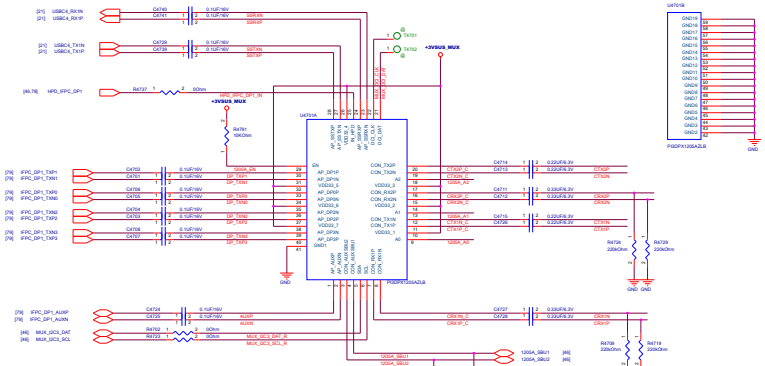


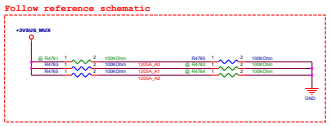












Address 0x56 with SPI ROM

3.9.1 I2C Address

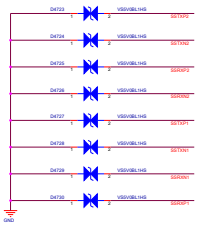
	Register Bits							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Slave address (First byte is slave address)	1	0	1	0	A2	A1	A0	0/1 (W/R)

NOTE 8. PIN ASSIGNMENT (FRONT VIEW)

Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
	GND	TX1+	TX1-	V_{BUS}	CC1	D+	D-	SBU1	V_{BUS}	RX2-	RX2+	GND
	GND	RX1+	RX1-	V_{BUS}	SBU2	D-	D+	CC2	V_{BUS}	TX2-	TX2+	GND
Pin No.	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

NOTE 9. LASER WELD POINTS MAY BE DISCOLORED.

USB3.0 ESD-Protection

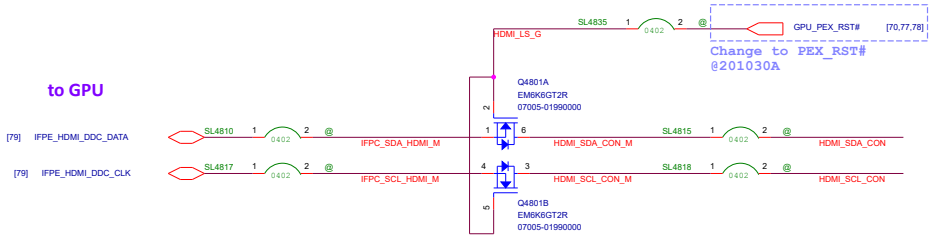


USB2.0 ESD-Protection

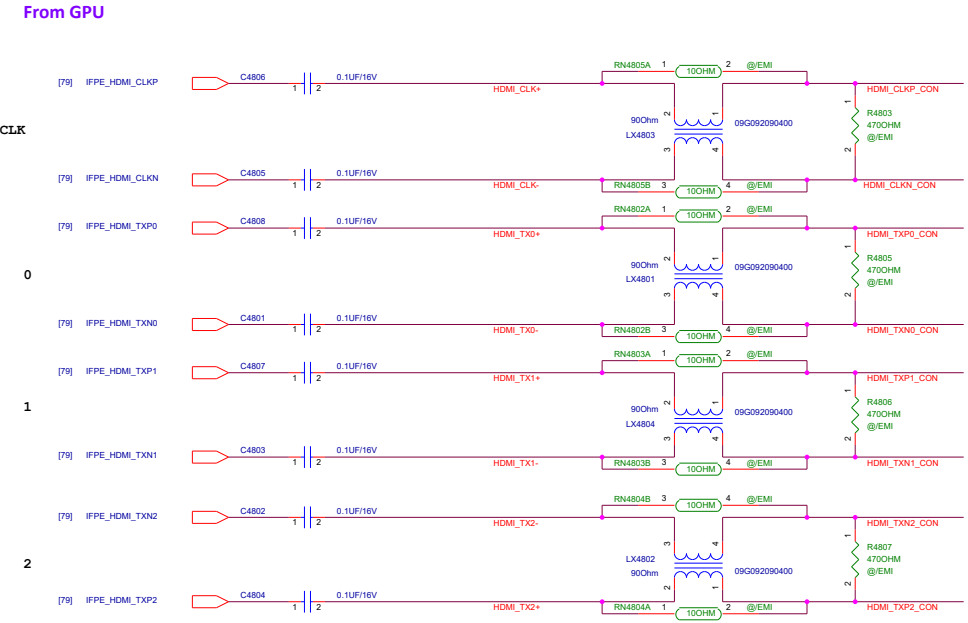
Title :	USB3.1 TYPE-C+TI 1046A		
Size: D	Dept.: ASUSTeK COMPUTER INC.	Engineer:	Design IP
Date: Friday, November 06, 2020	Sheet 47 of 104		

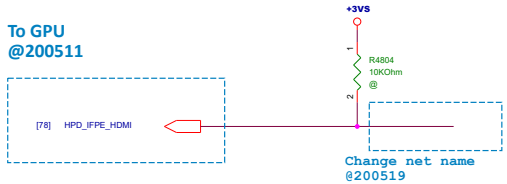
Main Board

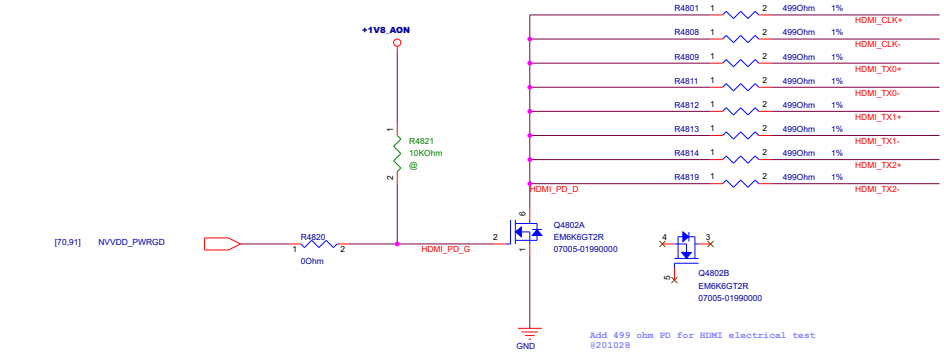
HDMI Active-Level Shift



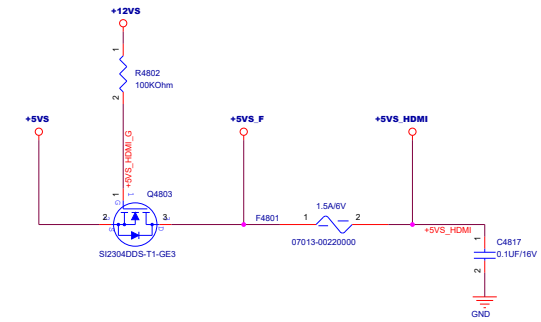
HDMI EMI



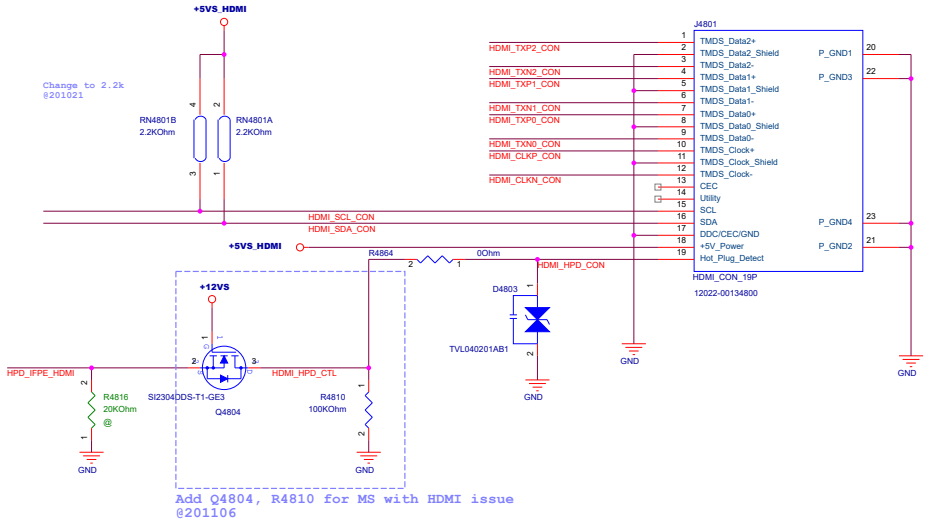




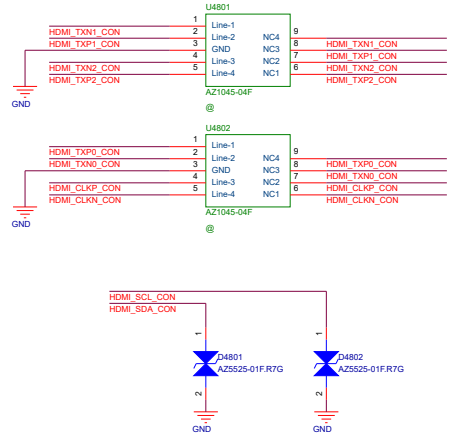
HDMI PWR_+5VS_HDMI



HDMI Conn.



ESD Protect



ASUS	Project Name: Design IP		Rev: R1.0
Title :	HDMI ReTimer_Revision History_R0.1A		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, November 06, 2020	Sheet 48 of 104		

Title <Title>		
Size A	Document Number <Doc>	Rev R1.0
Date: Friday, November 06, 2020	Sheet 54 of 104	

<Core Design>

Title :

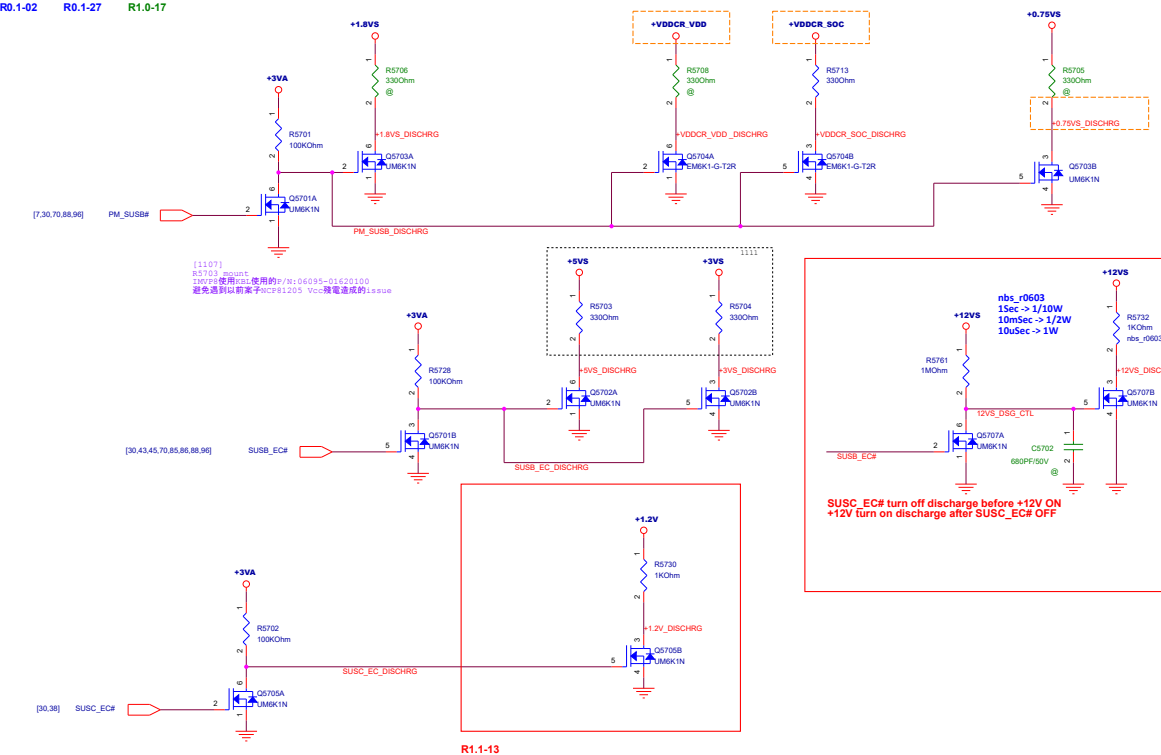
ASUSTeK COMPUTER

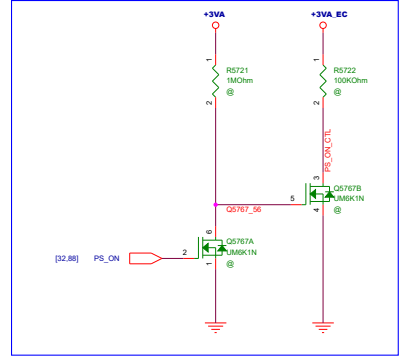
Engineer: EE

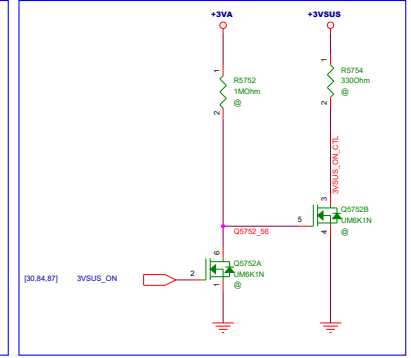
Size	Project Name	Rev
A	**GX502GX**	R1.0

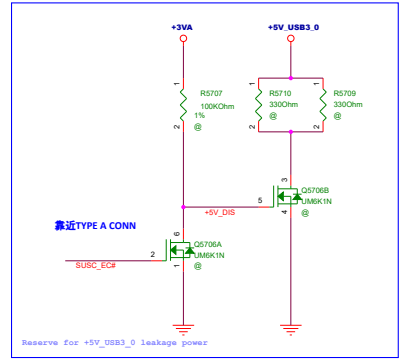
Date:	Friday, November 06, 2020	Sheet	55	of	104

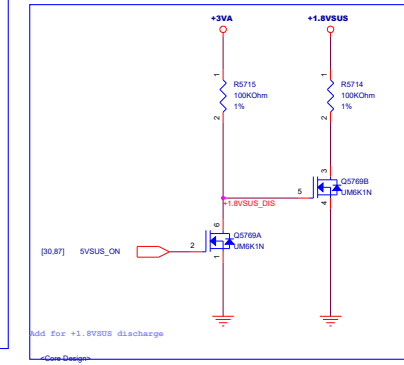
R0.1-02 R0.1-27 R1.0-17











ASUSTeK COMPUTER	Title : DSG_Discharge	
	Engineer: EE	
Size: Custom	Project Name: GX502GX	Rev: R1.0
Date: Friday, November 06, 2020	Sheet 57 of 104	

Thermal Sensor : SN170027

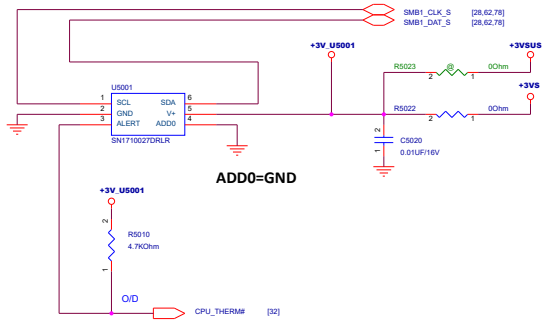
ALERT/SDA/SCL: Open-drain output; pullup resistor 5Kohm

Pin function Supply voltage.: 1.62 V to 3.6 V

power rail : 3.3V

SMBUS1 to EC

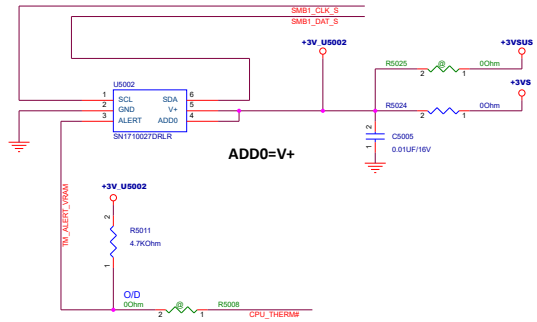
CPU



Near CPU

SMBUS addr=10010000 (90)

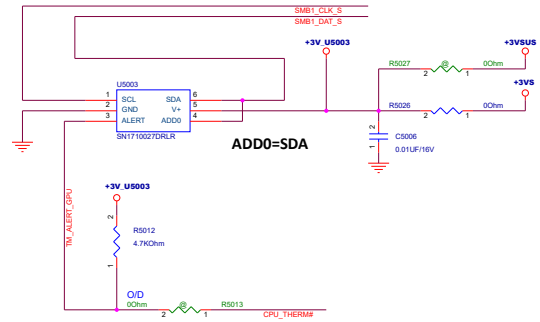
VRAM



Near VRAM

SMBUS addr=10010010 (92)

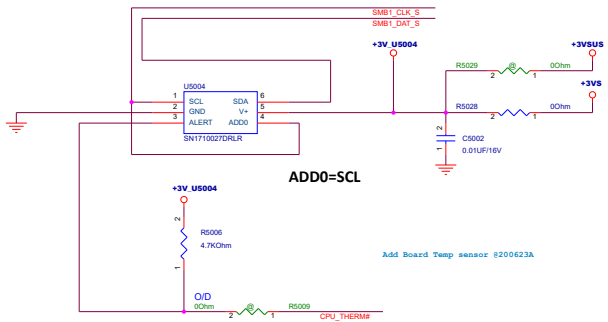
GPU



Near GPU

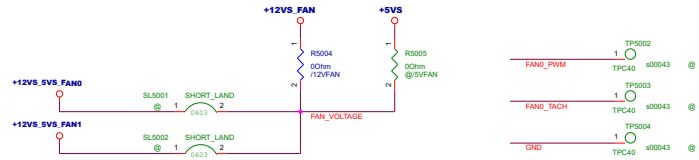
SMBUS addr=10010100 (94)

Board Temperature



Away from CPU

SMBUS addr=10010110 (96)

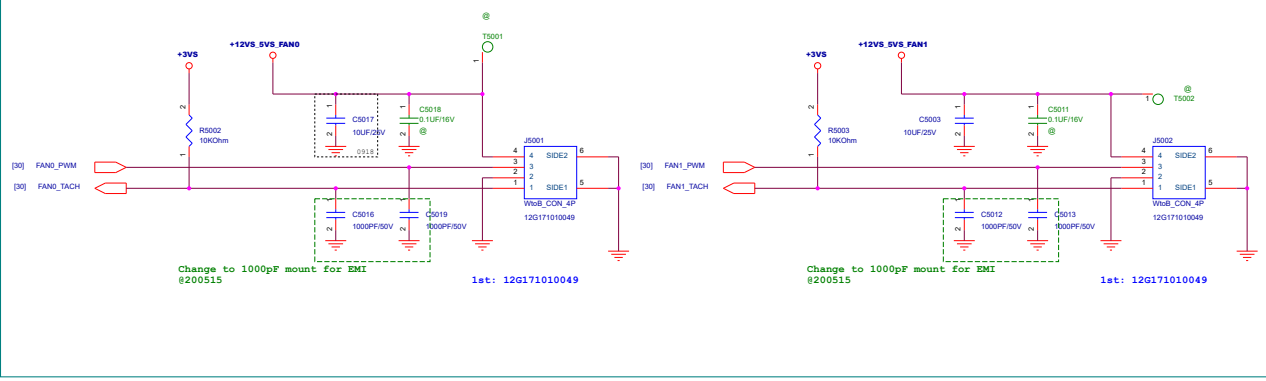


ADD0: Address select. Conne

Table 3. Address Pin and Slave Addresses

DEVICE TWO-WIRE ADDRESS	ADD0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL

CPU&GPU FAN



<Core Design>

ASUSTeK COMPUTER

Title : FAN_Thermal Sensor & Fan

Engineer: EE

Size	Project Name	Rev
C	GX502GX	R1.0

Date: Friday, November 06, 2020 Sheet 50 of 104

Title : USB Charger

Engineer: EE

Size	Project Name	Rev
A1	GX502GX	R1.0

<Core Design>

Title : IO Con. to MB

ASUSTeK COMPUTER

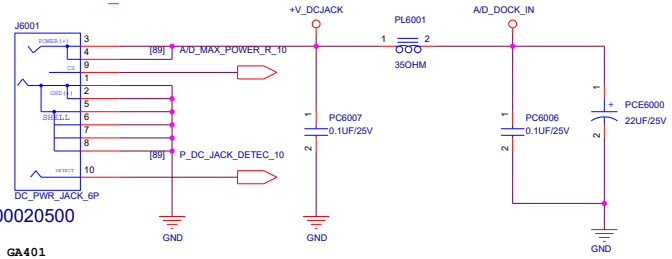
Engineer: EE

Size	Project Name	Rev
A	GX502GX	R1.0

DC-IN Connector

DC Jack使用請詢用River_Hsu

New 6 Phi 4 Pin DC_Jack

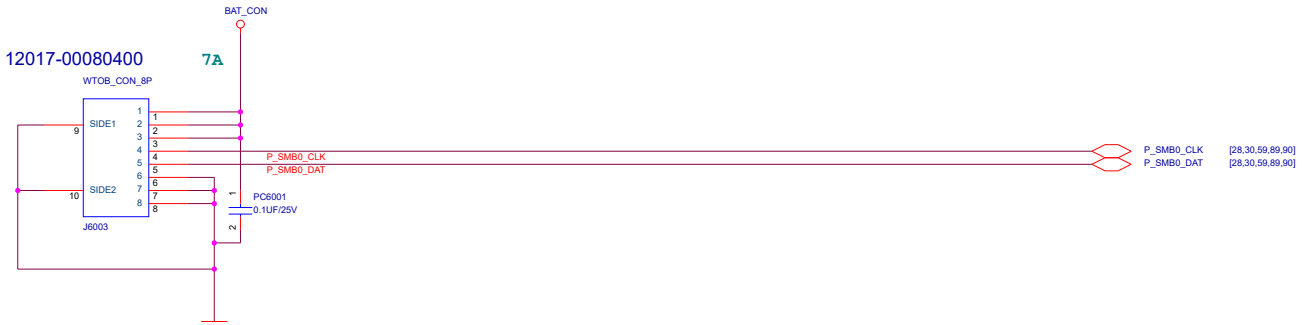


12033-00020500

leverage GA401

J6001	3.4CH	1.55CH
	12033-00020200	12033-00020300

Battery Connector



Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

ASUS	Project Name: GX700		Rev: R1.0
Title : DC & BAT IN			
Size: A3	Dept.: NB_Power team	Engineer: Benson	
Date: Friday, November 06, 2020	Sheet 60 of 104		

AMD-1.0

NGFF M.2 TYPE_E-KEY WIFI

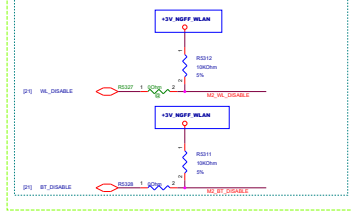
Main Board

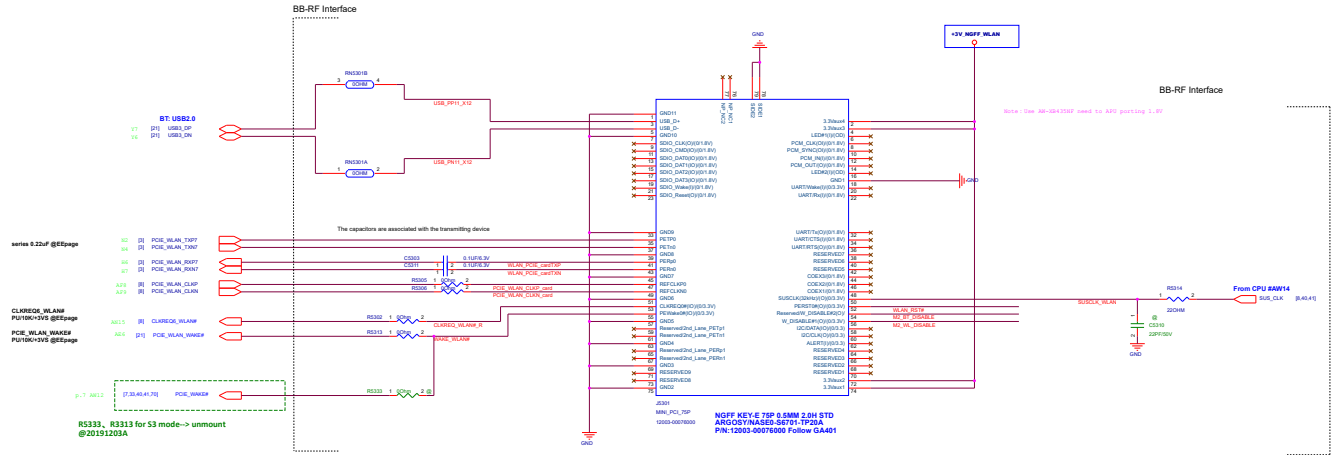
WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

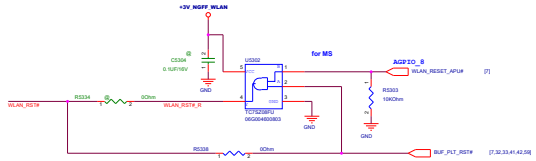
Support ASUS Open Cloud Computing (AOConnect)
WLAN PWR to +3VSUS

WLAN & BT Ext_HW_Kill

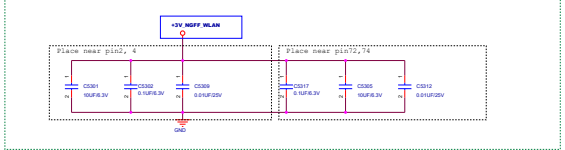
WLAN card Vendor recommend: (Intel/Realtek)
1. Module internal PU
2. Placeholder for protect unexpected issue





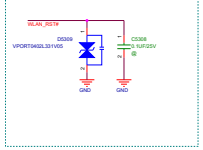


WLAN NGFF_WLAN bypass capactor



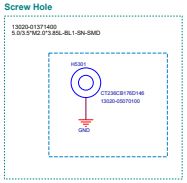
For EMI

Reserve for powr noise



Screw Hole

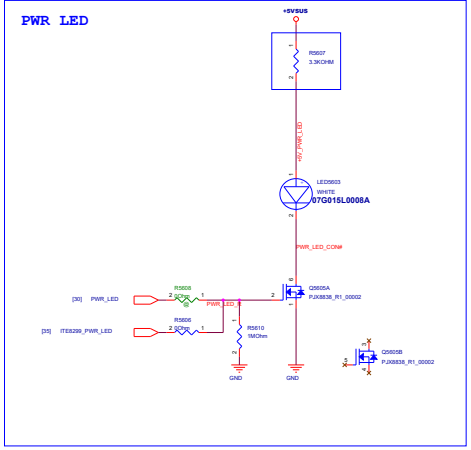
13020-01371400
S.D/3.5*M2.0*3.65L-BL1-SN-SMD



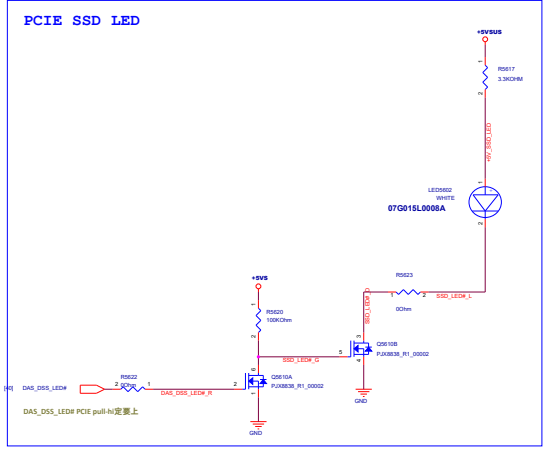
Change to 13020-05070100 @200703B

ASUSTeK COMPUTER	Title : BT_Bluetooth	
	Engineer: EE	
Size: C	Project Name: GX502GX	Rev: R1.0
Date: Friday, November 06, 2020	Sheet 61 of 104	

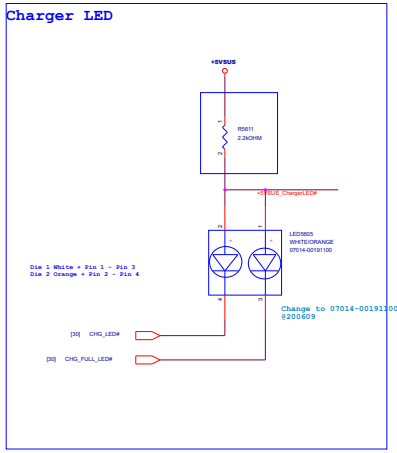
PWR LED



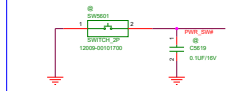
PCIE SSD LED



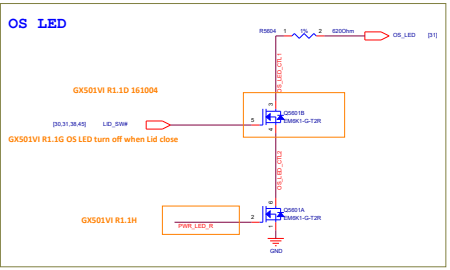
Charger LED

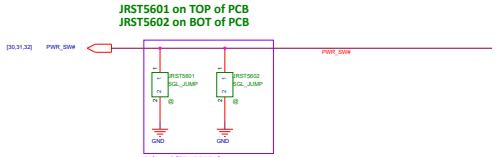


POWER button (For NPI, MP remove)20190521



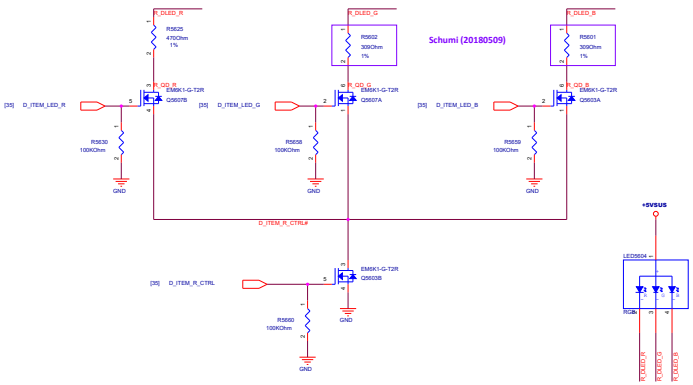
OS LED



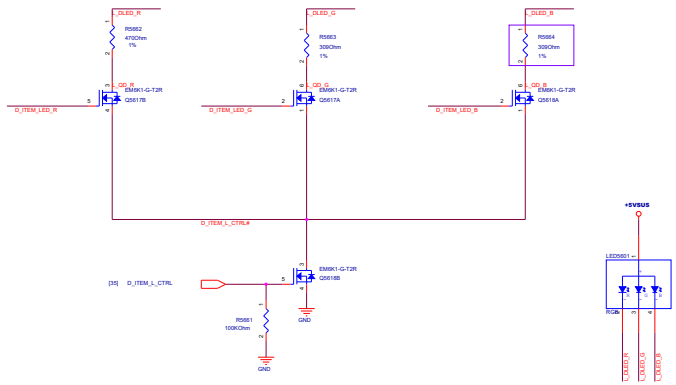


D item- RGB LED

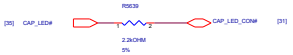
< D case LED R >



< D case LED L >



CAP LED



<Core Design>

ASUSTeK COMPUTER INC. NB3	Title : LED & LID	
	Engineer: EE	
Size: Custom	Project Name: GX550LXS	Rev: R1.0
Date: Friday, November 06, 2020	Sheet 58 of 103	

<Core Design>

Title : I/O_Main board Conn.

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	GX502GX	R1.0

Date:	Friday, November 06, 2020	Sheet	69	of	104

EMI1 SPRING 13NK00B1M01011 *5

Change to 13060-00660000 @200805

U5901 SMD148X73 13NK00B1M01011 /EMI
U5902 SMF169X130 13060-00660000 /EMI
U5903 SMF169X130 13060-00660000 /EMI
U5904 SMF169X130 13060-00660000 /EMI

Change to 13020-00280900 @201012

U5905 EMI_SPRING_2P /EMI 13020-00280900
U5907 EMI_SPRING_2P /EMI 13020-00280900

Add @200609

U5908 SMD93X93_S16 13020-05780000

Change to +5VSUS @201005

+5VSUS: C5907 0.1UF/25V, C5921 0.1UF/25V

+3VA: D5901 AZ5325-01F @, D5902 AZ5325-01F, D5903 AZ5325-01F

P_SMB0_CLK [28,30,60,89,90]
P_SMB0_DAT [28,30,60,89,90]

AC_BAT_SYS: C5932 0.1UF/25V, C5933 0.1UF/25V, C5934 0.1UF/25V, C5929 0.1UF/25V, C5930 0.1UF/25V @, C5904 0.1UF/25V, C5908 0.1UF/25V, C5909 0.1UF/25V, C5906 0.1UF/25V

EMI request @200630B

BAT_CON: C5922 0.1UF/25V, C5928 0.1UF/25V

BAT: C5931 0.1UF/25V

EMI request @200630B

G_PWR_SRC_NVVDD: C5901 0.1UF/25V, C5903 2.2UF/25V

G_PWR_SRC_FBVDDQ: C5902 2.2UF/25V

+NVVDD: C5910 10PF/50V @, C5911 10PF/50V @, C5912 10PF/50V @

AC_BAT_SYS: C5913 0.1UF/25V, C5914 0.1UF/25V, C5915 0.1UF/25V @, C5916 0.1UF/25V, C5917 0.1UF/25V, C5918 0.1UF/25V, C5920 0.1UF/25V, C5924 0.1UF/25V @

[58,86] 1.2V_PWRGD: C5919 100PF/50V

[30,58] ALL_SYSTEM_PWRGD: C5926 100PF/50V @

[7,32,33,41,42,53] BUF_PLT_RST#: C5927 100PF/50V

+1.8VSUS: C5905 0.1UF/25V

EMI request @200701

+3VS: C5923 0.1UF/25V, C5925 0.1UF/25V

EMI request @200630B

+5VS_PWR: C5935 10PF/50V @

<Core Design> 2017.05.02 EMI Reserve

ASUSTeK COMPUTER

Title : OTH_EMI
Engineer: EE

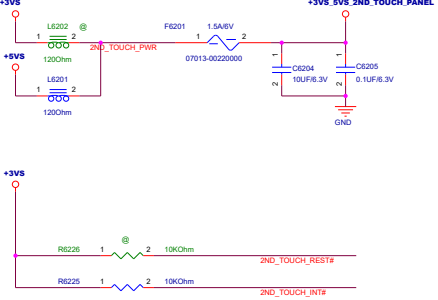
Size	Project Name	Rev
B	GX502GX	R1.0

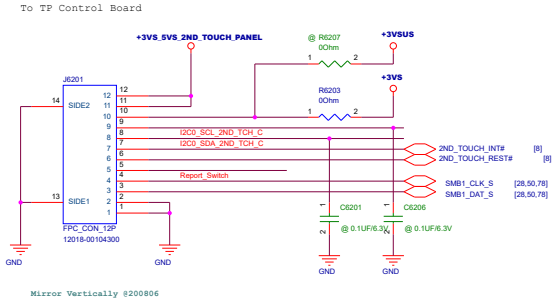
Date: Friday, November 06, 2020 Sheet 59 of 104

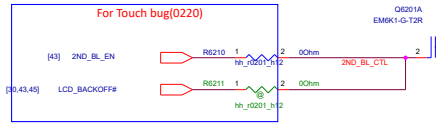
ASUSTeK COMPUTER	Title : ME_Screw Hole & Nut	
	Engineer: EE	
Size: A	Project Name: GX502GX	Rev: R1.0
Date: Friday, November 06, 2020	Sheet 67 of 104	

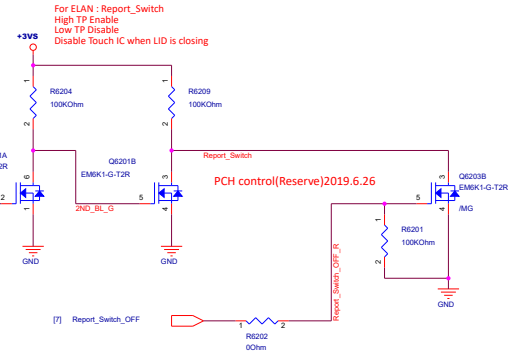
<Core Design>

ASUSTeK COMPUTER	Title : OTH_for test only	
	Engineer: EE	
Size: A	Project Name: GX502GX	Rev: R1.0
Date: Friday, November 06, 2020	Sheet 68 of 104	

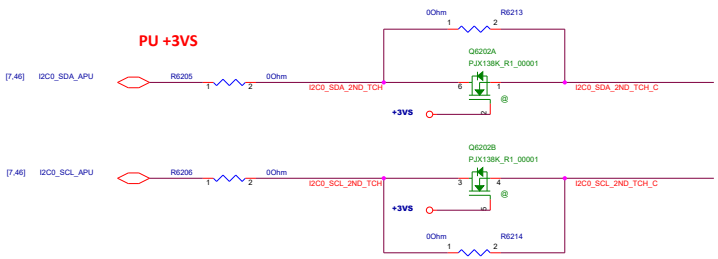


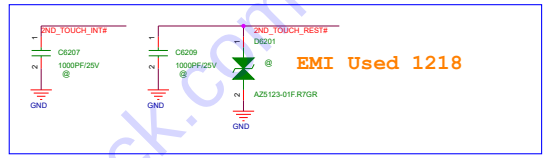






2nd Display Touch





ASUS	Project Name: GX550LXS	Rev: R1.0
Title : TOUCH_1		
Size: C	Dept.: NB_Power team	Engineer: Benson
Date: Friday, November 06, 2020	Sheet 62 of 104	

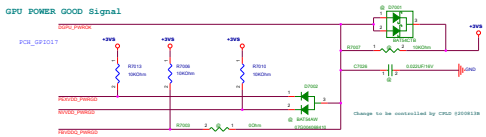
Title : NGFF SSD(MAXIM)

ASUSTeK COMPUTER

Engineer: Wendell_Lo

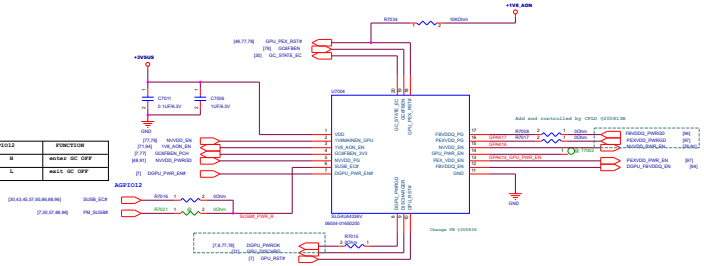
Size	Project Name	Rev
A	**GL752VW**	R1.0

Date:	Friday, November 06, 2020	Sheet	63	of	104



GPU POWER SEQUENCE CONTROL

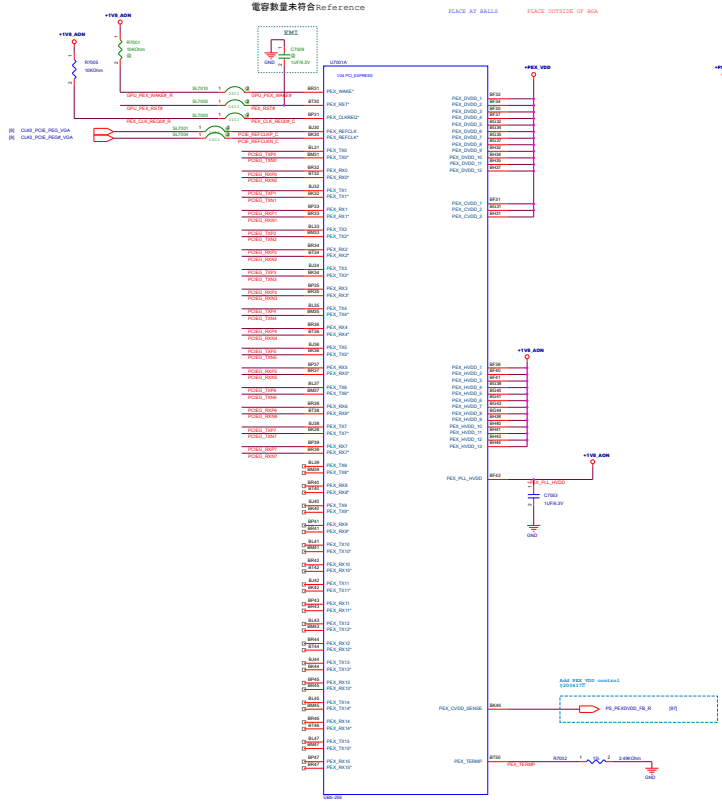
AGPIO12	FUNCTION
H	enter GC OFF
L	exit GC OFF



2013/6/21 change CPLD I2008138 PLD0102R00
2013/7/15 change PLD0102R00 part to PA004-0134S102

電容數量未符合Reference

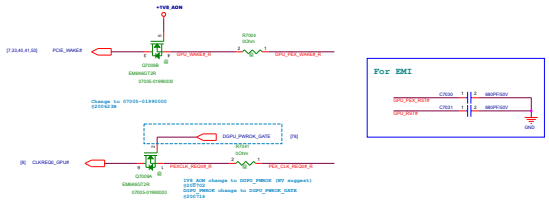
PLACE AT BALLS PLACE OUTSIDE OF BGA



6 x 1.0 uF(0402)
2 x 4.7uF(0603)
Place near GPU balls
Max:77mA
3 x 10uF(0805)
2 x 22uF(0805)
Place between GPU & PS
C7021, C7029 change to 10uF 0402 I2007016

9 x 1.0 uF(0402)
2 x 4.7uF(0603)
Place near GPU balls
Max:97mA
3 x 10uF(0805)
2 x 22uF(0805)
Place between GPU & PS

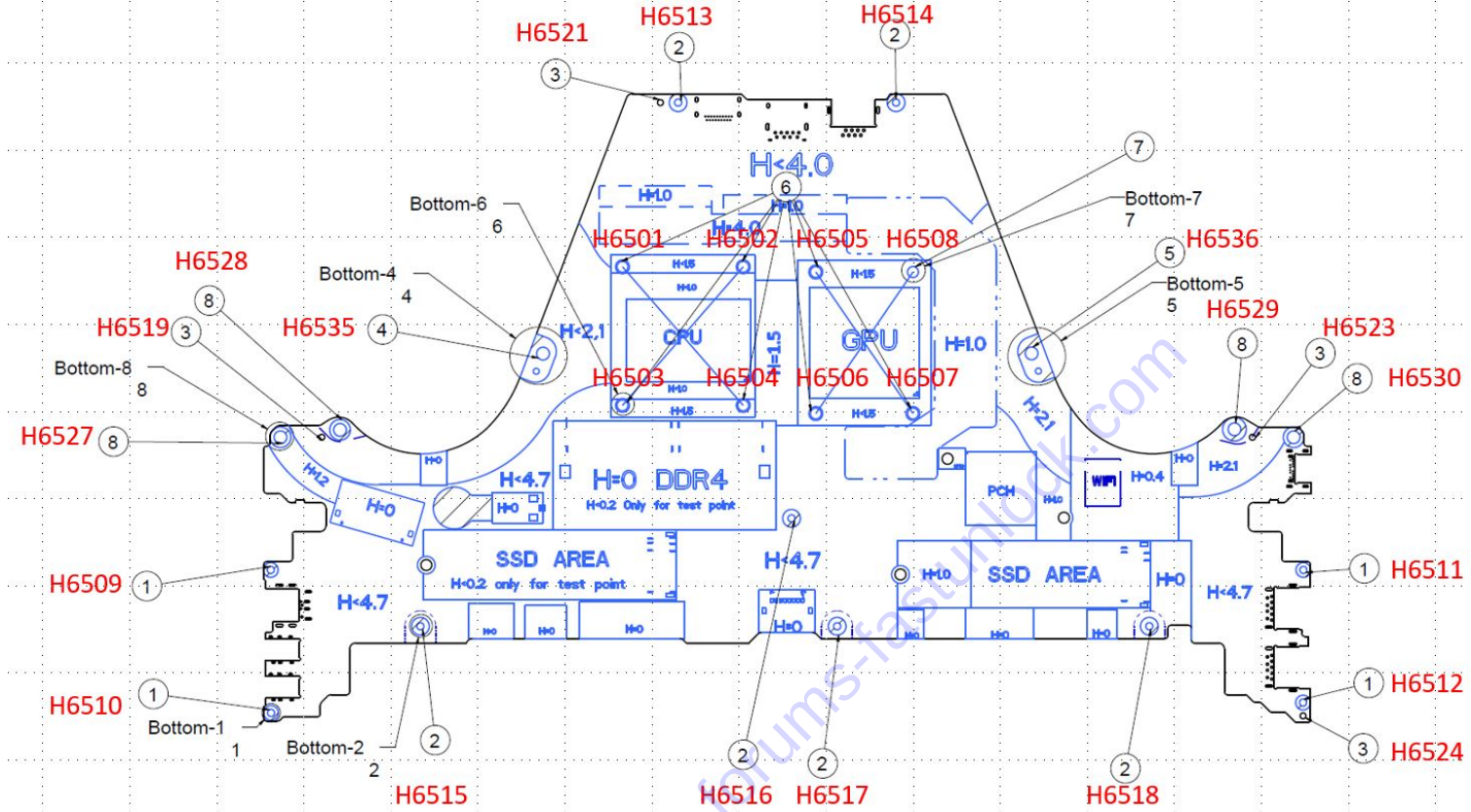
PCIEIG x8 TX Capacitors



ASUS	Project Name: GX502GX		Rev: 3G.2
Title : GPU PCIE I/F			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:	
Date: Friday, November 08, 2013	Sheet 79 of 101		

Main Board

Main Board



GPU

TOP 3.7/6.5, BOT 3.7/4.7

H6505 1 @ CT256CB185D146
H6506 1 @ CT256CB185D146
H6507 1 @ CT256CB185D146
H6508 1 @ C146D146N

CPU

TOP 3.7/6.5, BOT 3.7/4.7

H6501 1 @ CT256CB185D146
H6502 1 @ CT256CB185D146
H6503 1 @ CT256CB185D146
H6504 1 @ CT256CB185D146

1

GND 1 H6509 C197D94 @
GND 1 H6510 C197D94 @
GND 1 H6511 C197D94 @
GND 1 H6512 C197D94 @

2

GND 1 H6513 C236D94 @
GND 1 H6514 C236D94 @
GND 1 H6515 C236D94 @
GND 1 H6516 C236D94 @
GND 1 H6517 C236D94 @
GND 1 H6518 C236D94 @

3

1 H6519 s05823 @ O106X83DO106X83N
1 H6521 s04715 @
1 H6523 s05823 @ O106X83DO106X83N
1 H6524 s04715 @

4

H6535 1 2 2D_D169_D79 @

5

H6536 1 2 2D_D169_D79 @

8

GND 1 H6527 C276D169 @
GND 1 H6528 C276D169 @
GND 1 H6529 C276D169 @
GND 1 H6530 C276D169 @

GND 1 U6502 1 GASKET_1P 13040-00440000
GND 1 U6503 1 SMD239X89 13060-00031500
GND 1 U6504 1 SMD239X89 13060-00031500

<Core Design>

ASUSTeK COMPUTER

Title : I/O board FUNC key

Engineer: EE

Size	Project Name	Rev
B	GX550LXS	R1.0

Date: Friday, November 06, 2020 Sheet 65 of 103

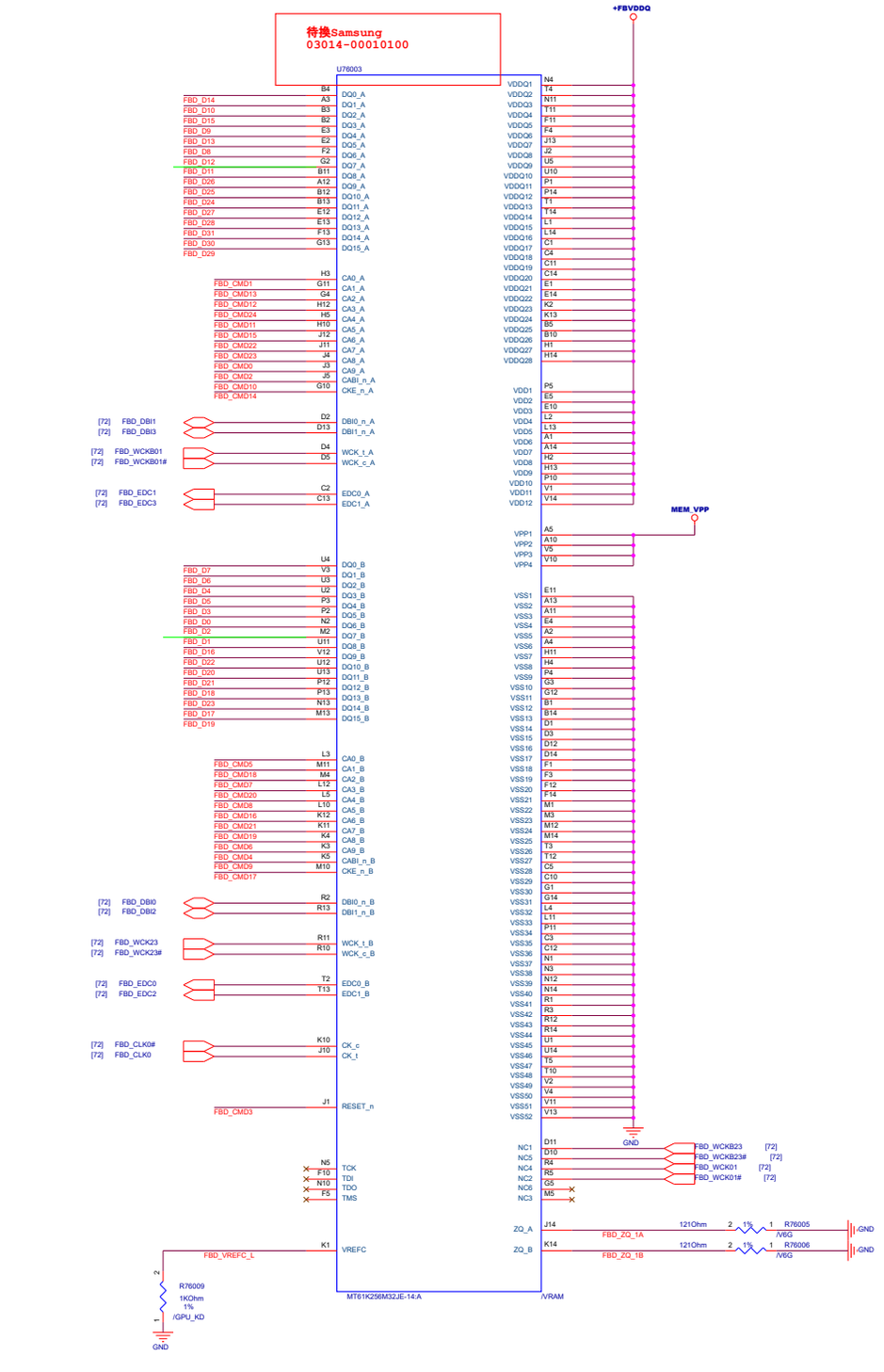
[72] FBD_D[31..0]

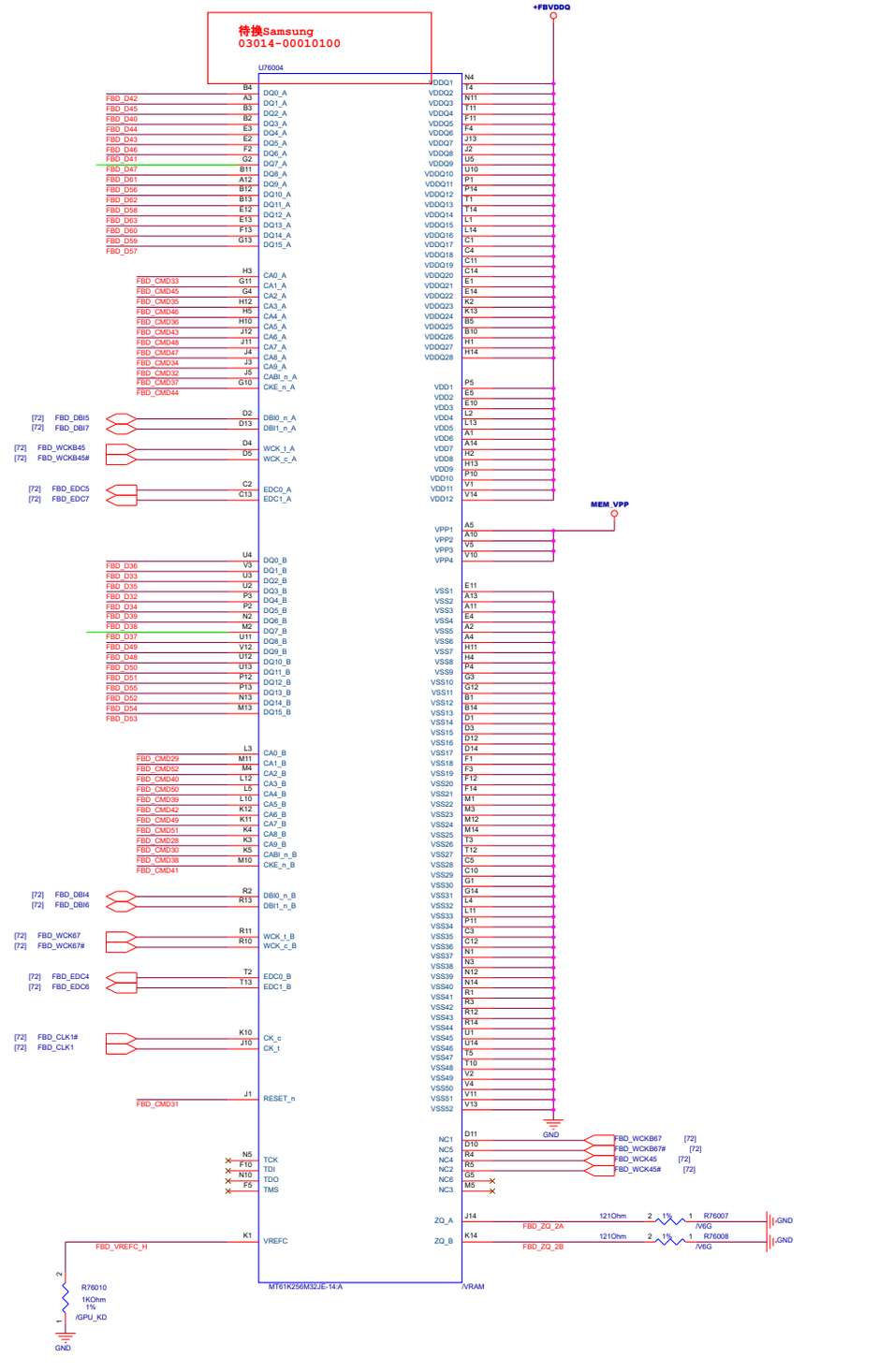
[72] FBD_CMD[52..0]

40 OHm_NET
FBD Partition 31..0
MF=1 Mirror

[72] FBD_D[63..32]

40 OHm_NET
FBDPartition 64..32
MF=0 Normal





Project Name: GX502GX			Rev: R1.2
Title : VRAM_Channel_D			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:	
Date: Friday, November 06, 2020	Sheet 76 of 101		

[72] FBA_D[31..0]

[72] FBA_CMD[52..0]

40 OHm NET
FBA Partition 31..0
MF=1 Mirror

[72] FBA_D[63..32]

40 OHm NET
FBA Partition 64..32
MF=0 Normal

待換Samsung
03014-00010100

U73001

U73002

+FBVDDQ

MEM_VPP

GND

MT61K256M32JE-14:A

/VRAM

R73005 1KOhm 1% /GPU_KA

R73006 1KOhm 1% /GPU_KA

FBA_ZQ_1A 121Ohm R73001 /GPU_KA

FBA_ZQ_1B 121Ohm R73002 /GPU_KA

FBA_ZQ_2A 121Ohm R73003 /GPU_KA

FBA_ZQ_2B 121Ohm R73004 /GPU_KA

Project Name	GX502GX		Rev R1.2
Title :	VRAM_Channel_A		
Size Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:	
Date: Friday, November 06, 2020	Sheet 73 of 101		

[72] FBB_D[31..0]

[72] FBB_CMD[52..0]

40 OHm_NET
FBB Partition 31..0
MF=1 Mirror

[72] FBB_D[63..32]

40 OHm_NET
FBB Partition 64..32
MF=0 Normal

待換Samsung
03014-00010100

U74003

MT61K256M32JE-14:A

/VRAM

待換Samsung
03014-00010100

U74004

MT61K256M32JE-14:A

/VRAM

+FBVDDQ

MEM_VPP

GND

FBB_VREFC_L

FBB_VREFC_H

R74009 1KOhm 1% /GPU_KB

R74010 1KOhm 1% /GPU_KB

FBB_ZQ_1A

FBB_ZQ_1B

FBB_ZQ_2A

FBB_ZQ_2B

R74005 /GPU_KA

R74006 /GPU_KA

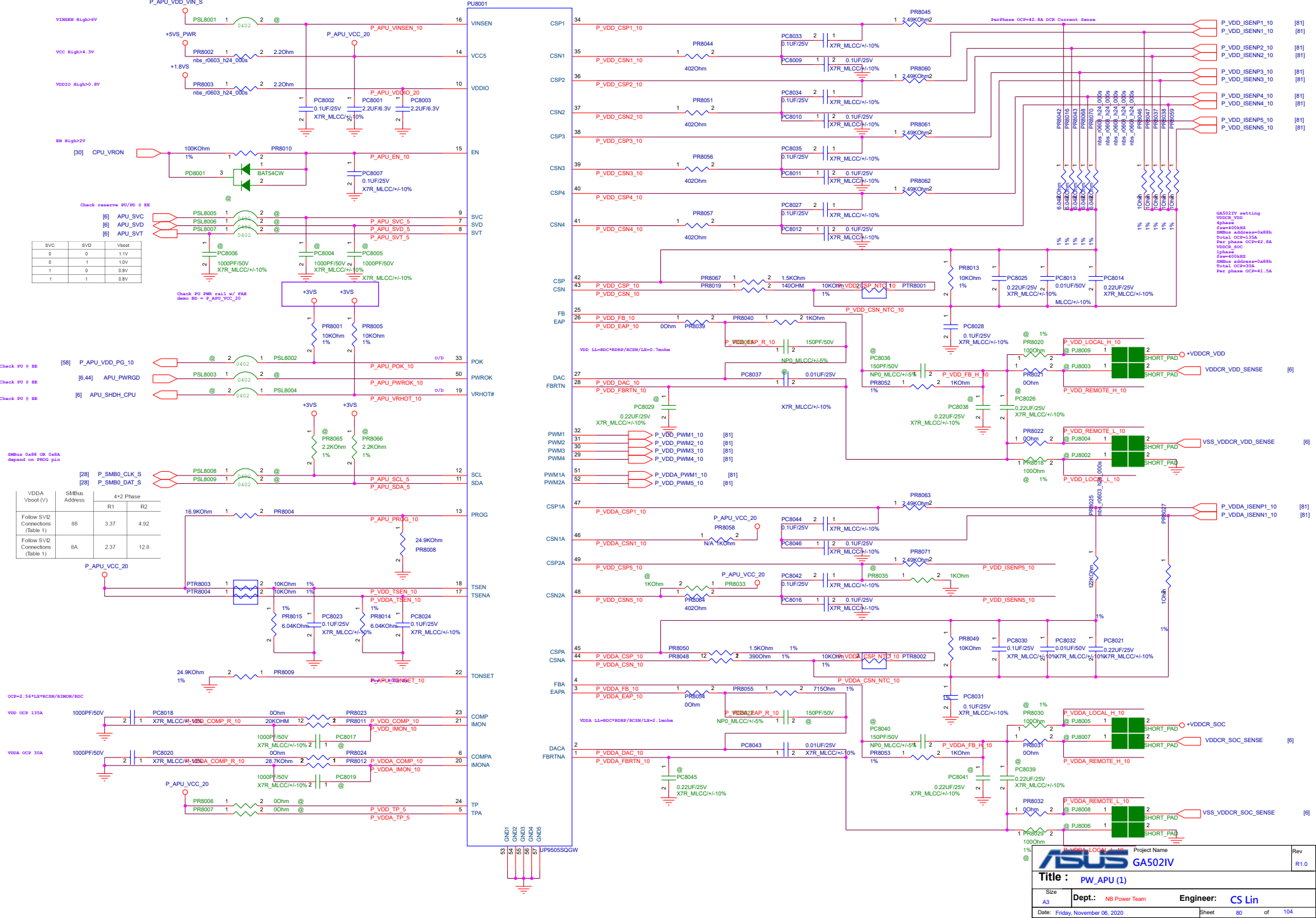
R74007 /GPU_KA

R74008 /GPU_KA

121Ohm 2 1% 1

/GND

Project Name	GX502GX		Rev R1.2
Title :	VRAM_Channel_B		
Size Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:	
Date: Friday, November 06, 2020	Sheet 74 of 101		



SVC	SVD	Vboot
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

VDDA Vboot (V)	SMBus Address	4+2 Phase	
		R1	R2
Follow SVI2 Connections (Table 1)	88	3.37	4.92
Follow SVI2 Connections (Table 1)	8A	2.37	12.8

[72] FBC_D[31..0]

[72] FBC_CMD[52..0]

40 OHm_NET
FBC Partition 31..0
MF=1 Mirror

待換Samsung
03014-00010100

U75003

+FBVDDQ

MEM_VPP

GND

MT61K256M32JE-14:A

/VRAM

R75009
1KOhm
1%
/GPU_KC

[72] FBC_D[63..32]

40 OHm_NET
FBC Partition 64..32
MF=0 Normal

待換Samsung
03014-00010100

U75004

+FBVDDQ

MEM_VPP

GND

MT61K256M32JE-14:A

/VRAM

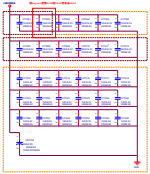
R75010
1KOhm
1%
/GPU_KC

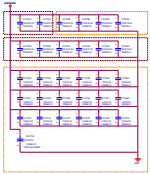
ASUS	Project Name: GX502GX		Rev: R1.2
Title : VRAM_Channel_C			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:	
Date: Friday, November 06, 2020	Sheet 75 of 101		

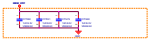
FBVDDQ
VRAM side

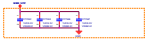
FBVDDQ
GPU side

Channel A

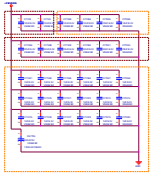


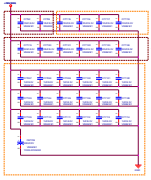


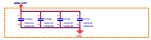


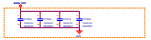


Channel B

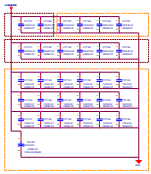


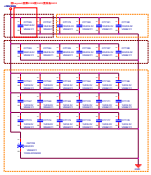




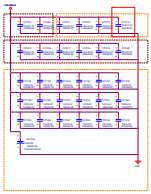


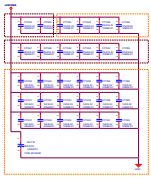
Channel C

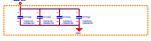


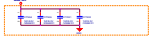


Channel D

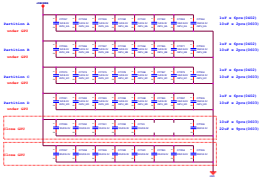








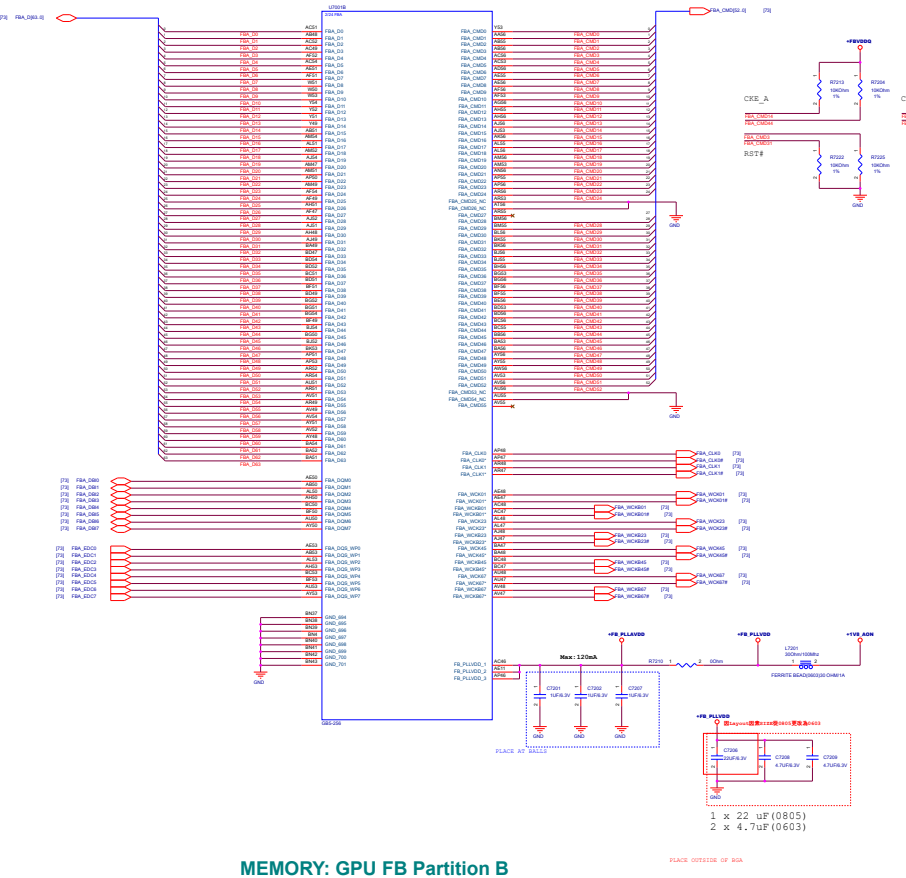
VRAM PWR_FBVDDQ



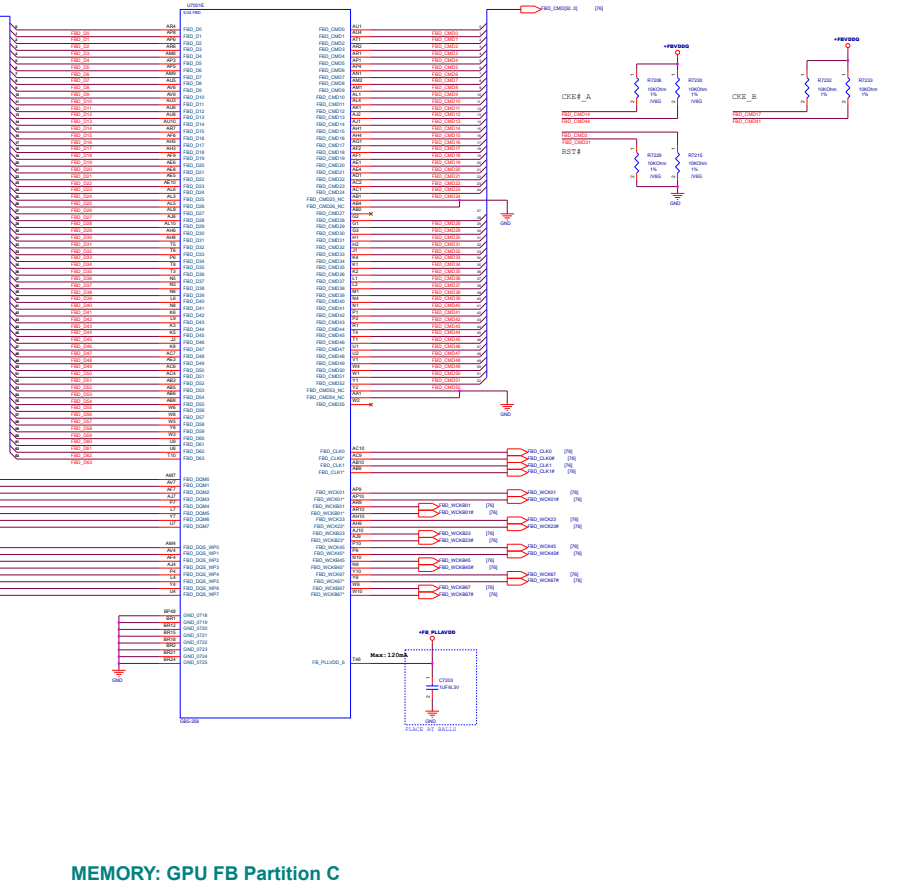
For power sequence measurement

Title						
Size	Number			Revision	1.0	
Date:		Sheet of		File:		

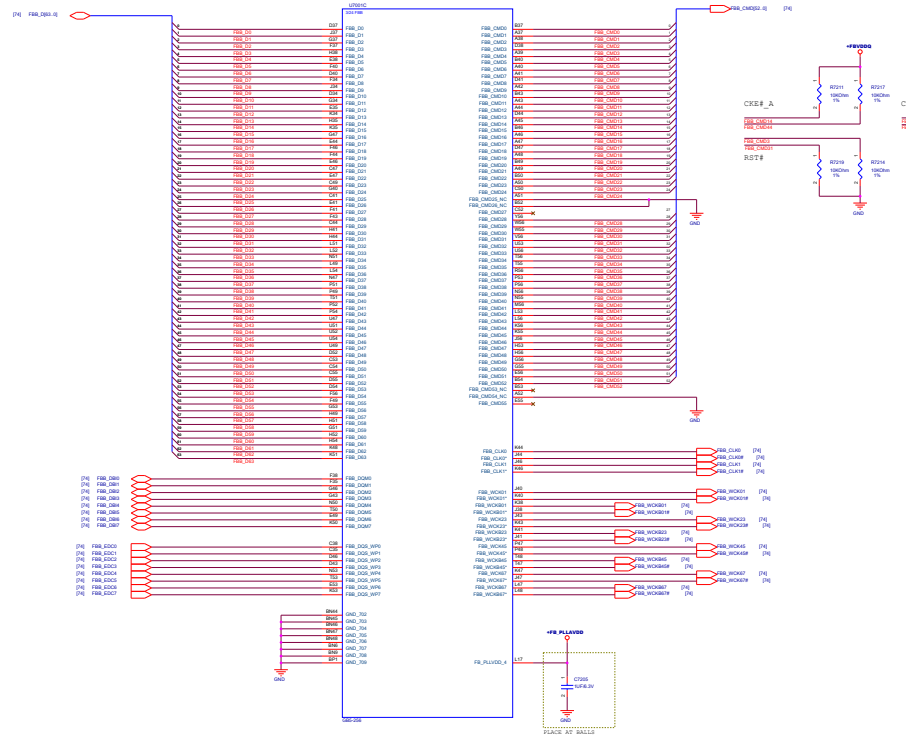
MEMORY: GPU FB Partition A



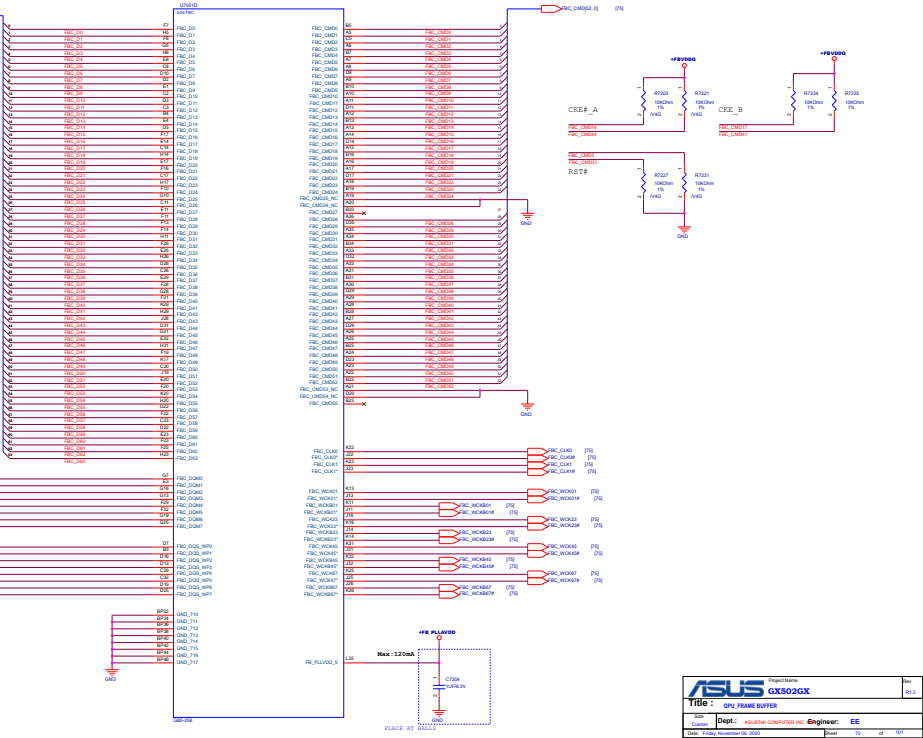
MEMORY: GPU FB Partition D



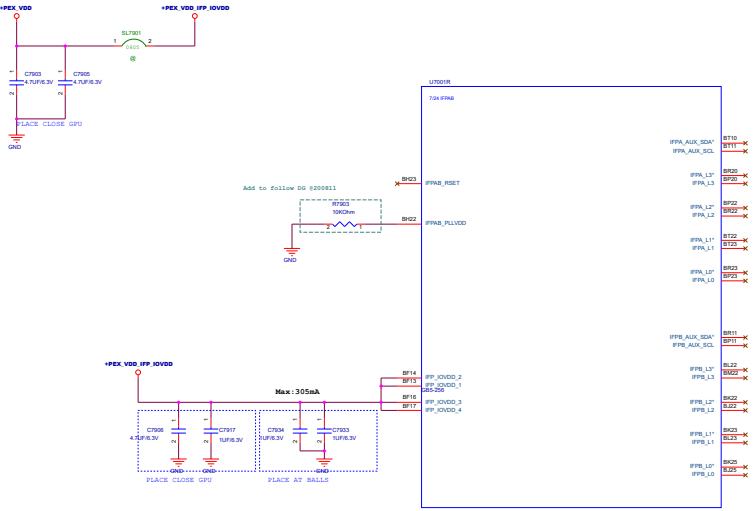
MEMORY: GPU FB Partition B



MEMORY: GPU FB Partition C



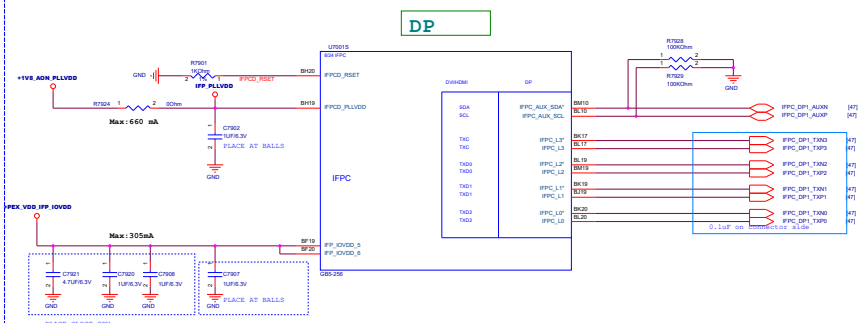
ASUS	Project Name: GX502GX		Rev: R1.2
Title : GPU_FRAME BUFFER			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Friday, November 06, 2020	Sheet 72 of 161		

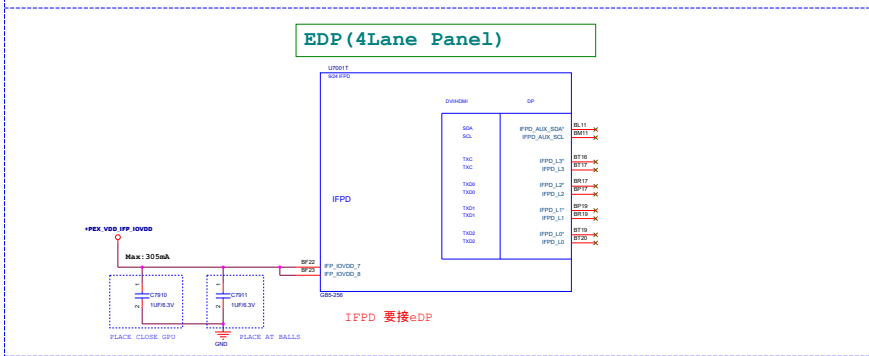


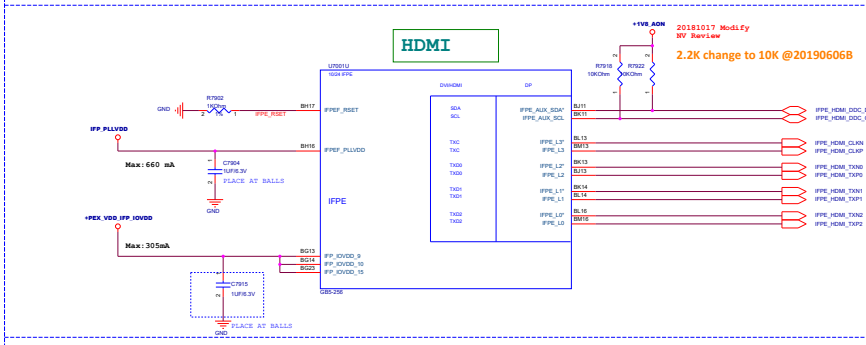
7.2 Unused pins

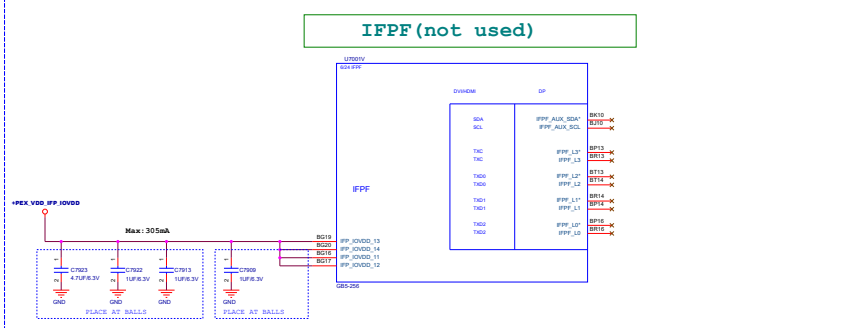
If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPxy_RSET (xy = AB,CD,EF) can be left unconnected and IFPxy_PLLVDD should be 10K PD to GND if neither of IFPx /IFPy is in use. For example, if neither link of the IFPA/IFPB macro is to be used, then IFPAB_PLLVDD must be 10K PD to GND, IFPAB_RSET should be left unconnected, and all signals and references associated with Link A and Link B should also be left unconnected.

IFP_IOVDD rail can be left unconnected if no IFP link is used. If any IFP is used; all IFP_IOVDD balls must be connected to power rail.

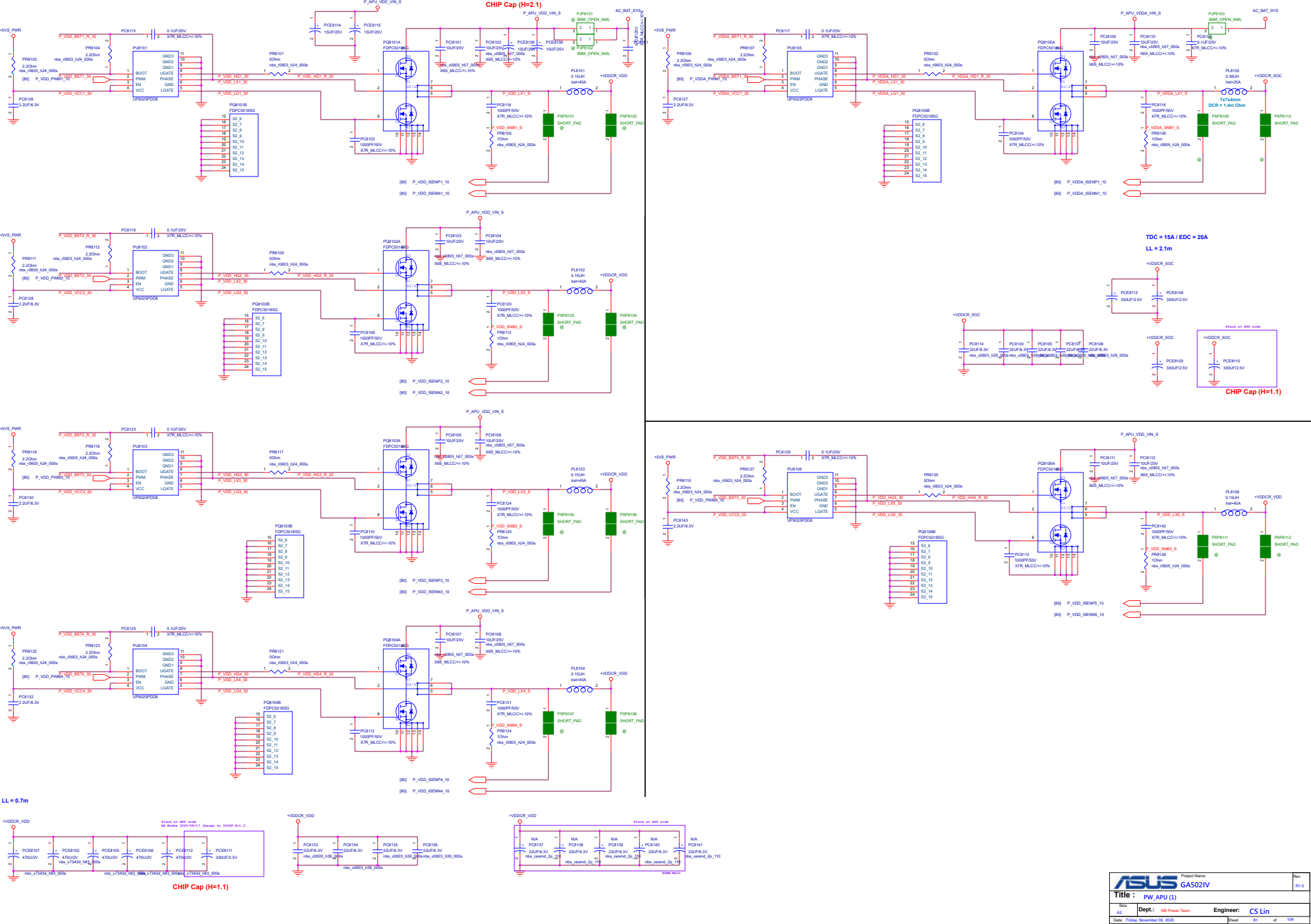


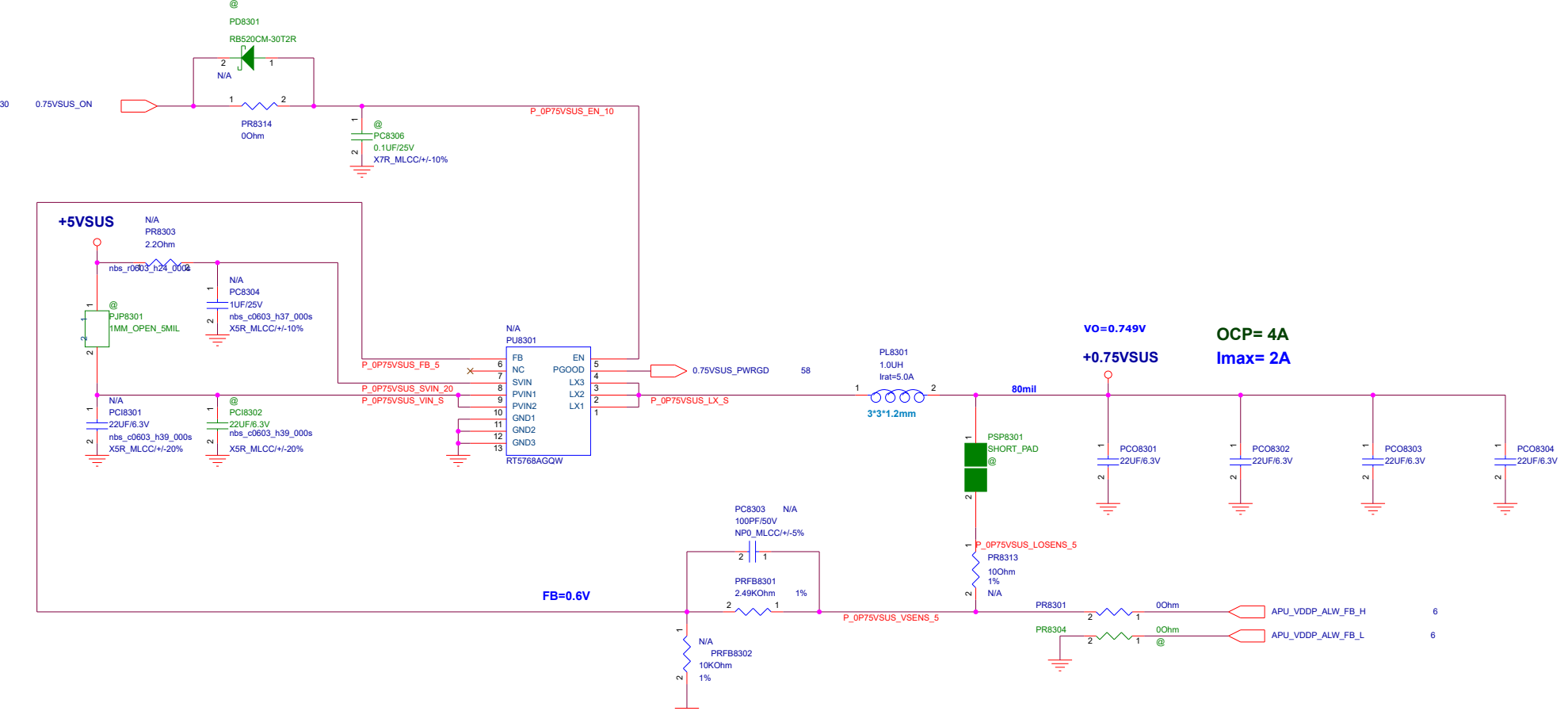






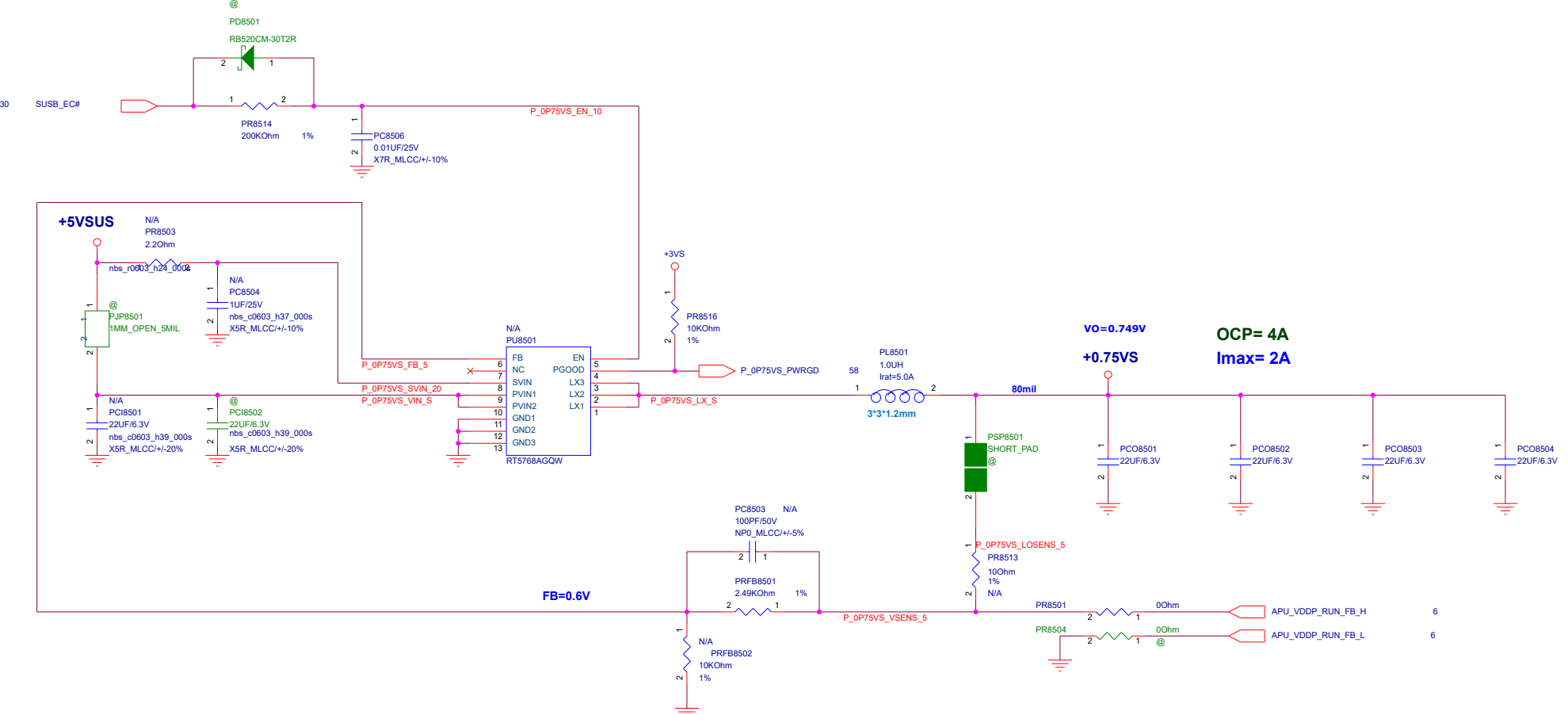
ASUS	Project Name: GX502GX		Rev: R1.2
Title : GPU_DP/EDP/HDMI/LVDS/CRT			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Friday, November 06, 2020	Sheet: 79	of: 101	


CHIP Cap (H=2.1)
TDC = 15A / EDC = 20A
LL = 2.1m
CHIP Cap (H=1.1)
LL = 0.7m
CHIP Cap (H=1.1)
Project Name GA502IV
Rev R1.0
Title : PW_APU (1)
Size A2
Dept.: NB Power Team
Engineer: CS Lin
Date: Friday, November 06, 2020
Sheet 81 of 104



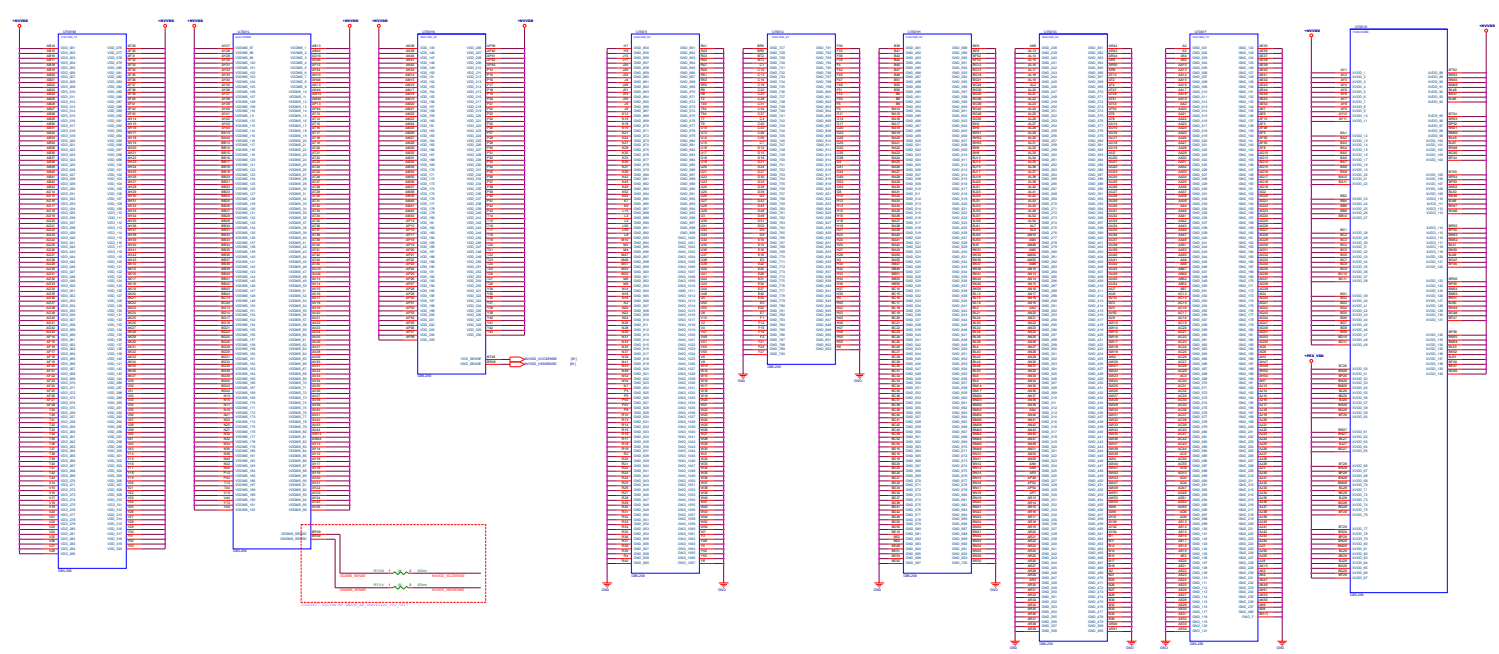
<Variant Name>

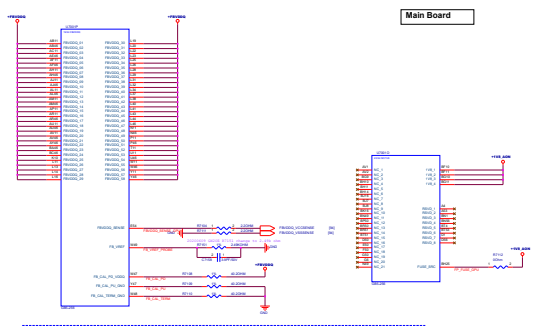
ASUS	Project Name: GA503QS	Rev: R1.0
Title : PW_+0.75VSUS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Friday, November 06, 2020	Sheet 83 of 104	

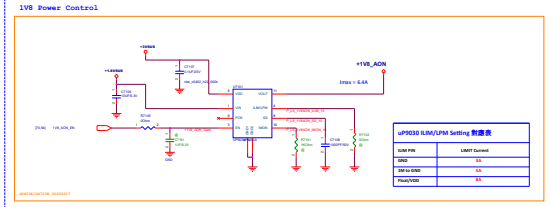


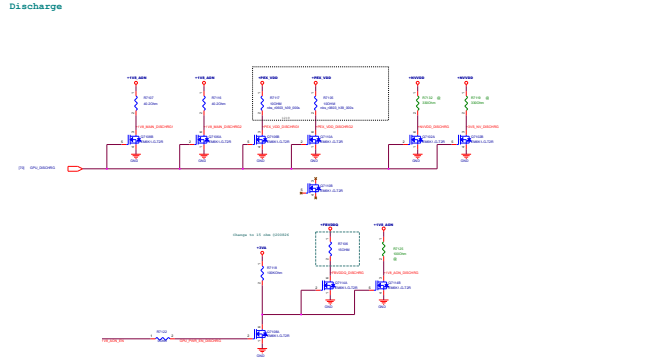
<Variant Name>

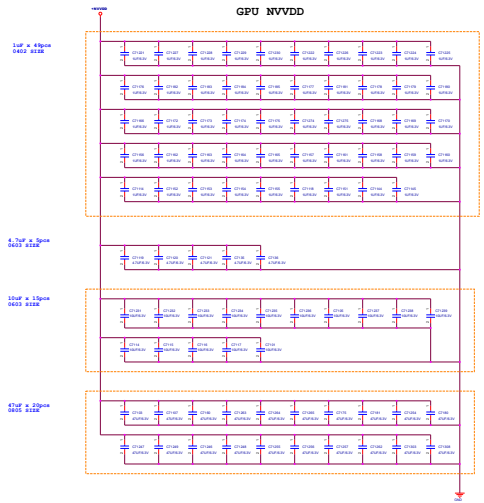
ASUS	Project Name: GA503QS	Rev: R1.0
Title : PW_+0.75VS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Friday, November 06, 2020	Sheet 85 of 104	

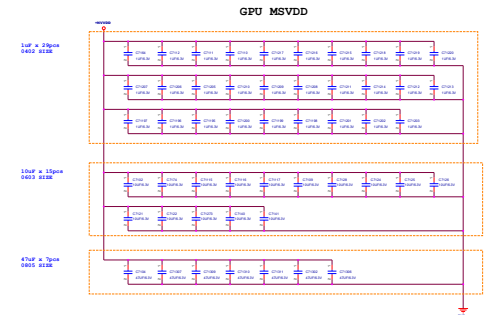


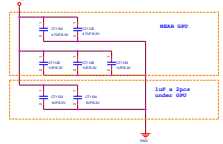

Main Board


1V8 Power Control
+1V8_AON
Imax = 6.6A
uP9030 ILIM/LPM Setting 對應表
SUM PIN
LIMIT Current
GND
5A
SW to GND
6A
Float/VDD
8A

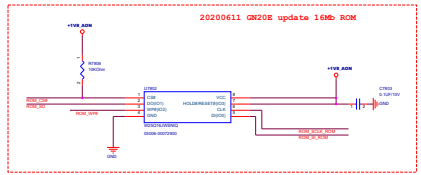

Discharge

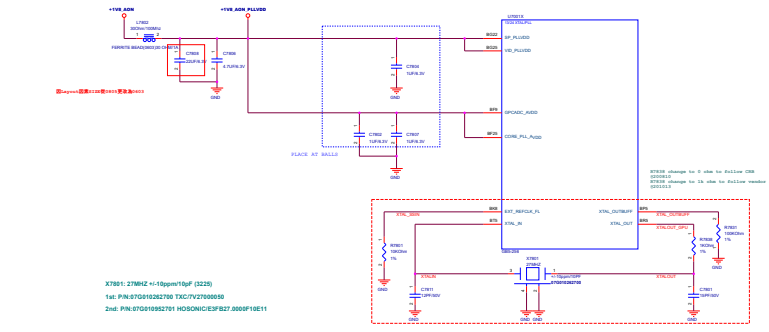

GPU NVVDD
1uF x 49pcs
0402 SIZE
4.7uF x 9pcs
0603 SIZE
10uF x 15pcs
0603 SIZE
47uF x 20pcs
0805 SIZE

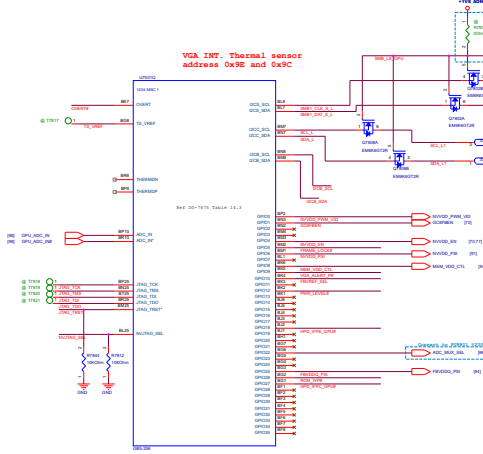

GPU MSVDD
1uF x 29pcs
0402 SIZE
10uF x 15pcs
0603 SIZE
47uF x 7pcs
0805 SIZE


NEXA GPU
1uF x 2pcs
under GPU

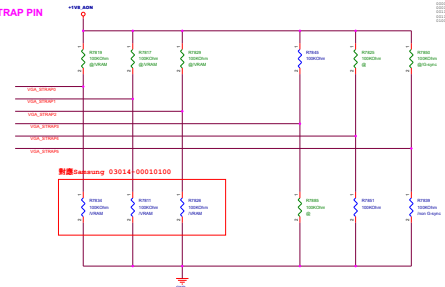

ASUS
GX502GX
Title : GPU_POWER
Engineer: EE

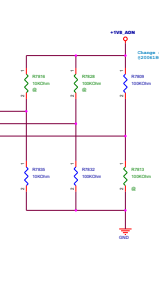






STRAP PIN





Level Option	Physical Configuration	
	Pull-Up to 1.8V via resistor (see Note 1). (Notebook designs also see Note 2.)	Pull-Down to GND via resistor Note 1
1.8V ("HIGH") Level	Populate	No Stuff
0.9V ("MIDDLE") Level	Populate	Populate
GND ("LOW") Level	No Stuff	Populate

Note 1: Resistor should be 10K Ohms 5% tolerance is acceptable.
Note 2: Notebook graphics circuit designs should pull up to the 1V8_AON rail rather than to 1V8 MAIN.

Strap Pins see Note			F1_OVERT Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	F1_OVERT function DISABLED
L	L	H	F1_OVERT function DISABLED (Invalid; do not configure)
all other configurations			(Invalid; do not configure)

DEFULT : L L L

Table 1 GN20-E7 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDDQ	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Data Code start	Qual Plan	Status
16 Gb	2Chx32Mx16	1.35V	Samsung	K4ZAF325BM-HC14	M-die	0x9	14 Gbps	N/A	Full	Production candidate
		1.25V	Micron	TBD	TBD	0x7	16 Gbps	2140	Full	Production candidate
		1.25V	Hynix	TBD	JHA	0x6	16 Gbps	N/A	Full	Production candidate
8 Gb	2Chx25Mx16	1.35V	Samsung	K4ZAF325BC-HC16	C-die	0x0	16 Gbps	2001	Full	Production candidate
		1.25V	Hynix	H56G20AAP-DNL	A-die	0x2	14 Gbps	N/A	Full	Production candidate
		1.25V	Micron	MT61K256M32JE-14:A	A-die	0x4	14 Gbps	1947	Full	Production candidate

Strap Pins see Note			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
STRAP2	STRAP1	STRAP0	
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	H	M	9 (0x0009)
L	M	H	10 (0x000A)
L	M	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins see Note			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
STRAP2	STRAP1	STRAP0	
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	1	1
L	H	L	0	0	M	0
L	H	H	0	1	0	0
H	L	L	0	1	1	0
H	L	H	0	1	M	0
H	H	L	1	0	0	1
H	H	H	1	0	1	1
L	L	M	1	0	M	1
L	M	L	1	1	0	1
L	M	H	1	1	1	1
L	M	M	1	1	M	1
M	L	L	1	1	0	0
M	L	H	1	1	1	1
M	H	H	1	1	1	1

Assorted Configuration Straps-
1. SMB_ALT_ADDR Enable: <u>0" signal SPI setting I2C5 address 0x9E</u>, "1" final SPI setting I2C5 address 0x9E/0xC, Level effect associated SPI
2. DEVID_SEL: G-sync function->"0"normal GPU ID, "1" support G-sync GPU ID-
3. PCIE_CFG: PCIE Swing ->"0" PCIE Swing default, "1" PCIE swing reduce-
4. VGA_DEVICE: Graphics circuit ->"0"_MS-Hybrid, "1" Discrete-

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

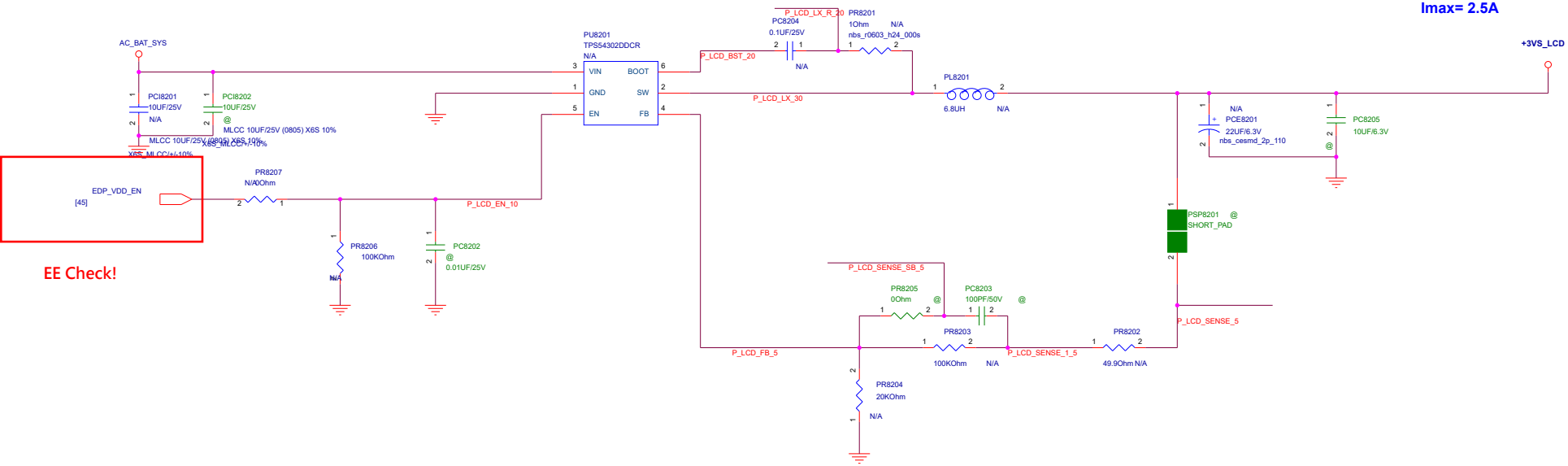
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

DEFULT : L L H

Project Name	GX502GX
Rev.	R1.2
Title :	GPU CLOCK/STRAP/GPIO
Size	Dept.: AUDIO&COMPUTER-MI Engineer: EE
Custom	
Date: Friday, November 08, 2019	Sheet 19 of 101

+3VS_LCD



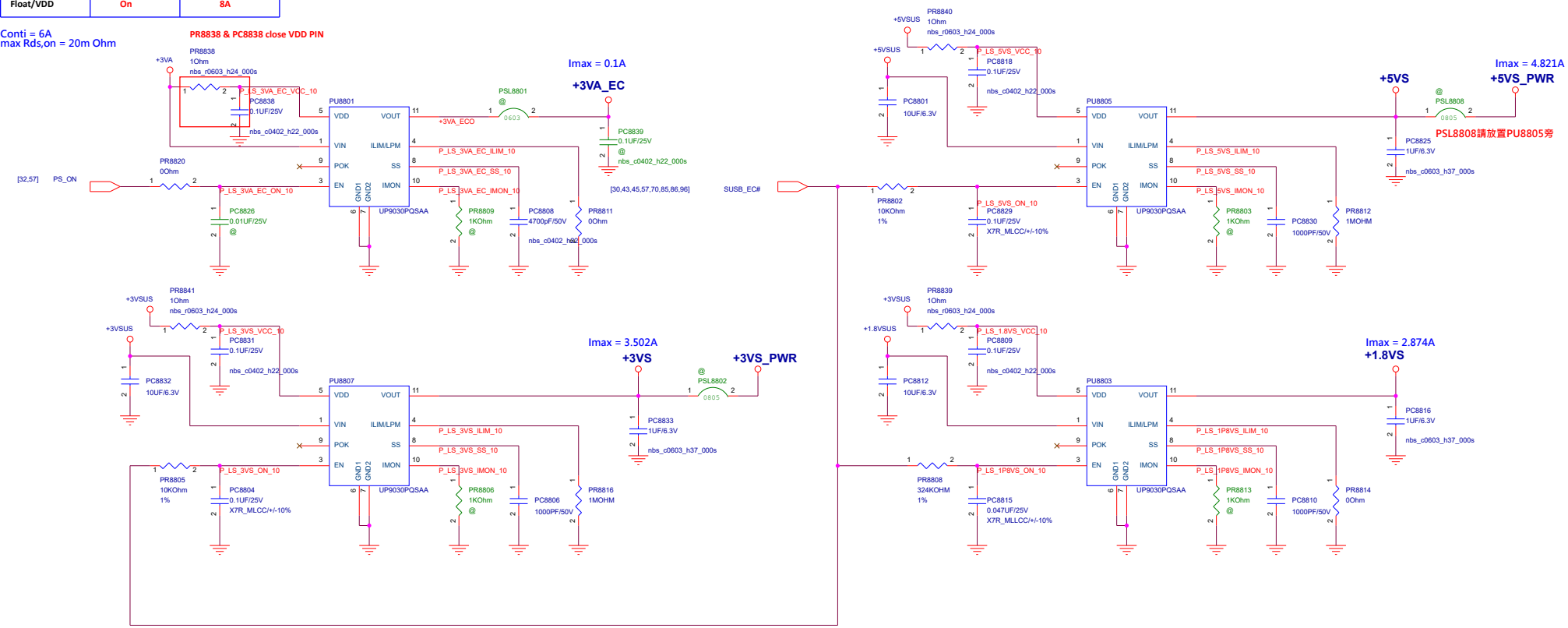
Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Friday, November 06, 2020	Sheet 82 of 104	

uP9030 ILIM/LPM Setting 對應表

ILIM PIN	LPM	LIMIT Current
GND	Off	3A
1M to GND	Off	5A
Float/VDD	On	8A

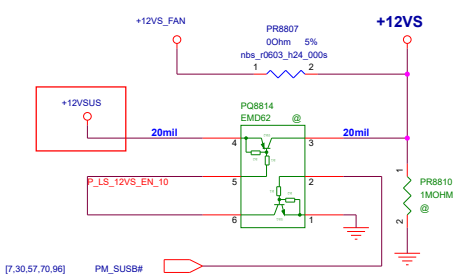
Conti = 6A
max Rds,on = 20m Ohm

PR8838 & PC8838 close VDD PIN



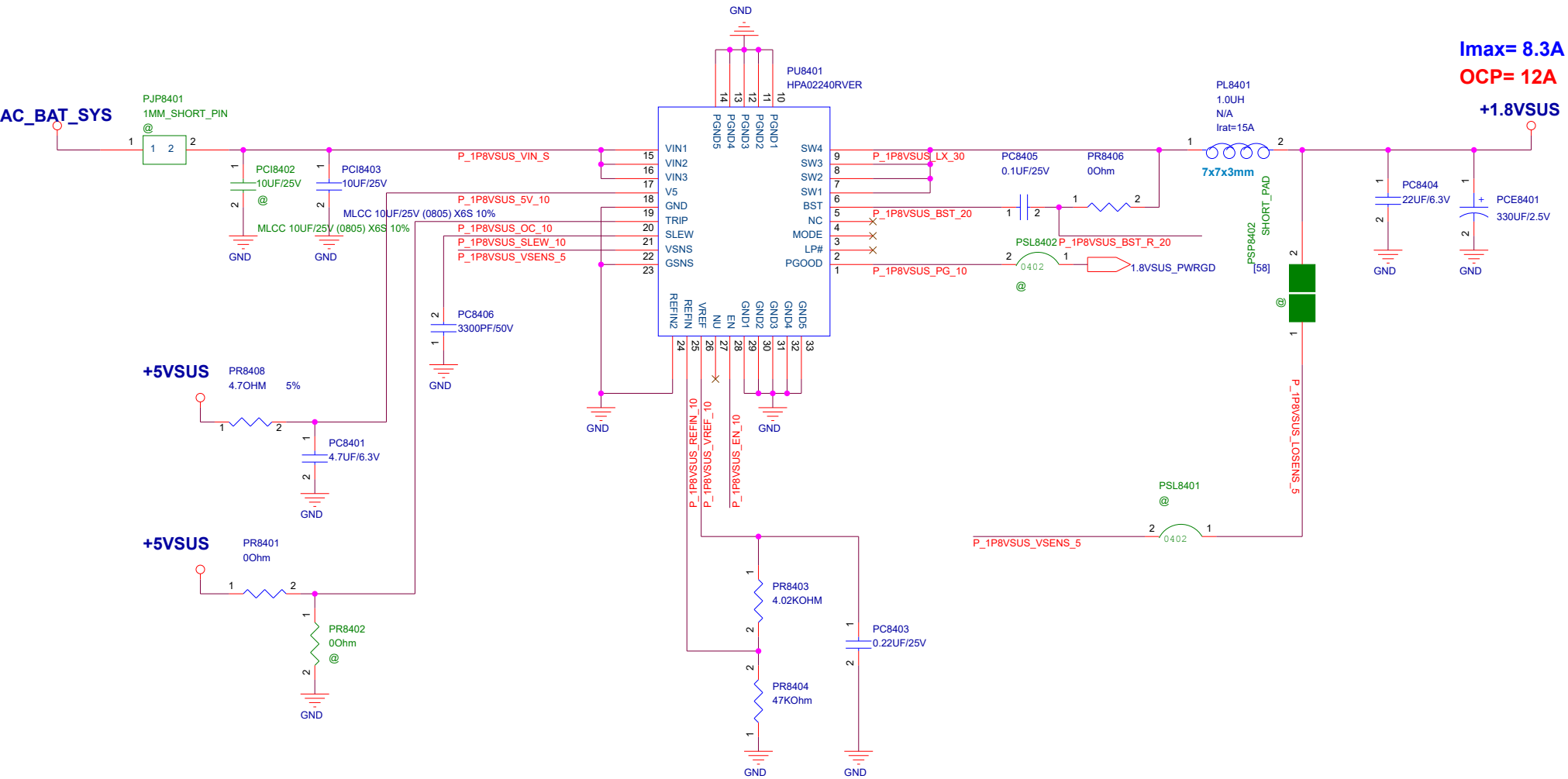
+12VS 的 Vin 對應 BOM 表

	+12VS_FAN	+12VSUS
PR8807	N/A	@
PR8810	@	N/A
PQ8814	@	N/A



ASUS	Project Name: GA503QS	Rev: R1.0
Title : PW_LOAD SWITCH		
Size: A3	Dept.: NB Power Team	Engineer: CS Lin
Date: Friday, November 06, 2020	Sheet 88 of 104	

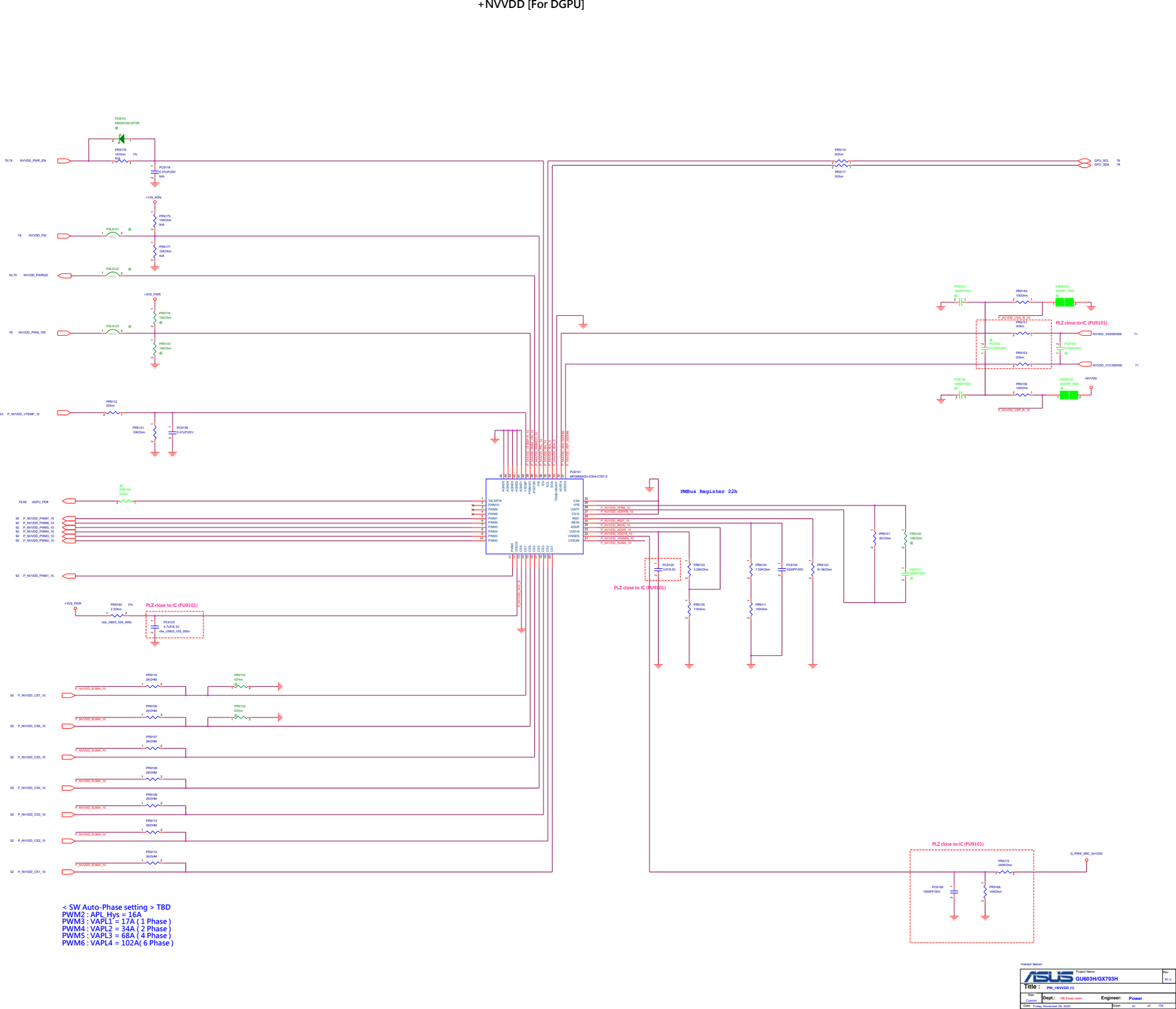
+1.8VSUS [For PCH]



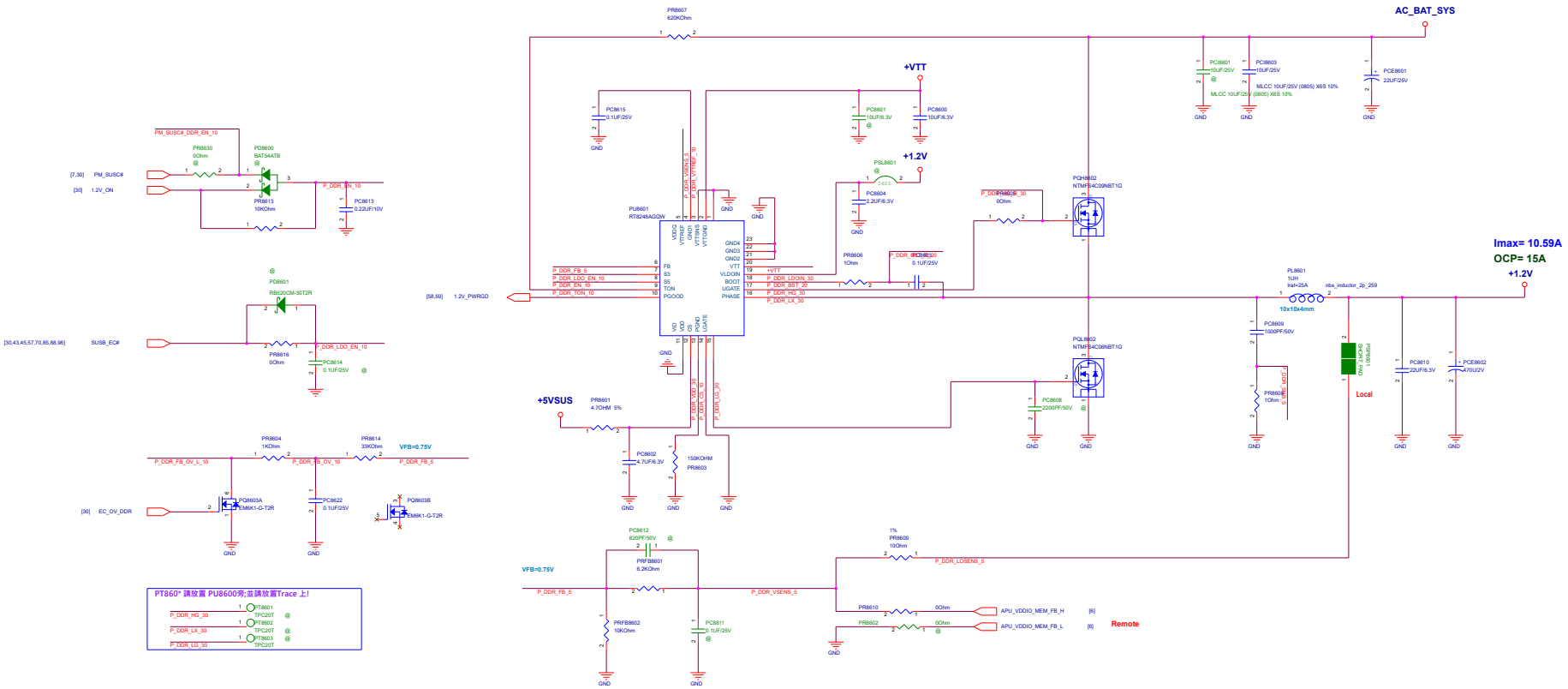
<Variant Name>

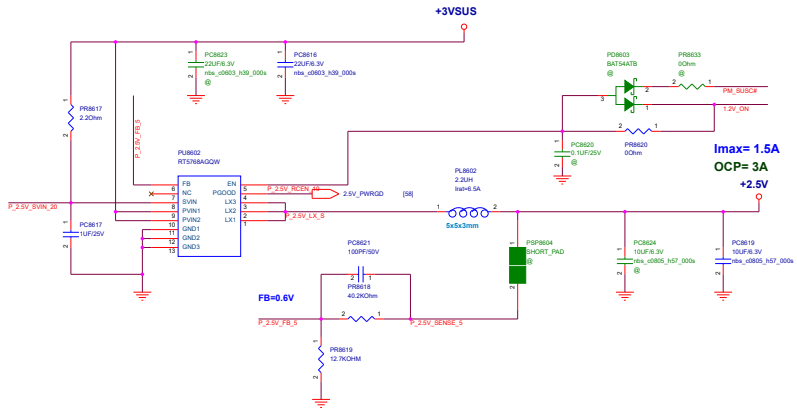
Project Name: Project Name		Rev: R1.0
Title : PW_+1.8VSUS		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Friday, November 06, 2020	Sheet 84 of 104	

+NVVDD [For DGPU]



+1.2V / +VTT / +2.5V[For Memory]





Main Board

PRS8901	ADP<120W	ADP<=230W	ADP>230W	ADP>330W
	TBD	5m	5m	2m
	TBD	10125-0008B100	10108-0004B000	10108-0008B000

AD : 17.8V

I limit : Charge 6A
DisCharge 24A

AC limit = 100% ADP
Bat limit = byte 7 x 1.7

AD : 17.5V
Place Close to PJ8901

dGPU_PD# ---> GPIO12(EE page 75 or 78)

HW_Throttle

Plug HW Throttle(Out)

Plug HW Throttle(In)

POP window

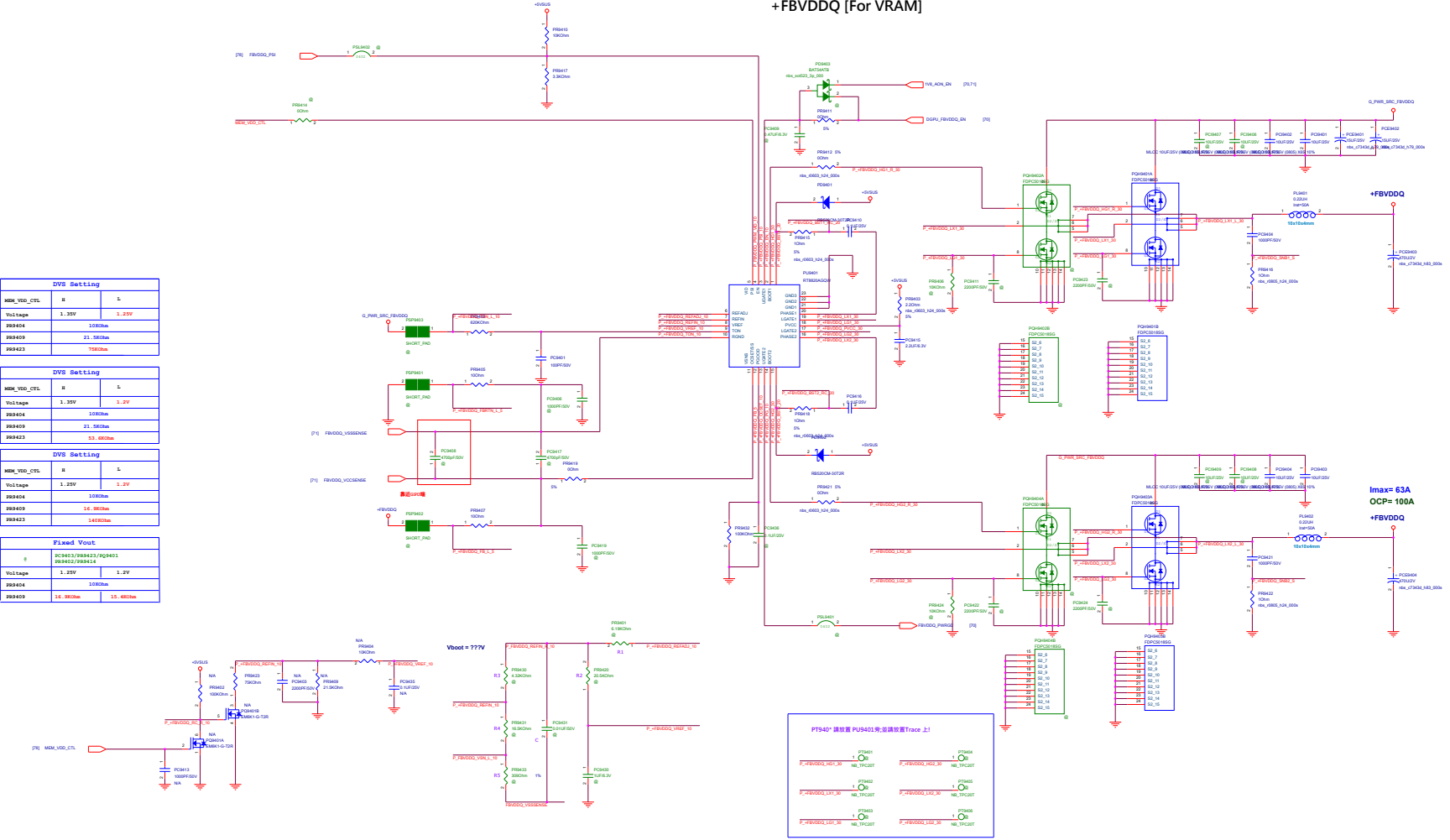
Adaptor select
total power = 90% ADP

Adaptor select

		3 Series	2 Series
PRS8901		10m	5m
PR8936			
14K (100212143403)	0.4V	45W	120W
31.6K (100212143403)	0.8V	150W	150W
56K (100212143403)	1.2V	180W	180W
93.1K (100212143401)	1.6V	65W	230W
150K (100212143403)	2.0V	NA	280W
270K (100212143403)	2.4V	90W	330W
560K (100212143403)	2.8V	120W	240W

Project Name	Coffee lake-H
Rev	R1.0
Title :	PW_CHARGER
Size	A3
Dept. :	MB Power Team
Engineer:	Benson
Date:	Friday, November 06, 2020
Sheet	89 of 104

+FBVDDQ [For VRAM]



Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, November 06, 2020	Sheet 95 of 104	

GM531GX R1.0 SKU Table

			CPU	Power	DIMM	VRAM			
Option	PCB	SKU							
60NB0H10-MB1030	R1.0	GM531GX SKU1	/I7-7700HQ	/230W	TBD	VBG_Micron			
60NB0H10-MB2000	R1.0	GM531GX SKU2	/I5-7300HQ	/230W	TBD	VBG_Samsung			

ASUSTeK COMPUTER

Title : GM531GX SKU Table R1.0

Engineer: EE

Size: C | Project Name: GX502GX | Rev: 1.0

Date: Friday, November 03, 2017 | Sheet: 103 of 104

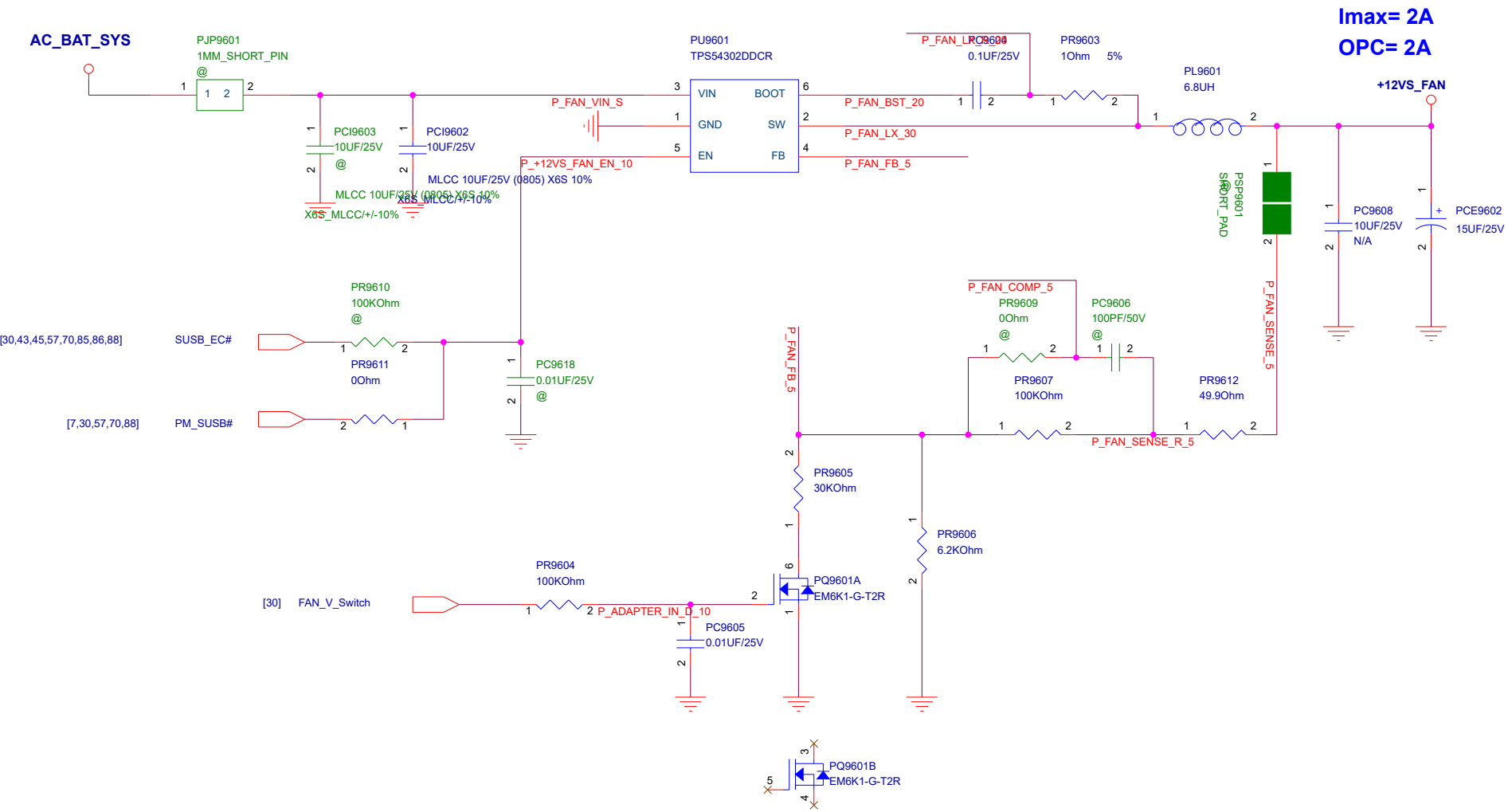
9. Card Reader: AU6435--02G630002400 (Page42)

10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)

+12VS_FAN [For FAN]



<Variant Name>

Project Name: Project Name		Rev: R1.0
Title : PW_+12VS_FAN		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Friday, November 06, 2020	Sheet 96 of 104	

1. P.01-30 reference FX505DY, P.31-104 reference GX502_(WW39_20180927C)
2. Net connection_(WW39_20180928A)
20181004
P.03
P.07
P.30 Copy FX505DY P.30
P.32 Modify Reset circuit
P.34 Modify LAN connector
P.35 Modify M-KEY IT8291E to IT8299E
P.36 修路
P.37 Modiffy Headphone, Mic, ESS
P.39 Remove Mute control
P.40 Modify circuit
P.41 Modify circuit & 修孔, 0 ohm short keep
P.45 Add Mic and HDR circuit
P.48 Keep SL4802
P.49 Modify circuit
P.50

ASUSTeK COMPUTER	Title : GM5GX0E_SKU Table_R1.0		
	Engineer: EE		
Size: C	Project Name: GX502GX		Rev: 1.0
Date: Friday, November 30, 2018	Sheet 103 of 104		

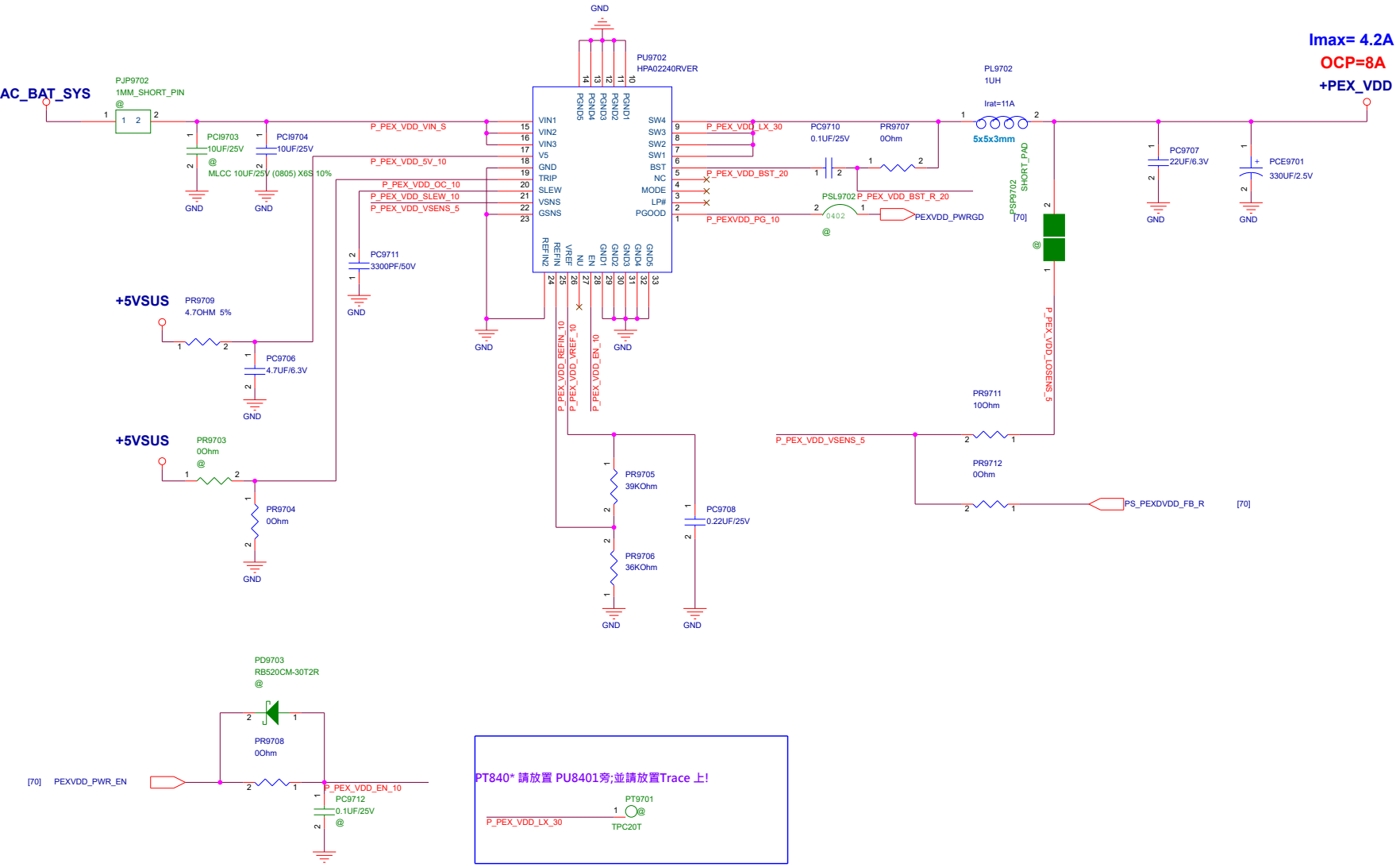
9. Card Reader: AU6435--02G630002400 (Page42)

10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

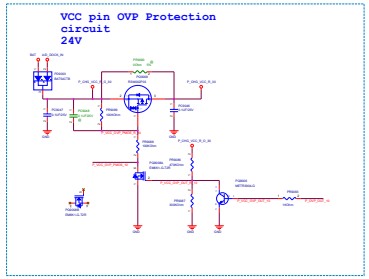
13. Audio Codec : 02043-00130000 (663-VA4)

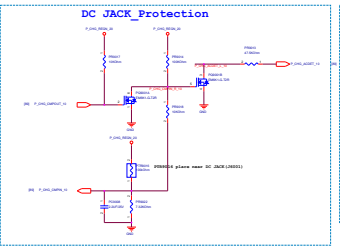
PEX_VDD [For GPU]

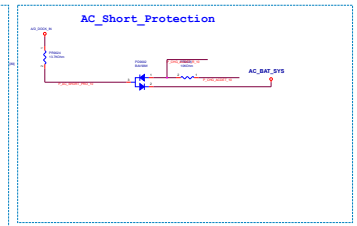


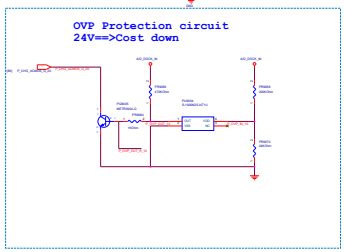
Project Name: **Project Name**		Rev: R1.0
Title : *****		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: Power RD	
Date: Friday, November 06, 2020	Sheet 97 of 103	

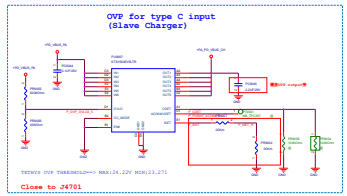
P90_PROTECTION

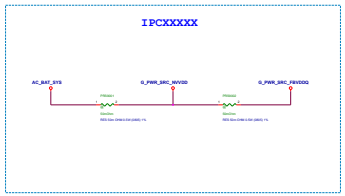










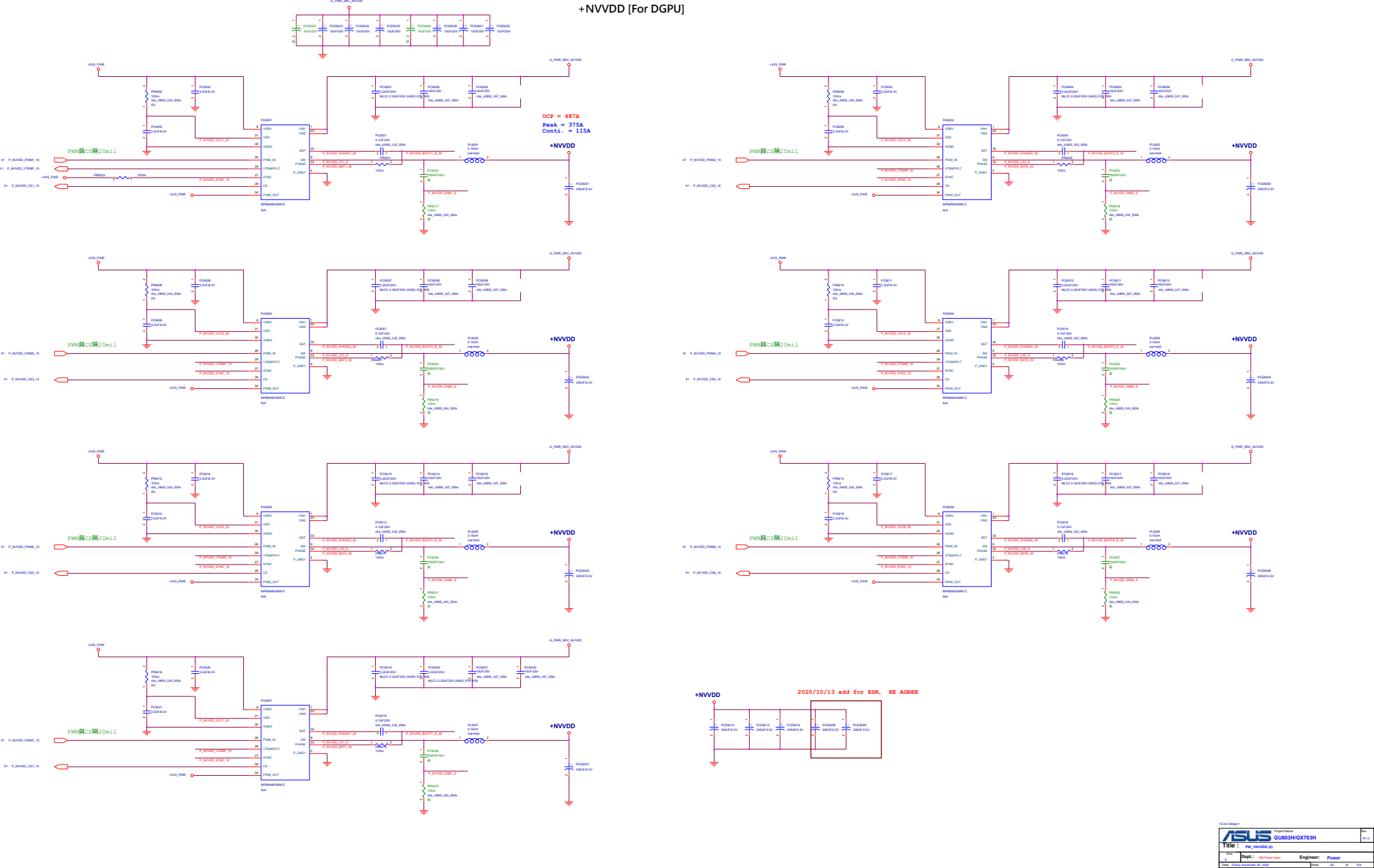


address	A6	A5	A4	A3	A2	A1	A0	R/W
8'h90	1	0	0	1	0	0	0	0
8'h91	1	0	0	1	0	0	0	1

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x38	x	x	x	x	x	x	x	x
function	PROG_CHARGE_CURRENT[7:0]							
default	0	0	0	0	0	0	0	0
0x39	x	x	x	x	x	x	x	x
function	PROG_CHARGE_VOLTAGE[7:0]							
default	0	0	0	0	0	0	0	0

Document Number: 90S21220906
Title: SW_P90_PROTECTION
Size: A3 | Date: 2021-Dec-Tue | Sheet: of | Engineer: 90S21220906

+NVVDD [For DGPU]

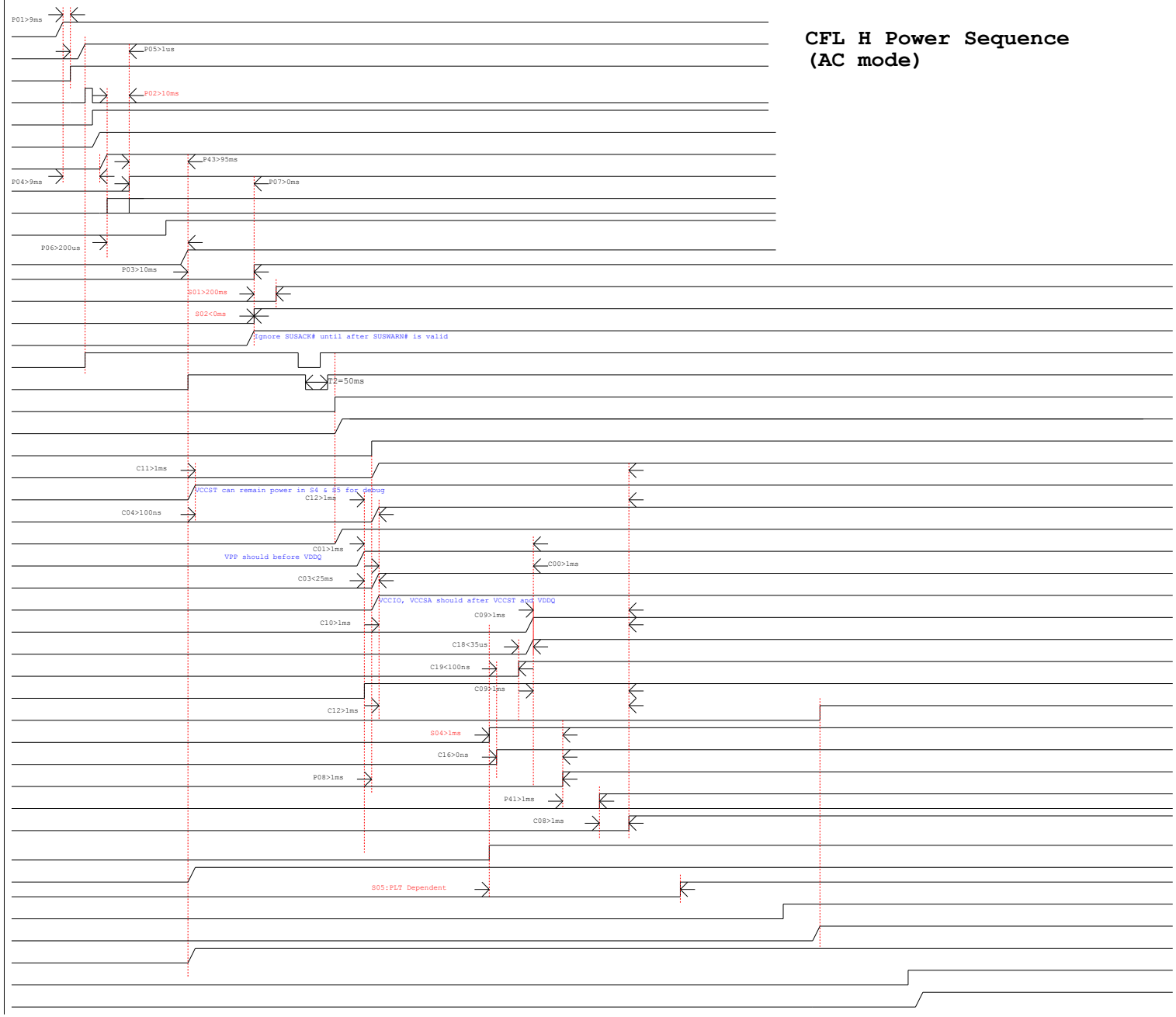


AC-IN Mode

CFL H Power Sequence (AC mode)

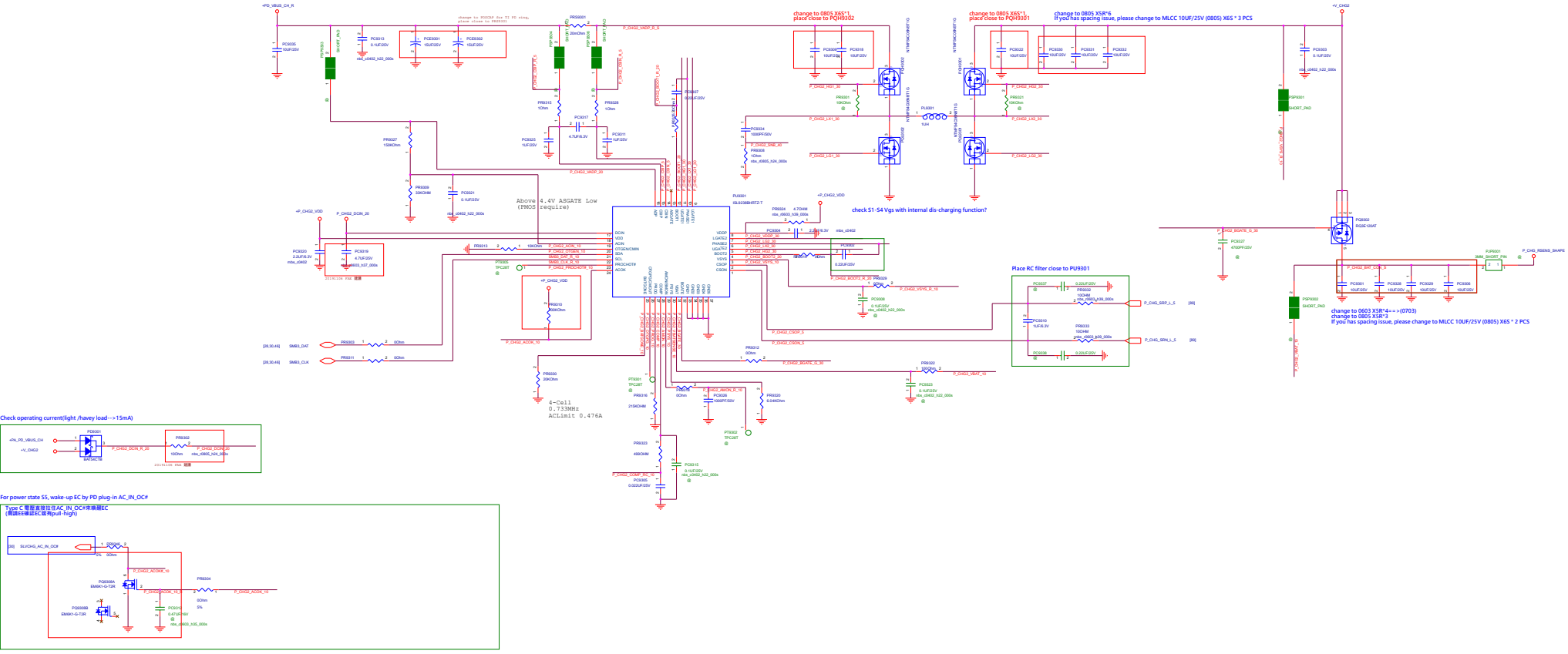
C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(SUSB_EC#) +1.0V_VCCST, VCCPLL
(SUSB_EC#) +VCCIO, (+12VS) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT

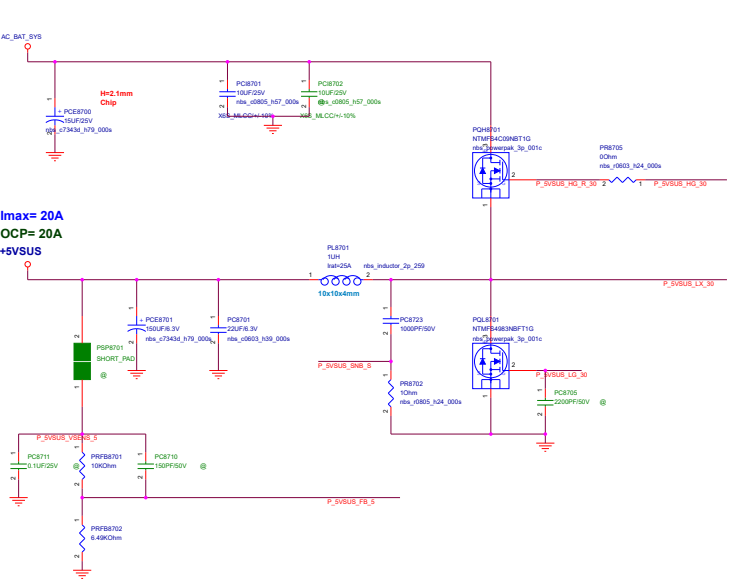


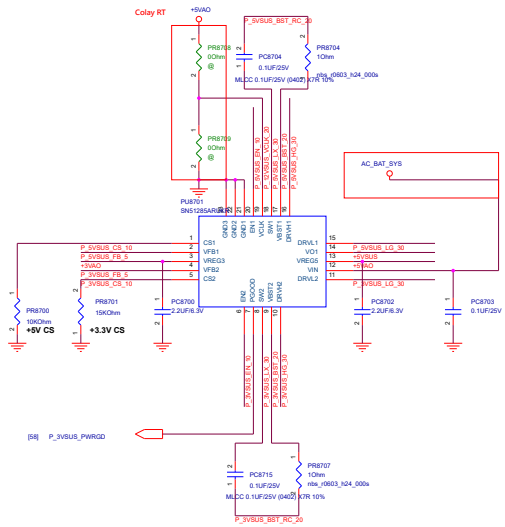
ASUS	Project Name: GX502GX		Rev: 1.0
Title : Power On Timing--AC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Friday, November 06, 2020	Sheet: 100 of 104		

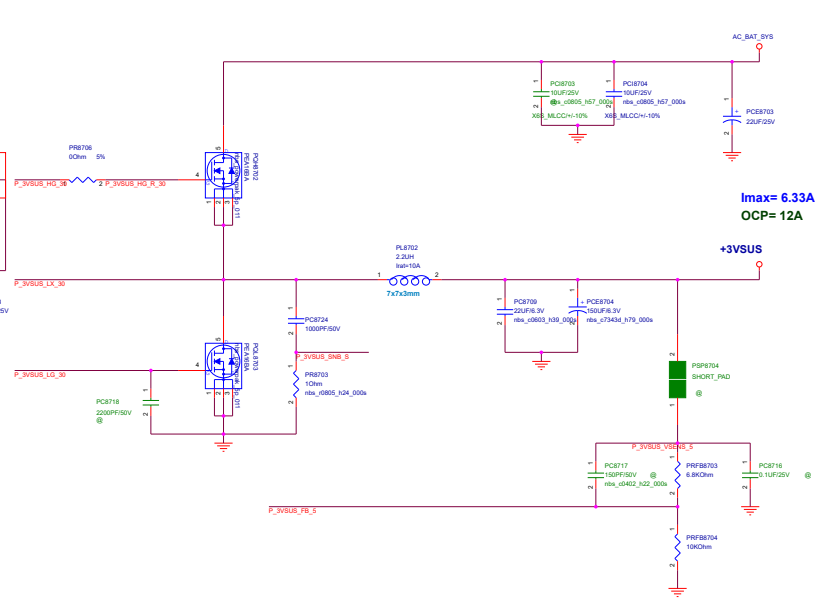
Charger ISL9238 (NVDC)

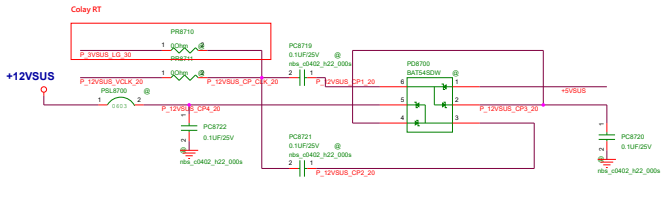


+3VA_DSW / +5VSUS [System Power]

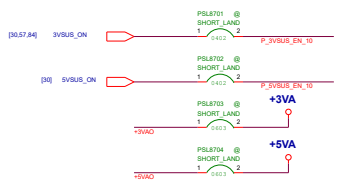








請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



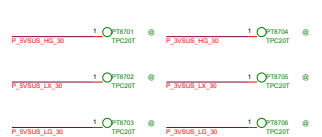
Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

PT870* 請放置 PU8700旁;並請放置Trace 上!



<Variant Name>

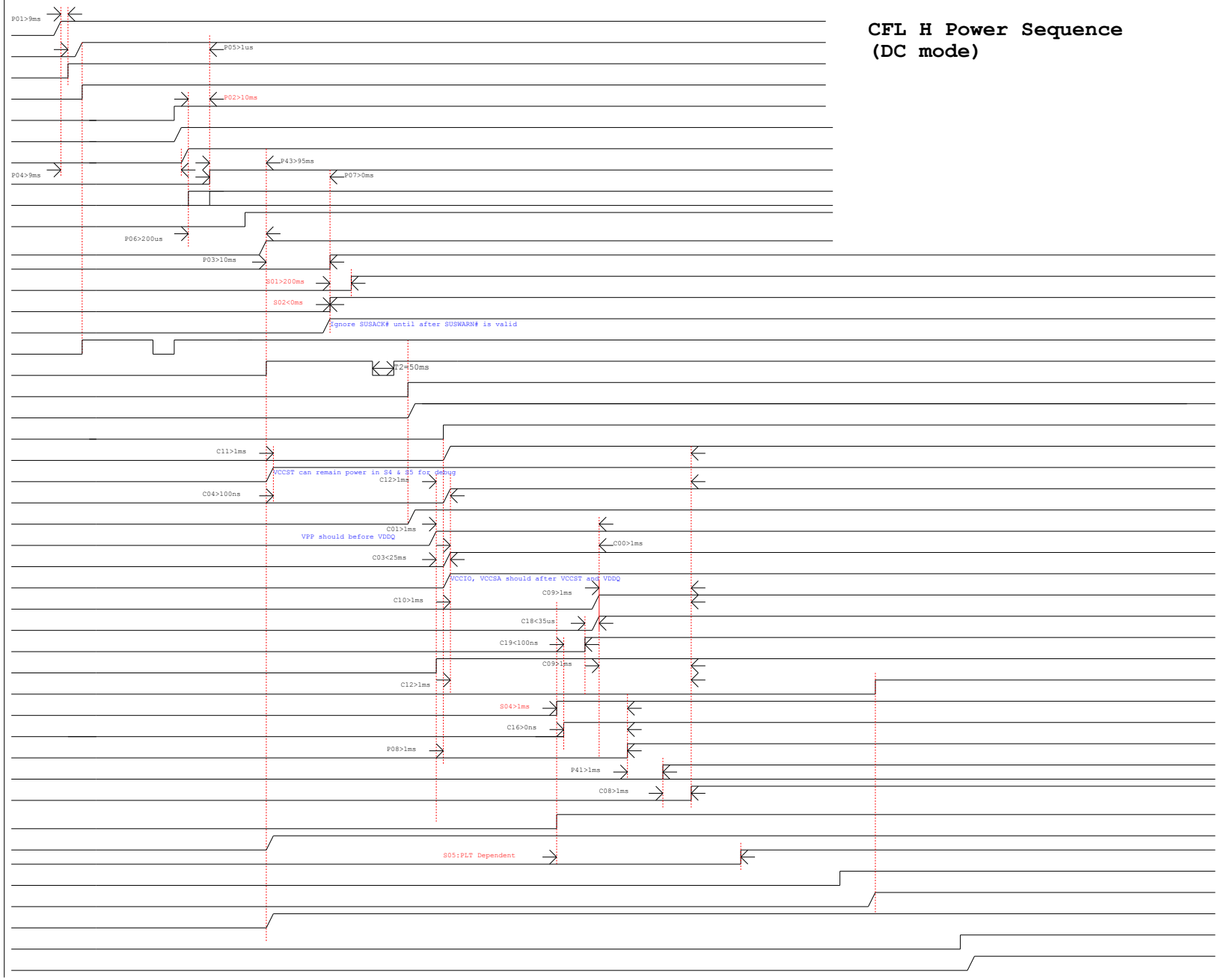
Project Name: Coffelake-H		Rev: R1.0
Title : PW_+3VSUS/+5VSUS		
Size: A2	Dept.: NB Power team	Engineer: Joe
Date: Friday, November 06, 2020	Sheet: 87	of 104

CFL H Power Sequence (DC mode)

DC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(VSUS_ON) +1.0V_VCCST,VCCPLL (VCCST_PWRGD)
(+VCCIO) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



ASUS	Project Name: GX502GX		Rev: 1.0
Title : Power On Timing-DC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: NB1 RD2 EE1	
Date: Friday, November 06, 2020	Sheet 101 of 104		

Rev	Date	Description
1.0	2017.03.03	P21 Remove CN
	2017.03.04	Q5602, Q5601 change for DXF Limitation
	2017.03.10	+1V9_MAIN, +3VS_NV Follow G753 Power sequence setting
	2017.03.11	R7821 Follow GL702 GPU Power seq
	2017.03.11	+PEX_VDD GPU Sequence update
	2017.03.14	PCE8104, PCE8107, PCE8106 update Cap for DXF Limit
	2017.03.14	GX501VIK Remove useless nut in P67
	2017.03.15	J5301 Connector list update
	2017.03.15	H6716, H6706, H6724, H6723 Screw Hole update
	2017.03.16	J5602 change LID SW for Angle Simulation
	2017.03.17	EMI Reserve C5606, C5607 Cap
	2017.03.17	RM3002, L4512, L4513, L4504, L4515, L4505 SWAP for Layout
1.1	2017.03.21	P30, P37, P39 AMP Change SNL04M25555
	2017.03.21	EMI Reserve P30 C77360 Cap and P69 Caps and Spring
	2017.03.23	AMP Change Remove P37 MUTE CONTROL schematic
	2017.03.23	AMP Change Reserve Q3701
	2017.03.27	P71 +PBVDDQ Discharge setting Follow G753 Power sequence setting
	2017.03.29	P12 Remove TBT Power Low Switch for Layout
1.2	2017.03.30	Change Cap C7105, C7101 for thermal request
	2017.03.30	Thermal Request for H6728
	2017.04.05	EMI Reserve Cap and Spring in P69
	2017.04.06	Reserve C2601 for +VCCPGPP_EF Ripple
	2017.04.07	25.00MHZ Cap C1126, C1124 change for Vendor Suggest
	2017.04.07	27MHz Cap C7811, C7801 change for Vendor Suggest
2.0	2017.04.11	P48 Reserve 0 ohm for SDA and SCL
	2017.04.17	P71 Add Caps for NVVDD Ripple
	2017.04.18	Q5704 Chnage MOS for DXF Limitation
	2017.04.20	P71 Add Caps for NVVDD Ripple
	2017.04.21	P67 Screw Hole H6705 update
	2017.04.21	P71 Add Caps for NVVDD Ripple C71119~C71122
	2017.04.25	P71 C7122, C7123, C7127, C7135, C7143, C7144, C7156, C7164, C7166,, C7186, C7187 change to 10UF
	2017.04.25	P70 C7007, C7002 change to 4.7UF
	2017.04.25	P70 C7020, C7024 change to 22UF
	2017.05.02	EMI Reserve C6948, C6949, C6950, C6951, C6952, C6953, C6954 and remove U6913
	2017.05.02	H6711, H6712 change screw hole type fot EMI Solution
	2017.05.03	Remove J4502 Pin 36 GND fot Factory Issue
	2017.05.05	P88, P58 Remove VCCST_PWRGD signal
	2017.05.05	P79, P45 Remove eDP Lan2 and Lan3 Signal
	2017.08.10	P31 R3121,R3122 change to unmount

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

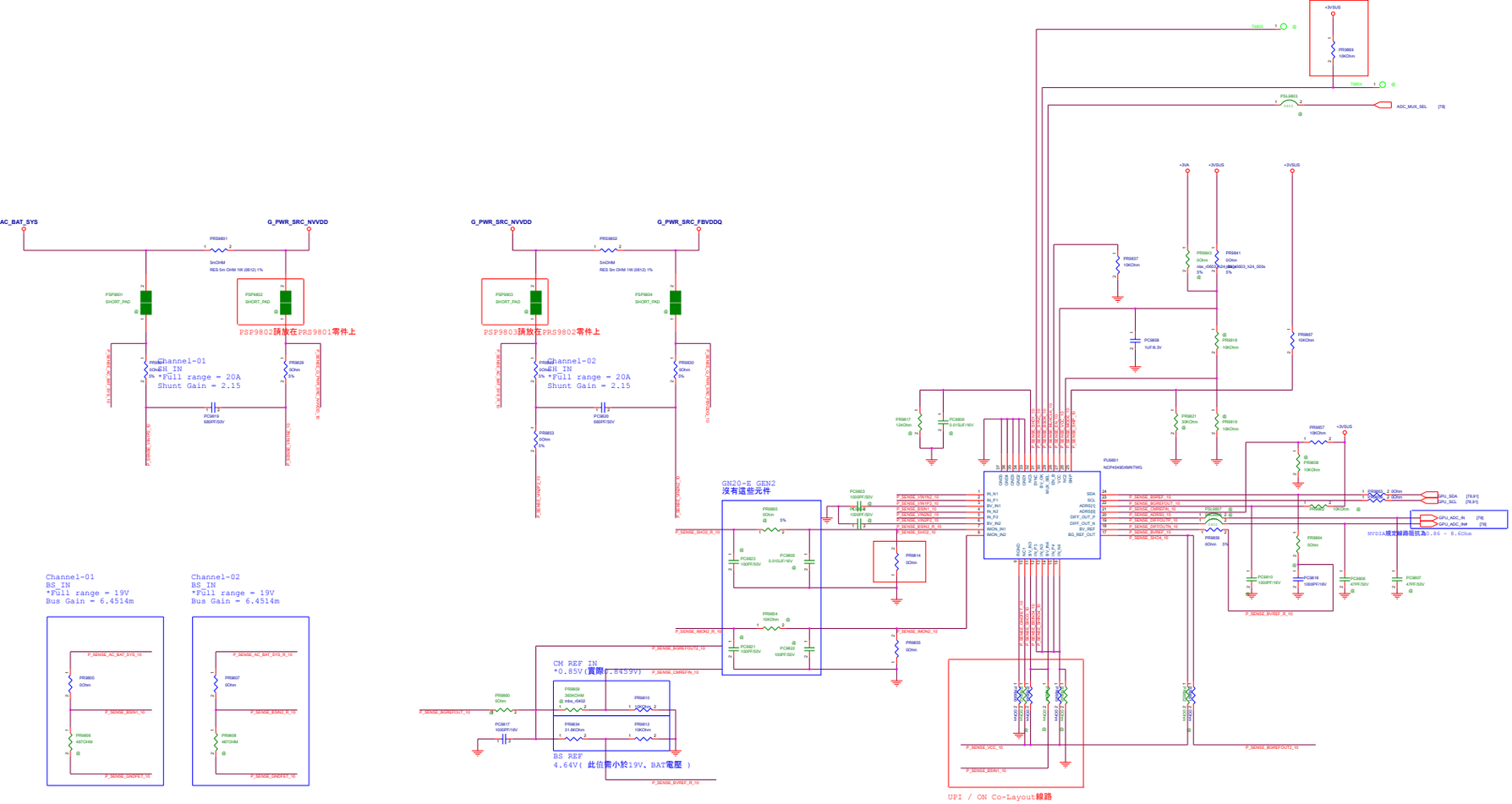
ASUSTeK COMPUTER

Title : Revision History

Engineer: EE

Size: D | Project Name: GX502GX | Rev: 1.0

Date: Friday, November 06, 2020 | Sheet 102 of 106

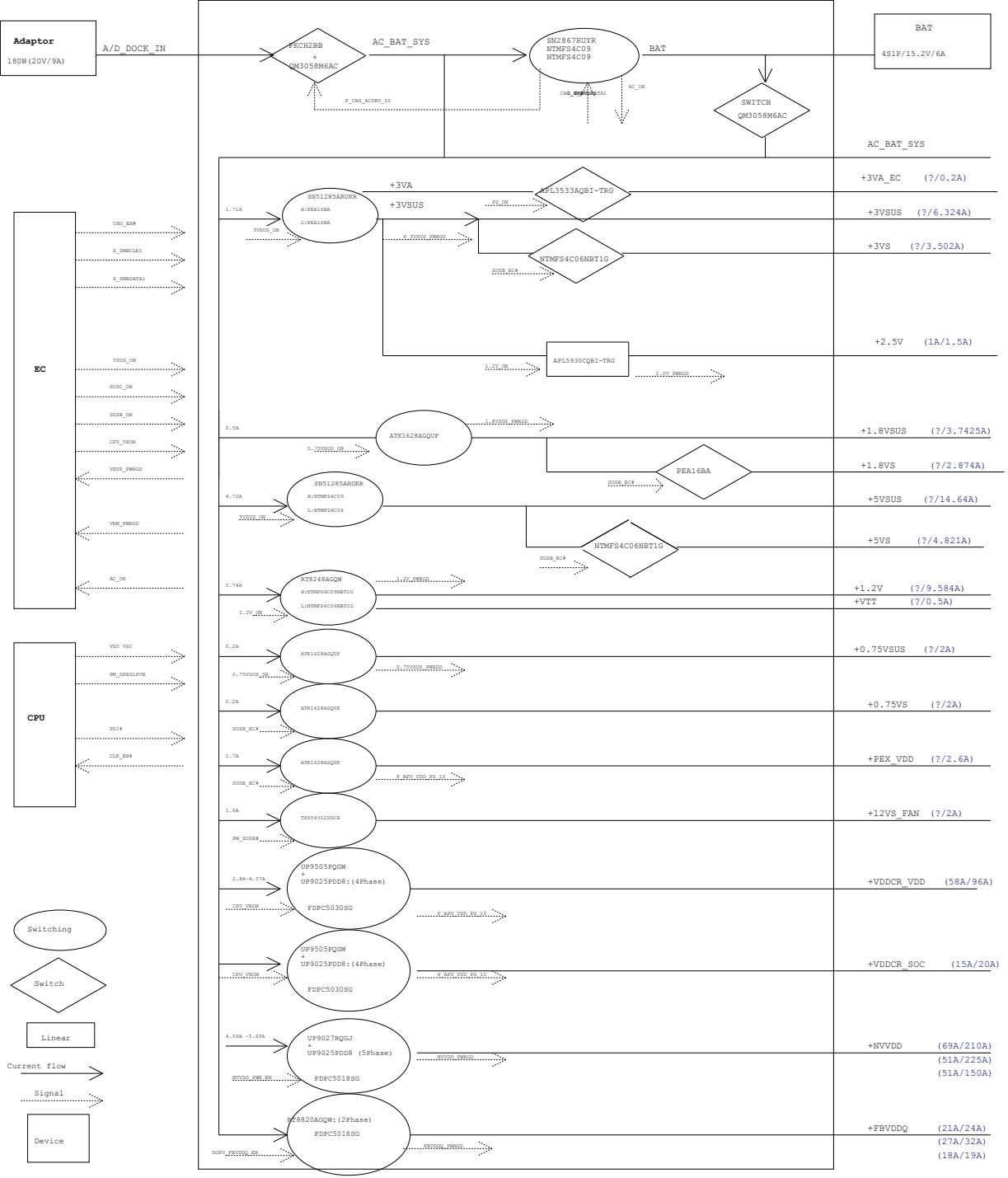


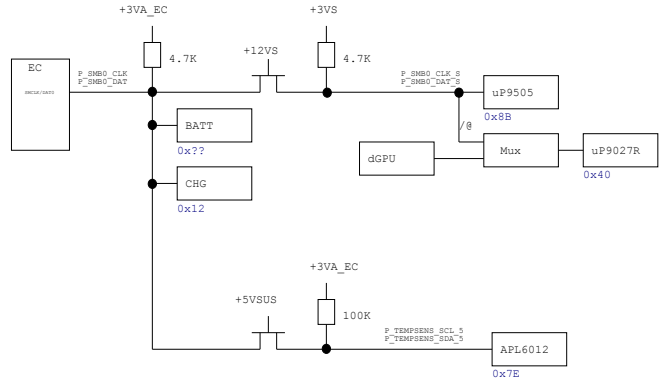
	PU9801	PR9805	PR9807	PC9803	PC9804	PC9805	PR9814	PR9855	PR9822
GN20	NCP45495XMNTWG 06129-00220000	0 Ohm 10G212000004030	0 Ohm 10G212000004030	@	@	@	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0 Ohm 10G212000004030
N18P-G1	UP9026QQKI 06129-00110100	75KOhm 10G212750214010	75KOhm 10G212750214010	1000PF/50V 11G232110214321	1000PF/50V 11G232110214321	0.015UF/16V 11G232115311360	357Ohm 10G212357014010	@	49.9Ohm 10G21249R914010

	PC9810	PR9860	PR9809	PR9810	PR9834	PR9863	PR9859	PC9809	PR9808
GN20	@	@	@	10KOhm 10G212100214010	31.6KOhm 10G212316214010	0 Ohm 10G212000004030	0 Ohm 10G212000004030	@	@
N18P-G1	1000PF/16V 11G232110211030	0 Ohm 10G212000004030	360KOhm 10G212364004010	680KOhm 10G212680314010	324KOhm 10G212324314010	@	@	0.015UF/16V 11G232115311360	487Ohm 10G212487014010

	PR9806	PR9861	PR9864	PR9857	PR9801	PR9853	PR9817	PR9844/PR9845	PR9846/PR9847
GN20	@	0 Ohm 10G212000004030	@	10KOhm 10G212100214010	0 Ohm 10G212000004030	0 Ohm 10G212000004030	@	0 Ohm 10G212000004030	@
N18P-G1	487Ohm 10G212487014010	@	0Ohm 10G212000004030	@	100hm 10G212100014010	49.9Ohm 10G21249R914010	357Ohm 10G212357014010	@	0 Ohm 10G212000004030

	PR9866	PR9818/PR9819	PR9821
GN20	0 Ohm 10G212000004030	@	@
N18P-G1	@	10KOhm 10G212100214030	30KOhm 10G212300214010





<Variant Name>
ASUS Project Name GA502IV Rev R1.0
Title : PW_FLOWCHART
Size Custom Dept.: NB Power team Engineer: CS Lin
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