Lenovo C340/C440 A01 (SIT) GPU Schematic

XTAl LIST

	PARTS	DIP/SMT	Frequence	PPM	CL
1	X1	SMT	25MHz	±20	10pF/10pF
2	X2	SMT	32.768KHz	±20	7pF/7pF
3	X5	SMT	27MHz	±30	12pF/12pF
4	X6	SMT	14.318MHz	±20	18pF/18pF
5	X7	SMT	24MHz	±20	12pF

SATA LIST

PORT	NET NAME	FUNCTION
SATA_TX0P/N	SATA_TX0P/N	SATA HDD
SATA_RX0P/N	SATA_RX0P/N	
SATA_TX1P/N	SATA_TX1P/N	SATA ODD
SATA_RX1P/N	SATA_RX1P/N	

USB LIST

PORT	NET NAME	FUNCTION
USB PORT 0	USB0P/N	SIDE IO
USB PORT 1	USB1P/N	SIDE IO
USB PORT 2	USB2P/N	REAR IO
USB PORT 3	USB3P/N	REAR IO
USB PORT 4	USB4_WLAN_P/N	WLAN CARD
USB PORT 5	USB5_WEBCAM_P/N	WEBCAM
USB PORT 8	USB8_TV_P/N	TV CARD
USB PORT 11	USB11_TSCREEN_P/N	TOUCH SCREEN

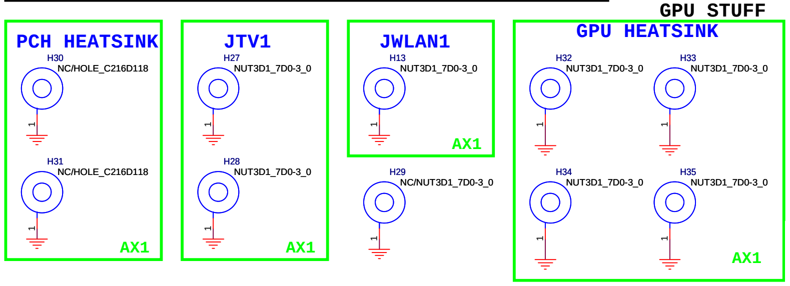
PCI-E LIST

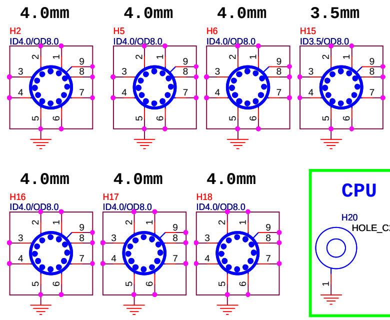
PORT	NET NAME	FUNCTION
2	PCIE_USB3_TXP/N	USB3.0
2	PCIE_USB3_RXP/N	
3	PCIE_LAN_TXP/N	GIGA LAN
3	PCIE_LAN_RXP/N	
4	PCIE_CR_TXP/N	CARD READER
4	PCIE_CR_RXP/N	
5	PCIE_TV_TXP/N	TV CARD
5	PCIE_TV_RXP/N	
6	PCIE_WLAN_TXP/N	WLAN CARD
6	PCIE_WLAN_RXP/N	

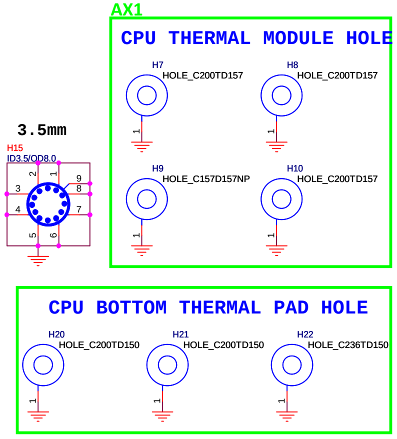
POWER STATES

SIGNAL \ STATE	VOTAGE	S0	S3	S5	G3
PCH_SLP_S3#	-	HIGH	LOW	LOW	LOW
PCH_SLP_S5#	-	HIGH	HIGH	LOW	LOW
S5_PWR_ON	-	HIGH	HIGH	HIGH	LOW
+VBAT_IN	+3.3V	O	O	O	O
+VIN (DC IN)	+19V	O	O	O	X
+3V_LDO/+5V_LDO	+3.3V/+5V	O	O	O	X
+3V_S5 (S5)	+3.3V	O	O	O	X
+5V_S5 (S5)	+5V	O	O	O	X
+5V_S3 (S3)	+5V	O	O	X	X
+3V_S3 (S3)	+3.3V	O	O	X	X
+1.1V_S3 (S3)	+1.1V	O	O	X	X
+1.5V_S3 (S3)	+1.5V	O	O	X	X
+MEM_VTT (S0)	+0.75V	O	X	X	X
+3V_S0/+5V_S0 (S0)	+3.3V/+5V	O	X	X	X
+12V_S0 (S0)	+12V	O	X	X	X
+1.8V_S0 (S0)	+1.8V	O	X	X	X
+1.5V_S0 (S0)	+1.5V	O	X	X	X
+1.05V_S0 (S0)	+1.05V	O	X	X	X
+CPU_VCCIO (S0)	+1.0V	O	X	X	X
+0.85V_S0 (S0)	+0.85V	O	X	X	X
+CPU_AXG (S0)	SVC/SVD	O	X	X	X
+CPU_VCC (S0)	SVC/SVD	O	X	X	X

BOM OPTION
GPU STUFF







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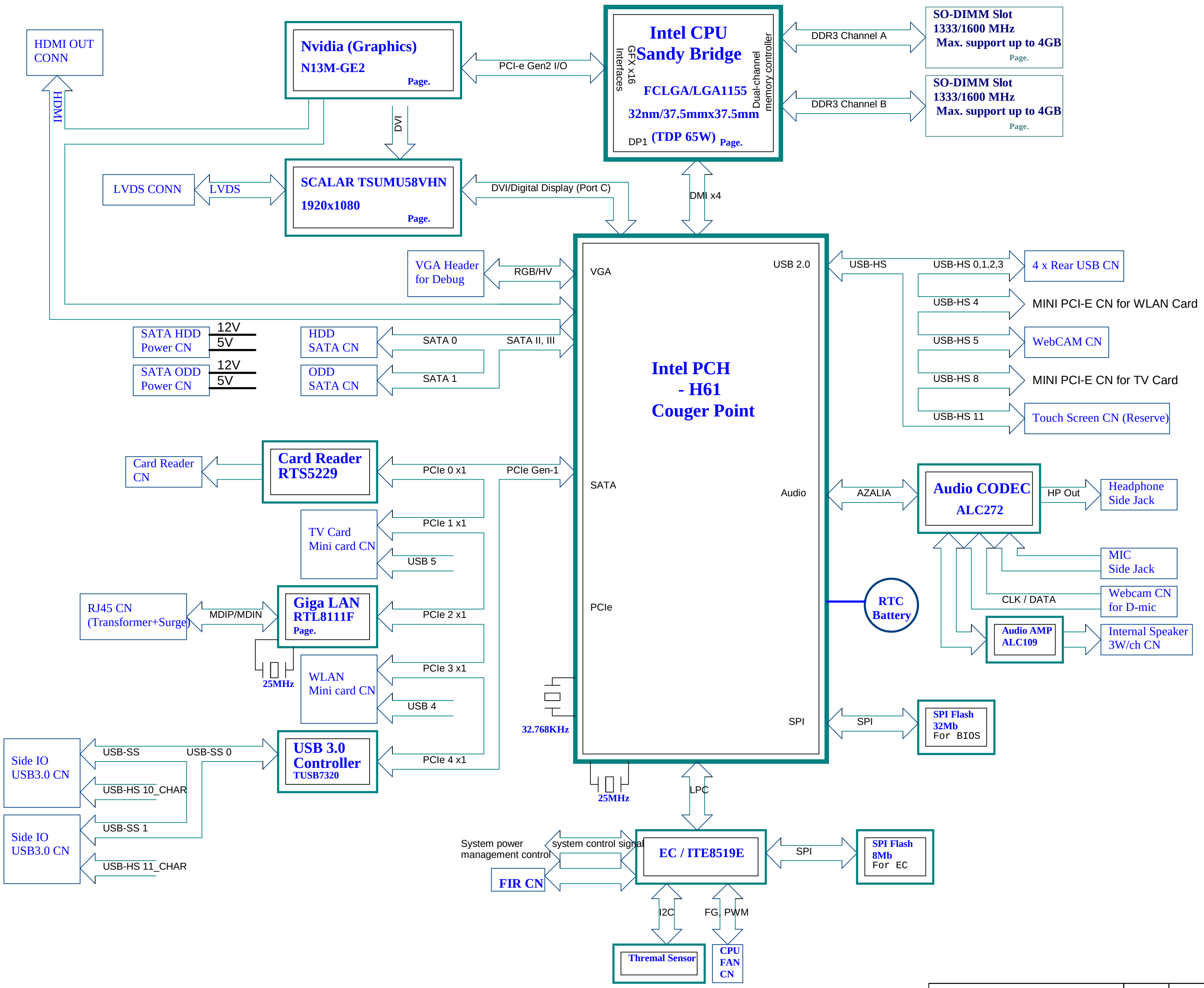
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Wednesday, April 25, 2012	Sheet	1 of 45		

C340/C440 SYSTEM BLOCK DIAGRAM



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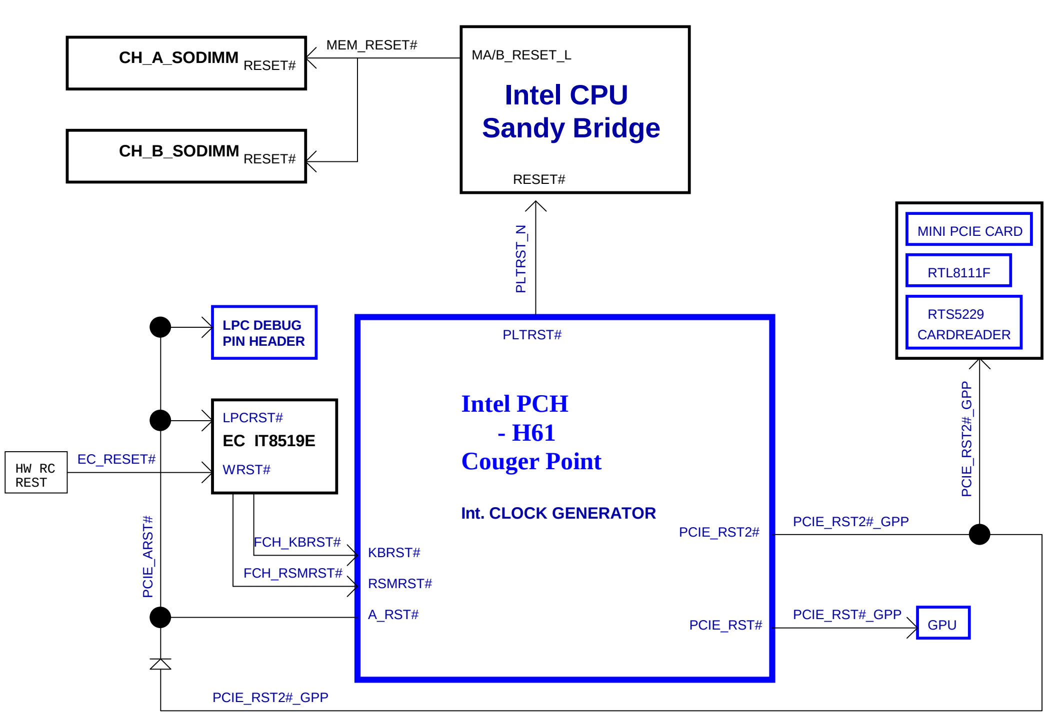
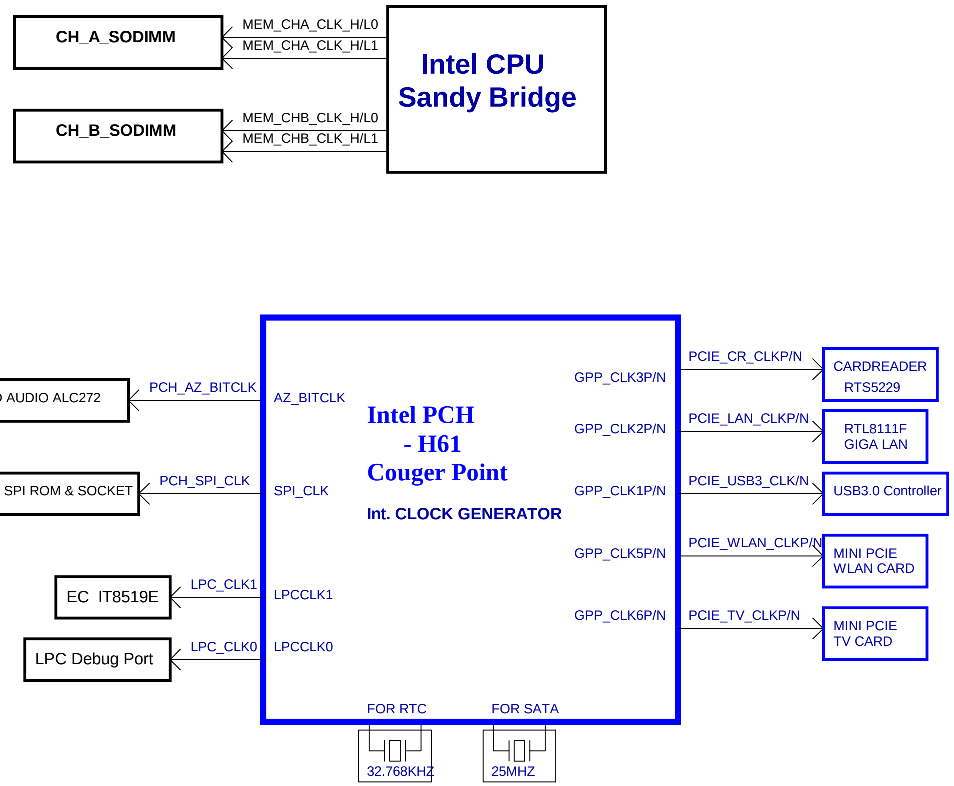
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	2 of 45		

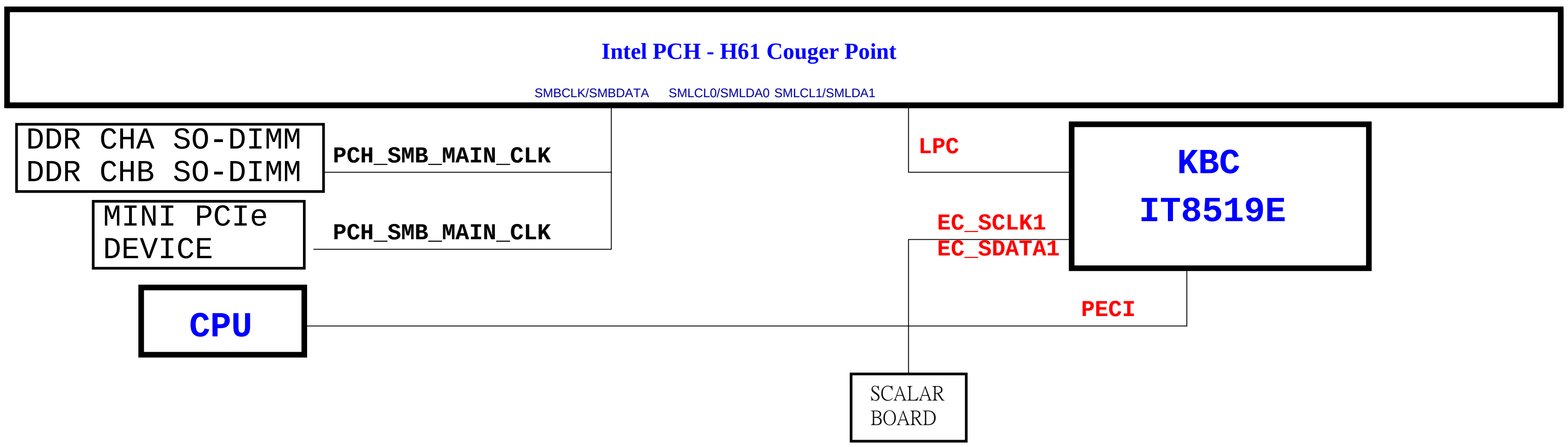
RESET Block Diagram



INTERNAL CLOCK MODE



SM Bus MAP



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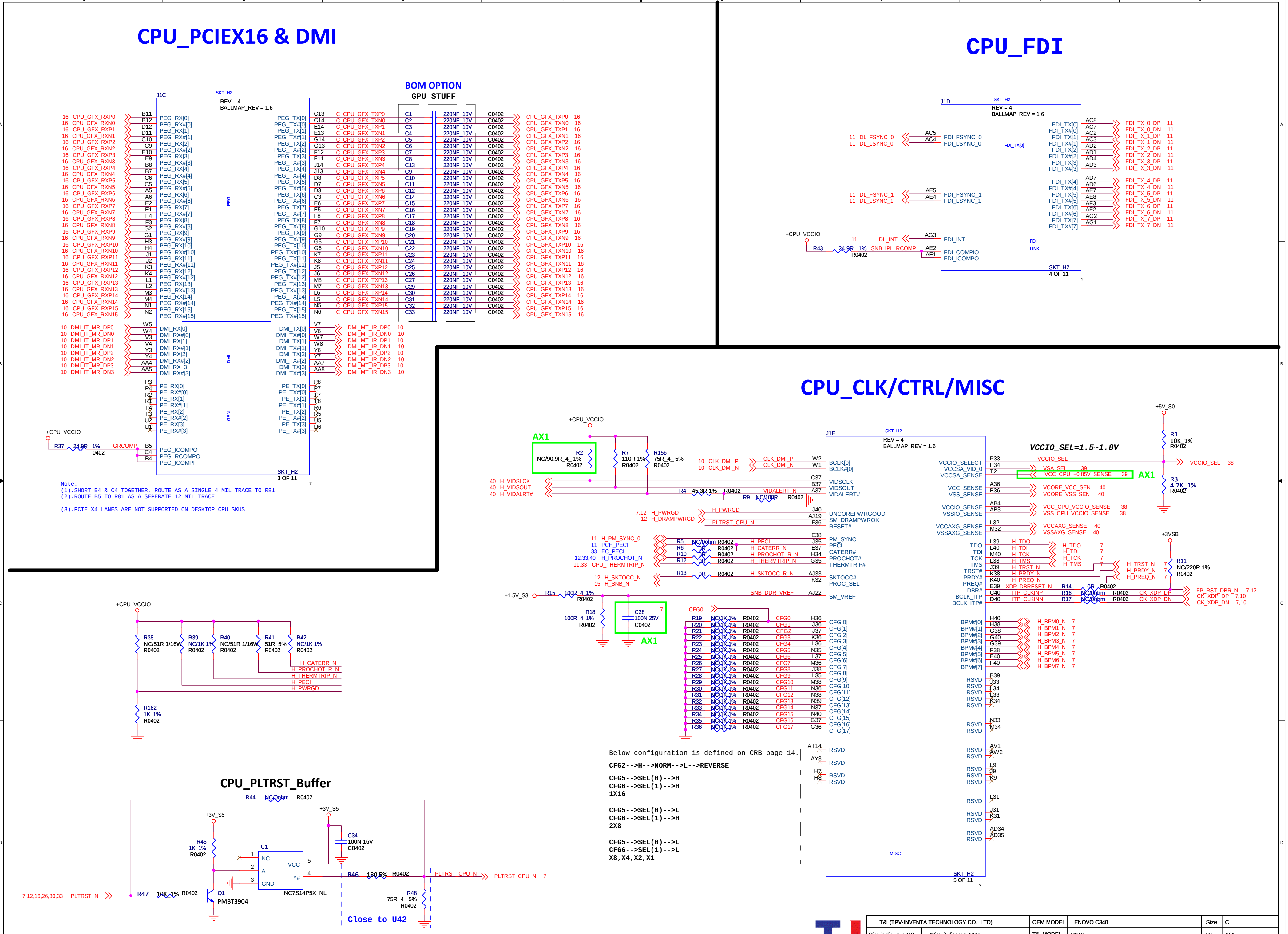
Date	Monday, April 23, 2012	Sheet	3 of 45		



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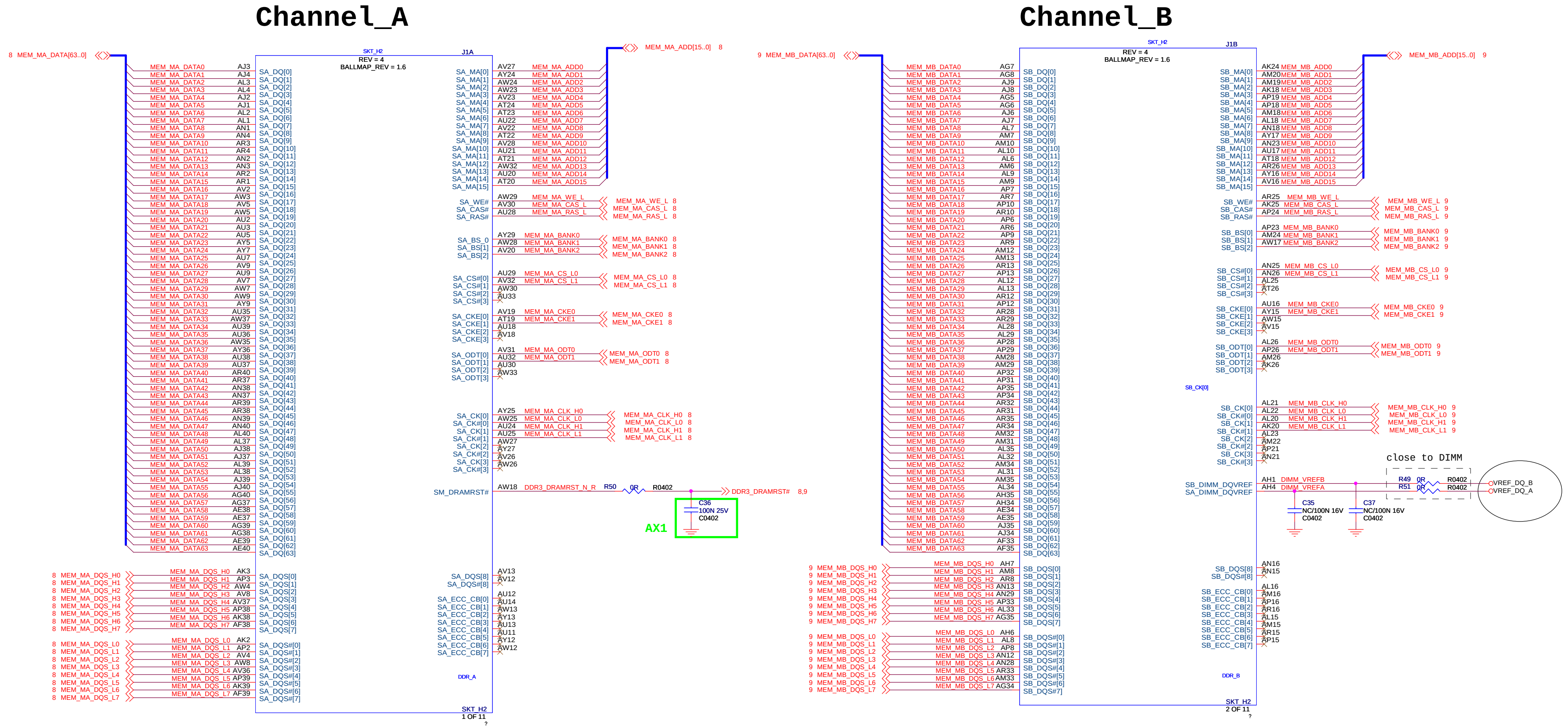
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	4 of 45		

CPU_DDR



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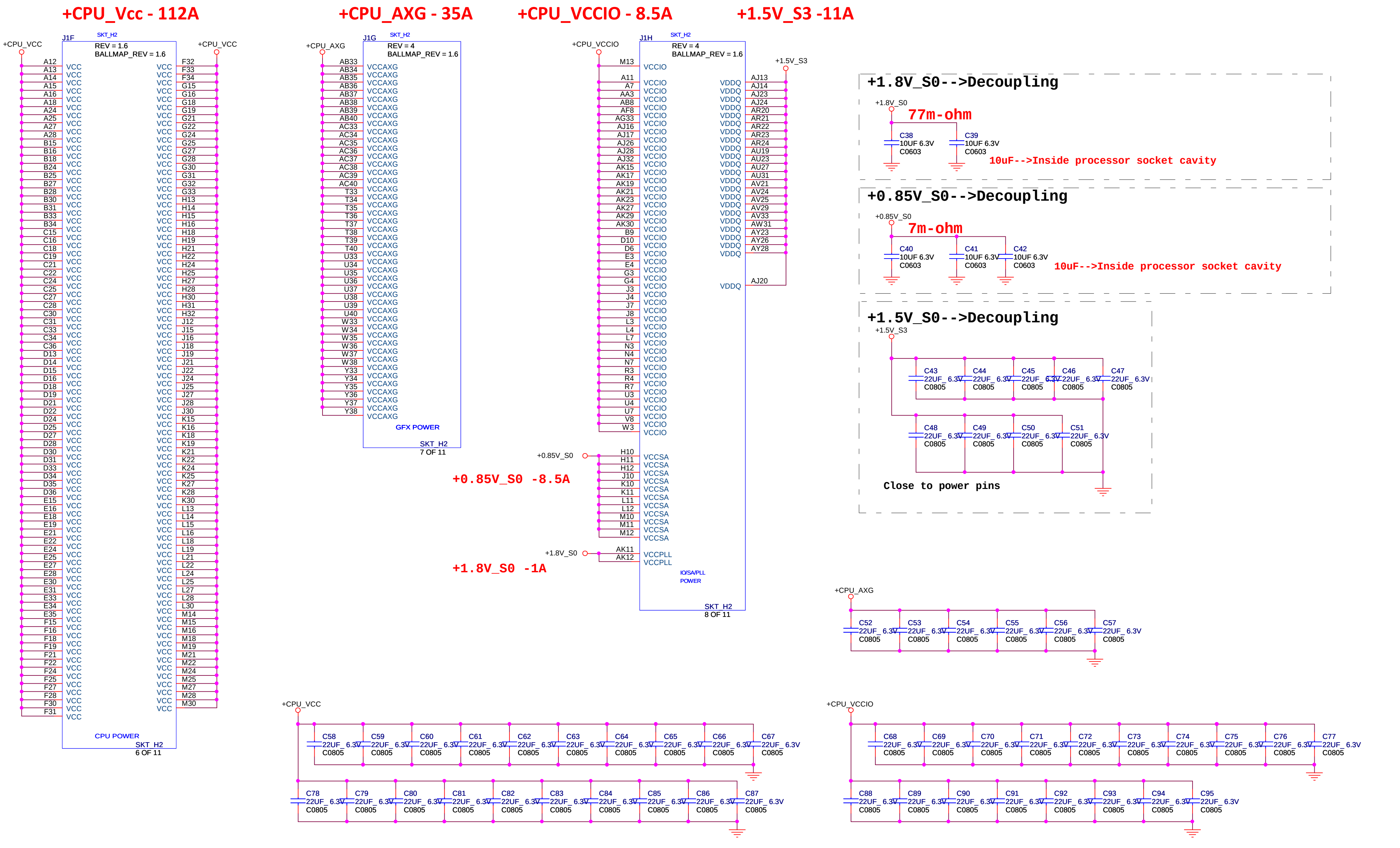
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	5 of 45		

CPU_POWER



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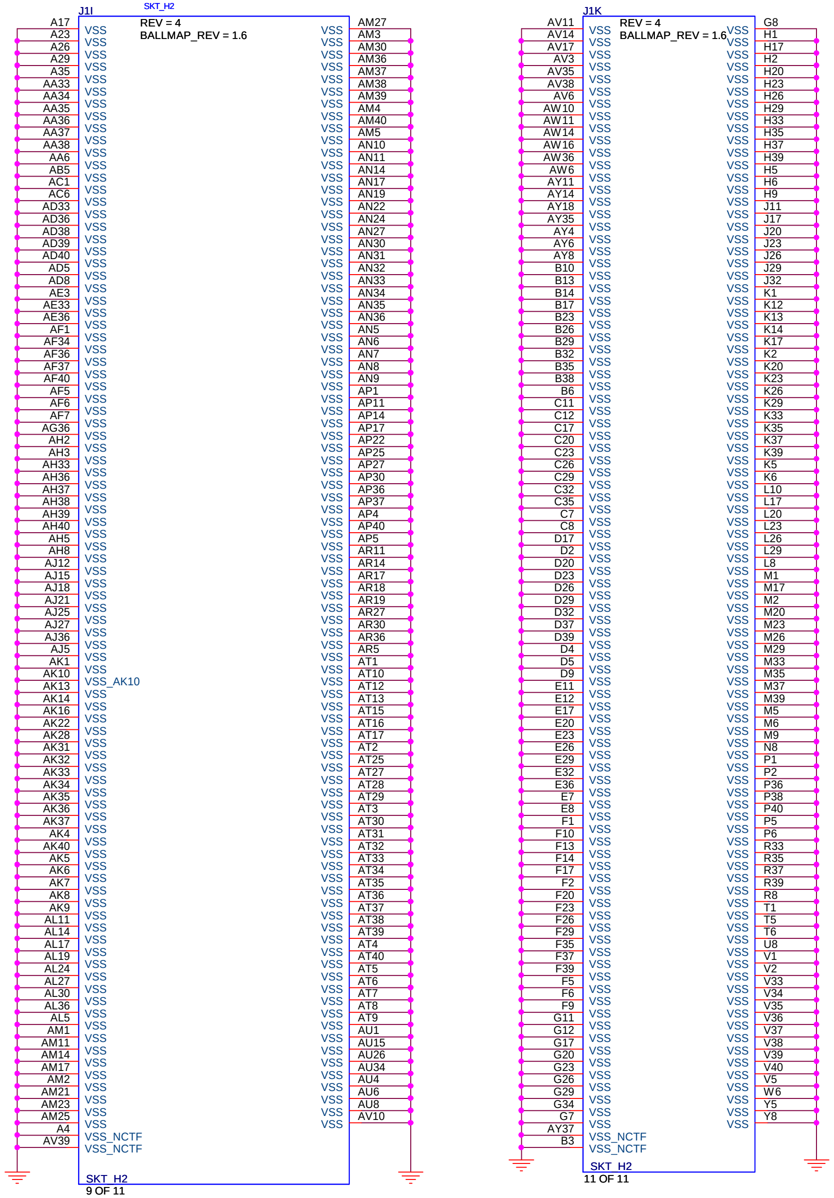
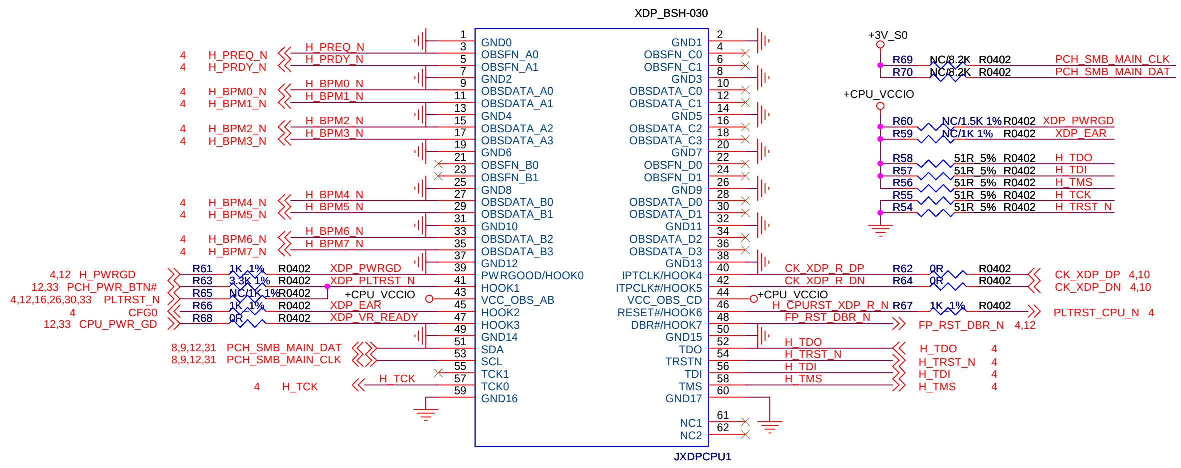
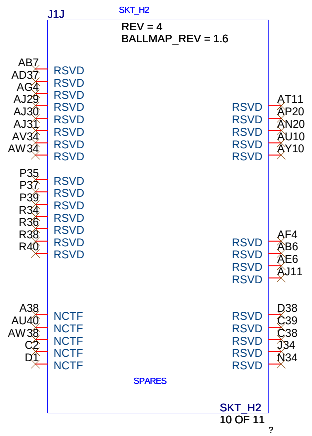
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	6 of 45		

CPU_GND



CPU_XDP CONNECTOR





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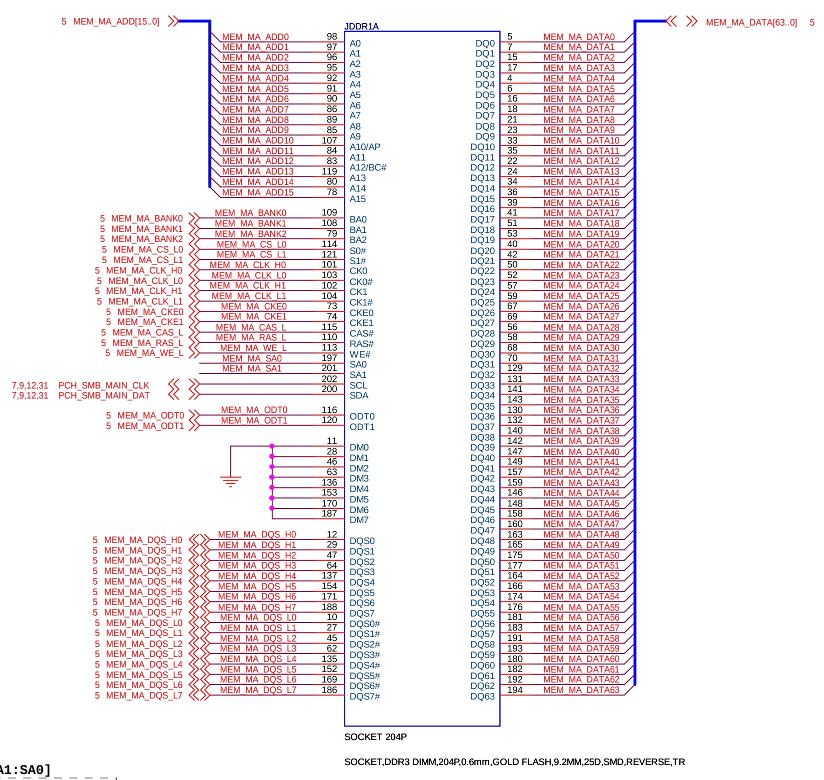
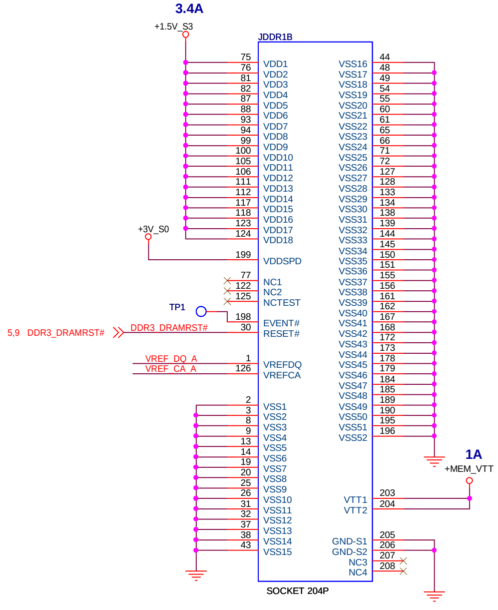
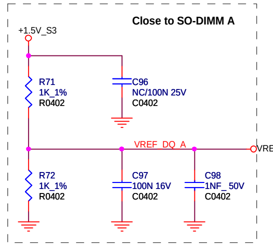
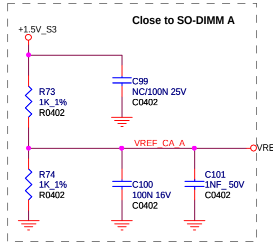
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	7 of 45		

CHA DDR 9.2H(DIMM-1)

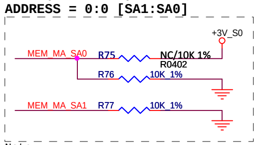






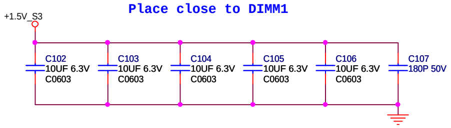


DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

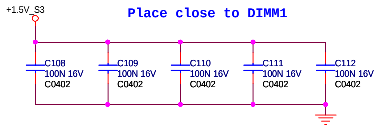


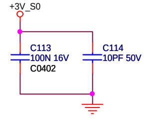
Note:
If SA0 = 0, SA1 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0= 1, SA1 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

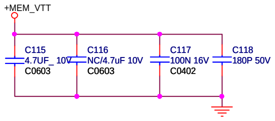
Place close to DIMM1



Place close to DIMM1







T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
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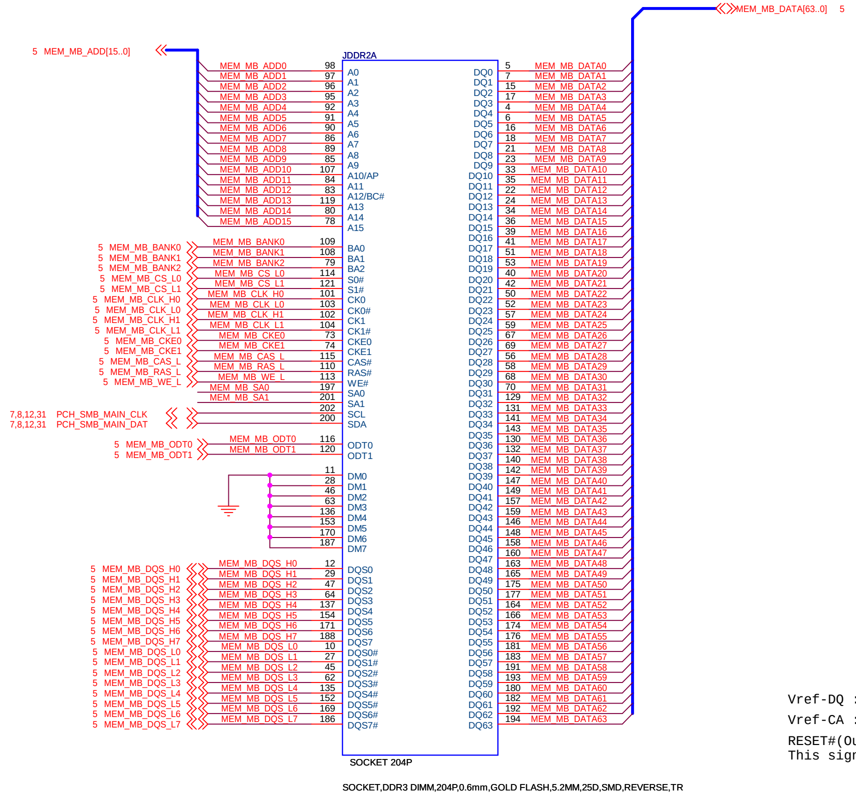
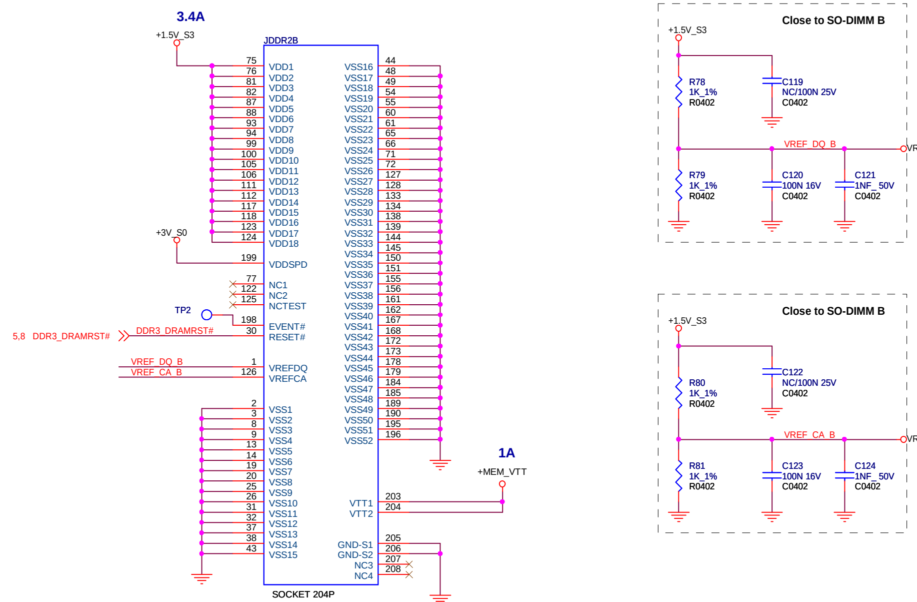
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	8 of 45		

CHB DDR 5.2H(DIMM-2)

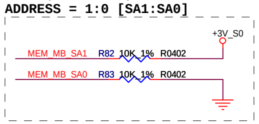


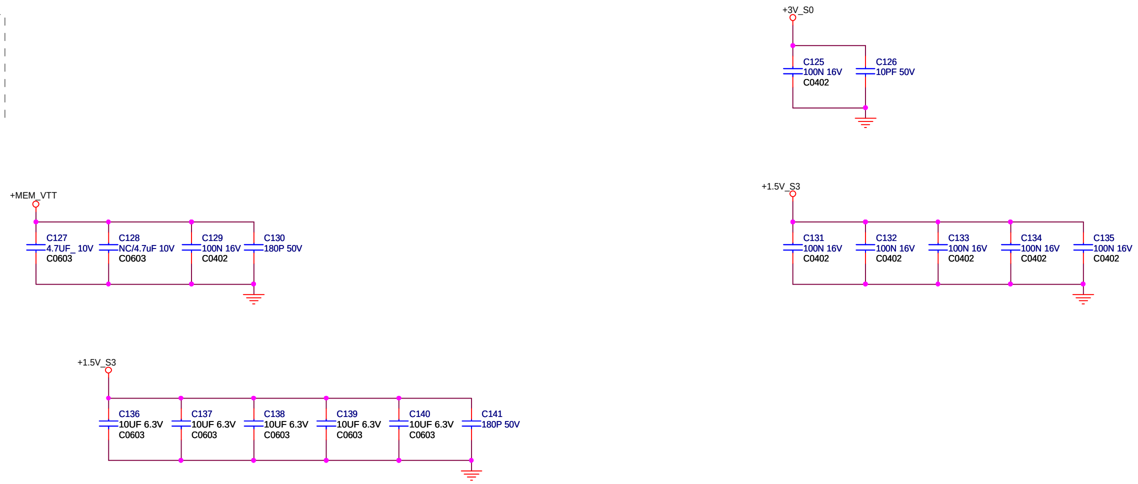
SOCKET,DDR3 DIMM,204P,0.6mm,GOLD FLASH,5.2MM,25D,SMD,REVERSE,TR




```
Vref-DQ : Reference voltage for DQ0–DQ63, CB0–CB7 and PAR_IN. When in single ended mode used for DQS0–DQS7.
Vref-CA : Reference voltage for A0-A15, BA0–BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.
RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW.
This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.
```

DIMM2(CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]





T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
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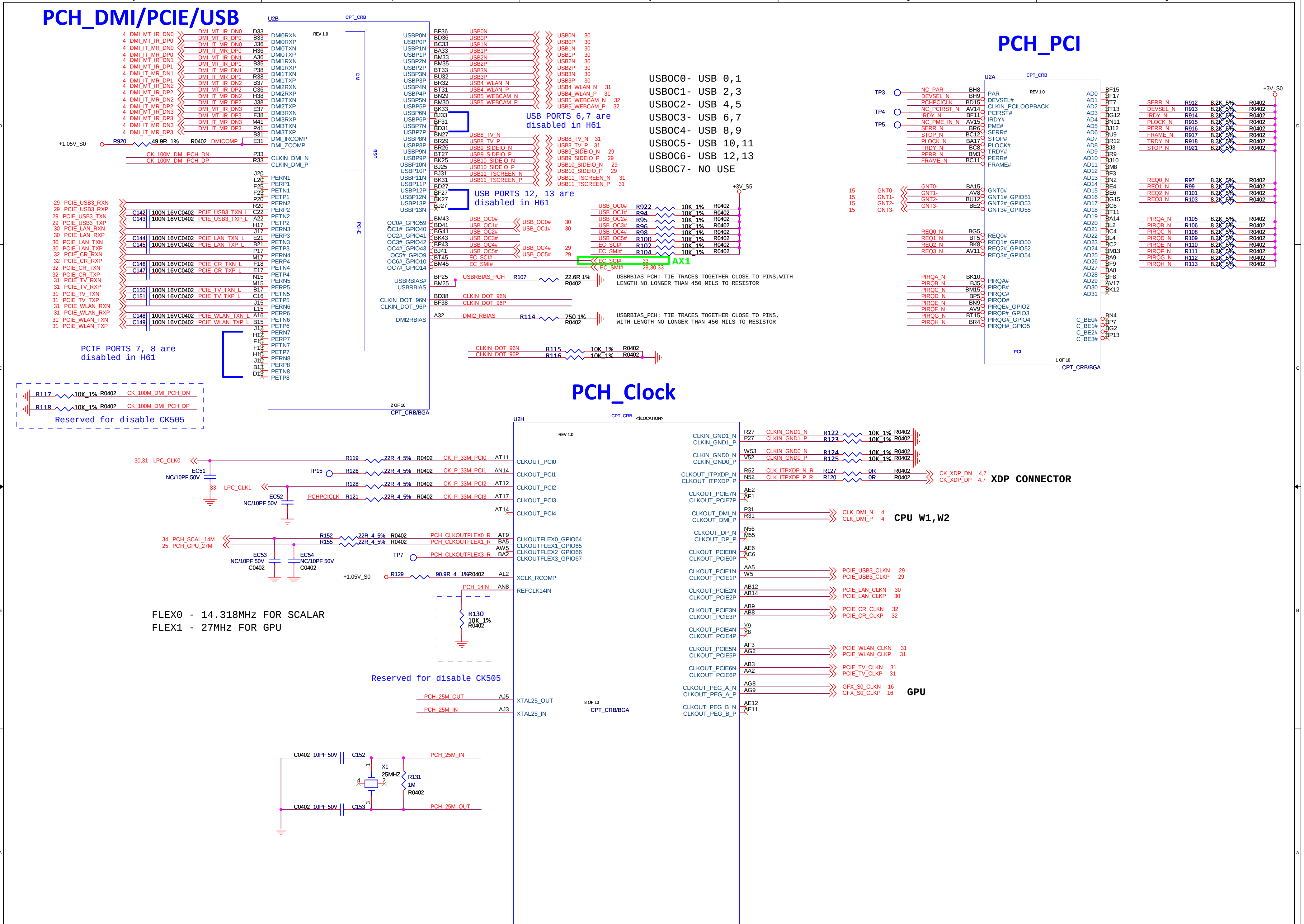
Date	Monday, April 23, 2012	Sheet	9 of 45		



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
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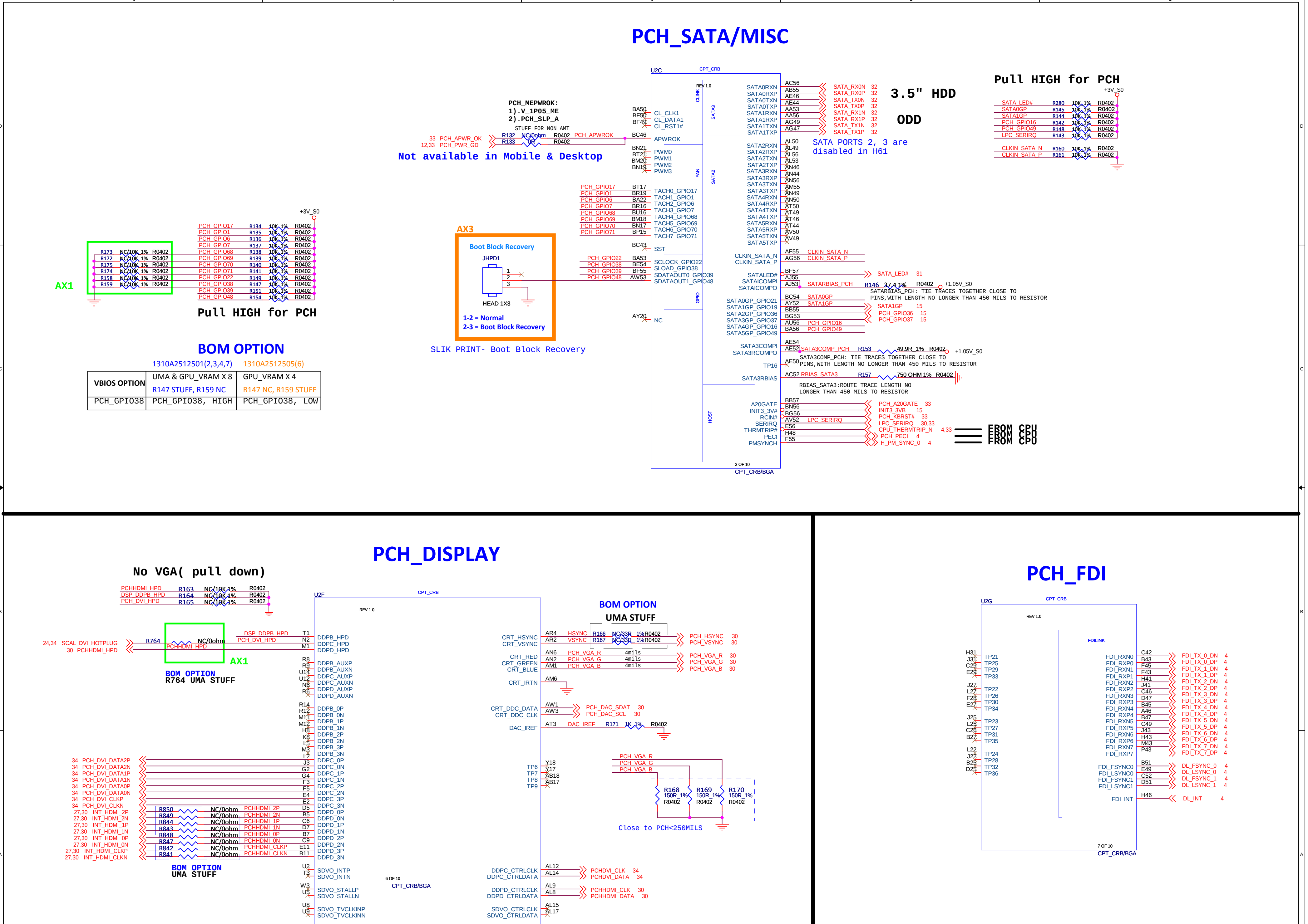
Date	Monday, April 23, 2012	Sheet	10 of 45		



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
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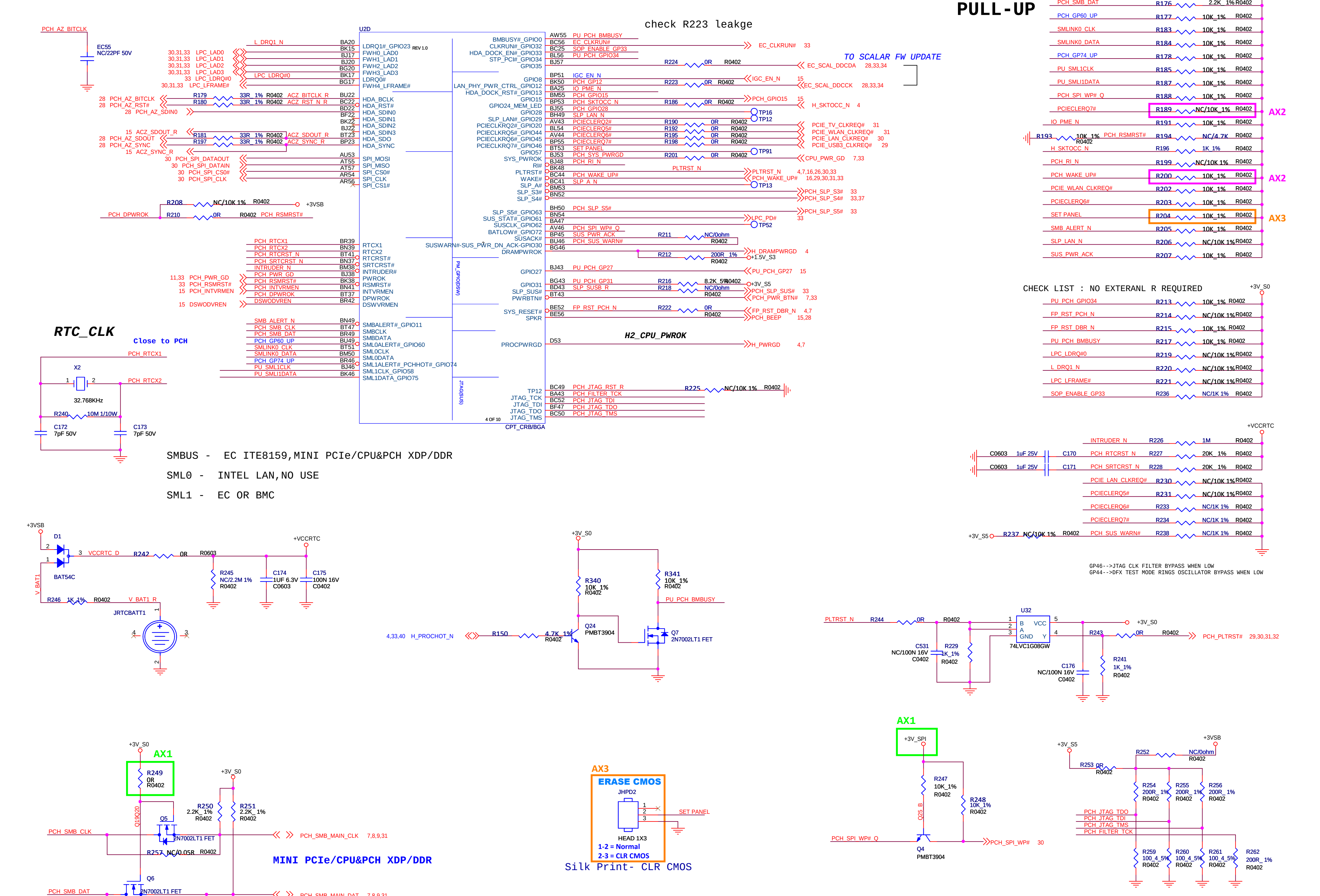
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	11 of 45		

PCH_HDA/SPI/LPC/MISC



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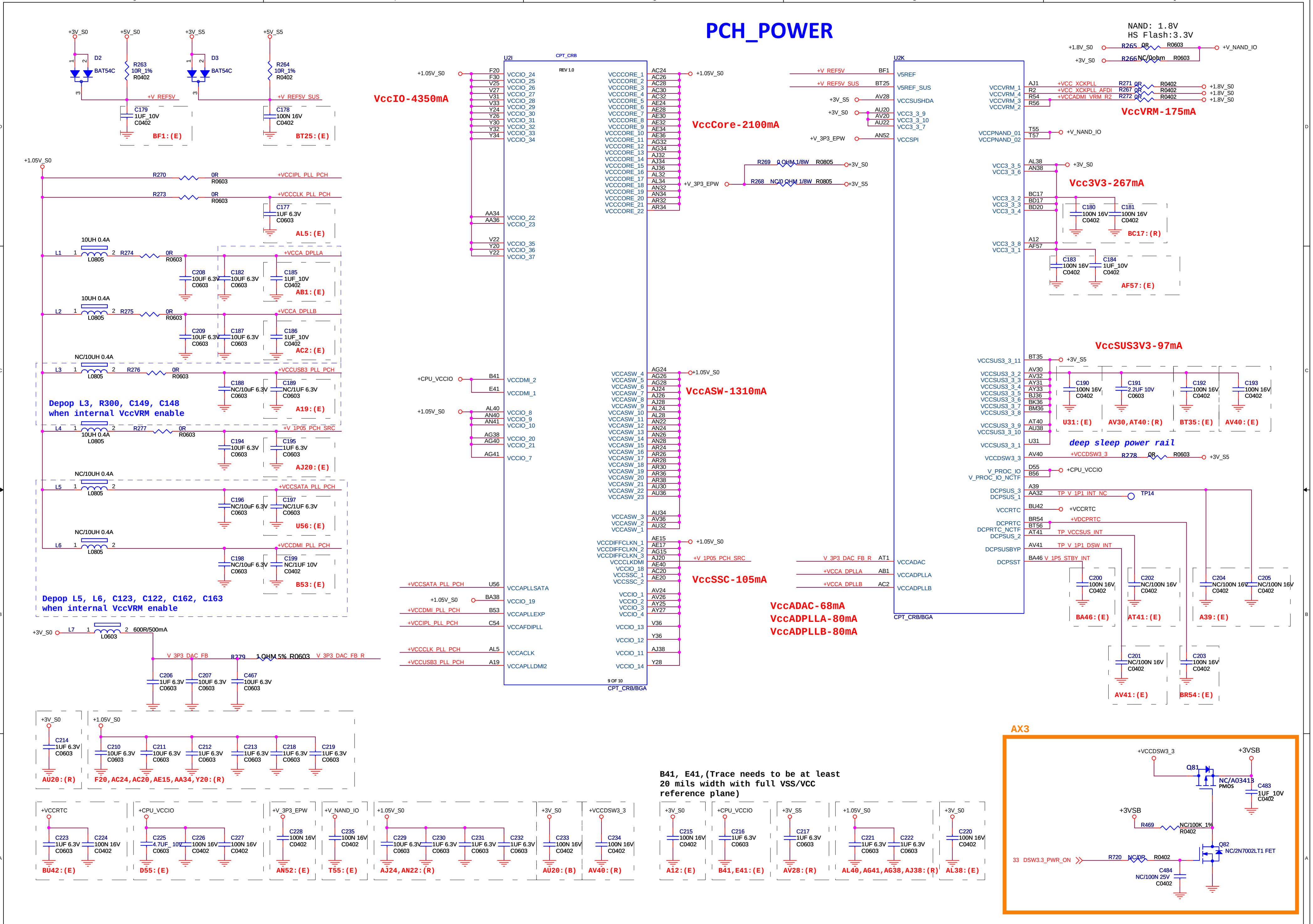
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXX	remark	<remark>
Date	Monday, April 23, 2012	Sheet	12 of 45		



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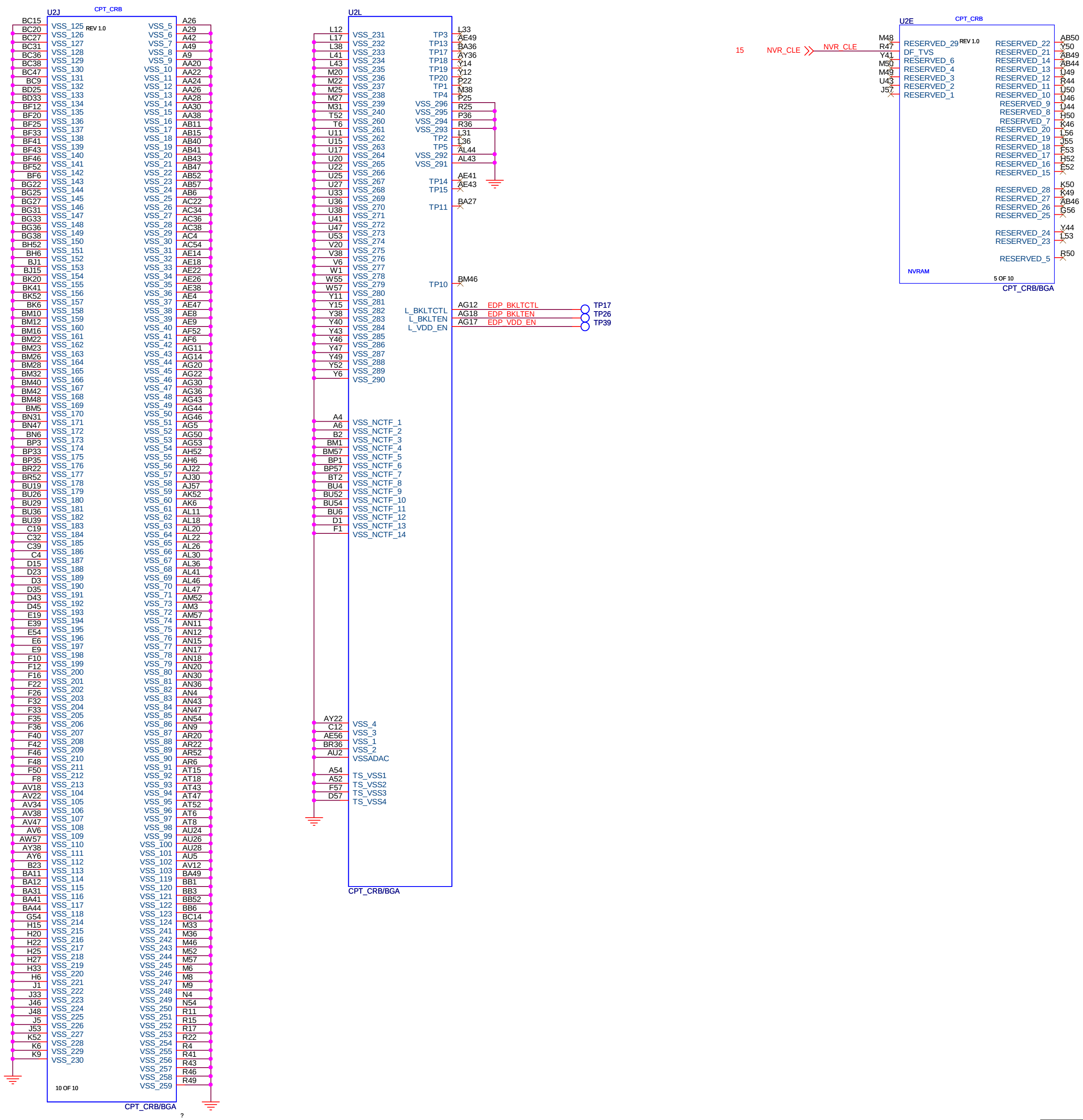
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	13 of 45		

PCH_GND



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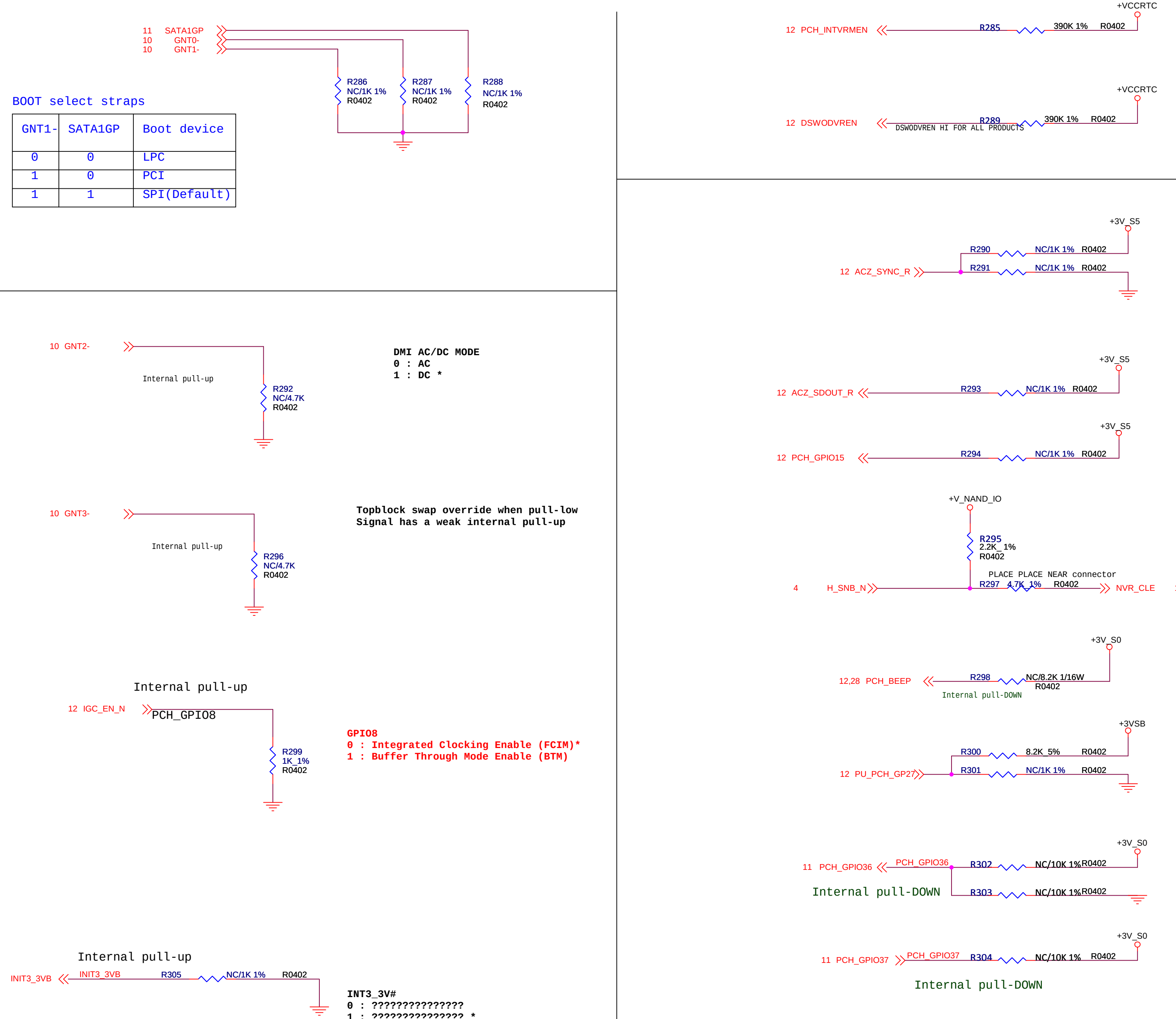
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	14 of 45		

PCH REQUIRED STRAPS



BOOT select straps

GNT1-	SATA1GP	Boot device
0	0	LPC
1	0	PCI
1	1	SPI(Default)

INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltageregulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.

DMI AC/DC MODE
0 : AC
1 : DC *

Topblock swap override when pull-low
Signal has a weak internal pull-up

GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

INT3_3V#
0 : ???????????????
1 : ??????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high

GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY

DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

In Deep Sleep Power Well.
If not used,require a weak pull-up(8.2k~10k) to VccDSW3_3

Cougar point EDS PAGE:93 This signal should not be pull high

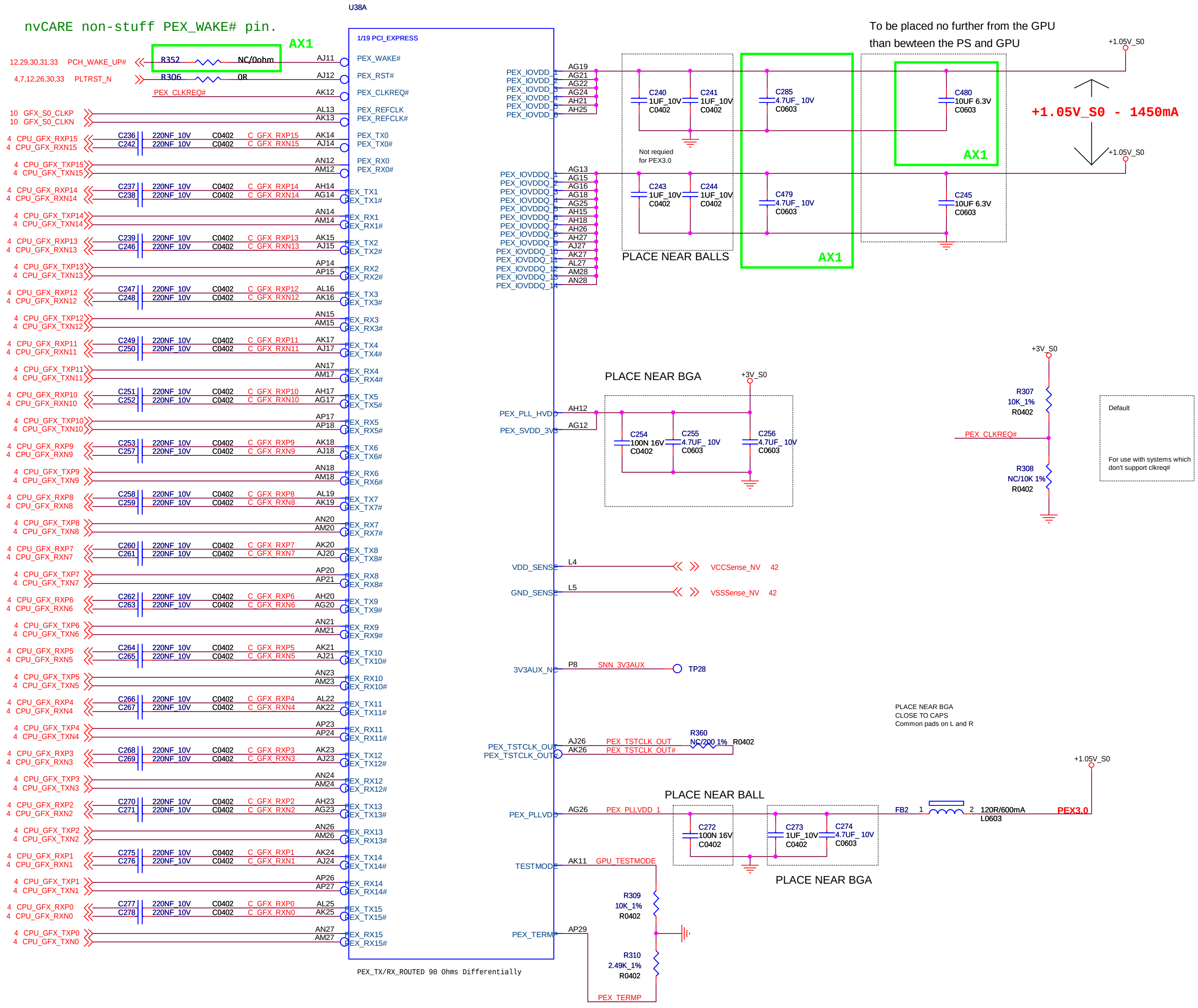
Cougar point EDS PAGE:93 This signal should not be pull high

T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	Custom
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	15 of 45		

GPU_PCI-Express Gen2 x16

BOM Option

GPU STUFF ALL



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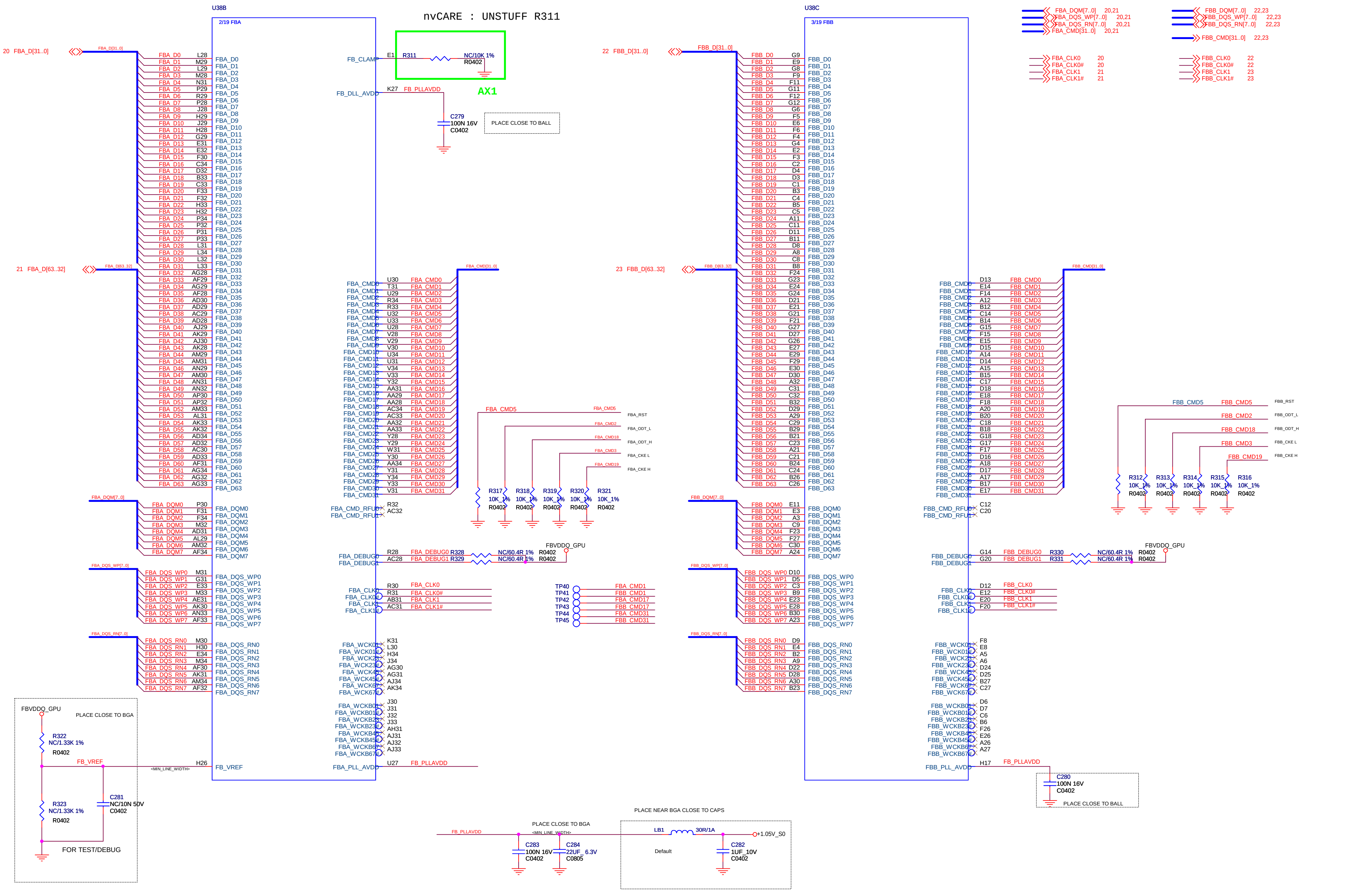
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	16 of 45		

GPU_Frame Buffer Partitions A/B

BOM Option

GPU STUFF



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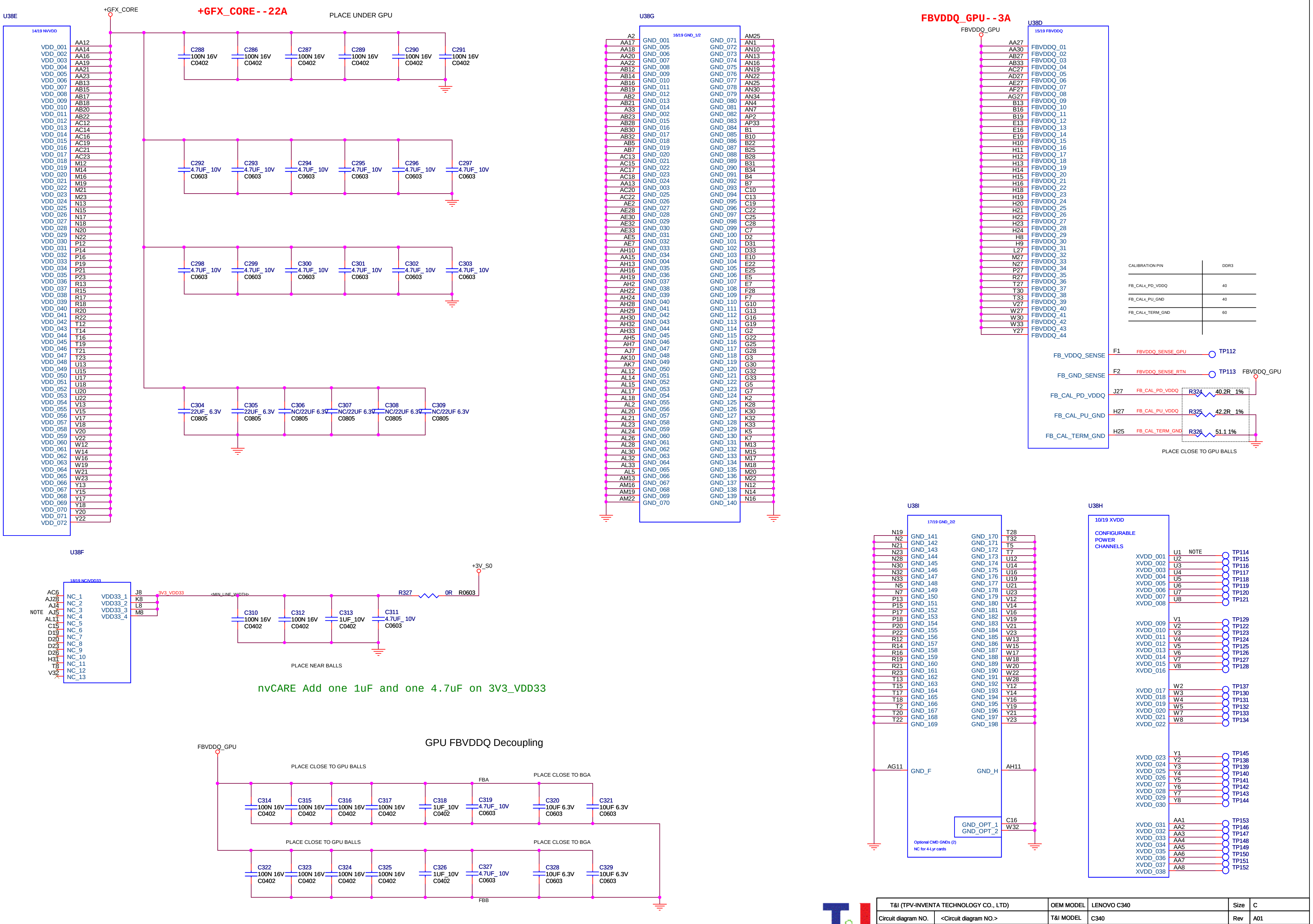
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	17 of 45		

GPU_POWER/GND/OPTIONAL

BOM OPTION
GPU STUFF



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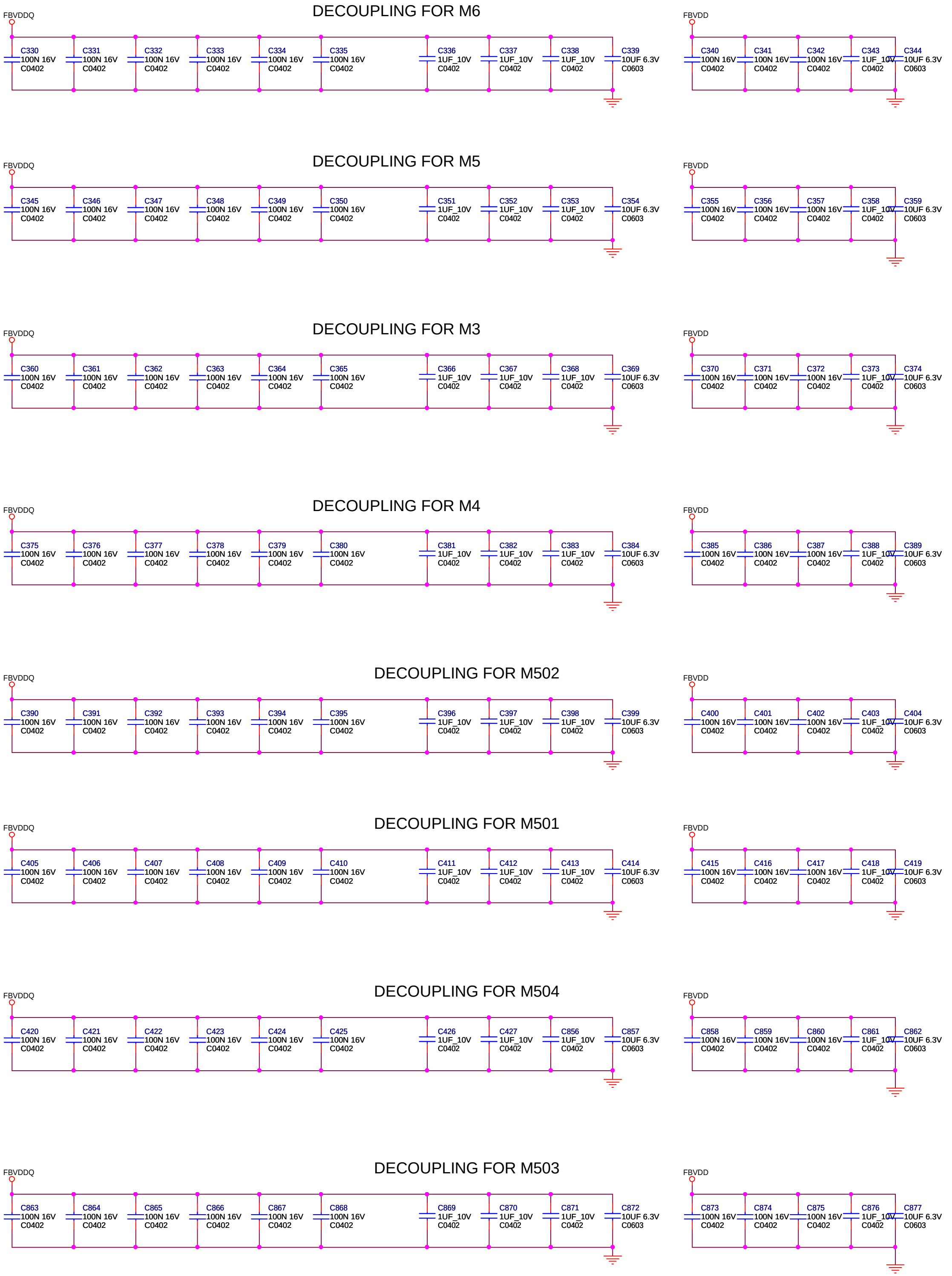
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	18 of 45		

GFX-Mem Decoupling

BOM Option

GPU STUFF



FBVDD--7.0A

BOM Option

UMA --> all don't stuff

GPU --> all stuff

T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	19 of 45		

GPU_Memory Lower Partition A

BOM OPTION

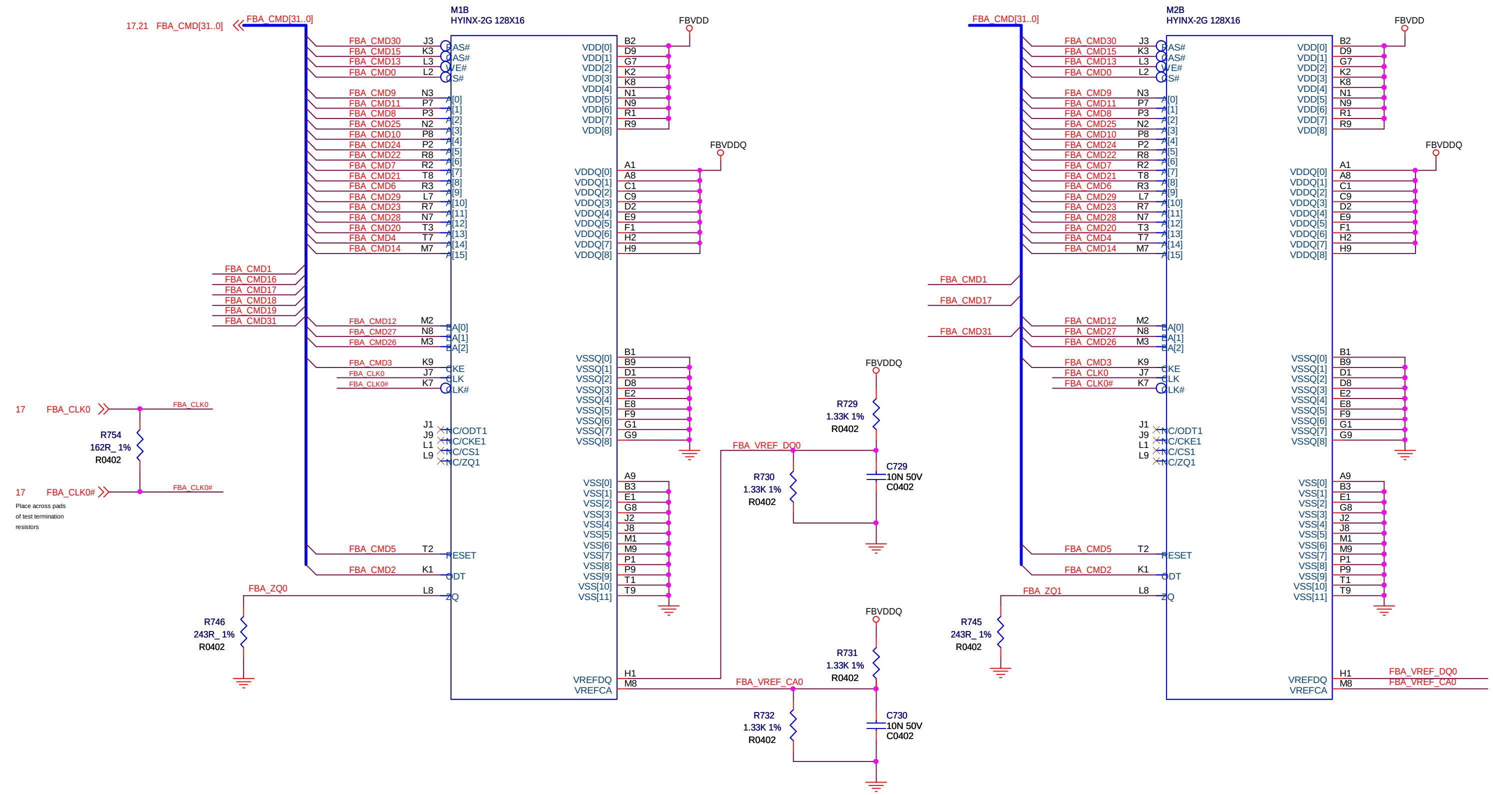
GPU STUFF

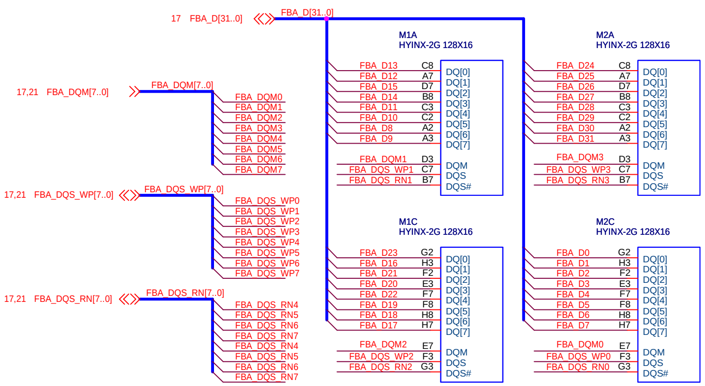
UMA --> all don't stuff

GPU --> N13M-GE2   512MB , 64Mbx16 x4

GPU --> N13M-GE2   1GB , 128Mbx16 x4

GPU --> N13M-GE2   2GB , 128Mbx16 x8





	LOWER 0..31	UPPER 32..63
CMD30	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD5	RST	RST

IN USE ON THIS PAGE

FBA_CLK/* 80DEZ

FBA_DQS_WP/RN 80DEZ

FBA_DQM/M_WP/RN 45SEZ

FBA_CMD 45SEZ

GPU_Memory Upper Partition A

BOM OPTION

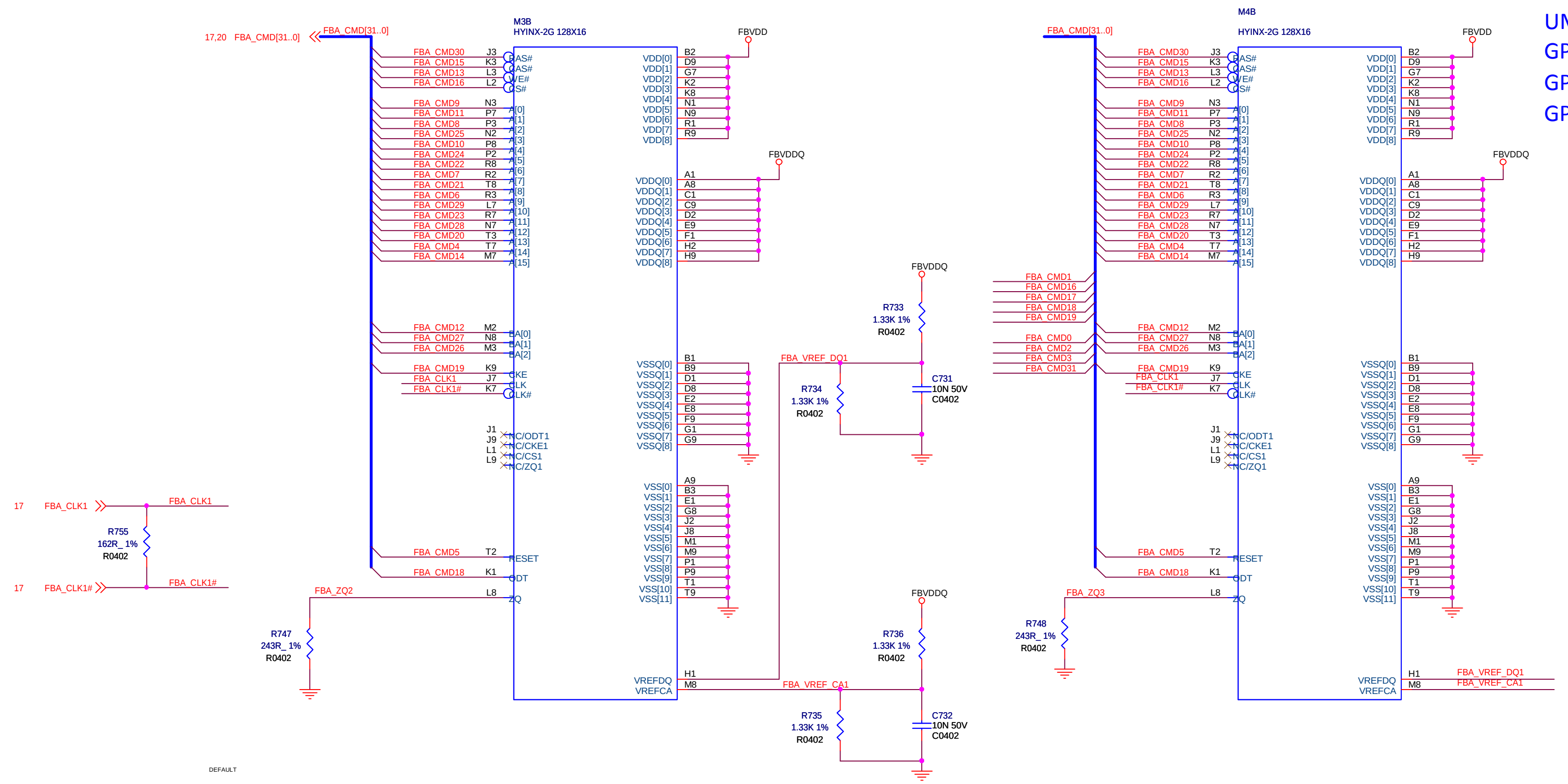
GPU STUFF

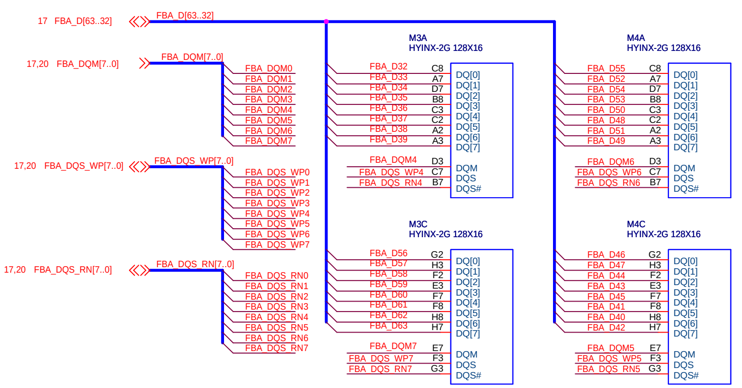
UMA --> all don't stuff

GPU --> N13M-GE2 512MB , 64Mbx16 x4

GPU --> N13M-GE2 1GB , 128Mbx16 x4

GPU --> N13M-GE2 2GB , 128Mbx16 x8





	LOWER 0..31	UPPER 32..63
CMD30	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD5	RST	RST

IN USE ON
THIS PAGE

T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	21 of 45		

GPU_Memory Lower Partition B

BOM OPTION

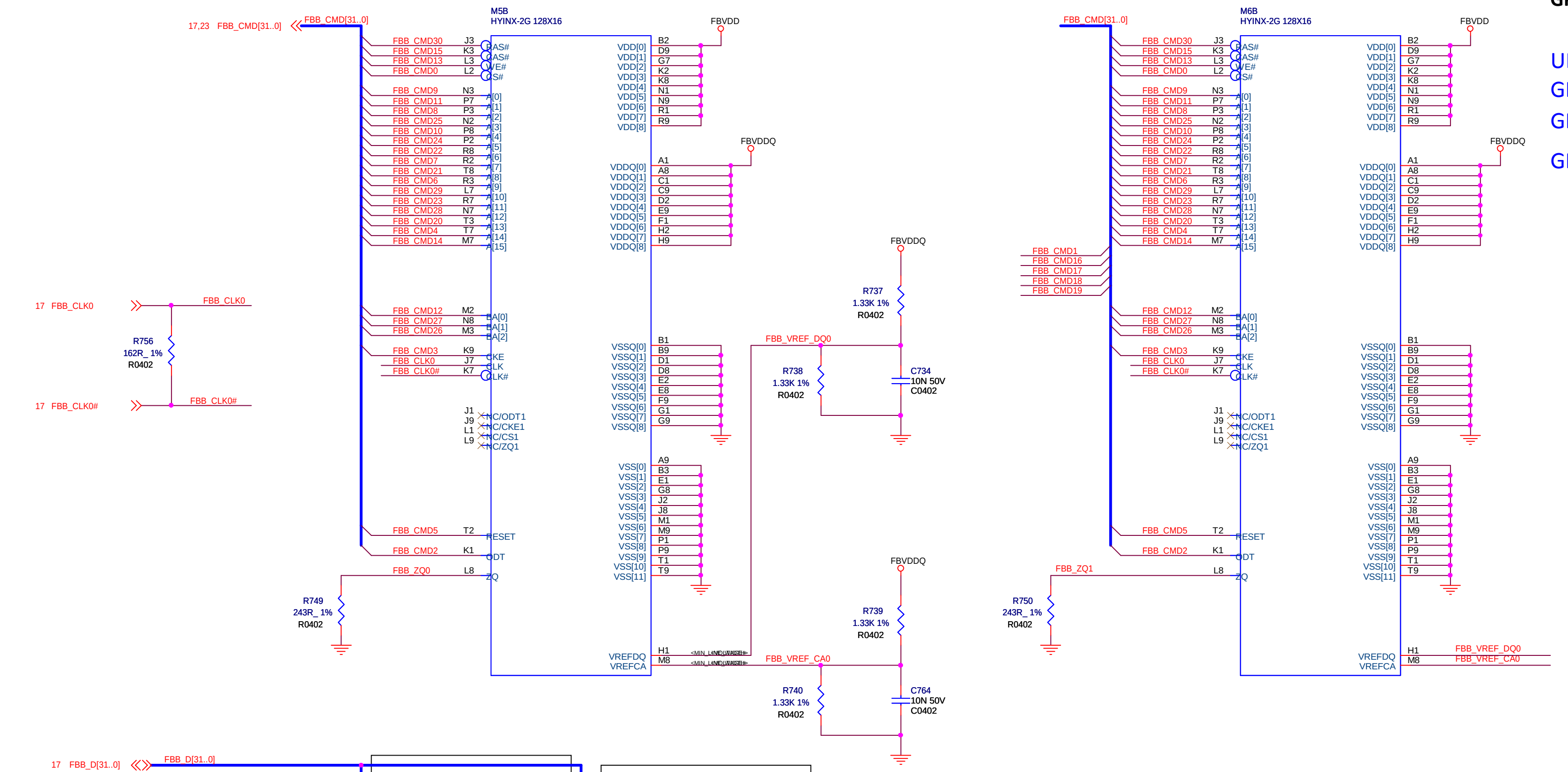
GPU STUFF

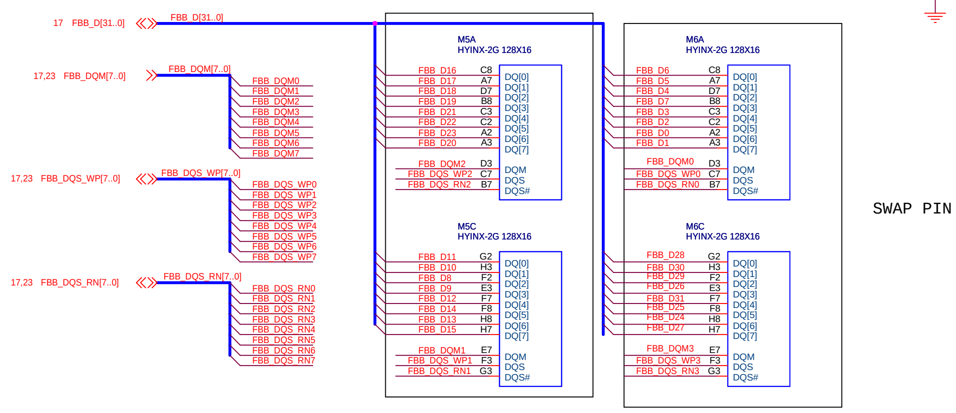
UMA --> all don't stuff

GPU --> N13M-GE2 512MB , 64Mbx16 x4

GPU --> N13M-GE2 1GB , 128Mbx16 x4

GPU --> N13M-GE2 2GB , 128Mbx16 x8





	LOWER 0..31	UPPER 32..63
CMD30	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD5	RST	RST

IN USE ON
THIS PAGE

FBA_CLK/* 80DEZ

FBA_DQS_WP/RN 80DEZ

FBA_DQ/M_WP/RN 45SEZ

FBA_CMD 45SEZ

T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	22 of 45		

GPU_Memory Upper Partition B

BOM OPTION

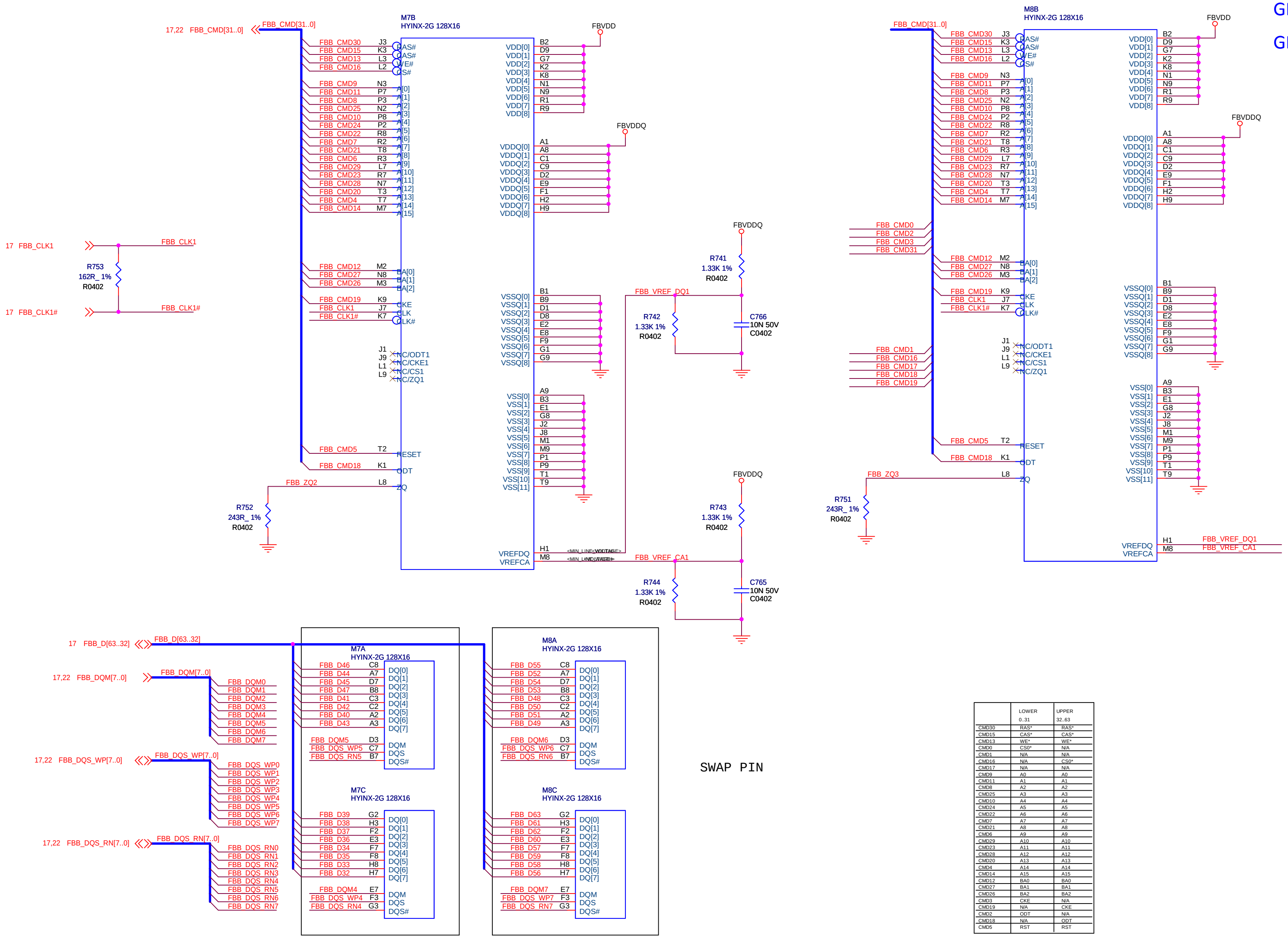
GPU STUFF

UMA --> all don't stuff

GPU --> N13M-GE2   512MB , 64Mbx16 x4

GPU --> N13M-GE2   1GB , 128Mbx16 x4

GPU --> N13M-GE2   2GB , 128Mbx16 x8



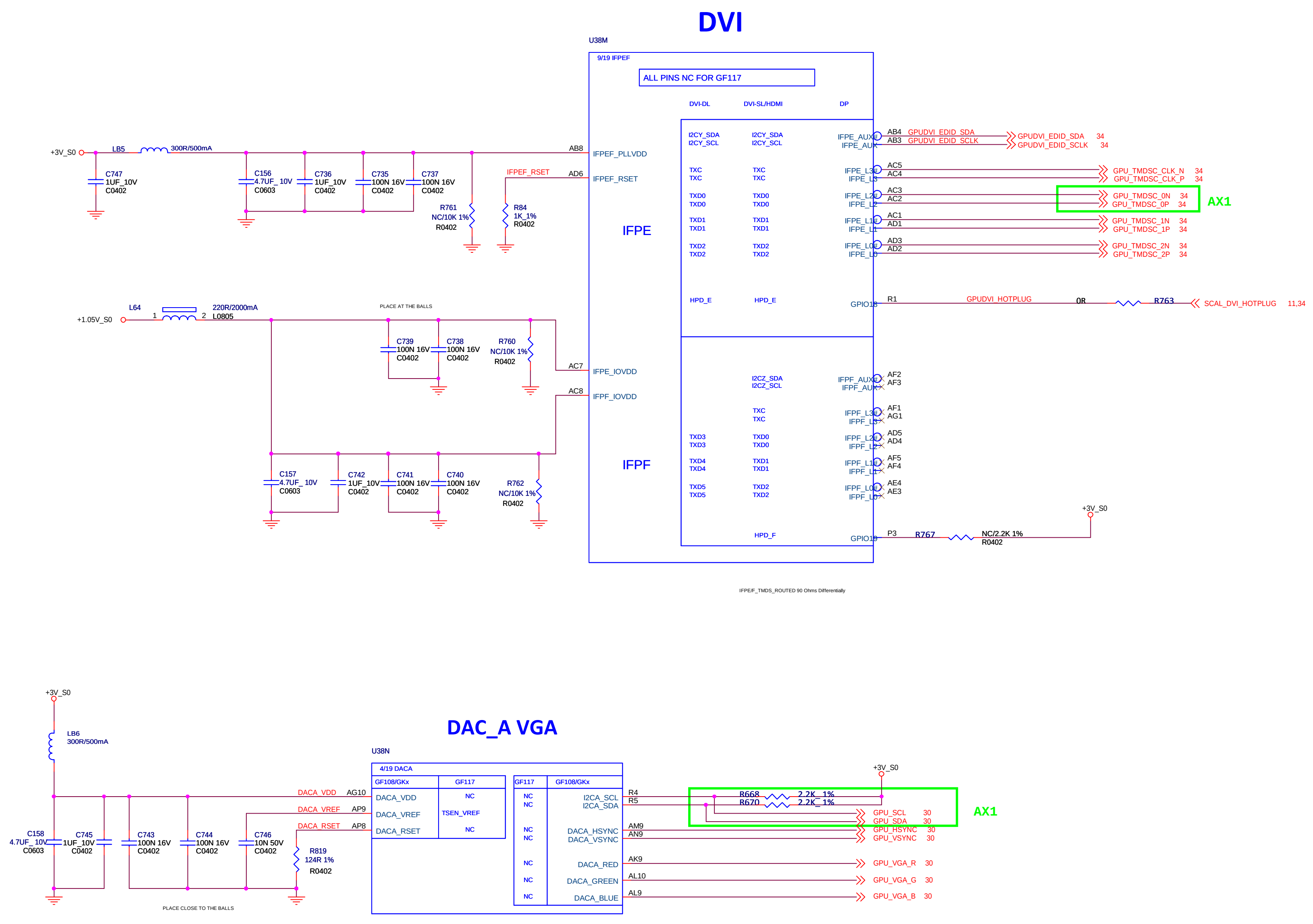
	LOWER 0..31	UPPER 32..63
CMD30	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD5	RST	RST

IN USE ON
THIS PAGE

GPU_IFPE/F Dual Link TMDS DVI-I

BOM Option

GPU STUFF

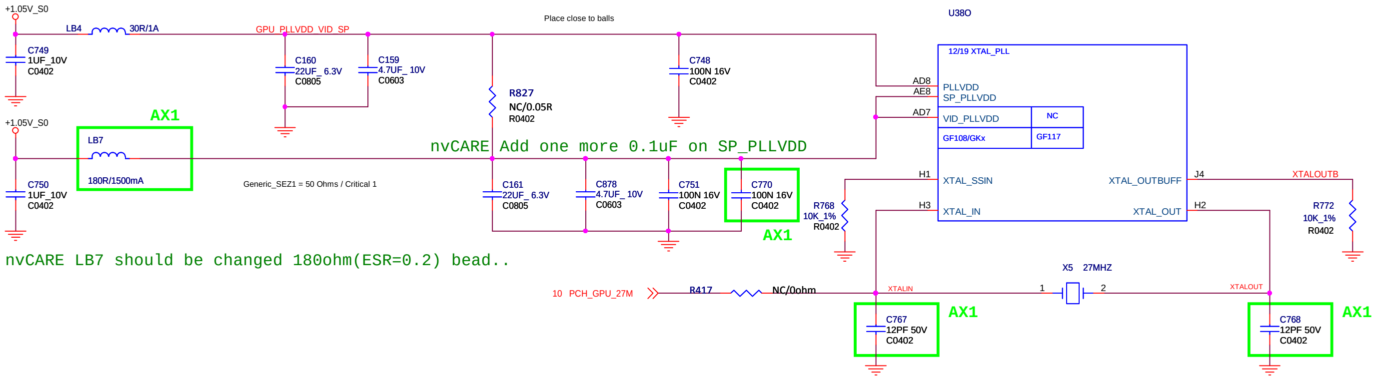


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	24 of 45		

GPU_BIOS, External SS, and Mechanical Components

BOM Option
GPU STUFF

Place Close to GPU



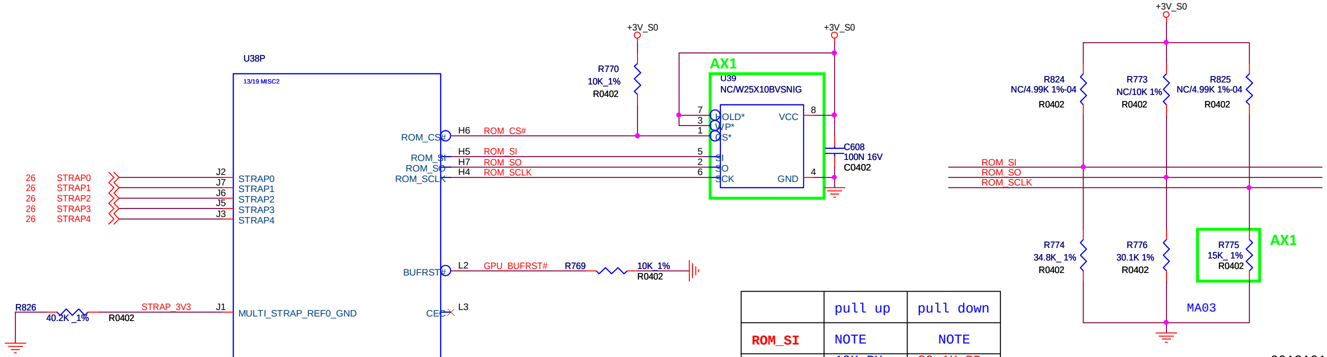
BOM OPTION
GPU STUFF

RESISTER MAPING

	PU_3V3	PD_GND
4.99K	1000 (8)	0000 (0)
10.0K	1001 (9)	0001 (1)
15.0K	1010 (A)	0010 (2)
20.0K	1011 (B)	0011 (3)
24.9K	1100 (C)	0100 (4)
30.1K	1101 (D)	0101 (5)
34.8K	1110 (E)	0110 (6)
45.3K	1111 (F)	0111 (7)

BOM OPTION

BIOS ROM



N13X DO NOT SUPPORT HDMI CEC FUNCTION,CEC PIN =NC

	pull up	pull down
ROM_SI	NOTE	NOTE
ROM_SO	10K PU N13P-GT	30.1K PD N13M-GE2
ROM_SCLK	24.9K PU N13P-GT	34.8K PD N13M-GE2

ROM_SCLK=> 34.8K 1%-04 Pull LOW N13M-GE2

NOTE N13M-GE2
128X16 DDR3 samsung 0X7 K4W2G1646C-HC11
PD 45.3K STRAP CODE 07(0111)
64X16 DDR3 samsung 0X3 K4W1G1646G-BC11
PD 20K STRAP CODE 03(0011)

128X16 DDR3 Hynix 0X6 H5TQ2G63BFR-11C
PD 34.8K Hynix 0X6 H5TQ2G63DFR-11C
PD 34.8K STRAP CODE 06(0110)
64x16 DDR3 Hynix 0X2 H5TQ1G63DFR-11C
PD 15K STRAP CODE 02(0010)

6013A0107901	45.3K_4_ 1%	6019B0906601	SS K4W2G1646C-HC11
6113A0003601	20K_4_ 1%	6019B0818501	SS K4W1G1646G-BC11
6013A0017901	34.8K_4_ 1%	6019B0938301	Hynix H5TQ2G63DFR-11C
6013A0017201	15K_4_ 1%	6019B0873101	Hynix H5TQ1G63DFR-11C

GF108 STRAPPING MODE TABLE

PIN NAME	MULTI-LEVEL	BINARY PRODUCTION	BINARY BRINGPUP
MULTI_STRAP_REF_GND	40.2K TO GND	NO STUFF	NOT SUPPORTED

GF117/GK10X STRAPPING MODE TABLE

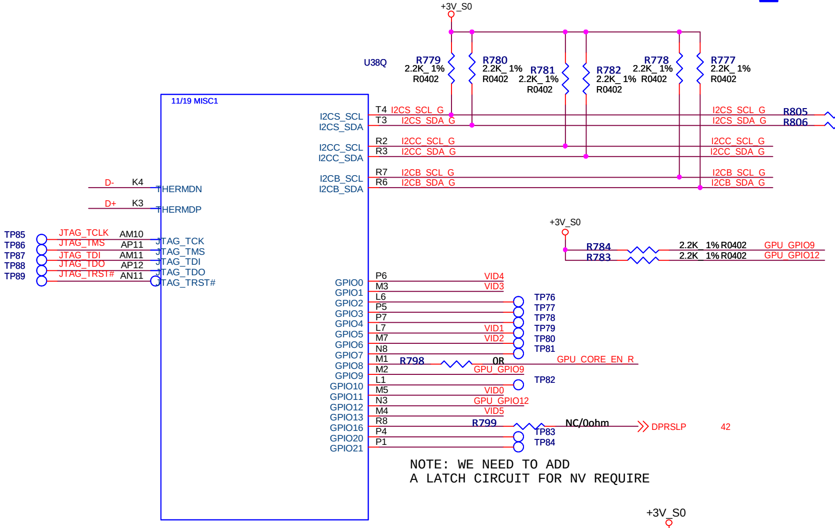
PIN NAME	MULTI-LEVEL	BINARY PRODUCTION	BINARY BRINGPUP
MULTI_STRAP_REF_GND	40.2K TO GND	NOT SUPPORTED	NO STUFF

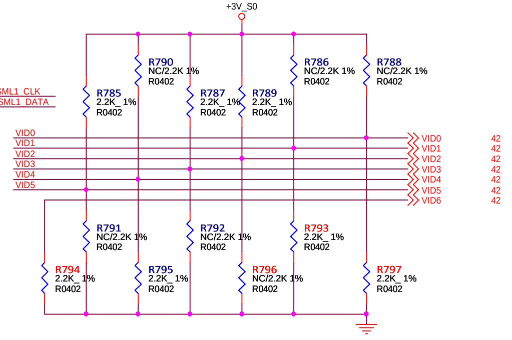
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	25 of 45		

GPU_GPIOs, Thermal Sensor, I2C/GPIO Expanders

BOM Option

GPU STUFF

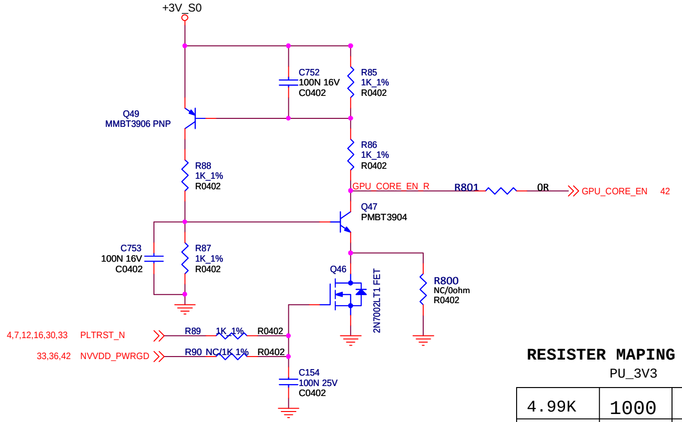




VID6	VID5	VID4	VID3	VID2	VID1	VID0	0,95V N13M-GE2
0	1	0	1	1	0	0	DEFULT

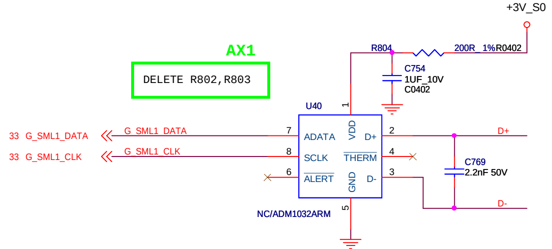
GPIO	Function	GPIO	Function
GPIO 0	Debug/Service Header/Alt_Fan PWM		I2C PORT C
GPIO 1	VID 2	EXPND 0	Level Shifter Error Correction
GPIO 2	LCD brightness control (BL PWM)	EXPND 1	NVGEM GPIO EXP1/ PS_Margin*
GPIO 3	LCD Power enable (PPEN)	EXPND 2	NVGEM GPIO EXP2/PS_MR*
GPIO 4	LCD Backlight enable (BLEN)	EXPND 3	GPIO_DEBUG_SERVICE HEADER
GPIO 5	VID 0		
GPIO 6	VID 1		SMBUS
GPIO 7	3D STEREO		
GPIO 8	GPU Overtemp	EXPND 4	GPU_PS_EN
GPIO 9	GPU thermal Alert	EXPND 5	RSVD
GPIO 10	FB Vref Control (not used sDDR3)	EXPND 6	PEX_RST
GPIO 11	FBVDD/Q VID (Reserved)	EXPND 7	RSVD
GPIO 12	PWR_Level AC Detect		
GPIO 13	PS1 Vprgm Enable		
GPIO 14	HPD for IFP AB (not used)		
GPIO 15	HPD for IFP C (HDMI/DP)		
GPIO 16	Fan PWM control		
GPIO 17	HPD for IFP D (DP)		
GPIO 18	HPD for IFP E (DVI-I DL)		
GPIO 19	HPD for IFP F (not used)		
GPIO 20	NVGEM Debug GPIO13		
GPIO 21	NVGEM Debug GPIO14		

	pull up	pull down
STARP0	GR133 PU 45.3K	
STARP1		GR139 PD 34.8K
STARP2	GR135 15k PU N13M-GE2	GR140 10k PD N13P-GT
STARP3	GR136 PU 34.8K 1110	
STARP4		GR142 PD GR142 NC N13P-GT N13M-GE2



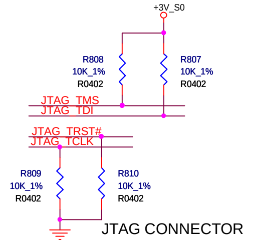
AX1

DELETE R802,R803



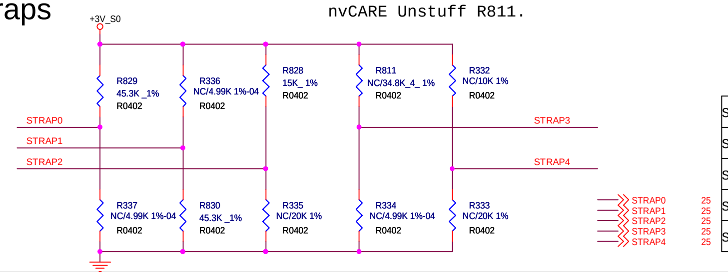
RESISTER MAPING

	PU_3V3	PD_GND
4.99K	1000	0000
10.0K	1001	0001
15.0K	1010	0010
20.0K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111



Straps

nvCARE Unstuff R811.



STRAP TABLE

STRAP 0	1111
STRAP 1	0111
STRAP 2	1010
STRAP 3	1110
STRAP 4	

GF108 STRAP PIN MODE TABLE

PIN NAME	MULTI-LEVEL bit [3:0]	BINARY PRODUCTION	BINARY BRINGUP
STRAP0	USER[3:0]	RAMCFG0	
STRAP1	3GIO_PADCFG_ADR[3:0]	RAMCFG1	
STRAP2	PCI_DEVID[3:0]	RAMCFG2	
ROM_SCLK	PCIDEVID[4], SUB_VENDOR, SLOT_CLK, PEX_PLL_EN_TERM	PCI_DEVID3	
ROM_SI	RAMCFG[3:0]	PCI_DEVID_EXT	
ROM_SO	XCLK_417, FB0_BAR_SIZE, SMB_ALT_ADDR, VGA_DEVICE	XCLK_417	

NOTE 2: See table 1 for the correct value/location of the strap resistor for the desired modes

NOTE 3: Bring-up SKU(s) have jumper configurable subvendor and DEVID_4 settings see the ROM_SCLK STRAP

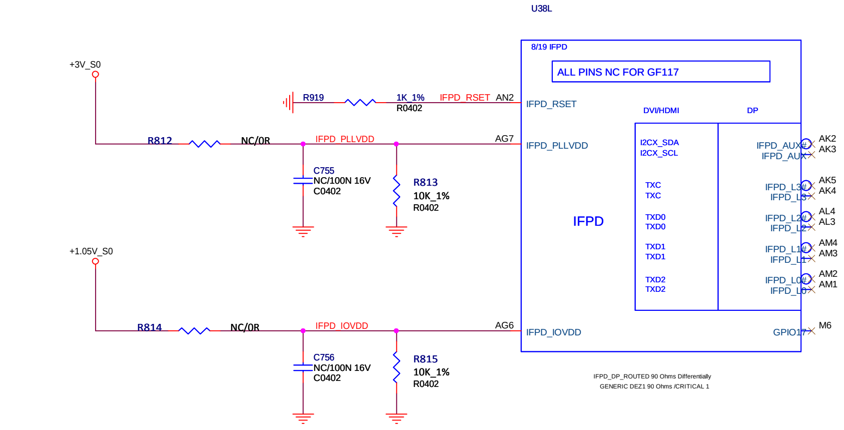
GF117/GK10X STRAP PIN MODE TABLE

PIN NAME	MULTI-LEVEL bit [3:0]	BINARY PRODUCTION	BINARY BRINGUP
STRAP0	USER[3:0]		3GIO_PADCFG_LUT_ADR0
STRAP1	3GIO_PADCFG_ADR[3:0]		3GIO_PADCFG_LUT_ADR1
STRAP2	PCI_DEVID[3:0]		3GIO_PADCFG_LUT_ADR2
STRAP3	SOR[3:0]_EXPOSED		3GIO_PADCFG_LUT_ADR3
STRAP4	RSV, RSV, PCIE_MAX_SPEED, DP_PLL_VDD33V		PCIE_MAX_SPEED
ROM_SCLK	DEVID[4], SUB_VENDOR, DEVID[5], PEX_PLL_EN_TERM		SMB_ALT_ADDR
ROM_SI	RAMCFG[3:0]		SUB_VENDOR
ROM_SO	FB[1]_BAR_SIZE, FB[0]_BS, SMB_ALT_ADDR, VGA_DEVICE		VGA_DEVICE

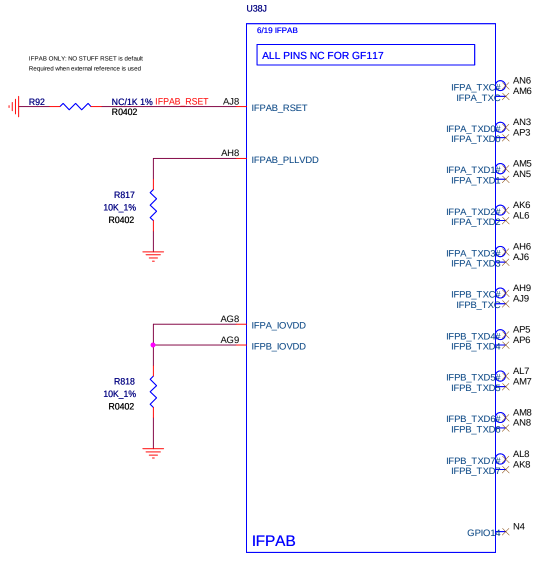
GPU_LVDS/HDMI

BOM Option
GPU STUFF

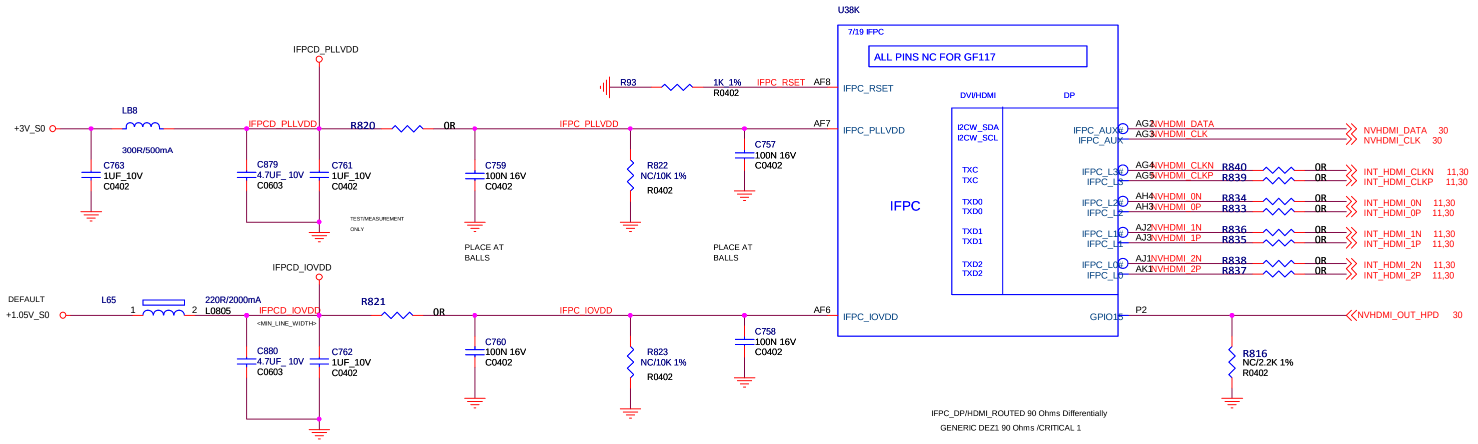
nvCARE : IFPD no used, 10K PD at IFPD_PLLVDD and IFPD_IOVDD.



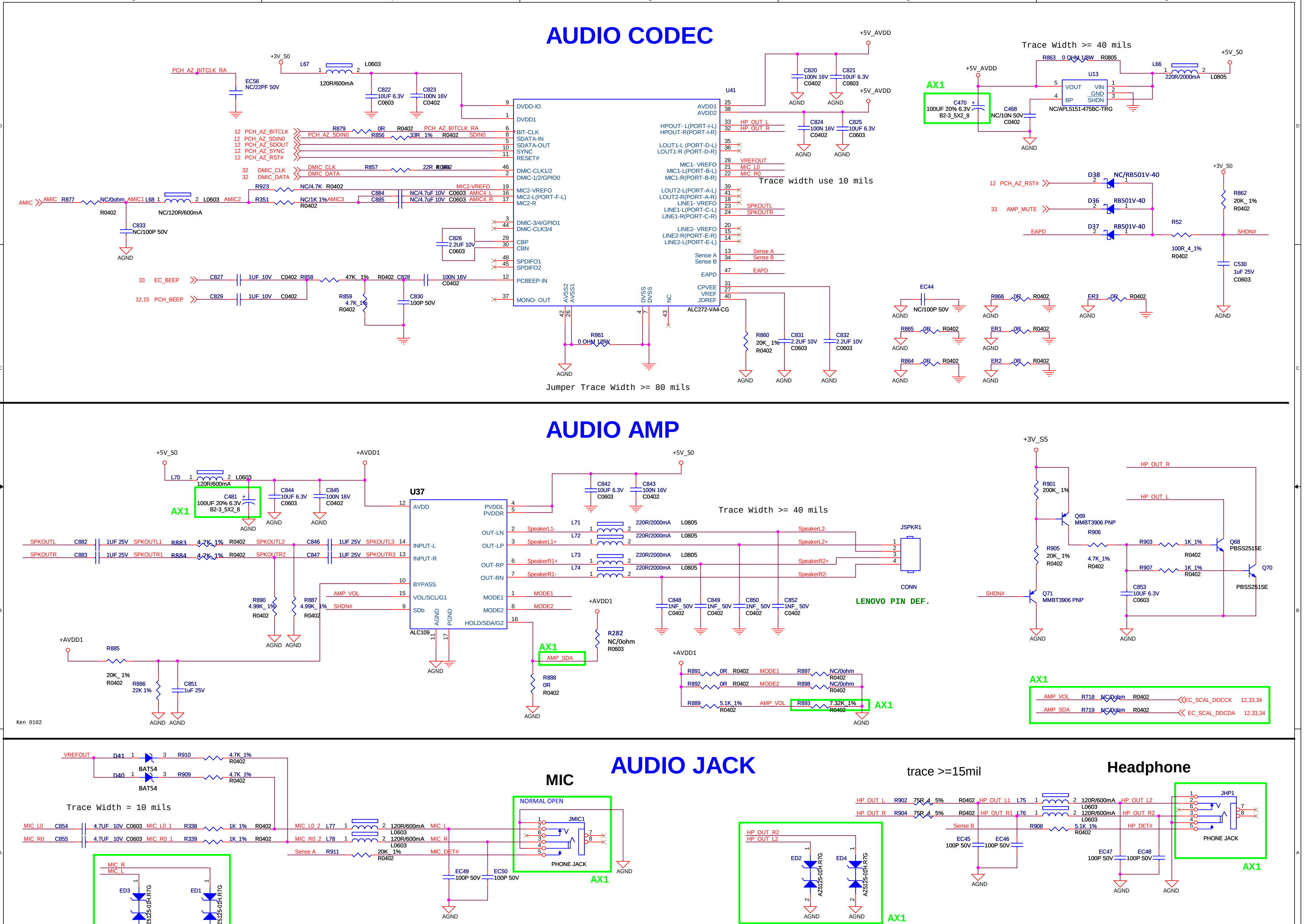
IFPA/B LVDS Dual Link



IFPC NATIVE HDMI OR DP



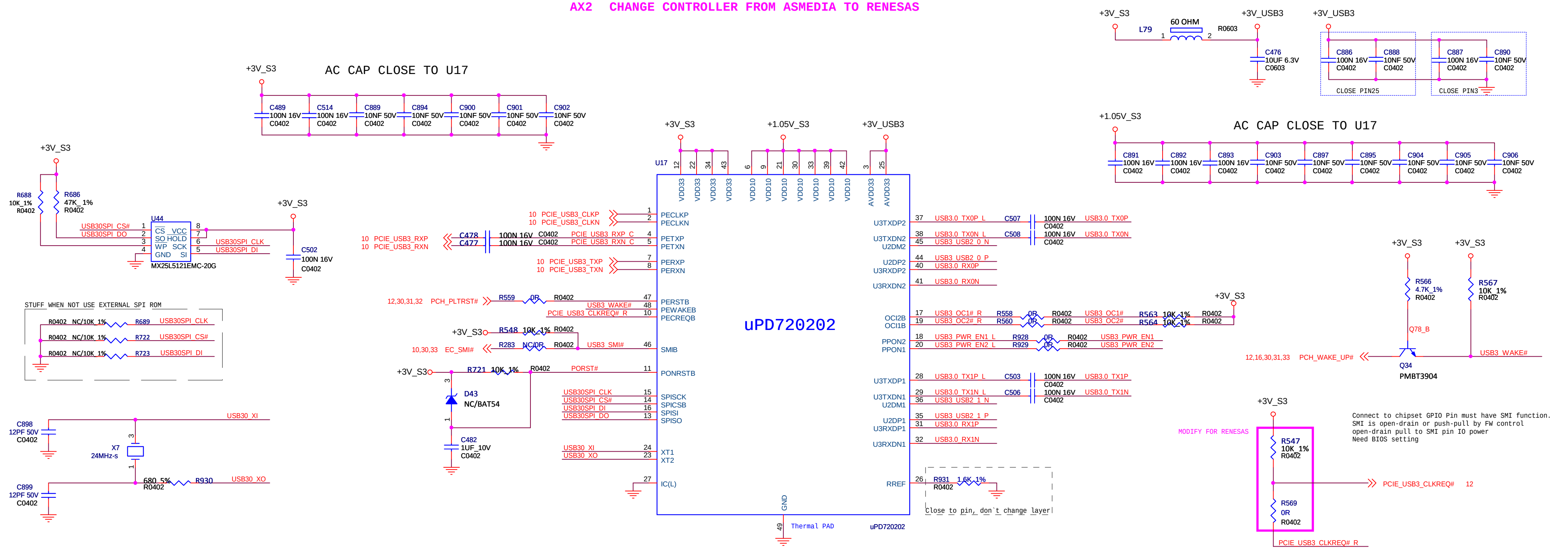
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	27 of 45		



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	28 of 45		

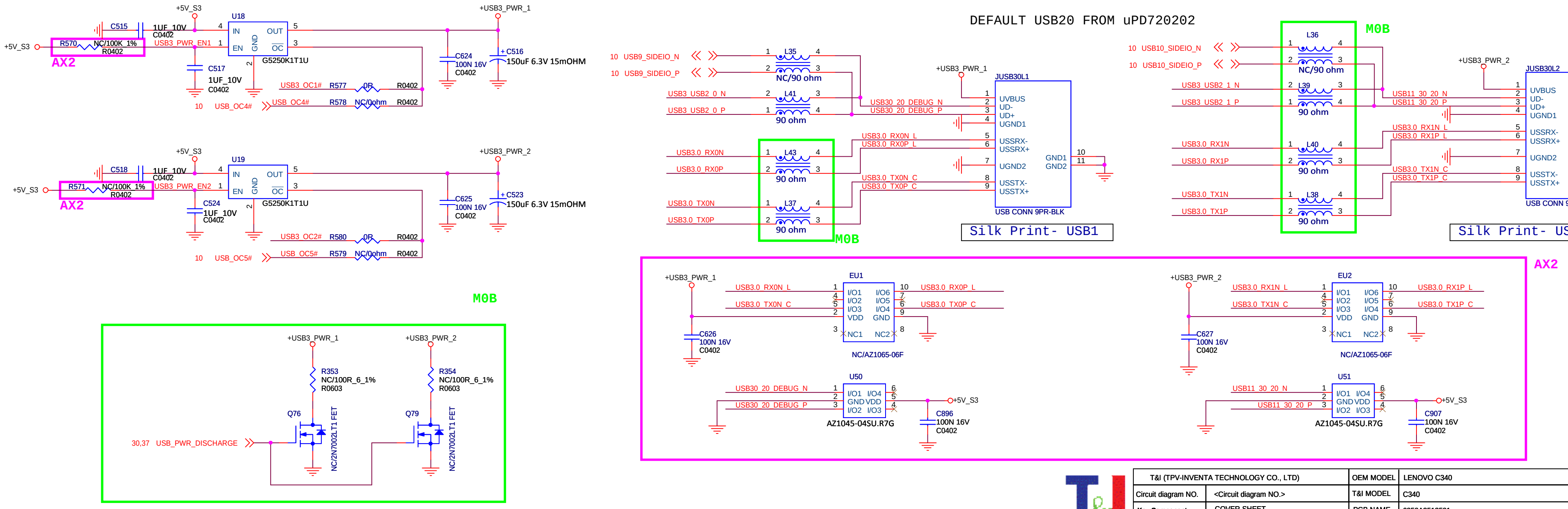
USB3.0 CONTROLLER

AX2 CHANGE CONTROLLER FROM ASMEDIA TO RENESAS



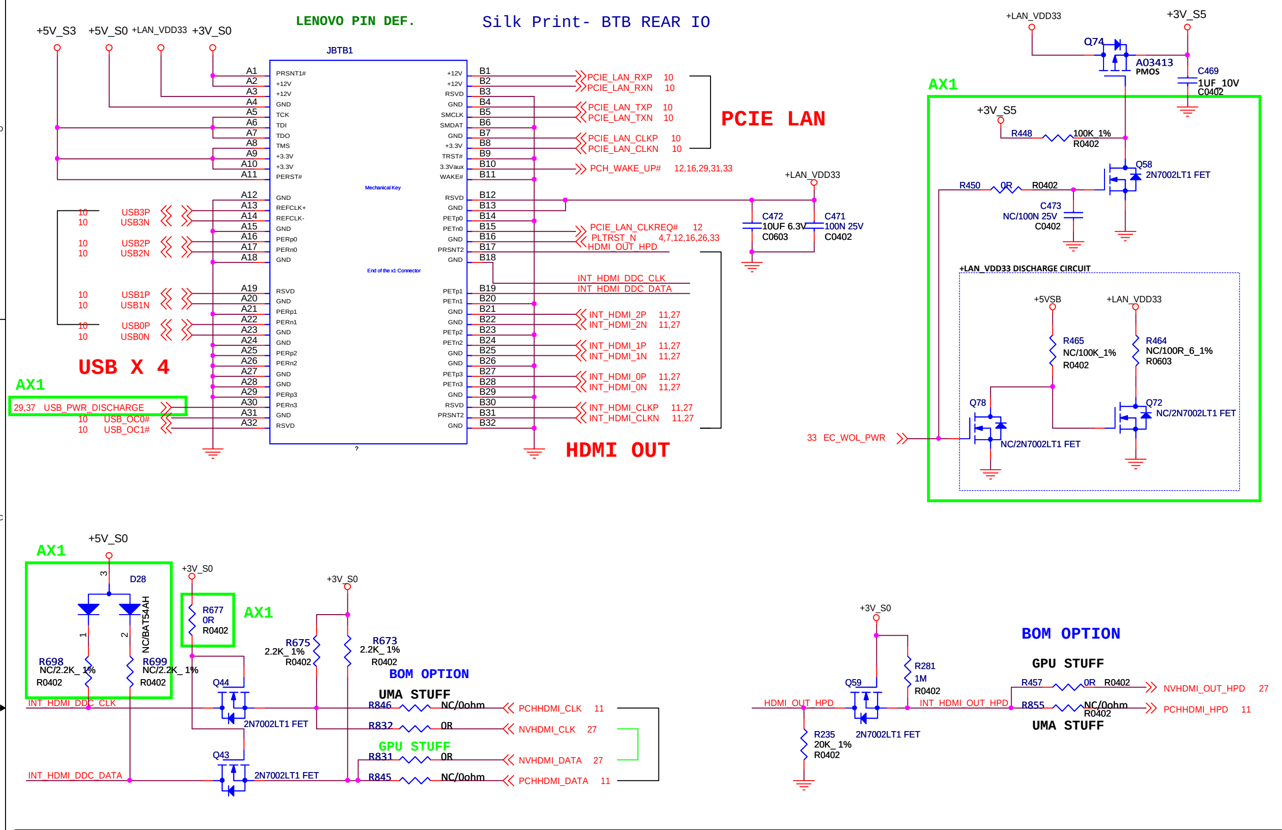
USB 3.0 (Side IO)

DEFAULT USB20 FROM uPD720202

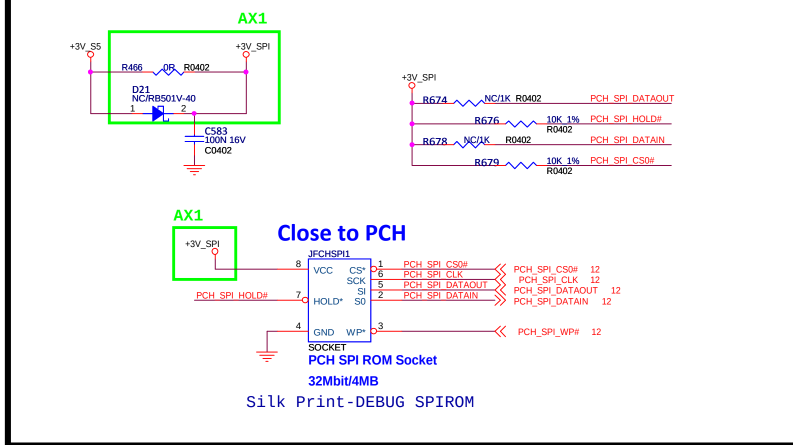


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	29 of 45		

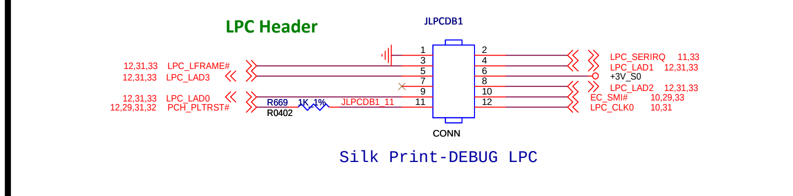
REAR I/O



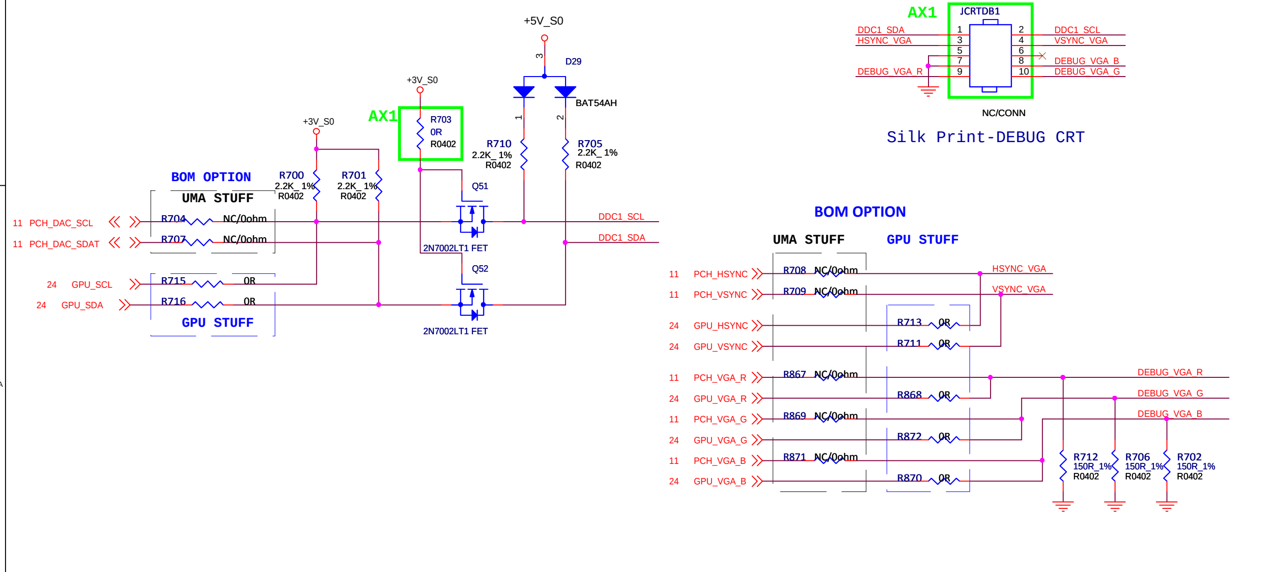
PCH SPI ROM



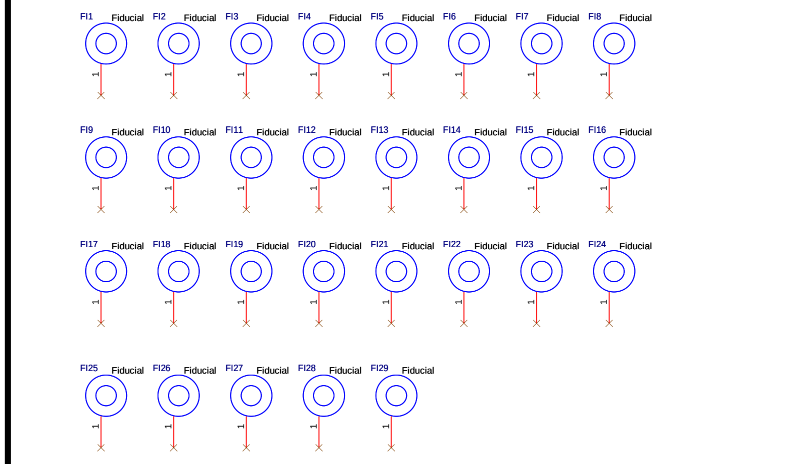
LPC DEBUG PORT



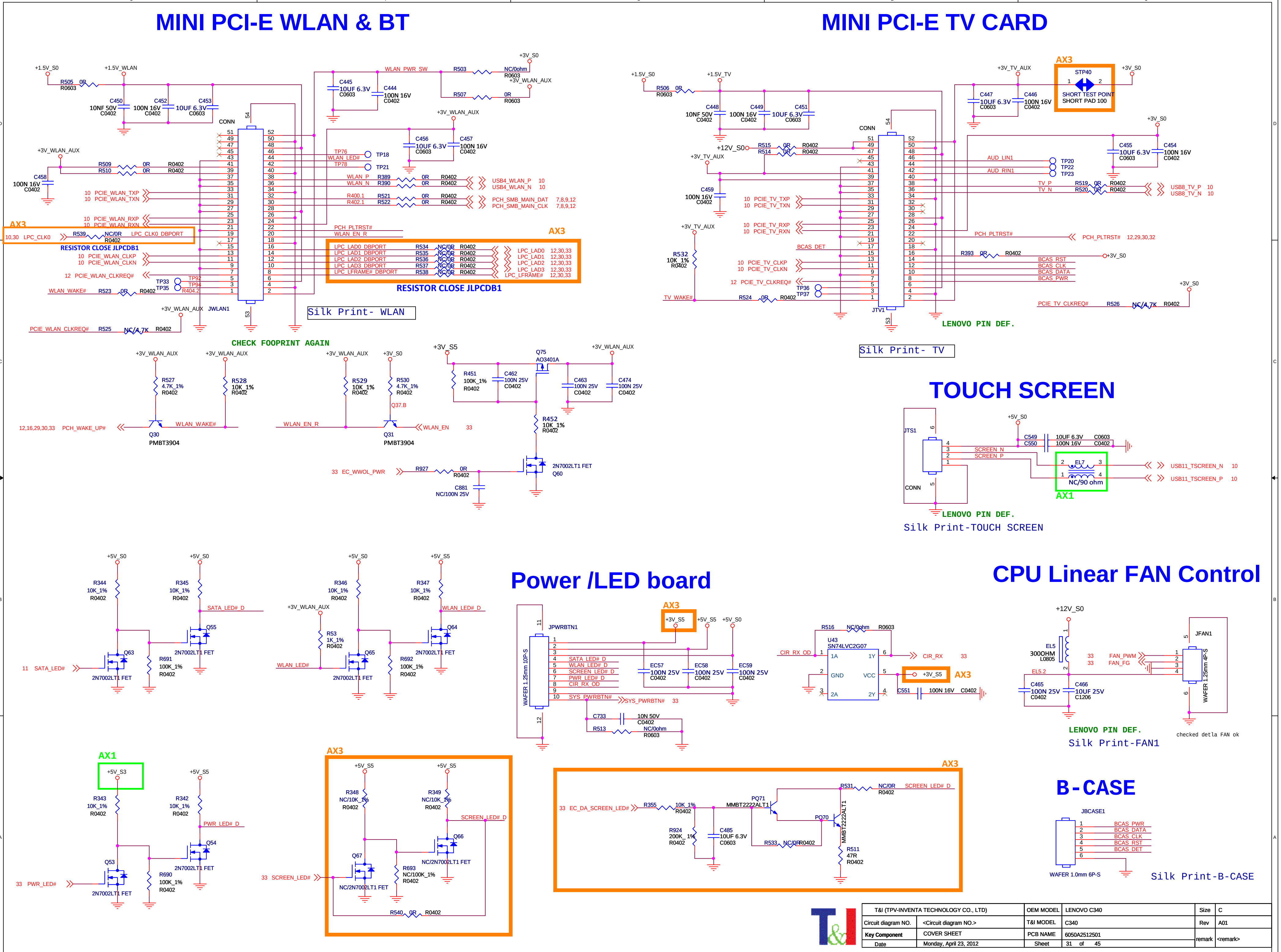
DEBUG CRT



Optical Point

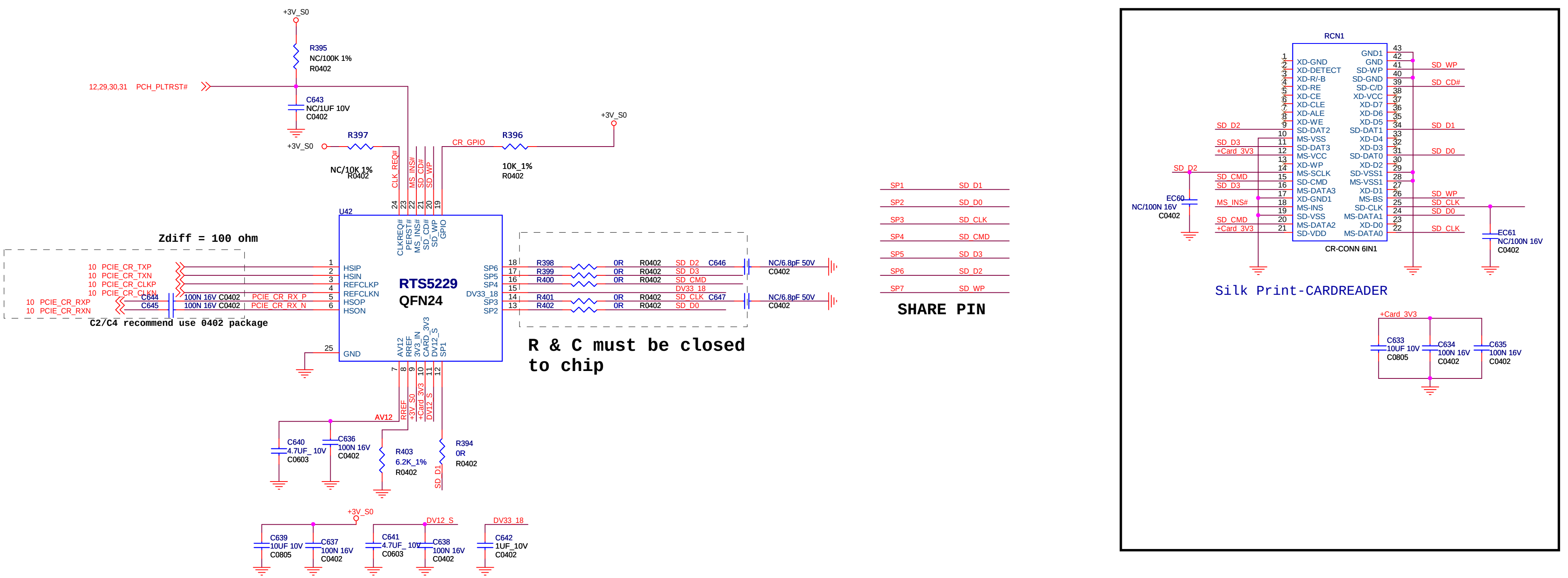


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	30 of 45		



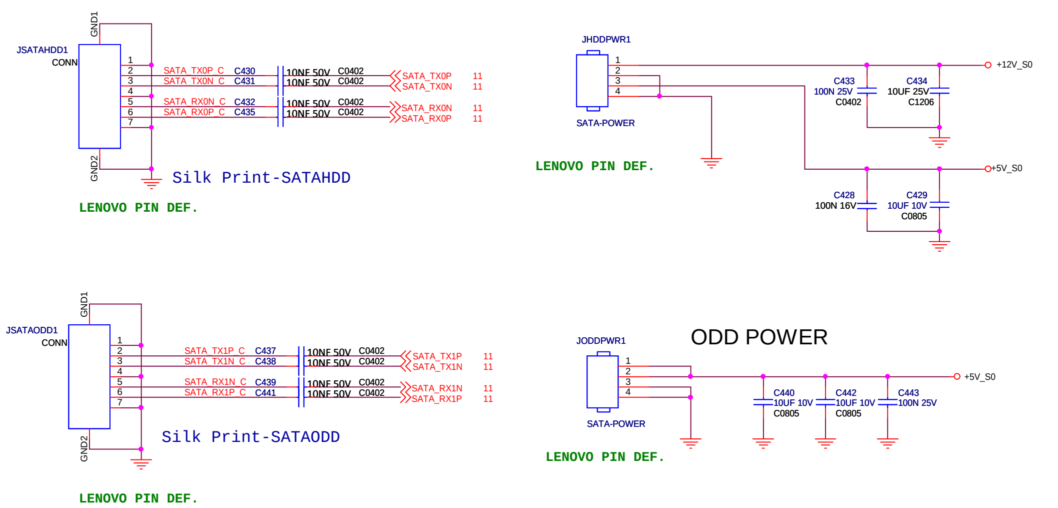
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	31 of 45		

Card Reader RTS5229

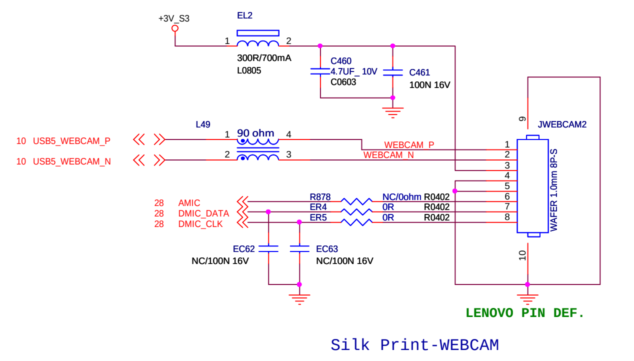


HDD/ODD

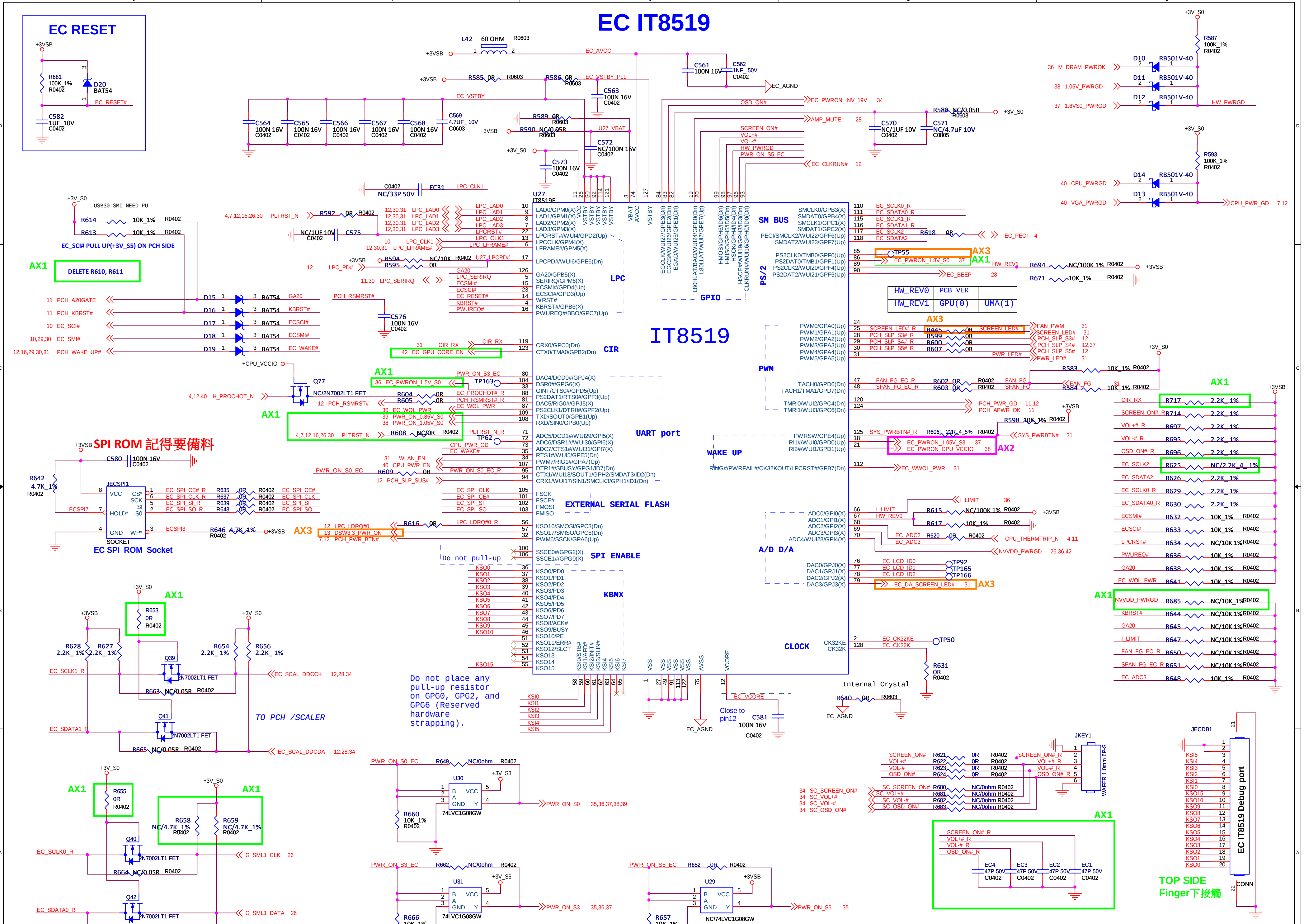
HDD POWER (3.5")



WEB CAM



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	32 of 45		

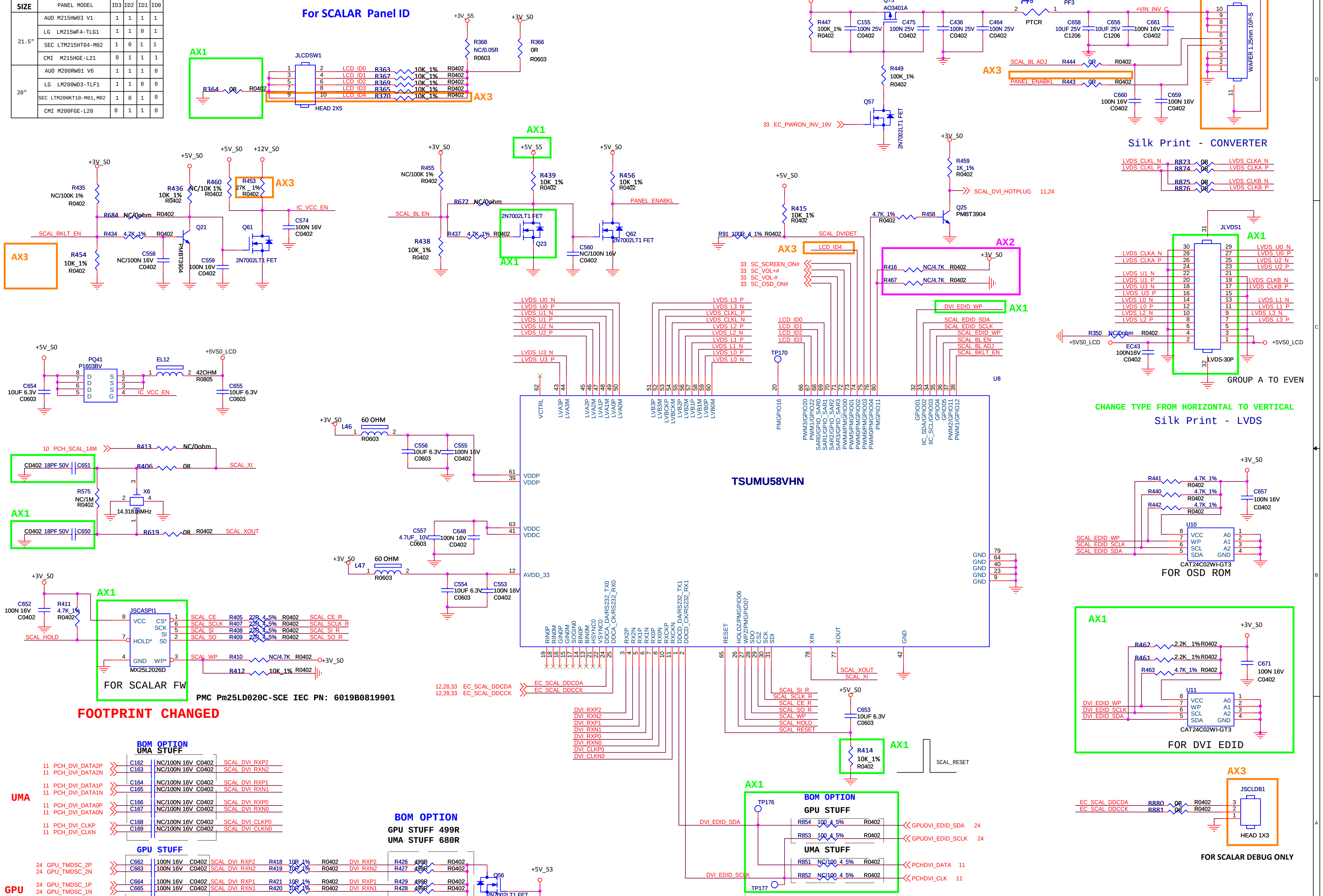


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	33 of 45		

SCALAR TSUMU58VHN

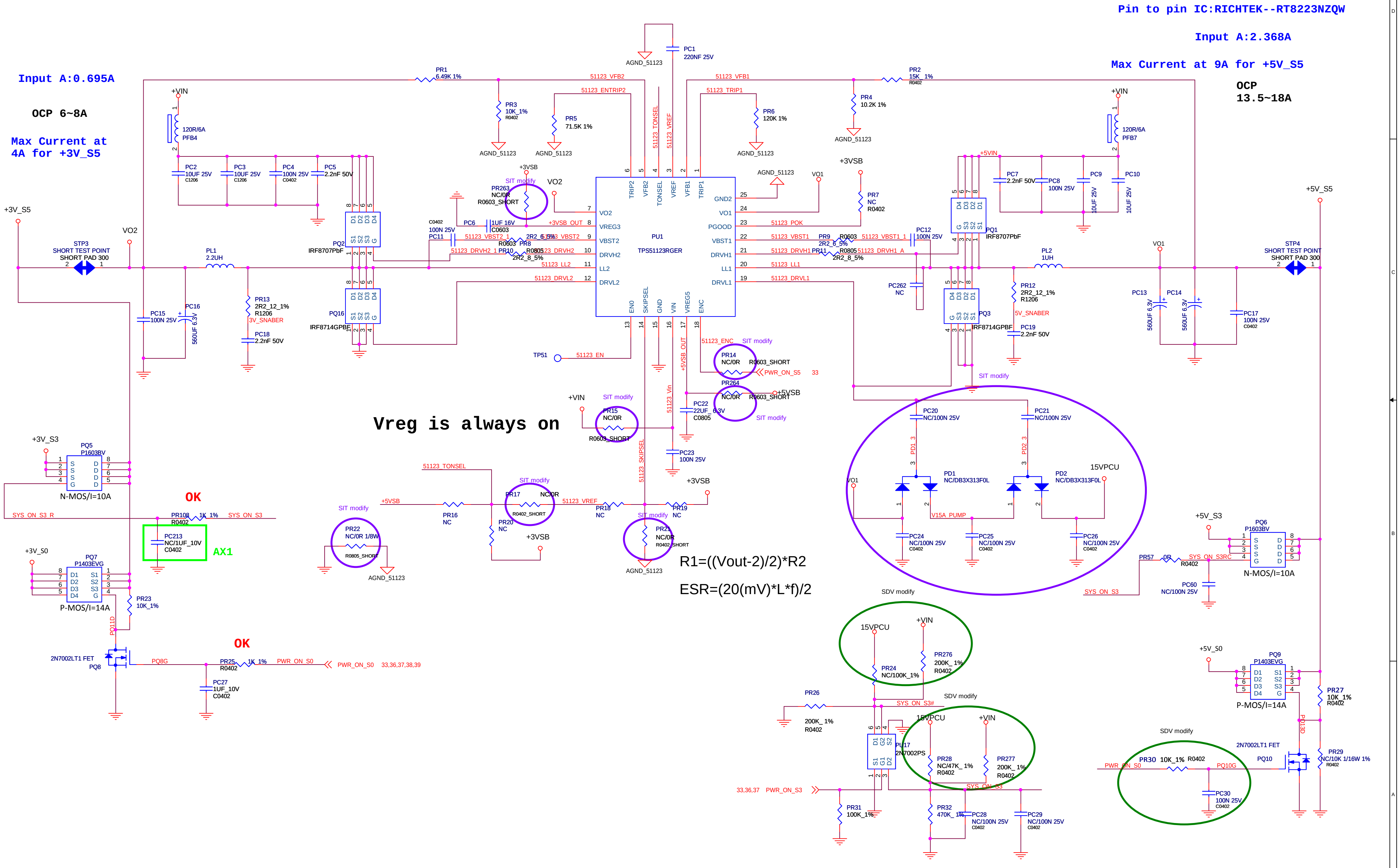
Panel ID

SIZE	PANEL MODEL	ID3	ID2	ID1	ID0
21.5"	AUO M215HW03 V1	1	1	1	1
	LG LM215WF4-TLG1	1	1	0	1
	SEC LTM215HT04-M02	1	0	1	1
	CMI M215HGE-L21	0	1	1	1
20"	AUO M200RW01 V0	1	1	1	0
	LG LM200WD3-TLF1	1	1	0	0
	SEC LTM200KT10-M01,M02	1	0	1	0
	CMI M200FGE-L20	0	1	1	0



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	34 of 45		

SYSTEM +3V_S5/+3V_S3/+3V_S0
+5V_S5/+5V_S3/+5V_S0



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Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
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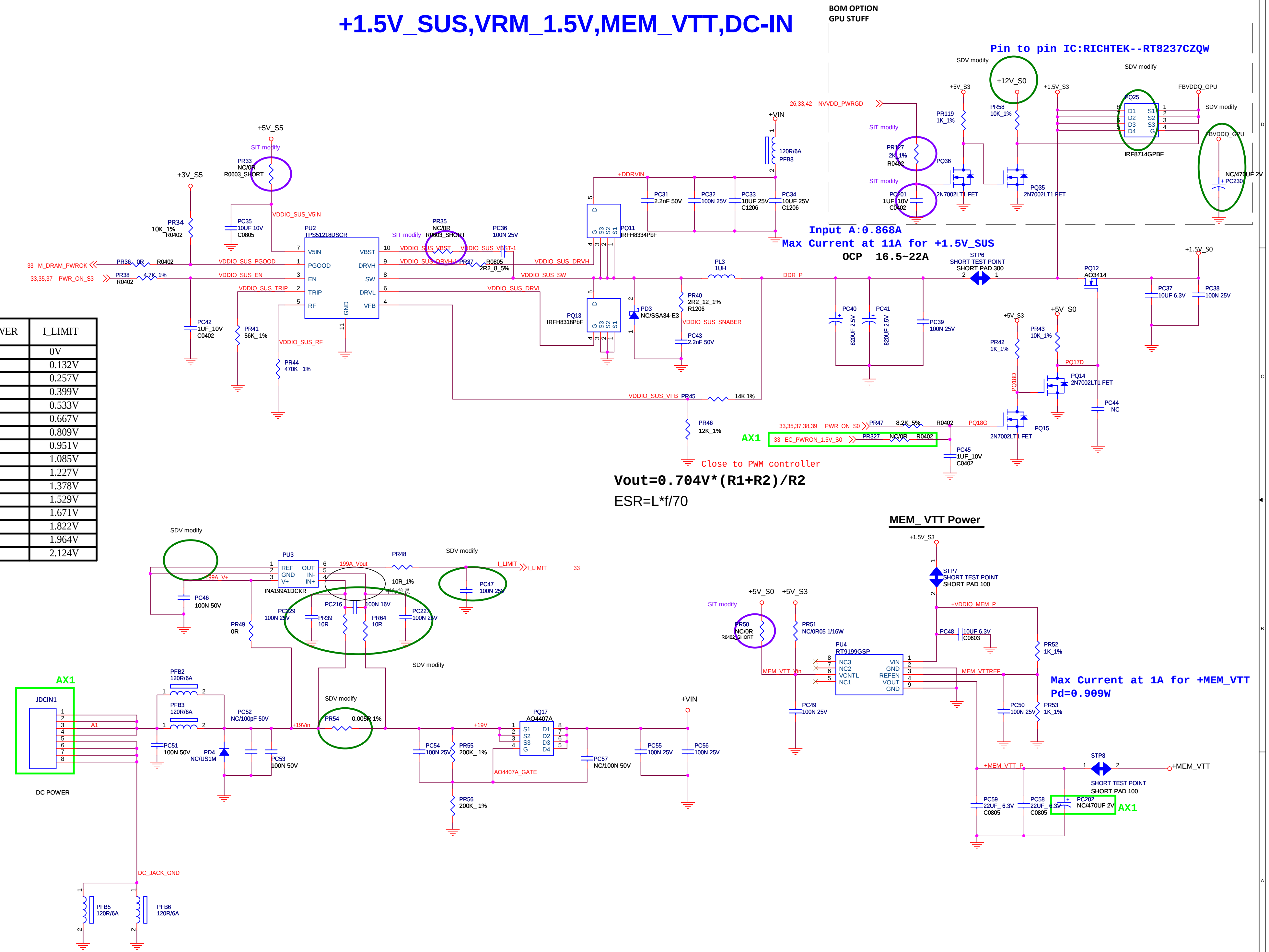
+1.5V_SUS,VRM_1.5V,MEM_VTT,DC-IN



TOTAL POWER	I_LIMIT
0W	0V
10W	0.132V
20W	0.257V
30W	0.399V
40W	0.533V
50W	0.667V
60W	0.809V
70W	0.951V
80W	1.085V
90W	1.227V
100W	1.378V
110W	1.529V
120W	1.671V
130W	1.822V
140W	1.964V
150W	2.124V

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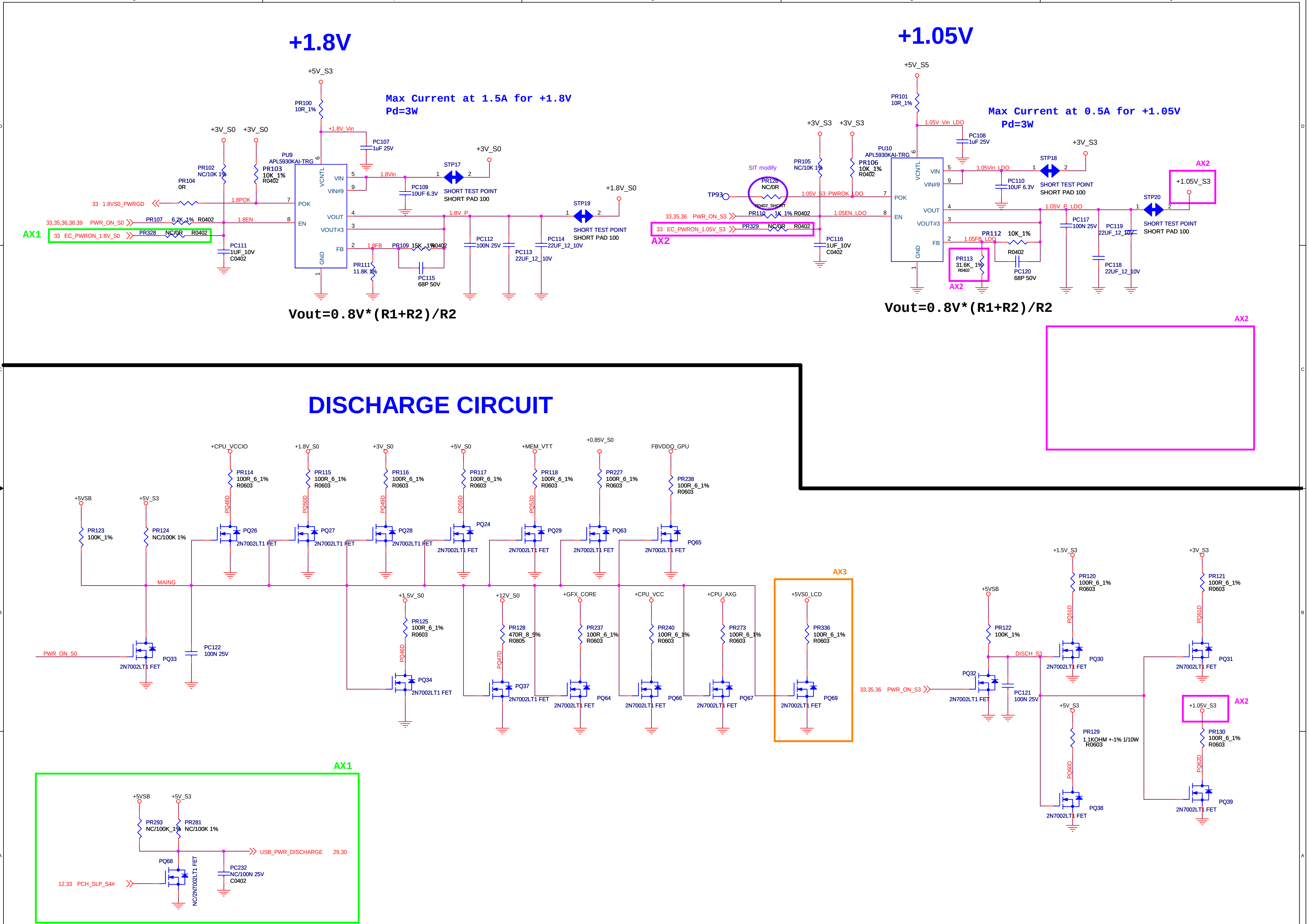
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	36 of 45		



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Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
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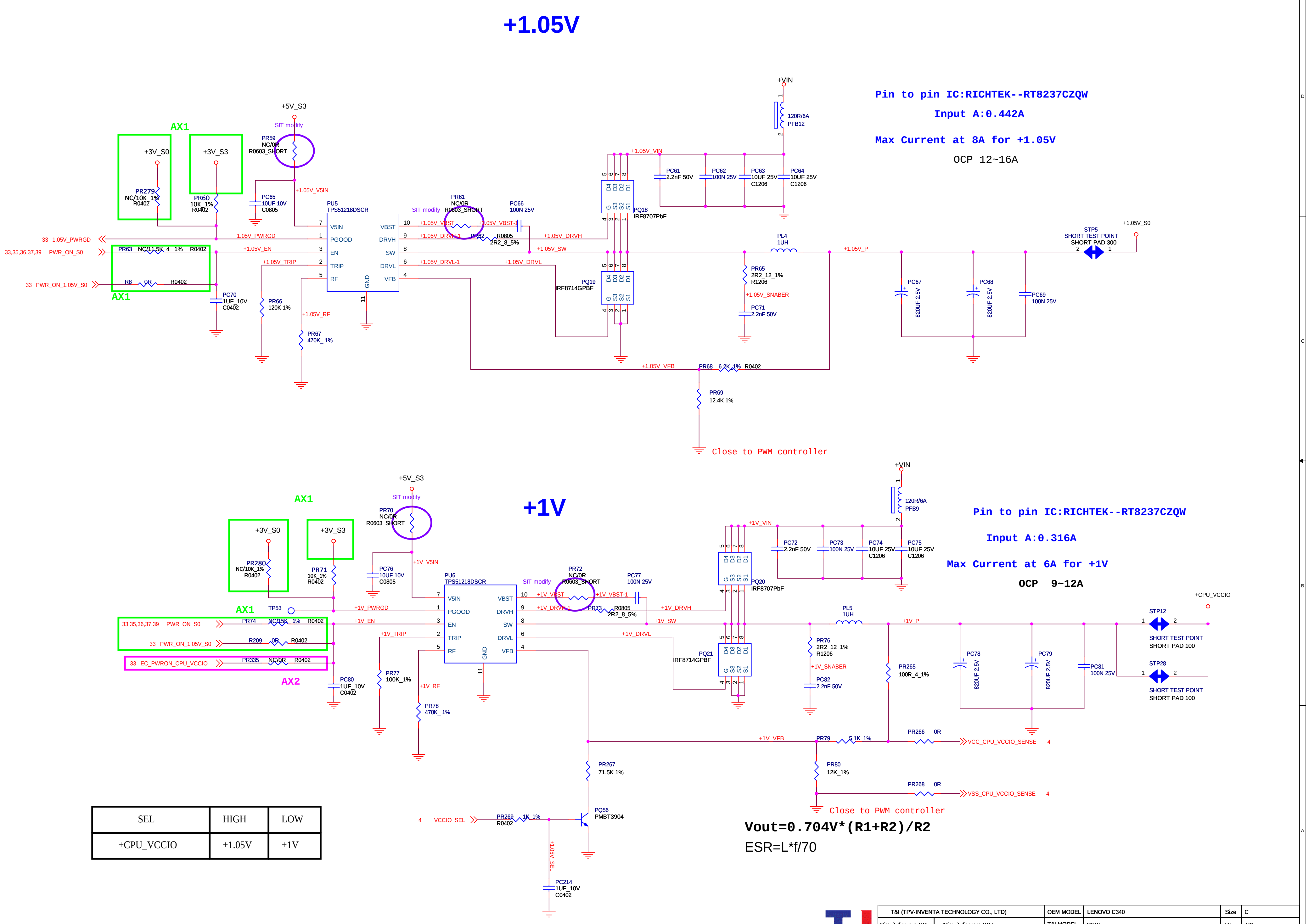
+1.05V



SEL	HIGH	LOW
+CPU_VCCIO	+1.05V	+1V

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Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	38 of 45		

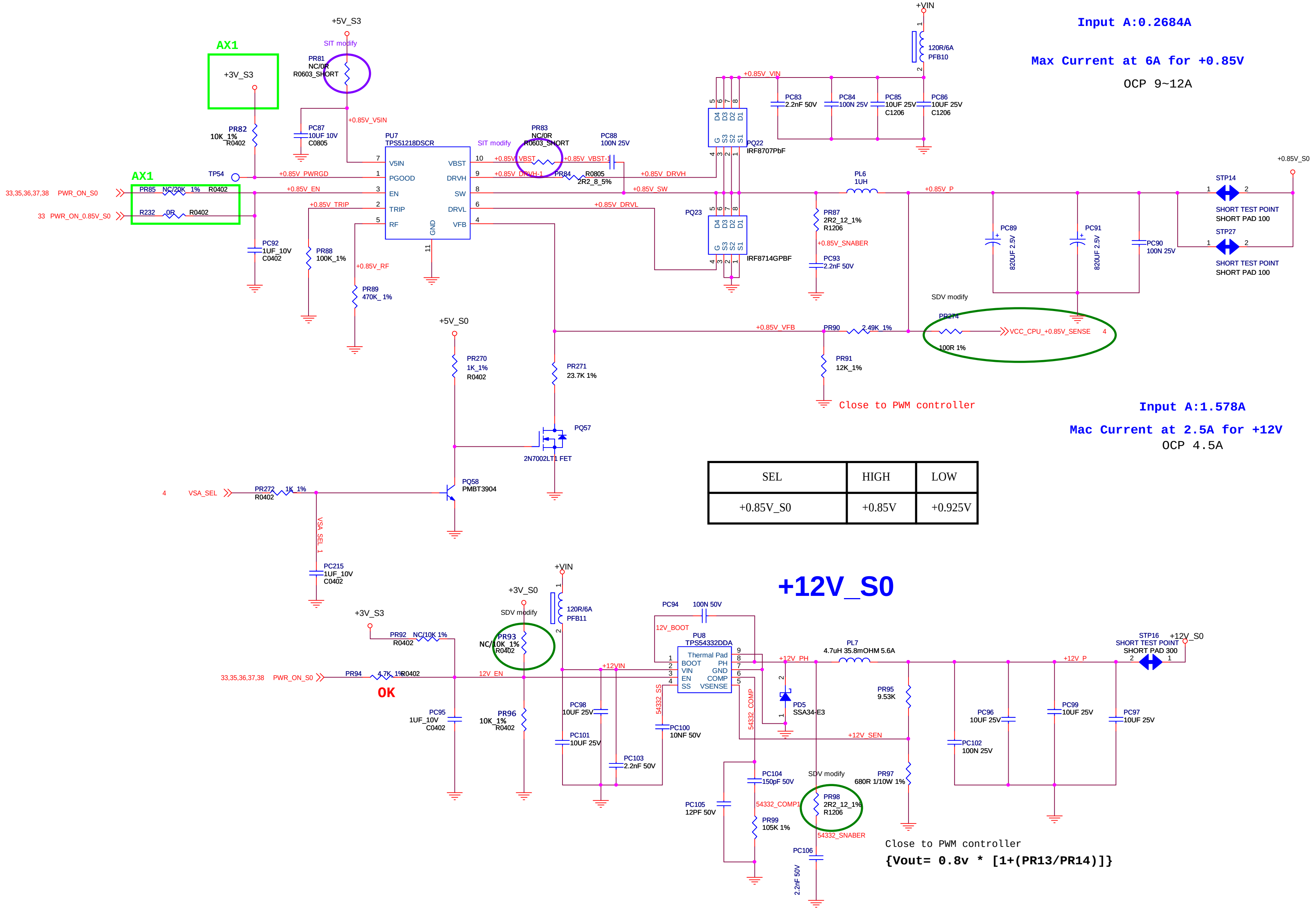
+0.85V

Pin to pin IC:RICHTEK--RT8237CZQW

Input A:0.2684A

Max Current at 6A for +0.85V

OCP 9~12A



Input A:1.578A

Mac Current at 2.5A for +12V

OCP 4.5A

SEL	HIGH	LOW
+0.85V_S0	+0.85V	+0.925V

Close to PWM controller

{Vout= 0.8v * [1+(PR13/PR14)]}

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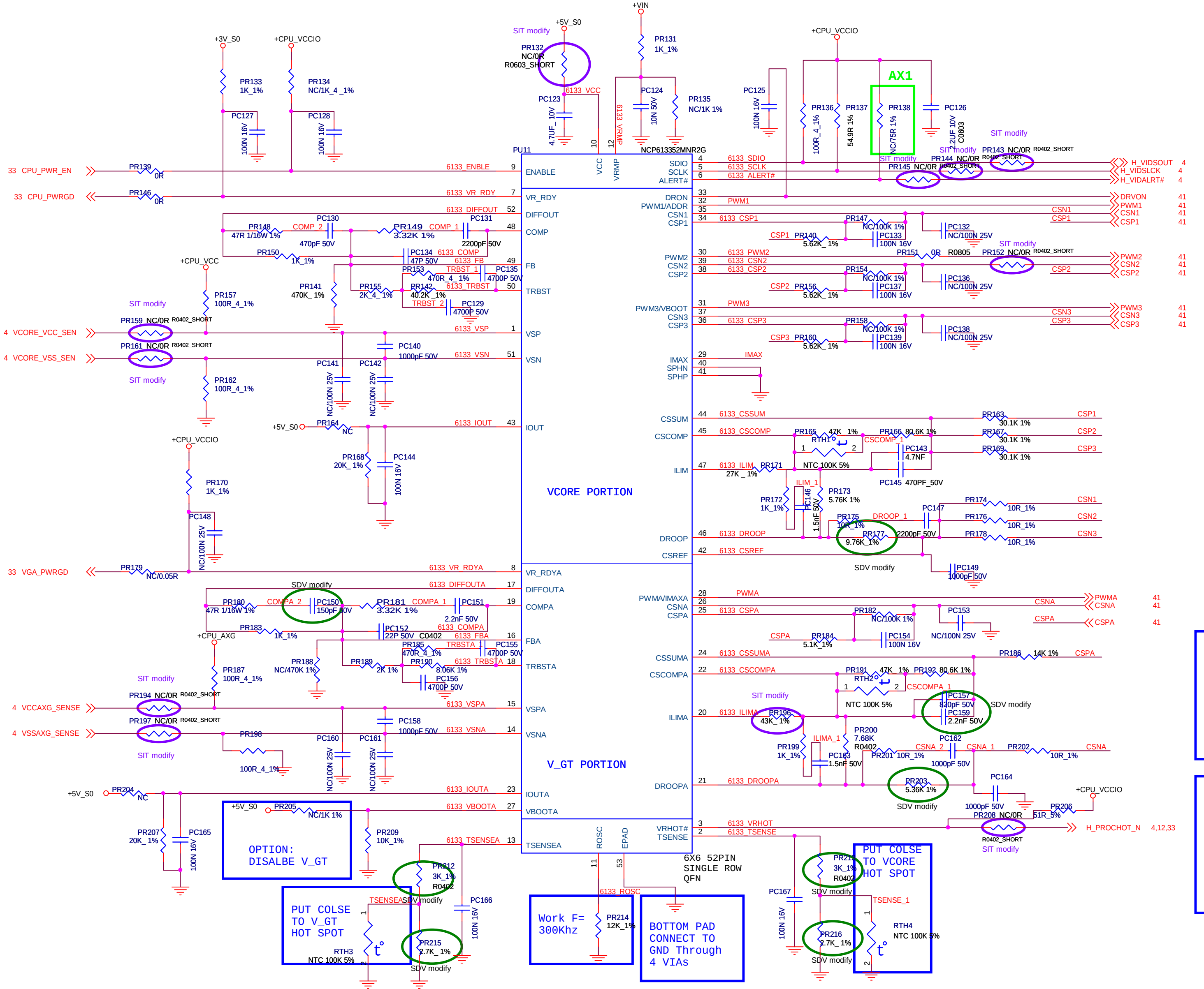
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	39 of 45		

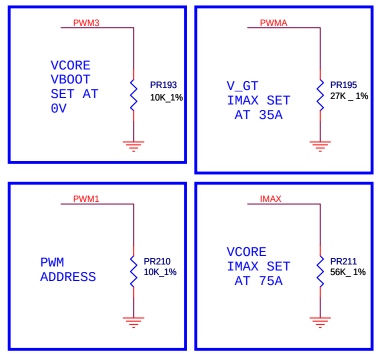


PWM ADDRESS

RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

BOOT VOLTAGE

RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.9V
45K	1V
70K	1.1V
95K	1.2V
125K	1.35V
165K	1.5V
VCC	SHUTDOWN



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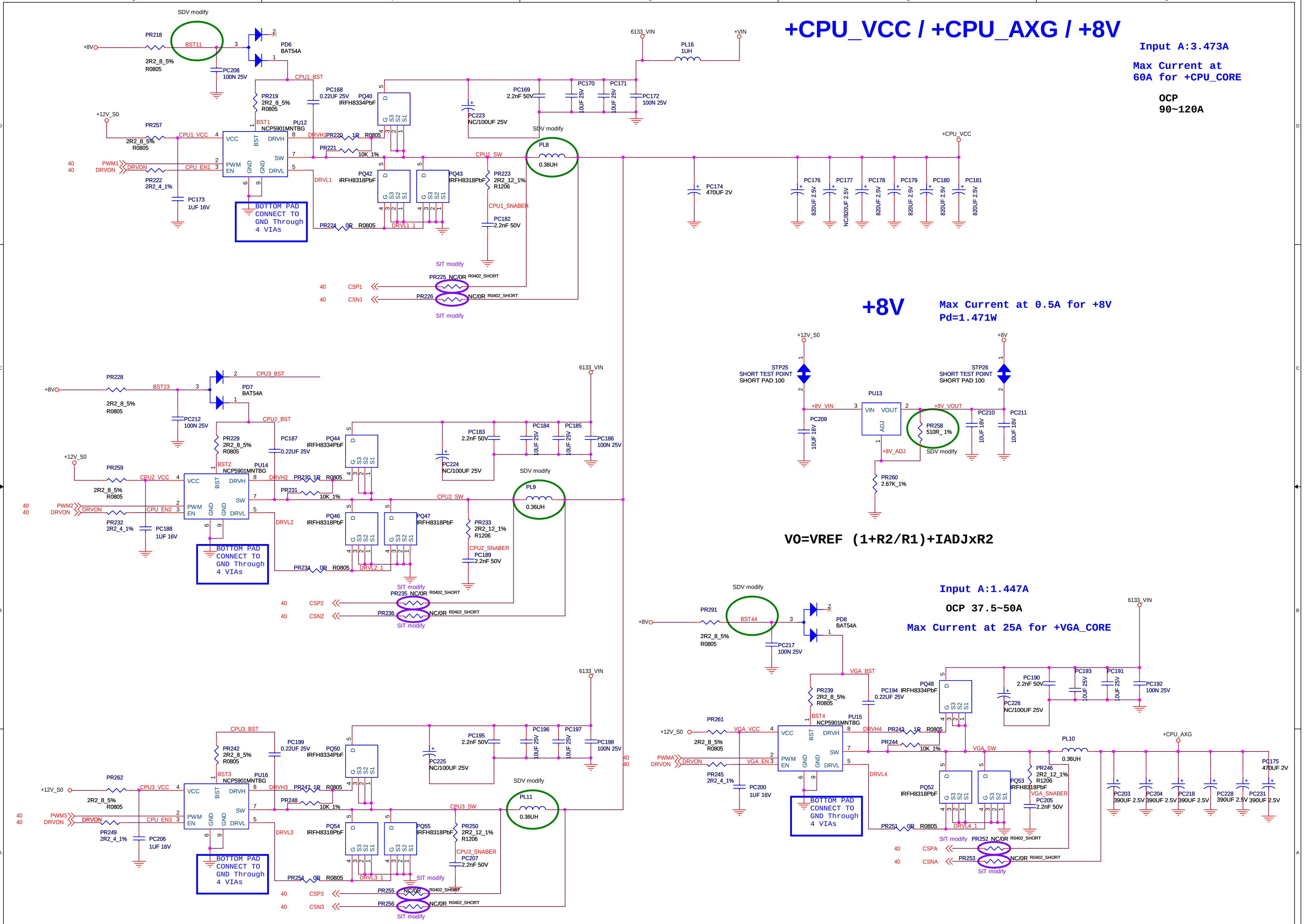
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	40 of 45		



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Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	41 of 45		

+GFX_CORE

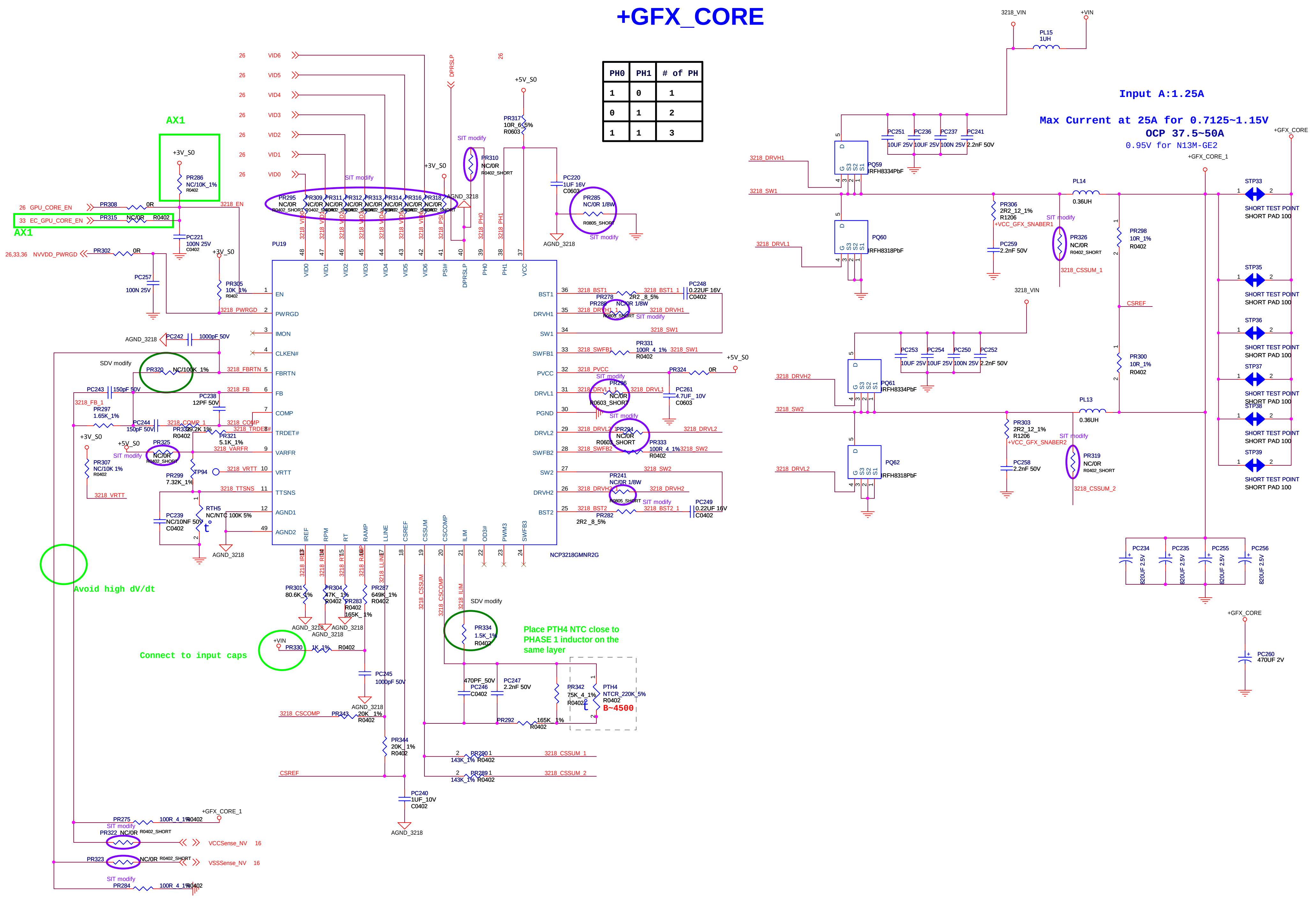
PH0	PH1	# of PH
1	0	1
0	1	2
1	1	3

Input A:1.25A

Max Current at 25A for 0.7125~1.15V

OCP 37.5~50A

0.95V for N13M-GE2



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
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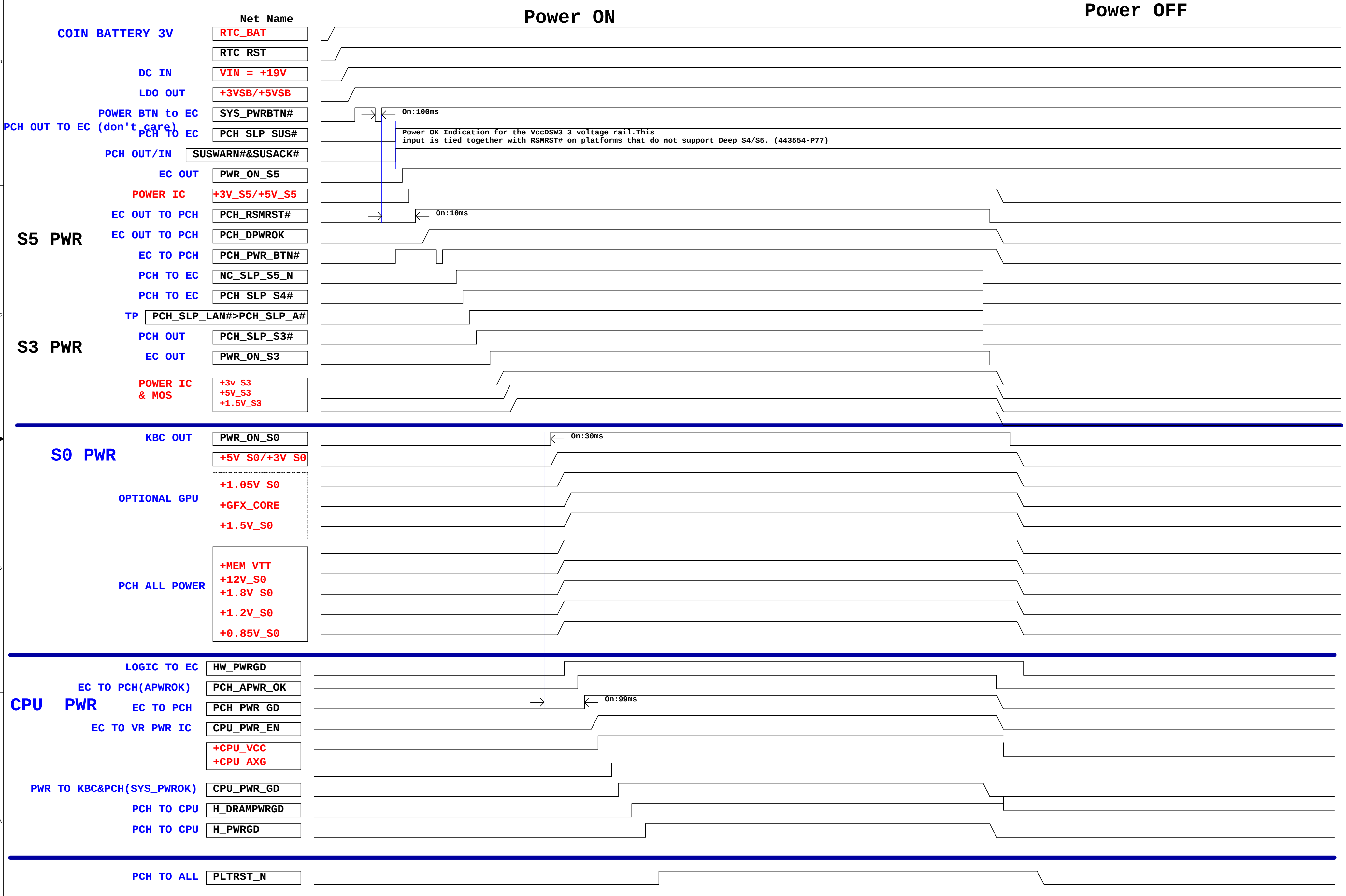
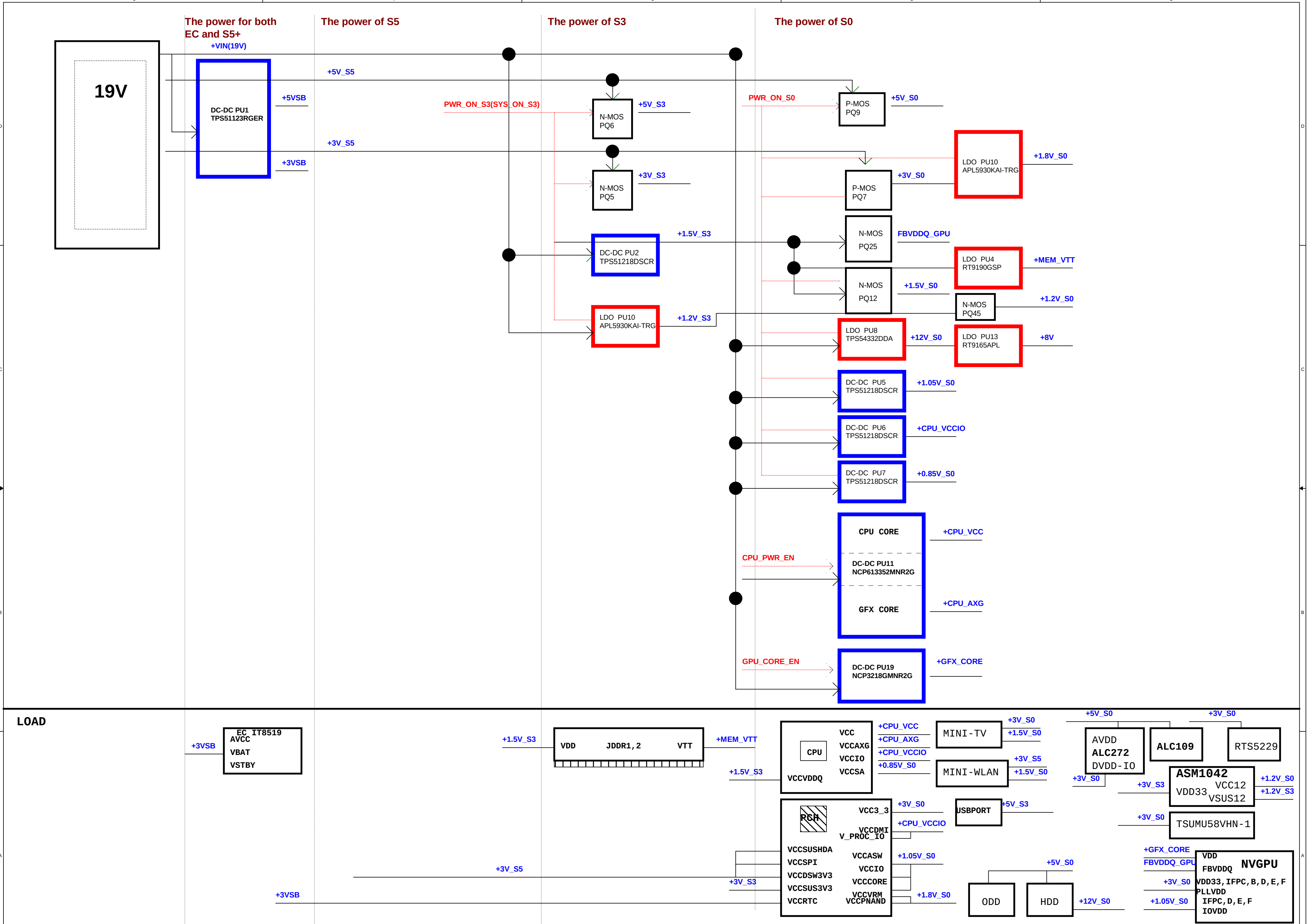
POWER SEQUENCE



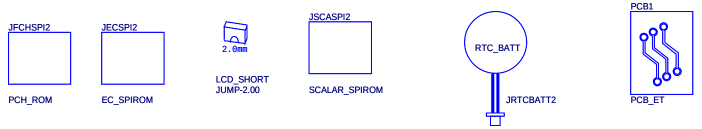
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	43 of 45		



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	LENOVO C340	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	C340	Rev	A01
Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	44 of 45		

AX1 Schematic Modify History

01. PAGE 01. H30,H31 NC NUT PARTS,H32,H33,H34,H35 UPDATE NUT P/N.
02. PAGE 03. U1 INSTALL ,UPDATE P/N.
03. PAGE 12,30. CHANGE POWER NEAME FROM +3V_SPI_ROM TO +3V_SPI FOR SPI ROM
04. PAGE 30. DELETE Q76,C471 FOR +LAN_VDD33 POWER CIRCUIT
05. PAGE 30. RESERVE R464,R465,Q78 FOR +LAN_VDD33 DISCHARGE CIRCUIT
06. PAGE 11. RESERVE R158,R159 FOR BOARD ID, RESERVE R172~174 FOR VRAM ID
07. PAGE 16. ADD C480 10uF C285 4.7uF FOR PEX_IOVDD, ADD C479 4.7uF FOR PEX_IOVDDQ
08. PAGE 17. R311 DEPOP
09. PAGE 24. SWAP GPU_TMDSC_0N/P, CHANGE GPU_SDA CONNECTOR TO U38.R5
11. PAGE 25. CHANGE LB7 VALUE TO 180 Ohm/100MHz, ADD C770 100nF
12. PAGE 31. RESERVE R516
13. PAGE 33. R717 ADD 2.2K FOR CIR_RX
14. PAGE 33. SCREEN_LED# CONNECTION CHANGE FROM U27 PIN 72 TO PIN 85
15. PAGE 16. ADD R352 NC P/N
16. PAGE 38. CORRECT 1.5V_S3 TO +3V_S3 ON PR60,PR71
17. PAGE 39. CORRECT 1.5V_S3 TO +3V_S3 ON PR82
18. PAGE 33. DEL R613 PULL UP FOR EC_SCI#
19. PAGE 01. CHANGE H7~H9 FOOTPRINT.
20. PAGE 01. H20 AND H21 CHANGE FOOTPRINT.
21. PAGE 01. H22 CHANGE FOOTPRINT.
22. PAGE 31. R343 CHANGE PULL HIGH TO +5V_S3
23. PAGE 33. R625 DEPOP FOR PECI NO PULL UP
24. PAGE 10. EC_SCI CHANGE FROM PCH GPIO28 TO GPIO 10
25. PAGE 33. SCREEN_LED# CHANGE CONTROL PIN FROM U27 PIN 72 TO PIN 85
26. PAGE 33. R685 DEPOP FOR NVVDD_PWRGD
27. PAGE 34. R364 CHANGE VALUE FROM 100 Ohm TO 0 Ohm
28. PAGE 34. ADD R461,R462,R463,C671,U11 FOR PANEL EDID
29. PAGE 34. R414 CHANGE VALUE FROM 1K TO 10K FOR SCALA RESET
30. PAGE 34. R439 CHANGE TO +5V_S5 AND Q23 CHANGE FROM 3904 TO 2N7002 FOR FIX PANEL SEQUENCE
31. PAGE 30. ADD R466 W/Z O Ohm AND DEPOP D21 FOR +3V_SPI
32. PAGE 33. ADD EC1~EC4 47pF FOR FUNCTION KEY
33. PAGE 28. ED1~ED4 STUFF AND CHANGE CONNECTOR FROM GND TO AGND
34. PAGE 28. R893 CHANGE VALUE 5.1K TO 7.32K
35. PAGE 28. RESERVE R718,R719 0 Ohm FOR EC_SMBUS
36. PAGE 34. JBL2 CHANGE CONNECTOR FROM 12 PIN(HORIZONTAL) TO 10 PIN(VERTICAL)
37. PAGE 34. JLVDS1 CHANGE TYPE FROM HORIZONTAL TO VERTICAL
38. PAGE 29. SWAP L36~L40 AND L43 FOR LAYOUT
39. PAGE 12. R249 CHANGE VALUE FROM 10K TO 0 Ohm
40. PAGE 38. PR63 NON STUFF, +1.05V_EN ADD R8 W/Z 0 Ohm CONNECTED TO EC PIN 108 FOR GPU POWER SEQUENCE
41. PAGE 38. PR74 NON STUFF, +1V_EN ADD R209 W/Z 0 Ohm CONNECTED TO EC PIN 108 FOR GPU POWER SEQUENCE
42. PAGE 39. PR85 NON STUFF, +0.85V_EN ADD R232 W/Z 0 Ohm CONNECTED TO EC PIN 109 FOR GPU POWER SEQUENCE
43. PAGE 29. C670 SHOULD BE 10pF (BOM WAS 10pF)
44. PAGE 29. C767,C768 CHANGE VALUE FROM 20pF TO 12pF
45. PAGE 34. C650,C651 CHANGE VALUE FROM 10pF TO 18pF
46. PAGE 04. ADD VCC_CPU_+0.85V_SENSE FOR CPU VCCSA_SENSE PIN
47. PAGE 37. 29,30 RESERVE USB_POWER DISCHARGE CIRCUIT BY LENOVO REQUEST.
48. PAGE 05. C36 STUFF 0.1uF FOR FIX DDR RESET GLICH
49. PAGE 33. DEPOP R658,R659 AND DELETE R802,R803 FOR G_SML1_CLK/DATA PULL UP
50. PAGE 34. RESERVE R720 FOR EC_SCAL_BKLT_EN
51. PAGE 04. C28 STUFF 0.1uF FOR SNB_DDR_VREF BY INTEL REQUESET
52. PAGE 04. R2 DEPOP, FOLLOW DEMO BOARD
53. PAGE 29. RESERVE R239 W/Z 0 Ohm FOR USB3 SMI
54. PAGE 30. R703 CHANGE VALUE FROM 4.7K TO 0 Ohm
55. PAGE 33. R653, R655 CHANGE VALUE FROM 10K TO 0 Ohm
56. PAGE 33. DELETE R610, R611 FOR SIGNAL DOUBLE PULL UP
57. PAGE 40. PR138 DEPOP, FOLLOW DEMO BOARD
58. PAGE 28. ADD C470 AND C481 FOR SOLVE AVDD POWER RIPPL
59. PAGE 31. DEPOP EL7 FOR TOUCH SCREEN USB(RESER ONLY)
60. PAGE 30. DEPOP JCRTDB1 FOR ME ISSUE
61. PAGE 33, 36, 37, 42 RESERVE R608, PR327, PR328, PR329, PR335, PR315 FOR POWER SEQUENCE
62. PAGE 01, H13, H27, H28 CHANGE FOOTPRINT(改孔壁吃錫)
63. PAGE 28, JMIC1,JHP1 CHANGE CONNECTOR FROM 6026B0208001(8 PIN) TO 6026B0225201 (6 PIN)
64. PAGE 11, R147 STUFF 10K, R159 NC FOR UMA & GPU_VRAM X 8 SKU, R147 NC, R159 STUFF 10K FOR GPU_VRAM X 4 SKU
65. PAGE 25, DELETE U39 AND R775 CHANGE VALUE FROM 34.8K TO 15K FOR VBIOS AND SYSTEM BIOS COMBINE
    IN JFCHSPI ROM



GPU SKU
B01. PAGE 34. R853,R854 CHANGE VALUE FROM 0 Ohm TO 100 Ohm
B02. PAGE 11. R764 DEPOP
B03. PAGE 11. UMA R764 DEPOP
B04. PAGE 11. UMA R166, R167 DEPOP

UMA SKU
B01. PAGE 34. R851,R852 CHANGE VALUE FROM 0 Ohm TO 100 Ohm
B02. PAGE 11. R764 ADD 0R FOR PCH DVI HPD
B03. PAGE 11. UMA R764 POP 0 Ohm
B04. PAGE 11. UMA R166, R167 STUFF

AX2 Schematic Modify History

01. PAGE 35. RECOVER PR17 0R
02. PAGE 37. +1.2V_S3 CHANGE TO +1.05V_S3. PR113 CHANGE VALUE FROM 20K TO 31.6K FOR
    VOLTAGE SETTING.
    REMOVE PQ45, PQ51, PQ49, PC219 PR86, PR75, PC222 FOR +1.2V_S0 CONTROL CIRCUIT.
    CHANGE PR37 CONNECTION FOR RESERVE +CPU_VCCIO POWER SEQUENCE CONTROL.
03. PAGE 37. CHANGE PR130 CONNECTION FROM +1.2V_S3 TO +1.05V_S3 FOR DISCHARGE CIRCUIT.
04. PAGE 34. RESERVE R416, R417 FOR SCALAR GIOP
05. PAGE 12. R200 CHANGE VALUE FROM 1K TO 10K FOR PCH_WAKE_UP#, BY RENESAS REQUEST
06. PAGE 12. R189 DEPOP AND R547 STUFF 10K FOR PCIE_USB3_CLKREQ#, BY RENESAS REQUEST
07. PAGE 29. R570 AND R571 DEPOP BY RENESAS REQUEST
08. PAGE 29. ADD U50,U51,C896,C907 FOR USB 3.0 LAYOUT SMOOTHLY.

AX3 Schematic Modify History

01. PAGE 11. CHANGE JHPD1 FROM 2PIN TO 3PIN HEADER FOR CLEAR CMOS FUNCTION.
02. PAGE 12. R204 ADD 10K Ohm, JHPD2 FUNCTION CHANGE TO CLEAR PASSWORD.
03. PAGE 34. JLCDSW1 PIN10 CHANGE TO LCD_ID4 AND ADD R370 10K Ohm PULL UP
    FOR 23" PANEL ID USE.
04. PAGE 34. ADD JSCLDB1 3PIN HEADER FOR SCALAR DEBUG ONLY.
05. PAGE 34. R453 CHANGE VALUE FROM 10K TO 27K Ohm FOR FIX PANEL SEQUENCE T1 ISSUE.
06. PAGE 37. ADD PR336 W/Z 100R AND PQ69 FOR +5VS0_LCD DISCHARGE CIRCUIT.
07. PAGE 12. RESERVE DSW POWER FOR PCH,
    CHANGE EC PIN 57 FUNCTION FROM EC_SCAL_BKLT_EN TO DSW3.3_PWR_ON
08. PAGE 31 CHANGE CIR POWER PLAN FROM +3V_S0 TO +3V_S5 FOR SUPPORT CIR WAKE ON S4.
09. PAGE 31 CHANGE CIR POWER PLAN FROM +3V_S0 TO +3V_S5 FOR SUPPORT CIR WAKE ON S4.
10. PAGE 31 ADD R355, R924, C485, PQ71, PQ70, R511 FOR RESERVE SCREEN LED BREATH CIRCUIT.
11. PAGE 31 R504 REPLACE TO SHORT PAD FOR SOLVE POWER DROP ISSUE.
12. PAGE 31 RESERVE R534~R539 FOR PCIE LPC DEBUG PORT.
13. PAGE 31 ADD R540 AND DEPOP R348, R349, R693, Q66, Q67 FOR SCREEN LED.

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Key Component	COVER SHEET	PCB NAME	6050A2512501	remark	<remark>
Date	Monday, April 23, 2012	Sheet	45 of 45		