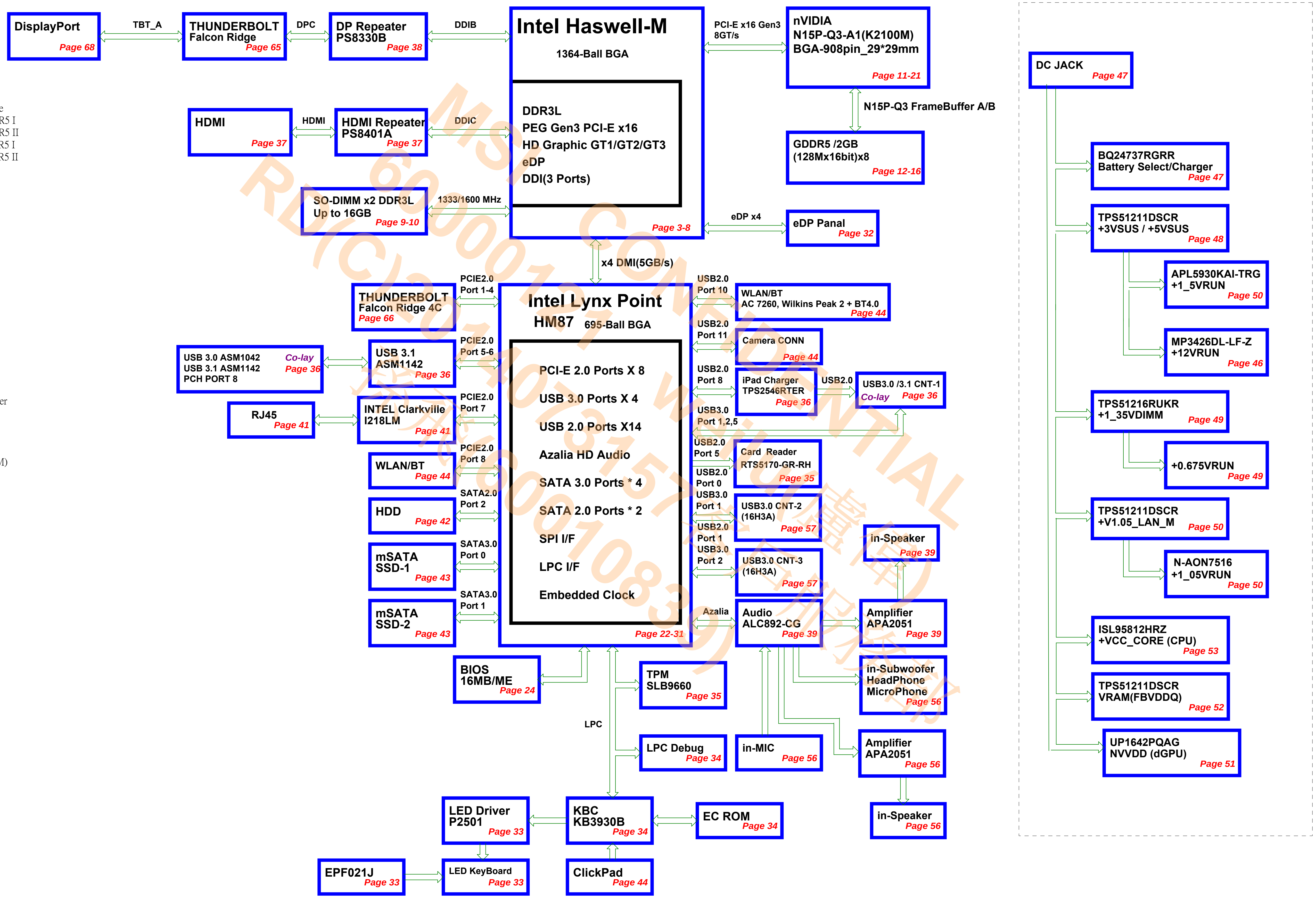
MS-16H3 Ver:0A

Wednesday, June 25, 2014

Shark Bay Mobile



MICRO-STAR INT'L CO.,LTD.

Title: Block Diagram

Document Number: MS-16H3

Rev: 1.0

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	DIMM_ON
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUN_ON
+VCC_CORE	1.8V Core Voltage for Processor	EC_ALLSYSPG
+1_05VRUN	1.05V rail for Processor	RUN_ON
NVVDD	V Core Voltage for nVIDIA dGPU	NVVDD_EN
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	FBVDDQ_ON
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	NVVDD_EN

POWER STATES

SIGNAL / STATE	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on and +V*SUS always keep high

Net Naming Conventions

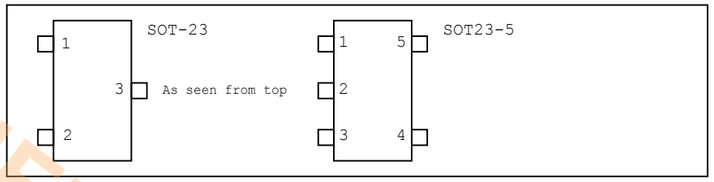
Suffix

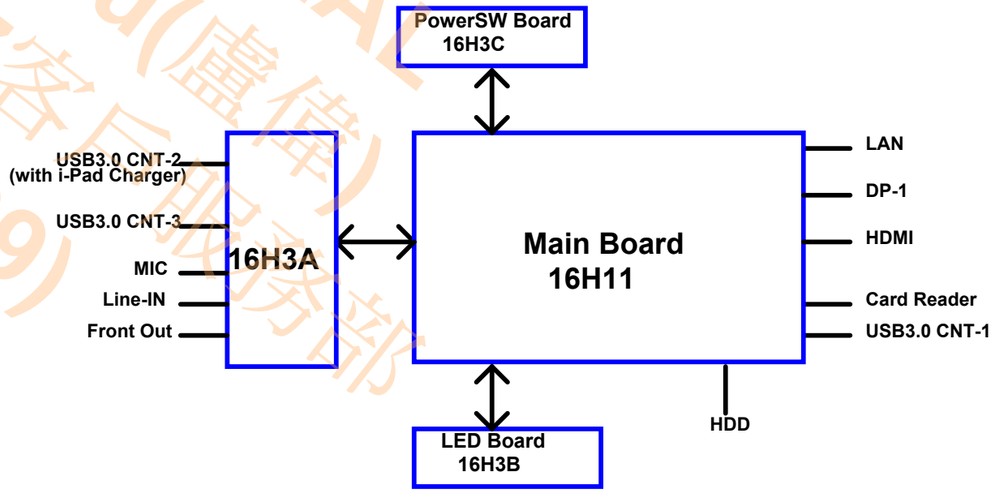
\# = Active Low Signal

Prefix

H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)
FB = DGPU VRAM
VIAxxx = Like Test Point, but using VIA.

PCB Footprints





msi	MICRO-STAR INT'L CO.,LTD.
Title	Platform
Size	Document Number: MS-16H3 — Rev: 1.0
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Haswell (DMI,PEG,FDI)

PEG_RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils

U1A — HASWELL_BGA_E

25 DMI_TXN0	AB2	DMI_RXN0	DMI
25 DMI_TXN1	AB3	DMI_RXN1	
25 DMI_TXN2	AC3	DMI_RXN2	
25 DMI_TXN3	AC1	DMI_RXN3	
25 DMI_TXP0	AB1	DMI_RXP0	
25 DMI_TXP1	AB4	DMI_RXP1	
25 DMI_TXP2	AC4	DMI_RXP2	
25 DMI_TXP3	AC2	DMI_RXP3	
25 DMI_RXN0	AF2	DMI_TXN0	
25 DMI_RXN1	AF4	DMI_TXN1	
25 DMI_RXN2	AG4	DMI_TXN2	
25 DMI_RXN3	AG2	DMI_TXN3	
25 DMI_RXP0	AF1	DMI_TXP0	
25 DMI_RXP1	AF3	DMI_TXP1	
25 DMI_RXP2	AG3	DMI_TXP2	
25 DMI_RXP3	AG1	DMI_TXP3	
25 FDI_CSYNC	F11	FDI_CSYNC	FDI
25 FDI_INT	F12	DISP_INT	

PEG_RCOMP AH6 PEG_COMP R252 24.9R1%0402 +VCCIOA_OUT

PEG_RXN0	E10	PEG_RXN0	11
PEG_RXN1	C10	PEG_RXN1	11
PEG_RXN2	B10	PEG_RXN2	11
PEG_RXN3	E9	PEG_RXN3	11
PEG_RXN4	D9	PEG_RXN4	11
PEG_RXN5	B9	PEG_RXN5	11
PEG_RXN6	L5	PEG_RXN6	11
PEG_RXN7	L2	PEG_RXN7	11
PEG_RXN8	M4	PEG_RXN8	11
PEG_RXN9	L4	PEG_RXN9	11
PEG_RXN10	M2	PEG_RXN10	11
PEG_RXN11	V5	PEG_RXN11	11
PEG_RXN12	V4	PEG_RXN12	11
PEG_RXN13	V1	PEG_RXN13	11
PEG_RXN14	Y3	PEG_RXN14	11
PEG_RXN15	Y2	PEG_RXN15	11
PEG_RXP0	F10	PEG_RXP0	11
PEG_RXP1	D10	PEG_RXP1	11
PEG_RXP2	A10	PEG_RXP2	11
PEG_RXP3	F9	PEG_RXP3	11
PEG_RXP4	C9	PEG_RXP4	11
PEG_RXP5	A9	PEG_RXP5	11
PEG_RXP6	M5	PEG_RXP6	11
PEG_RXP7	L1	PEG_RXP7	11
PEG_RXP8	M3	PEG_RXP8	11
PEG_RXP9	L3	PEG_RXP9	11
PEG_RXP10	M1	PEG_RXP10	11
PEG_RXP11	Y5	PEG_RXP11	11
PEG_RXP12	V3	PEG_RXP12	11
PEG_RXP13	V2	PEG_RXP13	11
PEG_RXP14	Y4	PEG_RXP14	11
PEG_RXP15	Y1	PEG_RXP15	11
PEG_TXN0	B6	PEG_TXN0	11
PEG_TXN1	C5	PEG_TXN1	11
PEG_TXN2	E6	PEG_TXN2	11
PEG_TXN3	D4	PEG_TXN3	11
PEG_TXN4	G4	PEG_TXN4	11
PEG_TXN5	E3	PEG_TXN5	11
PEG_TXN6	J5	PEG_TXN6	11
PEG_TXN7	G3	PEG_TXN7	11
PEG_TXN8	J3	PEG_TXN8	11
PEG_TXN9	J2	PEG_TXN9	11
PEG_TXN10	T6	PEG_TXN10	11
PEG_TXN11	R6	PEG_TXN11	11
PEG_TXN12	R2	PEG_TXN12	11
PEG_TXN13	R4	PEG_TXN13	11
PEG_TXN14	T4	PEG_TXN14	11
PEG_TXN15	T1	PEG_TXN15	11
PEG_TXP0	C6	PEG_TXP0	11
PEG_TXP1	B5	PEG_TXP1	11
PEG_TXP2	D6	PEG_TXP2	11
PEG_TXP3	E4	PEG_TXP3	11
PEG_TXP4	G5	PEG_TXP4	11
PEG_TXP5	E2	PEG_TXP5	11
PEG_TXP6	J6	PEG_TXP6	11
PEG_TXP7	G2	PEG_TXP7	11
PEG_TXP8	J4	PEG_TXP8	11
PEG_TXP9	J1	PEG_TXP9	11
PEG_TXP10	T5	PEG_TXP10	11
PEG_TXP11	R5	PEG_TXP11	11
PEG_TXP12	R1	PEG_TXP12	11
PEG_TXP13	R3	PEG_TXP13	11
PEG_TXP14	T3	PEG_TXP14	11
PEG_TXP15	T2	PEG_TXP15	11

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Haswell (CLK,MISC,JTAG)

SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil

U1B — HASWELL_BGA_E

C51	PROC_DETECT	MISC	
VIA_H_CATERR#	G50 CATERR	THERMAL	
34 H_PECI	G51 PECI		
H_PROCHOT#_R	E50 PROCHOT		
27 H_THRMTRIP#	D53 THERMTRIP		
25 H_PM_SYNC	D52 PM_SYNC	PWR	
27 H_CPUPWRGD	F50 PWRGOOD		
PM_DRAM_PWRGD_R	AP48 SM_DRAMPWROK		
27 PCH_PLTRST_CPU	L54 PLTRSTIN		
23 CLK_DPN	AC6 DPLL_REF_CLKN	CLOCK	
23 CLK_DPP	AE6 DPLL_REF_CLKP		
23 CLK_DP_SSCN	V6 SSC_DPLL_REF_CLKN		
23 CLK_DP_SSCP	Y6 SSC_DPLL_REF_CLKP		
23 CLK_EXP#	AB6 BCLKN		
23 CLK_EXP	AA6 BCLKP		

SM_RCOMP0	BB51	SM_RCOMP0_JNC	R277 100R1%0402 GND
SM_RCOMP1	BB53	SM_RCOMP1_JNC	R269 75R1%0402
SM_RCOMP2	BB52	SM_RCOMP2_JNC	R276 100R1%0402
SM_DRAMRST	BE51	CPUDRAMRST#	
DDR3			
PRDY	N53		
PREQ	N52	VIA_XDP_PREQ#	
TCK	N54	XDP_TCLK	
TMS	M51	VIA_XDP_TMS	
TRST	M53	XDP_TRST#	
TDI	N49	VIA_XDP_TDI	
TDO	M49	VIA_XDP_TDO	
DBR	F53	VIA_XDP_DBRESET#	
JTAG			
BPM#0	R51		
BPM#1	R50		
BPM#2	P49		
BPM#3	N50		
BPM#4	R49		
BPM#5	P53		
BPM#6	U51		
BPM#7	P51		

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R237 10KR1%0402 — GND

H_CPUPWRGD EC14 X_C15p50N0402 GND

EC Sink current 2 mA

+VCCIO_OUT
R236 681R1%0402
34 EC_PROCHOT# — R235 56R0402 — H_PROCHOT#_R
53 IMVP_PROCHOT# — 1 — 2 — JNC7 X_0402

47P close PWM

+1_35VDIMM
R22 1.8K1%0402
25 PM_DRAM_PWRGD — R20 0R1%0402 — PM_DRAM_PWRGD_R
R21 3.3KR1%0402
GND

Not Support Deep S3

1.35V

1K on CRB , 0R on DG

R,C Close SO-DIMM

9,10 DDR3_DRAMRST# — R29 0R1%0402 — CPUDRAMRST#
EC1 X_C0.1u50X70402
GND

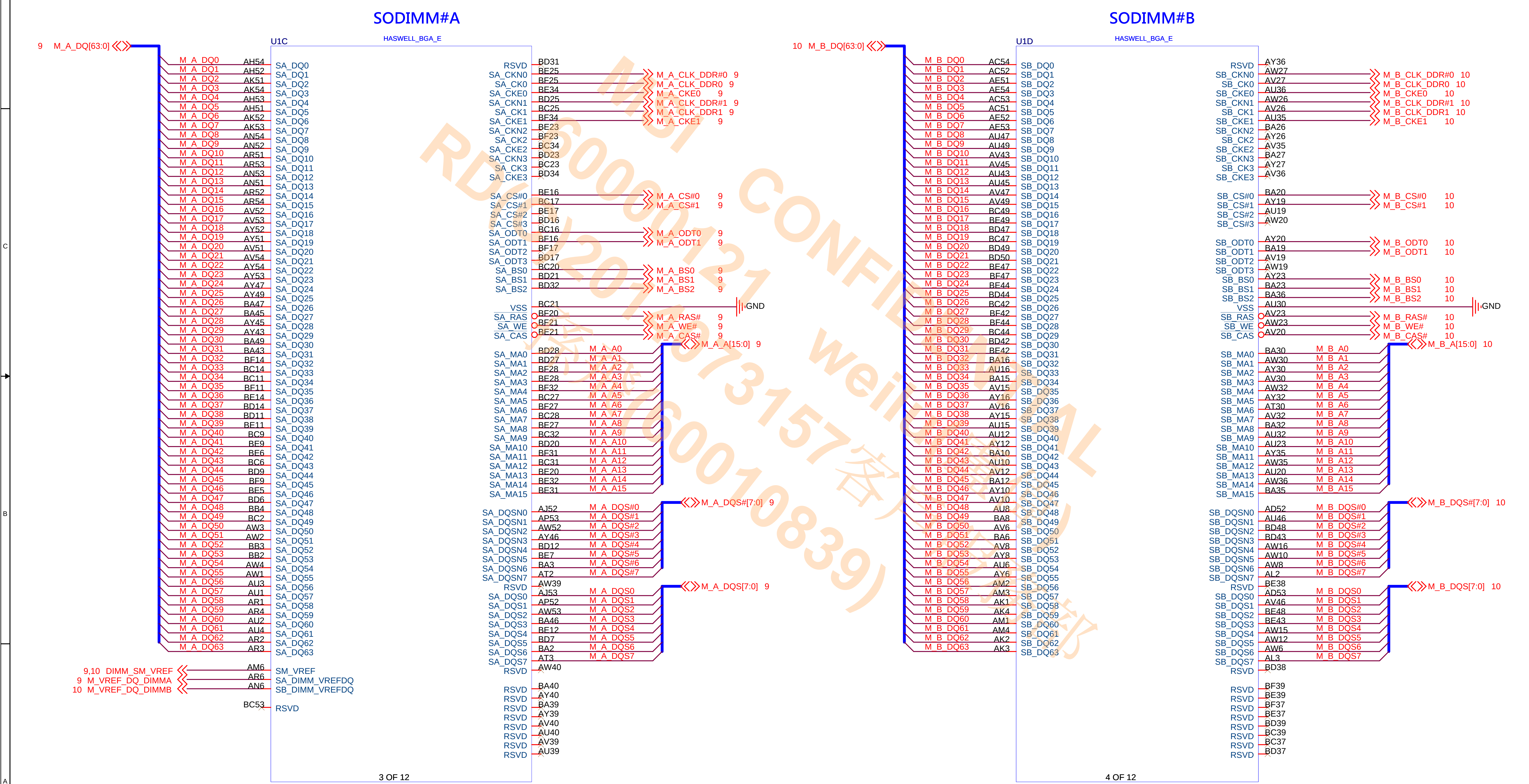
p.11 479493_479493_SharkBay_HSW_ext_rev2.0.pdf
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals, PREQ# and PRDY# signals signals have adequate internal bias resistances to support the removal of the external pull up and pull down on the board when debug is no longer needed.

XDP_TCLK R17 51R1%0402
XDP_TRST# R18 51R1%0402
GND

MICRO-STAR INT'L CO.,LTD.

Title	CPU-1 (Host Bus)		
Size	Document Number MS-16H3		Rev 1.0
Date:	Wednesday, June 25, 2014	Sheet 3 of 69	

Haswell (DDR3L)

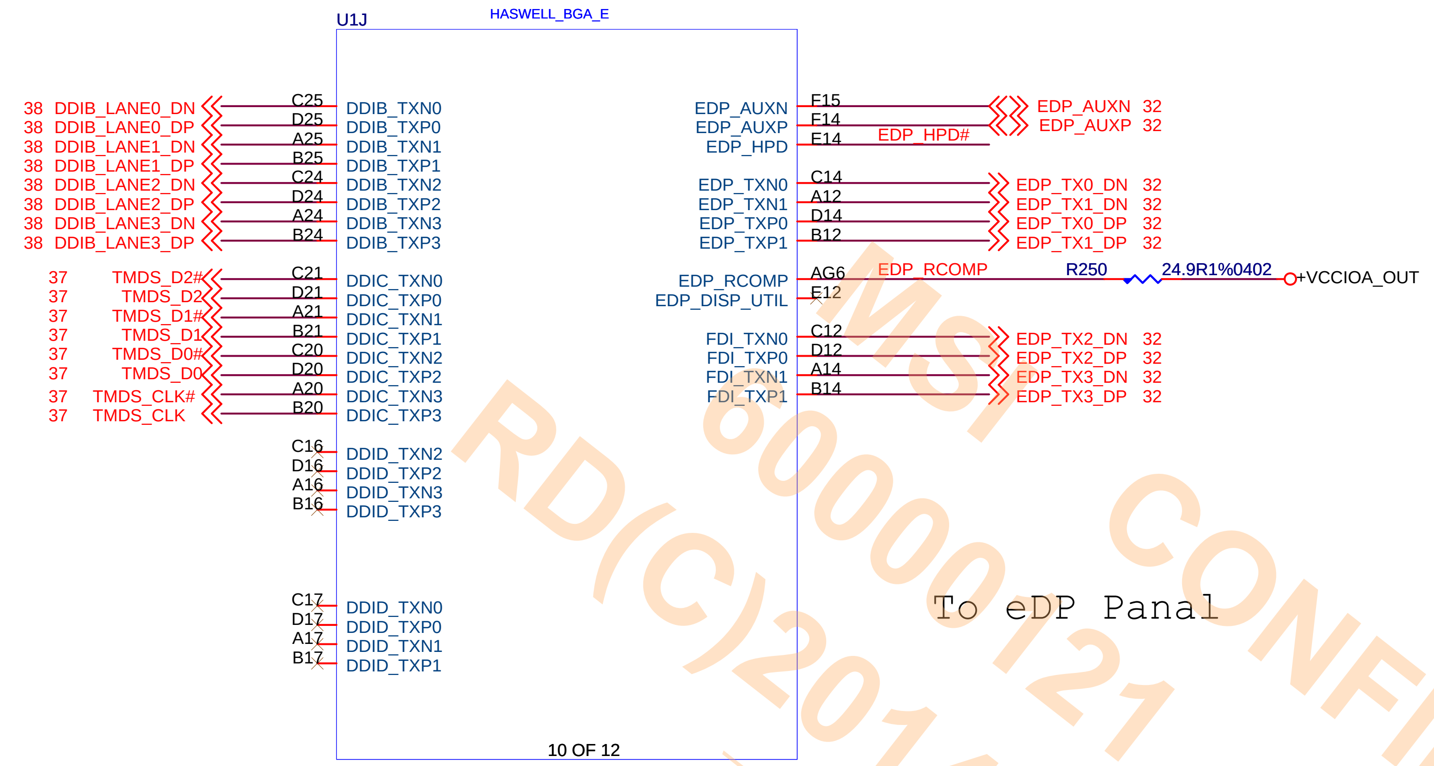


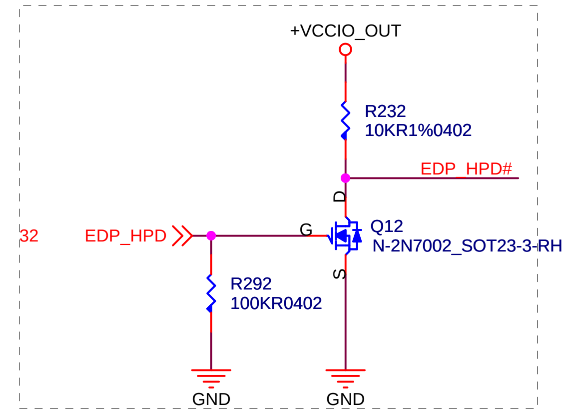
msi	MICRO-STAR INT'L CO.,LTD.	
Title	CPU-2 (DDR3L)	
Size	Document Number MS-16H3	Rev 1.0
Date: Wednesday, June 25, 2014	Sheet 4 of 69	

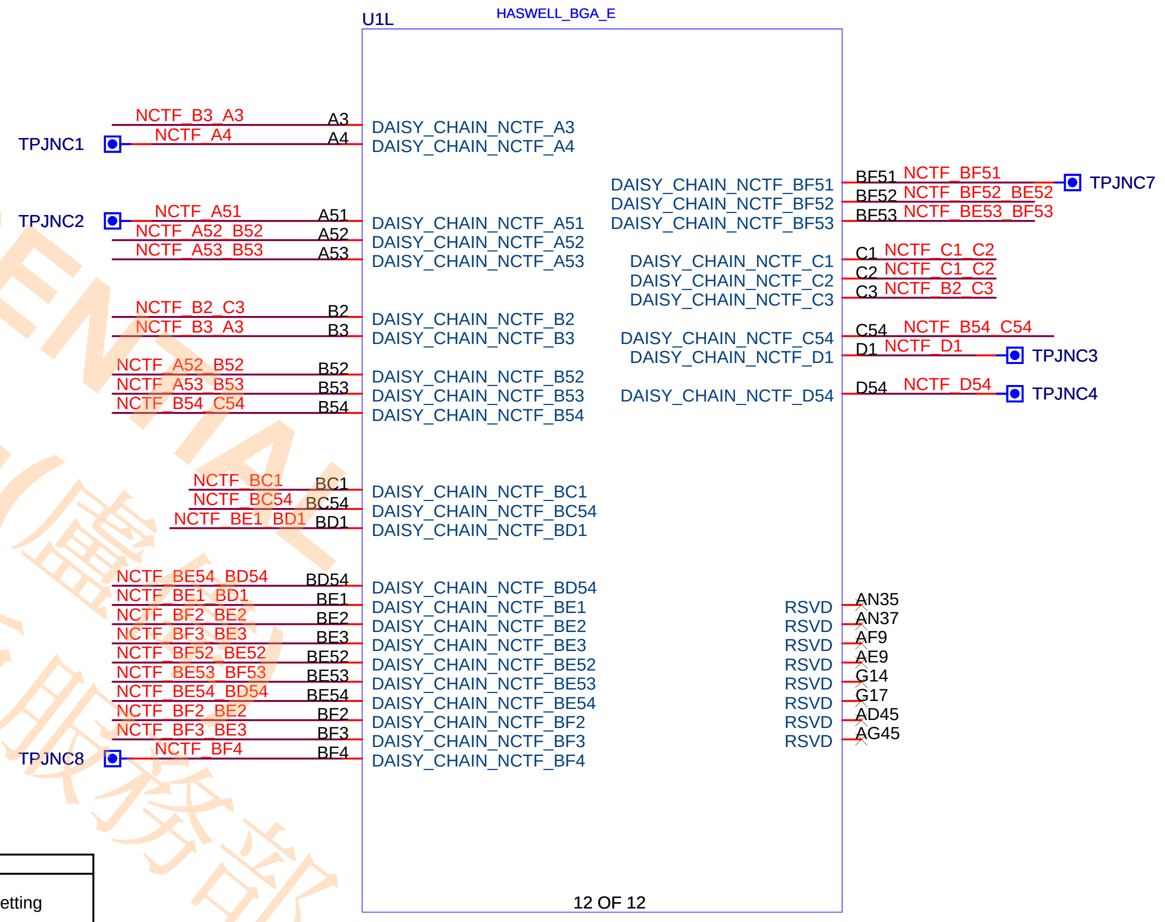
Display/Reserved

DP

HDMI


U1J HASWELL_BGA_E
38 DDIB_LANE0_DN C25 DDIB_TXN0
38 DDIB_LANE0_DP D25 DDIB_TXP0
38 DDIB_LANE1_DN A25 DDIB_TXN1
38 DDIB_LANE1_DP B25 DDIB_TXP1
38 DDIB_LANE2_DN C24 DDIB_TXN2
38 DDIB_LANE2_DP D24 DDIB_TXP2
38 DDIB_LANE3_DN A24 DDIB_TXN3
38 DDIB_LANE3_DP B24 DDIB_TXP3
37 TMDS_D2# C21 DDIC_TXN0
37 TMDS_D2 D21 DDIC_TXP0
37 TMDS_D1# A21 DDIC_TXN1
37 TMDS_D1 B21 DDIC_TXP1
37 TMDS_D0# C20 DDIC_TXN2
37 TMDS_D0 D20 DDIC_TXP2
37 TMDS_CLK# A20 DDIC_TXN3
37 TMDS_CLK B20 DDIC_TXP3
C16 DDID_TXN2
D16 DDID_TXP2
A16 DDID_TXN3
B16 DDID_TXP3
C17 DDID_TXN0
D17 DDID_TXP0
A17 DDID_TXN1
B17 DDID_TXP1
EDP_AUXN F15 EDP_AUXN 32
EDP_AUXP F14 EDP_AUXP 32
EDP_HPD E14 EDP_HPD#
EDP_TXN0 C14 EDP_TX0_DN 32
EDP_TXN1 A12 EDP_TX1_DN 32
EDP_TXP0 D14 EDP_TX0_DP 32
EDP_TXP1 B12 EDP_TX1_DP 32
EDP_RCOMP AG6 EDP_RCOMP R250 24.9R1%0402 +VCCIOA_OUT
EDP_DISP_UTIL E12
FDI_TXN0 C12 EDP_TX2_DN 32
FDI_TXP0 D12 EDP_TX2_DP 32
FDI_TXN1 A14 EDP_TX3_DN 32
FDI_TXP1 B14 EDP_TX3_DP 32
10 OF 12
To eDP Panal

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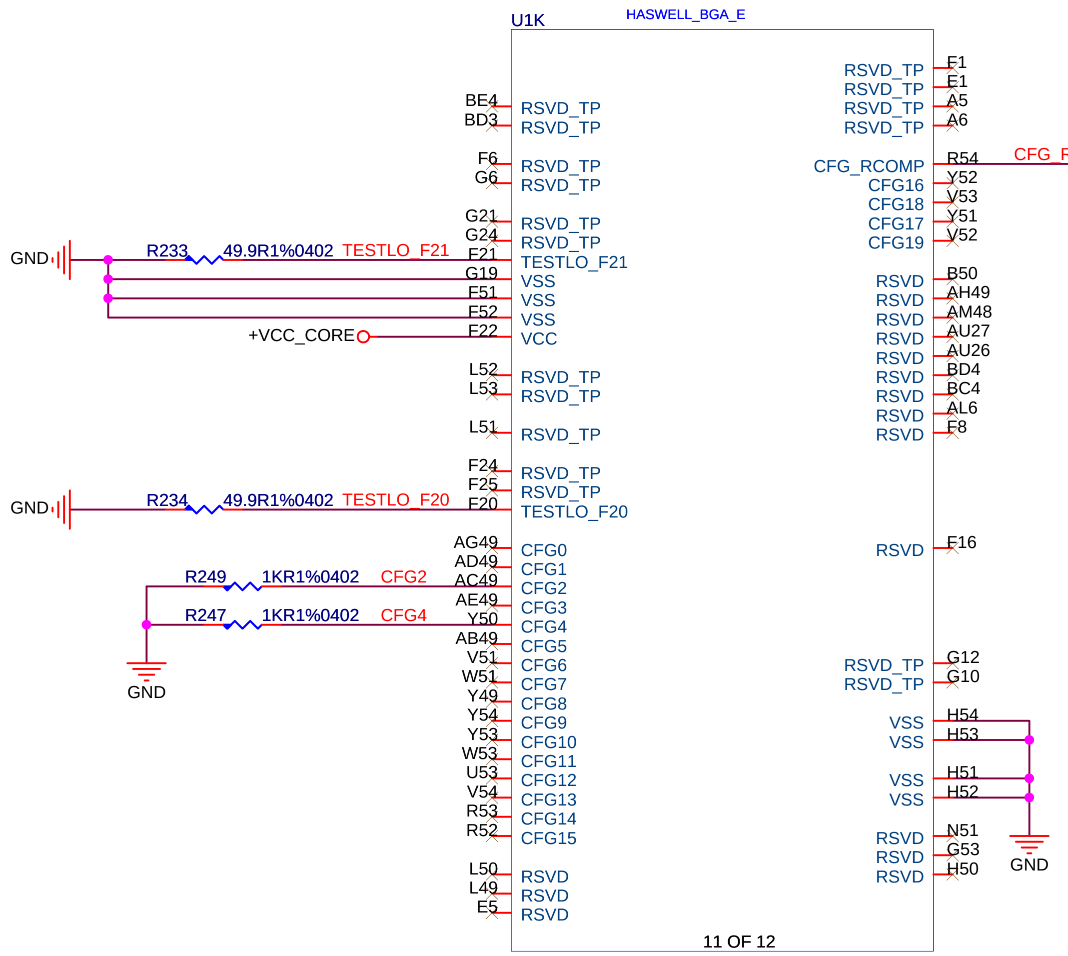
NCTF_B3_A3 A3 DAISY_CHAIN_NCTF_A3
TPJNC1 NCTF_A4 A4 DAISY_CHAIN_NCTF_A4
TPJNC2 NCTF_A51 A51 DAISY_CHAIN_NCTF_A51
NCTF_A52_B52 A52 DAISY_CHAIN_NCTF_A52
NCTF_A53_B53 A53 DAISY_CHAIN_NCTF_A53
NCTF_B2_C3 B2 DAISY_CHAIN_NCTF_B2
NCTF_B3_A3 B3 DAISY_CHAIN_NCTF_B3
NCTF_A52_B52 B52 DAISY_CHAIN_NCTF_B52
NCTF_A53_B53 B53 DAISY_CHAIN_NCTF_B53
NCTF_B54_C54 B54 DAISY_CHAIN_NCTF_B54
NCTF_BC1 BC1 DAISY_CHAIN_NCTF_BC1
NCTF_BC54 BC54 DAISY_CHAIN_NCTF_BC54
NCTF_BE1_BD1 BD1 DAISY_CHAIN_NCTF_BD1
NCTF_BE54_BD54 BD54 DAISY_CHAIN_NCTF_BD54
NCTF_BE1_BD1 BE1 DAISY_CHAIN_NCTF_BE1
NCTF_BF2_BE2 BE2 DAISY_CHAIN_NCTF_BE2
NCTF_BF3_BE3 BE3 DAISY_CHAIN_NCTF_BE3
NCTF_BF52_BE52 BE52 DAISY_CHAIN_NCTF_BE52
NCTF_BE53_BF53 BE53 DAISY_CHAIN_NCTF_BE53
NCTF_BE54_BD54 BE54 DAISY_CHAIN_NCTF_BE54
NCTF_BF2_BE2 BF2 DAISY_CHAIN_NCTF_BF2
NCTF_BF3_BE3 BF3 DAISY_CHAIN_NCTF_BF3
TPJNC8 NCTF_BF4 BF4 DAISY_CHAIN_NCTF_BF4
DAISY_CHAIN_NCTF_BF51 BF51 NCTF_BF51 TPJNC7
DAISY_CHAIN_NCTF_BF52 BF52 NCTF_BF52_BE52
DAISY_CHAIN_NCTF_BF53 BF53 NCTF_BE53_BF53
DAISY_CHAIN_NCTF_C1 C1 NCTF_C1_C2
DAISY_CHAIN_NCTF_C2 C2 NCTF_C1_C2
DAISY_CHAIN_NCTF_C3 C3 NCTF_B2_C3
DAISY_CHAIN_NCTF_C54 C54 NCTF_B54_C54
DAISY_CHAIN_NCTF_D1 D1 NCTF_D1 TPJNC3
DAISY_CHAIN_NCTF_D54 D54 NCTF_D54 TPJNC4
RSVD AN35
RSVD AN37
RSVD AF9
RSVD AE9
RSVD G14
RSVD G17
RSVD AD45
RSVD AG45
12 OF 12


U1K HASWELL_BGA_E
BE4 RSVD_TP
BD3 RSVD_TP
F6 RSVD_TP
G6 RSVD_TP
G21 RSVD_TP
G24 RSVD_TP
GND R233 49.9R1%0402 TESTLO_F21 F21 TESTLO_F21
G19 VSS
F51 VSS
F52 VSS
+VCC_CORE F22 VCC
L52 RSVD_TP
L53 RSVD_TP
L51 RSVD_TP
F24 RSVD_TP
F25 RSVD_TP
GND R234 49.9R1%0402 TESTLO_F20 F20 TESTLO_F20
AG49 CFG0
AD49 CFG1
R249 1KR1%0402 CFG2 AC49 CFG2
AE49 CFG3
R247 1KR1%0402 CFG4 Y50 CFG4
AB49 CFG5
V51 CFG6
W51 CFG7
Y49 CFG8
Y54 CFG9
Y53 CFG10
W53 CFG11
U53 CFG12
V54 CFG13
R53 CFG14
R52 CFG15
L50 RSVD
L49 RSVD
E5 RSVD
GND
RSVD_TP F1
RSVD_TP E1
RSVD_TP A5
RSVD_TP A6
CFG_RCOMP R54 CFG_RCOMP R19 49.9R1%0402 GND
CFG16 Y52
CFG18 V53
CFG17 Y51
CFG19 V52
RSVD B50
RSVD AH49
RSVD AM48
RSVD AU27
RSVD AU26
RSVD BD4
RSVD BC4
RSVD AL6
RSVD F8
RSVD F16
RSVD_TP G12
RSVD_TP G10
VSS H54
VSS H53
VSS H51
VSS H52
GND
RSVD N51
RSVD G53
RSVD H50
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PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

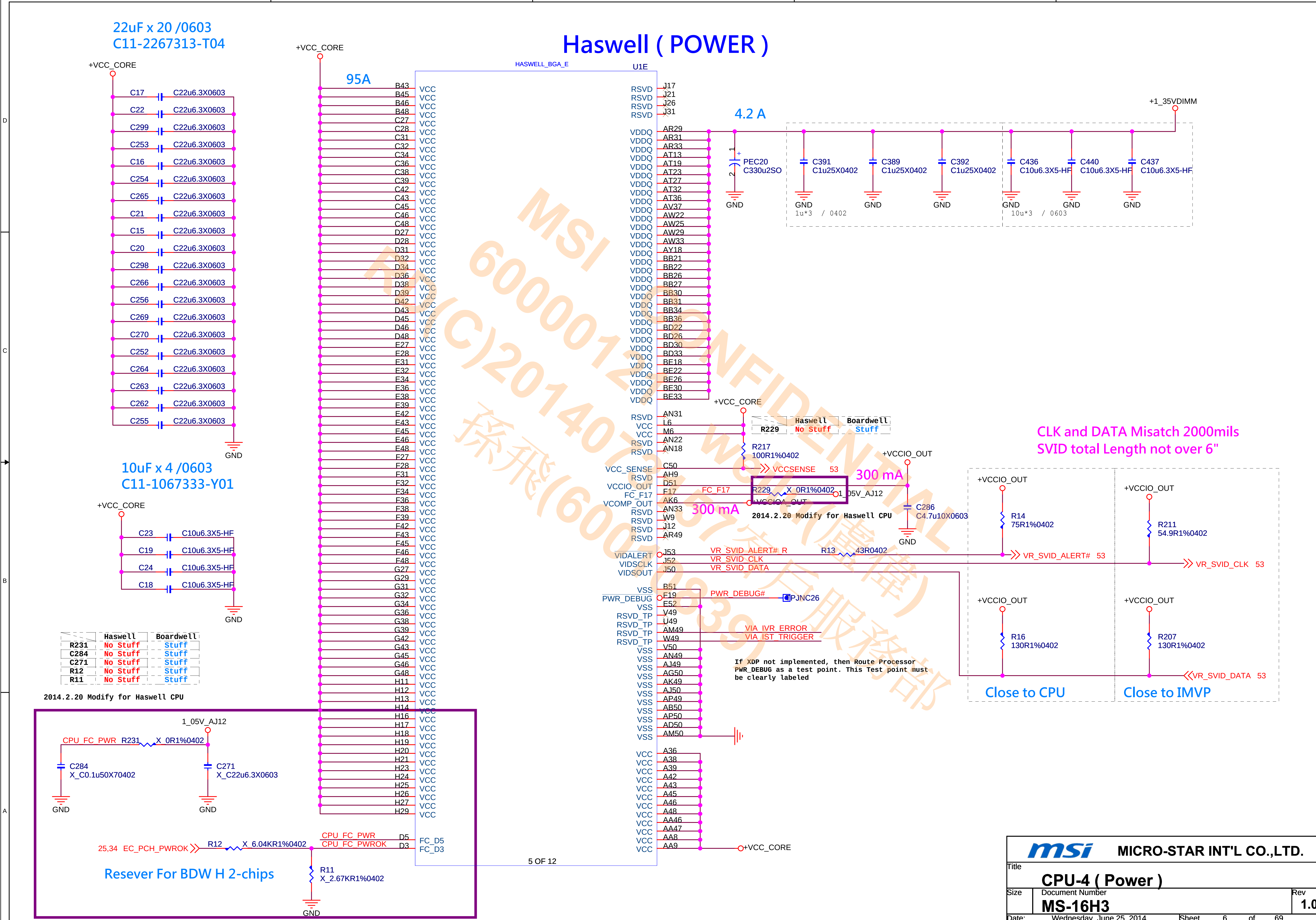
MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Haswell (POWER)



	Haswell	Boardwell
R229	No Stuff	Stuff

	Haswell	Boardwell
R231	No Stuff	Stuff
C284	No Stuff	Stuff
C271	No Stuff	Stuff
R12	No Stuff	Stuff
R11	No Stuff	Stuff

2014.2.20 Modify for Haswell CPU

MICRO-STAR INT'L CO.,LTD.

Title: CPU-4 (Power)

Size | Document Number: MS-16H3 | Rev: 1.0

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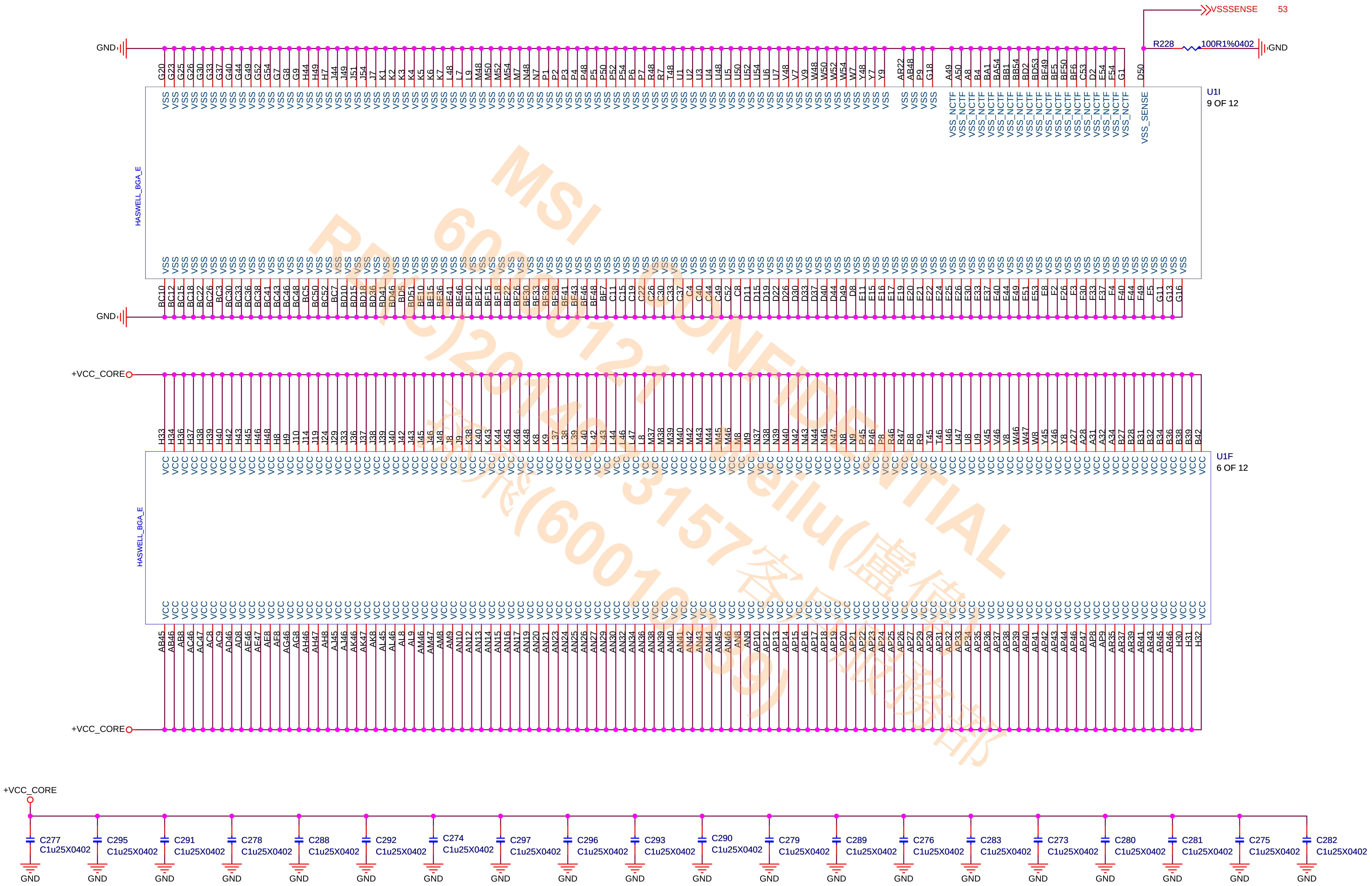
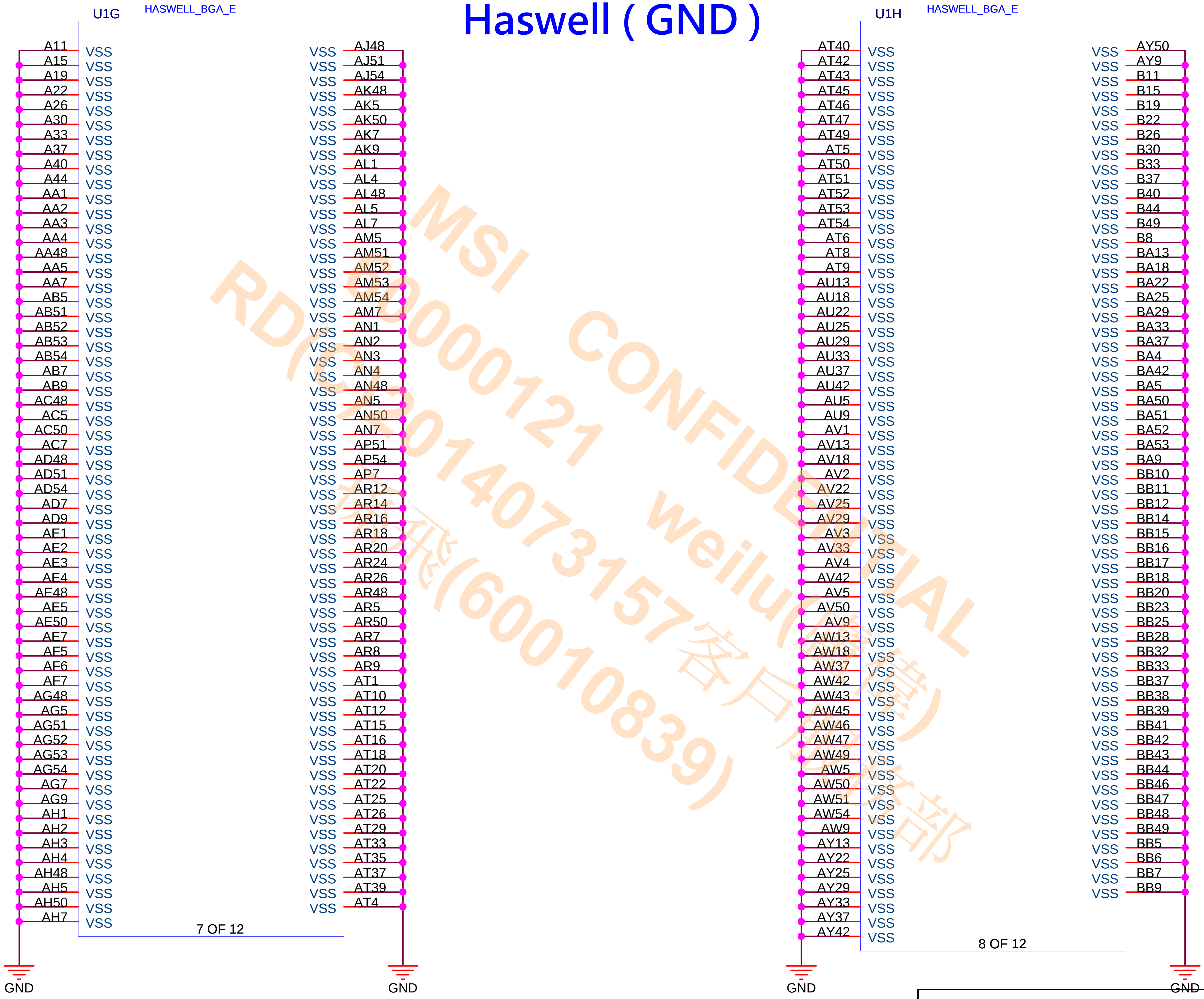
Haswell (Power & GND)



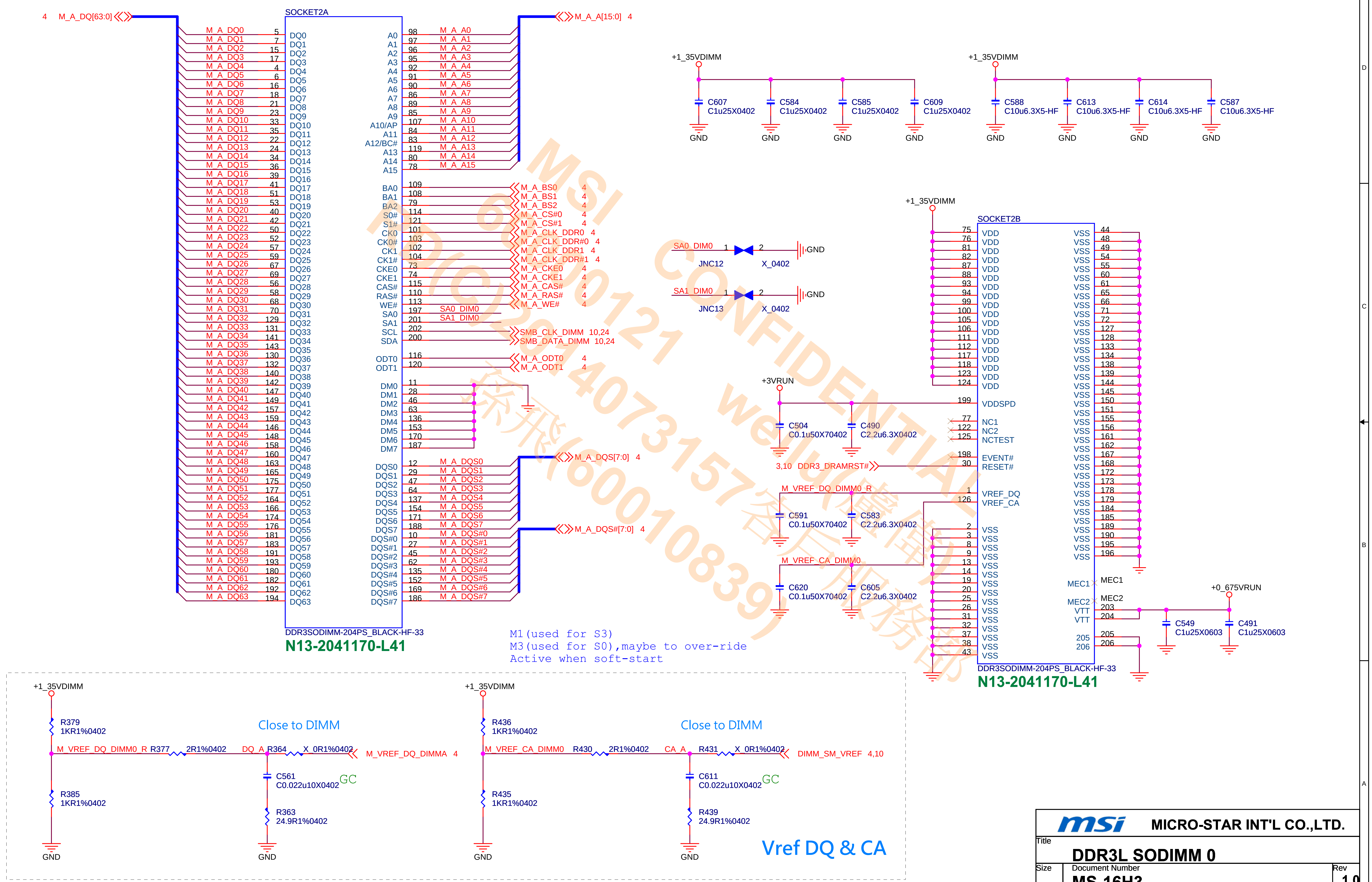
msi	MICRO-STAR INT'L CO.,LTD.	
Title	CPU-6 (Power & GND)	
Size	Document Number MS-16H3	Rev 1.0
Date: Wednesday, June 25, 2014	Sheet 7 of 69	

Haswell (GND)



msi	MICRO-STAR INT'L CO.,LTD.
Title	CPU-5 (GND)
Size / Document Number	MS-16H3 — Rev 1.0
Date: Wednesday, June 25, 2014	Sheet 8 of 69

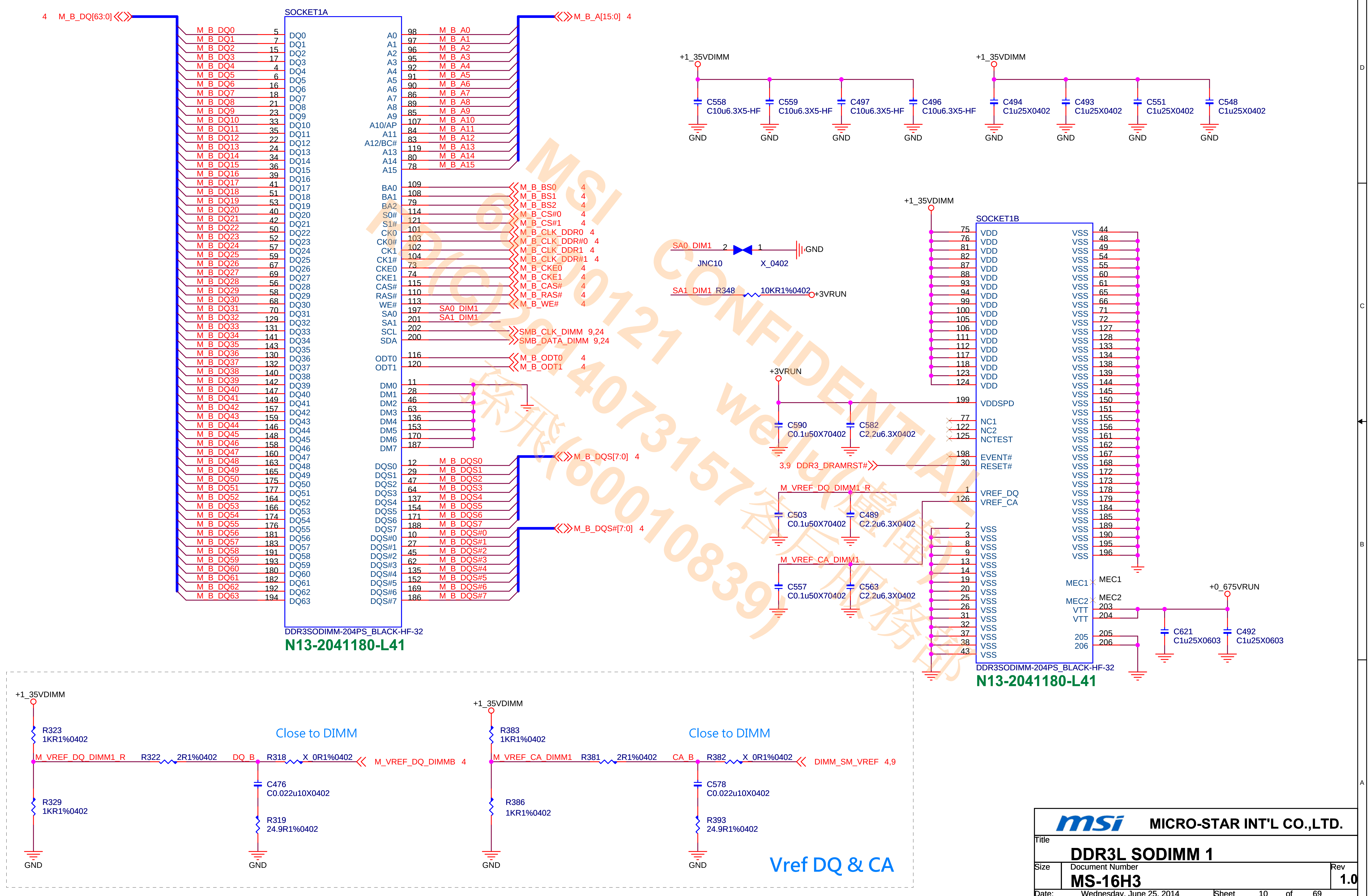
SODIMM#A



MICRO-STAR INT'L CO.,LTD.

Title	DDR3L SODIMM 0	
Size	Document Number: MS-16H3	Rev 1.0
Date: Wednesday, June 25, 2014	Sheet 9 of 69	

SODIMM#B



MICRO-STAR INT'L CO.,LTD.

Title: DDR3L SODIMM 1

Size | Document Number: MS-16H3 | Rev 1.0

Date: Wednesday, June 25, 2014 | Sheet 10 of 69

GPU CLK REQ#

18,20,27,34,52 DGPU_PWRGD

GPU_CLKREQ# 23

Q4 N-2N7002_SOT23-3-RH

PEX_CLKREQ#

Q3 X_N-2N7002_SOT23-3-RH

G5-N15P-GT-A2

X_N15P-GT-A2-RH

B03-0N15P25-N08

G5A

BGA908 COMMON

1/17 PCI_EXPRESS

GK107/GF108 GK208/GF117

2014.2.6 不上件
2014.3.3 改上件

+3V3_NV

R51 X_10KR0402

26 PCIE_RST#

TPJNC29

R27 100KR0402

PCIE_RST#

PEX_CLKREQ#

AJ11	PEX_WAKE	NC
AJ12	PEX_RST	
AK12	PEX_CLKREQ	
AL13	PEX_REFCLK	
AK13	PEX_REFCLK	

23 GFX_REFCLK
23 GFX_REFCLK#

3 PEG_RXP15	C396	C0.22u16X0402-HF	PEG_C_TXP15	AK14	PEX_TX0
3 PEG_RXN15	C403	C0.22u16X0402-HF	PEG_C_TXN15	AJ14	PEX_TX0
3 PEG_TXP15	C62	C0.22u16X0402-HF	PEG_C_RXP15	AN12	PEX_RX0
3 PEG_TXN15	C61	C0.22u16X0402-HF	PEG_C_RXN15	AM12	PEX_RX0
3 PEG_RXP14	C390	C0.22u16X0402-HF	PEG_C_TXP14	AH14	PEX_TX1
3 PEG_RXN14	C394	C0.22u16X0402-HF	PEG_C_TXN14	AG14	PEX_TX1
3 PEG_TXP14	C60	C0.22u16X0402-HF	PEG_C_RXP14	AN14	PEX_RX1
3 PEG_TXN14	C59	C0.22u16X0402-HF	PEG_C_RXN14	AM14	PEX_RX1
3 PEG_RXP13	C382	C0.22u16X0402-HF	PEG_C_TXP13	AK15	PEX_TX2
3 PEG_RXN13	C388	C0.22u16X0402-HF	PEG_C_TXN13	AJ15	PEX_TX2
3 PEG_TXP13	C58	C0.22u16X0402-HF	PEG_C_RXP13	AP14	PEX_RX2
3 PEG_TXN13	C57	C0.22u16X0402-HF	PEG_C_RXN13	AP15	PEX_RX2
3 PEG_RXP12	C370	C0.22u16X0402-HF	PEG_C_TXP12	AL16	PEX_TX3
3 PEG_RXN12	C381	C0.22u16X0402-HF	PEG_C_TXN12	AK16	PEX_TX3
3 PEG_TXP12	C56	C0.22u16X0402-HF	PEG_C_RXP12	AN15	PEX_RX3
3 PEG_TXN12	C55	C0.22u16X0402-HF	PEG_C_RXN12	AM15	PEX_RX3
3 PEG_RXP11	C368	C0.22u16X0402-HF	PEG_C_TXP11	AK17	PEX_TX4
3 PEG_RXN11	C359	C0.22u16X0402-HF	PEG_C_TXN11	AJ17	PEX_TX4
3 PEG_TXP11	C54	C0.22u16X0402-HF	PEG_C_RXP11	AN17	PEX_RX4
3 PEG_TXN11	C53	C0.22u16X0402-HF	PEG_C_RXN11	AM17	PEX_RX4
3 PEG_RXP10	C352	C0.22u16X0402-HF	PEG_C_TXP10	AH17	PEX_TX5
3 PEG_RXN10	C358	C0.22u16X0402-HF	PEG_C_TXN10	AG17	PEX_TX5
3 PEG_TXP10	C52	C0.22u16X0402-HF	PEG_C_RXP10	AP17	PEX_RX5
3 PEG_TXN10	C51	C0.22u16X0402-HF	PEG_C_RXN10	AP18	PEX_RX5
3 PEG_RXP9	C350	C0.22u16X0402-HF	PEG_C_TXP9	AK18	PEX_TX6
3 PEG_RXN9	C347	C0.22u16X0402-HF	PEG_C_TXN9	AJ18	PEX_TX6
3 PEG_TXP9	C50	C0.22u16X0402-HF	PEG_C_RXP9	AN18	PEX_RX6
3 PEG_TXN9	C49	C0.22u16X0402-HF	PEG_C_RXN9	AM18	PEX_RX6
3 PEG_RXP8	C341	C0.22u16X0402-HF	PEG_C_TXP8	AL19	PEX_TX7
3 PEG_RXN8	C344	C0.22u16X0402-HF	PEG_C_TXN8	AK19	PEX_TX7
3 PEG_TXP8	C48	C0.22u16X0402-HF	PEG_C_RXP8	AN20	PEX_RX7
3 PEG_TXN8	C47	C0.22u16X0402-HF	PEG_C_RXN8	AM20	PEX_RX7
3 PEG_RXP7	C340	C0.22u16X0402-HF	PEG_C_TXP7	AK20	PEX_TX8
3 PEG_RXN7	C329	C0.22u16X0402-HF	PEG_C_TXN7	AJ20	PEX_TX8
3 PEG_TXP7	C46	C0.22u16X0402-HF	PEG_C_RXP7	AP20	PEX_RX8
3 PEG_TXN7	C44	C0.22u16X0402-HF	PEG_C_RXN7	AP21	PEX_RX8
3 PEG_RXP6	C324	C0.22u16X0402-HF	PEG_C_TXP6	AH20	PEX_TX9
3 PEG_RXN6	C323	C0.22u16X0402-HF	PEG_C_TXN6	AG20	PEX_TX9
3 PEG_TXP6	C43	C0.22u16X0402-HF	PEG_C_RXP6	AN21	PEX_RX9
3 PEG_TXN6	C42	C0.22u16X0402-HF	PEG_C_RXN6	AM21	PEX_RX9
3 PEG_RXP5	C319	C0.22u16X0402-HF	PEG_C_TXP5	AK21	PEX_TX10
3 PEG_RXN5	C318	C0.22u16X0402-HF	PEG_C_TXN5	AJ21	PEX_TX10
3 PEG_TXP5	C41	C0.22u16X0402-HF	PEG_C_RXP5	AN23	PEX_RX10
3 PEG_TXN5	C40	C0.22u16X0402-HF	PEG_C_RXN5	AM23	PEX_RX10
3 PEG_RXP4	C315	C0.22u16X0402-HF	PEG_C_TXP4	AL22	PEX_TX11
3 PEG_RXN4	C317	C0.22u16X0402-HF	PEG_C_TXN4	AK22	PEX_TX11
3 PEG_TXP4	C39	C0.22u16X0402-HF	PEG_C_RXP4	AP23	PEX_RX11
3 PEG_TXN4	C38	C0.22u16X0402-HF	PEG_C_RXN4	AP24	PEX_RX11
3 PEG_RXP3	C312	C0.22u16X0402-HF	PEG_C_TXP3	AK23	PEX_TX12
3 PEG_RXN3	C308	C0.22u16X0402-HF	PEG_C_TXN3	AJ23	PEX_TX12
3 PEG_TXP3	C37	C0.22u16X0402-HF	PEG_C_RXP3	AN24	PEX_RX12
3 PEG_TXN3	C36	C0.22u16X0402-HF	PEG_C_RXN3	AM24	PEX_RX12
3 PEG_RXP2	C305	C0.22u16X0402-HF	PEG_C_TXP2	AH23	PEX_TX13
3 PEG_RXN2	C307	C0.22u16X0402-HF	PEG_C_TXN2	AG23	PEX_TX13
3 PEG_TXP2	C35	C0.22u16X0402-HF	PEG_C_RXP2	AN26	PEX_RX13
3 PEG_TXN2	C34	C0.22u16X0402-HF	PEG_C_RXN2	AM26	PEX_RX13
3 PEG_RXP1	C304	C0.22u16X0402-HF	PEG_C_TXP1	AK24	PEX_TX14
3 PEG_RXN1	C302	C0.22u16X0402-HF	PEG_C_TXN1	AJ24	PEX_TX14
3 PEG_TXP1	C33	C0.22u16X0402-HF	PEG_C_RXP1	AP26	PEX_RX14
3 PEG_TXN1	C32	C0.22u16X0402-HF	PEG_C_RXN1	AP27	PEX_RX14
3 PEG_RXP0	C301	C0.22u16X0402-HF	PEG_C_TXP0	AL25	PEX_TX15
3 PEG_RXN0	C300	C0.22u16X0402-HF	PEG_C_TXN0	AK25	PEX_TX15
3 PEG_TXP0	C31	C0.22u16X0402-HF	PEG_C_RXP0	AN27	PEX_RX15
3 PEG_TXN0	C29	C0.22u16X0402-HF	PEG_C_RXN0	AM27	PEX_RX15

PEX LANES 8 TO 15 NC FOR GF117/GK208

GF108 GK208/GK107/GF117

NC

PEX_PLL_HVDD AH12

PEX_SVDD_3V3 AG12

PEX_IOVDD AG19, AG21, AG22, AG24, AH21, AH25

PEX_IOVDDQ AG13, AG15, AG16, AG18, AG25, AH15, AH18, AH26, AH27, AJ27, AK27, AL27, AM28, AN28

Under GPU / Near GPU

PEX_VDD 1.05V

3.3A

C400 C1u6.3X60402-RH
C316 C1u6.3X60402-RH
C78 C4.7u6.3X6
C70 C10u6.3X7R_0805
C75 C10u6.3X7R_0805
C453 C22u6.3X60805-HF
C451 C22u6.3X60805-HF

C311 C1u6.3X60402-RH
C346 C1u6.3X60402-RH
C397 C4.7u6.3X6
C444 C10u6.3X7R_0805
C69 C10u6.3X7R_0805
C76 C22u6.3X60805-HF
C63 C22u6.3X60805-HF

2014.03.13 Modify

1x 0.1u under GPU;
2x 4.7u near GPU;

Near GPU

0.21A

+3V3_NV

C426 C0.1u10X0402
C424 C4.7u6.3X6

Near GPU

+3V3_NV

C415 C4.7u6.3X6

2014.03.13 remove

GPU to R < 10000mils

R to PWM < 2000mils

VDD_SENSE L4 NVVDD_SENSE_GPU 51

GND_SENSE L5 NVVDD_GND_SENSE_GPU 51

GPU to R < 10000mils

R to PWM < 2000 mils

2014.03.13 remove

Near PWM

Under GPU

PEX_VDD

C80 C1u6.3X60402-RH

2014.03.13 Change

3V3AUX_NC P8

PEX_TSTCLK_OUT AJ26 PEX_TSTCLK_OUT R244 X_200R1%0402

PEX_TSTCLK_OUT AK26 PEX_TSTCLK_OUT#

PEX_PLLVDD AG26 0.15A

Under GPU / Near GPU

PEX_VDD

C456 C0.1u10X0402
C454 C4.7u6.3X6

TESTMODE AK11 GPU_TESTMODE R260 10KR1%0402

PEX_TERMP AP29 PEX_TERMP R15 2.49KR1%0402

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	N15P-Q3_PCIE Host	
Size	Document Number MS-16H3	Rev 1.0
Date: Wednesday, June 25, 2014	Sheet 11 of 69	

G5B

BGA908 COMMON

2/17 FBA

13	FBA_D0	L28	FBA_D0
13	FBA_D1	M29	FBA_D1
13	FBA_D2	L29	FBA_D2
13	FBA_D3	M28	FBA_D3
13	FBA_D4	N31	FBA_D4
13	FBA_D5	P29	FBA_D5
13	FBA_D6	R29	FBA_D6
13	FBA_D7	P28	FBA_D7
13	FBA_D8	J28	FBA_D8
13	FBA_D9	H29	FBA_D9
13	FBA_D10	J29	FBA_D10
13	FBA_D11	H28	FBA_D11
13	FBA_D12	G29	FBA_D12
13	FBA_D13	E31	FBA_D13
13	FBA_D14	E32	FBA_D14
13	FBA_D15	F30	FBA_D15
13	FBA_D16	C34	FBA_D16
13	FBA_D17	D32	FBA_D17
13	FBA_D18	B33	FBA_D18
13	FBA_D19	C33	FBA_D19
13	FBA_D20	E33	FBA_D20
13	FBA_D21	E32	FBA_D21
13	FBA_D22	H33	FBA_D22
13	FBA_D23	H32	FBA_D23
13	FBA_D24	P34	FBA_D24
13	FBA_D25	P32	FBA_D25
13	FBA_D26	P31	FBA_D26
13	FBA_D27	P33	FBA_D27
13	FBA_D28	L31	FBA_D28
13	FBA_D29	L34	FBA_D29
13	FBA_D30	L32	FBA_D30
13	FBA_D31	L33	FBA_D31
14	FBA_D32	AG28	FBA_D32
14	FBA_D33	AF29	FBA_D33
14	FBA_D34	AG29	FBA_D34
14	FBA_D35	AE28	FBA_D35
14	FBA_D36	AD30	FBA_D36
14	FBA_D37	AD29	FBA_D37
14	FBA_D38	AC29	FBA_D38
14	FBA_D39	AD28	FBA_D39
14	FBA_D40	AJ29	FBA_D40
14	FBA_D41	AK29	FBA_D41
14	FBA_D42	AJ30	FBA_D42
14	FBA_D43	AK28	FBA_D43
14	FBA_D44	AM29	FBA_D44
14	FBA_D45	AM31	FBA_D45
14	FBA_D46	AN29	FBA_D46
14	FBA_D47	AM30	FBA_D47
14	FBA_D48	AN31	FBA_D48
14	FBA_D49	AN32	FBA_D49
14	FBA_D50	AP30	FBA_D50
14	FBA_D51	AP32	FBA_D51
14	FBA_D52	AM33	FBA_D52
14	FBA_D53	AL31	FBA_D53
14	FBA_D54	AK33	FBA_D54
14	FBA_D55	AK32	FBA_D55
14	FBA_D56	AD34	FBA_D56
14	FBA_D57	AD32	FBA_D57
14	FBA_D58	AC30	FBA_D58
14	FBA_D59	AD33	FBA_D59
14	FBA_D60	AF31	FBA_D60
14	FBA_D61	AG34	FBA_D61
14	FBA_D62	AG32	FBA_D62
14	FBA_D63	AG33	FBA_D63

13	FBA_DBI0	P30	FBA_DQM0
13	FBA_DBI1	F31	FBA_DQM1
13	FBA_DBI2	F34	FBA_DQM2
13	FBA_DBI3	M32	FBA_DQM3
14	FBA_DBI4	AD31	FBA_DQM4
14	FBA_DBI5	AL29	FBA_DQM5
14	FBA_DBI6	AM32	FBA_DQM6
14	FBA_DBI7	AE34	FBA_DQM7

NC
NC
GF117/GK208
GK107/GF108

13	FBA_EDC0	M31	FBA_DQS_WP0
13	FBA_EDC1	G31	FBA_DQS_WP1
13	FBA_EDC2	E33	FBA_DQS_WP2
13	FBA_EDC3	M33	FBA_DQS_WP3
14	FBA_EDC4	AE31	FBA_DQS_WP4
14	FBA_EDC5	AK30	FBA_DQS_WP5
14	FBA_EDC6	AN33	FBA_DQS_WP6
14	FBA_EDC7	AF33	FBA_DQS_WP7

		M30	FBA_DQS_RN0
		H30	FBA_DQS_RN1
		E34	FBA_DQS_RN2
		M34	FBA_DQS_RN3
		AF30	FBA_DQS_RN4
		AK31	FBA_DQS_RN5
		AM34	FBA_DQS_RN6
		AF32	FBA_DQS_RN7

THE FBA_WCKBxx PINS ARE USED ONLY ON GK107 THEY ARE NC FOR GK208/GF108 /GF117

		H26	FB_VREF

FBVDDQ

R246 X_1.3KR1%0402

R245 X_1.3KR1%0402

C328 X_C0.01u25X0402

FB_CLAMP E1

FB_CLAMP 18,20,34

R47 10KR0402

FB_DLL_AVDD K27

FB_DLL_AVDD 50mA

PEX_VDD

L4 30L5A-10-RH

2014.03.17 Change to BEAD,300hm,25%,0603,5000mA,0.010hm

Under GPU

C310 C0.1u10X0402

Near GPU

C268 C22u6.3X60805-HF

2014.03.13 Stuff

		U30	FBA_CMD0
		T31	FBA_CMD1
		U29	FBA_CMD2
		R34	FBA_CMD3
		R33	FBA_CMD4
		U32	FBA_CMD5
		U33	FBA_CMD6
		U28	FBA_CMD7
		V28	FBA_CMD8
		V29	FBA_CMD9
		V30	FBA_CMD10
		U34	FBA_CMD11
		U31	FBA_CMD12
		V34	FBA_CMD13
		V33	FBA_CMD14
		V32	FBA_CMD15
		AA31	FBA_CMD16
		AA29	FBA_CMD17
		AA28	FBA_CMD18
		AC34	FBA_CMD19
		AC33	FBA_CMD20
		AA32	FBA_CMD21
		AA33	FBA_CMD22
		Y28	FBA_CMD23
		Y29	FBA_CMD24
		W31	FBA_CMD25
		Y30	FBA_CMD26
		AA34	FBA_CMD27
		Y31	FBA_CMD28
		Y34	FBA_CMD29
		Y33	FBA_CMD30
		V31	FBA_CMD31

		R32	FBA_CMD_RFU0
		AC32	FBA_CMD_RFU1

TPJNC27

TPJNC28

FBVDDQ

		R28	FBA_DEBUG0
		AC28	FBA_DEBUG1

FBA_DEBUG0 R239 X_60.4R1%0402

FBA_DEBUG1 R240 X_60.4R1%0402

For debug purposes only,no-stuffed. ---Dragon 9/10

		R30	FBA_CLK0
		R31	FBA_CLK0#
		AB31	FBA_CLK1
		AC31	FBA_CLK1#

		K31	FBA_WCK01
		L30	FBA_WCK01#
		H34	FBA_WCK23
		J34	FBA_WCK23#
		AG30	FBA_WCK45
		AG31	FBA_WCK45#
		AJ34	FBA_WCK67
		AK34	FBA_WCK67#

		J30	FBA_WCKB01
		J31	FBA_WCKB01
		J32	FBA_WCKB23
		J33	FBA_WCKB23
		AH31	FBA_WCKB45
		AJ31	FBA_WCKB45
		AJ32	FBA_WCKB67
		AJ33	FBA_WCKB67

		U22	FBA_PLL_AVDD

120mA

FA_PLLAVDD

L5 X_30L5A-10-RH

For N14P

+3V3_NV

For N14E-GL

L6 30L5A-10-RH

2014.03.17 Change to BEAD,300hm,25%,0603,5000mA,0.010hm

Under GPU

C378 C0.1u10X0402

C322 C.1u10X

C267 C22u6.3X60805-HF

Near GPU

2014.03.13 Modify

GDDR5 CMD Mapping Table

<0..31>	<32..63>	MEMORY
12	28	RAS*
15	31	CAS*
5	21	WE*
0	16	CS*
8	24	ABI*
10	26	A0_A10
11	27	A1_A9
2	18	A2_BA0
1	17	A3_BA3
3	19	A4_BA2
4	20	A5_BA1
7	23	A6_A11
6	22	A7_A8
9	25	A12_RFU
14	30	CKE*
13	29	RESET*

FBVDDQ

RN8 8P4R-10KR0402

FBA CKE H FBA_CMD30

FBA CKE L FBA_CMD14

FBA RST H FBA_CMD29

FBA RST L FBA_CMD13

G5C

BGA908 COMMON

3/17 FBB

ALL PINS NC FOR GF117/GK208

15	FBB_D0	G9	FBB_D0
15	FBB_D1	E9	FBB_D1
15	FBB_D2	G8	FBB_D2
15	FBB_D3	E8	FBB_D3
15	FBB_D4	F11	FBB_D4
15	FBB_D5	G11	FBB_D5
15	FBB_D6	F12	FBB_D6
15	FBB_D7	G12	FBB_D7
15	FBB_D8	G6	FBB_D8
15	FBB_D9	F5	FBB_D9
15	FBB_D10	E6	FBB_D10
15	FBB_D11	F6	FBB_D11
15	FBB_D12	F4	FBB_D12
15	FBB_D13	G4	FBB_D13
15	FBB_D14	E2	FBB_D14
15	FBB_D15	F3	FBB_D15
15	FBB_D16	C2	FBB_D16
15	FBB_D17	D4	FBB_D17
15	FBB_D18	D3	FBB_D18
15	FBB_D19	C1	FBB_D19
15	FBB_D20	B3	FBB_D20
15	FBB_D21	C4	FBB_D21
15	FBB_D22	B5	FBB_D22
15	FBB_D23	C5	FBB_D23
15	FBB_D24	A11	FBB_D24
15	FBB_D25	C11	FBB_D25
15	FBB_D26	D11	FBB_D26
15	FBB_D27	B11	FBB_D27
15	FBB_D28	D8	FBB_D28
15	FBB_D29	A8	FBB_D29
15	FBB_D30	C8	FBB_D30
15	FBB_D31	B8	FBB_D31
16	FBB_D32	F24	FBB_D32
16	FBB_D33	G23	FBB_D33
16	FBB_D34	E24	FBB_D34
16	FBB_D35	G24	FBB_D35
16	FBB_D36	D21	FBB_D36
16	FBB_D37	E21	FBB_D37
16	FBB_D38	G21	FBB_D38
16	FBB_D39	F21	FBB_D39
16	FBB_D40	G27	FBB_D40
16	FBB_D41	D27	FBB_D41
16	FBB_D42	G26	FBB_D42
16	FBB_D43	E27	FBB_D43
16	FBB_D44	E29	FBB_D44
16	FBB_D45	F29	FBB_D45
16	FBB_D46	E30	FBB_D46
16	FBB_D47	D30	FBB_D47
16	FBB_D48	A32	FBB_D48
16	FBB_D49	C31	FBB_D49
16	FBB_D50	C32	FBB_D50
16	FBB_D51	B32	FBB_D51
16	FBB_D52	D29	FBB_D52
16	FBB_D53	A29	FBB_D53
16	FBB_D54	C29	FBB_D54
16	FBB_D55	B29	FBB_D55
16	FBB_D56	B21	FBB_D56
16	FBB_D57	C23	FBB_D57
16	FBB_D58	A21	FBB_D58
16	FBB_D59	C21	FBB_D59
16	FBB_D60	B24	FBB_D60
16	FBB_D61	C24	FBB_D61
16	FBB_D62	B26	FBB_D62
16	FBB_D63	C26	FBB_D63

15	FBB_DBI0	E11	FBB_DQM0
15	FBB_DBI1	E3	FBB_DQM1
15	FBB_DBI2	A3	FBB_DQM2
15	FBB_DBI3	C9	FBB_DQM3
16	FBB_DBI4	F23	FBB_DQM4
16	FBB_DBI5	F27	FBB_DQM5
16	FBB_DBI6	C30	FBB_DQM6
16	FBB_DBI7	A24	FBB_DQM7

15	FBB_EDC0	D10	FBB_DQS_WP0
15	FBB_EDC1	D5	FBB_DQS_WP1
15	FBB_EDC2	C3	FBB_DQS_WP2
15	FBB_EDC3	B9	FBB_DQS_WP3
16	FBB_EDC4	F23	FBB_DQS_WP4
16	FBB_EDC5	E28	FBB_DQS_WP5
16	FBB_EDC6	B30	FBB_DQS_WP6
16	FBB_EDC7	A23	FBB_DQS_WP7

		D9	FBB_DQS_RN0
		E4	FBB_DQS_RN1
		B2	FBB_DQS_RN2
		A9	FBB_DQS_RN3
		D22	FBB_DQS_RN4
		D28	FBB_DQS_RN5
		A30	FBB_DQS_RN6
		B23	FBB_DQS_RN7

		D13	FBB_CMD0
		E14	FBB_CMD1
		F14	FBB_CMD2
		A12	FBB_CMD3
		B12	FBB_CMD4
		C14	FBB_CMD5
		B14	FBB_CMD6
		G15	FBB_CMD7
		F15	FBB_CMD8
		E15	FBB_CMD9
		D15	FBB_CMD10
		A14	FBB_CMD11
		D14	FBB_CMD12
		A15	FBB_CMD13
		B15	FBB_CMD14
		C17	FBB_CMD15
		D18	FBB_CMD16
		E18	FBB_CMD17
		F18	FBB_CMD18
		A20	FBB_CMD19
		B20	FBB_CMD20
		C18	FBB_CMD21
		B18	FBB_CMD22
		G18	FBB_CMD23
		G17	FBB_CMD24
		F17	FBB_CMD25
		D16	FBB_CMD26
		A18	FBB_CMD27
		D17	FBB_CMD28
		A17	FBB_CMD29
		B17	FBB_CMD30
		E17	FBB_CMD31

		C12	FBB_CMD_RFU0
		C20	FBB_CMD_RFU1

FBVDDQ

		G14	FBB_DEBUG0
		G20	FBB_DEBUG1

FBB_DEBUG0 R255 X_60.4R1%0402

FBB_DEBUG1 R251 X_60.4R1%0402

For debug purposes only,no-stuffed. ---Dragon 9/10

		D12	FBB_CLK0
		E12	FBB_CLK0#
		E20	FBB_CLK1
		F20	FBB_CLK1#

		E8	FBB_WCK01
		A5	FBB_WCK01#
		A6	FBB_WCK23
		D24	FBB_WCK23#
		D25	FBB_WCK45
		B27	FBB_WCK45#
		C27	FBB_WCK67
			FBB_WCK67#

THE FBB_WCKBxx PINS ARE USED ONLY ON GK107 THEY ARE NC FOR GF108

		D6	FBB_WCKB01
		D7	FBB_WCKB01
		C6	FBB_WCKB23
		B6	FBB_WCKB23
		F26	FBB_WCKB45
		E26	FBB_WCKB45
		A26	FBB_WCKB67
		A27	FBB_WCKB67

		H17	FBB_PLL_AVDD

NC
GF108
GK107

120mA

FA_PLLAVDD

C330 C0.1u10X0402

Under GPU

FBB CKE H FBB_CMD30

FBB CKE L FBB_CMD14

FBB RST H FBB_CMD29

FBB RST L FBB_CMD13

RN9 8P4R-10KR0402

FBVDDQ

Title	N15P-Q3 MEM Interface
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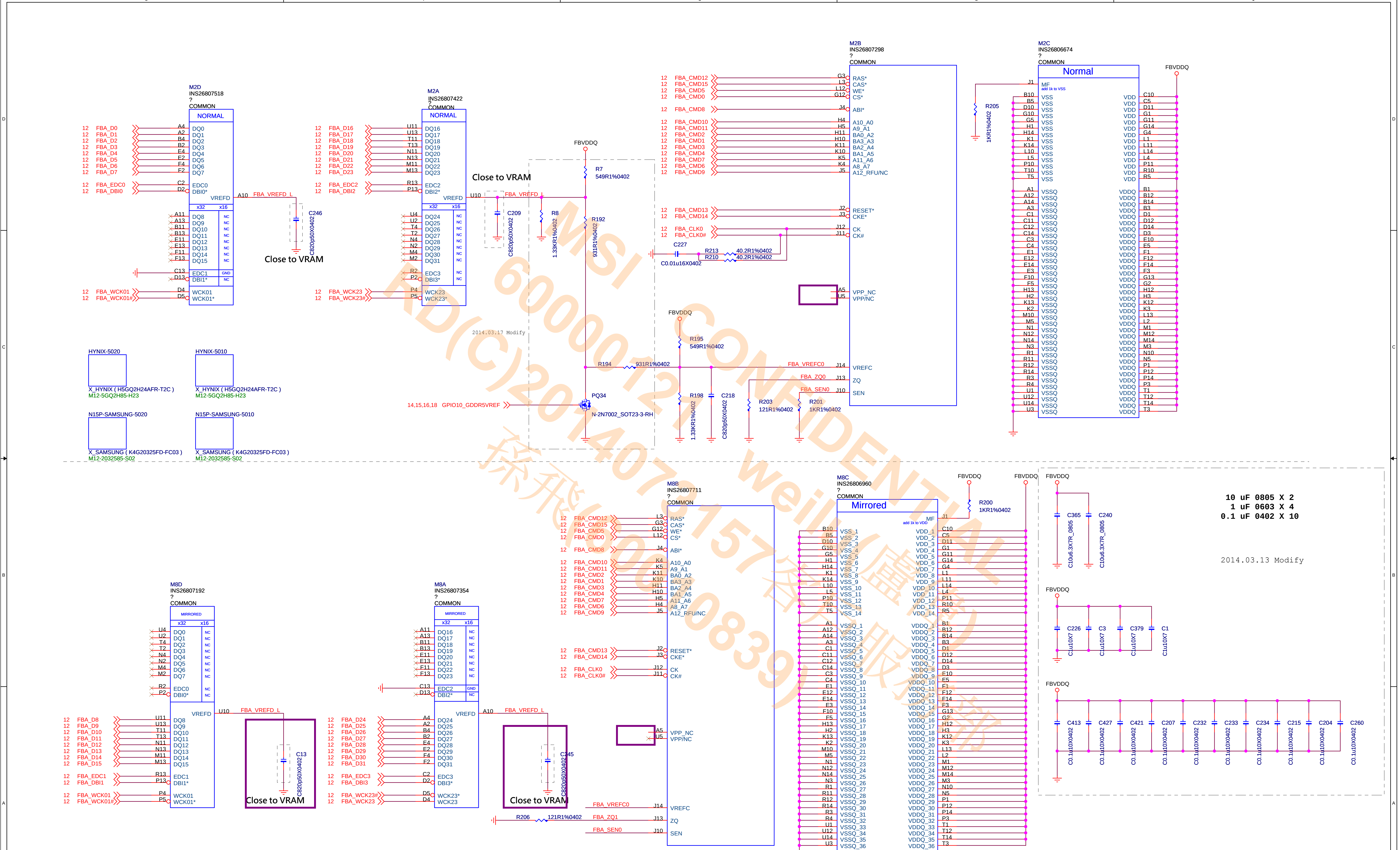
MICRO-STAR INT'L CO.,LTD.

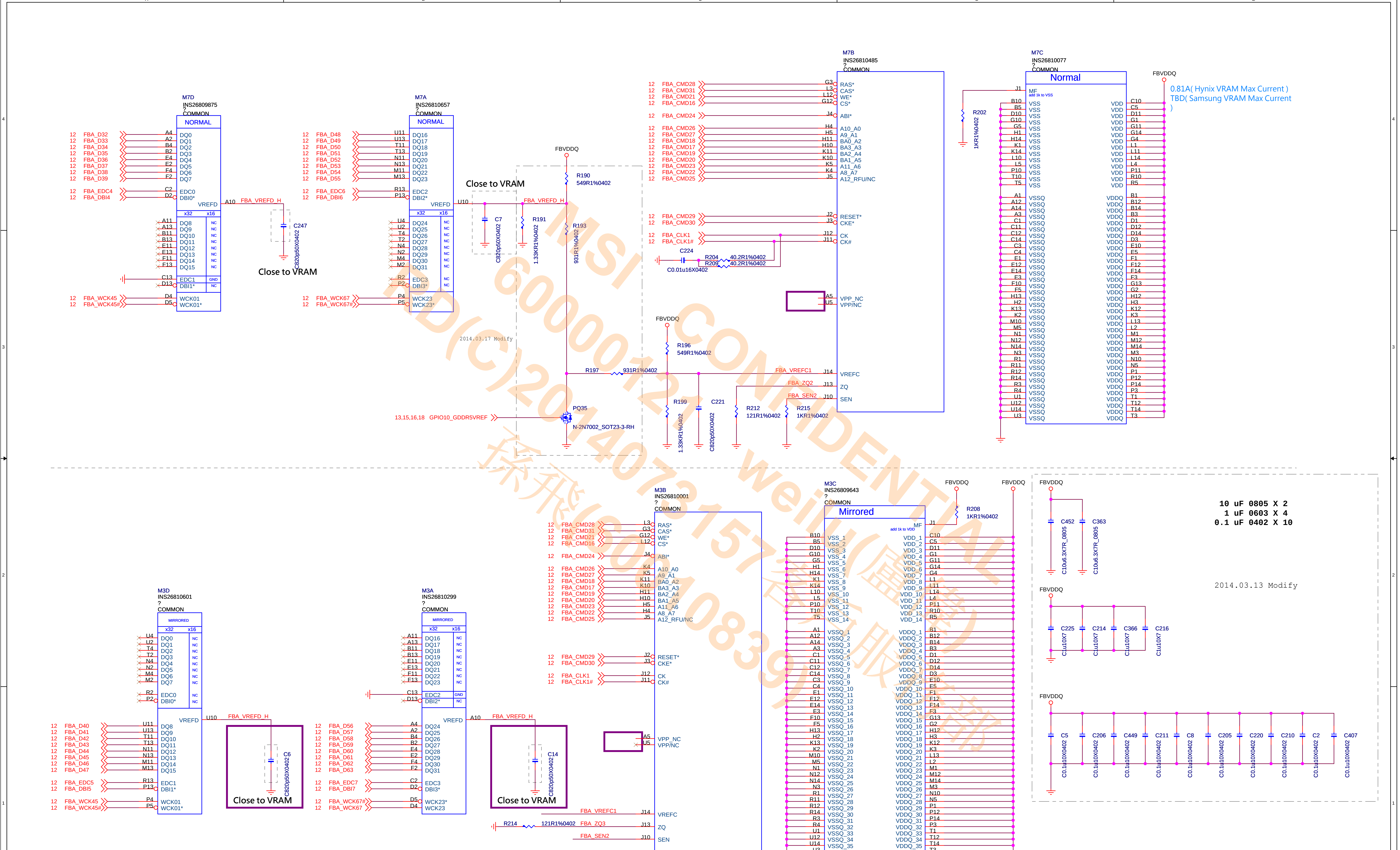


MICRO-STAR INT'L CO.,LTD.

Title: N15P-Q_FrameA GDDR5 I

Size | Document Number: MS-16H3 | Rev 1.0

Date: Wednesday, June 25, 2014 | Sheet 13 of 69



MICRO-STAR INT'L CO.,LTD.

Title	N15P-Q3_FrameA GDDR5 II
Size	Document Number: MS-16H3
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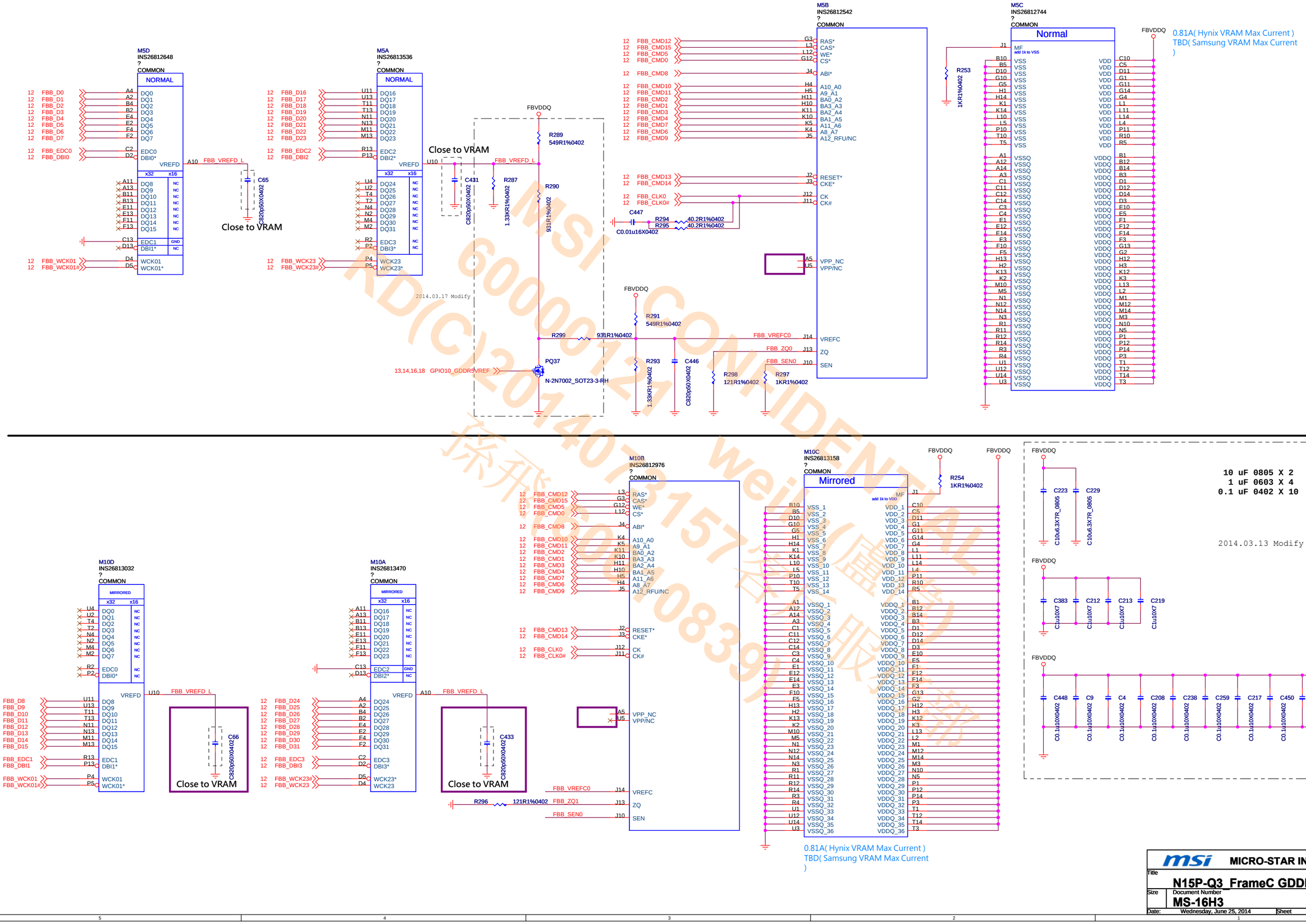
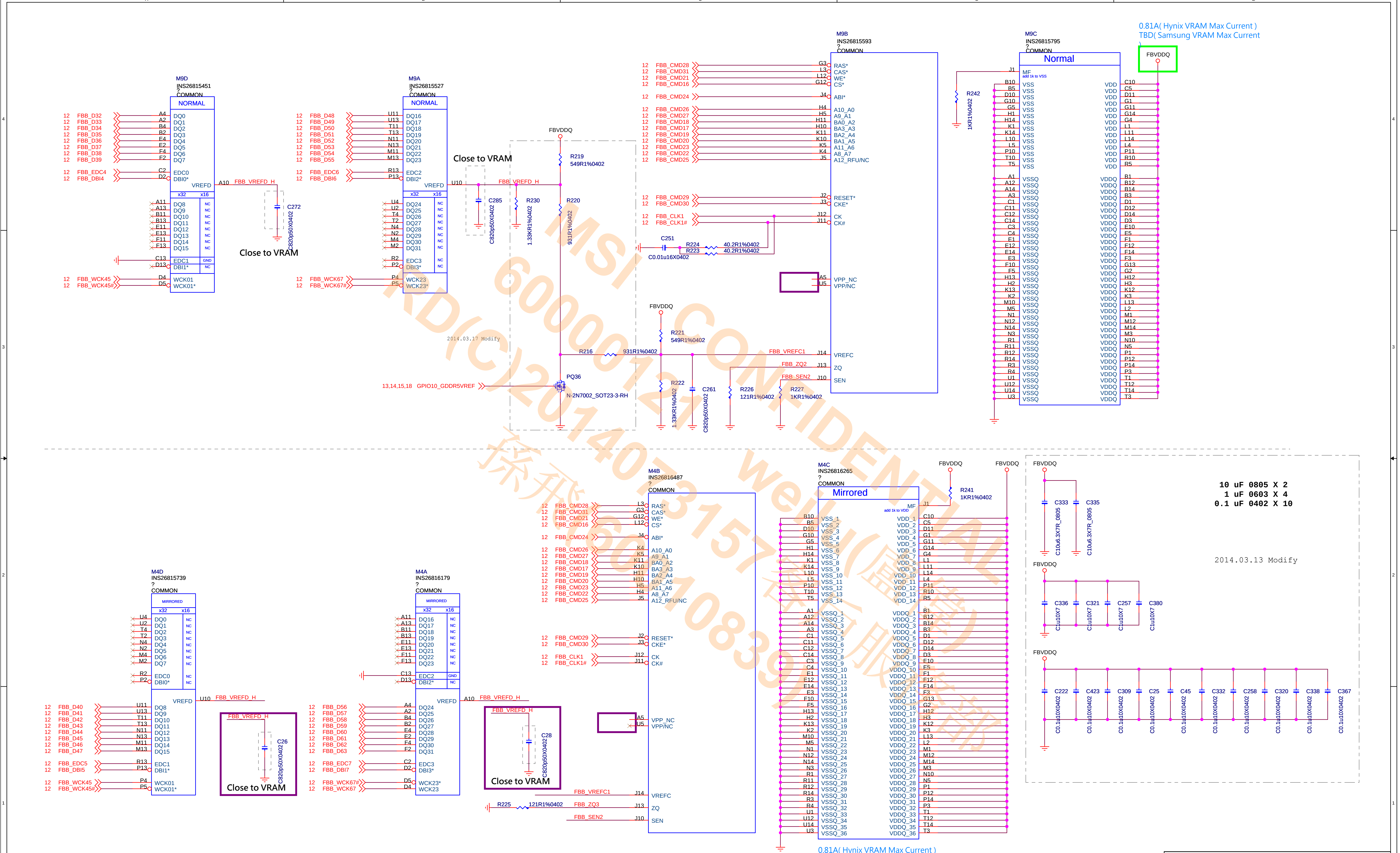
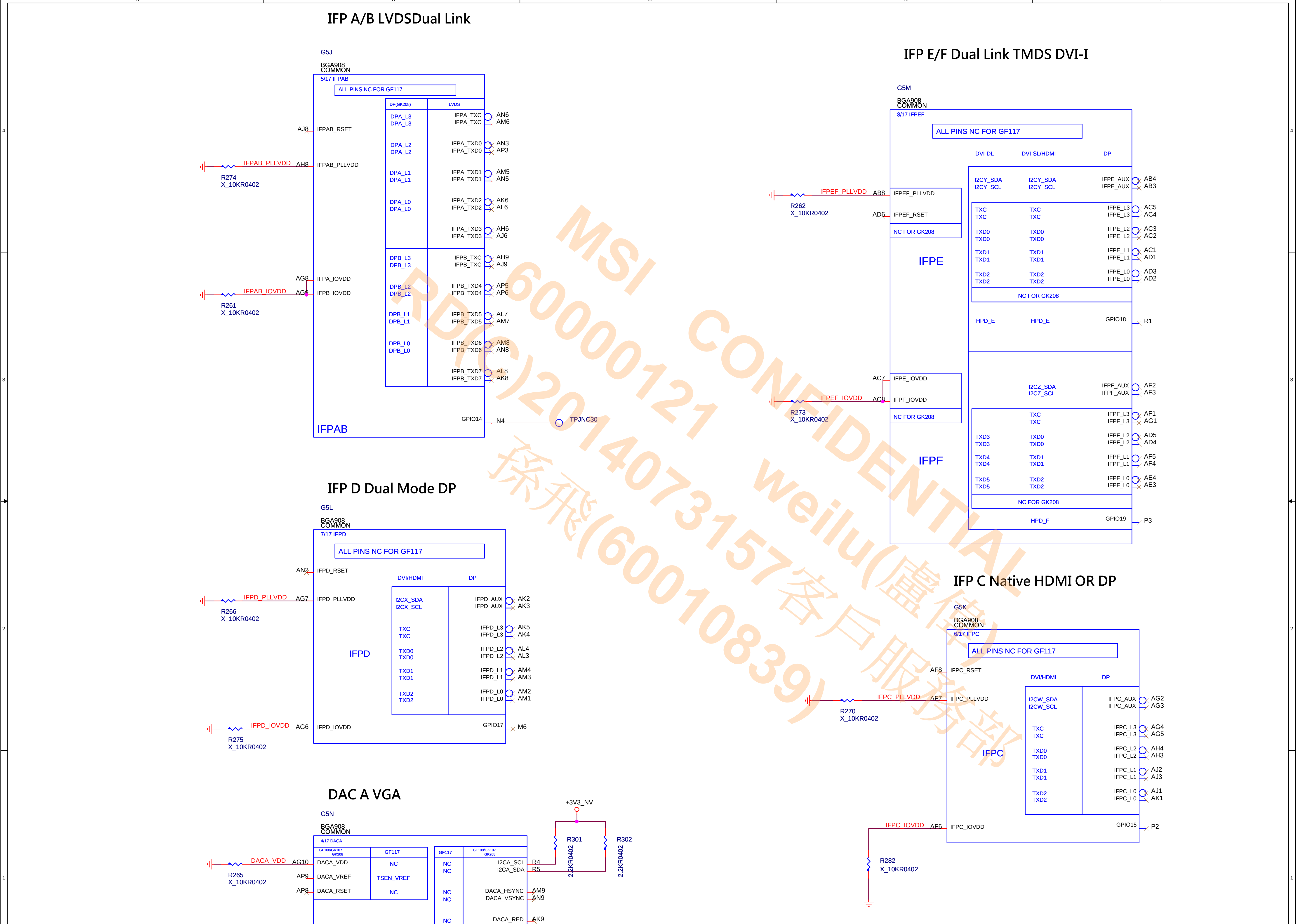

M5D
INS26812648
?
COMMON
NORMAL
M5A
INS26813536
?
COMMON
NORMAL
M5B
INS26812542
?
COMMON
M5C
INS26812744
?
COMMON
Normal
M10D
INS26813032
?
COMMON
MIRRORED
M10A
INS26813470
?
COMMON
MIRRORED
M10B
INS26812976
?
COMMON
M10C
INS26813158
?
COMMON
Mirrored
Close to VRAM
2014.03.17 Modify
2014.03.13 Modify
0.81A(Hynix VRAM Max Current)
TBD(Samsung VRAM Max Current)
10 uF 0805 X 2
1 uF 0603 X 4
0.1 uF 402 X 10
MICRO-STAR INT'L CO.,LTD.
N15P-Q3_FrameC GDDR5 I
MS-16H3
Wednesday, June 25, 2014



M9D INS26815451 COMMON NORMAL
M9A INS26815527 COMMON NORMAL
M9B INS26815593 COMMON
M9C INS26815795 COMMON Normal
M4D INS26815739 COMMON MIRRORED
M4A INS26816179 COMMON MIRRORED
M4B INS26816487 COMMON
M4C INS26816265 COMMON Mirrored
Close to VRAM
0.81A(Hynix VRAM Max Current)
TBD(Samsung VRAM Max Current)
FBVDDQ
10 uF 0805 X 2
1 uF 0603 X 4
0.1 uF 0402 X 10
2014.03.13 Modify
2014.03.17 Modify
13,14,15,18 GPIO10_GDDR5VREF
PQ36 N-2N7002_SOT23-3-RH

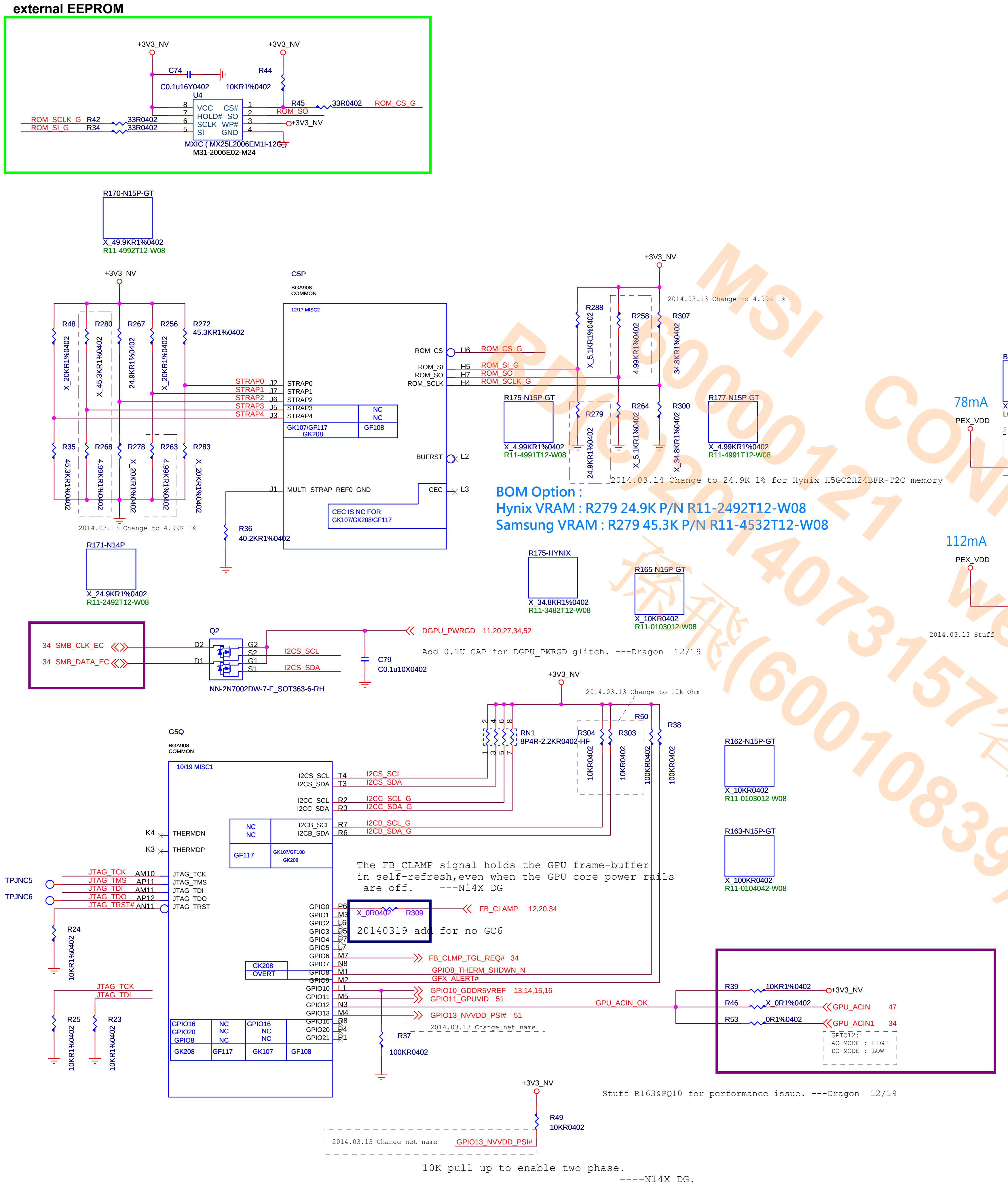


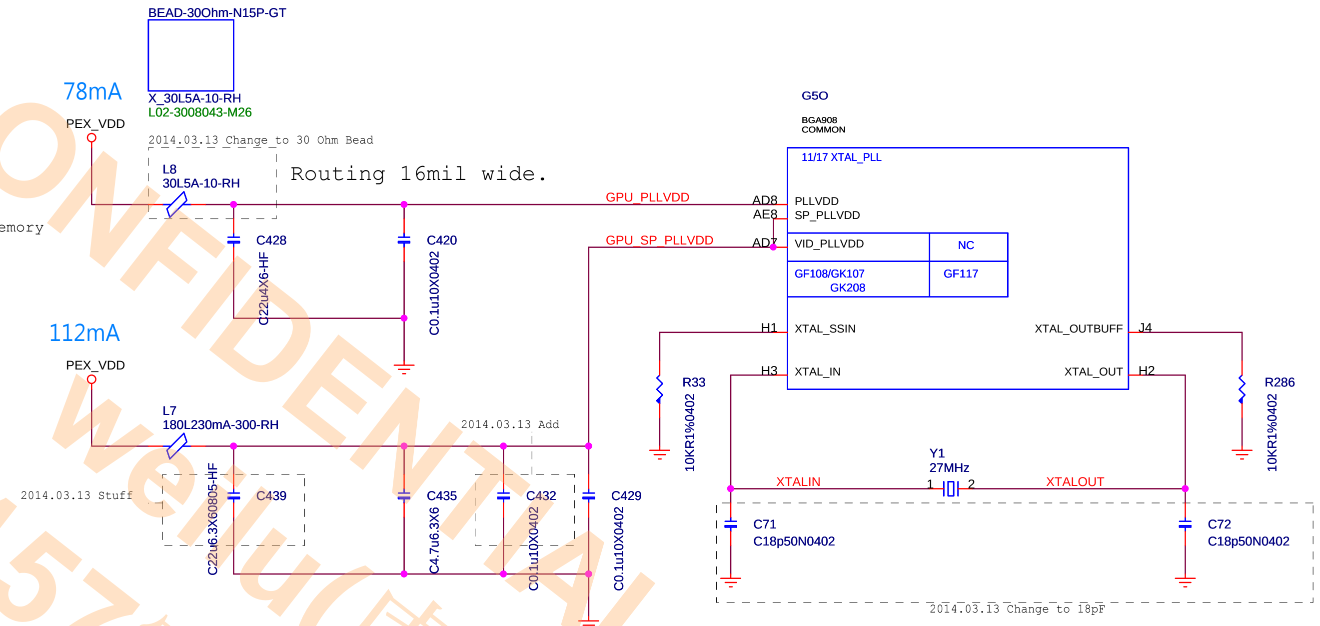
MICRO-STAR INT'L CO.,LTD.

Title: N15P-Q3 Display Interface

Size	Document Number	Rev
	MS-16H3	1.0

Date: Wednesday, June 25, 2014 Sheet 17 of 69





Item	Location	N15P-Q3
Strap Mode	R3365	MULTISTRAP_REF_GND,40.2K PD to GND
Device ID		0x11FC
Package		GB4-128
Memory Type		GDDR5
ROM_SI	R3175	0x4, Hynix 2G, 24.9kohm PD
	R3175	0x7, Samsung 2G, 45kohm PD
ROM_SO	R3193	0x8, 5kohm pull up
ROM_SCLK	R3179	0x1110,35kohm PU(with ROM)
Strap0	R3170	45kohm pull up
Strap1	R3180	5kohm pull down
Strap2	R3171	DID,0x1100, 24.9kohm PU
Strap3	R3188	0x0 for Optimus, 5kohm pull down
Strap4	R3183	0x0111, 45kohm pull down

Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor	
GPIO1	NC	O		
GPIO2	NC	O		
GPIO3	NC	O		
GPIO4	NC	O		
GPIO5	NC	O		
GPIO6	FB_CLAMP_TGL_REQ	O	FB Clamp toggle request	
GPIO7	NC	O		
GPIO8	OVERT	I	Thermal Over Temperature	100K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect	100K pull-up
GPIO13	SPI	O	Phase Shedding	10K pull-up
GPIO14	NC	I		
GPIO15	NC	I		
GPIO16	NC	O		
GPIO17	NC	I		
GPIO18	NC	I		
GPIO19	NC	I		
NC	NC			

MICRO-STAR INT'L CO.,LTD.

Title: N15P-Q3_Thermal & GPIO

Size | Document Number: MS-16H3 | Rev 1.0

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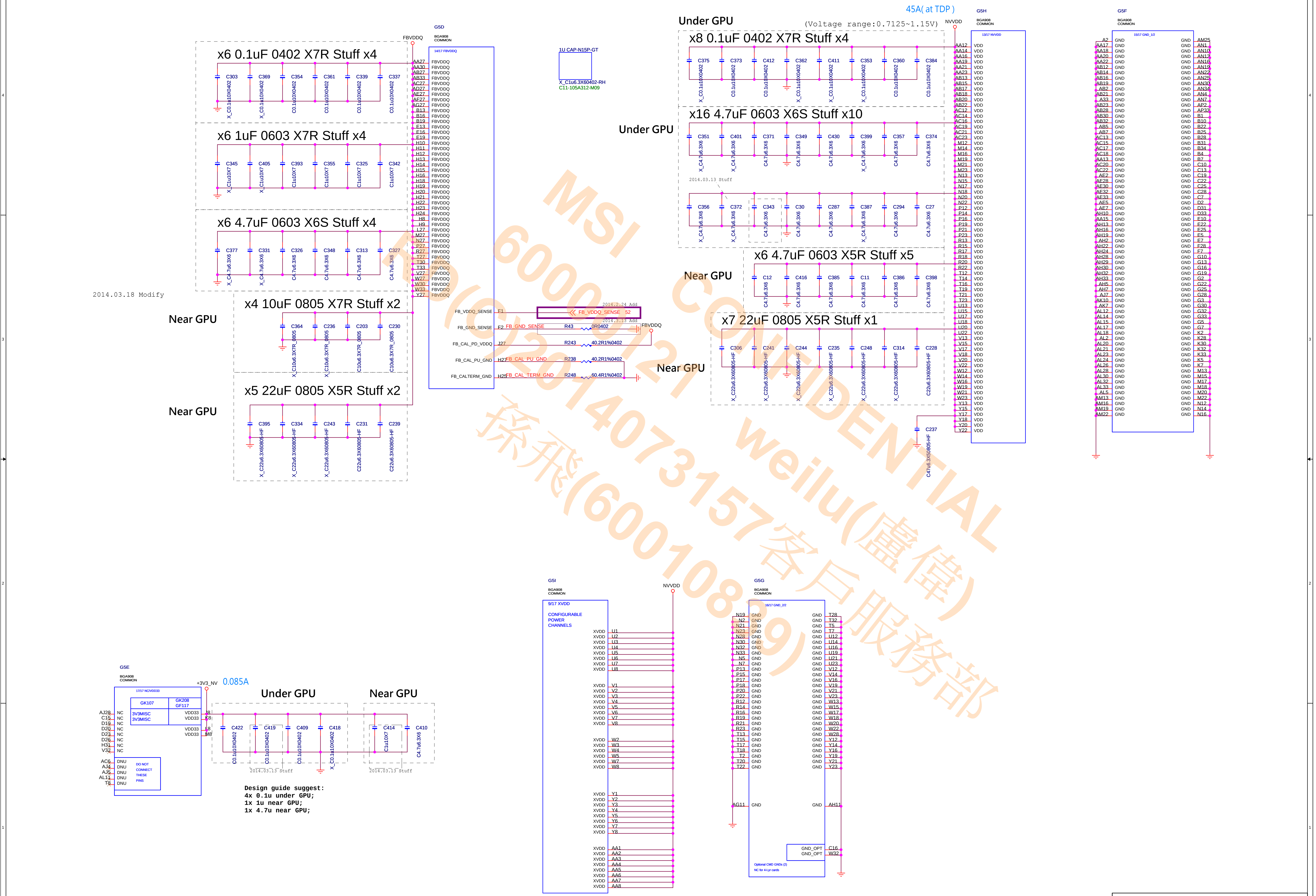

MICRO-STAR INT'L CO.,LTD.

Title: N15P-Q3 Power & GND

Size | Document Number: MS-16H3 | Rev 1.0

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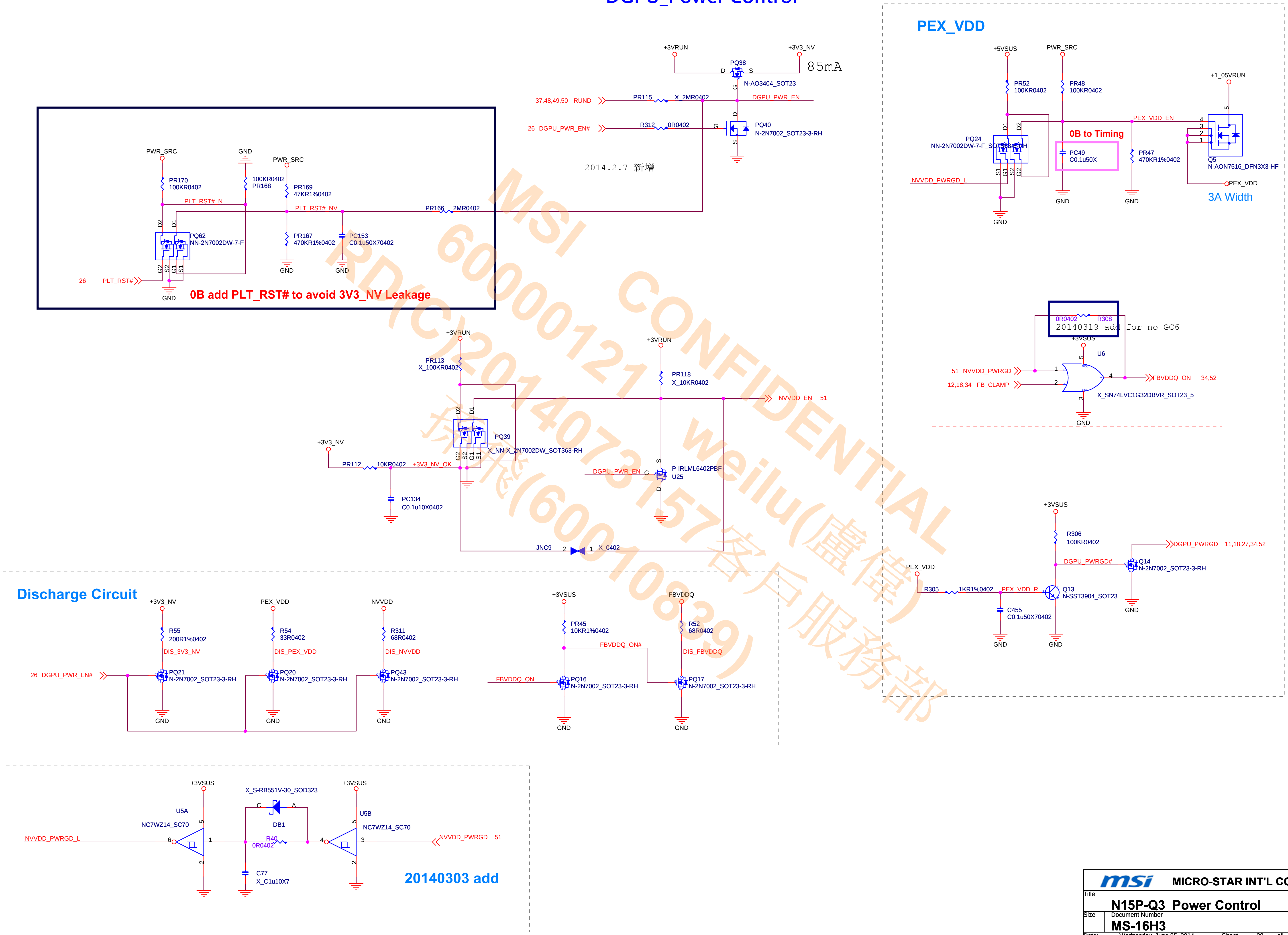
DGPU_Power Control



MSI MICRO-STAR INT'L CO.,LTD.

Title: N15P-Q3_Power Control

Size | Document Number: MS-16H3 | Rev 1.0

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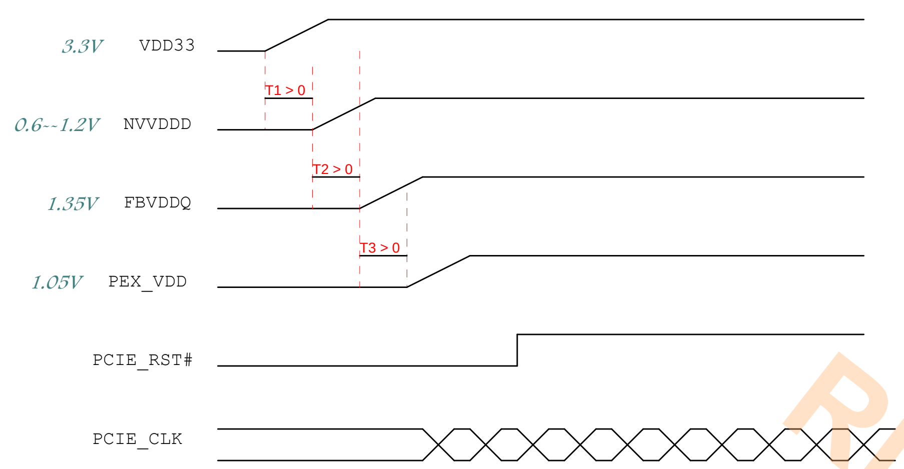
GPU POWER ON SEQUENCE

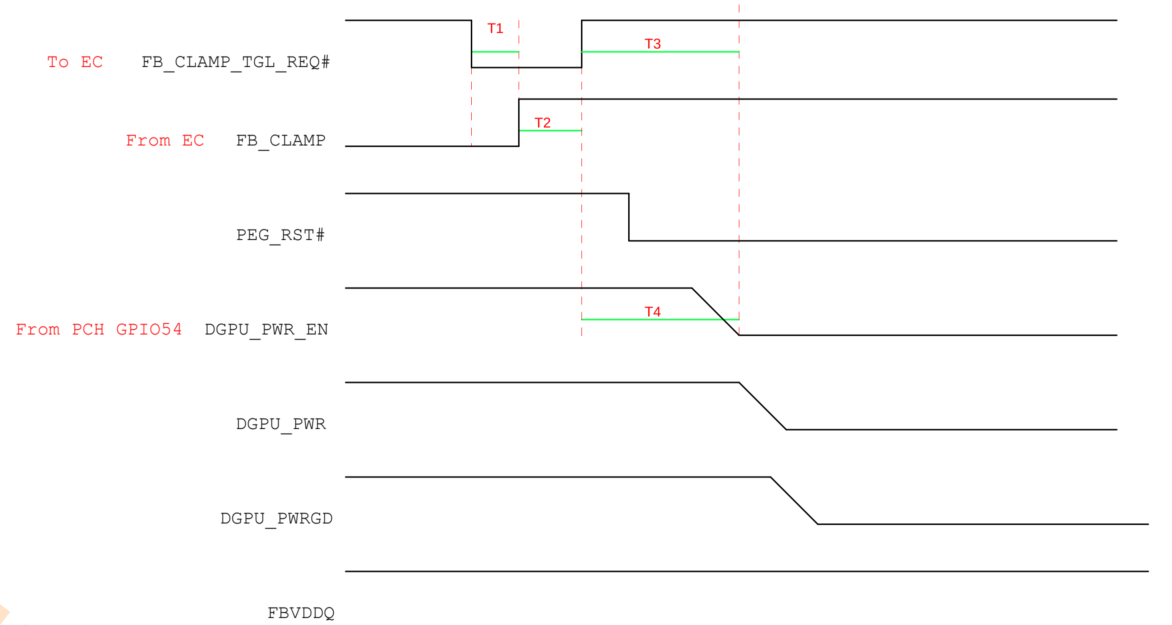


NOTES: The ramp time for any rail must be more than 40 us.
The total time for all rails to ramp up should be within 6ms.
A power rail has to ramp up to 90% before the next rail in sequence can start ramping up.
No signal should be applied to the GPU before the power rails are fully ramped

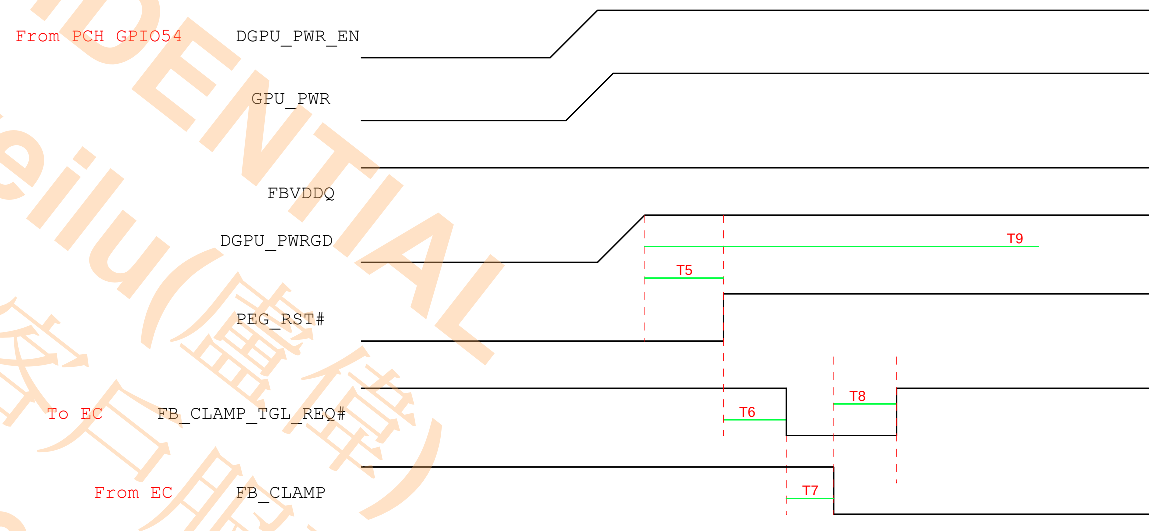
NOTES: For optimus system, VDD33 usually drops down earlier than NVVDD and FBVDDQ.

NOTES: All rails must be powered off within 10 ms from the first rail powering off.

GC6 ENTRY SEQUENCE(NOT support)



GC6 EXIT SEQUENCE



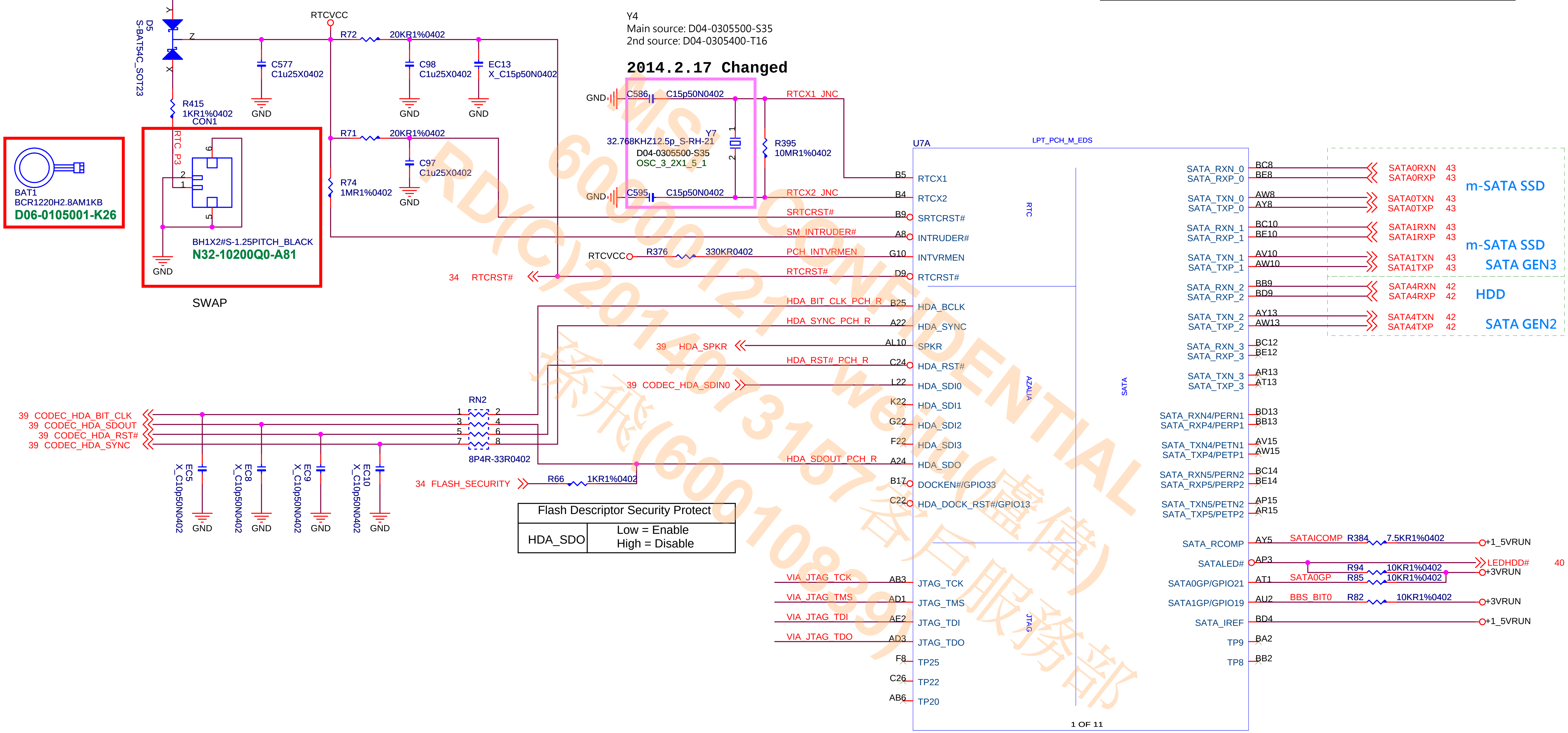
GC6 TIMING

	Min	Max	Unit	Description
T1	0	10	mS	GPU asserts toggle request to GB_CLAMP assertion
T2	0	1	mS	Assertion of FB_CLAMP to de-assertion of toggle request
T3	0	10	mS	De-assertion of toggle request to GPU PWR_EN=0
T4	0.01	1	mS	PEX reset assertion to GPU PWR_EN de-assertion
T5	0.1	5	mS	GPU power stable to de-assertion of PEX reset
T6	3.3		mS	De-assertion of PEX reset to toggle request assertion
T7	0	1	mS	Assertion of toggle request to de-assertion of FB_CLAMP
T8	0	1	mS	De-assertion of FB_CLAMP to de-assertion of toggle request
T9	TBD	TBD	mS	GPU power enable to GPU ready for normal operatioon

Notes: *System designers should minimize T1,T3,T4,T5,T6,and T7 to increase the time spent in GC6.
This increased GC6 residency will improve both power savings and user experience.
**If10 ms expirs for T1, the GPU will de-assert FB_CLAMP_TGL_REQ# and abort the GC6 entry procedure.
FB_CLAMP should never assert outside an FB_CLAMP_TGL_REQ# handshake.

Lynx Point (HDA/JTAG/SATA)

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3

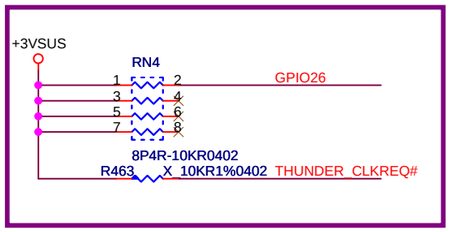


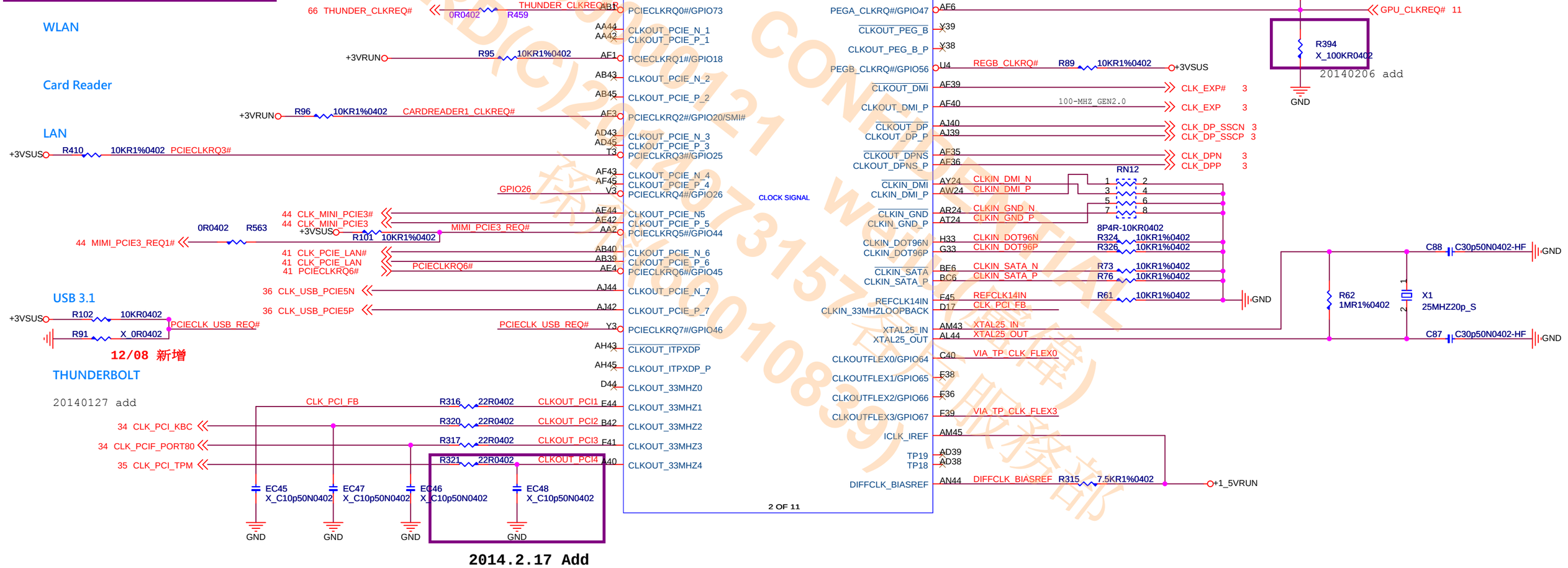
Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

SPK	The Signal has a weak internal pull-down Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)

Lynx Point (Clock)

PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 kΩ ±10% external pull-up resistor instead of No Connect.
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.





The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

MICRO-STAR INT'L CO.,LTD.		
Title: PCH-2 (CLK)		
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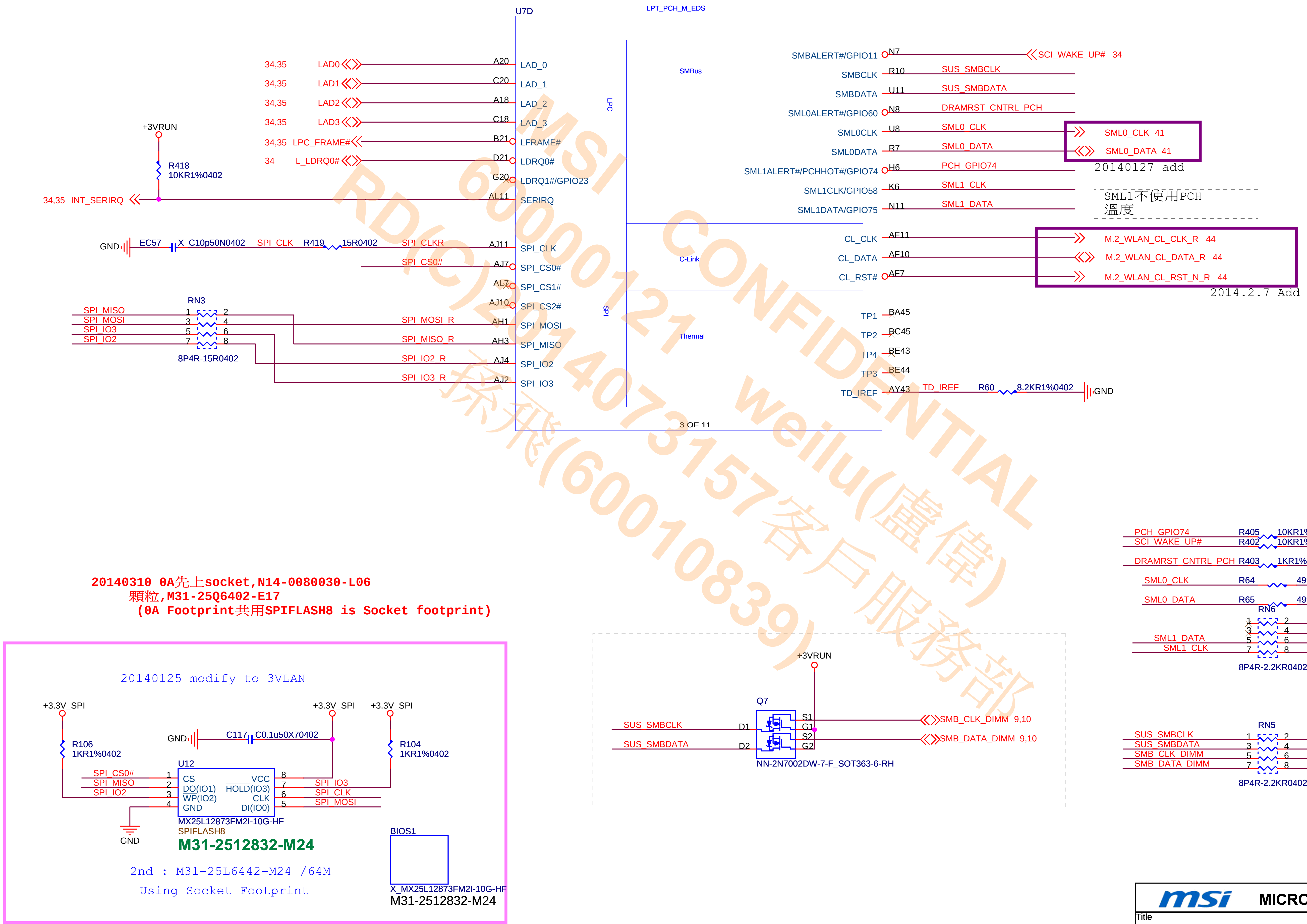
Lynx Point (LPC,SMBUS)



MICRO-STAR INT'L CO.,LTD.

Title	PCH-3 (LPC,SMBUS)	
Size	Document Number MS-16H3	Rev 1.0
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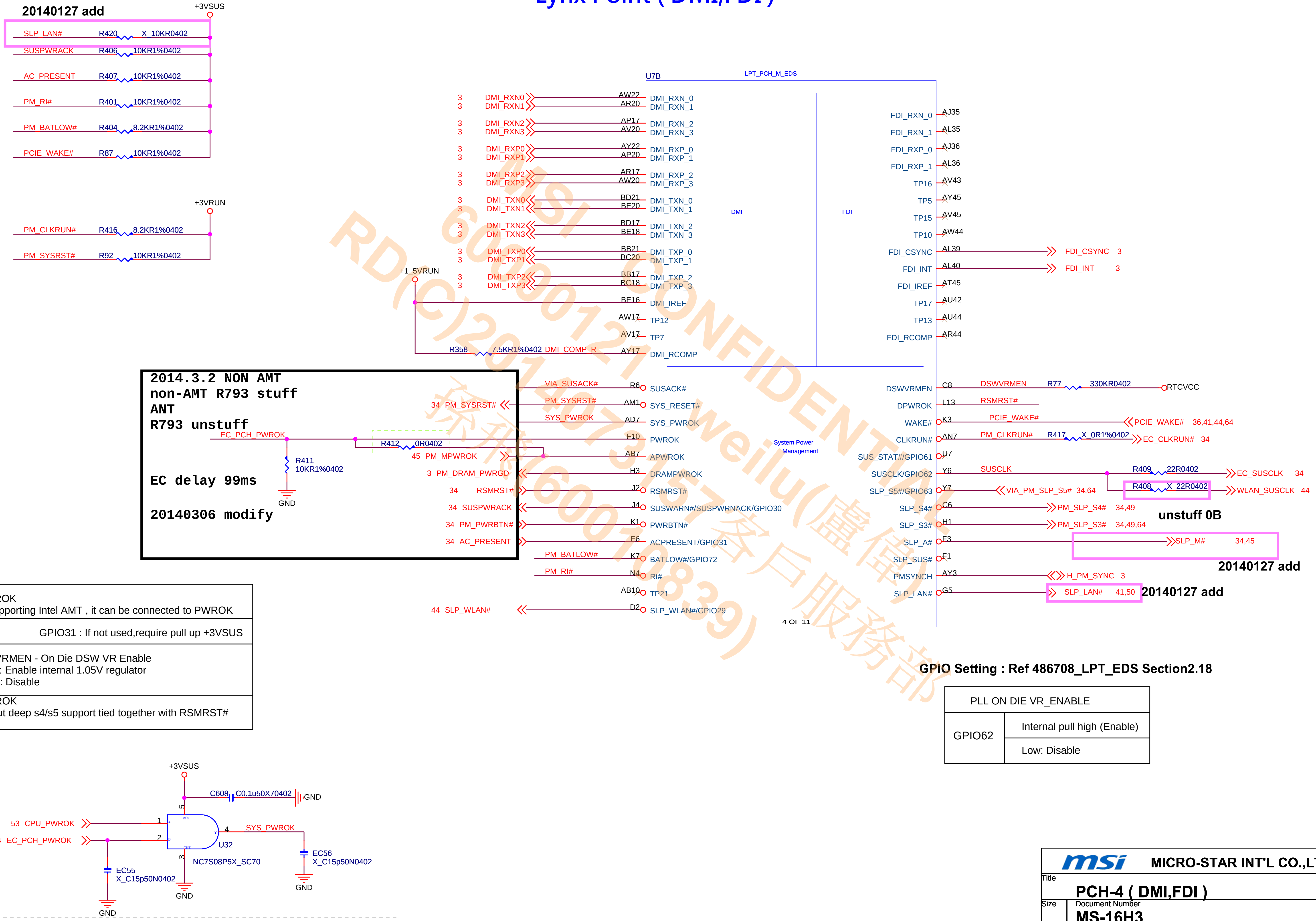
Lynx Point (DMI,FDI)



20140127 add
+3VSUS
SLP_LAN# R420 X_10KR0402
SUSPWRACK R406 10KR1%0402
AC_PRESENT R407 10KR1%0402
PM_RI# R401 10KR1%0402
PM_BATLOW# R404 8.2KR1%0402
PCIE_WAKE# R87 10KR1%0402
+3VRUN
PM_CLKRUN# R416 8.2KR1%0402
PM_SYSRST# R92 10KR1%0402
U7B LPT_PCH_M_EDS
DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3 DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3
DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3 DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3
DMI_IREF TP12 TP7 DMI_RCOMP
+1_5VRUN
R358 7.5KR1%0402 DMI_COMP_R
DMI FDI
FDI_RXN_0 FDI_RXN_1 FDI_RXP_0 FDI_RXP_1 TP16 TP5 TP15 TP10 FDI_CSYNC FDI_INT FDI_IREF TP17 TP13 FDI_RCOMP
FDI_CSYNC 3
FDI_INT 3
2014.3.2 NON AMT
non-AMT R793 stuff
ANT
R793 unstuff
EC delay 99ms
20140306 modify
EC_PCH_PWROK
R411 10KR1%0402
R412 0R0402
GND
VIA_SUSACK# 34 PM_SYSRST# SYS_PWROK 45 PM_MPWROK 3 PM_DRAM_PWRGD 34 RSMRST# 34 SUSPWRACK 34 PM_PWRBTN# 34 AC_PRESENT PM_BATLOW# PM_RI# 44 SLP_WLAN#
SUSACK# SYS_RESET# SYS_PWROK PWROK APWROK DRAMPWROK RSMRST# SUSWARN#/SUSPWRNACK/GPIO30 PWRBTN# ACPRESENT/GPIO31 BATLOW#/GPIO72 RI# TP21 SLP_WLAN#/GPIO29
System Power Management
DSWVRMEN DPWROK WAKE# CLKRUN# SUS_STAT#/GPIO61 SUSCLK/GPIO62 SLP_S5#/GPIO63 SLP_S4# SLP_S3# SLP_A# SLP_SUS# PMSYNCH SLP_LAN#
DSWVRMEN R77 330KR0402 RTCVCC
RSMRST#
PCIE_WAKE# 36,41,44,64
PM_CLKRUN# R417 X_0R1%0402 EC_CLKRUN# 34
SUSCLK R409 22R0402 EC_SUSCLK 34
R408 X_22R0402 WLAN_SUSCLK 44
VIA_PM_SLP_S5# 34,64
PM_SLP_S4# 34,49
PM_SLP_S3# 34,49,64
unstuff 0B
SLP_M# 34,45
20140127 add
H_PM_SYNC 3
SLP_LAN# 41,50
20140127 add
4 OF 11
+3VSUS
C608 C0.1u50X70402 GND
53 CPU_PWROK
6,34 EC_PCH_PWROK
SYS_PWROK
U32 NC7S08P5X_SC70
EC55 X_C15p50N0402
EC56 X_C15p50N0402
GND

APWROK not supporting Intel AMT , it can be connected to PWROK
GPIO31 : If not used,require pull up +3VSUS
DSWVRMEN - On Die DSW VR Enable HIGH : Enable internal 1.05V regulator LOW : Disable
DPWROK Without deep s4/s5 support tied together with RSMRST#

GPIO Setting : Ref 486708_LPT_EDS Section2.18

PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

MICRO-STAR INT'L CO.,LTD.

Title: PCH-4 (DMI,FDI)

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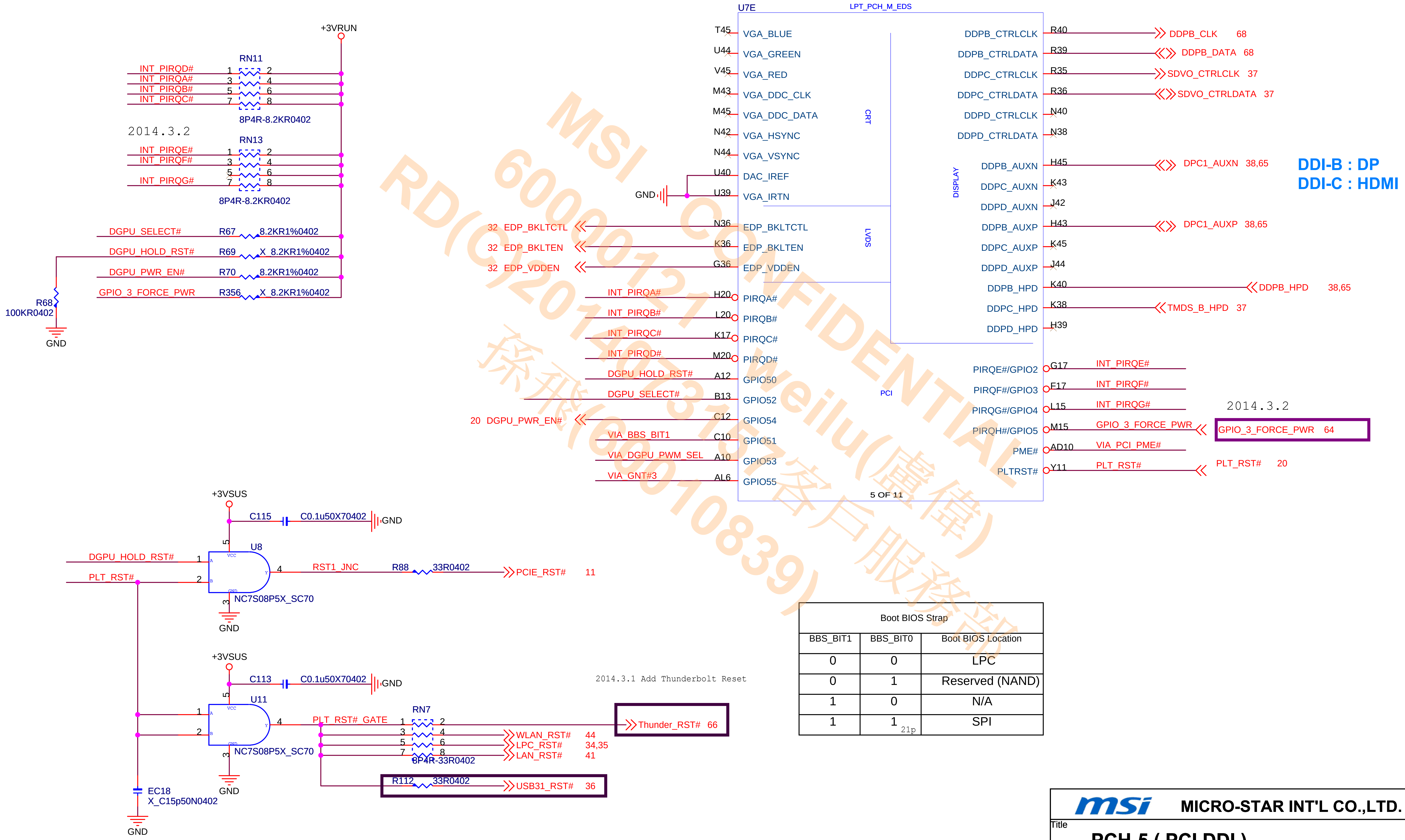
Lynx Point (PCI,DDI)



Boot BIOS Strap

BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

21p

MICRO-STAR INT'L CO.,LTD.

Title: PCH-5 (PCI,DDI)

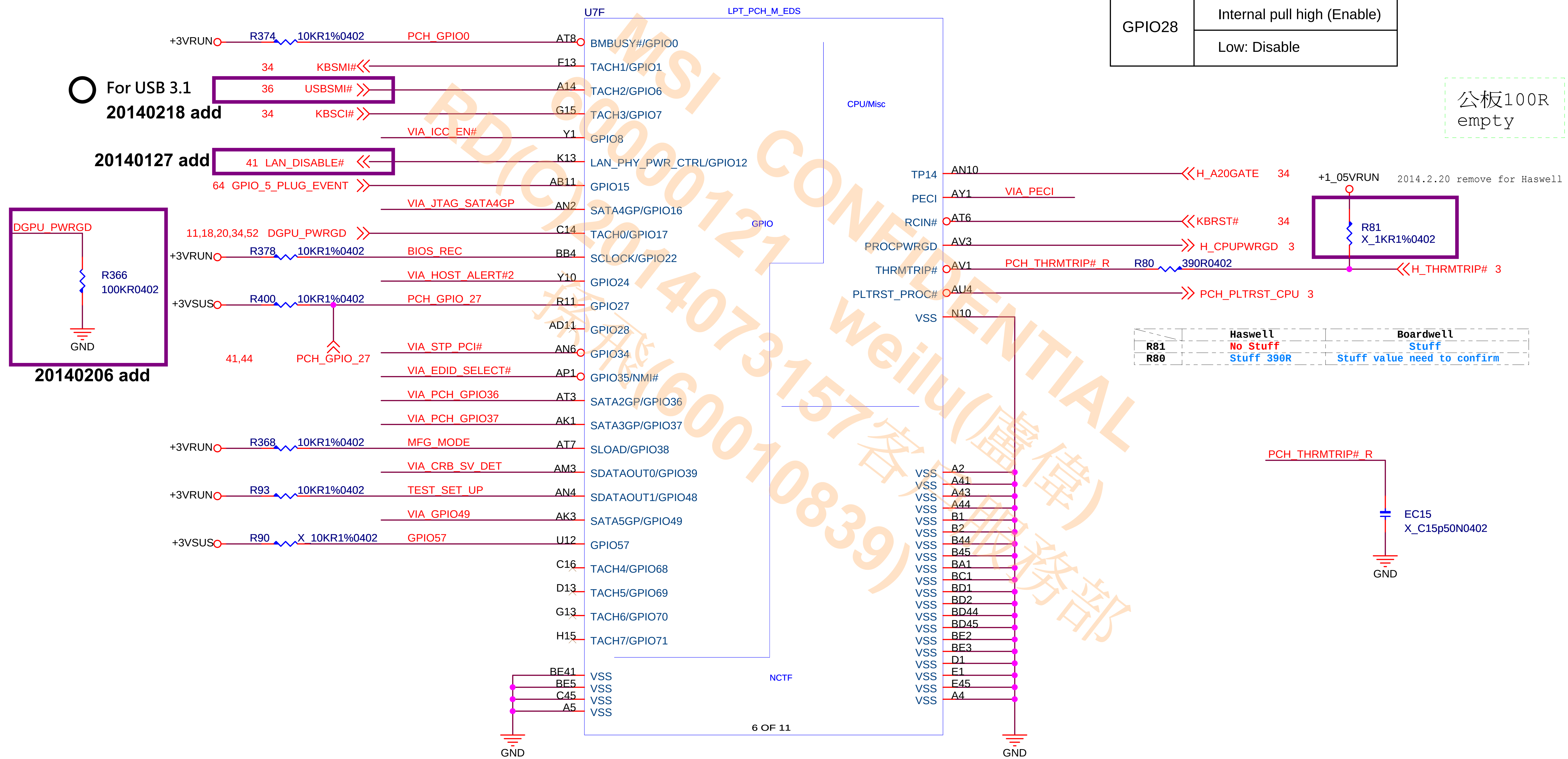
Size | Document Number: MS-16H3 | Rev 1.0

Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

公板100R
empty



U7F
LPT_PCH_M_EDS
+3VRUN R374 10KR1%0402 PCH_GPIO0 AT8 BMBUSY#/GPIO0
34 KBSMI# F13 TACH1/GPIO1
For USB 3.1
20140218 add
36 USBSMI# A14 TACH2/GPIO6
34 KBSCI# G15 TACH3/GPIO7
VIA_ICC_EN# Y1 GPIO8
20140127 add
41 LAN_DISABLE# K13 LAN_PHY_PWR_CTRL/GPIO12
64 GPIO_5_PLUG_EVENT AB11 GPIO15
VIA_JTAG_SATA4GP AN2 SATA4GP/GPIO16
DGPU_PWRGD
R366
100KR0402
GND
20140206 add
11,18,20,34,52 DGPU_PWRGD C14 TACH0/GPIO17
+3VRUN R378 10KR1%0402 BIOS_REC BB4 SCLOCK/GPIO22
VIA_HOST_ALERT#2 Y10 GPIO24
+3VSUS R400 10KR1%0402 PCH_GPIO_27 R11 GPIO27
AD11 GPIO28
41,44 PCH_GPIO_27
VIA_STP_PCI# AN6 GPIO34
VIA_EDID_SELECT# AP1 GPIO35/NMI#
VIA_PCH_GPIO36 AT3 SATA2GP/GPIO36
VIA_PCH_GPIO37 AK1 SATA3GP/GPIO37
+3VRUN R368 10KR1%0402 MFG_MODE AT7 SLOAD/GPIO38
VIA_CRB_SV_DET AM3 SDATAOUT0/GPIO39
+3VRUN R93 10KR1%0402 TEST_SET_UP AN4 SDATAOUT1/GPIO48
VIA_GPIO49 AK3 SATA5GP/GPIO49
+3VSUS R90 X_10KR1%0402 GPIO57 U12 GPIO57
C16 TACH4/GPIO68
D13 TACH5/GPIO69
G13 TACH6/GPIO70
H15 TACH7/GPIO71
BF41 BE5 C45 A5 VSS VSS VSS VSS
GND
GPIO
CPU/Misc
NCTF
6 OF 11
TP14 AN10 H_A20GATE 34
PECI AY1 VIA_PECI
RCIN# AT6 KBRST# 34
PROCPWRGD AV3 H_CPUPWRGD 3
THRMTRIP# AV1 PCH_THRMTRIP#_R R80 390R0402 H_THRMTRIP# 3
PLTRST_PROC# AU4 PCH_PLTRST_CPU 3
VSS N10
+1_05VRUN
2014.2.20 remove for Haswell
R81
X_1KR1%0402
VSS A2 A41 A43 A44 B1 B2 B44 B45 BA1 BC1 BD1 BD2 BD44 BD45 BE2 BE3 D1 E1 E45 A4
GND
PCH_THRMTRIP#_R
EC15
X_C15p50N0402
GND

	Haswell	Boardwell
R81	No Stuff	Stuff
R80	Stuff 390R	Stuff value need to confirm

msi MICRO-STAR INT'L CO.,LTD.

Title	PCH-6 (GPIO,MISC)	
Size	Document Number MS-16H3	Rev 1.0
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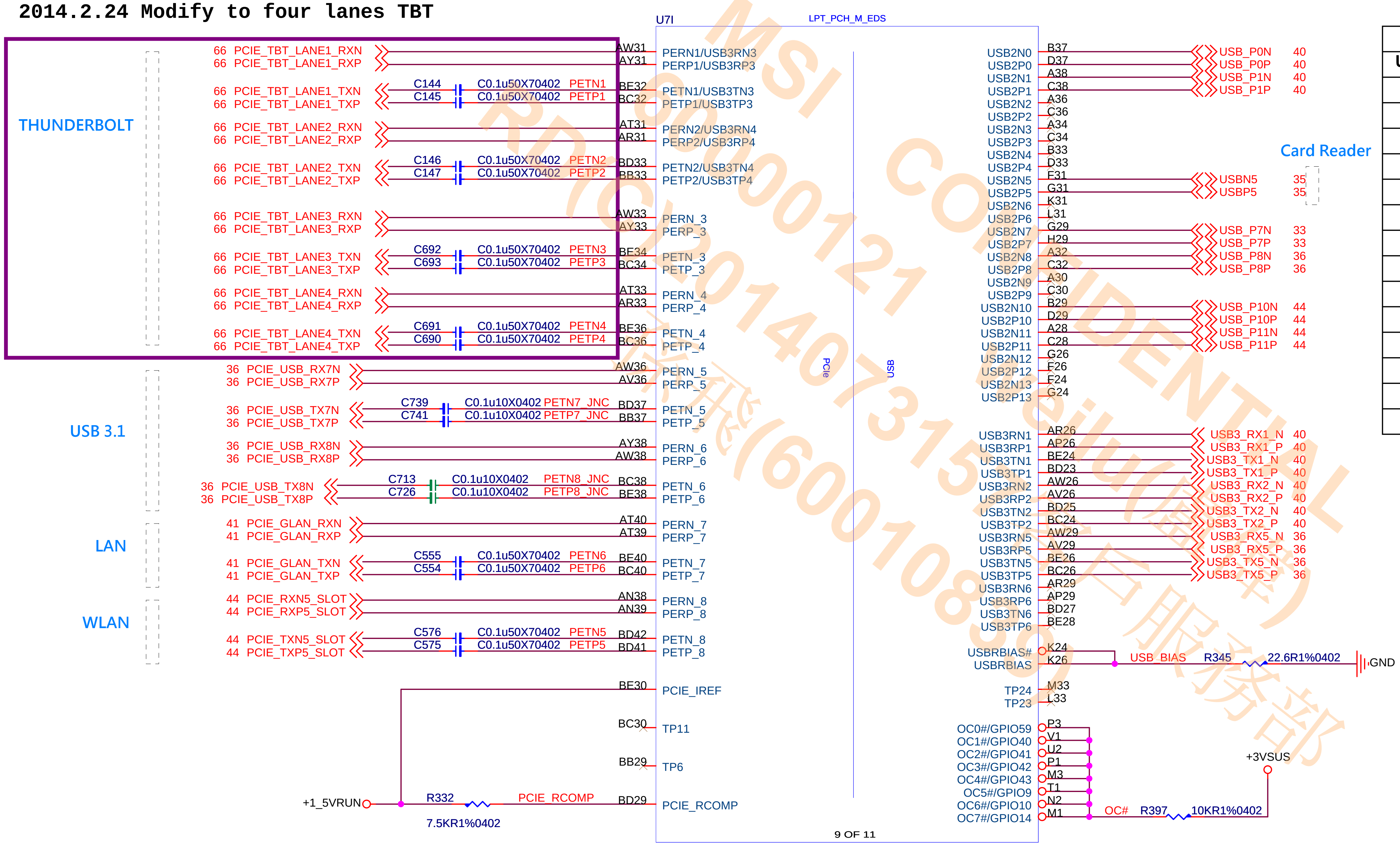
Lynx Point (PCIE,USB)

Intel Lynx Point ECHI USB(2.0) debug transport 需接Port1 or Port9

2014.2.24 Modify to four lanes TBT



USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	**16H3A**
1	2	USB 3.0 Port 2	**16H3A**
2			
3			NC
4			NC
5			NC
6			NC
7		EPF021	3 色KBC
8	3	USB 3.0 Port 5	**16H31**
9	4	USB 3.0 Port 6	**no use**
10		WLAN	
11		WebCam	
12		SECOND DISPLAY	
13			NC

HM86 沒USB3.0 PORT 5,6

MICRO-STAR INT'L CO.,LTD.

Title: PCH-7 (PCIE,USB)

Size | Document Number: MS-16H3 | Rev: 1.0

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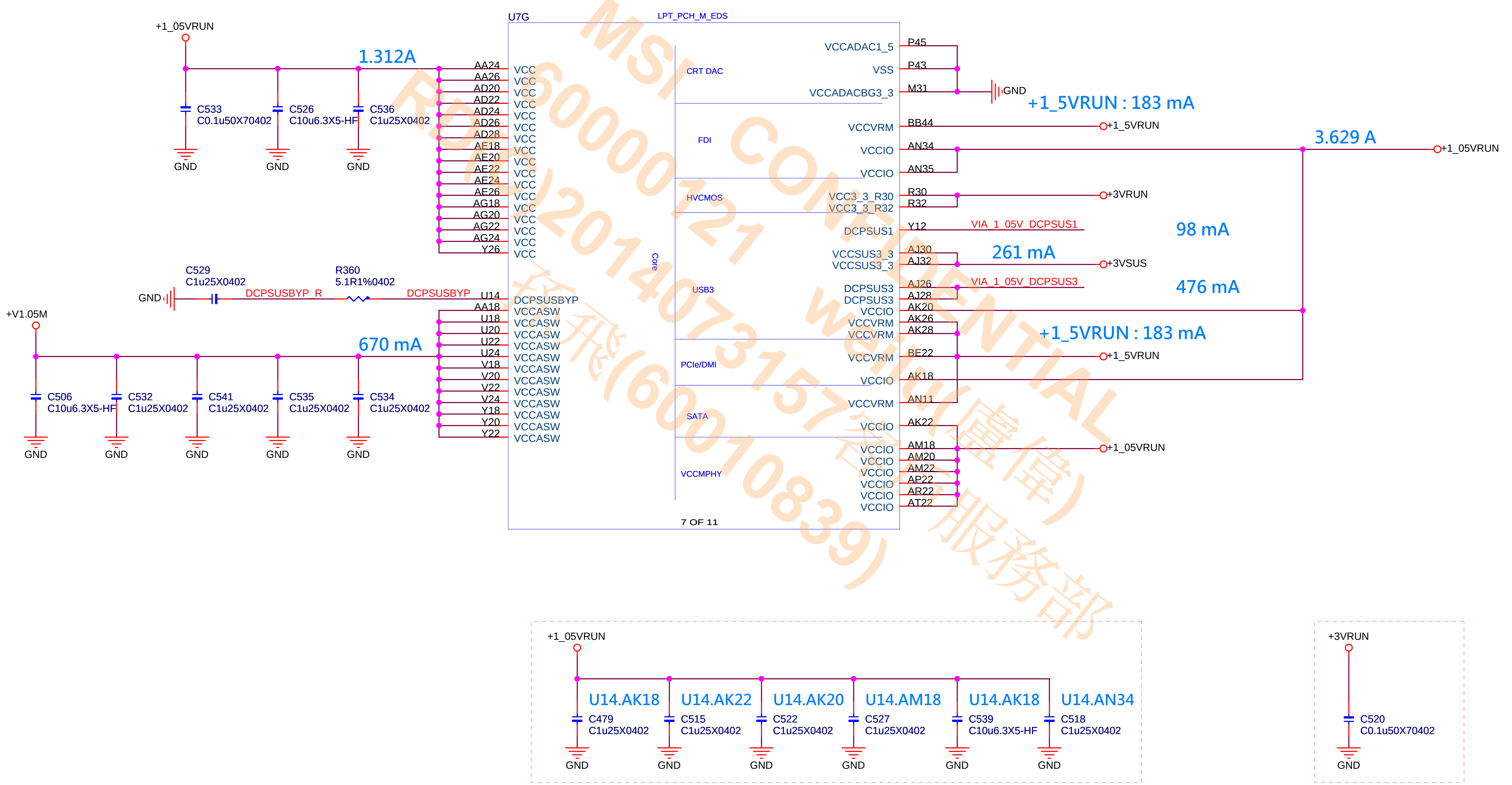
Lynx Point (Power)



MICRO-STAR INT'L CO.,LTD.

Title: PCH-8 (Power)

Size | Document Number: MS-16H3 | Rev 1.0

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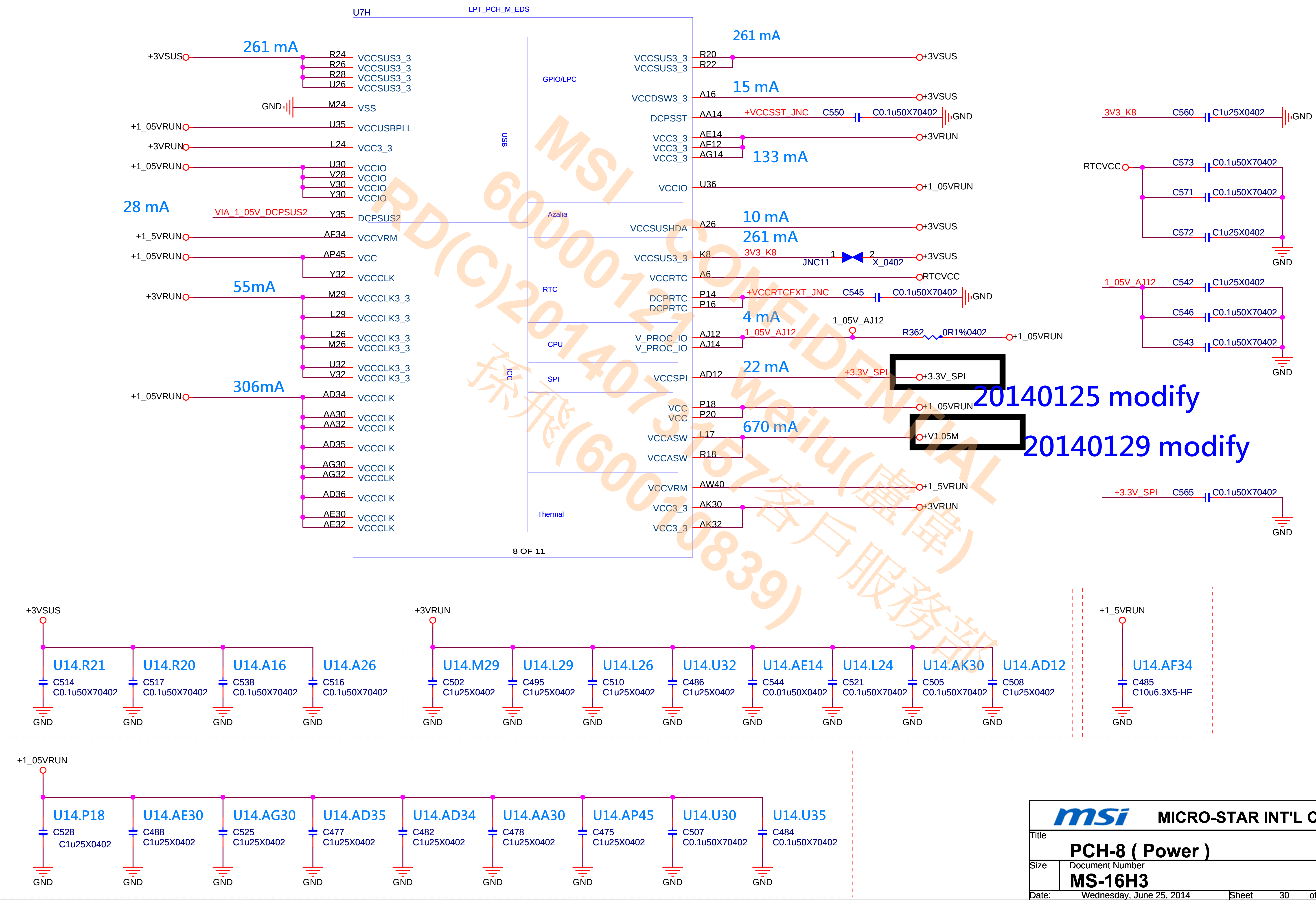
Lynx Point (Power)



msi MICRO-STAR INT'L CO.,LTD.

Title	PCH-8 (Power)
Size	Document Number: MS-16H3
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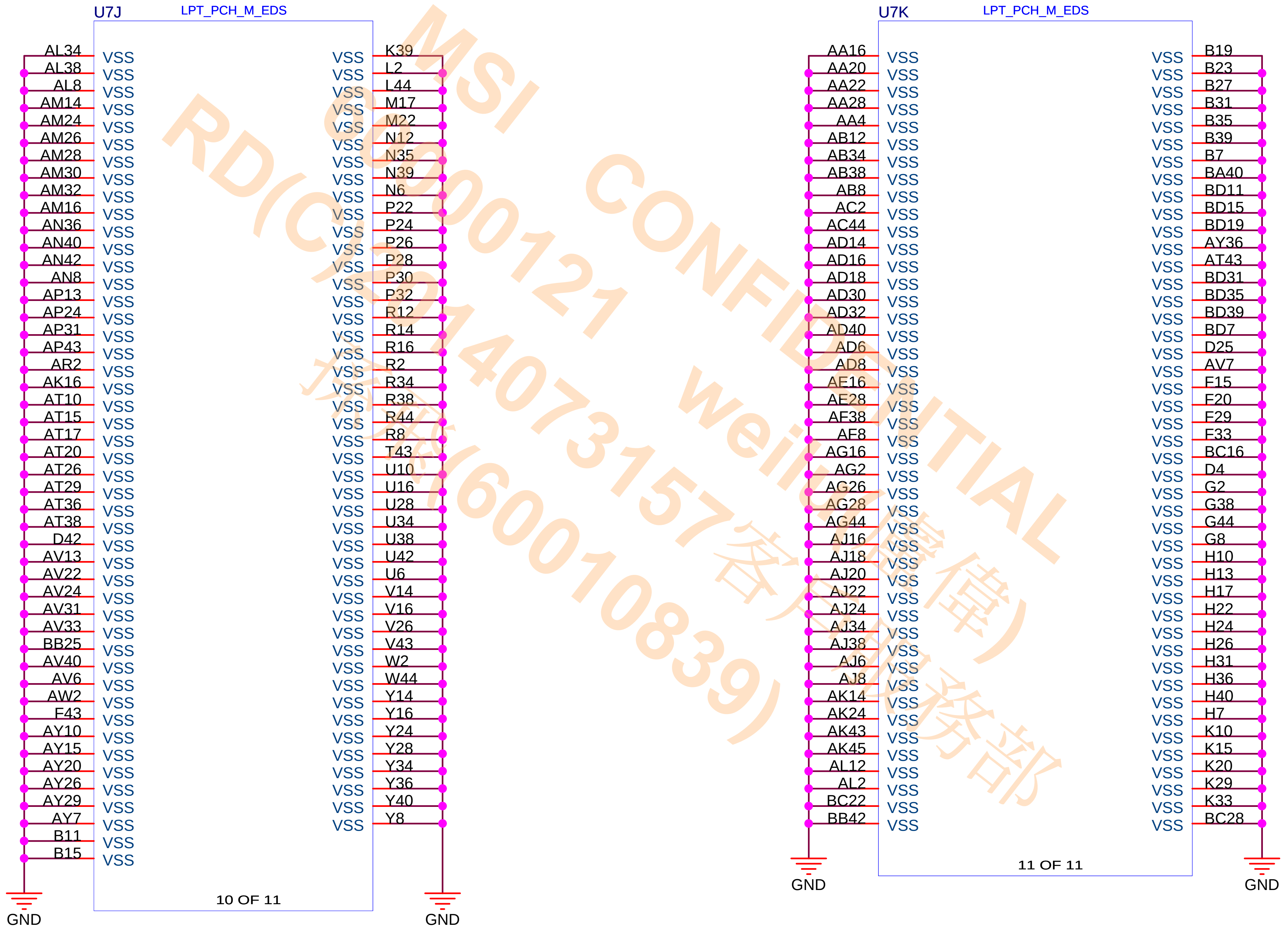
Lynx Point (GND)



MICRO-STAR INT'L CO.,LTD.

Title	PCH-8 (GND)	
Size	Document Number: MS-16H3	Rev 1.0
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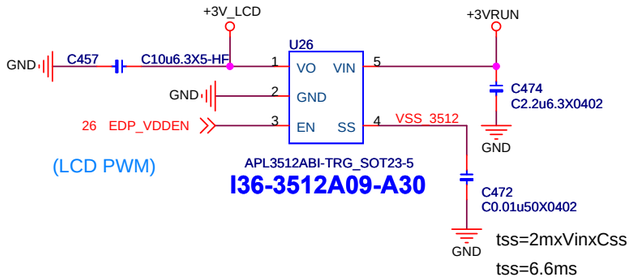
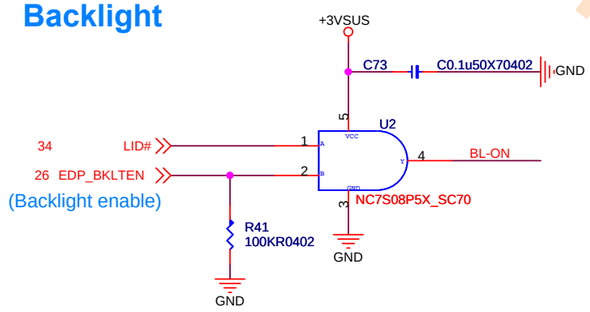
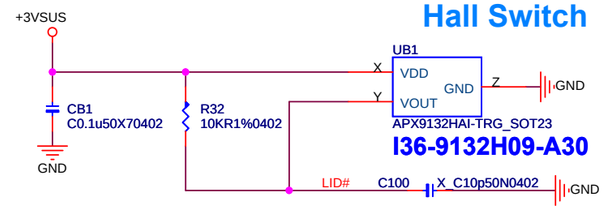
Pannel Device Logic Power



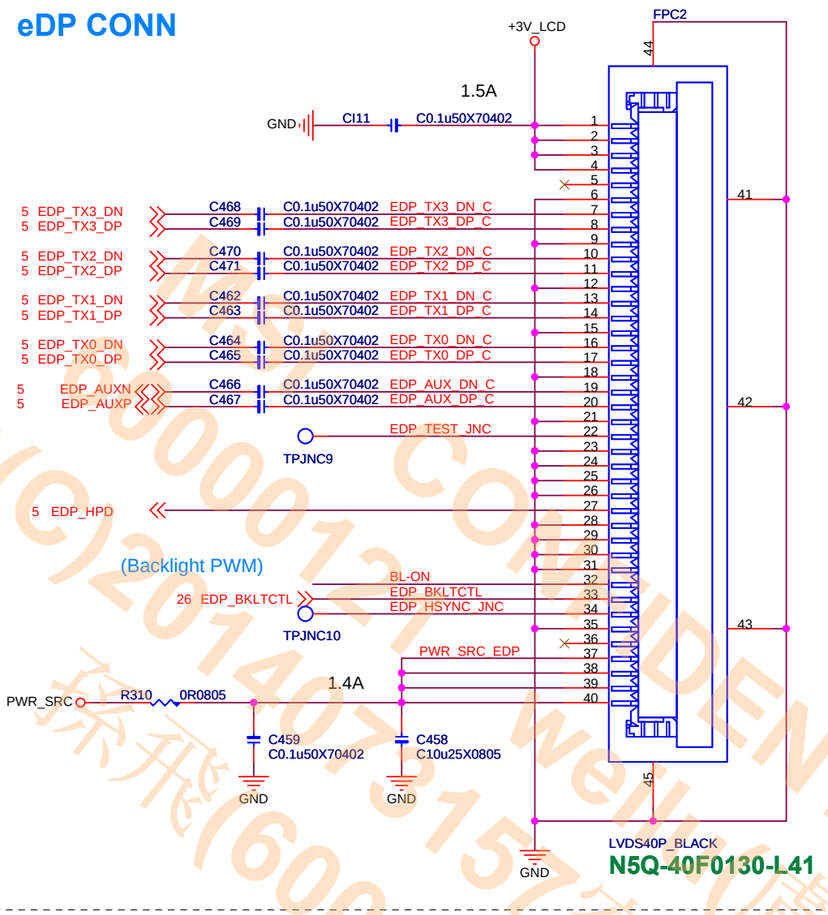
Backlight



Hall Switch

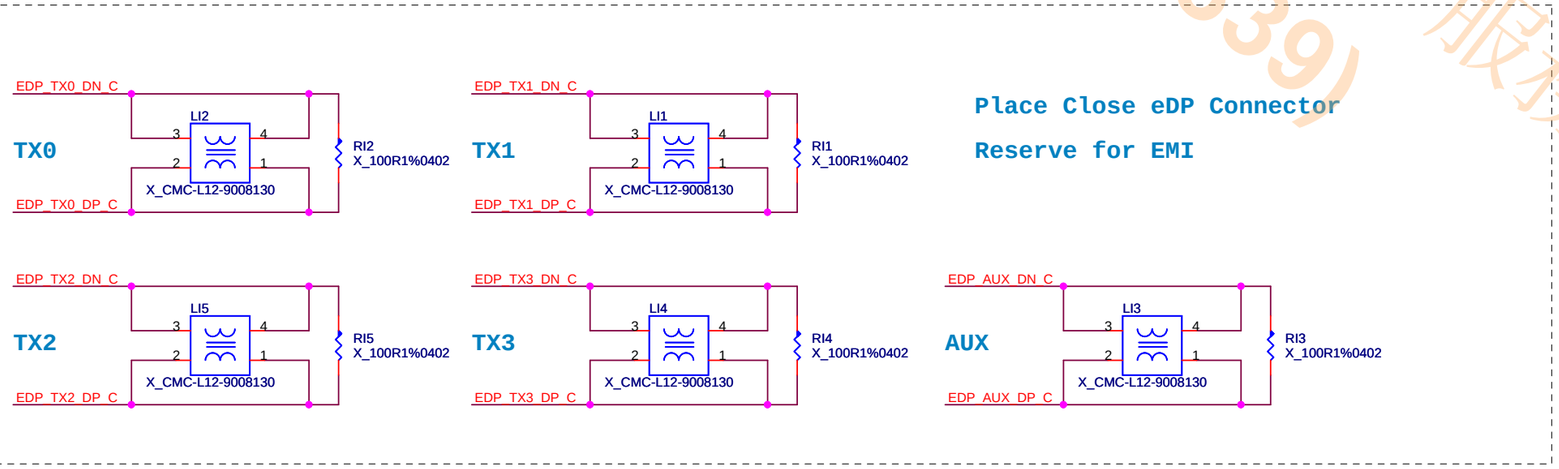


eDP CONN



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon



MICRO-STAR INT'L CO.,LTD.

Title: eDP switch & Conn/CAM/Lid

Size: Custom | Document Number: MS-16H3 | Rev: 1.0

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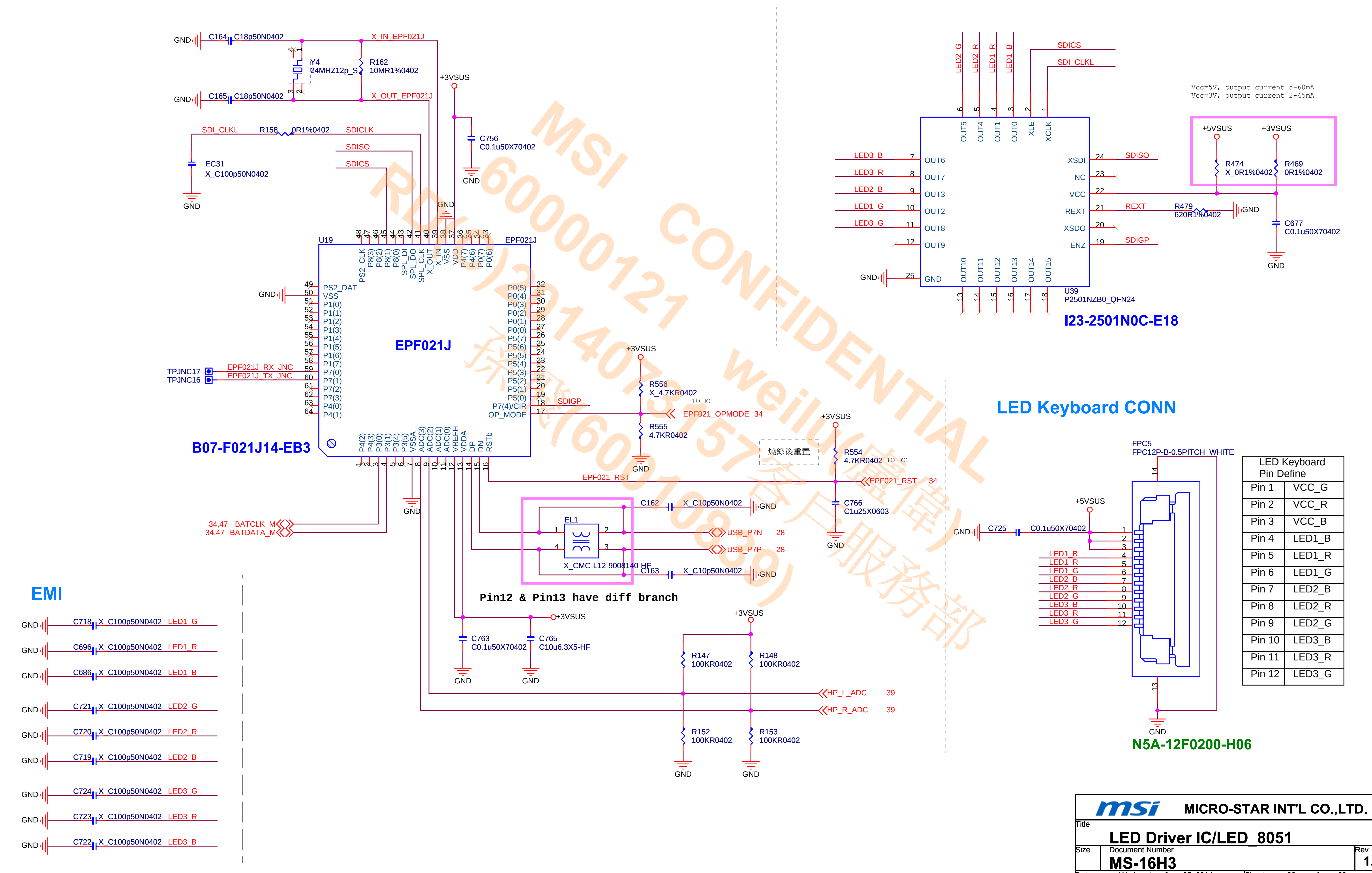
LED 8051 Controller



LED Keyboard Pin Define

Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

MICRO-STAR INT'L CO.,LTD.

Title: LED Driver IC/LED_8051

Document Number: MS-16H3 | Rev 1.0

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KBC(KB3930QFB1)

Hardware Reset

MEC1, MEC2, SW1 SW-TACTB1-4PS5, ED before RC, RST_SW#, R139 47KR1%0402, ED1 ESD-SFI0402-050E101NP, C149 C0.1u50X70402, GND, +3VALW

N71-0100560-D02

RC and R Close SW: R140 33R0402

EC_RST# 37 → ECRST#

27 KBRST# → KBRST# 2
27 KBSCI# → KBSCI# 20
27 H_A20GATE → GA20 1
26,35 LPC_RST# → PCIRST# 13

40 UMA_ON# → PWM0/GPIO0F 21
47 AC_CTL → PWM1/GPIO10 23
GPIO11/PWM2 25
22 FLASH_SECURITY → GPIO19/PWM3 34
40 FAN1_PWM0 → FANPWM0/GPIO12 26
43 FAN1_PWM1 → FANPWM1/GPIO13 27
40 CPUFAN_FB → FANFB0/GPIO14 28
43 GPUFAN_FB → FANFB1/GPIO15 29

SW Debug (LPC)

CON5 BH1X14#S-1PITCH N32-1140130-H06

LPC_FRAME# 1, LAD3 2, LAD2 3, LAD1 4, LAD0 5
24 L_LDRQ0# 6
23 CLK_PCIF_PORT80 7
INT_SERIRQ 8
LPC_RST# 9
GND C684 X_C10p50N0402
+5VRUN 10
+3VRUN 11
GND R500 X_10KR1%0402 FWH_ID0 12 13 14
15 16 GND

2014.3.3 add

18 FB_CLMP_TGL_REQ# → R552 X_0R0402 → FB_CLMP_TGL_REQ# EC
Q23 X_N-BSS138_SOT23 (D, S, G)
R538 X_10KR0402 → +3V3_NV
R528 10KR0402 → +3VRUN

U17

LPC I/F

24,35 INT_SERIRQ → SERIRQ 3
24,35 LPC_FRAME# → LFARAME# 4
23 CLK_PCI_KBC → PCICLK 12
25 EC_CLKRUN# → CLKRUN#/GPIO1D 38
24,35 LAD0 → LAD0 10
24,35 LAD1 → LAD1 8
24,35 LAD2 → LAD2 7
24,35 LAD3 → LAD3 5

POWER/GROUND

VCC 9, 22, 33, 96, 111, 125
AVCC 67 (EC_AVCC)
AGND 69
GND 11, 24, 35, 94, 113

+3VALW
C761 C0.1u50X70402 GND
C169 C0.1u50X70402 GND
L2 80L700mA-150
C151 C0.1u50X70402
C150 C10u6.3X5-HF
C156 C0.1u50X70402
C752 C0.1u50X70402
C152 C0.1u50X70402
+3VALW
GND

SMBUS

SDA0/GPIO45 78 → BATDATA_M 33,47
SCL0/GPIO44 77 → BATCLK_M 33,47
SDA1/GPIO47 80 → SMB_DATA_EC 18
SCL1/GPIO46 79 → SMB_CLK_EC 18

AD/DA

DA0/GPO3C 68 → EPF021_RST 33
DA1/GPO3D 70 → EPF021_OPMODE 33
DA2/GPO3E 71 → DGPU_ON# 40
DA3/GPO3F 72 → CTL1_EC 36
AD0/GPI38 63 → FBVDDQ_ON 20,52
AD1/GPI39 64 ← MB_ID
AD2/GPI3A 65 → ADP_ICC 47
AD3/GPI3B 66 → SUSPWRACK 25
AD4/GPI42 75 → AC_OK# 47
AD5/GPI43 76 → BAT_IN# 47

SDI

GPXIOA00/SDICS# 97 → AC_PRESENT 25
GPXIOA01/SDICLK 98 → SUS_ON 46,48
GPXIOA02/SDIMOSI 99 → RSMRST# 25

IKB

KBOUT0 39 … KBOUT17 82 → KSO00/GPIO20/TP_TEST … KSO17/GPIO49

KBIN0 55 … KBIN7 62 → KSI0/GPIO30/E51TXD(ISP) … KSI7/GPIO37/EDI_DO

GPXIOA03 100 → DIMM_ON 49
GPXIOA04 101 → RUN_ON 46,48,50
GPXIOA05 102 → EC_PCH_PWROK 6,25
GPXIOA06 103 → BATLOW_N 64
GPXIOA07 104 → WLAN_PWRON 44
GPXIOA08 105 → LED_ACPI# 40
GPXIOA09 106 → LED_CHARGE# 40
GPXIOA10 107 → LED_BATLOW# 40
GPXIOA11 108 → LED_BLUETOOTH# 40
GPXIOD0 109 → SUSPWROK 48
GPXIOD1 110 → PM_SLP_S4# 25,49
GPXIOD2 112 → PM_SLP_S3# 25,49,64
GPXIOD3 114 ← EC_ALLSYSPG
GPXIOD4 115 → PWR_SW# 40
GPXIOD5 116 → SCI_WAKE_UP# 24
GPXIOD6 117 → LID# 32
GPXIOD7/PECI 118 → H_PECI 3
R535 43R0402 H_PECI_R
C751 X_C47p50N0402 GND

ESB

39,40 EC_MUTE# → GPIO0B/ESB_CLK 17
47 BAT_BM# → GPIO0C/ESB_DAT_O/ESB_DAT_I 18

CIR

39 EAPD → GPIO40/CIR_RX/AD6 73
GPIO41/CIR_RLC_TX/AD7 74
GPIO0A/RLC_RX2 16
12,18,20 FB_CLAMP → GPIO0D/RLC_TX2 19

SPI FLASH

EC_RD# 119
EC_WR# 120
EC_SPI_CLK 126
EC_CS# 128
MISO
MOSI
SPICLK/GPIO58
SPICS#

PS2 I/F

44 TP_CLK → PSCLK2/GPIO4E 87
44 TP_DATA → PSDAT2/GPIO4F 88
36 CTL2_EC → PSCLK1/GPIO4C 85
36 CTL3_EC → PSDAT1/GPIO4D 86
3 EC_PROCHOT# → PSCLK0/GPIO4A/P80CLK 83
36,40 USB_ENABLE → PSDAT0/GPIO4B/P80DAT 84

UART

TPJNC15 → E51TXD_JNC 30 → E51TXD/GPIO16
TPJNC14 → E51RXD_JNC 31 → E51RXD/GPIO17

LED

GPIO04 6
GPIO07/i_clk_8051 14 → GPU_ACIN1 18
GPIO08/i_clk_peri 15 → DGPU_PWRGD 11,18,20,27,52
GPIO18 32 → KBSMI# 27
GPIO50 89
E51CS#/GPIO52 90 → BATT_OFF 47
E51TMR0/GPIO54/WDT_LED# 92 → LED_WLAN# 40
E51INT1/GPIO56 95 → PM_PWRBTN# 25
GPIO57/XCLK32K 121 → BT_PWR_ON 44
GPIO59/TEST_CLKSPICLKI 127 → CAMERA_ON# 44

GPIO1A/NUMLED# 36 → LED_NUM# 40
E51TMR1/GPIO53/CAPSLED# 91 → LED_CAP# 40
E51INT0/GPIO55/SCROLED# 93 ← SCROLED# JNC → TPJNC18

KB3930QFB1

2014.3.2 DELETE, then add it.

Pin 105-108 8mA-16mA Sink

2014.2.7 新增

Pin 92 16mA-20mA Sink

Pin 39,91 16mA-20mA Sink

B02-0393024-E18

XCLK

25 EC_SUSCLK → R168 0R1%0402 → EC_XIN 122, EC_XOUT 123
R169 680KR0402 GND
ER2 X_22R0402 SUSCLK_RC
C175 X_C22p50N0402 GND
R167 X_10MR1%0402
Y5 X_32.768KHZ12.5p
EC_XOUT_JNC
C170 X_C18p50N0402 GND
C171 X_C18p50N0402 GND
V18R 124
C748 C4.7u10X0603 GND

MB_ID

+3VALW
PR70 X_100KR0402
MB_ID
R141 10KR1%0402 GND

MB_ID=1=AMT
MB_ID=0=non-AMT

Keyboard conn

CON6 FPC26P-B-1PITCH_BLACK N5A-26F0340-H06

KBOUT17 26, KBOUT16 25, KBIN0 24, KBIN1 23, KBIN2 22, KBIN3 21, KBIN4 20, KBIN5 19, KBIN6 18, KBIN7 17, KBOUT15 16, KBOUT14 15, KBOUT13 14, KBOUT12 13, KBOUT11 12, KBOUT10 11, KBOUT9 10, KBOUT8 9, KBOUT7 8, KBOUT6 7, KBOUT5 6, KBOUT4 5, KBOUT3 4, KBOUT2 3, KBOUT1 2, KBOUT0 1

CNI4 8P4C-100p50N0402
KBOUT0 1, KBOUT1 3, KBOUT2 5, KBOUT3 7

CNI3 8P4C-100p50N0402
KBOUT4 1, KBOUT5 3, KBOUT6 5, KBOUT7 7

CNI1 8P4C-100p50N0402
KBOUT8 1, KBOUT9 3, KBOUT10 5, KBOUT11 7

CNI2 8P4C-100p50N0402
KBOUT12 1, KBOUT13 3, KBOUT14 5, KBOUT15 7

KBOUT17 CI14 C100p50N0402
KBOUT16 CI13 C100p50N0402

FLASH/ME DEBUG MODE STRAP

20140311 add

25,64 VIA_PM_SLP_S5# → TPJNC32
22 RTCRST# → TPJNC11
25 PM_PWRBTN# → TPJNC19
25 PM_SYSRST# → TPJNC12

FOR APS TOOL

APS1 X_H2X3M_BLACK-RH
25,45 SLP_M#
25,49,64 PM_SLP_S3#
25,49 PM_SLP_S4#
+3VALW, +3VSUS, +3VSUS

MP remove

ROM

+3VALW
C158 C0.1u50X70402 GND
R172 2.2KR1%0402 WP# EC_ROM
R173 10KR1%0402
U20 MX25L512EMI-10G
SPI_HOLD#
EC_SPICLK
EC_WR#
EC_CS#
EC_RD#
M31-2551222-M24

EC_SPI_CLK ER1 22R0402 EC_SPICLK EC32 C22p50N0402 GND

ALLSYSPG

+3VRUN
R542 10KR1%0402
50 +1_5VRUN_PWRGD → JNC15 X_0402
45 +1_05VRUN_PWRGD → R527 X_0R1%0402
3/2 AMT
49 +1_35VDIMM_PWRGD → JNC14 X_0402 → EC_ALLSYSPG 53
50 +1_05V_PWRGD → X_R2 0R1%0402
3/2 non AMT

	non AMT	AMT
R527	No Stuff	Stuff
R2	Stuff	No Stuff
	Stuff	No Stuff
	No Stuff	Stuff
	No Stuff	Stuff

PU/PD

+3VALW
BATCLK_M R145 2.2KR1%0402
BATDATA_M R146 2.2KR1%0402
+3VRUN
SMB_CLK_EC R149 2.2KR1%0402
SMB_DATA_EC R151 2.2KR1%0402

KBRST#, H_A20GATE

KBRST# R159 X_100KR0402
RSMRST# R84 10KR1%0402
GND

msi	MICRO-STAR INT'L CO.,LTD.		
Title	KBC(KB3930QFB1)		
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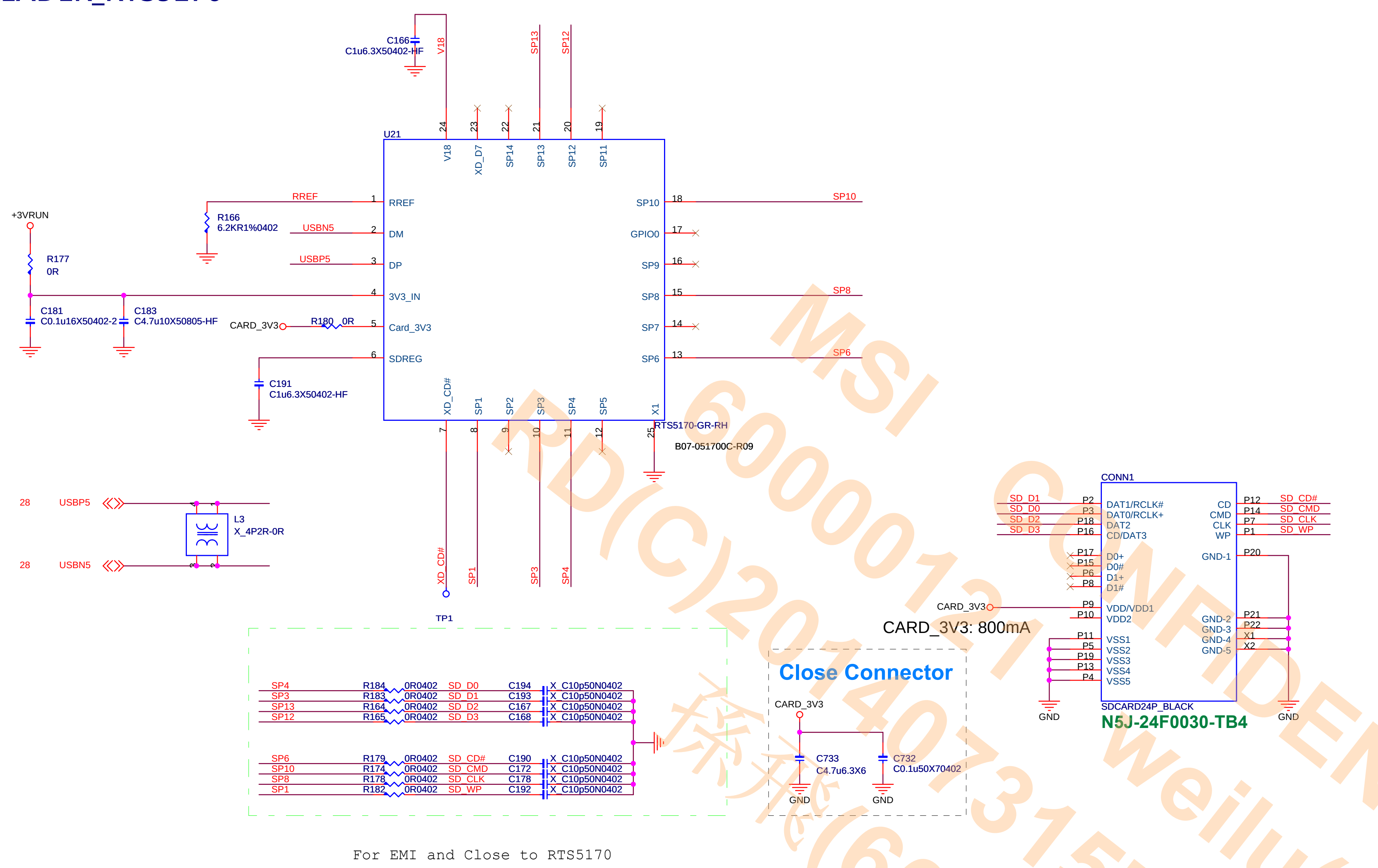
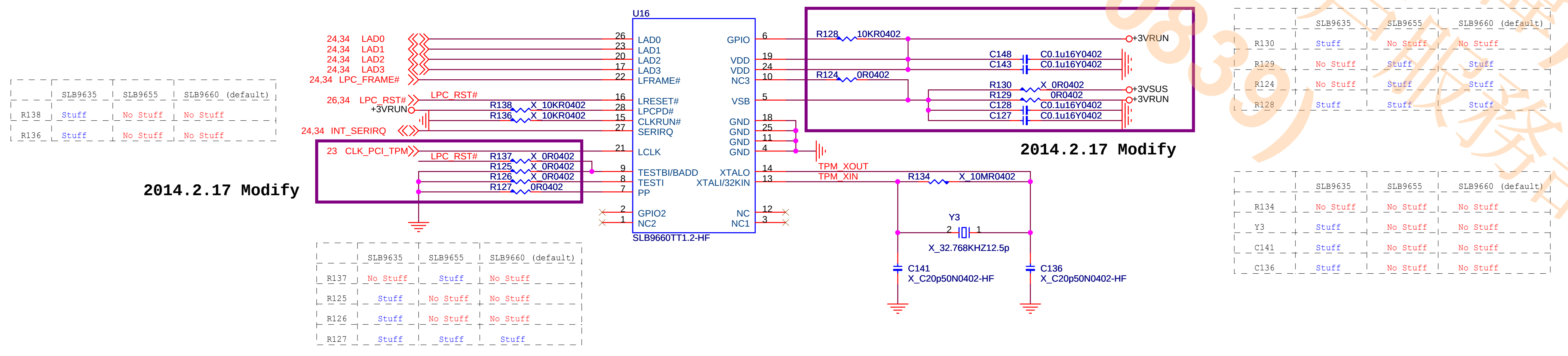
CARD READER_RTS5170



Pin#	Name	I/O Type	Description
1	RREF	I	Connect external resistor (6.2K ± 1%) to reference ground
2	DM	I/O	USB D- signal
3	DP	I/O	USB D+ signal
4	3V3_IN	I	3.3V power input
5	CARD_3V3	O	3.3V power for all cards
6	SDREG	O	Internal regulator for SD card. An external capacitor should be connected
7	XD_CD#	I	xD Card Detect (xD_CD#)
8	SP1	I/O	xD Ready Signal (xD_RDY), SD Write Protect (SD WP) and MS Clock (MS_CLK)
9	SP2	I/O	xD RE# and MS Card Detect (MS_INS#)
10	SP3	I/O	xD CE# and SD Data 1 (SD_DAT1)
11	SP4	I/O	xD_CLE, SD Data 0 (SD_DAT0) and MS Data 7 (MS_D7)
12	SP5	I/O	xD ALE, SD Data 7 (SD_DAT7) and MS Data 3 (MS_D3)
13	SP6	I/O	xD_WE# and SD Card Detect (SD_CD#)
14	SP7	I/O	xD Write Protect (xD_WP), SD_Data 6 (SD_DAT6) and MS Data 6 (MS_D6)
15	SP8	I/O	xD Data 0 (xD_D0), SD Clock (SD_CLK) and MS Data 2 (MS_D2)
16	SP9	I/O	xD Data 1 (xD_D1), SD Data 5 (SD_D5) and MS Data 0 (MS_D0)
17	GPIO0	I/O	General purpose input/output with interrupt ability
18	SP10	I/O	xD Data 2 (xD_D2) and SD command signal (SD_CMD)
19	SP11	I/O	xD Data 3 (xD_D3), SD Data 4 (SD_DAT4) and MS Data 4 (MS_D4)
20	SP12	I/O	xD Data 4 (xD_D4), SD Data 3 (SD_DAT3) and MS Data 1 (MS_D1)
21	SP13	I/O	xD Data 5 (xD_D5), SD Data 2 (SD_DAT2) and MS Data 5 (MS_D5)
22	SP14	I/O	xD Data 6 (xD_D6) and MS BS
23	XD_D7	I/O	xD Data 7 (xD_D7)
24	V18	O	Regulated supply voltage (1.8V ±10%) from internal 3.3V to 1.8V regulator; supplies internal digital circuits. An external capacitance should be connected

TPM



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Title	Card Reader & TPM
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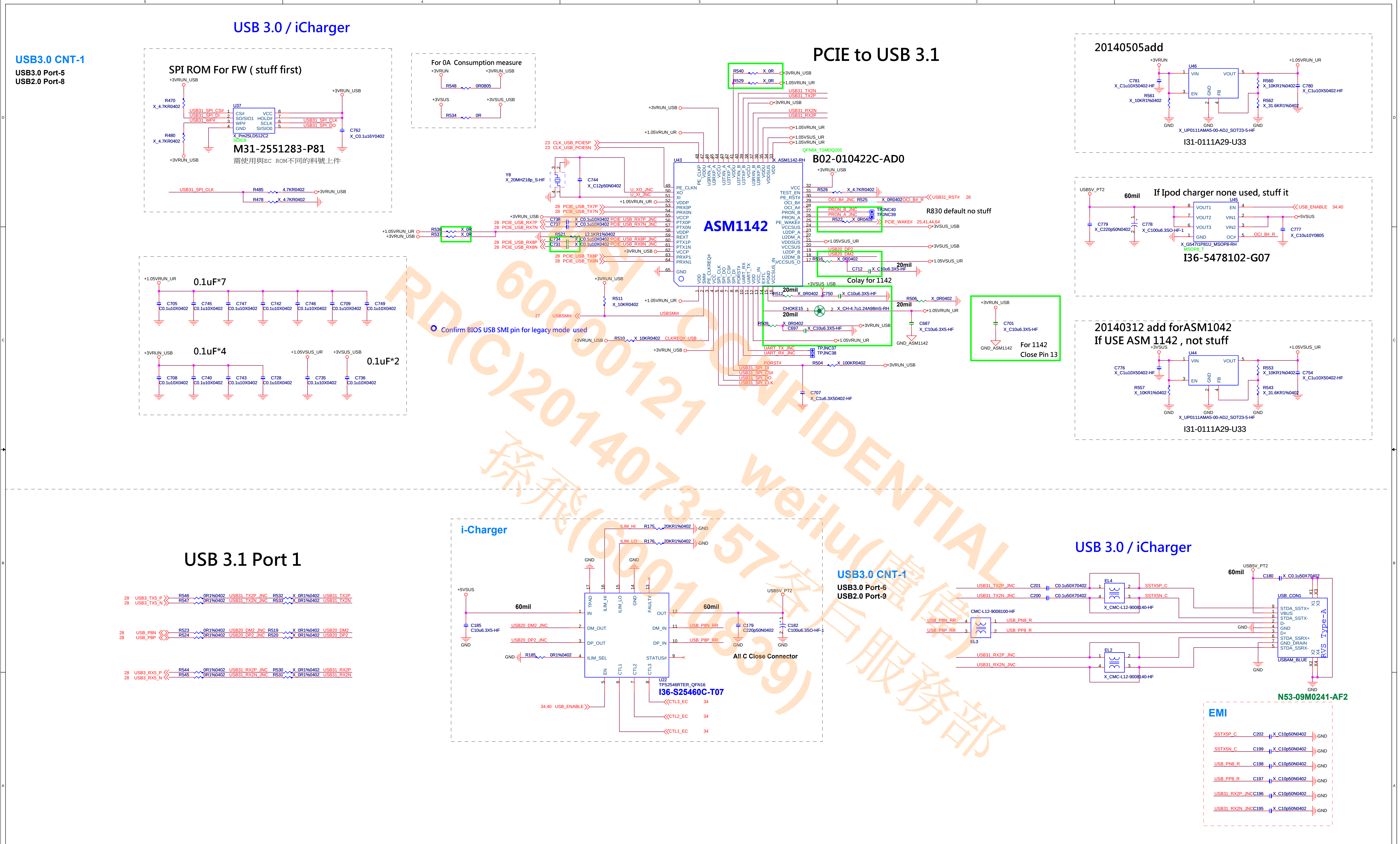
USB 3.0 / iCharger



MICRO-STAR INT'L CO.,LTD.

Title: USB 3.0 / iCharger

Size | Document Number: MS-16H3 | Rev: 1.0

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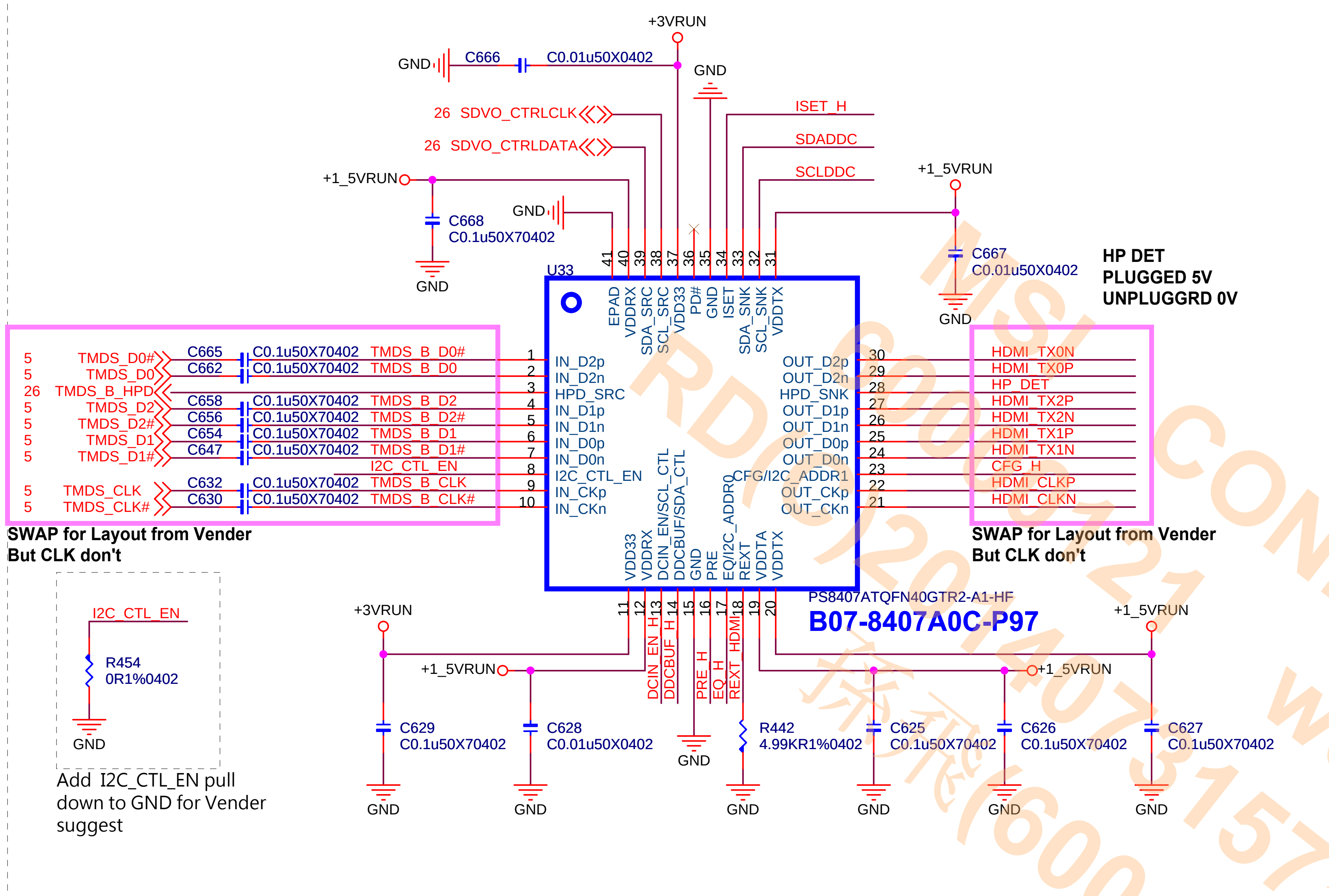
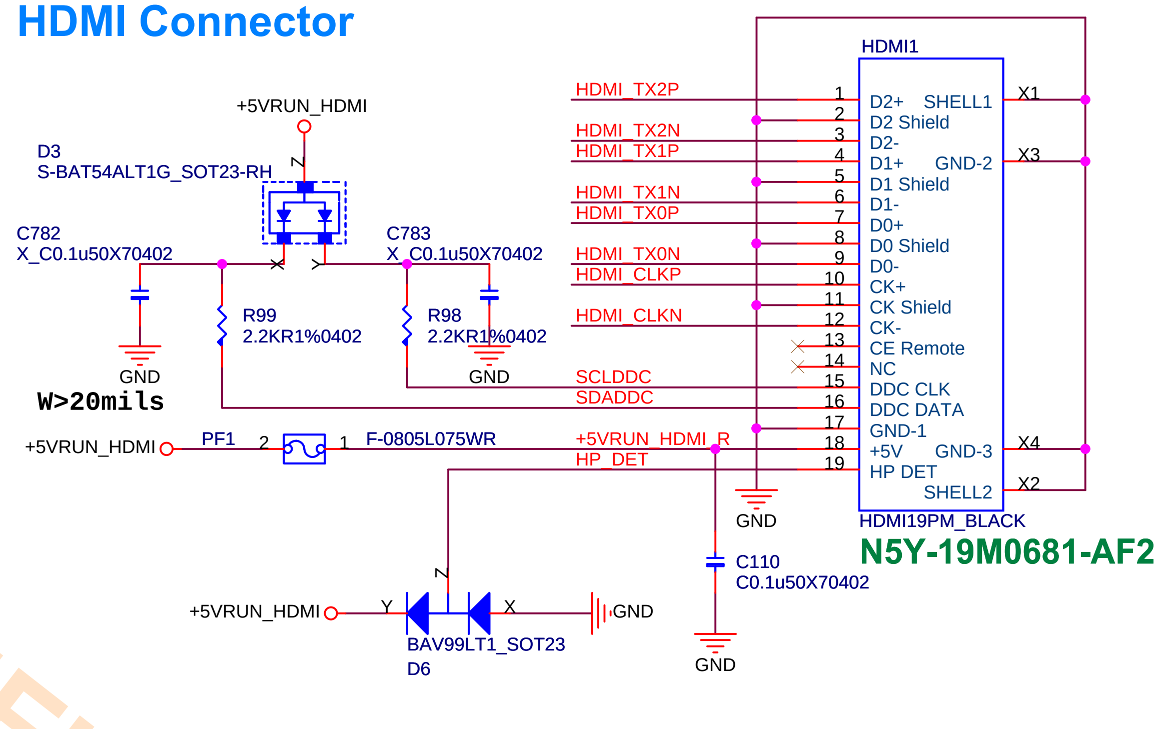
HDMI Repeater



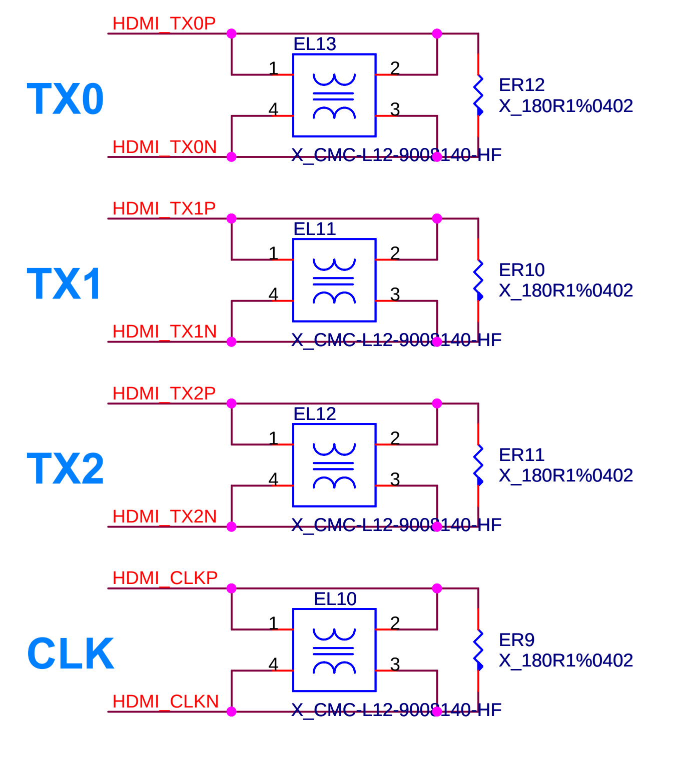
HDMI Connector

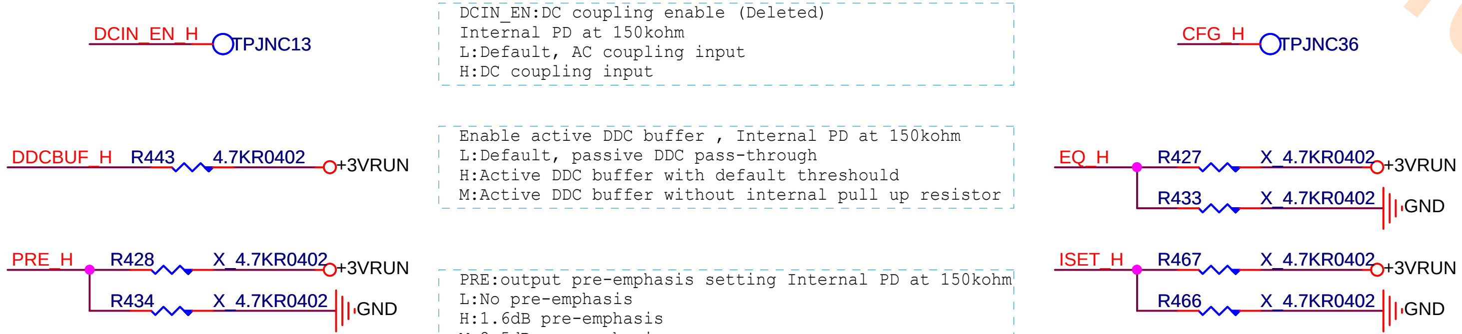


An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

HPD_SNK Internal PD 150kohm

EMI Close Connector





DCIN_EN:DC coupling enable (Deleted)
Internal PD at 150kohm
L:Default, AC coupling input
H:DC coupling input

Configuation pin (Deleted)
Internal PD at 150kohm
L:HDMI ID disable
H:HDMI ID enable

Enable active DDC buffer , Internal PD at 150kohm
L:Default, passive DDC pass-through
H:Active DDC buffer with default threshould
M:Active DDC buffer without internal pull up resistor

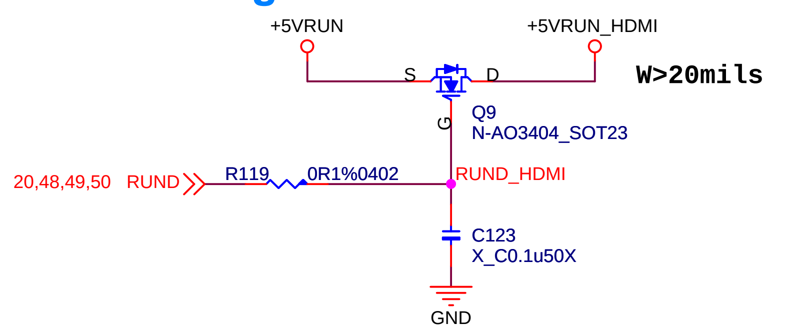
Receiver equalization setting
Internal PD at 150kohm
L:programmable EQ for channel loss up to 12.4dB
H:programmable EQ for channel loss up to 4.3dB
M:programmable EQ for channel loss up to 48.6dB

PRE:output pre-emphasis setting Internal PD at 150kohm
L:No pre-emphasis
H:1.6dB pre-emphasis
M:2.5dB pre-emphasis

TMDS output swing adjustment
Internal PD at 150kohm
L:Default
H:Increase +13%
M:reduce -13%

ADDR1 (CFG)	ADDR0 (EQ)	I2C control bus address (Internal pull down at ~150kΩ, 3.3V I/O)
0	0	0x4C / 4D (default)
0	1	0x5C / 5D
1	0	0xCC / CD
1	1	0xEC / ED

Avoid HDMI Leakage



MICRO-STAR INT'L CO.,LTD.

Title	HDMI Repeater	
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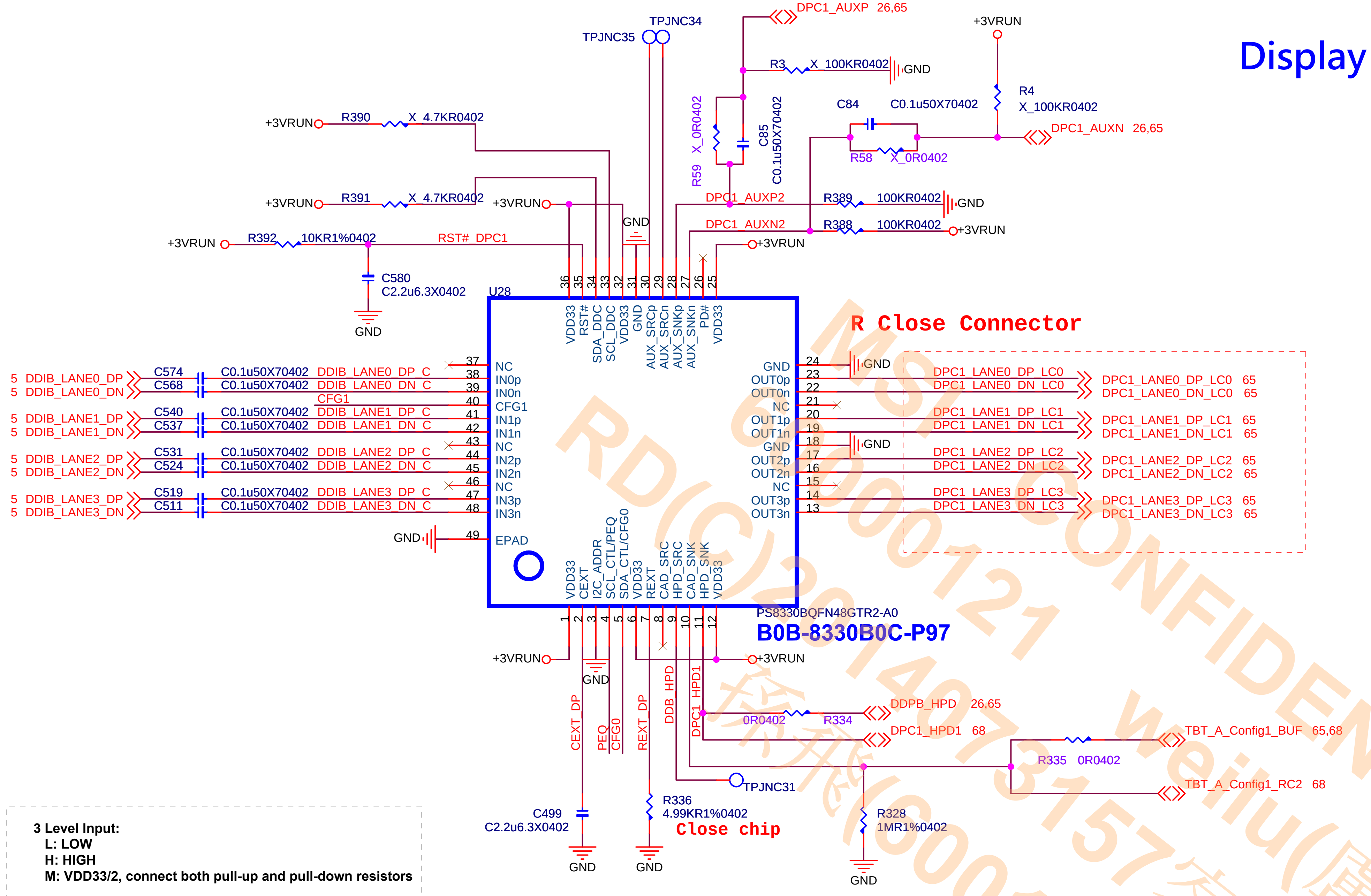
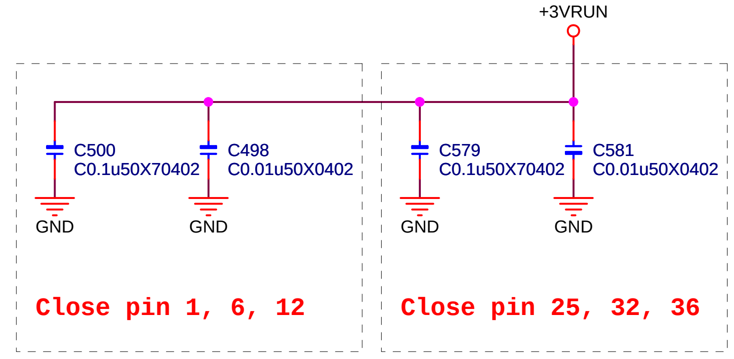
Display Port

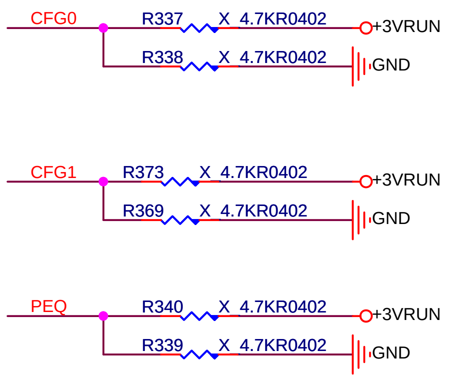




CAD_SNK Have internal Pull down 1Mohm.

HPD_SNK Have internal Pull down 150kohm.
No problem with Leakage from DP device
The DP_PWR and RETURN pins of the
box-to-box connectors must support the
maximum current rating of 500mA.

3 Level Input:
- L: LOW
- H: HIGH
- M: VDD33/2, connect both pull-up and pull-down resistors

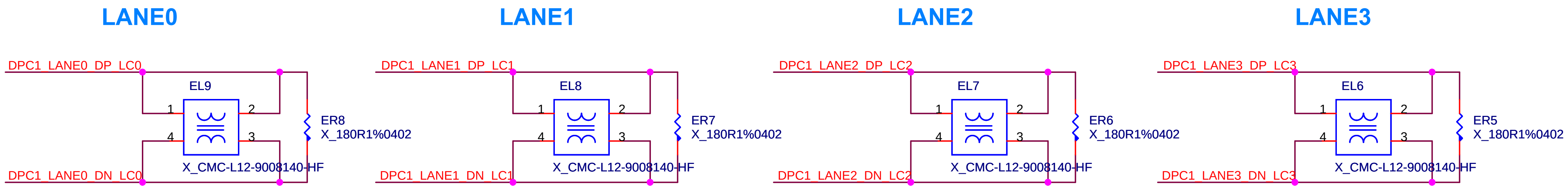


Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
- L: default, automatic EQ enable & AUX interception enable
- H: automatic EQ disable & AUX interception enable
- M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
- H: default, auto test disable & input offset cancellation enable
- L: auto test enable & input offset cancellation enable
- M: auto test disable & input offset cancellation disable

Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.
- L: default, LEQ, compensate channel loss up to 12dB @ HBR2
- H: HEQ, compensate channel loss up to 15dB @ HBR2
- M: LLEQ, compensate channel loss up to 5dB @ HBR2

EMI Close Connector



Audio CODEC/Audio AMP

L11 X_0R
JNC4 X_93519
C689 C0.1u50X70402
C139 C0.1u50X70402
C661 C0.1u50X70402
C660 C0.1u50X70402
EC20 X_C0.1u50X70402
EC21 X_C0.1u50X70402
GND AGND

CODEC_HDA_SDIN0
EC59 C10p50N0402
GND
EMI(RADIATION SOLUTION)

DVDD
Close Codec
+3VSUS
C650 C10u6.3X5-HF
C675 C0.1u50X70402
GND GND

Close Pin25
Close Pin38
CODEC_LDOOUT
C685 C10u6.3X5-HF
C682 C0.1u50X70402
C641 C10u6.3X5-HF
C648 C0.1u50X70402
AGND

AVDD5V
1A
L10 180L1.5A-90
+5VSUS
C671 C0.1u50X70402
C669 C10u6.3X5-HF
AGND AGND
AVDD5V

U34
ALC892-CG
B05-LC89214-R09

GND C643 X_C10p50N0402
34 EAPD
40 SPDIFO R457 10R1%0402 SPDIFO_R
22 CODEC_HDA_SDOUT
22 CODEC_HDA_SDIN0
22 CODEC_HDA_SYNC
22 CODEC_HDA_RST#
R471 33R0402 HD_SDIN
22 CODEC_HDA_BIT_CLK
REGREF
GND C663 C10u6.3X5-HF
40 FRONT_JD R499 5.1KR1%0402
40 MIC_JD R498 20KR1%0402
VREF_ALC898
Close Codec
AGND C673 C10u6.3X5-HF
Close Codec
AGND R458 20KR1%0402 JDREF
AVDD5V
MIC-VREFO-R
MIC-VREFO-L
22 HDA_SPKR R489 47KR1%0402 PC_BEEP_A C681 C1u25X0402 PC_BEEP
R490 4.7KR0402
C680 C0.1u50X70402
GND GND
PDM_DATA
GND AGND

EAPD/SPDIFI
SPDIF-OUT
SDATA-OUT
SDATA-IN
SYNC
RESET#
BCLK
GPIO0/DMIC-CLK/SPDIF-OUT2
REGREF
SENSE A
SENSE B
MIC1-VREFO-R
MIC2-VREFO
MIC1-VREFO-L
PIN37-VREFO
LDO-IN
LINE2-VREFO
VREF
SENSE C
JDREF
BEEP
GPIO1/DMIC-DATA
DVSS
DVDD
DVDD-IO
LDO-OUT1
LDO-OUT2
AVSS
AVSS

FRONT-R 36 FRONT_OUT_R C657 C10u6.3X5-HF FRONT_OUTR 40
FRONT-L 35 FRONT_OUT_L C659 C10u6.3X5-HF FRONT_OUTL 40
SURR-R 41 BACK_SPK_R_F C646 C0.47u10X0402 BACK_SPK_R 40
SURR-L 39 BACK_SPK_L_F C649 C0.47u10X0402 BACK_SPK_L 40
CENTER 43
LFE 44
SIDE-R 46 HP_R_ADC_R C644 C1u25X0402 HP_R_ADC 33
SIDE-L 45 HP_L_ADC_R C645 C1u25X0402 HP_L_ADC 33
LINE1-R 24
LINE1-L 23
LINE2-R 15 FRONT_SPK_R_F C695 C0.47u10X0402 FRONT_SPK_R
LINE2-L 14 FRONT_SPK_L_F C694 C0.47u10X0402 FRONT_SPK_L
MIC1-R 22 MIC_R C700 C4.7u10X0603 MIC_R_C R502 75R1%0402
MIC1-L 21 MIC_L C699 C4.7u10X0603 MIC_L_C R507 75R1%0402
MIC2-R 17
MIC2-L 16
CD-R 20
CD-GND 19
CD-L 18

R497 2.2KR1%0402 MIC-VREFO-R
MIC_IN_R 40
MIC_IN_L 40
R508 2.2KR1%0402 MIC-VREFO-L

APA2051 Pin23: Gain Setting
Speaker Spec: 2.0W(Normal), 2.5W (Max)
Vo=(2*4)^0.5=2.828
dB-20LOG(Vo/Vi)
Gain: 2.828Vrms/1.2Vrms=2.36
7dB =~ 20LOG 2.36
7dB : Setting Pin23 on 3.1V
(R103:13Kohm, R106:22Kohm)

For 6dB When Using 1.5W (Normal)
(R103:10Kohm, R106:15Kohm)

AMP

+5VSUS
R109 100KR0402
+5VSUS
R103 10KR1%0402
6DB/1.5W
AGND C122 C1u25X0402 BIAS_AMP
SET_AMP
Q8 NN-2N7002DW-7-F_SOT363-6-RH
R114 15KR1%0402
34,40 EC_MUTE#
AGND
FRONT_SPK_R
FRONT_SPK_L
AGND R122 0R1%0402 HP_EN
CP+_AMP
C138 C2.2u6.3X0402
CP-_AMP

U14
INR_A
INL_A
BIAS
/AMP_EN
SET
HP EN
NC
CP+
CP-
INR_H
INL_H
GND-PAD
ROUT+
ROUT-
LOUT+
LOUT-
HVDD
VDD
GND
PVDD
PVDD
CVDD
PGND
PGND
CGND
VSS
NC
HP_R
HP_L

OUT_R+
OUT_R#
OUT_L+
OUT_L#
R135 0R1%0402 +3VSUS
HVDD_AMP
C135 C0.1u50X70402
C636 C10u6.3X5-HF
C142 C1u25X0402
C137 C0.1u50X70402
C121 C0.1u50X70402
+5V_AMP
L9 180L1.5A-90
50mil
VSS_AMP
C140 C1u25X0402
APA2051QBI-TRG_TQFN28
I71-020510C-A30

EMI Close Codec

Internal Mic

R464 33R0402 PDM_CLK_CONN PDM_CLK_CONN 44
R468 0R1%0402 PDM_DATA_CONN PDM_DATA_CONN 44
PDM_CLK
PDM_DATA
EC58 X_C22p50N0402
C670 X_C22p50N0402
GND GND

Internal Speaker Conn

OUT_L# ER13 0R1%0402 OUT_L#_R
OUT_L+ ER14 0R1%0402 OUT_L+_R
OUT_R+ ER15 0R1%0402 OUT_R+_R
OUT_R# ER16 0R1%0402 OUT_R#_R
CON7
C711 X_C680p50X70402
C714 X_C680p50X70402
C727 X_C680p50X70402
C730 X_C680p50X70402
GND
BH1X4#S-1.25PITCH_WHITE
N32-1040AV0-H06

msi	MICRO-STAR INT'L CO.,LTD.
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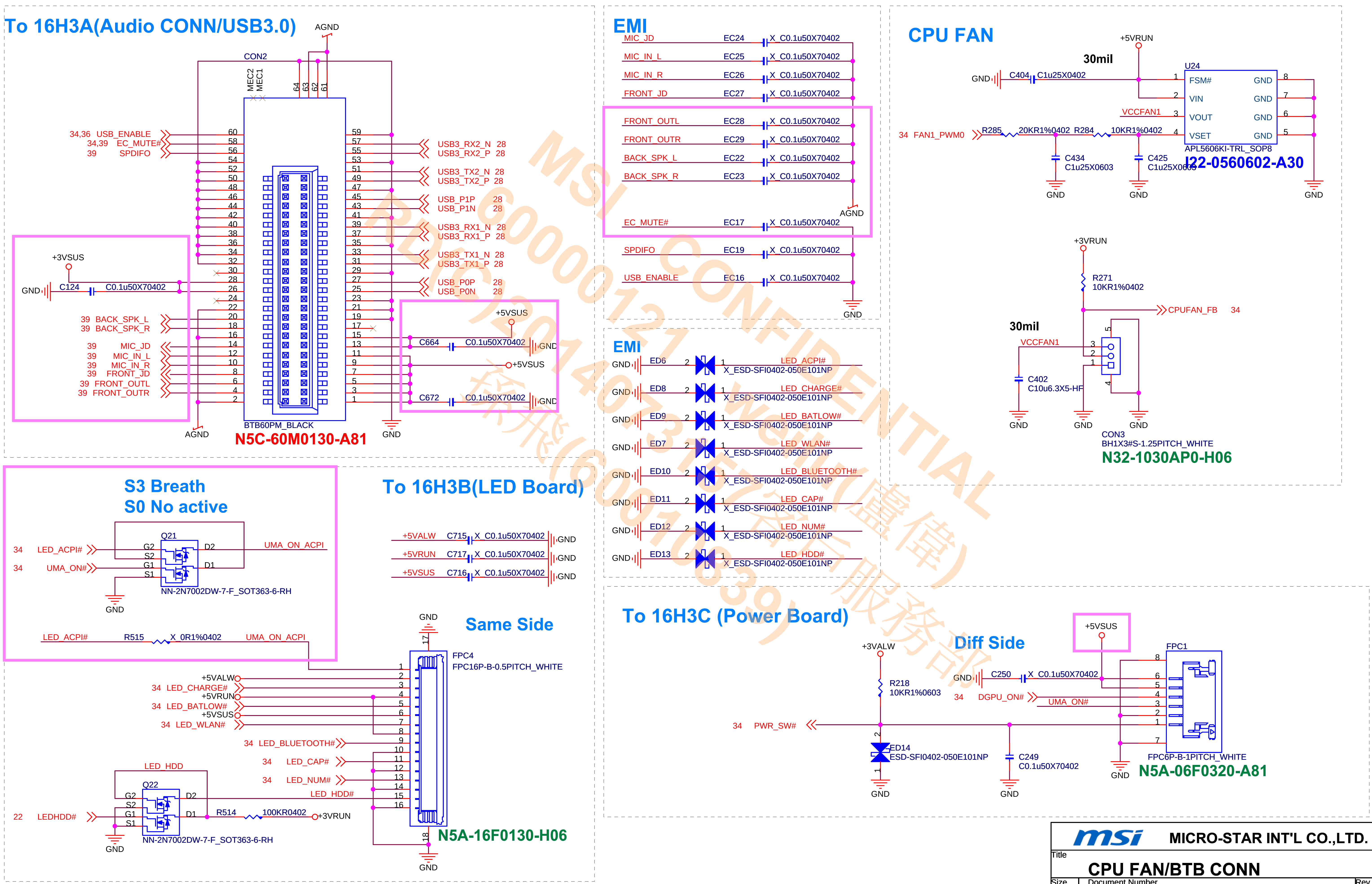
CPU FAN/BTB CONN



MSI MICRO-STAR INT'L CO.,LTD.

Title	CPU FAN/BTB CONN	
Size	Document Number: MS-16H3	Rev 1.0
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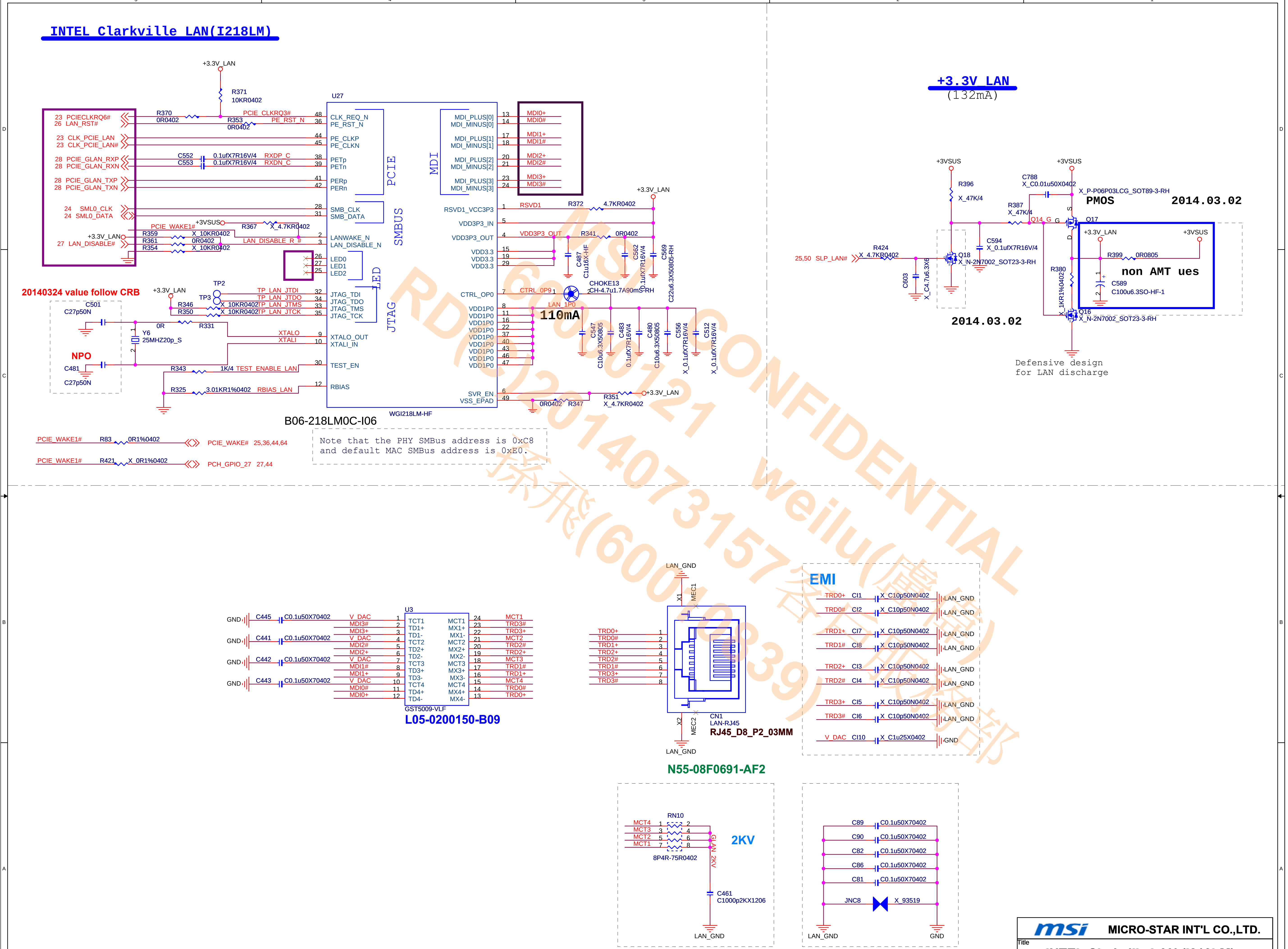

msi MICRO-STAR INT'L CO.,LTD.

Title	INTEL Clarkville LAN (I218LM)	
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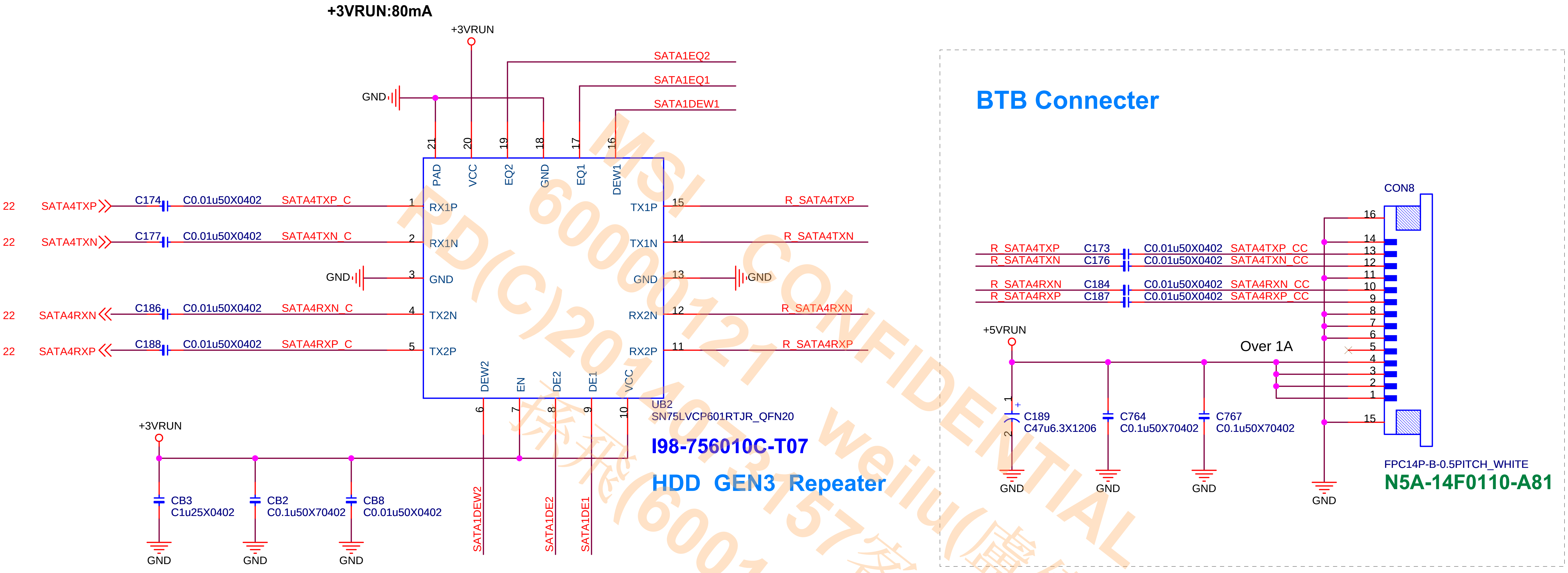
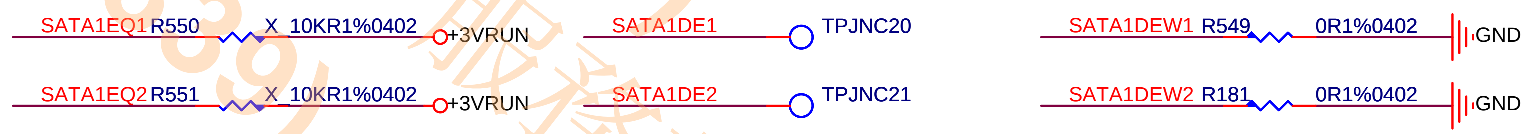
HDD (With Repeater)





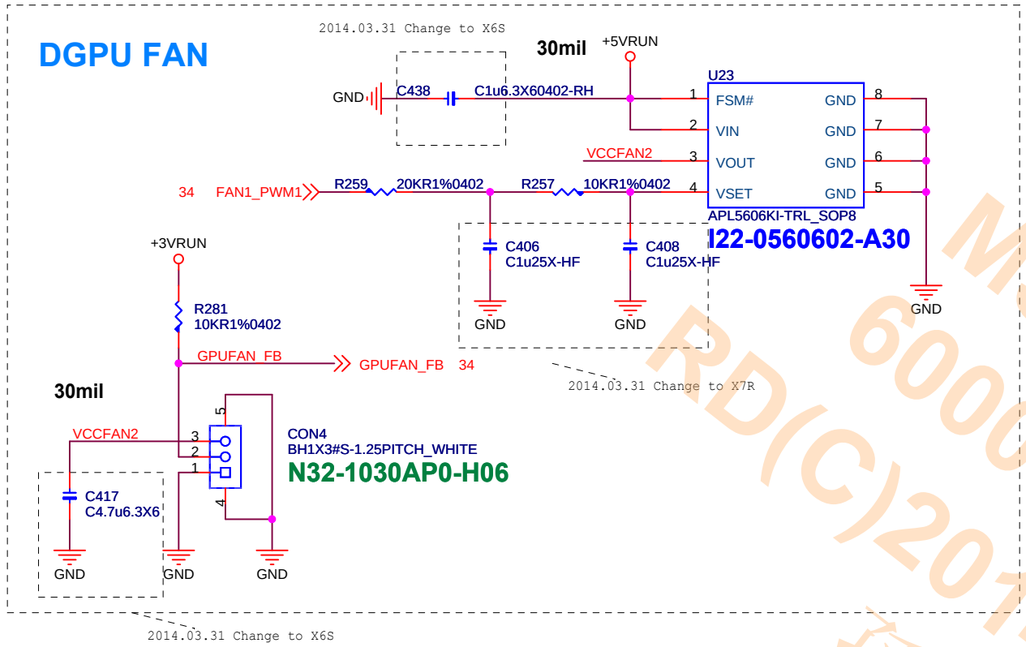
TI SN75LVCP601RTJR HW Setting

DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	EQ1/EQ2	CH1/CH2Equalization dB (at 6Gbps)
NC (***default***)	–4	NC (***default***)	0
0	0	0	7
1	–2	1	14

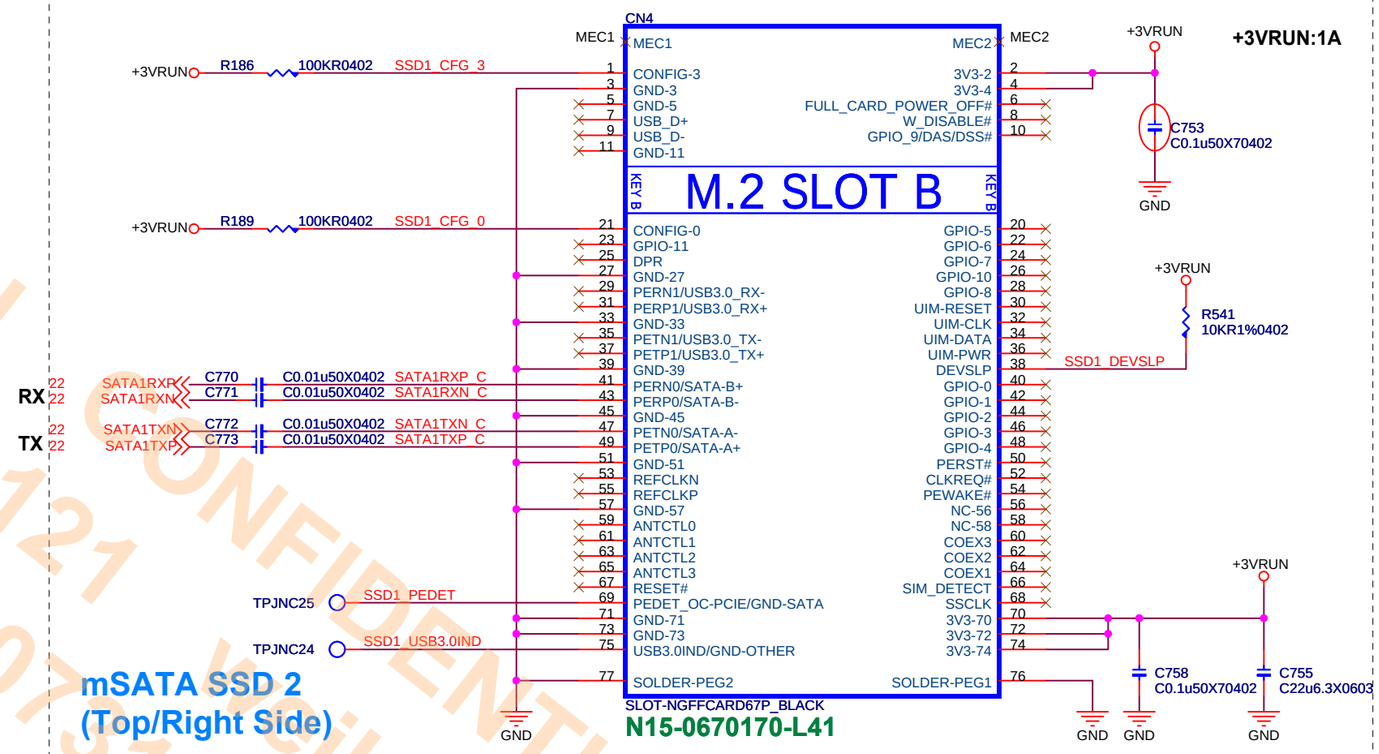
DEW1/DEW2	Device Function → DE Width for CH1/CH2
0	De-emphasis pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps)
1 (***default***)	De-emphasis pulse duration, long (recommended setting when link operates at SATA 1.5/3 Gbps speed only)

SSD/ DGPU FAN

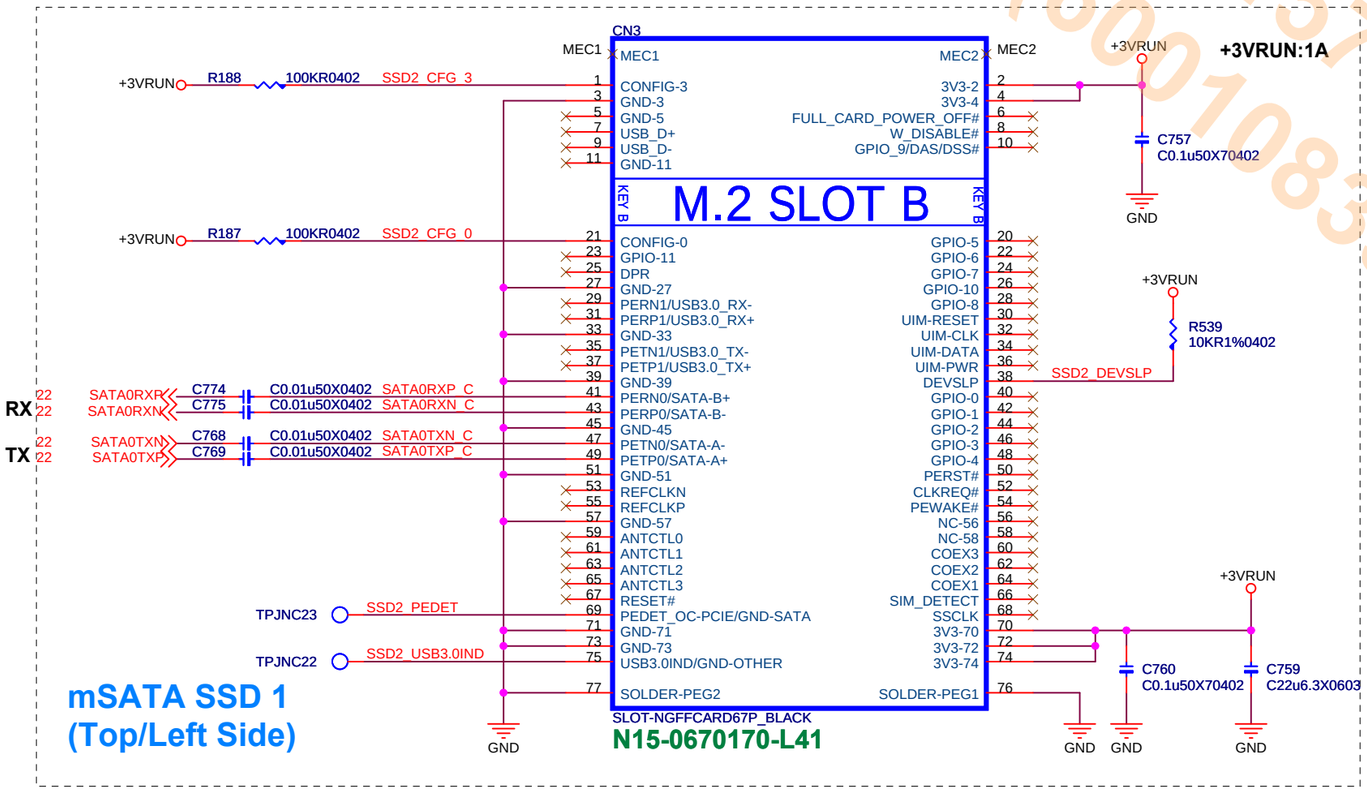
DGPU FAN



mSATA SSD 2 (Top/Right Side)



mSATA SSD 1 (Top/Left Side)



40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host transmitter differential signal pair

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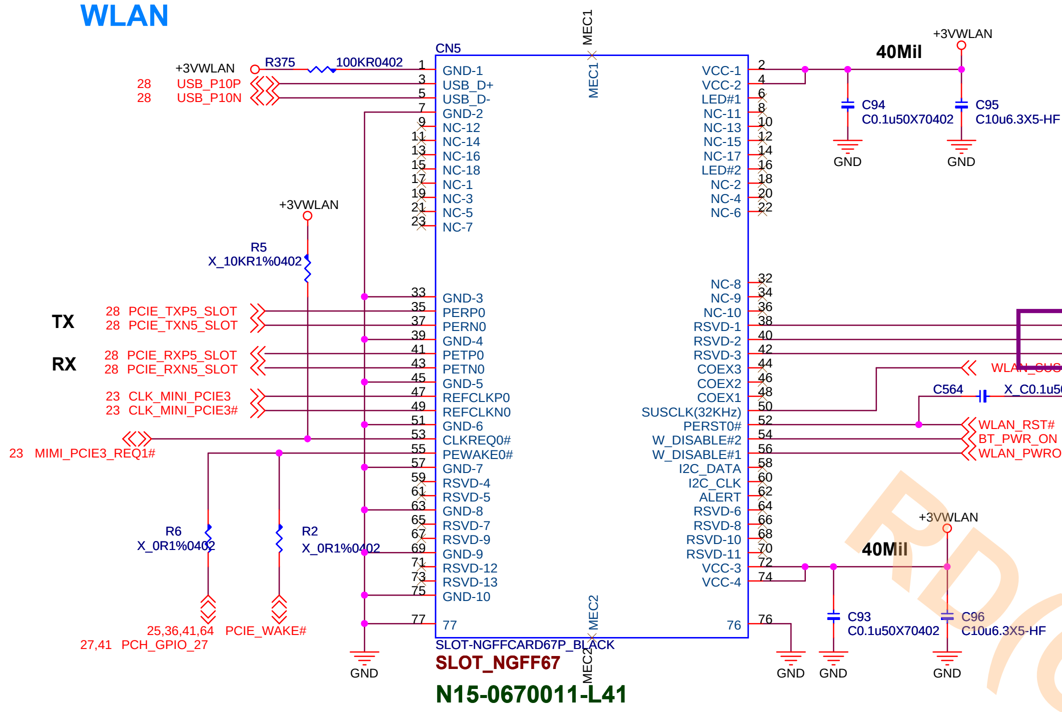
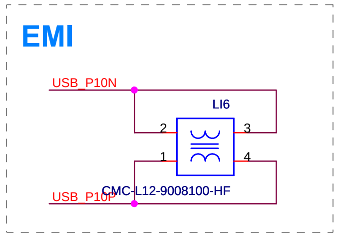
WLAN /Camera/ClickPad/FP

WLAN

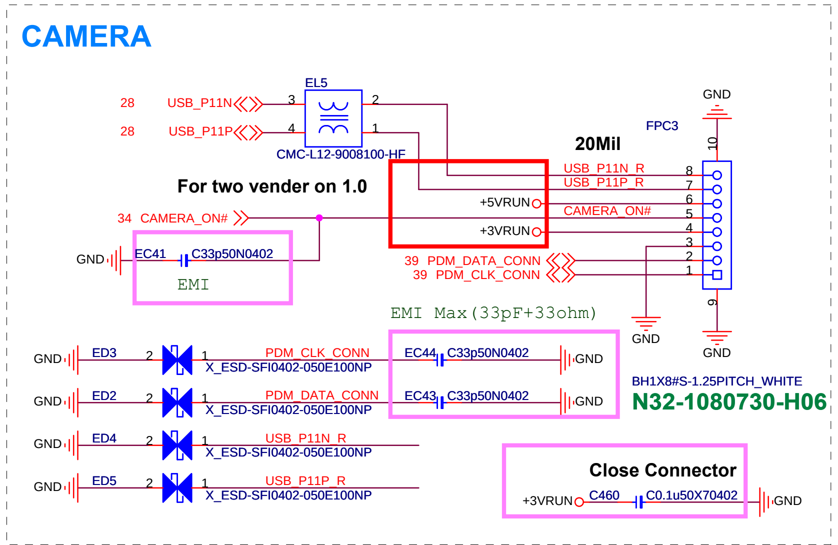


EMI

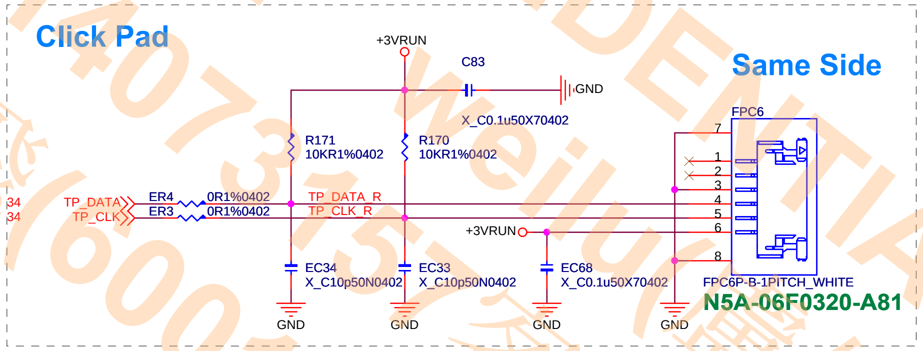


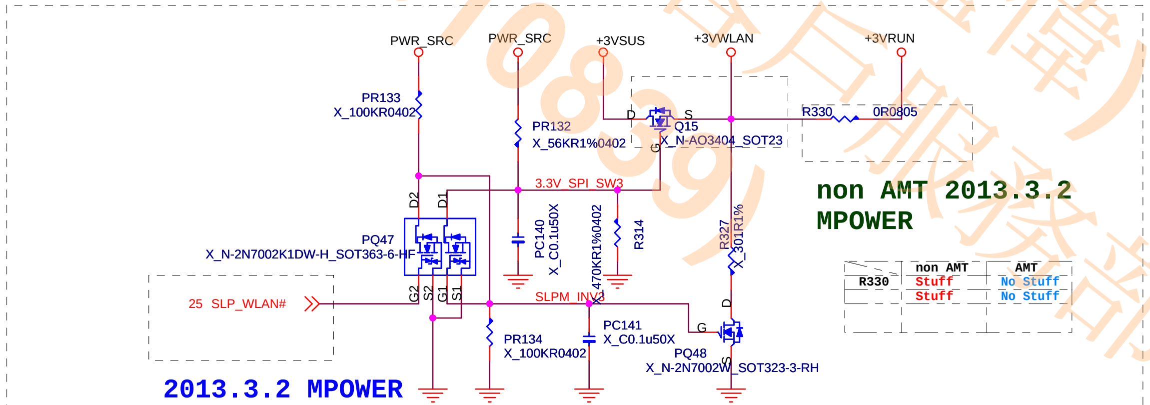
Pin	Signal	Pin	Signal
Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

CAMERA



Click Pad





2014.2.11 for EC ON/OFF,
from EC OD control.

If Non-AMT, R267 stuff.This block no-stuff
If AMT, This block stuff, R267 no-stuff

msi	MICRO-STAR INT'L CO.,LTD.
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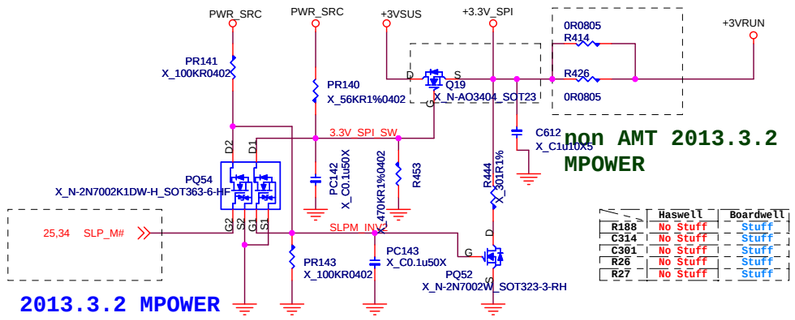
+3.3V_SPI

2A in 2013.3.2 MPOWER

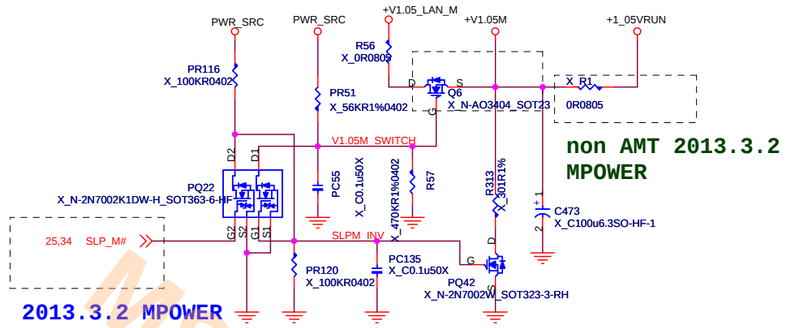


	Haswell	Boardwell
R188	No Stuff	Stuff
C314	No Stuff	Stuff
C301	No Stuff	Stuff
R26	No Stuff	Stuff
R27	No Stuff	Stuff

2013.3.2 MPOWER

+V1.05M

+V1.05M 2A in 2013.3.2 MPOWER

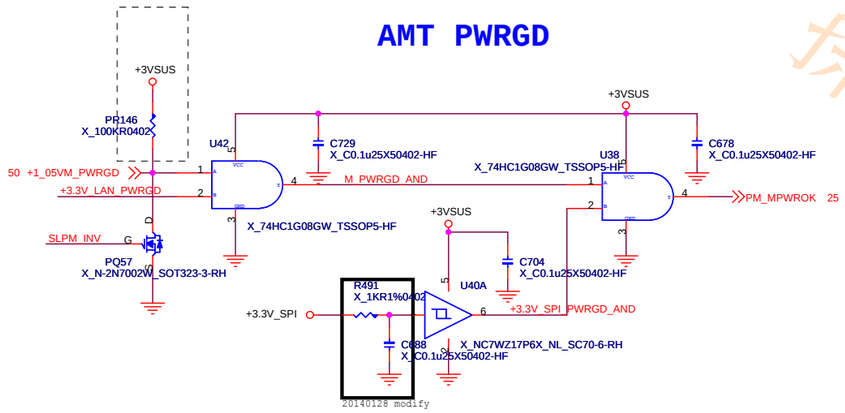


2013.3.2 MPOWER

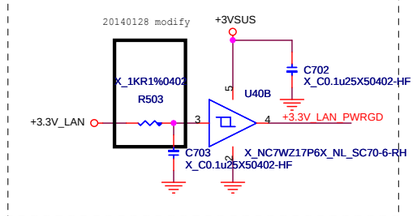
請靠近 PCH

2013.3.2 for AMT

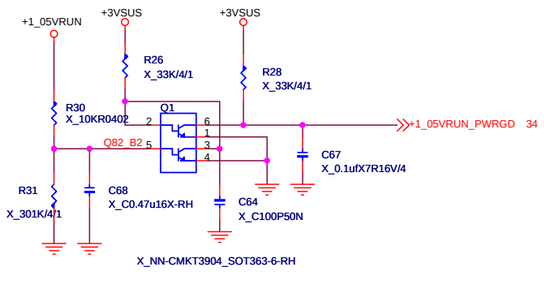
AMT PWRGD



+3.3V_LAN_PWRGD



+1_05VRUN_PWRGD, AMT used



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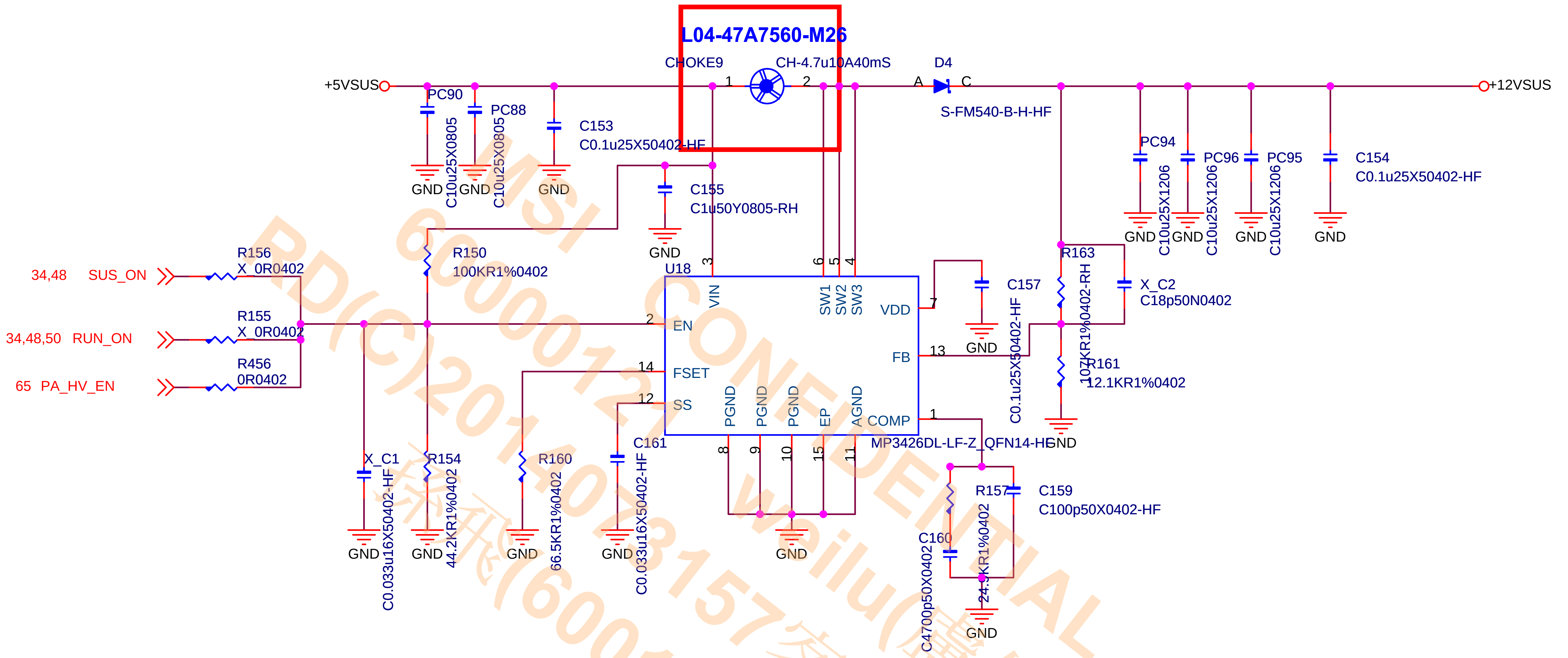
TBT Power 5V Boost 12V 1A



MICRO-STAR INT'L CO.,LTD.

Title	Thunderbolt Power	
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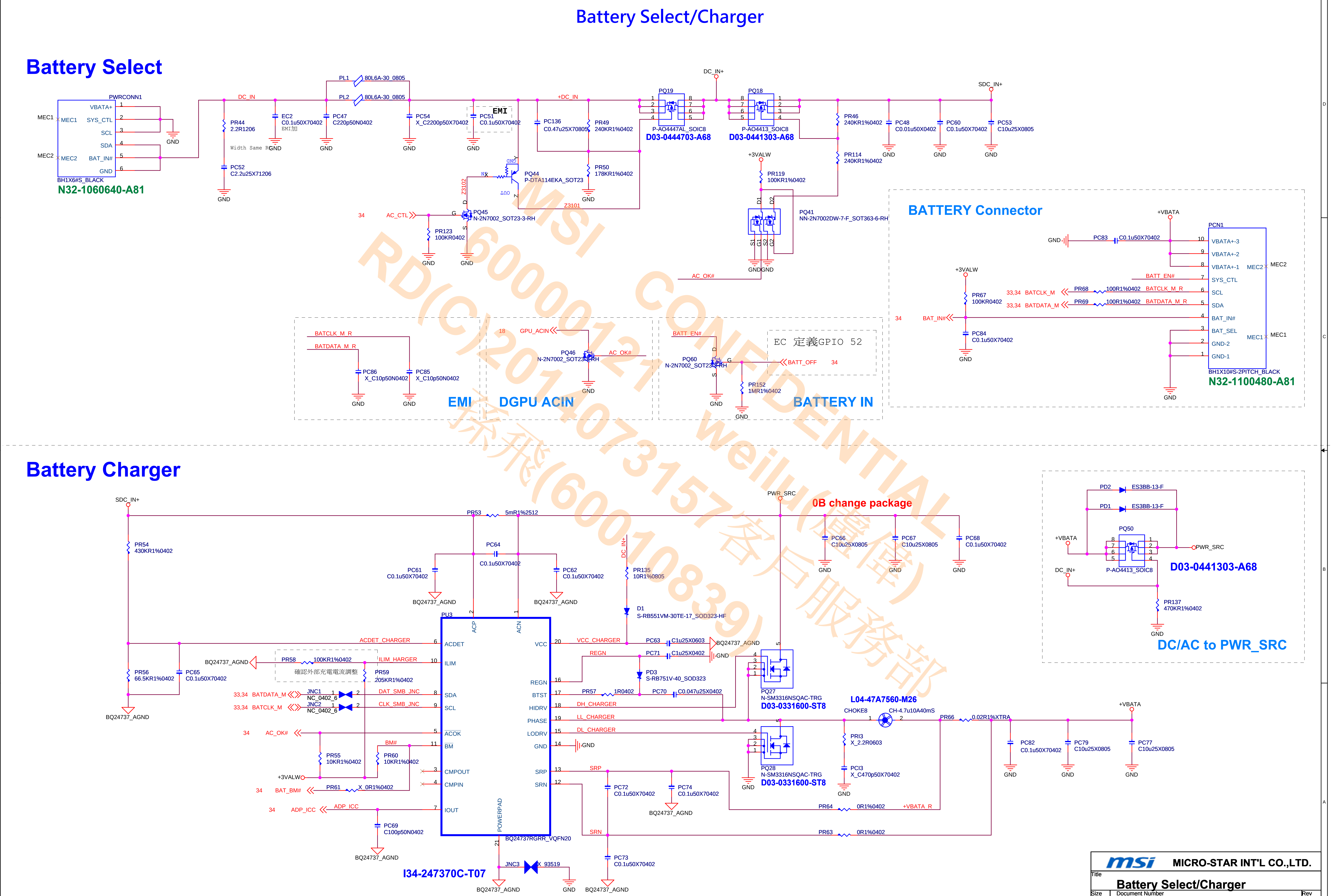
Battery Select/Charger



MICRO-STAR INT'L CO.,LTD.

Title	Battery Select/Charger
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System Power

OCP 13A
MAX 10A
+3VSUS

PWR_SRC
Close to high side Mosfet
PC110 C10u25X0805
PC102 C0.1u50X70402
PC108 C2200p50X70402
GND

PO31 D03-0331600-ST8
N-SM3316NSQAC-TRG
PR163 2.2R0603
PC149 C0.1u50X
L04-47A7620-M26
CHOKE12
CH-4.7u13A15.0mS
+3VSUS
PEC12 C220u6.3SO
PC100 C10u25X0805
PO32 N-SM3317NSQAC-TRG GND
D03-0331700-ST8
PRI5 X_2.2R0603
PCI5 X_C2200p50X70402
PR155 6.8KR1%0402
3.35V
PR157 10KR1%0402

PQ29 JNC5 X_0402 RUND +3VRUN
N-SM3316NSQAC-TRG
D03-0331600-ST8
+3VRUN

PWR_SRC
0B change PN
PC97 C1u25X70805
34,46 SUS_ON
PR162 100KR0402
SUSPWROK
SUSPWROK 34
PR160 10KR1%0402 +3VALW

PU9 TPS51225CRUKR_QFN20
VBST2 DH2 DRVH2 LL2 SW2 DL2 DRVL2 3V_FB VFB2 GPAD
VBST1 DH1 DRVH1 LL1 SW1 DL1 DRVL1 VO1 5V_FB VFB1
EN2 EN1 VIN PGOOD CS2 CS1 VERG3 VREG5 VCLK
GND
I32-512250C-T07

PR156 115KR1%0402-RH
PR161 100KR1%0402
+3VALW PC147 C1u25X0603 GND
+5VALW PC151 C1u25X0603 GND
+3VALW
+5VALW

PWR_SRC
Close to high side Mosfet
PC109 C2200p50X70402
PC112 C10u25X0805
PC111 C10u25X0805
GND

PO30 D03-0331600-ST8
N-SM3316NSQAC-TRG
PC150 C0.1u50X
PR165 2.2R0603
L04-47A7620-M26
CHOKE11
CH-4.7u13A15.0mS
+5VSUS
PCI6 X_C2200p50X70402
PR164 X_2.2R0603
PO33 N-SM3317NSQAC-TRG GND
D03-0331700-ST8
PR159 15KR1%0402
PR158 10KR1%0402
PC152 C10u25X0805
PEC13 C220u6.3SO

OCP 13A
MAX 10A
+5VSUS

RUND PQ61 N-SM3316NSQAC-TRG
+5VRUN
D03-0331600-ST8
+5VRUN

PWR_SRC
PR147 100KR0402
RUN_ON_R
PWR_SRC
PR154 47KR1%0402
RUND 20,37,49,50
PQ59 NN-2N7002DW-7-F_SOT363-6-RH
PR153 470KR1%0402
PC146 C0.1u50X70402
34,46,50 RUN_ON
PR151 100KR0402
PC144 C0.1u50X70402
GND

MICRO-STAR INT'L CO.,LTD.

Title	System Power	
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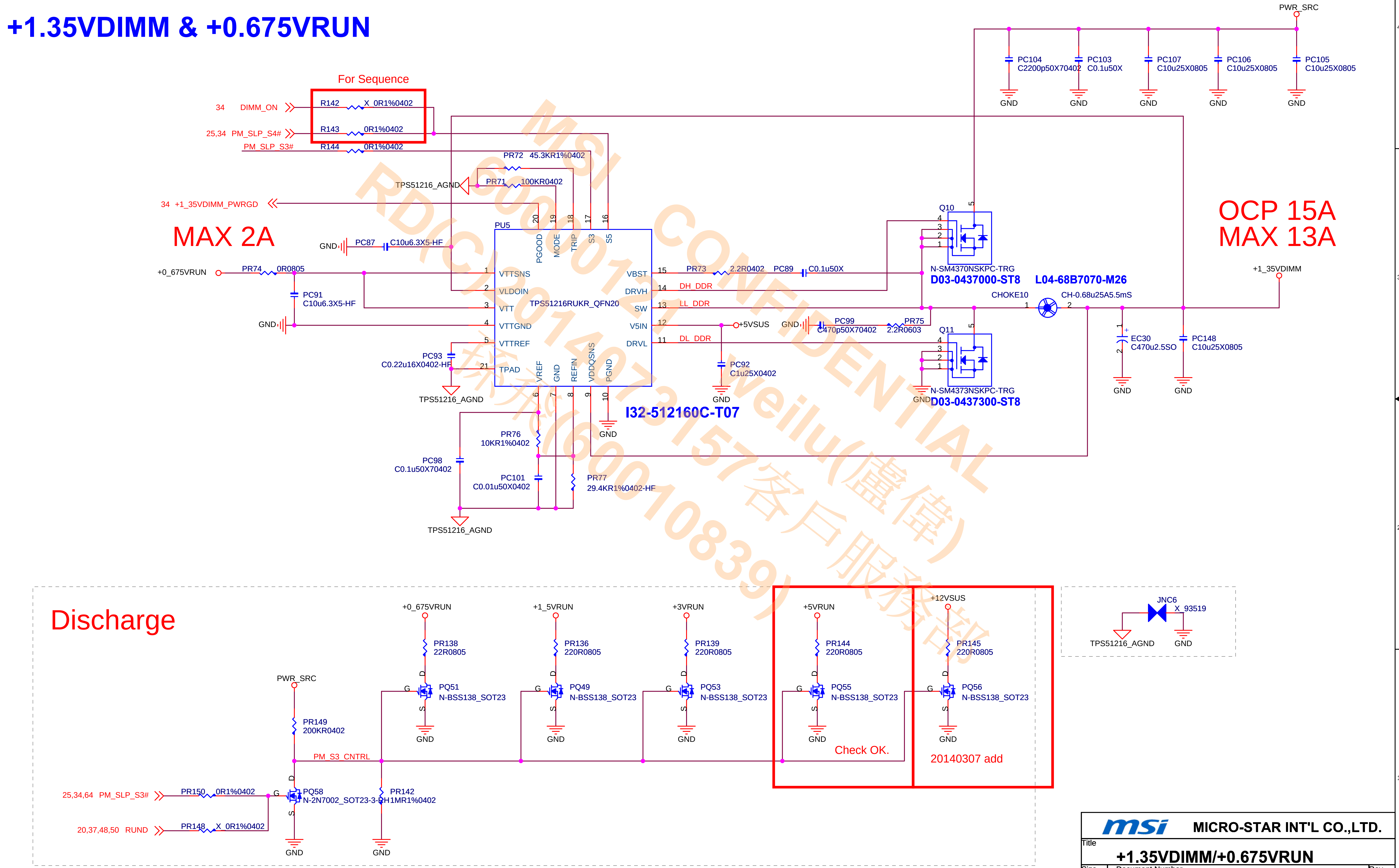
+1.35VDIMM/+0.675VRUN



MICRO-STAR INT'L CO.,LTD.

Title: +1.35VDIMM/+0.675VRUN

Size | Document Number: MS-16H3 | Rev: 1.0

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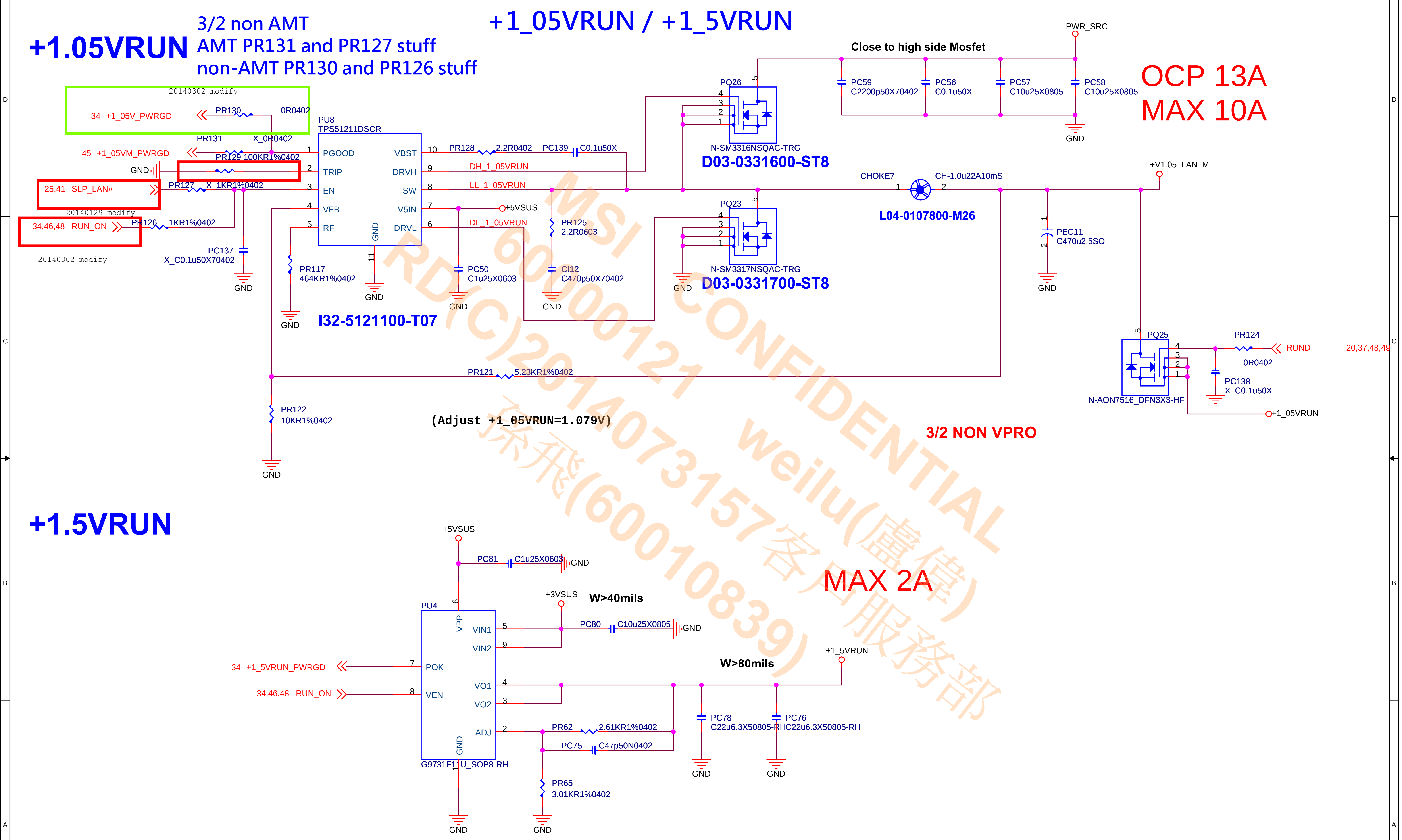
+1_05VRUN / +1_5VRUN



msi	MICRO-STAR INT'L CO.,LTD.
Title	+1_05VRUN / +1_5VRUN
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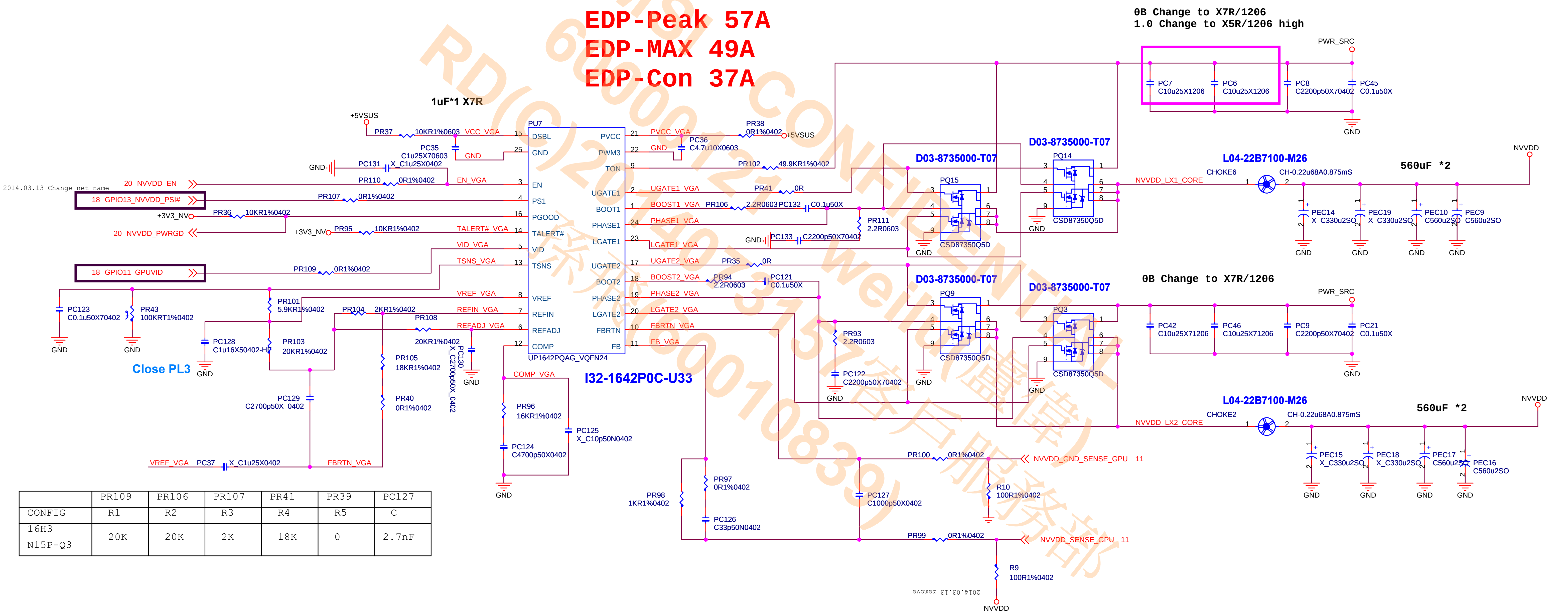
DGPU POWER NVVDD

DGPU POWER / UP1642PQAG

CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V



	PR109	PR106	PR107	PR41	PR39	PC127
CONFIG	R1	R2	R3	R4	R5	C
16H3 N15P-Q3	20K	20K	2K	18K	0	2.7nF

MICRO-STAR INT'L CO.,LTD.

Title: DGPU POWER NVVDD

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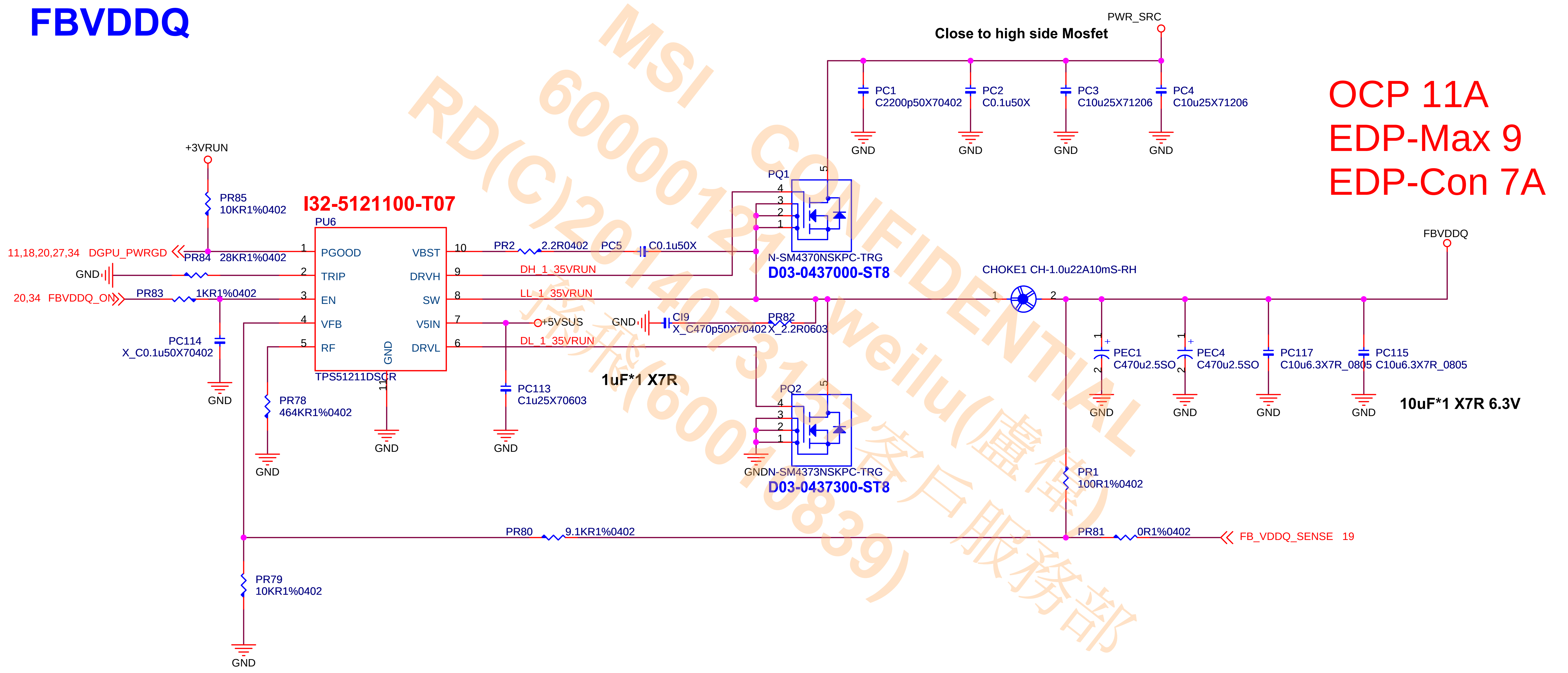
DGPU POWER FBVDDQ

FBVDDQ



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Title	DGPU POWER FBVDDQ	
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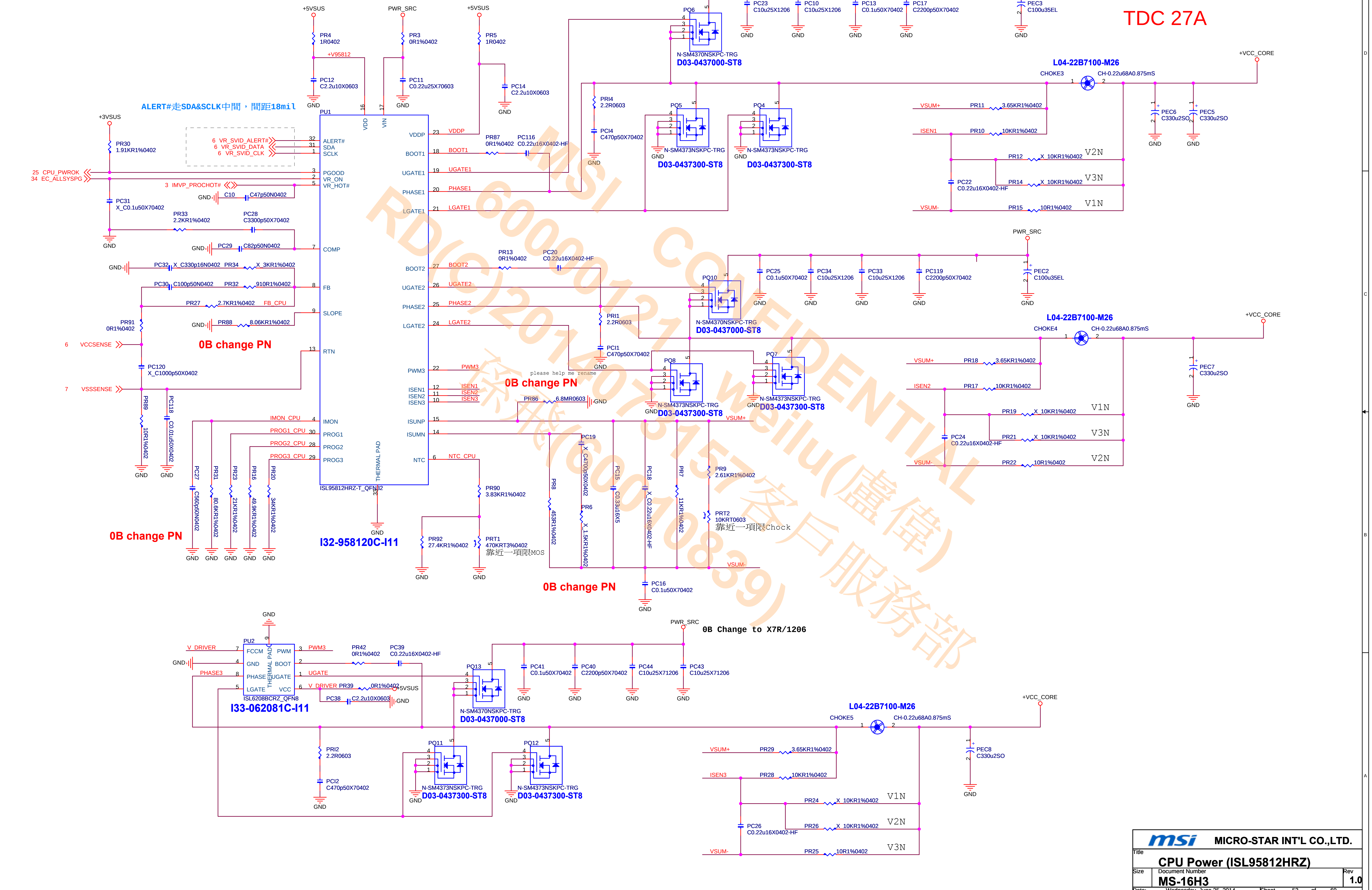
Date: Wednesday, June 25, 2014	Sheet 52 of 69	

CPU Core Power(ISL95812HRZ)

CPU Power (+VCC_CORE)

MAX 95A
TDC 27A



MICRO-STAR INT'L CO.,LTD.

Title: CPU Power (ISL95812HRZ)

Size | Document Number: MS-16H3 | Rev 1.0

Date: Wednesday, June 25, 2014

EMI/ Impedence

Impedence Connector No PN

40 ohm

J29 — L1_6.5mil_40_Ohm — GND2 — X_H1X2M_BLACK	J21 — L3_5mil_40_Ohm — GND2_GND4 — X_H1X2M_BLACK	J14 — L10_5mil_40_Ohm — GND9_GND11 — X_H1X2M_BLACK

45 ohm

J31 — L1_5.5mil_45_Ohm — GND2 — X_H1X2M_BLACK	J28 — L3_4mil_45_Ohm — GND2_GND4 — X_H1X2M_BLACK	J4 — L5_4mil_45_Ohm — GND4_GND6 — X_H1X2M_BLACK	J20 — L10_4mil_45_Ohm — GND9_GND11 — X_H1X2M_BLACK
J9 — L12_5.5mil_45_Ohm — GND11 — X_H1X2M_BLACK			

50 ohm

J30 — L1_4mil_50_Ohm — GND2 — X_H1X2M_BLACK	J27 — L3_3mil_50_Ohm — GND2_GND4 — X_H1X2M_BLACK	J12 — L5_3mil_50_Ohm — GND4_GND6 — X_H1X2M_BLACK	J13 — L10_3mil_50_Ohm — GND9_GND11 — X_H1X2M_BLACK
J1 — L12_4mil_50_Ohm — GND11 — X_H1X2M_BLACK			

80 ohm

J35 — L1_DIFF_4.5/4/4.5_80ohm+ / L1_DIFF_4.5/4/4.5_80ohm- — X_H1X4_BLACK — GND2	J25 — L3_DIFF_4.5/7/4.5_80ohm+ / L3_DIFF_4.5/7/4.5_80ohm- — X_H1X4_BLACK — GND2_GND4	J10 — L5_DIFF_4.5/7/4.5_80ohm+ / L5_DIFF_4.5/7/4.5_80ohm- — X_H1X4_BLACK — GND4_GND6	J16 — L10_DIFF_4.5/7/4.5_80ohm+ / L10_DIFF_4.5/7/4.5_80ohm- — X_H1X4_BLACK — GND9_GND11	J2 — L12_DIFF_4.5/4/4.5_80ohm+ / L12_DIFF_4.5/4/4.5_80ohm- — X_H1X4_BLACK — GND11

85 ohm

J36 — L1_DIFF_4.5/4.5/4.5_85ohm+ / L1_DIFF_4.5/4.5/4.5_85ohm- — X_H1X4_BLACK — GND2	J26 — L3_DIFF_4/6.5/4_85ohm+ / L3_DIFF_4/6.5/4_85ohm- — X_H1X4_BLACK — GND2_GND4	J11 — L5_DIFF_4/6.5/4_85ohm+ / L5_DIFF_4/6.5/4_85ohm- — X_H1X4_BLACK — GND4_GND6	J18 — L10_DIFF_4/6.5/4_85ohm+ / L10_DIFF_4/6.5/4_85ohm- — X_H1X4_BLACK — GND9_GND11	J7 — L12_DIFF_4.5/4.5/4.5_85ohm+ / L12_DIFF_4.5/4.5/4.5_85ohm- — X_H1X4_BLACK — GND11

88 ohm

J34 — L1_DIFF_4.5/6/4.5_88ohm+ / L1_DIFF_4.5/6/4.5_88ohm- — X_H1X4_BLACK — GND2	J23 — L3_DIFF_3.5/4.5/3.5_88ohm+ / L3_DIFF_3.5/4.5/3.5_88ohm- — X_H1X4_BLACK — GND2_GND4	J17 — L10_DIFF_3.5/4.5/3.5_88ohm+ / L10_DIFF_3.5/4.5/3.5_88ohm- — X_H1X4_BLACK — GND9_GND11

90 ohm

J33 — L1_DIFF_4/6/4_90ohm+ / L1_DIFF_4/6/4_90ohm- — X_H1X4_BLACK — GND2	J24 — L3_DIFF_3.5/5.5/3.5_90ohm+ / L3_DIFF_3.5/5.5/3.5_90ohm- — X_H1X4_BLACK — GND2_GND4	J8 — L5_DIFF_3.5/5.5/3.5_90ohm+ / L5_DIFF_3.5/5.5/3.5_90ohm- — X_H1X4_BLACK — GND4_GND6	J15 — L10_DIFF_3.5/5.5/3.5_90ohm+ / L10_DIFF_3.5/5.5/3.5_90ohm- — X_H1X4_BLACK — GND9_GND11	J5 — L12_DIFF_4/6/4_90ohm+ / L12_DIFF_4/6/4_90ohm- — X_H1X4_BLACK — GND11

100 ohm

J32 — L1_DIFF_3.5/7.5/3.5_100ohm+ / L1_DIFF_3.5/7.5/3.5_100ohm- — X_H1X4_BLACK — GND2	J22 — L3_DIFF_3/10/3_100ohm+ / L3_DIFF_3/10/3_100ohm- — X_H1X4_BLACK — GND2_GND4	J6 — L5_DIFF_3/10/3_100ohm+ / L5_DIFF_3/10/3_100ohm- — X_H1X4_BLACK — GND4_GND6	J19 — L10_DIFF_3/10/3_100ohm+ / L10_DIFF_3/10/3_100ohm- — X_H1X4_BLACK — GND9_GND11	J3 — L12_DIFF_3.5/7.5/3.5_100ohm+ / L12_DIFF_3.5/7.5/3.5_100ohm- — X_H1X4_BLACK — GND11

EMI

+3VRUN: EC69 X_C0.1u50X70402 → GND

+1_35VDIMM: EC40 X_C0.1u50X70402, EC63 X_C0.1u50X70402, EC62 X_C0.1u50X70402 → GND

+3VSUS: EC66 C0.1u50X70402, EC54 X_C0.1u50X70402 → GND

+5VSUS: EC70 X_C0.1u50X70402, EC65 X_C0.1u50X70402, EC67 X_C0.1u50X70402, EC61 X_C0.1u50X70402, EC60 X_C0.1u50X70402 → GND

PWR_SRC — 0B stuff

RFI: EC35 C0.1u50X70402, EC38 C0.1u50X70402, EC51 C0.1u50X70402, EC42 C0.1u50X70402, EC50 C0.1u50X70402

RFI: EC7 X_C0.1u50X70402, EC12 X_C0.1u50X70402, EC6 C1000p50X0402, EC11 C0.1u50X70402, EC4 C0.1u50X70402, EC3 C0.1u50X70402 → GND

+VBATA: EC52 C0.1u50X70402, EC64 C0.1u50X70402 — RFI → GND

NVVDD: EC36 X_C0.1u50X70402, EC37 X_C0.1u50X70402, EC39 X_C0.1u50X70402 → GND

+1_05VRUN: EC49 X_C0.1u50X70402 → GND

+0_675VRUN: EC53 X_C0.1u50X70402 → GND

PWR_SRC: C784 C0.1u10X0402, C785 C0.1u10X0402 → GND

+VBATA: C787 C0.1u10X0402 → GND

+3VRUN: C786 C0.1u10X0402 → GND

0507 add for RF

J49, J48, J45: E21-5801010-RH → GND

J41, J43: E21-5801010-RH → GND

0507 add for RF clamp

J44, J42, J46: E21-5801010-RH → GND

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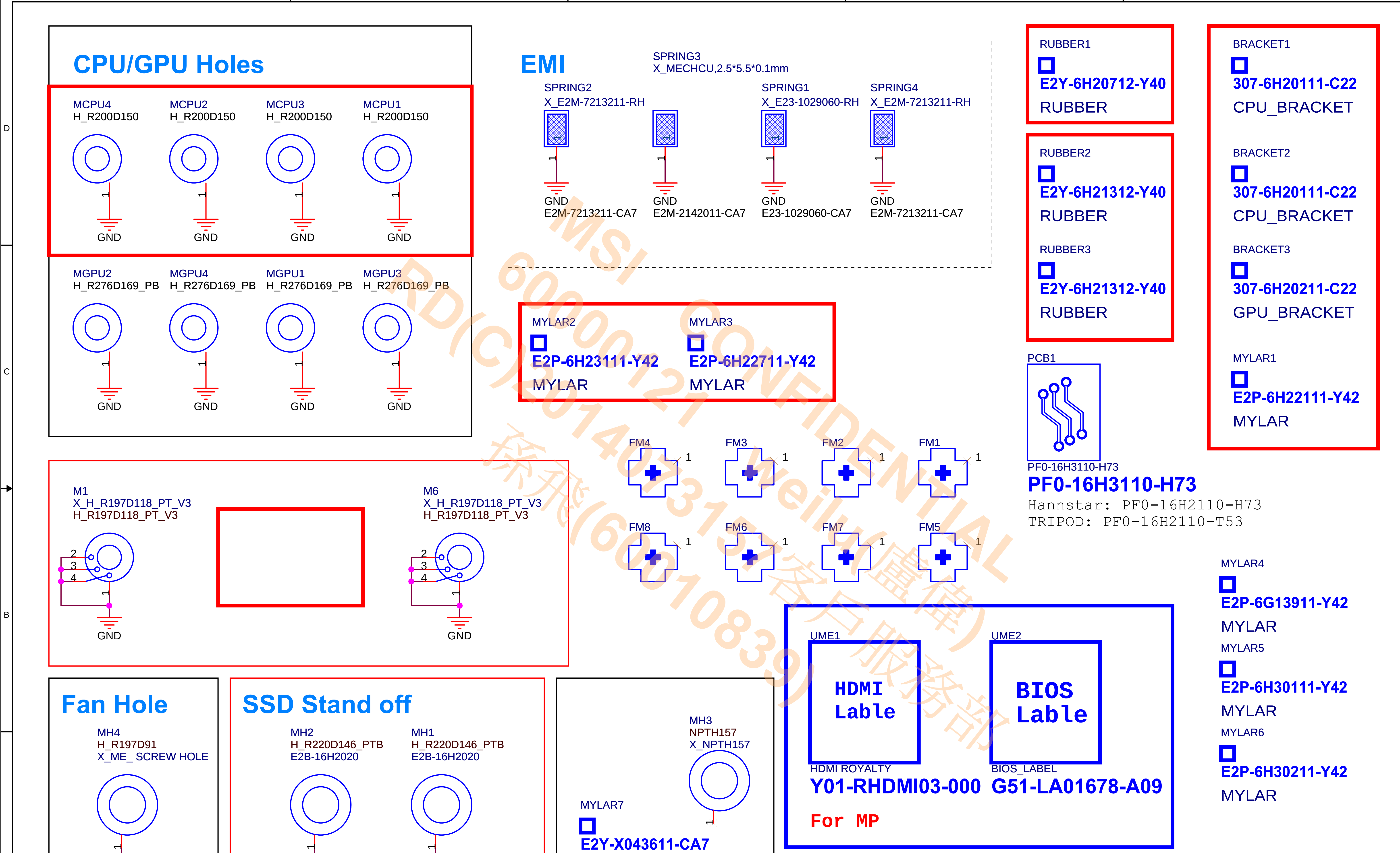
CPU/GPU Holes
MCPU4 H_R200D150
MCPU2 H_R200D150
MCPU3 H_R200D150
MCPU1 H_R200D150
GND
MGPU2 H_R276D169_PB
MGPU4 H_R276D169_PB
MGPU1 H_R276D169_PB
MGPU3 H_R276D169_PB
M1 X_H_R197D118_PT_V3 H_R197D118_PT_V3
M6 X_H_R197D118_PT_V3 H_R197D118_PT_V3
Fan Hole
MH4 H_R197D91 X_ME_ SCREW HOLE
SSD Stand off
MH2 H_R220D146_PTB E2B-16H2020
MH1 H_R220D146_PTB E2B-16H2020
MH3 NPTH157 X_NPTH157
MYLAR7 E2Y-X043611-CA7 Gaste
EMI
SPRING3 X_MECHCU,2.5*5.5*0.1mm
SPRING2 X_E2M-7213211-RH
SPRING1 X_E23-1029060-RH
SPRING4 X_E2M-7213211-RH
E2M-7213211-CA7
E2M-2142011-CA7
E23-1029060-CA7
E2M-7213211-CA7
MYLAR2 E2P-6H23111-Y42 MYLAR
MYLAR3 E2P-6H22711-Y42 MYLAR
FM4 FM3 FM2 FM1
FM8 FM6 FM7 FM5
RUBBER1 E2Y-6H20712-Y40 RUBBER
RUBBER2 E2Y-6H21312-Y40 RUBBER
RUBBER3 E2Y-6H21312-Y40 RUBBER
BRACKET1 307-6H20111-C22 CPU_BRACKET
BRACKET2 307-6H20111-C22 CPU_BRACKET
BRACKET3 307-6H20211-C22 GPU_BRACKET
MYLAR1 E2P-6H22111-Y42 MYLAR
PCB1 PF0-16H3110-H73
PF0-16H3110-H73
Hannstar: PF0-16H2110-H73
TRIPOD: PF0-16H2110-T53
MYLAR4 E2P-6G13911-Y42 MYLAR
MYLAR5 E2P-6H30111-Y42 MYLAR
MYLAR6 E2P-6H30211-Y42 MYLAR
UME1 HDMI Lable HDMI ROYALTY Y01-RHDMI03-000
UME2 BIOS Lable BIOS_LABEL G51-LA01678-A09
For MP

MICRO-STAR INT'L CO.,LTD.

Title	Screw/ME	
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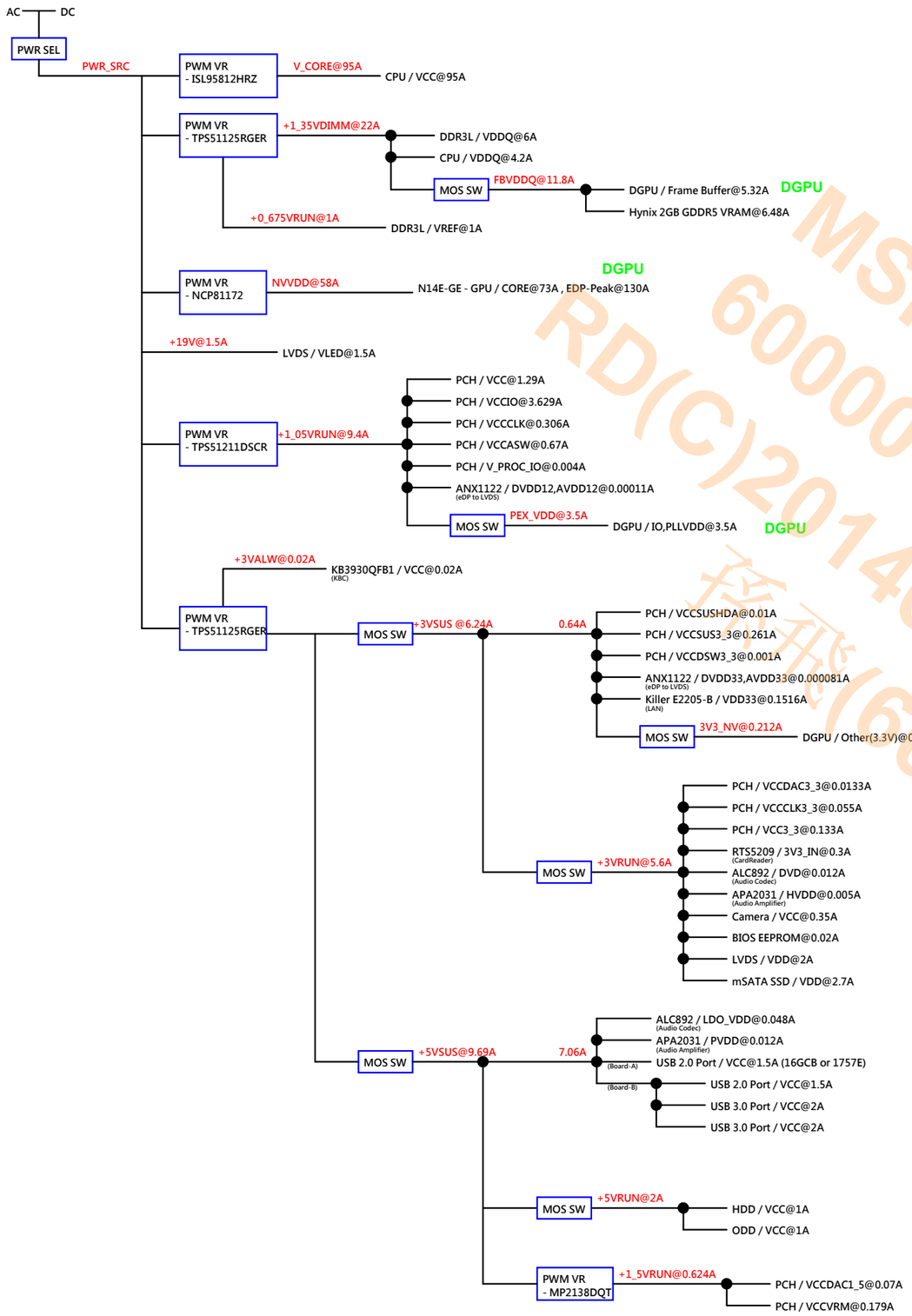
MS-16H2 Power Delivery Chart



msi	MICRO-STAR INT'L CO.,LTD.		
Title	Power Delivery Map		
Size	Document Number		Rev
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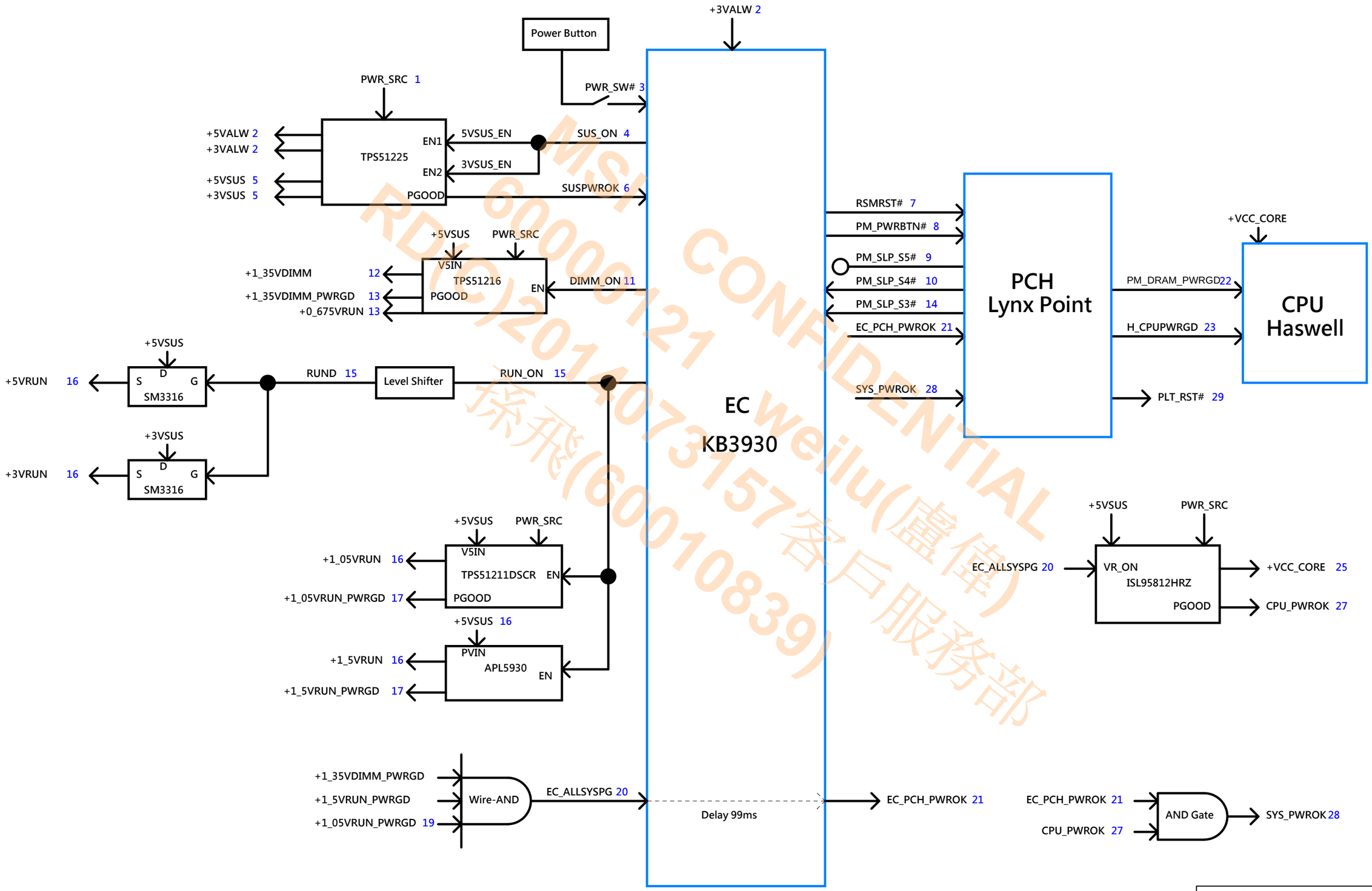
MS-16H2 Power on Block Diagram



msi MICRO-STAR INT'L CO.,LTD.			
Title: Power on Block Diagram			
Size	Document Number: MS-16H3		Rev: 1.0
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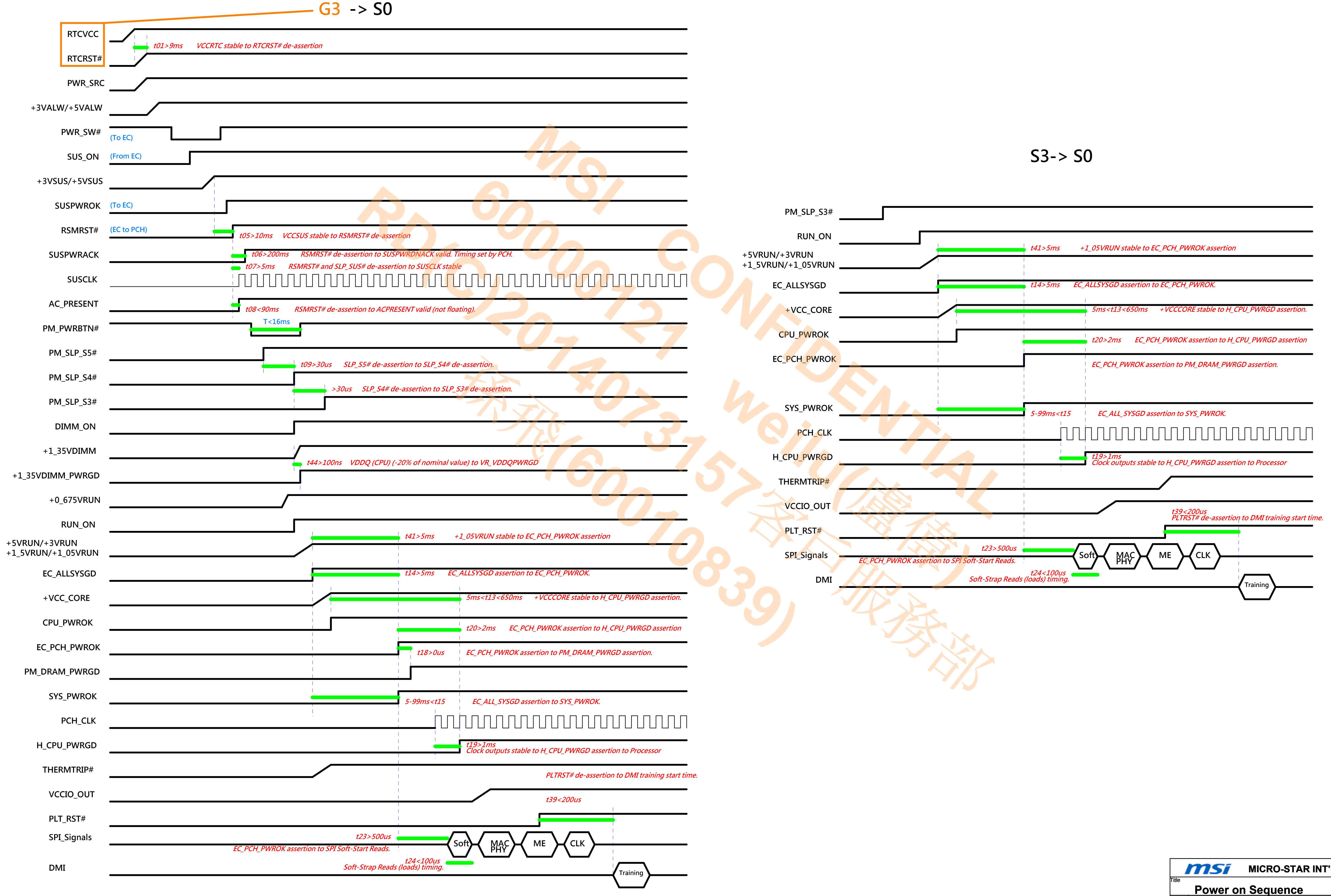
Power on Sequence



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Title	Power on Sequence	
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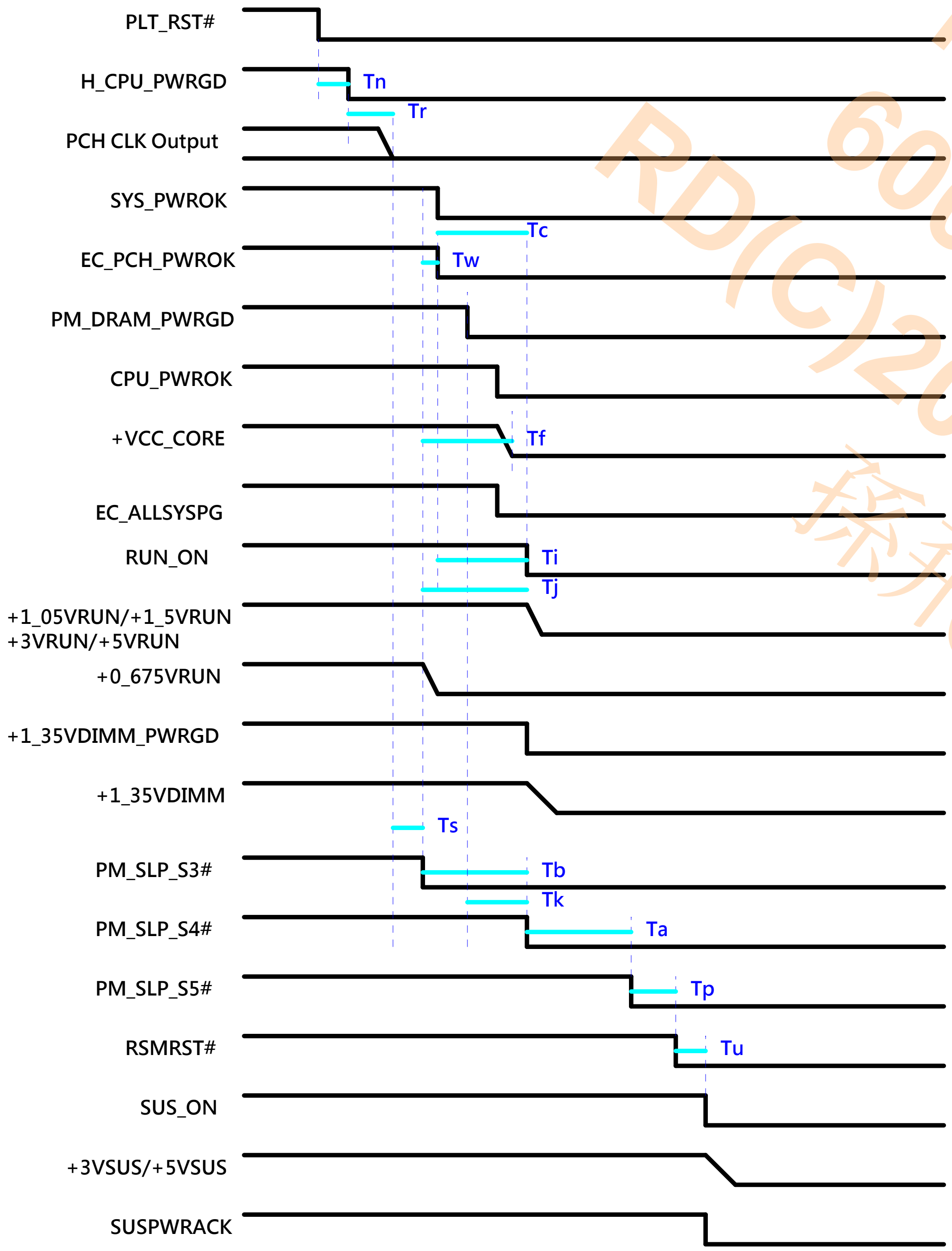
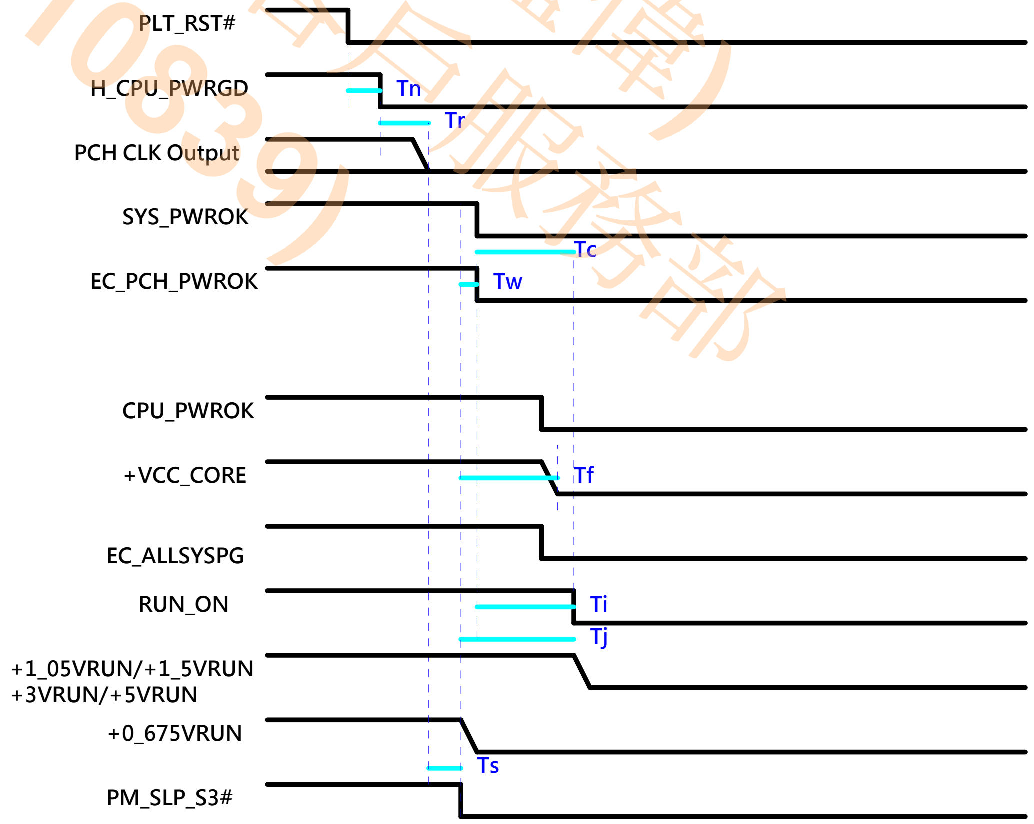
Power down Sequence

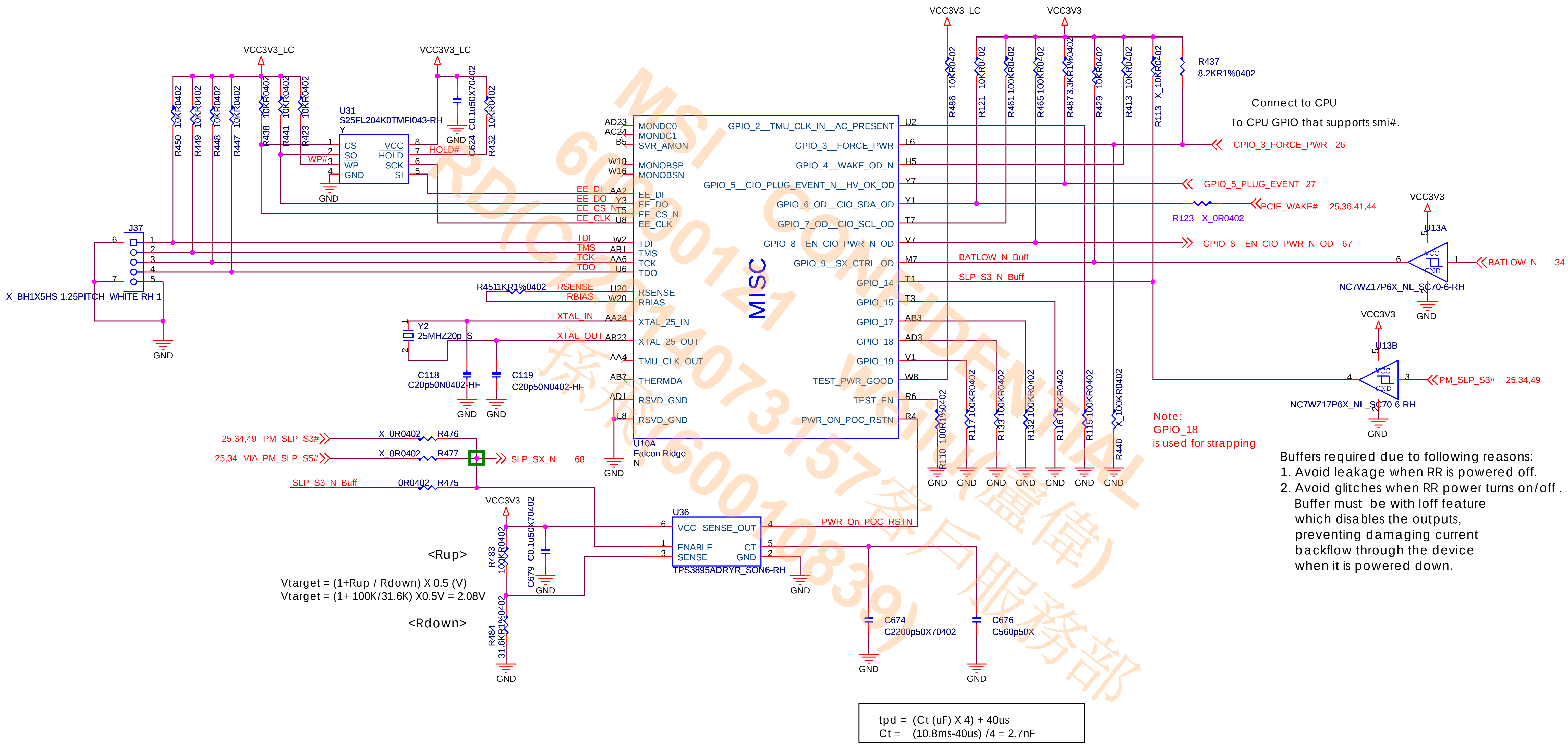
	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

S0 -> G3



S0 -> S3





MICRO-STAR INT'L CO.,LTD.

Title: INTEL Falcon Ridge 5320(2C)

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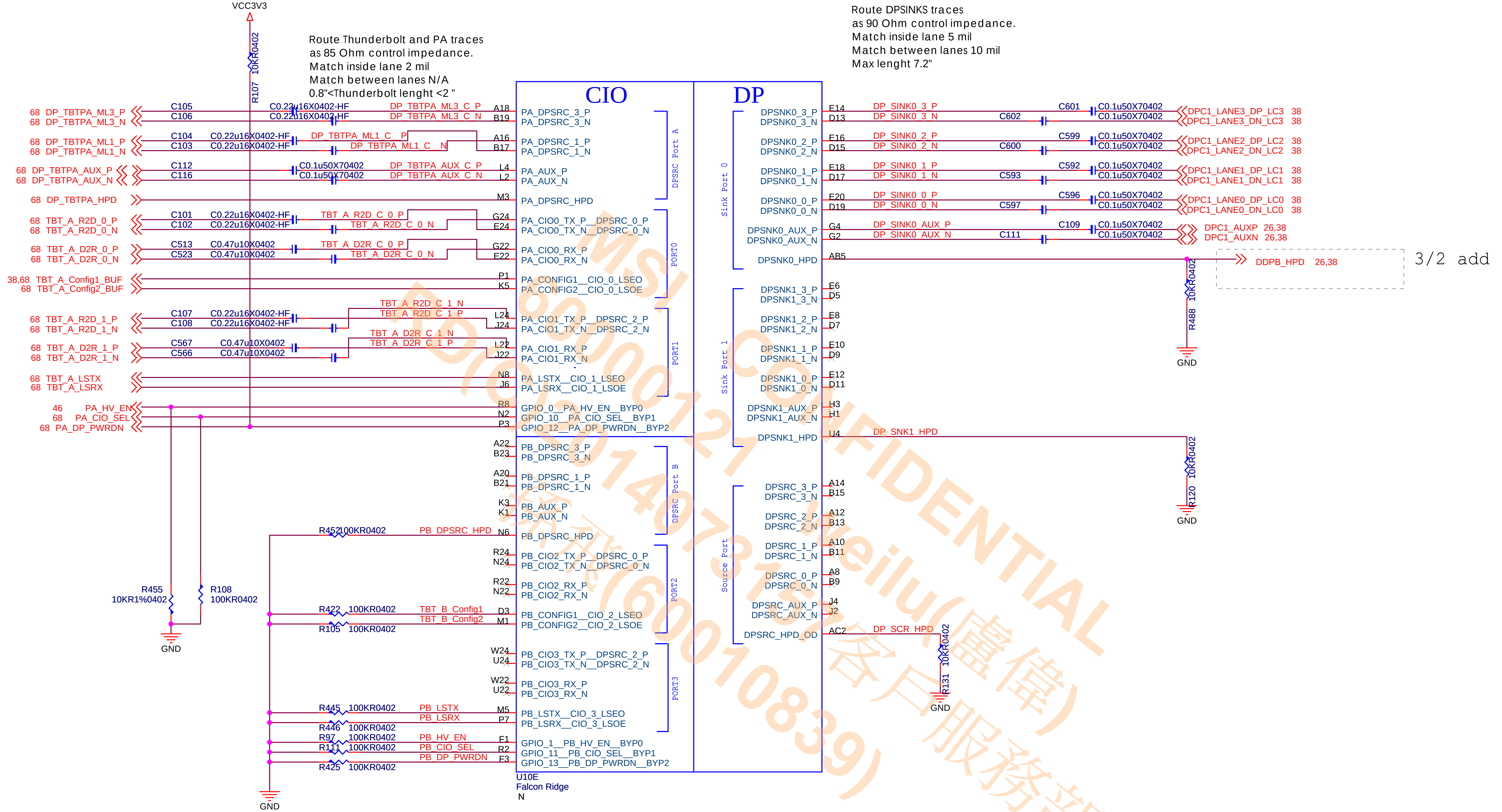
Route Thunderbolt and PA traces
as 85 Ohm control impedance.
Match inside lane 2 mil
Match between lanes N/A
0.8"<Thunderbolt lenght <2 "

Route DPSINKS traces
as 90 Ohm control impedance.
Match inside lane 5 mil
Match between lanes 10 mil
Max lenght 7.2"



VCC3V3
CIO
DP
R107 10KR0402
DP_TBTPA_ML3_P
DP_TBTPA_ML3_N
DP_TBTPA_ML1_P
DP_TBTPA_ML1_N
DP_TBTPA_AUX_P
DP_TBTPA_AUX_N
DP_TBTPA_HPD
TBT_A_R2D_0_P
TBT_A_R2D_0_N
TBT_A_D2R_0_P
TBT_A_D2R_0_N
TBT_A_Config1_BUF
TBT_A_Config2_BUF
TBT_A_R2D_1_P
TBT_A_R2D_1_N
TBT_A_D2R_1_P
TBT_A_D2R_1_N
TBT_A_LSTX
TBT_A_LSRX
PA_HV_EN
PA_CIO_SEL
PA_DP_PWRDN
R455 10KR1%0402
R108 100KR0402
GND
PA_DPSRC_3_P
PA_DPSRC_3_N
PA_DPSRC_1_P
PA_DPSRC_1_N
PA_AUX_P
PA_AUX_N
PA_DPSRC_HPD
PA_CIO0_TX_P__DPSRC_0_P
PA_CIO0_TX_N__DPSRC_0_N
PA_CIO0_RX_P
PA_CIO0_RX_N
PA_CONFIG1__CIO_0_LSEO
PA_CONFIG2__CIO_0_LSOE
PA_CIO1_TX_P__DPSRC_2_P
PA_CIO1_TX_N__DPSRC_2_N
PA_CIO1_RX_P
PA_CIO1_RX_N
PA_LSTX__CIO_1_LSEO
PA_LSRX__CIO_1_LSOE
GPIO_0__PA_HV_EN__BYP0
GPIO_10__PA_CIO_SEL__BYP1
GPIO_12__PA_DP_PWRDN__BYP2
PB_DPSRC_3_P
PB_DPSRC_3_N
PB_DPSRC_1_P
PB_DPSRC_1_N
PB_AUX_P
PB_AUX_N
PB_DPSRC_HPD
PB_CIO2_TX_P__DPSRC_0_P
PB_CIO2_TX_N__DPSRC_0_N
PB_CIO2_RX_P
PB_CIO2_RX_N
PB_CONFIG1__CIO_2_LSEO
PB_CONFIG2__CIO_2_LSOE
PB_CIO3_TX_P__DPSRC_2_P
PB_CIO3_TX_N__DPSRC_2_N
PB_CIO3_RX_P
PB_CIO3_RX_N
PB_LSTX__CIO_3_LSEO
PB_LSRX__CIO_3_LSOE
GPIO_1__PB_HV_EN__BYP0
GPIO_11__PB_CIO_SEL__BYP1
GPIO_13__PB_DP_PWRDN__BYP2
U10E
Falcon Ridge
DPSNK0_3_P
DPSNK0_3_N
DPSNK0_2_P
DPSNK0_2_N
DPSNK0_1_P
DPSNK0_1_N
DPSNK0_0_P
DPSNK0_0_N
DPSNK0_AUX_P
DPSNK0_AUX_N
DPSNK0_HPD
DPSNK1_3_P
DPSNK1_3_N
DPSNK1_2_P
DPSNK1_2_N
DPSNK1_1_P
DPSNK1_1_N
DPSNK1_0_P
DPSNK1_0_N
DPSNK1_AUX_P
DPSNK1_AUX_N
DPSNK1_HPD
DPSRC_3_P
DPSRC_3_N
DPSRC_2_P
DPSRC_2_N
DPSRC_1_P
DPSRC_1_N
DPSRC_0_P
DPSRC_0_N
DPSRC_AUX_P
DPSRC_AUX_N
DPSRC_HPD_OD
DPC1_LANE3_DP_LC3 38
DPC1_LANE3_DN_LC3 38
DPC1_LANE2_DP_LC2 38
DPC1_LANE2_DN_LC2 38
DPC1_LANE1_DP_LC1 38
DPC1_LANE1_DN_LC1 38
DPC1_LANE0_DP_LC0 38
DPC1_LANE0_DN_LC0 38
DPC1_AUXP 26,38
DPC1_AUXN 26,38
DDPB_HPD 26,38
3/2 add
R488 10KR0402
R120 10KR0402
R131 10KR0402
DP_SNK1_HPD
DP_SCR_HPD

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Title: INTEL Falcon Ridge 5320(2C)

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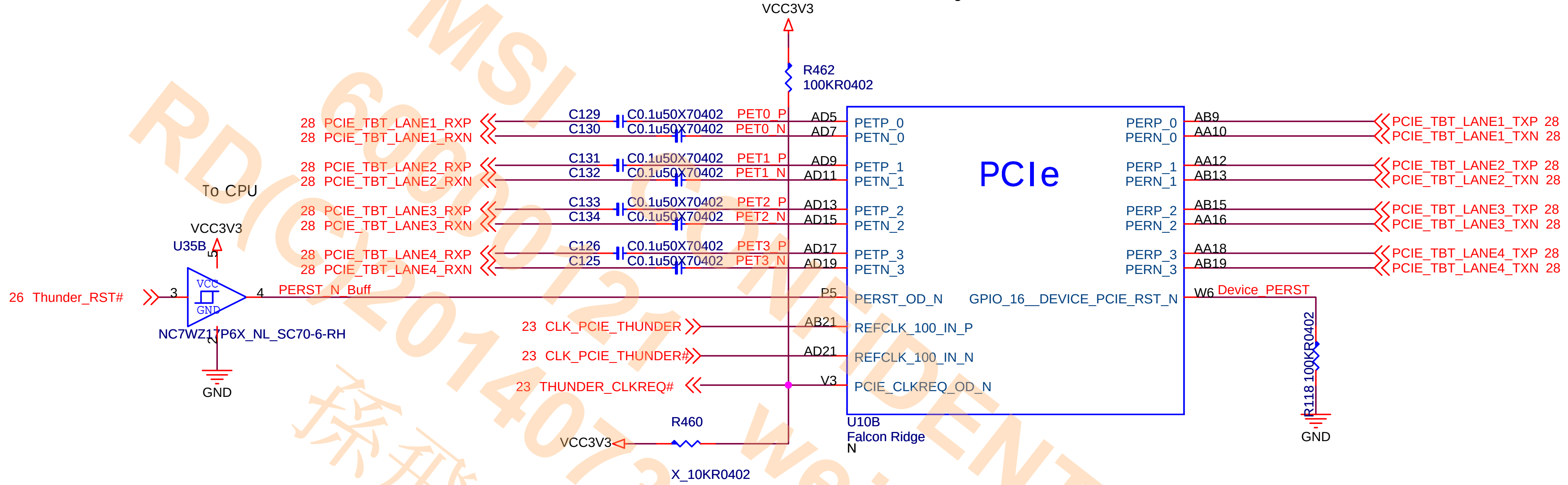
Route PCIe traces
as 85 Ohm control impedance
Match inside lanes 5mil
Match between lanes N/A
Max lenght 10"



Buffer required due to following reasons:
1. Avoid leakage when RR is powered off.
2. Avoid glitches when RR power turns on/off .
Buffer must be with Ioff feature which disables the outputs, preventing damaging current backflow through the device when it is powered down.

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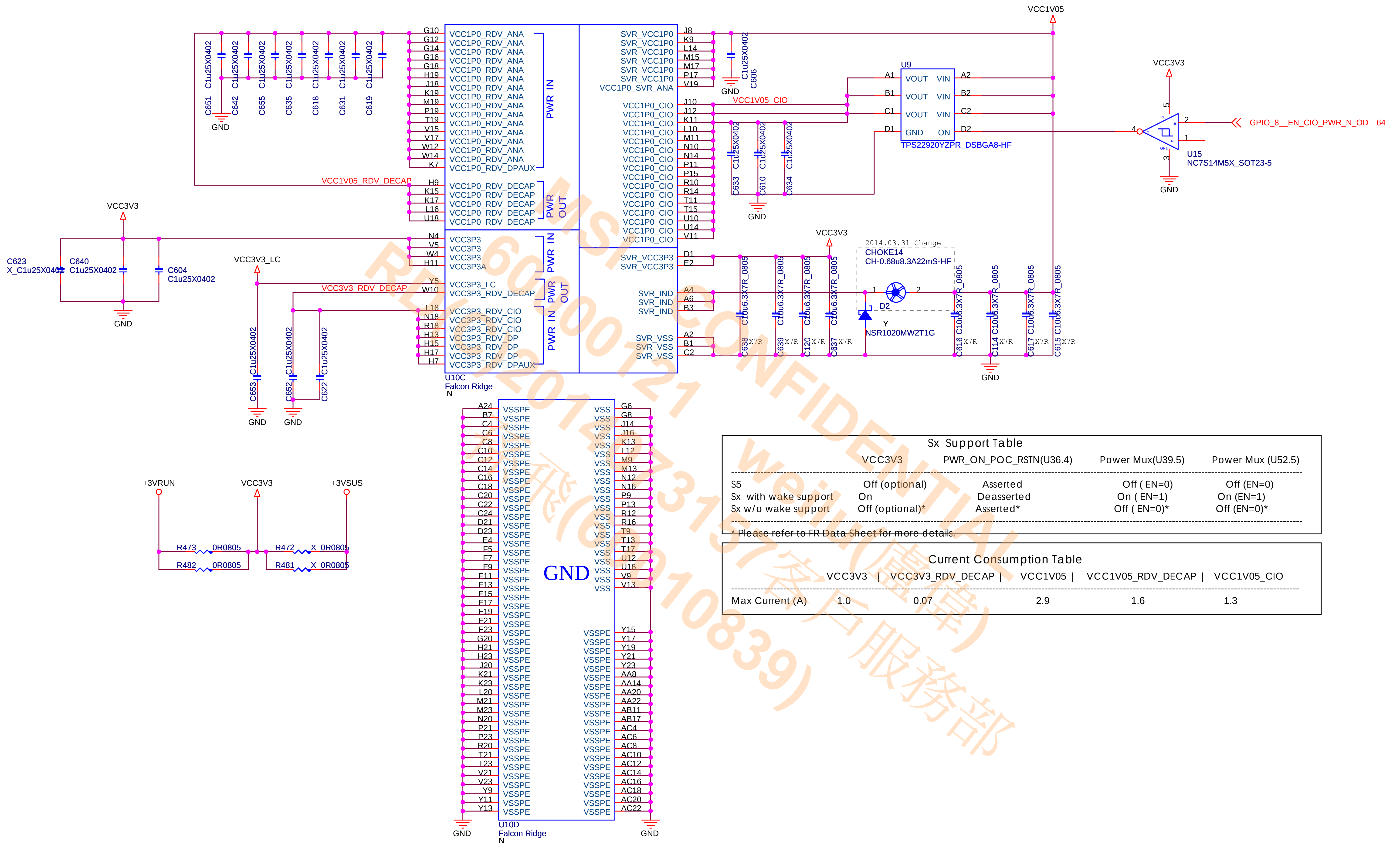

Sx Support Table

	VCC3V3	PWR_ON_POC_RSTN(U36.4)	Power Mux(U39.5)	Power Mux (U52.5)
S5	Off (optional)	Asserted	Off (EN=0)	Off (EN=0)
Sx with wake support	On	Deasserted	On (EN=1)	On (EN=1)
Sx w/o wake support	Off (optional)*	Asserted*	Off (EN=0)*	Off (EN=0)*

* Please refer to FR Data Sheet for more details.

Current Consumption Table

	VCC3V3	VCC3V3_RDV_DECAP	VCC1V05	VCC1V05_RDV_DECAP	VCC1V05_CIO
Max Current (A)	1.0	0.07	2.9	1.6	1.3

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Title: INTEL Falcon Ridge 5320(2C)

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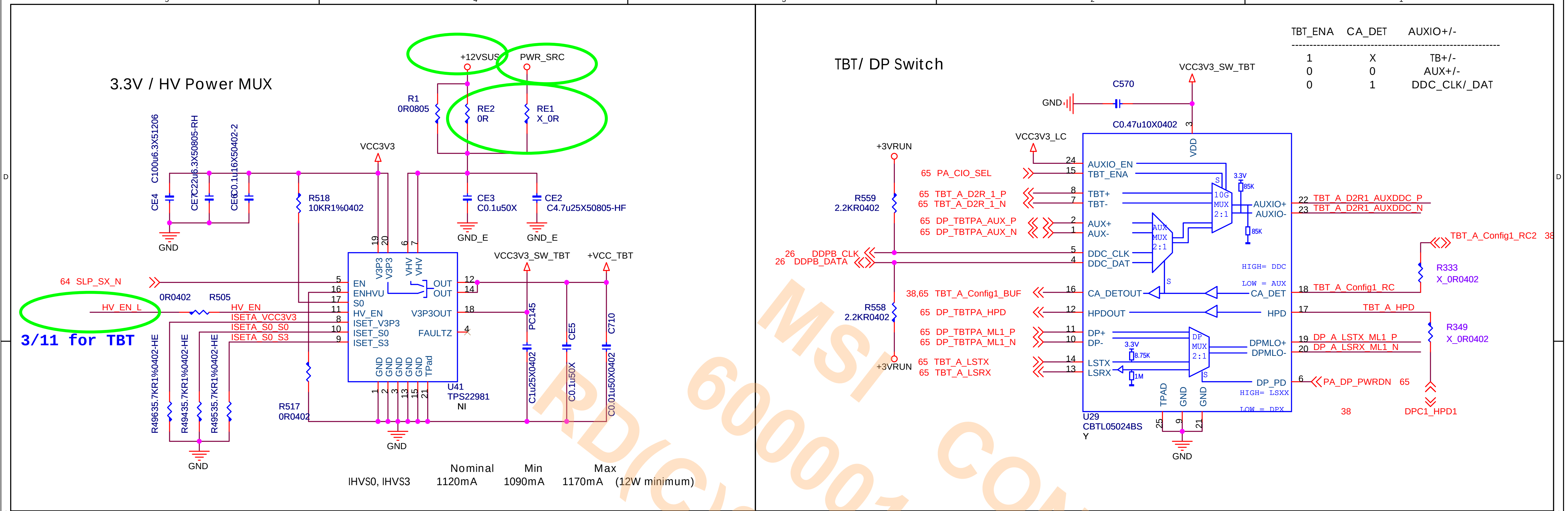
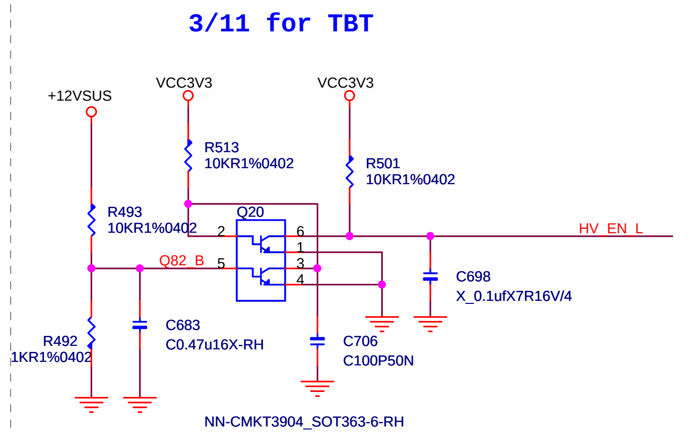
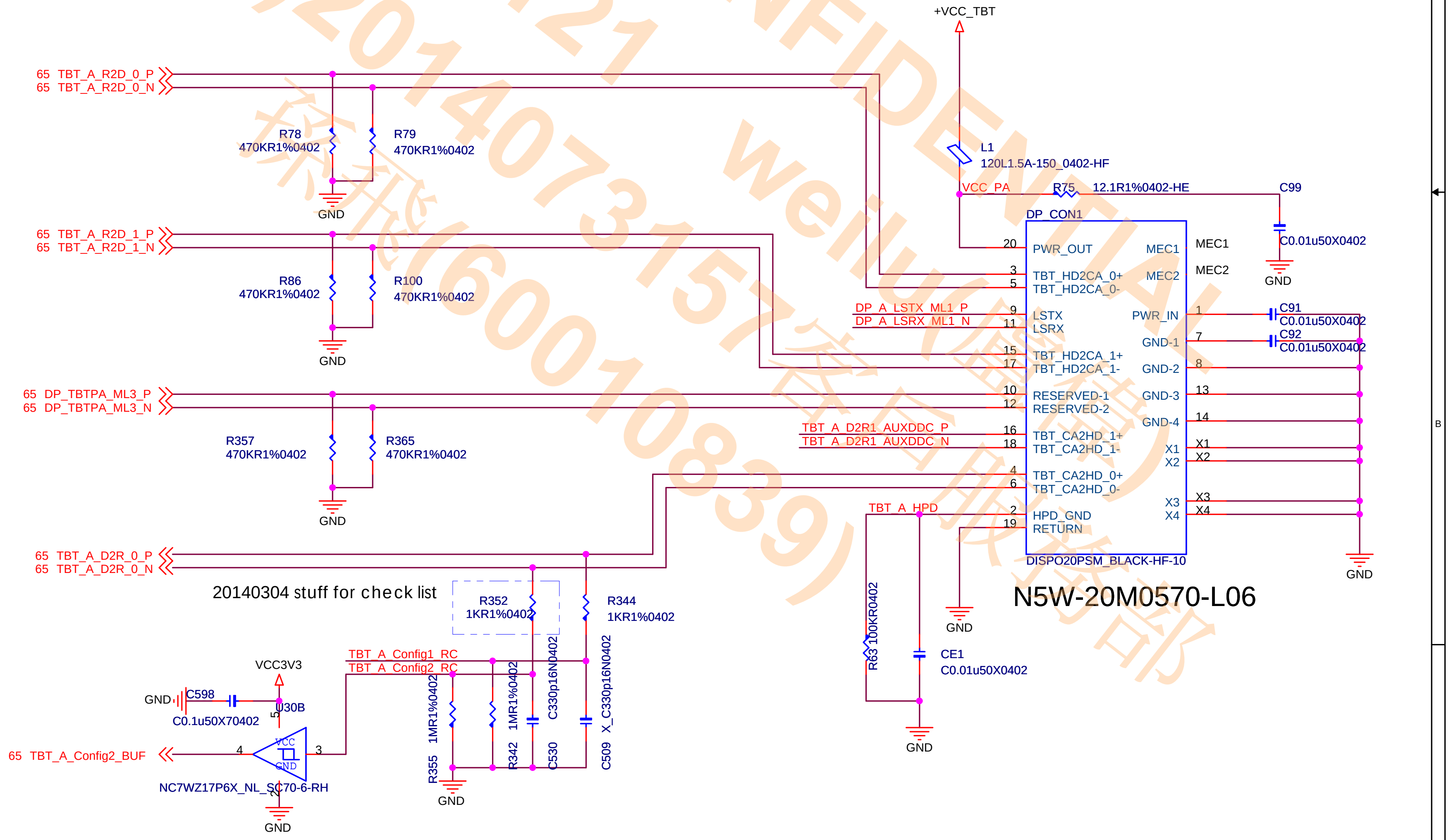




Power mux will be
on when VCC12V0 >=4.5V and
off when VCC12V0 <=3.4V
Vbe=770mV@Ic=10mA -->
4.5X2.05K/(10K+2.05K) = 0.766V

Note:
If generating the 12v from a supply
different than 3.3v - resistors values of
R52 and R53 should be different
Example: If VCC12V0 is boosted from 5V,
the R52 is 10K ohm and R53 is 1K ohm



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Title	INTEL Falcon Ridge 5320(2C)	
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History

0A: Hardware part

01.RB4 , RB6 RB5 , RB7 , RB9 , RB10 470R change to 680R
02. Modify WLAN CLKREQ SCH , add R101
03. R440 unstuff , R437 stuff
04. Add TBT DDC Pull-high 2.2K , R558 and R559
05. RA2 and RA6 unstuff
06. Add U46 sch for ASM1042 1.05VRUN
07. Modify HDMI SCH , D3 change to D01-BAT5429-D07 ,add C782 and C783
08. CPU change part number for each item.
09. Samsung VRAM EOL , change to Hynix
10. Add C785 and C784 for PWR_SCR
11. Add C786 for 3VRUN
12. Add C787 for VBATA
13. R396 change connect to 3VSUS
14. rename 3V3_NV to +3V3_NV
15. Swap RTC pin
16. change EL3 , ELA5 , ELA2 and LI6 PN to L12-9008100-I05
17. R30 change to 10k and C67 , C68 unstuff for EC_ALLSYSPG sequency
18. Revese Q6, Q15, Q19 DS pin for power on sequence
19. C594 unstuff
20. R40 change to 0ohm and C77 unstuff
21. Add eight RF clamp
22. remove F1
23. R387 change to 47K
24. Add PQ62 sch for DGPU power control
25. EC59 stuff
26. ASM 1042 SCH unstuff

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