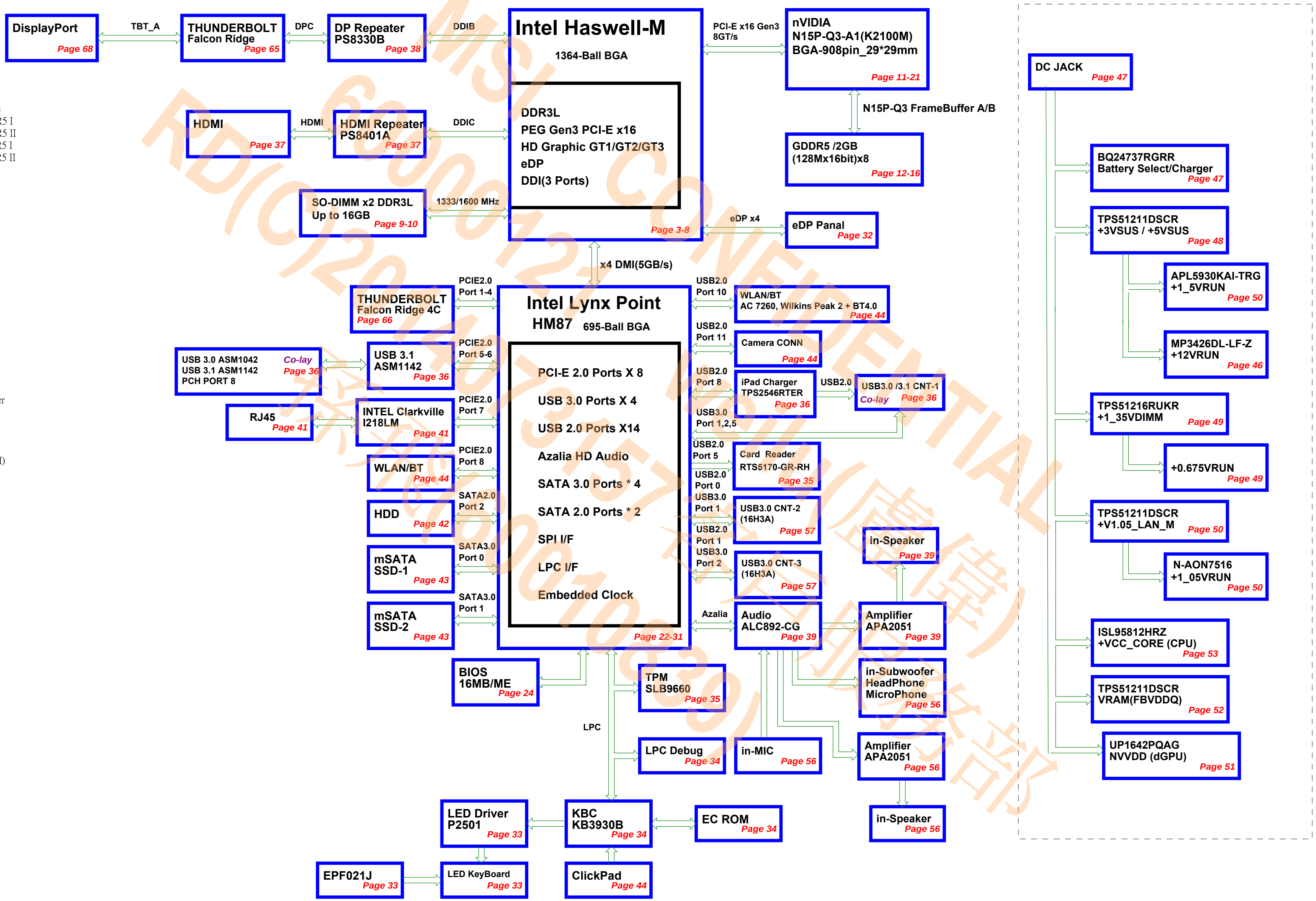
MS-16H3 Ver:0A

Tuesday, May 20, 2014

Shark Bay Mobile



MSI	MICRO-STAR INT'L CO.,LTD.
Title	Block Diagram
Document Number	MS-16H3
Rev	0B
Sheet	1 of 69

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	DIMM_ON
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUN_ON
+VCC_CORE	1.8V Core Voltage for Processor	EC_ALLSYSPG
+1_05VRUN	1.05V rail for Processor	RUN_ON
NVVDD	V Core Voltage for nVIDIA dGPU	NVVDD_EN
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	FBVDDQ_ON
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	NVVDD_EN

Net Naming Conventions

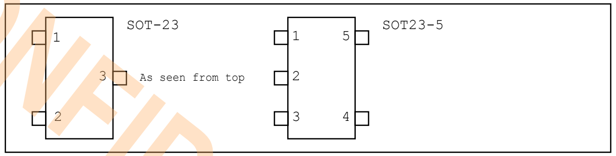
Suffix

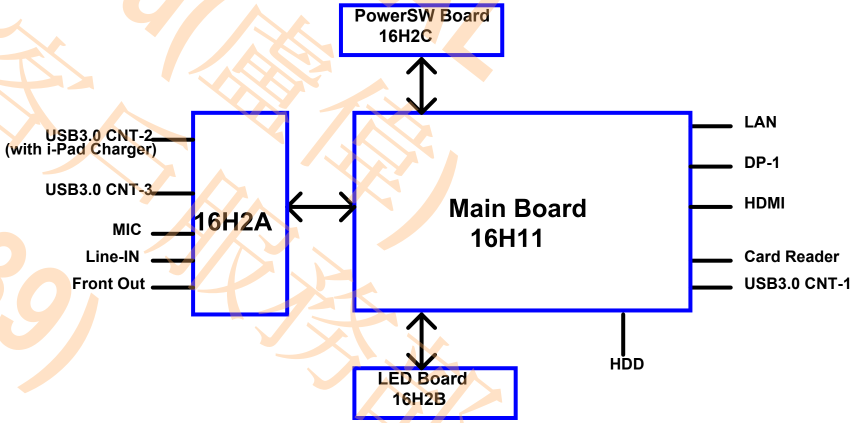
```
#  =  Active Low Signal
```

Prefix

```
H  =  Host
M  =  DDR Memory
TP =  Test Point (does not connect anywhere else)
FB = DGPU VRAM
VIAxxx =  Like Test Point, but using VIA.
```

PCB Footprints





POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

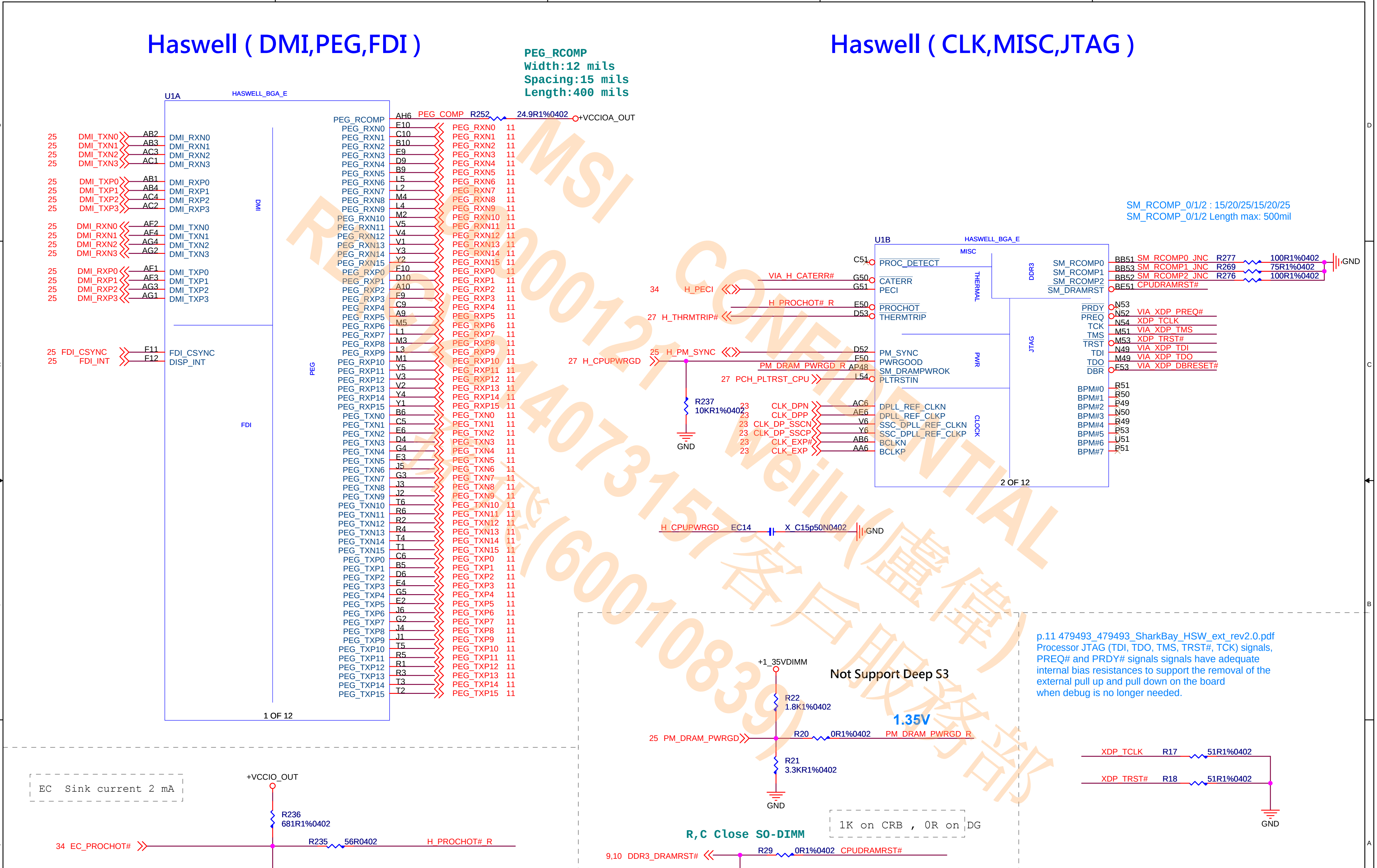
Note : WHEN AC MODE , System turn on and +V*SUS always keep high

MICRO-STAR INT'L CO.,LTD.

Title: Platform

Size | Document Number: MS-16H3 | Rev: 0B

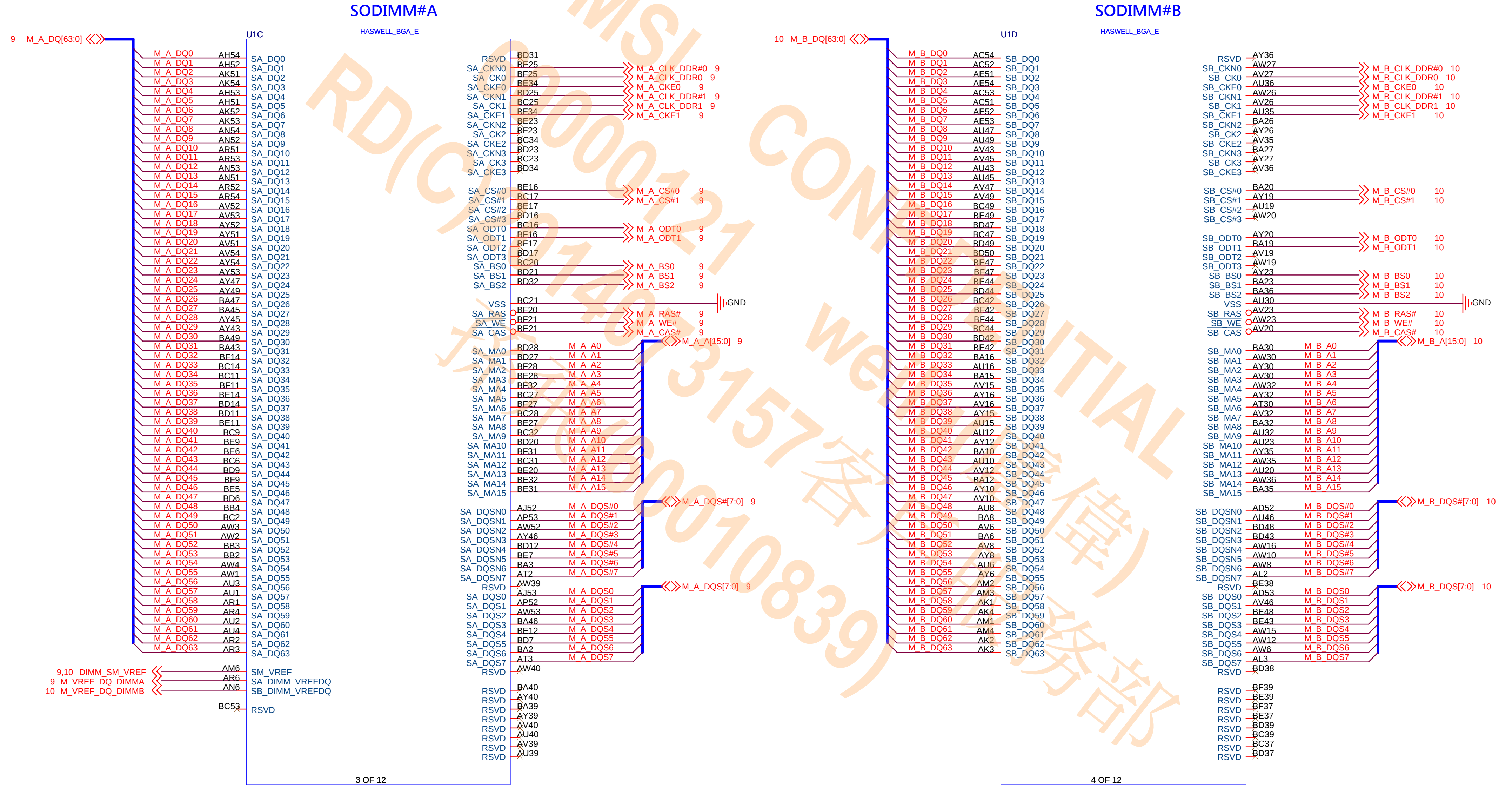
Date: Tuesday, May 20, 2014 | Sheet 2 of 69


Haswell (DMI,PEG,FDI)
Haswell (CLK,MISC,JTAG)
PEG_RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils
U1A
HASWELL_BGA_E
DMI_RXN0
DMI_RXN1
DMI_RXN2
DMI_RXN3
DMI_RXP0
DMI_RXP1
DMI_RXP2
DMI_RXP3
DMI_TXN0
DMI_TXN1
DMI_TXN2
DMI_TXN3
DMI_TXP0
DMI_TXP1
DMI_TXP2
DMI_TXP3
FDI_CSYNC
DISP_INT
FDI_INT
DMI
PEG
FDI
1 OF 12
PEG_RCOMP
PEG_COMP
R252
24.9R1%0402
+VCCIOA_OUT
PEG_RXN0 ... PEG_RXN15
PEG_RXP0 ... PEG_RXP15
PEG_TXN0 ... PEG_TXN15
PEG_TXP0 ... PEG_TXP15
SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil
U1B
HASWELL_BGA_E
MISC
PROC_DETECT
CATERR
PECI
PROCHOT
THERMTRIP
THERMAL
DDR3
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
SM_DRAMRST
SM_RCOMP0_JNC
SM_RCOMP1_JNC
SM_RCOMP2_JNC
R277
R269
R276
100R1%0402
75R1%0402
100R1%0402
GND
CPUDRAMRST#
VIA_H_CATERR#
H_PECI
H_PROCHOT#_R
H_THRMTRIP#
PRDY
PREQ
TCK
TMS
TRST
TDI
TDO
DBR
JTAG
VIA_XDP_PREQ#
XDP_TCLK
VIA_XDP_TMS
XDP_TRST#
VIA_XDP_TDI
VIA_XDP_TDO
VIA_XDP_DBRESET#
H_PM_SYNC
H_CPUPWRGD
PM_DRAM_PWRGD_R
PCH_PLTRST_CPU
PM_SYNC
PWRGOOD
SM_DRAMPWROK
PLTRSTIN
PWR
R237
10KR1%0402
GND
CLK_DPN
CLK_DPP
CLK_DP_SSCN
CLK_DP_SSCP
CLK_EXP#
CLK_EXP
DPLL_REF_CLKN
DPLL_REF_CLKP
SSC_DPLL_REF_CLKN
SSC_DPLL_REF_CLKP
BCLKN
BCLKP
CLOCK
BPM#0
BPM#1
BPM#2
BPM#3
BPM#4
BPM#5
BPM#6
BPM#7
2 OF 12
H_CPUPWRGD
EC14
X_C15p50N0402
GND
p.11 479493_479493_SharkBay_HSW_ext_rev2.0.pdf
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals,
PREQ# and PRDY# signals signals have adequate
internal bias resistances to support the removal of the
external pull up and pull down on the board
when debug is no longer needed.
+1_35VDIMM
Not Support Deep S3
R22
1.8K1%0402
1.35V
25 PM_DRAM_PWRGD
R20
0R1%0402
PM_DRAM_PWRGD_R
R21
3.3KR1%0402
GND
1K on CRB , 0R on DG
R,C Close SO-DIMM
9,10 DDR3_DRAMRST#
R29
0R1%0402
CPUDRAMRST#
EC1
X_C0.1u50X70402
GND
XDP_TCLK
R17
51R1%0402
XDP_TRST#
R18
51R1%0402
GND
EC Sink current 2 mA
+VCCIO_OUT
R236
681R1%0402
34 EC_PROCHOT#
R235
56R0402
H_PROCHOT#_R
53 IMVP_PROCHOT#
JNC7
X_0402
47P close PWM

MICRO-STAR INT'L CO.,LTD.

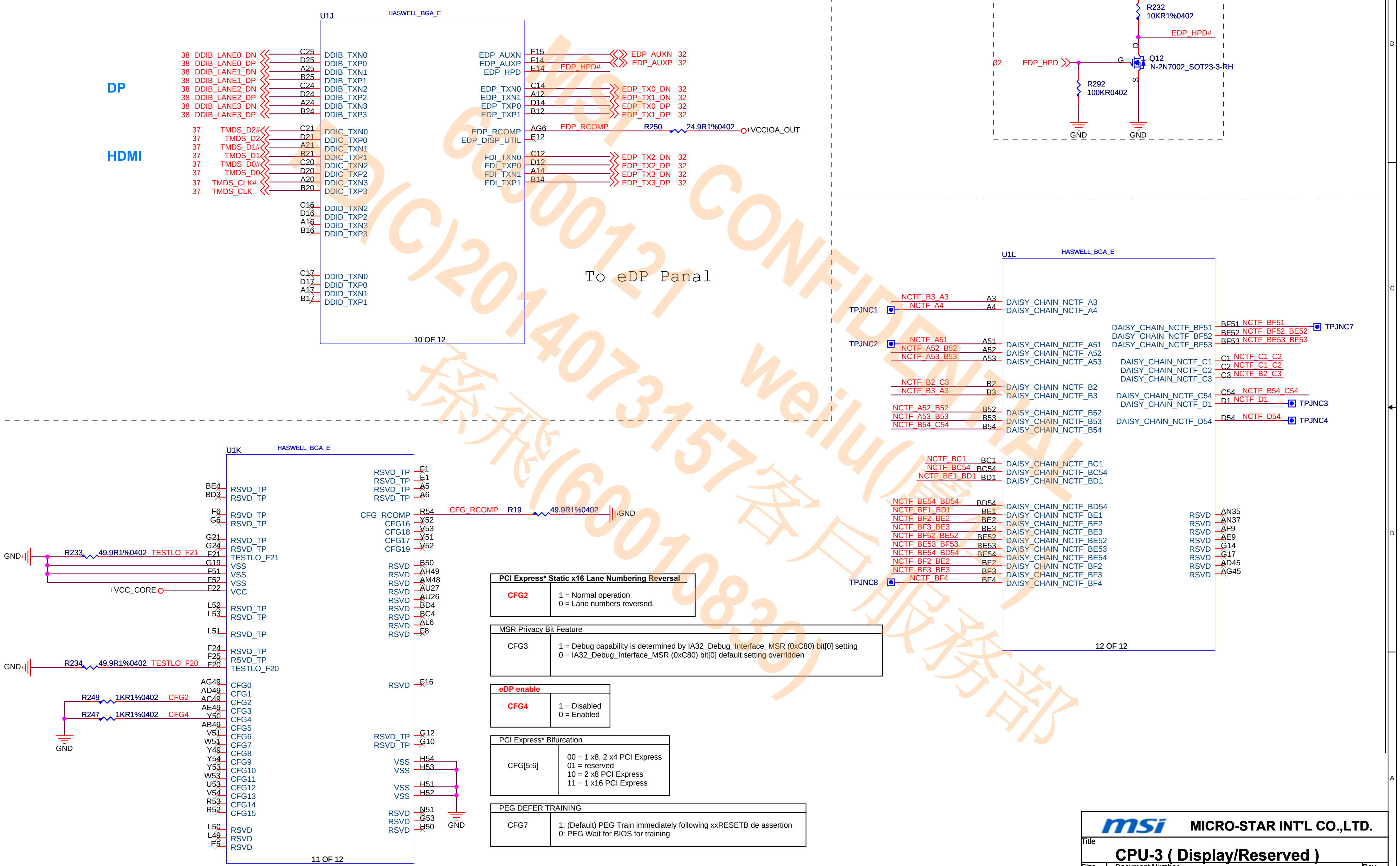
Title	CPU-1 (Host Bus)	
Size	Document Number: MS-16H3	Rev: 0B
Date: Tuesday, May 20, 2014	Sheet 3 of 69	

Haswell (DDR3L)



msi	MICRO-STAR INT'L CO.,LTD.
Title	CPU-2 (DDR3L)
Size / Document Number	MS-16H3
Rev	0B
Date:	Tuesday, May 20, 2014
Sheet	4 of 69

Display/Reserved



PCI Express* Static x16 Lane Numbering Reversal

CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature

CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable

CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation

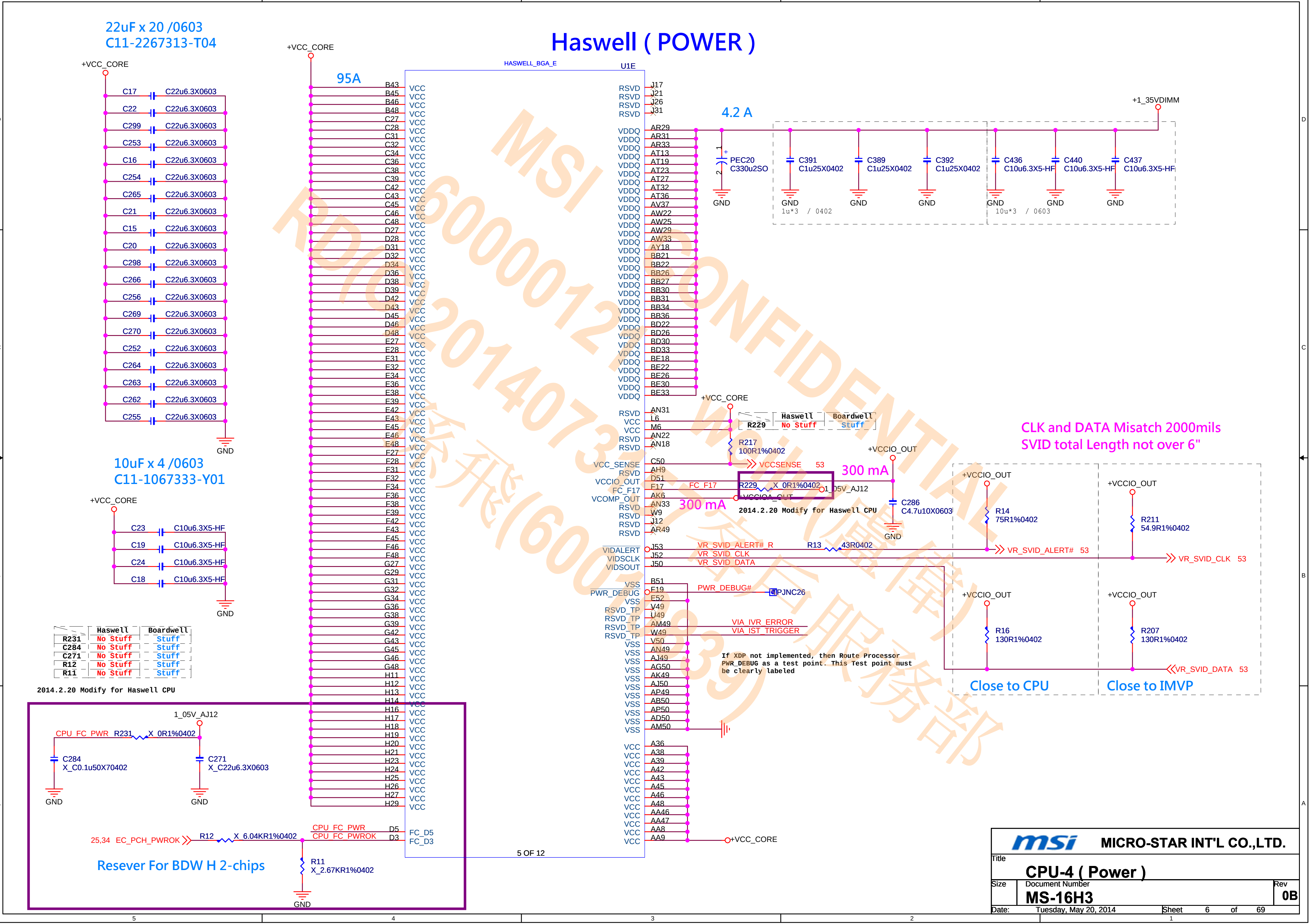
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING

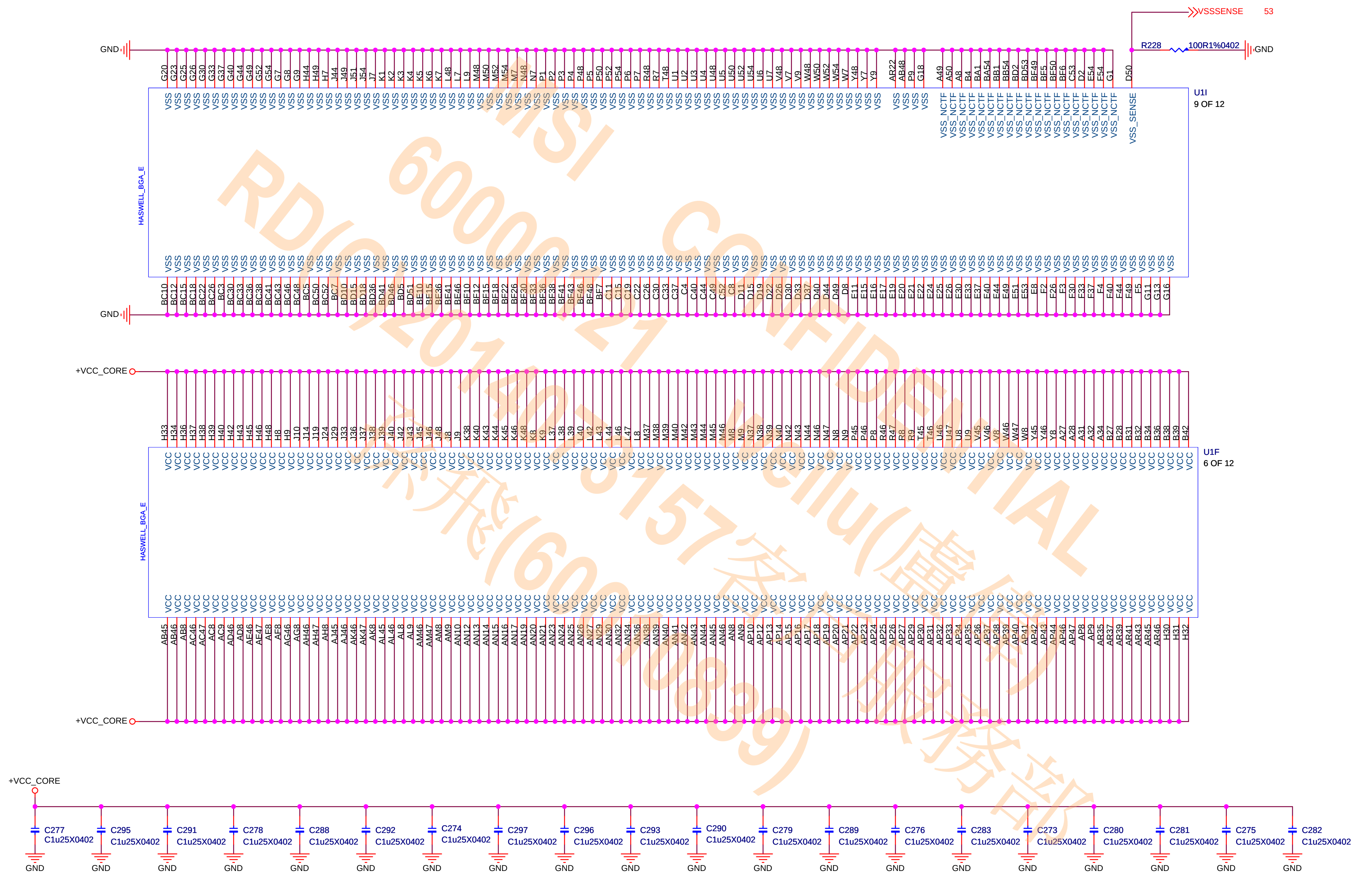
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

msi	MICRO-STAR INT'L CO.,LTD.	
Title	CPU-3 (Display/Reserved)	
Size	Document Number MS-16H3	Rev 0B
Date: Tuesday, May 20, 2014	Sheet 5 of 69	

Haswell (POWER)


22uF x 20 /0603
C11-2267313-T04
+VCC_CORE
C17 C22u6.3X0603
C22 C22u6.3X0603
C299 C22u6.3X0603
C253 C22u6.3X0603
C16 C22u6.3X0603
C254 C22u6.3X0603
C265 C22u6.3X0603
C21 C22u6.3X0603
C15 C22u6.3X0603
C20 C22u6.3X0603
C298 C22u6.3X0603
C266 C22u6.3X0603
C256 C22u6.3X0603
C269 C22u6.3X0603
C270 C22u6.3X0603
C252 C22u6.3X0603
C264 C22u6.3X0603
C263 C22u6.3X0603
C262 C22u6.3X0603
C255 C22u6.3X0603
GND
10uF x 4 /0603
C11-1067333-Y01
C23 C10u6.3X5-HF
C19 C10u6.3X5-HF
C24 C10u6.3X5-HF
C18 C10u6.3X5-HF
Haswell | Boardwell
R231 No Stuff | Stuff
C284 No Stuff | Stuff
C271 No Stuff | Stuff
R12 No Stuff | Stuff
R11 No Stuff | Stuff
2014.2.20 Modify for Haswell CPU
1_05V_AJ12
CPU_FC_PWR R231 X_0R1%0402
C284 X_C0.1u50X70402
C271 X_C22u6.3X0603
25,34 EC_PCH_PWROK R12 X_6.04KR1%0402
R11 X_2.67KR1%0402
CPU_FC_PWR
CPU_FC_PWROK
Reserver For BDW H 2-chips
95A
HASWELL_BGA_E
U1E
5 OF 12
FC_D5
FC_D3
4.2 A
+1_35VDIMM
PEC20 C330u2SO
C391 C1u25X0402
C389 C1u25X0402
C392 C1u25X0402
C436 C10u6.3X5-HF
C440 C10u6.3X5-HF
C437 C10u6.3X5-HF
1u*3 / 0402
10u*3 / 0603
R229 Haswell No Stuff | Boardwell Stuff
R217 100R1%0402
VCC_SENSE
VCCSENSE 53
300 mA
+VCCIO_OUT
FC_F17
R229 X_0R1%0402
1_05V_AJ12
VCCIOA_OUT
300 mA
2014.2.20 Modify for Haswell CPU
C286 C4.7u10X0603
CLK and DATA Misatch 2000mils
SVID total Length not over 6"
R14 75R1%0402
R211 54.9R1%0402
VIDALERT
VIDSCLK
VIDSOUT
VR_SVID_ALERT#_R
R13 43R0402
VR_SVID_ALERT# 53
VR_SVID_CLK
VR_SVID_CLK 53
VR_SVID_DATA
PWR_DEBUG#
PJNC26
VIA_IVR_ERROR
VIA_IST_TRIGGER
R16 130R1%0402
R207 130R1%0402
VR_SVID_DATA 53
If XDP not implemented, then Route Processor PWR_DEBUG as a test point. This Test point must be clearly labeled
Close to CPU
Close to IMVP
msi MICRO-STAR INT'L CO.,LTD.
Title
CPU-4 (Power)
Size
Document Number
MS-16H3
Rev
0B
Date: Tuesday, May 20, 2014
Sheet 6 of 69

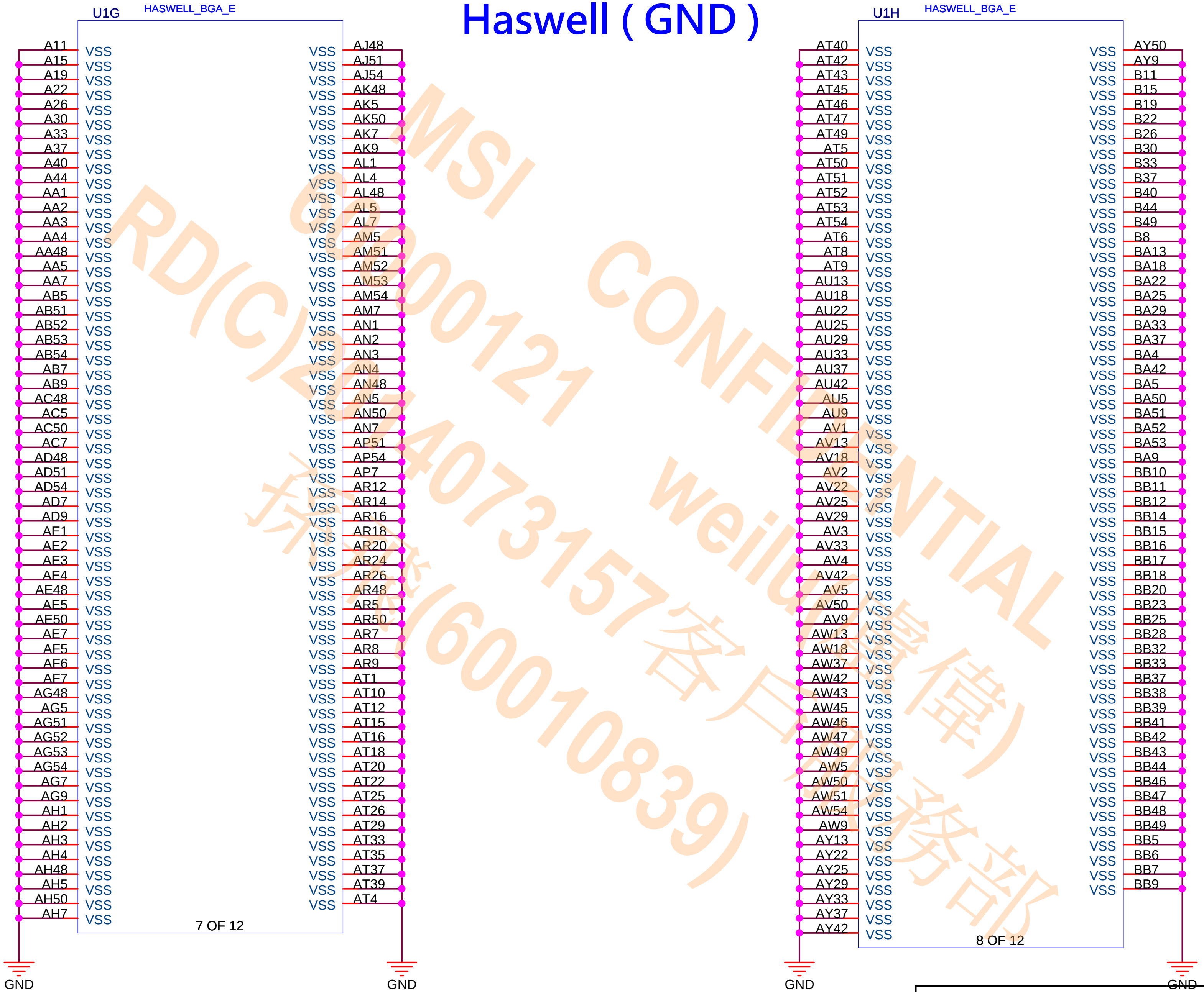
Haswell (Power & GND)



MICRO-STAR INT'L CO.,LTD.

Title	CPU-6 (Power & GND)
Size / Document Number	MS-16H3
Rev	0B
Date:	Tuesday, May 20, 2014
Sheet	7 of 69

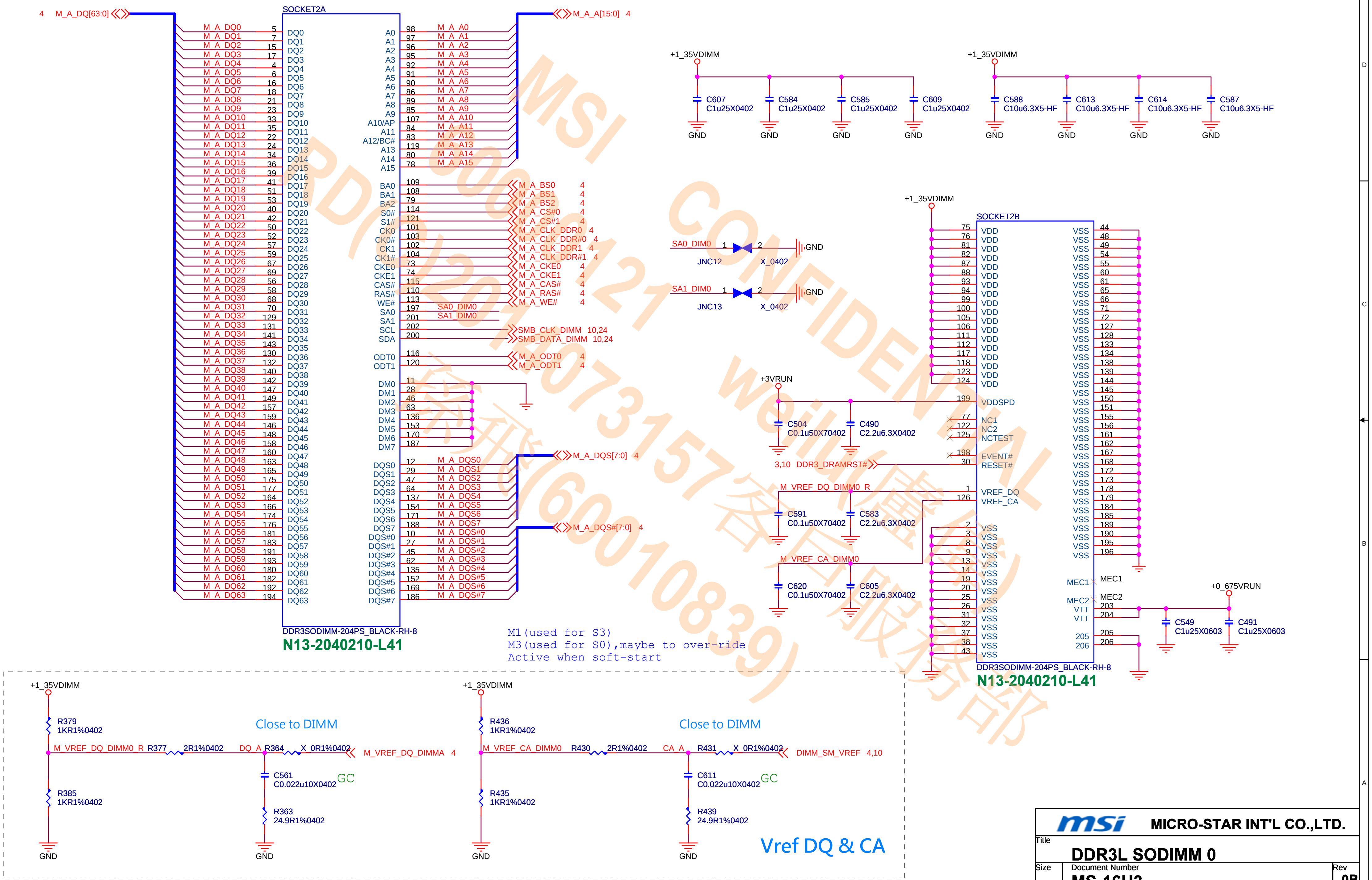
Haswell (GND)



MICRO-STAR INT'L CO.,LTD.

Title	CPU-5 (GND)	
Size	Document Number: MS-16H3	Rev: 0B
Date: Tuesday, May 20, 2014	Sheet 8 of 69	

SODIMM#A



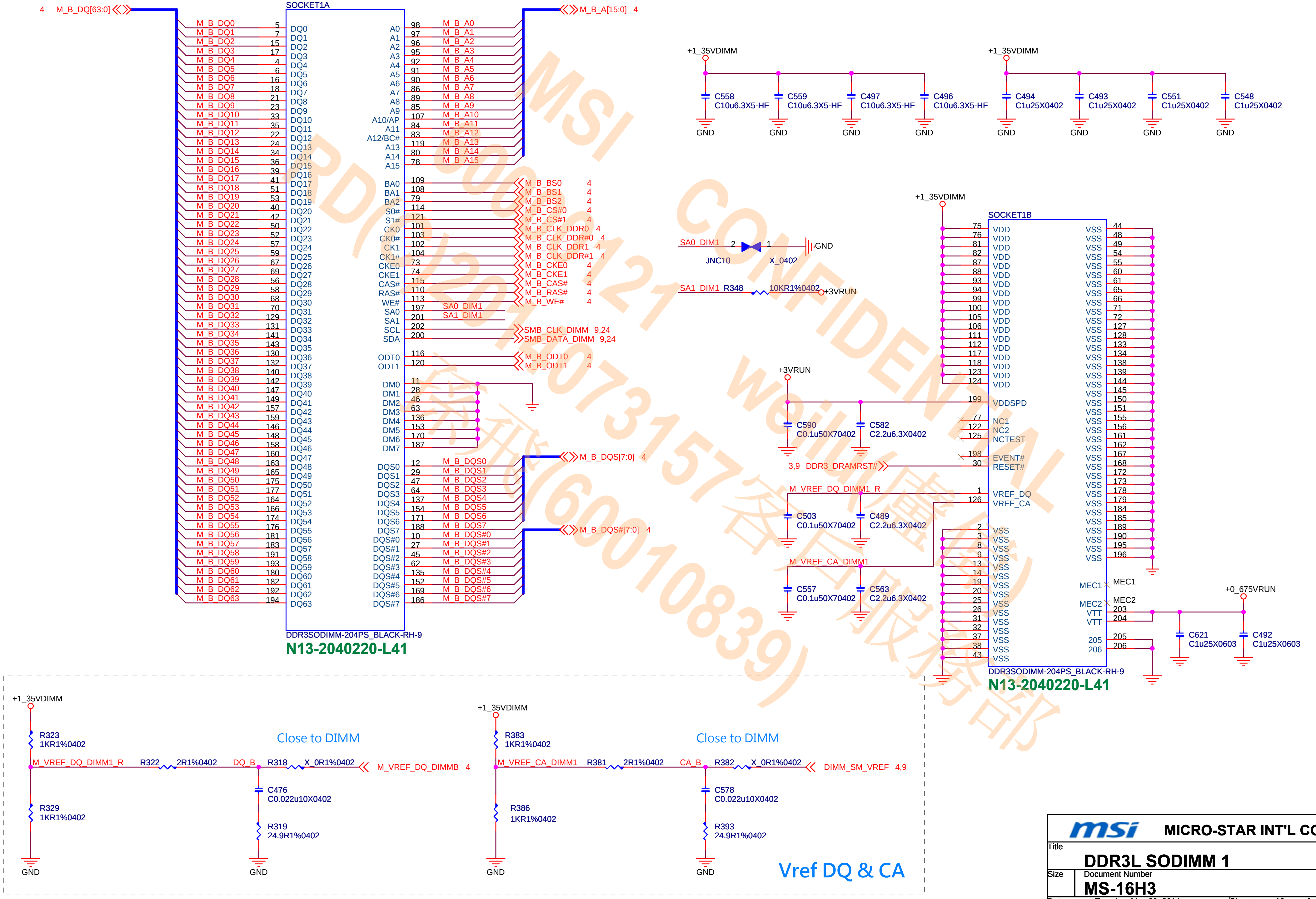
MICRO-STAR INT'L CO.,LTD.

Title: **DDR3L SODIMM 0**

Size	Document Number	Rev
	MS-16H3	0B

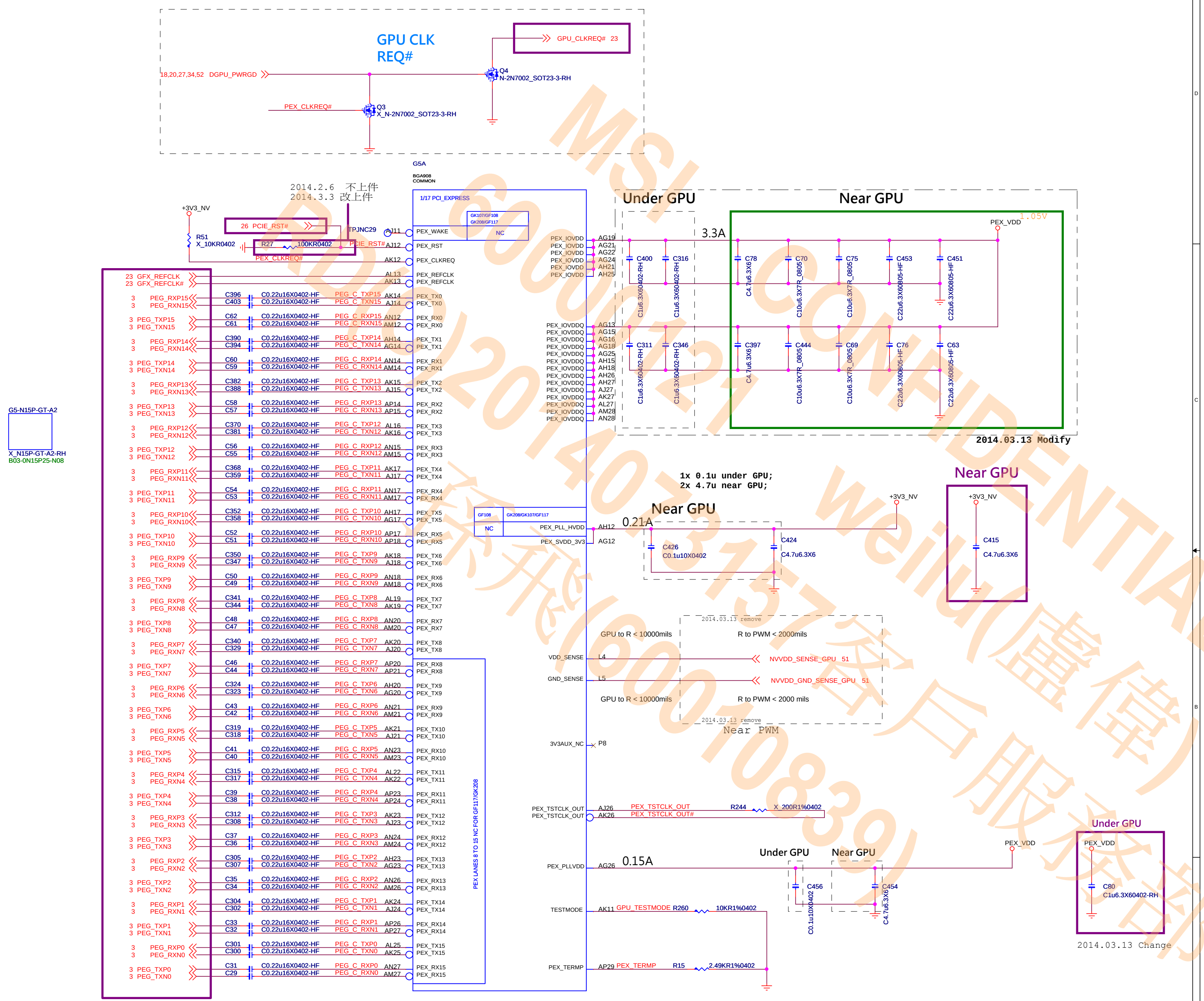
Date: Tuesday, May 20, 2014 Sheet 9 of 69

SODIMM#B



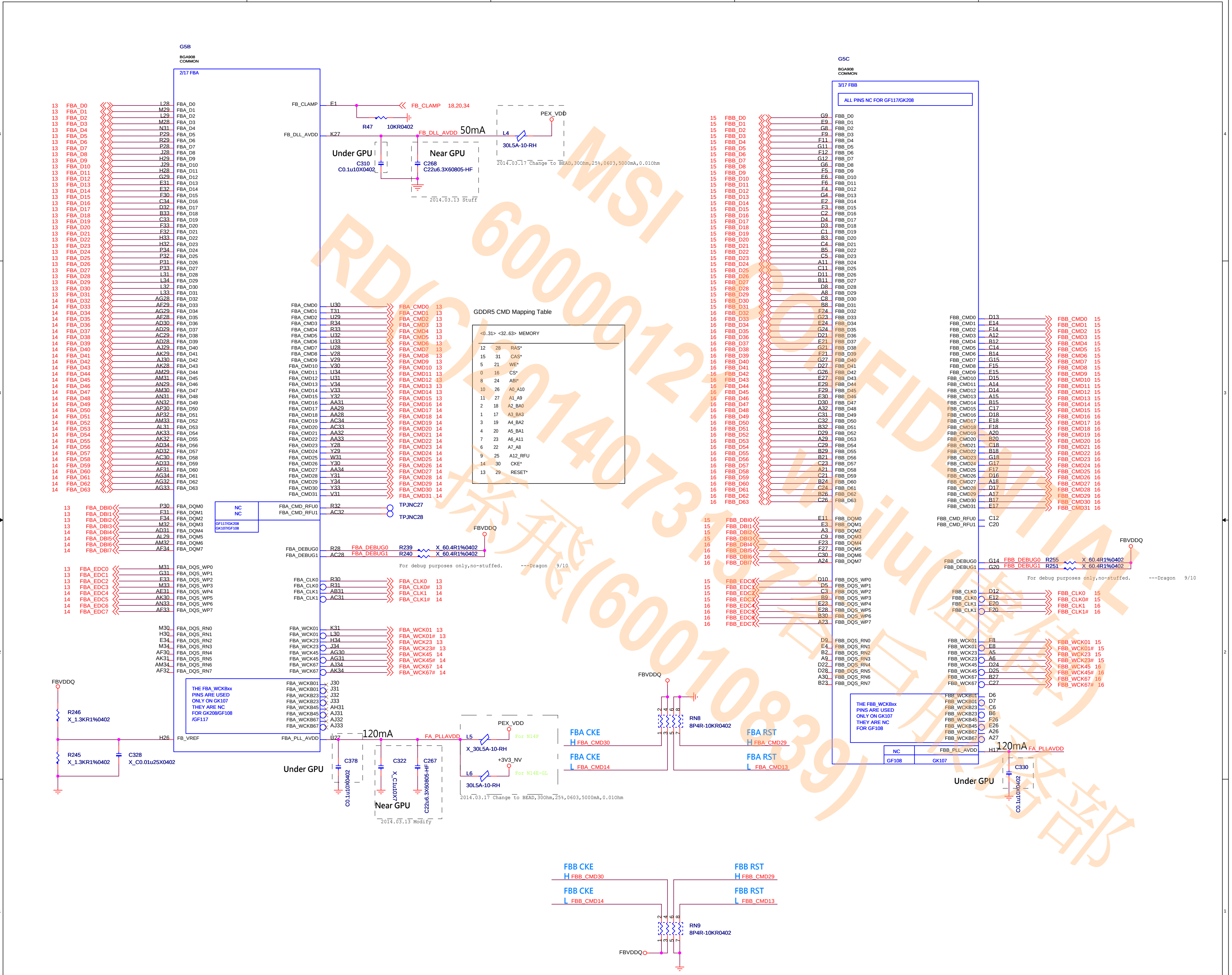
MICRO-STAR INT'L CO.,LTD.

Title	DDR3L SODIMM 1	
Size	Document Number: MS-16H3	Rev: 0B
Date: Tuesday, May 20, 2014	Sheet 10 of 69	



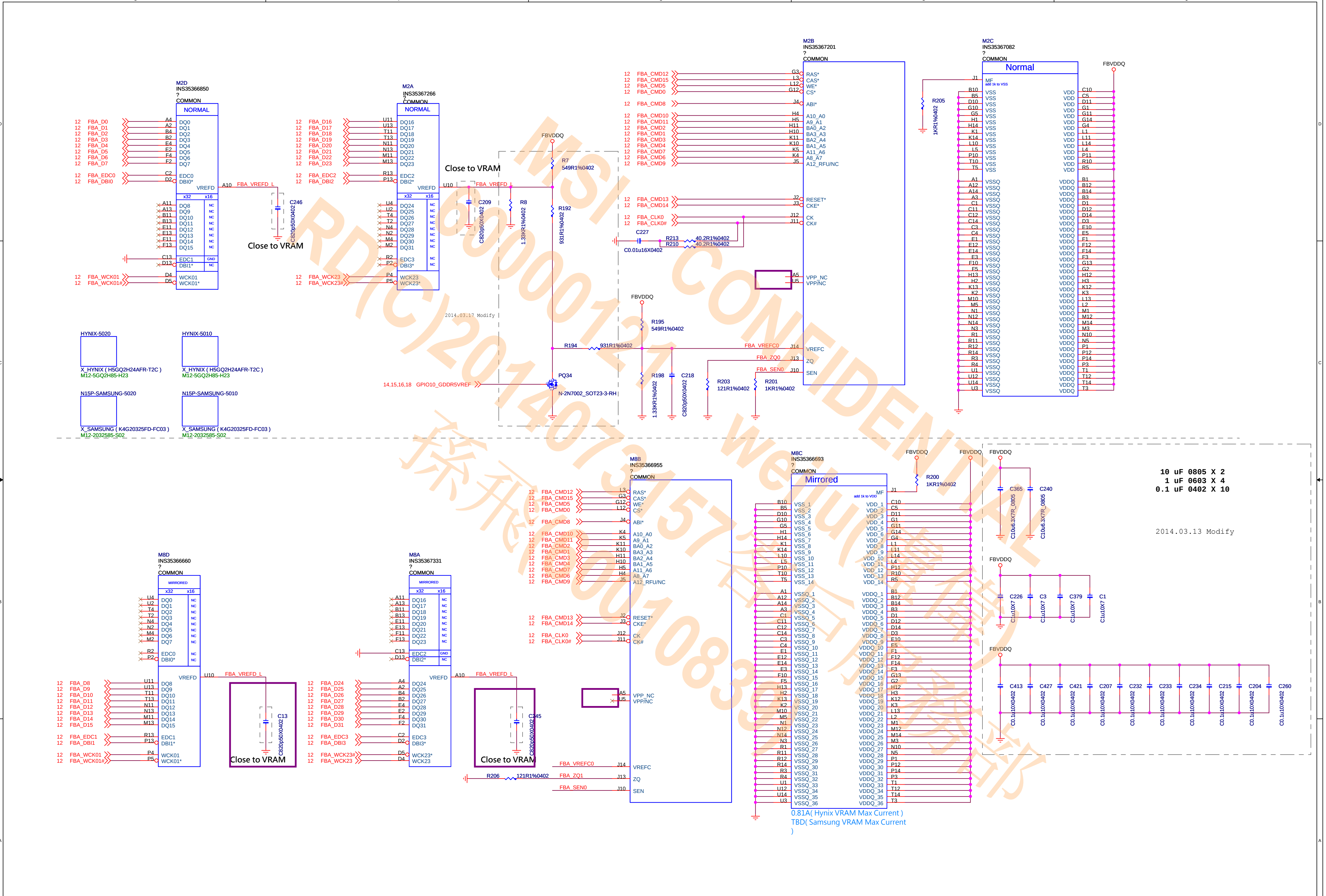
MICRO-STAR INT'L CO.,LTD.

Title	N15P-Q3_PCIE Host	
Size	Document Number MS-16H3	Rev 0B
Date: Tuesday, May 20, 2014	Sheet 11 of 69	



MICRO-STAR INT'L CO.,LTD.

Title	N15P-Q3_MEM Interface
Size / Document Number	MS-16H3
Rev	0B
Date:	Tuesday, May 20, 2014
Sheet	12 of 69

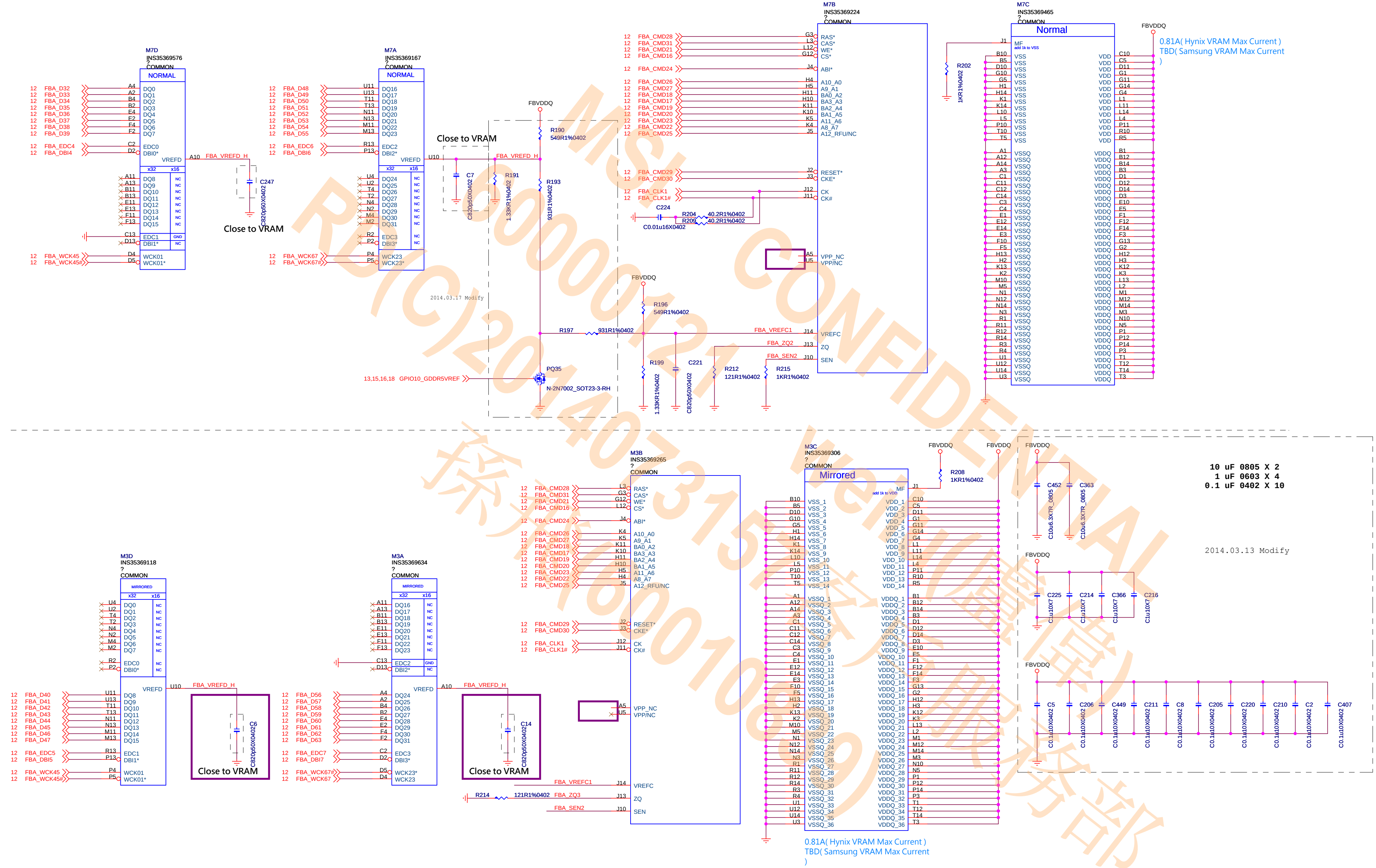


MICRO-STAR INT'L CO.,LTD.

Title: N15P-Q_FrameA GDDR5 I

Size | Document Number: MS-16H3 | Rev: 0B

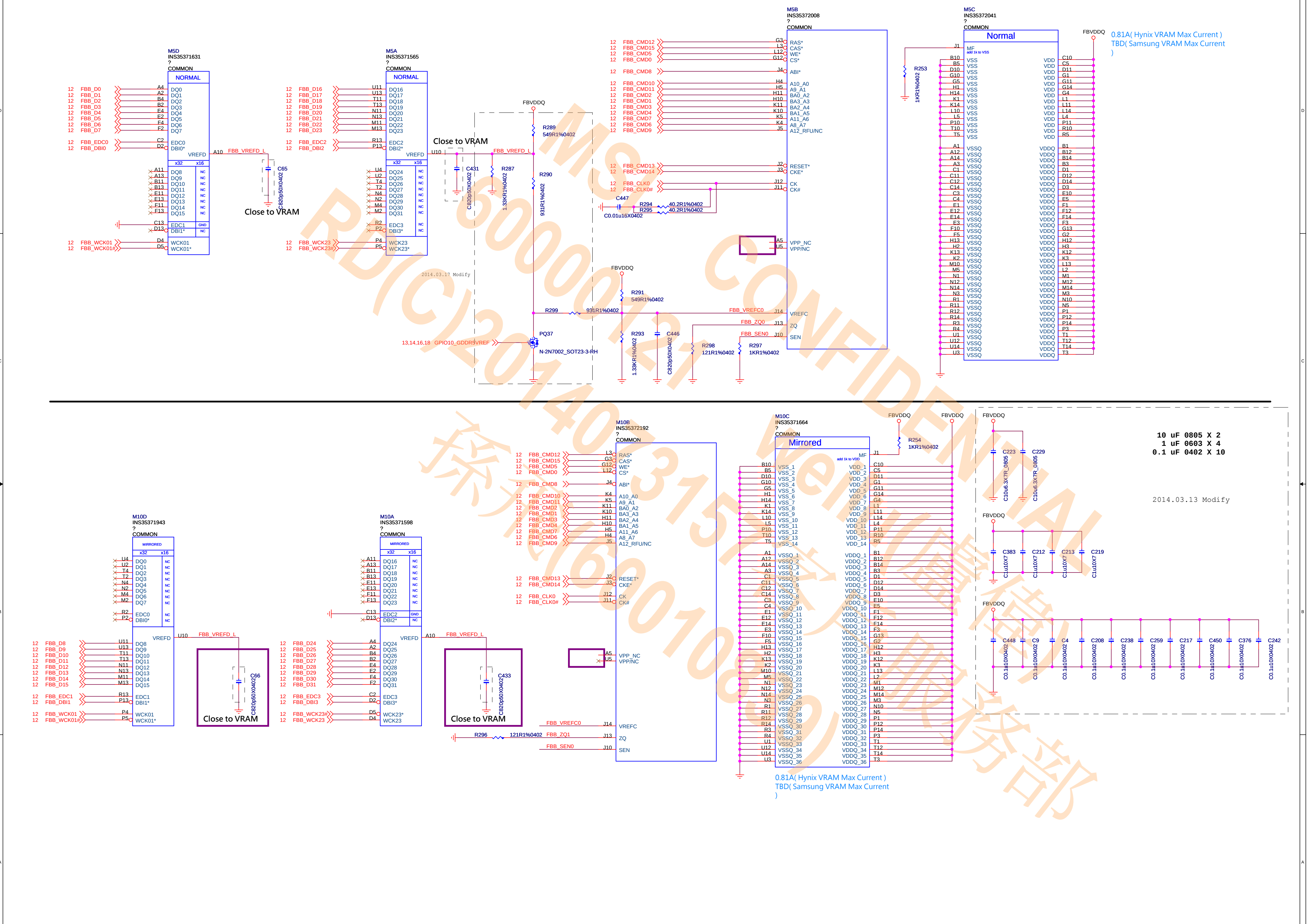
Date: Tuesday, May 20, 2014 | Sheet 13 of 69



MICRO-STAR INT'L CO.,LTD.

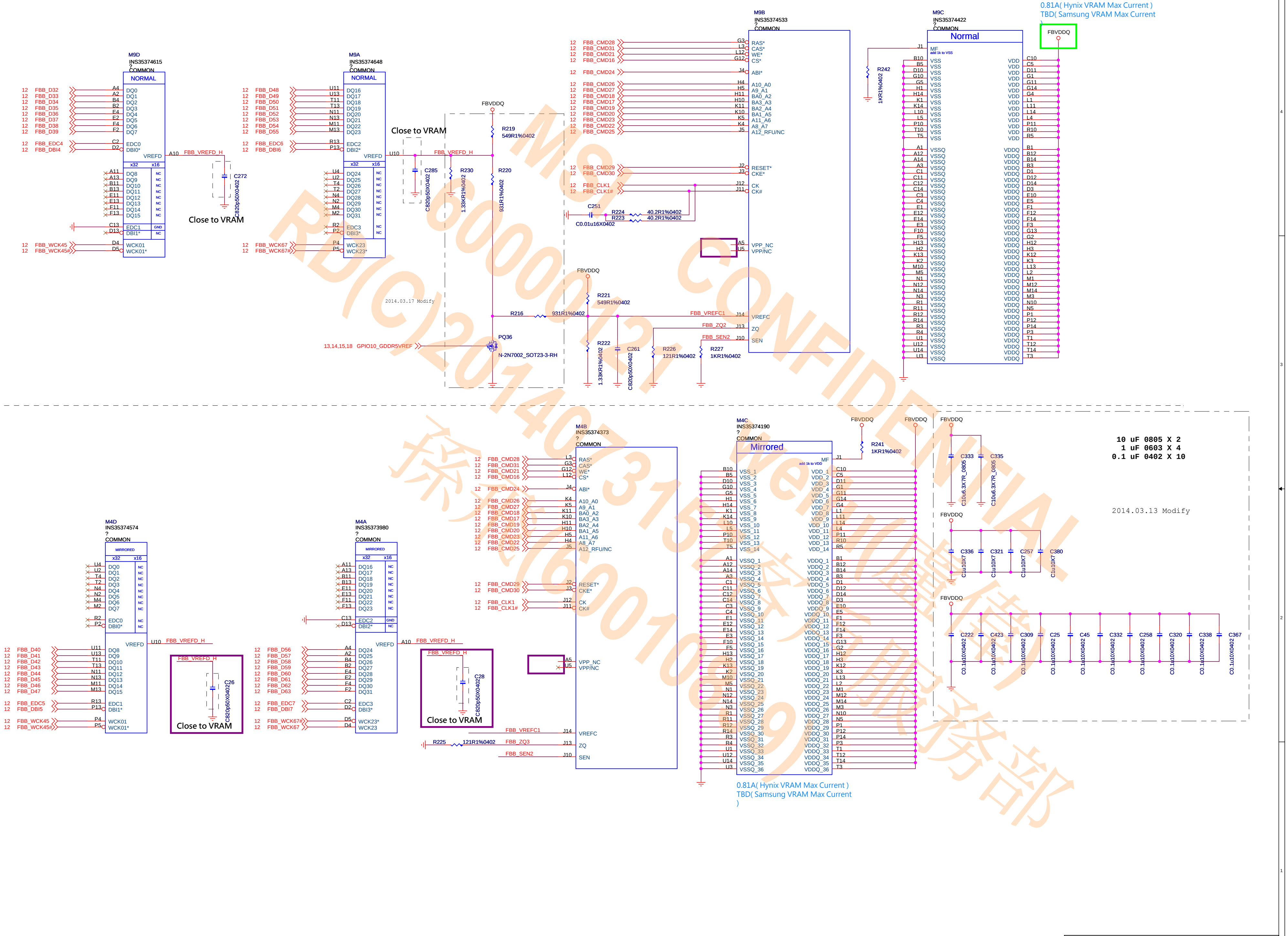
Title: N15P-Q3 FrameA GDDR5 II

Size | Document Number: MS-16H3 | Rev: 0B



MICRO-STAR INT'L CO.,LTD.

Title	N15P-Q3_FrameC GDDR5 I	
Size	Document Number MS-16H3	Rev 0B
Date: Tuesday, May 20, 2014	Sheet 15 of 69	

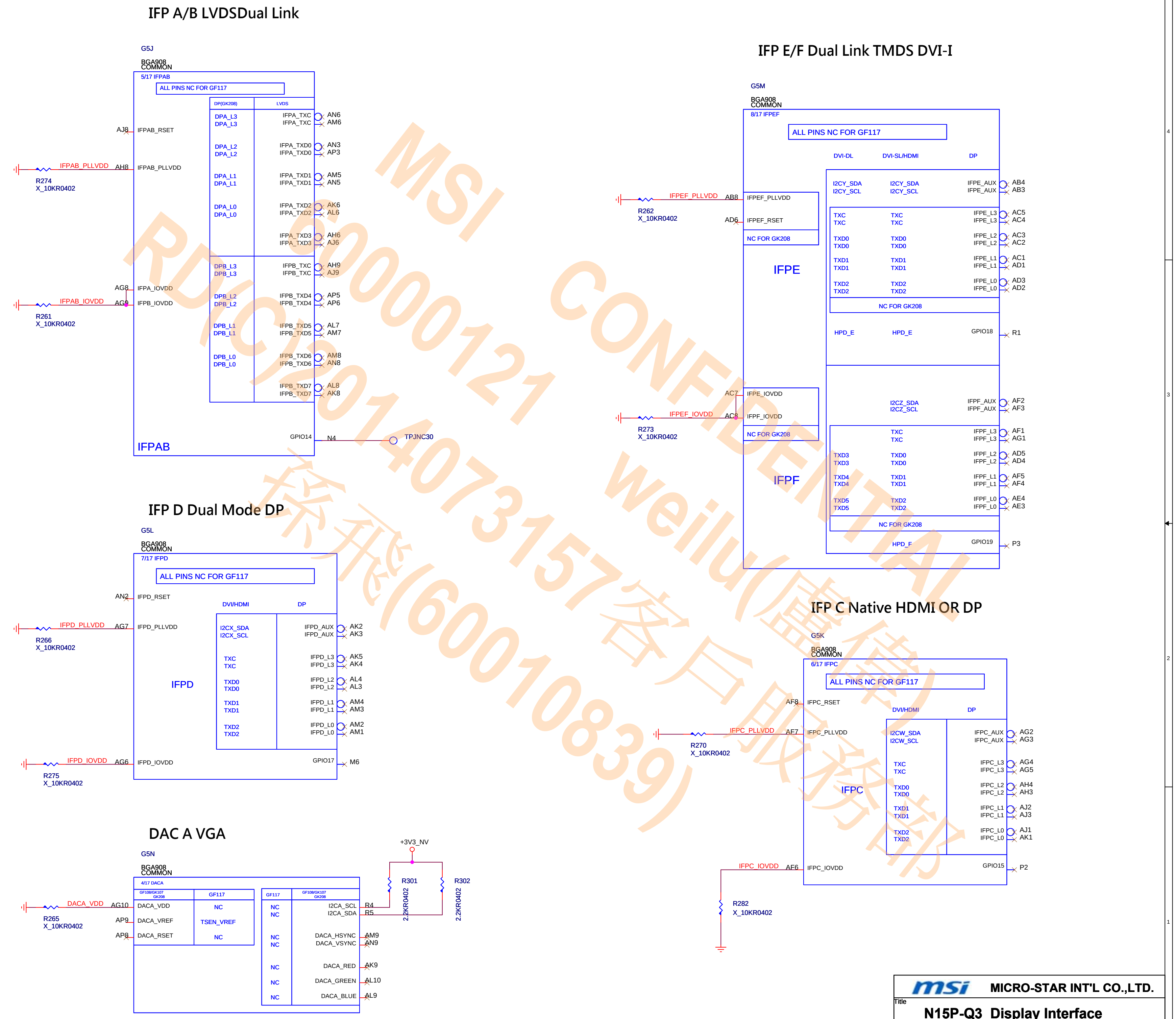


MICRO-STAR INT'L CO.,LTD.

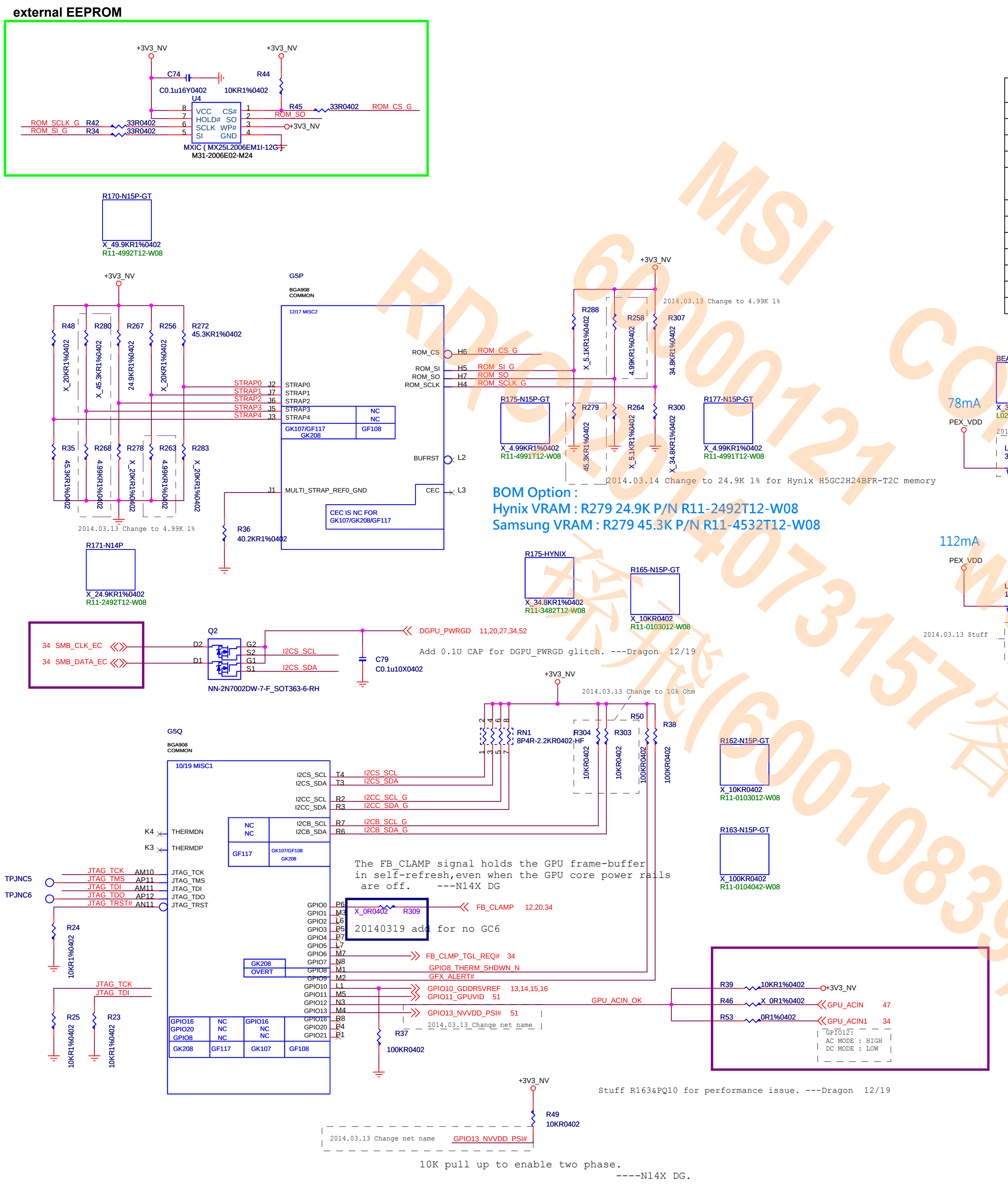
Title: N15P-Q3_FrameC GDDR5 II

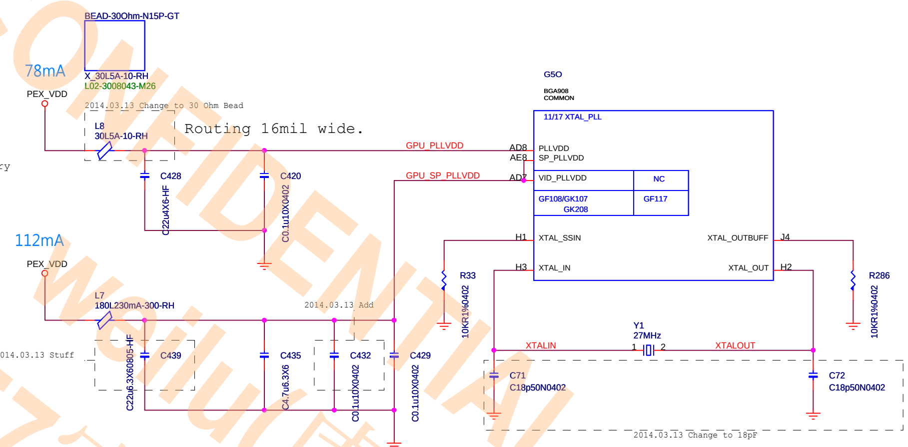
Size | Document Number: MS-16H3 | Rev: 0B

Date: Tuesday, May 20, 2014 | Sheet 16 of 69



MICRO-STAR INT'L CO.,LTD.	
Title	**N15P-Q3_Display Interface**
Size	Document Number **MS-16H3**	Rev 0B
Date: Tuesday, May 20, 2014	Sheet 17 of 69





Item	Location	N15P-Q3
Strap Mode	R3365	MULTISTRAP_REF_GND,40.2K PD to GND
Device ID		0x11FC
Package		GB4-128
Memory Type		GDDR5
ROM_SI	R3175	0x4, Hynix 2G, 24.9kohm PD
	R3175	0x7, Samsung 2G, 45kohm PD
ROM_SO	R3193	0x8, 5kohm pull up
ROM_SCLK	R3179	0x1110,35kohm PU(with ROM)
Strap0	R3170	45kohm pull up
Strap1	R3180	5kohm pull down
Strap2	R3171	DID,0x1100, 24.9kohm PU
Strap3	R3188	0x0 for Optimus, 5kohm pull down
Strap4	R3183	0x0111, 45kohm pull down

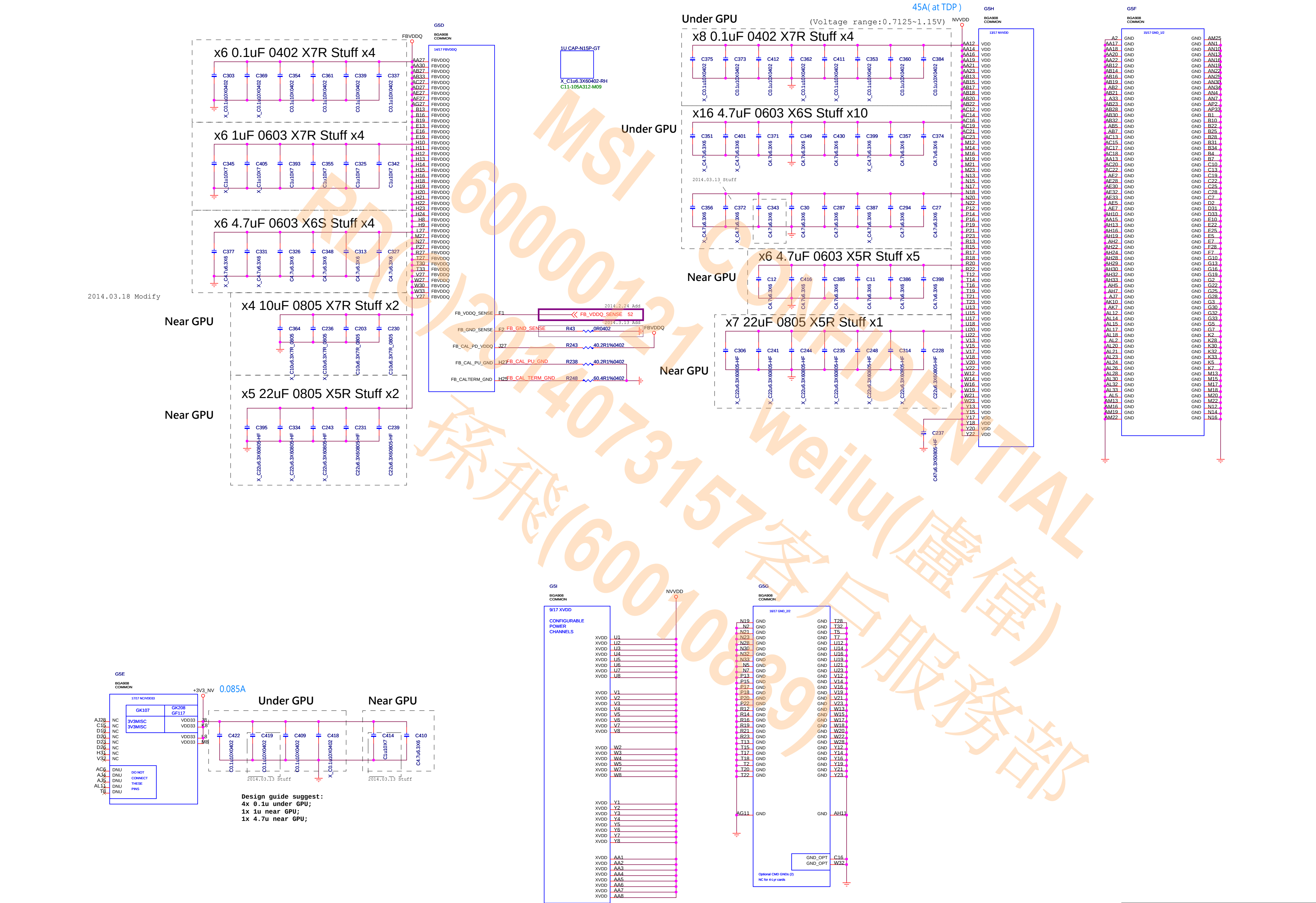
Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor	
GPIO1	NC	O		
GPIO2	NC	O		
GPIO3	NC	O		
GPIO4	NC	O		
GPIO5	NC	O		
GPIO6	FB_CLAMP_TGL_REQ	O	FB Clamp toggle request	
GPIO7	NC	O		
GPIO8	OVERT	I	Thermal Over Temperature	100K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect	100K pull-up
GPIO13	SPI	O	Phase Shedding	10K pull-up
GPIO14	NC	I		
GPIO15	NC	I		
GPIO16	NC	O		
GPIO17	NC	I		
GPIO18	NC	I		
GPIO19	NC	I		
NC	NC			

MICRO-STAR INT'L CO.,LTD.

Title: N15P-Q3_Thermal & GPIO

Document Number: MS-16H3 Rev: 0B

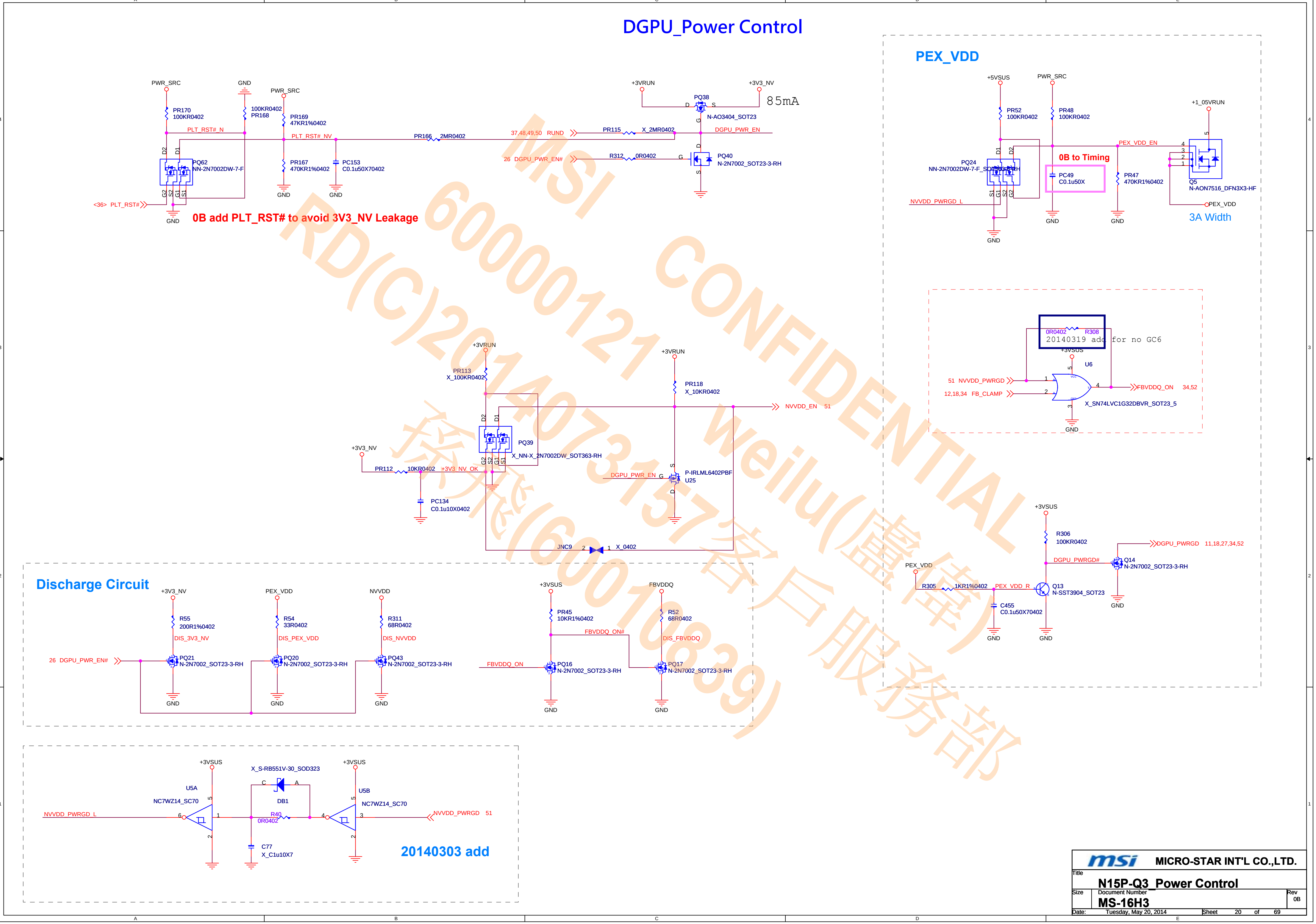
Date: Tuesday, May 20, 2014 Sheet 18 of 69



MICRO-STAR INT'L CO.,LTD.

Title	N15P-Q3_Power & GND
Size / Document Number	MS-16H3
Rev	0B
Date	Tuesday, May 20, 2014
Sheet	19 of 69

DGPU_Power Control



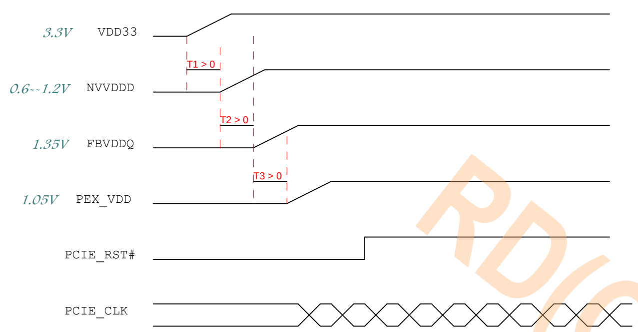
MICRO-STAR INT'L CO.,LTD.

Title: N15P-Q3_Power Control

Size | Document Number: MS-16H3 | Rev: 0B

Date: Tuesday, May 20, 2014 | Sheet 20 of 69

GPU POWER ON SEQUENCE

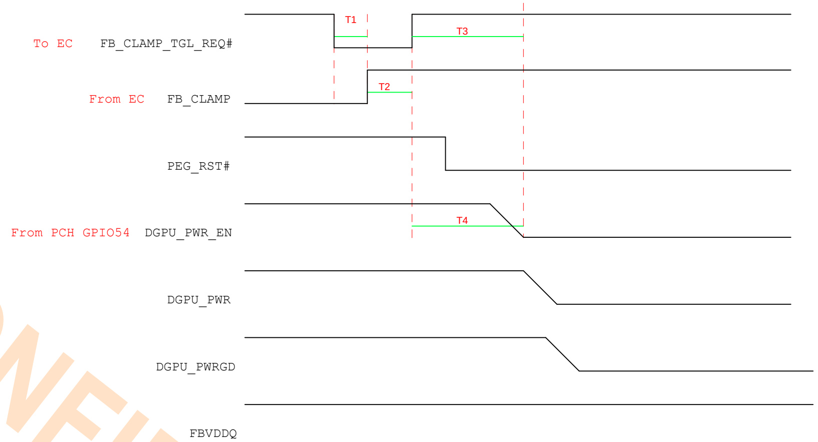


NOTES: The ramp time for any rail must be more than 40 us.
The total time for all rails to ramp up should be within 6ms.
A power rail has to ramp up to 90% before the next rail in sequence can start ramping up.
No signal should be applied to the GPU before the power rails are fully ramped

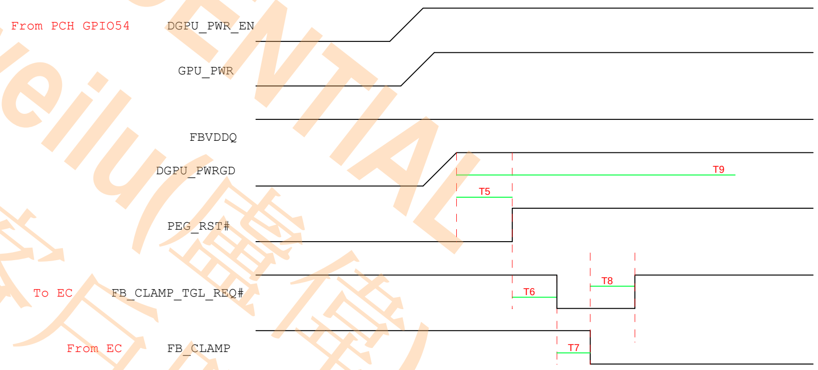
NOTES: For optimus system, VDD33 usually drops down earlier than NVVDD and FBVDDQ.

NOTES: All rails must be powered off within 10 ms from the first rail powering off.

GC6 ENTRY SEQUENCE(NOT support)



GC6 EXIT SEQUENCE



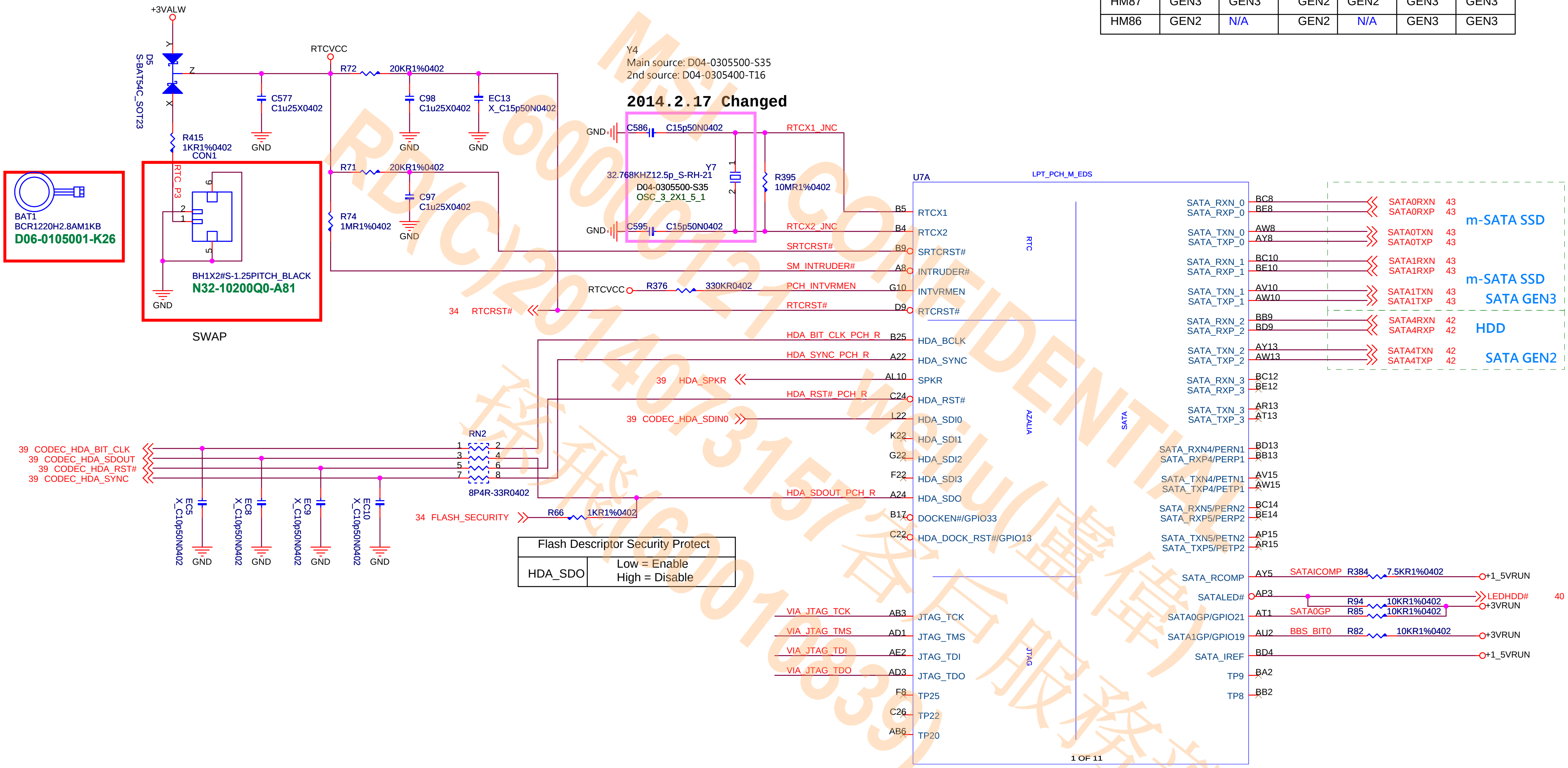
GC6 TIMING

	Min	Max	Unit	Description
T1	0	10	mS	GPU asserts toggle request to GB_CLAMP assertion
T2	0	1	mS	Assertion of FB_CLAMP to de-assertion of toggle request
T3	0	10	mS	De-assertion of toggle request to GPU PWR_EN=0
T4	0.01	1	mS	PEX reset assertion to GPU PWR_EN de-assertion
T5	0.1	5	mS	GPU power stable to de-assertion of PEX reset
T6	3.3		mS	De-assertion of PEX reset to toggle request assertion
T7	0	1	mS	Assertion of toggle request to de-assertion of FB_CLAMP
T8	0	1	mS	De-assertion of FB_CLAMP to de-assertion of toggle request
T9	TBD	TBD	mS	GPU power enable to GPU ready for normal operatioon

Notes: *System designers should minimize T1,T3,T4,T5,T6,and T7 to increase the time spent in GC6.
This increased GC6 residency will improve both power savings and user experience.
**If10 ms expirs for T1, the GPU will de-assert FB_CLAMP_TGL_REQ# and abort the GC6 entry procedure.
FB_CLAMP should never assert outside an FB_CLAMP_TGL_REQ# handshake.

Lynx Point (HDA/JTAG/SATA)

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3

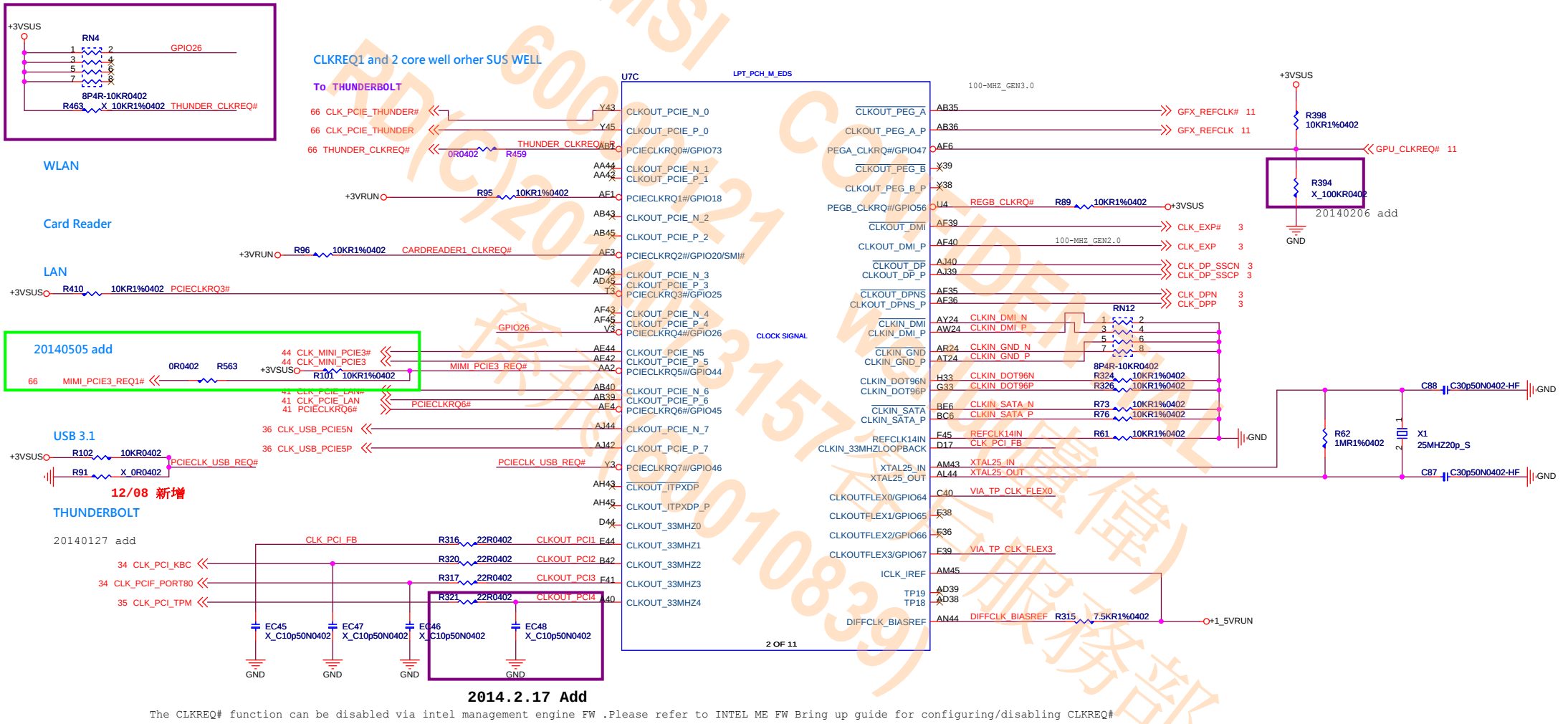


Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

SPK	The Signal has a weak internal pull-down Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)

Lynx Point (Clock)

PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 kΩ ±10% external pull-up resistor instead of No Connect.
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.

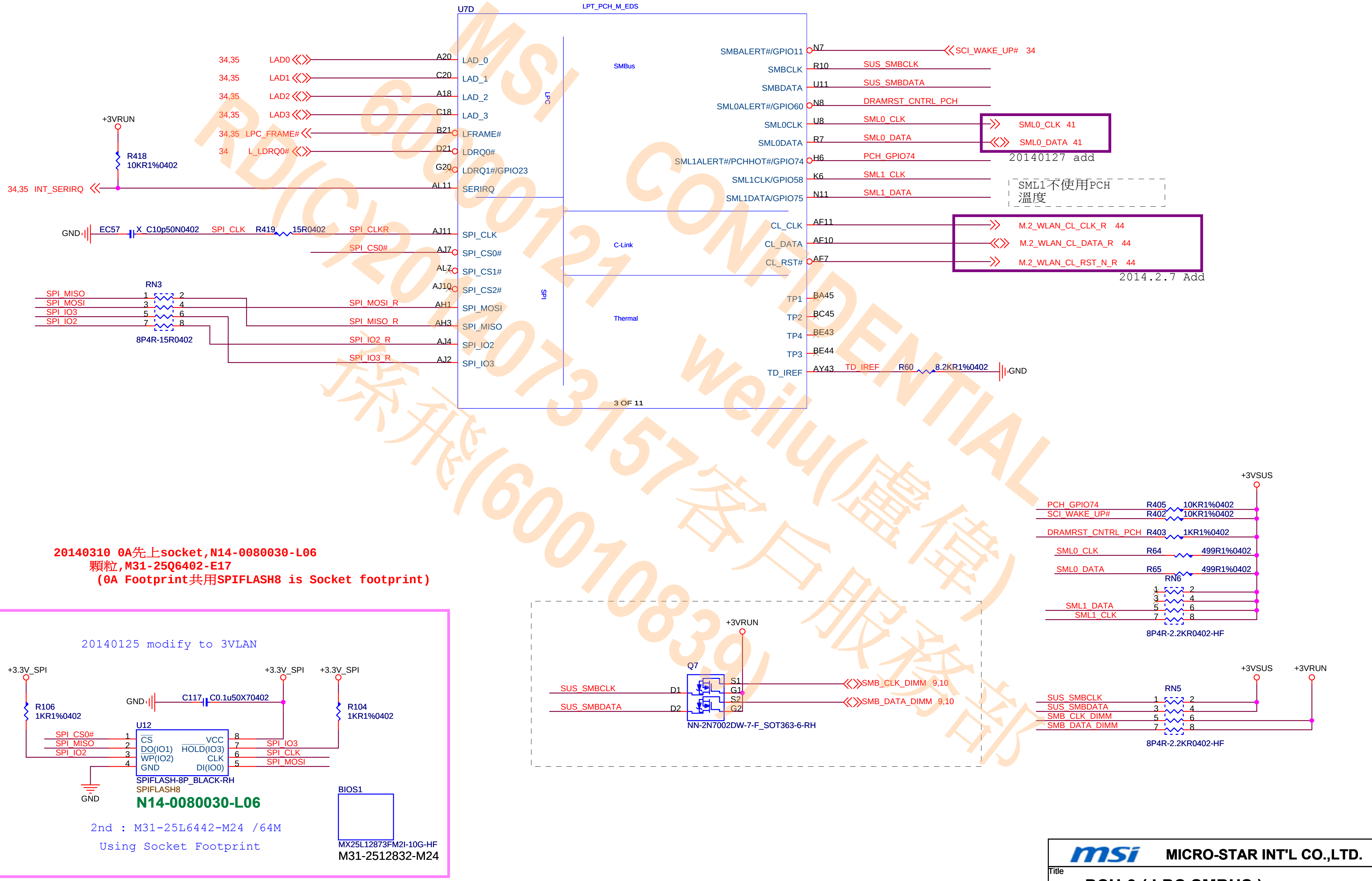


2014.2.17 Add

The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

MICRO-STAR INT'L CO.,LTD.		
Title: PCH-2 (CLK)		
Size	Document Number: MS-16H3	Rev: 0B
Date: Tuesday, May 20, 2014	Sheet 23 of 69	

Lynx Point (LPC,SMBUS)



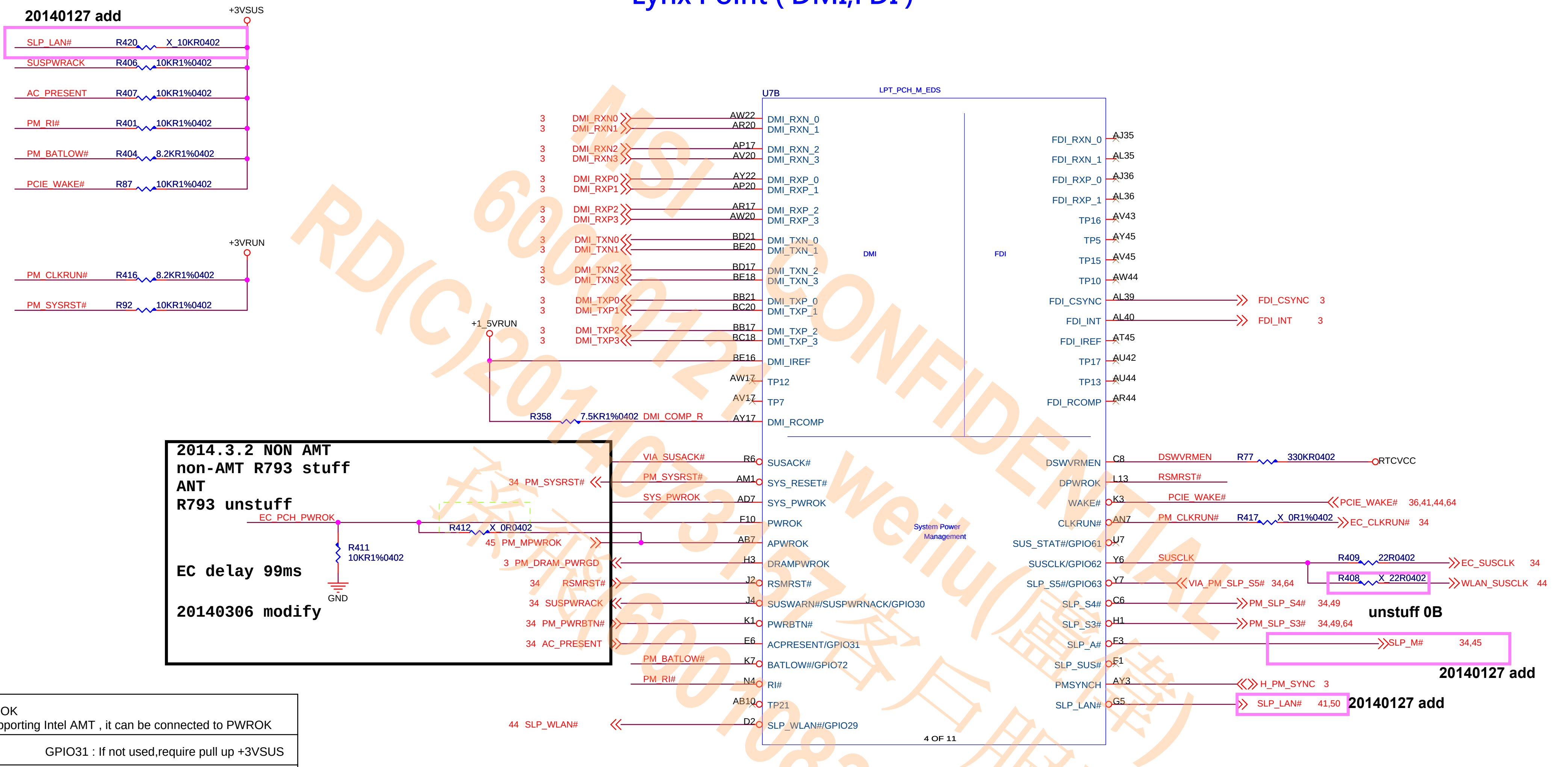
MICRO-STAR INT'L CO.,LTD.

Title: PCH-3 (LPC,SMBUS)

Size | Document Number: MS-16H3 | Rev: 0B

Date: Tuesday, May 20, 2014 | Sheet 24 of 69

Lynx Point (DMI,FDI)

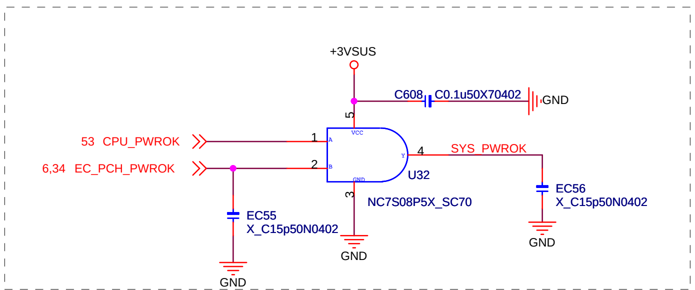


APWROK
not supporting Intel AMT , it can be connected to PWROK

GPIO31 : If not used,require pull up +3VSUS

DSWVRMEN - On Die DSW VR Enable
HIGH : Enable internal 1.05V regulator
LOW : Disable

DPWROK
Without deep s4/s5 support tied together with RSMRST#

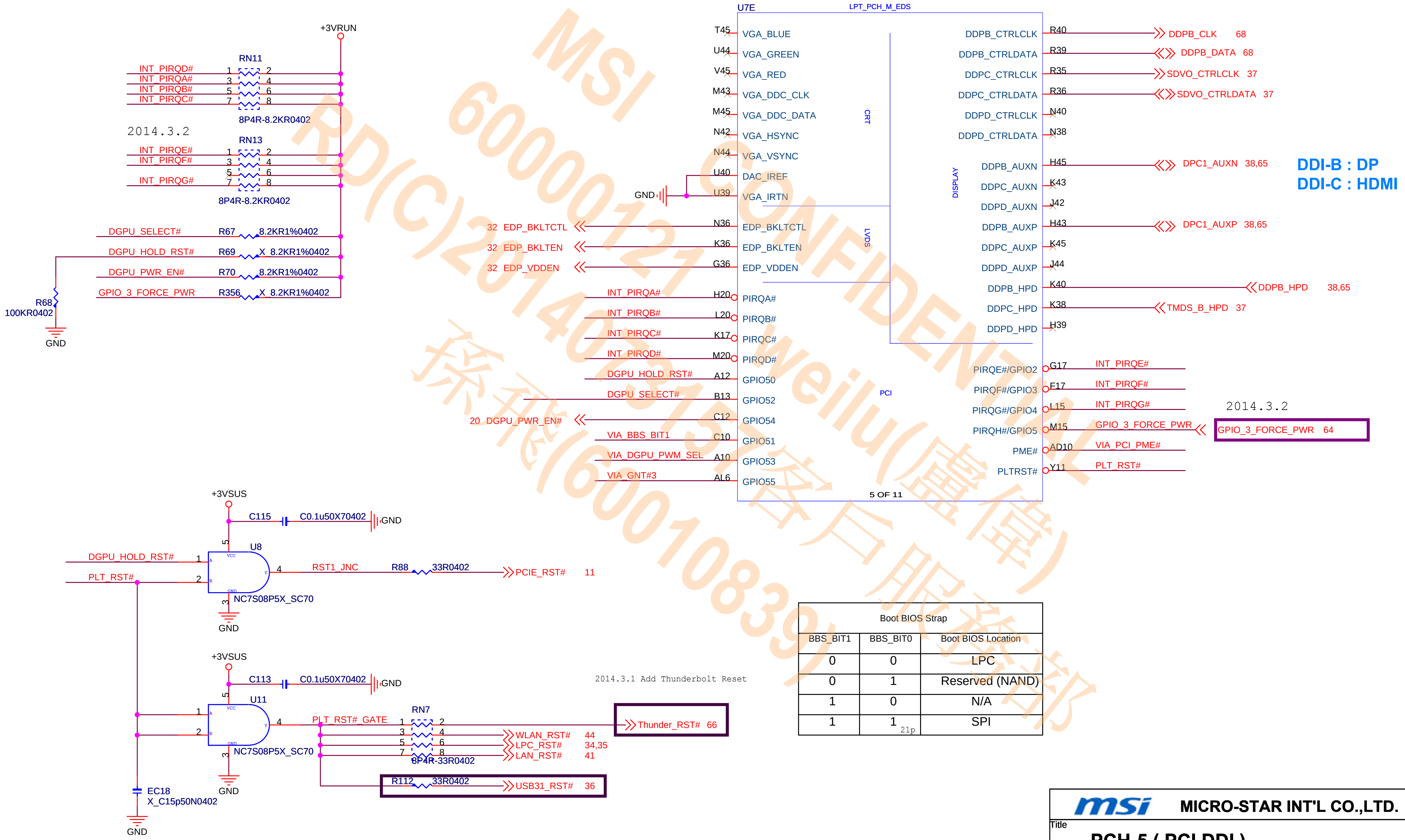


GPIO Setting : Ref 486708_LPT_EDS Section2.18

PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

MICRO-STAR INT'L CO.,LTD.
Title: PCH-4 (DMI,FDI)
Size | Document Number: MS-16H3 | Rev: 0B
Date: Tuesday, May 20, 2014 | Sheet 25 of 69

Lynx Point (PCI,DDI)



Boot BIOS Strap

BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

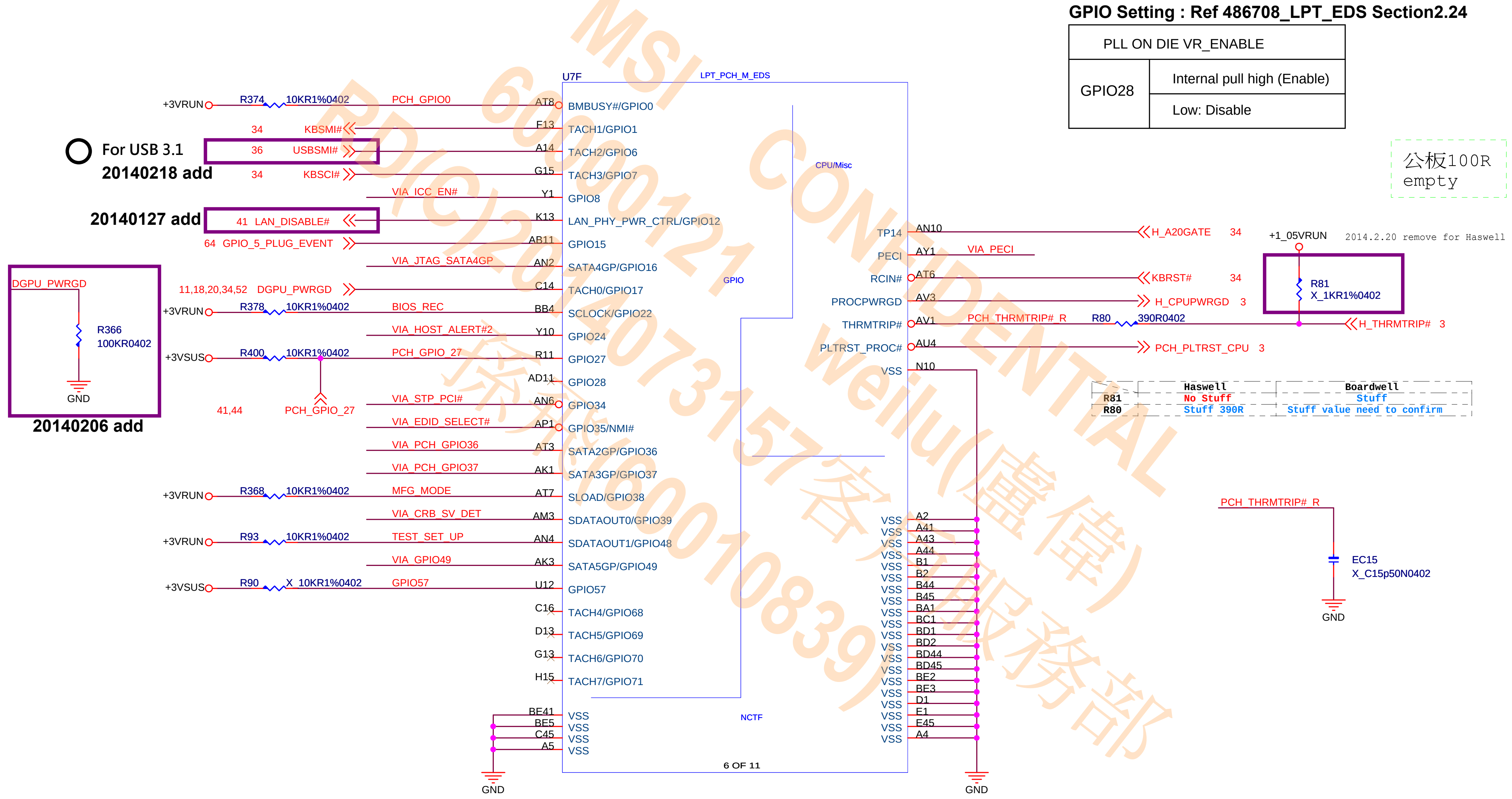
MICRO-STAR INT'L CO.,LTD.

Title: PCH-5 (PCI,DDI)

Size | Document Number: MS-16H3 | Rev: 0B

Date: Tuesday, May 20, 2014 | Sheet 26 of 69

Lynx Point (GPIO,MISC)



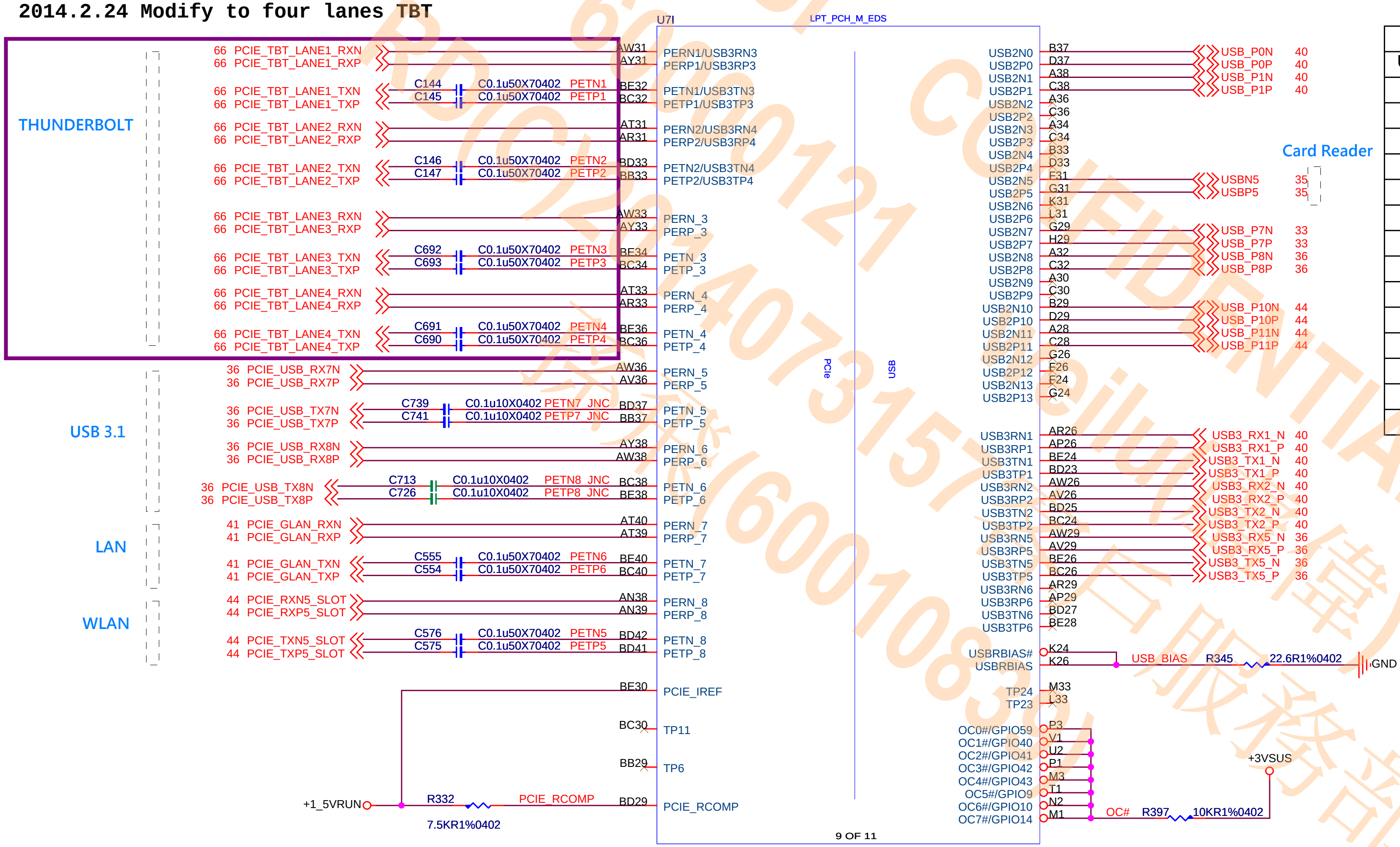
msi MICRO-STAR INT'L CO.,LTD.

Title	PCH-6 (GPIO,MISC)
Size	Document Number: MS-16H3
Rev	0B
Date:	Tuesday, May 20, 2014
Sheet	27 of 69

Lynx Point (PCIE,USB)

Intel Lynx Point ECHI USB(2.0) debug transport 需接Port1 or Port9

2014.2.24 Modify to four lanes TBT



USB			
USB 2.0	**USB 3.0**	**Device**	**Note**
0	1	USB 3.0 Port 1	**16H3A**
1	2	USB 3.0 Port 2	**16H3A**
2			
3			NC
4			NC
5			NC
6			NC
7		EPF021	3 色KBC
8	3	USB 3.0 Port 5	**16H31**
9	4	USB 3.0 Port 6	**no use**
10		WLAN	
11		WebCam	
12		SECOND DISPLAY	
13			NC

HM86 沒USB3.0 PORT 5,6

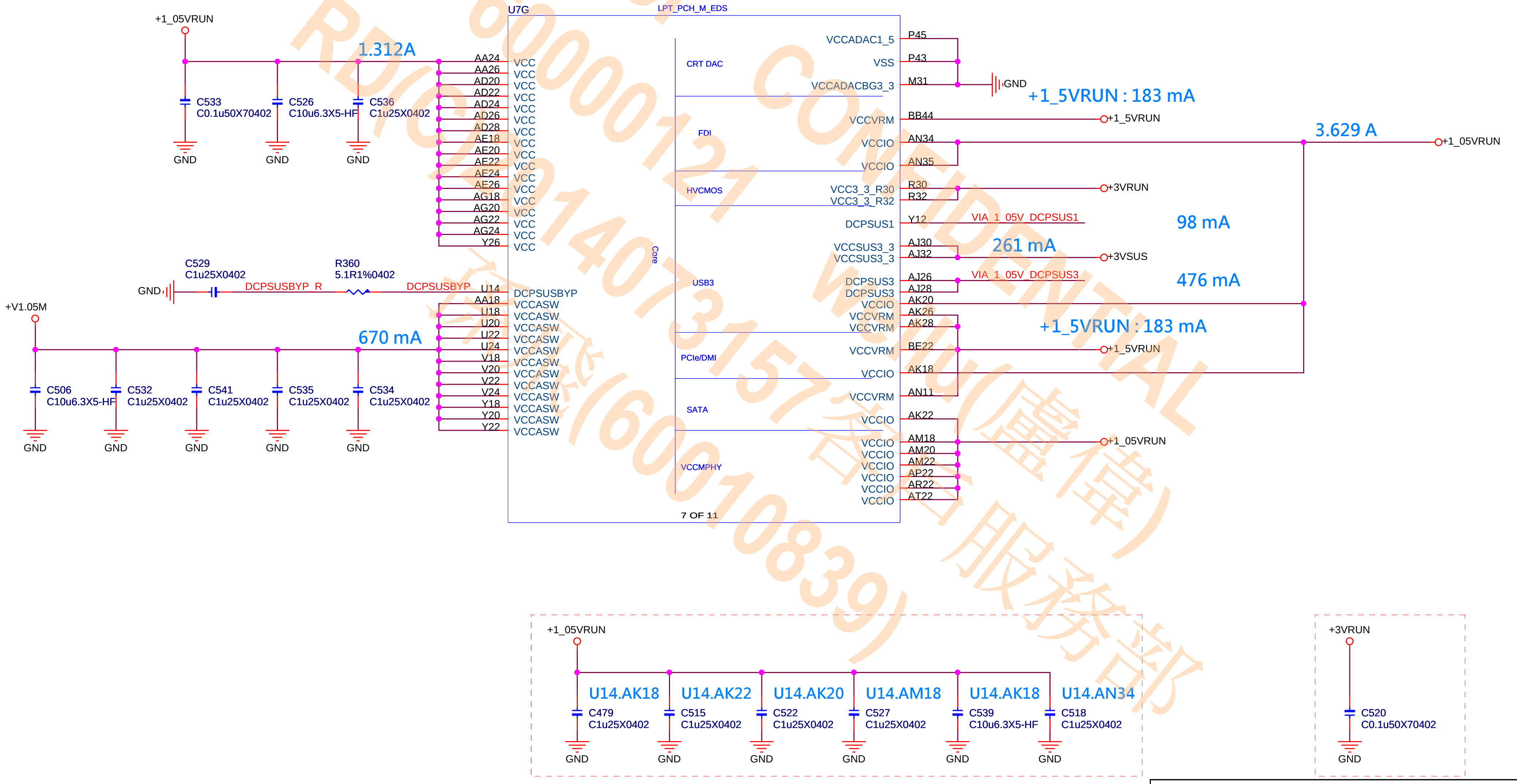
MICRO-STAR INT'L CO.,LTD.

Title: PCH-7 (PCIE,USB)

Size | Document Number: MS-16H3 | Rev: 0B

Date: Tuesday, May 20, 2014 | Sheet 28 of 69

Lynx Point (Power)



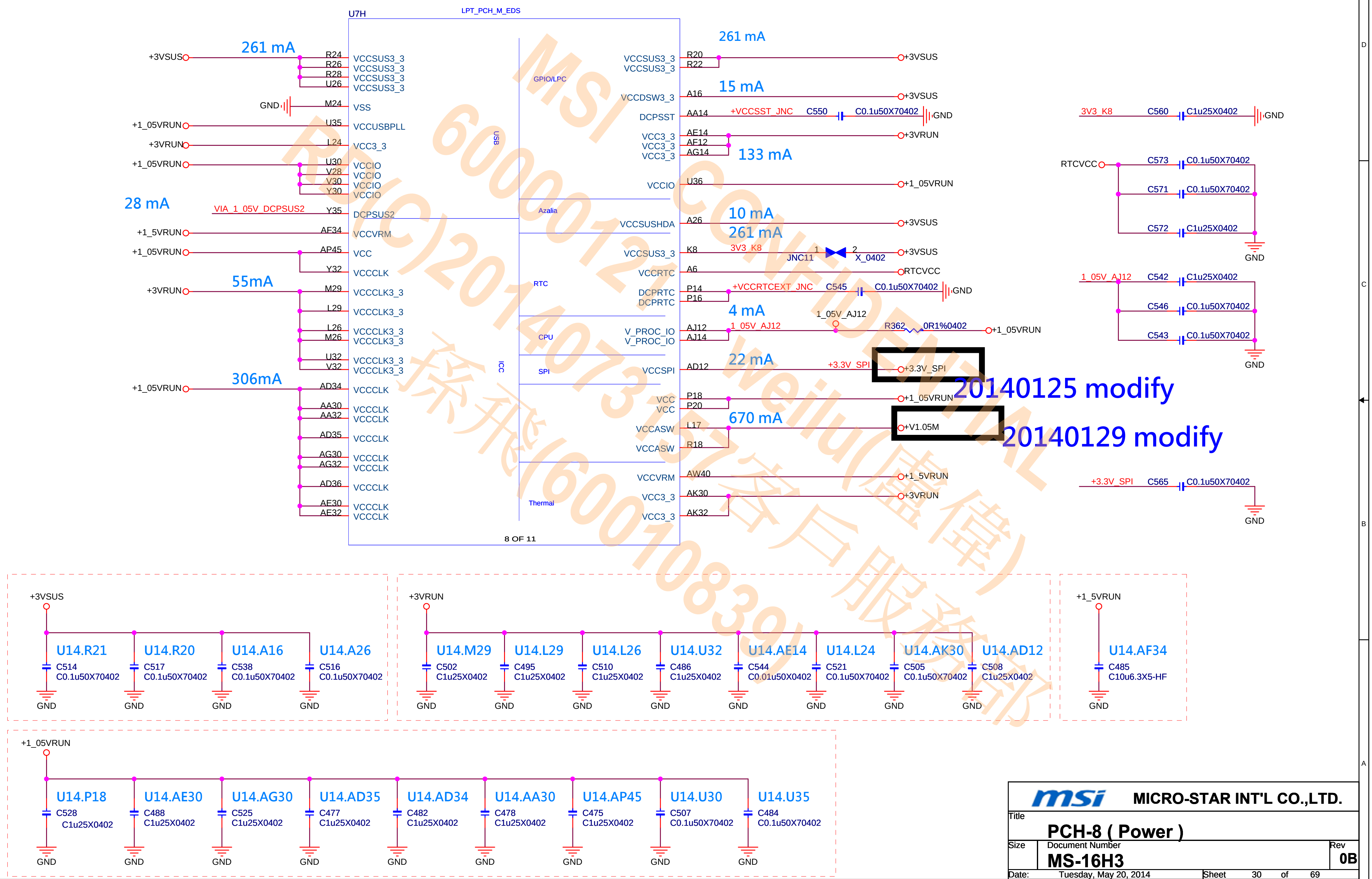
MICRO-STAR INT'L CO.,LTD.

Title: PCH-8 (Power)

Size | Document Number: MS-16H3 | Rev: 0B

Date: Tuesday, May 20, 2014 | Sheet 29 of 69

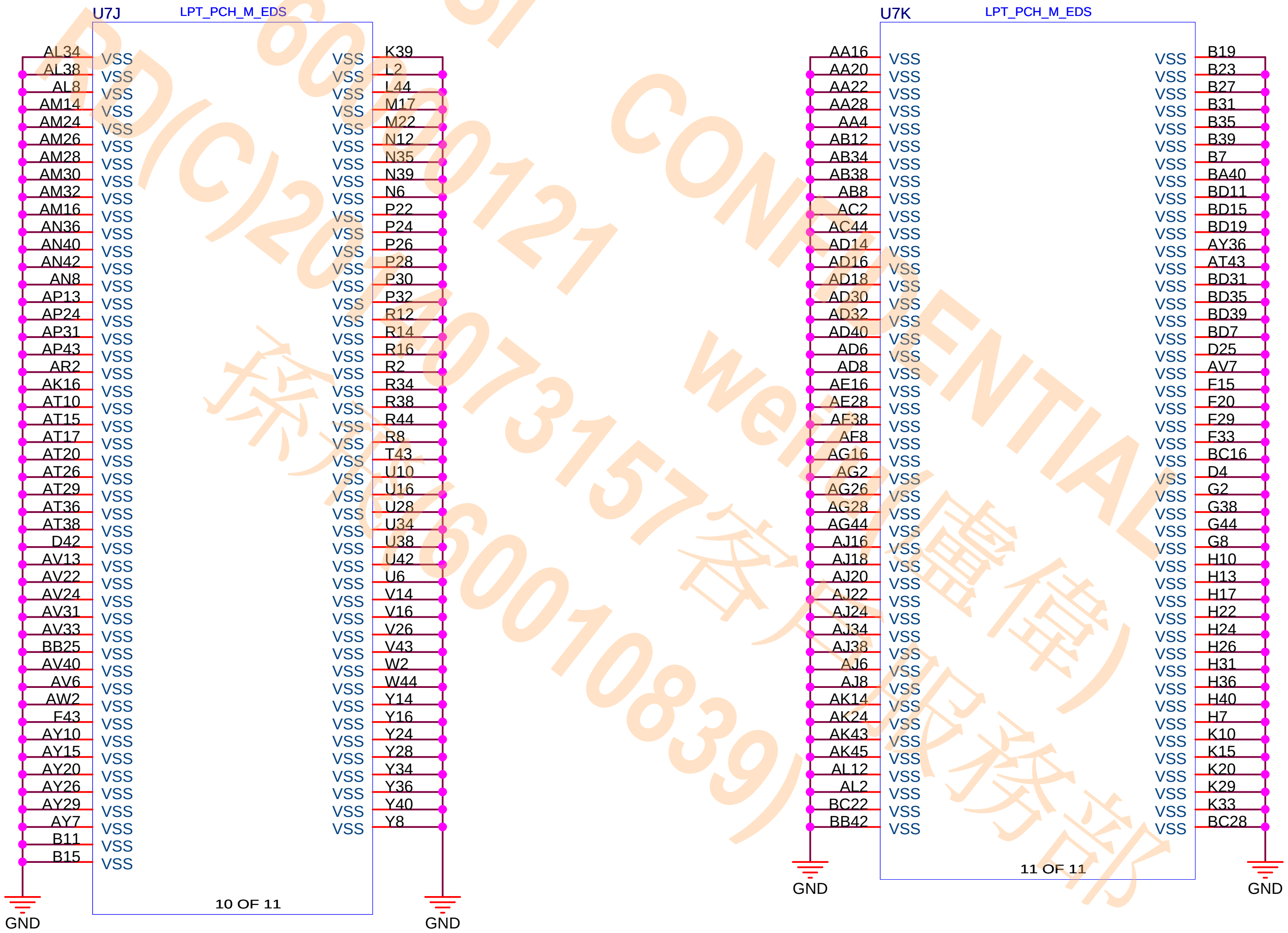
Lynx Point (Power)



MICRO-STAR INT'L CO.,LTD.

Title	PCH-8 (Power)	
Size	Document Number: MS-16H3	Rev: 0B
Date: Tuesday, May 20, 2014	Sheet 30 of 69	

Lynx Point (GND)



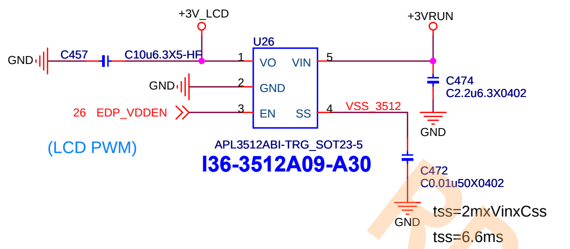
MICRO-STAR INT'L CO.,LTD.

Title: **PCH-8 (GND)**

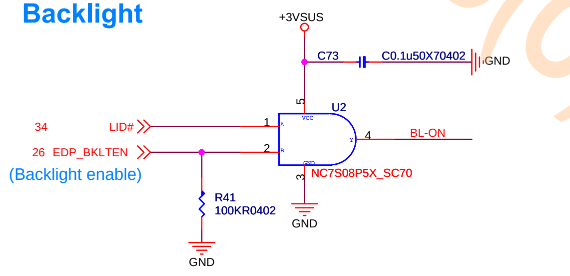
Size | Document Number: **MS-16H3** | Rev: **0B**

Date: Tuesday, May 20, 2014 | Sheet 31 of 69

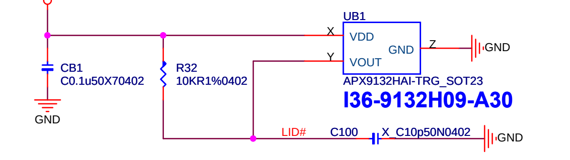
Pannel Device Logic Power



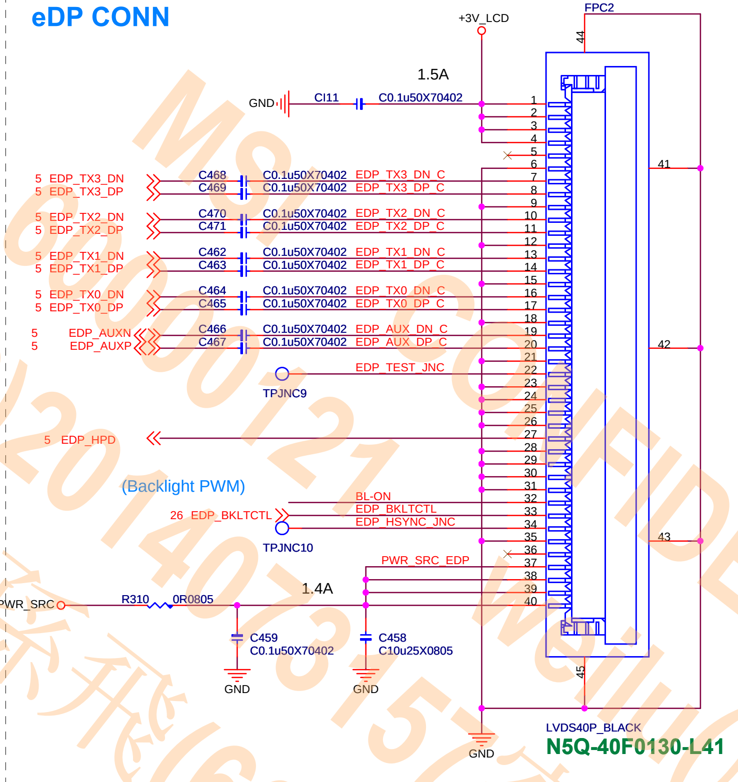
Backlight



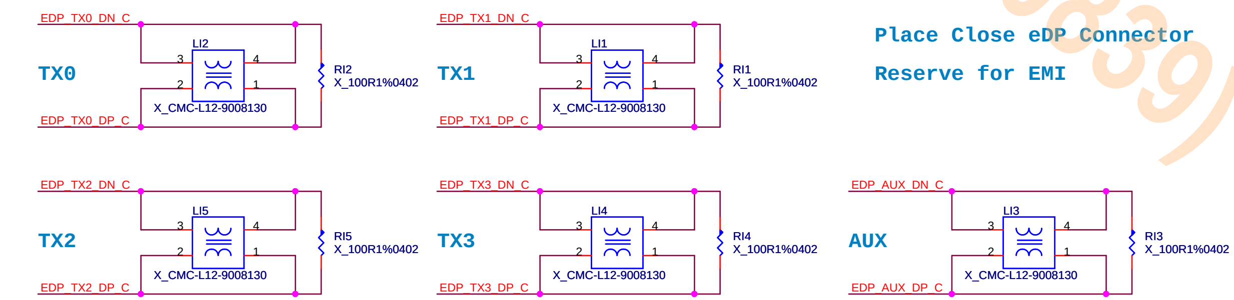
Hall Switch



eDP CONN



20140506 add for RF



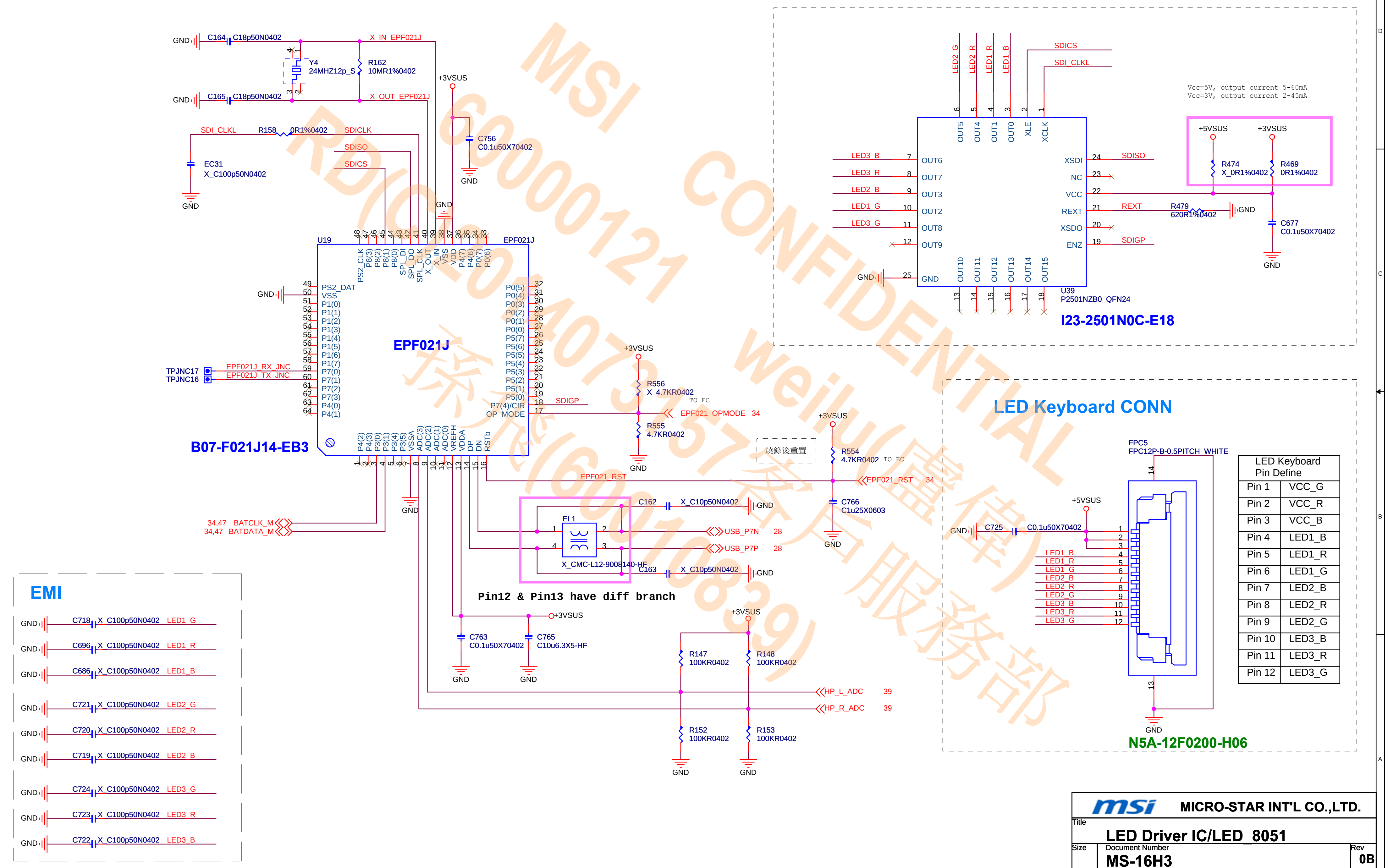
Place Close eDP Connector

Reserve for EMI

LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

LED 8051 Controller



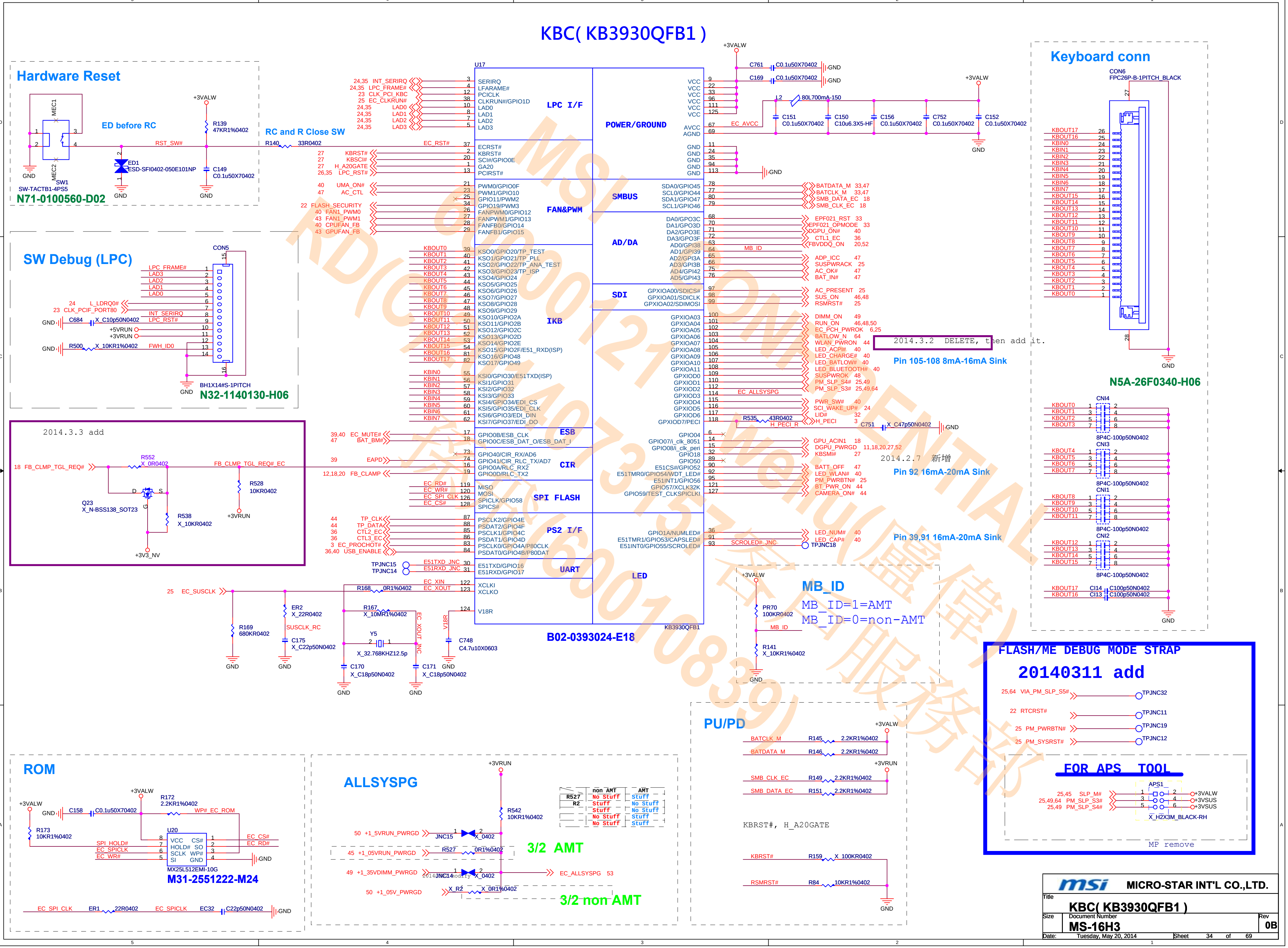
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

MICRO-STAR INT'L CO.,LTD.

Title: LED Driver IC/LED_8051

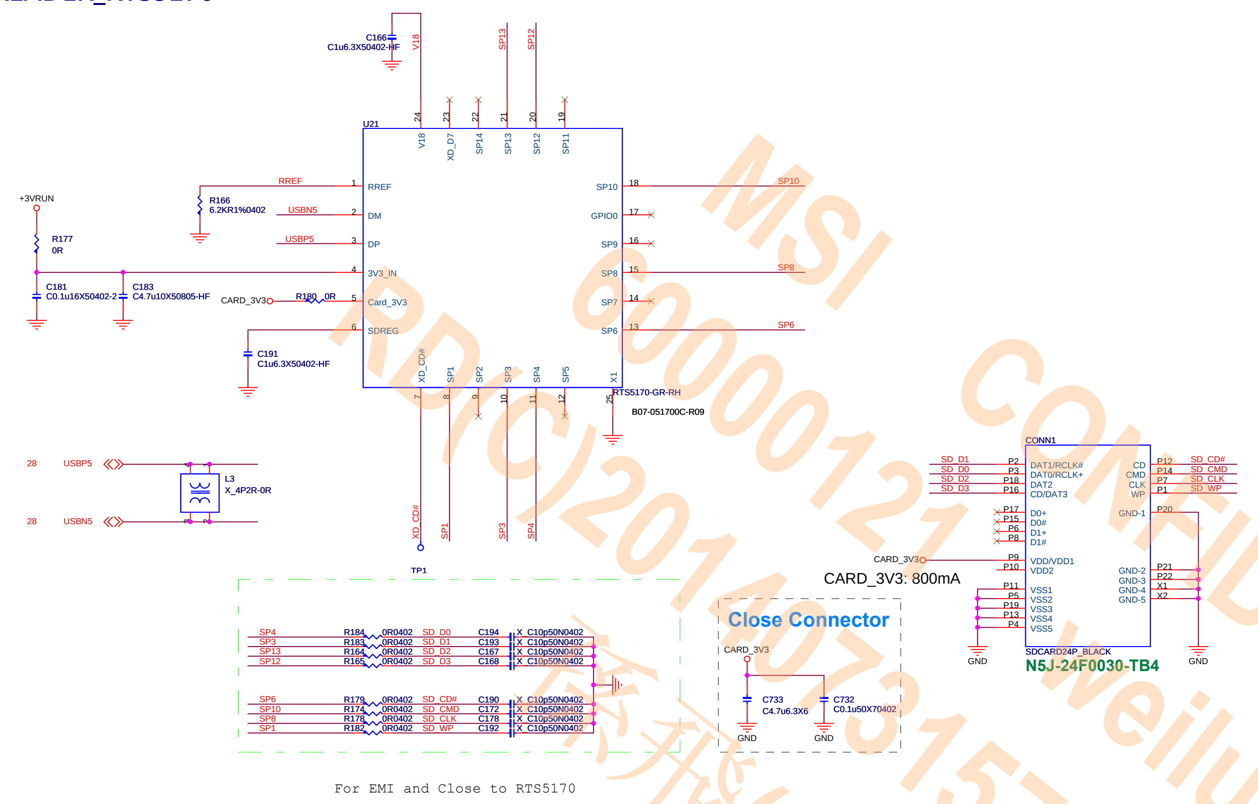
Size | Document Number: MS-16H3 | Rev: 0B

Date: Tuesday, May 20, 2014 | Sheet 33 of 69



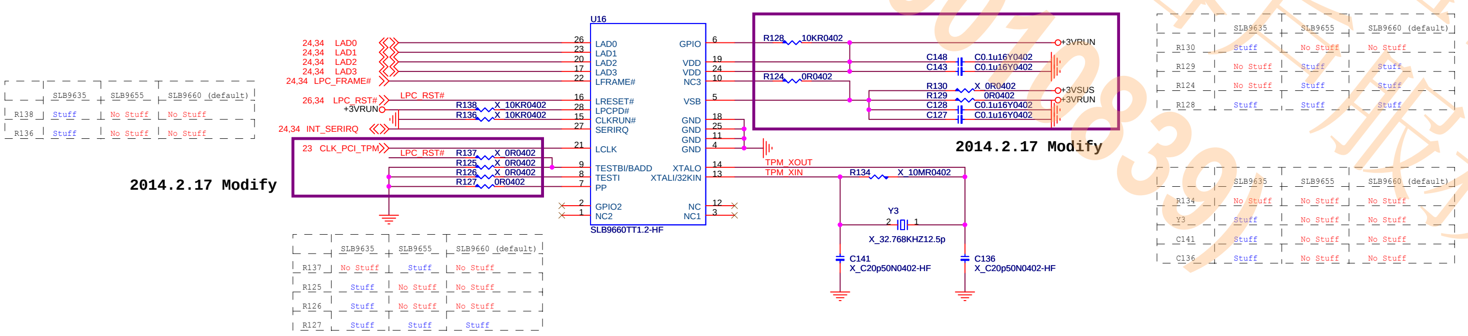
KBC(KB3930QFB1)
Hardware Reset
ED before RC
RC and R Close SW
SW-TACTB1-4PS5
N71-0100560-D02
SW Debug (LPC)
BH1X14#S-1PITCH
N32-1140130-H06
2014.3.3 add
U17
LPC I/F
POWER/GROUND
SMBUS
FAN&PWM
AD/DA
SDI
IKB
ESB
CIR
SPI FLASH
PS2 I/F
UART
LED
B02-0393024-E18
KB3930QFB1
2014.3.2 DELETE, then add it.
Pin 105-108 8mA-16mA Sink
2014.2.7 新增
Pin 92 16mA-20mA Sink
Pin 39,91 16mA-20mA Sink
Keyboard conn
FPC26P-B-1PITCH_BLACK
N5A-26F0340-H06
MB_ID
MB_ID=1=AMT
MB_ID=0=non-AMT
FLASH/ME DEBUG MODE STRAP
20140311 add
FOR APS TOOL
X_H2X3M_BLACK-RH
MP remove
PU/PD
KBRST#, H_A20GATE
ROM
MX25L512EMI-10G
M31-2551222-M24
ALLSYSPG
3/2 AMT
3/2 non AMT
MICRO-STAR INT'L CO.,LTD.
Title
KBC(KB3930QFB1)
Size
Document Number
MS-16H3
Rev
0B
Date: Tuesday, May 20, 2014
Sheet 34 of 69

CARD READER_RTS5170



Pin#	Name	I/O Type	Description
1	RREF	I	Connect external resistor (6.2K ± 1%) to reference ground
2	DM	I/O	USB D- signal
3	DP	I/O	USB D+ signal
4	3V3_IN	I	3.3V power input
5	CARD_3V3	O	3.3V power for all cards
6	SDREG	O	Internal regulator for SD card. An external capacitor should be connected
7	XD_CD#	I	xD Card Detect (xD_CD#)
8	SP1	I/O	xD Ready Signal (xD_RDY), SD Write Protect (SD WP) and MS Clock (MS_CLK)
9	SP2	I/O	xD RE# and MS Card Detect (MS_INS#)
10	SP3	I/O	xD CE# and SD Data 1 (SD_DAT1)
11	SP4	I/O	xD_CLE, SD Data 0 (SD_DAT0) and MS Data 7 (MS_D7)
12	SP5	I/O	xD ALE, SD Data 7 (SD_DAT7) and MS Data 3 (MS_D3)
13	SP6	I/O	xD_WE# and SD Card Detect (SD_CD#)
14	SP7	I/O	xD Write Protect (xD_WP), SD_Data 6 (SD_DAT6) and MS Data 6 (MS_D6)
15	SP8	I/O	xD Data 0 (xD_D0), SD Clock (SD_CLK) and MS Data 2 (MS_D2)
16	SP9	I/O	xD Data 1 (xD_D1), SD Data 5 (SD_D5) and MS Data 0 (MS_D0)
17	GPIO0	I/O	General purpose input/output with interrupt ability
18	SP10	I/O	xD Data 2 (xD_D2) and SD command signal (SD_CMD)
19	SP11	I/O	xD Data 3 (xD_D3), SD Data 4 (SD_DAT4) and MS Data 4 (MS_D4)
20	SP12	I/O	xD Data 4 (xD_D4), SD Data 3 (SD_DAT3) and MS Data 1 (MS_D1)
21	SP13	I/O	xD Data 5 (xD_D5), SD Data 2 (SD_DAT2) and MS Data 5 (MS_D5)
22	SP14	I/O	xD Data 6 (xD_D6) and MS BS
23	XD_D7	I/O	xD Data 7 (xD_D7)
24	V18	O	Regulated supply voltage (1.8V ±10%) from internal 3.3V to 1.8V regulator; supplies internal digital circuits. An external capacitance should be connected

TPM

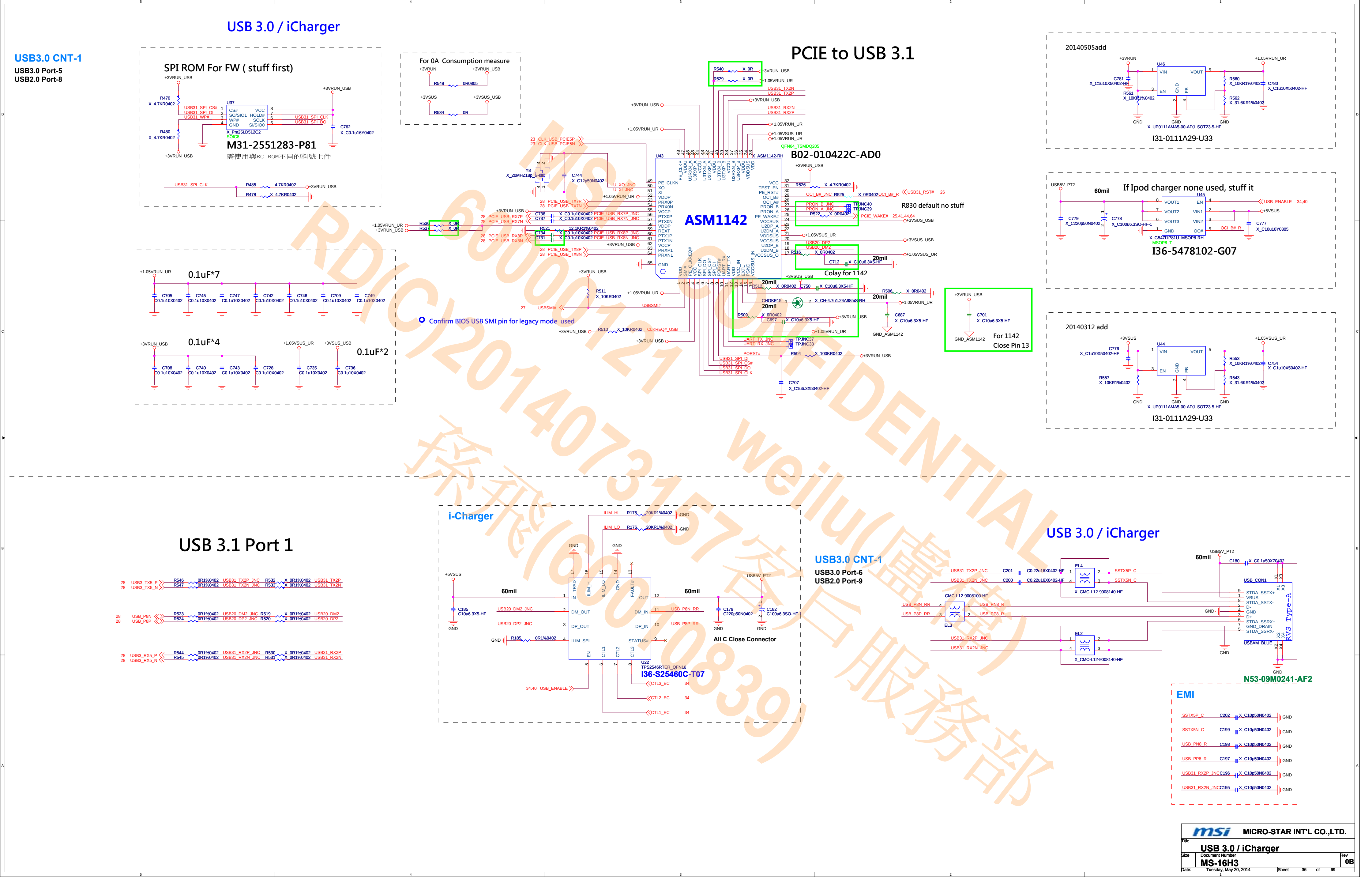


MICRO-STAR INT'L CO.,LTD.

Title: Card Reader & TPM

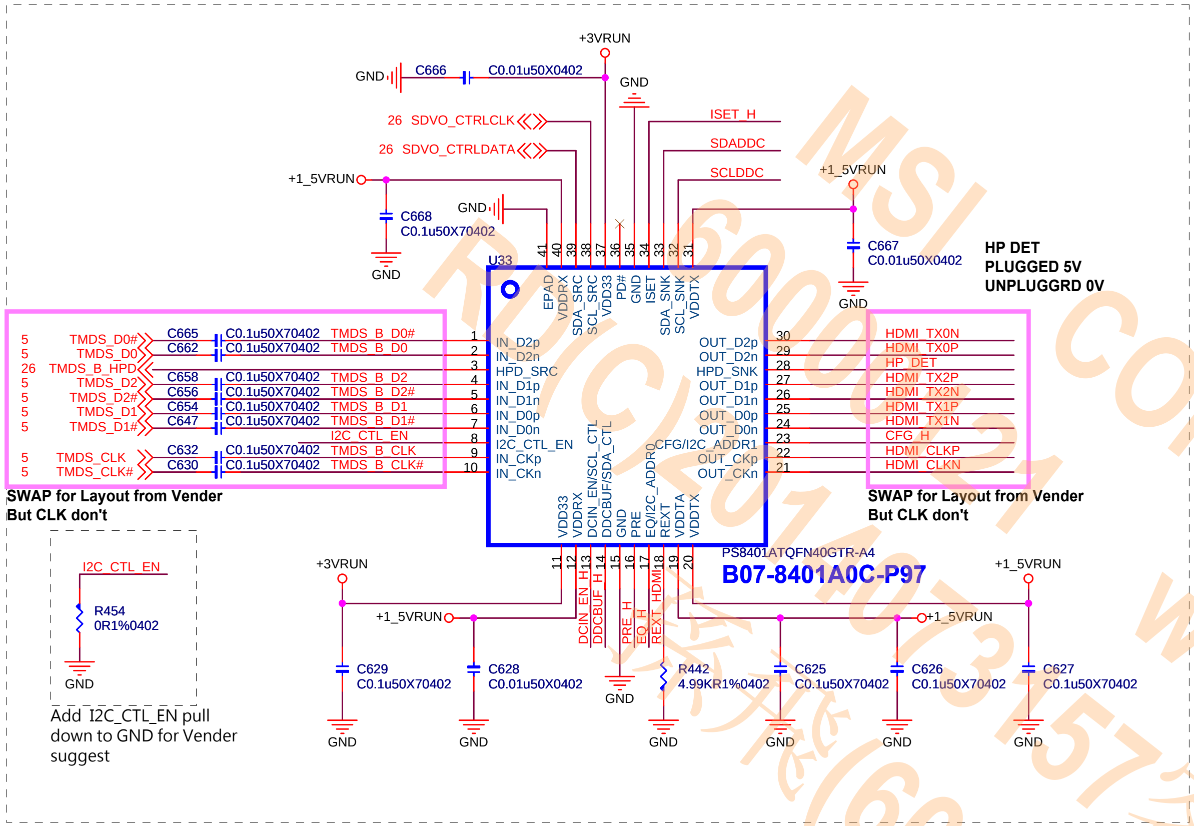
Size | Document Number: MS-16H3 | Rev: 0B

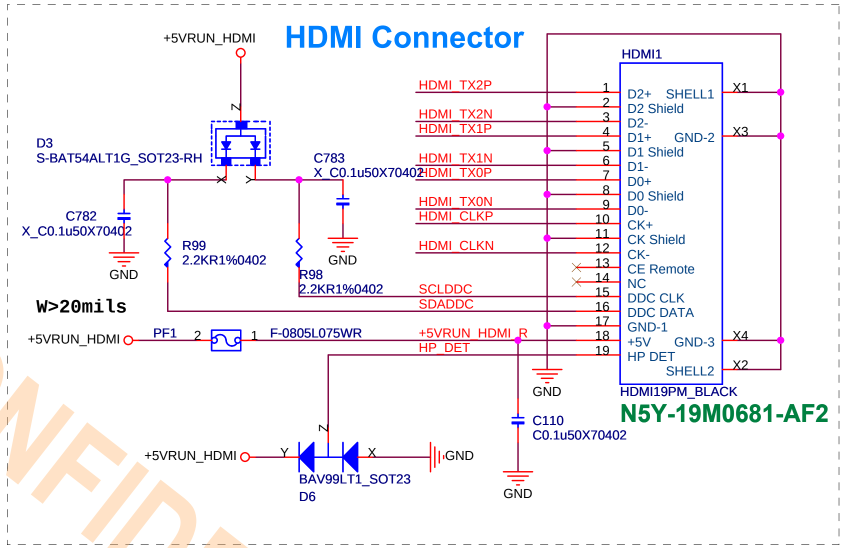
Date: Tuesday, May 20, 2014 | Sheet 35 of 69



USB 3.0 / iCharger
USB3.0 CNT-1
USB3.0 Port-5
USB2.0 Port-8
SPI ROM For FW (stuff first)
M31-2551283-P81
需使用與EC ROM不同的料號上件
For 0A Consumption measure
PCIE to USB 3.1
ASM1142
B02-010422C-AD0
R830 default no stuff
Colay for 1142
For 1142
Close Pin 13
0.1uF*7
0.1uF*4
0.1uF*2
Confirm BIOS USB SMI pin for legacy mode used
20140505add
I31-0111A29-U33
If Ipod charger none used, stuff it
I36-5478102-G07
20140312 add
I31-0111A29-U33
USB 3.1 Port 1
i-Charger
I36-S25460C-T07
All C Close Connector
USB 3.0 / iCharger
USB3.0 CNT-1
USB3.0 Port-6
USB2.0 Port-9
N53-09M0241-AF2
EMI
MICRO-STAR INT'L CO.,LTD.
USB 3.0 / iCharger
MS-16H3
0B
Tuesday, May 20, 2014
Sheet 36 of 69

HDMI Repeater

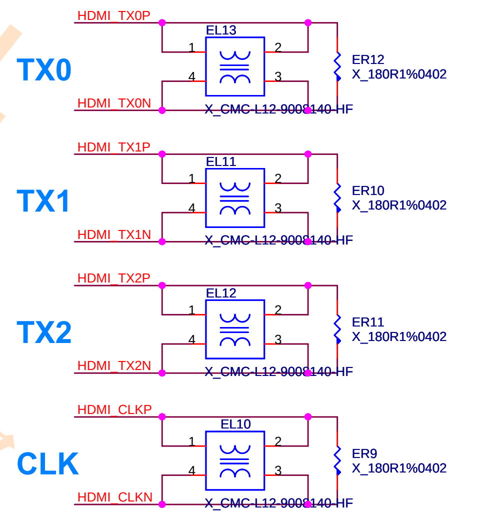


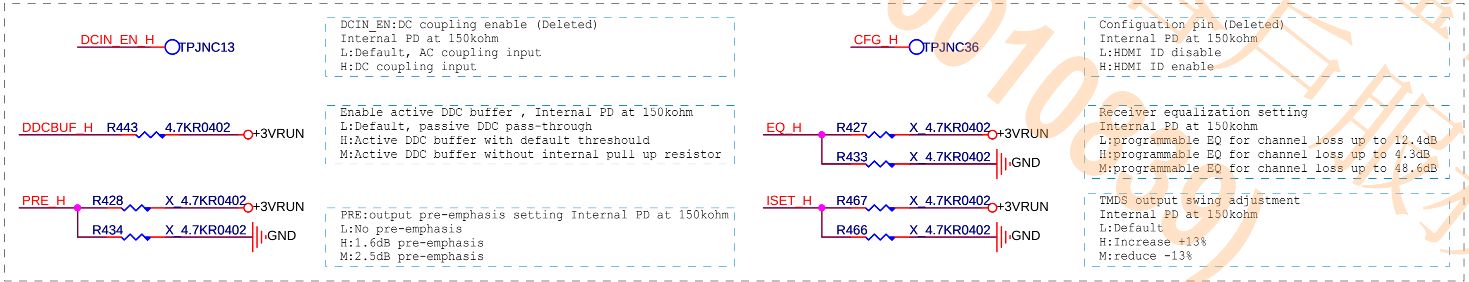


An HDMI Source shall have +5V Power signal
over-current protection of no more than 0.5A.

HPD_SNK Internal PD 150kohm

EMI Close Connector





DCIN_EN:DC coupling enable (Deleted)
Internal PD at 150kohm
L:Default, AC coupling input
H:DC coupling input

Enable active DDC buffer , Internal PD at 150kohm
L:Default, passive DDC pass-through
H:Active DDC buffer with default threshould
M:Active DDC buffer without internal pull up resistor

PRE:output pre-emphasis setting Internal PD at 150kohm
L:No pre-emphasis
H:1.6dB pre-emphasis
M:2.5dB pre-emphasis

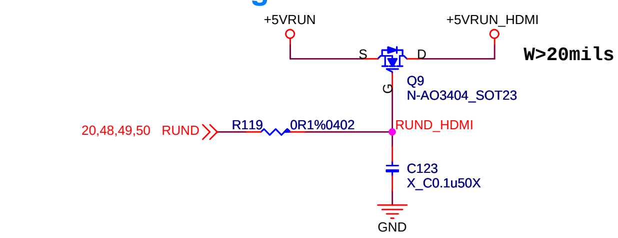
Configuation pin (Deleted)
Internal PD at 150kohm
L:HDMI ID disable
H:HDMI ID enable

Receiver equalization setting
Internal PD at 150kohm
L:programmable EQ for channel loss up to 12.4dB
H:programmable EQ for channel loss up to 4.3dB
M:programmable EQ for channel loss up to 48.6dB

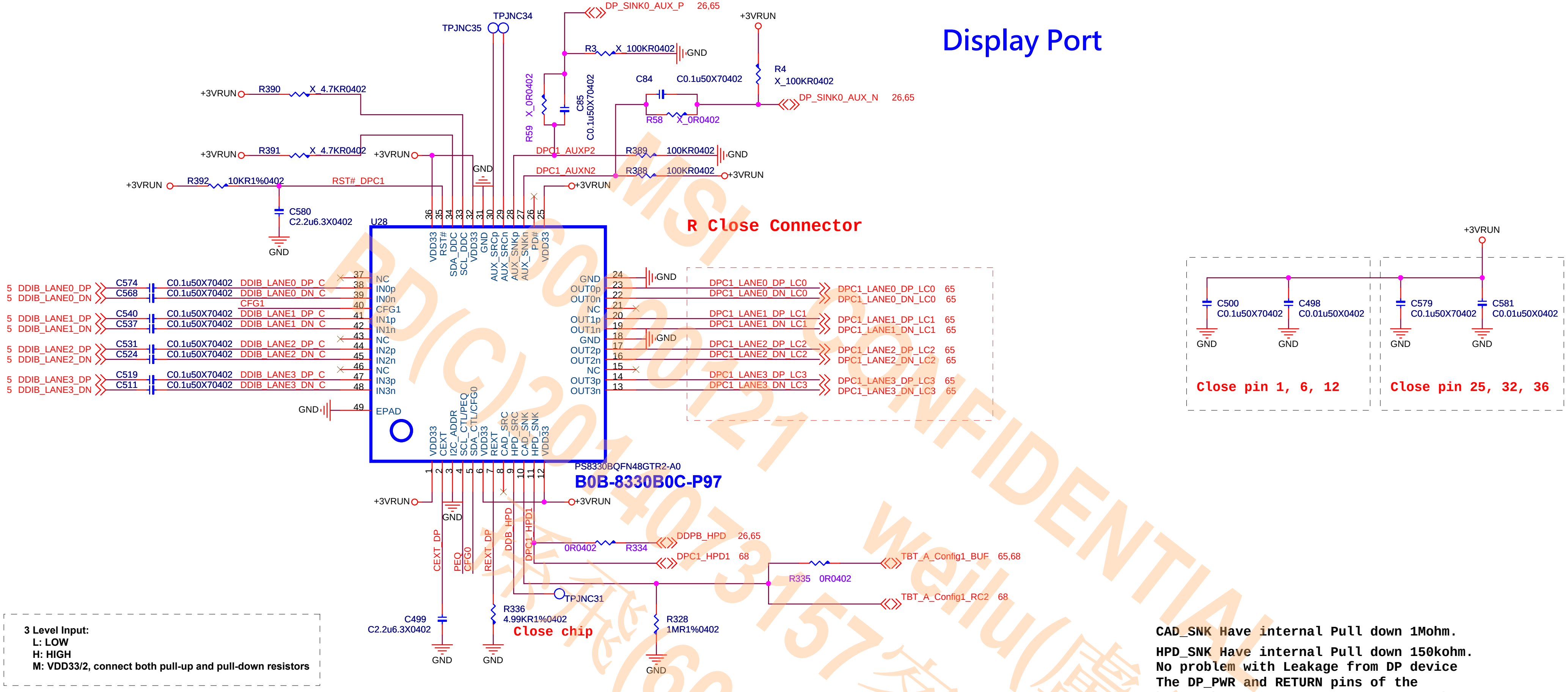
TMDS output swing adjustment
Internal PD at 150kohm
L:Default
H:Increase +13%
M:reduce -13%

ADDR1 (CFG)	ADDR0 (EQ)	I2C control bus address (Internal pull down at ~150kΩ, 3.3V I/O)
0	0	0x4C / 4D (default)
0	1	0x5C / 5D
1	0	0xCC / CD
1	1	0xEC / ED

Avoid HDMI Leakage



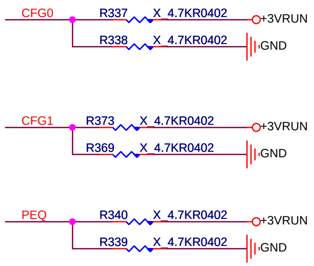
Display Port



3 Level Input:
- L: LOW
- H: HIGH
- M: VDD33/2, connect both pull-up and pull-down resistors

CAD_SNK Have internal Pull down 1Mohm.

HPD_SNK Have internal Pull down 150kohm.
No problem with Leakage from DP device
The DP_PWR and RETURN pins of the
box-to-box connectors must support the
maximum current rating of 500mA.

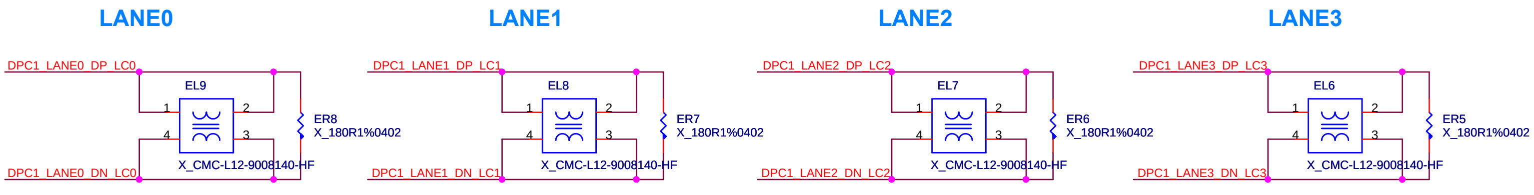



```
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
   L: default, automatic EQ enable & AUX interception enable
   H: automatic EQ disable & AUX interception enable
   M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing
```

```
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
   H: default, auto test disable & input offset cancellation enable
   L: auto test enable & input offset cancellation enable
   M: auto test disable & input offset cancellation disable
```

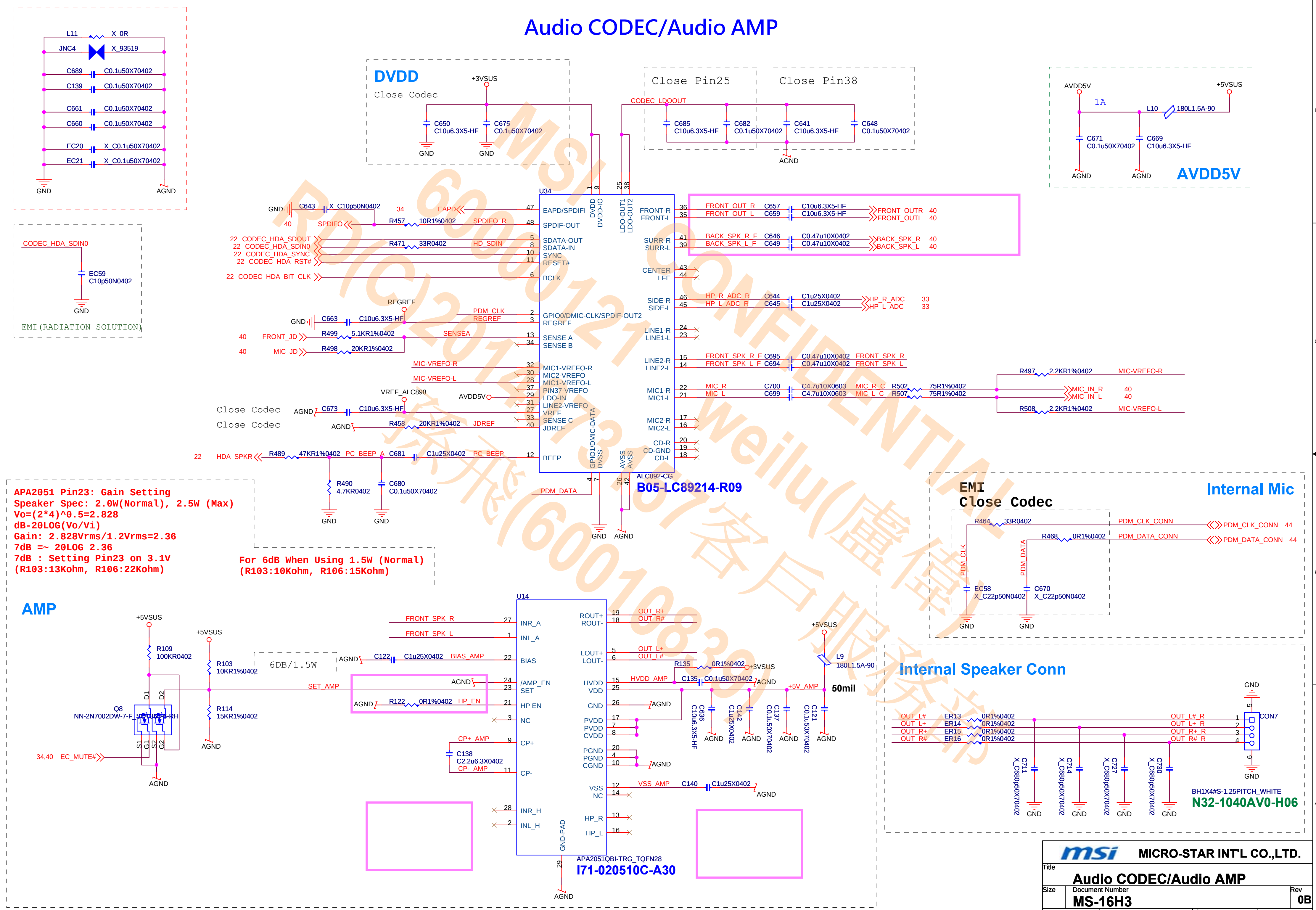
```
Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.
   L: default, LEQ, compensate channel loss up to 12dB @ HBR2
   H: HEQ, compensate channel loss up to 15dB @ HBR2
   M: LLEQ, compensate channel loss up to 5dB @ HBR2
```

EMI Close Connector



MICRO-STAR INT'L CO.,LTD.	
Title	DP witch Repeater
Size / Document Number	MS-16H3
Rev	0B
Date	Tuesday, May 20, 2014
Sheet	38 of 69

Audio CODEC/Audio AMP



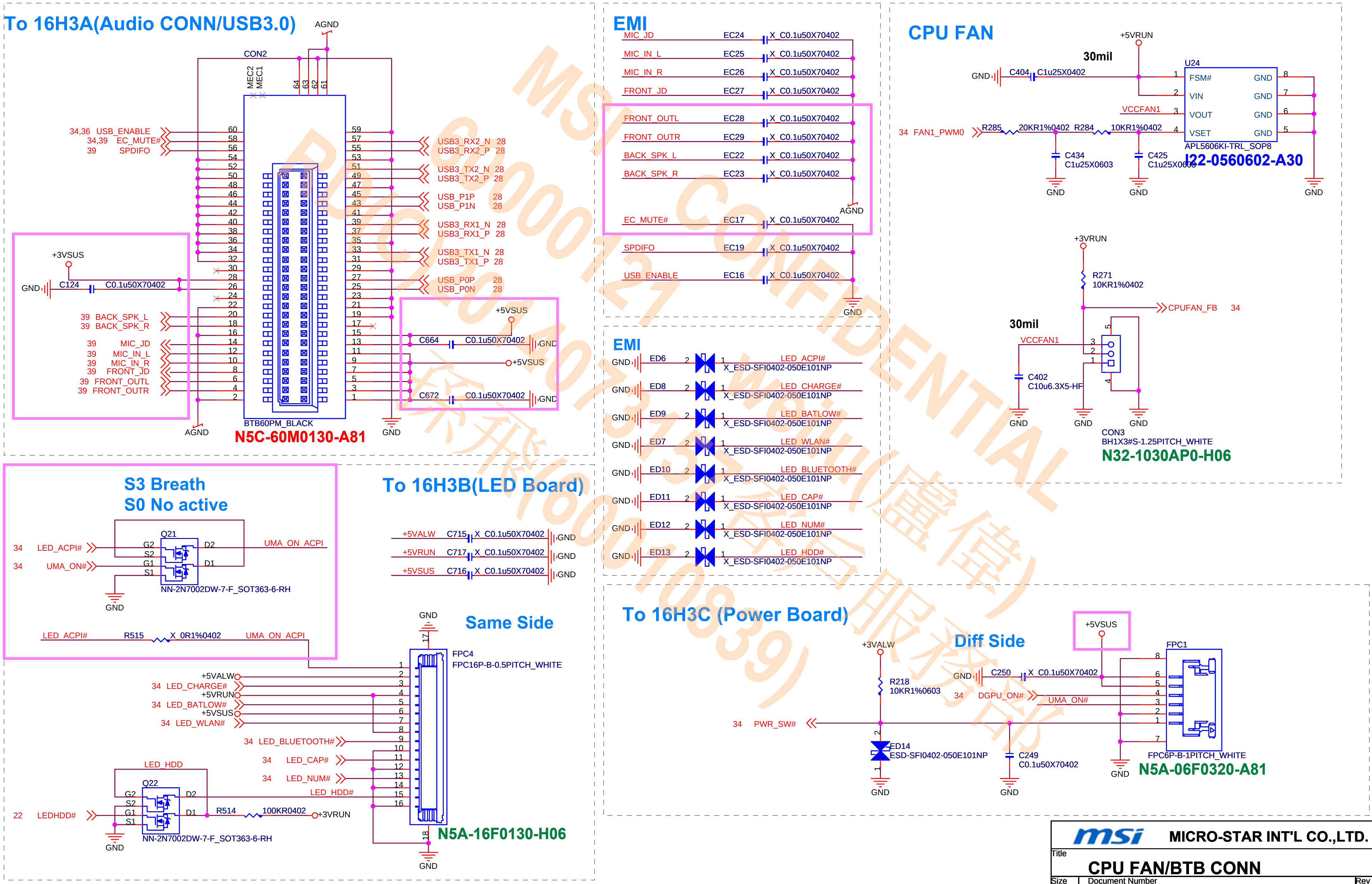
APA2051 Pin23: Gain Setting
Speaker Spec: 2.0W(Normal), 2.5W (Max)
Vo=(2*4)^0.5=2.828
dB-20LOG(Vo/Vi)
Gain: 2.828Vrms/1.2Vrms=2.36
7dB =~ 20LOG 2.36
7dB : Setting Pin23 on 3.1V
(R103:13Kohm, R106:22Kohm)

For 6dB When Using 1.5W (Normal)
(R103:10Kohm, R106:15Kohm)

MICRO-STAR INT'L CO.,LTD.

Title	Audio CODEC/Audio AMP	
Size	Document Number: MS-16H3	Rev: 0B
Date: Tuesday, May 20, 2014	Sheet 39 of 69	

CPU FAN/BTB CONN

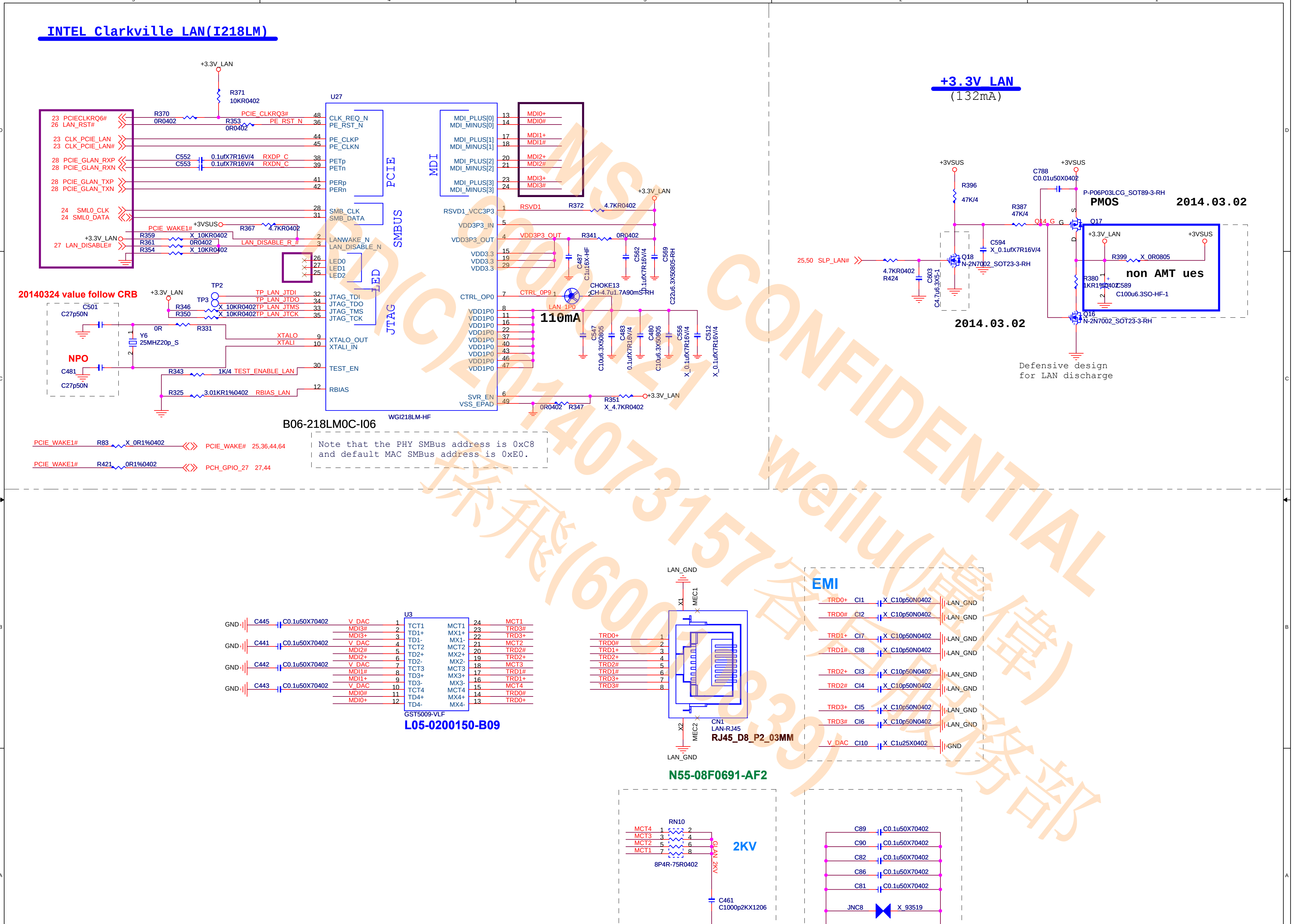


MICRO-STAR INT'L CO.,LTD.

Title: CPU FAN/BTB CONN

Size | Document Number: MS-16H3 | Rev: 0B

Date: Tuesday, May 20, 2014 | Sheet 40 of 69



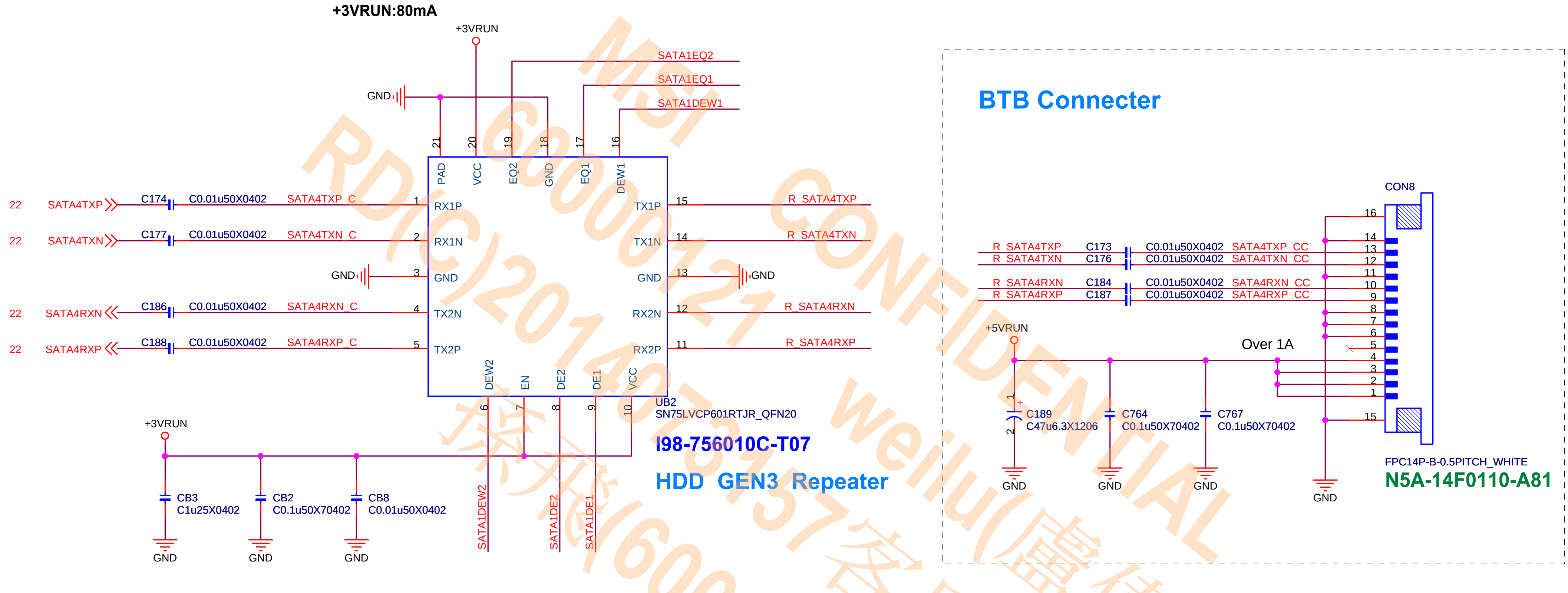
MICRO-STAR INT'L CO.,LTD.

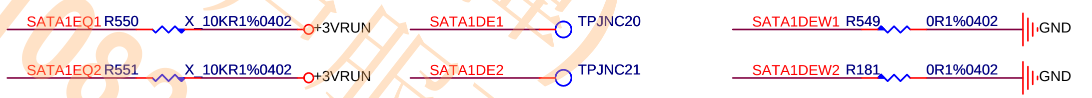
Title: **INTEL Clarkville LAN (I218LM)**

Size	Document Number	Rev
	MS-16H3	0B

Date: Tuesday, May 20, 2014 Sheet 41 of 69

HDD (With Repeater)





TI SN75LVCP601RTJR HW Setting

DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	EQ1/EQ2	CH1/CH2Equalization dB (at 6Gbps)
NC (***default***)	–4	NC (***default***)	0
0	0	0	7
1	–2	1	14

DEW1/DEW2	Device Function → DE Width for CH1/CH2
0	De-emphasis pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps)
1 (***default***)	De-emphasis pulse duration, long (recommended setting when link operates at SATA 1.5/3 Gbps speed only)

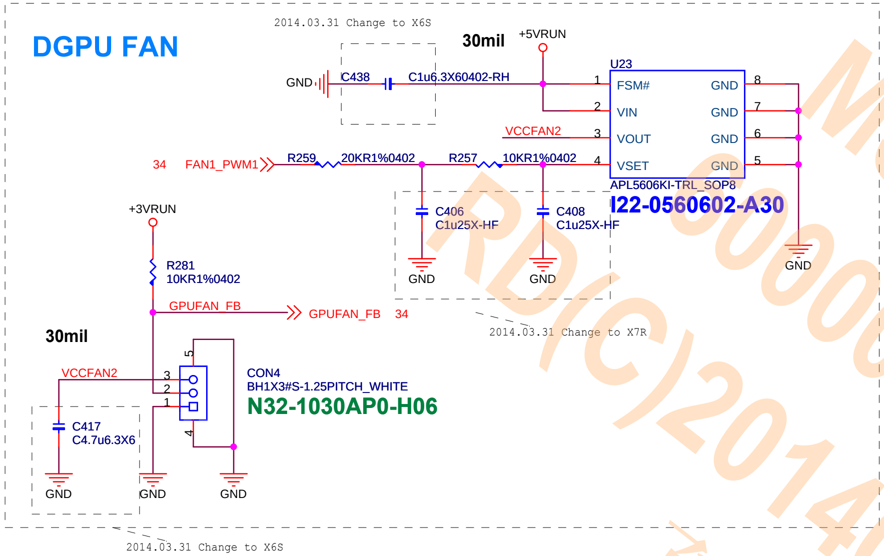
MICRO-STAR INT'L CO.,LTD.

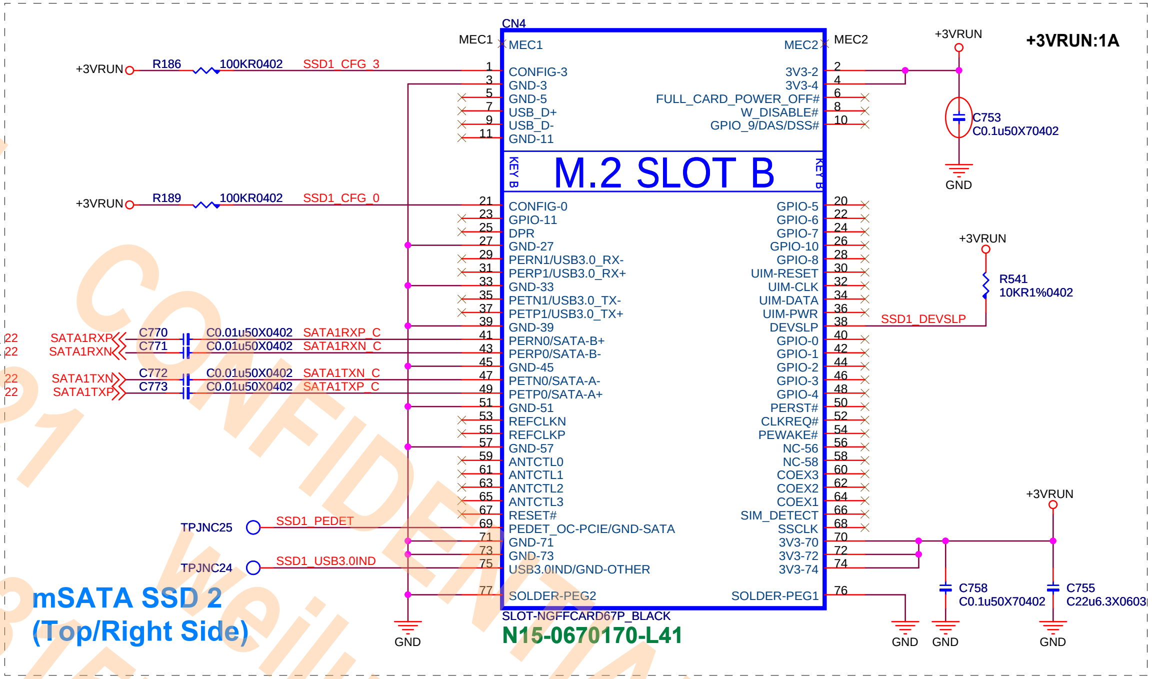
Title: **HDD With Repeater**

Size | Document Number: **MS-16H3** | Rev: **0B**

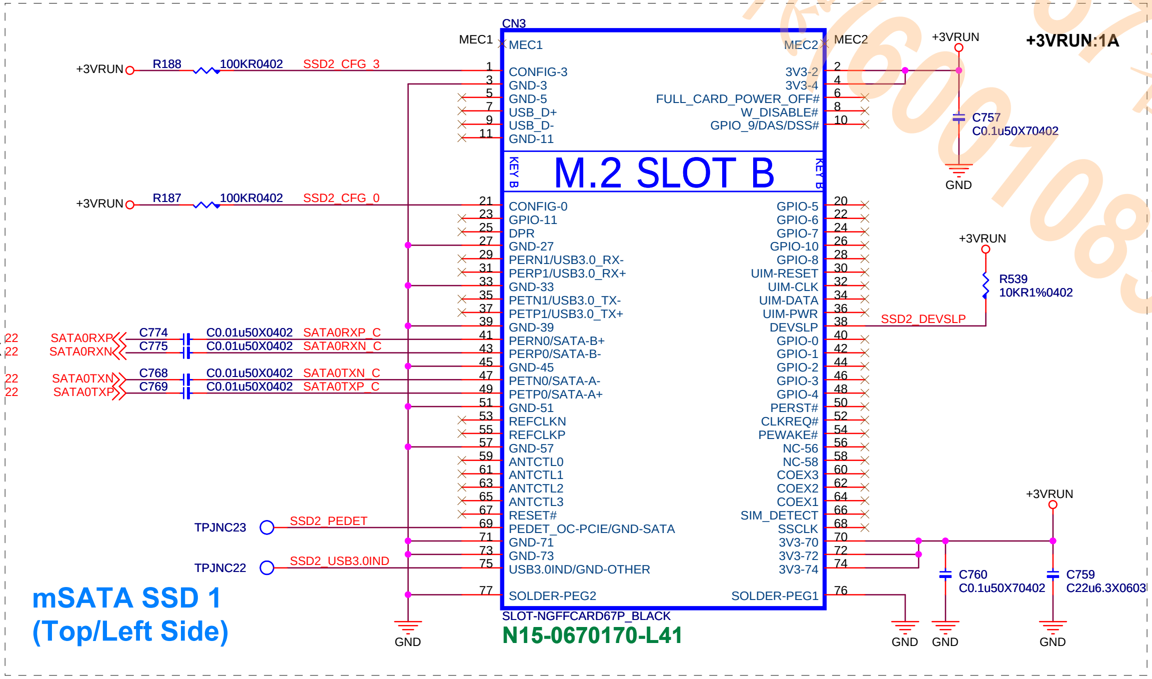
Date: Tuesday, May 20, 2014 | Sheet 42 of 69

SSD/ DGPU FAN





40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host transmitter differential signal pair



MICRO-STAR INT'L CO.,LTD.

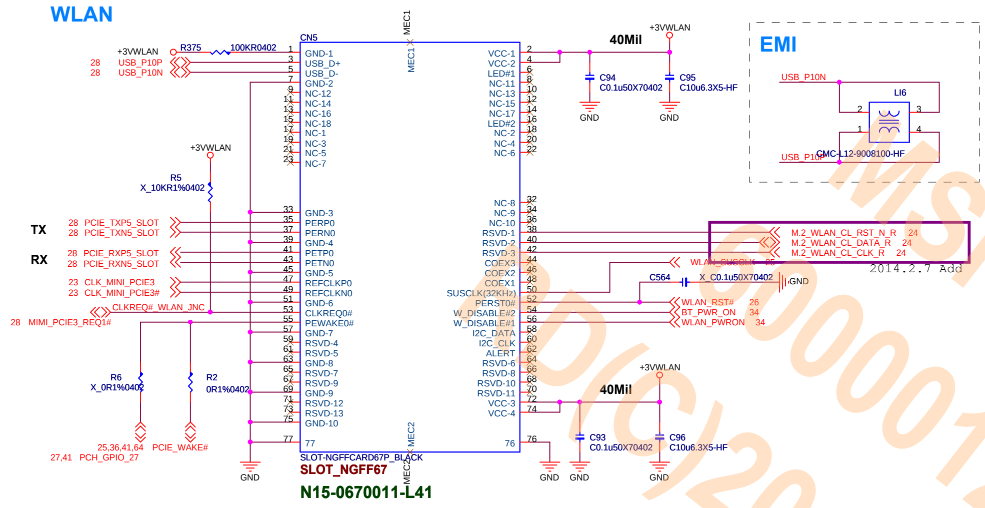
Title: SSD/ DGPU FAN

Size | Document Number: MS-16H3 | Rev: 0B

Date: Tuesday, May 20, 2014 | Sheet 43 of 69

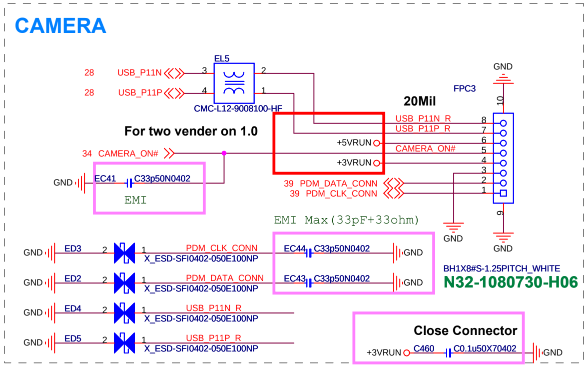
WLAN /Camera/ClickPad/FP

WLAN

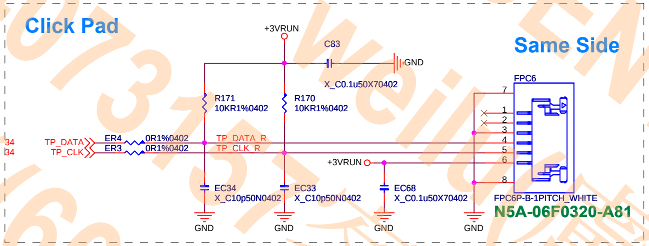


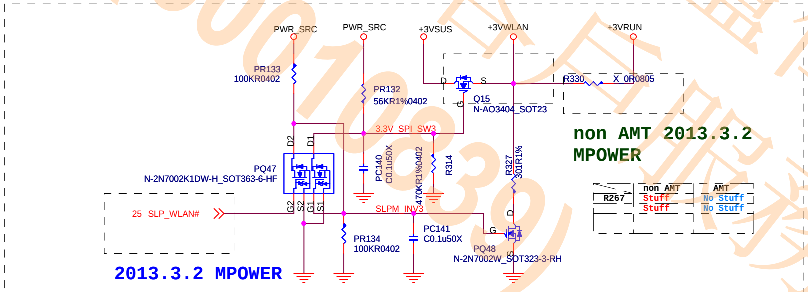
Pin	Signal	Pin	Signal
Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

CAMERA



Click Pad



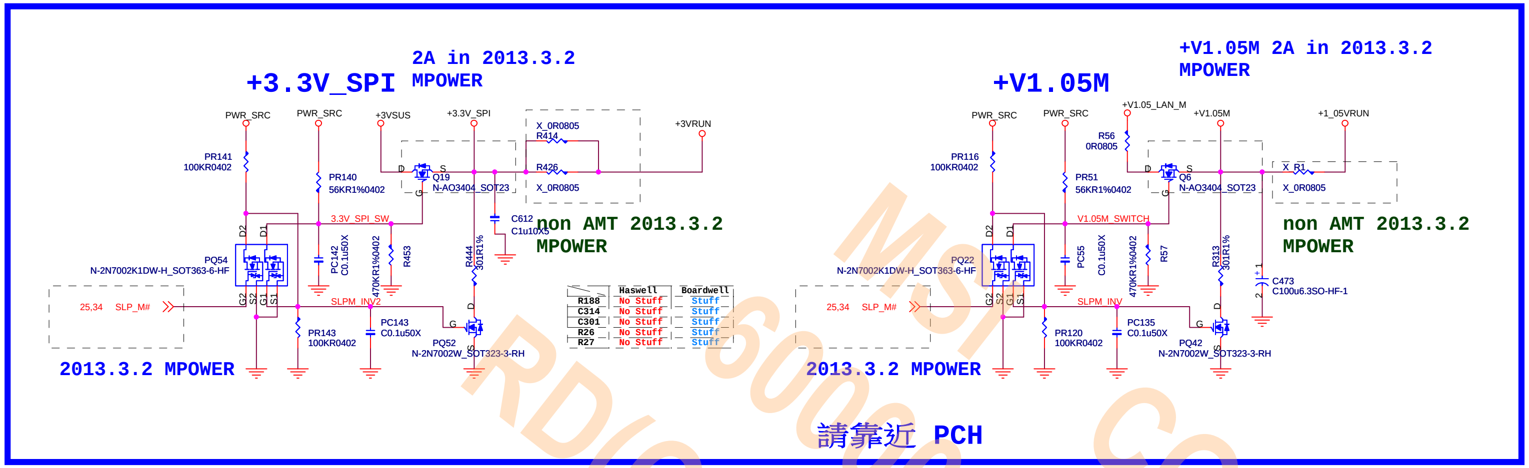


2014.2.11 for EC ON/OFF,
from EC OD control.

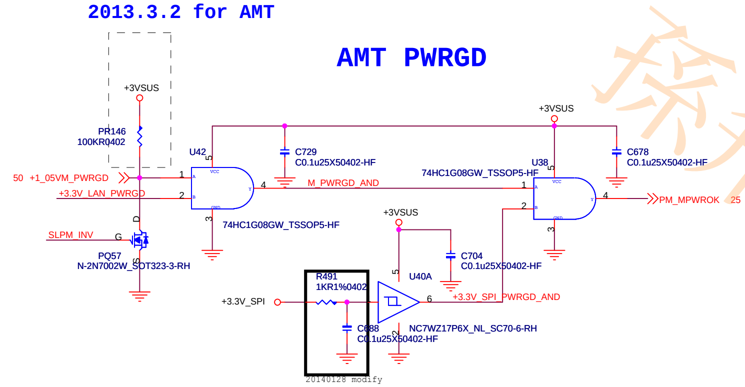
If Non-AMT, R267 stuff.This block no-stuff
If AMT, This block stuff, R267 no-stuff

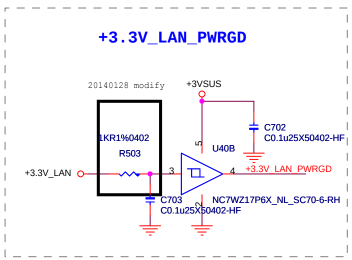
MICRO-STAR INT'L CO.,LTD.

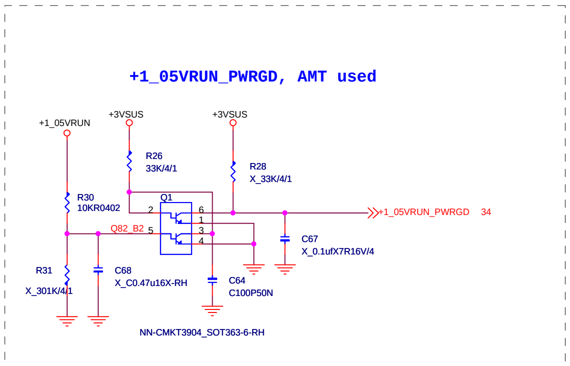
Title	WLAN /Camera/ClickPad/FP	
Size	Document Number: MS-16H3	Rev: 0B
Date: Tuesday, May 20, 2014	Sheet 44 of 69	



	Haswell	Boardwell
R188	No Stuff	Stuff
C314	No Stuff	Stuff
C301	No Stuff	Stuff
R26	No Stuff	Stuff
R27	No Stuff	Stuff







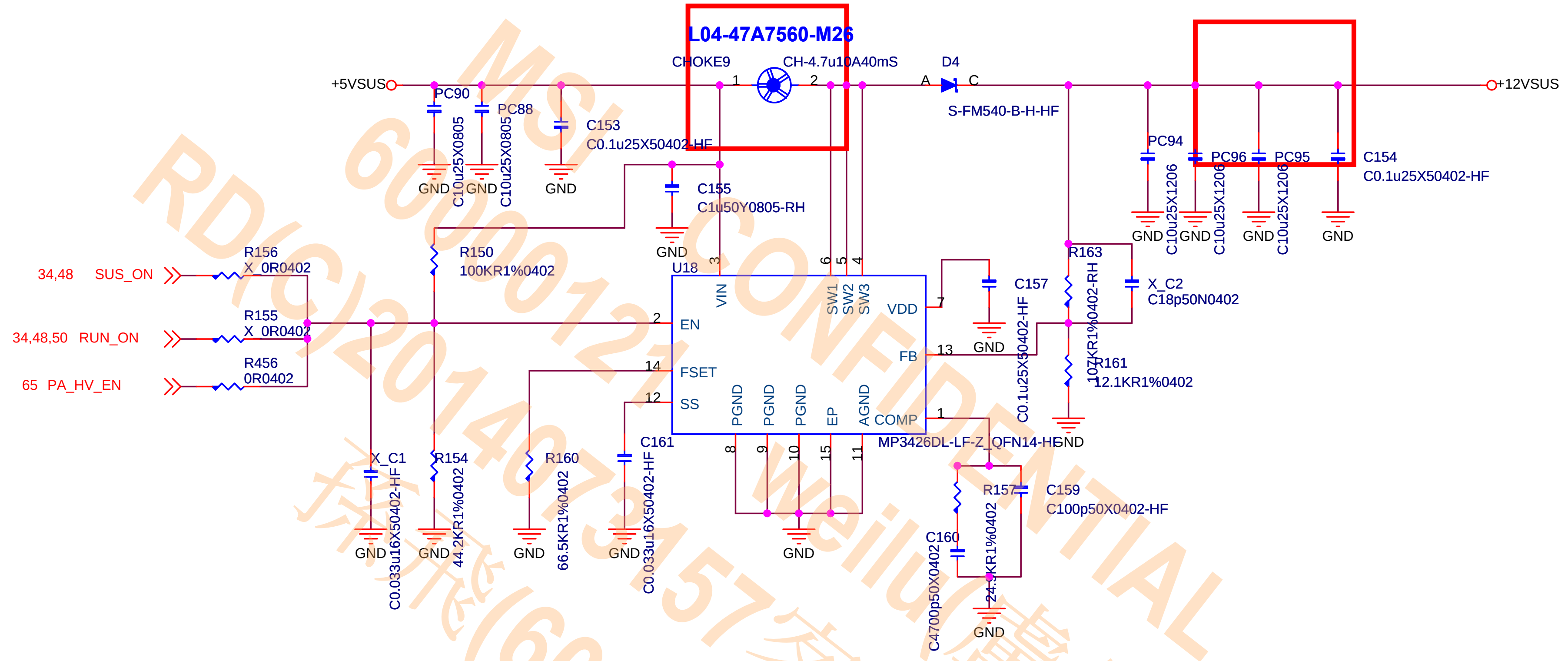
MICRO-STAR INT'L CO.,LTD.

Title: M-POWER

Size | Document Number: MS-16H3 | Rev: 0B

Date: Tuesday, May 20, 2014 | Sheet 45 of 69

TBT Power 5V Boost 12V 1A



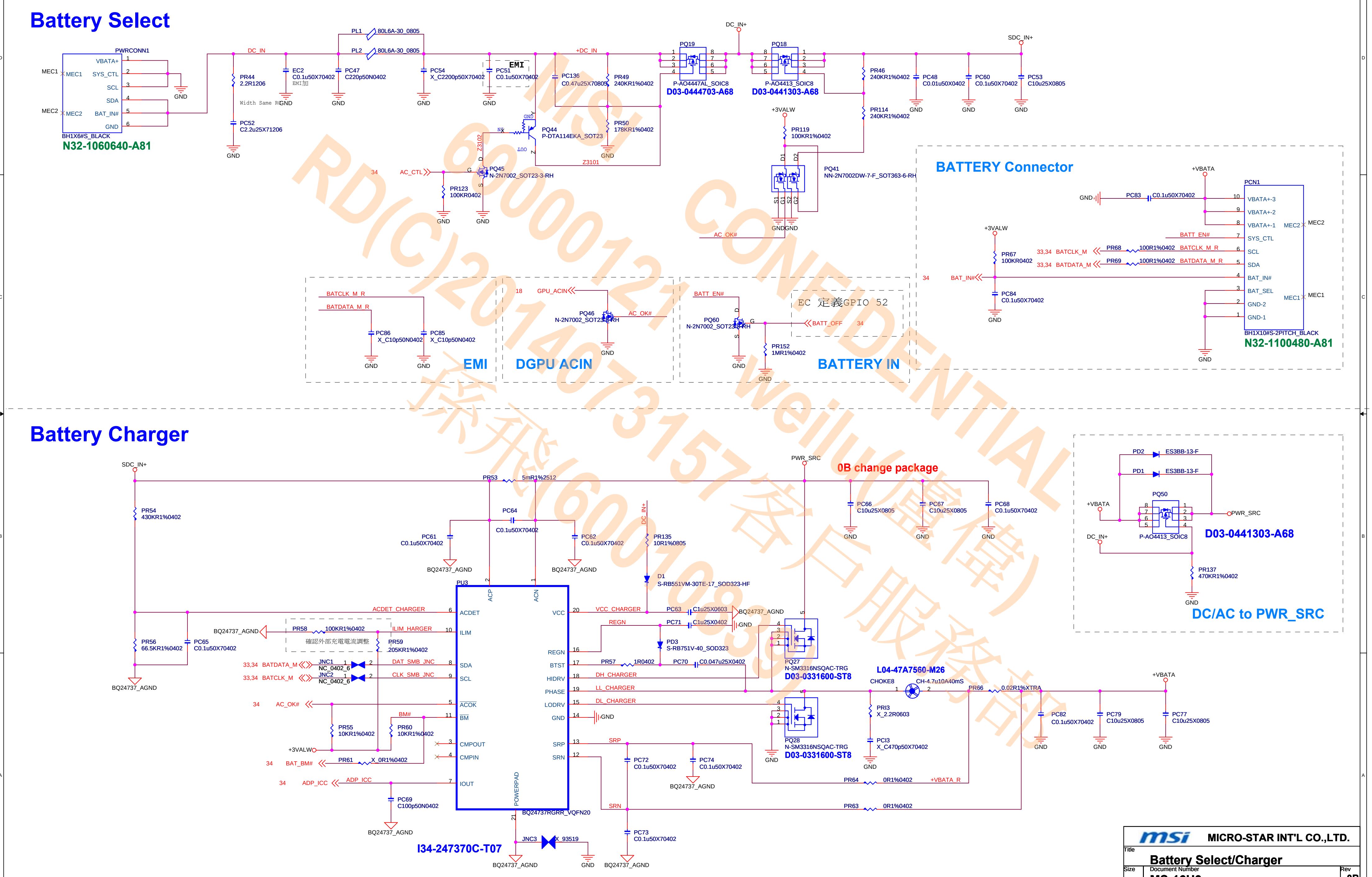
MICRO-STAR INT'L CO.,LTD.

Title: **Thunderbolt Power**

Size | Document Number: **MS-16H3** | Rev: **0B**

Date: Tuesday, May 20, 2014 | Sheet 46 of 69

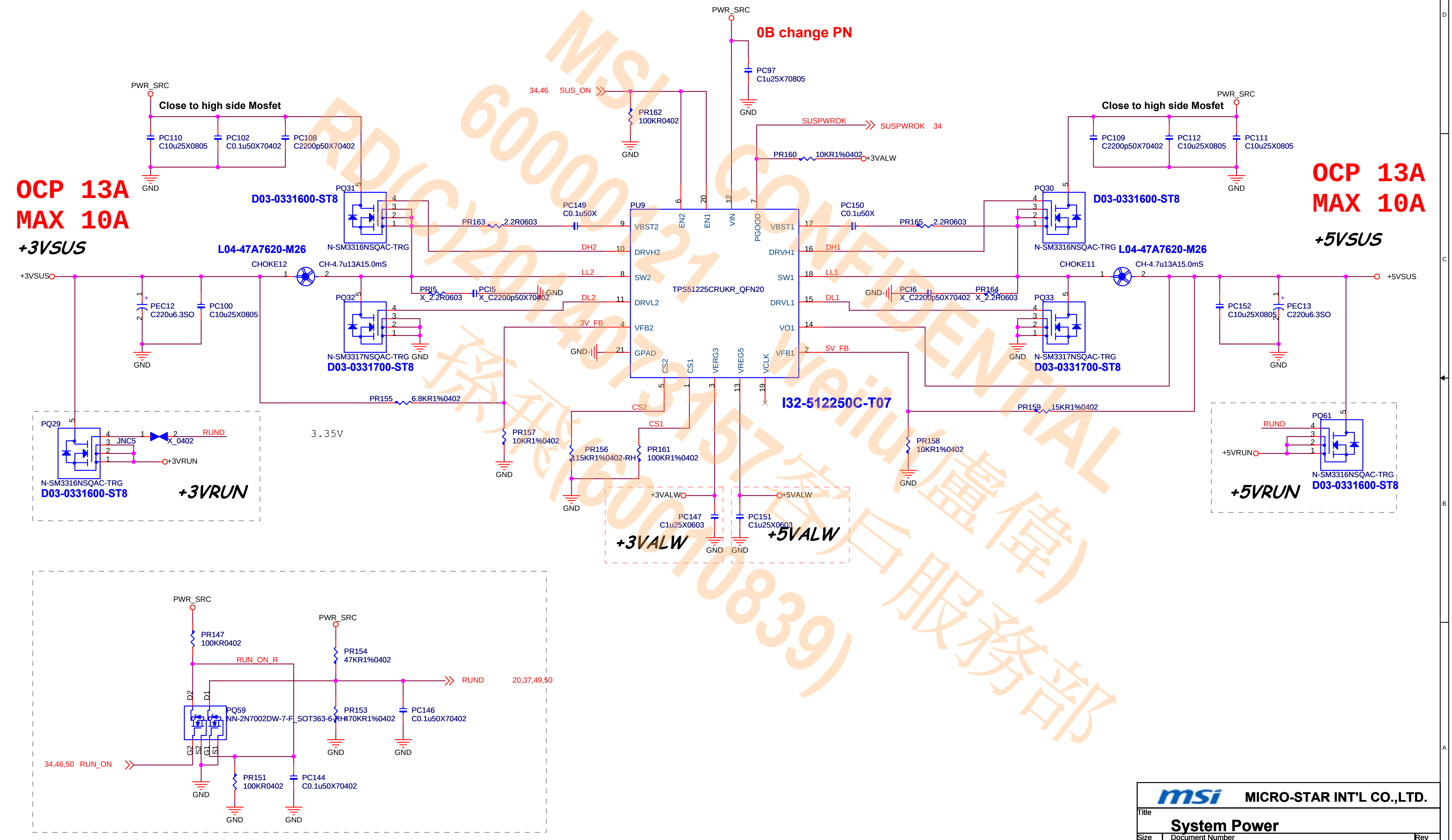
Battery Select/Charger



MICRO-STAR INT'L CO.,LTD.

Title	Battery Select/Charger
Size / Document Number	MS-16H3
Rev	0B
Date	Tuesday, May 20, 2014
Sheet	47 of 69

System Power

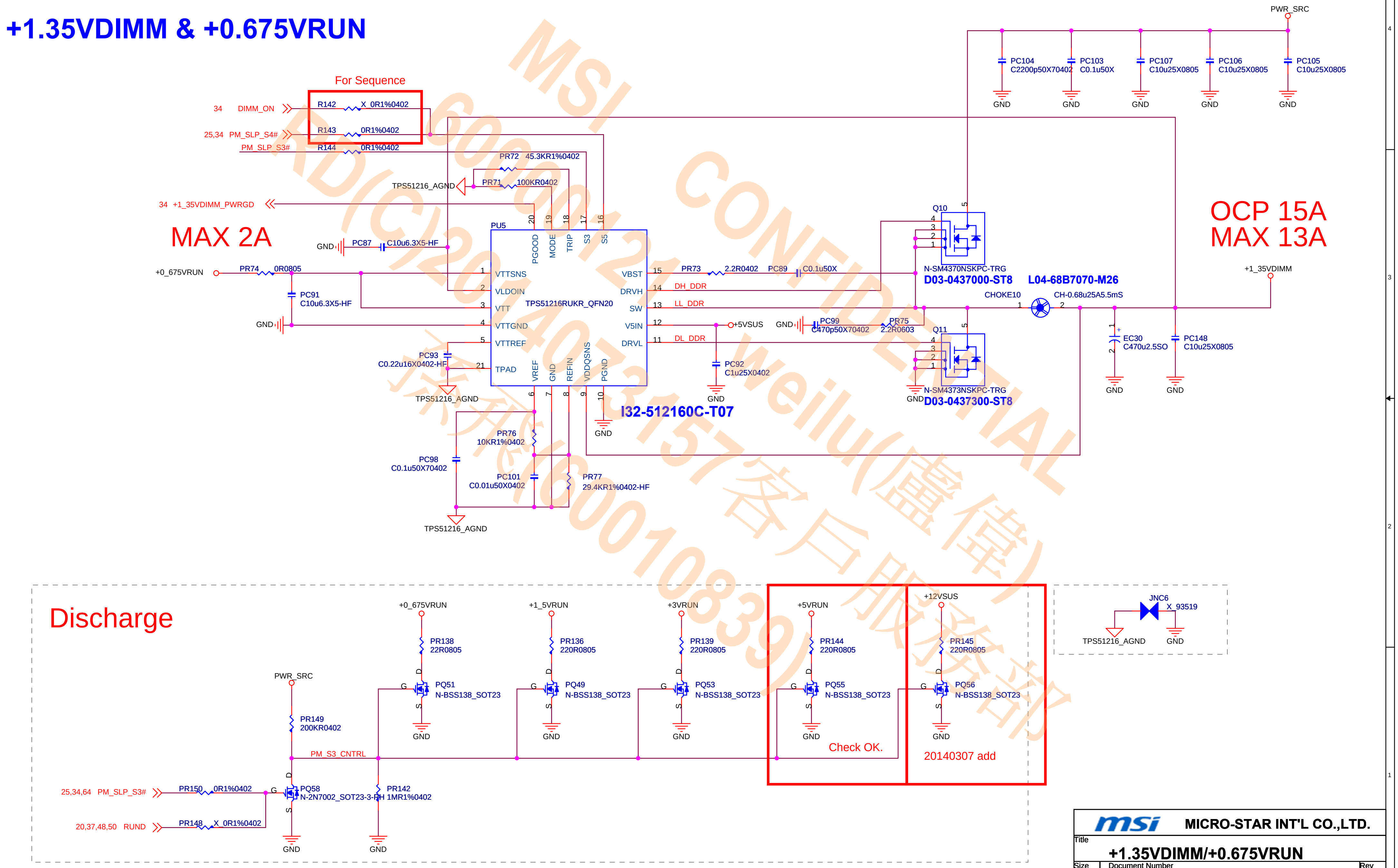


MICRO-STAR INT'L CO.,LTD.

Title	System Power	
Size	Document Number: MS-16H3	Rev: 0B
Date: Tuesday, May 20, 2014	Sheet 48 of 69	

+1.35VDIMM/+0.675VRUN

+1.35VDIMM & +0.675VRUN



msi	MICRO-STAR INT'L CO.,LTD.		
Title	+1.35VDIMM/+0.675VRUN		
Size	Document Number: MS-16H3		Rev: 0B
Date: Tuesday, May 20, 2014	Sheet 49 of 69		

+1_05VRUN / +1_5VRUN

+1.05VRUN

3/2 non AMT
AMT PR131 and PR127 stuff
non-AMT PR130 and PR126 stuff

20140302 modify
34 +1_05V_PWRGD
PR130 X_0R0402
PR131 0R0402
45 +1_05VM_PWRGD
PR129 100KR1%0402
GND
25,41 SLP_LAN#
PR127 1KR1%0402
20140129 modify
34,46,48 RUN_ON
PR126 X_1KR1%0402
20140302 modify
PC137 X_C0.1u50X70402
GND

PU8
TPS51211DSCR
PGOOD
TRIP
EN
VFB
RF
VBST
DRVH
SW
V5IN
DRVL
GND

PR128 2.2R0402
PC139 C0.1u50X
DH_1_05VRUN
LL_1_05VRUN
+5VSUS
DL_1_05VRUN
PR125 2.2R0603
PC50 C1u25X0603
CI12 C470p50X70402
PR117 464KR1%0402
I32-5121100-T07

PWR_SRC
Close to high side Mosfet
PC59 C2200p50X70402
PC56 C0.1u50X
PC57 C10u25X0805
PC58 C10u25X0805
PQ26
N-SM3316NSQAC-TRG
D03-0331600-ST8
PQ23
N-SM3317NSQAC-TRG
D03-0331700-ST8
CHOKE7
CH-1.0u22A10mS
L04-0107800-M26
+V1.05_LAN_M
PEC11 C470u2.5SO
PQ25
N-AON7516_DFN3X3-HF
PR124 0R0402
RUND
20,37,48,49
PC138 X_C0.1u50X
+1_05VRUN
PR121 5.23KR1%0402
PR122 10KR1%0402
(Adjust +1_05VRUN=1.079V)

OCP 13A
MAX 10A
3/2 NON VPRO

+1.5VRUN

+5VSUS
PC81 C1u25X0603
GND
+3VSUS
W>40mils
PU4
VPP
VIN1
VIN2
POK
VEN
VO1
VO2
ADJ
GND
G9731F11U_SOP8-RH
PC80 C10u25X0805
34 +1_5VRUN_PWRGD
34,46,48 RUN_ON
W>80mils
+1_5VRUN
PR62 2.61KR1%0402
PC75 C47p50N0402
PC78 C22u6.3X50805-RH
PC76 C22u6.3X50805-RH
PR65 3.01KR1%0402

MAX 2A

MSI	MICRO-STAR INT'L CO.,LTD.
Title	+1_05VRUN / +1_5VRUN
Size	
Document Number	MS-16H3
Rev	0B
Date:	Tuesday, May 20, 2014
Sheet	50 of 69

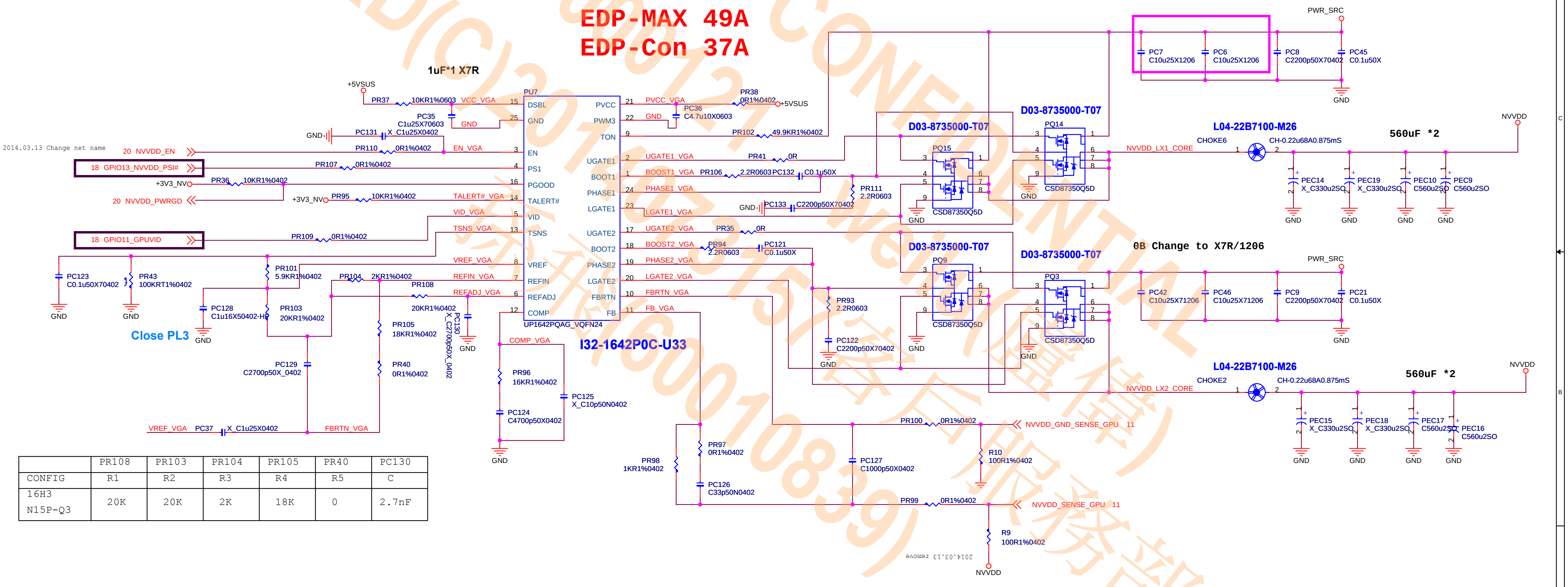
DGPU POWER NVVDD

DGPU POWER / UP1642PQAG

CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

EDP-Peak 57A
EDP-MAX 49A
EDP-Con 37A

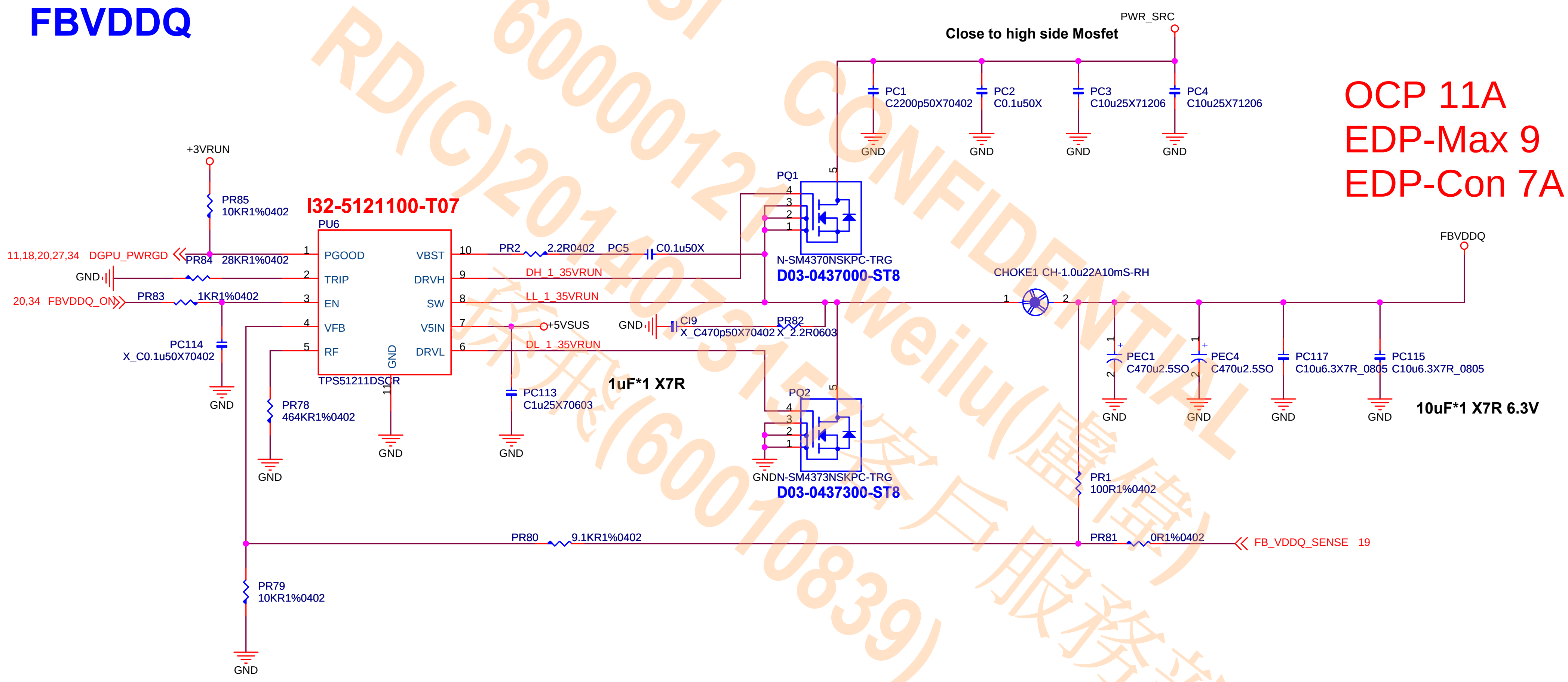
0B Change to X7R/1206
1.0 Change to X5R/1206 high



	PR108	PR103	PR104	PR105	PR40	PC130
CONFIG	R1	R2	R3	R4	R5	C
16H3 N15P-Q3	20K	20K	2K	18K	0	2.7nF

MICRO-STAR INT'L CO.,LTD.
Title: DGPU POWER NVVDD
Size | Document Number: MS-16H3 | Rev: 0B
Date: Tuesday, May 20, 2014 | Sheet 51 of 69

DGPU POWER FBVDDQ



MICRO-STAR INT'L CO.,LTD.

Title: DGPU POWER FBVDDQ

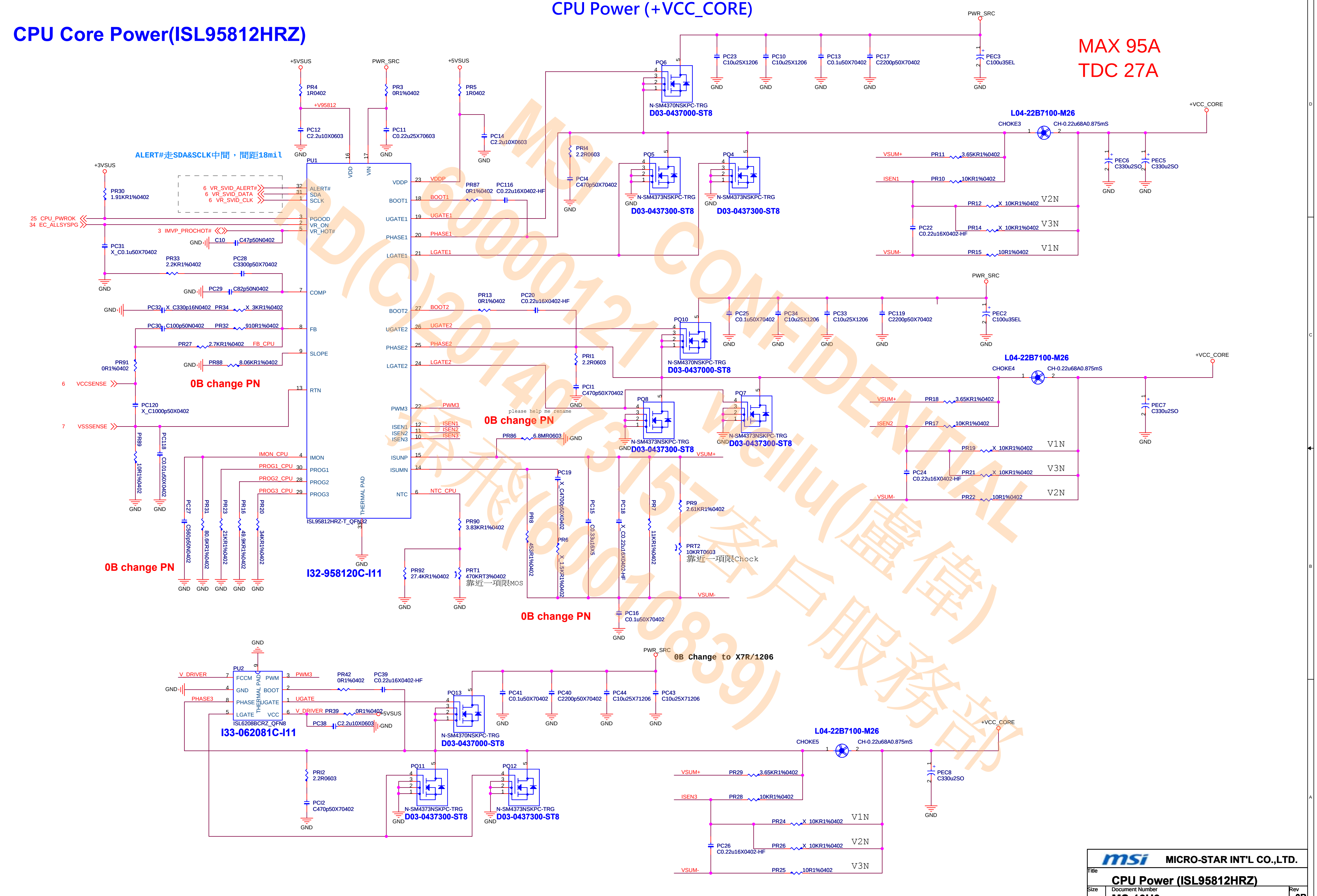
Size	Document Number	Rev
	MS-16H3	0B

Date: Tuesday, May 20, 2014 — Sheet 52 of 69

CPU Core Power(ISL95812HRZ)

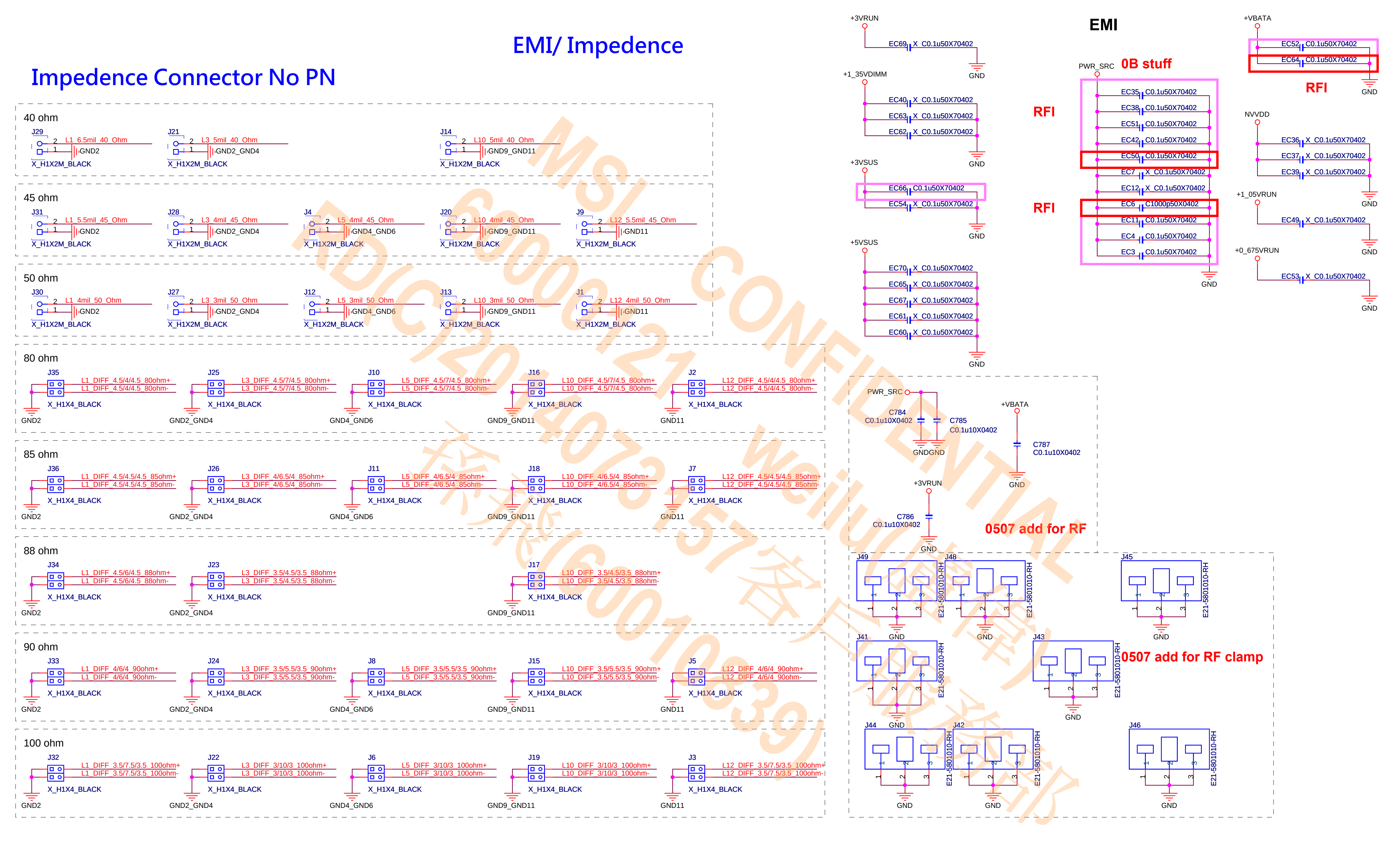
CPU Power (+VCC_CORE)

MAX 95A
TDC 27A



MICRO-STAR INT'L CO.,LTD.

Title	CPU Power (ISL95812HRZ)
Size	Document Number: MS-16H3
Rev	0B
Date	Tuesday, May 20, 2014
Sheet	53 of 69



MICRO-STAR INT'L CO.,LTD.

Title: EMI/ Impedence

Size	Document Number	Rev
	MS-16H3	0B

Date: Tuesday, May 20, 2014 Sheet 54 of 69

CPU/GPU Holes

MCPU4 H_R200D150 — GND
MCPU2 H_R200D150 — GND
MCPU3 H_R200D150 — GND
MCPU1 H_R200D150 — GND

MGPU2 H_R276D169_PB — GND
MGPU4 H_R276D169_PB — GND
MGPU1 H_R276D169_PB — GND
MGPU3 H_R276D169_PB — GND

EMI

SPRING3
X_MECHCU,2.5*5.5*0.1mm

SPRING2
X_E2M-7213211-RH
GND
E2M-7213211-CA7

SPRING1
X_E23-1029060-RH
GND
E23-1029060-CA7

SPRING4
X_E2M-7213211-RH
GND
E2M-7213211-CA7

SPRING3
GND
E2M-2142011-CA7

RUBBER1
E2Y-6H20712-Y40
RUBBER

RUBBER2
E2Y-6H21312-Y40
RUBBER

RUBBER3
E2Y-6H21312-Y40
RUBBER

BRACKET1
307-6H20111-C22
CPU_BRACKET

BRACKET2
307-6H20111-C22
CPU_BRACKET

BRACKET3
307-6H20211-C22
GPU_BRACKET

MYLAR1
E2P-6H22111-Y42
MYLAR

MYLAR2
E2P-6H23111-Y42
MYLAR

MYLAR3
E2P-6H22711-Y42
MYLAR

PCB1
PF0-16H3110-H73
PF0-16H310B-H73

M1
X_H_R197D118_PT_V3
H_R197D118_PT_V3
GND

M6
X_H_R197D118_PT_V3
H_R197D118_PT_V3
GND

FM4 FM3 FM2 FM1
FM8 FM6 FM7 FM5

Hannstar: PF0-16H2110-H73
TRIPOD: PF0-16H2110-T53

UME1
HDMI Lable
X_HDMI ROYALTY
Y01-RHDMI03-000

UME2
BIOS Lable
X_BIOS_LABEL
G51-LA01678-A09

For MP

Fan Hole

MH4
H_R197D91
X_ME_ SCREW HOLE
GND

SSD Stand off

MH2
H_R220D146_PTB
E2B-16H2020
GND

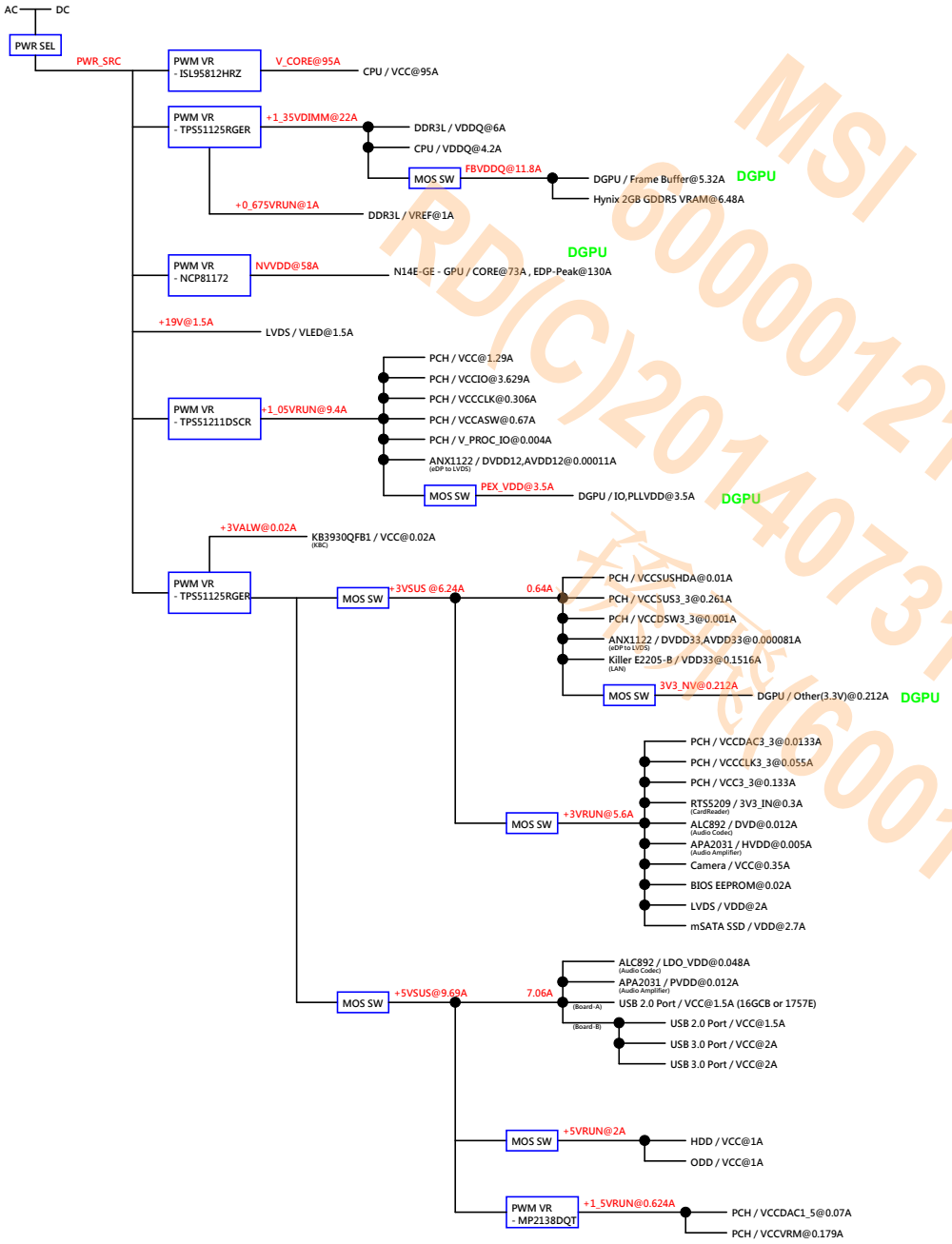
MH1
H_R220D146_PTB
E2B-16H2020
GND

MH3
NPTH157
X_NPTH157

MICRO-STAR INT'L CO.,LTD.

Title: Screw/ME
Size:
Document Number: MS-16H3
Rev: 0B
Date: Tuesday, May 20, 2014
Sheet 55 of 69

MS-16H2 Power Delivery Chart



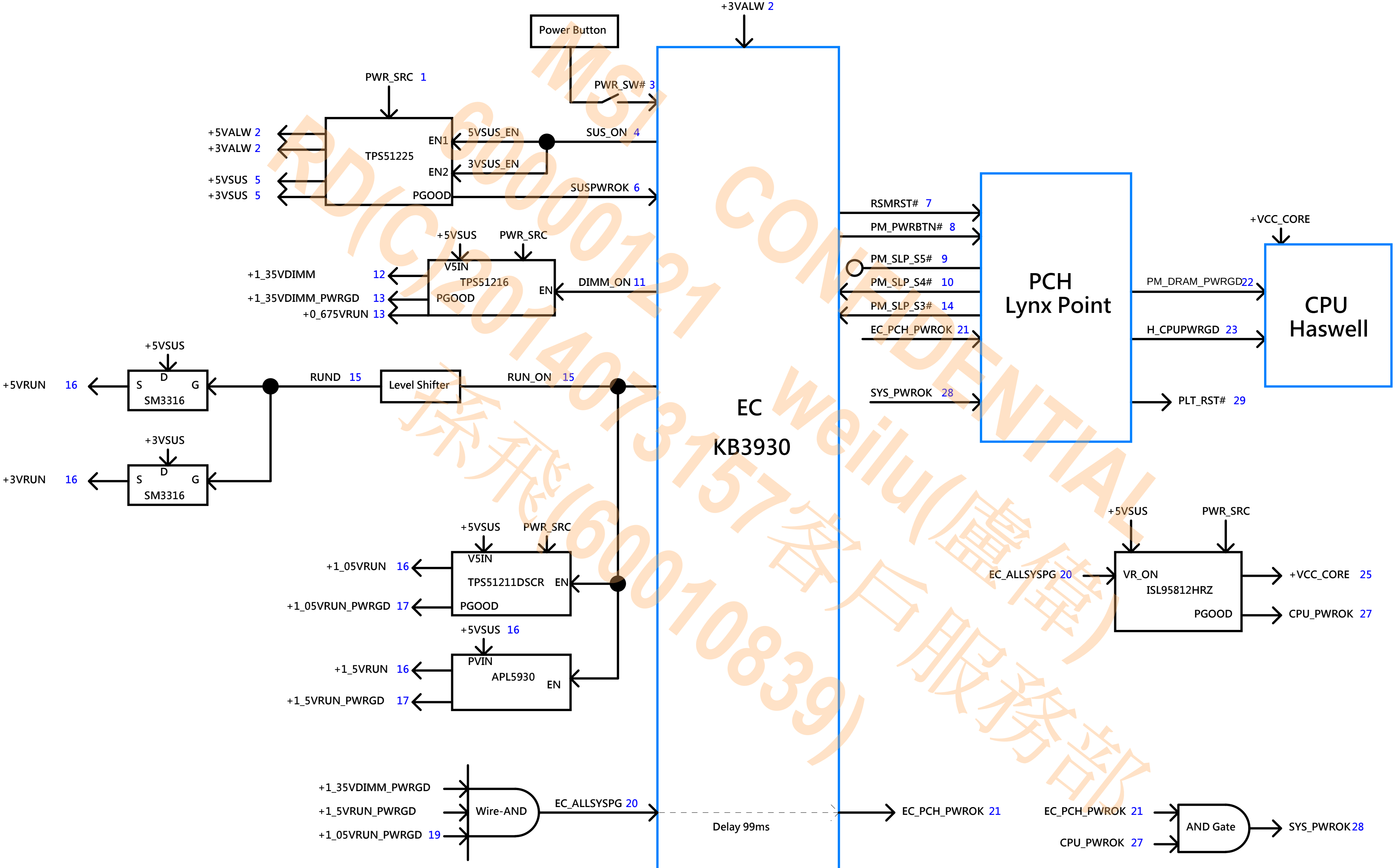
MICRO-STAR INT'L CO.,LTD.

Power Delivery Map

MS-16H3

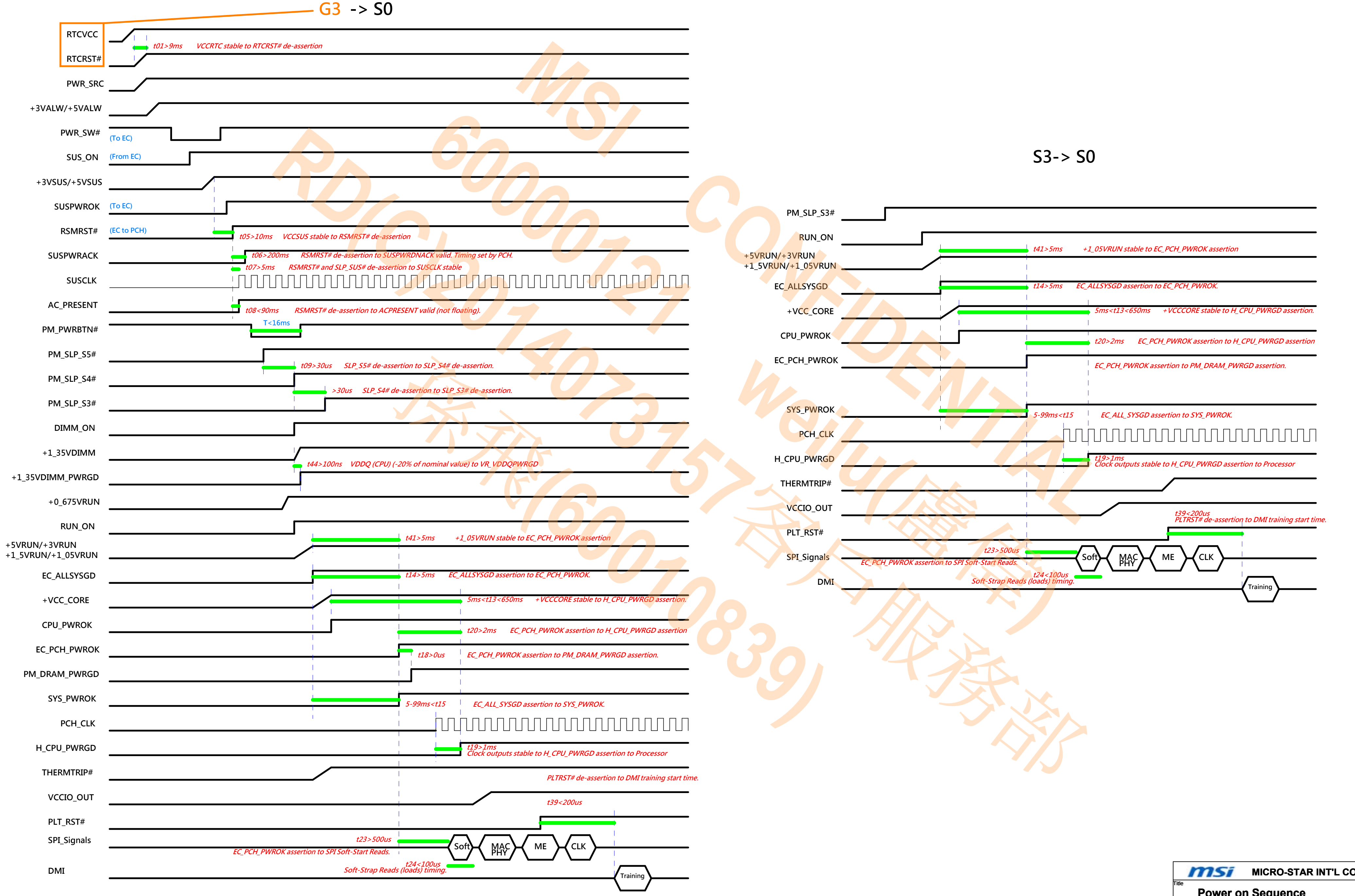
08

MS-16H2 Power on Block Diagram



msi MICRO-STAR INT'L CO.,LTD.
Title: Power on Block Diagram
Size | Document Number: MS-16H3 | Rev: 0B
Date: Tuesday, May 20, 2014 | Sheet 61 of 69

Power on Sequence

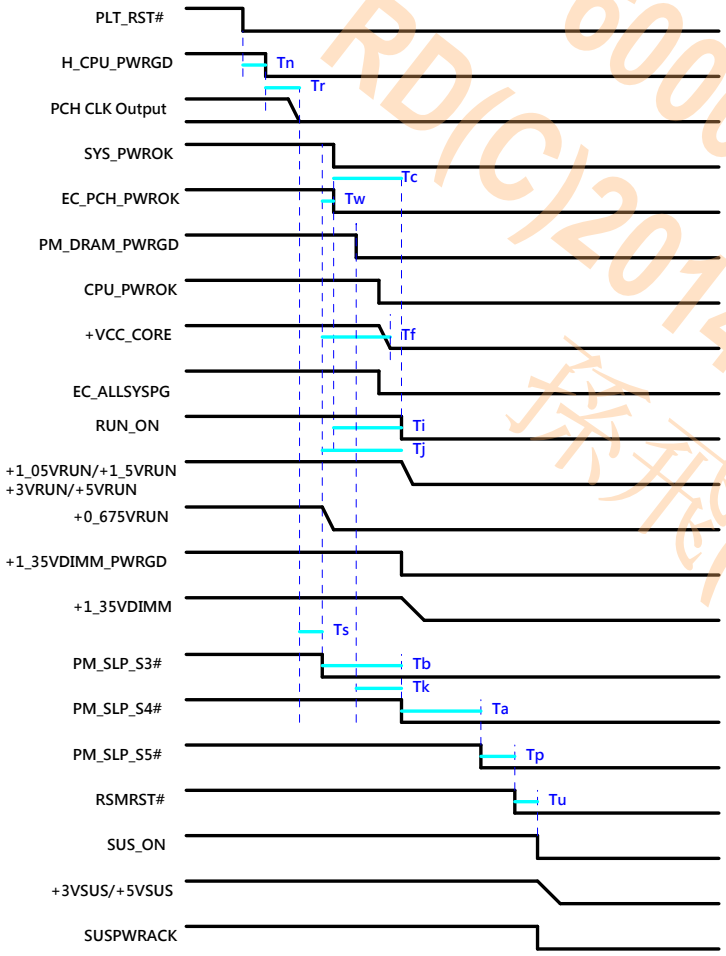


MICRO-STAR INT'L CO.,LTD.		
Title: Power on Sequence		
Size	Document Number: MS-16H3	Rev: 0B
Date: Tuesday, May 20, 2014	Sheet 62 of 69	

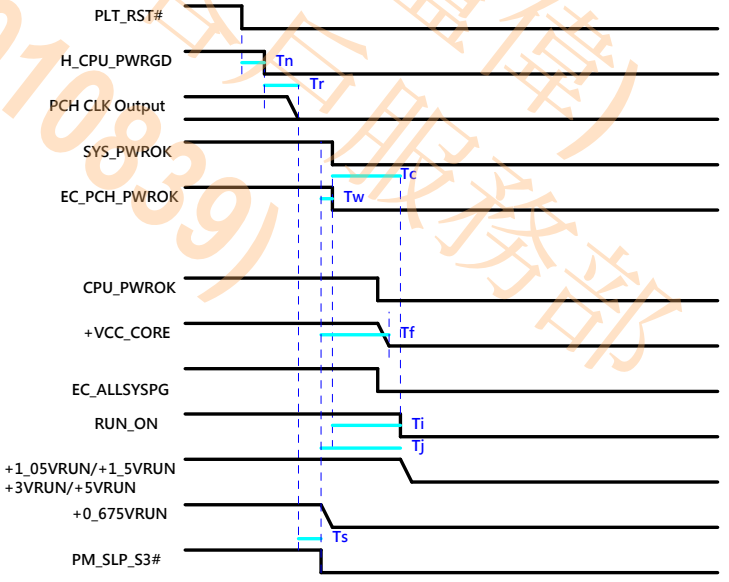
Power down Sequence

	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

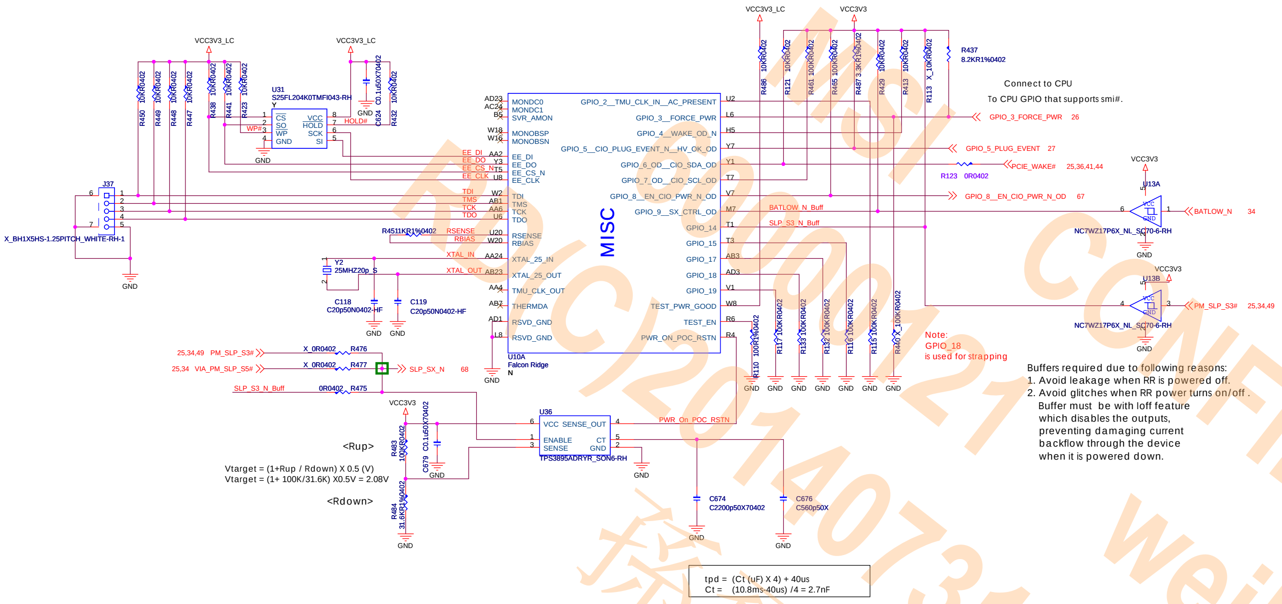
S0 -> G3



S0 -> S3



MICRO-STAR INT'L CO.,LTD.	
Title	Power down Sequence
Size	Document Number: MS-16H3
Rev	0B
Date:	Tuesday, May 20, 2014
Sheet	63 of 69



Buffers required due to following reasons:
1. Avoid leakage when RR is powered off.
2. Avoid glitches when RR power turns on/off .
Buffer must be with Ioff feature
which disables the outputs,
preventing damaging current
backflow through the device
when it is powered down.

Vtarget = (1+Rup / Rdown) X 0.5 (V)
Vtarget = (1+ 100K/31.6K) X0.5V = 2.08V

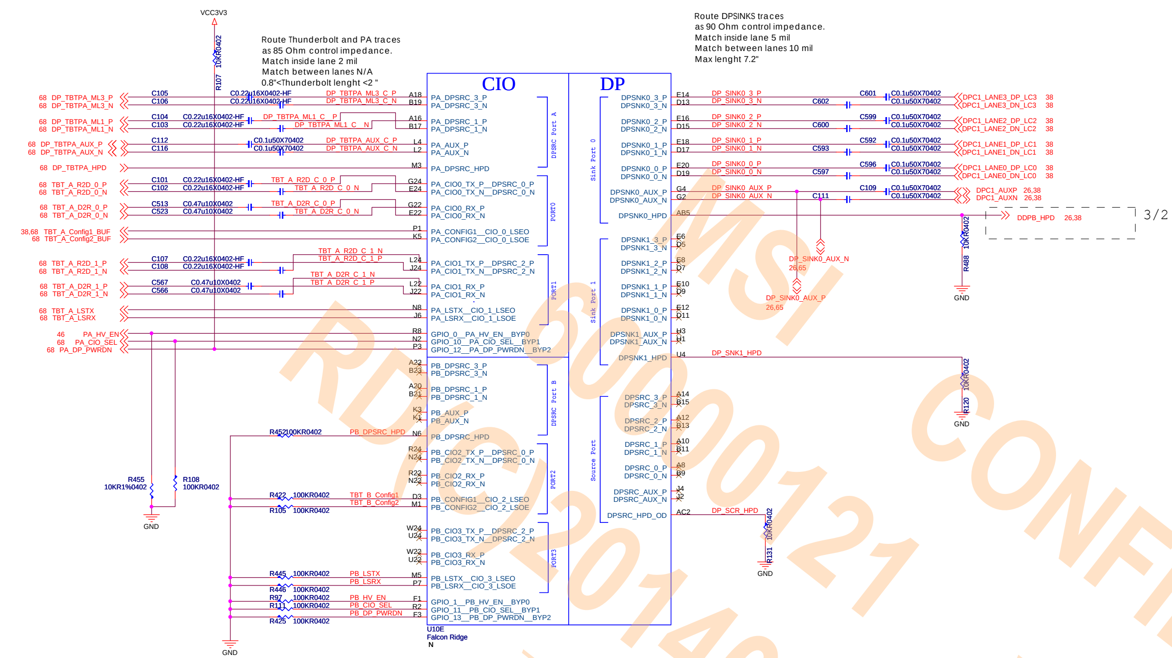
tpd = (Ct (uF) X 4) + 40us
Ct = (10.8ms-40us) /4 = 2.7nF

MICRO-STAR INT'L CO.,LTD.

Title: INTEL Falcon Ridge 5320(2C)

Size | Document Number: MS-16H3 | Rev: 0B

Date: Tuesday, May 20, 2014 | Sheet 64 of 69



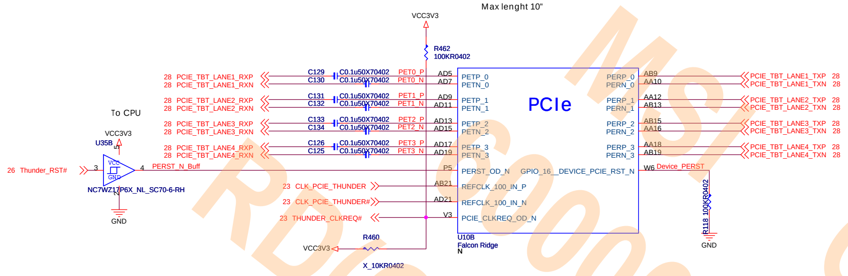
MICRO-STAR INT'L CO.,LTD.

Title
INTEL Falcon Ridge 5320(2C)

Size	Document Number	Rev
	MS-16H3	0B

Date: Tuesday, May 20, 2014 Sheet 65 of 69

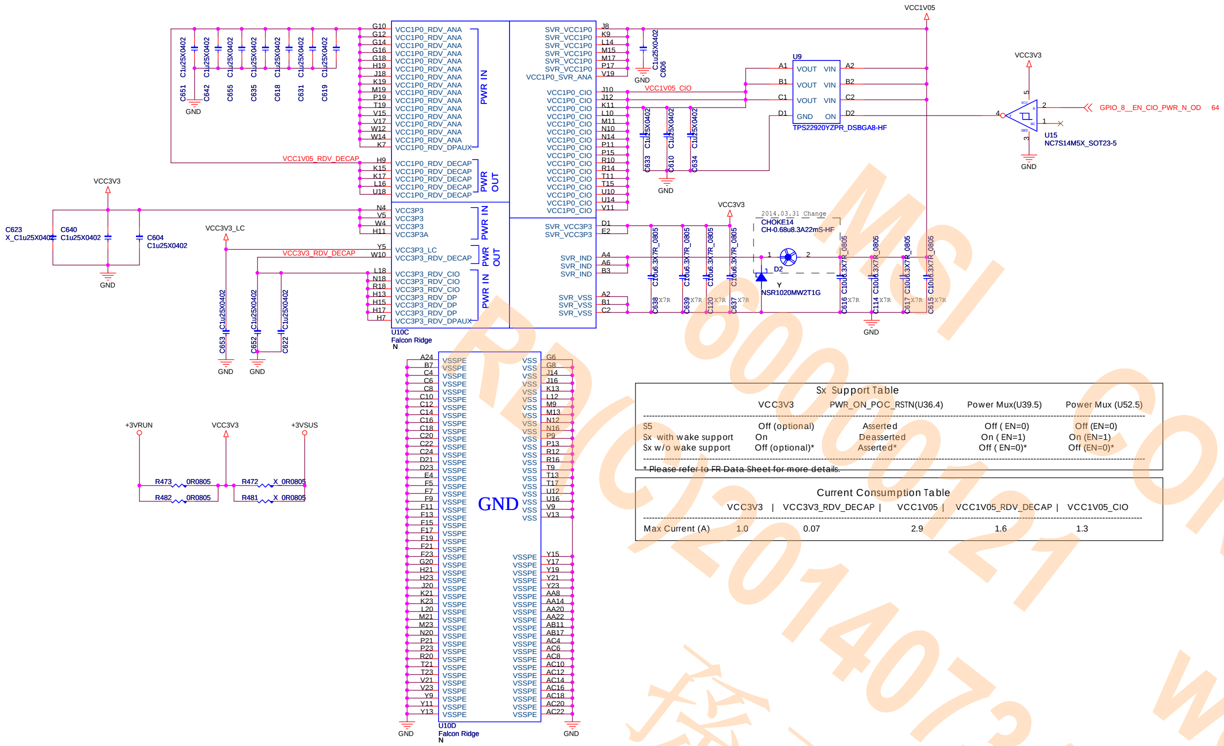
Route PCIe traces
as 85 Ohm control impedance
Match inside lanes 5mil
Match between lanes N/A
Max lenght 10"



Buffer required due to following reasons:
1. Avoid leakage when RR is powered off.
2. Avoid glitches when RR power turns on/off .
Buffer must be with Ioff feature
which disables the outputs,
preventing damaging current
backflow through the device
when it is powered down.

Intel Confidential

msi	MICRO-STAR INT'L CO.,LTD.
Title	INTEL Falcon Ridge 5320(2C)
Size / Document Number	MS-16H3
Rev	0B
Date:	Tuesday, May 20, 2014
Sheet	66 of 69



Sx Support Table

	VCC3V3	PWR_ON_POC_RSTN(U36.4)	Power Mux(U39.5)	Power Mux (U52.5)
S5	Off (optional)	Asserted	Off (EN=0)	Off (EN=0)
Sx with wake support	On	Deasserted	On (EN=1)	On (EN=1)
Sx w/o wake support	Off (optional)*	Asserted*	Off (EN=0)*	Off (EN=0)*

* Please refer to FR Data Sheet for more details.

Current Consumption Table

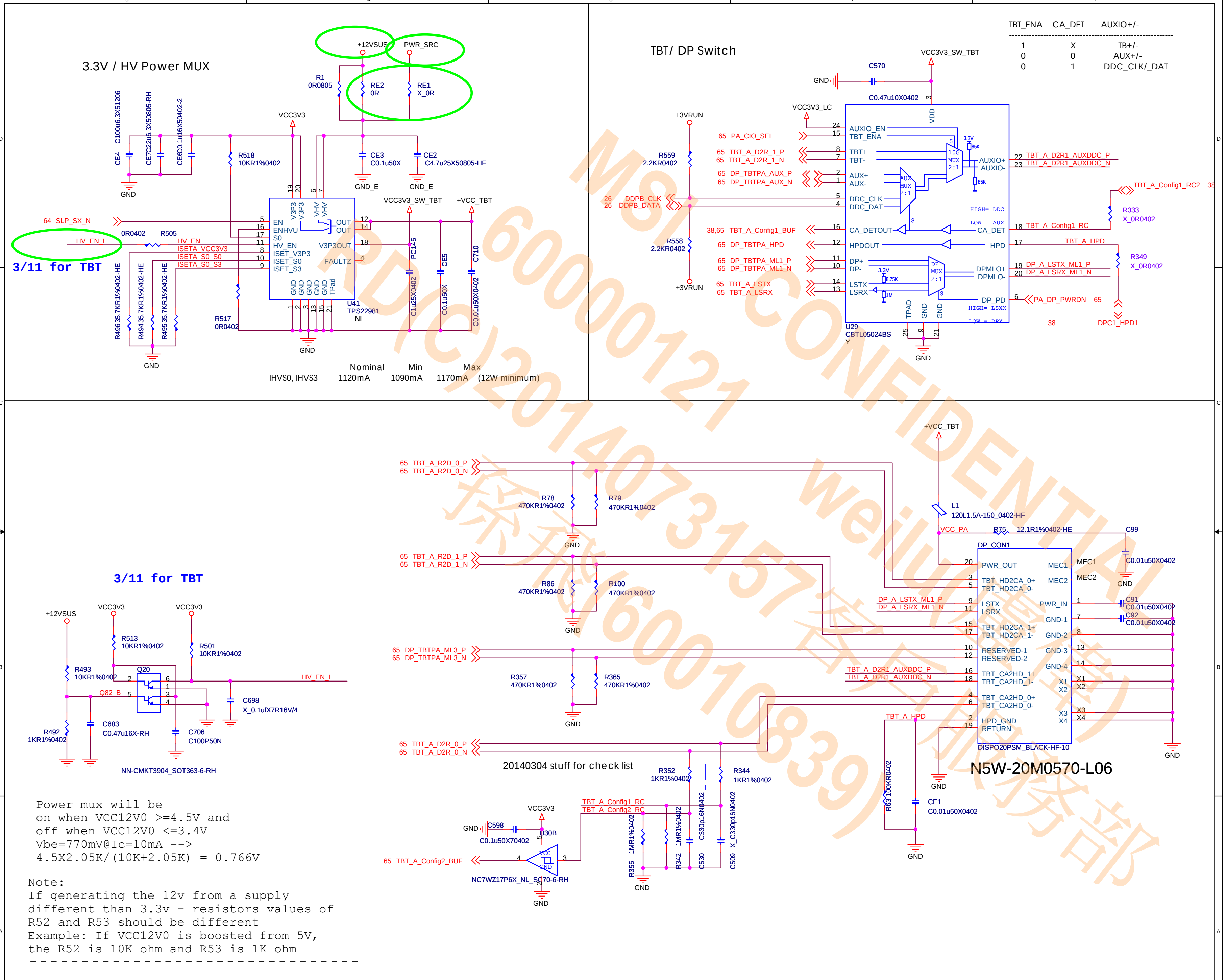
	VCC3V3	VCC3V3_RDV_DECAP	VCC1V05	VCC1V05_RDV_DECAP	VCC1V05_CIO
Max Current (A)	1.0	0.07	2.9	1.6	1.3

MICRO-STAR INT'L CO.,LTD.

Title: INTEL Falcon Ridge 5320(2C)

Size | Document Number: MS-16H3 | Rev: 0B

Date: Tuesday, May 20, 2014 | Sheet 67 of 69



MICRO-STAR INT'L CO.,LTD.	
Title	INTEL Falcon Ridge 5320(2C)
Size / Document Number	MS-16H3
Rev	0B
Date:	Tuesday, May 20, 2014
Sheet	68 of 69

History

0B: Hardware part

01. Remove All GAP for power parts.
02. Add 3V3_NV part for leakage
03. Change cardreader PN.
04. Change BTB PN
05. Change SPDIF/ Audio Jack PN
06. R116 unstuff, R117 stuff.
07. R346 unstuff
08. Remove SUBWOOFER
09. Add one more AMP for SPK

0B: Power part

01. PR33 2.2Kohm R11-0222T12-W08
02. PC29 82pF/50V C11-8201012-W08
03. PC30 100pF/16V C11-1011032-W08
04. PR34 unstuff
05. PC32 unstuff
06. PR27 2.7Kohm R11-0272T12-W08
07. PR90 8.06Kohm R11-8061T12-W08
08. PR32 910Rohm R11-0911T12-W08
09. PC27 560pF/16V C11-5611812-W08
10. PR31 80.6Kohm R11-8062T12-W08
11. PR23 21Kohm R11-0213T12-W08
12. PR88 6.8Mohm R11-0685T13-W08
13. PR8 453Rohm R11-4530T22-W08
14. PC19 unstuff
15. PR6 unstuff
16. PR140 100Kohm R11-0104T12-W08
17. PR145 93.1Kohm R11-9312T12-R01
18. PR143 15Kohm R11-0153T12-W08
19. PR124 95.3Kohm R11-9532T12-W08
20. PR86 28.7Kohm R11-2872T12-W08
21. PC69, PC70 change to 1206 package
22. PR88 6.8Mohm R11-0685T13-W08

msi	MICRO-STAR INT'L CO.,LTD.
Title	History
Size / Document Number	MS-16H3
Rev	0B
Date:	Tuesday, May 20, 2014
Sheet	69 of 69