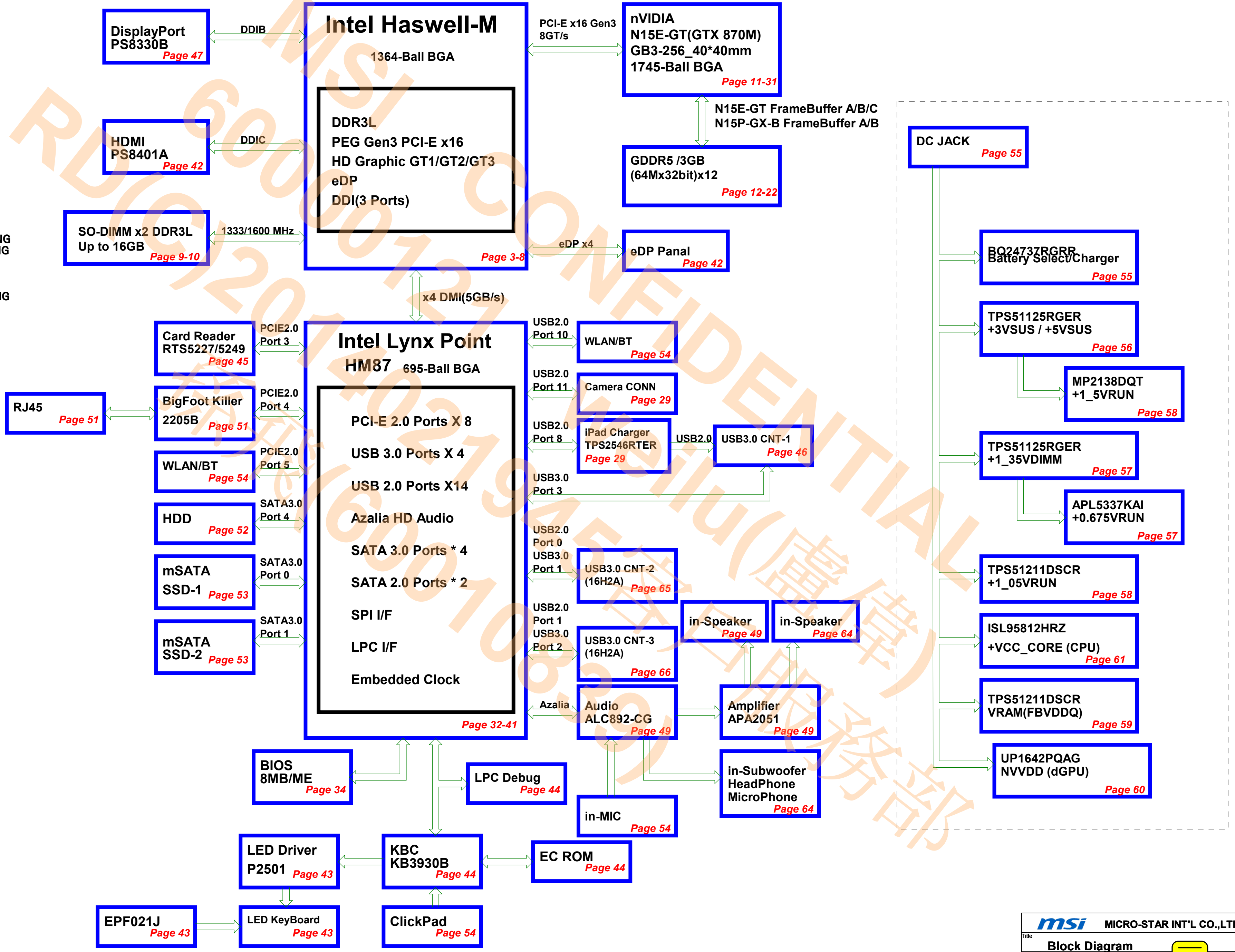
MS-16H2 Ver:1.1

Shark Bay Mobile

Thursday, February 13, 2014



MICRO-STAR INT'L CO.,LTD.

Title: Block Diagram

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	DIMM_ON
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUN_ON
+VCC_CORE	1.8V Core Voltage for Processor	EC_ALLSYSPG
+1_05VRUN	1.05V rail for Processor	RUN_ON
NVVDD	V Core Voltage for nVIDIA dGPU	NVVDD_EN
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	FBVDDQ_ON
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	NVVDD_EN

Net Naming Conventions

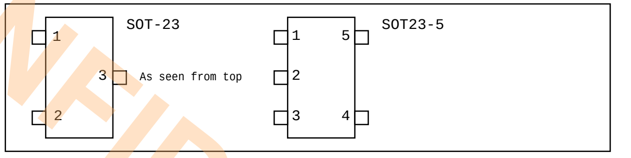
Suffix

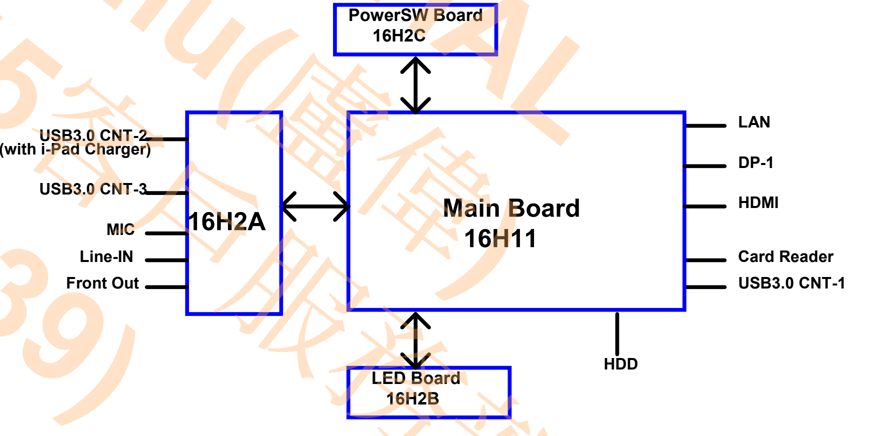
```
#  =  Active Low Signal
```

Prefix

```
H  =  Host
M  =  DDR Memory
TP =  Test Point (does not connect anywhere else)
FB = DGPU VRAM
VIAxxx =  Like Test Point, but using VIA.
```

PCB Footprints





POWER STATES

SIGNAL / STATE	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on and +V*SUS always keep high

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Title	Platform
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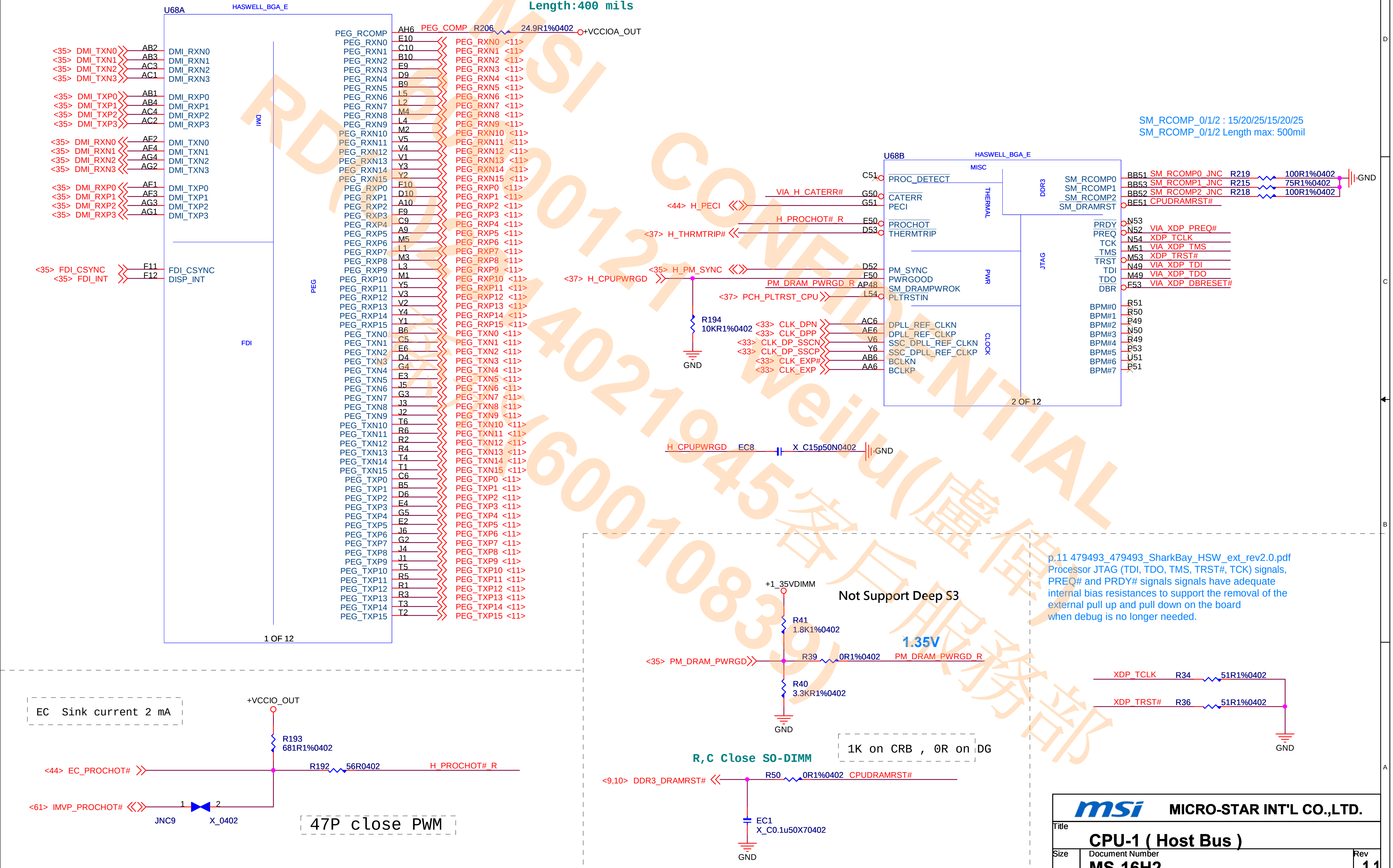
Haswell (DMI,PEG,FDI)

Haswell (CLK,MISC,JTAG)

PEG_RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils

SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil



p.11 479493_479493_SharkBay_HSW_ext_rev2.0.pdf
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals,
PREQ# and PRDY# signals signals have adequate
internal bias resistances to support the removal of the
external pull up and pull down on the board
when debug is no longer needed.

EC Sink current 2 mA

47P close PWM

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Title	CPU-1 (Host Bus)
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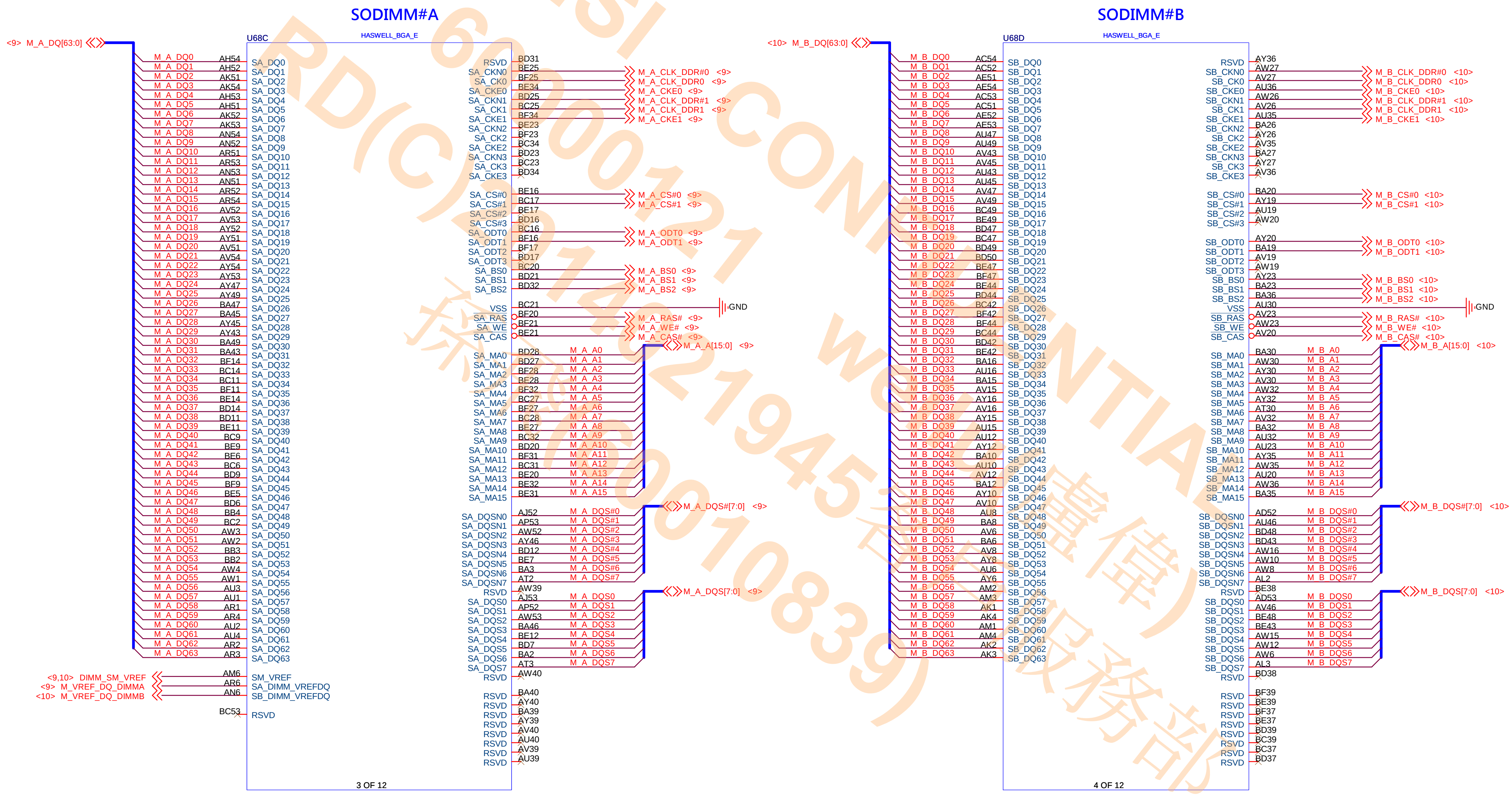
Haswell (DDR3L)



MICRO-STAR INT'L CO.,LTD.

Title	CPU-2 (DDR3L)	
Size	Document Number: MS-16H2	Rev 1.1
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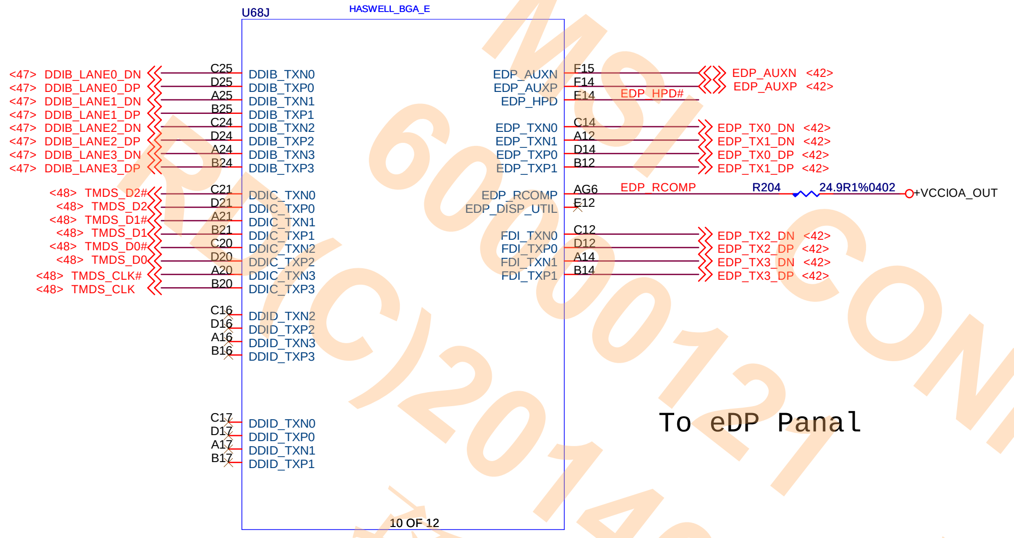
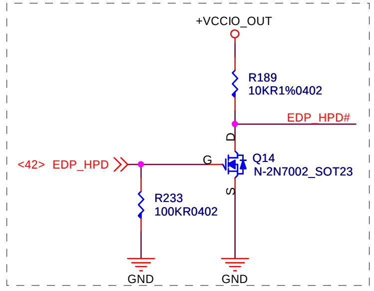
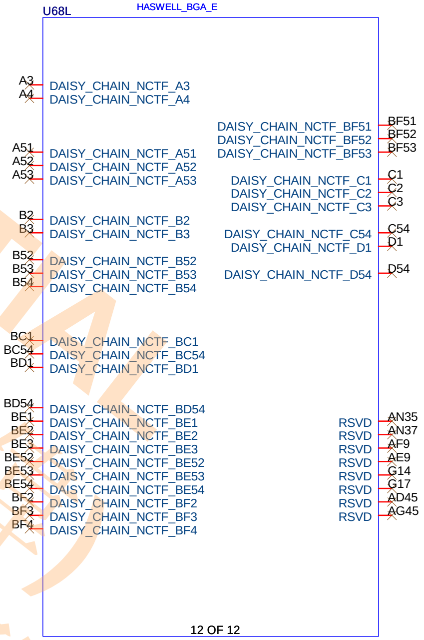
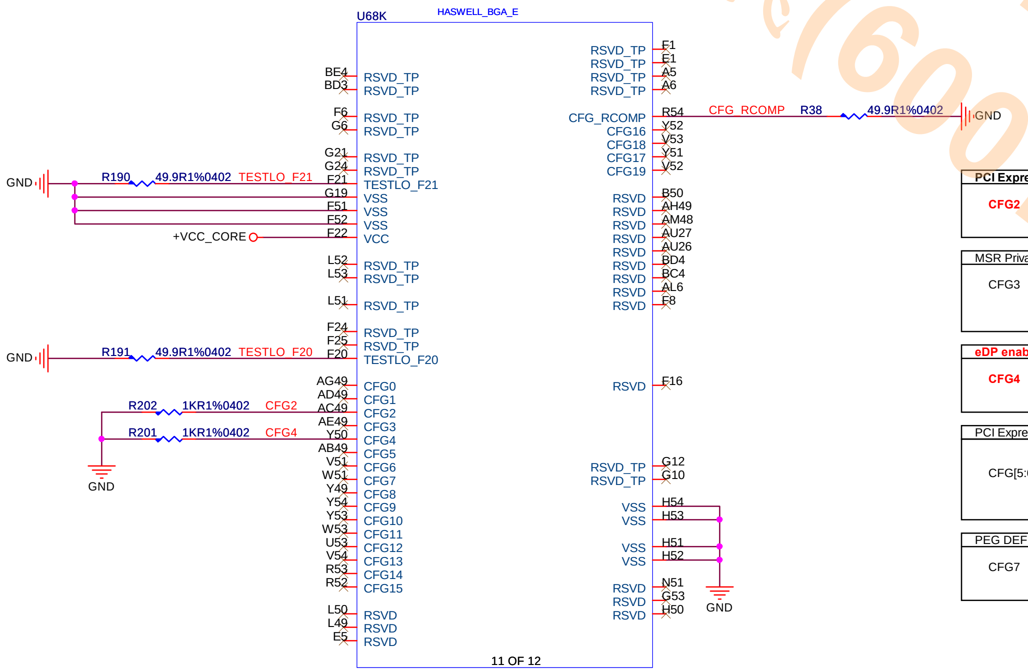
Display/Reserved









PCI Express* Static x16 Lane Numbering Reversal

CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature

CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable

CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation

CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

msi MICRO-STAR INT'L CO.,LTD.

Title: CPU-3 (Display/Reserved)

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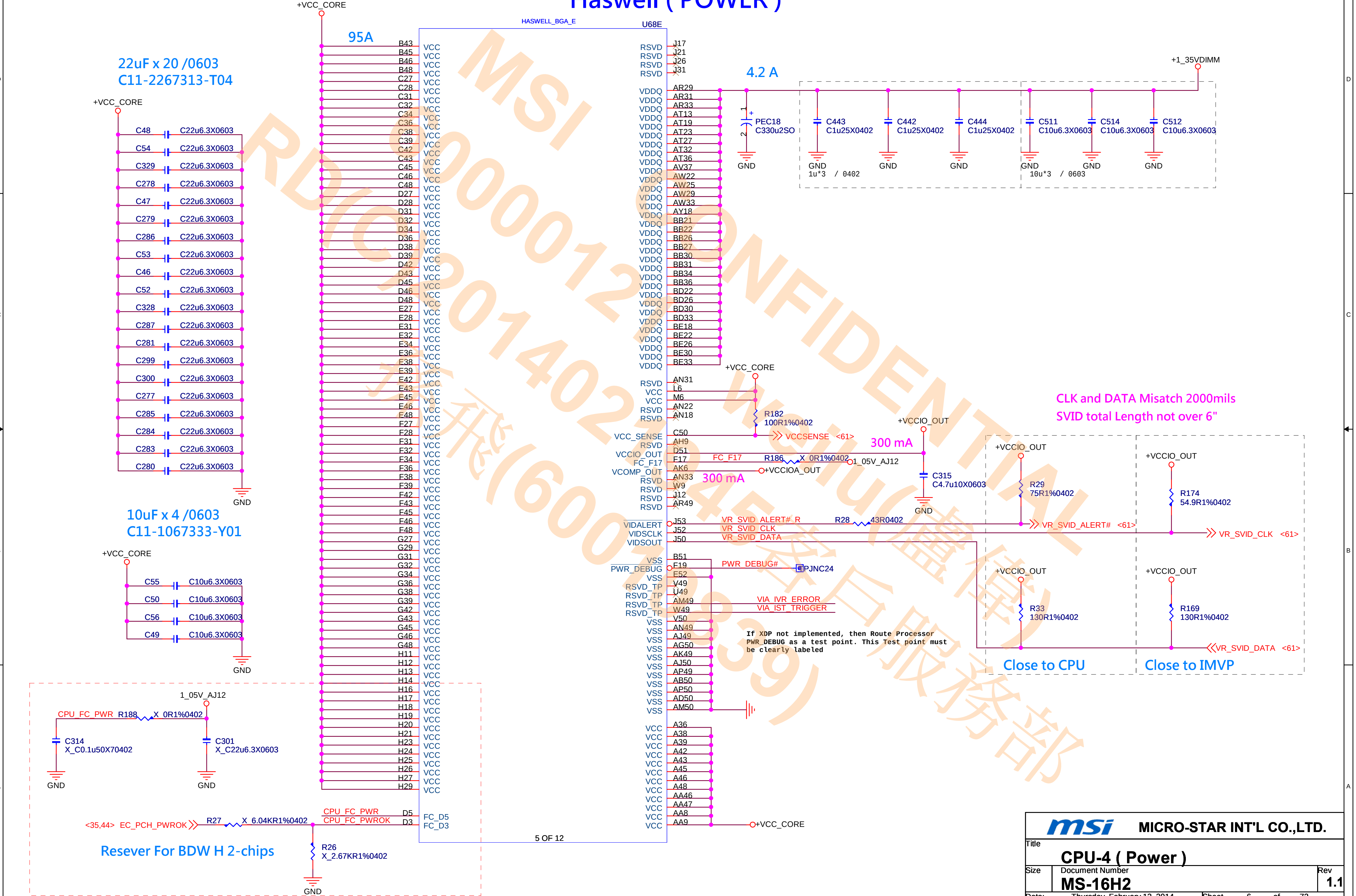
Haswell (POWER)



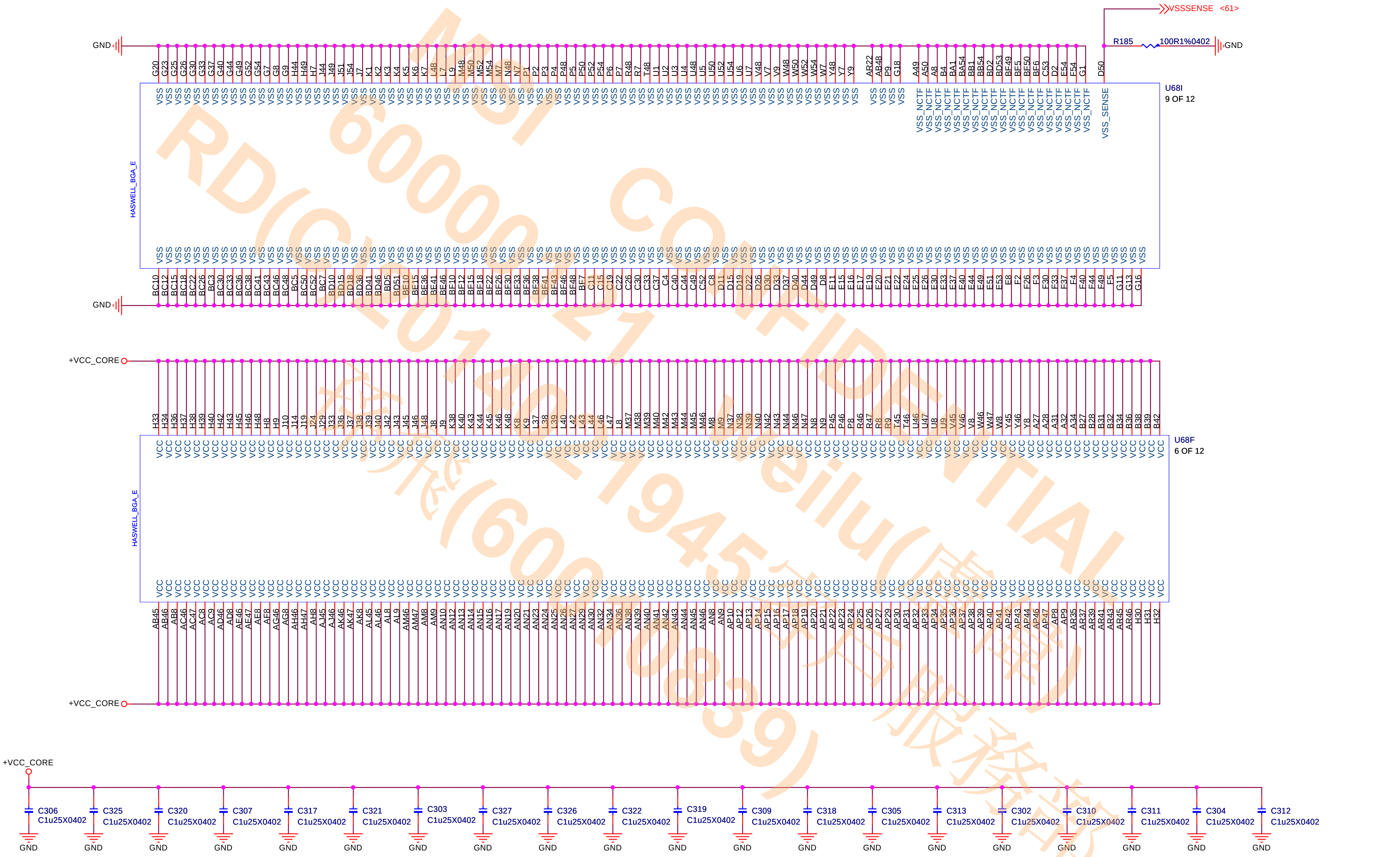
MICRO-STAR INT'L CO.,LTD.

Title: CPU-4 (Power)

Size | Document Number: MS-16H2 | Rev 1.1

Date: Thursday, February 13, 2014 | Sheet 6 of 72

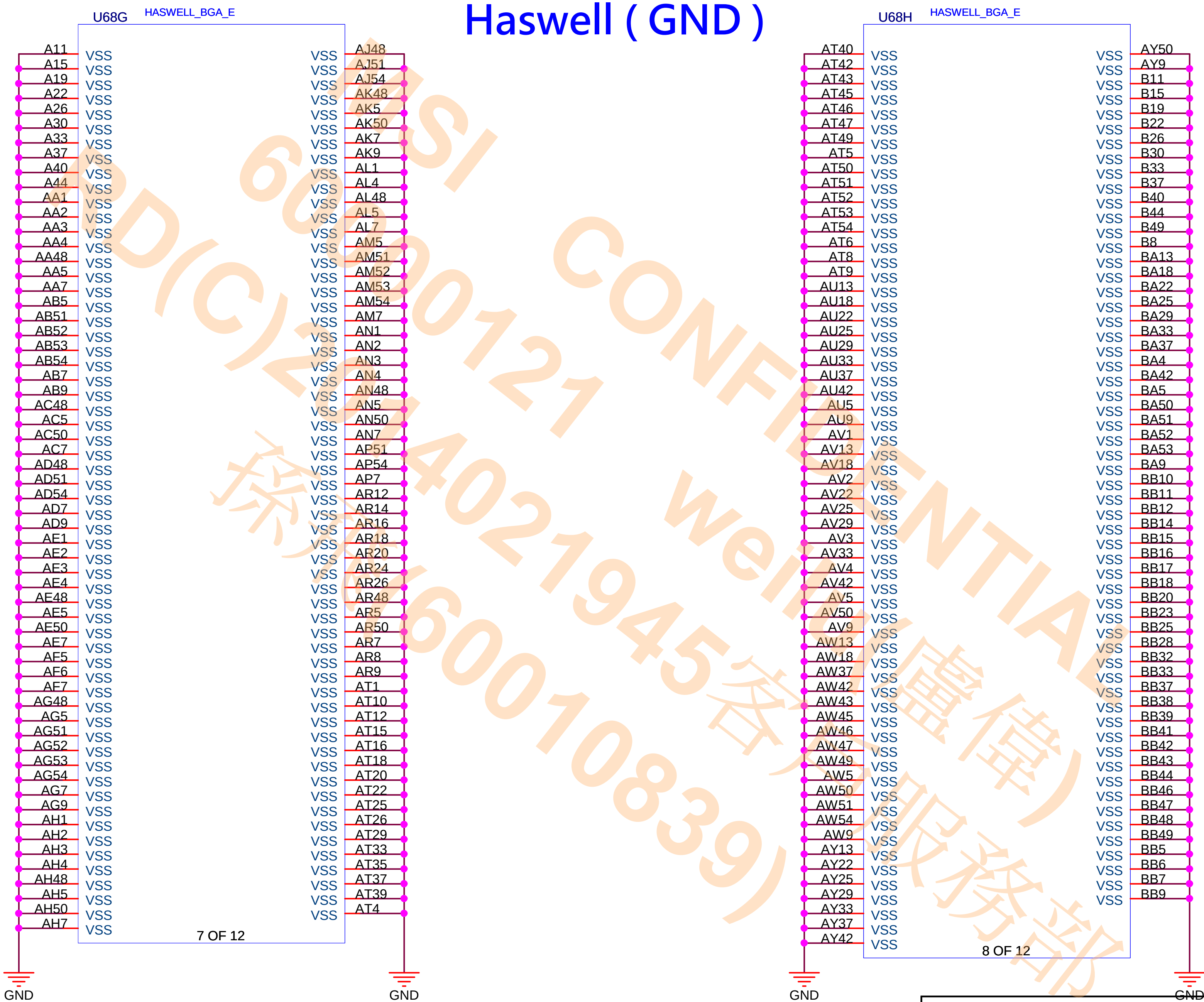
Haswell (Power & GND)



MICRO-STAR INT'L CO.,LTD.

Title	CPU-6 (Power & GND)	
Size	Document Number: MS-16H2	Rev 1.1
Date: Thursday, February 13, 2014	Sheet 7 of 72	

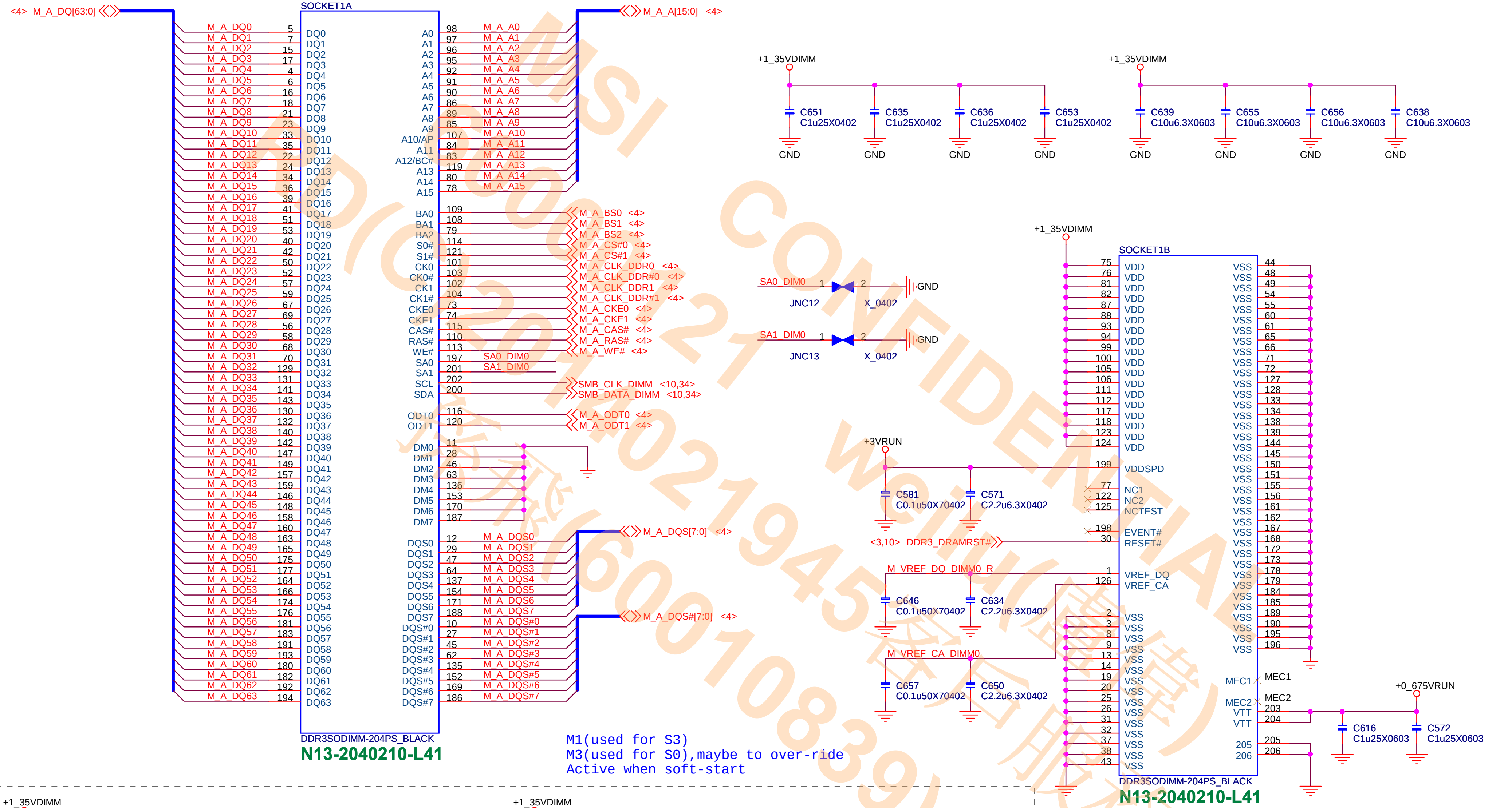
Haswell (GND)



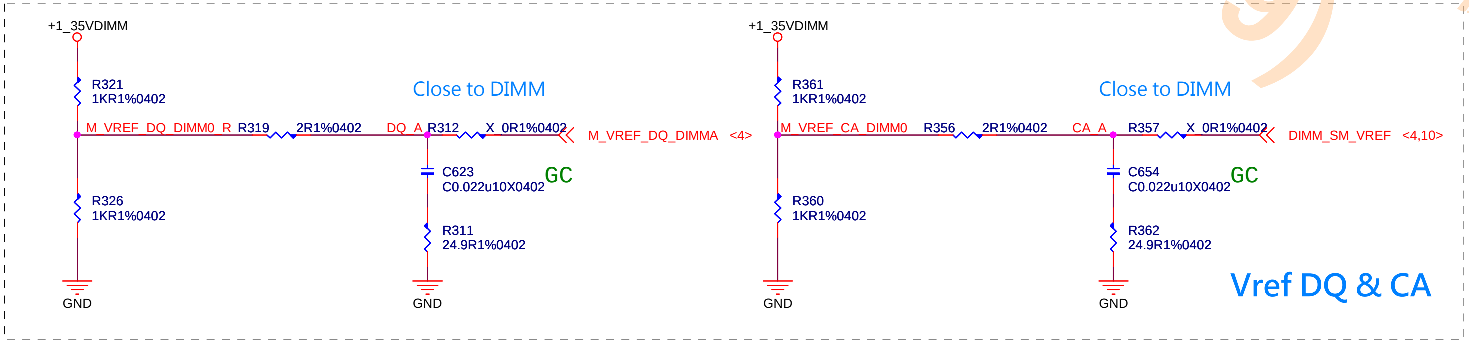
MICRO-STAR INT'L CO.,LTD.

Title	CPU-5 (GND)	
Size	Document Number MS-16H2	Rev 1.1
Date: Thursday, February 13, 2014	Sheet 8 of 72	

SODIMM#A



M1(used for S3)
M3(used for S0),maybe to over-ride
Active when soft-start



MICRO-STAR INT'L CO.,LTD.

Title	DDR3L SODIMM 0
Size / Document Number	MS-16H2
Rev	1.1
Date:	Thursday, February 13, 2014
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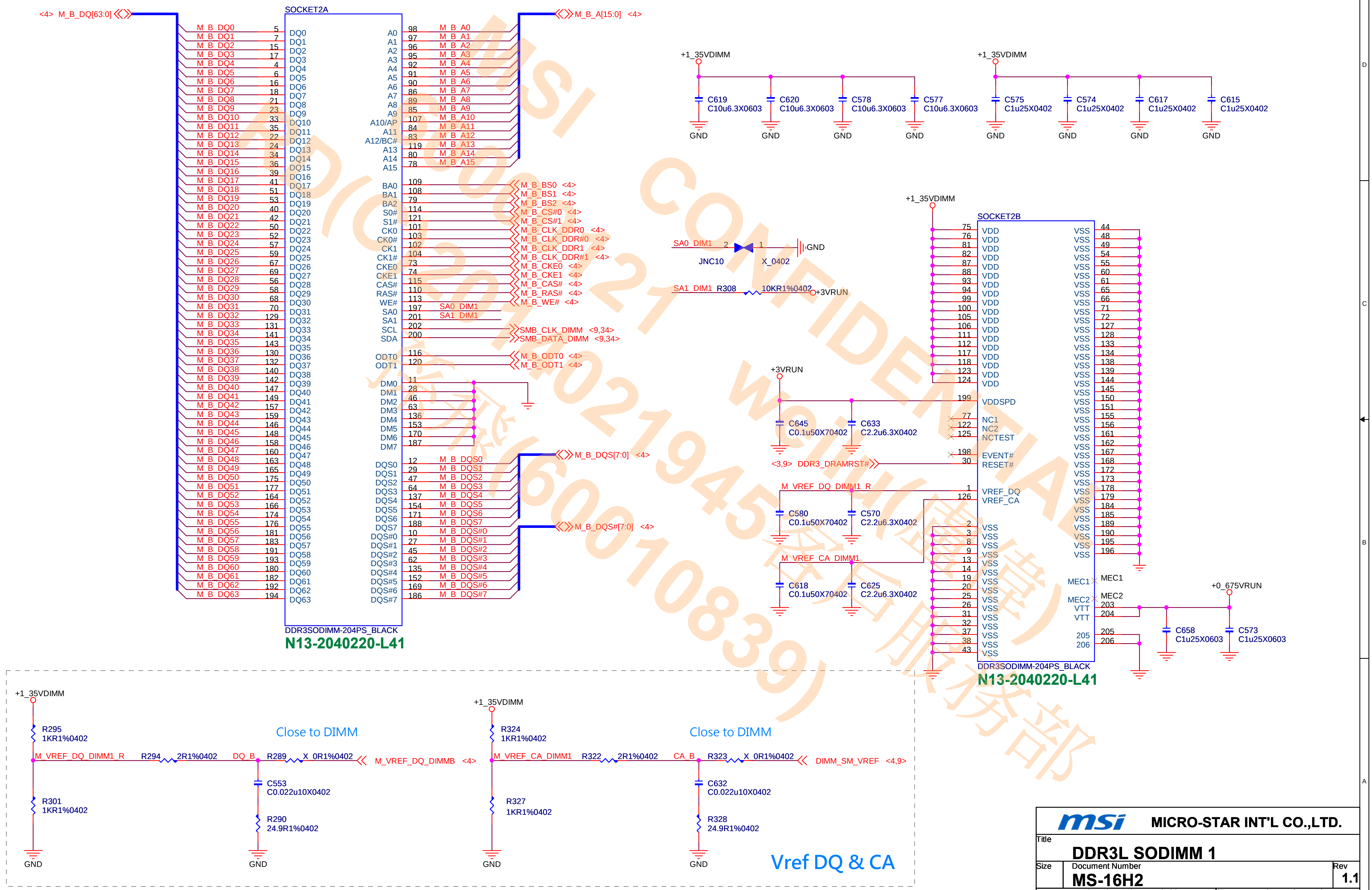
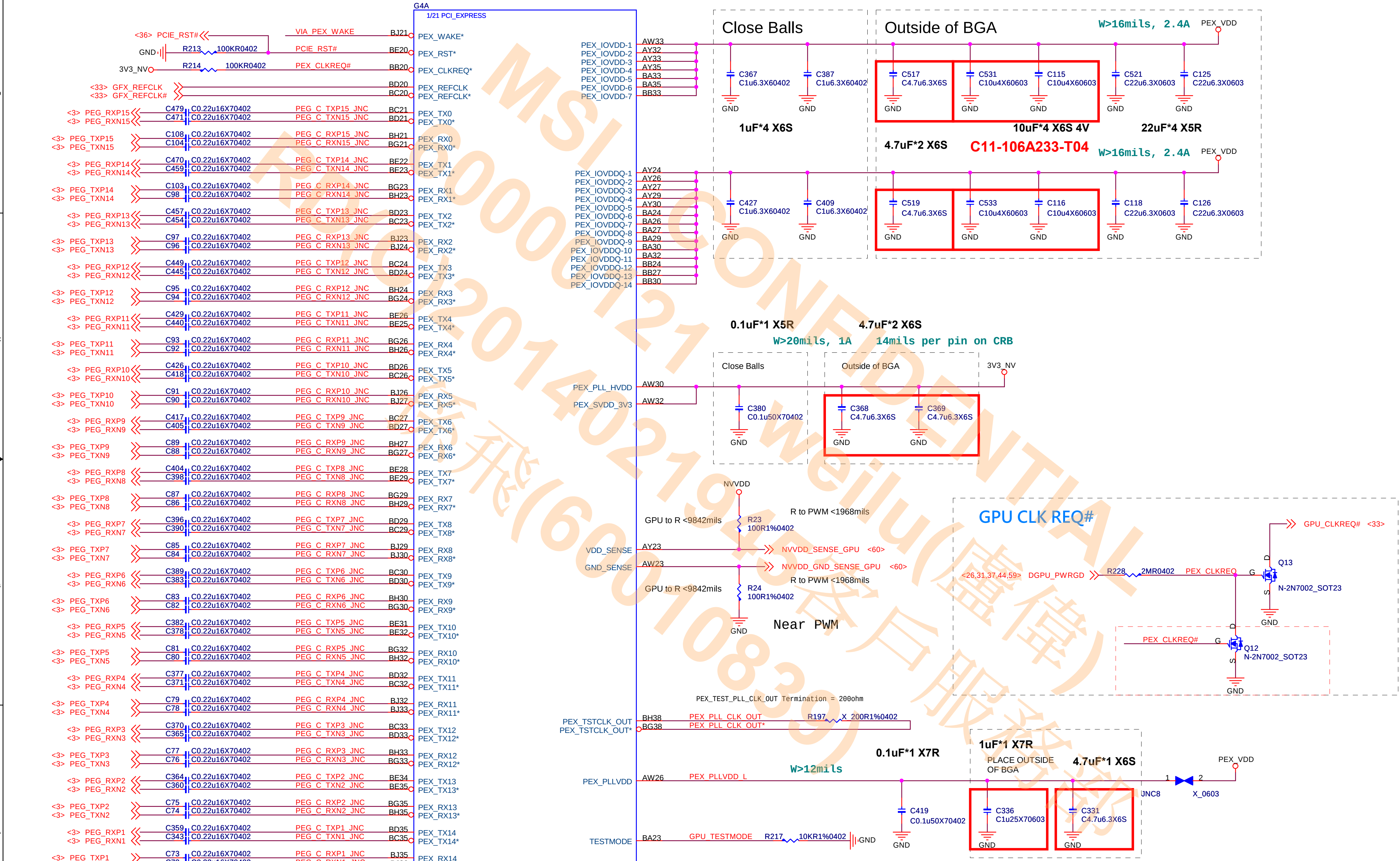
SODIMM#B



msi	MICRO-STAR INT'L CO.,LTD.	
Title	DDR3L SODIMM 1	
Size	Document Number MS-16H2	Rev 1.1
Date: Thursday, February 13, 2014	Sheet 10 of 72	

GPU PCI EXPRESS



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_PCI-E Host
Size / Document Number	MS-16H2
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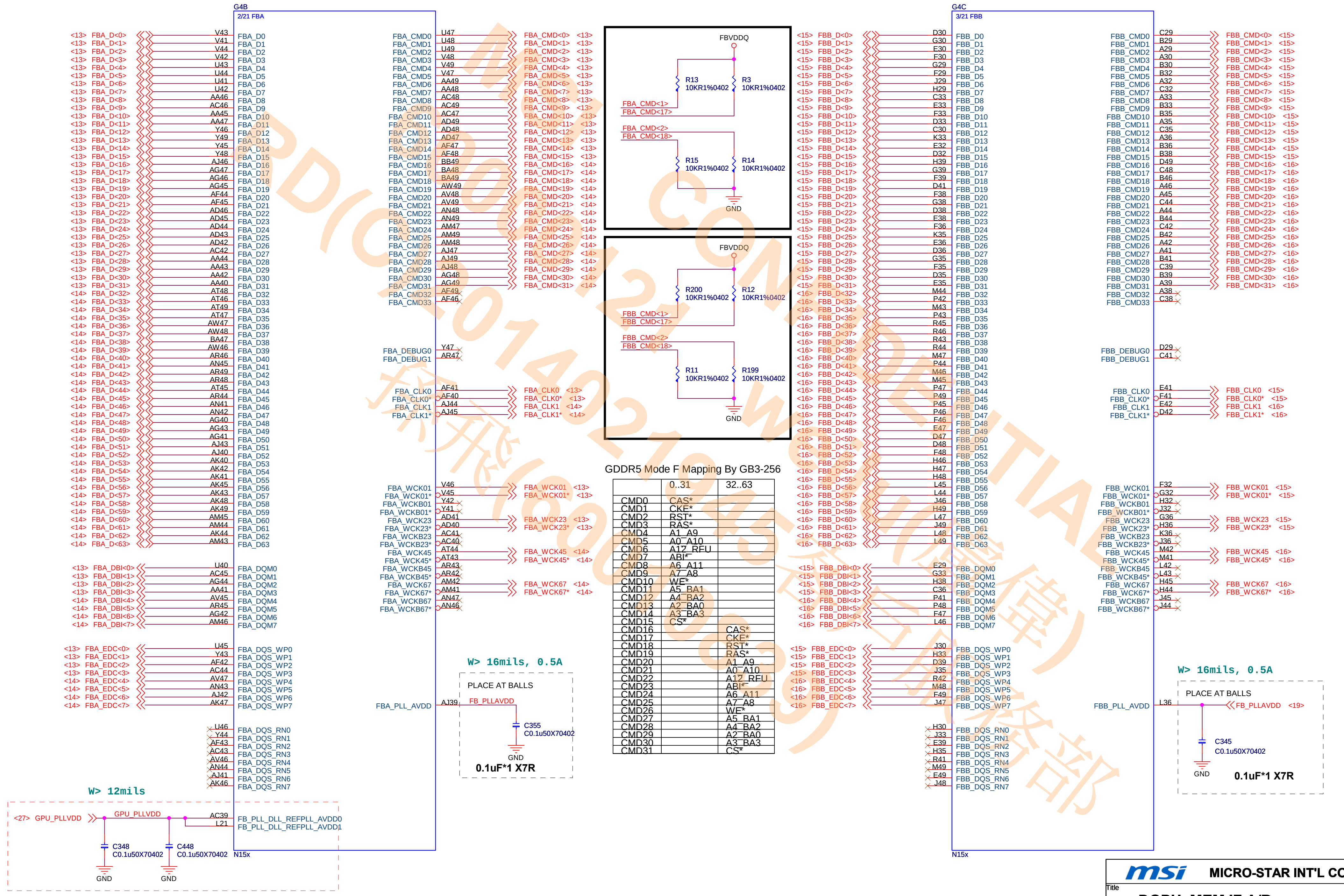
GPU Frame Buffer Partition A/B



GDDR5 Mode F Mapping By GB3-256

	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_MEM IF A/B

Size | Document Number: MS-16H2 | Rev 1.1

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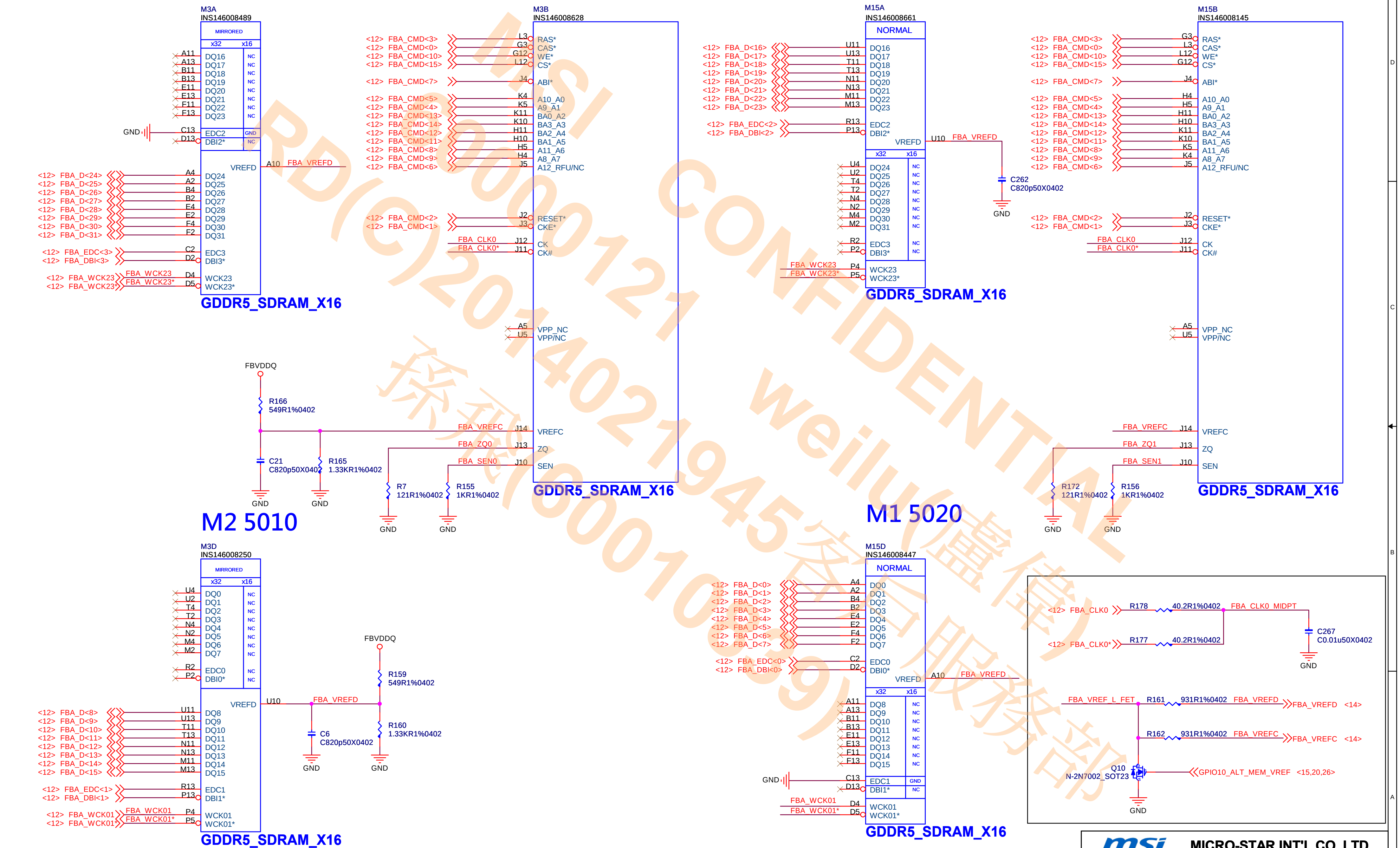
DGPU_GDDR5 FrameBuffer A0



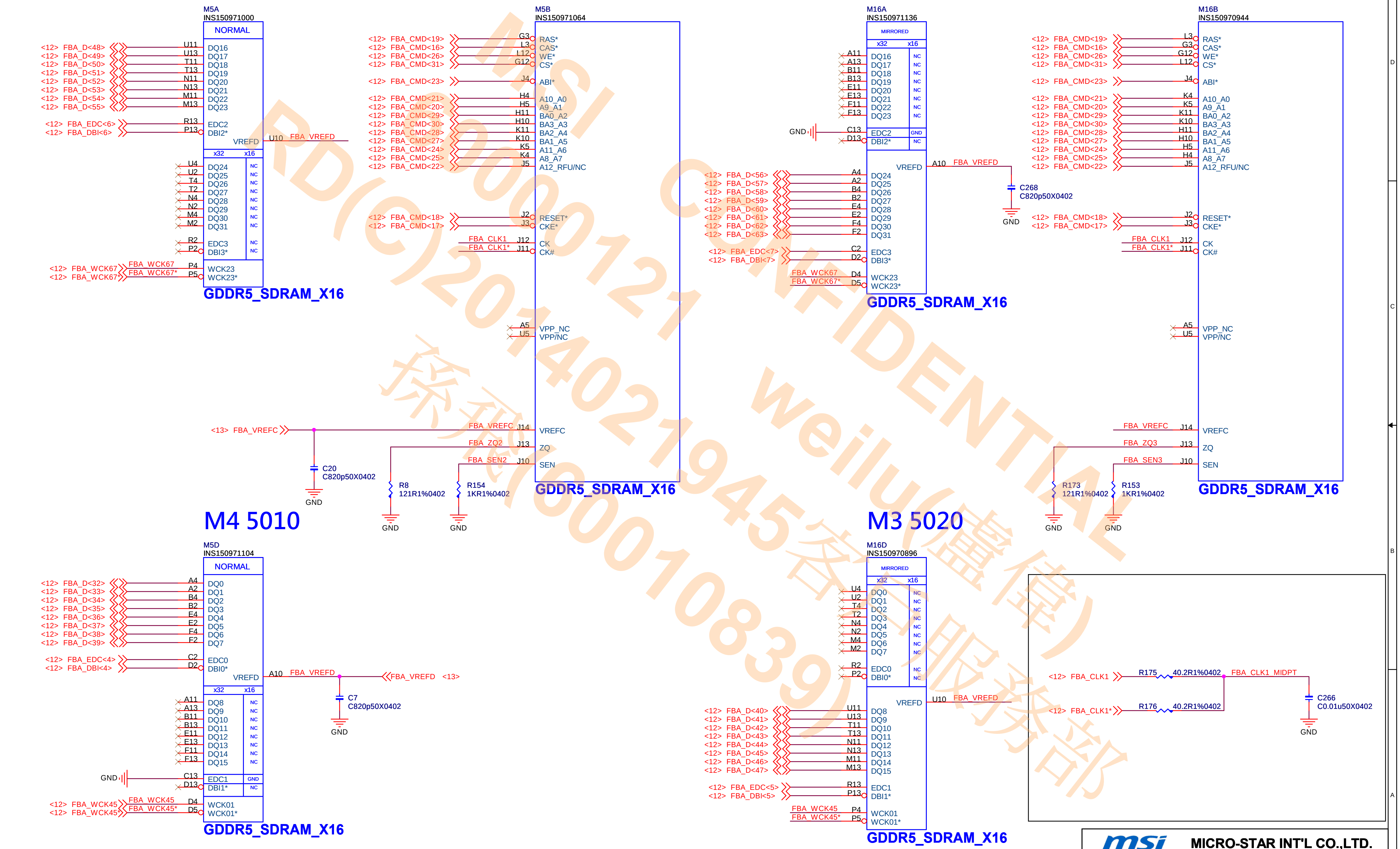
MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FrameBuffer A0

Size | Document Number: MS-16H2 | Rev: 1.1

Date: Thursday, February 13, 2014 | Sheet 13 of 72

DGPU_GDDR5 FrameBuffer A1



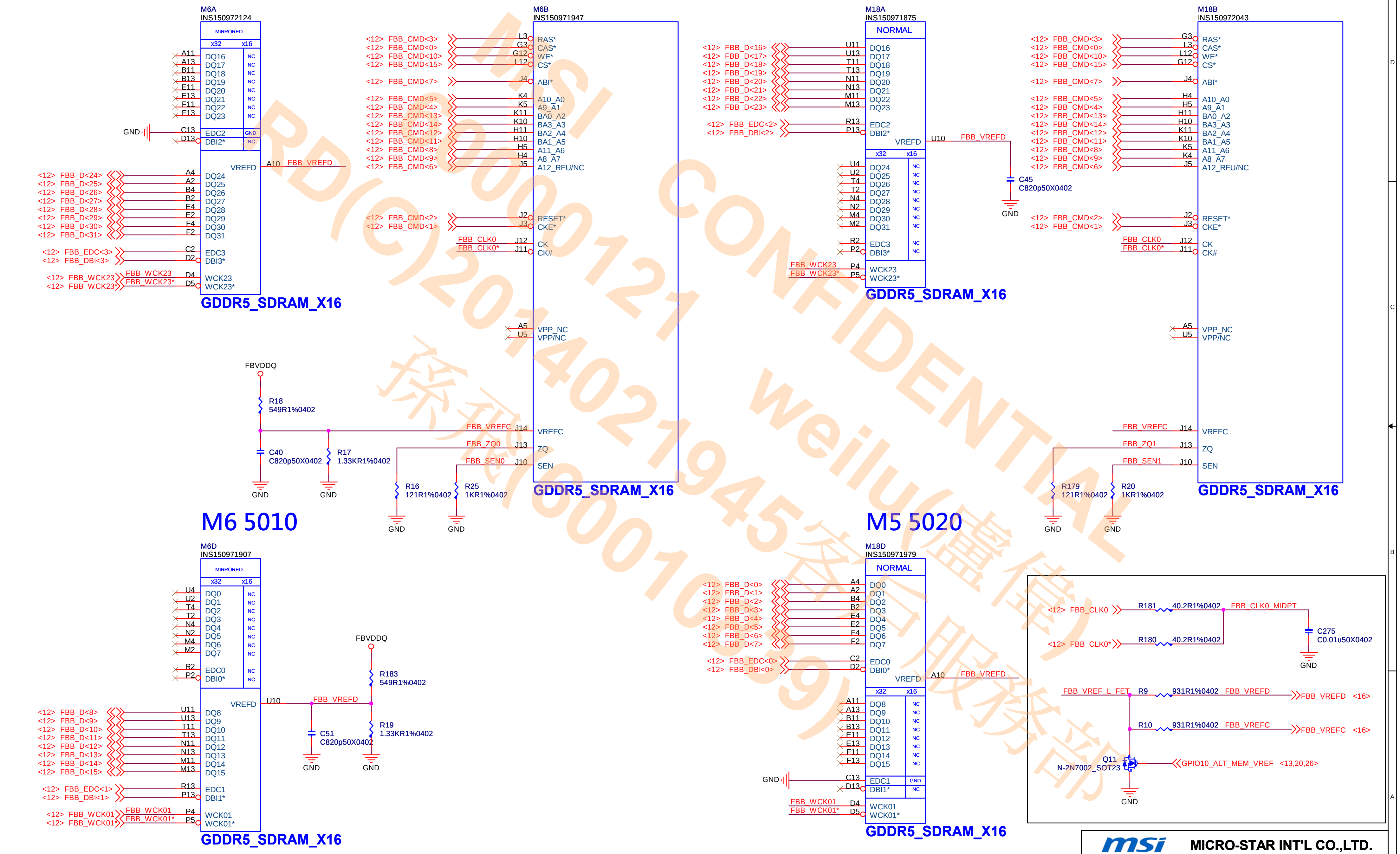
msi MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FrameBuffer A1

Size | Document Number: MS-16H2 | Rev 1.1

Date: Thursday, February 13, 2014 | Sheet 14 of 72

DGPU_GDDR5 FrameBuffer B0



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer B0
Size	Document Number: MS-16H2
Rev	1.1
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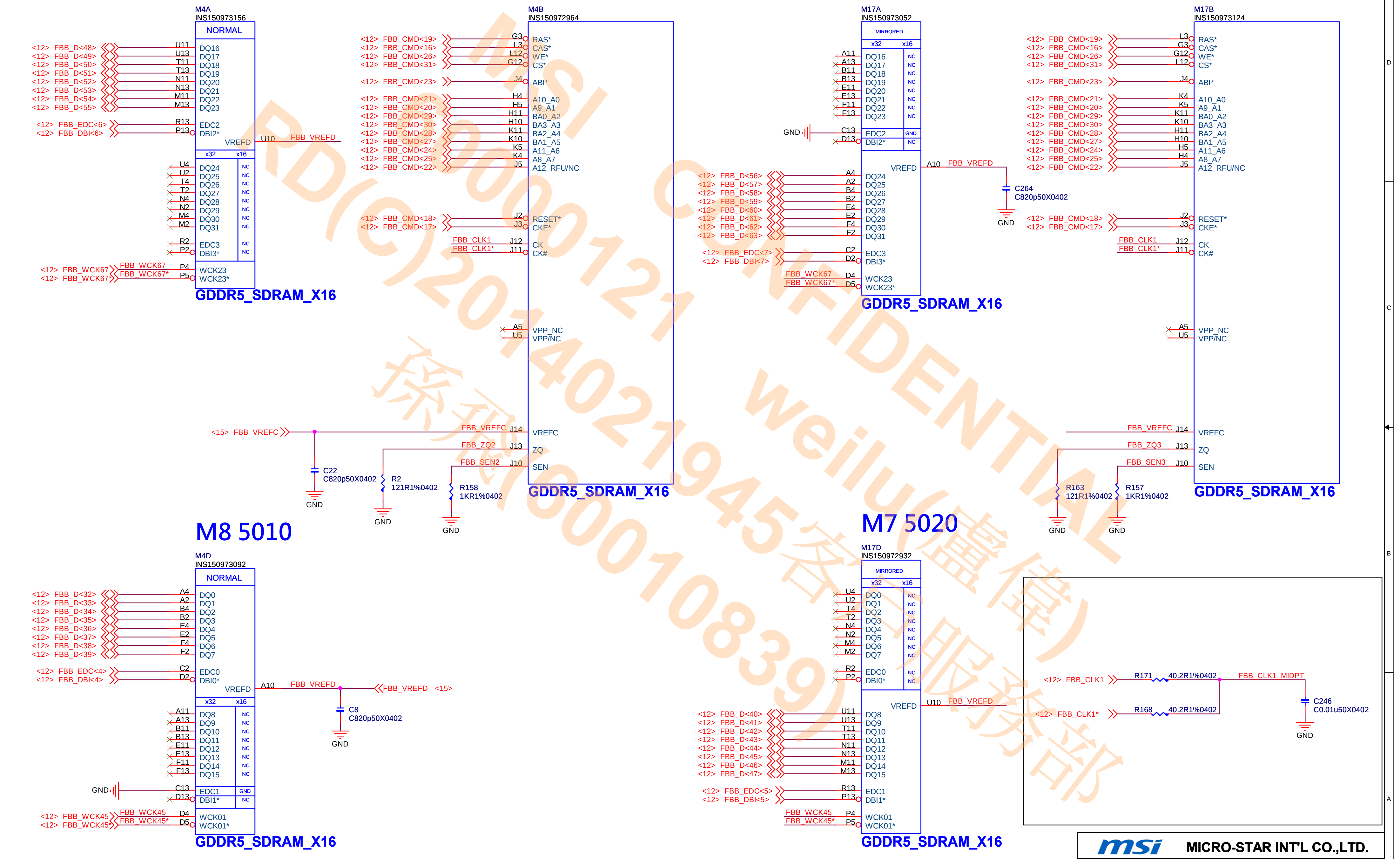
DGPU_GDDR5 FrameBuffer B1



MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FrameBuffer B1

Size | Document Number: MS-16H2 | Rev: 1.1

Date: Thursday, February 13, 2014 | Sheet 16 of 72

Frame Buffer Partition A Decoupling

MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FB-A_DECOUPLING	
Size	Document Number MS-16H2	Rev 1.1
Date: Thursday, February 13, 2014	Sheet 17 of 72	

Frame Buffer Partition B Decoupling

MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FB-B_DECOUPLING
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Date	Thursday, February 13, 2014
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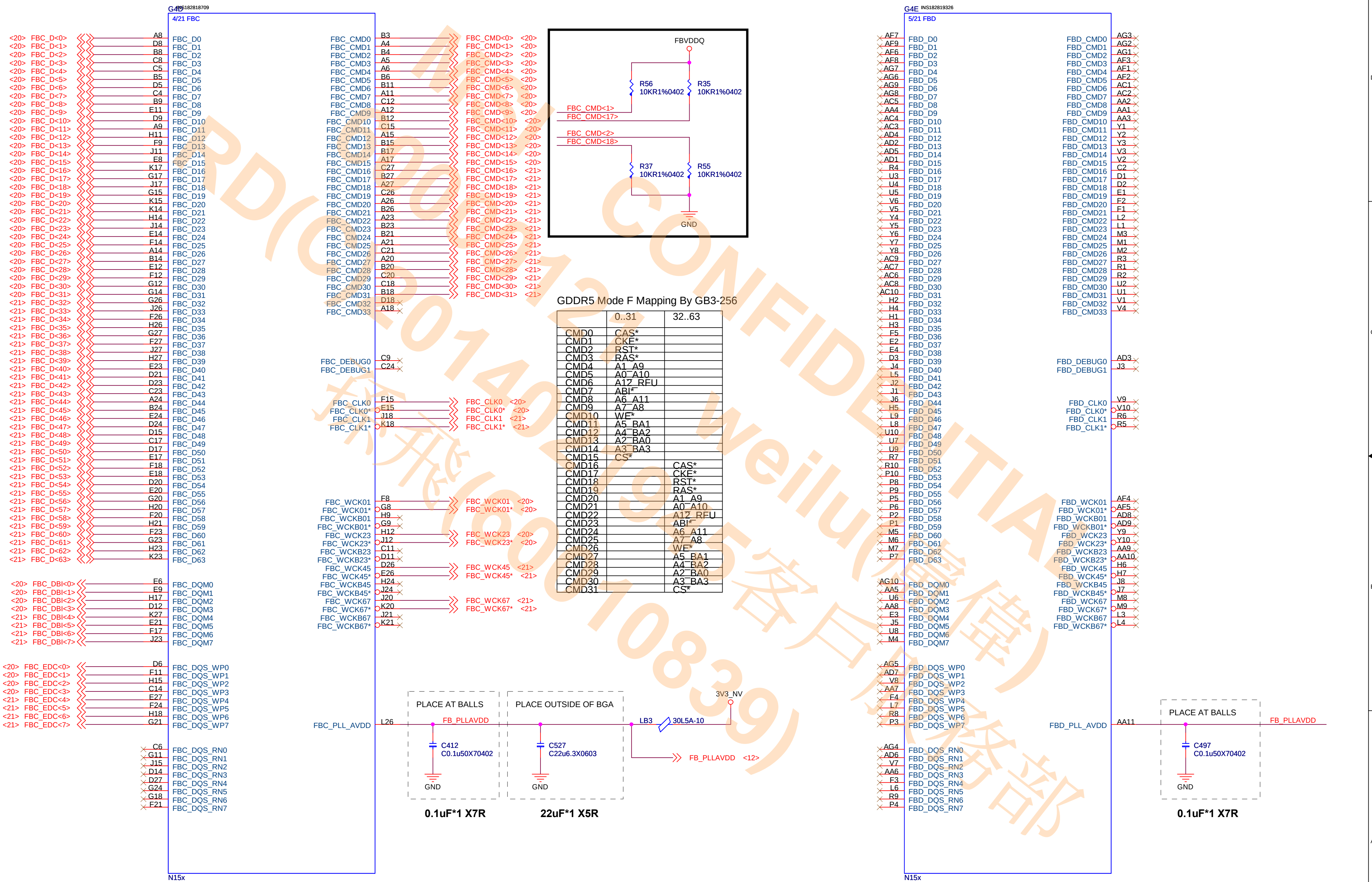
GPU Frame Buffer Partition C/D



GDDR5 Mode F Mapping By GB3-256

	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

MICRO-STAR INT'L CO.,LTD.

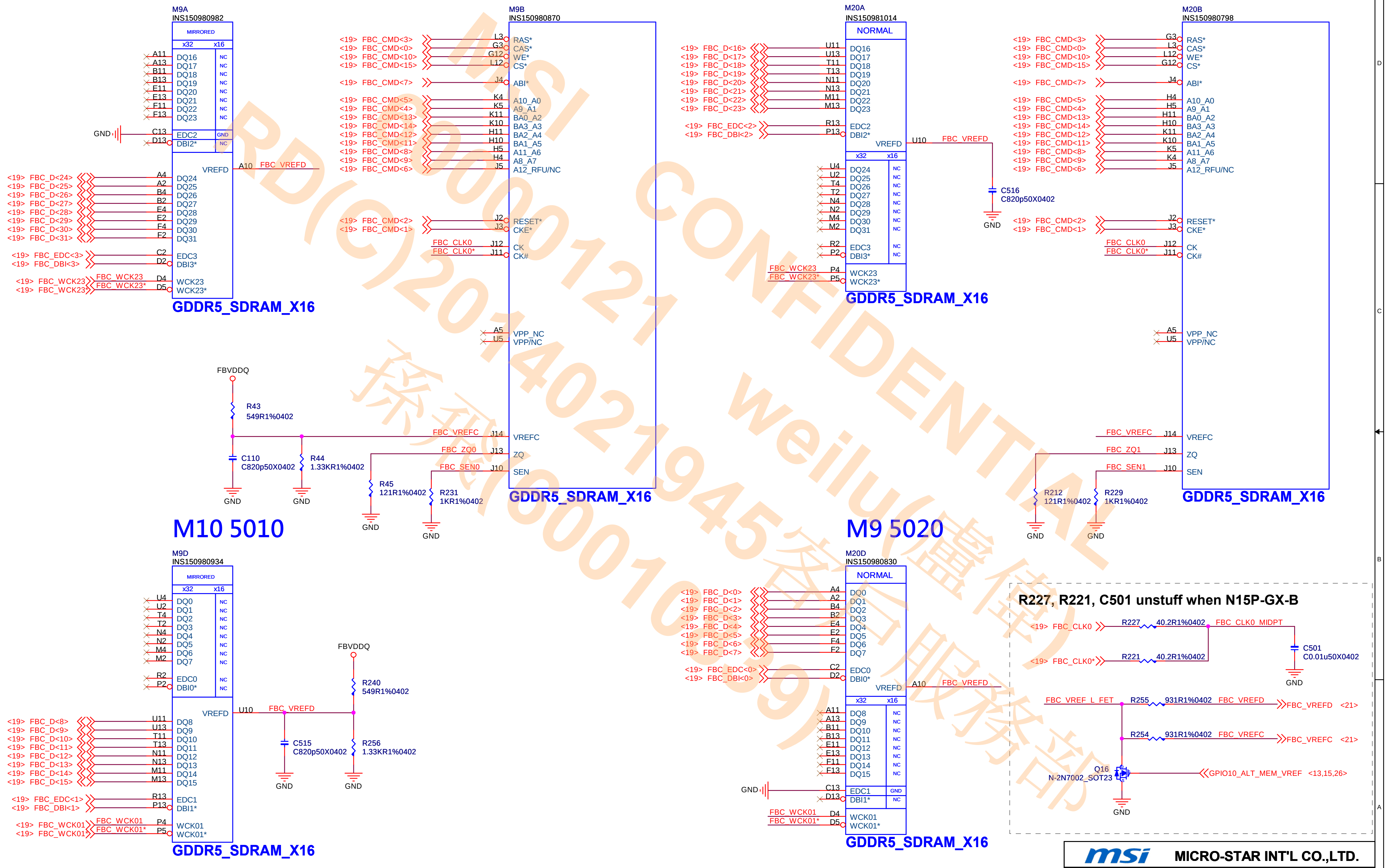
Title: DGPU_MEM IF C/D

Size | Document Number: MS-16H2 | Rev: 1.1

Date: Thursday, February 13, 2014 | Sheet 19 of 72

DGPU_GDDR5 FrameBuffer C0

(N15P-GX-B ALL unstuff)



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer C	
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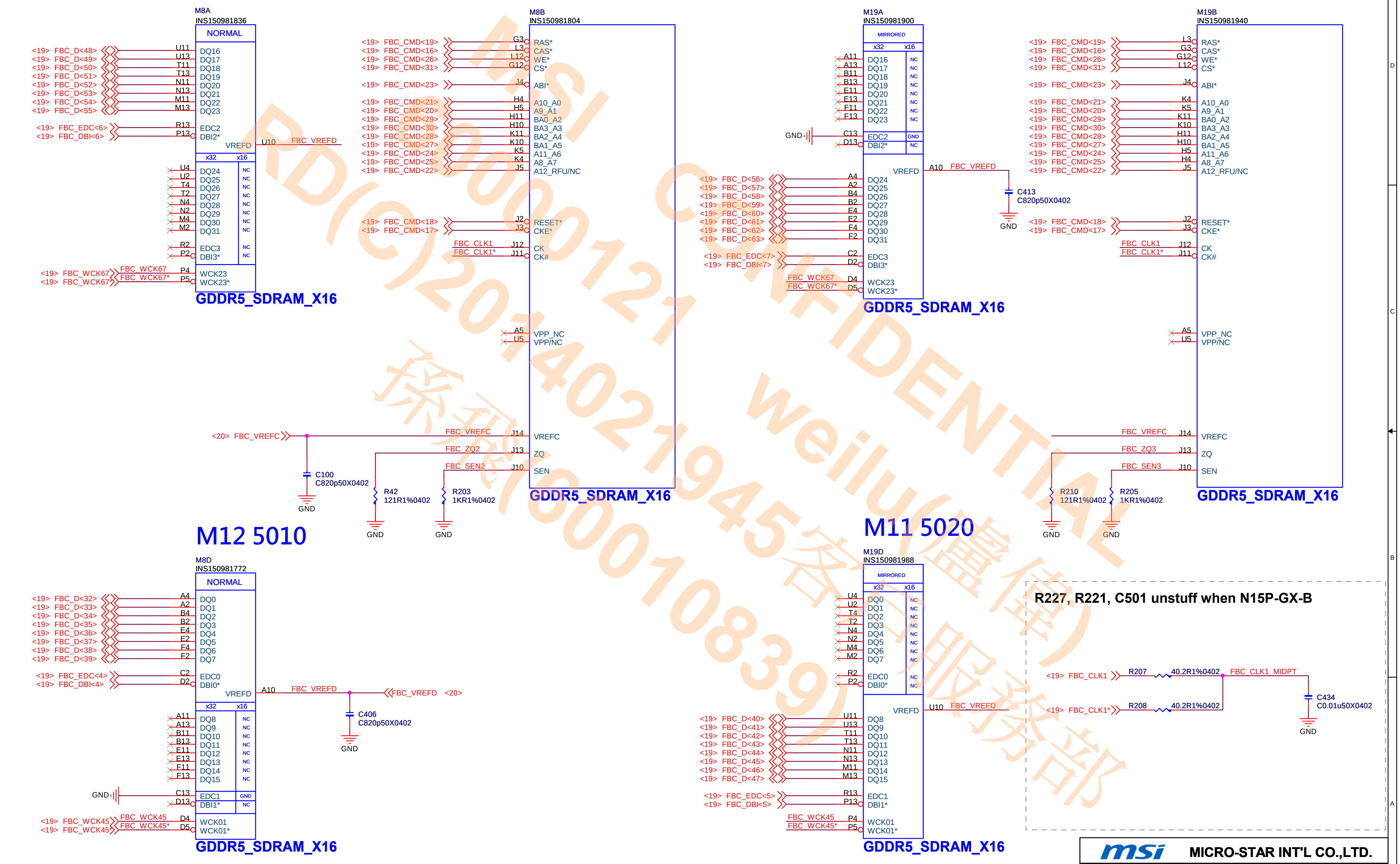
DGPU_GDDR5 FrameBuffer C1

(N15P-GX-B ALL unstuff)



msi	MICRO-STAR INT'L CO.,LTD.	
Title	DGPU_GDDR5 FrameBuffer C	
Size	Document Number: MS-16H2	Rev 1.1
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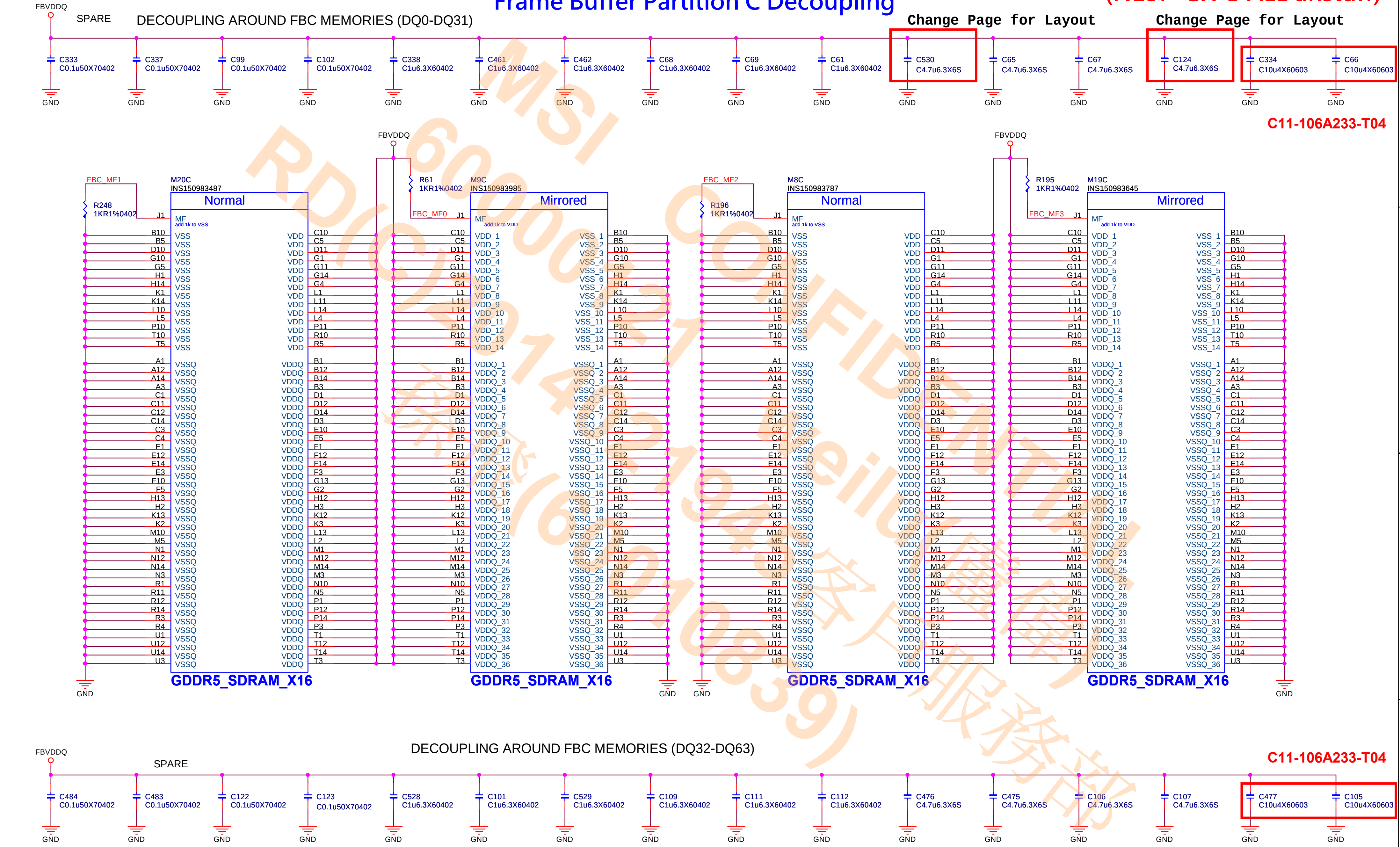
Frame Buffer Partition C Decoupling

(N15P-GX-B ALL unstuff)



DECOUPLING AROUND FBC MEMORIES (DQ0-DQ31)
FBVDDQ
SPARE
Change Page for Layout
Change Page for Layout
C333 C0.1u50X70402
C337 C0.1u50X70402
C99 C0.1u50X70402
C102 C0.1u50X70402
C338 C1u6.3X60402
C461 C1u6.3X60402
C462 C1u6.3X60402
C68 C1u6.3X60402
C69 C1u6.3X60402
C61 C1u6.3X60402
C530 C4.7u6.3X6S
C65 C4.7u6.3X6S
C67 C4.7u6.3X6S
C124 C4.7u6.3X6S
C334 C10u4X60603
C66 C10u4X60603
GND
C11-106A233-T04
FBC_MF1
R248 1KR1%0402
M20C INS150983487
Normal
MF add 1k to VSS
GDDR5_SDRAM_X16
R61 1KR1%0402
FBC_MF0
M9C INS150983985
Mirrored
MF add 1k to VDD
GDDR5_SDRAM_X16
FBC_MF2
R196 1KR1%0402
M8C INS150983787
Normal
MF add 1k to VSS
GDDR5_SDRAM_X16
R195 1KR1%0402
FBC_MF3
M19C INS150983645
Mirrored
MF add 1k to VDD
GDDR5_SDRAM_X16
DECOUPLING AROUND FBC MEMORIES (DQ32-DQ63)
SPARE
C11-106A233-T04
C484 C0.1u50X70402
C483 C0.1u50X70402
C122 C0.1u50X70402
C123 C0.1u50X70402
C528 C1u6.3X60402
C101 C1u6.3X60402
C529 C1u6.3X60402
C109 C1u6.3X60402
C111 C1u6.3X60402
C112 C1u6.3X60402
C476 C4.7u6.3X6S
C475 C4.7u6.3X6S
C106 C4.7u6.3X6S
C107 C4.7u6.3X6S
C477 C10u4X60603
C105 C10u4X60603

MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FB-C_DECOUPLING
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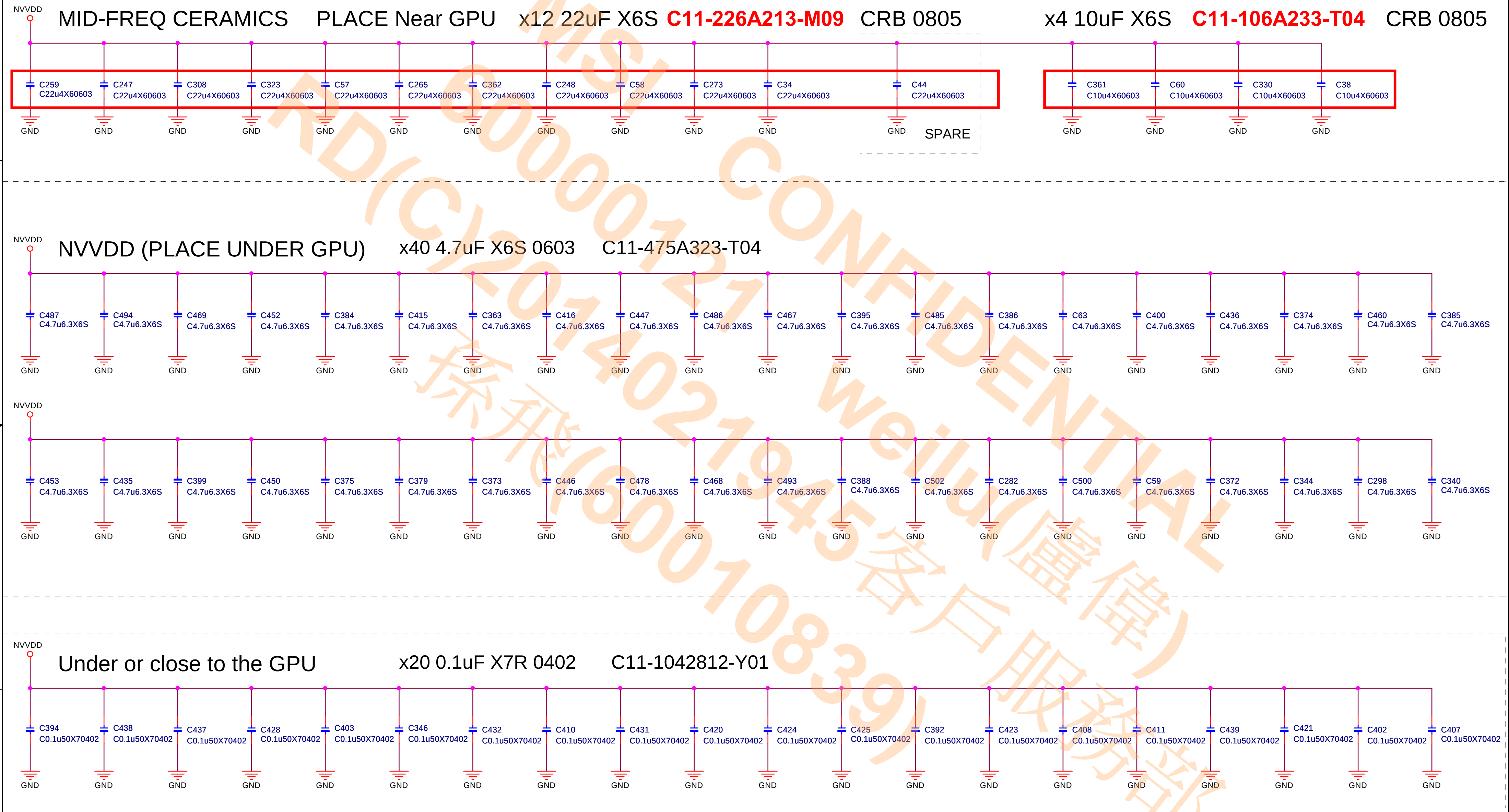
GPU DECOUPLING A



msi	MICRO-STAR INT'L CO.,LTD.
Title	DGPU_GPU DECOUPLING A
Size / Document Number	MS-16H2
Rev	1.1
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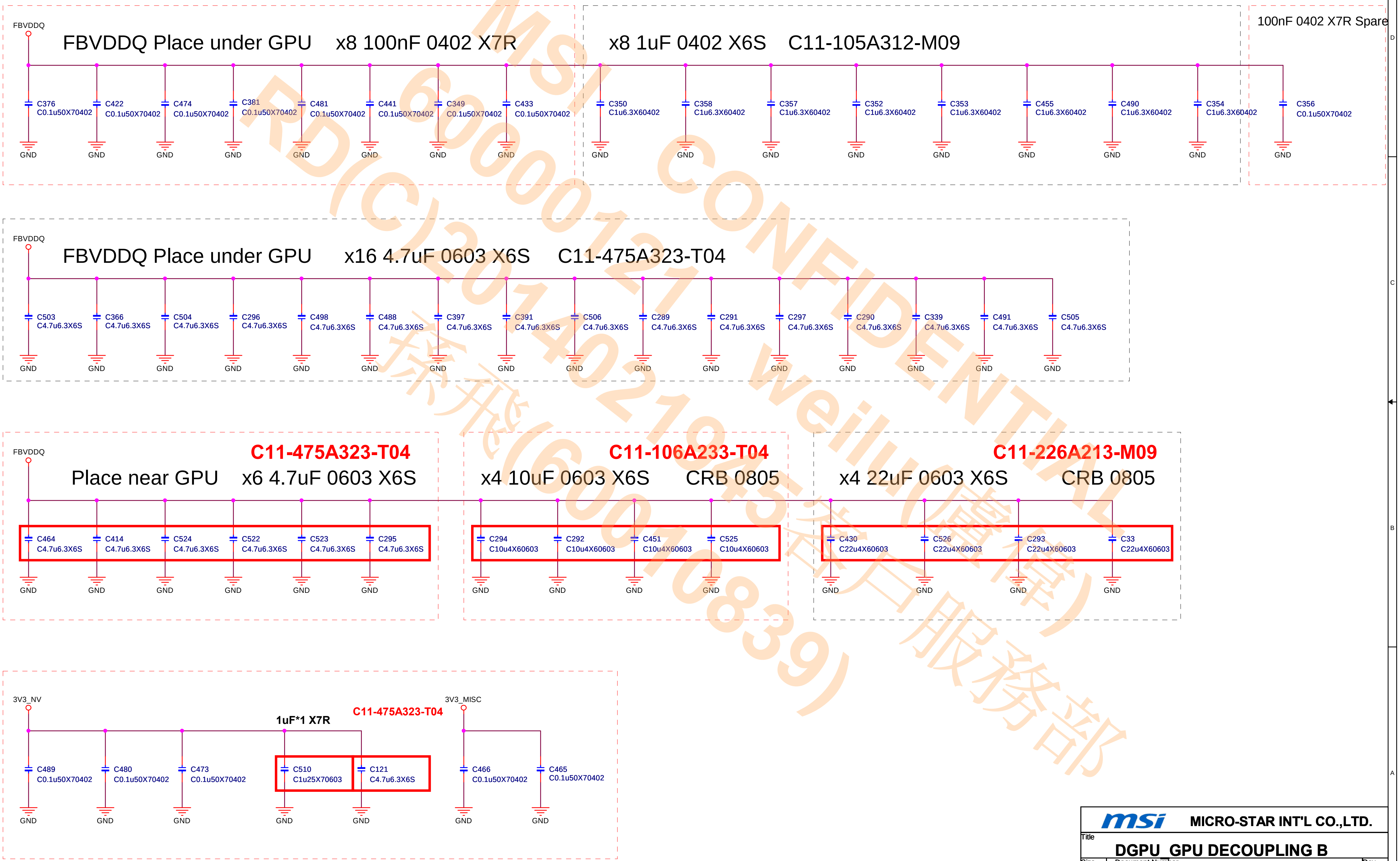
GPU DECOUPLING B



msi MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GPU DECOUPLING B

Size | Document Number: MS-16H2 | Rev: 1.1

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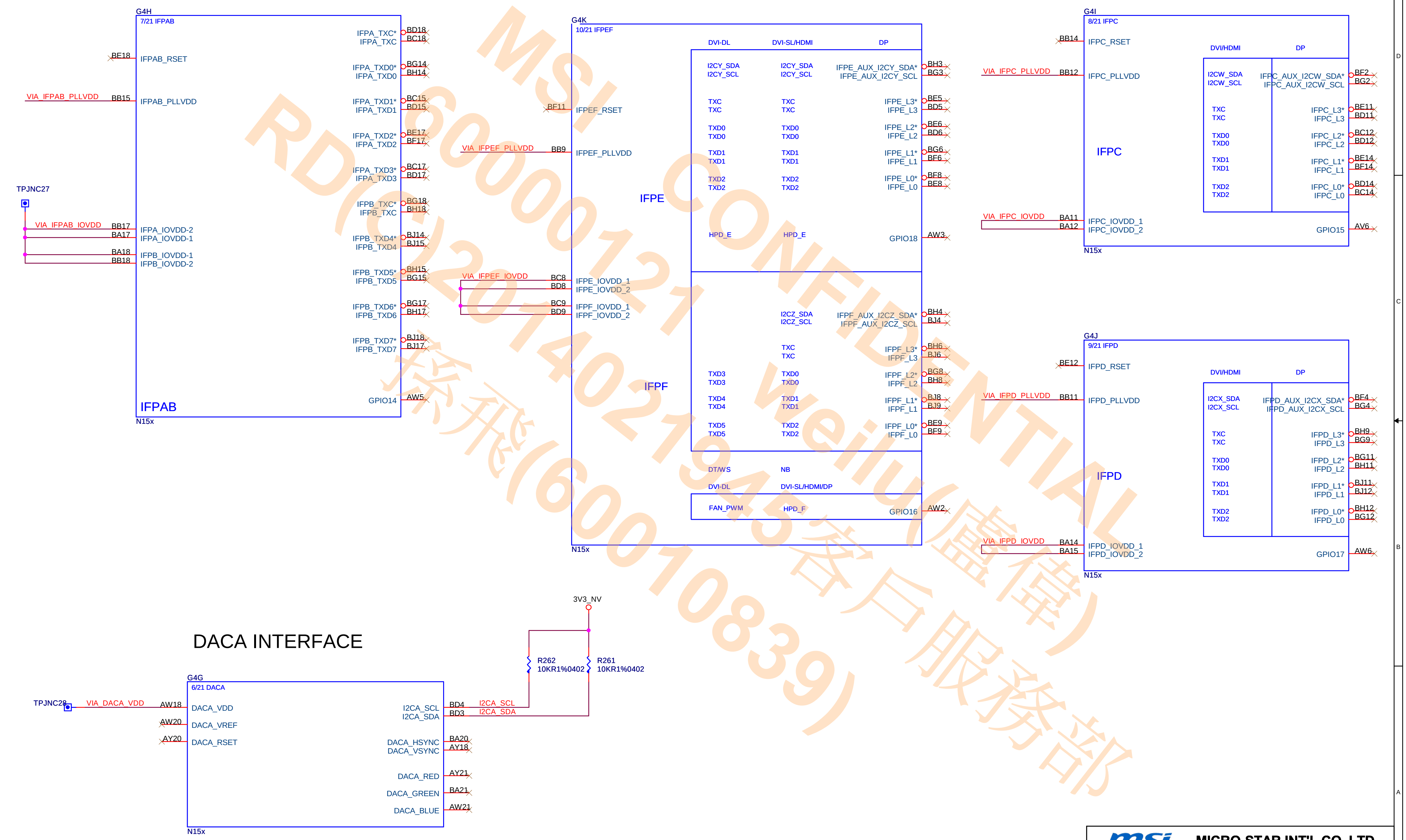
DACA,Display IF



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_DACA,Display IF
Size	
Document Number	MS-16H2
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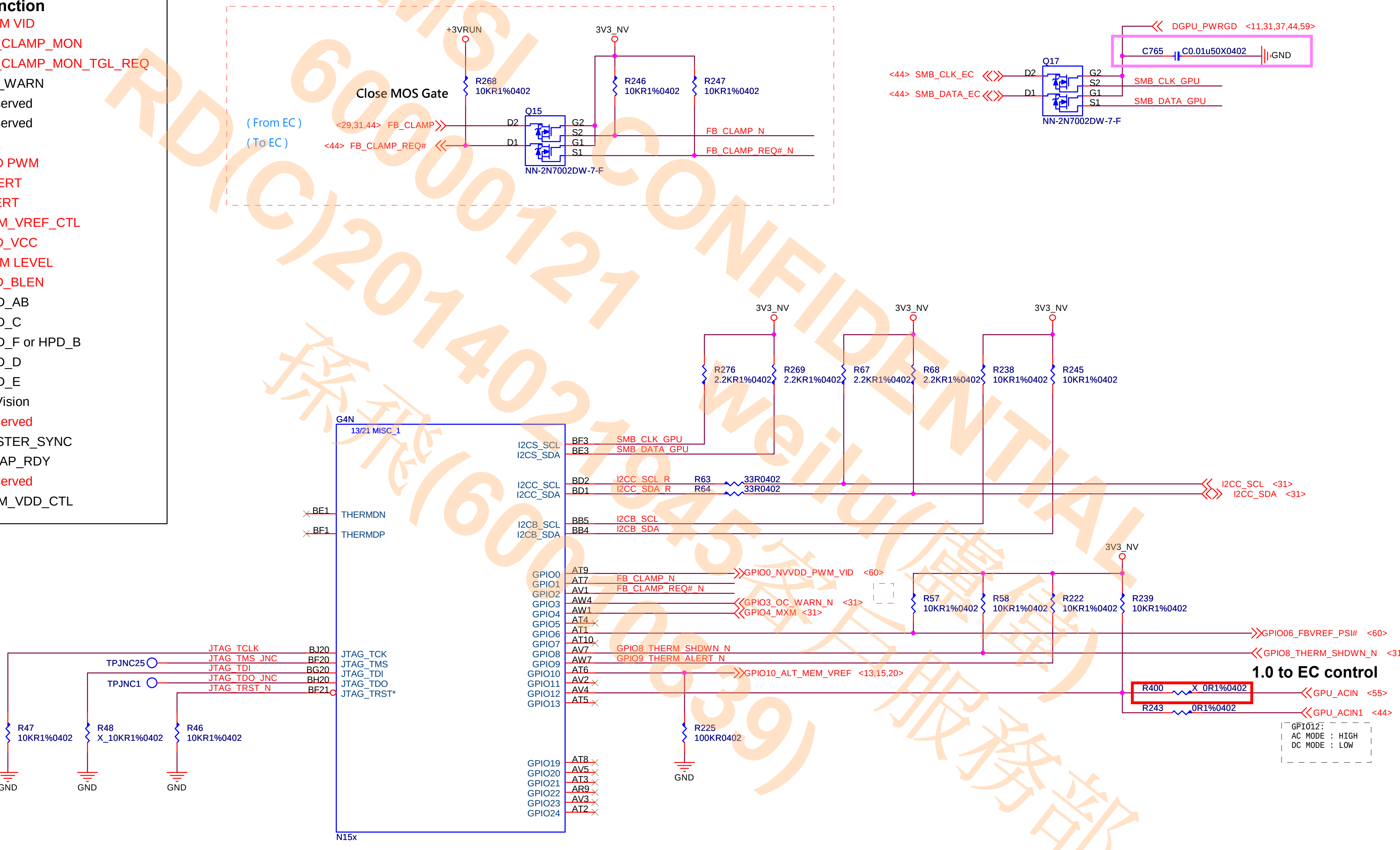
DGPU GPIO, I2C

GB3-256 GPIO(Design Guide Table 12-2)

GPIO	I/O	Function
0	OUT	PWM VID
1	IN	FB_CLAMP_MON
2	OUT	FB_CLAMP_MON_TGL_REQ
3	IN	OC_WARN
4	N/A	Reserved
5	N/A	Reserved
6	OUT	PSI
7	OUT	LCD PWM
8	OUT	OVERT
9	I/O	ALERT
10	OUT	MEM_VREF_CTL
11	OUT	LCD_VCC
12	IN	PWM LEVEL
13	OUT	LCD_BLEN
14	IN	HPD_AB
15	IN	HPD_C
16	IN	HPD_F or HPD_B
17	IN	HPD_D
18	IN	HPD_E
19	OUT	3DVision
20	N/A	Reserved
21	I/O	RASTER_SYNC
22	IN	SWAP_RDY
23	N/A	Reserved
24	OUT	MEM_VDD_CTL



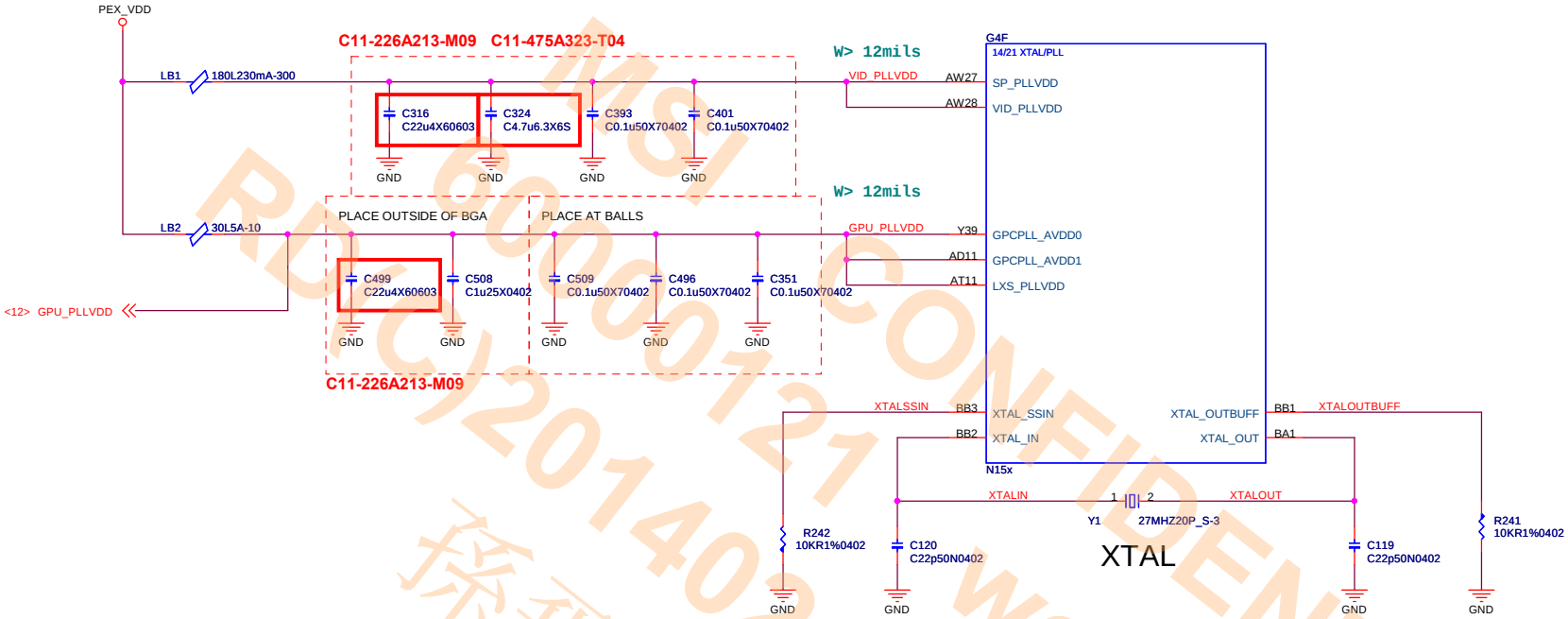
MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GPIO,I2C

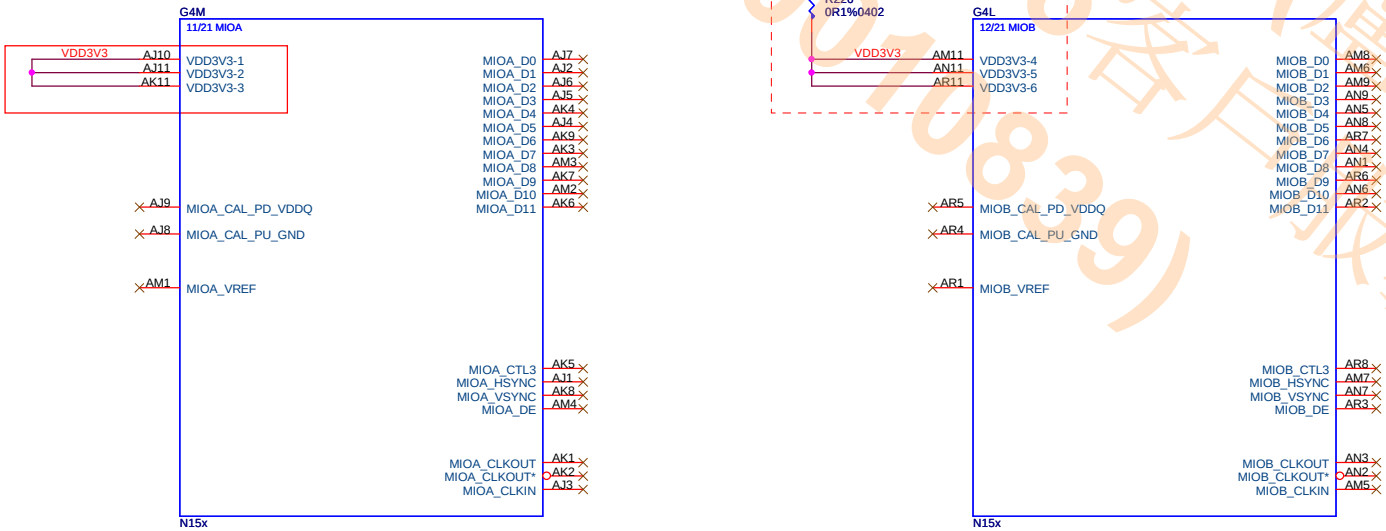
Size | Document Number: MS-16H2 | Rev: 1.1

Date: Thursday, February 13, 2014 | Sheet 26 of 72

DGPU MIO & XTAL



Multi-use IO(MIO) Interface



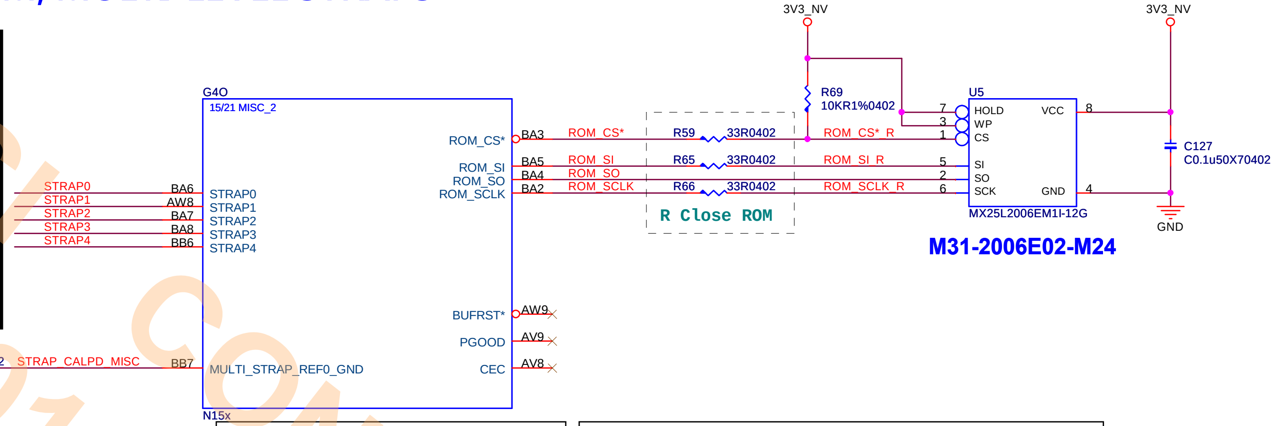
MICRO-STAR INT'L CO.,LTD.

Title	DGPU MIO & XTAL	
Size	Document Number MS-16H2	Rev 1.1
Date: Thursday, February 13, 2014	Sheet 27 of 72	

ROM, MULTI-LEVEL STRAPS

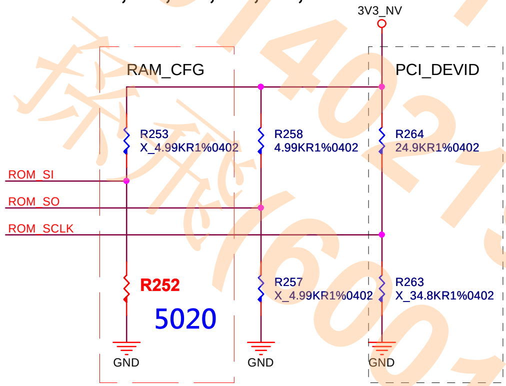
M12-4132525-S02   M12-5GC2H05-H23

	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111
	PD	PU



		5010		5020	
RCFG1 Hynix A-die 128Mx16bit	R11-3482T12-W08 X_34.8KR1%0402	GDDR5M1	M12-5GQ2HL5-H23 X_H5GQ2H24AFR-R0C	GDDR5M2	M12-5GQ2HL5-H23 X_H5GQ2H24AFR-R0C
RCFG2 Samsung 128Mx16bit	R11-4532T12-W08 X_45.3KR1%0402	GDDR5M3	M12-2032585-S02 X_K4G20325FD-FC03	GDDR5M4	M12-2032585-S02 X_K4G20325FD-FC03
RCFG3 Hynix 256Mx16bit	R11-0153T12-W08 X_15KR1%0402	GDDR5M5	M12-5GC4H05-H23 X_H5GC4H24MFR-T2C	GDDR5M6	M12-5GC4H05-H23 X_H5GC4H24MFR-T2C
RCFG4 Micron 256Mx16bit	R11-0103T12-W08 X_10KR1%0402	GDDR5M7	M12-4032B05-E59 X_EDW4032BABG-60-F	GDDR5M8	M12-4032B05-E59 X_EDW4032BABG-60-F
RCFG5 Samsung 256Mx16bit	R11-0203T12-W08 X_20KR1%0402	GDDR5M9	M12-4132525-S02 X_K4G41325FC-HC03	GDDR5M10	M12-4132525-S02 X_K4G41325FC-HC03
RCFG6 Hynix B-die 128Mx16bit	R11-2492T12-W08 X_24.9KR1%0402	GDDR5M11	M12-5GC2H05-H23 X_H5GC2H24BFR-T2C	GDDR5M12	M12-5GC2H05-H23 X_H5GC2H24BFR-T2C

GDDR5 Parts
5020 : M15, M16, M17, M18, M19, M20
5010 : M3, M4, M5, M6, M8, M9



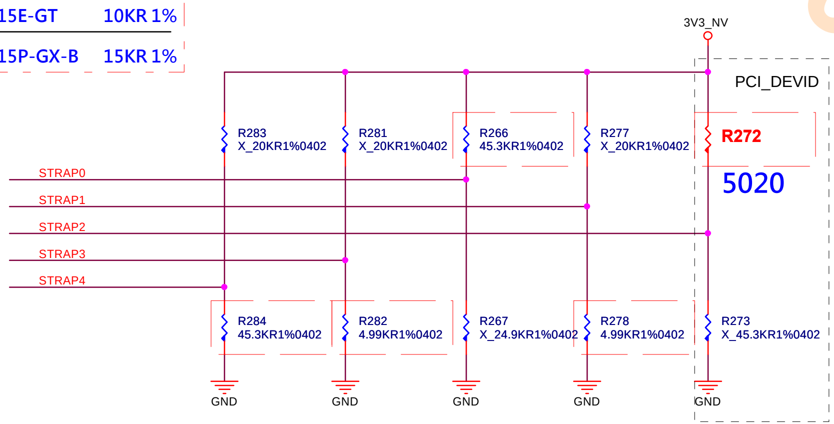
R252	
For Hynix 128Mx16 a-die	35KR 1%
For Samsung 128Mx16	45KR 1%
For Hynix 128Mx16 b-die	25KR 1%
For Hynix 256Mx16	15KR 1%
For Elpida 256Mx16	10KR 1%
For Samsung 256Mx17	20KR 1%

Setting	R252	5010	5020
Hynix 128Mx16 a-die	RCFG1	GDDR5M1	GDDR5M2
Samsung 128Mx16	RCFG2	GDDR5M3	GDDR5M4
Hynix 128Mx16 b-die	RCFG6	GDDR5M11	GDDR5M12
Hynix 256Mx16	RCFG3	GDDR5M5	GDDR5M6
Elpida 256Mx16	RCFG4	GDDR5M7	GDDR5M8
Samsung 256x16	RCFG5	GDDR5M9	GDDR5M10

STRAP0	USER_BIT[3:0]	0xF: EDID	45K PU	
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]	0x0: DDI no used	5K PD	
STRAP2	PCI_DEVID[3:0]	15E-GT 0x1199 15P-GX-B 0x119A	10K PU 15K PU	
ROM_SO	VGA_DEVICE SMB_ALT_ADDR FB_0_BAR_SIZE XCLK_417	0x0001	5K PU	
ROM_SI	RAM_CFG_0 RAM_CFG_1 RAM_CFG_2 RAM_CFG_3	0110 0111 0010 0001	35K PD 45K PD 15K PD 10K PD	Hynix 128x16bit Samsung 128x16bit Hynix 256xbit Elpida 256xbit
ROM_SCLK	PCI_DEVID[4] SUB_VENDOR PCI_DEVID[5] PEX_PLL_EN_TERM100	1: 0x119=>1001 1: VBIOS ROM is Present 0: 0x119=>1001	25K PU	
STRAP3	SOR_EXposed [3:0]	0000	5K PD	
STRAP4	Reserved PCIE_Speed_Change_Gen3 PCIE_MAX_SPEED DP_PLL_VDD_33V	0 1: Enable PCIE Gen3 operation 1: Allow booting to GEN2/Gen3 1: ENABLED	45K PD	

RGPU1	N15E-GT 5020	R11-0103T12-W08 X_10KR1%0402
DGPU1	5010	B03-0N15E05-N08 X_N15E-GT-A2
RGPU2	N15P-GX-B 5020	R11-0153T12-W08 X_15KR1%0402
DGPU2	5010	B03-0N15P35-N08 X_N15P-GX-B-A2

R272	
N15E-GT	10KR 1%
N15P-GX-B	15KR 1%



msi	MICRO-STAR INT'L CO.,LTD.	
Title	DGPU_ROM,HW Straps	
Size / Document Number	MS-16H2	Rev 1.1
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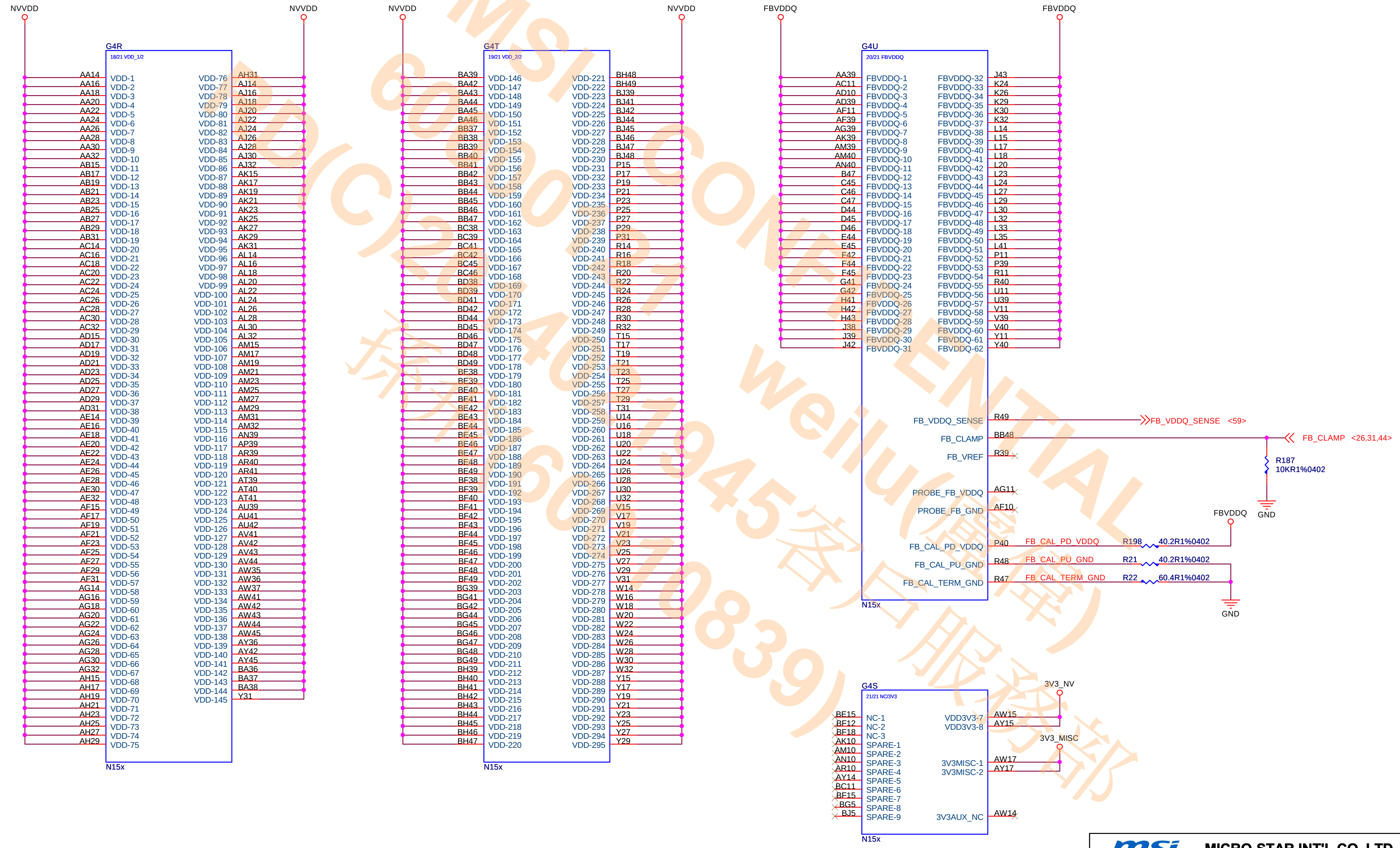
GPU NVVDD, FBVDDQ



MICRO-STAR INT'L CO.,LTD.

Title: DGPU NVVDD, FBVDDQ

Size | Document Number: MS-16H2 | Rev: 1.1

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DGPU GND

msi	MICRO-STAR INT'L CO.,LTD.	
Title	DGPU GND	
Size	Document Number: MS-16H2	Rev: 1.1
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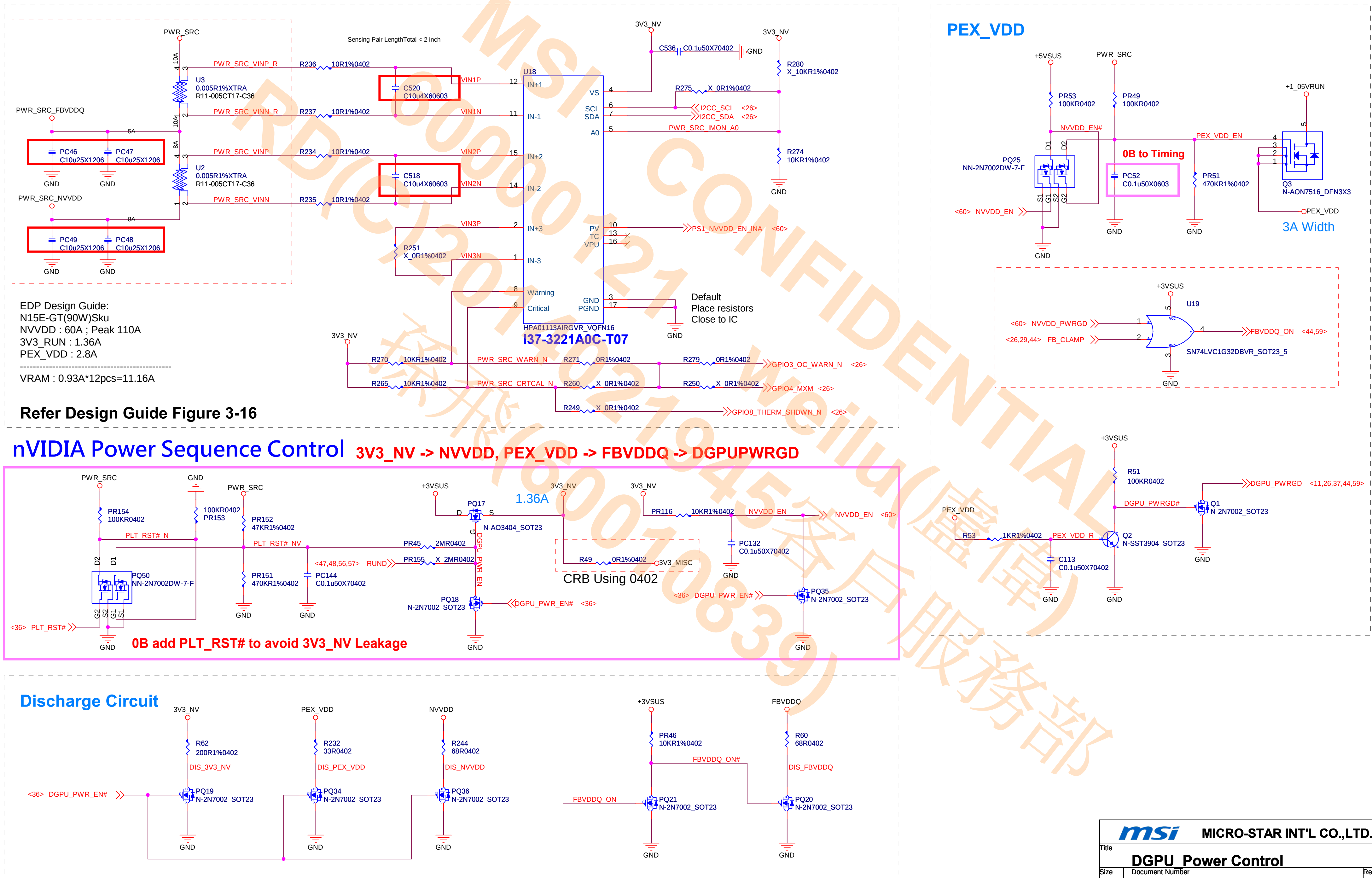
DGPU_Power Control

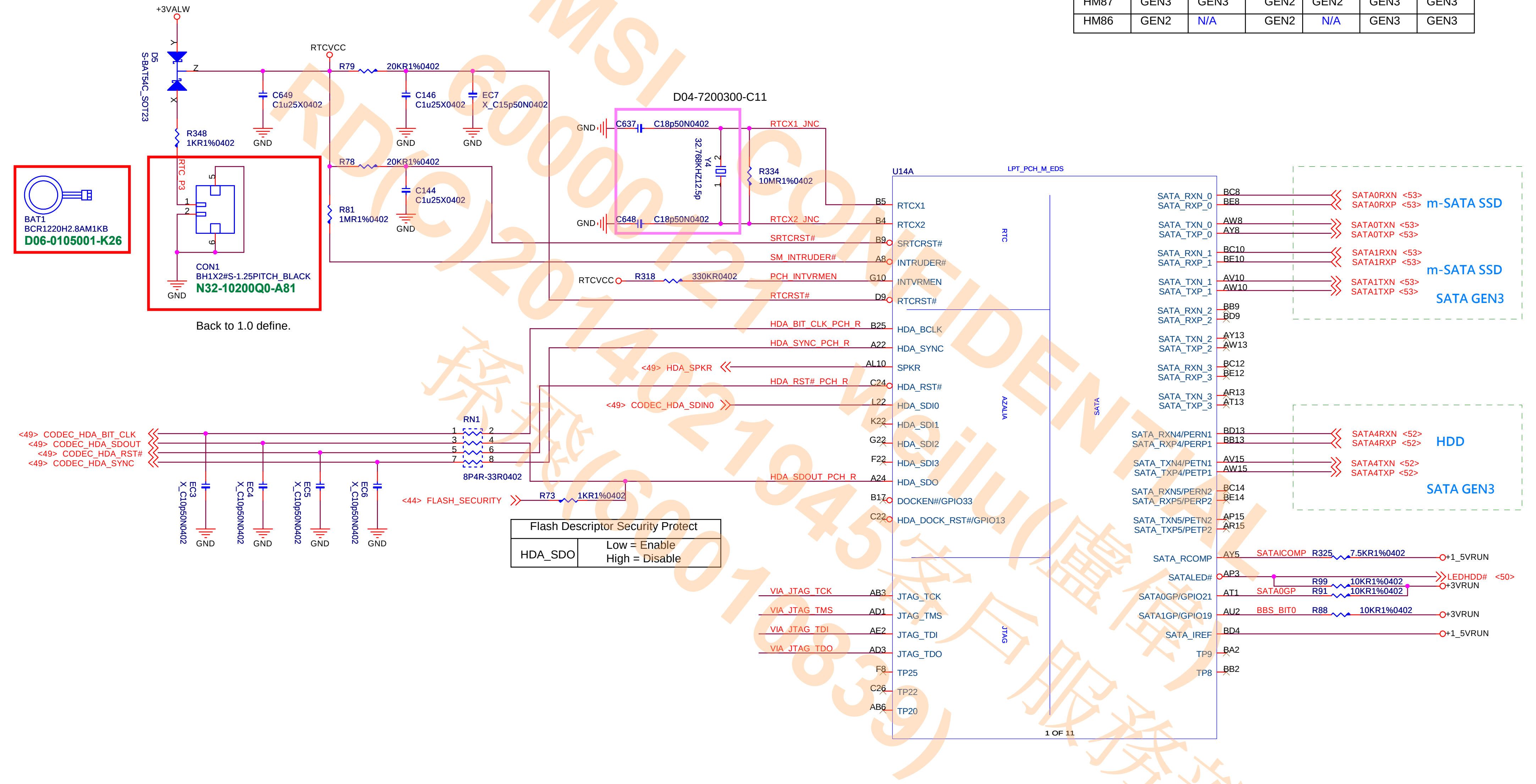


MICRO-STAR INT'L CO.,LTD.

Title	DGPU_Power Control	
Size	Document Number: MS-16H2	Rev 1.1
Date: Thursday, February 13, 2014	Sheet 31 of 72	

Lynx Point (HDA/JTAG/SATA)

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3



Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

SPK	The Signal has a weak internal pull-down Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)

MICRO-STAR INT'L CO.,LTD.

Title	PCH-1 (HDA/JTAG/SATA)
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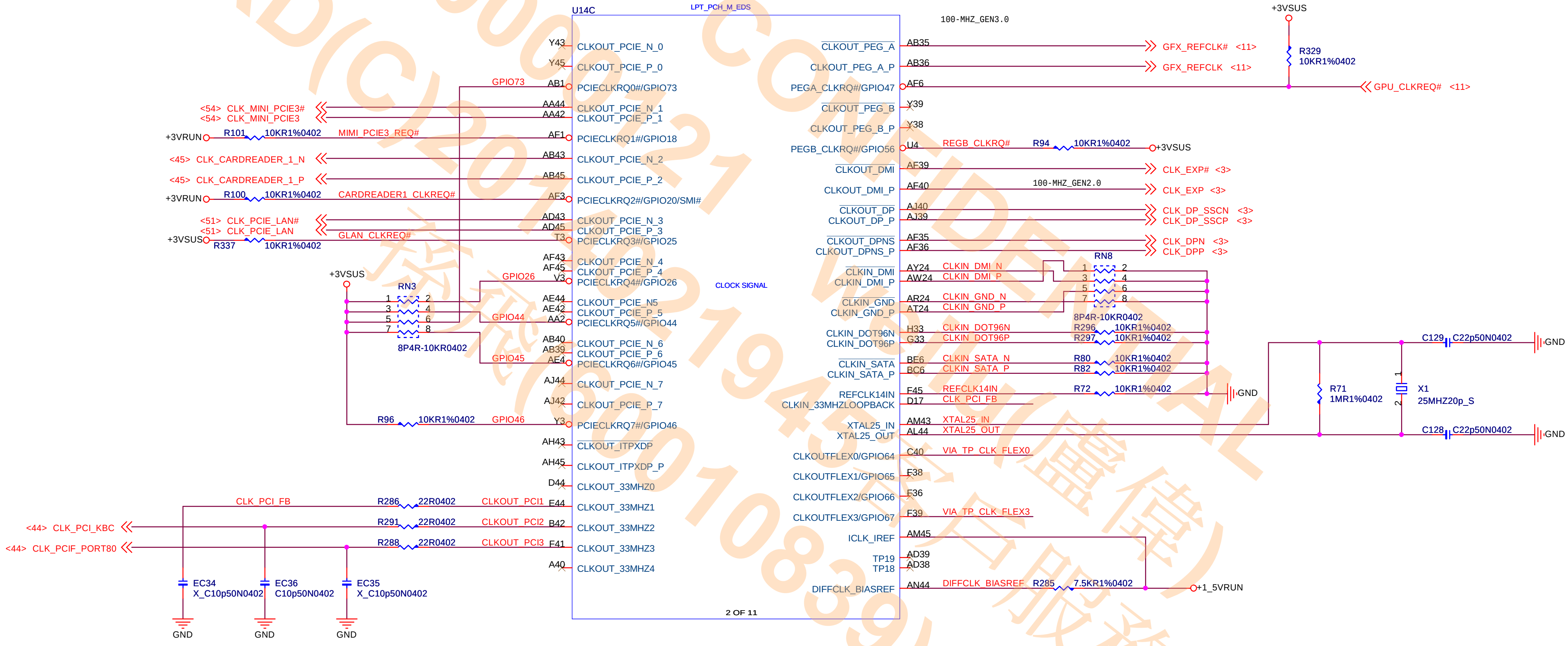
Lynx Point (Clock)

PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 kΩ ±10% external pull-up resistor instead of No Connect.
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.



The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

msi	MICRO-STAR INT'L CO.,LTD.
Title	PCH-2 (CLK)
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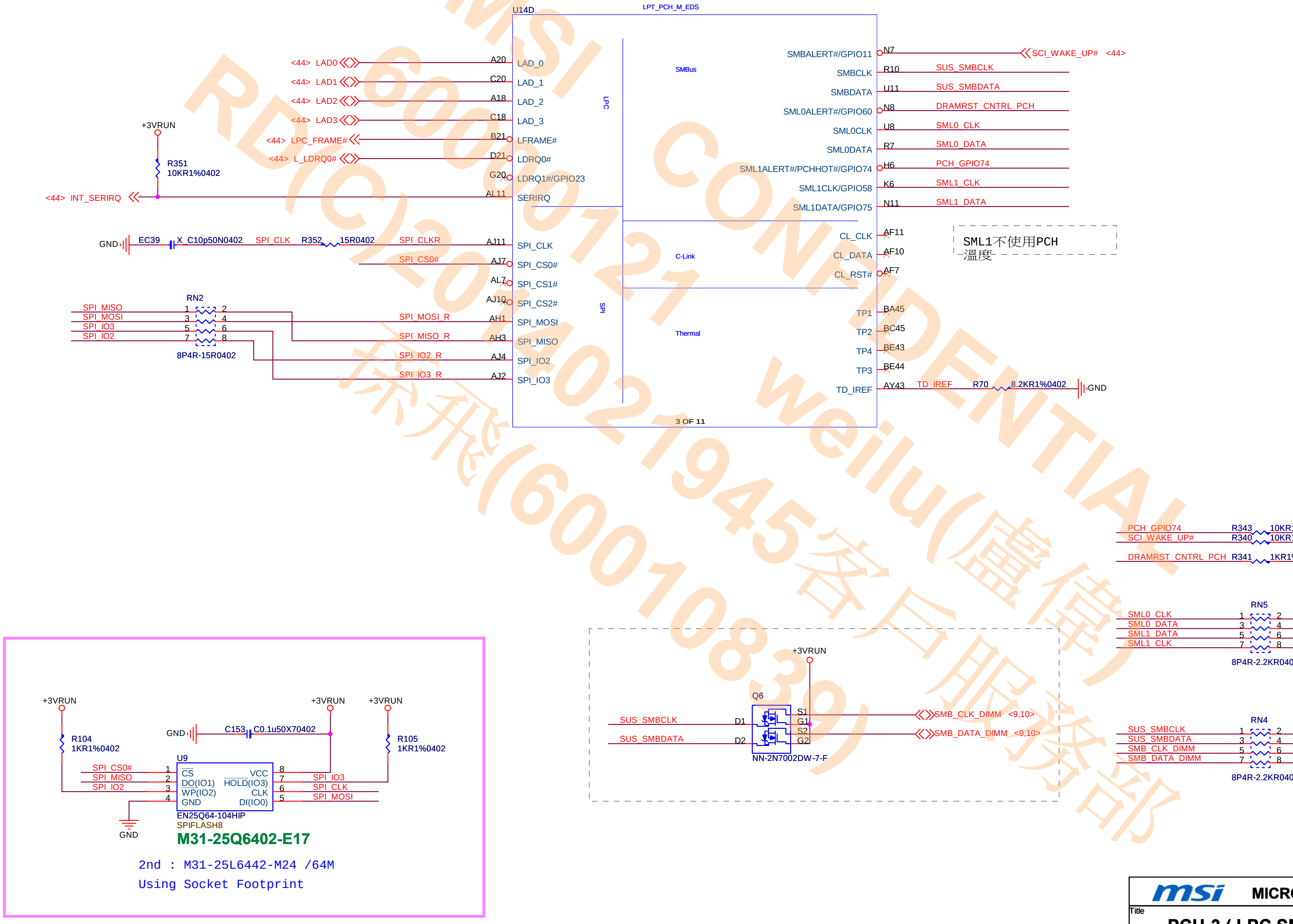
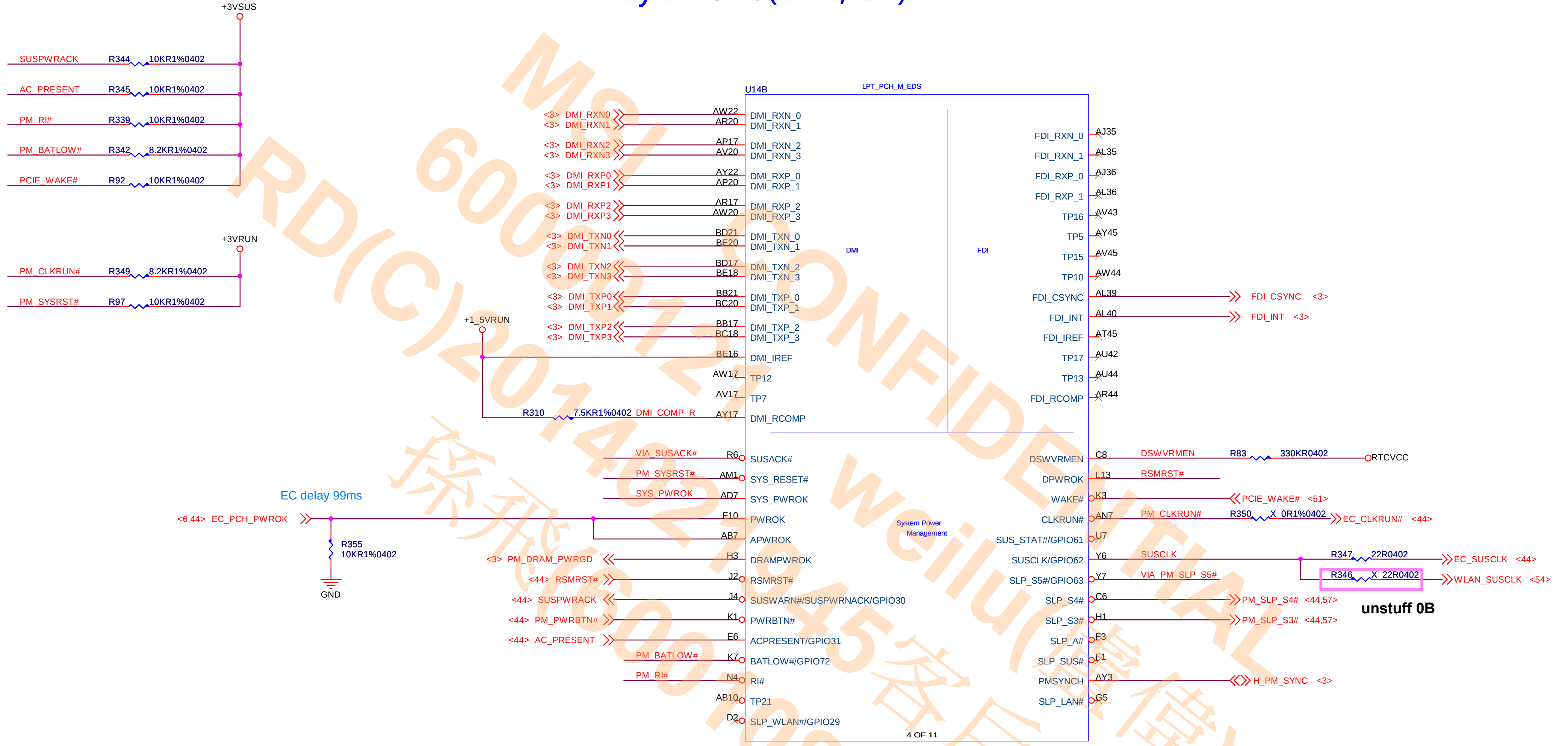
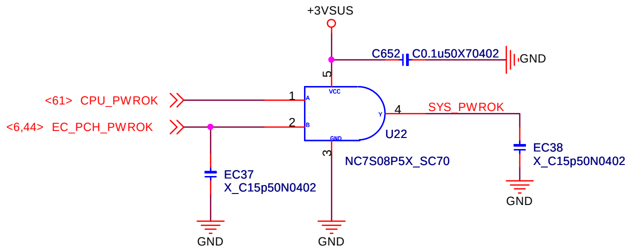
Lynx Point (LPC,SMBUS)



Lynx Point (DMI,FDI)





APWROK
not supporting Intel AMT , it can be connected to PWROK

GPIO31 : If not used,require pull up +3VSUS

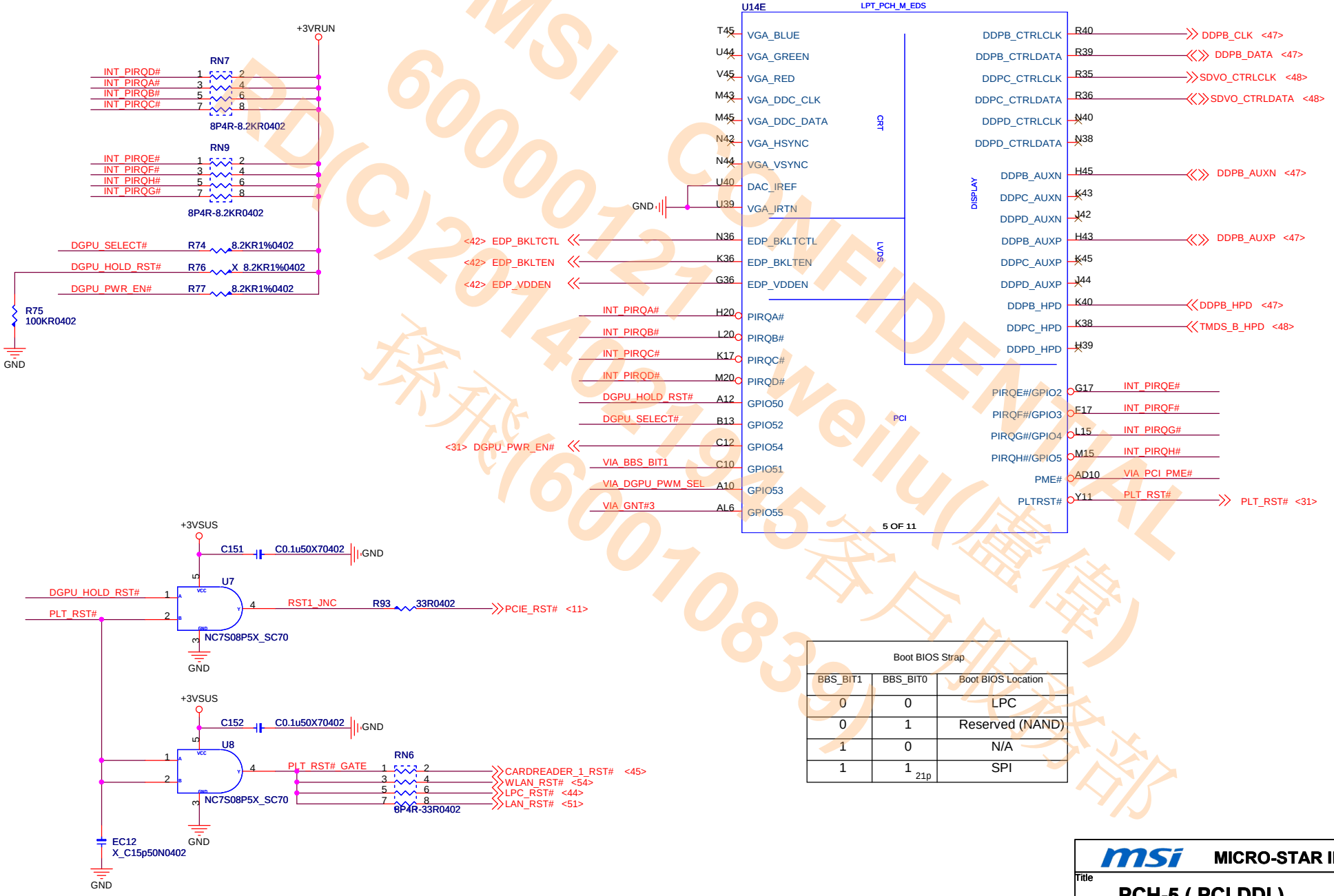
DSWVRMEN - On Die DSW VR Enable
HIGH : Enable internal 1.05V regulator
LOW : Disable

DPWROK
Without deep s4/s5 support tied together with RSMRST#

GPIO Setting : Ref 486708_LPT_EDS Section2.18

PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

Lynx Point (PCI,DDI)



Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

21p

MICRO-STAR INT'L CO.,LTD.

Title: PCH-5 (PCI,DDI)

Size | Document Number: MS-16H2 | Rev: 1.1

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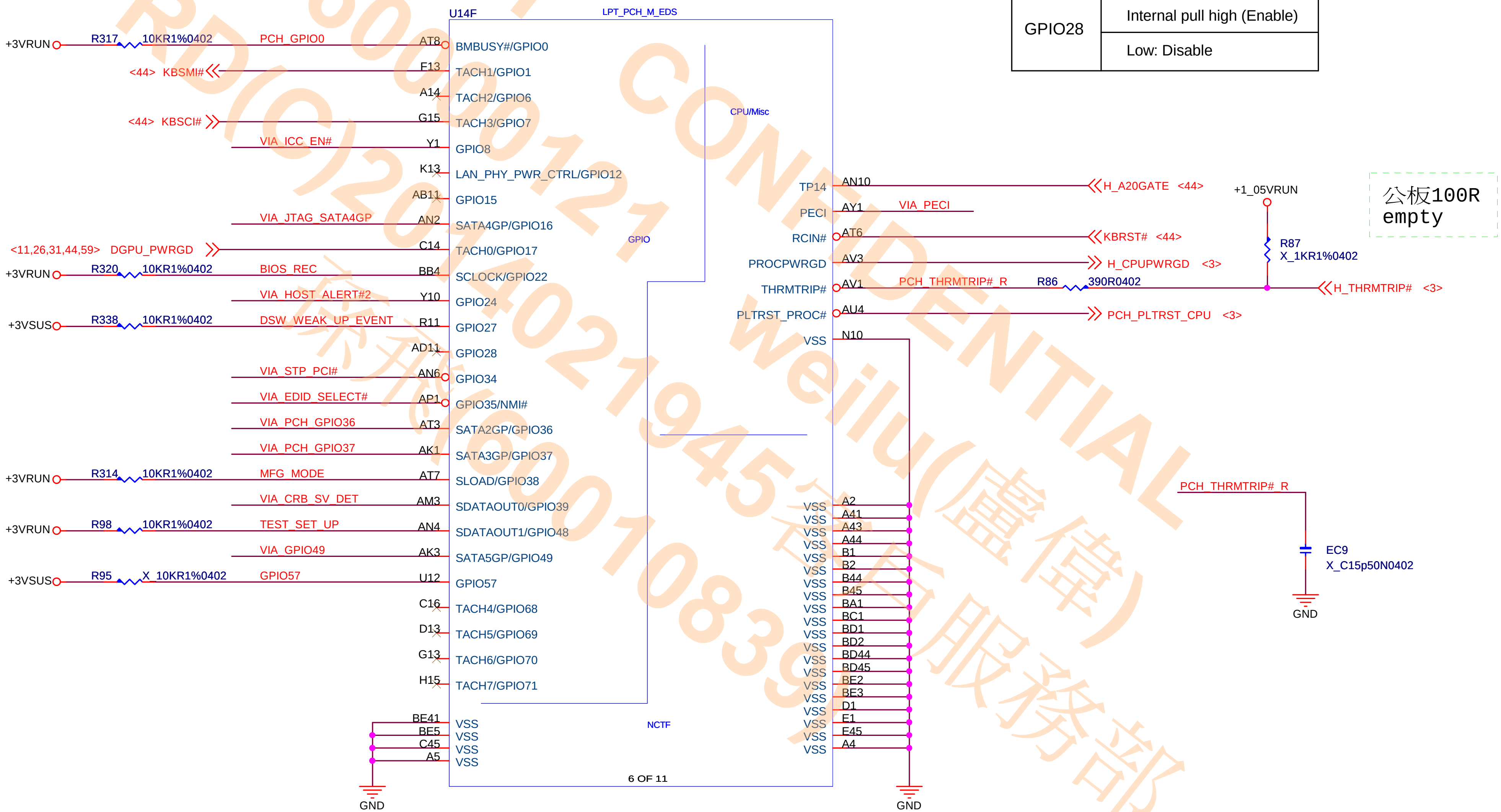
Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable



MICRO-STAR INT'L CO.,LTD.

Title: **PCH-6 (GPIO,MISC)**

Size	Document Number	Rev
	MS-16H2	1.1

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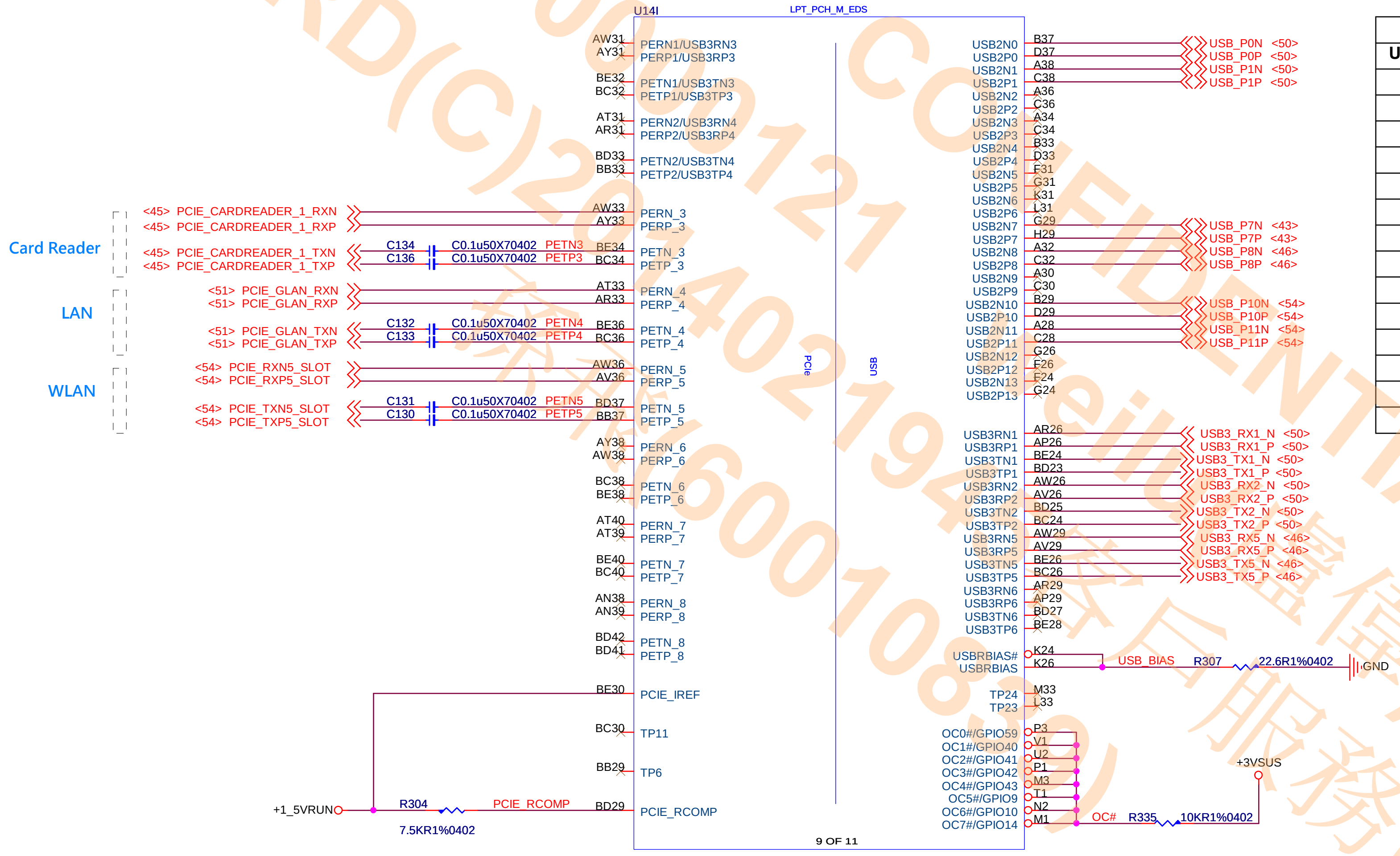
Lynx Point (PCIE,USB)

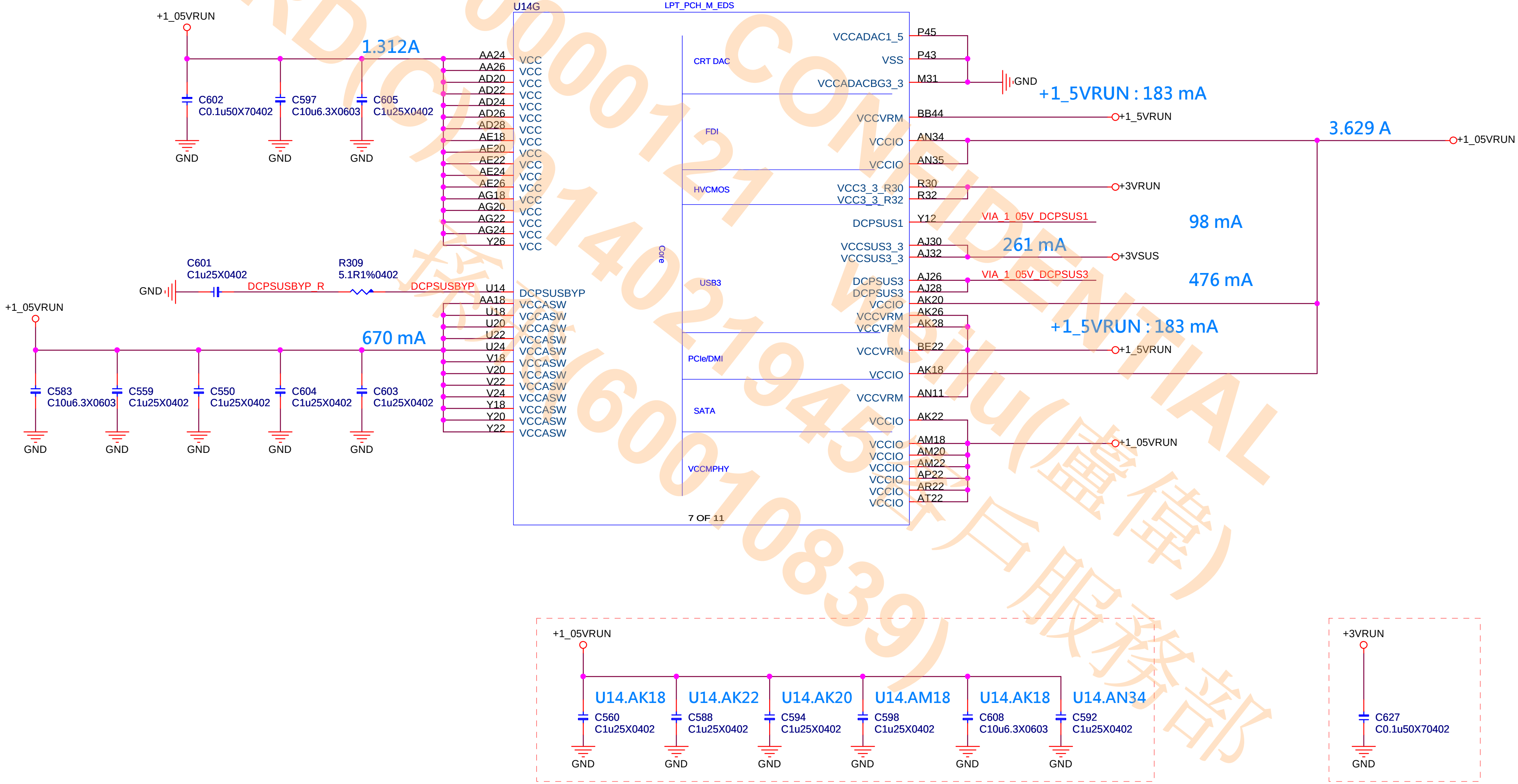
Intel Lynx Point ECHI USB(2.0) debug transport 需接Port1 or Port9



USB			
USB 2.0	**USB 3.0**	**Device**	**Note**
0	1	USB 3.0 Port 1	**16H2A**
1	2	USB 3.0 Port 2	**16H2A**
2			
3			NC
4			NC
5			NC
6			NC
7		EPF021	3 色KBC
8	3	USB 3.0 Port 5	**16H21**
9			NC
10		WLAN	
11		WebCam	
12		SECOND DISPLAY	
13			NC

HM86 沒USB3.0 PORT 5,6

Lynx Point (Power)



MICRO-STAR INT'L CO.,LTD.

Title	PCH-8 (Power)	
Size	Document Number MS-16H2	Rev 1.1
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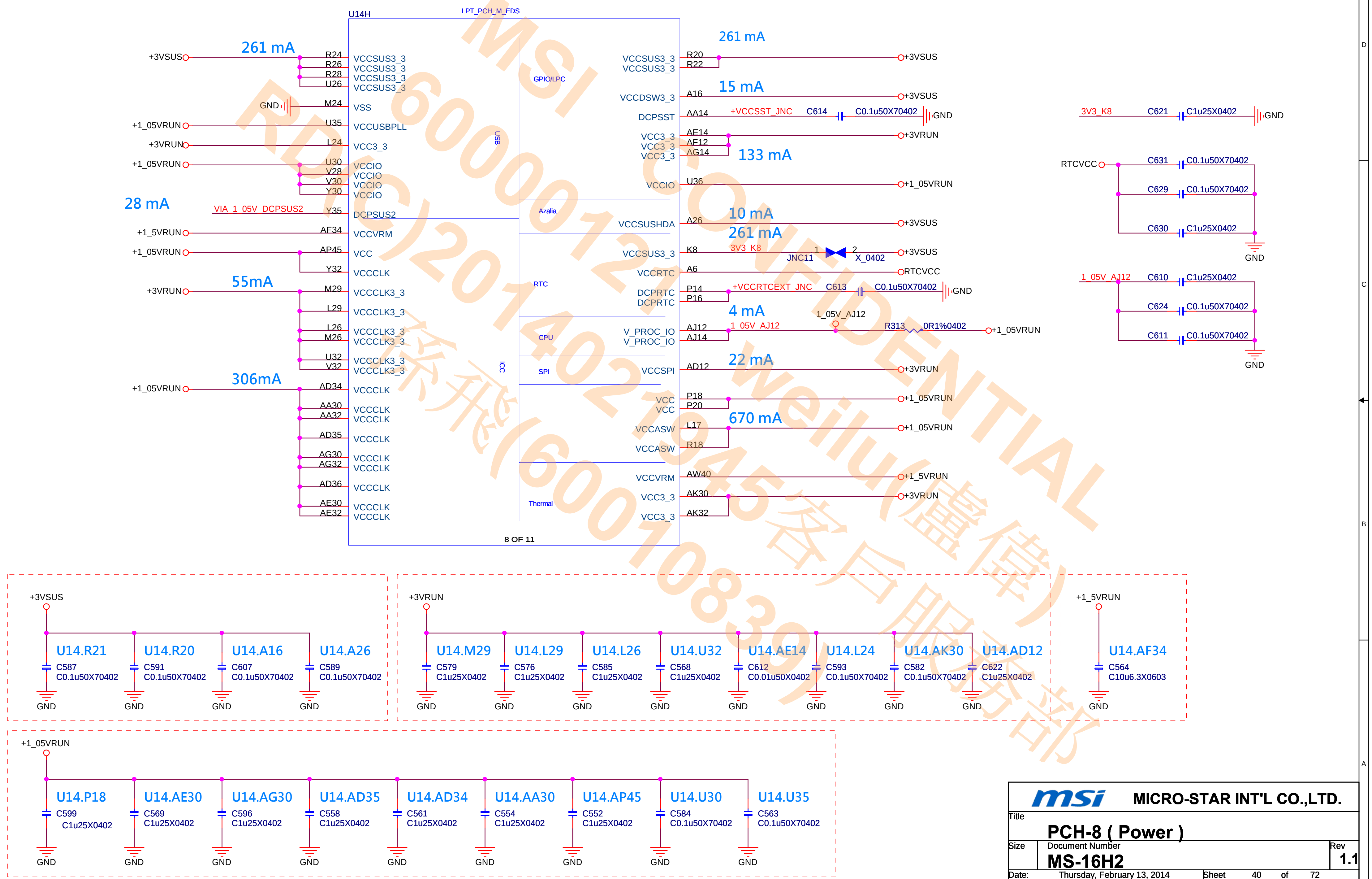
Lynx Point (Power)



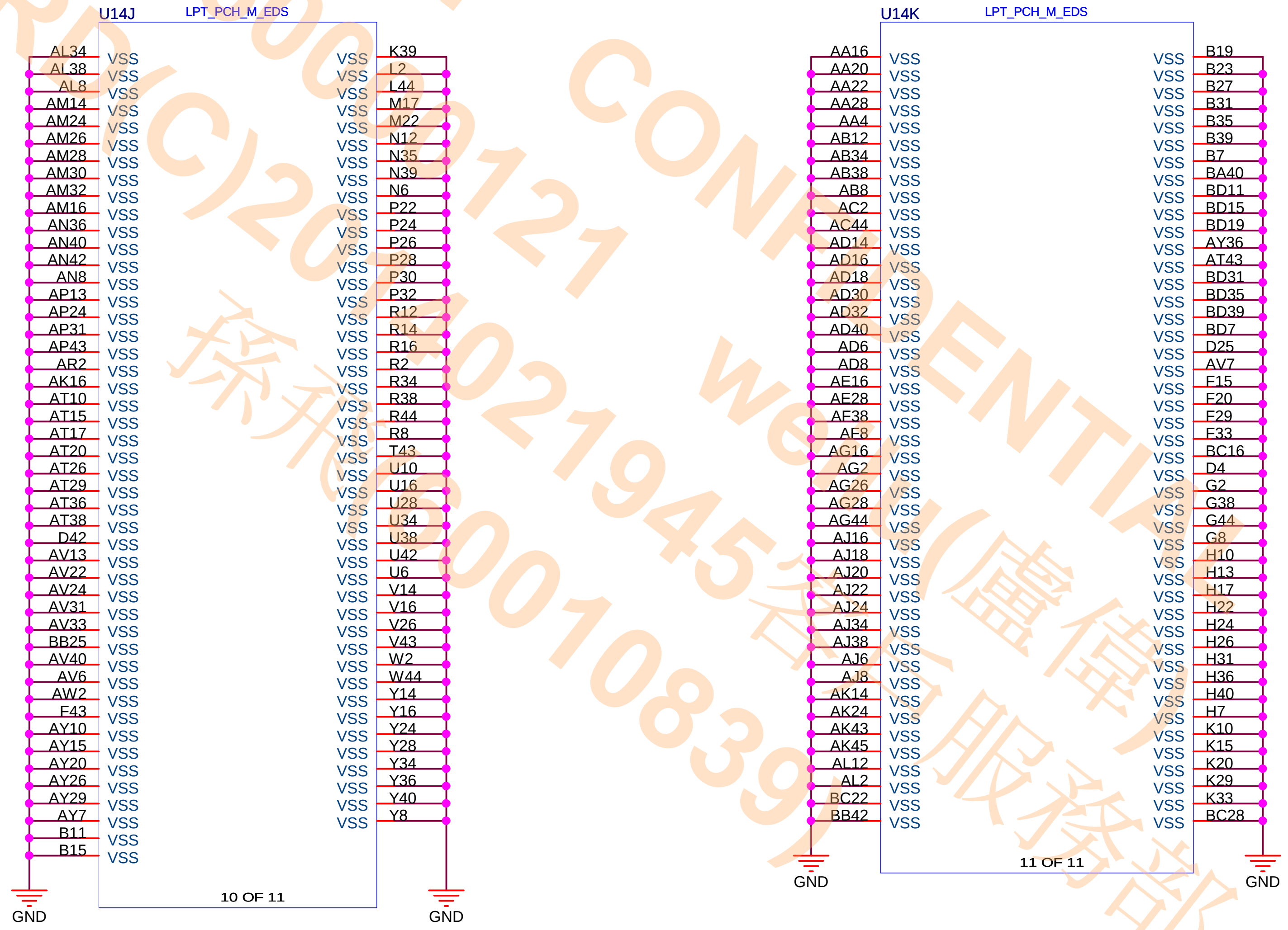
MICRO-STAR INT'L CO.,LTD.

Title: PCH-8 (Power)

Size | Document Number: MS-16H2 | Rev: 1.1

Date: Thursday, February 13, 2014 | Sheet 40 of 72

Lynx Point (GND)



MICRO-STAR INT'L CO.,LTD.

Title: **PCH-8 (GND)**

Size | Document Number: **MS-16H2** | Rev: **1.1**

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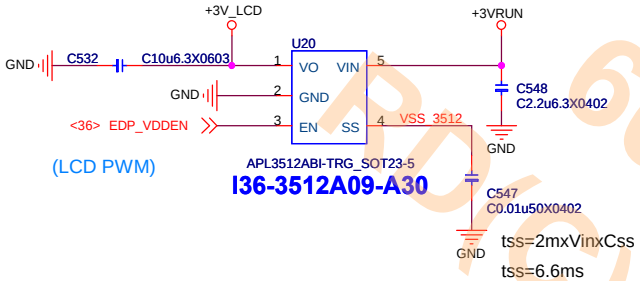
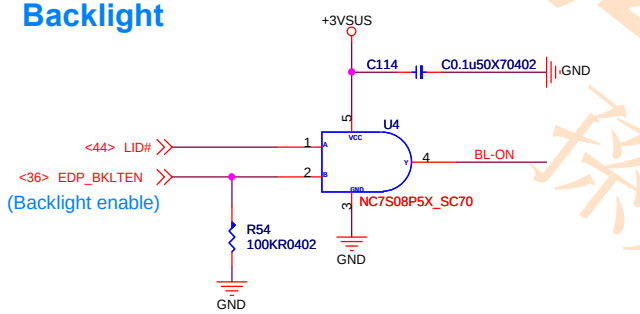
eDP Connector

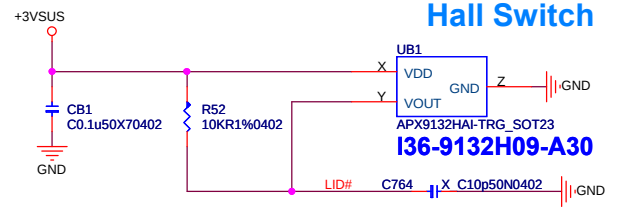
Pannel Device Logic Power



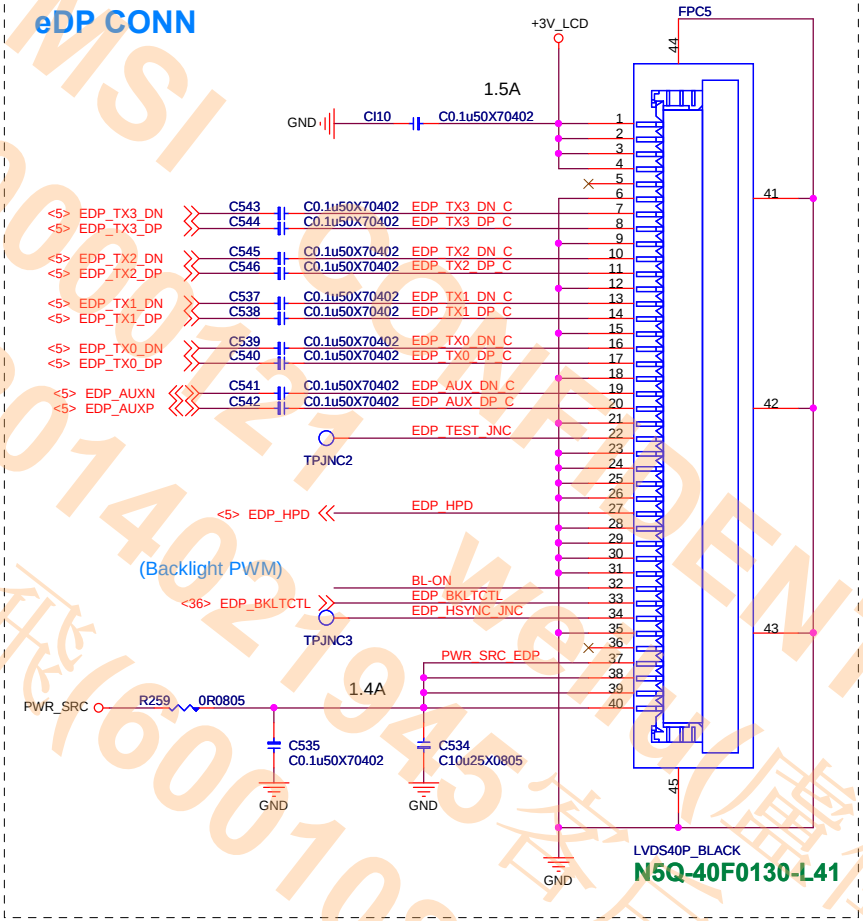
Backlight



Hall Switch

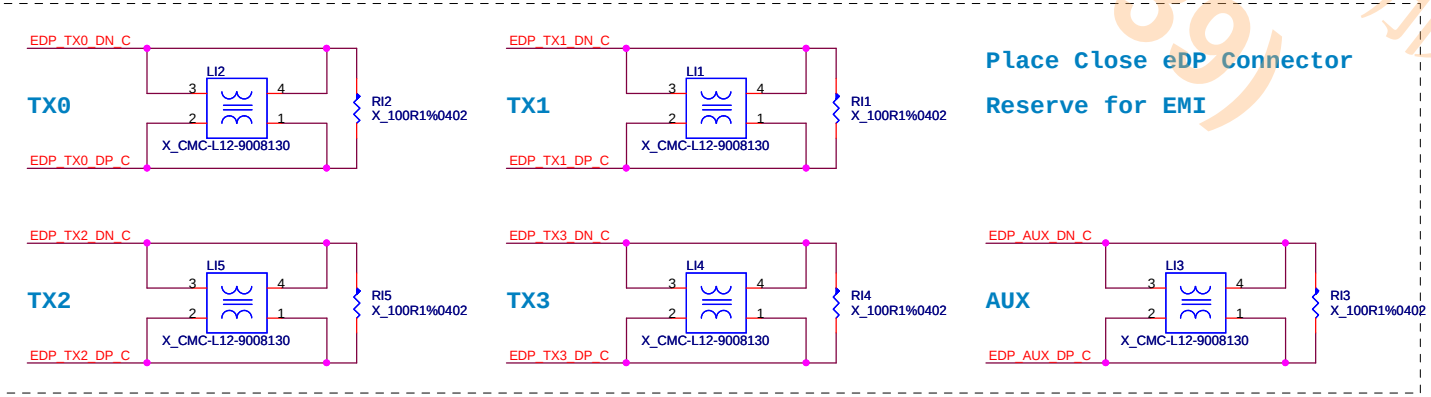


eDP CONN



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon



MICRO-STAR INT'L CO.,LTD.

Title: eDP Connector

Size | Document Number: MS-16H2 | Rev: 1.1

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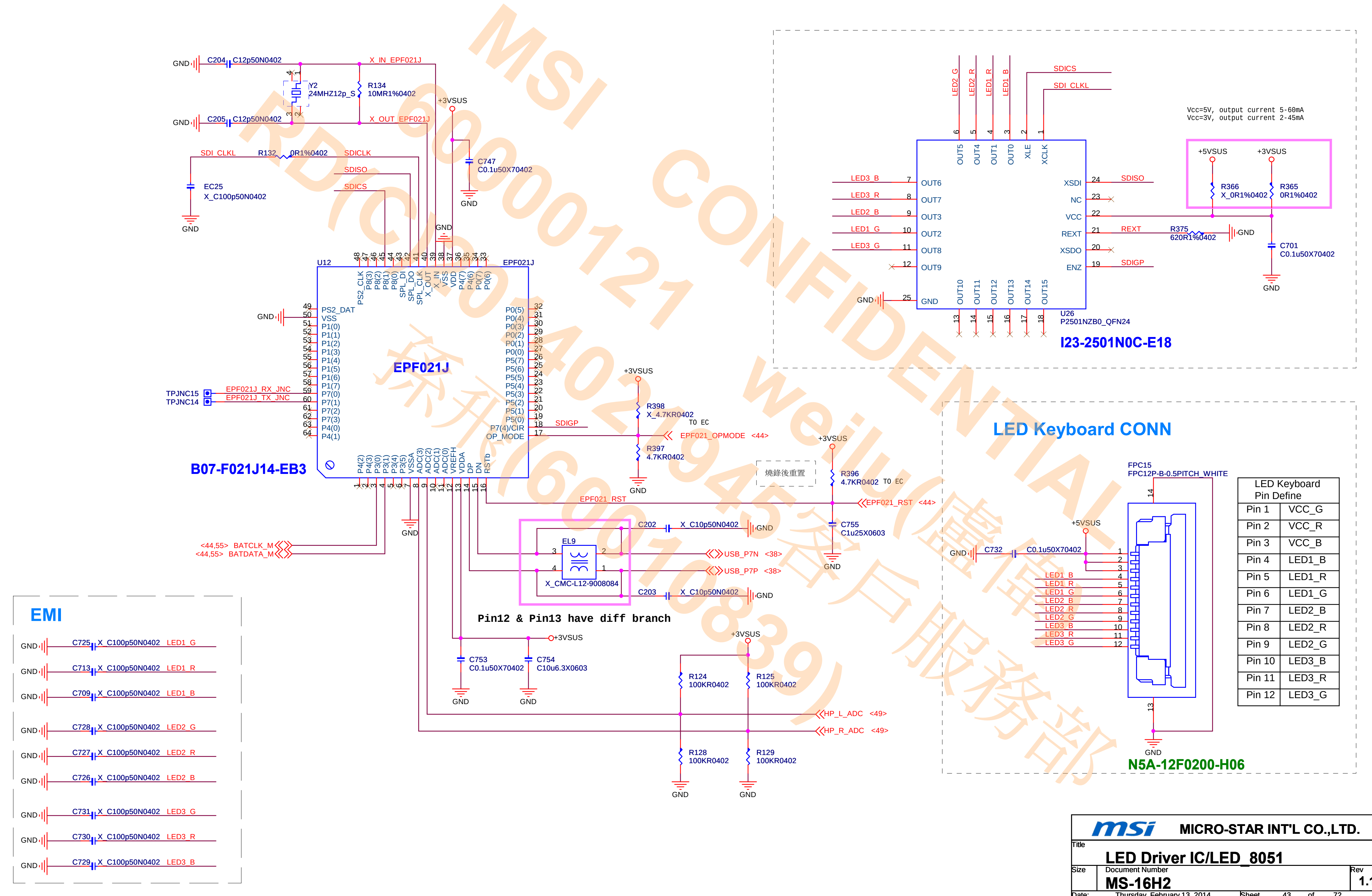
LED 8051 Controller



LED Keyboard Pin Define

Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

MICRO-STAR INT'L CO.,LTD.

Title: LED Driver IC/LED_8051

Size | Document Number: MS-16H2 | Rev: 1.1

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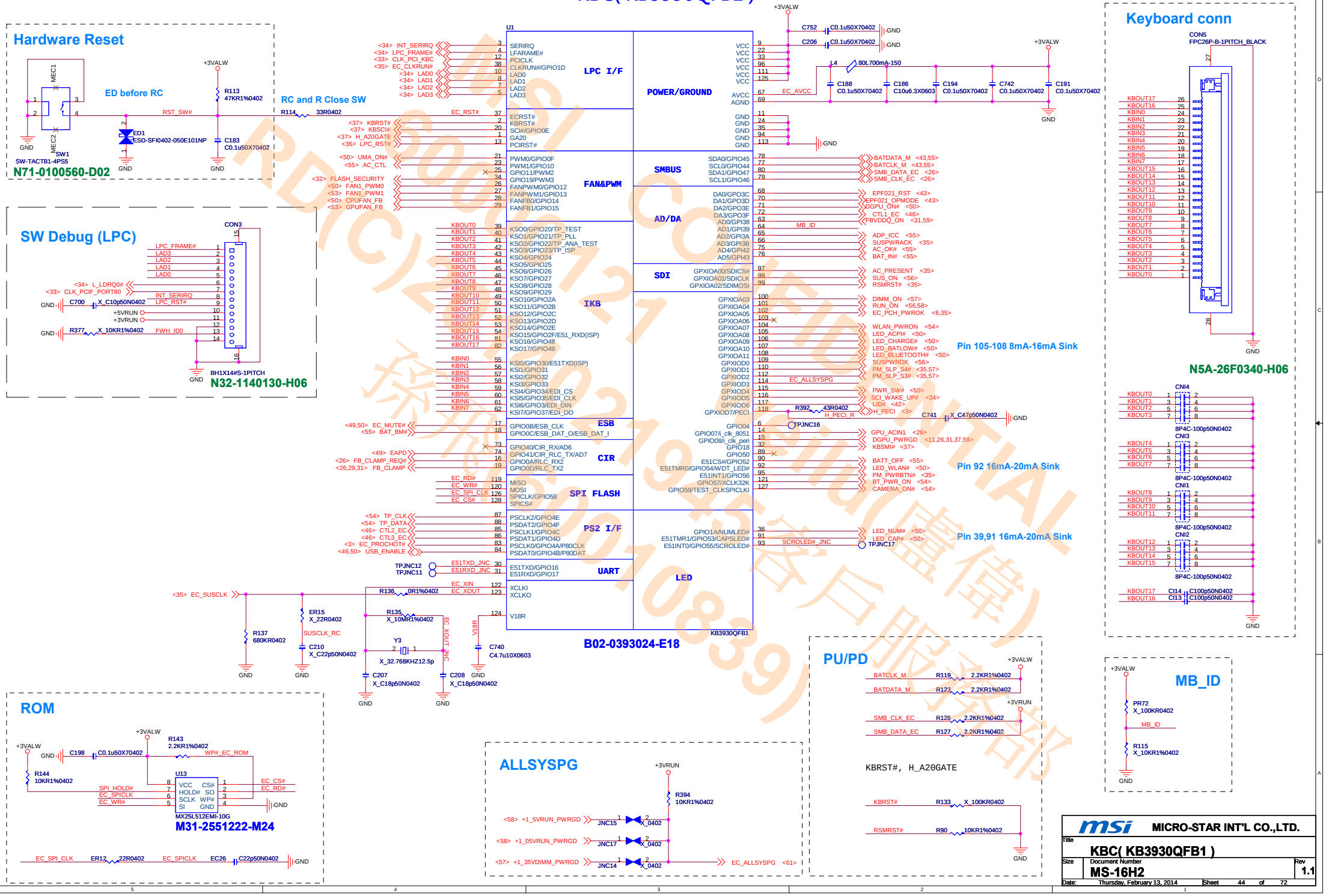
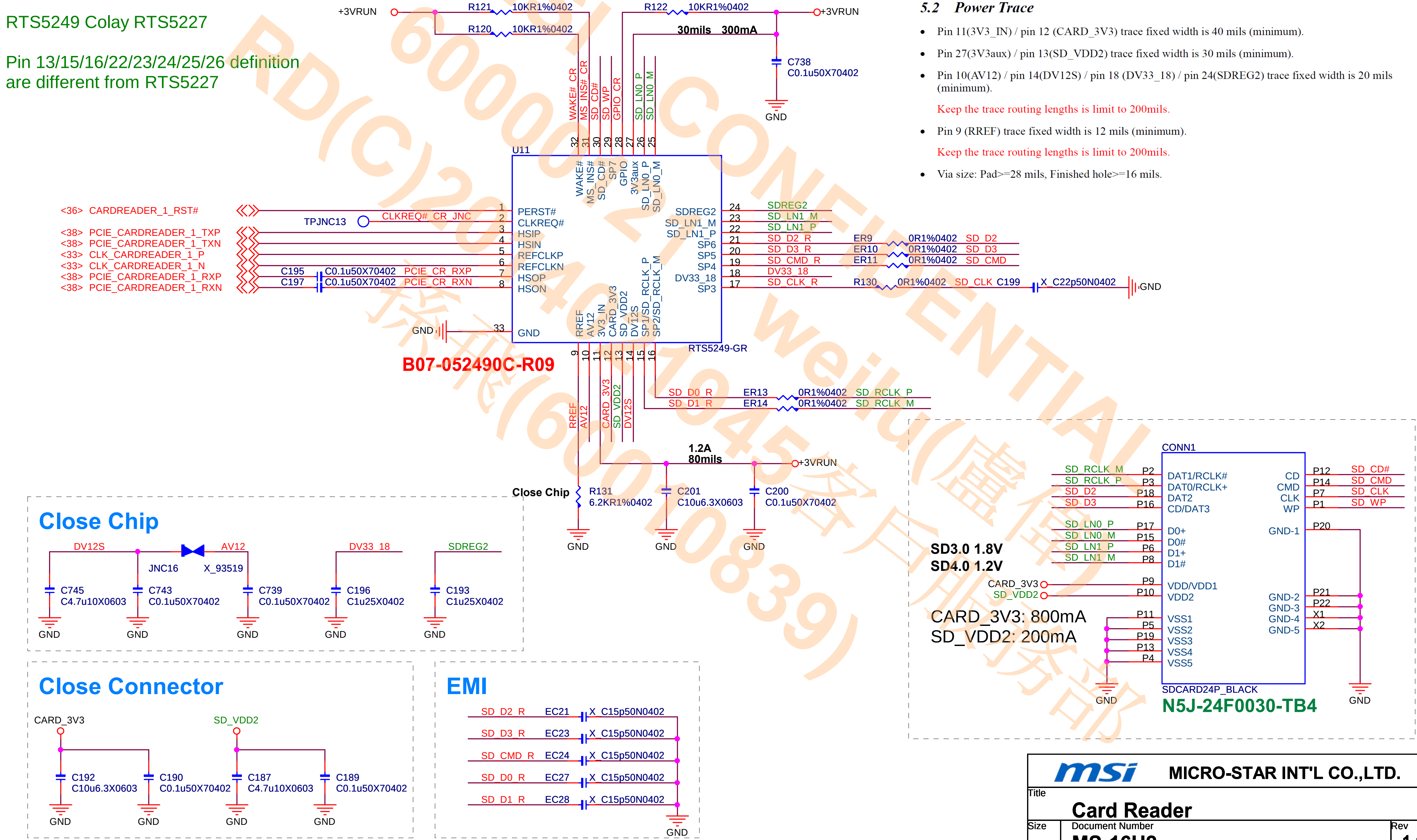
KBC(KB3930QFB1)



CardReader (RTS5249)



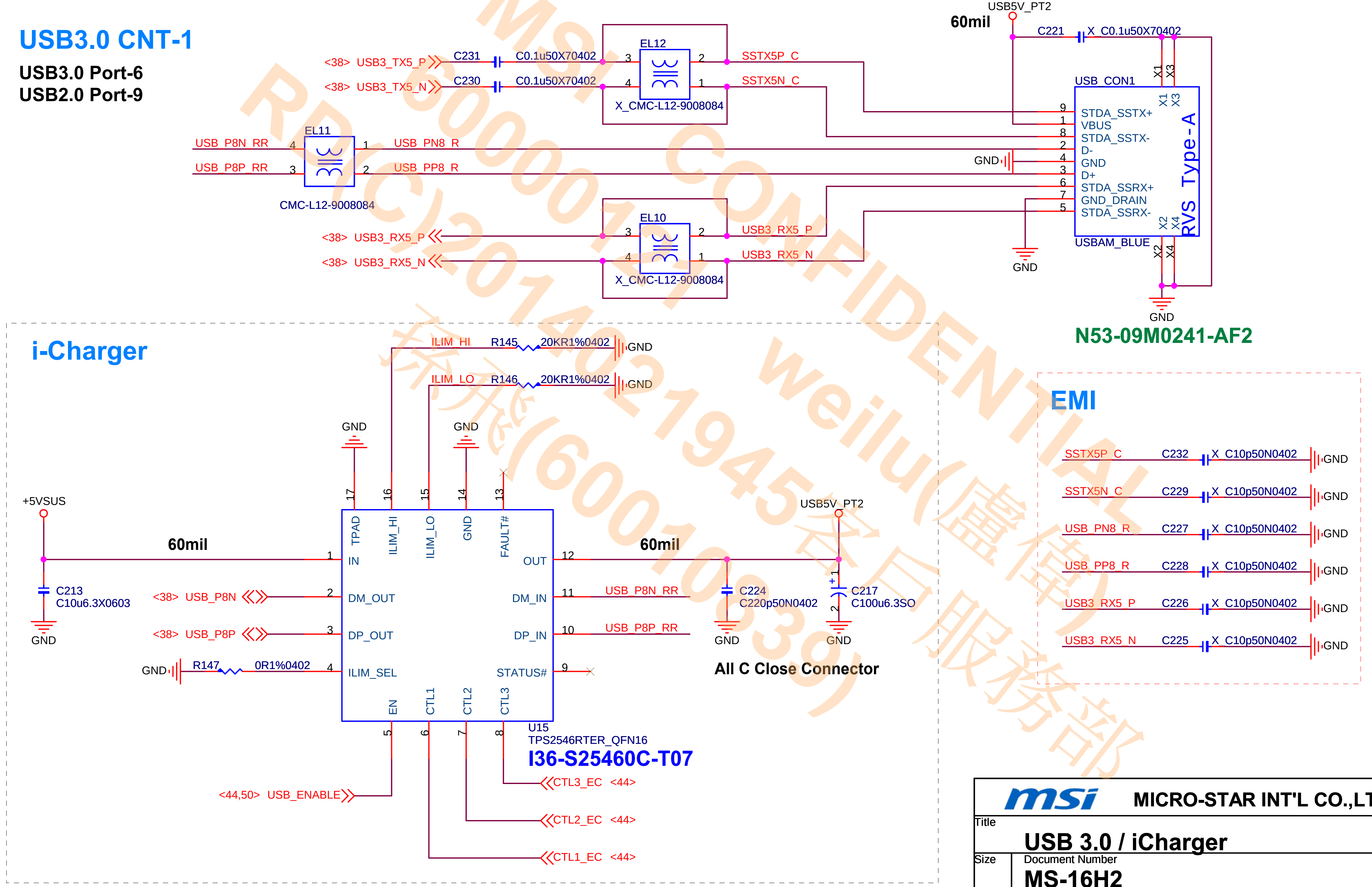
5.2 Power Trace

- Pin 11(3V3_IN) / pin 12 (CARD_3V3) trace fixed width is 40 mils (minimum).
- Pin 27(3V3aux) / pin 13(SD_VDD2) trace fixed width is 30 mils (minimum).
- Pin 10(AV12) / pin 14(DV12S) / pin 18 (DV33_18) / pin 24(SDREG2) trace fixed width is 20 mils (minimum).

  Keep the trace routing lengths is limit to 200mils.
- Pin 9 (RREF) trace fixed width is 12 mils (minimum).

  Keep the trace routing lengths is limit to 200mils.
- Via size: Pad>=28 mils, Finished hole>=16 mils.

USB 3.0 / iCharger



MICRO-STAR INT'L CO.,LTD.

Title	USB 3.0 / iCharger
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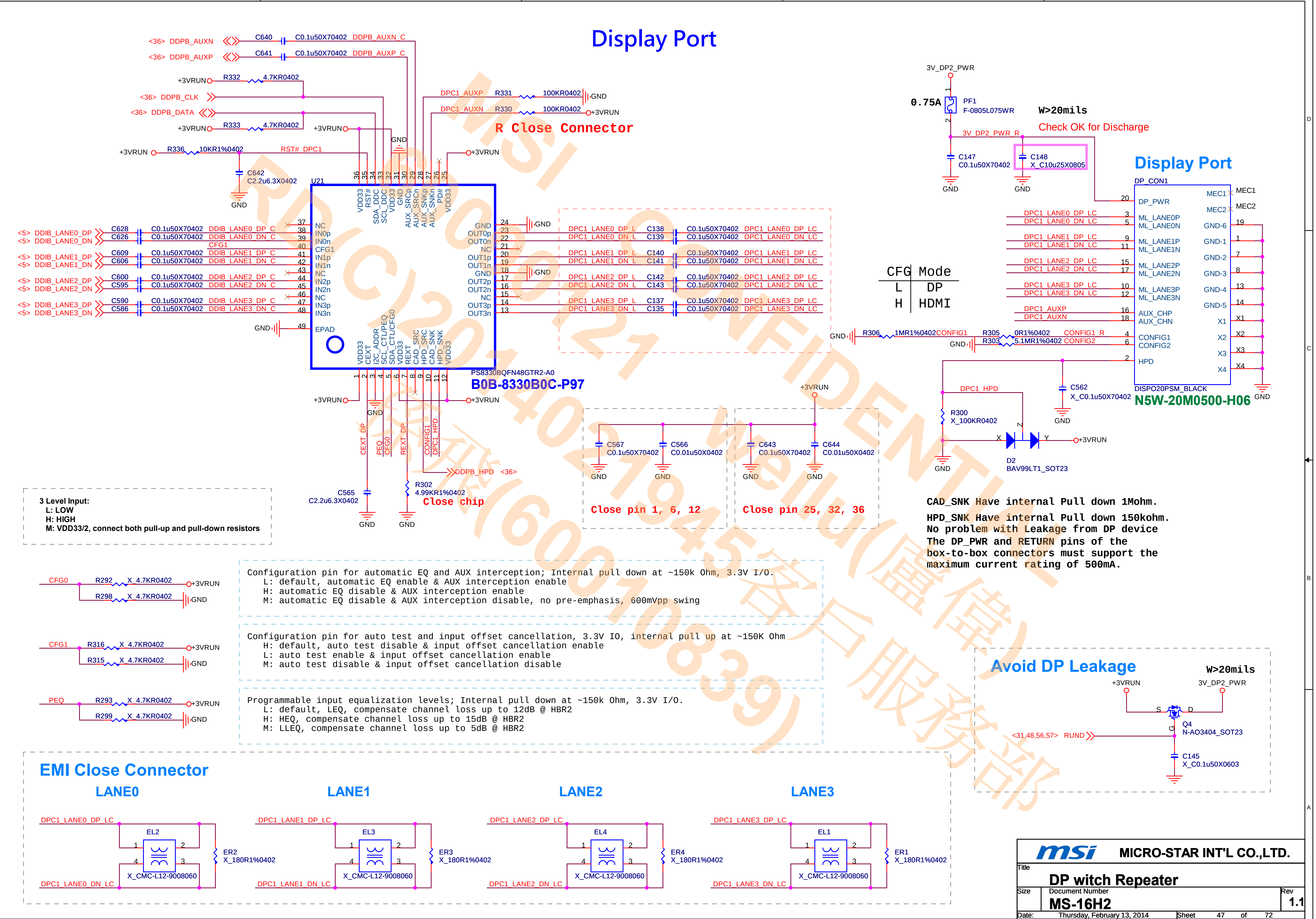
Display Port



3 Level Input:
- L: LOW
- H: HIGH
- M: VDD33/2, connect both pull-up and pull-down resistors

CAD_SNK Have internal Pull down 1Mohm.

HPD_SNK Have internal Pull down 150kohm.
No problem with Leakage from DP device
The DP_PWR and RETURN pins of the
box-to-box connectors must support the
maximum current rating of 500mA.

```
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
   L: default, automatic EQ enable & AUX interception enable
   H: automatic EQ disable & AUX interception enable
   M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing
```

```
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
   H: default, auto test disable & input offset cancellation enable
   L: auto test enable & input offset cancellation enable
   M: auto test disable & input offset cancellation disable
```

```
Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.
   L: default, LEQ, compensate channel loss up to 12dB @ HBR2
   H: HEQ, compensate channel loss up to 15dB @ HBR2
   M: LLEQ, compensate channel loss up to 5dB @ HBR2
```

MICRO-STAR INT'L CO.,LTD.

Title: DP witch Repeater

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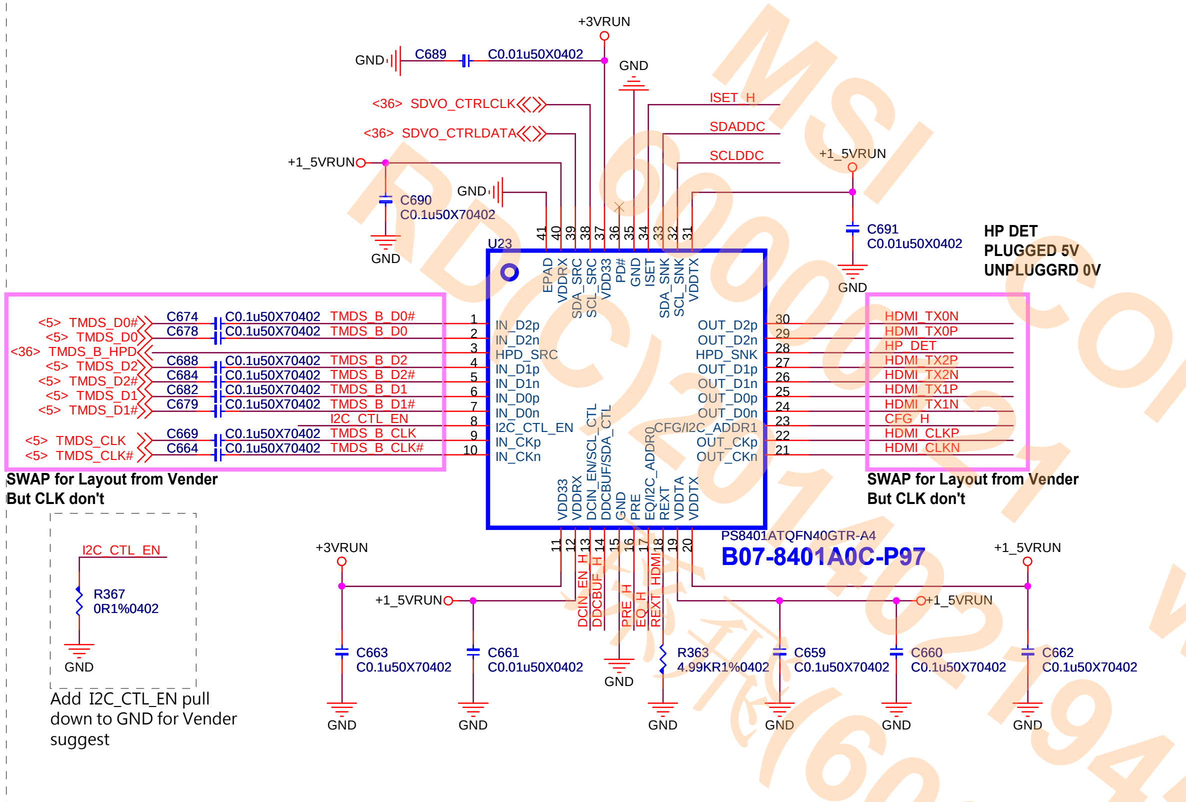
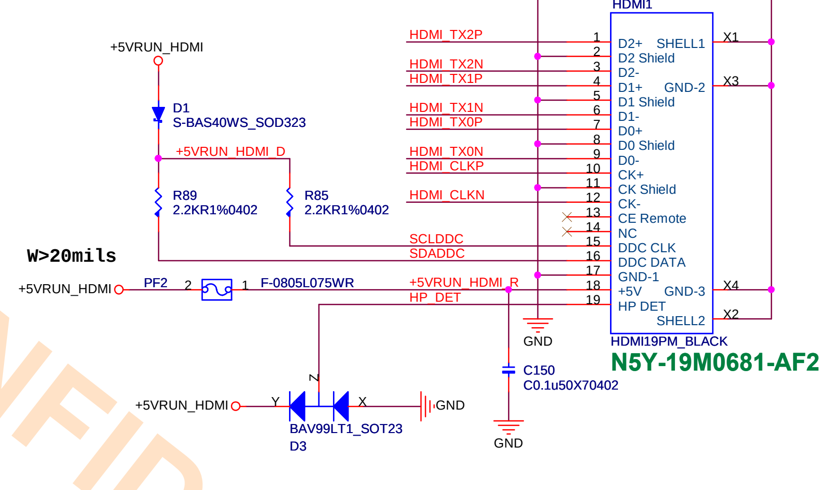
HDMI Repeater



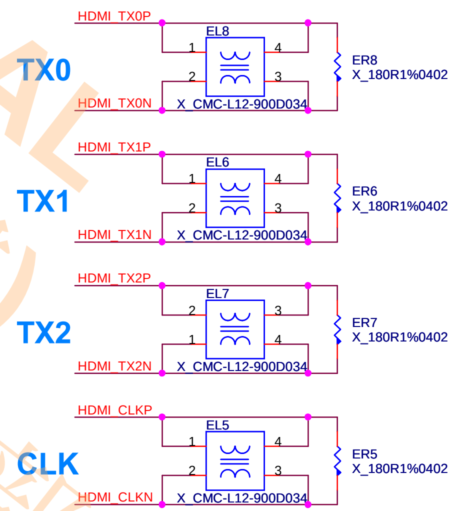
HDMI Connector

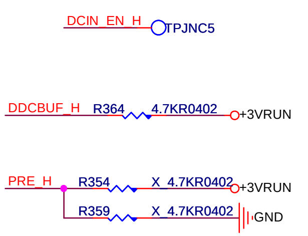


An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

HPD_SNK Internal PD 150kohm

EMI Close Connector

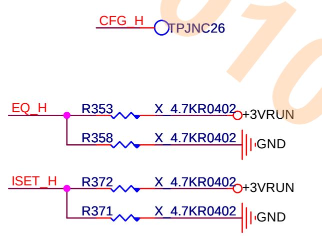




DCIN_EN:DC coupling enable (Deleted)
Internal PD at 150kohm
L:Default, AC coupling input
H:DC coupling input

Enable active DDC buffer , Internal PD at 150kohm
L:Default, passive DDC pass-through
H:Active DDC buffer with default threshold
M:Active DDC buffer without internal pull up resistor

PRE:output pre-emphasis setting Internal PD at 150kohm
L:No pre-emphasis
H:1.6dB pre-emphasis
M:2.5dB pre-emphasis



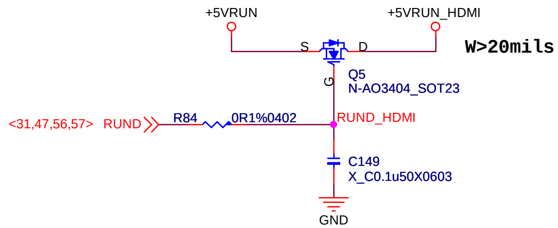
Configuation pin (Deleted)
Internal PD at 150kohm
L:HDMI ID disable
H:HDMI ID enable

Receiver equalization setting
Internal PD at 150kohm
L:programmable EQ for channel loss up to 12.4dB
H:programmable EQ for channel loss up to 4.3dB
M:programmable EQ for channel loss up to 48.6dB

TMDS output swing adjustment
Internal PD at 150kohm
L:Default
H:Increase +13%
M:reduce -13%

ADDR1 (CFG)	ADDR0 (EQ)	I2C control bus address (Internal pull down at ~150kΩ, 3.3V I/O)
0	0	0x4C / 4D (default)
0	1	0x5C / 5D
1	0	0xCC / CD
1	1	0xEC / ED

Avoid HDMI Leakage



MICRO-STAR INT'L CO.,LTD.

Title: HDMI Repeater

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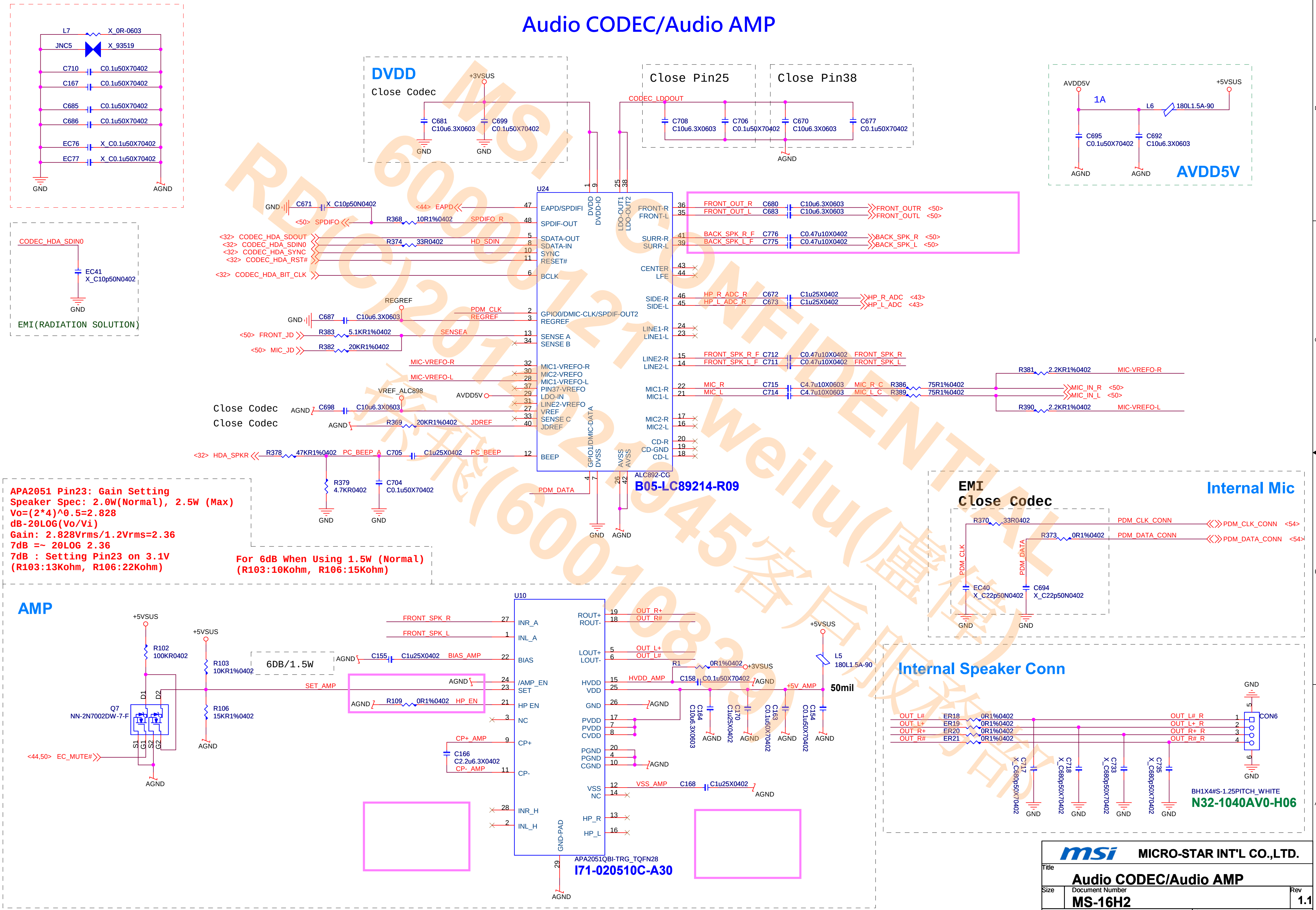
Audio CODEC/Audio AMP



APA2051 Pin23: Gain Setting
Speaker Spec: 2.0W(Normal), 2.5W (Max)
Vo=(2*4)^0.5=2.828
dB-20LOG(Vo/Vi)
Gain: 2.828Vrms/1.2Vrms=2.36
7dB =~ 20LOG 2.36
7dB : Setting Pin23 on 3.1V
(R103:13Kohm, R106:22Kohm)

For 6dB When Using 1.5W (Normal)
(R103:10Kohm, R106:15Kohm)

MICRO-STAR INT'L CO.,LTD.

Title	Audio CODEC/Audio AMP
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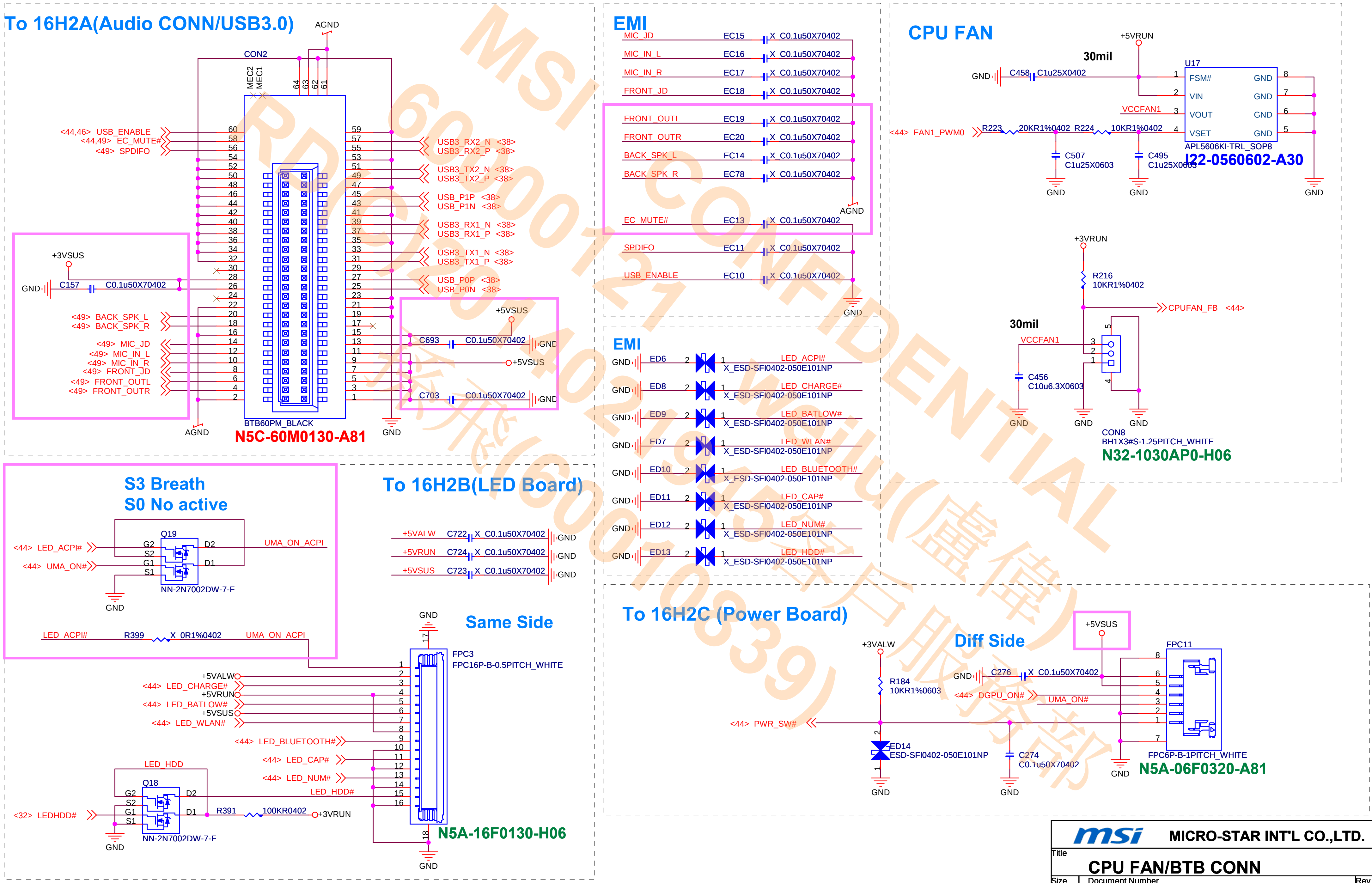
CPU FAN/BTB CONN



MICRO-STAR INT'L CO.,LTD.		
Title: CPU FAN/BTB CONN		
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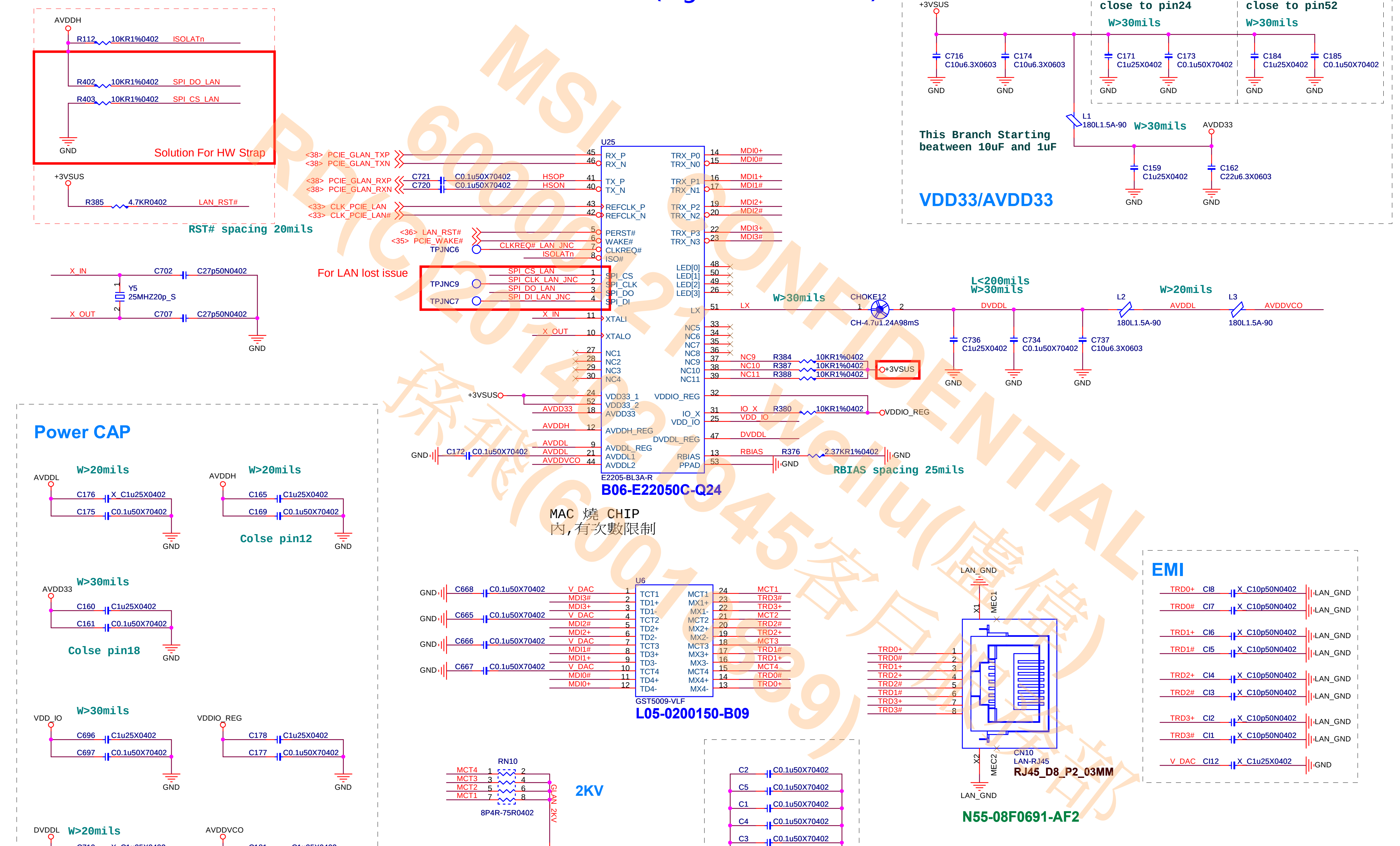
GIGA LAN(BigFoot BFN2205B)



MICRO-STAR INT'L CO.,LTD.

Title	GIGA LAN(BigFoot BFN2205B)	
Size	Document Number MS-16H2	Rev 1.1
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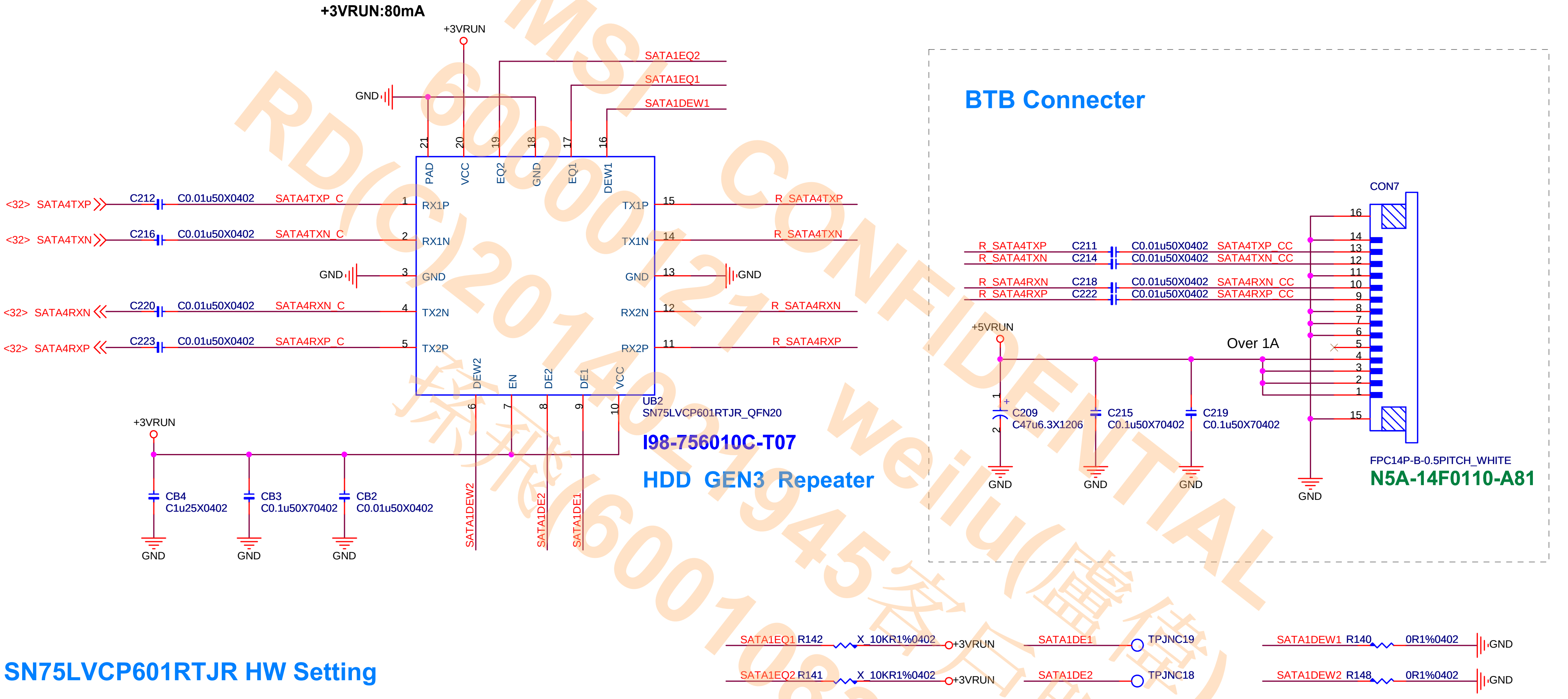
HDD (With Repeater)



TI SN75LVCP601RTJR HW Setting

DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	EQ1/EQ2	CH1/CH2Equalization dB (at 6Gbps)
NC (***default***)	–4	NC (***default***)	0
0	0	0	7
1	–2	1	14

DEW1/DEW2	Device Function → DE Width for CH1/CH2
0	De-emphasis pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps)
1 (***default***)	De-emphasis pulse duration, long (recommended setting when link operates at SATA 1.5/3 Gbps speed only)

MICRO-STAR INT'L CO.,LTD.

Title: HDD With Repeater

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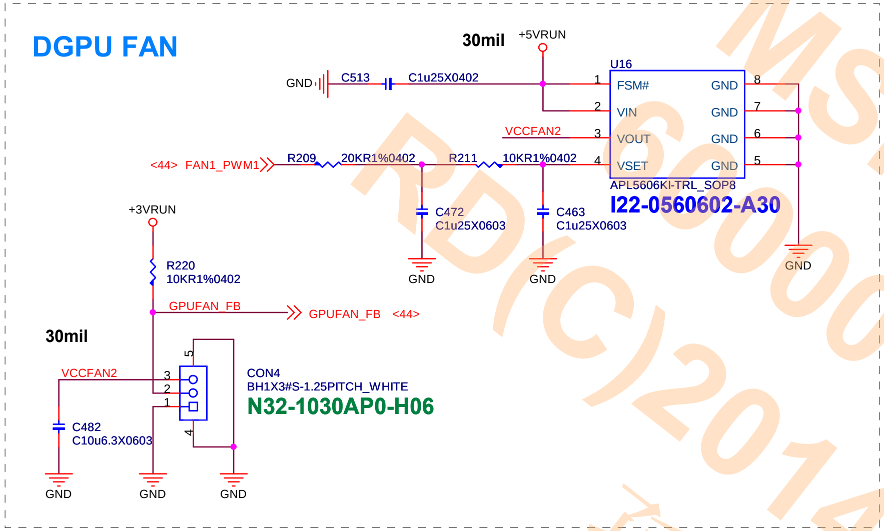
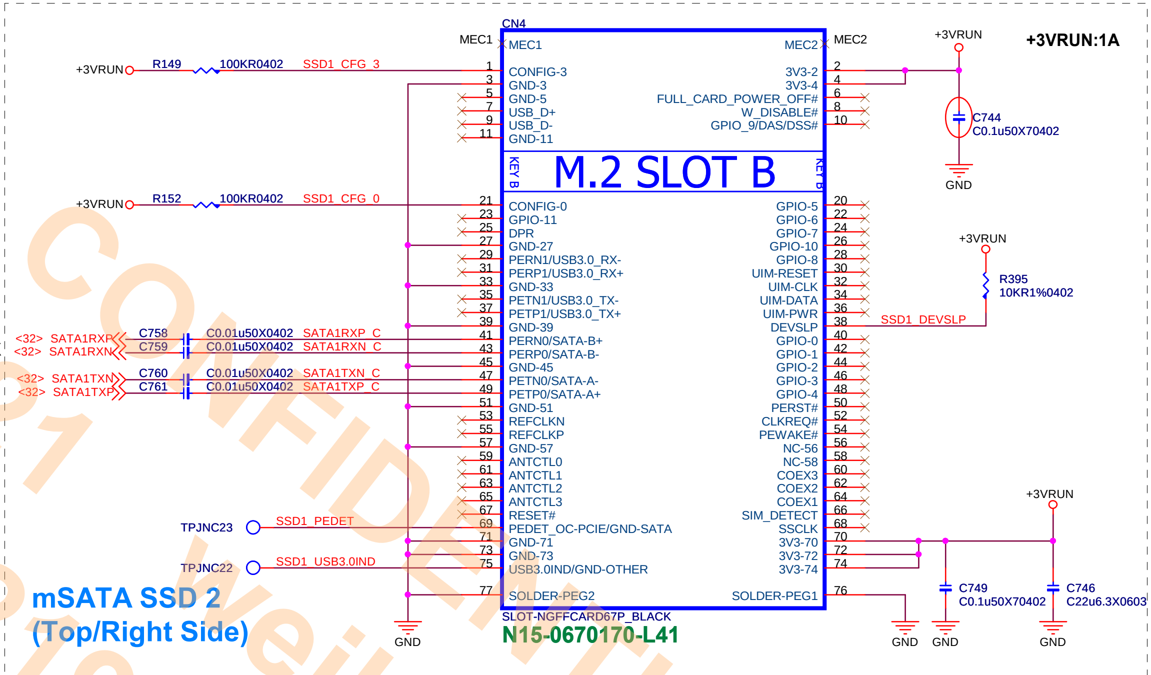
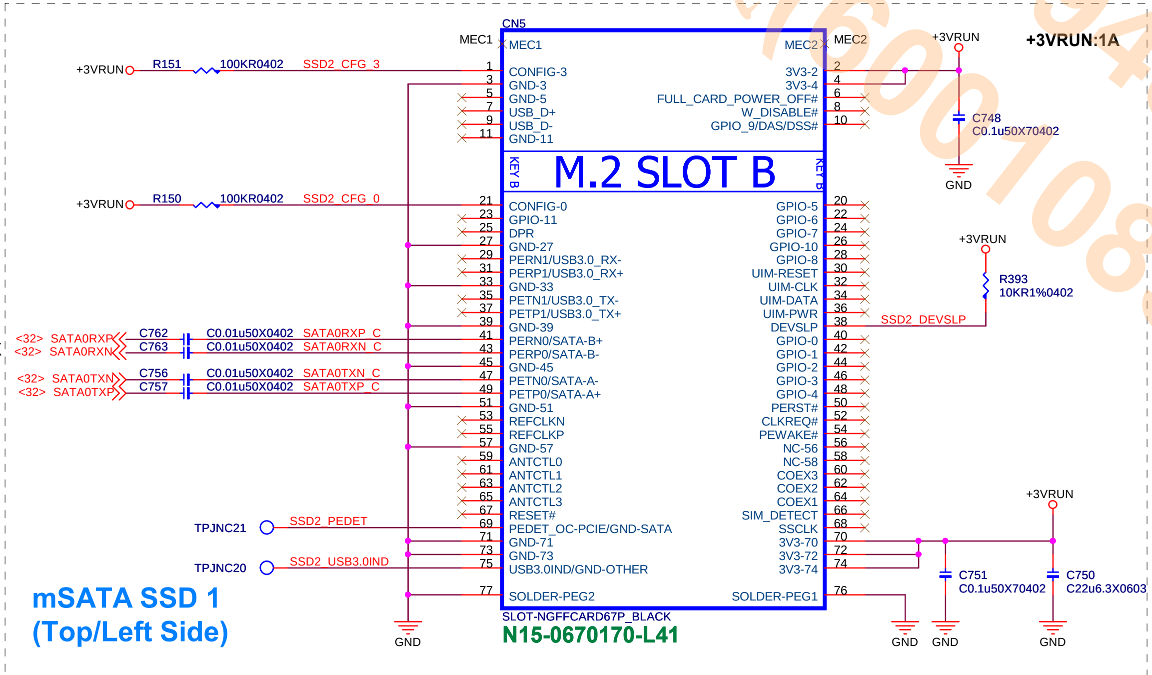
SSD/ DGPU FAN







40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host transmitter differential signal pair

MICRO-STAR INT'L CO.,LTD.

Title: SSD/ DGPU FAN

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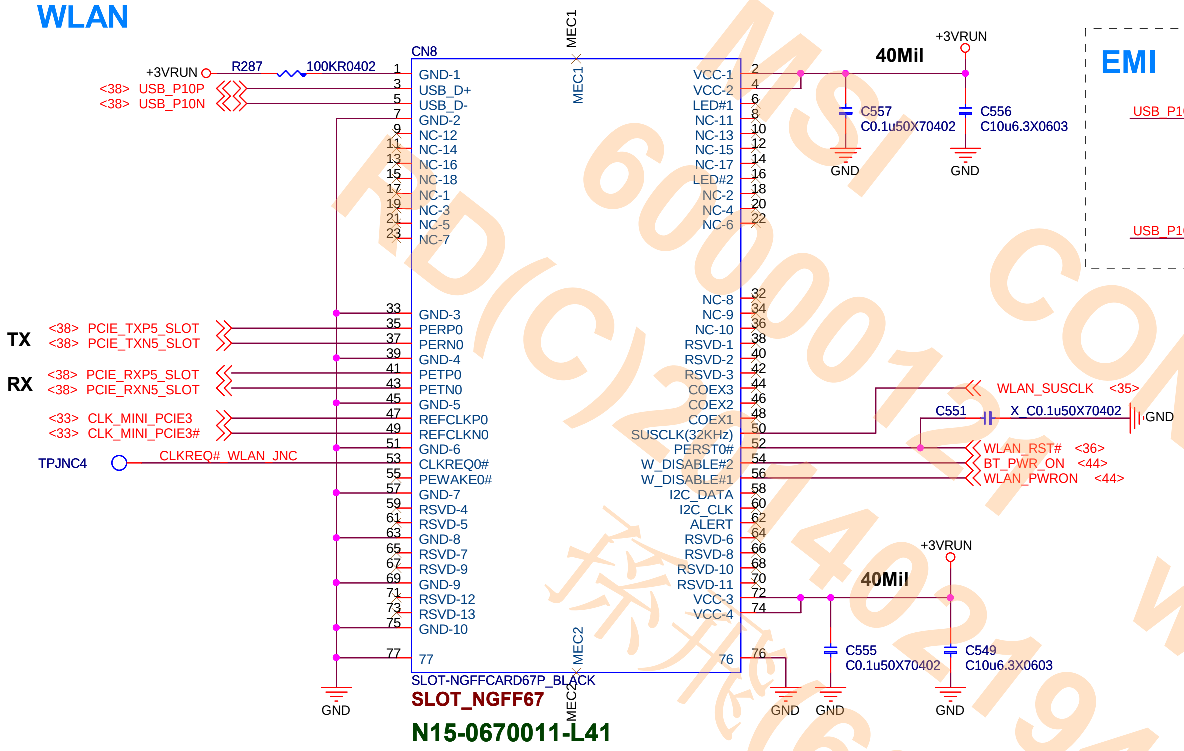
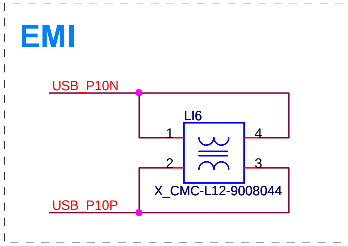
WLAN /Camera/ClickPad/FP

WLAN

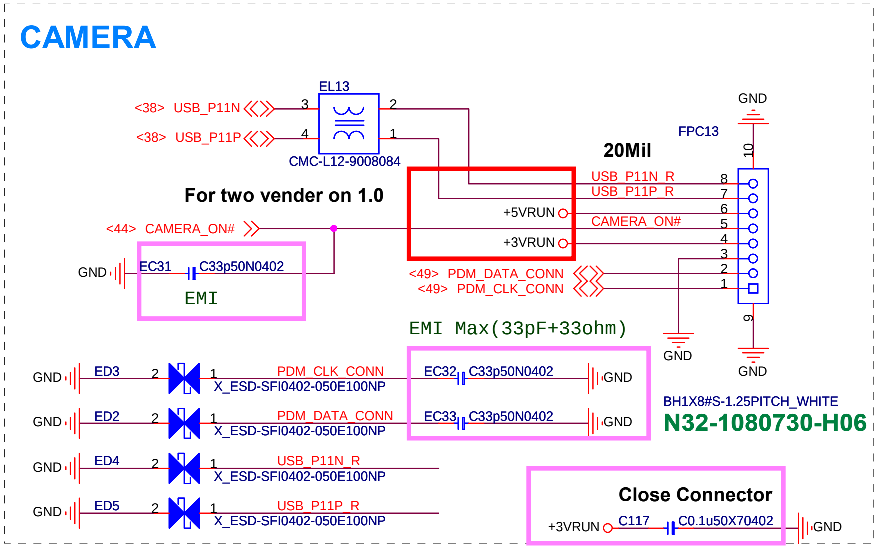


Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

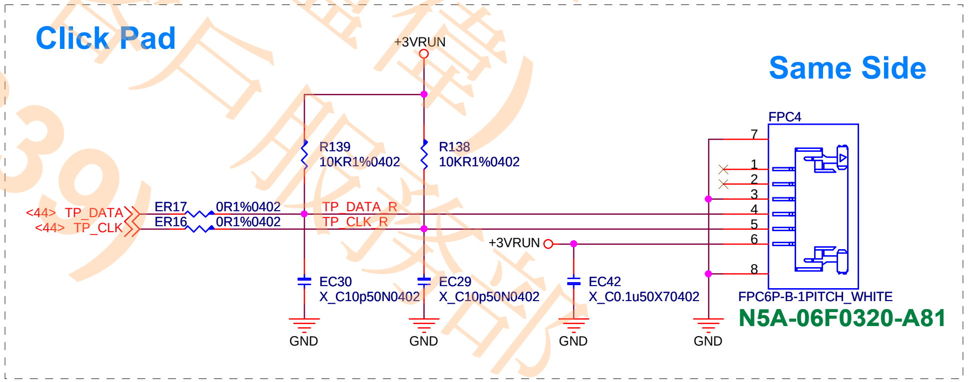
EMI



CAMERA



Click Pad



MICRO-STAR INT'L CO.,LTD.

Title: WLAN /Camera/ClickPad/FP

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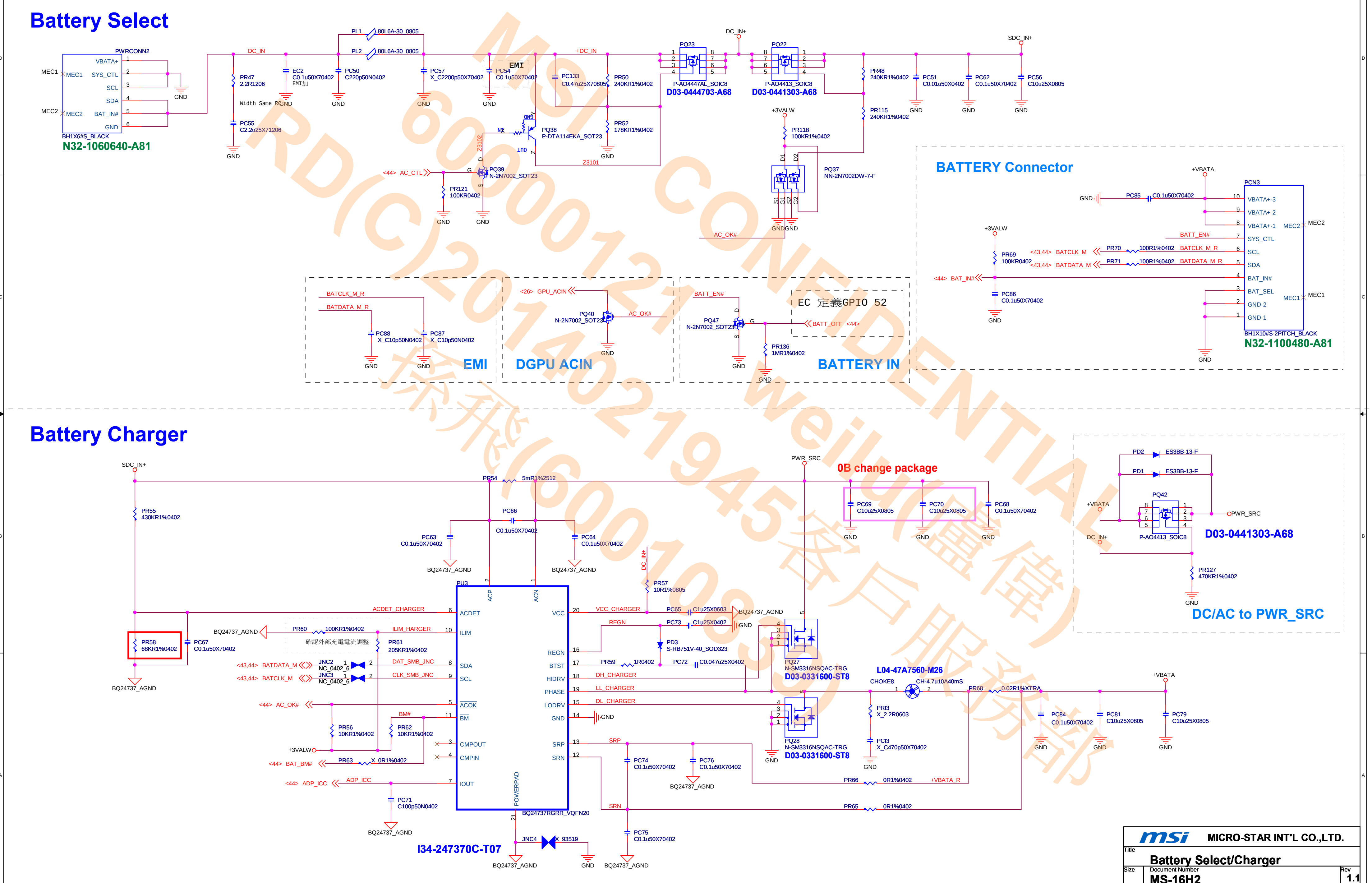
Battery Select/Charger



MSI MICRO-STAR INT'L CO.,LTD.

Title: Battery Select/Charger

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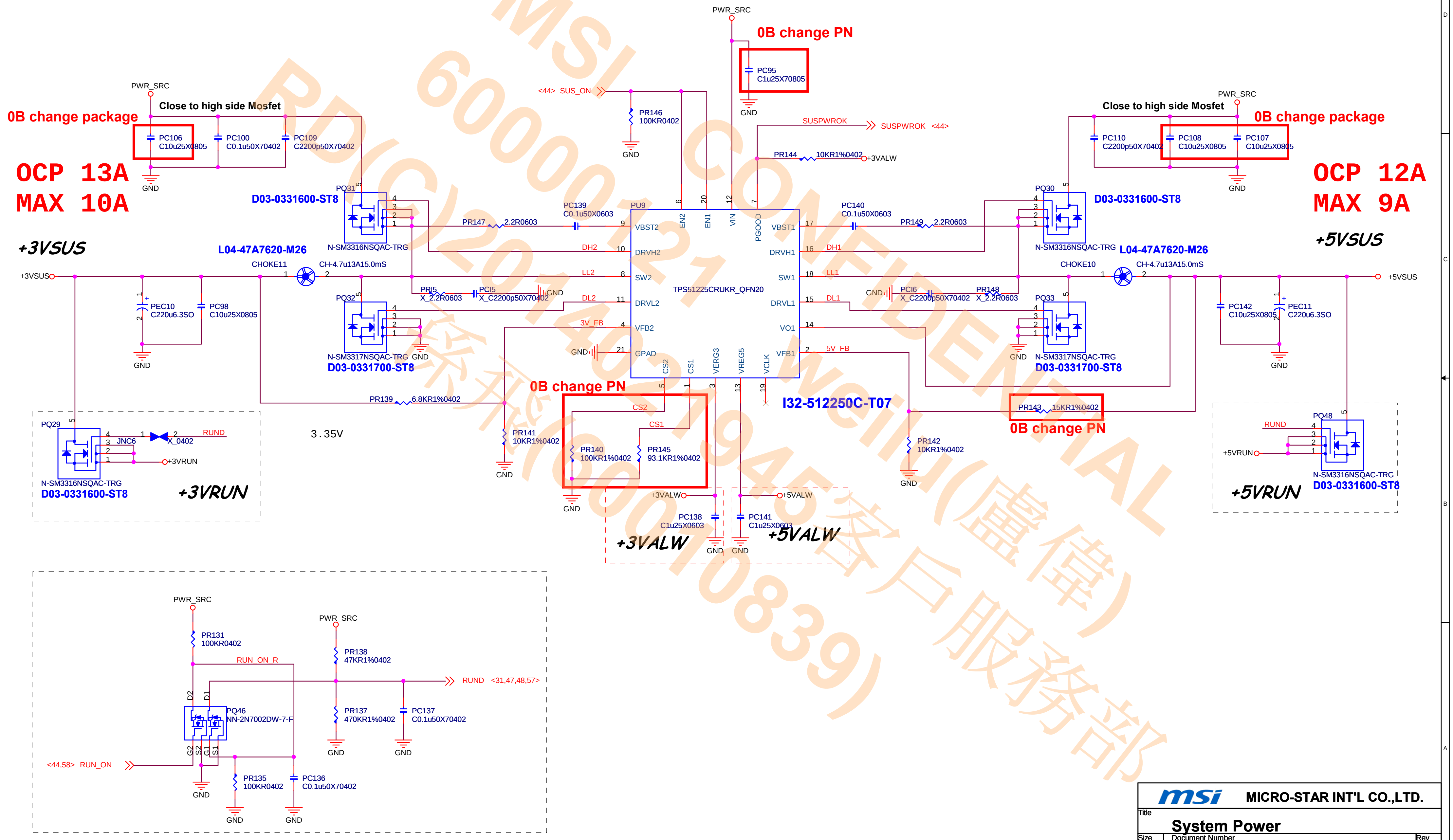
System Power



MICRO-STAR INT'L CO.,LTD.

Title: System Power

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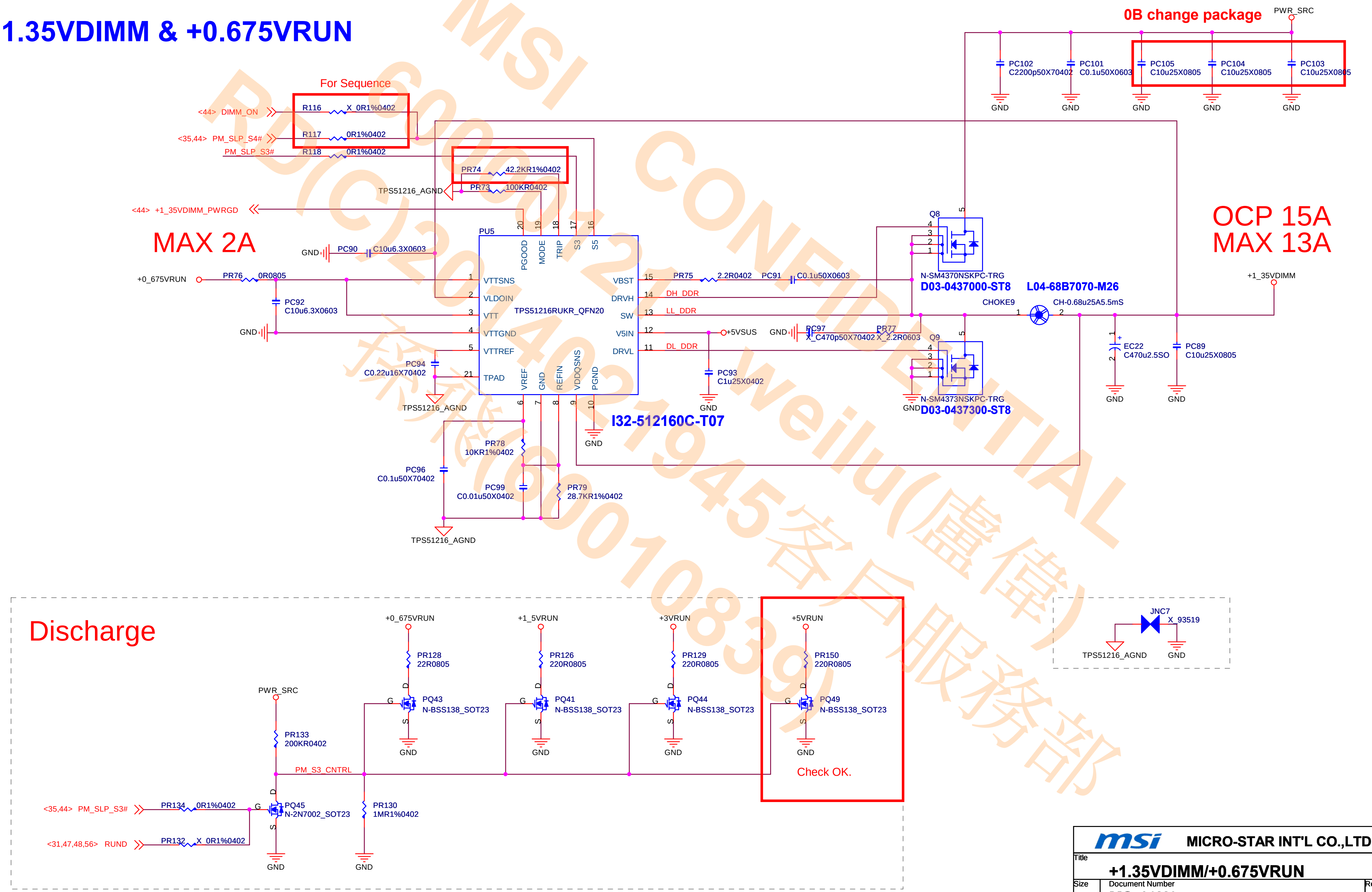
+1.35VDIMM/+0.675VRUN

+1.35VDIMM & +0.675VRUN



msi	MICRO-STAR INT'L CO.,LTD.	
Title	+1.35VDIMM/+0.675VRUN	
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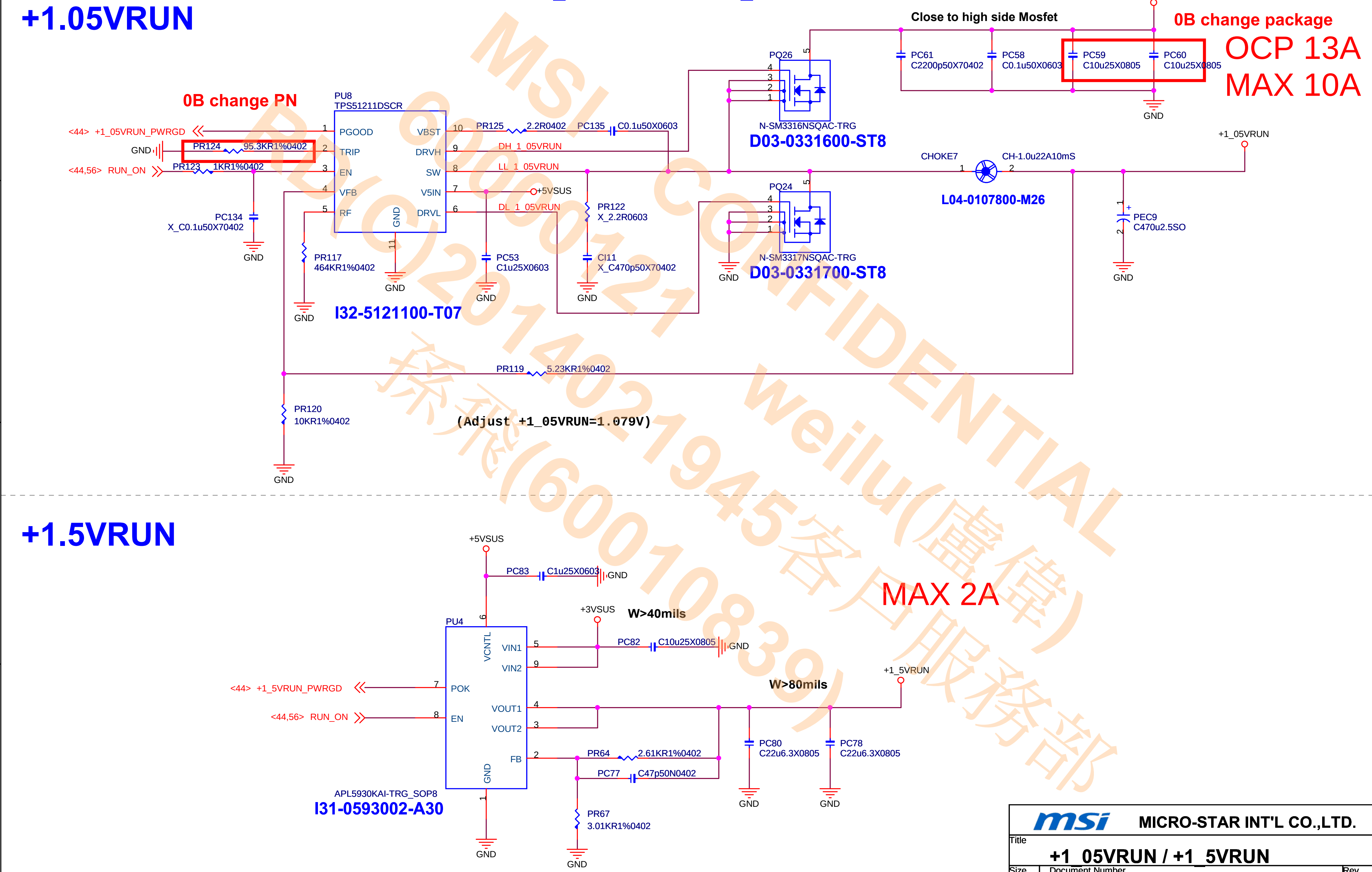
+1_05VRUN / +1_5VRUN

+1.05VRUN



msi	MICRO-STAR INT'L CO.,LTD.
Title	+1_05VRUN / +1_5VRUN
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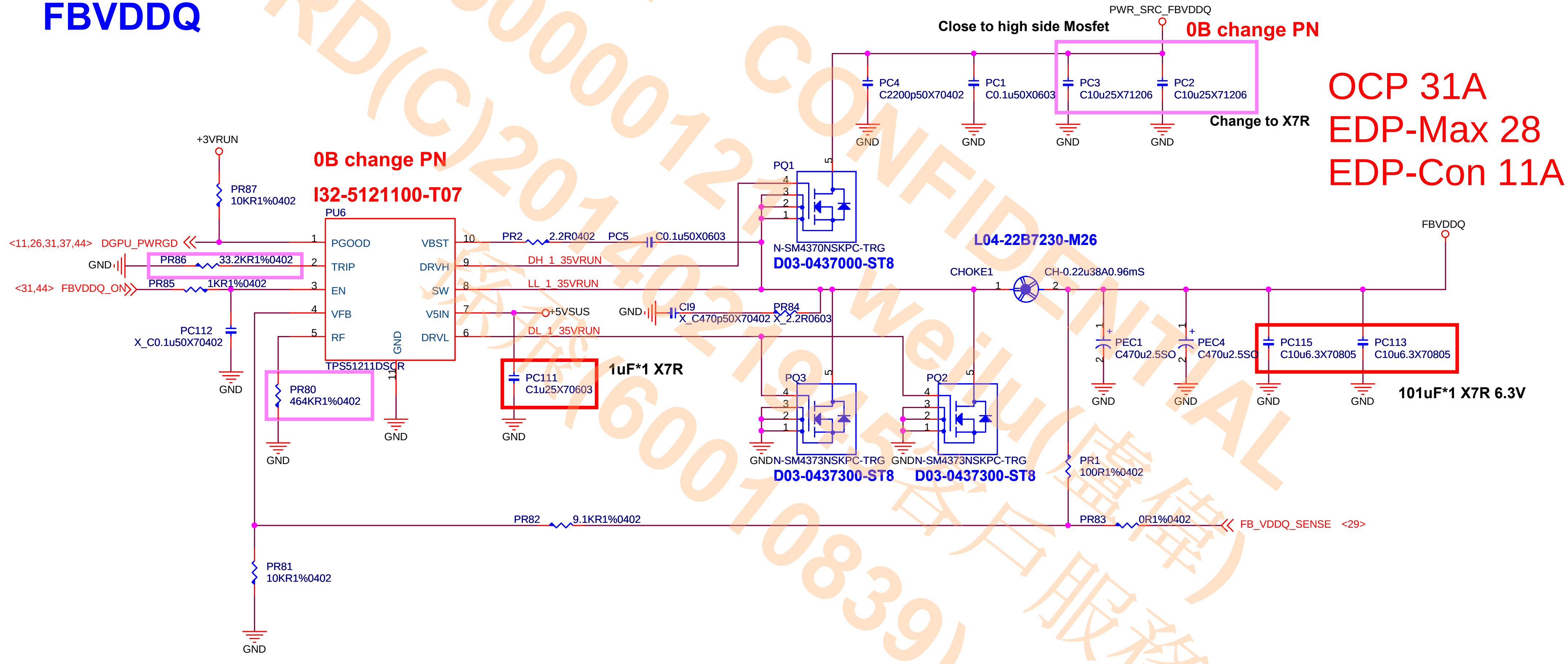
DGPU POWER FBVDDQ

FBVDDQ



MICRO-STAR INT'L CO.,LTD.

Title	DGPU POWER FBVDDQ	
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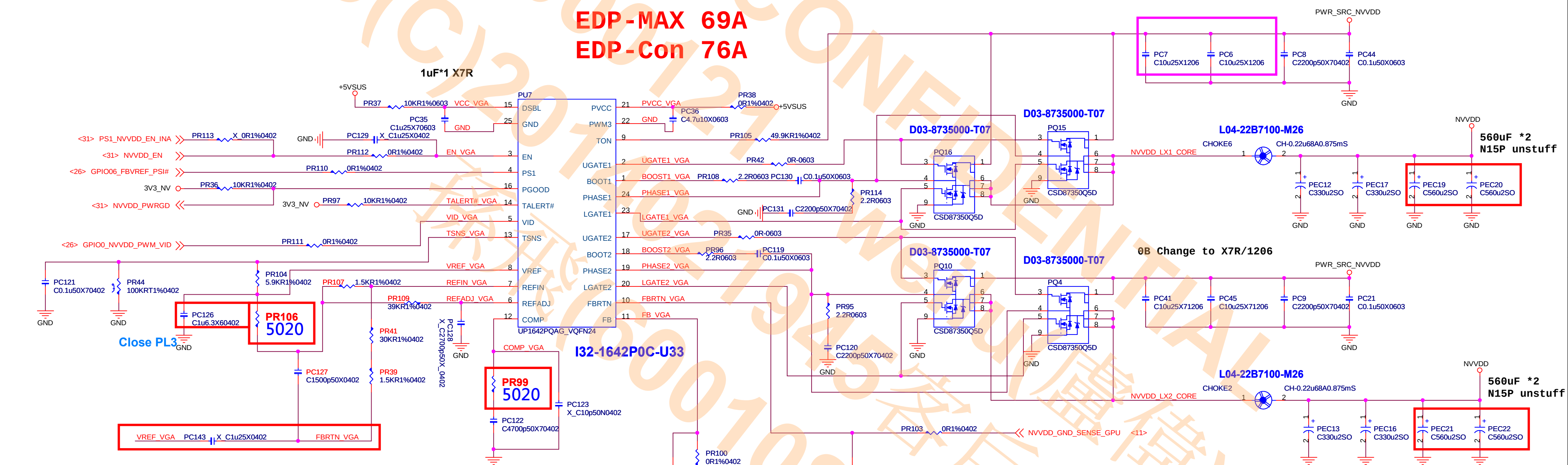
DGPU POWER NVVDD

DGPU POWER / UP1642PQAG

CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

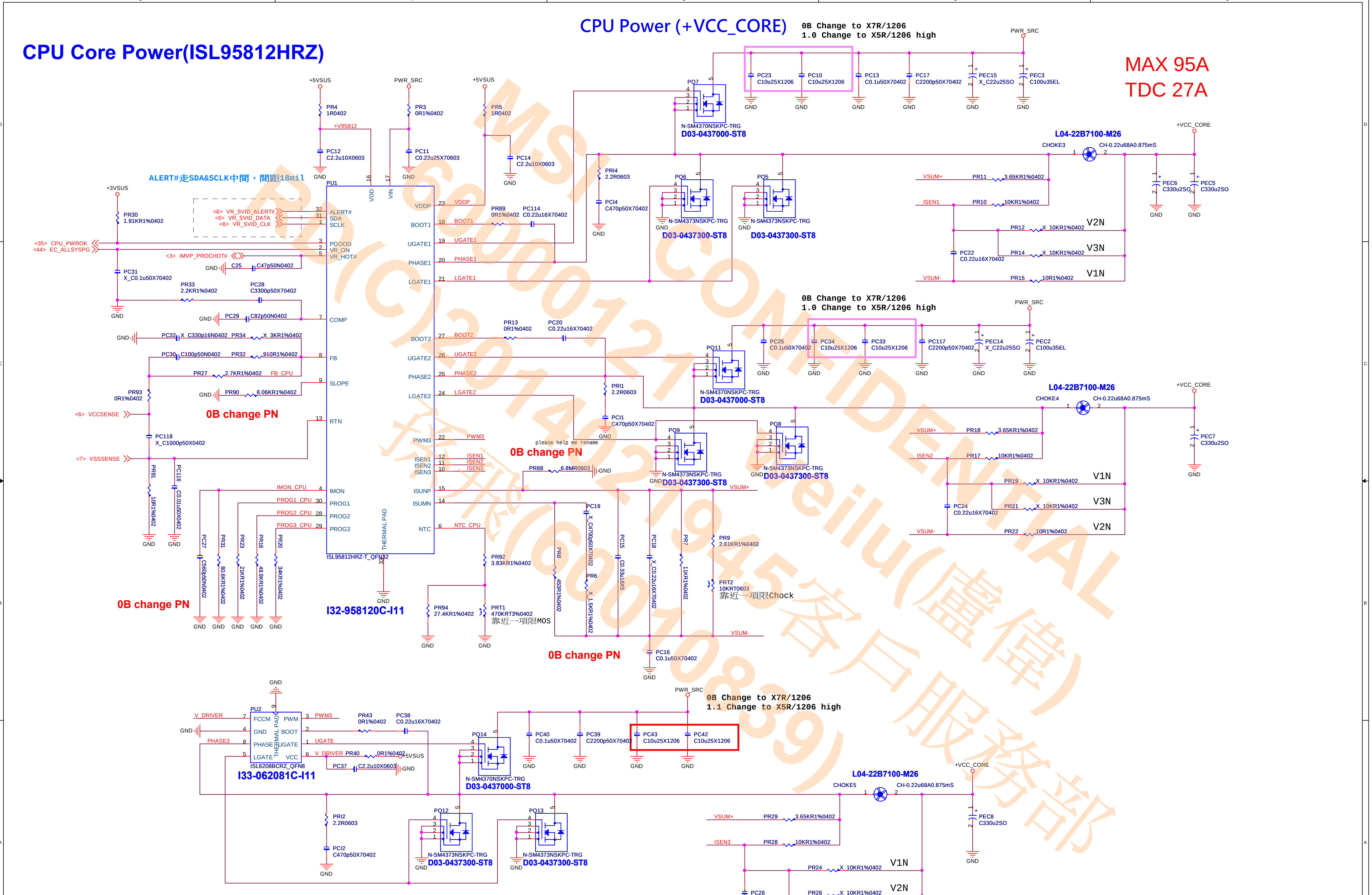
EDP-Peak 135A
EDP-MAX 69A
EDP-Con 76A



	PR109	PR106	PR107	PR41	PR39	PC127
CONFIG	R1	R2	R3	R4	R5	C
N15E-GT N15P-GX-B	39K	39K	1.5K	30K	1.5K	1.5nF

N15E-GT	N15P-GX-B
RCOMP1	RCOMP2
R11-0203T12-W08	R11-0163T12-W08
X_20KR1%0402	X_16KR1%0402
ROFFSET1	ROFFSET2
R11-0363T12-W08	R11-0393T12-W08
X_36KR1%0402	X_39KR1%0402

CPU Core Power(ISL95812HRZ)



msi MICRO-STAR INT'L CO.,LTD.

Title	CPU Power (ISL95812HRZ)	
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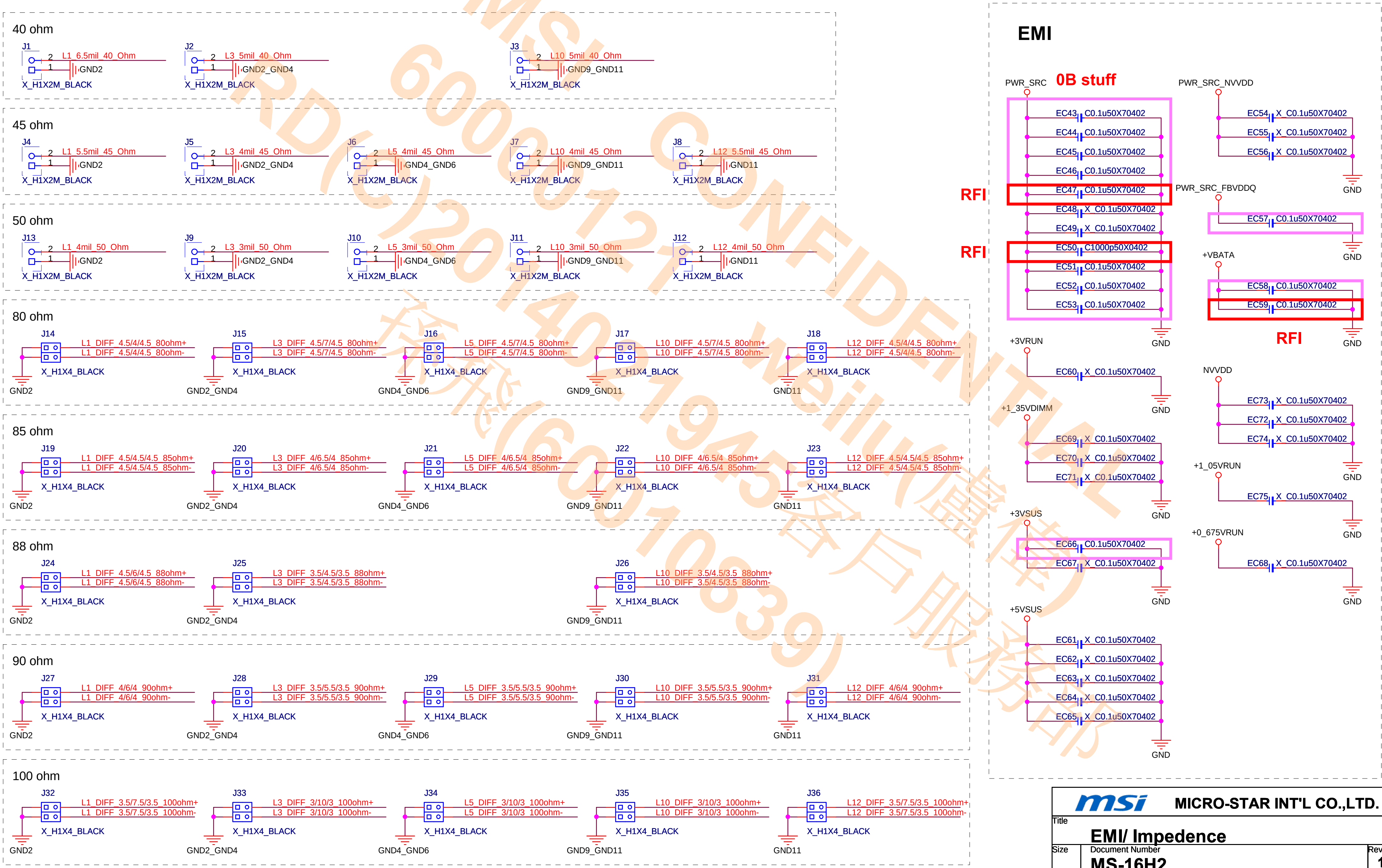
EMI/ Impedence

Impedence Connector No PN



msi MICRO-STAR INT'L CO.,LTD.

Title	EMI/ Impedence	
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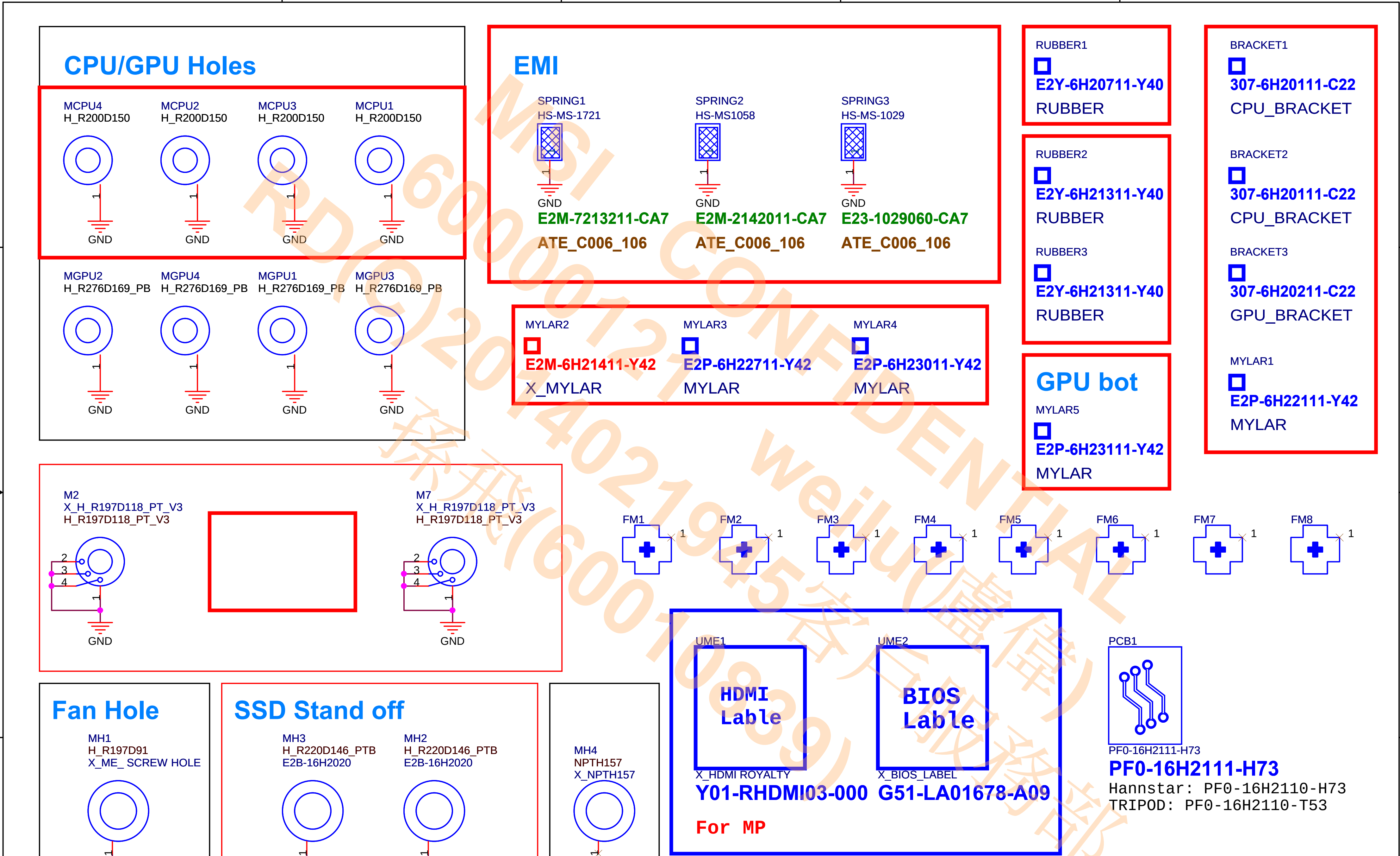

MICRO-STAR INT'L CO.,LTD.

Title: Screw/ME

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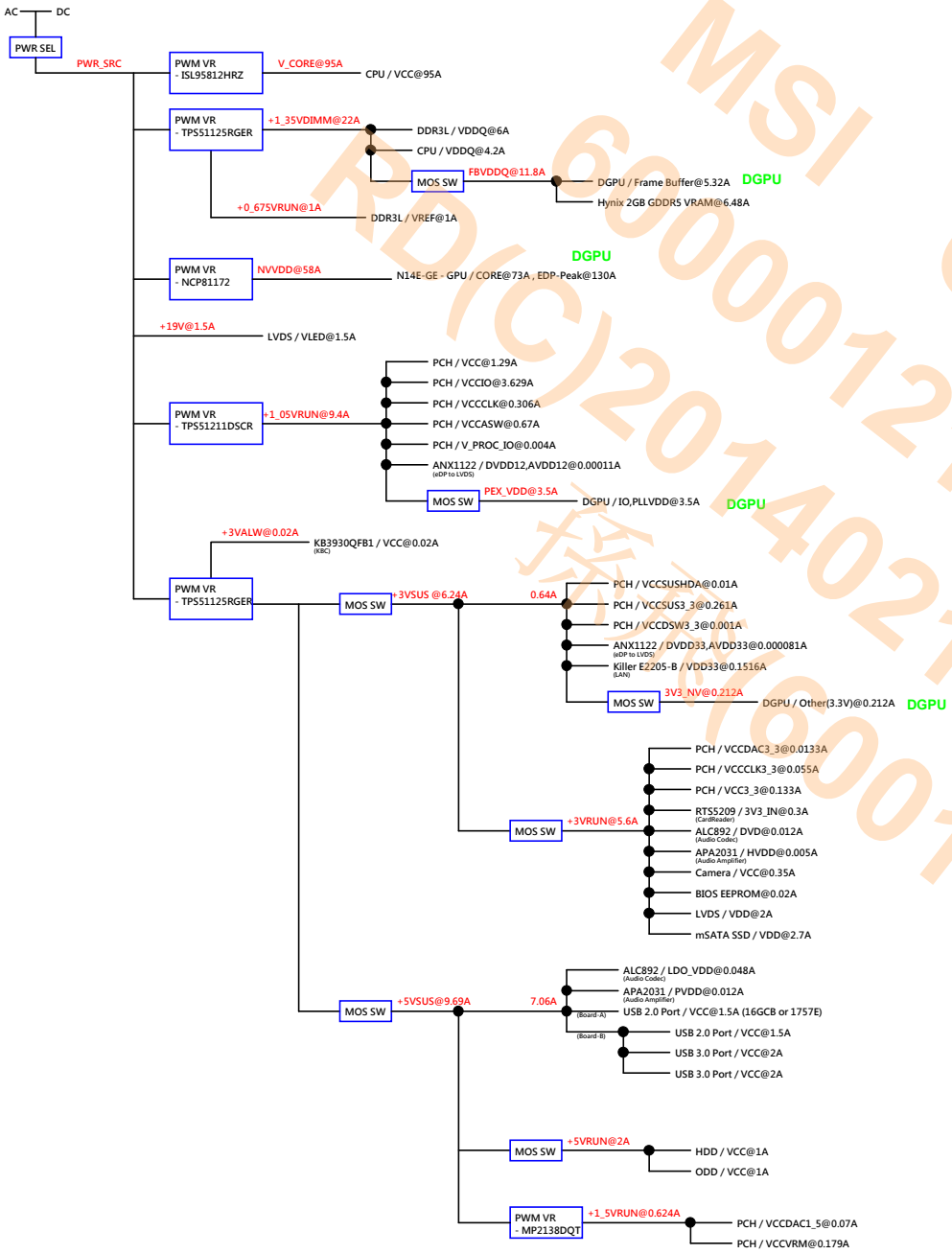
MS-16H2 Power Delivery Chart



msi	MICRO-STAR INT'L CO.,LTD.	
File	Power Delivery Map	
Size	Document Number: MS-16H2	Rev: 1.1
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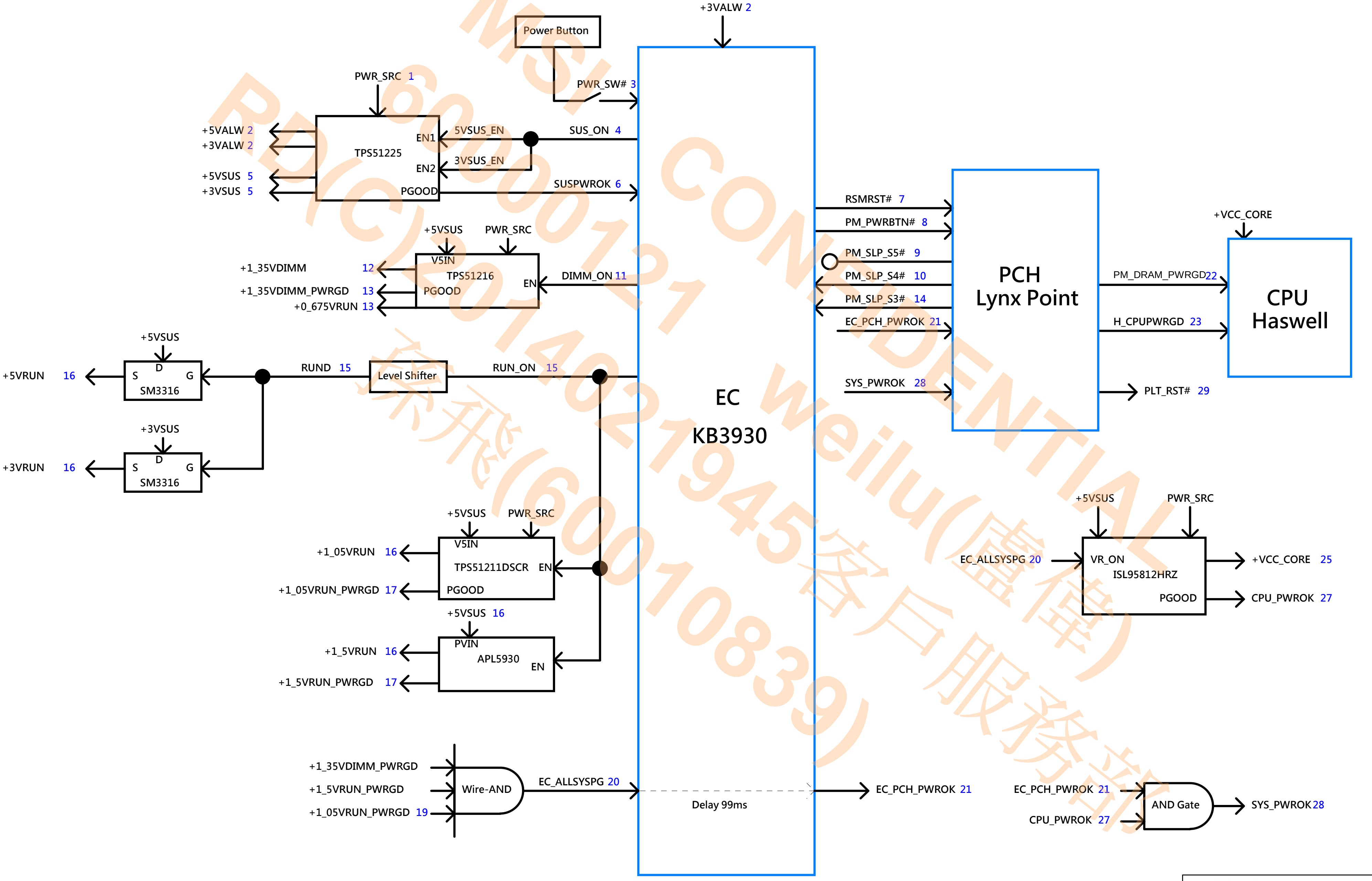
MS-16H2 Power on Block Diagram



MICRO-STAR INT'L CO.,LTD.

Title: Power on Block Diagram

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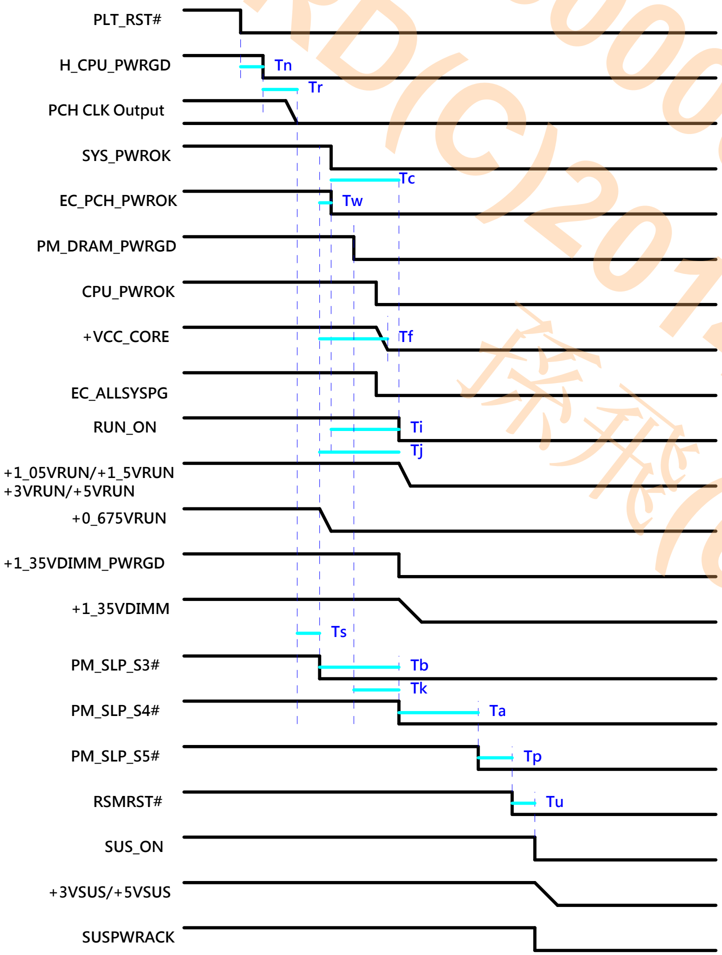
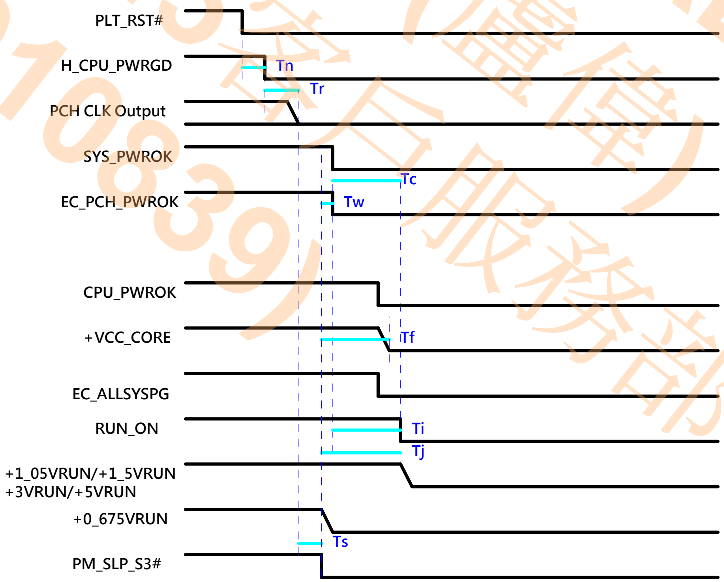
Power down Sequence

	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

S0 -> G3



S0 -> S3



msi	MICRO-STAR INT'L CO.,LTD.
Title	Power down Sequence
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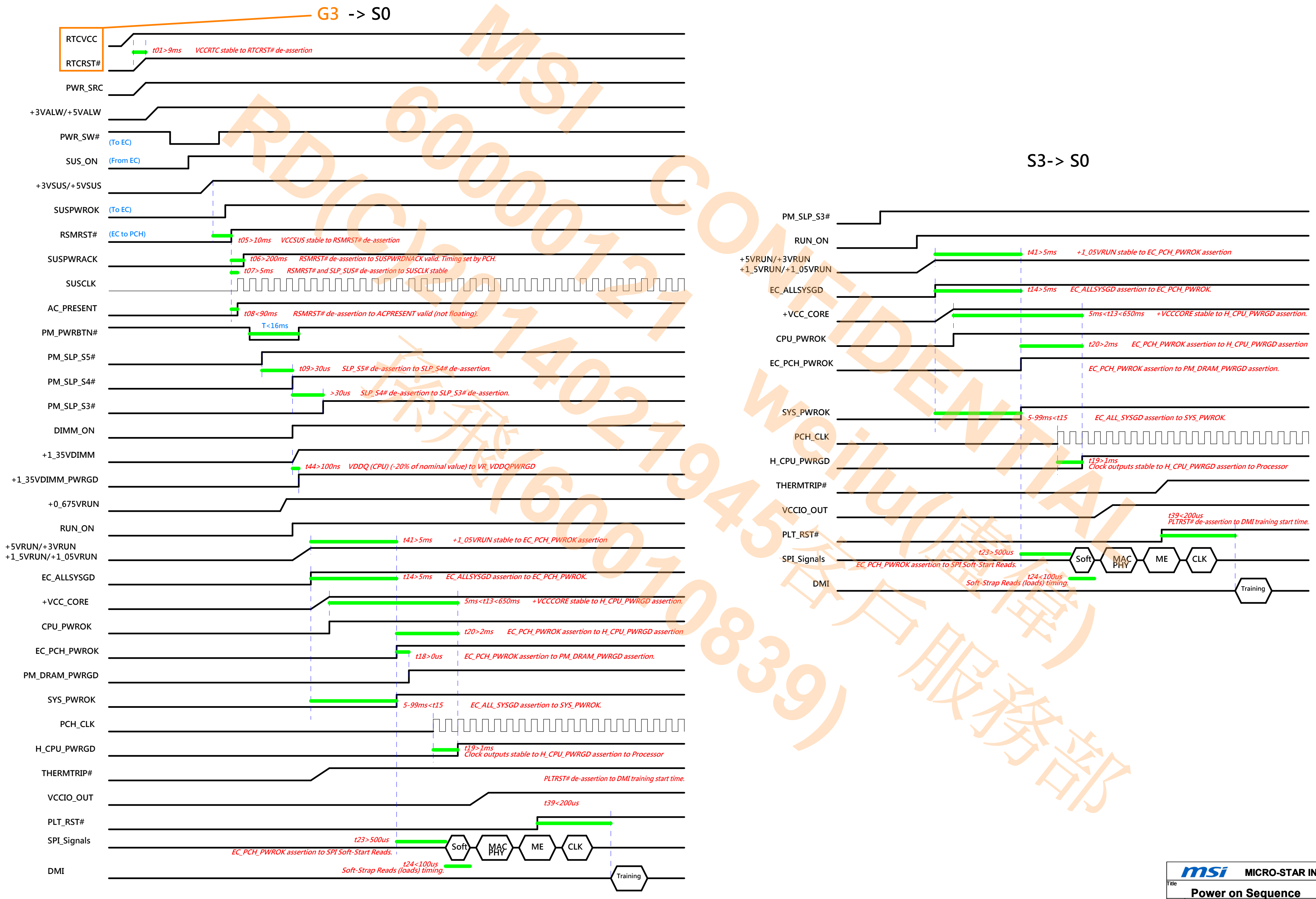
Power on Sequence



msi	MICRO-STAR INT'L CO.,LTD.	
Title	Power on Sequence	
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History

0B: Hardware part

01. Remove All GAP for power parts.
02. Add 3V3_NV part for leakage
03. Change cardreader PN.
04. Change BTB PN
05. Change SPDIF/ Audio Jack PN
06. R116 unstuff, R117 stuff.
07. R346 unstuff
08. Remove SUBWOOFER
09. Add one more AMP for SPK

0B: Power part

01. PR33 2.2Kohm R11-0222T12-W08
02. PC29 82pF/50V C11-8201012-W08
03. PC30 100pF/16V C11-1011032-W08
04. PR34 unstuff
05. PC32 unstuff
06. PR27 2.7Kohm R11-0272T12-W08
07. PR90 8.06Kohm R11-8061T12-W08
08. PR32 910Rohm R11-0911T12-W08
09. PC27 560pF/16V C11-5611812-W08
10. PR31 80.6Kohm R11-8062T12-W08
11. PR23 21Kohm R11-0213T12-W08
12. PR88 6.8Mohm R11-0685T13-W08
13. PR8 453Rohm R11-4530T22-W08
14. PC19 unstuff
15. PR6 unstuff
16. PR140 100Kohm R11-0104T12-W08
17. PR145 93.1Kohm R11-9312T12-R01
18. PR143 15Kohm R11-0153T12-W08
19. PR124 95.3Kohm R11-9532T12-W08
20. PR86 28.7Kohm R11-2872T12-W08
21. PC69, PC70 change to 1206 package
22. PR88 6.8Mohm R11-0685T13-W08