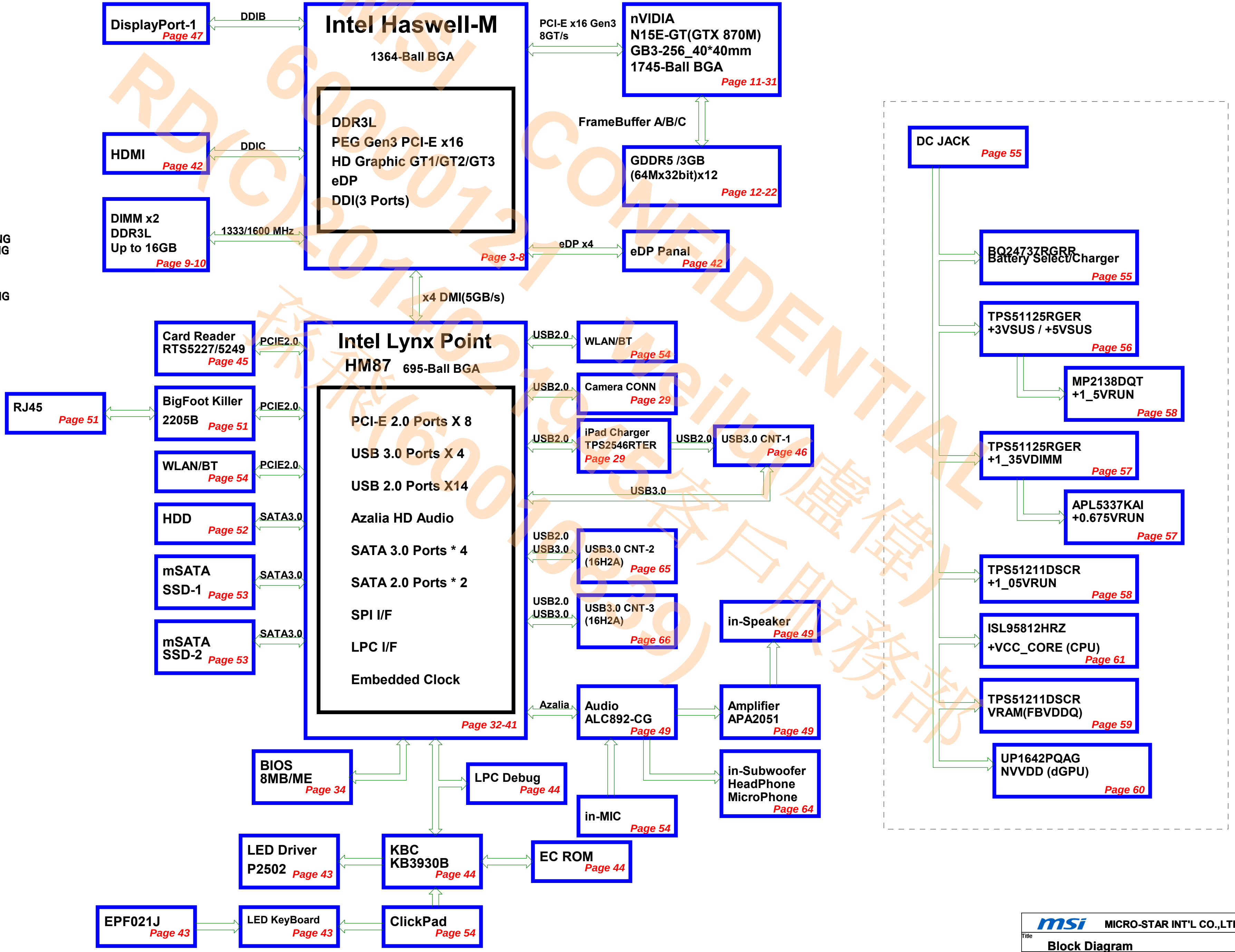
MS-16H2 Ver:0A

Shark Bay Mobile

Monday, September 09, 2013



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Title	Block Diagram	
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	PM_SLP_S5#
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	PM_SLP_S3#
+VCC_CORE	1.8V Core Voltage for Processor	EC_ALLSYSPG
+1_05VRUN	1.05V rail for Processor	PM_SLP_S3#
NVVDD	V Core Voltage for nVIDIA dGPU	NVVDD_EN
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	FBVDDQ_ON
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	NVVDD_EN

Net Naming Conventions

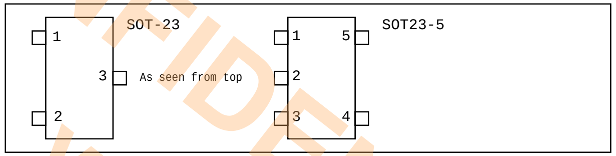
Suffix

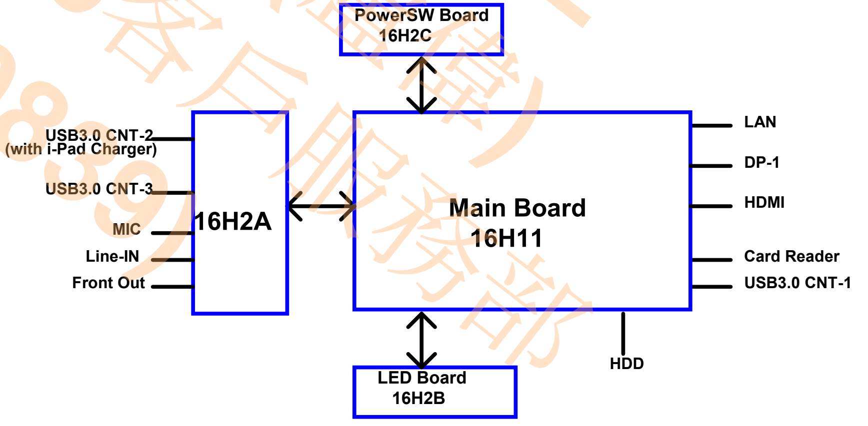
= Active Low Signal

Prefix

H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)
FB = DGPU VRAM
VIAxxx = Like Test Point, but using VIA.

PCB Footprints





POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on and +V*SUS always keep high

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Title: Platform

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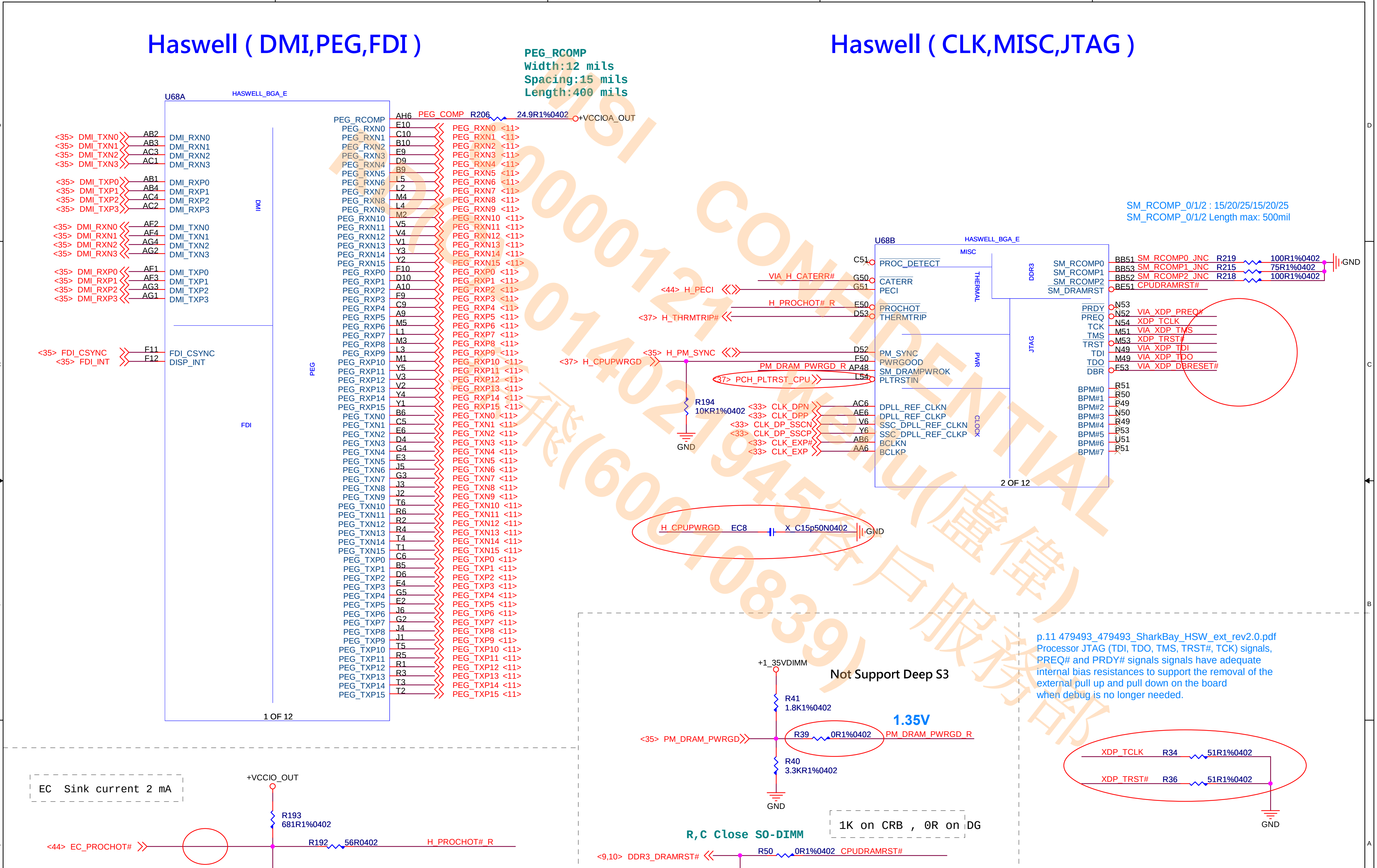

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Title: CPU-1 (Host Bus)

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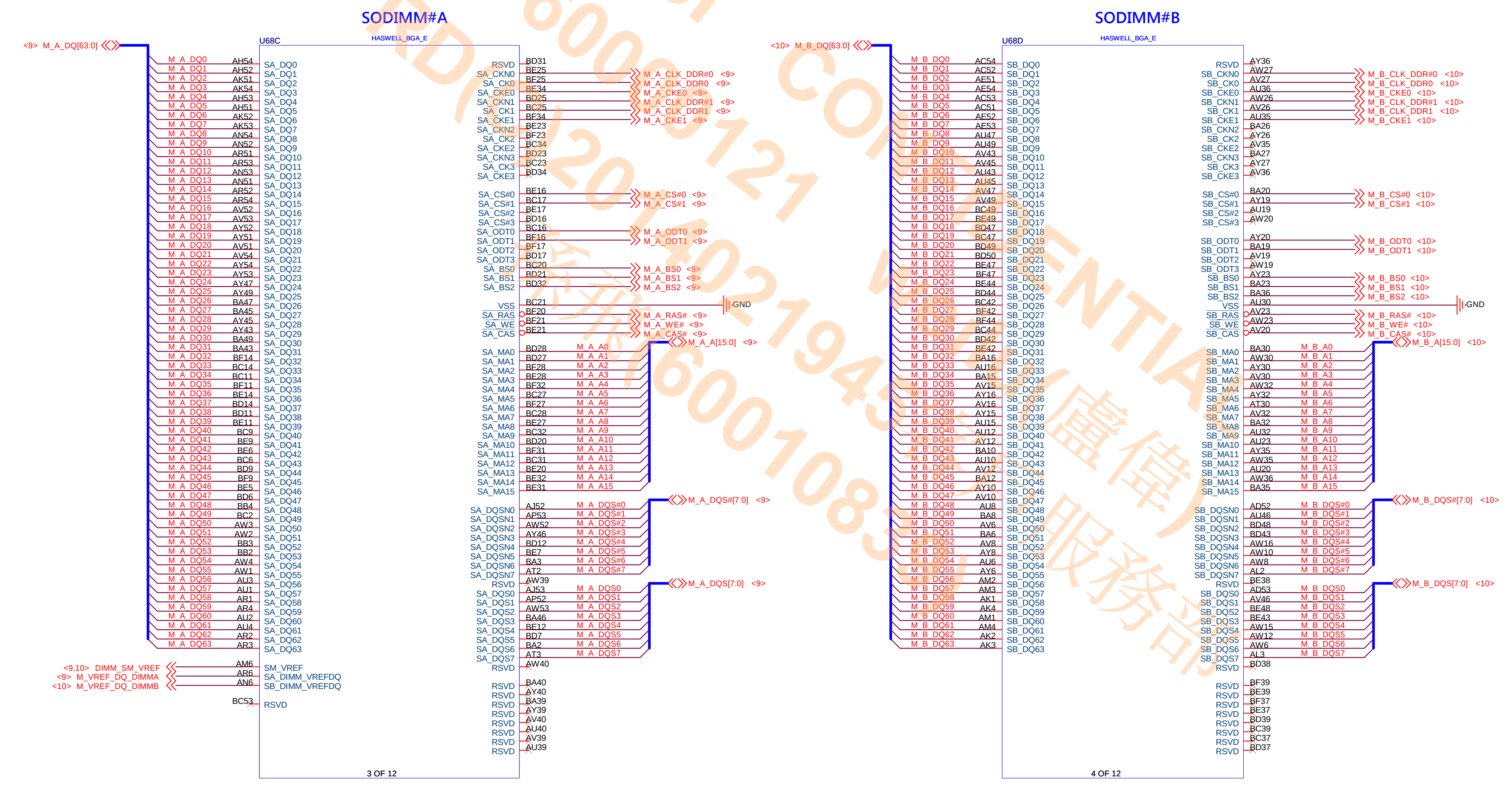
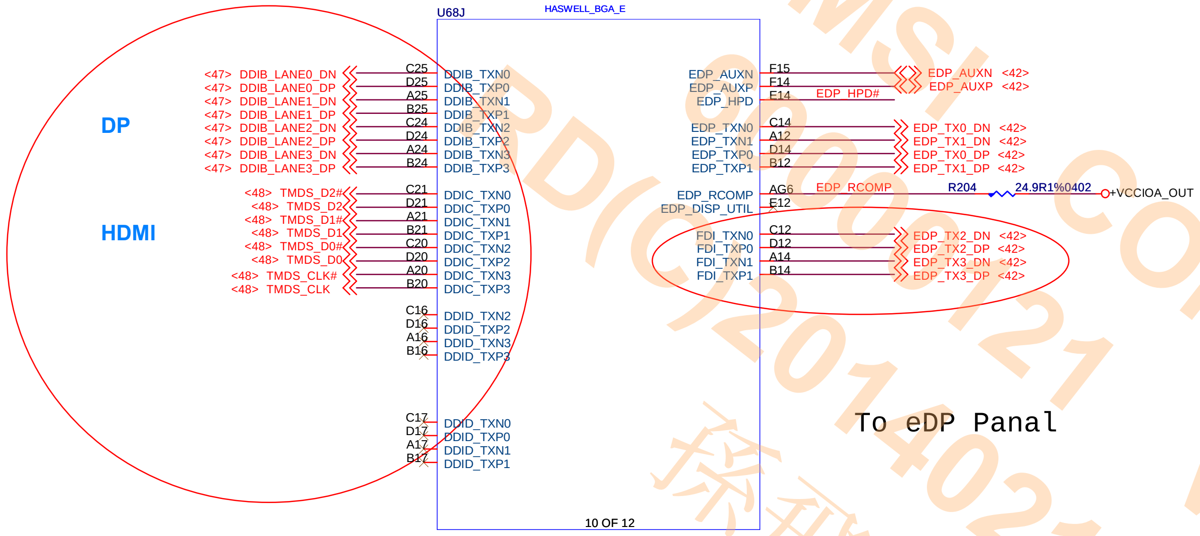
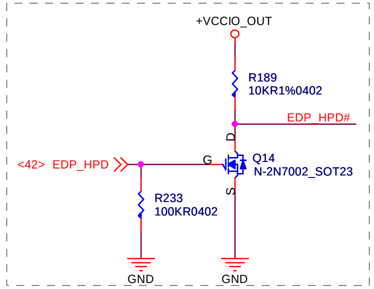
Haswell (DDR3L)

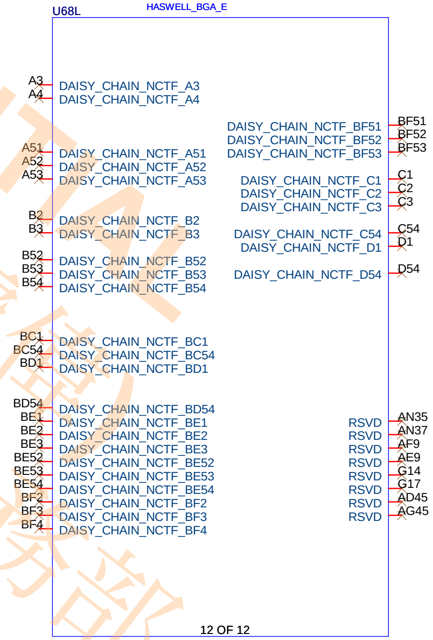


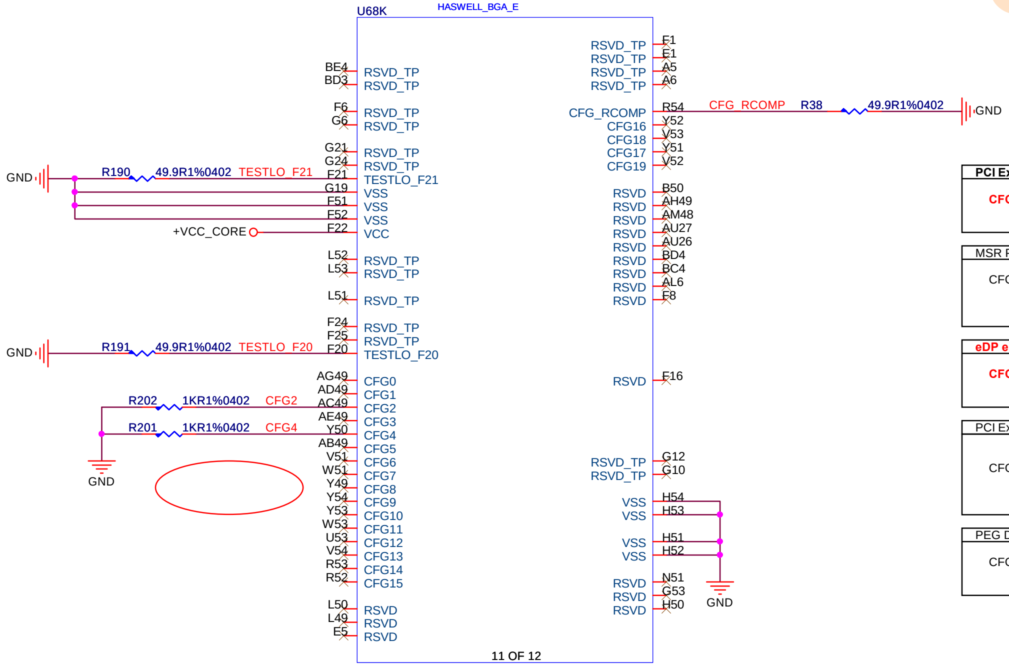
Display/Reserved





To eDP Panal





PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

MICRO-STAR INT'L CO.,LTD.		
Title	CPU-3 (Display/Reserved)	
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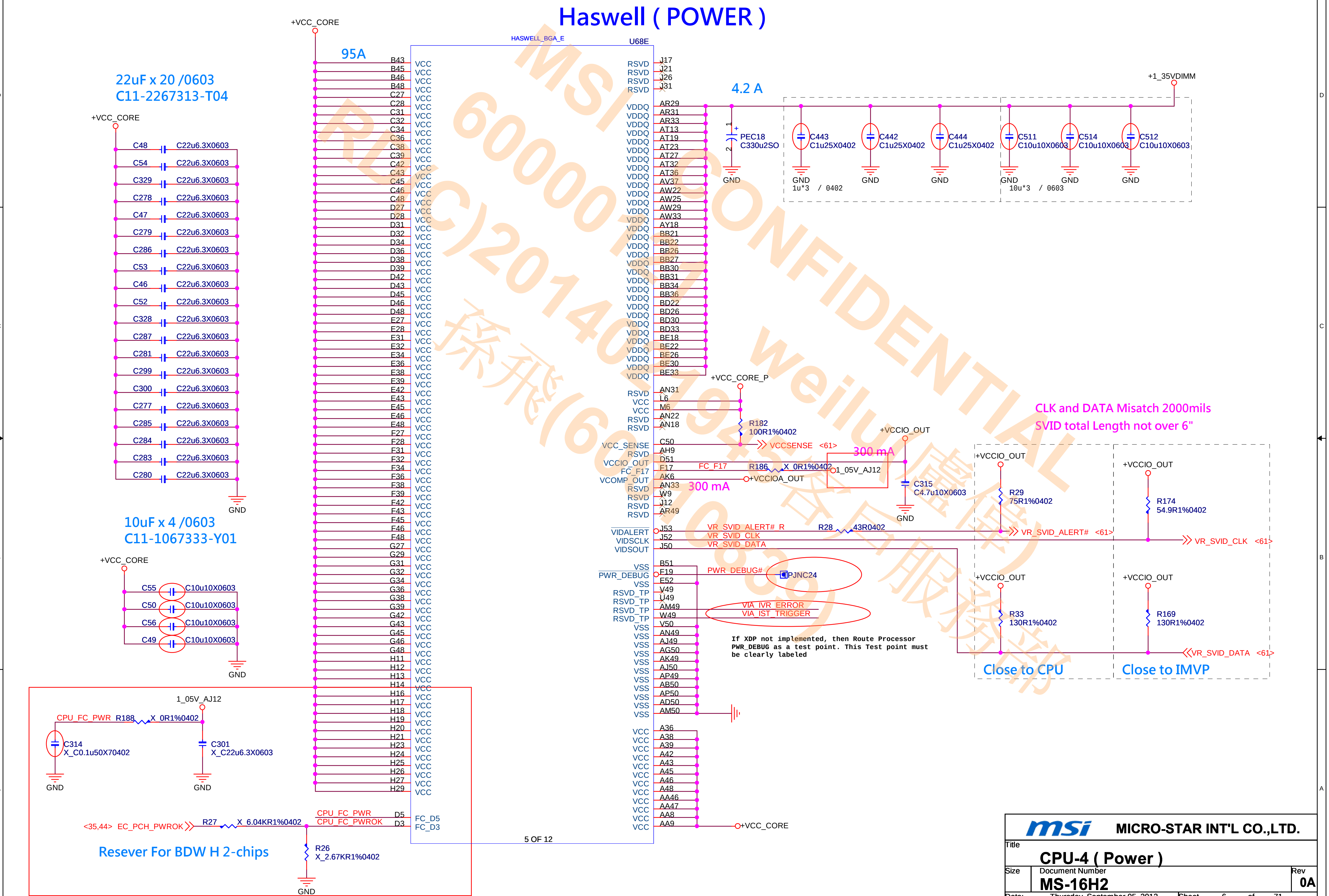
Haswell (POWER)



MICRO-STAR INT'L CO.,LTD.

Title: CPU-4 (Power)

Size	Document Number	Rev
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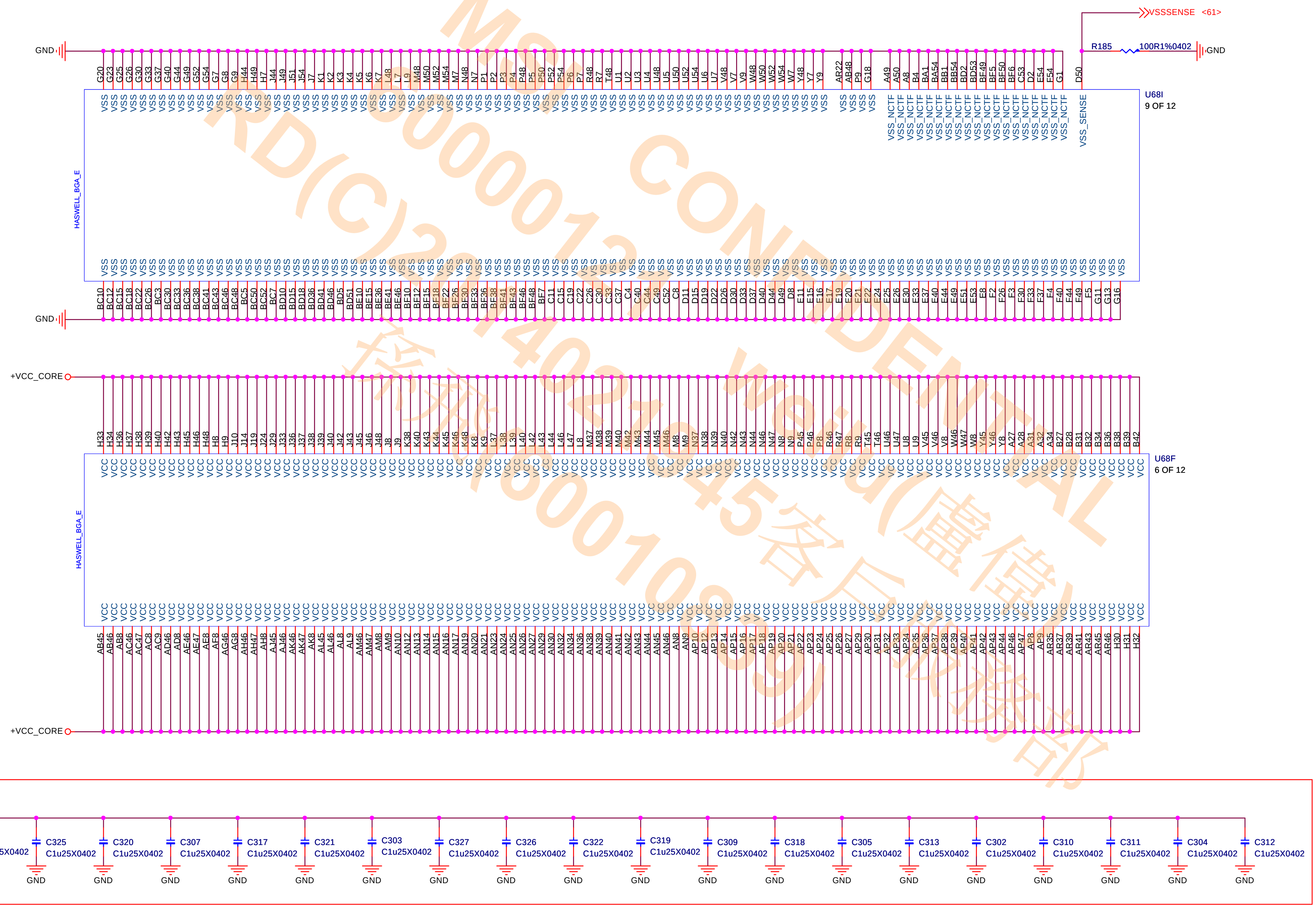
Haswell (Power & GND)



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Title	CPU-6 (Power & GND)
Size / Document Number	MS-16H2
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Date:	Thursday, September 05, 2013
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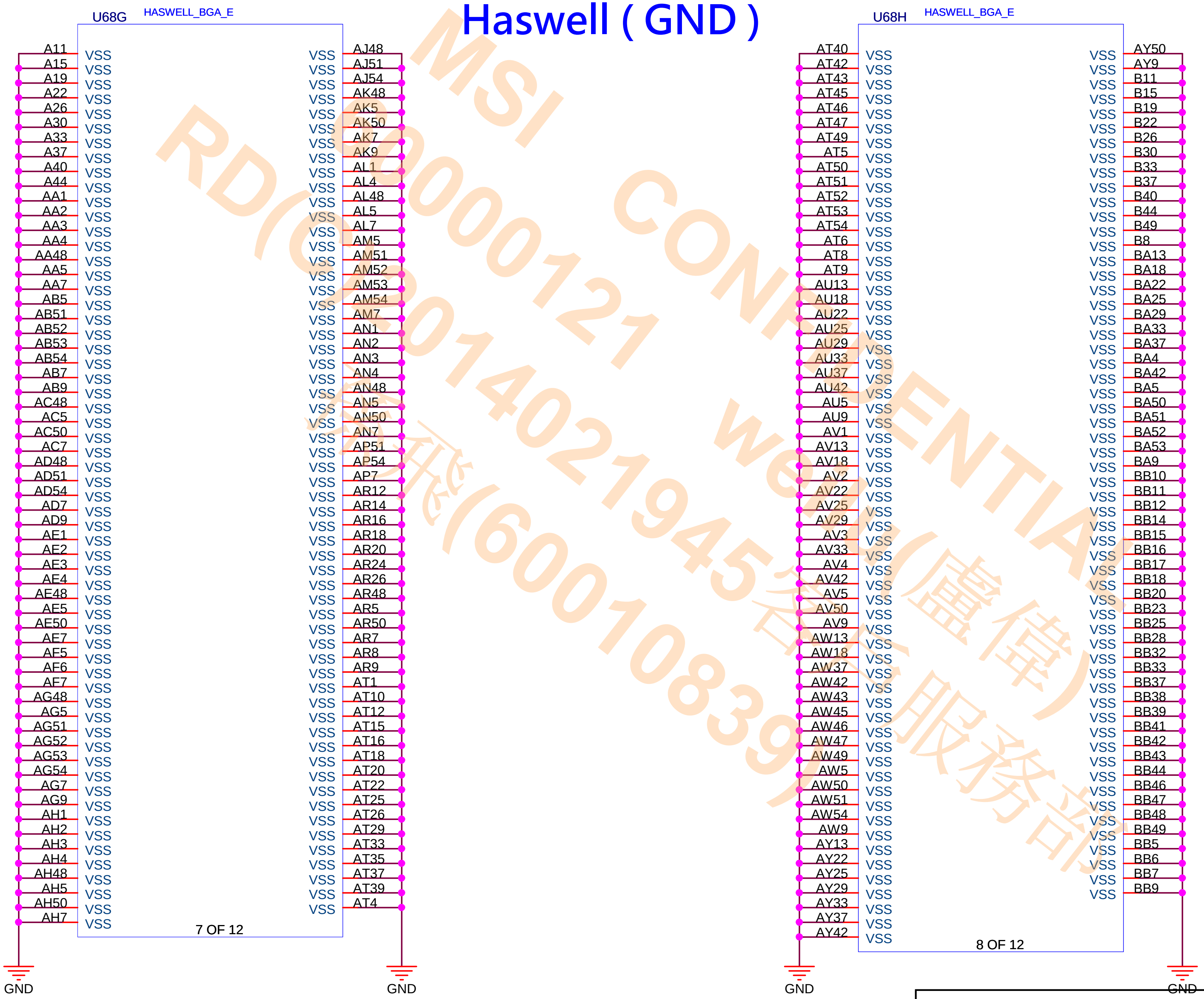
Haswell (GND)



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Title: CPU-5 (GND)

Size | Document Number: MS-16H2 | Rev: 0A

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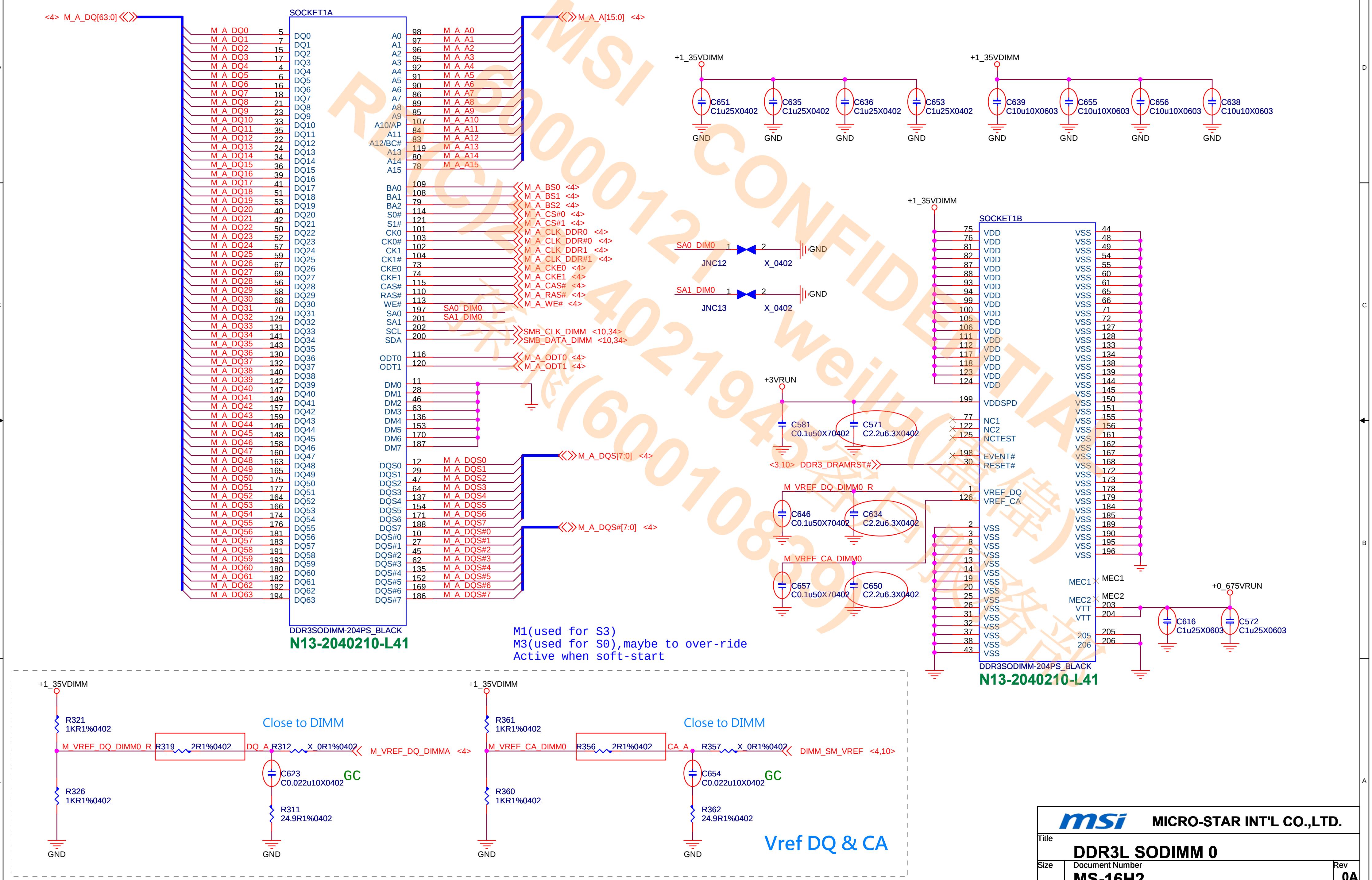
SODIMM#A



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Title	DDR3L SODIMM 0
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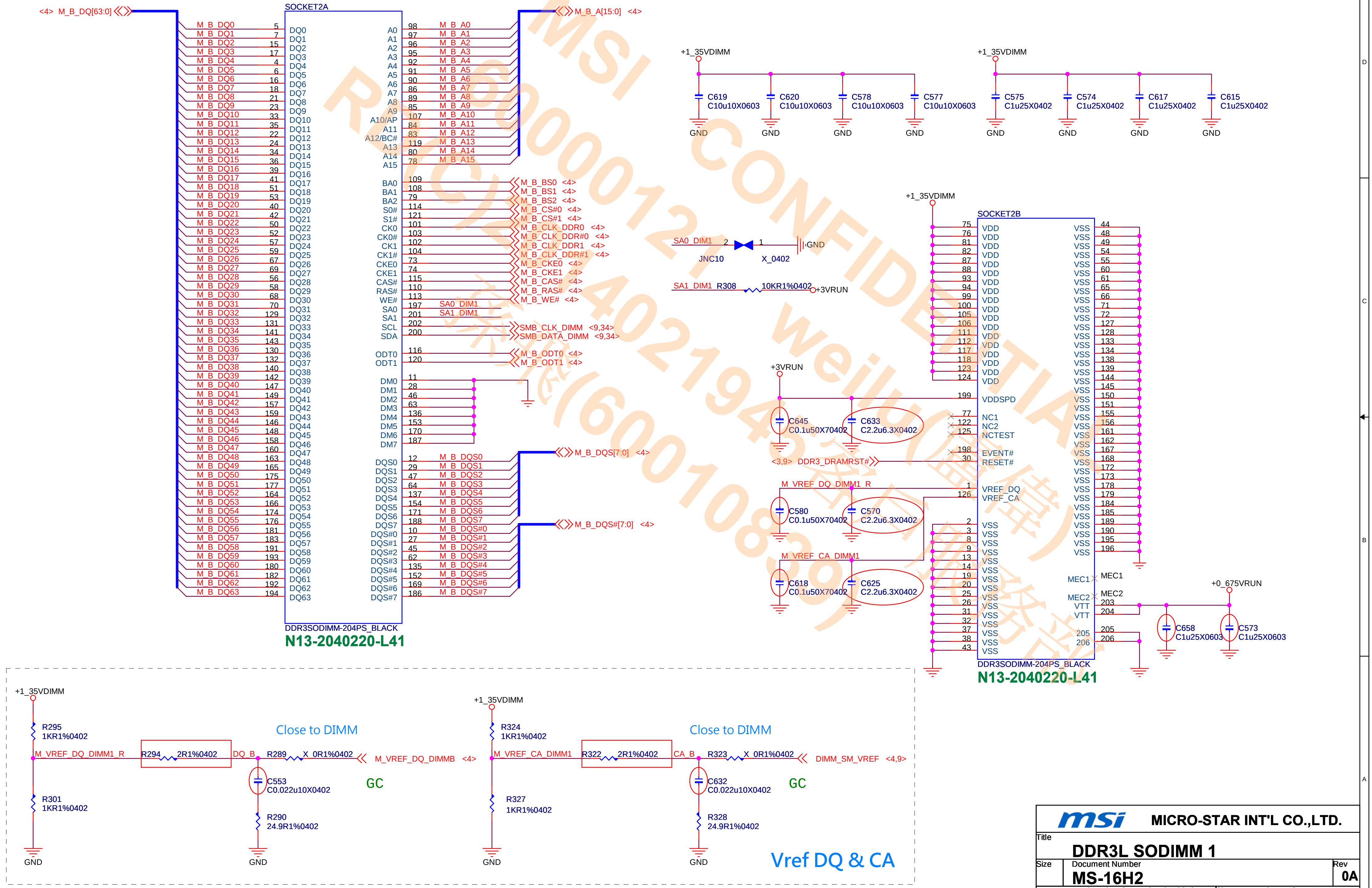
SODIMM#B



MICRO-STAR INT'L CO.,LTD.

Title: DDR3L SODIMM 1

Size | Document Number: MS-16H2 | Rev: 0A

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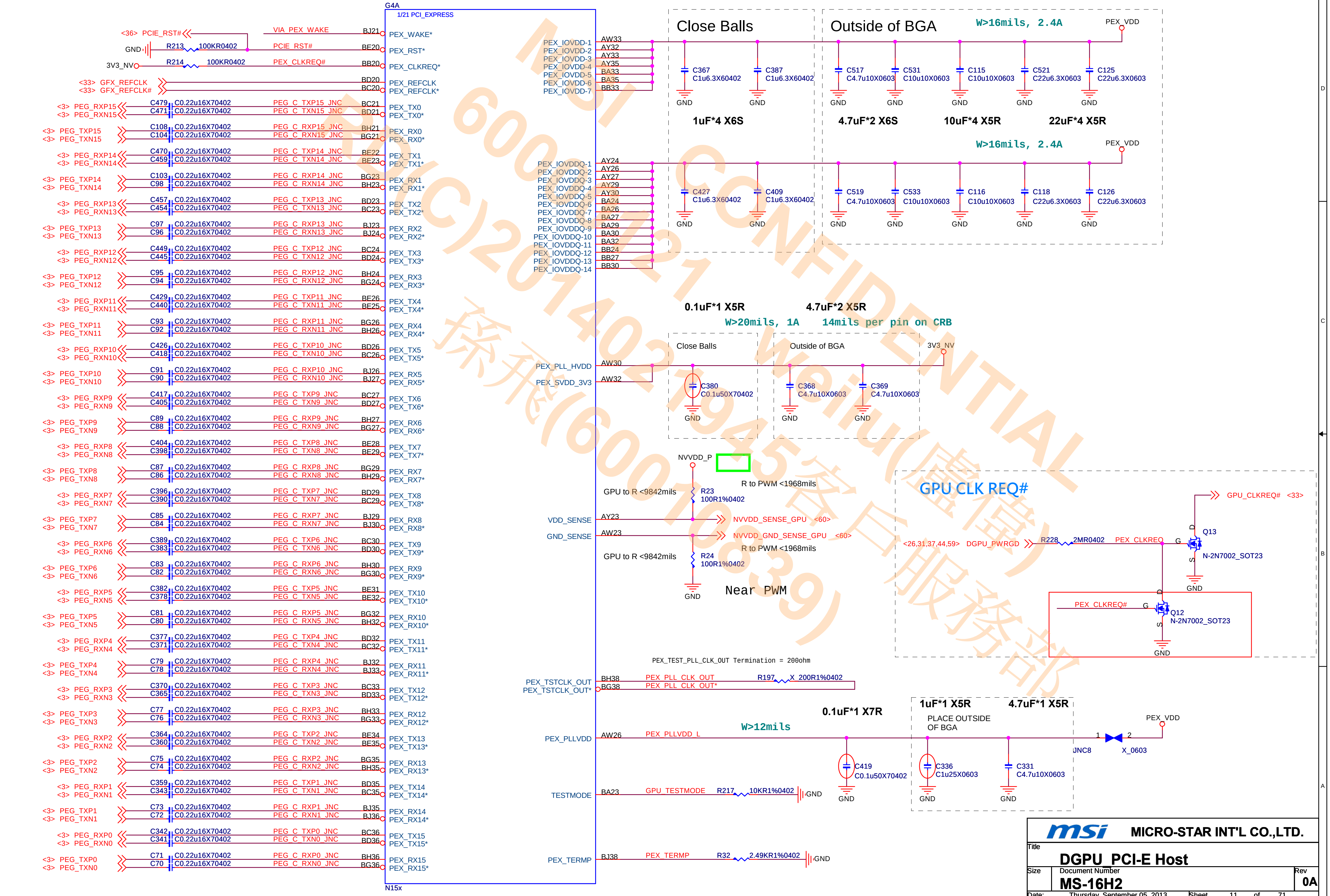
GPU PCI EXPRESS



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Title	DGPU_PCI-E Host	
Size	Document Number: MS-16H2	Rev: 0A
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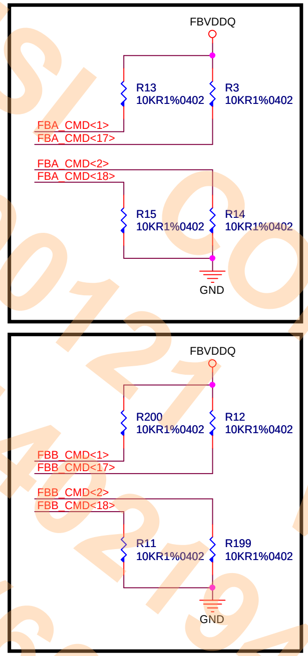
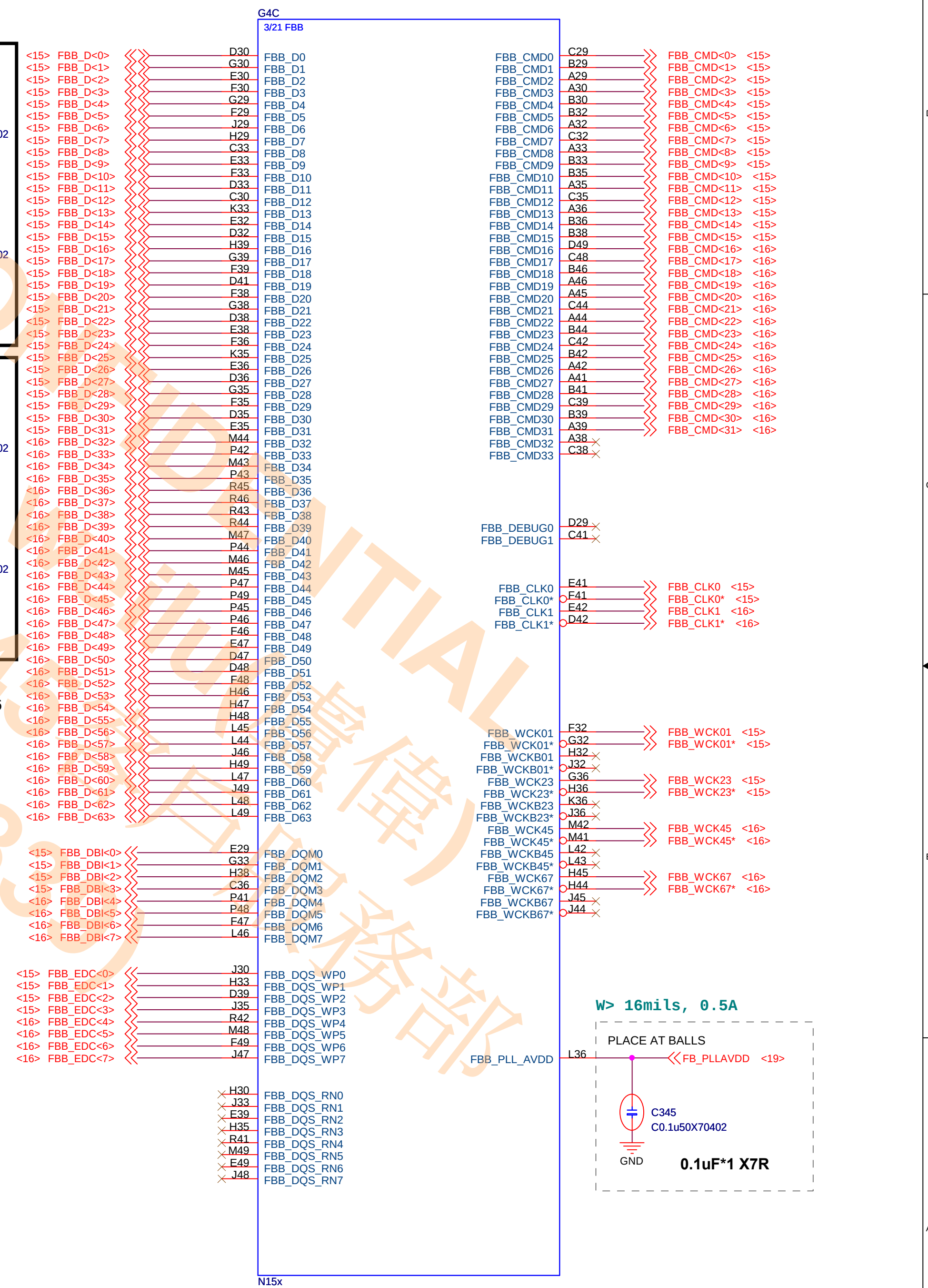
GPU Frame Buffer Partition A/B





GDDR5 Mode F Mapping By GB3-256

	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

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Title: DGPU_MEM IF A/B

Size | Document Number: MS-16H2 | Rev: 0A

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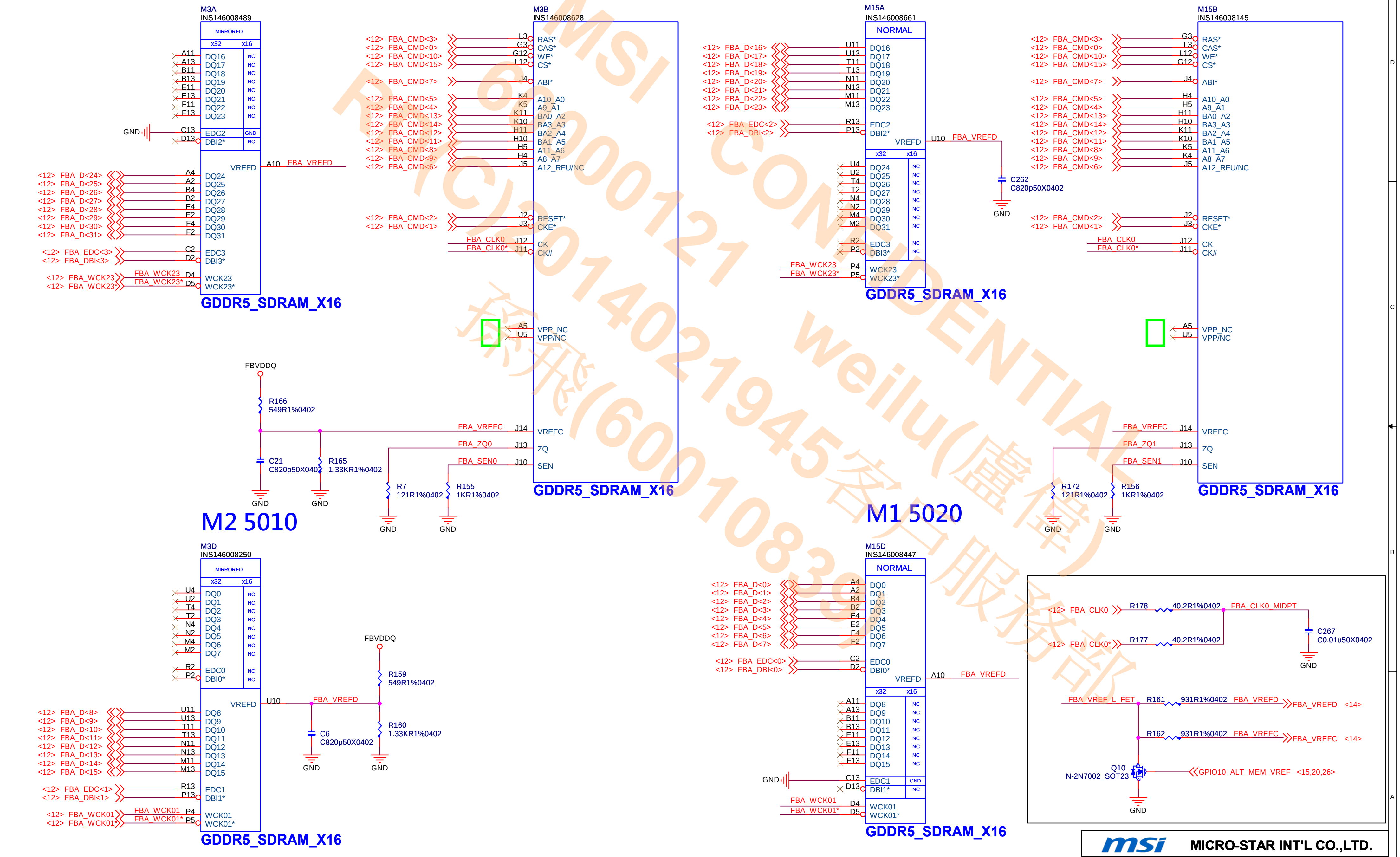
DGPU_GDDR5 FrameBuffer A0



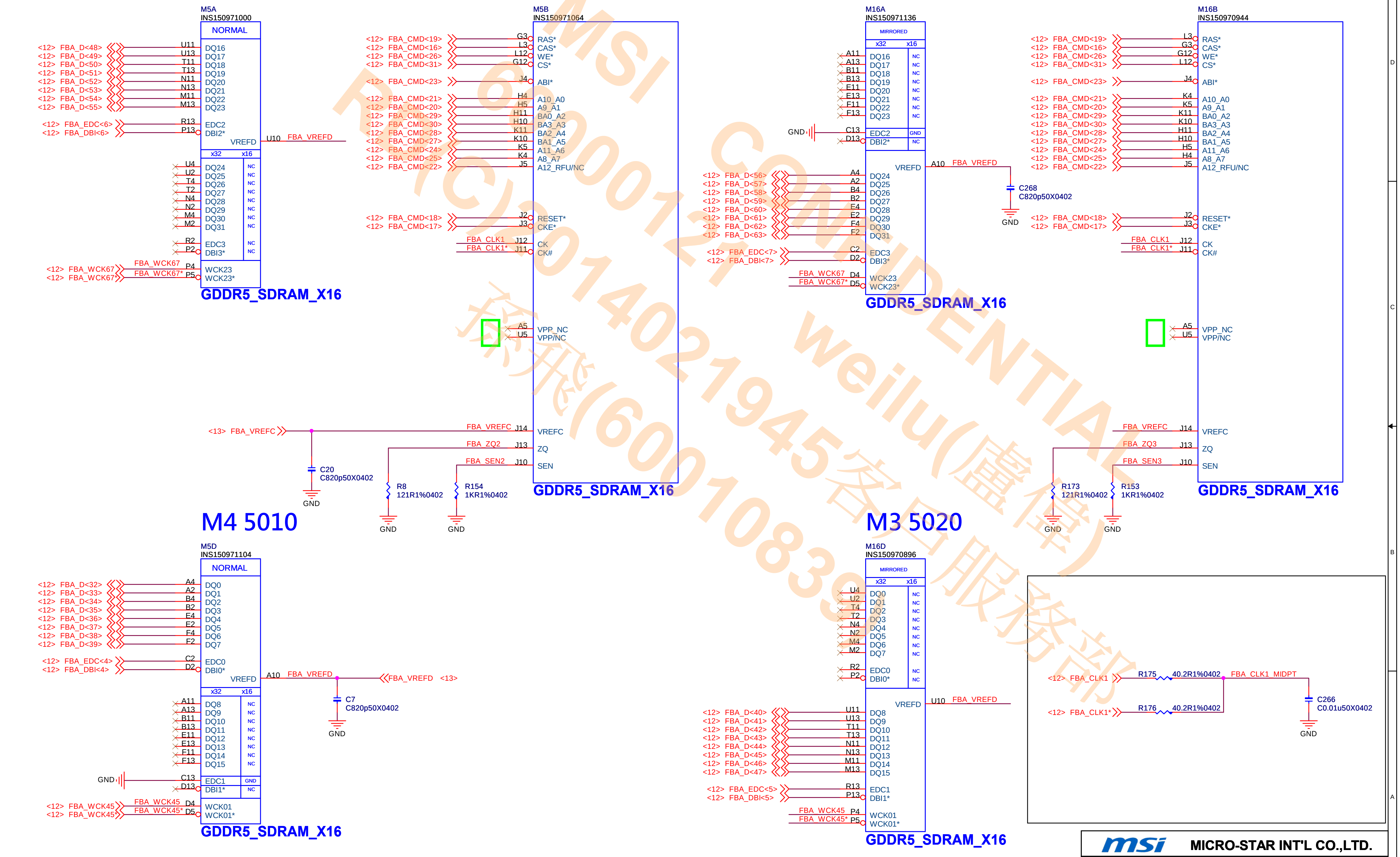
MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FrameBuffer A0

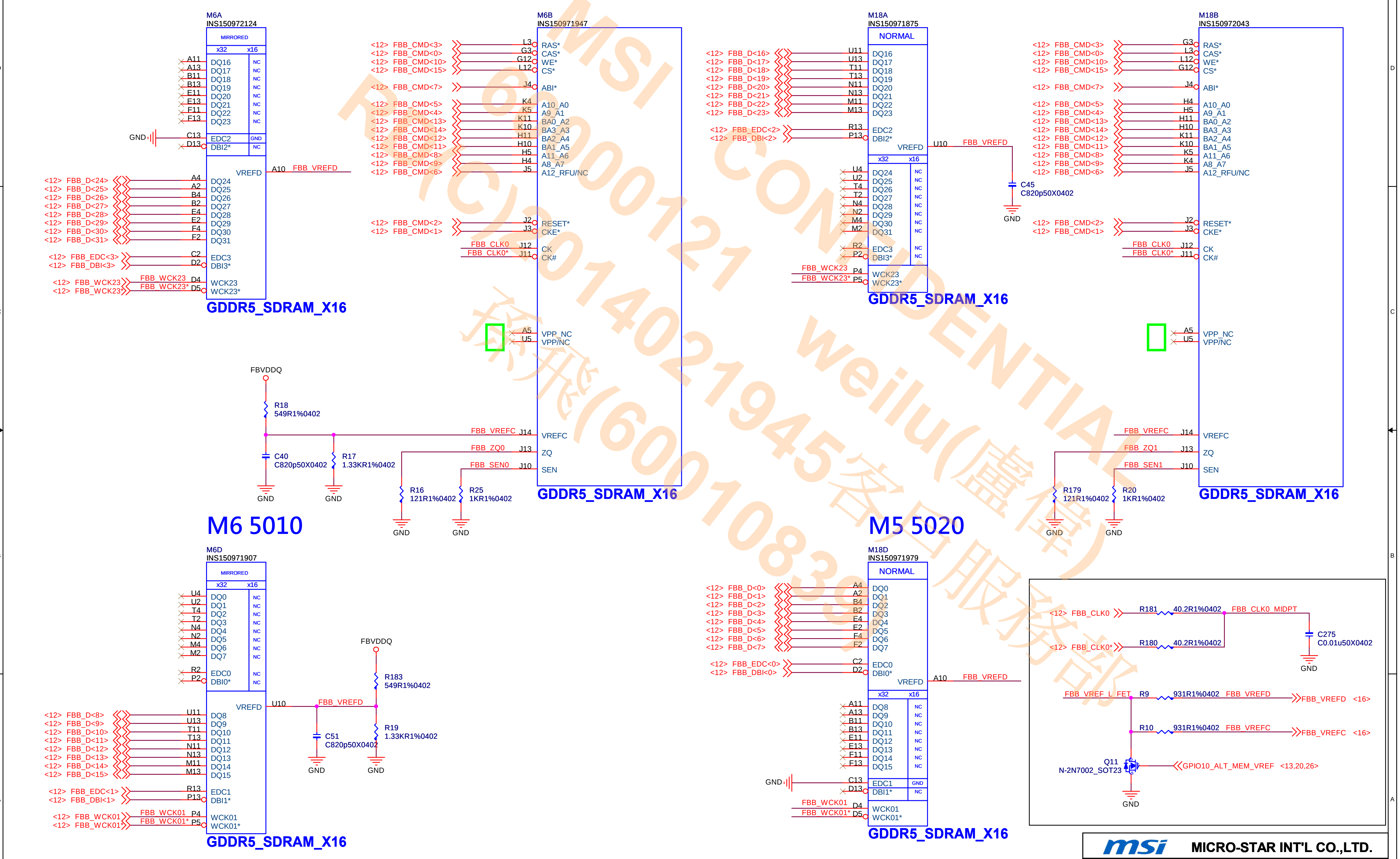
Size | Document Number: MS-16H2 | Rev: 0A

Date: Friday, September 06, 2013 | Sheet 13 of 71

DGPU_GDDR5 FrameBuffer A1



DGPU_GDDR5 FrameBuffer B0



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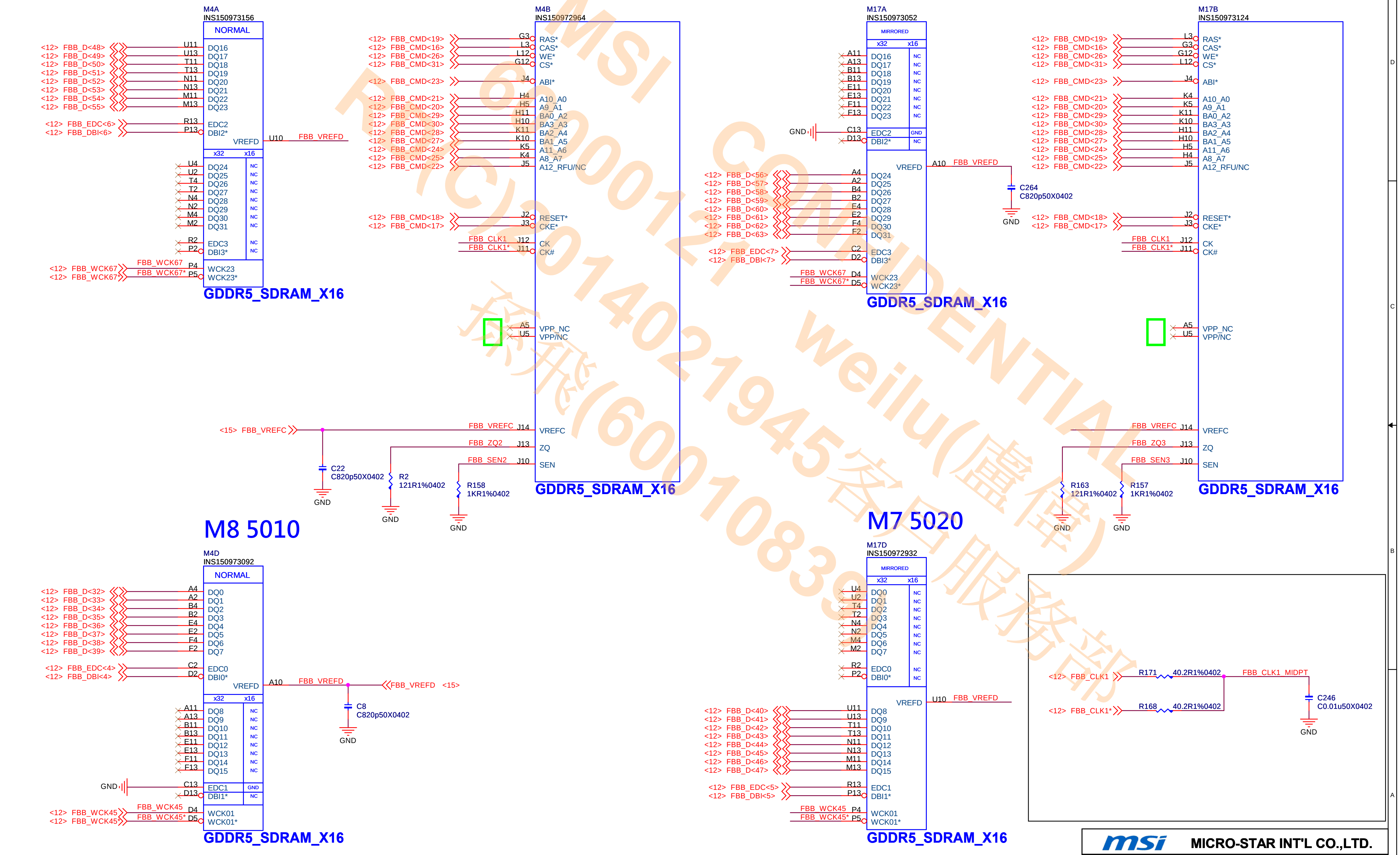
Title	DGPU_GDDR5 FrameBuffer B0	
Size	Document Number: MS-16H2	Rev: 0A
Date: Friday, September 06, 2013	Sheet 15 of 71	

DGPU_GDDR5 FrameBuffer B1



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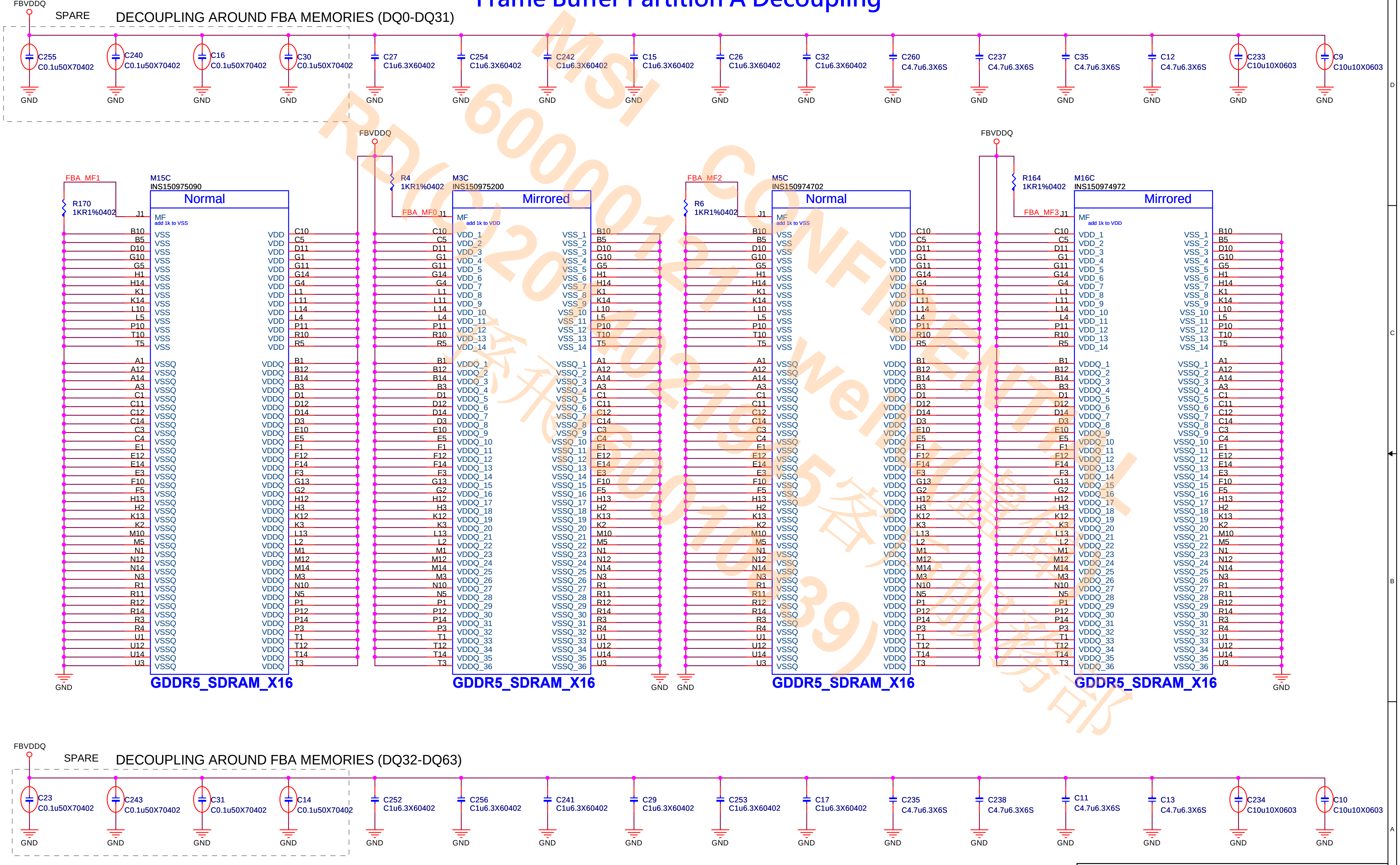
Title	DGPU_GDDR5 FrameBuffer B1	
Size	Document Number: MS-16H2	Rev: 0A
Date: Friday, September 06, 2013	Sheet 16 of 71	

Frame Buffer Partition A Decoupling



MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FB-A_DECOUPLING

Size	Document Number	Rev
	MS-16H2	0A

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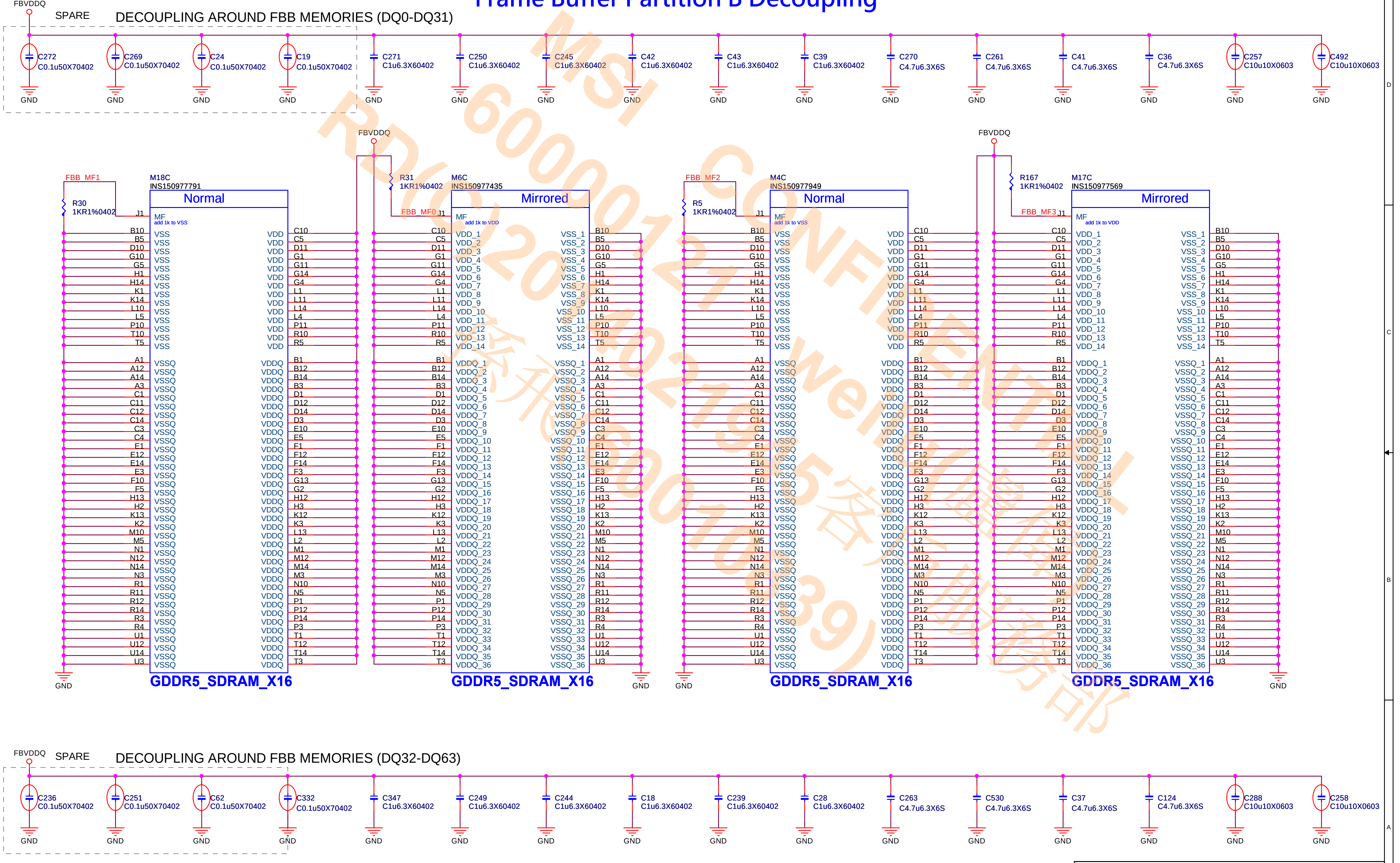
Frame Buffer Partition B Decoupling



msi	MICRO-STAR INT'L CO.,LTD.
Title	DGPU_GDDR5 FB-B_DECOUPLING
Size / Document Number	MS-16H2
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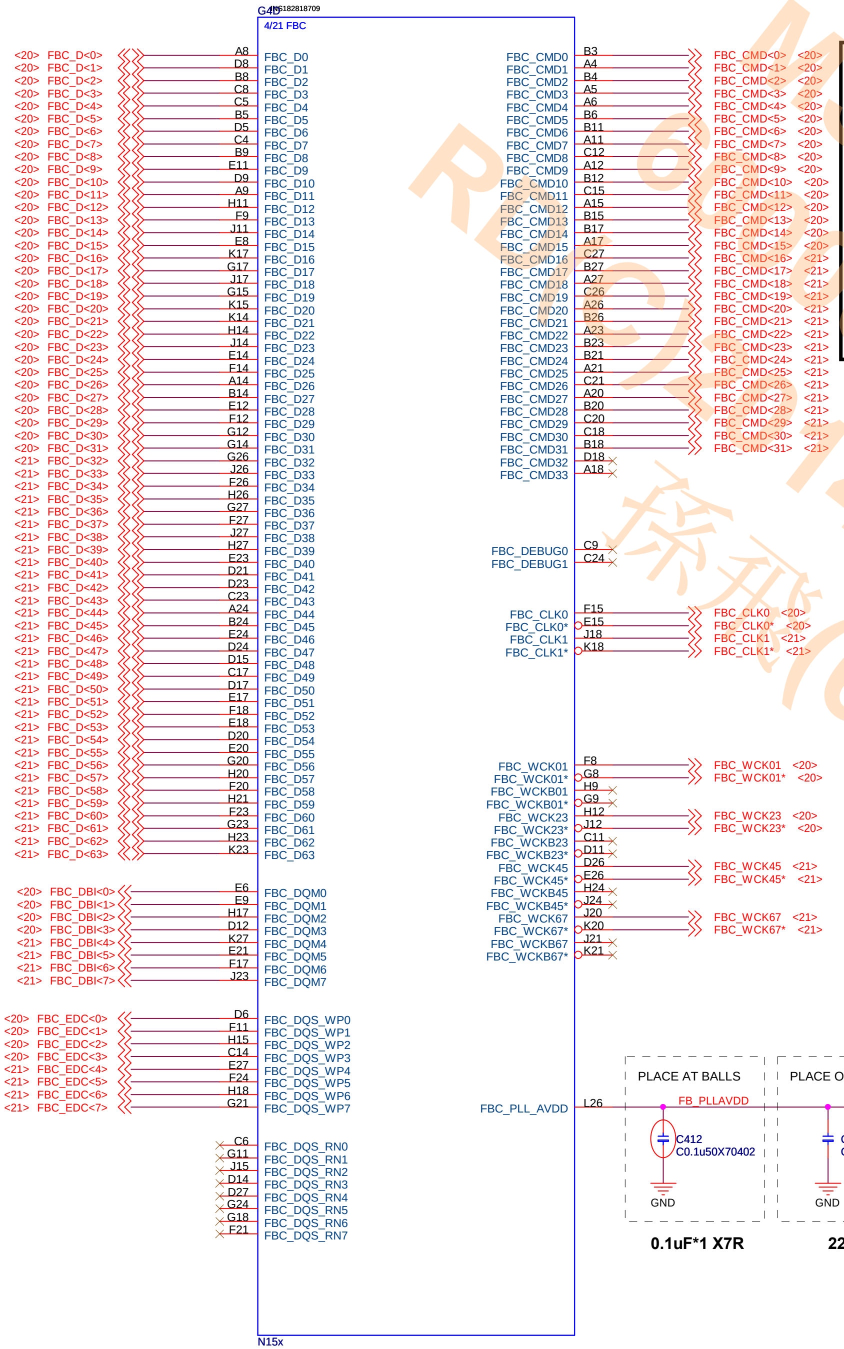
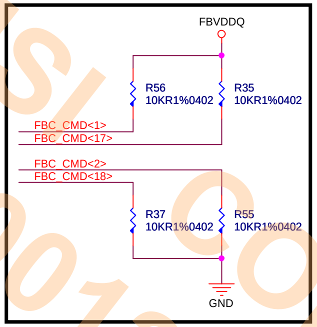
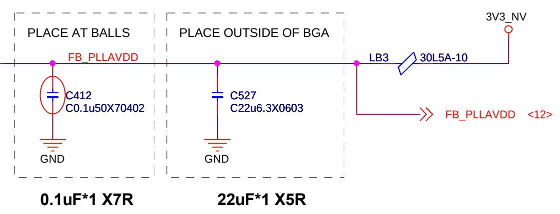
GPU Frame Buffer Partition C/D

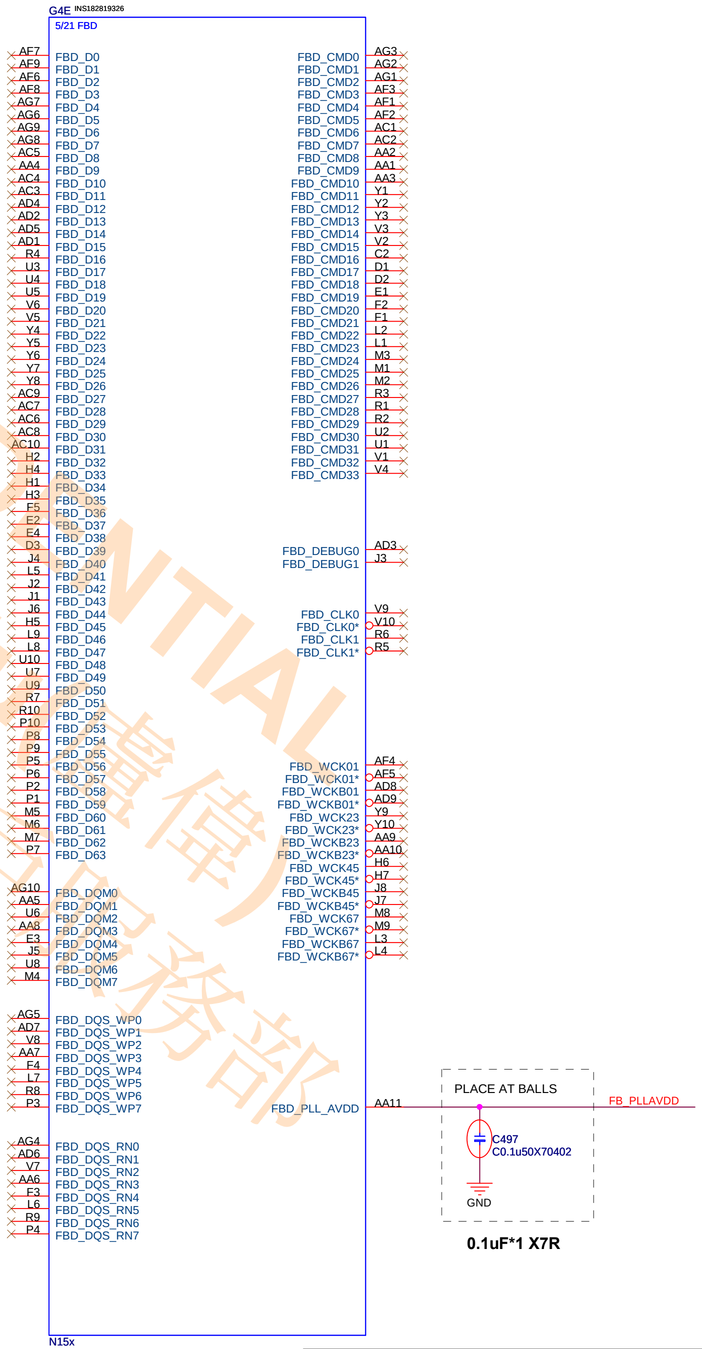




GDDR5 Mode F Mapping By GB3-256

	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*





MICRO-STAR INT'L CO.,LTD.

Title: **DGPU_MEM IF C/D**

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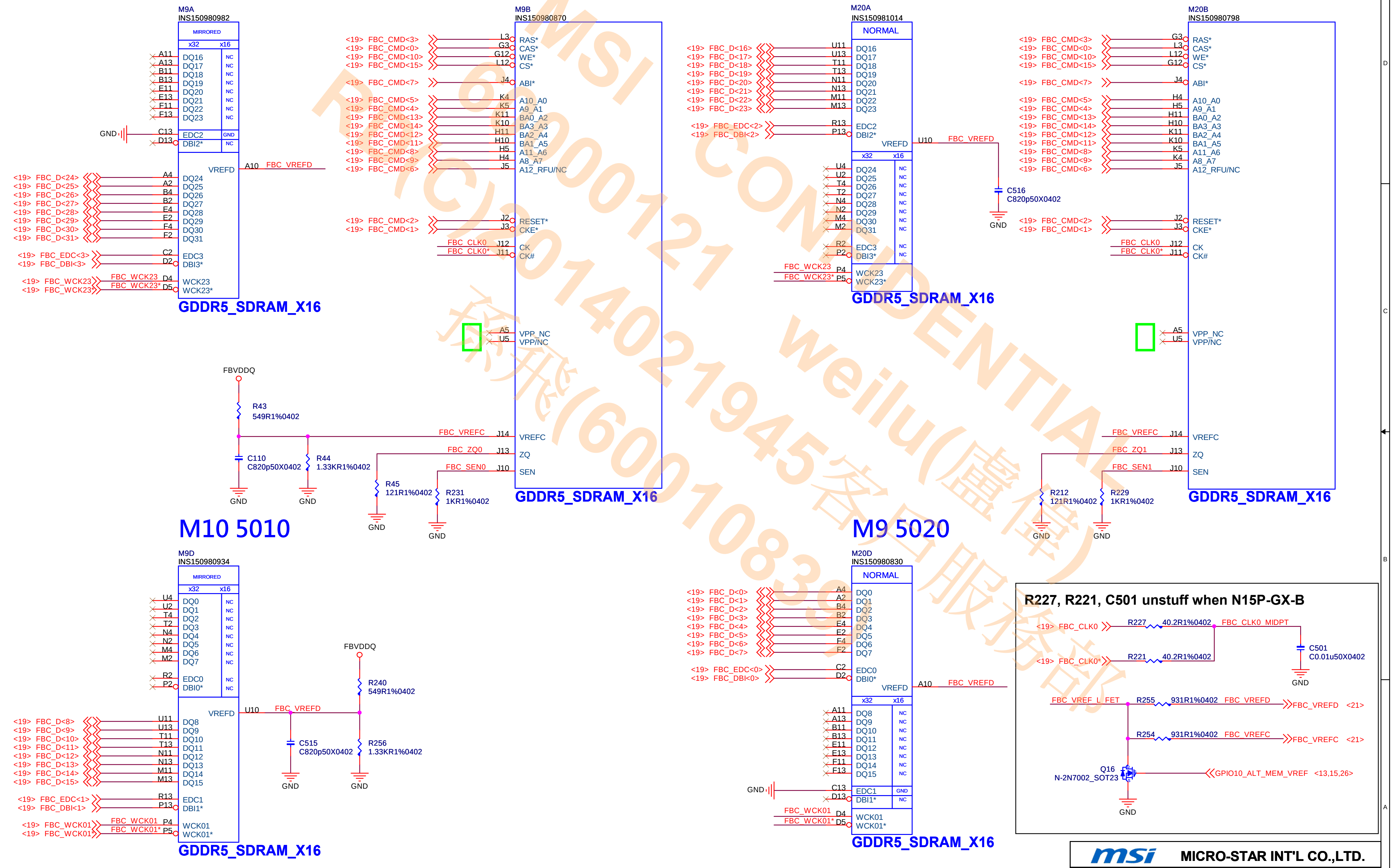
DGPU_GDDR5 FrameBuffer C0



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Title	DGPU_GDDR5 FrameBuffer C	
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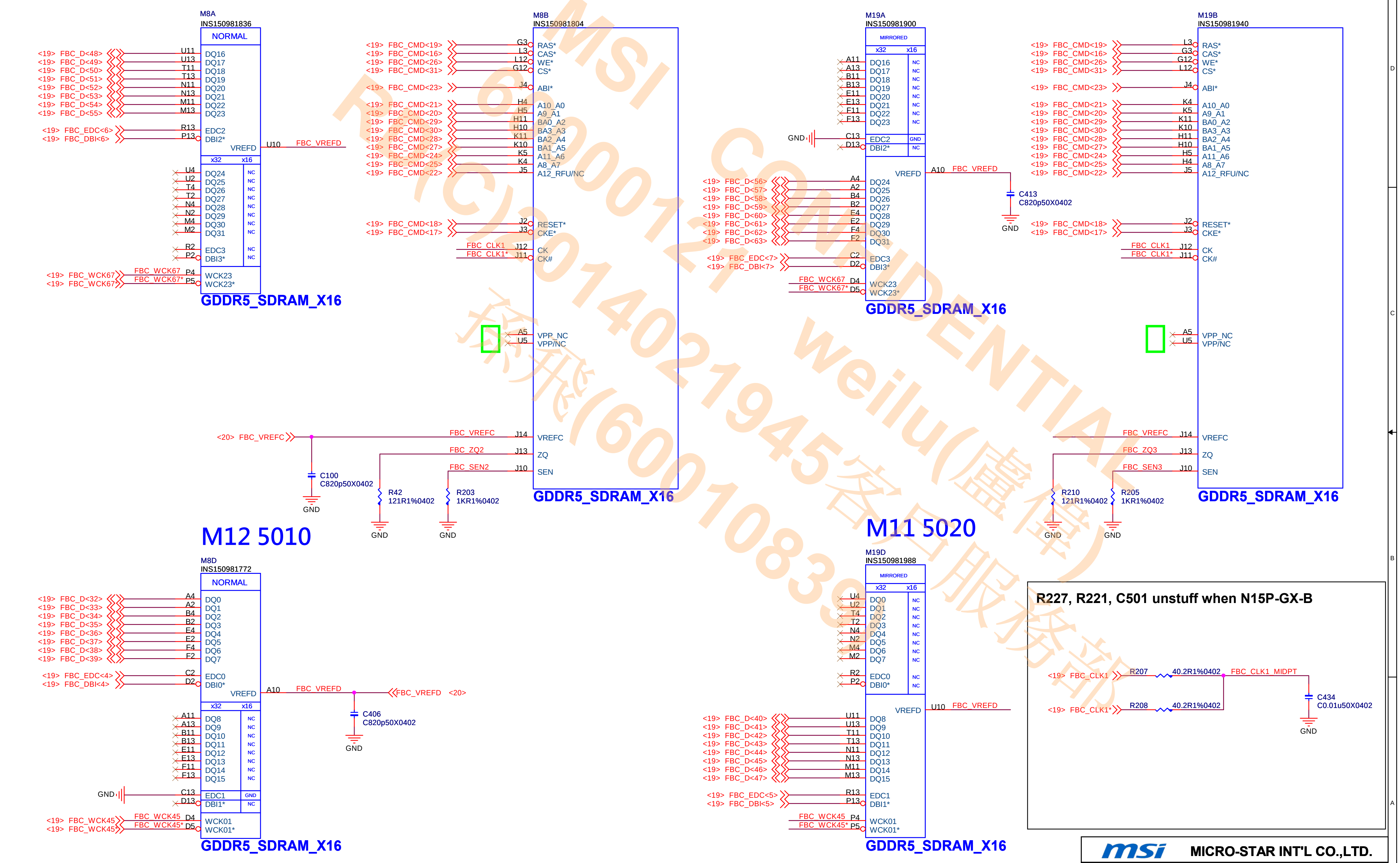
DGPU_GDDR5 FrameBuffer C1



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Title: DGPU_GDDR5 FrameBuffer C

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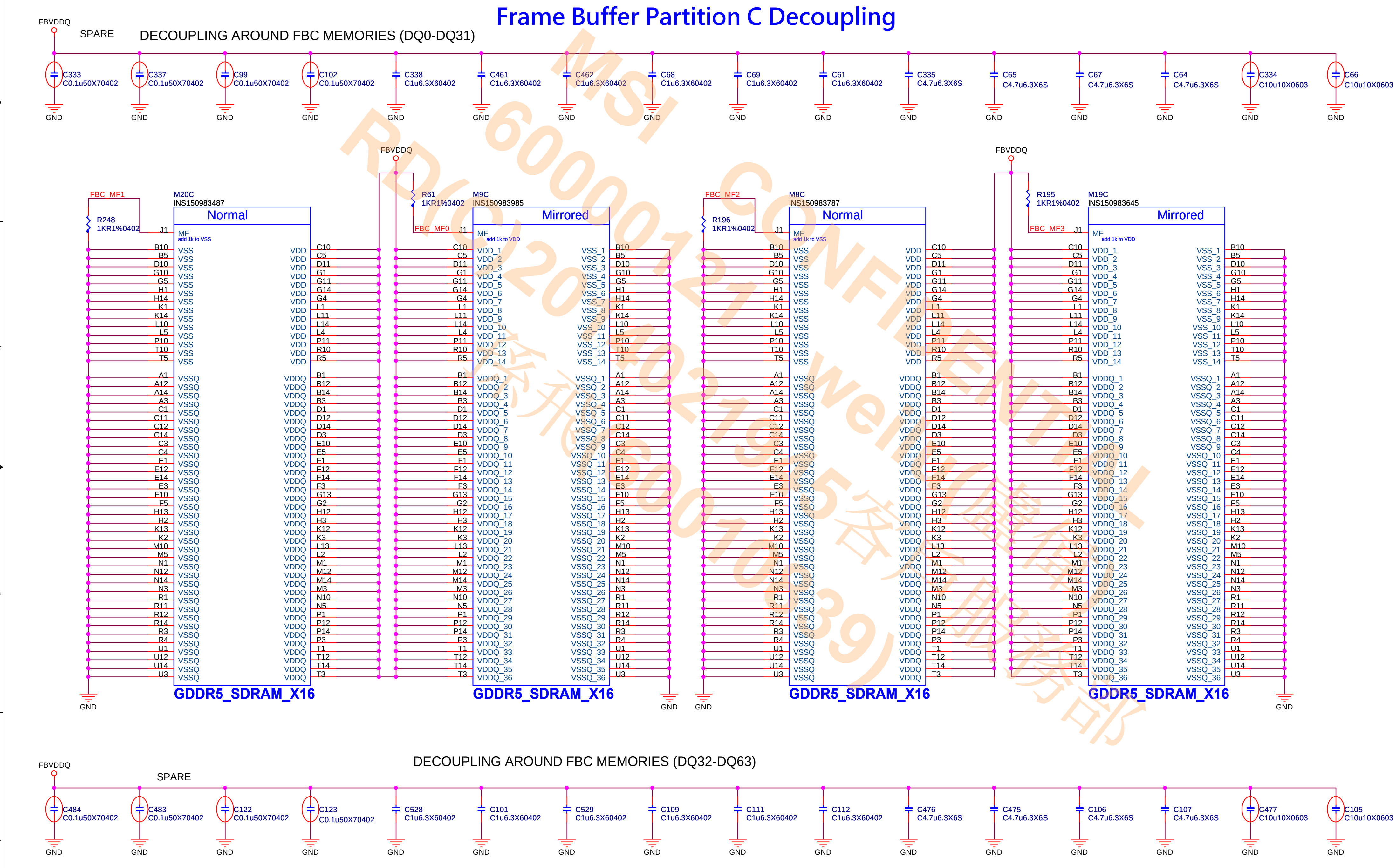
Date: Friday, September 06, 2013 | Sheet 21 of 71

Frame Buffer Partition C Decoupling



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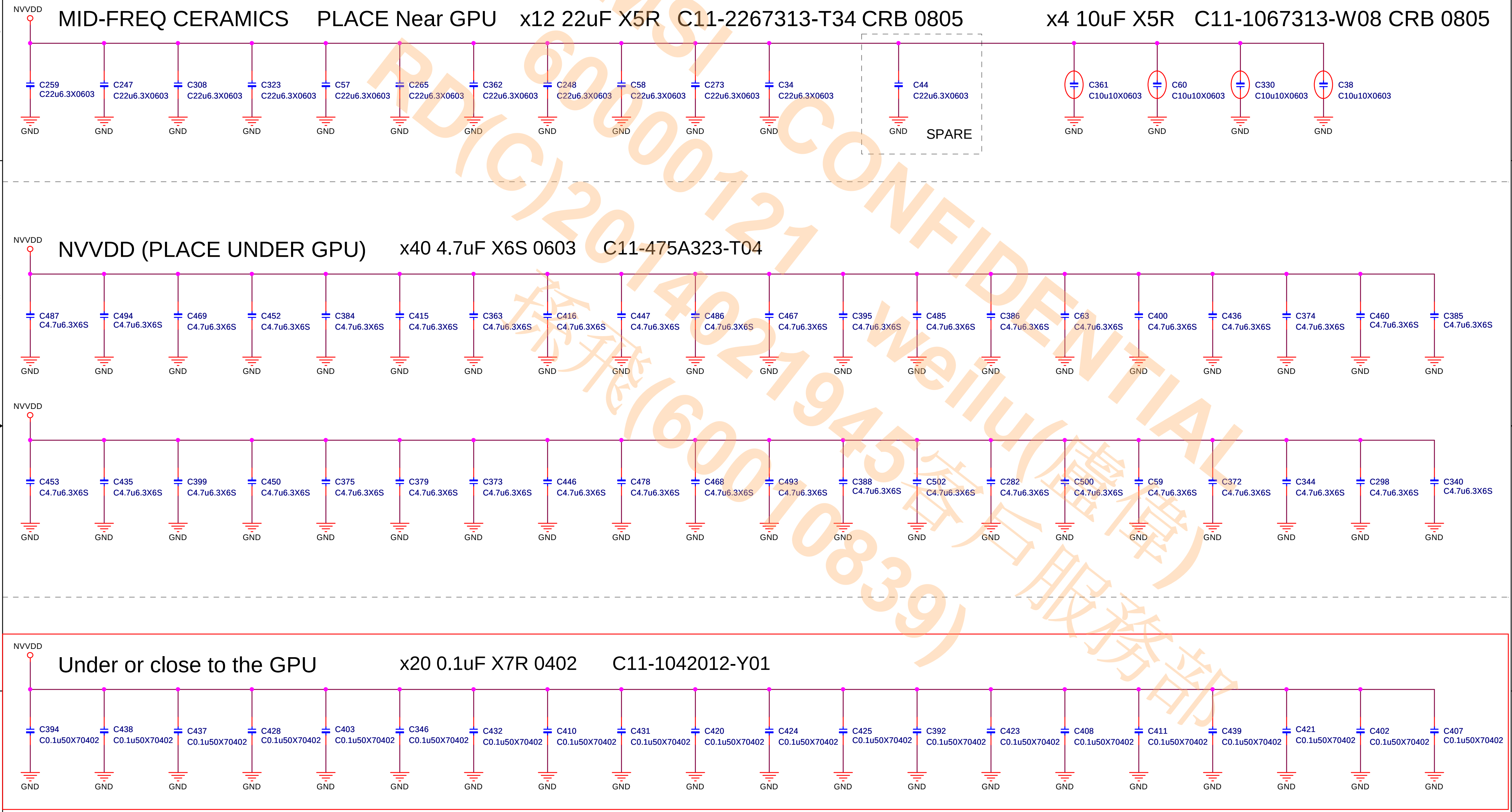
Title: DGPU_GDDR5 FB-C_DECOUPLING

Size | Document Number: MS-16H2 | Rev: 0A

Date: Friday, September 06, 2013 | Sheet 22 of 71

GPU DECOUPLING A



MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GPU DECOUPLING A

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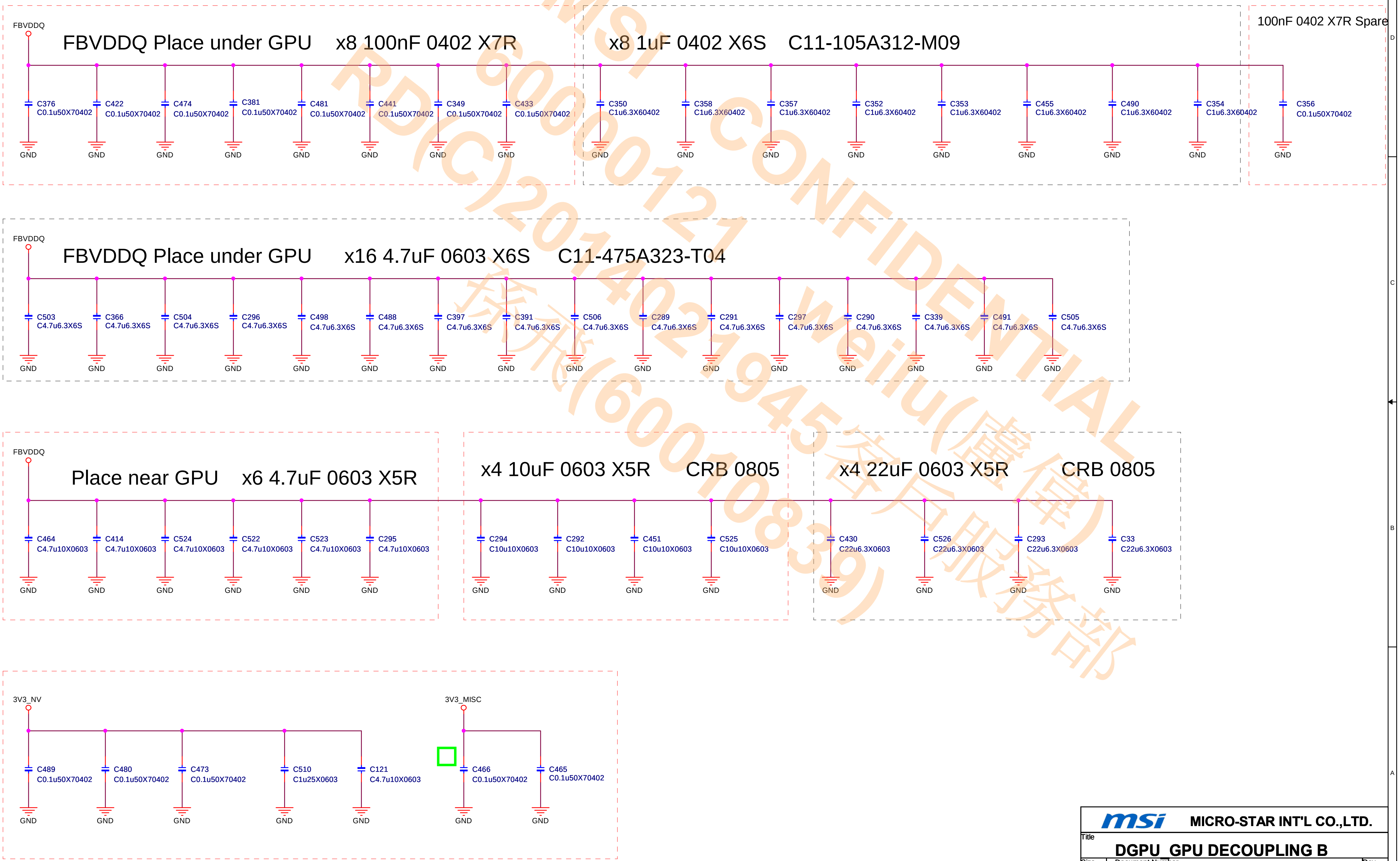
GPU DECOUPLING B



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GPU DECOUPLING B
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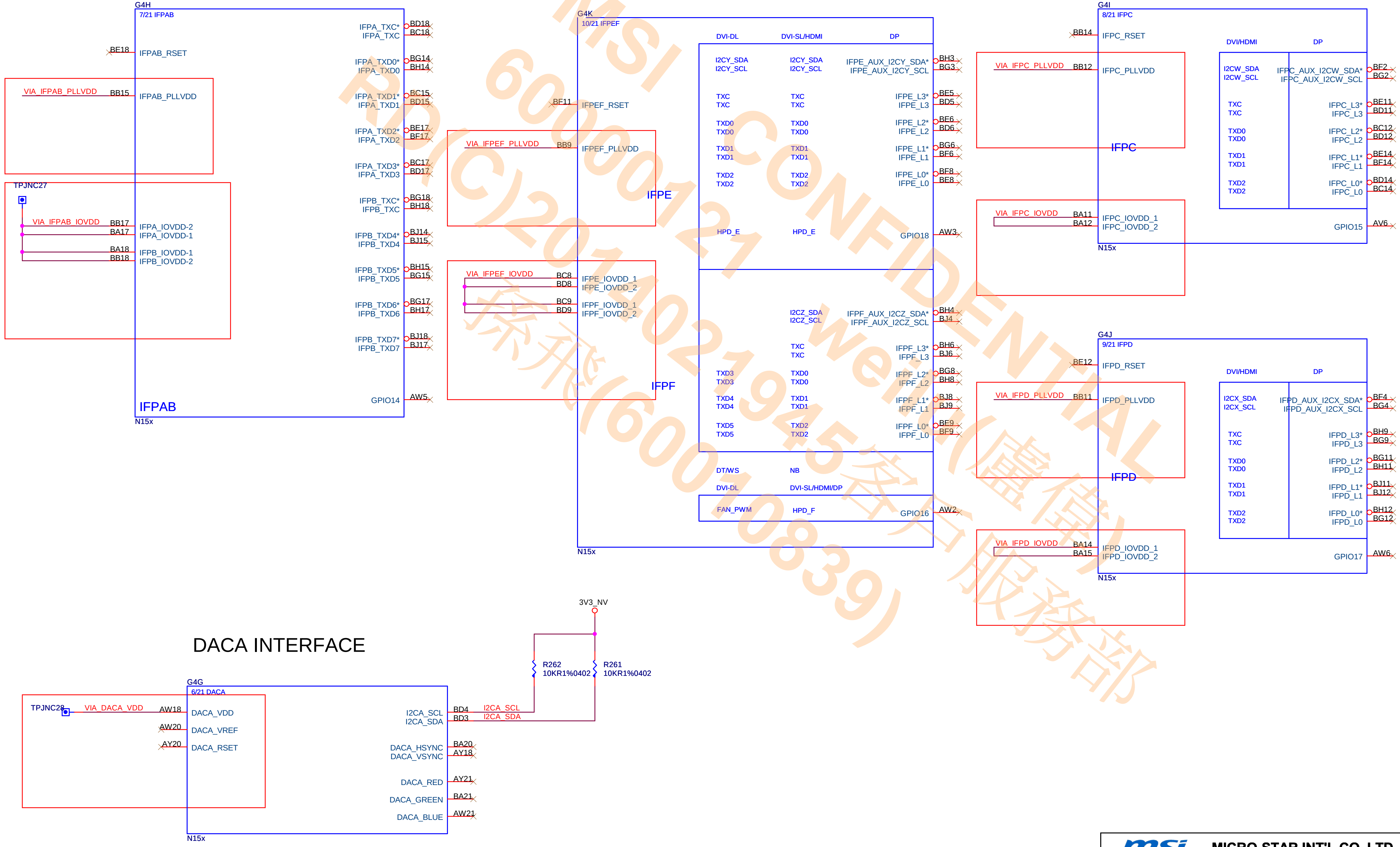
DACA,Display IF



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_DACA,Display IF
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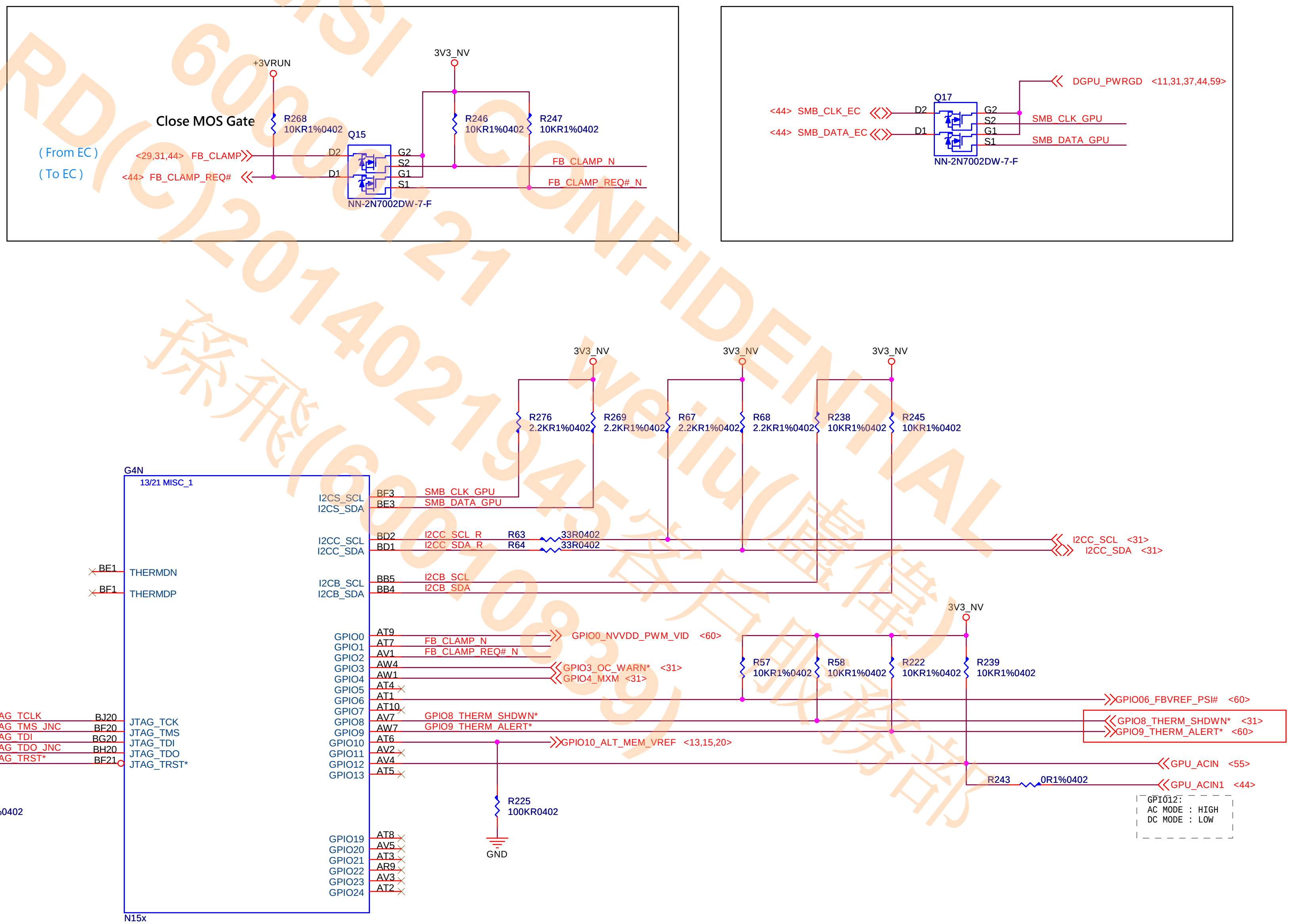
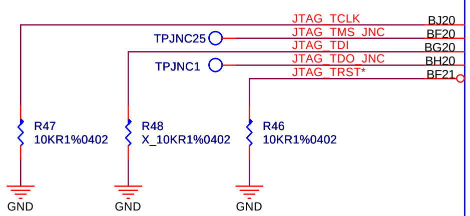
DGPU GPIO, I2C

GB3-256 GPIO(Design Guide Table 12-2)

GPIO	I/O	Function
0	OUT	PWM VID
1	IN	FB_CLAMP_MON
2	OUT	FB_CLAMP_MON_TGL_REQ
3	IN	OC_WARN
4	N/A	Reserved
5	N/A	Reserved
6	OUT	PSI
7	OUT	LCD PWM
8	OUT	OVERT
9	I/O	ALERT
10	OUT	MEM_VREF_CTL
11	OUT	LCD_VCC
12	IN	PWM LEVEL
13	OUT	LCD_BLEN
14	IN	HPD_AB
15	IN	HPD_C
16	IN	HPD_F or HPD_B
17	IN	HPD_D
18	IN	HPD_E
19	OUT	3DVision
20	N/A	Reserved
21	I/O	RASTER_SYNC
22	IN	SWAP_RDY
23	N/A	Reserved
24	OUT	MEM_VDD_CTL





MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GPIO,I2C
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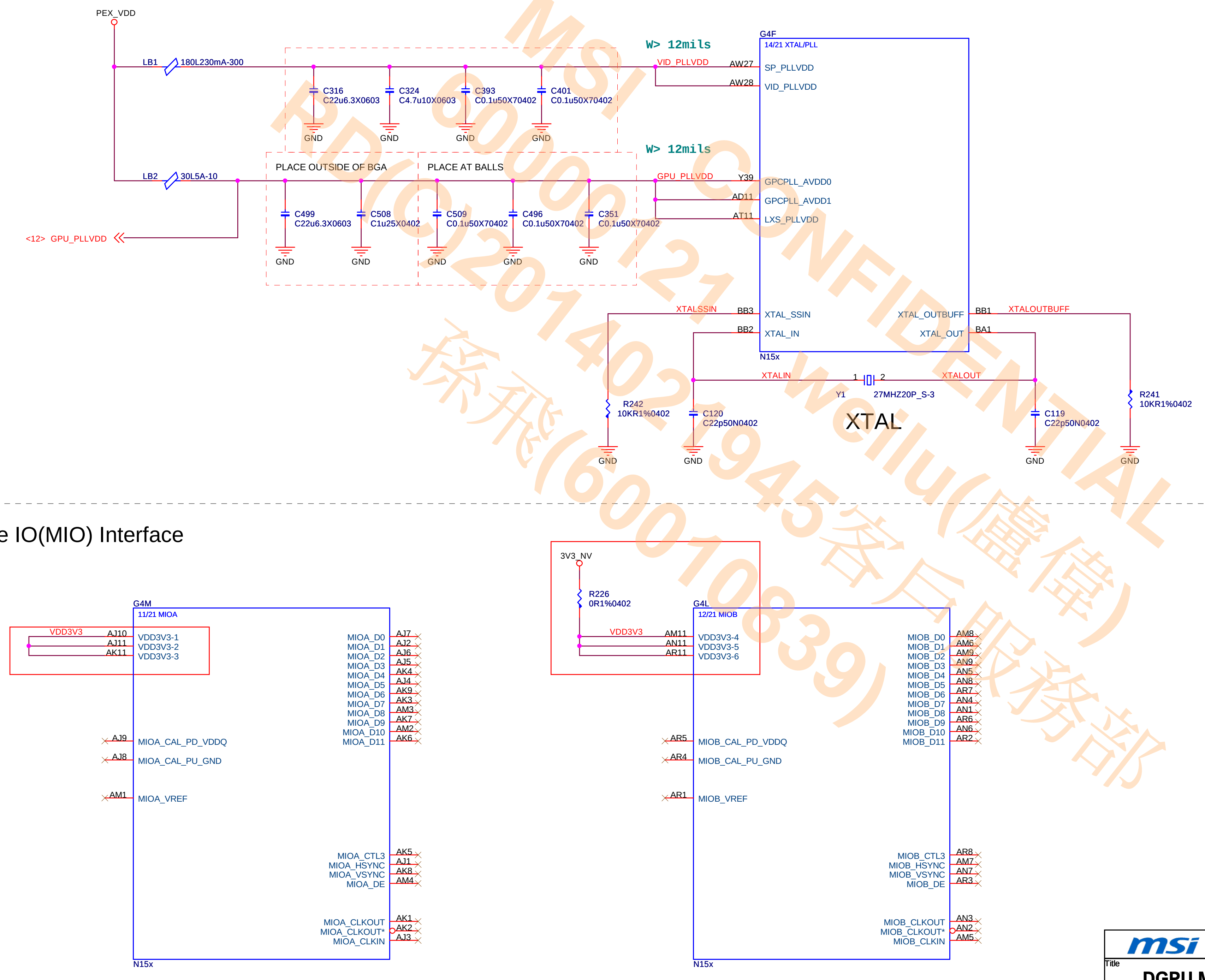
DGPU MIO & XTAL



MICRO-STAR INT'L CO.,LTD.

Title	DGPU MIO & XTAL	
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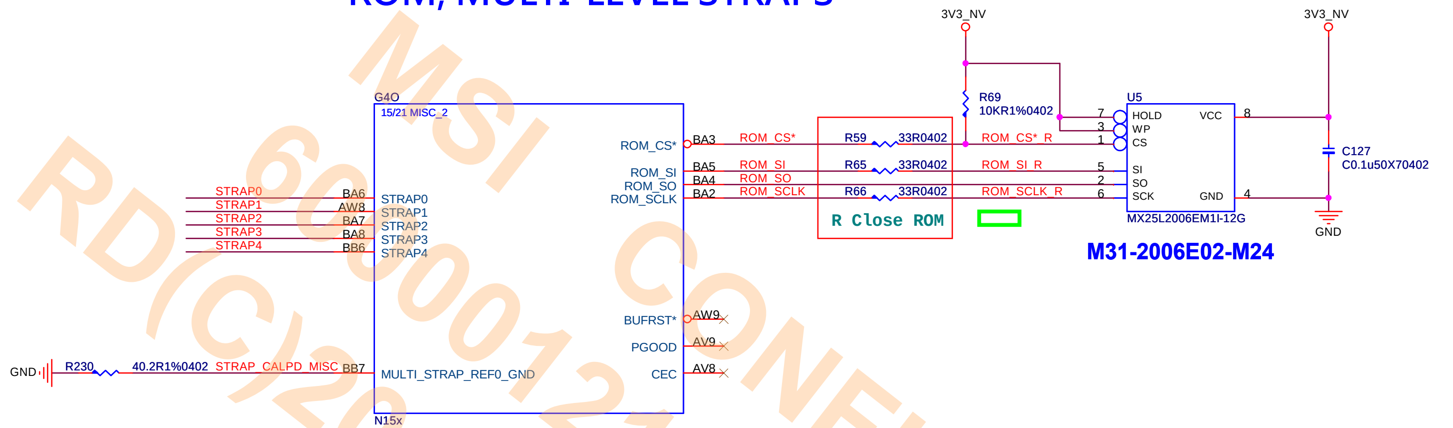
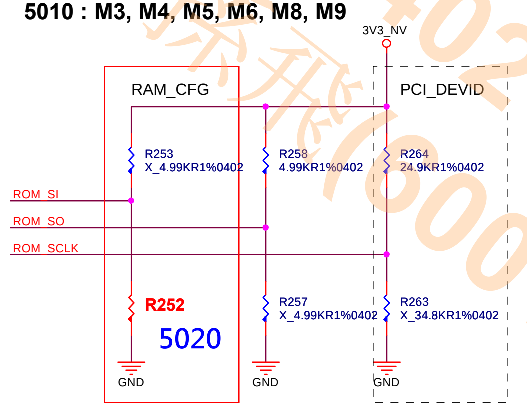
ROM, MULTI-LEVEL STRAPS

	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111
	PD	PU



RCFG1 Hynix 128Mx16bit R11-3482T12-W08 X_34.8KR1%0402	GDDR5M1 5010 M12-5GQ2HL5-H23 X_H5GQ2H24AFR	GDDR5M2 5020 M12-5GQ2HL5-H23 X_H5GQ2H24AFR
RCFG2 Samsung 128Mx16bit R11-4532T12-W08 X_45.3KR1%0402	GDDR5M3 5010 M12-2032585-S02 X_K4G20325FD	GDDR5M4 5020 M12-2032585-S02 X_K4G20325FD
RCFG3 Hynix 256Mx16bit R11-0153T12-W08 X_15KR1%0402	GDDR5M5 5010 M12-5GC4H05-H23 X_H5GC4H24MFR	GDDR5M6 5020 M12-5GC4H05-H23 X_H5GC4H24MFR
RCFG4 Elpida 256Mx16bit R11-0103T12-W08 X_10KR1%0402	GDDR5M7 5010 M12-4032B05-E59 X_EDW4032BABG	GDDR5M8 5020 M12-4032B05-E59 X_EDW4032BABG

GDDR5 Parts
5020 : M15, M16, M17, M18, M19, M20
5010 : M3, M4, M5, M6, M8, M9



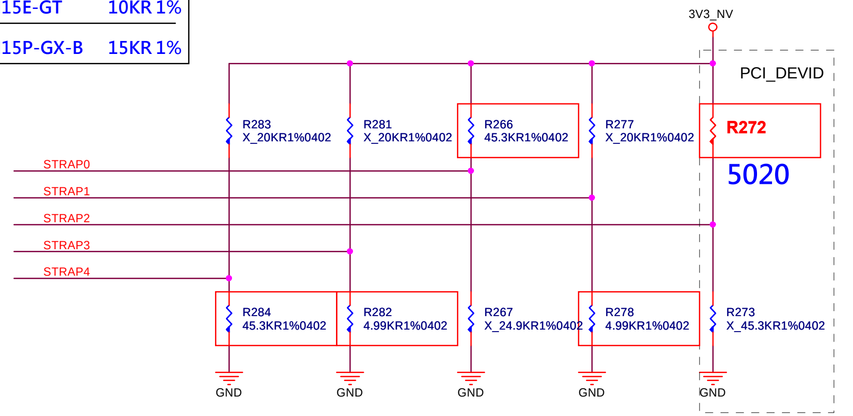
R252	
For Hynix 128Mx16	35KR 1%
For Samsung 128Mx16	45KR 1%
For Hynix 256Mx16	15KR 1%
For Elpida 256Mx16	10KR 1%

Setting	R252	5010	5020
Hynix 128Mx16	RCFG1	GDDR5M1	GDDR5M2
Samsung 128Mx16	RCFG2	GDDR5M3	GDDR5M4
Hynix 256Mx16	RCFG3	GDDR5M5	GDDR5M6
Elpida 256Mx16	RCFG4	GDDR5M7	GDDR5M8

STRAP0	USER_BIT[3:0]	0xF: EDID	45K PU	
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]	0x0: DDI no used	5K PD	
STRAP2	PCI_DEVID[3:0]	15E-GT 0x1199 15P-GX-B 0x119A	10K PU 15K PU	
ROM_SO	VGA_DEVICE SMB_ALT_ADDR FB_0_BAR_SIZE XCLK_417	0x0001	5K PU	
ROM_SI	RAM_CFG_0 RAM_CFG_1 RAM_CFG_2 RAM_CFG_3	0110 0111 0010 0001	35K PD 45K PD 15K PD 10K PD	Hynix 128x16bit Samsung 128x16bit Hynix 256xbit Elpida 256xbit
ROM_SCLK	PCI_DEVID[4] SUB_VENDOR PCI_DEVID[5] PEX_PLL_EN_TERM100	1: 0x119=>1001 1: VBIOS ROM is Present 0: 0x119=>1001	25K PU	
STRAP3	SOR_EXposed [3:0]	0000	5K PD	
STRAP4	Reserved PCIE_Speed_Change_Gen3 PCIE_MAX_SPEED DP_PLL_VDD_33V	0 1: Enable PCIE Gen3 operation 1: Allow booting to GEN2/Gen3 1: ENABLED	45K PD	

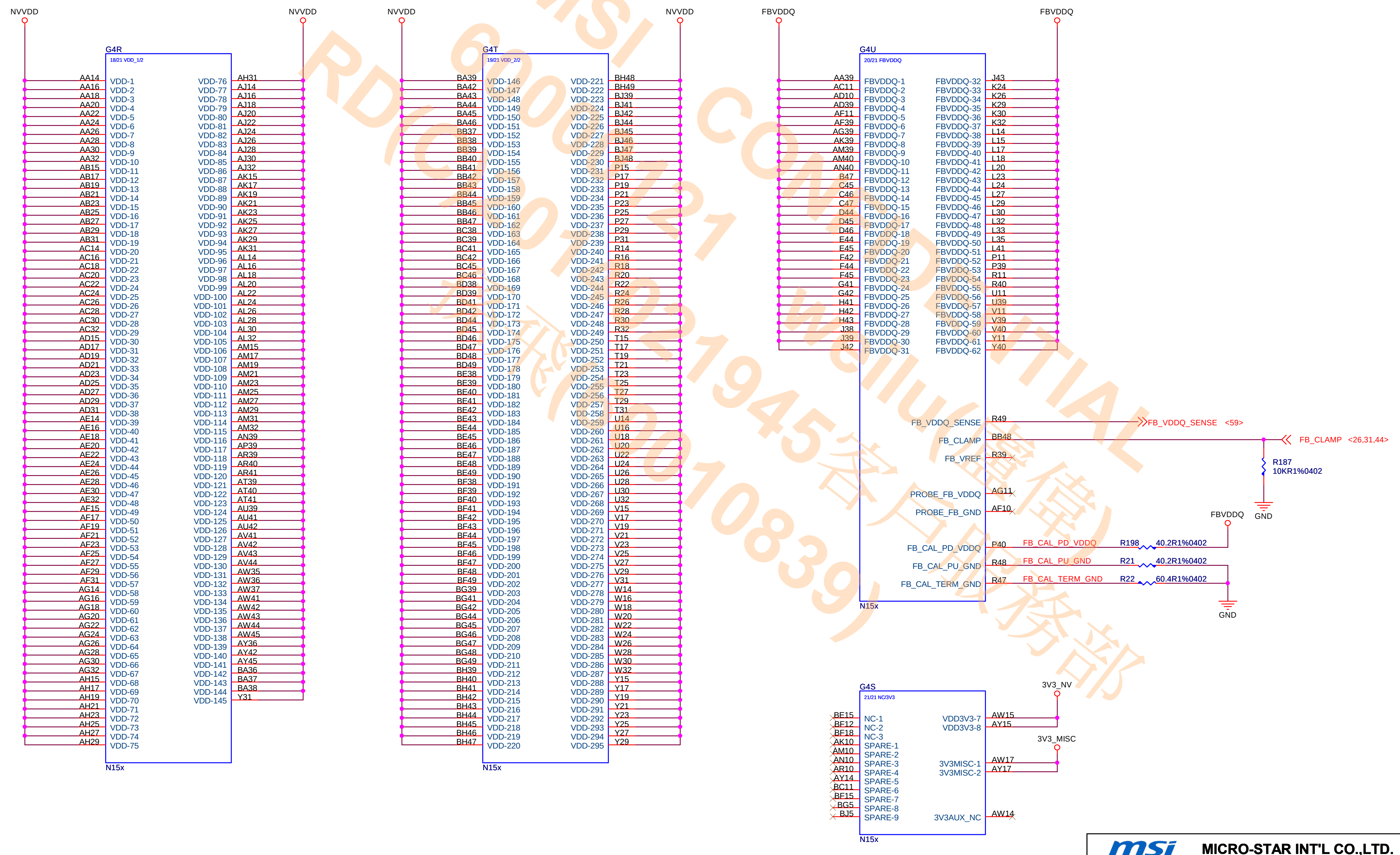
RGPU1 N15E-GT 5020 R11-0103T12-W08 X_10KR1%0402	
DGPU1 5010 B03-0N15E05-N08 X_N15E-GT-A2	
RGPU2 N15P-GX-B 5020 R11-0153T12-W08 X_15KR1%0402	
DGPU2 5010 OB3-16H2001 X_N15P-GX-B-A2	

R272	
N15E-GT	10KR 1%
N15P-GX-B	15KR 1%



MICRO-STAR INT'L CO.,LTD.
Title: **DGPU_ROM,HW Straps**
Size | Document Number: **MS-16H2** | Rev: **0A**
Date: Friday, September 06, 2013 | Sheet 28 of 71

GPU NVVDD, FBVDDQ



MICRO-STAR INT'L CO.,LTD.

Title: DGPU NVVDD, FBVDDQ

Size | Document Number: MS-16H2 | Rev: 0A

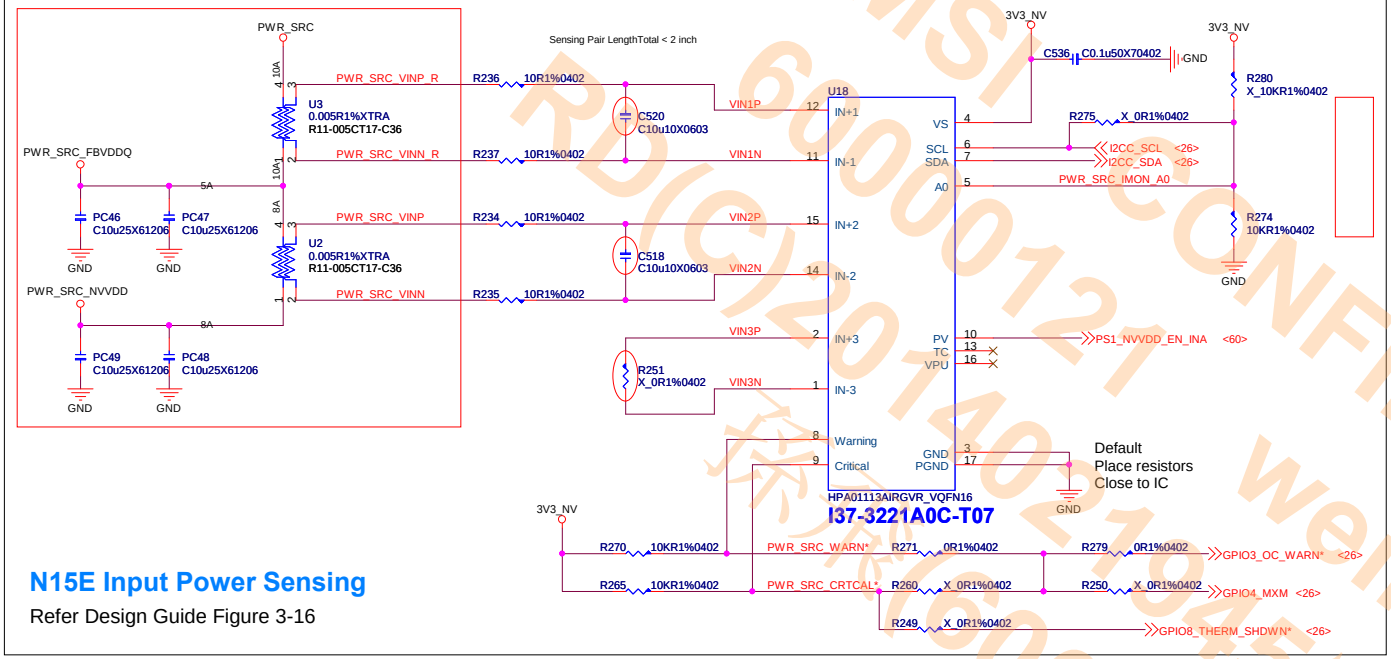
Date: Thursday, September 05, 2013 | Sheet 29 of 71

DGPU GND

MICRO-STAR INT'L CO.,LTD.

Title	DGPU GND	
Size	Document Number: MS-16H2	Rev: 0A
Date: Thursday, September 05, 2013	Sheet 30 of 71	

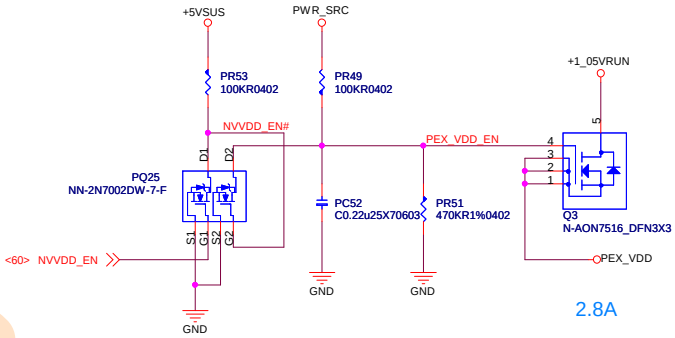
DGPU_Power Control

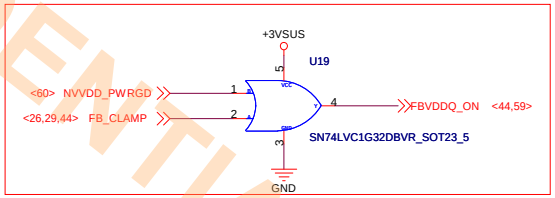


N15E Input Power Sensing

Refer Design Guide Figure 3-16

PEX_VDD





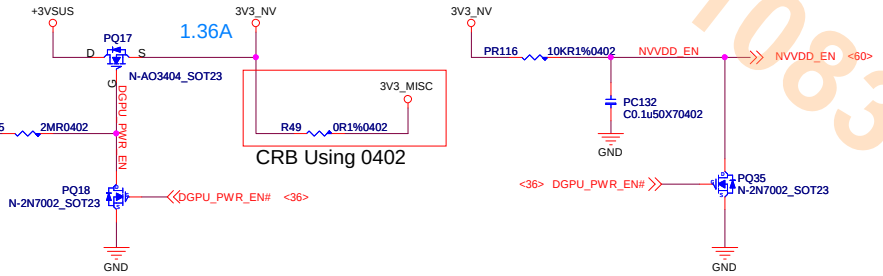
nVIDIA Power Sequence Control

3V3_NV -> NVVDD, PEX_VDD -> FBVDDQ -> DGPUPWRGD

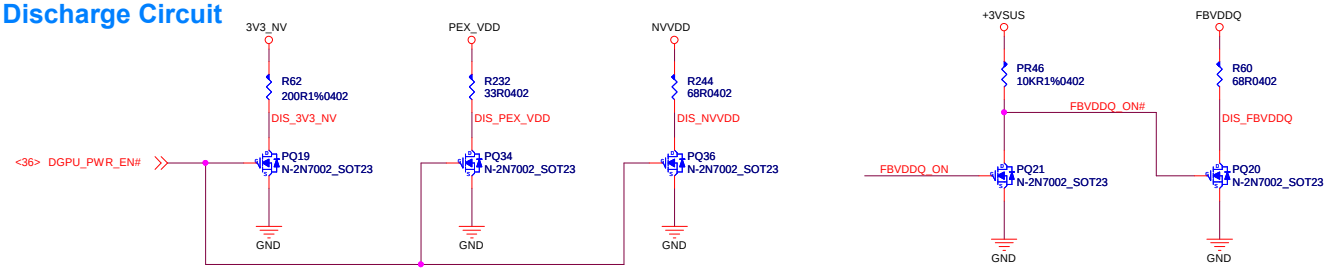
3V3_NV

EDP Design Guide:
N15E-GT(90W)Sku
NVVDD : 60A ; Peak 110A
3V3_RUN : 1.36A
PEX_VDD : 2.8A

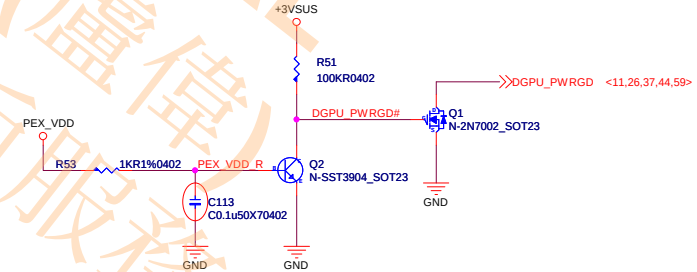
VRAM : 0.93A*12pcs=11.16A



Discharge Circuit



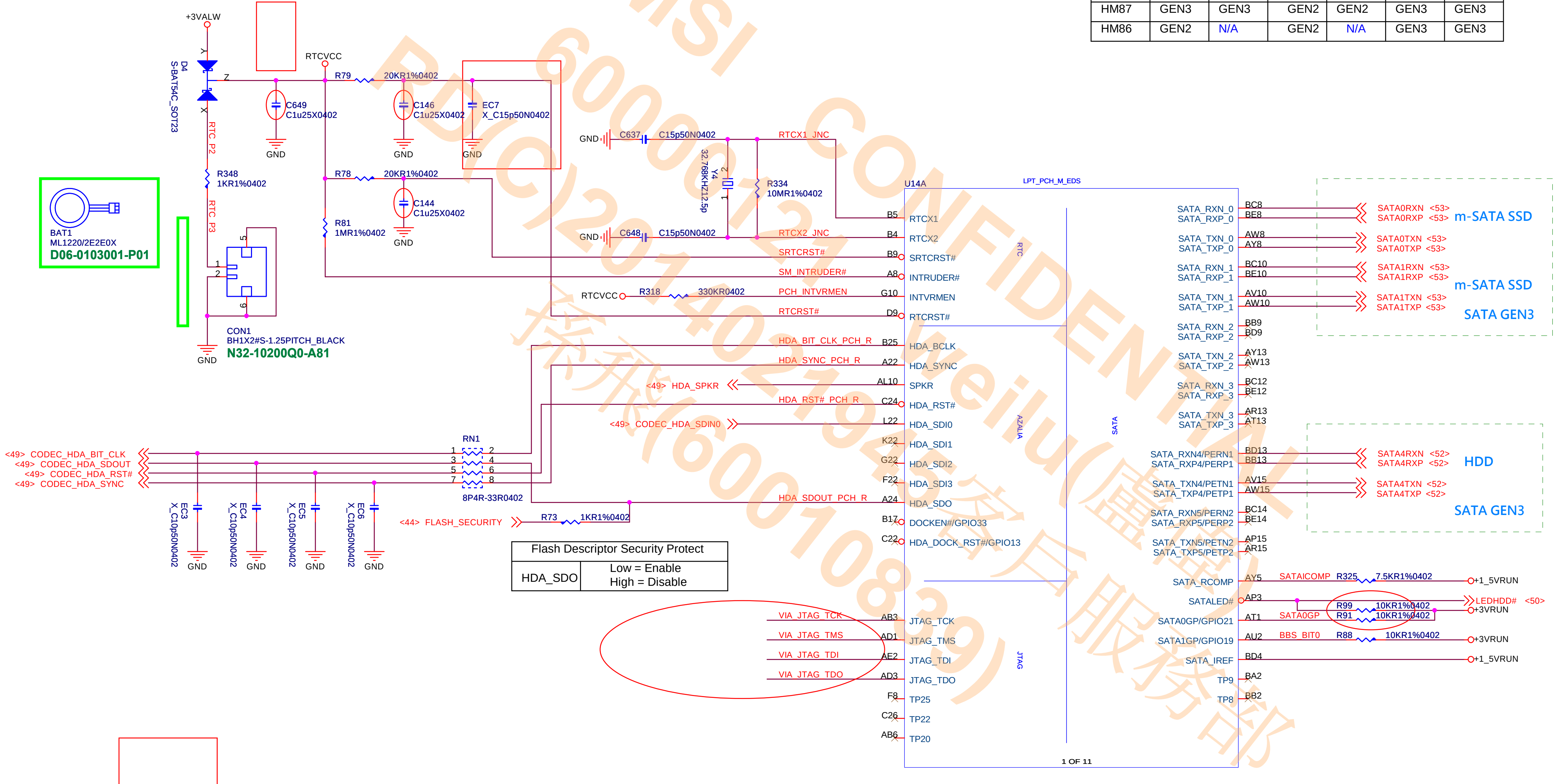
3V3_MISC



MICRO-STAR INT'L CO.,LTD.		
Title: DGPU_Power Control		
Size	Document Number: MS-16H2	Rev: 0A
Date: Thursday, September 05, 2013	Sheet 31 of 71	

Lynx Point (HDA/JTAG/SATA)

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3



Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

SPK	The Signal has a weak internal pull-down Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)

MICRO-STAR INT'L CO.,LTD.

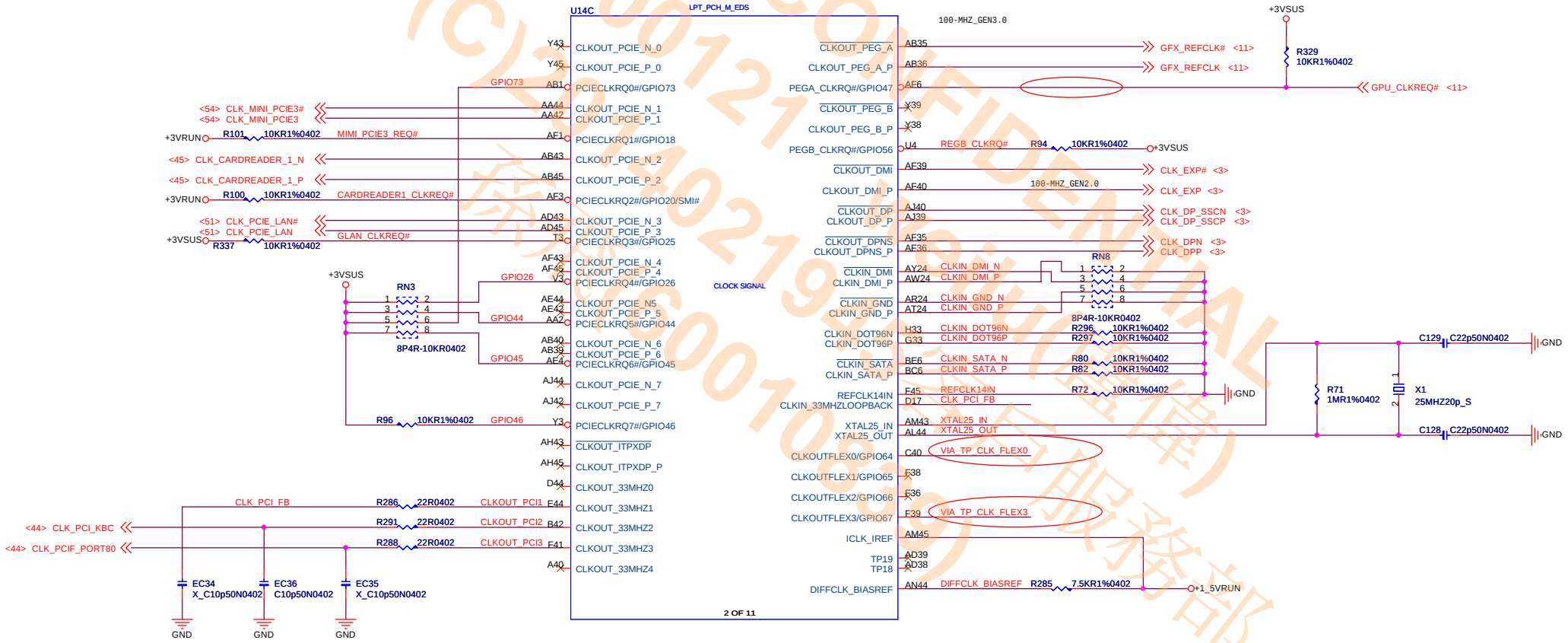
Title: PCH-1 (HDA/JTAG/SATA)

Size | Document Number: MS-16H2 | Rev: 0A

Date: Thursday, September 05, 2013 | Sheet 32 of 71

Lynx Point (Clock)

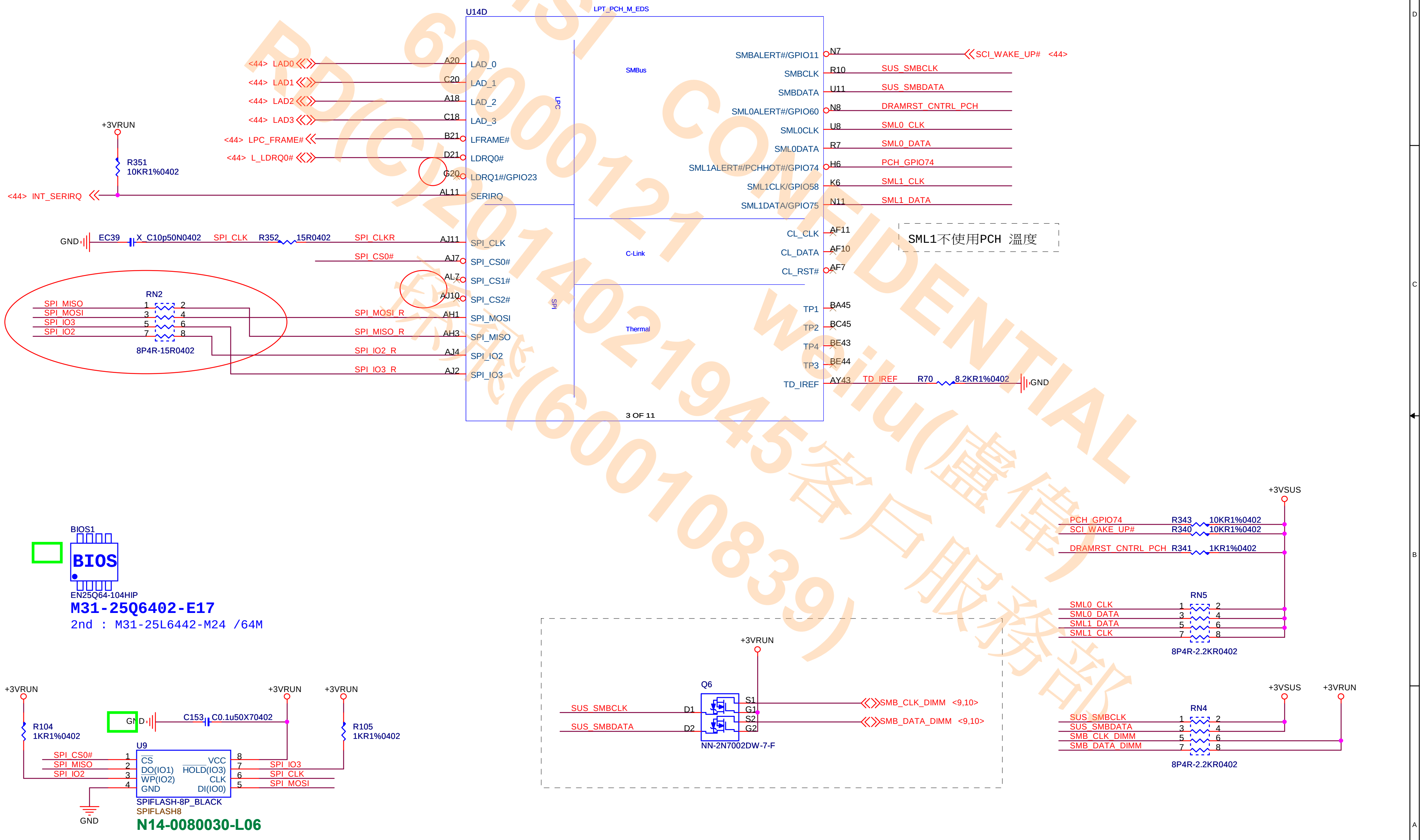
PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 kΩ ±10% external pull-up resistor instead of No Connect.
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.



The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

MICRO-STAR INT'L CO.,LTD.		
Title: PCH-2 (CLK)		
Size	Document Number: MS-16H2	Rev: 0A
Date: Thursday, September 05, 2013	Sheet 33 of 71	

Lynx Point (LPC,SMBUS)



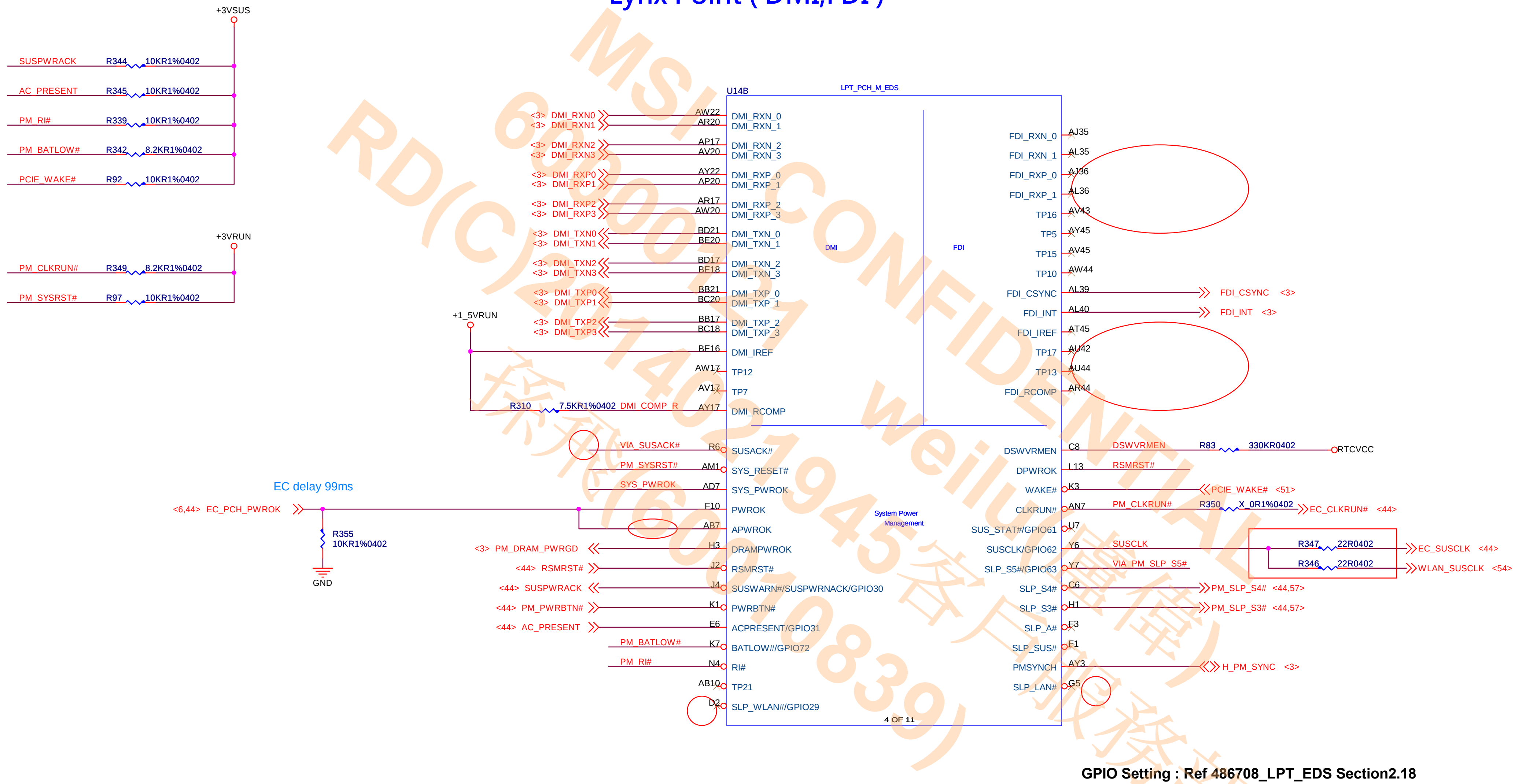
MICRO-STAR INT'L CO.,LTD.

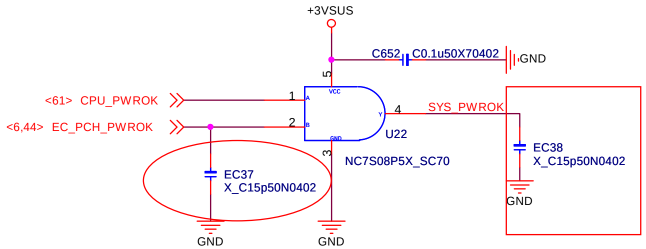
Title: PCH-3 (LPC,SMBUS)

Size | Document Number: MS-16H2 | Rev: 0A

Date: Thursday, September 05, 2013 | Sheet 34 of 71

Lynx Point (DMI,FDI)





APWROK not supporting Intel AMT , it can be connected to PWROK
GPIO31 : If not used,require pull up +3VSUS
DSWVRMEN - On Die DSW VR Enable HIGH : Enable internal 1.05V regulator LOW : Disable
DPWROK Without deep s4/s5 support tied together with RSMRST#

GPIO Setting : Ref 486708_LPT_EDS Section2.18

PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

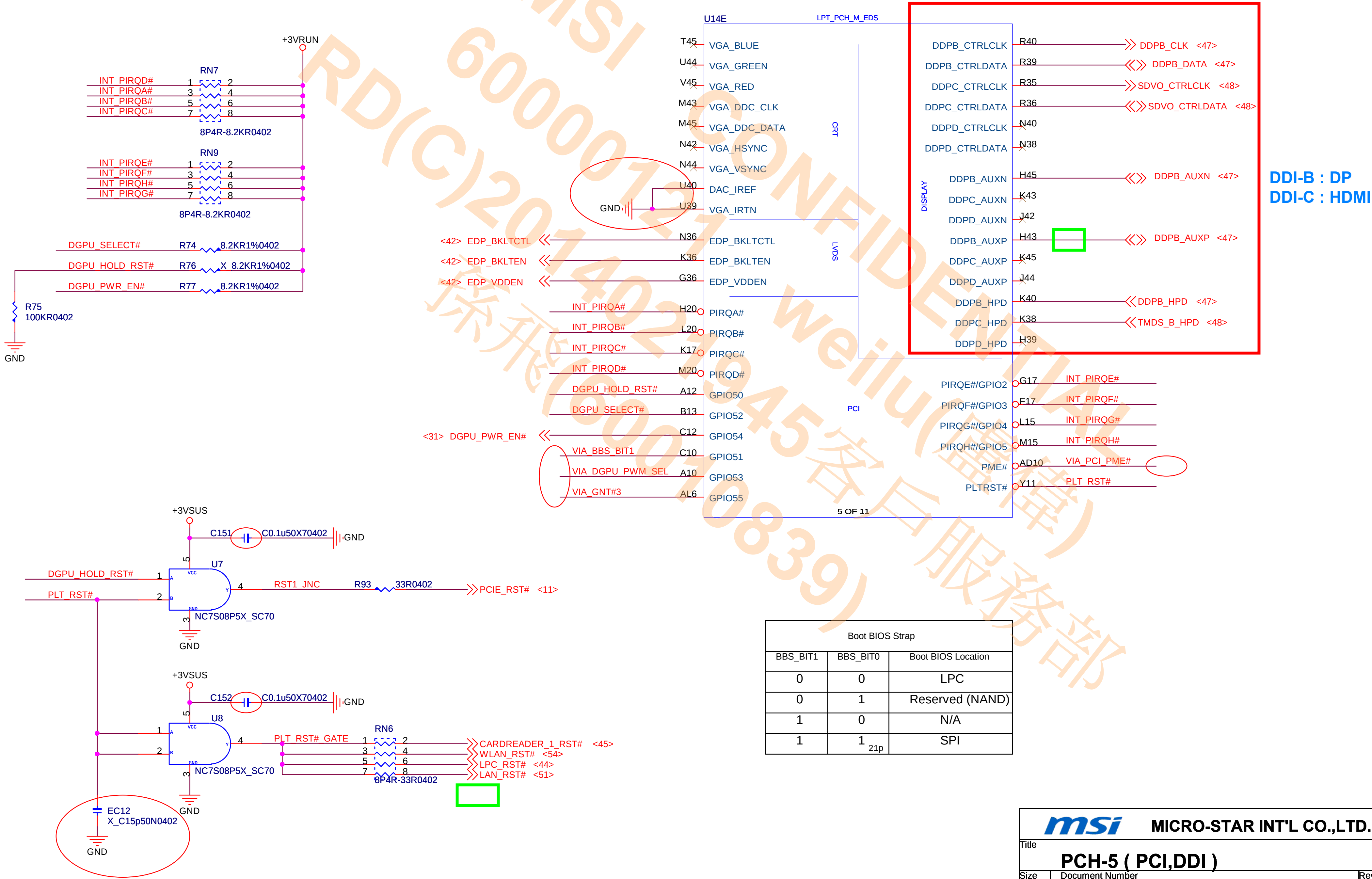
MICRO-STAR INT'L CO.,LTD.

Title: PCH-4 (DMI,FDI)

Size	Document Number	Rev
	MS-16H2	0A

Date: Thursday, September 05, 2013 Sheet 35 of 71

Lynx Point (PCI,DDI)



Boot BIOS Strap

BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1 21p	SPI

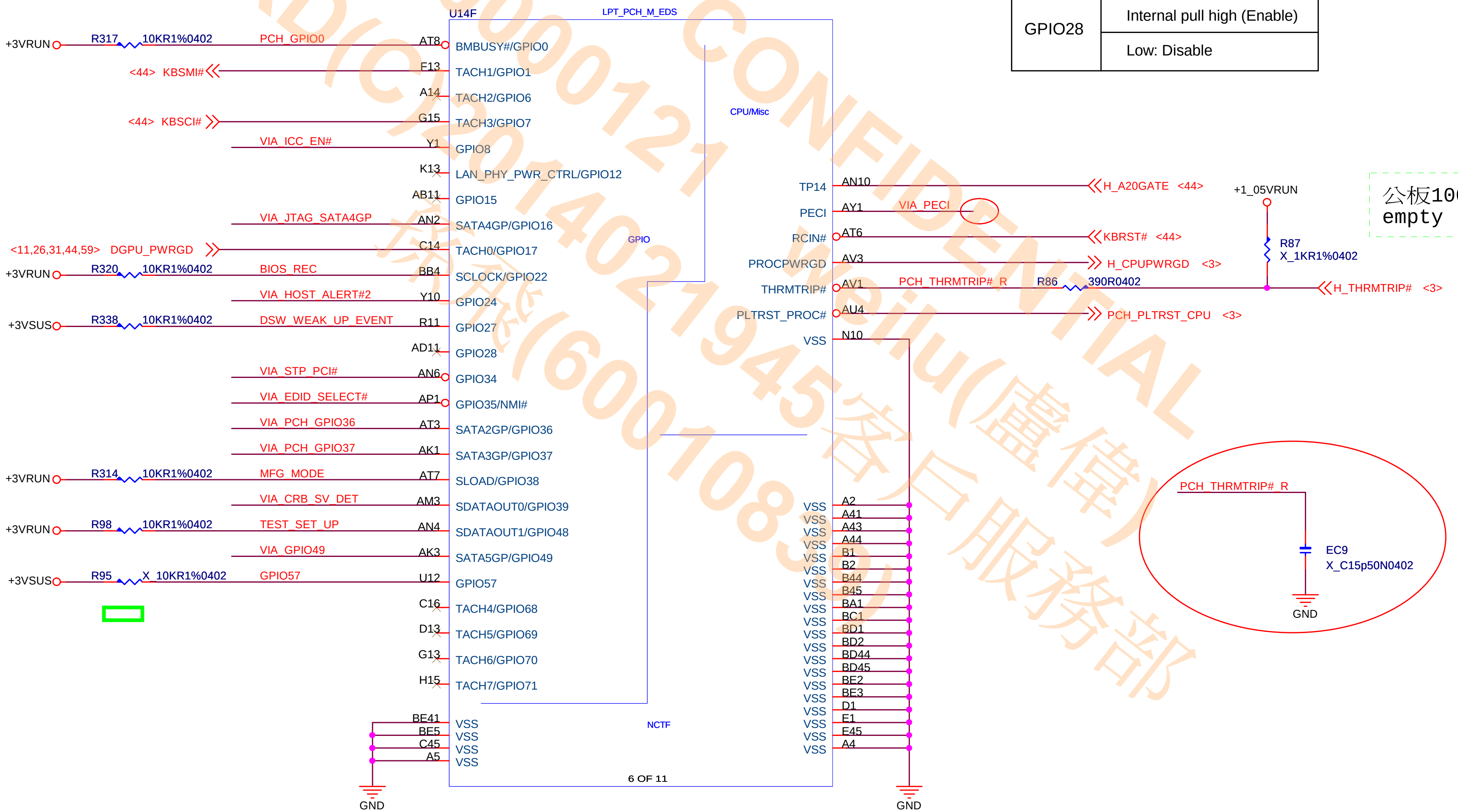
msi MICRO-STAR INT'L CO.,LTD.

Title	PCH-5 (PCI,DDI)	
Size	Document Number: MS-16H2	Rev: 0A
Date: Thursday, September 05, 2013	Sheet 36 of 71	

Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

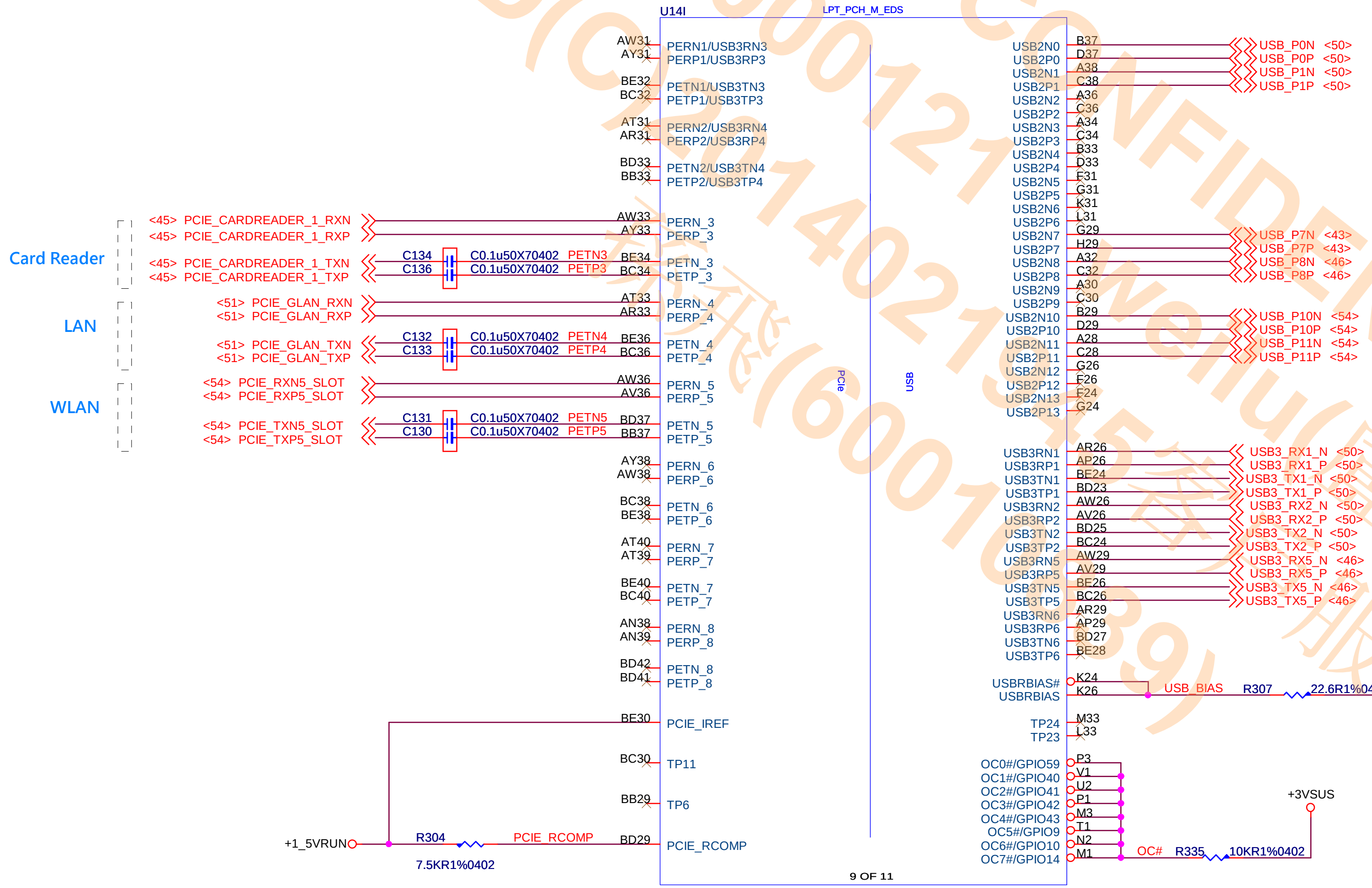


MICRO-STAR INT'L CO.,LTD.

Title	PCH-6 (GPIO,MISC)	
Size	Document Number: MS-16H2	Rev: 0A
Date: Thursday, September 05, 2013	Sheet 37 of 71	

Lynx Point (PCIE,USB)

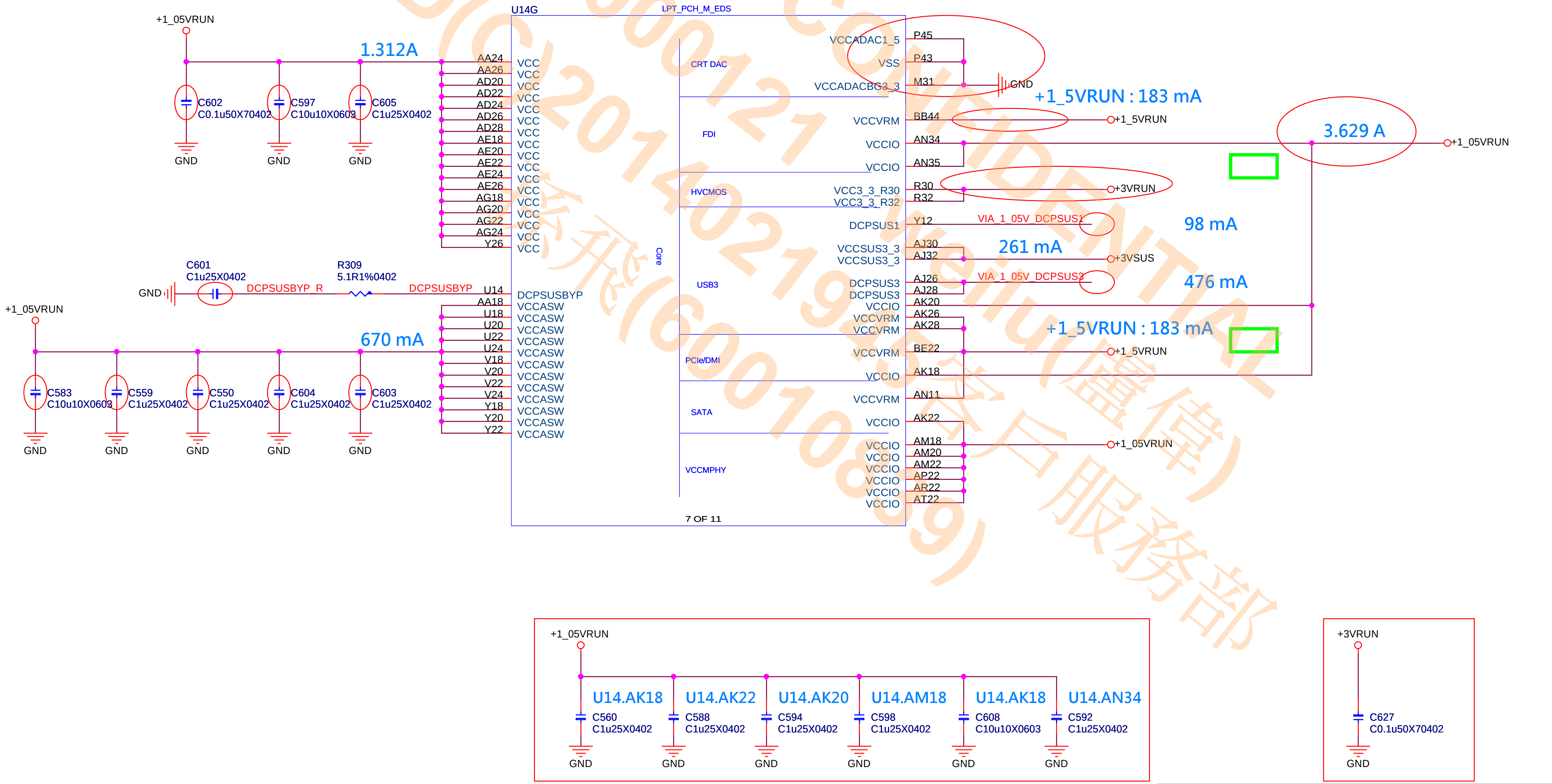
Intel Lynx Point ECHI USB(2.0) debug transport 需接Port1 or Port9



USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	16H2A
1	2	USB 3.0 Port 2	16H2A
2			NC
3			NC
4			NC
5			NC
6			NC
7		EPF021	3 色KBC
8	3	USB 3.0 Port 5	16H21
9			NC
10		WLAN	
11		WebCam	
12		SECOND DISPLAY	
13			NC

HM86 沒USB3.0 PORT 5,6

Lynx Point (Power)



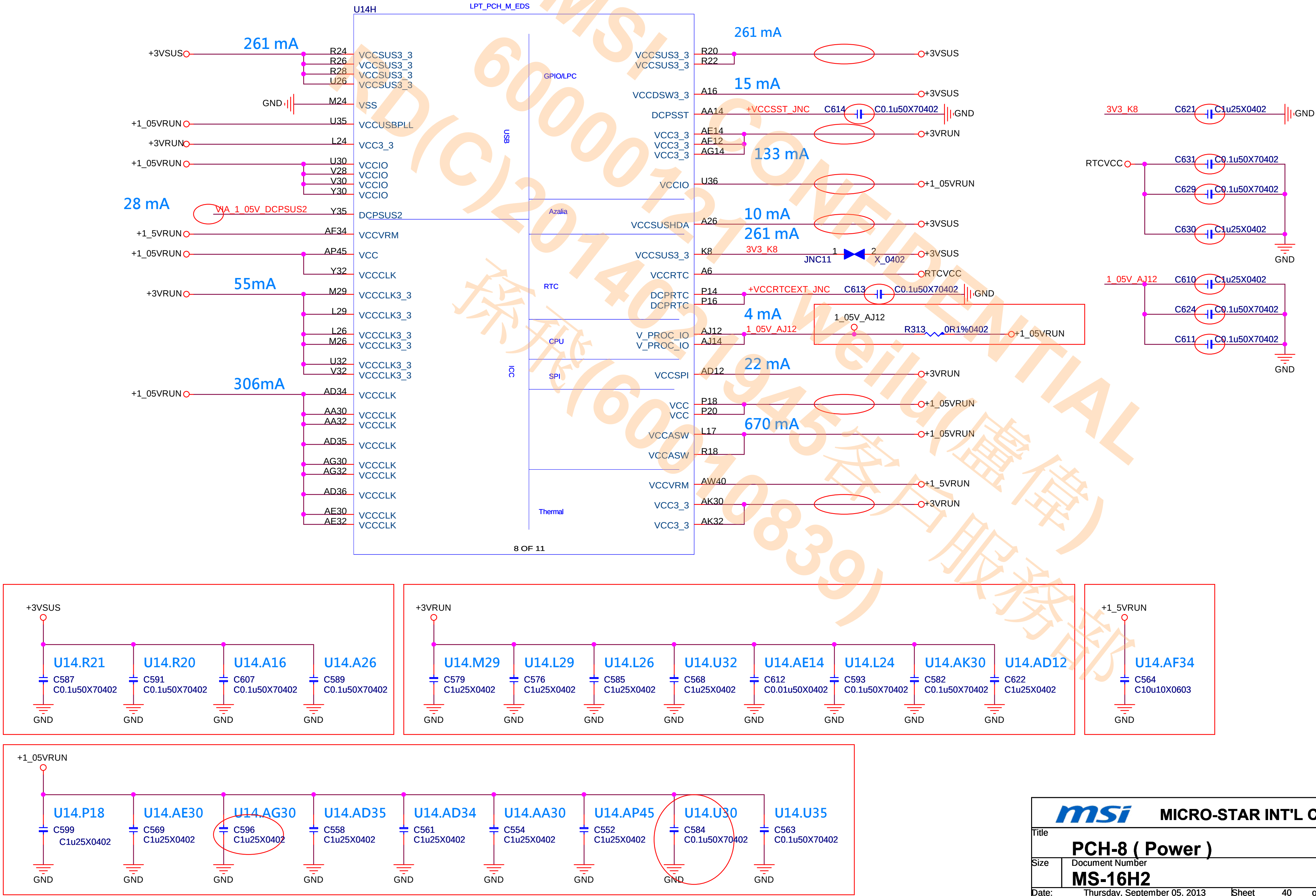
MICRO-STAR INT'L CO.,LTD.

Title: PCH-8 (Power)

Size | Document Number: MS-16H2 | Rev: 0A

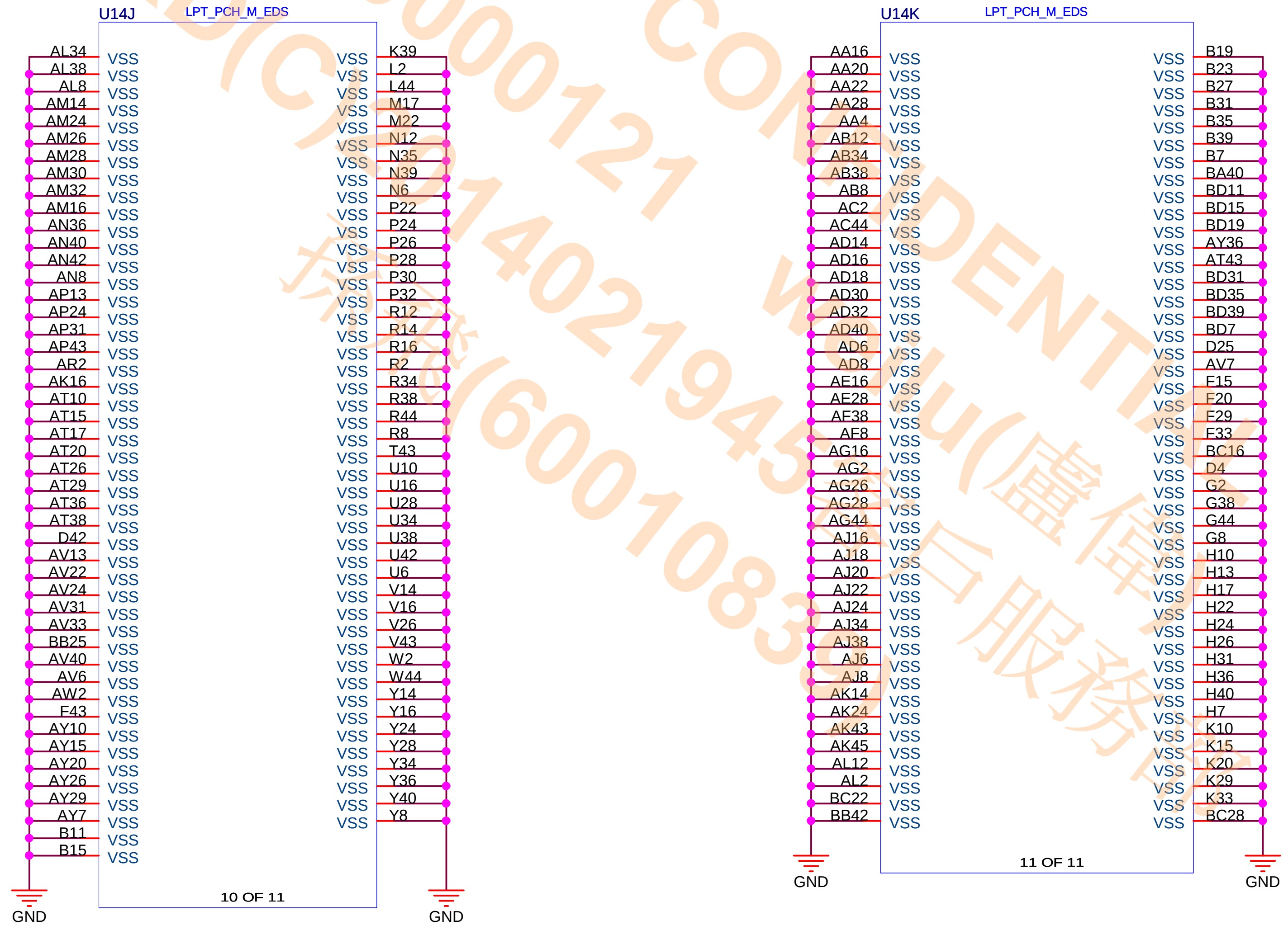
Date: Thursday, September 05, 2013 | Sheet 39 of 71

Lynx Point (Power)



msi	MICRO-STAR INT'L CO.,LTD.	
Title	PCH-8 (Power)	
Size	Document Number MS-16H2	Rev 0A
Date: Thursday, September 05, 2013	Sheet 40 of 71	

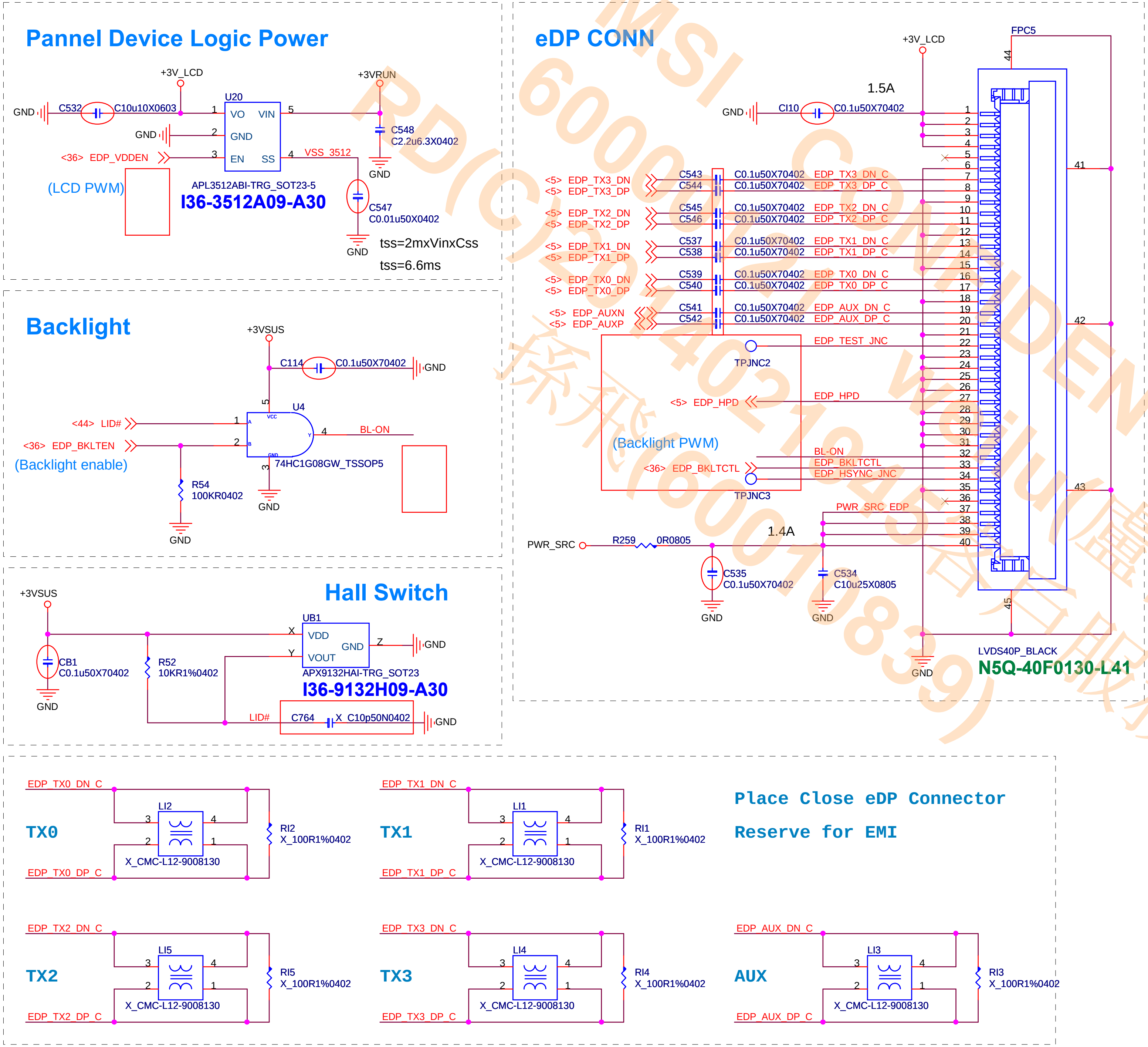
Lynx Point (GND)



MICRO-STAR INT'L CO.,LTD.

Title	PCH-8 (GND)	
Size	Document Number: MS-16H2	Rev: 0A
Date: Thursday, September 05, 2013	Sheet 41 of 71	

eDP Connector



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

msi MICRO-STAR INT'L CO.,LTD.
Title: eDP Connector
Size | Document Number: MS-16H2 | Rev: 0A
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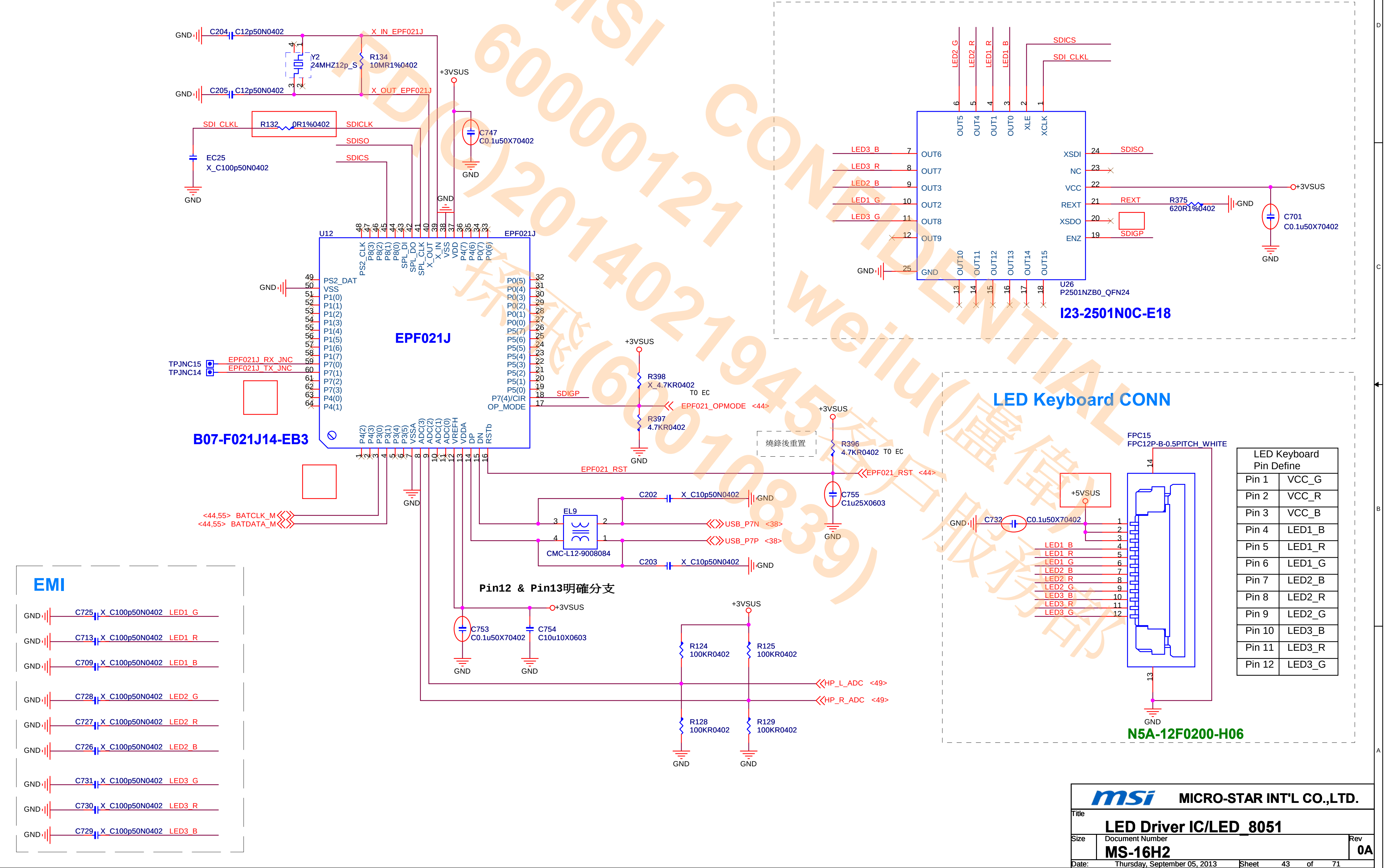
LED 8051 Controller



LED Keyboard Pin Define

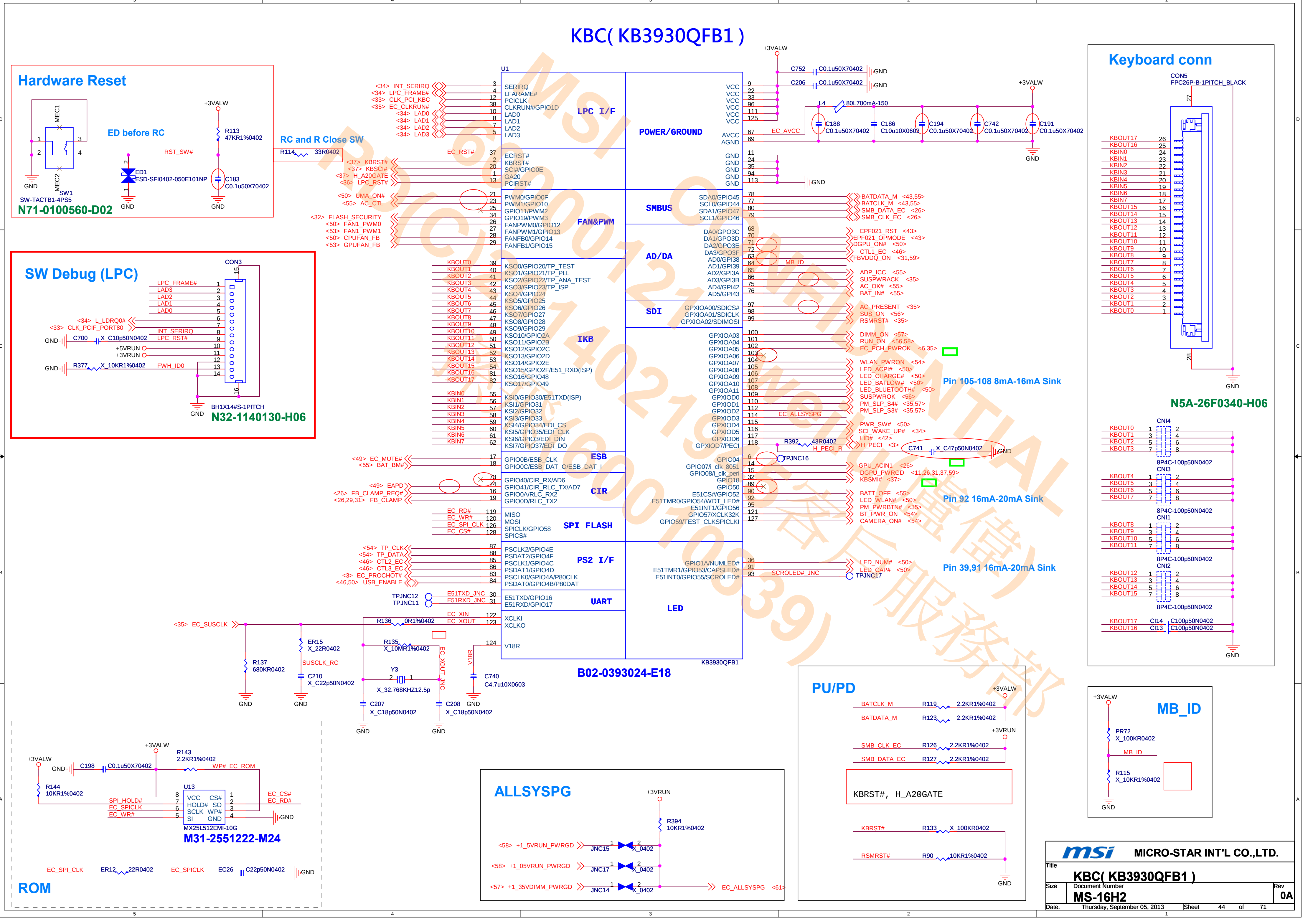
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

MICRO-STAR INT'L CO.,LTD.

Title: LED Driver IC/LED_8051

Size | Document Number: MS-16H2 | Rev: 0A

Date: Thursday, September 05, 2013 | Sheet 43 of 71


KBC(KB3930QFB1)
Hardware Reset
ED before RC
RC and R Close SW
SW-TACTB1-4PS5
N71-0100560-D02
SW Debug (LPC)
BH1X14#S-1PITCH
N32-1140130-H06
LPC I/F
POWER/GROUND
SMBUS
FAN&PWM
AD/DA
SDI
IKB
ESB
CIR
SPI FLASH
PS2 I/F
UART
LED
B02-0393024-E18
KB3930QFB1
Keyboard conn
FPC26P-B-1PITCH_BLACK
N5A-26F0340-H06
Pin 105-108 8mA-16mA Sink
Pin 92 16mA-20mA Sink
Pin 39,91 16mA-20mA Sink
PU/PD
KBRST#, H_A20GATE
MB_ID
ALLSYSPG
ROM
MX25L512EMI-10G
M31-2551222-M24
MICRO-STAR INT'L CO.,LTD.
Title
KBC(KB3930QFB1)
Size
Document Number
MS-16H2
Rev
0A
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CardReader (RTS5227)

RTS5249 Colay RTS5227

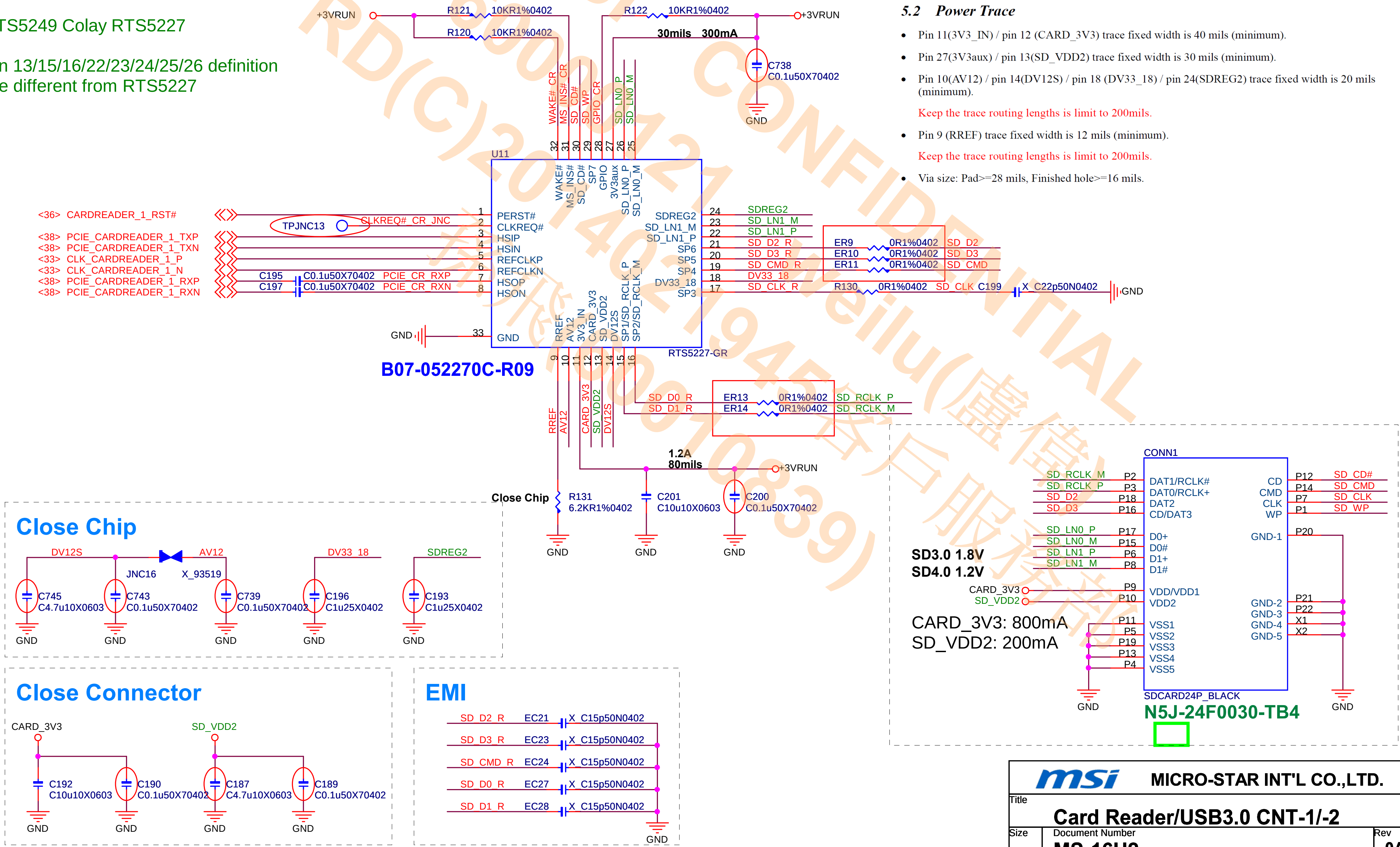
Pin 13/15/16/22/23/24/25/26 definition are different from RTS5227

5.2 *Power Trace*

- Pin 11(3V3_IN) / pin 12 (CARD_3V3) trace fixed width is 40 mils (minimum).
- Pin 27(3V3aux) / pin 13(SD_VDD2) trace fixed width is 30 mils (minimum).
- Pin 10(AV12) / pin 14(DV12S) / pin 18 (DV33_18) / pin 24(SDREG2) trace fixed width is 20 mils (minimum).

  Keep the trace routing lengths is limit to 200mils.
- Pin 9 (RREF) trace fixed width is 12 mils (minimum).

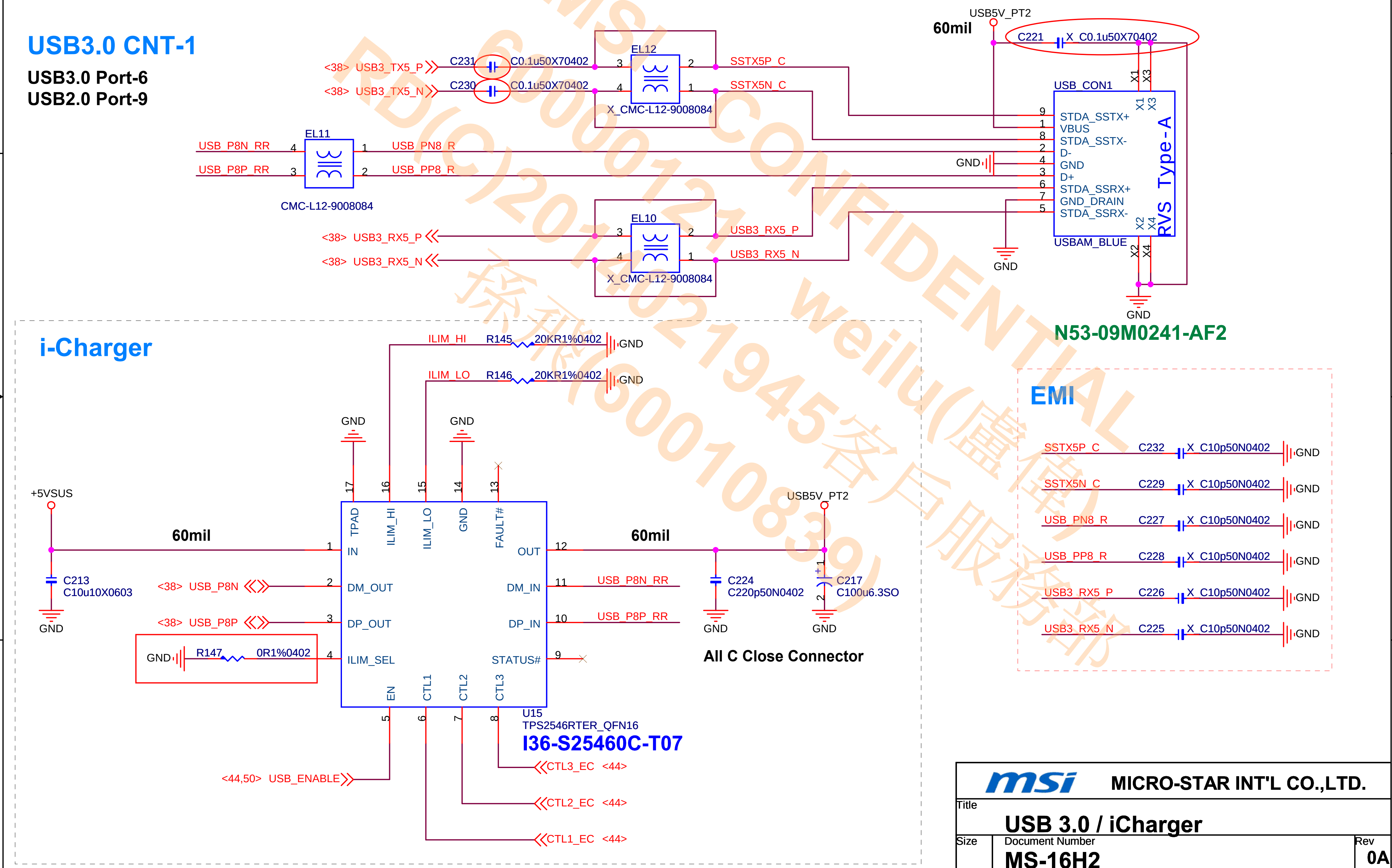
  Keep the trace routing lengths is limit to 200mils.
- Via size: Pad>=28 mils, Finished hole>=16 mils.



MICRO-STAR INT'L CO.,LTD.

Title	Card Reader/USB3.0 CNT-1/-2	
Size	Document Number: MS-16H2	Rev: 0A
Date: Thursday, September 05, 2013	Sheet 45 of 71	

USB 3.0 / iCharger



MICRO-STAR INT'L CO.,LTD.

Title	USB 3.0 / iCharger
Size / Document Number	MS-16H2
Rev	0A
Date:	Thursday, September 05, 2013
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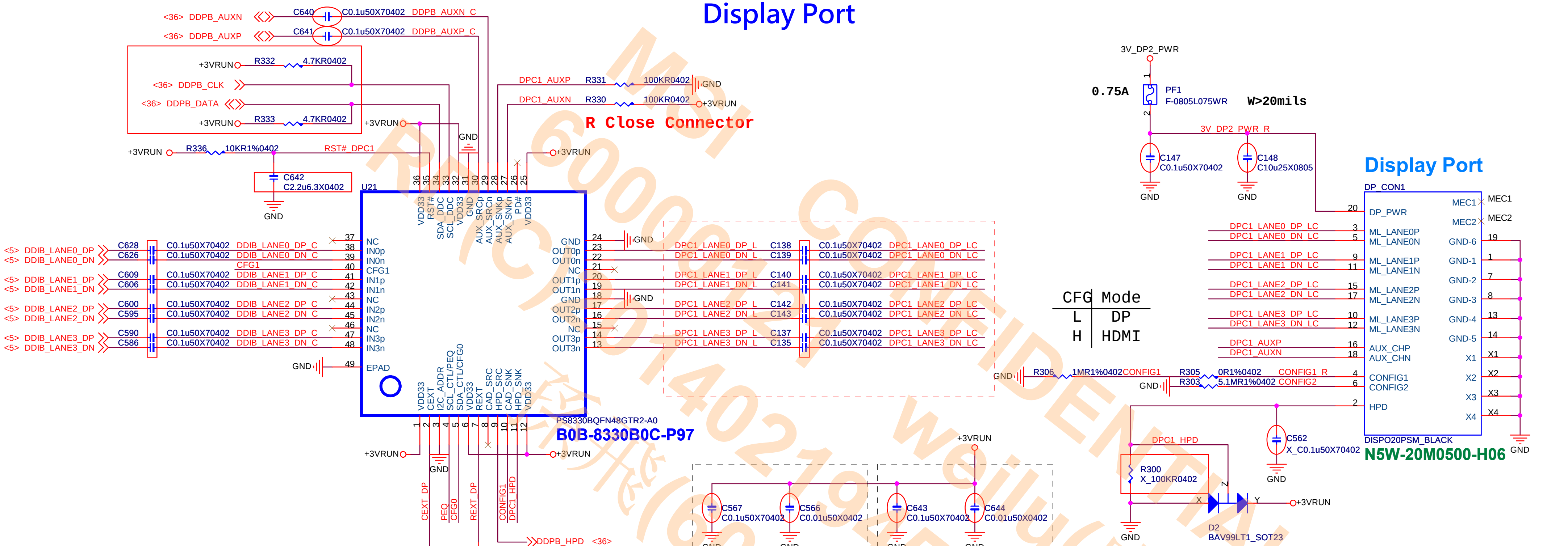
Display Port

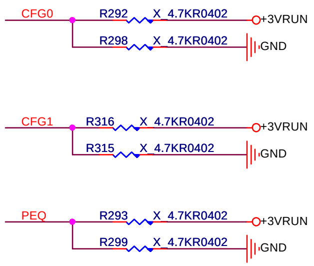


3 Level Input:
- L: LOW
- H: HIGH
- M: VDD33/2, connect both pull-up and pull-down resistors

The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

HPD_SNK Have internal Pull down 150kohm.
No problem with Leakage from DP device

CAD_SNK Have internal Pull down 1Mohm.

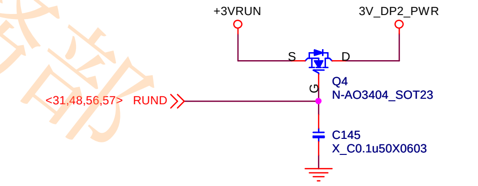


Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
- L: default, automatic EQ enable & AUX interception enable
- H: automatic EQ disable & AUX interception enable
- M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

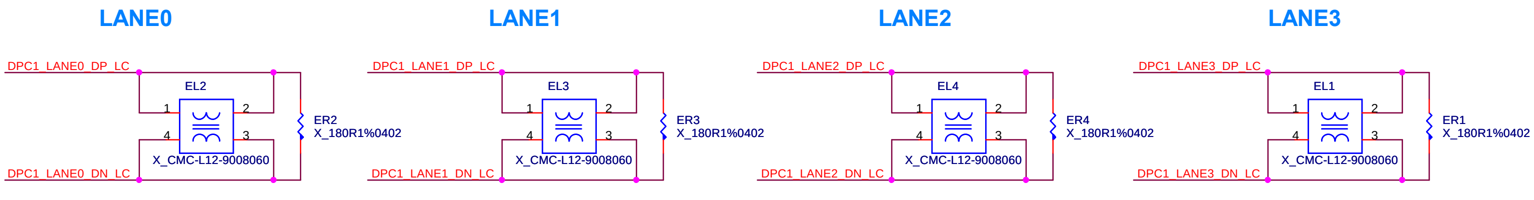
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
- H: default, auto test disable & input offset cancellation enable
- L: auto test enable & input offset cancellation enable
- M: auto test disable & input offset cancellation disable

Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.
- L: default, LEQ, compensate channel loss up to 12dB @ HBR2
- H: HEQ, compensate channel loss up to 15dB @ HBR2
- M: LLEQ, compensate channel loss up to 5dB @ HBR2

Avoid DP Leakage



EMI Close Connector



msi	MICRO-STAR INT'L CO.,LTD.
Title	DP witch Repeater
Size / Document Number	MS-16H2
Rev	0A
Date:	Thursday, September 05, 2013
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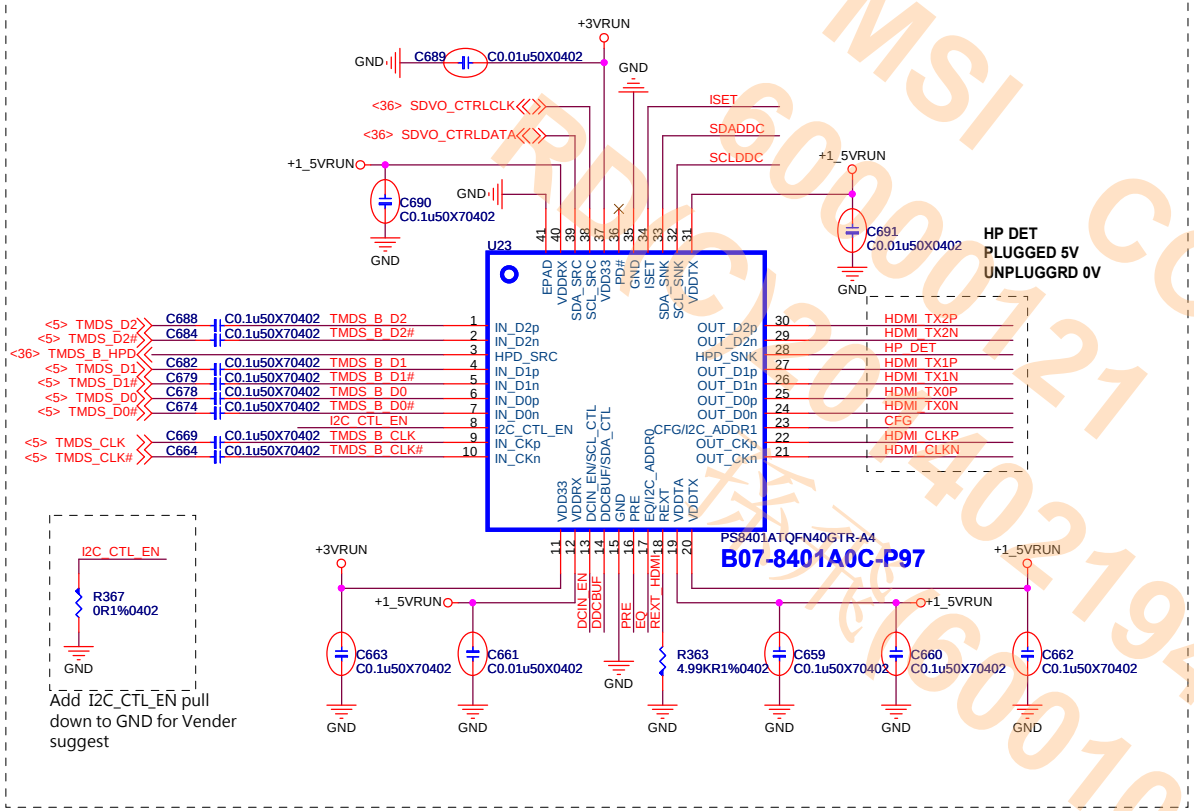
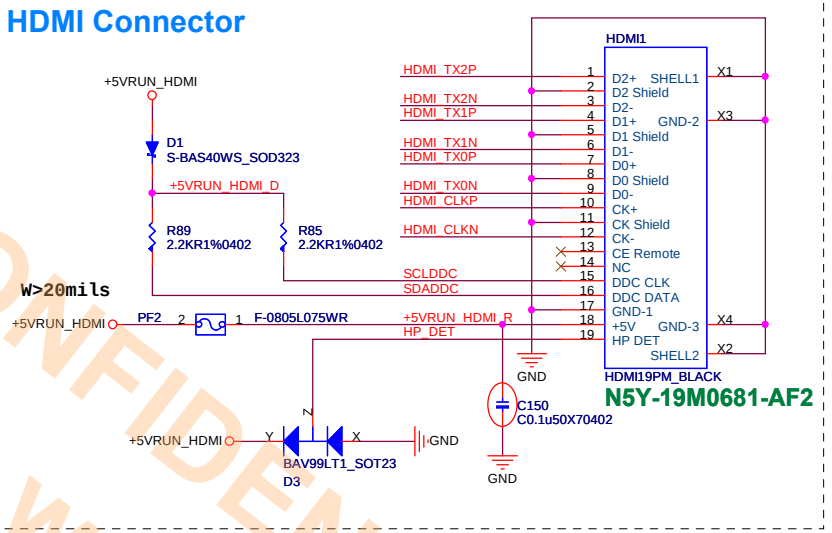
HDMI Repeater



HDMI Connector



An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

HPD_SNK Internal PD 150kohm

DCIN_EN — TPJNC5
DCIN_EN:DC coupling enable (Deleted)
Internal PD at 150kohm
L:Default, AC coupling input
H:DC coupling input

DDCBUF — R364 4.7KR0402 — +3VRUN
Enable active DDC buffer , Internal PD at 150kohm
L:Default, passive DDC pass-through
H:Active DDC buffer with default threshould
M:Active DDC buffer without internal pull up resistor

PRE — R354 X_4.7KR0402 — +3VRUN; R359 X_4.7KR0402 — GND
PRE:output pre-emphasis setting Internal PD at 150kohm
L:No pre-emphasis
H:1.6dB pre-emphasis
M:2.5dB pre-emphasis

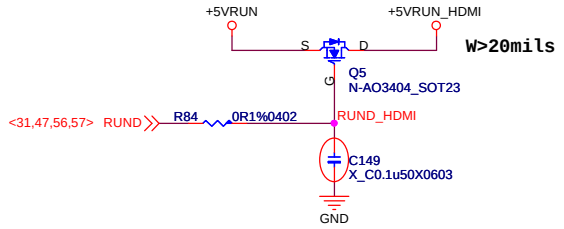
CFG — TPJNC26
Configuation pin (Deleted)
Internal PD at 150kohm
L:HDMI ID disable
H:HDMI ID enable

EQ — R353 X_4.7KR0402 — +3VRUN; R358 X_4.7KR0402 — GND
Receiver equalization setting
Internal PD at 150kohm
L:programmable EQ for channel loss up to 12.4dB
H:programmable EQ for channel loss up to 4.3dB
M:programmable EQ for channel loss up to 48.6dB

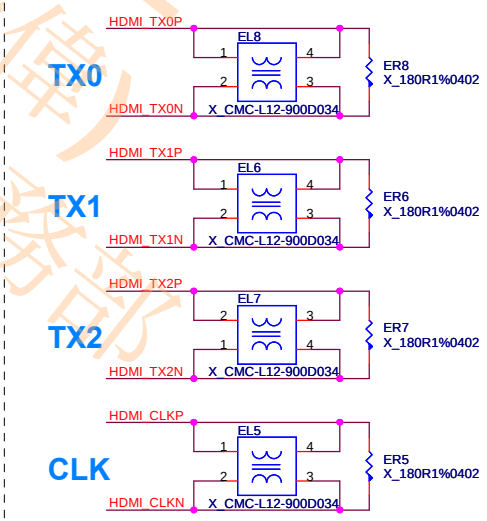
ISET — R372 X_4.7KR0402 — +3VRUN; R371 X_4.7KR0402 — GND
TMDS output swing adjustment
Internal PD at 150kohm
L:Default
H:Increase +13%
M:reduce -13%

ADDR1 (CFG)	ADDR0 (EQ)	I2C control bus address (Internal pull down at ~150kΩ, 3.3V I/O)
0	0	0x4C / 4D (default)
0	1	0x5C / 5D
1	0	0xCC / CD
1	1	0xEC / ED

Avoid HDMI Leakage



EMI Close Connector



MICRO-STAR INT'L CO.,LTD.

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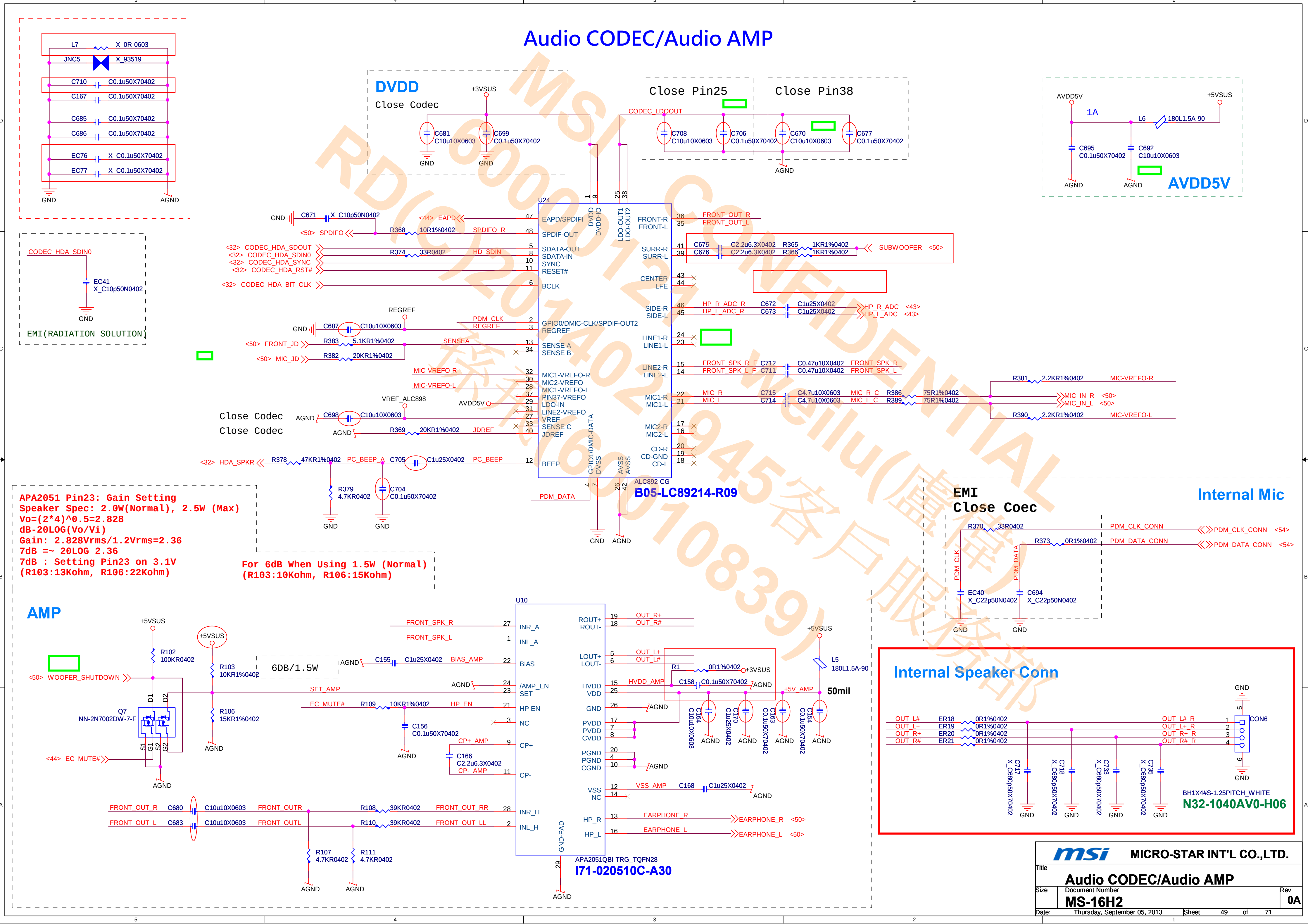
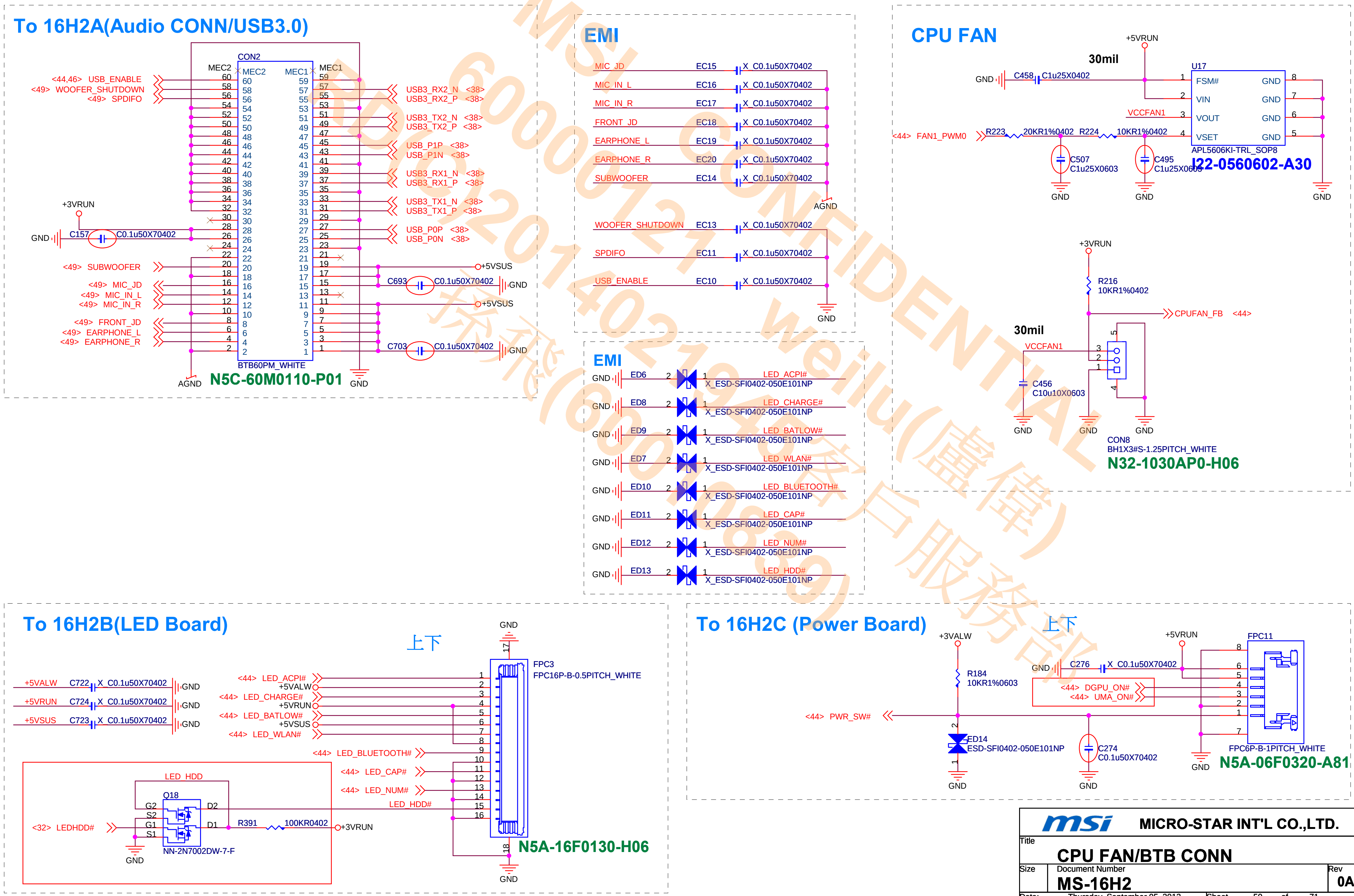
Audio CODEC/Audio AMP



CPU FAN/BTB CONN



MICRO-STAR INT'L CO.,LTD.

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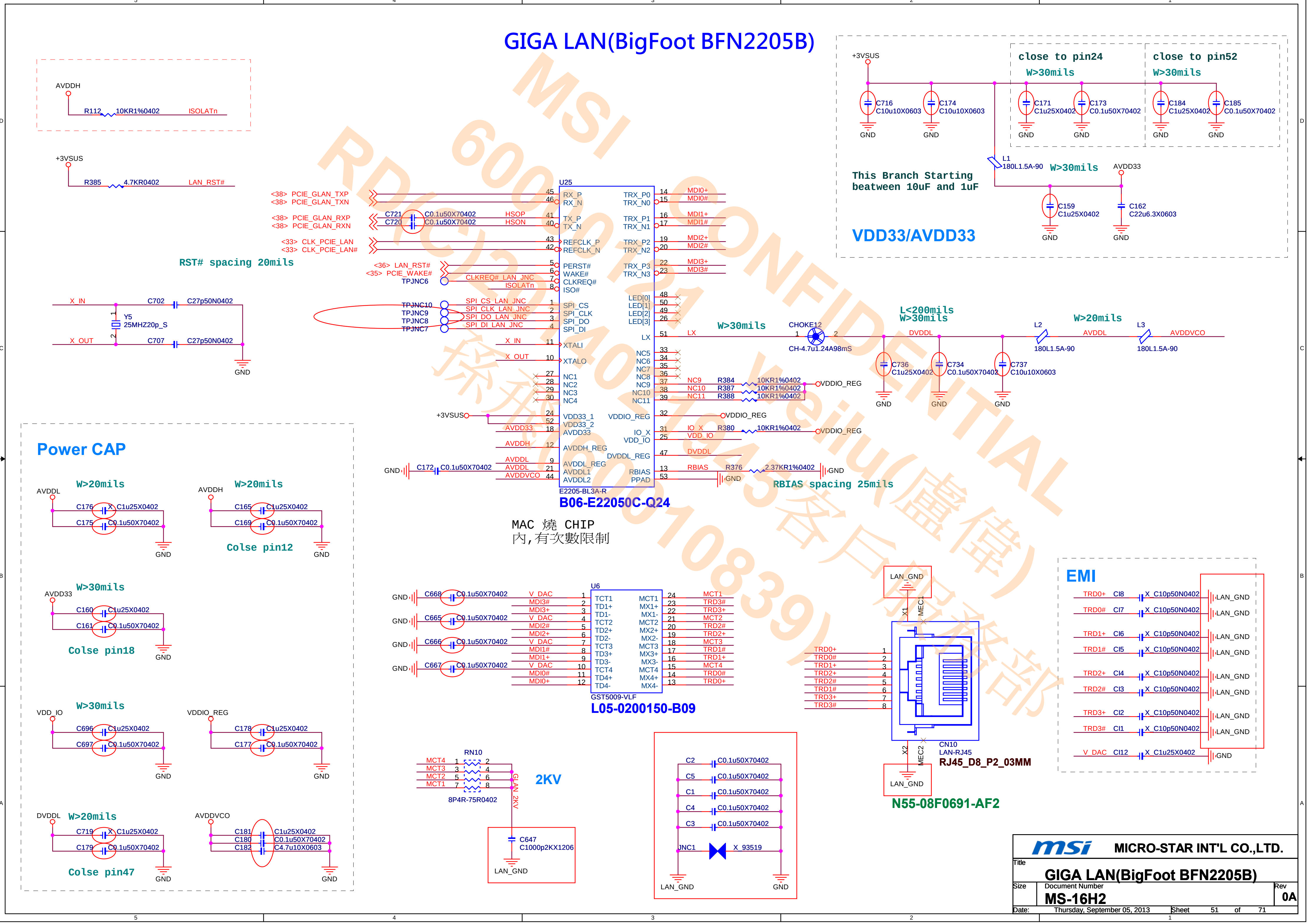

GIGA LAN(BigFoot BFN2205B)
AVDDH
R112 10KR1%0402 ISOLATn
+3VSUS
R385 4.7KR0402 LAN_RST#
RST# spacing 20mils
X_IN
C702 C27p50N0402
Y5 25MHZ20p_S
X_OUT
C707 C27p50N0402
GND
<38> PCIE_GLAN_TXP
<38> PCIE_GLAN_TXN
<38> PCIE_GLAN_RXP
<38> PCIE_GLAN_RXN
C721 C0.1u50X70402 HSOP
C720 C0.1u50X70402 HSON
<33> CLK_PCIE_LAN
<33> CLK_PCIE_LAN#
<36> LAN_RST#
<35> PCIE_WAKE#
TPJNC6
CLKREQ# LAN_JNC
ISOLATn
TPJNC10 SPI_CS_LAN_JNC
TPJNC9 SPI_CLK_LAN_JNC
TPJNC8 SPI_DO_LAN_JNC
TPJNC7 SPI_DI_LAN_JNC
U25
RX_P RX_N TX_P TX_N REFCLK_P REFCLK_N PERST# WAKE# CLKREQ# ISO#
SPI_CS SPI_CLK SPI_DO SPI_DI XTALI XTALO NC1 NC2 NC3 NC4
VDD33_1 VDD33_2 AVDD33 AVDDH_REG AVDDL_REG AVDDL1 AVDDL2
TRX_P0 TRX_N0 TRX_P1 TRX_N1 TRX_P2 TRX_N2 TRX_P3 TRX_N3
LED[0] LED[1] LED[2] LED[3] LX NC5 NC6 NC7 NC8 NC9 NC10 NC11
VDDIO_REG IO_X VDD_IO DVDDL_REG RBIAS PPAD
MDI0+ MDI0# MDI1+ MDI1# MDI2+ MDI2# MDI3+ MDI3#
R384 10KR1%0402
R387 10KR1%0402
R388 10KR1%0402
VDDIO_REG
R380 10KR1%0402
R376 2.37KR1%0402
C172 C0.1u50X70402
E2205-BL3A-R
B06-E22050C-Q24
RBIAS spacing 25mils
MAC 燒 CHIP
內,有次數限制
W>30mils
CHOKE12 CH-4.7u1.24A98mS
L<200mils
W>30mils
DVDDL
L2 180L1.5A-90
W>20mils
AVDDL
L3 180L1.5A-90
AVDDVCO
C736 C1u25X0402
C734 C0.1u50X70402
C737 C10u10X0603
close to pin24
close to pin52
W>30mils
C716 C10u10X0603
C174 C10u10X0603
C171 C1u25X0402
C173 C0.1u50X70402
C184 C1u25X0402
C185 C0.1u50X70402
L1 180L1.5A-90
AVDD33
This Branch Starting
beatween 10uF and 1uF
C159 C1u25X0402
C162 C22u6.3X0603
VDD33/AVDD33
Power CAP
AVDDL W>20mils
C176 C1u25X0402
C175 C0.1u50X70402
AVDDH W>20mils
C165 C1u25X0402
C169 C0.1u50X70402
Colse pin12
AVDD33 W>30mils
C160 C1u25X0402
C161 C0.1u50X70402
Colse pin18
VDD_IO W>30mils
C696 C1u25X0402
C697 C0.1u50X70402
VDDIO_REG
C178 C1u25X0402
C177 C0.1u50X70402
DVDDL W>20mils
C719 C1u25X0402
C179 C0.1u50X70402
Colse pin47
AVDDVCO
C181 C1u25X0402
C180 C0.1u50X70402
C182 C4.7u10X0603
U6
C668 C0.1u50X70402
C665 C0.1u50X70402
C666 C0.1u50X70402
C667 C0.1u50X70402
TCT1 TD1+ TD1- TCT2 TD2+ TD2- TCT3 TD3+ TD3- TCT4 TD4+ TD4-
MCT1 MX1+ MX1- MCT2 MX2+ MX2- MCT3 MX3+ MX3- MCT4 MX4+ MX4-
GST5009-VLF
L05-0200150-B09
RN10 8P4R-75R0402
2KV
C647 C1000p2KX1206
LAN_GND
C2 C0.1u50X70402
C5 C0.1u50X70402
C1 C0.1u50X70402
C4 C0.1u50X70402
C3 C0.1u50X70402
JNC1 X_93519
CN10
LAN-RJ45
RJ45_D8_P2_03MM
N55-08F0691-AF2
EMI
CI8 X_C10p50N0402
CI7 X_C10p50N0402
CI6 X_C10p50N0402
CI5 X_C10p50N0402
CI4 X_C10p50N0402
CI3 X_C10p50N0402
CI2 X_C10p50N0402
CI1 X_C10p50N0402
V_DAC CI12 X_C1u25X0402
MICRO-STAR INT'L CO.,LTD.
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GIGA LAN(BigFoot BFN2205B)
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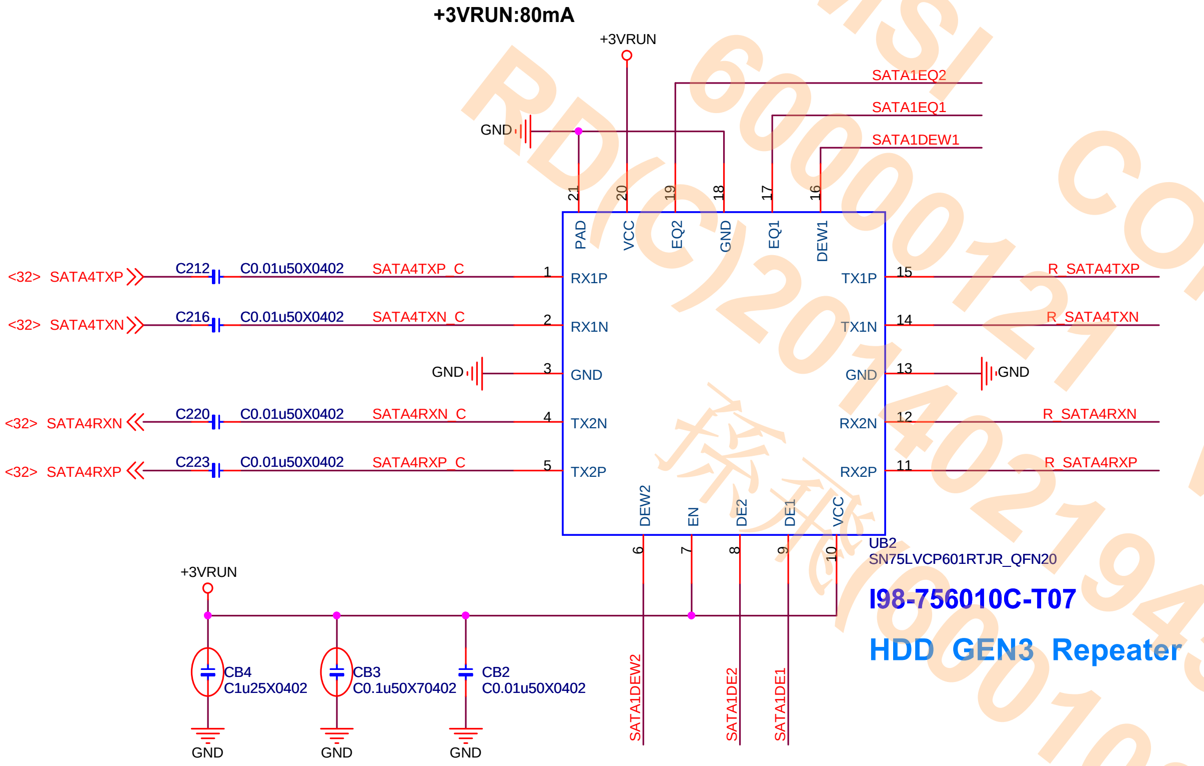
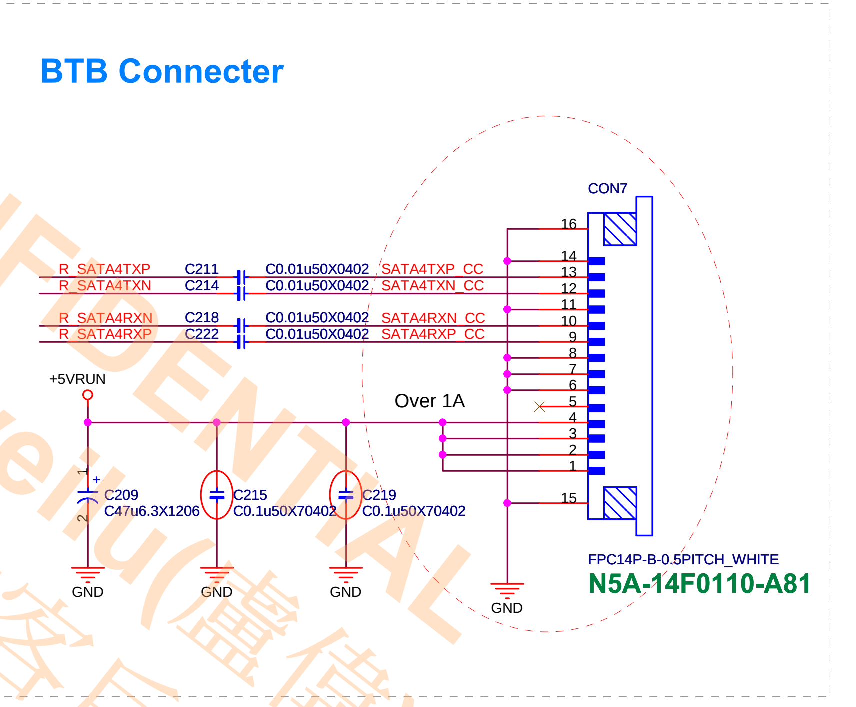
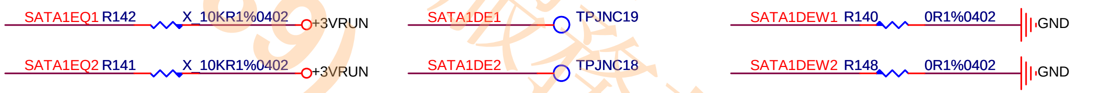
HDD (With Repeater)







TI SN75LVCP601RTJR HW Setting

DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	EQ1/EQ2	CH1/CH2Equalization dB (at 6Gbps)
NC (***default***)	–4	NC (***default***)	0
0	0	0	7
1	–2	1	14

DEW1/DEW2	Device Function → DE Width for CH1/CH2
0	De-emphasis pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps)
1 (***default***)	De-emphasis pulse duration, long (recommended setting when link operates at SATA 1.5/3 Gbps speed only)

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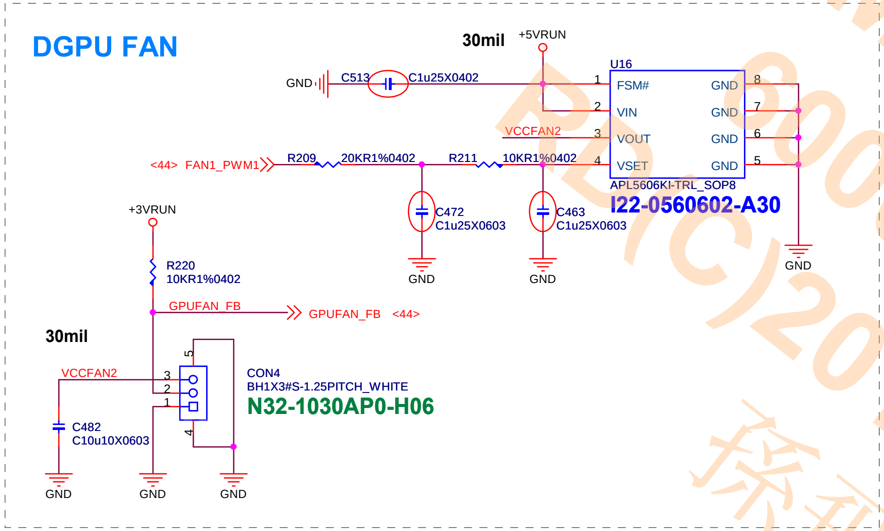
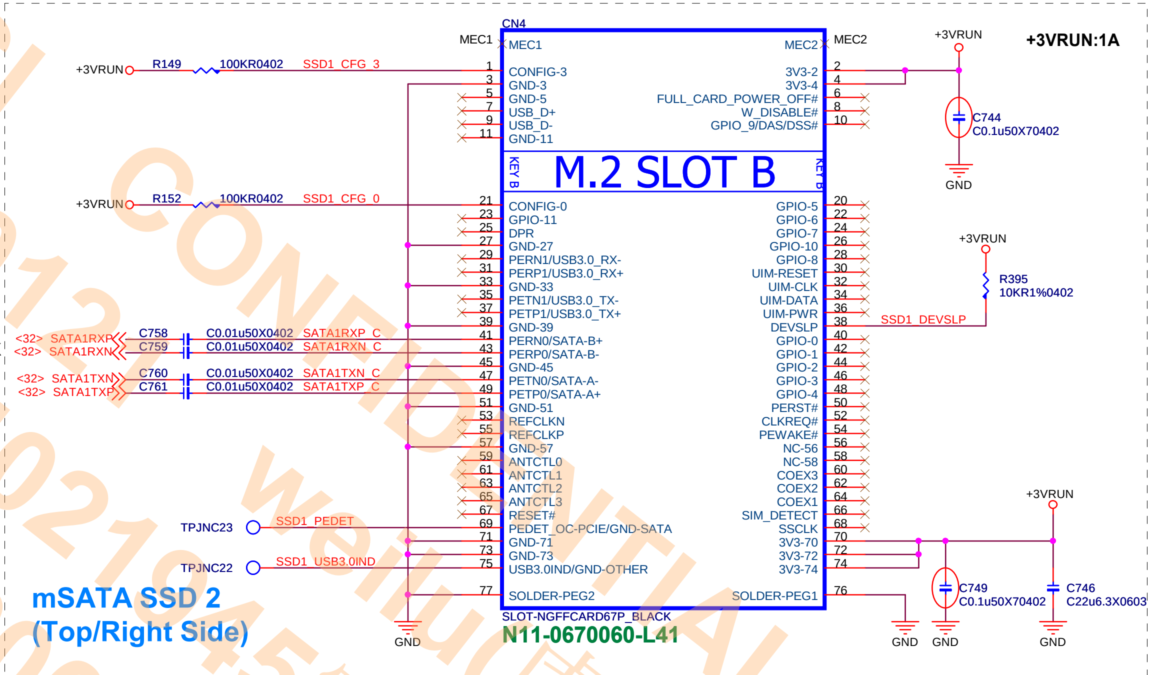
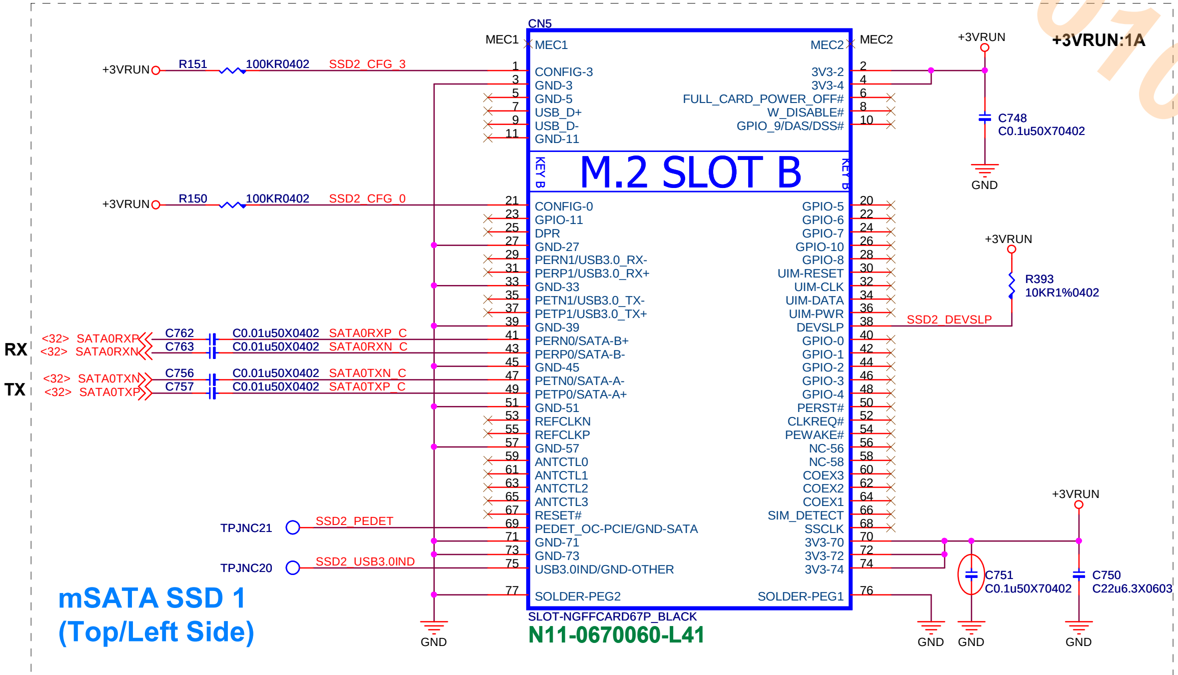
SSD/ DGPU FAN







40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host transmitter differential signal pair

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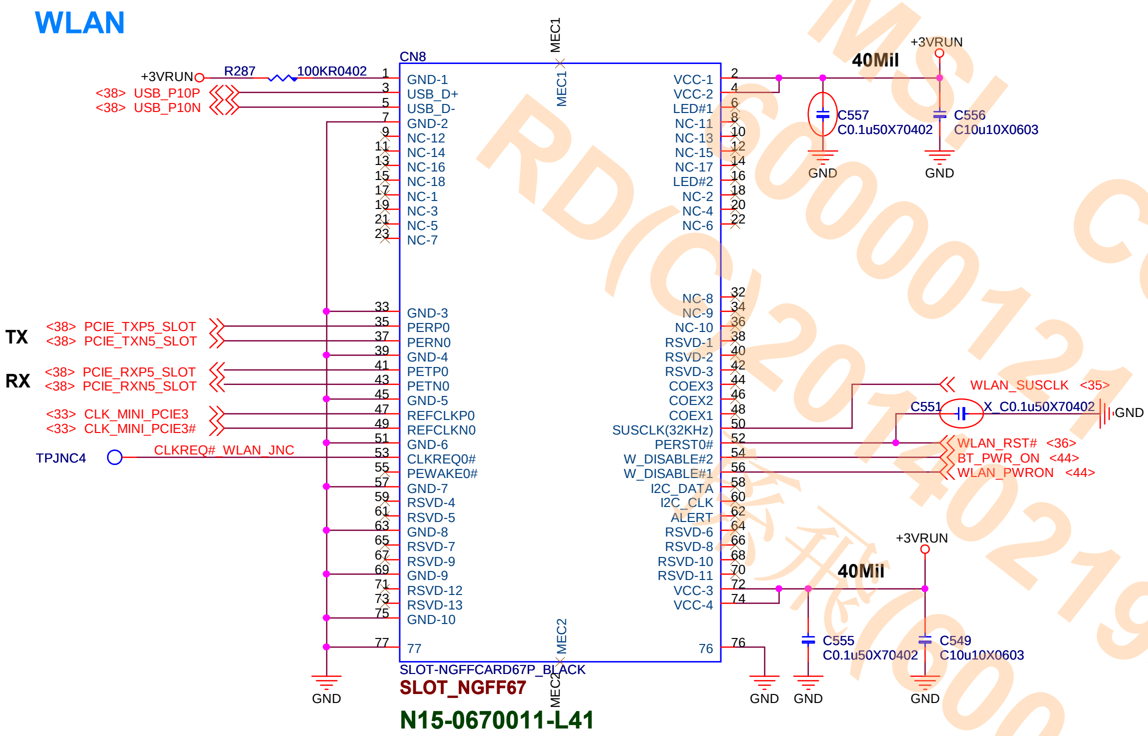
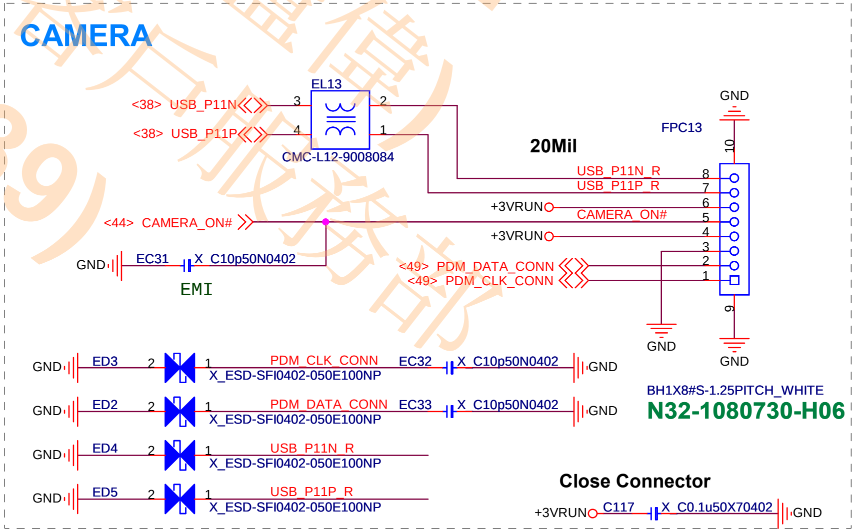
WLAN /Camera/ClickPad

WLAN

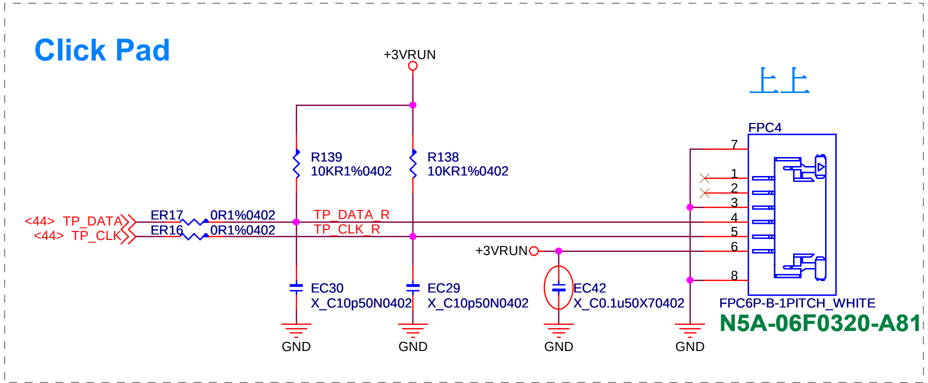


Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

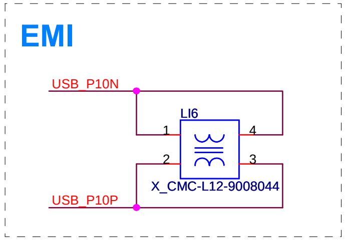
CAMERA



Click Pad



EMI



MICRO-STAR INT'L CO.,LTD.

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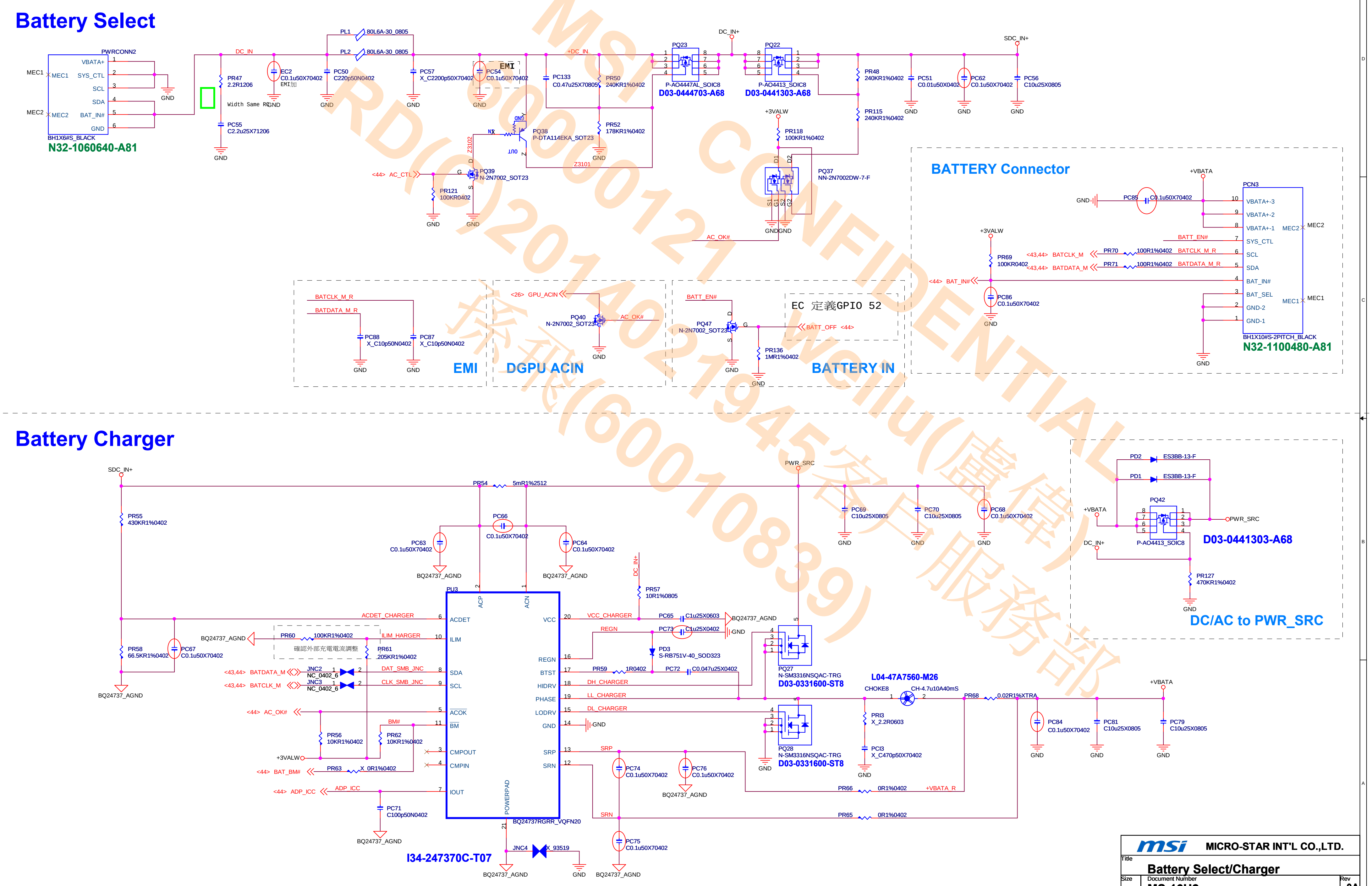
Battery Select/Charger



msi	MICRO-STAR INT'L CO.,LTD.
Title	Battery Select/Charger
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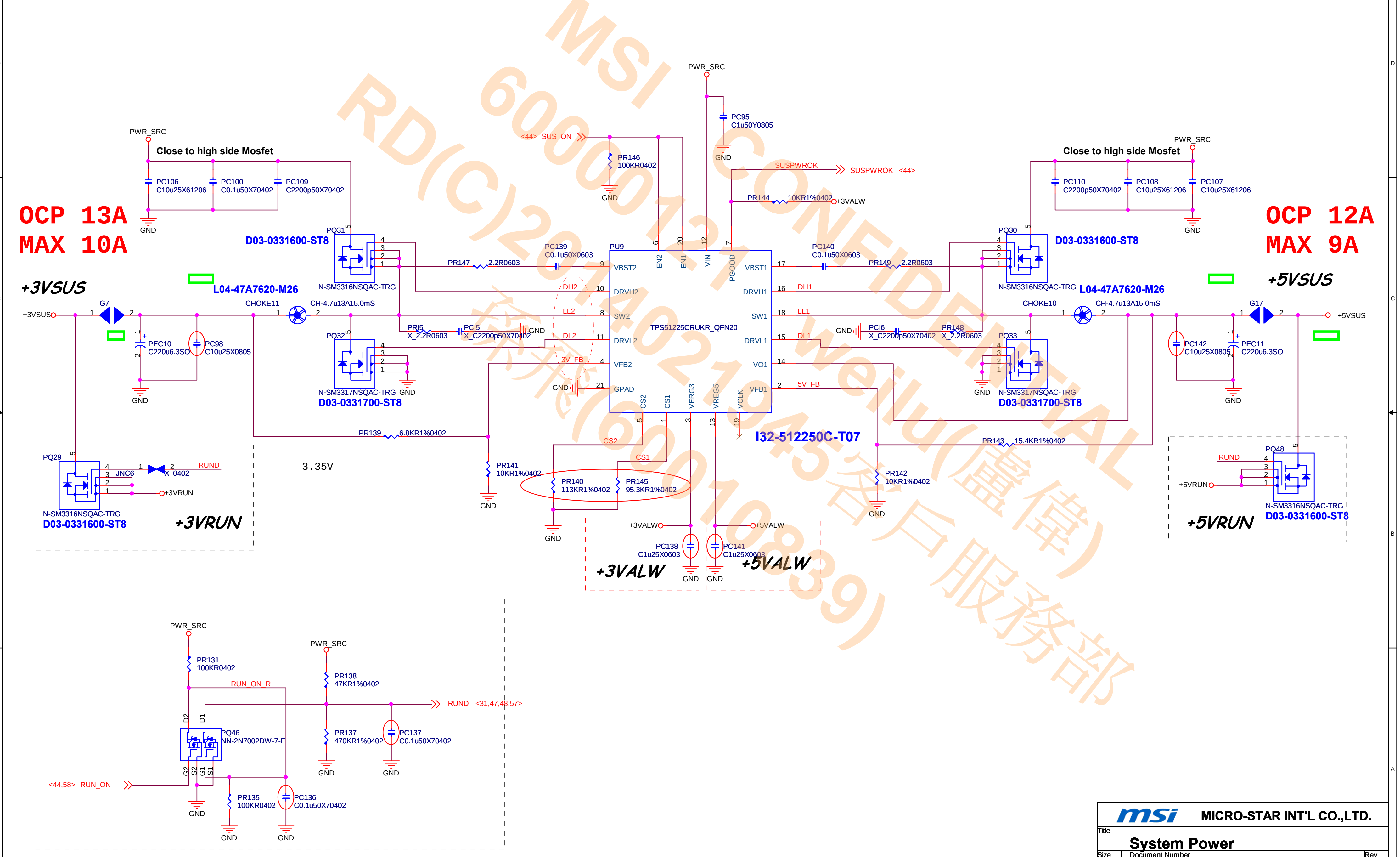
System Power



MICRO-STAR INT'L CO.,LTD.

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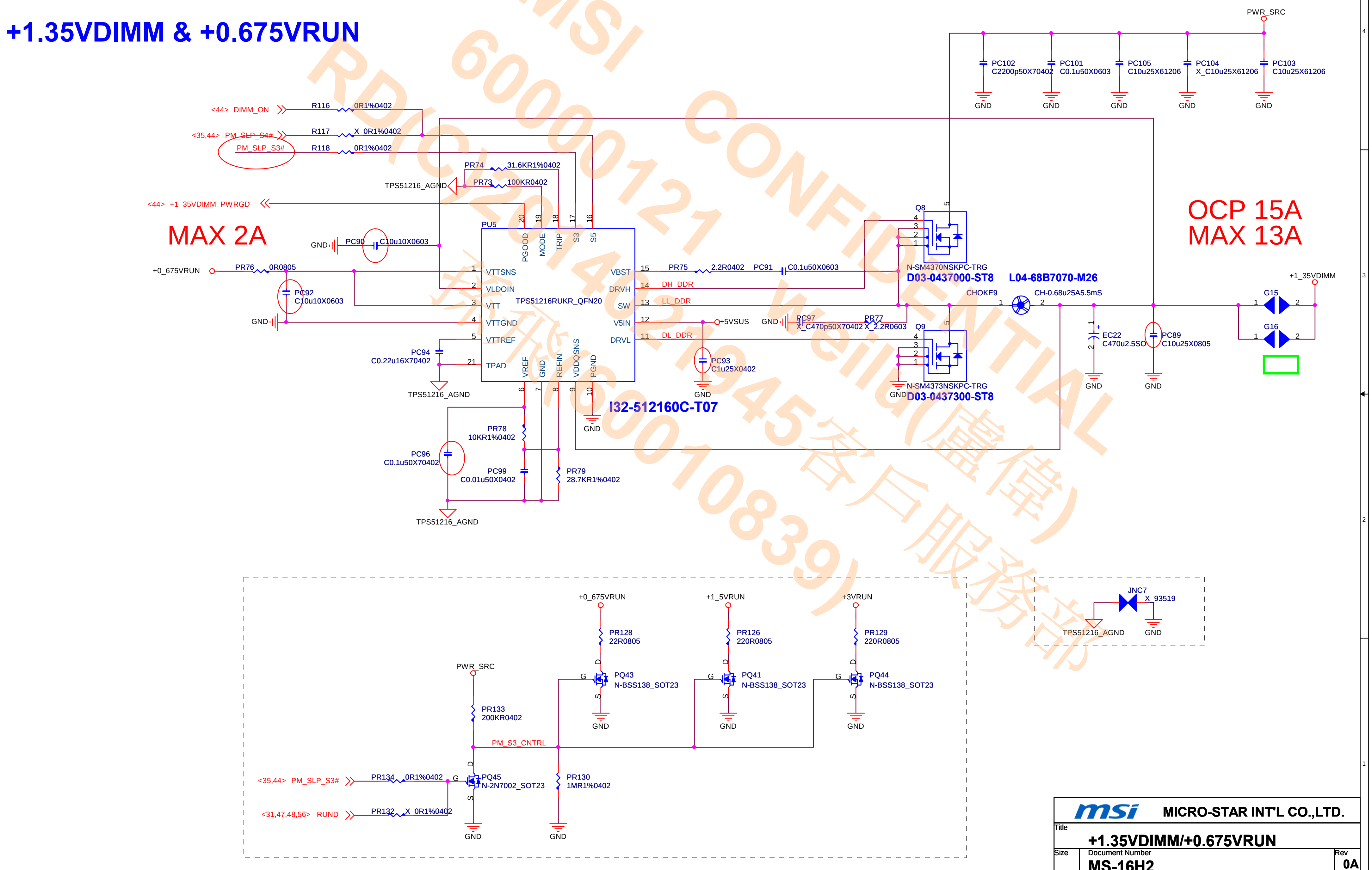
+1.35VDIMM/+0.675VRUN



MICRO-STAR INT'L CO.,LTD.

Title: +1.35VDIMM/+0.675VRUN

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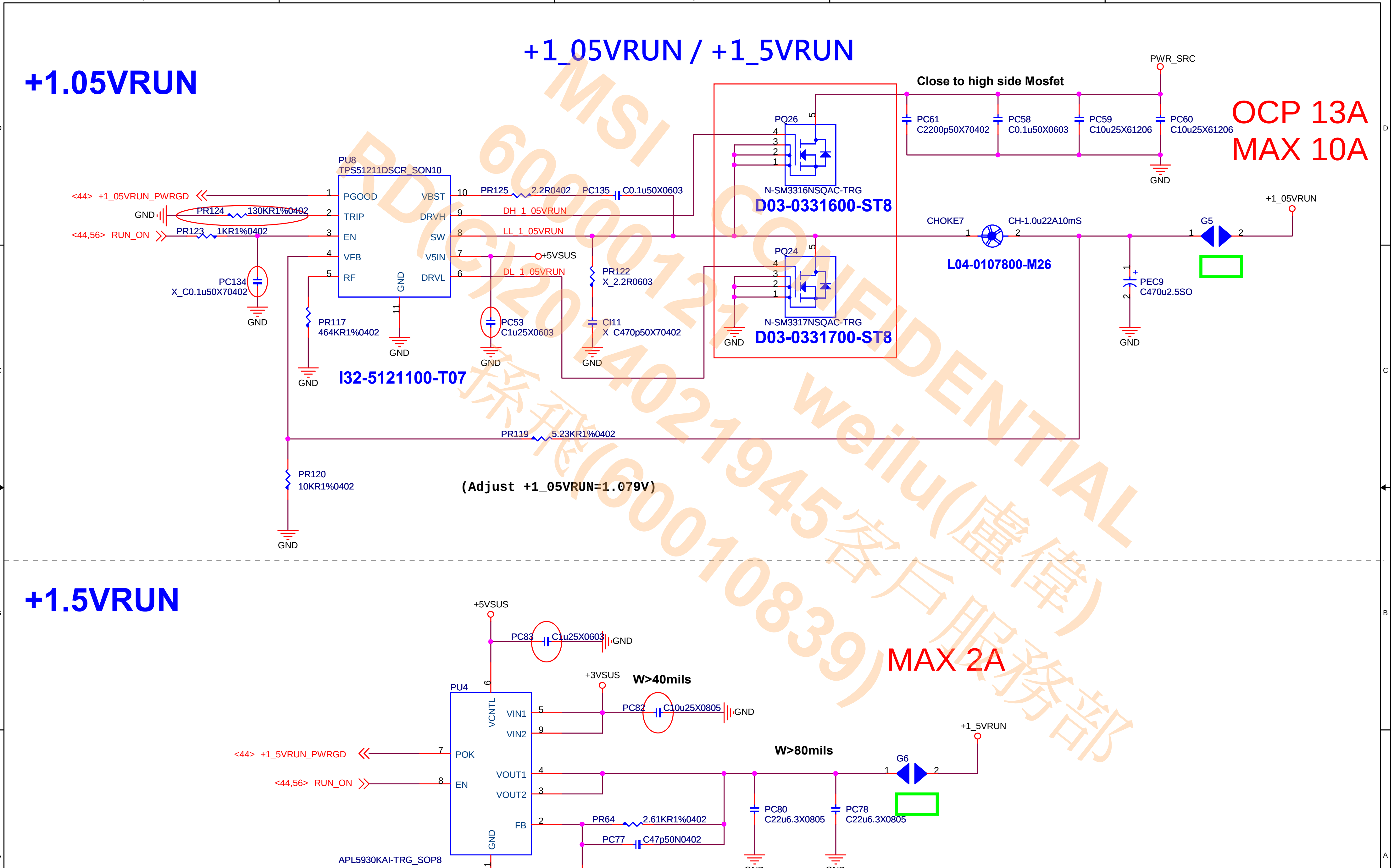

MICRO-STAR INT'L CO.,LTD.

Title	+1_05VRUN / +1_5VRUN	
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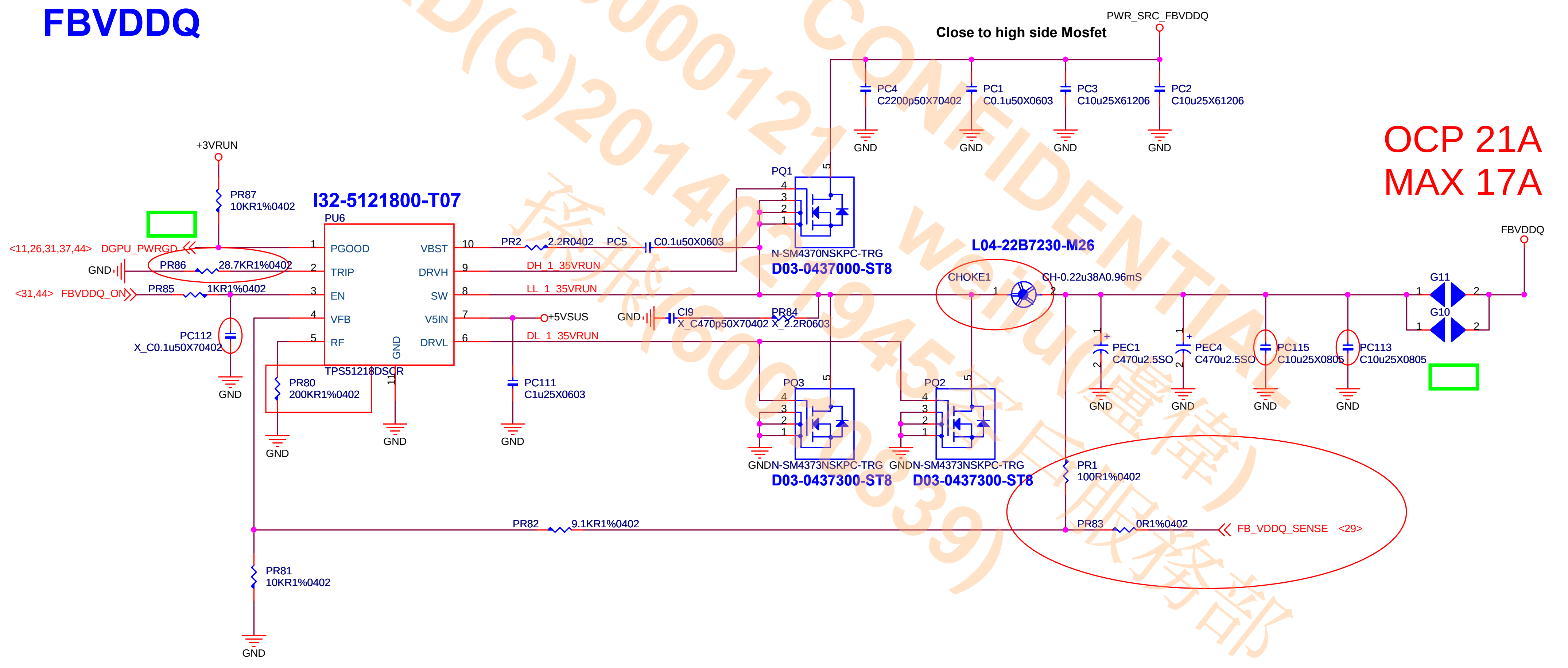
DGPU POWER FBVDDQ



MICRO-STAR INT'L CO.,LTD.

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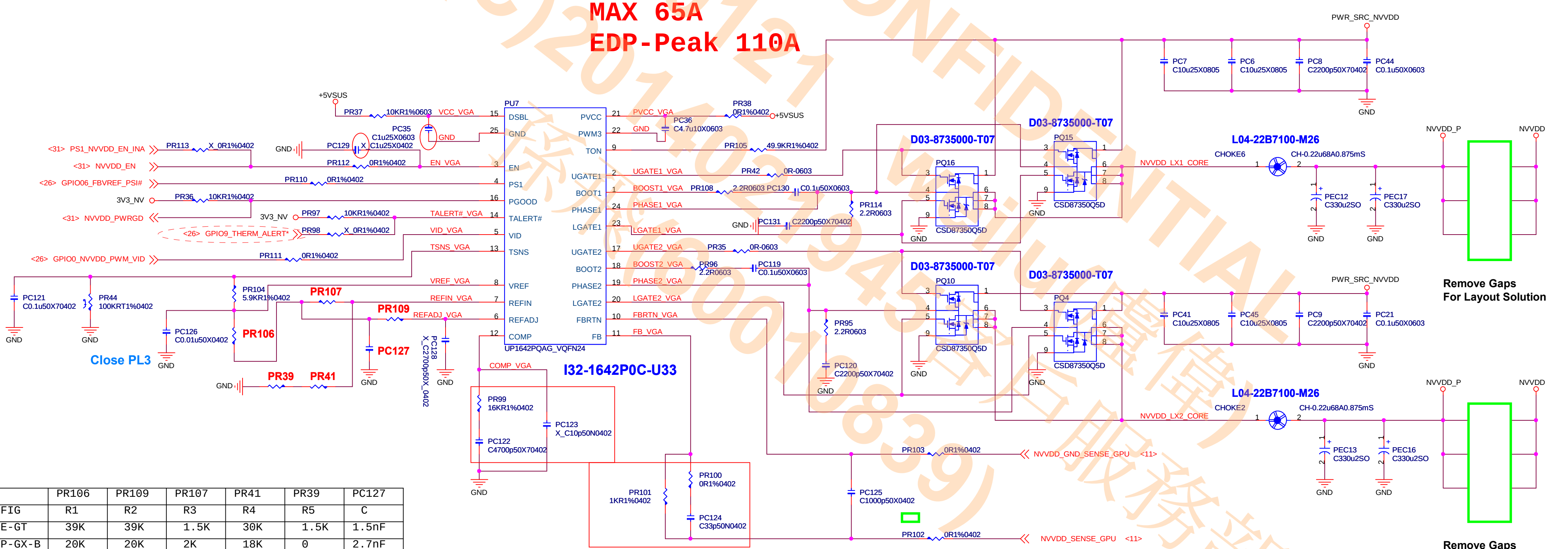
DGPU POWER NVVDD

DGPU POWER / UP1642PQAG

CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

MAX 65A
EDP-Peak 110A



	PR106	PR109	PR107	PR41	PR39	PC127
CONFIG	R1	R2	R3	R4	R5	C
N15E-GT	39K	39K	1.5K	30K	1.5K	1.5nF
N15P-GX-B	20K	20K	2K	18K	0	2.7nF

N15E-GT

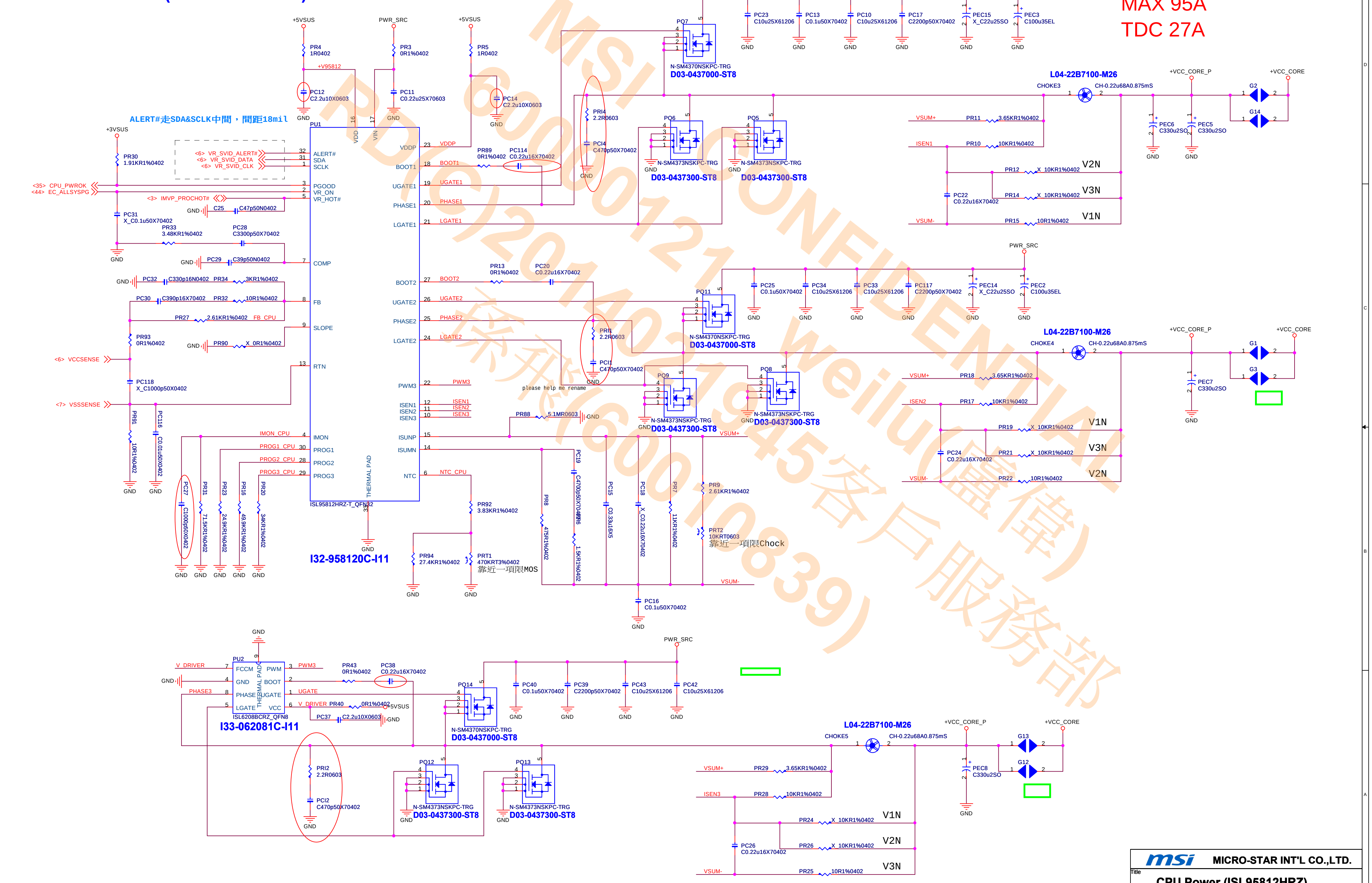
DGPU_GT_R1	DGPU_GT_R2	DGPU_GT_R3	DGPU_GT_R4	DGPU_GT_R5	DGPU_GT_C1
5020	5020	5020	5020	5010	5020
R11-0393T12-W08	R11-0393T12-W08	R11-0152T12-W08	R11-0303T12-W08	R11-0152T12-W08	C11-1522812-W08
X_39KR1%0402	X_39KR1%0402	X_1.5KR1%0402	X_30KR1%0402	X_1.5KR1%0402	X_C1500p50X0402

N15P-GX-B 5020

DGPU_GX_R1	DGPU_GX_R2	DGPU_GX_R3	DGPU_GX_R4	DGPU_GX_R5	DGPU_GX_C1
5020	5020	5020	5020	5010	5020
R11-0203T12-W08	R11-0203T12-W08	R11-0202T12-W08	R11-0183T12-W08	R11-0000T12-Y01	C11-2722812-W08
X_20KR1%0402	X_20KR1%0402	X_2KR1%0402	X_18KR1%0402	X_0R1%0402	X_C2700p50X_0402

CPU Core Power(ISL95812HRZ)

CPU Power (+VCC_CORE)



msi	**MICRO-STAR INT'L CO.,LTD.**
Title	CPU Power (ISL95812HRZ)
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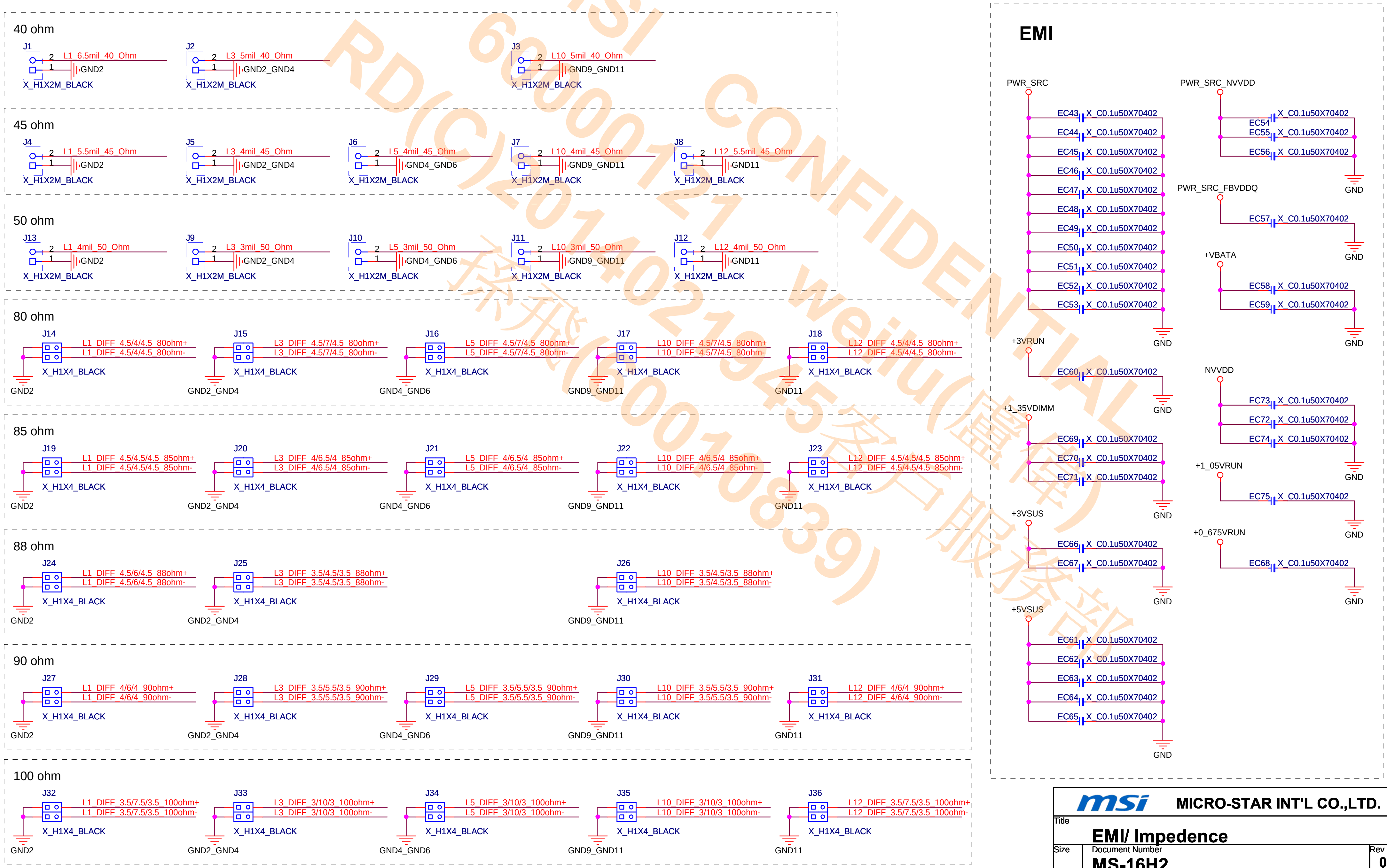
EMI/ Impedence

Impedence Connector No PN



MICRO-STAR INT'L CO.,LTD.

Title	EMI/ Impedence
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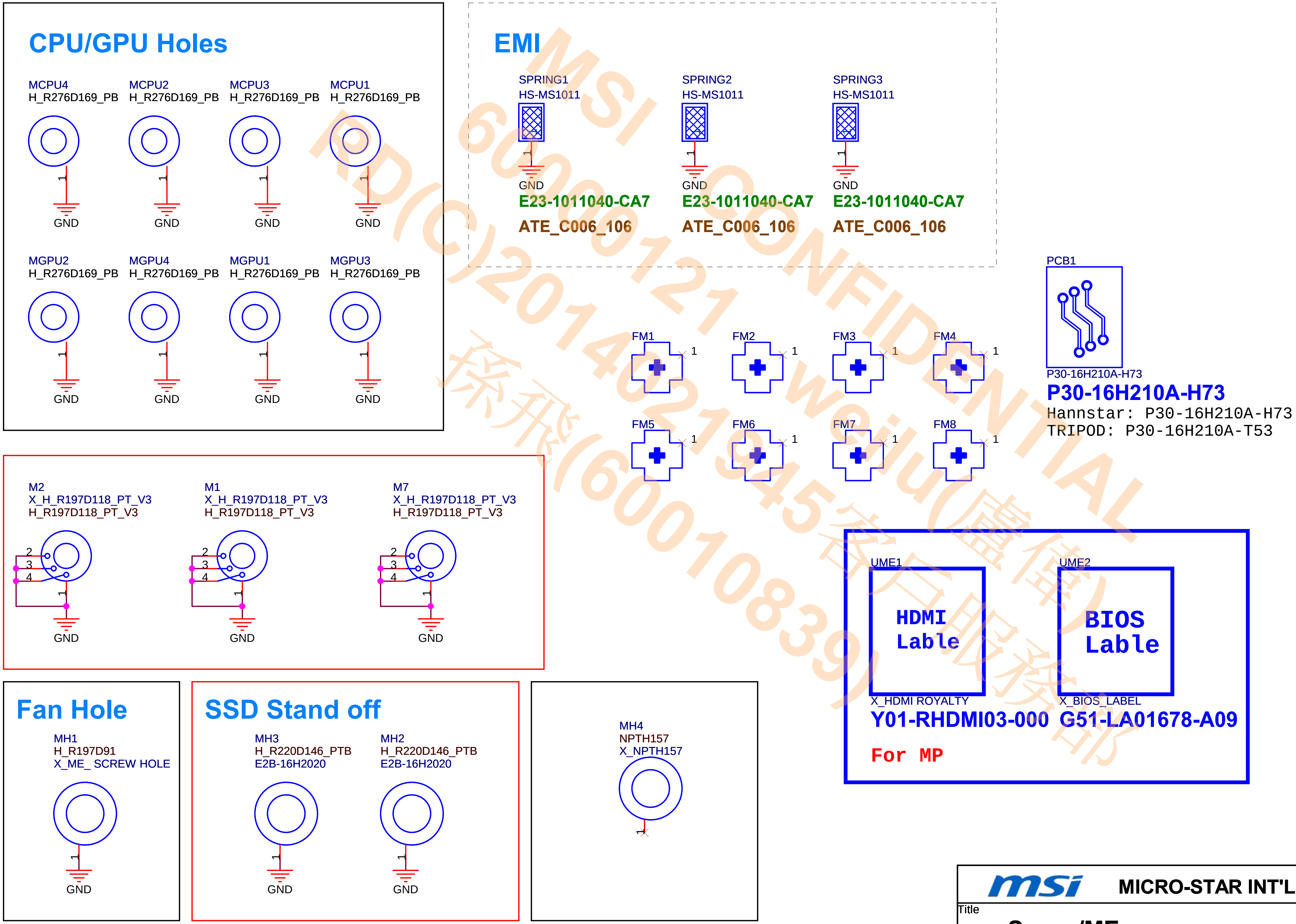

MICRO-STAR INT'L CO.,LTD.

Title: **Screw/ME**

Size | Document Number: **MS-16H2** | Rev: **0A**

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