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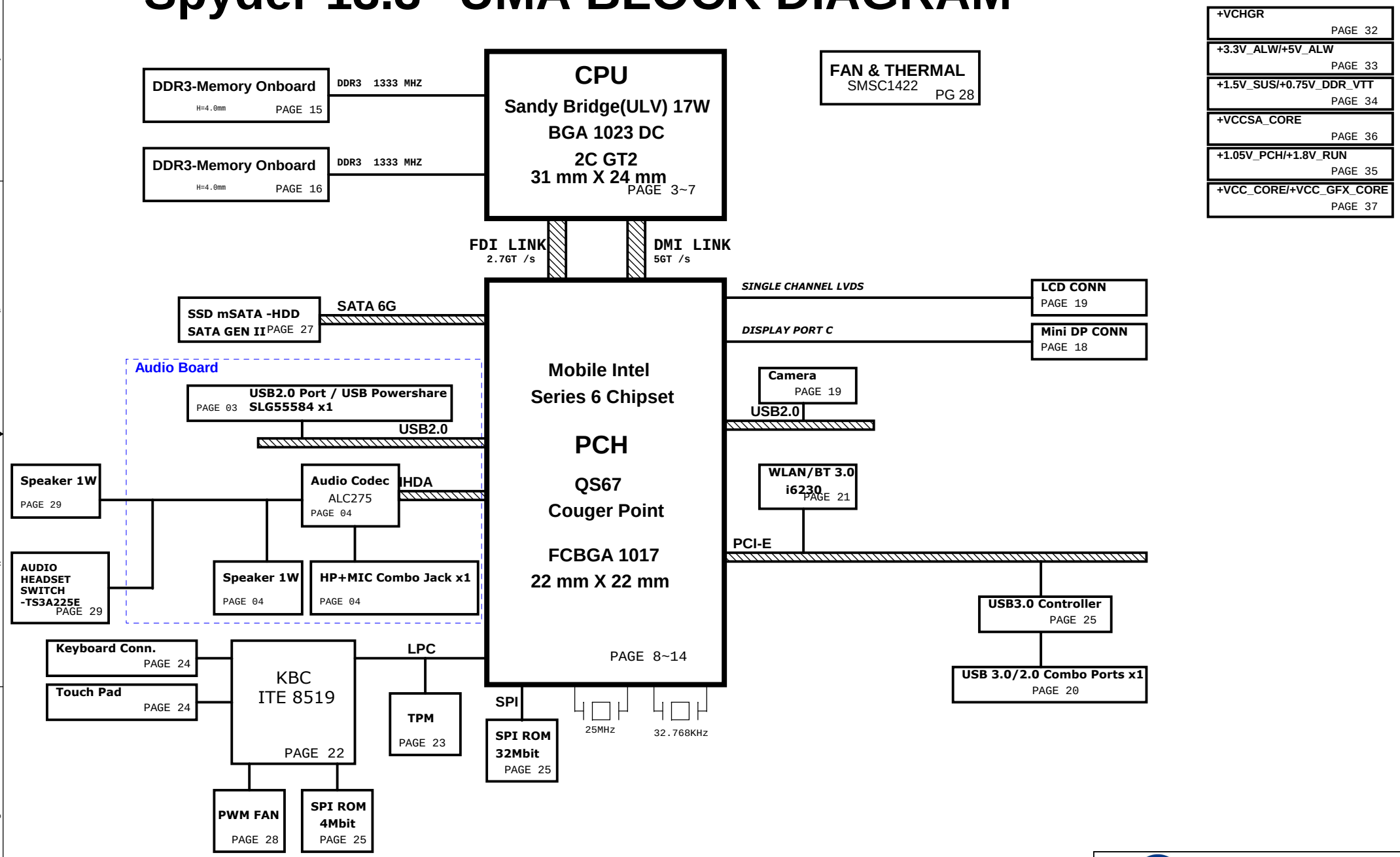
# Spyder 13.3" UMA BLOCK DIAGRAM

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| | BLOCK DIAGRAM | 1A |

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| power / State | SLP_S3# | SLP_S4# | SLP_S5# | ALW_ON | +3.3V_ALW | +5V_ALW | SUS_ON | +3.3V_SUS | +5V_SUS | RUN_ON | +3.3V_RUN | +5V_RUN | AOAC flag | USB2.0 Power share USB_BAK_EN# |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S0 | H | H | H | H | H | H | H | H | H | H | H | H | L | L |
| S3 | L | H | H | H | H | H | H | H | H | L | L | L | L | L |
| S4/S5 AC | L | L | L | H | H | H | L | L | L | L | L | L | L | L |
| S4/S5 DC Only | L | L | L | L | L | L | L | L | L | L | L | L | L | L |
| AC/DC No Exist | L | L | L | L | L | L | L | L | L | L | L | L | L | L |
| AOAC(S4) | L | L | L | H | H | H | H | H | H | L | L | L | H | H |

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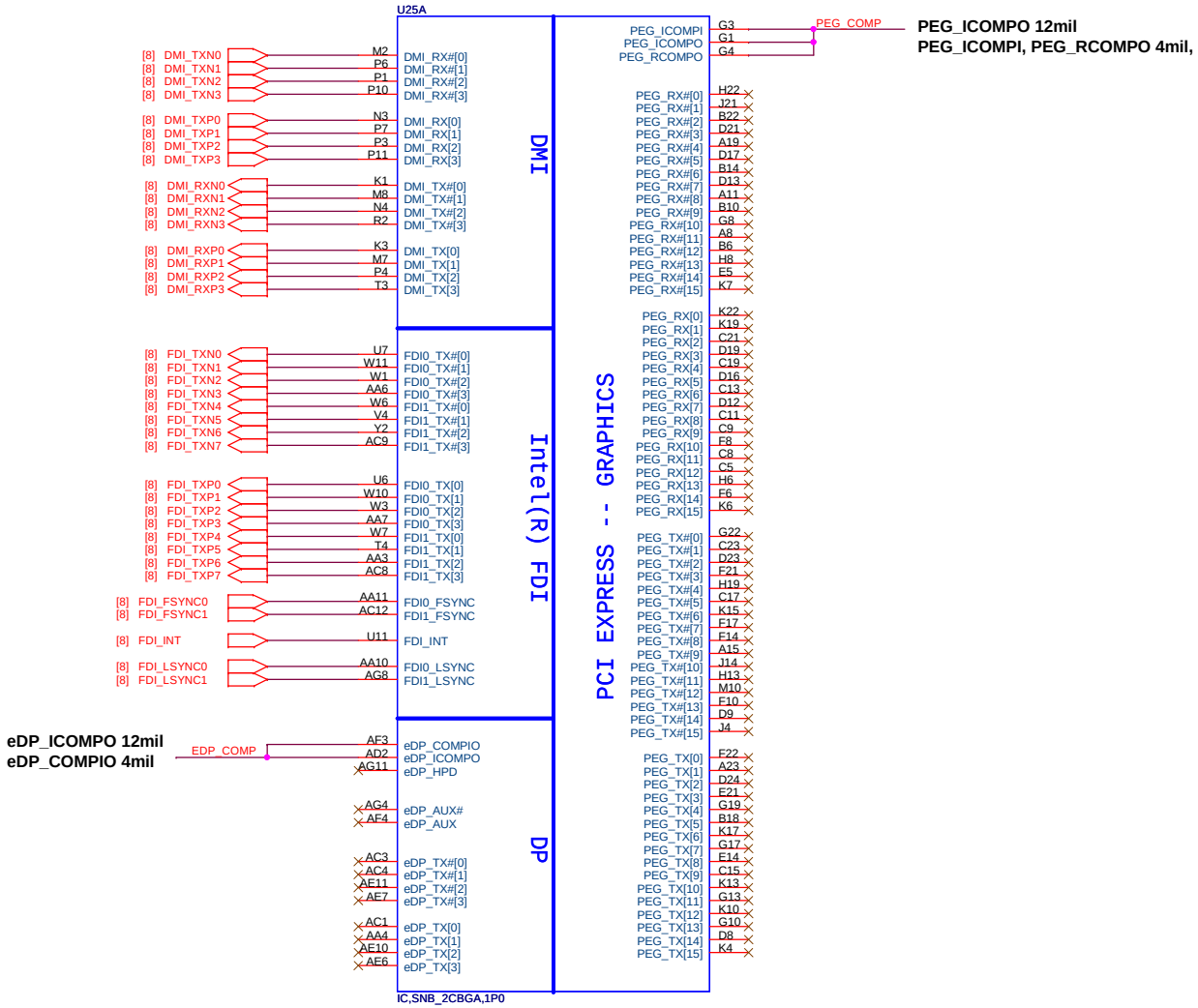
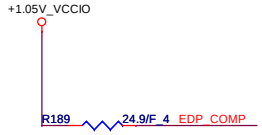
# Sandy Bridge Processor (DMI,PEG,FDI)

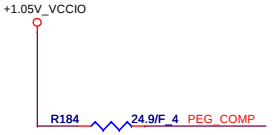
CPU is i7 in schematic




## DP & PEG Compensation




eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms




PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

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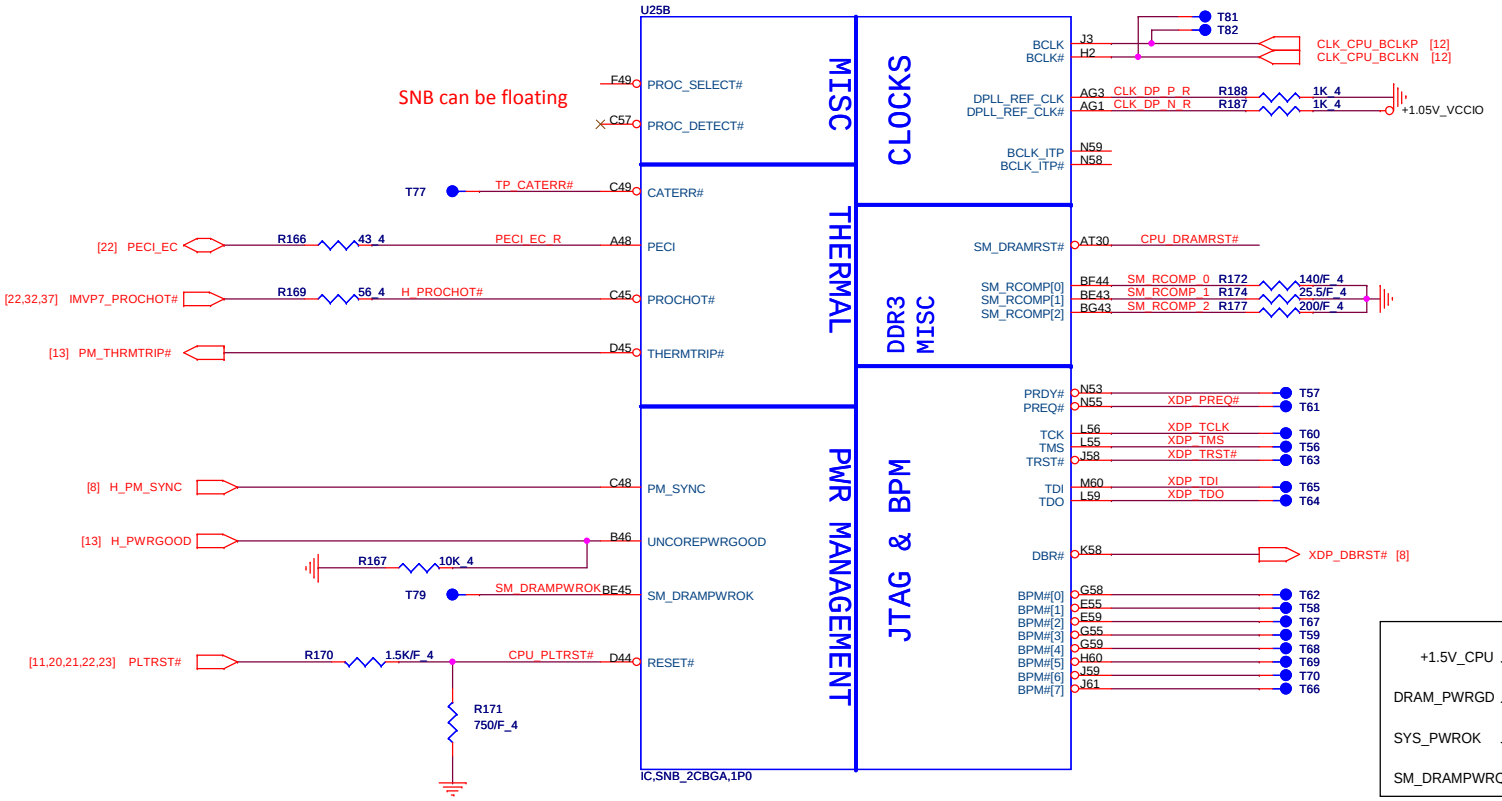
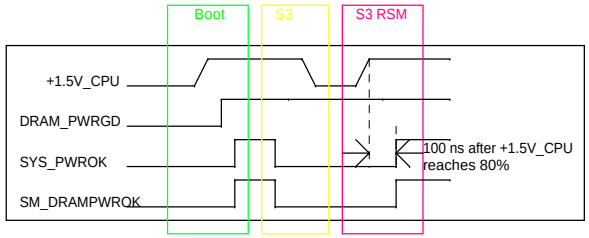
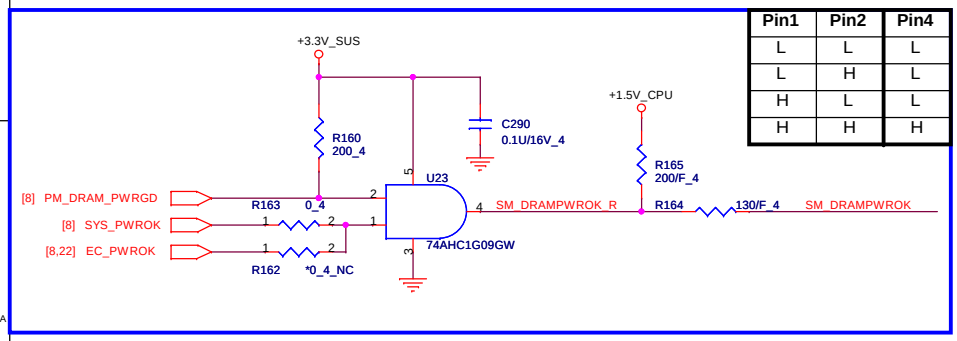
# Sandy Bridge Processor (CLK,MISC,JTAG)

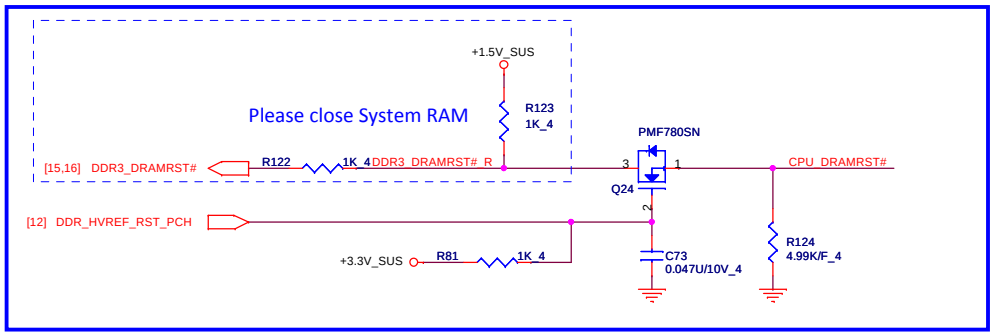
CPU is i7 in schematic




| Pin1 | Pin2 | Pin4 |
|---|---|---|
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |




| | | | |
|---|---|---|---|
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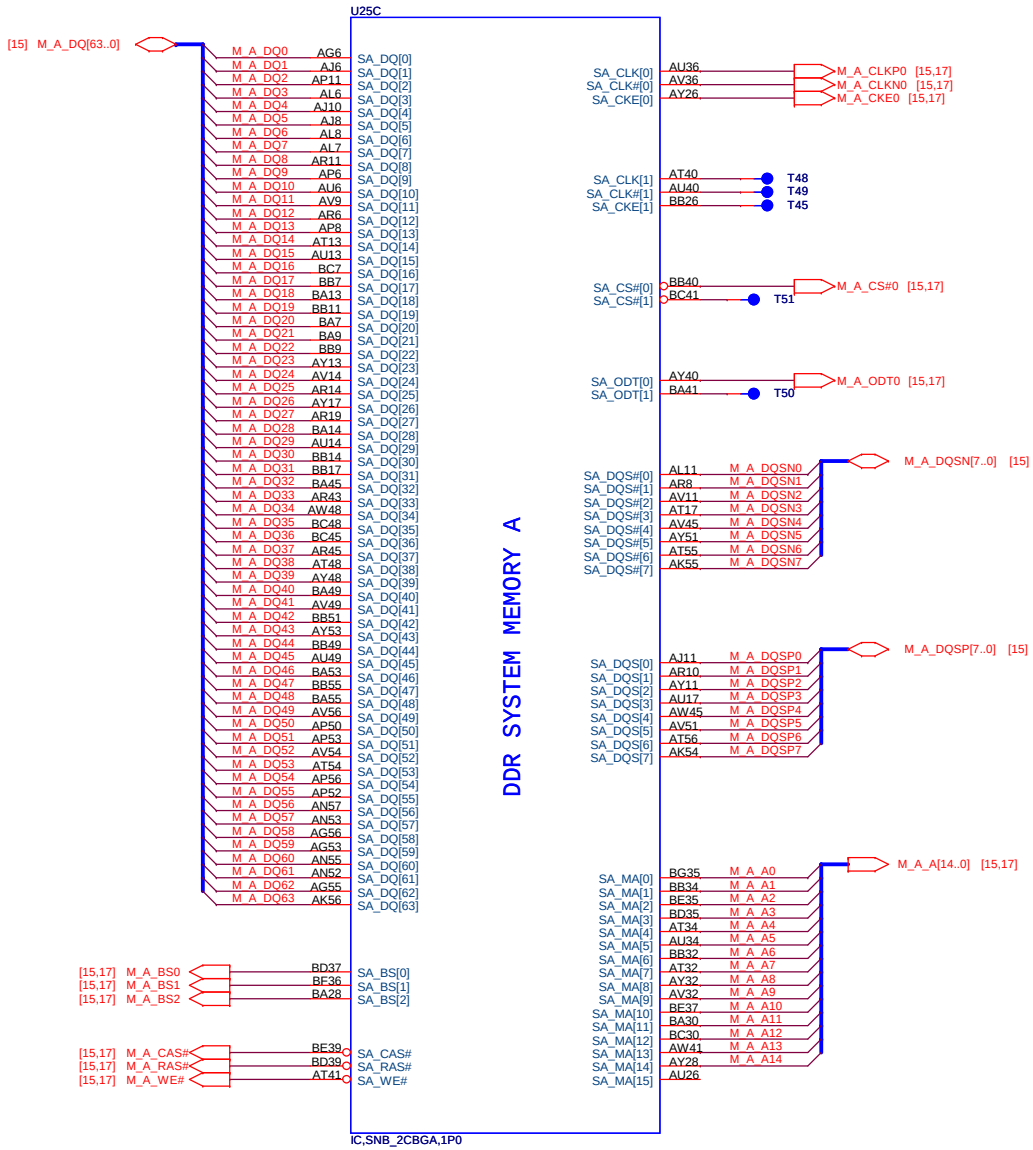
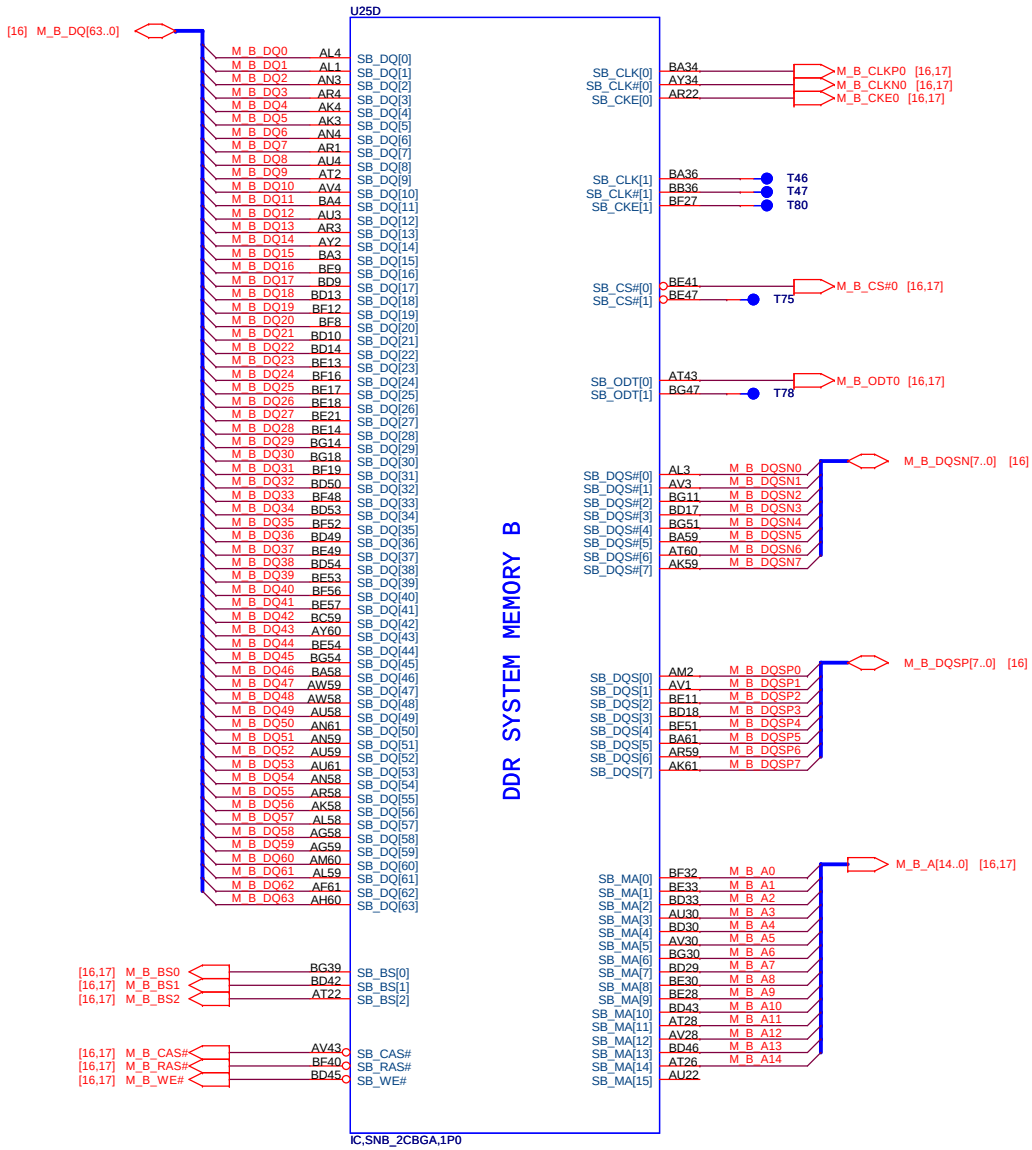
# Sandy Bridge Processor (DDR3)

CPU is i7 in schematic




CPU is i7 in schematic

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# Sandy Bridge Processor (POWER)

CPU is i7 in schematic

U25F

SNB:33A

+VCC_CORE

CORE SUPPLY

POWER

PEG AND DDR

8.5A

+1.05V_VCCIO

QUIET RAILS

SVID

SENSE LINES

Follow check list of Intel

IC,SNB_2CBGA,1P0

# Sandy Bridge Processor (GRAPHIC POWER)

CPU is i7 in schematic

U25G

18A

+VCC_GFX_CORE

POWER

GRAPHICS

DDR3 - 1.5V RAILS

10mil

SM_VREF

+VDDR_REF_CPU

SNB:5A

+1.5V_CPU

5A

+1.5V_SUS

Q26
AON7410

check with power Andy

[8] PS_S3CNTRL_S

C241
*4700P/25V/X7R_4_NC

Follow check list of Intel

[37] VCC_AXG_SENSE
[37] VSS_AXG_SENSE

SENSE LINES

1.8V RAIL

QUIET RAILS

3A

+1.8V_RUN

SNB:6A

+VCCSA_CORE

SA RAIL

SENSE LINES

08/11
For CPU cost down plan
C151, C150

IC,SNB_2CBGA,1P0

Sandy Bridge only:
VCCSA_VID[0] should be pull down
VCCSA_VID[1] should connect to SA VR

Follow check list of Intel

+1.5V_SUS

+1.5V_CPU

SVID DATA

Place resistor R55 close to CPU

R173
130/F_4

SVID ALERT

Place resistor R175 close to CPU

R175
75_4

VR_SVID_DATA

VR_SVID_ALERT#

VR_SVID_ALERT# [37]

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|---|---|---|
| | Sandy Bridge 4/5 | 1A |
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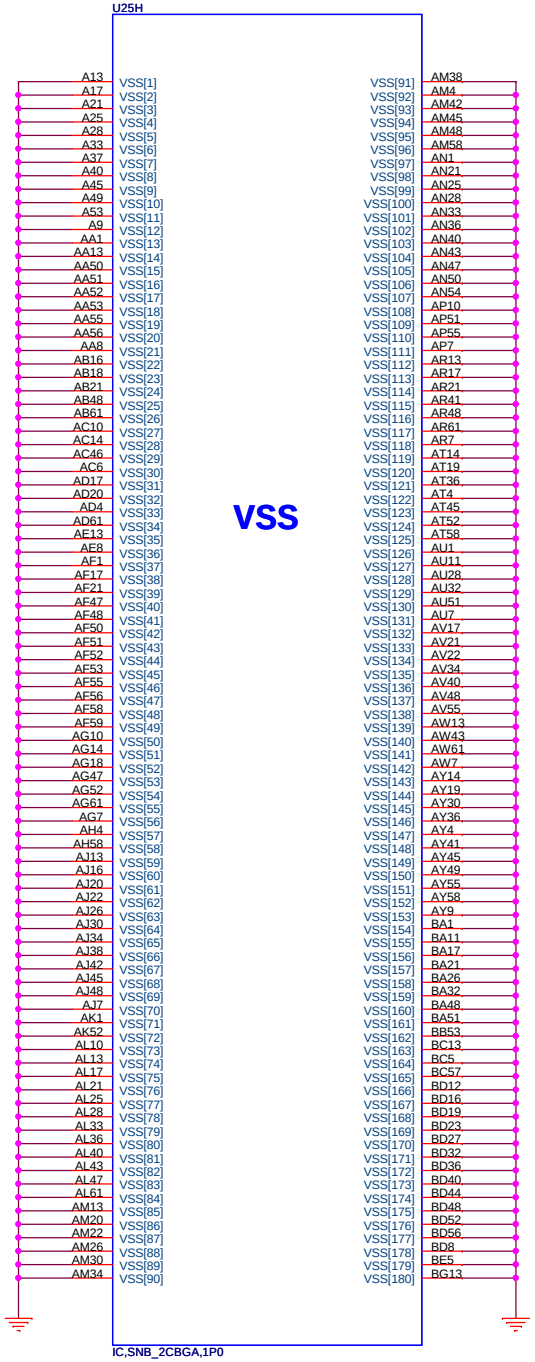
# Sandy Bridge Processor (GND)

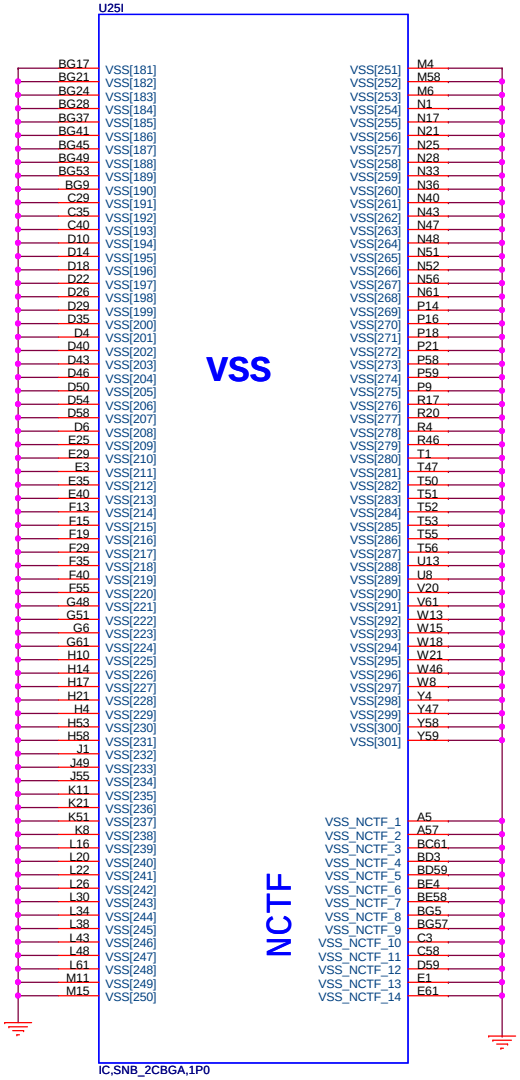
CPU is i7 in schematic

U25H




CPU is i7 in schematic

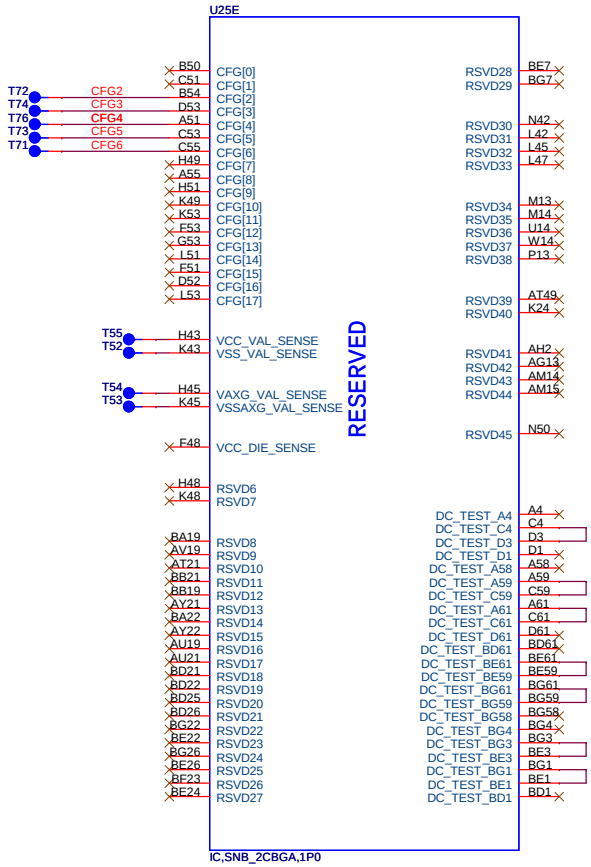
U25I




# Sandy Bridge Processor (RESERVED, CFG)

CPU is i7 in schematic

U25E




PGB straping pin unused for UMA only

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

## Processor Strapping

| | 1 | 0 |
|---|---|---|
| CFG2<br>(PCI-E Static x16 Lane Reversal) | Normal Operation | Lane Reversed |
| CFG3<br>(PCI-E Static x4 Lane Reversal) | Normal Operation | Lane Reversed |
| CFG4<br>(DP Presence Stra) | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP |

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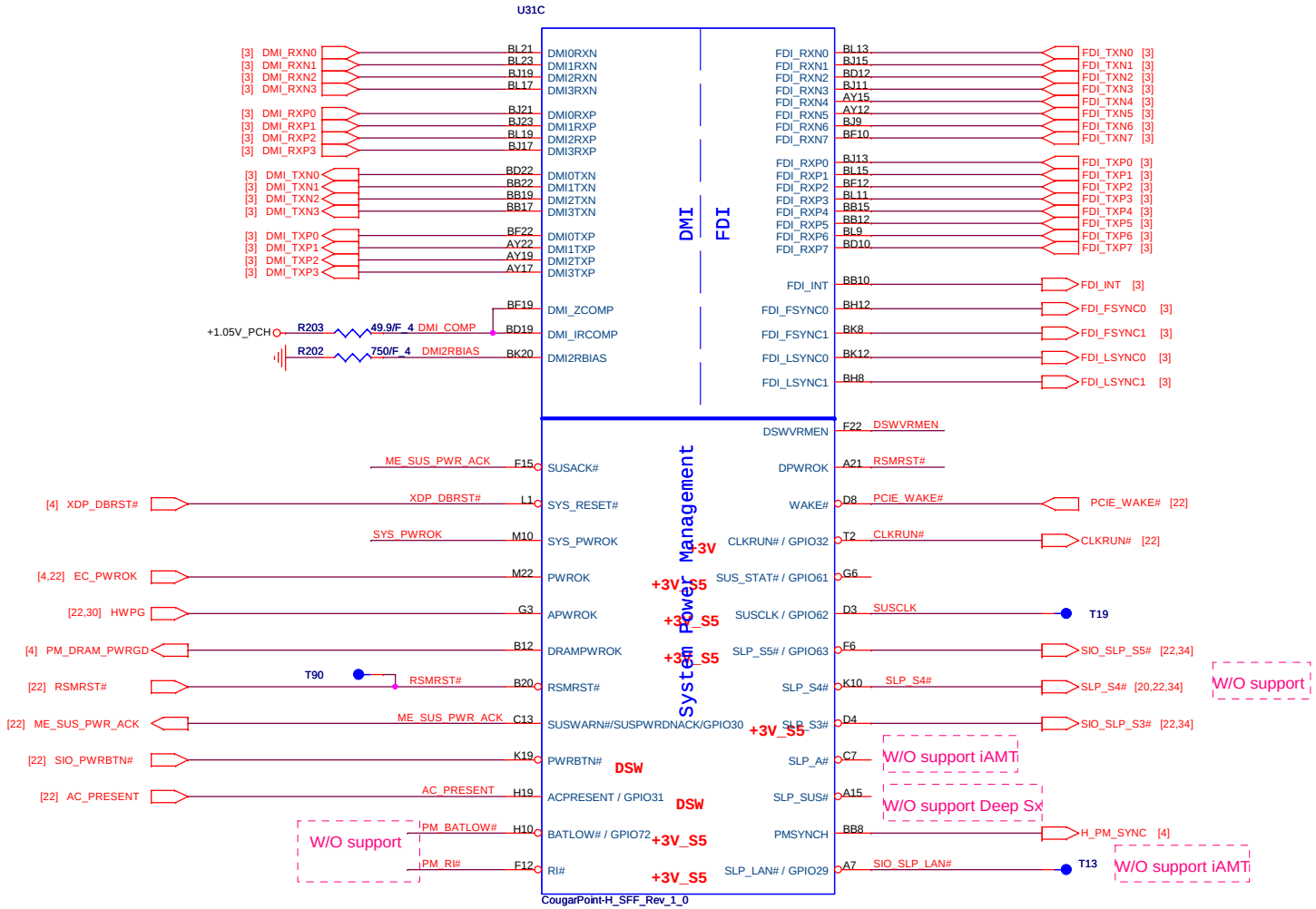
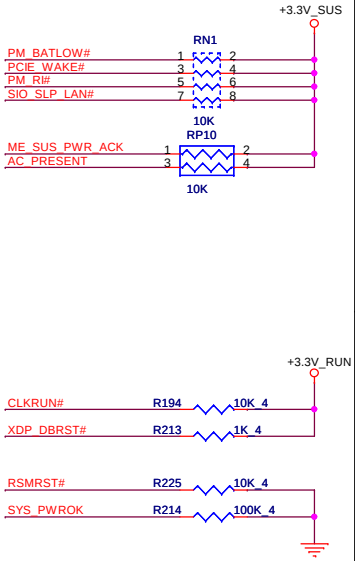
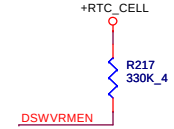
# Cougar Point (DMI,FDI,PM)



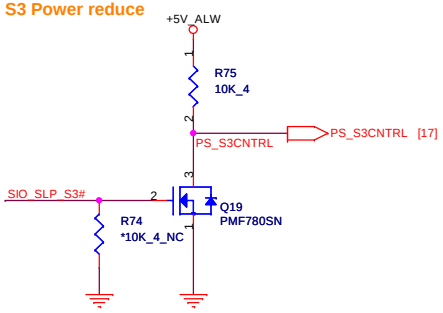

## PCH Pull-high/low(CLG)



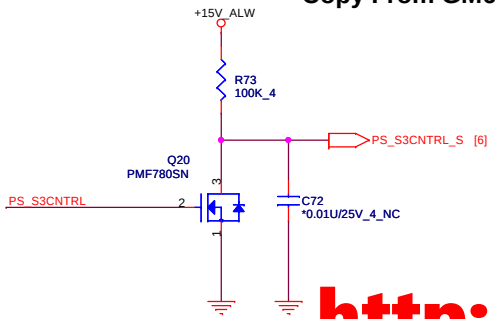

| On Die DSW VR Enable |
|---|
| High = Enable (Default) |
| Low = Disable |

## S3 Power reduce

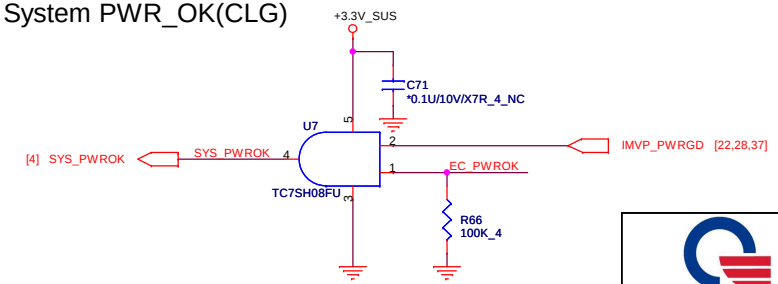



## S3 Power reduce

## Copy From GM6




## System PWR_OK(CLG)

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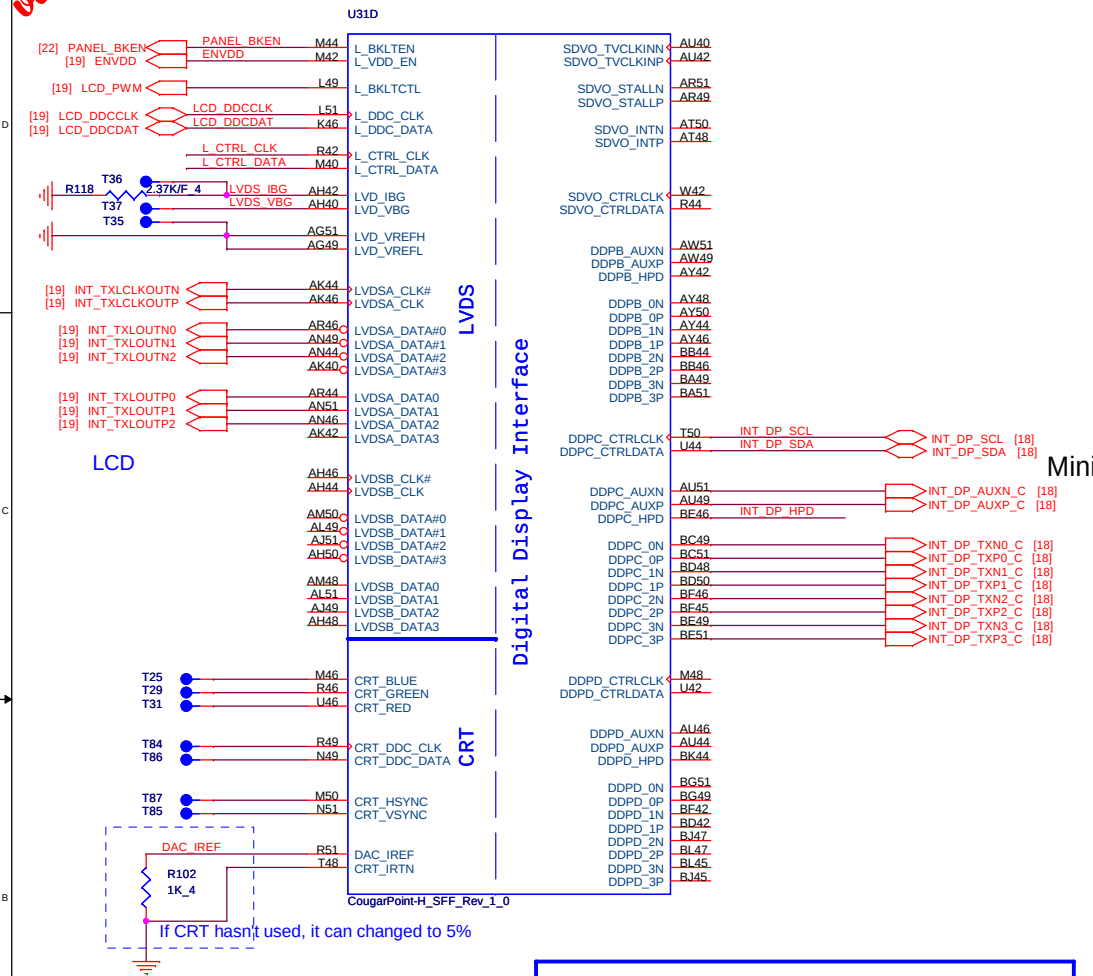
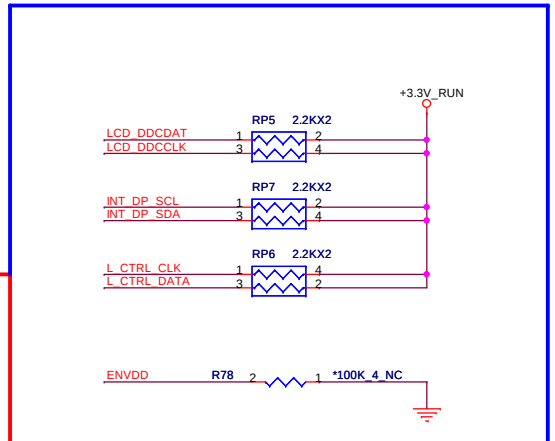
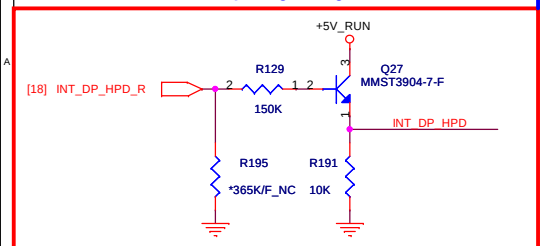
# Cougar Point (LVDS,DDI)

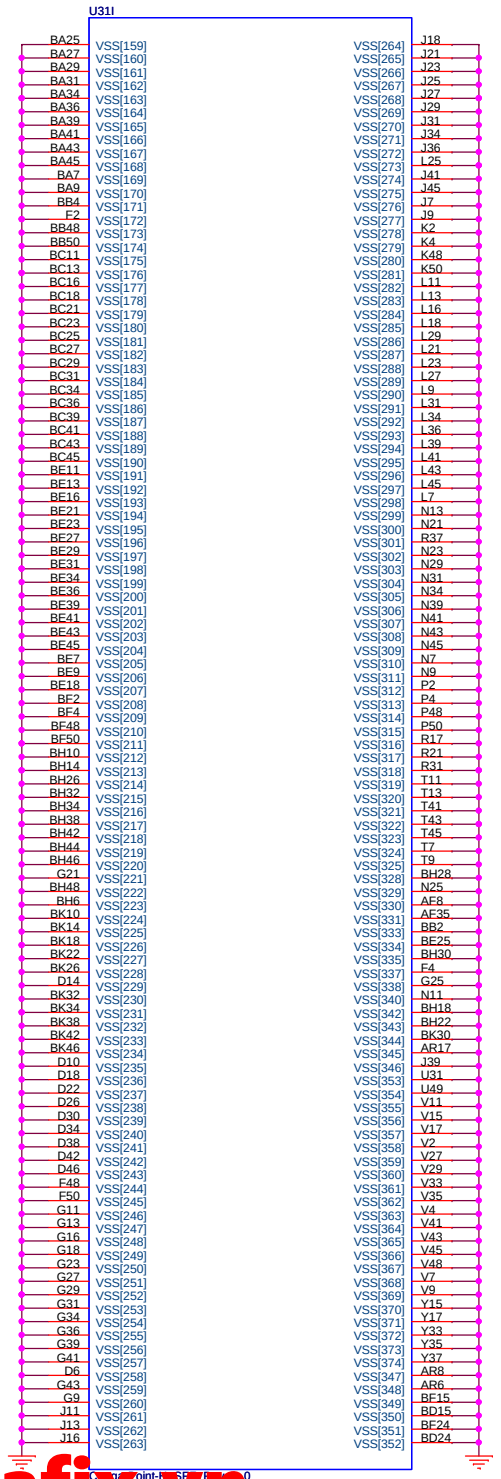


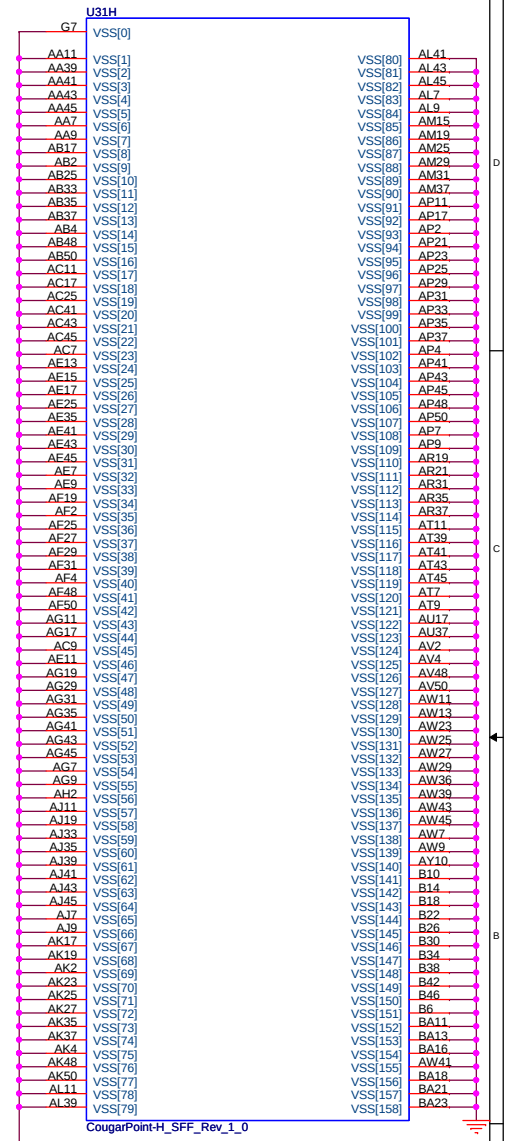




Follow R05 QT stage design




# Cougar Point (GND)

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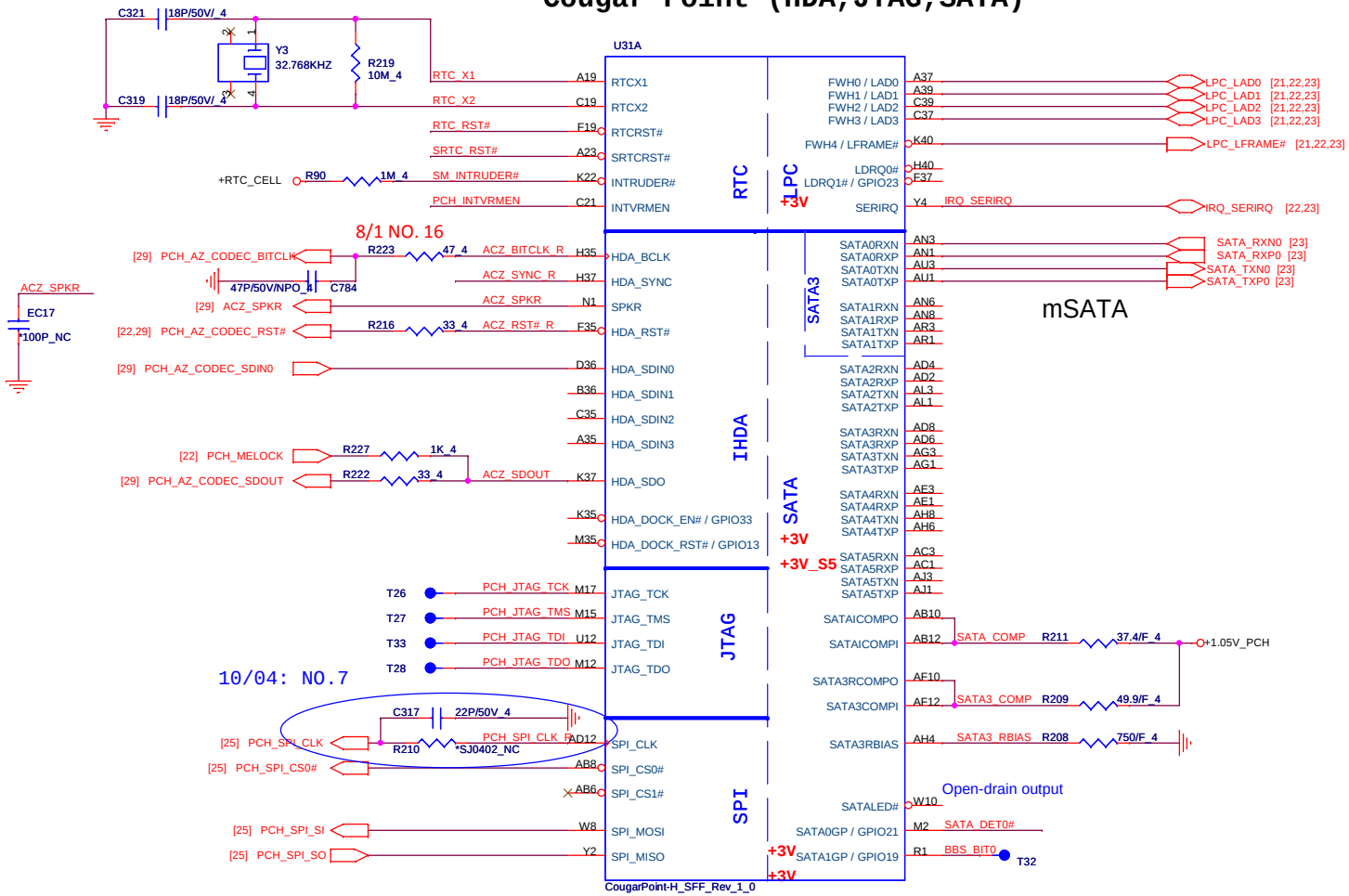
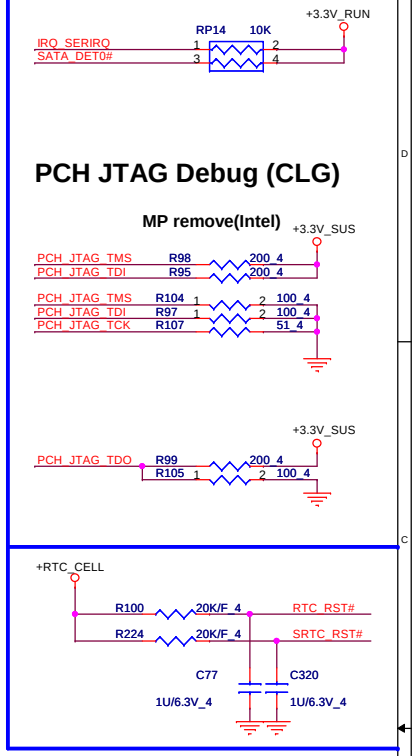
# Cougar Point (HDA,JTAG,SATA)




## PCH Strap Table

| Pin Name | Strap description | Sampled | Configuration | note |
|---|---|---|---|---|
| SPKR | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode | |
| HDA_SDO | Flash Descriptor Security | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Override | |
| Del 0510 | | | Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91 | |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up | +RTC_CELL R96 330K_4 PCH_INTVRMEN |
| HDA_SYNC | On-Die PLL VR Volatge Select | RSMRST | 0 = Support by 1.8V (weak PD)<br>1 = Support by 1.5V | [29] PCH_AZ_CODEC_SYNC R85 33_4 1K_4 R89 +3.3V_SUS ACZ_SYNC_R |




| | | | |
|---|---|---|---|
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# Cougar Point-M (PCI,USB,NVRAM)

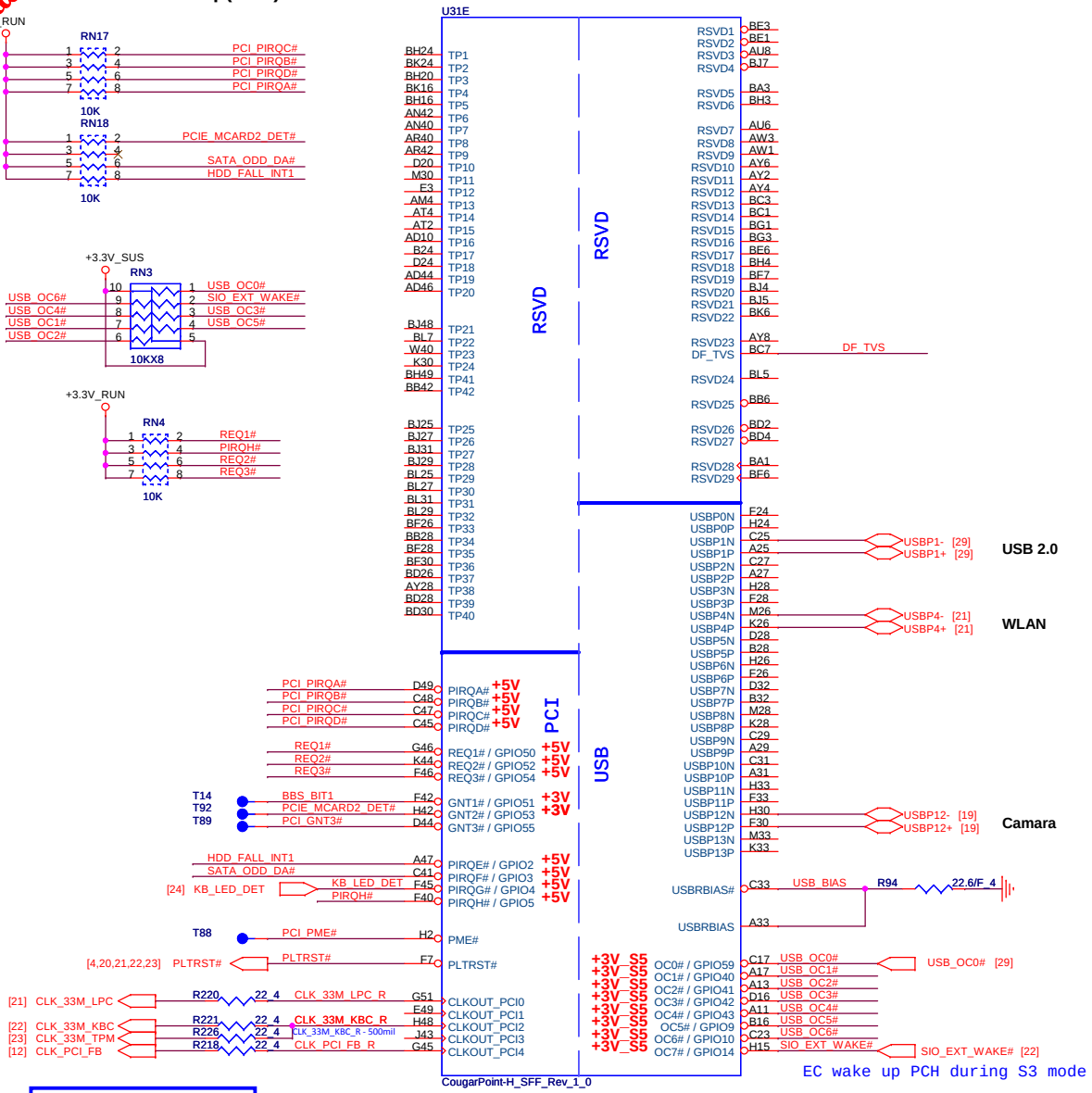
## PCI/USBOC# Pull-up(CLG)





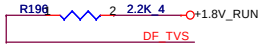




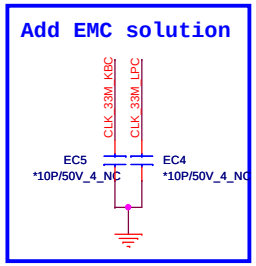




EC wake up PCH during S3 mode

| Pin Name | Strap description | Sampled | Configuration |
|---|---|---|---|
| GNT2# / GPIO53 | ESI strap (Server only) | PWROK | Should not be pull-down (weak pull-up 10K) |
| GNT3# / GPIO55 | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 10K) |
| GNT1# / GPIO51 | Boot BIOS Selection 1 [bit-1] | PWROK | Bit 0 / Bit 1 / Boot Location<br>1 / 1 / SPI *<br>0 / 0 / LPC |
| GPIO19 | Boot BIOS Selection 0 [bit-0] | PWROK | |
| | | | Default weak pull-up on GNT0/1# (Internal PU) |
| DF_TVS | DMI and FDI Tx/Rx Termination Voltage | PWROK | weak pull-down 20kohm |




CheckList_1.5 p72; HR_v1.5 p476

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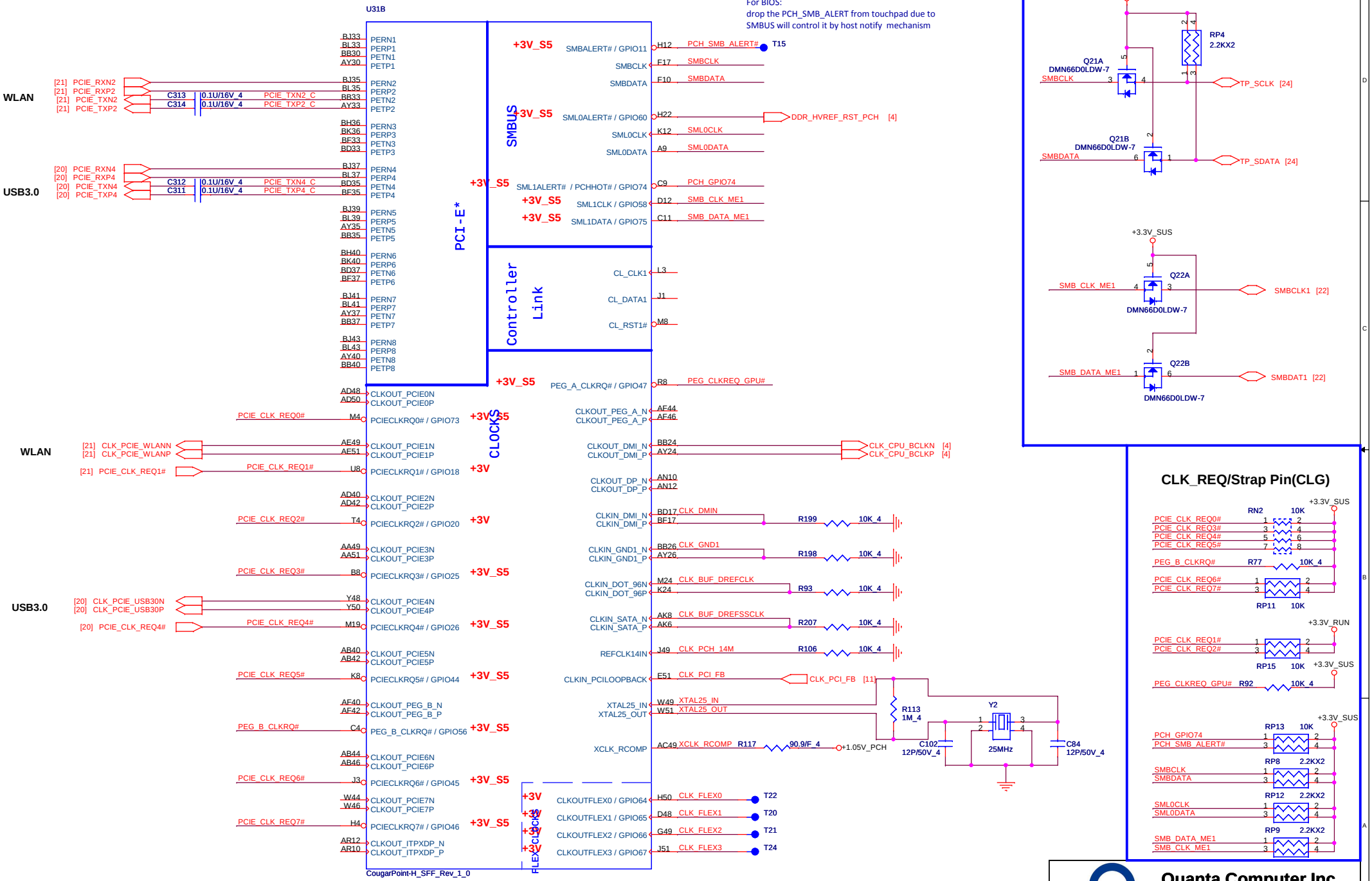
# Cougar Point-M (PCI-E,SMBUS,CLK)




## SMBus/Pull-up(CLG)




## CLK_REQ/Strap Pin(CLG)




| | | | |
|---|---|---|---|
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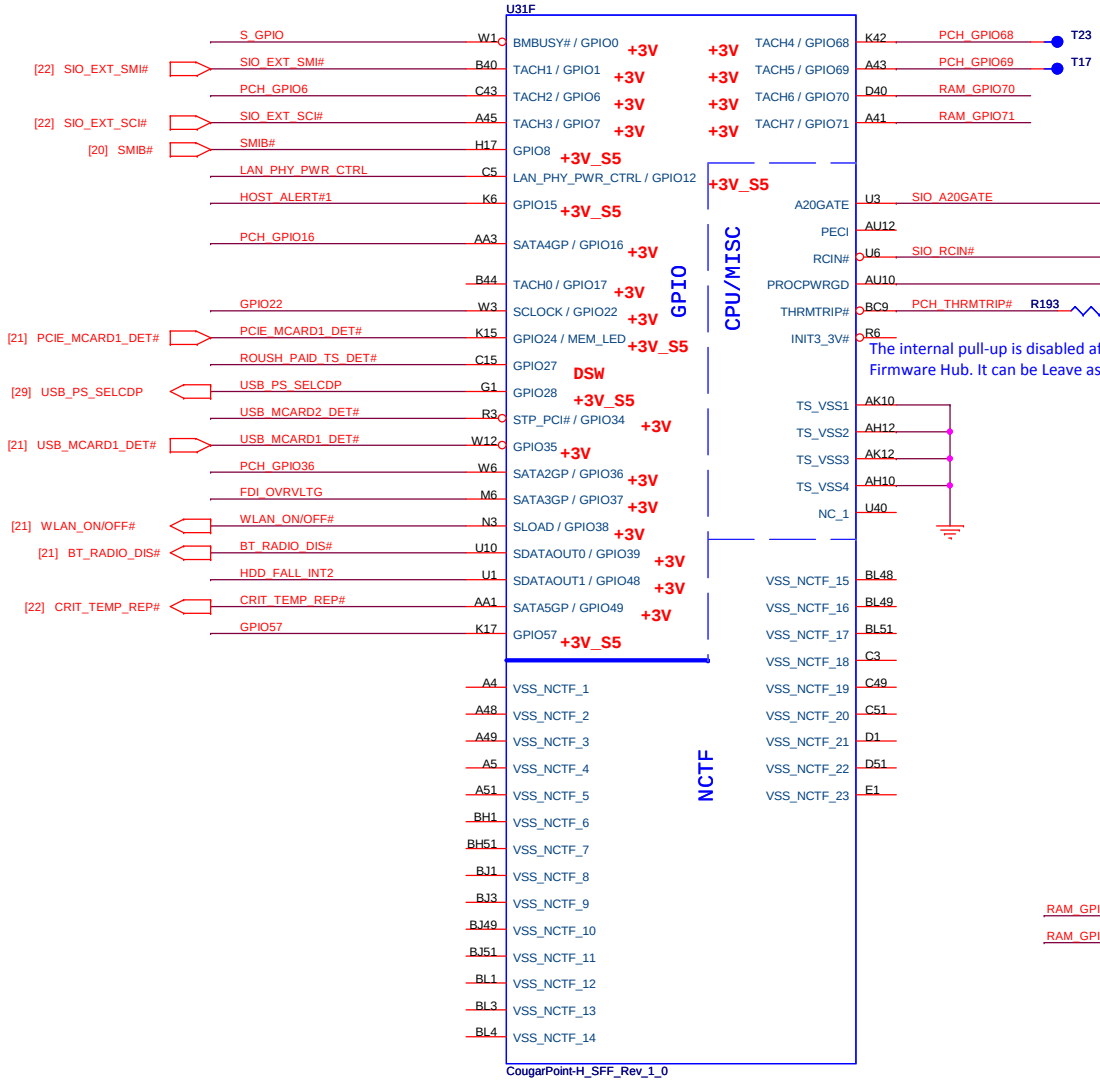
# Cougar Point (GPIO,VSS_NCTF,RSVD)

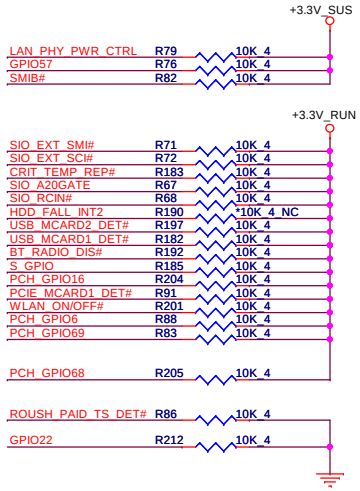
| Pin Name | Strap description | Sampled | Configuration |
|---|---|---|---|
| GPIO28 | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable<br>1 = Enable (Default) |
| Internal PU | | | |

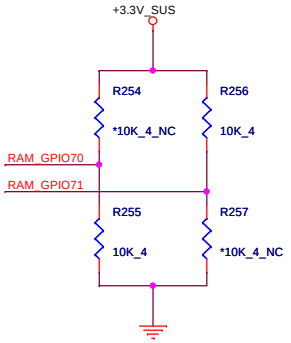
USB_PS_SELCDP R215 *10K_4_NC




The internal pull-up is disabled after PLTRST# deasserts. This signal is intended for Firmware Hub. It can be Leave as "No Connect". (desktop SKUs only)

## GPIO Pull-up/Pull-down(CLG)




RAM Vender select

| RAM_GPIO70 | R254(1) | R255(0) |
|---|---|---|
| Samsung | | V |
| Hynix | V | |

RAM size select

| RAM_GPIO71 | R256(1) | R257(0) |
|---|---|---|
| 2G | | V |
| 4G | V | |

FDI_OVRVLTG R111 100K_4

| | |
|---|---|
| FDI TERMINATION VOLTAGE OVERRIDE | LOW - Tx, Rx terminated to same voltage |

+3.3V_RUN R200 1 2 200K/F_4 PCH_GPIO36

| | |
|---|---|
| DMI TERMINATION VOLTAGE OVERRIDE | Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT) |

## Reserve (PDC)

+3.3V_SUS HOST_ALERT#1 R87 1K_4

| |
|---|
| Intel ME Crypto Transport Layer Security (TLS) cipher suite |
| Low = Disable (Default) |
| High = Enable |

MFG-TEST

del 0527

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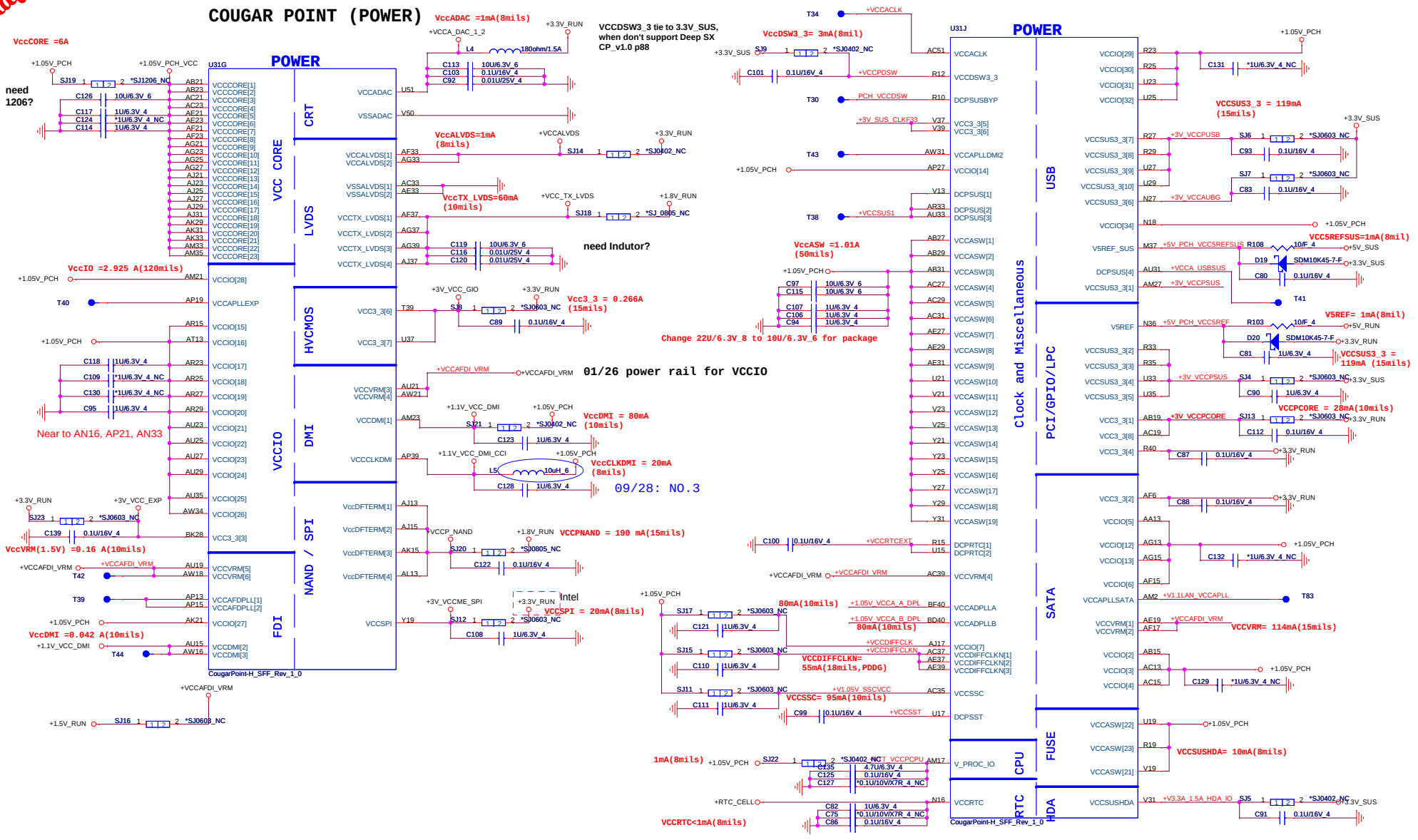
# COUGAR POINT (POWER)

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| | | |
|---|---|---|
| Quanta Computer Inc. | | |
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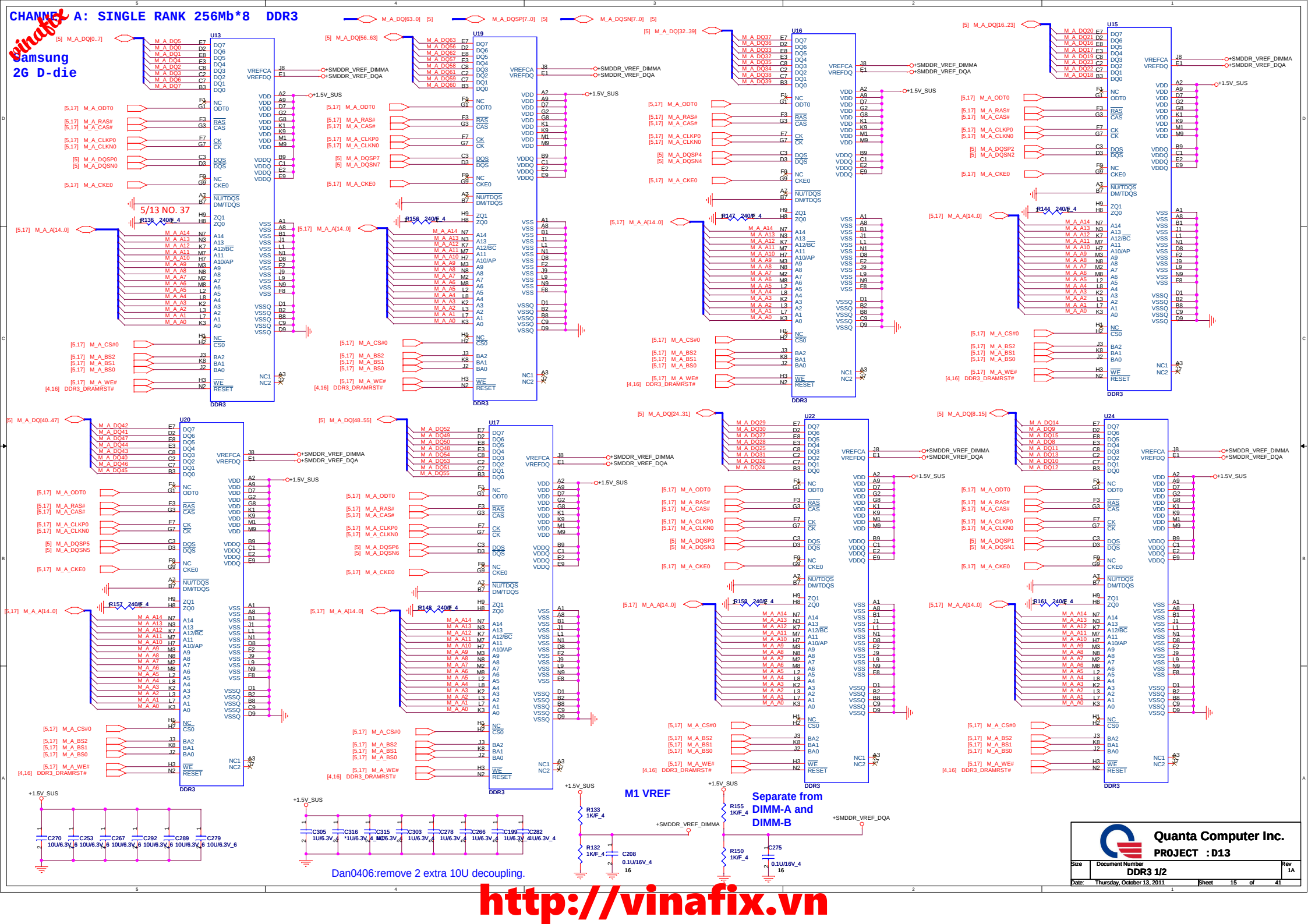
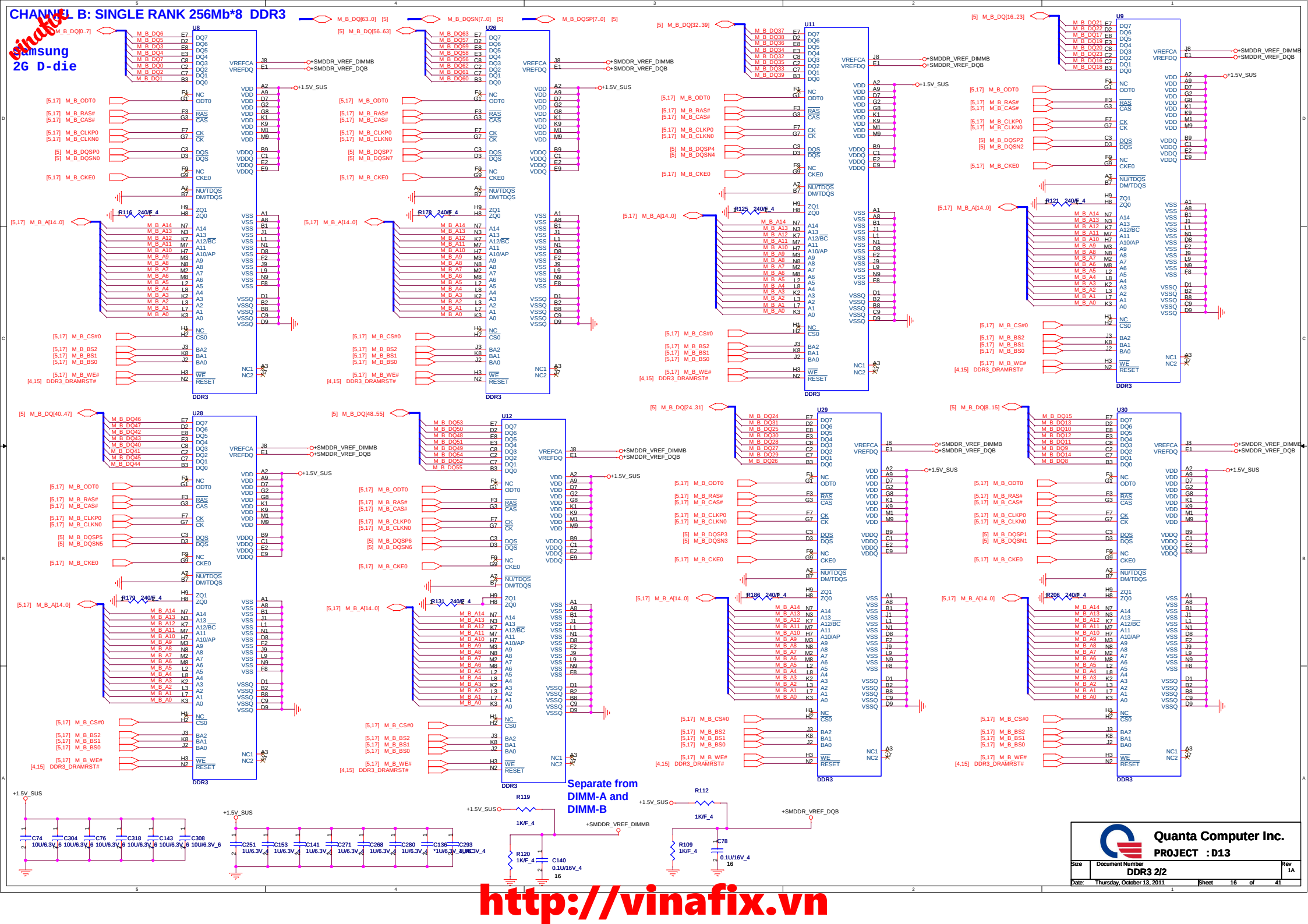

CHANNEL A: SINGLE RANK 256Mb*8 DDR3
vinafix
Samsung
2G D-die
5/13 NO. 37
M1 VREF
Separate from
DIMM-A and
DIMM-B
Dan0406:remove 2 extra 10U decoupling.
Quanta Computer Inc.
PROJECT : D13
DDR3 1/2
Thursday, October 13, 2011
http://vinafix.vn


CHANNEL B: SINGLE RANK 256Mb*8 DDR3
Samsung
2G D-die
U8
U26
U11
U9
U28
U12
U29
U30
DDR3
Separate from
DIMM-A and
DIMM-B
Quanta Computer Inc.
PROJECT : D13
DDR3 2/2
Thursday, October 13, 2011
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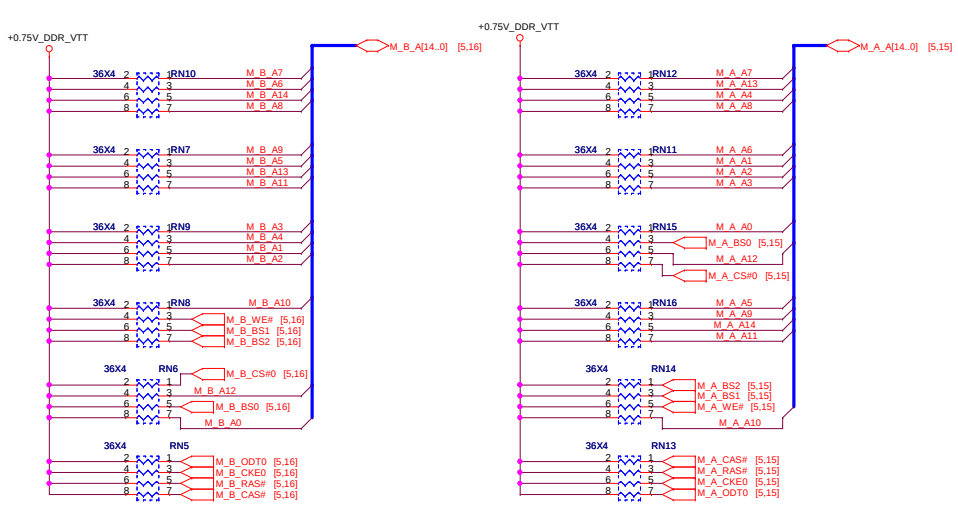





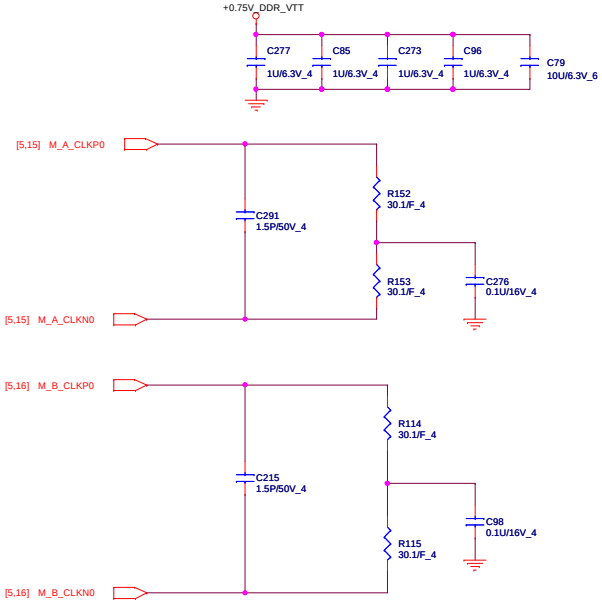


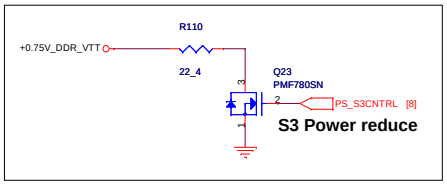


Quanta Computer Inc.
PROJECT : D13

| Size | Document Number | Rev |
|---|---|---|
| | DDR3 TERMINATION | 1A |
| Date: Thursday, October 13, 2011 | Sheet 17 of 41 | |

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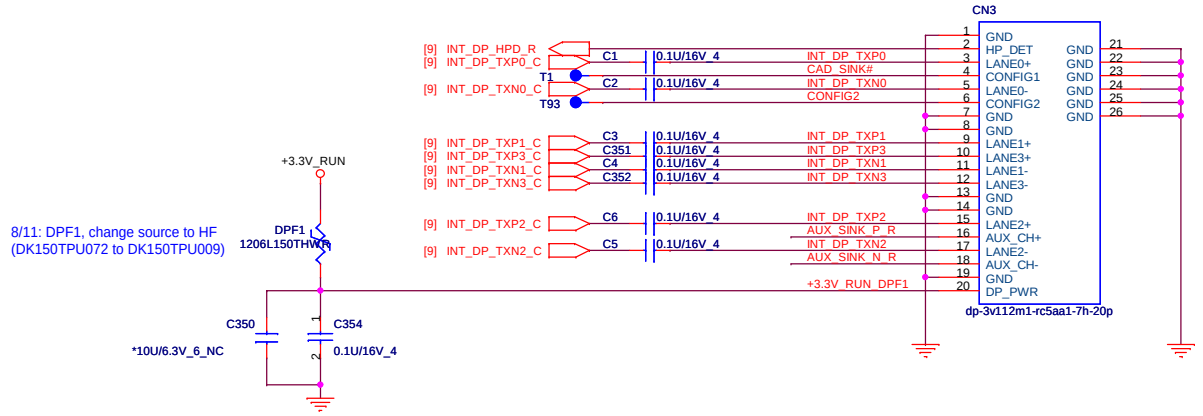
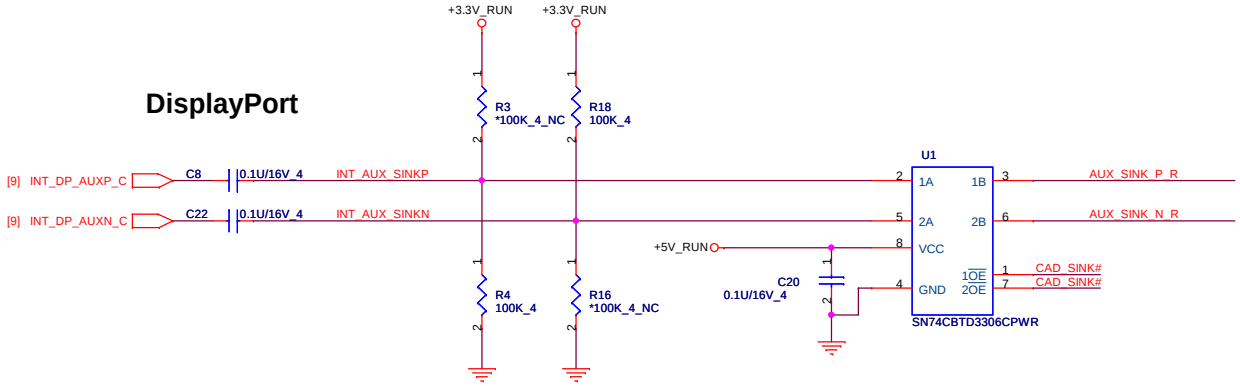
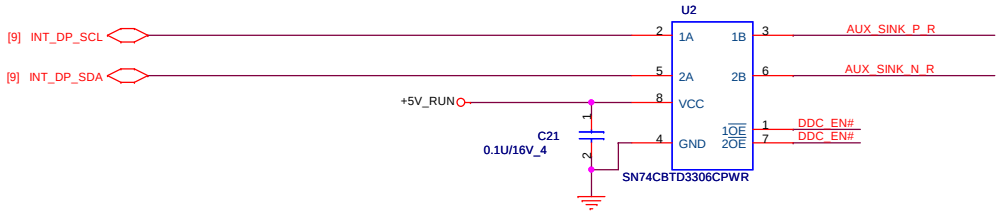
# MINI DISPLAY PORT CONNECTOR

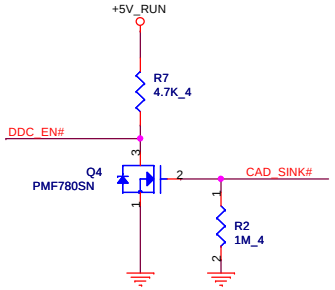



## DisplayPort




## HDMI

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| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : D13 | | |
| Size | Document Number: MINI DP CONN | Rev: 1A |
| Date: Thursday, October 13, 2011 | Sheet 18 of 41 | |

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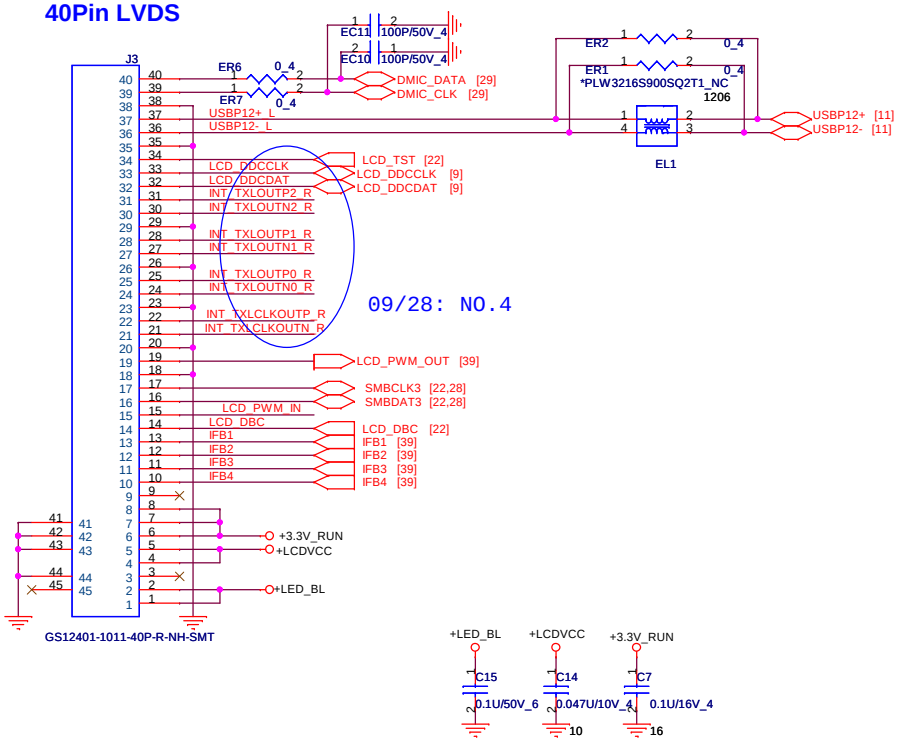
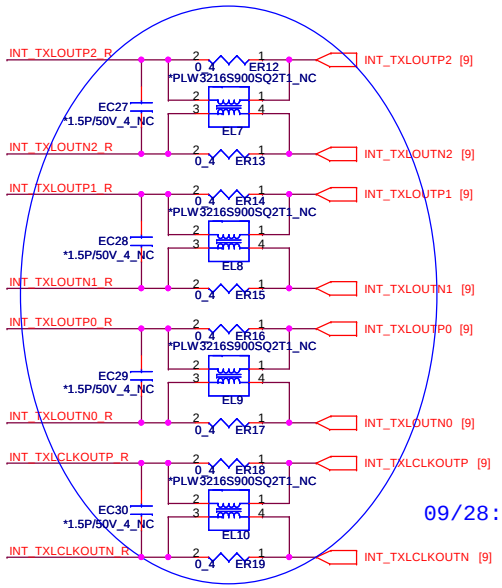
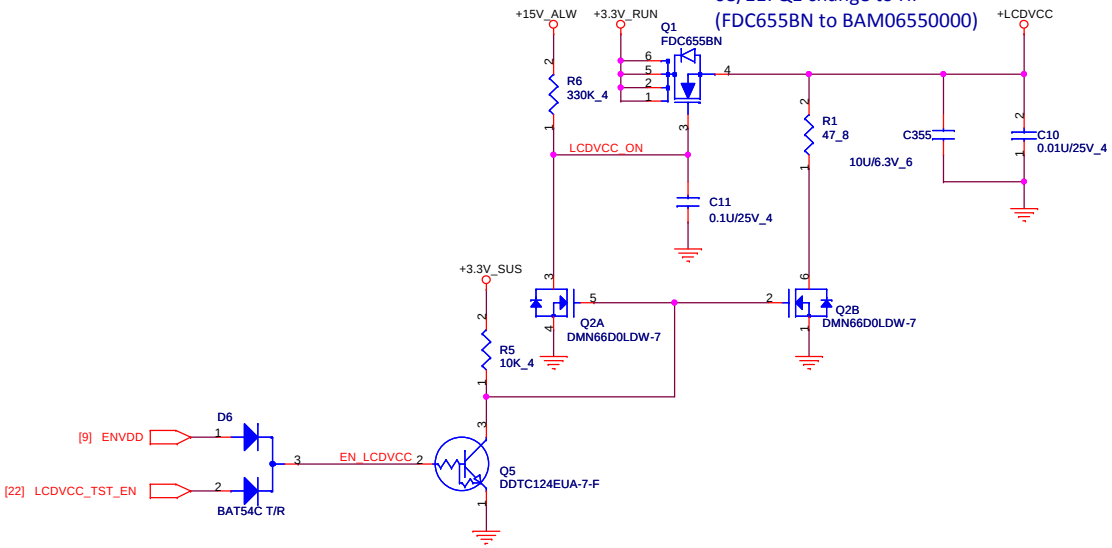
## 40Pin LVDS

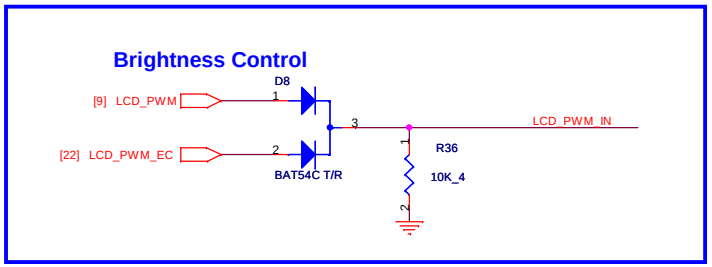






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| Size | Document Number | Rev |
|---|---|---|
| | LVDS CONN | 1A |
| Date: Thursday, October 13, 2011 | Sheet 19 of 41 | |

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| PVCC33X | | |
|---|---|---|
| Min | Typ | Max |
| 3.15V | 3.30V | 3.45V |
| Current = 36mA | | |

| PVCCA33X | | |
|---|---|---|
| Min | Typ | Max |
| 3.15V | 3.30V | 3.45V |
| Current = 72mA | | |

| AVCC10X | | |
|---|---|---|
| Min | Typ | Max |
| 1.00V | 1.05V | 1.10V |
| Current = 164mA | | |

| AVCC10 | | |
|---|---|---|
| Min | Typ | Max |
| 1.00V | 1.05V | 1.10V |
| Current = 9mA | | |

| DVCC33X | | |
|---|---|---|
| Min | Typ | Max |
| 2.97V | 3.30V | 3.63V |
| Current = 0mA | | |

| DVCC33 | | |
|---|---|---|
| Min | Typ | Max |
| 2.97V | 3.30V | 3.63V |
| Current = 5mA | | |

| DVCC10X | | |
|---|---|---|
| Min | Typ | Max |
| 1.00V | 1.05V | 1.10V |
| Current = 25mA | | |

| DVCC10 | | |
|---|---|---|
| Min | Typ | Max |
| 1.00V | 1.05V | 1.10V |
| Current = 90mA | | |

09/28: NO.5

TX base on FL1009

RX base on FL1009

CANNOT floating even if it hasn't been used

10/04 NO.7

Need closed to CN4

10/204 NO.7

Vout=0.8*(R222+R223)/R223

FL1009

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Quanta Computer Inc.

PROJECT : D13

TI USB 3.0

Rev 1A

Date: Thursday, October 13, 2011 Sheet 20 of 41

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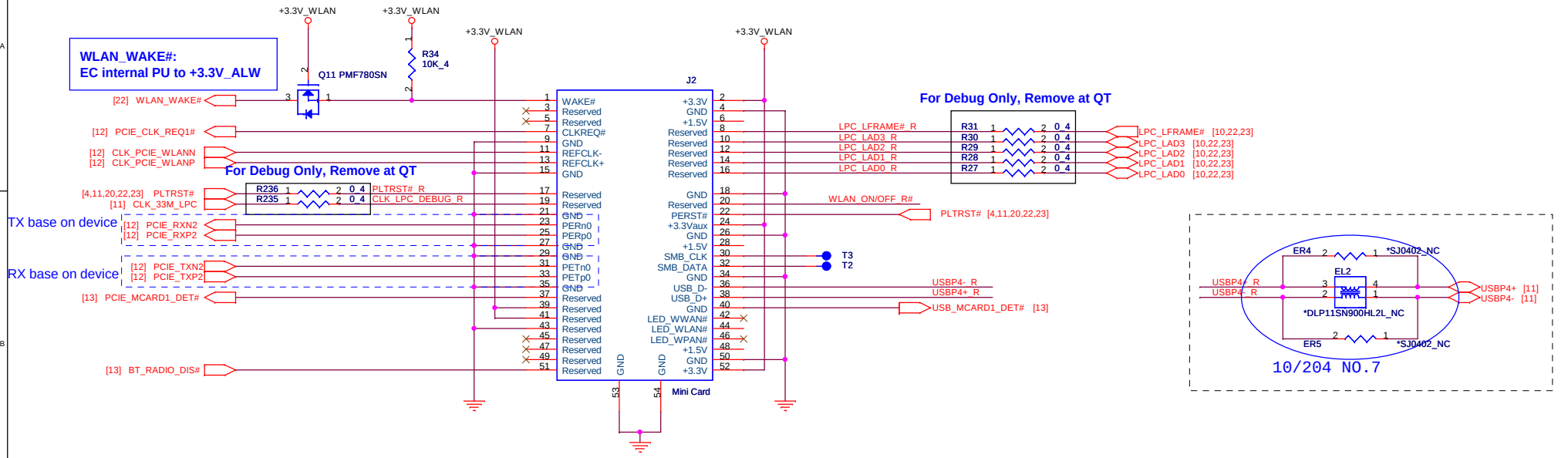
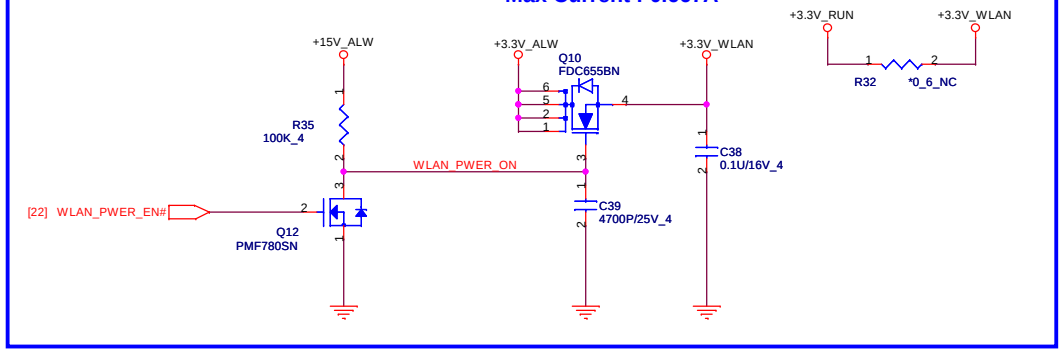
# MiniCard WLAN connector

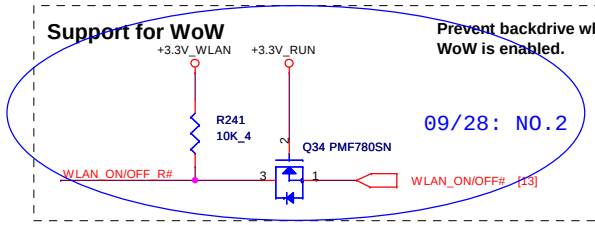


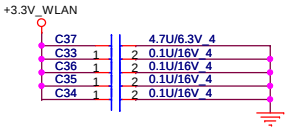




## +3.3V_WLAN
## Max Current : 0.667A




Quanta Computer Inc.
PROJECT : D13

| Size | Document Number | Rev |
|---|---|---|
| | MINI-PCI (WLAN/WPAN) | 1A |

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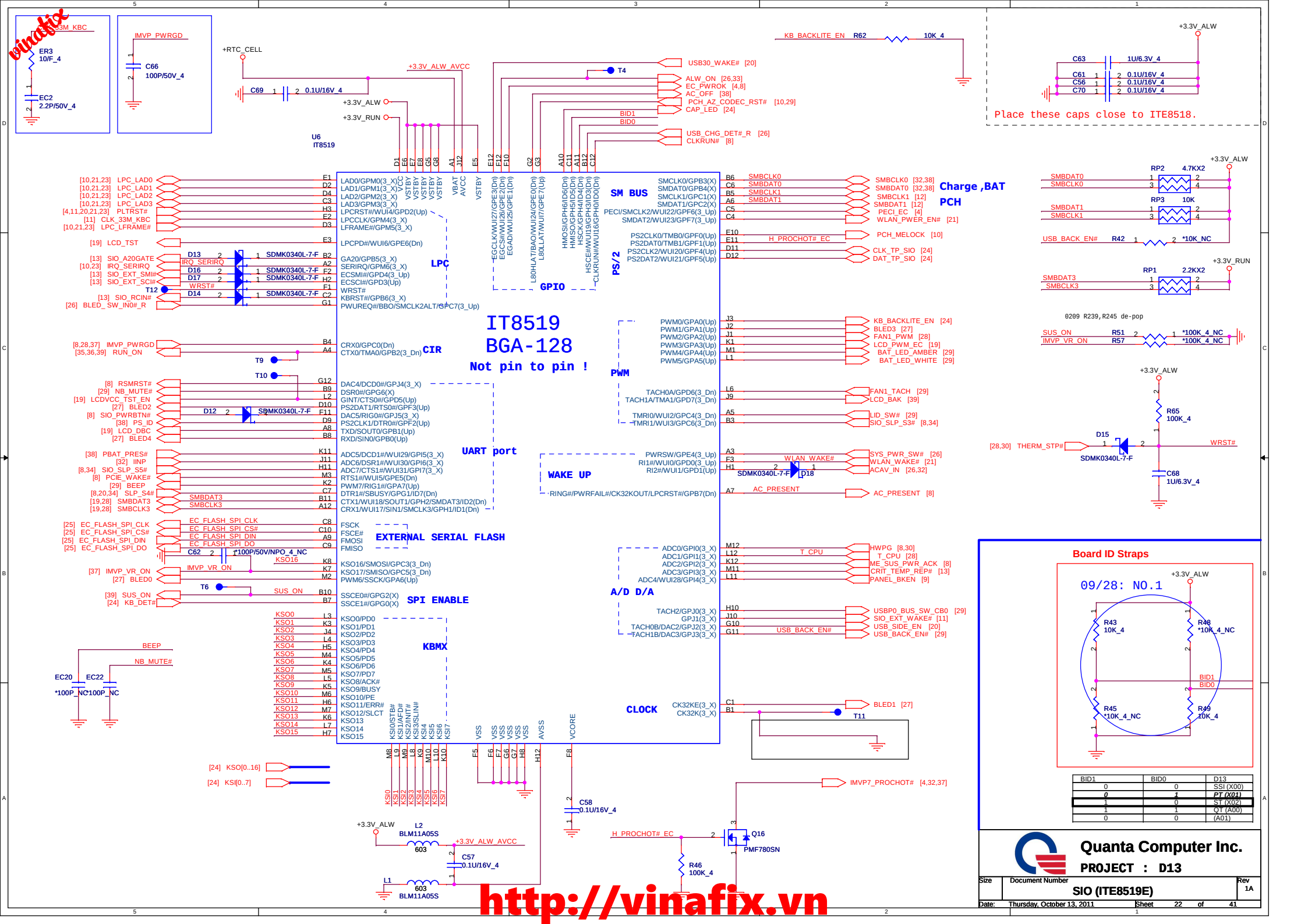
IT8519
BGA-128
Not pin to pin !
SM BUS
PS/2
GPIO
LPC
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Charge ,BAT
PCH
Place these caps close to ITE8518.
Board ID Straps
09/28: NO.1
0209 R239,R245 de-pop
Quanta Computer Inc.
PROJECT : D13
SIO (ITE8519E)
Thursday, October 13, 2011
http://vinafix.vn

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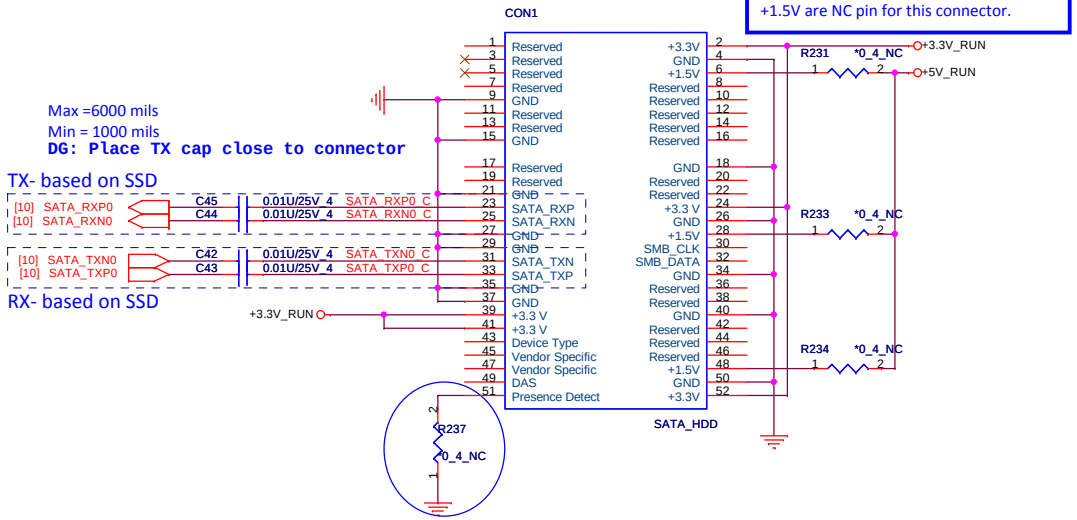
## mSATA Connector

+5V_RUN is for testing mSATA by factory.
+1.5V are NC pin for this connector.




Max =6000 mils
Min = 1000 mils
**DG: Place TX cap close to connector**

TX- based on SSD

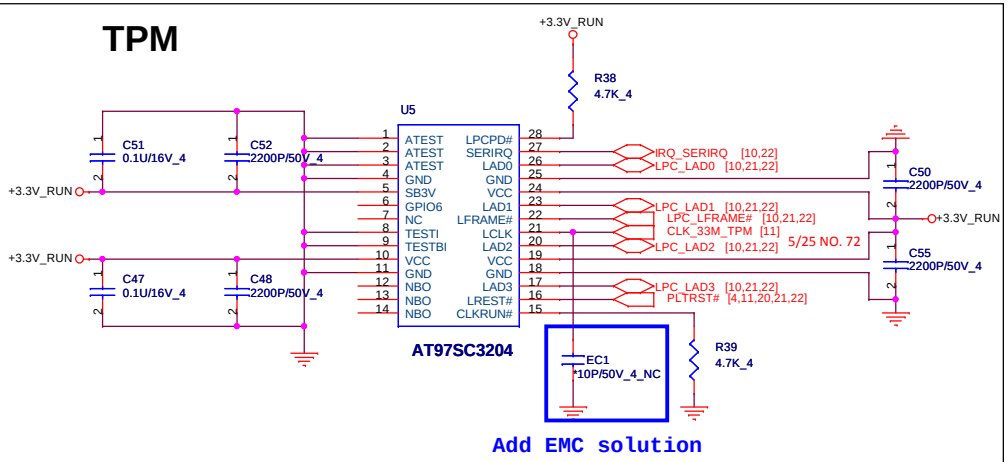
[10] SATA_RXP0 — C45 0.01U/25V_4 — SATA_RXP0_C
[10] SATA_RXN0 — C44 0.01U/25V_4 — SATA_RXN0_C

[10] SATA_TXN0 — C42 0.01U/25V_4 — SATA_TXN0_C
[10] SATA_TXP0 — C43 0.01U/25V_4 — SATA_TXP0_C

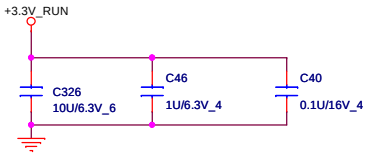
RX- based on SSD

10/204 NO.7

## TPM




**Add EMC solution**




**Place caps close to connector.**

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : D13 | | |
| Size | Document Number: SATA HDD/ODD | Rev 1A |
| Date: Thursday, October 13, 2011 | Sheet 23 of 41 | |

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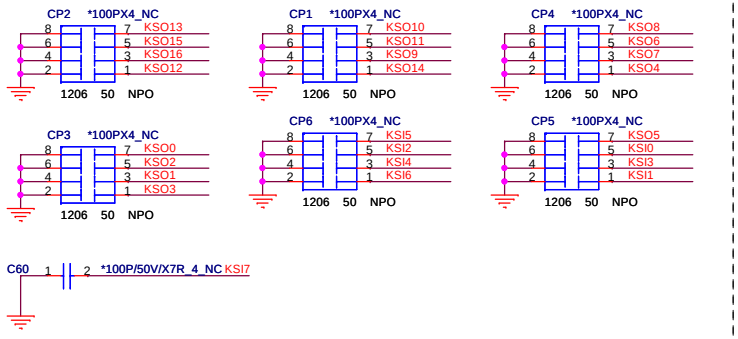
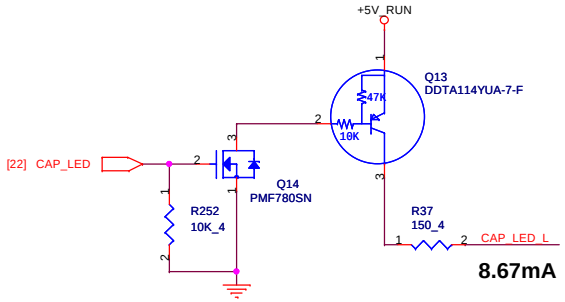
## KEYBOARD CONNECTOR

**03/30 Change CP1,CP2,CP3,CP4,CP5,CP6,C382 from Pop to Depop**



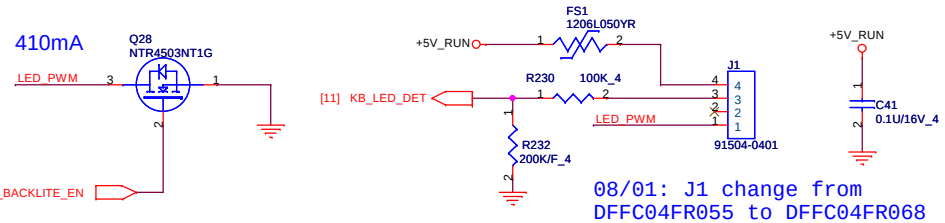

**Vi(on_max)= -1.4V**
**Vi(off_min)=-0.3**




**8.67mA**

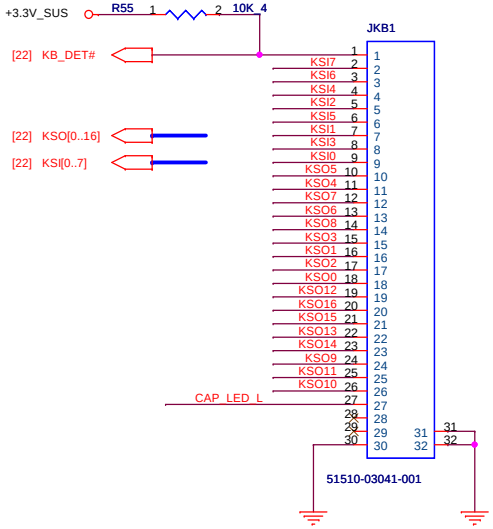
## Key board illumination

**+KB_LED power trace width >10 mil**



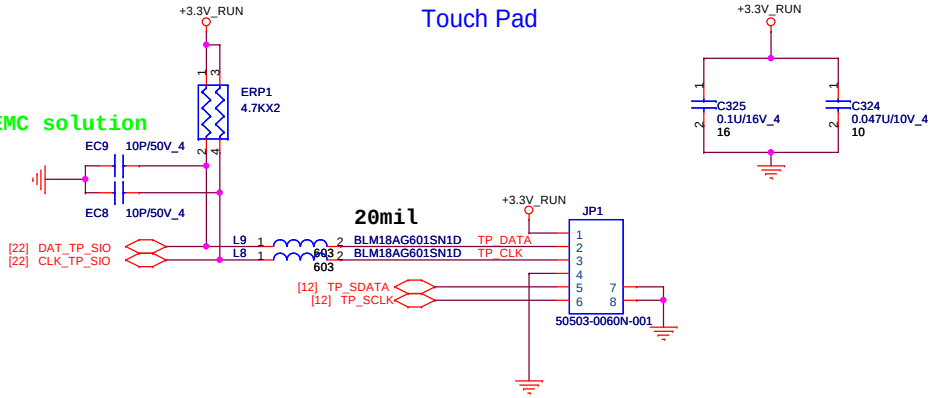

08/01: J1 change from
DFFC04FR055 to DFFC04FR068

## KEYBOARD CONNECTOR




## Touch Pad

**Add EMC solution**

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Quanta Computer Inc.
PROJECT : D13

| Size | Document Number | Rev |
|---|---|---|
| | TP / KB | 1A |

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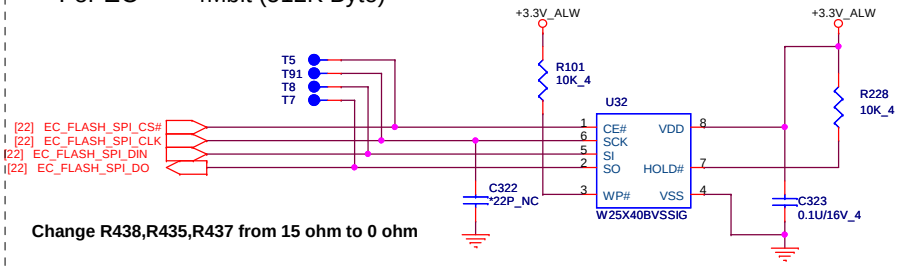
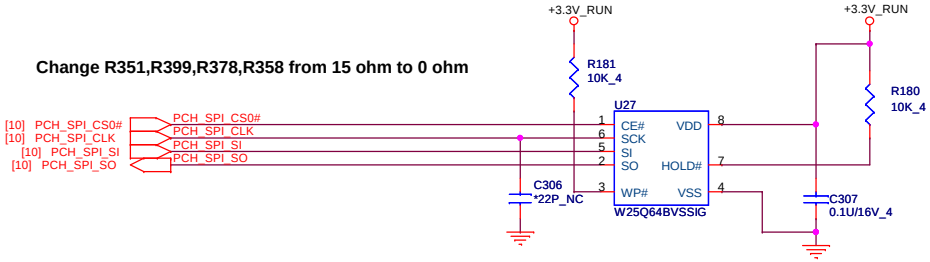
## For EC 4Mbit (512K Byte)




**Change R438,R435,R437 from 15 ohm to 0 ohm**

## For PCH 64Mbit (8M Byte)

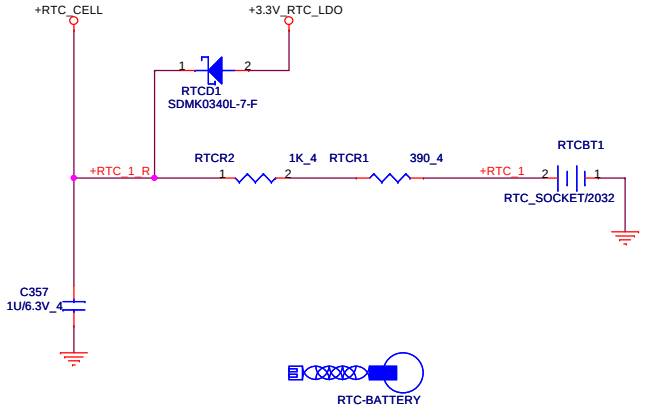



**Change R351,R399,R378,R358 from 15 ohm to 0 ohm**

Change SPI ROM for BIOS to AKE3EFP0N04 -0613

The max charge current is flow on charged at the end voltage of battery
2V. And the charge current is 1mA.
R >= (+RTC_CELL - 2)/1mA

## RTC BATTERY




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : D13 | | |
| Size | Document Number: FLASH / RTC | Rev: 1A |
| Date: Thursday, October 13, 2011 | Sheet 25 of 41 | |

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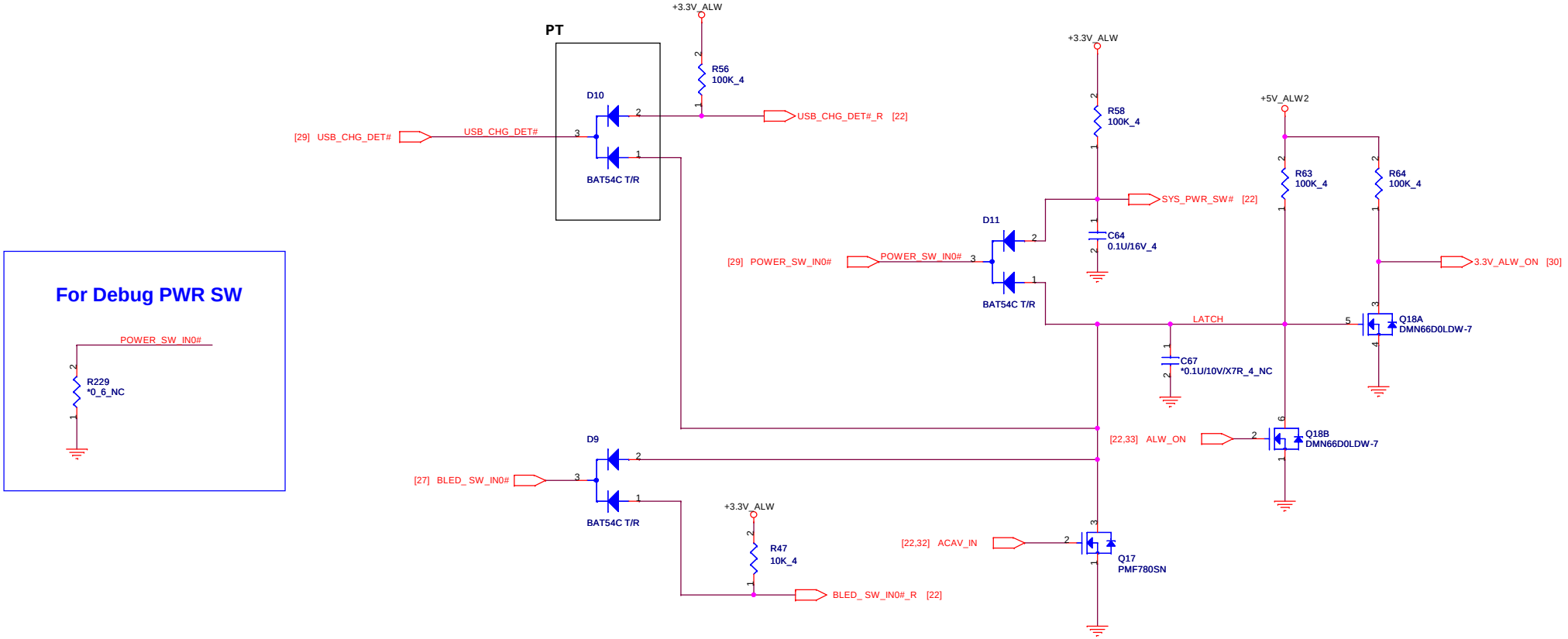
# 3VALW ON POWER LOGIC




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : D13 | | |
| Size | Document Number: PWR SW/LED | Rev: 1A |
| Date: Thursday, October 13, 2011 | Sheet 26 of 41 | |

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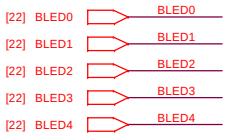
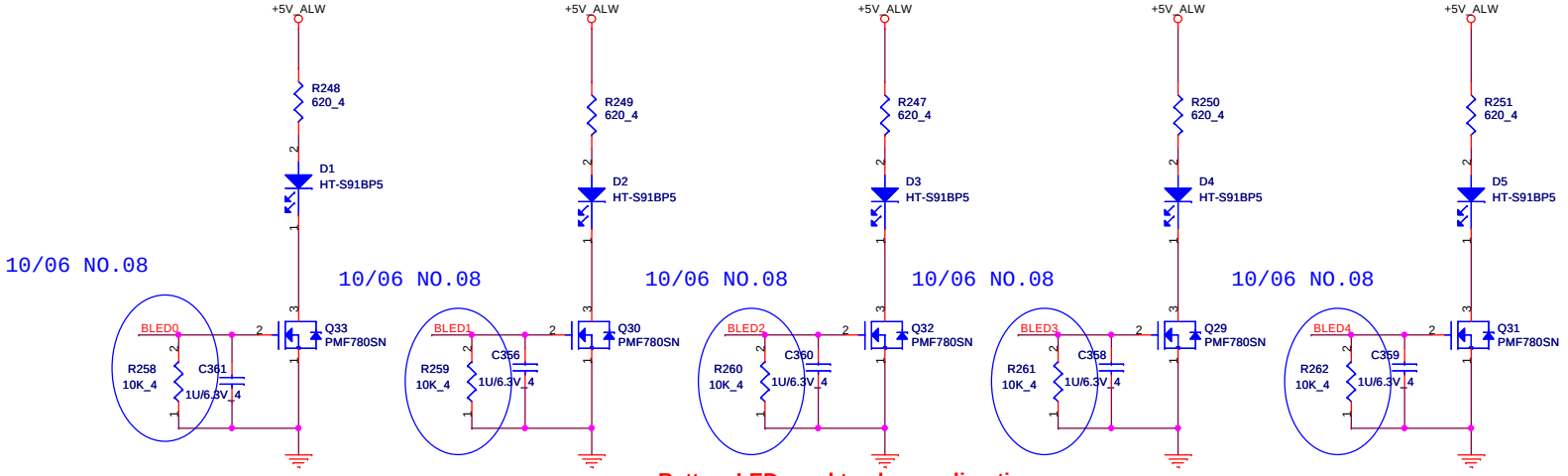
## Truth table of Battery LED

| Battery Power State | BLED4 | BLED3 | BLED2 | BLED1 | BLED0 | LED State |
|---|---|---|---|---|---|---|
| <20% | 0 | 0 | 0 | 0 | 0 | N/A |
| 20% | 0 | 0 | 0 | 0 | 1 | D29 |
| 40% | 0 | 0 | 0 | 1 | 1 | D29 D30 |
| 60% | 0 | 0 | 1 | 1 | 1 | D29 D30 D31 |
| 80% | 0 | 1 | 1 | 1 | 1 | D29 D30 D31 D32 |
| 100% | 1 | 1 | 1 | 1 | 1 | D29 D30 D31 D32 D33 |

## Battery Status LED

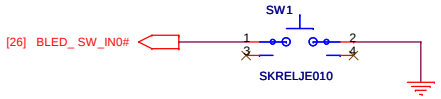



10/14, change current limit resistor from 365 ohm to 620




Battery LED need to change direction

### Battery LED button




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : D13 | | |
| Size | Document Number: LED SWITCH | Rev 1A |
| Date: Friday, October 14, 2011 | Sheet 27 of 41 | |

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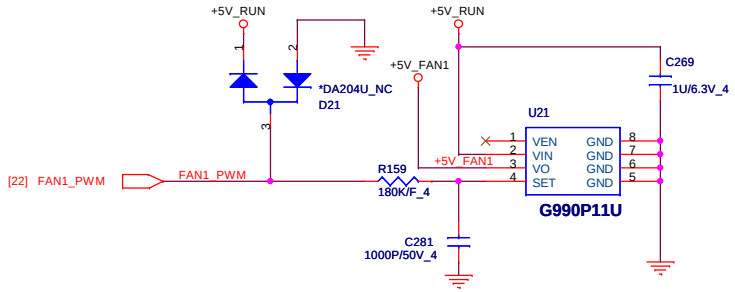
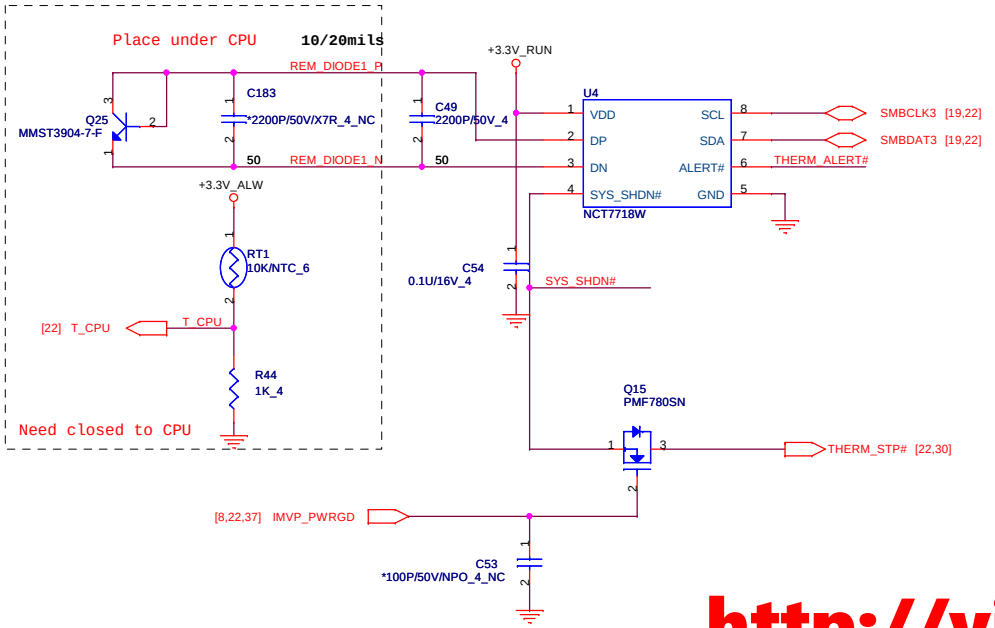
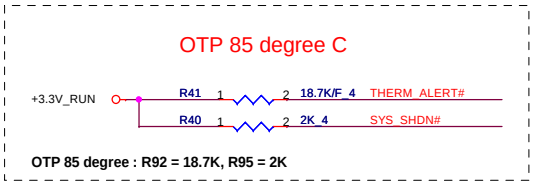



# THERMAL IC




| SYS_SHD# / ALERT# | 2K | 7.5K | 10.5K | 14K | 18.7K |
|---|---|---|---|---|---|
| 2K | 77'C | 87'C | 97'C | 107'C | 117'C |
| 7.5K | 79'C | 89'C | 99'C | 109'C | 119'C |
| 10.5K | 81'C | 91'C | 101'C | 111'C | 121'C |
| 14K | 83'C | 93'C | 103'C | 113'C | 123'C |
| 18.7K | 85'C | 95'C | 105'C | 115'C | 125'C |




Quanta Computer Inc.
PROJECT : D13

| Size | Document Number | Rev |
|---|---|---|
| | FAN & THERMAL | 1A |

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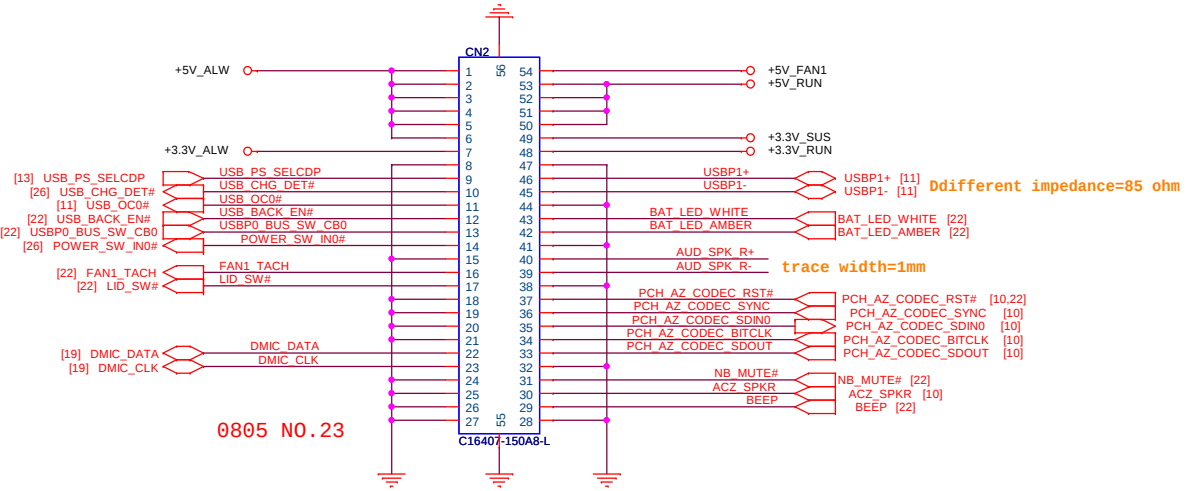
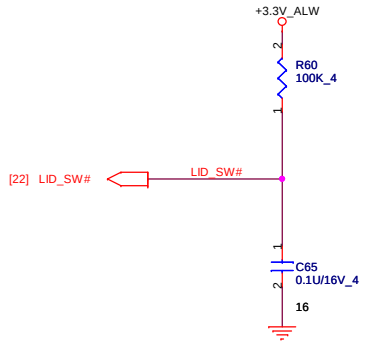
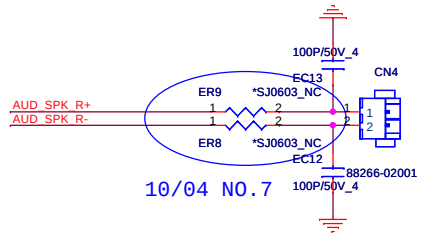



08/01: change CN4 PN from DFHD02MR401 change to DFHD02MR045




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : D13 | | |
| Size | Document Number: BTB connector | Rev: 1A |
| Date: Thursday, October 13, 2011 | Sheet 29 of 41 | |

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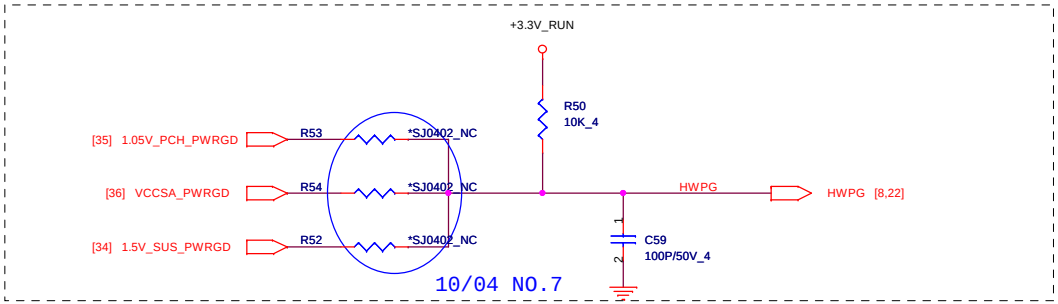


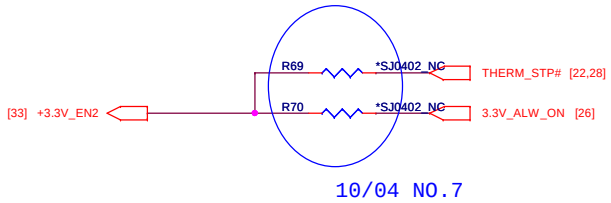


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Quanta Computer Inc.
PROJECT : D13

| Size | Document Number | Rev |
|---|---|---|
| | System Reset Circuit | 1A |

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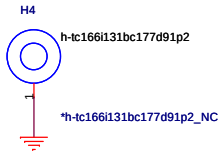
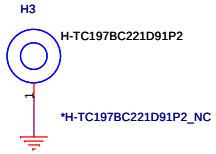
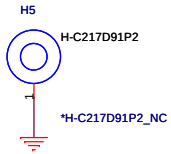
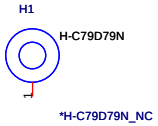
vinafix

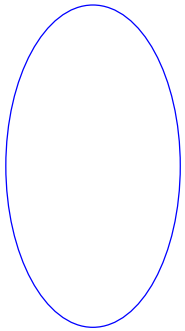


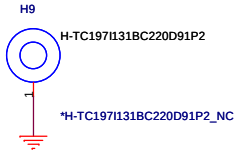



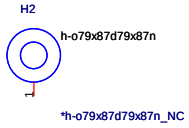



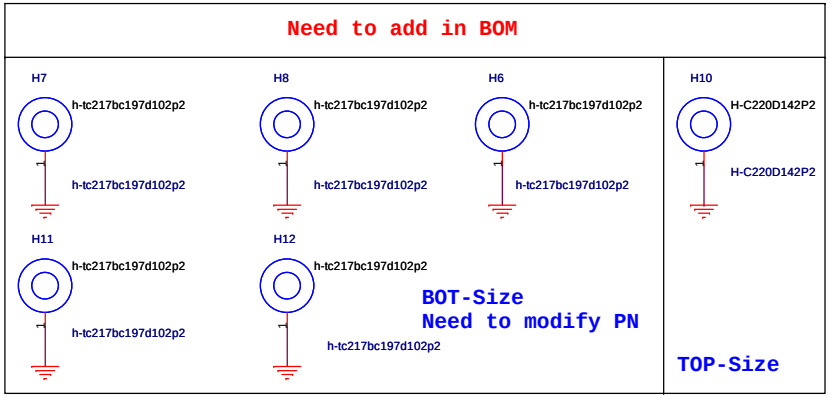




09/30: NO.6



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| Size | Document Number | Rev |
|---|---|---|
| | SCREW PAD | 1A |

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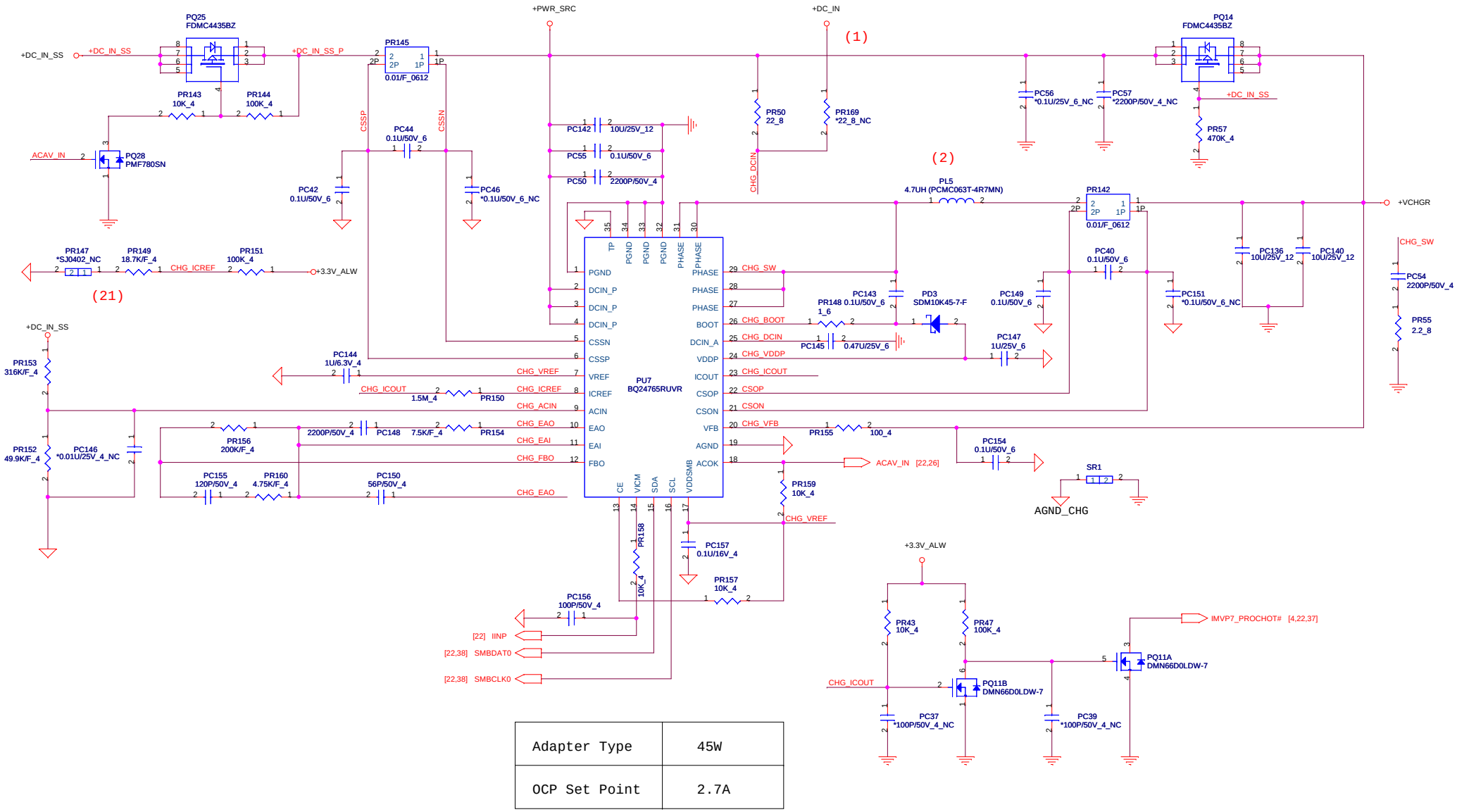


| | |
|---|---|
| Adapter Type | 45W |
| OCP Set Point | 2.7A |

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| Size | Document Number | Rev |
|---|---|---|
| | Charger (BQ24765RUVR) | 1A |

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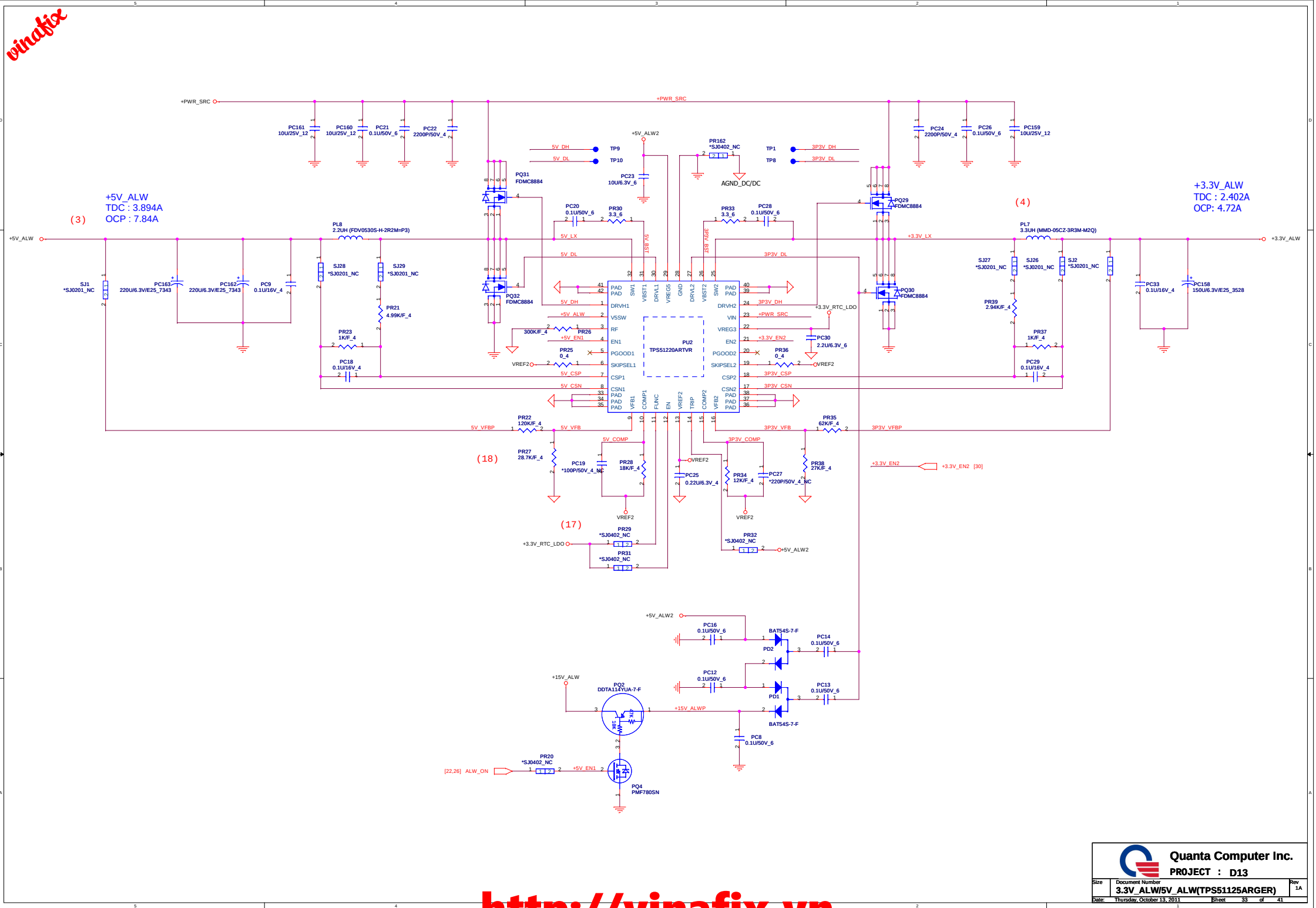


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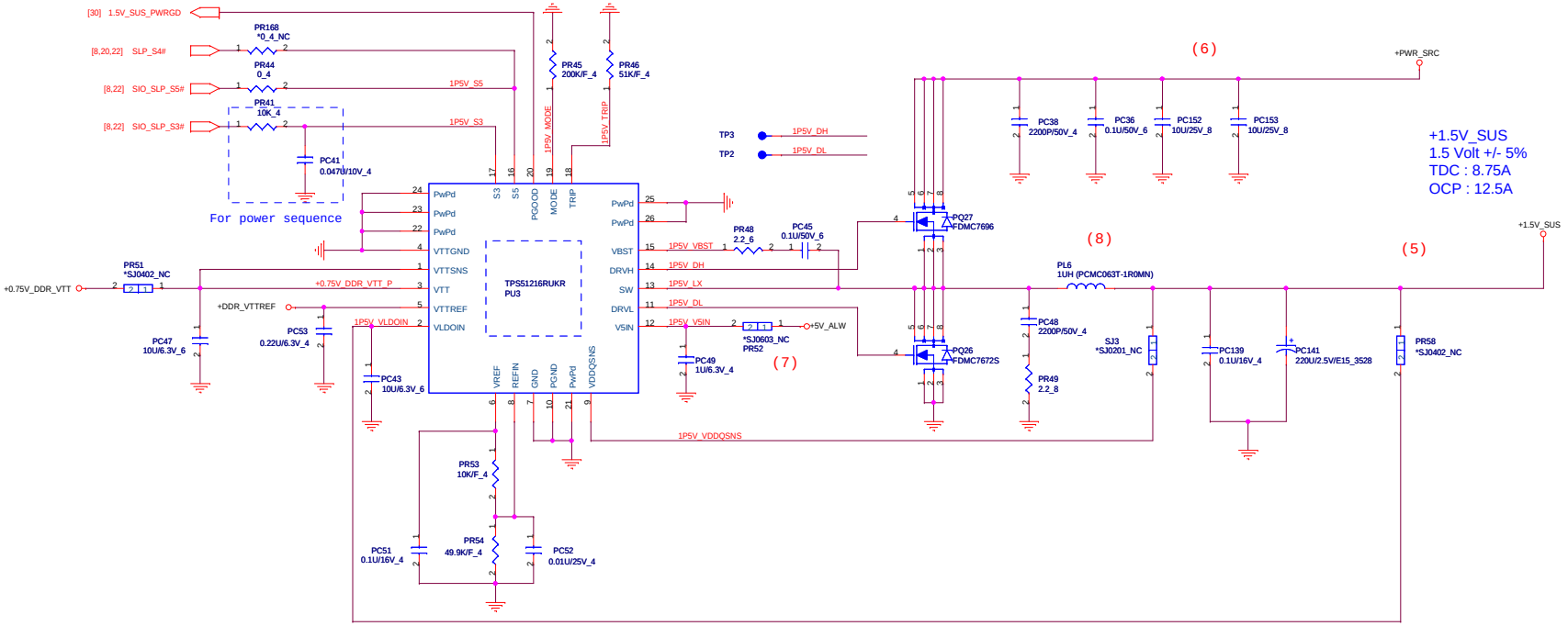


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| Size | Document Number | Rev |
|---|---|---|
| | 1.5_SUS/0.75_DDR_VTT | 1A |

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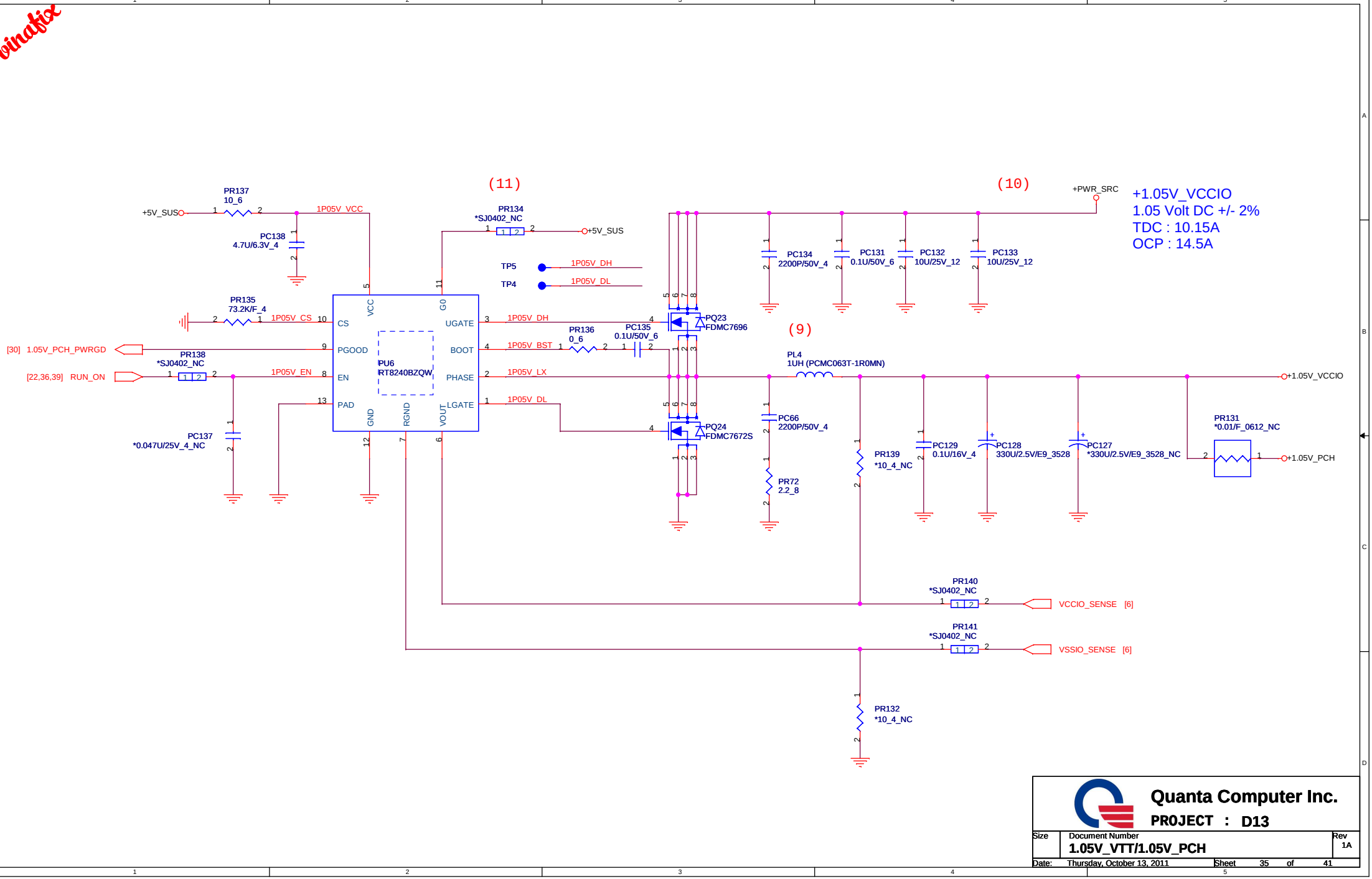


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| Size | Document Number | Rev |
|---|---|---|
| | 1.05V_VTT/1.05V_PCH | 1A |

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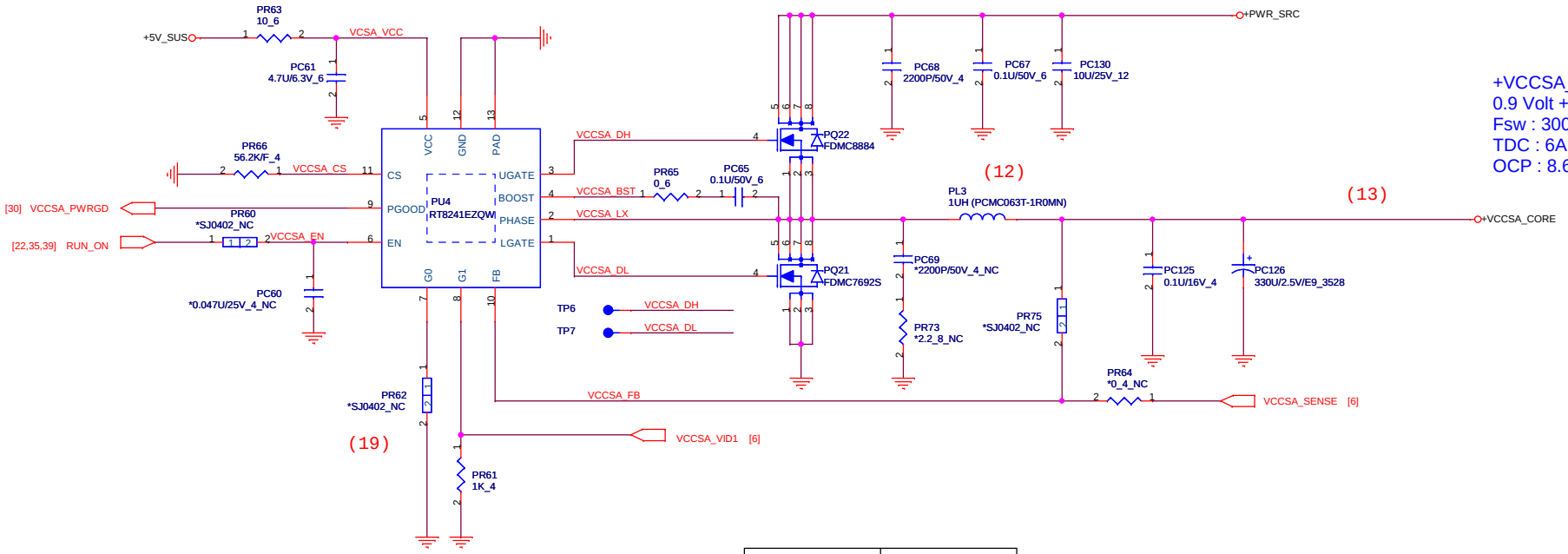
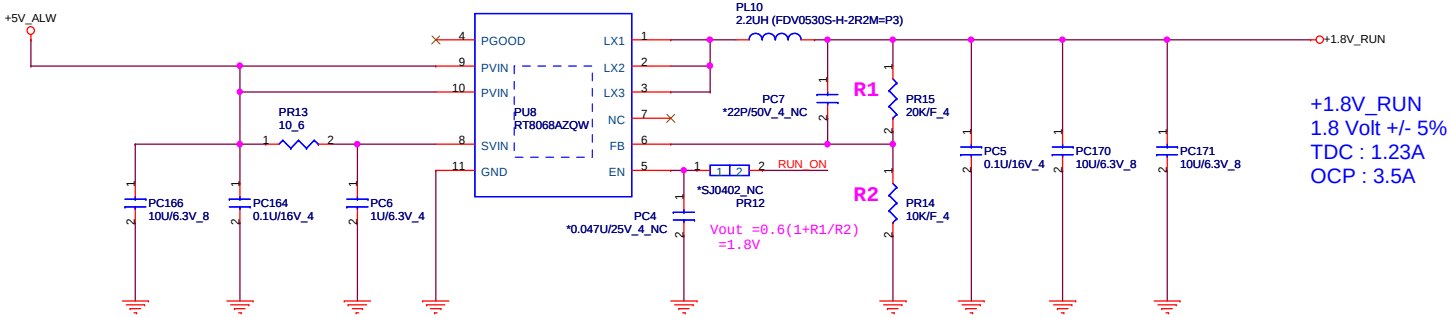



+VCCSA_CORE
0.9 Volt +/- 5%
Fsw : 300K
TDC : 6A
OCP : 8.6A

| VCCSA_VID1 | VCCSA_CORE |
|---|---|
| Low | 0.9V |
| High | 0.85V |




+1.8V_RUN
1.8 Volt +/- 5%
TDC : 1.23A
OCP : 3.5A

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| Size | Document Number | Rev |
|---|---|---|
| | VCCSA_CORE/1.8V_RUN | 1A |
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NOTE 1:
AXG Core power: Loadline ~-4.6mOhm
OCP~22A

CPU Core power: Loadline ~-2.9mOhm
OCP~40A

| | GT1 | GT2 |
|---|---|---|
| R6 | 931 / CS19312FB11 | 1.65K / CS21652FB29 |
| R7 | 1.78K / CS21782FB00 | 2.55K / CS22552FB01 |
| R8 | 169K / CS41692FB12 | 287K / CS42872FB13 |

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| Size | Document Number | Rev |
|---|---|---|
| | VCC_CORE/IGPU_CORE | 1A |

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+VCHGR

PC64 0.1U/50V_6
PC63 1000P/50V_4
PC62 2200P/50V_4

+3.3V_ALW

PD7 *DA204UGT106_NC
PD8 *DA204UGT106_NC
PD9 *DA204UGT106_NC

FOX_GS73091-10272-7H
JBAT1

PR67 100_4
PR68 100_4
PR69 100_4

SMBCLK0 [22,32]
SMBDAT0 [22,32]

PR70 10K_4

PBAT_PRES# [22]

+DCIN_JACK

EC14 0.01U/50V_4
EC15 4700P/50V_4
EC16 68P/50V_4

Reserve for EMI Solution

FL2 MHC2012S800UBP(80,5A)

+DC_IN

PC105 2200P/50V_4
PC113 1000P/50V_4
PC107 0.1U/50V_6
PC106 0.1U/50V_6

PQ15 IMD2A GZ T108

PC99 0.47U/25V_6
PR108 240K_4

PQ18 FDMC4435BZ

+DC_IN_SS

PC109 0.01U/25V_4
PC108 0.1U/50V_6
PR117 10K_6

PR103 *10K_4_NC

AC_OFF [22]

PR107 47K_4

9/30: CN1 change from D DFHD05MR080 to DFHD05MS074

CN1 50278-0050n

GND
Adapter2+ +DCIN_JACK
Adapter1+
PSID DOCK_PSID
Adapter2-
Adapter1-
GND

FL1 BLM11B102S (1K,100MA)

PD4 *BAS316_NC

PC104 100P/50V_4

PR114 100K_4
PR113 15K_4

PQ16 MMST3904-7-F

PQ17 FDV301N_G

PR116 33_4
PR112 10K_4

+5V_ALW2

+3.3V_ALW

PD5 DA204UGT106

PR115 2.2K_4

PS_ID [22]

+DC_IN_SS

EC6 0.1U/25V_4
EC7 1000P/50V_4

+DC_IN

(23)

EC3 *10P/50V_4_NC

Reserve for EMI Solution

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| Size | Document Number | Rev |
|---|---|---|
| | DCIN/BATT CONNECTOR | 1A |

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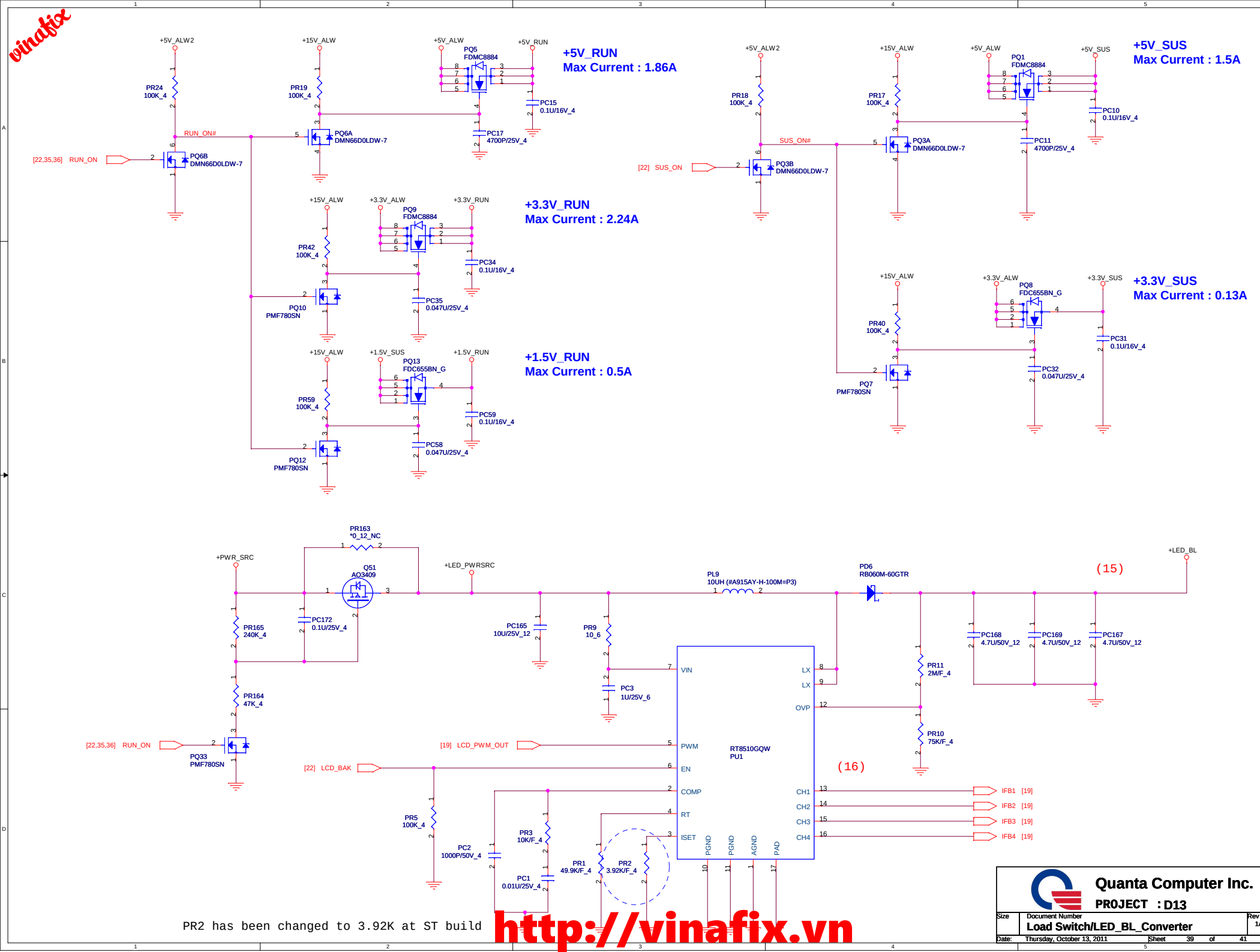
+5V_RUN
Max Current : 1.86A
+5V_SUS
Max Current : 1.5A
+3.3V_RUN
Max Current : 2.24A
+3.3V_SUS
Max Current : 0.13A
+1.5V_RUN
Max Current : 0.5A
RT8510GQW
PU1
PR2 has been changed to 3.92K at ST build
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Load Switch/LED_BL_Converter
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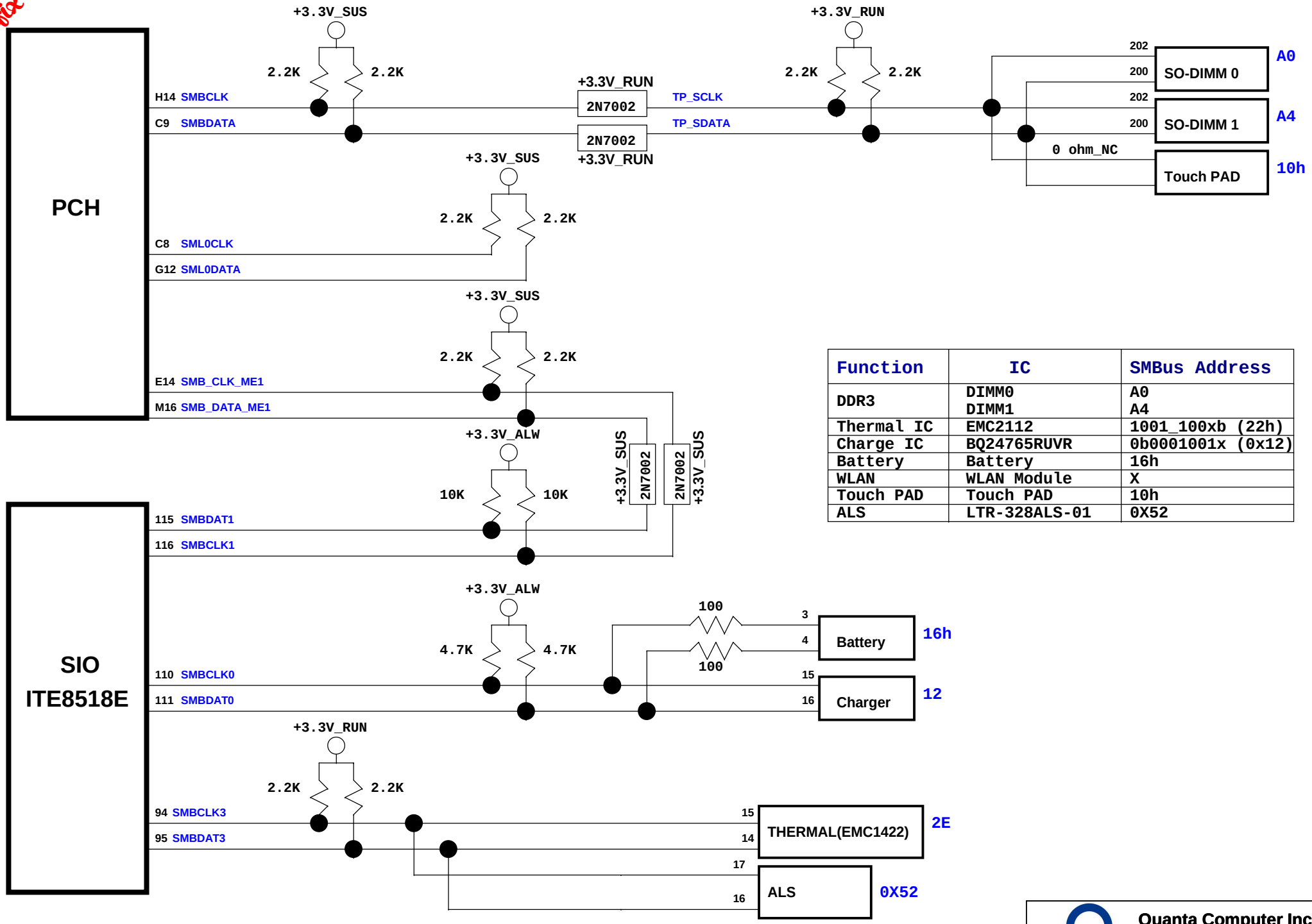


| Function | IC | SMBus Address |
|---|---|---|
| DDR3 | DIMM0<br>DIMM1 | A0<br>A4 |
| Thermal IC | EMC2112 | 1001_100xb (22h) |
| Charge IC | BQ24765RUVR | 0b0001001x (0x12) |
| Battery | Battery | 16h |
| WLAN | WLAN Module | X |
| Touch PAD | Touch PAD | 10h |
| ALS | LTR-328ALS-01 | 0X52 |

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| Size | Document Number | Rev |
|---|---|---|
| | SMBUS | 1A |

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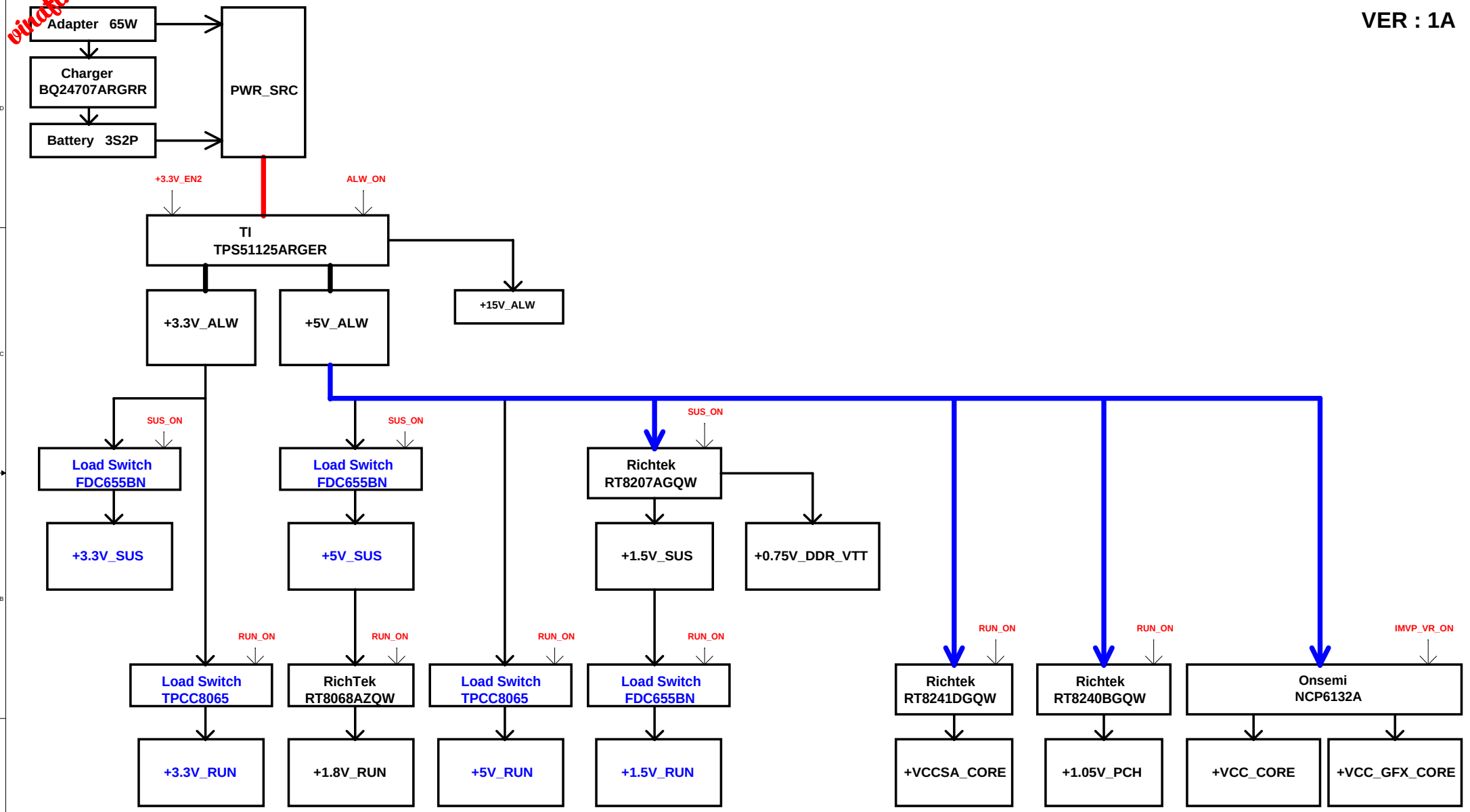
VER : 1A

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| Size | Document Number | Rev |
|---|---|---|
| | Power Block Diagram | 1A |

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