MS-1688 Ver : 20
Park XT

Calpella Platform

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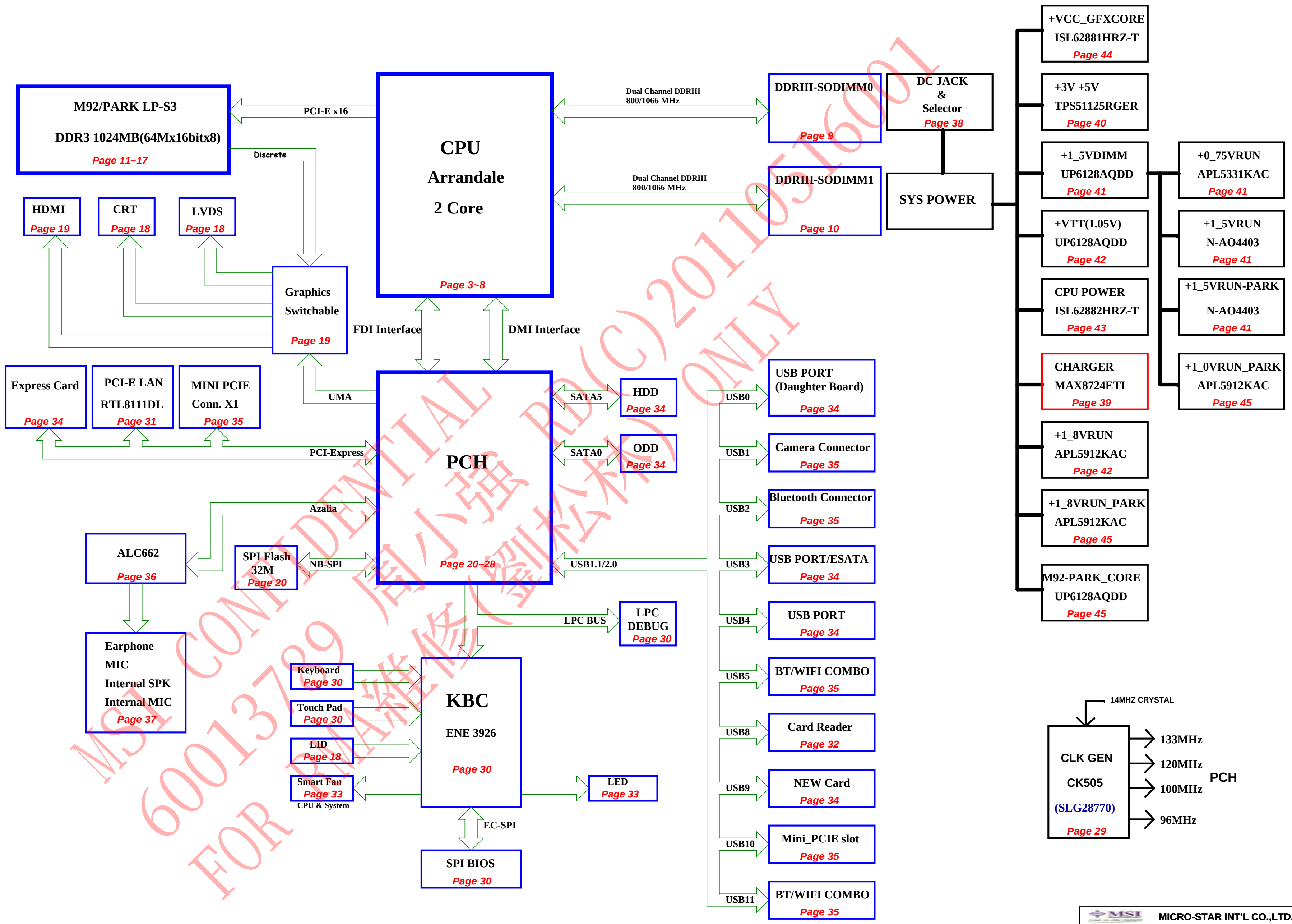

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CLK GEN
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120MHz
100MHz
96MHz
PCH

MICRO-STAR INT'L CO.,LTD.

Title	BLOCK DIAGRAM	
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	LAN
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	DDRIII core
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDRIII command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	Graphics core rail (Dual Core only)
M92S_VDD_CORE	0.95V	S0	GPU core power
+1_8VRUN_PARK	1.8V	S0	GPU PCIE power
+1_5VRUN_PARK	1.5V	S0	GPU DDR3 power
+1_0VRUN_PARK	1.0V	S0	GPU PCIE power
VDDR3	3.3V	S0	GPU I/O and DAC power

Net Naming Conventions

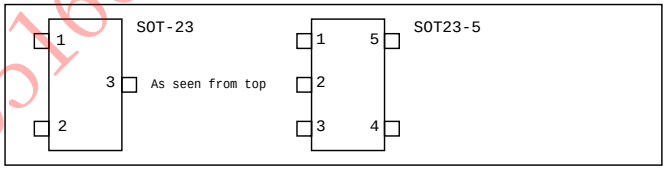
Suffix

\# = Active Low Signal

Prefix

H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

MICRO-STAR INT'L CO.,LTD.

Title: PLATFORM

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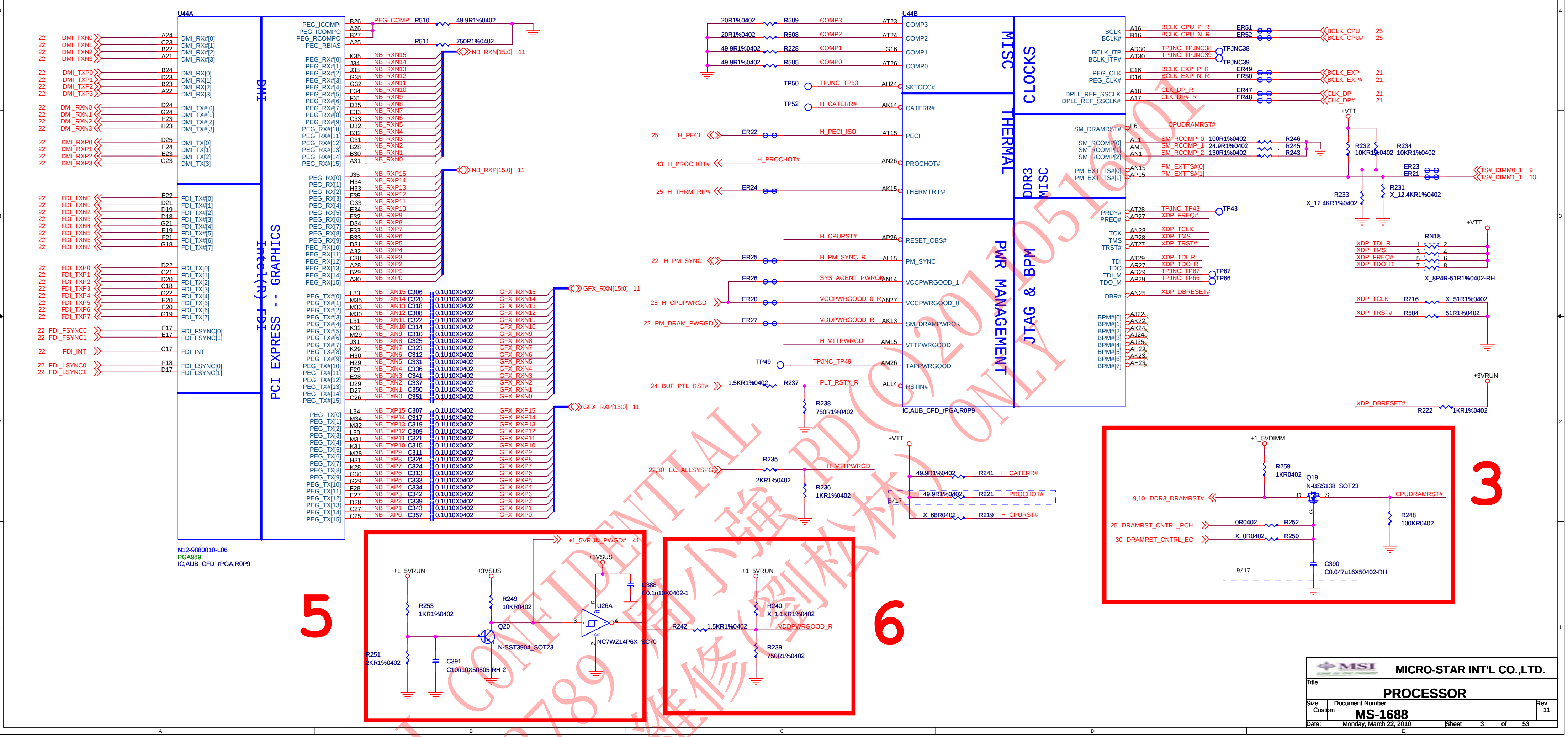
ARRANDALE PROCESSOR (CLK,MISC,JTAG)



MICRO-STAR INT'L CO.,LTD.

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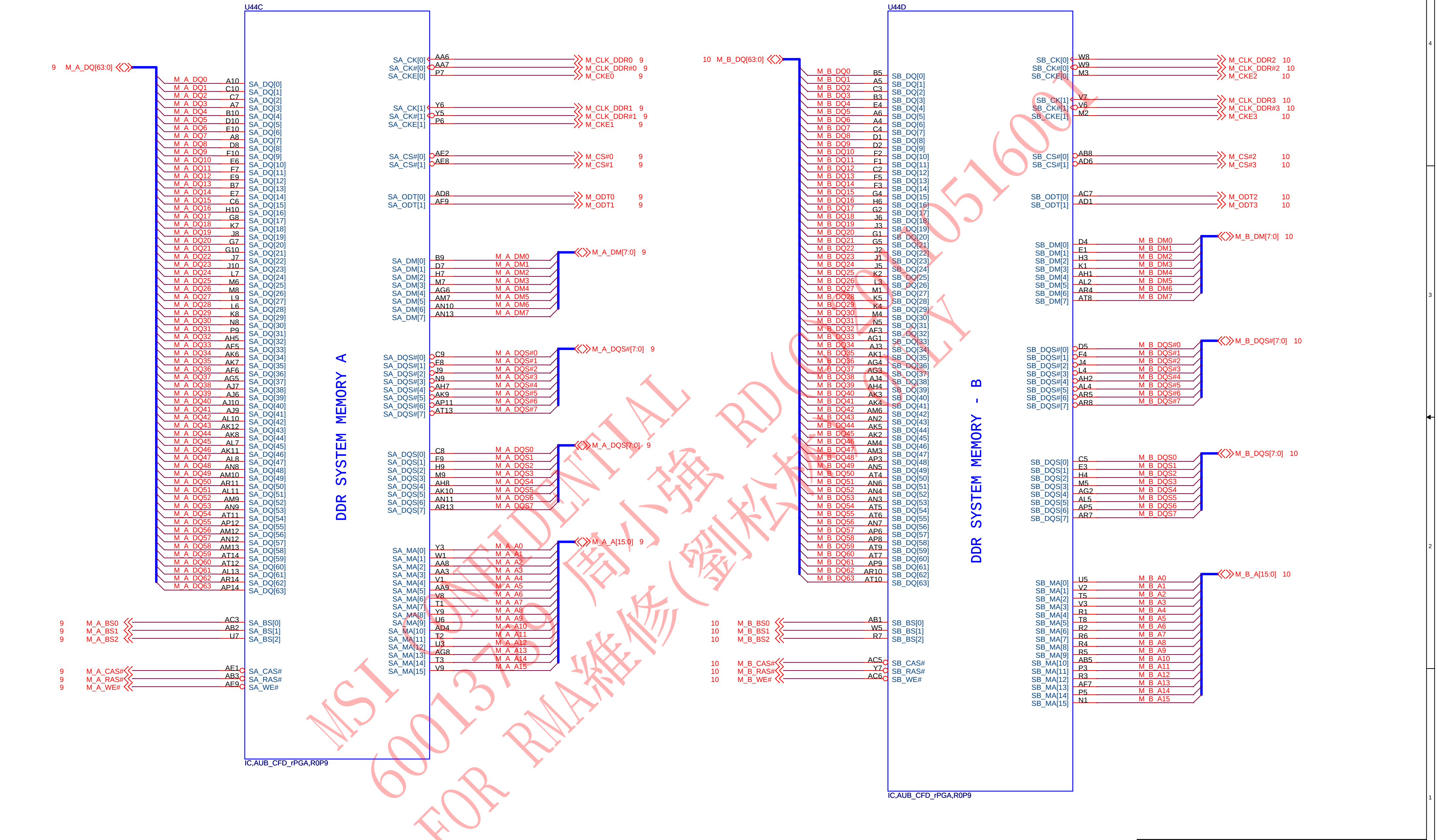
ARRANDALE PROCESSOR (DDR3)



MICRO-STAR INT'L CO.,LTD.

Title	DDR3	
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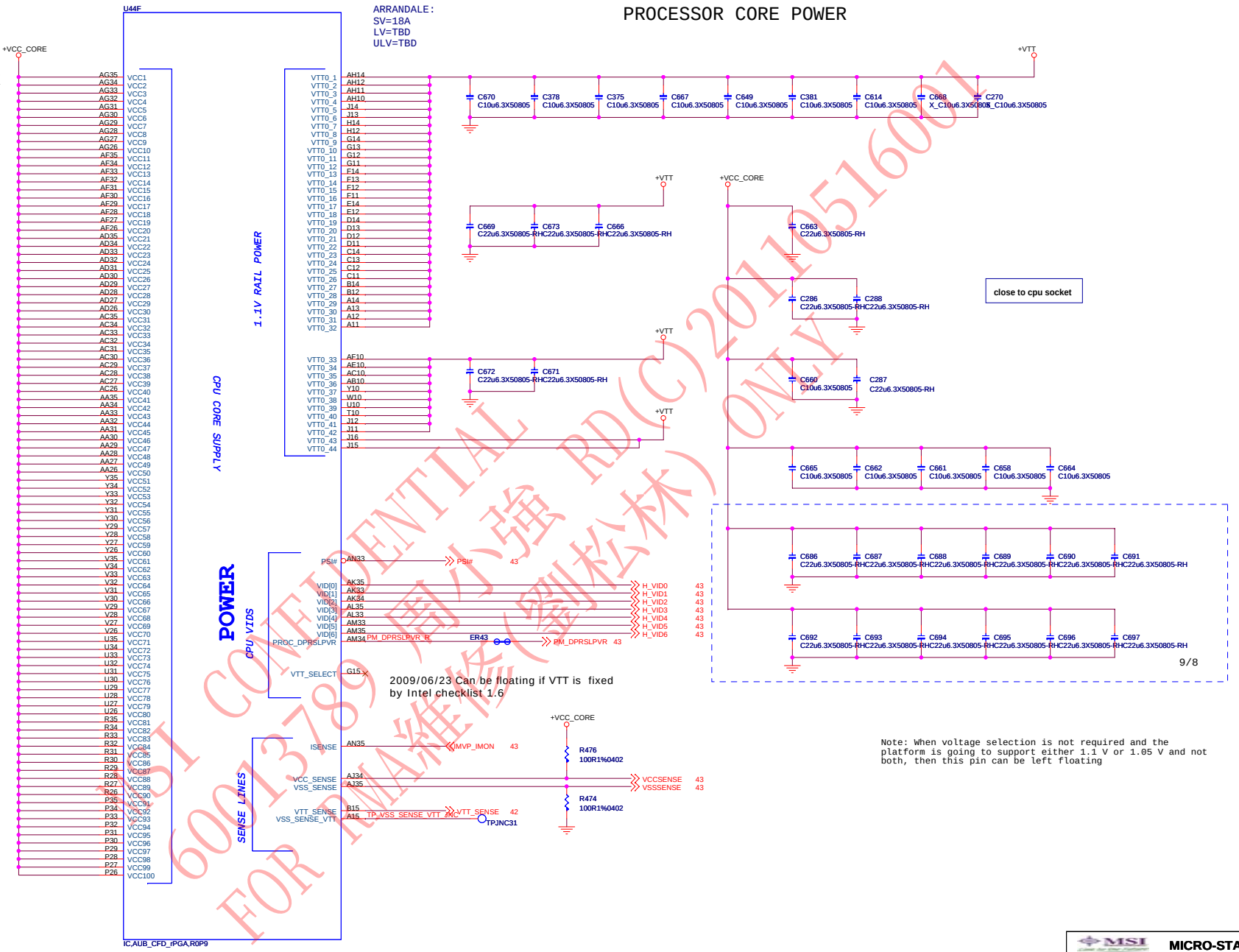
ARRANDALE PROCESSOR (POWER)

ARRANDALE:
SV=48A
LV=35A
ULV=27A

PROCESSOR CORE POWER

ARRANDALE:
SV=18A
LV=TBD
ULV=TBD

PROCESSOR CORE POWER



MSI MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR POWER

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ARRANDALE PROCESSOR (GRAPHICS POWER)

ARRANDALE:
SV=15A
LV=TBD
ULV=TBD

I=14A

+VCC_GFXCORE

C674 X_C22u6.3X50805-RH
C359 X_C22u6.3X50805-RH
C361 X_C22u6.3X50805-RH
C675 C10u6.3X50805
C656 C22u6.3X50805-RH
C655 C22u6.3X50805-RH
C373 C10u6.3X50805
C657 X_C10u6.3X50805

12/01 For DFM
12/01 For DFM

U44G

AT21 AT19 AT18 AT16 AR21 AR19 AR18 AR16 AP21 AP19 AP18 AP16 AN21 AN19 AN18 AN16 AM21 AM19 AM18 AM16 AL21 AL19 AL18 AL16 AK21 AK19 AK18 AK16 AJ21 AJ19 AJ18 AJ16 AH21 AH19 AH18 AH16

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36

GRAPHICS

SENSE LINES

VAXG_SENSE AR22
VSSAXG_SENSE AT22

VCC_AXG_SENSE 44
VSS_AXG_SENSE 44

GRAPHICS VIDs

GFX_VID[0] AM22
GFX_VID[1] AP22
GFX_VID[2] AN22
GFX_VID[3] AP23
GFX_VID[4] AM23
GFX_VID[5] AP24
GFX_VID[6] AN24

GFXVR_VID_0 44
GFXVR_VID_1 44
GFXVR_VID_2 44
GFXVR_VID_3 44
GFXVR_VID_4 44
GFXVR_VID_5 44
GFXVR_VID_6 44

PCB1.1

GFX_VR_EN AR25
GFX_DPRSLPVR AT25
GFX_IMON AM24

GFXVR_EN 44
GFXVR_DPRSLPVR 44
GFXVR_IMON 44

POWER

DDR3 - 1.5V RAILS

VDDQ1 AJ1
VDDQ2 AF1
VDDQ3 AE7
VDDQ4 AF4
VDDQ5 AC1
VDDQ6 AB7
VDDQ7 AB4
VDDQ8 Y1
VDDQ9 W7
VDDQ10 W4
VDDQ11 U1
VDDQ12 T7
VDDQ13 T4
VDDQ14 P1
VDDQ15 N7
VDDQ16 N4
VDDQ17 L1
VDDQ18 H1

ARRANDALE:
3A

+1_5VRUN

C385 C1u16X-RH
C384 C1u16X-RH
C382 C1u16X-RH
C377 C1u16X-RH
C380 C1u16X-RH
C386 C22u6.3X50805-RH
C383 C22u6.3X50805-RH
C389 C330u2.5pSO-1

+VTT

C363 C22u6.3X50805-RH
C364 C22u6.3X50805-RH

J24 J23 H25

VTT1_45 VTT1_46 VTT1_47

FDI

VTT0_59 P10
VTT0_60 N10
VTT0_61 L10
VTT0_62 K10

C362 C10u6.3X5-RH
C371 C10u6.3X5-RH

1.1V

VTT1_63 J22
VTT1_64 J20
VTT1_65 J18
VTT1_66 H21
VTT1_67 H20
VTT1_68 H19

C367 C22u6.3X50805-RH
C368 C22u6.3X50805-RH

PEG & DMI

1.8V

VCCPLL1 L26
VCCPLL2 L27
VCCPLL3 M26

+1_8VRUN

C345 C1u16X-RH
C346 C1u16X-RH
C347 C2.2u6.3X5
C348 C4.7u6.3X
C349 C22u6.3X50805-RH

ARRANDALE:
0.6A

+VTT

C360 C22u6.3X50805-RH
C376 C22u6.3X50805-RH
C659 C22u6.3X50805-RH
C652 C22u6.3X50805-RH

K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25

VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58

IC_AUB_CFD_rPGA_R0P9

1

MICRO-STAR INT'L CO.,LTD.

Title: GRAPHICS POWER

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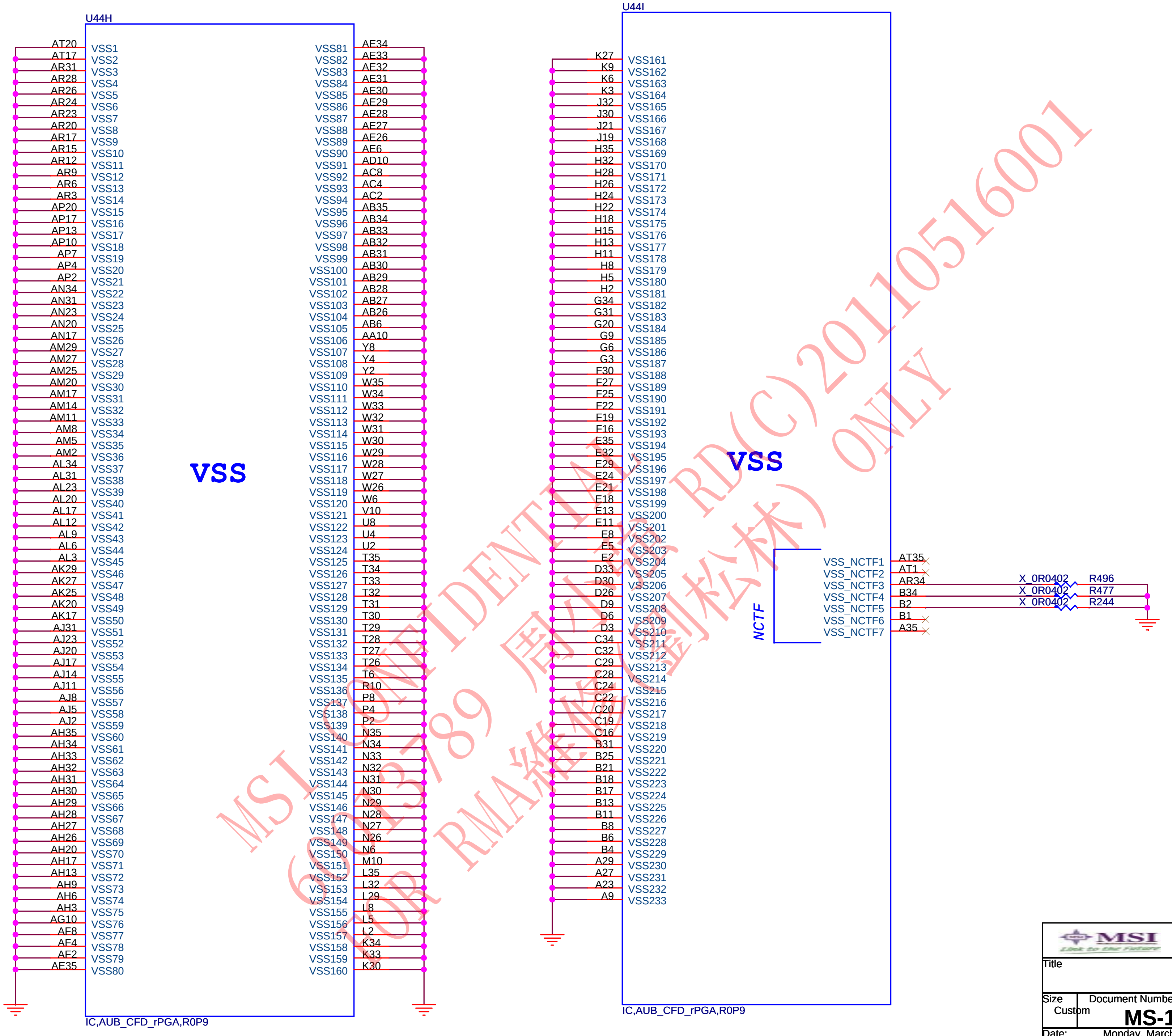
ARRANDALE PROCESSOR (GND)



MICRO-STAR INT'L CO.,LTD.

Title	PROCESSOR GND	
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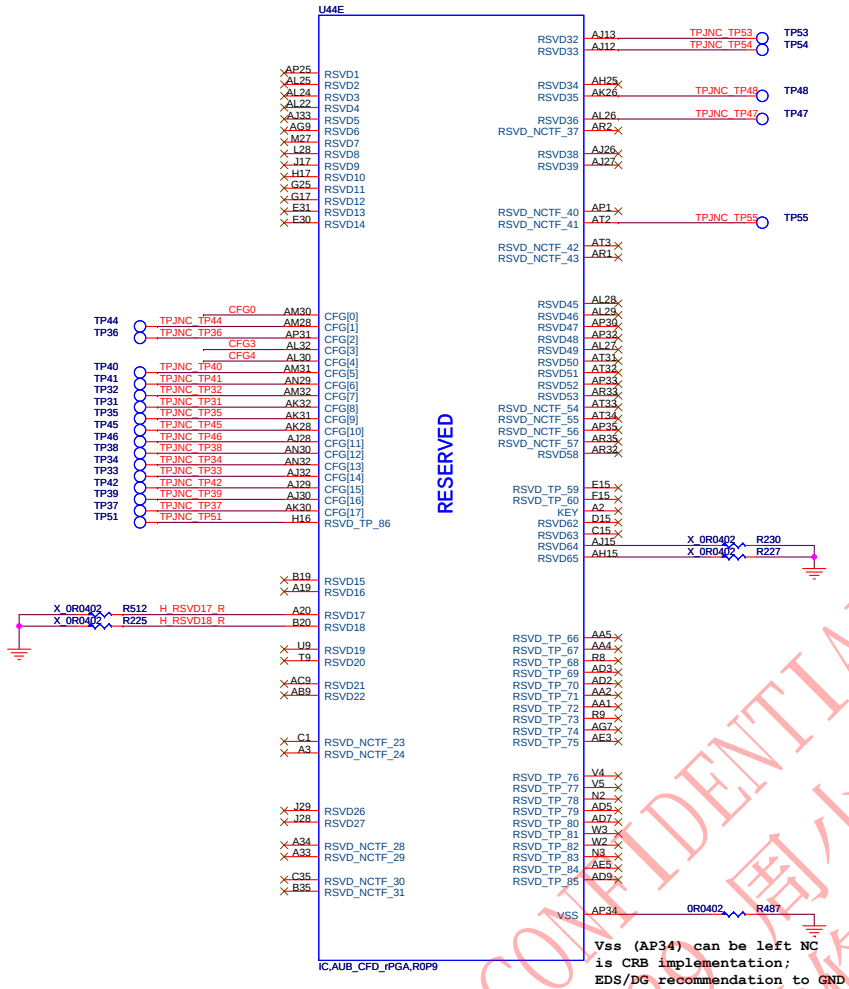
ARRANDALE PROCESSOR (RESERVED)



Vss (AP34) can be left NC
is CRB implementation;
EDS/DG recommendation to GND

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG0
NO_STUFF
R212
X_3.01KR1%0402

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG3
STUFF
R213
3.01KR1%0402

CFG[3] – PCI Express* Static Lane Numbering Reversal. Lane Reversal will be applied across all 16 Lanes.
- 1: No lane reversal
- 0: Reversal

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG4
NO_STUFF
R214
X_3.01KR1%0402

Layout Note:
Location of all CFG strap resistors needs to be close to trace to minimize stub

MICRO-STAR INT'L CO.,LTD.

Title: PROCESSOR RESERVED

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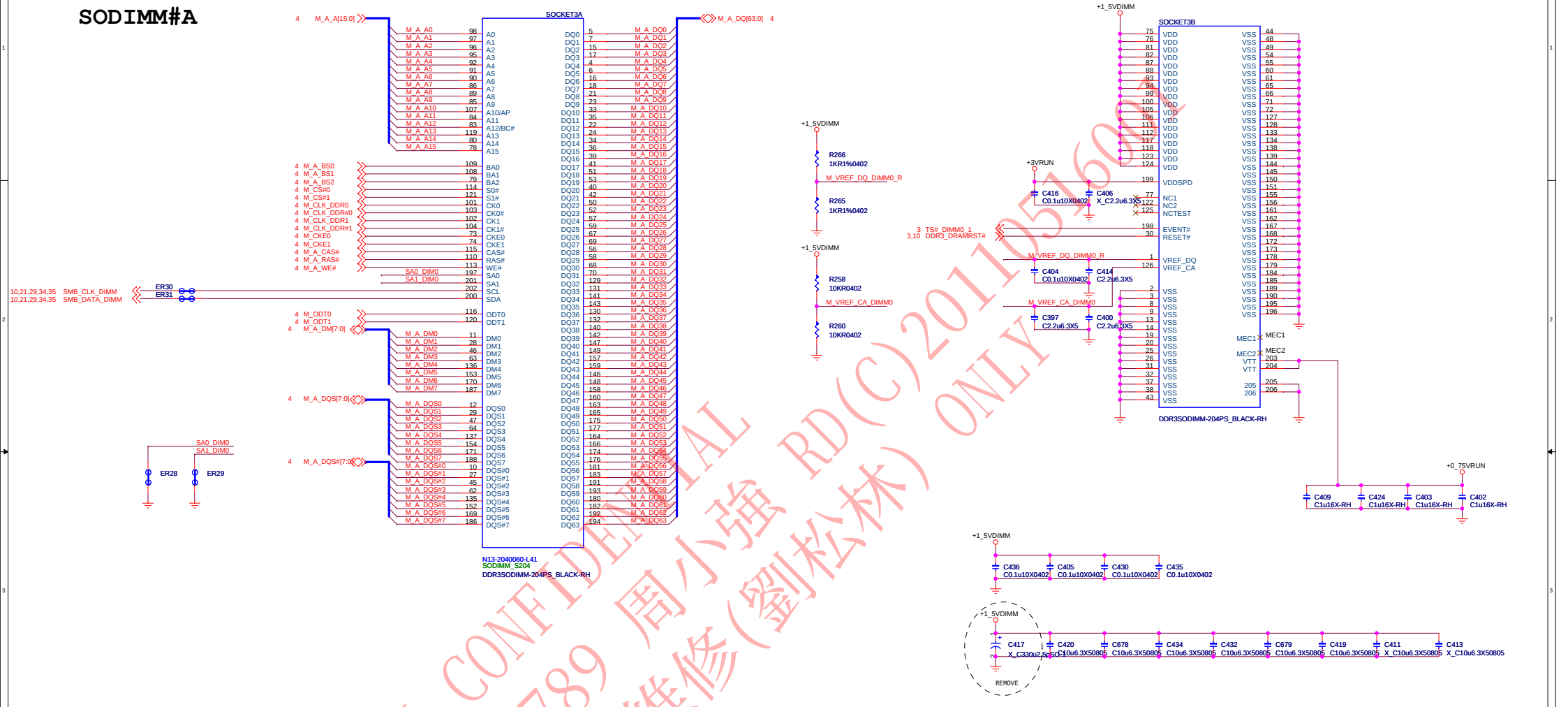
SODIMM#A



MICRO-STAR INT'L CO.,LTD.

Title: DDR3 SODIMM0

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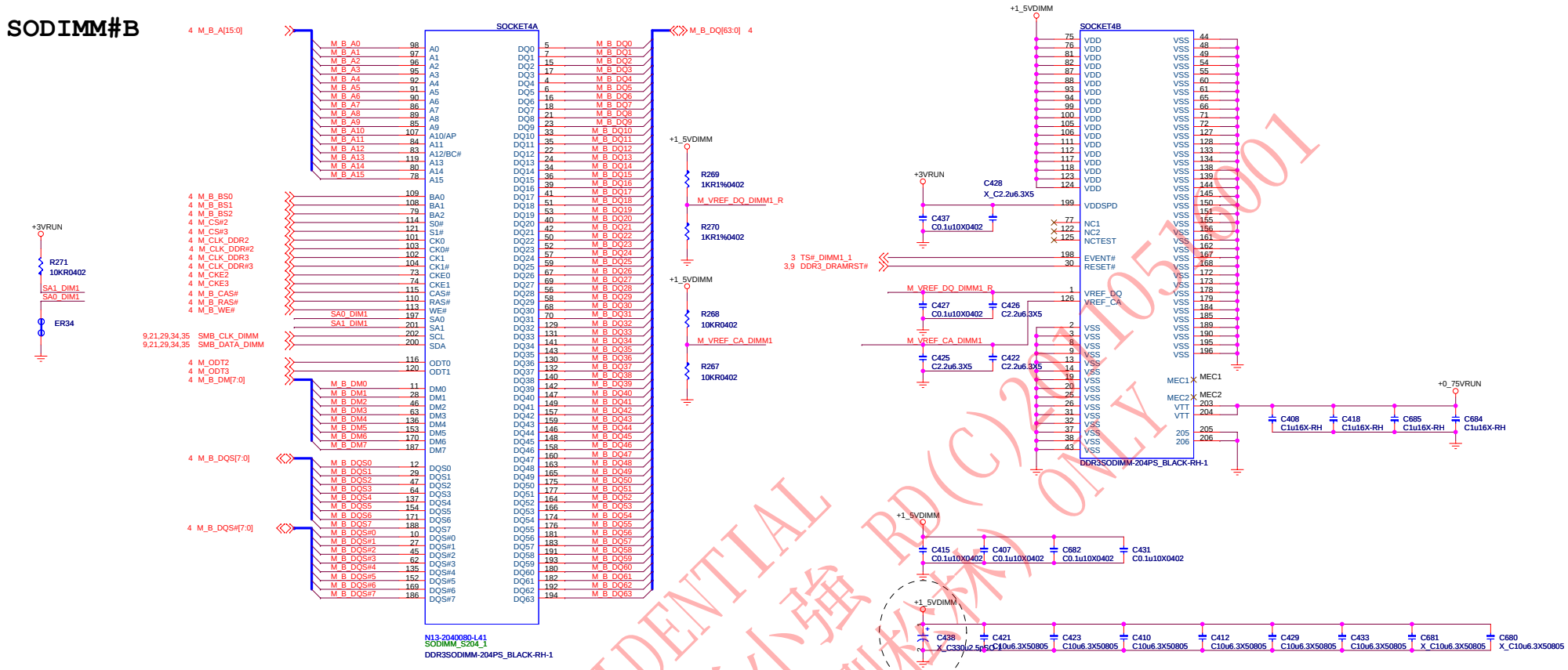
SODIMM#B



MICRO-STAR INT'L CO.,LTD.			
Title: DDR3 SODIMM1			
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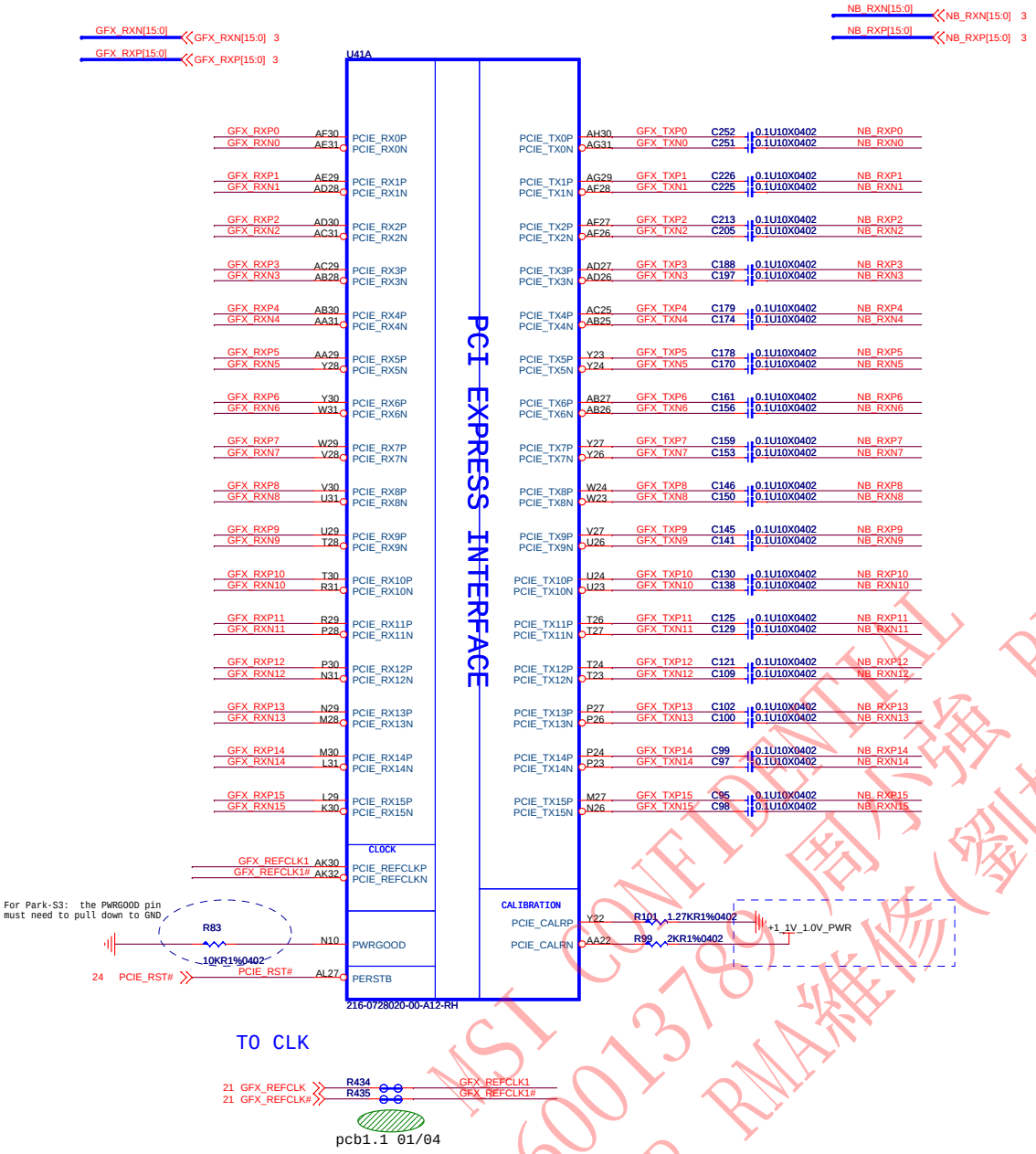

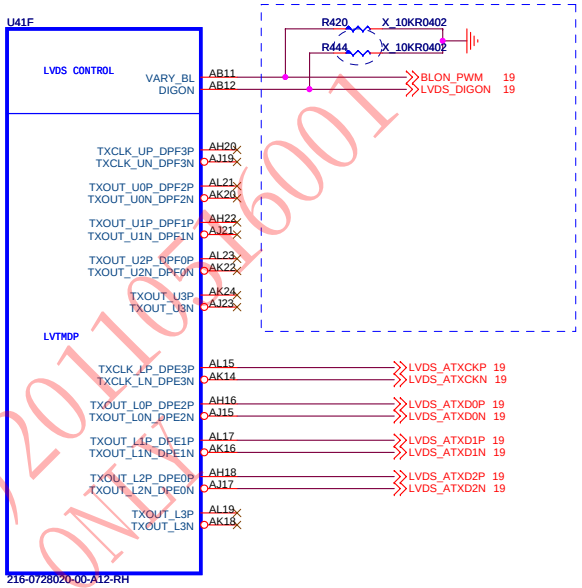

DisplayPort E Configuration

MSI CORPORATION			
Title: PARK-HOST/LVDS			
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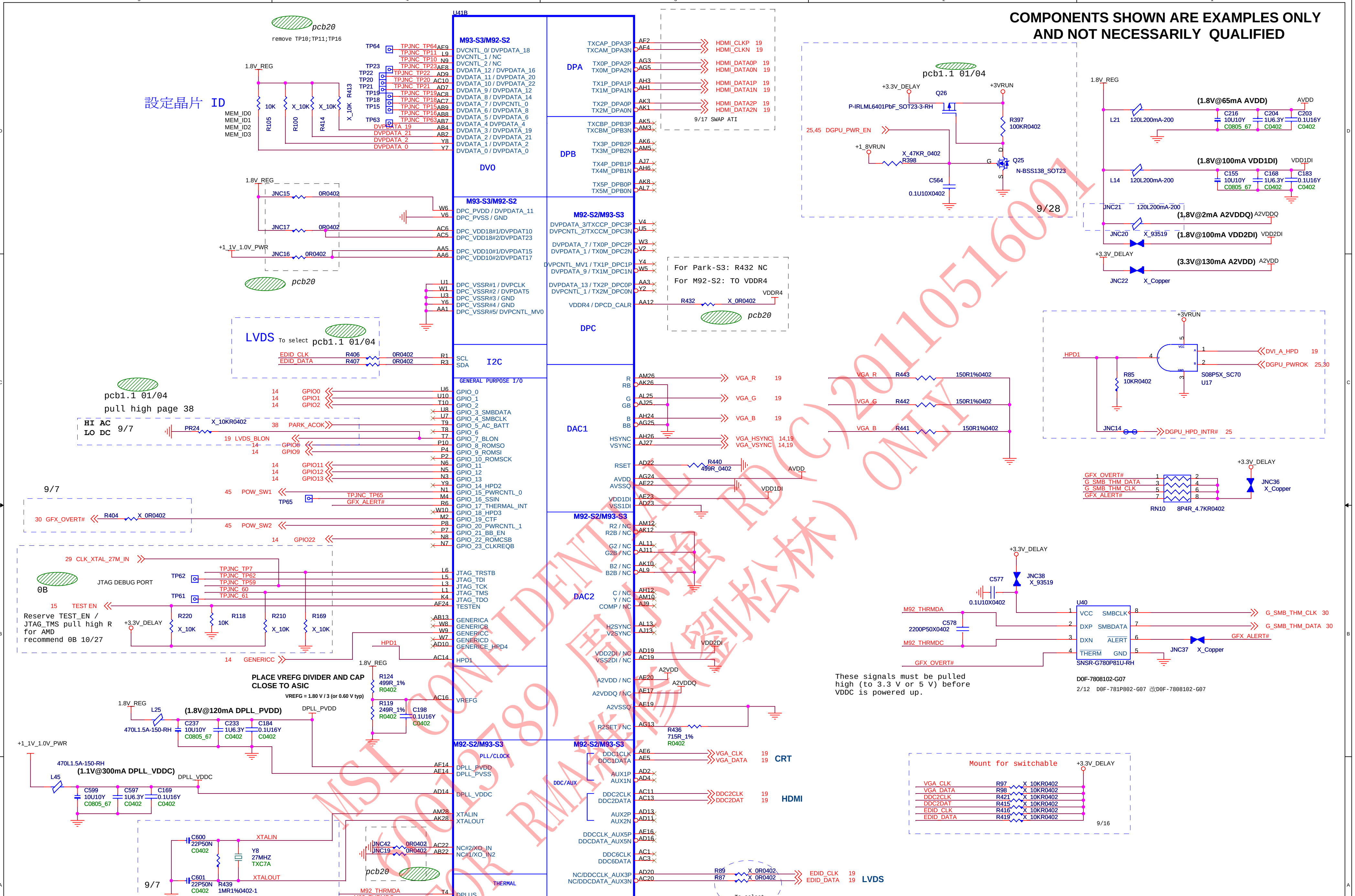

COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED
U41B
M93-S3/M92-S2
設定晶片 ID
MEM_ID0
MEM_ID1
MEM_ID2
MEM_ID3
remove TP10;TP11;TP16
pcb20
DVO
DPA
DPB
DPC
9/17 SWAP ATI
For Park-S3: R432 NC
For M92-S2: TO VDDR4
LVDS To select pcb1.1 01/04
I2C
GENERAL PURPOSE I/O
pcb1.1 01/04
pull high page 38
HI AC
LO DC 9/7
JTAG DEBUG PORT
Reserve TEST_EN /
JTAG_TMS pull high R
for AMD
recommend 0B 10/27
PLACE VREFG DIVIDER AND CAP
CLOSE TO ASIC
VREFG = 1.80 V / 3 (or 0.60 V typ)
(1.8V@120mA DPLL_PVDD)
(1.1V@300mA DPLL_VDDC)
For Park-S3: XO_IN and XO_IN2 can be use as 3.3V CLK Input. These poins can be grounded if not in use.
(1.8V@20mA TSVDD)
<New PN>
DAC1
DAC2
CRT
HDMI
LVDS
To select
THERMAL
pcb1.1 01/04
9/28
(1.8V@65mA AVDD)
(1.8V@100mA VDD1DI)
(1.8V@2mA A2VDDQ)
(1.8V@100mA VDD2DI)
(3.3V@130mA A2VDD)
These signals must be pulled high (to 3.3 V or 5 V) before VDDC is powered up.
SNSR-G780P81U-RH
D0F-7808102-G07
2/12 D0F-781P802-G07 改D0F-7808102-G07
Mount for switchable
9/16
216-0728020-00-A12-RH

DV DATA	3	2	1	0	
Hynix	0	0	0	0	64*16
SAMSUNG	0	0	0	1	64*16

M12-5TQ1G25-H23

M12-K4W1G85-S02

E34/M0

MSI CORPORATION

Title: PARK-IO

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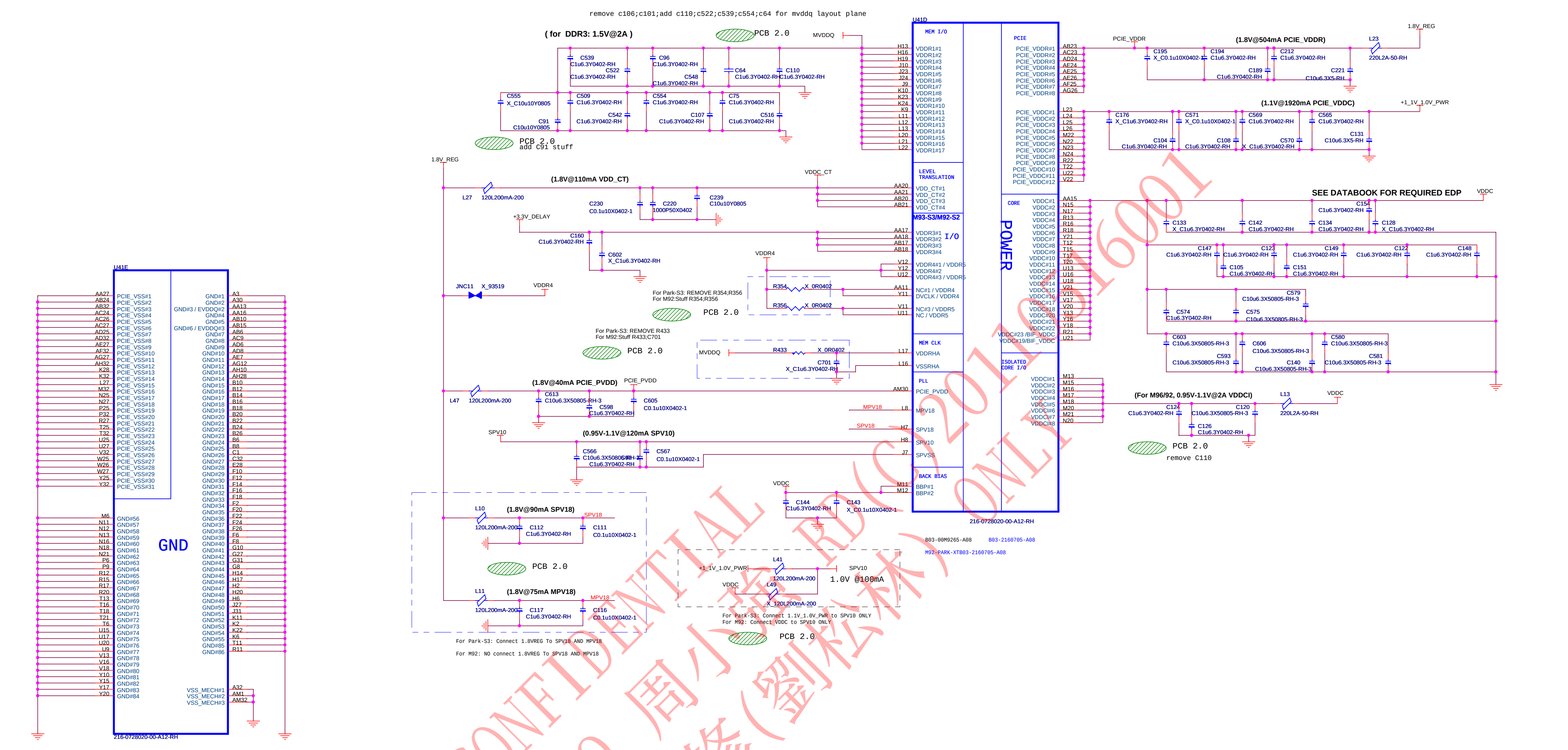

remove c106;c101;add c110;c522;c539;c554;c64 for mvddq layout plane
(for DDR3: 1.5V@2A)
PCB 2.0
MVDDQ
PCB 2.0
add C91 stuff
1.8V_REG
(1.8V@110mA VDD_CT)
VDDC_CT
L27 120L200mA-200
+3.3V_DELAY
VDDR4
For Park-S3: REMOVE R354;R356
For M92:Stuff R354;R356
PCB 2.0
For Park-S3: REMOVE R433
For M92:Stuff R433;C701
PCB 2.0
JNC11 X_93519
(1.8V@40mA PCIE_PVDD)
PCIE_PVDD
L47 120L200mA-200
SPV10
(0.95V-1.1V@120mA SPV10)
(1.8V@90mA SPV18)
(1.8V@75mA MPV18)
PCB 2.0
For Park-S3: Connect 1.8VREG To SPV18 AND MPV18
For M92: NO connect 1.8VREG To SPV18 AND MPV18
+1_1V_1.0V_PWR
SPV10
1.0V @100mA
For Park-S3: Connect 1.1V_1.0V_PWR to SPV10 ONLY
For M92: Connect VDDC to SPV10 ONLY
PCB 2.0
U41D
MEM I/O
LEVEL TRANSLATION
M93-S3/M92-S2
I/O
MEM CLK
PLL
BACK BIAS
PCIE
CORE
ISOLATED CORE I/O
POWER
216-0728020-00-A12-RH
B03-00M9265-A08
B03-2160705-A08
M92-PARK-XTB03-2160705-A08
PCIE_VDDR
(1.8V@504mA PCIE_VDDR)
1.8V_REG
L23 220L2A-50-RH
(1.1V@1920mA PCIE_VDDC)
+1_1V_1.0V_PWR
SEE DATABOOK FOR REQUIRED EDP
VDDC
(For M96/92, 0.95V-1.1V@2A VDDCI)
L13 220L2A-50-RH
PCB 2.0
remove C110
U41E
GND
216-0728020-00-A12-RH

E69/M0

MSI CORPORATION

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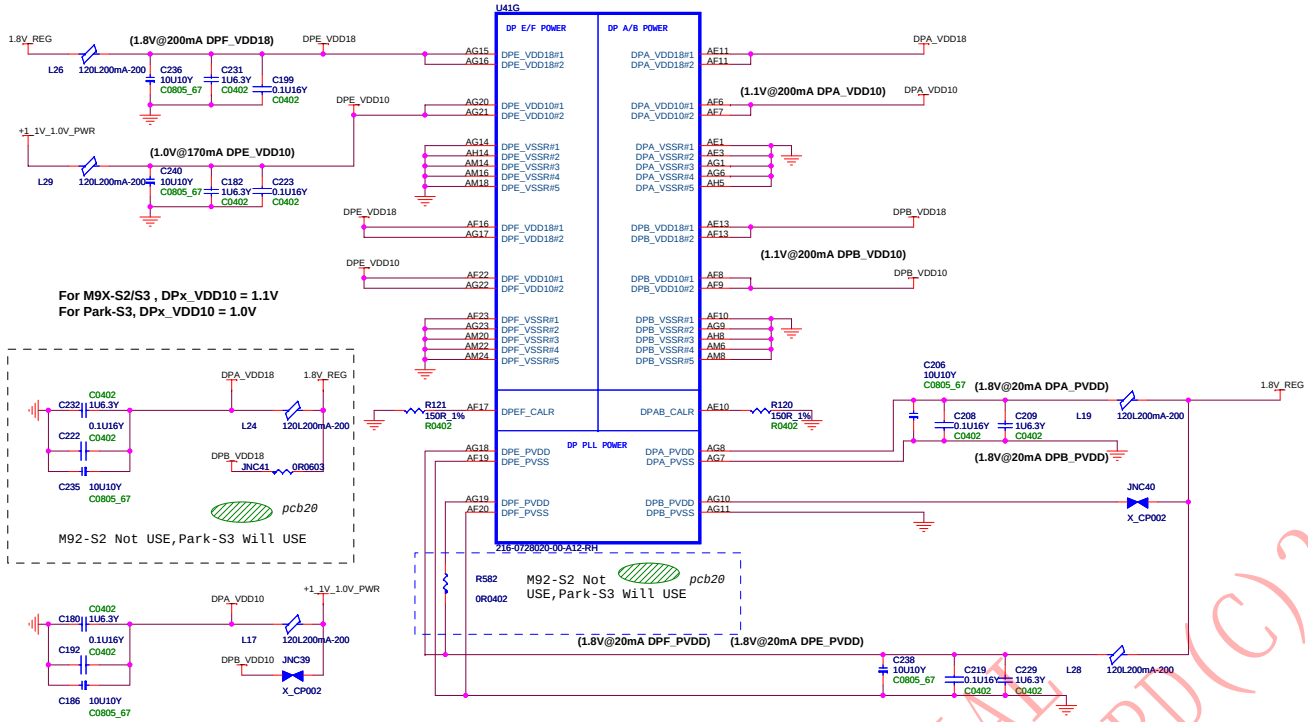

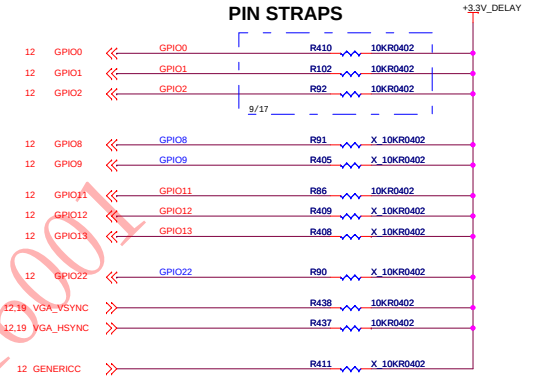

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 X X

GPIO 13 12 11

Size of the primary memory apertures	CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
512 MB 1G MB	001

Due to memory management constraints, the aperture size should be the same size as the frame buffer for 64 MB, 128 MB
and 256 MB. For frame buffers larger than 256 MB (e.g. 512 MB, 1 GB) the aperture size should be 256 MB.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

E23/M0

MSI CORPORATION

Title: **PARK-power straps**

Size: Custom | Document Number: **MS-1688** | Rev: 11

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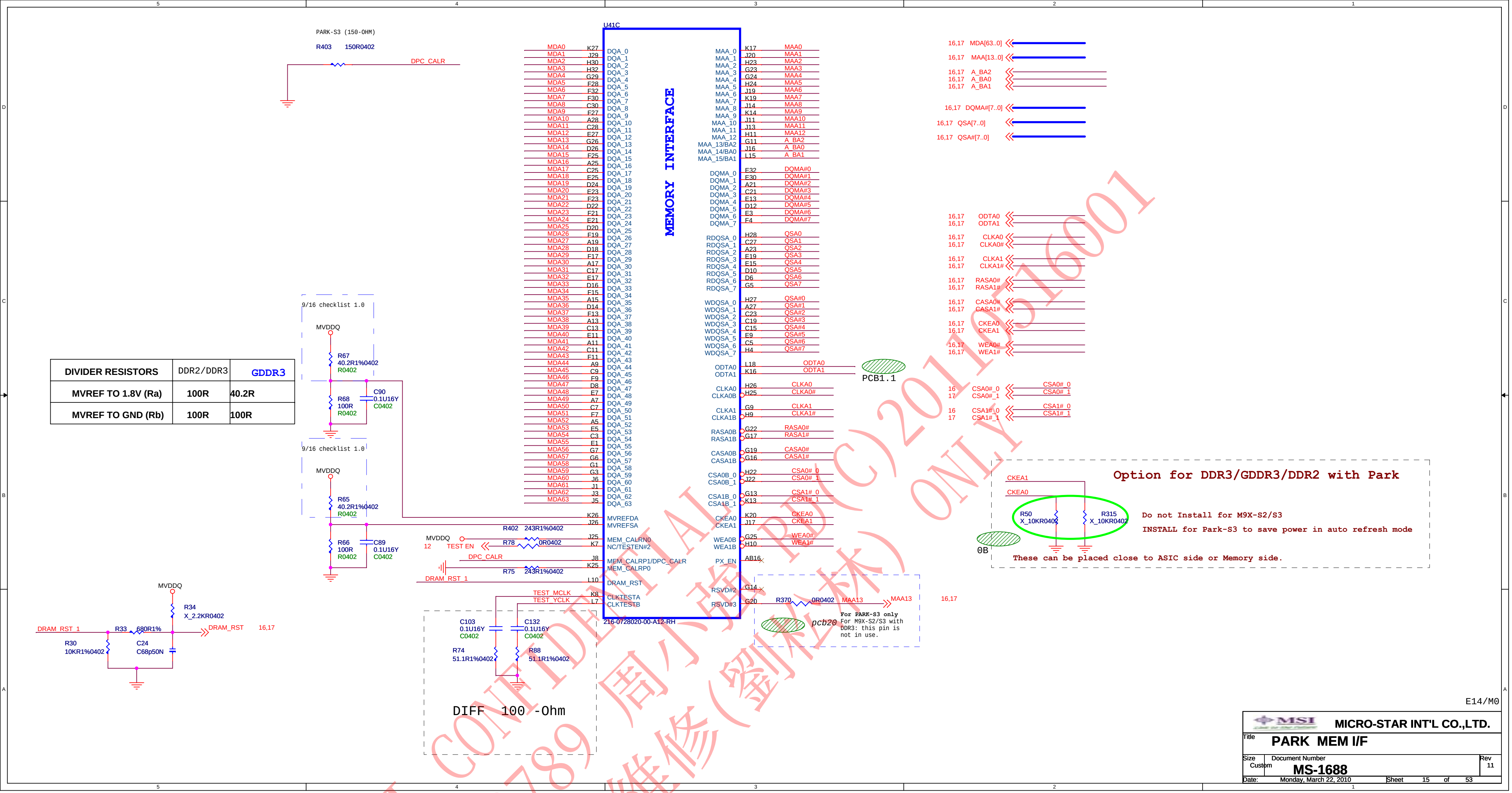


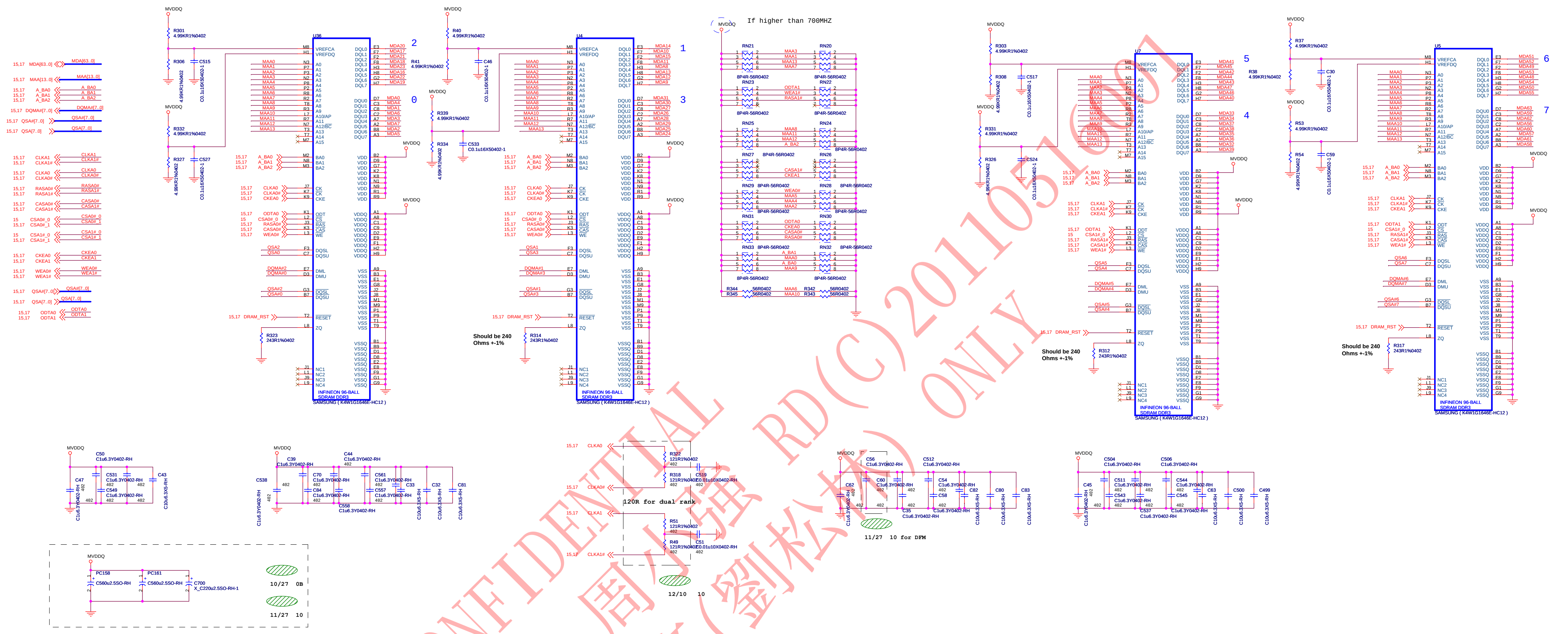
DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R

MICRO-STAR INT'L CO.,LTD.

Title: PARK MEM I/F

Size: Custom | Document Number: MS-1688 | Rev: 11

Date: Monday, March 22, 2010 | Sheet 15 of 53



MICRO-STAR INT'L CO.,LTD.

Title	PARK MEM DDR3 A0
Size: Custom	Document Number: MS-1688
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Date:	Monday, March 22, 2010
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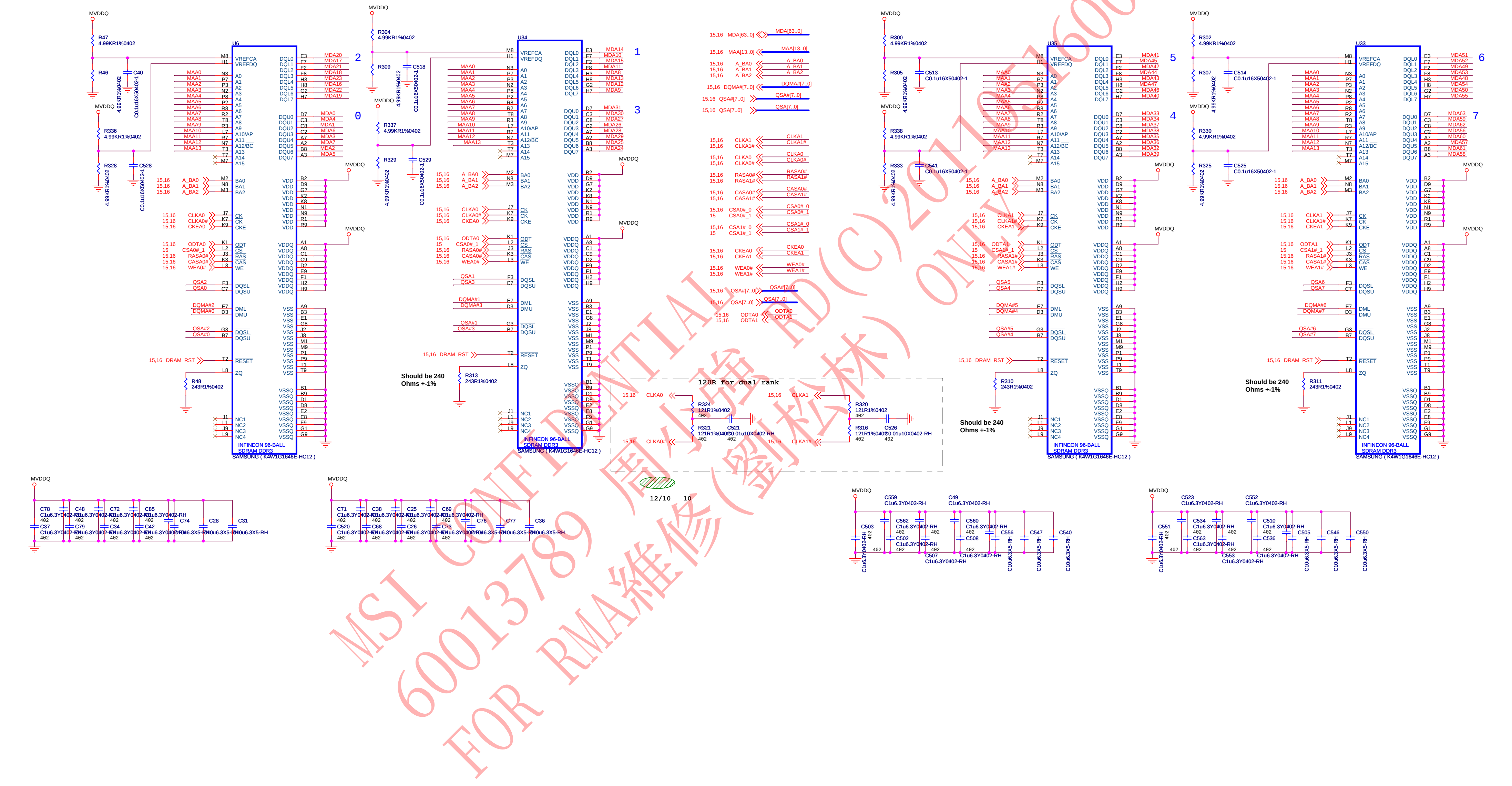
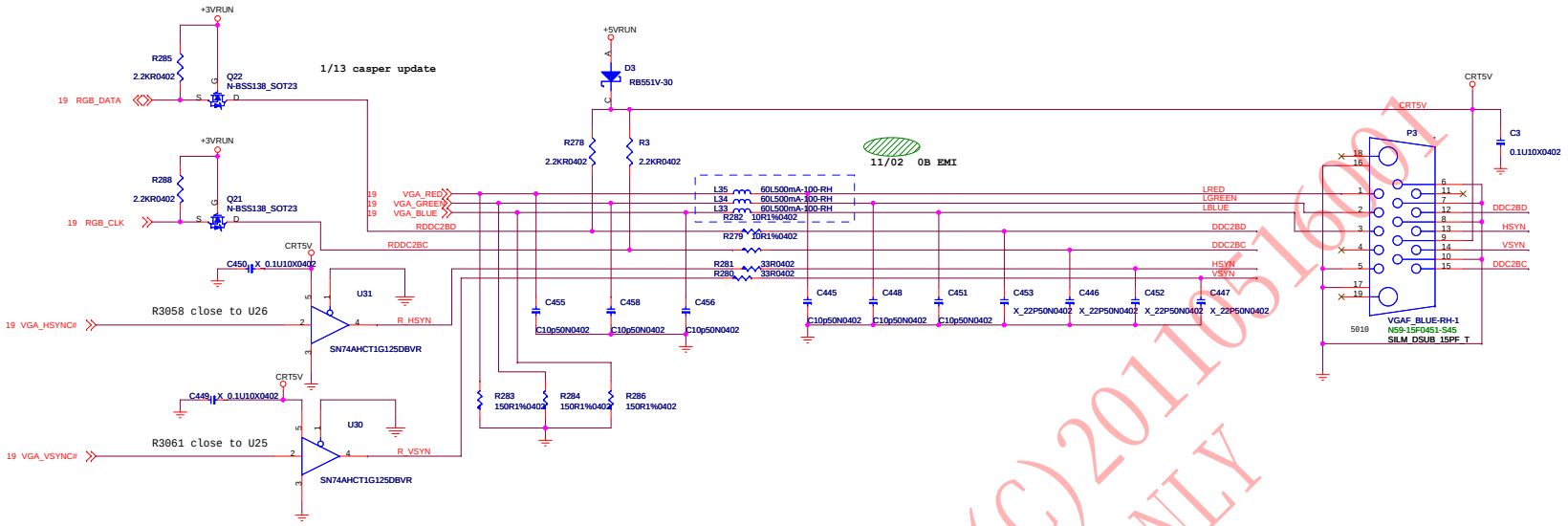


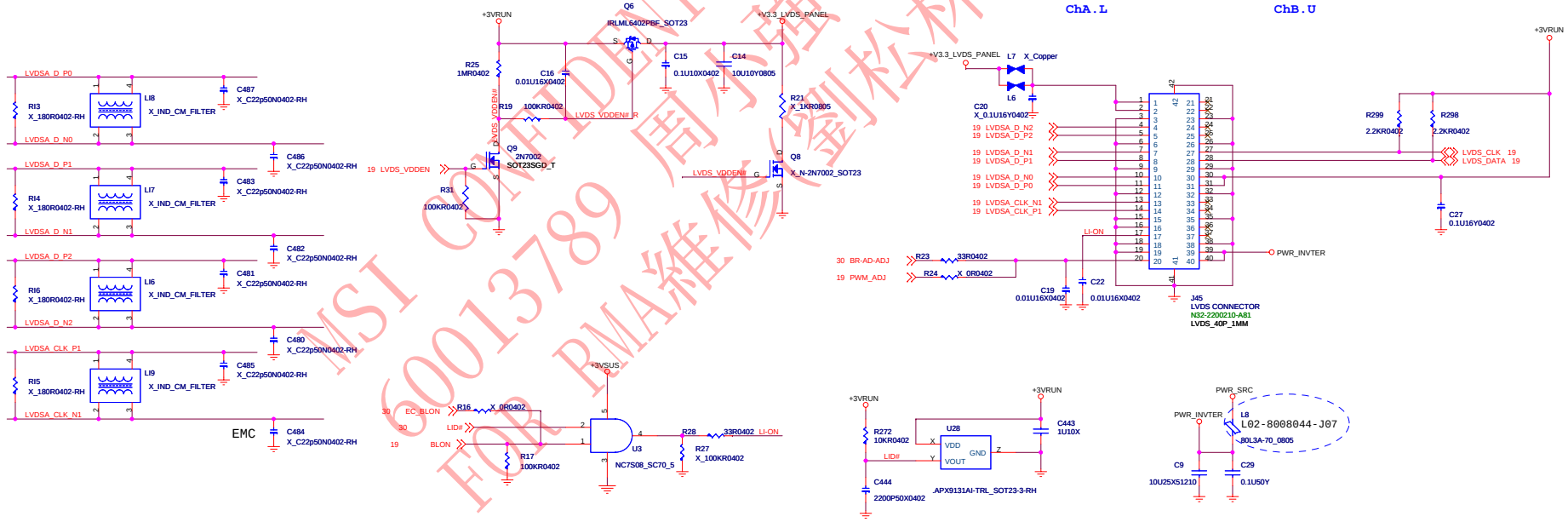
MICRO-STAR INT'L CO.,LTD.

Title: PARK MEM DDR3 A1

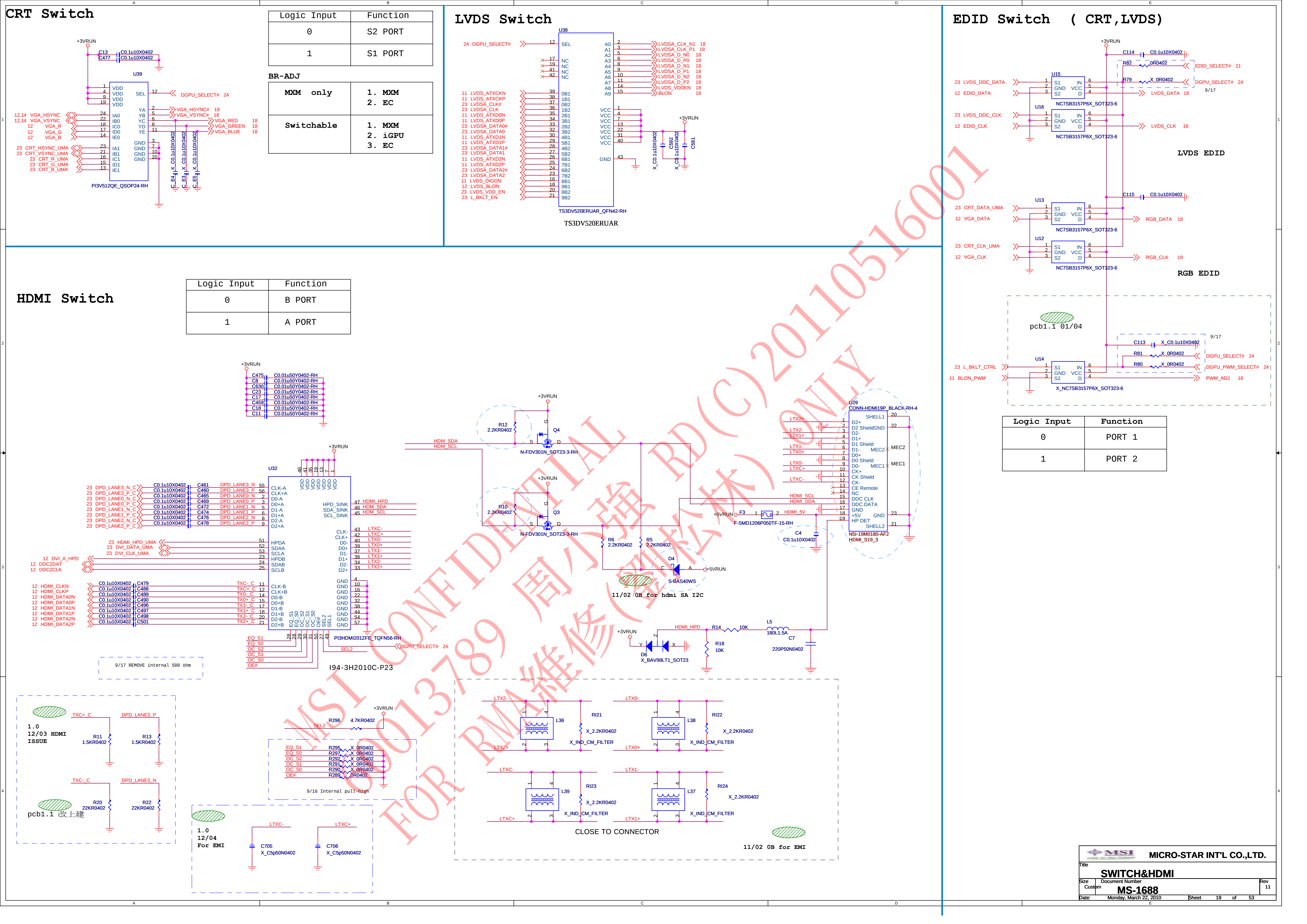
Size: Custom | Document Number: MS-1688 | Rev: 11

Date: Monday, March 22, 2010 | Sheet 17 of 53





MSI	MICRO-STAR INT'L CO.,LTD.		
Title	CRT,LVDS connector & LID		
Size: Custom	Document Number: MS-1688	Rev: 11	
Date: Monday, March 22, 2010	Sheet 18 of 53		



CRT Switch

Logic Input	Function
0	S2 PORT
1	S1 PORT

BR-ADJ

MXM only	1. MXM 2. EC
Switchable	1. MXM 2. iGPU 3. EC

HDMI Switch

Logic Input	Function
0	B PORT
1	A PORT

EDID Switch (CRT,LVDS)

Logic Input	Function
0	PORT 1
1	PORT 2

MICRO-STAR INT'L CO.,LTD.

Title	SWITCH&HDMI	
Size: Custom	Document Number: MS-1688	Rev: 11
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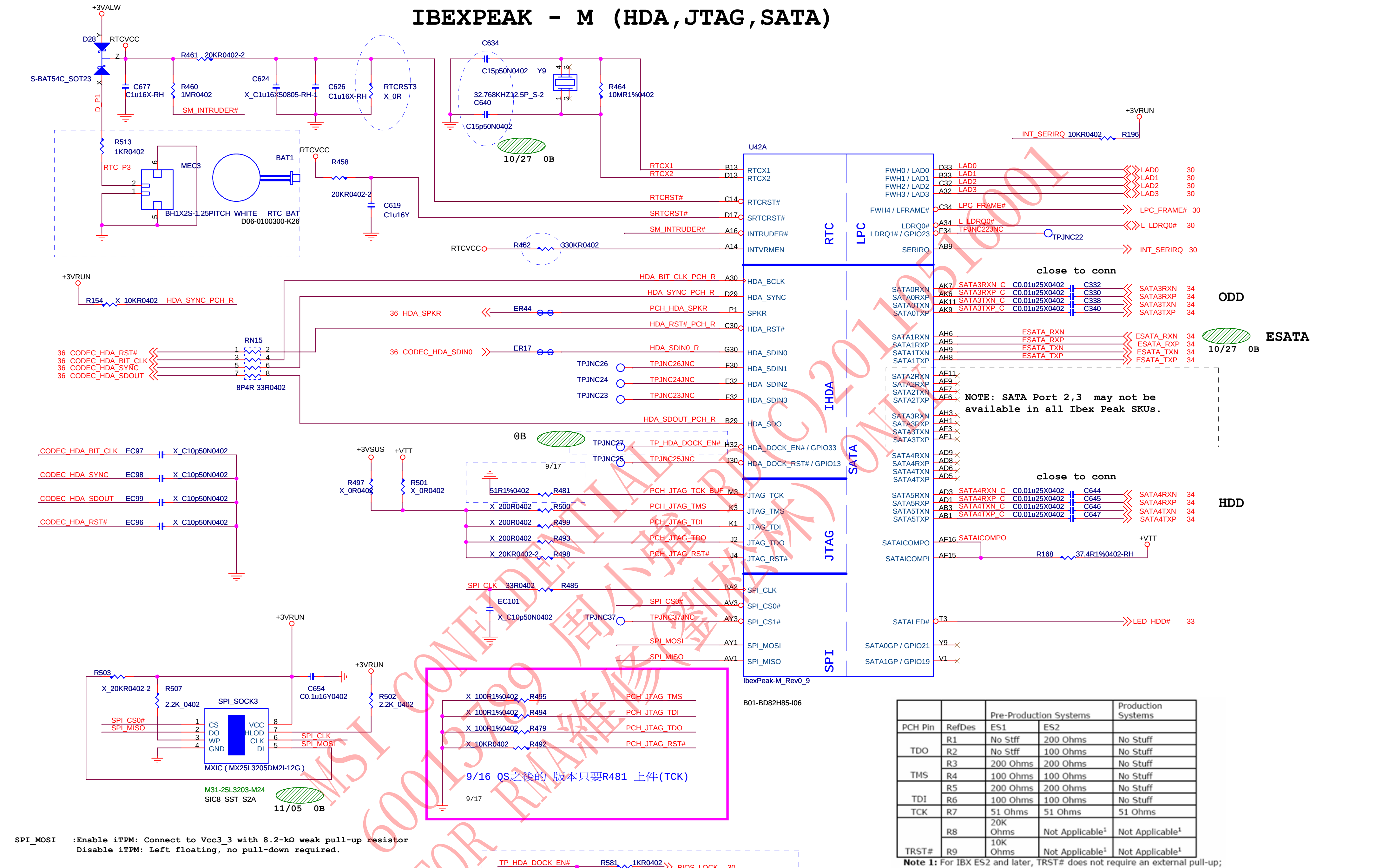
IBEXPEAK - M (HDA,JTAG,SATA)



SPI_MOSI :Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor
Disable iTPM: Left floating, no pull-down required.

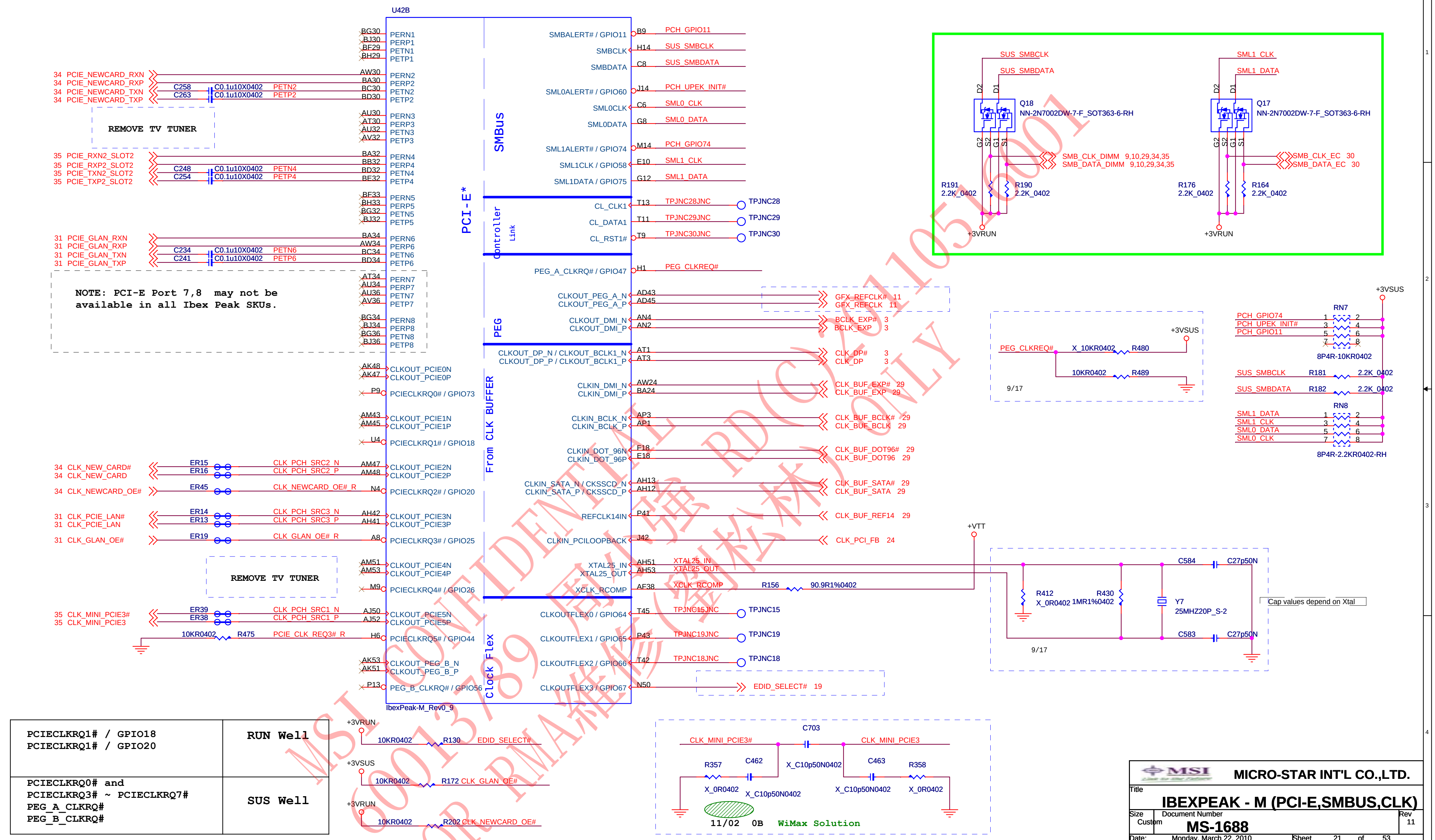
PCH Pin	RefDes	Pre-Production Systems ES1	ES2	Production Systems
TDO	R1	No Stff	200 Ohms	No Stuff
	R2	No Stff	100 Ohms	No Stuff
TMS	R3	200 Ohms	200 Ohms	No Stuff
	R4	100 Ohms	100 Ohms	No Stuff
TDI	R5	200 Ohms	200 Ohms	No Stuff
	R6	100 Ohms	100 Ohms	No Stuff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
TRST#	R8	20K Ohms	Not Applicable[1]	Not Applicable[1]
	R9	10K Ohms	Not Applicable[1]	Not Applicable[1]

Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test pad for PCH JTAG debug purposes

MICRO-STAR INT'L CO.,LTD.

Title	IBEXPEAK - M (HDA,JTAG,SATA)	
Size: Custom	Document Number: MS-1688	Rev: 11
Date: Monday, March 22, 2010	Sheet 20 of 53	

IBEXPEAK - M (PCI-E,SMBUS,CLK)

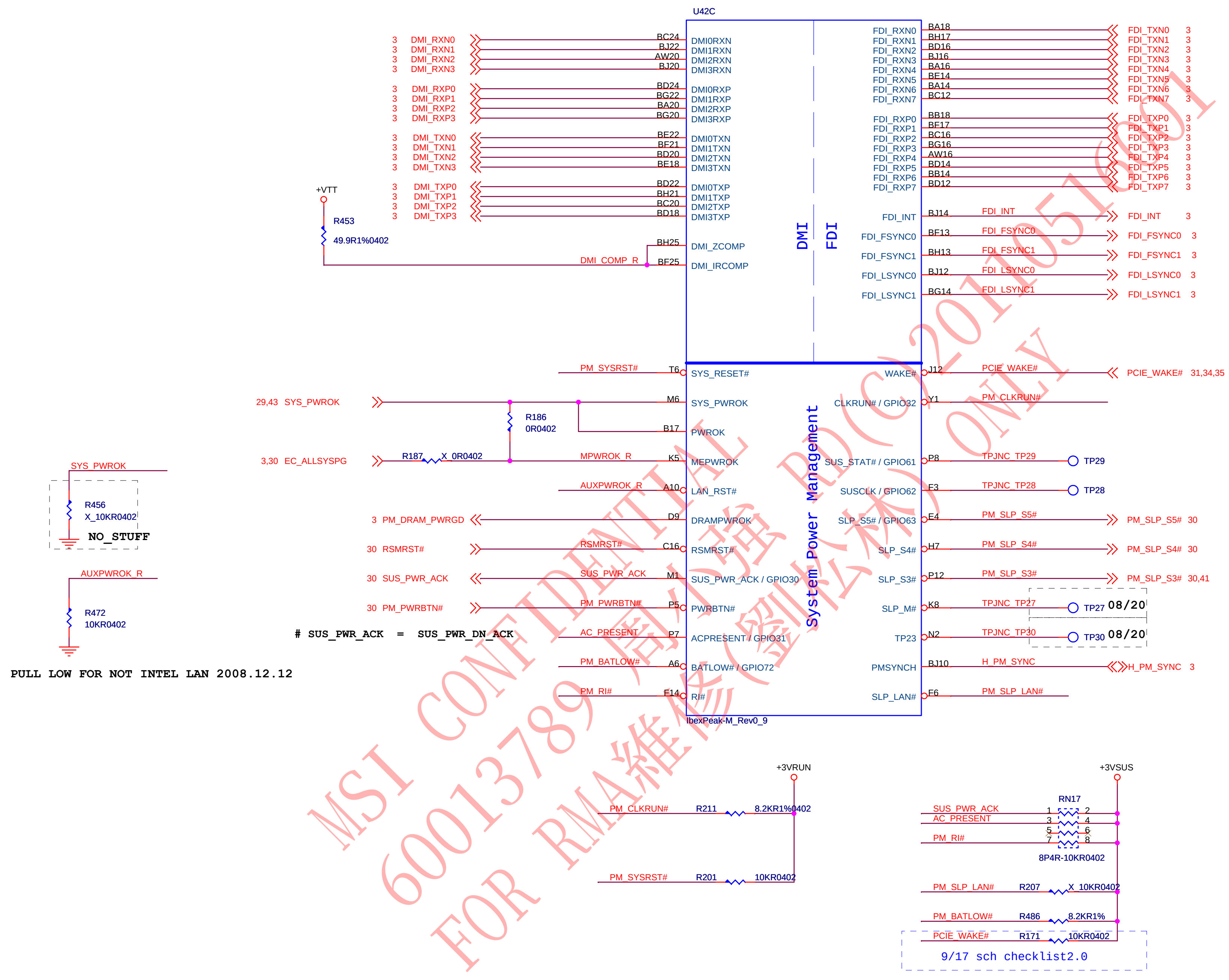


PCIECLKRQ1# / GPIO18 PCIECLKRQ1# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# PEG_B_CLKRQ#	SUS Well

MICRO-STAR INT'L CO.,LTD.

Title	IBEXPEAK - M (PCI-E,SMBUS,CLK)		
Size: Custom	Document Number: MS-1688		Rev: 11
Date: Monday, March 22, 2010		Sheet 21 of 53	

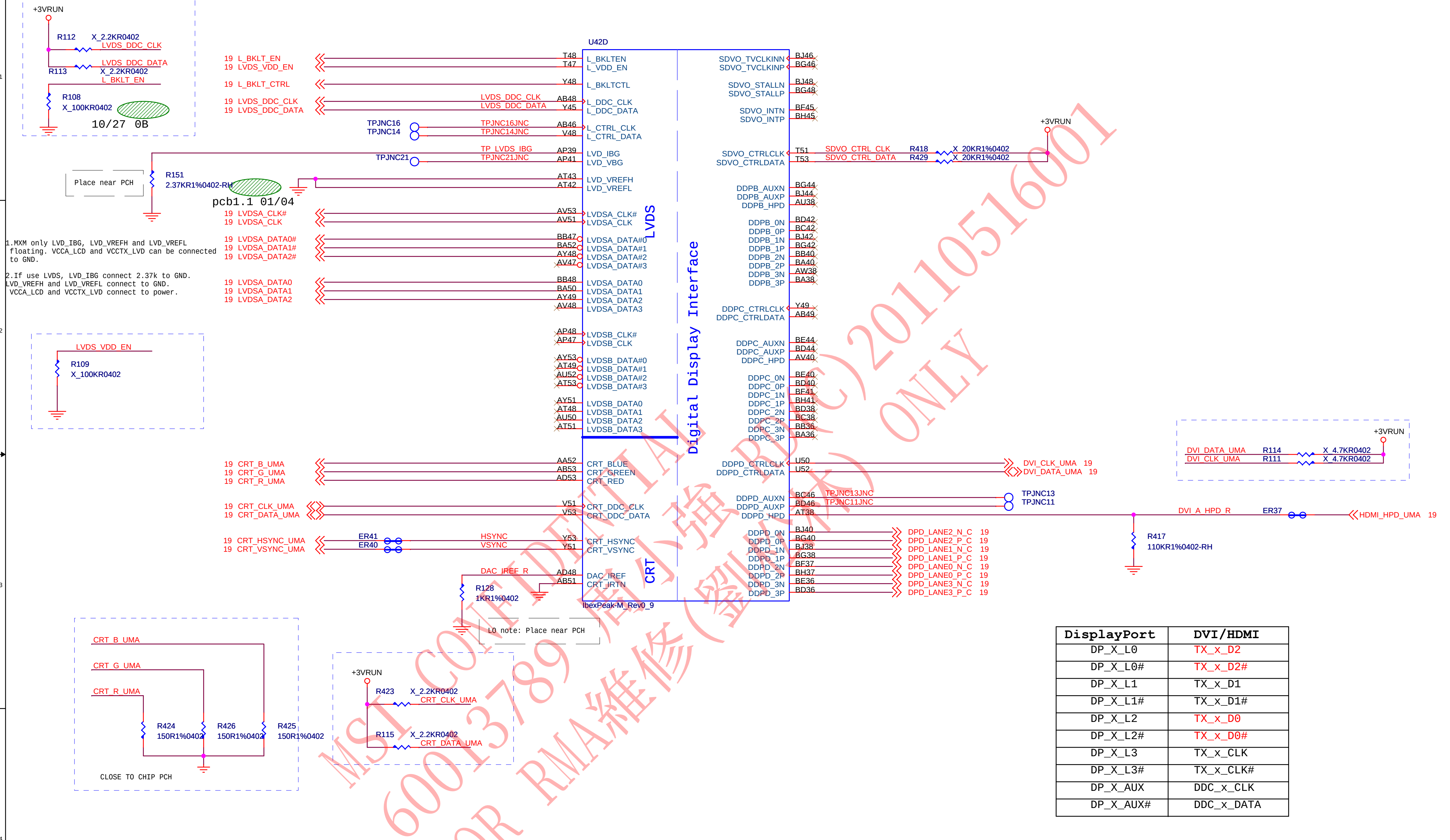
IBEXPEAK - M (DMI,FDI,GPIO)



MSI MICRO-STAR INT'L CO.,LTD.

Title	IBEXPEAK - M (DMI,FDI,GPIO)	
Size: Custom	Document Number: MS-1688	Rev: 11
Date: Monday, March 22, 2010	Sheet 22 of 53	

IBEXPEAK - M (LVDS,DDI)



DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

MSI MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (LVDS,DDI)

Size: Custom | Document Number: MS-1688 | Rev: 11

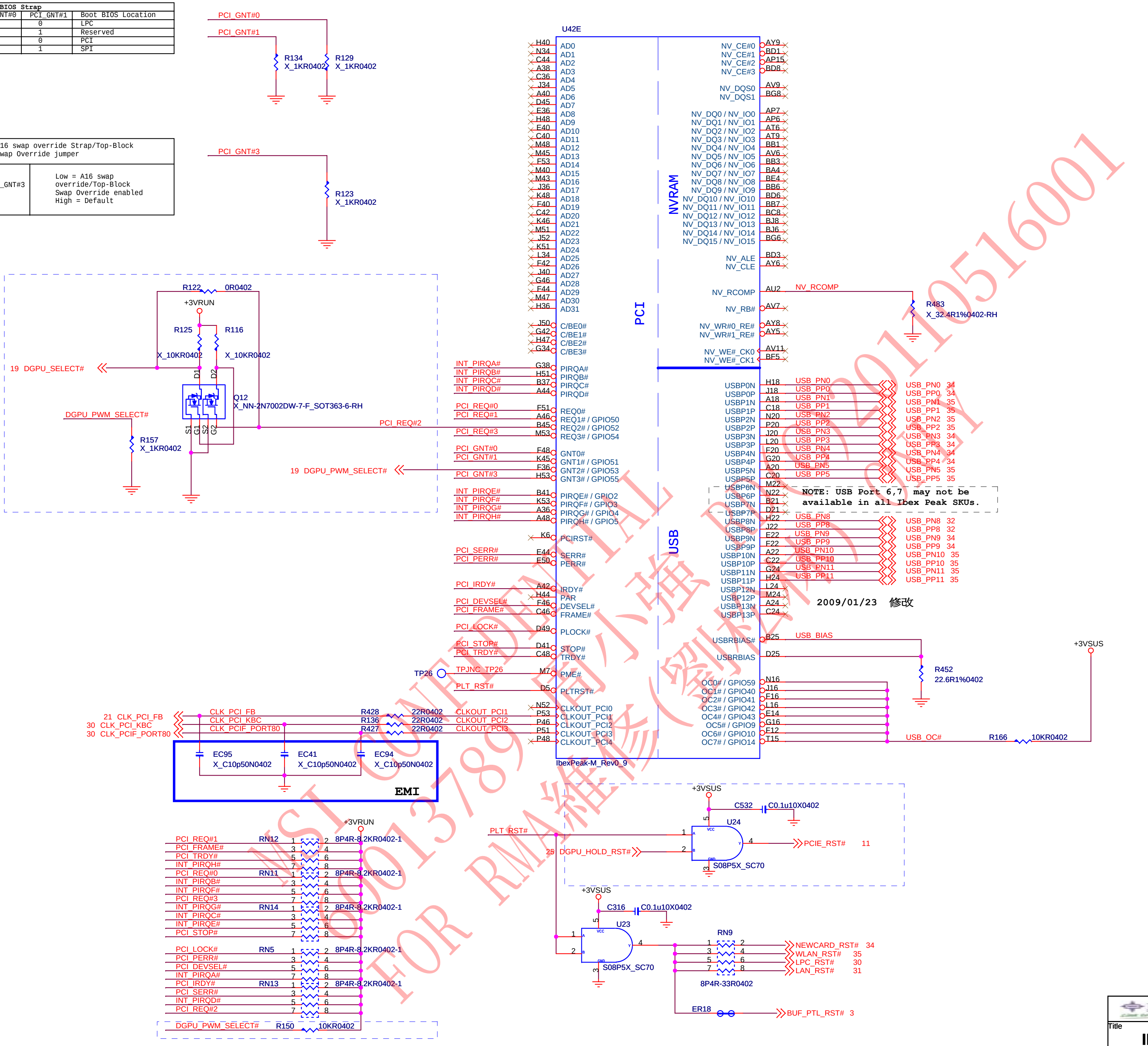
Date: Monday, March 22, 2010 | Sheet 23 of 53

IBEXPEAK - M (PCI,USB,NVRAM)

Boot BIOS Strap

PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



U42E
IbexPeak-M_Rev0_9
PCI
NVRAM
USB
AD0 … AD31
C/BE0# C/BE1# C/BE2# C/BE3#
PIRQA# PIRQB# PIRQC# PIRQD#
REQ0# REQ1# / GPIO50 REQ2# / GPIO52 REQ3# / GPIO54
GNT0# GNT1# / GPIO51 GNT2# / GPIO53 GNT3# / GPIO55
PIRQE# / GPIO2 PIRQF# / GPIO3 PIRQG# / GPIO4 PIRQH# / GPIO5
PCIRST#
SERR# PERR#
IRDY# PAR DEVSEL# FRAME#
PLOCK#
STOP# TRDY#
PME#
PLTRST#
CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4
NV_CE#0 NV_CE#1 NV_CE#2 NV_CE#3
NV_DQS0 NV_DQS1
NV_DQ0 / NV_IO0 … NV_DQ15 / NV_IO15
NV_ALE NV_CLE
NV_RCOMP
NV_RB#
NV_WR#0_RE# NV_WR#1_RE#
NV_WE#_CK0 NV_WE#_CK1
USBP0N USBP0P … USBP13N USBP13P
USBRBIAS# USBRBIAS
OC0# / GPIO59 OC1# / GPIO40 OC2# / GPIO41 OC3# / GPIO42 OC4# / GPIO43 OC5# / GPIO9 OC6# / GPIO10 OC7# / GPIO14
R483 X_32.4R1%0402-RH
R452 22.6R1%0402
R166 10KR0402
USB_OC#
+3VSUS
NOTE: USB Port 6,7 may not be available in all Ibex Peak SKUs.
2009/01/23 修改
USB_PN0 34 USB_PP0 34 USB_PN1 35 USB_PP1 35 USB_PN2 35 USB_PP2 35 USB_PN3 34 USB_PP3 34 USB_PN4 34 USB_PP4 34 USB_PN5 35 USB_PP5 35
USB_PN8 32 USB_PP8 32 USB_PN9 34 USB_PP9 34 USB_PN10 35 USB_PP10 35 USB_PN11 35 USB_PP11 35
USB_BIAS
PCI_GNT#0 PCI_GNT#1 R134 X_1KR0402 R129 X_1KR0402
PCI_GNT#3 R123 X_1KR0402
R122 0R0402 +3VRUN R125 R116 X_10KR0402 X_10KR0402
19 DGPU_SELECT#
Q12 X_NN-2N7002DW-7-F_SOT363-6-RH
DGPU_PWM_SELECT# R157 X_1KR0402
PCI_REQ#2
19 DGPU_PWM_SELECT#
TP26 TPJNC_TP26
PLT_RST#
21 CLK_PCI_FB
30 CLK_PCI_KBC
30 CLK_PCIF_PORT80
R428 22R0402 R136 22R0402 R427 22R0402
CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3
EC95 X_C10p50N0402 EC41 X_C10p50N0402 EC94 X_C10p50N0402
EMI
+3VRUN
RN12 8P4R-8.2KR0402-1
RN11 8P4R-8.2KR0402-1
RN14 8P4R-8.2KR0402-1
RN5 8P4R-8.2KR0402-1
RN13 8P4R-8.2KR0402-1
DGPU_PWM_SELECT# R150 10KR0402
C532 C0.1u10X0402
U24 S08P5X_SC70
25 DGPU_HOLD_RST#
PCIE_RST# 11
C316 C0.1u10X0402
U23 S08P5X_SC70
RN9 8P4R-33R0402
NEWCARD_RST# 34
WLAN_RST# 35
LPC_RST# 30
LAN_RST# 31
ER18
BUF_PTL_RST# 3

MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK - M (PCI,USB,NVRAM)

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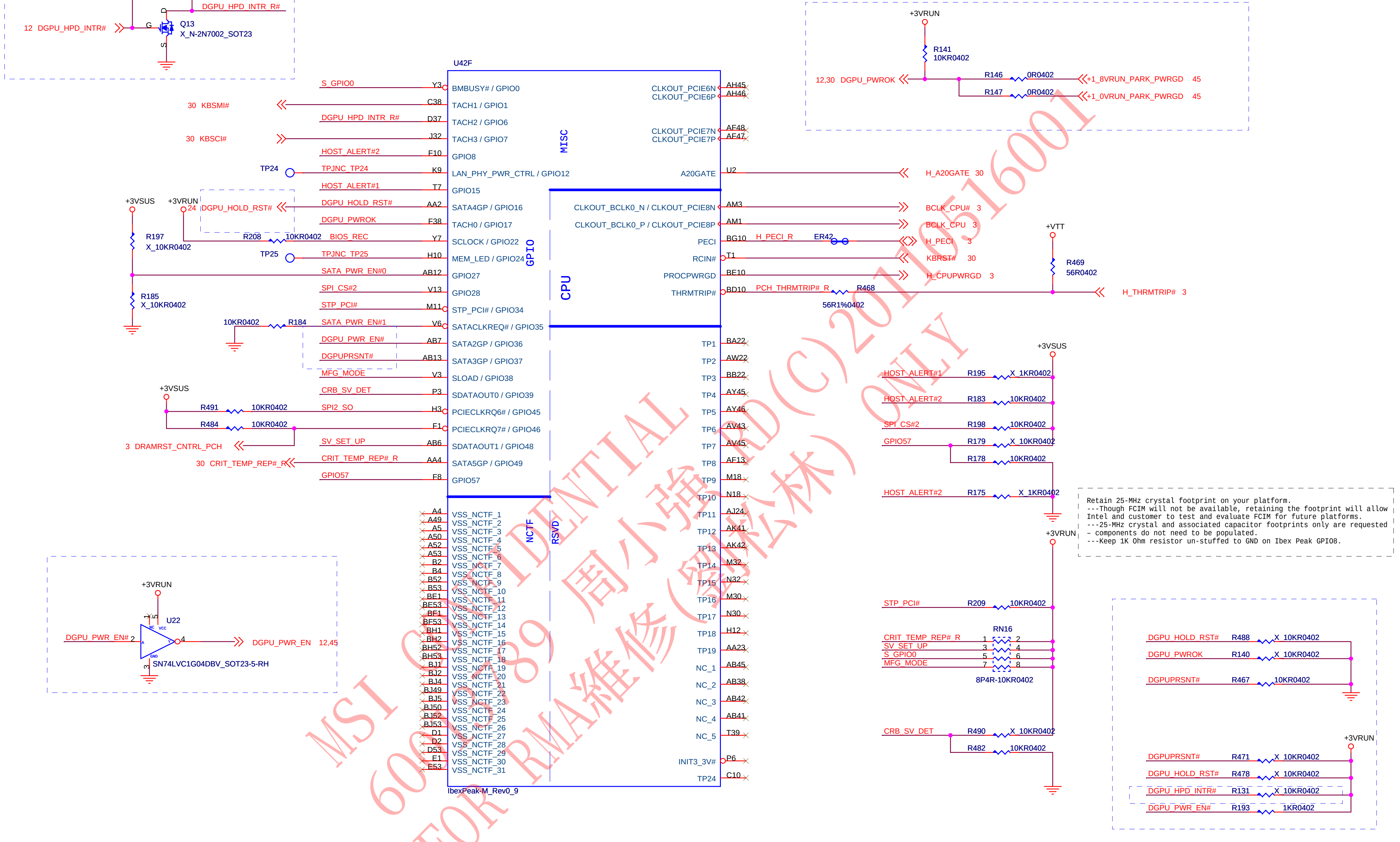
IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)



MICRO-STAR INT'L CO.,LTD.

Title: IBEXPEAK-M(GPIO,VSS_NCTF,RSVD)

Size	Document Number	Rev
Custom	MS-1688	11

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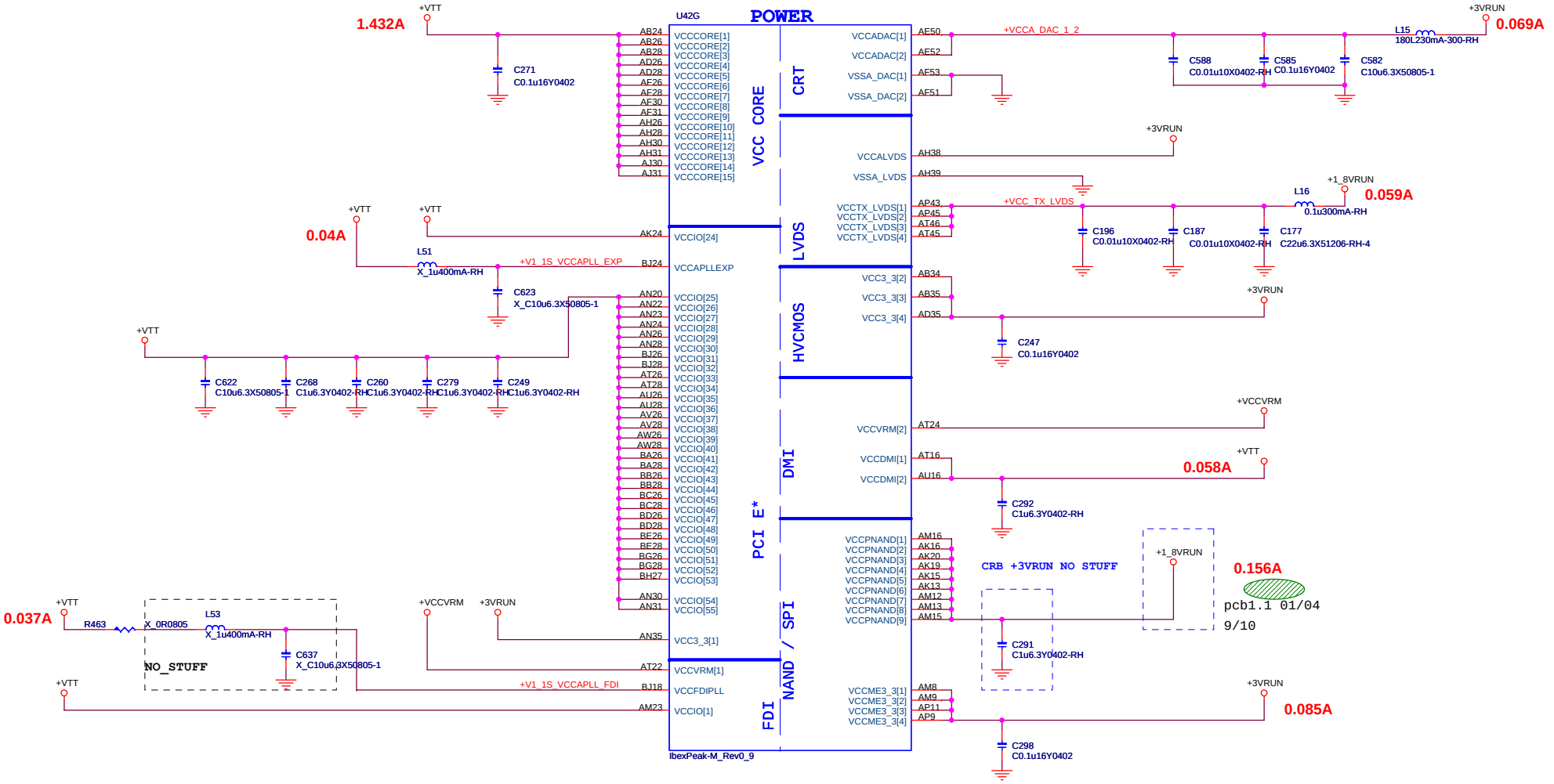
IBEXPEAK - M (POWER)



The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCACLK, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	IBEXPEAK - M (POWER)	
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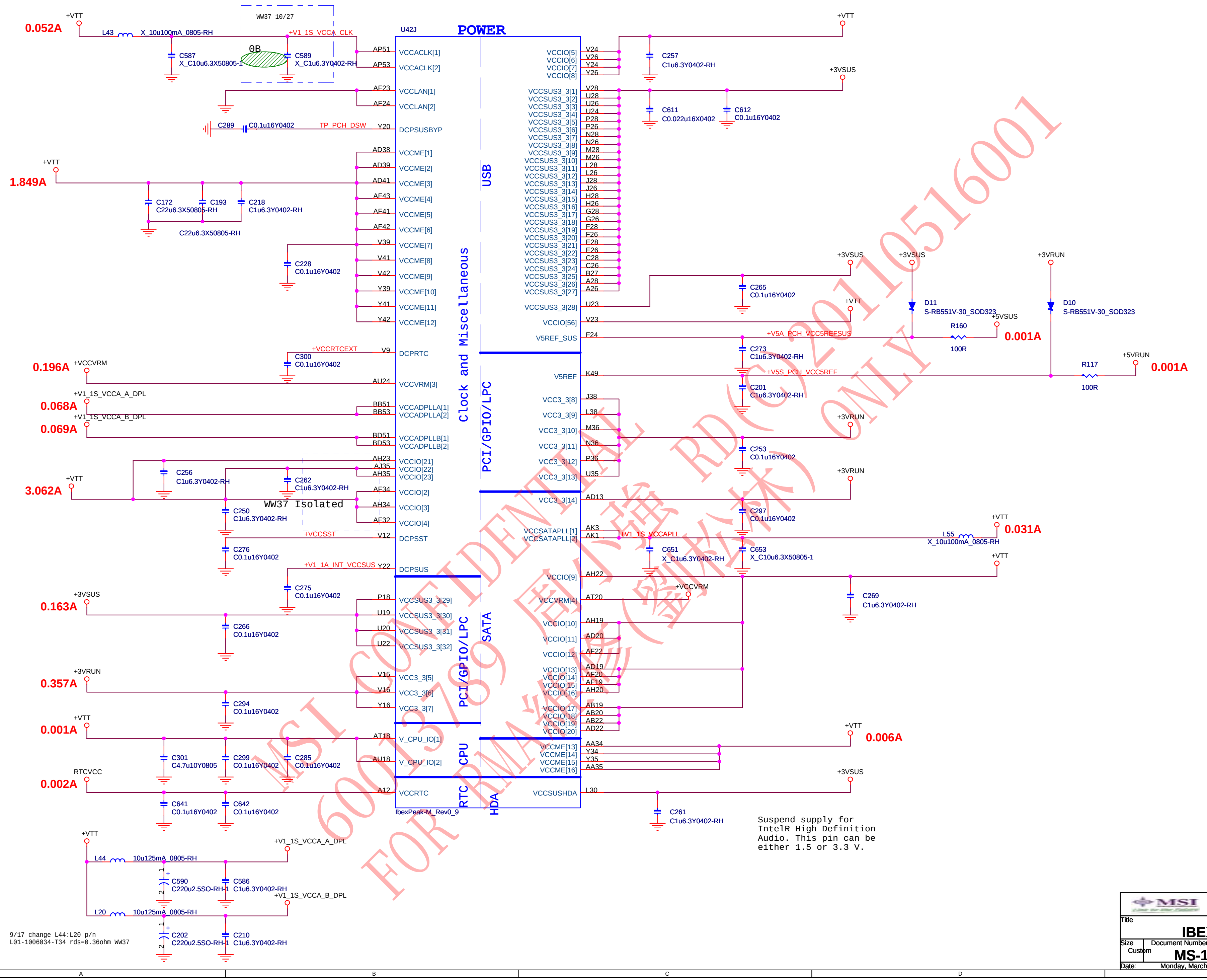
VccLAN may be grounded if Intel LAN is disabled.

IBEXPEAK - M (POWER)



Suspend supply for IntelR High Definition Audio. This pin can be either 1.5 or 3.3 V.

9/17 change L44:L20 p/n
L01-1006034-T34 rds=0.36ohm WW37

MICRO-STAR INT'L CO.,LTD.

Title	IBEXPEAK - M (POWER)	
Size: Custom	Document Number: MS-1688	Rev: 11
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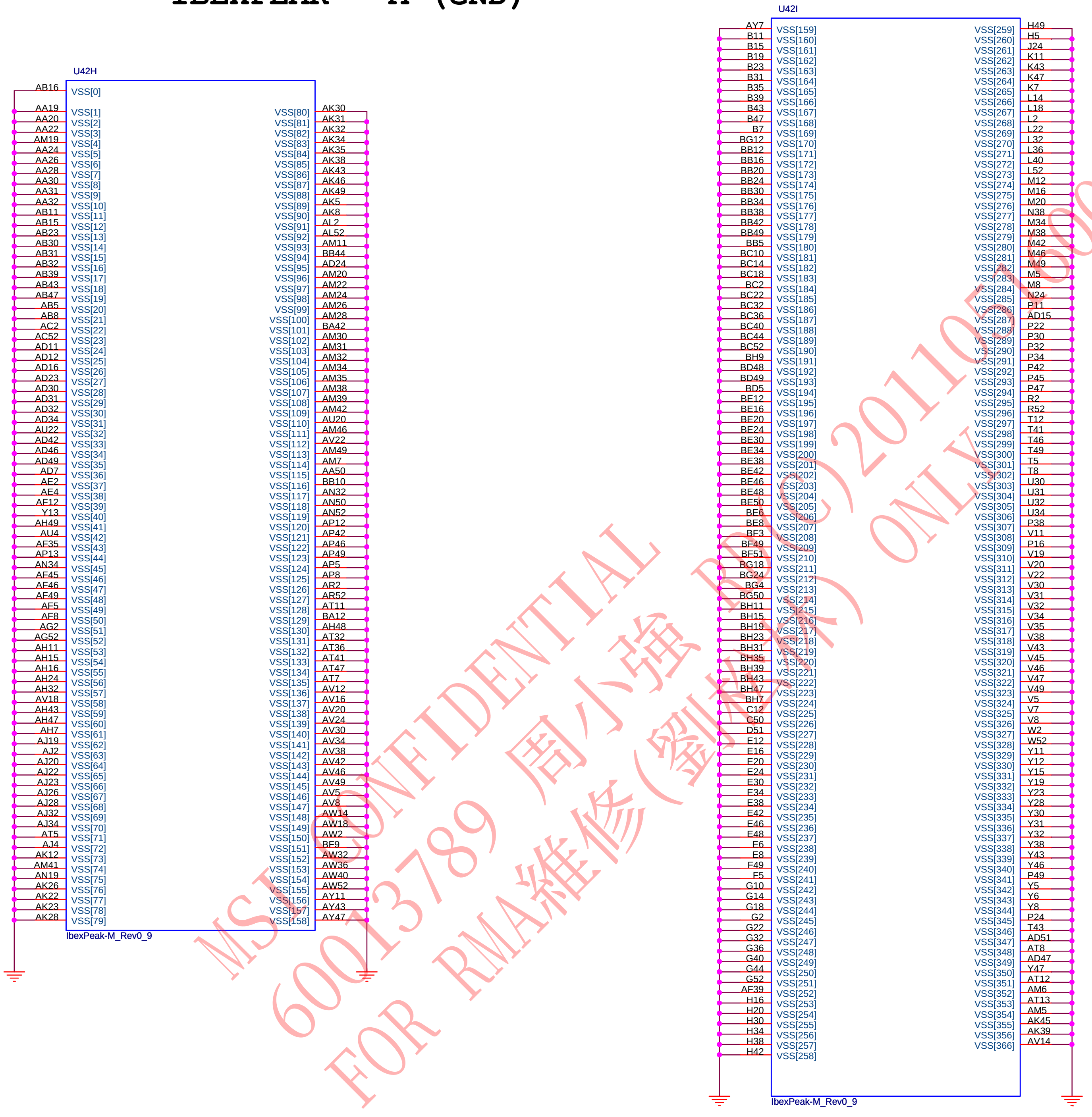
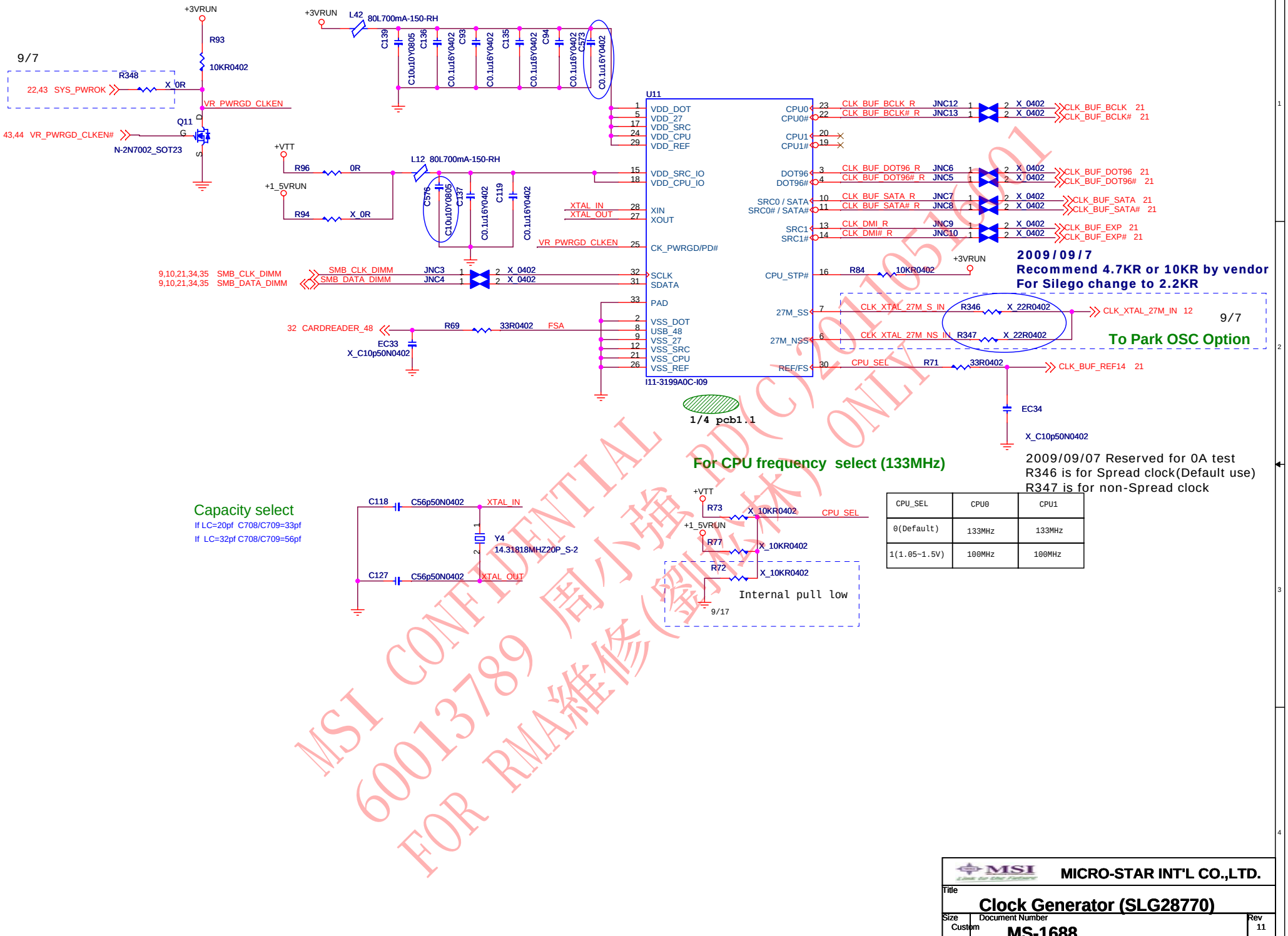
IBEXPEAK - M (GND)



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	IBEXPEAK - M (GND)		
Size: Custom	Document Number: MS-1688		Rev: 11
Date: Monday, March 22, 2010	Sheet 28 of 53		



CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

MICRO-STAR INT'L CO.,LTD.

Title: Clock Generator (SLG28770)

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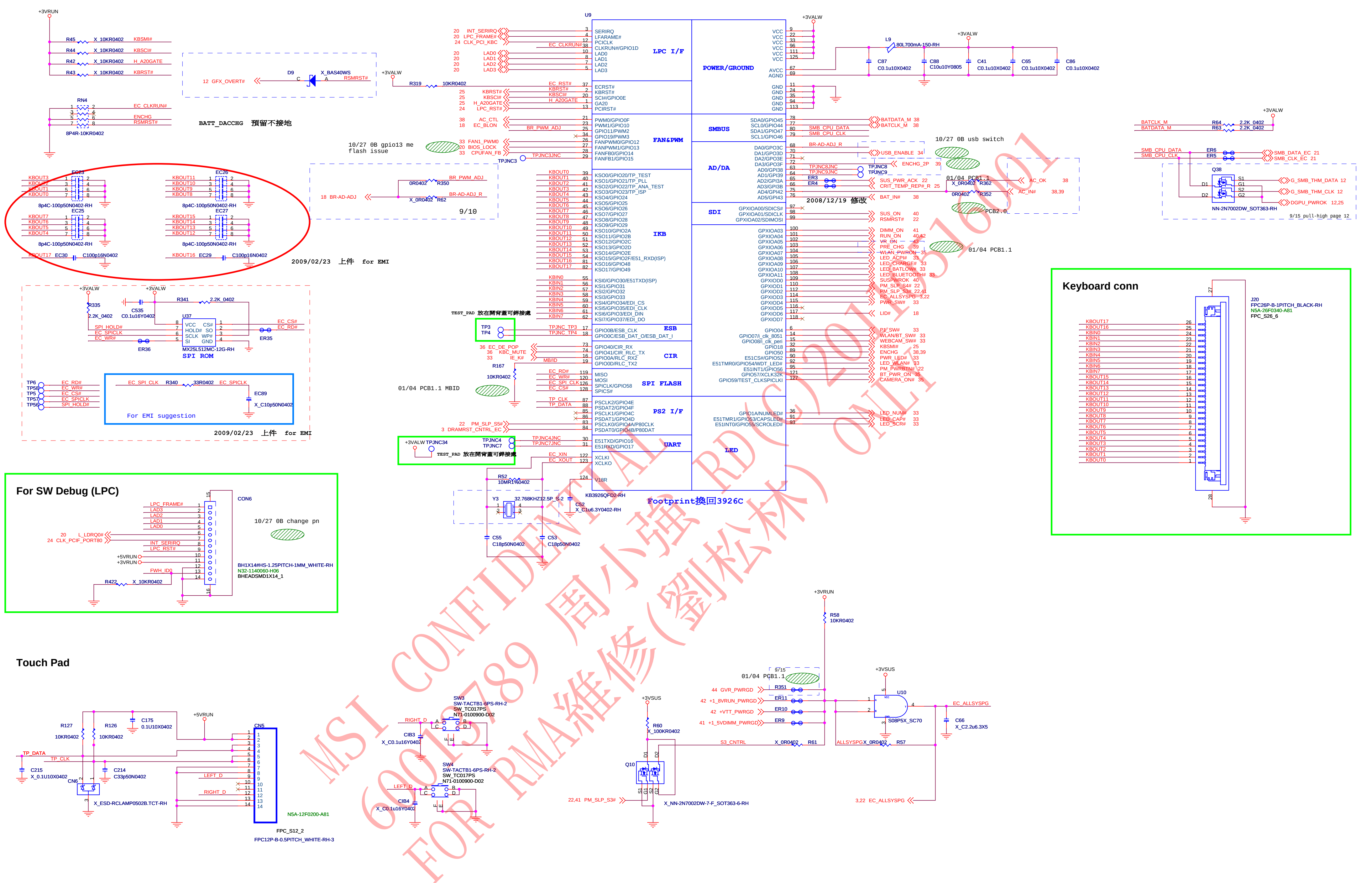

MICRO-STAR INT'L CO.,LTD.

Title: KBC/EC/uP (ENE3926-LFQP144)

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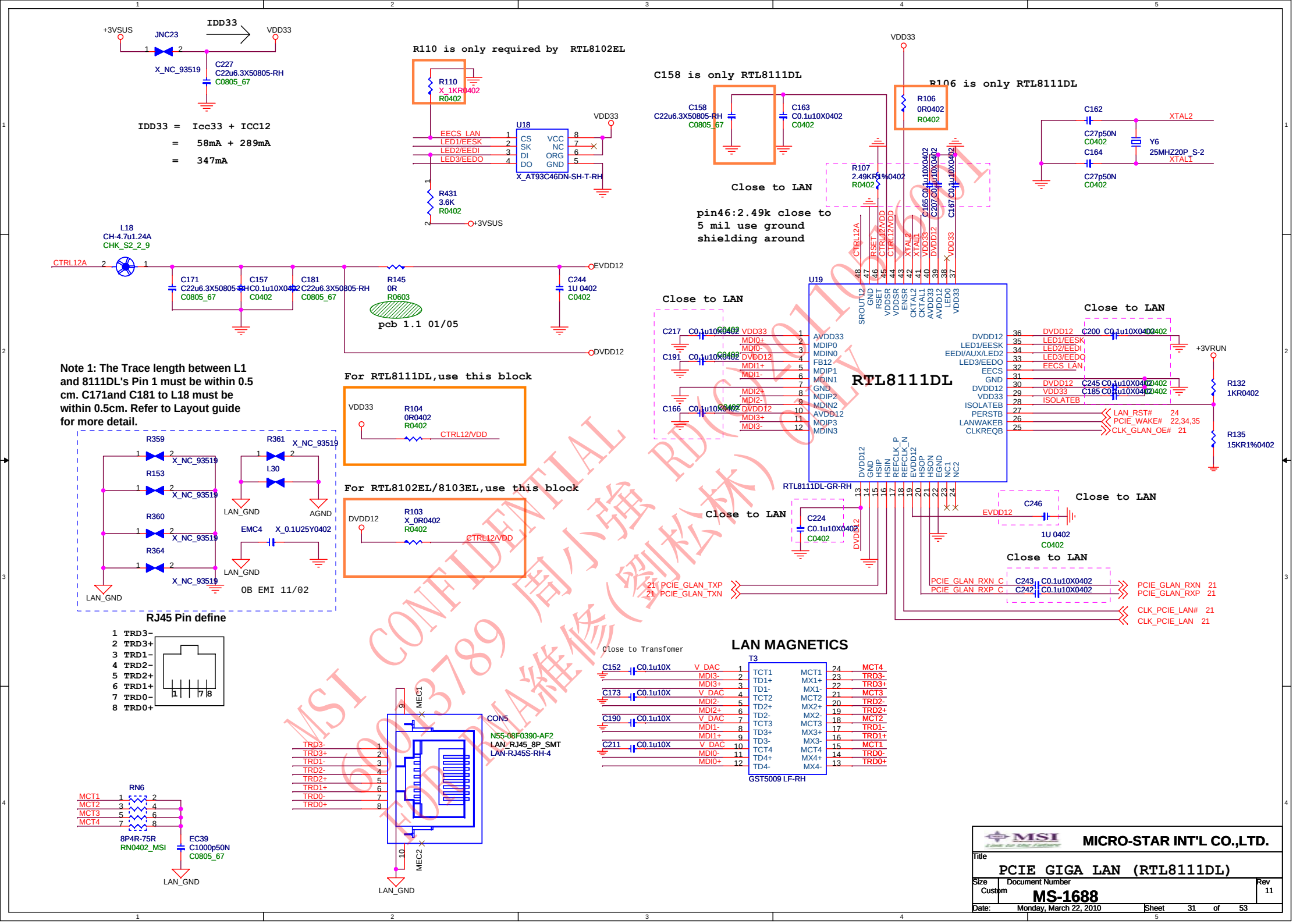

MICRO-STAR INT'L CO.,LTD.			
Title: PCIE GIGA LAN (RTL8111DL)			
Size: Custom	Document Number: MS-1688		Rev: 11
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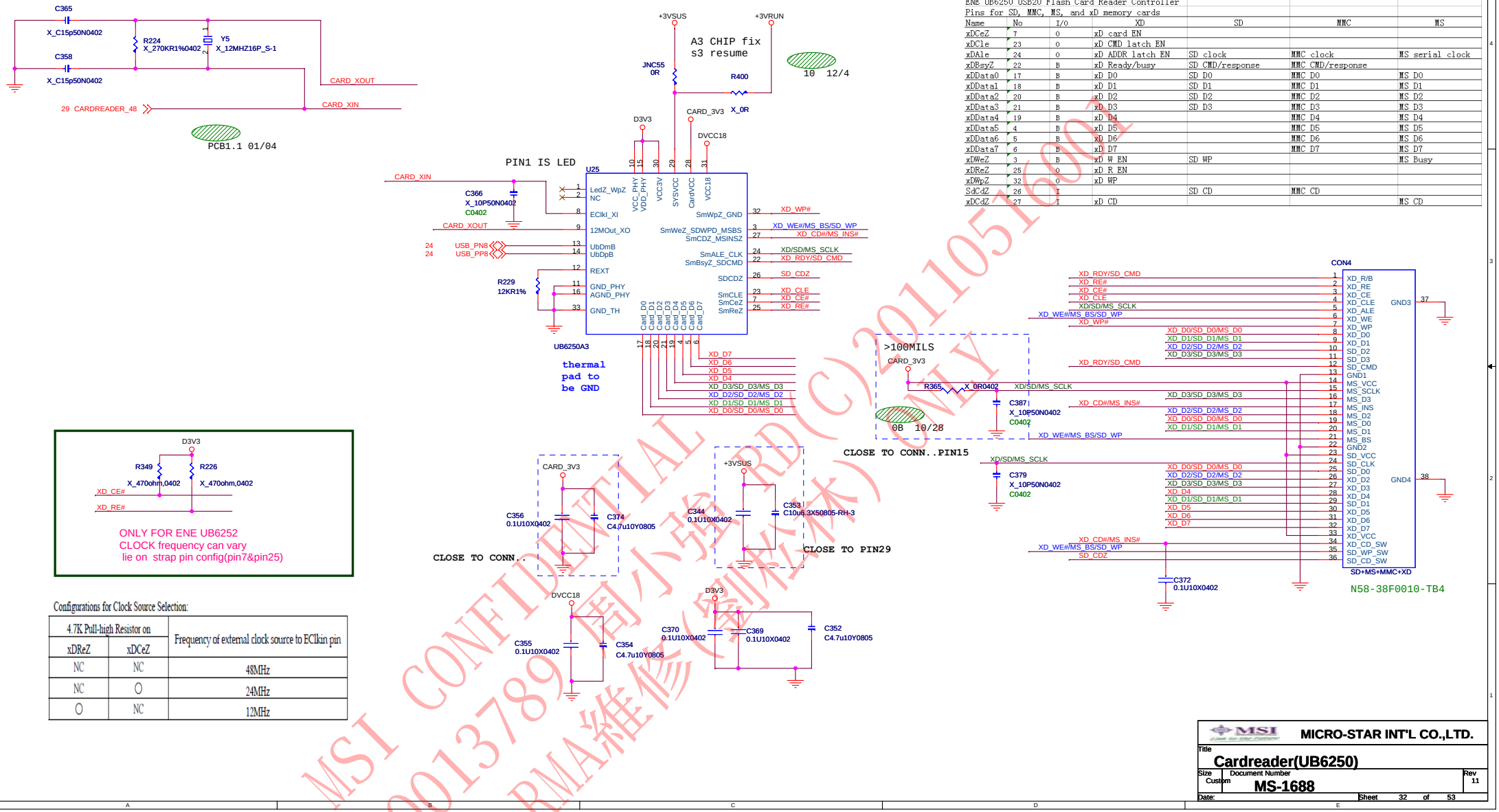

ENE UB6250 USB20 Flash Card Reader Controller
Pins for SD, MMC, MS, and xD memory cards

Name	No	I/O	XD	SD	MMC	MS
xDCeZ	7	O	xD card EN			
xDCle	23	O	xD CMD latch EN			
xDAle	24	O	xD ADDR latch EN	SD clock	MMC clock	MS serial clock
xDBsyZ	22	B	xD Ready/busy	SD CMD/response	MMC CMD/response	
xDData0	17	B	xD D0	SD D0	MMC D0	MS D0
xDData1	18	B	xD D1	SD D1	MMC D1	MS D1
xDData2	20	B	xD D2	SD D2	MMC D2	MS D2
xDData3	21	B	xD D3	SD D3	MMC D3	MS D3
xDData4	19	B	xD D4		MMC D4	MS D4
xDData5	4	B	xD D5		MMC D5	MS D5
xDData6	5	B	xD D6		MMC D6	MS D6
xDData7	6	B	xD D7		MMC D7	MS D7
xDWeZ	3	B	xD W EN	SD WP		MS Busy
xDReZ	25	O	xD R EN			
xDWpZ	32	O	xD WP			
SdCdZ	26	I		SD CD	MMC CD	
xDCdZ	27	I	xD CD			MS CD

Configurations for Clock Source Selection:

4.7K Pull-high Resistor on		Frequency of external clock source to EClkin pin
xDReZ	xDCeZ	
NC	NC	48MHz
NC	O	24MHz
O	NC	12MHz

MICRO-STAR INT'L CO.,LTD.

Title: Cardreader(UB6250)

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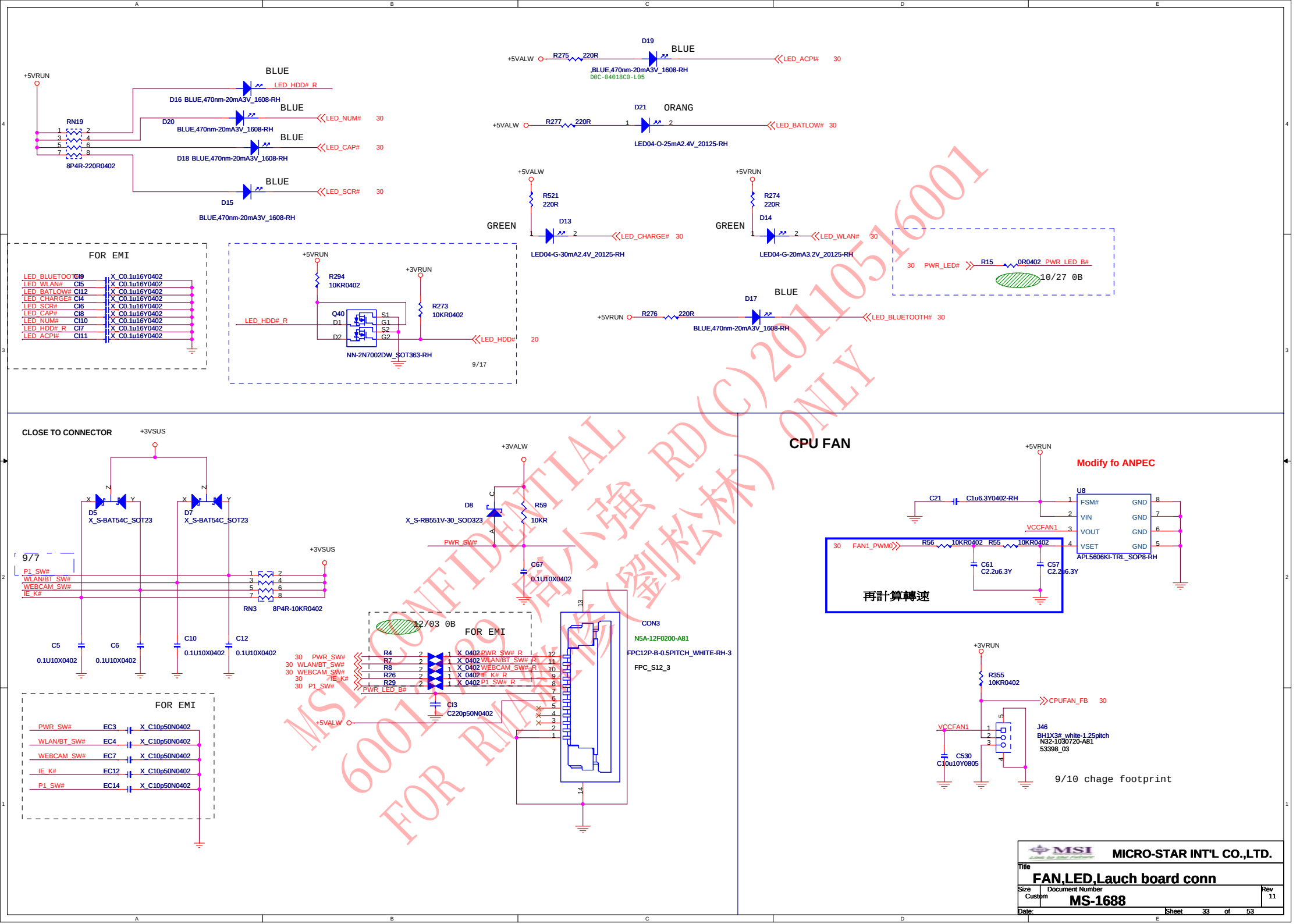

MICRO-STAR INT'L CO.,LTD.

Title: FAN,LED,Lauch board conn

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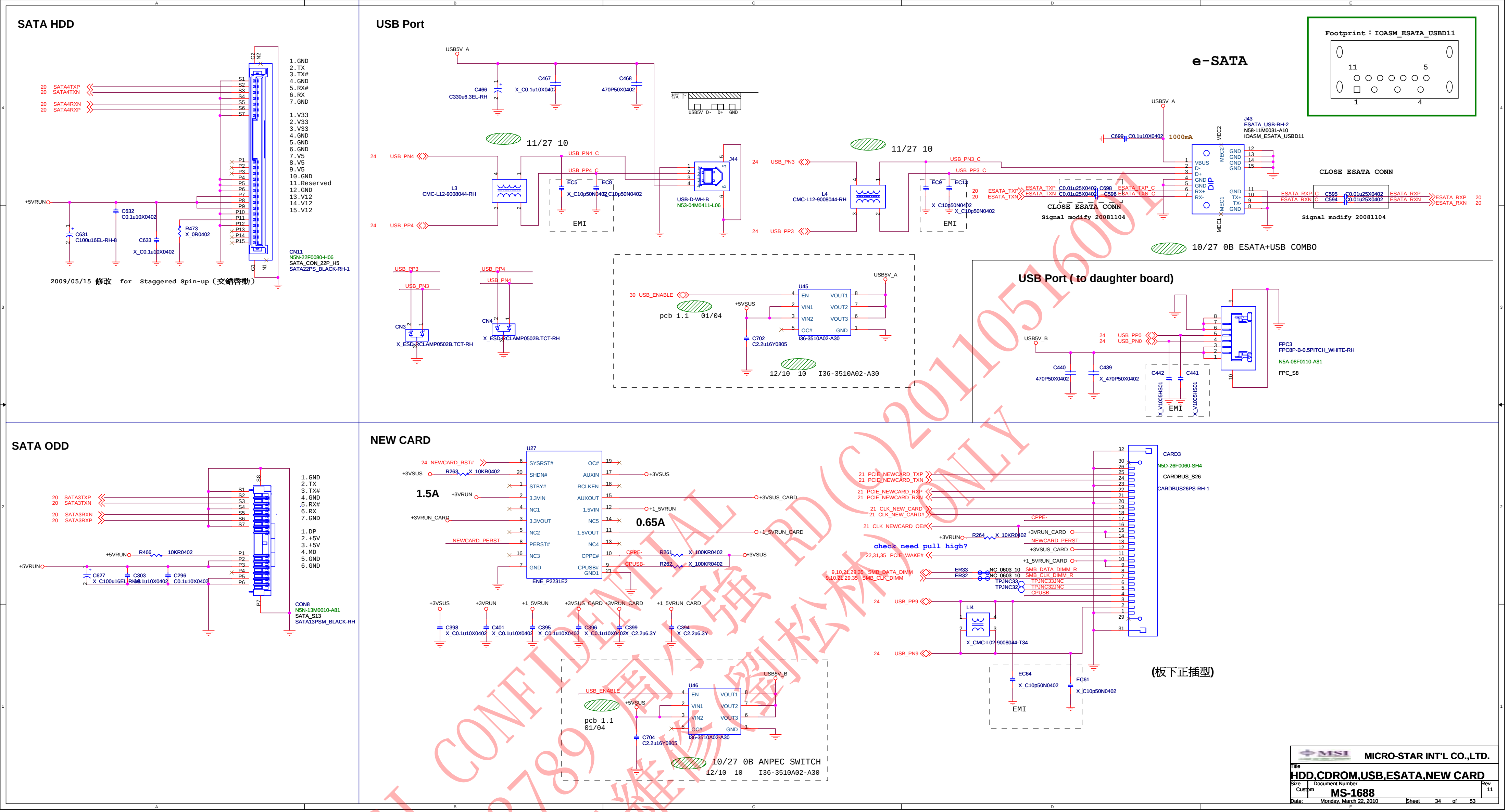

MICRO-STAR INT'L CO.,LTD.

Title: HDD,CDROM,USB,ESATA,NEW CARD

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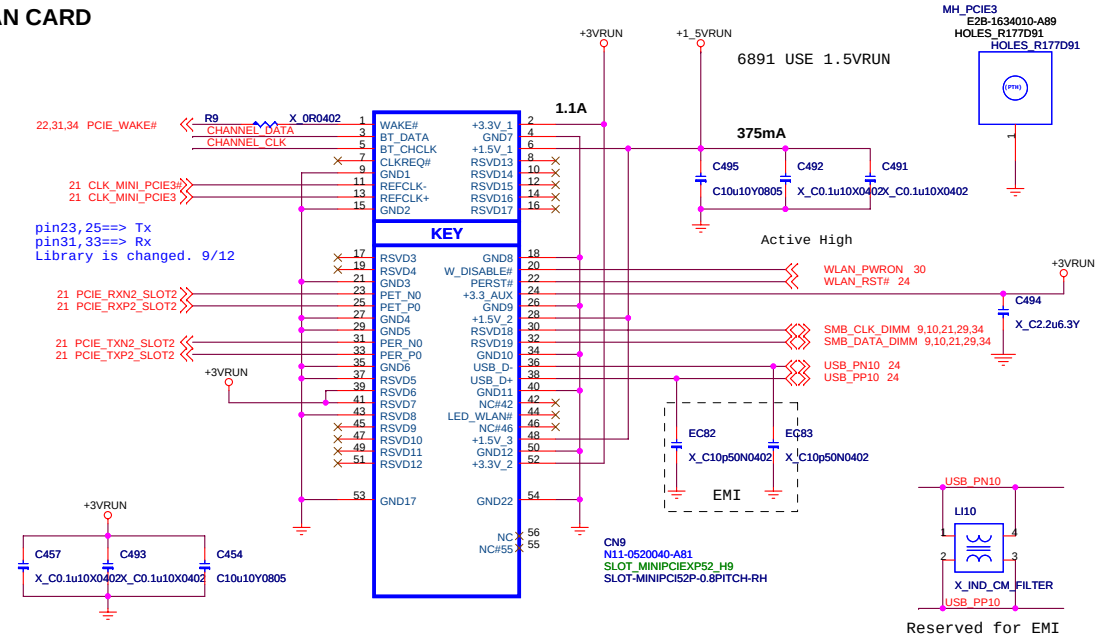
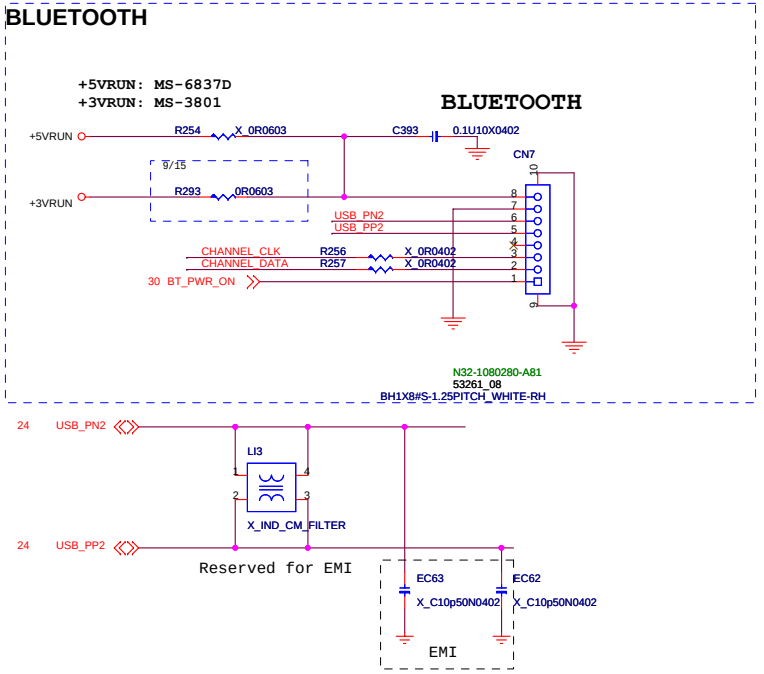
WLAN CARD

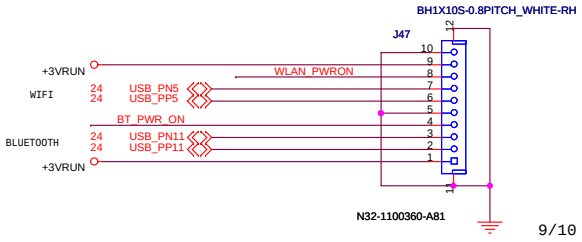


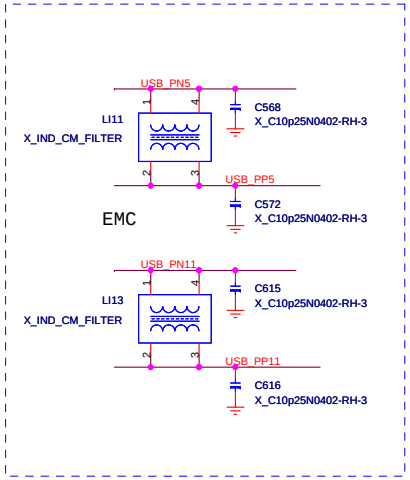
BLUETOOTH



MS-3870

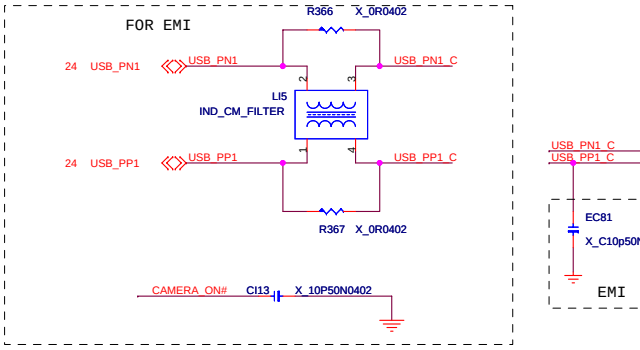
REMOVE TV TUNER

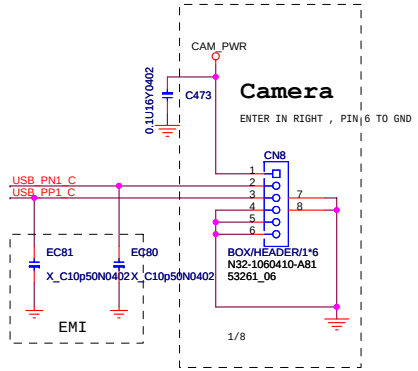


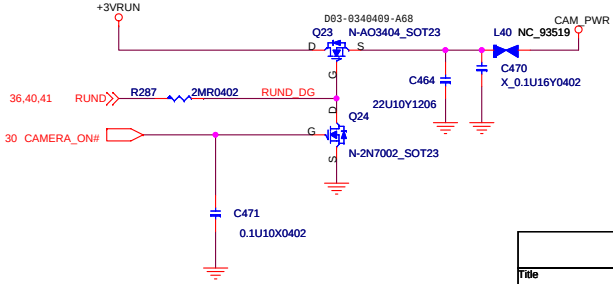


CAMERA

11/30 10







MSI CORPORATION		
Title: MINI_PCIE,CAMERA,BLUETOOTH		
Size: Custom	Document Number: MS-1688	Rev: 11
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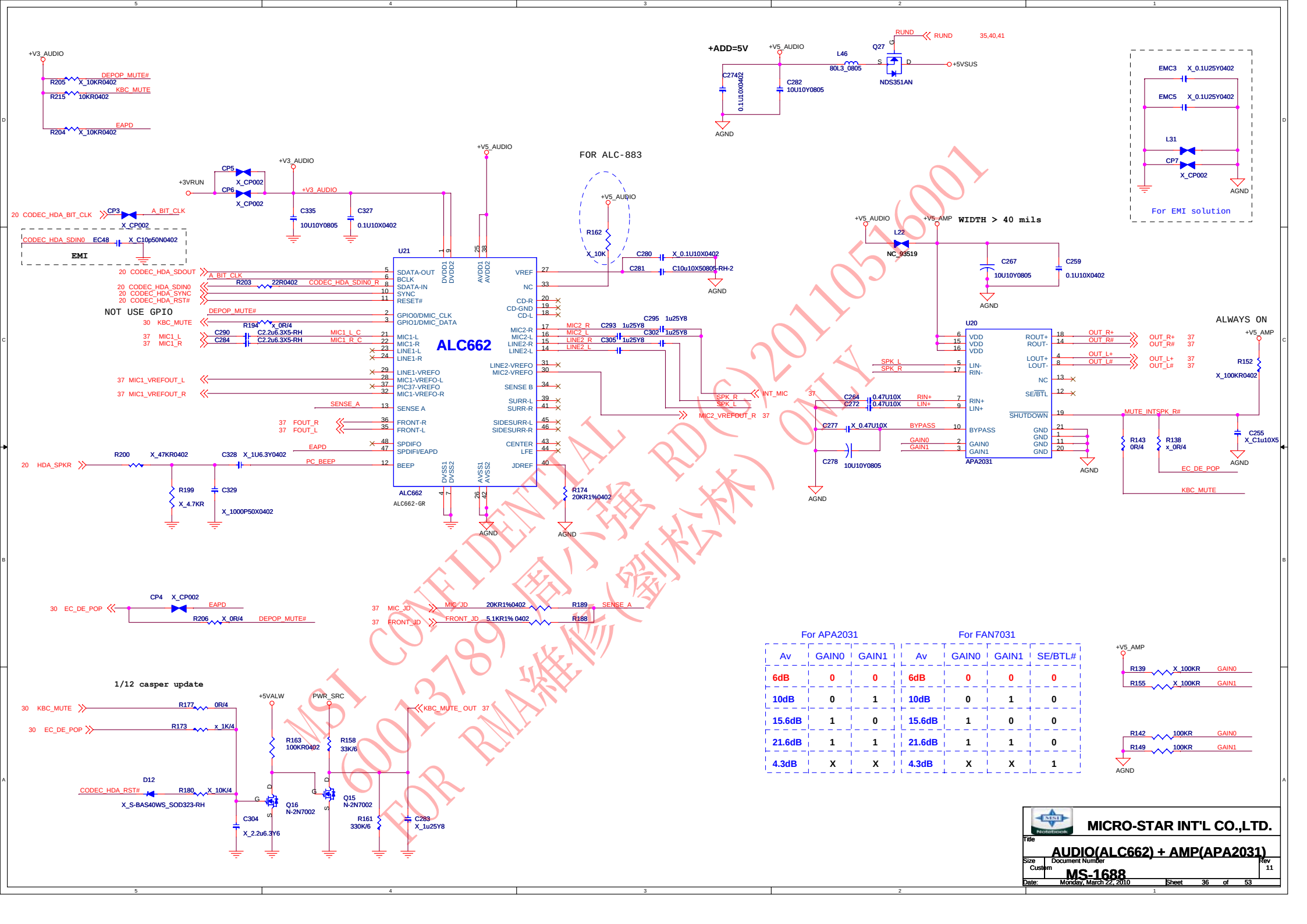
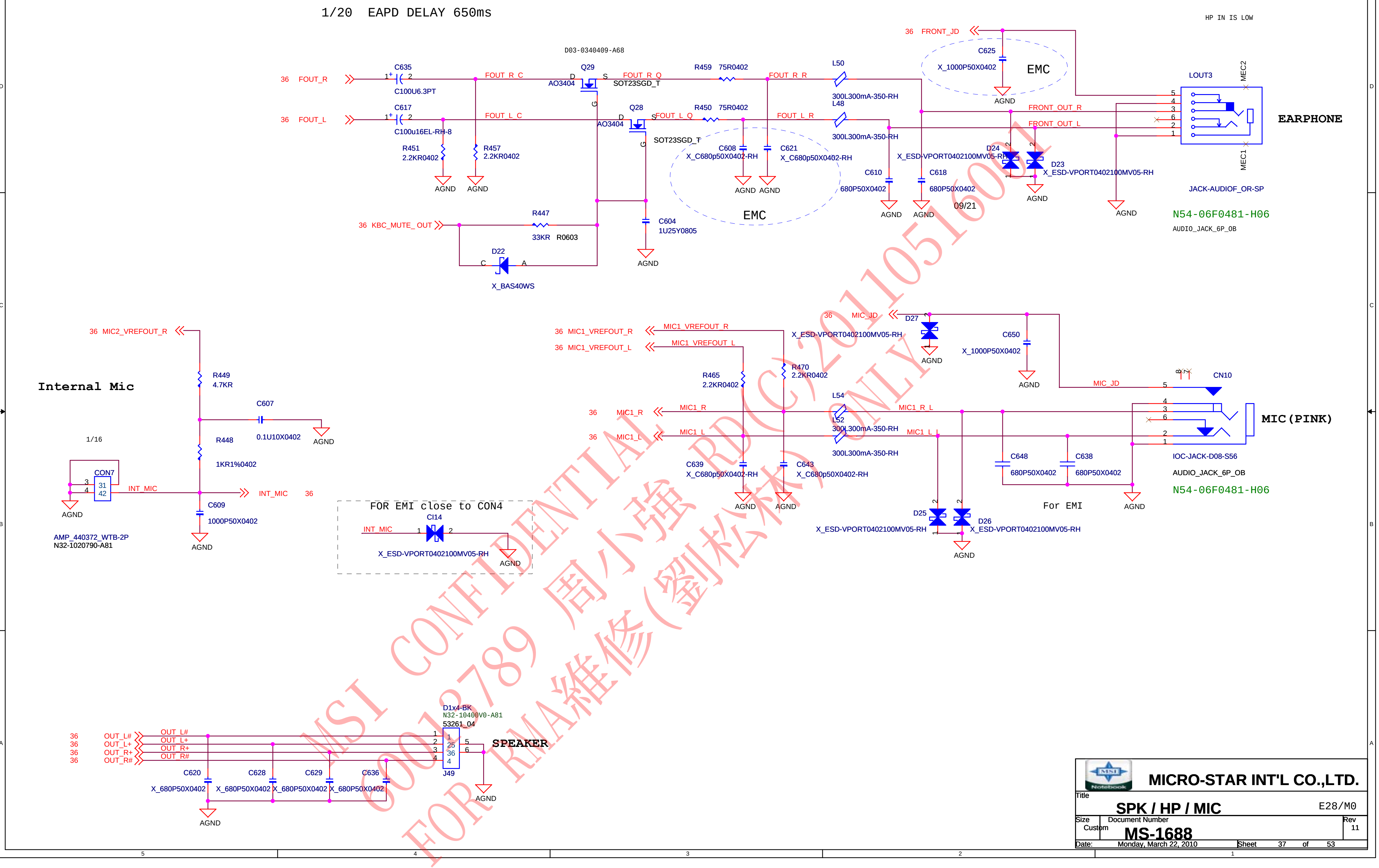


For APA2031			For FAN7031			
Av	GAIN0	GAIN1	Av	GAIN0	GAIN1	SE/BTL#
6dB	0	0	6dB	0	0	0
10dB	0	1	10dB	0	1	0
15.6dB	1	0	15.6dB	1	0	0
21.6dB	1	1	21.6dB	1	1	0
4.3dB	X	X	4.3dB	X	X	1



1/20 EAPD DELAY 650ms
D03-0340409-A68
HP IN IS LOW
FOUT_R
FOUT_L
C635 C100U6.3PT
C617 C100u16EL-RH-8
FOUT_R_C
FOUT_L_C
Q29 AO3404 SOT23SGD_T
Q28 AO3404 SOT23SGD_T
FOUT_R_Q
FOUT_L_Q
R459 75R0402
R450 75R0402
FOUT_R_R
FOUT_L_R
L50 300L300mA-350-RH
L48 300L300mA-350-RH
FRONT_JD
C625 X_1000P50X0402
EMC
LOUT3
MEC2
MEC1
FRONT_OUT_R
FRONT_OUT_L
EARPHONE
JACK-AUDIOF_OR-SP
N54-06F0481-H06
AUDIO_JACK_6P_OB
R451 2.2KR0402
R457 2.2KR0402
C608 X_C680p50X0402-RH
C621 X_C680p50X0402-RH
C610 680P50X0402
C618 680P50X0402
D24 X_ESD-VPORT0402100MV05-RH
D23 X_ESD-VPORT0402100MV05-RH
09/21
KBC_MUTE_OUT
R447 33KR R0603
C604 1U25Y0805
D22 X_BAS40WS
AGND
MIC2_VREFOUT_R
Internal Mic
R449 4.7KR
C607 0.1U10X0402
R448 1KR1%0402
1/16
CON7
INT_MIC
C609 1000P50X0402
AMP_440372_WTB-2P
N32-1020790-A81
MIC1_VREFOUT_R
MIC1_VREFOUT_L
MIC_JD
D27 X_ESD-VPORT0402100MV05-RH
C650 X_1000P50X0402
R465 2.2KR0402
R470 2.2KR0402
CN10
MIC (PINK)
MIC1_R
MIC1_L
MIC1_R_L
MIC1_L_L
L54 300L300mA-350-RH
L52 300L300mA-350-RH
C639 X_C680p50X0402-RH
C643 X_C680p50X0402-RH
C648 680P50X0402
C638 680P50X0402
IOC-JACK-D08-S56
AUDIO_JACK_6P_OB
N54-06F0481-H06
For EMI
D25 X_ESD-VPORT0402100MV05-RH
D26 X_ESD-VPORT0402100MV05-RH
FOR EMI close to CON4
CI14 X_ESD-VPORT0402100MV05-RH
OUT_L#
OUT_L+
OUT_R+
OUT_R#
D1x4-BK
N32-10400V0-A81
53261_04
J49
SPEAKER
C620 X_680P50X0402
C628 X_680P50X0402
C629 X_680P50X0402
C636 X_680P50X0402

MICRO-STAR INT'L CO.,LTD.

Title: SPK / HP / MIC E28/M0

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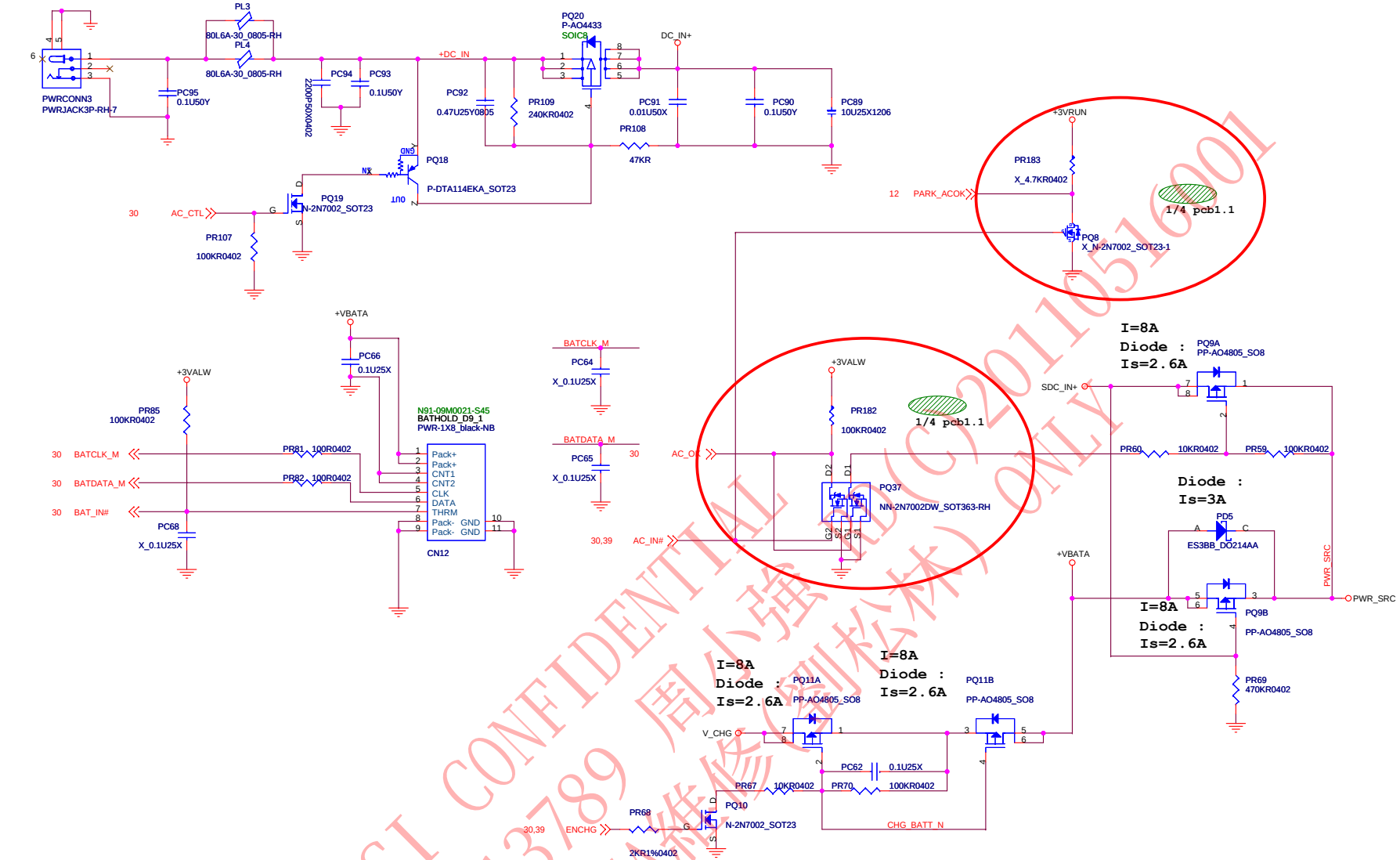
N92-03M0351-AF2



MICRO-STAR INT'L CO.,LTD.

Title: Battery select

E39/M0

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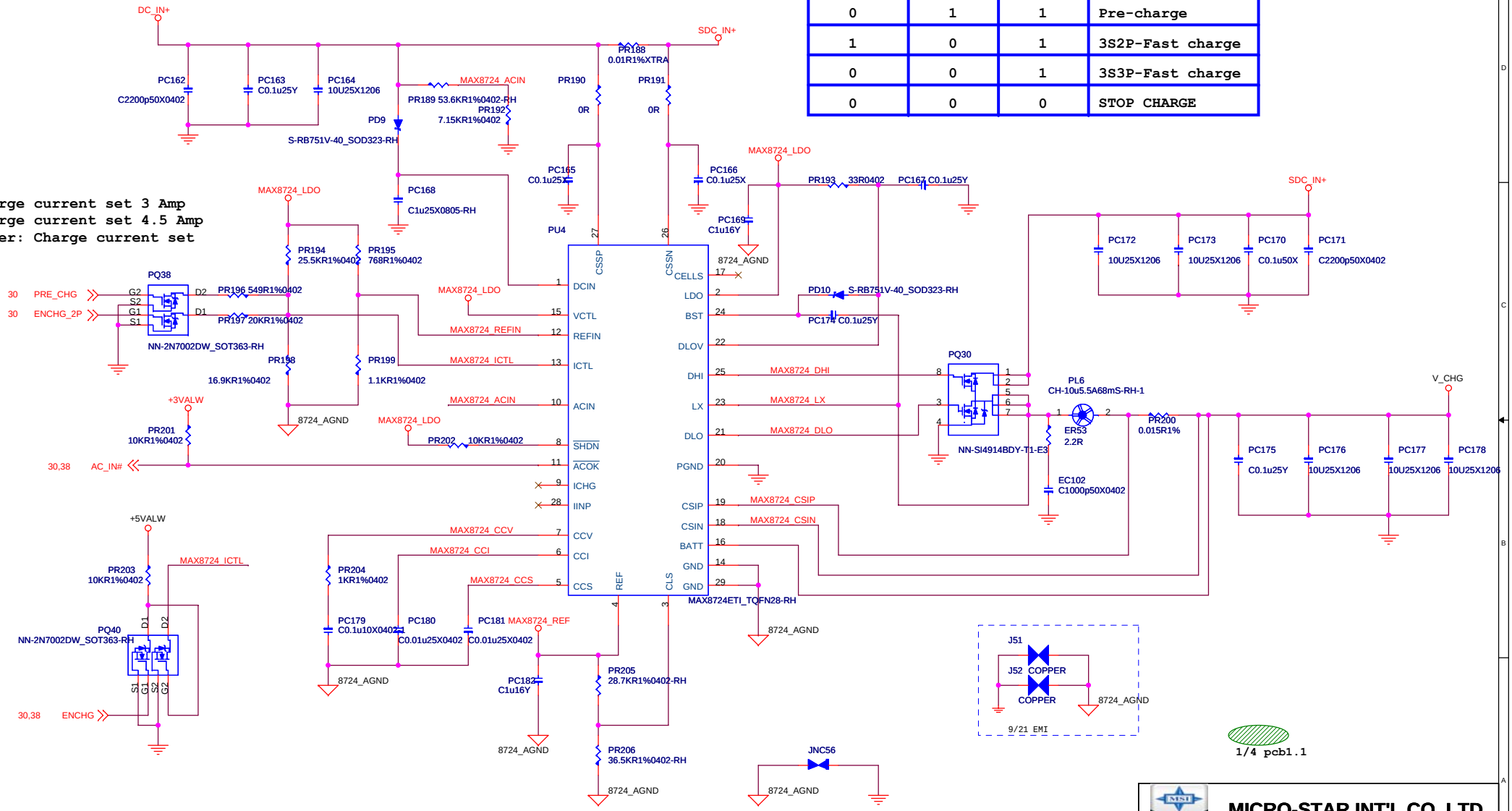
Adapter= 90 W 2.048/7.15*(53.6+7.15)=17.4V

Adapter input voltage set 17.4 Voltage

ENCHG-2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	3S2P-Fast charge
0	0	1	3S3P-Fast charge
0	0	0	STOP CHARGE

3S2P: Charge current set 3 Amp
3S3P: Charge current set 4.5 Amp
Pre-charger: Charge current set 220mA



MICRO-STAR INT'L CO.,LTD.

Title: **Battery Charger** E51/M0

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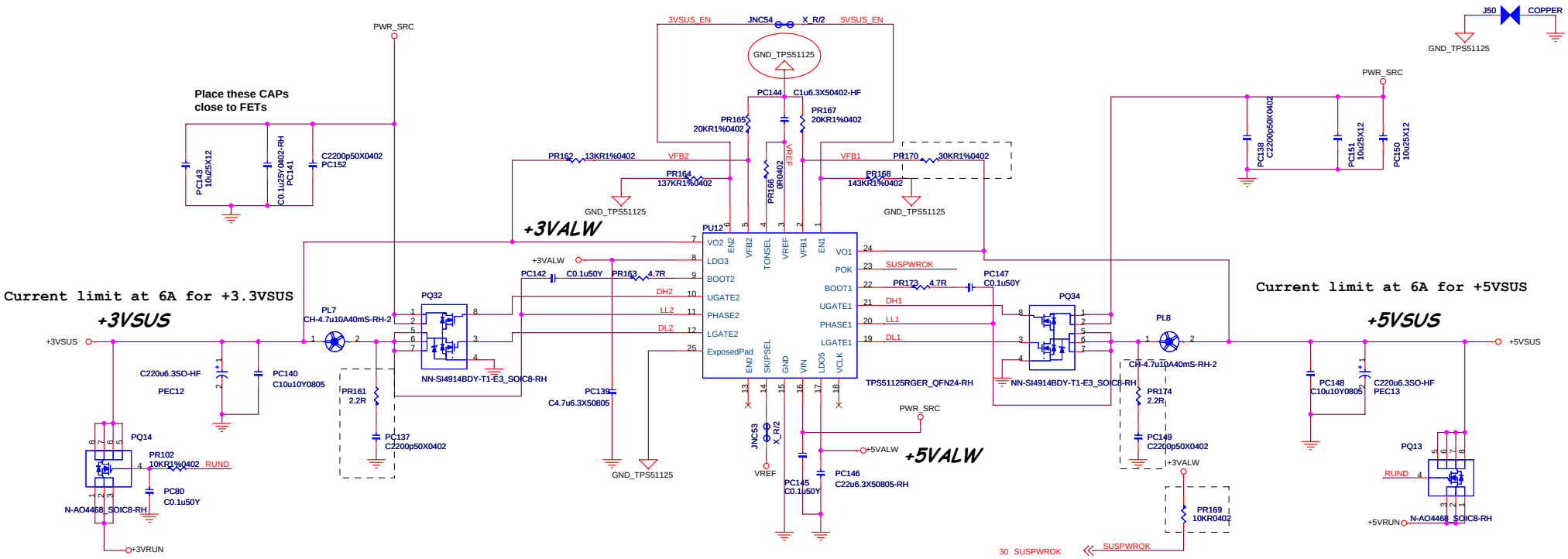

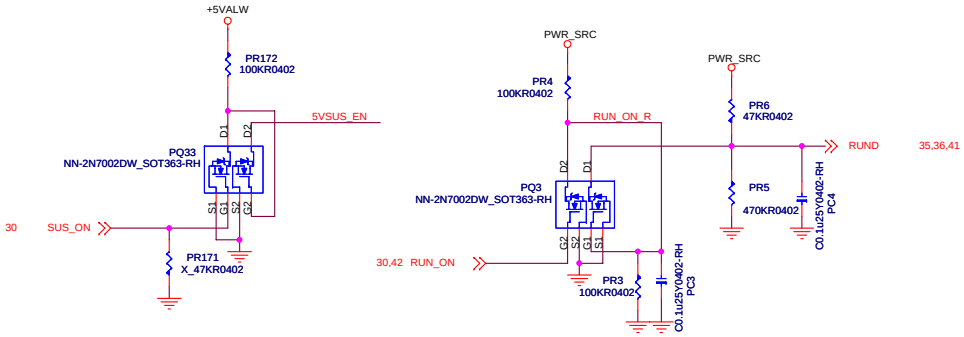

MICRO-STAR INT'L CO.,LTD.		
Title: System power		
Size: Custom	Document Number: MS-1688	Rev: 11
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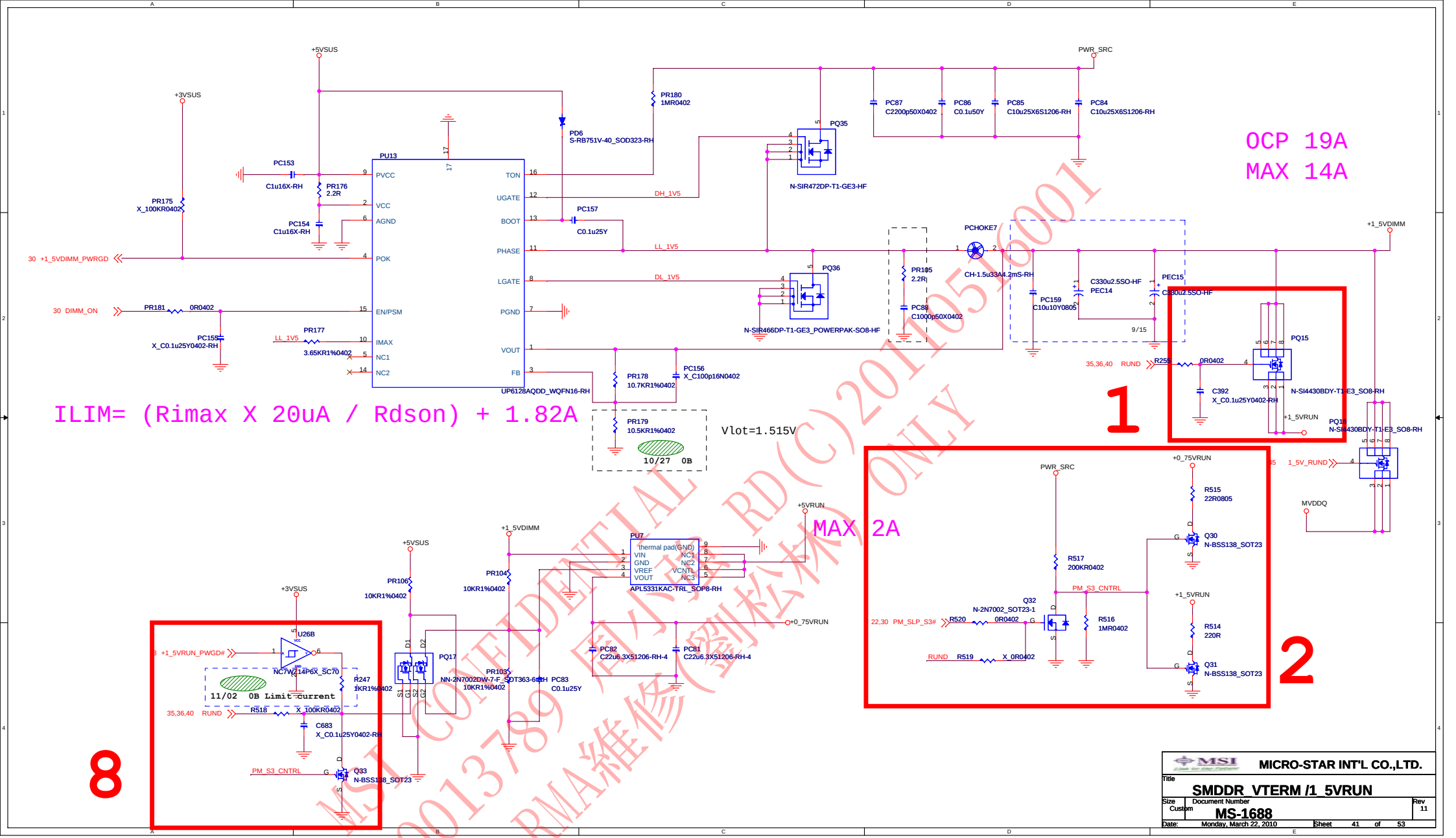

Title	SMDDR_VTERM /1_5VRUN
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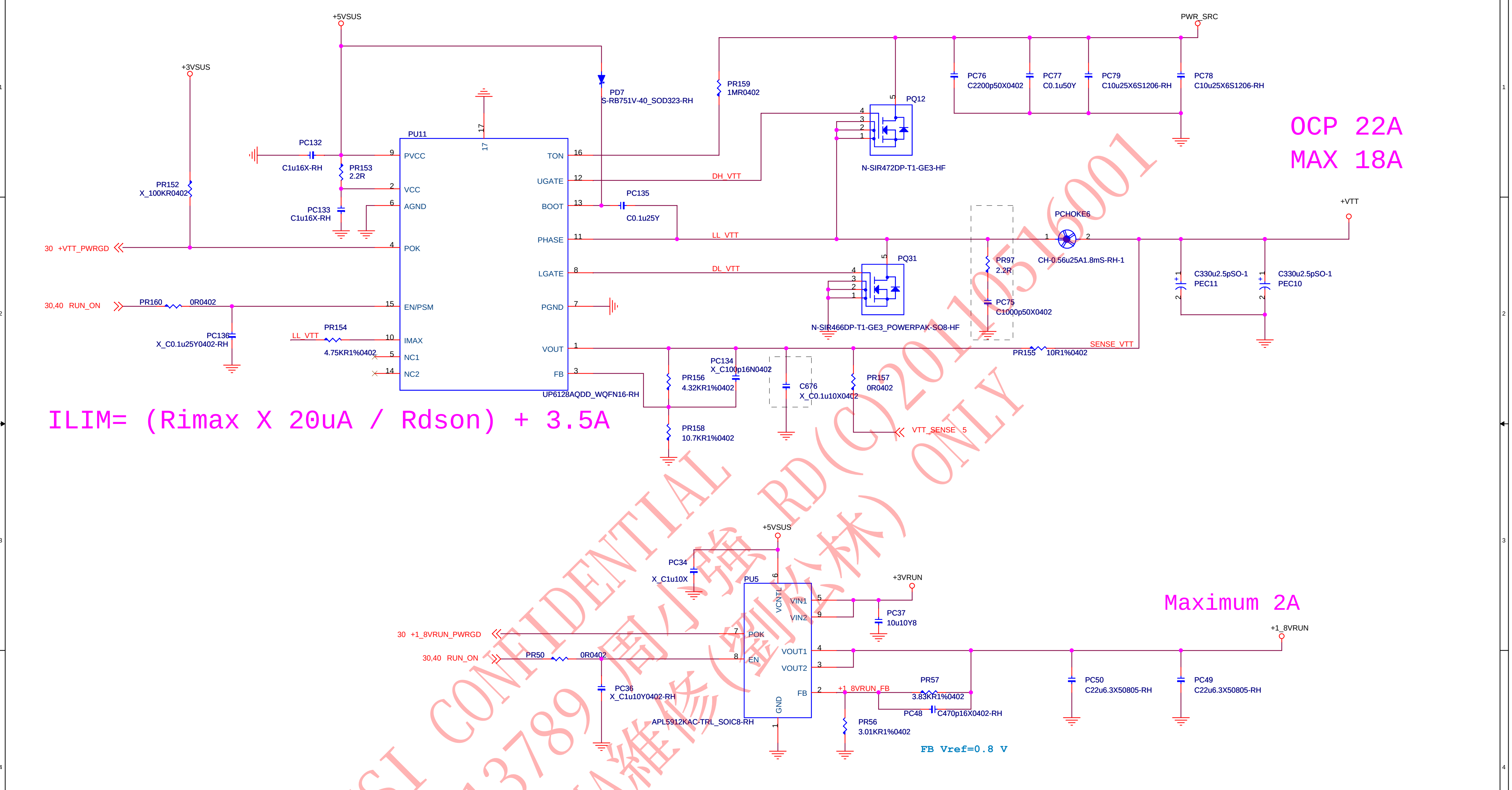
MICRO-STAR INT'L CO.,LTD.



MICRO-STAR INT'L CO.,LTD.

Title: VTT Power,+1.8VRUN

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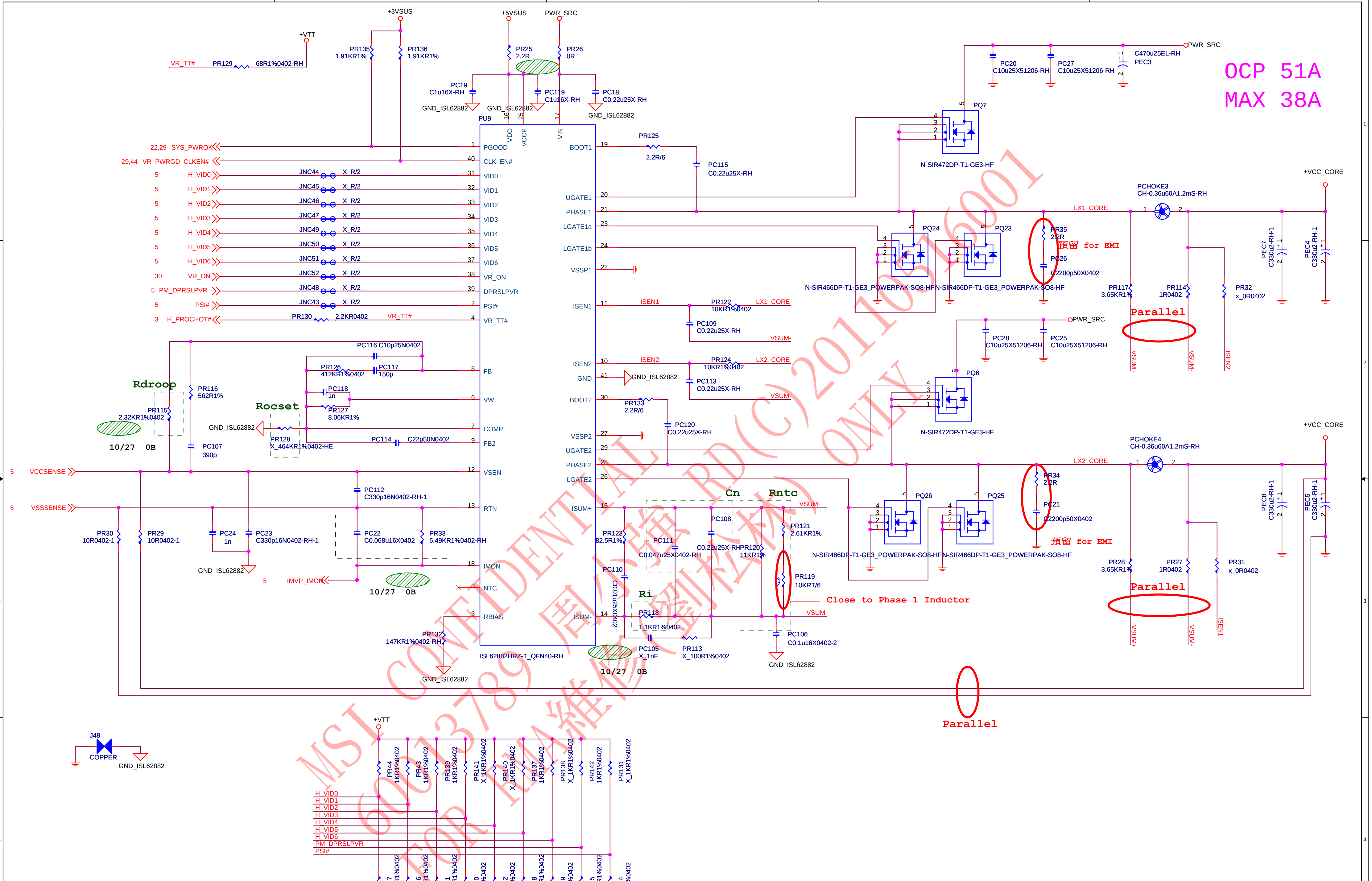
OCP 51A
MAX 38A
ISL62882HRZ-T_QFN40-RH
PU9
+3VSUS
+5VSUS
PWR_SRC
+VTT
+VCC_CORE
PGOOD
CLK_EN#
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VR_ON
DPRSLPVR
PSI#
VR_TT#
FB
VW
COMP
FB2
VSEN
RTN
IMON
NTC
RBIAS
BOOT1
UGATE1
PHASE1
LGATE1a
LGATE1b
VSSP1
ISEN1
ISEN2
GND
BOOT2
VSSP2
UGATE2
PHASE2
LGATE2
ISUM+
ISUM-
VDD
VCCP
VIN
SYS_PWROK
VR_PWRGD_CLKEN#
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
PM_DPRSLPVR
H_PROCHOT#
VCCSENSE
VSSSENSE
IMVP_IMON
LX1_CORE
LX2_CORE
VSUM+
VSUM-
GND_ISL62882
Rdroop
Rocset
Cn
Rntc
Ri
10/27 0B
預留 for EMI
Parallel
Close to Phase 1 Inductor
PCHOKE3
CH-0.36u60A1.2mS-RH
PCHOKE4
CH-0.36u60A1.2mS-RH
N-SIR472DP-T1-GE3-HF
N-SIR466DP-T1-GE3_POWERPAK-SO8-HF
PQ7
PQ6
PQ23
PQ24
PQ25
PQ26
J48
COPPER
MSI CONFIDENTIAL

MICRO-STAR INT'L CO.,LTD.

Title

CPU Power

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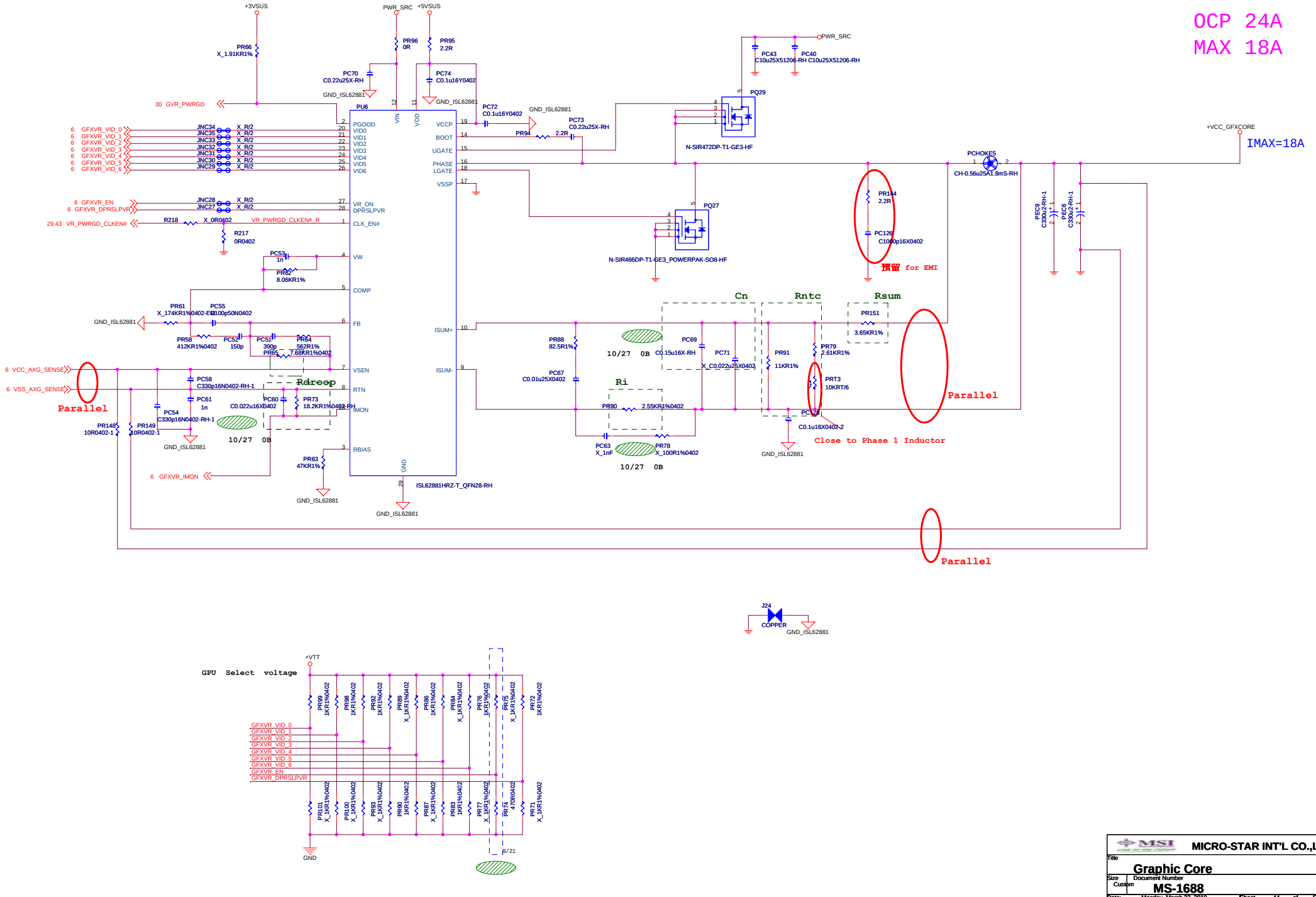
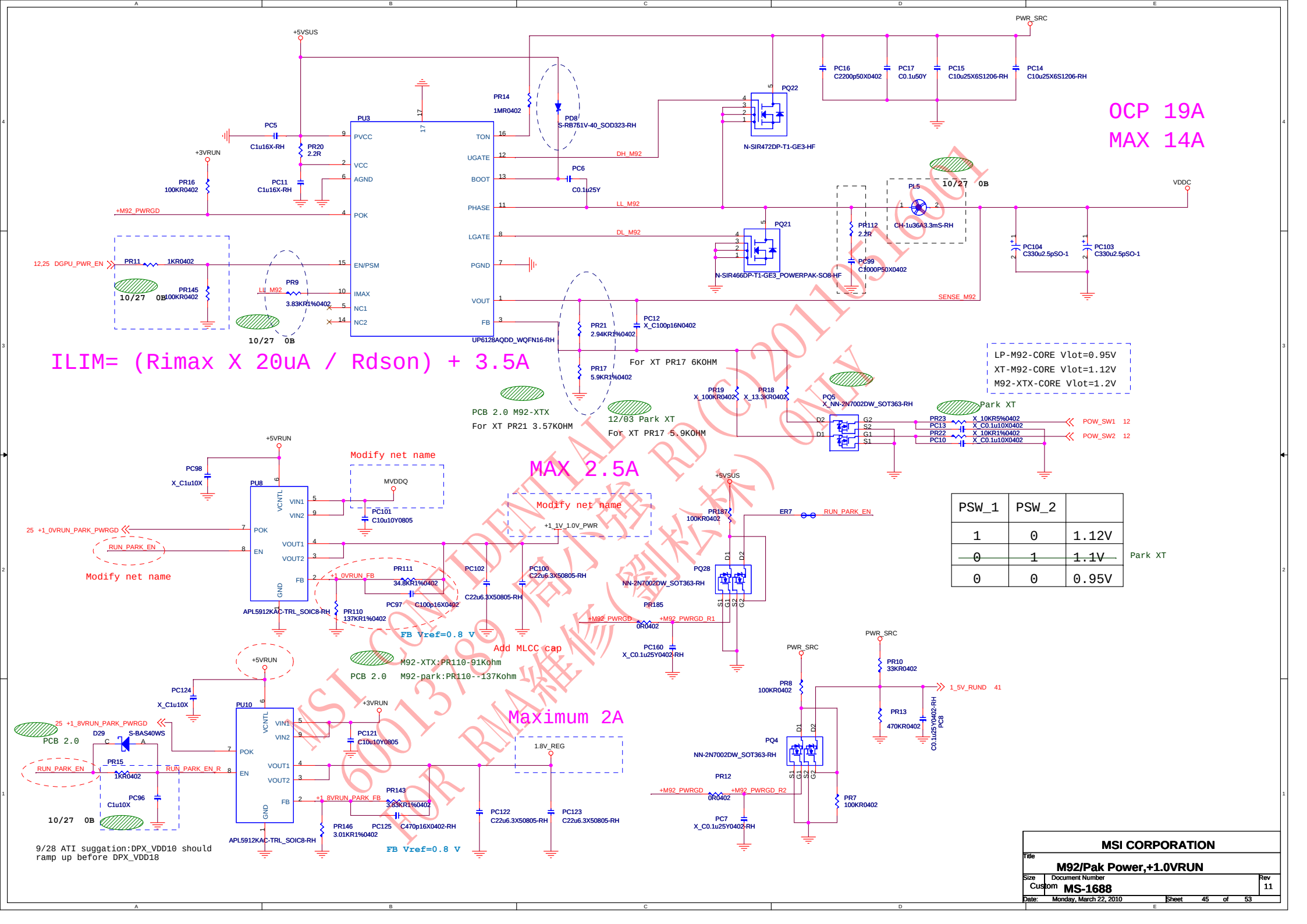

OCP 24A
MAX 18A
IMAX=18A
+3VSUS
PWR_SRC
+5VSUS
+VCC_GFXCORE
PU6
ISL62881HRZ-T_QFN28-RH
N-SIR472DP-T1-GE3-HF
N-SIR466DP-T1-GE3_POWERPAK-SO8-HF
PQ29
PQ27
PCHOKE5
CH-0.56u25A1.8mS-RH
Parallel
Parallel
Parallel
Close to Phase 1 Inductor
Rdroop
Cn
Rntc
Rsum
Ri
GPU Select voltage
+VTT
J24
COPPER
MICRO-STAR INT'L CO.,LTD.
Graphic Core
MS-1688
Monday, March 22, 2010



PSW_1	PSW_2	
1	0	1.12V
~~0~~	~~1~~	~~1.1V~~ Park XT
0	0	0.95V

MSI CORPORATION		
Title: M92/Pak Power,+1.0VRUN		
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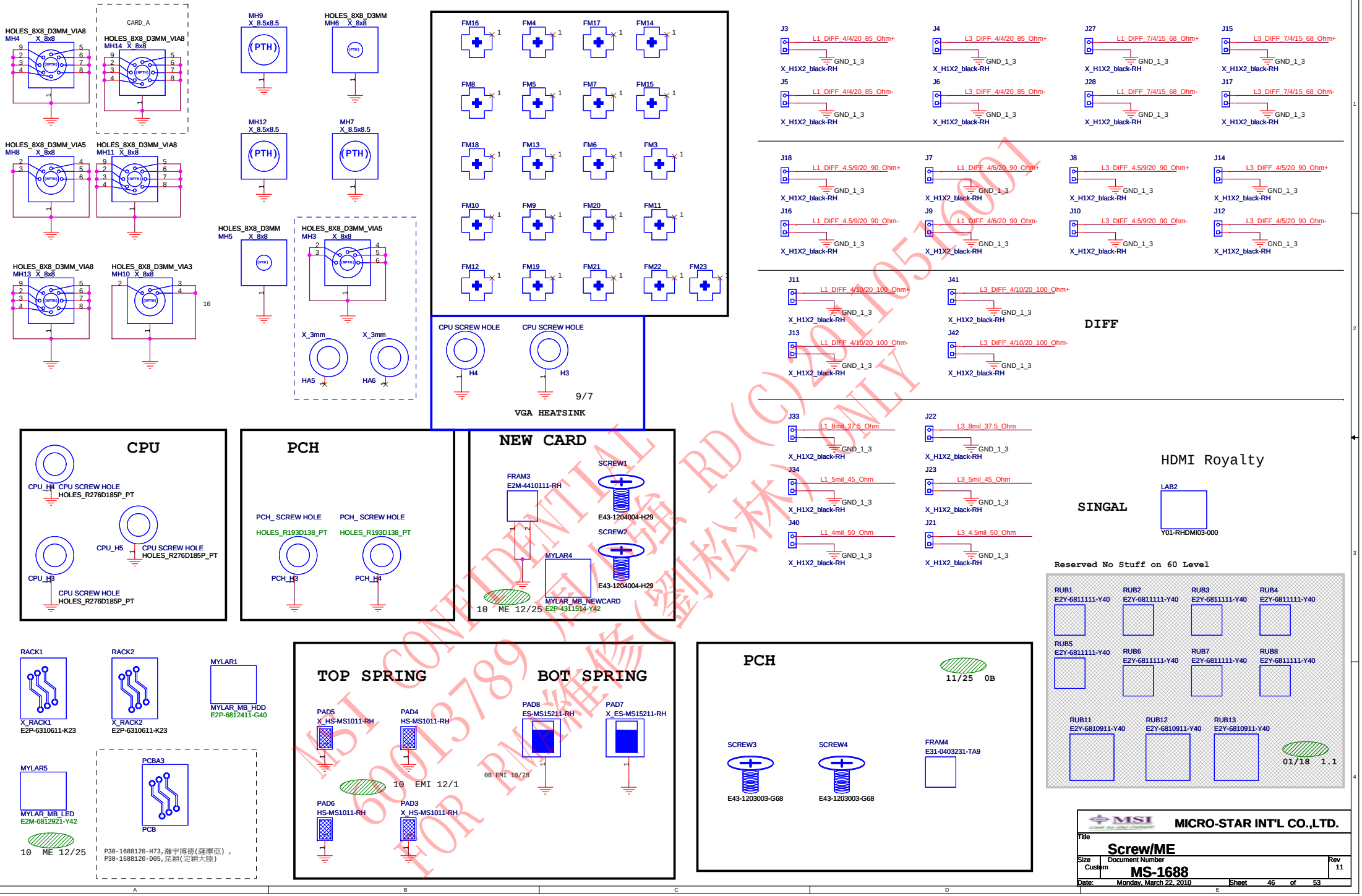

MSI MICRO-STAR INT'L CO.,LTD.

Title: Screw/ME

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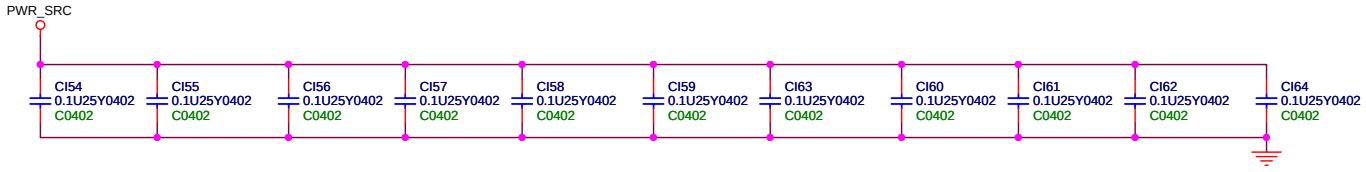

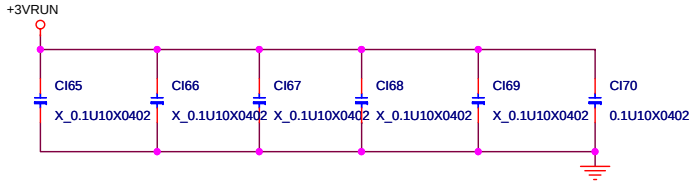

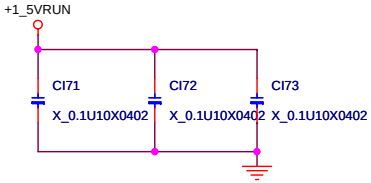

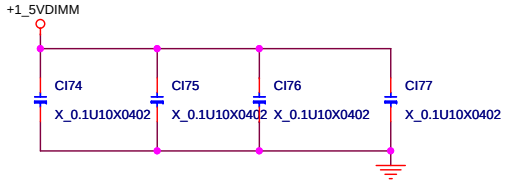

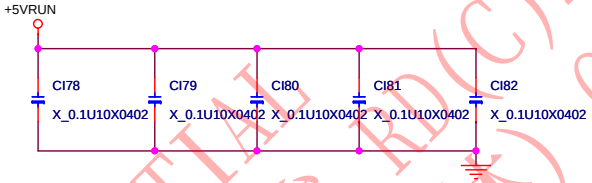

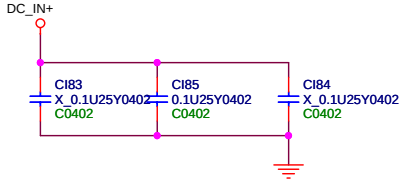

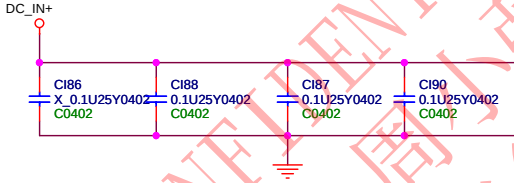

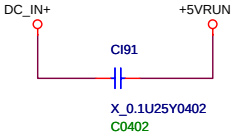

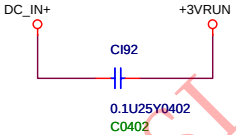

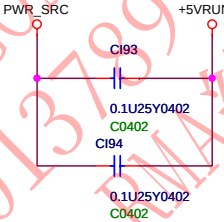

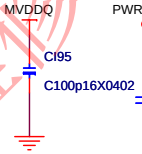

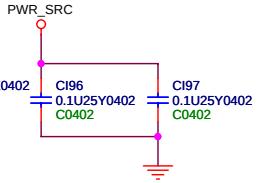

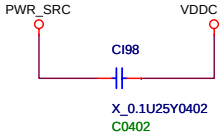

MICRO-STAR INT'L CO.,LTD.

Title: EMI

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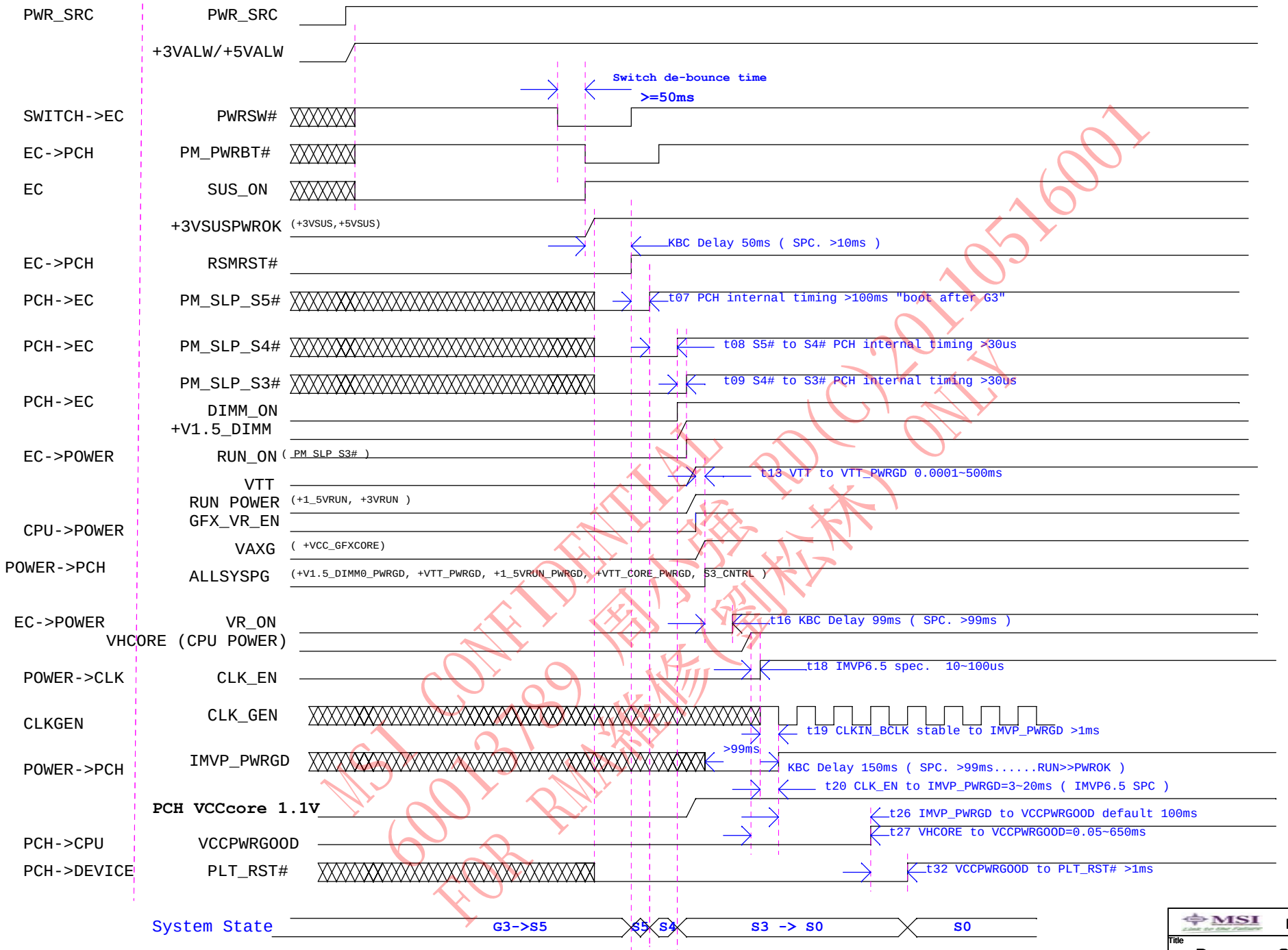
Calpella System Power on Sequence DC mode



MICRO-STAR INT'L CO.,LTD.

Title: Power on Sequency

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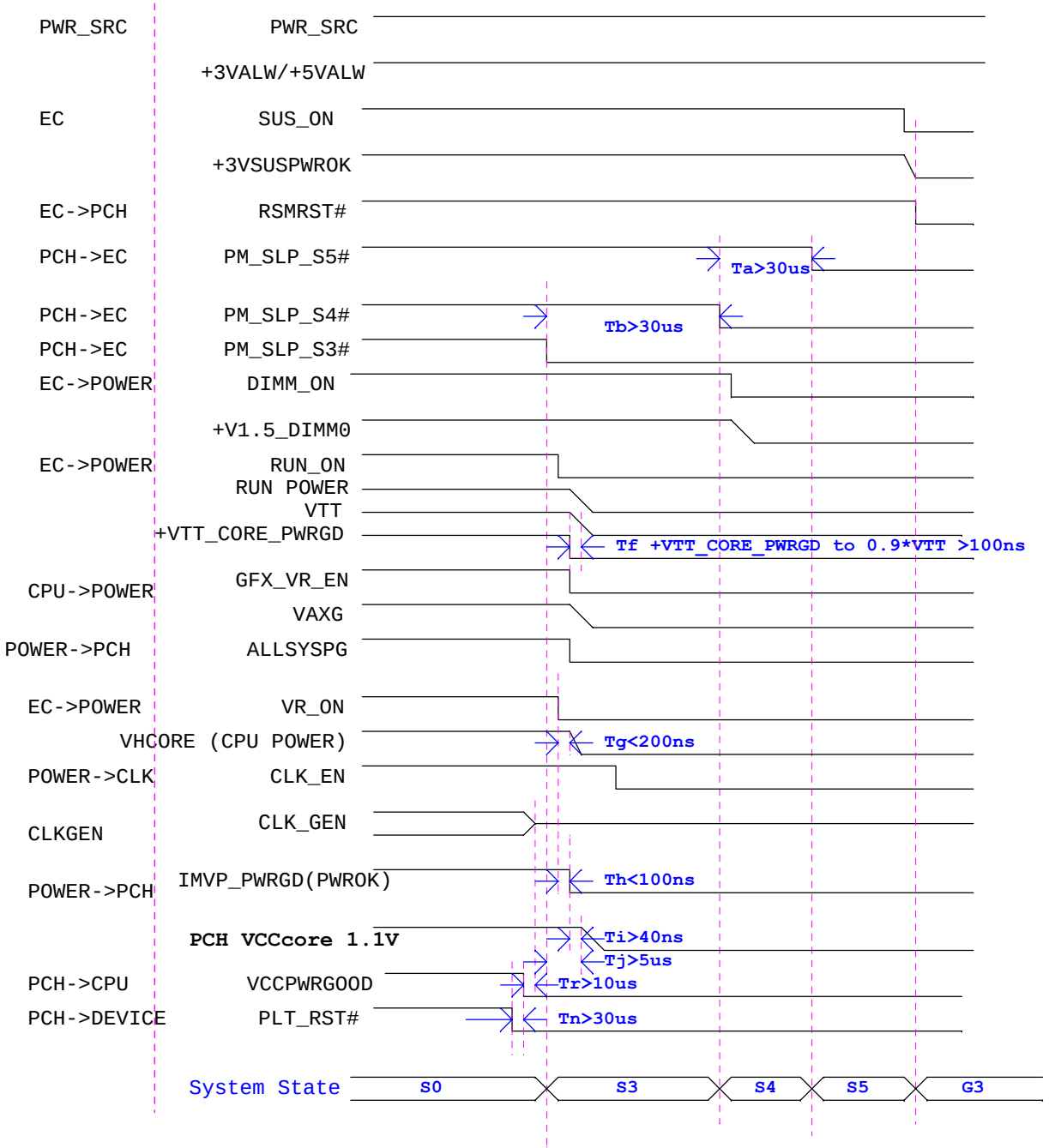
Power down Sequence DC mode S0 to G3



MSI	MICRO-STAR INT'L CO.,LTD.		
Title: Power down Sequency			
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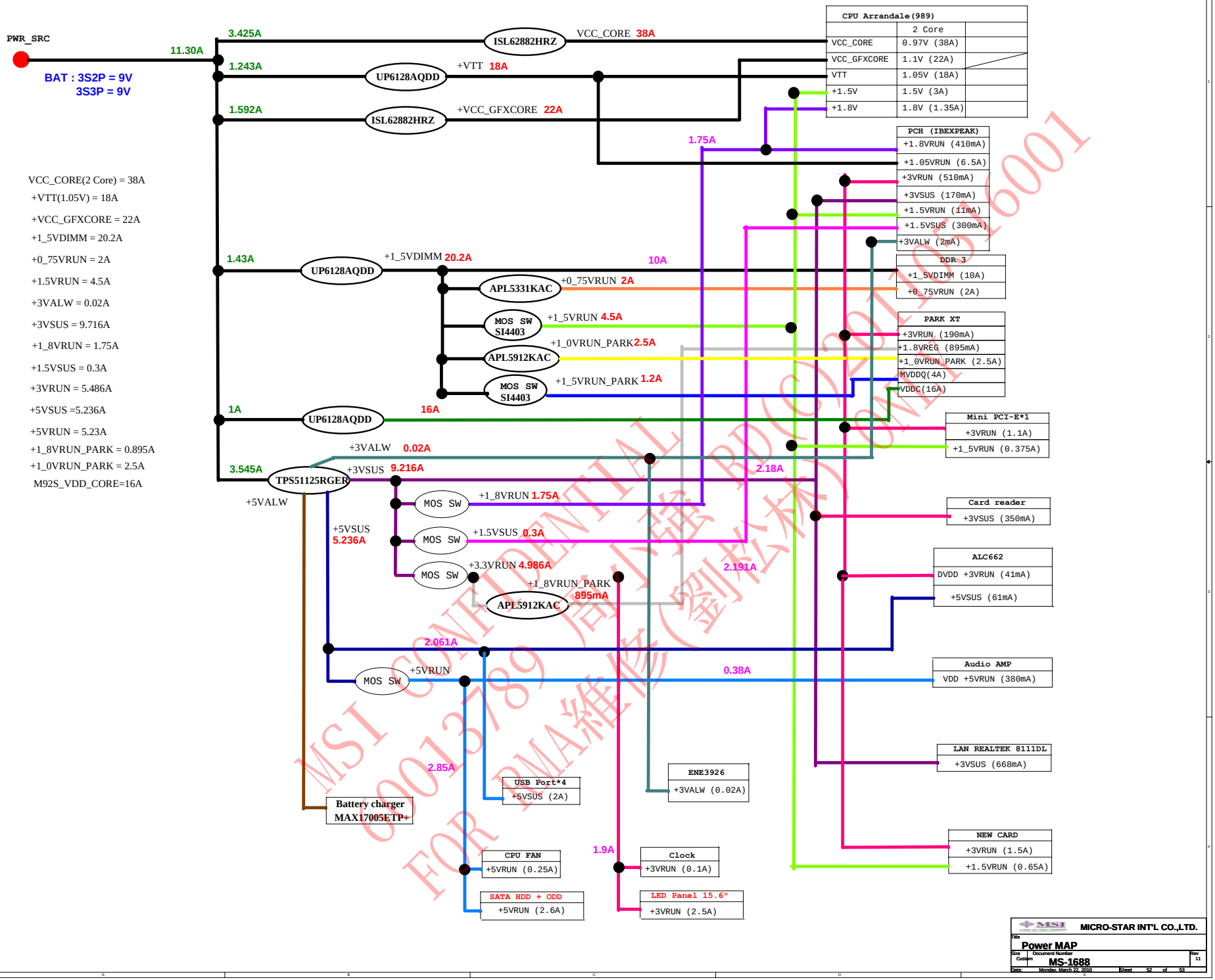

MICRO-STAR INT'L CO.,LTD.

Power MAP

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0B

1. Page 13, Add R354, R356 0 ohm for Park VDDR4 connection
2. Page 14, Stuff R92 10K ohms for GPIO2 straps
3. Page 15, Remove R50, R315
4. Page 18, Change L33~35 for CRT RGB
5. Page 19, Change D4 to BAS40 for HDMI testing
6. Page 20, Remove BIOS1 socket
7. Page 20, Add R581 1K ohms for PCH GPIO33 to EC GPIO13 connection and remove R159
8. Page 20, Change C634, C640 to 15pF
9. Page 23, Remove R108
10. Page 30, Change CON6 to vertical type for debug card
11. Page 33, Remove Q5, Q14 for Power switch LED and change R15 to 0 ohm
12. Page 34, Change J43 to eSATA connector and add C594~596, C698, C699 for eSATA solution, Remove C462
13. Page 34, Add U45, U46, C702, C704, R353, R362 for USB power protect switch and remove F4, F5
14. Page 38, Change PR183 to 4.7K to reduce the drop voltage
15. Page 39, Stuff ER46, EC102 for V_CHG
16. Page 40, Stuff PR161, PC137 for +3VSUS, PR174, PC149 for +5VSUS
17. Page 41, Stuff R247 1K ohms, No stuff R518, Change PR179 to 10.5K, R517 to 200K
18. Page 41, Stuff PR105, PC88 for +1_5VDIMM
19. Page 42, Stuff PR97, PC75 for +VTT
20. Page 43, Stuff PR35, PC26, PR34, PC21 for +VCC_CORE
21. Page 43, Change PC22 to 0.047uF, PR33 to 8.06K, PR115 to 2.32K, PR118 to 1.1K
22. Page 44, Stuff PR144, PC126 for +VCC_GFXCORE
23. Page 44, Change PC60 to 0.022uF, PC69 to 0.15uF, PR65 to 7.68K, PR73 to 18.2K, PR80 to 2.55K
24. Page 45, Change PR9 to 3.83K
25. Page 45, Stuff PR112, PC99 for VDDC and change PL5 to 1uH for reduce noise
26. Page 45, Change PR15 to 30K and stuff PC96 1uF for 1.8V_REG delay 1.2mS after +1_1V_1.0V_PWR
27. Page 45, Change PR11 to 1K and stuff PR145 100K to reduce current leakage
28. Page 46, Stuff PAD8 for EMI and add SCREW1, 2 in BOM. Remove BRAKET1
29. Page 49, Stuff CI54~64, CI70, CI85, CI87~90, CI92~97 for EMI
30. Page 16, Add PC158, PC161, Reserve C700, C701 for MVDDQ
31. Page 12, Add ATI debug point
32. Page 31, Add EMI cooper to seperate LAN GND
33. Page 32, Reserve R365 for cardreader issue
34. Page 45, Stuff PR18 13.3K, PQ5, PR23 10K for Park XT

10

1. Page 12, No stuff R118; stuff R220,R210,R169 for ATI PARK SAMPLE
2. Page 16, Remove C701 location, No stuff C64 for DFM
3. Page 16,page17, modify R322,R318,R51,R49,R324,R321,R320,R316 to 121R ohm for 3D device lost
4. Page 19, Add R11, R13, R20, R22 for GPU switch issue
5. Page 19, Add C705, C706 5pF0402 for EMI
6. Page 29, stuff R347 for ATI PARK sample
7. Page 32, Reserve R400 for ene S3 resume issue
8. Page 33, Change R26, R29 location name (Org. is R11, R13) and change the footprint to NC_0402_6
9. Page 34, Stuff CMC L3, L4 for EMI
10. Page 35, Stuff CMC LI5 for EMI, and reserve R366, R367
11. Page 44, PR74 change to 470ohm for intel ww48
12. Page 45, unstuff PR19 PQ5 PR22 ,PR17 change to 5.9Kohm fix =1.12vlot,stuff PC103 for PARK--XT
13. Page 47, Stuff CMC LIA3 for EMI, and reserve R368, R369
14. Page 48, Stuff CB3~7, JNCB3~7 for ESD
15. Page 46, Stuff PAD4, PAD6 for ESD, Add Fram4, SCREW3, SCREW4
16. Page 46, ADD mylar4;mylar5 for newcard and led ESD

11

1. page 6 remove R506;page 11 R434,R435 modify cooper;page 12 remove R95,R522,R399,R406,R407 ; page 13 unstuff R354,R356
2. page 15 remove R76,R70;page 19 stuff R11,R13,R20,R22,;unstuff R81,U14,C113
3. page 23 remove R148,R144;page 26 remove R192
4. page 29 modify pn:SLG28770ELC
5. page 30 add GPIO3F :2P_CHG;GPIO0D MB/ID;GPXIOA06:PRE_CHG;AC_OK change to AC_IN#;modify R351 to cooper
6. page 31 reomove R106,R103,R133;modify R145,R104 to cooper
7. page 32 reomove R223;page 34 remove R353,R352,R362,R363
8. page 38 modify AC_OK to AC_IN#
9. page 39 modiy MAX 8724 charge IC
10. page 43 ,page44 modiy PC119 ,PC72 to digital GND
11. page 49 ,No Stuff CI62
12. page 32 ,Change U25 PN to Ver:A3
13. page 46 ,Add Rubber Rub1~8, Rub11~13 to 60 level for IE request

PCB 2.0 base on pcb 1.0

9. page 19 un-stuff U14,C113,R81,R80
10. page 23 un-stuff R144,R148;page 26 Remove R192
11. page 30 add GPIO3F :2P_CHG;GPIO0D MB/ID;GPXIOA06:PRE_CHG;AC_OK change to AC_IN# ;ADD R362 R352 FOR AC_IN#;modify R351 to cooper
12. page 32 Remove R223 ;page 34 remove R353,R352,R362,R363
13. page 38 modify AC_OK to AC_IN#
14. page 39 modiy MAX 8724 charge IC;PR190 PR191 0 ohm;un-stuff pc165 pc166
15. page 48 modiy 1688B un-stuff PCB3 ,remove CB8
16. page 46 Add MYLAR1 PN:E2P-6812411-G40
17. page 43 modify imon current PC22=0.068 uf ,PR33=5.49kohm

2010/03/11 Add BIOS Lable, HDMI Royalty, MS-1688B switch change to 4.9mm
Stuff R11, R13, R20, R22

MSI CORPORATION		
Title: Change Histoy		
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