Compal Confidential

GPT52 MB
SCHEMATIC DOCUMENT

LA-K201P

2020-09-18 REV 1.0

Security Classification	Compal Secret Data		
Issued Date	2019/05/07	Deciphered Date	2019/12/31

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Title	Cover Sheet	
Size	Document Number: LA-K201P	Rev 1.0
Date: Monday, September 14, 2020	Sheet 1 of 100	

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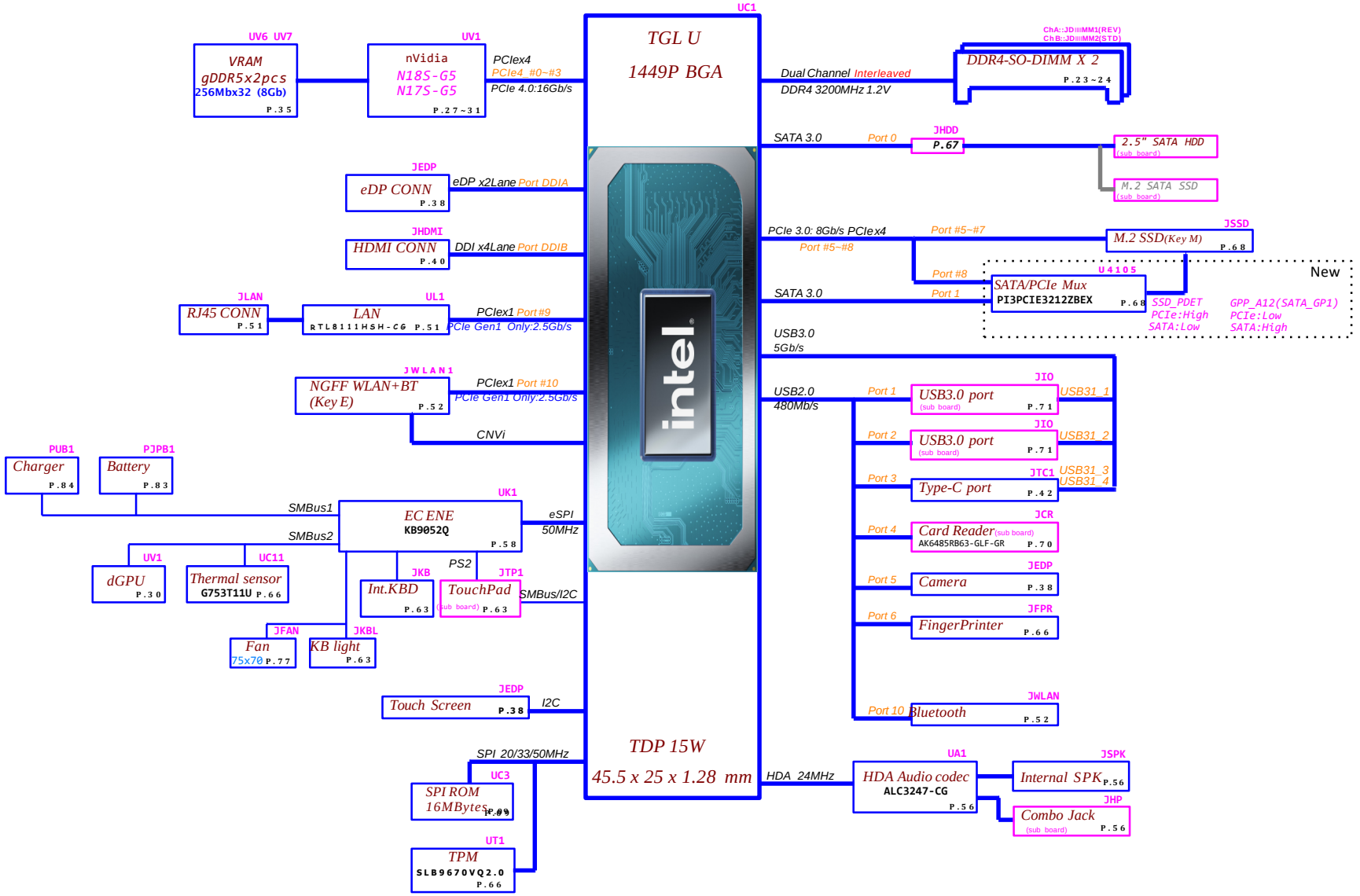
Model Name: TGL-U

Project Name: LA-K201P



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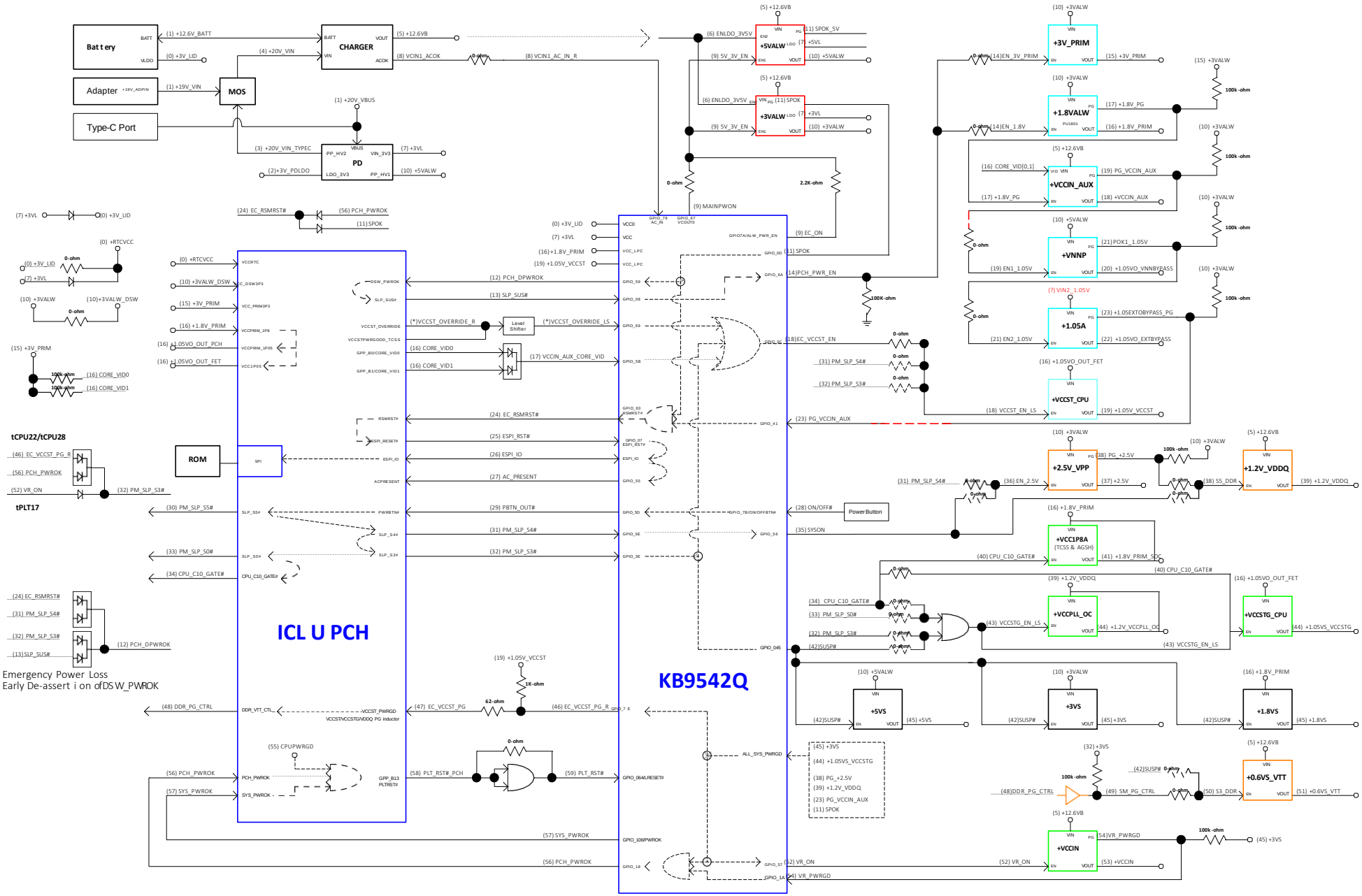
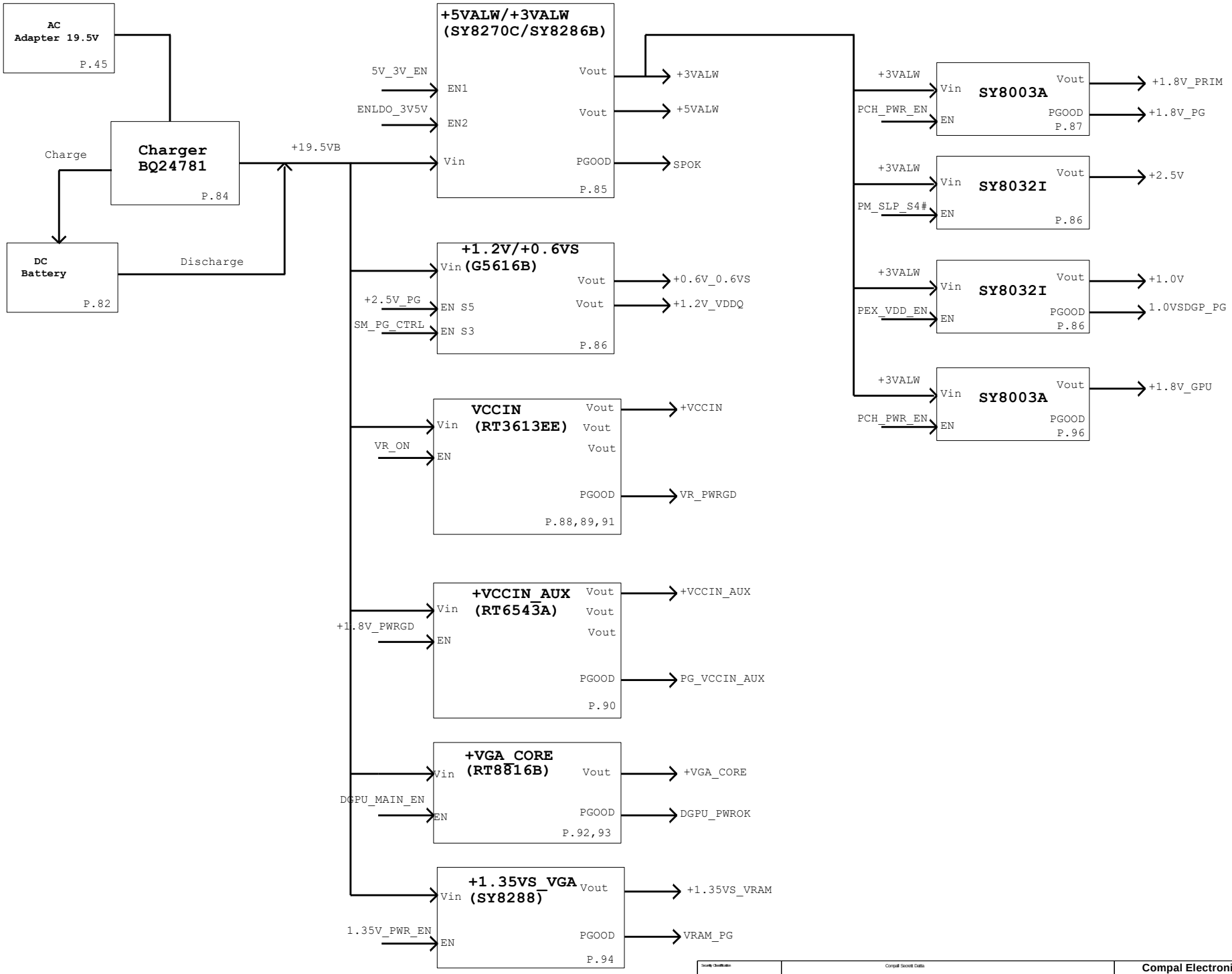
Title: **TGL-U 4+2 Block Diagrams**

Size: Document Number: **LA-K201P** Rev: 1.0

Date: Monday, September 14, 2020 Sheet 2 of 100



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/08/05	Deciphered Date	2015/08/17
			P075 - AC_Power up Sequence
			Document Number: LA-K201P
			Rev: 1.0
Date: Monday, November 16, 2015			Sheet 5 of 55



Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

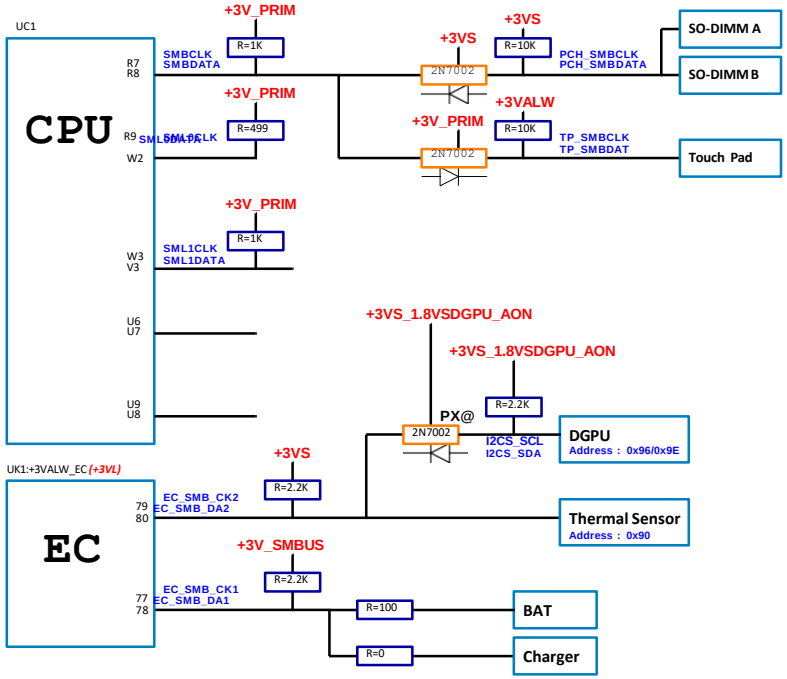
Power Block Diagram

2019OPP TGL

V0.3

Monday, September 14, 2020

81 100



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Issued Date	2018/05/17	Deciiphered Date	2021/05/17

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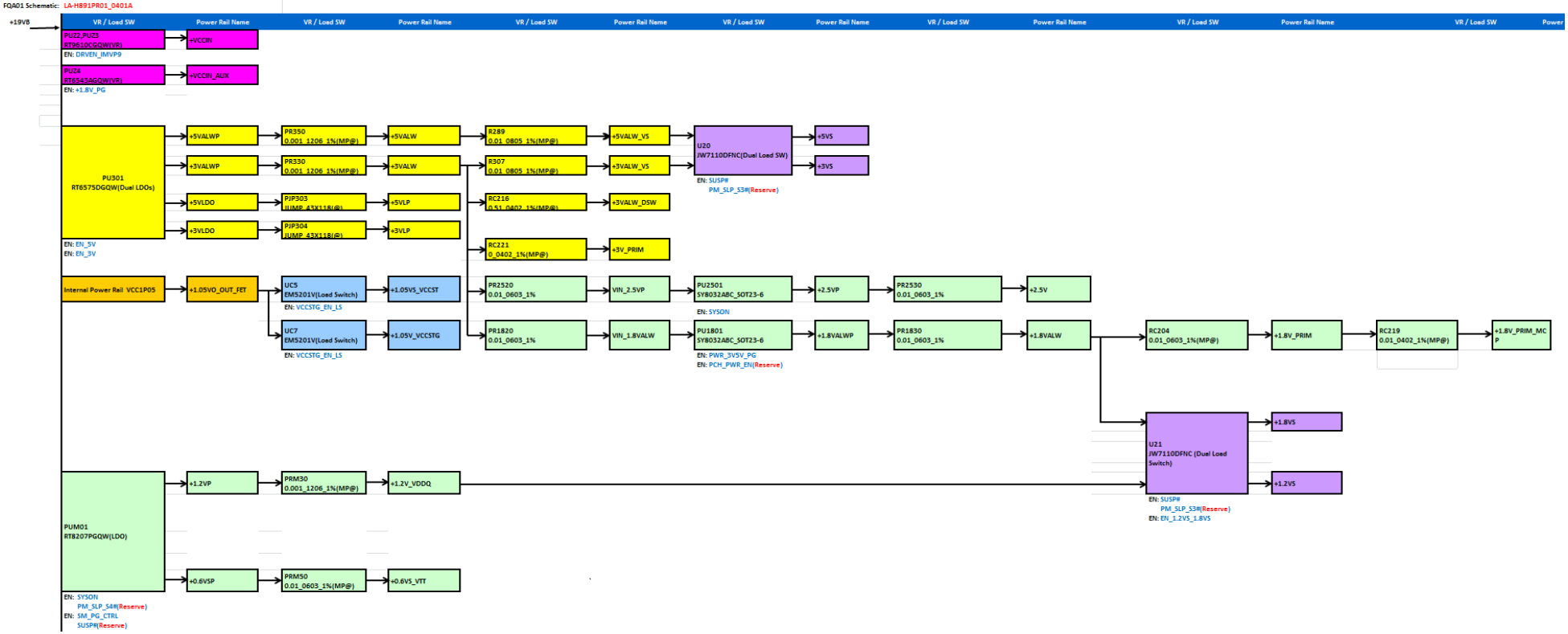
Compal Electronics, Inc.			
Title: Notes List			
Size: Custom	Document Number: LA-K201P		Rev: 1.0
Date: Monday, September 14, 2020		Sheet: 3 of 100	

[FQA01-Power Map_TGL-UP3_DDR4_Volume_S0ix]

FQA01 Schematic: LA-H891PR01_0401A



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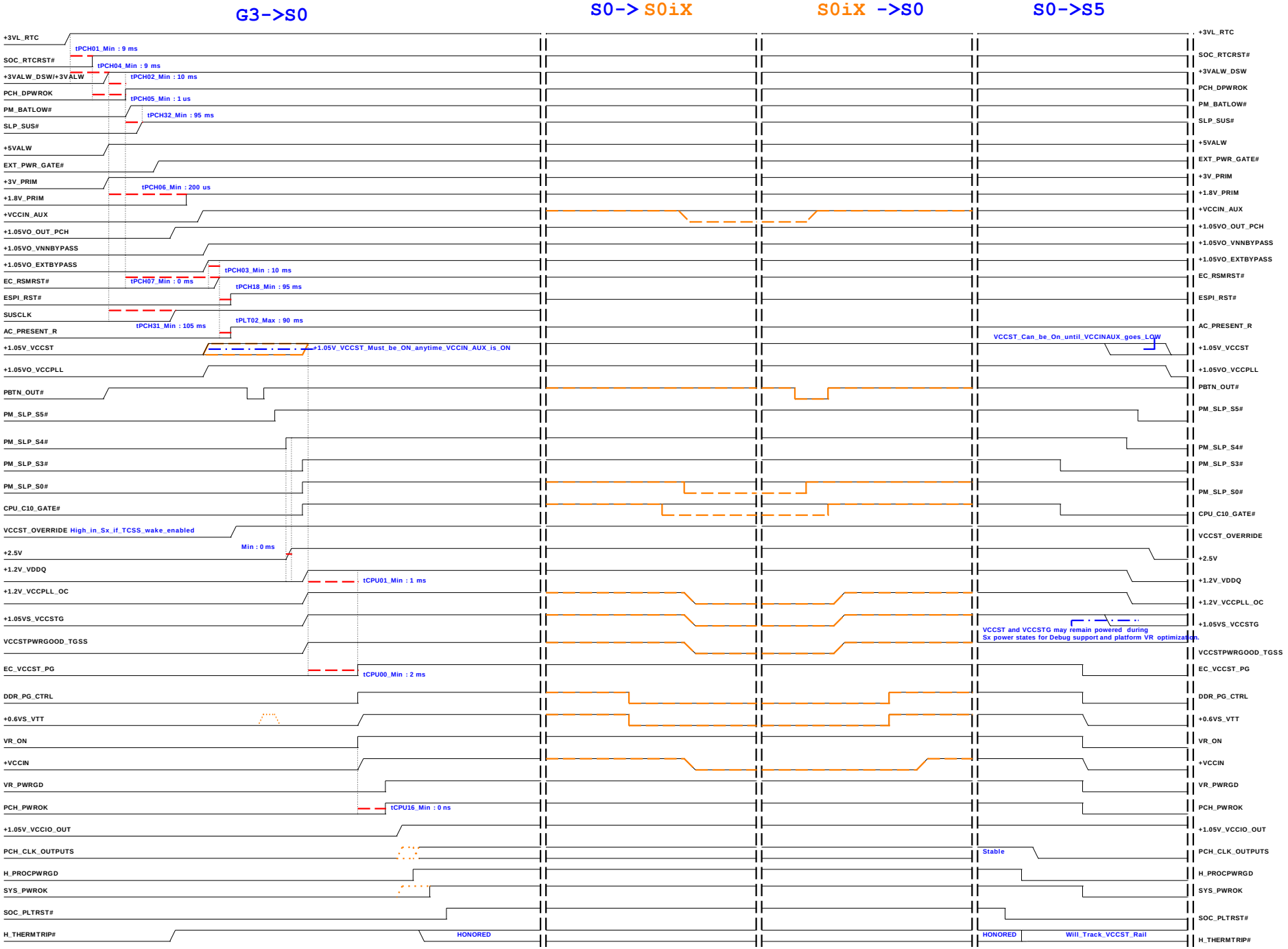
Title: Power MAP		
Size: Document Number: LA-K201P		Rev: 1.0
Date: Monday, September 14, 2020	Sheet 4 of 100	

[FQA01-PWR Sequence_TGL-UP3_DDR4_Volume_S0iX]

Will be Update



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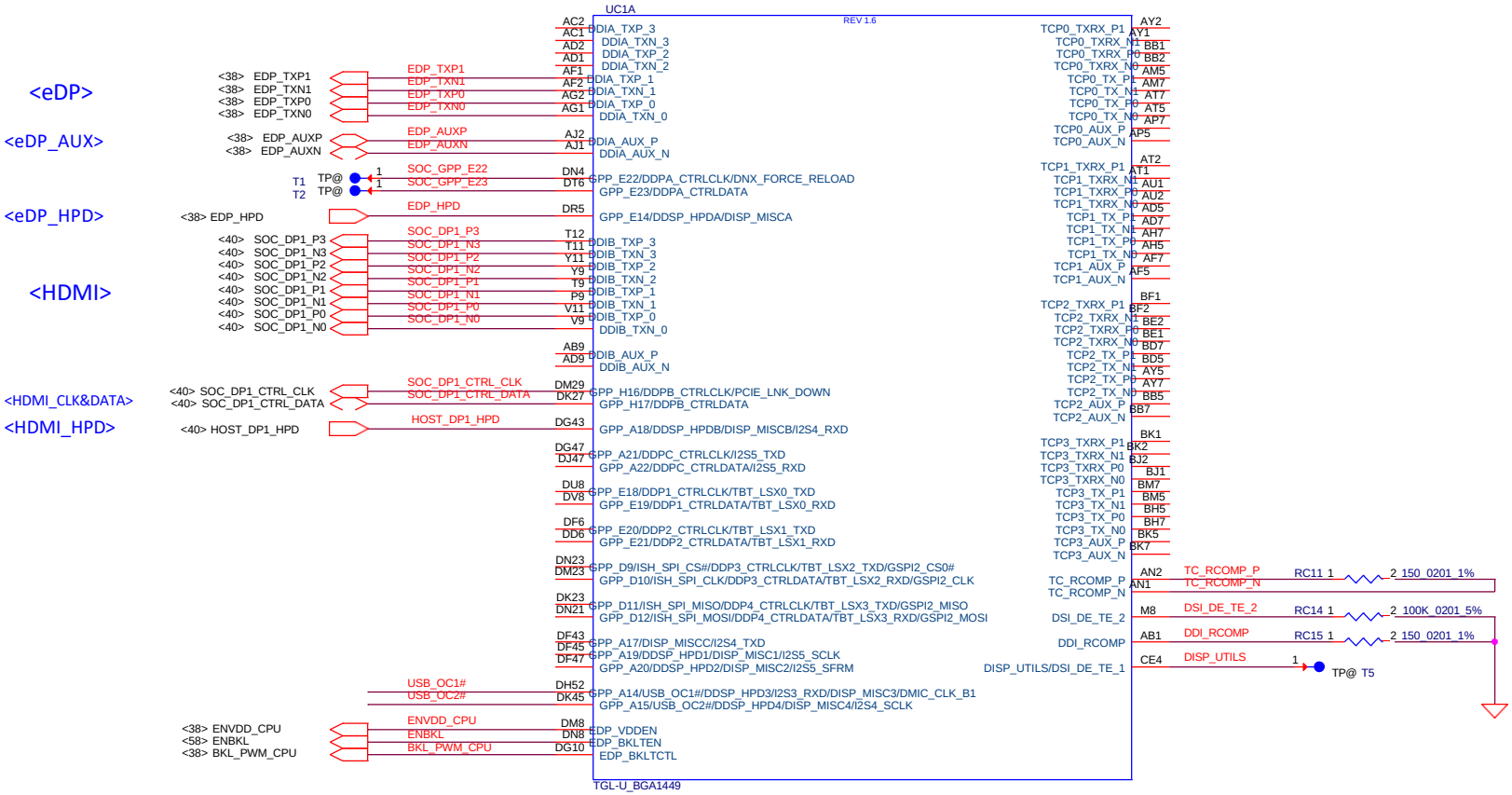

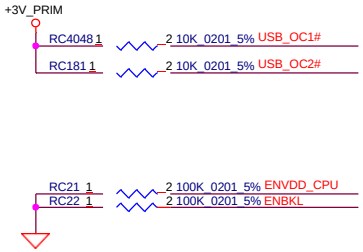

Table 32. USB3/USB2 Port Pairing for USB-C* Connectors

	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

To make split xDCI controller working functionally for different USB-C* connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C* connectors, but it is not strictly required.

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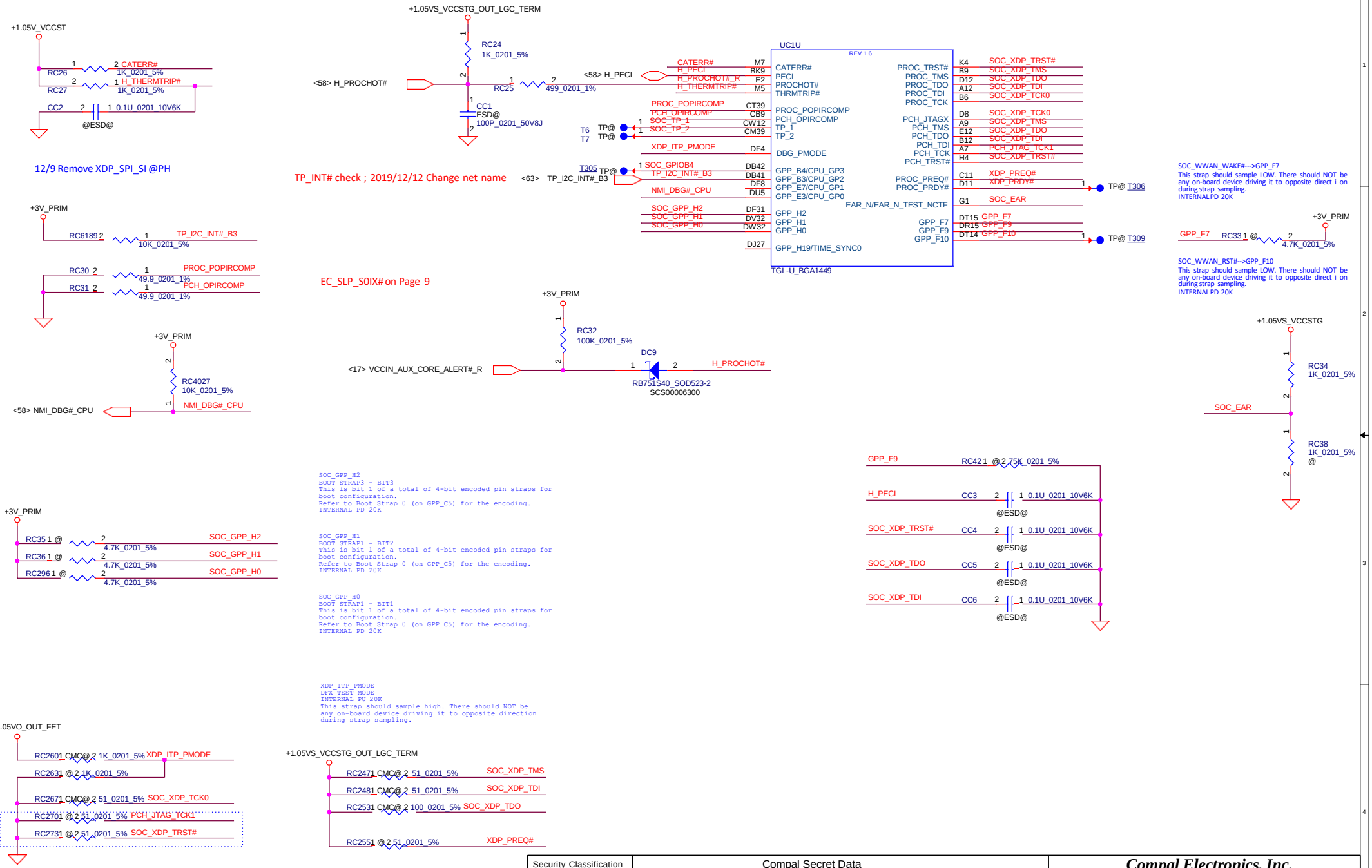
Title: TGL-UP3(1/14)DDI,EDP

Size: D | Document Number: LA-K201P | Rev: 1.0

Date: Monday, September 14, 2020 | Sheet 6 of 100



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Compal Electronics, Inc.

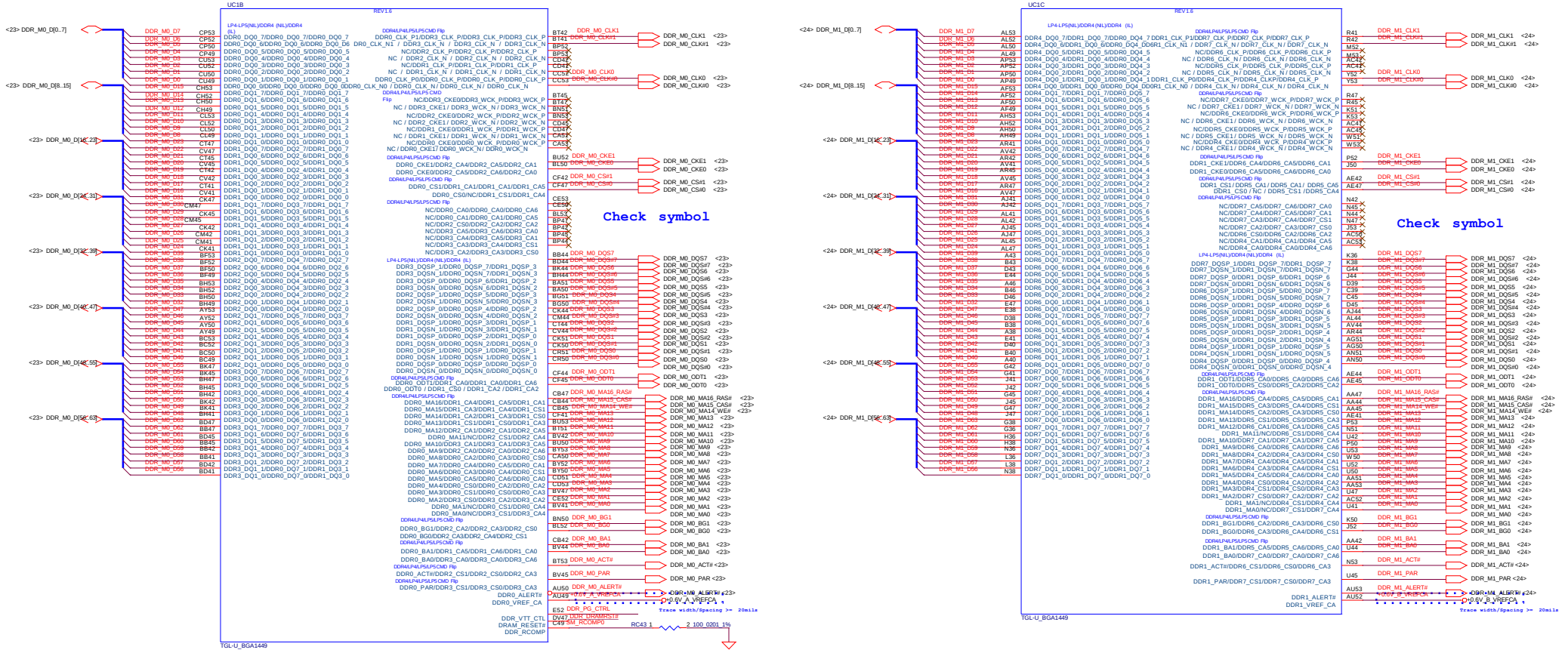
Title: **TGL-UP3(1/14)DDI,MSIC,XDP**

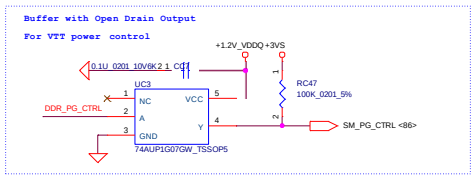
Size	Document Number	Rev
	LA-K201P	1.0

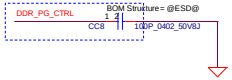
Date: Wednesday, September 16, 2020 Sheet 7 of 100

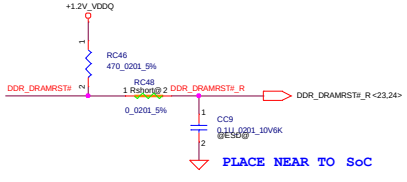
Follow Intel DDR4 NIL

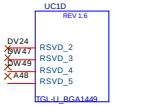
DDR4: Refer to 609003_TGL_U_DDR4_SODIMM_RVP_SCH_REV0p5











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Title: **TGL-UP3(3/14)DDR4**

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SOC_SPI_0_D0
BOOT HALT
NO INTERNAL PU/PD
HIGH: ENABLED
LOW: DISABLED

SOC_SPI_0_D2
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
NO INTERNAL PU/PD

SOC_SPI_0_D3
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
NO INTERNAL PU/PD

SOC_GPP_C2
TLS CONFIDENTIALITY
INTERNAL PD 20K
HIGH: TLS CONFIDENTIALITY ENABLE
LOW: TLS CONFIDENTIALITY DISABLE(Default)

2019/12/12 Change net name

SOC_SML0ALERT#
ESPI OR EC LESS
INTERNAL PD 20K
HIGH: ESPI DISABLE
LOW: ESPI ENABLE
This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).

SOC_THC_0_RST#
JTAG ODT DISABLE
NO INTERNAL PU/PD
HIGH: JTAG ODT ENABLED
LOW: JTAG ODT DISABLED

UC1E
REV1.6
TGL-U_BGA1449

SOC_GPP_B23
CPUNSSC CLOCK FREQ
INTERNAL PD 20K
HIGH: 19.2 MHz (form internal divider)
LOW: 38.4 MHz (direct form crystal) (Default)

Follow 607872_TGL_UY_PDG for Glitch

Single SPI ROM_CS0#

Follow 607872_TGL_UY_PDG

16M SPI ROM(Support ISH)

UC2 SO8@ W25Q128JVSIQ_SO8 SA00005VV20

UC2 WSON@ W25Q128JVPIQ WSON SA00007XA10

MAF - Master Attached Flash
Single SPI Flash attached to SPI Bus
EC FW access through eSPI Bus

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Title: TGL-UP3(4/14)SPI,ESPI,SMB,LPC

Size: A3 | Document Number: LA-K201P | Rev: 1.0

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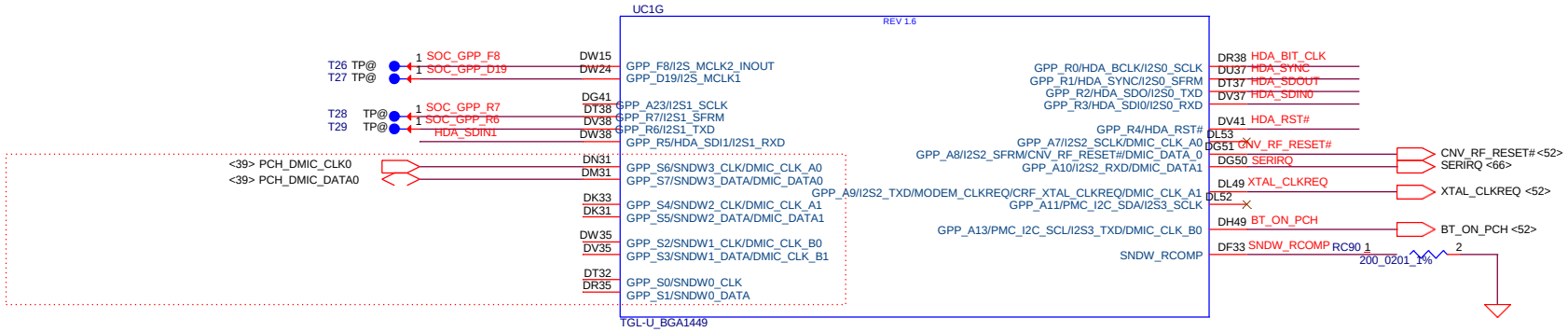
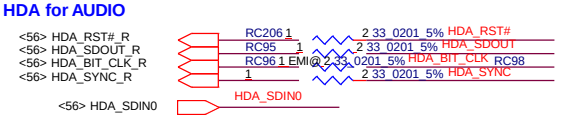
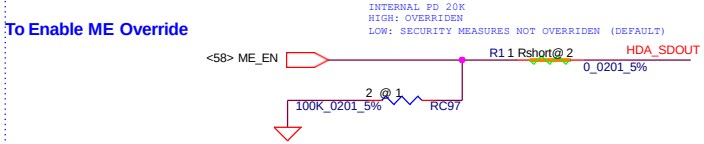
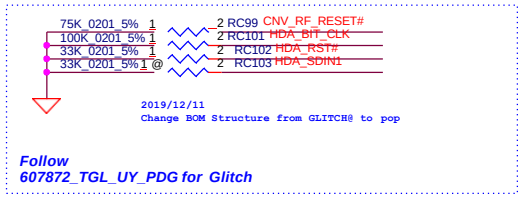


HDA for AUDIO



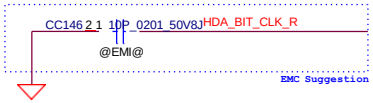
To Enable ME Override





Follow
607872_TGL_UY_PDG for Glitch

572631_ICL_PCH_LP_EDS_Vol_1_Rev_0p7
VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO



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Title: **TGL-UP3(5/14)HDA,SNDW**

Size: Document Number: **LA-K201P** Rev: 1.0

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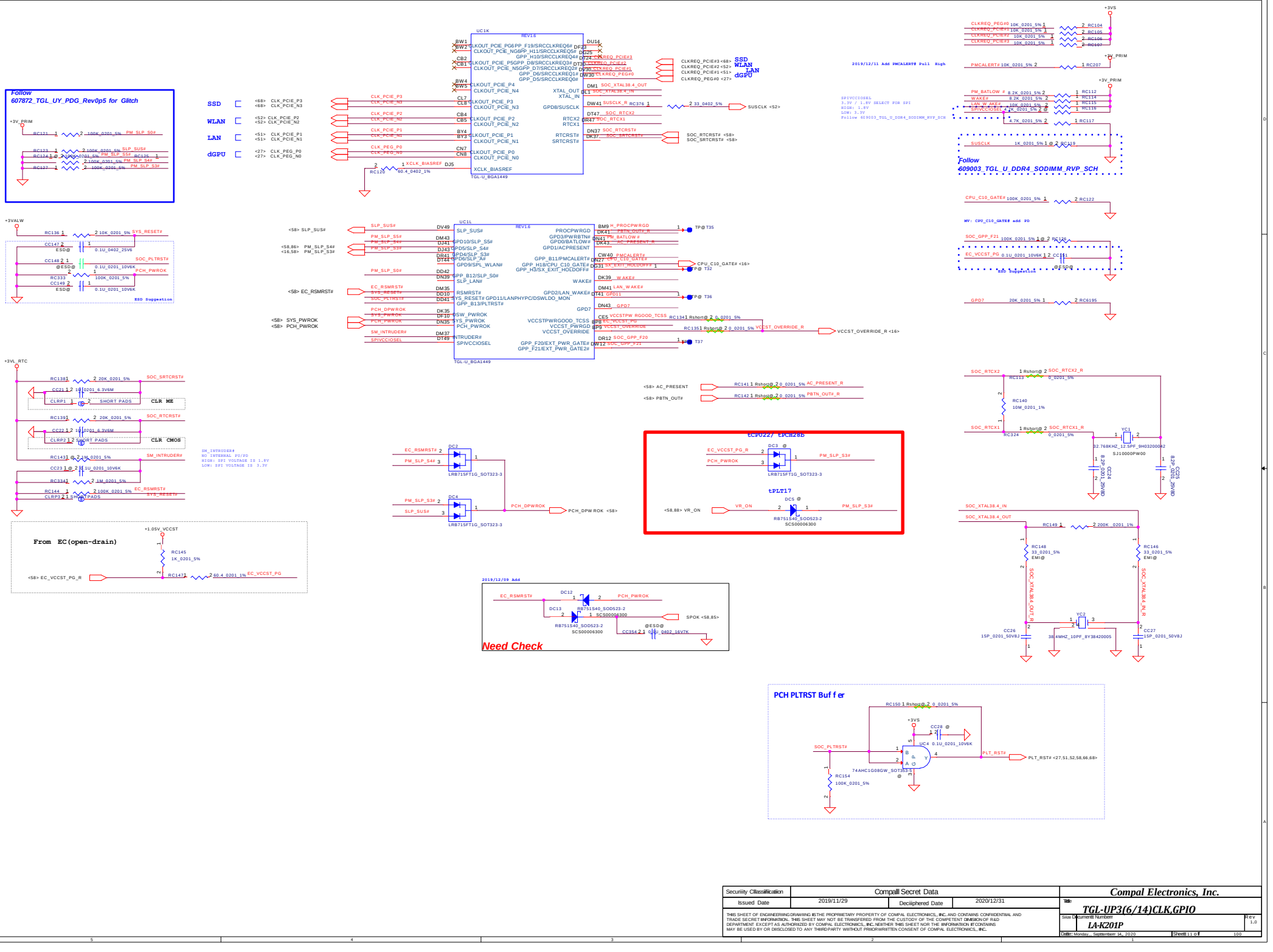
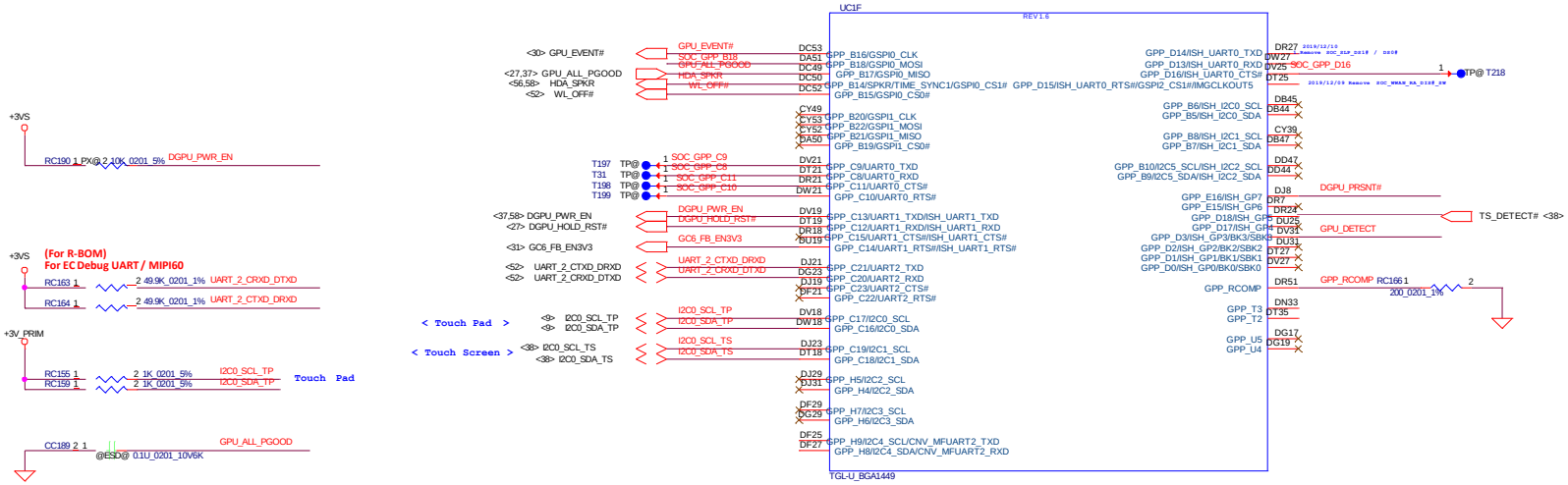
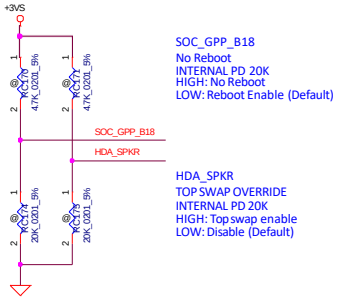

Follow
607872_TGL_UY_PDG_Rev0p5 for Glitch
SSD
WLAN
LAN
dGPU
UC1K
TGL-U_BGA1449
SUSCLK <52>
Follow
609003_TGL_U_DDR4_SODIMM_RVP_SCH
UC1L
From EC(open-drain)
Need Check
PCH PLTRST Buffer
Compall Secret Data
Compal Electronics, Inc.
TGL-UP3(6/14)CLK,GPIO
LA-K201P



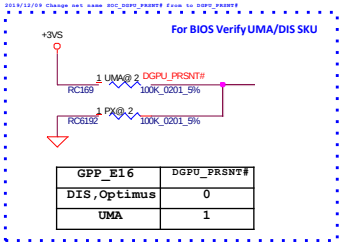
Strap Pin



SOC_GPP_B18
No Reboot
INTERNAL PD 20K
HIGH: No Reboot
LOW: Reboot Enable (Default)

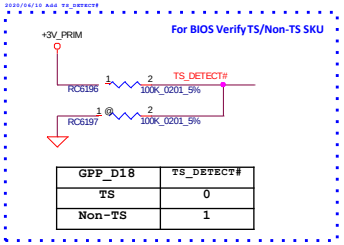
HDA_SPKR
TOP SWAP OVERRIDE
INTERNAL PD 20K
HIGH: Top swap enable
LOW: Disable (Default)

2019/12/09 Change net name SOC_DGPU_PRSNT# from to DGPU_PRSNT#



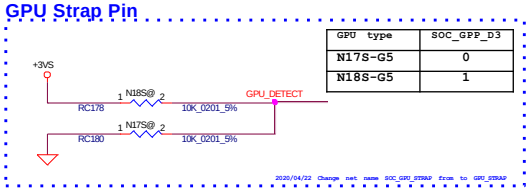
GPP_E16	DGPU_PRSNT#
DIS,Optimus	0
UMA	1

2020/04/10 Add TS_DETECT#



GPP_D18	TS_DETECT#
TS	0
Non-TS	1

GPU Strap Pin



GPU type	SOC_GPP_D3
N17S-G5	0
N18S-G5	1

2020/04/22 Change net name SOC_GPU_STRAP from to GPU_STRAP

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Title: TGL-UP3(7/14)GPIO

Size: Document Number: LA-K201P

Rev: 1.0

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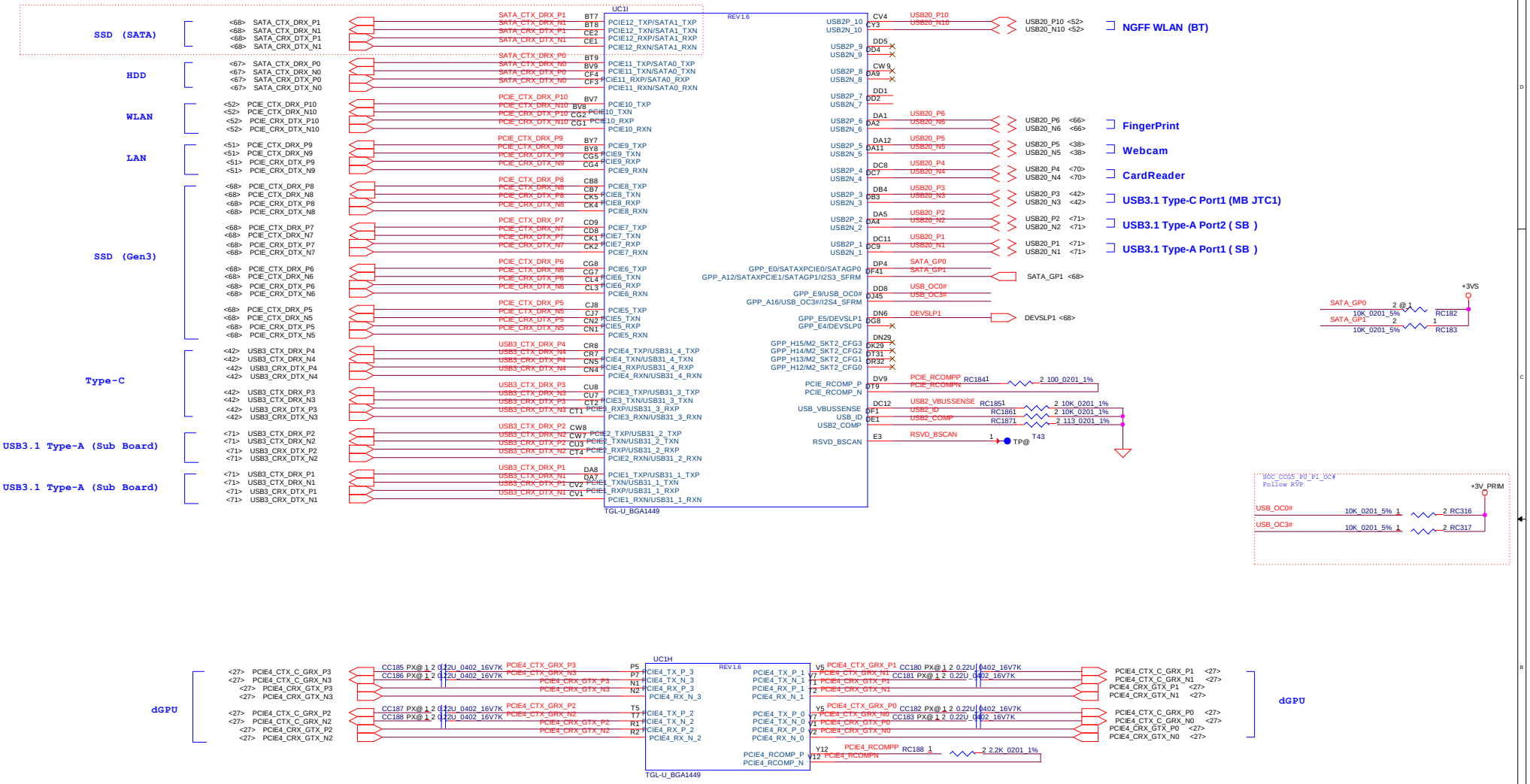

Table 58. Signal Descriptions

Name	Type	SSC Capable	Description
PCH-LP (U): • CLKOUT_PCIE_P[6:0] • CLKOUT_PCIE_N[6:0] PCH-LP (Y): • CLKOUT_PCIE_P[6:1] • CLKOUT_PCIE_N[6:1]	O	Yes	**PCI Express* Clock Output**: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices • CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1/2/3 support • CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support

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Compal Electronics, Inc.

Title: TGL-UP3(8/14)PCIE,USB,SATA

Size: LA-K201P | Document Number | Rev: 1.0

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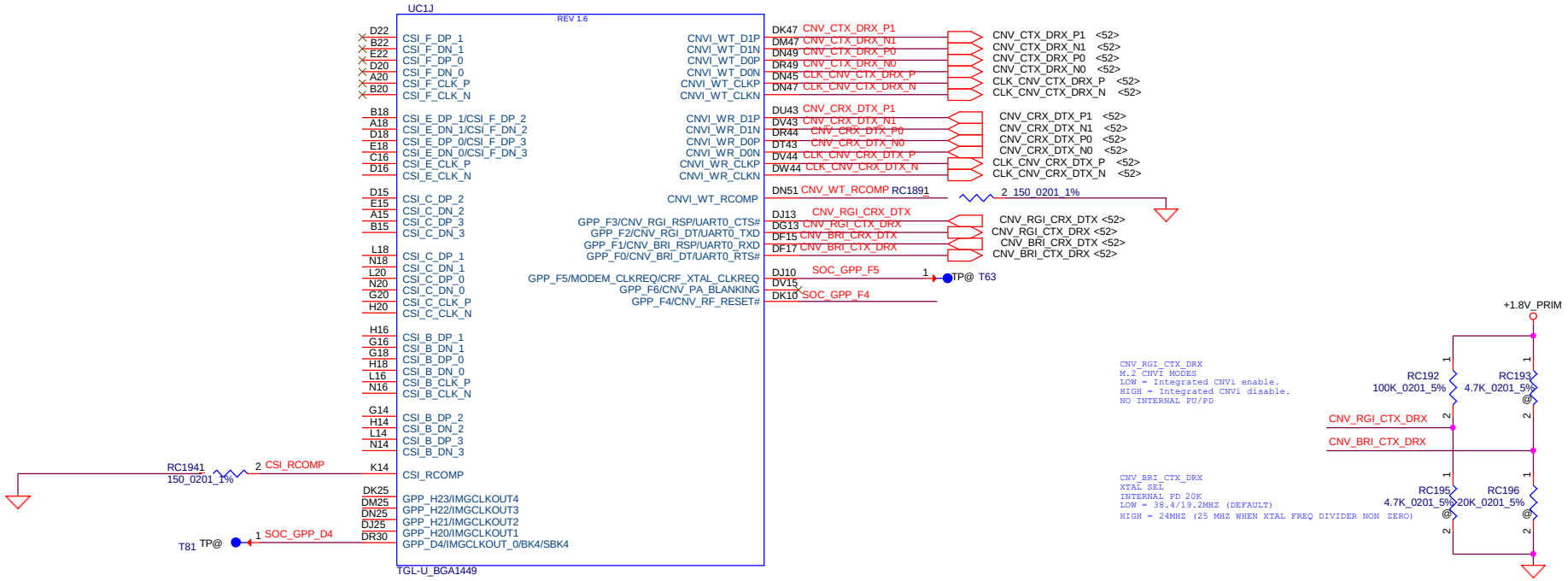

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Compal Electronics, Inc.

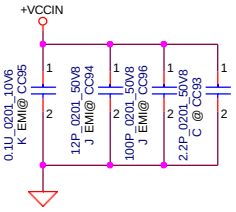
Title: **TGL-UP3(9/14)CSI,CNV**

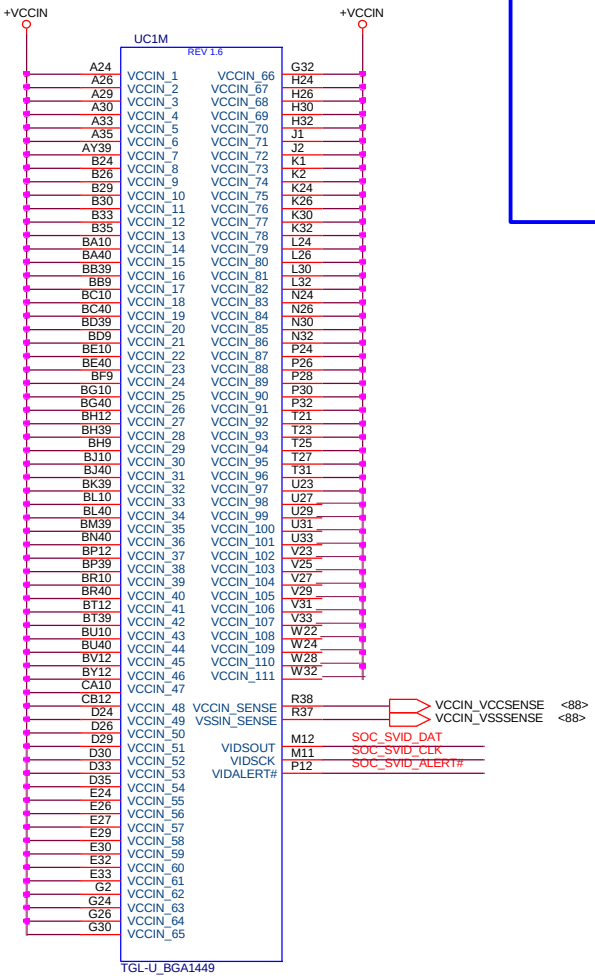
Size | Document Number: **LA-K201P** | Rev: 1.0

Date: Monday, September 14, 2020 | Sheet 14 of 100

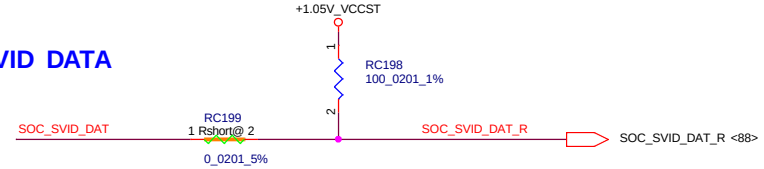
Package size?

EMC CAPS-PLACE
< 5mm from SOC VCCIN





SVID DATA



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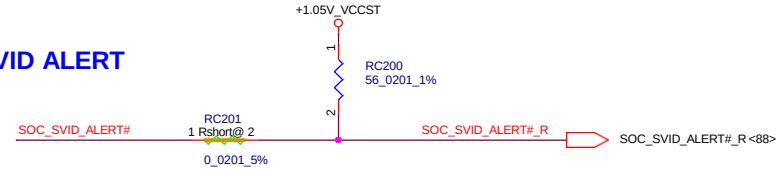
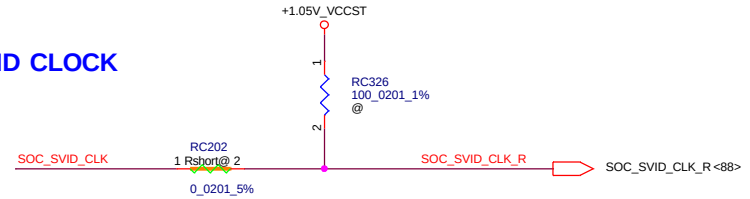


SVID CLOCK



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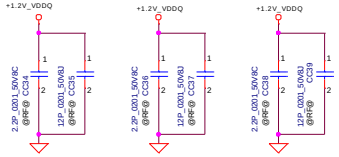
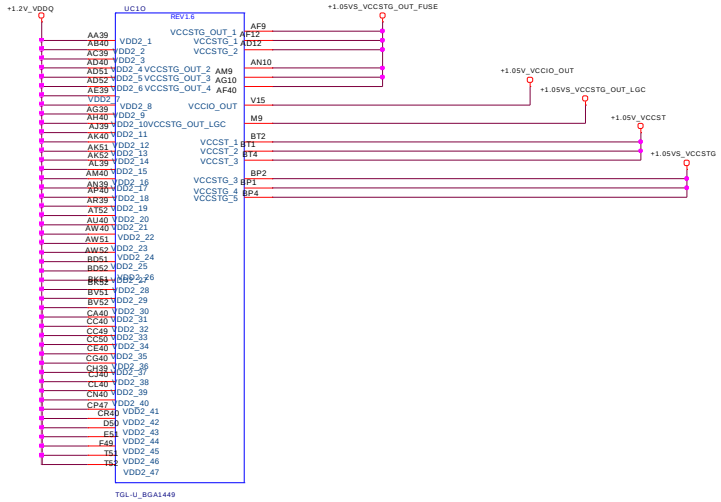
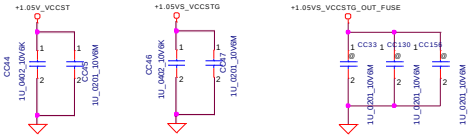
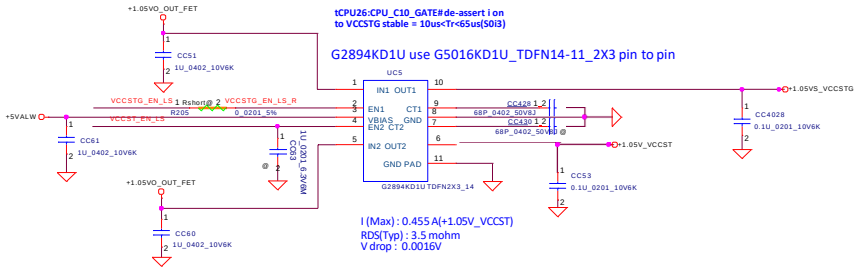
EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 3 (EMI@)
2.2pF* 3 (EMI@)

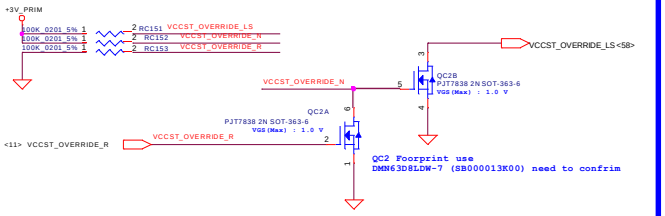


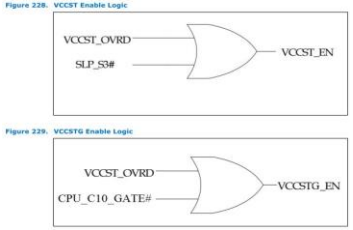




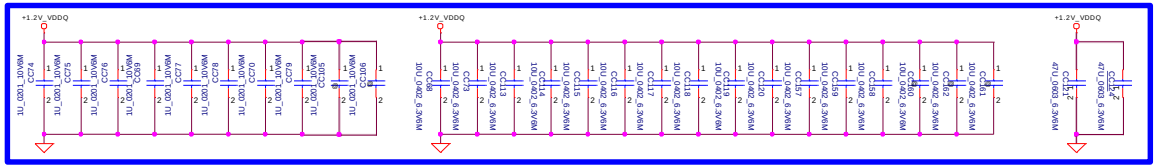
12/23 VCCST/VCCSTG change to dual load switch



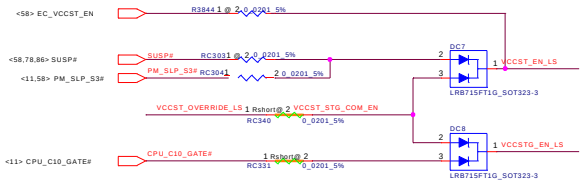




Place on CPU Side
1uF* 10
10uF* 16
47uF * 2



VCCST/VCCSTG Enable



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Title: TGL-UP3(11/14)Power

Size: Document Number: LA-K201P Rev: 1.0

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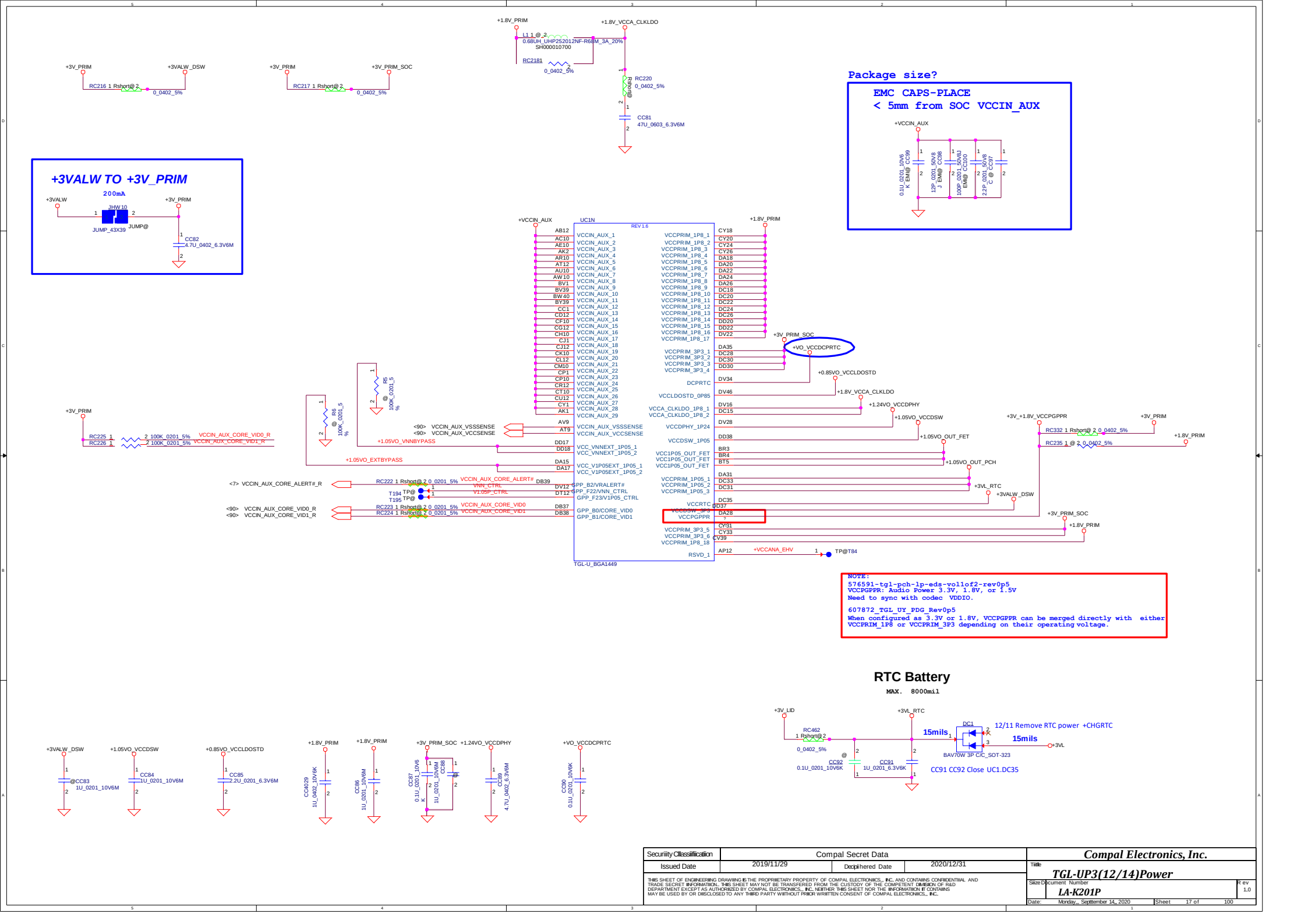

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Title: **TGL-UP3(12/14)Power**

Size	Document Number	Rev
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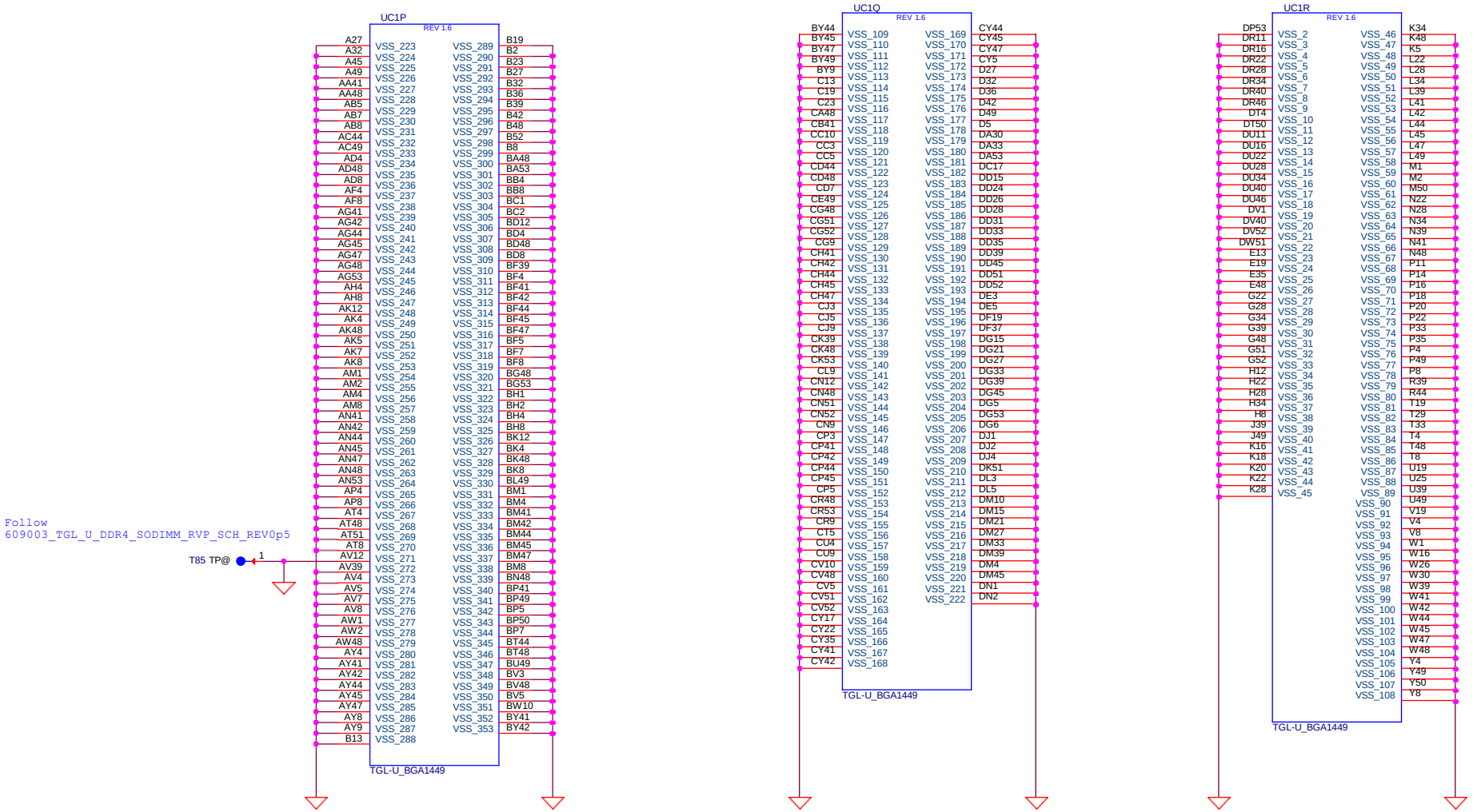

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Compal Electronics, Inc.

Title: **TGL-UP3(13/14)GND**

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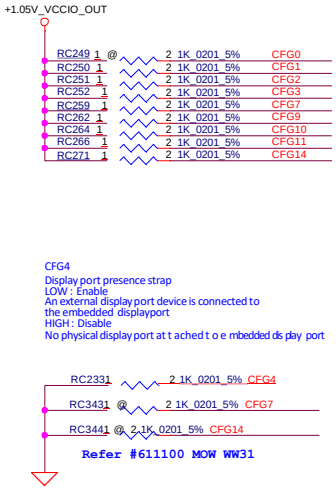
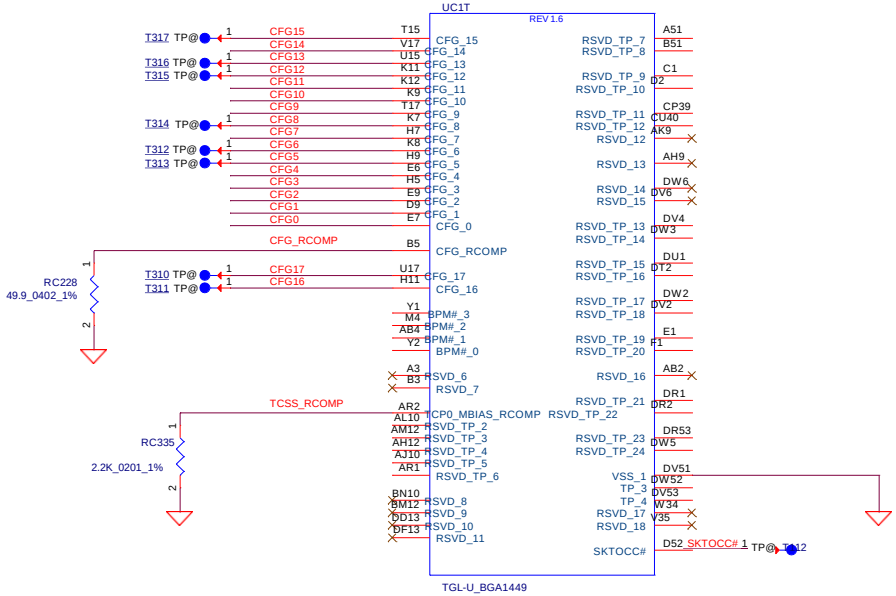
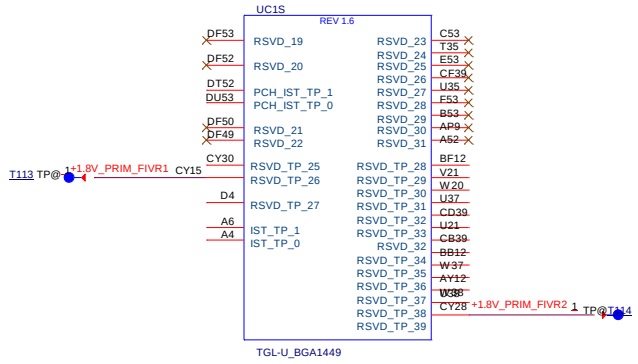
12/10 Refer 607872_TGL_UP3_UP4_PLATFORM_DOCUMENT_REV1.0 Page114

CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

Processor BPM#[3:0] nets can be left floated when not use for debug. Processor CFG[19:0] and PCH chipset test interfaces might have dual purpose usage. From







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Title: **TGL-UP3(14/14)RSVD,CFG**

Size: Document Number: **LA-K201P** Rev: 1.0

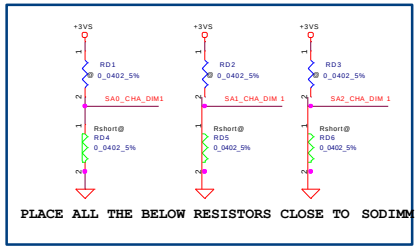
Date: Monday, September 14, 2020 Sheet 19 of 100

CHANNEL-M0

REVERSE TYPE

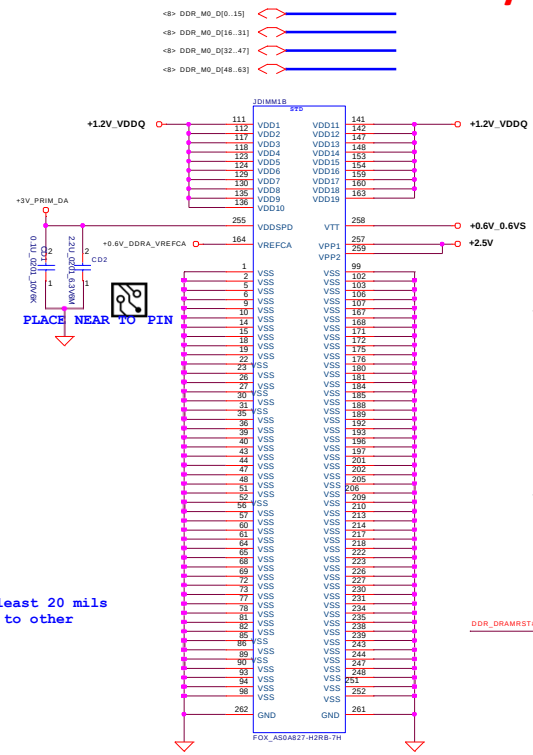
Non-Interleaved Memory

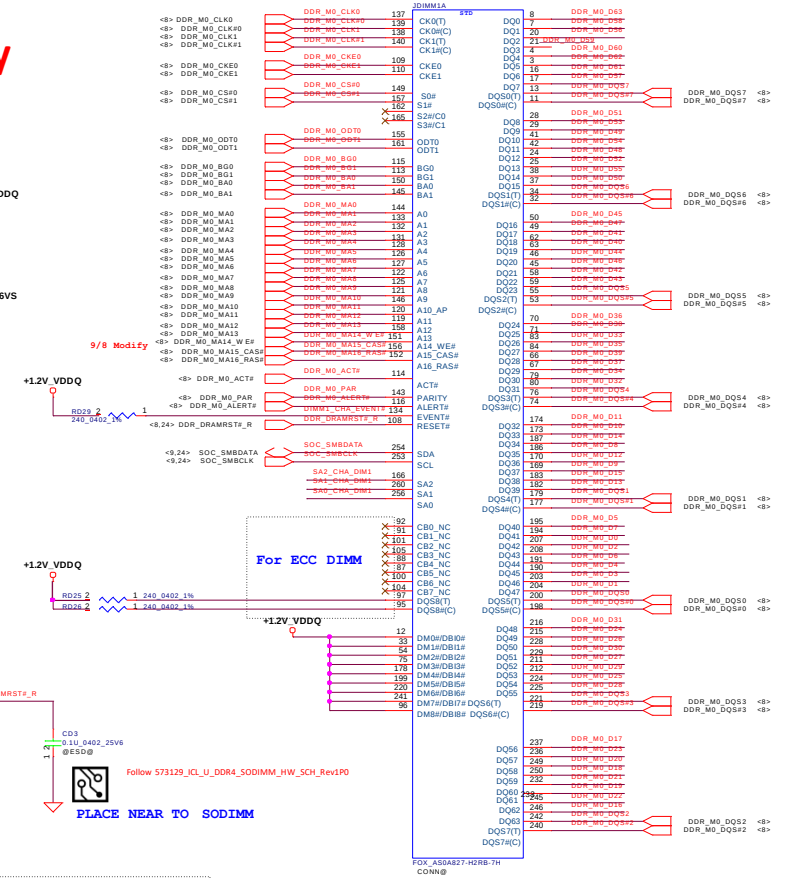
TOP: JDIMM1 CONN Non-ECC DIMM

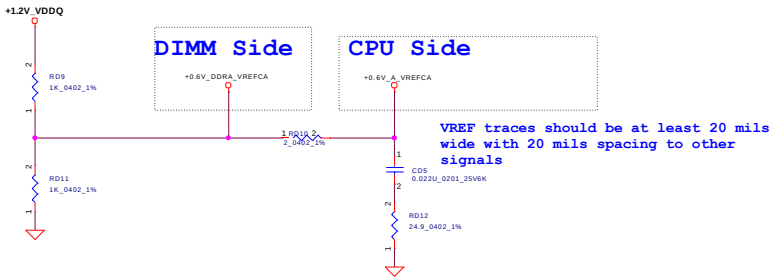


SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

12/16 Remove RD32

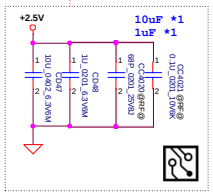




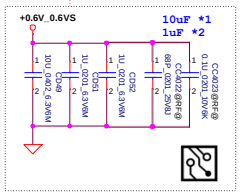


Decoupling Cap._Channel A

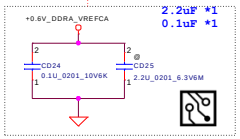
Layout Note:
Place near JDIMM2.257,259

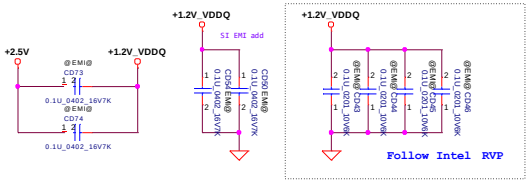


Layout Note:
Place near JDIMM2.258

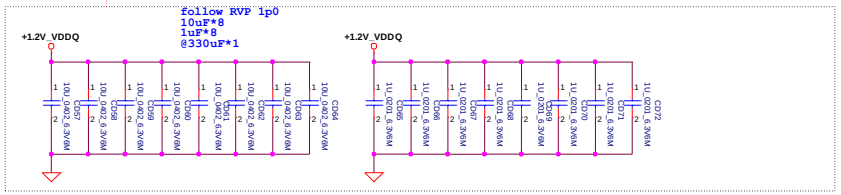


Layout Note:
PLACE THE CAP near JDIMM2. 164

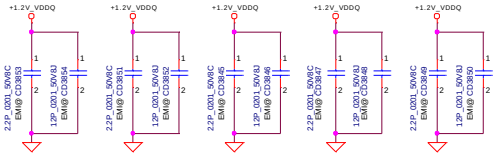




Layout Note:
Place near JDIMM2



EMC CAPS-PLACE
< 4mm from SO-DIMM VDDQ
with each pair < 12mm Apart
12pF* 5 (EMI@)
2.2pF* 5 (EMI@)



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Title: DDR4 CHM0: DIMM0		
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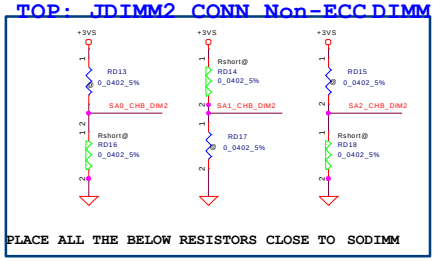
CHANNEL-M1

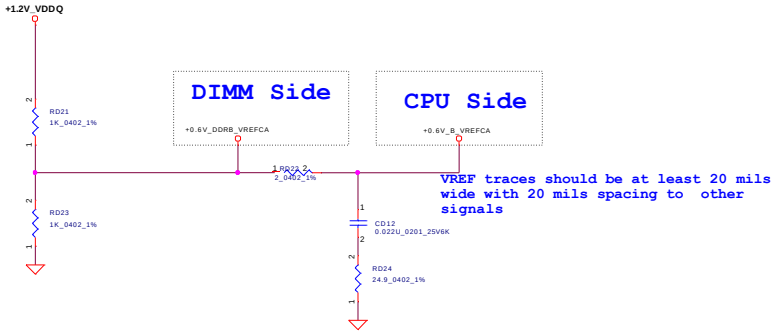
Non-Interleaved Memory

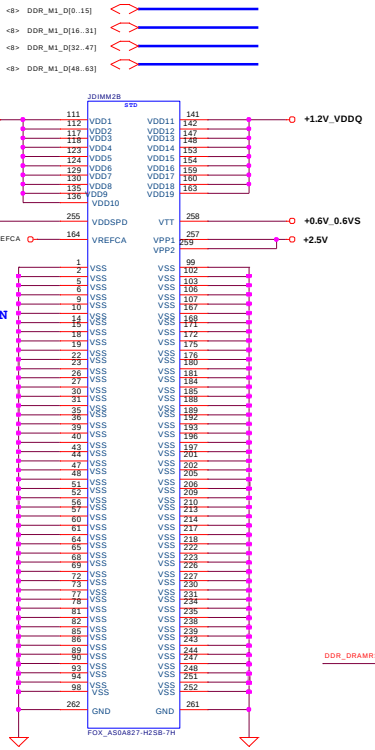
STD (5.2 mm)

TOP: JDIMM2_CONN_Non-ECC DIMM

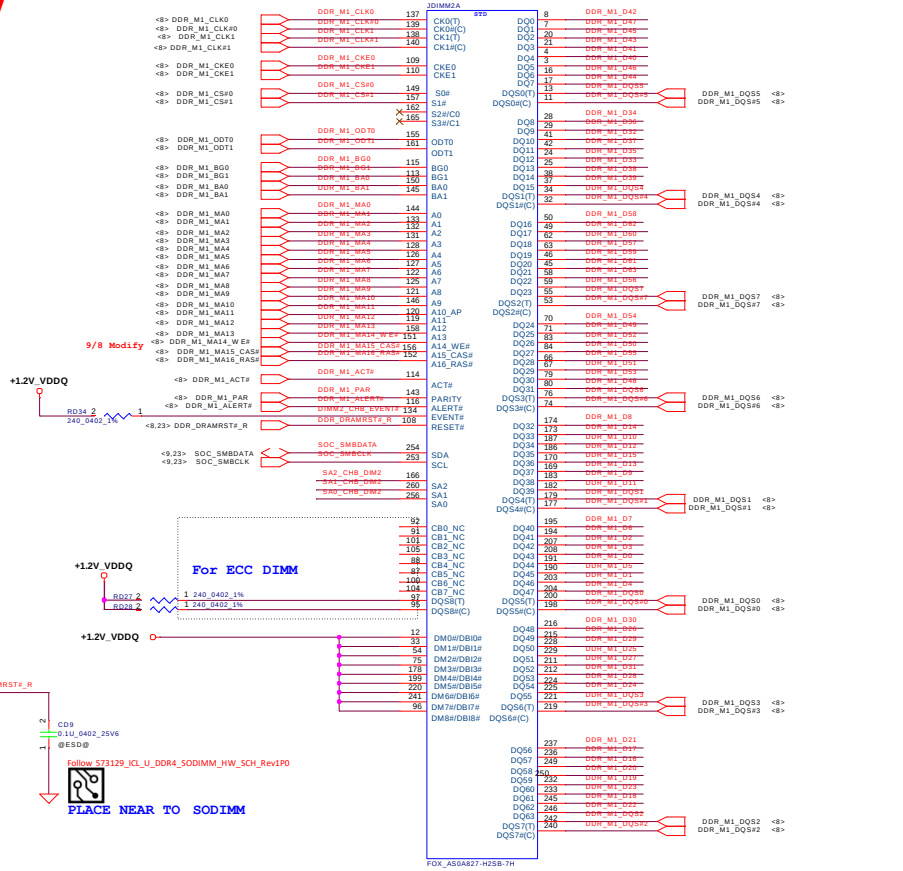


SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S



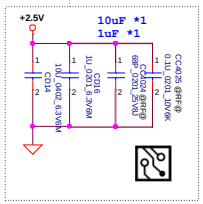


12/16 Remove RD36

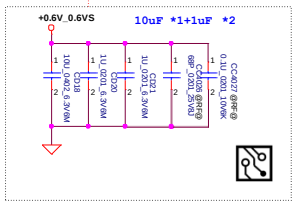


Decoupling Cap._Channel B

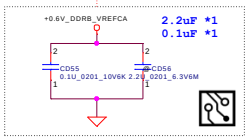
Layout Note:
Place near JDIMM1.257,259



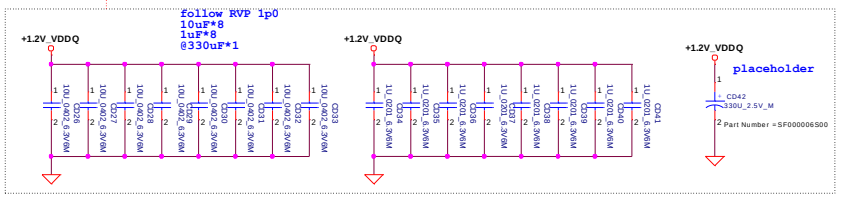
Layout Note:
Place near JDIMM1.258



Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM1



Layout Note:
Place near JDIMM1



Update Table 4-26 for DDR4 SO-DIMM Decoupling Caps
572907_ICL_U_Y_PDG_Rev0p7

Table 4-26. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 SODIMM 1DPC	VDDQ/ VDD	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)
		placeholder	1x 330µF (7343)
	VTT	Place on VTT plane close to DIMM 1 cap stuffed, 1 placeholder	2x 10µF (0603)
		Place on VTT plane close to DIMM	4x 1µF (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10µF (0603)
		DIMM pin side, 1 per DIMM	2x 1µF (0402)
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)
		Place close to DIMM	2x 2.2µF (0402)

Note:
1. Total quantity is referring to 2 channels.

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Title: DDR4 CHM1: DIMM1
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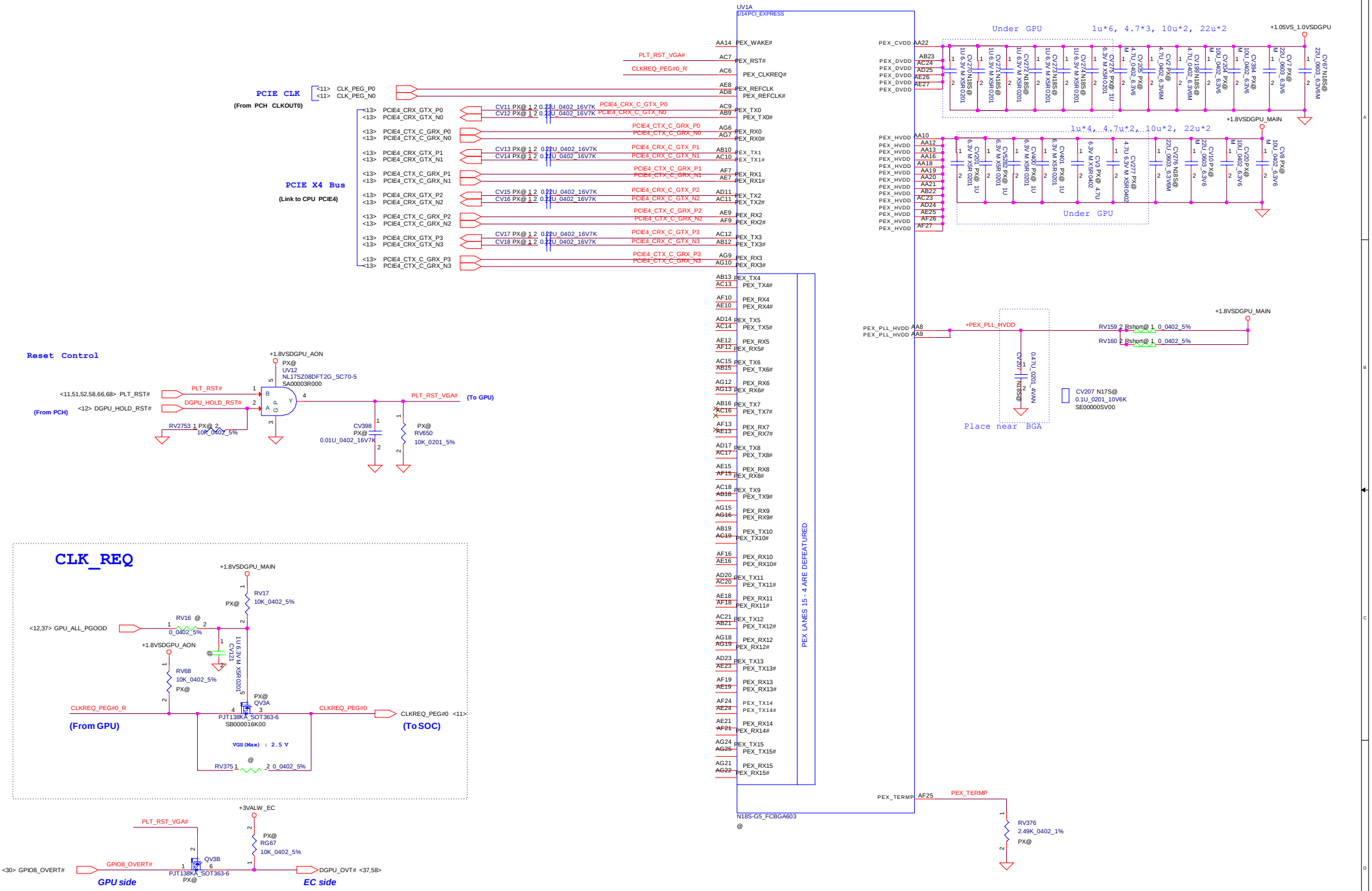

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Compal Electronics, Inc.

Title: NV(1/5)-PCIE

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Custom	LA-K201P	1.0
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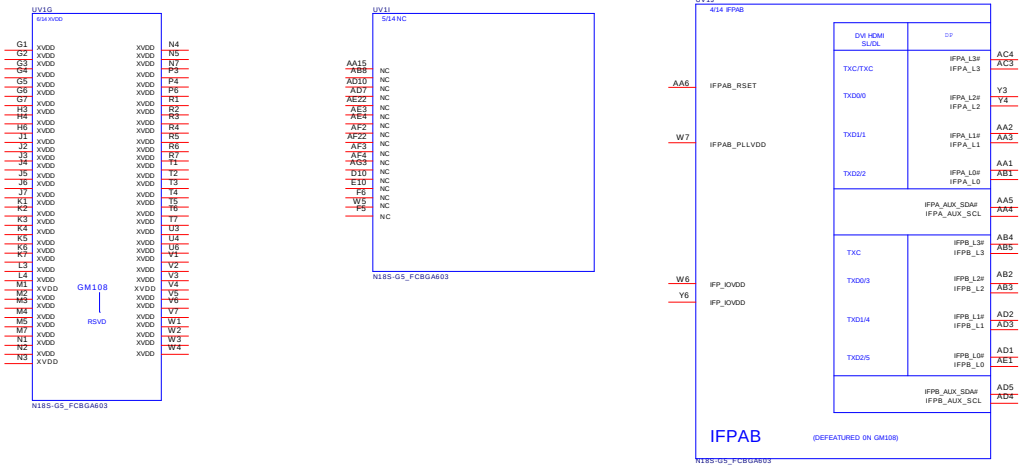

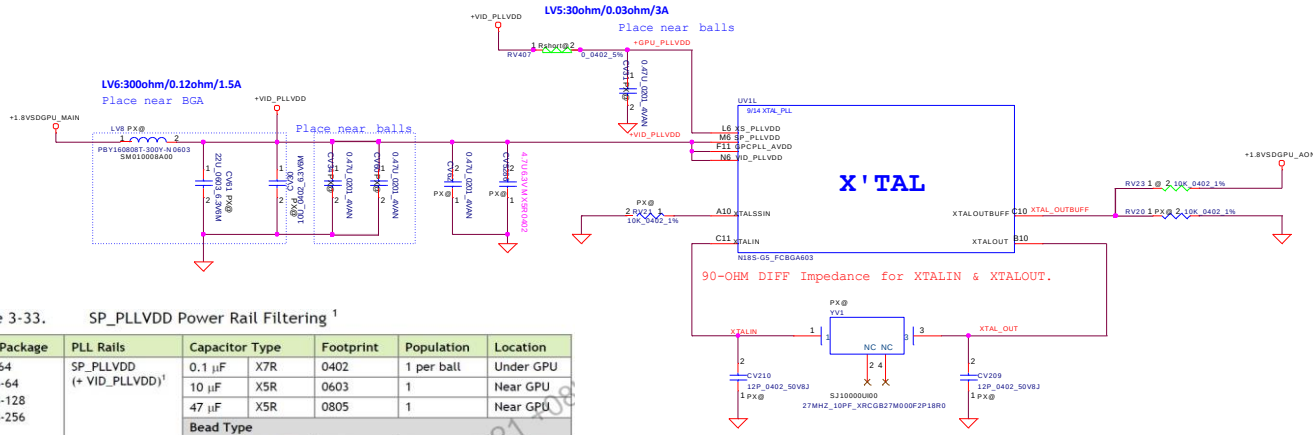

Table 3-33. SP_PLLVDD Power Rail Filtering [1]

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2-64 GB2B-64 GB4B-128 GB3B-256	SP_PLLVDD (+ VID_PLLVDD)[1]	0.1 µF	X7R	0402	1 per ball	Under GPU
		10 µF	X5R	0603	1	Near GPU
		47 µF	X5R	0805	1	Near GPU
		Bead Type				
		300 Ω (ESR=0.2 Ω)		0603	1	Near GPU

Note:
1. SP_PLLVDD and VID_PLLVDD power rails can be combined for customers who either do not use VGA display or uses VGA display with maximum resolution lower than 1024 x 768 with a 240 Hz refresh rate.

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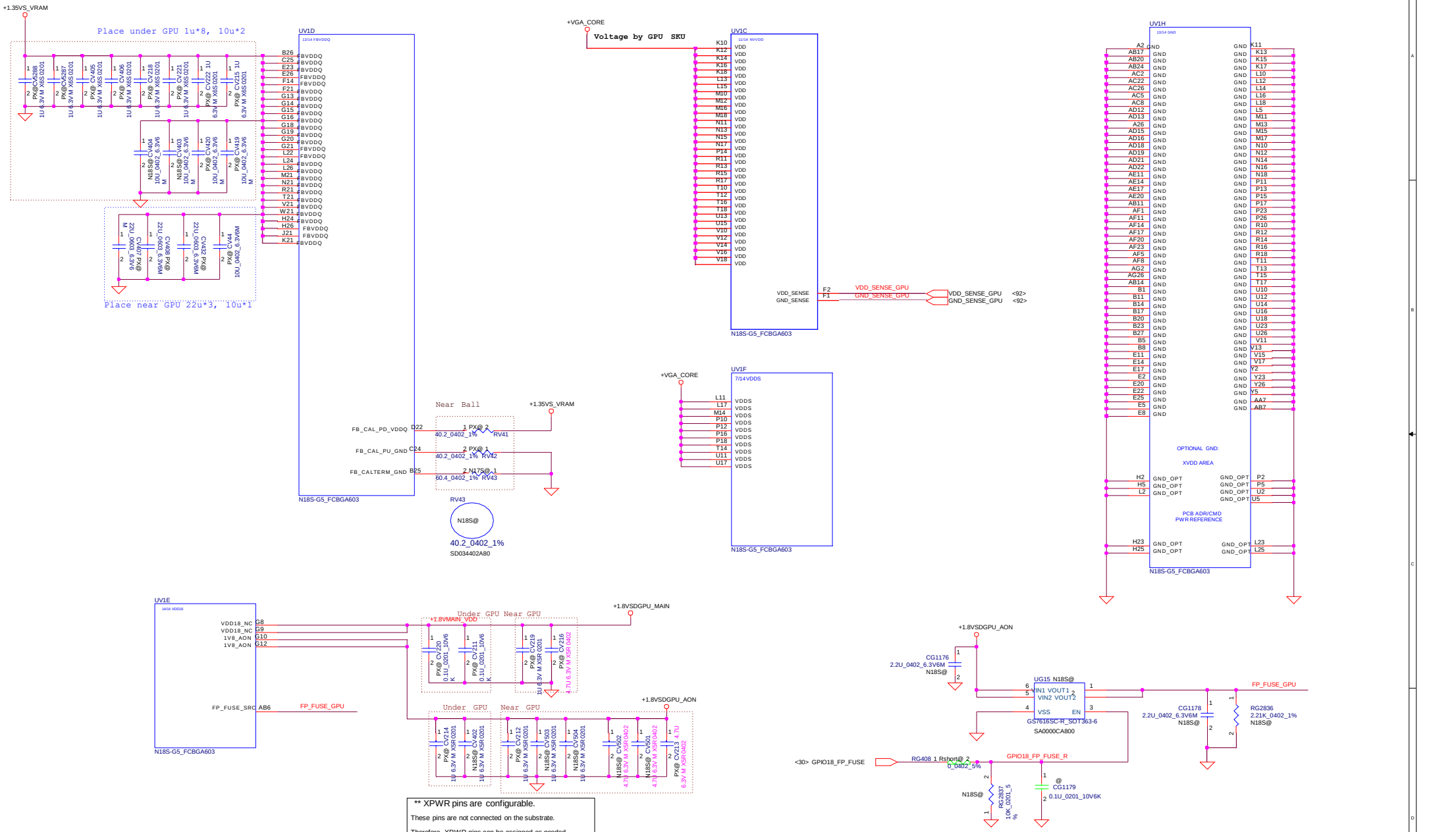

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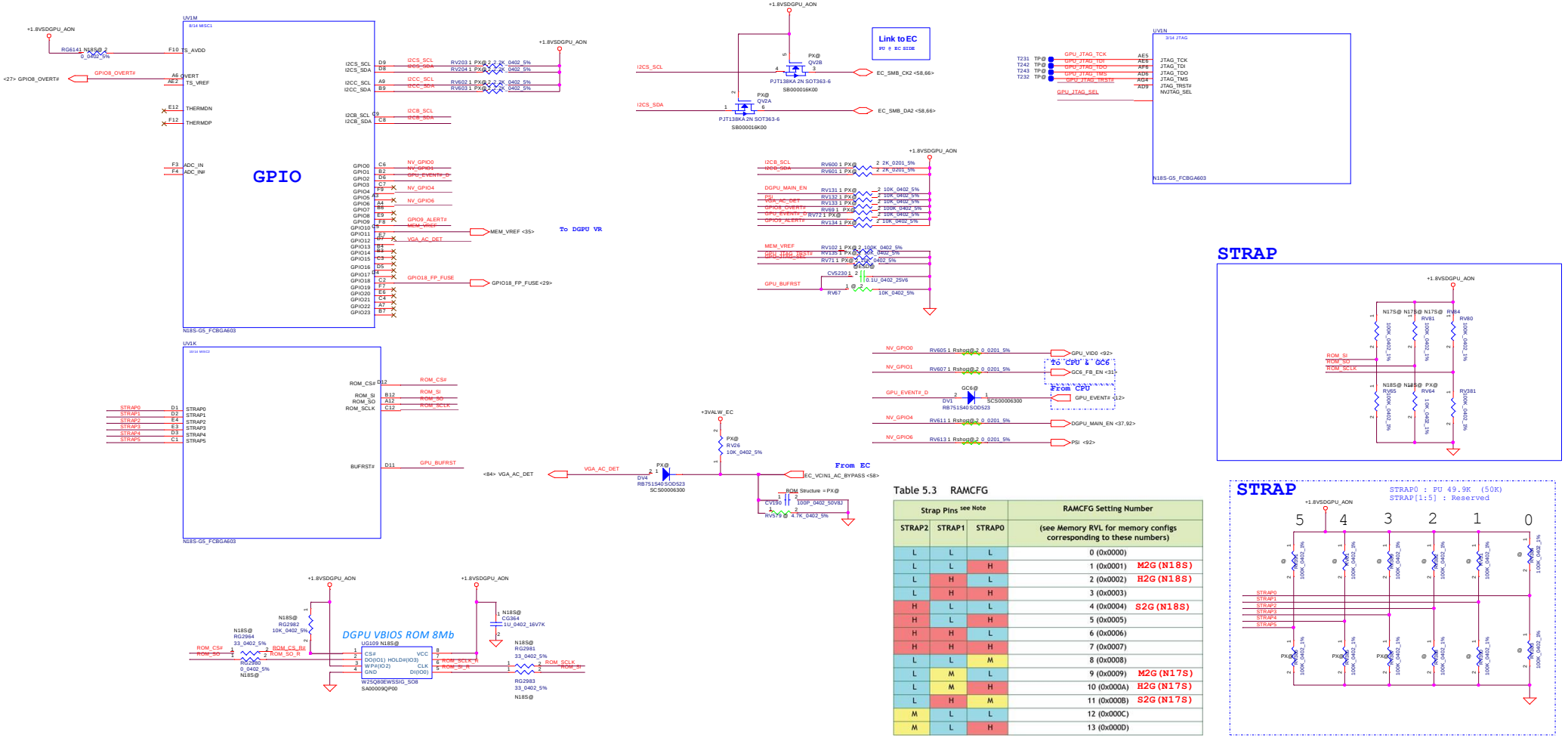

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001) M2G(N18S)
L	H	L	2 (0x0002) H2G(N18S)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004) S2G(N18S)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009) M2G(N17S)
L	M	H	10 (0x000A) H2G(N17S)
L	H	M	11 (0x000B) S2G(N17S)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 4. N17S-G5/LP GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production candidate
			Samsung	K4G80325FC-HC25	C-die	0xB	8 Gbps	N/A	Full	Production candidate

Table 13. N18S-G5 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0x2	8 Gbps	N/A	Full	Production candidate
			Samsung	K4G80325FC-HC25	C-die	0x4	8 Gbps	N/A	Full	Production candidate

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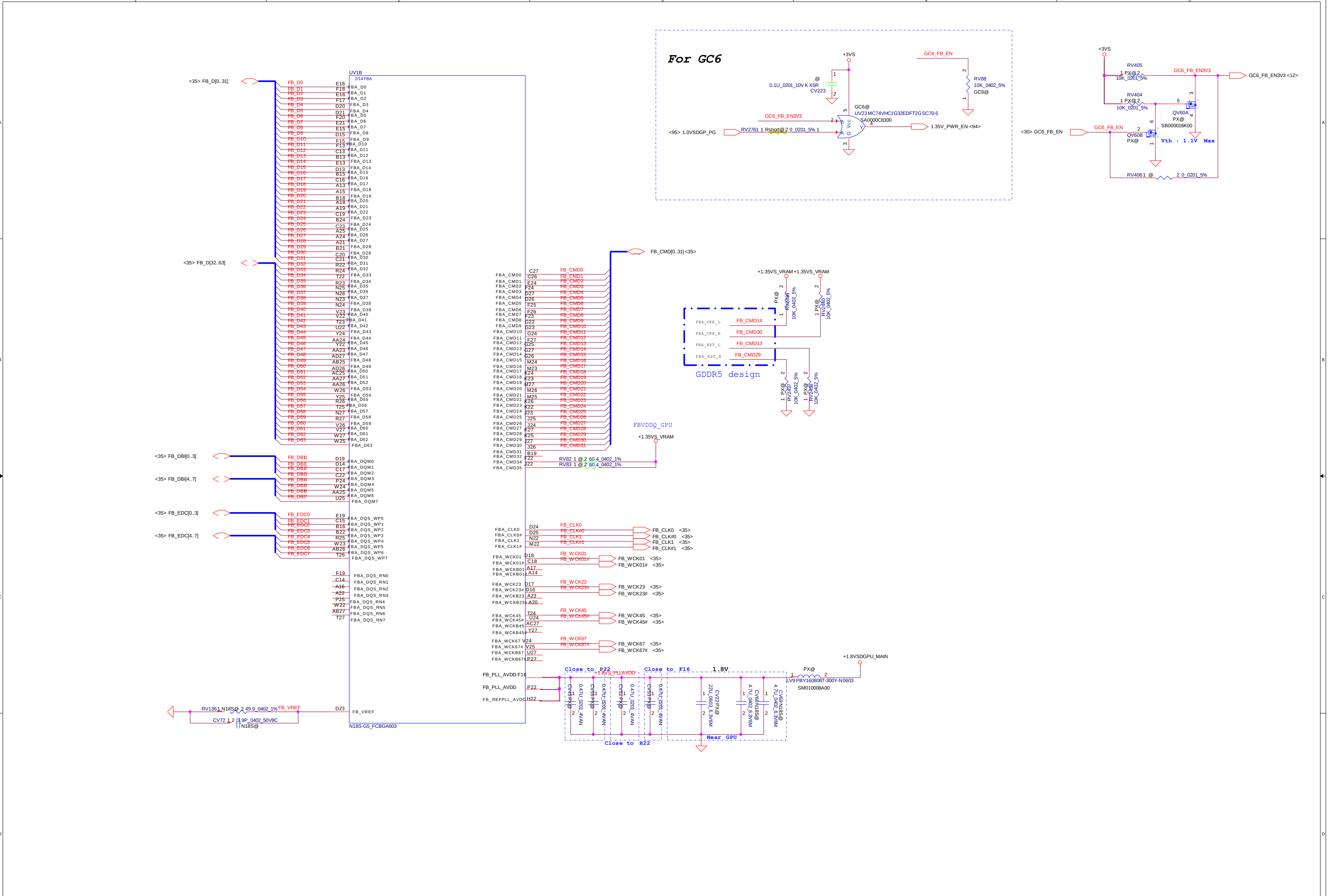

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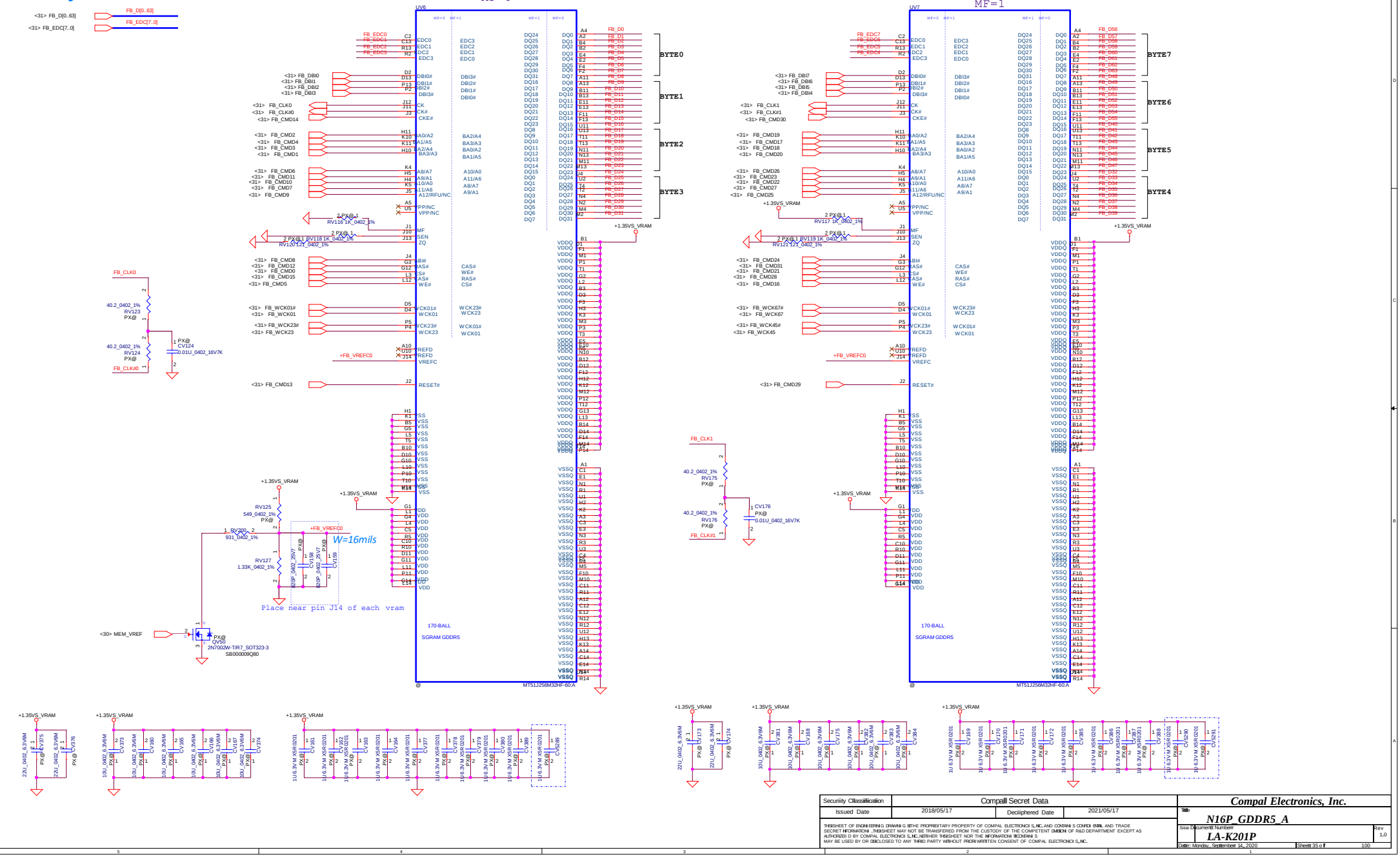
Memory Partition A



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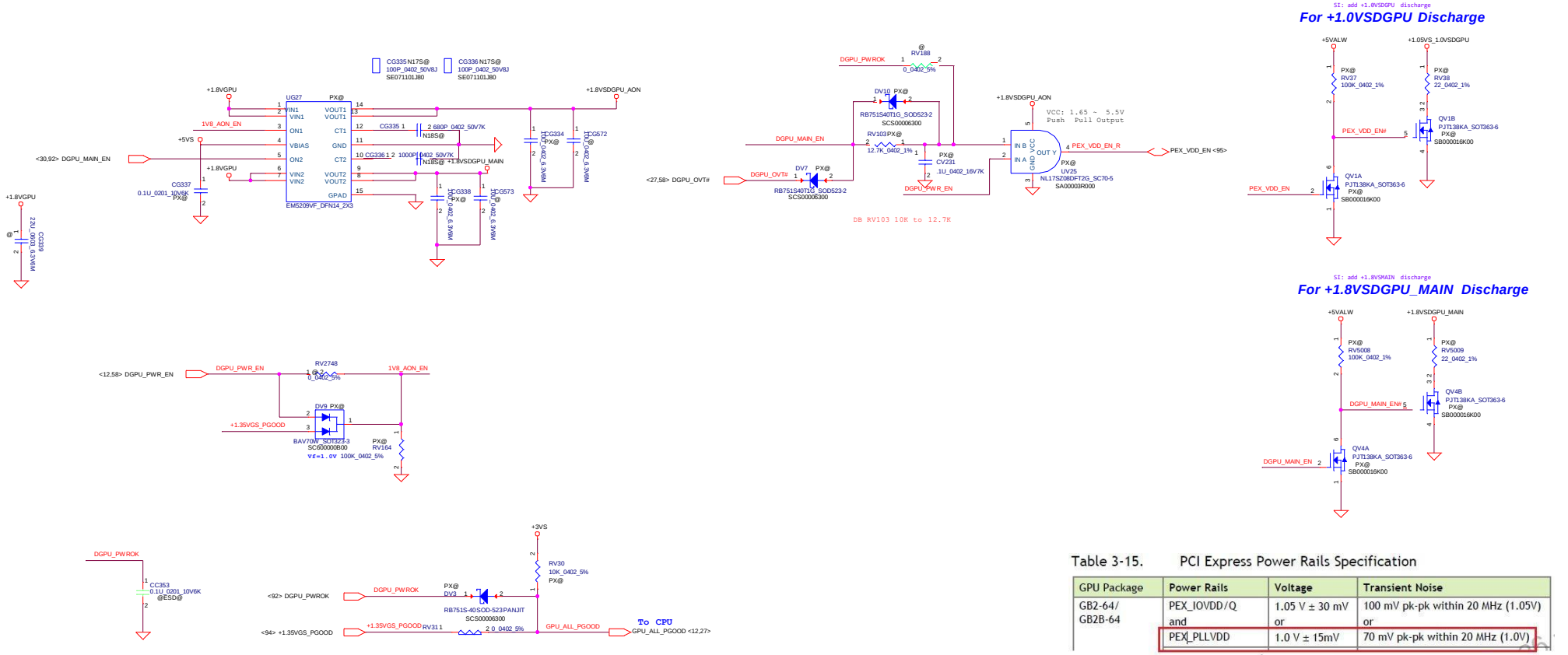


Table 3-7. Power Rail Specification for DDR3 Frame Buffer Interface

Constraint Parameter	Requirement
FBVDDQ/FBVDD	1.5 V (DDR3) or 1.35V (DDR3L)
DC tolerance	± 3%
AC tolerance	Transient noise tolerance: 80 mV pk-pk within 20 MHz BW
	High frequency noise tolerance: 200 mV pk-pk within 1 GHz BW

Table 5. EDP-Continuous [3]

Products	VRAM Type	GPU Core	GPU FBIO		FB Total [1,5]		1.05V Total [2]	3.3V Total
		–	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]	3.3V [4]
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	19.0	–	2.0	–	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5	26.5	–	2.0	–	4.2	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06

Table 3-15. PCI Express Power Rails Specification

GPU Package	Power Rails	Voltage	Transient Noise
GB2-64/ GB2B-64	PEX_IOVDD/Q	1.05 V ± 30 mV	100 mV pk-pk within 20 MHz (1.05V)
	and	or	or
	PEX_PLLVDD	1.0 V ± 15mV	70 mV pk-pk within 20 MHz (1.0V)

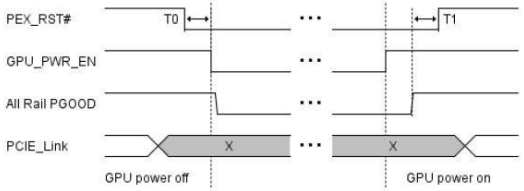
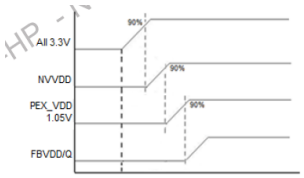


Figure 18-7. Optimus Entry/Exit Timing Diagram

Note:
- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-7. Example of Power-Up Sequencing Order

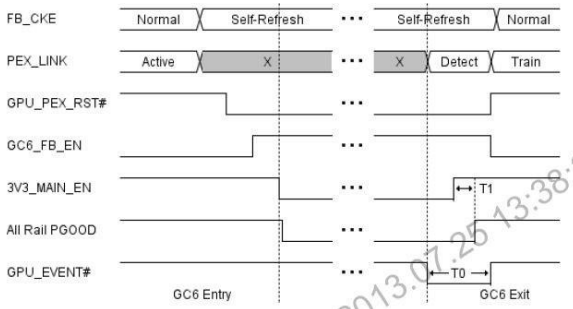


Figure 18-15. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

Table 18-3. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

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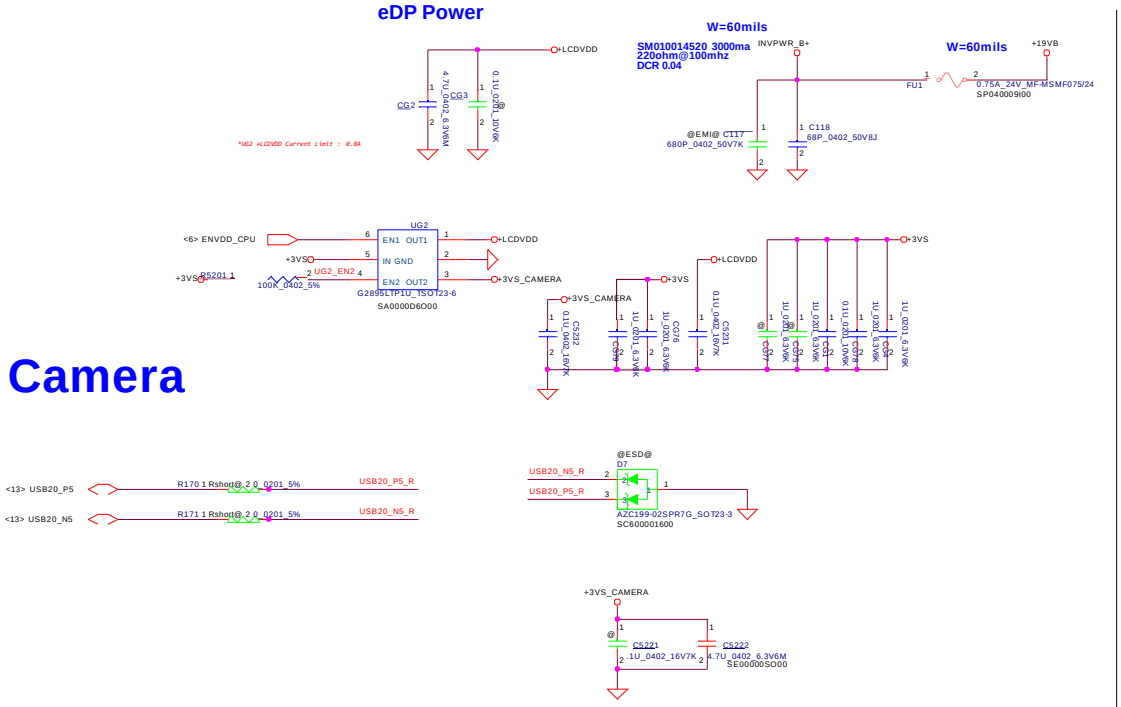

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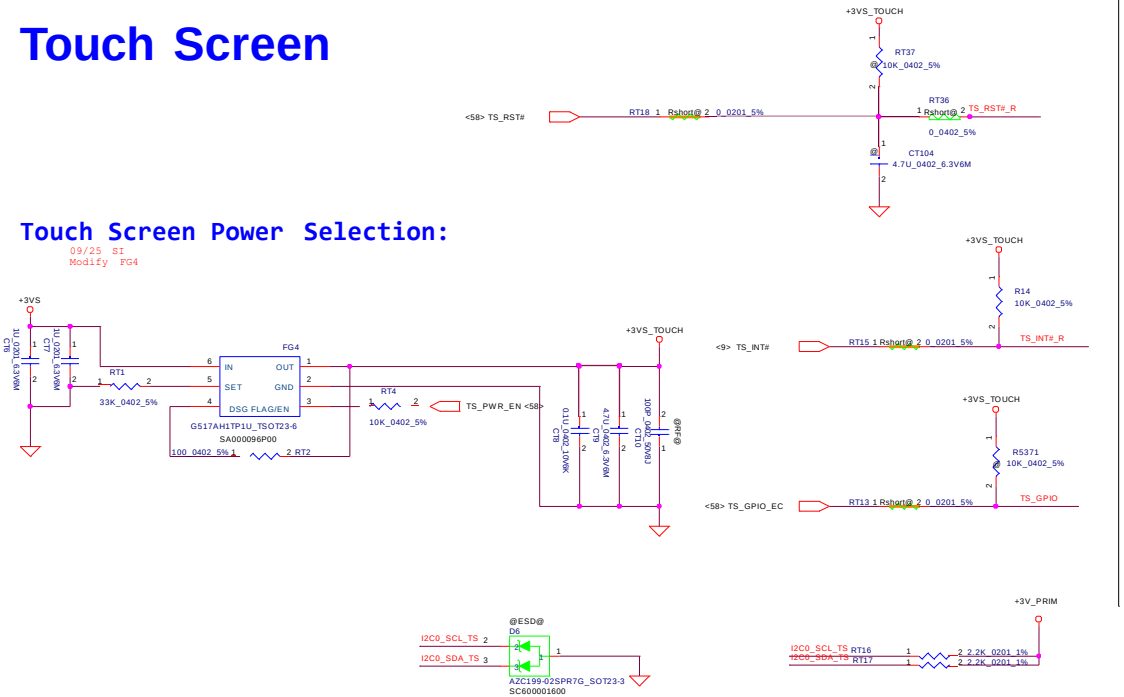

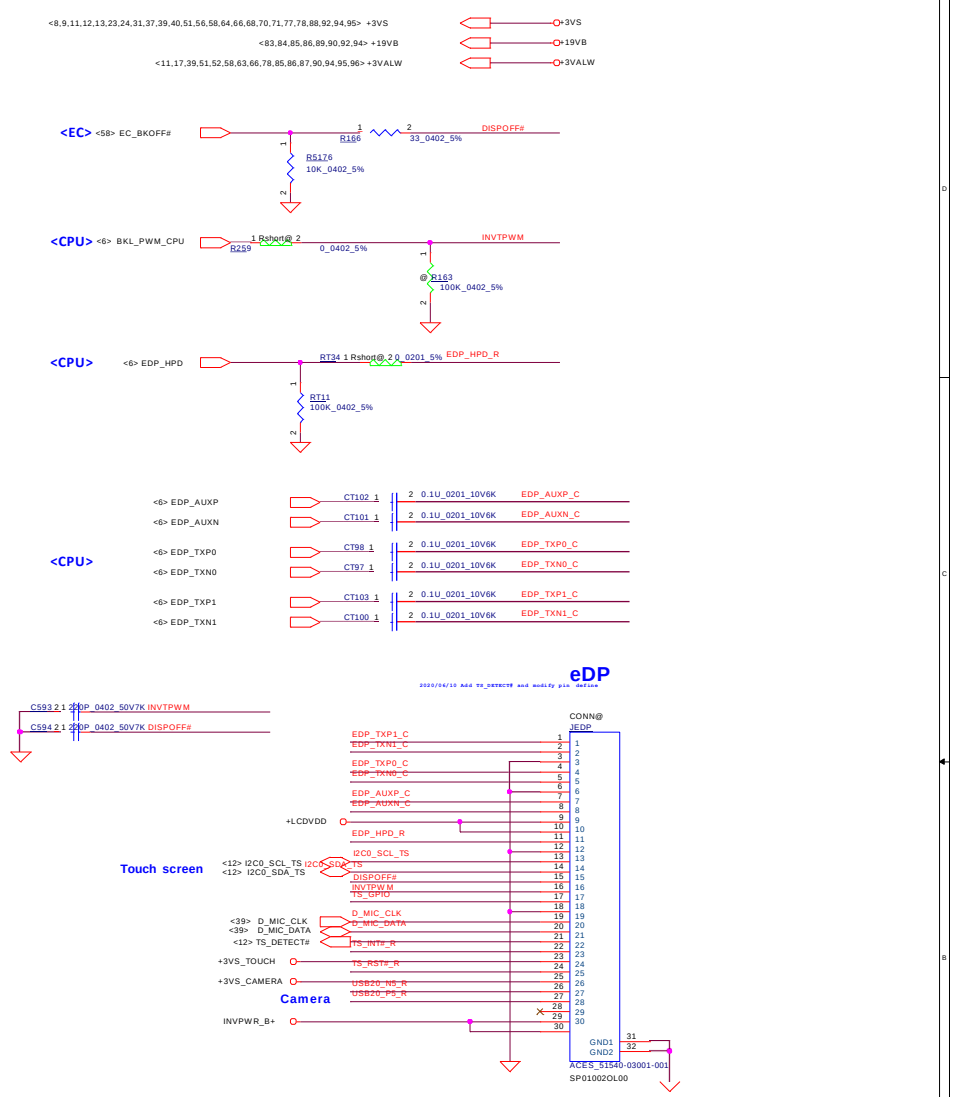

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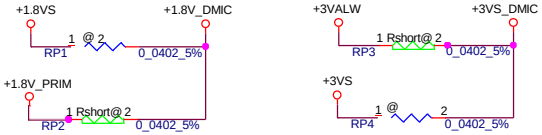

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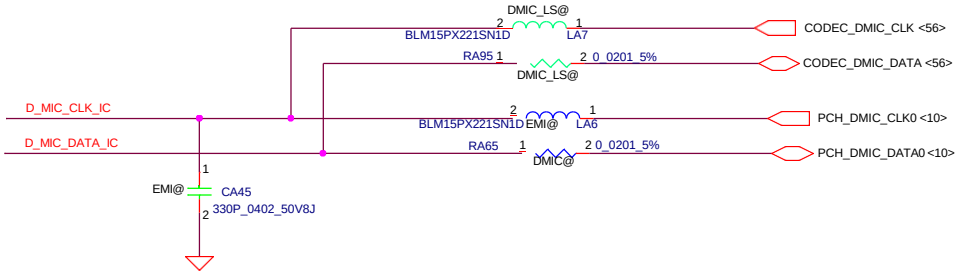
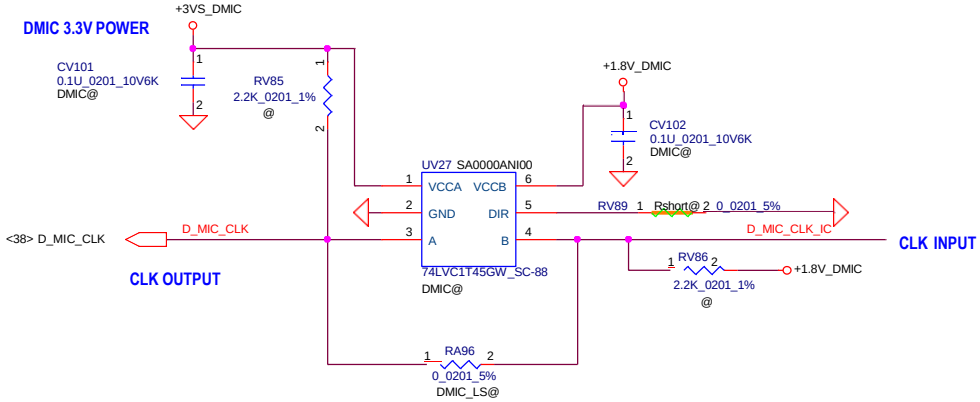
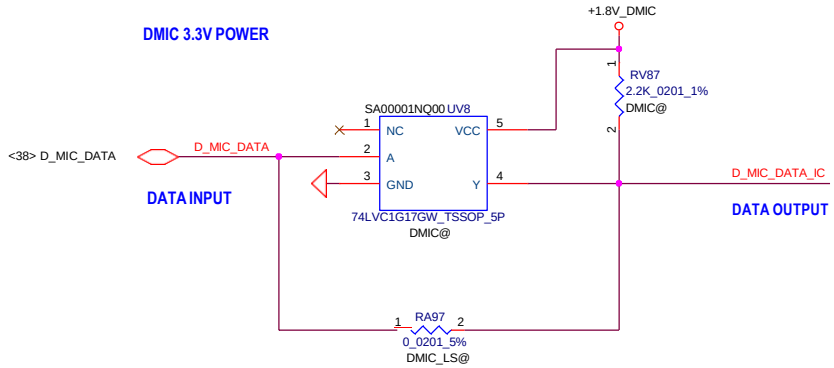
DMIC_LS@=Normal







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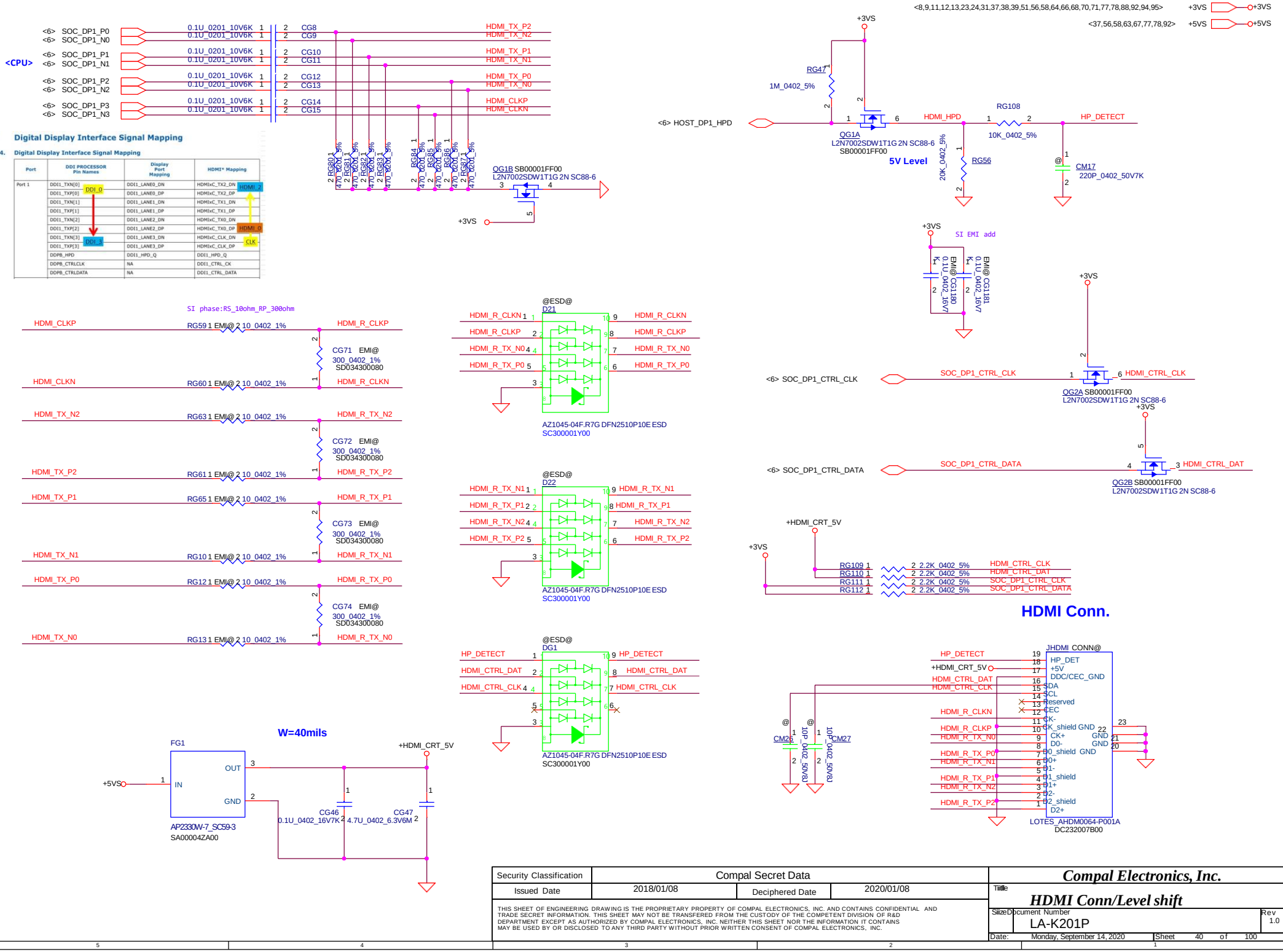

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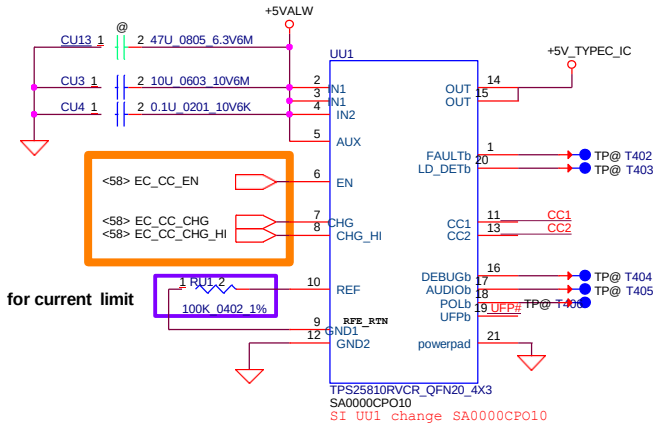

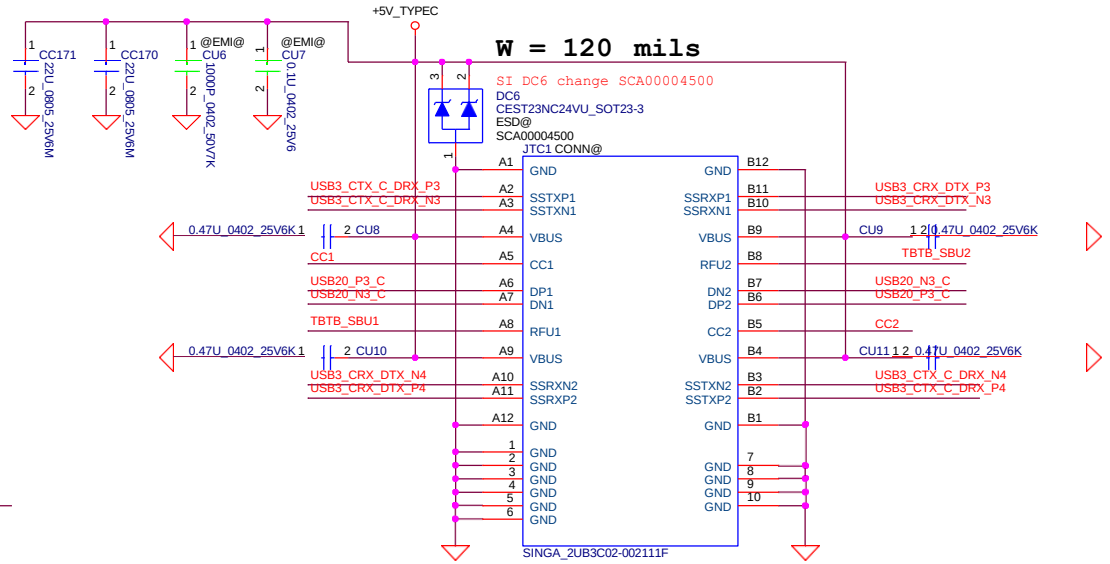

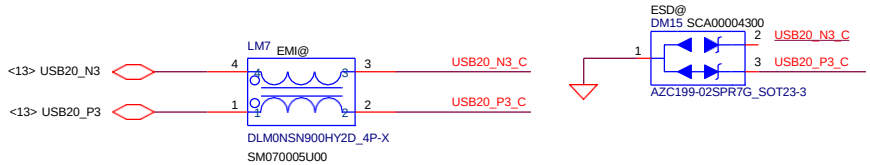

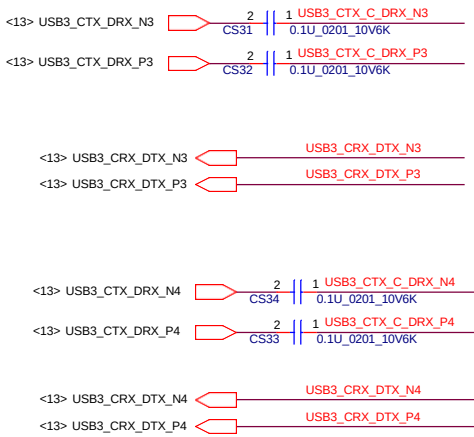

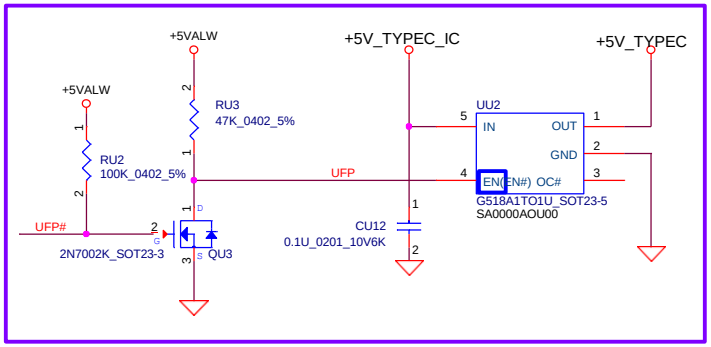

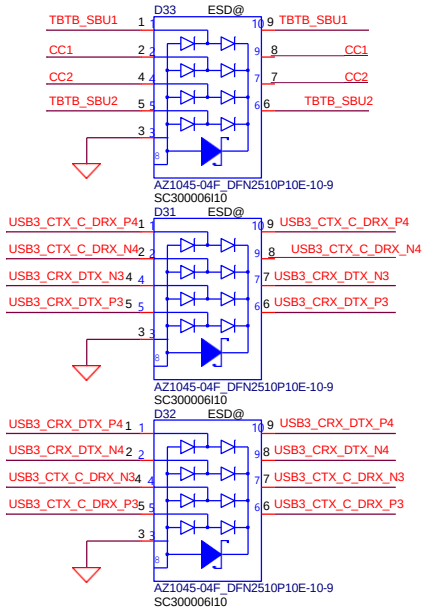

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+LAN_VDD_3V3 Rising time
need>0.5mS and <100mS

CL8, CL23 close LL2.
CL26 close UL1 Pin 3.
CL12 close UL1 Pin 8.
CL13 ~ CL15 close UL1 Pin 22.
CL11, CL27 close UL1 Pin 30.

RTL8107ESH-CG/RTL8111HSH-CG Co-Lay

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

CL9, CL20 close to UL1 Pin 11
CL5 & CL19 close to UL1: Pin 32

CL10& CL16 close to UL1: Pin 23

(SA000084T00) RTL8111HSH-CG Giga

LAN_ACT# Amber
LAN_LINK# White

B (back) : LAN_LINK_White

power rail need to check

power rail need to check

Singatron En 信音企業
LOTES

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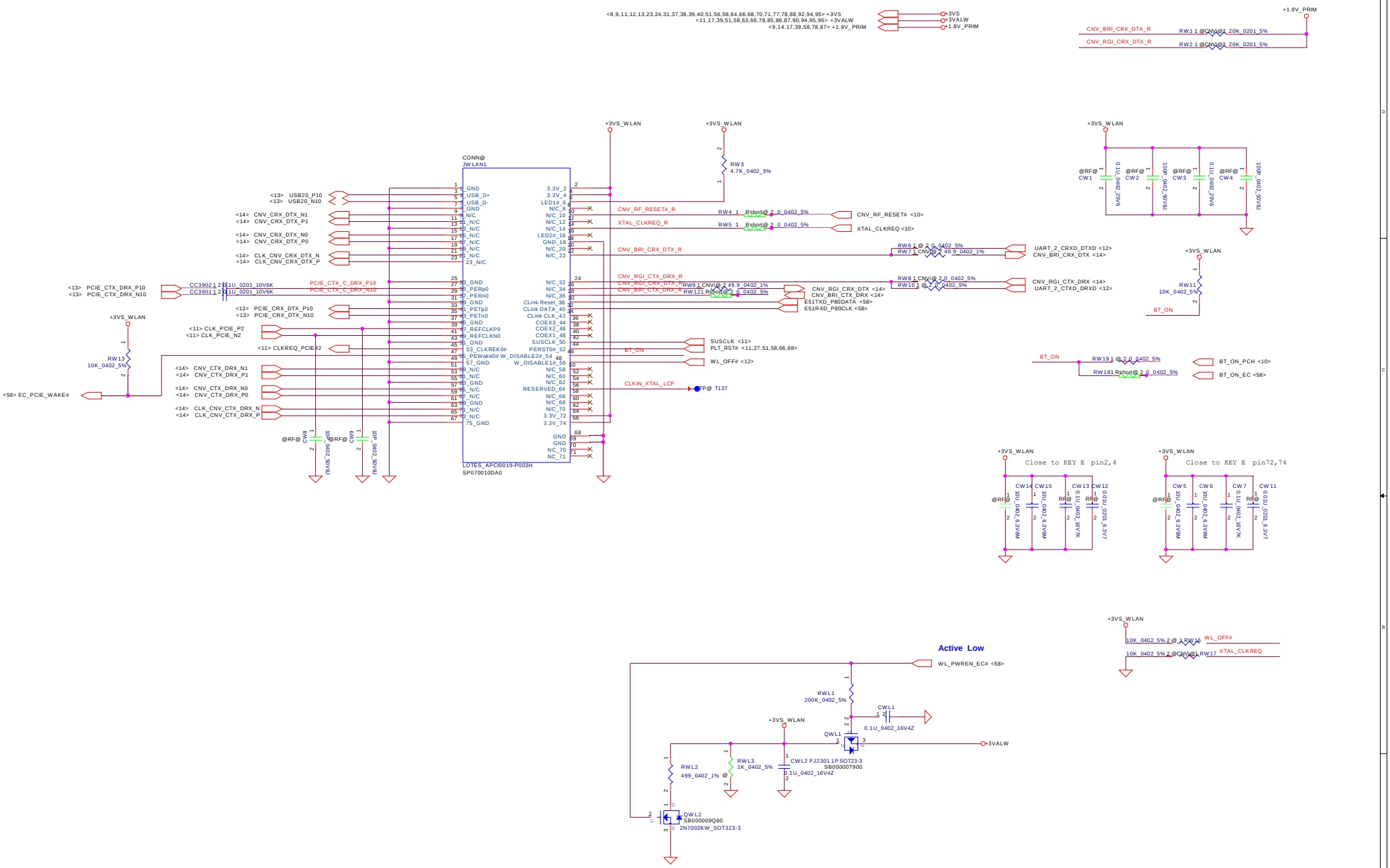

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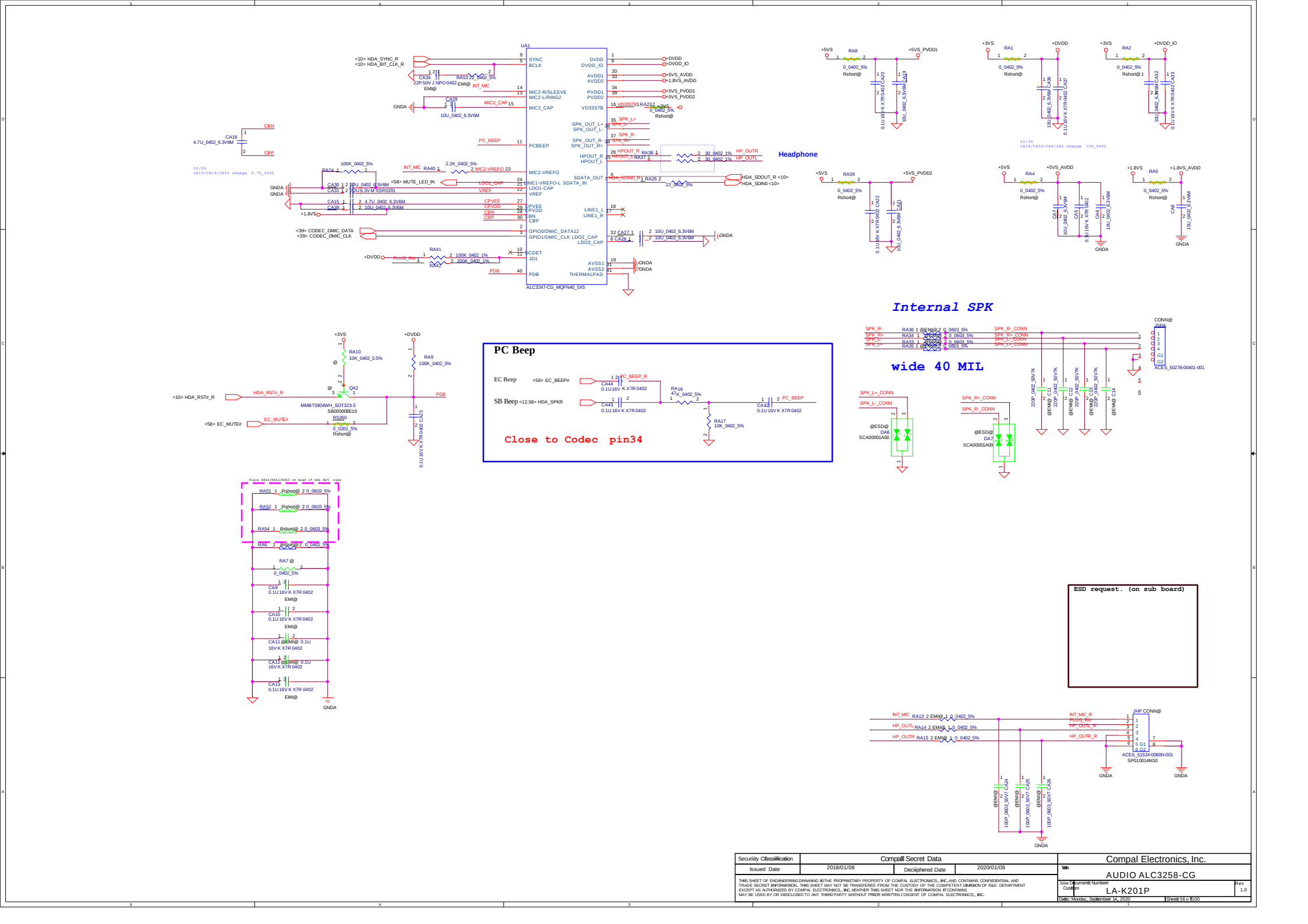
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wide 40 MIL
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EC Beep
SB Beep
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ESD request. (on sub board)
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2020/01/08
Monday, September 14, 2020

08/22
Need to find power source

For Power consumption Measurement

pin 1-14 power domain follow VCC_LPC(1.8V)

UK1 eSPI & MISC

PWM Output
AD Input
DA Output
PS2 Interface
GPIO
SPI ROM
Int. K/B Matrix
SMBUS

KB9052Q-D_LQFP128_14X14
20mil

Board ID

	DB	SI	PV	MV
UMA	0 ohm	15k ohm	27K ohm	43K ohm
DIS	12k ohm	20k ohm	33k ohm	56k ohm

OPMODE (Internal Pull High) :

Pull Up : Intel eSPI Master Attached Flash Sharing Topology
--> For KB9042 / KB9052

Pull Down : Intel Legacy Wire-OR share ROM.
--> For KB9022/9042 Use

For Solve tPCH04(Min 9ms) Sequence Timing

(Link to dGPU/Thermal sensor)

09/25
Add CMOS

need to check RTCRST connection

Security Classification	Compal Secret Data		
Issued Date	2018/9/25	Deciphered Date	2018/12/31

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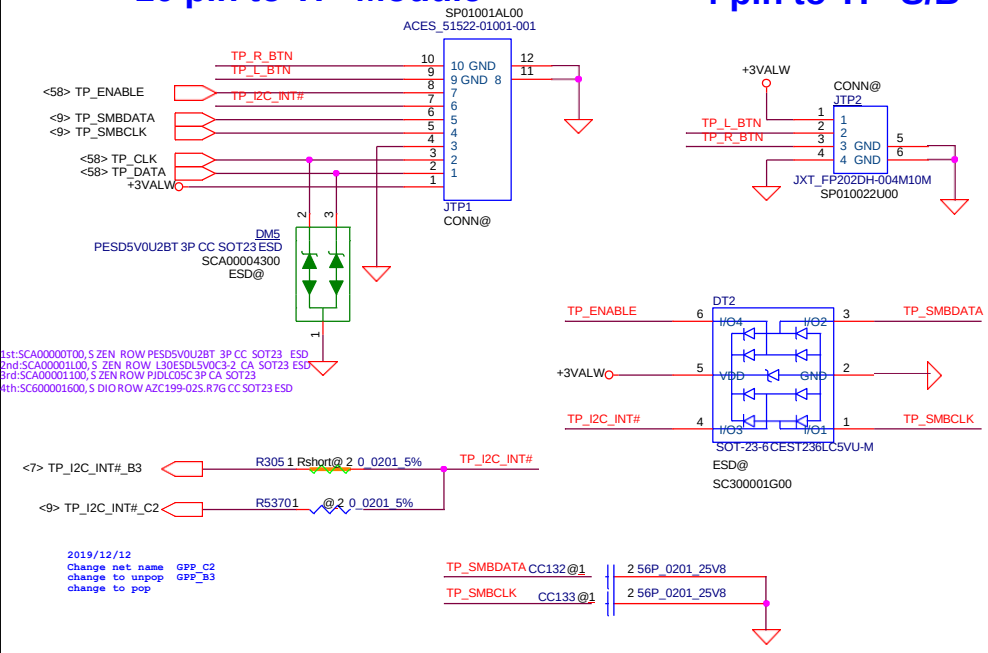
Title: EC ENE-KB9052QA Only

Size: A3 | Document Number: LA-K201P | R ev: 1.0

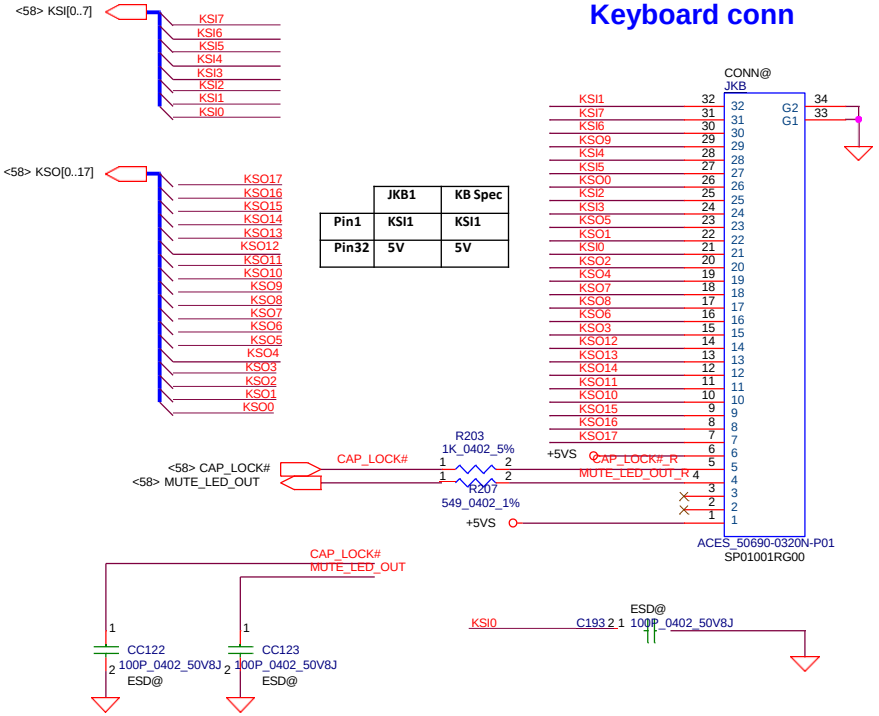
Date: Monday, September 14, 2020 | Sheet 58 of 100

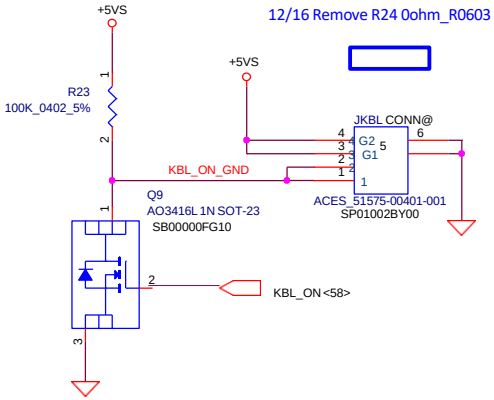
10 pin to TP Module



4 pin to TP S/B

Keyboard conn





Security Classification	Compal Secret Data		
Issued Date	2018/01/08	Deciphered Date	2020/01/08

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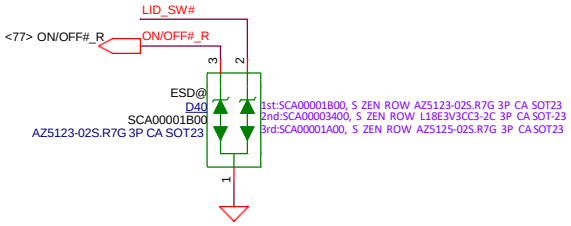
Compal Electronics, Inc.

Title: KB/TP

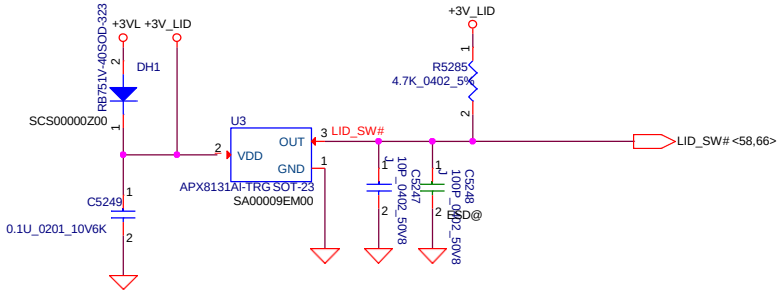
Size: Custom | Document Number: LA-K201P | Rev: 1.0

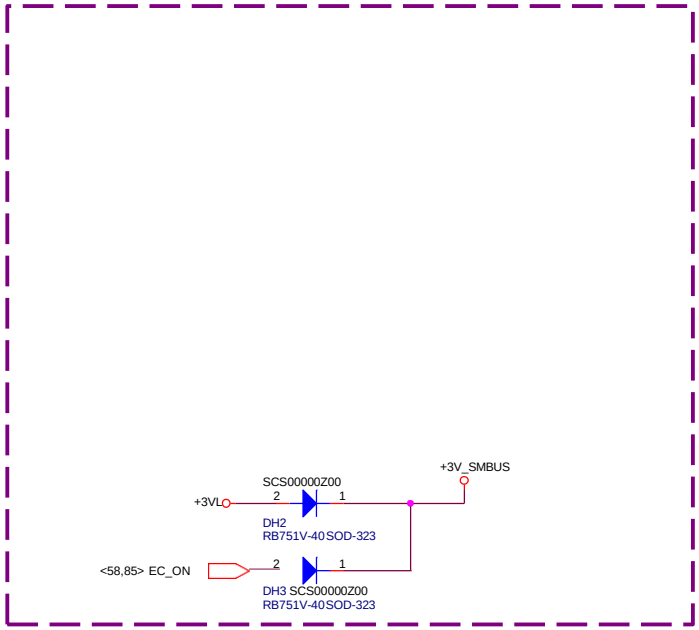
Date: Monday, September 14, 2020 | Sheet 63 of 100

ESD Diode

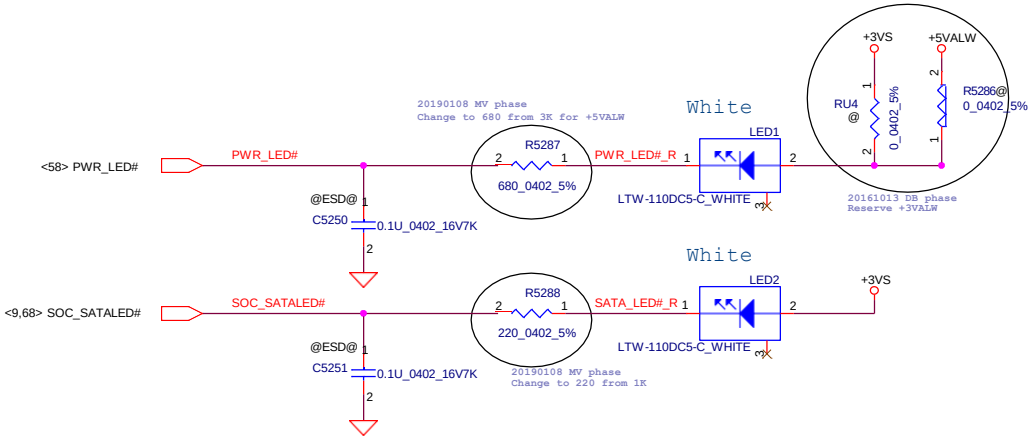


Lid Switch (Hall Effect Sensor)





HDD LED/ POWER LED



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Compal Electronics, Inc.

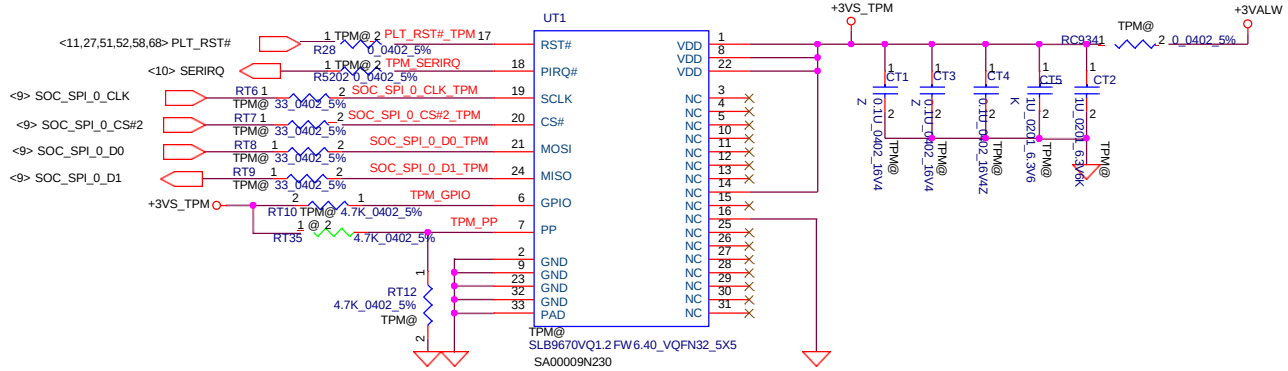
Title: HW Reserve

Size: Custom | Document Number: LA-K201P | Rev: 1.0

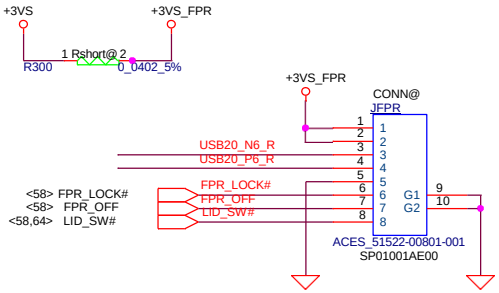
Date: Monday, September 14, 2020 | Sheet 64 of 100

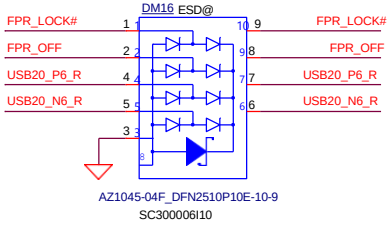
+3VALW +3VALW <11,17,39,51,52,58,63,78,85,86,87,90,94,95,96>

TPM2.0

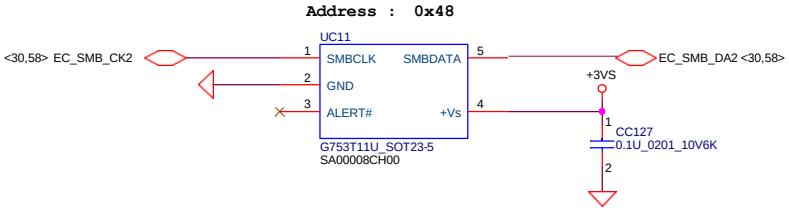


Finger printer





CPU THERMAL SENSOR



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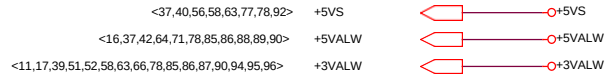
Compal Electronics, Inc.

Title: **TPM/Screw**

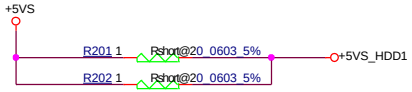
Size: Document Number: LA-K201P Rev: 1.0

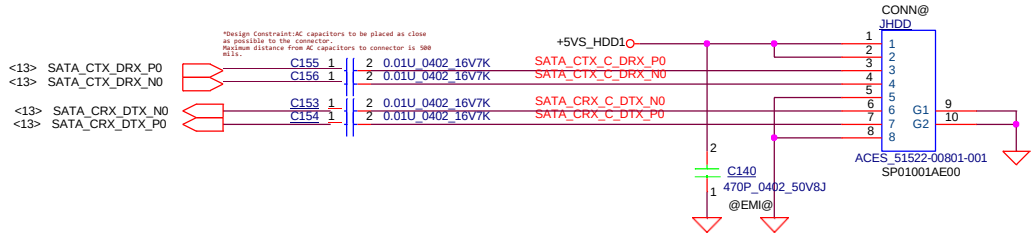
Date: Monday, September 14, 2020 Sheet 66 of 100

2.5" SATA HDD



<PV> change short pad





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Title: HDD/ODD Conn

Size	Document Number	Rev
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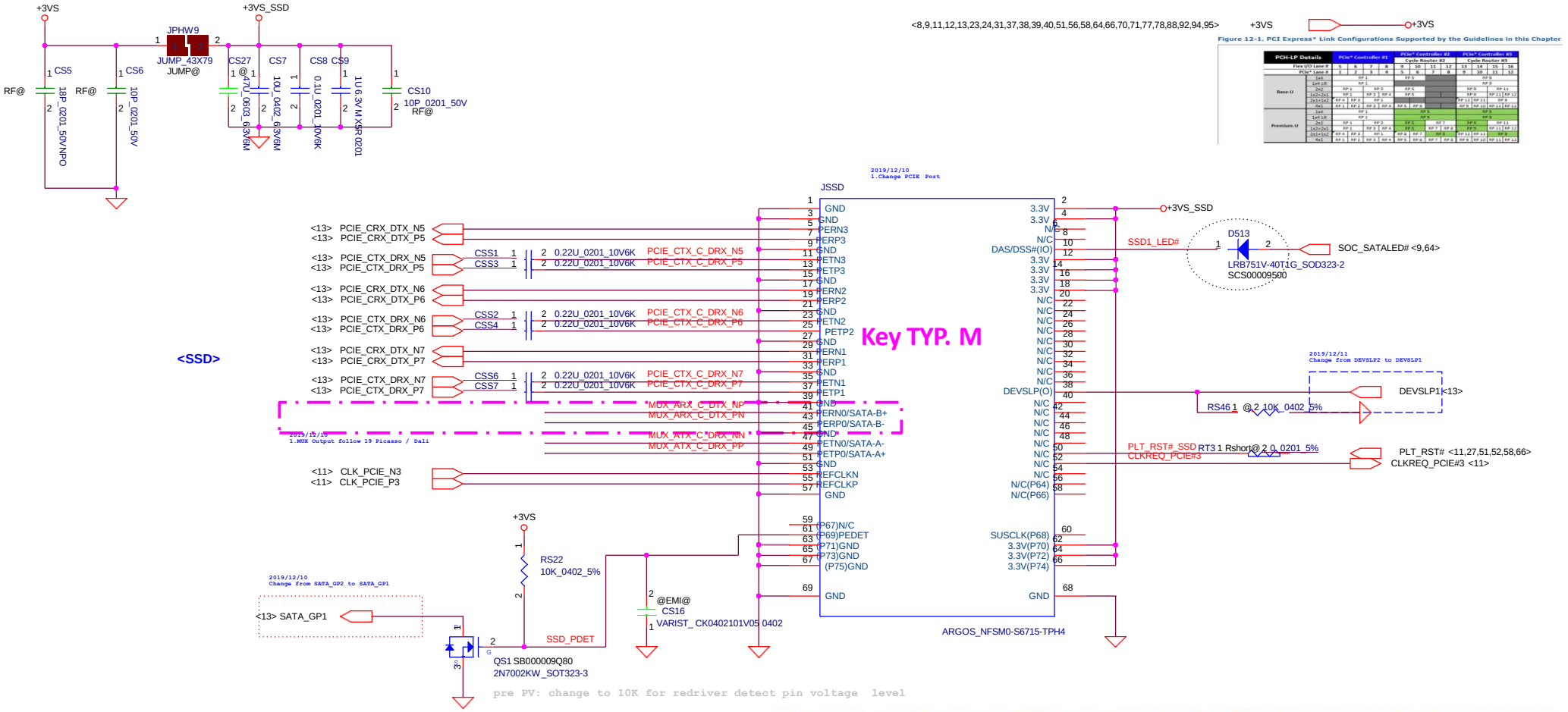

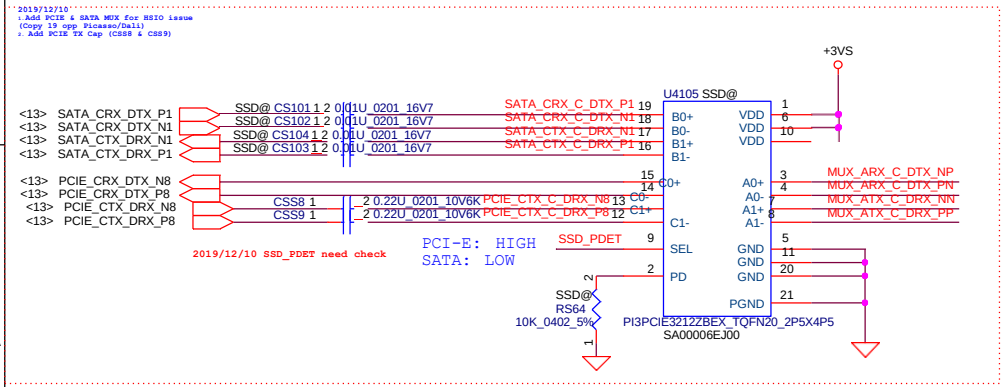

36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

39	GND	PCIeMVMe_DD90000NU90_MZVLW1T0HMLH-000H1 F73H1Q 0FH		
41	PETn0	PCIe TX	42	N/C
43	PETp0	PCIe TX	44	N/C
45	GND	Return current path	46	N/C
47	PERn0	PCIe Rx	48	N/C
49	PERp0	PCIe Rx	50	PERST#
51	GND	Return current path	52	CLKREQ#

Security Classification	Compal Secret Data		
Issued Date	2018/01/08	Deciphered Date	2020/01/08

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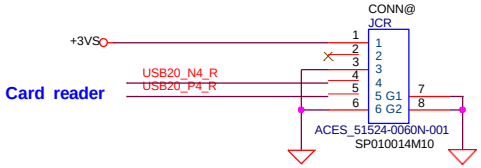
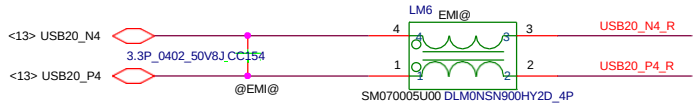
Compal Electronics, Inc.

Title	*M.2 SSD*
Size	Document Number: **LA-K201P**
Rev	1.0
Date:	Monday, September 14, 2020
Sheet	68 of 100

<8,9,11,12,13,23,24,31,37,38,39,40,51,56,58,64,66,68,71,77,78,88,92,94,95> +3VS





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Title: HW Reserve

Size	Document Number	Rev
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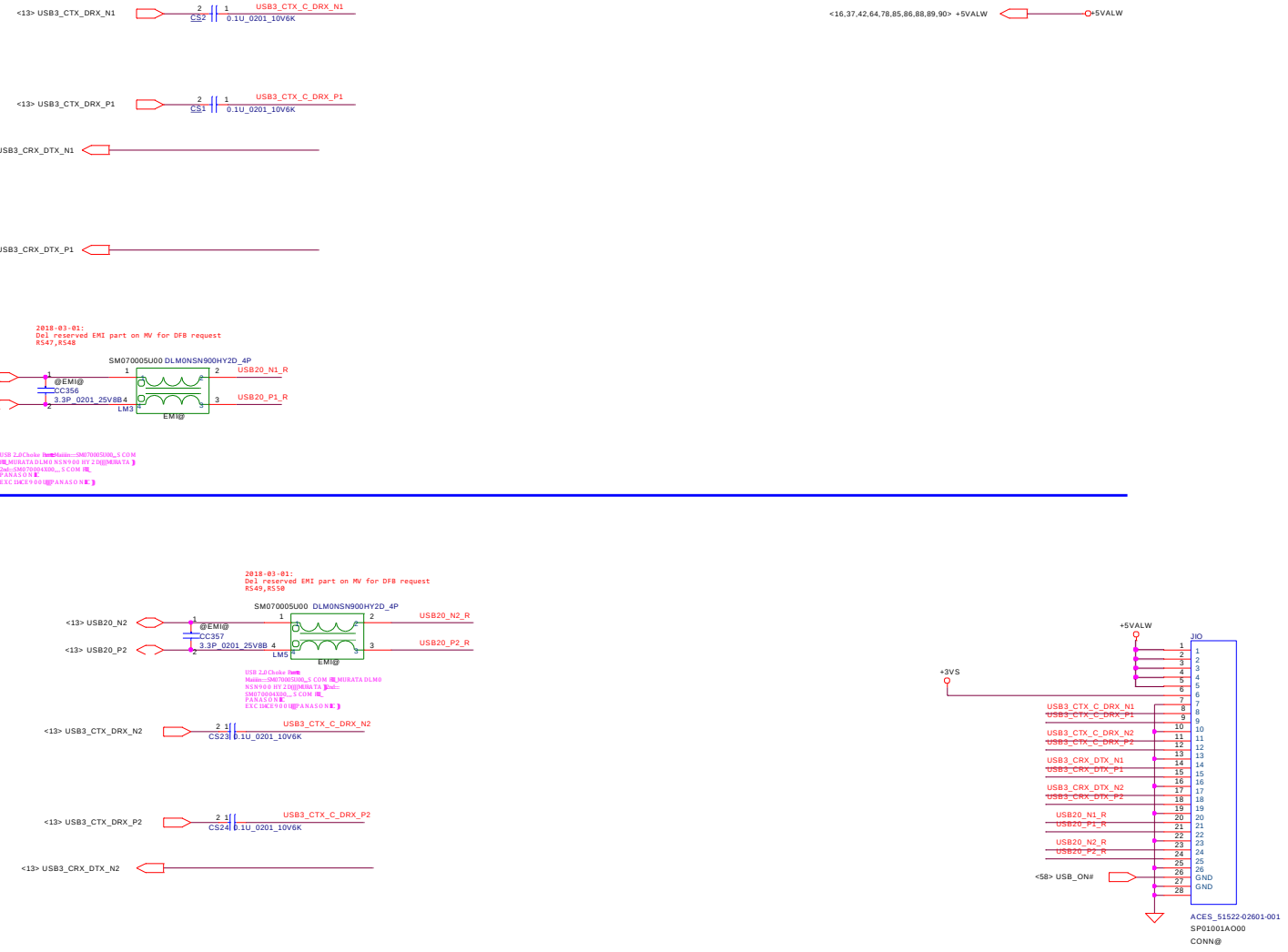

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Compal Electronics, Inc.

Title: USB 3.0/2.0 conn

Size	Document Number	Rev
Custom	LA-K201P	1.0

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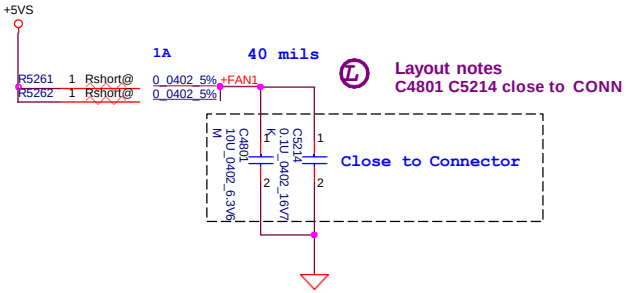
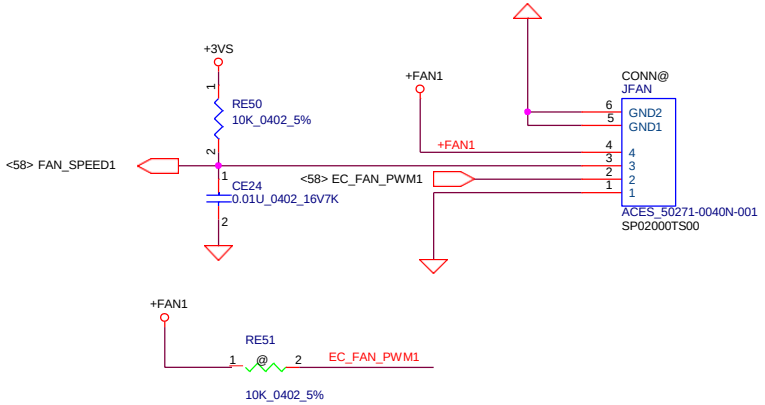
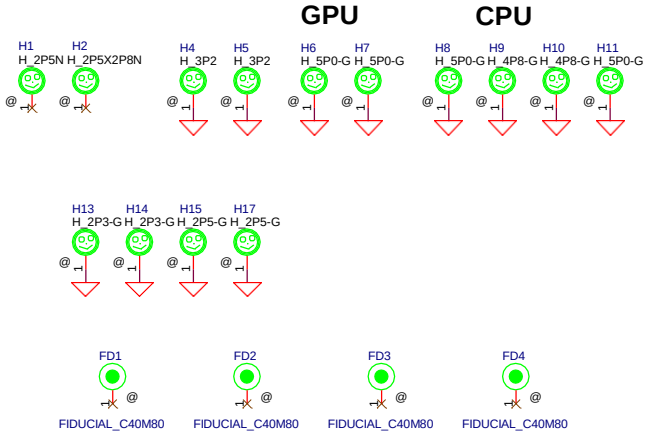
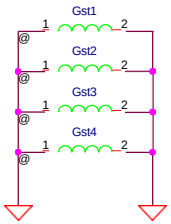


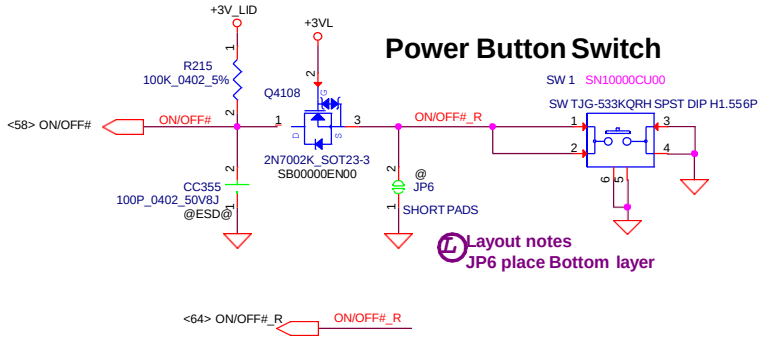


Screw Hole



EMI Gasket





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Size Custom	Document Number LA-K201P		Rev 1.0
Date: Monday, September 14, 2020	Sheet 77 of 100		

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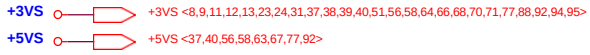
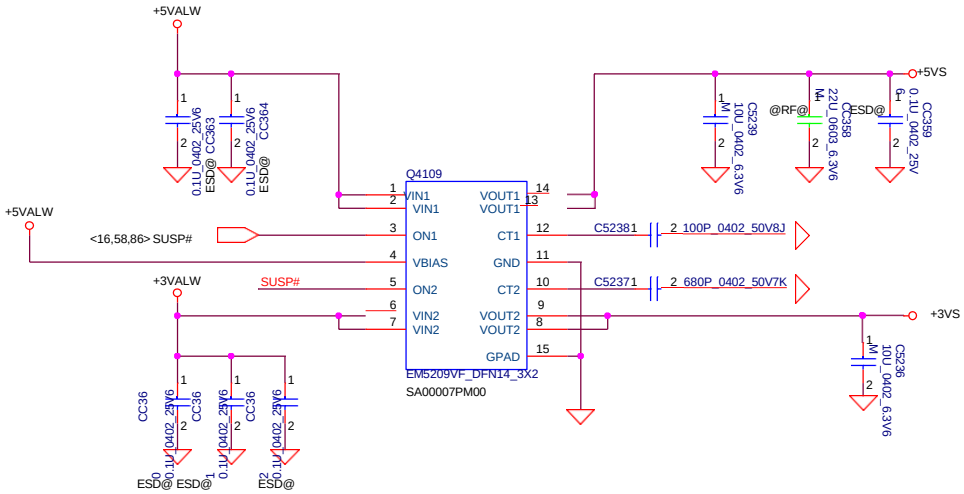
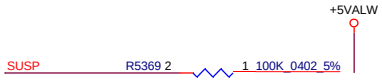
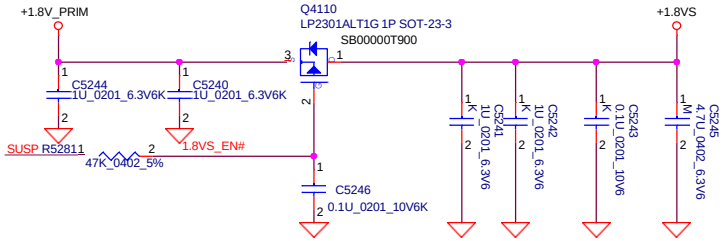




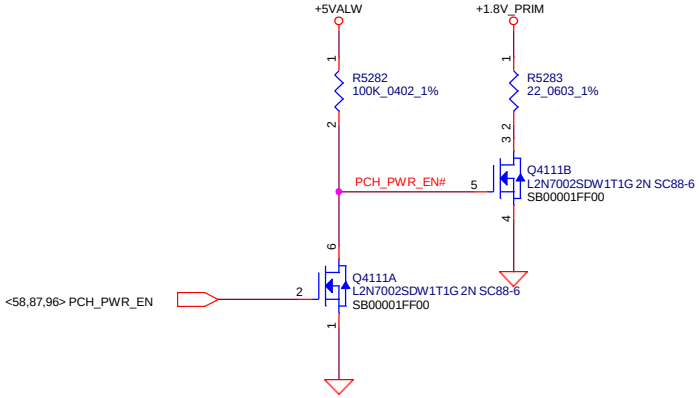


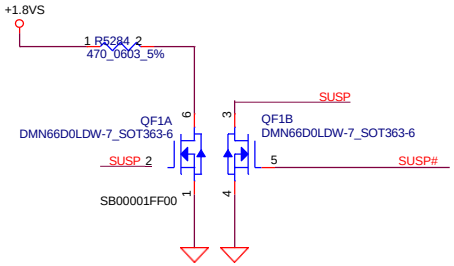
+1.8V_PRIM TO +1.8VS

I (Max) : 0.2 A(Codec)
RDS(max) : 150 mohm
V drop : 0.03V



For +1.8V_PRIM Discharge





Add +1.8VS power down

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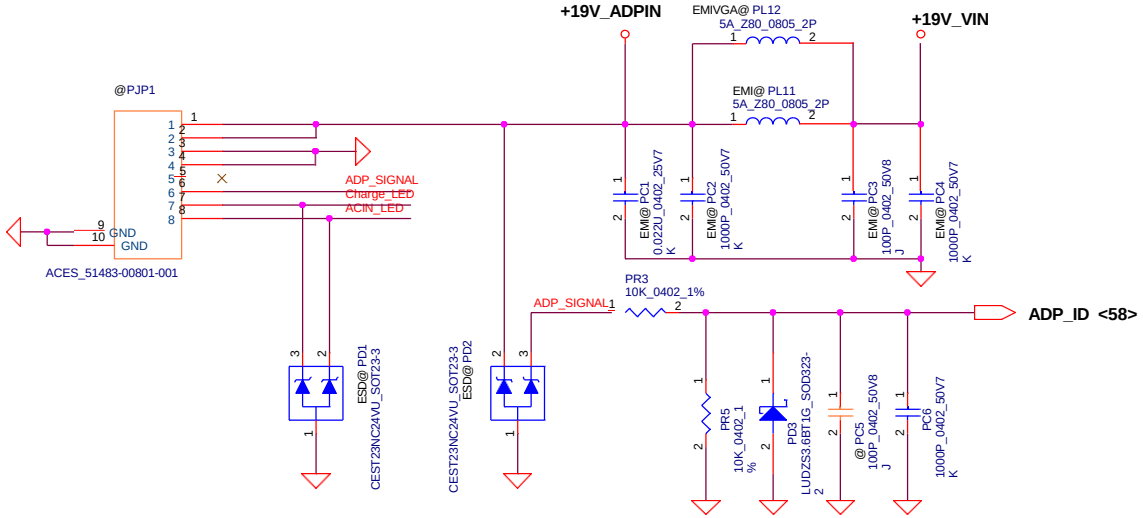
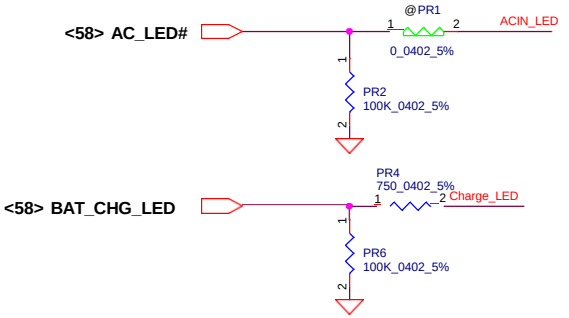
Compal Electronics, Inc.

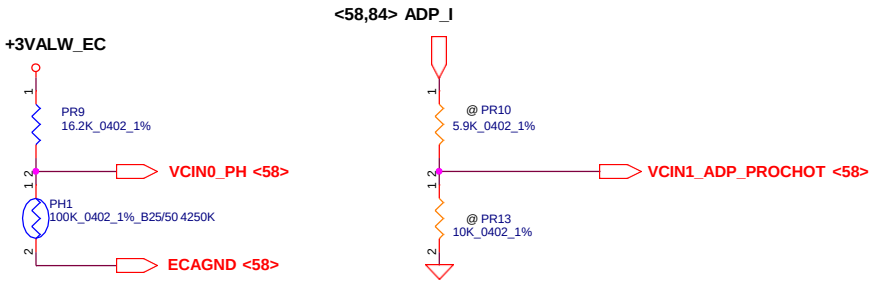
Title: DC Interface

Size: Custom | Document Number: LA-K201P | Rev: 1.0

Date: Monday, September 14, 2020 | Sheet 78 of 100







Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Title: DC Conn

Size: Document Number: 2019OPP TGL

Rev: v0.3

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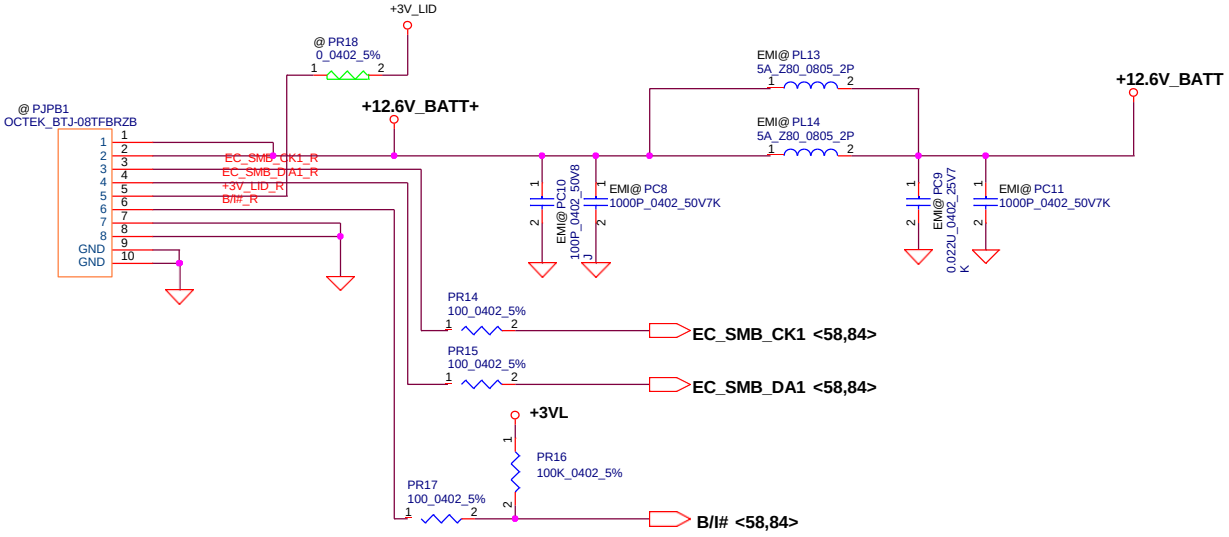

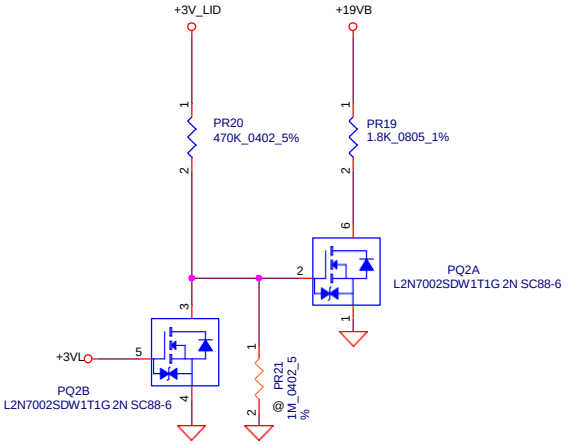

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Issued Date	2016/09/01	Deciphered Date	2019/09/01

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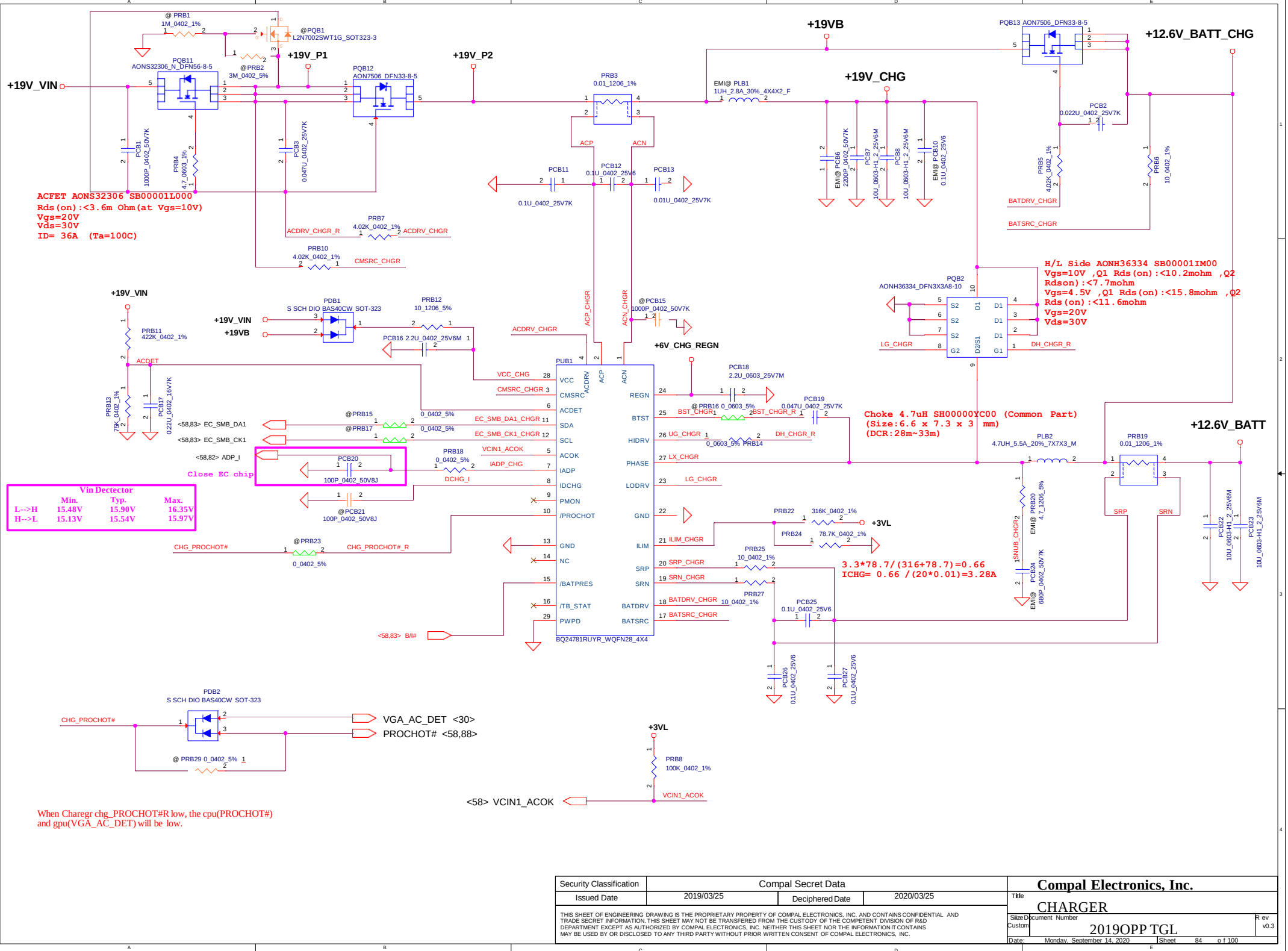
Compal Electronics, Inc.

Title: BATT Conn

Size: | Document Number: 2019OPP TGL | Rev: v0.3

Date: Monday, September 14, 2020 | Sheet 83 of 100



Security Classification	Compal Secret Data		
Issued Date	2019/03/25	Deciphered Date	2020/03/25

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Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: 2019OPP TGL | Rev: v0.3

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Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Compal Electronics, Inc.

Title: 3VALW/5VALW

Size	Document Number	Rev
Custom	2019OPP TGL	v0.3

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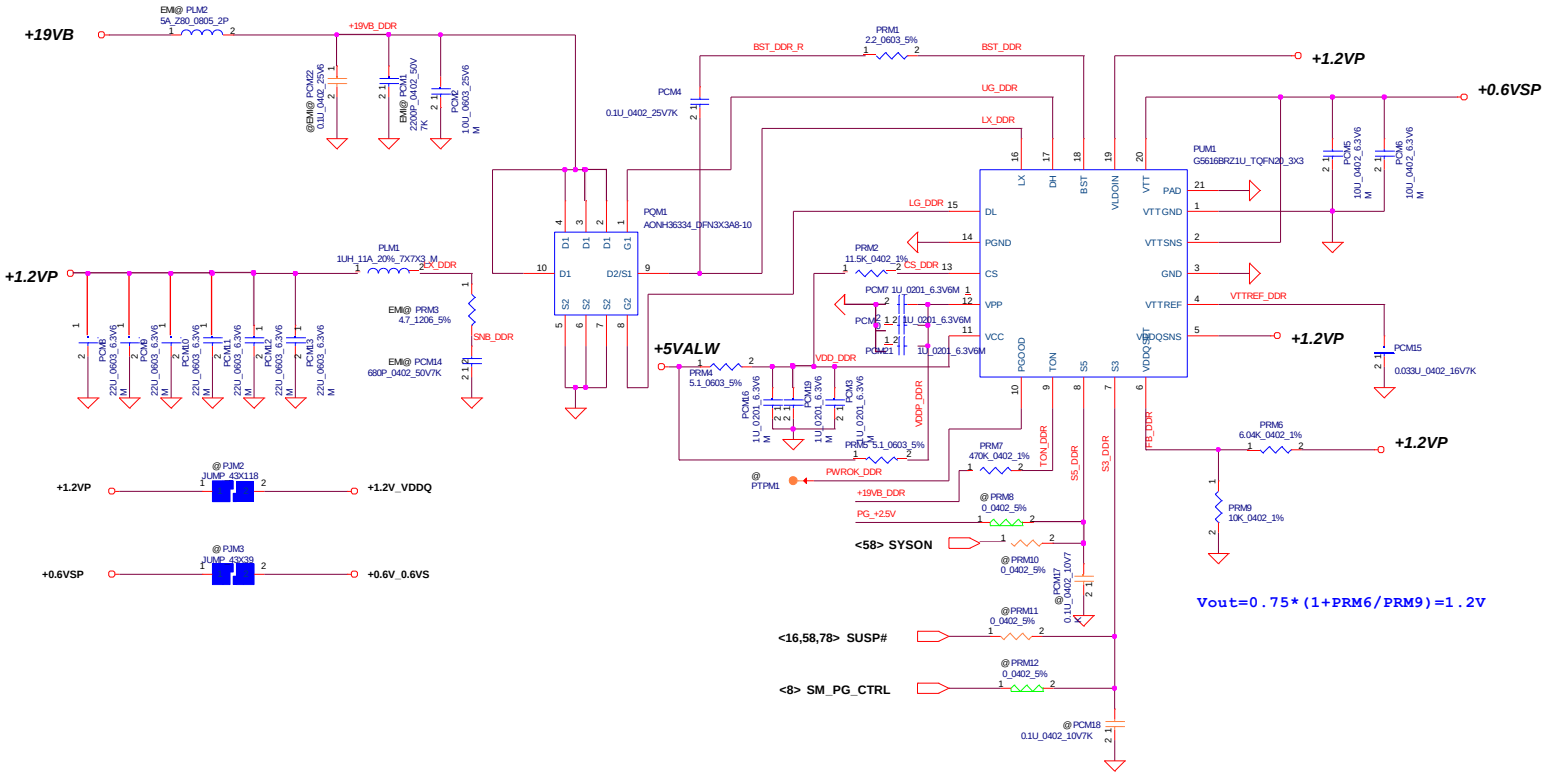

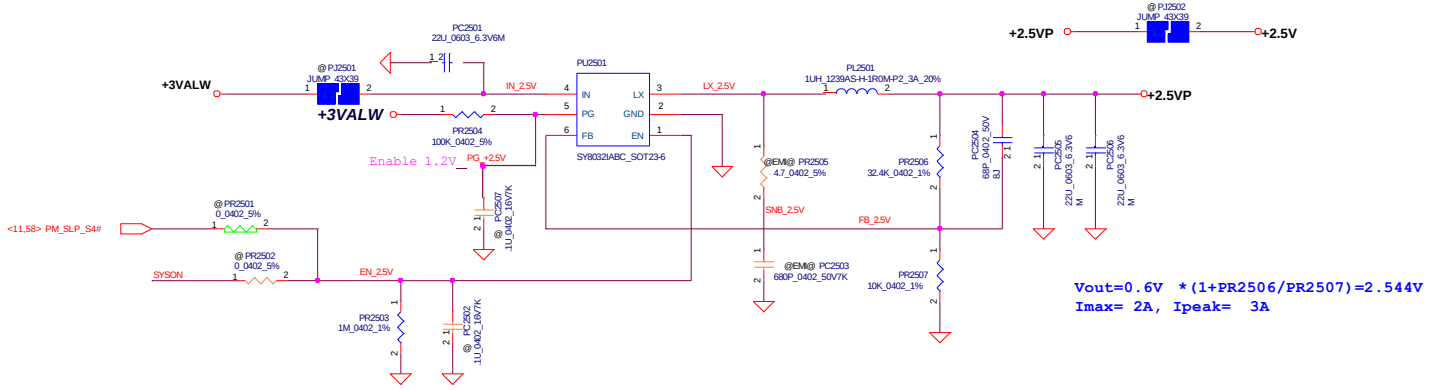

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Compal Electronics, Inc.

Title	1.2VP/0.6VSP/2.5V	
Size: C	Document Number: 2019OPP TGL	Rev: v0.3
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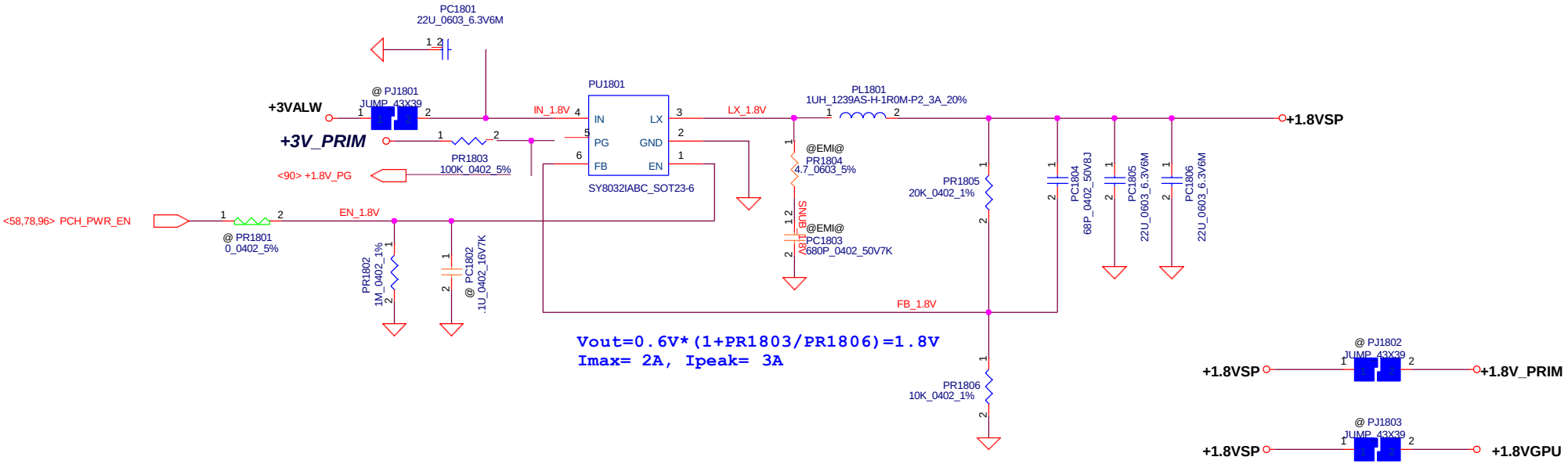

PJ1803 is for N17.

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Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Compal Electronics, Inc.

Title: +1.8V_PRIM

Size	Document Number	Rev
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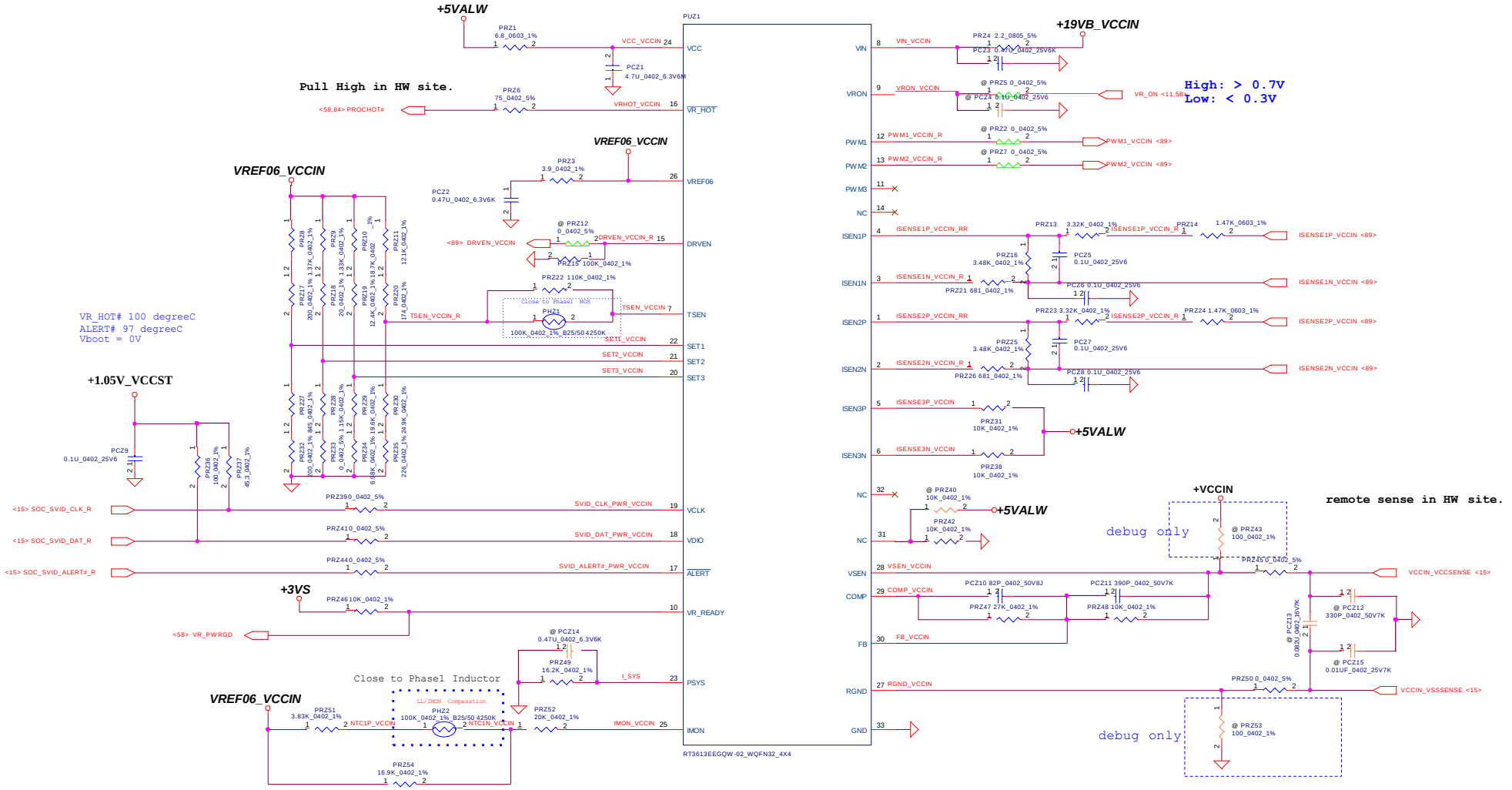
RT3613EEGQW-02 is not MP part



31 pin is a function to fix decay down slew rate to reduce acoustic noise.
High(5V): enable
Low:(0V): disable
this pin can dynamic change state.

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Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Compal Electronics, Inc.

Title: CPU_CORE

Size: Document Number: 2019OPP TGL Rev: V0.3

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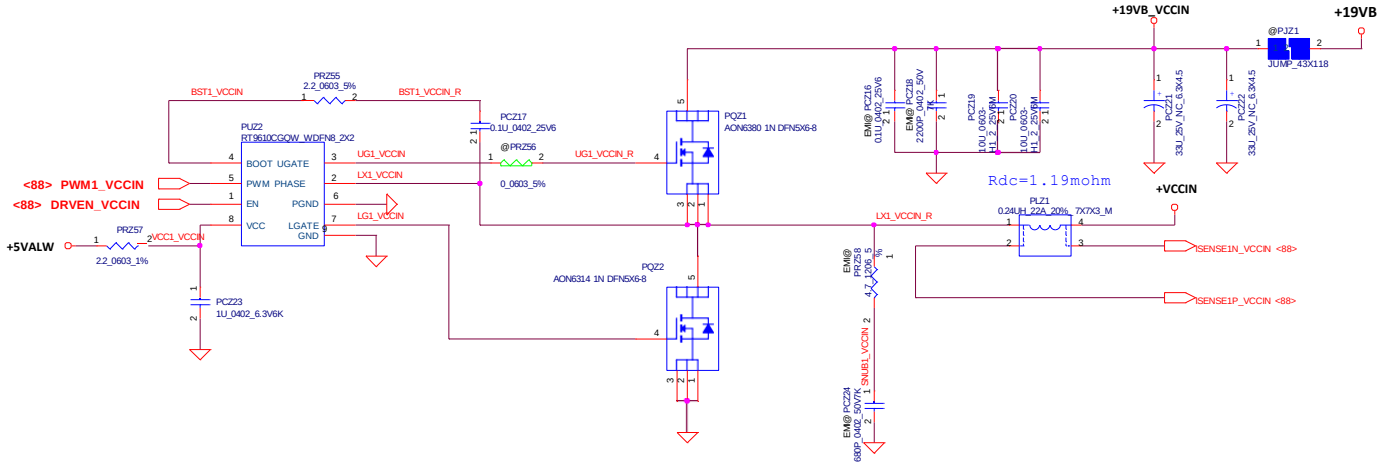
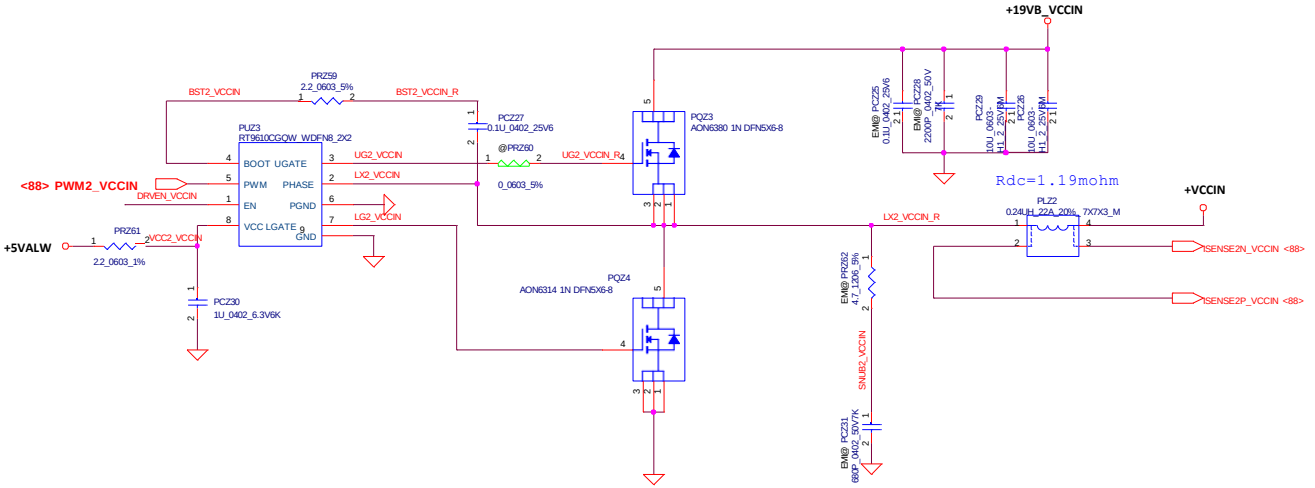
AON6380
R DS(ON) (at V GS =10V) < 6.8mohm
R DS(ON) (at V GS =4.5V) < 10.5mohm

AON6314
R DS(ON) (at V GS =10V) < 2.8mohm
R DS(ON) (at V GS =4.5V) < 3.5mohm





For 2 phase:
OCP=74.1A
ICCMAX=47A
TDC=30A
DC_LL=2mohm
AC_LL=4.4mohm

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Compal Electronics, Inc.

Title: CPU Power stage

Size	Document Number	Rev
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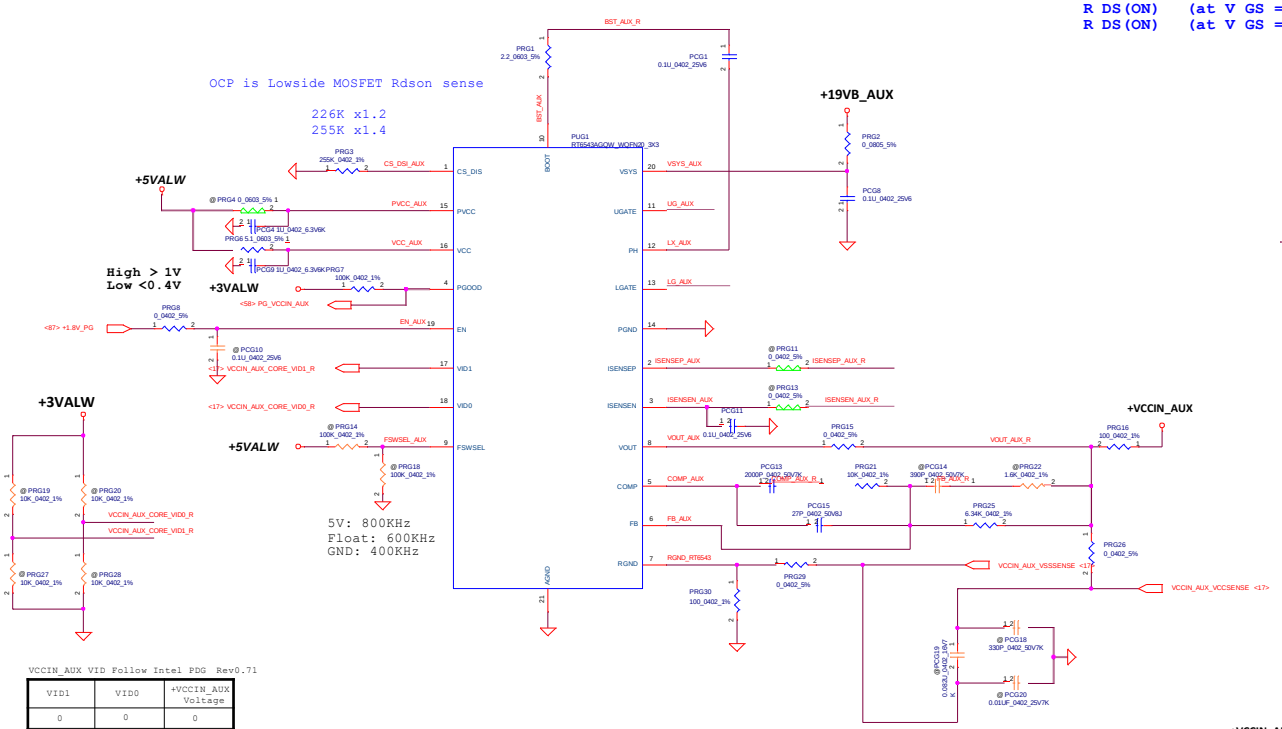
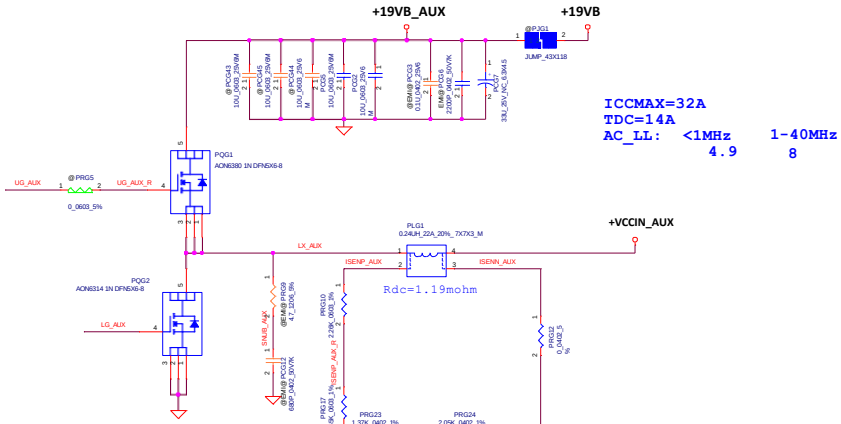
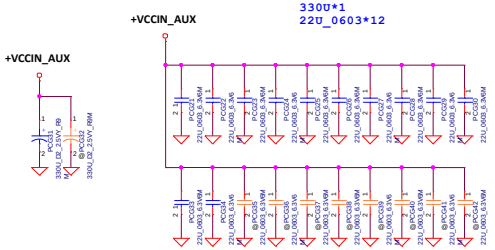
Date: Monday, September 14, 2020 Sheet 89 of 100

AON6380
R DS(ON) (at V GS =10V) < 6.8mohm
R DS(ON) (at V GS =4.5V) < 10.5mohm

AON6314
R DS(ON) (at V GS =10V) < 2.8mohm
R DS(ON) (at V GS =4.5V) < 3.5mohm







VCCIN_AUX VID Follow Intel PDG Rev0.71

VID1	VID0	+VCCIN_AUX Voltage
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

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Issued Date	2016/09/01	Deciphered Date: 2019/09/01

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Compal Electronics, Inc.

Title: VCCINAUX

Size: Document Number: 2019QPPTGL Rev: 0.3

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PWM-VID Spec and component Values

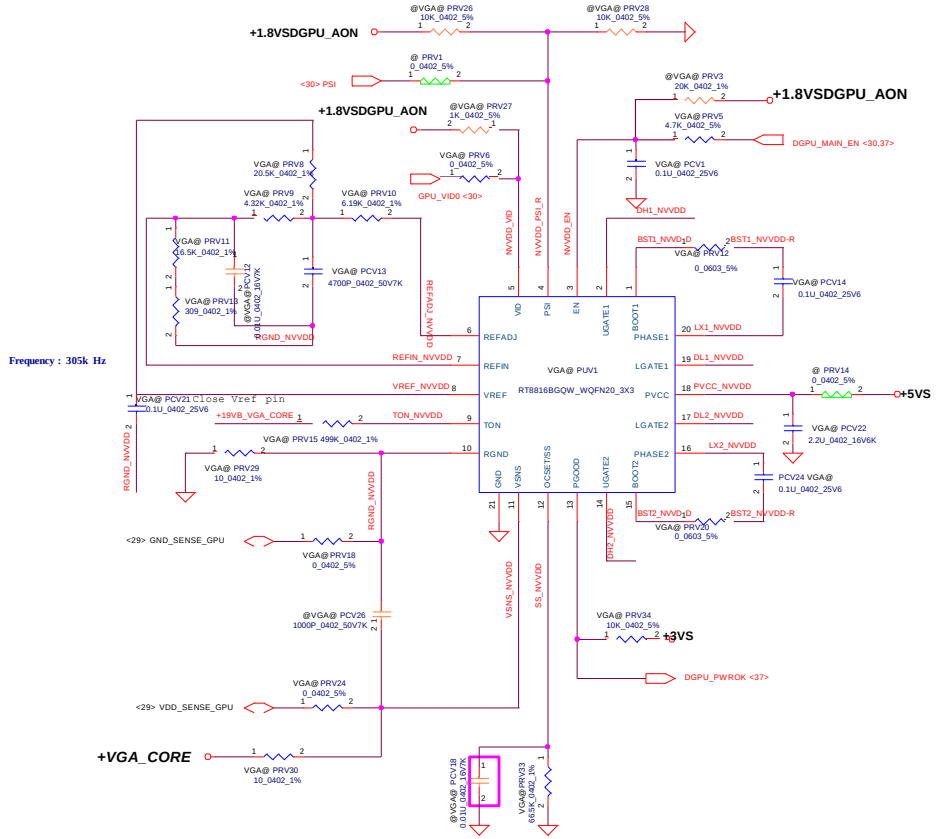
PWM-VID Spec		
Vmin		0.3V
Vmax		1.3V
Vboot		0.8V
Voltage step		6.25mV
N of Voltage level		160
Rrefadj	PRV10	6.19K
Rref1	PRV8	20.5K
Rboot	PRV9	4.32K
Rref2=PRV8+PRV11	PRV11	16.5K
	PRV13	0.309K
C	PCV13	4.7nf

VGA Chip	N17S-G5
OpenVReg Configurations	
Rated TDP Power at Tj=102C	25W
EDP-Continuous at Tj=102C	35A
EDP-Peak at Tj=102C	70A
Istep max (Evaluation)	A
OCP Setting Current	92A
Rocset	66.5K
Recommendation	2phase

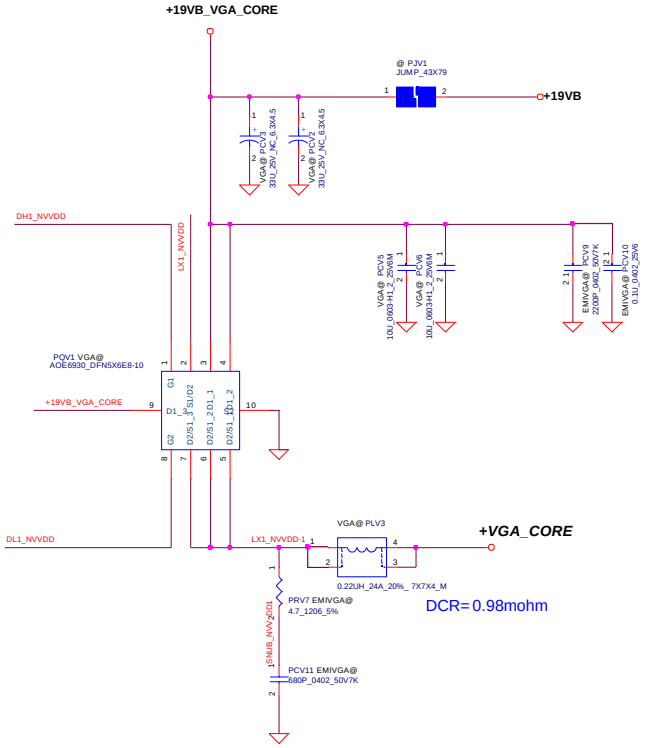
VGA Chip	N18S-G5
OpenVReg Configurations	
Rated TDP Power at Tj=102C	25W
EDP-Continuous at Tj=102C	35A
EDP-Peak at Tj=102C	75A
Istep max (Evaluation)	A
OCP Setting Current	92A
Rocset	66.5K
Recommendation	2phase

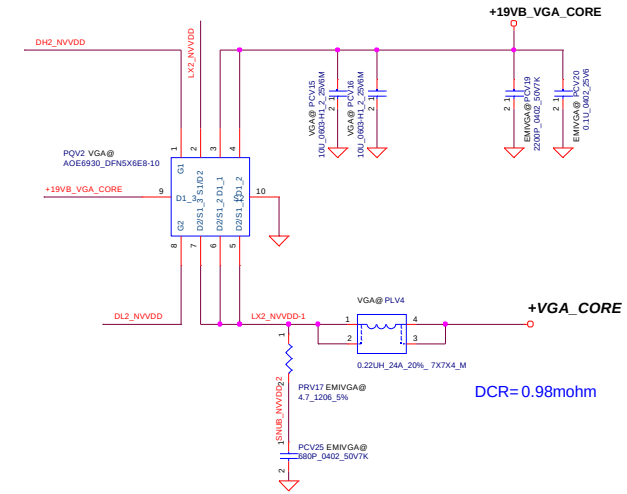
VGA N17@
TDC = 35A
Ipeak = 78A
OCP = 92A(valley)

VGA N18@
TDC = 30A
Ipeak = 75A
OCP = 92A(valley)



Frequency : 305k Hz





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Issued Date	2015/09/01	Deciphered Date	2018/09/01

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Compal Electronics, Inc.

Title: VGA_CORE

Size: Document Number: 2019OPP TGL

Rev: v0.3

Date: Monday, September 14, 2020

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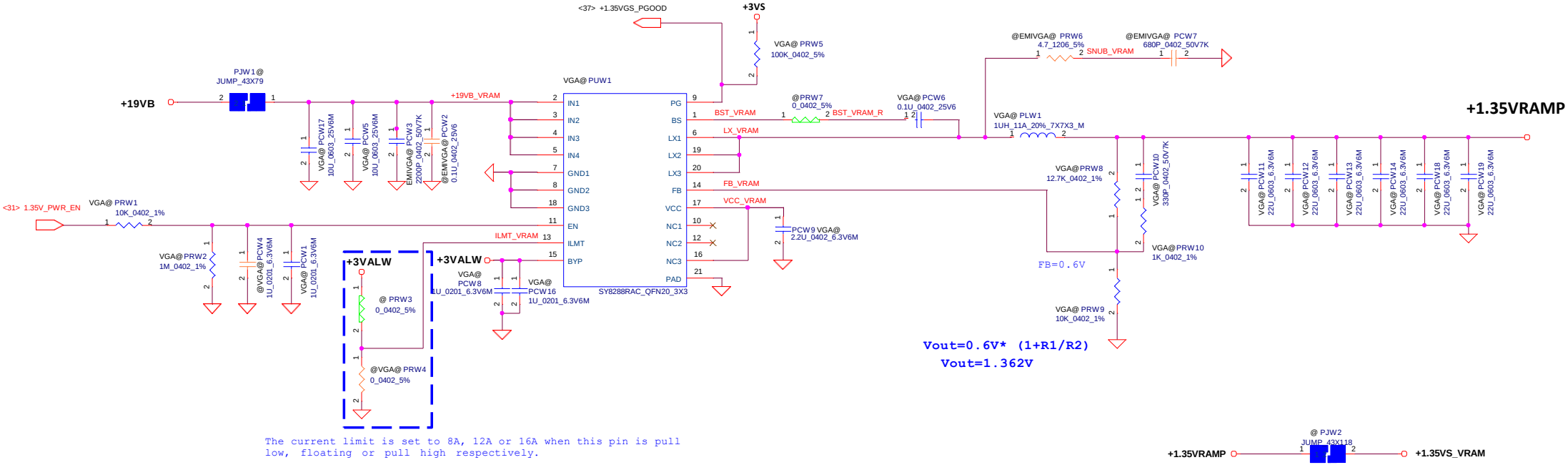
VGA N17@
TDC = 7.1A
Ipeak = 7.6A

VGA N18@
TDC = 7A
Ipeak = 8A



Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Compal Electronics, Inc.

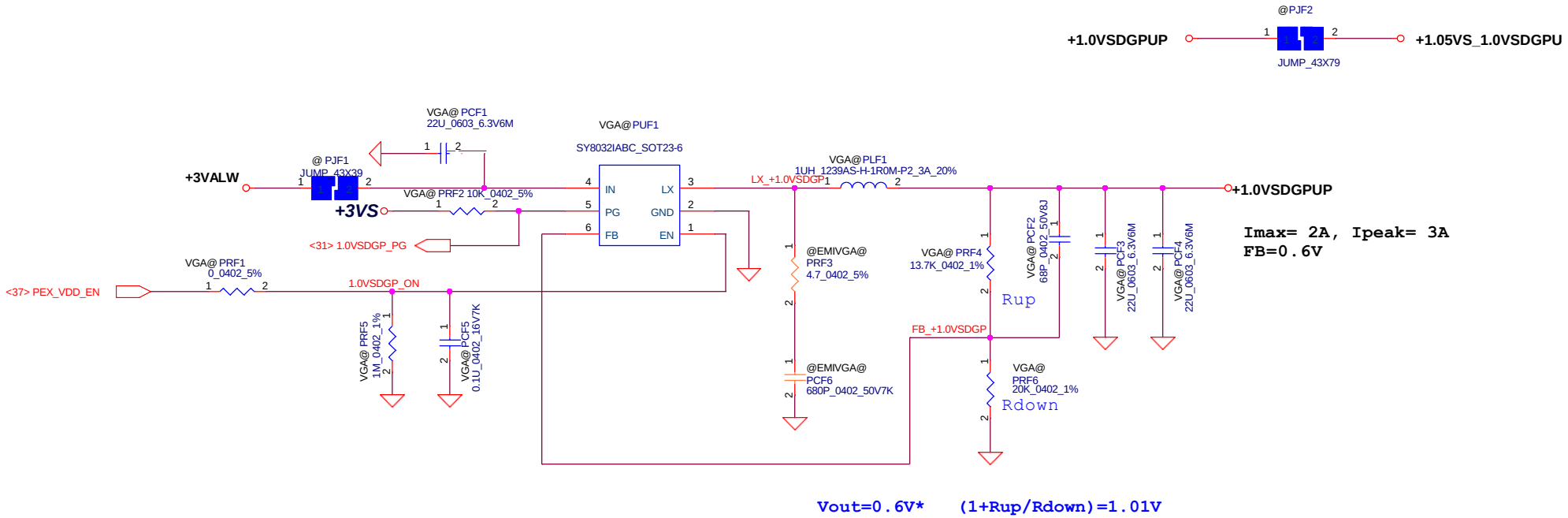
Title: +1.35VS_VRAM

Size: Document Number: 2019OPP TGL Rev: V0.3

Date: Monday, September 14, 2020 Sheet 94 of 100

VGA N17@
TDC = 0.3A
Ipeak = 0.4A

VGA N18@
TDC = 1.6A
Ipeak = 1.9A



Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Compal Electronics, Inc.

Title	+1.0VSDGPU	
Size	Document Number: 2019OPP TGL	Rev: v0.3
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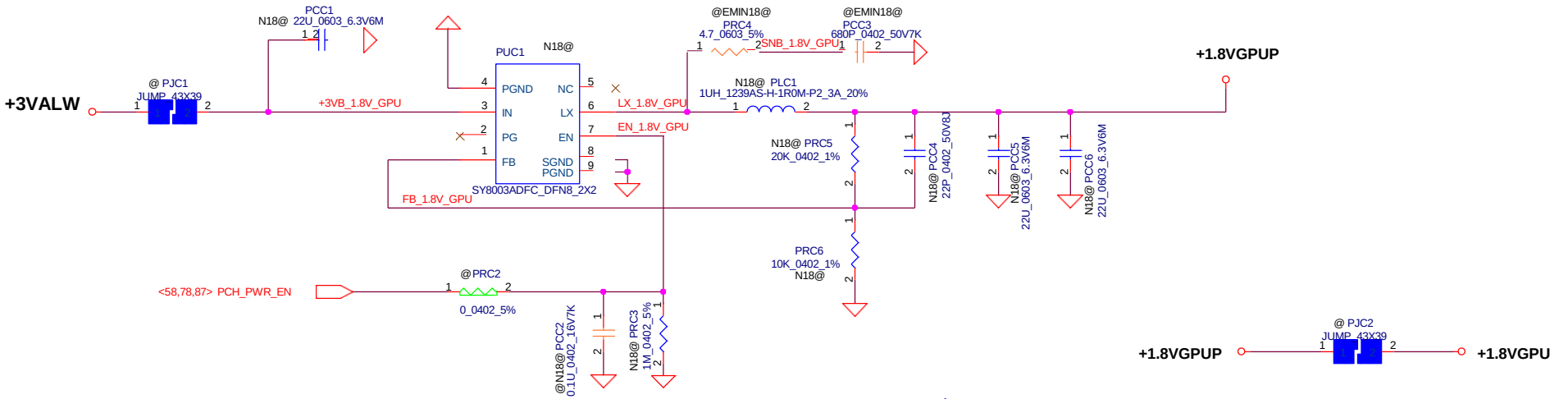

Vout=0.6V*(1+PR1803/PR1806)=1.83V
Imax= 3A
current limit=3.5A

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

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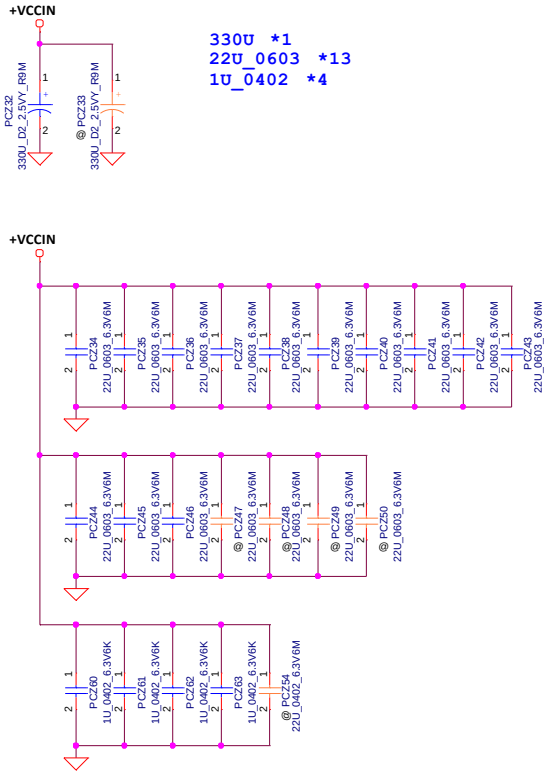
Compal Electronics, Inc.

Title: +1.8V_GPU

Size: B | Document Number: 2019OPP TGL | Rev: v0.3

Date: Monday, September 14, 2020 | Sheet 96 of 100



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Issued Date	2016/09/01	Deciphered Date	2019/09/01

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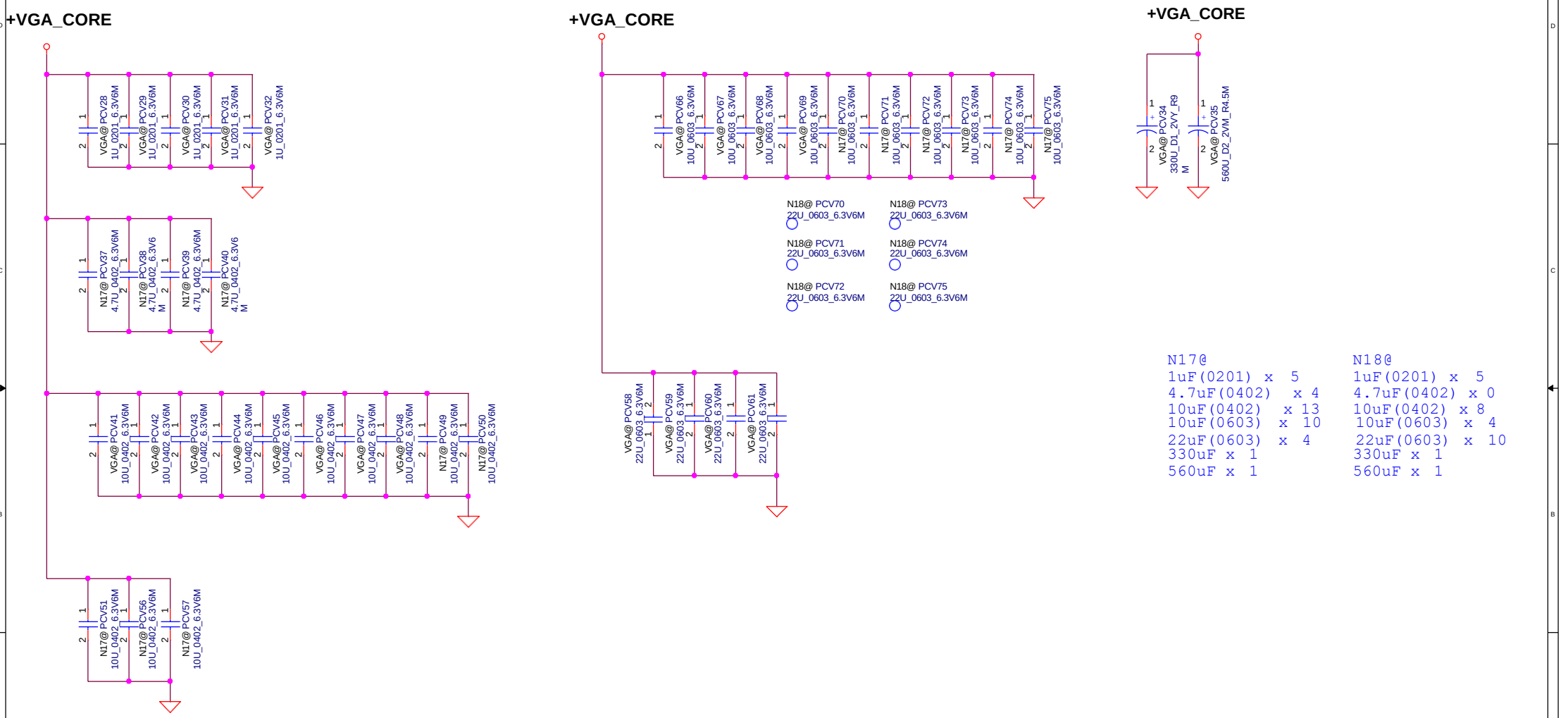
Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size: Document Number: 2019OPP TGL

Rev: v0.3

Date: Monday, September 14, 2020



N17@	N18@
1uF(0201) x 5	1uF(0201) x 5
4.7uF(0402) x 4	4.7uF(0402) x 0
10uF(0402) x 13	10uF(0402) x 8
10uF(0603) x 10	10uF(0603) x 4
22uF(0603) x 4	22uF(0603) x 10
330uF x 1	330uF x 1
560uF x 1	560uF x 1

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2018/09/01

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Compal Electronics, Inc.

Title: VGA CHIP DECOUPLING

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Date: Monday, September 14, 2020 | Sheet 93 of 100

Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

BOM Structure Table (1/2)

Funct i on	*Stuf f*	*Un-Stuff*
DGPU SKU	PX@	
UMA SKU	UMA@	
TPM	TPM@	

SOC SMBUS Address Table

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBCLK SMBDATA	+3V_PRIM	DIMM1	0x50	0xA0	0xA1
		DIMM2	0x52	0xA4	0xA5
		Touch PAD	0x15	0x58	0x59

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port 2	+3VS	dGPU	
		Thermal Sensor	0x90
		PCH	

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

HDMI 45@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM

RO0000003HM

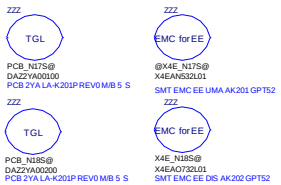
<USB2.0 port>

USB2.0 port	DESTINATION
1	USB3.0(S/B)
2	USB3.0(S/B)
3	USB3.0 Type-C
4	Card Reader
5	Camera
6	Fingerprint
7	X
8	X
9	X
10	Bluetooth

<PCI-E,SATA,USB3.0/CLK>

Lane#	PCI-E	SATA	USB3.0		DESTINATION		CLK
0	1			1	USB3.0(S/B)		X
1	2			2	USB3.0(S/B)		X
2	3			3	USB3.0 Type-C		X
3	4			4			
4	5				PCIe x4	SSD	CLK3
5	6						
6	7						
7	8						
8	9				LAN		CLK1
9	10				WLAN		CLK2
10	11	0			HDD		X
11	12	1			SATA	SATA SSD	X

Lane#	PCI-E 4	DESTINATION	CLK
0	1	DGPU	CLK0
1	2		
2	3		
3	4		



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Issued Date	2018/05/17	Deciiphered Date 2021/05/17	Title: Notes List

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Size: Document Number:	Custom: LA-K201P	Rev: 1.0
Date: Monday, September 14, 2020	Sheet: 3 of 100	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							

Security Classification	Compal Secret Data		
Issued Date	2019/05/07	Deciphered Date	2018/12/31

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Title		
Size: Custom	Document Number	Rev: 0.5
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