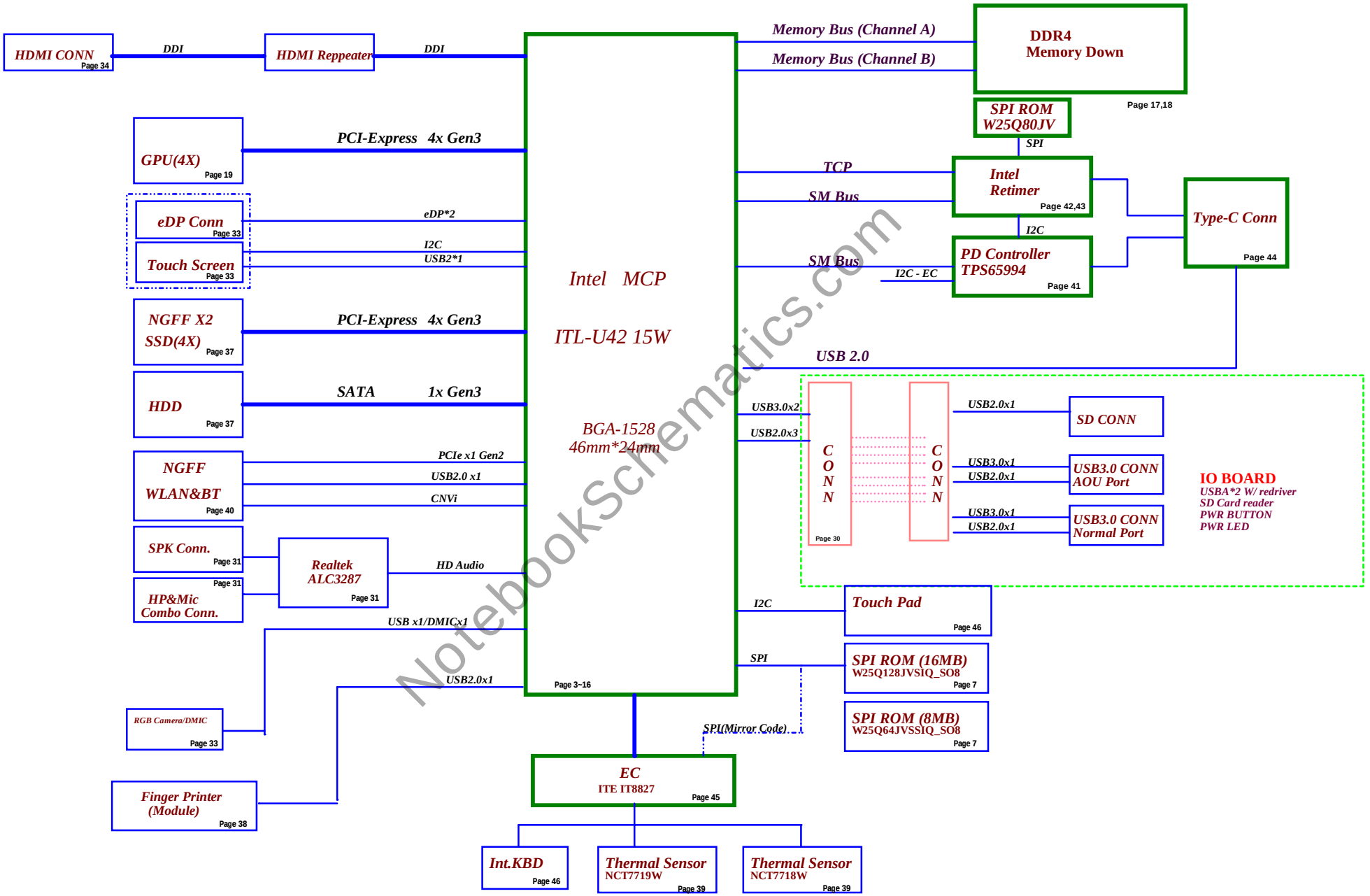
LCFC Confidential

S550 MB Schematic Document

Tiger Lake_U42 with DDR4

2020-02
REV:0.1

Title	S550-ITL	
Size: C	Document Number: Cover Page	Rev: 0.1
Date: Thursday, May 28, 2020	Sheet 1 of 61	



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2019/08/20

Title	S550-IIL		
Size	Document Number		Rev
C	Block Diagram		0.1
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V9B+	+3VALW +5VALW	+1.8VALW +3ALW_PCH	+1.2V +2.5V_DDR +VCCST +VCCIN +VCCIN_AUX	+5VS +3VS +1.8VS +0.6VS	+VCCSTG
S0	O	O	O	O	O	O
S0IX	O	O	O	O	O	X
S5 S4 AC Only	O	O	O	X	X	X
S5 S4 Battery only	O	O	X	X	X	X

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001_001xb
Battery	0x34

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7719W)	1001_101xb
Thermal Sensor(NCT7718W)	1001_100xb
GPU	0x9E

EC SMBus3 address

Device	Address
PMIC	0X34

PCH SM Bus address

Device	Address
PD	

BOM Structure	BTO Item
@	Un-stuff
14@	For 14" part
15@	For 15" part
BL@	For KB backlight part
EMC@	For EMC part
EMC_14@	For EMC 14" part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC un-stuff part
ME@	For ME@
MP@	For MP part
NPI@	For NPI part
CNVI@	For CNVI WLAN
DDP@	For DDP MD part
SDP@	For SDP MD part
RF@	For RF part
RF_NS@	For RF un-stuff part

HSIO PORT		Function
USB3.0	1	USB Type-C1
	2	USB Type-A AOU
	3	USB Type-A
	4	USB Type-C2
	5	NC
	6	NC
USB2.0	1	USB Type-A AOU
	2	USB Type-A
	3	NC
	4	Finger Printer
	5	NC
	6	NC
	7	CAMERA
	8	USB Type-C1
	9	USB Type-C2
	10	BT
PCIE	1~8	1~4 SUB3.0 5~4 NC
	9	WLAN
	10~12	NC
	13~16 X4	SSD-2

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Title	S550-IIL		
Size	Document Number		Rev
C	Notes List		0.1
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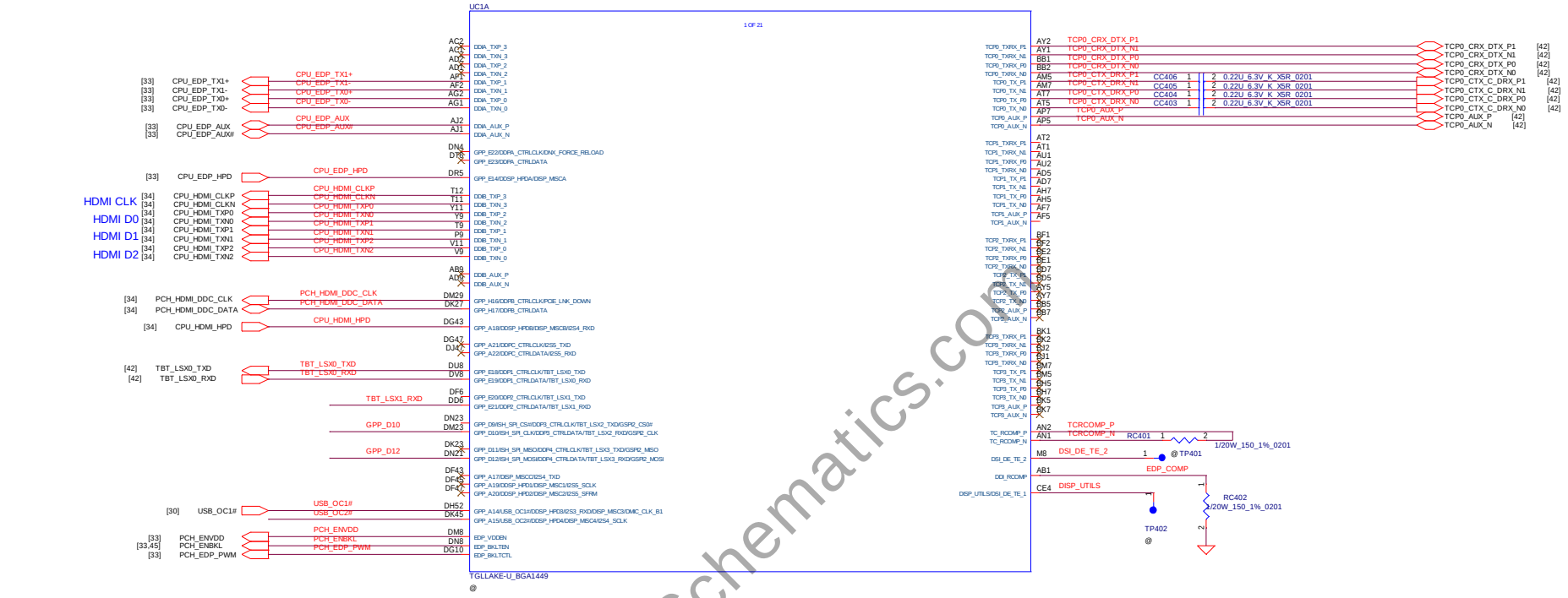
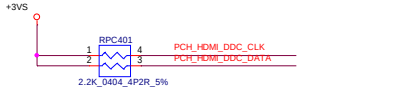
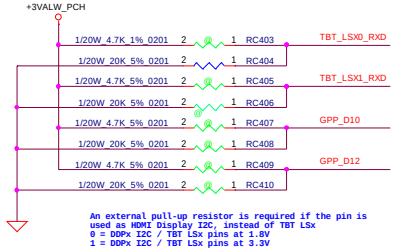
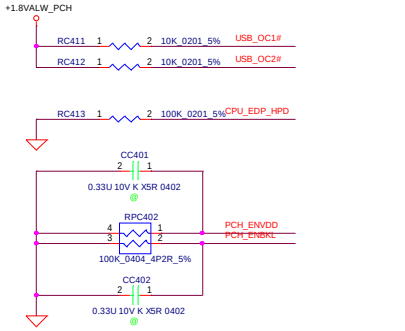




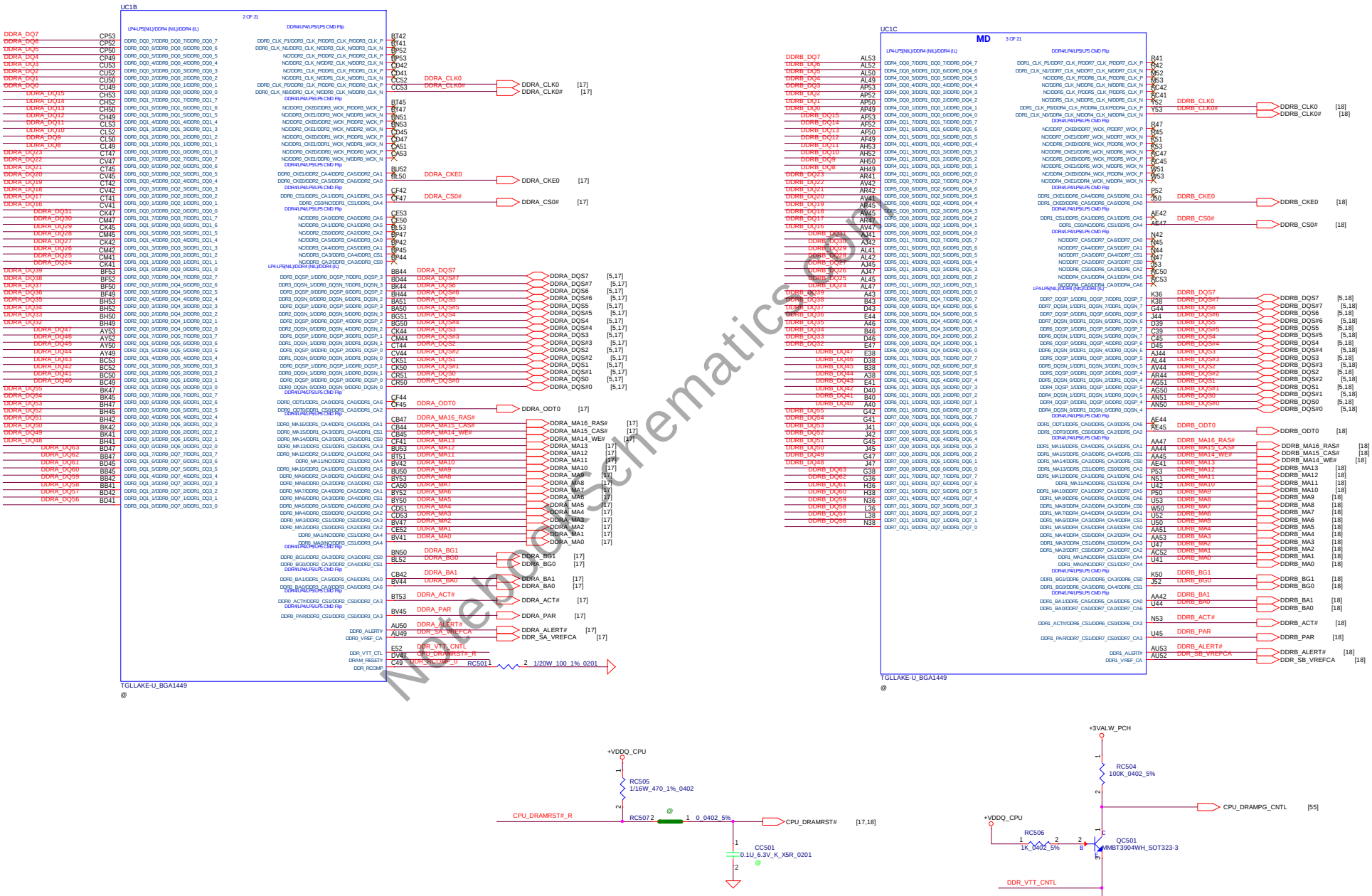




GPIO Group	Power Supply
GPP_A	1.8V
GPP_B/C/D/E	3.3V
GPP_F	1.8V(only)
GPP_G/H	3.3V
GPP_R/S	1.8V
GPD	3.3V(only)

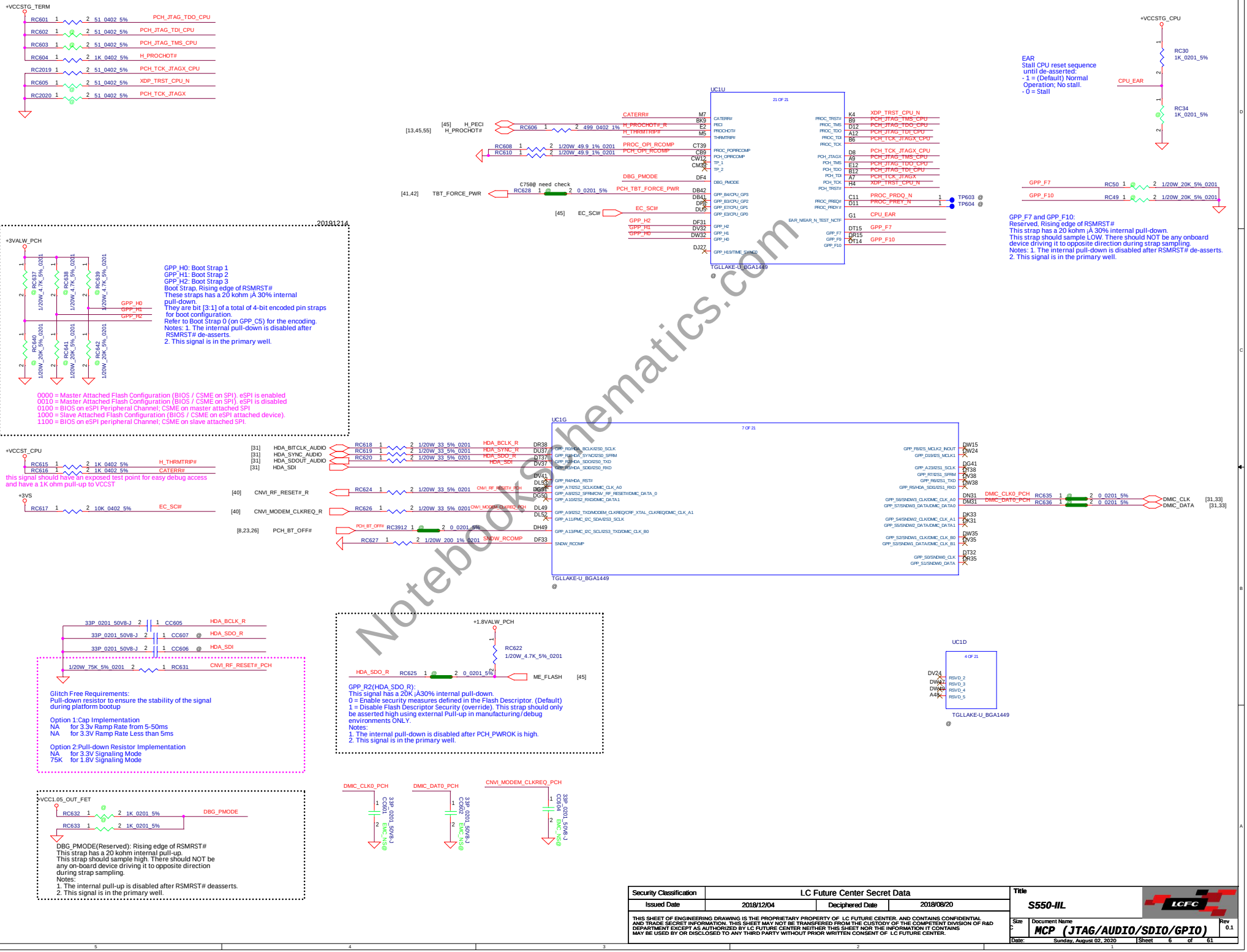
Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

Title	S550-IIL		
Size	Document Name		Rev
C	MCP (DDI/EDP/HDMI)		0.1
Date:	Thursday, May 28, 2020	Sheet	4 of 61



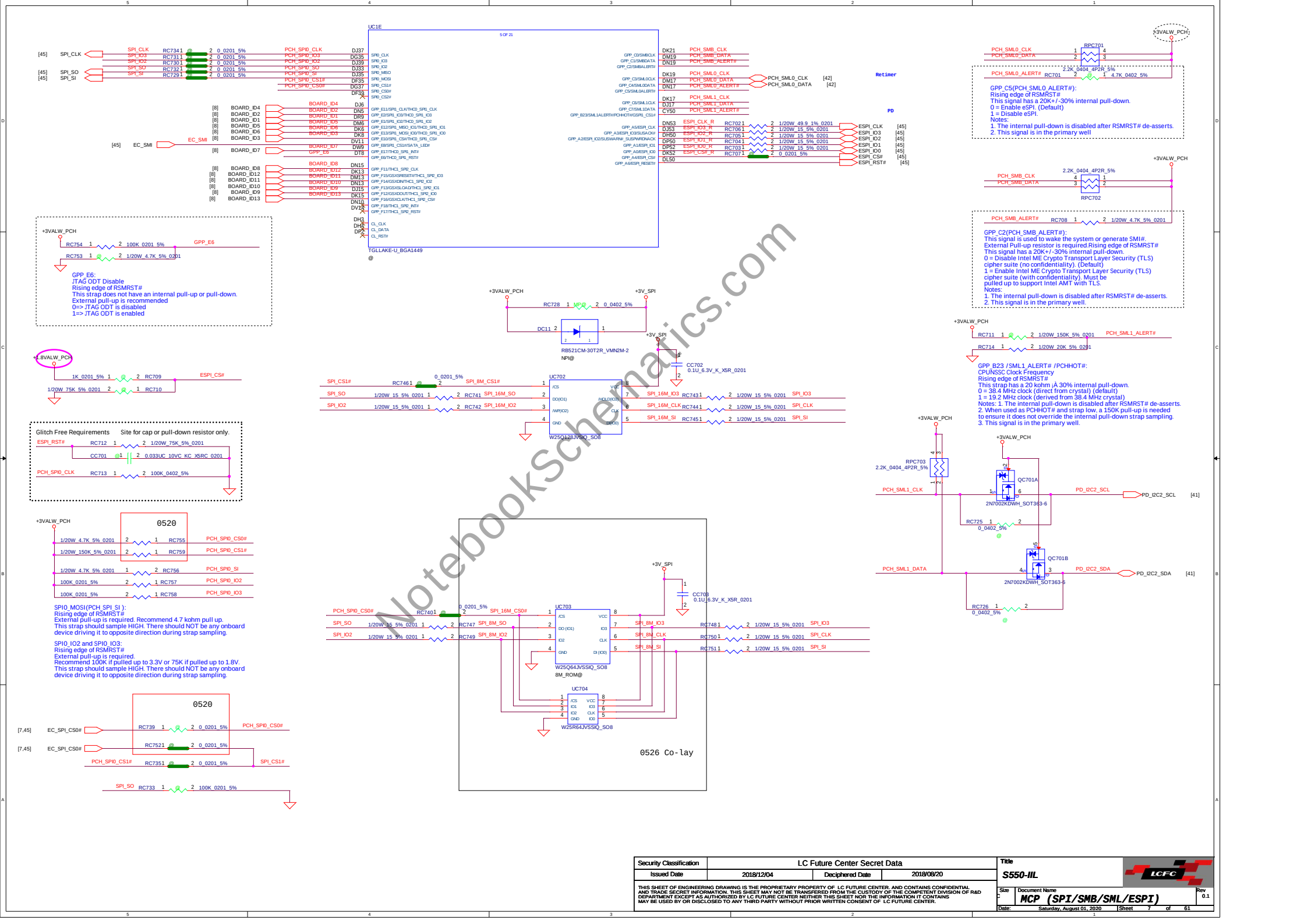
Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

Title	S550-IIL		
Size: C	Document Name: MCP (DDR4)		Rev: 0.1
Date: Thursday, July 30, 2020	Sheet 5 of 61		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

Title	S550-IIL		
Size	Document Name		Rev
C	MCP (JTAG/AUDIO/SDIO/GPIO)		0.1
Date:	Sunday, August 02, 2020	Sheet	6 of 61



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Issued Date	2018/12/04	Deciphered Date	2019/08/20

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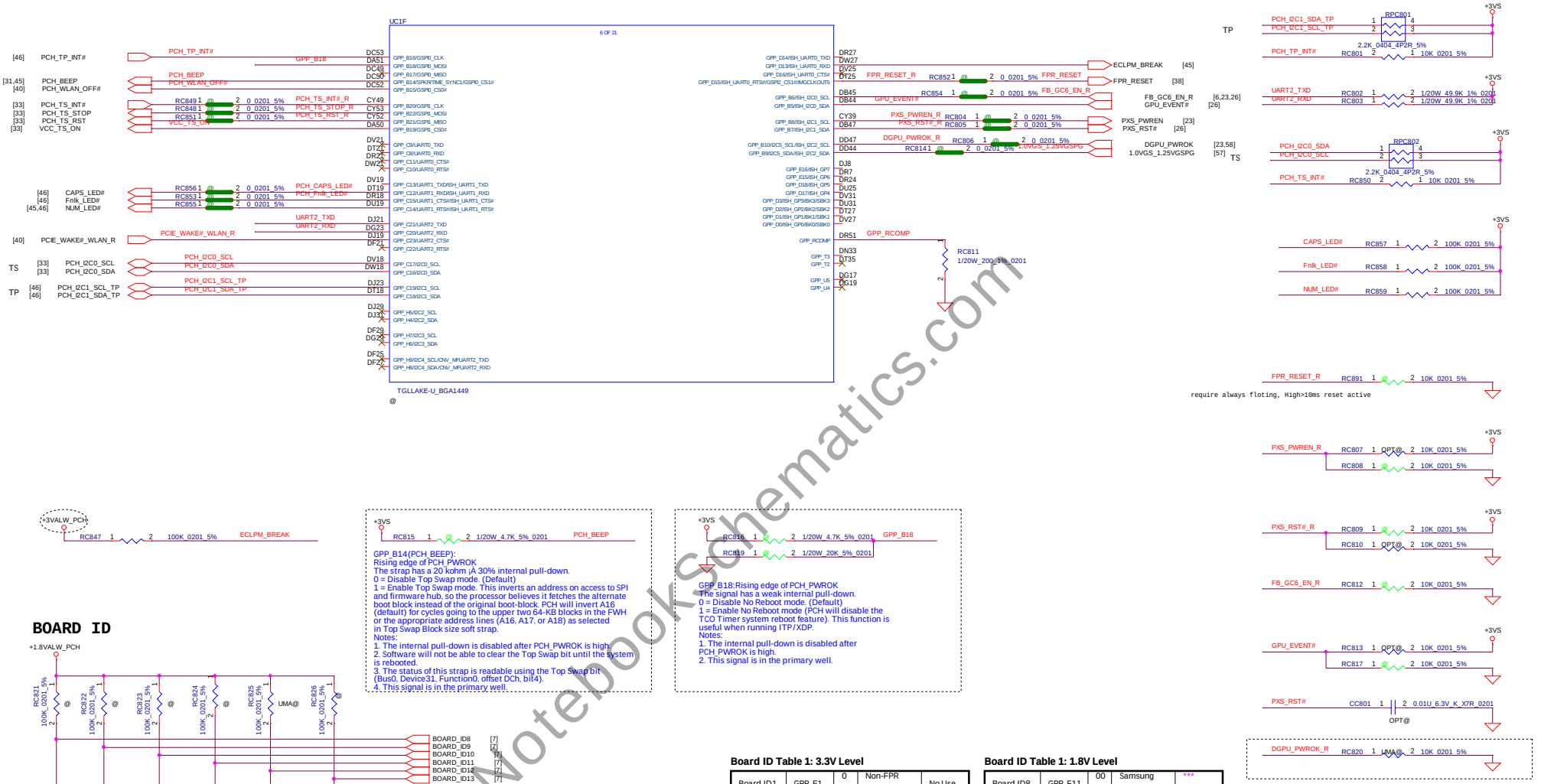
Title	S550-IIL		
Size	Document Name		Rev
C	MCP (SPI/SMB/SML/ESPI)		0.1
Date:	Saturday, August 01, 2020	Sheet 7	of 61

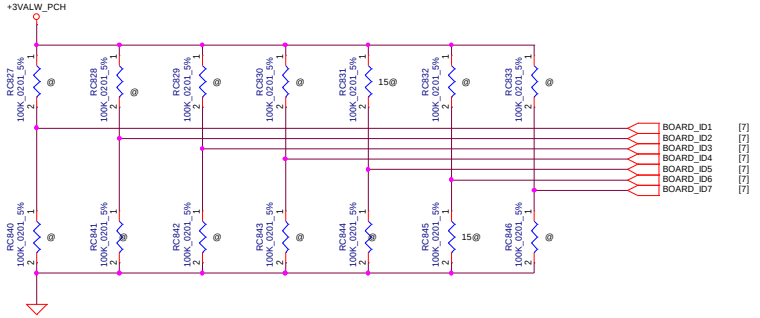


GPP_B14(PCH_BEEP):
Rising edge of PCH_PWROK
The strap has a 20 kohm ¡Ó 30% internal pull-down.
0 = Disable Top Swap mode. (Default)
1 = Enable Top Swap mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap.
Notes:
1. The internal pull-down is disabled after PCH_PWROK is high.
2. Software will not be able to clear the Top Swap bit until the system is rebooted.
3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4).
4. This signal is in the primary well.

GPP_B18:Rising edge of PCH_PWROK
The signal has a weak internal pull-down.
0 = Disable No Reboot mode. (Default)
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
Notes:
1. The internal pull-down is disabled after PCH_PWROK is high.
2. This signal is in the primary well.

BOARD ID

BOARD ID



Board ID Table 1: 3.3V Level

Board ID1	GPP_E1	0	Non-FPR	No Use
		1	FPR	
Board ID2	GPP_E2	0	Non-TS	No Use
		1	TS	
Board ID3	GPP_E10 H	00	FHD	***
		01	UHD	No Use
Board ID4	GPP_E11 L	10	FHD HDR	***
		11	Reserved	No Use
Board ID5	GPP_E12 H	00	13"	No Use
		01	14"	***
Board ID6	GPP_E13 L	10	15"	***
		11	17"	No Use
Board ID7	GPP_E17	0	Non-TPM	No Use
		1	TPM	

Board ID Table 1: 1.8V Level

Board ID8	GPP_F11 H	00	Samsung	***
		01	Micro	***
Board ID9	GPP_F12 L	10	Hynix	***
		11		No Use
Board ID10	GPP_F13 H	00	4G	No Use
		01	8G	***
Board ID11	GPP_F14 L	10	12G	***
		11	16G	***
Board ID12	GPP_F15	0	OPT	No Use
		1	UMA	Reserved for dGPU
Board ID13	GPP_F16	10		
		11		
				No Use
				Reserved for Project

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Title	S550-IIL		
Size	Document Name		Rev
C	MCP (UART/I2C/ISH/GSPI)		0.1
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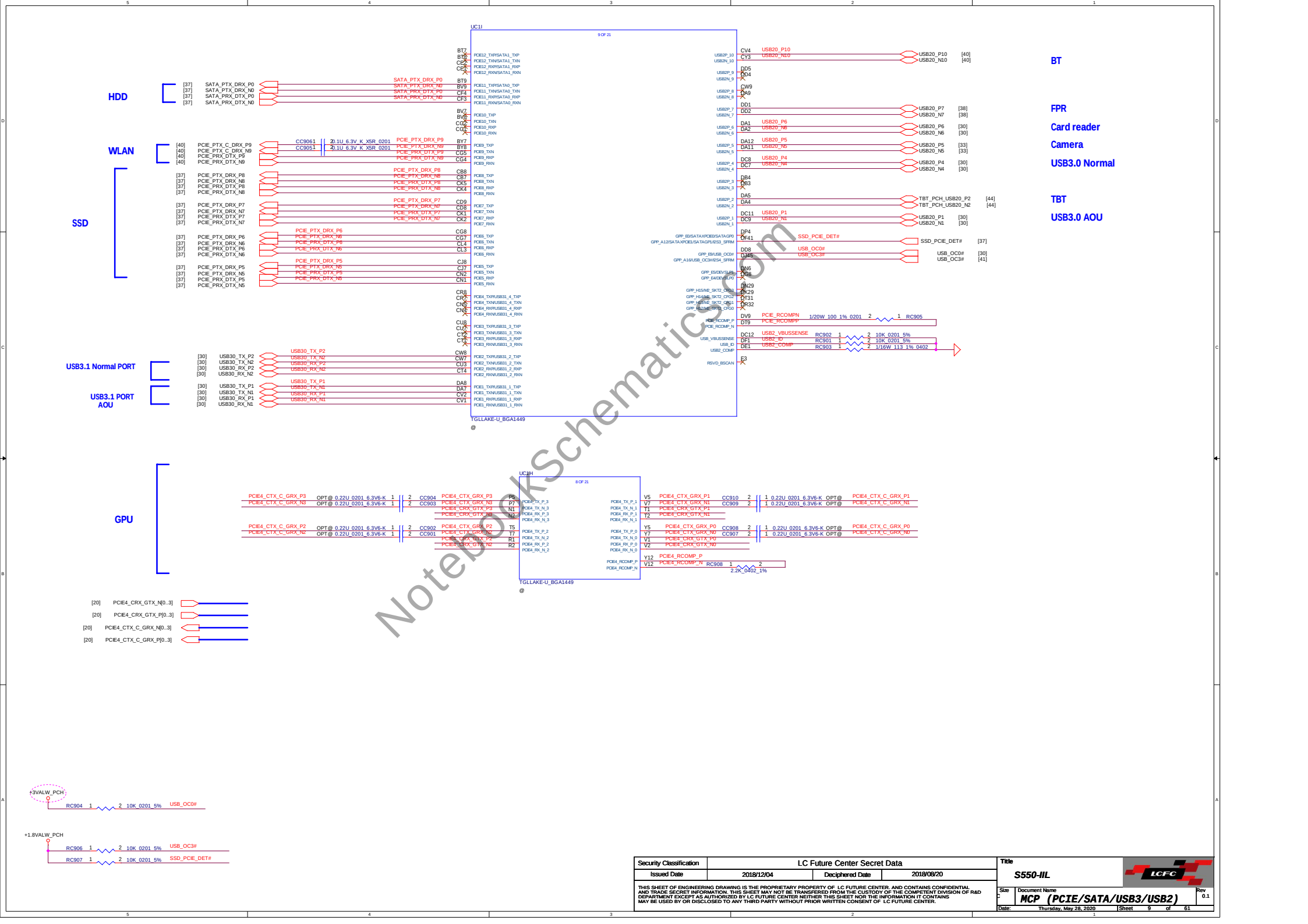

Security Classification	LC Future Center Secret Data		
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Title: S550-IIL

Size	Document Name	Rev
C	MCP (PCIE/SATA/USB3/USB2)	0.1

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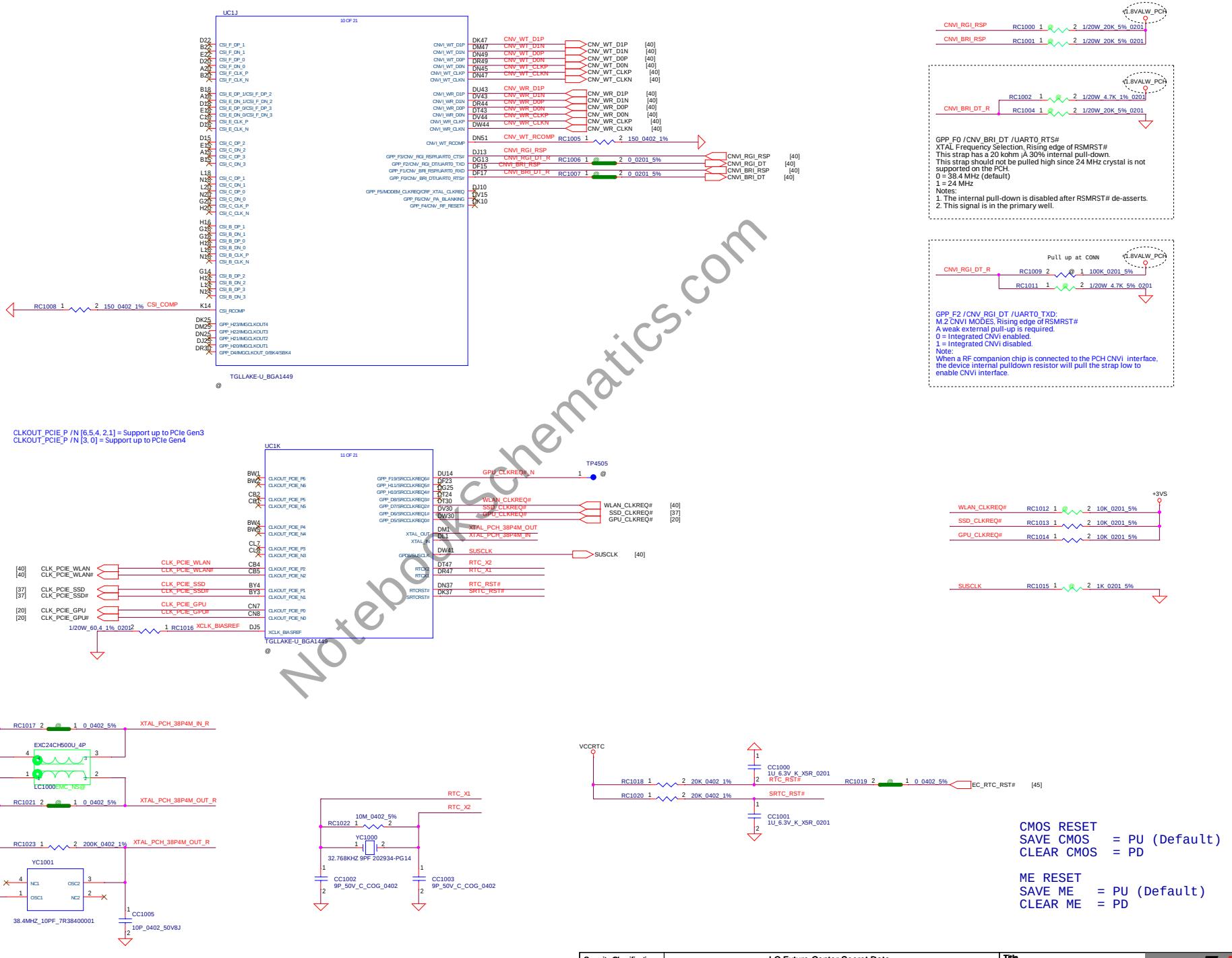

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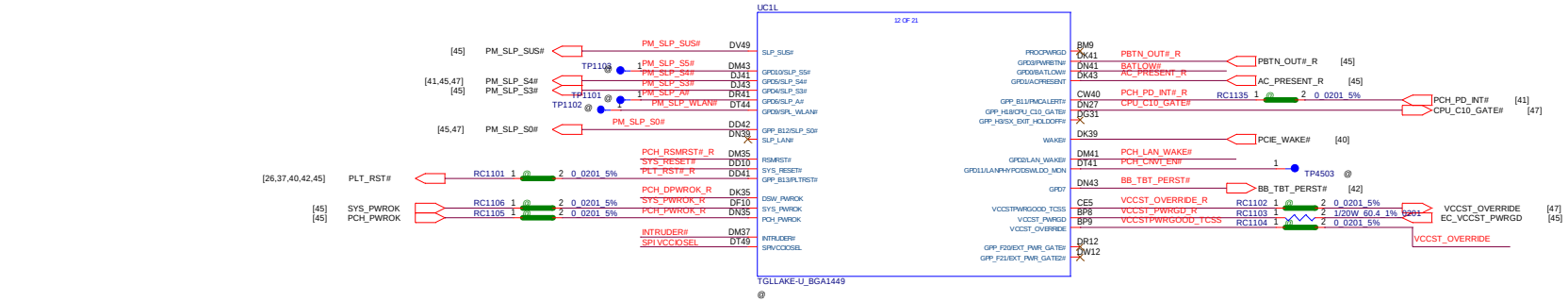
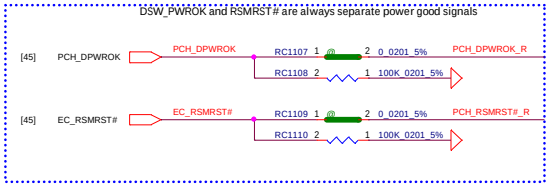
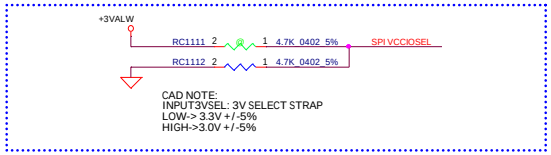
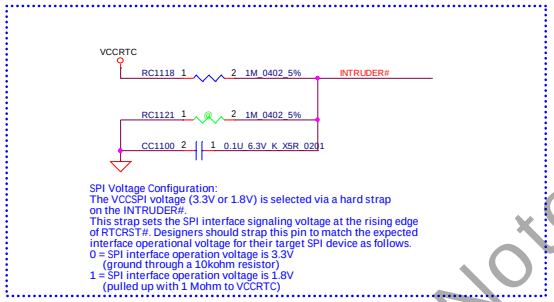
Issued Date	2018/12/04	Deciphered Date	2019/08/20

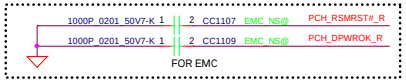
Title	S550-IIL		
Size	Document Name		Rev
C	MCP (CSI/EMMC/CNVI/CLK)		0.1
Date:	Saturday, August 01, 2020	Sheet 10 of 61	

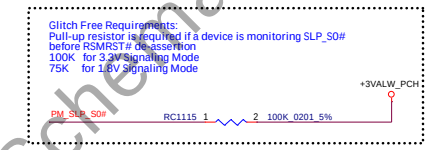


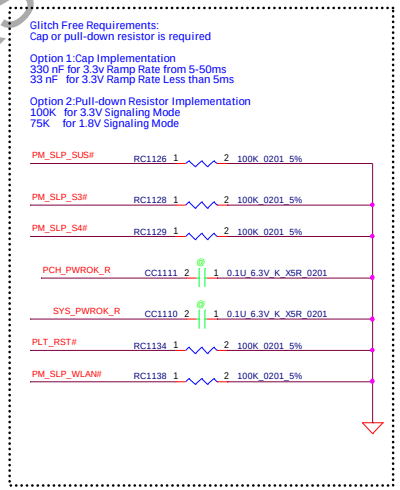


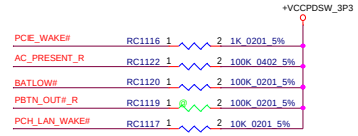


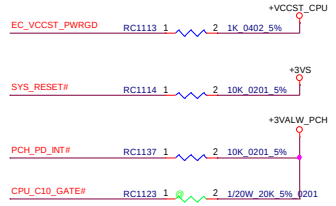


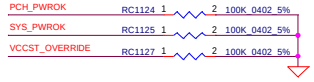






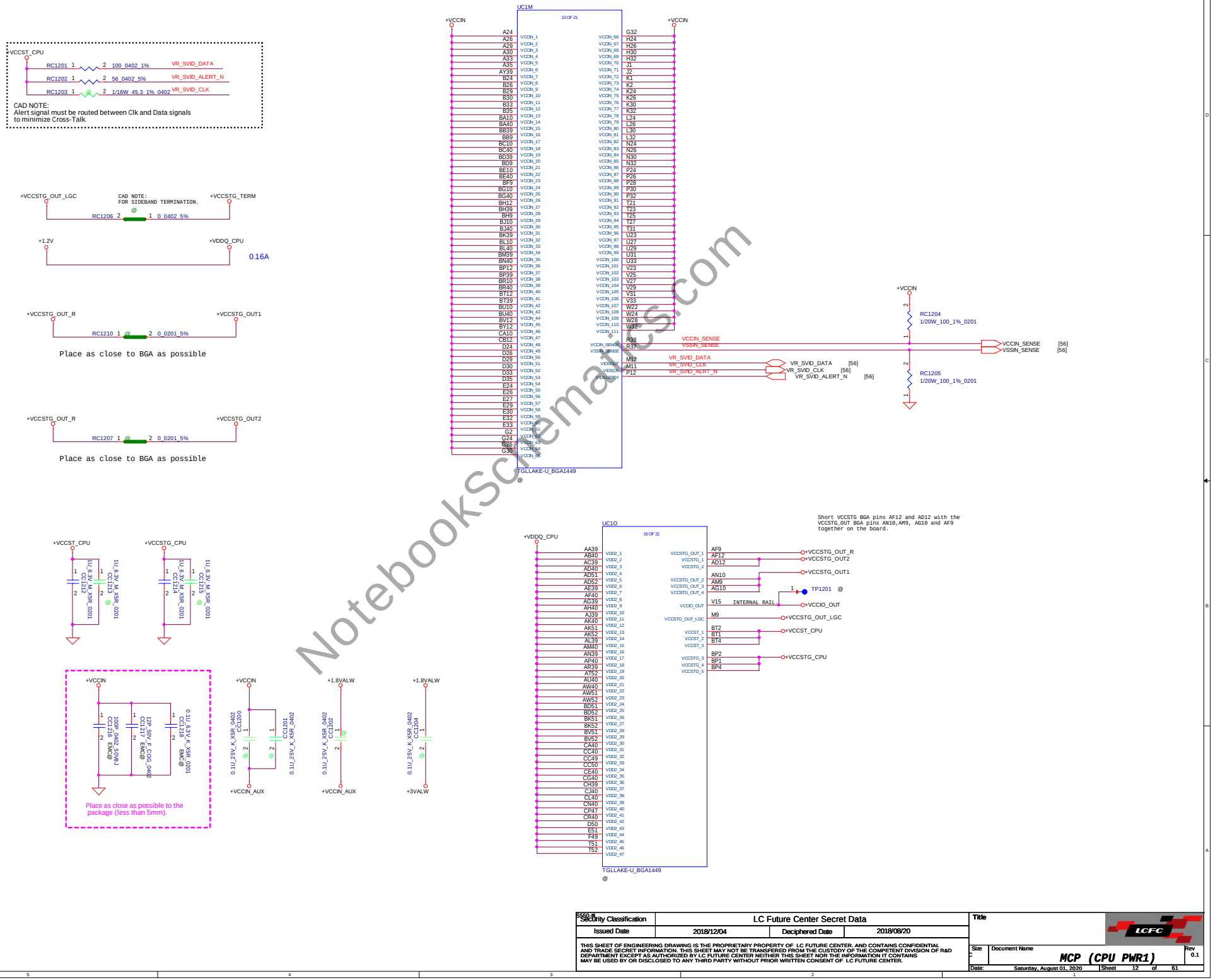






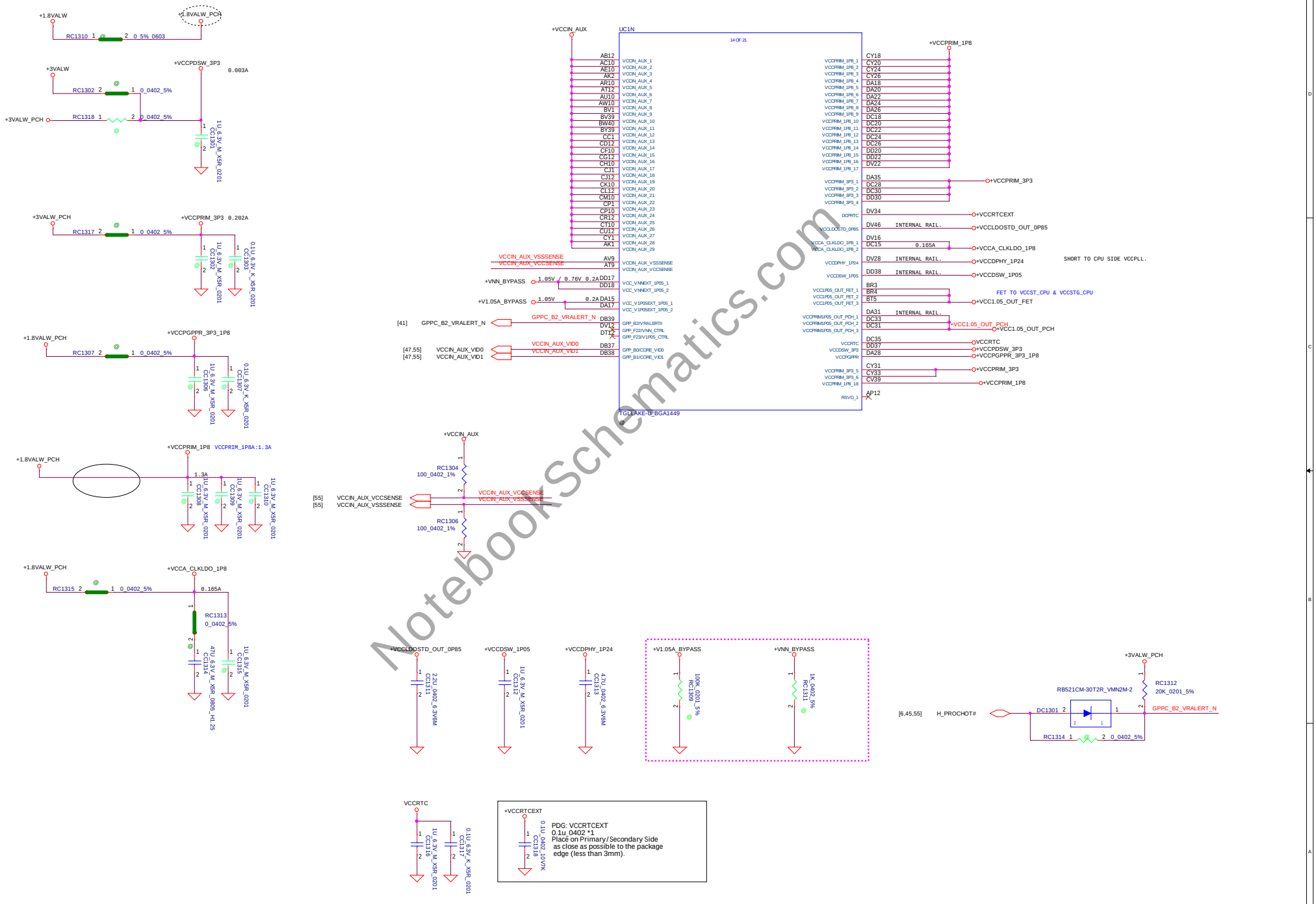
Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

Title	S550-IIL	
Size: C	Document Name: MCP (MANAGEMENT-CFG)	Rev: 0.1
Date: Saturday, August 01, 2020	Sheet 11 of 61	



Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

Title			
Size: C	Document Name: MCP (CPU PWR1)		Rev: 0.1
Date: Saturday, August 01, 2020	Sheet 12 of 61		

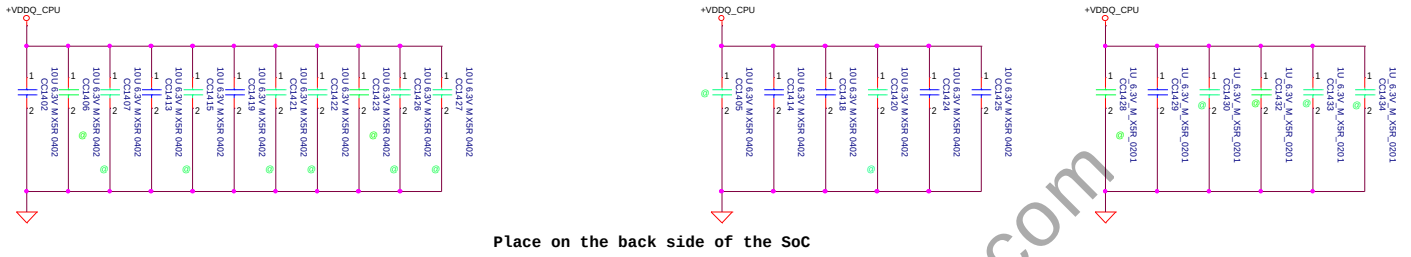


Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

Title	S550-IIL		
Size	Document Name		Rev
C	MCP (CPU PWR2)		0.1
Date:	Sunday, August 02, 2020	Sheet	13 of 61

VDDQ_CPU :

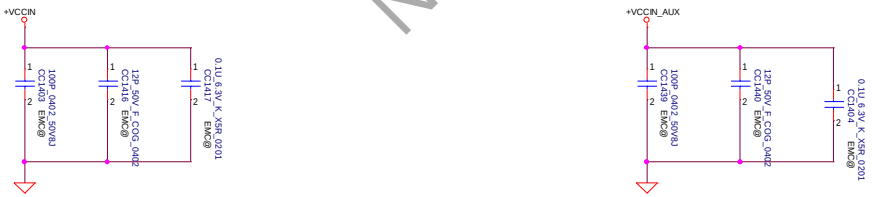
PDG:1 , 2x47uF 0603, 8x10uF 0402, 8x1uF 0402,
VS
C750 ITL: 6x10uF 0402, 3x1uF 0402,10x1uF 0201,Reserve 8x10uF 0402,7x1uF 0201
S550 ITL 6x10uF 0402, 9x1uF 0201 Reserve 11x10uF 0402, 7x1uF 0201



Place on the back side of the SoC

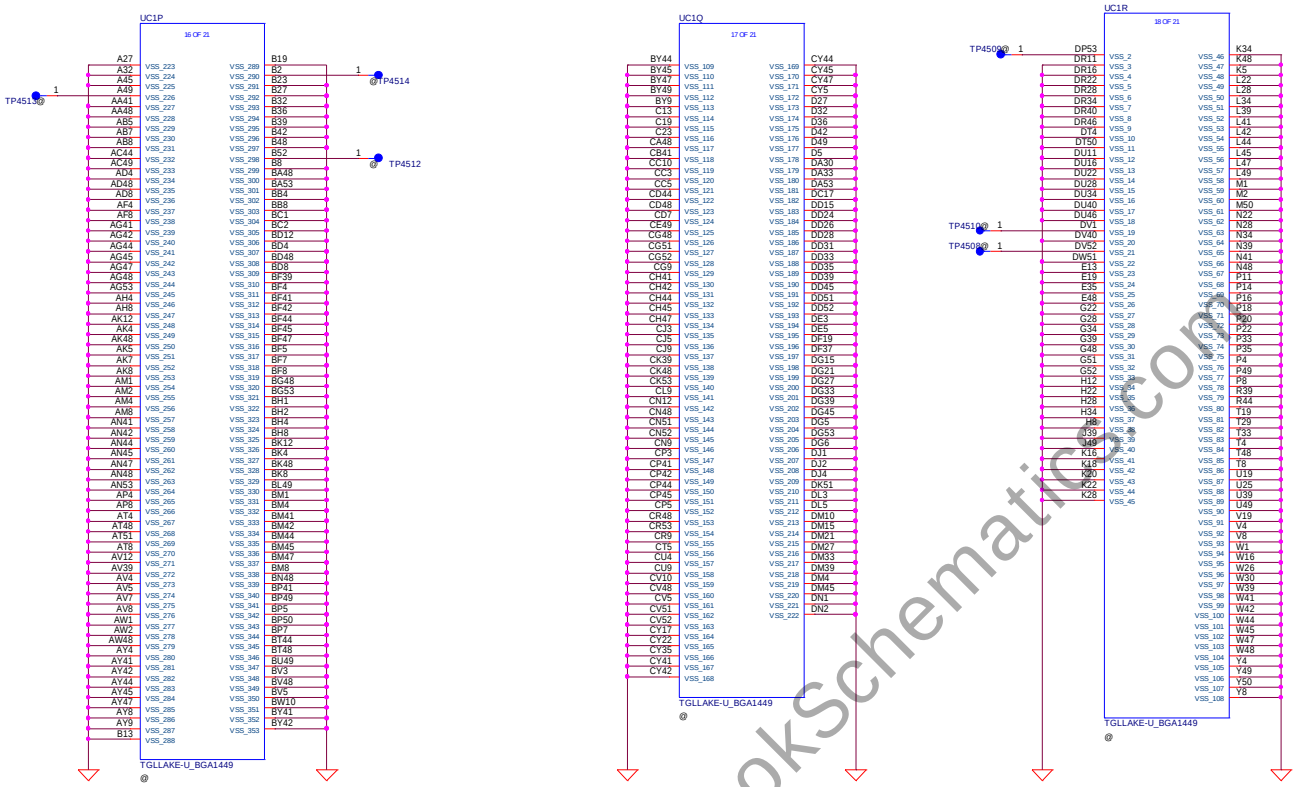
Place on the same side of the SoC

EMC CAPS refer CRB



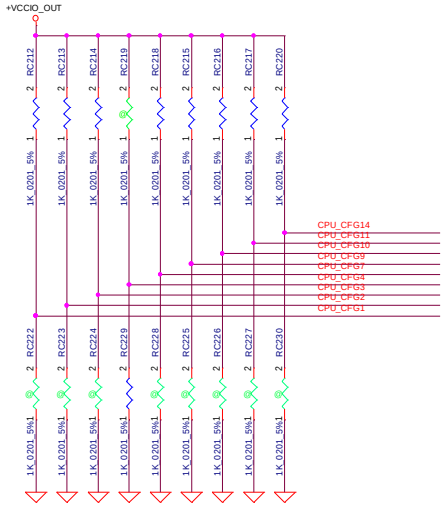
Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

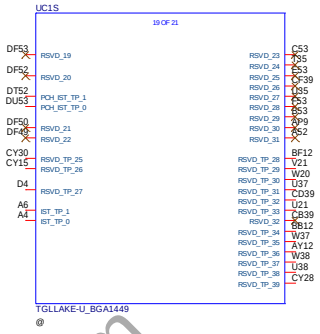
Title	S550-IIL		
Size	Document Name		Rev
C	MCP (PCH PWR)		0.1
Date:	Monday, June 01, 2020	Sheet	14 of 61

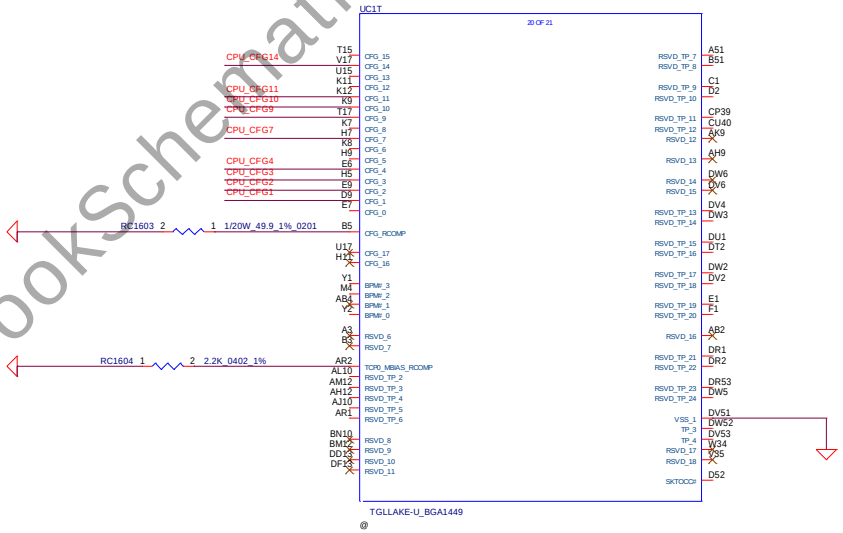


Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

Title	S550-IIL		
Size	Document Name		Rev
C	MCP (VSS)		0.1
Date:	Thursday, May 28, 2020	Sheet	15 of 61







****
Change CFG Follow PDG_V1.0---Xukun1220
****

Pin Name	Strap Description	Configuration	Default Value
CFG[0]	RSVD	None	
CFG[3:1]	RSVD	Pull-up to VCCIO	1Kohm
CFG[4]	eDP enable strap 1 = Disabled 0 = Enabled	Pull-up to VCCIO / Pull-down Platform design dependent	1Kohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training 1 = (default) PEG Trainimmediately following RESET# de-assertion. 0 = PEG Wait for BIOS for training.	Pull-up to VCCIO / Pull-down Platform design dependent	1Kohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1Kohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal 1 = Normal(Default) 0 = Reversed	Pull-up to VCCIO / Pull-down Platform design dependent	1Kohm
CFG[17:15]	RSVD	None	

CPU PCIe Gen4 Bifurcation and Lane Reversal Mapping

Bifurcation	CFG Signals	Lanes			
	CFG [14]	0	1	2	3
1x4	1	0	1	2	3
1x4(Reversed)	0	3	2	1	0

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Size	Document Name		Rev
C	Debug		0.1
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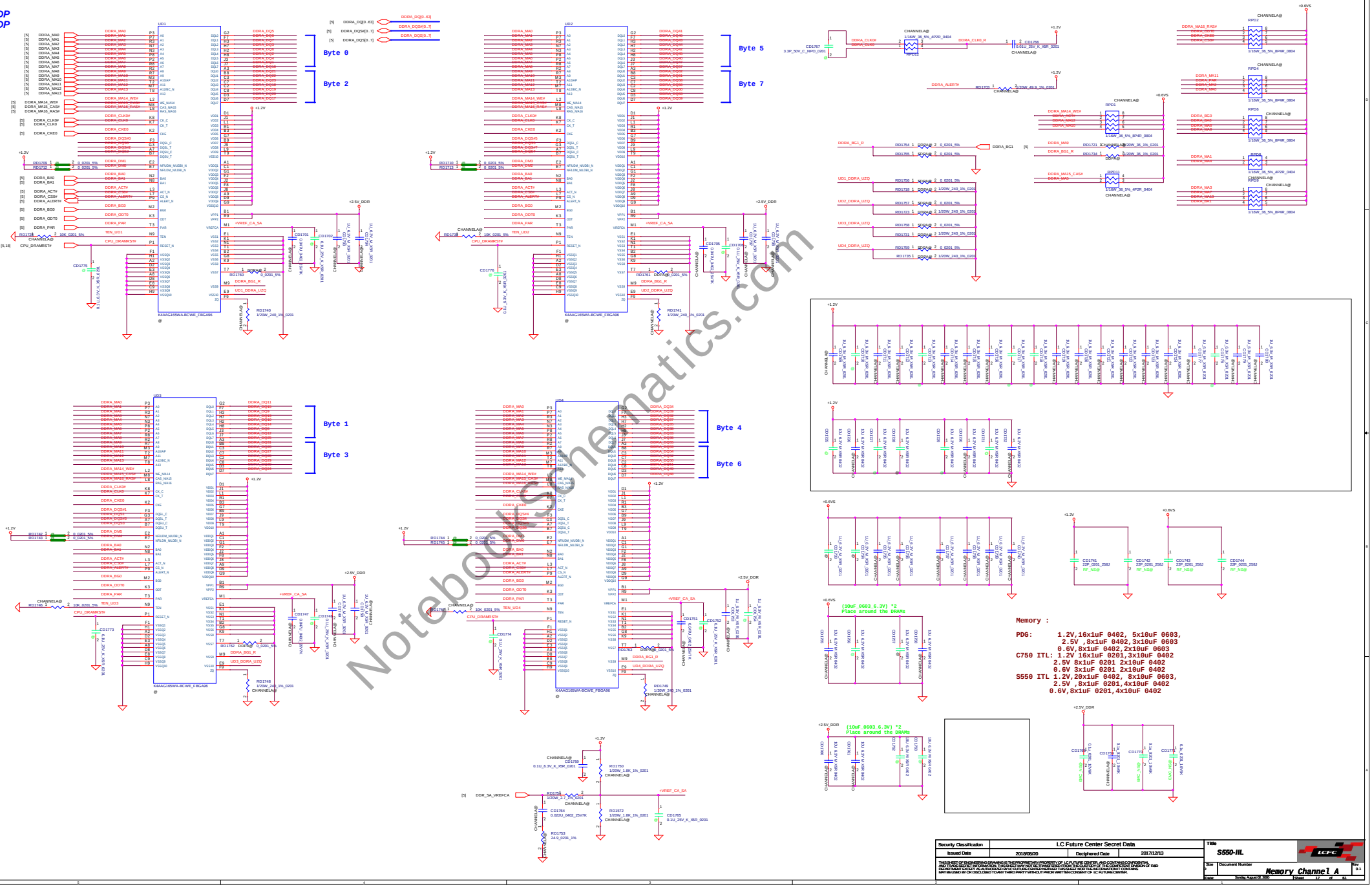
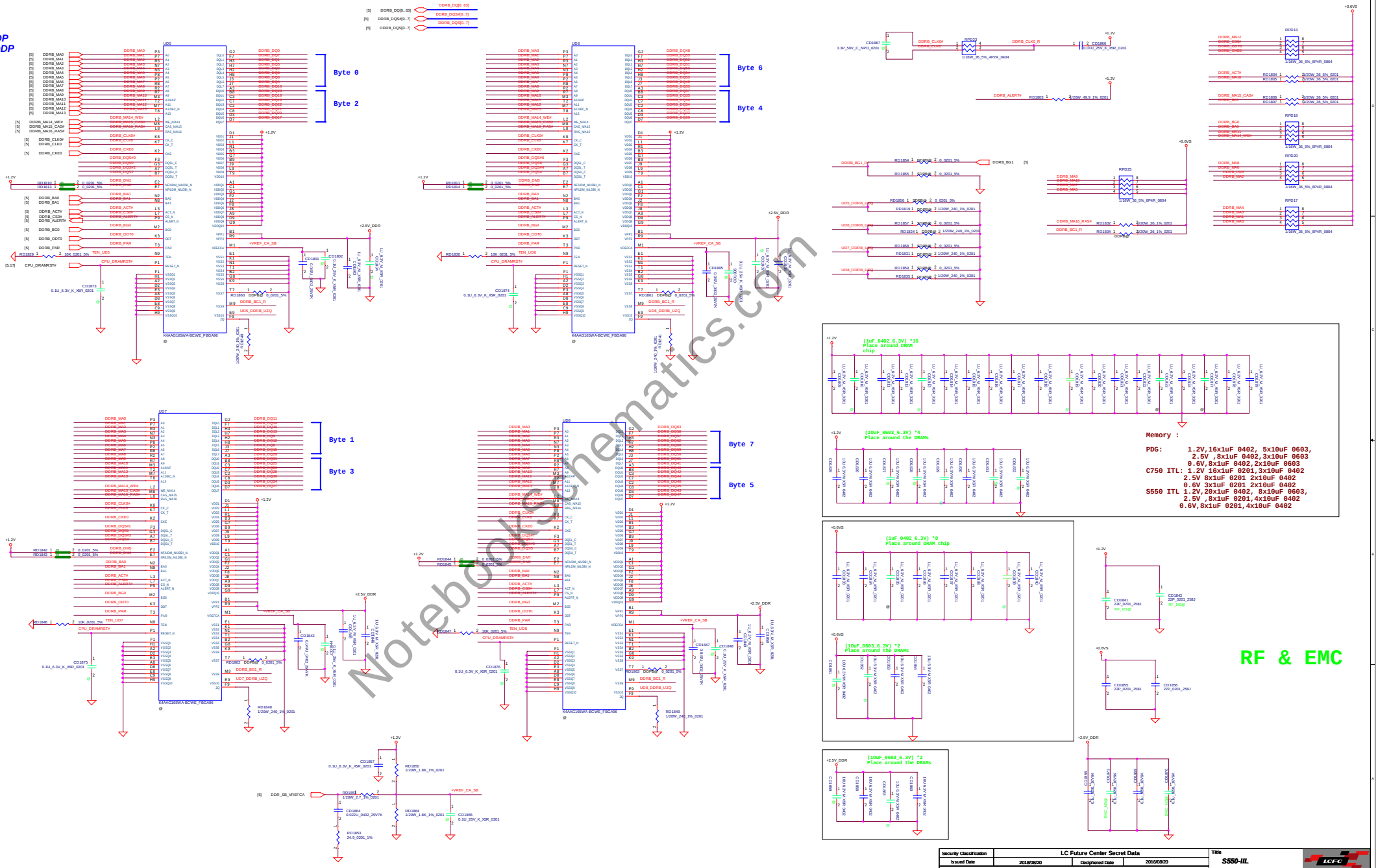
8Gb SDP
16Gb DDP



8Gb SDP
16Gb DDP



Security Classification	LC Future Center Secret Data		Title: S550-IIL
Issued Date: 2018/08/20	Deciphered Date: 2018/08/20		
Size: B	Document Number: Memory Channel B	Rev: 0.1	
Date: Tuesday, August 21, 2018	Sheet: 39 of 61		

GPIOs

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	GPU EVENT
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	1.8VGS_PWR_EN_R FOR 1.8VGS&1.0VGS&NVDD
GPIO5	OUT	N/A	
GPIO6	OUT	-	PSI_VGA
GPIO7	OUT	N/A	
GPIO8	OUT	-	VRAM_VDDQ_ADJ control the power voltage
GPIO9	I/O	N/A	10K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR6
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	OUT	N/A	GPIO18_FP_FUSE
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

Product	TDP		Min Core Clk	EDP									
	GPU	Mem		NVVDD		GPU FBIO (1.35V)		FB Total (GPU+Mem) (1.35V)		1.0V Total (1.0V@N17s) (1.05V@N16s)		1.8V/3.3V Total	
												1.8V N17s	3.3V N16s
	(W)	(W)	(MHz)	Cont. (A)	Peak (A)	Cont. (A)	Peak (A)	Cont. (A)	Peak (A)	Cont. (A)	Peak (A)	Cont. (A)	Cont. (A)
N16S-GMR	16	1.6	849	19	34	2.0	2.9	4.2	6.8	0.8	2.1	---	0.06
N16S-GTR	18	1.7	965	26.5	53	2.0	2.9	4.2	6.8	0.8	2.1	---	0.06
N17S-LG(0x1D12)	10	1.6	936	15.4	48.3	2.5	2.8	5.0	5.8	0.1	0.2	0.2	---
N17S-LG(0x1D52)	10.5	1.7	936	15.6	48.6	2.7	3.0	5.3	6.2	0.1	0.2	0.2	---
N17S-G1	25	1.9	1468	30.0	60.1	3.0	3.4	5.6	6.9	0.1	0.2	0.3	---
N17S-G0	25	1.9	1518	27.8	42.0	3.2	3.9	5.8	7.4	0.2	0.3	0.5	---
N17S-G2	25	1.9	1518	28.6	60.3	3.2	3.9	5.8	7.4	0.2	0.3	0.5	---

Product	TDP			
N18S-G5/GDDR6	25W			

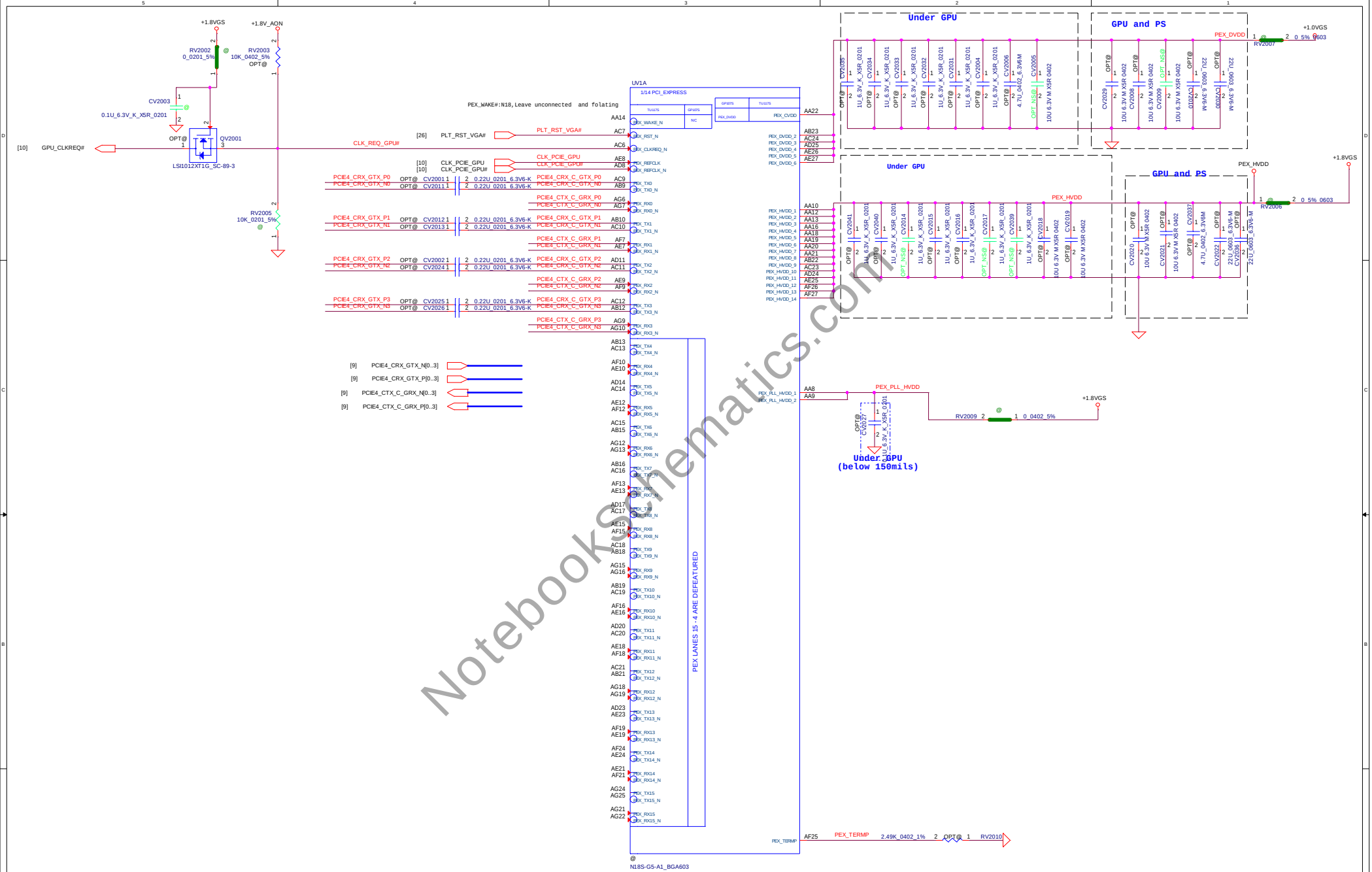
GDDR6 Mapping table

	DRAM1(0...31)		DRAM2(32...63)		
	CHA(Bytes 0,1)	CHB(Bytes 2,3)	CHA(Bytes 4,5)	CHB(Bytes 4,5)	Remark
CMD0	CA0_A				
CMD9	CA1_A				
CMD8	CA2_A				
CMD32	CA3_A				
CMD4		CA0_B			
CMD12		CA1_B			
CMD5		CA2_B			
CMD13		CA3_B			
CMD7	CA4_A	CA4_B			
CMD11	CA5_A	CA5_B			
CMD15	CA6_A	CA6_B			
CMD14	CA7_A	CA7_B			
CMD3	CA8_A	CA8_B			
CMD1	CA9_A	CA9_B			
CMD6	CABI_A	CABI_B			
CMD10	CKE_A	CKE_B			10K Pull 1.25VGS
CMD2	REST	REST			10K Pull GND
CMD20			CA0_A		
CMD28			CA1_A		
CMD21			CA2_A		
CMD29			CA3_A		
CMD16				CA0_B	
CMD25				CA1_B	
CMD24				CA2_B	
CMD33				CA3_B	
CMD23			CA4_A	CA4_B	
CMD27			CA5_A	CA5_B	
CMD30			CA6_A	CA6_B	
CMD31			CA7_A	CA7_B	
CMD19			CA8_A	CA8_B	
CMD17			CA9_A	CA9_B	
CMD22			CABI_A	CABI_B	
CMD26			CKE_A	CKE_B	10K Pull 1.25VGS
CMD18			REST	REST	10K Pull GND
CMD35					NC

POWER RAIL

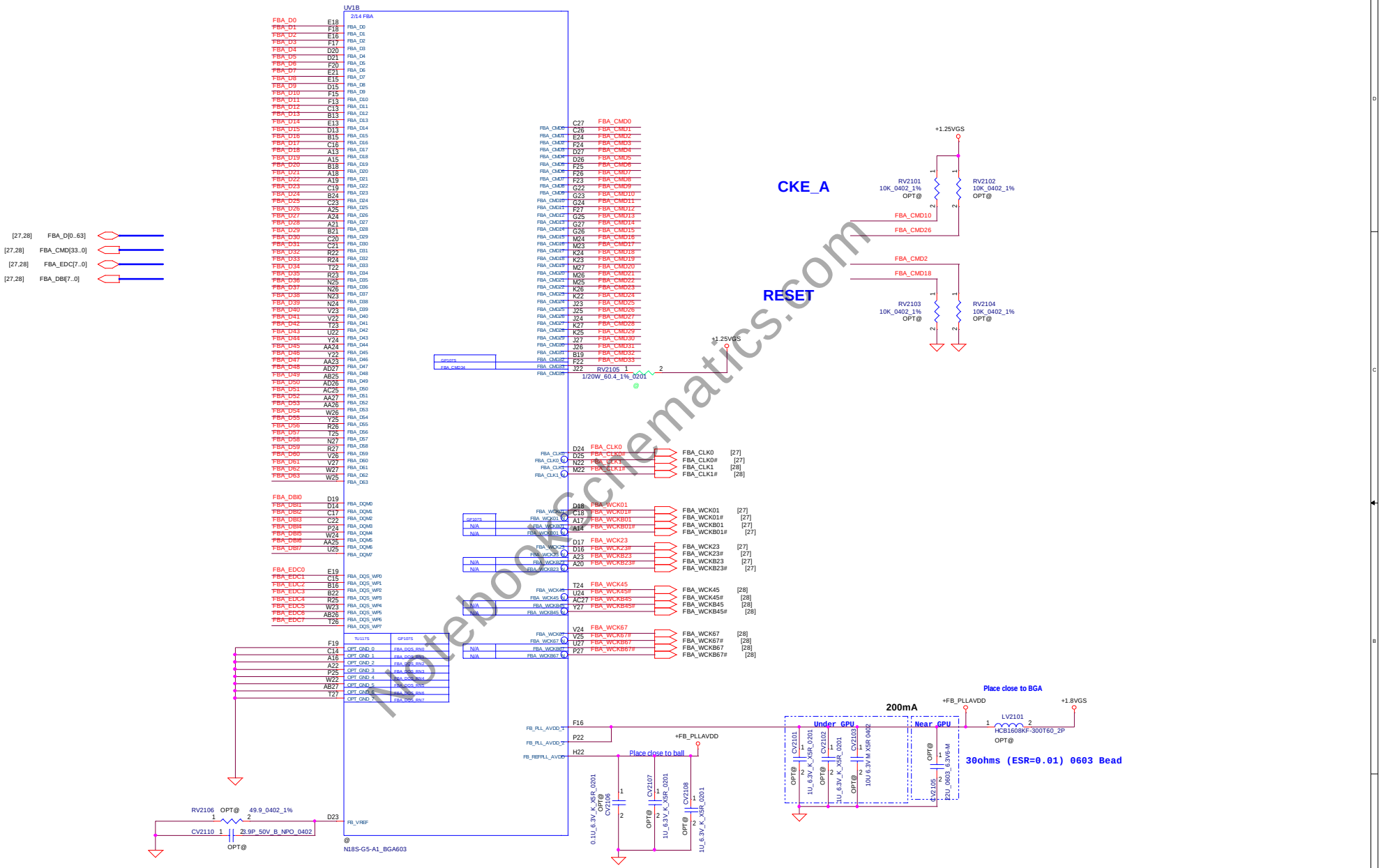
FB_PLL_AVDD	Frame Buffer PLL analog Power Rail	1.8V
GPCPLL_AVDD	Core PLL analog Power Rails	1.8V
SP_PLLVDD	Core Clock PLL Analog Power Rail	1.8V
VDD,VDDS	Primary Core Power Rail	NVVDD
VDD_SENSE GND_SENSE		
VDDS_SENSE GNDS_SENSE		
VDD18 or 1V8_MAIN 1V8_AON	1.8V Power Rail	1.8V
VID_PLLVDD	Thermal Controller and Video Pixel Clock PLL Analog Power Rail	1.8V
XS_PLLVDD	Core PLL analog Power Rails	1.8V

Title: S550-IIL
Size: C
Document Name: VGA Notes List
Rev: 0.1
Date: Thursday, May 28, 2020
Sheet 19 of 61



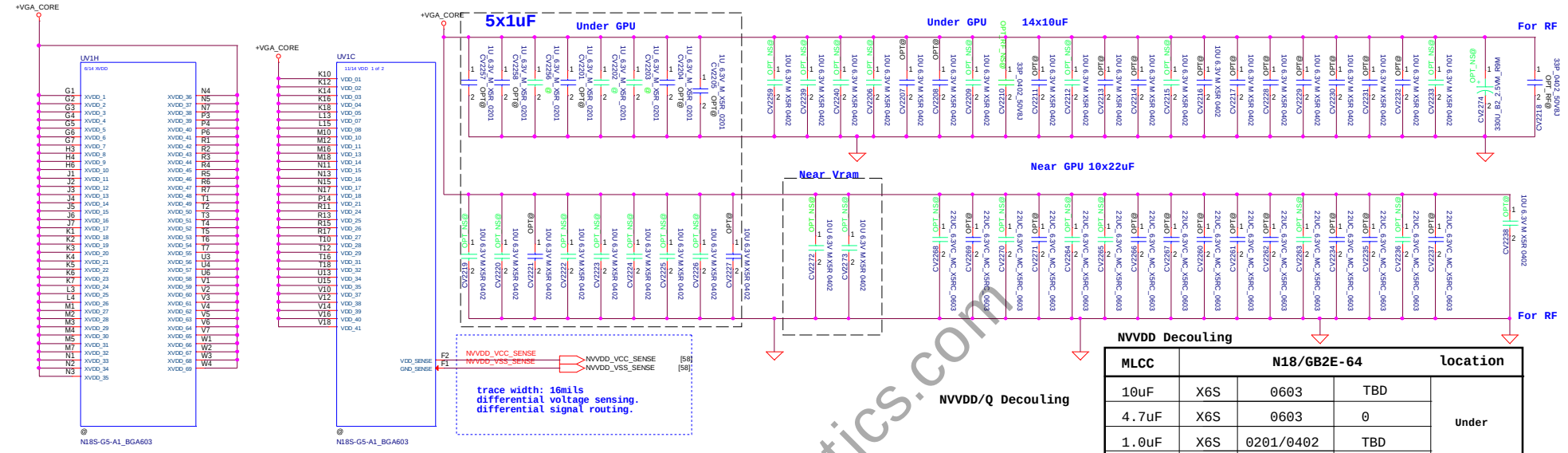
Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

Title	S550-IIL		
Size	Document Name		Rev
C	GPU_PCIE Interface		0.1
Date:	Monday, August 03, 2020	Sheet	20 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

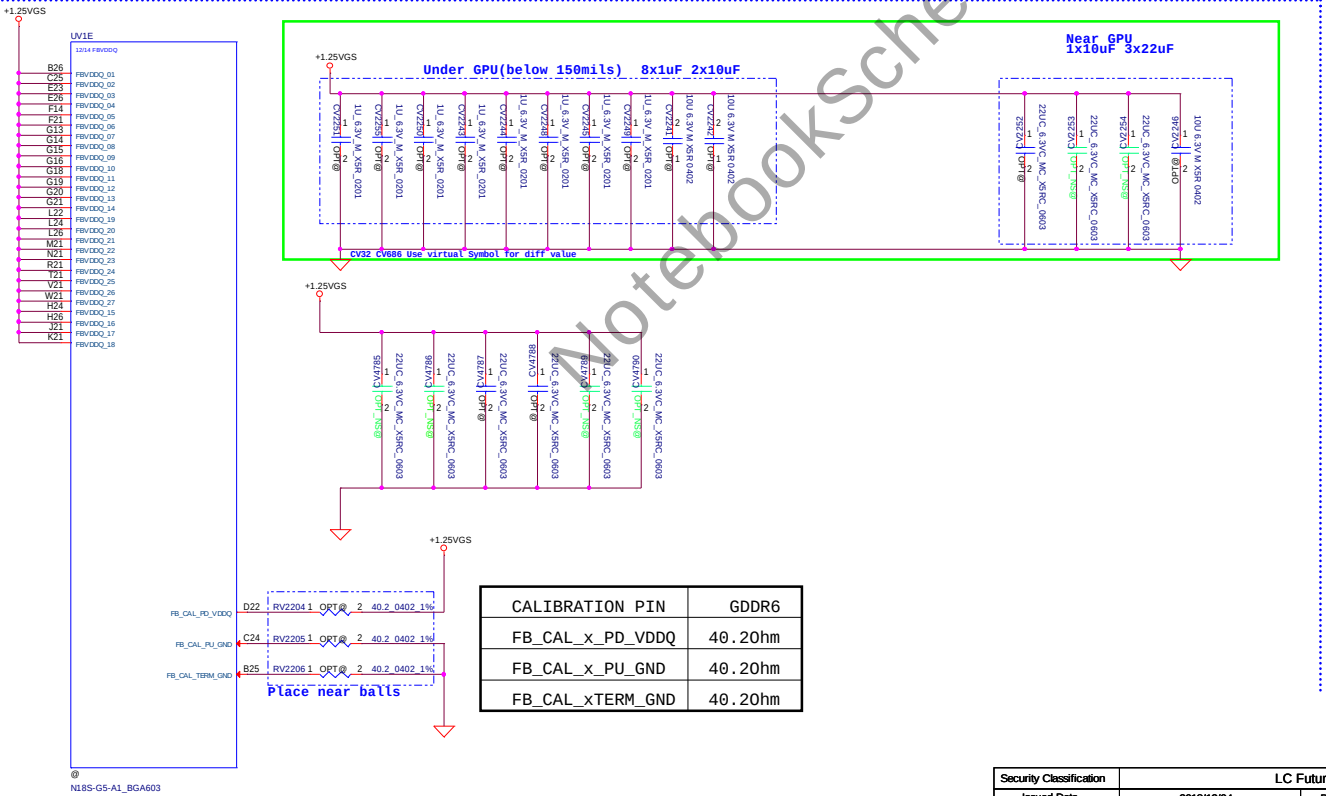
Title	S550-IIL		
Size	Document Name		Rev
C	GPU_MEM Interface		0.1
Date:	Thursday, May 28, 2020	Sheet	21 of 61



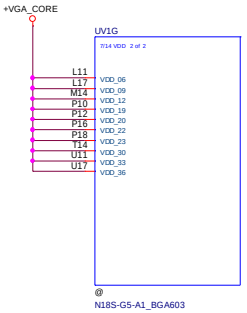
NVVDD Decoupling

MLCC	N18/GB2E-64			location
10uF	X6S	0603	TBD	Under
4.7uF	X6S	0603	0	
1.0uF	X6S	0201/0402	TBD	
0.47uF	X6S	0201/0402	0	
10uF	X6S	0603	0	Near
22uF	X6S	0805	TBD	
4.7uF	X6S	0603	0	
470uF	POS	7343	TBD	

NVVDD/Q Decoupling



CALIBRATION PIN	GDDR6
FB_CAL_x_PD_VDDQ	40.20hm
FB_CAL_x_PU_GND	40.20hm
FB_CAL_xTERM_GND	40.20hm

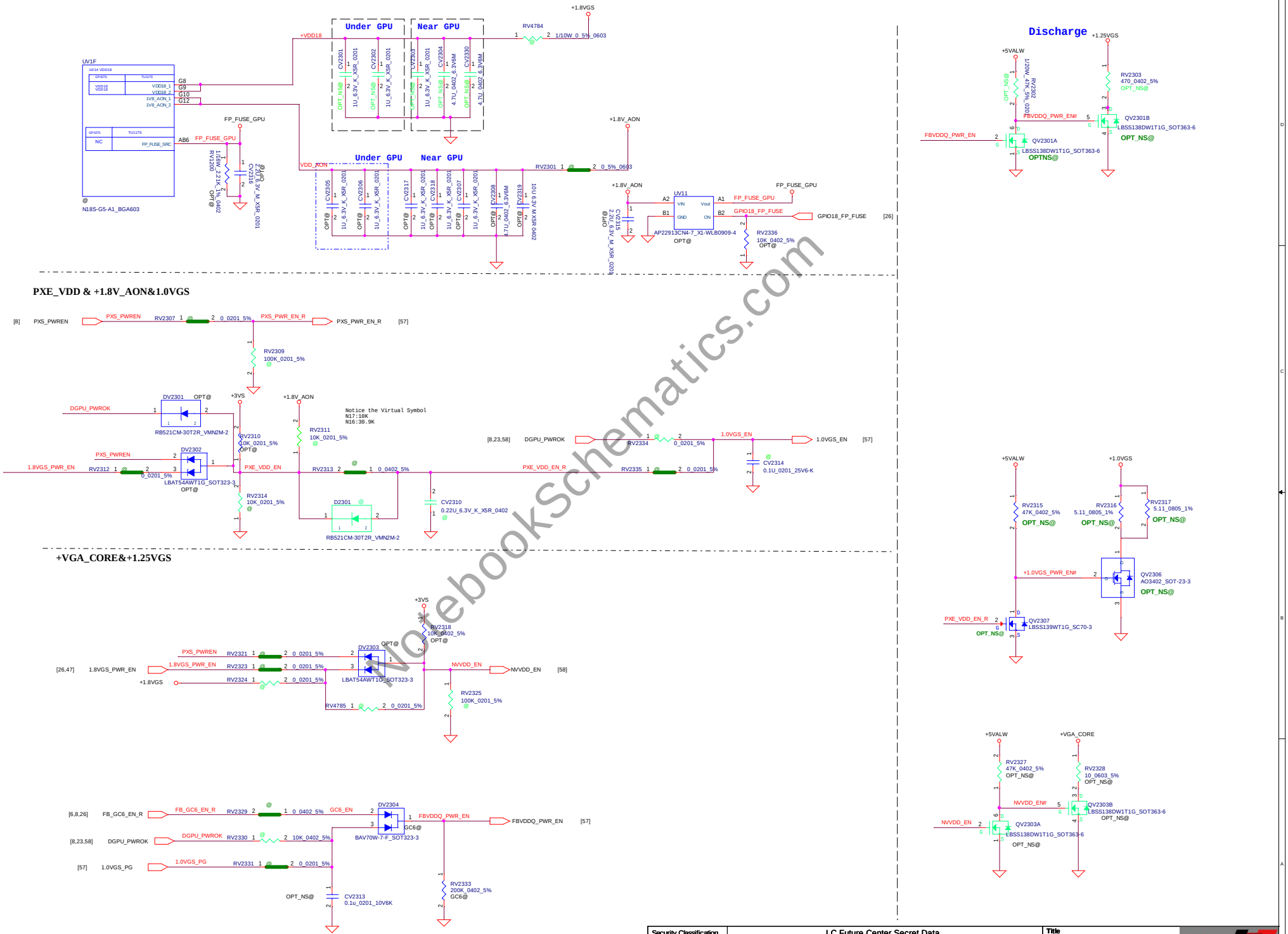


FBVDDQ Decoupling

MLCC	N18/GB2E-64			location
0.47uF	X6S	0201	24	Under
1.0uF	X6S	0201/0402	0	
10uF	X6S	0603	4	
10uF	X6S	0603	2	Near
22uF	X6S	0603	5	

Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

Title			
S550-IIL			
Size: C	Document Name: GPU_+VGA_CORE, FBVDDQ		Rev: 0.1
Date: Thursday, May 28, 2020	Sheet 22 of 61		

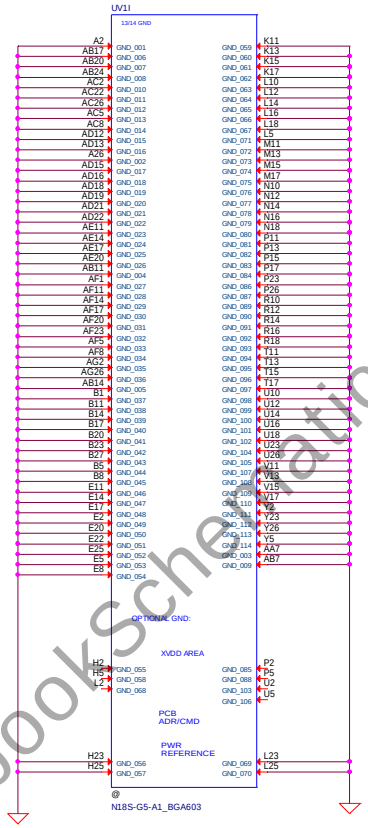


Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

Title: S550-IIL

Size: C | Document Name: GPU_AON/MAIN PWR/SEQUENCE | Rev: 0.1

Date: Monday, August 03, 2020 | Sheet 23 of 61

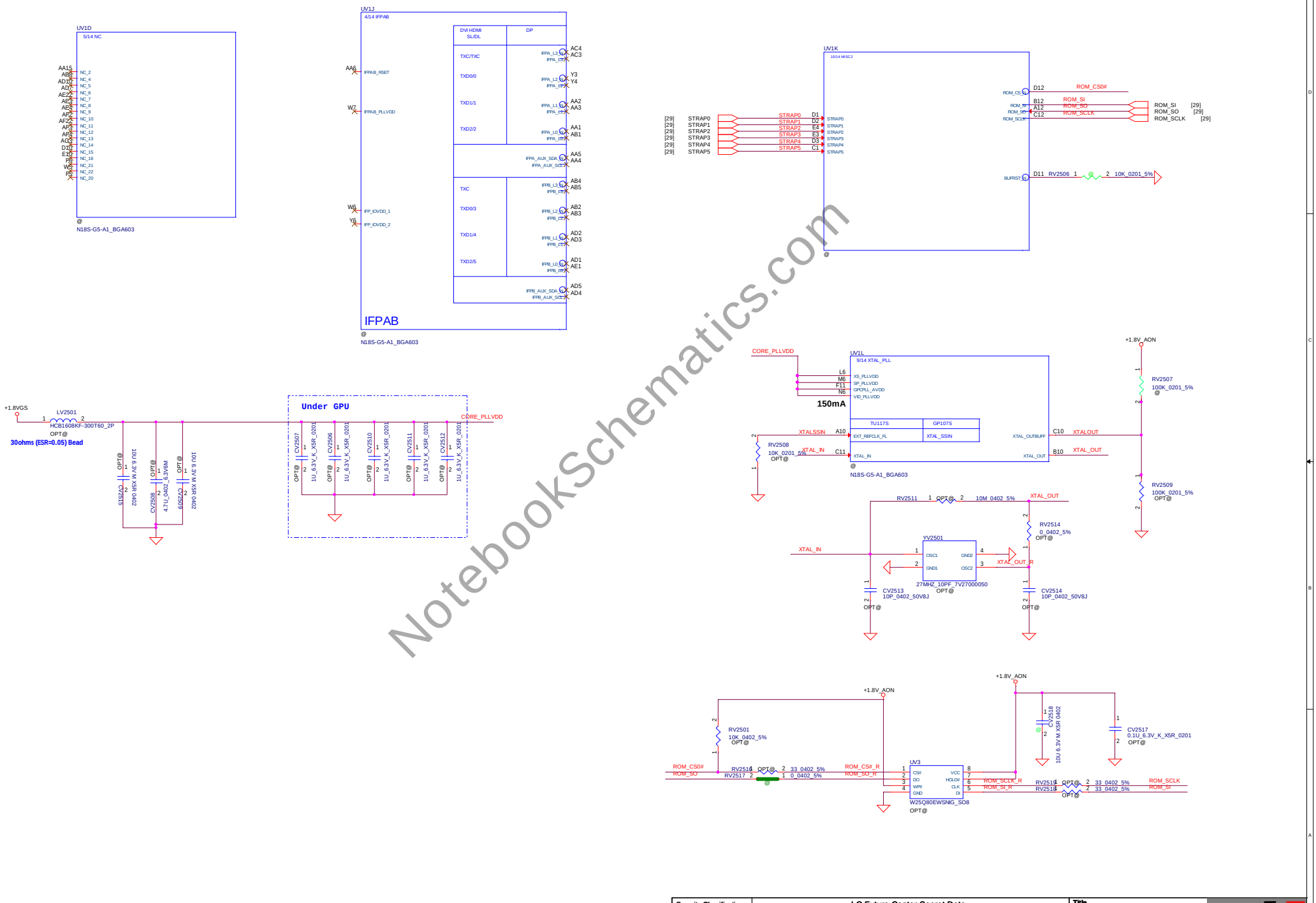


Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2018/09/20

Title: S550-IIL

Size	Document Name	Rev
C	GPU_GND	0.1

Date: Thursday, May 28, 2020 | Sheet 24 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

Title: S550-IIL

Size	Document Name	Rev
C	GPU_STRAP/DP/HDMI	0.1

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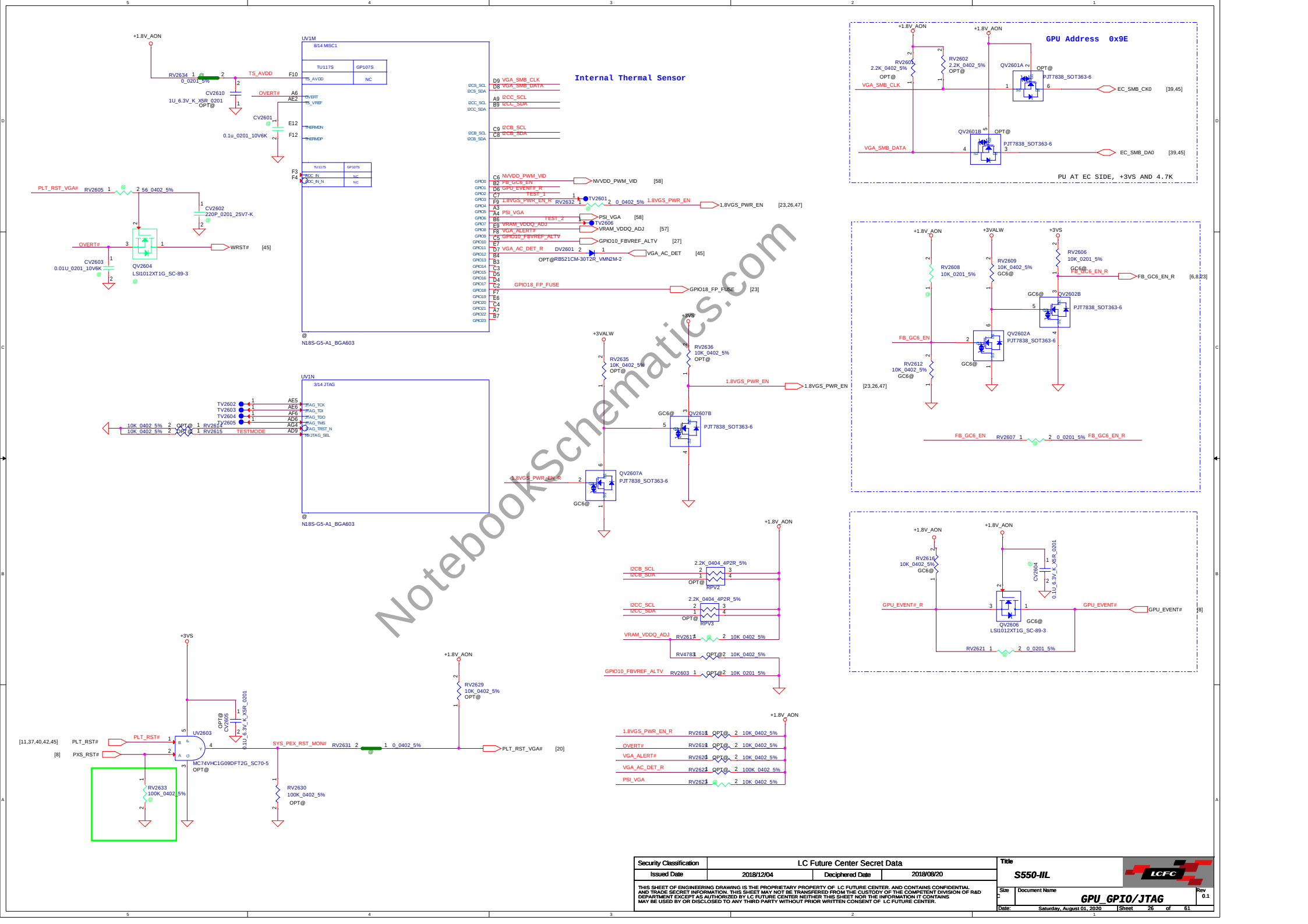

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Issued Date	2018/12/04	Deciphered Date	2019/08/20

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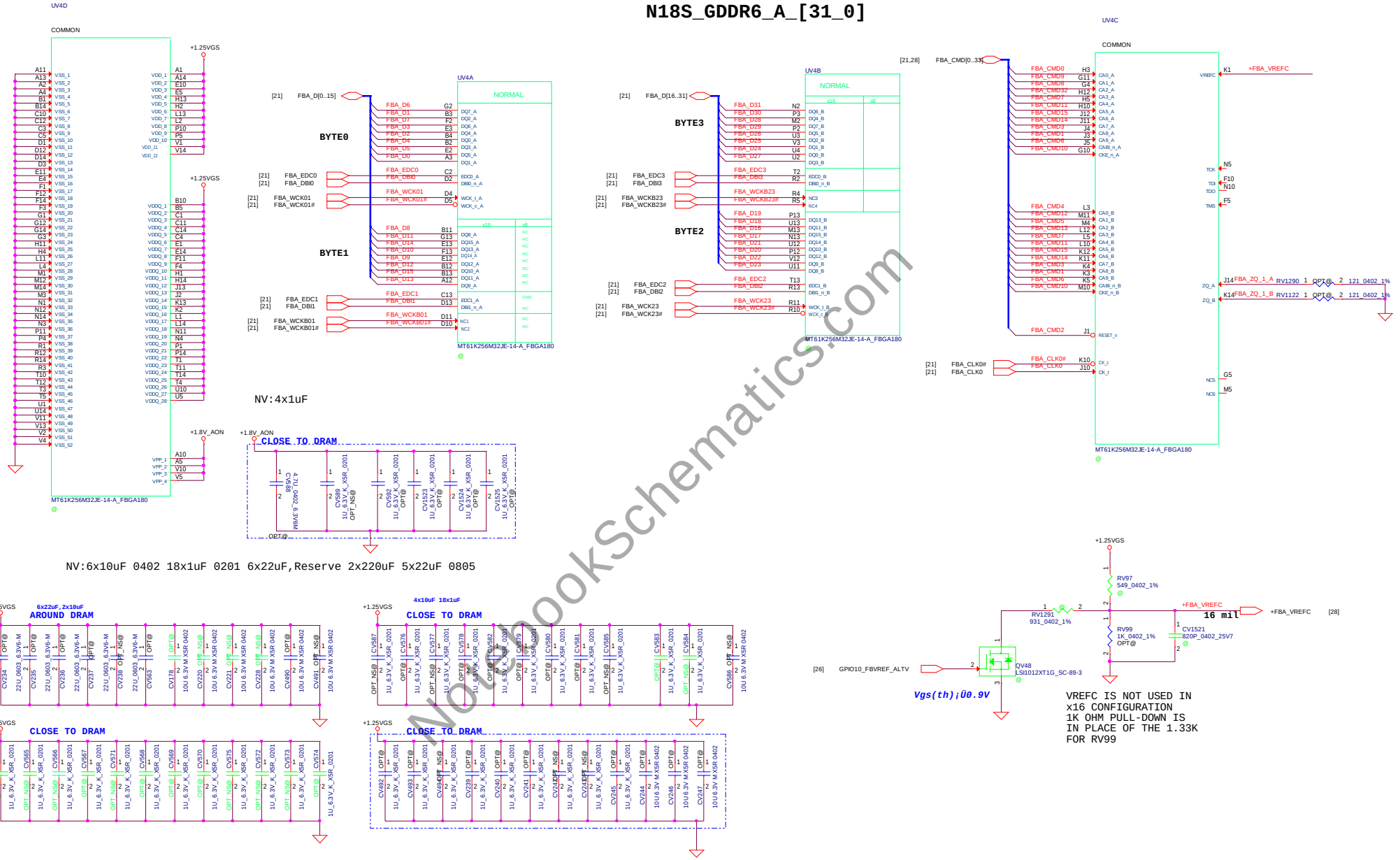
Title	S550-IIL		
Size	Document Name		Rev
C	GPU_GPIO/JTAG		0.1
Date:	Saturday, August 01, 2020	Sheet 26 of 61	

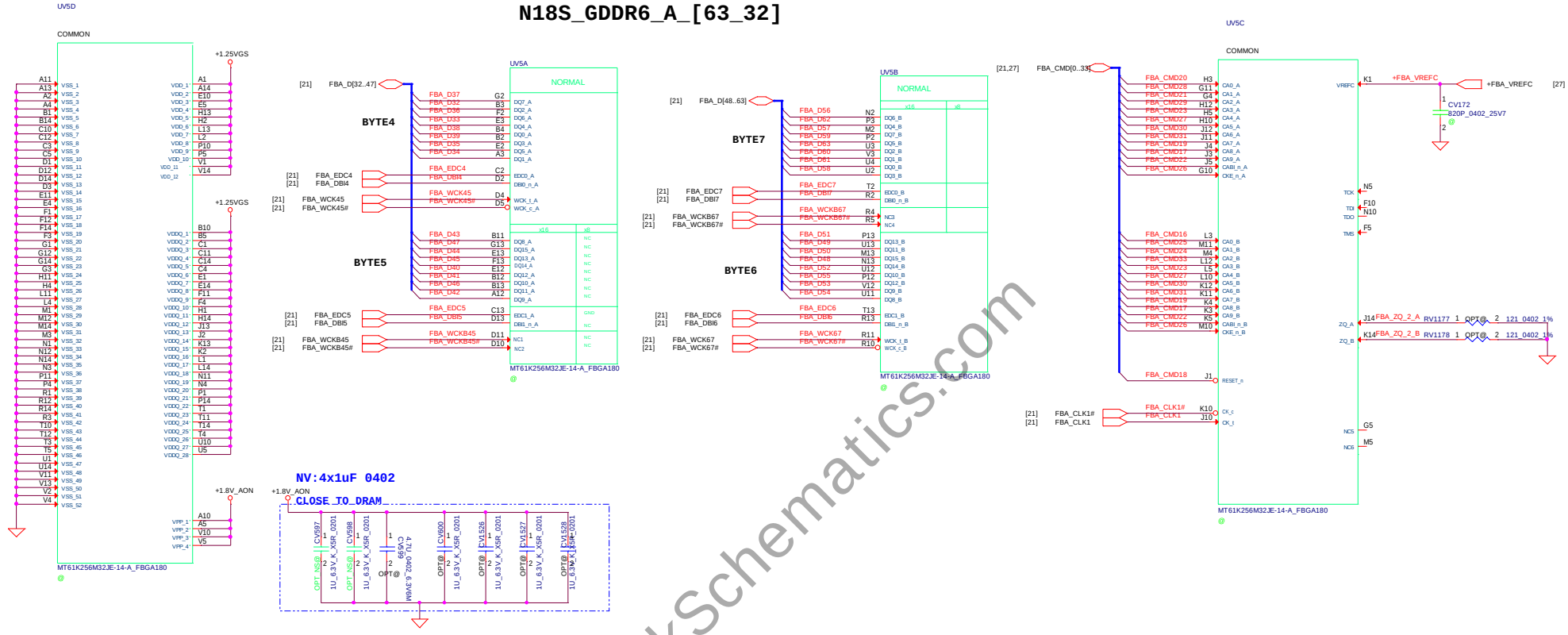
N18S_GDDR6_A_[31_0]



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2019/08/02

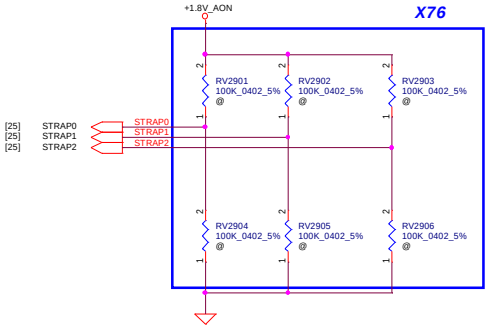
Title	N18S_GDDR6_A_[31_0]		
Size	Document Number		Rev
C	S550-ITL		2.0
Date:	Thursday, May 28, 2020	Sheet	27 of 73

N18S_GDDR6_A_[63_32]



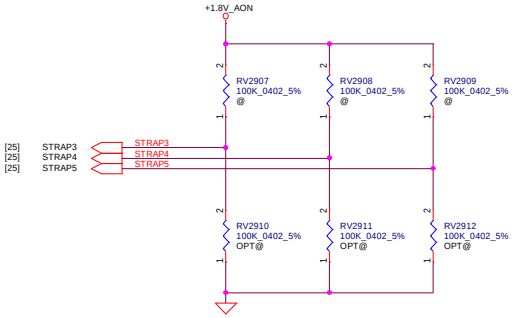
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2019/08/02

Title	N18S_GDDR6_A_[63_32]		
Size	Document Number		Rev
C	S550-ITL		2.0
Date:	Thursday, May 28, 2020	Sheet	28 of 73



VRAMCFG

GPU VRAM	FB Memory (GDDR6)		Starp	STRAP2	STRAP1	STRAP0
2GB	Samsung 8Gb	K4Z80325BC-HC14	0x0	L	L	L
	Micron 8Gb	MT61K256M32JE-14:A	0x1	L	L	H



STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

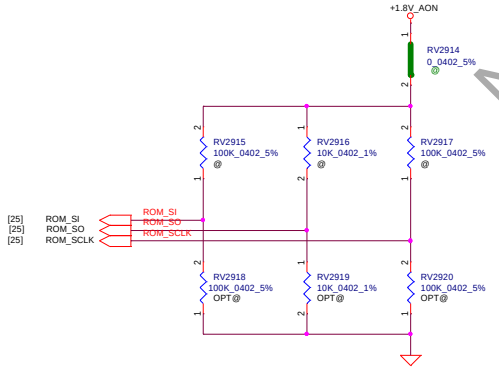
1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE

SMB_ALT_ADDR	
0	Single GPU configurations
1	Dual GPU configurations

DEVID_SEL	
0	Original PCIE DEVID
1	Alternate "re-band"DEVID

PCIE_CFG	
0	(Default)
1	

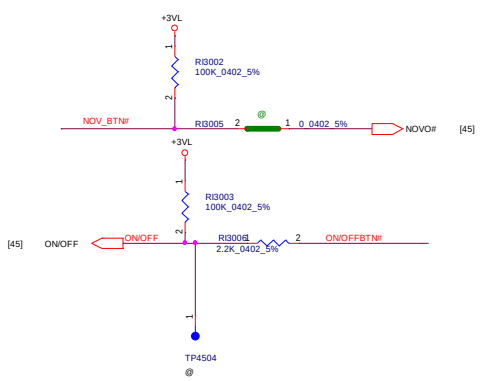
VGA_DEVICE	
0	3D Device (Class Code 302)
1	3D Device (Class Code 300)



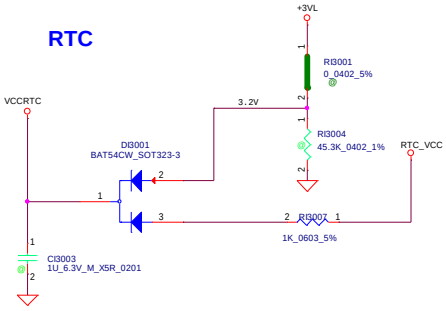
	ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT*Function
N18S-G5	L	L	L	FS_OVERT*function ENABLE

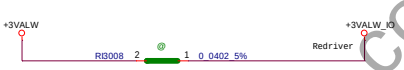
Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

Title	S550-IIL		
Size	Document Name		Rev
C	GPU_Strap		0.1
Date:	Saturday, August 01, 2020	Sheet 29 of 61	

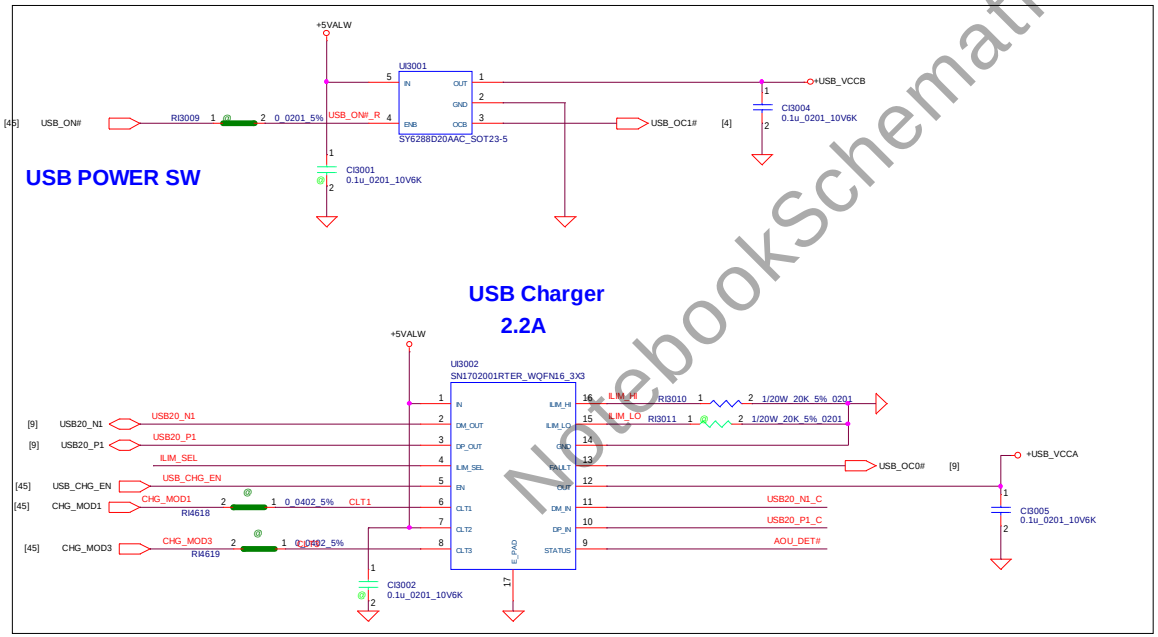


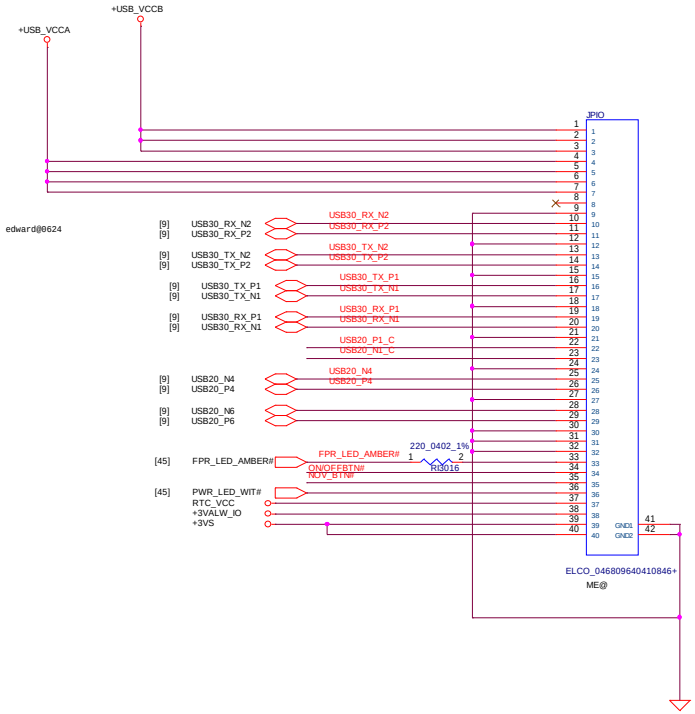
RTC



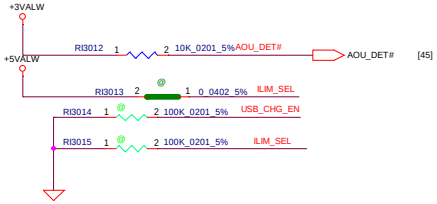


BUTTON



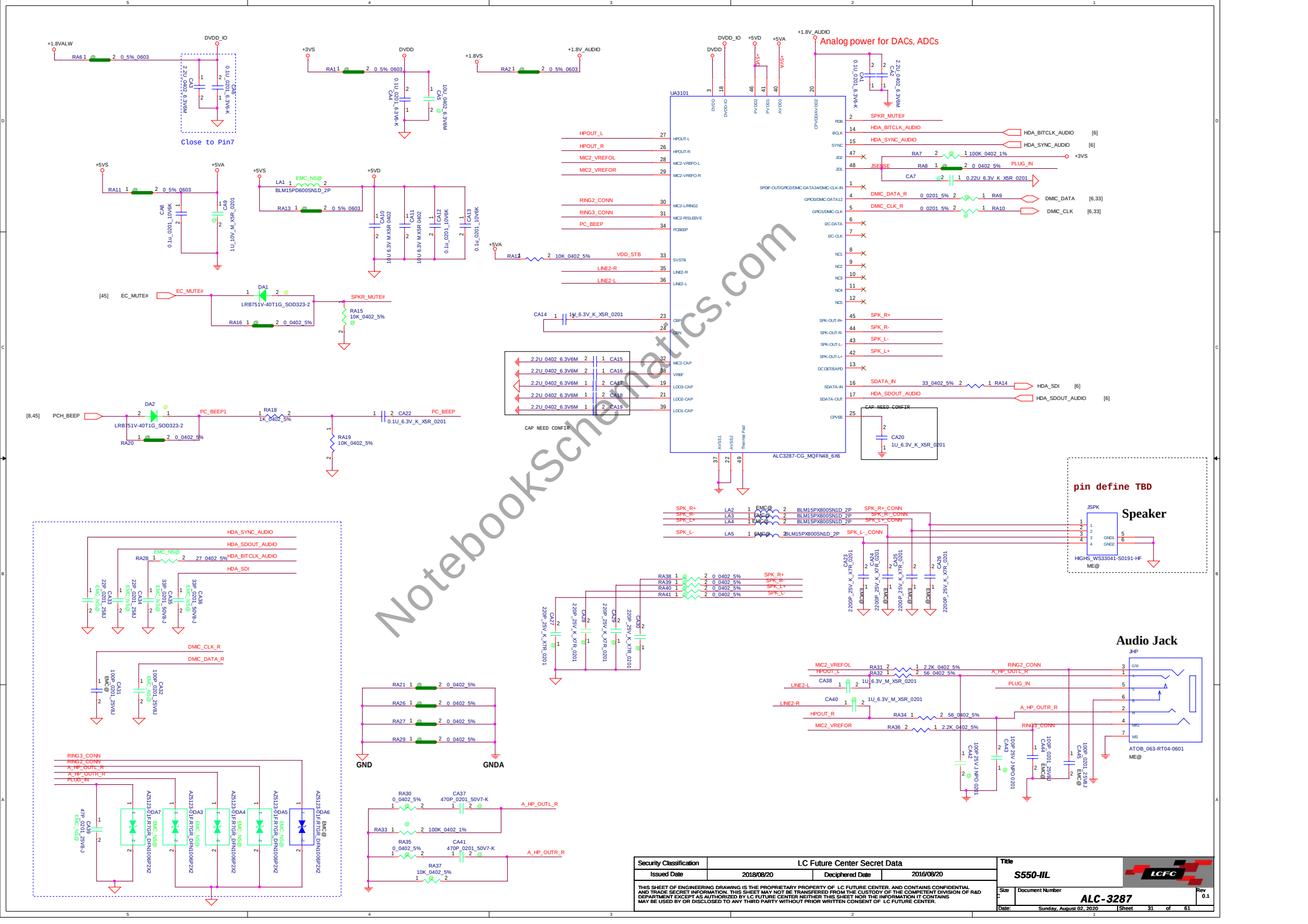


	CLT1	CLT2	CLT3	ILIM_SEL	MOD	
*	0	0	0	X	**DCH**	OUT held low
*	1	1	1	1	**CDP**	Data Connected and Load Detect Active
*	1	1	1	0	**SDP2**	Data Connected
*	1	1	0	X	**SDP1**	Data Connected
*	0	1	0	X	**SDP1**	Data Connected
*	1	0	0	X	**DCP_Short**	Device Forced to stay in DCP BC 1.2 charging mode
*	1	0	1	X	**DCP_Divider**	Device Forced to stay in DCP Divider 1 Charging Mode
*	0	1	1	X	**DCP_Auto**	Data Disconnected and Load Detect Active
*	0	0	1	X	**DCP_Auto**	Data Disconnected and Load Detect Active



Security Classification	LC Future Center Secret Data		
Issued Date	2018/03/15	Deciphered Date	2019/03/14

Title	S550-IIL		
Size	Document Number		Rev
C	IO CONN		0.1
Date:	Saturday, August 01, 2020	Sheet	30 of 61



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Issued Date	2018/08/20	Deciphered Date	2019/08/20

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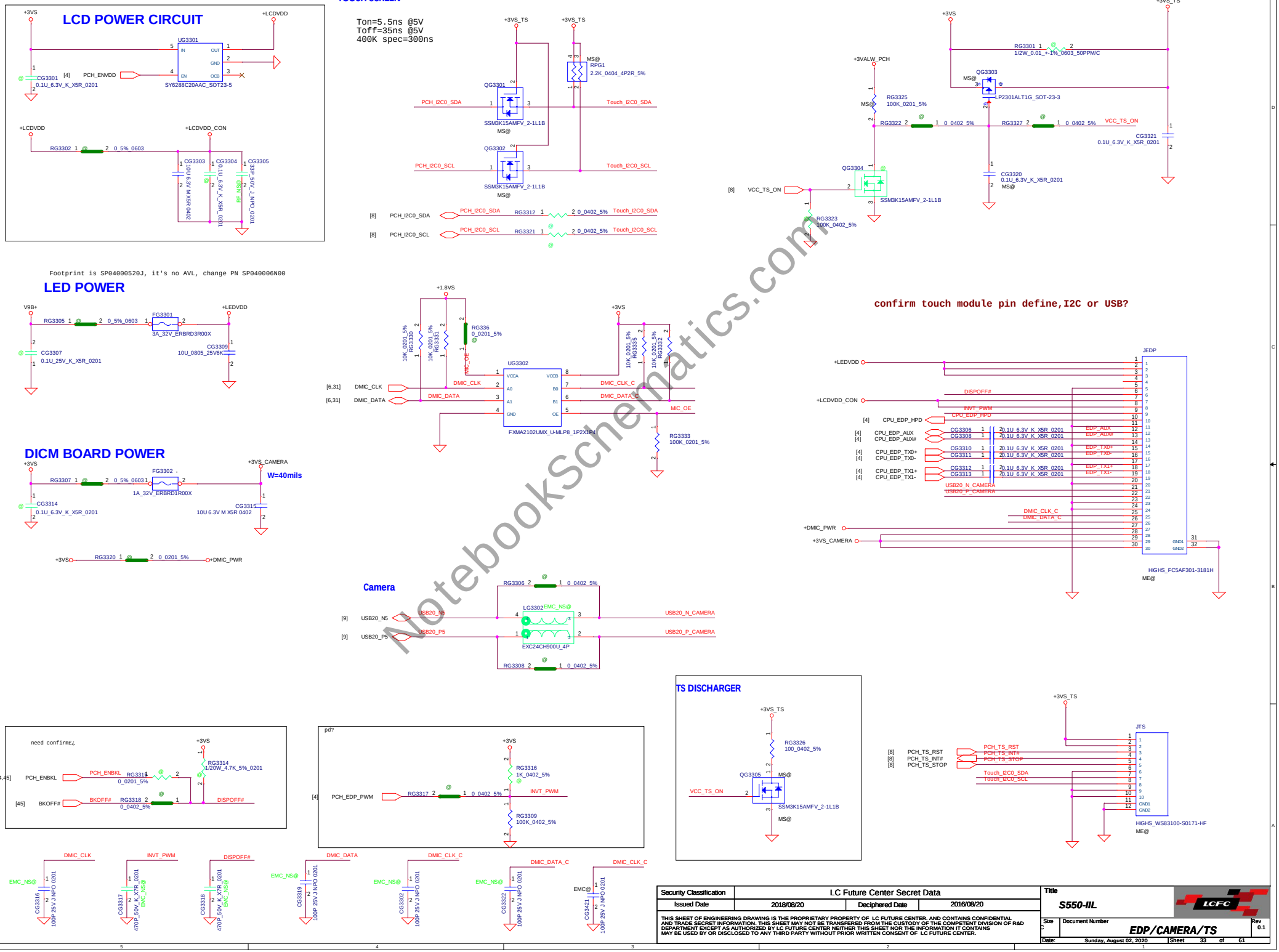
Title	S550-IIL
Size	C
Document Number	ALC-3287
Rev	0.1
Date:	Sunday, August 02, 2020
Sheet	31 of 61

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2019/08/20

Title: *S550-IIL*

Size	Document Number	Rev
C		0.1

Date: Thursday, May 28, 2020 | Sheet 32 of 61

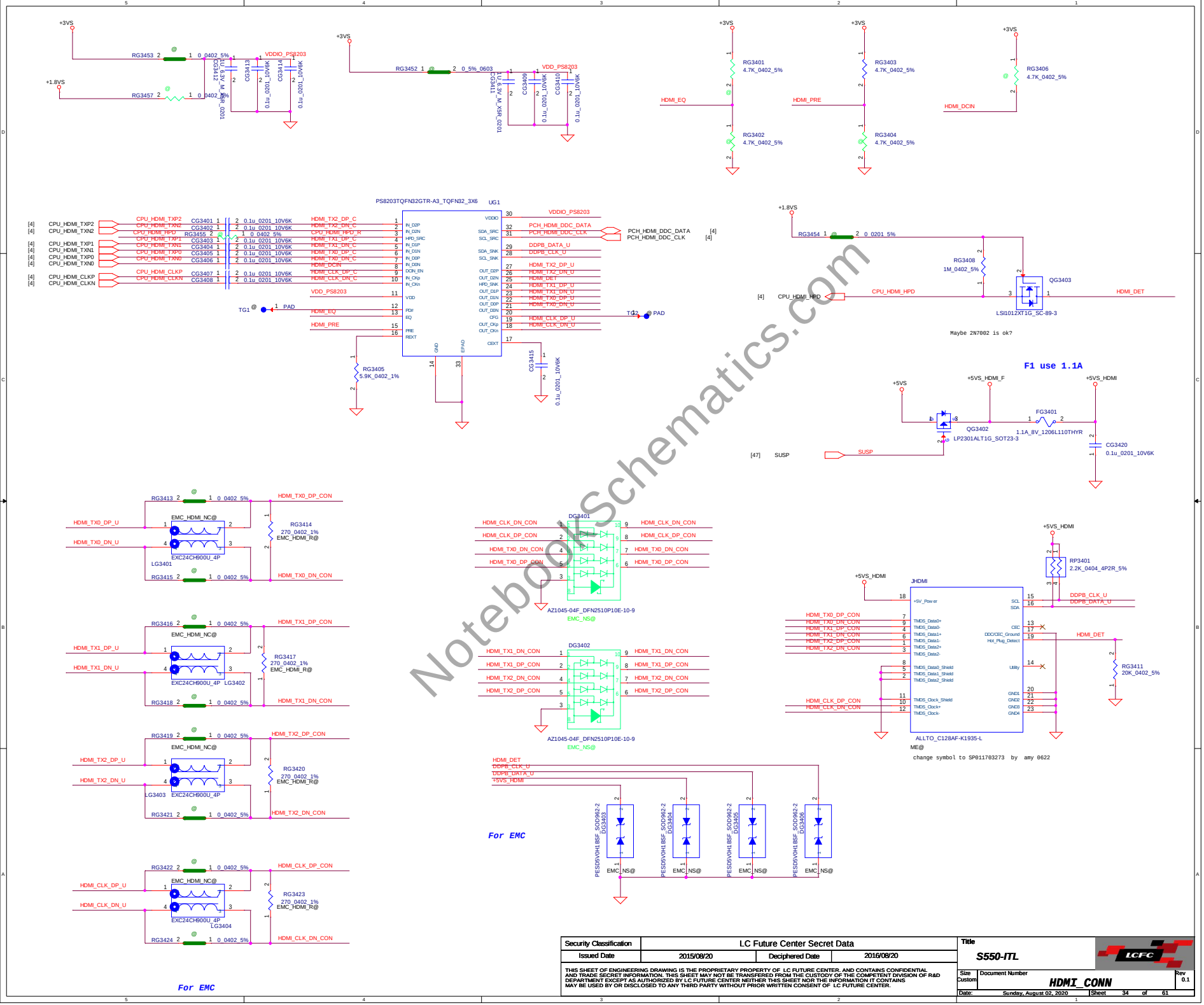


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2019/08/20

Title: S550-IIL

Size: C | Document Number: EDP/CAMERA/TS | Rev: 0.1

Date: Sunday, August 02, 2020 | Sheet 33 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/20	Deciphered Date	2016/09/20

Title	S550-ITL		
Size: Custom	Document Number: HDMI_CONN		Rev: 0.1
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20190813

Page 45: UE4501,change 128K

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: S550-IIL

Size	Document Number	Rev
C		0.1

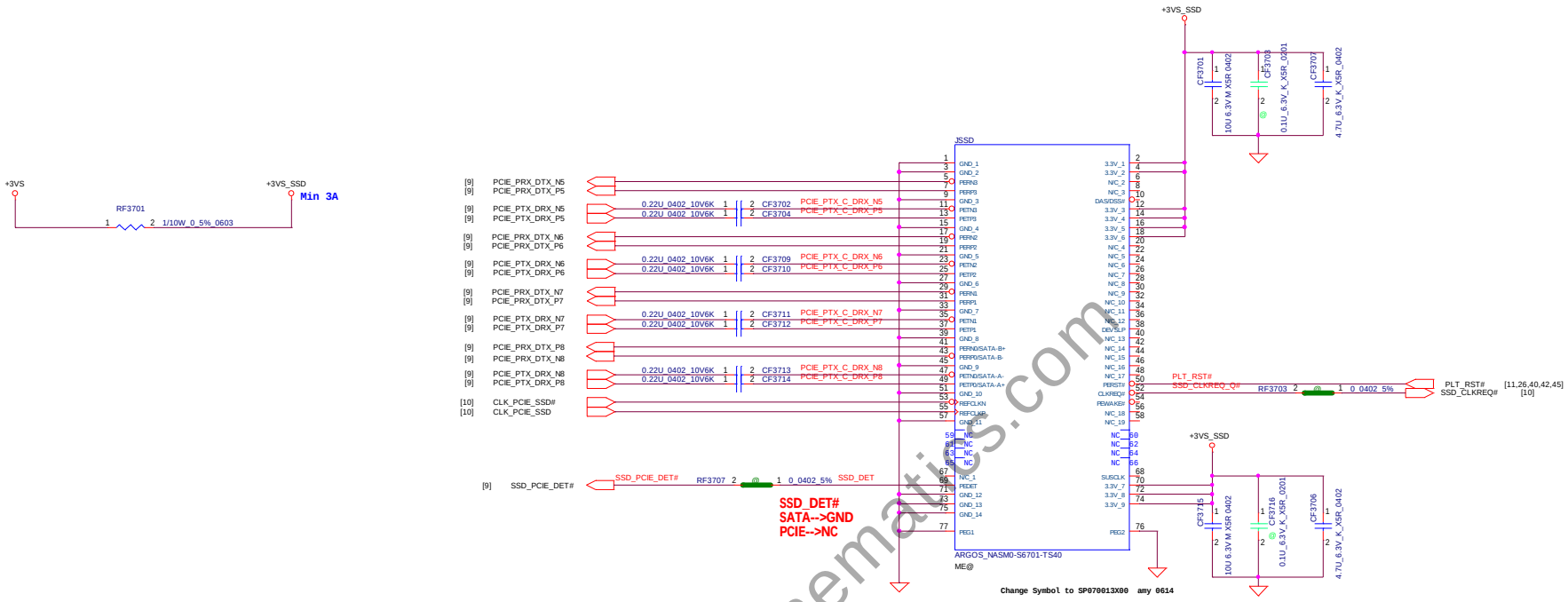
Date: Thursday, May 28, 2020 | Sheet 35 of 61

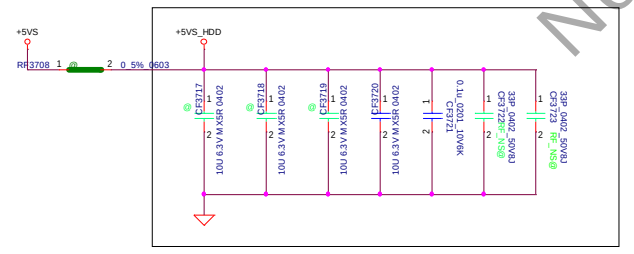
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2019/08/20

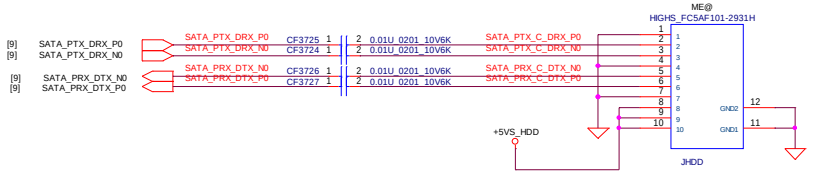
Title

LCFC

Size C	Document Number	Rev 0.1
Date: Thursday, May 28, 2020	Sheet 36 of 61	



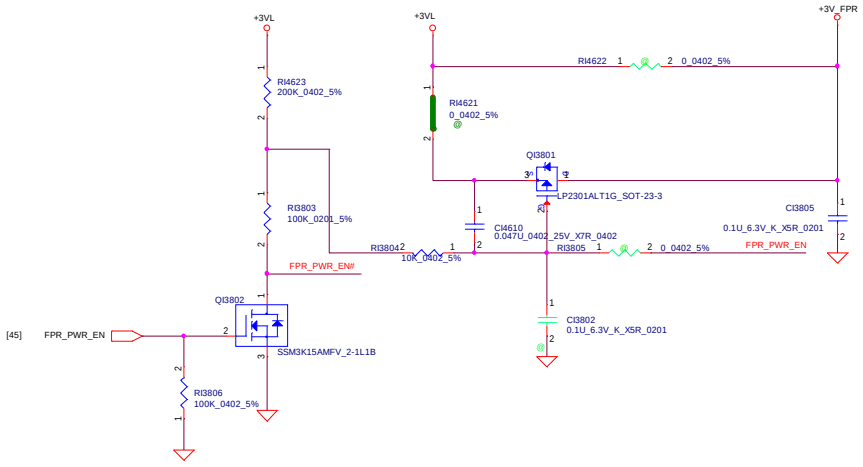




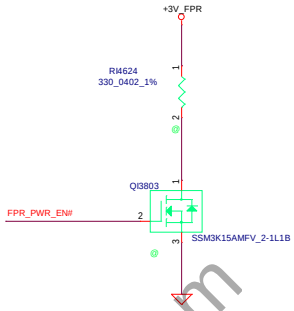
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

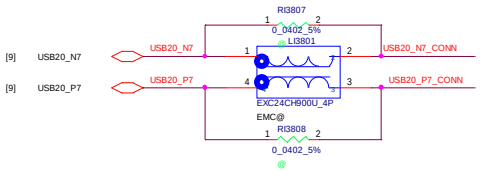
Title	S550-IIL		
Size	Document Number		Rev
C	NGFF_SSD/HDD		0.1
Date:	Tuesday, August 11, 2020	Sheet	37 of 61

FPR POWER

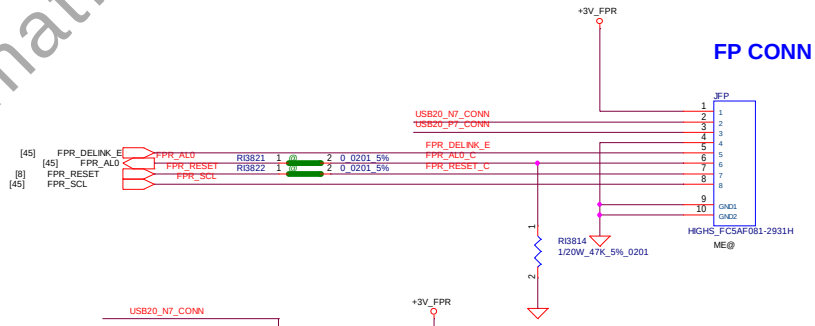


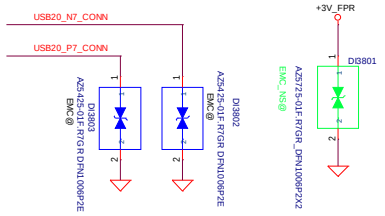
FPR POWER DISCHAGER





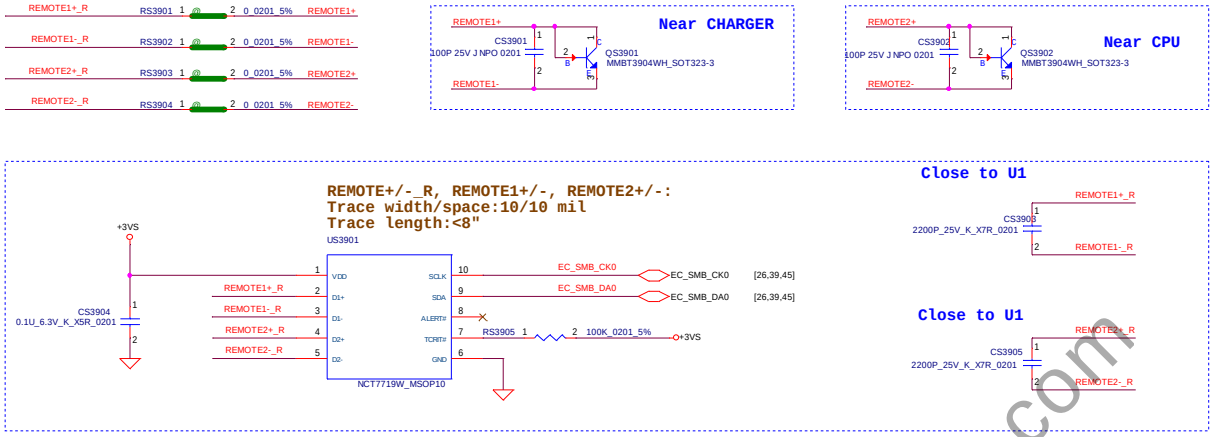
FP CONN

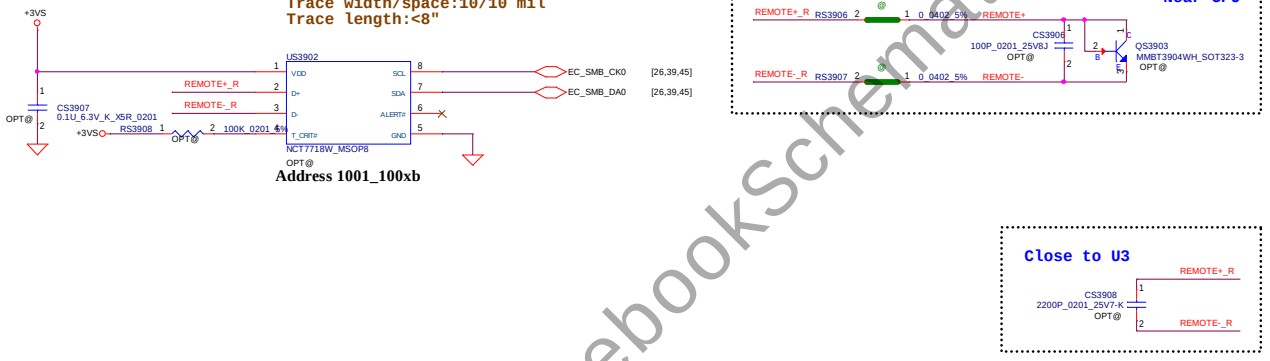




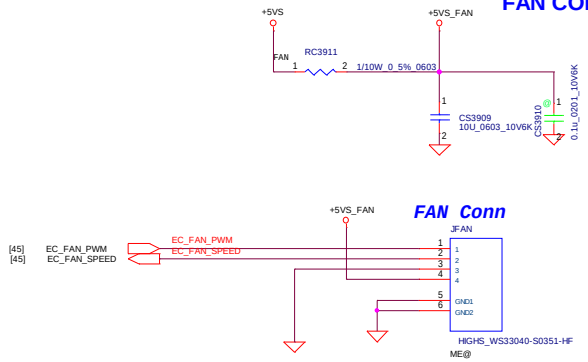
Security Classification	LC Future Center Secret Data		
Issued Date		Deciphered Date	2019/06/01

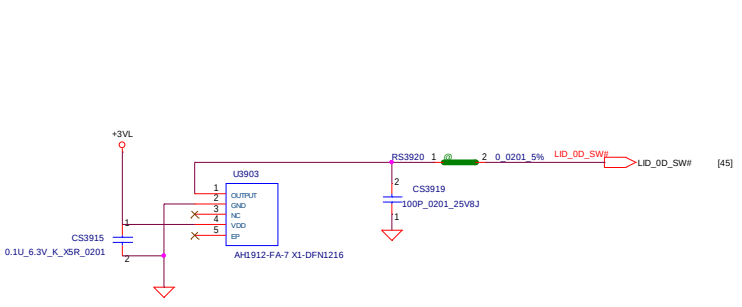
Title	S550-IIL	
Size: C	Document Number: FPR	Rev: 0.1
Date: Saturday, August 01, 2020	Sheet 38 of 61	





Confirm need???

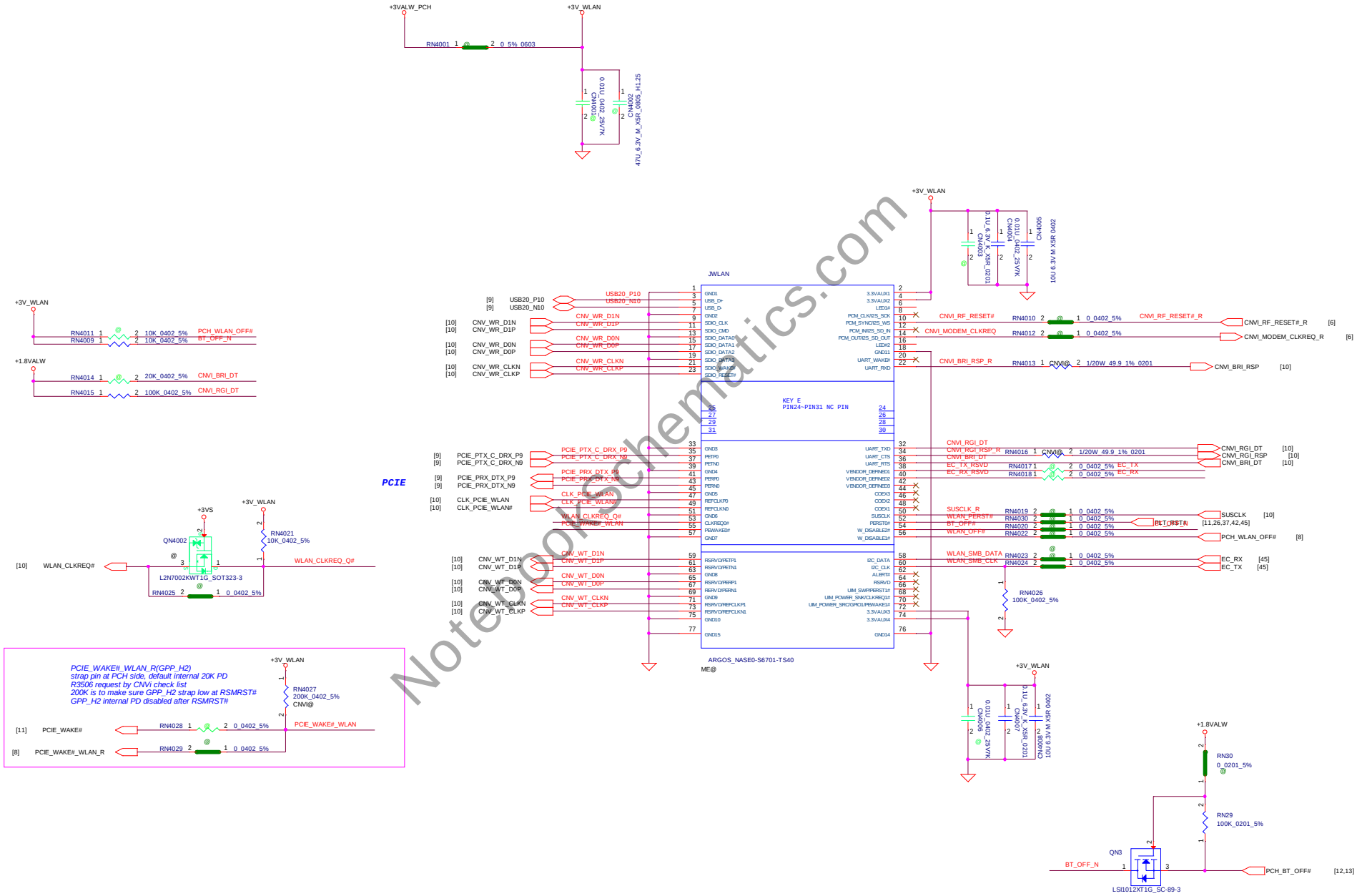




Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2017/08/15

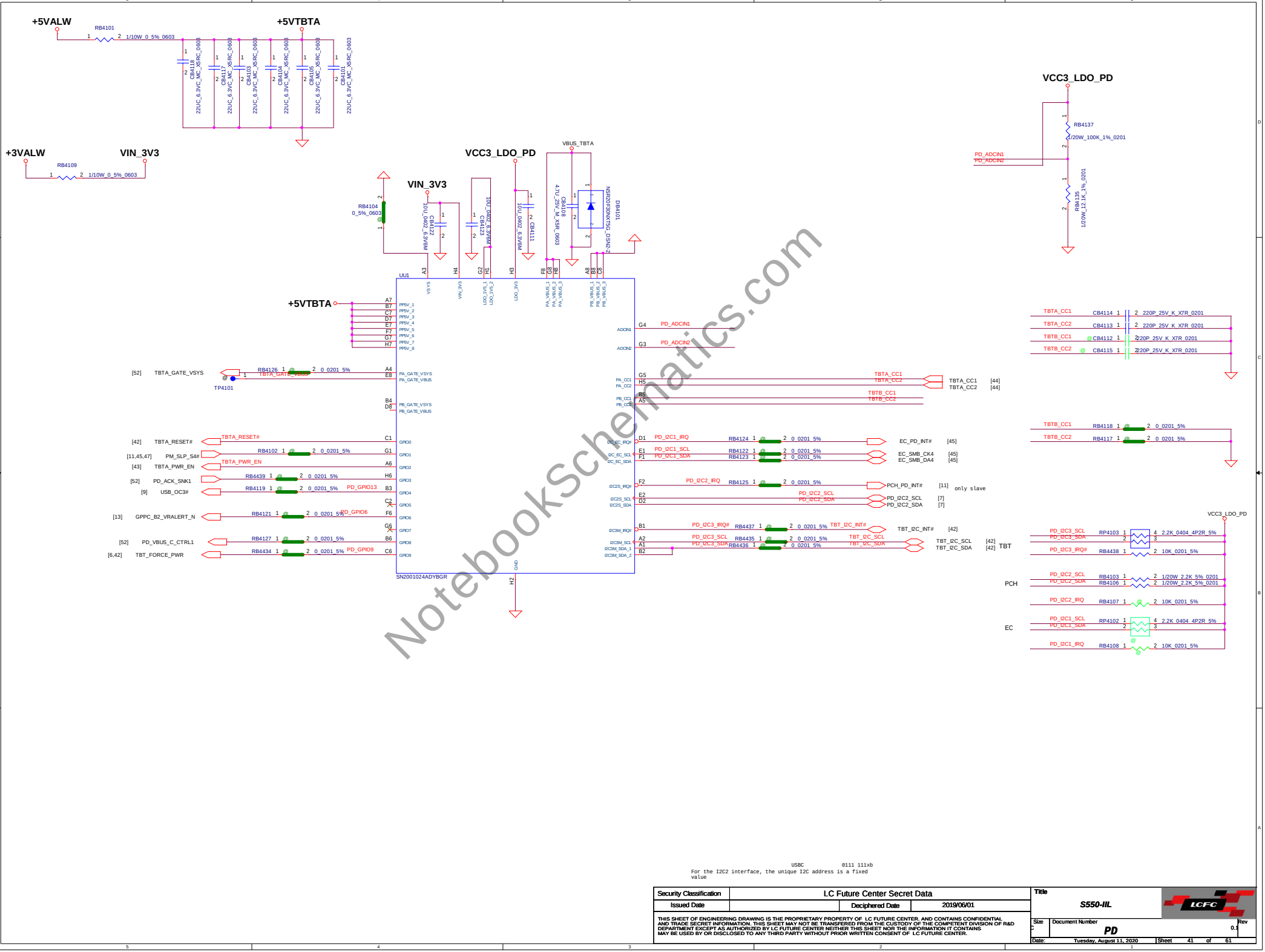
Title	S550-IIL		
Size: C	Document Number: Thermal Sensor/LID		Rev: 0.1
Date: Tuesday, August 11, 2020	Sheet 39 of 61		

Mini-Express Card(WLAN/WiMAX)



Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

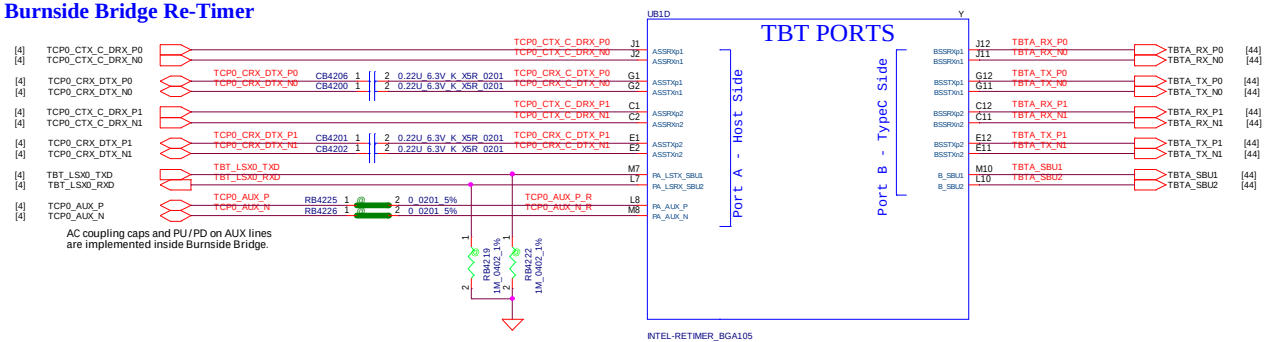
Title	S550-IIL		
Size	Document Number		Rev
C	NGFF_WLAN		0.1
Date:	Sunday, August 02, 2020	Sheet	40 of 61

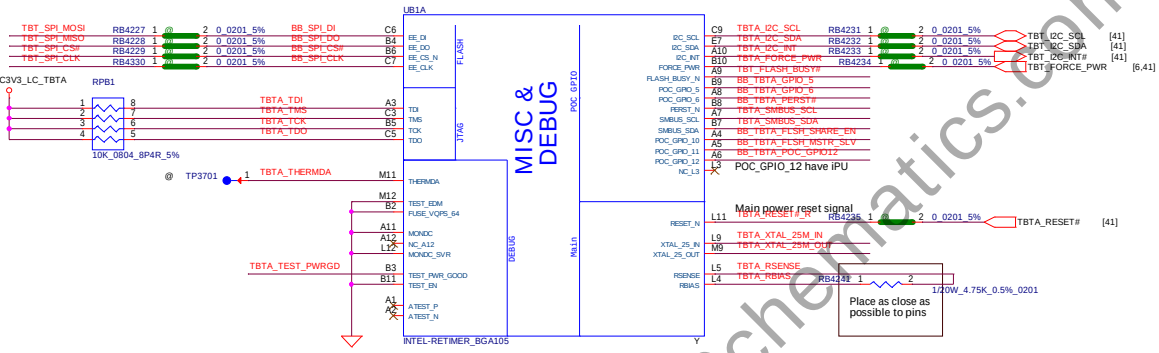


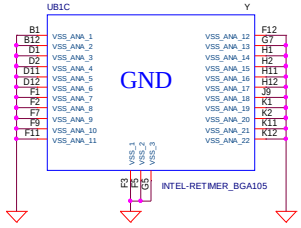
Security Classification	LC Future Center Secret Data		
Issued Date		Deciphered Date	2019/06/01

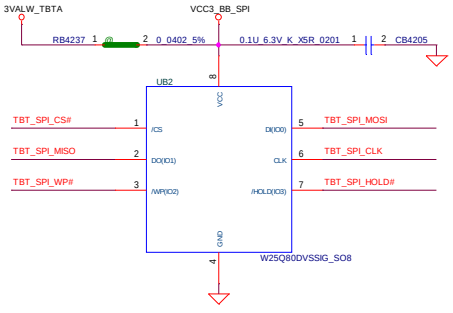
Title	S550-IIL	
Size: C	Document Number: PD	Rev: 0.1
Date: Tuesday, August 11, 2020	Sheet 41 of 61	

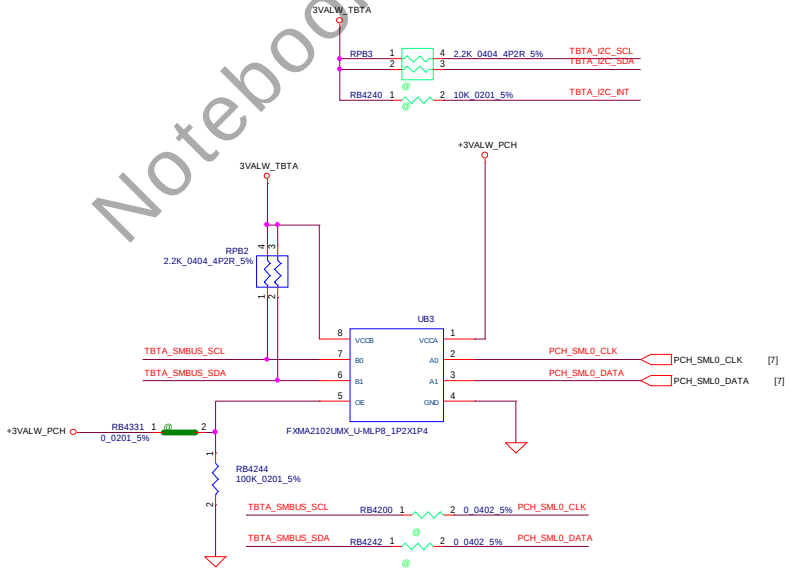
Burnside Bridge Re-Timer

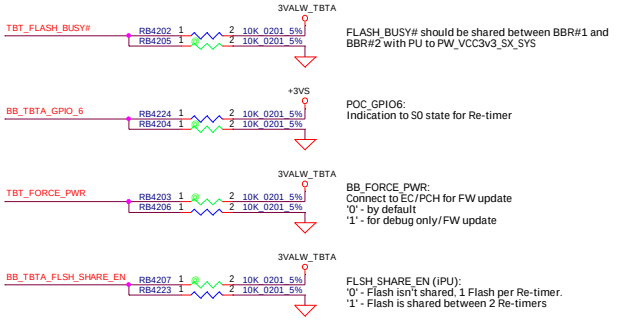


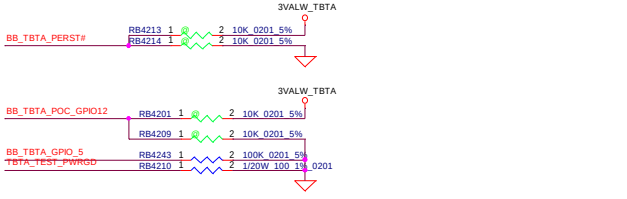






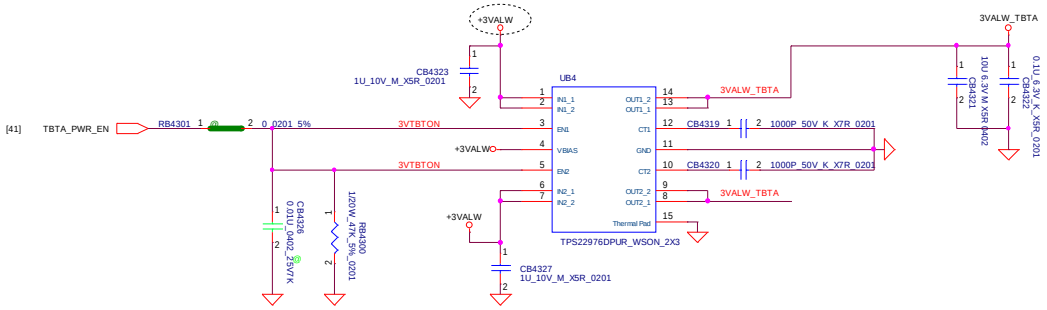




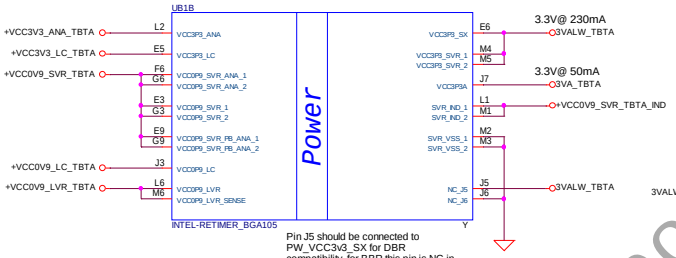


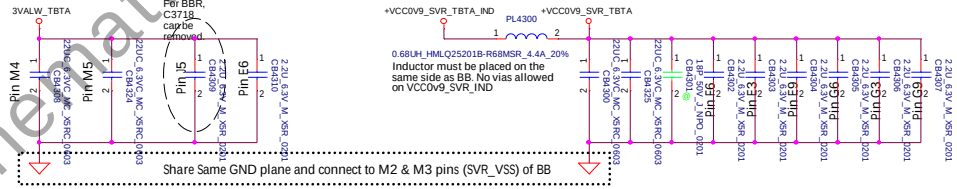
Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

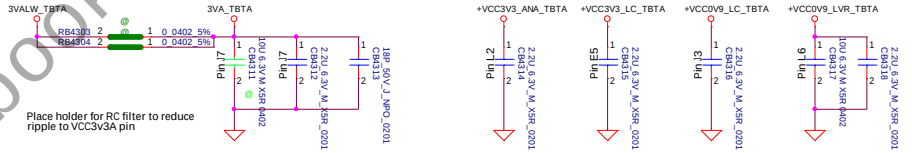
Title	S550-IIL		
Size C	Document Number	TBT_BB_PORTA	Rev 1.0
Date:	Sunday, August 02, 2020	Sheet 42 of 61	



PW_VCC3v3_SX(=3VALW_TBTA) Tolerance (+ 5%/-7.5%).
Burnside Bridge power pins which connected to PW_VCC3v3_SX should be 3.465v maximum and 3.07v minimum for normal operation.
PW_VCC3v3_SX ripple: 40mVp-p

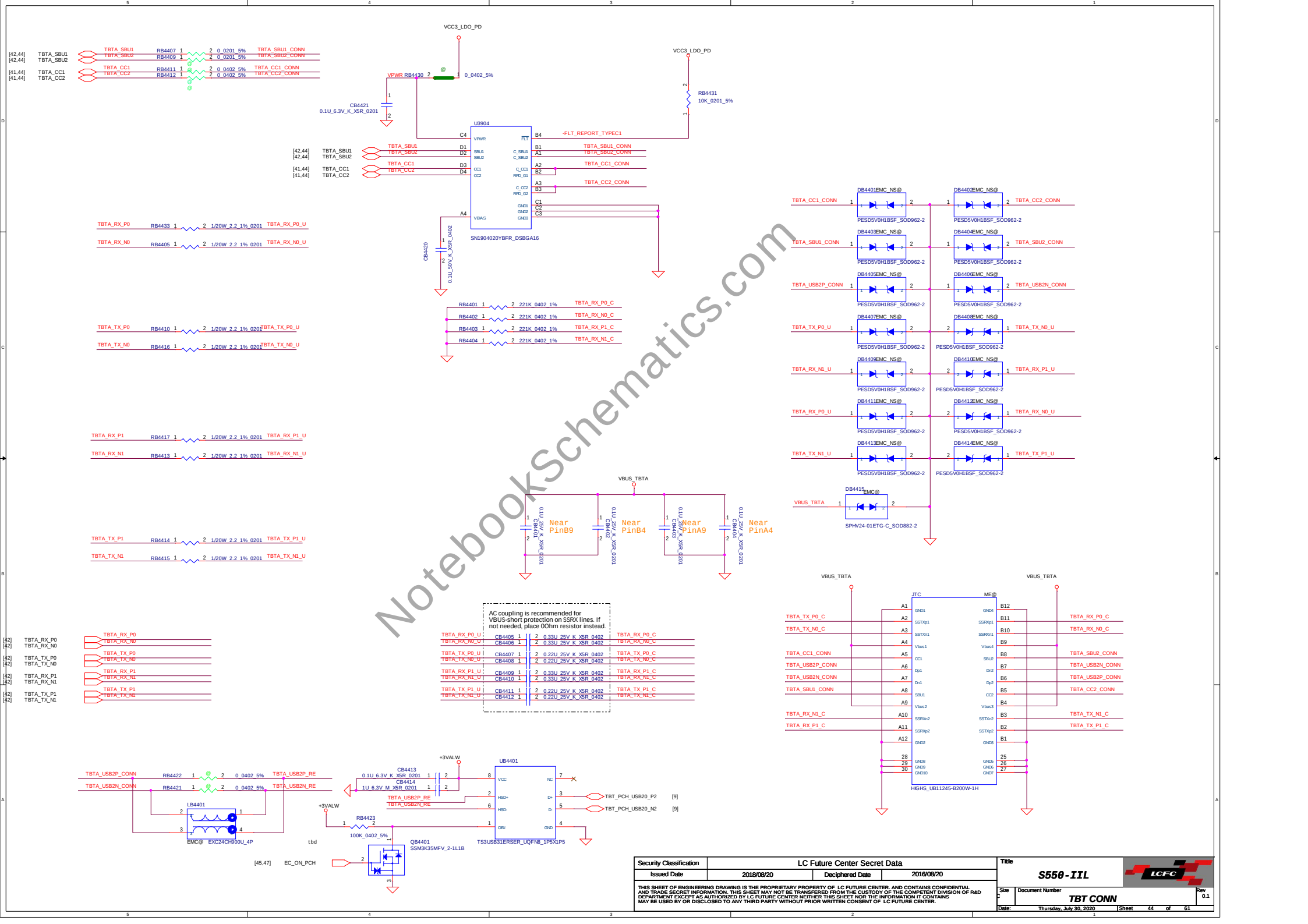






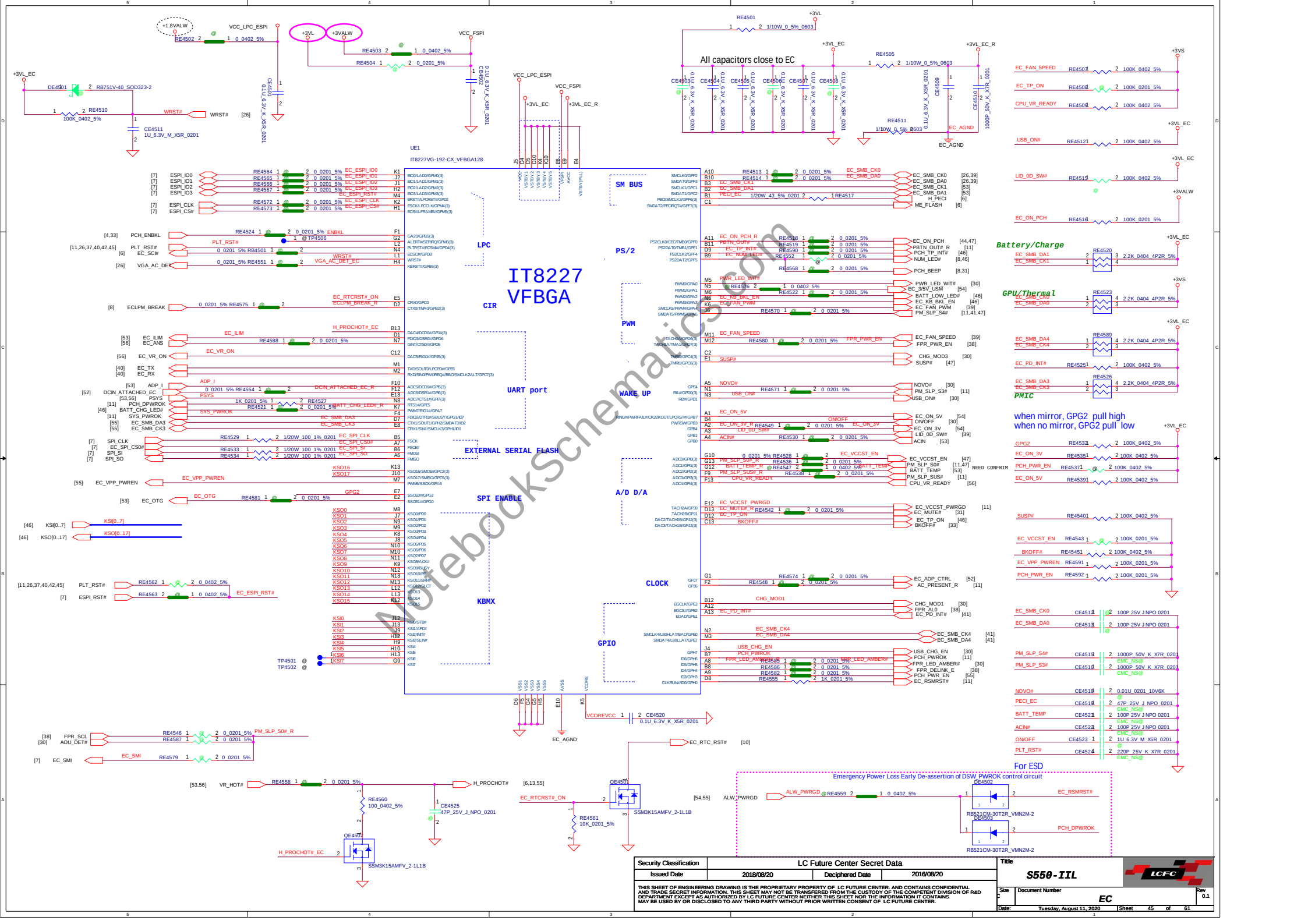
Security Classification	LC Future Center Secret Data		
Issued Date	2018/12/04	Deciphered Date	2019/08/20

Title	S550-IIL		
Size	C	Document Number	TBT_BB_PWR
Rev	1.0		
Date:	Saturday, August 01, 2020	Sheet	43 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title	S550-IIL		
Size: C	Document Number: TBT CONN		Rev: 0.1
Date: Thursday, July 30, 2020	Sheet 44 of 61		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2019/08/20

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Title	S550-IIL
Size	C
Document Number	EC
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Date:	Tuesday, August 11, 2020
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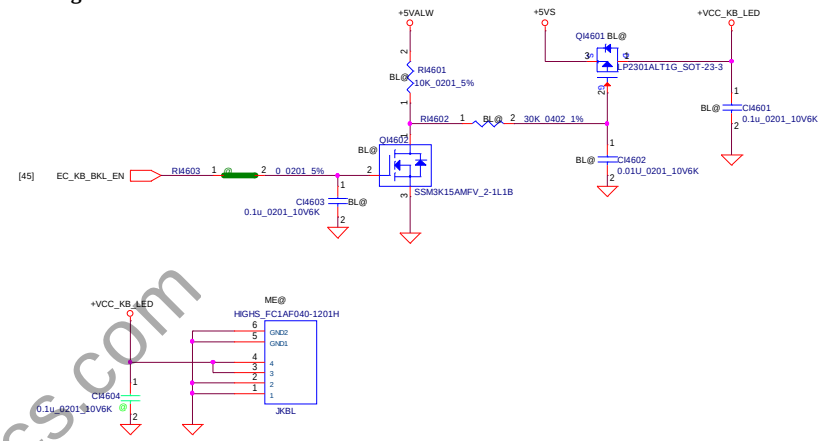
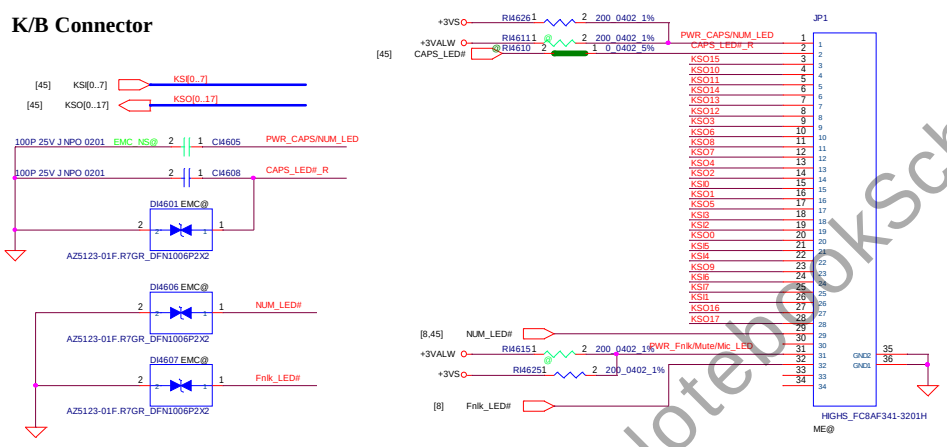
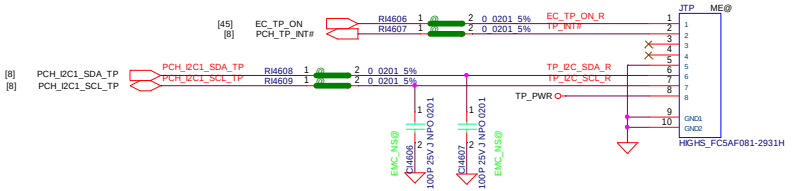
KB Backlight Connector

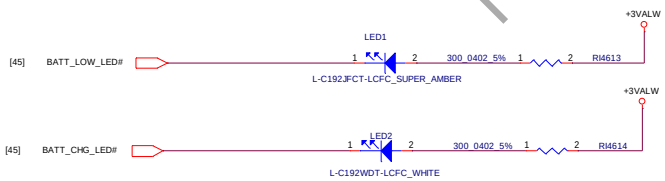


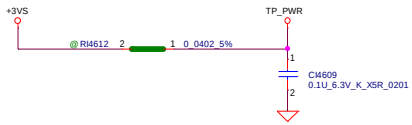
K/B Connector

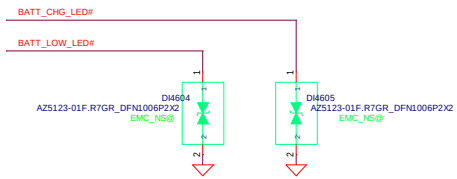


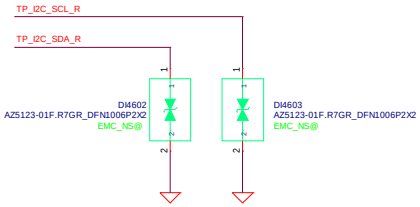
TP/B Connector







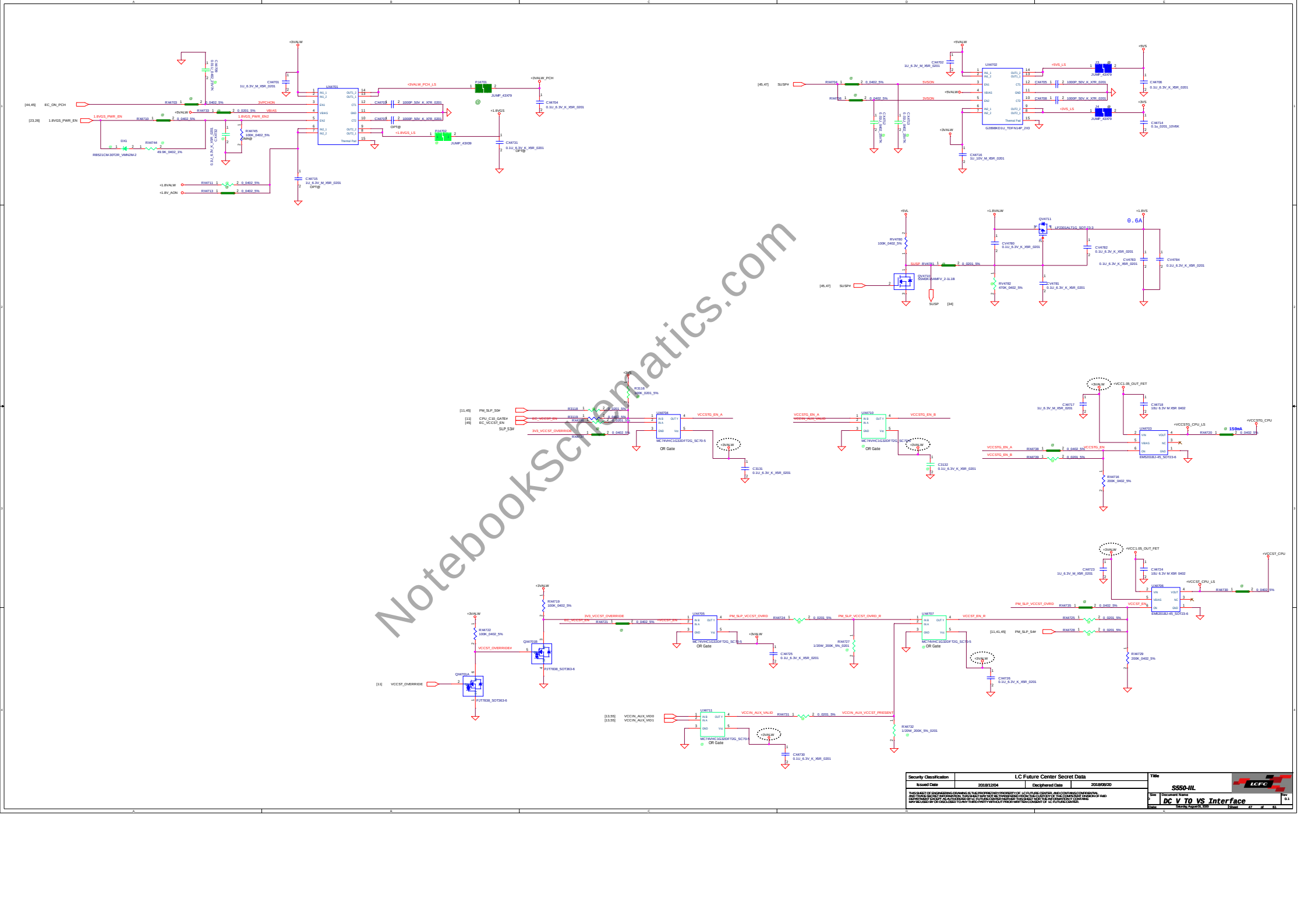




LED	Stute	LED Behavior
Charge LED	Battery only	OFF
	Charging	Amber_on(battery£°1%~90%)
		White_on(battery£°91%~100%)

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2019/08/20

Title	S550-IIL		
Size	Document Number		Rev
C	KB/FP/TP_CONN.		0.1
Date:	Sunday, August 02, 2020	Sheet	46 of 61

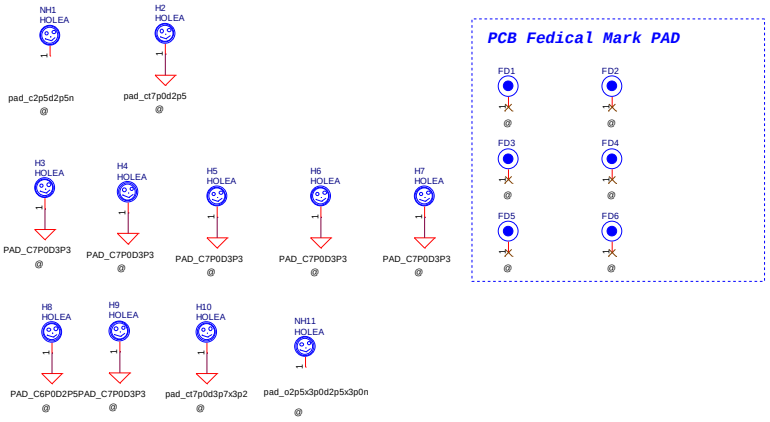


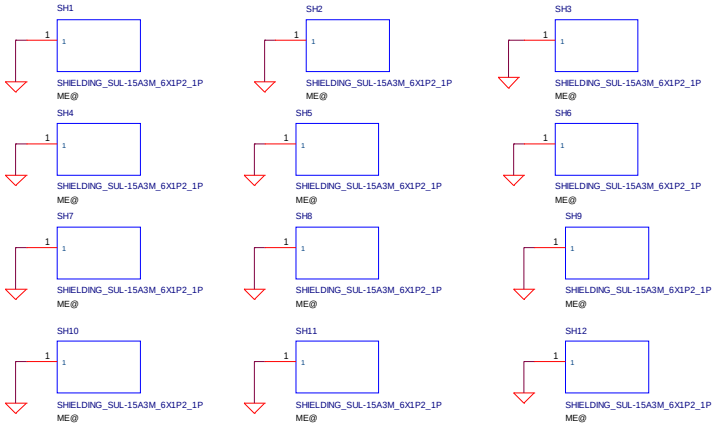
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2019/08/20

Title: **S550-IIL**

Size	Document Number	Rev
C		0.1

Date: Thursday, May 28, 2020 | Sheet 48 of 61

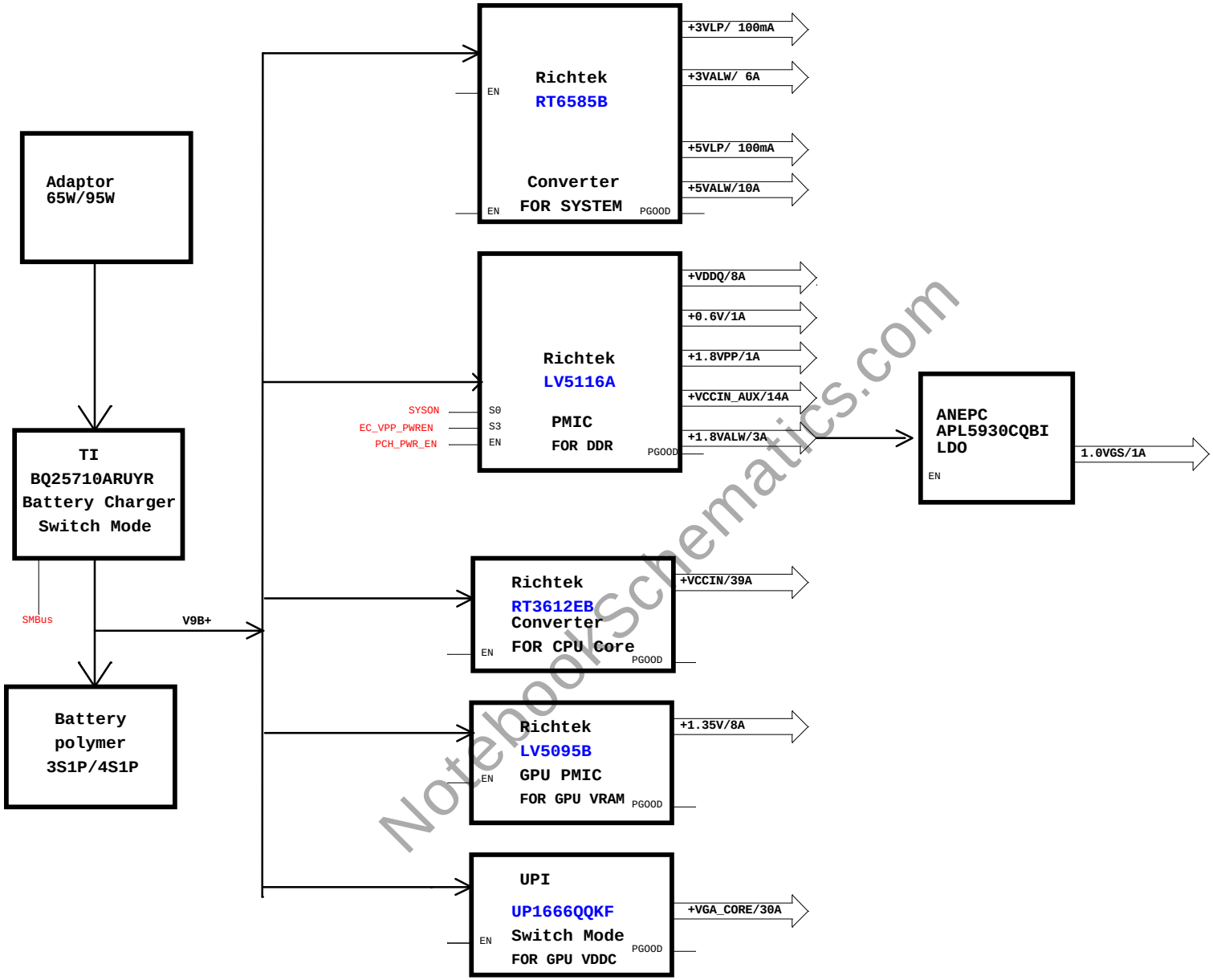




MEMORY SHELDING

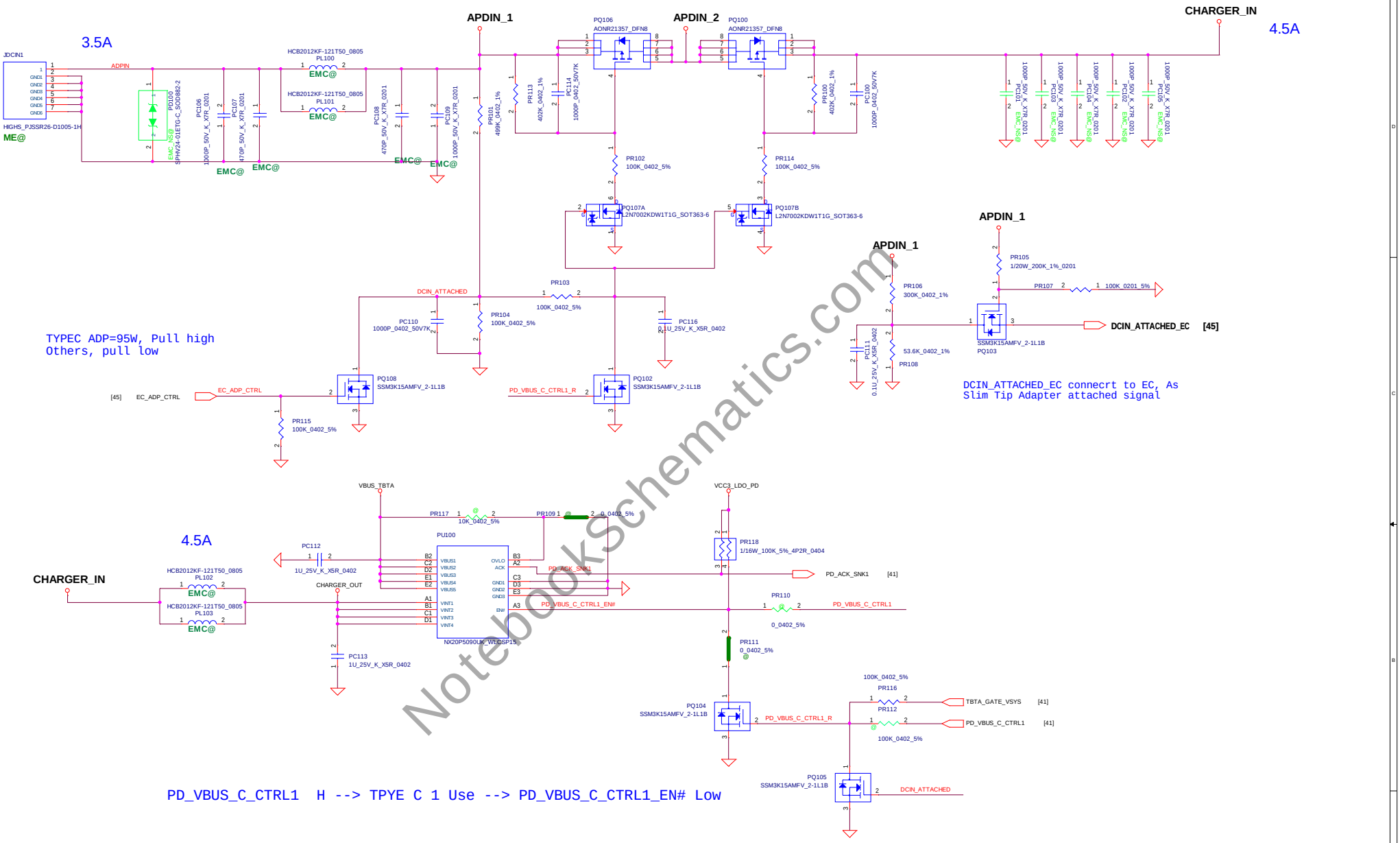
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2019/08/20

Title	S550-IIL		
Size	Document Number		Rev
C	Hole		0.1
Date:	Thursday, August 13, 2020	Sheet	49 of 61



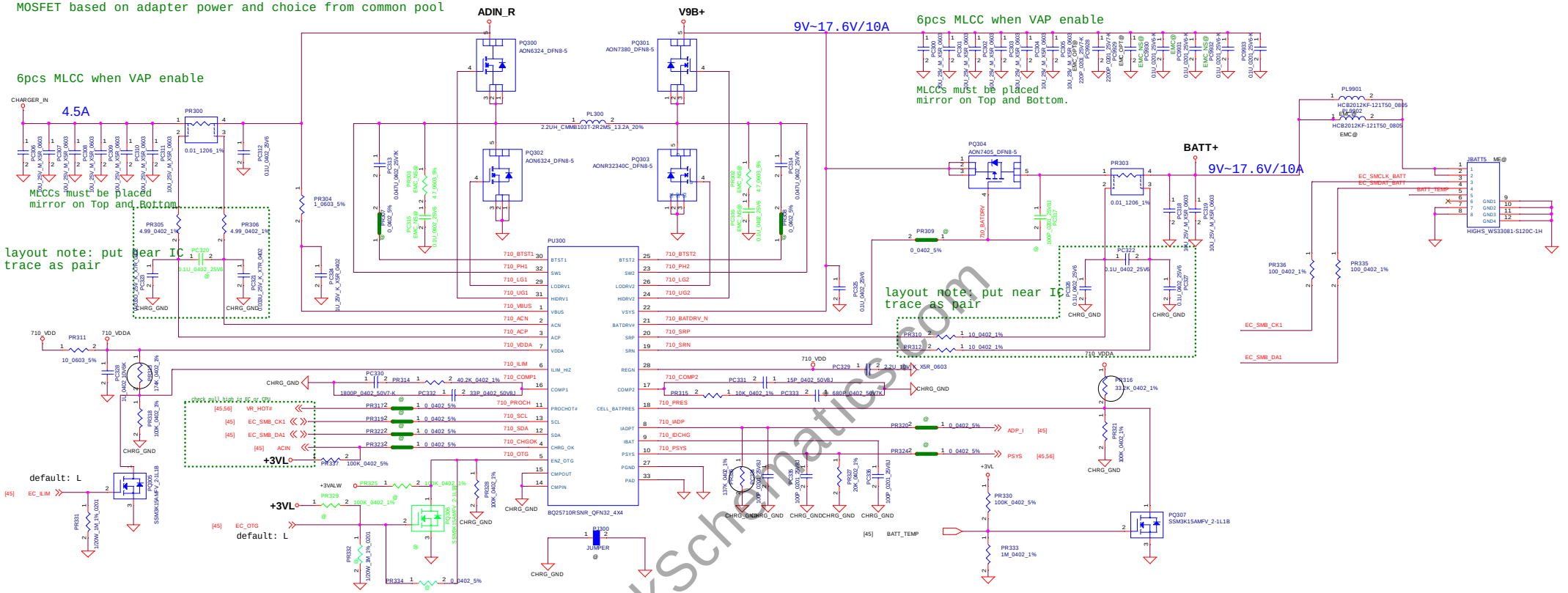
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	S550-IIL		
Size	Custom	Document Number	PWR-Power Diagram
Rev	0.1		
Date:	Thursday, May 28, 2020	Sheet	51 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	POWER SYMBOL		
Size	Document Number		Rev
C	S550 ICL		0.1
Date:	Thursday, July 30, 2020	Sheet	52 of 61



IDPM	V(ILIM)	PR313
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K
4.0A	2.6V	162K

LOGIC

VILIM=1V+40x(VACP-VACN)=1+40xIDPMxRAC

IND IN USE	PR326
1uH	93K
2.2uH	137K
3.3uH	169K

LOGIC

# of CELL	VCELL_PRES	PR316
1-CELL	1.5V	301K
2-CELL	2.4V	150K
3-CELL	3.3V	82K
4-CELL	4.5V	33.2K

LOGIC

Security Classification	LC Future Center Secret Data		
Issued Date	2018/10/25	Deciphered Date	2018/10/25

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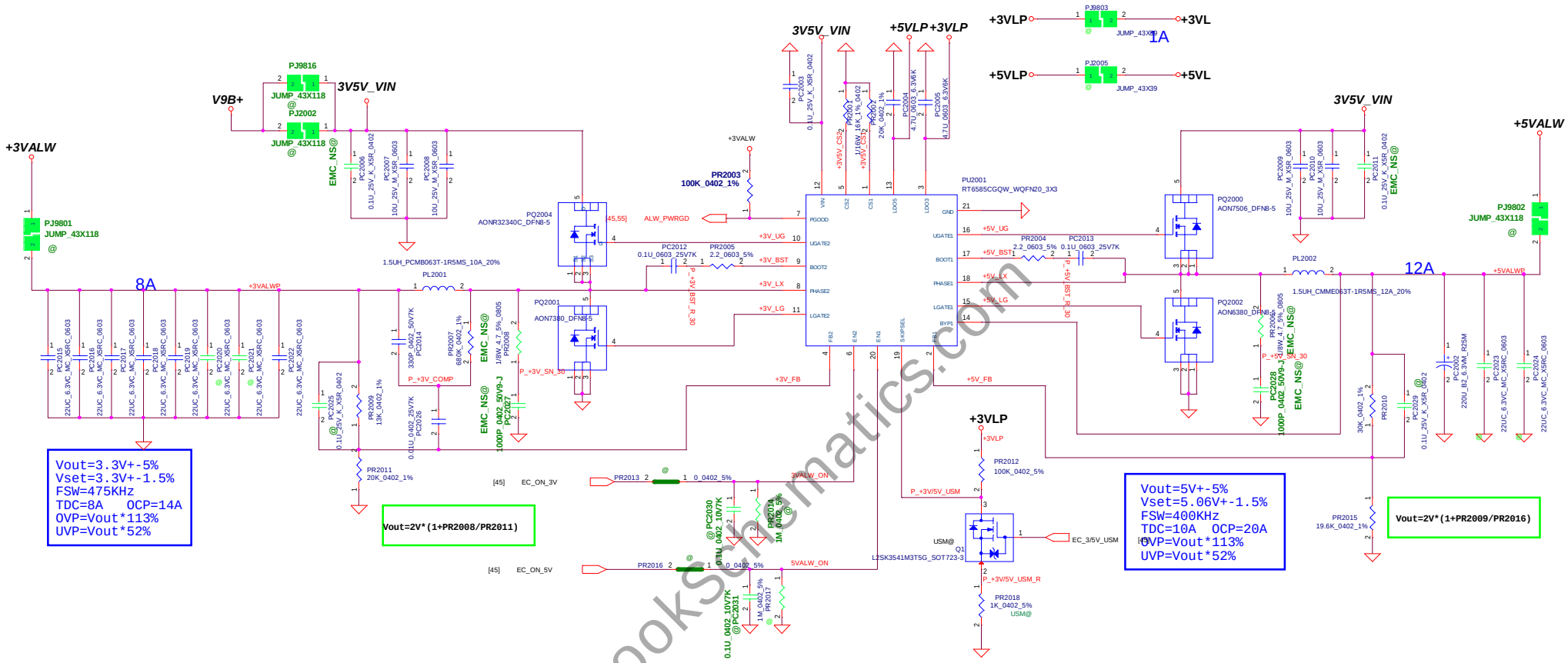
Title			
P-0301-V1.0			
Size: Custom	Document Number: S550-ICL		Rev: 1.0
Date: Thursday, July 30, 2020	Sheet 53 of 61		



	RT6585B&TPS51285B	RT6575D&TPS51275B
Mode	DEM/CCM	USM/CCM
3V FSW	475K	355K
5V FSW	400K	300K
CSx	Rlimit=(Ilimit*Rdson)*8/50uA	Rlimit=(Ilimit*Rdson)*8/10uA

RT6585B&TPS51285B BOM to BOM
RT6575D&TPS51275B BOM to BOM
RT6585B&RT6575D PIN to PIN, with different work mode, FSW, and CS setting

Security Classification	LC Future Center Secret Data		
Issued Date	2019/11/06	Deciphered Date	2019/11/05

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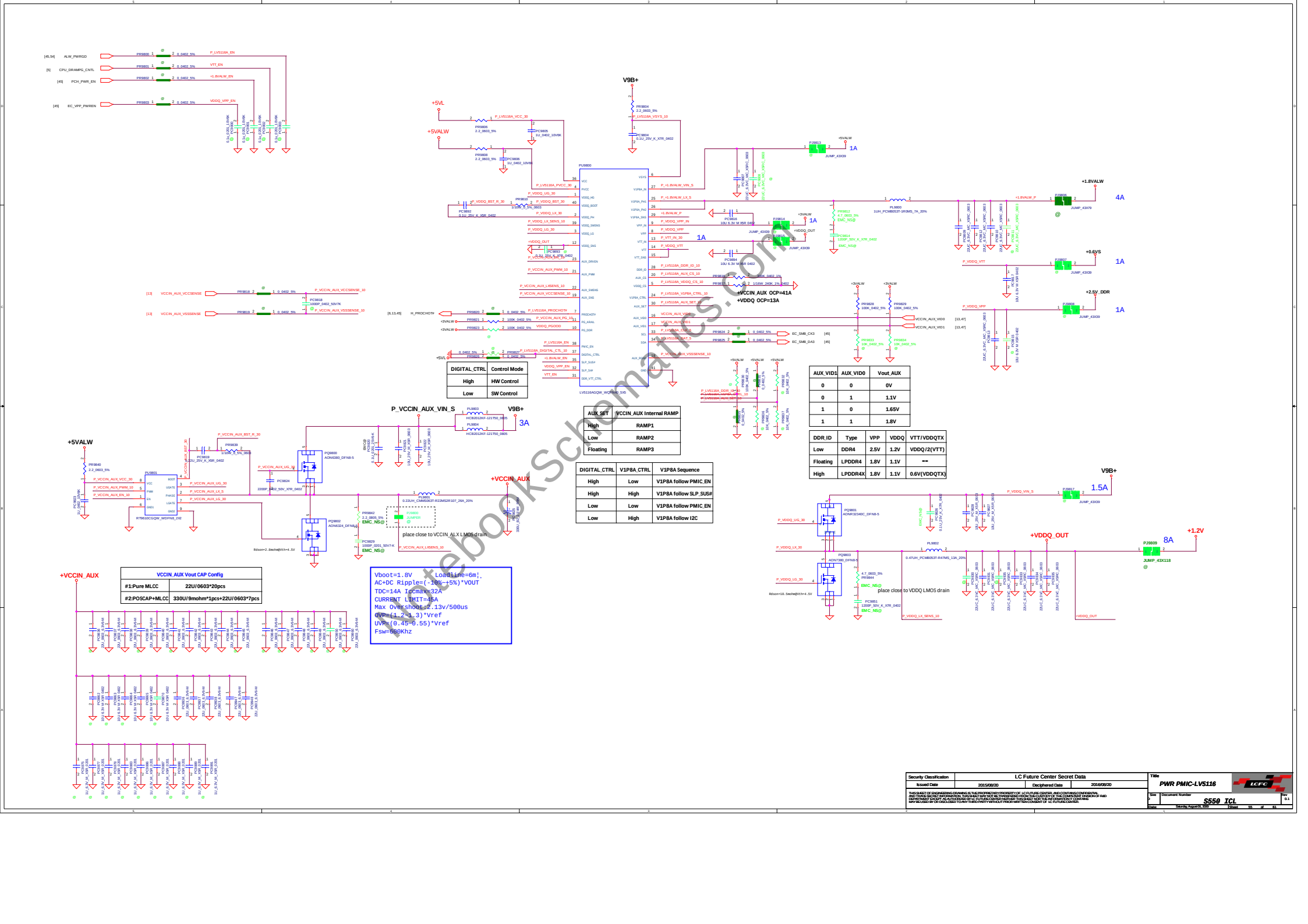
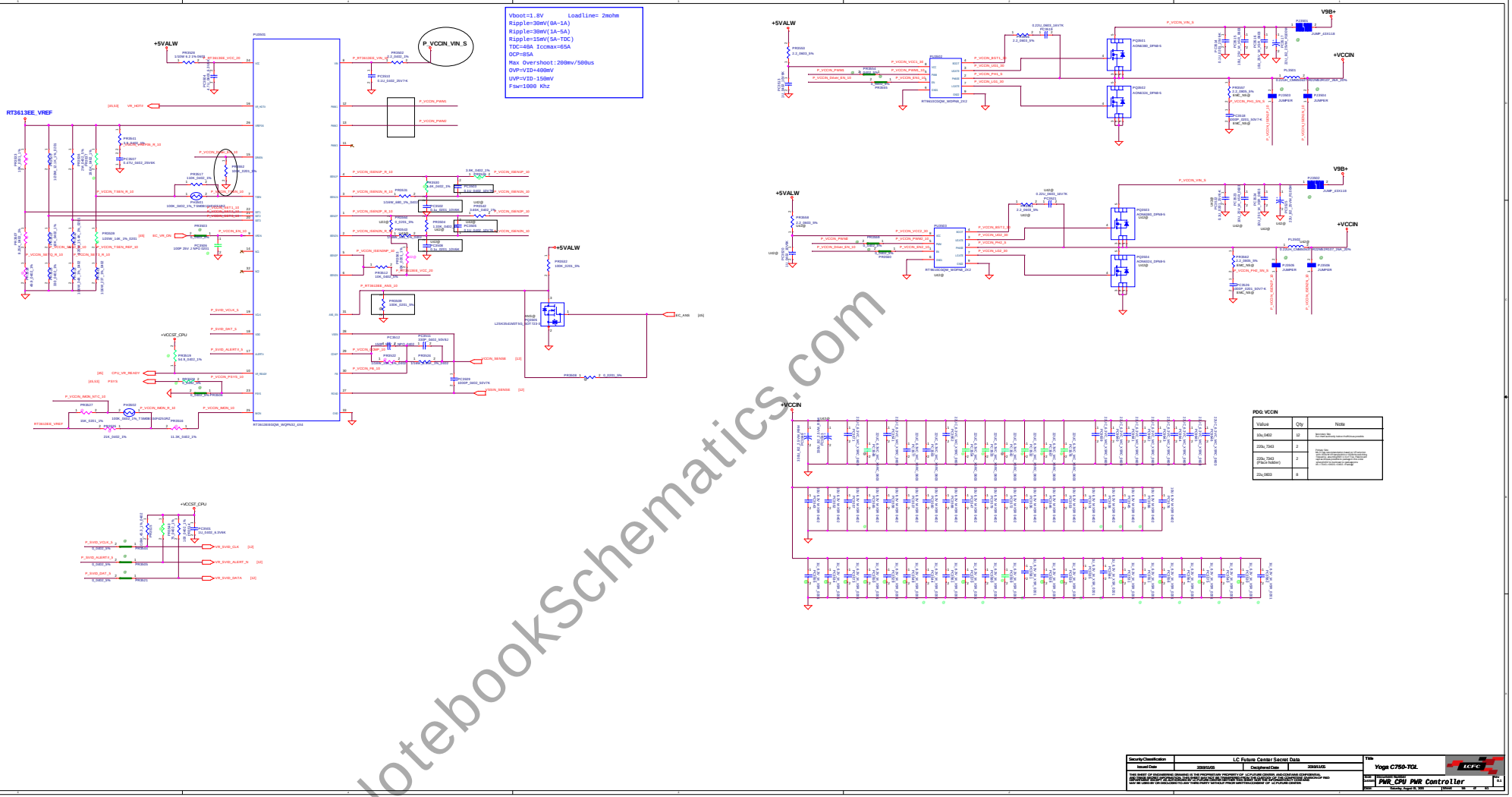
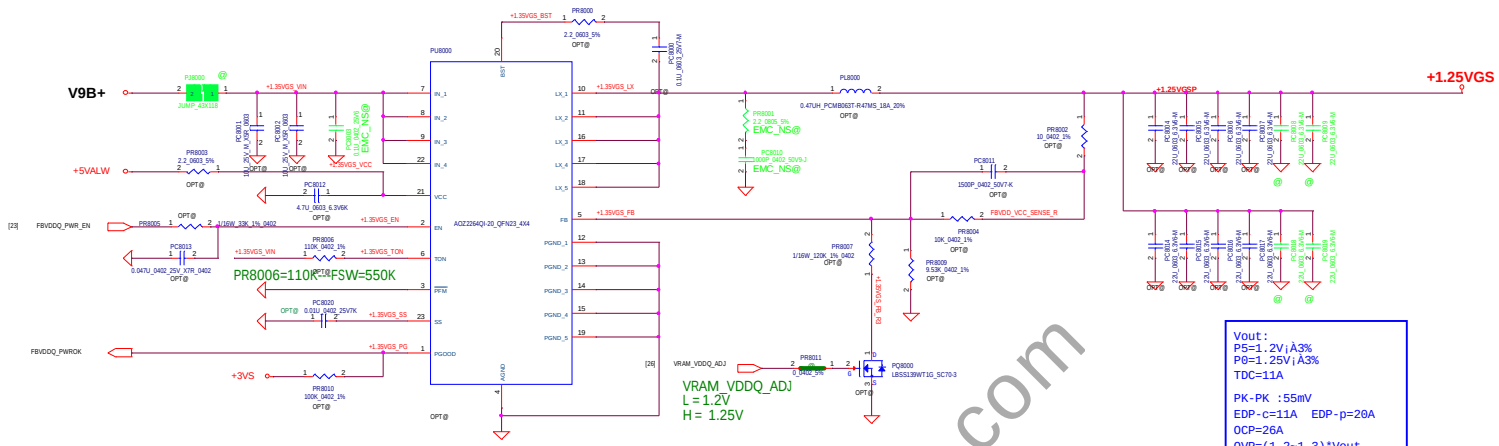
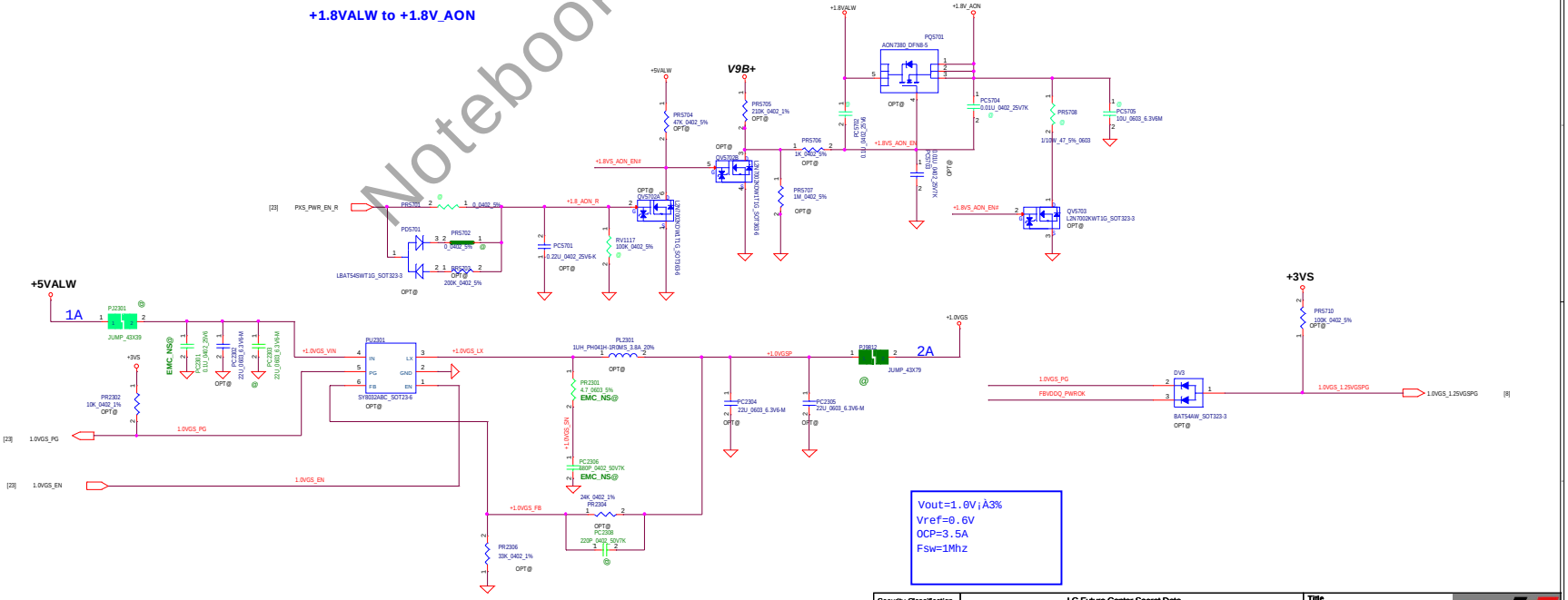
Title	Yoga C750-TGL		
Size	Document Number		Rev
C	PWR_3VALW/5VALW		0.1
Date: Saturday, August 01, 2020	Sheet 54 of 61		





Security Classification	LC Future Center Secret Data		Title: Yoga C750-TGL
Issued Date: 2020/01/03	Deciphered Date: 2020/01/03		
Size: A3	Project Code: PWR_CPU PWR Controller		Rev: 0.1
Date: Saturday, August 08, 2020	Sheet: 58 of 61		





Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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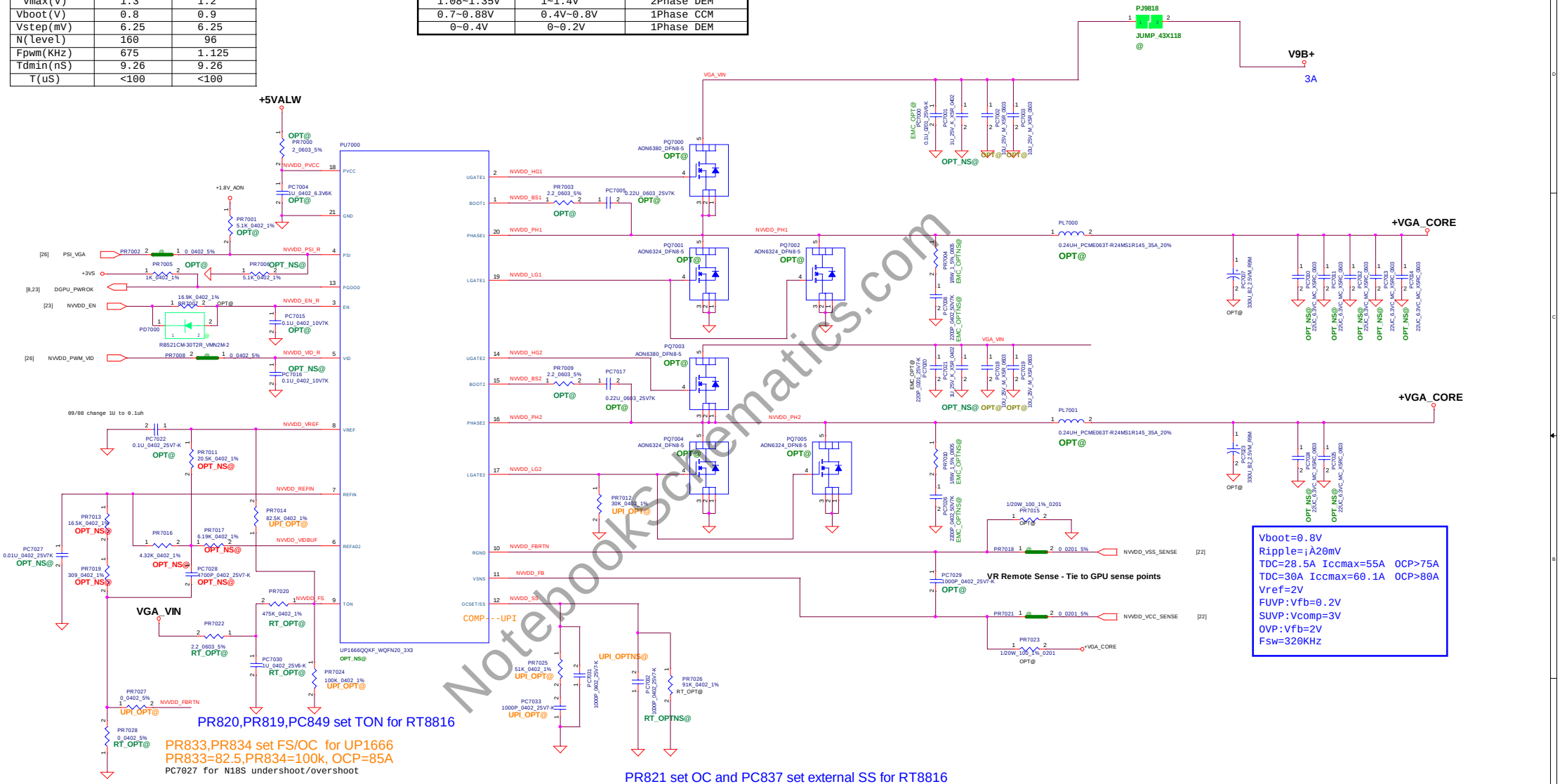
Title	PWR-FBVDDQ-AOZ2767QI		
Size: Custom	Document Number: S550-ITL		Rev: 0.1
Date: Saturday, August 01, 2020	Sheet 57 of 61		

PWM-VID Specification		
	N17 Config	N16 Config B
Vmin(V)	0.3	0.6
Vmax(V)	1.3	1.2
Vboot(V)	0.8	0.9
Vstep(mV)	6.25	6.25
N(level)	160	96
Fpwm(KHz)	675	1.125
Tdmin(nS)	9.26	9.26
T(uS)	<100	<100

RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM



PR816,PR812,PR815,PR813,PR818,PC826 BOM structure control for N16 or N17

Component	Value	N17	N16
R1(K¦¸)	PR7017	6.19	20
R2(K¦¸)	PR7011	20.5	20
R3(K¦¸)	PR7016	4.32	2
R4(K¦¸)	PR7013	16.5	18
R5(K¦¸)	PR7019	0.309	0
C(nF)	PC7028	4.7	2.7

UPI_OPT@ : for UP1666
RT_OPT@ : for RT8816A

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR-VGA_CORE
Size: Custom | Document Number: S550 ICL | Rev: 0.1
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Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/20	Deciphered Date	2016/08/20

Title: **POWER CHANGE LIST**

Size	Document Number	Rev
C	FYG41	0.1

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20200513
1. P045: GPF4 change form CAPS_LED# to PCH_TP_INT# add RE4590
2.P06:GPP_A13 change form FB_GC6_EN_R to PCH_BT_OFF#
3.P08: Remove GPP_C13 PCH_BT_OFF#
4.P40:Add QN3&RN30&RN29 for level shirft to PCH_BT_OFF#

20200514
1. P033: Add 100pf cup CG3421 on DMIC_CLK
2. P08: Add PU on CAPS_LED#/Fnlk_LED#/NUM_LED#
3. P055 Add 3*22u cap on VCCIN_AUX PC9936/PC9937/PC9938
4. P056 ADD 8*22u cap

20200518
1. P11: Add PD Resistor on Sleep_wlan RC1138
2. P45: Add PD Resistor on VPP_EN/PCH_POWER_EN RE4591/RE4592
3. P40: RN4009 change net name

20200520
1. P07: SPI ROM Co-lay

20200525
1. P55:Add 2*22U cap on VCCIN_AUX
2.Add NCTF test pad PIN DW51,DV52,DP53,DV1,DN1,B52,A49,B2

20200526
1. P07:change SPI ROM Colay
2.remove NCTF test pad TP4507&TP4511

20200624
1. P41 Remove L4401,L4402,L4403,L4404
2.P41 change RB4433,RB4405,RB4410,RB4416,RB4417,RB4413,RB4414,RB4415 from 0ohm to 2.2ohm

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **POWER SYMBOL**

Size	Document Number	Rev
C	S550-IIL	0.1

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