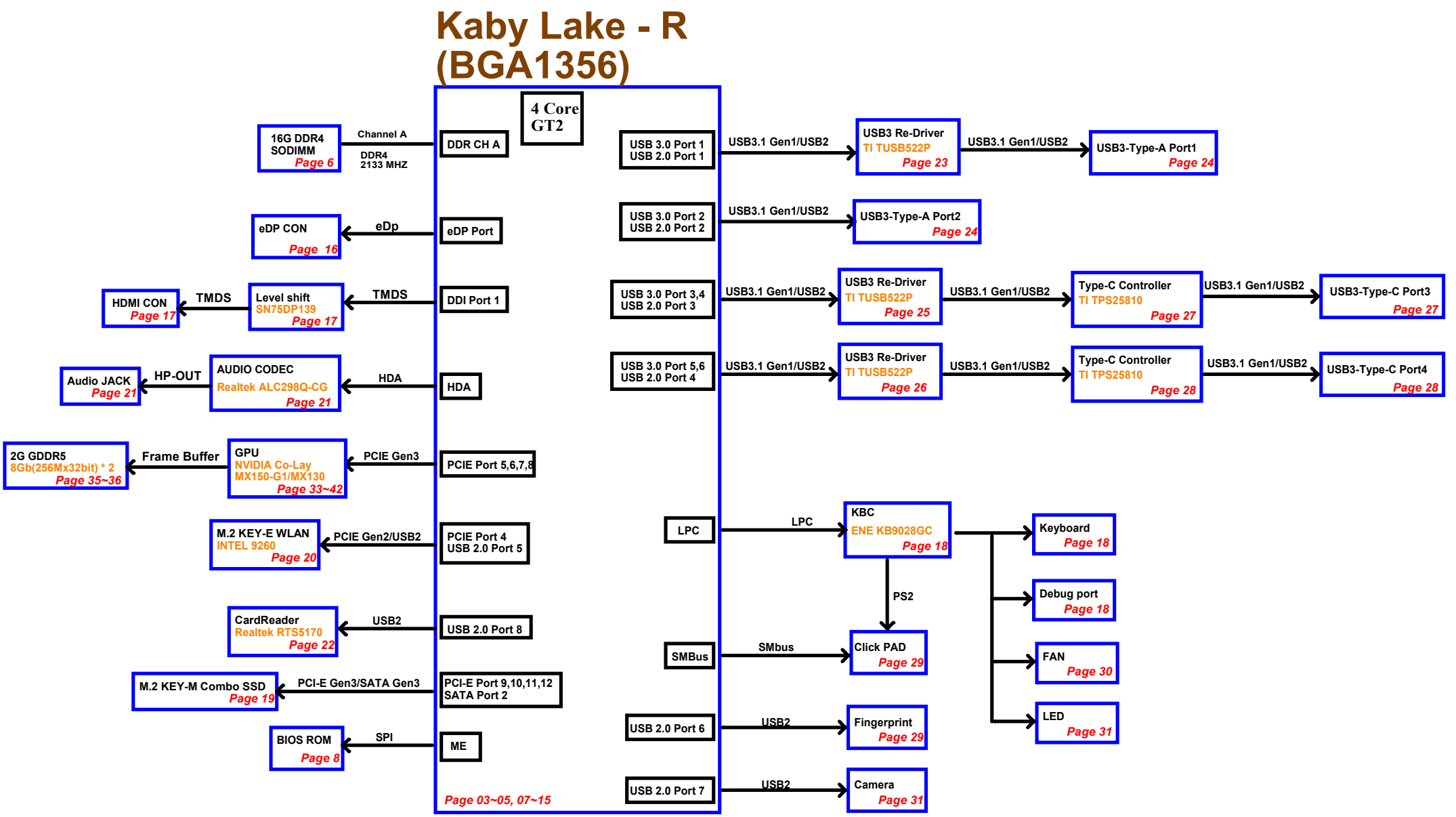
KabyLake Processor-R Platform MS-14B1 VER : 0C



MICRO-STAR INT'L CO.,LTD.

Title: BLOCK DIAGRAM

Size: Custom | Document Number: MS-14B1 | Rev: 0C

Date: Thursday, December 21, 2017 | Sheet 1 of 57

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

POWER STATES

Voltage	Description	Control Signal	SLP_S5#	SLP_S4#	SLP_S3#
PWR_SRC	AC ADAPTER OR BATTERY IN		HIGH	HIGH	HIGH
+5VALW	5.0V always on power rail	PWR_SRC	ON	ON	ON
+3VALW	3.3V always on power rail	PWR_SRC	ON	ON	ON
+5VSUS	5.0V power rail	SUS_ON	ON	ON	ON
+3VSUS	3.3V power rail	SUS_ON	ON	ON	ON
+1_8VSUS	1.8V power rail	3V5VSUSPWRGD	ON	ON	ON
+1VSUS	1.0V power rail	1_8VSUSPWRGD	ON	ON	ON
+2_5VMEM_VPP	2.5V power rail DDR (off in S4-S5)	DIMM_ON_VPP	OFF	ON	ON
+VCCST	1.0V power rail CPU (off in S4-S5)	DIMM_ON_VPP	OFF	ON	ON
+VCCPLL	1.0V power rail CPU (off in S4-S5)	+VCCST	OFF	ON	ON
+1_2VDIMM	1.2V power rail DDR (off in S4-S5)	DIMM_ON_VDDQ	OFF	ON	ON
+VDDQC	1.2V power rail CPU DRAM (off in S4-S5)	+1_2VDIMM	OFF	ON	ON
+VCCPLL_OC	1.2V power rail CPU (off in S4-S5)	+1_2VDIMM	OFF	ON	ON
+5VRUN	5.0V switched power rail (off in S3-S5)	RUND	OFF	OFF	ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUND	OFF	OFF	ON
+1_8VRUN	1.8V power rail AUDIO (off in S3-S5)	RUND	OFF	OFF	ON
+VCC_IO	1.0V rail for Processor & PCH (off in S3-S5)	RUND	OFF	OFF	ON
+VCCSTG	1.0V power rail CPU (off in S3-S5)	+VCC_IO	OFF	OFF	ON
+0_6VTT_RUN	0.6V DDR Termination voltage (off in S3-S5)	DDR_VTT_CTRL	OFF	OFF	ON
+VCC_SA	0.55V to 1.15V Voltage for Processor	VR_ON	OFF	OFF	ON
+VCC_CORE	0.55V to 1.5V Voltage for Processor	VR_ON	OFF	OFF	ON
+VCC_GT	0.55V to 1.52V Core Voltage for Processor	VR_ON	OFF	OFF	ON

Note: WHEN AC MODE, System turn on then +*VSUS will always keep high

S4(Suspend to Disk)
S3(Suspend to RAM)
S0(Full ON)

MICRO-STAR INT'L CO.,LTD.

Title: PLATFORM

Size: Custom | Document Number: MS-14B1 | Rev: 0C

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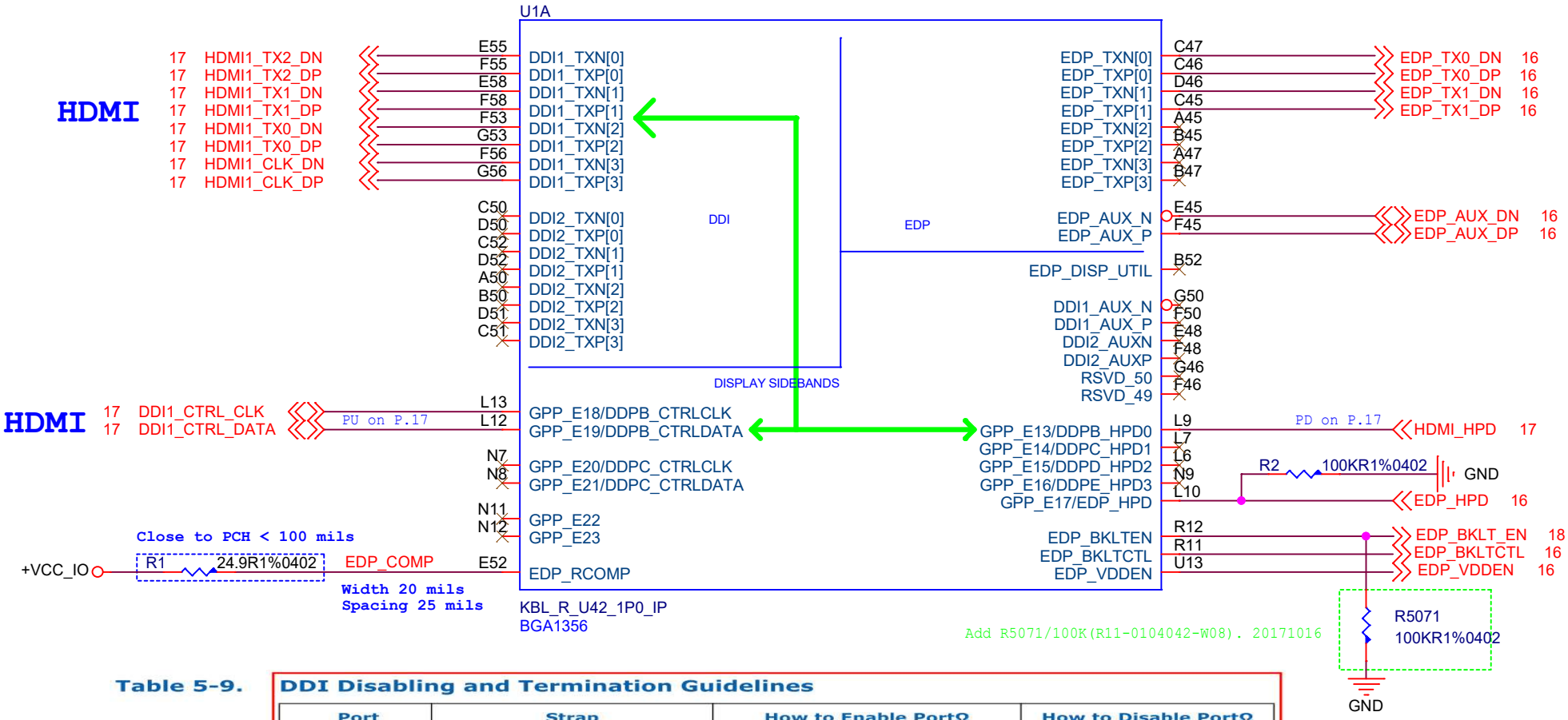

Table 5-9. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable PortΩ	How to Disable PortΩ
Port 1	DDPB_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect

CPU1

CPU

X_KABY LAKE-R,QUAD CORE i7-8550U

A0D-8550U05-I06

CPU2

CPU

MVT要換掉

X_KABY LAKE-R,QUAD CORE i5-8250U

OAC-14B1001-I06

Change CPU2 P/N from A0C-8250U05-I06 to OAC-14B1001-I06 for PM. 20171020

MICRO-STAR INT'L CO.,LTD.

Title: Kabylake-R (EDP & HDMI)

Size	Document Number	Rev
Custom	MS-14B1	0C

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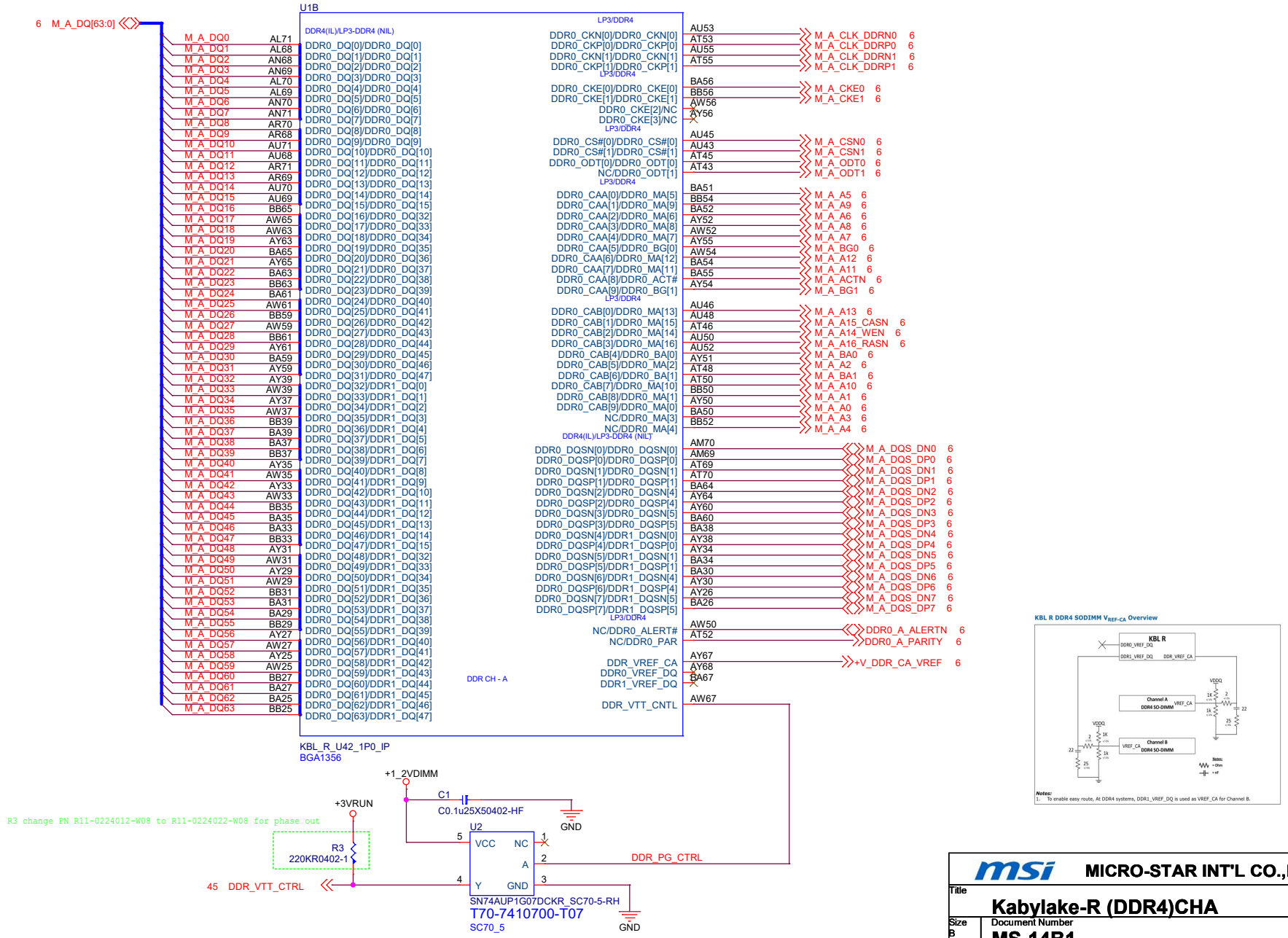
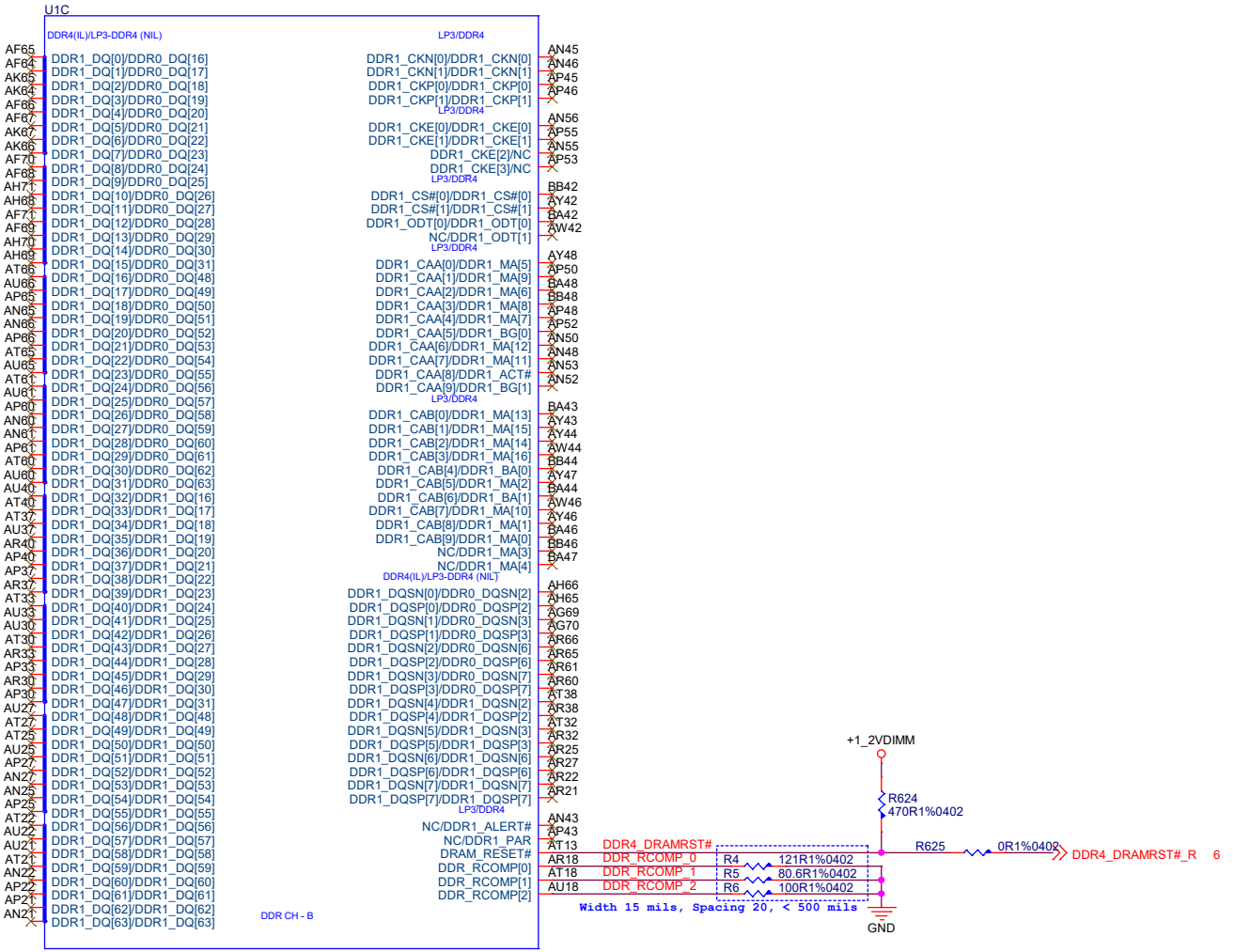


MICRO-STAR INT'L CO.,LTD.			
Title: Kabylake-R (DDR4)CHA			
Size: B	Document Number: MS-14B1		Rev: 0C
Date: Thursday, December 21, 2017	Sheet 4 of 57		



MICRO-STAR INT'L CO.,LTD.		
Title: Kabylake-R (DDR4)CHB		
Size: B	Document Number: MS-14B1	Rev: 0C
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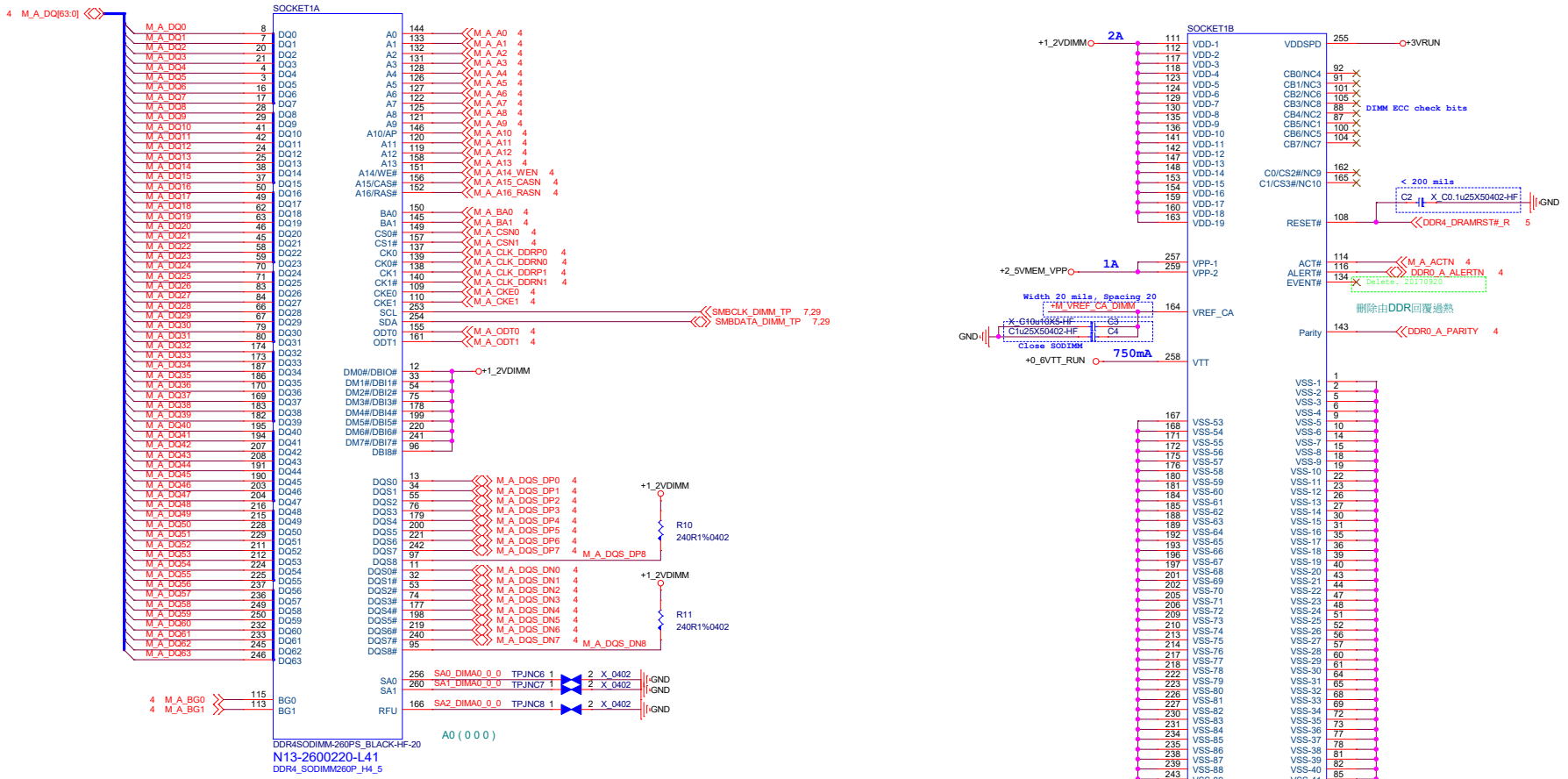
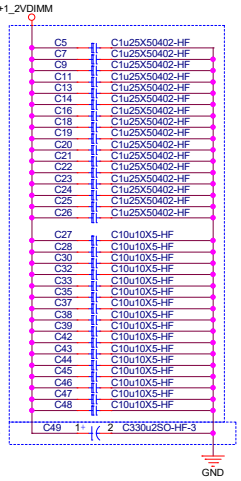
SODIMM_A (Bottom)



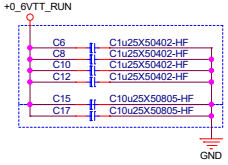
VDDQ

Close to VDD pin



1 placehoder

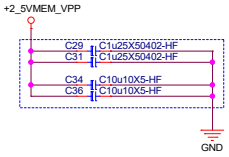
VTT



Place VTT plane to close SODIMM

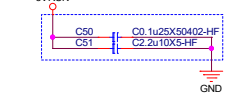
Placehoder Place VTT plane to close SODIMM

VPP

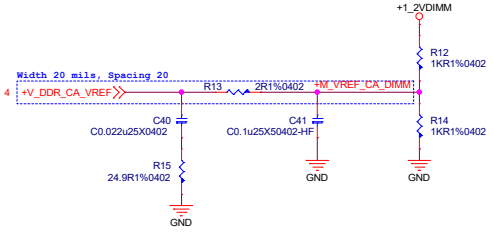


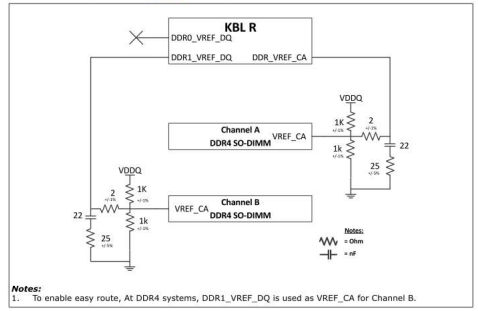
DRAM Side

VDDSPD



Place close to DRAM





msi	MICRO-STAR INT'L CO.,LTD.	
Title	DDR4_SODIMM_A	
Size: Custom	Document Number: MS-14B1	Rev: 0C
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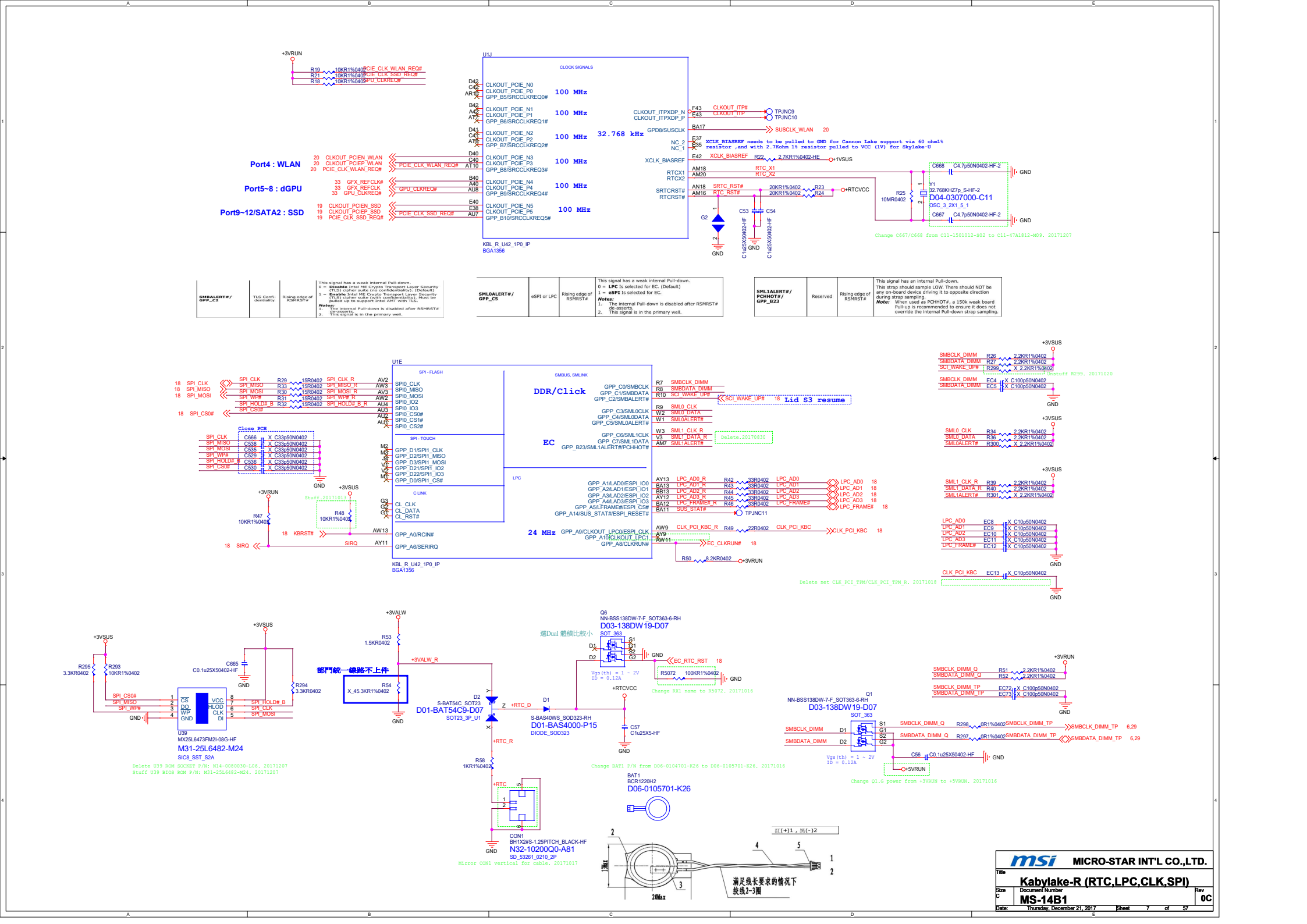
+3VRUN
R19 10KR1%0402 PCIE_CLK_WLAN_REQ#
R21 10KR1%0402 PCIE_CLK_SSD_REQ#
R18 10KR1%0402 GPU_CLKREQ#
U1J
CLOCK SIGNALS
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
GPP_B5/SRCCLKREQ0#
100 MHz
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
GPP_B6/SRCCLKREQ1#
100 MHz
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
GPP_B7/SRCCLKREQ2#
100 MHz
32.768 kHz
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
GPP_B8/SRCCLKREQ3#
100 MHz
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
GPP_B9/SRCCLKREQ4#
100 MHz
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
GPP_B10/SRCCLKREQ5#
100 MHz
Port4 : WLAN
Port5~8 : dGPU
Port9~12/SATA2 : SSD
PCIE_CLK_WLAN_REQ#
GPU_CLKREQ#
PCIE_CLK_SSD_REQ#
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_ITP#
CLKOUT_ITP
TPJNC9
TPJNC10
GPD8/SUSCLK
SUSCLK_WLAN
XCLK_BIASREF needs to be pulled to GND for Cannon Lake support via 60 ohm1% resistor ,and with 2.7Kohm 1% resistor pulled to VCC (1V) for Skylake-U
XCLK_BIASREF
R22 2.7KR1%0402-HE
+1VSUS
RTCX1
RTCX2
RTC_X1
RTC_X2
SRTCRST#
RTCRST#
SRTC_RST#
RTC_RST#
20KR1%0402 R23
20KR1%0402 R24
+RTCVCC
R25 10MR0402
Y1 32.768KHZ7p_S-HF-2
D04-0307000-C11
OSC_3_2X1_5_1
C668 C4.7p50N0402-HF-2
C667 C4.7p50N0402-HF-2
GND
C53 C54
C1u25X5402-HF
Change C667/C668 from C11-1501012-S02 to C11-47A1812-M09. 20171207
KBL_R_U42_1P0_IP
BGA1356
SMBALERT#/ GPP_C2
TLS Confidentiality
Rising edge of RSMRST#
This signal has a weak internal Pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
Notes:
1. The internal Pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.
SML0ALERT#/ GPP_C5
eSPI or LPC
Rising edge of RSMRST#
This signal has a weak internal Pull-down.
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.
Notes:
1. The internal Pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.
SML1ALERT#/ PCHHOT#/ GPP_B23
Reserved
Rising edge of RSMRST#
This signal has an internal Pull-down.
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
Note: When used as PCHHOT#, a 150k weak board Pull-up is recommended to ensure it does not override the internal Pull-down strap sampling.
U1E
SPI - FLASH
SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#
SPI_CLK
SPI_MISO
SPI_MOSI
SPI_WP#
SPI_HOLD#_B
SPI_CS0#
15R0402
SPI_CLK_R
SPI_MISO_R
SPI_MOSI_R
SPI_WP#_R
SPI_HOLD#_B_R
Close PCH
C666 X_C33p50N0402
C538 X_C33p50N0402
C535 X_C33p50N0402
C529 X_C33p50N0402
C536 X_C33p50N0402
C530 X_C33p50N0402
SPI - TOUCH
GPP_D1/SPI1_CLK
GPP_D2/SPI1_MISO
GPP_D3/SPI1_MOSI
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
GPP_D0/SPI1_CS#
C LINK
CL_CLK
CL_DATA
CL_RST#
SMBUS, SMLINK
DDR/Click
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
SMBCLK_DIMM
SMBDATA_DIMM
SCI_WAKE_UP#
Lid S3 resume
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
SML0_CLK
SML0_DATA
SML0ALERT#
EC
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#
SML1_CLK_R
SML1_DATA_R
SML1ALERT#
Delete.20170830
LPC
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A14/SUS_STAT#/ESPI_RESET#
LPC_AD0_R
LPC_AD1_R
LPC_AD2_R
LPC_AD3_R
LPC_FRAME#_R
SUS_STAT#
33R0402
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
TPJNC11
24 MHz
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A8/CLKRUN#
CLK_PCI_KBC_R
22R0402
CLK_PCI_KBC
EC_CLKRUN#
8.2KR0402
GPP_A0/RCIN#
GPP_A6/SERIRQ
KBRST#
SIRQ
R47 10KR1%0402
R48 10KR1%0402
Stuff.20171017
KBL_R_U42_1P0_IP
BGA1356
+3VSUS
SMBCLK_DIMM R26 2.2KR1%0402
SMBDATA_DIMM R27 2.2KR1%0402
SCI_WAKE_UP# R299 X_2.2KR1%0402
Unstuff R299. 20171020
SMBCLK_DIMM EC4 X_C100p50N0402
SMBDATA_DIMM EC5 X_C100p50N0402
SML0_CLK R34 2.2KR1%0402
SML0_DATA R36 2.2KR1%0402
SML0ALERT# R300 X_2.2KR1%0402
SML1_CLK_R R39 2.2KR1%0402
SML1_DATA_R R40 2.2KR1%0402
SML1ALERT# R301 X_2.2KR1%0402
LPC_AD0 EC8 X_C10p50N0402
LPC_AD1 EC9 X_C10p50N0402
LPC_AD2 EC10 X_C10p50N0402
LPC_AD3 EC11 X_C10p50N0402
LPC_FRAME# EC12 X_C10p50N0402
CLK_PCI_KBC EC13 X_C10p50N0402
Delete net CLK_PCI_TPM/CLK_PCI_TPM_R. 20171018
+3VALW
R53 1.5KR0402
+3VALW_R
R54 X_45.3KR1%0402
部門統一線路不上件
R295 3.3KR0402
R293 10KR1%0402
C665 C0.1u25X50402-HF
R294 3.3KR0402
U39
MX25L6473FM2I-08G-HF
M31-25L6482-M24
SIC8_SST_S2A
Delete U39 ROM SOCKET P/N: N14-0080030-L06. 20171207
Stuff U39 BIOS ROM P/N: M31-25L6482-M24. 20171207
Q6
NN-BSS138DW-7-F_SOT363-6-RH
D03-138DW19-D07
SOT_363
選Dual 體積比較小
Vgs(th) = 1 ~ 2V
ID = 0.12A
EC_RTC_RST
R5072 100KR1%0402
Change RX1 name to R5072. 20171016
D2 S-BAT54C_SOT23 D01-BAT54C9-D07 SOT23_3P_U1
D1 S-BAS40WS_SOD323-RH D01-BAS4000-P15 DIODE_SOD323
+RTC_D
+RTC_R
R58 1KR1%0402
+RTCVCC
C57 C1u25X5-HF
BAT1 BCR1220H2 D06-0105701-K26
Change BAT1 P/N from D06-0104701-K26 to D06-0105701-K26. 20171016
+RTC
CON1 BH1X2#S-1.25PITCH_BLACK-HF
N32-10200Q0-A81
SD_53261_0210_2P
Mirror CON1 vertical for Cable. 20171017
紅(+)1，黑(-)2
滿足线长要求的情况下
绞线2-3圈
Q1
NN-BSS138DW-7-F_SOT363-6-RH
D03-138DW19-D07
SOT_363
SMBCLK_DIMM_Q R51 2.2KR1%0402
SMBDATA_DIMM_Q R52 2.2KR1%0402
SMBCLK_DIMM_TP EC72 X_C100p50N0402
SMBDATA_DIMM_TP EC73 X_C100p50N0402
SMBCLK_DIMM_Q R298 0R1%0402 SMBCLK_DIMM_TP
SMBDATA_DIMM_Q R297 0R1%0402 SMBDATA_DIMM_TP
C56 C0.1u25X50402-HF
+5VRUN
Change Q1.G power from +3VRUN to +5VRUN. 20171016
MICRO-STAR INT'L CO.,LTD.
Title
Kabylake-R (RTC,LPC,CLK,SPI)
Size C
Document Number MS-14B1
Rev 0C
Date: Thursday, December 21, 2017
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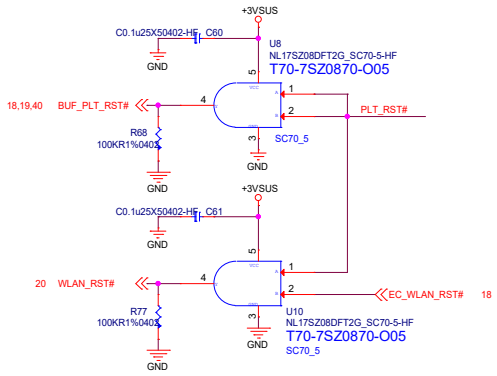
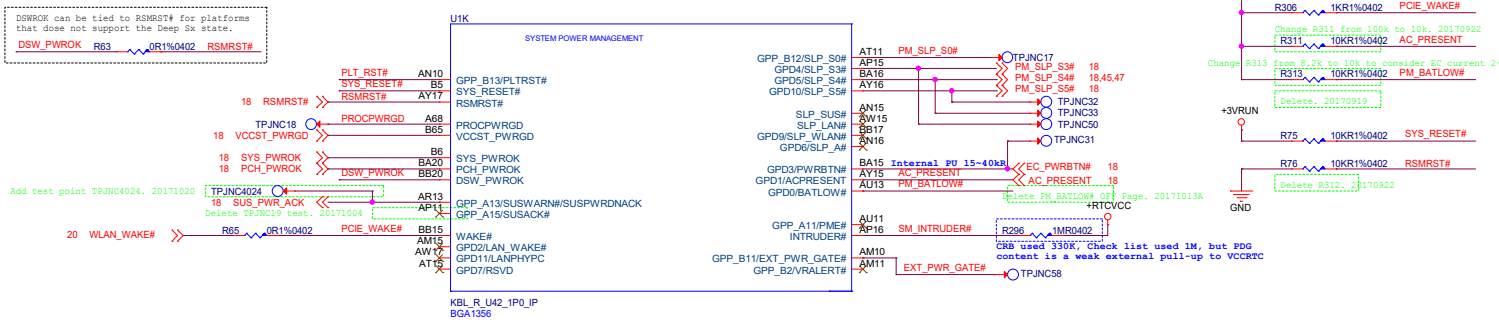
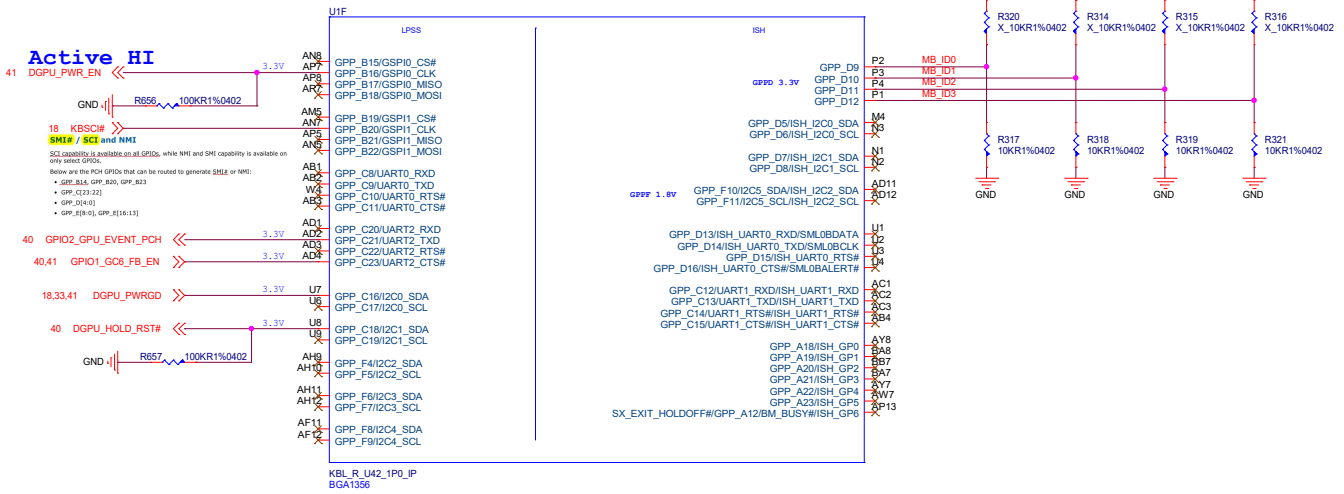




Signal	GPIO Assignment
DGPU_PWR_EN	GPP_B16
DGPU_PWROK	GPP_C16
DGPU_HOLD_RST#	GPP_C18



MICRO-STAR INT'L CO.,LTD.

Title: Kabylake-R (LPSS,ISH,I2C)

Size: Custom | Document Number: MS-14B1 | Rev: 0C

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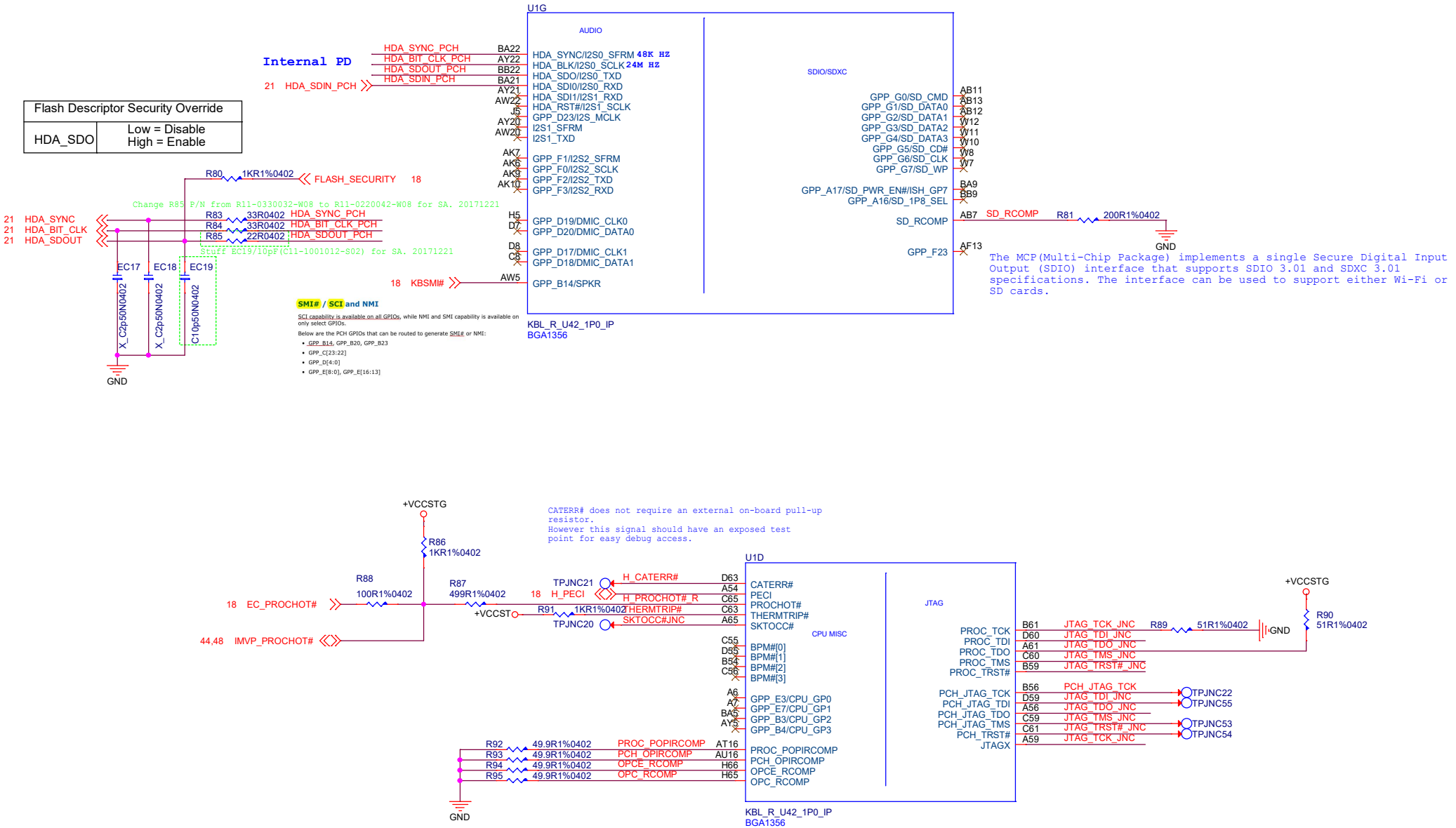
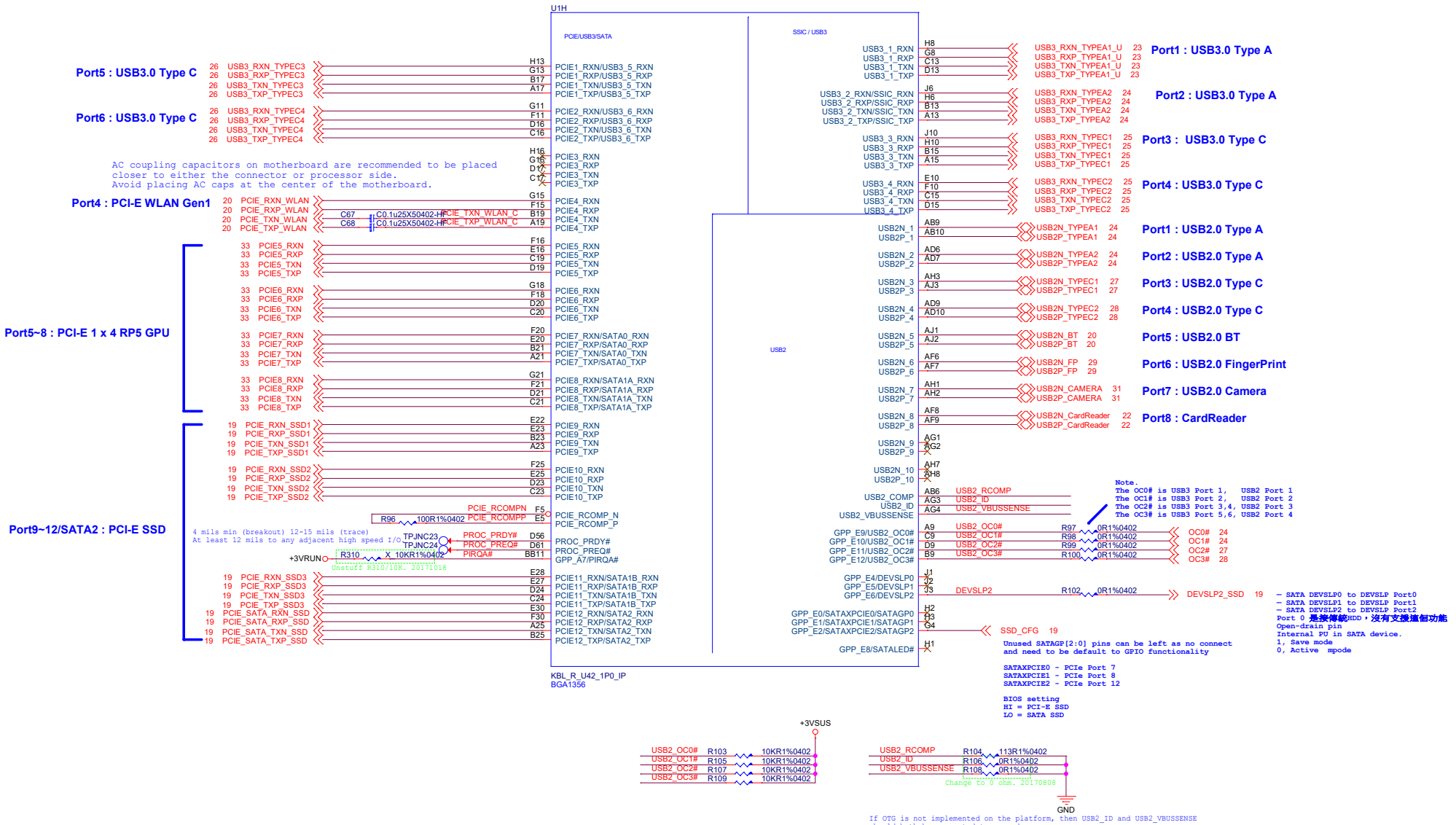


msi MICRO-STAR INT'L CO.,LTD.			
Title: Kabylake-R (HDA,MISC,JTAG)			
Size: Custom	Document Number: MS-14B1		Rev: 0C
Date: Thursday, December 21, 2017	Sheet 9 of 57		



Title	Kabylake-R (PCIE,SATA,USB)
Size / Custom	Document Number: MS-14B1
Rev	0C
Date:	Thursday, December 21, 2017
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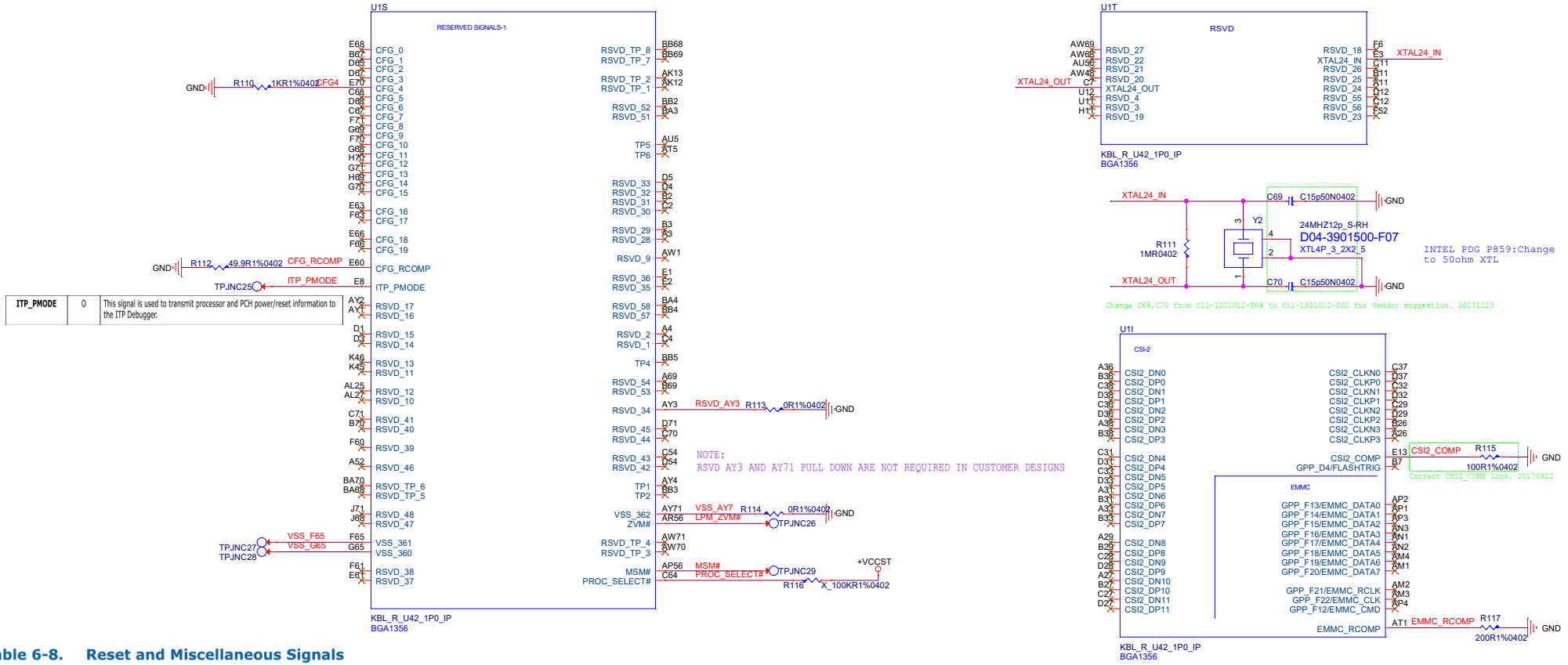
MICRO-STAR INT'L CO.,LTD.



ITP_PMODE	0	This signal is used to transmit processor and PCH power/reset information to the ITP Debugger.

Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I	GTL	SE	All Processor Lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-Processor Line only and test point may be placed on the board for them.

PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for the processor.

RSVD		All the RSVD pins should be left unconnected (floating) on the board.

Name	Type	Description
CSI2_DP[11:0] CSI2_DN[11:0]	I	MIPI CSI-2 Data
CSI2_CLKP[3:0] CSI2_CLKN[3:0]	I	MIPI CSI-2 Clock
CSI2_COMP	I	External Reference (100 Ohm+/- 1% pull down to ground)

Name	Type	Description
EMMC_CMD	I/O	eMMC Command/Response
EMMC_DATA0	I/O	eMMC Data
EMMC_DATA1	I/O	eMMC Data
EMMC_DATA2	I/O	eMMC Data
EMMC_DATA3	I/O	eMMC Data
EMMC_DATA4	I/O	eMMC Data
EMMC_DATA5	I/O	eMMC Data
EMMC_DATA6	I/O	eMMC Data
EMMC_DATA7	I/O	eMMC Data
EMMC_RCLK	I	eMMC Receive Clock
EMMC_CLK	O	eMMC Clock
EMMC_RCOMP	I/O	External reference (200 Ohm+/- 1% pull down to ground)

MICRO-STAR INT'L CO.,LTD.

Title: Kabylake-R (CFG,CSI,RSVD)

Size: Custom | Document Number: MS-14B1 | Rev: 0C

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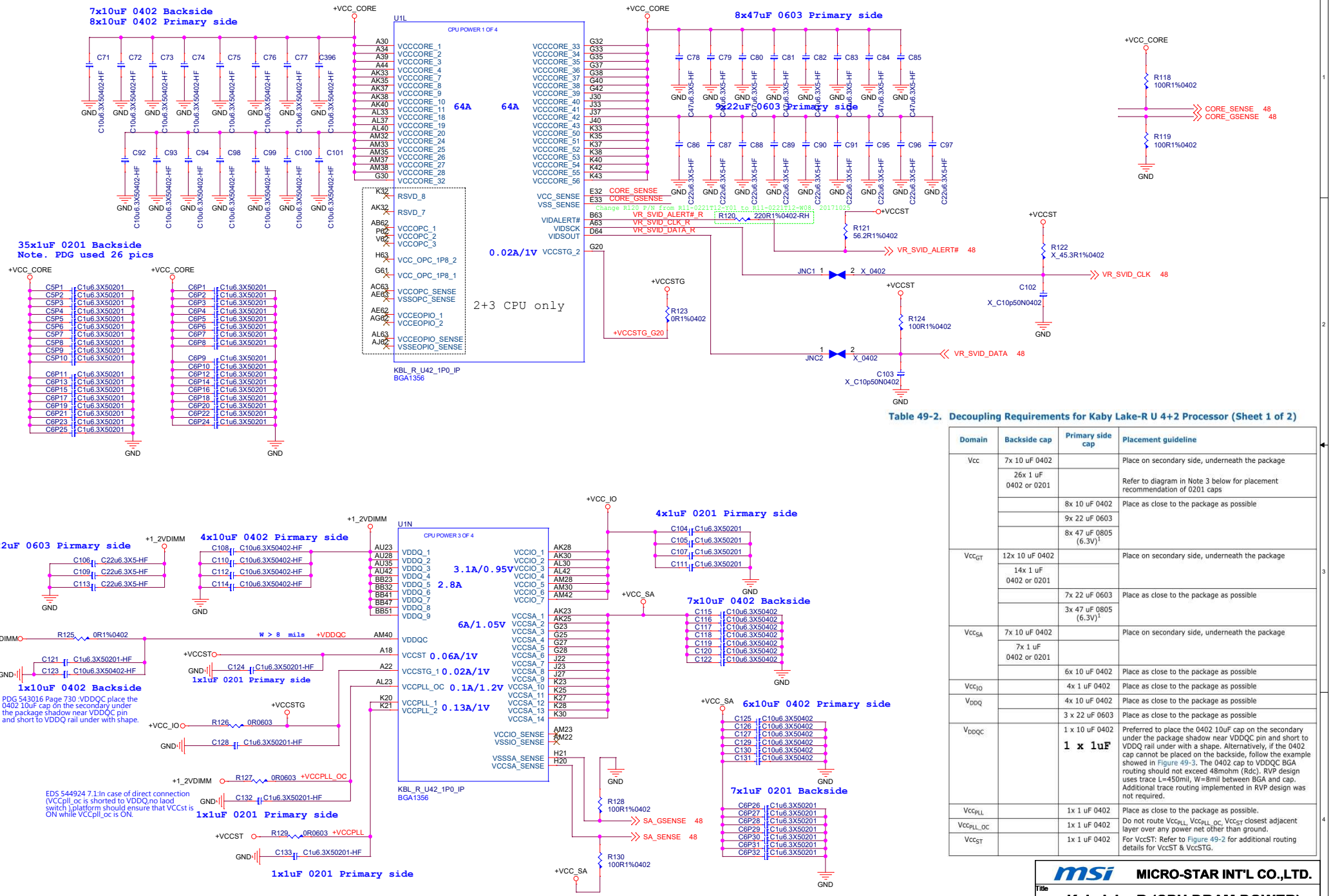

Table 49-2. Decoupling Requirements for Kaby Lake-R U 4+2 Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	26x 1 uF 0402 or 0201		Refer to diagram in Note 3 below for placement recommendation of 0201 caps
		8x 10 uF 0402	Place as close to the package as possible
		9x 22 uF 0603	
		8x 47 uF 0805 (6.3V)[1]	
Vcc_{GT}	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V)[1]	
Vcc_{SA}	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
Vcc_{IO}		4x 1 uF 0402	Place as close to the package as possible
V_{DDQ}		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible
V_{DDQC}		1 x 10 uF 0402 **1 x 1uF**	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 49-3. The 0402 cap to VDDQC BGA routing should not exceed 48mohm (Rdc). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
Vcc_{PLL}		1x 1 uF 0402	Place as close to the package as possible.
Vcc_{PLL_OC}		1x 1 uF 0402	Do not route Vcc_{PLL}, Vcc_{PLL_OC}, Vcc_{ST} closest adjacent layer over any power net other than ground.
Vcc_{ST}		1x 1 uF 0402	For VccST: Refer to Figure 49-2 for additional routing details for VccST & VccSTG.

MSI MICRO-STAR INT'L CO.,LTD.

Title: Kabylake-R (CPU DRAM POWER)

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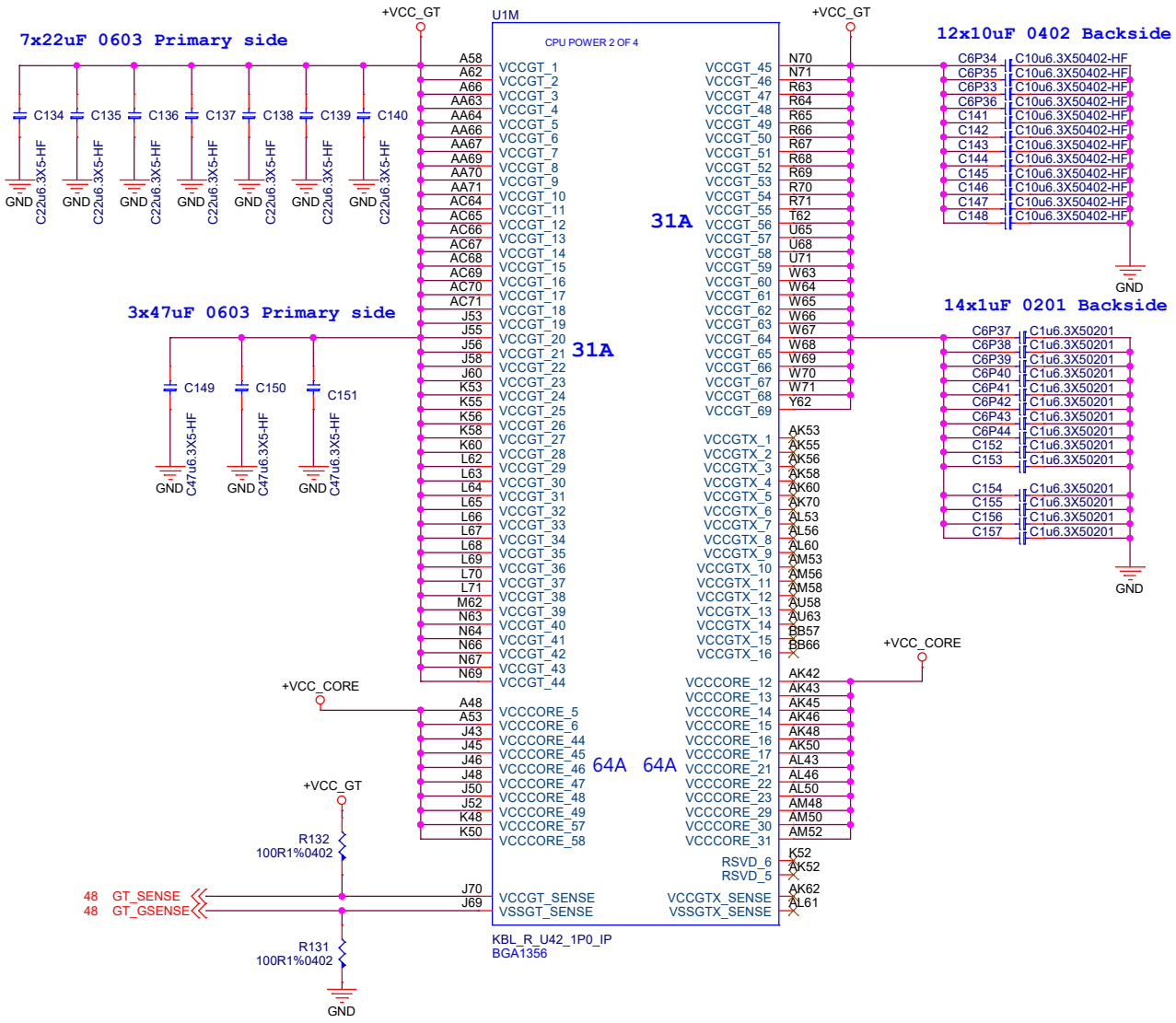

Table 49-2. Decoupling Requirements for Kaby Lake-R U 4+2 Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	26x 1 uF 0402 or 0201		Refer to diagram in Note 3 below for placement recommendation of 0201 caps
		8x 10 uF 0402	Place as close to the package as possible
		9x 22 uF 0603	
		8x 47 uF 0805 (6.3V)[1]	
Vcc_{GT}	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V)[1]	
Vcc_{SA}	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
Vcc_{IO}		4x 1 uF 0402	Place as close to the package as possible
V_{DDQ}		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible
V_{DDQC}		1 x 10 uF 0402 **1 x 1uF**	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 49-3. The 0402 cap to VDDQC BGA routing should not exceed 48mohm (Rdc). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
Vcc_{PLL}		1x 1 uF 0402	Place as close to the package as possible.
Vcc_{PLL_OC}		1x 1 uF 0402	Do not route Vcc_{PLL}, Vcc_{PLL_OC}, Vcc_{ST} closest adjacent layer over any power net other than ground.
Vcc_{ST}		1x 1 uF 0402	For VccST: Refer to Figure 49-2 for additional routing details for VccST & VccSTG.

MICRO-STAR INT'L CO.,LTD.

Title: Kabylake-R (GT POWER)

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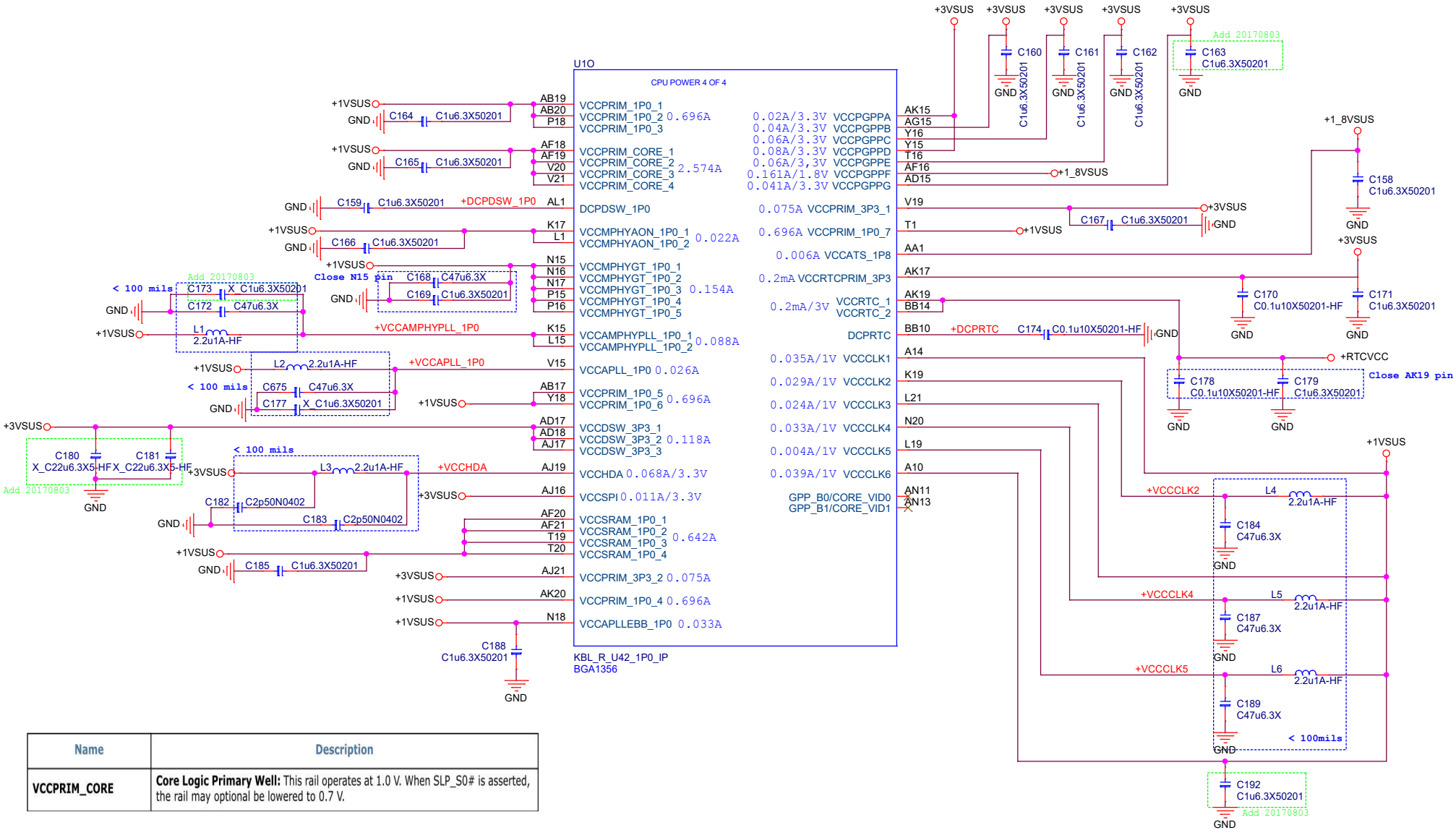

Name	Description
VCCPRIM_CORE	**Core Logic Primary Well:** This rail operates at 1.0 V. When SLP_S0# is asserted, the rail may optional be lowered to 0.7 V.

MSI MICRO-STAR INT'L CO.,LTD.

Title: Kabylake-R (PCH POWER)

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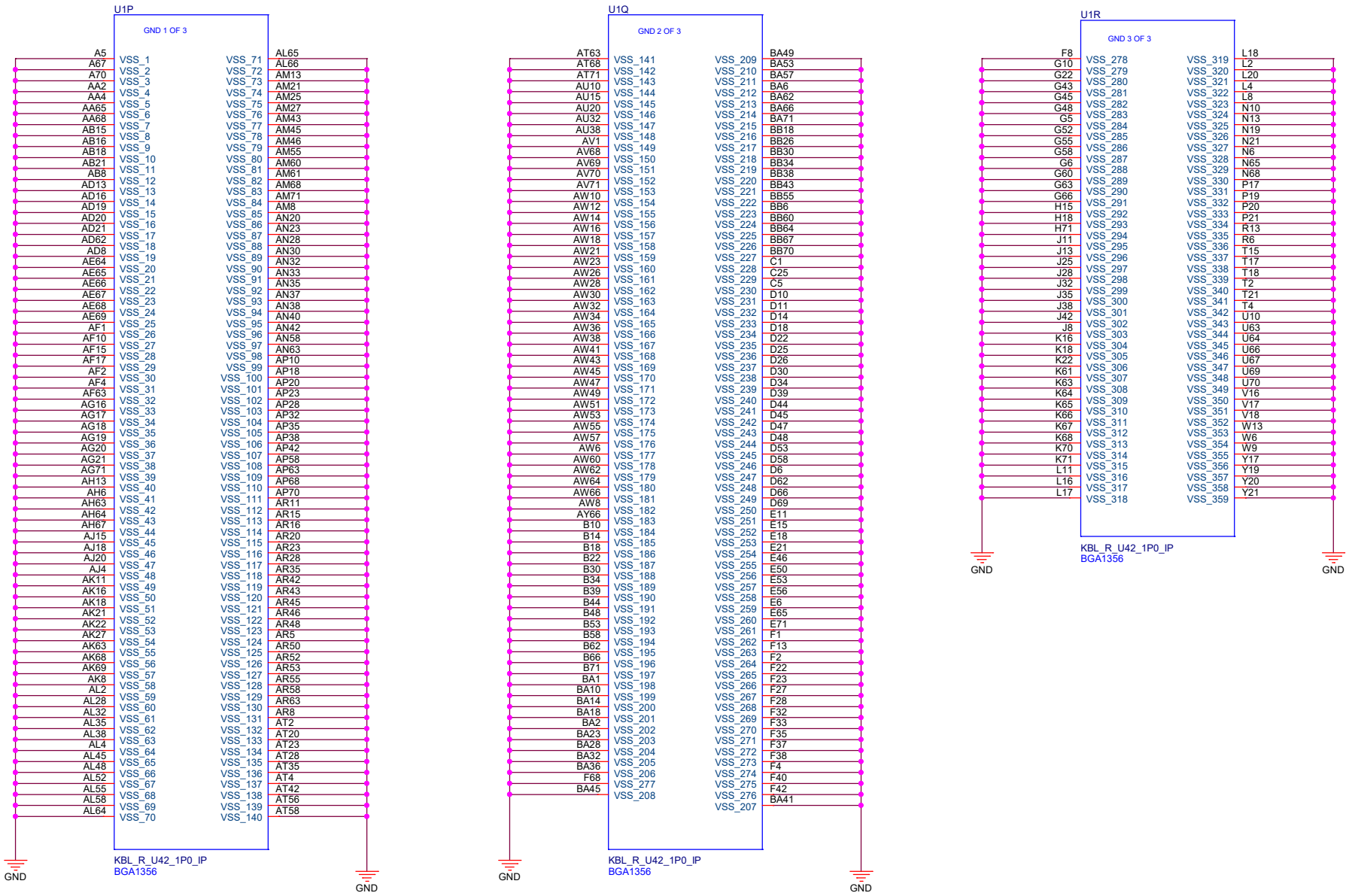

MICRO-STAR INT'L CO.,LTD.

Title: Kabylake-R (GND)

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CON2
FPC40P-0.5PITCH_NATURAL-HF
N5A-40F0180-A81
FPC_S40_10

Check cable arrange with ME

eDP

< 750 mills

3 EDP_TX1_DN	C193	C0.1u25X50402-HF	EDP_TX1_DN_C
3 EDP_TX1_DP	C194	C0.1u25X50402-HF	EDP_TX1_DP_C
3 EDP_TX0_DN	C195	C0.1u25X50402-HF	EDP_TX0_DN_C
3 EDP_TX0_DP	C196	C0.1u25X50402-HF	EDP_TX0_DP_C
3 EDP_AUX_DP	C197	C0.1u25X50402-HF	EDP_AUX_DP_C
3 EDP_AUX_DN	C198	C0.1u25X50402-HF	EDP_AUX_DN_C

1.5A
+3V_LCD

3 EDP_HPD

Change LVDS_BKLTCTL_R net name to EDP_BKLTCTL_R. 20170925

18 EC_BL-ON
3 EDP_BKLTCTL
R136 0R1%0402 EC_BL-ON_R
R137 0R1%0402 EDP_BKLTCTL_R
GND C200 X_C0.1u25X50402-HF

1.5A
+PWR_SRC
GND C204 C1u25X5

Camera move to Page. 31. 20171116

41 GND
42 GND

<Table 6. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	CABC_Enable	CABC (not enable)
2	H-GND	Ground
3	LAN1_N	Complement Signal Link _Lane1
4	LAN1_P	True Signal Link _Lane1
5	H-GND	Ground
6	LAN0_N	Complement Signal Link _Lane0
7	LAN0_P	True Signal Link _Lane0
8	H-GND	High Speed Ground
9	AUXP	True Signal Link _Auxiliry Channel
10	AUXN	Complement Signal Link _Auxiliry Channel
11	H-GND	Ground
12	LCD_VCC	Power Supply, 3.3V (typ.)
13	LCD_VCC	Power Supply, 3.3V (typ.)
14	BIST	Panel self test enable
15	H-GND	Ground
16	H-GND	Ground
17	HPD	HPD(Hot Plug Detect) Signal Pin
18	BL_GND	High Speed Ground
19	BL_GND	High Speed Ground
20	BL_GND	High Speed Ground
21	BL_GND	High Speed Ground
22	BL_EN	Backlight on/off Control pin
23	BL_PWM	Back light PWM Dimming
24	Hsnyc	Line synchronization
25	NC	No connection
26	BL_PWR	Backlight power
27	BL_PWR	Backlight power
28	BL_PWR	Backlight power
29	BL_PWR	Backlight power
30	NC	No connection

4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for LCD test)	
2	H_GND	High Speed Ground	
3	NC	No Connection (Reserved for ML1-)	
4	NC	No Connection (Reserved for ML1+)	
5	H_GND	High Speed Ground	
6	ML0-	Complement Signal-Lane 0	
7	ML0+	True Signal-Main Lane 0	
8	H_GND	High Speed Ground	
9	AUX+	True Signal-Auxiliary Channel	
10	AUX-	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply +3.3 V (typical)	
13	VCCS	Power Supply +3.3 V (typical)	
14	NC	No Connection (Reserved for INNOLUX test)	
15	GND	Ground	
16	GND	Ground	
17	HPD	Hot Plug Detect	
18	BL_GND	BL Ground	
19	BL_GND	BL Ground	
20	BL_GND	BL Ground	
21	BL_GND	BL Ground	
22	LED_EN	BL_Enable Signal of LED Converter	
23	LED_PWM	PWM Dimming Control Signal of LED Converter	
24	NC	No Connection (Reserved for Hsync signal)	
25	NC	No Connection (Reserved for INNOLUX test)	
26	LED_VCCS	BL Power	
27	LED_VCCS	BL Power	
28	LED_VCCS	BL Power	
29	LED_VCCS	BL Power	
30	NC	No Connection (Reserved for INNOLUX test)	

U16
APL3512ABI-TRG_SOT23-5-HF
I36-3512A09-A30
SOT23_5_NPC30X

+3VRUN
C199 C1u25X50402-HF
GND
C203 X_C0.1u25X50402-HF
GND
VIN VO GND SS EN
+3V_LCD_R
R323 0R0603
Max 2A
+3V_LCD
C201 C0.1u25X50402-HF
C202 C10u10X5-HF
GND
GND
EDP_VDDEN 3
R138 100KR1%0402
GND

EDP_TX1_DN_C
EDP_TX1_DP_C
EL2
ER2 X_100R1%0402
X_CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1

EDP_TX0_DN_C
EDP_TX0_DP_C
EL1
ER1 X_100R1%0402
X_CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1

EDP_AUX_DN_C
EDP_AUX_DP_C
EL3
ER3 X_100R1%0402
X_CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1

MICRO-STAR INT'L CO.,LTD.

Title: eDP Pannel

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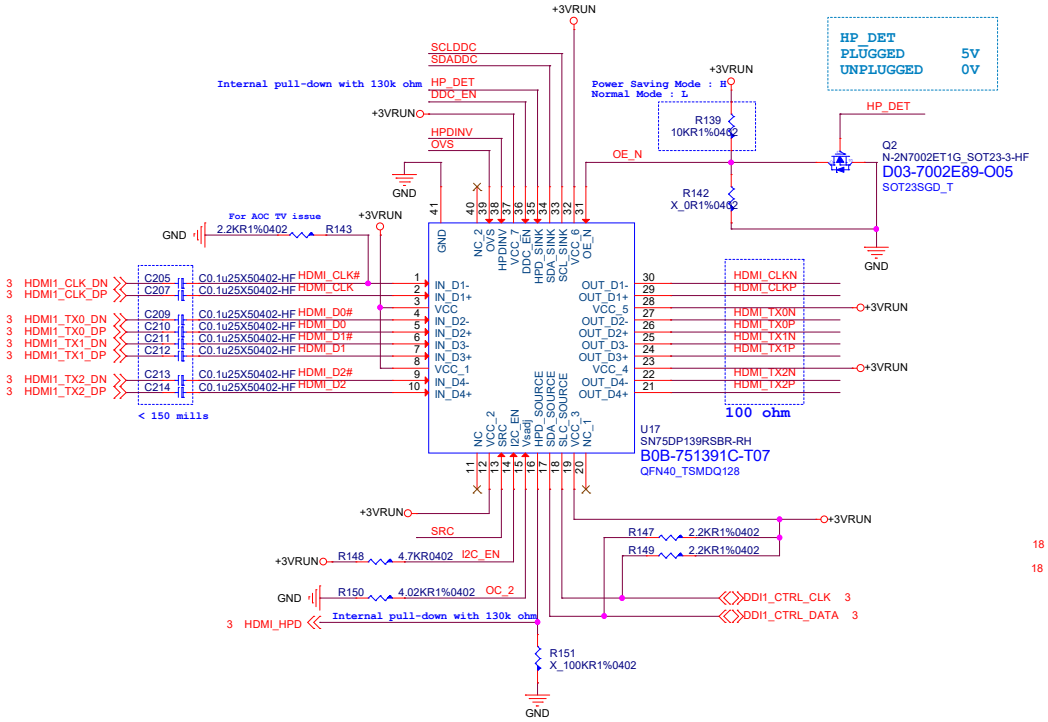
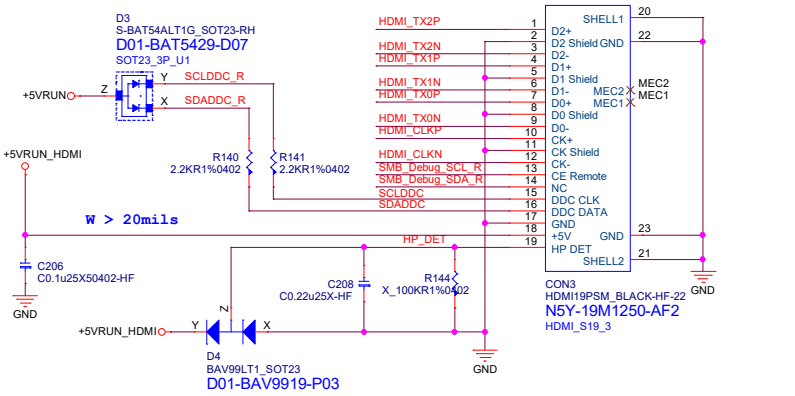
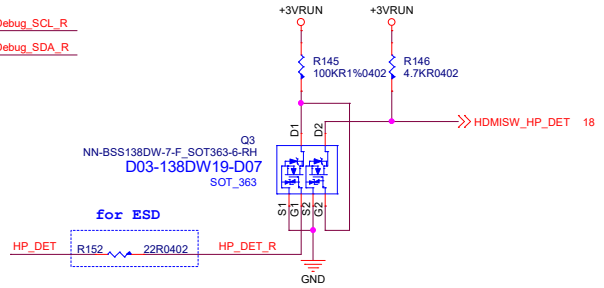
HDMI Level Shifter

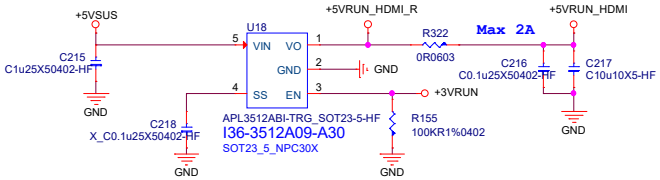


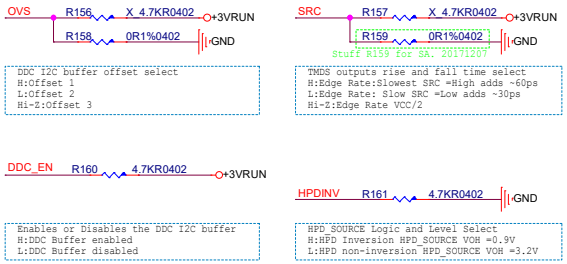
HDMI Connector

Change CON3 P/N from N5Y-19M0910-AF2 to N5Y-19M1250-AF2 for ME. 20171102A

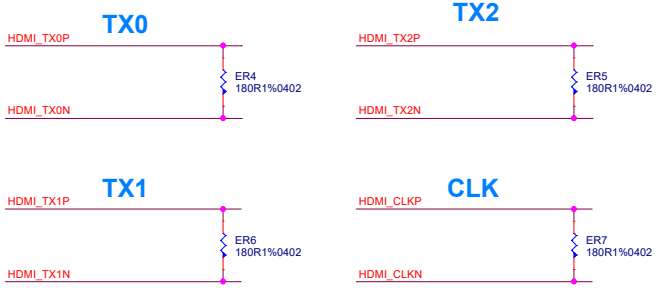


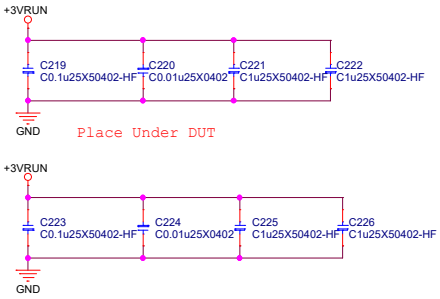






EMI Close Connector





Delete EL4~7(L12-9008100-I05) for Layout. 20171024A

MICRO-STAR INT'L CO.,LTD.

Title: HDMI Level Shifter_SN75DP139

Size: Custom | Document Number: MS-14B1 | Rev: 0C

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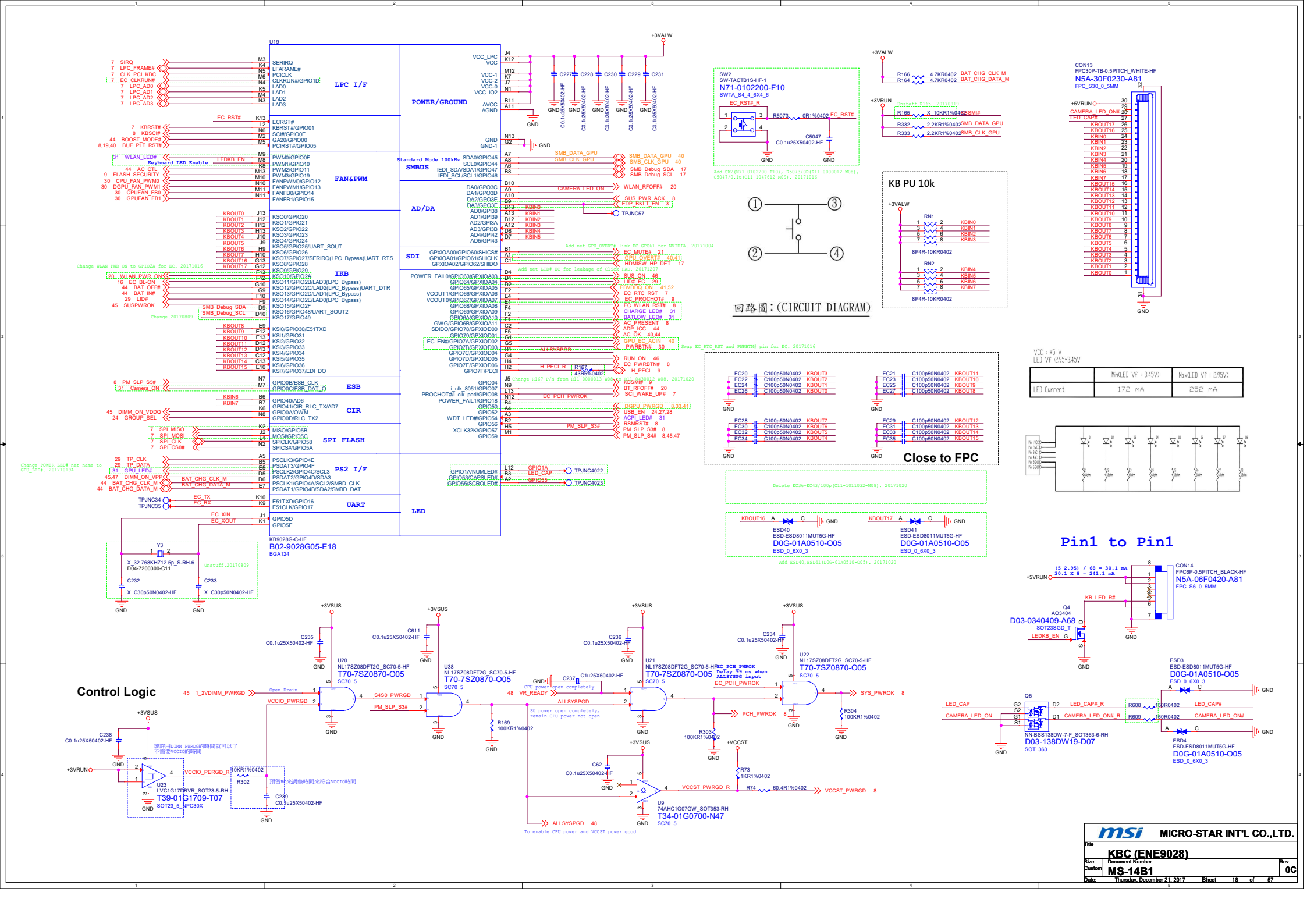
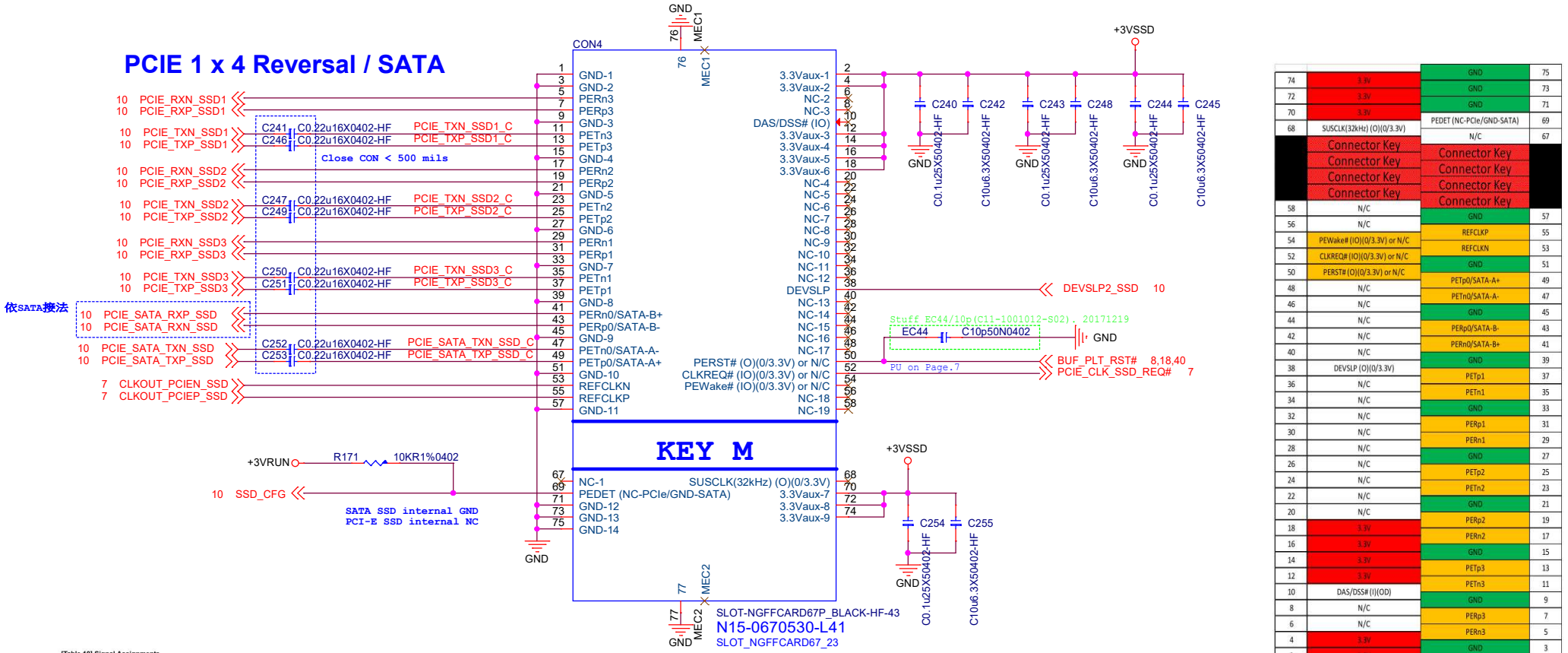

U19
LPC I/F
POWER/GROUND
FAN&PWM
SMBUS
AD/DA
SDI
IKB
ESB
CIR
SPI FLASH
PS2 I/F
UART
LED
KB9028G-C-HF
B02-9028G05-E18
BGA124
回路圖:(CIRCUIT DIAGRAM)
KB PU 10k
Close to FPC
Pin1 to Pin1
Control Logic
MICRO-STAR INT'L CO.,LTD.
KBC (ENE9028)
MS-14B1
Thursday, December 21, 2017

PCIE 1 x 4 Reversal / SATA



74	3.3V		GND	75
72	3.3V		GND	73
70	3.3V		GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)		PEDET (NC-PCIe/GND-SATA)	69
	Connector Key		N/C	67
	Connector Key		Connector Key	
	Connector Key		Connector Key	
	Connector Key		Connector Key	
	Connector Key		Connector Key	
58	N/C		GND	57
56	N/C		REFCLKP	55
54	PEWake# (IO)(0/3.3V) or N/C		REFCLKN	53
52	CLKREQ# (IO)(0/3.3V) or N/C		GND	51
50	PERST# (O)(0/3.3V) or N/C		PETp0/SATA-A+	49
48	N/C		PETn0/SATA-A-	47
46	N/C		GND	45
44	N/C		PERp0/SATA-B-	43
42	N/C		PERn0/SATA-B+	41
40	N/C		GND	39
38	DEVSLP (O)(0/3.3V)		PETp1	37
36	N/C		PETn1	35
34	N/C		GND	33
32	N/C		PERp1	31
30	N/C		PERn1	29
28	N/C		GND	27
26	N/C		PETp2	25
24	N/C		PETn2	23
22	N/C		GND	21
20	N/C		PERp2	19
18	3.3V		PERn2	17
16	3.3V		GND	15
14	3.3V		PETp3	13
12	3.3V		PETn3	11
10	DAS/DSS# (I)(OD)		GND	9
8	N/C		PERp3	7
6	N/C		PERn3	5
4	3.3V		GND	3
2	3.3V		GND	1

[Table 10] Signal Assignments

Pin#	Assignment	Description	Pin#	Assignment	Description
1	GND	Return current path	2	3.3V	3.3V source
3	GND	Return current path	4	3.3V	3.3V source
5	PETn3	PCIe TX	6	N/C	N/C
7	PETp3	PCIe TX	8	N/C	N/C
9	GND	Return current path	10	LED1#[1)]	Device Active Signal (Refer to [Table 11])
11	PERn3	PCIe Rx	12	3.3V	3.3V source
13	PERp3	PCIe Rx	14	3.3V	3.3V source
15	GND	Return current path	16	3.3V	3.3V source
17	PETn2	PCIe TX	18	3.3V	3.3V source
19	PETp2	PCIe TX	20	N/C	N/C
21	GND	Return current path	22	N/C	N/C
23	PERn2	PCIe Rx	24	N/C	N/C
25	PERp2	PCIe Rx	26	N/C	N/C
27	GND	Return current path	28	N/C	N/C
29	PETn1	PCIe TX	30	N/C	N/C
31	PETp1	PCIe TX	32	N/C	N/C
33	GND	Return current path	34	N/C	N/C
35	PERn1	PCIe Rx	36	N/C	N/C
37	PERp1	PCIe Rx	38	N/C	N/C
39	GND	Return current path	40	N/C	N/C
41	PETn0	PCIe TX	42	N/C	N/C
43	PETp0	PCIe TX	44	N/C	N/C
45	GND	Return current path	46	N/C	N/C
47	PERn0	PCIe Rx	48	N/C	N/C
49	PERp0	PCIe Rx	50	PERST#	PCIe Reset
51	GND	Return current path	52	CLKREQ#	PCIe Device Clock Request
53	REFCLKN	PCIe Reference Clock	54	PEWake#	N/C
55	REFCLKP	PCIe Reference Clock	56	Reserved for MFG_Data	N/C
57	GND	Return current path	58	Reserved for MFG_CLOCK	N/C
67	N/C	N/C	68	SUSCLK	N/C
69	PEDET	N/C	70	3.3V	3.3V source
71	GND	Return current path	72	3.3V	3.3V source
73	GND	Return current path	74	3.3V	3.3V source
75	GND	Return current path			

PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1 PERp2, PERn2/ PETp2, PETn2 PERp3, PERn3/ PETp3, PETn3	I/O	PCIe TX/RX Differential signals defined by the PCIe 3.0 specification	
	REFCLK+/ REFCLK-	I	PCIe Reference Clock signals (100 MHz) defined by the PCIe 3.0 specification	
	PERST#	O	PE-Reset is a functional reset to the card as defined by the PCIe Mini Card CEM specification	3.3V
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the PCIe Mini Card CEM specification; Also used by L1 PM Substates	3.3V
	WAKE#/OBFF	I/O	PCIe PME Wake. Open Drain with pull up on platform; Active Low	3.3V

+3VRUN — R5035 0R0603 — +3VSSD

Add R5035/0R and +3VSSD. 20170926

SSD STAND OFF

Spacer Support

UME29
E2B-16K1010-RH
E2B-16K1010-A89
H_R201D118_PT_N

GND

Add UME29 P/N:E2B-16K1010-A89 Footprint:H_R201D118_PT for ME.20171014
Change UME29 footprint to H_R201D118_PT_N for Layout. 20171030

MICRO-STAR INT'L CO.,LTD.

Title: M.2 KEY-M Combo SSD

Size: Custom | Document Number: MS-14B1 | Rev: 0C

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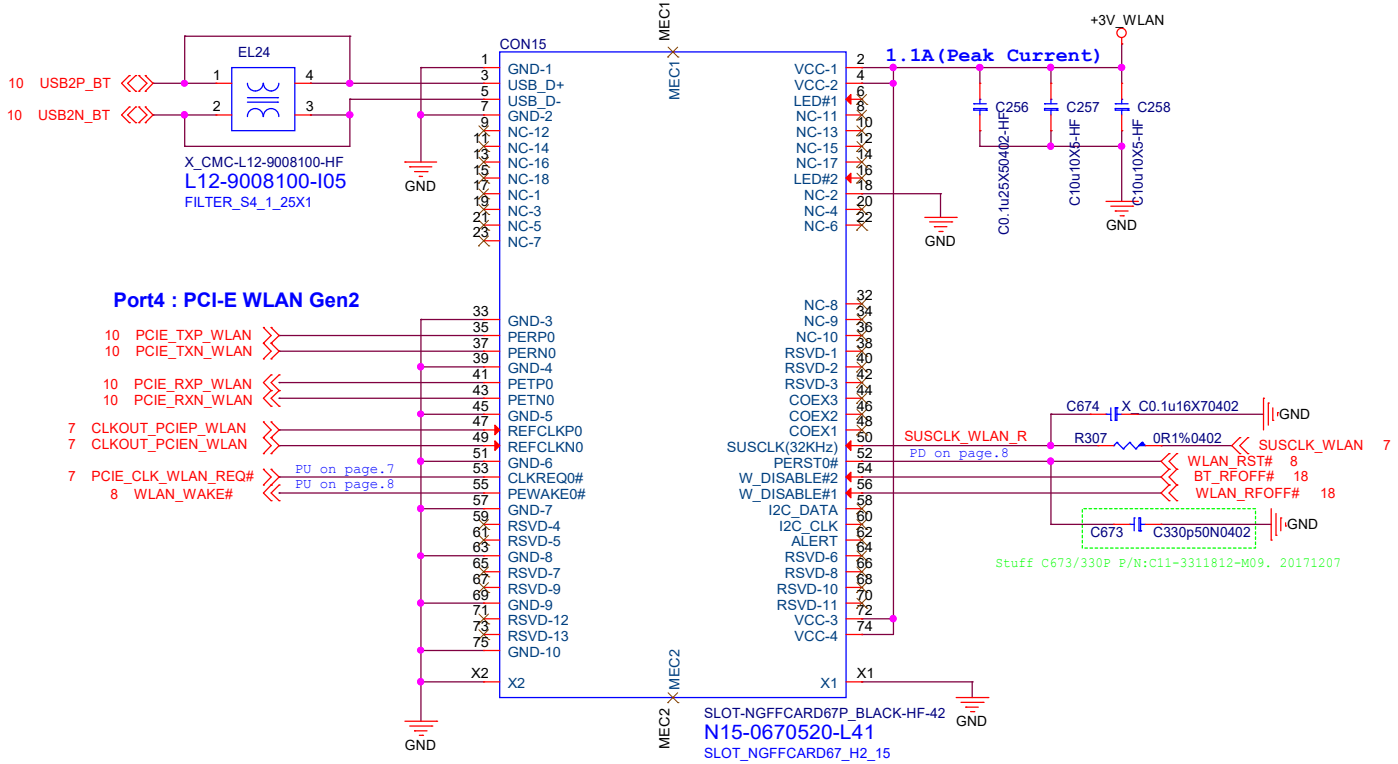
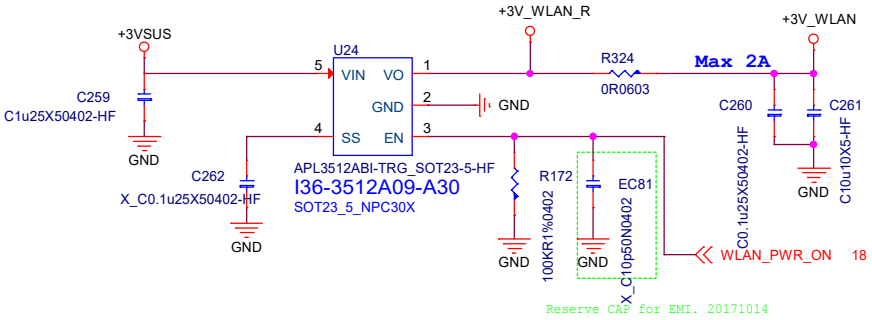


(Mechanical Key E) On Platform

Pin	Signal	Signal	Pin
74	3.3 V	GND	
72	3.3 V	RESERVED/REFCLKn1	73
70	UIM_POWER_SRC/GPIO_1/PEWAKE1#	RESERVED/REFCLKp1	71
68	UIM_POWER_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	RESERVED/PERn1	67
64	RESERVED	RESERVED/PERp1	65
62	ALERT# (I)(0/1.8 V)	GND	63
60	I2C_CLK (O)(0/1.8 V)	RESERVED/PETn1	61
58	I2C_DATA (I/O)(0/1.8 V)	RESERVED/PETp1	59
56	W_DISABLE1# (O)(0/3.3V)	GND	57
54	W_DISABLE2# (O)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX_TXD (O)(0/1.8V)	REFCLKn0	49
46	COEX_RXD (I)(0/1.8V)	REFCLKp0	47
44	COEX3 (I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O)(0/1.8V)	PETn0	37
34	UART CTS (I)(0/1.8V)	PETp0	35
32	UART TXD (O)(0/1.8V)	GND	33
	CONNECTOR KEY E	CONNECTOR KEY E	
	CONNECTOR KEY E	CONNECTOR KEY E	
	CONNECTOR KEY E	CONNECTOR KEY E	
	CONNECTOR KEY E	CONNECTOR KEY E	
	CONNECTOR KEY E	CONNECTOR KEY E	
22	UART RXD (I)(0/1.8V)	SDIO RESET#/TX_BLANKING (O)(0/1.8V)	23
20	UART WAKE# (I)(0/3.3V)	SDIO WAKE# (I)(0/1.8V)	21
18	GND	SDIO DATA3(I/O)(0/1.8V)	19
16	LED_2# (I)(OD)	SDIO DATA2(I/O)(0/1.8V)	17
14	PCM_OUT/I2S SD_OUT (O)(0/1.8V)	SDIO DATA1(I/O)(0/1.8V)	15
12	PCM_IN/I2S SD_IN (I)(0/1.8V)	SDIO DATA0(I/O)(0/1.8V)	13
10	PCM_SYNC/I2S WS (I/O)(0/1.8V)	SDIO CMD(I/O)(0/1.8V)	11
8	PCM_CLK/I2S SCK (I/O)(0/1.8V)	SDIO CLK/SYSCLK (O)(0/1.8V)	9
6	LED_1# (I)(OD)	GND	7
4	3.3 V	USB_D-	5
2	3.3 V	USB_D+	3
		GND	1

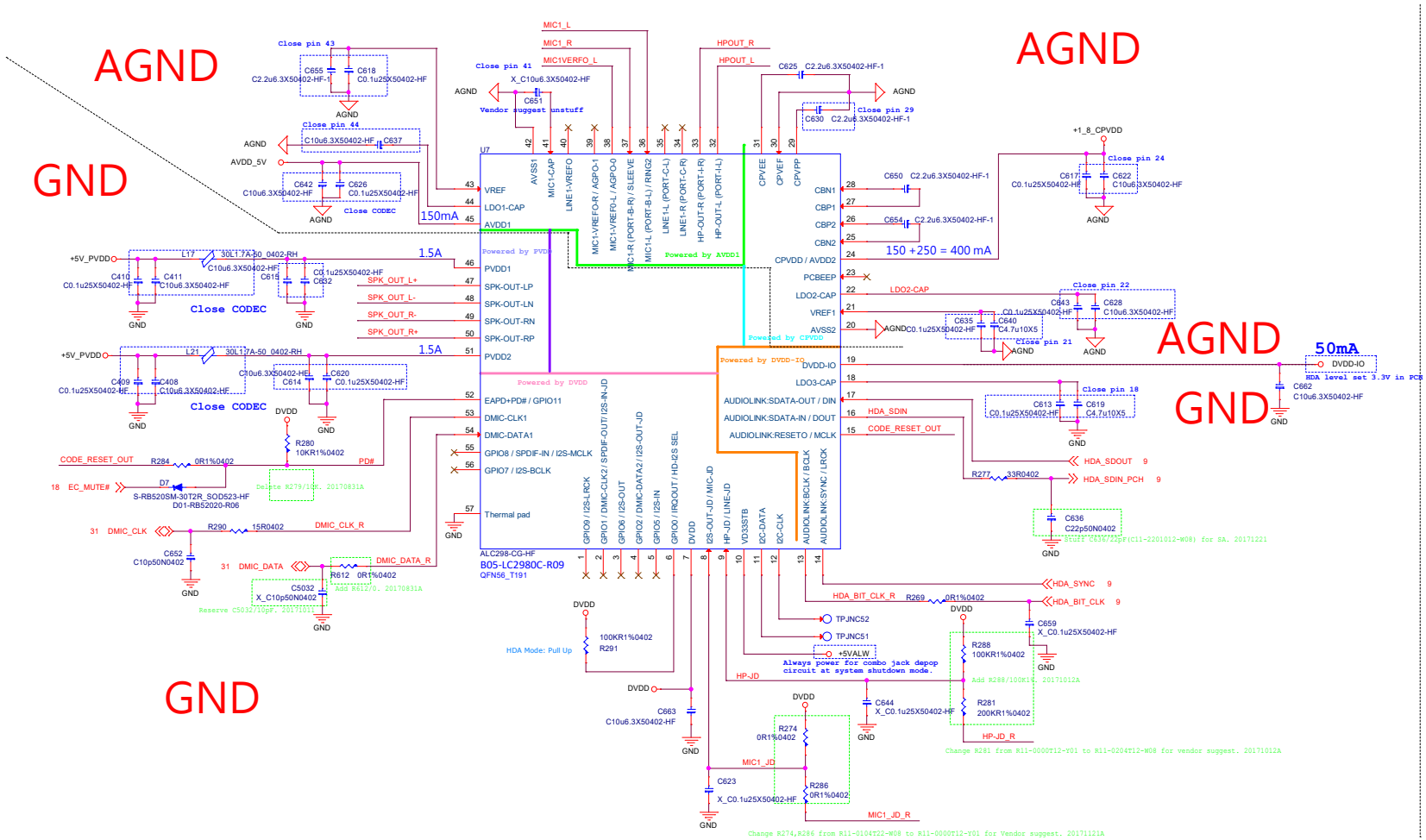


MICRO-STAR INT'L CO.,LTD.

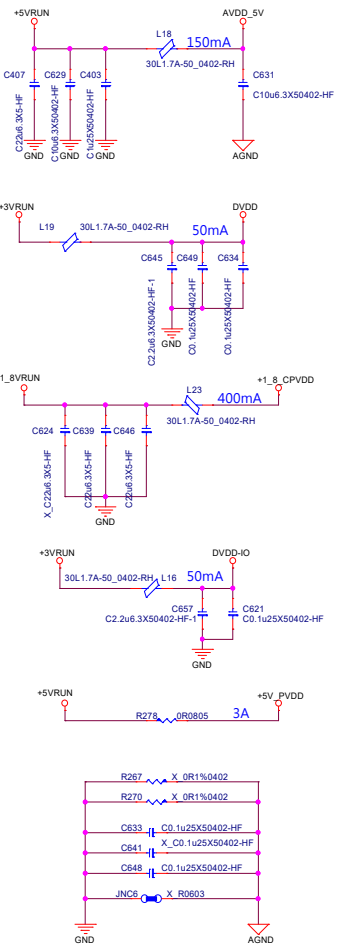
Title: M.2 KEY-E WLAM(9260)

Size	Document Number	Rev
Custom	MS-14B1	0C

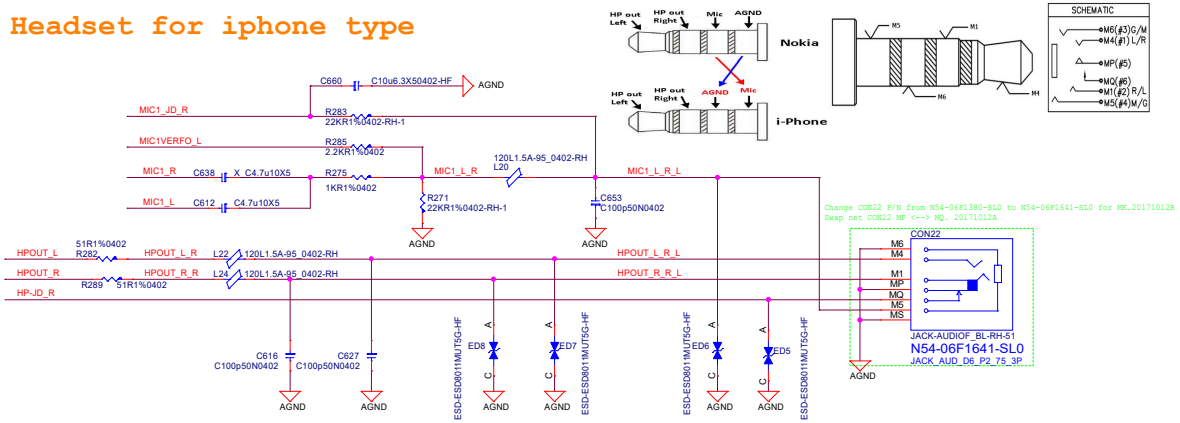
Date: Thursday, December 21, 2017 Sheet 20 of 57



POWER

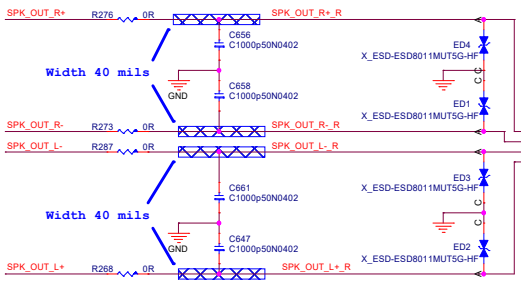


Headset for iphone type



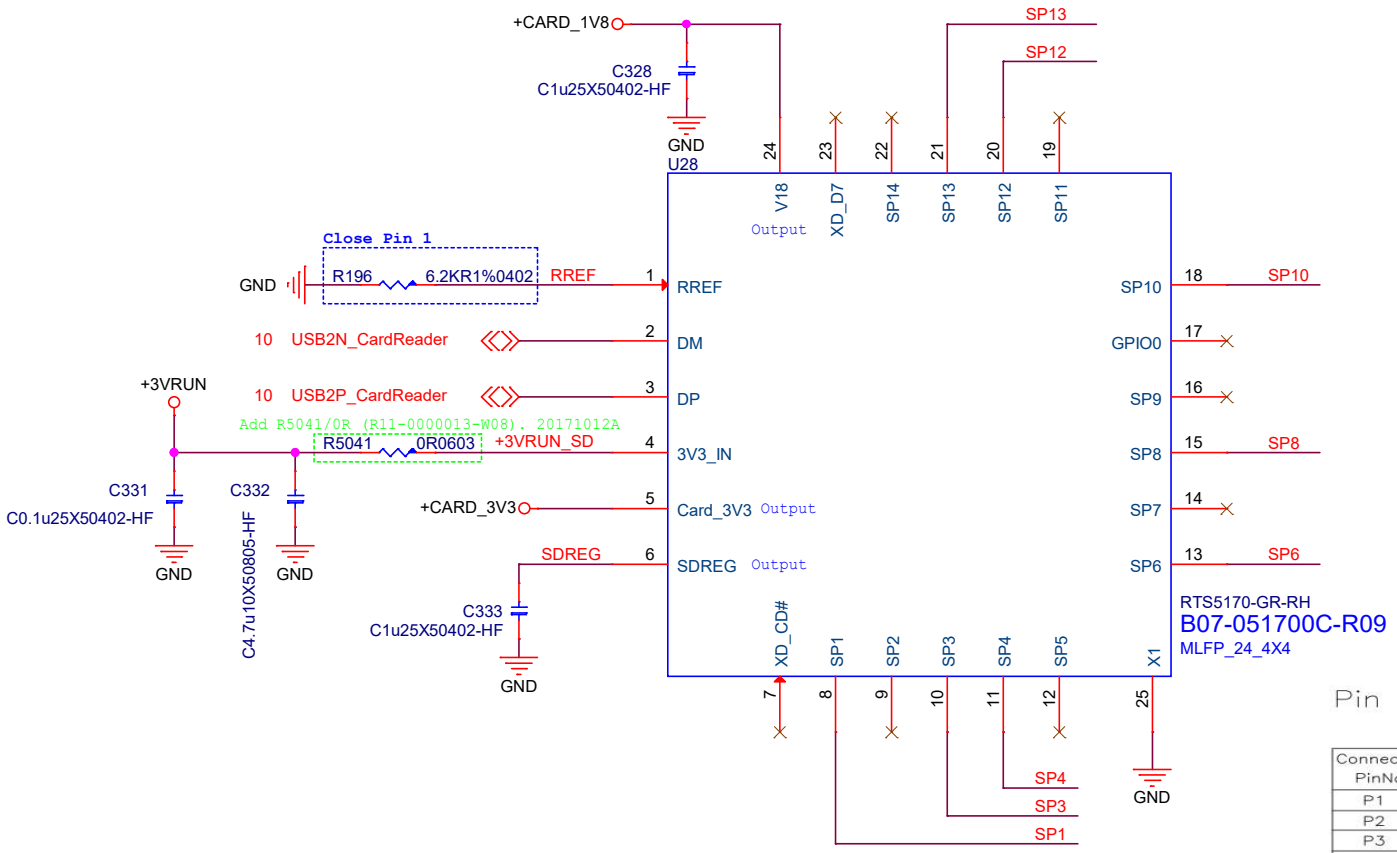
SPEAKER

1.SPK L+ L- R+ R- trace width: Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils
2.If you mount the LC filter((L1~L4;C4/C11;C2/C7/C10/C13),Please let them together and close to codec.
3.Please make the trace length/ Speaker wire length of SPKL+/L-/R+/R- be the same as possible as you can.
4.If L1,L2,L3,L4 are replaced by 0 ohm/1.6A resistetor(please don't use general bead, because it may influence the THD+N quality),and C4,C11 should be NC



Checking pin define

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	Audio (ALC298-CG), JACK		
Size: Custom	Document Number: MS-14B1		Rev: 0C
Date: Thursday, December 21, 2017	Sheet 21 of 57		



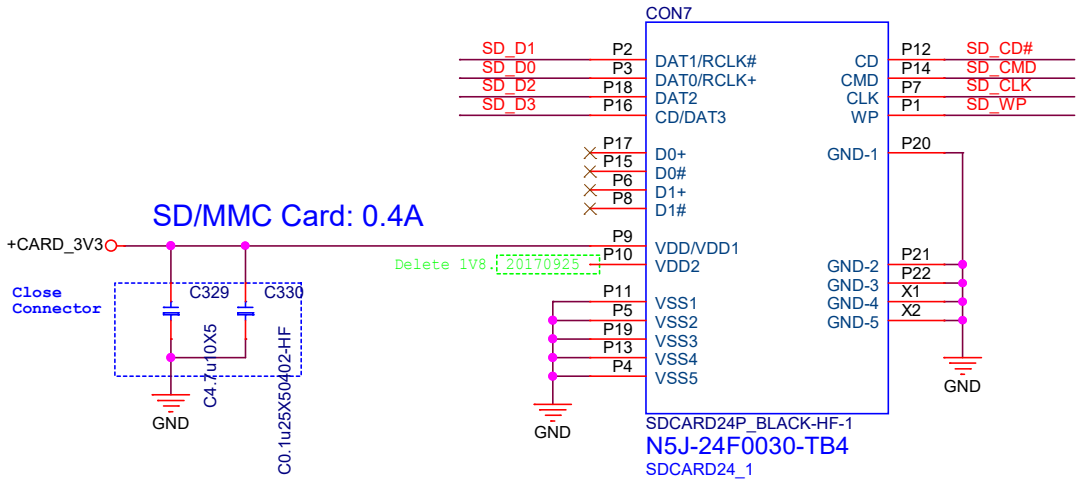
	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		

For EMI and Close to RTS5170

SP1	0R1%0402	R331	SD_WP	EC74	X_C10p50N0402
SP3	0R1%0402	R198	SD_D1	EC62	C15p50N0402
SP4	0R1%0402	R197	SD_D0	EC61	C15p50N0402
SP6	0R1%0402	R201	SD_CD#	EC65	X_C10p50N0402
SP8	0R1%0402	R203	SD_CLK	EC67	C15p50N0402
SP10	0R1%0402	R202	SD_CMD	EC66	X_C10p50N0402
SP12	0R1%0402	R200	SD_D3	EC64	C15p50N0402
SP13	0R1%0402	R199	SD_D2	EC63	C15p50N0402

Stuff EC61~64, EC67/15pF(C11-1501012-S02) for SA. 20171221

GND



Pin Define

Connector PinNo.	Specifications SD4.0 PinNo.	Specifications MMC PinNo.	SD Mode Name	Type	Description
P1			WP		
P2	P8		DAT1	I/O/PP	Data Line[Bit 1]
P3	P7	P7	DAT0	I/O/PP	Data Line[Bit 0]
P4	P17		—		Not Used(Connected to ground)
P5	P6	P6	VSS2	S	Supply voltage ground
P6	P16		—		Not Used
P7	P5	P5	CLK	I	Clock
P8	P15		—		Not Used
P9	P4	P4	VDD	S	Supply voltage
P10	P14		—		Not Used
P11	P3	P3	VSS1	S	Supply voltage ground
P12			CD		
P13	P13		—		Not Used(Connected to ground)
P14	P2	P2	CMD	PP	Command/Response
P15	P12		—		Not Used
P16	P1	P1	CD/DAT3	I/O/PP	Card Detect/ Data Line[Bit 3]
P17	P11		—		Not Used
P18	P9		DAT2	I/O/PP	Data Line[Bit 2]
P19	P10		—		Not Used(Connected to ground)
P20			GND		
P21			GND		
P22			GND		
P23			GND		
P24			GND		

MICRO-STAR INT'L CO.,LTD.

Title: **Card Reader (RTS5170)**

Size	Document Number	Rev
Custom	MS-14B1	0C

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USB3.0 TYPE-A Port 1 Redriver

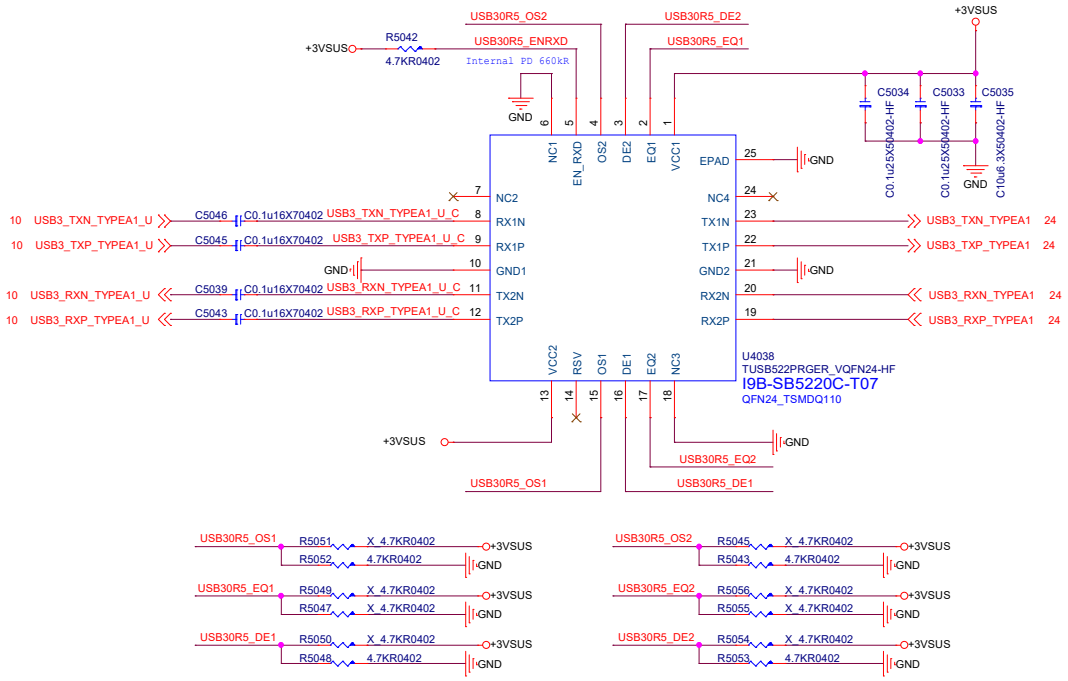


Table 4. TUSB522P OS Control Pin Settings

Pin	Description	Logic State	Transition Bit Output Differential Voltage (mV)
OS1/2	Output Swing	Low (Floating)	900
		High	1200

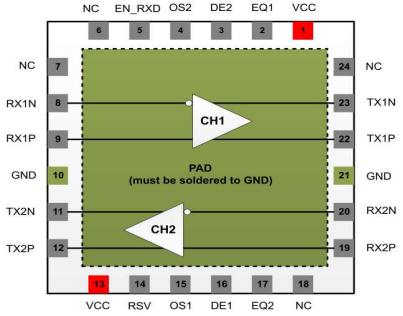
Table 6. TUSB522P De-Emphasis Control Pin Settings

Pin	Description	Logic State	De-Emphasis Ratio (dB)	
			OS = Low(Floating)	OS = High
DE1/2	De-Emphasis Amount	Low	0	–2.6
		Floating	–3.5	–5.9
		High	–6.2	–8.3

Table 2. TUSB522P Equalization Control Pin Settings

Pin	Description	Logic State	Gain (dB)
EQ1/EQ2	Equalization Amount	Low	3
		Floating	6
		High	9

RGE Package
24-Pin (VQFN)
Top View

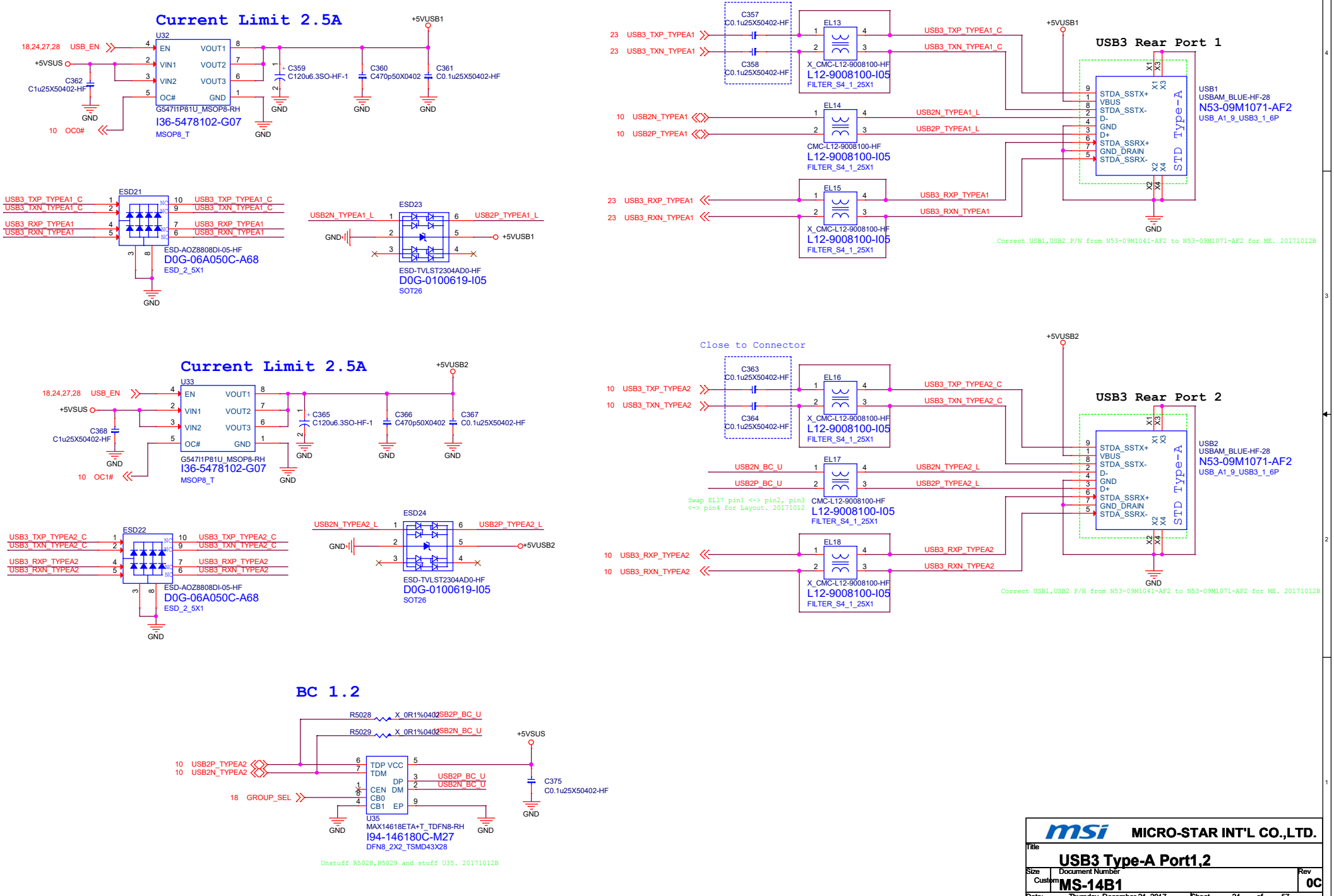


MICRO-STAR INT'L CO.,LTD.

Title: U3 Re-driver TYPE-A Port1,2

Size: Custom | Document Number: MS-14B1 | Rev: 0C

Date: Thursday, December 21, 2017 | Sheet 23 of 57



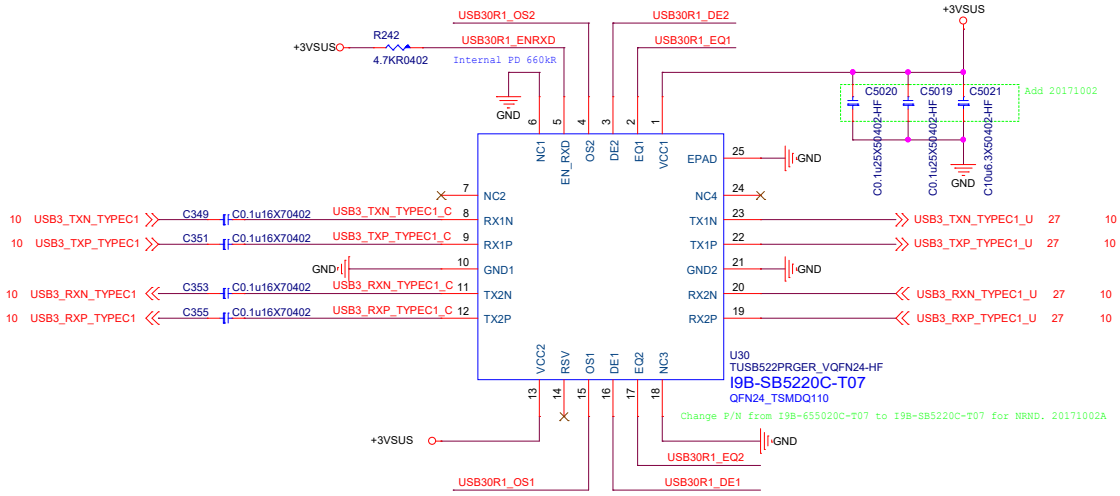
MICRO-STAR INT'L CO.,LTD.

Title: USB3 Type-A Port1,2

Size: Custom | Document Number: MS-14B1 | Rev: 0C

Date: Thursday, December 21, 2017 | Sheet 24 of 57

USB3.0 TYPE-C Port 3 Redriver TOP



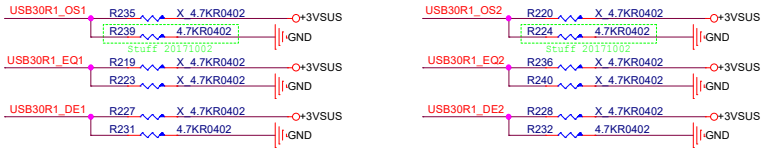


Table 4. TUSB522P OS Control Pin Settings

Pin	Description	Logic State	Transition Bit Output Differential Voltage (mV)
OS1/2	Output Swing	Low (Floating)	900
		High	1200

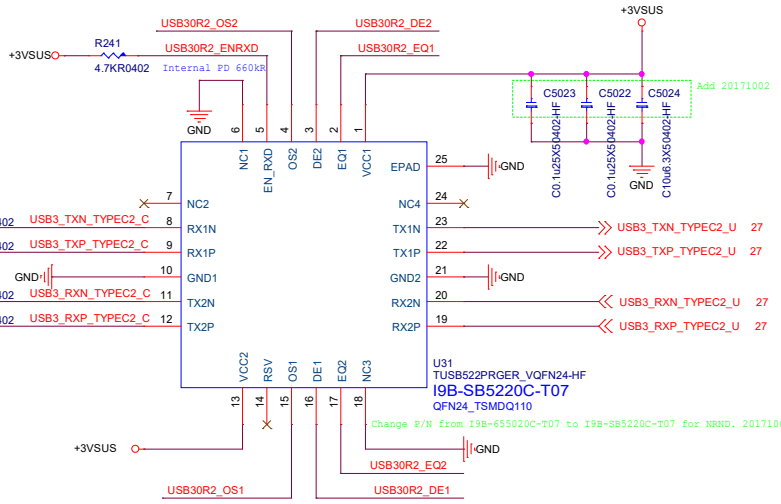
Table 2. TUSB522P Equalization Control Pin Settings

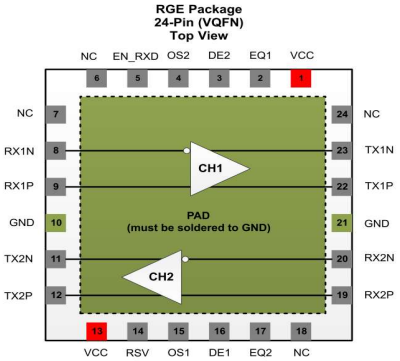
Pin	Description	Logic State	Gain (dB)
EQ1/EQ2	Equalization Amount	Low	3
		Floating	6
		High	9

Table 6. TUSB522P De-Emphasis Control Pin Settings

Pin	Description	Logic State	De-Emphasis Ratio (dB)	
			OS = Low(Floating)	OS = High
DE1/2	De-Emphasis Amount	Low	0	–2.6
		Floating	–3.5	–5.9
		High	–6.2	–8.3

USB3.0 TYPE-C Port 3 Redriver BOT





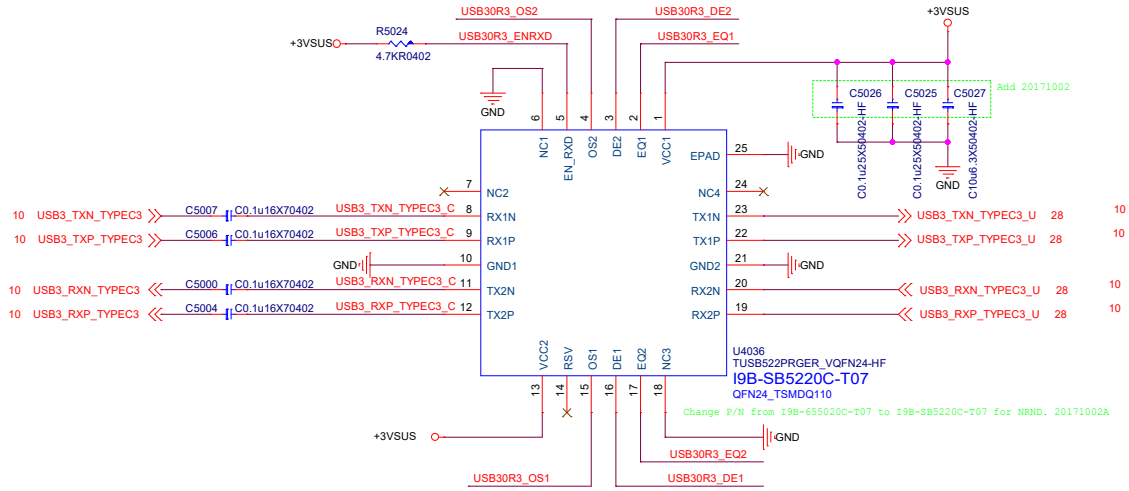
MICRO-STAR INT'L CO.,LTD.

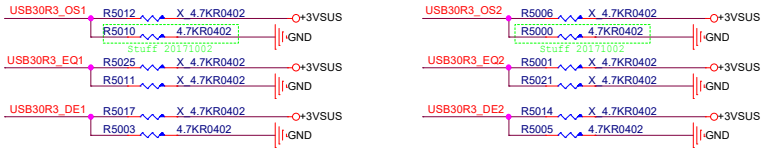
Title: U3 Re-driver TYPE-C Port3

Size: Custom | Document Number: MS-14B1 | Rev: 0C

Date: Thursday, December 21, 2017 | Sheet 25 of 57

USB3.0 TYPE-C Port 4 Redriver TOP





USB3.0 TYPE-C Port 4 Redriver BOT

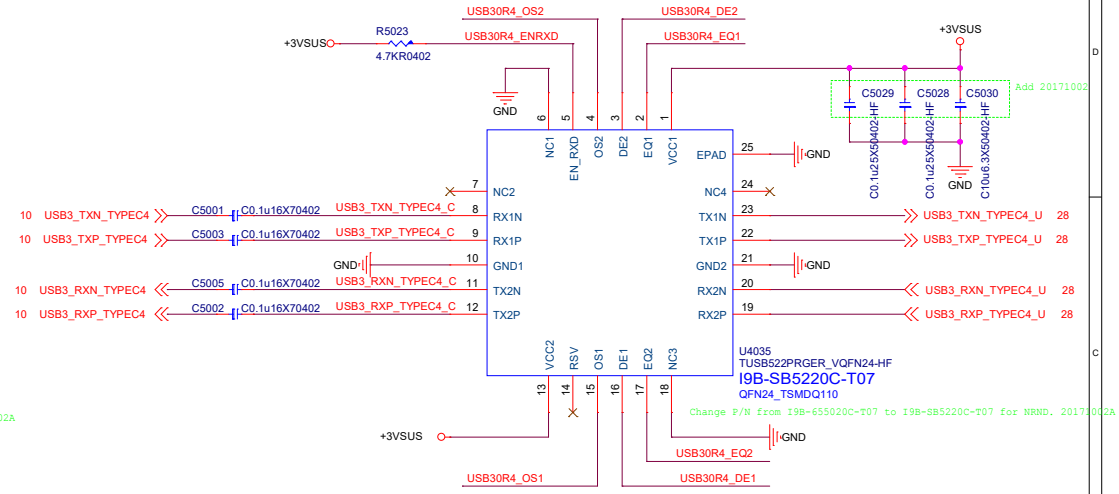


Table 4. TUSB522P OS Control Pin Settings

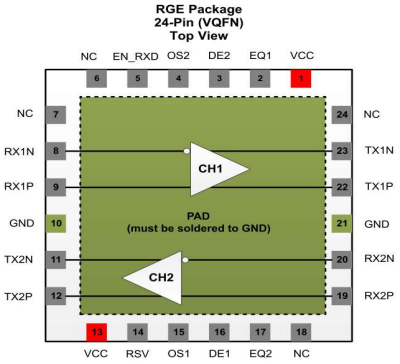
Pin	Description	Logic State	Transition Bit Output Differential Voltage (mV)
OS1/2	Output Swing	Low (Floating)	900
		High	1200

Table 2. TUSB522P Equalization Control Pin Settings

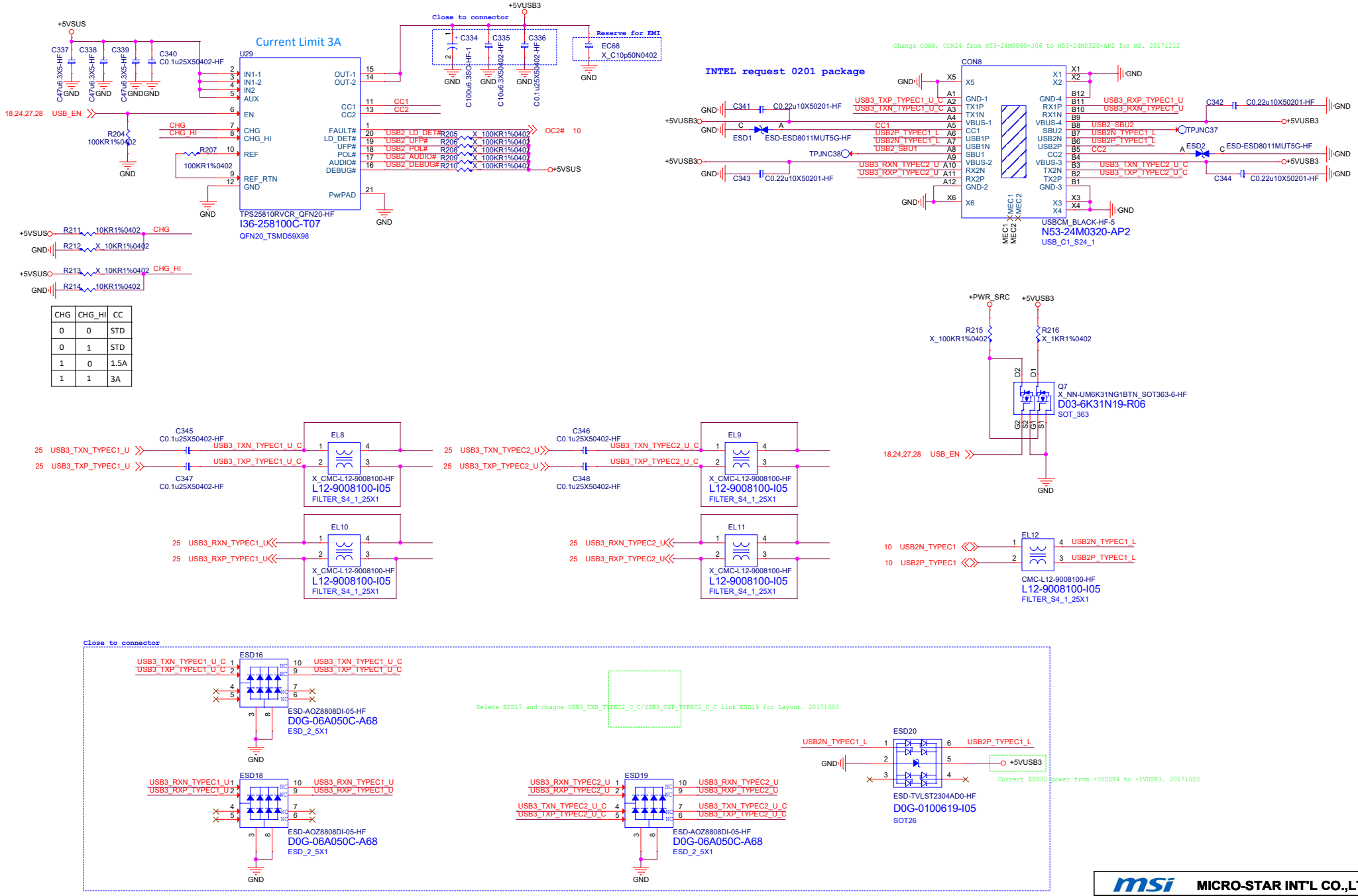
Pin	Description	Logic State	Gain (dB)
EQ1/EQ2	Equalization Amount	Low	3
		Floating	6
		High	9

Table 6. TUSB522P De-Emphasis Control Pin Settings

Pin	Description	Logic State	De-Emphasis Ratio (dB)	
			OS = Low(Floating)	OS = High
DE1/2	De-Emphasis Amount	Low	0	–2.6
		Floating	–3.5	–5.9
		High	–6.2	–8.3

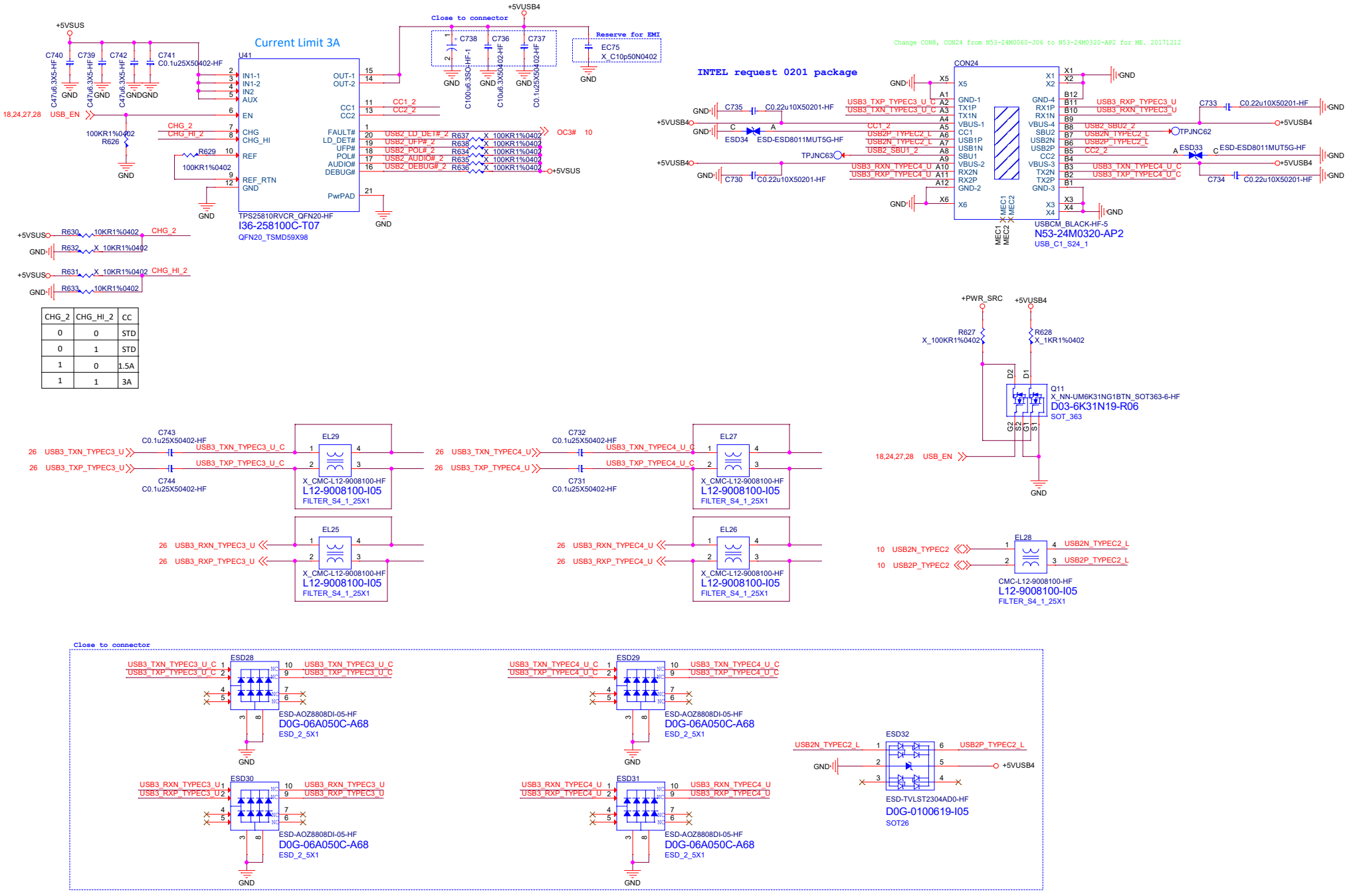


MSI	MICRO-STAR INT'L CO.,LTD.
Title	U3 Re-driver TYPE-C Port4
Size: Custom	Document Number: MS-14B1
Rev	0C
Date: Thursday, December 21, 2017	Sheet 26 of 57



CHG	CHG_HI	CC
0	0	STD
0	1	STD
1	0	1.5A
1	1	3A

Title	MICRO-STAR INT'L CO.,LTD.	
	USB Type-C (TPS25810) Port3	
Size: Custom	Document Number: MS-14B1	Rev: 0C
Date: Thursday, December 21, 2017	Sheet 27 of 57	



CHG_2	CHG_HI_2	CC
0	0	STD
0	1	STD
1	0	1.5A
1	1	3A

MICRO-STAR INT'L CO.,LTD.

Title: USB Type-C(TPS25810) Port4

Size: Custom | Document Number: MS-14B1 | Rev: 0C

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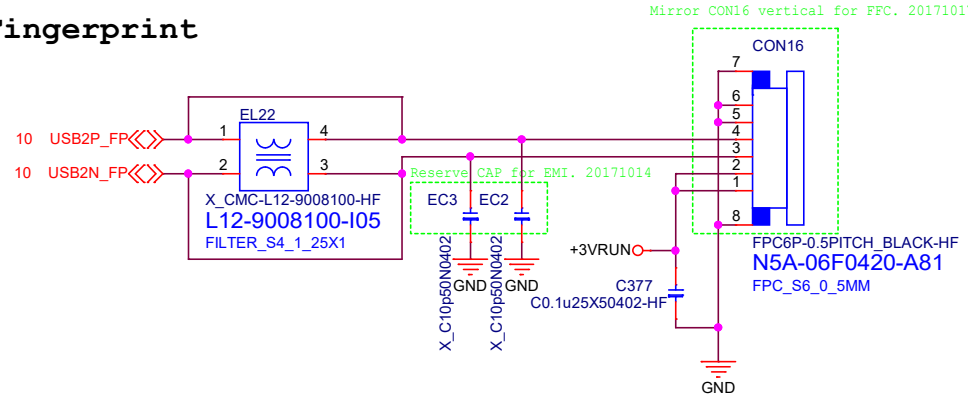
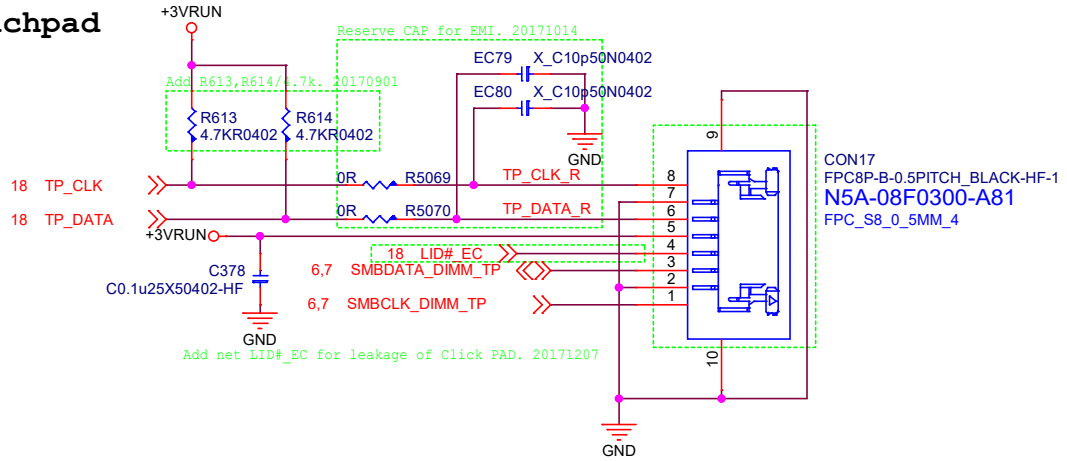
Fingerprint



J2 Pin Assignments and Definitions

Pin Number	Pin Name	Description
1	VDD	Power Supply
2	VDD	Power Supply
3	USB D-	USB D-
4	USB D+	USB D+
5	GND	Ground
6	GND	Ground

Touchpad



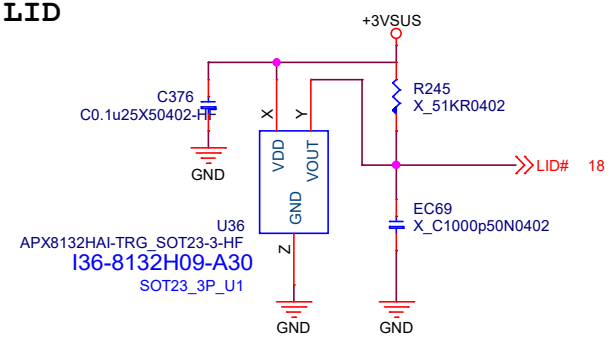
J1 (Host Interface) Pin Assignments and Definitions

Pin Number	Pin Name	Description
1	SMB_CLK	SMbus Clock
2	GND	Ground
3	SMB_DAT	SMbus Data
4	LID Close	Disable when lid is closed(1)
5	VDD	Power Supply
6	PS2_DAT	PS2 Data
7	GND	Ground
8	PS2_CLK	PS2 Clock

(1) Disable Touchpad when lid is closed (system sleep), to prevent from LCD noise coupling to touchpad and cause sensor malfunction

Change CON17 P/N from N5A-08F0160-A81 to N5A-08F0300-A81 for ME.20171004

LID



MICRO-STAR INT'L CO.,LTD.			
Title: Click,FingerPrint,LID			
Size: Custom	Document Number: MS-14B1		Rev: 0C
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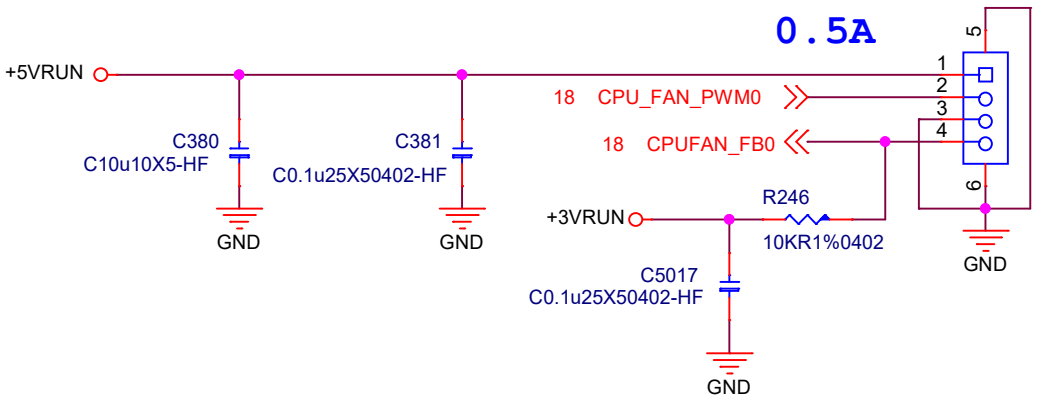
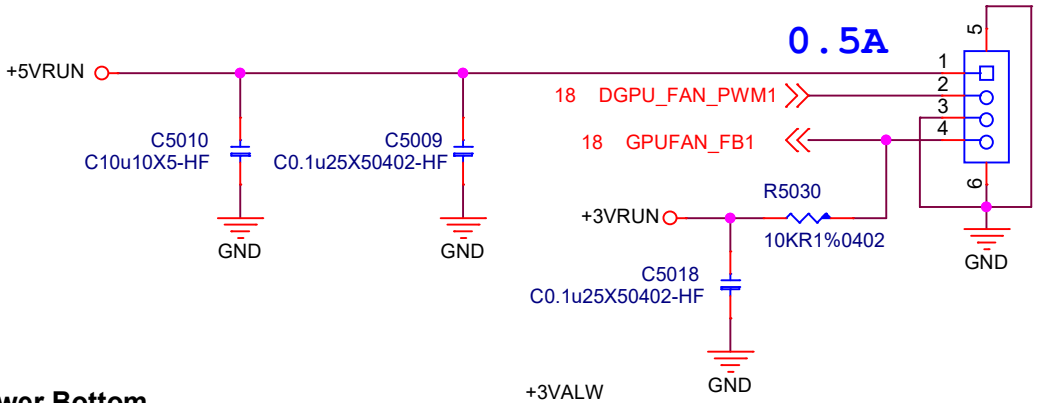
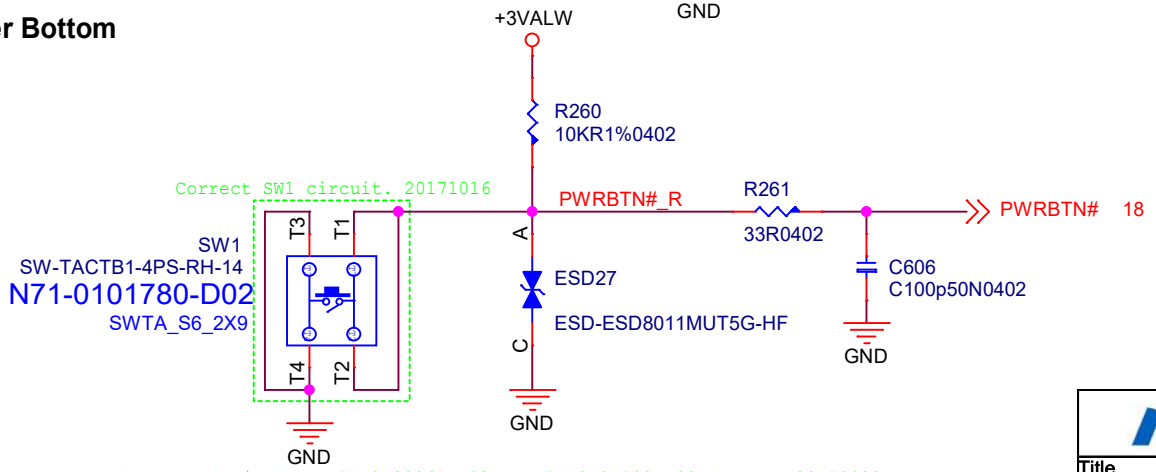
FAN

PIN NO.	LEAD COLOR
1	RED(+)
2	BLUE(PWM)
3	BLACK(−)
4	YELLOW(FG)

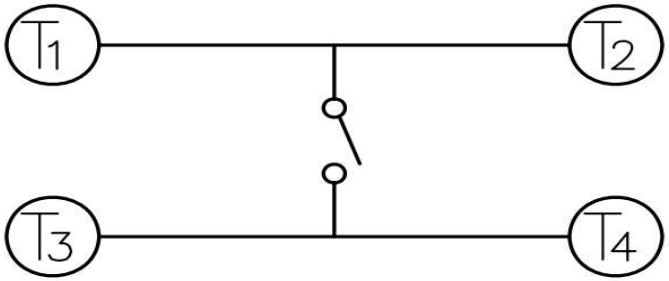




Power Bottom



Change SW1 P/N from N71-0103361-D02 to N71-0101780-D02 for ME. 20170929



CIRCUIT DIAGRAM

MICRO-STAR INT'L CO.,LTD.

Title: FAN,Power SW

Size: Custom | Document Number: MS-14B1 | Rev: 0C

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Change LED1,LED2,LED3 P/N from D0C-0405800-L05 to D0C-040C300-L05 for ME. 20171117A
Change LED4 P/N from D0C-0405400-L05 to D0C-040J800-L05 for ME. 20171117A

+5VSUS
R5031 330R0402
LED1
LED04-WHI-20mA3.15V_1608-RH
D0C-040C300-L05
LEDS_19_21SYGC
(5-2.8)/330 = 6.7mA
ACPI_LED# 18

R5032 330R0402
LED2
LED04-WHI-20mA3.15V_1608-RH
D0C-040C300-L05
LEDS_19_21SYGC
(5-2.8)/330 = 6.7mA
CHARGE_LED# 18

R5033 330R0402
LED4
LED04-O-30mA2.3V_1608-RH
D0C-040J800-L05
LEDS_19_21SYGC
(5-2)/330 = 9mA
BATLOW_LED# 18

R5034 330R0402
LED3
LED04-WHI-20mA3.15V_1608-RH
D0C-040C300-L05
LEDS_19_21SYGC
(5-2.8)/330 = 6.7mA
WLAN_LED# 18

R5036 330R0402
LED5
LED04-WHI-20mA3.15V_1608-RH
D0C-040C300-L05
LEDS_19_21SYGC
(5-2.7)/330 = 6.9mA
GPU_LED# 18
Change POWER_LED# net name to GPU_LED#. 20171019A

0.23A
+5VRUN
R610
0R0603
+5VRUN_Camera
Delete Camera power switch circuit. 20170926

USB2P_CAMERA
USB2N_CAMERA
EL23
X_CMC-L12-9008100-HF
L12-9008100-I05
FILTER_S4_1_25X1

Correct CON26 P/N:N5A-10F0240-A81. 20171212B
Change CON26 from N5A-10F0240-A81 to N5Q-10F0030-A81 for ME. 20171212
CON26
N5A-10F0240-A81
FPC_S10_0_5MM_1
FPC10P-0.5PITCH_BLACK-HF

21 DMIC_CLK
21 DMIC_DATA
+3VRUN
0.01A
18 Camera_ON
+5VRUN_Camera
10 USB2P_CAMERA
10 USB2N_CAMERA
USB2P_CAMERA
USB2N_CAMERA
GND-2
GND-1

Delete TPM circuit for Layout space. 20171018
Reserve CAP for EMI. 20171014
EC78 EC77 EC1 C5011 C379
X_C10p50N0402 X_C10p50N0402 C330p50X0402 C0.1u25X50402-HF C0.1u25X50402-HF
GND

Stuff EC1(C11-3312012-M09) for EMI. 20171218

ESD38
ESD-ESD8011MUT5G-HF
D0G-01A0510-O05
ESD_0_6X0_3

ESD35
ESD-ESD8011MUT5G-HF
D0G-01A0510-O05
ESD_0_6X0_3

ESD36
ESD-ESD8011MUT5G-HF
D0G-01A0510-O05
ESD_0_6X0_3

ESD37
ESD-ESD8011MUT5G-HF
D0G-01A0510-O05
ESD_0_6X0_3

ESD39
ESD-ESD8011MUT5G-HF
D0G-01A0510-O05
ESD_0_6X0_3
GND

Pin Description

Pin No.	Name	Pin Type	Function Des.	Pin No.	Name	Pin Type	Function Des.
1	DMIC_CLK	CLK	D-MIC clock	6	EN	Power	EN_3.3V
2	DMIC_DATA	Data	D-MIC data	7	VCC	Power	Cam_5V
3	GND	GND	GND	8	GND	GND	GND
4	MIC_VCC	Power	MIC_3.3V	9	D+	Data	USB_DP
5	NC	NC	NC	10	D-	Data	USB_DM

MICRO-STAR INT'L CO.,LTD.

Title: LED / Camera

Size: Custom | Document Number: MS-14B1 | Rev: 0C

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CPU STAND OFF

UME1 E2B_1P-5 E2B-13D2010-A89 H_R236D142_PB_N
UME2 E2B_1P-5 E2B-13D2010-A89 H_R236D142_PB_N
UME7 E2B_1P-5 E2B-13D2010-A89 H_R236D142_PB_N
UME8 E2B_1P-5 E2B-13D2010-A89 H_R236D142_PB_N

SPRING1 X_E23-1004060-CA7
SPRING2 X_E23-1004060-CA7

Add SPRING1,2 P/N:E23-1004060-CA7. 20171024A

MYL1 Mylar MYLAR,318.9*119*0.2mm E2P-4B10911-G40
MYL2 Mylar MYLAR,FR283,64*25.5*0.15mm E2P-0112911-G40

Add MYL1(E2P-4B10911-G40), MYL2(E2P-0112911-G40) for ME. 20171207

UME26 NPTH_98
UME27 NPTH_98
UME28 NPTH_98

X1 H_NR118D118
X2 H_NR118D118
X3 H_NR118D118
X4 H_NR118D118

UME3 H_R276D118_N
UME17 H_R276D118_N
UME18 H_R276D118_N
UME19 H_R276D118_N
UME20 H_R276D118_N
UME21 H_R276D118_N
UME22 H_R276D118_N
UME24 H_R276D118_N
UME25 H_R276D118_N

Change UME23, UME14, UME15 footprint to H_R276D118_V5_N for Layout. 20171030

UME23 H_R276D118_V5_N
UME14 H_R276D118_V5_N
UME15 H_R276D118_V5_N
UME13 H_R276D118_V8_N
UME16 H_R276D118_V8_N

Correct UME13,UME14,UME15,UME16,UME23 library. 20171020A

Delete FM1 for Layout. 20171024A

FM2 X_F_PAD_X F_PAD_X
FM3 X_F_PAD_X F_PAD_X
FM4 X_F_PAD_X F_PAD_X
FM5 X_F_PAD_X F_PAD_X
FM6 X_F_PAD_X F_PAD_X
FM7 X_F_PAD_X F_PAD_X
FM21 X_F_PAD_X F_PAD_X
FM8 X_F_PAD_X F_PAD_X
FM9 X_F_PAD_X F_PAD_X
FM10 X_F_PAD_X F_PAD_X
FM11 X_F_PAD_X F_PAD_X
FM12 X_F_PAD_X F_PAD_X
FM13 X_F_PAD_X F_PAD_X
FM14 X_F_PAD_X F_PAD_X
FM22 X_F_PAD_X F_PAD_X
FM15 X_F_PAD_X F_PAD_X
FM16 X_F_PAD_X F_PAD_X
FM17 X_F_PAD_X F_PAD_X
FM18 X_F_PAD_NB_2 F_PAD_NB_2
FM19 X_F_PAD_NB_2 F_PAD_NB_2
FM23 X_F_PAD_NB_1 F_PAD_NB_2
FM25 X_F_PAD_NB_2 F_PAD_NB_2
FM20 X_F_PAD_NB_1 F_PAD_NB_2
FM27 X_F_PAD_NB_2 F_PAD_NB_2
FM28 X_F_PAD_NB_2 F_PAD_NB_2
FM30 X_F_PAD_NB_2 F_PAD_NB_2
FM31 X_F_PAD_NB_1 F_PAD_NB_2

Delete FM24, FM26, FM29, FM32 for Layout. 20171026

Delete FM33,FM34 for Layout. 20171025

GPU STAND OFF

UME9 E2B_1P-5 E2B-13D2010-A89 H_R236D142_PB_N
UME10 E2B_1P-5 E2B-13D2010-A89 H_R236D142_PB_N
UME11 E2B_1P-5 E2B-13D2010-A89 H_R236D142_PB_N
UME12 E2B_1P-5 E2B-13D2010-A89 H_R236D142_PB_N

PCB1 PD0-14B110B-H73

PD0-14B110B-H73

Change PCB1 from PD0-14B110A-H73 to PD0-14B110B-H73. 20171121

+5VRUN
EC89 X_C0.1u25X50402-HF

+PWR_SRC
EC88 X_C0.1u25X50402-HF
EC82 X_C0.1u25X50402-HF
EC83 X_C0.1u25X50402-HF
EC84 X_C0.1u25X50402-HF
EC85 X_C0.1u25X50402-HF
EC86 X_C0.1u25X50402-HF
EC87 X_C0.1u25X50402-HF

Reserve EC82~89/0.1uF for EMI. 20171024

Differential 80 ohm

J62 L1_DIFF_5/4.5/5_80_Ohm+ L1_DIFF_5/4.5/5_80_Ohm- GND2 GND2 X_H1X2_black
J63 L3_DIFF_4/4.5/4_80_Ohm+ L3_DIFF_4/4.5/4_80_Ohm- GND2GND4 GND2GND4 X_H1X2_black
J64 L8_DIFF_4/4.5/4_80_Ohm+ L8_DIFF_4/4.5/4_80_Ohm- GND7GND9 GND7GND9 X_H1X2_black
J65 L10_DIFF_5/4.5/5_80_Ohm+ L10_DIFF_5/4.5/5_80_Ohm- GND9 GND9 X_H1X2_black

Differential 90 ohm

J66 L1_DIFF_4/4.5/4_90_Ohm+ L1_DIFF_4/4.5/4_90_Ohm- GND2 GND2 X_H1X2_black
J67 L3_DIFF_3.5/5.5/3.5_90_Ohm+ L3_DIFF_3.5/5.5/3.5_90_Ohm- GND2GND4 GND2GND4 X_H1X2_black
J68 L8_DIFF_3.5/5.5/3.5_90_Ohm+ L8_DIFF_3.5/5.5/3.5_90_Ohm- GND7GND9 GND7GND9 X_H1X2_black
J69 L10_DIFF_4/4.5/4_90_Ohm+ L10_DIFF_4/4.5/4_90_Ohm- GND9 GND9 X_H1X2_black

Single 40 Ohm

J38 L1_7mil_40_Ohm X_PIN1*2 GND2
J1 L3_4.5mil_40_Ohm X_PIN1*2 GND2GND4
J4 L8_4.5mil_40_Ohm X_PIN1*2 GND7GND9
J5 L10_7mil_40_Ohm X_PIN1*2 GND9

Single 50 Ohm

J39 L1_4.5mil_50_Ohm X_PIN1*2 GND2
J3 L3_3mil_50_Ohm X_PIN1*2 GND2GND4

Delete J40/L5_3.5mil_50_Ohm, J6/L6_3.5mil_50_Ohm. 20171019

J7 L8_3mil_50_Ohm X_PIN1*2 GND7GND9
J41 L10_4.5mil_50_Ohm X_PIN1*2 GND9

Differential 83 ohm

J21 L1_DIFF_4.5/4/4.5_83_Ohm+ L1_DIFF_4.5/4/4.5_83_Ohm- GND2 GND2 X_H1X2_black
J51 L3_DIFF_4/5/4_83_Ohm+ L3_DIFF_4/5/4_83_Ohm- GND2GND4 GND2GND4 X_H1X2_black
J52 L8_DIFF_4/5/4_83_Ohm+ L8_DIFF_4/5/4_83_Ohm- GND7GND9 GND7GND9 X_H1X2_black
J53 L10_DIFF_4.5/4/4.5_83_Ohm+ L10_DIFF_4.5/4/4.5_83_Ohm- GND9 GND9 X_H1X2_black

Differential 85 ohm

J54 L1_DIFF_4.5/4.5/4.5_85_Ohm+ L1_DIFF_4.5/4.5/4.5_85_Ohm- GND2 GND2 X_H1X2_black
J55 L3_DIFF_3.5/5/3.5_85_Ohm+ L3_DIFF_3.5/5/3.5_85_Ohm- GND2GND4 GND2GND4 X_H1X2_black
J56 L8_DIFF_3.5/5/3.5_85_Ohm+ L8_DIFF_3.5/5/3.5_85_Ohm- GND7GND9 GND7GND9 X_H1X2_black
J57 L10_DIFF_4.5/4.5/4.5_85_Ohm+ L10_DIFF_4.5/4.5/4.5_85_Ohm- GND9 GND9 X_H1X2_black

Differential 100 ohm

J58 L1_DIFF_3.5/6.5/3.5_100_Ohm+ L1_DIFF_3.5/6.5/3.5_100_Ohm- GND2 GND2 X_H1X2_black
J59 L3_DIFF_3/6/3_100_Ohm+ L3_DIFF_3/6/3_100_Ohm- GND2GND4 GND2GND4 X_H1X2_black
J60 L8_DIFF_3/6/3_100_Ohm+ L8_DIFF_3/6/3_100_Ohm- GND7GND9 GND7GND9 X_H1X2_black
J61 L10_DIFF_3.5/6.5/3.5_100_Ohm+ L10_DIFF_3.5/6.5/3.5_100_Ohm- GND9 GND9 X_H1X2_black

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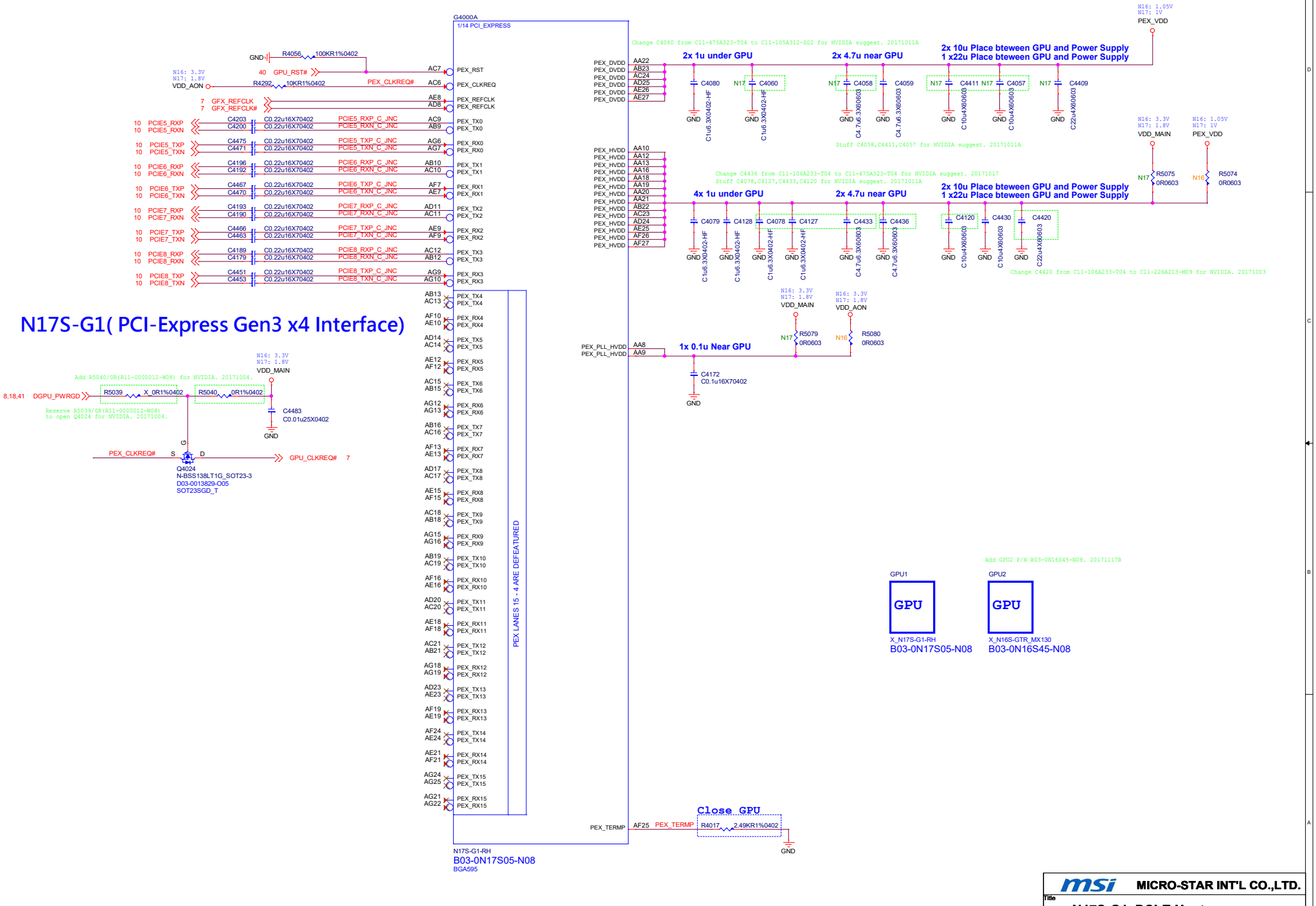
G4000A
1/14 PCI_EXPRESS
N17S-G1(PCI-Express Gen3 x4 Interface)
PEX LANES 15 - 4 ARE DEFEATURED
2x 1u under GPU
2x 4.7u near GPU
2x 10u Place bteween GPU and Power Supply
1 x22u Place bteween GPU and Power Supply
4x 1u under GPU
1x 0.1u Near GPU
Close GPU
PEX_VDD
VDD_MAIN
VDD_AON
GPU1
GPU2
X_N17S-G1-RH
B03-0N17S05-N08
X_N16S-GTR_MX130
B03-0N16S45-N08
N17S-G1-RH
B03-0N17S05-N08
BGA595
MICRO-STAR INT'L CO.,LTD.
N17S-G1_PCI-E Host
MS-14B1
0C
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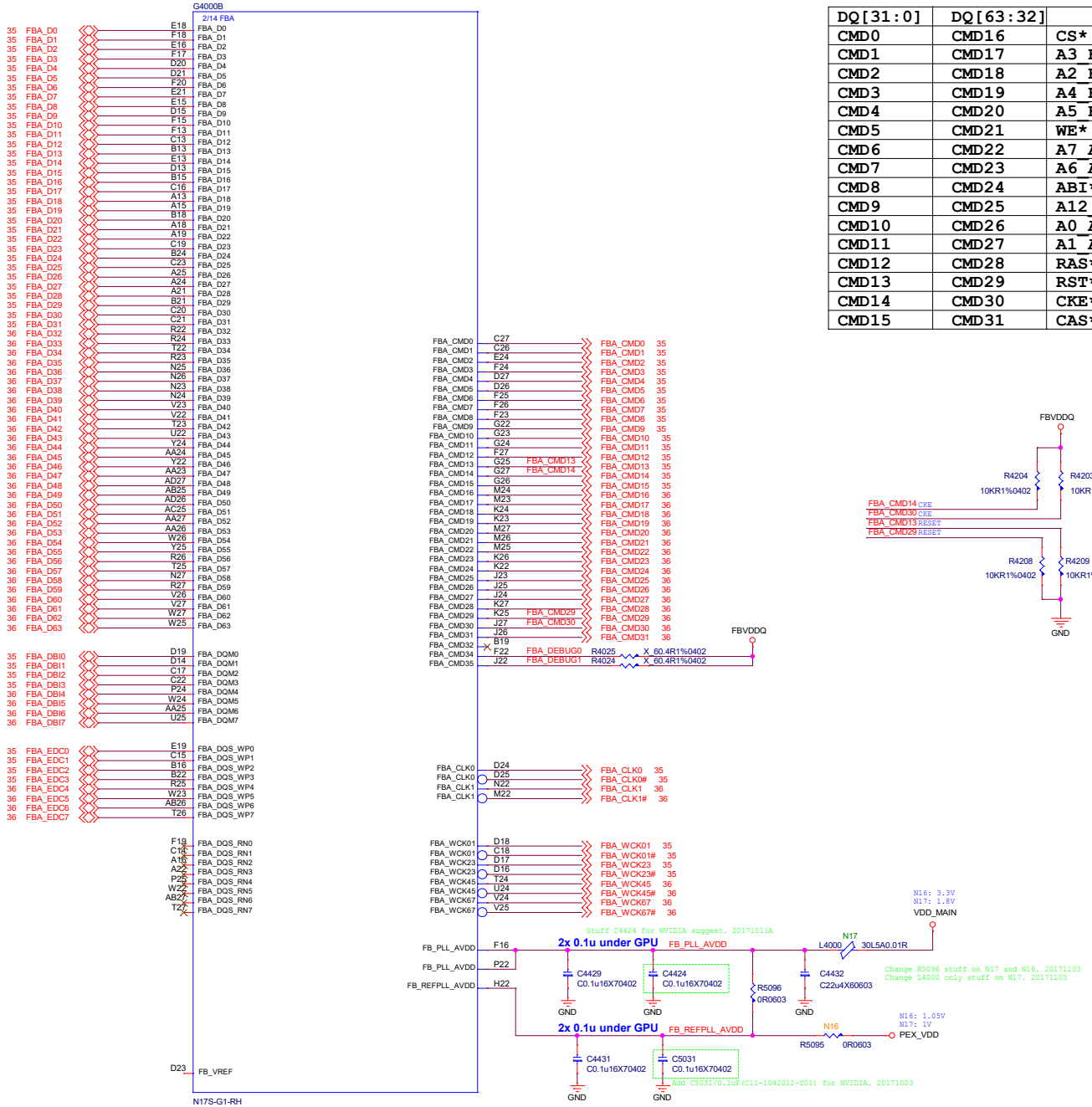
N17S-G1(Frame Buffer Interface)

GDD5 Command Mapping GB2C-64

DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	N17S-G1_MEM IF-A	
Size: Custom	Document Number: MS-14B1	Rev: 0C
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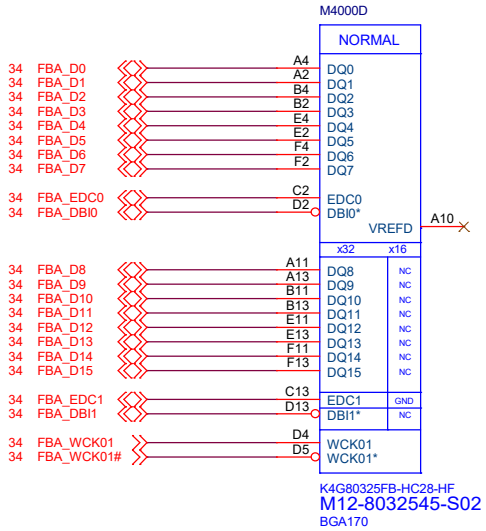
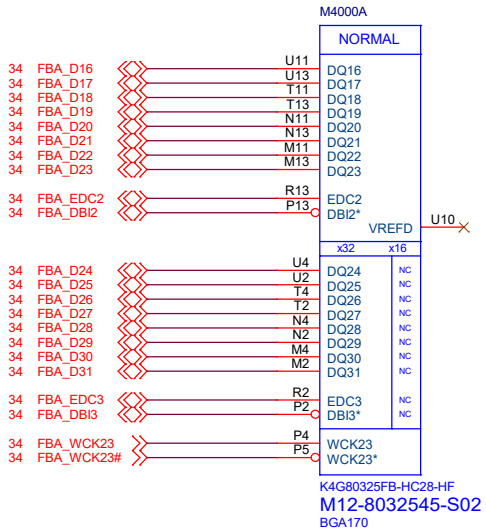
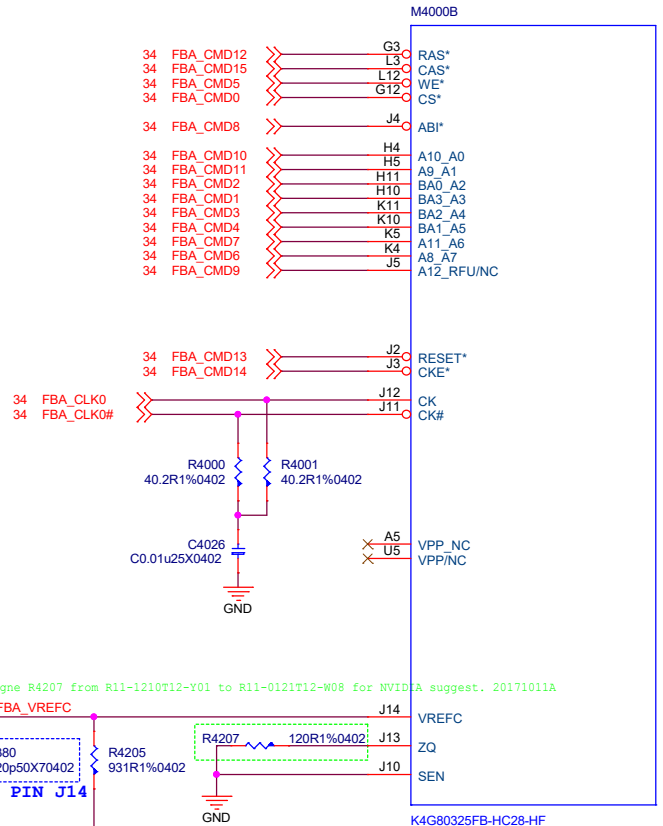
N17S-G1_GDDR5 Frame A-1

GDD5 Command Mapping GB2C-64

DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*







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Title: N17S-G1_GDDR5 Frame A-1

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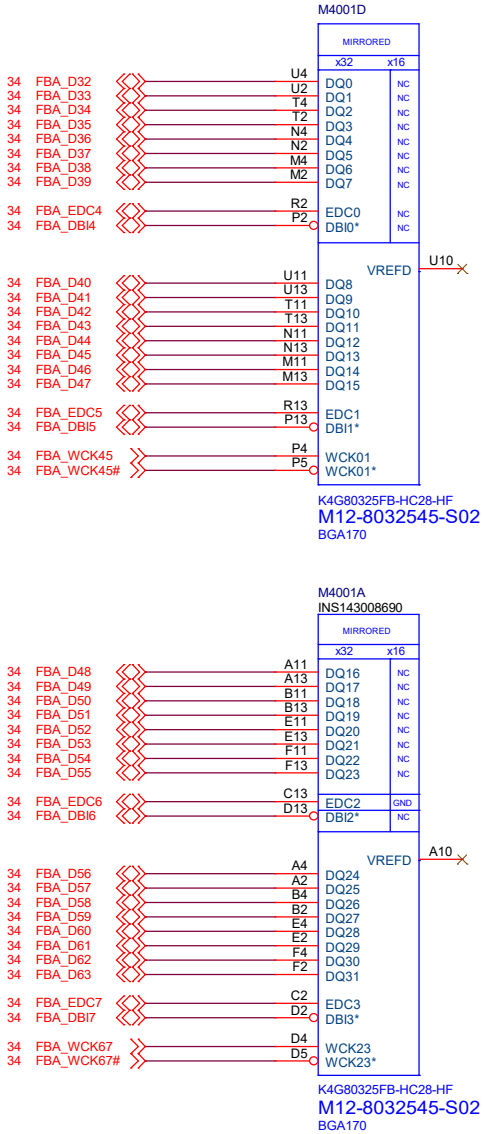
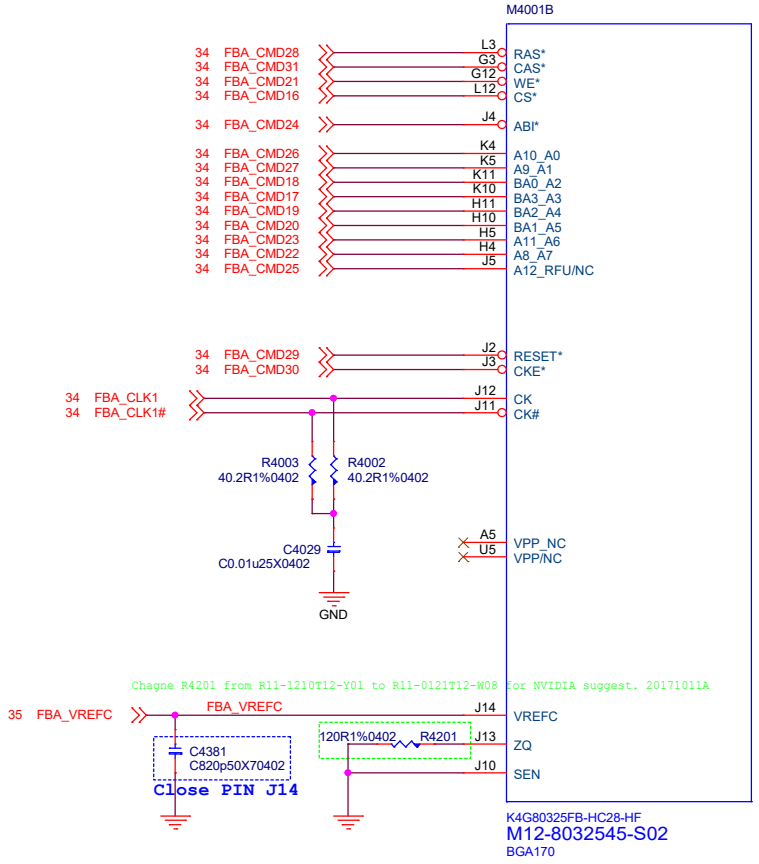
N17S-G1_GDDR5 Frame A-2



GDD5 Command Mapping GB2C-64

DQ[31:0]	DQ[63:32]	
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*



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Title: N17S-G1_GDDR5 Frame A-2

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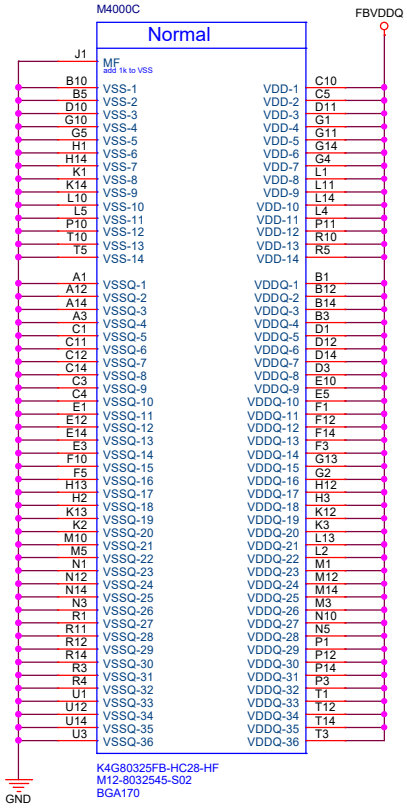
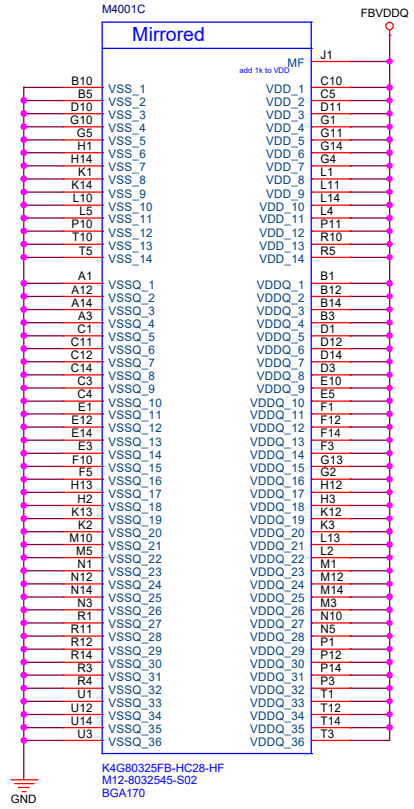
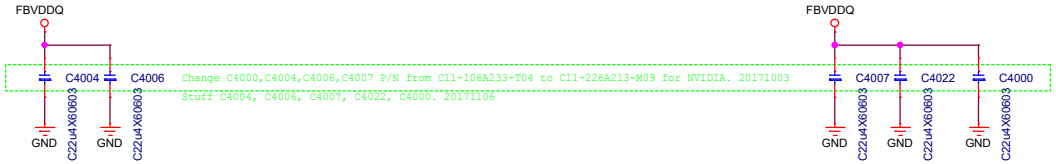
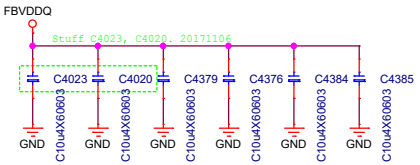
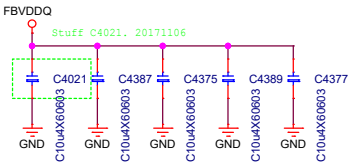
N17S-G1_GDDR5_DECOUPLING

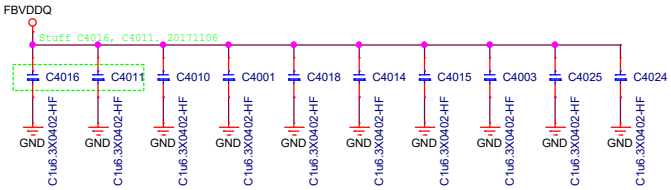


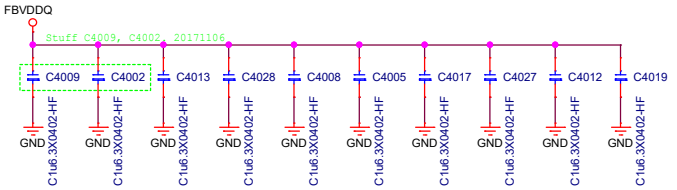












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Title: N17S-G1_GDDR5_DECOUPLING

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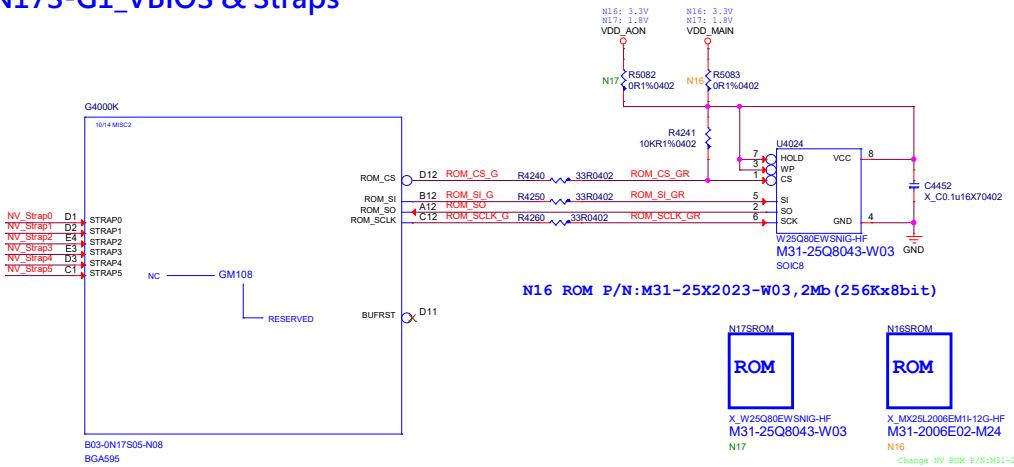
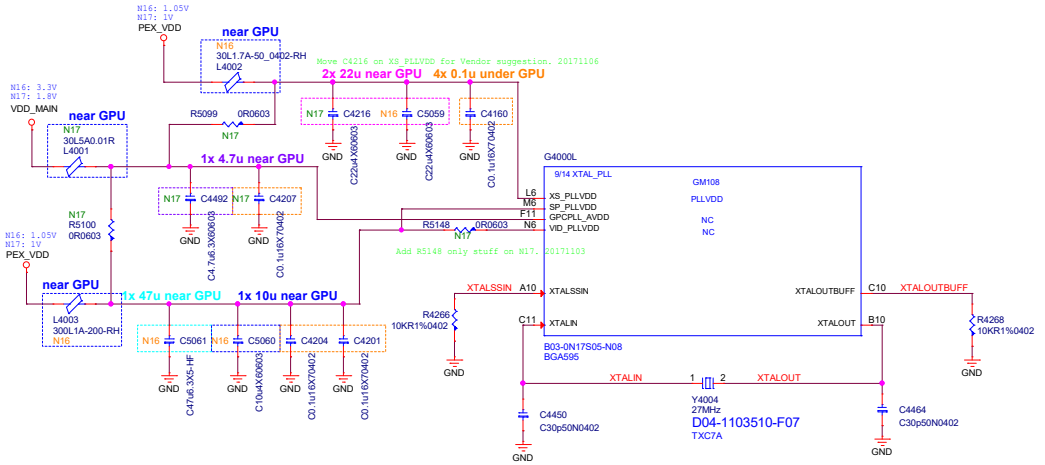
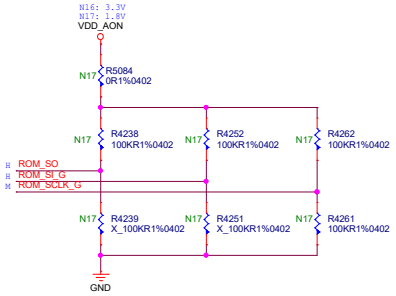
N17S-G1_VBIOS & Straps



N16 ROM P/N:M31-25X2023-W03,2Mb(256Kx8bit)

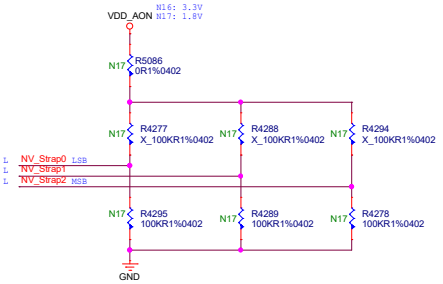
Change NV ROM P/N:M31-2006E02-M24 in N16S. 20171207



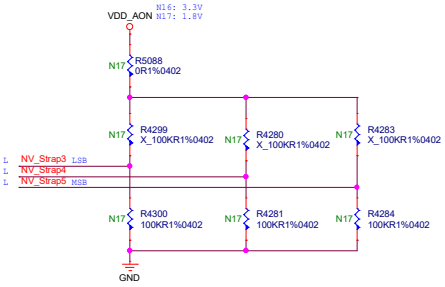


ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED3	SOR_EXPOSED2	SOR_EXPOSED1	SOR_EXPOSED0
L	L	L	1:ENABLE	1:ENABLE	1:ENABLE	1:ENABLE
L	L	H	1:ENABLE	1:ENABLE	1:ENABLE	0:DISABLE
L	H	L	1:ENABLE	1:ENABLE	0:DISABLE	1:ENABLE
L	H	H	1:ENABLE	1:ENABLE	0:DISABLE	0:DISABLE
H	H	H	1:ENABLE	0:DISABLE	0:DISABLE	0:DISABLE
H	H	M	0:DISABLE	0:DISABLE	0:DISABLE	0:DISABLE

256Mx32	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
	Samsung	K4G80325FB-HC28	B-die	0x0	3000	N/A	Substitution allowed with waiver[2]



STRAP 2	STRAP 1	STRAP 0			
L	L	L	0x0	Samsung K4G80325FB-HC28	
L	L	H	0x1	Microm MT51J2256M32HF-70:A	256M*32
L	H	L	0x2	Hynix H5GC8H24MJR-R0C	
H	H	L	0x6	Hynix H5GC4H24AJR-R0C	
H	H	H	0x7	Samsung K4G41325FE-HC28	128M*32
L	L	M	0x8	Microm EDW4032BABG-70-F	



STRAP 5	STRAP 4	STRAP 3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
L	L	L	0	0	0	0	Optimus
L	L	H	0	0	0	1	Discrete
H	L	H	0	1	0	1	Discrete with Gsync

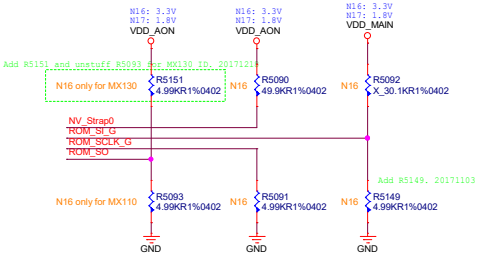


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 12. N16/GB2B-64 Multi-Level Straps

Strap Pin	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Stuff 49.9 kΩ pull-up to VDD_AON (3.3V).			
STRAP1	Reserved			
STRAP2	Reserved			
STRAP3	Reserved			
STRAP4	Reserved			

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Title: N17S-G1_VBIOS & Straps

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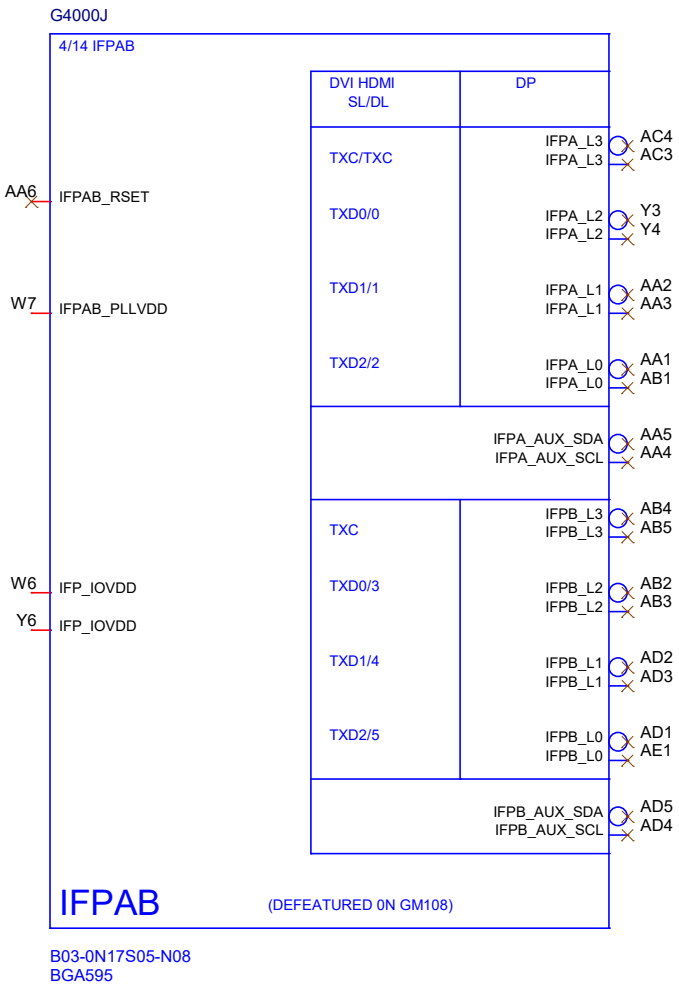
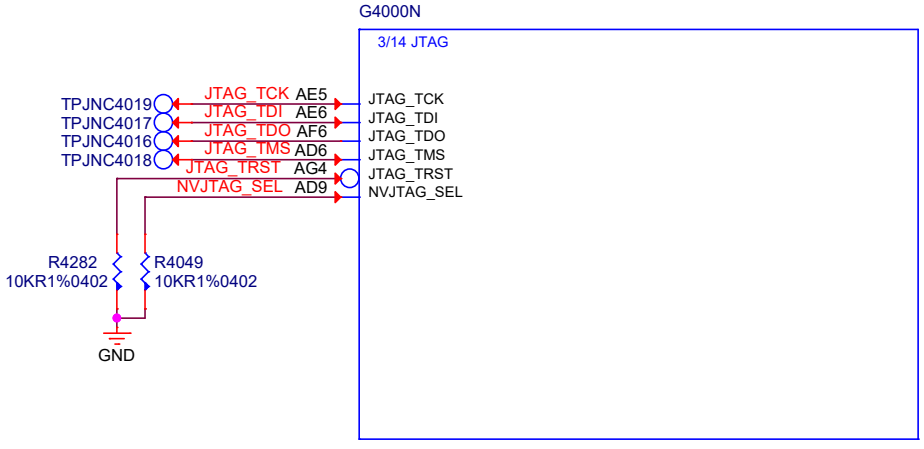
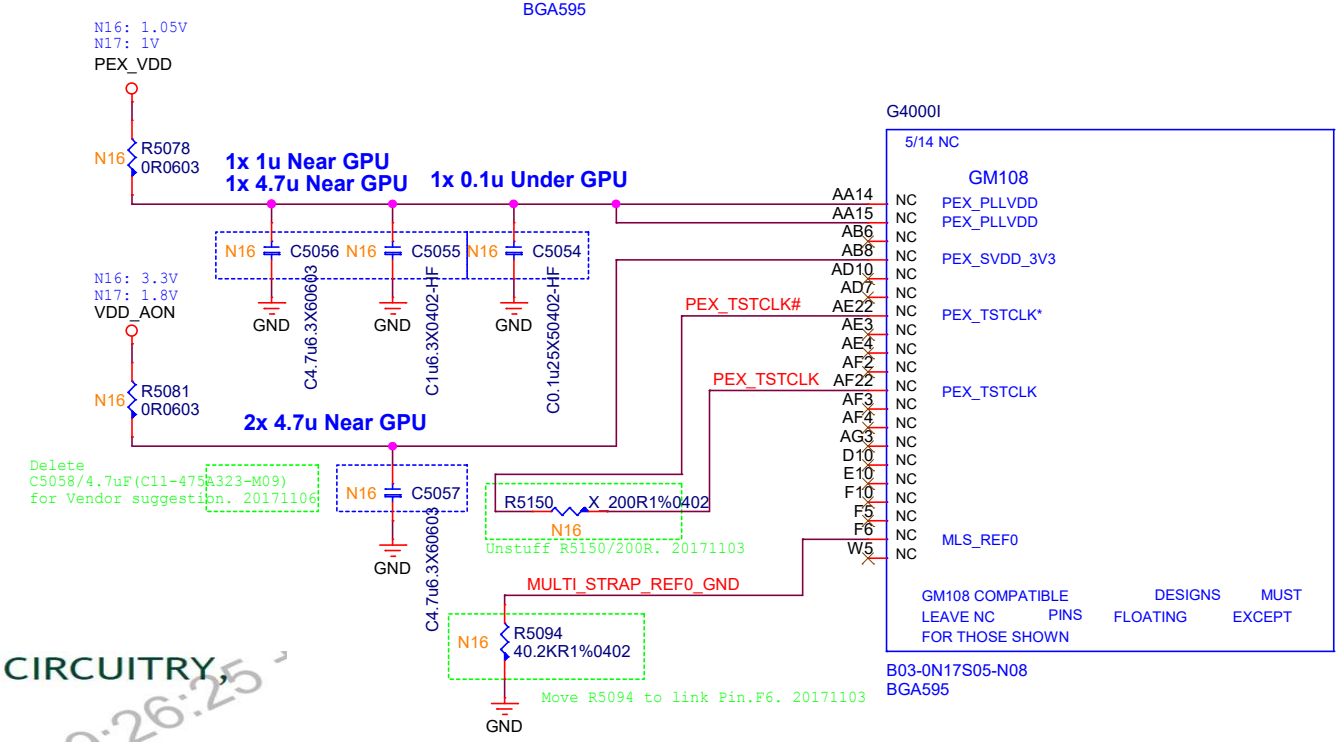
N17S-G1_Display IF







15.2 INTERFACE CONFIGURATION, CIRCUITRY, SAMPLE CIRCUITRY

To select different Strap Mode, MULTI_STRAP_REF0_GND pins need to be stuffed accordingly. Table 15-1 provides the necessary connections to set the correct strapping mode for each device.

Table 15-1. Device Specific Strap Mode Selection

	All N16x GPUs
Multi_Strap_Ref0_GND	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 40.2k 1% to GND

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Title: N17S-G1_Display IF

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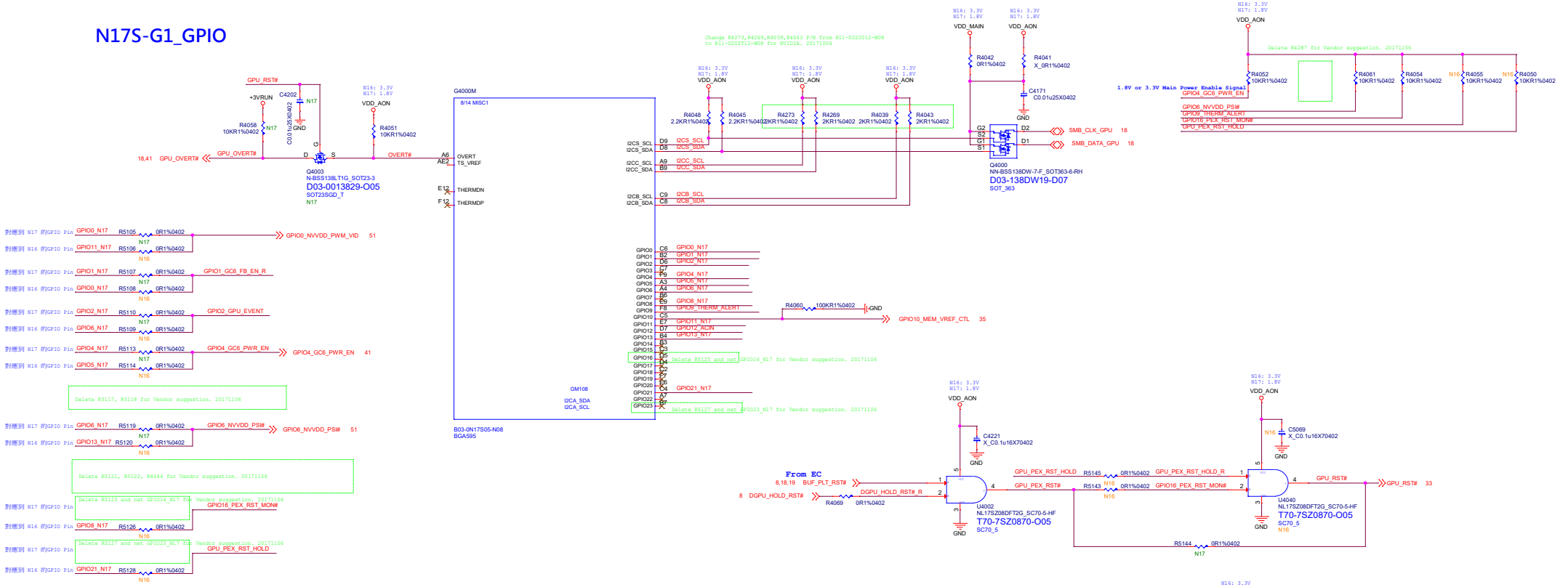
N17S-G1_GPIO



AC_OK#	GPU_ACIN1 (EC Ctrol)	GPIO12_GPU_ACIN
0	0	1
0	1	1
1	0	1
1	1	0

Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	NVVDD_PWM	O	PWM Output To Contral NVVDD	0 TO 1V8 PWM Output
GPIO1	GC6M:GC6_FB_EN	O	FB Enable For GC6 2.1	Open Source 10K Pull-Down
GPIO2	GC6M:GC6_EVENT / WAKE	I	GPU Wake Signal For GC6 2.1	10K Pull-Up To 1V8_AON Unless Driven Actively
GPIO3	NVVDDS_PWM(NC)	I/O	PWM Output To Control The NVVDS Power Supply	0 TO 1V8 Output
GPIO4	GC6M:1V8_MAIN_EN	O	GPU Power Sequencing For GC6 2.1	Open Drain 10K Pull-Up To 1V8_AON
GPIO5	FRM_LCK	I	Active Low Frame Lock	Open Drain 10K Pull-Up To 1V8_AON
GPIO6	NVVDD_PSI/NVVDDS_PSI	O	Phase Shedding	10K Pull-Up To 1V8_AON To Enable Multiple Phases
GPIO7	LCD_BL_PWM(NC)	O	Panel Backlight Enable	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	Pull-Up/Pull-Down To Set The FBVDD/Q Power ON Voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10K Pull-Up To 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VDD(NC)	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC Power Detect Or Power Supply Overdraw Input	100K Pull-Up To 1V8_AON
GPIO13	LCD_BLEN(NC)	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA(NC)	I	Hot Plug Detect for IFPA	
GPIO15	HPD_IFPB(NC)	I	Hot Plug Detect for IFPB	
GPIO16	GC6M:SYS_PEX_RST_MON	I	System Side PCIE Reset Monitor	10K Pull-Up To 1V8_AON Unless Driven Actively
GPIO17	UNUSED(NC)	I/O		
GPIO18	UNUSED(NC)	I/O		
GPIO19	3D_Vision(NC)	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE(NC)	I/O		
GPIO21	OC_WARN/HT	I	Over Current Throttling Trigger	10K Pull-Up To 1V8_AON
GPIO22	UNUSED(NC)	I/O		
GPIO23	GC6M:GPU_PEX_RST_HOLD	O	GPU PCIE Self Reset Control	Open Drain 10K Pull-Up To Gated 3V3

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Title: N17S-G1_GPIO

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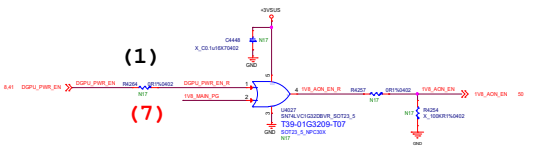
N17S-G1_Power Control

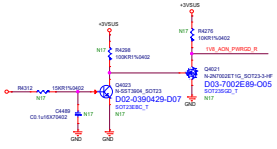
Power on = 1V8_AON -> (VDD_MAIN) 1V8_MAIN -> NVVDD+NVVDDS -> PEX_VDD -> FBVDDQ -> DGPUPWRGD

Power down = PEX_VDD/FBVDDQ -> NVVDD+NVVDDS -> 1V8_MAIN -> 1V8_AON

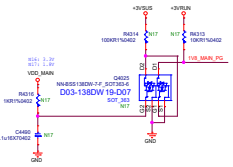
1V8_AON



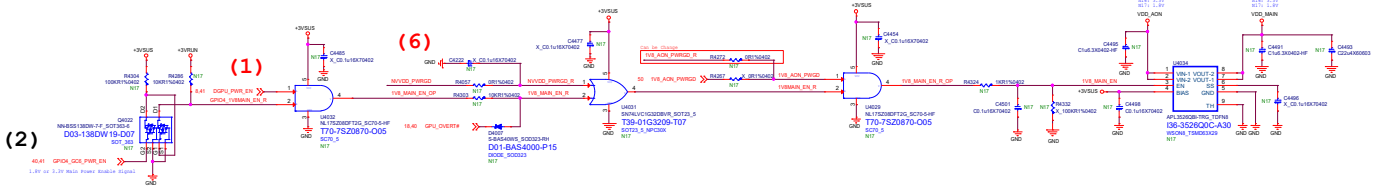
1V8_AON POWER GOOD



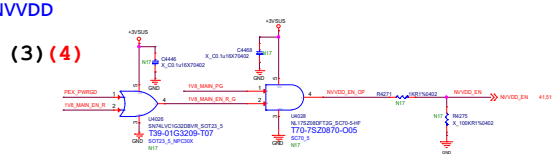
1V8_MAIN POWER GOOD



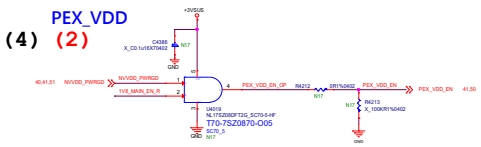
1V8_MAIN



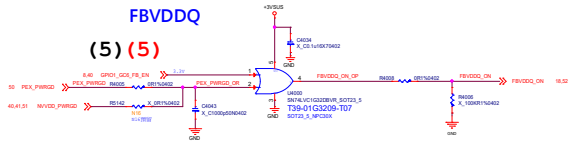
NVVDD



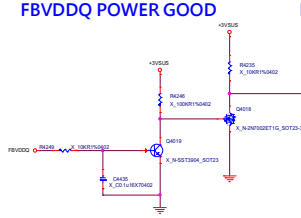
PEX_VDD



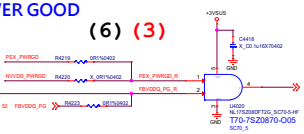
FBVDDQ



FBVDDQ POWER GOOD

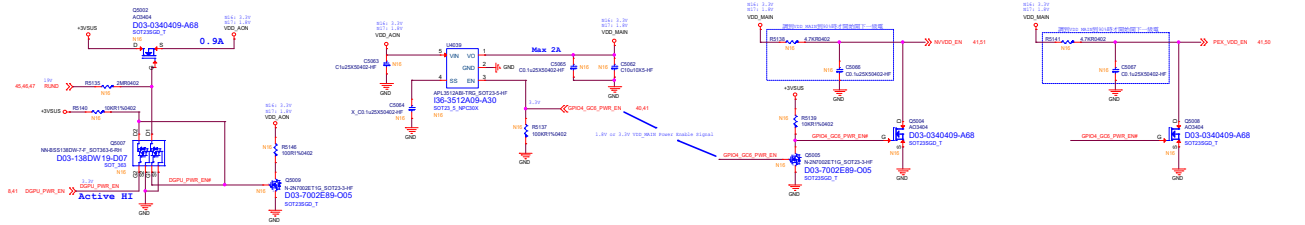


DGPU POWER GOOD

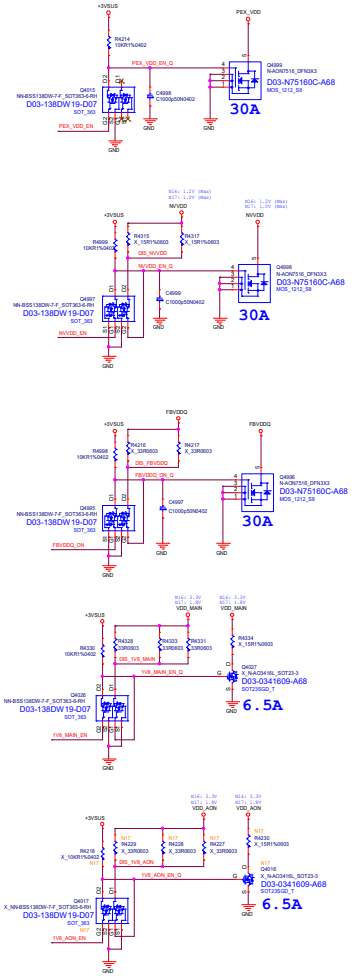


N16S_Power Control

Power on = 3V3_AON -> VDD_MAIN (3V3_MAIN) (3V3_NV) -> NVVDD ->PEX_VDD -> FBVDDQ -> DGPUPWRGD



Discharge Circuit



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Title: N17S-G1 Power Control			
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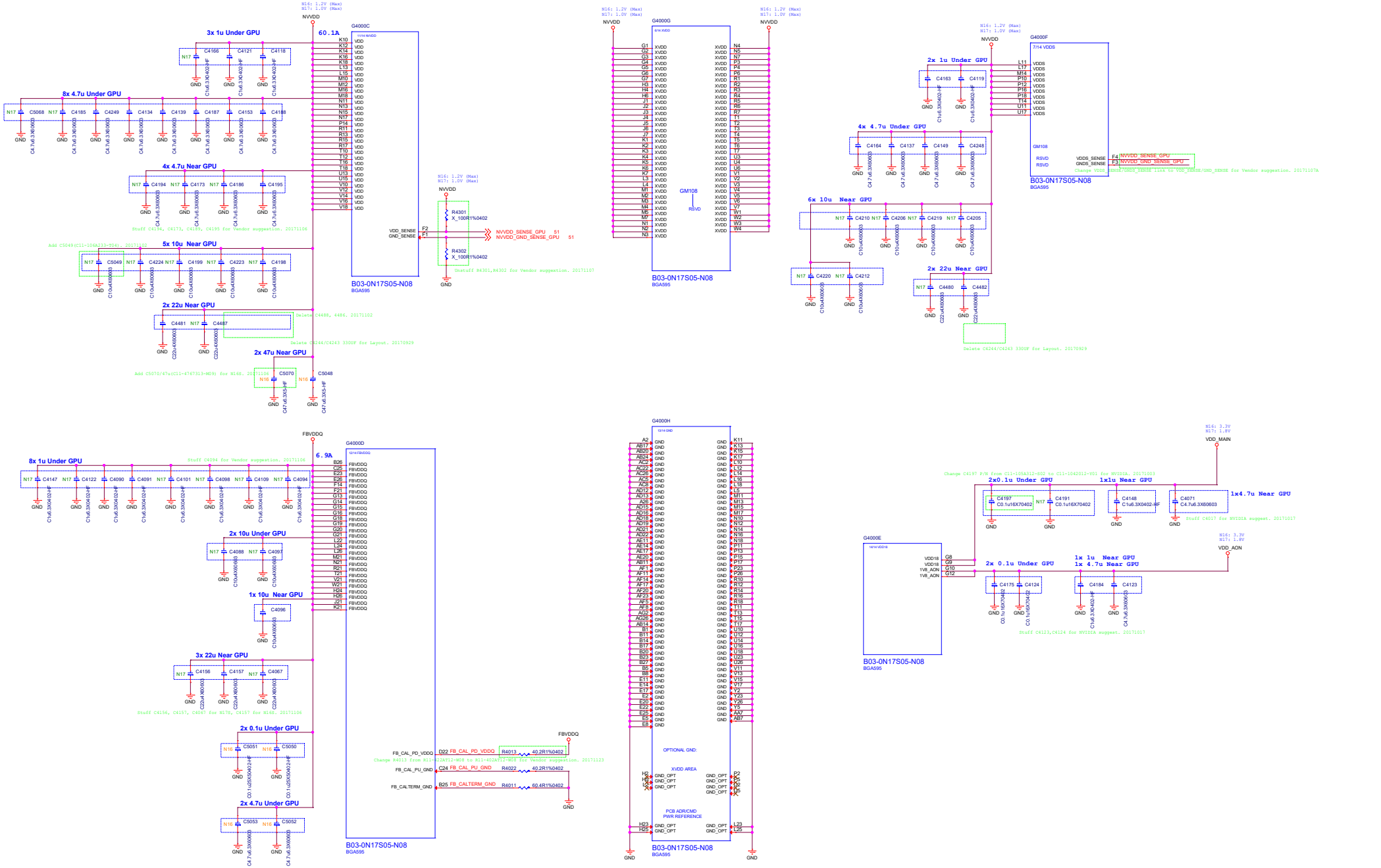
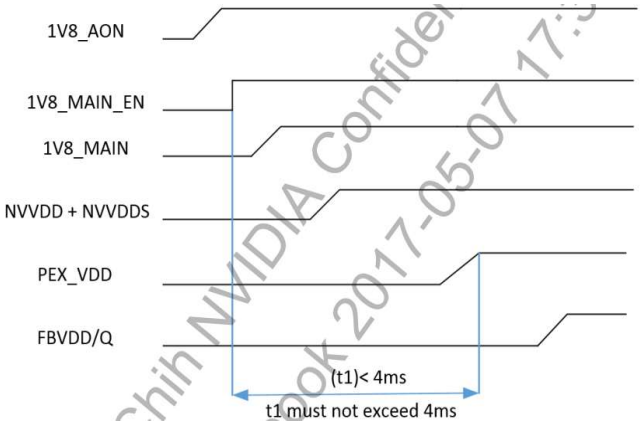
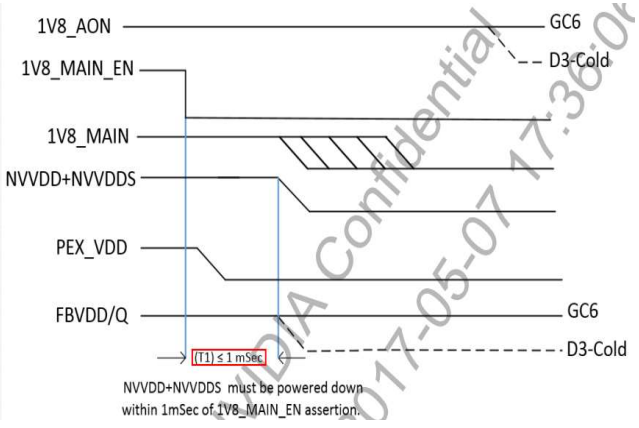
N17S-G1_Power & GND



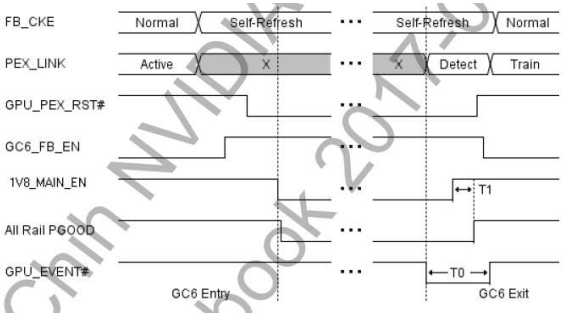
N17 Power Up



N17 Power Down



GC6 2.1



GC6 2.1 Entry/Exit Sequence Timing Diagram

Symbol	Description	Min	Max	Units
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

GC6 2.0

18.3.4.3 GC6 2.0 Entry/Exit Timing

The following timing diagram in Figure 18-14 and Table 18-3 describes the GC6 2.0 entry and exit sequence and timing requirements.

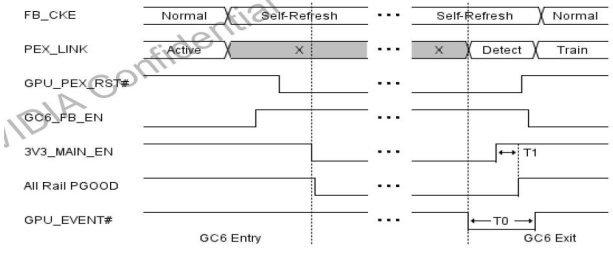


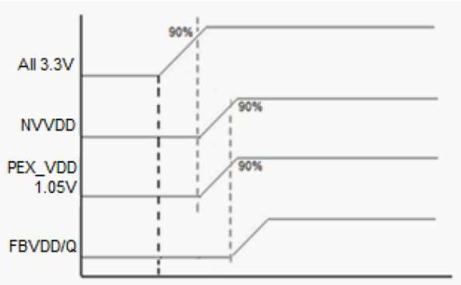
Figure 18-14. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-3. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Note:
- ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in GC6 for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.

N16 Power Up



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-7. Example of Power-Up Sequencing Order

Note:
- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- A VDD33 must ramp up to 90% before NVVDD and PEXVDD in sequence can start ramping up. NVVDD must ramp up to 90% before FBVDD/Q in sequence can start ramping up
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.

Optimus

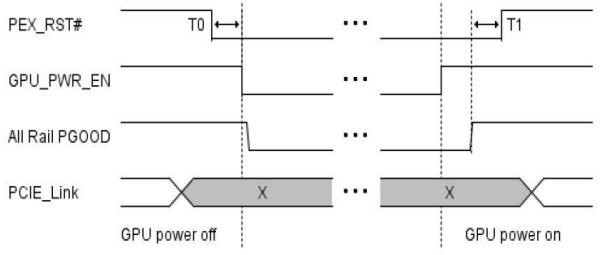


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

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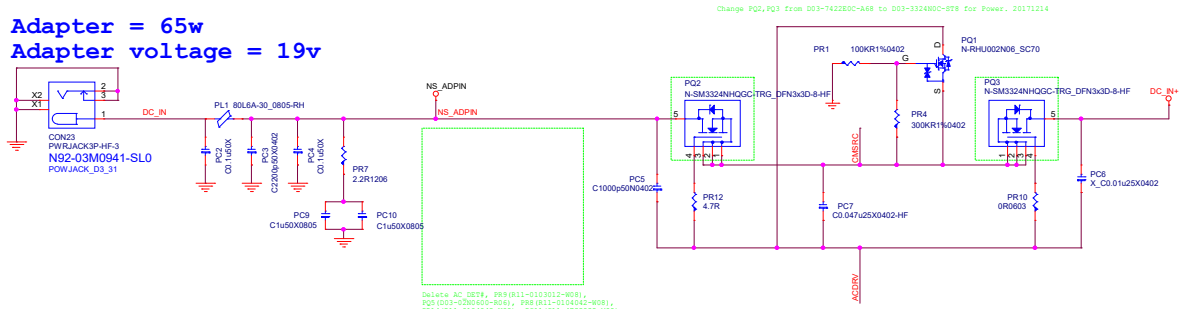
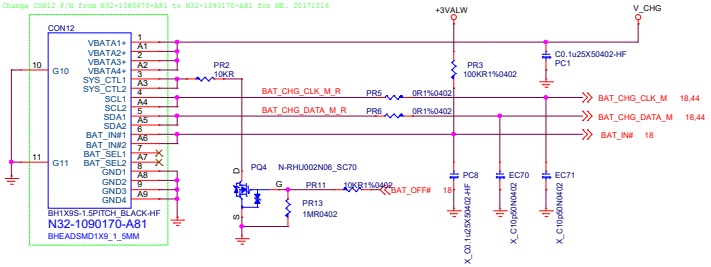
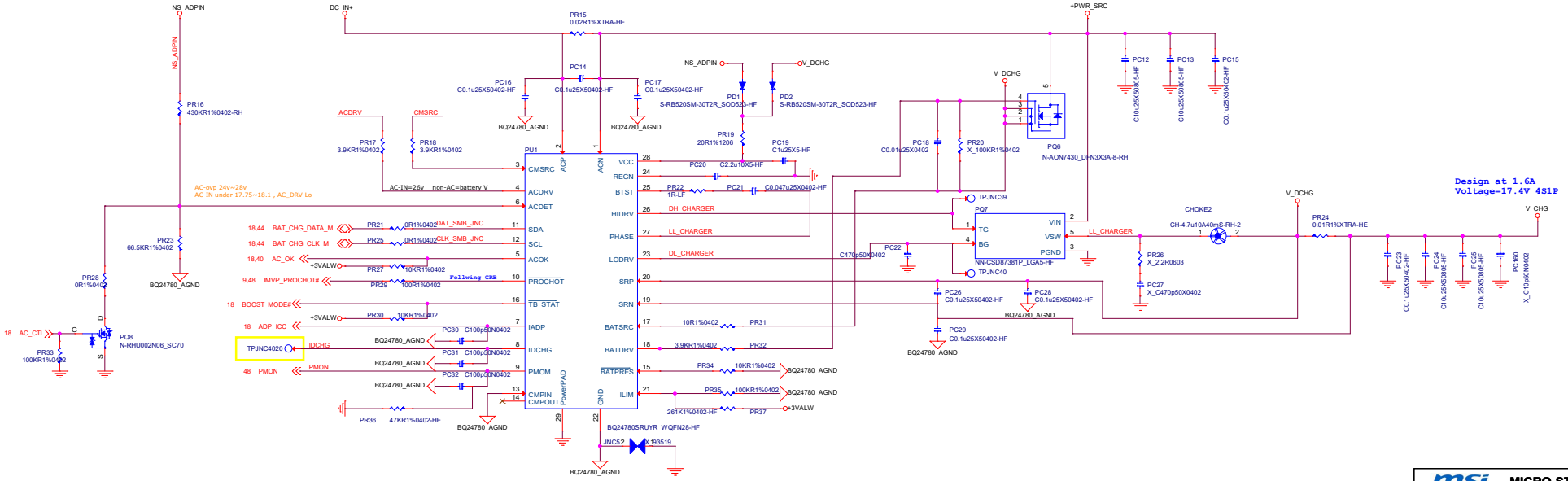
Adapter = 65w
Adapter voltage = 19v







msi MICRO-STAR INT'L CO.,LTD.			
Title: AC_IN & Battery charge			
Size: Custom	Document Number: MS-14B1		Rev: 0C
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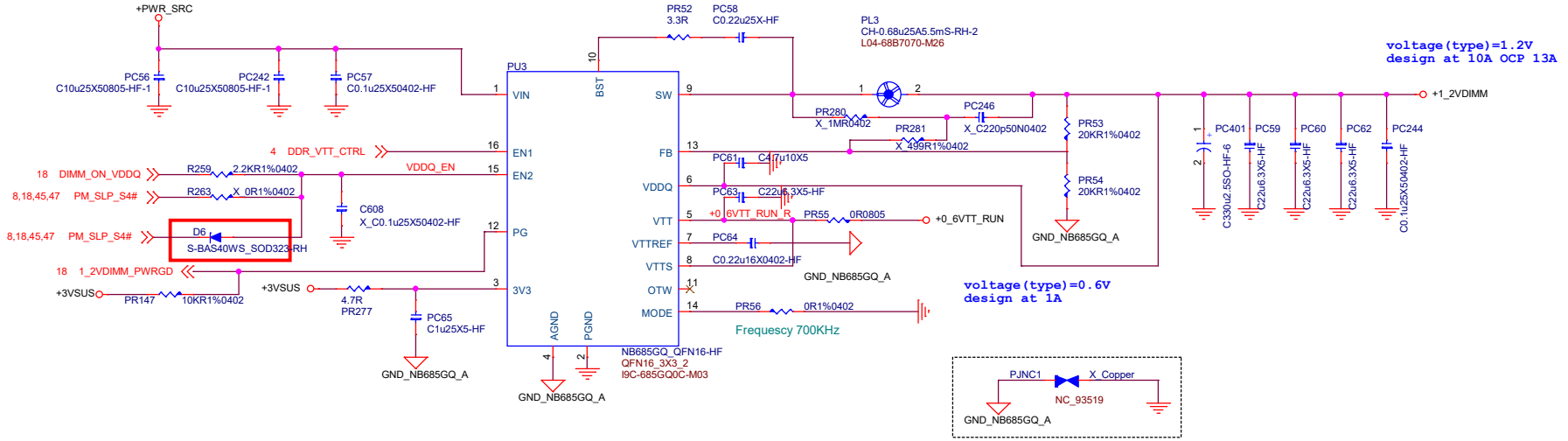

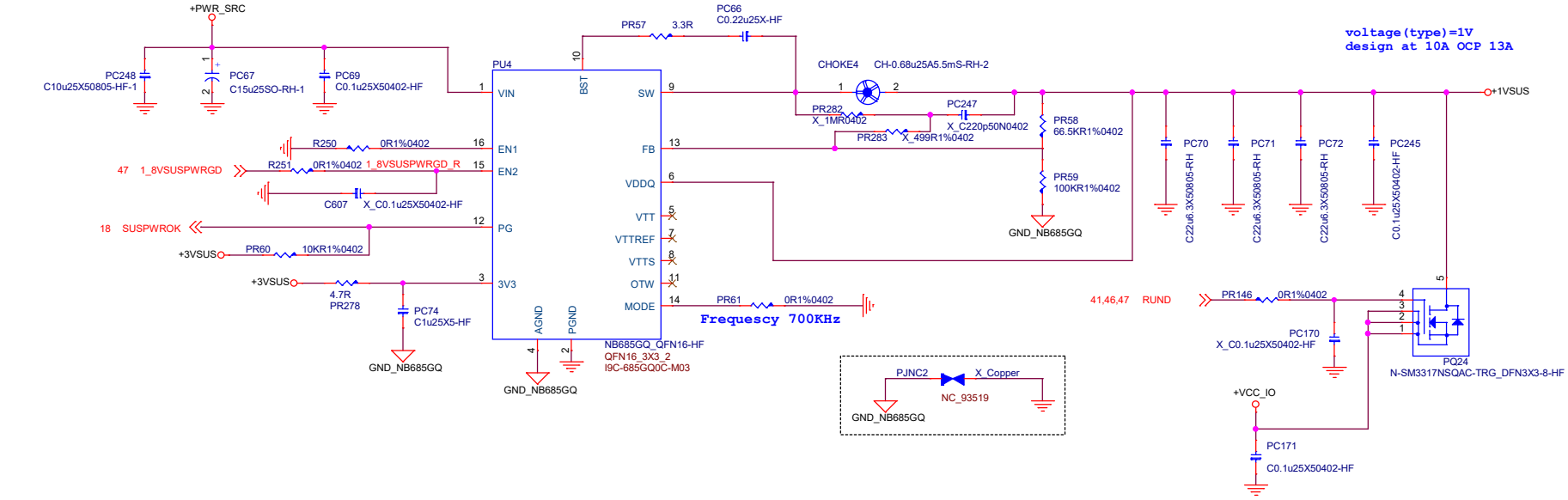

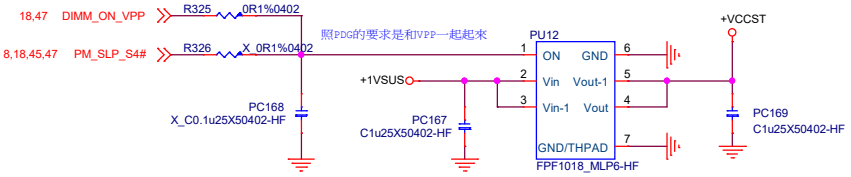

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Size: Custom	Document Number: MS-14B1		Rev: 0C
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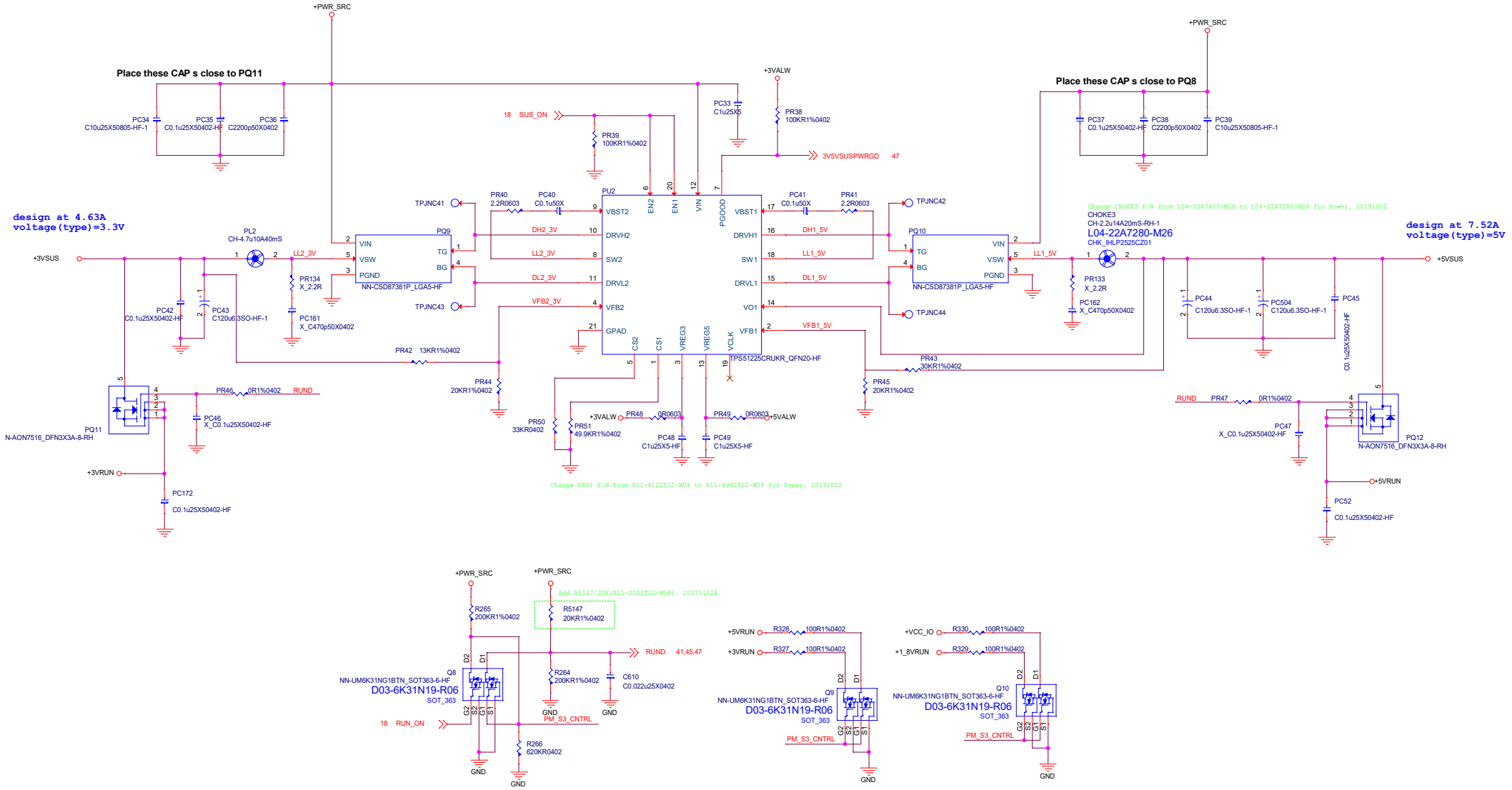

MSI	MICRO-STAR INT'L CO.,LTD.		
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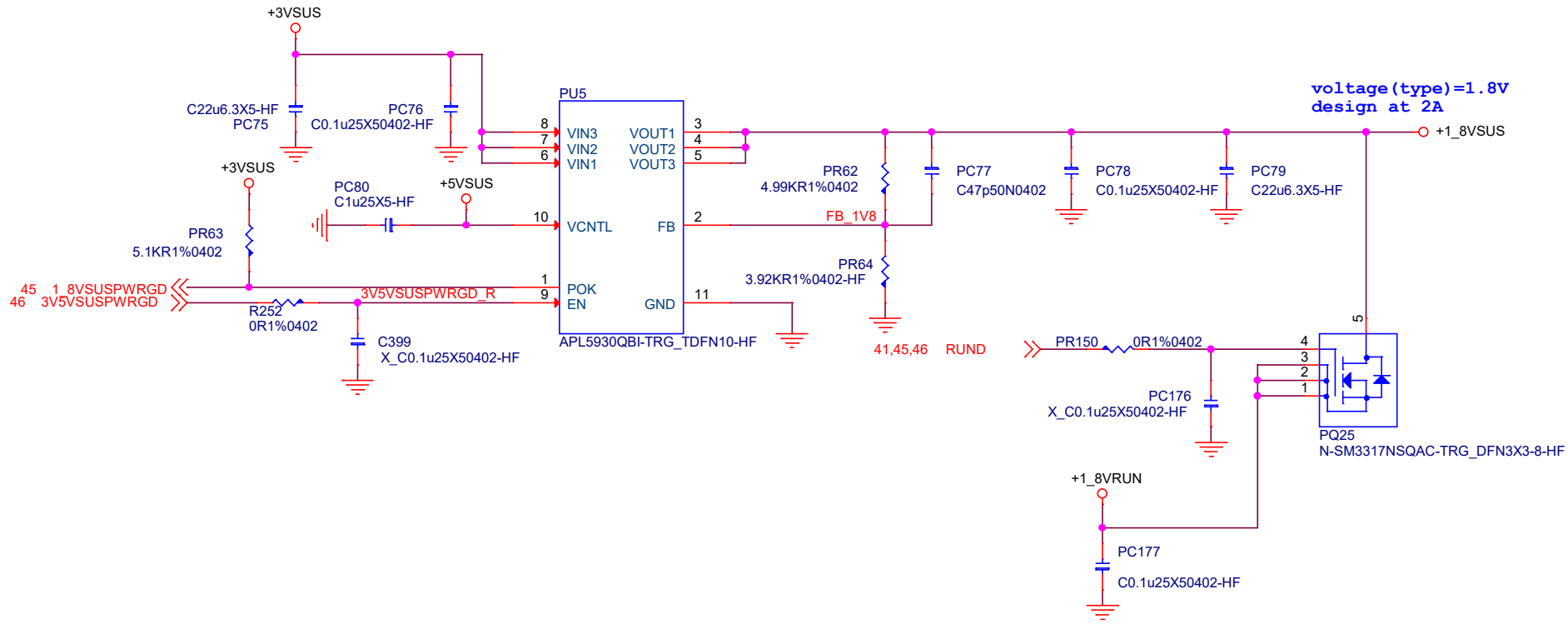
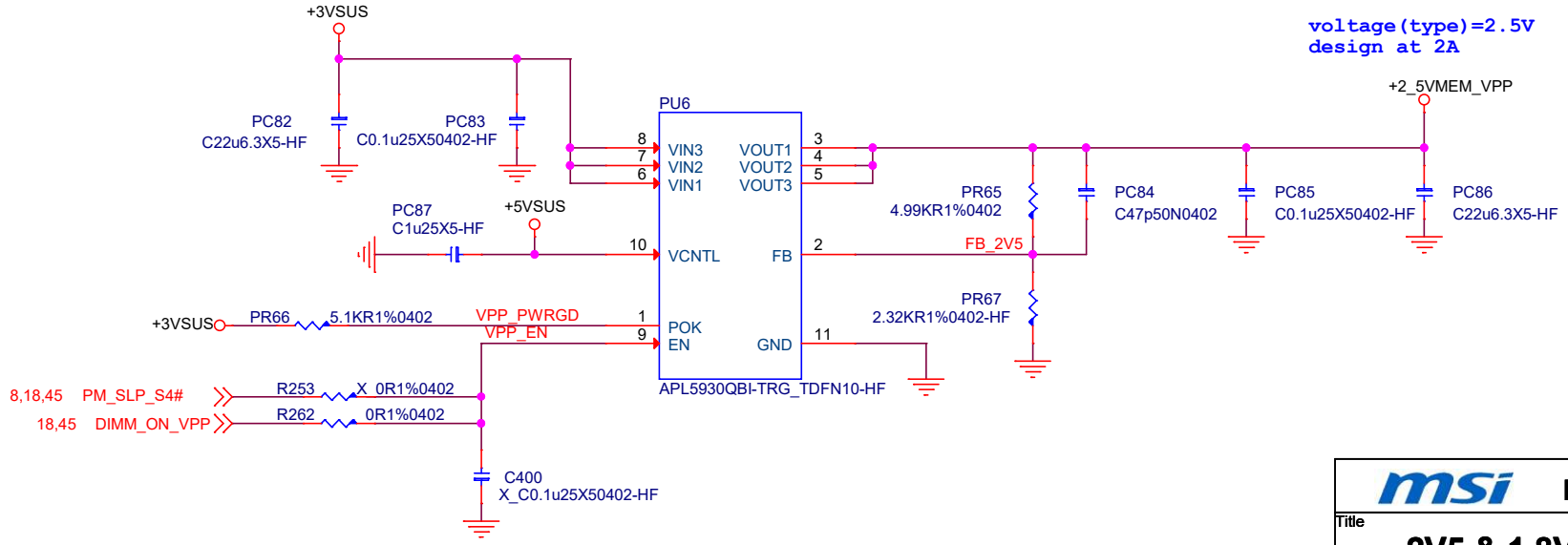
Size: Custom	Document Number: MS-14B1	Rev: 0C	
Date: Thursday, December 21, 2017	Sheet 46 of 57		





MICRO-STAR INT'L CO.,LTD.

Title: 2V5 & 1.8VSUS

Size	Document Number	Rev
Custom	MS-14B1	0C

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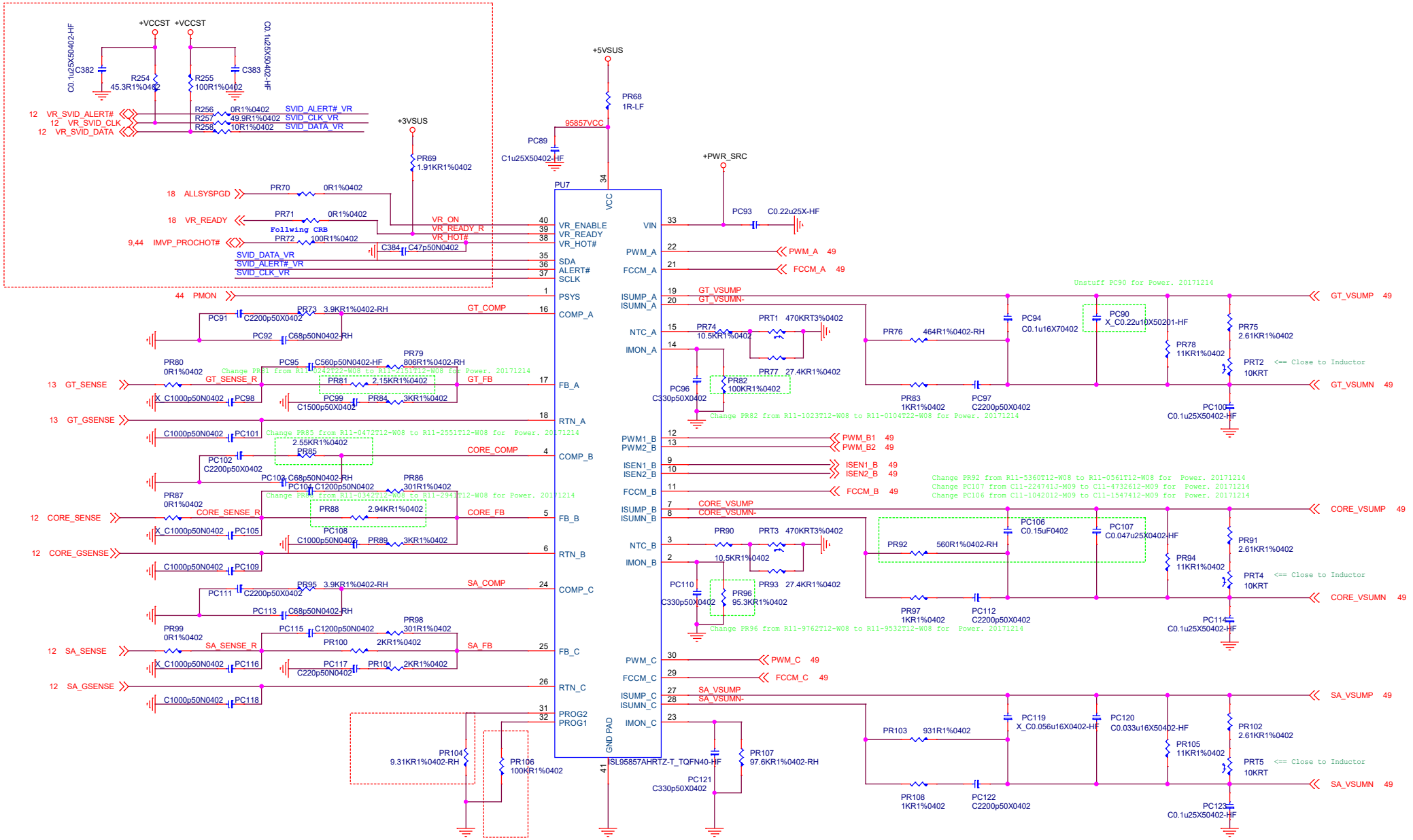

MICRO-STAR INT'L CO.,LTD.		
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Size: Custom	Document Number: MS-14B1	Rev: 0C
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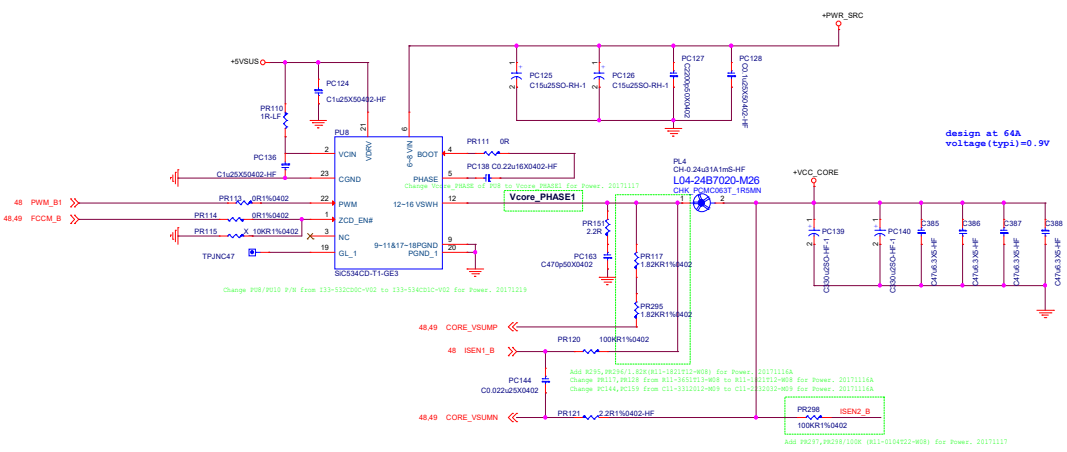

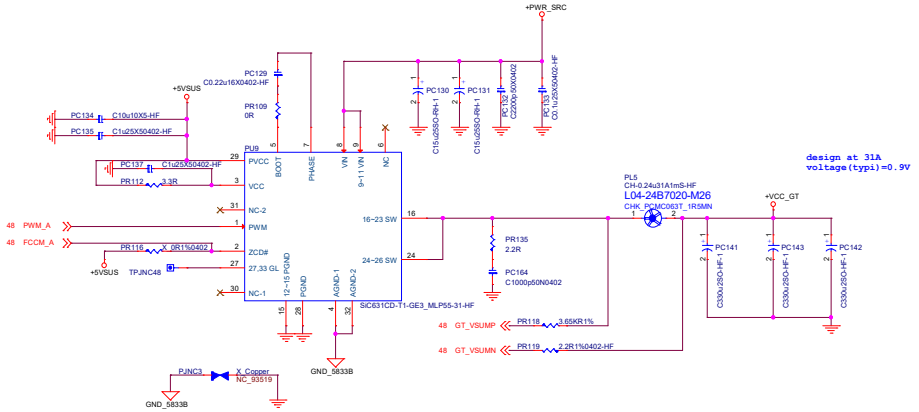

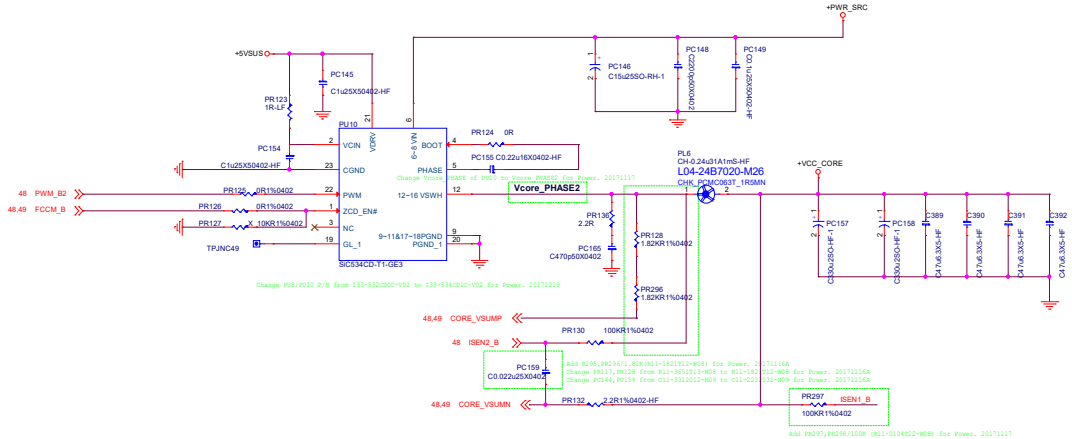

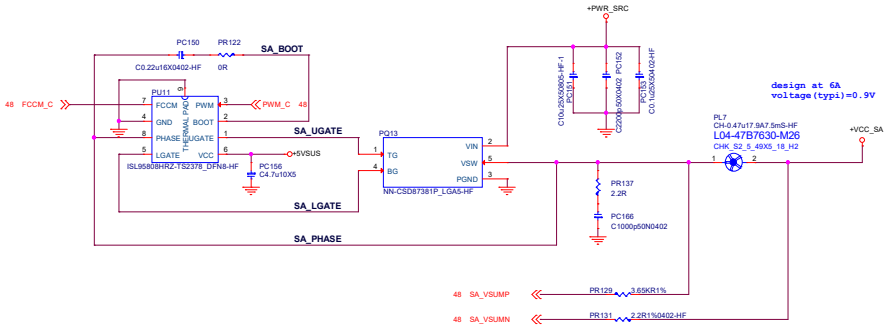

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Size	Document Number		Rev
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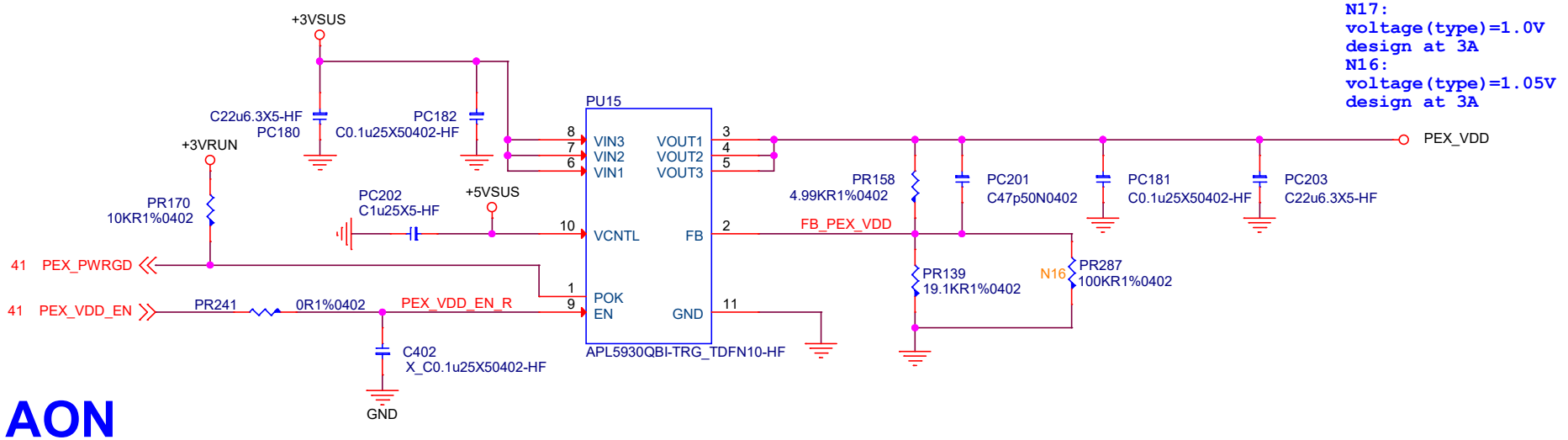
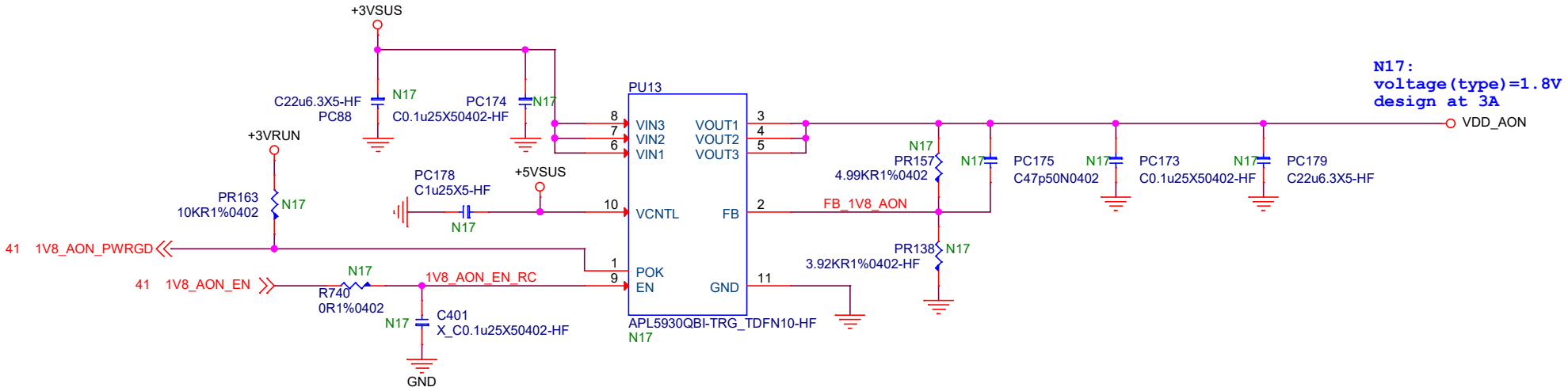
PEX_VDD



1V8_AON



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Title: DGPU POWER PEX_VDD/1V8_AON		
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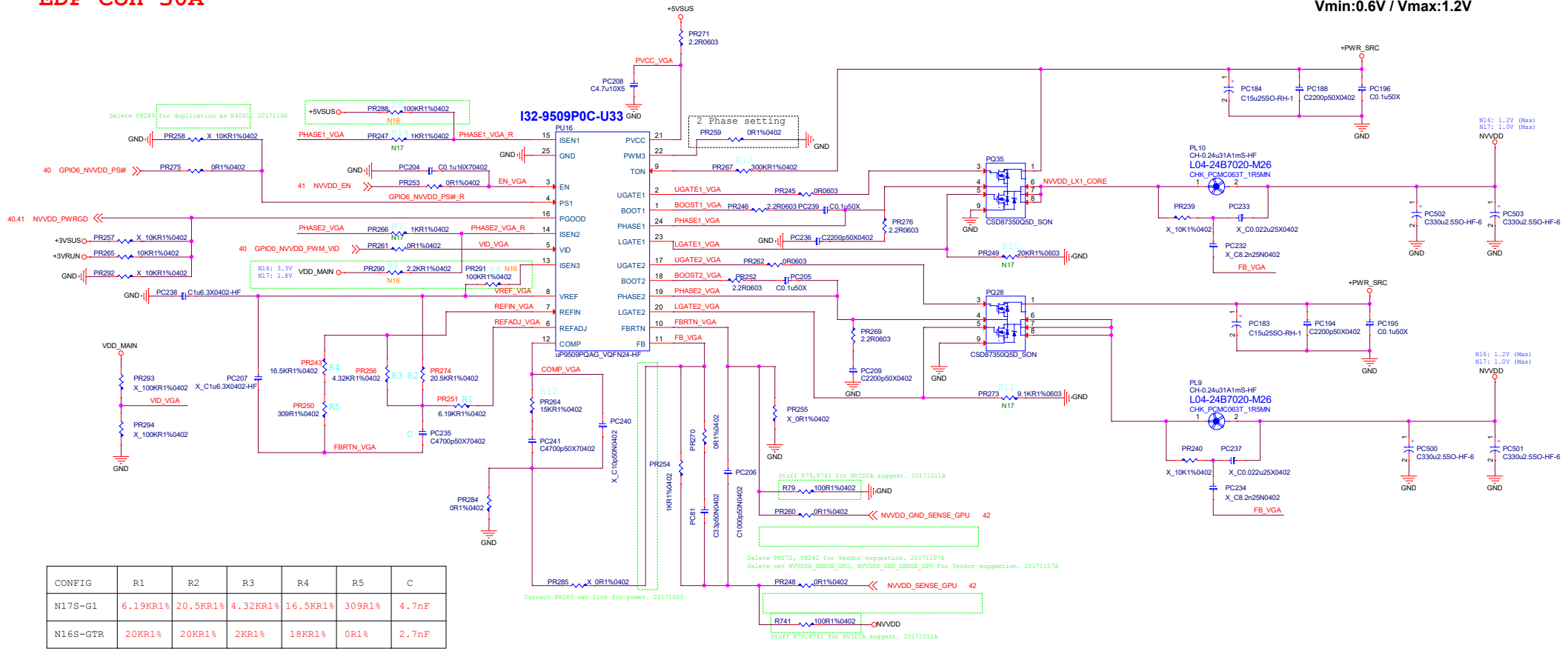
DGPU POWER NVVDD

CONFIG A
VBoot: N16S-0.9V, N17S-0.8V
Vmin:0.6V / Vmax:1.2V

EDP-Peak 60.1A
EDP-Con 30A



CONFIG	R1	R2	R3	R4	R5	C
N17S-G1	6.19KR1%	20.5KR1%	4.32KR1%	16.5KR1%	309R1%	4.7nF
N16S-GTR	20KR1%	20KR1%	2KR1%	18KR1%	0R1%	2.7nF

CONFIG	R6	R7	R8	R9	R10	R11	R12	R13	R14
N17S-G1	NC	1KR1%	NC	NC	20KR1%	9.1KR1%	15KR1%	300KR1%	1KR1%
N16S-GTR	100KR1%	NC	2.2KR1%	100KR1%	NC	NC	20KR1%	91KR1%	NC

N17

R1	R2	R3	R4	R5	C	PWM	R12	R13
X_6.19KR1%0402	X_20.5KR1%0402	X_4.32KR1%0402	X_16.5KR1%0402	X_309R1%0402	X_C4700p50X70402	X_uP9509PQAG_VQFN24-HF	X_15KR1%0402	X_300KR1%0402
R11-6191T12-W08	R11-2052T12-W08	R11-4321T12-W08	R11-1652T12-W08	R11-3090T12-R01	C11-4722812-M09	I32-9509P0C-U33	R11-0153T12-W08	R11-0304T12-W08
N17	N17	N17	N17	N17	N17	N17	N17	N17

N16

R1	R2	R3	R4	R5	C	PWM	R12	R13
X_20KR1%0402	X_20KR1%0402	X_2KR1%0402	X_18KR1%0402	X_0R1%0402	X_C2700p50X_0402-RH	X_UP1642PQAG_VQFN24-HF	X_20KR1%0402	X_91KR1%0402
R11-0203T12-W08	R11-0203T12-W08	R11-0202T12-W08	R11-0183T12-W08	R11-0000T12-Y01	C11-2722812-W08	I32-1642P0C-U33	R11-0203T12-W08	R11-0913T12-W08
N16	N16	N16	N16	N16	N16	N16	N16	N16

190.Change R1A name to N17R1 for BOM. 20171127.
191.Change R1B name to N16R1 for BOM. 20171127.
192.Change R2A name to N17R2 for BOM. 20171127.
193.Change R2B name to N16R2 for BOM. 20171127.
194.Change R3A name to N17R3 for BOM. 20171127.
195.Change R3B name to N16R3 for BOM. 20171127.
190.Change R4A name to N17R4 for BOM. 20171127.
191.Change R4B name to N16R4 for BOM. 20171127.
192.Change R5A name to N17R5 for BOM. 20171127.
193.Change R5B name to N16R5 for BOM. 20171127.
194.Change R12A name to N17R12 for BOM. 20171127.
195.Change R12B name to N16R12 for BOM. 20171127.
194.Change R13A name to N17R13 for BOM. 20171127.
195.Change R13B name to N16R13 for BOM. 20171127.

以後注意Option的Location不要選會跟其他Location撞到的，因為程式不會分A/B。

MICRO-STAR INT'L CO.,LTD.

Title: DGPU POWER NVVDD

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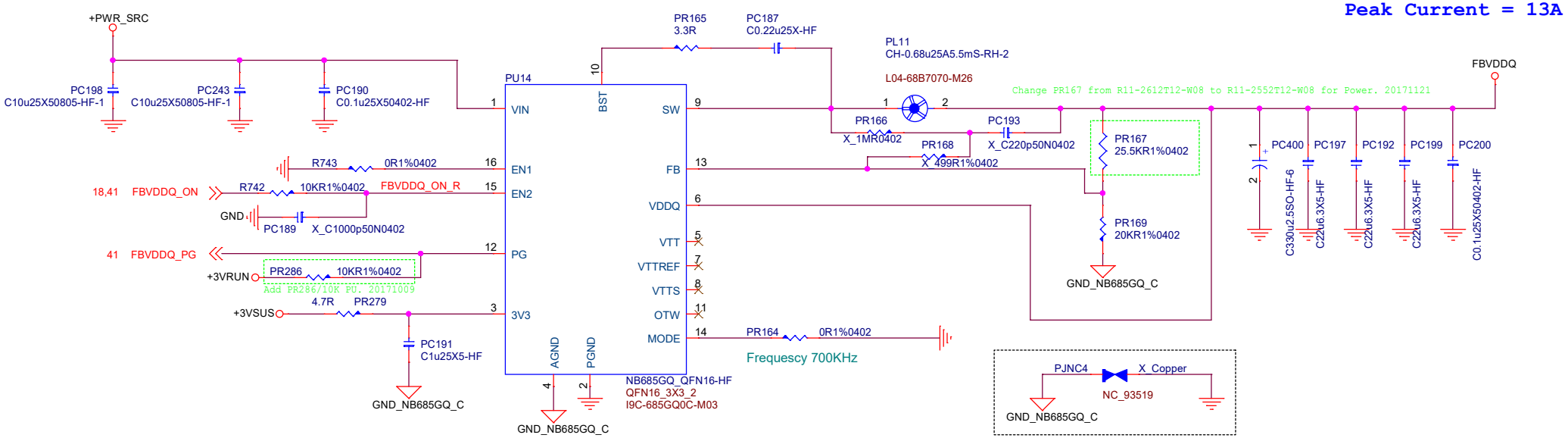
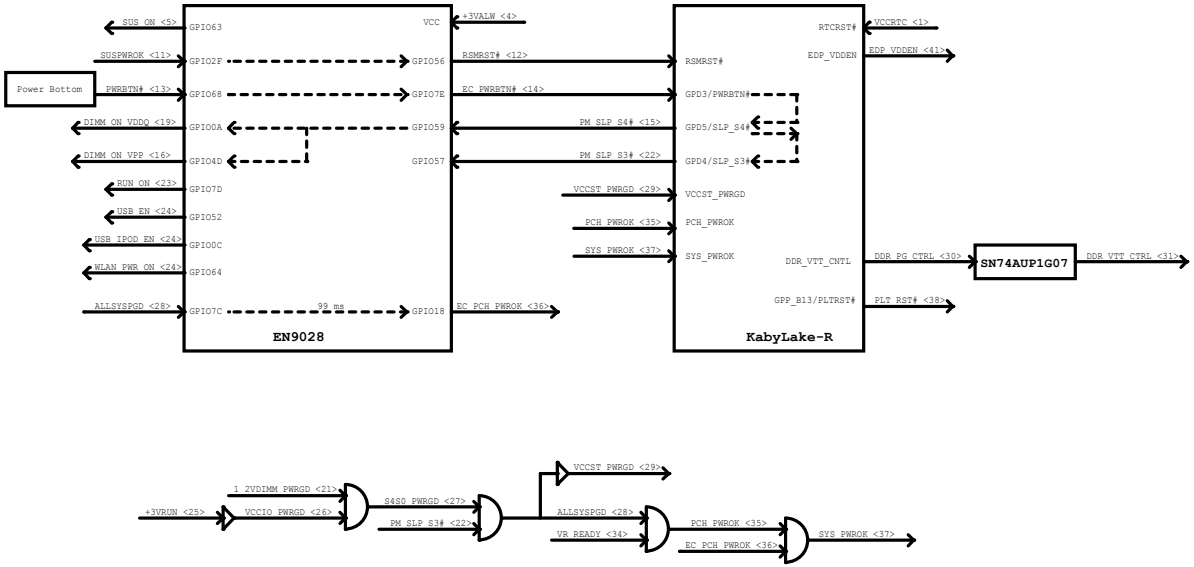
FBVDDQ POWER

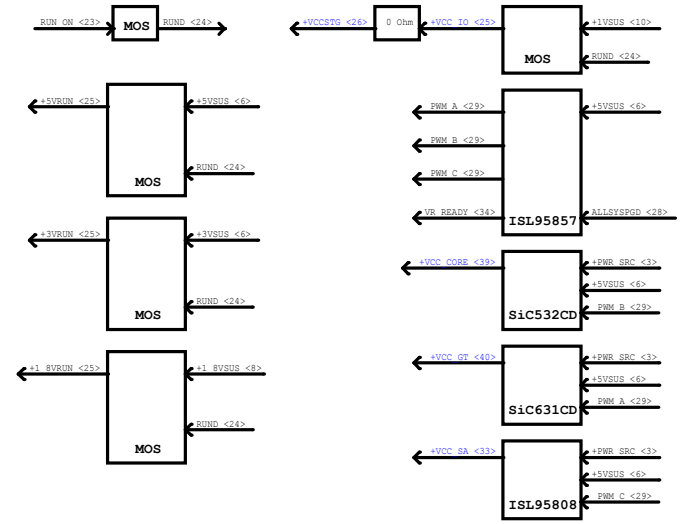
FBVDDQ
Voltage = 1.35V
AVG Current = 10A
Peak Current = 13A



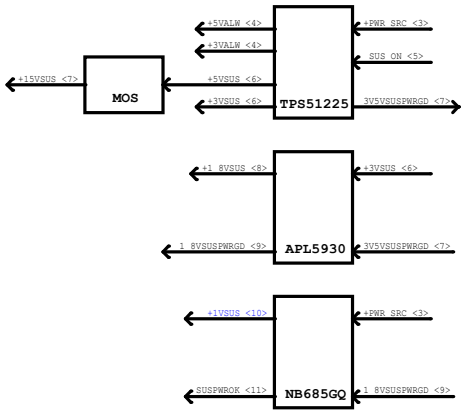
MICRO-STAR INT'L CO.,LTD.			
Title: DGPU POWER FBVDDQ			
Size: Custom	Document Number: MS-14B1		Rev: 0C
Date: Thursday, December 21, 2017	Sheet 52 of 57		



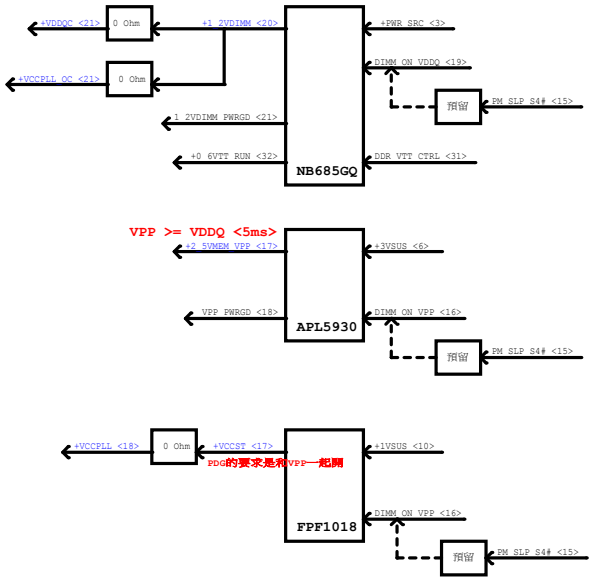
S0

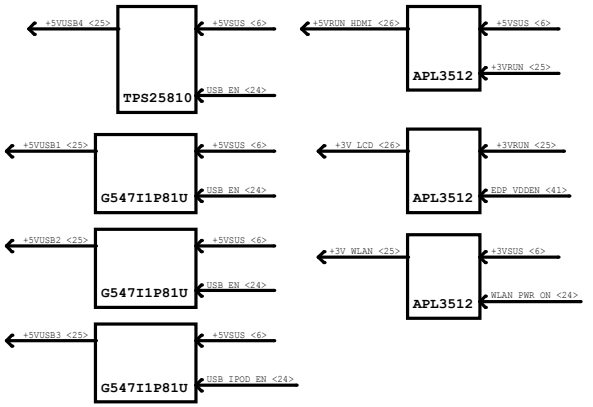


S4/S5



S3





MICRO-STAR INT'L CO.,LTD.

Title: Power on Block Diagram

Size	Document Number	Rev
Custom	MS-14B1	0C

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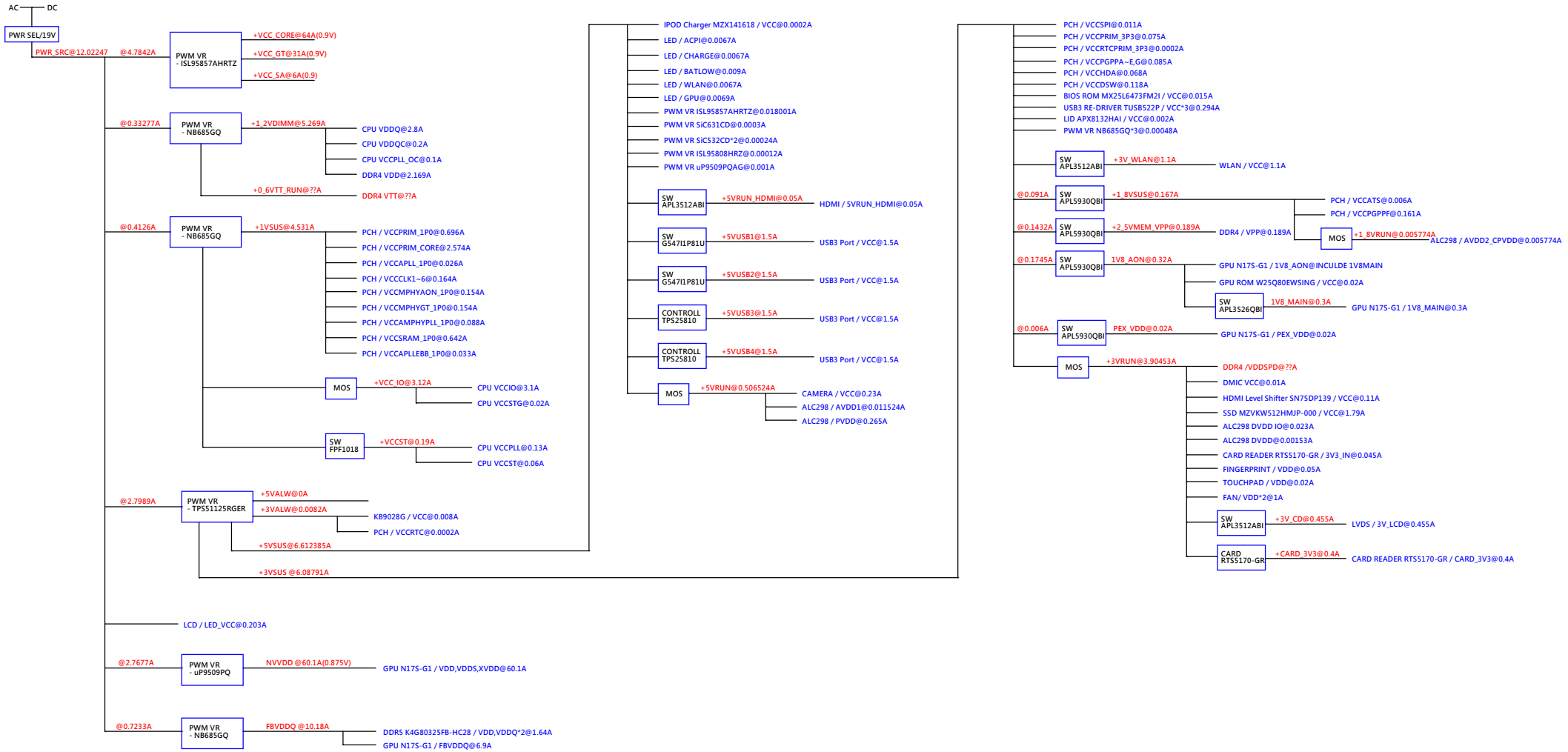
14B1 Power Delivery Chart

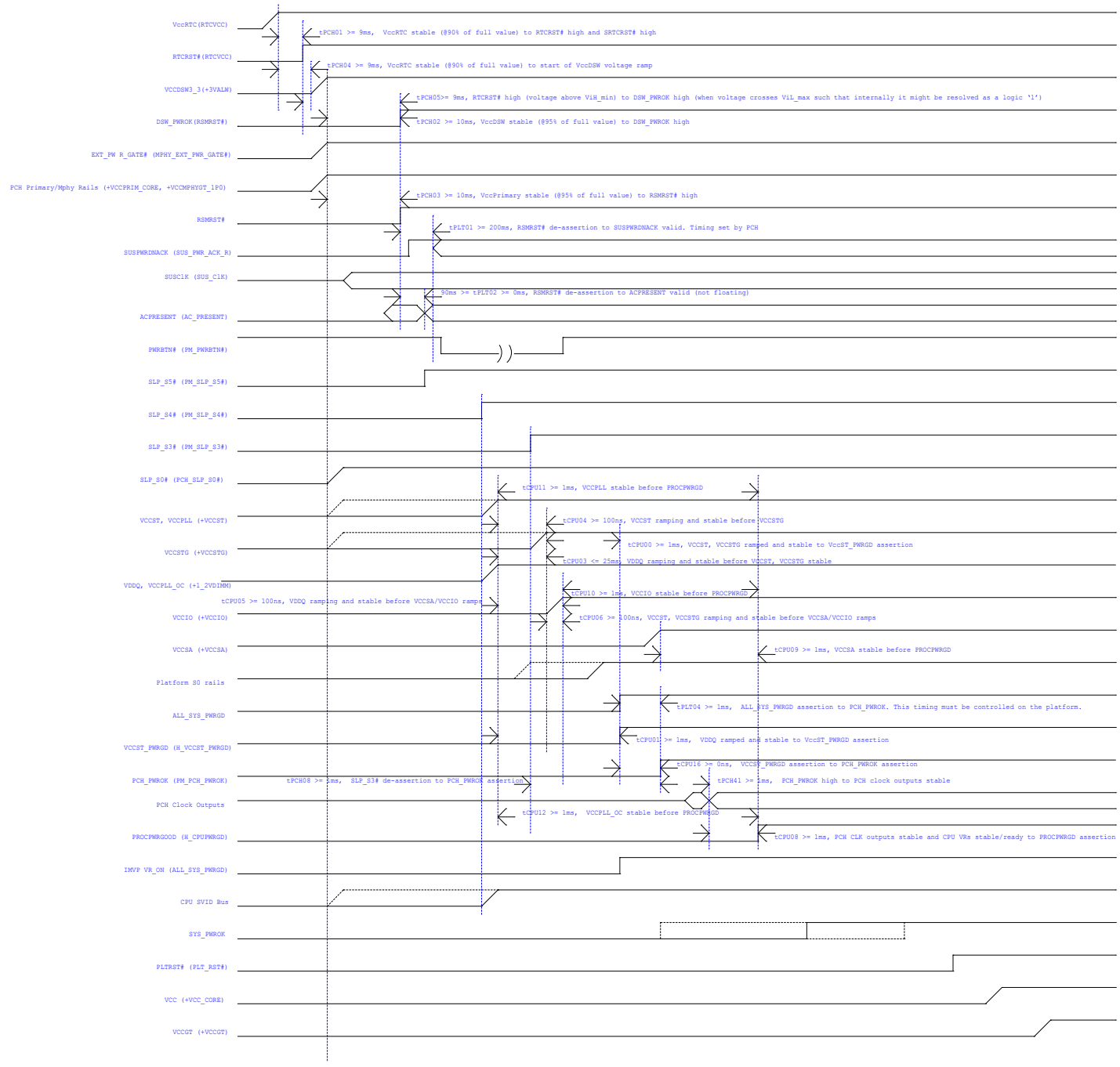


MICRO-STAR INT'L CO.,LTD.

Power Delivery Chart

MS-14B1

G3 to S0



MICRO-STAR INT'L CO.,LTD.

Title: G3 into S0 without M

Size	Document Number	Rev
C	MS-14B1	0C

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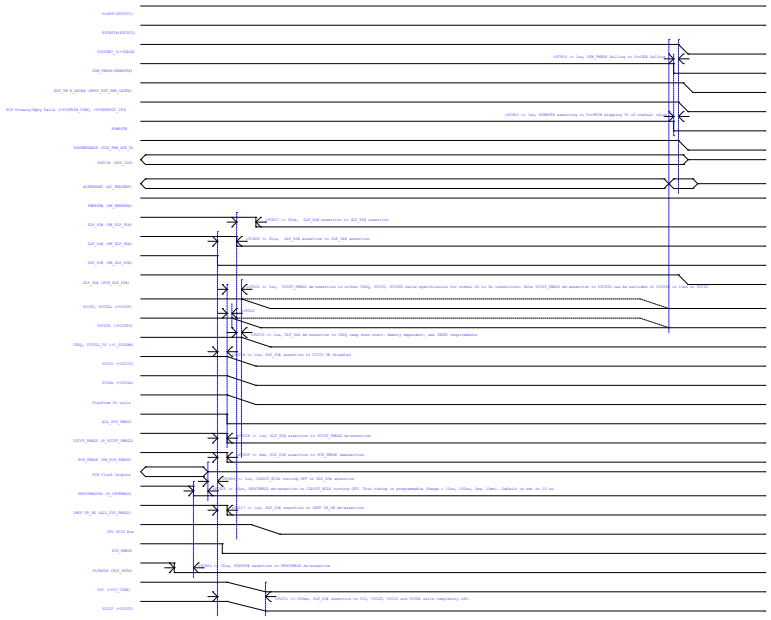
S0 to G3



MICRO-STAR INT'L CO.,LTD.			
Title	S0 into G3 without M		
Size	Document Number		Rev
*	MS-14B1		0C
Date:	Wednesday, December 21, 2022	Sheet	45 of 61

1. Change R311 from 100k to 10k. 20170922
2. Delete R312. 20170922
3. Change R313 from 8.2k to 10k to consider EC current 2~4mA. 20170922
4. Correct CSI2_COMP link. 20170922

5. Change LVDS_BKLTCTL_R net name to EDP_BKLTCTL_R. 20170925

6. Delete Camera power switch circuit. 20170926
7. Add R5035/0R and +3VSSD. 20170926

8. Delete DDR Channel B. 20170927
9. Swap EL17 pin1 <-> pin2, pin3 <-> pin4 for Layout. 20170927

10.Delete C4244/C4243 330UF for Layout. 20170929
11.Change SW1 P/N from N71-0103361-D02 to N71-0101780-D02 for ME. 20170929
12.Place Audio connecter P/N, Footprint. 20170929
13.Add LED5(D0C-040C300-L05), R5036/330R(R11-0331012-W08), ESD39(D0G-01A0510-O05) for ME. 20170929
14.Add TPM(B0C-0966002-I14) cirucit for PM. 20170929
15.Add C5017,C5018/0.1uF(C11-1047612-M09). 20170929
16.Modify Page Size. 20170930

17.Change CHOKE3 P/N from L04-33A7400-M26 to L04-22A7280-M26 for Power. 20191002
18.Change PR51 P/N from R11-4122T12-W08 to R11-4992T12-W08 for Power. 20191002
19.Change U30,U31,U4036,U4035 P/N from I9B-655020C-T07 to I9B-SB5220C-T07 for NRND. 20171002A
20.Delete 4.7K/R244,R243,R5026,R5015 for internal PD. 20171002A
21.Stuff 4.7K/R239,R224,R237,R222,R5010,R5000,R5018,R5002. 20171002A
22.Correct ESD20 power from +5VUSB4 to +5VUSB3. 20171002
23.Add 0.1uF(C11-1047612-M09)/C5019 ~ C5023, C5025,C5026,C5028,C5029. 20171002A
24.Add 10uF(C11-1067312-M09)/C5021,C5024,C5027,C5030. 20171002A

25.Change C4420 from C11-106A233-T04 to C11-226A213-M09 for NVIDIA. 20171003
26.Change C4197 P/N from C11-105A312-S02 to C11-1042012-Y01 for NVIDIA. 20171003
27.Add C5031/0.1uF(C11-1042012-Y01) for NVIDIA. 20171003
28.Change C4000,C4004,C4006,C4007 P/N from C11-106A233-T04 to C11-226A213-M09 for NVIDIA. 20171003
29.Delete ESD17 and chagne USB3_TXN_TYPEC2_U_C/USB3_TXP_TYPEC2_U_C link ESD19 for Layout. 20171003
30.Stuff R4052/10K for NVIDIA. 20171003
31.Unstuff R4050/10K for NVIDIA. 20171003

32.Mark EC SMBus standard mode speed 100kHz. 20171004
33.Change R4273,R4269,R4039,R4043 P/N from R11-0222012-W08 to R11-0202T12-W08 for NVIDIA. 20171004
34.Reserve R5039/0R(R11-0000012-W08) to open Q4024 for NVIDIA. 20171004.
35.Add R5040/0R(R11-0000012-W08) for NVIDIA. 20171004.
36.Add net GPU_OVERT# link EC GPO61 for NVIDIA. 20171004
37.Delete TPJNC19 test. 20171004
38.Change USB1,USB2 P/N from N53-09M1041-AF2 to N53-09M1071-AF2 for ME. 20171004
39.Change CON17 P/N from N5A-08F0160-A81 to N5A-08F0300-A81 for ME.20171004

40.Correct PR285 net link for power. 20171005

41.Add PR286/10K PU. 20171009
42.Net FBVDDQ_ON connect to EC/GPIO7A. 20171009

43.Reserve C5032/10pF. 20171011
44.Add H_R276D118_N*14, NPTH98*3. 20171011

45.Change C4060 from C11-475A323-T04 to C11-105A312-S02 for NVIDIA suggest. 20171011A
46.Stuff C4058,C4411,C4057 for NVIDIA suggest. 20171011A
47.Stuff C4078,C4127,C4433,C4120 for NVIDIA suggestion. 20171011A
48.Stuff C4424 for NVIDIA suggest. 20171011A
49.Stuff R79,R741 for NVIDIA suggest. 20171011A
50.Change R4201,R4207 from R11-1210T12-Y01 to R11-0121T12-W08 for NVIDIA suggest. 20171011A
51.Unstuff R4044/10KR for NVIDIA suggest. 20171011A52
52.Change footprint fromt H_R236142_PB to H_R236D142_PB_N for Layout. 20171011A

53.Swap EL17 pin1 <-> pin2, pin3 <-> pin4 for Layout. 20171012

54.Swap net CON22 MP <--> MQ. 20171012A
55.Add R5041/0R (R11-0000013-W08) for vendor suggestion. 20171012A
56.Add R274,R288/100K1% for vendor suggestion. 20171012A
57.Change R281 from R11-0000T12-Y01 to R11-0204T12-W08 for vendor suggestion. 20171012A
58.Change R286 from R11-0000T12-Y01 to R11-0104T22-W08 for vendor suggestion. 20171012A

59.Unstuff R5028,R5029 and stuff U35. 20171012B
60.Correct USB1,USB2 P/N from N53-09M1041-AF2 to N53-09M1071-AF2 for ME. 20171012B
61.Change CON22 P/N from N54-06F1380-SL0 to N54-06F1641-SL0 for ME.20171012B

62.Stuff R48/10K for INTEL suggestion. 20171013
63.Add U3 re-driver for USB3 typeA prot1, port2 for TCL. 20171013

64.Change UME1,2,7,8,9,10,11,12 footprint from H_R236D142_PB to H_R236D142_PB_N. 20171013A
65.Correct UME3,13,14,15,16,17,18,19,20,21,22,23,24,25 footprint from H_R236D142_PB_N to H_R276D118_N. 20171013A
66.Delete AC_DET#, PR9(R11-0103012-W08), PQ5(D03-02N0600-R06), PR8(R11-0104042-W08), PR14(R11-0104042-W08), PC11(C11-4722022-M09). 20171013A
67.Delete PM_BATLOW#. 20171013A
68.Modify GPIO12_ACIN circuit. 20171013A

69.Change CON12 P/N from N32-1090170-A81 to N32-1080670-A81 for ME. 20171014
70.Add UME29(EZB-16K1010-A89) for ME. 20171014
71.Reserve EC77, EC78, EC2, EC3, EC81, EC79, EC80, EC81/10P(C11-1001012-S02) for EMI. 20171014
72.Reserve EC1/330P(C11-3312012-W08) for EMI. 20171014
73.Add net name TP_CLK_R, TP_DATA_R. 20171014

74.Update Properties CGF. 20171016
75.Change Q1.G power from +3VRUN to +5VRUN. 20171016
76.Correct SW1 circuit. 20171016
77.Add GPIO64 test point. 20171016
78.Change WLAN_PWR_ON to GPIO2A for EC. 20171016
79.Swap EC_RTC_RST and PWRBTN# pin for EC. 20171016
80.Add R5071/170K(R11-0104042-W08). 20171016
81.Change BAT1 P/N from D06-0104701-K26 to D06-0105701-K26. 20171016
82.Change RX1 name to R5072. 20171016
83.Change CON12 P/N from N32-1080670-A81 to N32-1090170-A81 for ME. 20171016
84.Add SW2(N71-0102200-F10), R5073/0R(R11-0000012-W08), C5047/0.1u(C11-1047612-M09). 20171016
85.Delete TPJNC30. 20171016

86.Change C4436 from C11-106A233-T04 to C11-475A323-T04 for NVIDIA suggestion. 20171017
87.Stuff C4123, C4124, C4017 for NVIDIA suggestion. 20171017
88.Mirror CON16 vertical for FFC. 20171017
89.Mirror CON1 vertical for cable. 20171017

90.Delete USB3 TYPE-A2 Re-driver circuit. 20171017A

91.Unstuff R310/10K. 20171018
92.Delete net CLK_PCI_TPM/CLK_PCI_TPM_R and TPM circuit for Layout space. 20171018

93.Delete J40/L5_3.5mil_50_Ohm, J6/L6_3.5mil_50_Ohm. 20171019
94.Change UME14, UME15, UME23 footprint to H_R276D118_V5 for EMI. 20171019
95.Change UME13, UME16 footprint to H_R276D118_V8_N for EMI. 20171019
96.Add X1~4 footprint H_NR118D118. 20171019

97.Change POWER_LED# net name to GPU_LED#. 20171019A
98.Change C0402/F_C0402 footprint to C0402_MXM_1. 20171019A
99.Change R0402/F_R0402 footprint to R0402_MXM_1. 20171019A
100.Change L0402 footprint to L0402_MXM_1. 20171019A

101.Change CPU2 P/N from A0C-8250U05-I06 to OAC-14B1001-I06 for PM. 20171020
102.Add test point TPJNC4024. 20171020
103.Change R167 P/N from R11-0000013-W08 to R11-0430012-W08. 20171020
104.Unstuff R299. 20171020
105.Delete R4047. 20171020
106.Delete EC36~EC43/100p(C11-1011032-W08). 20171020
107.Add ESD40,ESD41(D0G-01A0510-O05). 20171020

108.Correct UME13,UME14,UME15,UME16,UME23 library. 20171020A

109.Change P/N from C11-4764223-M09 to C11-4767313-M09. 20171023
110.Stuff C4492, C4207, C4204 for vendor suggestion. 20171023A

111.Reserve EC82~89/0.1uF for EMI. 20171024
112.Update R,C main P/N. 20171024

113.Delete EL4~7(L12-9008100~I05) for Layout. 20171024A
114.Add SPRING1,2 P/N:E23-1004060-CA7 for EMI. 20171024A
113.Delete FM1 for Layout. 20171024A
114.Add FM29~34(F_PAD_NB_2) for Layout. 20171024A

115.Unstuff Q7,Q11(D03-5121N09~O05), R215,R627(R11-0104T22-W08), R216,R628(R11-0102T12-W08). 20171024B

116.Delete FM33,FM34 for Layout. 20171025
117.Change R120 P/N from R11-0221T12-Y01 to R11-0221T12-W08. 20171025

118.Delete FM24, FM26, FM29, FM32 for Layout. 20171026

119.Update D,T component main P/N. 20171026A

120.Change PC132,PC127,PC152,PC148,PC209,PC236,PC194,PC188,PC111,PC122,PC91,PC102,PC112,PC97,PC36,PC38,PC3 P/N to C11-2222022-T04. 20171027
121.Change PC113,PC92,PC103 P/Nto C11-6801812-T04. 20171027
122.Change PC401,PC500,PC503,PC502,PC501,PC400 P/N to C71-331024G-P01. 20171027
123.Change D4 P/N to D01-BAV9919-P03. 20171027
124.Change R121 P/N to R11-562AT12-W08. 20171027

125.Change UME23, UME14, UME15 footprint to H_R276D118_V5_N for Layout. 20171030
126.Change UME29 footprint to H_R201D118_PT_N for Layout. 20171030

127.Update Power Delivery Chart. 20171030A

128.Modify GPU Strap pin. 20171031
129.Modify GPU PCI EXPRESS. 20171031
130.Note N16 ROM P/N:M31-25X2023-W03,2Mb(256Kx8bit). 20171031

131.Modify GPU POWER RAIL DECOUPLING AND FILTERING. 20171101
132.Modify GPIO DIFFERNCES. 20171101

133.Add N16 Power Sequence 3V3_AON, 3V3_MAIN. 20171101A

134.Add C5049(C11-106A233-T04). 20171102
135.Delete C4488, 4486. 20171102

136.Add PR288,PR291,PR293,PR294/100K(R11-0104T22-W08), PR289,PR290,PR292/10K(R11-0103T12-W08). 20171102A
137.Add R5147/20K(R11-0203T12-W08). 20171102A
138.Add N16 Power Sequence NVVDD, PEX_VDD, FBVDDQ. 20171102A
139.Change CON3 P/N from N5Y-19M0910-KF2 to N5Y-19M1250-AF2 for ME. 20171102A

140.Change R5096 stuff on N17 and N16. 20171103
141.Change L4000 only stuff on N17. 20171103
142.Add R5148 only stuff on N17. 20171103
143.Move R5094 to link Pin.F6. 20171103
144.Unstuff R5092/30.1KR(R11-3012T12-W08) and R5150/200R(R11-0201T12-W08). 20171103
145.Add R5149/4.99K(R11-4991T12-W08). 20171103

146.Add DDR1, DDR2 P/N option. 20171103A

147.Delete DDR1, DDR2 and update N16S DDR5 RVL. 20171103B

148.Delete C5058/4.7uF(C11-475A323-M09) for Vendor suggestion. 20171106
149.Move C4216 on XS PLLVDD for Vendor suggestion. 20171106
150.Stuff C4194, C4173, C4189, C4195 for Vendor suggestion. 20171106
151.Add C5070/47u(C11-4767313-M09) for N16S. 20171106
152.Delete PR289 for duplication as R4061. 20171106
151.Stuff C4094 for Vendor suggestion. 20171106
152.Stuff C4096/10uF. 20171106
153.Stuff C4156, C4157, C4067 for N17S, C4157 for N16S. 20171106
154.Stuff C4016, C4011, C4009, C4002. 20171106
155.Stuff C4023, C4020, C4021. 20171106
156.Stuff C4004, C4006, C4007, C4022, C4000. 20171106
157.Delete R5117, R5118, R4287 for Vendor suggestion. 20171106
158.Delete R5121, R5122, R4044 for Vendor suggestion. 20171106
159.Delete R5125 and net GPIO16_N17 for Vendor suggestion. 20171106
160.Delete R5127 and net GPIO23_N17 for Vendor suggestion. 20171106

161.Unstuff R4301,R4302 for Vendor suggextion. 20171107

162.Delete R4997, R4996 for Vendor suggextion. 20171107A
163.Change VDDS_SENSE/GNDS_SENSE link to VDD_SENSE/GND_SENSE for Vendor suggestion. 20171107A
164.Delete PR27Z, PR242 for Vendor suggestion. 20171107A
165.Delete net NVVDDS_SENSE_GPU, NVVDDS_GND_SENSE_GPU for Vendor suggestion. 20171107A

166.Moidfy Power NVVDD configuration. 20171108
167.Unstuff 1V8_AON on N16S. 20171108

168.Stuff PR247 on N17 only. 20171109

169.Add CFG_N17S_i7, CFG_N17S_i5, CFG_N16S_i7, CFG_N16S_i5 configuration. 20171114

170.Camera move to Page. 31 for ME. 20171116
171.Add Camera CON26 for ME. 20171116

172.Add R295,PR296/1.82K(R11-1821T12-W08) for Power. 20171116A
173.Change PR117,PR128 from R11-3651T13-W08 to R11-1821T12-W08 for Power. 20171116A
174.Change PC144,PC159 from C11-3312012-M09 to C11-2232032-M09 for Power. 20171116A

174.5hange PR117,PR295,PR128,PR296 footprint R0402 to R0402_MXM_1 for Layout. 20171116B

179.Change LED1,LED2,LED3 P/N from D0C-0405800-L05 to D0C-040C300-L05 for ME. 20171117A
180.Change LED4 P/N from D0C-0405400-L05 to D0C-0403800-L05 for ME. 20171117A

181.Add GPU2 P/N B03-0N16S45-N08. 20171117B

182.Change PR167 from R11-2612T12-W08 to R11-2552T12-W08 for Power. 20171121
183.Change PCB1 from PD0-14B110A-H73 to PD0-14B110B-H73. 20171121

184.Change R274,R286 from R11-0104T22-W08 to R11-0000T12-Y01 for Vendor suggestion. 20171121A

185.Update component SMT ASM for Layout. 20171122

186.Change R4013 from R11-422AT12-W08 to R11-402AT12-W08 for Vendor suggestion. 20171123
187.Change C69,C70 from C11-1201012-T04 to C11-1501012-S02 for Vendor suggestion. 20171123

188.Correct PR291 Value. 20171125
189.Unstuff R5142 in N16S. 20171125

190.Change R1A name to N17R1 for BOM. 20171127.
191.Change R1B name to N16R1 for BOM. 20171127.
192.Change R2A name to N17R2 for BOM. 20171127.
193.Change R2B name to N16R2 for BOM. 20171127.
194.Change R3A name to N17R3 for BOM. 20171127.
195.Change R3B name to N16R3 for BOM. 20171127.
190.Change R4A name to N17R4 for BOM. 20171127.
191.Change R4B name to N16R4 for BOM. 20171127.
192.Change R5A name to N17R5 for BOM. 20171127.
193.Change R5B name to N16R5 for BOM. 20171127.
194.Change R12A name to N17R12 for BOM. 20171127.
195.Change R12B name to N16R12 for BOM. 20171127.
194.Change R13A name to N17R13 for BOM. 20171127.
195.Change R13B name to N16R13 for BOM. 20171127.

196.Stuff C673/330P P/N:C11-3311812-M09. 20171207
197.Add net LID# EC for leakage of Click PAD. 20171207
198.Change NV ROM P/N:M31-2006E02-M24 in N16S. 20171207
199.Delete U39 ROM SOCKET P/N: N14-0080030-L06. 20171207
200.Stuff U39 BIOS ROM P/N: M31-25L6482-M24. 20171207
201.Change C667/C668 from C11-1501012-S02 to C11-47A1812-M09. 20171207
202.Stuff R159 for SA. 20171207
203.Add MYL1(E2P-4B10911-G40), MYL2(E2P-0112911-G40) for ME. 20171207

204.Change CON26 from N5A-10F0240-A81 to N5Q-10F0030-A81 for ME. 20171212
205.Change CON8, CON24 from N53-24M0060-J06 to N53-24M0320-AP2 for ME. 20171212

206.Modify CON26 Library pin number. 20171212A
207.Correct CON26 P/N:N5A-10F0240-A81. 20171212B

208.Change PR81 from R11-0242T22-W08 to R11-2151T12-W08 for Power. 20171214
209.Change PR82 from R11-1023T12-W08 to R11-0104T22-W08 for Power. 20171214
210.Unstuff PC90 for Power. 20171214
211.Change PR88 from R11-0342T12-W08 to R11-2941T12-W08 for Power. 20171214
212.Change PR96 from R11-9762T12-W08 to R11-9532T12-W08 for Power. 20171214
213.Change PC106 from C11-1042012-M09 to C11-1547412-M09 for Power. 20171214
214.Change PC107 from C11-2247413-M09 to C11-4732612-M09 for Power. 20171214
215.Change PR92 from R11-5360T12-W08 to R11-0561T12-W08 for Power. 20171214
216.Change PR85 from R11-0472T12-W08 to R11-2551T12-W08 for Power. 20171214
217.Change PQ2,PQ3 from D03-7422E0C-A68 to D03-3324N0C-ST8 for Power. 20171214

218.Add R5151 and unstuff R5093 for MX130 ID. 20171218
219.Stuff EC1(C11-3312012-M09) for EMI. 20171218

220.Stuff EC44/10p(C11-1001012-S02). 20171219
221.Change PU8/PU10 P/N from I33-532CD0C-V02 to I33-534CD1C-V02 for Power. 20171219
222.Correct LED configuration. 20171219

223.Stuff C636/22pF(C11-2201012-W08) for SA. 20171221
224.Stuff EC19/10pF(C11-1001012-S02) for SA. 20171221
225.Change R85 P/N from R11-0330032-W08 to R11-0220042-W08 for SA. 20171221
226.Stuff EC61~64, EC67/15pF(C11-1501012-S02) for SA. 20171221

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