LCFC NM-D041

Y550 M/B Schematics Document

Renoir H-Processor with DDR4 + NV N18P-G61/G62 GPU

2020-02-24

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title	Cover Page		
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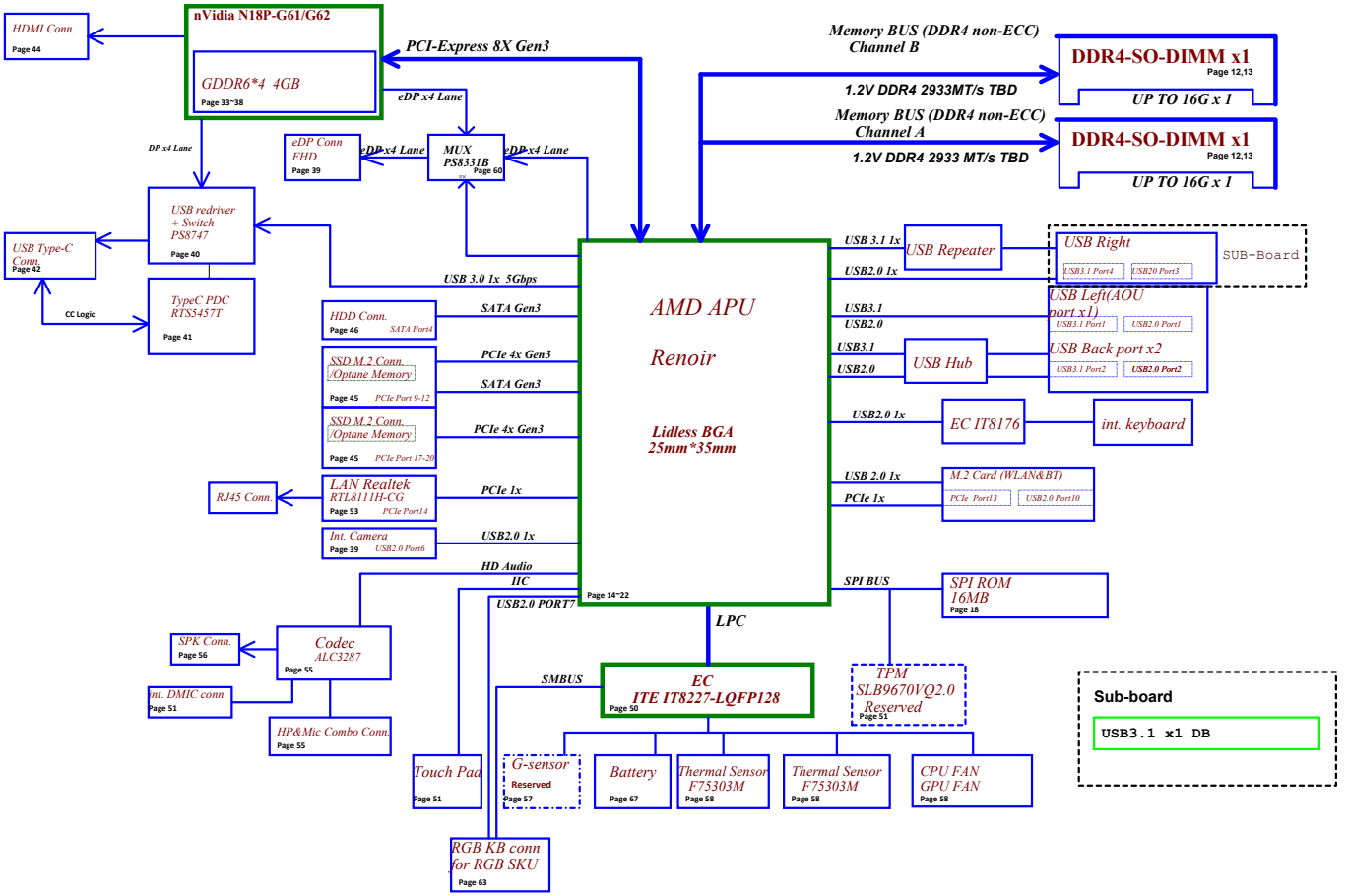

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Title: **Block Diagram**

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW / +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS VCCIO VCCSA VCCSTG VCCCPUCORE VCCGFXCORE +1.8VS_AON +1.8VGS NVVDD +1.0VGS FBVDDQ
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Control Table

BOM Structure	BTO Item
@	Not stuff
15@	15'' Stuff
17@	17'' stuff
7000P@	7000P stuff
7502M@	7502 stuff
8111GUL@	LAN Chip 8111GUL part
8111H@	LAN Chip 8111H part
AG@	Anti-ghost
AOAC@	AOAC support part
BL@	BL
CD@	Cost down part
CNVI@	CNVi support part
DCI@	DCI
Debug@	USB2.0 port 1for Debug
EMC@	EMC part
EMC_8111H@	LAN 8111H EMC Part
EMC_NS@	EMC not stuff
GC6@	GC6
GYSNC@	GSYNC support part
HDMI@	HDMI
i5@i7@i9@	CPU Part
ME@	ME part(connector, hole)
M6GX6@S6GX6@	VRAM part

BOM Structure	BTO Item
MIRROR@	MIRROR
N18EG0@N18EG1@	GPU part
NOMIRROR@	17'' stuff
NPI@	SPI VCC diode stuff
OPT@	For NV GPU part
OPTANE@	Optane memory support part
TPM@	For support TPM sku part
UP9632_@	UP9632 part stuff
USB@	USB2.0 port1 for USB Port
X76@	VRAM
GS@	Reserved for G-sensor

USB2.0 Port table	
Port	Function
1	Back USB3.0
2	Left USB3.0
3	Right USB3.0
4	Type-C Port
5	NA
6	Camera
7:8	NA
9	AG
10	Back USB3.0
11:13	NA
14	BT

USB3.0 Port table	
Port	Function
1	Back USB3.0
2	Type-C Port
3	Left USB3.0
4	Right USB3.0
5	Back USB3.0
6	NA

SATA Port table	
Port	Function
0A	NA
0B	NA
1A	M.2 SSD Gen3
1B	NA
2	NA
3	HDD Gen3
4	NA
5	NA
7	M.2 SSD Gen3

PCIE Port table	
Port	Function
1:8	NA
9	M.2 SSD/Optane
10	M.2 SSD/Optane
11	M.2 SSD/Optane
12	M.2 SSD/Optane
13	WLAN Gen1
14	LAN Gen1
15	Reserved for Card Reader
17:20	M.2 SSD

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Title: **Notes List**

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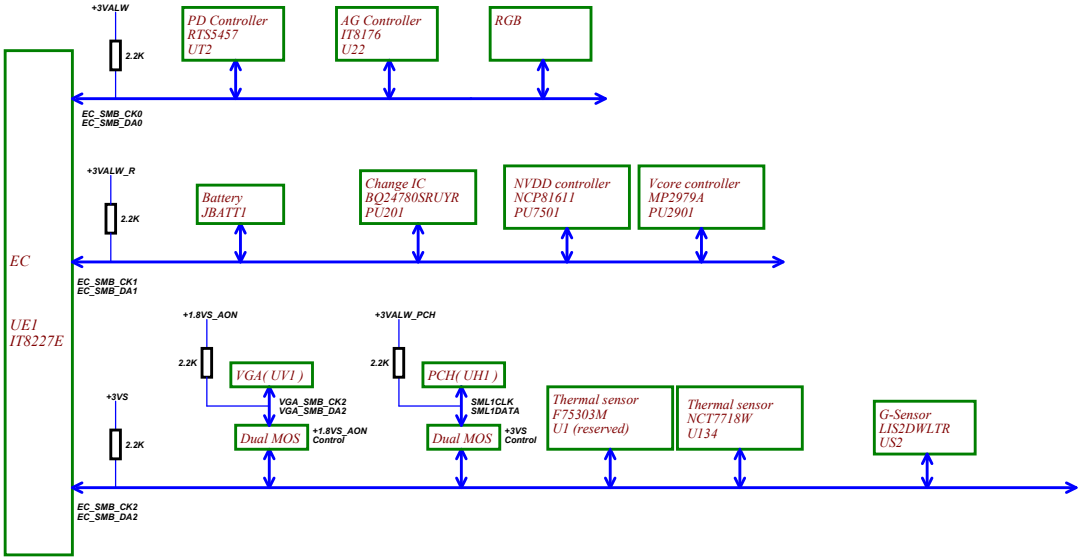

SMBUS Control Table

	SOURCE	VGA	BATT	IT8226E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	Charger	RGB KB Backlight	USB-C PD	HiFi Audio	Anti-ghost
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +5VS	X	V +3VALW_AG
EC_SMB_CK1 EC_SMB_DA1	IT8226E +3VALW_R	X	V +3VALW_R	V +3VALW_R	X	X	X	X	X	V +3VALW_R	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8226E +3VS	V +1.8VS_AON	X	V +3VS	X	X	V +3VS Reserve	V +3VALW_PCH	X	X	X	X	X	X
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW_PCH	X	X	X	V +3VS	X	X	X	V +3VS	X	X	X	X	X
PCH_RSMRST_N1 PCH_RSMRST_N2A	X	X	X	X	X	X	X	X	X	X	V +LDO_3V3	X	X	X
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +5VS	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0B16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001 100x b 0x98 (default)
VGA	Need to update
PCH	1001100xb
Thermal Sensor NCT7718W	

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000X b
DDR DIMMB	1010 001X b
TP Module	Need to update
WLan	Reserved

PCH I2C 2 Bus address

Device	Address
RGB Backlight	Need to update

Security Classification	LC Future Center Secret Data		Title: Blank
Issued Date: 2016/07/02	Deciphered Date: 2016/02/24		
Size: C	Document Number: Y550	Rev: 1A	
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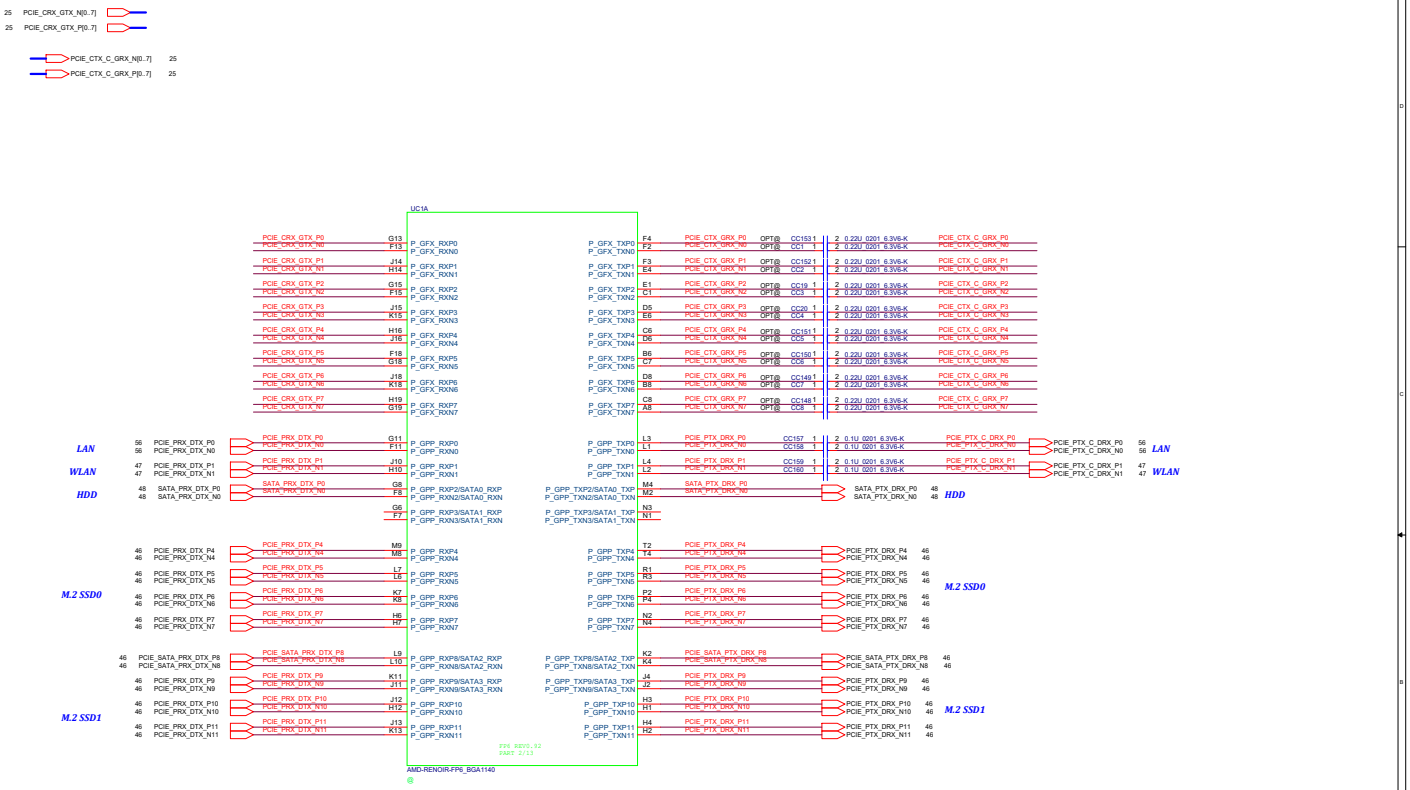

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Title: FP5 (PCIE SATA I/F)

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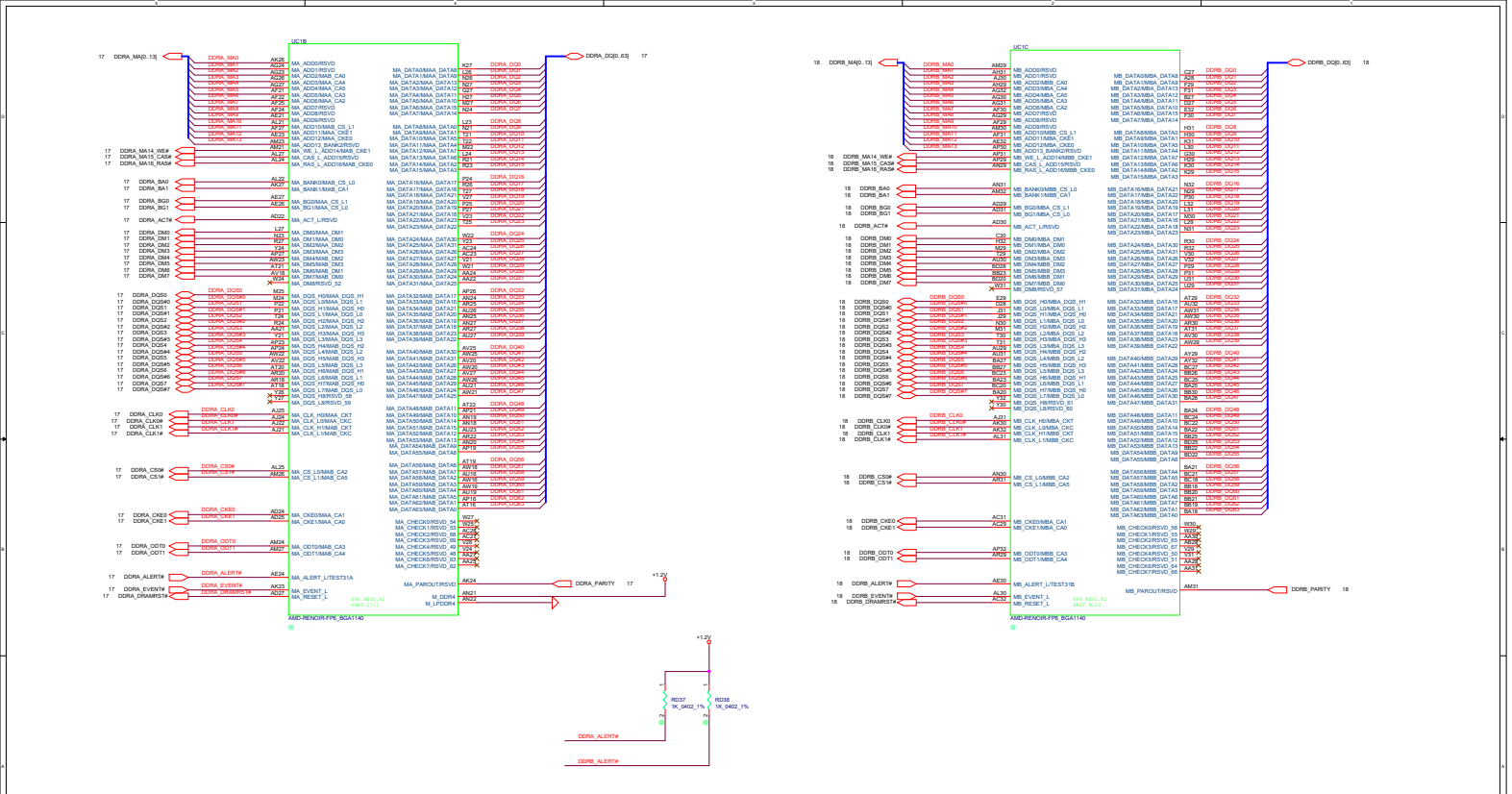

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Title	FP5 (MEM)		
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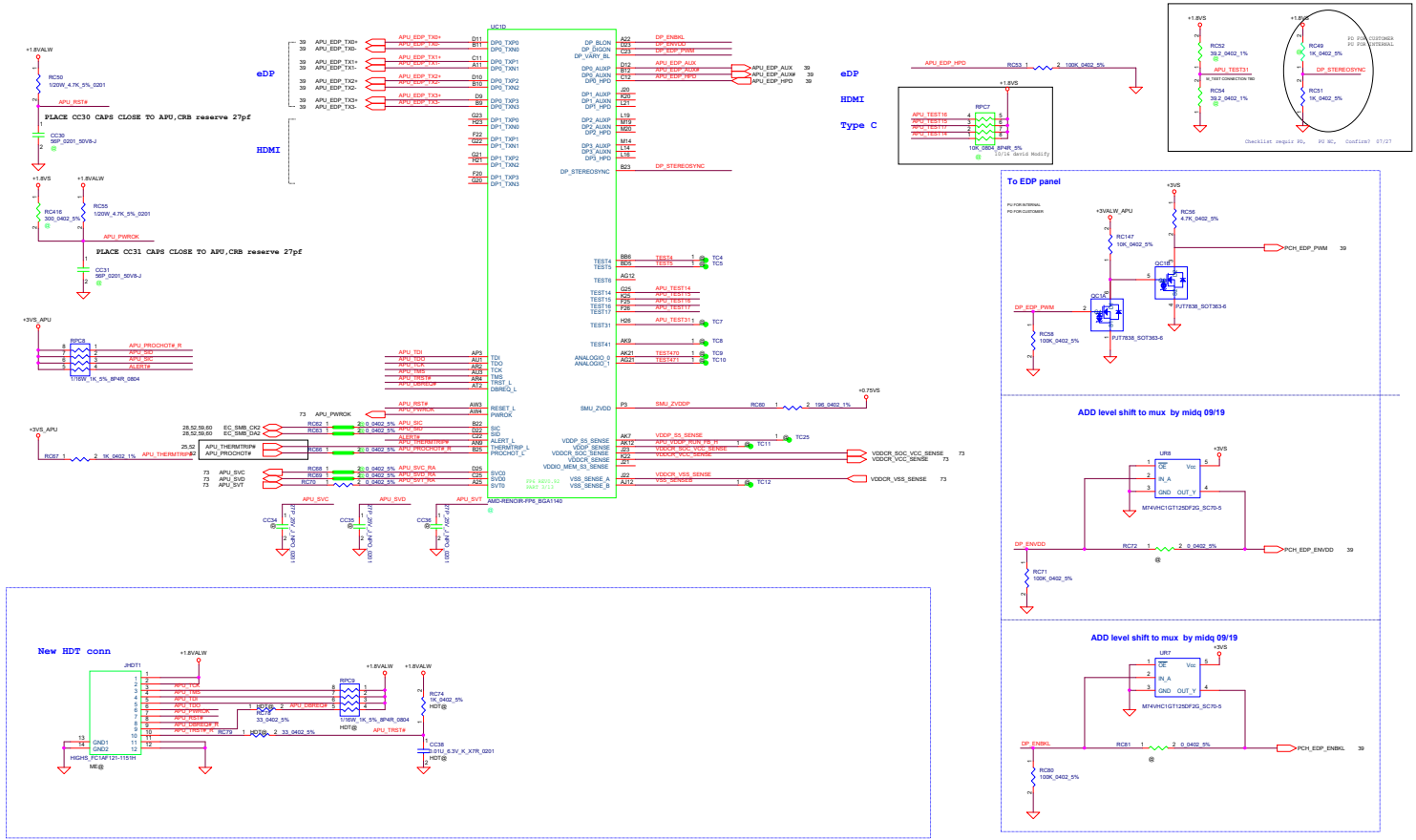

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Title: FP5 (DP/JTAG/SIV2/MISC)

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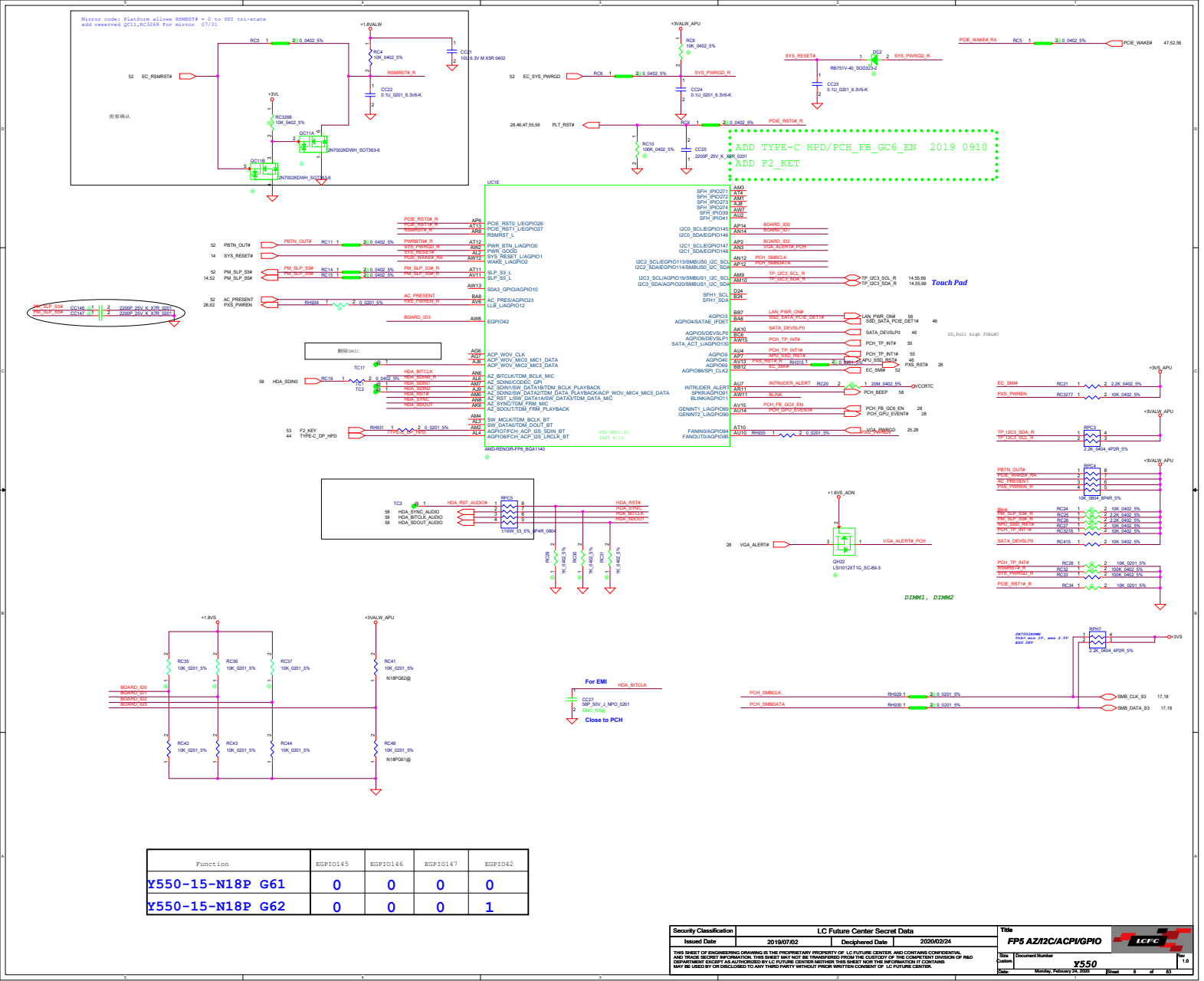

Function	EGPIO145	EGPIO146	EGPIO147	EGPIO42
Y550-15-N18P G61	0	0	0	0
Y550-15-N18P G62	0	0	0	1

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Title: FP5 AZ/I2C/ACPI/GPIO

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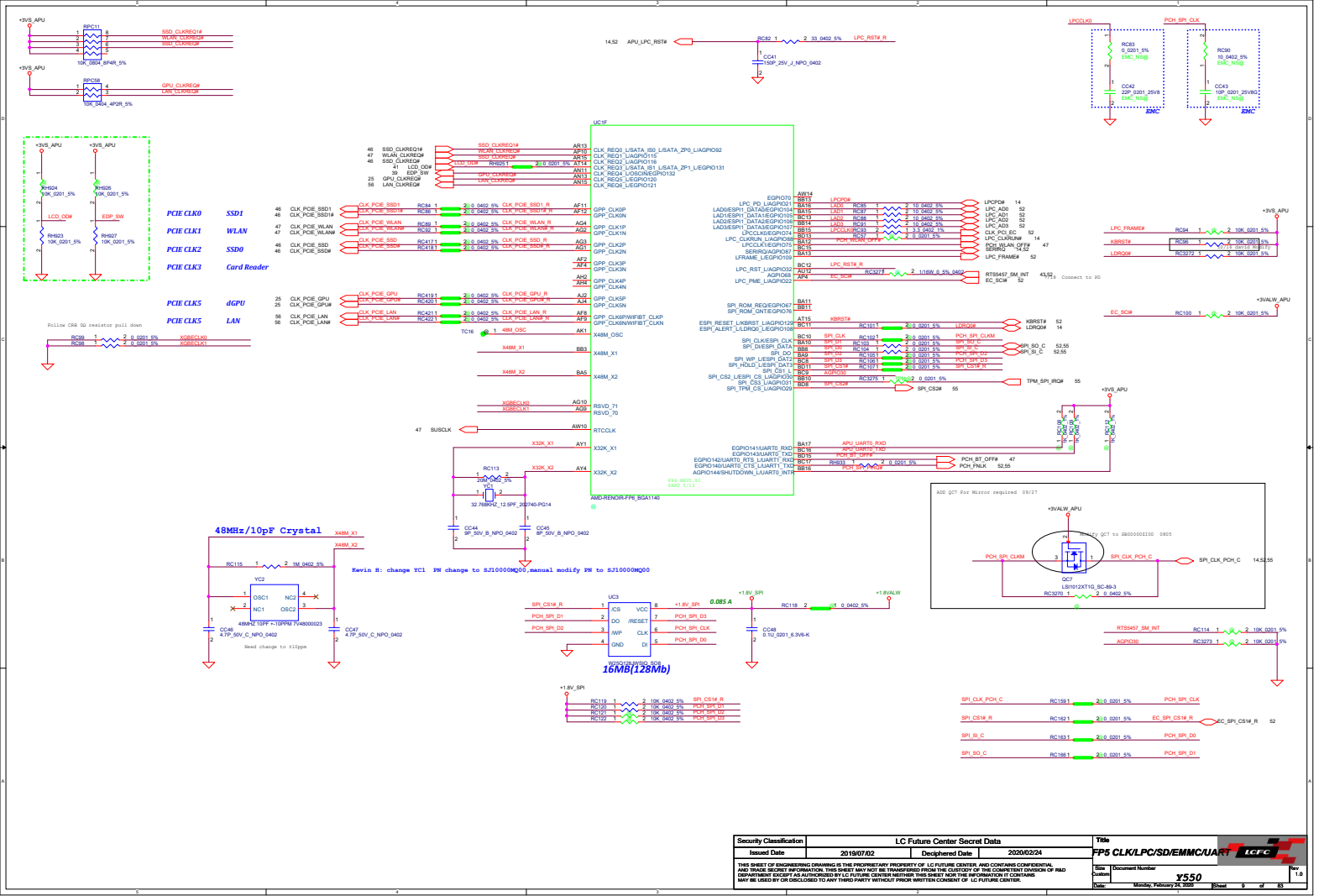

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FP5 CLK/LPC/SD/EMMC/UART

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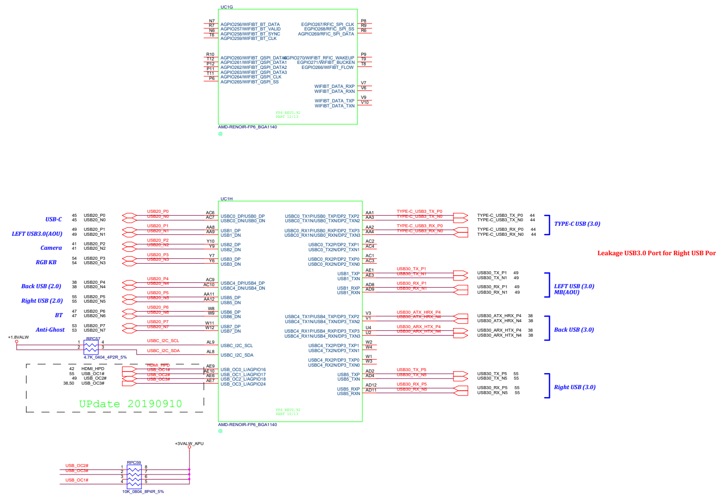

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Title: **FP5 USB/WIFI**

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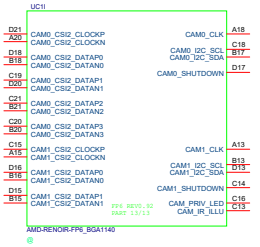

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Title: FP5 CAM

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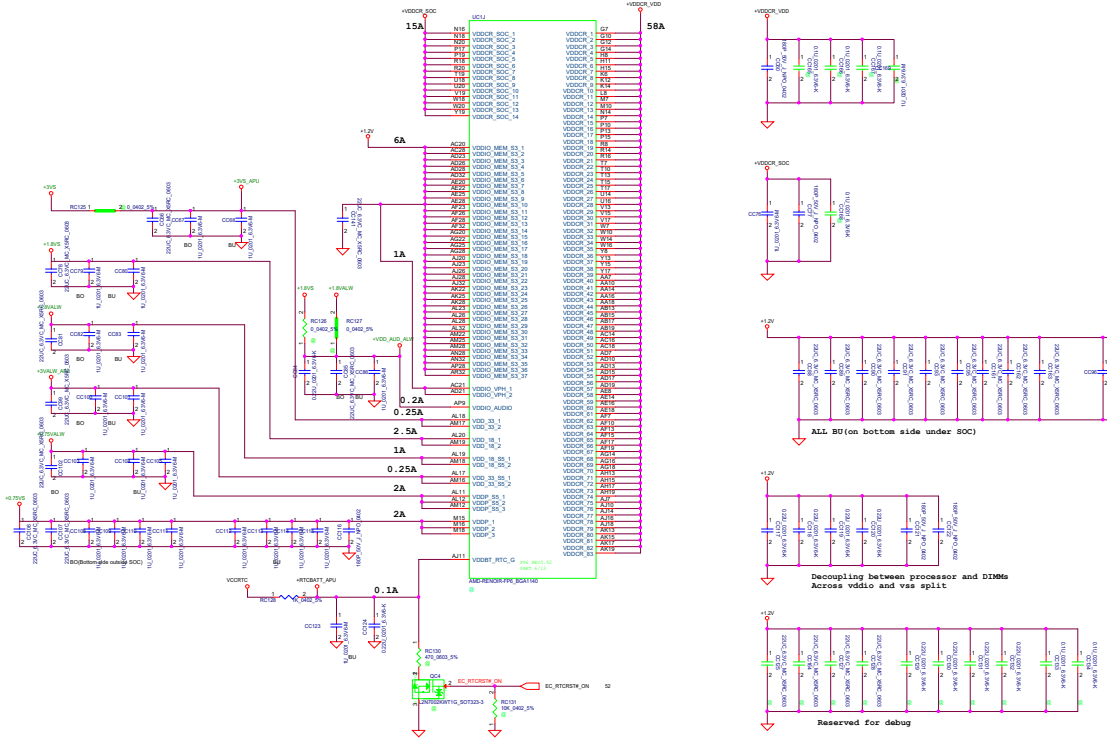

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Title: FP5 POWER

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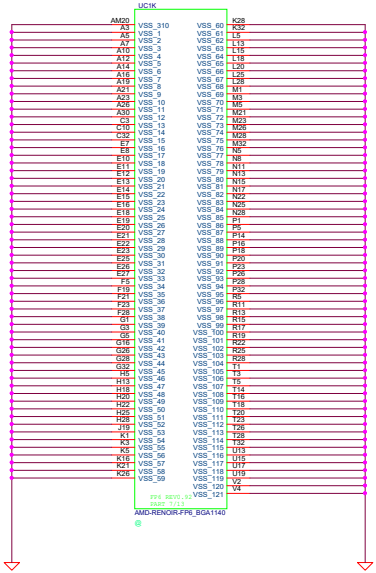

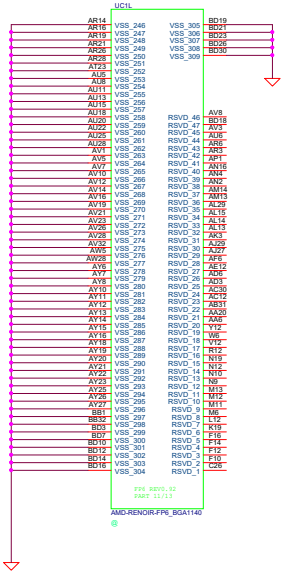

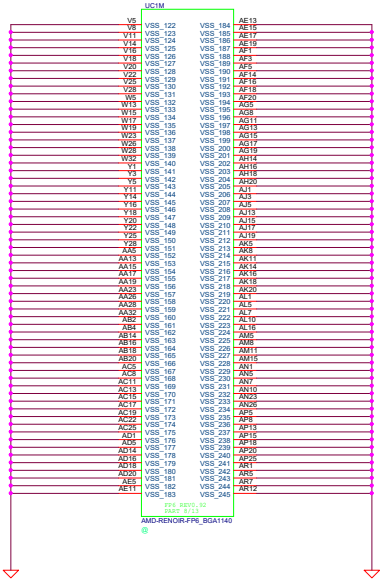

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Title: FP5 GND

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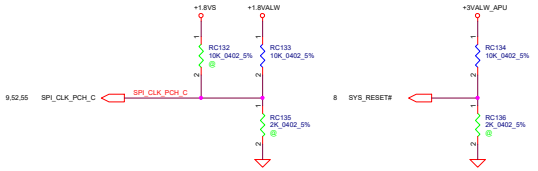
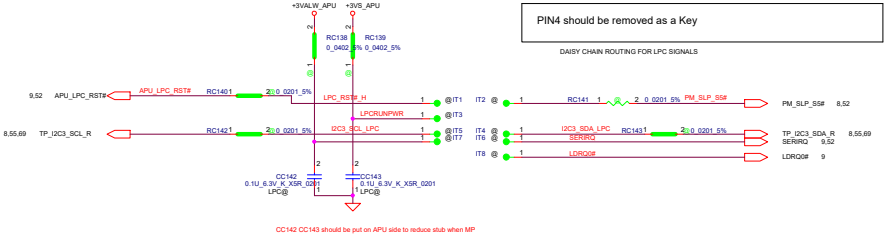


STRAP PINS	SYS_RESET#
PCH_SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET#	1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE

LPC ROM EMULATOR HEADER



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Title	FP5 Straps		
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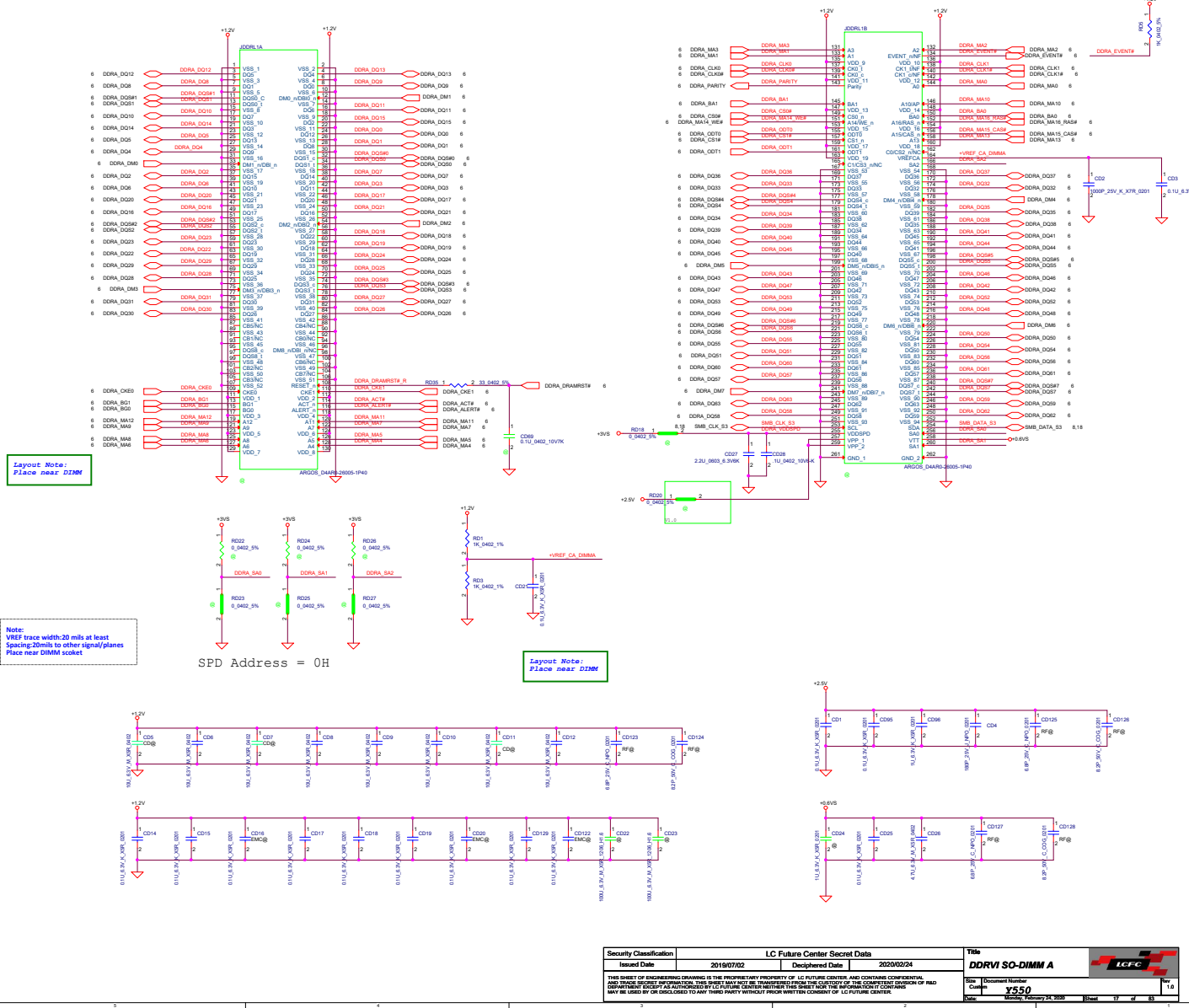
DDR4 SO-DIMM A



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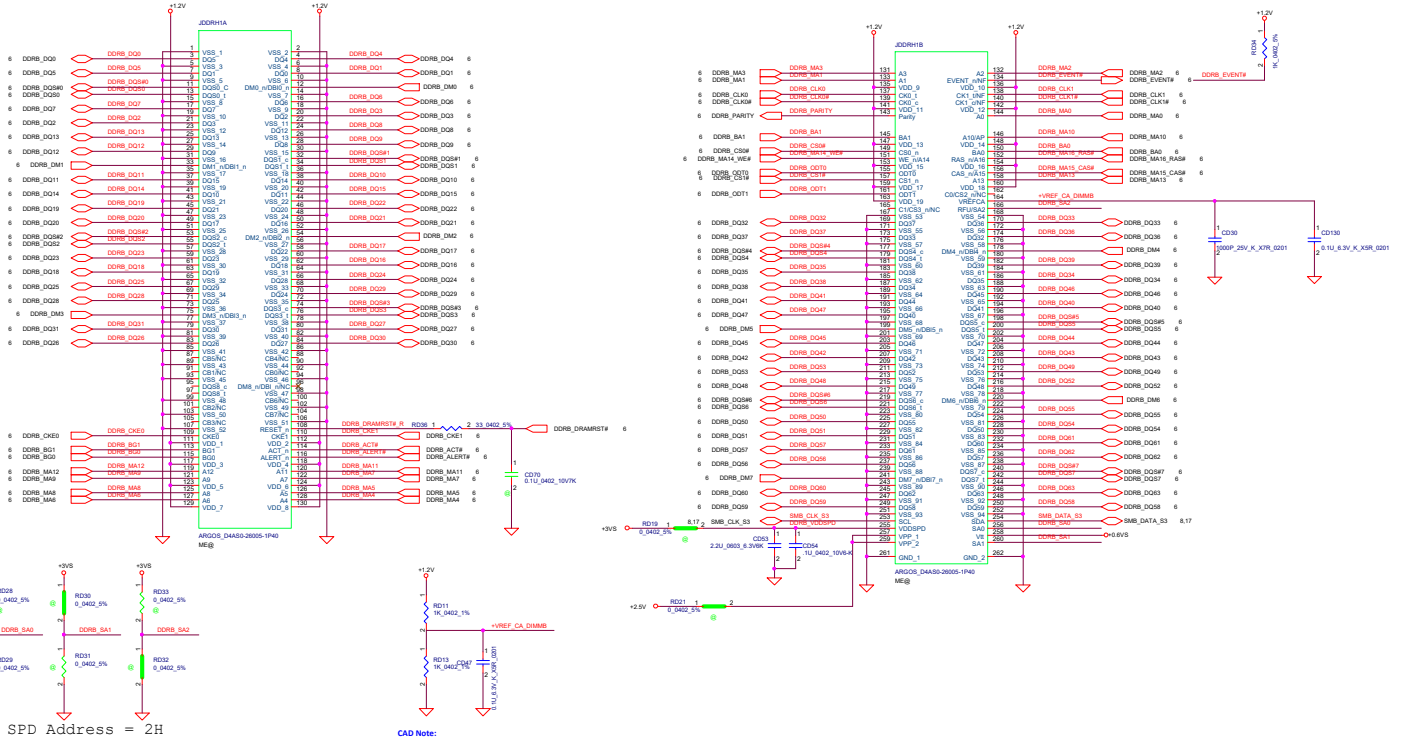
DDR4 SO-DIMM B



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Title

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N17P-G1 GPIO

GPIO	I/O	ACTIVE	Function Description	I/O Termination
GPIO0	OUT	-	PWM Output to control NVVDD	
GPIO1	OUT	-	FB Enable for GC6 2.1	
GPIO2	IN	-	GPU wake signal for GC6 2.1	
GPIO3	OUT	-	PWM Output to control the SRAM power supply	
GPIO4	OUT	-	GPU power sequencing for GC6 2.1 --- 1V8_MAIN_EN	
GPIO5	IN	N/A	Active low Frame Lock	
GPIO6	OUT	-	Phase Shedding, NVVDD_PSI	
GPIO7	OUT	N/A	Panel Backlight enable	
GPIO8	OUT	-	Memory voltage Control	
GPIO9	I/O	-	Active Low Thermal Alert	
GPIO10	OUT	-	Memory VREF Control (100K pull Down)	
GPIO11	OUT	-	Panel Power enable	
GPIO12	IN	-	AC power detect or power supply overdraw input	(10K pull High)
GPIO13	OUT	N/A	LCD Panel Backlight Enable	
GPIO14	IN	N/A	Hot Plug Detect for IFPA	
GPIO15	IN	N/A	Hot Plug Detect for IFPB	
GPIO16	OUT	-	System side PCIe reset monitor	
GPIO17	IN	N/A	Hot Plug Detect for IFPD	
GPIO18	IN	N/A	Hot Plug Detect for IFPE	
GPIO19	OUT	N/A	3D Vision L/R Signal	
GPIO20		N/A	GC5_MODE	
GPIO21	I/O	N/A	UNUSED	
GPIO22	I/O	N/A	UNUSED	
GPIO23	OUT	-	GPU PCIe self-reset control	
GPIO24	IN	N/A	Hot Plug Detect for IFPF	
GPIO25		N/A	UNUSED	
GPIO26		N/A	UNUSED	
GPIO27	IN	N/A	Hot Plug Detect for IFPC	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

1:ENABLE 0:DISABLE

SOR0/1/2/3 ENABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

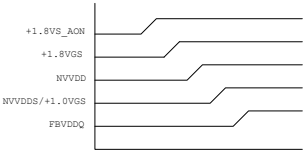
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

N17P-G1 Power Sequence

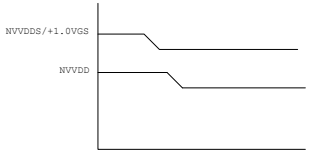


1. All power rail ramp up time should be larger than 40us and is recommended to be less than 2ms.

2. T (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_Pgood) must NOT exceed 4ms.

3. All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU can NOT have any 3.3V leakage path before 1V8_AON present.

4. The previous power rail must ramp up to 90% before the next power rail can start ramping up.



1. NVVDDS/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD.

2. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.

3. The previous power rail must ramp down to 10% before the next power rail can start ramping down.

Security Classification	LC Future Center Secret Data			Title
Issued Date	2019/07/02	Deciphered Date	2020/02/24	VGA Notes List

Size	Document Number	Rev
C	¥550	1.0

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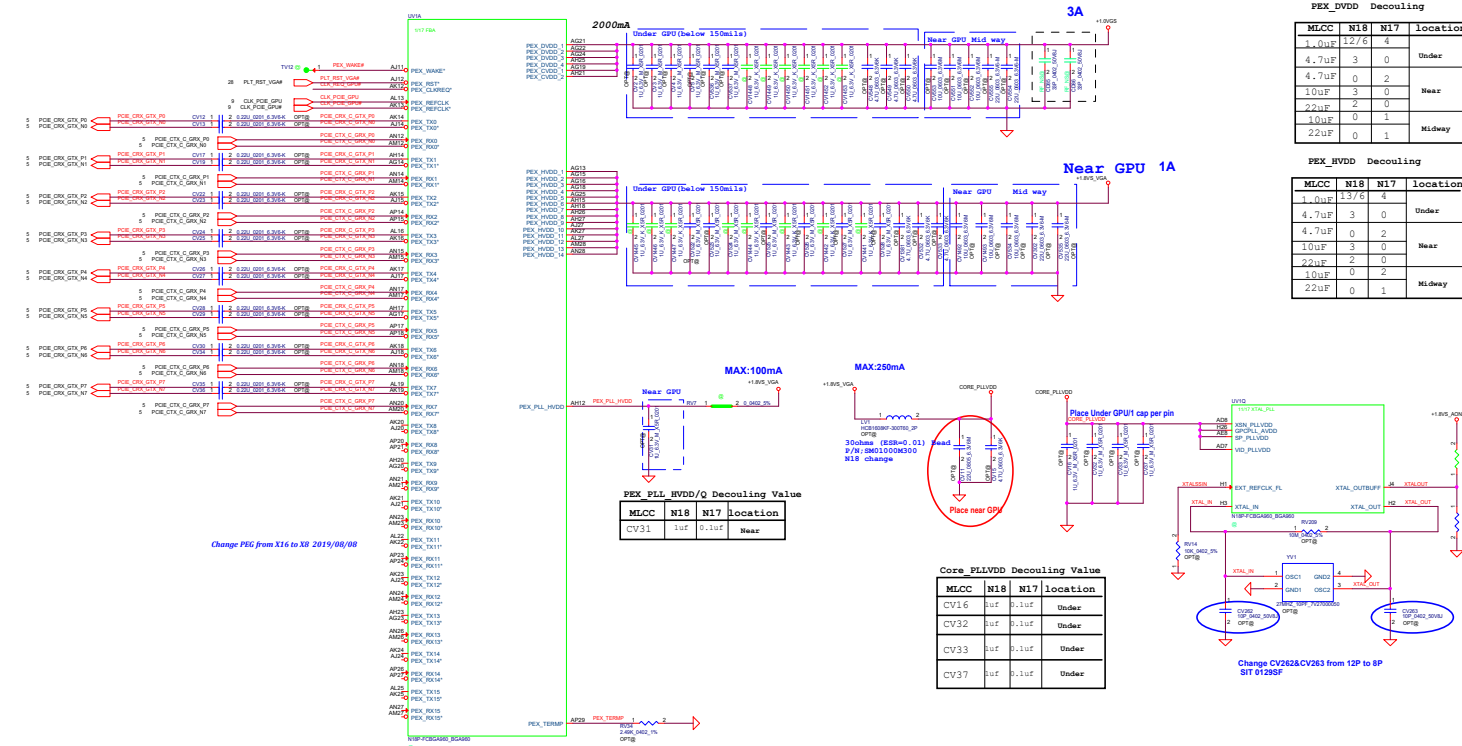


PEX_DVDD Decoupling

MLCC	N18	N17	location
1.0uF	12/6	4	Under
4.7uF	3	0	
4.7uF	0	2	Near
10uF	3	0	
22uF	2	0	
10uF	0	1	Midway
22uF	0	1	

PEX_HVDD Decoupling

MLCC	N18	N17	location
1.0uF	13/6	4	Under
4.7uF	3	0	
4.7uF	0	2	Near
10uF	3	0	
22uF	2	0	Midway
10uF	0	2	
22uF	0	1	

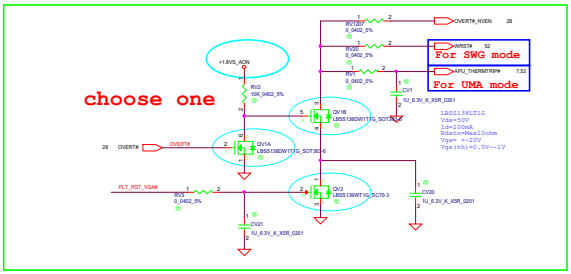
PEX_PLL_HVDD/Q Decoupling Value

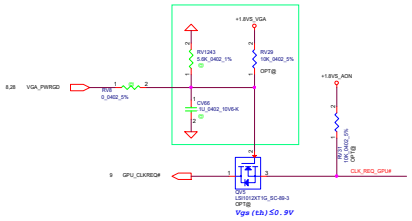
MLCC	N18	N17	location
CV31	1uf	0.1uf	Near

Core_PLLVDD Decoupling Value

MLCC	N18	N17	location
CV16	1uf	0.1uf	Under
CV32	1uf	0.1uf	Under
CV33	1uf	0.1uf	Under
CV37	1uf	0.1uf	Under

Change CV262&CV263 from 12P to 8P
SIT 0129SF





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Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title	N18P_(1/8):PEG I/F		
Size	Document Number		Rev
Custom	Y550		1.0
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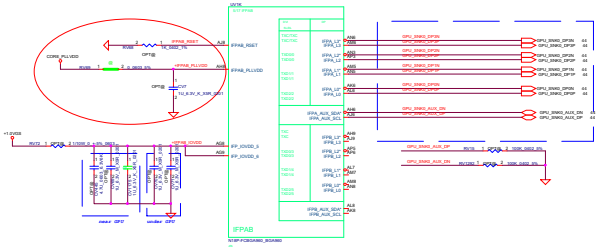
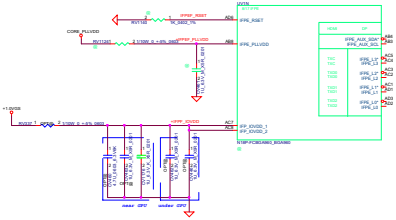
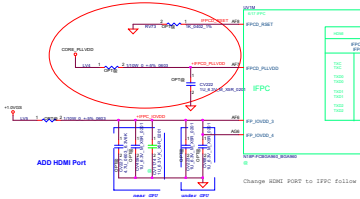
Ref NV DG-08780-001
If an IFP link is unused, in general it should be left unconnected.
This includes Main and Aux links.
IFPxy_RSET and IFPxy_PLLVDD (xy=AB,CD,EF)
can be left unconnected if neither of IFPx /IFPy is in use

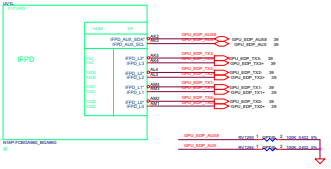




Decouling Value

MLCC	N18	N17	location
CV7	1uf	0.1uf	Under
CV222	1uf	0.1uf	Under
CV461	1uf	0.1uf	Under
CV70	1uf	0.1uf	Under
CV71	1uf	0.1uf	Under
CV223	1uf	0.1uf	Under
CV68	1uf	0.1uf	Under
CV462	1uf	0.1uf	Under
CV484	1uf	0.1uf	Under





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Title: N18P_(34):VRAM I/F

Size: A3 | Document Number: Y550 | Rev: 1A

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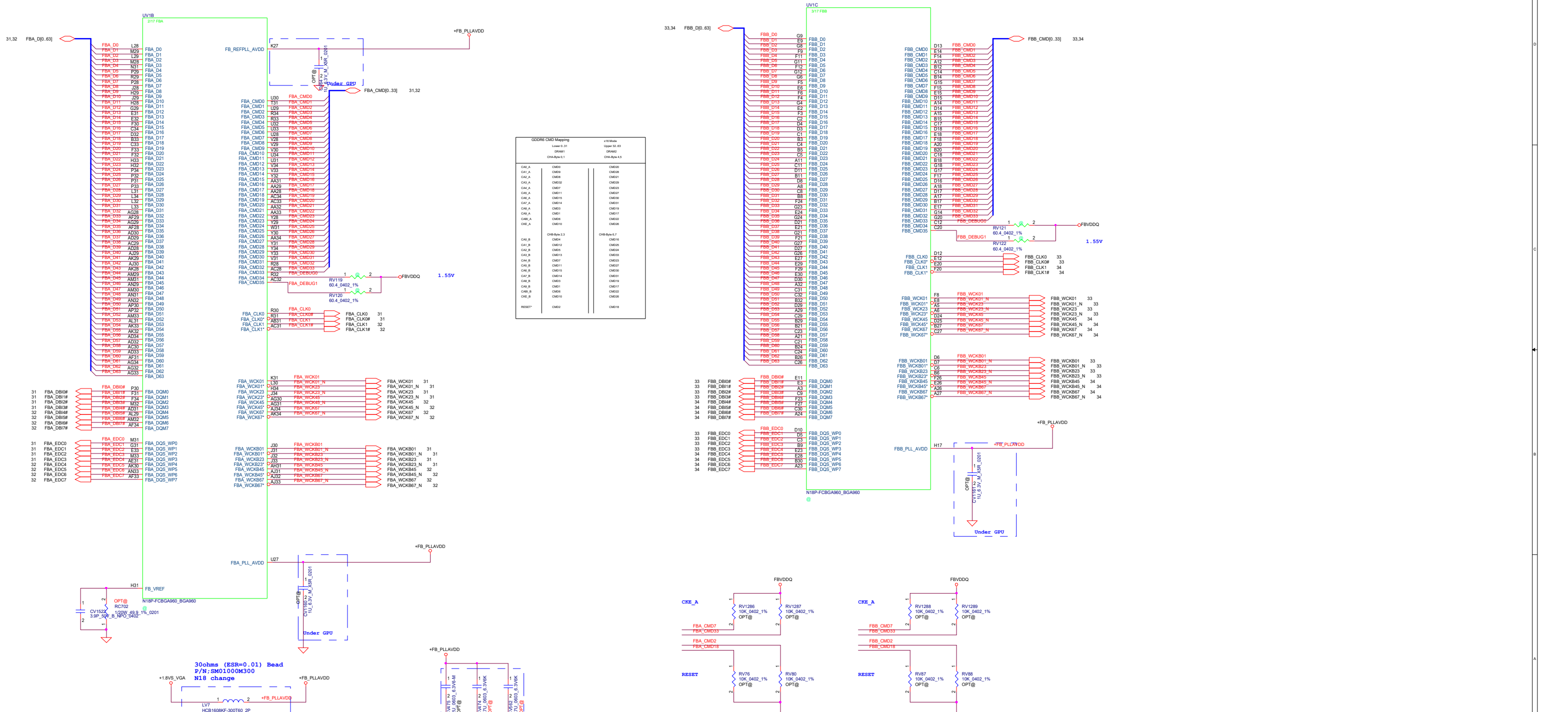

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Issued Date	2019/07/02	Deciphered Date	2020/02/24

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Title: N18P_(3/6):VRAM I/F

Size: Custom | Document Number: Y550 | Rev: 1.0

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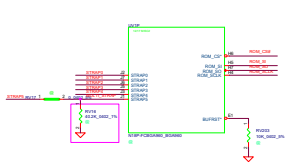
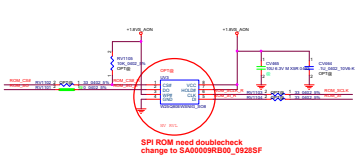
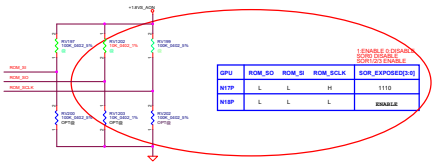
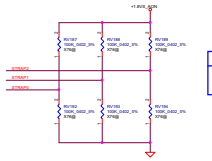




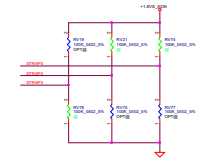


GPU	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N17P	L	L	H	1110
N18P	L	L	L	ENABLE

1:ENABLE 0:DISABLE
SOR0 DISABLE
SOR1 DISABLE



VRAMCFG					
GPU VRAM	FB Memory (GDDR6)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
4GB	Samsung 8Gb	K4Z80325BC-HC14	0(0x0000)	L	L	L
	Micron 8Gb	MT61K256M32JE-14:A	1(0x0001)	L	L	H



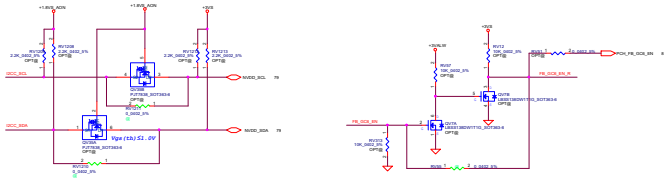
VGA_DEVICE							
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	H	0	0	0	1

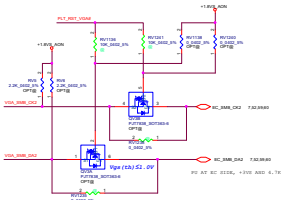
1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

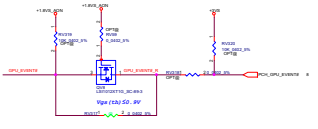
1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

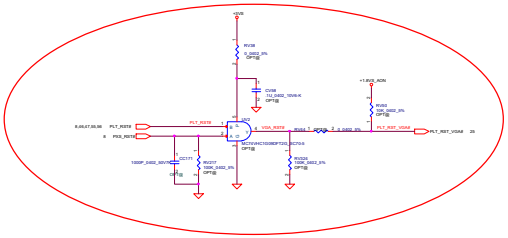
1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE

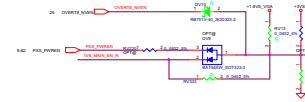




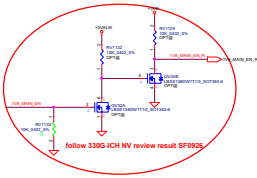




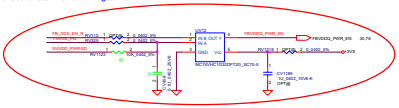
DG Power on/off sequence



discharger circuit



For GC6 20180827 ref Y540 change09275F



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Title	N18P_(4/6):GPIO		
Size	Document Number		Rev
C	Y550		1.0
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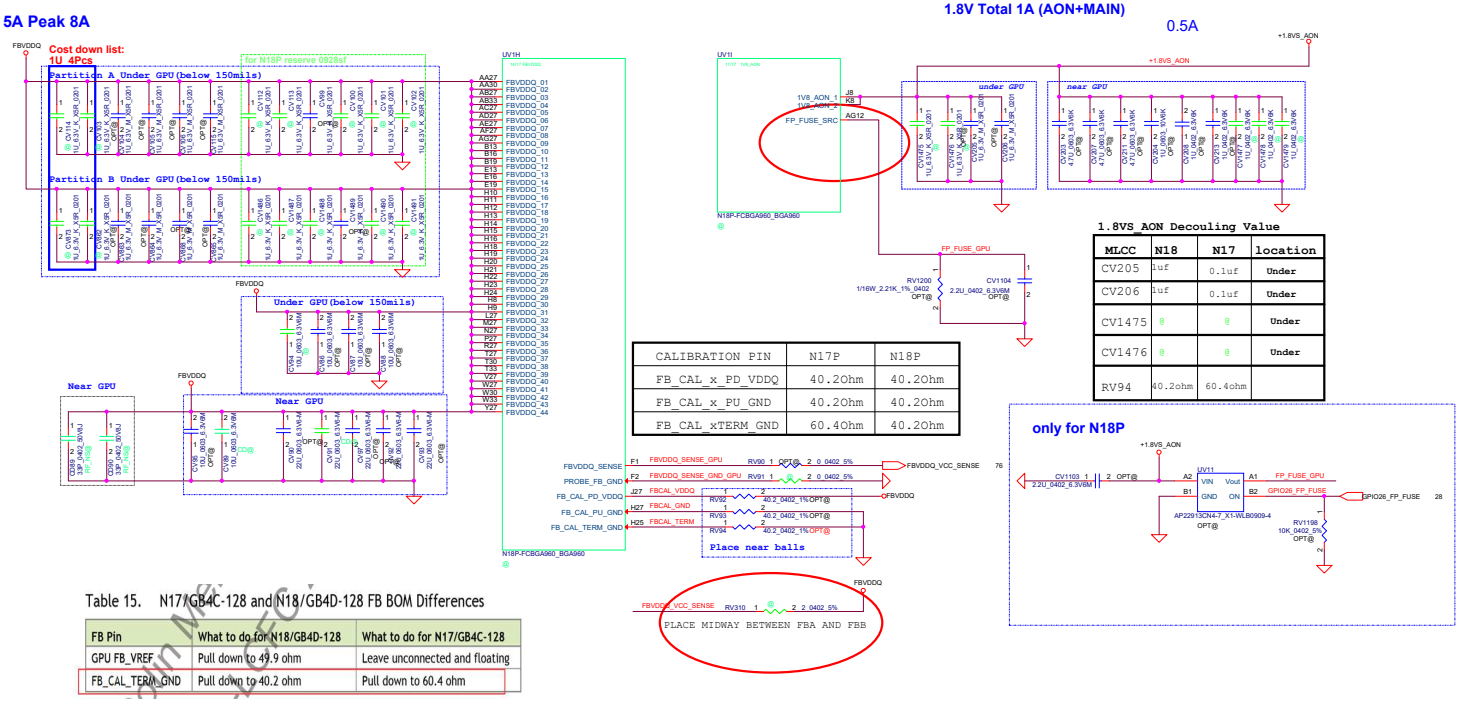

CALIBRATION PIN	N17P	N18P
FB_CAL_x_PD_VDDQ	40.2Ohm	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm	40.2Ohm

1.8VS_AON Decouling Value

MLCC	N18	N17	location
CV205	1uf	0.1uf	Under
CV206	1uf	0.1uf	Under
CV1475	@	@	Under
CV1476	@	@	Under
RV94	40.2ohm	60.4ohm	

Table 15. N17/GB4C-128 and N18/GB4D-128 FB BOM Differences

FB Pin	What to do for N18/GB4D-128	What to do for N17/GB4C-128
GPU FB_VREF	Pull down to 49.9 ohm	Leave unconnected and floating
FB_CAL_TERM_GND	Pull down to 40.2 ohm	Pull down to 60.4 ohm

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Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title: N18P_(5/6):PWR

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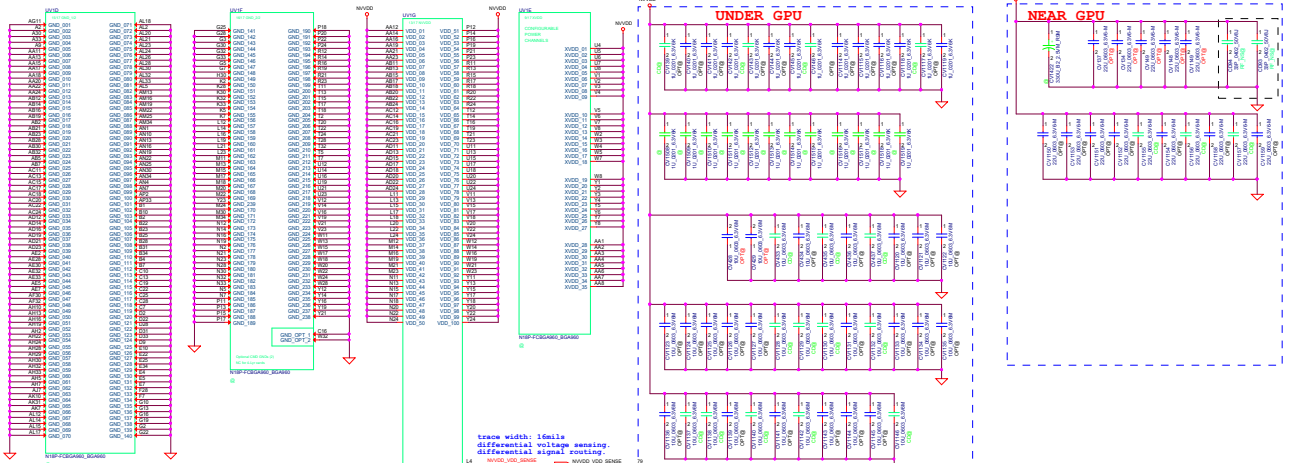
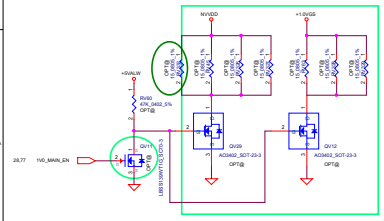
BOTH GP107 AND N18P-G5 NEED.
NC_AF30,AF32,AK31,AM34,E34,H30,M30,M34,
A30,A9,BZ,BZ3,D22,D28,D9,E4

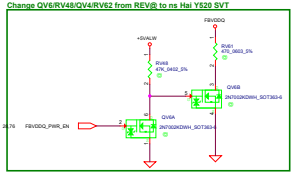


Add RV332 for NVVDDS discharge Hai Y520 SVT

Change NVVDDS & +1.0VGS discharge circuit
HLZ SIV 0725



Change QV6/RV48/QV4/RV62 from REV@ to ns Hai Y520 SVT



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Title: N18P_(6/6):PWR,VSS

LCFC

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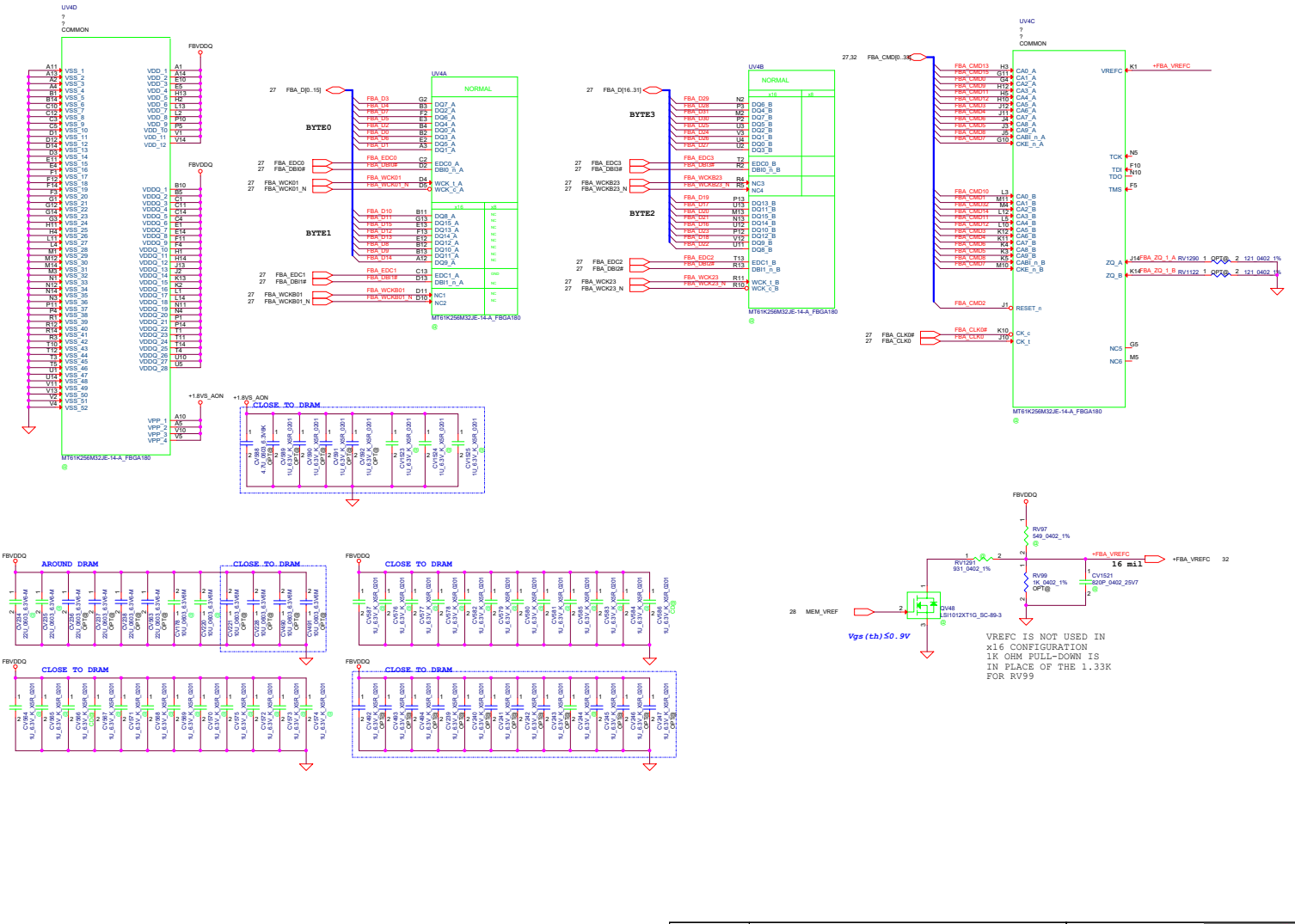

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Title: N18P_GDDR6_A_[31_0]

Size: C | Document Number: ¥550 | Rev: 1.0

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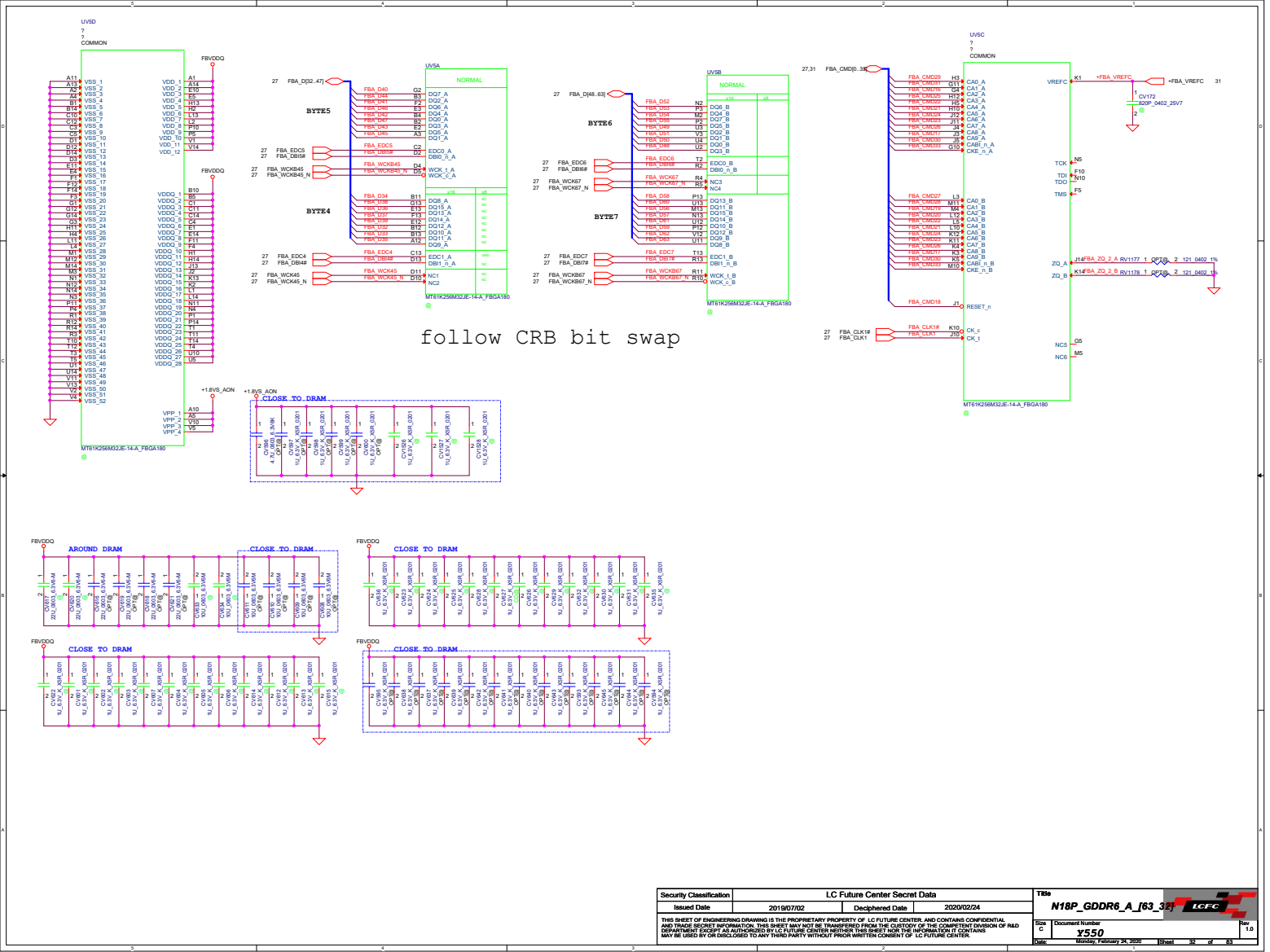

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

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Title: N18P_GDDR6_A_[63_32]

Size	Document Number	Rev
C	¥550	1.0

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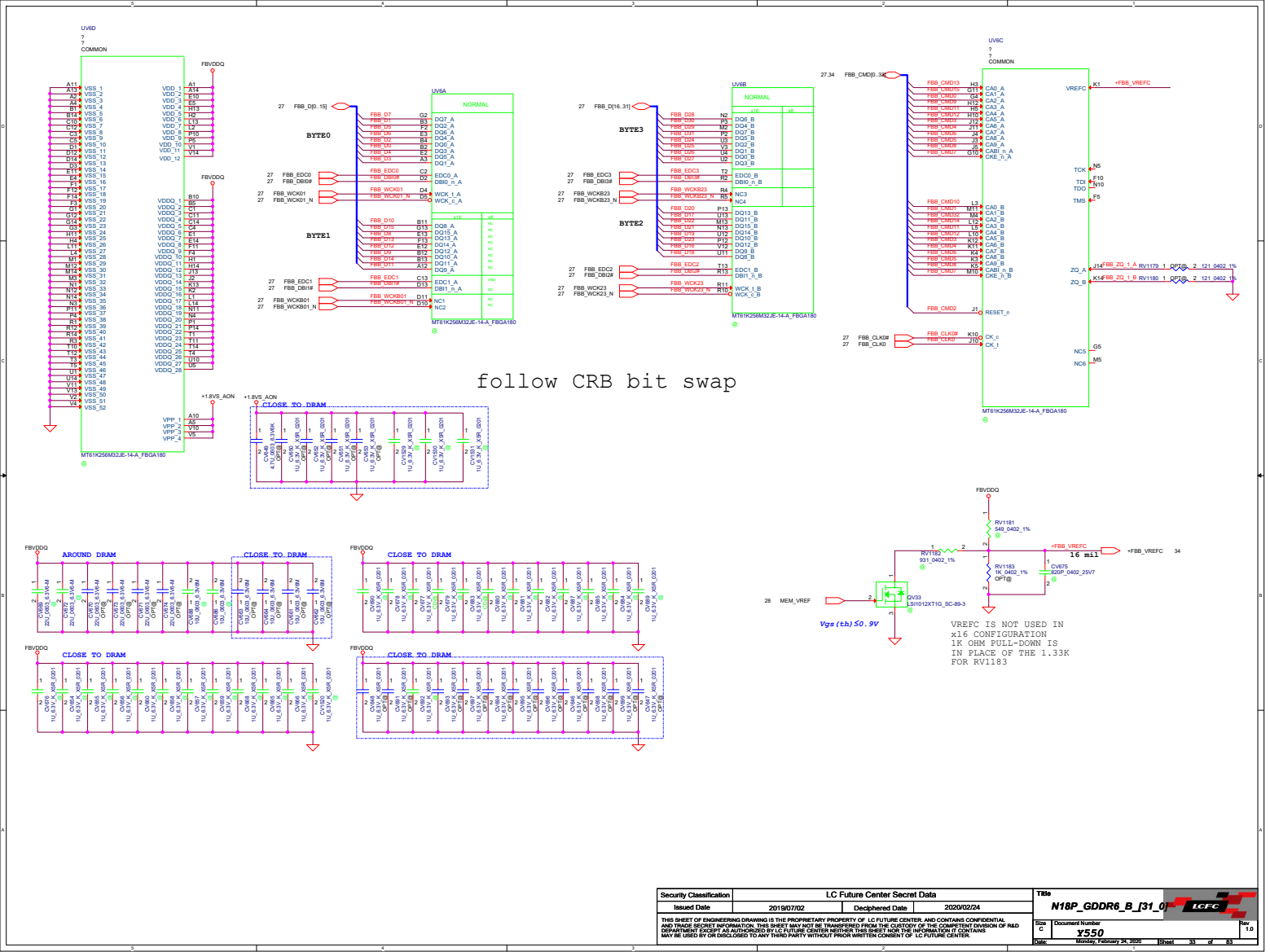
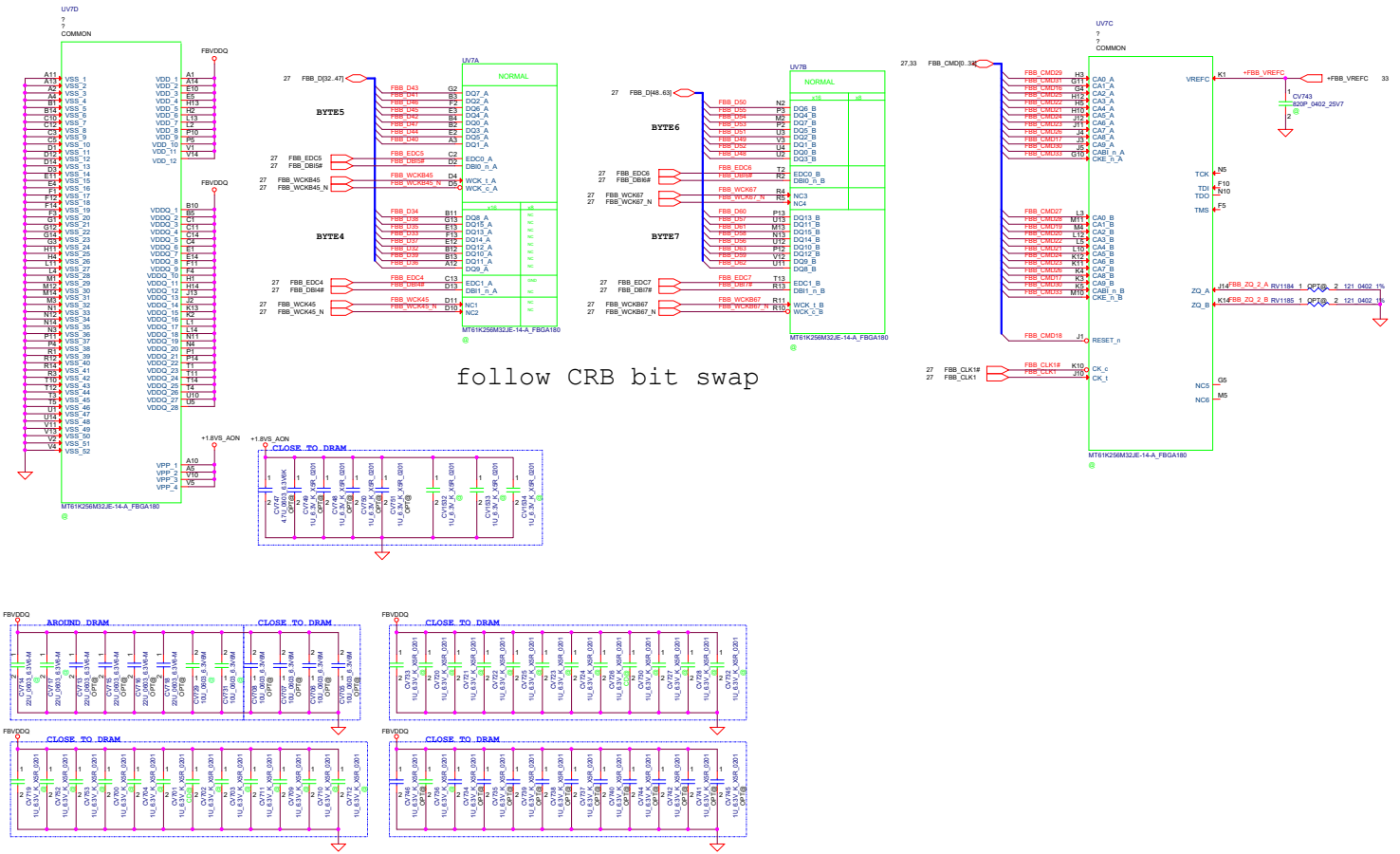


Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title	N18P_GDDR6_B_[31_0]		
Size C	Document Number ¥550		Rev 1.0
Date: Monday, February 24, 2020	Sheet 33 of 83		



Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

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Title: N18P_GDDR6_B_[63_32]

Size: C | Document Number: ¥550 | Rev: 1.0

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Title

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Size	Document Number	Rev
B	***¥550***	1.0

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Title

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Size	Document Number	Rev
B	***Y550***	1.0

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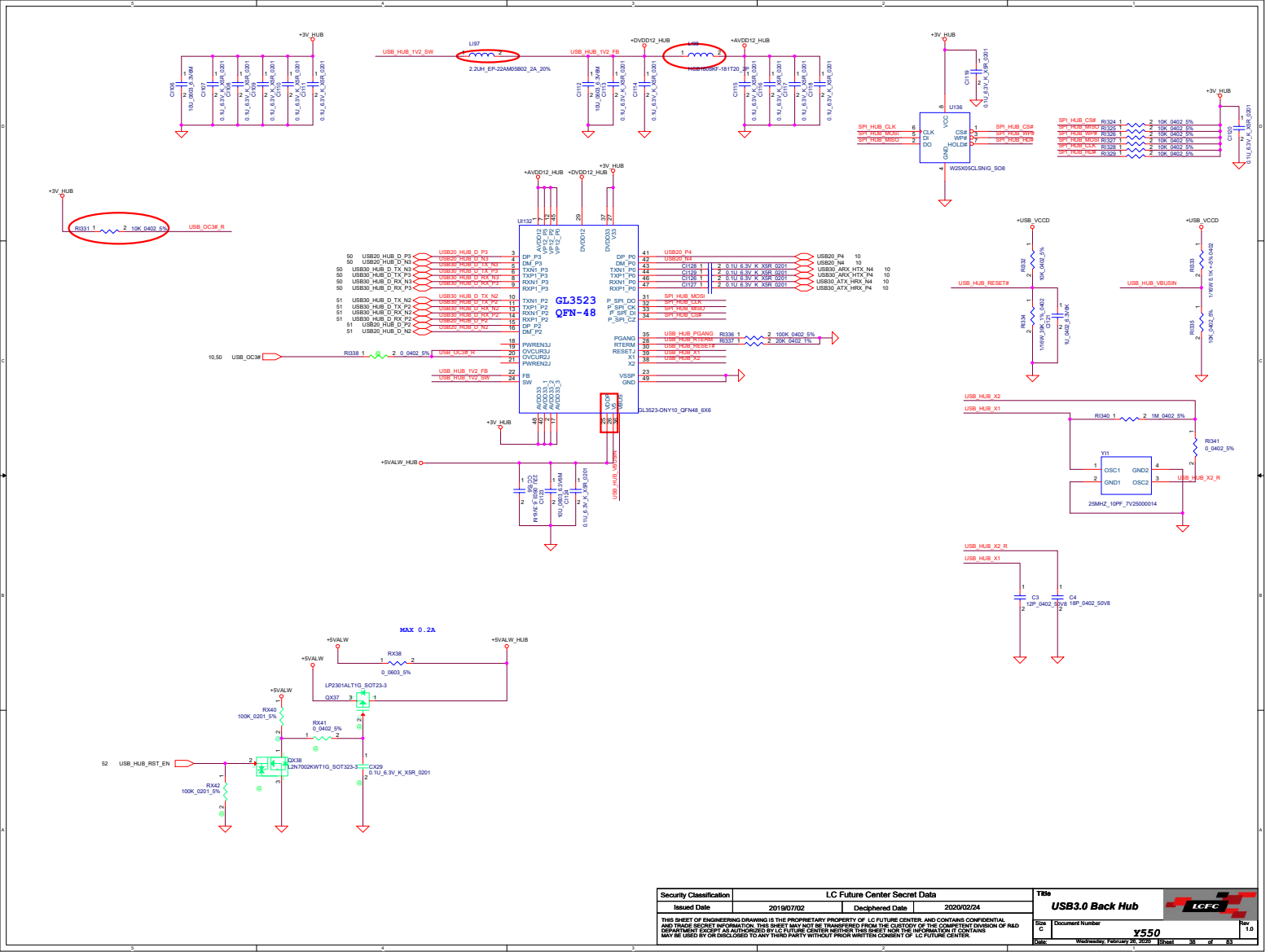
USB Redriver移到小板

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title: DDI Redriver PS8330

Size: C	Document Number: ¥540	Rev: 1.0
Date: Monday, February 24, 2020	Sheet 37 of 83	



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Issued Date	2019/07/02	Deciphered Date	2020/02/24

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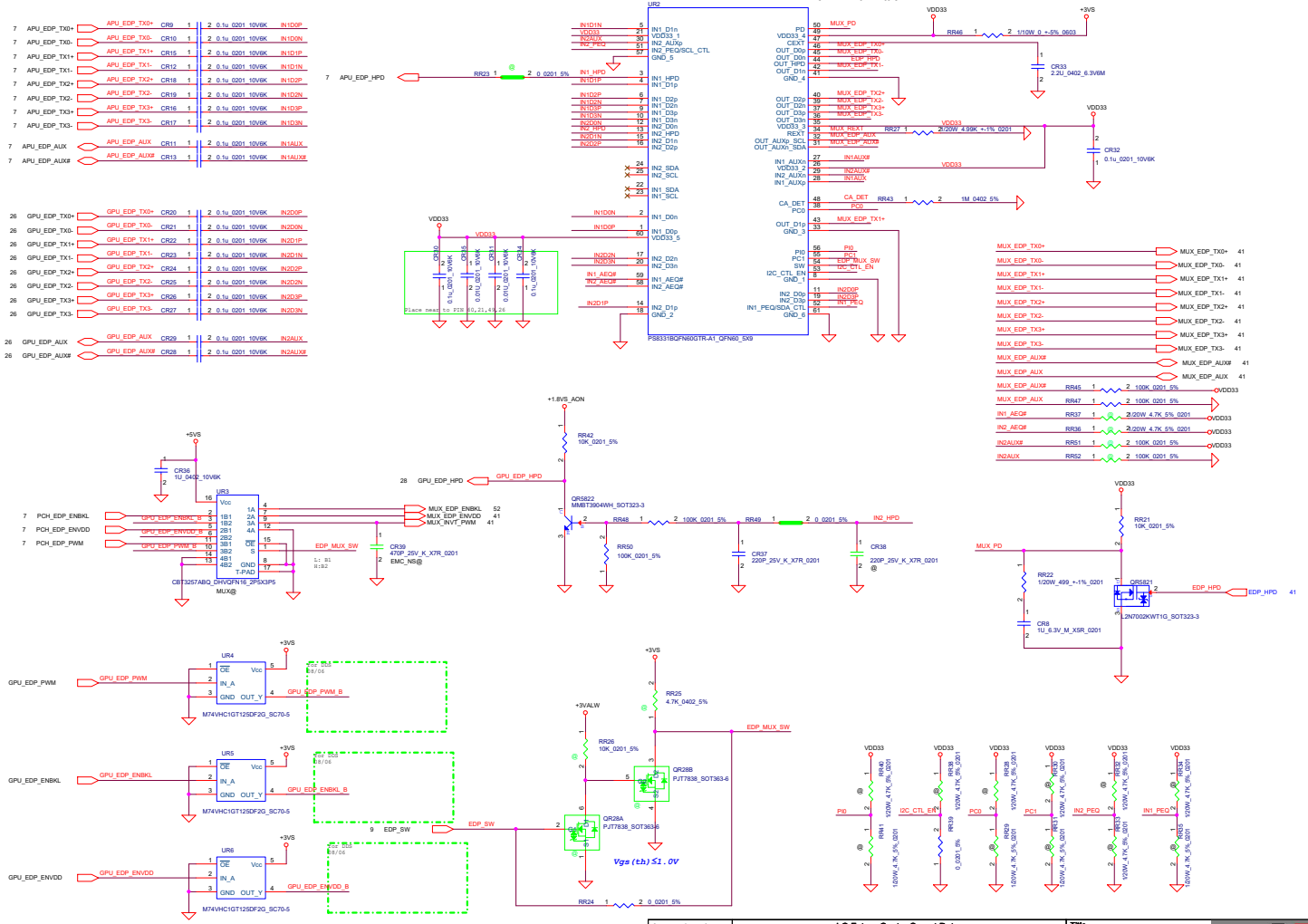
Title: **USB3.0 Back Hub**

LCFC

Size: C | Document Number: ¥550 | Rev: 1.0

Date: Wednesday, February 26, 2020 | Sheet 38 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

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Title: EDP MUX

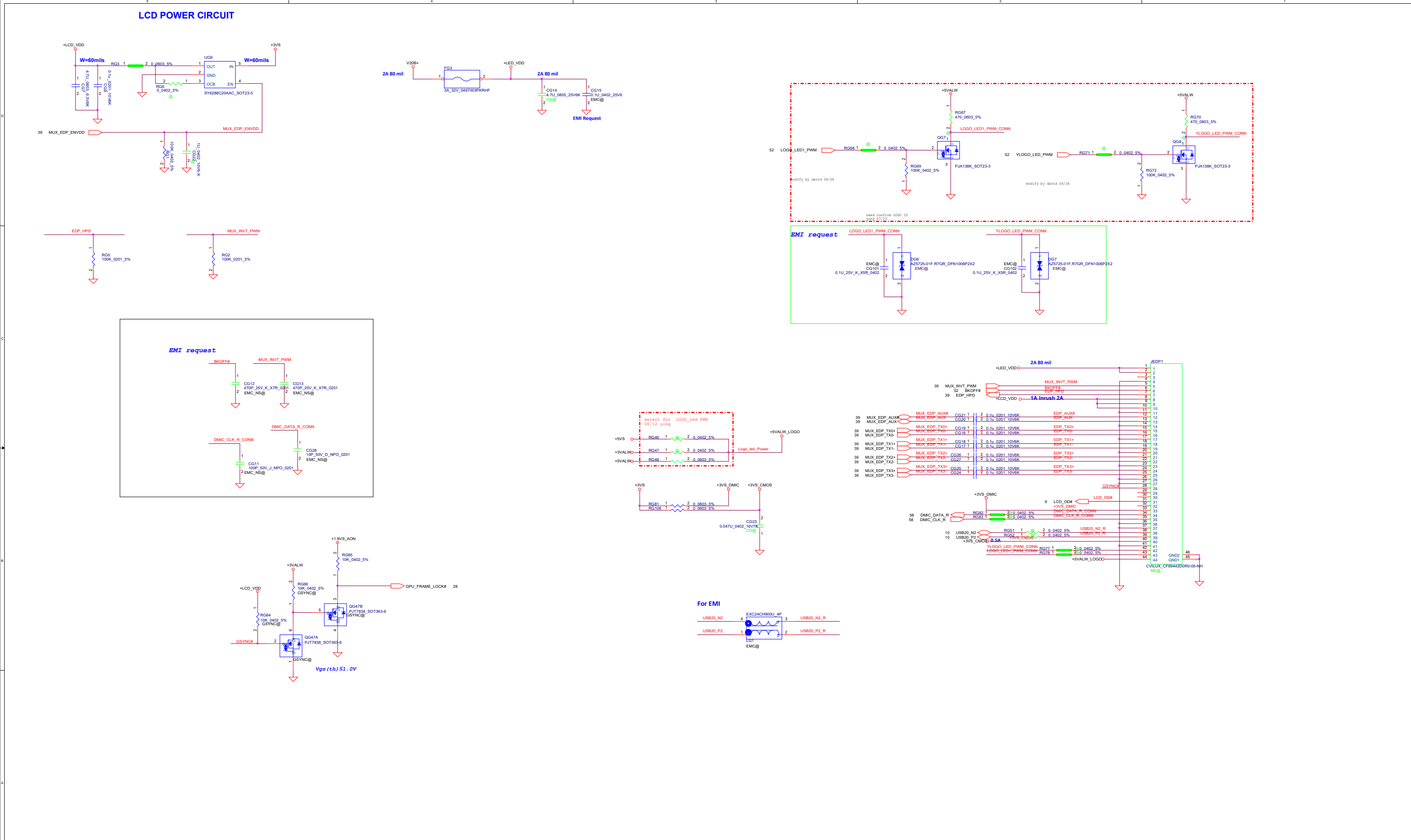
Size	Document Number	Rev
C	Y540	1.0

Date: Monday, February 24, 2020 Sheet 39 of 83

删除DDS线路

Security Classification	LC Future Center Secret Data		Title: DC V TO VS INTERFACE
Issued Date	2019/07/22	Declassified Date	2020/02/24

Size: A1	Document Number: Y540		Rev: 1.0
Date: Monday, February 24, 2020	Sheet: 45 of 63		

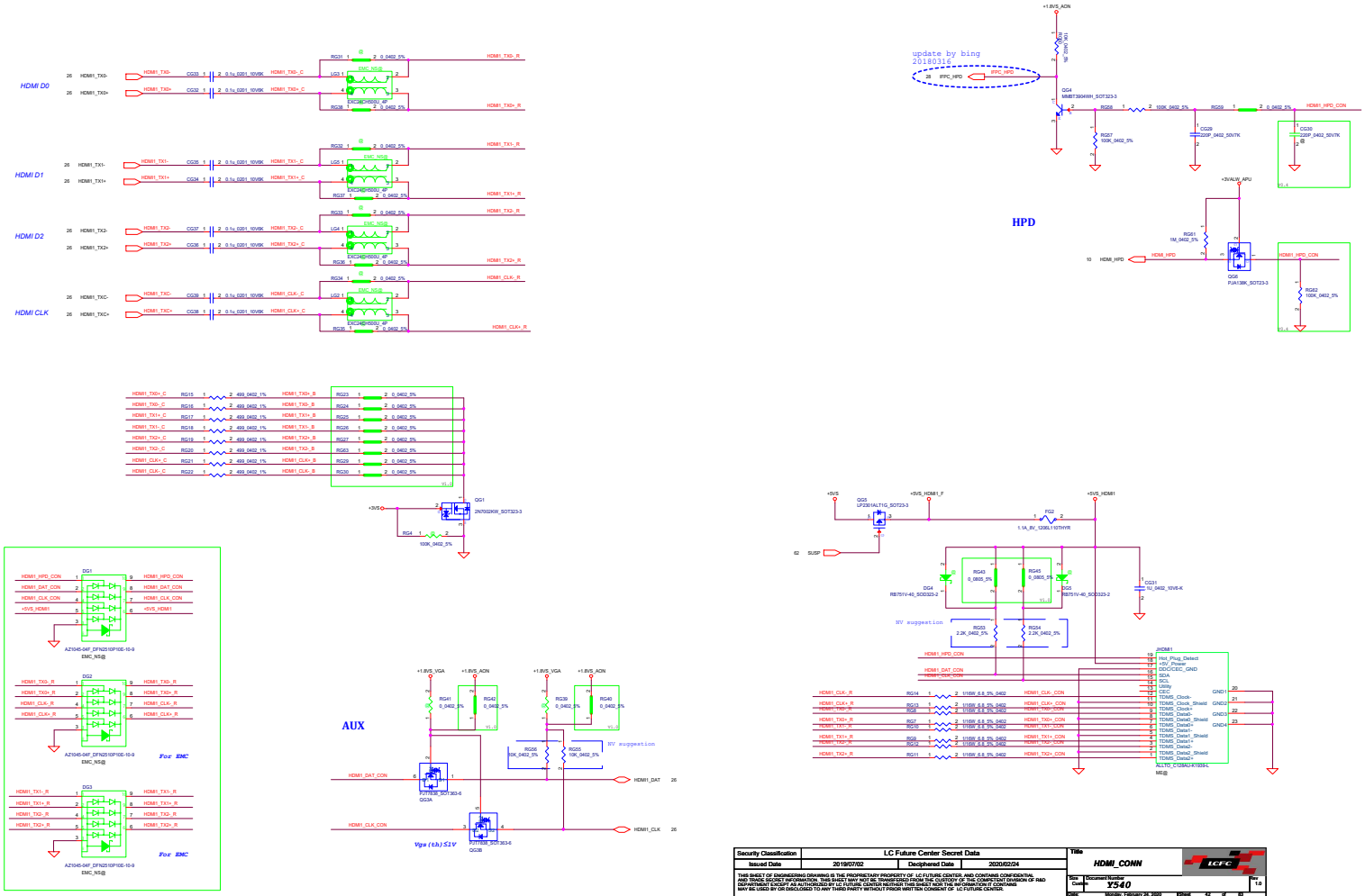


Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title: eDP/ CMOS/Touch screen

Size: D | Document Number: Y540 | Rev: 1.0

Date: Wednesday, February 26, 2020 | Sheet 41 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

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Title	HDMI_CONN
Size	C
Document Number	Y540
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Date	Monday, February 24, 2020
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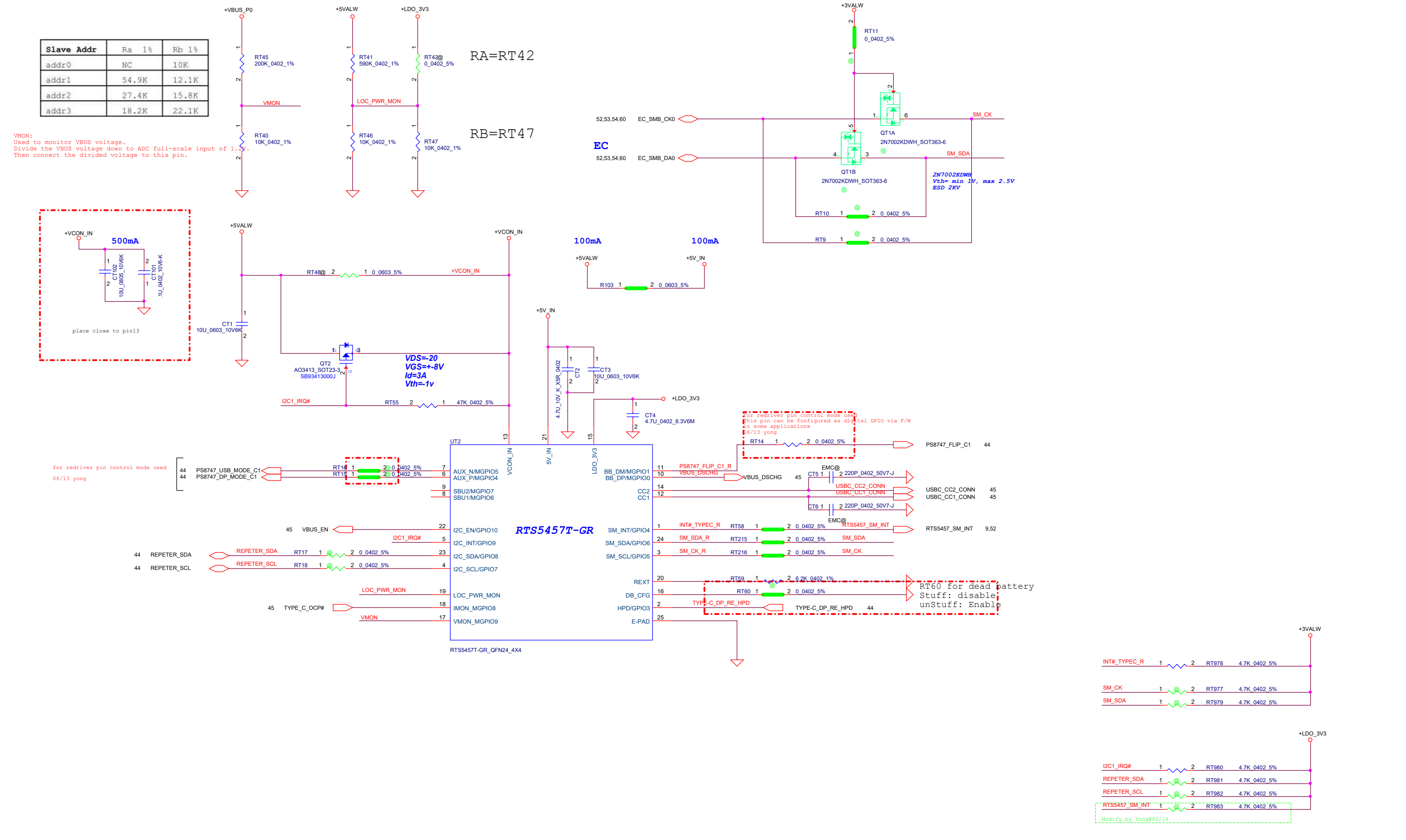
Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K

VMON:
Used to monitor VBUS voltage.
Divide the VBUS voltage down to ADC full-scale input of 1.2V.
Then connect the divided voltage to this pin.



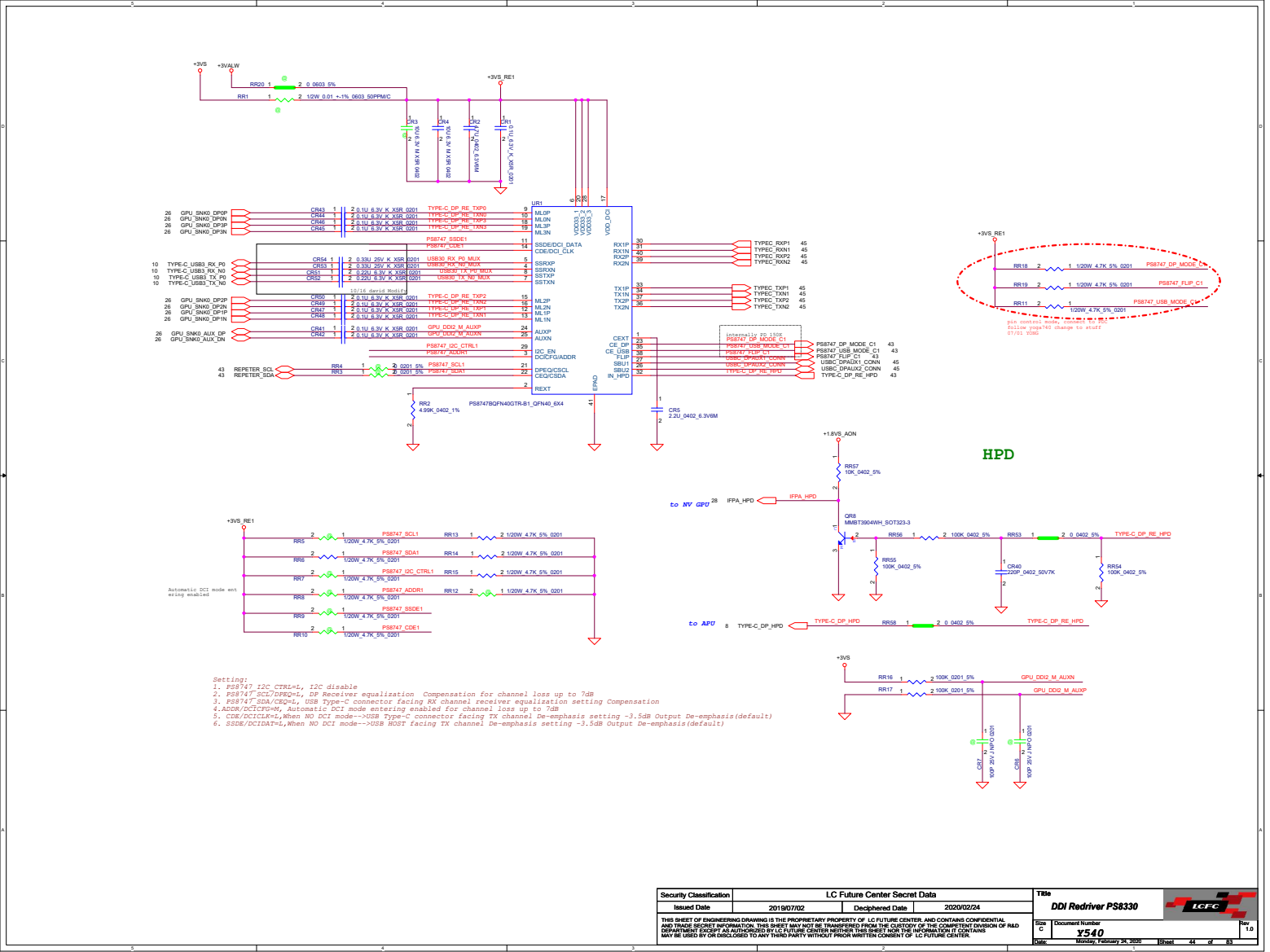
RA=RT42
RB=RT47
EC
+VBUS_P0
+5VALW
+LDO_3V3
+3VALW
RT45 200K_0402_1%
RT40 10K_0402_1%
RT41 590K_0402_1%
RT46 10K_0402_1%
RT42@ 0_0402_5%
RT47 10K_0402_1%
VMON
LOC_PWR_MON
RT11 0_0402_5%
52,53,54,60 EC_SMB_CK0
52,53,54,60 EC_SMB_DA0
QT1A 2N7002KDWH_SOT363-6
QT1B 2N7002KDWH_SOT363-6
SM_CK
SM_SDA
2N7002KDWH
Vth= min 1V, max 2.5V
ESD 2KV
RT10 0_0402_5%
RT9 0_0402_5%
+VCON_IN
500mA
CT102 10U_0805_10V6K
CT101 .1U_0402_10V6-K
place close to pin13
CT1 10U_0603_10V6K
RT48@ 0_0603_5%
QT2 AO3413_SOT23-3 SB93413000J
VDS=-20
VGS=+-8V
Id=3A
Vth=-1v
I2C1_IRQ#
RT55 47K_0402_5%
100mA
100mA
+5V_IN
R103 0_0603_5%
CT2 4.7U_10V_K_X5R_0402
CT3 10U_0603_10V6K
CT4 4.7U_0402_6.3V6M
for redriver pin control mode used
This pin can be fonfigured as digital GPIO via F/W in some applications
06/13 yong
RT14 0_0402_5%
PS8747_FLIP_C1 44
UT2
RTS5457T-GR
RTS5457T-GR_QFN24_4X4
AUX_N/MGPIO5
AUX_P/MGPIO4
SBU2/MGPIO7
SBU1/MGPIO6
I2C_EN/GPIO10
I2C_INT/GPIO9
I2C_SDA/GPIO8
I2C_SCL/GPIO7
LOC_PWR_MON
IMON_MGPIO8
VMON_MGPIO9
VCON_IN
5V_IN
LDO_3V3
BB_DM/MGPIO1
BB_DP/MGPIO0
CC2
CC1
SM_INT/GPIO4
SM_SDA/GPIO6
SM_SCL/GPIO5
REXT
DB_CFG
HPD/GPIO3
E-PAD
for redriver pin control mode used
06/13 yong
44 PS8747_USB_MODE_C1
44 PS8747_DP_MODE_C1
RT16 0_0402_5%
RT15 0_0402_5%
45 VBUS_EN
44 REPETER_SDA
44 REPETER_SCL
RT17 0_0402_5%
RT18 0_0402_5%
45 TYPE_C_OCP#
PS8747_FLIP_C1_R
VBUS_DSCHG
VBUS_DSCHG 45
CT5 220P_0402_50V7-J
CT6 220P_0402_50V7-J
EMC@
USBC_CC2_CONN 45
USBC_CC1_CONN 45
INT#_TYPEC_R
RT58 0_0402_5%
RTS5457_SM_INT
RTS5457_SM_INT 9,52
SM_SDA_R
RT215 0_0402_5%
SM_CK_R
RT216 0_0402_5%
RT59 6.2K_0402_1%
RT60 0_0402_5%
RT60 for dead battery
Stuff: disable
unStuff: Enable
TYPE-C_DP_RE_HPD
TYPE-C_DP_RE_HPD 44
RT978 4.7K_0402_5%
RT977 4.7K_0402_5%
RT979 4.7K_0402_5%
RT980 4.7K_0402_5%
RT981 4.7K_0402_5%
RT982 4.7K_0402_5%
RT983 4.7K_0402_5%
Modify by Yong@05/14

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title: USB TYPE-C Controller

Size: Custom | Document Number: Y540 | Rev: 1.0

Date: Monday, February 24, 2020 |



Setting:
1. *PS8747_I2C_CTRL=L, I2C disable*
2. *PS8747_SCLTDPEQ=L, DP Receiver equalization Compensation for channel loss up to 7dB*
3. *PS8747_SDA/CEQ=L, USB Type-C connector facing RX channel receiver equalization setting Compensation*
4. *ADDR/DCTCFG=M, Automatic DCI mode entering enabled for channel loss up to 7dB*
5. *CDE/DCICLK=L,When NO DCI mode-->USB Type-C connector facing TX channel De-emphasis setting -3.5dB Output De-emphasis(default)*
6. *SSDE/DCIDAT=L,When NO DCI mode-->USB HOST facing TX channel De-emphasis setting -3.5dB Output De-emphasis(default)*

Security Classification	LC Future Center Secret Data		
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Title	DDI Redriver PS8330
Size	C
Document Number	¥540
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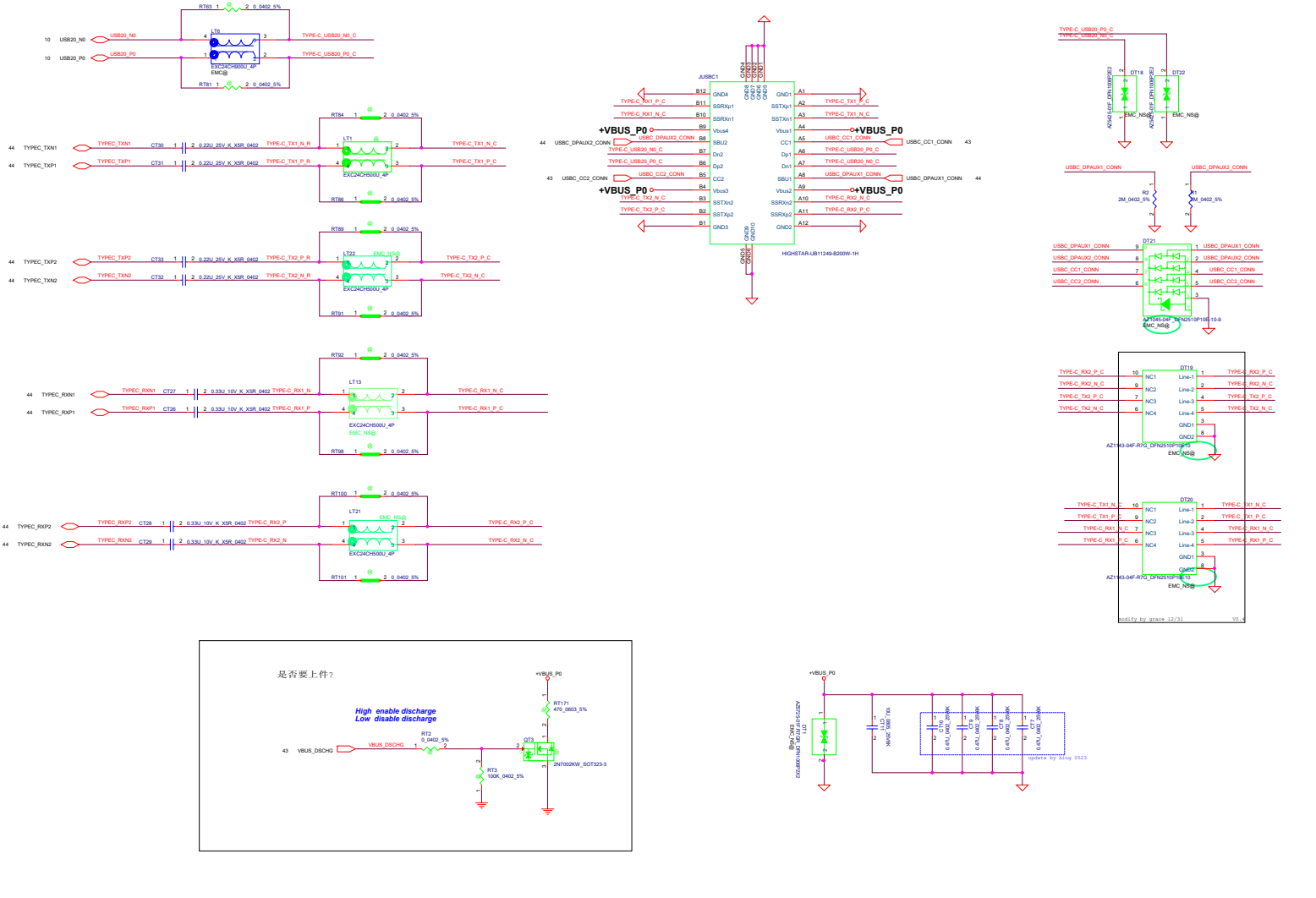

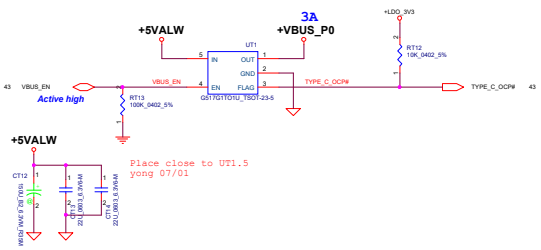

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

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Title	USB TYPE-C Port	
Size: Custom	Document Number: Y540	Rev: 1.0
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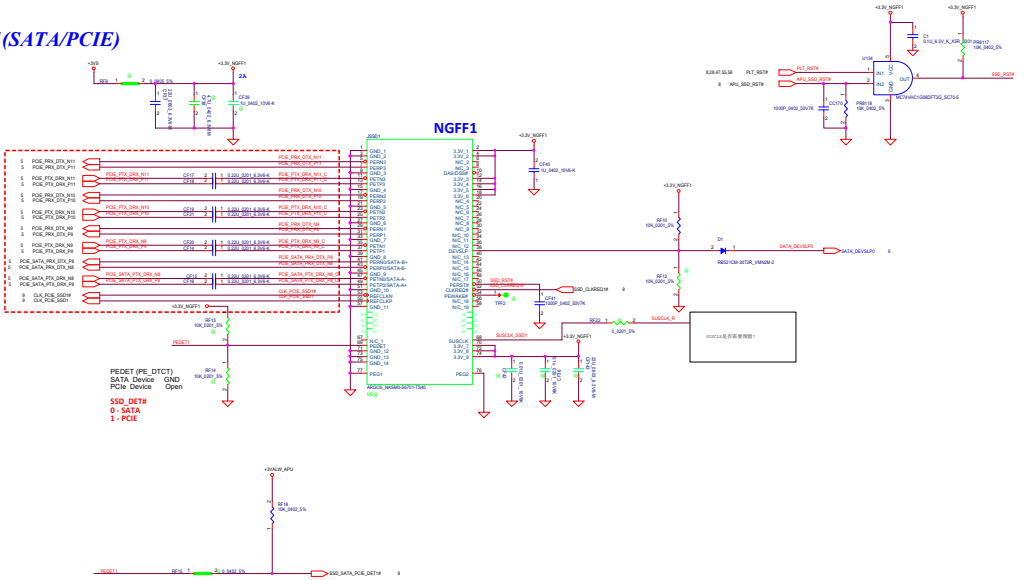
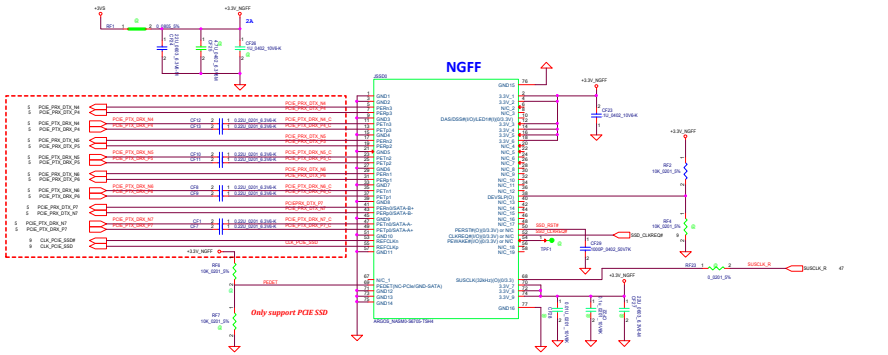
M.2 SSD1(SATA/PCIE)



M.2 SSD0(PCIE)



Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

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Title: NGFF WLAN

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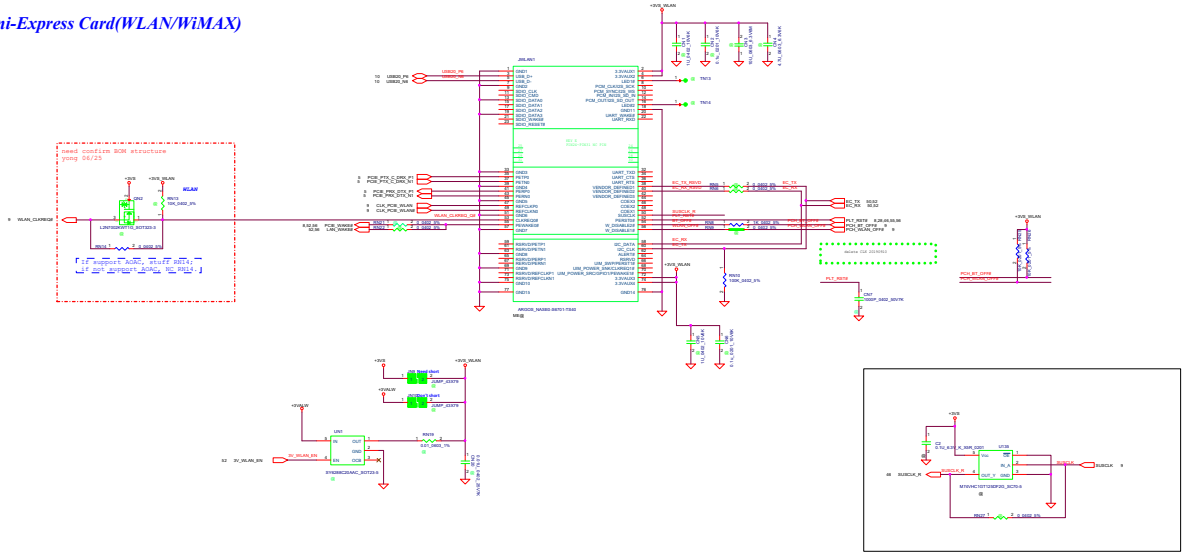
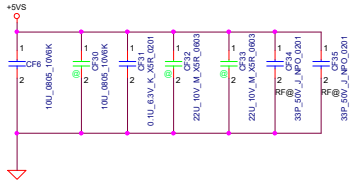
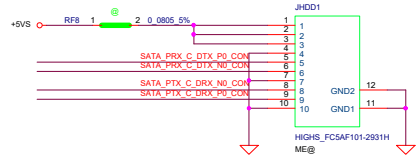
Mini-Express Card(WLAN/WiMAX)



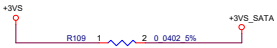
File:	<Title>		
Size: A	Document Number <Doc>		Rev: 1.0
Date: Monday, February 04, 2013		Sheet 49 of 63	

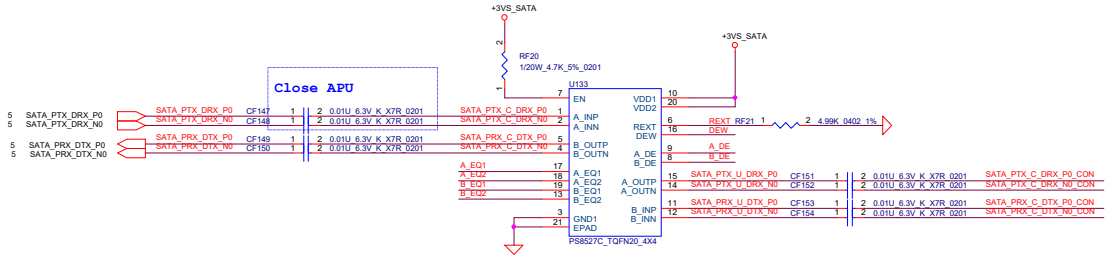
SATA HDD Conn.

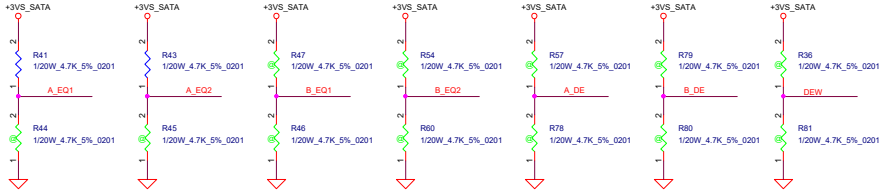




SATA HDD Redriver(NEW ADD 20190614)



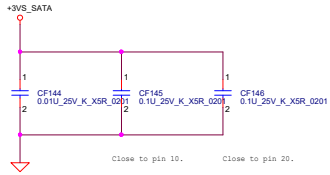




Equalization level setting for Channel x(x=A/B), internally tied to VDD/2
[x_EQ2, x_EQ1] ==
L/H: for channel loss up to 2.4dB
L/L: for channel loss up to 7.4dB
L/H: for channel loss up to 14.4dB
M/H: for channel loss up to 12.2dB (default)
M/L: for channel loss up to 9.4dB
H/H: for channel loss up to 13.3dB
H/M: for channel loss up to 6.2dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB

De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2
[x_DE] ==
M: -3.5dB (default)
L: 0dB
H: -6dB

De-emphasis width adjustment, internally pulled down
[DEW] ==
H: for SATA3(default)
L: for SATA3
H: for SATA2



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Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title	HDD/XBOX CONN		
Size	Document Number		Rev
Custom	Y540		1.0
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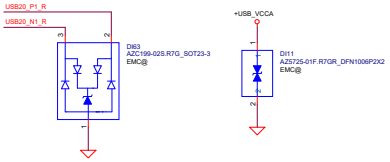
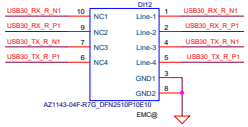
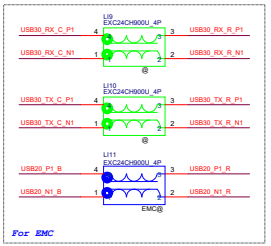
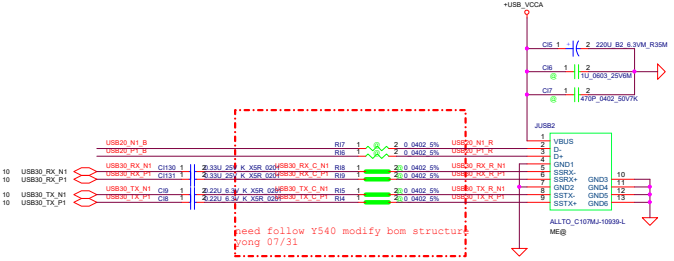




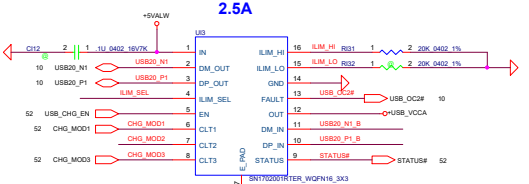
For EMC

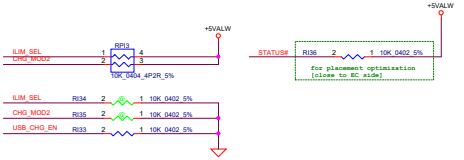


For EMC



USB charger
2.5A





CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT held low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title	USB2.0/USB3.0 PORT (LEFT)		
Size C	Document Number Y540		Rev 1.0
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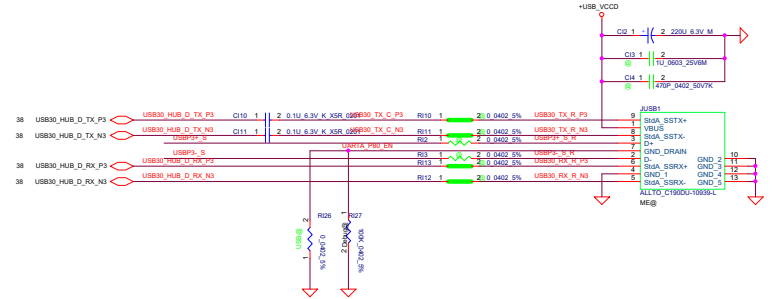
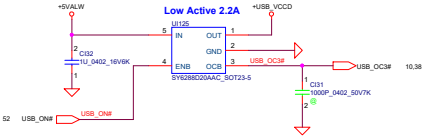
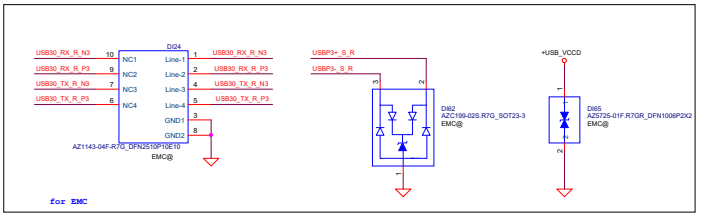
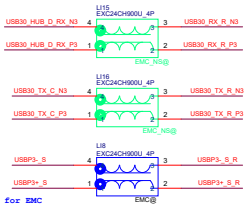


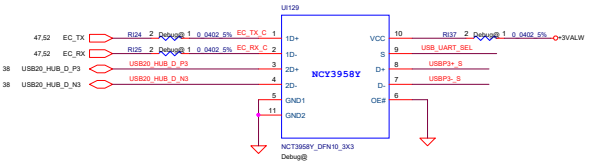
USB3.1 PORT x2



For USB Debug Function



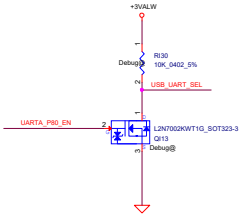




USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D1(+/-) to 1D1(+/-)
L	H	D1(+/-) to 2D1(+/-)



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Issued Date	2019/07/02	Deciphered Date	2020/02/24

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Title	Size	Document Number	Rev
USB2.0	C	¥540	1.0
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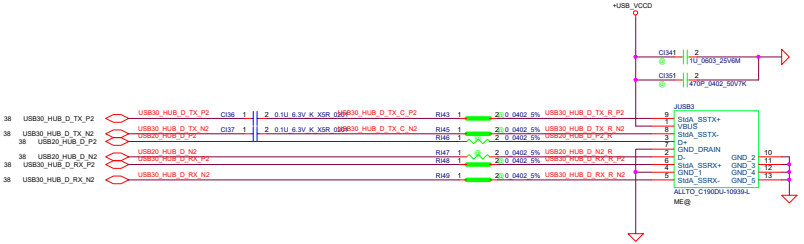

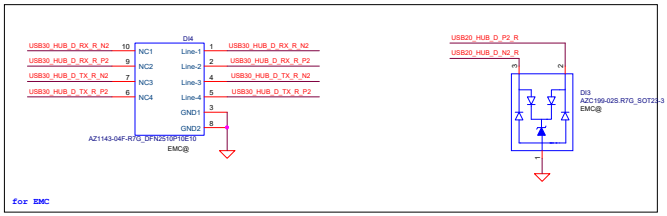

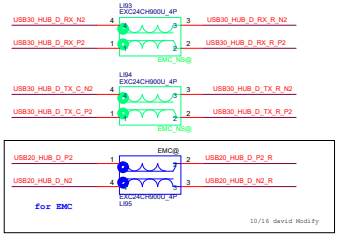

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

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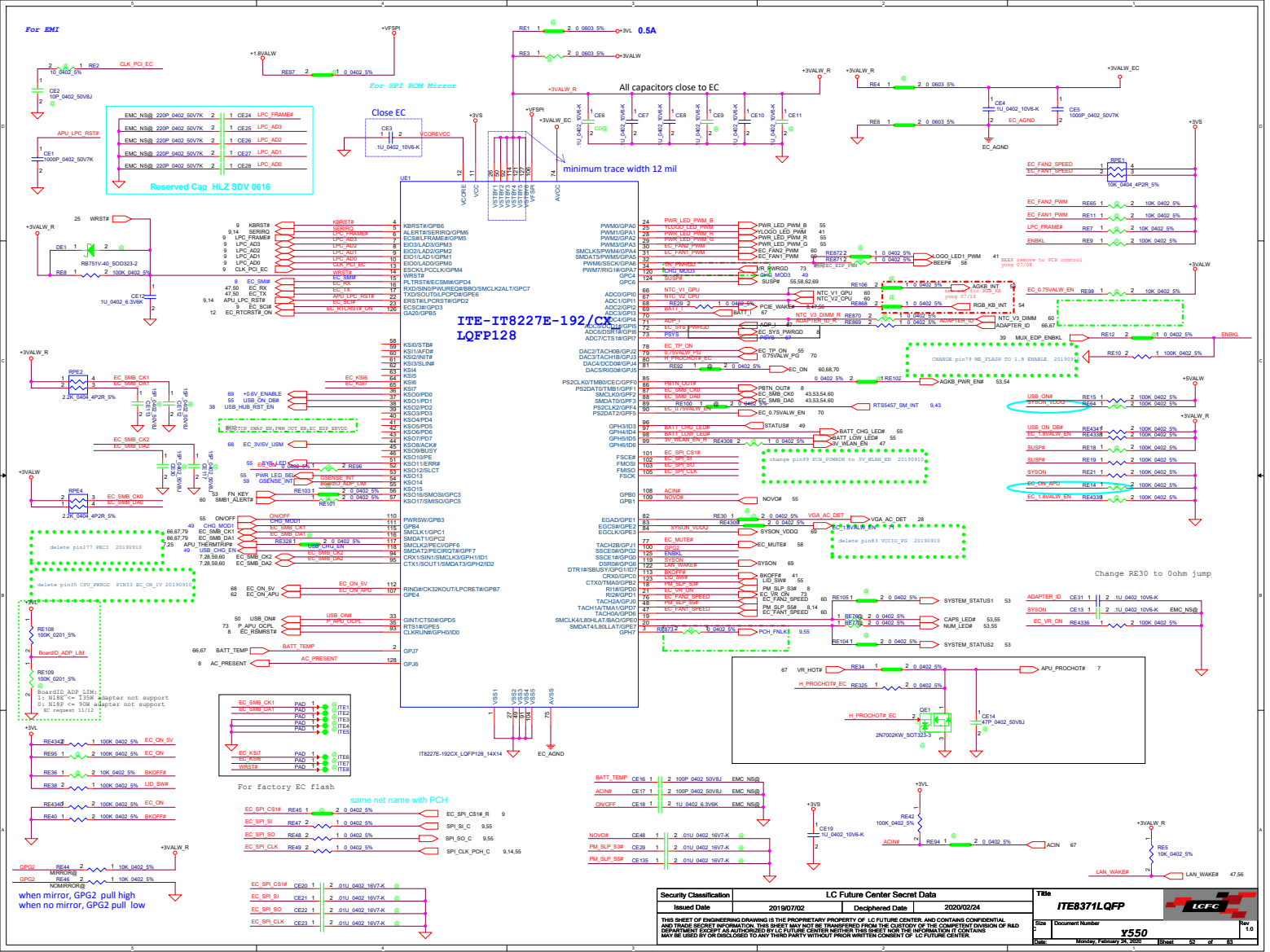
Title	USB2.0	
Size C	Document Number ¥540	Rev 1.0
Date: Monday, February 24, 2020	Sheet 51 of 83	


For EMI
0.5A
All capacitors close to EC
Close EC
minimum trace width 12 mil
For SPI ROM Mirror
Reserved Cap HLZ SDV 0616
ITE-IT8227E-192/CX
LQFP128
IT8227E-192CX_LQFP128_14X14
For factory EC flash
same net name with PCH
Change RE30 to 0ohm jump
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
Security Classification
LC Future Center Secret Data
Issued Date
2019/07/02
Deciphered Date
2020/02/24
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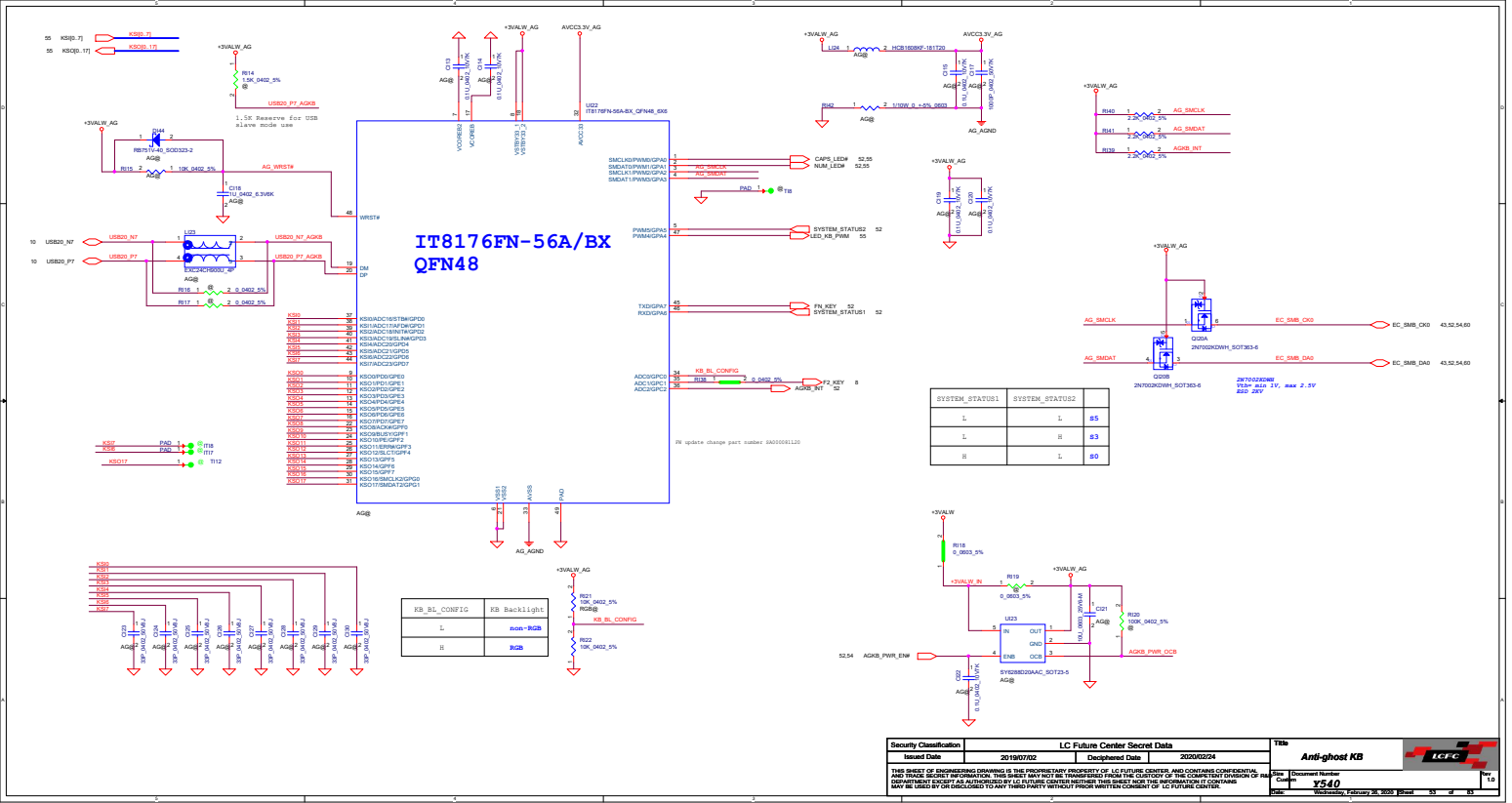
Title
ITE8371LQFP
Size
C
Document Number
Y550
Rev
1.0
Date:
Monday, February 24, 2020
Sheet
52
of
83



SYSTEM_STATUS1	SYSTEM_STATUS2	
L	L	85
L	H	83
H	L	80

KB_BL_CONFIG	KB Backlight
L	non-RGB
H	RGB

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

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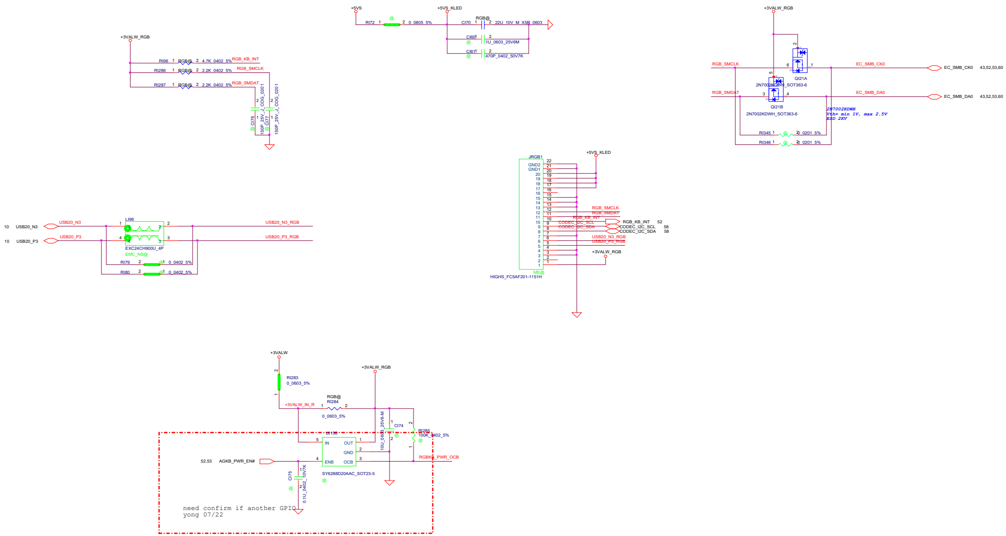
Title: Anti-ghost KB

Size	Document Number	Rev
Custom	Y540	1.0

Date: Wednesday, February 26, 2020 Sheet 53 of 83

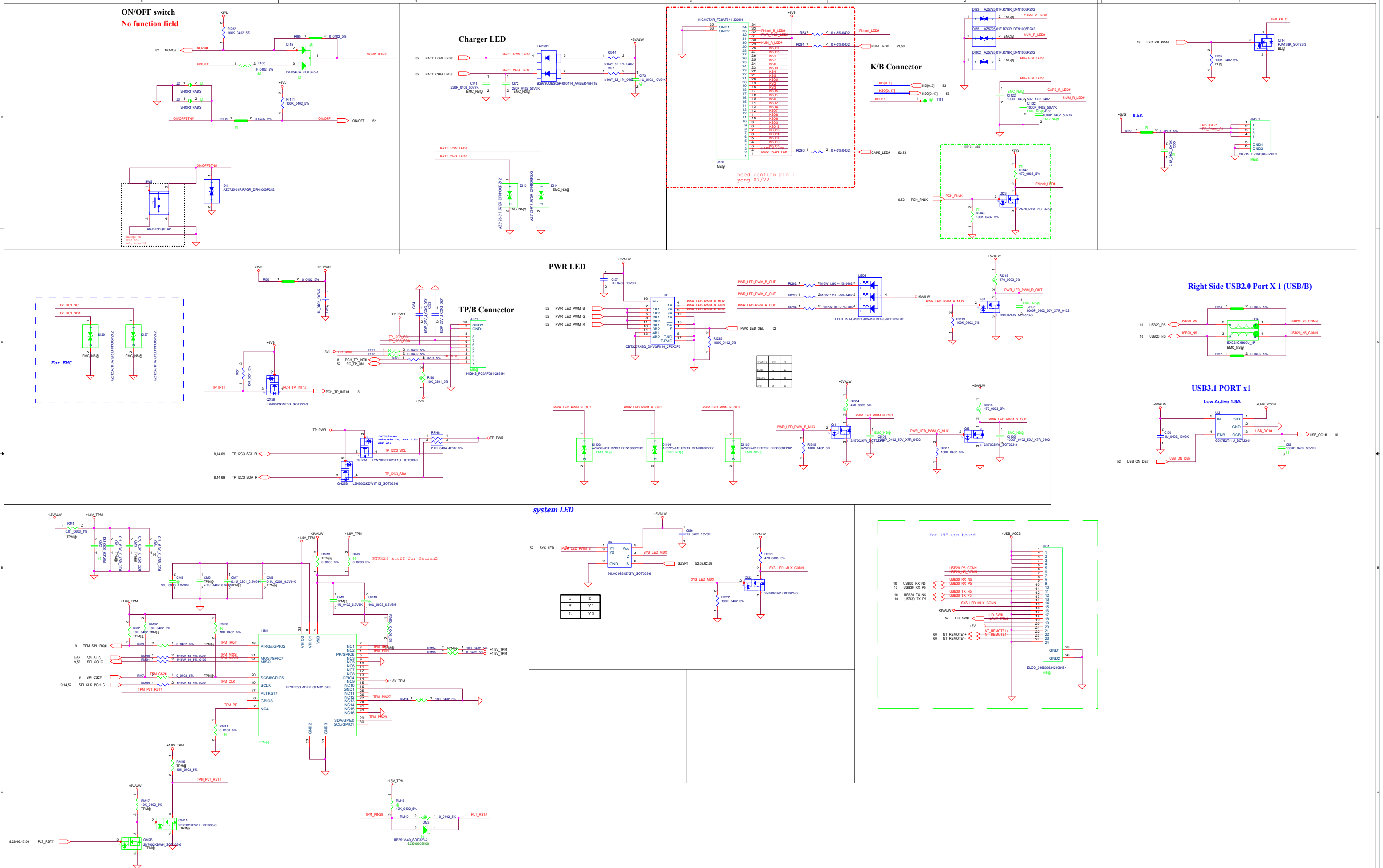


Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title
RGB KB

Size	Document Number	Rev
D	Y540	1.0

Date: Monday, February 24, 2020



Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

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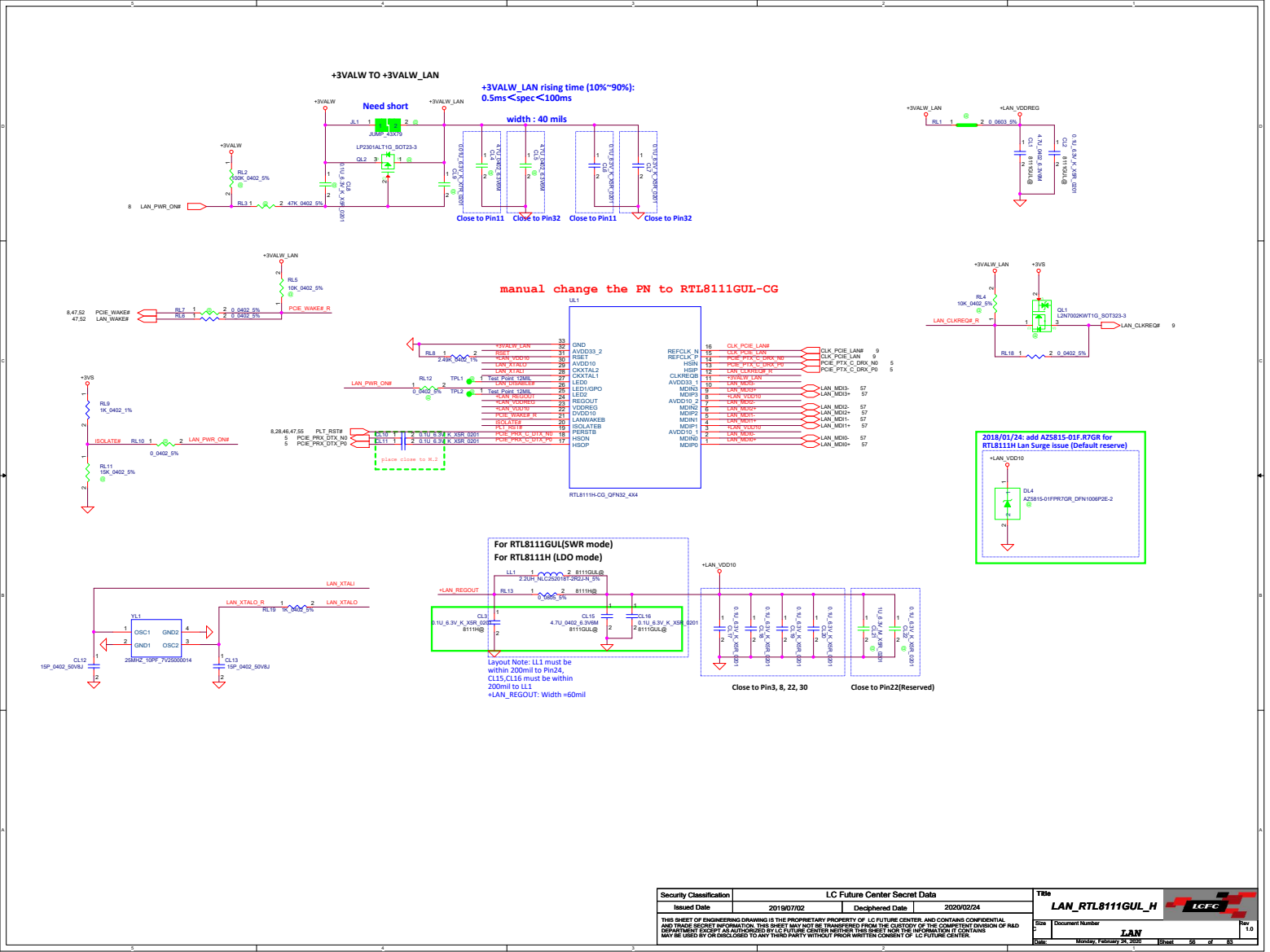
Title: KBD/PWR/IO/LED/TP Conn.

Size: Custom — Document Number: Y540 — Rev: 1.0

Date: Wednesday, March 04, 2020 — Sheet 55 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

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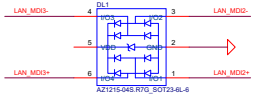
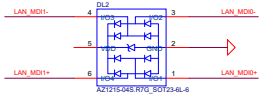
Title: LAN_RTL8111GUL_H

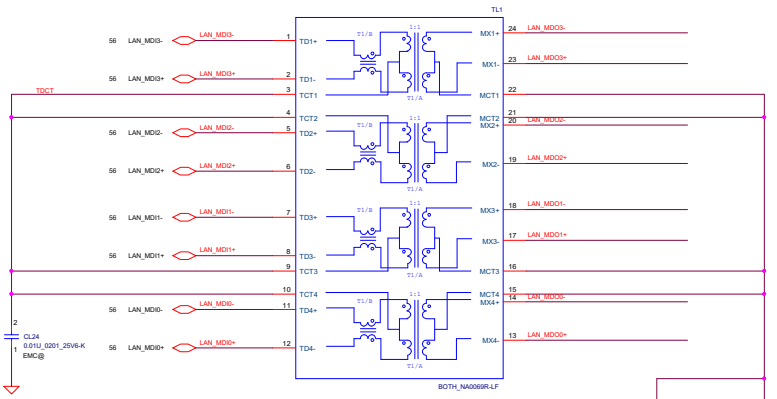
Size	Document Number	Rev
C	LAN	1.0

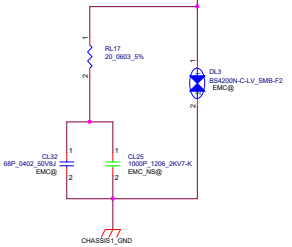
Date: Monday, February 24, 2020 Sheet 56 of 83

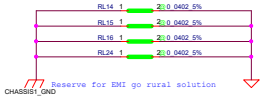
DL1/DL2
1'S PN:SC300005900
Place Close to TL1

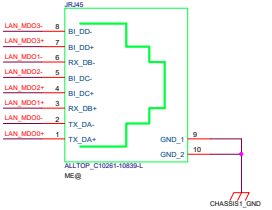






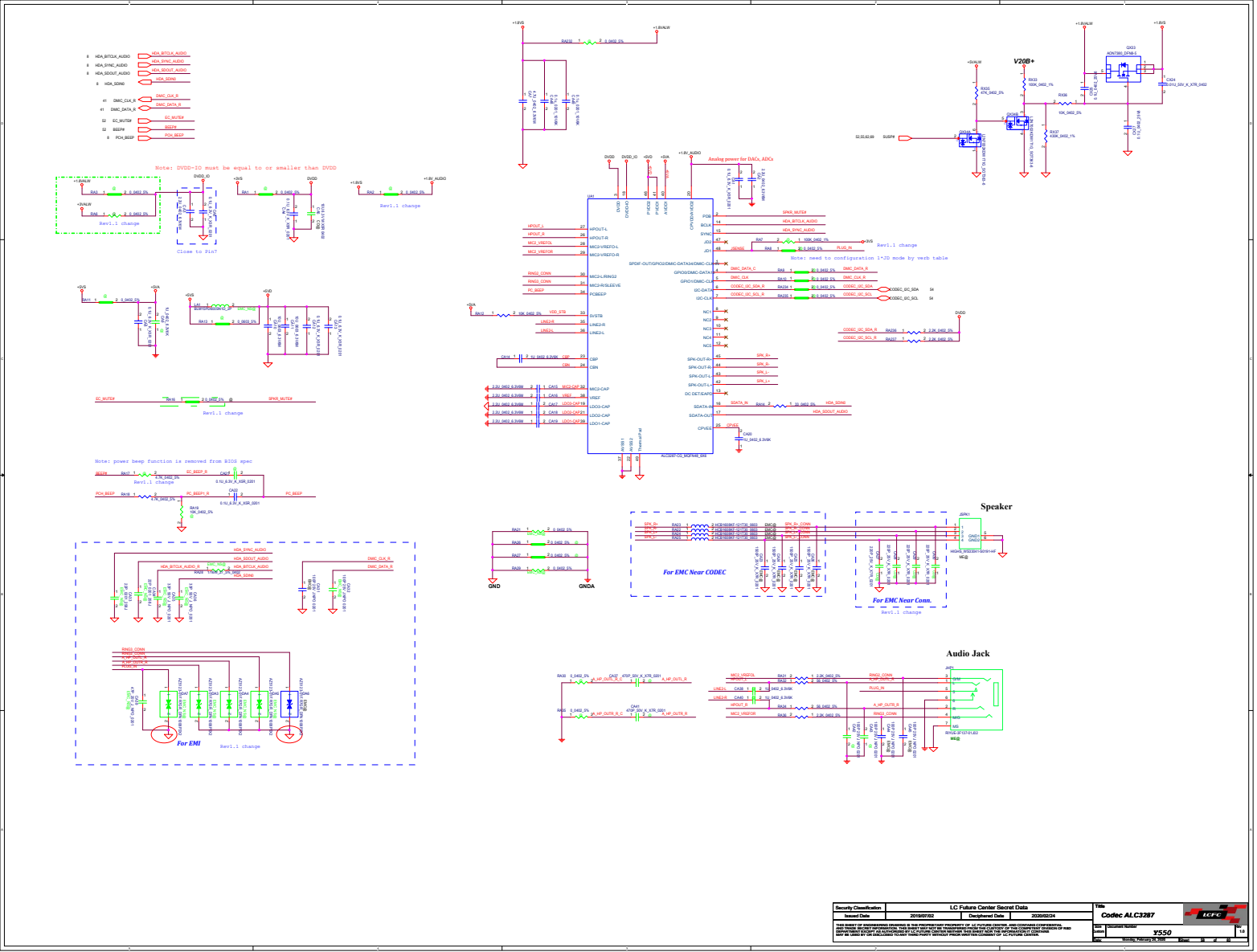






Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title	LAN_Transformer		
Size	Document Number		Rev
C	Y540		1.0
Date:	Monday, February 24, 2020	Sheet	57 of 83


Note: DVDD-IO must be equal to or smaller than DVDD
Close to Pin7
Rev1.1 change
Analog power for DACs, ADCs
Note: need to configuration I*JD mode by verb table
Note: power beep function is removed from BIOS spec
For EMI
For EMC Near CODEC
For EMC Near Conn.
Speaker
Audio Jack
V20B+
Codec ALC3287
Y550
LC Future Center Secret Data
Issued Date 2015/07/02
Deciphered Date 2030/02/24
Monday, February 24, 2020

APS G-Sensor

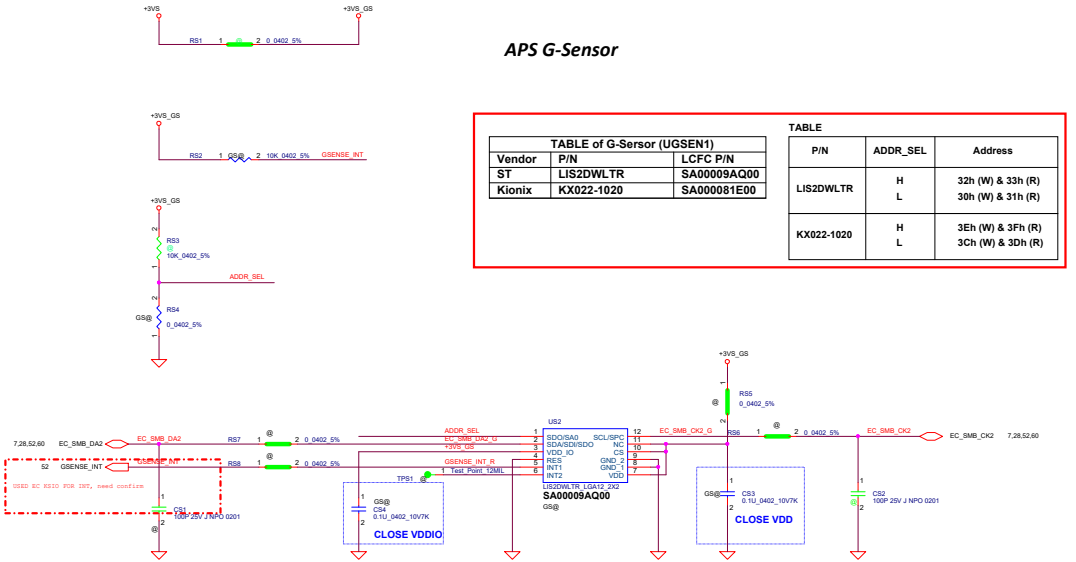


TABLE of G-Sersor (UGSEN1)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
Kionix	KX022-1020	SA000081E00

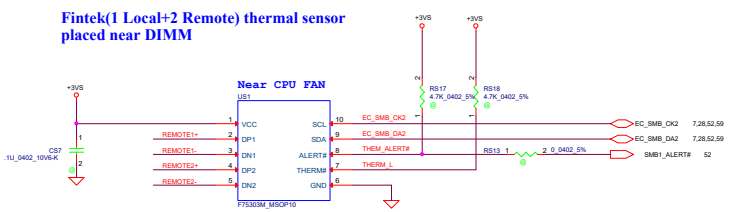
TABLE

P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

Title			
USB2.0			
Size: C	Document Number: ¥540		Rev: 1.0
Date: Monday, February 24, 2020	Sheet 59 of 83		

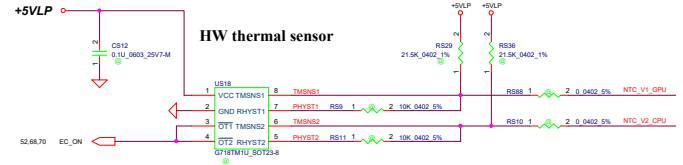
Fintek(1 Local+2 Remote) thermal sensor placed near DIMM



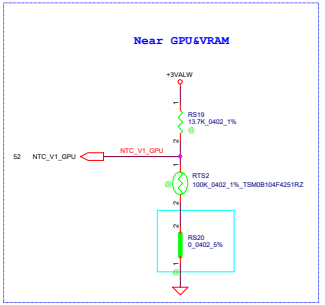
REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:

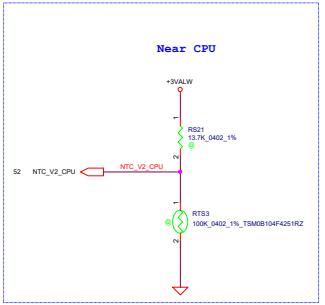
Trace width/space:10/10 mil
Trace length:<8"

HW thermal sensor

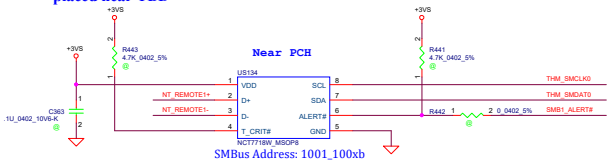


over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C





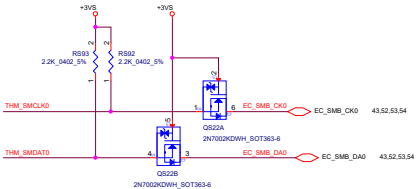
Nuvoton(1 Local+1 Remote) thermal sensor placed near TBD

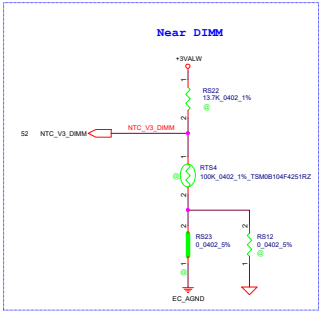


SMBus Address: 1001_100xb

Thermal Diode Near GPU FAN(DB)
NT_REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"

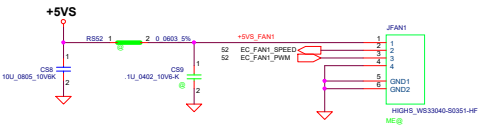
for layout optimized, change the EC_AGND to GND



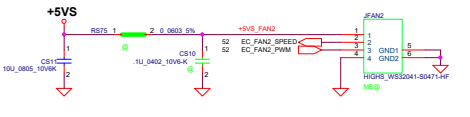


Address 1001_101xb

FAN Conn Right



FAN Conn LEFT



Security Classification	LC Future Center Secret Data			Title
Issued Date	2019/07/02	Deciphered Date	2020/02/24	Thermal sensor/FAN CONN

Size	Document Number	Rev
C	X540	1.0

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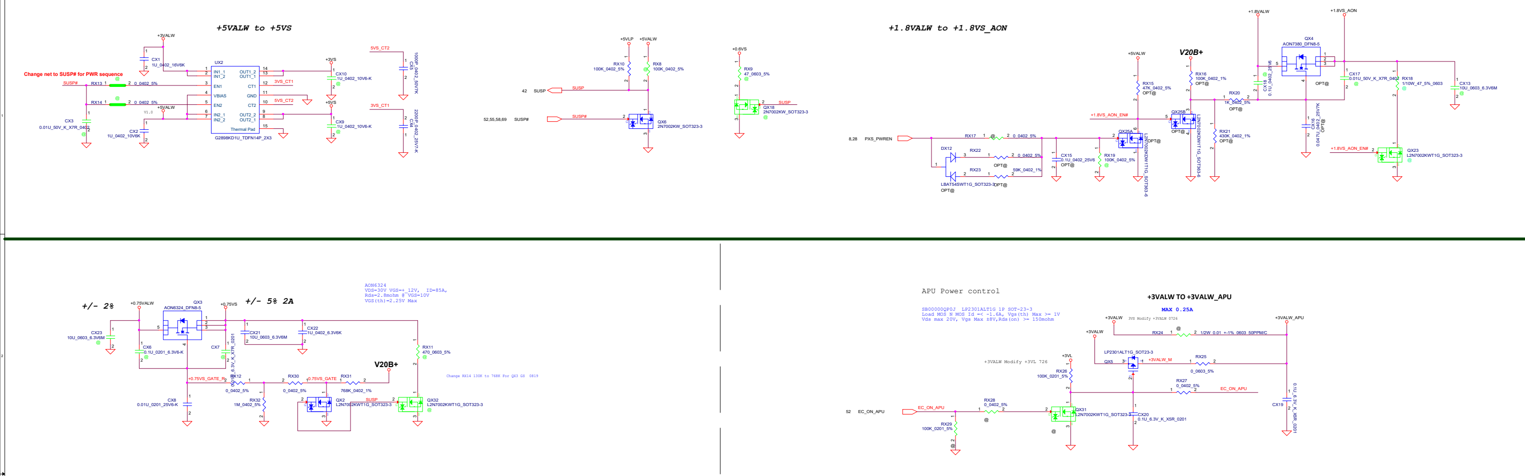
Title

XDP

Size	Document Number	Rev
Custom	X540	1.0

Date: Monday, February 24, 2020 Sheet 61 of 63



Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

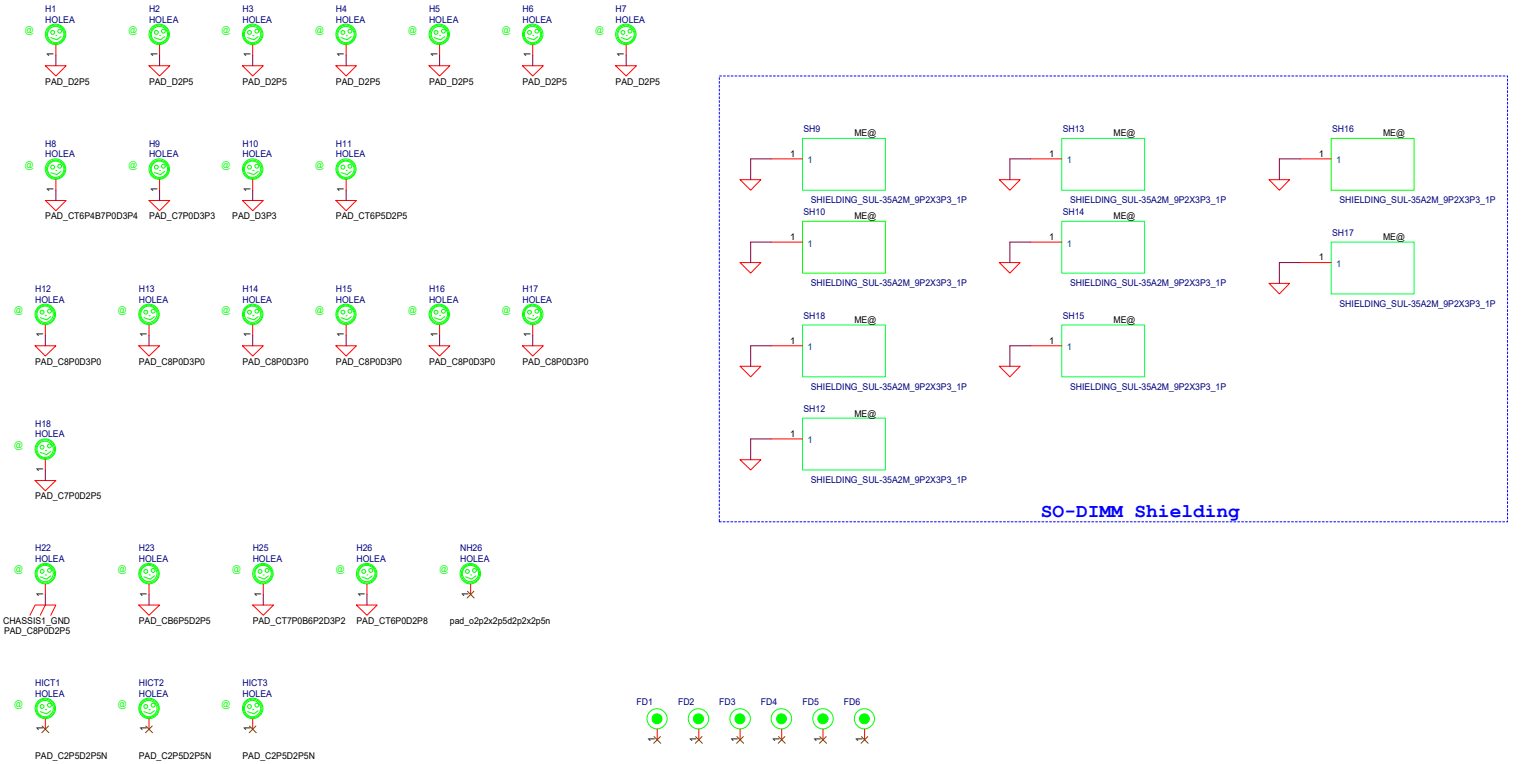
Title: DC V TO VS INTERFACE

LCFC

Size: D | Document Number: Y540 | Rev: 1.0

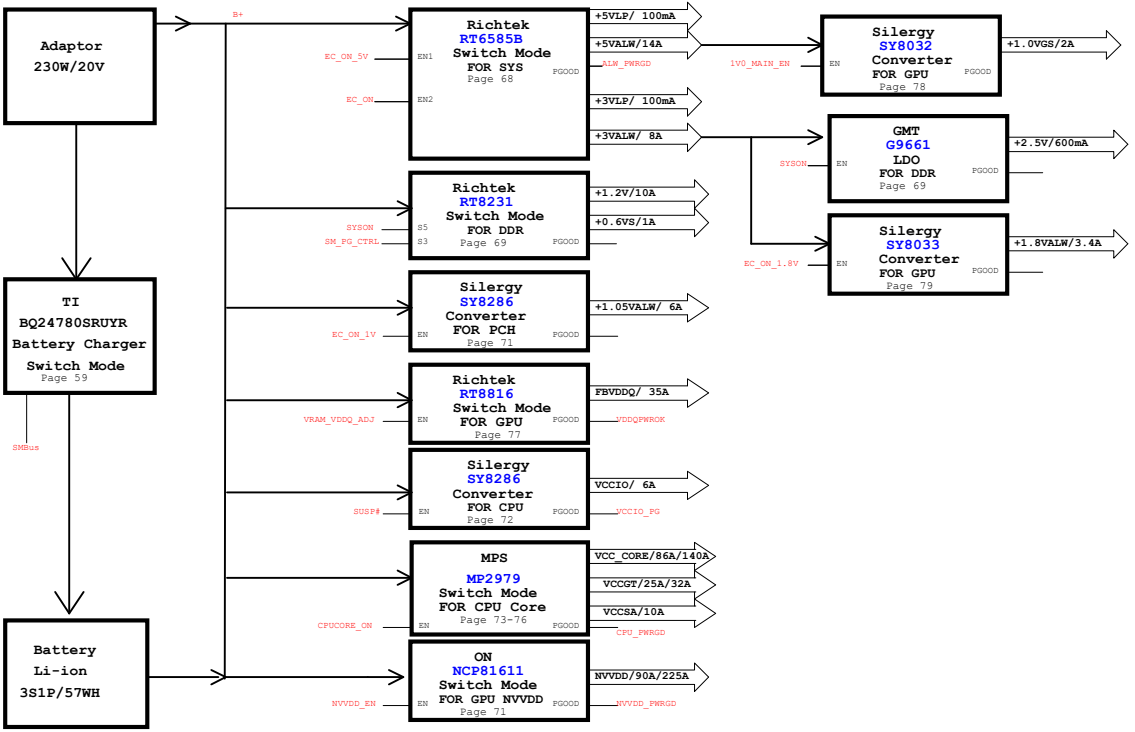
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	*Virtual symbol*		
Size	Document Number		Rev
C	¥550		0.1
Date:	Thursday, February 27, 2020	Sheet	83 of 83



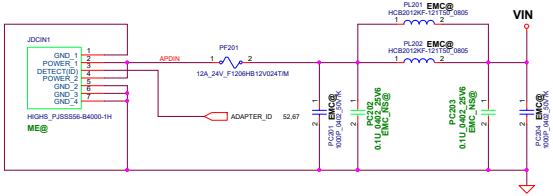
Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2020/02/24

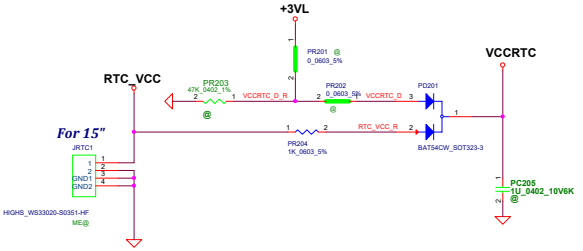
Title	Hole		
Size B	Document Number ¥550		Rev 1.0
Date:	Monday, February 24, 2020	Sheet 64 of 83	

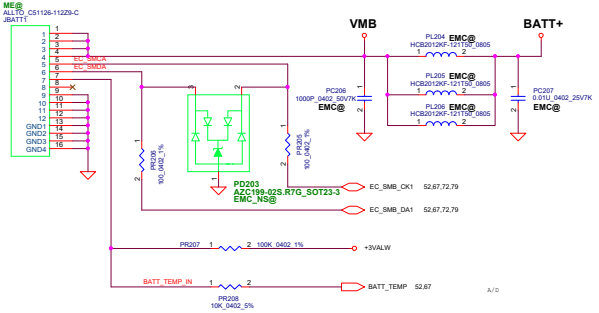


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	Power Diagram		
Size	Document Number		Rev
Custom	Y550		6.1
Date:	Wednesday, February 26, 2020	Sheet	65 of 83

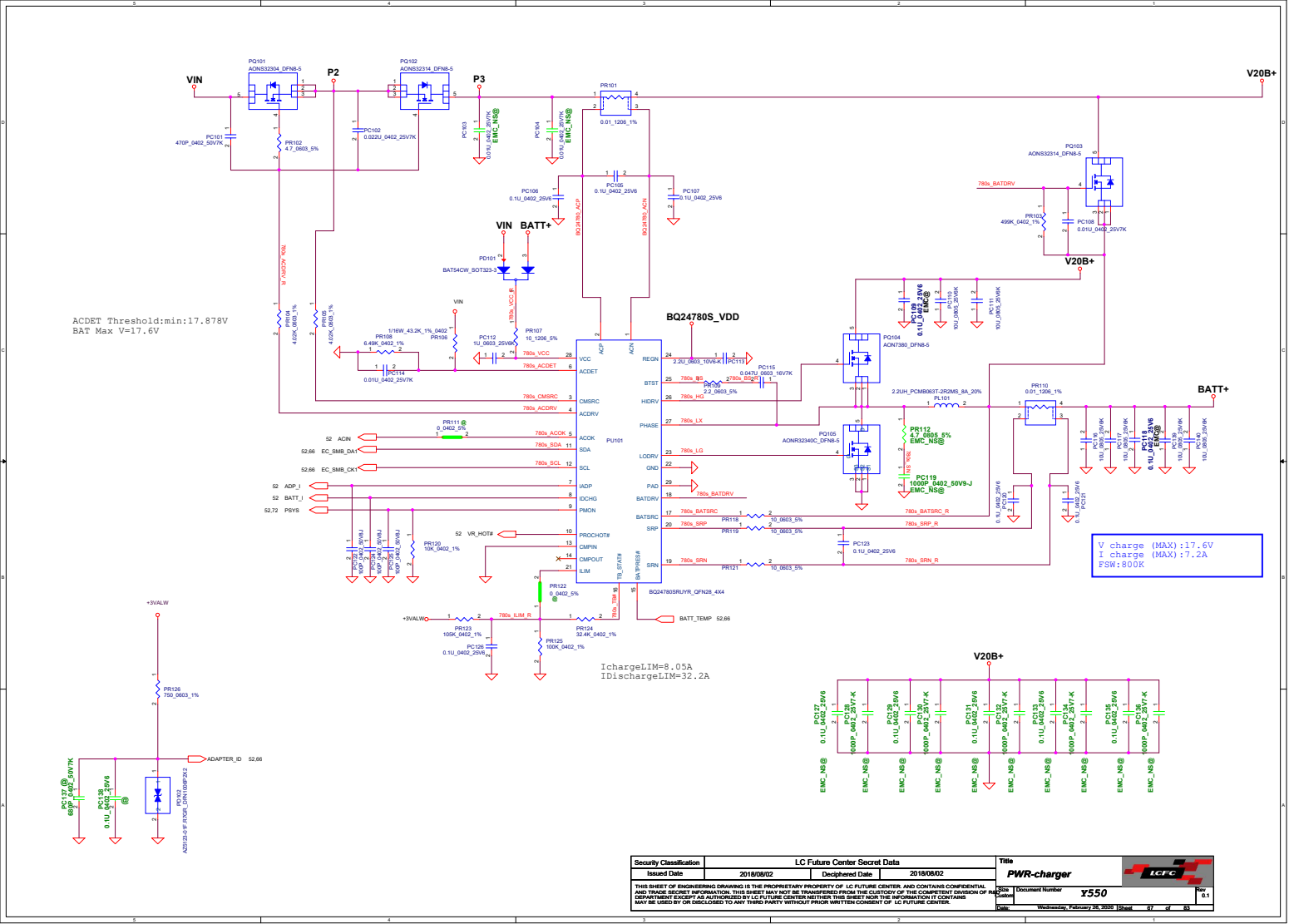






Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-DCIN/BATT/RTC		
Size C	Document Number Y550		Rev 0.1
Date: Wednesday, February 26, 2020	Sheet 66 of 83		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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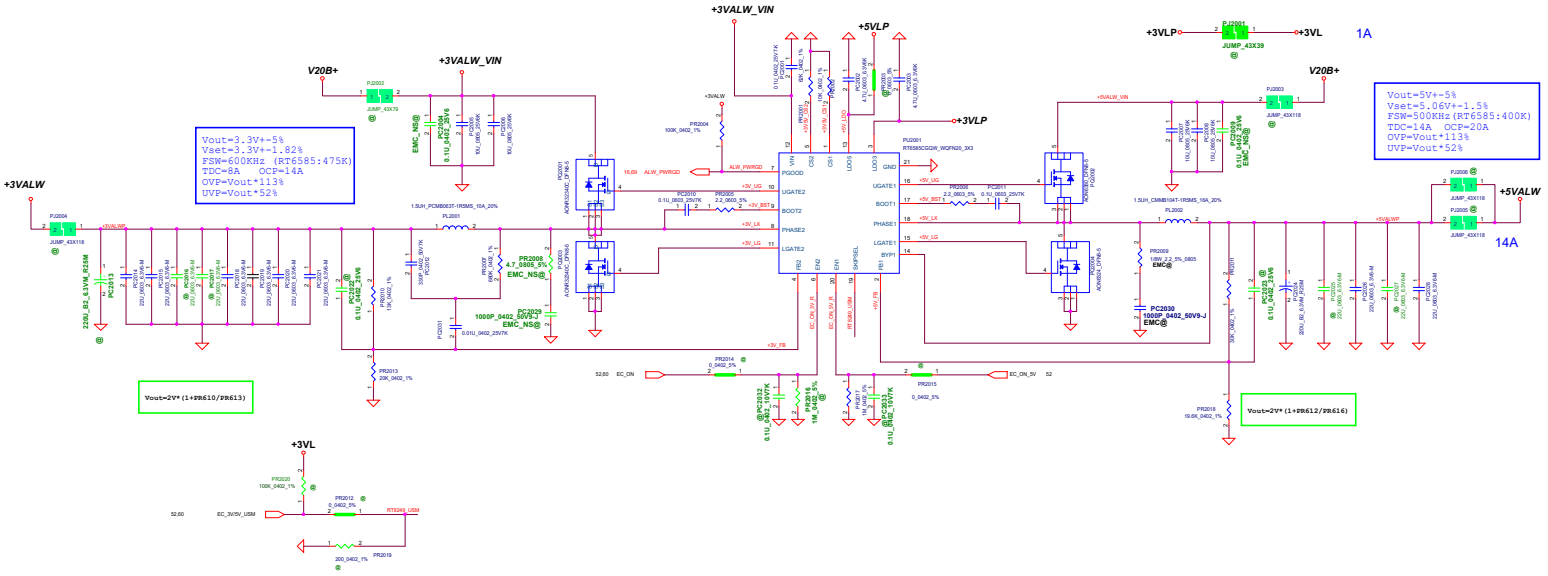
Title: PWR-charger

Size	Document Number	Rev
Custom	Y550	0.1

Date: Wednesday, February 26, 2020 Sheet 67 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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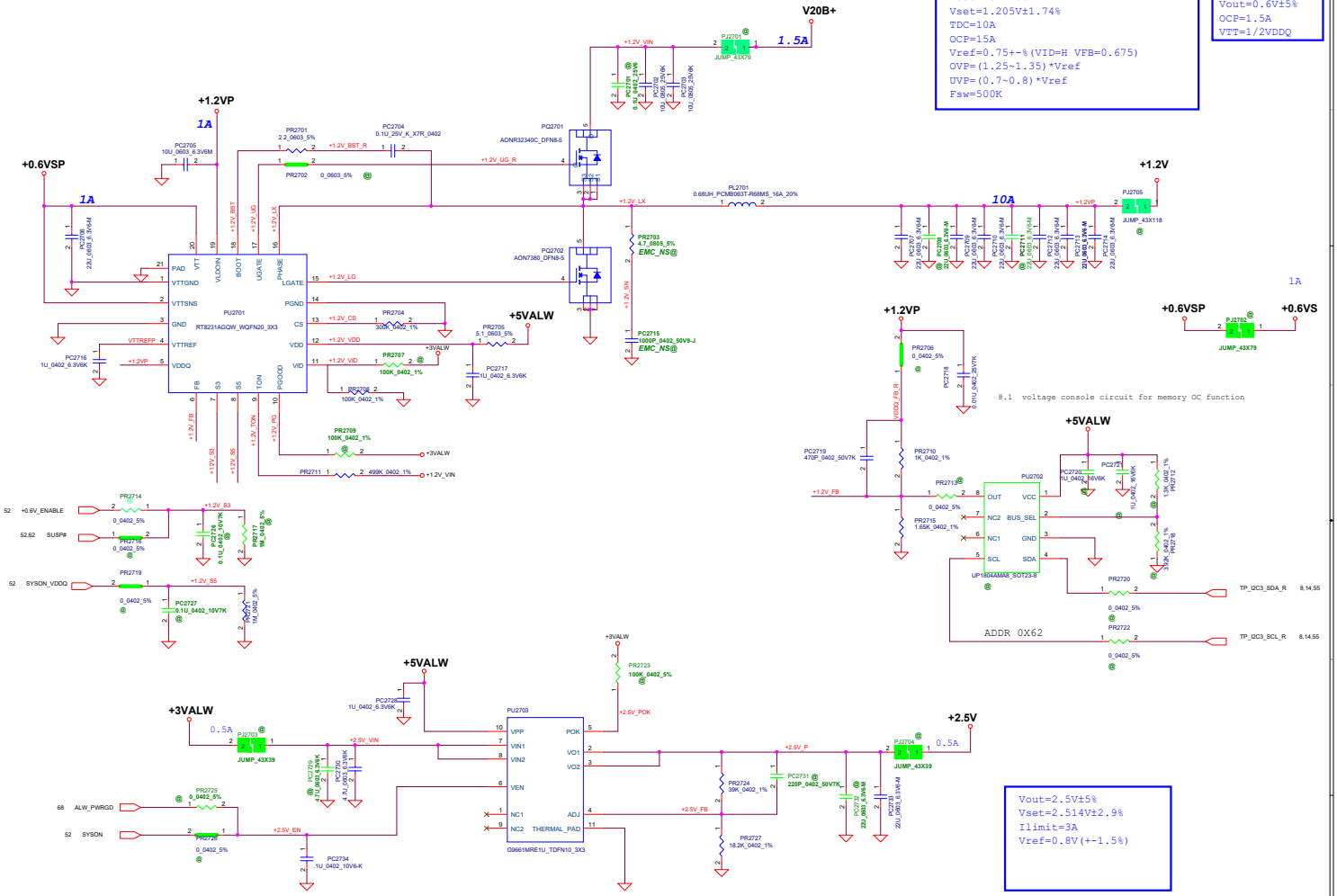
Title	PWR-3/5VALW		
Size: Custom	Document Number: Y550		Rev: 0.1
Date: Wednesday, February 26, 2020	Sheet 68 of 83		



STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

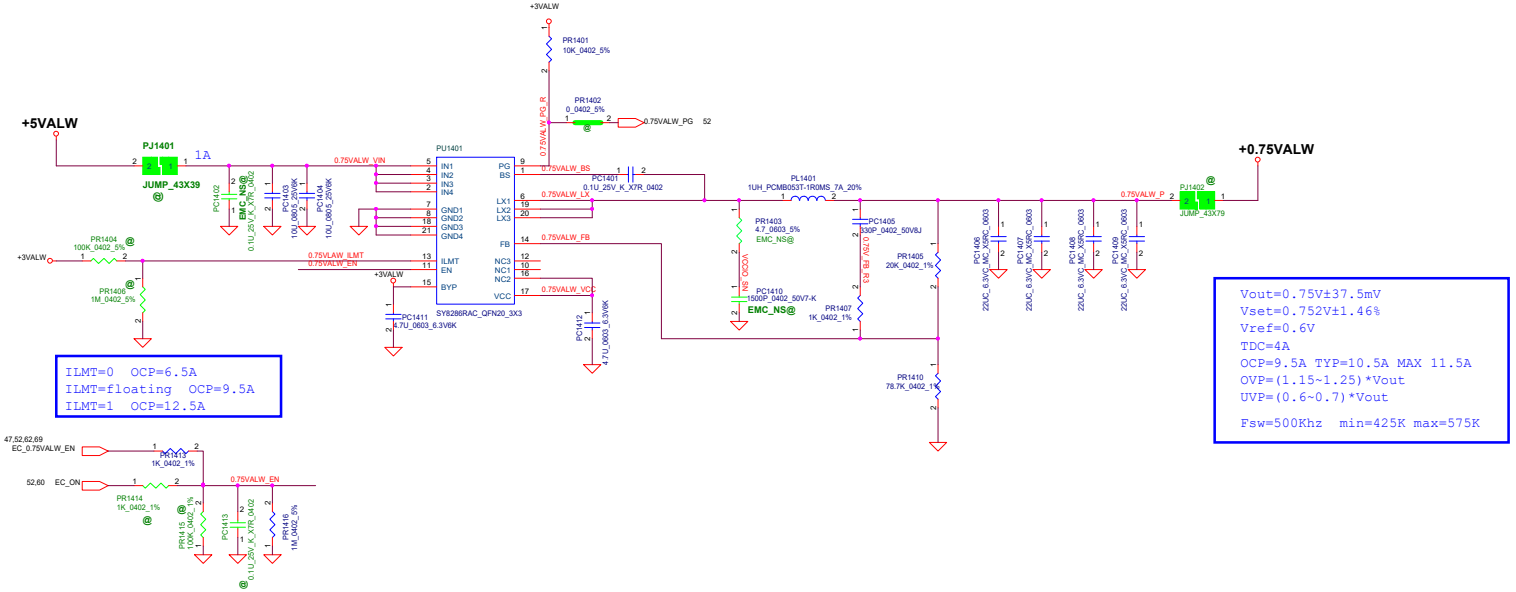
Address	0X6A	0X68	0X66	0X64	0X62	0X60
TOP R (Kohm)	OPEN	3.9	3	2.3	1.3	10
BOT R (Kohm)	10	1.3	2.3	3	3.9	OPEN
Bus_sel Volt (% of VCC)	0%	25%	40%	60%	75%	100%

Security Classification	LC Future Center Secret Data		
Issued Date	2019/07/02	Deciphered Date	2019/07/02

Title: PWR-VDDQ/VTT

Size	Document Number	Rev
Custom	¥550	0.1

Date: Wednesday, February 26, 2020 Sheet 69 of 83

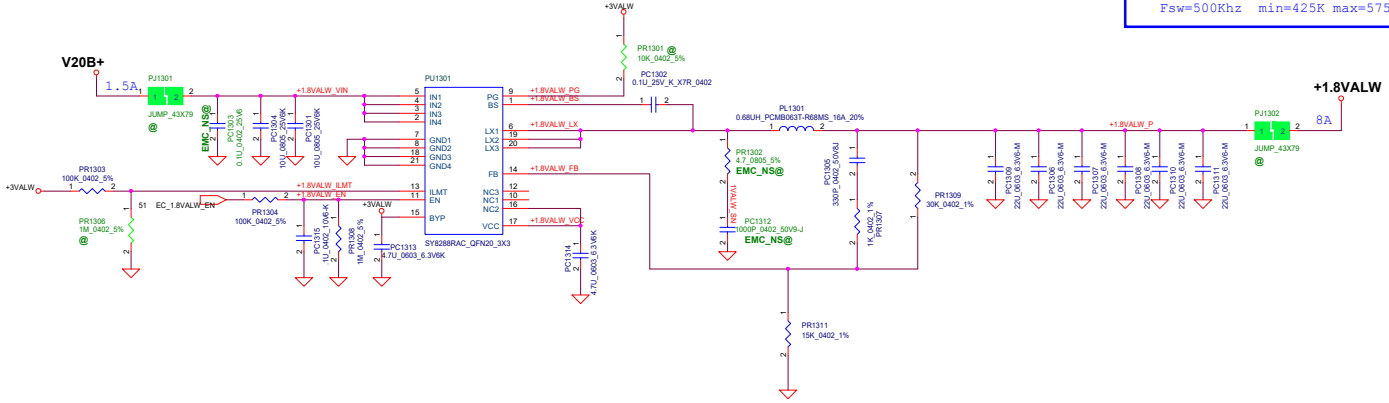


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-VCCIO

Size	Document Number	Rev
Custom	¥550	0.1

Date: Wednesday, February 26, 2020 Sheet 70 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-1.0VALW**

Size	Document Number	Rev
Custom	¥550	0.1

Date: Wednesday, February 26, 2020 Sheet 71 of 83

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *Blank*

Size: C | Document Number: *¥550* | Rev: 0.1

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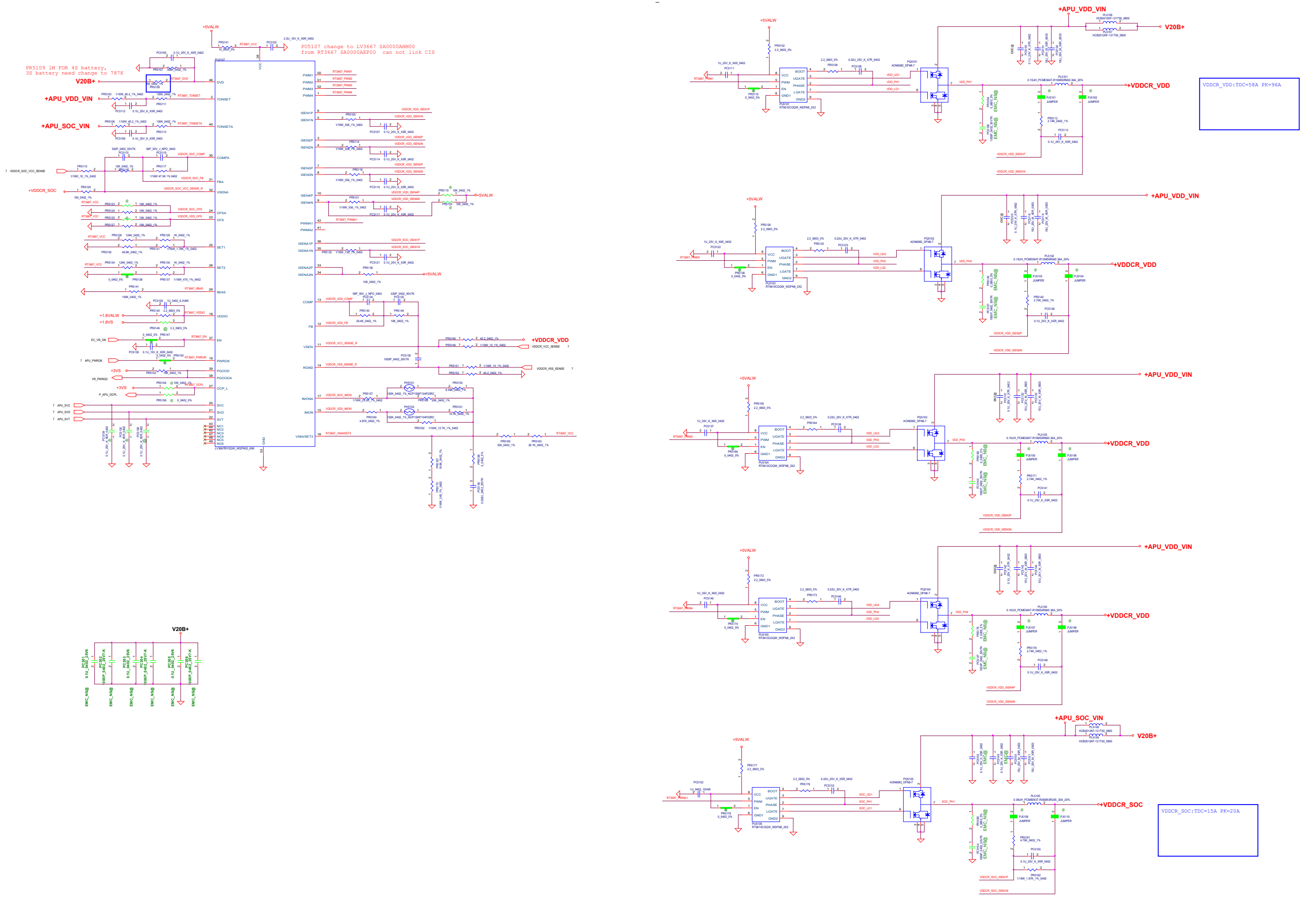

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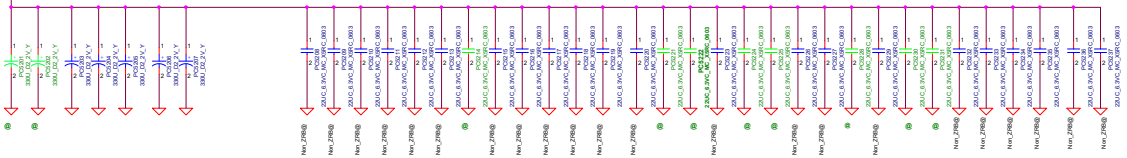
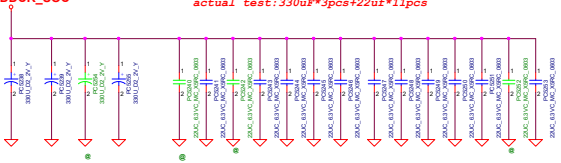
+VDDCR_VDD

Vendor suggest:330uF*7PCS+22uF*30PCS
actual test:330uF*5pcs+22uF*22pcs



+VDDCR_SOC

Vendor suggest:330uF*1PCS+470uF*1pcs+22uF*12PCS
actual test:330uF*3pcs+22uF*11pcs



Security Classification	LC Future Center Secret Data		
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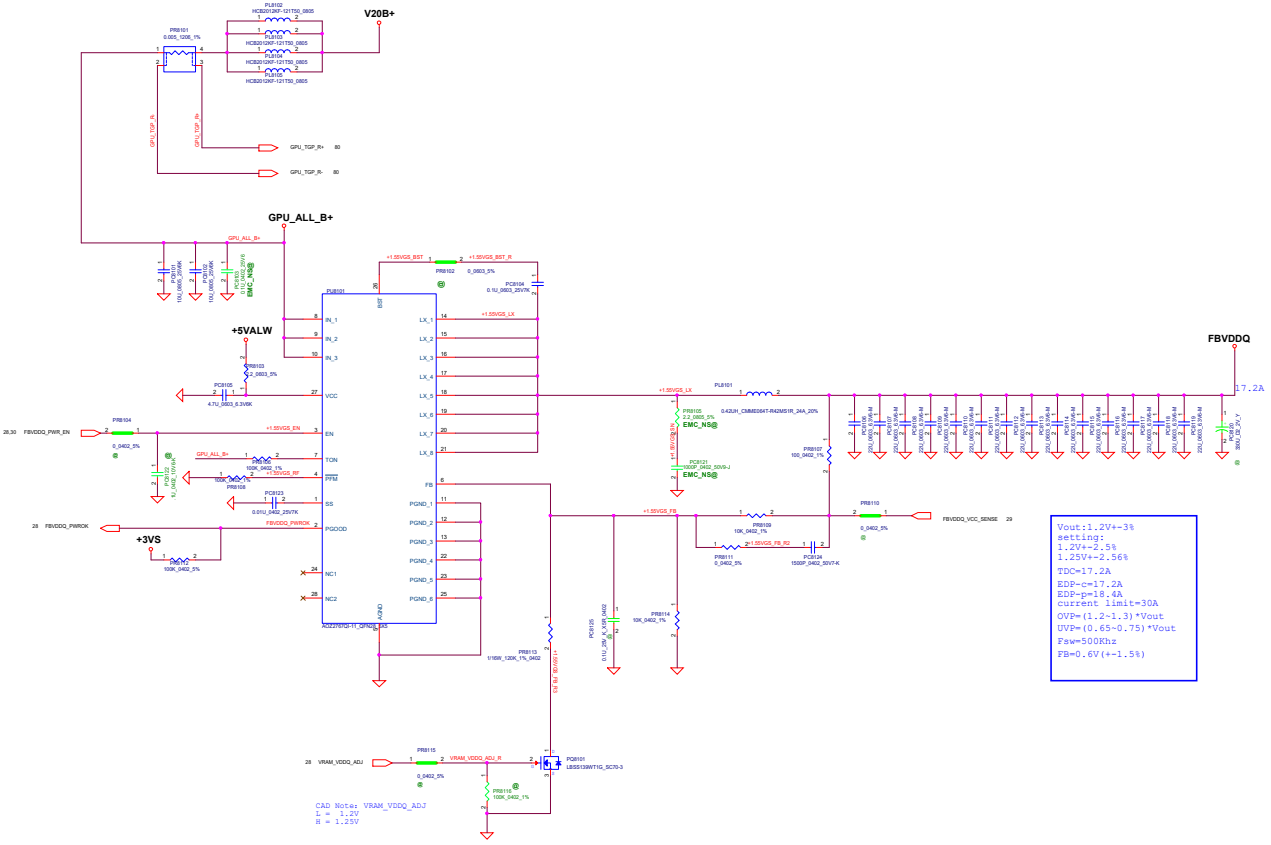

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Title	PWR-FBVDDQ		
Size: Custom	Document Number: Y540		Rev: 0.1
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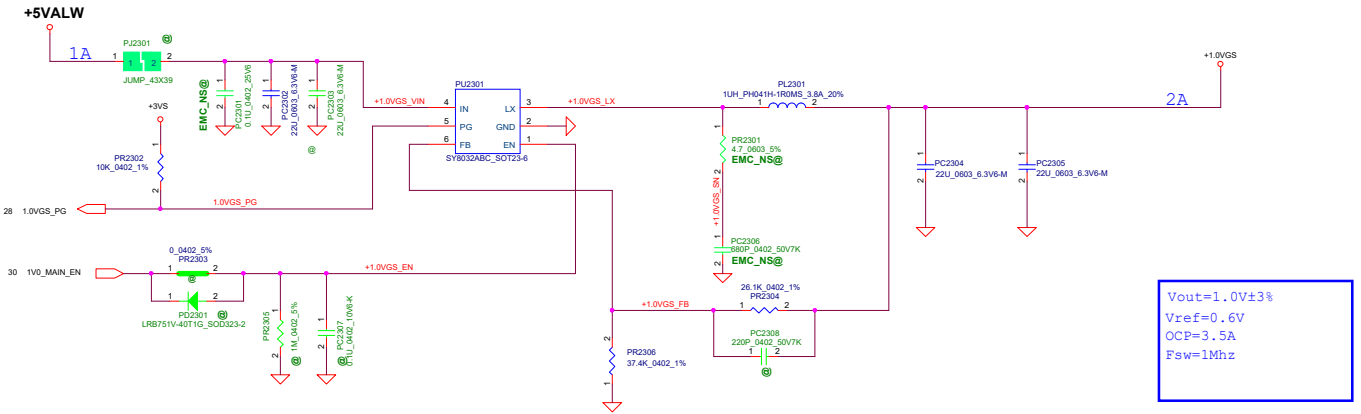

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-1.8/1.0VGS		
Size: Custom	Document Number: Y550		Rev: 0.1
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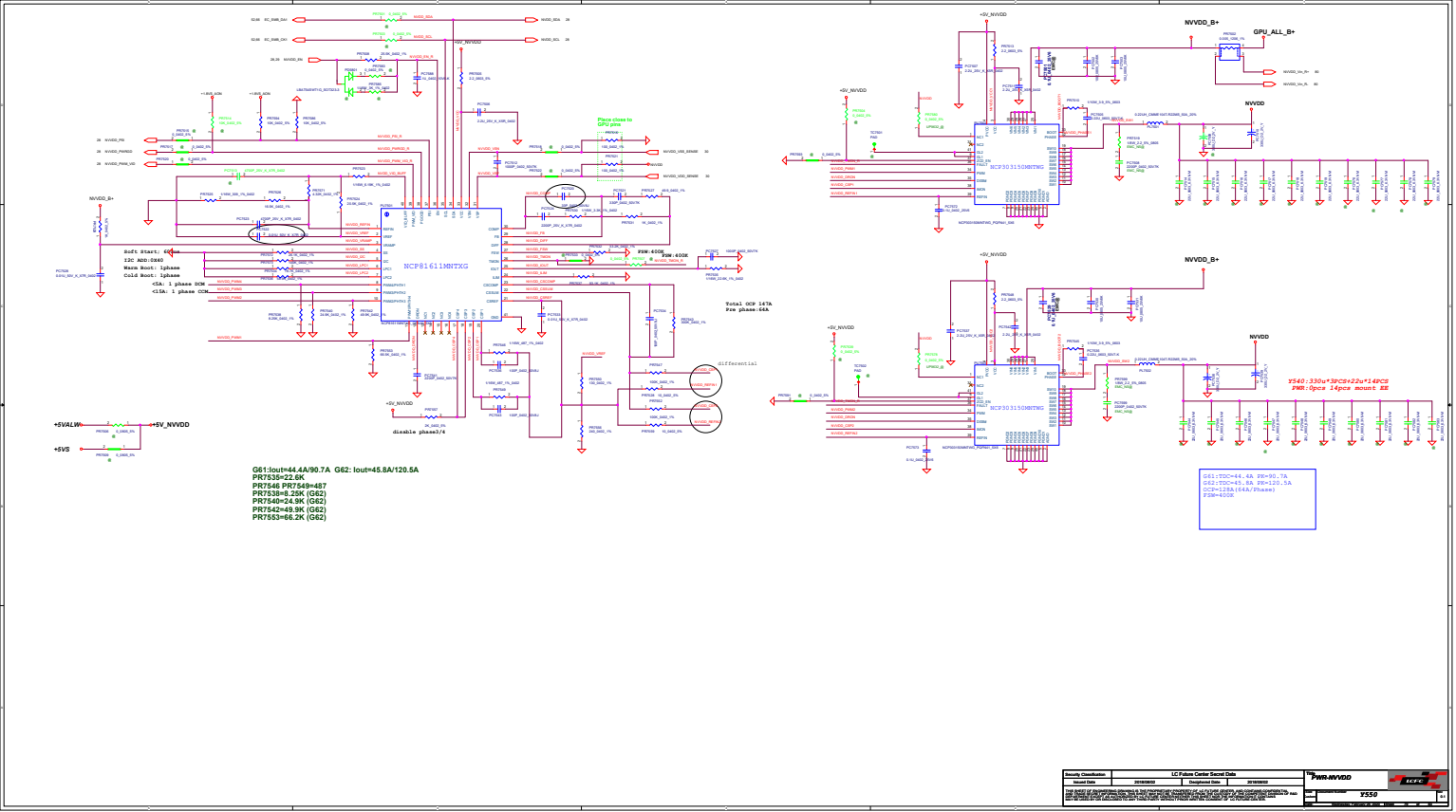
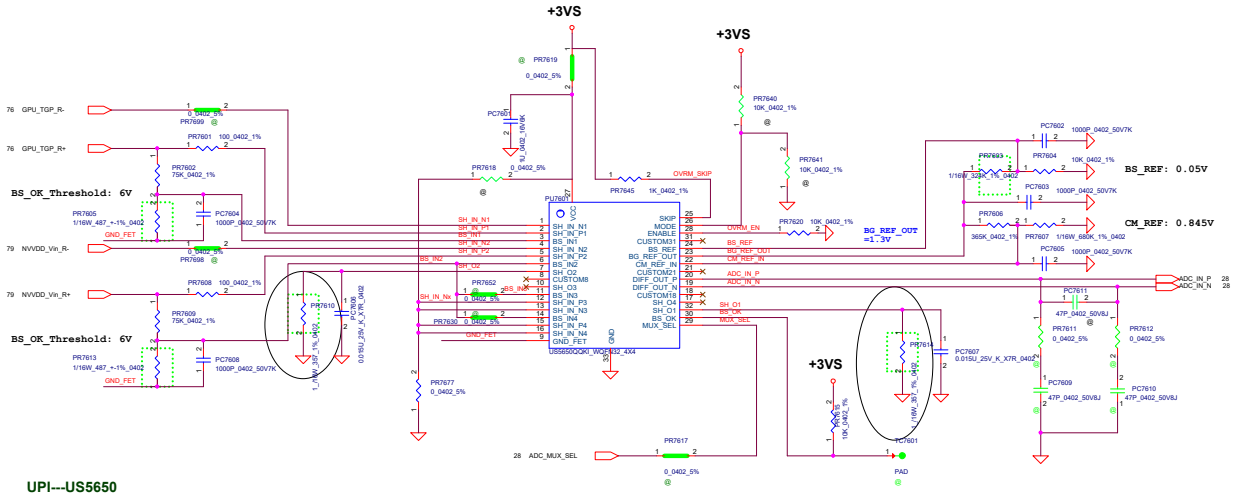

NCP81611MNTXG
NCP303150MNTWG
Soft Start: 60us
I2C ADD:0240
Warm Boot: 1phase
Cold Boot: 1phase
<5A: 1 phase DCM
<15A: 1 phase CCM
FSW:600K
FSW:400K
Total OCP 147A
Pre phase:6&4
differential
disable phase3/4
Place close to GPU pins
NVVDD_B+
GPU_ALL_B+
+5V_NVVDD
+5VALW
+5V_NVVDD
+5VS
G61:Iout=44.4A/90.7A G62: Iout=45.8A/120.5A
PR7535=22.6K
PR7546 PR7549=4B7
PR7538=8.25K (G62)
PR7540=24.9K (G62)
PR7542=49.9K (G62)
PR7553=66.2K (G62)
G61:TOC=44.4A PK=90.7A
G62:TOC=45.8A PK=120.5A
OCP=128A(64A/Phase)
FSW=400K
Y540:330u*3PCS+22u*14PCS
PWR:0pcs 14pcs mount XE
PWR-NVVDD
Y550



UPI---US5650
PR7605=487
PR7613=487
PR7610=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR7614=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
PR7603=324K
PR7602=75K
PR7609=75K
PC7604=1nF
PC7608=1nF

ON---NCP45491
PR7605=649
PR7613=649
PR7610=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR7614=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
PR7603=243K
PR7602=75K
PR7609=75K
PC7604=1nF
PC7608=1nF

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Title: *Virtual symbol*

Size	Document Number	Rev
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Security Classification	LC Future Center Secret Data		
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Title
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Size	Document Number	Rev
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Security Classification	LC Future Center Secret Data		
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Title: *Blank*

Size	Document Number	Rev
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