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PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	BC1I#	Native	BC_I3#		PU 10K	+3VSUS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_48CPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_CHSEC_X1			
GPP_A11	PME#	Native	PCI_PME#			
GPP_A12	GPI	GPI	PCH_GPP_A12			
GPP_A13	SUSWARN#	Native	ME_BusPwrDnAck		PD 10K(E)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPI	GPP_A16 (TP)			
GPP_A17	GPI	GPI	(N.C)			
GPP_A18	GPO	GPI	PCH_GPP_A18			
GPP_A19	GPO	GPI	PCH_GPP_A19			
GPP_A20	GPI	GPI	(N.C)			
GPP_A21	GPI	GPI	(N.C)			
GPP_A22	GPI	GPI	(N.C)			
GPP_A23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	PCH_GPP_B0			
GPP_B1	GPO	GPO	PD_I2C_INT_PCH		PU 10K	+3VSUS
GPP_B2	GPI	GPI	PCH_GPP_B2			
GPP_B3	GPI	GPI	(N.C)			
GPP_B4	GPI	GPI	(N.C)			
GPP_B5	GPI	Native	CLK_FREQ_REQ0# _X1		PU 10K	+3VSUS
GPP_B6	GPO	GPO	(N.C)			
GPP_B7	GPI	Native	CLK_REQ1#/CLKREQ1_WLAN#		PU 10K	+3VSUS
GPP_B8	GPO	GPO	(N.C)			
GPP_B9	GPO	GPO	(N.C)			
GPP_B10	GPO	GPO	(N.C)			
GPP_B11	GPO	GPO	(N.C)			
GPP_B12	SLP_S0#	Native	SLP_S0# (TP)			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPP0914	PD	Pull-dn (40K/dn)	
GPP_B15	GPO	GPO	(N.C)			
GPP_B16	GPO	GPO	(N.C)			
GPP_B17	GPO	GPO	(N.C)			
GPP_B18	GPO	Strap	PCH_GPP918	PD	Pull-dn (40K/dn)	
GPP_B19	GPI	GPO	PCH_GPP419/WT_GN_PCH		PD 10K(E)	+3V_DUAL
GPP_B20	GPI	GPO	PCH_GPP820/NV_GPO_EVENT#		PU 10K	+3VSUS
GPP_B21	GPI	GPI	PCH_GPP821/NV_GC6_FB_EN		PU 10K(E)	+3VS
GPP_B22	GPO	Strap	PCH_GPP822	PD	Pull-dn (40K/dn)	
GPP_B23	GPO	GPO	SMOLARITY#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	Strap	PCH_GPPC2		PU 4.7K(E)	+3V_DUAL
GPP_C3	SMLOCLK	Native	SMLO_CLK		PU 2.2K	+3VSUS
GPP_C4	SMLODATA	Native	SMLO_DAT		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPP25	PD	Pull-dn (40K/dn)	
GPP_C6	GPI	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	GPI	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPO	GPO	(N.C)			
GPP_C9	GPO	GPO	(N.C)			
GPP_C10	GPO	GPO	(N.C)			
GPP_C11	GPI	GPI	WLAN_ON#		PD 10K	
GPP_C12	GPI	GPI	DIMM_SELO		PD 10K	
GPP_C13	GPI	GPI	DIMM_SEL1		PD 10K	
GPP_C14	GPI	GPI	DIMM_SEL2		PD 10K	
GPP_C15	GPI	GPI	NPC_ID		PD 10K	+3VSUS
GPP_C16	GPO	GPO	PD_I2C_SDA_PCH		PU 2.2K	+3VSUS
GPP_C17	GPI	GPO	PD_I2C_SCL_PCH		PU 2.2K	+3VSUS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PU 10K	+3VS
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPO	GPO	(N.C)			
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPO	GPO	(N.C)			
GPP_D1	GPO	GPO	(N.C)			
GPP_D2	GPO	GPO	(N.C)			
GPP_D3	GPO	GPO	(N.C)			
GPP_D4	GPO	GPO	(N.C)			
GPP_D5	GPI	GPI	PCH_GPP05 / M.2_WT_PCHRST#		PD 75K	
GPP_D6	GPI	GPI	PCH_GPP06 / M.2_WT_PCMCLK		PD 71.5K	
GPP_D7	GPI	GPO	PCH_GPP07 / M.2_WT_PCMEN			
GPP_D8	GPI	GPI	PCH_GPP08 / M.2_WT_PCMCLK			
GPP_D9	GPO	GPO	(N.C)			
GPP_D10	GPO	GPO	(N.C)			
GPP_D11	GPO	GPO	(N.C)			
GPP_D12	GPO	GPO	(N.C)			
GPP_D13	GPO	GPO	(N.C)			
GPP_D14	GPO	GPO	(N.C)			
GPP_D15	GPO	GPO	(N.C)			
GPP_D16	GPO	GPO	(N.C)			
GPP_D17	GPO	GPO	(N.C)			
GPP_D18	GPO	GPO	(N.C)			
GPP_D19	GPO	GPO	(N.C)			
GPP_D20	GPO	GPO	(N.C)			
GPP_D21	GPO	GPO	(N.C)			
GPP_D22	GPO	GPO	(N.C)			
GPP_D23	GPO	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPO	GPO	(N.C)			
GPP_E1	GPO	GPO	(N.C)			
GPP_E2	GPO	GPO	(N.C)			
GPP_E3	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_E4	GPO	GPO	(N.C)			
GPP_E5	GPI	Native	MODPI1_DEVSLP			
GPP_E6	GPO	GPO	(N.C)			
GPP_E7	GPI	GPI	EXT_SCI#			
GPP_E8	GPO	GPO	(N.C)		PU 10K(E)	+3VS
GPP_E9	GPI	Native	USB_OC#0	PU	PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1	PU	PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2	PU	PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3	PU	PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPO	GPO	(N.C)			
GPP_F1	GPI	Native2	SATAPCIE_SET4		PU 10K	+3VS
GPP_F2	GPO	GPO	(N.C)			
GPP_F3	GPO	GPO	(N.C)			
GPP_F4	GPO	GPO	(N.C)			
GPP_F5	GPO	GPO	(N.C)			
GPP_F6	GPO	GPO	(N.C)			
GPP_F7	GPO	GPO	(N.C)			
GPP_F8	GPO	GPO	(N.C)			
GPP_F9	GPO	GPO	(N.C)			
GPP_F10	GPO	GPO	(N.C)			
GPP_F11	GPO	GPO	(N.C)			
GPP_F12	GPO	GPO	(N.C)			
GPP_F13	GPO	GPO	(N.C)			
GPP_F14	GPO	GPO	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	Native	I_VDDEN_PCH		PD 100K	
GPP_F20	GPI	Native	LCD_BACKEN_PCH			
GPP_F21	GPI	Native	I_RESCUTL_PCH		PD 1M	
GPP_F22	GPO	GPO	(N.C)			
GPP_F23	GPO	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPI	(N.C)			
GPP_G1	GPI	GPO	SATA_ODD_PWRGT			
GPP_G2	GPI	GPI	SATA_ODD_DA#			
GPP_G3	GPI	GPI	(N.C)			
GPP_G4	GPI	GPI	(N.C)			
GPP_G5	GPI	GPI	(N.C)			
GPP_G6	GPI	GPI	(N.C)			
GPP_G7	GPI	GPI	(N.C)			
GPP_G8	FAN_PWM_0	Native	(N.C)			
GPP_G9	FAN_PWM_1	Native	(N.C)			
GPP_G10	FAN_PWM_2	Native	(N.C)			
GPP_G11	FAN_PWM_3	Native	(N.C)			
GPP_G12	GPI	GPI	(N.C)			
GPP_G13	GPI	GPI	(N.C)			
GPP_G14	GPI	GPI	(N.C)			
GPP_G15	GPI	GPI	(N.C)			
GPP_G16	GPI	GPI	(N.C)			
GPP_G17	GPI	GPI	(N.C)			
GPP_G18	GPI	GPI	PCH_GPP_G18			
GPP_G19	GPI	GPI	PCH_GPP_G19			
GPP_G20	GPI	GPI	(N.C)			
GPP_G21	GPI	GPI	(N.C)			
GPP_G22	GPI	GPI	(N.C)			
GPP_G23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLKREQ0_MODPI1#_X1		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLKREQ7_USB31#_X1		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K	+3VSUS
GPP_H4	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H5	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H6	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H7	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H8	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H9	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H10	GPI	GPI	(N.C)			
GPP_H11	GPI	GPI	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD		
GPP_H13	GPI	GPI	(N.C)			
GPP_H14	GPI	GPI	(N.C)			
GPP_H15	GPI	GPI	(N.C)			
GPP_H16	GPI	GPI	(N.C)			
GPP_H17	GPI	GPI	(N.C)			
GPP_H18	GPI	GPI	(N.C)			
GPP_H19	GPI	GPI	(N.C)			
GPP_H20	GPI	GPI	(N.C)			
GPP_H21	GPI	GPI	(N.C)			
GPP_H22	GPI	GPI	(N.C)			
GPP_H23	GPI	GPO	WLAN_WAKE_CTRL_CS#			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	Native	(N.C)		PD 150K	
GPP_I1	GPI	Native	(N.C)		PD 150K	
GPP_I2	GPI	Native	(N.C)			
GPP_I3	GPI	Native	(N.C)			
GPP_I4	GPI	Native	CLK_FREQ_14		PU 100K	
GPP_I5	GPI	Native	(N.C)		PU 2.2K	+3VS
GPP_I6	GPO	Native	(N.C)	PD	PU 2.2K	+3VS
GPP_I7	GPI	Native	(N.C)		PU 2.2K	+3VS
GPP_I8	GPO	Native	(N.C)	PD	PU 2.2K	+3VS
GPP_I9	GPI	Native	(N.C)		PD 2.2K(E)	+3VS
GPP_I10	GPO	Native	(N.C)	PD	PU 2.2K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 8.2K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#/PM_PWRBTN#		PU 10K(E)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#/PM_SUS3#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#/PM_SUS5#		PD 100K	
GPD6	SLP_A#	Native	SLP_A#			
GPD7	RSTD	GPO	(N.C)			
GPD8	SUSCLK	Native	SUS_CLK#/SUS_CLK			
GPD9	SLP_WLAN#	Native	SLP_WLAN#		PU 10K(E)	+3VA_DSW
GPD10	SLP_S5#	Native	SLP_S5#			
GPD11	LANPHYPC	Native	LAN_PHYPC#		PU 10K	+3VA_DSW

EC IT8995 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#	PU 10K (E)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (E)	+3VA_EC
GPA3	Alt	PWM	FAN1_PWM		
GPA4	O	GPO	EC_GPA4		
GPA5	Alt	PWM	FAN2_PWM		
GPA6	Alt	PWM	PM_LED_PWM		
GPA7	O	GPO	G2_LED#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_DC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PD_DE_EC		
GPB5	O	GPO	HDMI_WAIT	PD 10K	
GPB6	OD	GPO	BC_I3#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	PM_EXTTS#0	PU 10K (E)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K (E)	+3VSUS
GPC4	I	GPI	EC_SATA/ISPI#4	PU 10K	+3VSUS
GPC5	I	GPI	PM_SUSC#	PU 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PU 100K	
GPC7	O	GPO	EC_SPI7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_SUS#		
GPD1	O	GPO	EC_SMI1/WE_AC_PRESENT	PU 100K	+3VA_DSW
GPD2	Alt	GPI	BUF_PLT_RST#	PU 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/G9_SI#		
GPD6	Alt	GPI	FAN2_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN1_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PU 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PU 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	P_SUSB2SB# _VCC		
GPE4	O	GPO	USB_EC1_2_OFF#		
GPE5	I	GPI	PM_SUSB#	PU 100K	
GPE6	Alt	GPI	CAP_LED#		
GPE7	OD	GPO	TYPEC_CTS#	PU 10K (E)	+3VA_EC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0 CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0 DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2/PHRLIMIT_EC#	PU 100K	+3VA_EC
GPG3	GPI		EC_SCK#/EC_SCK#_PCH		
GPG4	GPI		EC_SI/EC_SI_PCH		
GPG5	GPI		EC_SO/EC_SO_PCH		
GPG6	O	GPO	USB30_5VEC#		
GPG7	GPI		EC_SCK_PCH	PU 10K (E)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3 CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3 DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_SUSWDT#	PU 10K (E)	
GPH4	O	GPO	DPMROK_EC	PU 10K	
GPH5	O	GPO	PM_PWROK	PU 10K	
GPH6	O	GPO	PM_SYSPWROK	PU 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_S10#		
GPI1	I	GPI	SYSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3V
GPI3	I	GPI	IMVP9_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	PD 100K	+3VACC
GPI7	Alt	AD	WA_MAX_POWER	PD 100K & PU 93.1K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0/USB31_5VEC1#	PU 10K	+3VSUS
GPJ1	O	GPO	3VAOSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	P1_EEP_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_SUS_STAT#		
GPJ4	Alt	DA	I2AT_REP_EC		
GPJ5	O	GPO	EC_GPJ5		
GPJ6	I	GPI	PD_WAKE#	PU 100K	+3VA_DSW
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EC0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EC01		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EC02		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EC03		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/EC0K		CLK_EC0CK1_PCH		
GPM5	LFRAME#/EC0#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

GX502/GU502 Source:

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	**SM-Bus Address**
on board memory CHA	
SO-DIMM B(0)	A4h
ESS_ES9118EQ	90h

EC Master (SMB0)	
SM-Bus Device	**SM-Bus Address**
SN2560_RX(PX)(CHARGER)	12h
BATTERY(GAUGE)	16h
AFL6012(PROTECTION)	78h

EC Master (SMB1)	
SM-Bus Device	**SM-Bus Address**
GPU INT. Thermal sensor	98h, 9Ch
PCH INT. Thermal sensor	94h
CPU Thermal Sensor	90h
GPU Thermal Sensor	98h
TB2(PIN key)	E2h

EC Master (SMB3)	
SM-Bus Device	**SM-Bus Address**
CYPD4126(PD)	08h
TAS5825(SMARTAMP)	94h, 96h

Device Identification

CPU Thermal Sensor		
1st	0x810 00120000	SCT7770-A
2nd		

GPU Thermal Sensor		
1st	0x9000040000	STSH-1PW
2nd		

HSIO	HM370	QM370	CM246	IRST	Devices Assign	GX502GX(型號)(0928)
0	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1		Type-C USB3.1 Type-C	(Port1)USB3.1 Gen2 TypeA
1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2		Type-C USB3.1 Type-C	(Port2)USB3.1 Gen2 TypeA
2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3		Type-C USB3.1 Type-A USB3.1 Type-A	(Port3)USB3.1 Gen2 TypeA
3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4		Type-C USB3.1 Type-A USB3.1 Type-A	(Port4)USB3.1 Gen2 TypeC
4	USB3.1 Gen1 #5	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #5		Type-C USB3.1 Type-A USB3.1 Type-A	
5	USB3.1 Gen1 #6	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1/Gen2 #6		Type-C USB3.1 Type-A USB3.1 Type-A	Need only for QM370 / CM246
6	USB3.1 Gen1 #7	USB3.1 Gen1 #7	USB3.1 Gen1 #7	PCH #1	2.5 GBE(I 219LM)	Need only for QM370 / CM246
7	USB3.1 Gen1 #8	USB3.1 Gen1 #8	USB3.1 Gen1 #8	PCH #2		
8	NA	USB3.1 Gen1 #9	USB3.1 Gen1 #9	PCH #3		
9	NA	USB3.1 Gen1 #10	USB3.1 Gen1 #10	PCH #4		
10	NA	PCH #5	PCH #5			
11	NA	PCH #6	PCH #6		Thunderbolt (shared by 1)	
12	NA	PCH #7	PCH #7			
13	NA	PCH #8	PCH #8			
14	PCIE #1	PCH #9	PCH #9		1st M.2 SSD (PCIE*2, optional)	1st M.2 SSD (PCIE*2, optional)
15	PCIE #2	PCH #10	PCH #10			
16	PCIE #11	PCH #11	PCH #11		PCIE*4 / SATA*2 (optional)	PCIE*4 / SATA*2 (optional)
17	PCIE #12	PCH #12	PCH #12			
18	PCIE #13	PCH #13	PCH #13			
19	PCIE #14	PCH #14	PCH #14			
20	PCIE #15	PCH #15	PCH #15		LAN	GLAN
21	PCIE #16	PCH #16	PCH #16		WLAN	WLAN
22	PCIE #17	PCH #17	PCH #17		2nd M.2 SSD (PCIE*2, optional)	2nd M.2 SSD (PCIE*2, optional)
23	PCIE #18	PCH #18	PCH #18			
24	PCIE #19	PCH #19	PCH #19		PCIE*4 / SATA*1 (optional)	
25	PCIE #20	PCH #20	PCH #20			
26	PCIE #21	PCH #21	PCH #21			
27	PCIE #22	PCH #22	PCH #22		3rd M.2 SSD (PCIE*2, optional)	3rd M.2 SSD (PCIE*4)
28	PCIE #23	PCH #23	PCH #23			
29	PCIE #24	PCH #24	PCH #24			

PCH17-18 support PCIE only CM246

571182_CNL_PCH_H_EDS_Vol_1_Rev_0_7, page24

Table 1-7. PCH HSIO Detail (SKU 9-11of 11)

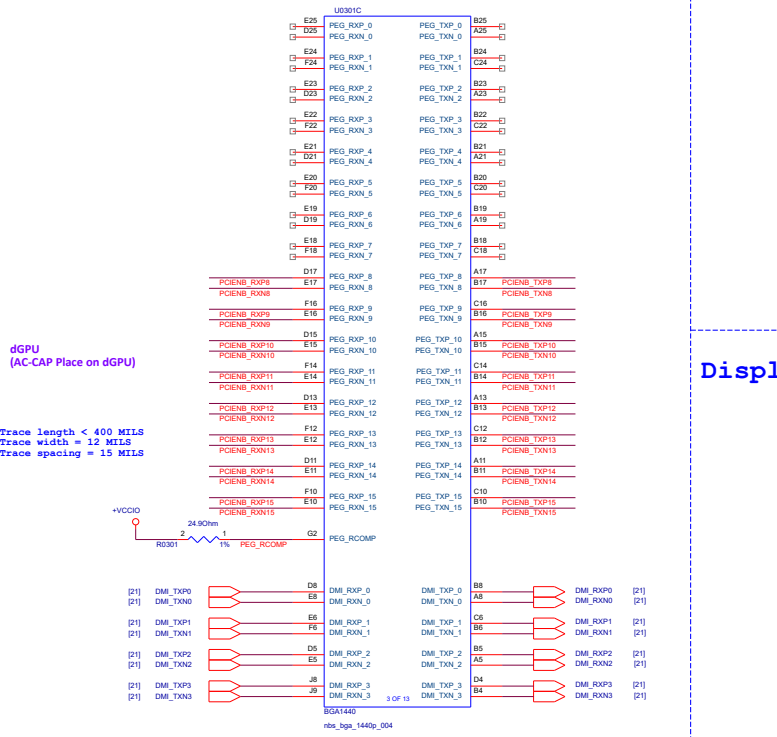
Flex I/O Lane	SKU		
	HM370	QM370	CM246
0	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
4	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
5	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
6	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
7	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
8	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
9	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
10	GbE	PCIe*, GbE	PCIe*, GbE
11	N/A	PCIe*	PCIe*
12	N/A	PCIe*	PCIe*
13	N/A	PCIe*	PCIe*
14	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
15	PCIe*	PCIe*	PCIe*
16	PCIe*, SATA 0A	PCIe*, SATA 0A	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B	PCIe*, SATA 1B	PCIe*, SATA 1B
20	PCIe*	PCIe*	PCIe*, SATA 2
21	PCIe*	PCIe*	PCIe*, SATA 3
22	PCIe*, SATA 4	PCIe*, SATA 4	PCIe*, SATA 4
23	PCIe*, SATA 5	PCIe*, SATA 5	PCIe*, SATA 5
24	PCIe*	PCIe*	PCIe*, SATA 6
25	PCIe*	PCIe*	PCIe*, SATA 7
26	PCIe*	PCIe*	PCIe*
27	PCIe*	PCIe*	PCIe*
28	PCIe*	PCIe*	PCIe*
29	PCIe*	PCIe*	PCIe*

571391_CFL_H_PDG_RevOp71, page 230

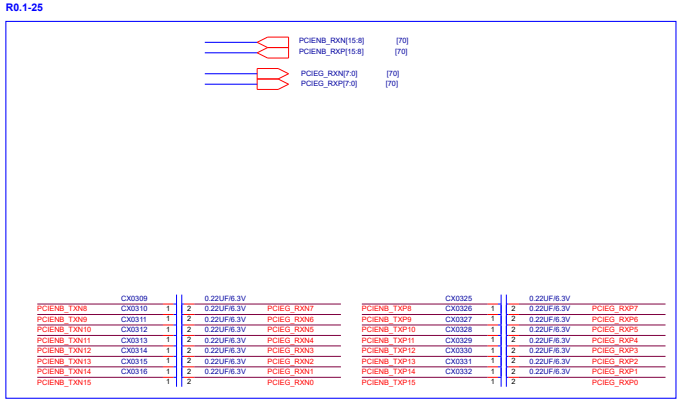
Figure 14-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

Title :	GX502GX	
Size:	Project Name:	Rev:
Date:	Dept:	Engineer:
Sheet	of	

PCIEG



R0.1-25



Display

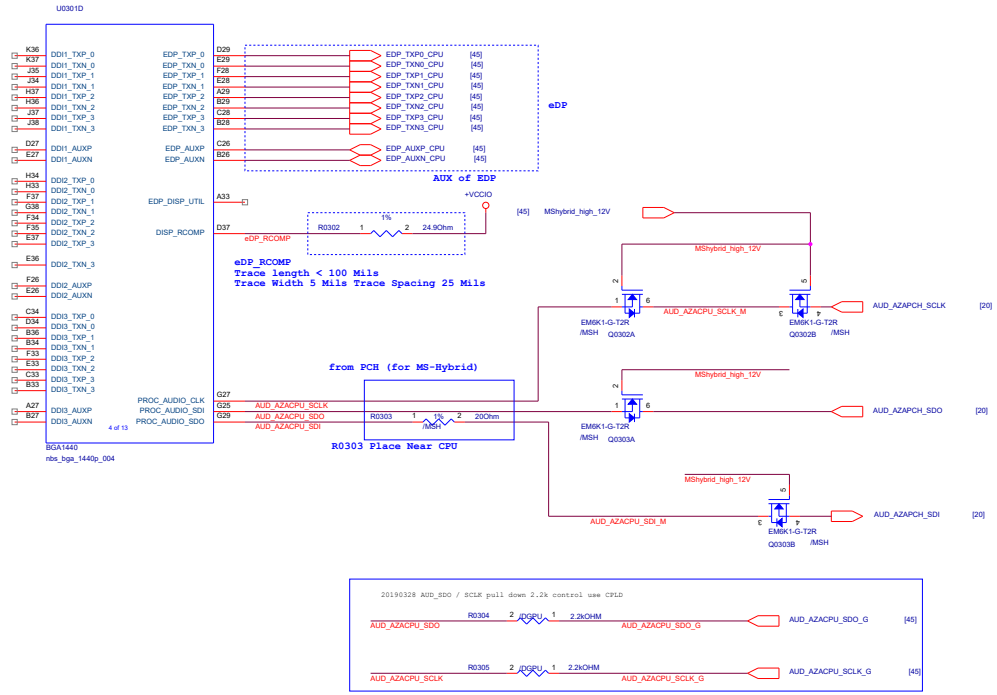


Table 81. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes: 1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.

2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   - Connect lane 0 of 1st device to lane 0.
   - Connect lane 0 of 2nd device to lane 8.
   - Connect lane 0 of 3rd device to lane 12.
   - For example:
     a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
     b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
     c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9,one lane device must use lane12.

Refer to CML-H PDG P.339 (Doc.611586)

Disabling and Termination Guidelines for the Intel High Definition Audio Interface and the Intel Display Audio Interface

When the Intel HD Audio interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI on the CPU need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO on the CPU can be left unconnected. The Intel Display Audio pins on the PCH may be left disconnected.

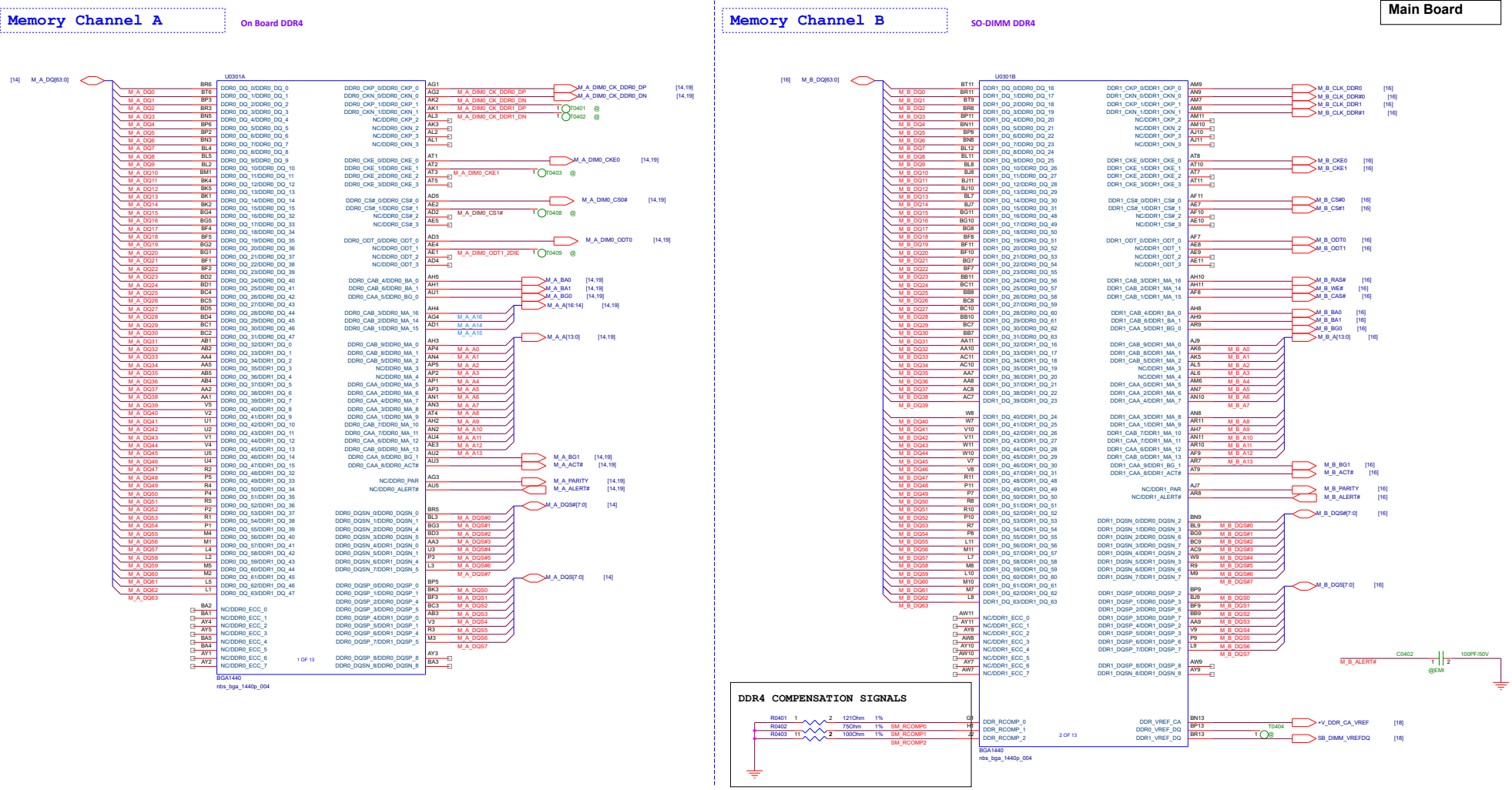
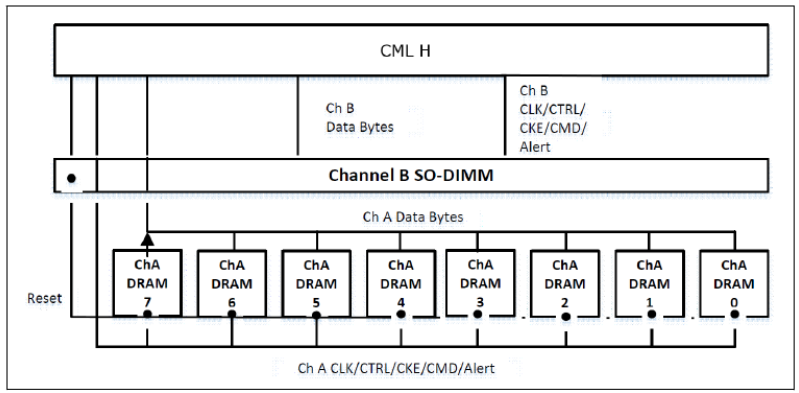
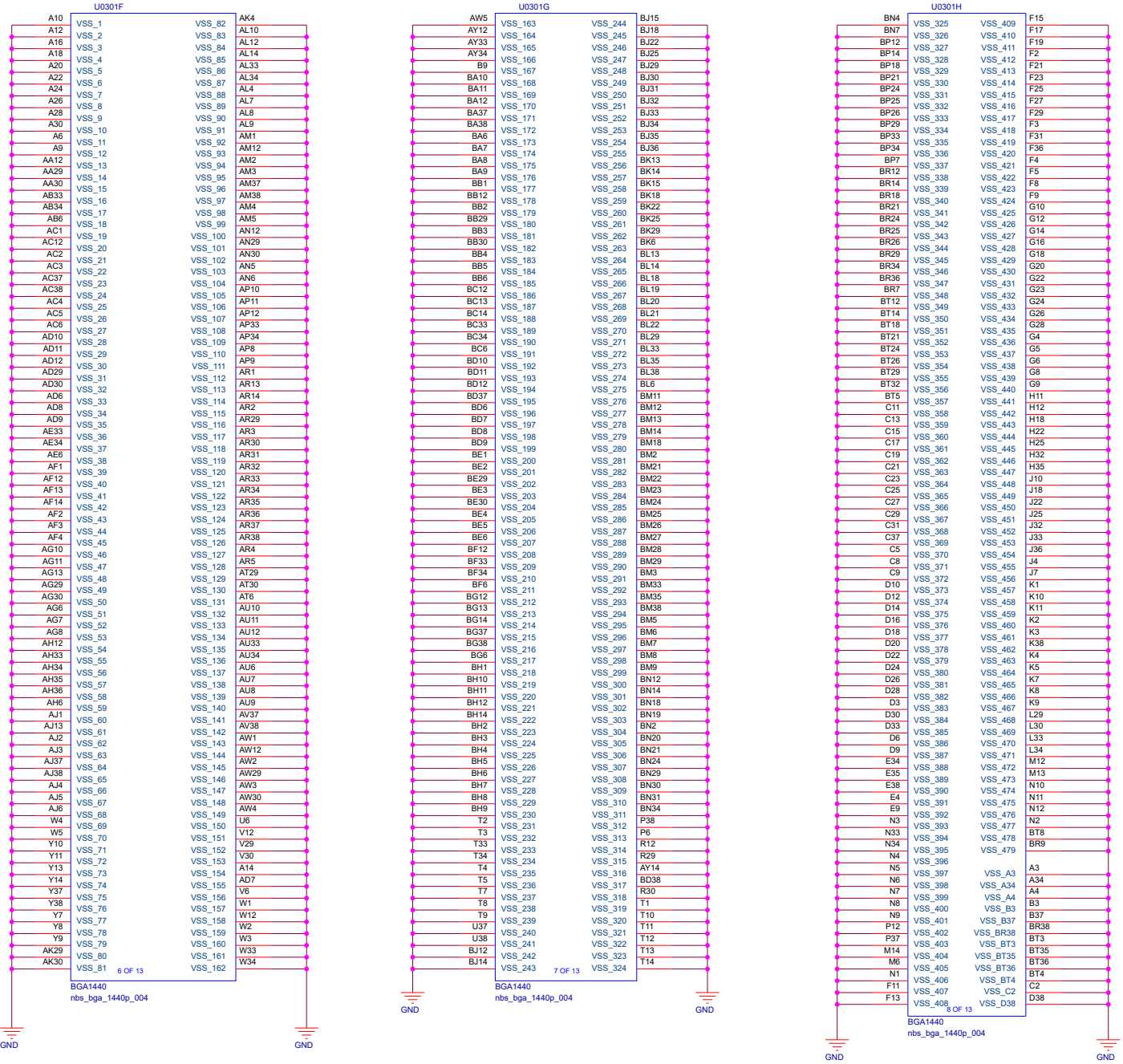


Figure 72. CML H DDR4 x8 Memory Down Placement and Block Diagram

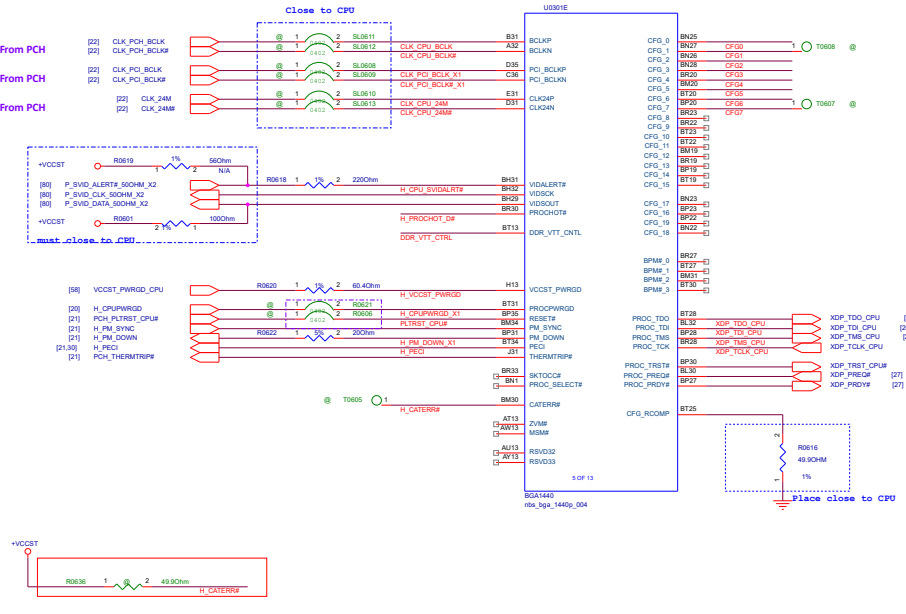


Project Name: GX502GX			Rev: R1.2
Title: CPU_DDR4			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, February 21, 2020	Sheet 4 of 99		



ASUS	Project Name: GX502GX	Rev: R1.2
Title :	CPU_CFG,RSVD,GND	
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, February 21, 2020	Sheet 5 of 99	

CFG



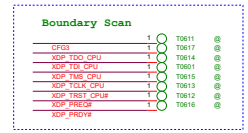
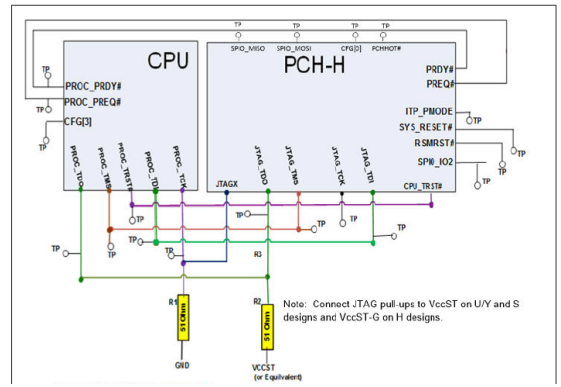
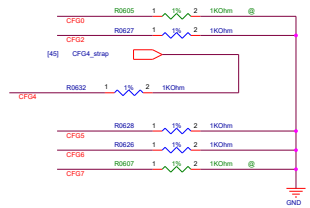


Figure 415. Connector Less Routing Topology



CFG Straps



CFG Straps for Processor

ref : Intel 570805_Coffeelake_EDS_Vol_1_Rev1.4 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Expres* Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

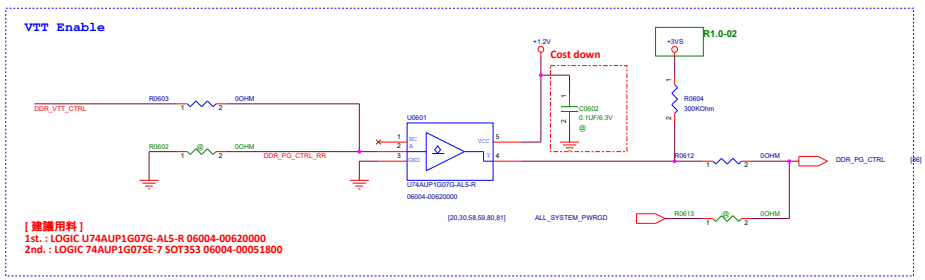
CFG[7] : PEG Training

- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

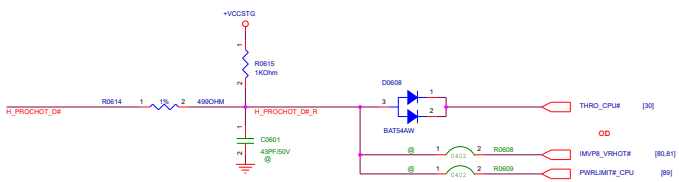
CFG[19:8] : Reserved Configuration Lanes

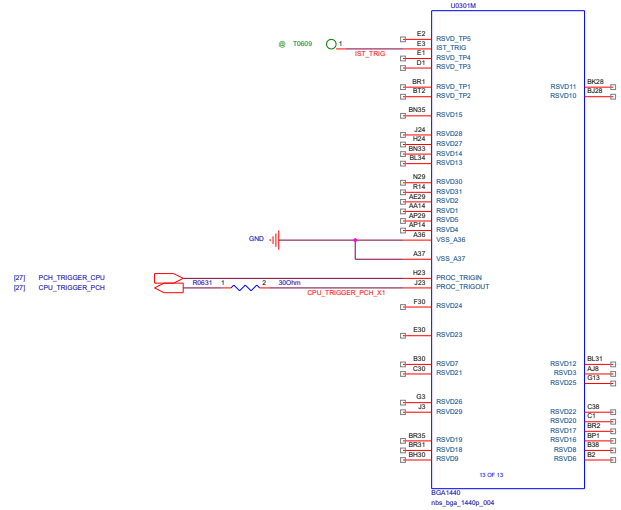
Reserved Configuration Lanes

DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref: Intel 570805_Coffeelake_EDS_Vol_1_Rev1.5 P.116

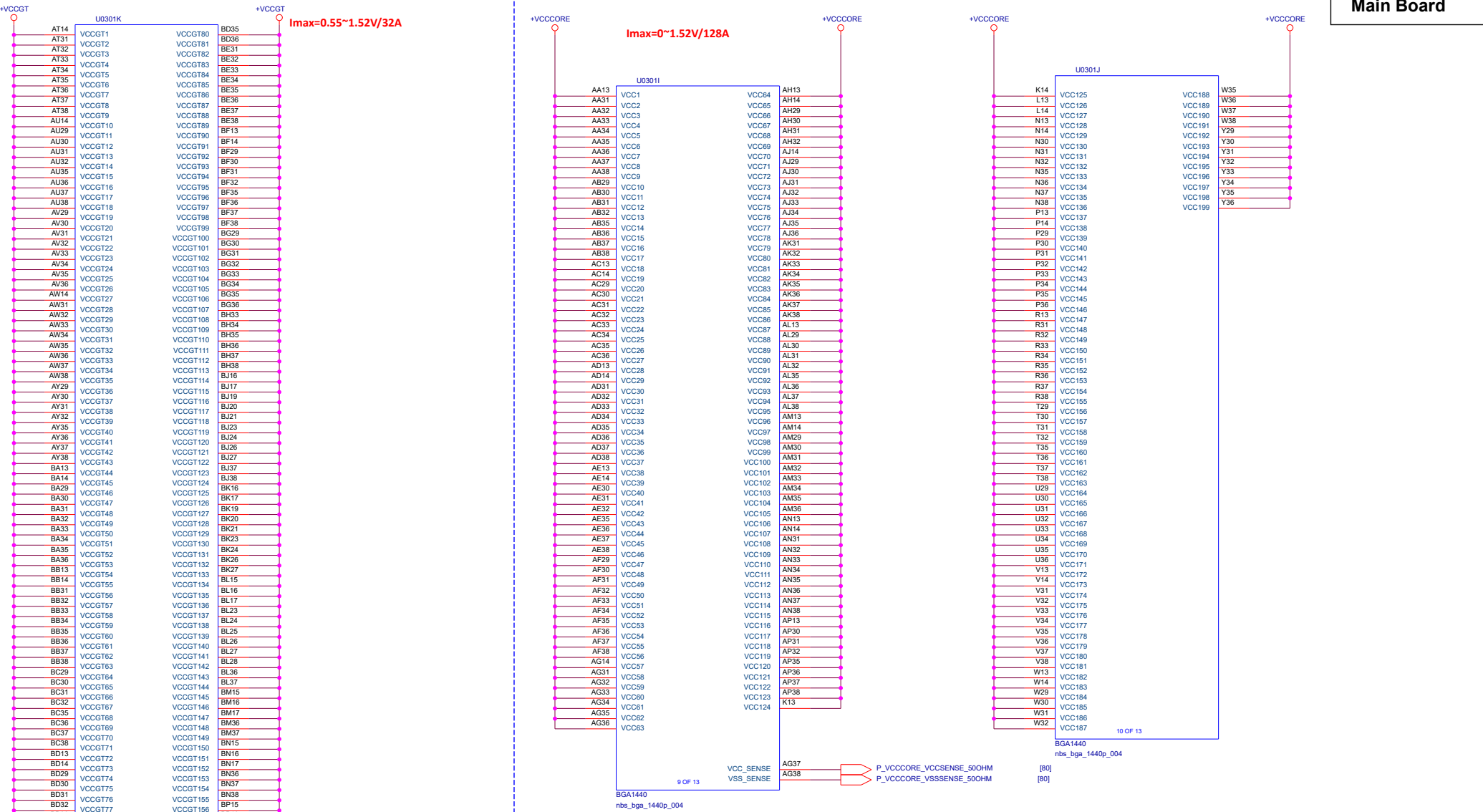


CPU SIDEBAND SIGNALS





ASUS	Project Name: GX502GX	Rev: R1.2
Title : CPU XDP		
Size: A	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, February 21, 2020	Sheet 7 of 99	



Project Name: GX502GX			Rev: R1.2
Title: CPU_PWR			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, February 21, 2020	Sheet 9 of 99		

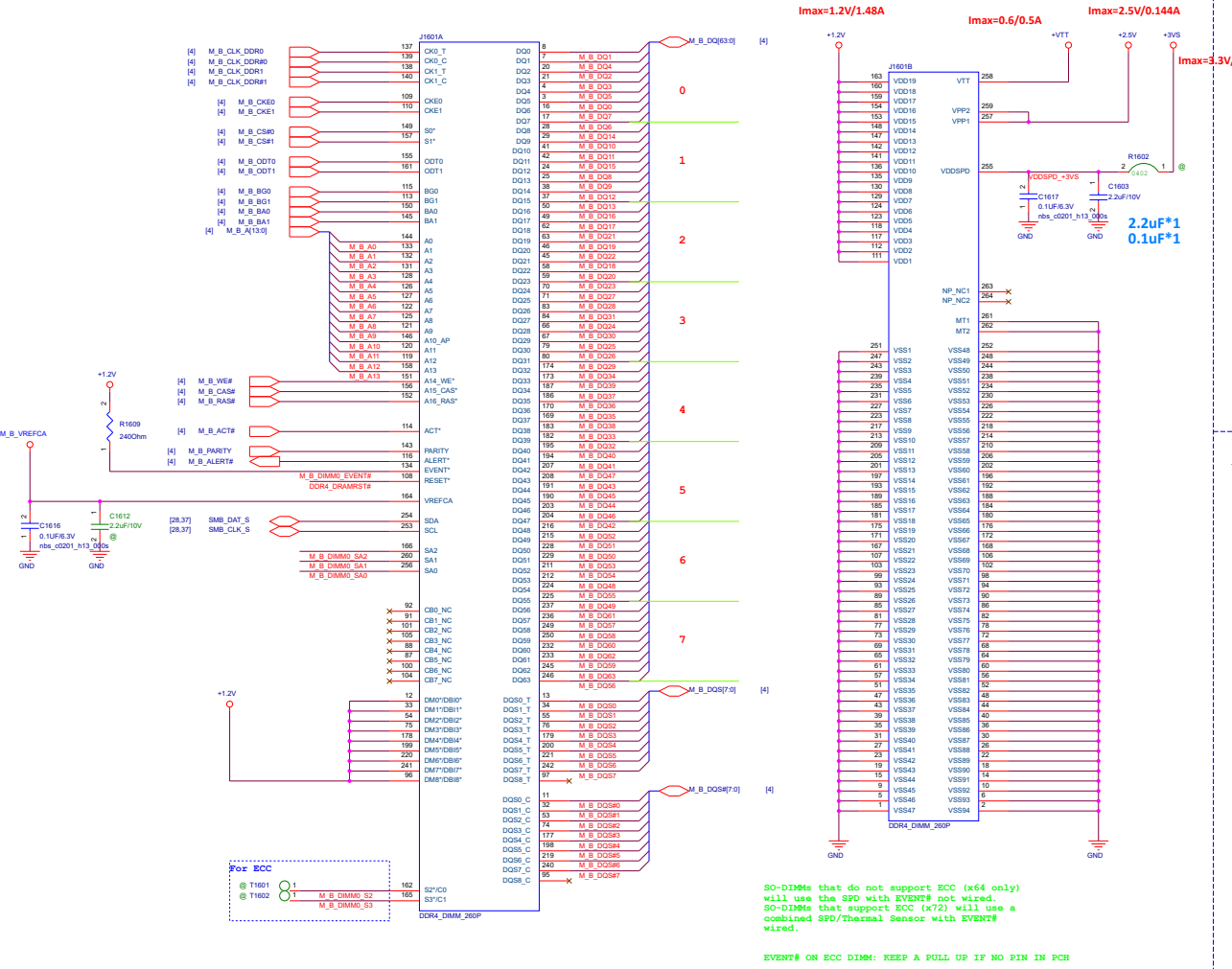
Title : DDR4_ON-BOARD_A2

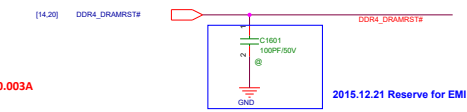
ASUSTeK COMPUTER

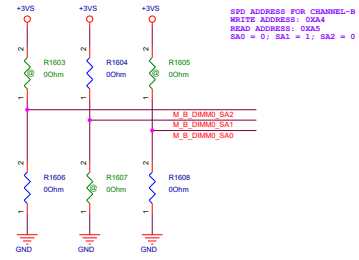
Engineer: EE

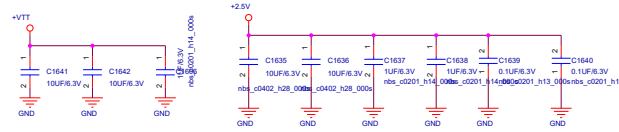
Size	Project Name	Rev
A	GX502GX	R1.2

SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)









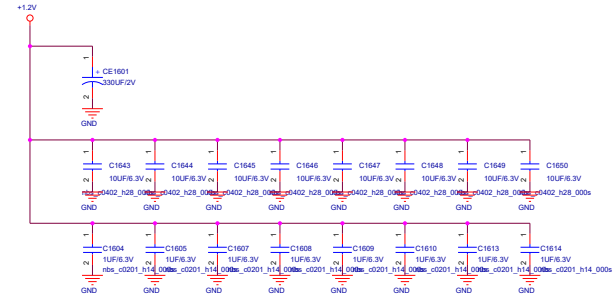


Table 4-24. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10µF (0603)	
		Placed on VTT plane close to DIMM	4x 1µF (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10µF (0603)	
		DIMM Pin side, 1 per DIMM	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0402)	

DDR4 - 2666MHz (8G)
1st : Hynix - 03A08-00051800
2nd : Samsung - 03A08-00051700
DDR4 - 2666MHz (16G)
1st : Hynix - 03A08-00061900
2nd : Samsung - 03A08-00061800

Project Name: GX502GX			Rev: R1.2
Title : DIM_DDR4 SO-DIMM B1			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Friday, February 21, 2020	Sheet 16 of 99		

<Core Design>

Title : NB_****

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	**GX502GX**	R1.2

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Figure 4-24. CFL-H DDR4 x8 Memory Down V_{REF-CA} Overview

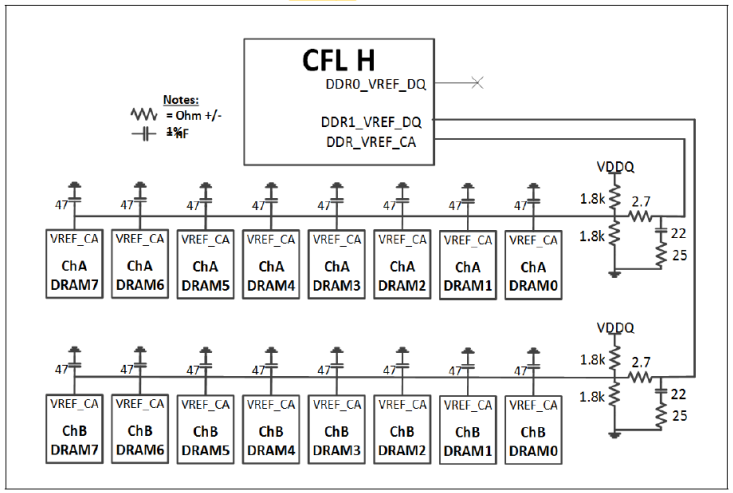
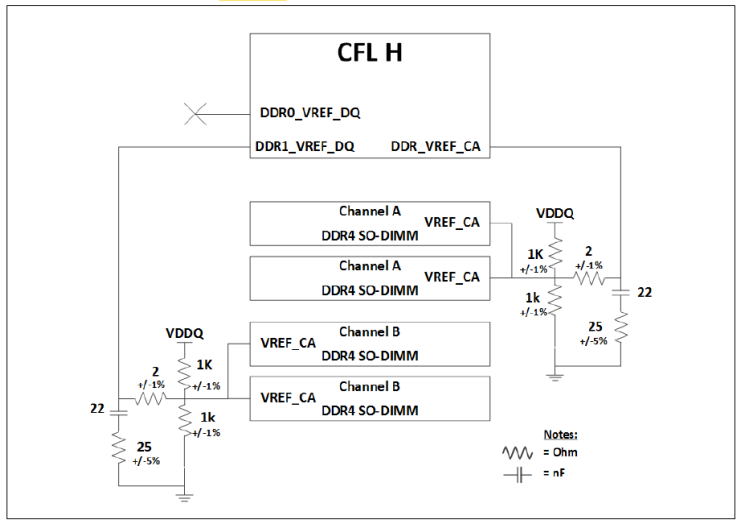
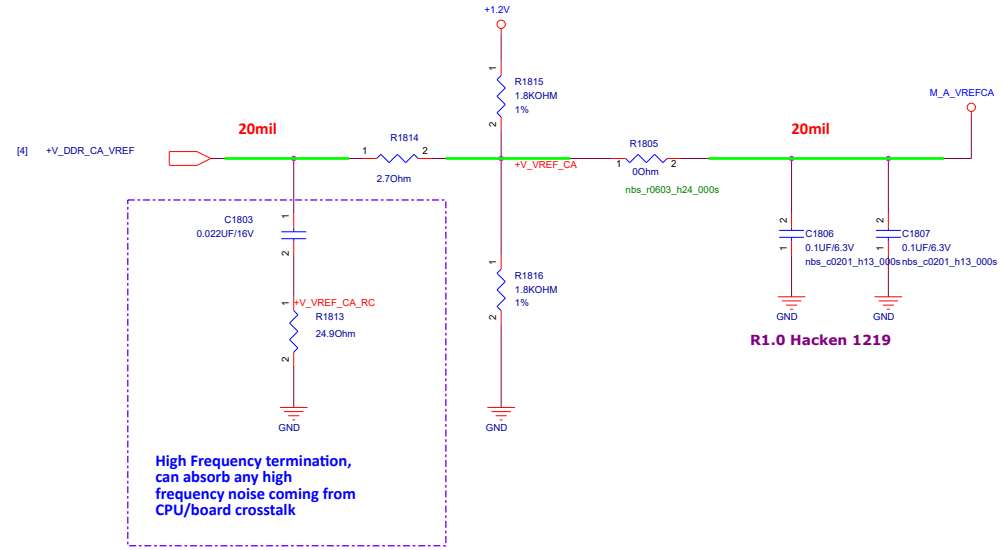


Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview

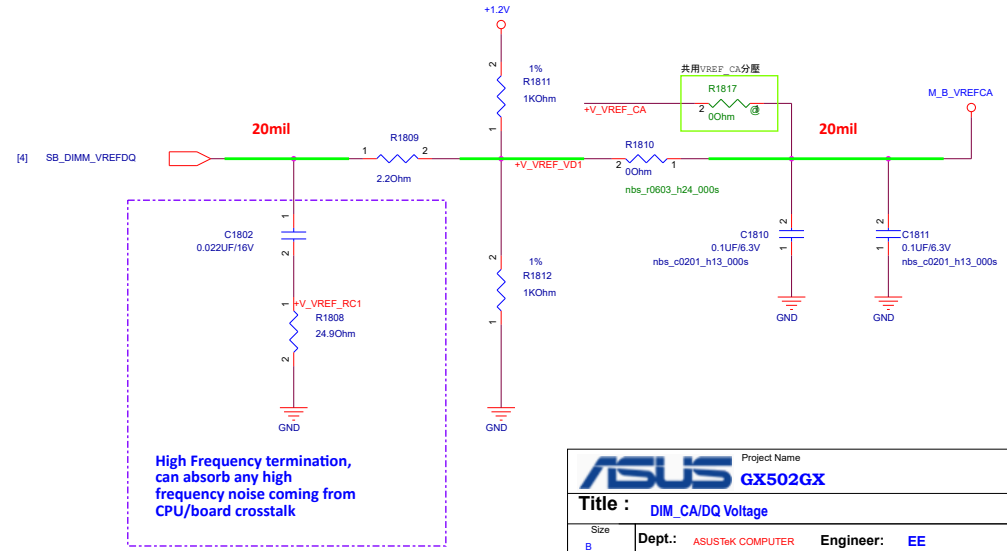


Memory Down Vref

Main Board



SO-DIMM1 Vref



Project Name: GX502GX		Rev: R1.2
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, February 21, 2020	Sheet 18 of 99	

HD Audio

RN2001 33ohm for HDA 3.3V
RN2001 33ohm for HDA 1.8V

ACZ_RST# AUD
ACZ_SYNC_AUD
ACZ_SDOUT_AUD
ACZ_BCLK_AUD
RN2001A
RN2001B
RN2001C
RN2001D
ACZ_RST# AUD_X1
ACZ_SYNC_AUD_X1
ACZ_SDOUT_AUD_X1
ACZ_BCLK_AUD_X1

ACZ_SDIN0_AUD
ACZ_SDOUT_AUD_X1
ACZ_SYNC_AUD_X1
ACZ_BCLK_AUD_X1
ACZ_RST#_AUD_X1

RF requirement

ACZ_SDOUT:

(1) PCH: Internal PD 20k ohm, VIL=0.35V, VIH>0.65*3.3V
(2) ALC295:VIL<0.4*3.3V, VIH>0.6*3.3V

+0.3A_V1.8A_VCCPAZBO
R2005 2.2KOhm
R2006 /CML 0Ohm
Q2001B EMBK1-G-T2R
R2005 1% 1KOhm
R2007 330Ohm
Q2001A EMBK1-G-T2R
@CFL
ACZ_SDOUT_AUD_X1
Q2001_D
PCH_SPI_OV

ACZ_SDOUT is a signal used for Flash Descriptor security Override/ME debug mode
HIGH : get overridden, LOW : disable override

Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.05VSUS	+VCCST		
	+1.2V			
	+3VAO	+3VA	+3VA_EC	
	+3VA_DSW	+3VSUS	+3VSUS_PCH	
		+3VS		

RTC battery

+3VA_RTC
CMOS Settings | JRST2001
Clear CMOS | Shunt
Keep CMOS | Open (Default)
R2027 20KOhm nbx_r0402_h16_000x
RTC_RST#
JRST2001 SGL_JUMP
C2002 1UF/6.3V
R2026 20KOhm nbx_r0402_h16_000x
SRTC_RST#
TPM Settings | JRST2002
Clear ME RTC Registers | Shunt
Keep ME RTC Registers | Open (Default)
JRST2002 SGL_JUMP
C2003 1UF/6.3V

+3VA
+RTCBAT
BAT2001 SIDE1 SIDE2 WTOB_CON_2P 12G17100002C
R2003 1K 1KOhm
+RTC_BAT
D2001 BAT54CTB
RTC_BAT
C2001 1UF/6.3V
C2004 0.1UF/25V

2nd : 12017-00020200

USE RTC Battery:
P/N: 0B100-00040500 BATT-LI CR1220 3V

Power failure solution (S0-->G3,S5-->G3):

U2001D
BD11 HDA_BCLK/I2S0_SCLK
BE11 HDA_SDI/I2S0_RXD
BF12 HDA_SDO/I2S0_TXD
BD13 HDA_SYNC/I2S0_SFRM
BE10 HDA_RST#/I2S1_SCLK
BF10 HDA_SDI/I2S1_RXD
BE12 I2S1_TXD/SNDW2_DATA
BD12 I2S1_SFRM/SNDW2_CLK
AM2 HDACPU_SDO
AN3 HDACPU_SDI
AM3 HDACPU_SCLK
AV18 GPP_D6/I2S2_SCLK
AW18 GPP_D7/I2S2_RXD
BA17 GPP_D8/I2S2_TXD/MODEM_CLKREQ
BE16 GPP_D9/I2S2_SFRM/CNV_RF_RESET#
BF16 GPP_D10/DMIC_DATA0/SNDW4_DATA
BD16 GPP_D11/DMIC_CLK0/SNDW4_CLK
AV16 GPP_D16/DMIC_DATA1/SNDW3_DATA
AW15 GPP_D17/DMIC_CLK1/SNDW3_CLK
BD47 RTCRST#
BD46 SRTCRST#
AV42 PCH_PWROK
BA47 RSMRST#
AW41 DSW_PWROK
BE25 GPP_C0/SMBALERT#
BE26 GPP_C1/SMBCLK
BF24 GPP_C2/SMBDATA
BF25 GPP_C3/SML0ALERT#
BE24 GPP_C4/SML0CLK
BD23 GPP_B23/SML1ALERT#/PCHHOT#
BF27 GPP_C6/SML1CLK
BE27 GPP_C7/SML1DATA
4 OF 13
COMETLAKE_H_PCH

ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A12/BM_BUSY#/
GPP_A13/SUSWARN#/SUSPWRDNACK
GPD3/LAN_WAKE#
GPD10/SLP_S5#
GPD11/LANPHYPC
GPD8/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B11/GSPI1_CS1#/TIME_SYNC1
GPP_B0/GSPI0_CS1#
GPP_A17/ADR_COMPLETE
GPP_B11/I2S_MCLK
SYS_PWROK
GPD0/SLP_A#
GPD1/SLP_LAN#
GPD2/SLP_S3#
GPD3/SLP_S4#
GPD9/SLP_S5#
GPD5/ISCLK
GPD6/BATLOW#
GPP_A15/SUSACK#
ME_SusPwrDnAck
GPD3/LAN_WAKE#
GPD10/PMCRESET
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
CPUPWRGD
ITP_PMODE
PCH_ITP_PMODE
PCH_JTAG#
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
PCH_JTAG_TRST#

PM_CLKRUN#
PCH_GPP_A12
PCH_GPP_B2
PCH_GPP_B0
PM_SYSPWROK_X1
PCIE_WAKE#
PCIE_WAKE#_X1
SLP_A#
SLP_LAN#
SLP_S3#
SLP_S4#
SLP_S5#
SUS_CLK
PM_BATLOW#
PCH_SUSACK#
ME_SusPwrDnAck
LAN_WAKE#
ME_AC_PRESENT_X1
PM_PWRBTN#
PM_SYSRST#_PCH
PCH_GPP14
H_CPUPWRGD
PCH_ITP_PMODE
PCH_JTAG#
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
PCH_JTAG_TRST#

T2004 T2005 T2006 T2008 T2001 T2010 T2011
R2039 R2042 R2043 R2040
R2009 82Ohm 1% 0402 Series
PCH_GPP_B2 [49]
PM_CLKRUN# [30]
eDP_HDMI_Switch [45]
PCIE_WAKE# [11,33,53,70]
PM_SUS#
PM_SUSC#
SLP_S5# [12]
SUS_CLK [40,41,53]
PCH_SUSACK# [30]
PM_SLP_SUS# [30]
PM_PWRBTN# [30]
H_CPUPWRGD [6]
XDP_TCLK_CPU [6]
XDP_TMS_CPU [6]
XDP_TDO_CPU [6]
XDP_TDI_CPU [6]
SL2006 SL2007 SL2005 SL2004 SL2003 SL2002 SL2001

from EC

ACZ_SDIN0_AUD [36]
Strap Pin
ACZ_BCLK_AUD_X1
ACZ_SDOUT_AUD_X1
ACZ_SYNC_AUD_X1
ACZ_RST#_AUD_X1
HDACPU_SDO
HDACPU_SDI
HDACPU_SCLK
R2070 R2071 30Ohm
AUD_AZAPCH_SDO [3]
AUD_AZAPCH_SDI [2]
AUD_AZAPCH_SCLK [3]
M.2_BT_PCMCLK [53]
M.2_BT_PCMIN [53]
M.2_BT_PCMOUT [53]
M.2_BT_PCMSRC_CLKREQ [53]
M.2_BT_PCMRIM_CRF_RST_N [53]
09/11 RF add
R2029 R2035 R2036 R2010 10KOhm
GPP_D6
GPP_D7
GPP_D8
GPP_D9
DMIC_DATA0_PCH [45]
DMIC_CLK0_PCH [45]

Change to 1K by TG 20180604

Boundary Scan
PCH_JTAG_TMS T2016
PCH_JTAG_TDO T2020
PCH_JTAG_TDI T2015
PCH_JTAG_TCK T2012
PCH_JTAG_TRST# T2018
PCH_ITP_PMODE T2014
PM_SYSRST#_PCH T2017
PM_RSMRST#_X1 T2013
SMLTALERT# T2019

+3VS
R2046 8.2KOhm
PM_CLKRUN#
+3VSUS
R2048 10KOhm
PM_SYSRST#_PCH
R2067 150KOHM
SML1ALERT#
+3VA_DSW
R2050 10KOhm
SLP_S5#
R2045 1KOhm
PCH_GPP_A12
R2030 10KOhm
CAN_WAKE#
R2031 10KOhm
eDP_HDMI_Switch
R2075 10KOhm
PM_RSMRST#_X1
R2028 10KOhm
PM_PWROK_X1
R2047 10KOhm
SLP_S5#
R2027 10KOhm

20190725 Sherwin follow CML-R PDG Modify
+VCCSTG
R2004 1K 1% 51Ohm
PCH_JTAG_TDO
R2012 1K 1% 51Ohm
PCH_JTAG#
PM_PWRBTN#
C2005 100PF/50V @EMI
PM_SUSACK#
C2007 100PF/50V @EMI
M.2_BT_PCMRIM_CRF_RST_N
R2013 75KOhm

for DDR

Strap Pin
GPP_A8_BT_UART_WAKE_N
SMB_CLK
SMB_SDA
PCH_GPPC5
SMLI_CLK
SMLI_DAT
SML1ALERT#
[28] SMB_CLK
[28] SMB_SDA
[28] SML1_CLK
[28] SML1_DAT

Strap => eSPI or LPC

+3VSUS
R2057 4.7KOhm
PCH_GPPC5
R2056 20KOhm
change R2057 to 4.7k/R2056 to 20k to 20180606

PCH_GPPC5: weak internal pull down	
PU	eSPI
PD	LPC (default)

Strap => Top Swap Override

+3VS
R2053 10KOhm
PCH_GPPB14
R2051 1KOhm

PCH_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)

20190725 Sherwin follow CML-R Reference Schematic Modify
+3VSUS
R2069 4.7KOhm
GPP_C2_BT_UART_WAKE_N

GPP_C2_BT_UART_WAKE_N(PCH_GPP_C2): weak internal pull down
0 : Disable Intel ME crypto Transport Layer Security(TLS) cipher suite (no confidentiality). (Default)
1 : Enable Intel ME Crypto Transport Layer Security(TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

SMBUS

+3VSUS
RN2002A SMB_SDA
RN2002B SMB_CLK
RN2002C
RN2002D
2.2KOhm
RN2003A SML0_DAT
RN2003B SML0_CLK
RN2003C SML1_DAT
RN2003D SML1_CLK

PM_PWROK,PM_RSMRST#: previous platform solution.
ME_PWROK,ME_AC_PRESENT: reserved for test.

+3VSUS +3VA_DSW
R2019 R2021 10KOhm
R2023 10KOhm
R2024 N/A
05'MeW04:
Optional if ME FW is Ignition FW

[30] PM_SYSPWROK
[6,30,58,59,60,61] ALL_SYSTEM_PWRGD
[30] PM_PWROK
[30] PM_RSMRST#
[30] ME_AC_PRESENT
R2020 10KOhm
R2052 0OHM
R2014 10KOhm
R2015 1KOhm
R2016 10KOhm
PM_SYSPWROK_X1
PM_PWROK_X1
PM_RSMRST#_X1
ME_AC_PRESENT_X1
1N4148WS
D2002
R2018 R2017 10KOhm
D2002: Prevent EC drive high. SUS_PWRGD sink low in S5-->G3.

[12,30,58] DPWROK_EC
R2023 10KOhm
To prevent EC burn out
R2022 10KOhm
DPWROK_R

+1.2V
PCH
DIMM
R2001 470Ohm 1%
R2002 0Ohm
DRAMRST#
DDR4_DRAMRST# [14,16]
C2006 0.1UF/6.3V
Changed by TG 20180321
R2001 tie to DRAMRST#
C2006 tie to DDR4_DRAMRST#

Power failure solution (S0-->G3,S5-->G3):

R1.0-34

PCH_GPPC2: weak internal pull down
[30,59,60] IMVP8_PWRGD
D2004 BAT54CTB
PM_SYSPWROK_X1
PM_PWROK_X1
[30,58,87] 3VA_DSW_PWRGD
D2005 BAT54CTB
PM_RSMRST#_X1
DPWROK_R

Power failure solution (S0-->G3,S5-->G3):

D2006
3VA_DSW_PWRGD
PM_SUSACK#
DATSHOLD_PRESENT_X1
R1.1-03
Change D2040 to 10Kohm if mount D2006
Deep SX discharge (S0-->DSX,S5-->DSX)

ASUS	Project Name: GX502GX		Rev: R1.2
Title : PCH-CPT(1)SATA,IHDA,RTC,JTAG			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, February 21, 2020	Sheet: 20 of 99		

Main Board

PCIE Setting

GX502GX PCIE/SATA Function define

CNL HM370 (PCIE#1-PCIE#8 not support)

HSIO Capabilities	Function
PCIEG (From GPU)	
PCIE#01 - USB3.1#07	
PCIE#02 - USB3.1#08	
PCIE#03 - USB3.1#09	
PCIE#04 - USB3.1#10	
PCIE#05	
PCIE#06	
PCIE#07	
PCIE#08	
PCIE#09	**PCIE9_SSD_P3**
PCIE#10	**PCIE10_SSD_P2**
PCIE#11- SATA-0a	**PCIE11_SSD_P1**
PCIE#12- SATA-1a	**PCIE12_SSD_P0/SATA**
PCIE#13- SATA-0b	
PCIE#14- SATA-1b	
PCIE#15 / SATA#2	**GLAN**
PCIE#16 / SATA#3	**WLAN**
PCIE#17 / SATA#4	**Thunderbolt_P0**
PCIE#18 / SATA#5	**Thunderbolt_P1**
PCIE#19 / SATA#6	**Thunderbolt_P2**
PCIE#20 / SATA#6	**Thunderbolt_P3**
PCIE#21	**PCIE21_SSD_P0**
PCIE#22	**PCIE22_SSD_P1**
PCIE#23	**PCIE23_SSD_P2**
PCIE#24	**PCIE24_SSD_P3**

	Function
CLKREQ-0	**GPU**
CLKREQ-1	
CLKREQ-2	**WLAN**
CLKREQ-3	
CLKREQ-4	**GLAN**
CLKREQ-5	**Thunderbolt**
CLKREQ-6	**SSD1**
CLKREQ-7	
CLKREQ-8	**SSD2**
CLKREQ-9	
CLKREQ-10~15	

USB Setting

GX502GX USB Function define

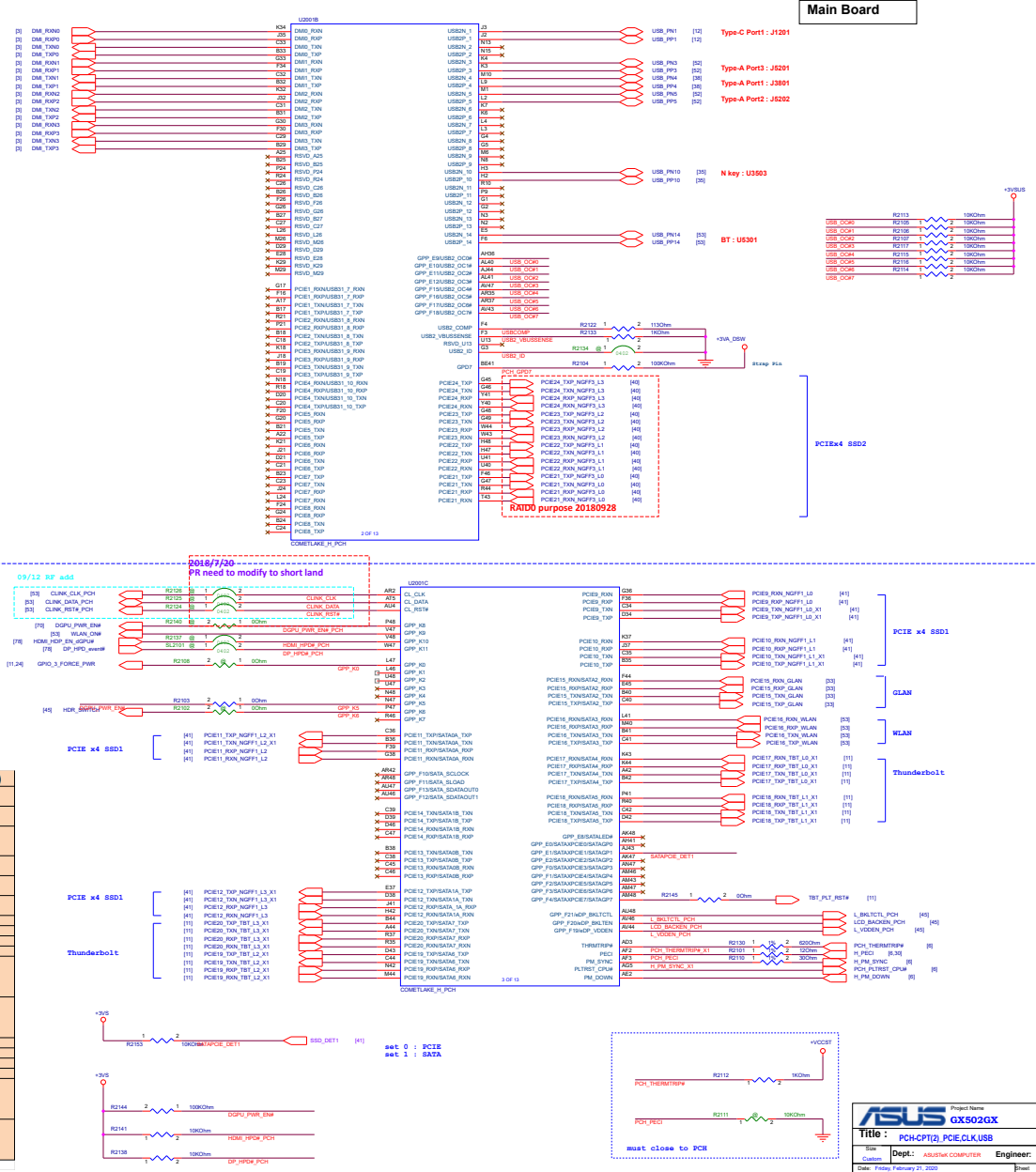
CNL HM370 (only #1-#4 support GEN2)

USB 2.0	Function
USB2_01	**(Port1)Thunderbolt**
USB2_02	
USB2_03	**(Port3)USB3.1 Gen1 TypeA**
USB2_04	**(Port1)USB3.1 Gen2 TypeA**
USB2_05	**(Port2)USB3.1 Gen1 TypeA**
USB2_06	
USB2_07	
USB2_05	
USB2_09	
USB2_10	**N key**
USB2_11	
USB2_12	
USB2_13	
USB2_14	**BT**

USB 3.1	Function
USB3.1#01	**(Port1)USB3.1 Gen2 TypeA**
USB3.1#02	**(Port2)USB3.1 Gen1 TypeA**
USB3.1#03	**(Port3)USB3.1 Gen1 TypeA**
USB3.1#04	
USB3.1#05	
USB3.1#06	
USB3.1#07	
USB3.1#08	

HSIO	HM370	QM370	CM246	IRST	Devices Assign		GX502GX組態(0928)
0	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1		(port1) USB3.1 Type C		(Port1)USB3.1 Gen2 TypeA
1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2		(port2) USB3.1 Type C		(Port2)USB3.1 Gen2 TypeA
2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3		(port1) USB3.0 Type A USB3.1 Type A		(Port3)USB3.1 Gen2 TypeA
3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4		(port2) USB3.0 Type A USB3.1 Type A		(Port1)USB3.1 Gen2 TypeC
4	USB3.1 Gen1 #5	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #5		(port3) USB3.0 Type A USB3.1 Type A	Gen2 only for QM370 / CM246	
5	USB3.1 Gen1 #6	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1/Gen2 #6		(port4) USB3.0 Type A USB3.1 Type A	Gen2 only for QM370 / CM246	
6	USB3.1 Gen1 #7	USB3.1 Gen1 #7	USB3.1 Gen1 #7 PCIE #1		CR (USB3.0 / PCIE)		
7	USB3.1 Gen1 #8	USB3.1 Gen1 #8	USB3.1 Gen1 #8 PCIE #2				
8	NA	USB3.1 Gen1 #9	USB3.1 Gen1 #9 PCIE #3	NO	x4 x2		
9	NA	USB3.1 Gen1 #10	USB3.1 Gen1 #10 PCIE #4	NO	x4 x2		
10	NA GbE	PCIE #5 GbE	PCIE #5 GbE	NO	x4 x2	Thunderbolt (priority 1)	
11	NA	PCIE #6	PCIE #6	NO	x4 x2		
12	NA	PCIE #7	PCIE #7	NO	x4 x2		
13	NA	PCIE #8	PCIE #8	NO	x4 x2		
14	PCIE #9 GbE	PCIE #9 GbE	PCIE #9 GbE	Yes	x4 x2	1st M.2 SSD (PCIE*2, optane)	1st M.2 SSD (PCIE*4 / SATA)
15	PCIE #10	PCIE #10	PCIE #10	Yes	x4 x2		
16	SATA #0a	PCIE #11 SATA #0a	PCIE #11 SATA #0a	Yes	x4 x2		
17	PCIE #12 SATA #1a GbE	PCIE #12 SATA #1a GbE	PCIE #12 SATA #1a GbE	Yes	x4 x2		
18	PCIE #13 SATA #0b GbE	PCIE #13 SATA #0b GbE	PCIE #13 SATA #0b GbE	NO	x4 x2	HDD (SATA#0b)	
19	PCIE #14 SATA #1b	PCIE #14 SATA #1b	PCIE #14 SATA #1b	NO	x4 x2	ODD (SATA#1b)	
20	PCIE #15	PCIE #15	PCIE #15 SATA #2			GLAN	GLAN
21	PCIE #16	PCIE #16	PCIE #16 SATA #3			WLAN	WLAN
22	PCIE #17 SATA #4	PCIE #17 SATA #4	PCIE #17 SATA #4	Yes	x4 x2	2nd M.2 SSD (PCIE*2, optane)	
23	PCIE #18 SATA #5	PCIE #18 SATA #5	PCIE #18 SATA #5	Yes	x4 x2		
24	PCIE #19	PCIE #19	PCIE #19 SATA #6	Yes	x4 x2		
25	PCIE #20	PCIE #20	PCIE #20 SATA #7	Yes	x4 x2	3rd M.2 SSD (PCIE*2, optane)	2nd M.2 SSD (PCIE*4)
26	PCIE #21	PCIE #21	PCIE #21	Yes	x4 x2		
27	PCIE #22	PCIE #22	PCIE #22	Yes	x4 x2		
28	PCIE #23	PCIE #23	PCIE #23	Yes	x4 x2		
29	PCIE #24	PCIE #24	PCIE #24	Yes	x4 x2		

PCIE17-20 support IRST only CM246



Project Name	GX502GX
Rev	R1.2
Title :	PCH-CPT(2)_PCIE,CLK,USB
Size	Custom
Dept.:	ASUSTeK COMPUTER
Engineer:	EE
Date:	Friday, February 21, 2020
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XTAL 24MHz

2017/12/25 Changed by James
(1) X2201 from 07009-0062000 to 07009-00065700
(2) R2212 from 1M to 200K

C2201 27PF/50V — XTAL24_IN_X1 — R2211 nbs_r020_h12_000s 0Ohm — XTAL24_IN
X2201 24MHZ 07009-00065700
R2212 200KOhm nbs_r0402_h16_000s
C2202 27PF/50V — XTAL24_OUT_X1 — R2209 nbs_r020_h12_000s 0Ohm — XTAL24_OUT
GND

RTC CRYSTAL 32.768KHz

C2203 15PF/50V — RTC_X1_X1 — R2213 nbs_r020_h12_000s 0Ohm — RTC_X1
X2202 32.768khz 07009-00112000
R2210 10MOHM
C2204 15PF/50V — RTC_X2_X1 — R2221 nbs_r020_h12_000s 0Ohm — RTC_X2
GND

DGPU CLKReq#

+3VSUS
R2203 10KOhm
CLKREQ0_PEGA#
For Optimus
Q2201 2N7002K
[25,45,77] DGPU_PWROK
GND

PCH CLKREQ Setting:

+3VSUS
R2219 10KOhm CLK_REQ2#
R2214 10KOhm CLK_REQ4#
R2226 10KOhm CLK_REQ5#
+3VS
R2217 10KOhm CLK_REQ6#
R2215 10KOhm CLK_REQ8#
Prevent leackage Modied by TG 20180706
R2223 10KOhm CLK_REQ0#
GND

U2001G

@ T2211 — GPP_A16 — BE33 GPP_A16/CLKOUT_48
[6] CLK_24M — D7 CLKOUT_CPUNSSC_P
[6] CLK_24M — C6 CLKOUT_CPUNSSC_N
[6] CLK_PCH_BCLK — B8 CLKOUT_CPUBCLK_P
[6] CLK_PCH_BCLK# — C8 CLKOUT_CPUBCLK_N
U9 XTAL_OUT — XTAL24_OUT — U10 XTAL_IN — XTAL24_IN
R2218 1% 60.4Ohm — T3 XCLK_BIASREF
BA49 RTCX1 — RTC_X1
BA48 RTCX2 — RTC_X2

#0 : GPU	[70]	CLKREQ0_PEGA#	R2222 0402	BF31 GPP_B5/SRCCLKREQ0#	CLK_REQ0#
#2 : WLAN	[53]	CLKREQ2_WLAN#	R2206 0402	BE31 GPP_B6/SRCCLKREQ1#	CLK_REQ2#
#4 : GLAN	[33]	CLKREQ4_GLAN#	R2202 0402	AR32 GPP_B7/SRCCLKREQ2#	CLK_REQ4#
#5 : TBT	[11]	CLKREQ5_TBT#	R2225 0Ohm	BB30 GPP_B8/SRCCLKREQ3#	CLK_REQ5#
#6 : SSD1	[41]	CLKREQ6_NGFF1#	R2255 0402	BA30 GPP_B9/SRCCLKREQ4#	CLK_REQ6#
#8 : SSD2	[40]	CLKREQ8_NGFF2#	R2207 0402	AN29 GPP_B10/SRCCLKREQ5#	CLK_REQ8#
				AE47 GPP_H0/SRCCLKREQ6#	
				AC48 GPP_H1/SRCCLKREQ7#	
				AE41 GPP_H2/SRCCLKREQ8#	
				AF48 GPP_H3/SRCCLKREQ9#	
				AC41 GPP_H4/SRCCLKREQ10#	
				AC39 GPP_H5/SRCCLKREQ11#	
				AE39 GPP_H6/SRCCLKREQ12#	
				AB48 GPP_H7/SRCCLKREQ13#	
				AC44 GPP_H8/SRCCLKREQ14#	
				AC43 GPP_H9/SRCCLKREQ15#	

V2 CLKOUT_PCIE_N15 — V3 CLKOUT_PCIE_P15
T2 CLKOUT_PCIE_N14 — T1 CLKOUT_PCIE_P14
AA1 CLKOUT_PCIE_N13 — Y2 CLKOUT_PCIE_P13
AC7 CLKOUT_PCIE_N12 — AC6 CLKOUT_PCIE_P12
7 OF 13
COMETLAKE_H_PCH

CLKOUT_ITPXDP_P — Y4 — T2231 @ — PCH XDP 100 MHz
CLKOUT_ITPXDP_N — Y3 — T2230 @
CLK_ITP_BCLK_PCH
CLK_ITP_BCLK_PCH#

CLKOUT_CPUPCIBCLK_P — A6 — CLK_PCI_BCLK [6] — CPU 100 MHz
CLKOUT_CPUPCIBCLK_N — B6 — CLK_PCI_BCLK# [6]

CLKOUT_PCIE_N0 — AJ6 — CLK0_PCIE_PEG#_VGA [70] — GPU 100 MHz
CLKOUT_PCIE_P0 — AJ7 — CLK0_PCIE_PEG_VGA [70]
CLKOUT_PCIE_N1 — AH9 — CLK0_PCIE_PEG_GPU_X1
CLKOUT_PCIE_P1 — AH10

CLKOUT_PCIE_N2 — AE14 — R2204 0402 — CLK2_PCIE_WLAN# [53] — PCIE#16 WLAN
CLKOUT_PCIE_P2 — AE15 — R2205 0402 — CLK2_PCIE_WLAN [53]
CLKOUT_PCIE_N3 — AE6
CLKOUT_PCIE_P3 — AE7
CLKOUT_PCIE_N4 — AC2 — R2236 0402 — CLK4_PCIE_GLAN# [33] — PCIE#15 GLAN
CLKOUT_PCIE_P4 — AC3 — R2234 0402 — CLK4_PCIE_GLAN [33]
CLK4_PCIE_GLAN_X1
CLKOUT_PCIE_N5 — AB2 — R2216 0Ohm — CLK5_PCIE_TBT# [11] — PCIE#17-20 TBT
CLKOUT_PCIE_P5 — AB3 — R2224 0Ohm — CLK5_PCIE_TBT [11]
CLK5_PCIE_TBT_X1
CLKOUT_PCIE_N6 — W4 — R2228 0402 — CLK6_PCIE_NGFF1# [41] — PCIE #9~12 NGFF1 (SSD)
CLKOUT_PCIE_P6 — W3 — R2229 0402 — CLK6_PCIE_NGFF1 [41]
CLK6_PCIE_NGFF1_X1
CLKOUT_PCIE_N7 — W7
CLKOUT_PCIE_P7 — W6
CLKOUT_PCIE_N8 — AC14 — R2252 0402 — CLK8_PCIE_NGFF2# [40] — PCIE #21~24 NGFF2 (SSD)
CLKOUT_PCIE_P8 — AC15 — R2220 0402 — CLK8_PCIE_NGFF2 [40]
CLK8_PCIE_NGFF2_X1
CLKOUT_PCIE_N9 — U2
CLKOUT_PCIE_P9 — U3
CLKOUT_PCIE_N10 — AC9
CLKOUT_PCIE_P10 — AC11
CLKOUT_PCIE_N11 — AE9
CLKOUT_PCIE_P11 — AE11
CLKIN_XTAL — R6

CLKIN_XTAL — R2249 10KOhm @ — GND
R2250 @ 0Ohm — CLKIN_XTAL_PCH — CLKIN_XTAL_PCH [53]
C2206 2.2PF/50V @ — GND

U2001F

USB3.1 Port1 : Standard A
J3801

[38]	U3_U3TXDN1	F9	USB31_1_TXN	
[38]	U3_U3TXDP1	F7	USB31_1_TXP	
[38]	U3_U3RXDN1	D11	USB31_1_RXN	
[38]	U3_U3RXDP1	C11	USB31_1_RXP	

USB3.1 Port2 : Standard A
J5202

[52]	U3_U3TXDN2	C3	USB31_2_TXN	
[52]	U3_U3TXDP2	D4	USB31_2_TXP	
[52]	U3_U3RXDN2	B9	USB31_2_RXN	
[52]	U3_U3RXDP2	C9	USB31_2_RXP	

USB3.1 Port3 : Standard A
J5201

[52]	U3_U3TXDP3	G12	USB31_3_TXP	
[52]	U3_U3TXDN3	F11	USB31_3_TXN	
[52]	U3_U3RXDP3	C10	USB31_3_RXP	
[52]	U3_U3RXDN3	B10	USB31_3_RXN	

C17 USB31_6_TXN
C16 USB31_6_TXP
G14 USB31_6_RXN
F14 USB31_6_RXP
C15 USB31_5_TXN
B15 USB31_5_TXP
J13 USB31_5_RXN
K13 USB31_5_RXP
C14 USB31_4_TXP
B14 USB31_4_TXN
J15 USB31_4_RXP
K16 USB31_4_RXN
6 OF 13
COMETLAKE_H_PCH

BB39 GPP_A1/LAD1/ESPI_IO0 — LPC_AD0 [30,44]
AW37 GPP_A2/LAD1/ESPI_IO1 — LPC_AD1 [30,44]
AV37 GPP_A3/LAD2/ESPI_IO2 — LPC_AD2 [30,44]
BA38 GPP_A4/LAD3/ESPI_IO3 — LPC_AD3 [30,44]
BE38 GPP_A5/LFRAME#/ESPI_CS0# — LPC_FRAME# [30,44]
AW35 GPP_A6/SERIRQ/ESPI_CS1# — INT_SERIRQ [30]
BA36 GPP_A7/PIRQA#/ESPI_ALERT0#
BE39 GPP_A8/RCIN#/ESPI_ALERT1# — PCI_INTA# — RC_IN# [30]
BF38 GPP_A14/SUS_STAT#/ESPI_RESET# — PCH_SUS_STAT#
BB36 GPP_A9/CLKOUT_LPC0/ESPI_CLK — R2245 22Ohm — CLK_KBCPCI_PCH [30]
BB34 GPP_A10/CLKOUT_LPC1 — CLK_KBCPCI_PCH_X1 — R2201 220Ohm — CLK_DEBUG [44]
CLK_DEBUG_X1
T48 GPP_K19/SMI# — T47 GPP_K18/NMI# — GPP_K18 — R2227 0Ohm — TBT_WAKE# [11]
/TBTNE_RTD3
AH40 GPP_E6/SATA_DEVSLP2
AH35 GPP_E5/SATA_DEVSLP1 — NGFF1_DEVSLP [41]
AL48 GPP_E4/SATA_DEVSLP0
AP47 GPP_F9/SATA_DEVSLP7
AN37 GPP_F8/SATA_DEVSLP6
AN46 GPP_F7/SATA_DEVSLP5
AR47 GPP_F6/SATA_DEVSLP4
AP48 GPP_F5/SATA_DEVSLP3

T2205 @

2017/11/30
Add NGFF1_DEVSLP

+3VS
PCI_INTA# — R2208 10KOhm
INT_SERIRQ — R2246 10KOhm
NGFF1_DEVSLP — R2251 @ 10KOhm

+3VSUS
GPP_K18 — R2230 10KOhm

ASUS	Project Name: GX502GX		Rev: R1.2
Title :	PCH-CPT(3)_FDI,DMI,SYS PWR		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, February 21, 2020	Sheet 22 of 99		

Main Board

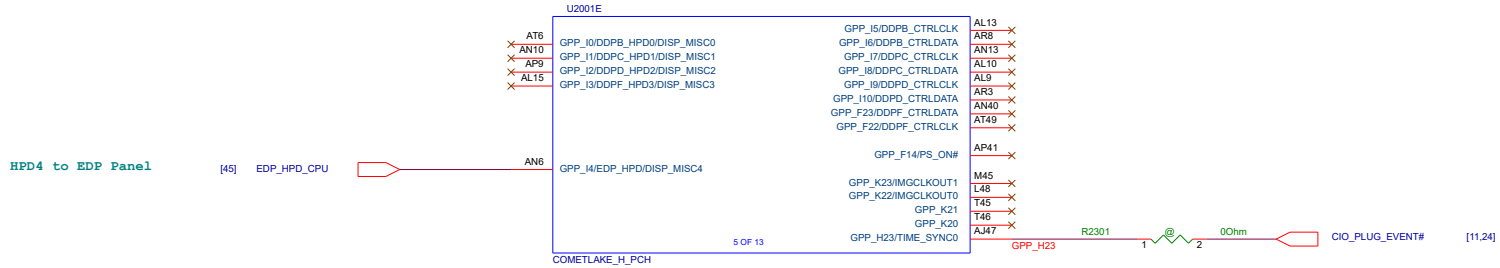
HPD0 to DP

HPD1 to HDMI

HPD2 to TBT

HPD3 to VGA

HPD4 to EDP Panel



DDP Strap Setting Update :
0 = Port is not detected (Default)
1 = Port is detected

GPP_I6 / DDPB_CTRLDATA	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I8 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I10 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_F23	Display Port F Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well. 3. This strap applies to platforms that support Display Port F only. Refer to the platform's processor documentation for info on Display Port F support.

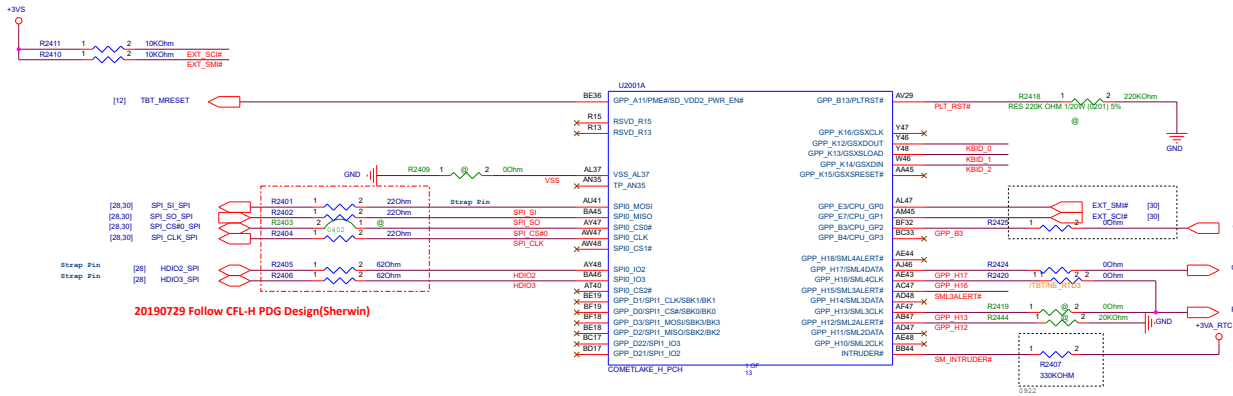
5.6 Digital Display Interface Disabling and Termination Guidelines

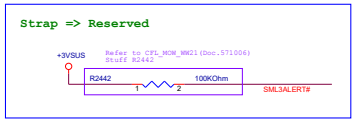
All the digital display ports on the Coffee Lake processor have a strap associated with it. The port strap needs to be set to configure each digital port irrespective of the digital display technology HDMI/DP. The following table lists all the digital display straps and guidelines to enable/disable a respective port on the platform. All the straps are sampled on the rising edge of the PWROK signal.

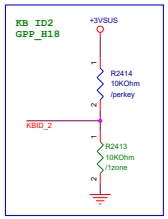
Table 5-15. DDI Disabling and Termination Guidelines

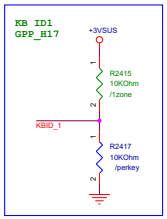
Port	Strap	How to Enable PortΩ	How to Disable PortΩ
Port 1	DDPB_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect
Port 3	DDPD_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect

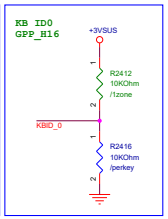
Project Name: GX502GX		Rev: R1.2
Title : PCH-CPT(4)_eDP,PCI,DP		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, February 21, 2020	Sheet 23 of 99	



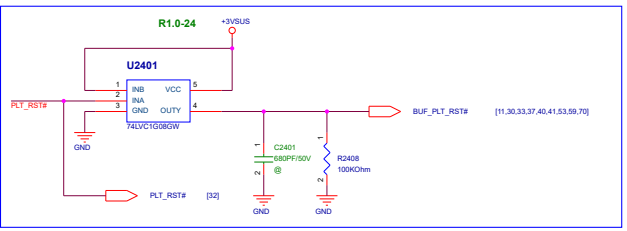








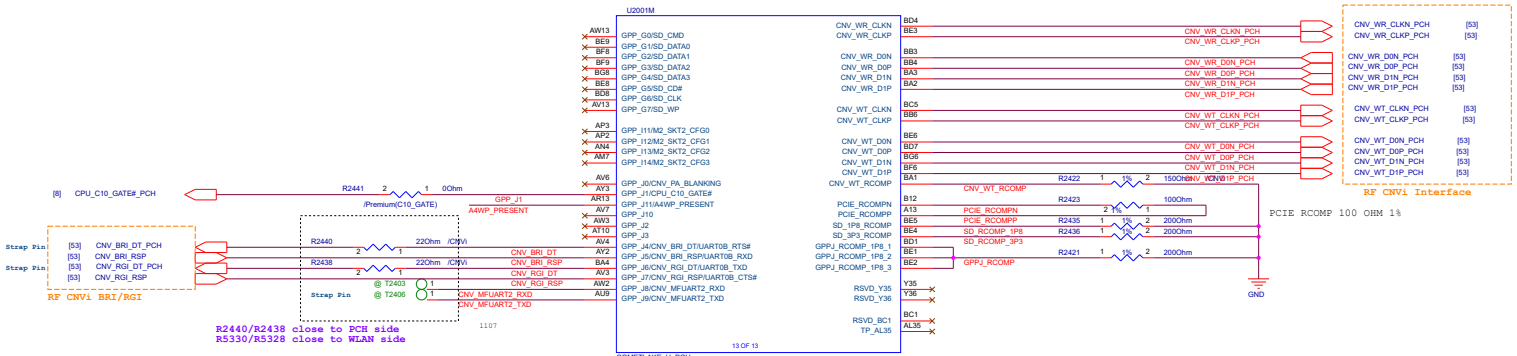
KB ID PCH Side(HW請依照此表格做設計判斷) *BIOS會再反向				
Code	ROG RGB KB Type	KBID 2 (GPP_H18)	KBID 1 (GPP_H17)	KBID 0 (GPP_H16)
0x00	Normal Keyboard	H	H	H
0x01	QWERASD Partition Keyboard	H	H	L
0x02	4 Zone RGB Keyboard	H	L	H
0x03	Per Key RGB Keyboard	H	L	L
0x04	1 Zone RGB Keyboard	L	H	H



PCH_GPP_H12: weak internal pull down

Strap => eSPI Flash Sharing Mode

0: Master Attached Flash Sharing (MAFS) enable (Default)
1: Slave Attached Flash Sharing (SAFS) enable



GPP_J4(CNV_BRI_DT):
This signal has a weak internal pull down.
0 = 38.4MHz XTAL frequency selected.(Default)
1 = 24MHz XTAL frequency selected.

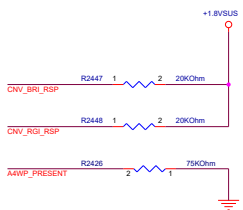
(MOW39)
Pin Strap for XTAL frequence selection
An external 4.7K PU to VCC(1.8V or 3.3V) is required on this strap for PCH 24 MHZ XTAL operation

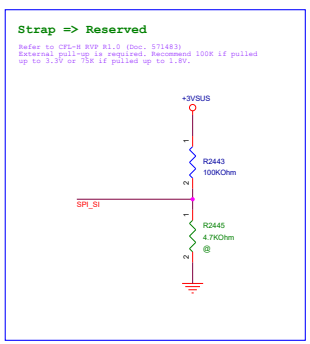
GPP_J6(CNV_RGI_DT):
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
[Intel FAE]
RGI_DT has an automatic detect CNVi mechanism, please do not use external PD.
The CRF has an internal strong 1K PD already.
Do not leave this pin float,
if CNVi is not used, it still need a 20K ohm PU.

GPP_J9:
The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

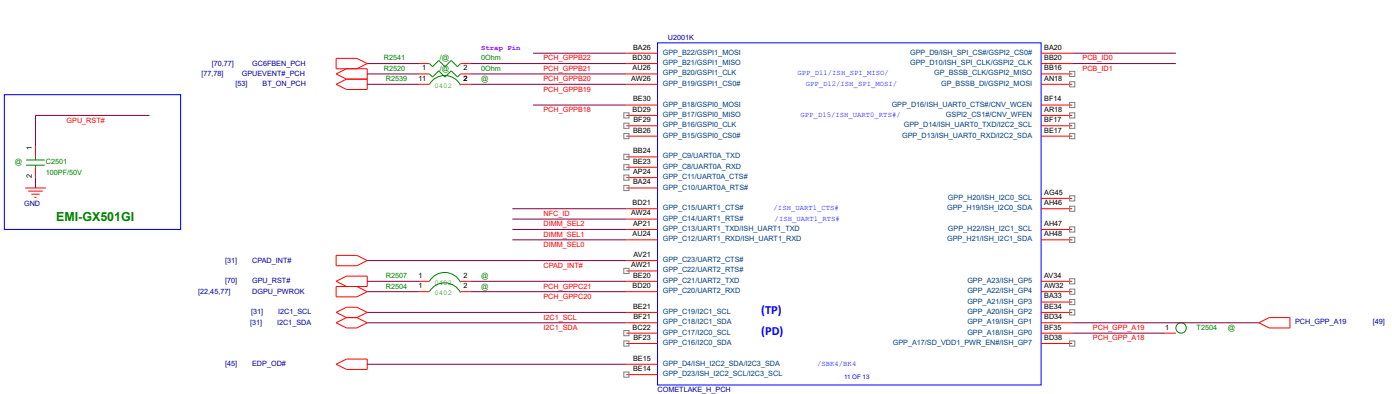
Strap

GPP_J4(CNV_BRI_DT):Must PU 4.7K
GPP_J6(CNV_RGI_DT):Must PU 20K

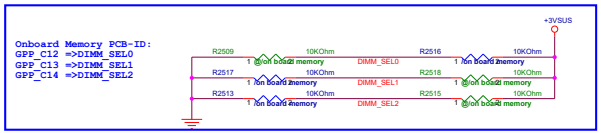




Project Name	GX502GX	Rev	R1.2
Title :	PCH-CPT(5)_LPC,SPI,SMBUS		
Size	Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, February 21, 2020		Sheet 24	of 99

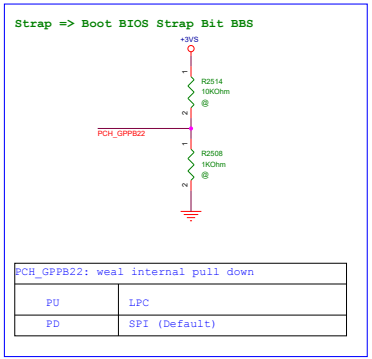


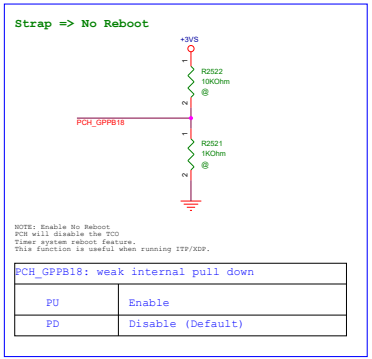
2017/12/05 Remove TBT_I2C_SCL_PCH/TBT_I2C_SDA_PCH by James



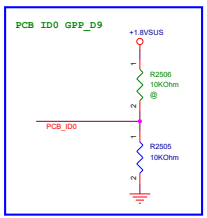
DDR4 Memory Down pool

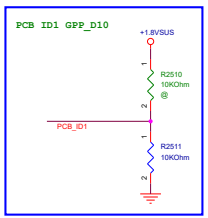
	DDR4 SDRAM X8					
	Micron (1Rx8Gb) 03012-00030700 Micron_DDR4_2666 MT40A1G8SA-075:E	Samsung (1Rx16Gb) 03012-00060000 Samsung_DDR4_2666 K4AAG085WA-BCTD	Micron (1Rx8Gb) 03012-00030900 Micron_DDR4_3200 MT40A1G8SA-062E:J	Micron (1Rx16Gb) 03012-00060300 Micron_DDR4_3200 MT40A2G8VA-062E:B	Samsung (1Rx8Gb) 03012-00031000 Samsung_DDR4_3200 K4AAG085WC-BCWE	Samsung (1Rx16Gb) 03012-00060100 Samsung_DDR4_3200 K4AAG085WA-BCWE
DIMM_SEL0	L	L	L	H	H	L
DIMM_SEL1	L	L	H	L	H	L
DIMM_SEL2	H	L	L	L	L	L





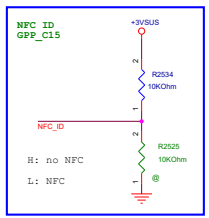
PCH_GPPC21 : DGPU_RST#
PCH_GPPC22 : DGPU_PWR_EN#





Touch Pad ID
GPP_D11

Touch Panel ID
GPP_D12



X-tal Frequency Select

Cannon Lake PCH-LP

- XTAL_Freq_Select = GPP_H21
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

Cannon Lake PCH-H

- XTAL_Freq_Select = GPP_J4
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

Project Name: GX502GX			Rev: R1.2
Title: PCH-CPT(6)_GPIO,MISC			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, February 21, 2020	Sheet 25 of 99		

Refer to CNL-H PCH EDS R1.0 (Doc.571182)

Table 8-1. Power Descriptions for PCH in CNL-H

Name	Description
VCCPHVLDO_1P8	**1.8V Primary Well.** On the motherboard, this power pin must be connected to VCCPRIM_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.

VCCPHVLDO_1P8	AF19
VCCPHVLDO_1P8	AF20

VCCDPHY_1P24	**1.24V for CNVi logic**. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Cannon Lake -U/Y PDG for implementation details.

GPIO Voltage Level

Group	Power pin	Power option	Power plane
GPP_A	VCCGPPPA	3.3V	+3VSUS
GPP_B	VCCGPPBC	3.3V	+3VSUS
GPP_C	VCCGPPBC	3.3V	+3VSUS
GPP_D	VCCGPPPD	1.8V or 3.3V	+1.8VSUS
GPP_E	VCCGPPEF	3.3V	+3VSUS
GPP_F	VCCGPPEF	3.3V	+3VSUS
GPP_G	VCCGPPG_3P3 VCCPRIM_3P3	Dynamic voltage to be config SDIO	+3VSUS +3.8VSUS
GPP_H	VCCGPPHK	3.3V	+3VSUS
GPP_I	VCCPRIM_3P3	3.3V Only	+3VSUS
GPP_J	VCCPRIM_1P8	1.8V Only	+1.8VSUS
GPP_K	VCCGPPHK	3.3V	+3VSUS
GPD	VCCDSW_3P3	3.3V Only	+3VA_DSW

Main Board

09/12 NF add

SHORT PCH PINS AJ22, AJ23 ,AK22, AK23 TOGETHER IN SURFACE LAYER AND CONNECT BGS TO EDGE CAP WITH LOWEST LOOP INDUCTANCE AS PDG RECOMMENDS.

11/22 Remove R2634/R2635 by James

11/22 Remove R2610/14/62/16/17/60/61/56/07/08 by James

11/22 Changed R2609/59 size from 1uH to 0 ohm by James

11/22 Changed R2649 size from 0603 to 0402 by James

Pureple reference CRB
Blue reference EDS

11/22 Remove R2669/02/03/04/36 by James

11/22 Remove R2667 by James

11/22 Changed R2668 size from 0603 to 0402 by James

11/22 Remove R2648 by James

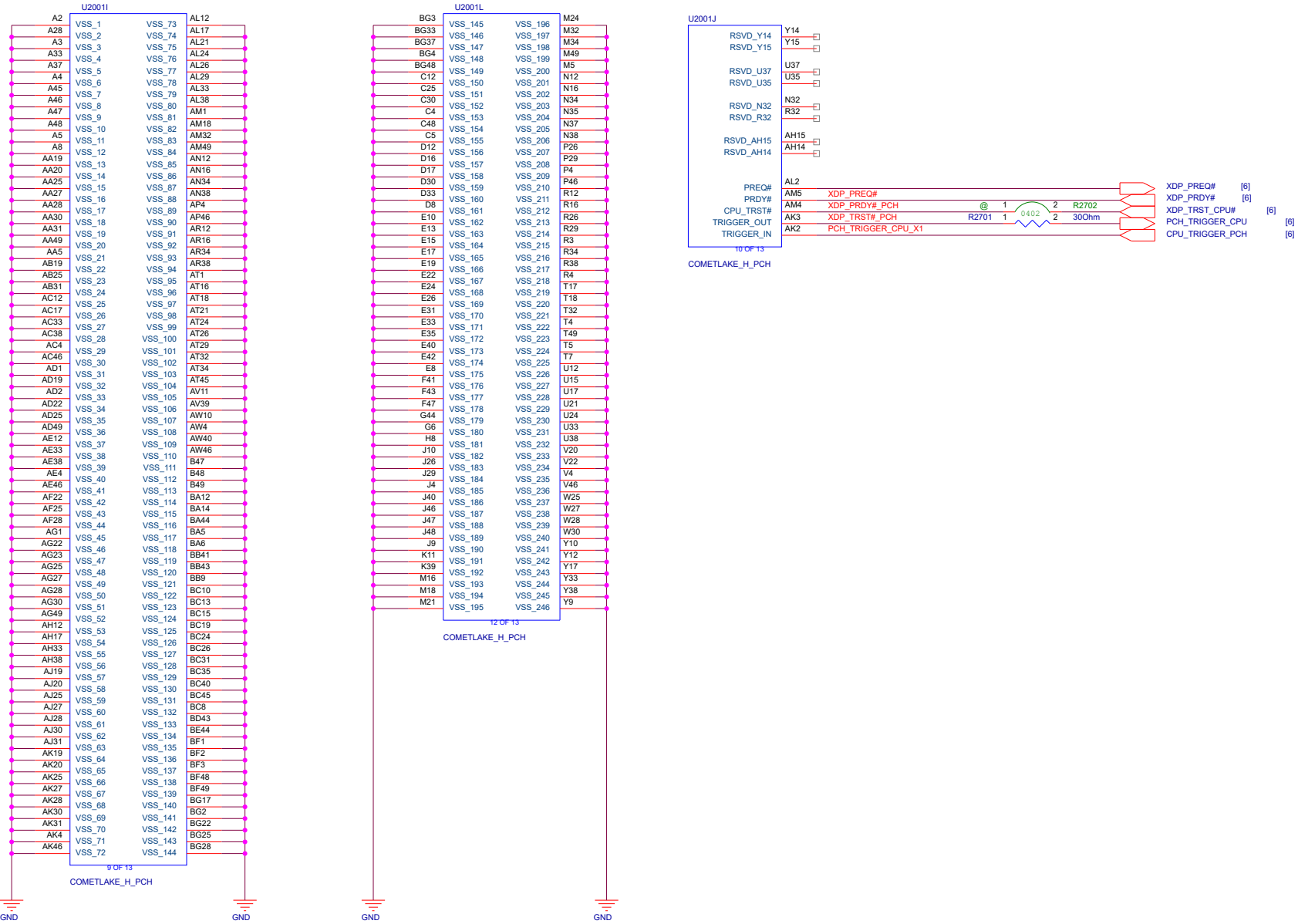
11/22 Remove R2666/65/30/32/31/39/41/43 by James

Project Name	Rev
GX502GX	R1.2

Title : PCH-CPT(7)_POWER.GND

Size: | Dept.: ASUSTeK COMPUTER | Engineer: EE

Date: Friday, February 21, 2020 | Sheet 26 of 89



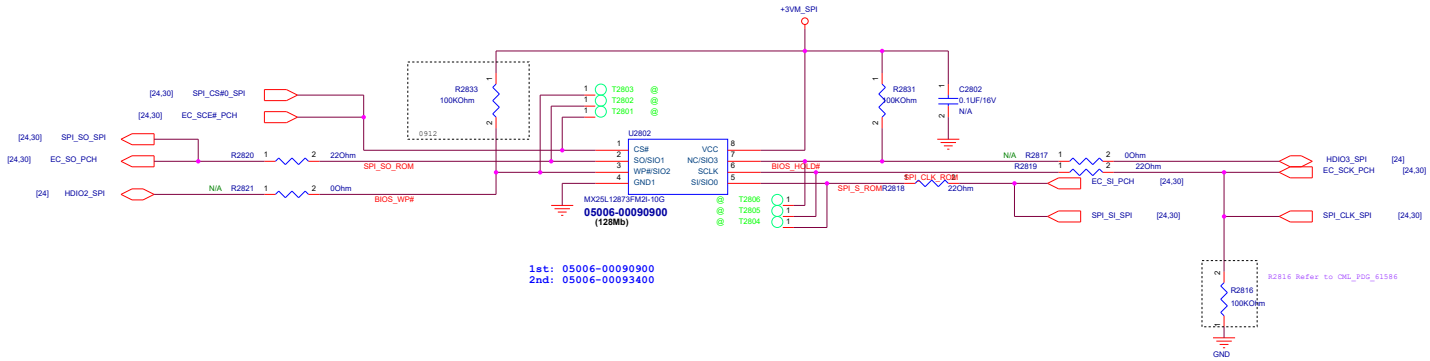
Project Name: GX502GX		Rev: R1.2
Title : PCH-CPT(8)_POWER,GND		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, February 21, 2020	Sheet 27 of 99	

SPI Power

1st SPI ROM

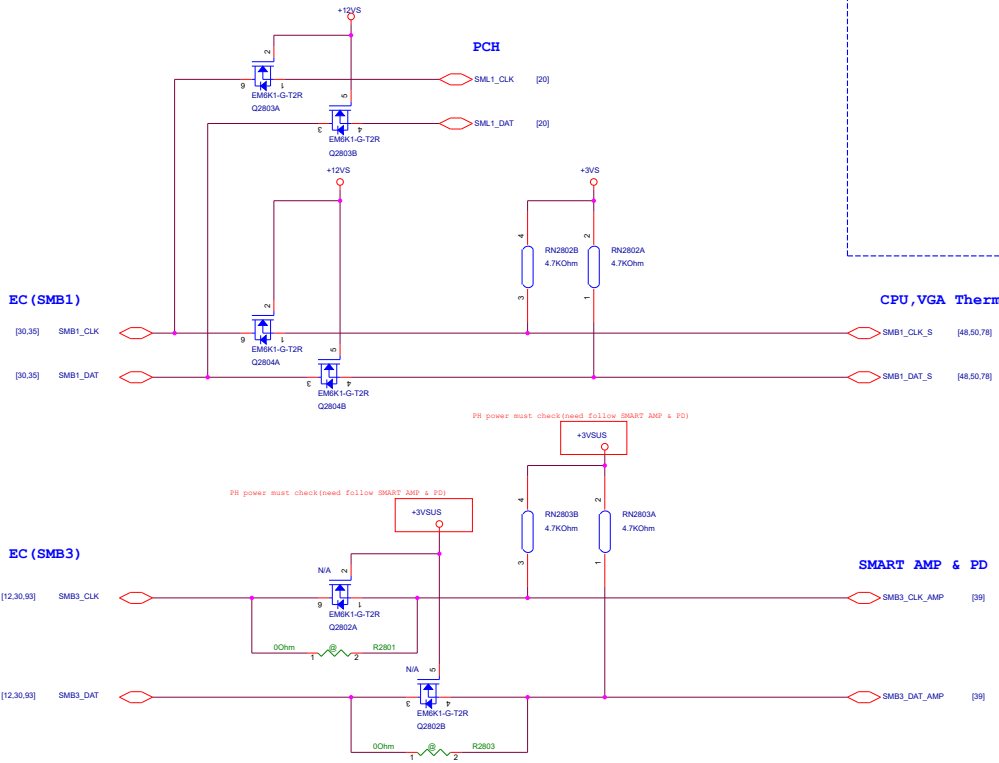
1st: 05006-00090900 FLASH MXIC MX25L12873FM2I-10G 128M SOP-8L
2nd: 05006-00093100 FLASH GD25B127DSIGG IGADEVICE 128MB SOP8

Main Board

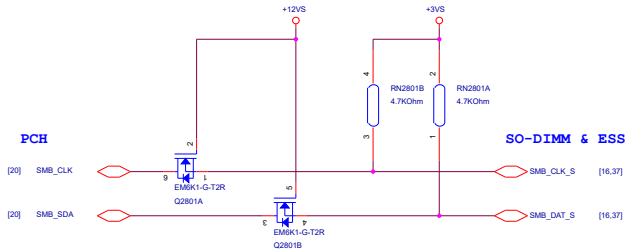


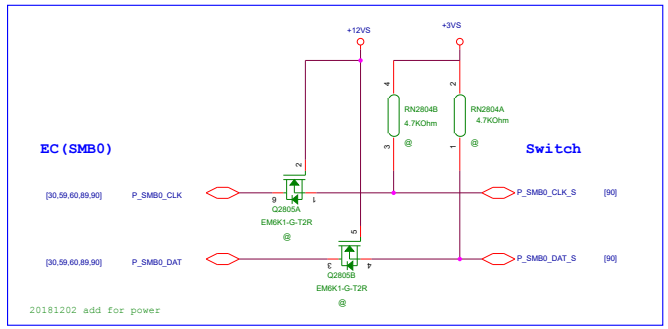
1st: 05006-00090900
2nd: 05006-00093400

System Management Interface



SMBus Interface





ASUS	Project Name: GX502GX		Rev: R1.2
Title : PCH-SPI ROM,OTH			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, February 21, 2020	Sheet 28 of 99		

Main Board

ASUS	Project Name: GX502GX	Rev: R1.2
Title : TEST POINT		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, February 21, 2020	Sheet 29 of 99	

EC 8995

Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

ITE Version	ASUS P/N
IT8225VG-128/CX	06037-00260300
IT5125VG-128/CX	06037-00370000

Power
R1.0-29
+3VS
+3VA_EC
+3VPLL
+3VA
C3002 0.1UF/16V
C3051 0.1UF/16V
C3052 0.1UF/16V
C3053 0.1UF/16V
C3054 0.1UF/16V
C3004 0.1UF/16V
C3005 0.1UF/16V
C3007 0.1UF/16V
C3001 0.1UF/16V
SL3005 0603
closed to pin A1

N key
+3VA_DSW
THRO_CPU# R3032 10KOhm
NKey_WRST R3050 10KOhm

NVDD_SMB_SEL R3016 10KOhm
20181202 add for power

D3001 BAT54AW 07G004068011
AC_IN_OC# MANCHG_AC_IN_OC# [89] SLVCHG_AC_IN_OC# [93]
2018/06/28 by James

LCD_BACKOFF# [45]
C3016 N/A 0.1UF/16V

U3001 IT5125VG-128/CX

PU/PD
PWR_SW# R3037 100KOhm
AC_IN_OC# R3042 100KOhm
LID_SW# R3063 100KOhm
FAN_V_Switch R3026 100KOhm
SLVCHG_AC_IN_OC# R3067 100KOhm
EC_GPG2 R3035 100KOhm
AMP_SLEEP# R3034 100KOhm
PD_IRQ# R3095 100KOhm
SMB1_DAT RN3001A 4.7KOhm
SMB1_CLK RN3001B 4.7KOhm
P_SMB0_DAT RN3001D 4.7KOhm
P_SMB0_CLK RN3001C 4.7KOhm
SMB3_DAT RN3002B 2.2KOhm
SMB3_CLK RN3002A 2.2KOhm
Modified for rising time by TG 20180731
3VADSW_ON R3017 100KOhm
5VSUS_ON R3053 100KOhm
VSUS_ON R3006 1MOhm
R3056 100KOhm
R3051 1MOhm
R3030 100KOhm
for load code

IMVP8 SA Power Good
Robby 0613
IMVP8_PWRGD D3003 BAT54AW R3027 0Ohm
IMVP8_SA_PWRGD [81]

Support Slave CHG
(Prevent from leakage)
ADAPTER_IN#_R D3002 BAT54AW
ADAPTER_IN# [89]

PM_PWRBTN# R3041 10KOhm
RC_IN# R3003 10KOhm
+3VSUS
+3VS

BAT1_IN_OC# R3065 100KOhm
N501 R3008 100KOhm
PM_SLP_SUS# R3019 100KOhm
PM_SUS3# R3004 100KOhm
PM_SUS5# R3005 100KOhm
SUSB_EC# R3092 4.7KOhm
SUSC_EC# R3093 4.7KOhm
EC_OV_DDR R3021 100KOhm
LAN_PWR_EN R3033 100KOhm
EC_SCK R3002 10KOhm
EC_SCE# R3011 10KOhm
EC_SO R3007 10KOhm
EC_SI R3013 10KOhm
NKEY_PWR_EN R3001 10KOhm
PM_RSMRST# R3058 10KOhm

Battery
Thermal sensor

C3003 EC_RST# 100PF/50V @EMI
C3006 PM_PWROK 100PF/50V @EMI
C3009 BUF_PLT_RST# 100PF/50V @EMI
C3011 RC_IN# 100PF/50V @EMI
C3012 3VA_DSW_PWRGD_EC 100PF/50V @EMI
C3013 3VSUS_PWRGD 100PF/50V @EMI
C3014 3VA_DSW_PWRGD 100PF/50V @EMI
GND

C3008 0.1UF/16V
C3015 0.1UF/16V
SL3006 SL3007 0603
EC_AGND 單點下地

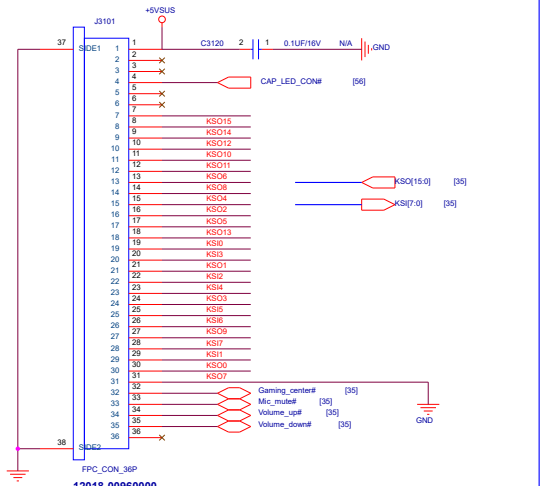
For EMI
C3025 CHG_FULL_LED# 100PF/50V
C3026 PWR_LED 100PF/50V
C3027 CHG_LED# 100PF/50V
C3028 MECH_PRESENT 100PF/50V @EMI

C3018 CLK_KBCPCI_PCH 8.2PF/50V
C3010 PWR_SW# 0.01UF/16V

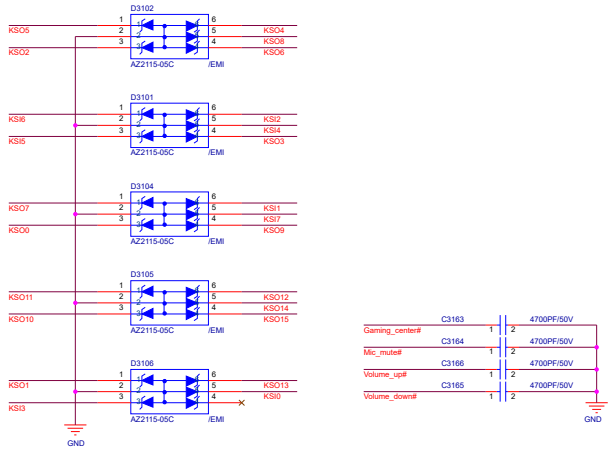
R1.0-34
R3055 100KOhm 3VA_DSW_PWRGD
R3054 100KOhm IMVP8_PWRGD
R3029 100KOhm IMVP8_SA_PWRGD
R3015 10KOhm
R3052 3VA_DSW_PWRGD_EC 3VA_DSW_PWRGD [20,58,87]

<Core Design>
Title : CR_KBC_IT8521
ASUSTeK COMPUTER
Engineer: EE
Size C | Project Name GX502GX | Rev R1.2
Date: Friday, February 21, 2020 | Sheet 30 of 99

Keyboard Connector

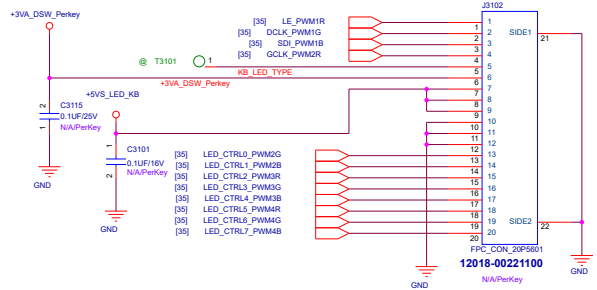


For EMI

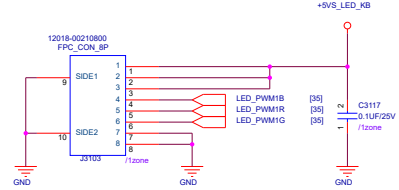


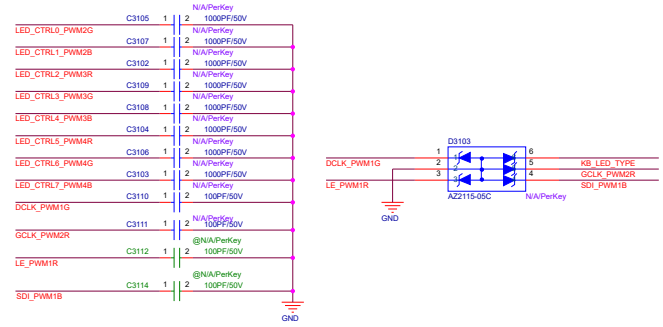
Keyboard Backlight

Perkey

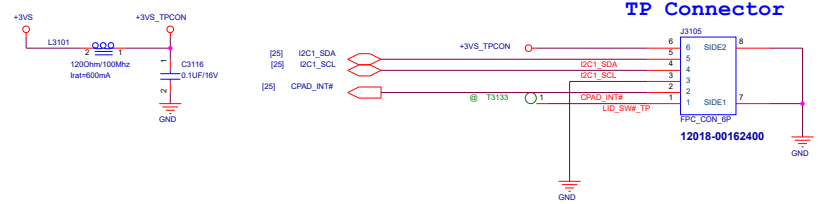


1Zone

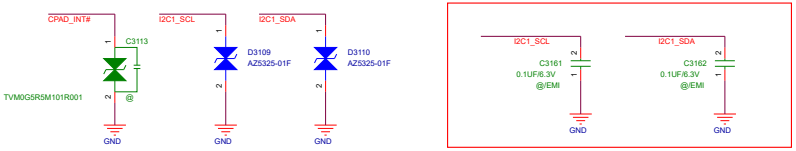




TP Connector

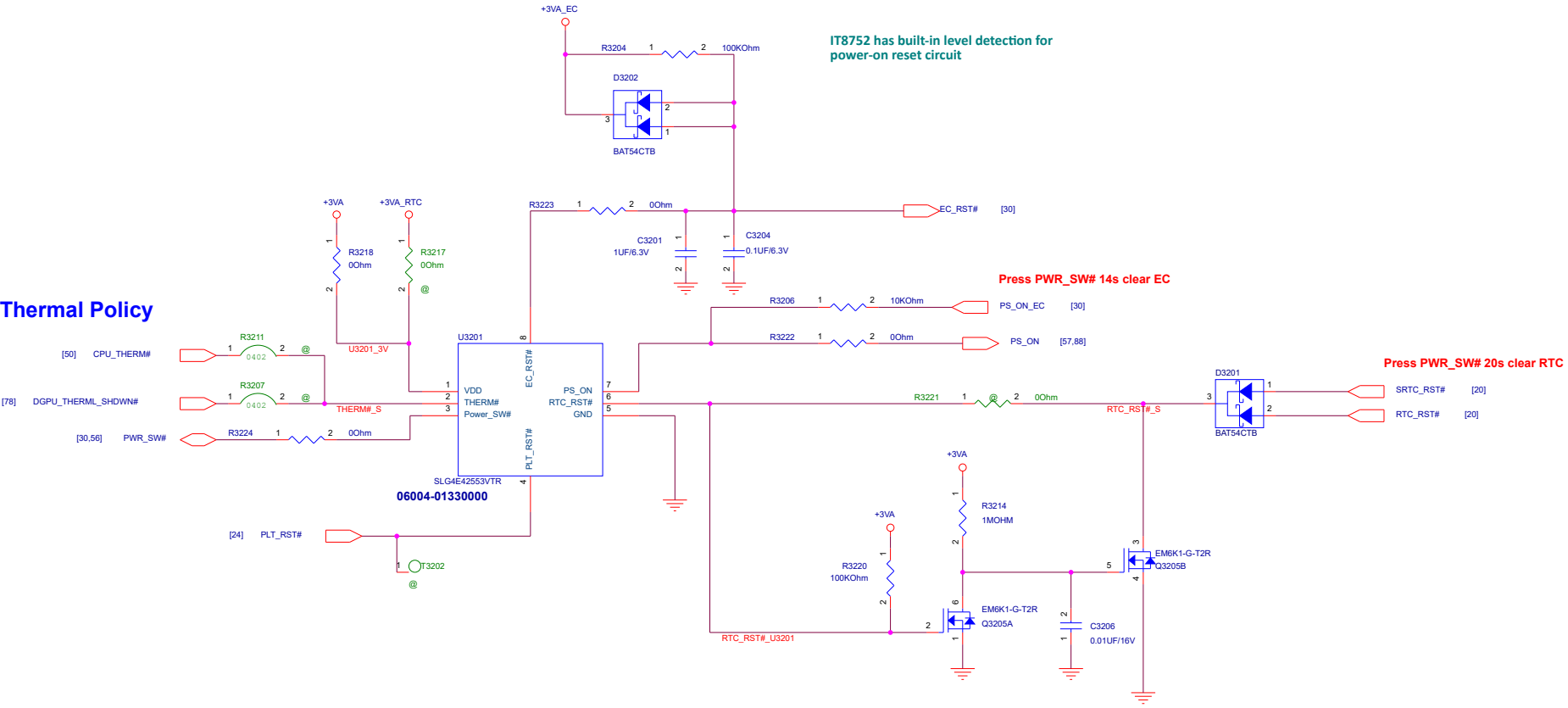


EMI Reserve
如要上件請確認容值(選擇Pico等級)



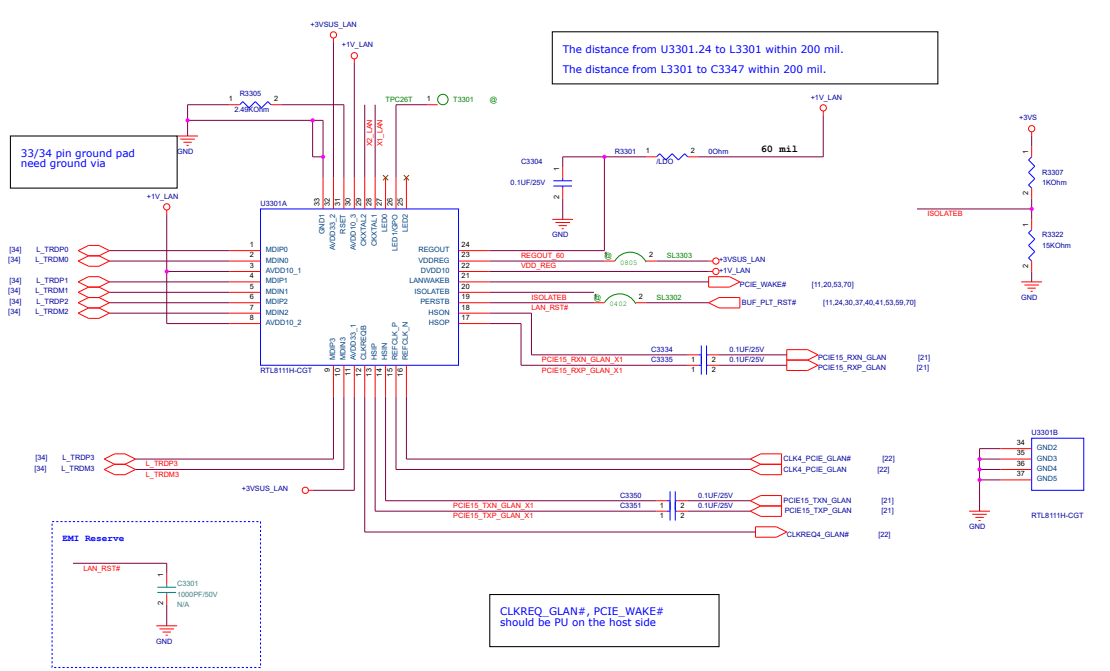
<Core Design>

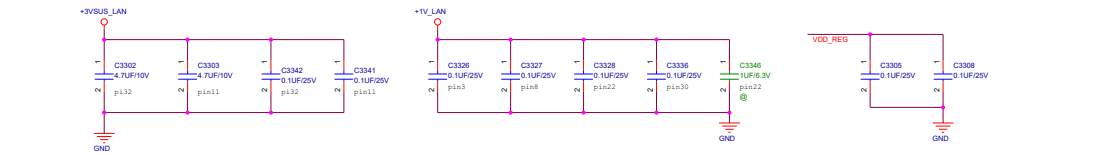
ASUSTeK COMPUTER	Title : KBC_KB & TP	
	Engineer: EE	
Size: Custom	Project Name: GX502GX	Rev: R1.2
Date: Friday, February 21, 2020	Sheet 31 of 99	



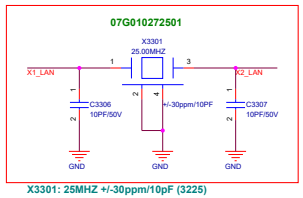
<Core Design>

ASUSTeK COMPUTER	Title : RST_Reset Circuit	
	Engineer: EE	
Size: Custom	Project Name: GX502GX	Rev: R1.2
Date: Friday, February 21, 2020	Sheet 32 of 99	





Main Board

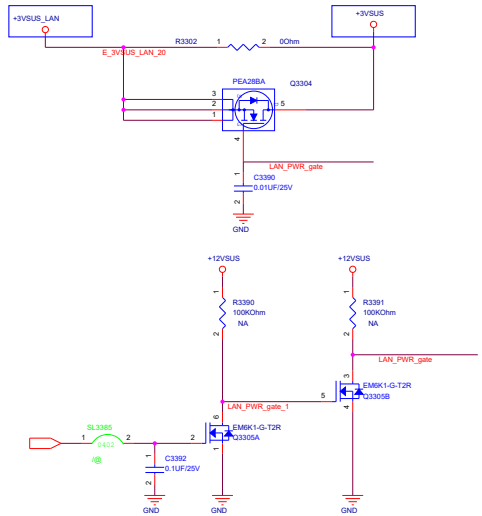


X3301: 25MHZ +/-30ppm/10pF (3225)

1st: P/N:07G010272501 TXC/7V25000011

2nd: P/N:07G010952500 HOSONIC/E3FB25

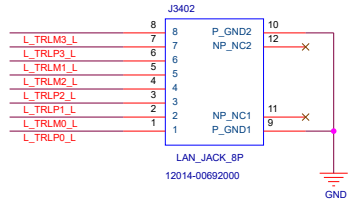
Realtek suggests 3V_LAN raise time >1ms

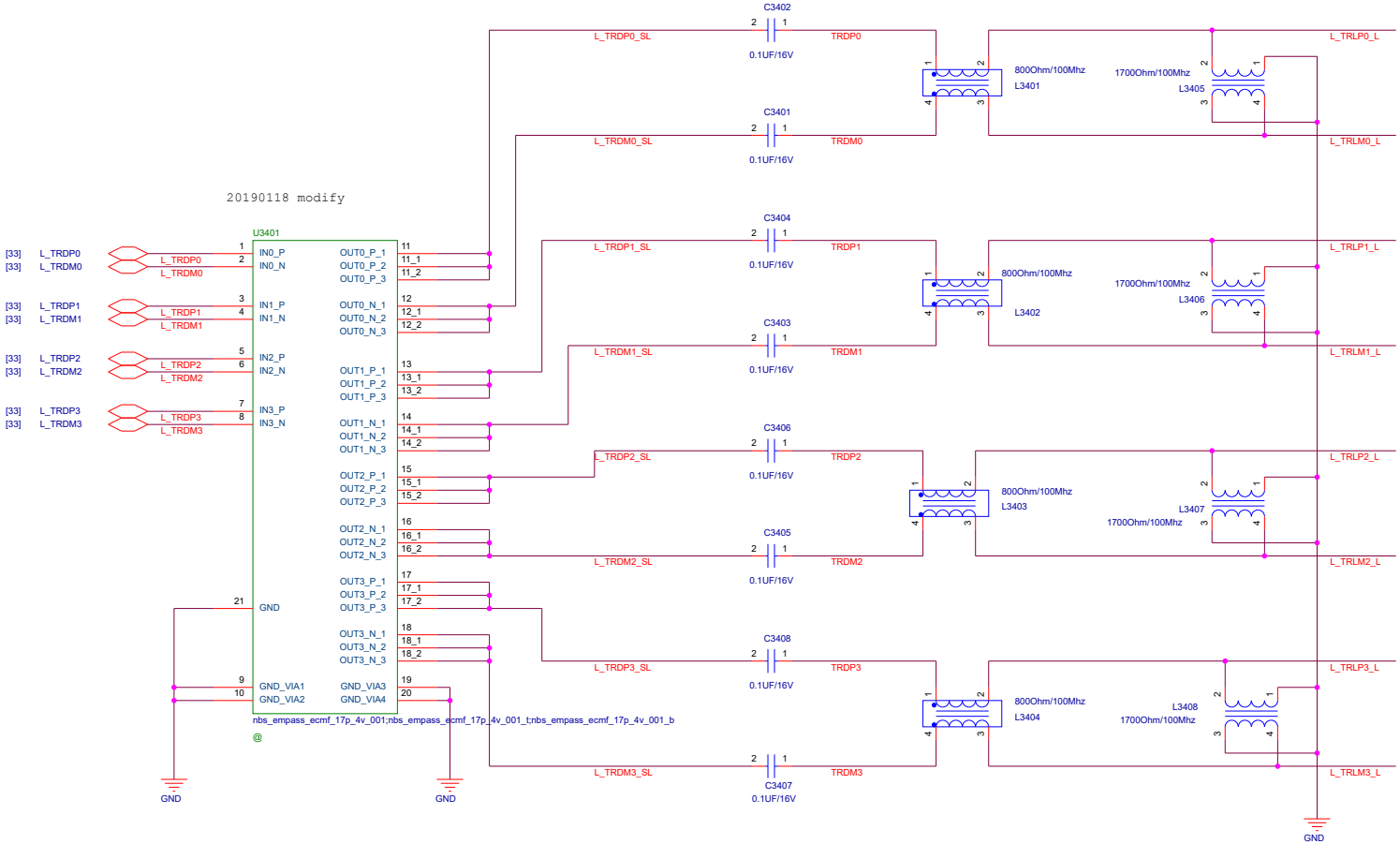


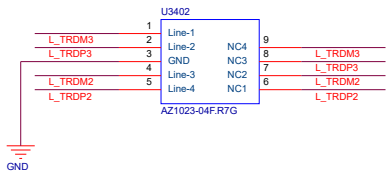
Project Name: GX502GX		Rev: R1.2
Title: LAN RTL8111GUX-CG		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, February 21, 2020	Sheet 33 of 99	

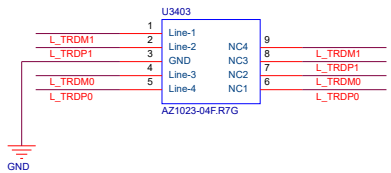
Main Board

LAN Connector







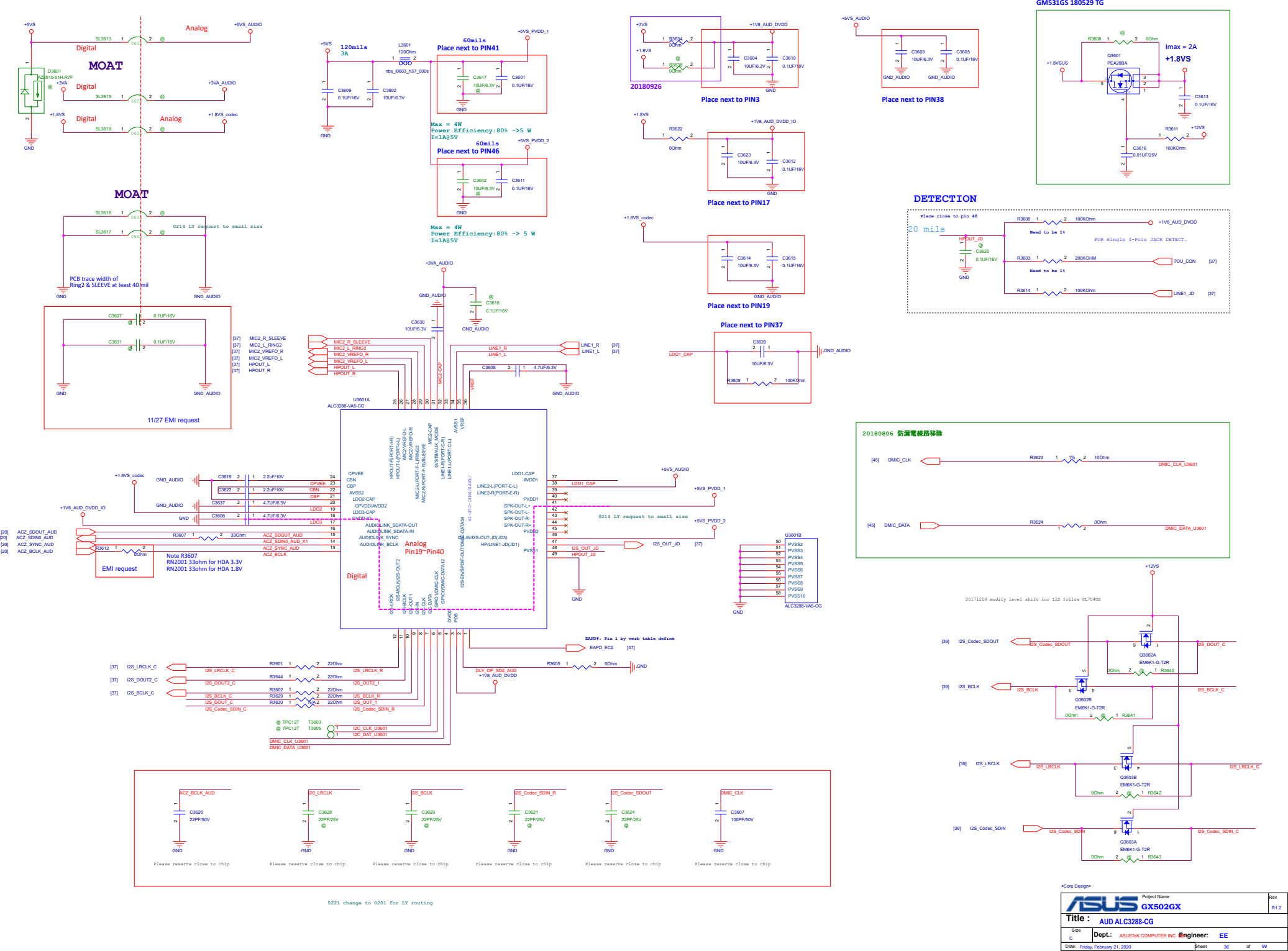


D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

ASUS	Project Name: GX502GX	Rev: R1.2
Title : LAN_RJ45_CON		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, February 21, 2020	Sheet 34 of 99	

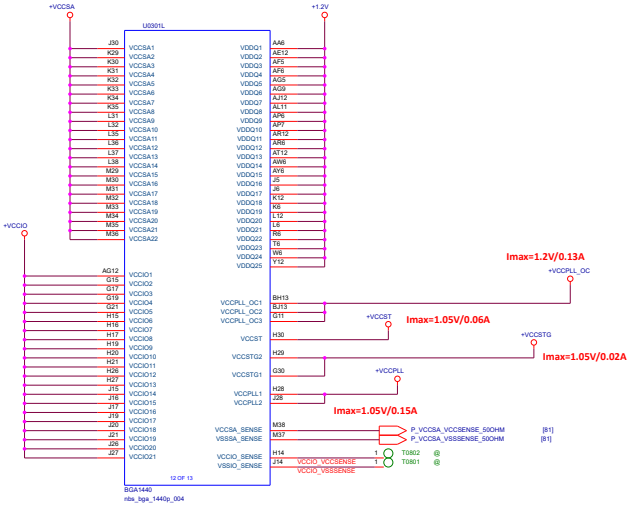


<Core Design>

Project Name: GX502GX		Rev: R1.2
Title : AUD ALC3288-CG		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Friday, February 21, 2020	Sheet 36 of 99	

Imax=1.05V/11.1A

Imax=1.2V/3.3A

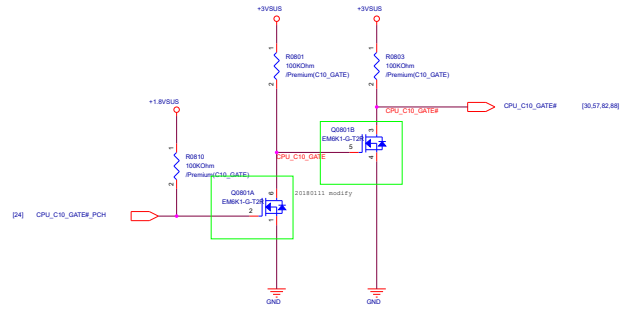


Domain	Board Edge cap	Backside cap	Notes
Vcc_{SA}	2x 47uF 0805		
	2x 22uF 0603		
		7x 10uF 0402	
		1x 1uF 0201	
V_{DDQ}		4x 22uF 0603	
		11x 10uF 0402	
Vcc_{IO}		3x 10uF 0402	
		3x 0402 (placeholder)	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.
Vcc_{ST}		1x 1uF 0201	Must be Ground referenced. Board routing resistance from BGA to Power gate should be less than 10mOhm. Do not route Vcc_{ST} closest adjacent layer over any power net other than ground.
Vcc_{STG}		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail
Vcc_{PLL}		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail. Board resistance from BGA to Power gate should be less than 130mOhm.
	1x 22uF/47uF 0805 (placeholder)		*Placeholder not stuffed.* To be placed as close as possible to BGA (H28, J28) and be placed either at board edge or backside.
Vcc_{PLL_OC}		2x 1uF 0201	Must be Ground referenced. Share with V_{DDQ}. Board resistance from BGA to Power gate should be less than 86mOhm.

Domain	Board Edge cap	Backside cap	Notes
Vcc_{ST}		1x 1uF 0201	Must be Ground referenced. Board routing resistance from BGA to Power gate should be less than 10mOhm. Do not route Vcc_{ST} closest adjacent layer over any power net other than ground.
Vcc_{STG}		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail
Vcc_{PLL}		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail. Board resistance from BGA to Power gate should be less than 130mOhm.
	1x 22uF/47uF 0805 (placeholder)		*Placeholder not stuffed.* To be placed as close as possible to BGA (H28, J28) and be placed either at board edge or backside.
Vcc_{PLL_OC}		2x 1uF 0201	Must be Ground referenced. Share with V_{DDQ}. Board resistance from BGA to Power gate should be less than 86mOhm.

Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.05VSUS	+VCCST	+VCCPLL
		+VCCSTG	
	+1.2V	+VTT	
		+VCCPLL_OC	
	+VCCSA		
	+VCCIO		

Main Board

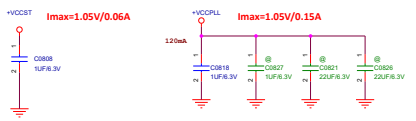


Configuration		Estimated SoC Power Delta from Config #1 to #2
Config #1 (Premium)	Config #2 (Volume)	CFL H
VccST off in S3	On in S3	+25-30mW
VccPLL_OC off in S0/C10	On in S0/C10	+3-10mW
VccPLL_OC off in S0ix	On in S0ix	+3-10mW

Other than what is documented in the table above, there is no expected SoC power delta in Sx states between Volume and Premium configurations. Independently, implementing Deep Sx (also known as DSW) may lower platform power over traditional Sx.

CPU_C10_GATE# is a signal from the Coffee Lake SoC that can be used for geting off VccSTG, VccPLL_OC and VccIO (CFL-H) in the S0/C10 system state in order to save power.

+VCCST/+VCCPLL DECAPS Place Back Side (TOP)



CFL U/H PDG Update for VCCPLL Power Rail Design Guidelines

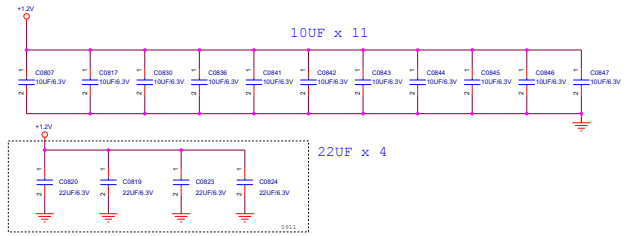
Due to Display PLL lock issues observed on systems with high noise level on VCCPLL, CFL-H BIP#571391 and CFL-U BIP#571021 Platform design guidelines has been updated with new recommendation for VCCPLL power rail.

An additional capacitor 0805 size placeholder near CPU BGA ball is recommended for better power delivery, this should be stuffed when encountered a noisy VCCPLL power rail.

This new recommendation not required for systems that follows the PDG Power Integrity guidance and kept low noise level on VCCPLL.

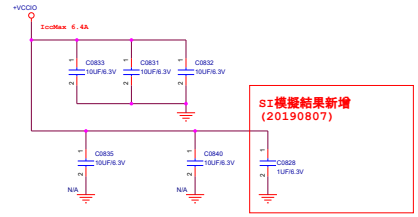
+VDDQ DECAPS Place Back Side (TOP)

Imax=1.2V/3.3A

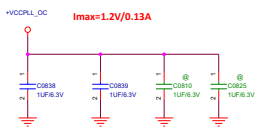


+VCCIO DECAPS Place Back Side (TOP)

Imax=0.95V/6.4A

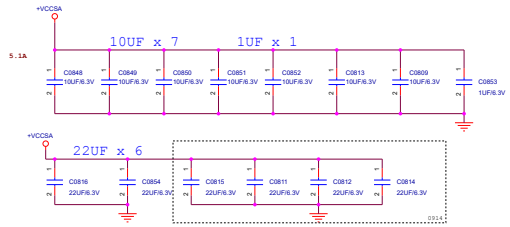


+VCCPLL_OC DECAPS Place Back Side (TOP)

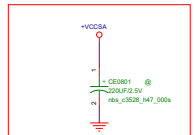


+VCCSA DECAPS Place Back Side (TOP)

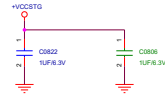
Imax=1.05V/11.1A



+VCCSA near CPU

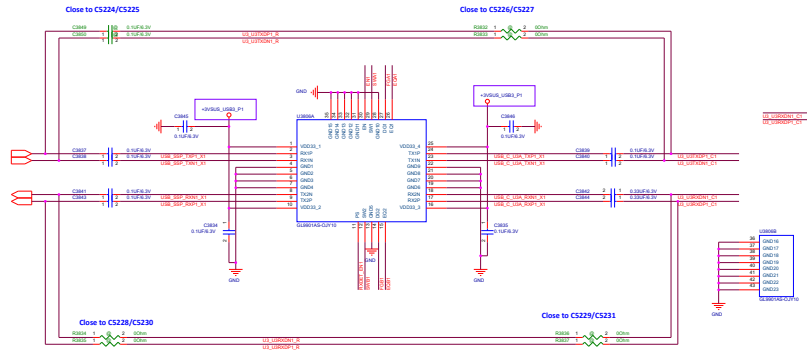


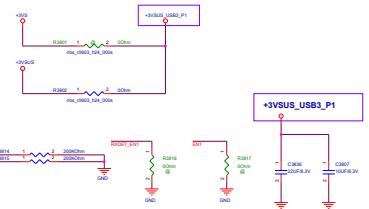
+VCCSTG DECAPS Place Back Side (TOP)



Project Name: GX502GX			Rev: R1.2
Title: CPU_PWR			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, February 21, 2020	Sheet: 8	of: 99	

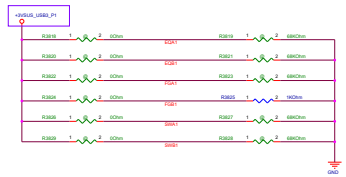
[Bypass Path]

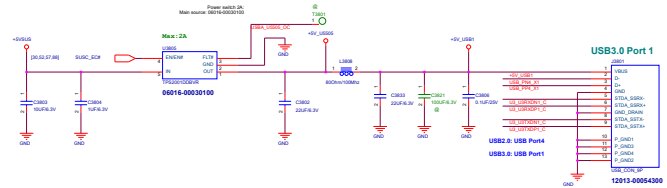




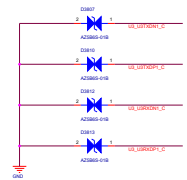
< Channel / Receiver setting for Pericom 1002B >

Setting	Channel Enable [EN]	Receiver Detection [RXDET_EN]
0 : 0 Ω to GND	Disable	Disable
1 : 0 Ω to VDD	Enable(Default)	Enable(Default)
Note	Channel Enable / Receiver detection With internal 300K pull-up R.	





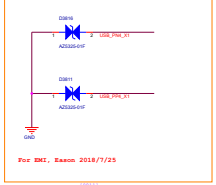
USB3.0 ESD-Protection



ESD PROTECTION

1st Source: P/N:07024-01360000 ESD PROTECTION AZ5865-01B

USB2.0 ESD-Protection



< Fine tune table for Pericom (One port Gen2) >

< EQ table for Pericom 1002B >

EQ[A:B]	Gen 1 @2.5GHz(dB)	Gen 2 @5GHz(dB)
0 : 0 Ω to GND	5.1	10.9
R : Rext to GND	1.9	6.7
F : Leave Open	3.5(Default)	8.9(Default)
1 : 0 Ω to VDD	6.8	13.1

Note : With internal 100Kohm pull-up Rup and 200kohm pull-down Rdown.
Rext = 68Kohm

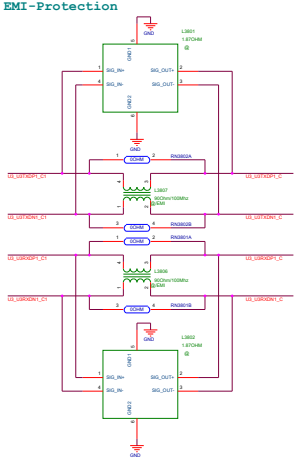
< FG table for Pericom 1002B >

FG[A:B]	Flat Gain (dB)
0 : 0 Ω to GND	-3.0
R : Rext to GND	-1.5
F : Leave Open	0 (Default)
1 : 0 Ω to VDD	+2.0

< SW table for Pericom 1002B >

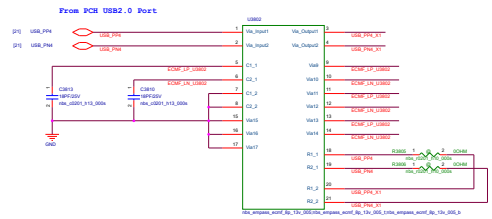
SW[A:B]	Output Linear Swing (mV)
0 : 0 Ω to GND	800
R : Rext to GND	1200
F : Leave Open	1000 (Default)
1 : 0 Ω to VDD	1100

USB3.0 EMI-Protection



R1.5

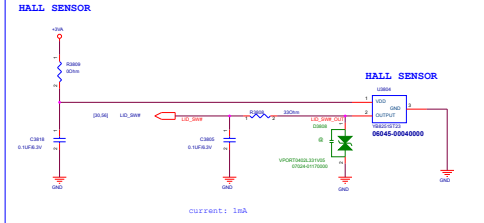
USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)



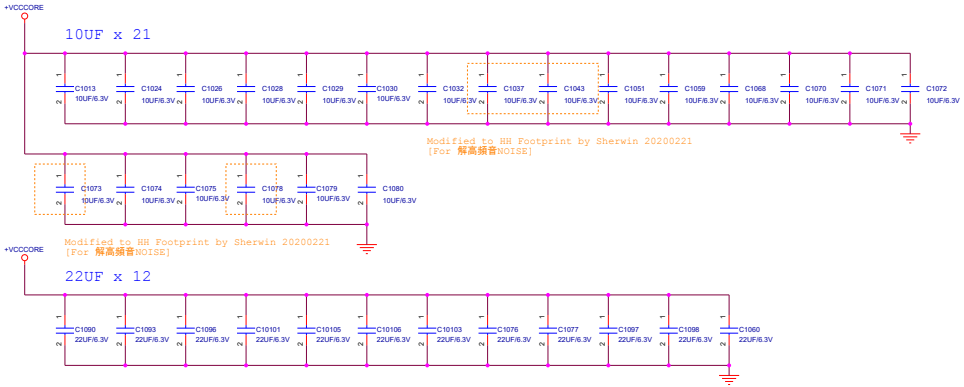
Note : 1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
2. C3809&C3810 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
4. Pin13 to Pin16 are floated in regular scheme

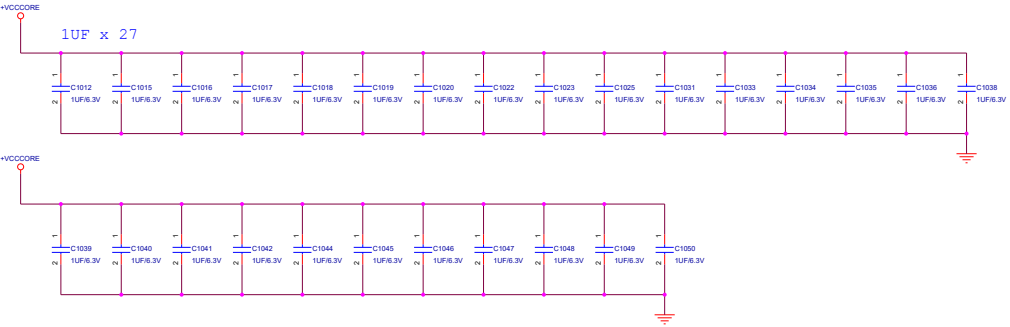
temp_M08_000010層名順序是：TOP/GND/IN1/GND1/IN2/VCC/GND2/IN3/GND3/BOTTOM

HALL SENSOR

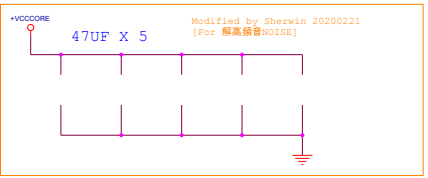


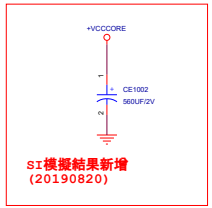
+VCCORE DECAPS Place Back Side (TOP)



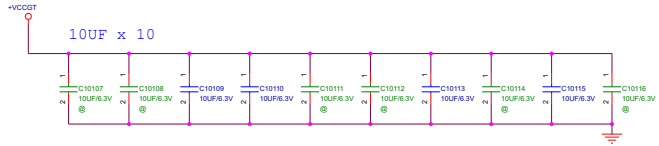


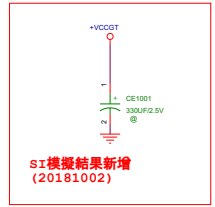
+VCCORE near CPU

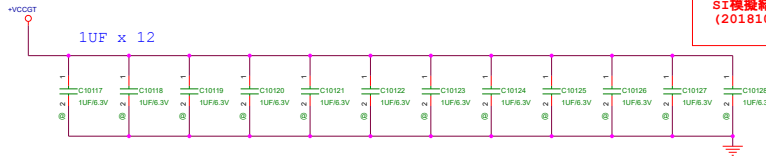




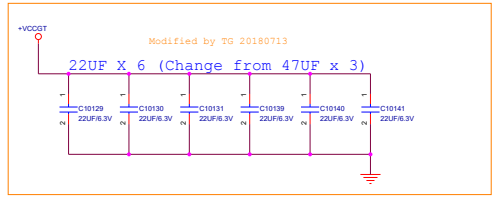
+VCCGT DECAPS Place Back Side (TOP)

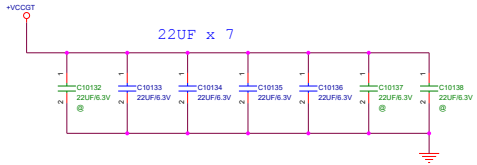






+VCCGTX near CPU





Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
Vcc_{GT}	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	

Project Name	GX502GX	Rev R1.2
Title :	010_CPU_POWER_CAP	
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, February 21, 2020	Sheet 10 of 99	

TBT PORTS

DP

PCIe

MISC & DEBUG

GND

Support RTD3

Support RTD3 -\/TBT/HR RTD3 mount, /TBT/HR unmount
NO Support RTD3 -\/TBT/HR mount,/TBT/HR RTD3 unmount

BOM修改為TR RT料號
(P/N:06118-00050200/06118-00050300)

+3VA_DSW確認OK

Review suggest Note:VCCST1.05
power connection to +3VALW

Project Name:	DesignZP
Title :	TBT TBT/C_DP R0.0a
Engineer:	BBT_MB3
Date:	Sheet: of

<Core Design>

Title : DDR4_TERMINATION

ASUSTeK COMPUTER INC.

Engineer: EE

Size	Project Name	Rev
A	GX502GX	R1.2

Date:	Friday, February 21, 2020	Sheet	13	of	99

SPK Power

AC_BAT_SYS — R3901 1 2 @ 0603 — R3931 1 2 @ 0603 — +PVDD_AMP

IO Power

+1.8VSUS — R3907 1 2 @ 0Ohm — +1.8V_3.3V_IOVDD

+3VSUS — R3921 1 2 0Ohm — +1.8V_3.3V_IOVDD

0926 Modify

5mA

+1.8V_3.3V_IOVDD — C3907 1 2 1UF/6.3V — GND

INTERNAL SPK1 Conn.

SPK L+ L- R+ R- trace width
Speaker 8 ohm
Max = 1.5W / Channel
I = 0.43 A

(Smart AMP MAX 2A/Channel) ==> 60mils

	J3901
ADR_AMP	4
H_SPKL-_CON	3
H_SPKL+_CON	2
H_SPKR-_CON	1
H_SPKR+_CON	

J3901: 6 SIDE2 8; 5 4 3 2 1; SIDE1 7

WTOB_CON_6P

12017-00011400

GND

+PVDD_AMP

C3903 1 2 22UF/25V
C3904 1 2 22UF/25V
C3905 1 2 0.1UF/50V
GND

+1.8V_3.3V_IOVDD

C3911 1 2 4.7UF/10V
C3910 1 2 0.1UF/16V
GND GND

C3947 2 1 0.22UF/50V — H_SPKL- — H_SPKL- — GND
C3944 2 1 0.22UF/50V — H_SPKR- — H_SPKR- — GND

C3938 2 1 0.22UF/50V — H_SPKL+ — H_SPKL+

C3939 2 1 1UF/16V
R3913 2 1KOHM 1 ADR_AMP
GND GND

U3905A

BST_A+	1	33	GND1
OUT_A+	2	32	PGND4
PVDD1	3	31	PGND3
PVDD2	4	30	OUT_A-
DGND	5	29	BST_A-
DVDD	6	28	BST_B-
VR_DIG	7	27	OUT_B-
ADR	8	26	PGND2
		25	PGND1

BST_B+	24	9	GPIO0
OUT_B+	23	10	GPIO1
PVDD4	22	11	GPIO2
PVDD3	21	12	LRCLK
AGND	20	13	SCLK
AVDD	19	14	SDIN
GVDD	18	15	SDA
PDN#	17	16	SCL

C3946 2 1 0.22UF/50V — H_SPKR+ — H_SPKR+

C3942 2 1 1UF/16V
C3943 2 1 1UF/16V

TAS5825MRHBR

06040-01420000

+1.8V_3.3V_IOVDD
R3924 @ 2 10KOhm 1 AMP_GPIO0
R3925 @ 2 10KOhm 1 AMP_GPIO2

[36] I2S_Codec_SDIN — I2S_Codec_SDIN
[36] I2S_LRCLK — I2S_LRCLK
[36] I2S_BCLK — I2S_BCLK
[36] I2S_Codec_SDOUT — I2S_Codec_SDOUT

SMB3_CLK_AMP — SMB3_CLK_AMP [28]
SMB3_DAT_AMP — SMB3_DAT_AMP [28]

+PVDD_AMP

C3945 1 2 0.1UF/50V
C3914 1 2 22UF/25V
C3912 1 2 22UF/25V
GND

+1.8V_3.3V_IOVDD
R3930 2 1 10KOhm
R3902 1 2 0Ohm — AMP_PDN# — REST_AMP# [30]
GND

C3948 1 2 0.1UF/16V @
GND

U3905B

34	GND2
35	GND3
36	GND4
37	GND5
38	GND6
39	GND7
40	GND8
41	GND9
42	GND10
43	GND11
44	GND12
45	GND13
46	GND14

GND — TAS5825MRHBR

0926 Change for additional 13 VIA

I2C Address Table

	ADR_AMP(SPK)	Address 8bit
Main(N.C.)	Open	0x9A
Second	Short	0x98

SPK Output

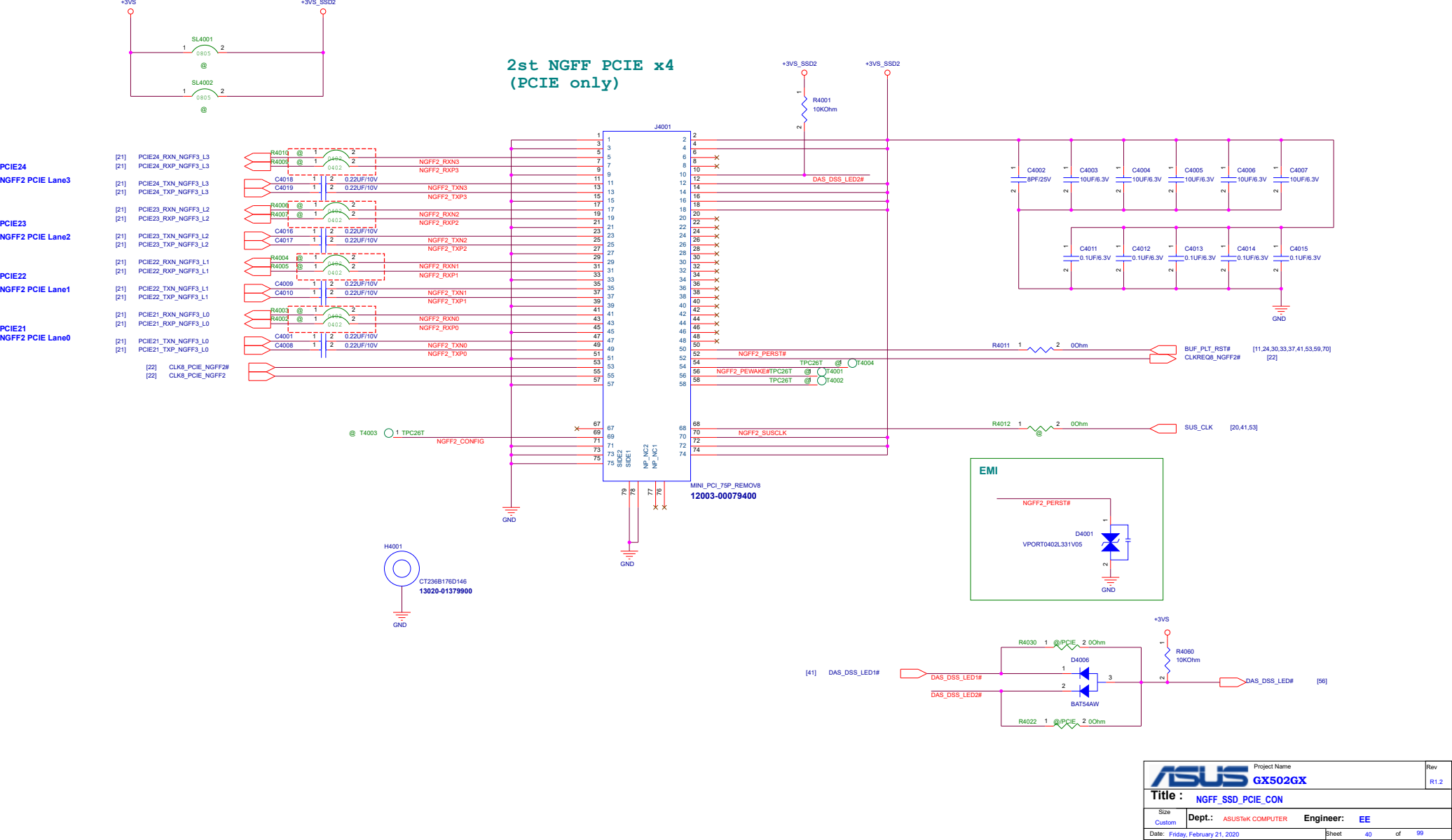
H_SPKL- — L3901 1 2 30Ohm/100Mhz — H_SPKL-_CON
D3903 AZ4024-01F @
C3915 1000PF/50V
GND GND

H_SPKR- — L3902 1 2 30Ohm/100Mhz — H_SPKR-_CON
D3904 AZ4024-01F @
C3919 1000PF/50V
GND GND

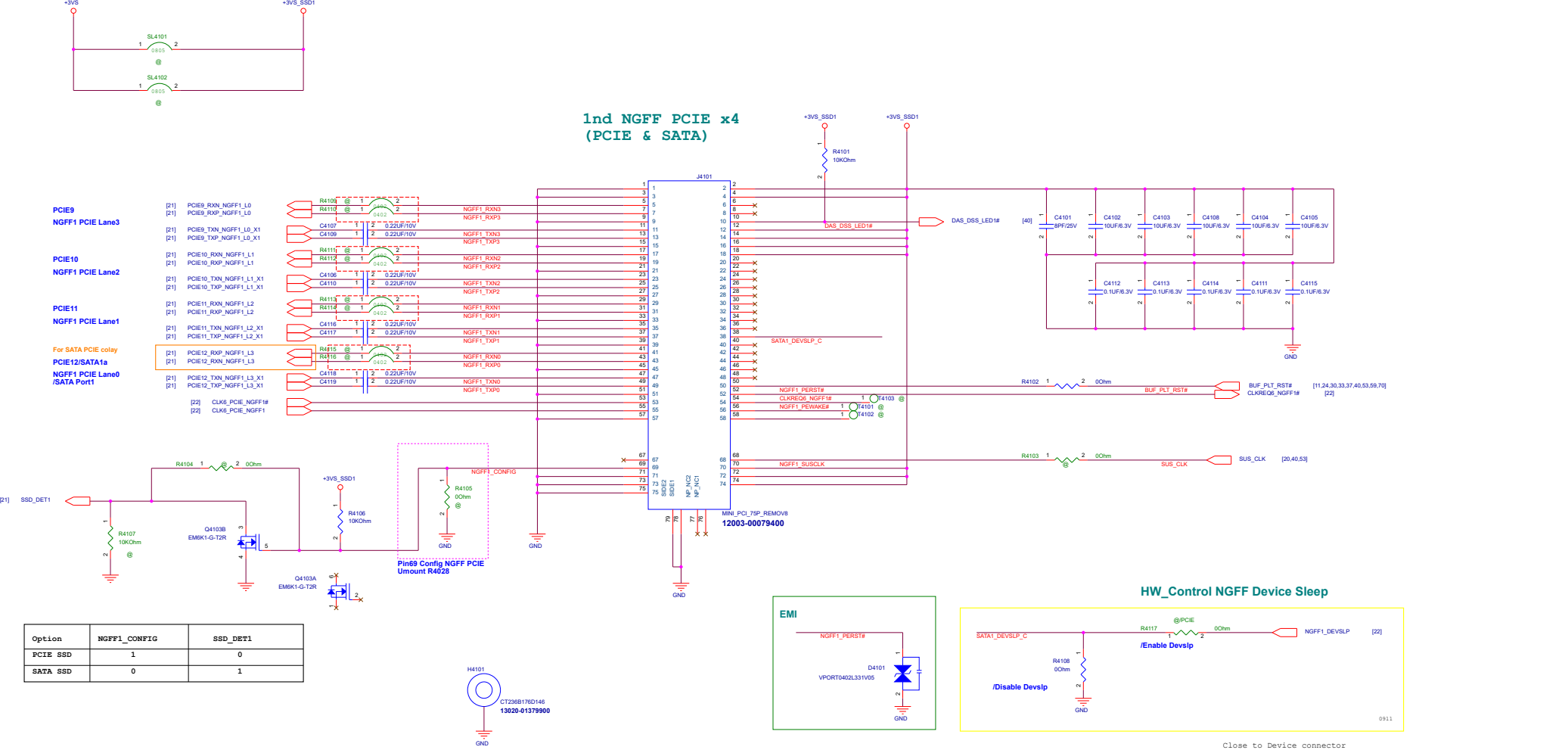
H_SPKL+ — L3903 1 2 30Ohm/100Mhz — H_SPKL+_CON
D3905 AZ4024-01F @
C3917 1000PF/50V
GND GND

H_SPKR+ — L3904 1 2 30Ohm/100Mhz — H_SPKR+_CON
D3906 AZ4024-01F @
C3921 1000PF/50V
GND GND

ASUS	Project Name: GX502GX	Rev: R1.2
Title : AUD_INT SPK		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Friday, February 21, 2020	Sheet 39 of 99	



Project Name	GX502GX
Rev	R1.2
Title :	NGFF_SSD_PCIE_CON
Size	Custom
Dept.:	ASUSTeK COMPUTER
Engineer:	EE
Date:	Friday, February 21, 2020
Sheet	40 of 99



Option	NGFF1_CONFIG	SSD_DET1
PCIE SSD	1	0
SATA SSD	0	1

<Core Design>

ASUSTeK COMPUTER	Title : NGFF_SSD_CPU	
	Engineer: EE	
Size: Custom	Project Name: GX502GX	Rev: R1.2
Date: Friday, February 21, 2020	Sheet 41 of 99	

<Core Design>

Title : XDD_HDD & ODD CON

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	GX502GX	R1.2

Date:	Friday, February 21, 2020	Sheet	42	of	99

Project Name

GX502GX

Rev

R1.2

Title : CB_CON

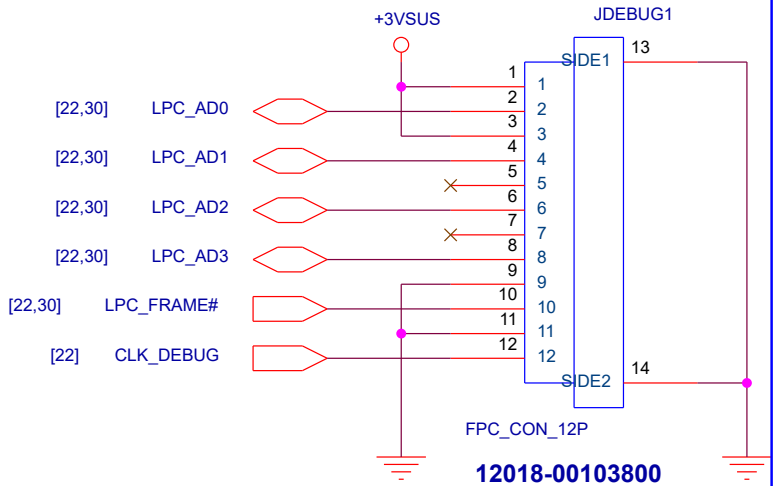
Size	Dept.:	Engineer:
A	ASUSTeK COMPUTER	EE

Date: Friday, February 21, 2020

Sheet 43 of 99

LPC Debug Port

2017/11/10



12018-00103800

/PR_Remove

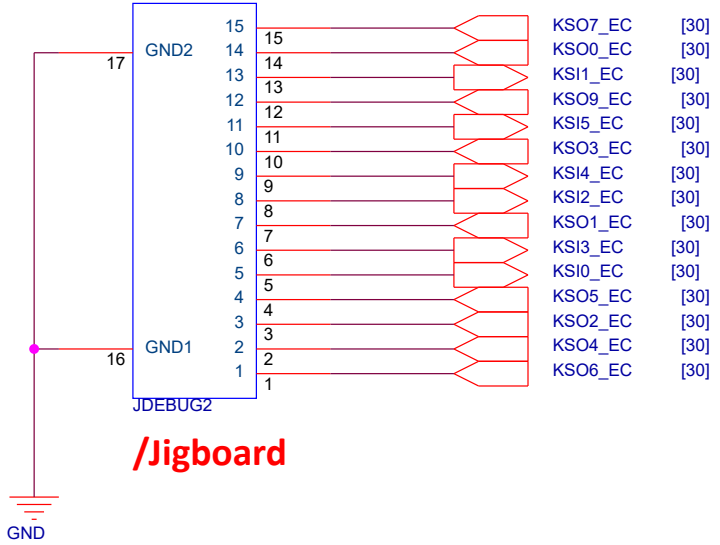
1st: 12018-00103800
2nd :12018-00103300

2017/11/10

Flash BIOS

12018-00390900

FPC_CON_15P



/Jigboard

<Core Design>

ASUSTeK COMPUTER	Title : DEBUG_LPC	
	Engineer: EE	
Size: A	Project Name: GX502GX	Rev: R1.2
Date: Friday, February 21, 2020	Sheet 44 of 99	

<Core Design>

Title : USB3_*****

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
B	GX502GX	R1.2

Date:	Friday, February 21, 2020	Sheet	46	of	99

<Core Design>

Title : TYPE-C USB3.1_R1.5_4

ASUSTeK COMPUTER INC. NB1

Engineer:

Size	Project Name	Rev
D	**GX502GX**	R1.2

Date:	Friday, February 21, 2020	Sheet	47	of	99

Main Board

HDMI Active-Level Shift

Modify (20181018)

to GPU

From GPU

Q4801只用07005-00660200與07005-00950000

06106-00390100

SN75DP159RSBT

HDMI PWR_+5VS_HDMI

Remove SL4802 (20180927)

HDMI Conn.

HDMI_CON_19P

12022-00130800

HDMI EMI

HDMI LDO 1.1VS

Imax = 0.35A

Imax = 0.35A

Slew rate control when I2C_EN/PIN = Low.
SLEW_CTL = H, fastest data rate
SLEW_CTL = L, 5 ps slow
SLEW_CTL = No Connect, 10 ps slow

HDMI_SEL when I2C_EN/PIN = Low
HDMI_SEL = High: Device configured for DVI
HDMI_SEL = Low: Device configured for HDMI

Input Receive Equalization pin strap when I2C_EN/PIN = Low
EQ_SEL = L: Fixed EQ at 7.5 dB
EQ_SEL = No Connect: Adaptive EQ
EQ_SEL = H: Fixed at 14 dB

De-emphasis pin strap when I2C_EN/PIN = Low.
PRE_SEL = L: - 2 dB de-emphasis level
PRE_SEL = No Connect: 0 dB
PRE_SEL = H: Reserved

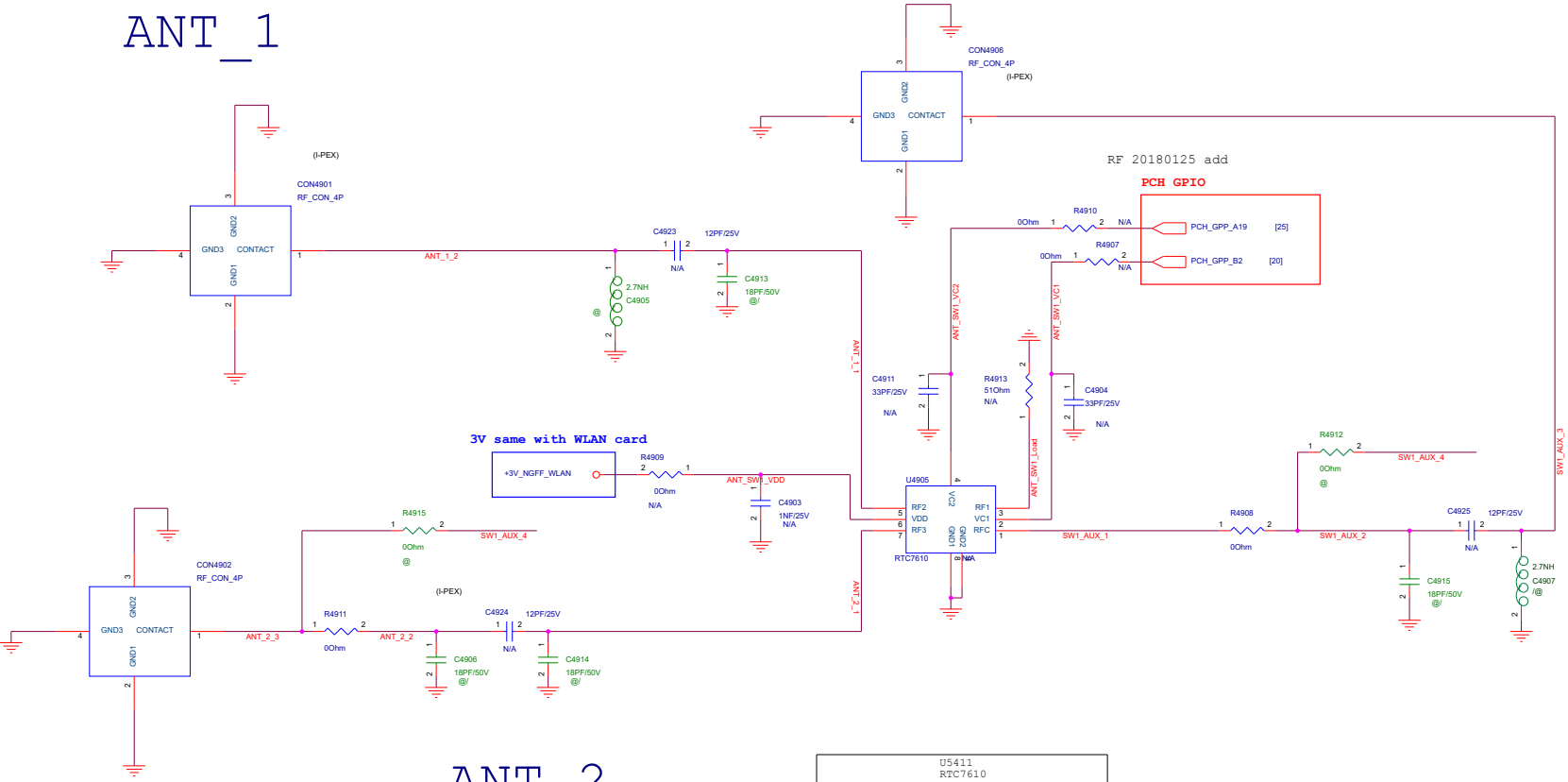
I2C_EN/PIN = High; puts device into I2C control mode
I2C_EN/PIN = Low; puts device into pin strap mode

Operation enable/reset pin
OE = L: Power-down mode OE = H: Normal operation
Internal weak pullup: Resets device when transitions from H to L

Project Name: Design IP			Rev: 0.1B
Title : HDMI ReTimer_Revision History_R0.1B			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, February 21, 2020	Sheet 48 of 99		

Module_AUX

ANT_1



ANT_2

U5411 RTC7610			
		VC1	VC2
ANT	Port	GPP_B2	GPP_A19
50 Ω	RF1	1	0
ANT_1	RF2	X	1
ANT_2	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

<Core Design>

ASUS	Project Name: GX502GX	Rev: R1.2
Title : ANT		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, February 21, 2020	Sheet 49 of 99	

Main Board

Thermal Sensor : SN170027

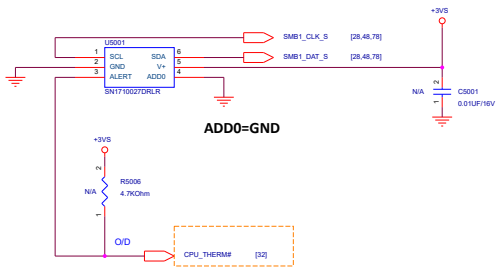
power rail : 3.3V

SMBUS1 to EC

ALERT/SDA/SCL: Open-drain output; pullup resistor 5Kohm

Pin function Supply voltage.: 1.62 V to 3.6 V

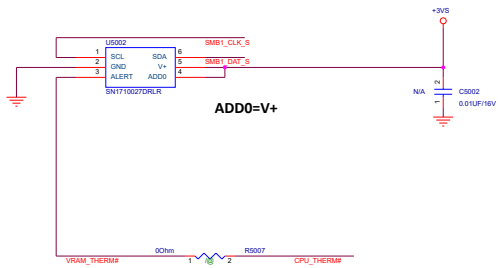
CPU



Near CPU

SMBUS addr=10010000 (90)

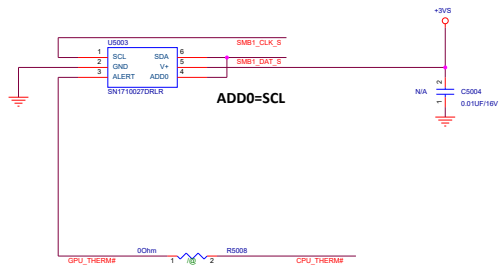
VRAM



Near VRAM

SMBUS addr=10010001 (92)

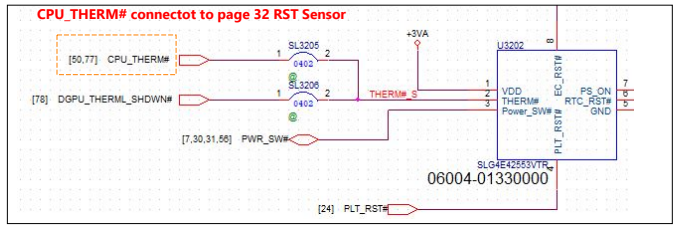
GPU



Near GPU

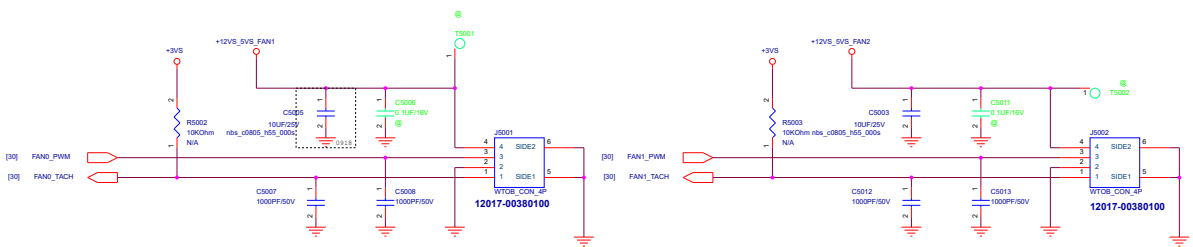
SMBUS addr=1001011 (96)

example



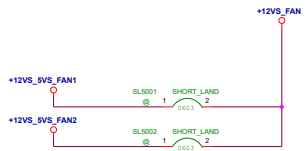
CPU&GPU FAN

Note : connector and power are by project design



ADD0: Address select. Connect to GND, SDA, SCL, or V+

DEVICE TWO-WIRE ADDRESS	ADD0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL



<Variant Name>

Title : Thermal Sensor

ASUSTeK COMPUTER INC. NB1

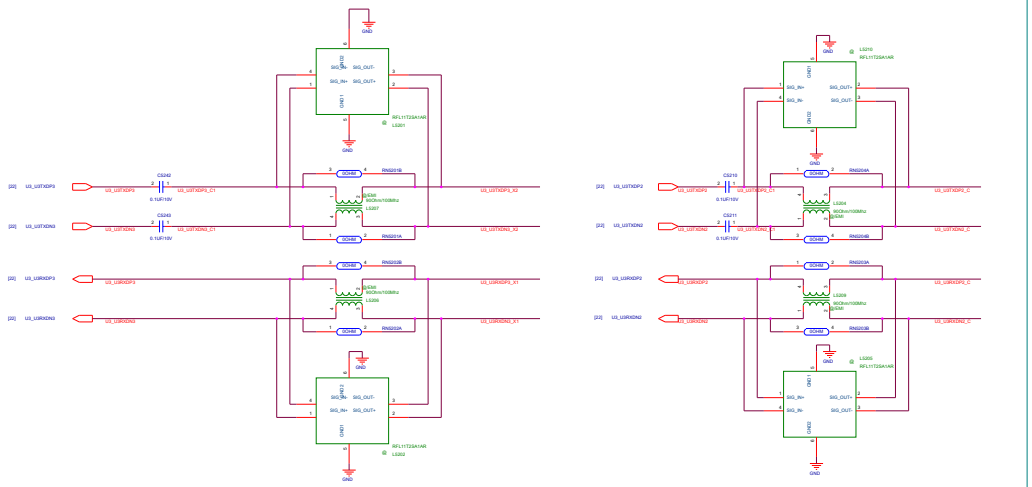
Engineer: EE

Size: Custom | Project Name: thermal sensor & fan | Rev: R1.0

Date: Friday, February 21, 2020 | Sheet 50 of 103

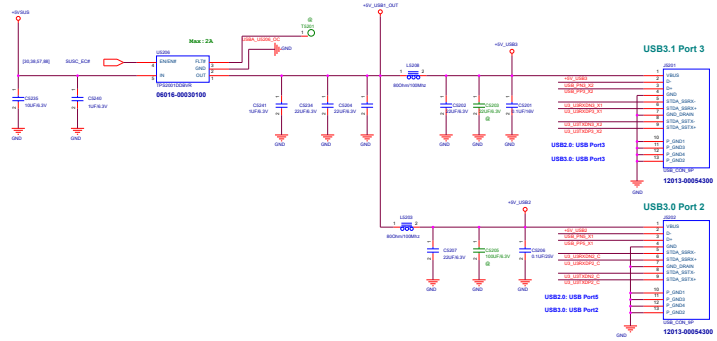
TYPE-C USB3.1

USB3.0 EMI-Protection



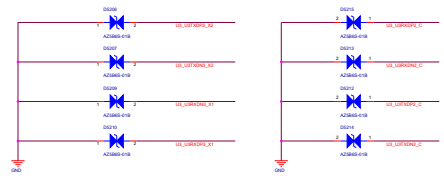
5.PIN DEFINE TABLE:

PIN NO.	1	2	3	4		
SIGNAL NAME	VBUS	D-	D+	GND		
PIN NO.	5		6	7	8	9
SIGNAL NAME	StdA_SSRX-		StdA_SSRX+	GND-DRAIN	StdA_SSTX-	StdA_SSTX+



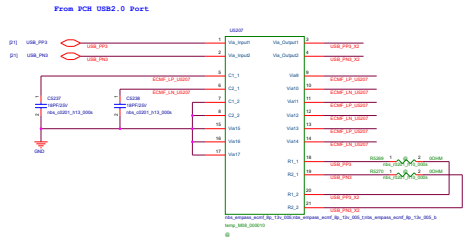
USB3.0 ESD-Protection

1st Source: P/N:07024-01360000 ESD PROTECTION AZ5865-01B



For EMI, Eason 2018/8/24

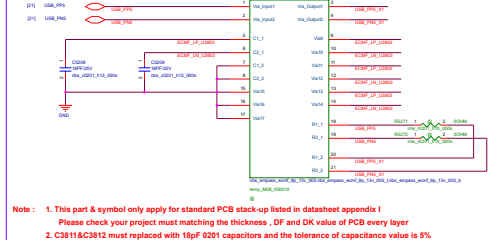
R1.5 USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)



Note : 1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
2. C5237&C5238 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
4. Pin13 to Pin16 are floated in regular scheme

temp_M08_000010層名順序是：TOP/GND/IN1/GND1/IN2/VCC/GND2/IN3/GND3/BOTTOM

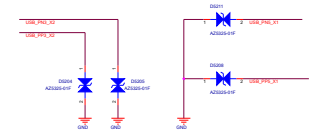
R1.5 USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)



Note : 1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
2. C3811&C3812 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
4. Pin13 to Pin16 are floated in regular scheme

temp_M08_000010層名順序是：TOP/GND/IN1/GND1/IN2/VCC/GND2/IN3/GND3/BOTTOM

USB2.0 ESD-Protection



For EMI, Eason 2018/8/24

Title <Title>		
Size A	Document Number <Doc>	Rev R1.2
Date: Friday, February 21, 2020	Sheet 54 of 99	

<Core Design>

Title : IO Con. to MB

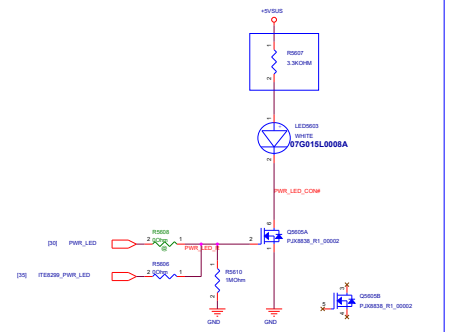
ASUSTeK COMPUTER

Engineer: EE

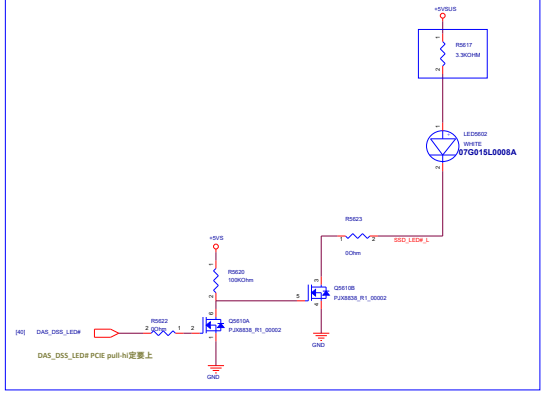
Size	Project Name	Rev
A	**GX502GX**	R1.2

Date:	Friday, February 21, 2020	Sheet	55	of	99

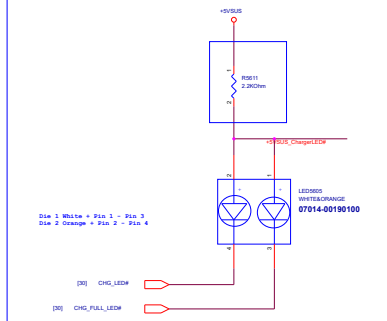
PWR LED



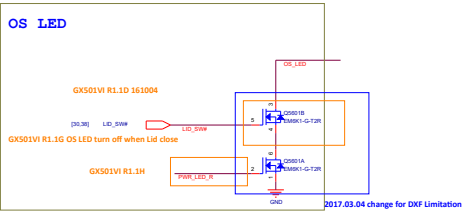
PCIE SSD LED

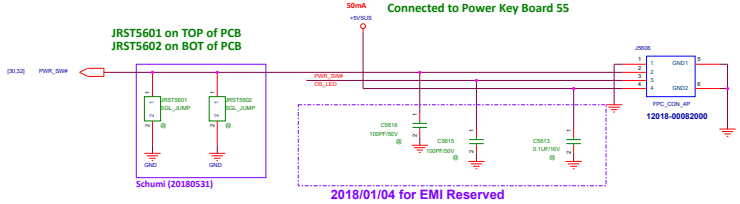


Charger LED



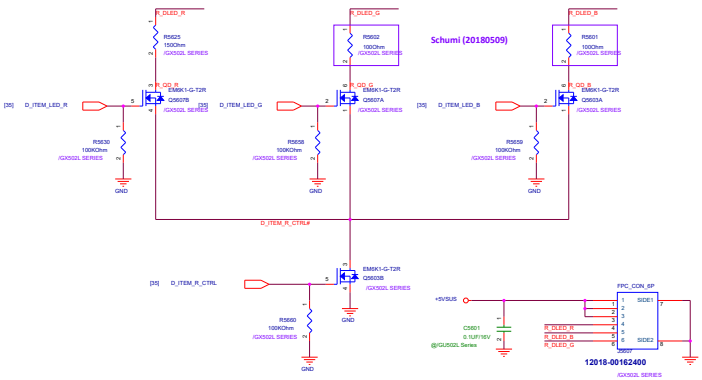
OS LED



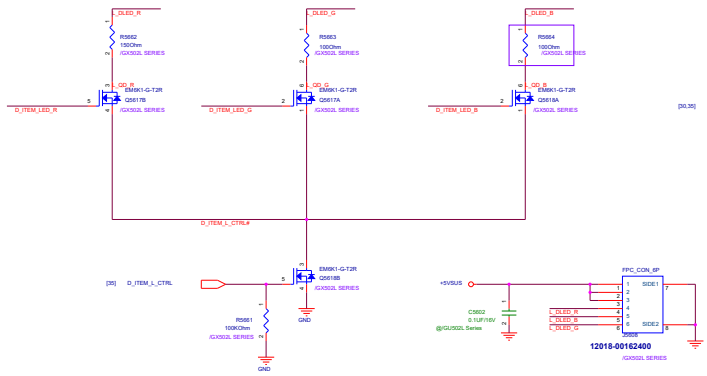


D item- RGB LED

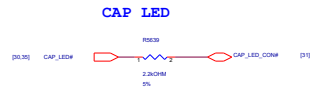
< D case LED R >

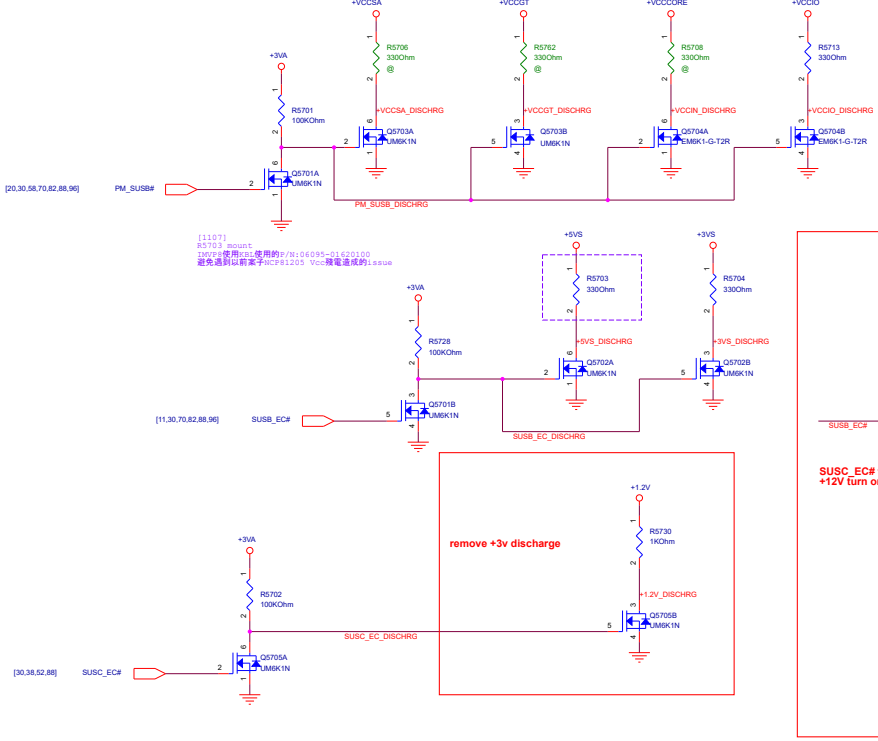


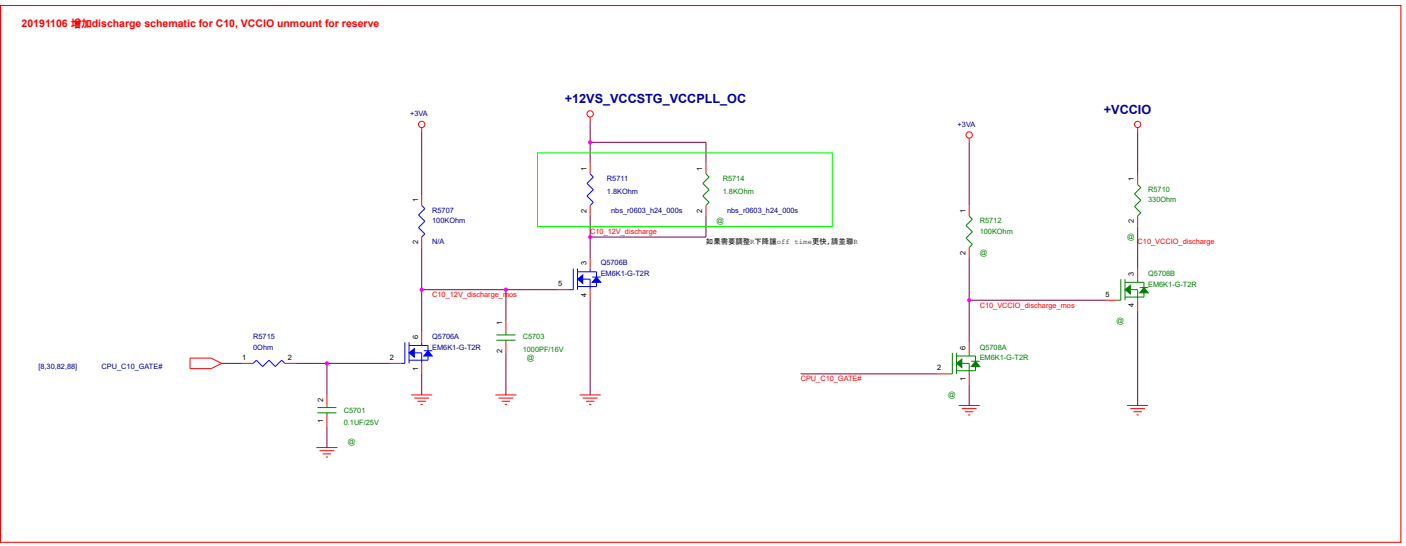
< D case LED L >

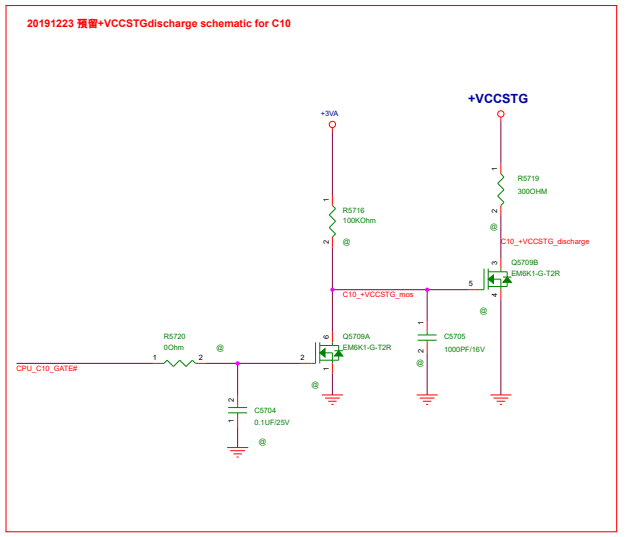


CAP LED







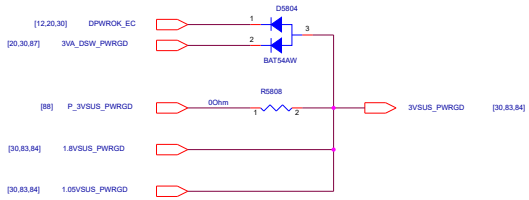


<Core Design>

ASUSTeK COMPUTER	Title : DSG_Discharge	
	Engineer: EE	
Size: C	Project Name: GX502GX	Rev: R1.2
Date: Friday, February 21, 2020	Sheet 57 of 99	

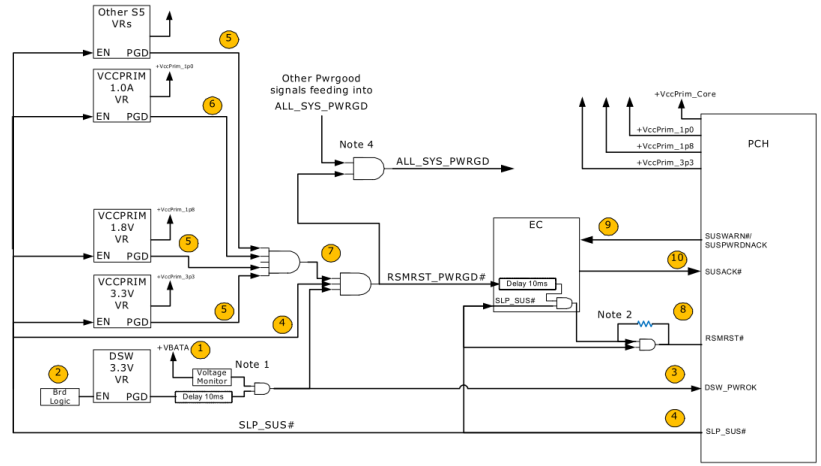
[SUS_VR_PWRGD]

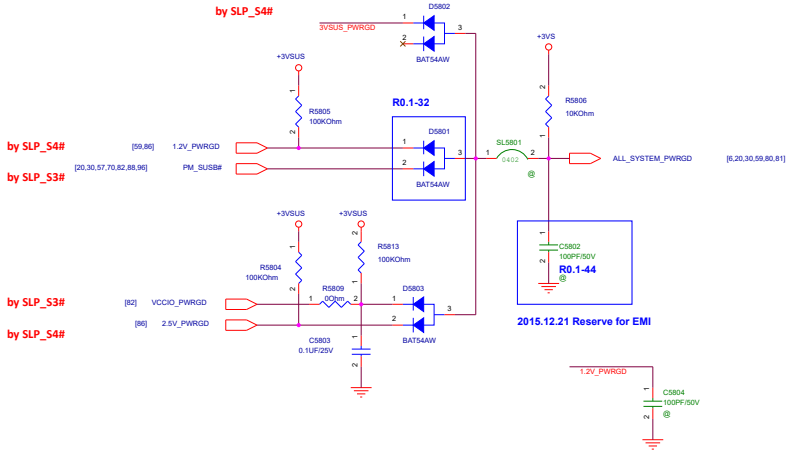
SLP_SUS_N
V0.85_PWRGD
V3.3A_V5A_PWRGD
V1.0A_PWRGD
V1.8A_PWRGD
DPWROK=3.3A_DSWPWRGD+10ms & BATT>5.35V

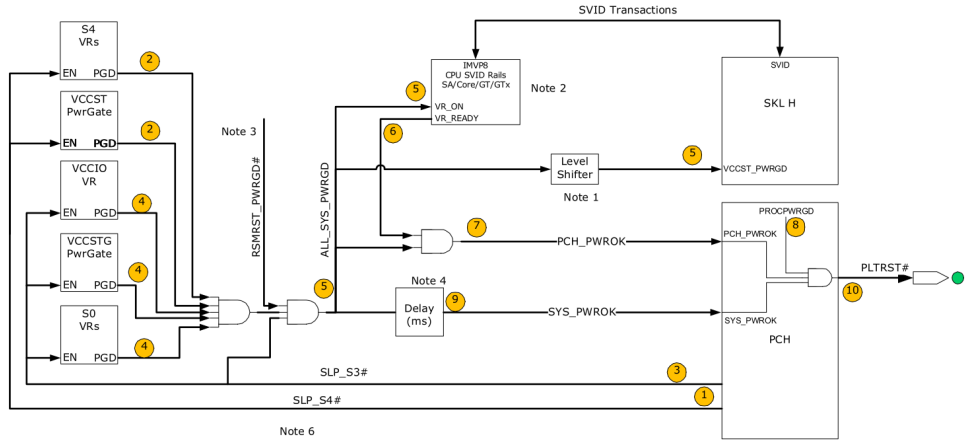


[ALL_SYSTEM_PWRGD]

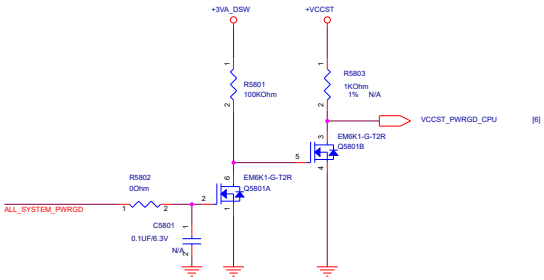
SLP_S3_N
DDR_PWRGD
VCCIO_PWRGD
3.3S_MON
1.00U_MON
1.8S_MON
RSMRST_PWRGD
SYS_PWROK







[VCCST_PWRGD for PCH]



EMI SPRING (2.6H)*3 13NB0I50M01011

EMI SPRING (4.2H)*2 13NK00B1M01011

EMI SPRING (3.5H)*1 13GOK0F10M010-10

U5902 SMD120X93 13NB0I50M01011 GND

U5904 SMD120X93 13NB0I50M01011 GND

U5901 SMD120X93 13NB0I50M01011 GND

U5903 SMD148X73 13NK00B1M01011 GND

U5906 SMD128X43 13GOK0F10M010-10 GND

U5905 SMD148X73 13NK00B1M01011 GND

+3VA

D5903 AZ5325-01F @ GND

D5901 AZ5325-01F GND

D5902 AZ5325-01F GND

P_SMB0_CLK [28,30,60,89,90]

P_SMB0_DAT [28,30,60,89,90]

AC_BAT_SYS

C5932 0.1UF/25V

C5906 0.1UF/25V

C5920 0.1UF/25V

GND

AC_BAT_SYS

C5926 0.1UF/25V @

C5919 0.1UF/25V @

C5912 0.1UF/25V @

C5942 0.1UF/25V @

C5922 0.1UF/25V

C5925 0.1UF/25V

C5928 0.1UF/25V

C5934 0.1UF/25V

C5939 0.1UF/25V

C5944 0.1UF/25V

C5930 0.1UF/25V

C5908 0.1UF/25V

C5914 0.1UF/25V

C5917 0.1UF/25V

C5924 0.1UF/25V

GND

2018.12.18 EMI Need

G_PWR_SRC_NVVDD

C5943 0.1UF/25V

GND

G_PWR_SRC_NVVDD

C5909 2.2UF/25V

C5903 2.2UF/25V

GND

+NVVDD

C5904 10PF/50V @

C5915 10PF/50V @

C5902 10PF/50V @

GND

AC_BAT_SYS

C5923 0.1UF/25V

C5918 0.1UF/25V

C5937 0.1UF/25V @

C5931 0.1UF/25V

C5933 0.1UF/25V

C5929 0.1UF/25V

C5941 0.1UF/25V

C5921 0.1UF/25V

C5935 0.1UF/25V

C5913 0.1UF/25V

C5927 0.1UF/25V @

C5940 0.1UF/25V

GND

+3VA

C5916 10PF/50V @

C5907 10PF/50V @

C5911 10PF/50V @

GND

2018.11.19 EMI Reserve

[58,86] 1.2V_PWRGD

[11,24,30,33,37,40,41,53,70] BUF_PLT_RST#

[20,30,80] IMVP8_PWRGD

[6,20,30,58,80,81] ALL_SYSTEM_PWRGD

C5936 100PF/50V @

C5938 100PF/50V @

C5901 100PF/50V

C5905 100PF/50V

GND

+5VS_PWR

C5910 10PF/50V @

GND

2017.05.02 EMI Reserve

<Core Design>

ASUSTeK COMPUTER

Title : I/O_Main board Conn.

Engineer: EE

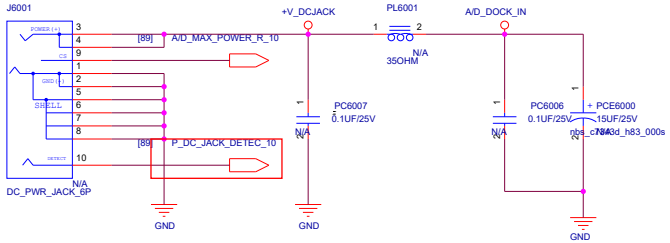
Size	Project Name	Rev
B	GX502GX	R1.2

Date: Friday, February 21, 2020 Sheet 59 of 99

DC-IN Connector

DC Jack使用請詢用River_Hsu

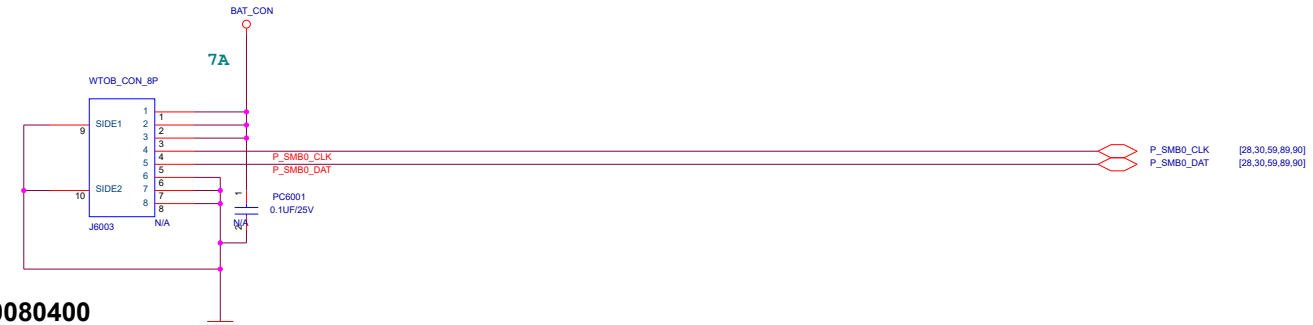
New 6 Phi 4 Pin DC_Jack 1.55ch



12033-00020300

J6001	3.4CH	1.55CH
	12033-00020200	12033-00020300

Battery Connector



12017-00080400

Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

Project Name: GX502GX			Rev: R1.2
Title : DC & BAT IN			
Size: A3	Dept.: NB_Power team	Engineer: Benson	
Date: Friday, February 21, 2020	Sheet 60 of 99		

<Core Design>

Title : I/O board(1-1)_CR_RTS5139

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	GX502GX	R1.2

Date:	Friday, February 21, 2020	Sheet	62	of	99

<Core Design>

Title : USB Port

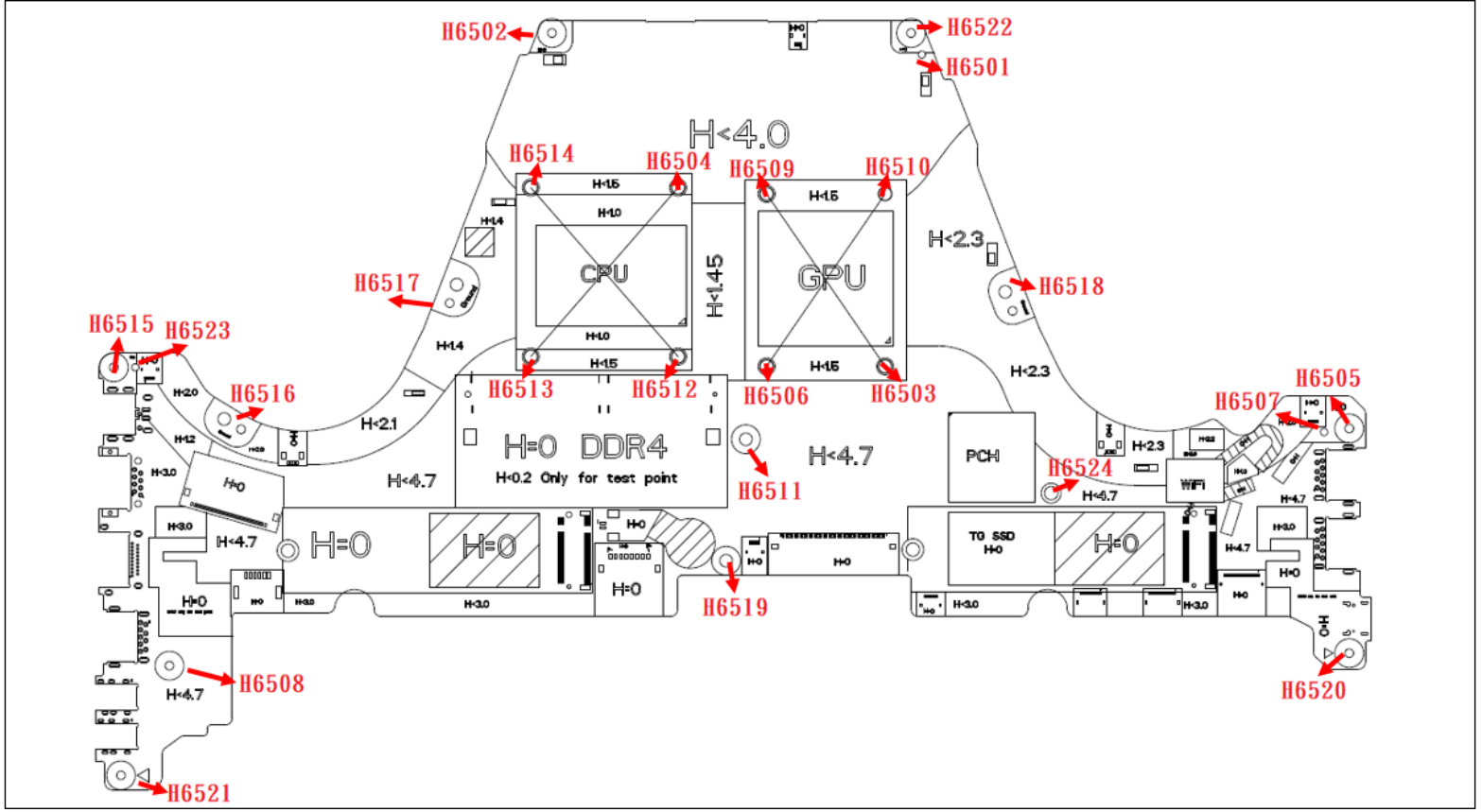
ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	GX502GX	R1.2

Date:	Friday, February 21, 2020	Sheet	63	of	99

ASUSTeK COMPUTER	Title : I/O board(1-3)_USB	
	Engineer: EE	
Size: A	Project Name: GX502GX	Rev: R1.2
Date: Friday, February 21, 2020	Sheet 64 of 69	



GPU

TOP 3.7/6.5, BOT 3.7/4.7

H6503 1 @ CT256CB185D146

H6510 1 @ C146D146N

H6509 1 @ CT256CB185D146

H6506 1 @ CT256CB185D146

CPU

TOP 3.7/6.5, BOT 3.7/4.7

H6504 1 @ CT256CB185D146

H6512 1 @ CT256CB185D146

H6514 1 @ CT256CB185D146

H6513 1 @ CT256CB185D146

PCH

H6524

CT236B176D146

13020-04421400

GND

TOP&BOT 2.4/8

GND 1 H6502 C315D94 @

GND 1 H6522 C315D94 @

1 H6501 C79D79N @

不裸銅NPTH

TOP&BOT 3.5/8

GND 1 H6519 C315D138 @

GND 1 H6511 C315D138 @

GND 1 H6515 C315D94 @

GND 1 H6508 C315D94 @

GND 1 H6521 C315D94 @

GND 1 H6505 C315D94 @

GND 1 H6520 C315D94 @

H6523

GND 1 NP_NC GND4 5 GND

GND 2 GND1 GND3 4 GND

3 GND2

CT236D79N

s12526

@

H6507

GND 1 NP_NC GND4 5 GND

GND 2 GND1 GND3 4 GND

3 GND2

CT236D79N

s12526

@

H6517

GND @ 1 2 GND

s12527

2D_D138_D94

H6518

GND @ 1 GND NP_NC 2

s12536

2D_D138_D94N

H6516

GND @ 1 2 GND

s12529

2D_D138_D94

<Core Design>

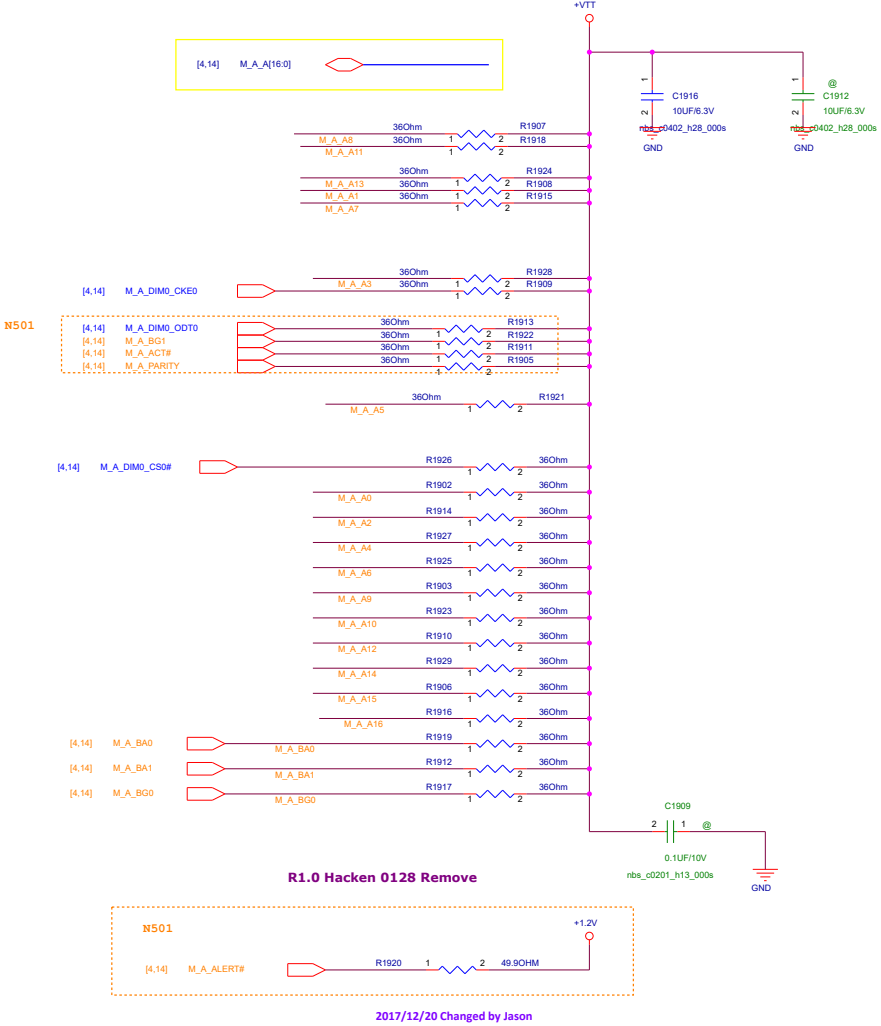
ASUSTeK COMPUTER

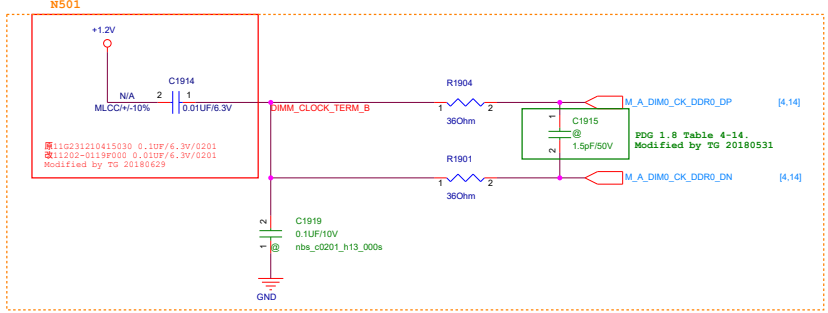
Title : ME_Screw Hole & Nut

Engineer: EE

Size	Project Name	Rev
B	GX502GX	R1.2

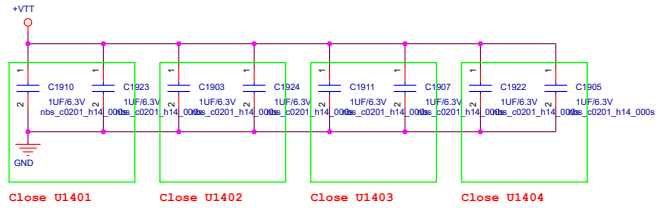
Date: Friday, February 21, 2020 Sheet 65 of 99

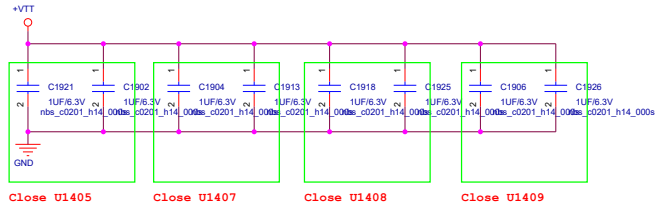




Clock Pull up power change from +0.6V to +1.2V (CFL PDG) 20820601

10uF*4
1uF*16





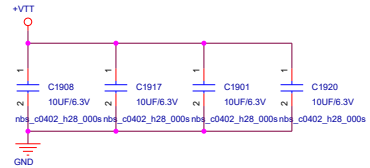
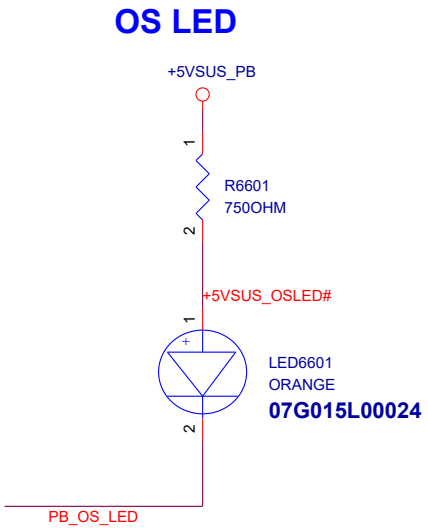


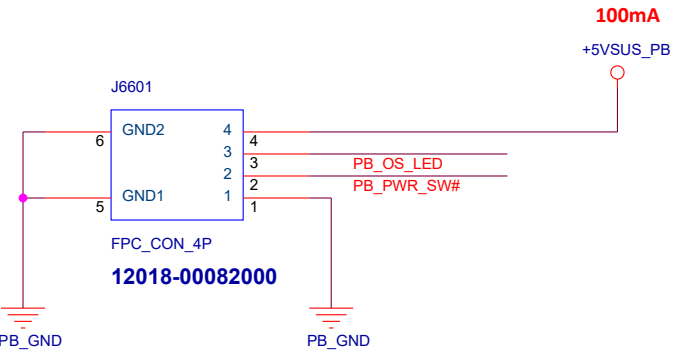
Table 4-25. DDR4 Memory Down Power Plane Decoupling

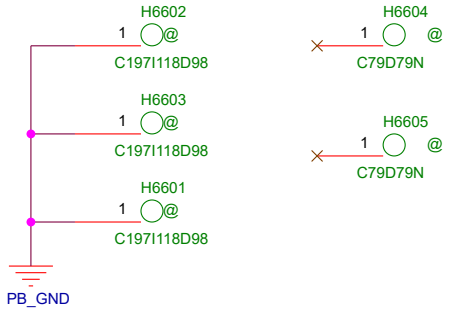
Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x8- 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x8 DRAM device as possible	64x 1µF (0402) (min of 48 stuffed)	
		Distributed around the DRAM devices	20x 10µF (0603) (min of 12 stuffed)	
	VPP	2 as near each x8 DRAM device as possible	32x 1µF (0402)	
		Distributed around the DRAM devices	10x 10µF (0603)	
	VTT	Distributed along termination resistors	32x 1µF (0402)	
		Distributed evenly across domain	8x 10µF (0603)	

Connected to MB Page56

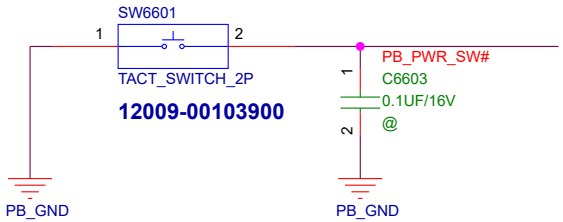
OS LED

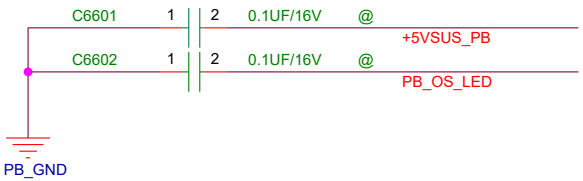


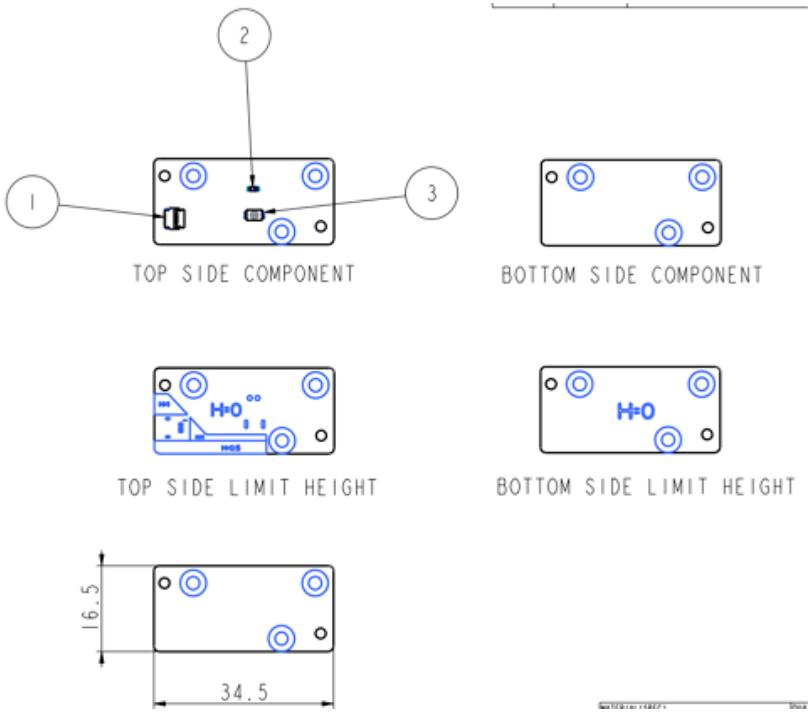




POWER button







<Core Design>

ASUSTeK COMPUTER	Title :	
	Engineer: EE	
Size: A	Project Name: GX502GX	Rev: R1.2
Date: Friday, February 21, 2020	Sheet 66 of 99	

<Core Design>

Title : I/O board FUNC key

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
B	**GX502GX**	R1.2

Date:	Friday, February 21, 2020	Sheet	67	of	99

<Core Design>

Title : OTH_for test only

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	**GX502GX**	R1.2

Date:	Friday, February 21, 2020	Sheet	68	of	99

Title : OTH_EMI

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	GX502GX	R1.2

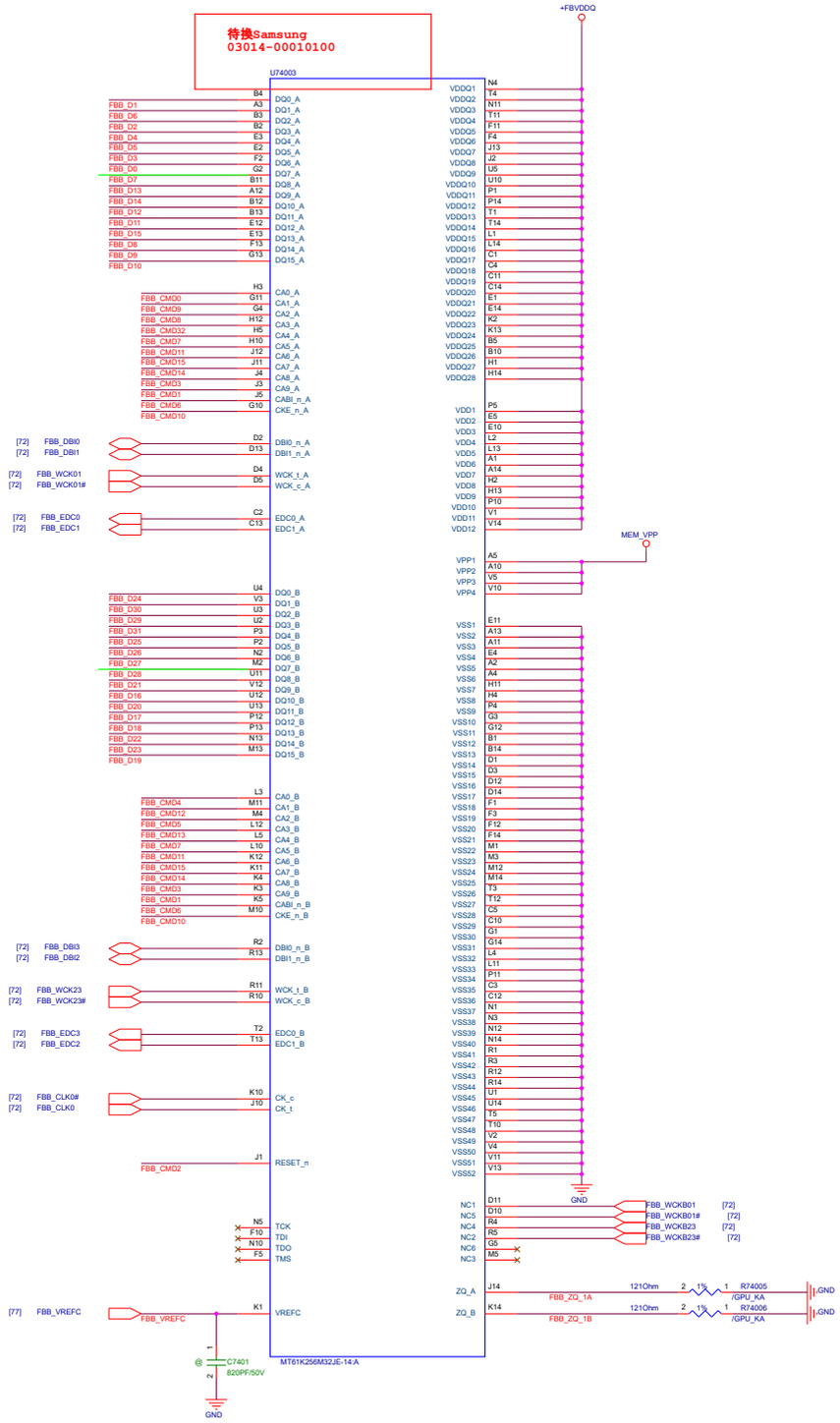
[72] FBB_D[31..0]

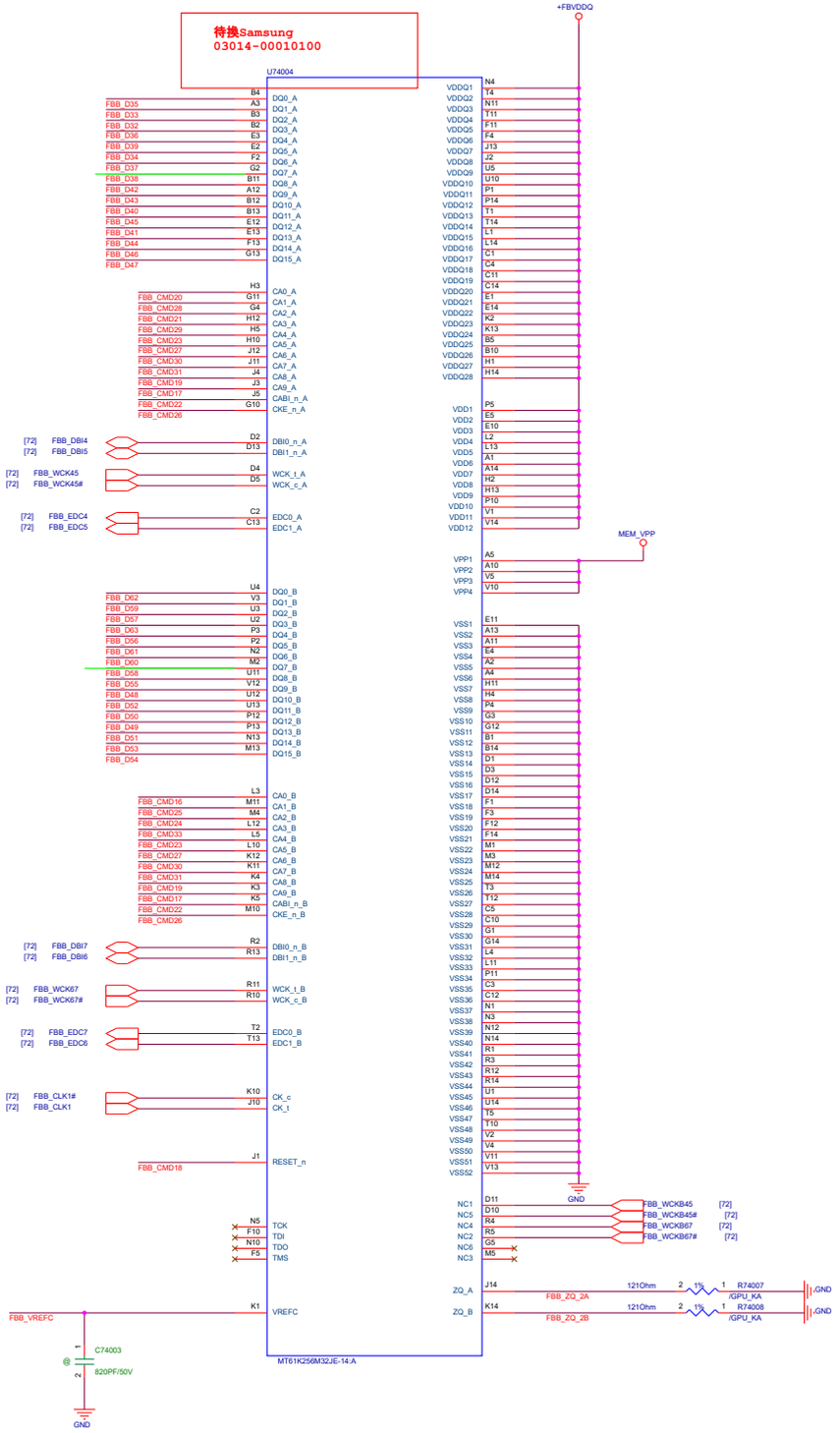
[72] FBB_CMD[33..0]

40 OHm_NET
FBB Partition 31..0
MF=1 Mirror

[72] FBB_D[63..32]

40 OHm_NET
FBB Partition 64..32
MF=0 Normal





Project Name: GX502GX				Rev: R1.2
Title: VRAM_Channel_B				
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:		
Date: Friday, February 21, 2020		Sheet 74 of 99		

[72] FBD_D[31..0]

[72] FBD_CMD[33..0]

40 OHm_NET
FBD_Partition 31..0
MF=1 Mirror

[72] FBD_D[63..32]

40 OHm_NET
FBDPartition 64..32
MF=0 Normal

待換Samsung
03014-00010100

U76003

+FBVDDQ

MEM_VPP

GND

MT61K256M32JE-14:A

C7601
820PF/50V
@/V6G

待換Samsung
03014-00010100

U76004

+FBVDDQ

MEM_VPP

GND

MT61K256M32JE-14:A

C76003
820PF/50V
@/V6G

Project Name	GX502GX		Rev R1.2
Title :	VRAM_Channel_D		
Size Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:	
Date: Friday, February 21, 2020	Sheet 76 of 99		

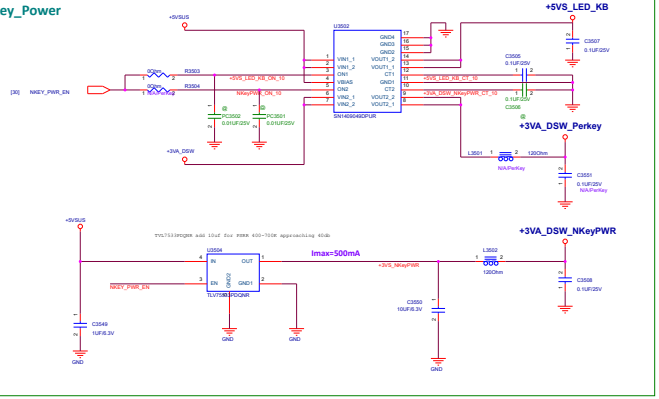
N_KEY_IT8299E

Nkey_Power_Cap

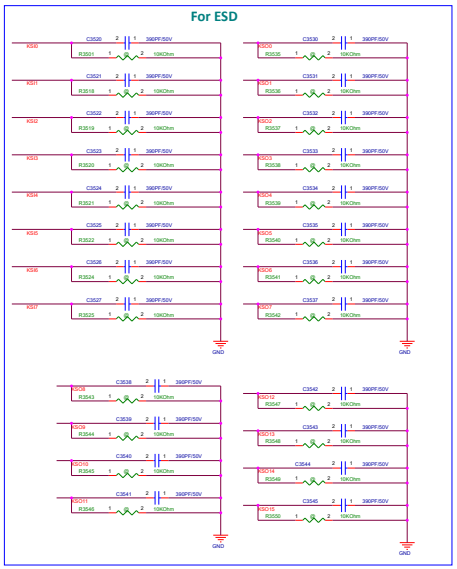
For EC Reset N_key

Pull up

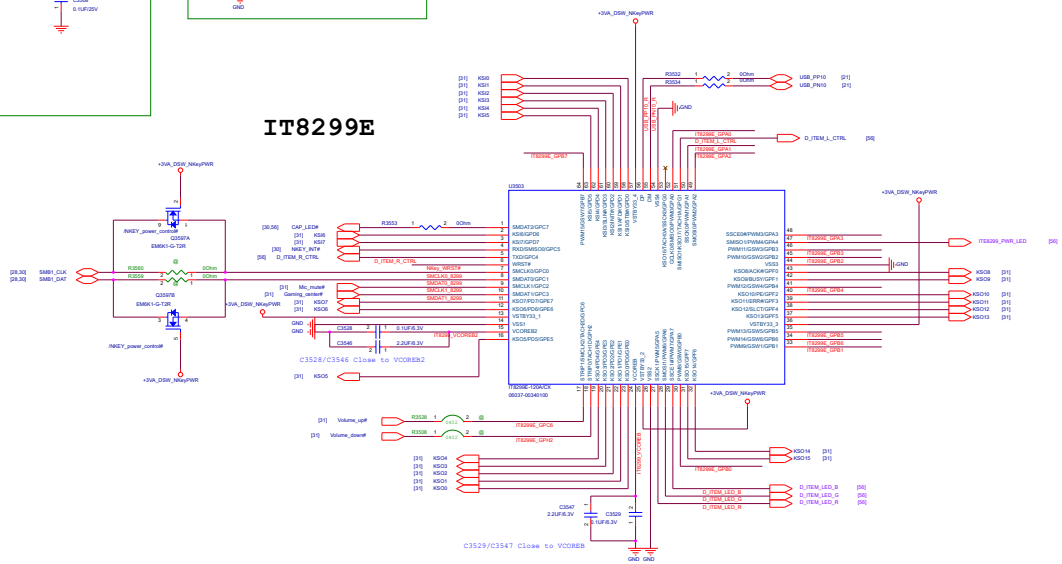
Nkey_Power



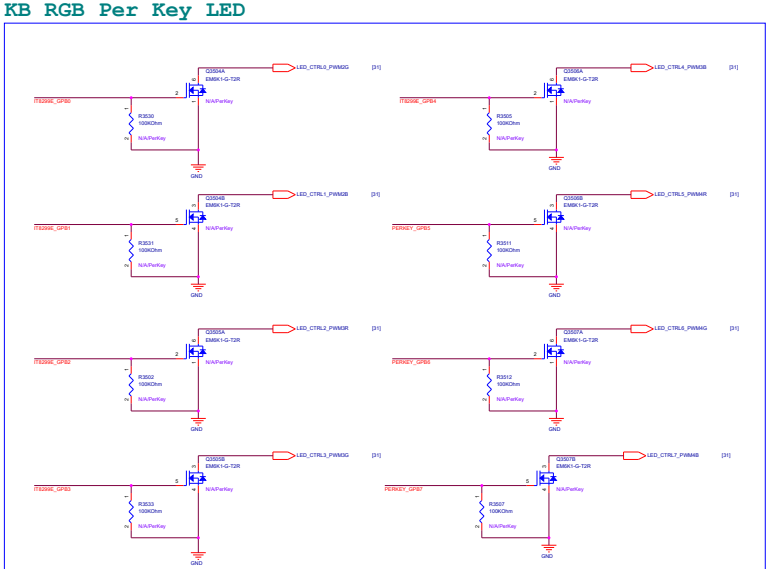
For ESD



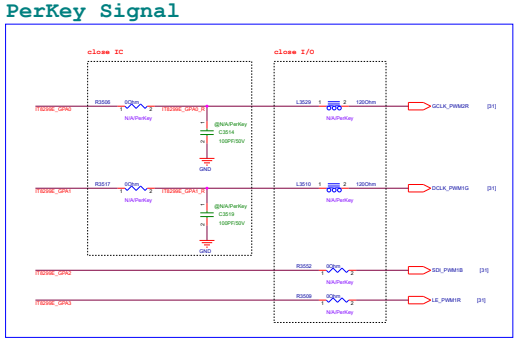
IT8299E



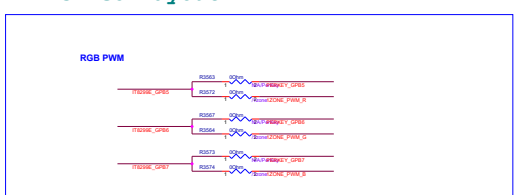
KB RGB Per Key LED



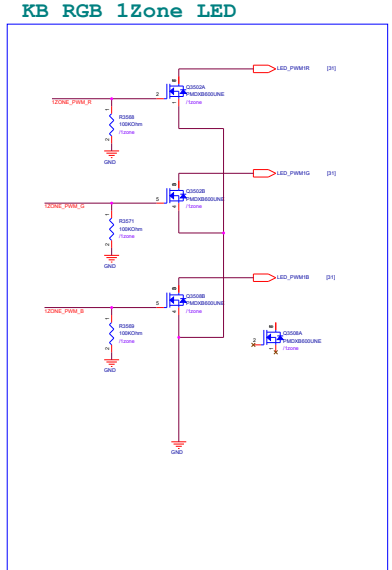
PerKey Signal



KB RGB co-layout



KB RGB 1Zone LED



Title :	LAN_*****		
Engineer:	EE		
Size	Project Name		Rev
Custom	GX502GX		R1.2
Date:	Friday, February 21, 2020	Sheet 35	of 103

Main Board

Headphone&MIC

A_GND / GND

C3709 2 1 0.1UF/16V
C3710 2 1 0.1UF/16V
C3708 2 1 0.1UF/16V
GND_AUDIO GND

HP & MIC Connector

[36] MIC2_VREFO_L
[36] MIC2_R_SLEEVE
[36] MIC2_L_RING2
R3713 2.2K/1%
R3714 2.2K/1%
Change to BEAD by EMI Eason (20180827)
L3703 1 2 120OHM/100MHz
L3702 1 2 120OHM/100MHz
MIC_MIX_CON
MIC2_LRING2_CON
C3712 470PF/50V
C3711 470PF/50V
GND_AUDIO GND_AUDIO

HP & MIC Connector

[36] TOU_CON
MIC_MIX_CON
ESS_HP_L_CON
ESS_HP_R_CON
MIC2_LRING2_CON
J3701
AUDIO_JACK_8P
12016-00778100
配套插头参考图
电原理图
M/G
L/R
R/L
G/M

EMI

MIC2_LRING2_CON C3713 470PF/50V GND_ESS
TOU_CON C3715 470PF/50V GND_ESS
MIC_MIX_CON C3716 470PF/50V GND_ESS
MIC2_LRING2_CON D3701 AZ9122-01F.R7GR GND_ESS
TOU_CON D3702 AZ5325-01F GND_ESS
ESS_HP_L_CON C3714 470PF/50V GND_ESS
ESS_HP_R_CON C3717 470PF/50V GND_ESS
MIC_MIX_CON D3703 AZ9122-01F.R7GR GND_ESS
ESS_HP_L_CON D3704 AZ5325-01F GND_ESS
ESS_HP_R_CON D3705 AZ5325-01F GND_ESS

2019.02.26 Modify DEPOP solution(MOS low Rds on)

MUTE

R3703 1 2 0Ohm
MUTE_POP#
Q3737 MUTE_POP#
Q3738 MUTE_POP#
ESS_HP_L
ESS_HP_L_CON
ESS_HP_R
ESS_HP_R_CON
AC_HP_L_O
AC_HP_R_O
R3704 1 2 0Ohm

20190620 Follow Audio Design IP ALC3288_ES9118_SMARTAMP_MULTISTREAM_0617(Modified by Eberwin)

MUTE CONTROL

[35] ACZ_RST#_AUD
+1VS_AUD_DVDD
MIC2_VREFO_R
R3731 100KOhm
R3732 100KOhm
R3734 100KOhm
Q3717A UMW1N
Q3717B UMW1N
Q3718A UMW1N
Q3718B UMW1N
R3722 1 2 0Ohm
MUTE_POP#
C3757 2.2UF/16V
I2S_OUT_JD
R3737 1 2 0Ohm
Q3719A UMW1N
Q3719B UMW1N
Q3720A UMW1N
Q3720B UMW1N

ACZ_RST#_AUD	MIC2_VREFO_R	I2S_OUT_JD	Mute_POP#
L	L	X	L
H	L	L	L
H	L	H	H
H	H	L	H
H	H	H	H

EXTERNAL MICROPHONE

[36] HPOUT_R
[36] HPOUT_L
[36] LINE1_L
[36] LINE1_R
R3712 1 2 680HM
R3713 1 2 680HM
HP_JACK_R_O_L
HP_JACK_L_O_L
L3704 1 2 120OHM/100MHz
L3701 1 2 120OHM/100MHz
HP_JACK_R_O_C
HP_JACK_L_O_C
C3702 2 1 4.7UF/6.3V
C3701 2 1 4.7UF/6.3V
R3711 1MOHM
R3705 1KOHM
C3703 100PF/50V
C3704 100PF/50V
GND_AUDIO
[36] LINE1_JD
J3701
SLJ3722
SLJ3721
MIC_IN_AC_L_CON
MIC_IN_AC_R_CON
J3702
AUDIO_JACK_8P
12014-00718100
D3708 AZ5325-01F
D3709 AZ5325-01F
D3710 AZ5325-01F
LINE1_JD

ESS ES9118EQ

+3.3VS_AVDD
R3704 47KOhm
ESS_RESET#
C3779 1000PF/50V
[11,24,30,33,40,41,53,59,72]
BLIF_PLT_RST#
R3777 0Ohm
R3780 47KOhm
R3782 47KOhm
R3791 47KOhm
ESS_GPIO3
ESS_GPIO4
ESS_ADDR
R3792 100KOhm
ESS_ADDR : 0 = 0x90
ESS_ADDR : 1 = 0x92
[16,38] SMB_CLK_S
[16,38] SMB_DAT_S
R3793 0Ohm
R3794 0Ohm
ESS_CLK
ESS_DAT

R3773 5.11KOHM
C3763 2200PF/16V
C3764 1000PF/50V
Review update
C3762 2200PF/16V
R3772 5.11KOHM
C3760 4.7UF/6.3V
C3761 1UF/10V
ESS_AVCC_DAC
ESS_HP_L
ESS_HP_R
ESS_DVDD
[36] I2S_DOUT2_C
[36] I2S_LRCLK_C
[36] I2S_BCLK_C
ES9118EQ
DVDD
GPIO2
GPIO1
DATA2
DATA1
DATA_CLK
RESETB
SCL
SDA
ADDR
AVCC_HP
AVCC_CP
C1_SW
C2_SW
C1
C2
PREG_SW
PREG
AGND_CP
AGND_HP
HTI
HTO
LRCK
BCK
SDIN
SDOUT
MCLK
GPIO3
GPIO4
ADDR
DOUT_EN
U3701
Address 0x90(Write)
XTAL/OSC_OUT
XTAL/OSC_IN
R3778 0Ohm
C3765 2200PF/16V
C3766 1000PF/50V
Review update
C3767 2200PF/16V
R3765 5.11KOHM
C3754 2200PF/16V
R3767 5.11KOHM

+3VS_VCCA
ESS_DVDD
ESS_AVCC_DAC
+3VS_AVDD
C3767 1UF/10V
C3768 1UF/10V
C3766 2.2UF/10V
C3769 1UF/10V
+1.8VS_AVCC_HP
+1.8VS_AVCC_CP
C3760 2.2UF/10V
C3759 2.2UF/10V
ESS vendor recommend to reserve one ERIS closed to 3.5mm jack at least. Remark another's resistance.
R3781 0Ohm

MOAT
C3757 0.1UF/25V
C3758 0.1UF/25V
C3759 0.1UF/25V
MOAT
C3779 0.1UF/25V
2012/05 Add for MIC Noise

+3VS_AUDIO
R3757 100KOhm
R3761 100KOhm
MIC2_LRING2_CON
C3756 0.1UF/16V
C3746 0.1UF/16V
GND_AUDIO
[36] MIC2_VREFO_R
R3760 0Ohm
[0921] add Q3756_Q3705 reduce MP # cosmetic

Modify 1216

Codec LDO +3.3VS_AVDD

+3VS
L3705 1 2 120OHM
+3.3VS_AVDD
C3752 4.7UF/6.3V
GND

Codec LDO +3VS_VCCA

+3VS
+3VS_VCCA
R3768 0Ohm
U3707
IN GND EN OUT NC
LP5907MFX-2.8/CP6
R3771 0Ohm
C3774 4.7UF/6.3V
C3776 4.7UF/6.3V
Indo: 24007-01620000
UTC LR5320-18-AE3-R cost down

Codec LDO +1.8VS_AVCC_HP

+3VS
+1.8VS_AVCC_HP
R3769 0Ohm
U3708
LP5907MFX-1.8
R3770 0Ohm
C3772 4.7UF/6.3V
C3773 4.7UF/6.3V
Indo: UTC LR5320-18-AE3-R cost down

Codec LDO +1.8VS_AVCC_CP

+3VS
+1.8VS_AVCC_CP
R3784 0Ohm
U3709
LP5907MFX-1.8
R3785 0Ohm
C3771 4.7UF/6.3V
C3775 4.7UF/6.3V
Indo: UTC LR5320-18-AE3-R cost down

50MHz XTAL

C3775 22PF/50V
Y3701 50MHz
C3777 22PF/50V
R3763 0Ohm
R3776 1MOhm
R3764 0Ohm
XTAL/OSC_IN
XTAL/OSC_OUT

RECOMMENDED POWER UP SEQUENCE

Before or after VCCA as long as RESETB is asserted (i.e. held low) until all external power supplies are stable
AVDD
VCCA
AVCC_SW, AVCC_HP
XI (if externally supplied)
Same time as VCCA or later
RESETB
At power up, assert RESETB until at least 1ms after all external power supplies (and XI if supplied externally) are stable
Subsequent reset(s), if necessary, should be asserted for 20ns or longer

Driver 行為會follow 下表

	EAPD_EC#	I2S_OUT_JD	MIC2_VREFO_R
Default	LOW	LOW	LOW
CTIA (L/R/G/M) Iphone	LOW	LOW	HIGH
OMTP (L/R/M/G) Nokia	LOW	HIGH	LOW
一般耳機	LOW	HIGH	HIGH
Speaker擴音單	HIGH	LOW	LOW
Speaker不擴音單	LOW	LOW	LOW

ASUSTeK COMPUTER INC.
Project Name: GX531GX
Rev: R1.0
Title: AUDIO ALC3236-CG/VB2 Jack
Size: D
Dept.: Mobile&COMPUTER Engineer:
Date: Friday, February 21, 2020
Sheet 37 of 66

BOM修改為TPS987DDJ料號
(P/N:06050-00920000)

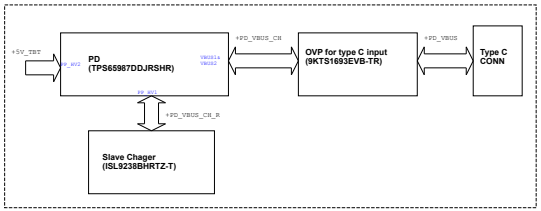
Imax=1port+1CC=3.6A

+5V_TBT

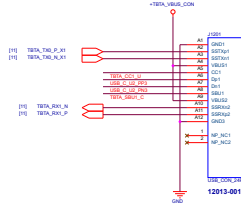
25mils

120mils

Power Flow Chart



TYPE-C Connector



TBT_MRESET Function Description

When assert MRESET, RESET2 signal will be asserted
as well and resend a reset signal to TBT.

Notice

Connect to PCH GPP_A11(CFL Platform)
Reveal Reset to TB for better gpio4 support
Should be connected to BC7302 GPIO
0 - No Action, Reset is being asserted
1 - Manual Reset is being assert

I2C1 address	R1219 DIV = 0	R1219+R1230 DIV = 0.338	R1219+R1247 DIV = 0.5	R1219+R1209 DIV = 0.90
I2C1_C1_ADDR	000b	001b	010b	011b
I2C1_C2_ADDR	100b	101b	110b	111b

Table 2. I²C Default Unique Address I2C1 - Port 1

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	0	I2C_ADDR_DECODE_C1[2:0]		R/W

Note 1: Any bit is mutable for slave port independently providing firmware override of the I²C address.

Table 3. I²C Default Unique Address I2C1 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	0	I2C_ADDR_DECODE_C2[2:0]		R/W

Note 1: Any bit is mutable for each port independently providing firmware override of the I²C address.

For the I2C2 interface, the unique I²C address is a fixed value as shown in Table 4 and Table 5.

Table 4. I²C Default Unique Address I2C2 - Port 1

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	0	0	0	R/W

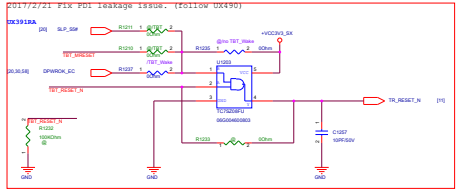
Note 1: Any bit is mutable for each port independently, providing firmware override of the I²C address.

I2C address Setting

Dead battery configuration

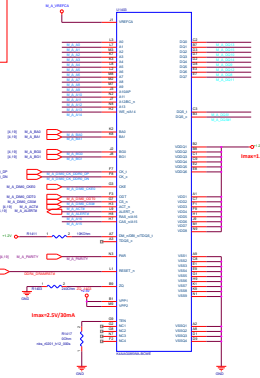
確認是否需要

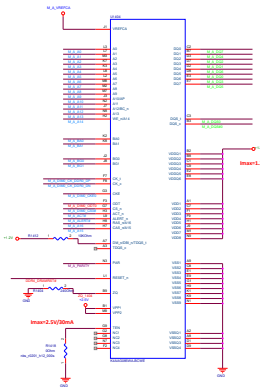
2017/2/21 Fix PDI leakage issue. (follow UX490)

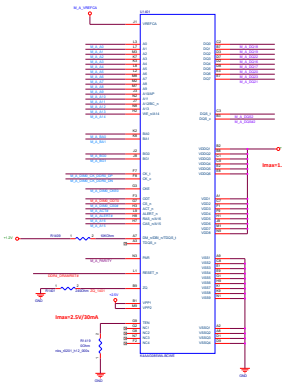


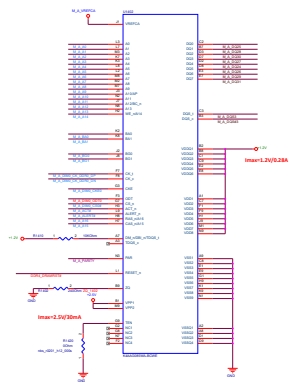
Project Name: DesignIP			Rev: R2.0a
Title : TBT_TPS65982&Type C_DP_R2.0a			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE1_RD3	
Date: Friday, February 21, 2020	Sheet: 12 of 106		

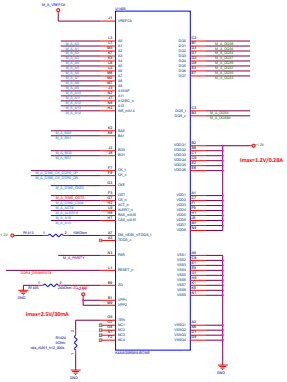
Micron 8G 03012-00030900
Strap Resistance
R2509,R2518,R2513 mount
R2516,R2517,R2515 unmount
Micron 16G 03012-00040300
Strap Resistance
R2516,R2517,R2513 mount
R2509,R2518,R2515 unmount

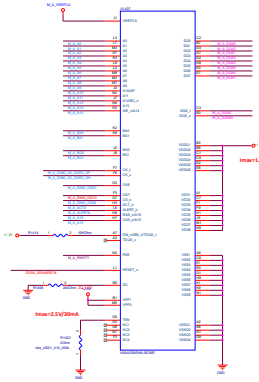


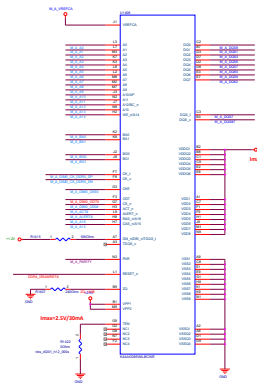


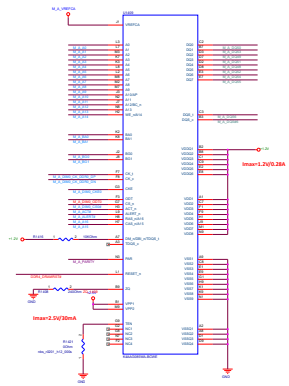


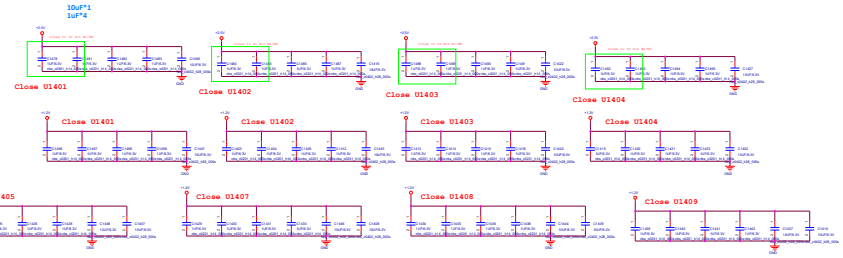


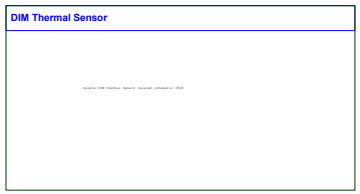


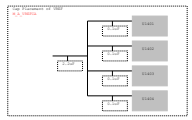


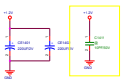












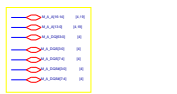
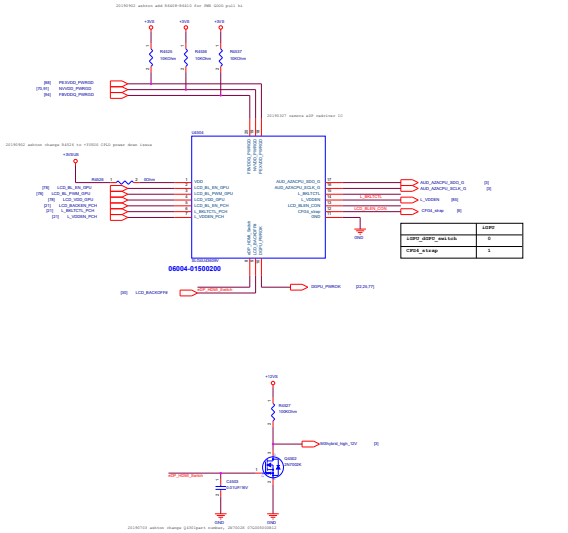


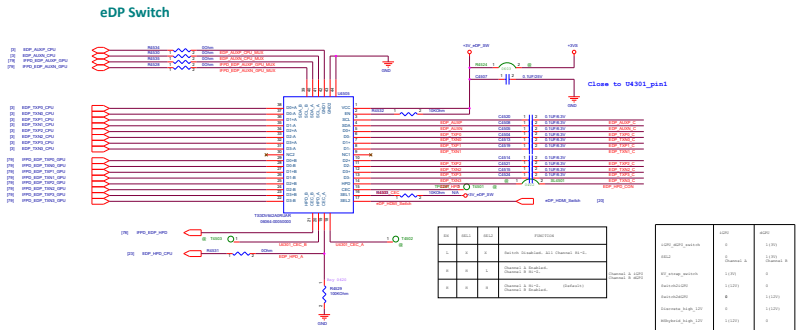
Table 4-25. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x8- 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x8 DRAM device as possible	64x 1µF (0402) (min of 48 stuffed)	
		Distributed around the DRAM devices	20x 10µF (0603) (min of 12 stuffed)	
	VPP	2 as near each x8 DRAM device as possible	32x 1µF (0402)	
		Distributed around the DRAM devices	10x 10µF (0603)	
	VTT	Distributed along termination resistors	32x 1µF (0402)	
		Distributed evenly across domain	8x 10µF (0603)	

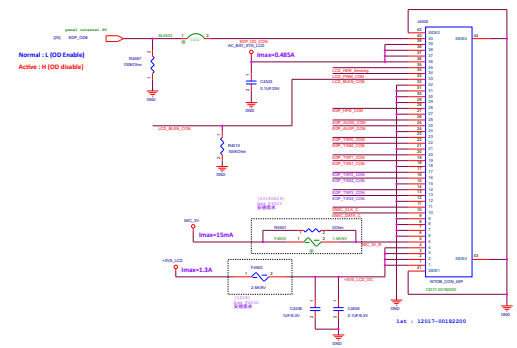
BL_EN/BL_PWM/L_VDDEN SWITCH IC(Switchable Use)



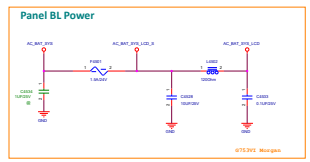
eDP Switch



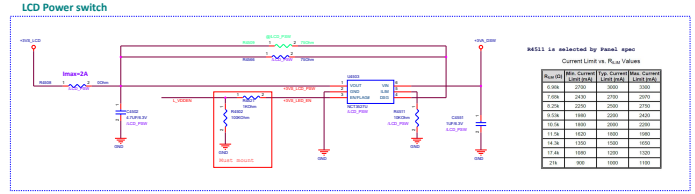
eDP Panel Conn.



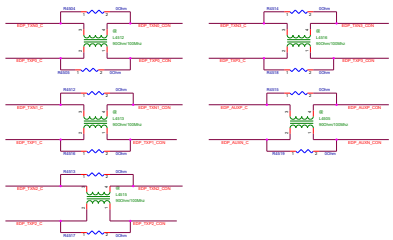
Panel BL Power



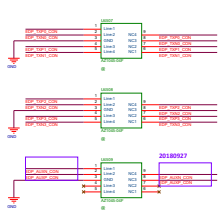
LCD Power switch



For EMI

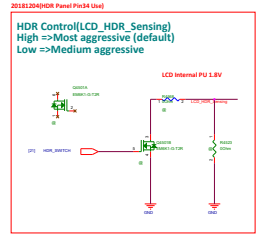


For ESD



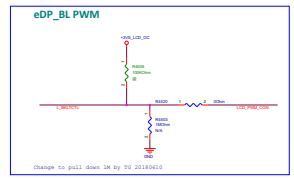
HDR Control(LCD_HDR_Sensing)

High =>Most aggressive (default)
Low =>Medium aggressive

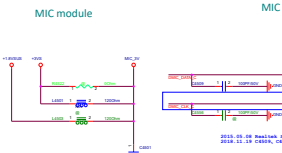


eDP_HPD (CPU)

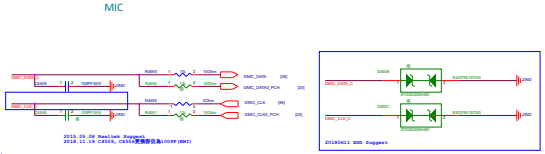
eDP_BL PWM



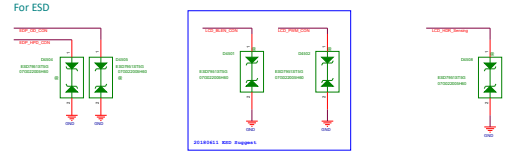
MIC module

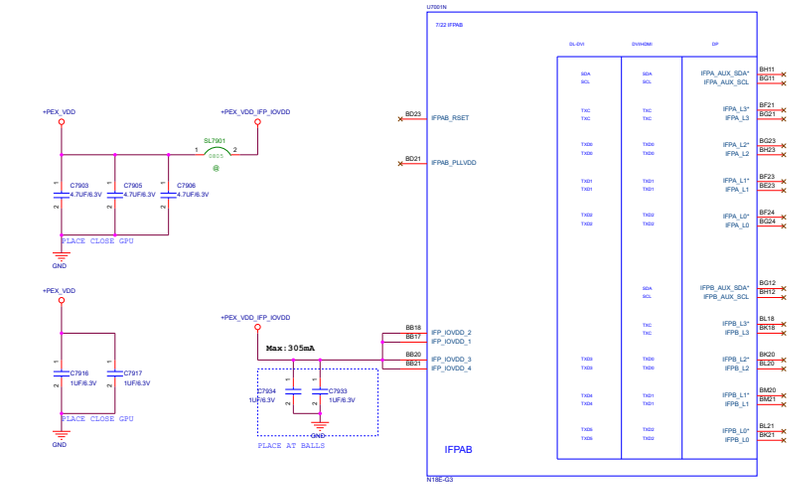


MIC

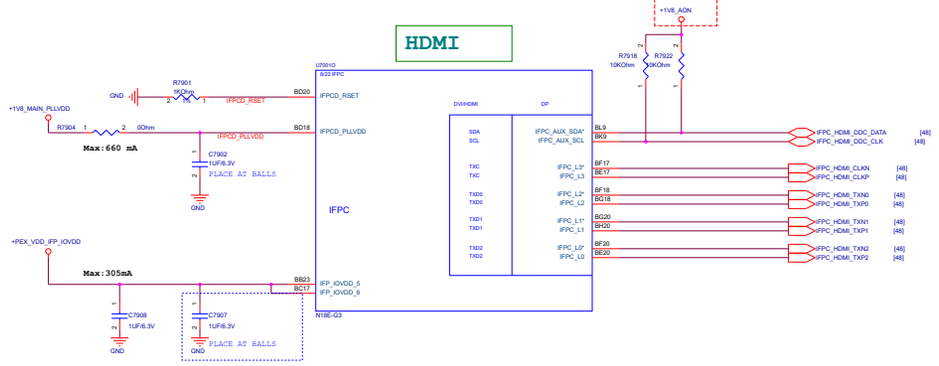


For ESD

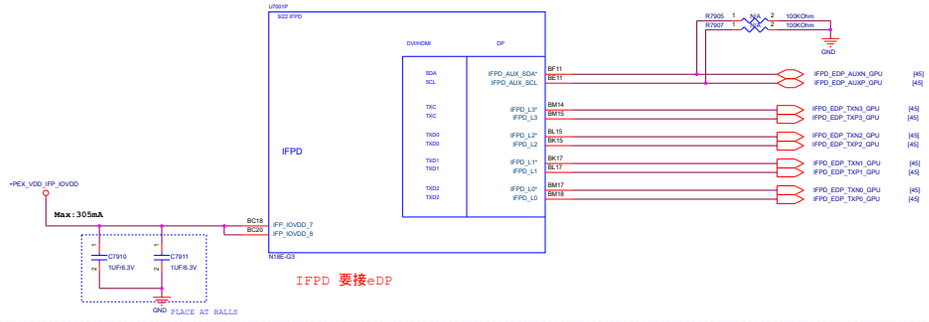




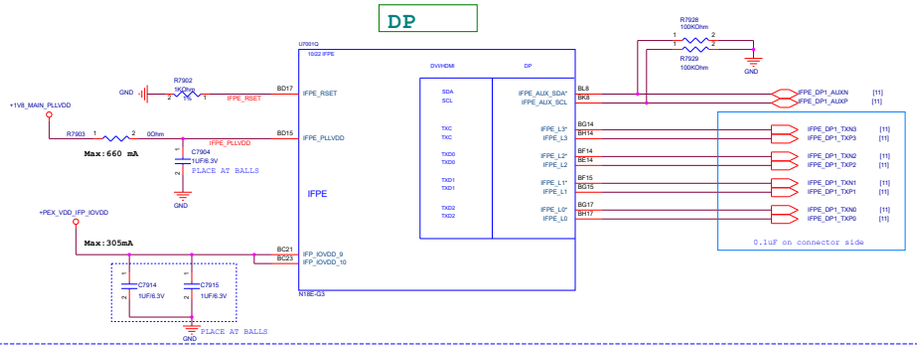
HDMI



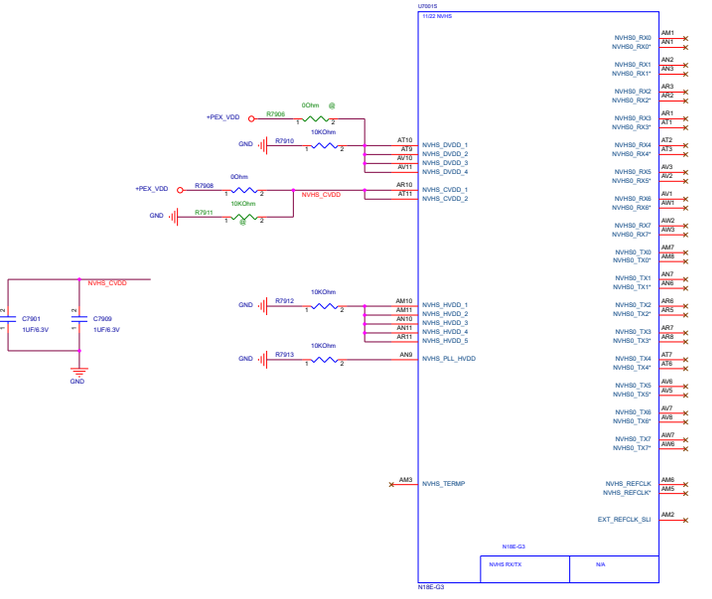
EDP(4Lane Panel)



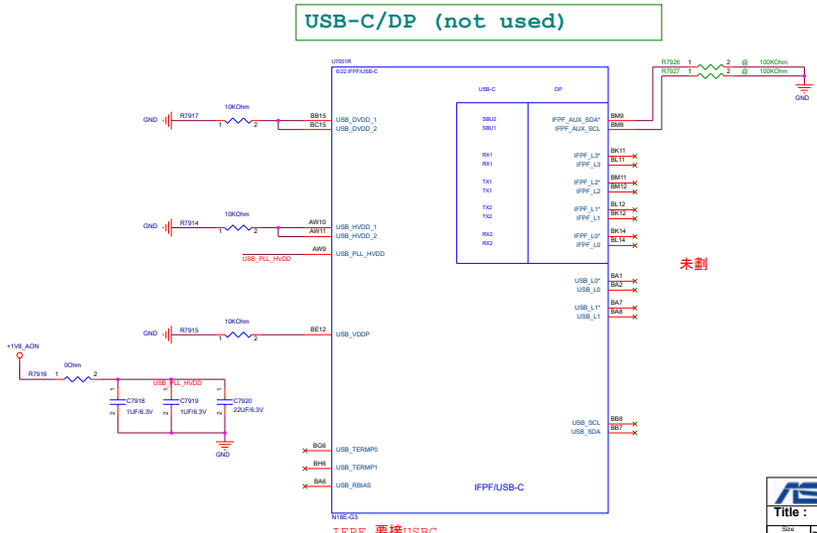
DP



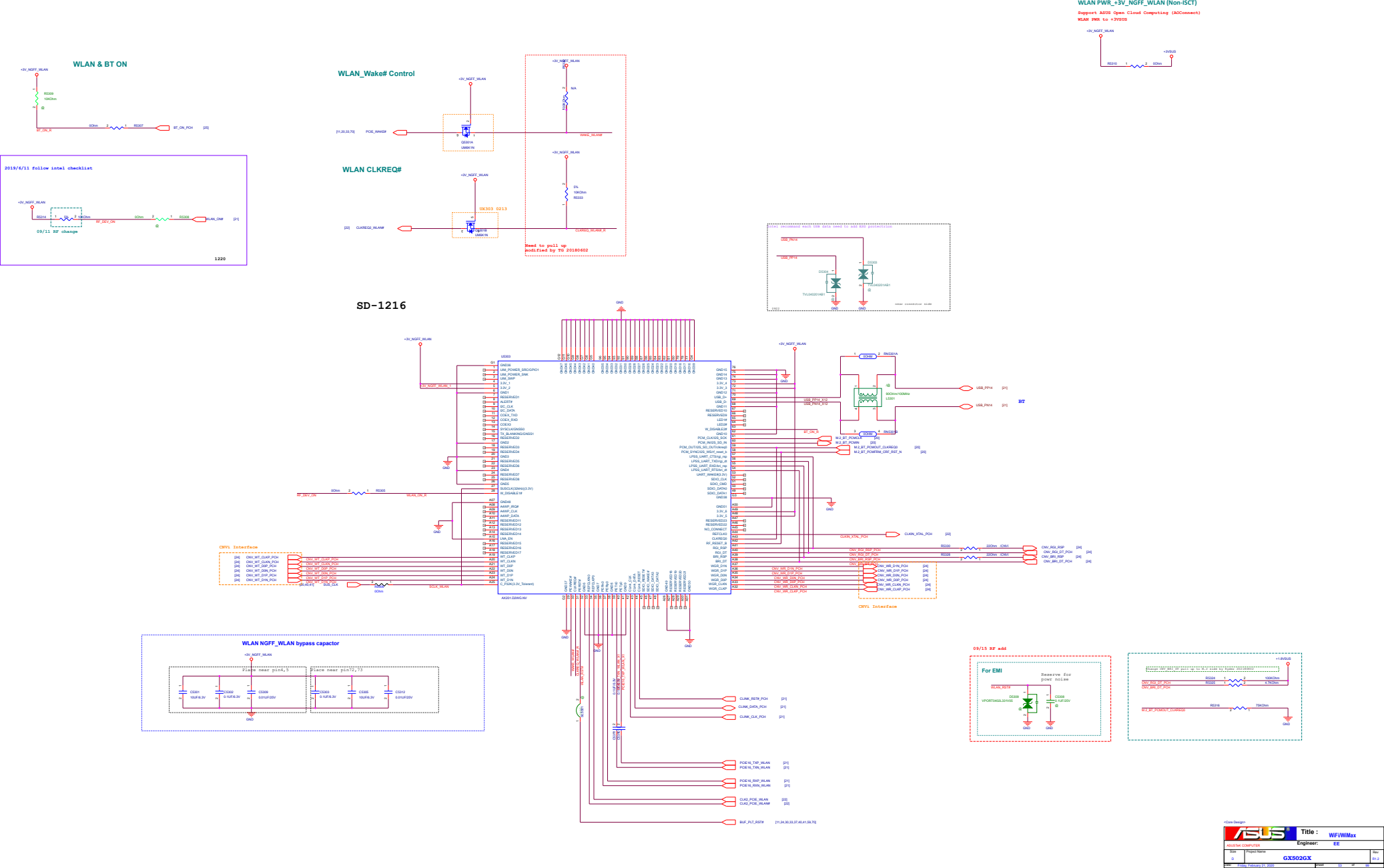
NVLink (not used)



USB-C/DP (not used)



ASUS	Project Name: GX502GX		Rev: R1.2
Title : GPU_DP/EDP/HDMI/LVDS/CRT			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Friday, February 21, 2020	Sheet: 79	of: 99	


WLAN & BT ON
WLAN_Wake# Control
WLAN CLKREQ#
WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)
Support ASUS Open Cloud Computing (AOConnect)
WLAN PWR to +3VSUS
2019/6/11 follow intel checklist
09/11 RF change
1220
SD-1216
WLAN NGFF_WLAN bypass capactor
09/15 RF add
For EMI
Reserve for power noise
CNVi Interface
Title : WiFi/WiMax
Engineer: EE
GX502GX

<Core Design>

Title : BT_Bluetooth

ASUSTeK COMPUTER

Engineer: EE

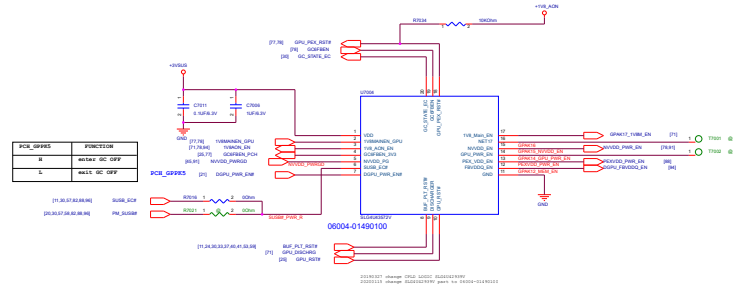
Size	Project Name	Rev
A	**GX502GX**	R1.2

Date:	Friday, February 21, 2020	Sheet	61	of	99

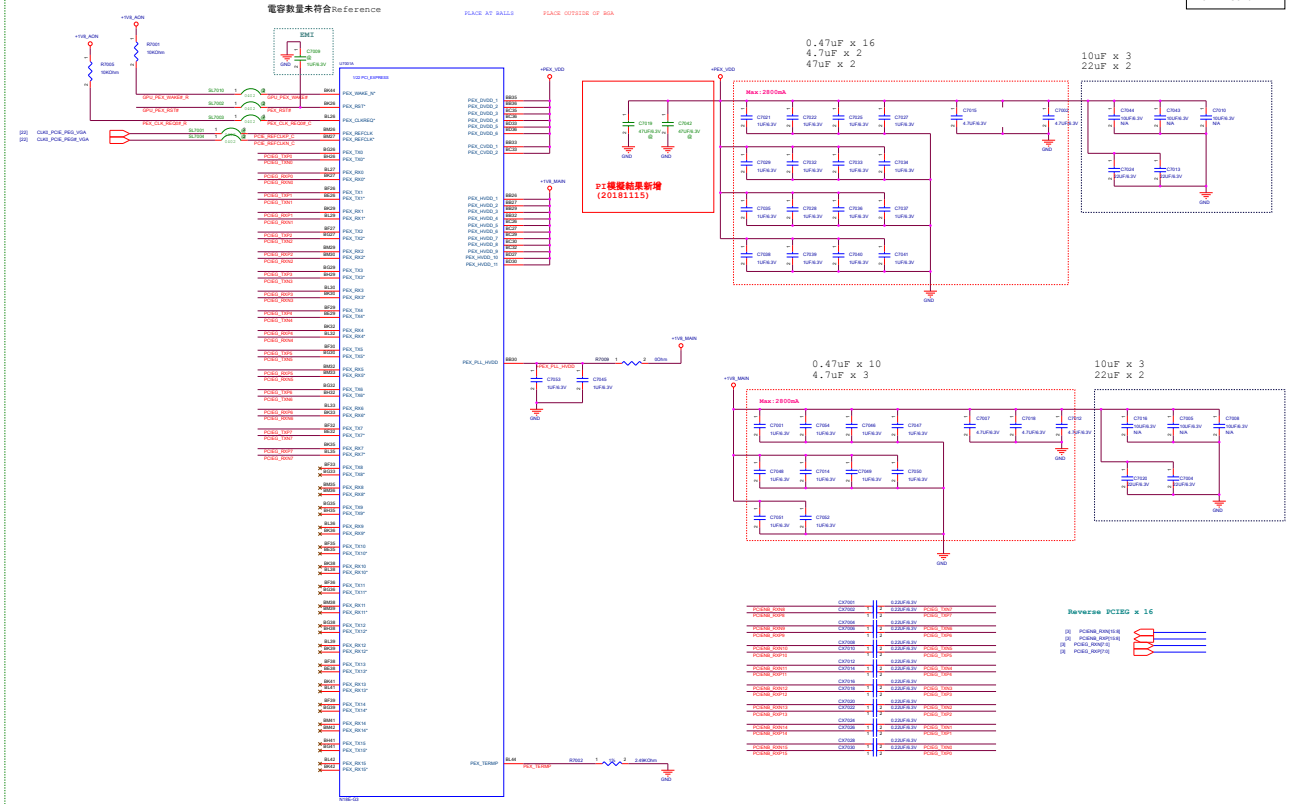
Main Board

GPU POWER SEQUENCE CONTROL

PCH_GPIO55	FUNCTION
H	enter GC OFF
L	exit GC OFF

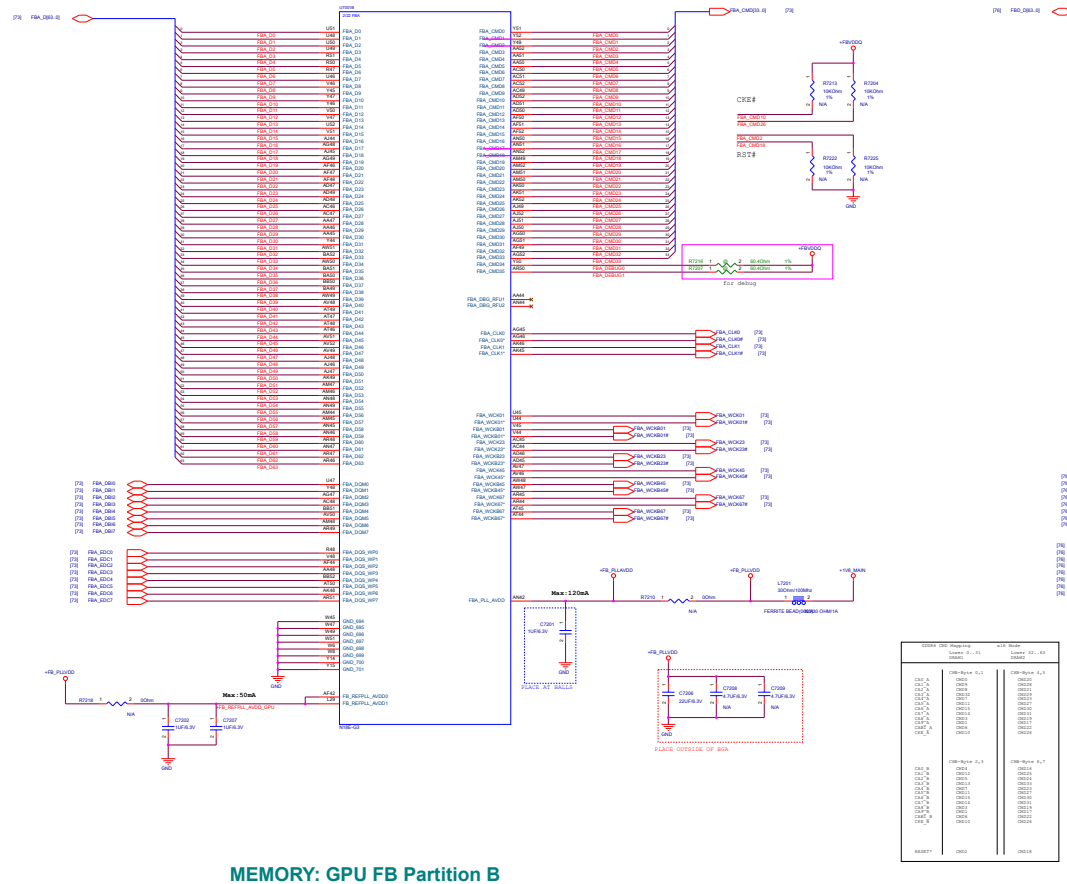


電容數量未符合Reference

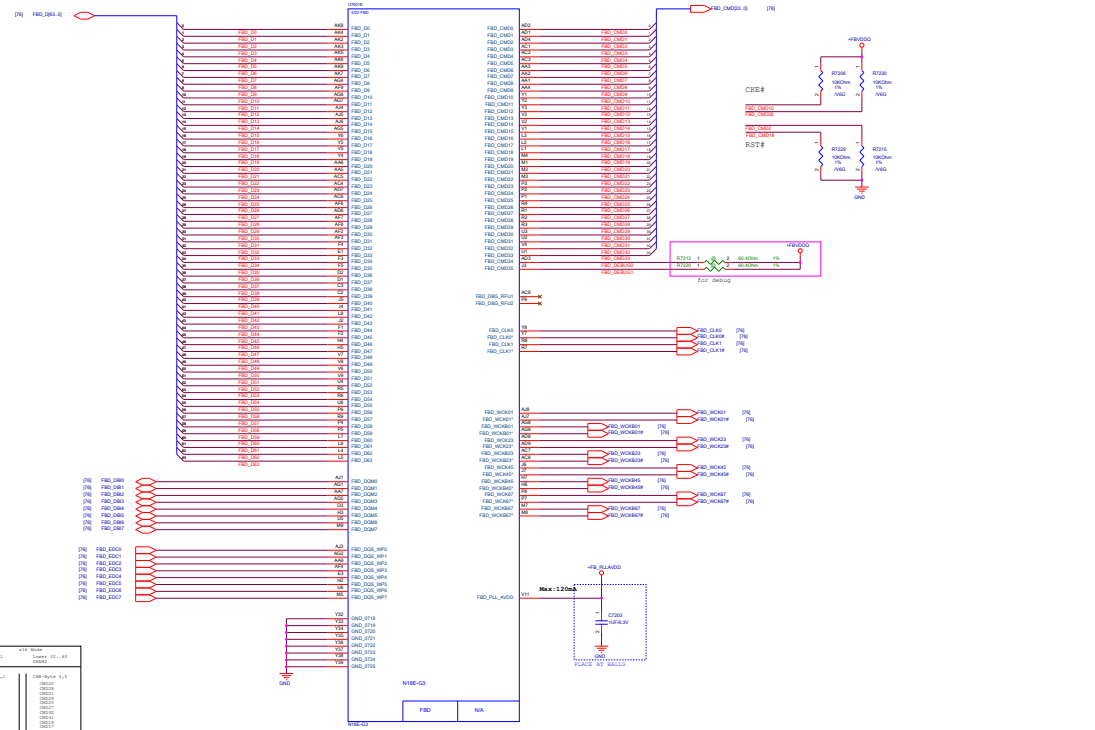


Project Name	GX502GX
Title :	GPU PCIE IF
Dept. :	ASUSTeK COMPUTER INC. Engineer:
Date:	Friday, February 21, 2020
Sheet	70 of 89

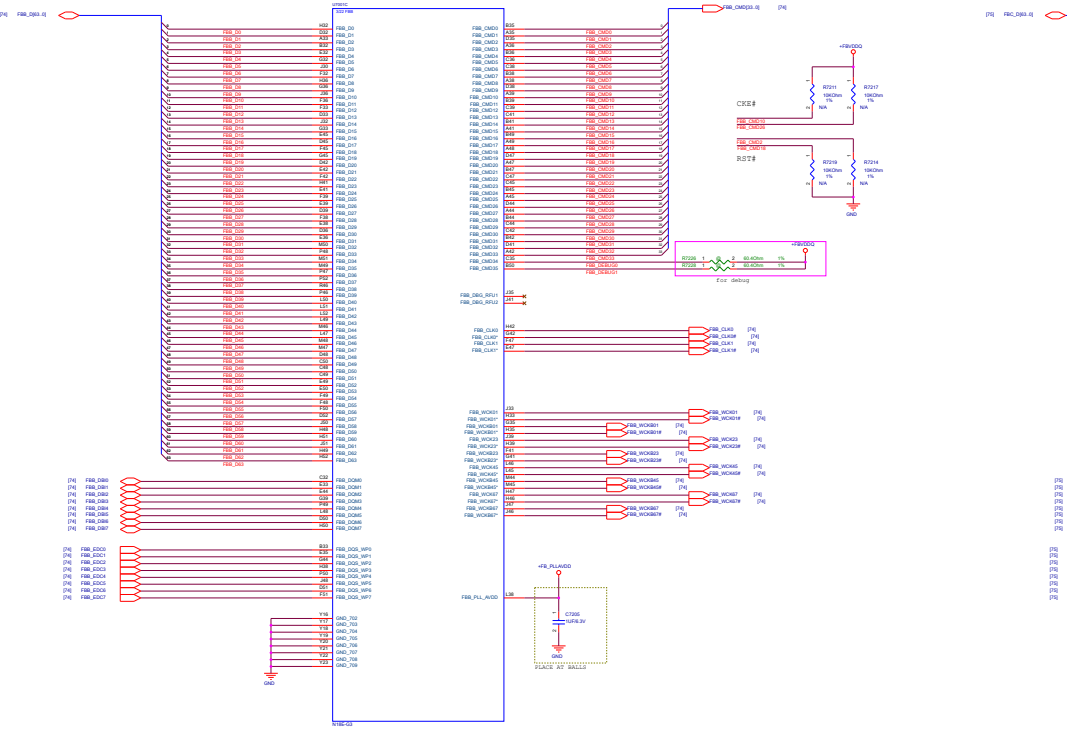
MEMORY: GPU FB Partition A



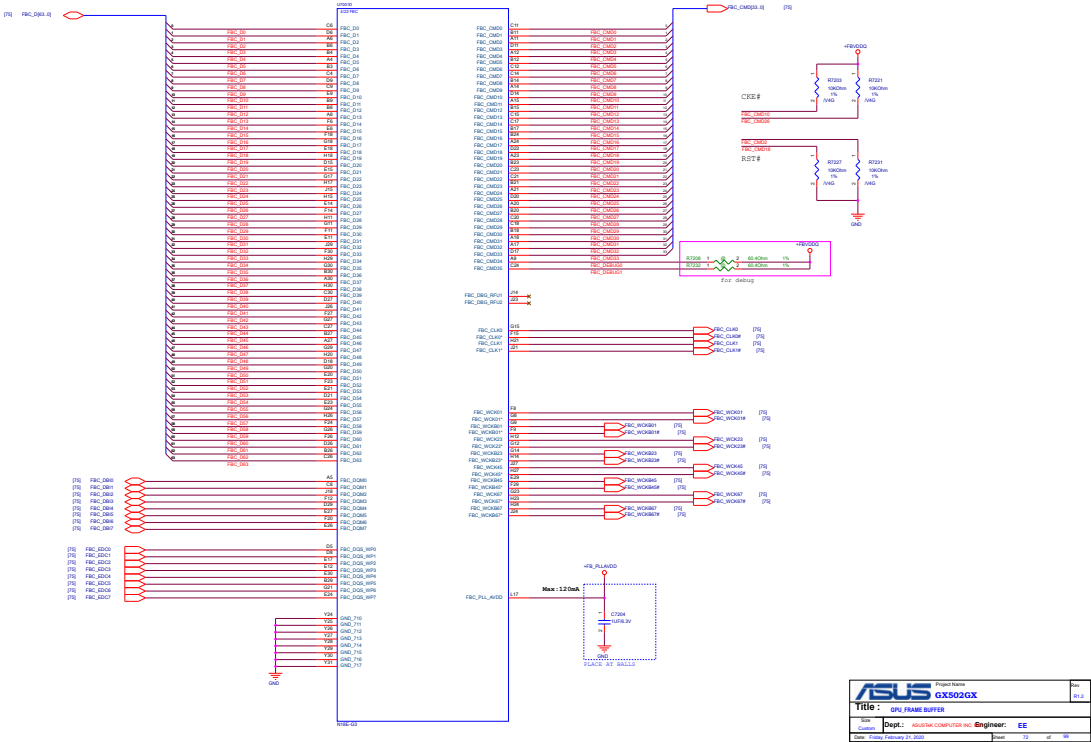
MEMORY: GPU FB Partition D



MEMORY: GPU FB Partition B



MEMORY: GPU FB Partition C



ASUS	Project Name: GX502GX		Rev: 81.2
Title :	GPU_FRAME BUFFER		
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Friday, February 21, 2020		Sheet: 72 of 98	

[72] FBA_D[31..0]

[72] FBA_CMD[33..0]

40 OHm_NET
FBA Partition 31..0
MF=1 Mirror

[72] FBA_D[63..32]

40 OHm_NET
FBA Partition 64..32
MF=0 Normal

待換Samsung
03014-00010100

U73001

U73002

+FBVDDQ

MEM_VPP

GND

MT61K256M32JE-14:A

C73001 820PF/50V

C73002 820PF/50V

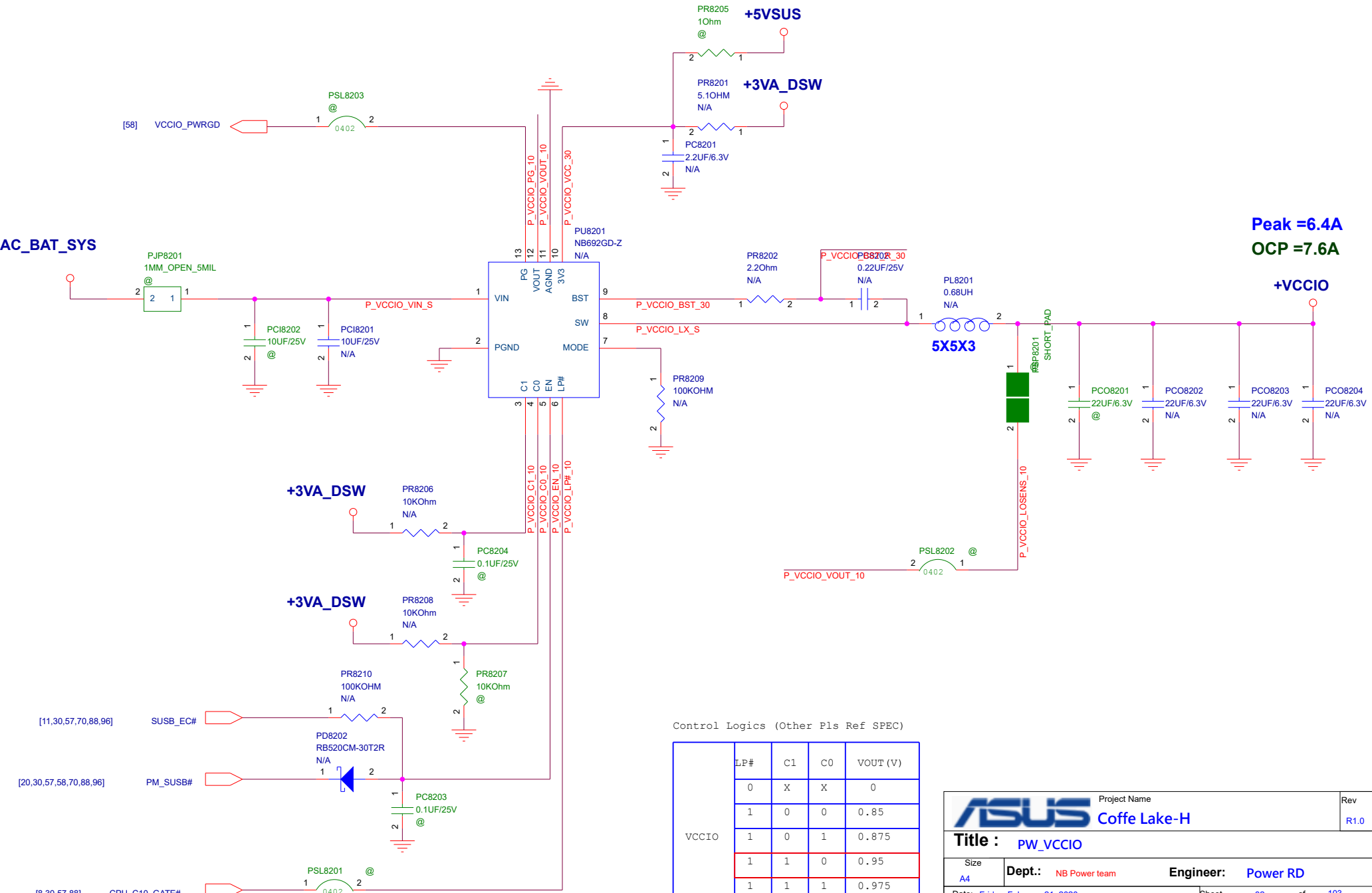
Project Name	Rev
GX502GX	R1.2

Title : VRAM_Channel_A

Size: Custom | Dept.: ASUSTeK COMPUTER INC. | Engineer:

Date: Friday, February 21, 2020 | Sheet 73 of 99

+VCCIO [For CPU]

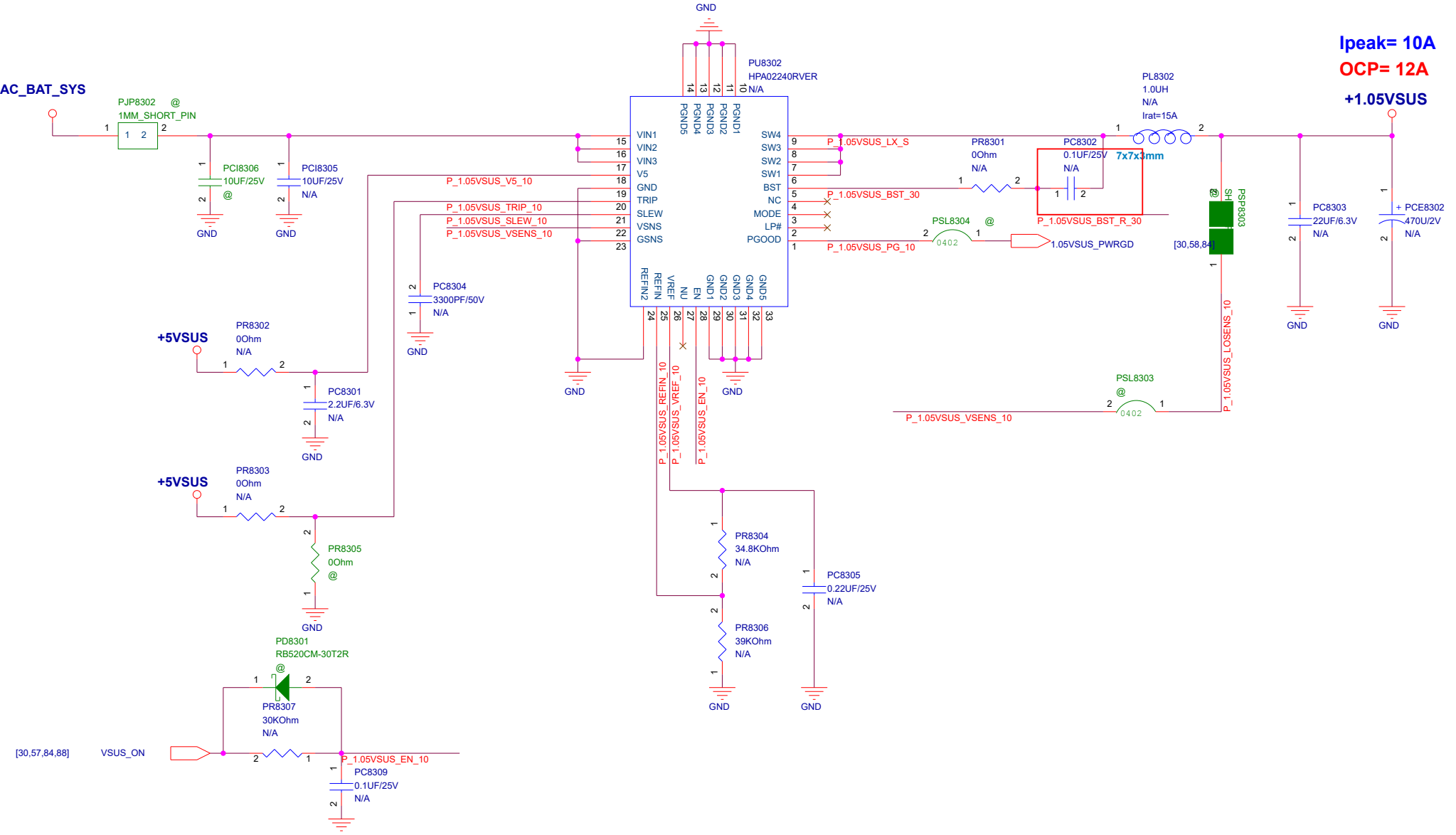


Control Logics (Other Pls Ref SPEC)

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

Project Name: Coffe Lake-H		Rev: R1.0
Title : PW_VCCIO		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Friday, February 21, 2020	Sheet 82 of 103	

+1.05VSUS [For PCH]

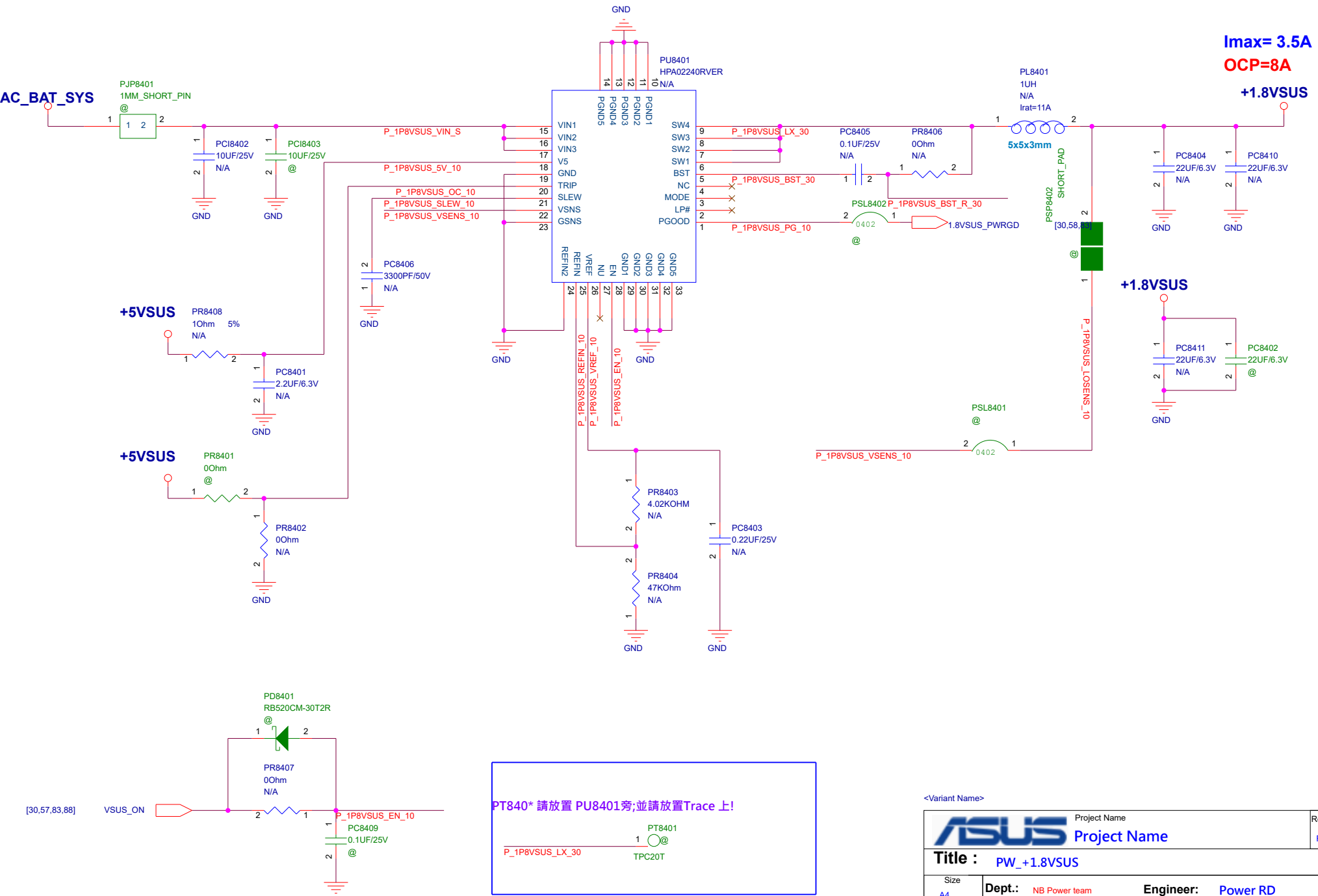


PT840* 請放置 PU8401旁;並請放置Trace 上!

<Variant Name>

Project Name: Coffe Lake-H		Rev: R1.0
Title : PW_+1.0VSUS		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Friday, February 21, 2020	Sheet 83 of 103	

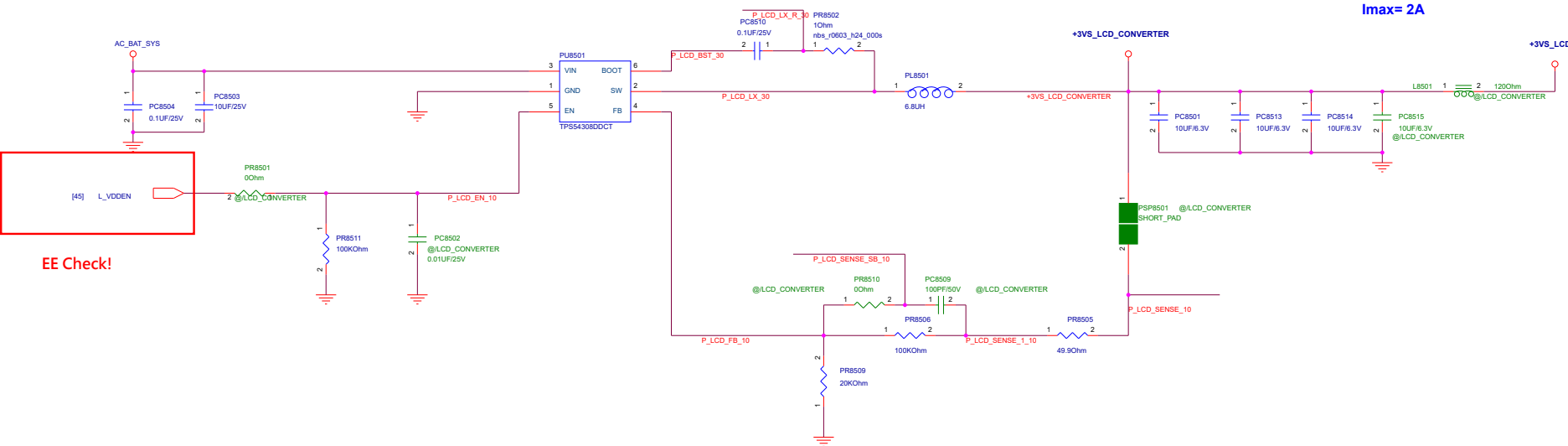
+1.8VSUS [For PCH]



<Variant Name>

Project Name: Project Name		Rev: R1.0
Title : PW_+1.8VSUS		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Friday, February 21, 2020	Sheet 84 of 103	

+3VS_LCD

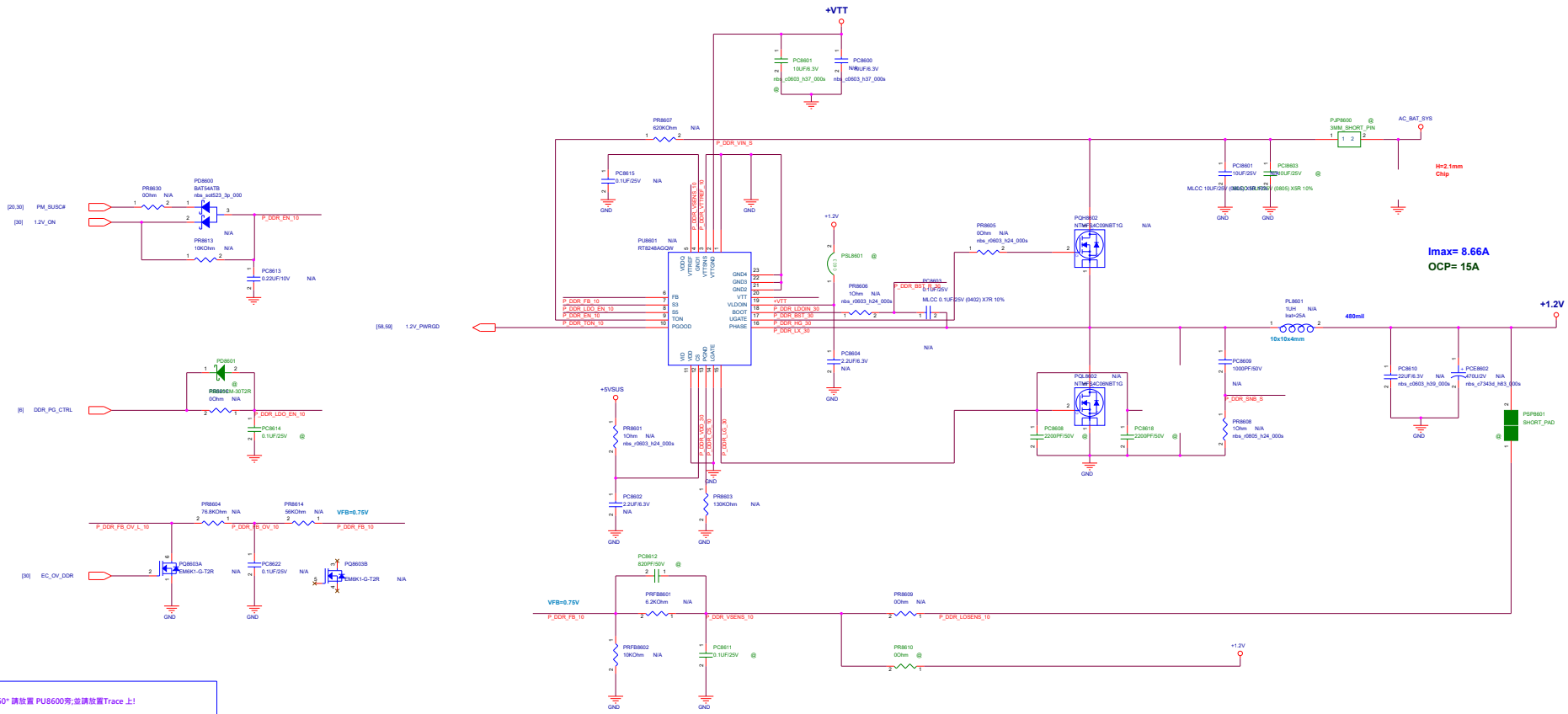


EE Check!

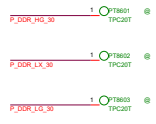
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : <Title>	
	Engineer: EE	
Size: C	Project Name: GX701	Rev: 1.0
Date: Friday, February 21, 2020	Sheet 85 of 103	

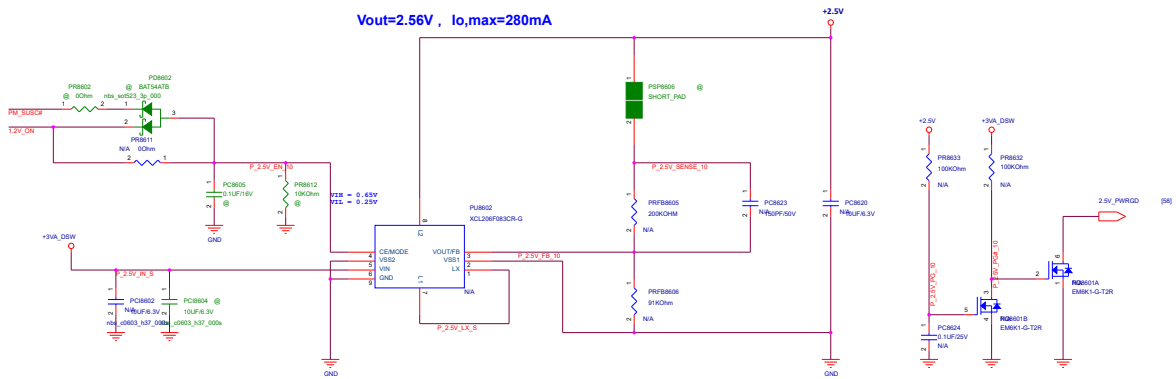
+1.2V / +VTT / +2.5V[For Memory]



PT860* 請放置 PU8600旁;並請放置Trace 上!



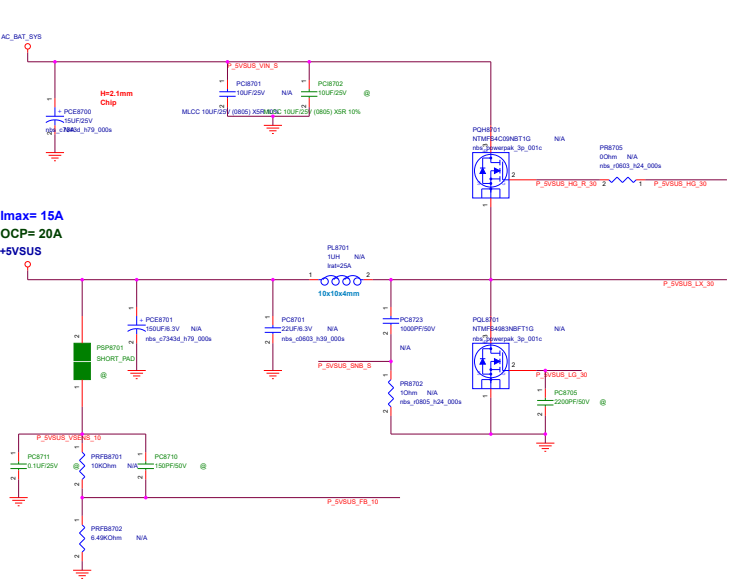
+2.5V BUCK (XCL206)

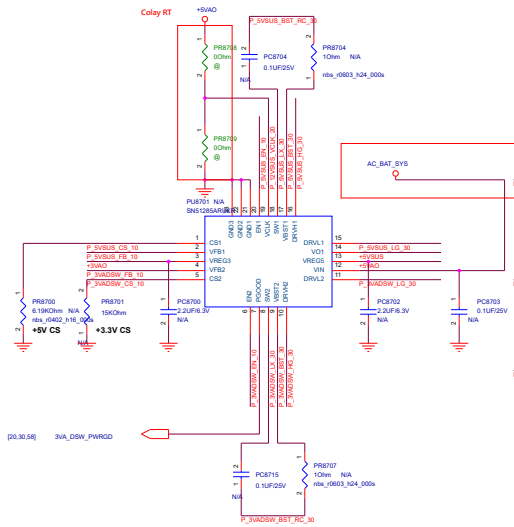


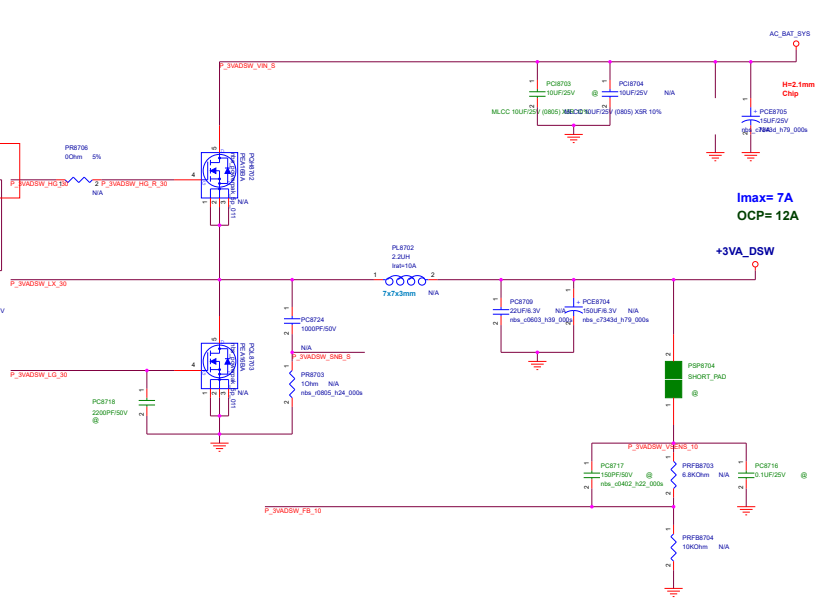
<Core Design>

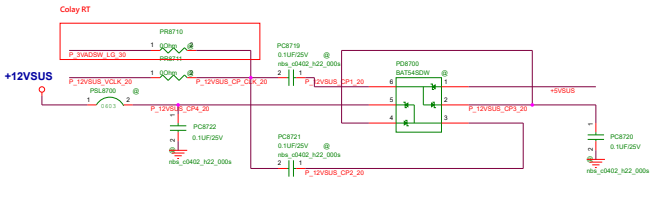
ASUS	Project Name: Coffee Lake-H		Rev: R1.0
Title : PW_+1.2V/+VTT/+2.5V			
Size: A2	Dept.: NB Power team	Engineer: HON	
Date: Friday, February 21, 2020	Sheet: 86 of 103		

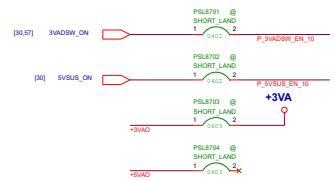
+3VA_DSW / +5VSUS [System Power]











請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm

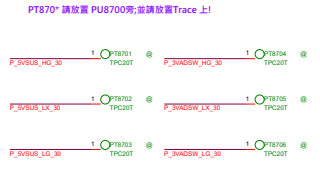
Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

PT870* 請放置 PU8700旁;並請放置Trace 上!

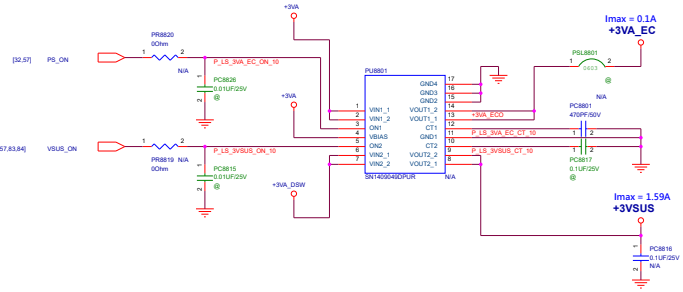


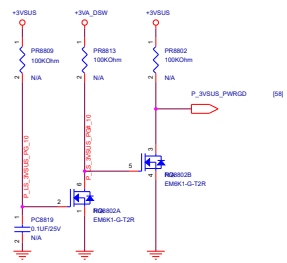
<Core Design>

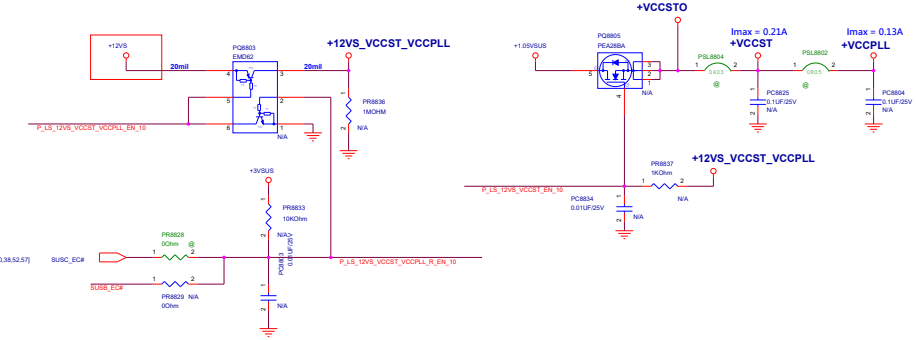
ASUS	Project Name: GX502GX		Rev: R1.2
Title : PW_+3VA_DSW/+5VSUS			
Size: A2	Dept.: NB Power team	Engineer: Joe	
Date: Friday, February 21, 2020	Sheet: 87	of: 99	

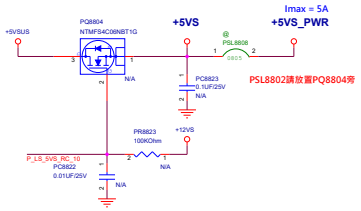
Load Switch

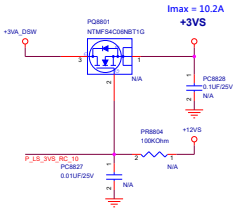
Main Board

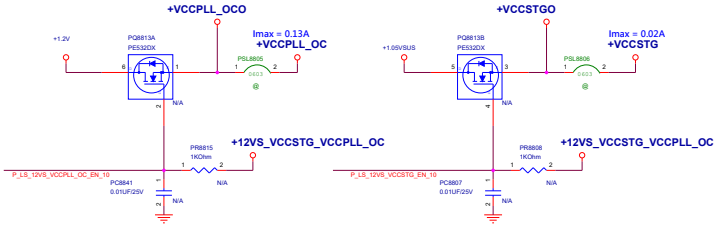




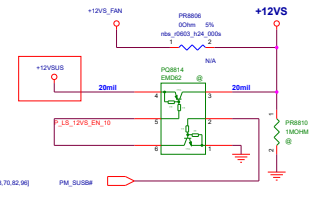


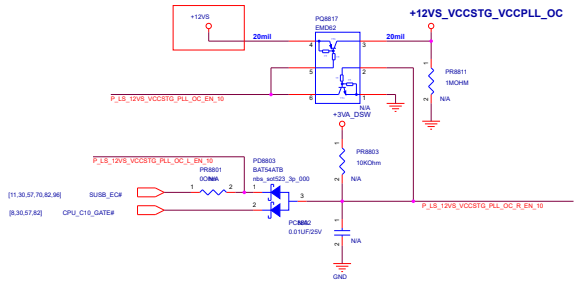


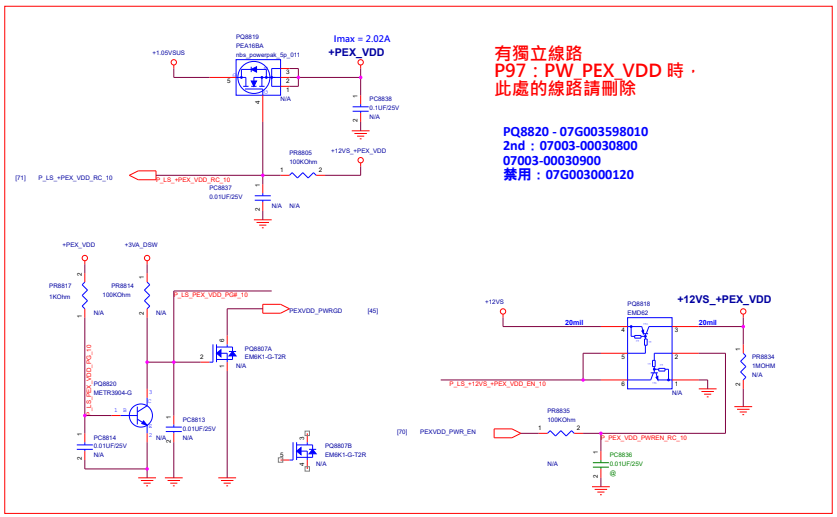




+12VS 的 Vin 對應 BOM 表		
	+12VS_FAN	+12VSUS
PR8806	N/A	@
PR8810	@	N/A
PQ8814	@	N/A







有獨立線路
P97：PW_PEX_VDD 時，
此處的線路請刪除

PQ8820 - 07G003598010
2nd：07003-00030800
07003-00030900
禁用：07G003000120

ASUS	Project Name: Coffeelake-H		Rev: R1.0
Title : PW_LOAD SWITCH			
Size: A2	Dept.: NB Power team	Engineer: Besnon	
Date: Friday, February 21, 2020		Sheet: 88 of 103	

PRS8901	ADP<120W	ADP<=230W	ADP>230W	ADP>330W
	TBD	5m	5m	2m
	TBD	10125-0008B100	10108-0008B000	10108-0008B000

PRS8903	ADP=120W	ADP=150W	ADP=180W	ADP=230W	ADP=240W	ADP=280W	ADP=330W
	200m	255m	X	X	330m	X	560m
	10114-00180000	10114-00221000	X	X	10021598311010	X	10114-00211000

AC_BAT_SYS

PJP8900,PJP8901
請從PR8921內側中間拉線。

AD_DOCK_IN

AD : 17.8V

If you support Slave CHG, please select Green Box and check off-page net name with EE

BAT

AD : 17.5V
Place Close to PJP8901

Limit : Charge 4A
DisCharge 16A

HW_Throttle

AC limit = 100% ADP
Bat limit = byte 7 x 1.7

dGPU_PD# ---> GPIO12(EE page 75 or 78)

Plug HW Throttle(Out)

Plug HW Throttle(In)

POP window

Adaptor select
total power = 90% ADP

Adaptor select		N Series	S Series
PRS8901		10m	5m
PR8936			
14E 100210150014630	0.4V	45W	120W
31.6K 100210161614630	0.8V	150W	150W
56E 100210156014630	1.2V	180W	180W
93.1K 100210193114631	1.6V	65W	230W
150K 100210115014631	2.0V	NA	280W
270K 100210127014630	2.4V	90W	330W
560K 100210156014630	2.8V	120W	240W

Project Name	Coffee lake-H
Rev	R1.0
Title :	PW_CHARGER
Dept.:	NB Power Team
Engineer:	Benson
Date:	Friday, February 21, 2020
Sheet	88 of 103

Address Selection Table

Address	0x78	0x79	0x7A	0x7B	0x7C	0x7D	0x7E	0x7F
PBR003	10k	1.1k	2k	4.4k	7.5k	12.4k	19.1k	40k
PBR002	Open	8.2k	8.2k	8.2k	8.2k	8.2k	8.2k	8.2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	R	R	R	R	R	R	R
Function		Temp. Alert threshold setting		Sensed temp. data			bit 4 = 0 bit 3 = 0 bit 2 = 0 Rhee 310579 added

+5VSUS

+3VA_EC

Ch15:VCCIO PTB9015 near PU8201

Ch14:+3V_FAN PTB9014 near PU9601

Ch13:+1.8VSUS PTB9013 near PU8401

Ch12:+5VSUS PTB9012 near PQL8701

Ch11:+3VA_DSW PTB9011 near PQL8703

Ch10:1.05VSUS PTB9010 near PU8302

Ch9:+1.2V PTB9009 near PQL8602

Ch8:PSVDDQ PTB9008 near PQ89401

Ch7:NVVDD PTB9007 near PQ89201

Ch6:VCCSA PTB9006 near PU8105

Ch5:VCCGT PTB9005 near PQ88119

Ch4:VCCCORE PTB9016 near PQ88101

Ch3:AC FET PTB9003 near PQ8901

Ch2:JE003 PTB9002 near BAT Connect

Ch1:Charger PTB9001 near PQ8901

P_SMB6_DAT

P_SMB6_CLK

VAIN=3.56V~1V
NTC=115kohm~2.75kohm
(22度~125度)

Table 2. TRUTH TABLE

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

單獨下地

DC JACK_Protection

PTB9016 place near DC JACK(JE001)

AC_Short_Protection

AC_BAT_SYS

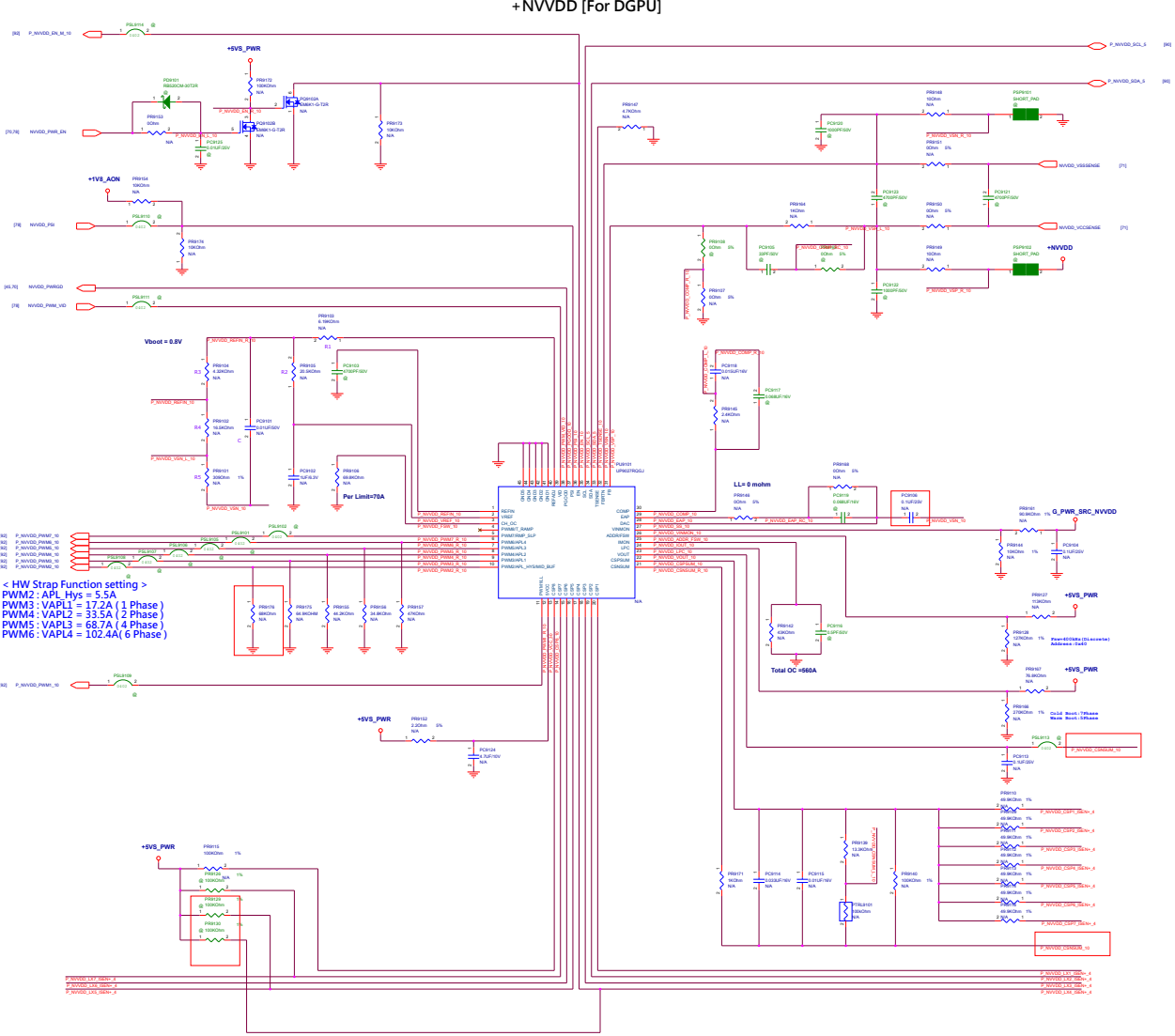
OVP Protection circuit 24V==>Cost down

OVP for type C input (Slave Charger)

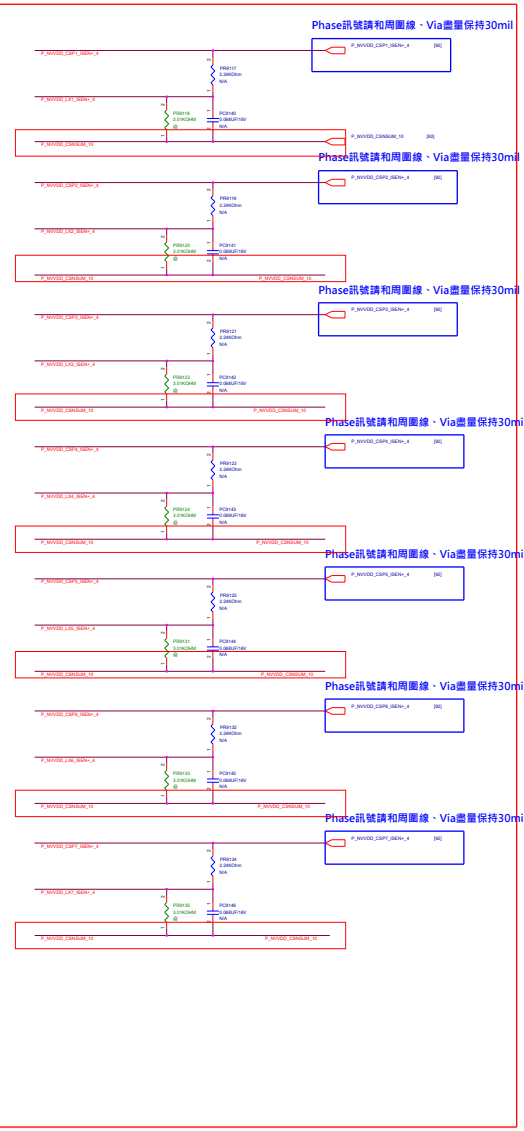
TETHYS OVP THRESHOLD==> MAX:24.22V MIN:23.271

Project Name	INS21220906
Title	PW_PROTECTION
Dept.	NB Power Team
Engineer	INS21220925
Date	Friday, February 21, 2020

+NVVDD [For DGPU]



請放靠近PU9101



Project Name: GX502GX			Rev: R1.2
Title : PW_+NVVDD (1)			
Size: A3	Dept.: NB Power team	Engineer: Neil	
Date: Friday, February 21, 2020	Sheet 91 of 103		

[72] FBC_D[31..0]

[72] FBC_CMD[33..0]

40 OHm_NET
FBC Partition 31..0
MF=1 Mirror

[72] FBC_D[63..32]

40 OHm_NET
FBC Partition 64..32
MF=0 Normal

待換Samsung
03014-00010100

U75003

+FBVDDQ

MEM_VPP

GND

MT61K256M32JE-14:A

[77] FBC_VREFC

C7501
820PF/50V
@/V4G

待換Samsung
03014-00010100

U75004

+FBVDDQ

MEM_VPP

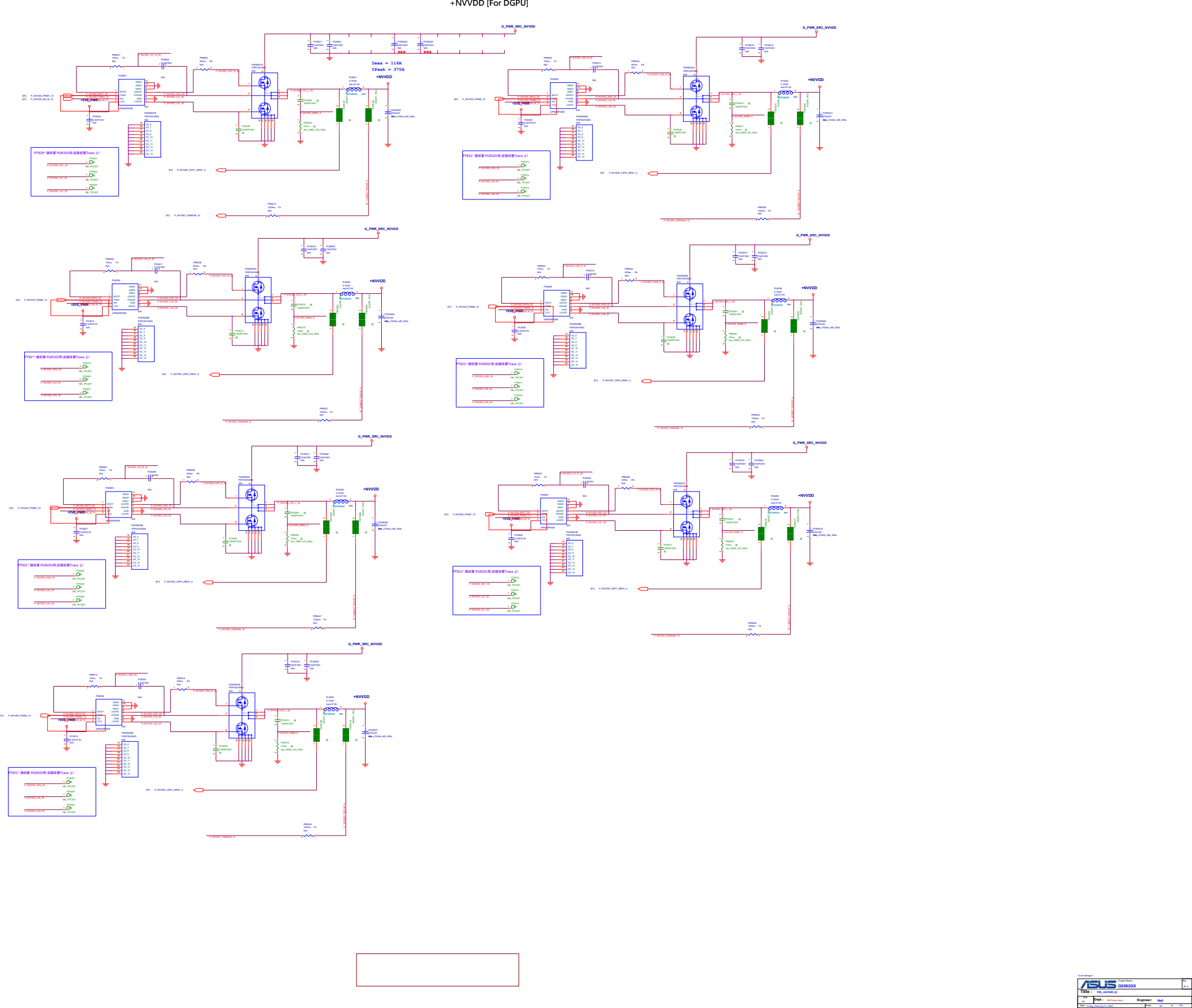
GND

MT61K256M32JE-14:A

C75003
820PF/50V
@/V4G

ASUS	Project Name: GX502GX		Rev: R1.2
Title : VRAM_Channel_C			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:	
Date: Friday, February 21, 2020	Sheet 75 of 99		

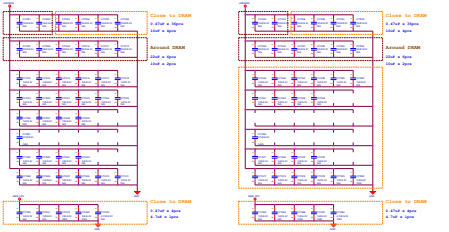
+NVVDD [For DGPU]



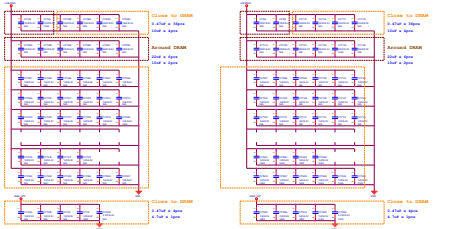
FBVDDQ
VRAM side

FBVDDQ
GPU side

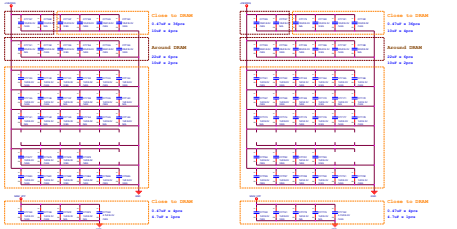
Channel A



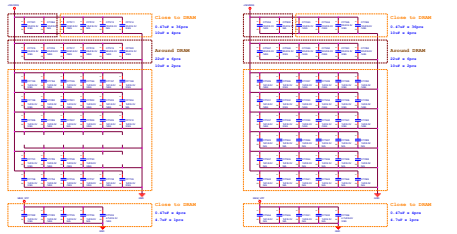
Channel B



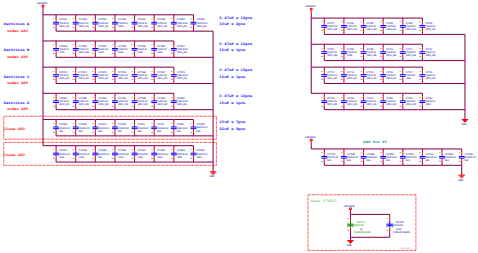
Channel C



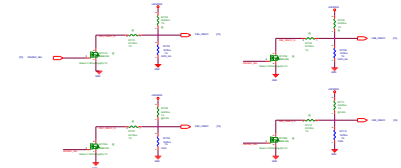
Channel D



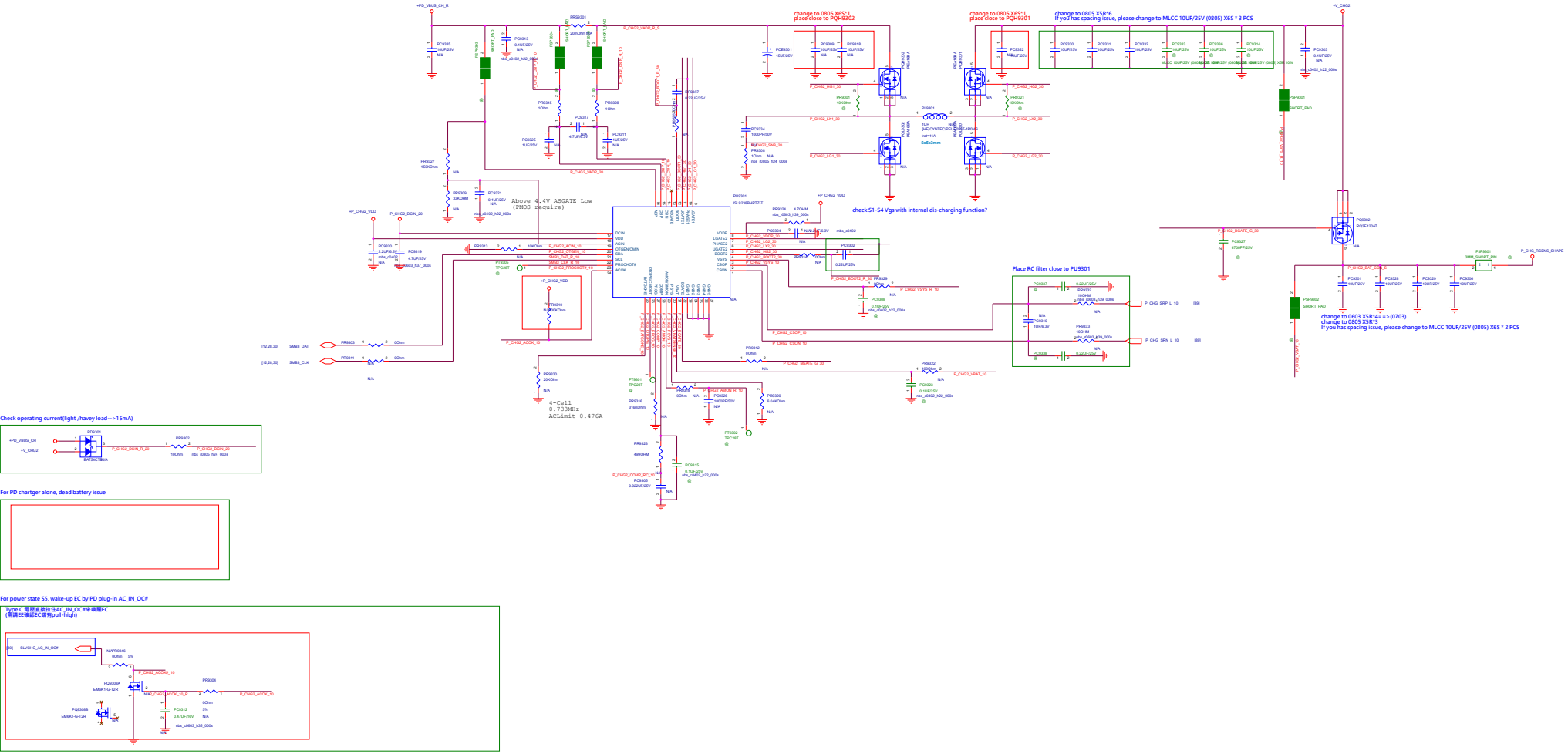
VRAM PWR_FBVDDQ



For power sequence measurement



Charger ISL9238 (NVDC)

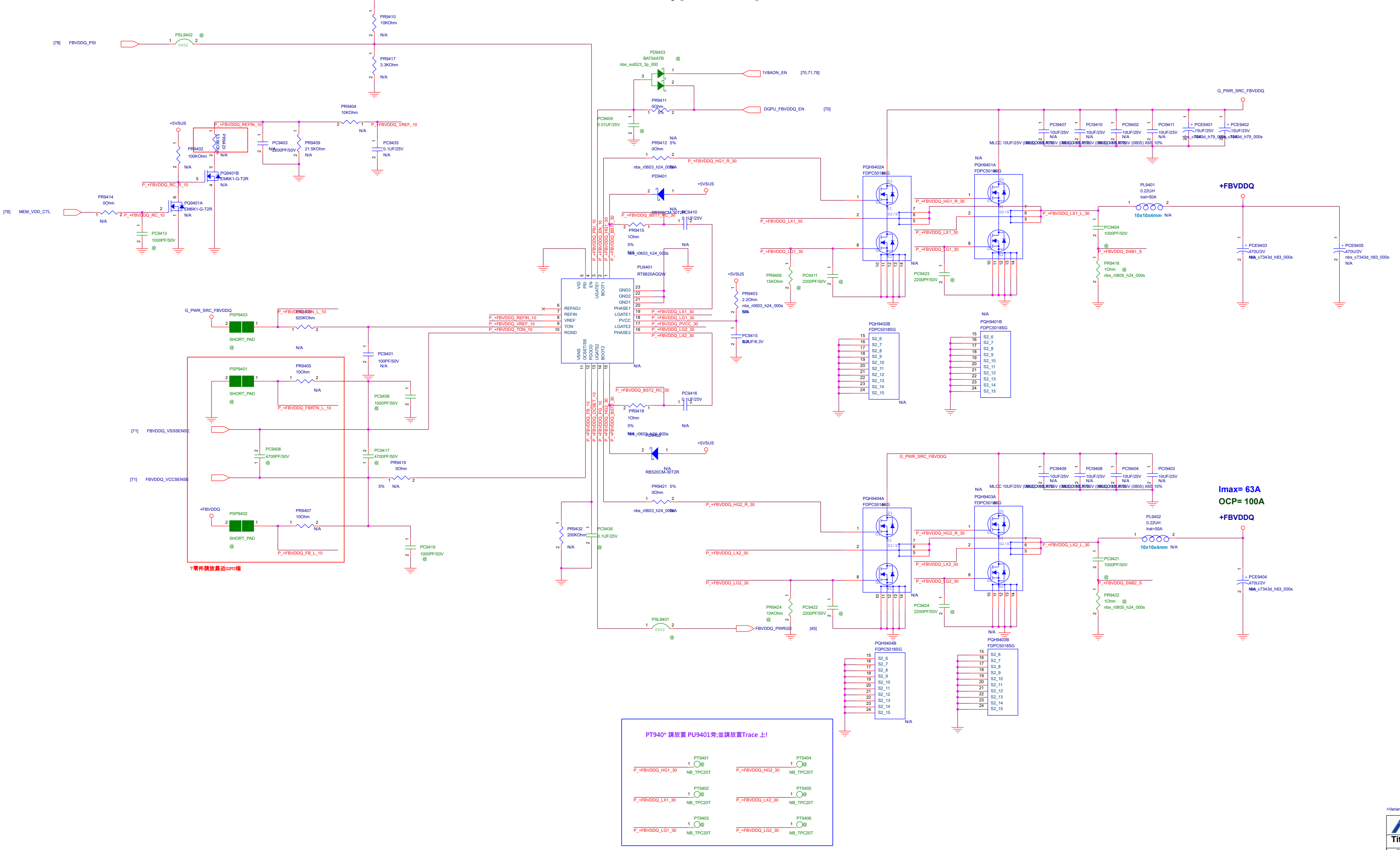


+FBVDDQ [For VRAM]

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.25V
PR9404	10KOhm	
PR9409	21.5KOhm	
PR9423	75KOhm	

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.2V
PR9404	10KOhm	
PR9409	21.5KOhm	
PR9423	53.6KOhm	

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.25V	1.2V
PR9404	10KOhm	
PR9409	16.9KOhm	
PR9423	140KOhm	



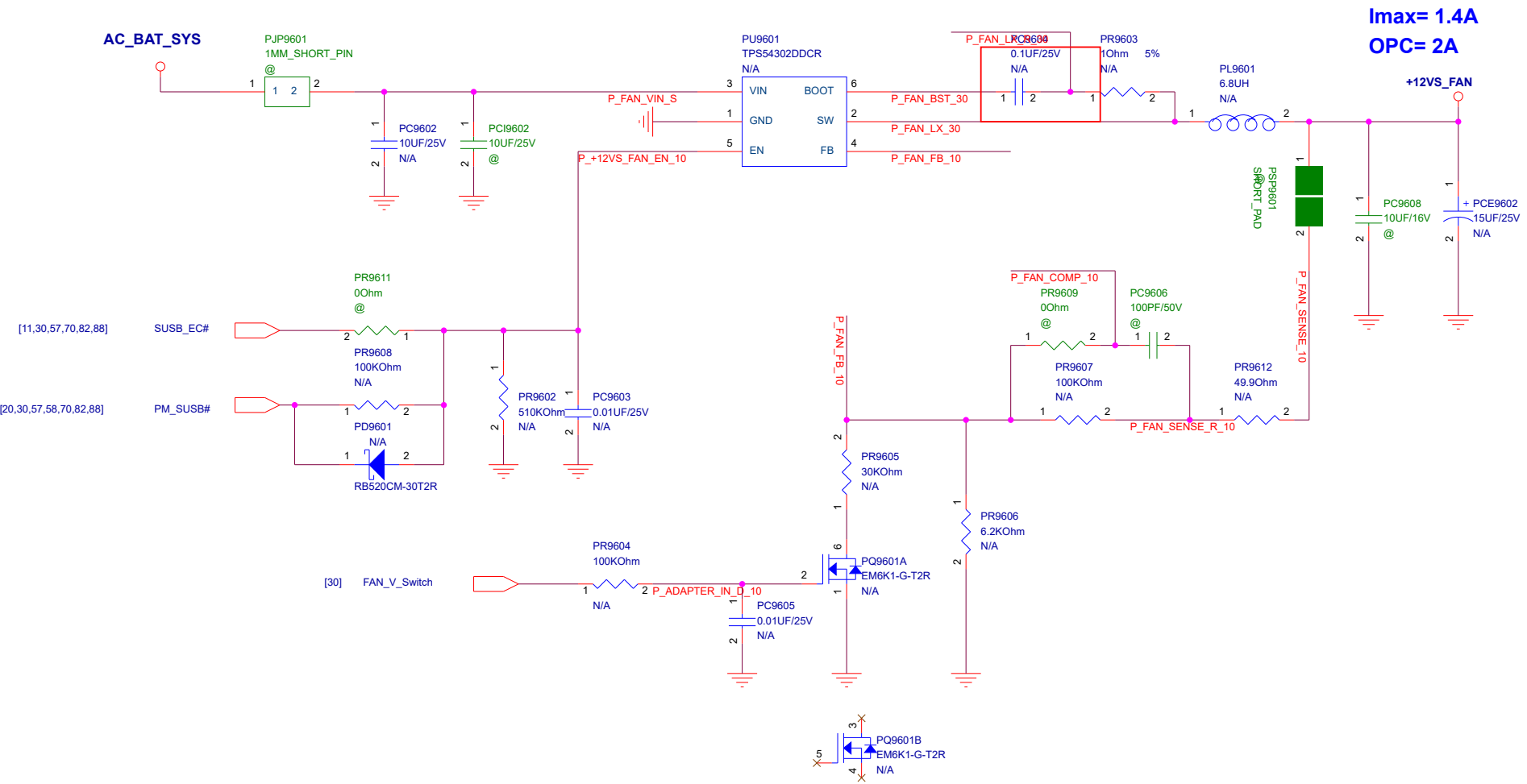
<Variant Name>

Project Name: GM531GX		Rev: R1.0
Title : PW_+FBVDDQ		
Size: Custom	Dept.: NB Power Team	Engineer: Joe
Date: Friday, February 21, 2020	Sheet 94 of 103	

<Core Design>

ASUSTeK COMPUTER	Title : OTH_for test only	
	Engineer: EE	
Size: A	Project Name: GX502GX	Rev: R1.2
Date: Friday, February 21, 2020	Sheet 95 of 99	

+12VS_FAN [For FAN]



<Variant Name>

Project Name: Project Name		Rev: R1.0
Title : PW_+12VS_FAN		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Friday, February 21, 2020	Sheet 96 of 103	

<Core Design>

Title : OTH_for test only

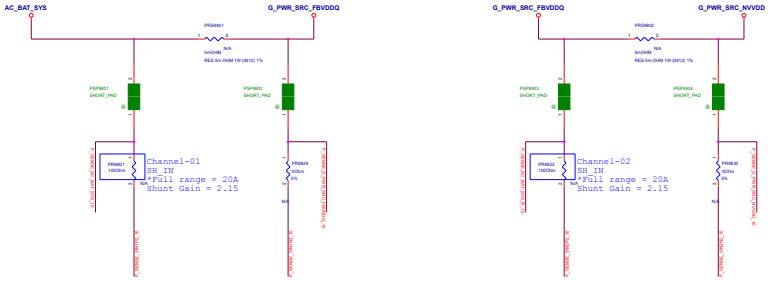
ASUSTeK COMPUTER

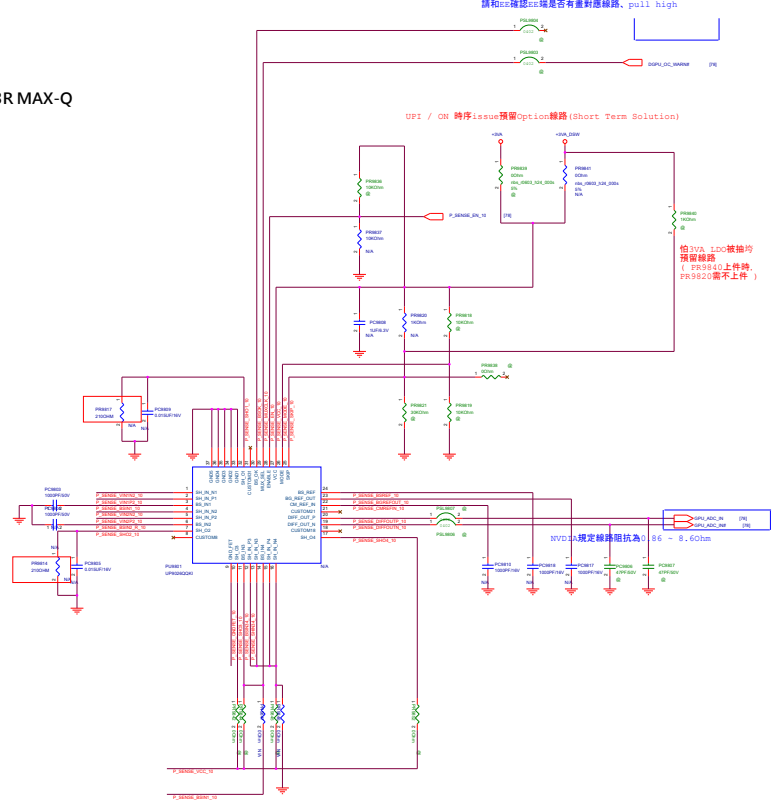
Engineer: EE

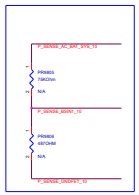
Size	Project Name	Rev
A	GX502GX	R1.2

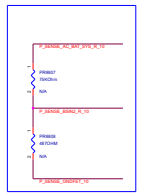
Date:	Friday, February 21, 2020	Sheet	97	of	99

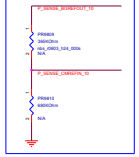
N18E-G3R MAX-Q

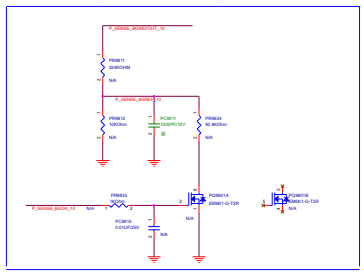












N18E

N18E-G3/N18E-G3R

	UP9026PQKI(UPI)
PR9801	100Ω(10G2121000140l0)
PR9817	124Ω (10G2121240140l0)
PR9822	100Ω(10G2121000140l0)
PR9814	124Ω (10G2121240140l0)
PR9805	75kΩ(10G2127502140l0)
PR9806	487Ω (10G2124870140l0)
PR9807	75kΩ(10G2127502140l0)
PR9808	487Ω (10G2124870140l0)
PR9811	324kΩ (10G2123243140l0)
PR9812	10kΩ(10G2121002140l0)
PR9834	90.9kΩ(10G2129092140l0)

N18E-G2/N18E-G2R
N18E-G1R

	UP9026PQKI(UPI)
PR9817	140Ω (10G2121400140l0)
PR9814	140Ω (10G2121400140l0)

N18E-G0
N18E-G1
N18E-G3R MAX-Q
N18E-G2R MAX-Q
N18E-G1R MAX-Q

	UP9026PQKI(UPI)
PR9817	210Ω (10G2122100140l0)
PR9822	
PR9814	210Ω (10G2122100140l0)

N18E-G0 MAX-Q

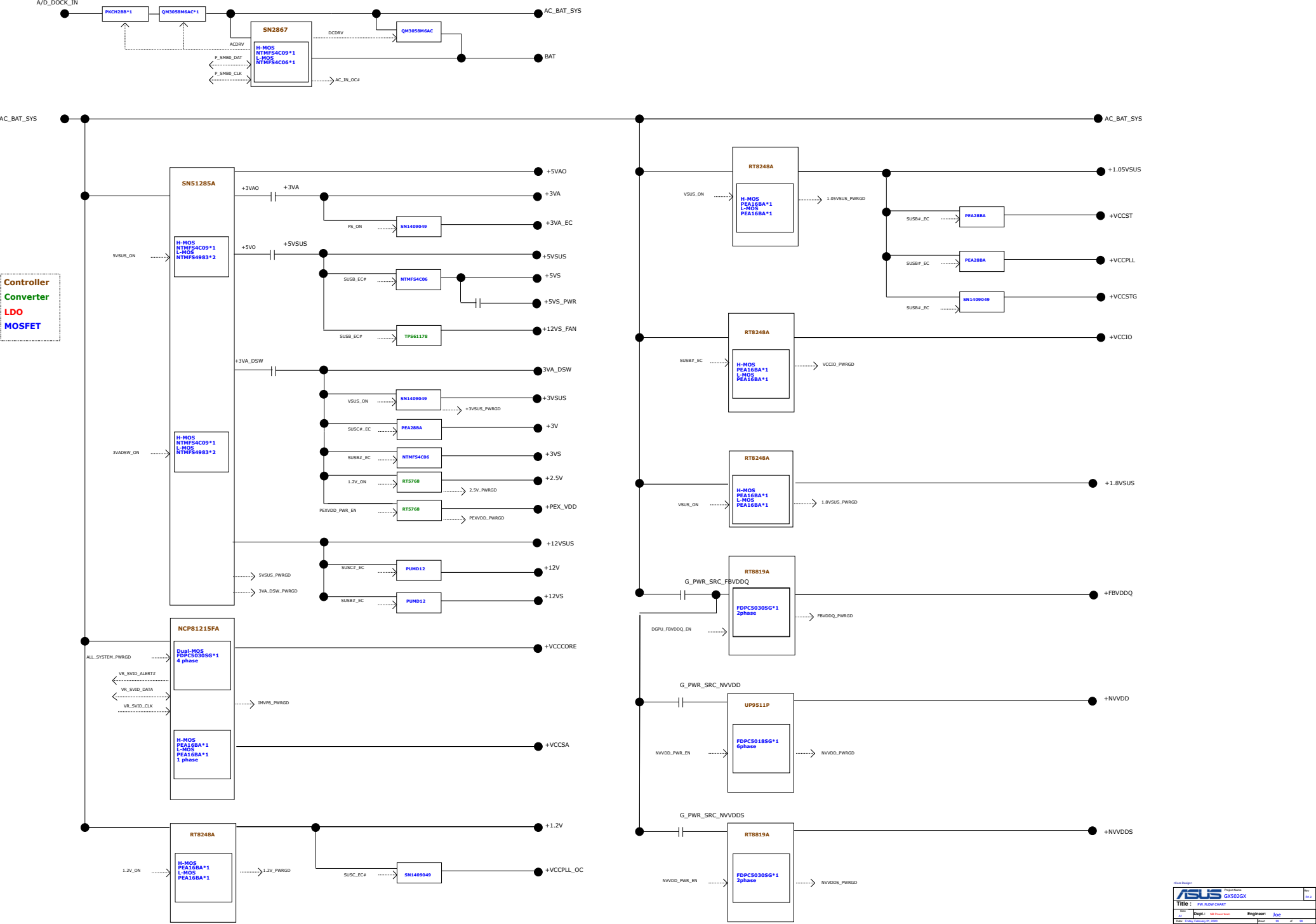
	UP9026PQKI(UPI)
PR9817	348Ω (10G2123480140l0)
PR9822	
PR9814	348Ω (10G2123480140l0)

N18P

	UP9026PQKI(UPI)
PR9801	100Ω(10G2121000140l0)
PR9817	348Ω (10G2123480140l0)
PR9822	100Ω(10G2121000140l0)
PR9814	348Ω (10G2123480140l0)
PR9805	75kΩ(10G2127502140l0)
PR9806	487Ω (10G2124870140l0)
PR9807	75kΩ(10G2127502140l0)
PR9808	487Ω (10G2124870140l0)
PR9811	324kΩ (10G2123243140l0)
PR9812	10kΩ(10G2121002140l0)
PR9834	90.9kΩ(10G2129092140l0)

N18P-G0-MP
N18P-G0-MP MAX-Q
N18P-G0-Q13 MAX-Q
N18P-G62
N18P-G62 MAX-Q
N18P-G61
N18P-G61 MAX-Q

ASUS GM531GX
Title : PWR_SPC
Dept.: Power Team
Engineer: Joe
Date: Friday, February 21, 2020

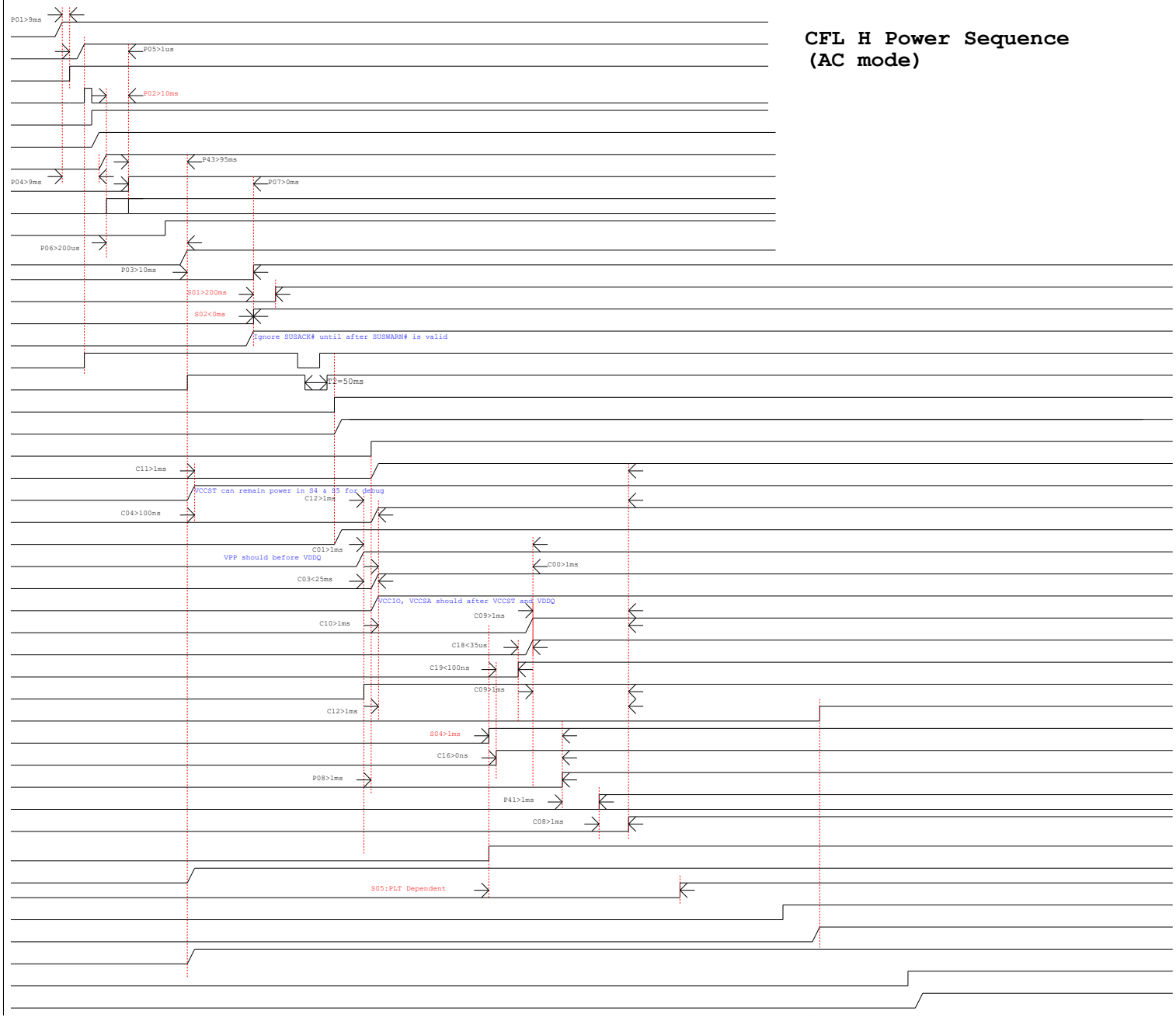

A/D_DOCK_IN
PKCH2BB*1
QM30S8M6AC*1
AC_BAT_SYS
SN2867
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4C06*1
ACDRV
DCDRV
QM30S8M6AC
BAT
P_SMB0_DAT
P_SMB0_CLK
AC_IN_OC#
AC_BAT_SYS
AC_BAT_SYS
Controller
Converter
LDO
MOSFET
SN51285A
+5VAO
+3VAO
+3VA
+3VA
PS_ON
SN1409049
+3VA_EC
5VSUS_ON
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4983*2
+5VO
+5VSUS
+5VSUS
SUSB_EC#
NTMFS4C06
+5VS
+5VS_PWR
SUSB_EC#
TPS61178
+12VS_FAN
+3VA_DSW
3VA_DSW
VSUS_ON
SN1409049
+3VSUS_PWRGD
+3VSUS
SUSC#_EC
PEA288A
+3V
3VADSW_ON
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4983*2
SUSB#_EC
NTMFS4C06
+3VS
1.2V_ON
RT5768
2.5V_PWRGD
+2.5V
PEXVDD_PWR_EN
RT5768
PEXVDD_PWRGD
+PEX_VDD
+12VSUS
5VSUS_PWRGD
SUSC#_EC
PUMD12
+12V
3VA_DSW_PWRGD
SUSB#_EC
PUMD12
+12VS
NCP81215FA
Dual-MOS
FDPC5030SG*1
4 phase
ALL_SYSTEM_PWRGD
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
+VCCCORE
IMVP8_PWRGD
H-MOS
PEA168A*1
L-MOS
PEA168A*1
1 phase
+VCCSA
RT8248A
H-MOS
PEA168A*1
L-MOS
PEA168A*1
1.2V_ON
1.2V_PWRGD
+1.2V
SUSC_EC#
SN1409049
+VCCPLL_OC
AC_BAT_SYS
RT8248A
VSUS_ON
H-MOS
PEA168A*1
L-MOS
PEA168A*1
1.05VSUS_PWRGD
+1.05VSUS
SUSB#_EC
PEA288A
+VCCST
SUSB#_EC
PEA288A
+VCCPLL
SUSB#_EC
SN1409049
+VCCSTG
RT8248A
SUSB#_EC
H-MOS
PEA168A*1
L-MOS
PEA168A*1
VCCIO_PWRGD
+VCCIO
RT8248A
VSUS_ON
H-MOS
PEA168A*1
L-MOS
PEA168A*1
1.8VSUS_PWRGD
+1.8VSUS
RT8819A
G_PWR_SRC_FBVDDQ
FDPC5030SG*1
2phase
DGPU_FBVDDQ_EN
FBVDDQ_PWRGD
+FBVDDQ
G_PWR_SRC_NVVDD
UP9511P
FDPC5018SG*1
6phase
NVVDD_PWR_EN
NVVDD_PWRGD
+NVVDD
G_PWR_SRC_NVVDDS
RT8819A
FDPC5030SG*1
2phase
NVVDD_PWR_EN
NVVDDS_PWRGD
+NVVDDS
ASUS
Project Name
GX502GX
Rev
0.1.2
Title :
PW_FLOW CHART
Dept.:
MB Power team
Engineer:
Joe
Friday, February 21, 2020

AC-IN Mode

CFL H Power Sequence (AC mode)

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(SUSB_EC#) +1.0V_VCCST, VCCPLL
(SUSB_EC#) +VCCIO, (+12VS) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



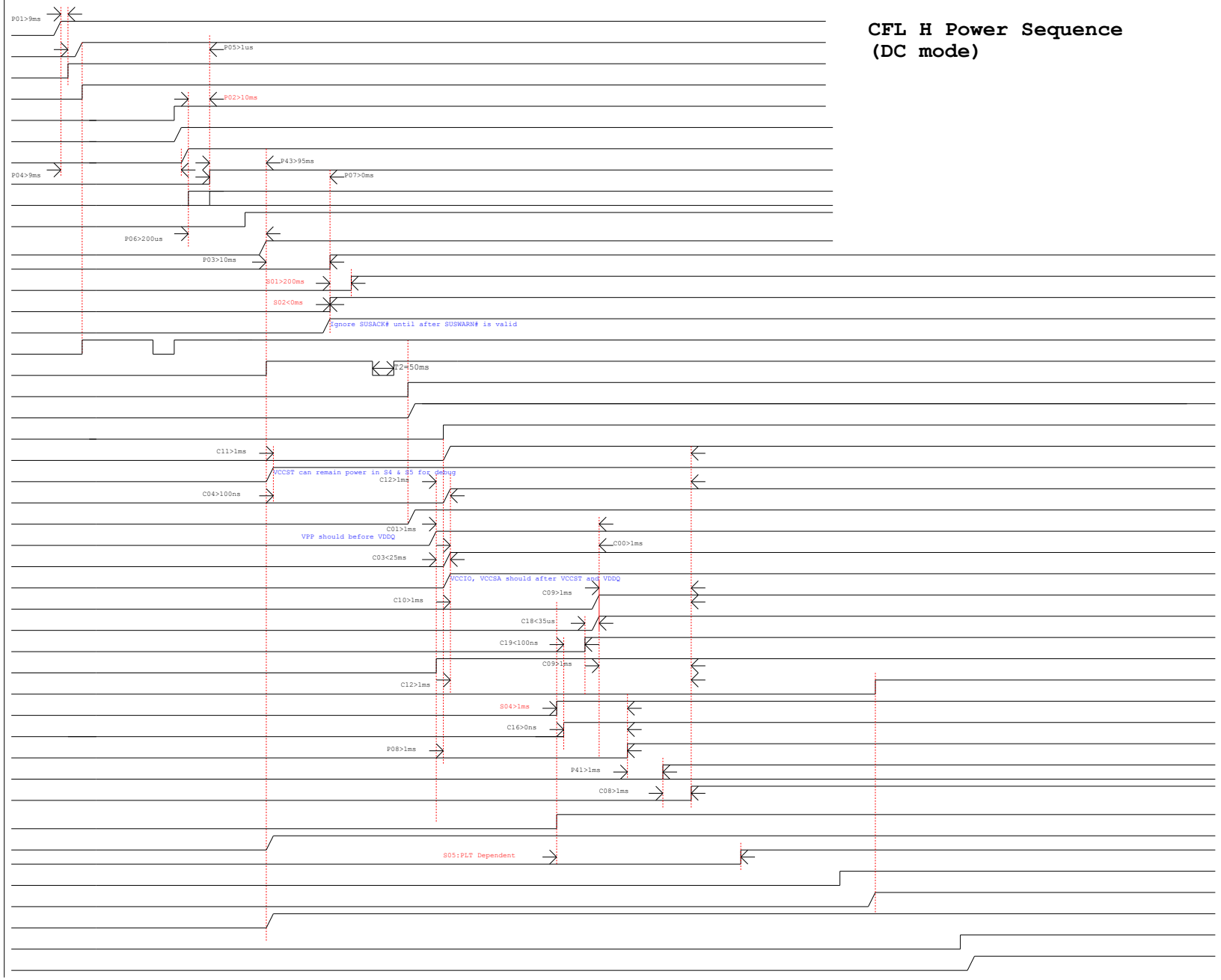
ASUS	Project Name: GX502GX		Rev: R1.2
Title : Power On Timing--AC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Friday, February 21, 2020	Sheet 100 of 99		

CFL H Power Sequence (DC mode)

DC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(VSUS_ON) +1.0V_VCCST,VCCPLL (VCCST_PWRGD)
(+VCCIO) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



ASUS	Project Name: GX502GX		Rev: R1.2
Title : Power On Timing-DC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: NB1 RD2 EE1	
Date: Friday, February 21, 2020	Sheet 101 of 99		

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

ASUSTeK COMPUTER INC.

Title : Revision History

Engineer: EE

Size: D | Project Name: GX502GX | Rev: R1.2

Date: Friday, February 21, 2020 | Sheet 102 of 99

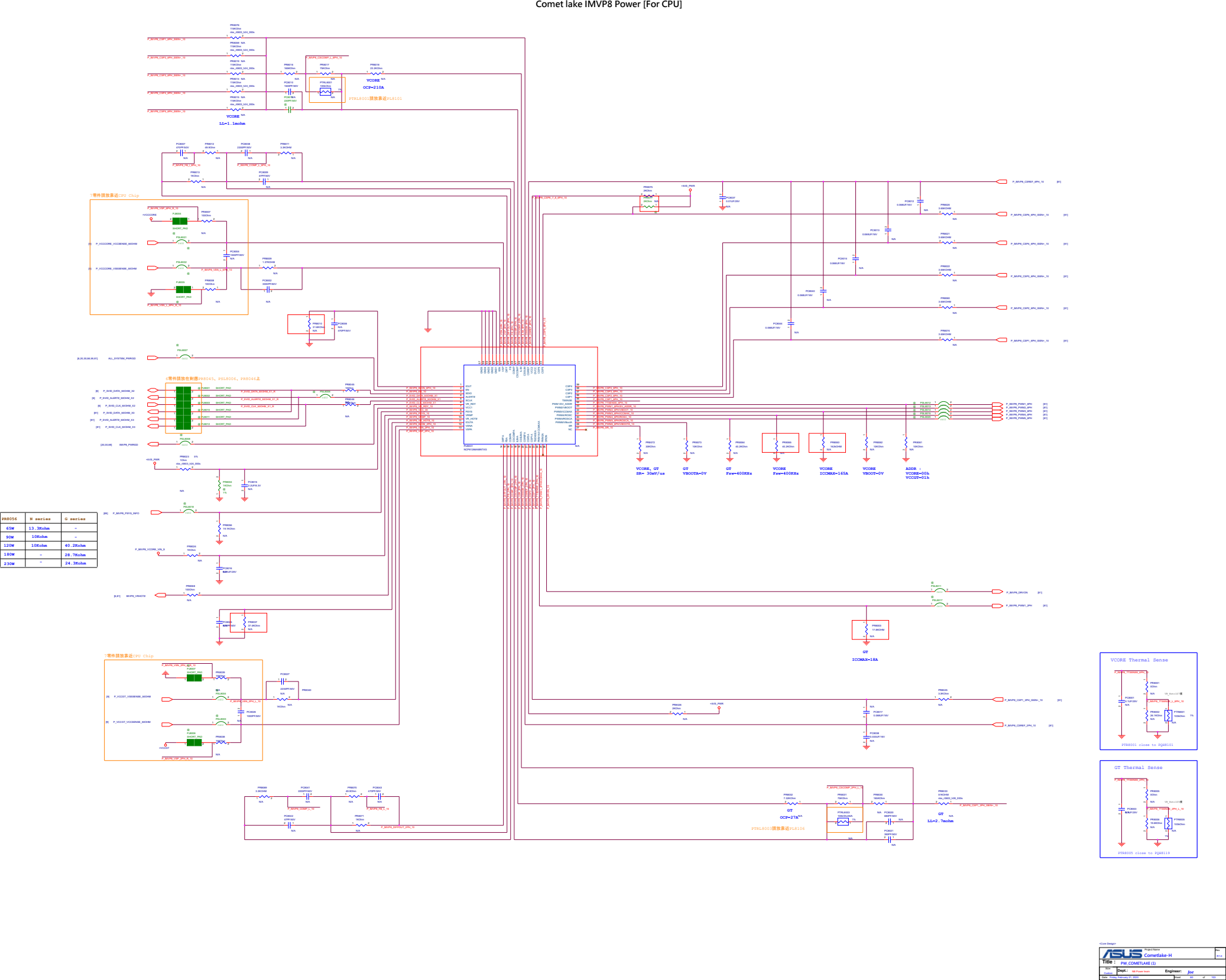
EE PART

GX502GX R1.1 SKU Table

			CPU	Power	DIMM	VRAM			
Option	PCB	SKU							

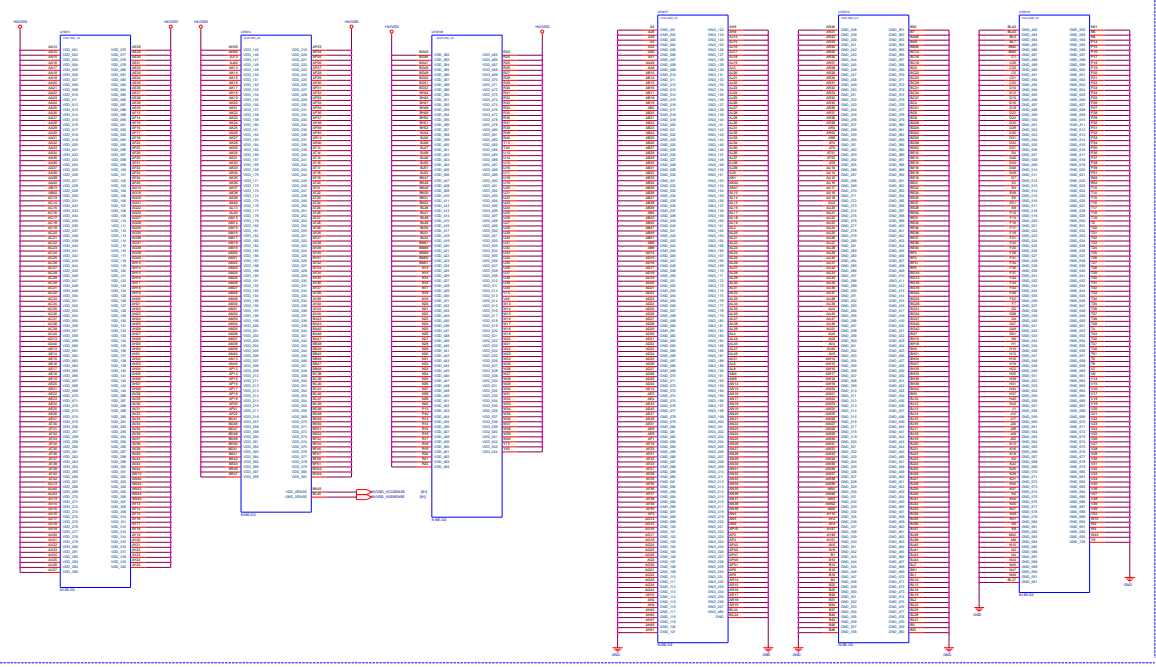
13. Audio Codec : 02043-00130000 (663-VA4)

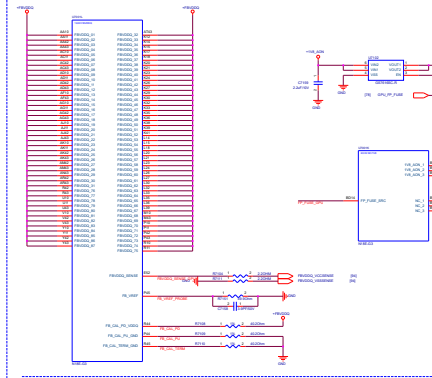
Comet lake IMVP8 Power [For CPU]



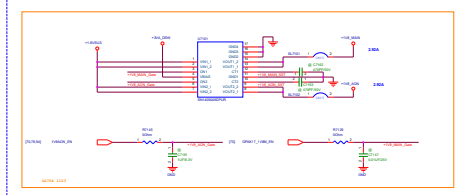
PN8056	H series	G series
65W	13.3Kohm	"
90W	10Kohm	"
120W	10Kohm	40.2Kohm
180W	"	28.7Kohm
230W	"	24.3Kohm

Project Name	Cometlake-H
Title :	PW_COMETLAKE (1)
Dept. :	NB Power team
Engineer:	Joe
Date:	Friday, February 21, 2020
Sheet	80 of 103

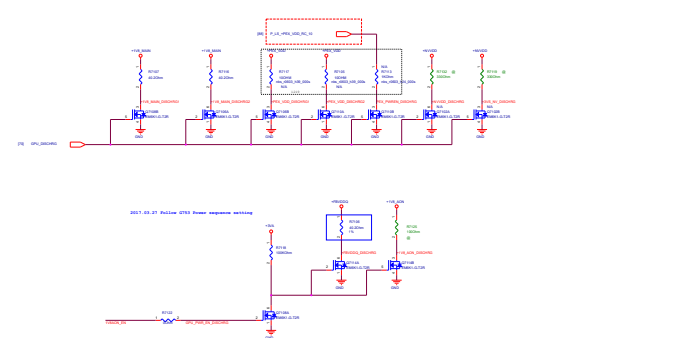


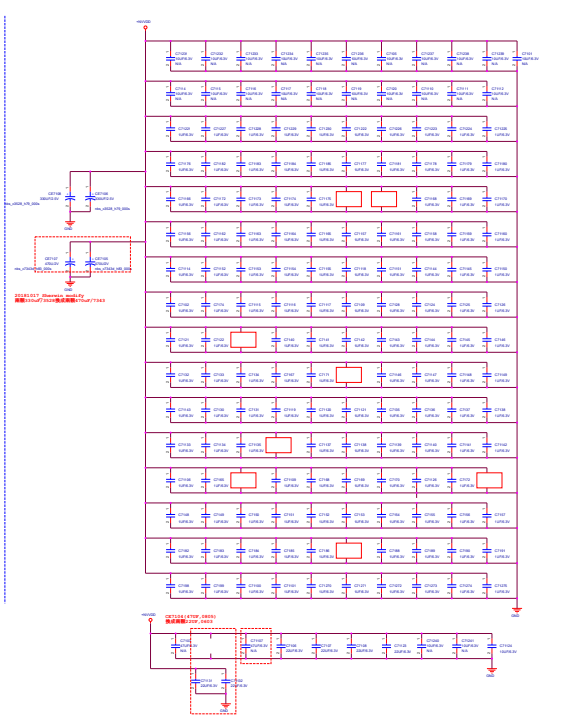


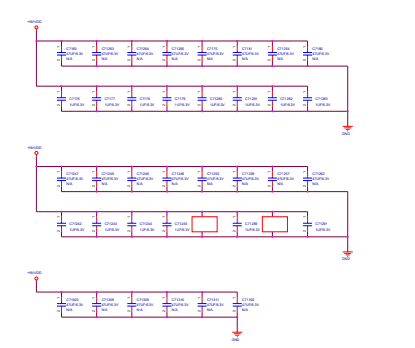
1V8 & 3V3 Power Control

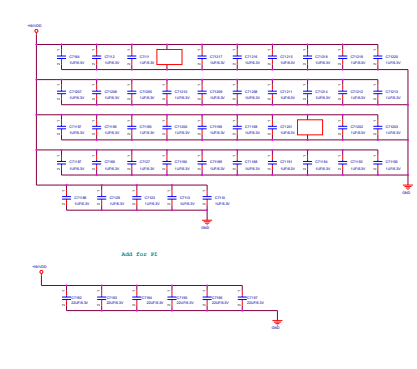


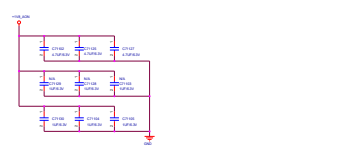
Discharge





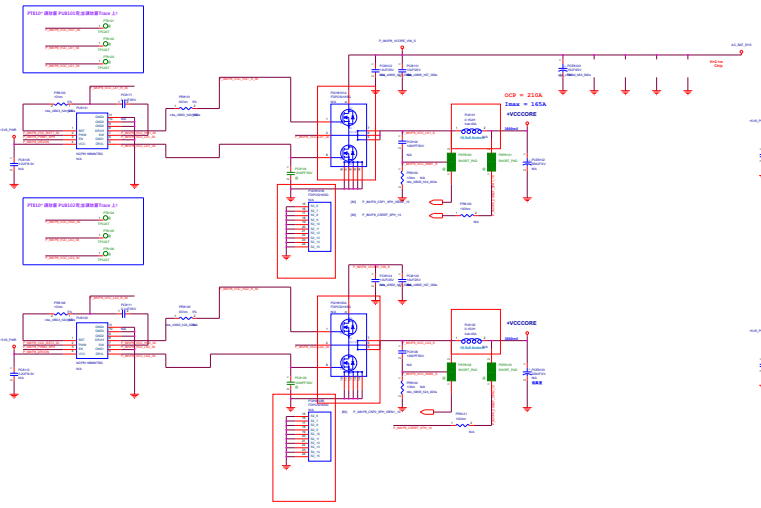


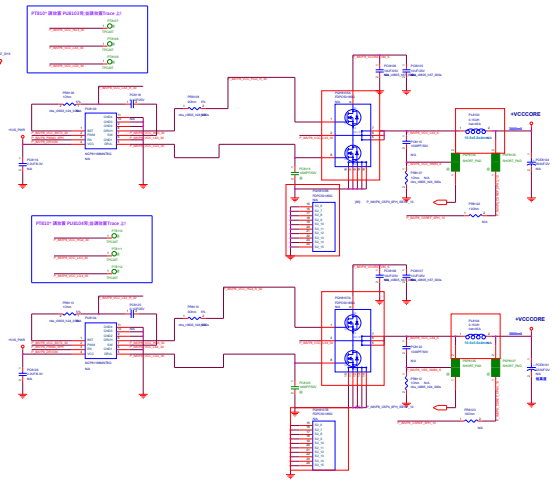


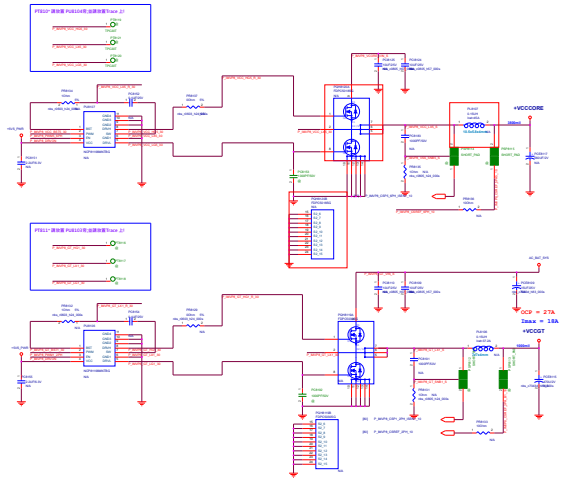


Add for PI

ASUS	Project Name: GX503GX		Rev: 0.2
Title: GPU POWER			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Friday, February 21, 2020		Sheet 71 of 98	


OCP = 210A
Imax = 165A
+VCCCORE

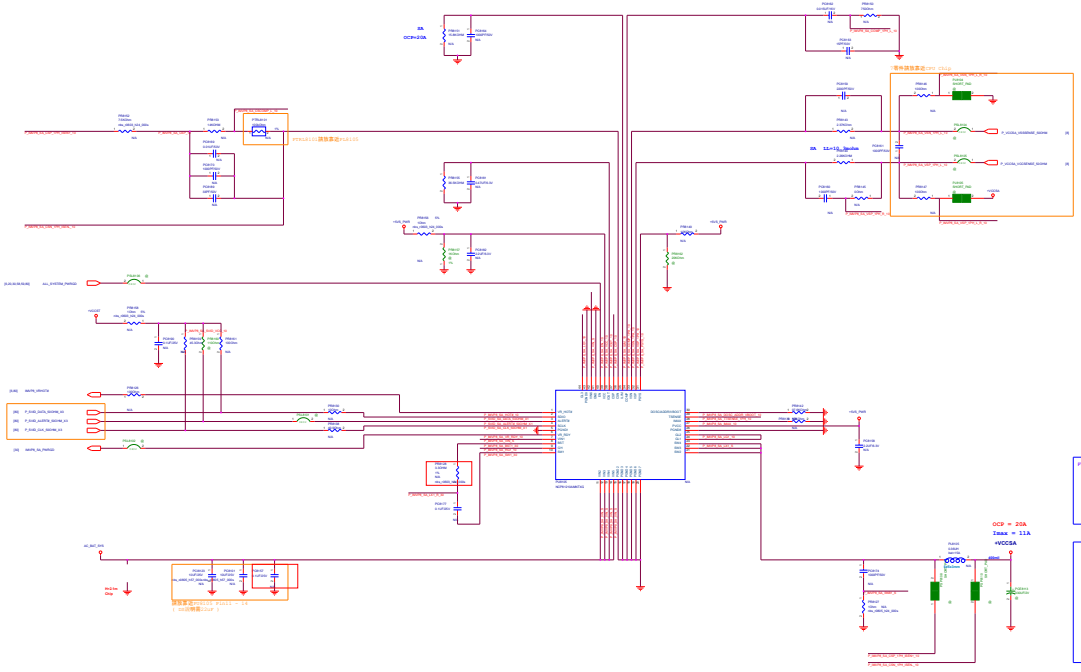

+VCCCORE

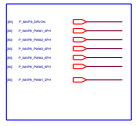

+VCCCORE

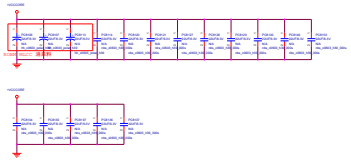
+VCCCORE

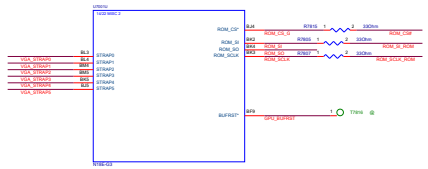
+VCCCORE

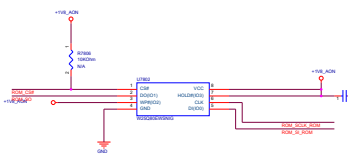
OCP = 27A
Imax = 18A
+VCCGT

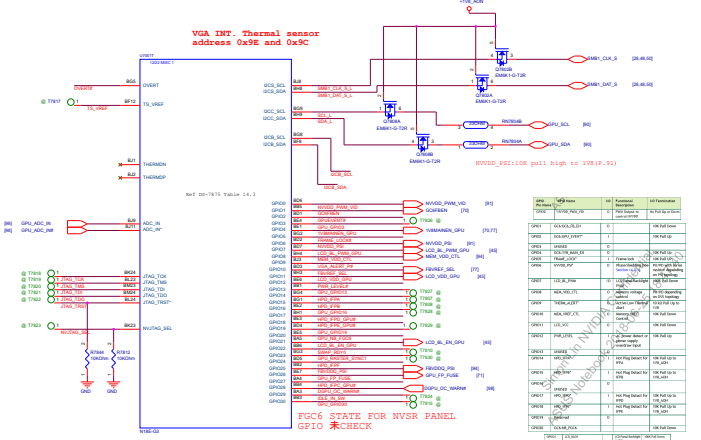

OCP=210A
OCP = 20A
Imax = 11A
+VCCSA
SA Thermal Sense

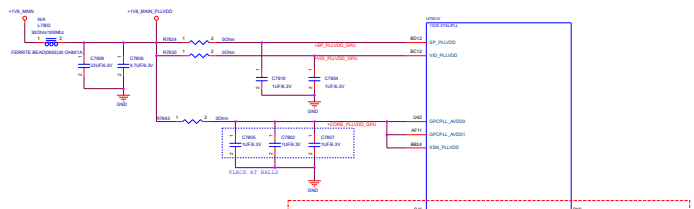


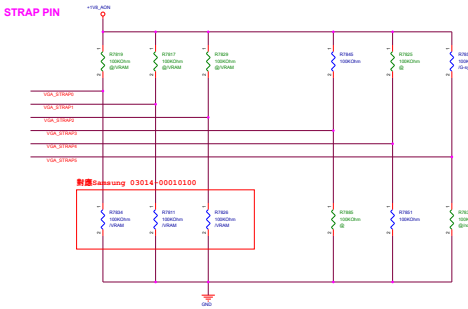

VCCGT
470uF x 1
22uF x 10
VCCSA
22uF x 5

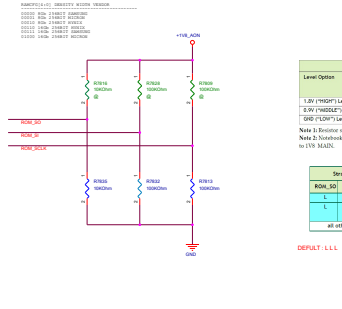










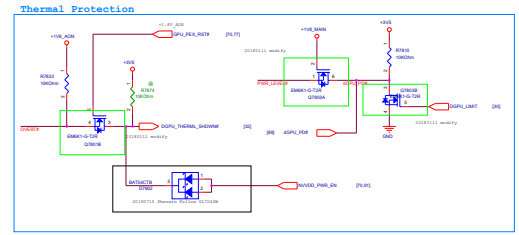


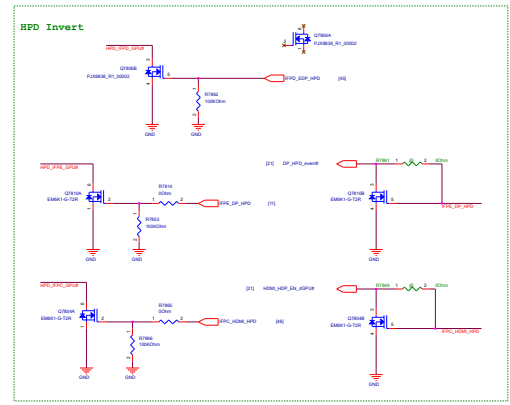
Physical Configuration		
Level Option	Pull-Up to 1.8V via resistor (see Note 1). (Notebook designs also see Note 2.)	Pull-Down to GND via resistor Note 1
1.8V ("HIGH") Level	Populate	No Stuff
0.9V ("MIDDLE") Level	Populate	Populate
GND ("LOW") Level	No Stuff	Populate

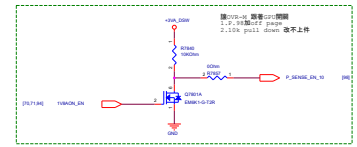
Note 1: Resistor should be 10K Ohms. 5% tolerance is acceptable.
Note 2: Notebook graphics circuit designs should pull up to the 1V8_AON rail rather than to 1V8 MAIN.

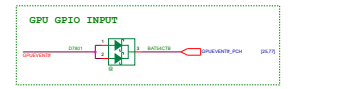
Strap Pins see Note			FS_OVERT Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT function ENABLED
L	L	H	FS_OVERT function DISABLED (Notebook: do not configure)
all other configurations			(Invalid: do not configure)

DEFULT : L L L









Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
M	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	1	1
L	H	L	0	0	0	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	1	1
H	H	L	0	1	0	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	L	M	1	0	1	1
L	M	L	1	0	0	0
L	M	H	1	0	1	1
L	H	M	1	1	0	0
M	L	L	1	1	0	0
M	L	H	1	1	1	1
M	H	L	1	1	0	0
M	H	H	1	1	1	1

Assorted Configuration Straps.
1. SMB_ALT_ADDR Enable - "0" signal GPU setting I2C address 0x9E, "1" Dual GPU setting I2C address add 0x9C, used when a second GPU
2. DEVID_SEL: G-sync function --"0" normal GPU ID, "1" support G-sync GPU ID.
3. PCIE_CFG: PCIE Swing --"0" PCIE Swing default, "1" PCEI swing reduce.
4. VGA_DEVICE: Graphics circuit --"0" MS-Hybrid, "1" Discrete.

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

DEFULT : L L H

ASUS	Project Name: GX502GX	Rev: R1.2
Title : GPU_CLOCK/STRAP/GPIO		
Size: Custom	Dept.: ASUSTEK COMPUTER INC	Engineer: EE
Date: Friday, February 21, 2020	Sheet: 78 of 90	