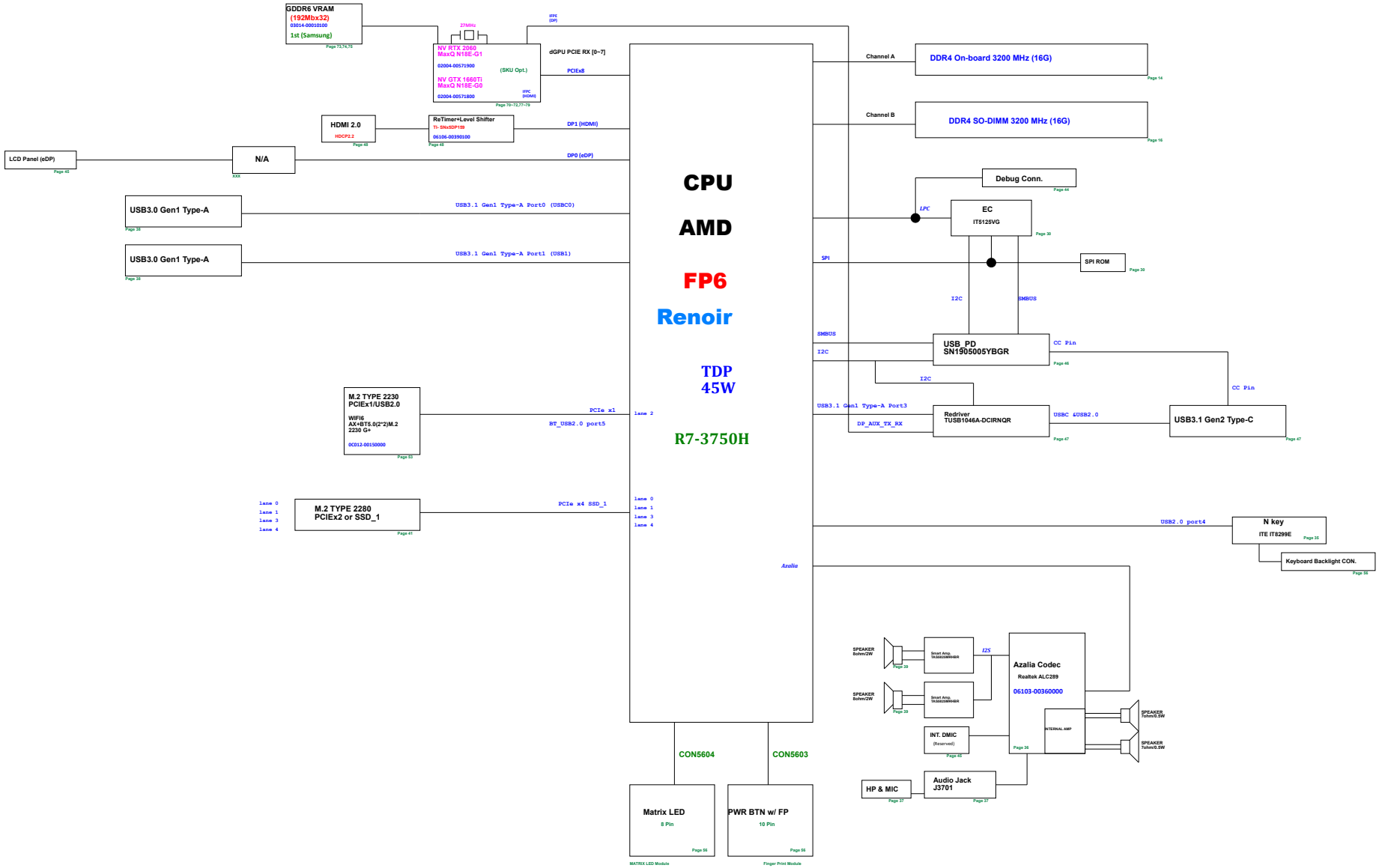
GA401IV/IU AMD+NVIDIA Block Diagram



Project Name	GA401
Rev	PG 0
Title	CFL-H_Block Diagram_R1.3B
Size	Custom
Dept.	ASUSTeK COMPUTER INC.
Engineer	NB1 RD2 EE1
Date	Tuesday, February 11, 2020
Sheet	1 of 106

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	RCIN#	Native	RC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	GPO	(N.C)			
GPP_A12	GPI	GPO	(N.C)			
GPP_A13	SUSWANRN#	Native	ME_SusPwrDnAck		PU 10K(@)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPO	(N.C)			
GPP_A17	GPI	GPO	(N.C)			
GPP_A18	GPI	GPO	(N.C)			
GPP_A19	GPI	GPO	(N.C)			
GPP_A20	GPI	GPO	(N.C)			
GPP_A21	GPI	GPO	TBTA_MRESET(Reserved)			
GPP_A22	GPI	GPO	PCH_RTD3_CIO_PWR_EN		PU 10K	+VCC3V3_SX
GPP_A23	GPI	GPO	PCH_RTD3_USB_PWR_EN		PD 100K	

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPI	GPI	TBT_I2C_INT_PCH		PU 10K	+3VSUS
GPP_B2	GPI	GPO	(N.C)			
GPP_B3	GPI	GPO	(N.C)			
GPP_B4	GPI	GPO	(N.C)			
GPP_B5	GPI	Native	CLK_REQ0#/CLKREQ0_PEGA#		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K(@)	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#/CLKREQ2_WLAN_AC#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLK_REQ3#		PU 10K(@)	+3VSUS
GPP_B9	GPI	Native	CLK_REQ4#/CLKREQ4_GLAN#		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLK_REQ5#/CLKREQ5_TBT #		PU 10K	+3VSUS
GPP_B11	GPO	GPO	(N.C)			
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPPB14	PD		
GPP_B15	GPI	GPI	PCH_GPPB15/KB_LANG_ID0		PU 10K	+3VS
GPP_B16	GPI	GPI	PCH_GPPB16/KB_LANG_ID1		PU 10K	+3VS
GPP_B17	GPI	GPO	PCH_GPPB17/XBOX_WRST		PD 10K	
GPP_B18	GPO	Strap	PCH_GPPB18	PD		
GPP_B19	GPI	GPO	PCH_GPPB19/BT_ON_PCH		PD 10K(@)	
GPP_B20	GPI	GPO	PCH_GPPB20/GPUEVENT#_PCH		PU 10K	+3VSUS
GPP_B21	GPI	GPI	PCH_GPPB21/GC6FBEN_PCH		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPPB22	PD		
GPP_B23	GPO	Native	SML1ALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	GPI	GPP_C2_BT_UART_WAKE_N	PD	PU 4.7K	+3VSUS
GPP_C3	SML0CLK	Native	SML0_CLK (Reserved)		PU 2.2K	+3VSUS
GPP_C4	SML0DATA	Native	SML0_DAT (Reserved)		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		
GPP_C6	SML1CLK	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	SML1DATA	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPO	(N.C)			
GPP_C9	GPI	GPO	(N.C)			
GPP_C10	GPI	GPO	(N.C)			
GPP_C11	GPI	GPO	(N.C)			
GPP_C12	GPI	GPI	DIMM_SEL0			
GPP_C13	GPI	GPI	DIMM_SEL1			
GPP_C14	GPI	GPI	DIMM_SEL2			
GPP_C15	GPI	GPI	NFC_ID		PU 10K	+3VSUS
GPP_C16	GPI	Native	TBT_I2C_SDA_PCH		PU 2.2K	+3VSUS
GPP_C17	GPI	Native	TBT_I2C_SCL_PCH		PU 2.2K	+3VSUS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PU 10K	+3VS_NV
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	(N.C)			
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPO	(N.C)			
GPP_D1	GPI	GPO	(N.C)			
GPP_D2	GPI	GPO	(N.C)			
GPP_D3	GPI	GPO	(N.C)			
GPP_D4	GPI	GPO	(N.C)			
GPP_D5	GPI	Native3	PCH_GPPD5/M.2_BT_PCMFRM_CRF_RST_N		PD 75K	
GPP_D6	GPI	Native3	PCH_GPPD6/M.2_BT_PCMOUT_CLKREQ0		PD 75K(@)	
GPP_D7	GPI	GPO	PCH_GPPD7/M.2_BT_PCMIN		PD 100K(@)	
GPP_D8	GPI	GPO	PCH_GPPD8/M.2_BT_PCMCLK			
GPP_D9	GPI	GPO	(N.C)			
GPP_D10	GPI	GPO	(N.C)			
GPP_D11	GPI	GPO	(N.C)			
GPP_D12	GPI	GPO	(N.C)			
GPP_D13	GPI	GPO	(N.C)			
GPP_D14	GPI	GPO	(N.C)			
GPP_D15	GPI	GPO	(N.C)			
GPP_D16	GPI	GPO	(N.C)			
GPP_D17	GPI	GPO	(N.C)			
GPP_D18	GPI	GPO	(N.C)			
GPP_D19	GPI	GPO	(N.C)			
GPP_D20	GPI	GPO	(N.C)			
GPP_D21	GPI	GPO	(N.C)			
GPP_D22	GPI	GPO	(N.C)			
GPP_D23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	Native	SATAPCIE_DET0		PU 10K(@)	+3VS
GPP_E1	GPI	Native	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	Native	SATAPCIE_DET2		PU 10K(@)	+3VS
GPP_E3	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_E4	GPI	Native	SATA0_HDD1_DEVSLP		PU 10K(@)	+3VS
GPP_E5	GPI	Native	SATA1_NGFF3_DEVSLP		PU 10K(@)	+3VS
GPP_E6	GPI	Native	NGFF3_DEVSLP		PU 10K(@)	+3VSUS
GPP_E7	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_E8	GPI	Native	SATA_LED#		PU 10K	+3VS
GPP_E9	GPI	Native	USB_OC#0		PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1		PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2		PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3		PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	Native	SATAPCIE_DET3		PU 10K(@)	+3VS
GPP_F1	GPI	Native	SATAPCIE_DET4		PU 10K	+3VS
GPP_F2	GPI	GPO	(N.C)			
GPP_F3	GPI	GPO	(N.C)			
GPP_F4	GPI	GPO	(N.C)			
GPP_F5	GPI	GPO	(N.C)			
GPP_F6	GPI	GPO	(N.C)			
GPP_F7	GPI	GPO	(N.C)			
GPP_F8	GPI	GPO	(N.C)			
GPP_F9	GPI	GPO	(N.C)			
GPP_F10	GPI	GPO	(N.C)			
GPP_F11	GPI	GPO	(N.C)			
GPP_F12	GPI	GPO	(N.C)			
GPP_F13	GPI	GPO	(N.C)			
GPP_F14	GPI	GPO	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	GPO	(N.C)			
GPP_F20	GPI	GPO	(N.C)			
GPP_F21	GPI	GPO	(N.C)			
GPP_F22	GPI	GPO	(N.C)			
GPP_F23	GPI	GPO	PCH_GPPF23		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPO	(N.C)			
GPP_G1	GPI	GPO	(N.C)			
GPP_G2	GPI	GPO	(N.C)			
GPP_G3	GPI	GPO	(N.C)			
GPP_G4	GPI	GPO	(N.C)			
GPP_G5	GPI	GPO	(N.C)			
GPP_G6	GPI	GPO	(N.C)			
GPP_G7	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLK_REQ6#/CLKREQ6_NGFF1#		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLK_REQ7#/CLKREQ7_NGFF2#		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#/CLKREQ8_NGFF3#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K(@)	+3VSUS
GPP_H4	GPI	Native	CLK_REQ10#		PU 10K(@)	+3VSUS
GPP_H5	GPI	Native	CLK_REQ11#		PU 10K(@)	+3VSUS
GPP_H6	GPI	Native	CLK_REQ12#		PU 10K(@)	+3VSUS
GPP_H7	GPI	Native	CLK_REQ13#		PU 10K(@)	+3VSUS
GPP_H8	GPI	Native	CLK_REQ14#		PU 10K(@)	+3VSUS
GPP_H9	GPI	Native	CLK_REQ15#		PU 10K(@)	+3VSUS
GPP_H10	GPI	GPO	(N.C)			
GPP_H11	GPI	GPO	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD	PD 20K(@)	
GPP_H13	GPI	GPO	(N.C)			
GPP_H14	GPI	GPO	(N.C)			
GPP_H15	GPI	GPO	SML3ALERT#		PU 100K	+3VSUS
GPP_H16	GPI	GPI	KBID_0			
GPP_H17	GPI	GPI	KBID_1			
GPP_H18	GPI	GPI	KBID_2			
GPP_H19	GPI	GPO	(N.C)			
GPP_H20	GPI	GPO	(N.C)			
GPP_H21	GPI	GPO	(N.C)			
GPP_H22	GPI	GPO	(N.C)			
GPP_H23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	GPO	(N.C)			
GPP_I1	GPI	GPO	(N.C)			
GPP_I2	GPI	GPO	(N.C)			
GPP_I3	GPI	GPO	(N.C)			
GPP_I4	GPI	GPO	EDP_HPD		PD 100K	
GPP_I5	GPI	GPO	(N.C)			
GPP_I6	GPO	GPO	(N.C)			
GPP_I7	GPI	GPO	(N.C)			
GPP_I8	GPO	GPO	(N.C)			
GPP_I9	GPI	GPO	(N.C)			
GPP_I10	GPO	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_J0	GPI	GPO	(N.C)			
GPP_J1	CPU_VCCIO_PWR_GATE#	Native	CPU_C10_GATE#_PCH		PU 100K	+1.8VSUS
GPP_J2	GPI	GPO	(N.C)			
GPP_J3	GPI	GPO	(N.C)			
GPP_J4	CNV_BRI_DT	Native	CNV_BRI_DT		PU 4.7K	+1.8VSUS
GPP_J5	CNV_BRI_RSP	Native	CNV_BRI_RSP		PU 20K(@)	+1.8VSUS
GPP_J6	CNV_RGI_DT	Native	CNV_RGI_DT		PD 75K	
GPP_J7	CNV_RGI_RSP	Native	CNV_RGI_RSP		PU 20K(@)	+1.8VSUS
GPP_J8	GPI	GPO	(N.C)			
GPP_J9	GPO	GPO	(N.C)			
GPP_J10	GPI	GPO	(N.C)			
GPP_J11	A4WP_PRESENT	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_K0	GPI	GPO	GPIO_3_FORCE_PWR		PD 100K	
GPP_K1	GPI	GPI	PCB_ID0		PD 10K	
GPP_K2	GPI	GPI	PCB_ID1		PD 10K	
GPP_K3	GPI	GPO	GPP_K3/WLAN_BT_LED		PD 100K	
GPP_K4	GPI	GPO	GPP_K4/WLAN_LED		PD 100K	
GPP_K5	GPI	GPO	VOL_DOWN#(N.C)			
GPP_K6	GPI	GPO	VOL_UP#(N.C)			
GPP_K7	GPI	GPO	GPP_K7/TBT_HPD#		PU 10K	+3VS
GPP_K8	GPI	GPO	GPP_K8/DGPU_PWR_EN#		PU 10K(@)	+3VS
GPP_K9	GPI	GPO	WLAN_ON#		PD 100K	
GPP_K10	Reserved	GPO	GPP_K10/HDMI_HPD#		PU 10K	+3VS
GPP_K11	Reserved	GPO	GPP_K11/DP_HPD#		PU 10K	+3VS
GPP_K12	GPI	GPO	(N.C)			
GPP_K13	GPI	GPO	(N.C)			
GPP_K14	GPI	GPO	(N.C)			
GPP_K15	GPI	GPO	(N.C)			
GPP_K16	GPI	GPO	(N.C)			
GPP_K17	GPI	GPO	(N.C)			
GPP_K18	GPI	GPO	(N.C)			
GPP_K19	GPI	GPO	(N.C)			
GPP_K20	Reserved	GPO	(N.C)			
GPP_K21	Reserved	GPO	(N.C)			
GPP_K22	GPI	GPO	(N.C)			
GPP_K23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 10K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#(N.C)		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#		PD 100K	
GPD6	SLP_A#	Native	SLP_A# (N.C)			
GPD7	GPO	GPO	PCH_GPD7		PU 10K	+3VA_DSW
GPD8	SUSCLK	Native	SUS_CLK#			
GPD9	SLP_WLAN#	Native	SLP_WLAN# (N.C)			
GPD10	SLP_S5#	Native	SLP_S5# (N.C)			
GPD11	LANPHYPC	GPO	LAN_PWREN (N.C)		PU 10K(@)	+3VA_DSW

IT8225VG-128/BX GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#		
GPA2	OD	GPO	CHG_FULL_LED#		
GPA3	Alt	PWM	FAN2_PWM		
GPA4	O	GPO	EC_GPA4(N.C)		
GPA5	Alt	PWM	FAN1_PWM		
GPA6	Alt	GPO	EC_GPA6(N.C)		
GPA7	O	GPO	EC_GPA7(N.C)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	EC_GPB2(N.C)		
GPB3	Alt	GPI	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	EC_GPB5/NKey_WRST	PD 10K	
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	EC_GPC0		
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K(@)	+3VSUS
GPC4	I	GPI	EC_GPC4/PM_SUSB#	PD 100K	
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PD 100K	
GPC7	O	GPO	EC_GPC7/NKEY_PWR_EN	PD 10K(@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPO	EC_GPD0/EC_OV_DDR		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/OP_SD#		
GPD6	Alt	GPI	FAN1_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN2_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	5VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE4	O	GPO	VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE5	I	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPE6	OD	GPO	WLAN_PWR_EN	PD 100K	
GPE7	OD	GPO	THRO_CPU#	PU 10K	+3VA_DSW

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	CAP_LED#		
GPF1	O	GPO	NUM_LED#		
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_PECI	PD 10K(@)	
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2	PU 100K	+3VA_EC
GPG6	O	GPO	EC_GPG6(N.C)		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK/TBT_I2C_SCL_EC	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT/TBT_I2C_SDA_EC	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_RSMRST#	PD 10K	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#	PD 100K(@)	
GPI1	I	GPI	3VSUS_PWRGD	PU 100K	+3VSUS
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP8_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD_EC	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#	PU 10K(@)	+3VSUS
GPI6	Alt	AD	A/D_MAX_POWER		
GPI7	Alt	AD	MB_MAX_POWER	PU 100K&PD 270K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPO	EC_GPJ0		
GPJ1	O	GPI	GC6FBEN_PCH	PU 10K(@)	+3VS
GPJ2	Alt	GPI	EC_GPJ2/TBTA_I2C_INT_EC		
GPJ3	O	GPO	EC_GPJ3/USB_BC1.2_OFF#		
GPJ4	Alt	GPO	EC_GPJ4/USB30_5VBUS		
GPJ5	O	GPI	EC_GPJ5/MB_DOCK_JACK_DETECT	PU 100K(@)	+3VA
GPJ6	I	GPI	NKEY_INT#	PU 10K	+3VA_DSW_NKeyPWR
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ESCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

G703GI Source:

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	**SM-Bus Address**
SO-DIMM A(0)	A0h
SO-DIMM B(0)	A4h
SO-DIMM A(1)	A2h
SO-DIMM B(1)	A6h
EC Master (SMB1)	**SM-Bus Address**
SM-Bus Device	
GPU INT. Thermal sensor	9Eh, 9Ch
CPU Thermal Sensor	90h
TI_TAS5766M*2	98h, 9Ah
ASM1562	66h
GPU (Thermistor sense)	74h
PWR(Thermistor sense)	7Eh, 7Ch, 7Ah, 78h, 76h

Device Identification

CPU Thermal Senser		
1st	06G023123010	NCT7717U
2nd		

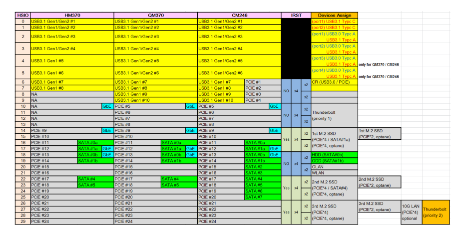
GPU Thermistor		
1st	06021-00260000	APL6002A8I-TRG
2nd		

USB3.0/PCIE/SATA Setting

1	USB3#1	
2	USB3#2	
3	USB3#3	USB Port1
4	USB3#4	
5	USB3#5	USB Port3
6	USB3#6	USB Port4
7	USB3#7	Card Reader
8	PCIE#2	
9	PCIE#3	
10	PCIE#4	
11	PCIE#5	ThunderBolt x4
12	PCIE#6	
13	PCIE#7	
14	PCIE#8	
15	PCIE#9	PCIE3.0 x 4 SSD
16	PCIE#10	
17	PCIE#11	
18	PCIE#12	
19	PCIE#13(SATA0B)	SATA HDD
20	PCIE#14(SATA1B)	
21	PCIE#15	GLAN
22	PCIE#16	WLAN_11AC
23	PCIE#17	PCIE3.0 x 4 SSD
24	PCIE#18	
25	PCIE#19	
26	PCIE#20	
27	PCIE#21	PCIE3.0 x 4 SSD
28	PCIE#22	
29	PCIE#23	
30	PCIE#24	

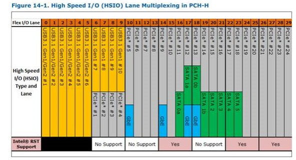
USB2.0 Setting

1	USB2#1	
2	USB2#2	
3	USB2#3	USB Port1
4	USB2#4	
5	USB2#5	USB Port3
6	USB2#6	USB Port4
7	USB2#7	Card Reader
8	USB2#8	XBOX WLAN
9	USB2#9	Camera
10	USB2#10	N-Key
11	USB2#11	
12	USB2#12	Tobii IS4
13	USB2#13	TBT
14	USB2#14	BT



571391_CFL_H_PDG_Rev0p71, page 230

Figure 14-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H



571182_CNL_PCH_H_EDS_Vol_1_Rev_0_7, page24

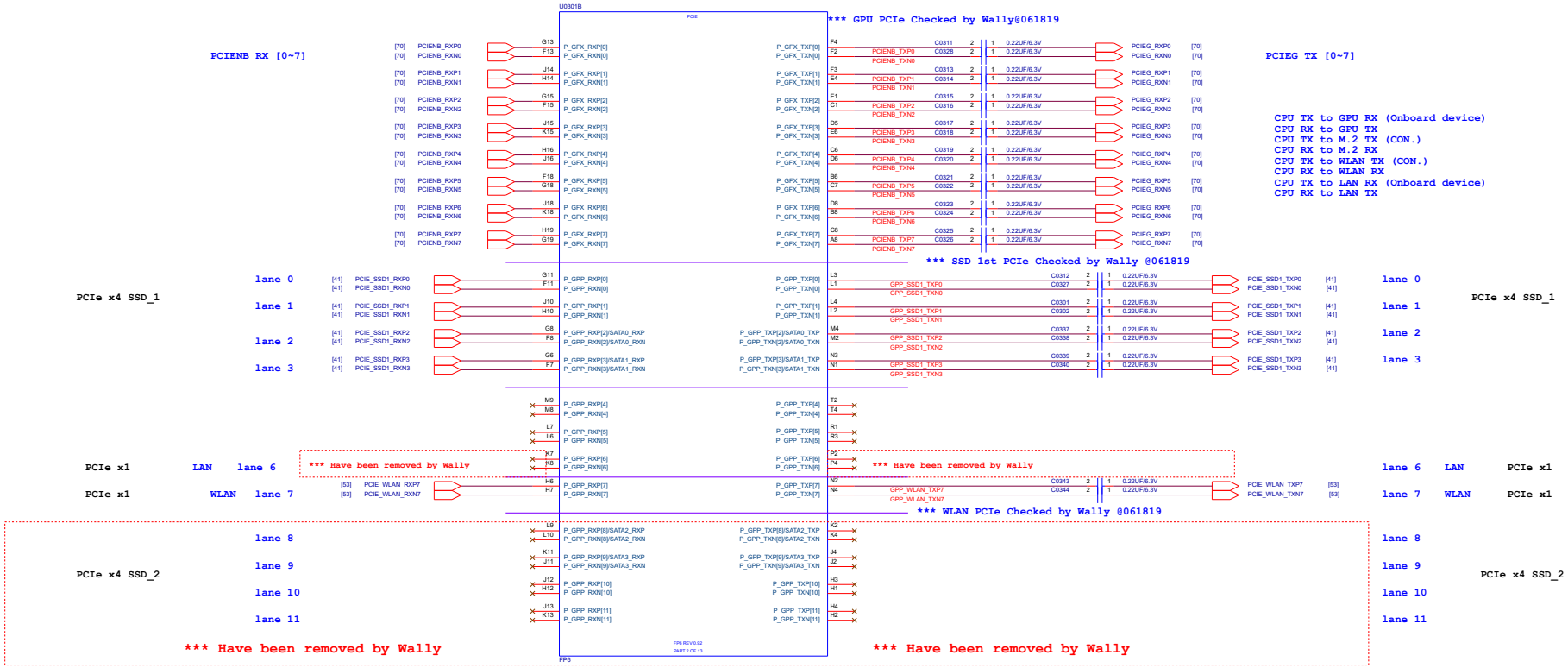
Table 1-7. PCH HSIO Detail (SKU 9-11of 11)

Flex I/O Lane	SKU		
	HM370	QM370	CM246
0	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
4	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
5	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
6	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
7	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
8	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
9	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
10	GbE	PCIe*, GbE	PCIe*, GbE
11	N/A	PCIe*	PCIe*
12	N/A	PCIe*	PCIe*
13	N/A	PCIe*	PCIe*
14	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
15	PCIe*	PCIe*	PCIe*
16	PCIe*, SATA 0A	PCIe*, SATA 0A	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B	PCIe*, SATA 1B	PCIe*, SATA 1B
20	PCIe*	PCIe*	PCIe*, SATA 2
21	PCIe*	PCIe*	PCIe*, SATA 3
22	PCIe*, SATA 4	PCIe*, SATA 4	PCIe*, SATA 4
23	PCIe*, SATA 5	PCIe*, SATA 5	PCIe*, SATA 5
24	PCIe*	PCIe*	PCIe*, SATA 6
25	PCIe*	PCIe*	PCIe*, SATA 7
26	PCIe*	PCIe*	PCIe*
27	PCIe*	PCIe*	PCIe*
28	PCIe*	PCIe*	PCIe*
29	PCIe*	PCIe*	PCIe*

PCIE/WLAN/LAN/SSD

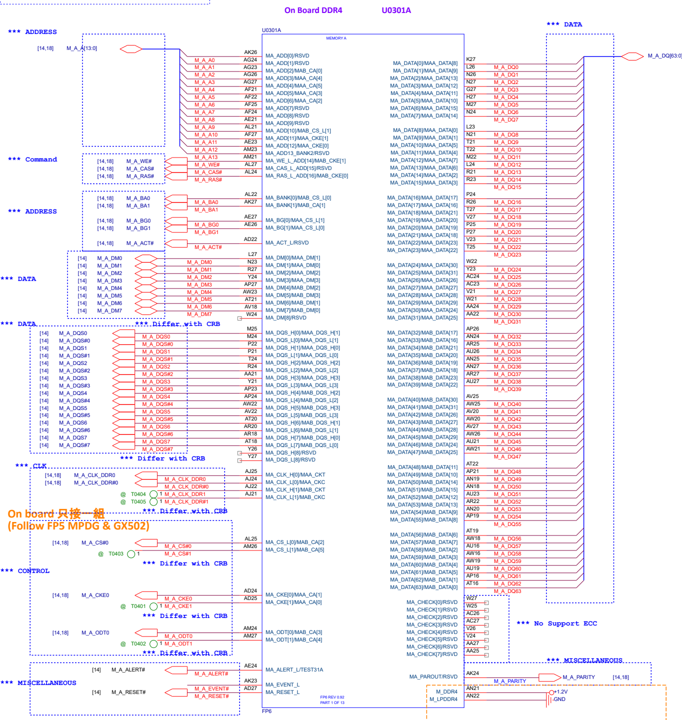
RX Side

TX Side



Project Name	GA401
Rev	R1.0
Title :	CFL-H_CPU_DMI,PEG,FDI,eDP,DDI_R1.3B
Size	C
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	NB1 RD2 EE1
Date:	Tuesday, February 11, 2020
Sheet	3 of 104

Memory Channel A



On board 只接一組
(Follow FP5 MPDG & GX502)

@20190617G

Follow FP5 MPDG no connect and pull-H@20181005B

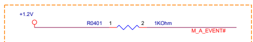


Table 12. DDR4 Signal Descriptions

Signal Group	Processor Signal Name	Description	Processor Pin Type
Data	MA_DATA[63:0]	Memory Data	Bidirectional
	MA_DQS_H[7:0] MA_DQS_L[7:0]	Data Strobe true Data Strobe complement	Bidirectional
	MA_DM[7:0]	Data Mask	Bidirectional
Clocks	MA_CLK_H[1:0]	Differential Clock true	Output
	MA_CLK_L[1:0]	Differential Clock complement	
Address	MA_ADD[12:0]	Memory Address	Output
	MA_ADD13_BANK2	Memory Address / Bank Address	
	MA_BANK[1:0]	Bank Address	Output
	MA_BG[1:0]	Bank Group	Output
Command	MA_ACT_L	Activation Command	Output
	MA_RAS_L_ADD[16]	Multi-function Command/Address: Row Address Strobe or Address 16, depending on the state of the Activation command signal.	Output
	MA_CAS_L_ADD[15]	Multi-function Command/Address: Column Address Strobe or Address 15, depending on the state of the Activation command signal.	Output

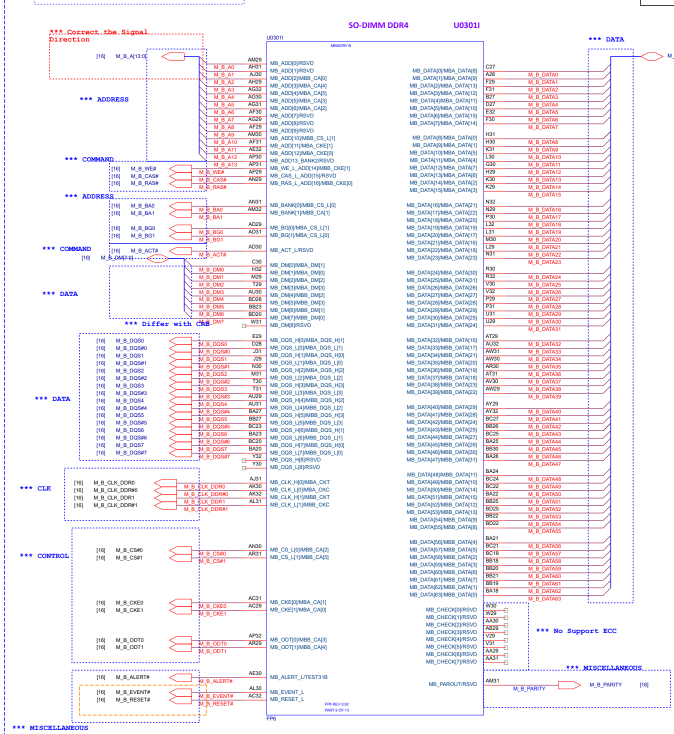
Table 12. DDR4 Signal Descriptions (continued)

Signal Group	Processor Signal Name	Description	Processor Pin Type
Command	MA_WE_L_ADD[14]	Multi-function Command/Address: Write Enable or Address 14, depending on the state of the Activation command signal.	Output
Control	MA_CKE[1:0]	Clock Enable	Output
	MA_ODT[1:0]	DRAM On-Die Termination	Output
	MA_CS_L[1:0]	Chip Select	Output
Miscellaneous	MA_EVENT_L	Memory Thermal Event	Input
	MA_RESET_L	Memory Reset	Output
	MA_ALERT_L	Multi-function : CRC error flag and Command and Address parity error.	Input/Output
	MA_PAROUT	Command and Address Parity Output: DDR4 Supports Even Parity check in DRAMs with MR setting.	Output

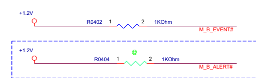
M_DDR4	EnableDDR4	Strap II	platform dependent	0	Disable DDR4 (need to have LPDDR4x enabled) 0Ω (± 5%) pull-down resistor or direct connect to VSS
				1	Enable DDR4 memory controller 0Ω (± 5%) pull-up resistor or direct connect to VDDIO_MEM_S3
M_LPDDR4	EnableLPDDR4	Strap II	platform dependent	0	Disable LPDDR4x (need to have DDR4 enabled) 0Ω (± 5%) pull-down resistor or direct connect to VSS
				1	Enable LPDDR4x memory controller 0Ω (± 5%) pull-up resistor or direct connect to VDDIO_MEM_S3
				Note:	• *Either M_DDR4 strap or M_LPDDR4 strap must be pulled-up (one or the other - NEVER both) to select either DDR4 mode or LPDDR4x mode.*

Note:
All strap pins must be configured with either external pull-up or pull-down resistors or direct connections as listed in table.

Memory Channel B

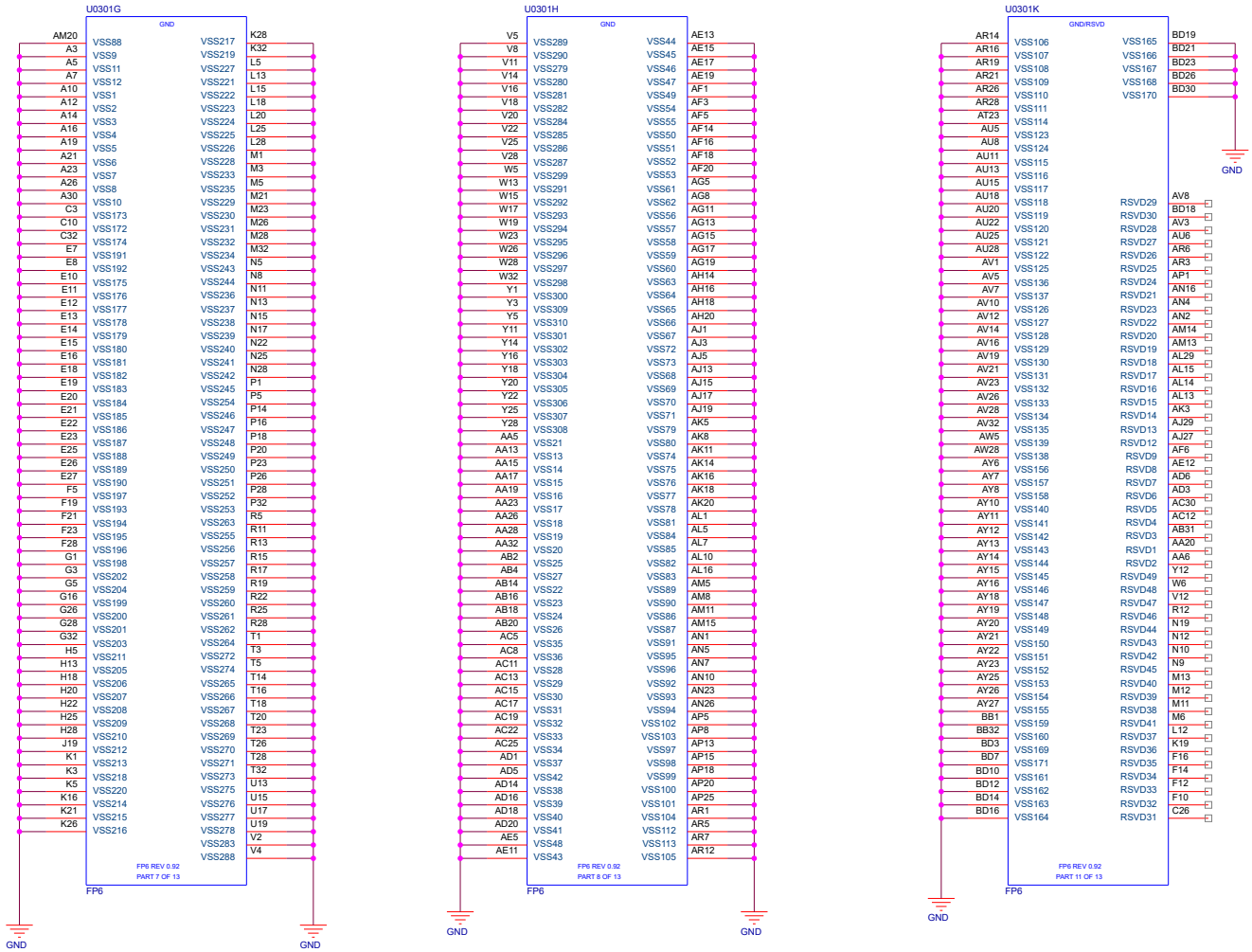


EVENT# 對接pull-H +1.2V (Follow FX505 & 公版)
RESET# only對接 (Follow FX505 & 公版)



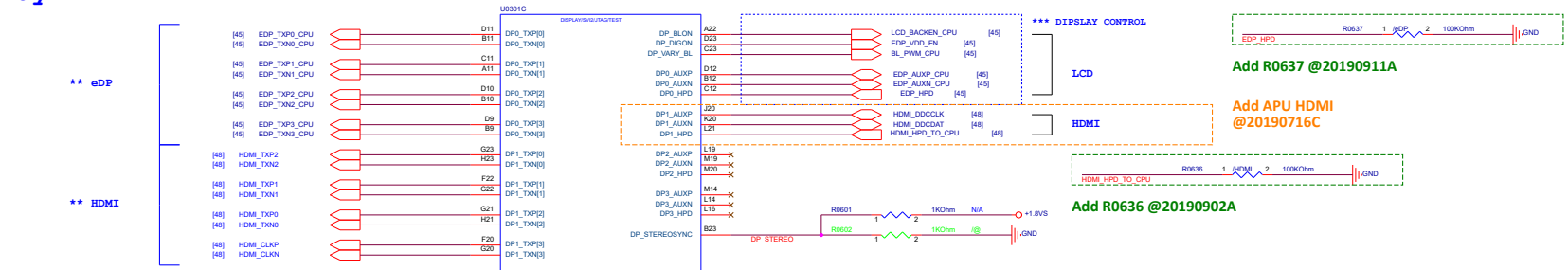
No Connect Follow 17880034747_FP5_Processor Motherboard Design_Guide

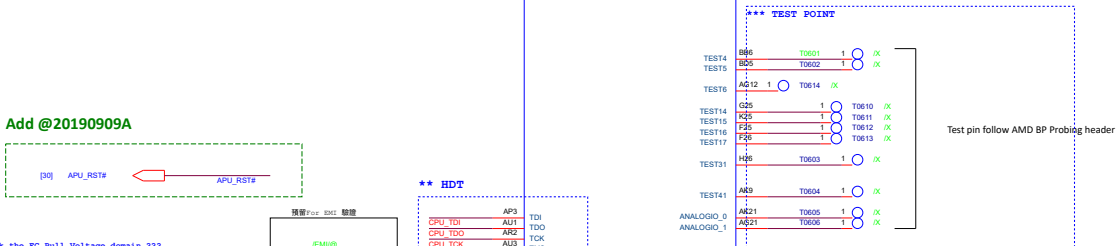
CPU_GND

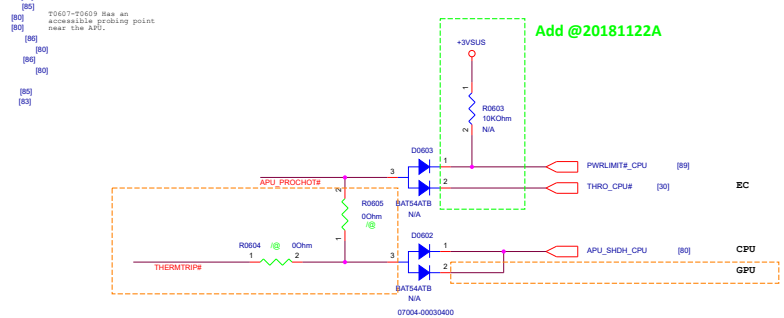


Project Name: GA401		Rev: R1.0
Title : AMD_CPU_GND		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: RD2 EE3	
Date: Tuesday, February 11, 2020	Sheet 5 of 104	

Display

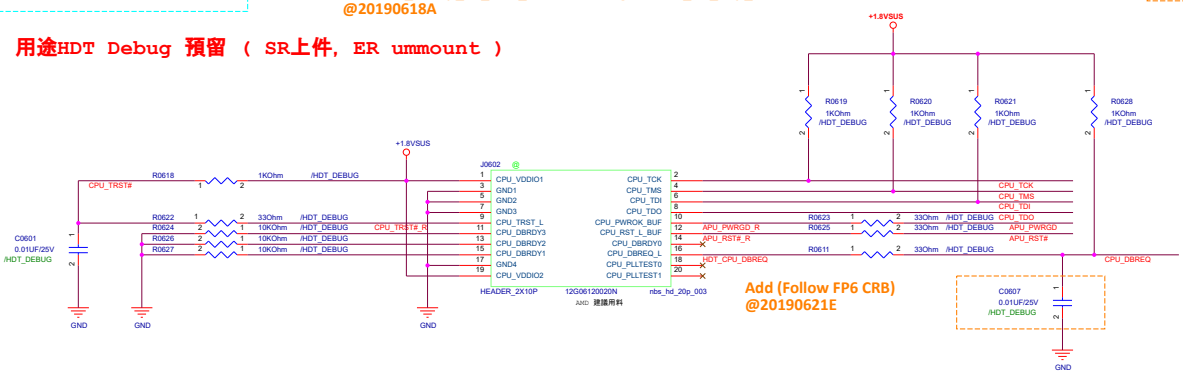




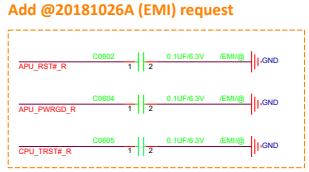


J0602 hd_2x10p_50_sam_nomask change to nbs_hd_20p_003
@20190618A

用途HDT Debug 預留 (SR上件, ER ummount)



與POWER討論此PIN改由SW動作拉降頻(cost down)
故此PIN不接
P.30 &P.78 DGPU_LIMIT
@20181015E



<variant_name>

Project Name: FX505DY		Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Tuesday, February 11, 2020	Sheet 6 of 104	

I2C/RST/GPIO/AZ

Add R0741 @20190904A following VC

** R0702, C0701- Unmount @071019A

** Diffe with CRB

** Tocuh pad

PU +3.3V_ALW (FP6 CRB)

Add @1009A

Add @1021A

** To GPU Controller

EGPIO42 EXT_SMI# --> T0705 @20190910A

** SWAP APU-#AP7 EXT_SMI# to PCIE_SSD_RST# @071019A

Audio

** To Codec/ Audio

Add @20190911A

@20181013B

Onboard Memory PCB-ID:
AGPIO6 =>DIMM_SEL0
AGPIO4 =>DIMM_SEL1

DDR4 Memory Down pool

	Samsung (1024*8)	Samsung (2048*8)	Micron (1024*8)	Micron (2048x8)
	03012-00031000 8G /Samsung/K4A8G085WC-BCWE	03012-00060100 16G /Samsung/ K4AAG085WA-BCWE	03012-00030900 Micron DDR4 3200 MT40A1G8SA-062E:J	03012-00060300 Micron DDR4 3200 MT40A2G8VA-062E:B
DIMM_SEL0	L	H	L	H
DIMM_SEL1	L	H	H	L

<Variant Name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Tuesday, February 11, 2020	Sheet 7 of 104	

CPU CLK

DGPU CLKReq#

For Optimus

CLKREQ6_GPU# --> CLKREQ0_GPU#
@20190624A

@20190624A

CLKREQ6_GPU# --> CLKREQ0_GPU#

CLKREQ0_SSD1# --> CLKREQ4_SSD1#
CLKREQ3_SSD2# --> CLKREQ5_SSD2#

CLKREQ1_WLAN# --> CLKREQ6_WLAN#

GPU

LAN

SSD1

SSD2

WLAN

PCIE_CLK P/N
後端記得預留0 ohm

*** Remove R0802/ CLKREQ2_LAN#@0625

*** Remove LAN CLK Signal

*** Remove SSD2 CLK Signal

Add T0803
@20190910A

LPC

** No Pull high differ with INTEL?
** LPC Power Domain ?

** Check with EC for GPIO status?

** Pull High differ with Spec. (No Mention)
** AGPIO68 No use

Add R0823 to +1.8VS (AMD comment)
R0815 --> unmount
@20190827A

** Connect to P.53 @070519B

DGPU Power EN pin

DGPU Power EN pin

Add T0801 & T0802 for UART debug
@20190909A

** Check Crystal RVL

design guide pull high

WLAN_SUS_CLK Update

<Variant Name>

ASUS	Project Name: FX505DY	Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Tuesday, February 11, 2020	Sheet 8 of 104	

CPU_Power

20A EDC
0.7~1.325V @ 15A TDC

96A EDC
0.3~1.400V 58A TDC

+VDDCR_SOC

+APU_VDDSOC_RUN @15A TDC @20A EDC

U0301F

POWER

VDDCR_SOC1 N16
VDDCR_SOC2 N18
VDDCR_SOC3 N20
VDDCR_SOC4 P17
VDDCR_SOC5 P19
VDDCR_SOC6 R18
VDDCR_SOC7 R20
VDDCR_SOC8 T19
VDDCR_SOC9 U18
VDDCR_SOC10 U20
VDDCR_SOC11 V19
VDDCR_SOC12 W18
VDDCR_SOC13 W20
VDDCR_SOC14 Y19

VDDCR48 G7
VDDCR45 G10
VDDCR46 G12
VDDCR47 G14
VDDCR51 H8
VDDCR49 H11
VDDCR50 H15
VDDCR54 K6
VDDCR52 K12
VDDCR53 K14
VDDCR55 L8
VDDCR57 M7
VDDCR56 M10
VDDCR58 N14
VDDCR62 P7
VDDCR59 P10
VDDCR60 P13
VDDCR61 P15
VDDCR65 R8
VDDCR63 R14
VDDCR64 R16
VDDCR70 T7
VDDCR66 T10
VDDCR67 T13
VDDCR68 T15
VDDCR69 T17
VDDCR71 U14
VDDCR72 U16
VDDCR73 V13
VDDCR74 V15
VDDCR75 V17
VDDCR79 W7
VDDCR76 W10
VDDCR77 W14
VDDCR78 W16
VDDCR83 Y8
VDDCR80 Y13
VDDCR81 Y15
VDDCR82 Y17
VDDCR5 AA7
VDDCR1 AA10
VDDCR2 AA14
VDDCR3 AA16
VDDCR4 AA18
VDDCR6 AB13
VDDCR7 AB15
VDDCR8 AB17
VDDCR9 AB19
VDDCR10 AC14
VDDCR11 AC16
VDDCR12 AC18
VDDCR18 AD7
VDDCR13 AD10
VDDCR14 AD13
VDDCR15 AD15
VDDCR16 AD17
VDDCR17 AD19
VDDCR22 AE8
VDDCR19 AE14
VDDCR20 AE16
VDDCR21 AE18
VDDCR28 AF7
VDDCR23 AF10
VDDCR24 AF13
VDDCR25 AF15
VDDCR26 AF17
VDDCR27 AF19
VDDCR29 AG14
VDDCR30 AG16
VDDCR31 AG18
VDDCR32 AH13
VDDCR33 AH15
VDDCR34 AH17
VDDCR35 AH19
VDDCR40 AJ7
VDDCR36 AJ10
VDDCR37 AJ14
VDDCR38 AJ16
VDDCR39 AJ18
VDDCR41 AK13
VDDCR42 AK15
VDDCR43 AK17
VDDCR44 AK19

+VDDCR_VDD

+APU_VDDCORE_RUN @58A TDC @96A EDC

VDDIO_MEM_S3 @ 6A
1.2±0.06

+1.2V

VDDIO_MEM_S3_1 AC20
VDDIO_MEM_S3_2 AC28
VDDIO_MEM_S3_3 AD23
VDDIO_MEM_S3_4 AD26
VDDIO_MEM_S3_5 AD28
VDDIO_MEM_S3_6 AD32
VDDIO_MEM_S3_7 AE20
VDDIO_MEM_S3_8 AE22
VDDIO_MEM_S3_9 AE25
VDDIO_MEM_S3_10 AE28
VDDIO_MEM_S3_11 AF23
VDDIO_MEM_S3_12 AF26
VDDIO_MEM_S3_13 AF28
VDDIO_MEM_S3_14 AF32
VDDIO_MEM_S3_15 AG20
VDDIO_MEM_S3_16 AG22
VDDIO_MEM_S3_17 AG25
VDDIO_MEM_S3_18 AG28
VDDIO_MEM_S3_19 AJ20
VDDIO_MEM_S3_20 AJ23
VDDIO_MEM_S3_21 AJ26
VDDIO_MEM_S3_22 AJ28
VDDIO_MEM_S3_23 AJ32
VDDIO_MEM_S3_24 AK22
VDDIO_MEM_S3_25 AK25
VDDIO_MEM_S3_26 AK28
VDDIO_MEM_S3_27 AL23
VDDIO_MEM_S3_28 AL26
VDDIO_MEM_S3_29 AL28
VDDIO_MEM_S3_30 AL32
VDDIO_MEM_S3_31 AM22
VDDIO_MEM_S3_32 AM25
VDDIO_MEM_S3_33 AM28
VDDIO_MEM_S3_34 AN28
VDDIO_MEM_S3_35 AN32
VDDIO_MEM_S3_36 AP28
VDDIO_MEM_S3_37 AR32

VDDIO_VPH1 AC21
VDDIO_VPH2 AD21
VDDIO_AUDIO AP9

VDD_33_1 AL18
VDD_33_2 AM17
VDD_18_1 AL20
VDD_18_2 AM19
VDD_18_S5_1 AL19
VDD_18_S5_2 AM18
VDD_33_S5_1 AL17
VDD_33_S5_2 AM16
VDDP_S5_1 AL11
VDDP_S5_2 AL12
VDDP_S5_3 AM12
VDDP1 M15
VDDP2 M16
VDDP3 M18
VDDBT_RTC_G AJ11

FP6 REV 0.92
PART 6 OF 13
FP6

11G232210526360 (1UF/10V) change to 11G232210515320 (1UF/6.3V)
C0902
@20190705C

BO (Bottom side outside SOC)
BU (on bottom side under SOC)

1pcs 22uF / 1pcs 1uF

C0901 22UF/6.3V
C0902 1UF/6.3V
C0903 22UF/6.3V
BO
BU
GND

R0902 0Ohm /NA
R0904 0Ohm /@

+VDDIO_VPH

VDDIO_AZ_ALW @ 0.2A

VDDIO_AUDIO:
1.8±0.09
+1.8VSUS
R0906 0Ohm N/A
VDD_33 @ 0.25A
+1.8VS_R
+VDDIO_AUDIO

VDD_18 @ 2.5A

VDD_18:
1.8±0.09
+1.8VS
R0907 0Ohm N/A
+VDD_18

VDD_18_ALW @ 1A

VDD_18_S5:
1.8±0.09
+1.8VSUS
R0909 0Ohm N/A
+1.8VSUS_R
+VDD_18_S5

VDD_33_ALW @ 0.25A

VDD_33:
3.3±0.165
+3VS
R0908 0Ohm N/A
+3VS_R
+VDD_33

VDD_33_S5:
3.3±0.165
+3VSUS
R0910 0Ohm N/A
+3VSUS_R
+VDD_33_S5

VDDP_S5 @ 2A

VDDP_S5:
0.75±0.0375
+0.75VSUS
R0911 0Ohm N/A
+0.75VSUS_R
+VDDP_S5

VDDP @ 2A

VDDP:0.75±0.0375
+0.75VS
R0912 0Ohm N/A
+0.75VS_R
+VDDP

VDDBT_RTC_G:
1.425 ~ 3.465
+3VA_RTC
R0901 1KOhm N/A
[10,32] VDDBT_RTC_G

RTC Power

+3VA
SL0907 0603 /@
R0905 45.3KOhm
C0907 10PF/50V
GND
RTC battery

R0903 1K change to 10K (FP6 CRB)
@20190613A

+VCC_RTC
D0902 BAV70_L
+RTC_BAT
R0903 N/A 10KOhm
+RTCBAT
BAT0901
SIDE1
SIDE2
WTOB_CON_2P
12G17100002C
C0908 0.1UF/6.3V
C0906 0.1UF/6.3V /@

Delete PU0901, C0903, C0904
Add SL0906
@20190613A

+3VA_RTC
SL0906 0603 /@
+VCC_RTC

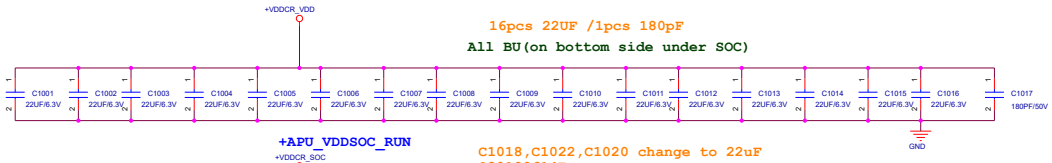
Project Name: FX505DY			Rev: R1.0
Title: CFL-H_CPU_PWR(1)_R1.3B			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD EE3	
Date: Tuesday, February 11, 2020	Sheet 9 of 104		

CPU_CAP

+APU_VDDCORE_RUN

7pcs 22UF /1pcs 1uF/1pcs 180pF
@20190614E

16pcs 22UF /1pcs 180pF
All BU(on bottom side under SOC)

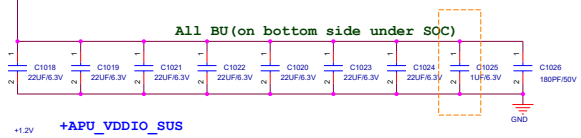


+APU_VDDSOC_RUN

C1018,C1022,C1020 change to 22uF
@20190614E

All BU(on bottom side under SOC)

Follow FP6 CRB
@20190614E

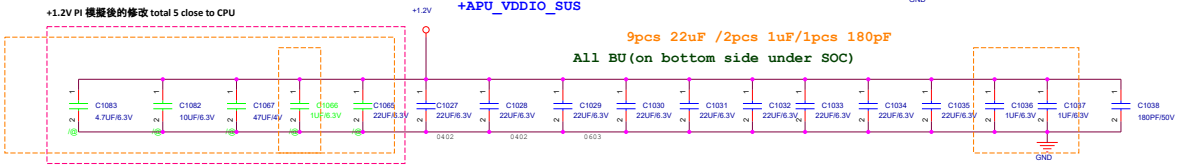


C1083,C1082,C1067C1066C1065 change to unmount
@20190614E

+APU_VDDIO_SUS

+1.2V PI 模擬後的修改 total 5 close to CPU

9pcs 22uF /2pcs 1uF/1pcs 180pF
All BU(on bottom side under SOC)



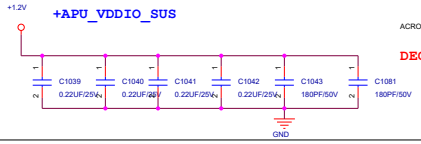
+APU_VDDIO_SUS

ACROSS VDDIO AND VSS SPLIT

DECOUPLING BETWEEN PROCESSOR AND DIMMs

4pcs 0.22uF / 2pcs 180pF

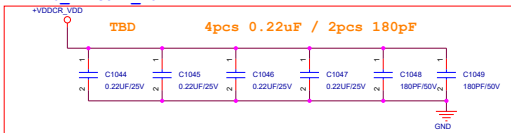
All BU(on bottom side under SOC)



+APU_VDDCORE_RUN

TBD 4pcs 0.22uF / 2pcs 180pF

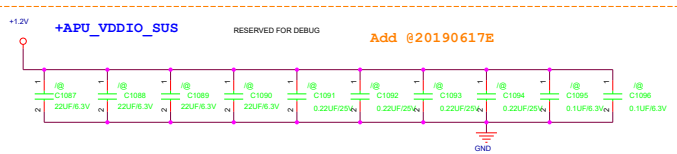
DECOUPLING BETWEEN PROCESSOR AND DIMMs ACROSS VDDIO AND VSS SPLIT



+APU_VDDIO_SUS

RESERVED FOR DEBUG

Add @20190617E

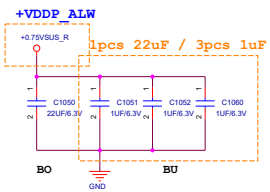


If the VSS plane is cut to create a VDDIO_MEM_S3 plane, ceramic capacitors with NP0 or C0G dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.

+VDDP change to +0.75VS
@20190704D

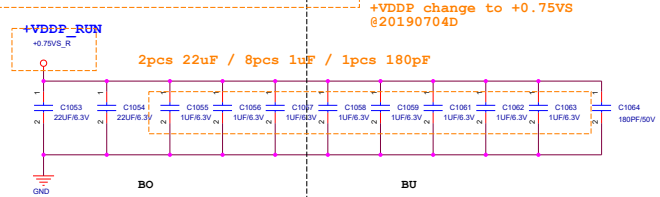
+VDDP_ALW

1pcs 22uF / 3pcs 1uF



+VDDP_RUN

2pcs 22uF / 8pcs 1uF / 1pcs 180pF

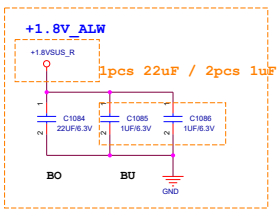


+VDD_18_S5 change to +1.8VSUS
@20190704D

Add @20190617D

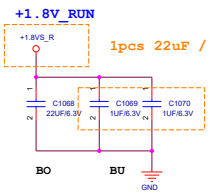
+1.8V_ALW

1pcs 22uF / 2pcs 1uF



+1.8V_RUN

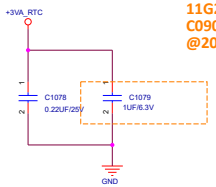
1pcs 22uF / 2pcs 1uF

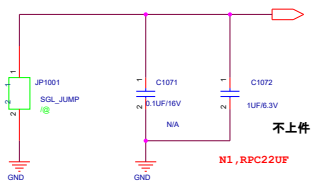


1pcs 0.22uF / 1pcs 1uF

+VDDBT_RTC

11G232210526360 (1UF/10V) change to 11G232210515320 (1UF/6.3V)
C0902
@20190705C

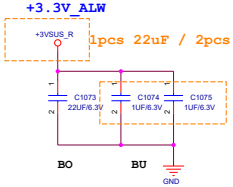




+VDD_18 change to +1.8VS
@20190704D

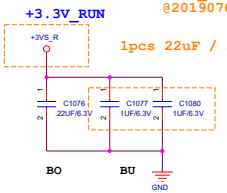
+3.3V_ALW

1pcs 22uF / 2pcs 1uF



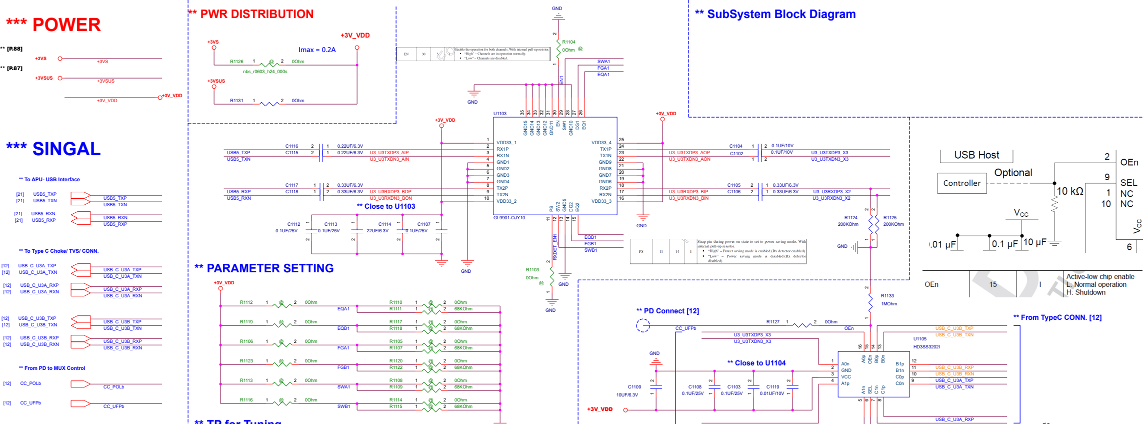
+3.3V_RUN

1pcs 22uF / 2pcs 1uF



ASUS	Project Name: FX505DY		Rev: R1.0
Title : CFL-H_CPU_PWR(1)_R1.3B			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD EE3	
Date: Tuesday, February 11, 2020	Sheet 10 of 104		

Main Board



** TP for Tuning

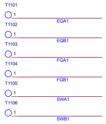


Table 4.1 – 4-leve Control Pin Settings

Setting Level	Connecting Condition
0	Tie to GND
R	Tie 68K R to GND
F	Float (Leave open)
1	Tie to VDD

Table 4.2 – Receiver Equalization Settings

EQx Setting	EQ @ 2.5 GHz	EQ @ 5 GHz
0	6.3 dB	10.1 dB
R	2.2 dB	4.4 dB
F	4.1 dB	7.1 dB
1	7.6 dB	11.6 dB

Table 4.3 – DC Gain Settings

DGx Setting	Gain Level
0	-2 dB
R	-0.5 dB
F	0.5 dB
1	2 dB

Table 4.4 – Output Swing Settings

SWx Setting	Output Swing Level
0	800 mV
R	1200 mV
F	1000 mV
1	1100 mV

Table 1. Port Select Control Logic(1)

PORT A CHANNEL	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL	
	SEL = L	SEL = H
A0p	B0p	C0p
A0n	B0n	C0n
A1p	B1p	C1p
A1n	B1n	C1n

Project Name: USB3-10G + PD		Rev: R1.0
Title : TypeC_U3SSP_repeater		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Design IP
Date: Tuesday, February 11, 2020	Sheet 11 of 104	

Main Board

*** POWER

** [P.87]

+5VSUS — +5VSUS

** [P.11]

+3V_VDD — +3V_VDD

*** SINGAL

** USB 2.0 to APU

[21] USB5_DN — USB5_DN
[21] USB5_DP — USB5_DP

[11] USB_C_U3A_TXP — USB_C_U3A_TXP
[11] USB_C_U3A_TXN — USB_C_U3A_TXN

[11] USB_C_U3A_RXP — USB_C_U3A_RXP
[11] USB_C_U3A_RXN — USB_C_U3A_RXN

[11] USB_C_U3B_TXP — USB_C_U3B_TXP
[11] USB_C_U3B_TXN — USB_C_U3B_TXN

[11] USB_C_U3B_RXP — USB_C_U3B_RXP
[11] USB_C_U3B_RXN — USB_C_U3B_RXN

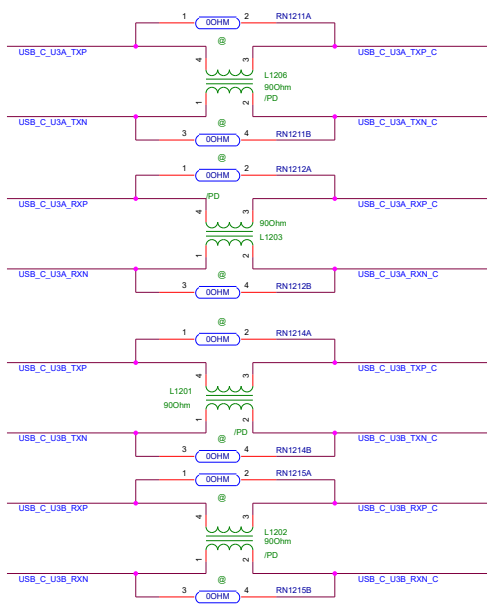
** EC Control

[30,38,57] SUSC_EC# — SUSC_EC#

** PD Control MUX Flip Flop

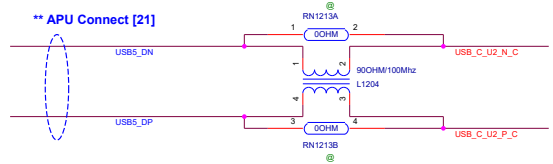
[11] CC_POLb — CC_POLb
[11] CC_UFPb — CC_UFPb

** USB 3.0 Gen2 to Re-Driver

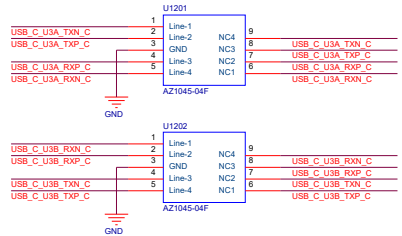


** USB 2.0 to APU

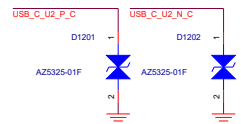
** APU Connect [21]



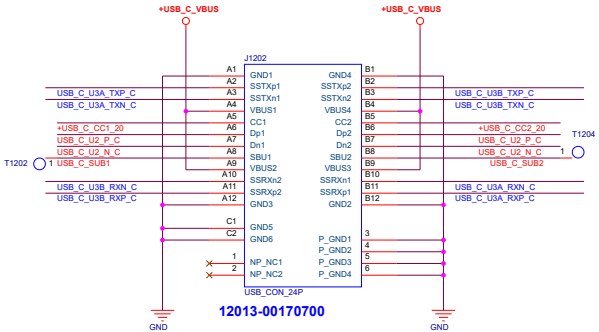
** USB3.0 ESD-Protection



** USB2.0 ESD-Protection



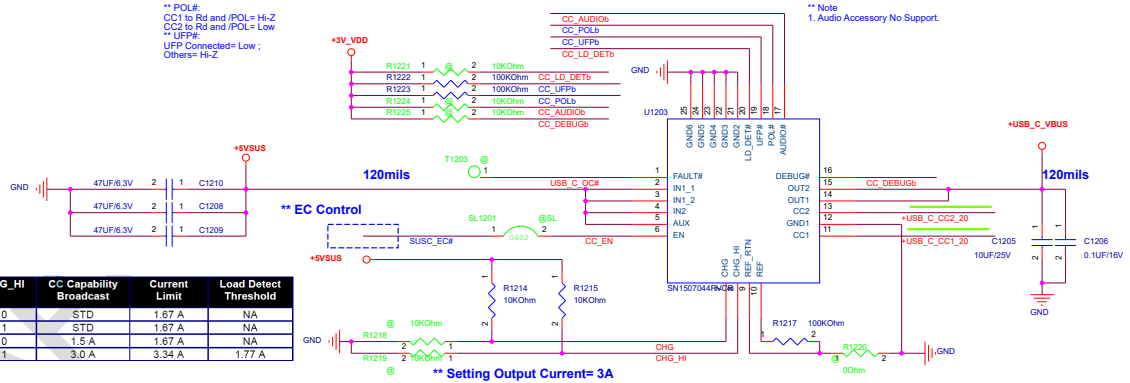
TYPE-C Connector



** TI PD Controller

** POL#:
CC1 to Rd and /POL= Hi-Z
CC2 to Rd and /POL= Low
** UFP#:
UFP Connected= Low ;
Others= Hi-Z

** Note
1. Audio Accessory No Support.



CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

SN1507044RVCR Type C Port	CC1	CC2	SN1507044RVCR Response					
			OUT	VCONN On CC1 or CC2	/POL	/UFP	/AUDIO	/DEBUG
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

ASUS	Project Name: USB3-10G + PD		Rev: R1.0
Title :	TypeC&SN1507044		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:	Gaming RD4 EE1
Date: Tuesday, February 11, 2020	Sheet 12 of 104		

Title : DDR4_TERMINATION

ASUSTeK COMPUTER INC.

Engineer: EE

Size	Project Name	Rev
C	GA401	1.0

<Core Design>

Title : DDR4_ON-BOARD_A1

ASUSTeK COMPUTER INC.

Engineer: EE

Size	Project Name	Rev
B	GA401	1.0

Date:	Tuesday, February 11, 2020	Sheet	15	of	104

<Variant Name>

Title <Title>		
Size A	Document Number GA401	Rev <RevCode>
Date: Tuesday, February 11, 2020	Sheet 17 of 104	

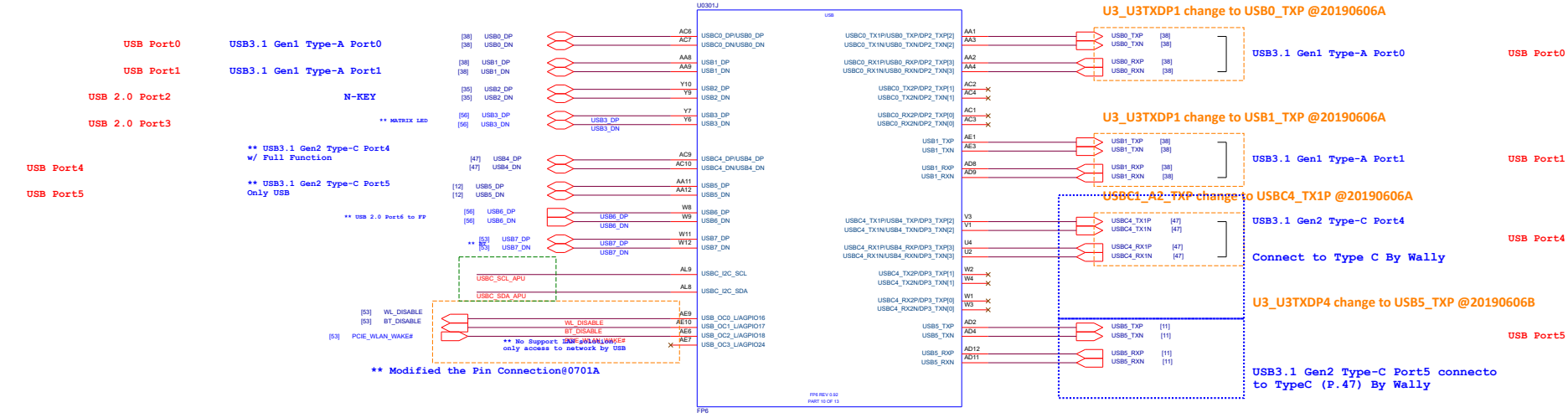
<Variant Name>

Title <Title>		
Size A	Document Number GA401	Rev R1.0
Date: Tuesday, February 11, 2020	Sheet 19 of 104	

<Variant Name>

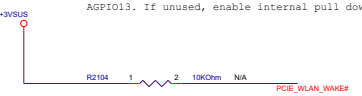
Title <Title>		
Size A	Document Number GA401	Rev <RevCode>
Date: Tuesday, February 11, 2020	Sheet 20 of 104	

CPU_USB

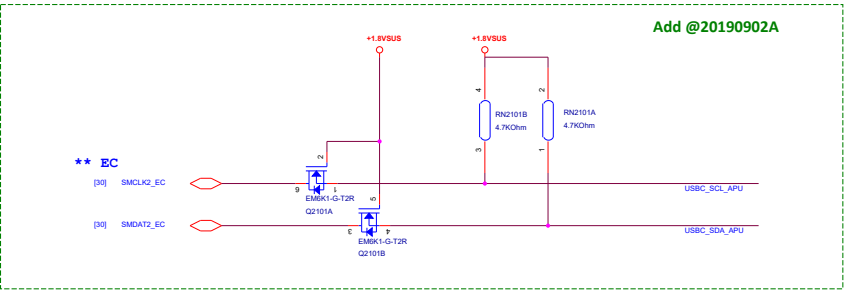


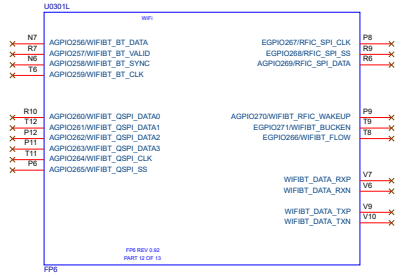
AMD Design check

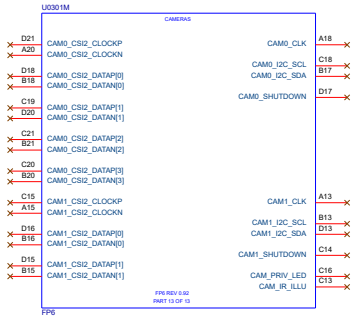
AGPIO13. If unused, enable internal pull down by software.



USB Port 0,1,4,5
USB-A USB3.2 Gen1(5Gbps): 304.8mm (12000mil)
USB-C USB3.2 Gen1(5Gbps): 177.8mm (7000mil)
USB-A & USB-C USB3.2 Gen2(10Gbps): 152.4mm (6000mil)







<Variant Name>

ASUS	Project Name: GA401	Rev: R1.0
Title :		
Size: C	Dept.: NB-SZ-RD3	Engineer:
Date: Tuesday, February 11, 2020	Sheet 21 of 104	

<Variant Name>

Title <Title>		
Size A	Document Number GA401	Rev <RevCode>
Date: Tuesday, February 11, 2020	Sheet 22 of 104	

<Variant Name>

Title <Title>		
Size A	Document Number GA401	Rev <RevCode>
Date: Tuesday, February 11, 2020	Sheet 23 of 104	

<Variant Name>

Title <Title>		
Size A	Document Number GA401	Rev <RevCode>
Date: Tuesday, February 11, 2020	Sheet 24 of 104	

<Variant Name>

Title <Title>		
Size A	Document Number GA401	Rev <RevCode>
Date: Tuesday, February 11, 2020	Sheet 25 of 104	

<Variant Name>

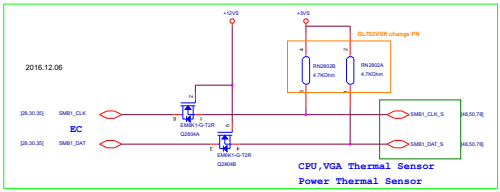
Title <Title>		
Size A	Document Number GA401	Rev <RevCode>
Date: Tuesday, February 11, 2020	Sheet 26 of 104	

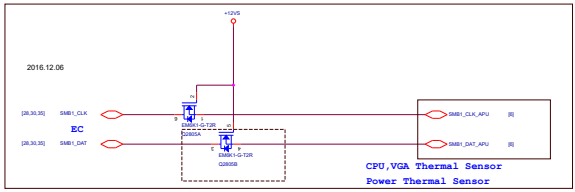
<Variant Name>

Title <Title>		
Size B	Document Number GA401	Rev <RevCode>
Date: Tuesday, February 11, 2020	Sheet 27 of 104	

Follow GL702ZM
@20181022C

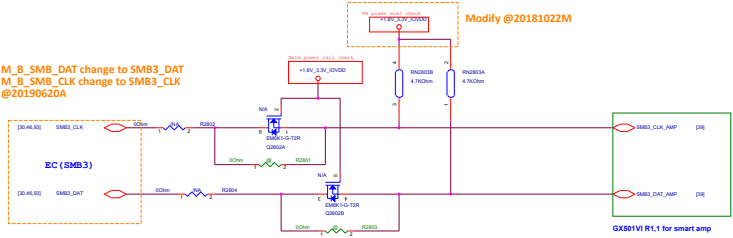
Avoid SIC, SID leakage



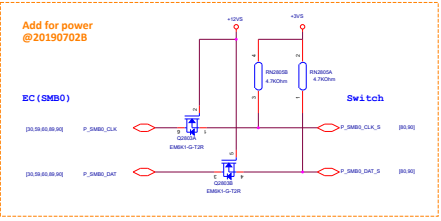


Modify @20181022M

M_B_SMB_DAT change to SMB3_DAT
M_B_SMB_CLK change to SMB3_CLK
@20190620A



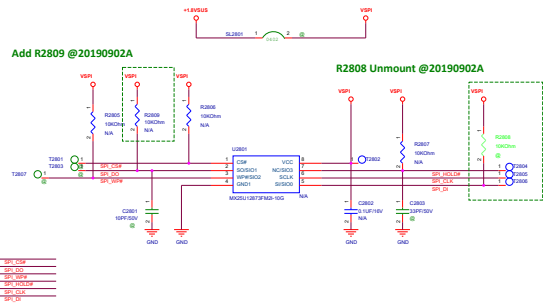
Add for power
@20190702B



SPI ROM

Add R2809 @20190902A

R2808 Unmount @20190902A



[30] SPI_CS#
[30] SPI_DO
[30] SPI_WP#
[30] SPI_HOLD#
[30] SPI_CLK
[30] SPI_DI

NKEY_預留0 OHM對接
APU_PU +3VS
EC_PU +3VA

APU I2C3_PU +3VSUS
DDR4 SO-DIMM_對接
EC (SMB3)
Type-C PD
Slave charger

EC (SMB1) — Isolation — +3VS

GPU sensor
VRAM sensor
CPU sensor
HDMI_預留

EC (SMB3) M_B_SMB_DAT — Isolation — +3VSUS SMB3_CLK_AMP

Audio AMP

ASUS	Project Name: GX531GX		Rev: 1.0
Title : PCH-SPI ROM.OTH			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, February 11, 2020	Sheet: 28	of: 104	

<Variant Name>

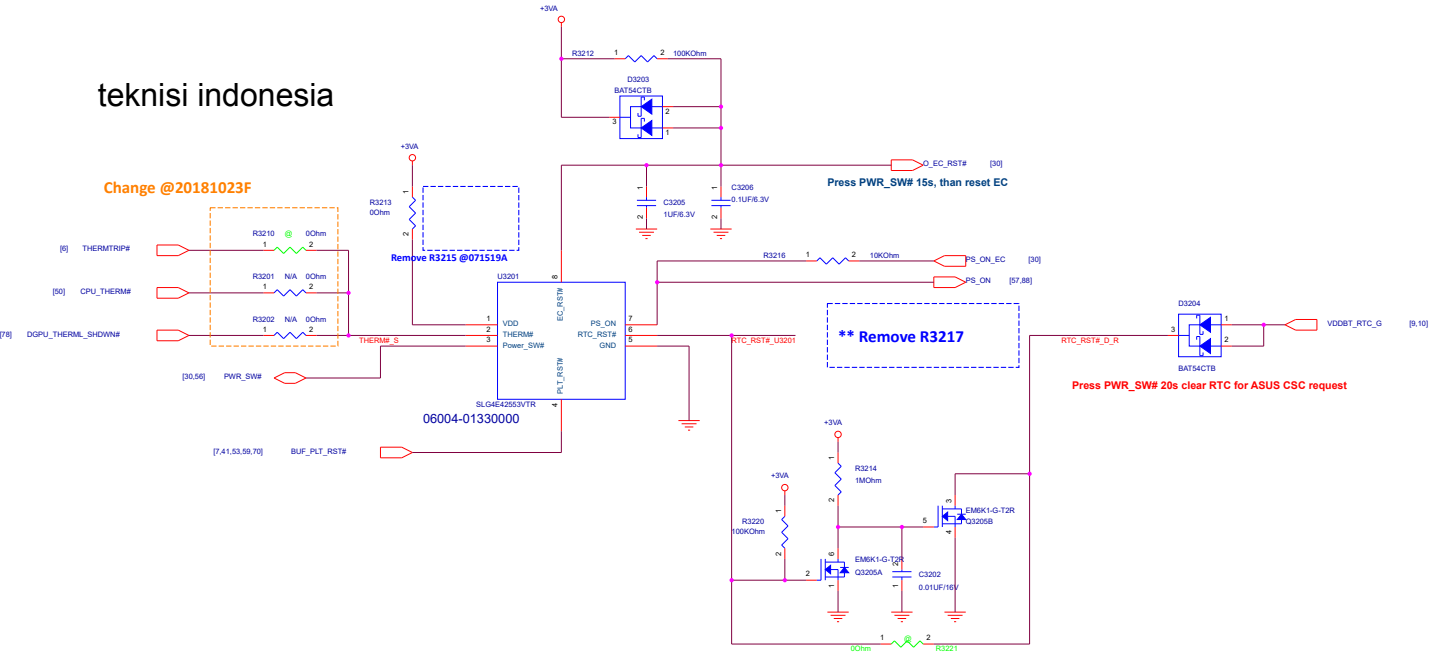
Title <Title>		
Size A	Document Number GA401	Rev <RevCode>
Date: Tuesday, February 11, 2020	Sheet 29 of 104	

Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

6.6.2 Power button behavior

https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components

UX362FA R1.3 board will verify this circuit 7/E



<Variant Name>

ASUSTeK COMPUTER INC. NB4	Title :	RST_Reset Circuit
	Engineer:	SZNB1
Size: C	Project Name: GA401	Rev: R1.0
Date: Tuesday, February 11, 2020	Sheet 32 of 104	

ASUS	Project Name: GA401	Rev: R1.0
Title : LAN RTL8111GUX-CG		
Size: B	Dept.: ASUSTeK COMPUTER INC. (I	Engineer: EE
Date: Tuesday, February 11, 2020	Sheet 33 of 104	

ASUS	Project Name: GA401	Rev: 1.0
Title : LAN_RJ45_CON		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1
Date: Tuesday, February 11, 2020	Sheet 34 of 104	

*** POWER

** [P.36] +12VS_AUDIO

** [P.30] +3VA_EC

** [P.36] +1V8_AUD_DVDD_IO

*** SINGAL

** Line to Codec [36]

[36] LINE1_R
[36] LINE1_L

** Headset from Codec [36]

[36] HPOUT_R
[36] HPOUT_L
[36] MIC2_VREFO_L
[36] MIC2_L_RING2
[36] MIC2_R_SLEEVE
[36] MIC2_VREFO_R

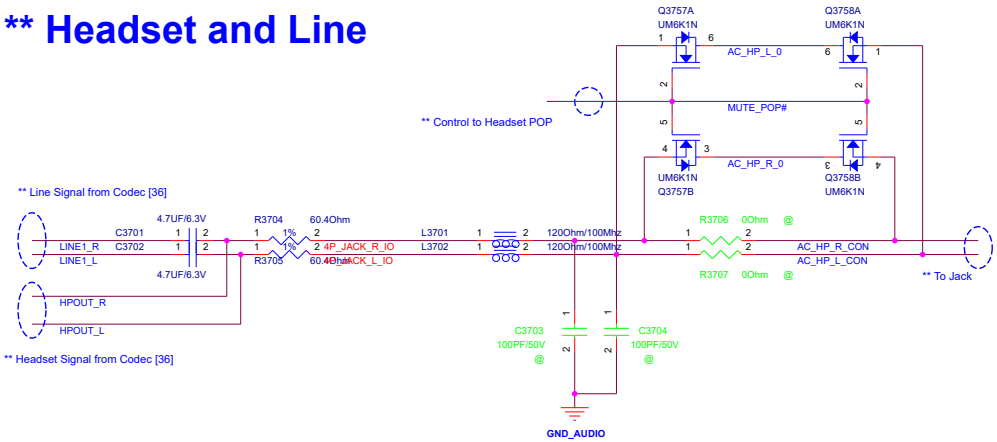
** Control Pin from Codec [36]

[36] EAPD#
[36] TOU_CON_L

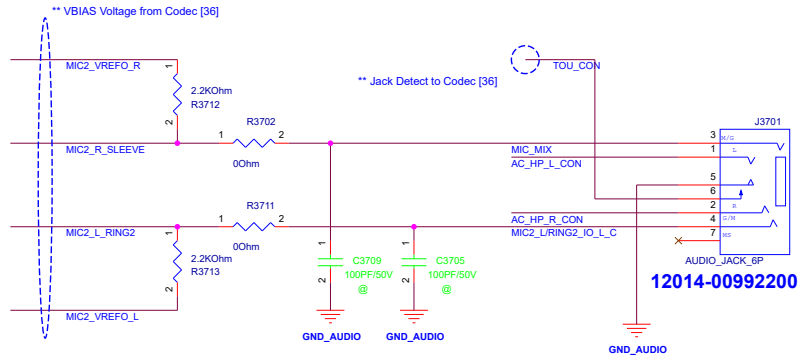
** Control Pin from APU [7]

[7] ACZ_RST#_AUD

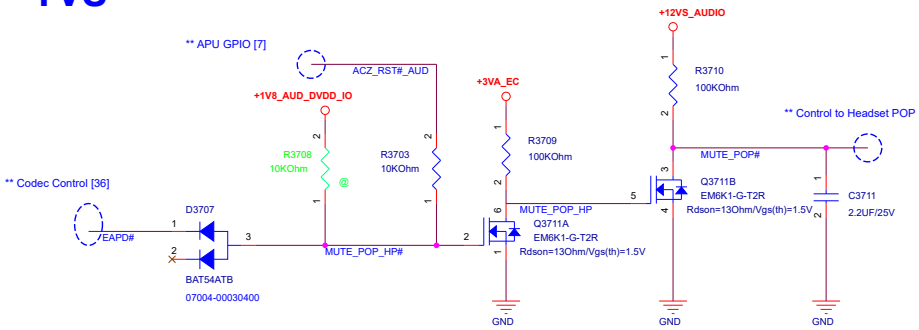
** Headset and Line



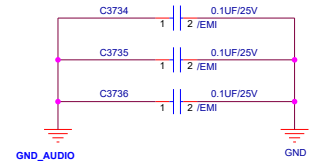
** Jack and MIC



** TVS



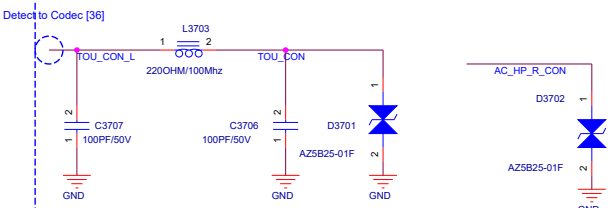
** A_GND / GND



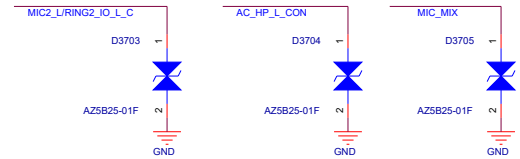
** TVS

HP & MIC Connector

HP ESD Protect

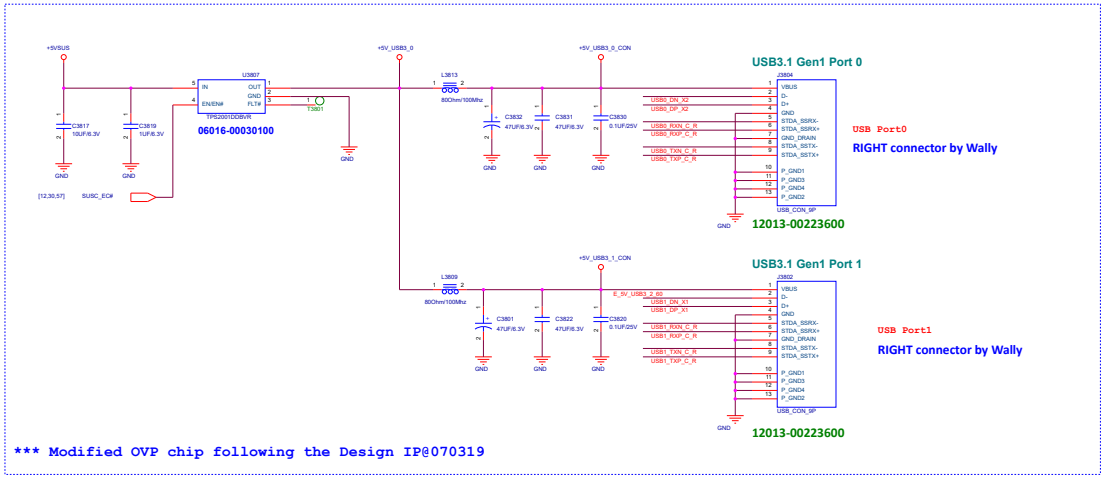


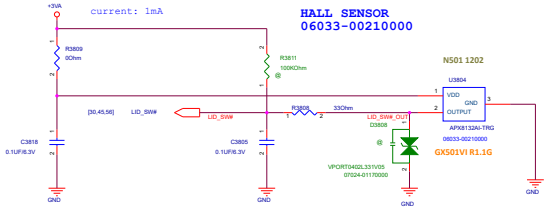
EXTERNAL MICROPHONE



ASUS	Project Name: ALC285+SMARTAMP	Rev: R1.2
Title : AUD_EXT Jack		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Tuesday, February 11, 2020	Sheet 37 of 104	

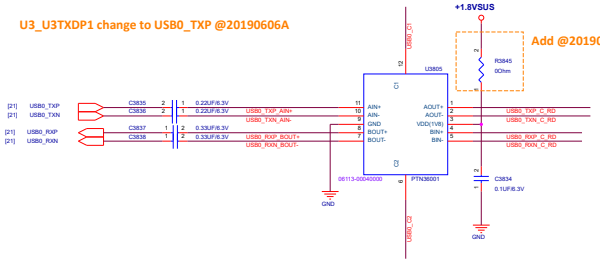
*** Remove all Charger Plus@070319A



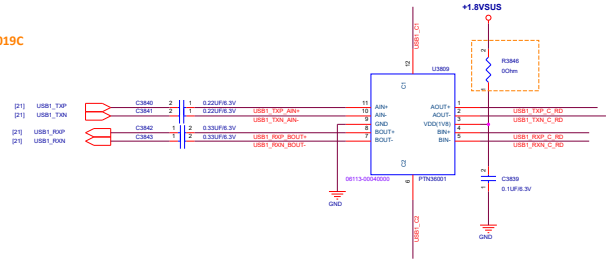


USB3.1 Gen1 Port0

U3_U3TXDP1 change to USB0_TXP @20190606A



USB3.1 Gen1 Port1



Redriver Control strap pin

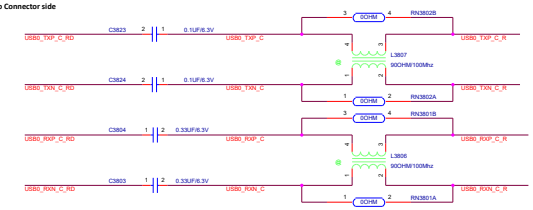
	USB1		USB2		USB0	
	USB1_C1	USB1_C2	USB2_C1	USB2_C2	USB0_C1	USB0_C2
PULL HIGH	DNI: unmout	DNI: unmout	DNI: unmout	DNI: unmout	DNI: unmout	DNI: unmout
OPEN MEDIUM						
PULL LOW	DNI: unmout	DNI: unmout	DNI: unmout	DNI: unmout	DNI: unmout	DNI: unmout

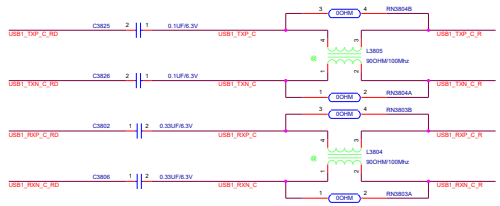
DNI: unmout
NI: mout

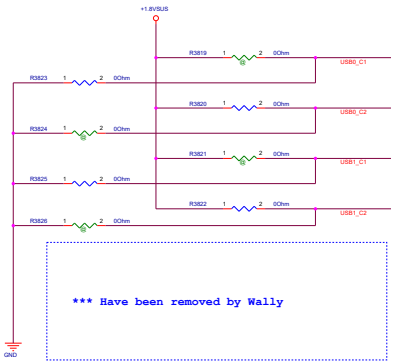
CPU 到 USB-redriver 長度: 11 Inch -> 建議先使用Medum (若是fail 再改Low)
Vendor layout 建議: 每一段等長要5mil 以內, 建議穿層僅能換2次;

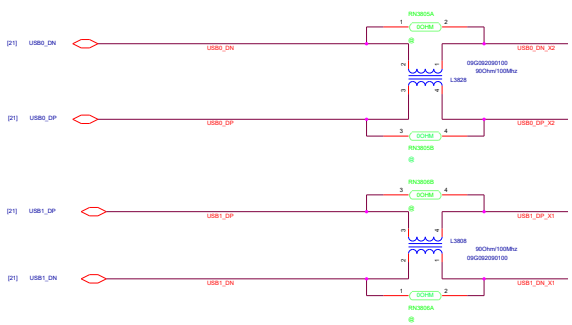
USB3.0 EMI-Protection

Close to Connector side

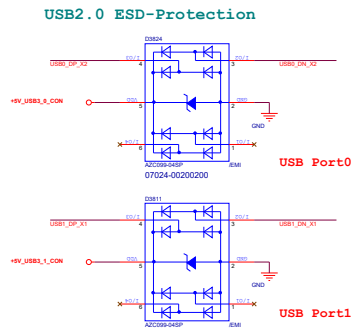




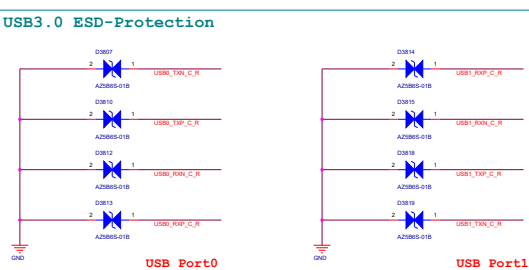




USB2.0 ESD-Protection



USB3.0 ESD-Protection



<Core Design>

ASUSTeK COMPUTER INC. NB1

Title : Aud_HP Jack, MIC
Engineer: EE
Size: Custom
Project Name: GA401
Rev: 1.0
Date: Friday, February 14, 2020
Sheet 38 of 104

*** POWER

AC_BAT_SYS

+1.8VSUS

+3VSUS

*** SINGAL

** from EC [36]

[30] REST_AMP#

** from Codec [36]

[36] I2S_Codec_SDIN

[36] I2S_LRCLK

[36] I2S_BCLK

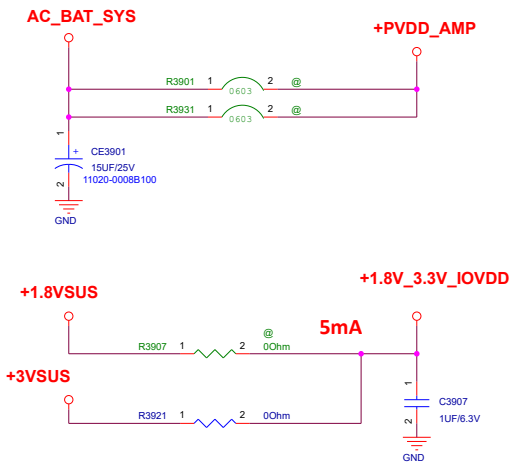
[36] I2S_Codec_SDOUT

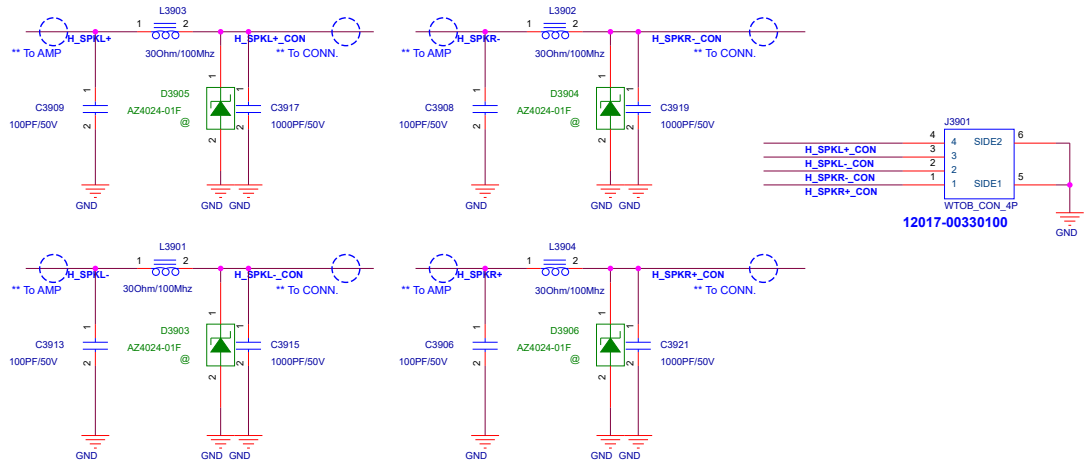
** from EC and APU [28]

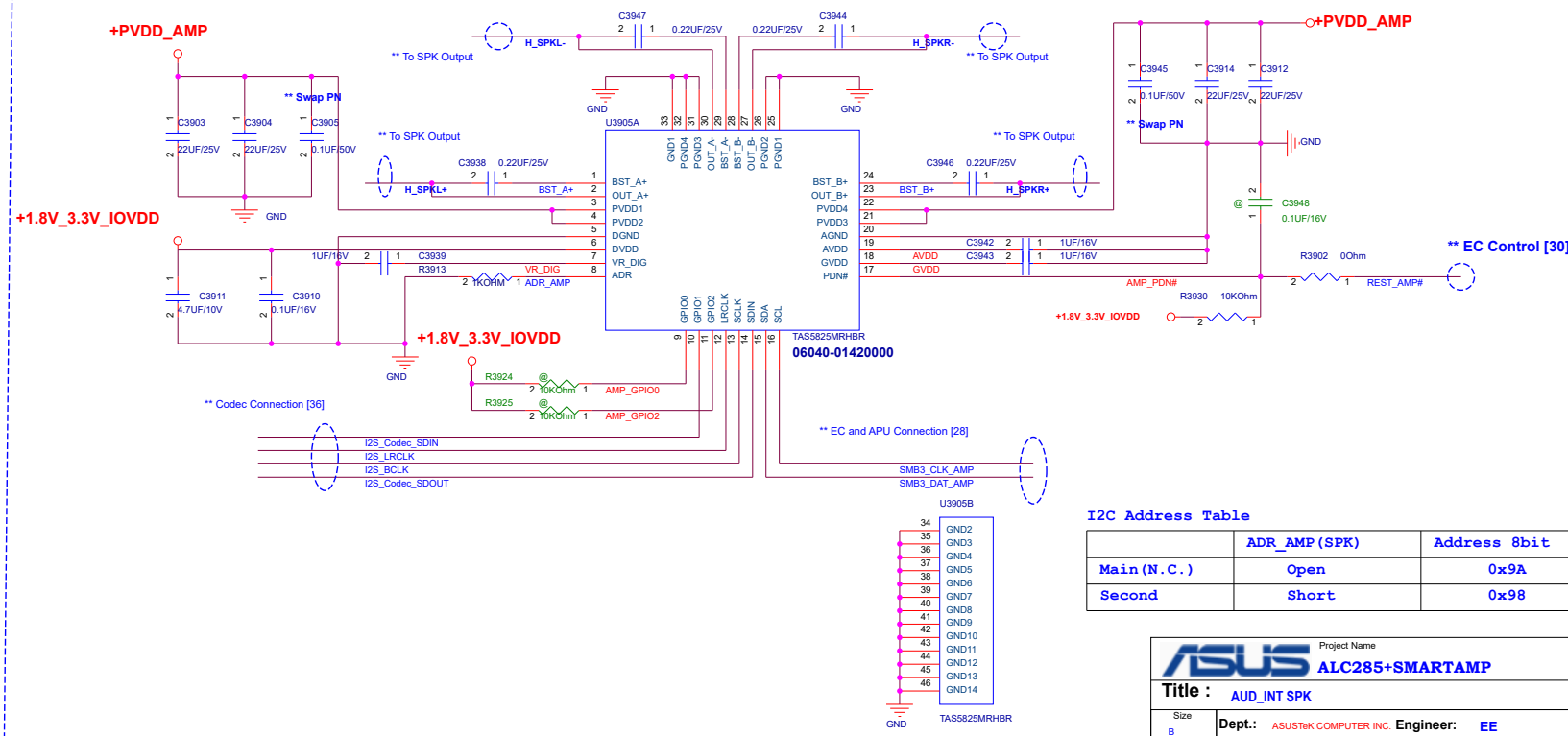
[28] SMB3_CLK_AMP

[28] SMB3_DAT_AMP

** PWR DISTRIBUTION







I2C Address Table

	ADR_AMP(SPK)	Address 8bit
Main(N.C.)	Open	0x9A
Second	Short	0x98

Project Name	ALC285+SMARTAMP	Rev R1.2
Title :	AUD_INT SPK	
Size B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Tuesday, February 11, 2020	Sheet 39 of 104	

Project Name

GA401

Rev

1.0

Title : NGFF_SSD_PCIE_CON

Size	Dept.:	Engineer:
Custom	ASUSTeK COMPUTER	NB1 RD2 EE1

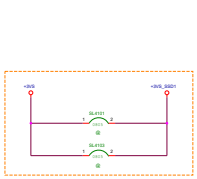
Date: Tuesday, February 11, 2020

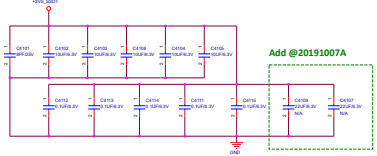
Sheet 40 of 104

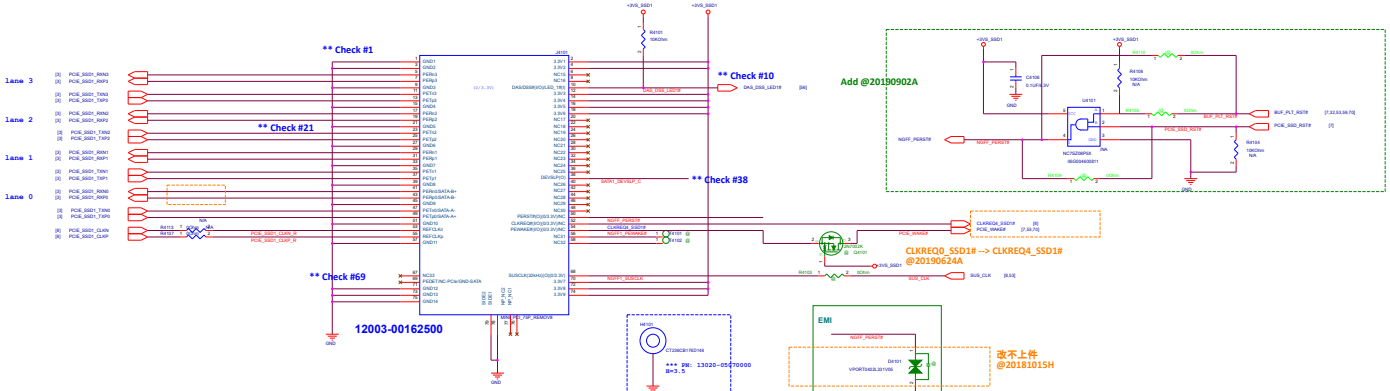
< KEY-M NGFF_SSD_PCH >

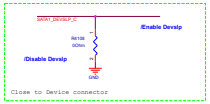
Follow GX502_1002_2330

1nd NGFF PCIE x2









<Variant Name>

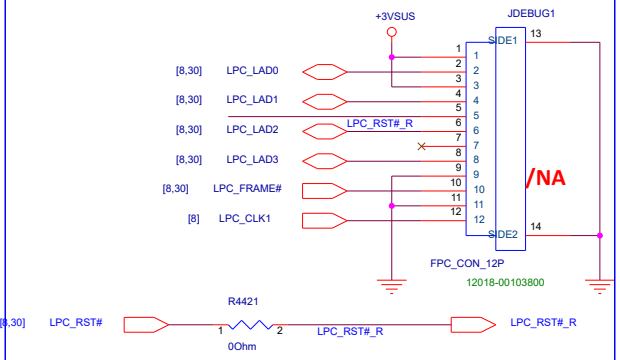
ASUSTeK COMPUTER	Title : XDD_HDD & ODD CON	
	Engineer: EE	
Size: A	Project Name: GA401	Rev: 1.0
Date: Tuesday, February 11, 2020	Sheet 42 of 104	

HDMI Switch

ASUS	Project Name: G4401	Rev: 1.0
Title : CB_CON		
Size: A3	Dept.: INDUSTRIAL COMPUTER	Engineer: EE
Date: Tuesday, February 11, 2020	Sheet 43 of 104	

LPC Debug Port

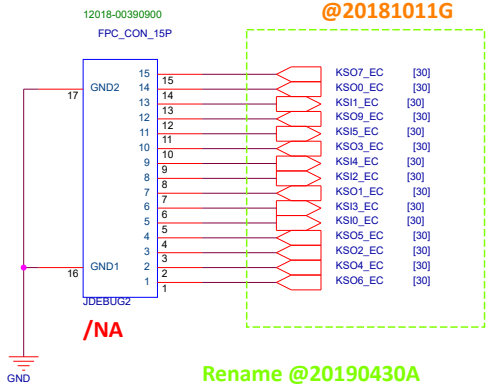
2017/11/10



2017/11/10

Flash BIOS

Rename @20181011G



Rename @20190430A

<Core Design>

ASUSTeK COMPUTER	Title : DEBUG_LPC	
	Engineer: EE	
Size: B	Project Name: GA401	Rev: 1.0
Date: Tuesday, February 11, 2020	Sheet 44 of 104	

Main Board

*** POWER

** [P.88] +3VS
** [P.71] +1V8_AON
** [P.88] +1.8VS
** [P.88] +5VS
** [P.88] +12VS

*** SINGAL

** HDMI Signal Output From APU [6]

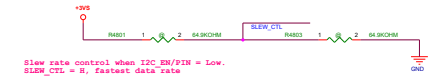
[6] HDMI_DDCDAT / [6] HDMI_DDCCLK
[6] HDMI_TXP2 / [6] HDMI_TXN2
[6] HDMI_TXP1 / [6] HDMI_TXN1
[6] HDMI_TXP0 / [6] HDMI_TXN0
[6] HDMI_CLKP / [6] HDMI_CLKN

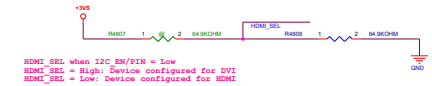
** I2C Signal From EC and APU [28]

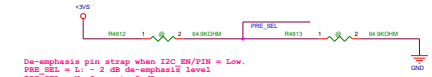
[28,50,78] SMB1_CLK_S / [28,50,78] SMB1_DAT_S

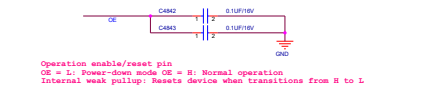
** I2C Signal From EC and APU [28]

[6] HDMI_HPD_TO_CPU

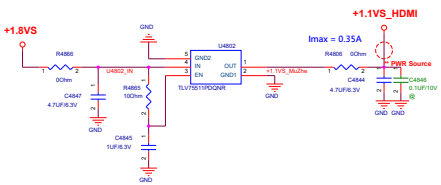




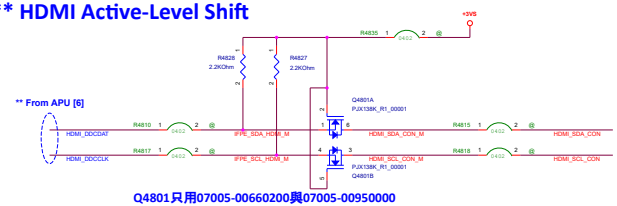




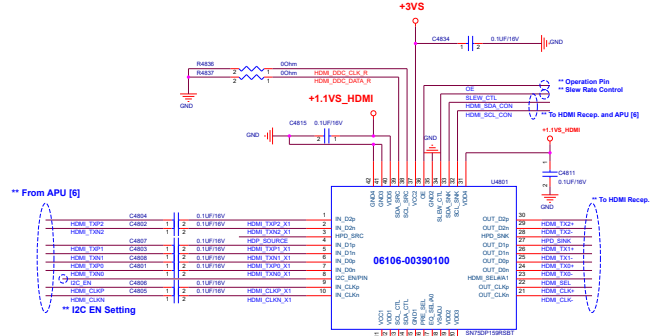
** HDMI LDO 1.1VS

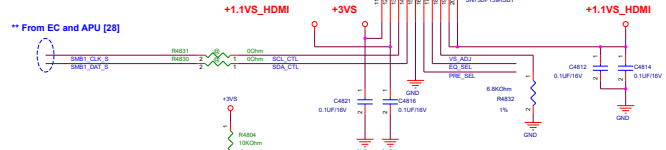


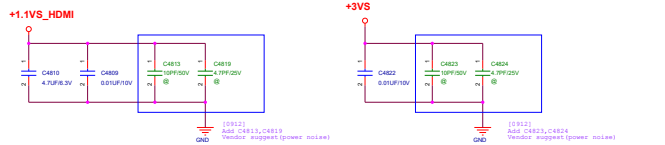
** HDMI Active-Level Shift



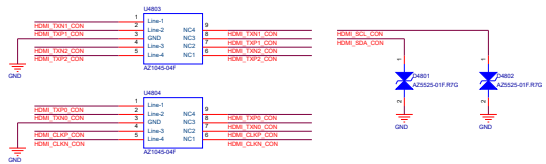
Q4801只用07005-00660200與07005-00950000



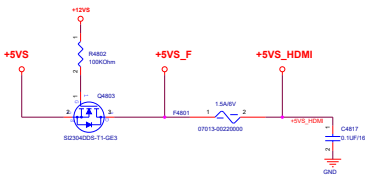




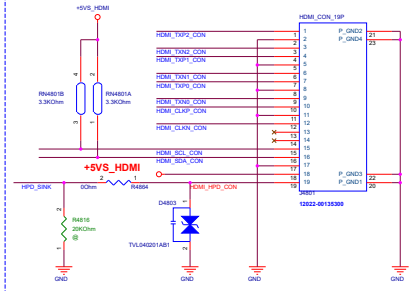
** TVS



** HDMI PWR_+5VS_HDMI

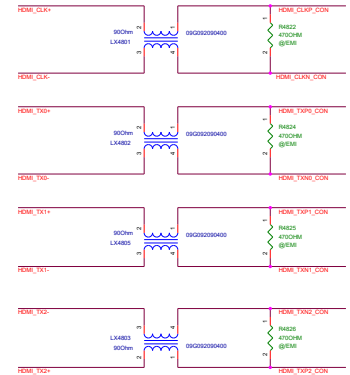


** HDMI Receptacle



Pin	Pin定义
1	TMDS Data2+
2	TMDS Data2 Shield
3	TMDS Data2–
4	TMDS Data1+
5	TMDS Data1 Shield
6	TMDS Data1–
7	TMDS Data0+
8	TMDS Data0 Shield
9	TMDS Data0–
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock–
13	CEC
14	Reserved (N.C. on device)
15	SCL
16	SDA
17	DDC/CEC Ground
18	+5V Power
19	Hot Plug Detect

** HDMI EMI



Project Name: Design IP			Rev: 0.1A
Title : HDMI ReTimer_Revision History_R0.1A			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, February 11, 2020	Sheet: 48 of 104		

<Core Design>

	Project Name **GA401**	Rev 1.0

Title : ANT

Size		
C	**Dept.:** ASUSTeK COMPUTER	**Engineer:** EE

Date: Tuesday, February 11, 2020	Sheet	49	of	104

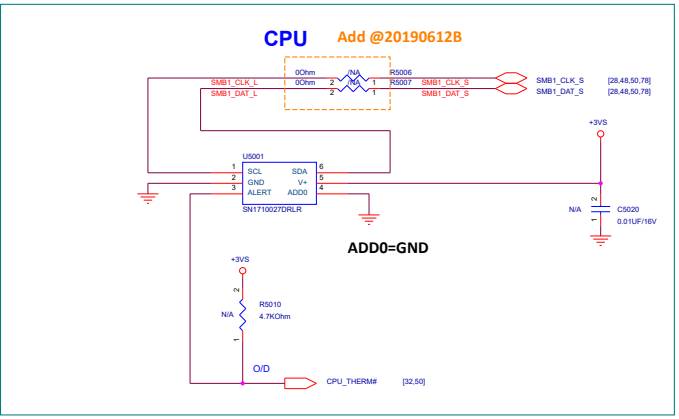
Thermal Sensor : SN170027

power rail : 3.3V

SMBUS1 to EC

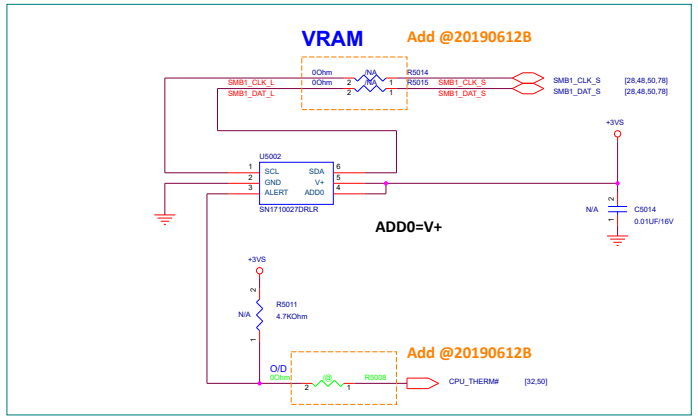
ALERT/SDA/SCL: Open-drain output; pullup resistor 5Kohm

Pin function Supply voltage.: 1.62 V to 3.6 V



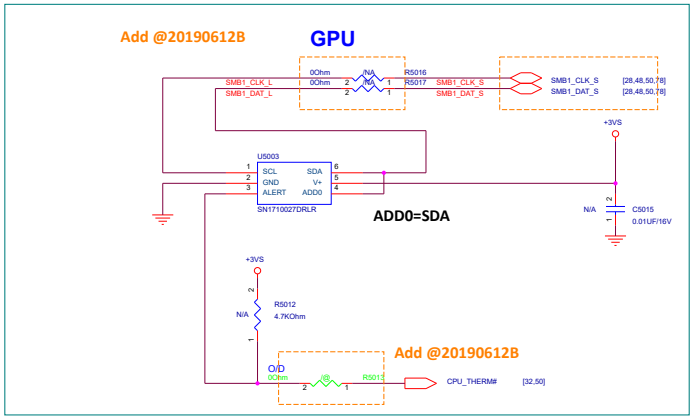
Near CPU

SMBUS addr=10010000 (90)



Near VRAM

SMBUS addr=10010001 (91)

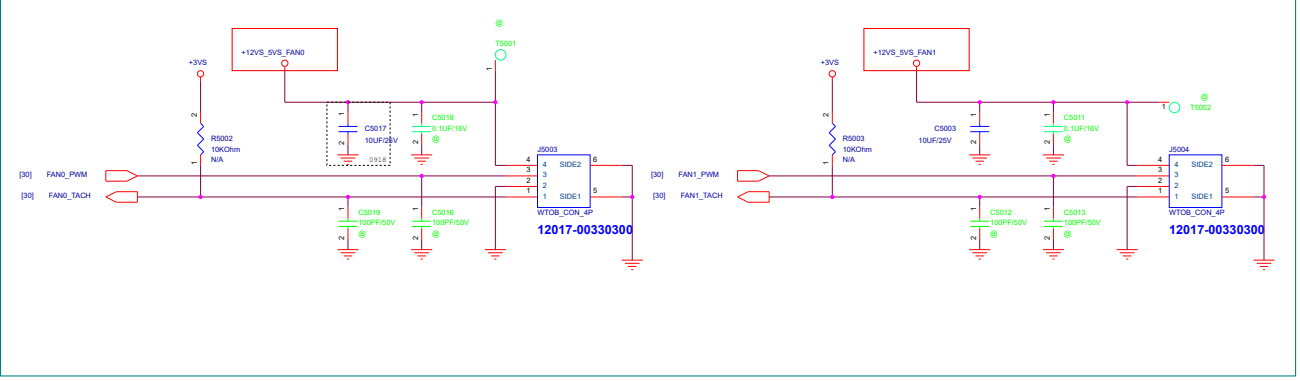


Near GPU

SMBUS addr=10010010 (92)

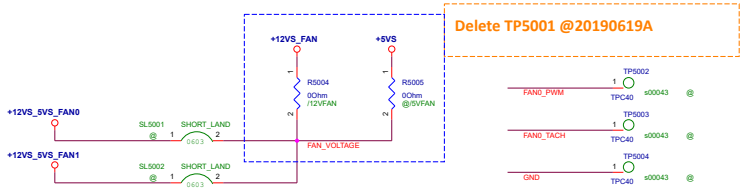
CPU&GPU FAN

Note : connector and power are by project design



ADD0: Address select. Connect to GND, SDA, SCL, or V+

DEVICE TWO-WIRE ADDRESS		ADD0 PIN CONNECTION	Output
1001000	90	Ground	CPU
1001001	91	V+	VRAM
1001010	92	SDA	GPU
1001011	93	SCL	



** R5004 mount & R5005 unmount @071519A

** Check FAN CONN Define!!!!!!

TYPE-C USB3.1

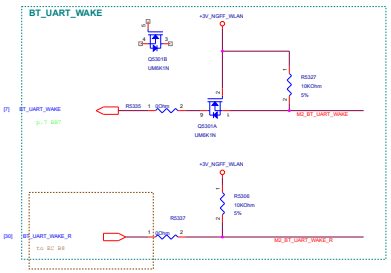
Main Board

AMD-1.0

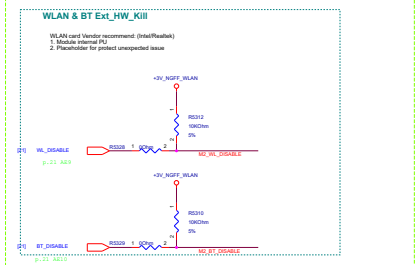
NGFF M.2 TYPE_E-KEY WIFI

Main Board

BT_UART_WAKE

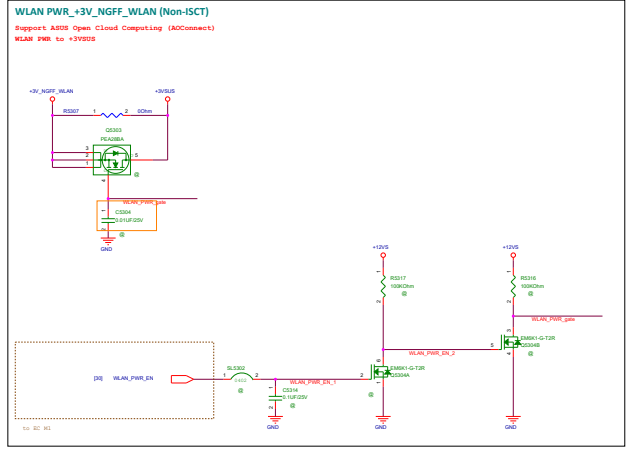


WLAN & BT Ext_HW_Kill

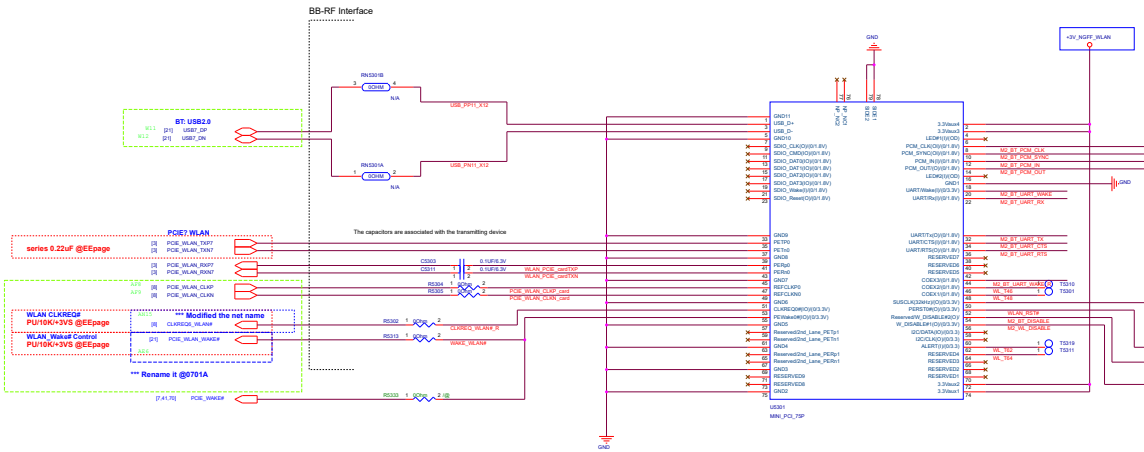


WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

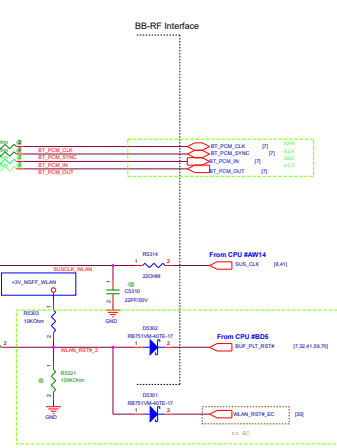
Support ASUS Open Cloud Computing (AOConnect)
WLAN PWR to +3VSUS



BB-RF Interface

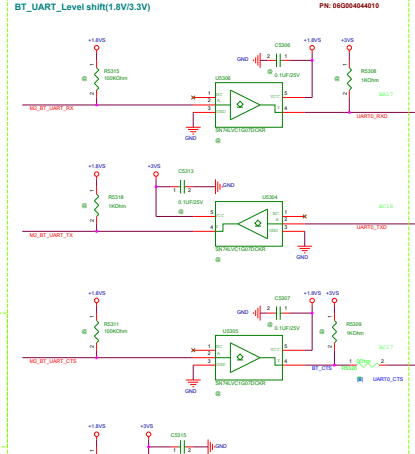


BB-RF Interface



BT_UART_Level shift(1.8V/3.3V)

P/N: 06G004044010

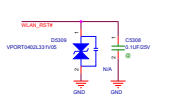


CON5301 NGFF E-KEY WLAN Connector
H= 4 mm / under WLAN card = 2.4 mm
AGROSYN/ASES0-S6701-TS40
P/N:12003-00160100

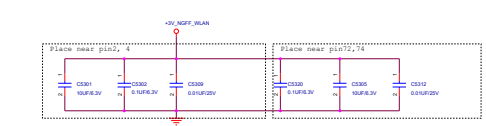
[8] UART0_RXD
[8] UART0_TXD

For EMI

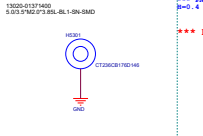
Reserve for powr noise



WLAN NGFF_WLAN bypass capactor



Screw Hole



*** PN: 13020-05070100
R=0.4

*** Modified NUT for ME By Wally@061819

<Variant Name>

ASUSTeK COMPUTER	Title: NGFF Type_WLAN&BT		
	Engineer: EE		
Size: Custom	Project Name: GA401		Rev: R1.0
Date: Tuesday, February 11, 2020	Sheet: 53 of 104		

<Variant Name>

Title <Title>		
Size A	Document Number GA401	Rev <RevCode>
Date: Tuesday, February 11, 2020	Sheet 54 of 104	

<Core Design>

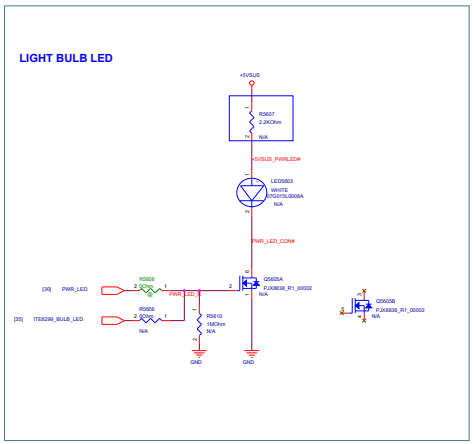
ASUSTeK COMPUTER	Title : IO Con. to MB	
	Engineer: EE	
Size: A	Project Name: GA401	Rev: 1.0
Date: Tuesday, February 11, 2020	Sheet 55 of 104	

*** POWER

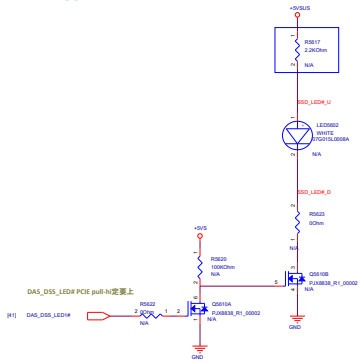
*** SINGAL

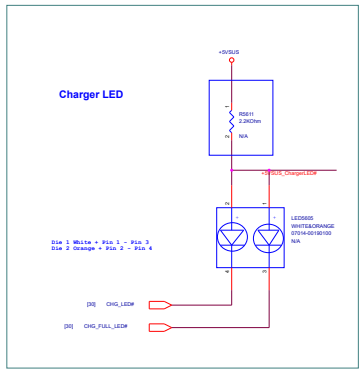
[30] LED_WHITE_#1 — LED_WHITE_#1
[30] LED_WHITE_#2 — LED_WHITE_#2
[21] USB3_DP — USB3_DP
[21] USB3_DN — USB3_DN
[21,56] USB6_DP — USB6_DP
[21,56] USB6_DN — USB6_DN

LIGHT BULB LED

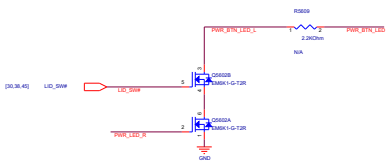


PCIE SSD LED



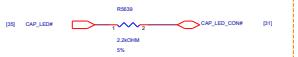


PWR BUTTON LED

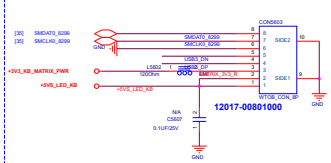


CAPS LOCK LED
@20181015C

CAP LED



Matrix LED CONN.



** Add C5607 and Trace Connection@070919A

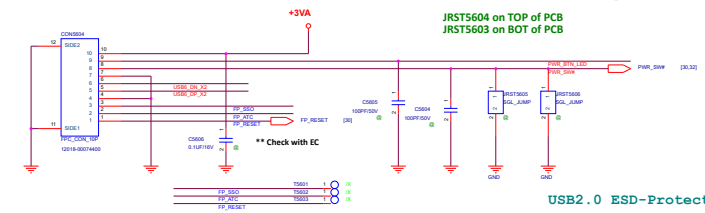
Martix LED

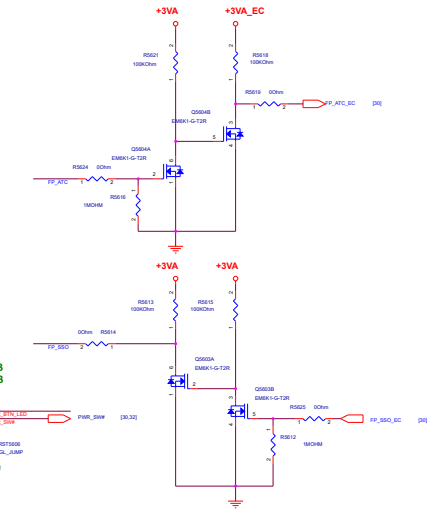
Pin	Pin define
1	+5VCC
2	+5VCC
3	+3.3VCC
4	USB/D+
5	USB/D-
6	GND
7	GND
8	GND

MB_PWR BUTTON CON._10pin

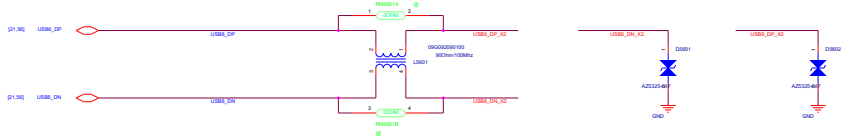
Connected to Power Key Board 55

JRST5604 on TOP of PCB
JRST5603 on BOT of PCB

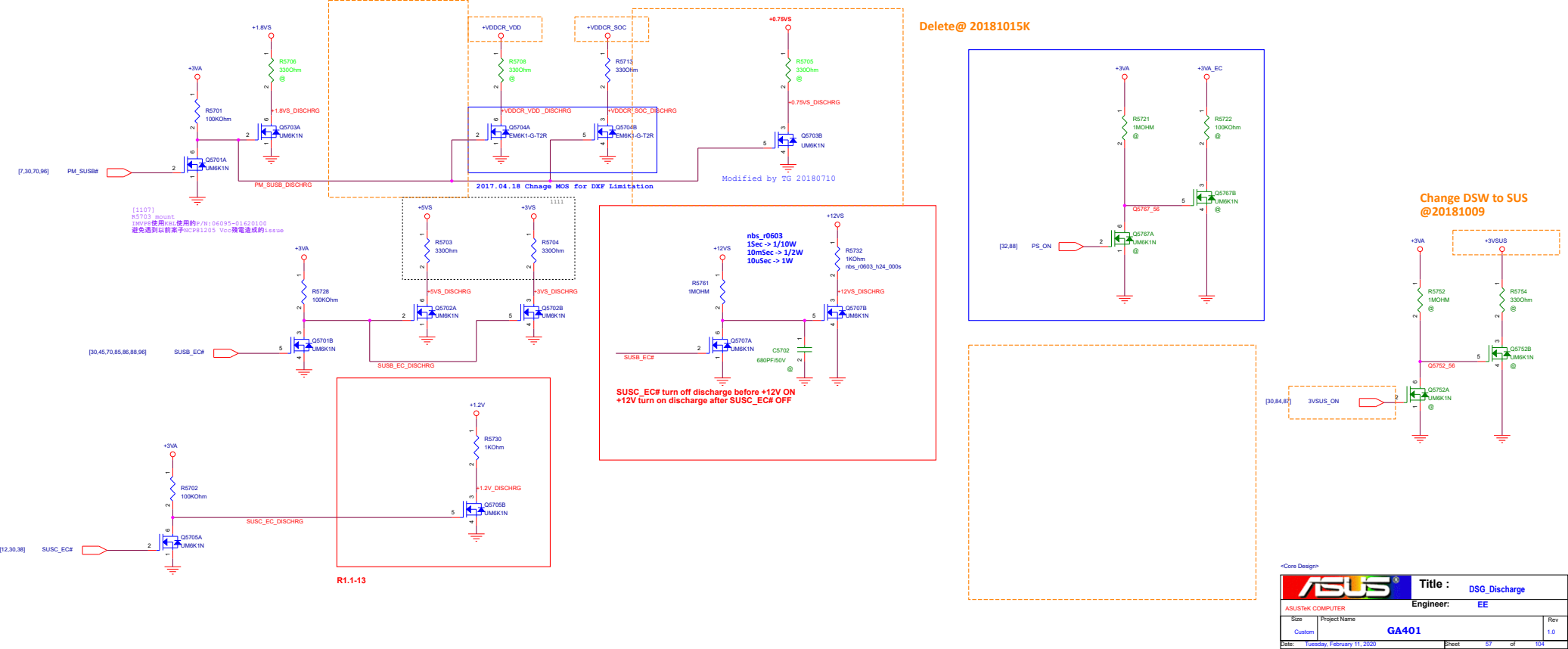




USB2.0 ESD-Protection



NOTE:
1. PERKEY CHIP PWR ADD !!!!


Delete@ 20181015K
+1.8VS
+3VA
R5706
330Ohm
@
+1.8VS_DISCHRG
R5701
100KOhm
Q5703A
UM6K1N
Q5701A
UM6K1N
[7,30,70,96]
PM_SUSB#
PM_SUSB_DISCHRG
+VDDCR_VDD
+VDDCR_SOC
R5708
330Ohm
@
R5713
330Ohm
+VDDCR_VDD_DISCHRG
+VDDCR_SOC_DISCHRG
Q5704A
EMBK1-G-T2R
Q5704B
EMBK1-G-T2R
2017.04.18 Chnage MOS for DXF Limitation
+0.75VS
R5705
330Ohm
@
+0.75VS_DISCHRG
Q5703B
UM6K1N
Modified by TG 20180710
[1107]
R5703 mount
IMVP8使用R8L使用的P/N:06095-01620100
避免遇到以前案子NCP81205 Vcc微電過成的issue
+5VS
+3VS
R5703
330Ohm
R5704
330Ohm
+5VS_DISCHRG
+3VS_DISCHRG
Q5702A
UM6K1N
Q5702B
UM6K1N
+3VA
R5728
100KOhm
Q5701B
UM6K1N
[30,45,70,85,86,88,96]
SUSB_EC#
SUSB_EC_DISCHRG
+12VS
nbs_r0603
15ec -> 1/10W
10mSec -> 1/2W
10uSec -> 1W
R5761
1MOHM
Q5707A
UM6K1N
C5702
680PF/50V
@
R5732
1KOhm
nbs_r0603_h24_000s
+12VS_DISCHRG
Q5707B
UM6K1N
SUSB_EC#
SUSC_EC# turn off discharge bofore +12V ON
+12V turn on discharge after SUSC_EC# OFF
+1.2V
R5730
1KOhm
+1.2V_DISCHRG
Q5705B
UM6K1N
+3VA
R5702
100KOhm
Q5705A
UM6K1N
[12,30,38]
SUSC_EC#
SUSC_EC_DISCHRG
R1.1-13
+3VA
+3VA_EC
R5721
1MOHM
@
R5722
100KOhm
@
Q5767B
UM6K1N
@
Q5767_56
Q5767A
UM6K1N
@
[32,88]
PS_ON
Change DSW to SUS
@20181009
+3VA
+3VSUS
R5752
1MOHM
@
R5754
330Ohm
@
Q5752B
UM6K1N
@
Q5752_56
Q5752A
UM6K1N
@
[30,84,87]
3VSUS_ON
<Core Design>
Title :
DSG_Discharge
ASUSTeK COMPUTER
Engineer:
EE
Size
Custom
Project Name
GA401
Rev
1.0
Date:
Tuesday, February 11, 2020
Sheet
57
of
104

<Variant Name>

Title : NGFF SSD(MAXIM)

ASUSTeK COMPUTER

Engineer: Wendell_Lo

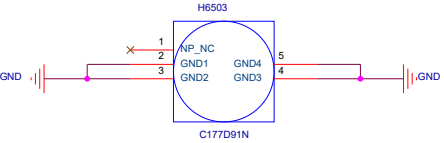
Size	Project Name	Rev
D	GA401	1.0

Date:	Tuesday, February 11, 2020	Sheet	63	of	104

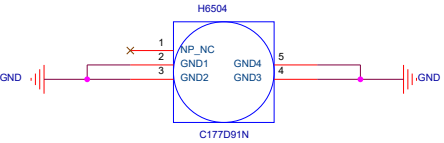
Main Board

s13041

s13041



s06060



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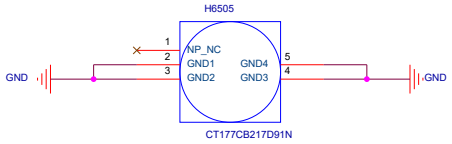
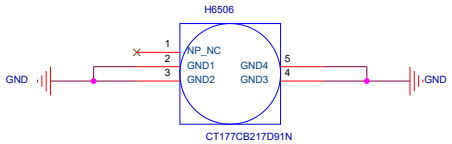


s13036



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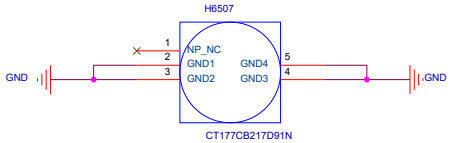

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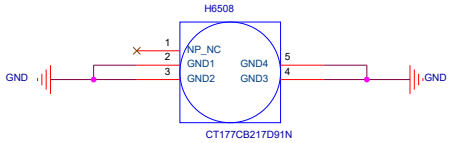
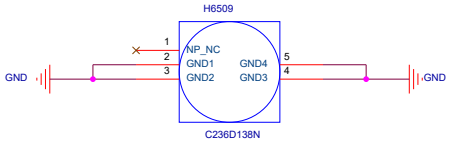
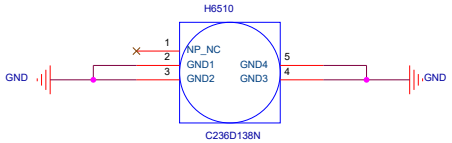


s13036



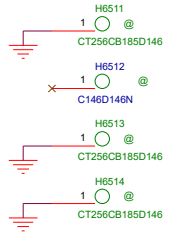
s06383



s06383

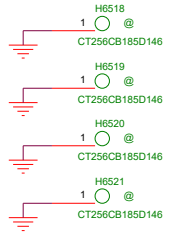
GPU

TOP 3.7/6.5, BOT 3.7/4.7

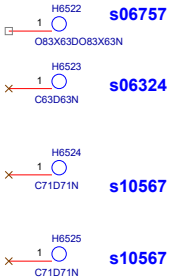


CPU

TOP 3.7/6.5, BOT 3.7/4.7



PCB HOLDER



s06757

s06324

s10567

s10567

<Core Design>

ASUSTeK COMPUTER

Title : I/O board FUNC key

Engineer: EE

Size	Project Name	Rev
B	GA401	1.0

Date: Tuesday, February 11, 2020 Sheet 65 of 104

Title :

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	**GA401**	1.0

Title : I/O board FUNC key

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
B	GA401	1.0

<Core Design>

Title : OTH_for test only

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	GA401	1.0

Date:	Tuesday, February 11, 2020	Sheet	68	of	104

Title : OTH_EMI

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
B	GA401	1.0

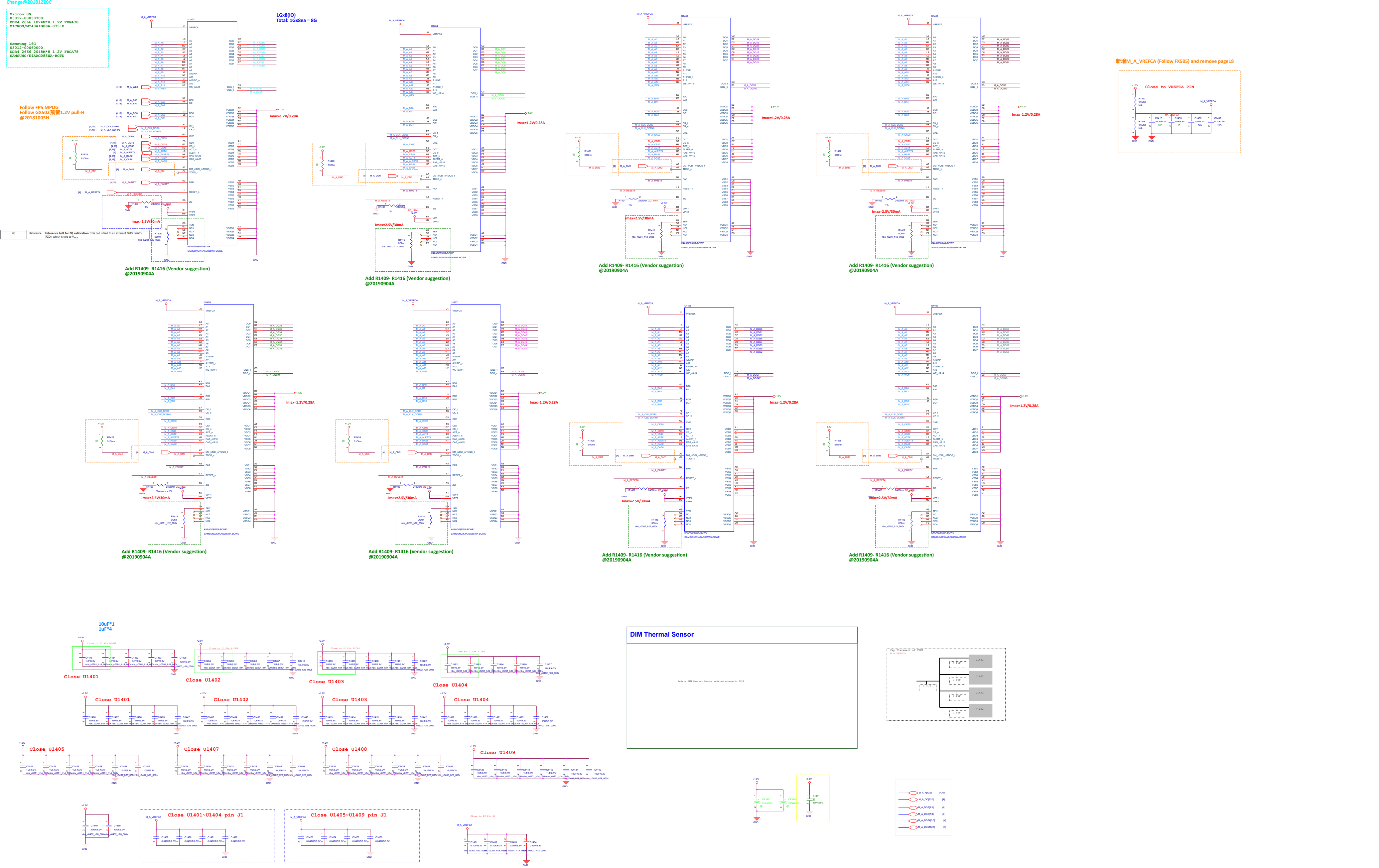


Table 4-25. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x8- 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x8 DRAM device as possible	64x 1µF (0402) (min of 48 stuffed)	
		Distributed around the DRAM devices	20x 10µF (0603) (min of 12 stuffed)	
	VPP	2 as near each x8 DRAM device as possible	32x 1µF (0402)	
		Distributed around the DRAM devices	10x 10µF (0603)	
	VTT	Distributed along termination resistors	32x 1µF (0402)	
		Distributed evenly across domain	8x 10µF (0603)	

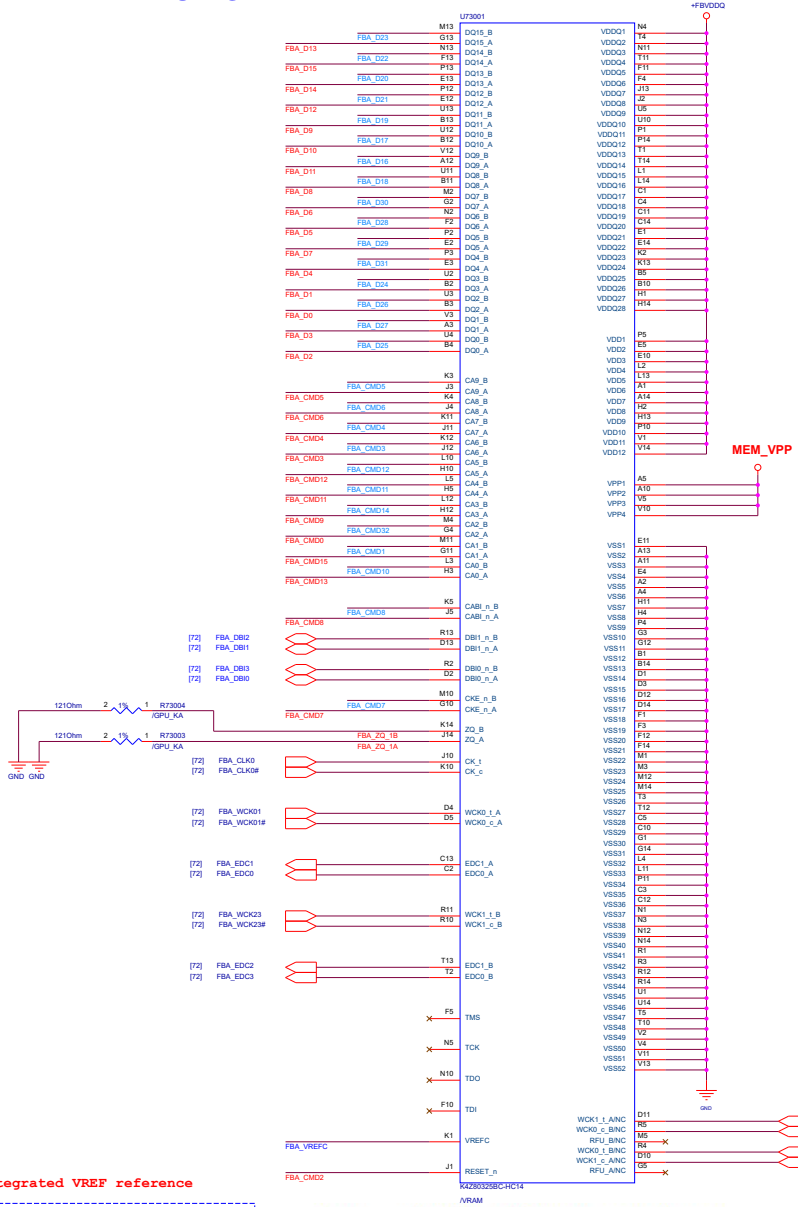
*** POWER

MEM_VPP — MEM_VPP From +1VS_AON [77]

[72] FBA_D[31..0]
[72] FBA_CMD[33..0]

40 OHm_NET
FBA Partition 31..0

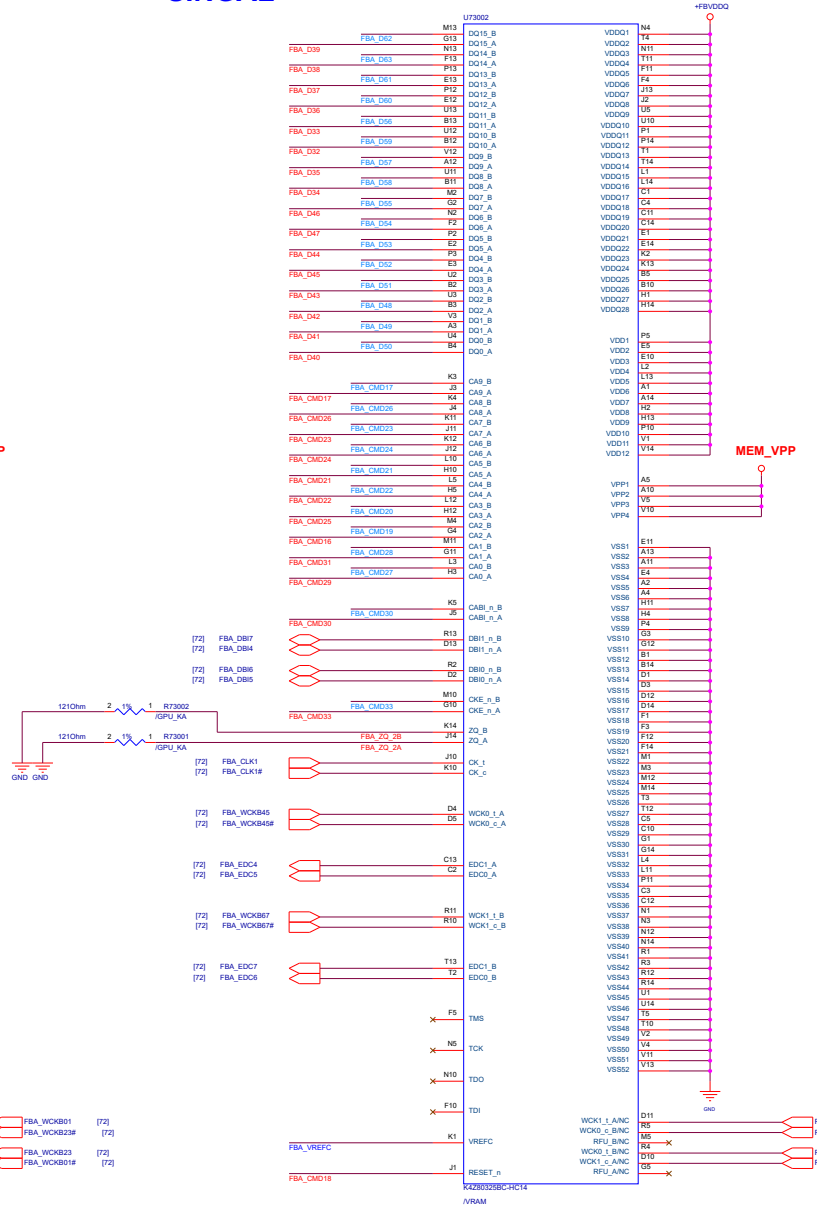
*** SINGAL



[72] FBA_D[63..32]

40 OHm_NET
FBA Partition 64..32

*** SINGAL



Integrated VREF reference

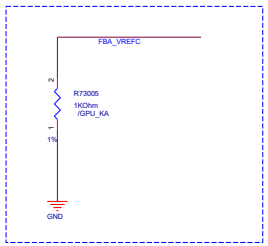


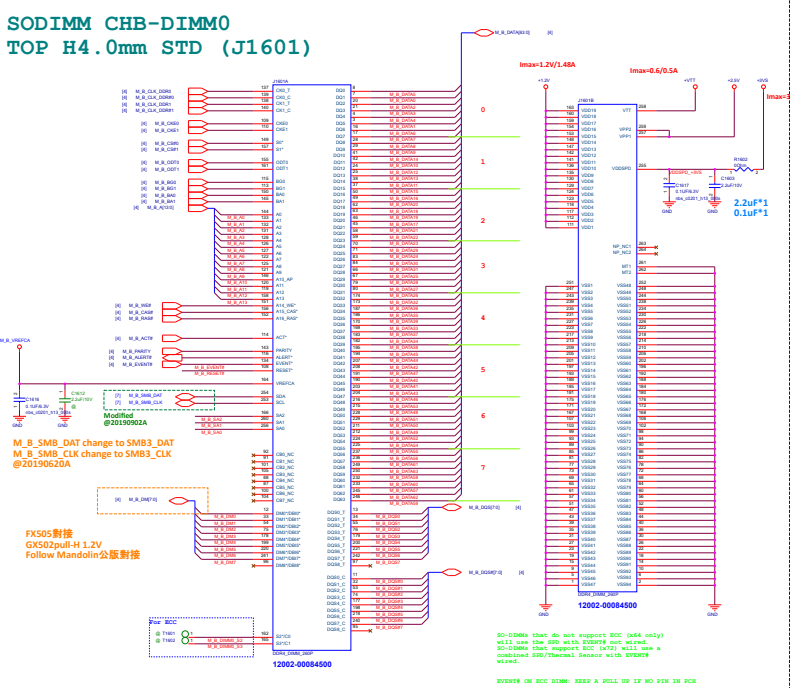
Table 4. N18P-G62/G61 GDDR6 Recommended Memories

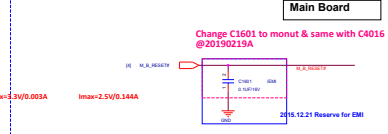
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	Yes, TBD[2]	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	Yes, TBD[2]	Full	Production candidate

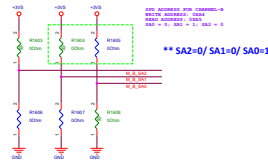
Notes:
1. For N18P-G62/G61, the maximum allowable memory case temperature is 95 °C.
2. Requires Production GDDR6 with a specific date code restriction. Exact date code is currently TBD.

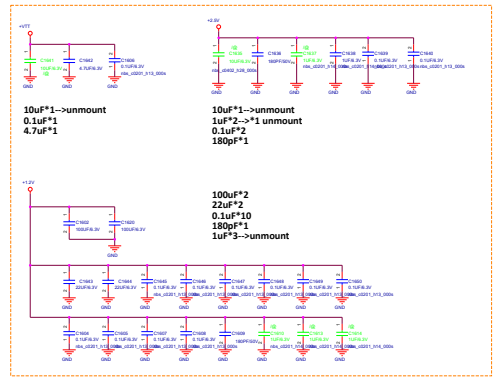
ASUS	Project Name: G512LI		Rev: R1.0
Title : VRAM_Channel_A			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, February 11, 2020	Sheet 73 of 103		

SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)









Follow FP6 CRB CAP number
@20190701A

新增M_B_VREFCA (Follow FX505) and remove page18

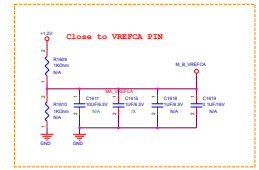


Table 4-24. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10µF (0603)	
		Placed on VTT plane close to DIMM	4x 1µF (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10µF (0603)	
		DIMM Pin side, 1 per DIMM	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0402)	

DDR4 - 2666MHz (8G)
1st : Hynix - 03A08-00051400
2nd : Samsung - 03A08-00051300
DDR4 - 2666MHz (16G)
1st : Hynix - 03A08-00061400
2nd : Samsung - 03A08-00061500

<Variant Name>

Title <Title>		
Size A1	Document Number G512LI	Rev R1.0
Date: Tuesday, February 11, 2020	Sheet 75 of 103	

<Variant Name>

Title <Title>		
Size A1	Document Number G512LI	Rev R1.0
Date: Tuesday, February 11, 2020	Sheet 76 of 103	

Change to 39 OHM
@20181009P
Change to 0201
@20181015F

[4,14] M_A_A[13:0]

+VTT

C1802 10UF/6.3V nbs_c0402_h28_000s

C1803 @ 10UF/6.3V nbs_c0402_h28_000s

GND

N501

[4,14] M_A_CKE0

[4,14] M_A_ODT0
[4,14] M_A_BG1
[4,14] M_A_ACT#
[4,14] M_A_PARITY

[4,14] M_A_CS#0

[4,14] M_A_WE#
[4,14] M_A_CAS#
[4,14] M_A_RAS#

[4,14] M_A_BA0
[4,14] M_A_BA1
[4,14] M_A_BG0

39OHM R1801 M_A_A8
39OHM R1804 M_A_A11
39OHM R1805 M_A_A13
39OHM R1806 M_A_A1
39OHM R1807 M_A_A7
39OHM R1808 M_A_A3
39OHM R1809
39OHM R1810
39OHM R1811
39OHM R1812
39OHM R1813
39OHM R1814 M_A_A5
39OHM R1815
39OHM R1816 M_A_A0
39OHM R1817 M_A_A2
39OHM R1818 M_A_A4
39OHM R1819 M_A_A6
39OHM R1820 M_A_A9
39OHM R1821 M_A_A10
39OHM R1822 M_A_A12
39OHM R1823 M_A_WE#
39OHM R1824 M_A_CAS#
39OHM R1825 M_A_RAS#
39OHM R1826 M_A_BA0
39OHM R1827 M_A_BA1
39OHM R1828 M_A_BG0

C1812 2 1 @ 0.1UF/10V nbs_c0201_h13_000s GND

R1.0 Hacken 0128 Remove

2017/12/20 Changed by Jason

Remove (Page4 PULL-H)
@20181009M

5.4.3.1.2 DDR4 x8 DRAM Down Layout Guidelines—ADD/CMD/CTL

Figure 53 shows the ADD/CMD/CTL routing model for a single-rank x8 configuration. For SDP DRx8 configuration install Rank 1 DRAMs on opposite side of board and mirror the layout of Rank 0. All signals routed reference either the VSS plane or the VDDIO_MEM_S3 plane.

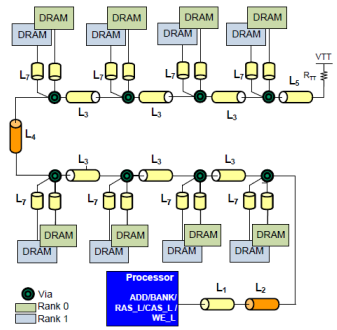


Figure 53. ADD/CMD/CTL Routing Model (DDR4 x8 DRAM Down)

The termination component values for ADD/CMD/CTL are listed in Table 35.

Table 35. Component Table—DDR4 x8 ADD/CMD/CTL Termination

Ref	Value	Tolerance	Package	Comments
R_{TT}	39Ω	5%	0402	ADD/CMD/CTL termination to VTT

Change to 39 OHM
20181009P

Change to 0.1UF
20181009N

N501 +1.2V C1827 2 1 0.1UF/6.3V nbs_c0201_h13_000s

DIMM_CLOCK_TERM_B

39OHM R1802 M_A_CLK_DDR0 [4,14]

C1801 @ 1.5PF/25V

39OHM R1803 M_A_CLK_DDR#0 [4,14]

Change to 0201 @20181122B

C1805 2 1 @ 0.1UF/10V nbs_c0201_h13_000s GND

Clock Pull up power change from +0.6V to +1.2V (CFL PDG) 20820601

10uF*4
1uF*16

+VTT

C1828 C1829 C1830 C1831 C1832 C1833 C1834 C1835
1UF/6.3V nbs_c0201_h14_000s

GND

Close U1401 Close U1402 Close U1403 Close U1404

+VTT

C1836 C1837 C1838 C1839 C1840 C1841 C1842 C1843
1UF/6.3V nbs_c0201_h14_000s

GND

Close U1405 Close U1407 Close U1408 Close U1409

+VTT

C1804 C1806 C1807 C1808
10UF/6.3V nbs_c0402_h28_000s

GND

<Core Design>

ASUSTeK COMPUTER INC.

Title : DDR4_TERMINATION

Engineer: EE

Size C | Project Name GA401 | Rev 1.0

Date: Tuesday, February 11, 2020 Sheet 18 of 104

EC Chip - IT8225

EC Power

**** Check EC Pin Define

SPI_CLK 10k change to 10 OHM @20181029G

Short Land & 0 ohm

Follow FP6 CRB PN

EC GPIO

Add GPG1 @20190725C

Add @201906288

VCC => +3VS system power ; LPC

VSTBY=>+3VA_EC ;Power supply of EC power

+3VACC=+3VA_EC,
+3VAPLL=+3VA_EC_0906

Add FAN_V_Switch @20181218C

Add @20181219B (EMI request)

AMD_SPI_CLK

M_B_SMB_DAT change to SMB3_DAT
M_B_SMB_CLK change to SMB3_CLK
@20190620A

C3015 Change to mount @20181219B

C3016 Change to mount @20181219B

Add @20190902A

IT5129VG-128/CX

Add U3002 (High speed switch)
@20190904A

Modified PN- 06016-02220000 for cost-effective
@100819A

Table 1. TMUX1101 Truth table

SEL	SWITCH STATE
0	OFF (HI-Z)
1	ON

Table 2. TMUX1102 Truth table

SEL	SWITCH STATE
0	ON
1	OFF (HI-Z)

Support Slave CHG
(Prevent from leakage)

Add @20190702A (From GX502)

** Differ with CRB(1uF) @062258.10

DEEP_S3

** NOTE
1. BT_UART_WAKE_R Should connect to EC
2. WLAN_RST#_EC Should connect to EC

** Remove R3056, R3057

** How to trigger by EC?

Confirm with RF
@20181015K

for load code

Del 1.8V_ON_EC NET, 0910

** Remove R3055 @070919A

Change PWR_LED# to PWR_LED
CHG_LED#_O to CHG_LED#
CHG_LED#_W to CHG_FULL_LED#
@20181017E

Add Pull-L
@20181023R

C3019 Change to mount @20181219B

Change netname and unmount
@20181017E

built-in Battery : mount R1937

LPC_CLKRUN# OD, LPC Power Rail +3VS

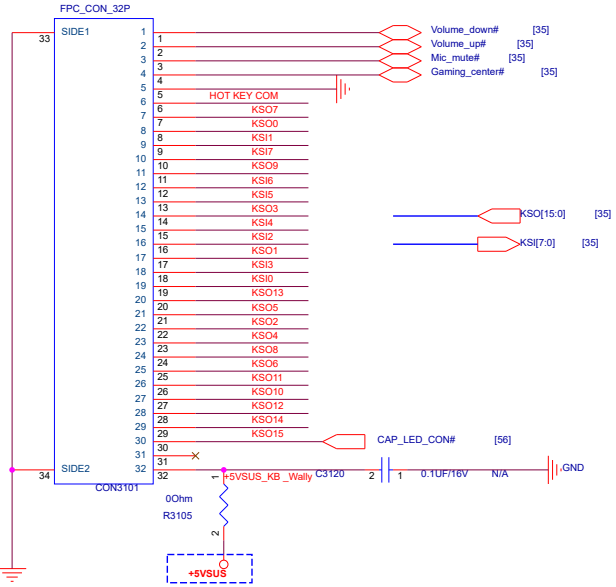
Project Name	GA401
Title :	EC
Dept.:	
Engineer:	
Date:	Tuesday, February 11, 2020

Main Board

Keyboard Connector

** Mirror with Pin Define

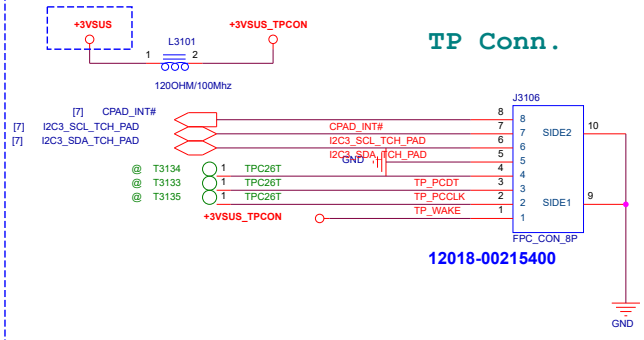
12018-00620100



PIN 1	LED VCC
PIN 2	NC
PIN 3	CapsLock LED
PIN 4	KSO15
PIN 5	KSO14
PIN 6	KSO12
PIN 7	KSO10
PIN 8	KSO11
PIN 9	KSO6
PIN 10	KSO8
PIN 11	KSO4
PIN 12	KSO2
PIN 13	KSO5
PIN 14	KSO13
PIN 15	KSI0
PIN 16	KSI3
PIN 17	KSO1
PIN 18	KSI2
PIN 19	KSI4
PIN 20	KSO3
PIN 21	KSI5
PIN 22	KSI6
PIN 23	KSO9
PIN 24	KSI7
PIN 25	KSI1
PIN 26	KSO0
PIN 27	KSO7
PIN 28	Hot key com
PIN 29	C4
PIN 30	C3
PIN 31	C2
PIN 32	C1

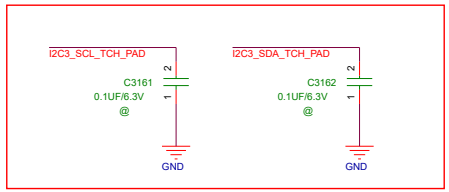
** ADD TP PIN DEFINE @070319A

Pin Assignment and Description			
Pin#	Signal	I/O	Description
1	VCC	VCC	VCC, 3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.
2	WAKE	O	Just pin reserved in the connector for system wake-up
3	PS2_CLK (Just pin reserved)		Not connected (Just reserve pin in the connector)
4	PS2_DATA (Just pin reserved)		Not connected (Just reserve pin in the connector)
5	GND	GND	Ground
6	I²C_SDA	I/O	I²C data.
7	I²C_SCL	I/O	I²C clock
8	/INT	O	Indicates touchpad likes to send data to system (host)

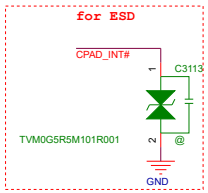


12018-00215400

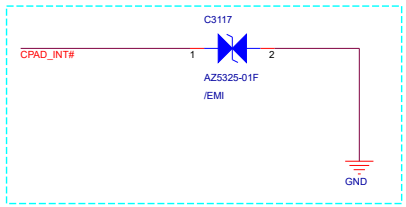
EMI Reserve
如要上件請確認容值(選擇Pico等級)

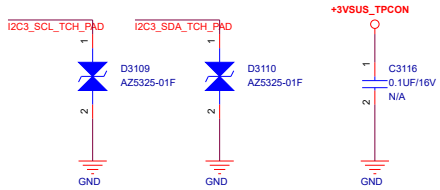


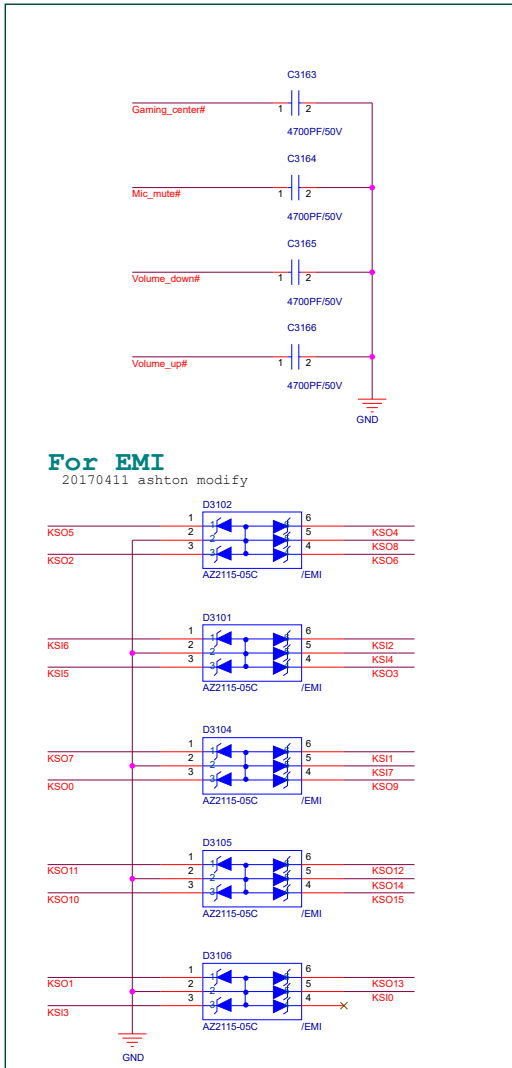
D3110 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



Add @20181219B (EMI request)



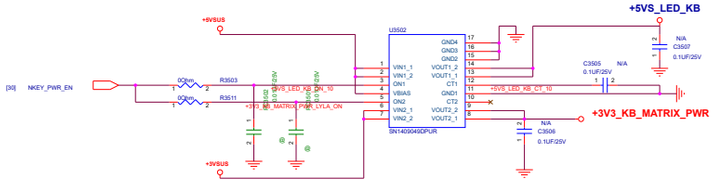


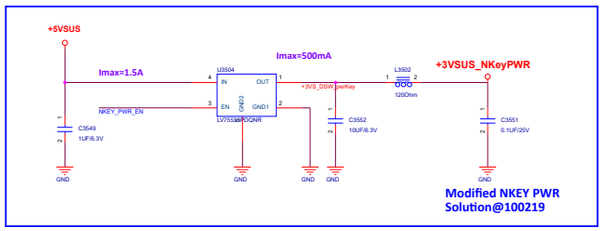


<Variant Name>

ASUSTeK COMPUTER		Title :	KBC_KB & TP
		Engineer:	EE
Size	Project Name		Rev
B	GA401		R1.0
Date: Tuesday, February 11, 2020		Sheet 31 of 104	

N_KEY_IT8299E

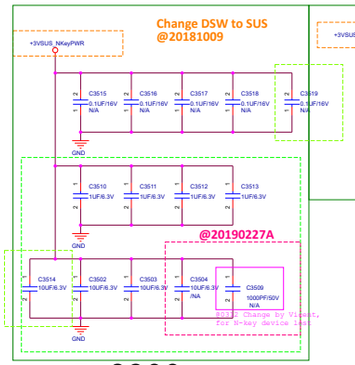




Nkey_Power

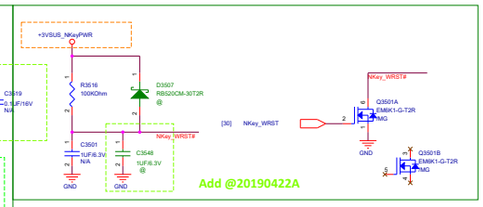
Add @20190422A

Change DSW to SUS
@20181009



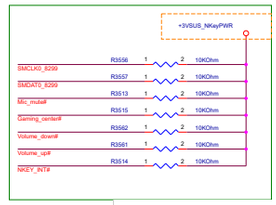
IT8299E

For EC Reset N_key



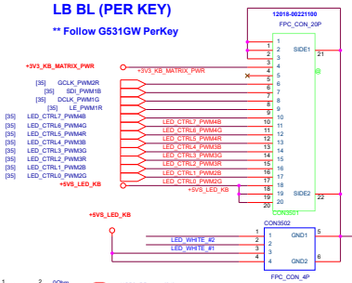
Pull up

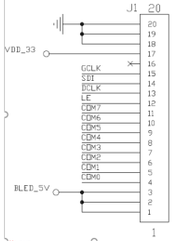
Change DSW to SUS
@20181009



LB BL (PER KEY)

** Follow G531GW PerKey

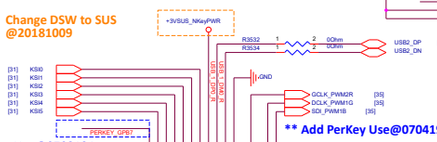




LB BL (WHITE)

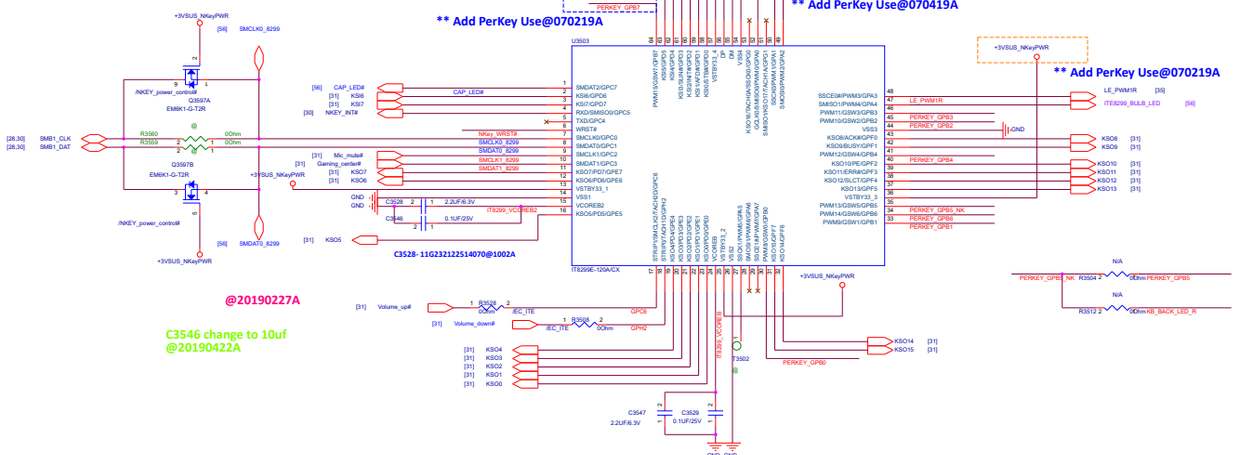
** Follow GA502IV

Change DSW to SUS
@20181009

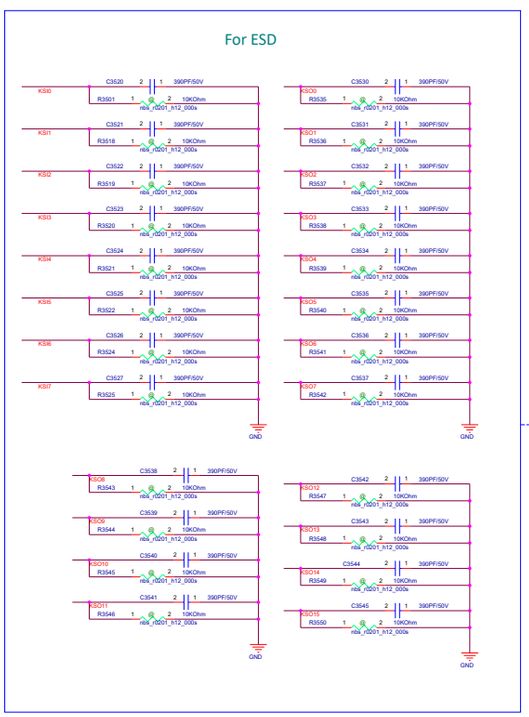


** Add PerKey Use@070419A

** Add PerKey Use@070219A



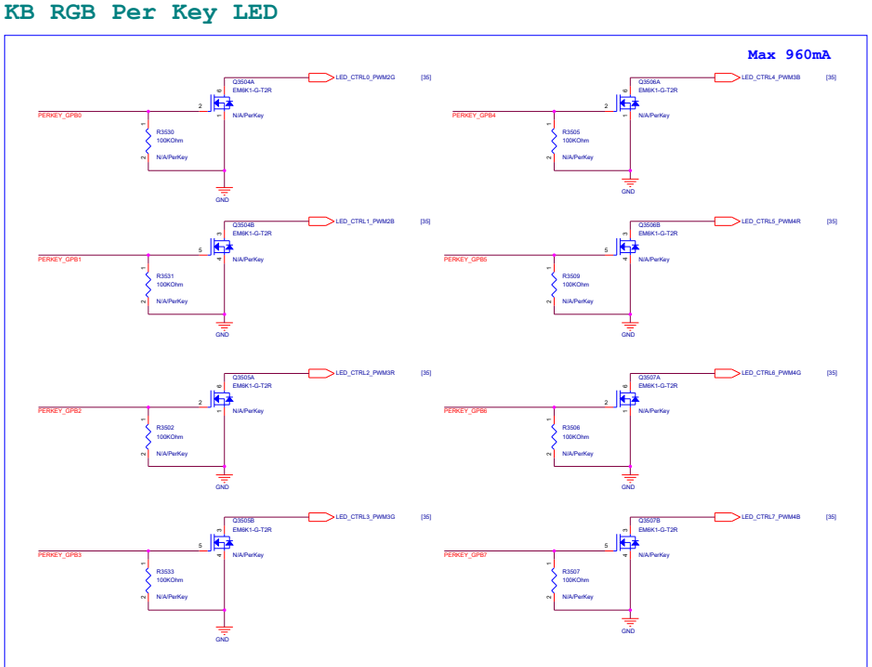
** Add PerKey Use@070219A



** Add PerKey Use@070219A WALLY

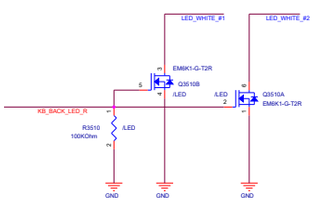
KB RGB Per Key LED

Max 960mA



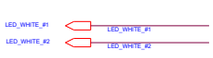
KB WHITE LED

** Add PerKey Use@070219A



*** POWER

*** SINGAL



*** POWER

** [R.88] +3VS — +3VS
** [R.87] +3VSUS — +3VSUS
** [R.87] +1.8VS — +1.8VS
** [R.84] +1.8VSUS — +1.8VSUS
** [R.88] +5VS — +5VS
** [R.87] +5VSUS — +5VSUS
** [R.87] +12VS — +12VS
** [R.87] +12VSUS — +12VSUS
+3VA_EC — +3VA_EC

*** SINGAL

** PCH Control

[7] A_Z_BITCLK — A_Z_BITCLK
[7] A_Z_SYNC — A_Z_SYNC
[7] A_Z_SDIN0 — A_Z_SDIN0
[7] A_Z_SDOUT — A_Z_SDOUT

** EC Control

[30] AMP_SLEEP# — AMP_SLEEP#
[30] OP_SD# — OP_SD#

** Jack Control

[37] EAPD# — EAPD#
[37] TOU_CON_L — TOU_CON_L

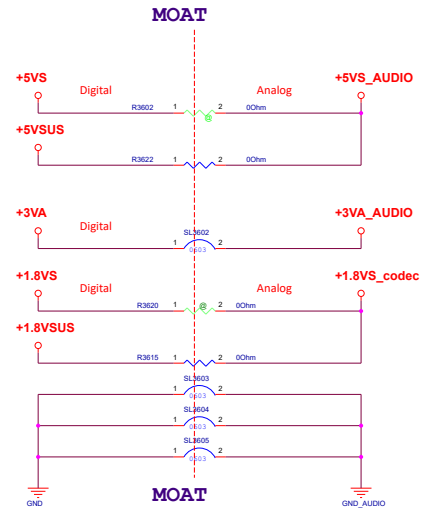
*** To EXT. Amp.

[39] I2S_Codec_SDIN — I2S_Codec_SDIN
[39] I2S_Codec_SDOUT — I2S_Codec_SDOUT
[39] I2S_BCLK — I2S_BCLK
[39] I2S_LRCLK — I2S_LRCLK

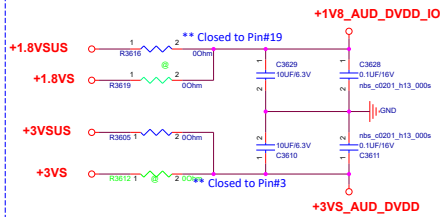
*** Headset Connection

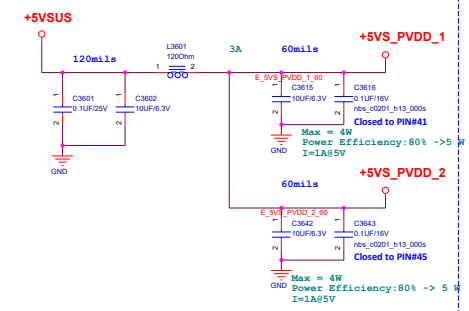
[37] LINE1_R — LINE1_R
[37] LINE1_L — LINE1_L
[37] MIC2_R_SLEEVE — MIC2_R_SLEEVE
[37] MIC2_L_RING2 — MIC2_L_RING2
[37] MIC2_VREFO_R — MIC2_VREFO_R
[37] MIC2_VREFO_L — MIC2_VREFO_L
[37] HPOUT_L — HPOUT_L
[37] HPOUT_R — HPOUT_R

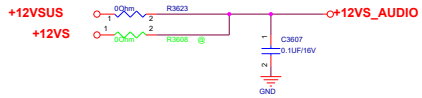
** PWR DISTRIBUTION (ANALOG)



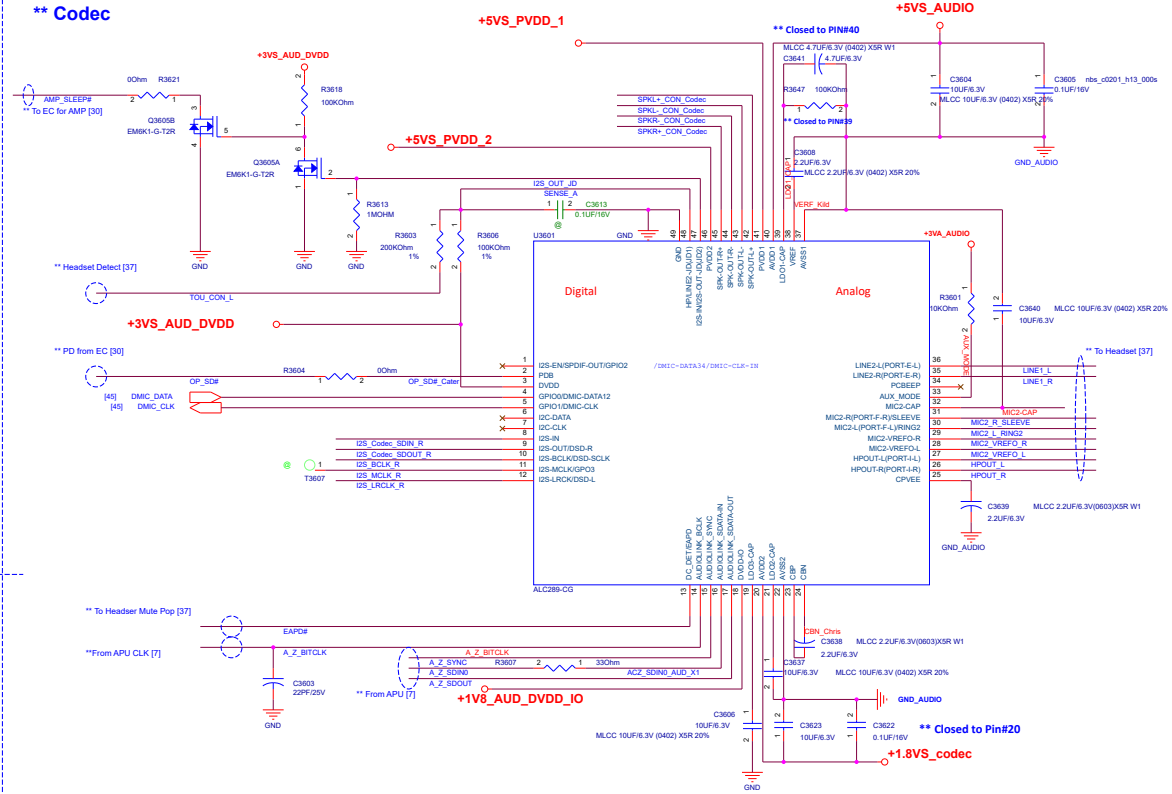
** PWR DISTRIBUTION (DIGITAL)



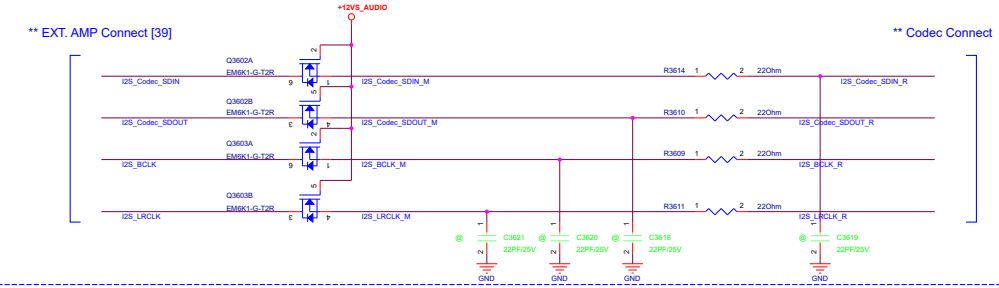




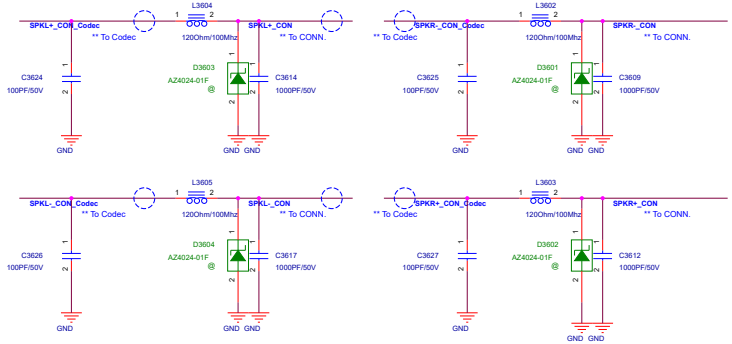
** Codec



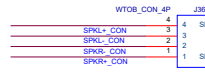
** EXT. AMP Connection



** Tweeter AMP CONN.

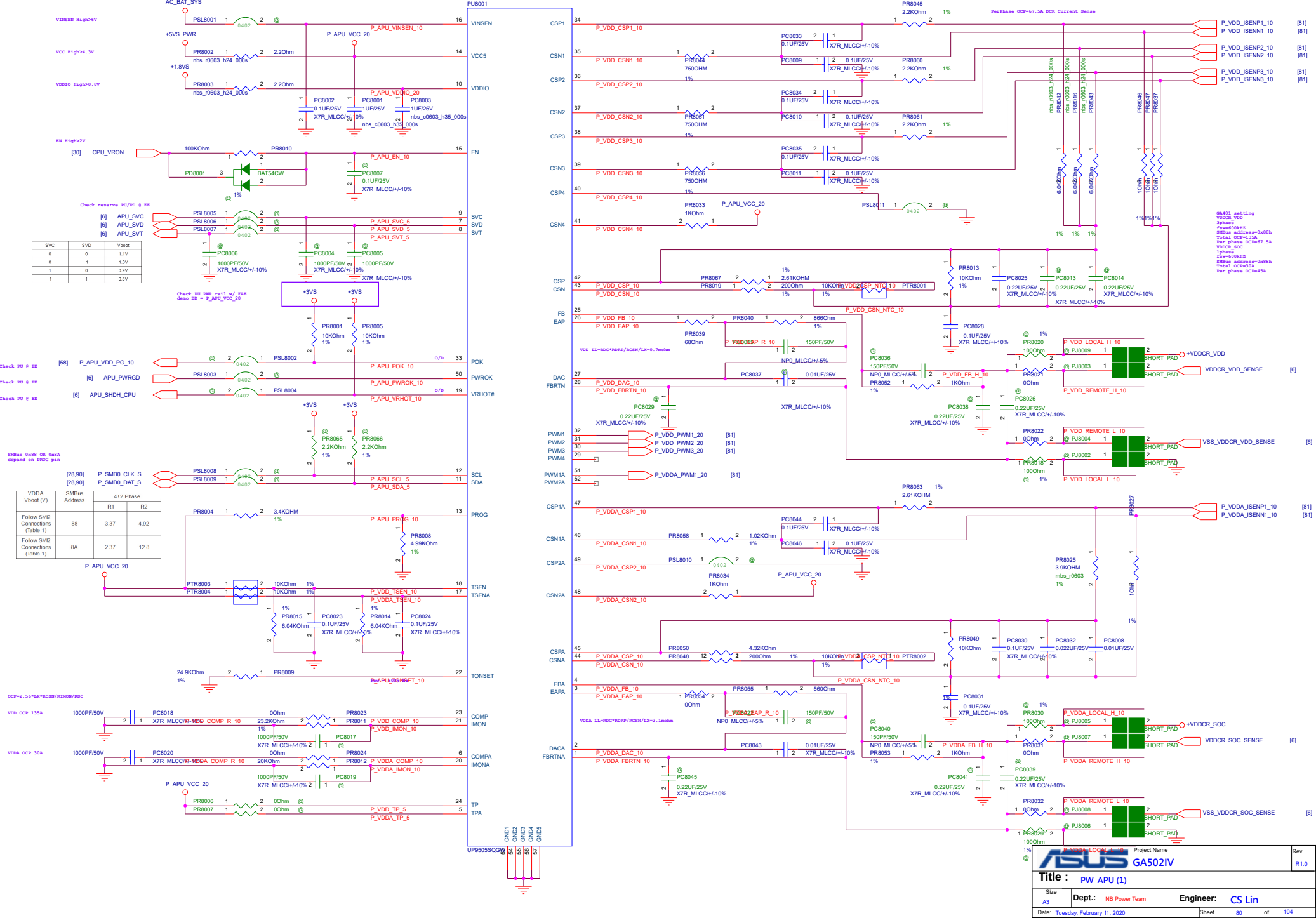


12017-00330300



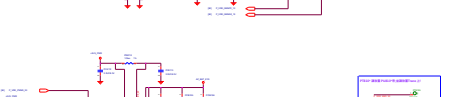
<Core Design>

Project Name: ALC285+SMARTAMP		Rev: R1.3
Title : AUD-ALC285		
Size: C	Dept.: ASUSTeK COMPUTER INC. Engineer: NB1 RD2 EE1	
Date: Tuesday, February 11, 2020	Sheet 36 of 104	



SVC	SVD	Vboot
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

VDDA Vboot (V)	SMBus Address	4+2 Phase	
		R1	R2
Follow SVI2 Connections (Table 1)	88	3.37	4.92
Follow SVI2 Connections (Table 1)	8A	2.37	12.8

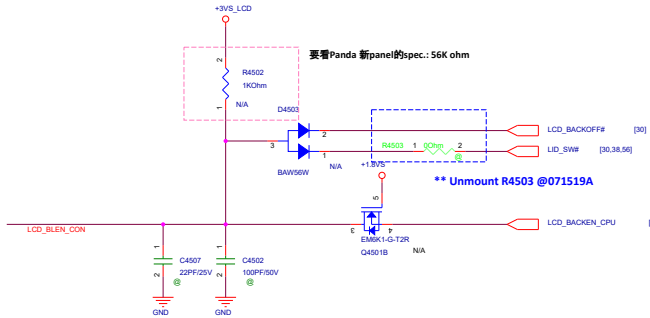


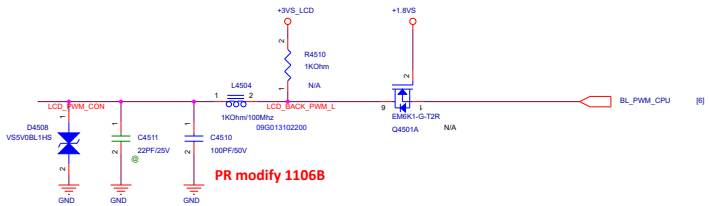
*** POWER

*** SINGAL

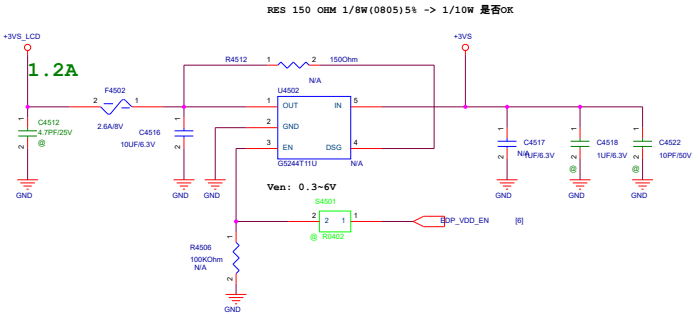
** Note
1. DMIC Add FUSE

Controll Signal (LCD/BL)

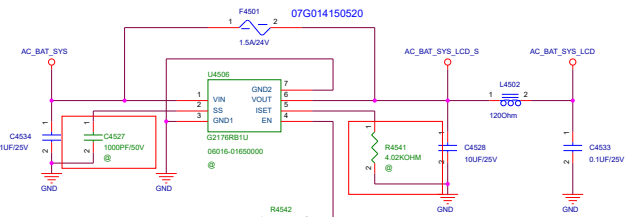




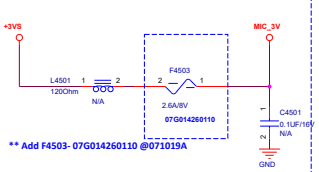
LCD VDDEN / +3VS_LCD

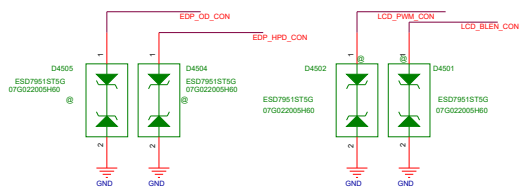


** Panel BL Power



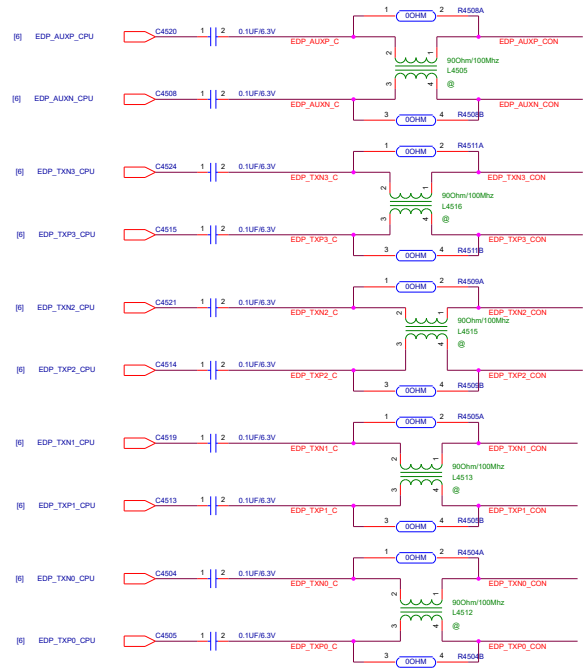
** MIC PWR





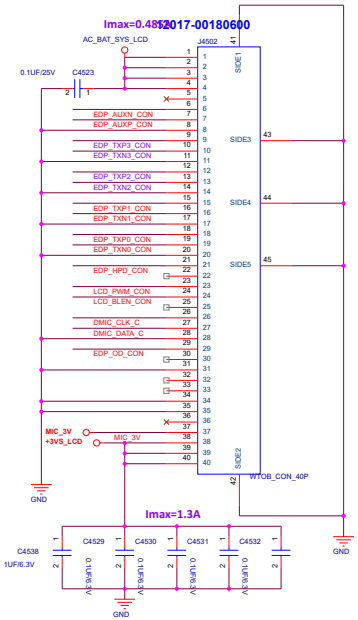
eDP from CPU

For EMI

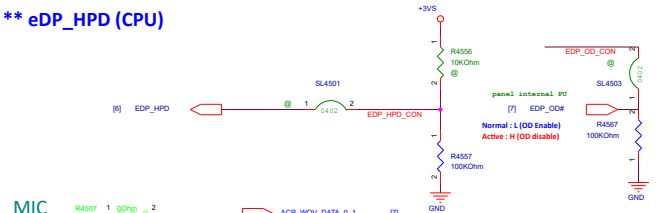


** Modified the LCM CONN@07002219

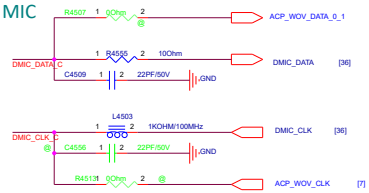
eDP Panel Conn.



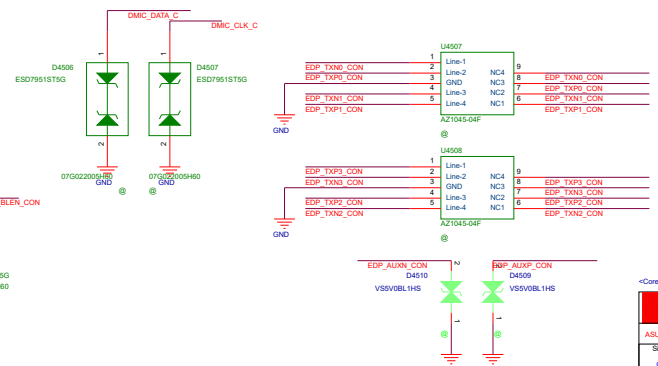
** eDP_HPD (CPU)



MIC



** For ESD



M/B side (CN1)

Pin	Pin define	wire count	
1	LCD_VCC	1	<100m ohm
2	LCD_VCC	1	
3	LCD_VCC	1	
4	MIC_3V_SS	1	
5	NC		
6	H_GND	1	<100m ohm
7	H_GND	1	
8	NC		
9	NC		
10	H_GND	1	<100m ohm
11	NC		
12	OD	1	
13	H_GND	1	<100m ohm
14	DMIC_DATA_R	1	50 ohm
15	DMIC_CLK_R	1	
16	NC		
17	BL_Enable	1	
18	BL PWM DIM	1	
19	NC		
20	HPD	1	
21	H_GND	1	
22	LaneO_N	1	Coaxial 90 ohm
23	LaneO_P	1	
24	H_GND	1	
25	Lane1_N	1	Coaxial 90 ohm
26	Lane1_P	1	
27	H_GND	1	
28	Lane2_N	1	Coaxial 90 ohm
29	Lane2_P	1	
30	H_GND	1	
31	Lane3_N	1	Coaxial 90 ohm
32	Lane3_P	1	
33	H_GND	1	
34	AUX_CH_P	1	Coaxial 90 ohm
35	AUX_CH_N	1	
36	NC		
37	BL_PWR	1	<100m ohm
38	BL_PWR	1	
39	BL_PWR	1	
40	BL_PWR	1	

<Core Design>

ASUSTeK COMPUTER

Title : CRT_eDP

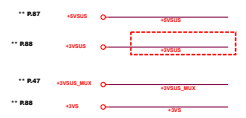
Engineer: EE

Size	Project Name	Rev
C	GA401	1.0

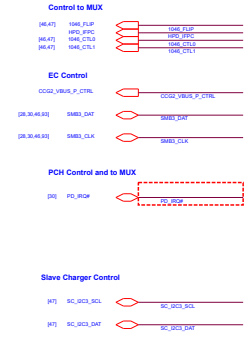
Date: Tuesday, February 11, 2020 Sheet 45 of 104

Main Board

*** POWER



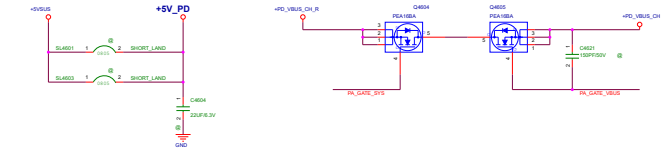
*** SINGAL

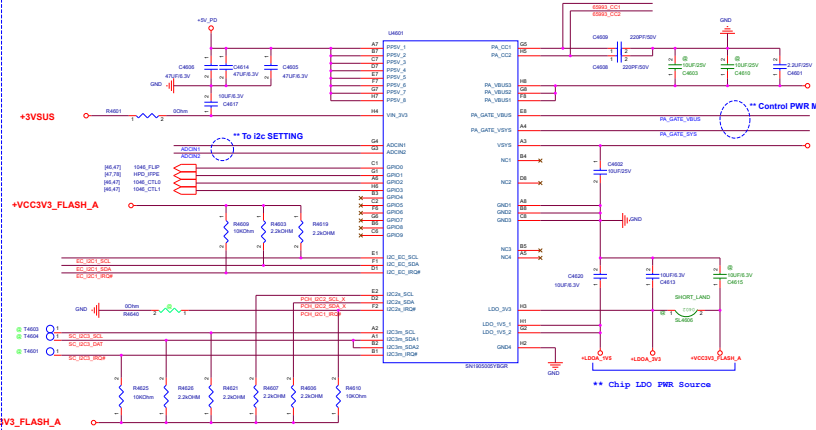


*** Note

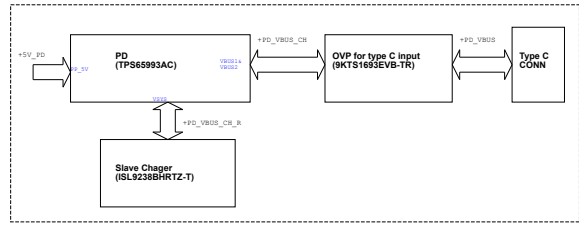
1. Check wtih IP for Power Supply path?

Imax=1port+1CC=3.6A

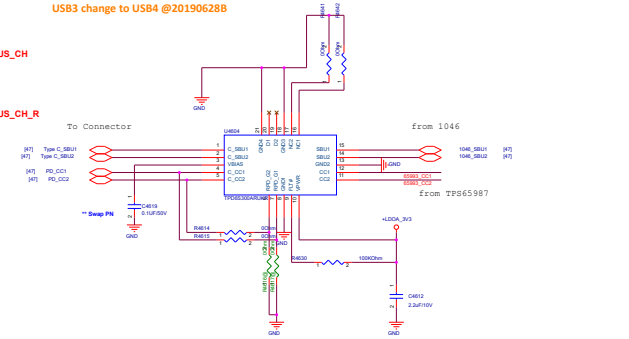




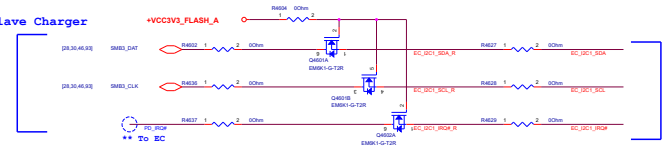
Power Flow Chart



USB3 change to USB4 @20190628

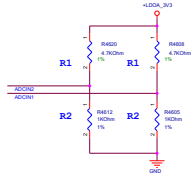


** EC & Slave Charger



** Connect to EC/ PCH/ Slave Charger

** I2C Default Slave Address ->
0x20 (7 bits)/ W: 0x42 R: 0x43



$DIV = R_{Down} / (R_{Up} + R_{Down})$ [1] MIN	MAX	Without using R_{Up} or R_{Down}	ADCINx decoded value
0.0229	0.0722	N/A	1
0.0723	0.1423	N/A	2
0.1425	0.2372	N/A	3
0.2373	0.3671	N/A	4
0.3672	0.5364	tie to LDO_1V5	5
0.7855	0.9880	N/A	6
0.9881	1.0	tie to LDO_3V3	7

Table 7. Device Configuration using ADCIN1 and ADCIN2 .

ADCIN1 decoded value [1]	ADCIN2 decoded value [1]	I²C address Index [2]	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	0	#3	
1	7	#4	
7	4	#1	SinkRequires_3.0A [3]: The device only enables the sink path if the attached source is offering at least 3.0A. USB PD is disabled until configuration is loaded.
4	4	#2	
3	0	#3	
2	7	#4	
7	5	#1	SinkRequires_1.5A [3]: The device only enables the sink path if the attached source is offering at least 1.5A. USB PD is disabled until configuration is loaded.
6	6	#2	
5	5	#3	
6	7	#4	
7	0	#1	SafeMode: The device does not enable the sink path. USB PD is disabled until configuration is loaded. Note that the configuration could put the device into a source-only mode.
0	0	#2	
6	0	#3	
5	7	#4	

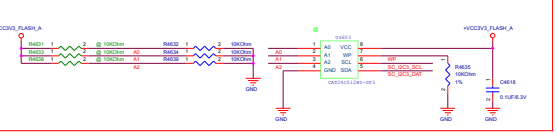
Table 6. I²C Default Slave Address for I2C_EC_SCL/SDA.

I²C address Index (decoded from ADCIN1 and ADCIN2) [1]	Port	Slave Address Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Available During BOOT
#1	A	0	1	0	0	0	0	0	R/W	Yes
#2	A	0	1	0	0	0	0	1	R/W	Yes
#3	A	0	1	0	0	0	1	0	R/W	Yes
#4	A	0	1	0	0	0	1	1	R/W	Yes

Table 3. Decoding of ADCIN1 and ADCIN2 pins.

$DIV = R_{Down} / (R_{Up} + R_{Down})$ [1] MIN	MAX	Without using R_{Up} or R_{Down}	ADCINx decoded value
0	0.0229	tie to GND	0

I2C ROM ** Add I2C address (0xA0)!!!



ASUS	Project Name: Type-C_ALT_USB3-1GG + DP + PD + Slave_Charger_TI		Rev: 1.0
Title :	PD_TPS65987DDJ		
Size: Custom	Dept.: ASUSTEK COMPUTER INC	Engineer: Design IP	
Date: Tuesday, February 11, 2020	Sheet: 40 of 104		

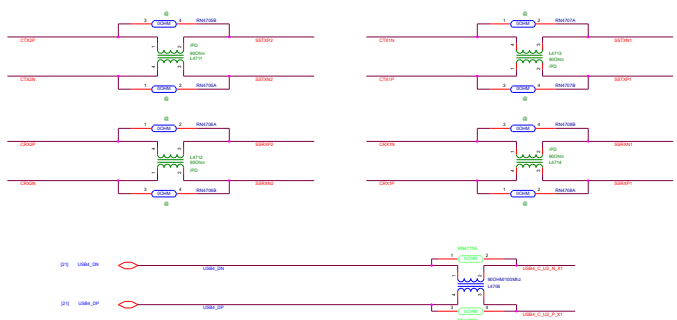
<Core Design>

ASUSTeK COMPUTER	Title : OTH_for test only	
	Engineer: EE	
Size: A	Project Name: GA401	Rev: R1.2
Date: Tuesday, February 11, 2020	Sheet 82 of 104	

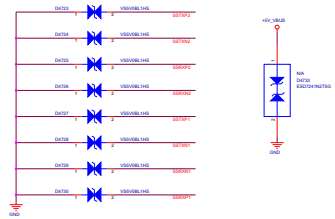
*** POWER

*** SINGAL

USB EMI-Protection



USB3.0 ESD-Protection

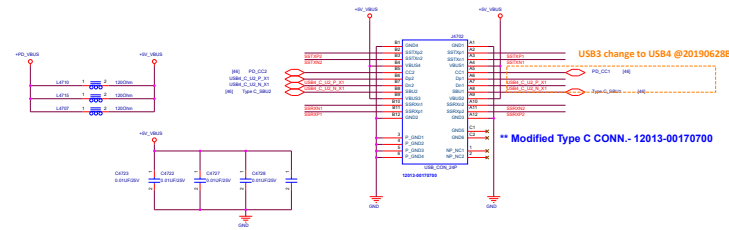


NOTE 8. PIN ASSIGNMENT (FRONT VIEW)

Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
	GND	TX1+	TX1-	V_{BUS}	CC1	D+	D-	SBU1	V_{BUS}	RX2-	RX2+	GND
	GND	RX1+	RX1-	V_{BUS}	SBU2	D-	D+	CC2	V_{BUS}	TX2-	TX2+	GND
Pin No.	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

NOTE 9. LASER WELD POINTS MAY BE DISCOLORED.

TYPE-C Connector

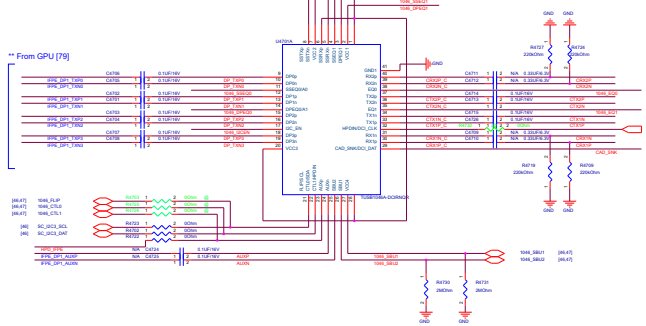


USB3 change to USB4 @20190628B

** Modified Type C CONN.- 12013-00170700

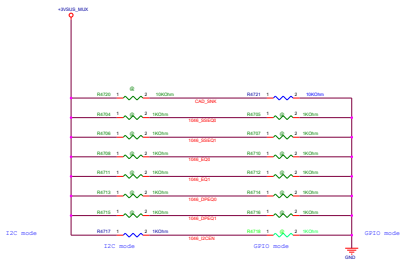
** APU Connection [21]

** From GPU [79]



HPD_IFPC change to HPD_IFPE @20190628B

*** GPIO Setting and OD Pull High



Change to I2C mode @20190909A

Table 2. GPIO Configuration Control

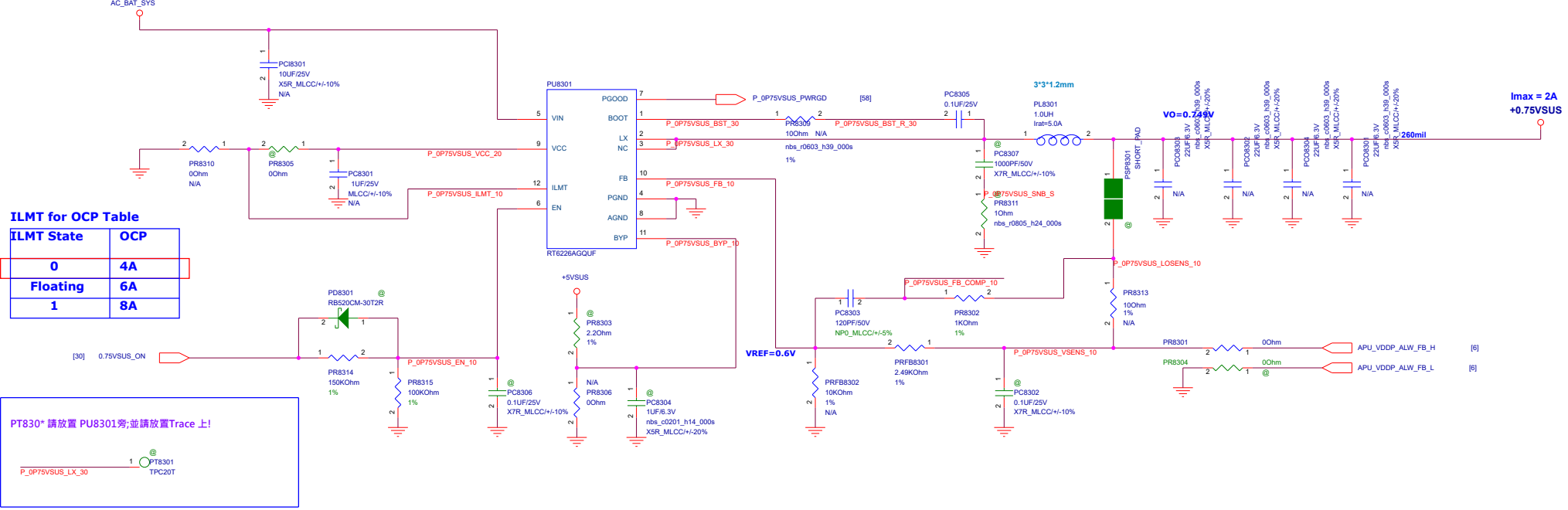
CTL1 PIN	CTL0 PIN	FLIP PIN	TUSB1046-DCI CONFIGURATION	VESA DisplayPort ALT MODE DFP_D CONFIGURATION
L	L	L	Power Down	—
L	L	H	Power Down	—
L	H	L	One Port USB 3.1 - No Flip	—
L	H	H	One Port USB 3.1 – With Flip	—
H	L	L	4 Lane DP - No Flip	C and E
H	L	H	4 Lane DP – With Flip	C and E
H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D and F
H	H	H	One Port USB 3.1 + 2 Lane DP– With Flip	D and F

ASUS Project Name: Type-C_ALT_USB3-1G3 + DP + PD + Slave_Charger_TI Rev 2.0

Title : USB3.1 TYPE-C+TI 1046A

Size: D Dept.: ASUSTeK COMPUTER INC Engineer: Design IP

Date: Tuesday, February 11, 2020 Sheet 67 of 104



ILMT for OCP Table

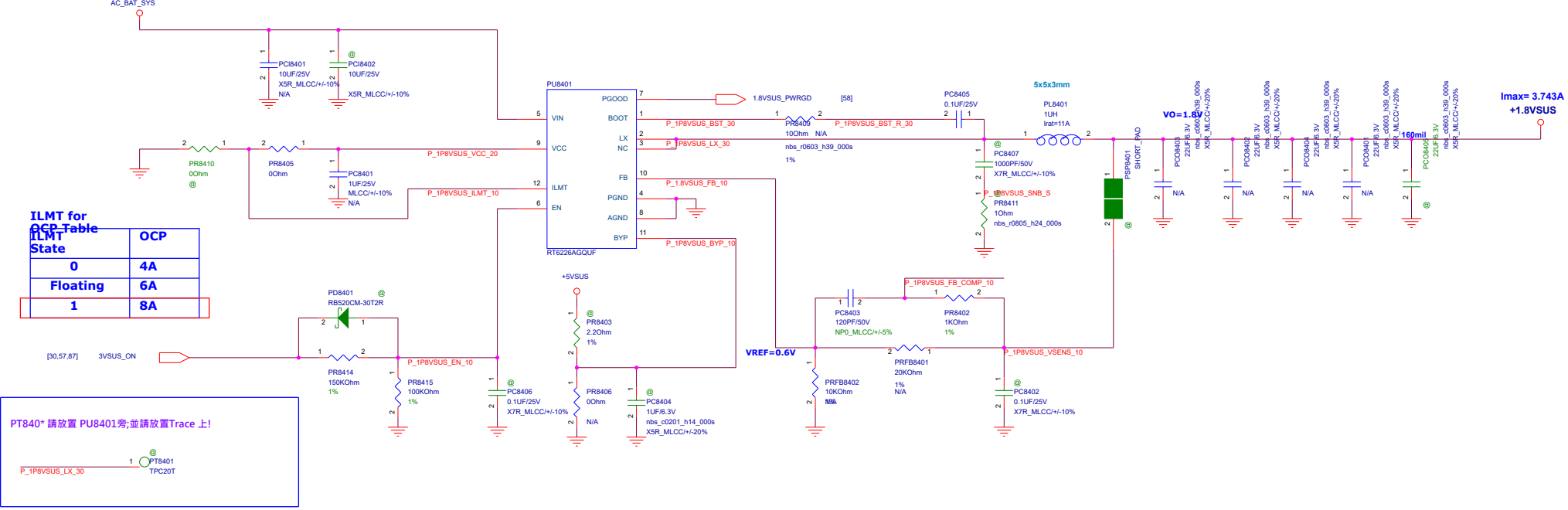
ILMT State	OCP
0	4A
Floating	6A
1	8A

PT830* 請放置 PU8301旁;並請放置Trace 上!

P_0P75VSUS_LX_30 — PT8301 TPC20T

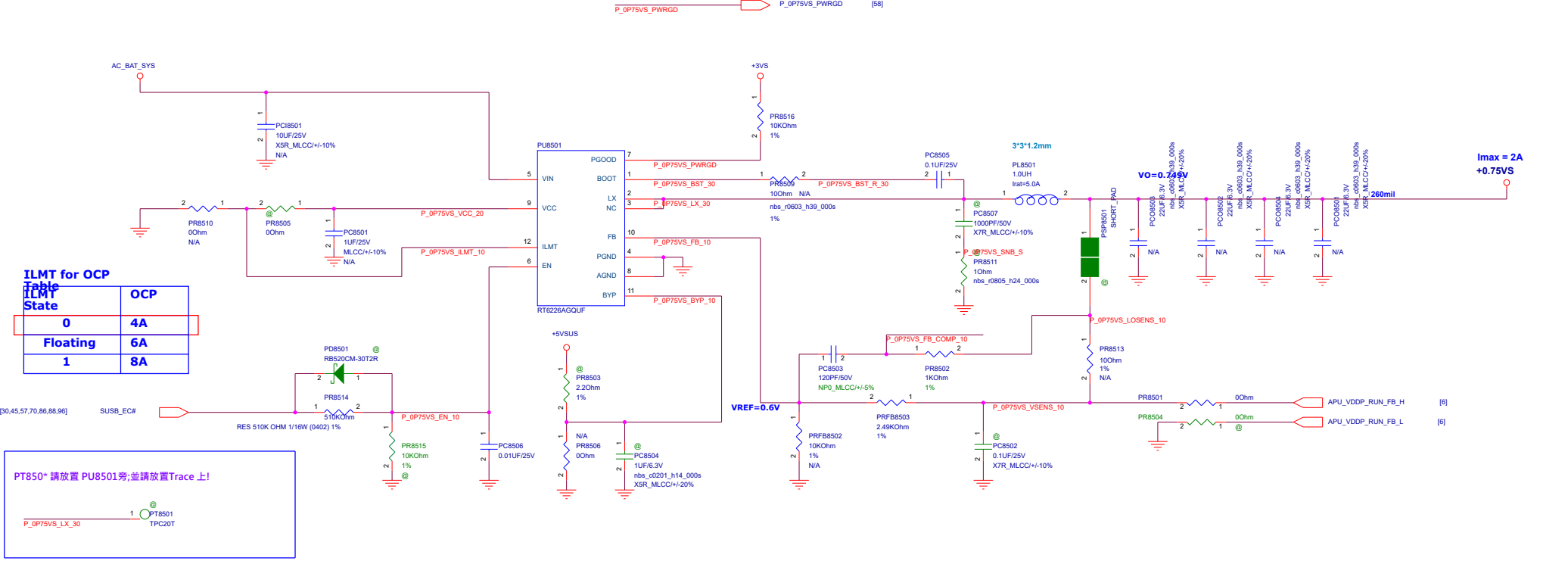
<Variant Name>

ASUS	Project Name: GA502IV		Rev: R1.0
Title : PW_+0.75VSUS			
Size: A3	Dept.: NB Power team	Engineer: CS Lin	
Date: Tuesday, February 11, 2020	Sheet 83 of 104		



<Variant Name>

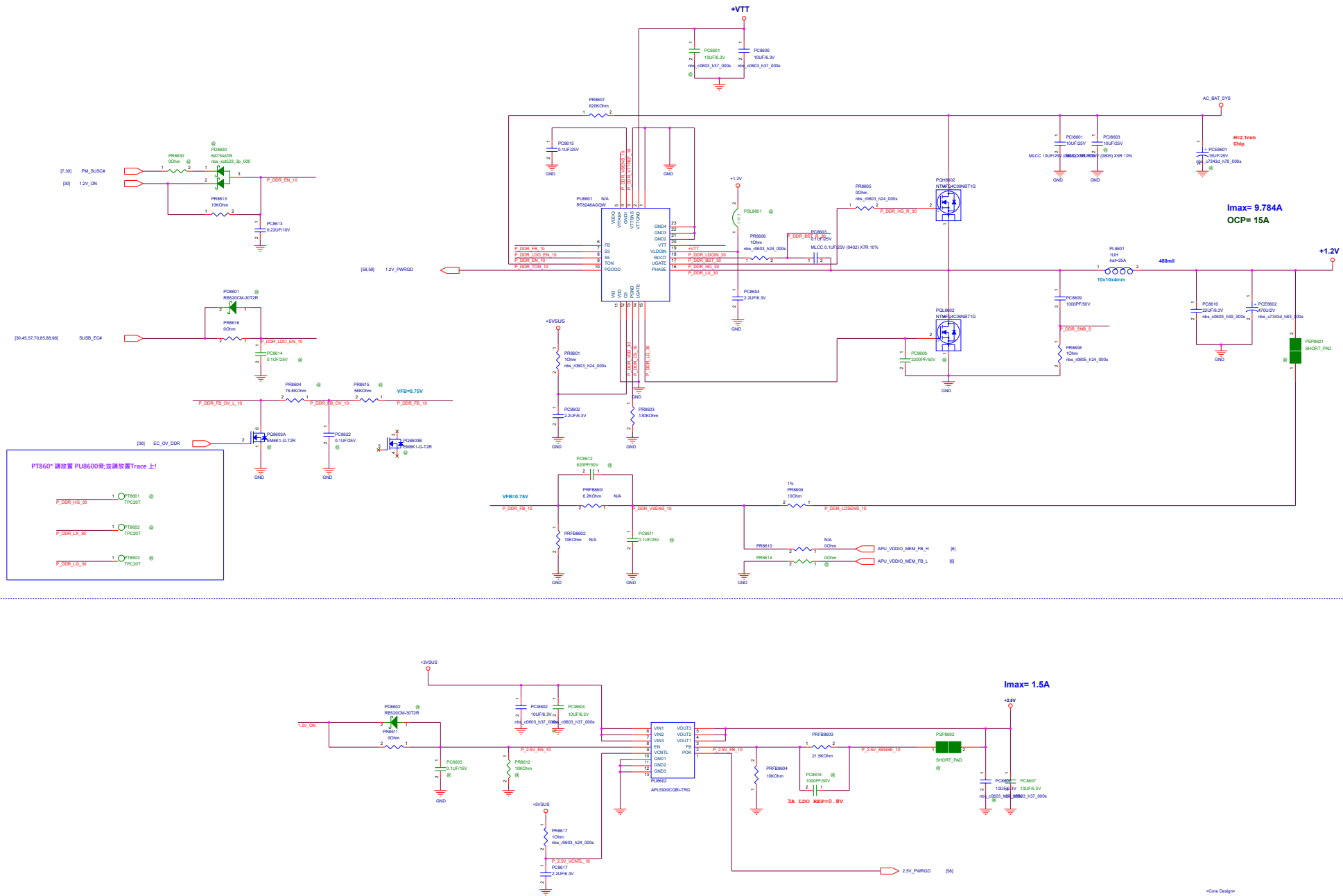
Project Name: GA502IV		Rev: R1.0
Title : PW_+1.8VSUS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Tuesday, February 11, 2020	Sheet 84 of 104	



<Variant Name>

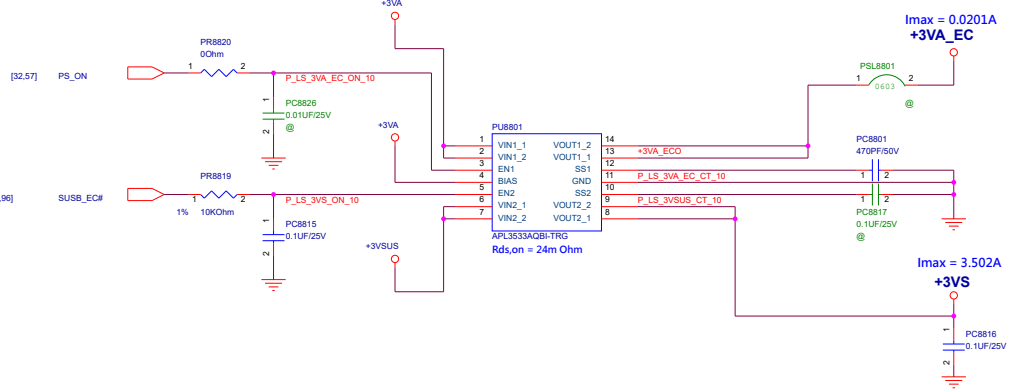
Project Name: GA502IV		Rev: R1.0
Title: PW_+0.75VS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Tuesday, February 11, 2020	Sheet 85 of 104	

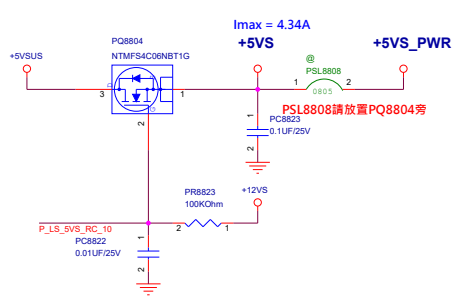
+1.2V / +VTT / +2.5V[For Memory]

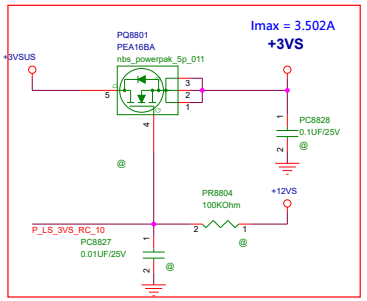


<Core Design>

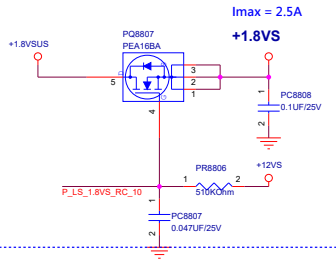
ASUS	Project Name: Coffee Lake-H	Rev: R1.0
Title : PW_+1.2V/+VTT/+2.5V		
Size: A2	Dept.: NB Power team	Engineer: HON
Date: Tuesday, February 11, 2020	Sheet 86 of 104	

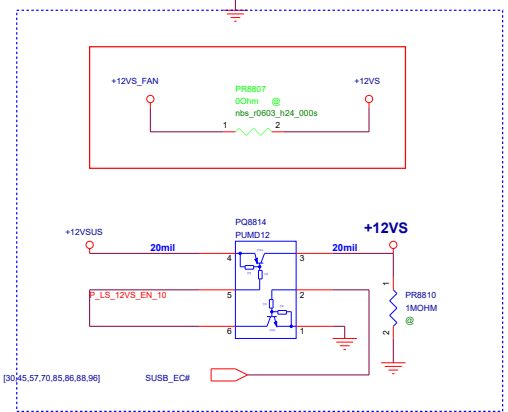






** Remove or not ?? Check with PWR

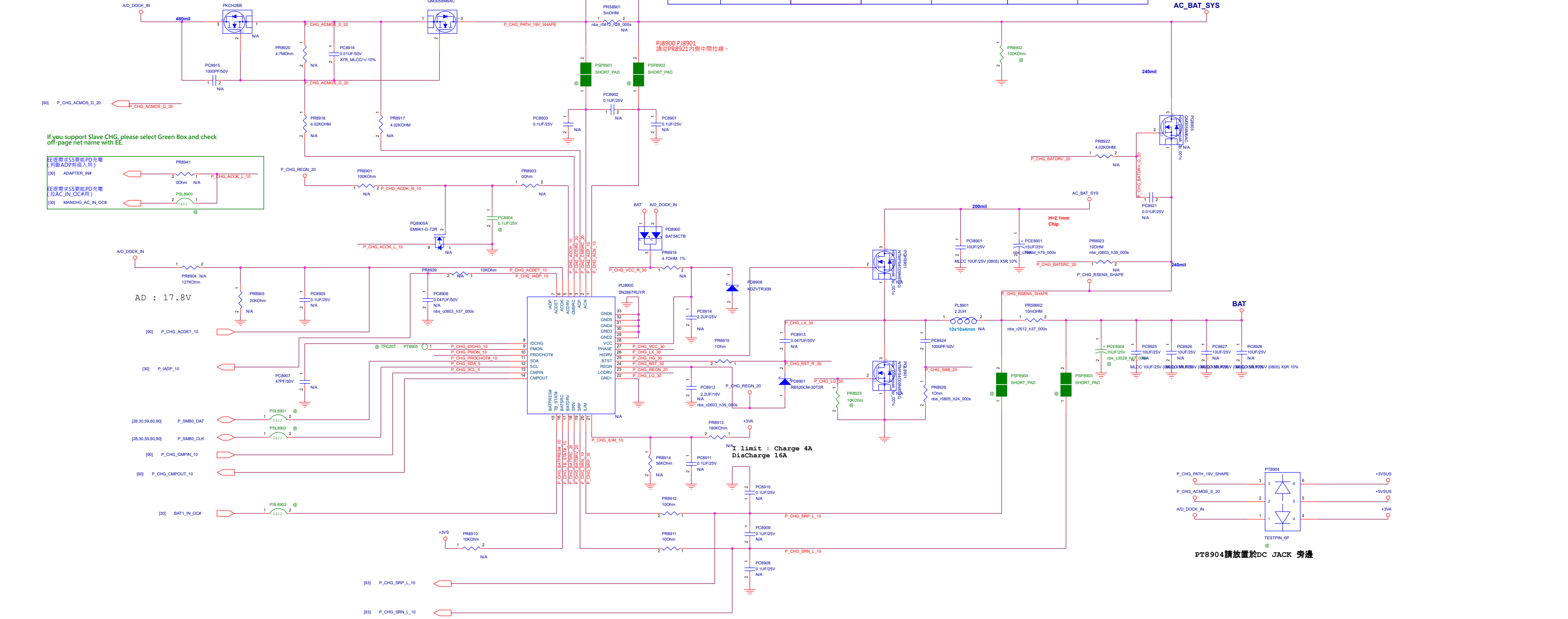


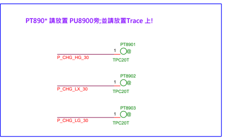


ASUS	Project Name: GA401		Rev: R1.0
Title : PW_LOAD SWITCH			
Size: A3	Dept.: NB Power team	Engineer: Besnon	
Date: Tuesday, February 11, 2020		Sheet 88 of 104	

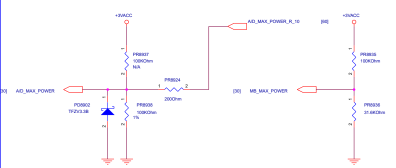
PRS8901	ADP<120W	ADP<=230W	ADP>230W	ADP>330W
	TBD	5m	5m	2m
	TBD	10125-0008B100	10108-0006B000	10108-0008B000

PRS8903	ADP=120W	ADP=150W	ADP=180W	ADP=230W	ADP=280W	ADP=330W
	200m	255m	X	X	X	560m
	10114-0018B000	10114-00221000	X	X	X	10114-00211000

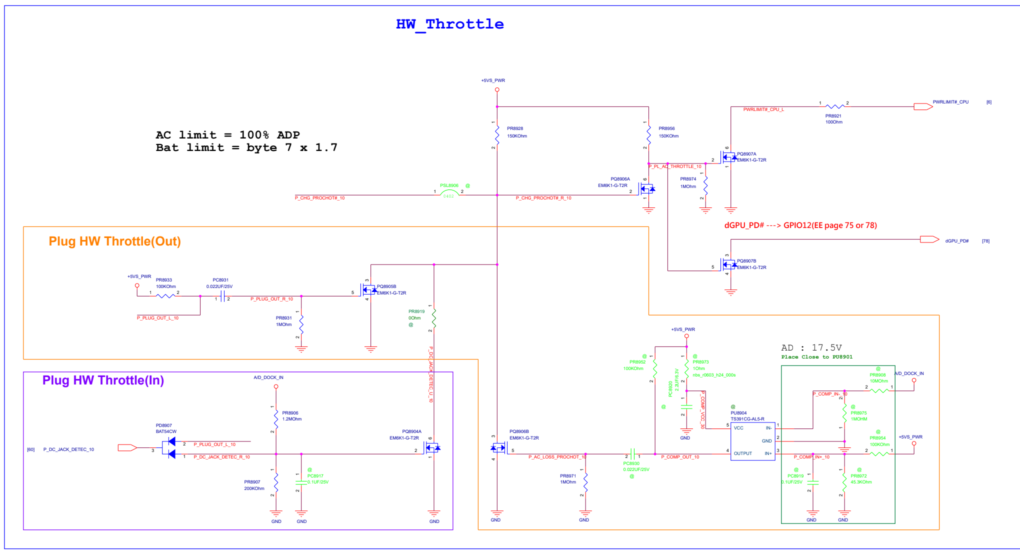


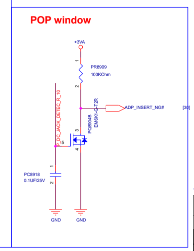


Adaptor select
total power = 90% ADP



Adaptor select			
		X/UX Series	G Series
PRS8901		10m	5m
PR8936			
14K 10G212140214030	0.4V	30W	120W
31.6K 10G212316214030	0.8V	40W	150W
56K 10G212560214030	1.2V	45W	180W
93.1K 10G212931214031	1.6V	65W	230W
150K 10G212150314031	2.0V	75W	300W
270K 10G212270314030	2.4V	90W	330W
560K 10G212560314030	2.8V	120W	400W





Title : PW_CHARGER

Coffee lake-H

Dept.: NB Power Team   Engineer: Benson

Date: Tuesday, February 11, 2020   Sheet 89 of 104   Rev R1.0

+NVVDD [For DGPU]

X50 Ti : PR9117不上件 / PR9115、PR9116上件
X50 : PR9117上件 / PR9115、PR9116不上件

< HW Strap Function setting >
PWM2 : APL_Hys = 13.9A
PWM3 : VAPL1 = 16.7A (1 Phase)
PWM4 : VAPL2 = 34.1A (2 Phase)

Vboot = 0.8V

Per Limit=70A

LL= 0 mohm

Total OC =230A

請放靠近PU9101

Phase訊號請和周圍線、Via盡量保持30mil

Phase訊號請和周圍線、Via盡量保持30mil

Phase訊號請和周圍線、Via盡量保持30mil

<Variant Name>

ASUS	Project Name: G711GW		Rev: R0.0
Title : PW_+NVVDD (1)			
Size: Custom	Dept.: NB Power Team	Engineer: Neil	
Date: Tuesday, February 11, 2020	Sheet: 91	of: 103	

+FBVDDQ [For VRAM]

BOM Option for EE:
N18E-G1 65 = PR9409 (stuff)
N18E-G0 Max Q = PR9499 (stuff)
N18P-G42-B = PR9423 / PR9402 / PR9414 / PQ9401 (stuff)
+ PR9409

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.25V	1.2V
PR9404	10KOhm	
PR9499	16.9KOhm	
PR9423	140KOhm	

FBVDDQ PR9499 Setting			
GA401IV	1.20V	15KOhm	1G021215214030
GA401U	1.25V	16.9KOhm	1G021216914030
GA401I	1.25V	16.9KOhm	1G021216914030
GA401IH	1.20V	16.9KOhm 140KOhm	1G021216914030 10102-00052000

N18E-G1_65 = 1.2V
N18E-G0 Max Q = 1.25V
N18P-G42-B = 1.25V
N18P-G61 = 1.2/1.25V

CHIP Cap (H=2.1)

Imax= 21A
IPeak = 24A
OCP= 100A

+FBVDDQ

PT940* 請放置 PU9401旁;並請放置Trace 上!

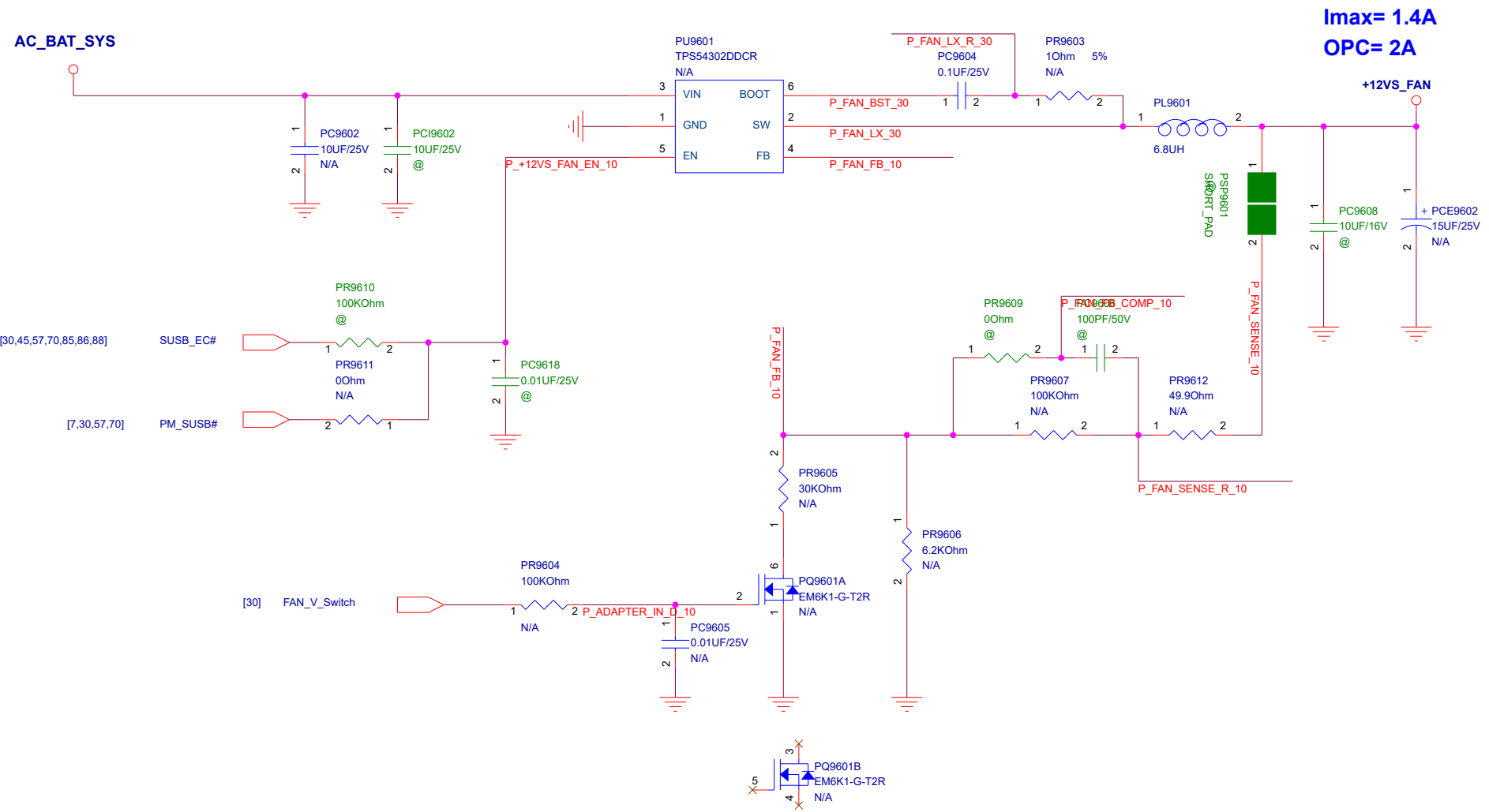
7.零件請放靠近GPU端

<Variant Name>			
Project Name: GA502IV			Rev: 81.0
Title : PW_+FBVDDQ			
Size: Custom	Dept.: NB Power Team	Engineer: CS Lin	
Date: Tuesday, February 11, 2020	Sheet: 94 of 104		

<Core Design>

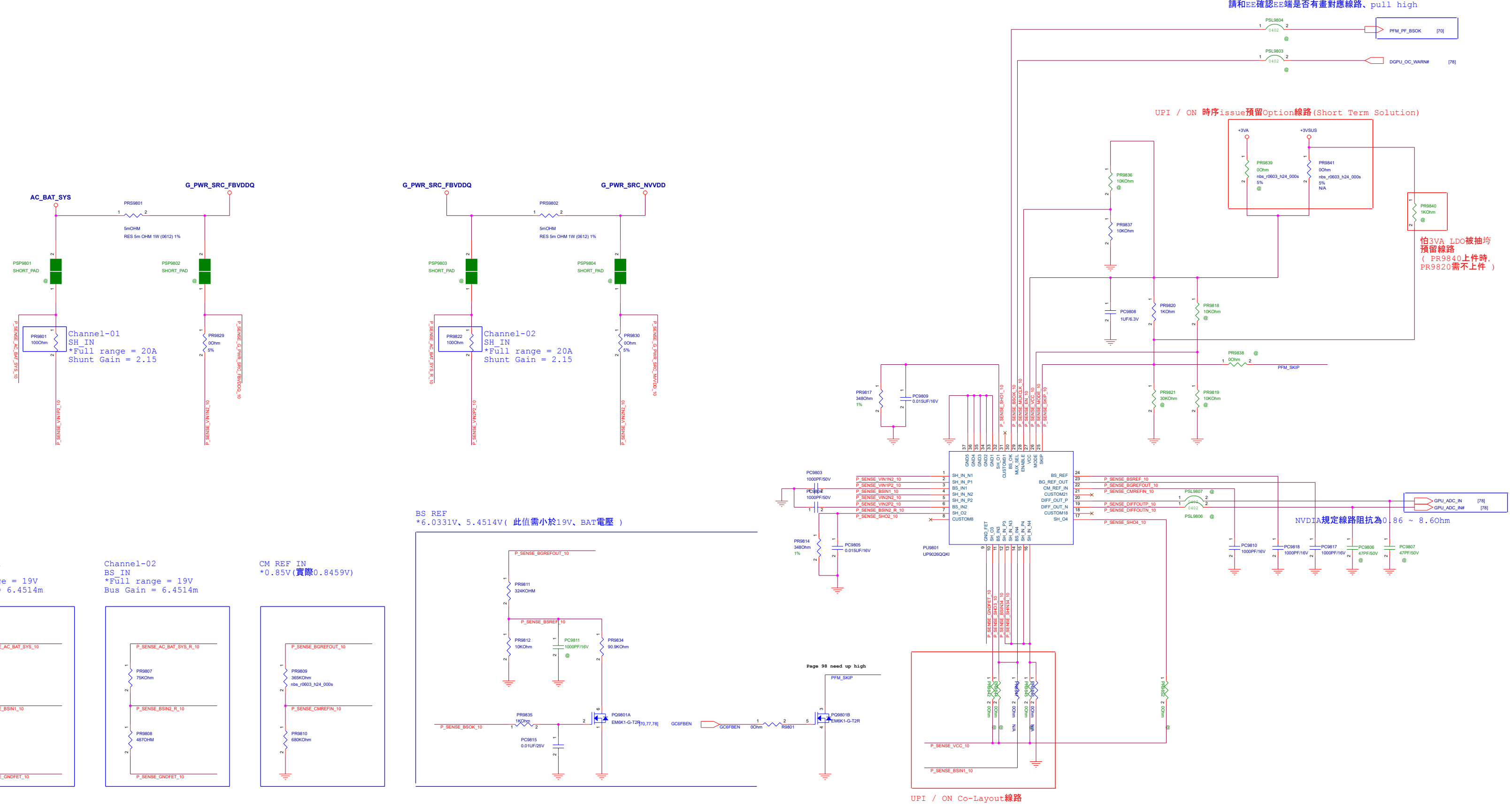
ASUSTeK COMPUTER	Title : OTH_for test only	
	Engineer: EE	
Size: A	Project Name: GA401	Rev: R1.2
Date: Tuesday, February 11, 2020	Sheet 95 of 104	

+12VS_FAN [For FAN]



<Variant Name>

Project Name: Project Name		Rev: R1.0
Title : PW_+12VS_FAN		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Tuesday, February 11, 2020	Sheet 96 of 104	



N18E

150W+

	UP9026PQKI(UPI)	NCP45491(ON)
PR9801	100Ω(10G212100014010)	
PR9817	127Ω (10G212127014010)	169Ω (10G212169014010)
PR9822	100Ω(10G212100014010)	
PR9814	127Ω (10G212127014010)	169Ω (10G212169014010)
PR9805	75kΩ(10G212750214010)	
PR9806	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9807	75kΩ(10G212750214010)	
PR9808	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9811	324kΩ (10G212324314010)	243kΩ (10G212243314010)
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

115W ~ 130W

	UP9026PQKI(UPI)	NCP45491(ON)
PR9817	143Ω (10G212143014010)	191Ω (10G212191014010)
PR9814	143Ω (10G212143014010)	191Ω (10G212191014010)

100W ~ 110W

	UP9026PQKI(UPI)	NCP45491(ON)
PR9817	165Ω (10G212165014010)	221Ω (10G212221014010)
PR9822		
PR9814	165Ω (10G212165014010)	221Ω (10G212221014010)

75W ~ 90W

	UP9026PQKI(UPI)	NCP45491(ON)
PR9817	215Ω (10102-00571000)	287Ω (10G212287014010)
PR9822		
PR9814	215Ω (10102-00571000)	287Ω (10G212287014010)

75W-

	UP9026PQKI(UPI)	NCP45491(ON)
PR9817	357Ω (10G212357014010)	475Ω (10G212475014010)
PR9822		
PR9814	357Ω (10G212357014010)	475Ω (10G212475014010)

N18P

75W-

	UP9026PQKI(UPI)	NCP45491(ON)
PR9801	100Ω(10G212100014010)	
PR9817	357Ω (10G212357014010)	475Ω (10G212475014010)
PR9822	100Ω(10G212100014010)	
PR9814	357Ω (10G212357014010)	475Ω (10G212475014010)
PR9805	75kΩ(10G212750214010)	
PR9806	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9807	75kΩ(10G212750214010)	
PR9808	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9811	324kΩ (10G212324314010)	243kΩ (10G212243314010)
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

150w+

	UP9026PQKI(UPI)	NCP45491(ON)
PR9801	200Ω(10G212200014010)	
PR9817	127Ω (10G212127014010)	
PR9822	200Ω(10G212200014010)	
PR9814	127Ω (10G212127014010)	
PR9805	33kΩ (10G212330214010)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G212330214010)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G212324314010)	
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

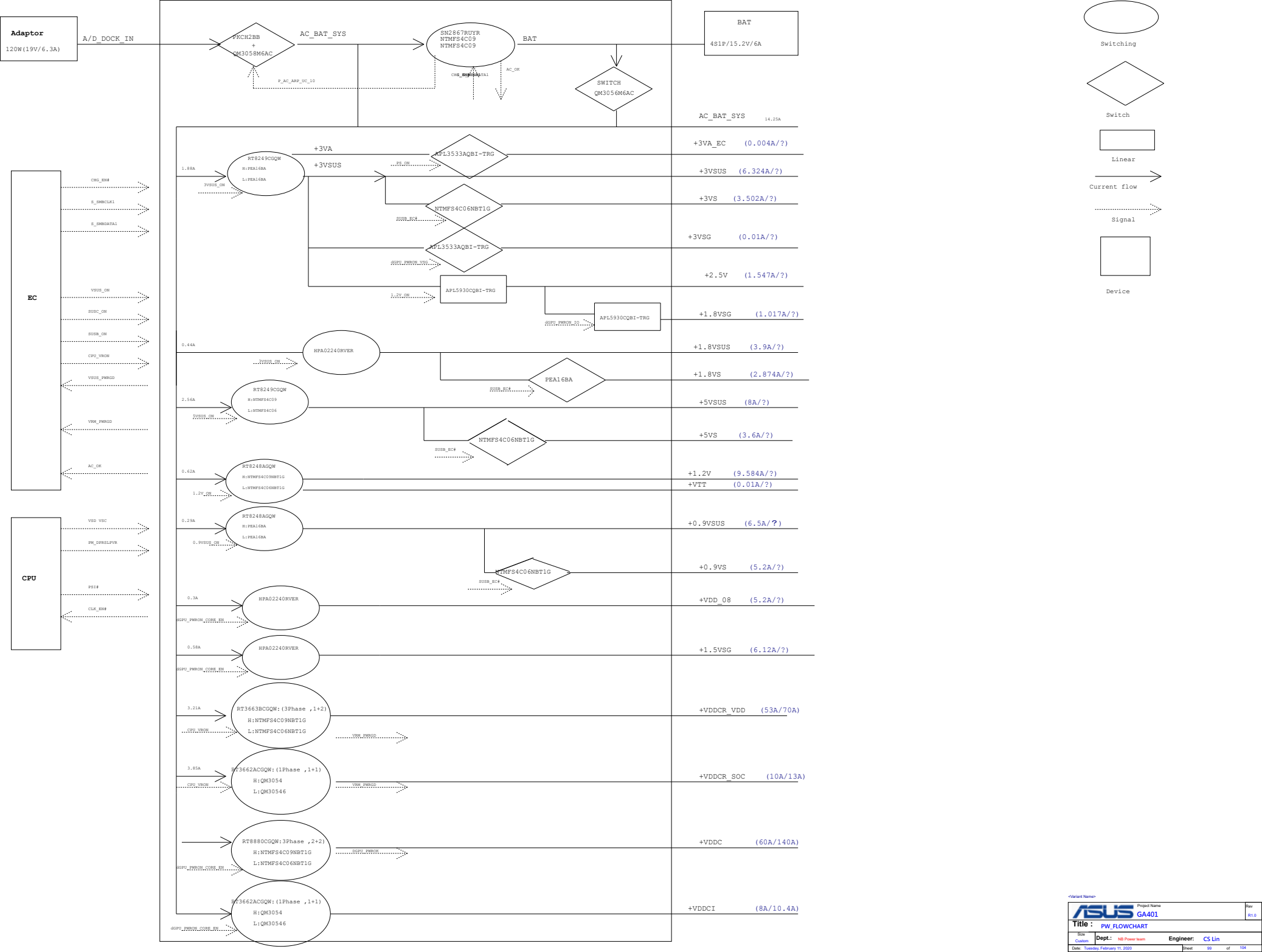
115W ~ 130W

	UP9026PQKI(UPI)	NCP45491(ON)
PR9801	200Ω(10G212200014010)	
PR9817	143Ω (10G212143014010)	
PR9822	200Ω(10G212200014010)	
PR9814	143Ω (10G212143014010)	
PR9805	33kΩ (10G212330214010)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G212330214010)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G212324314010)	
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

75W ~ 90W

	UP9026PQKI(UPI)	NCP45491(ON)
PR9801	200Ω(10G212200014010)	
PR9817	215Ω (10102-00571000)	
PR9822	200Ω(10G212200014010)	
PR9814	215Ω (10102-00571000)	
PR9805	33kΩ (10G212330214010)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G212330214010)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G212324314010)	
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

ASUS Project Name: GA401
Title: PW_IPC
Dept.: Power Team Engineer: Joe



<Variant Name>

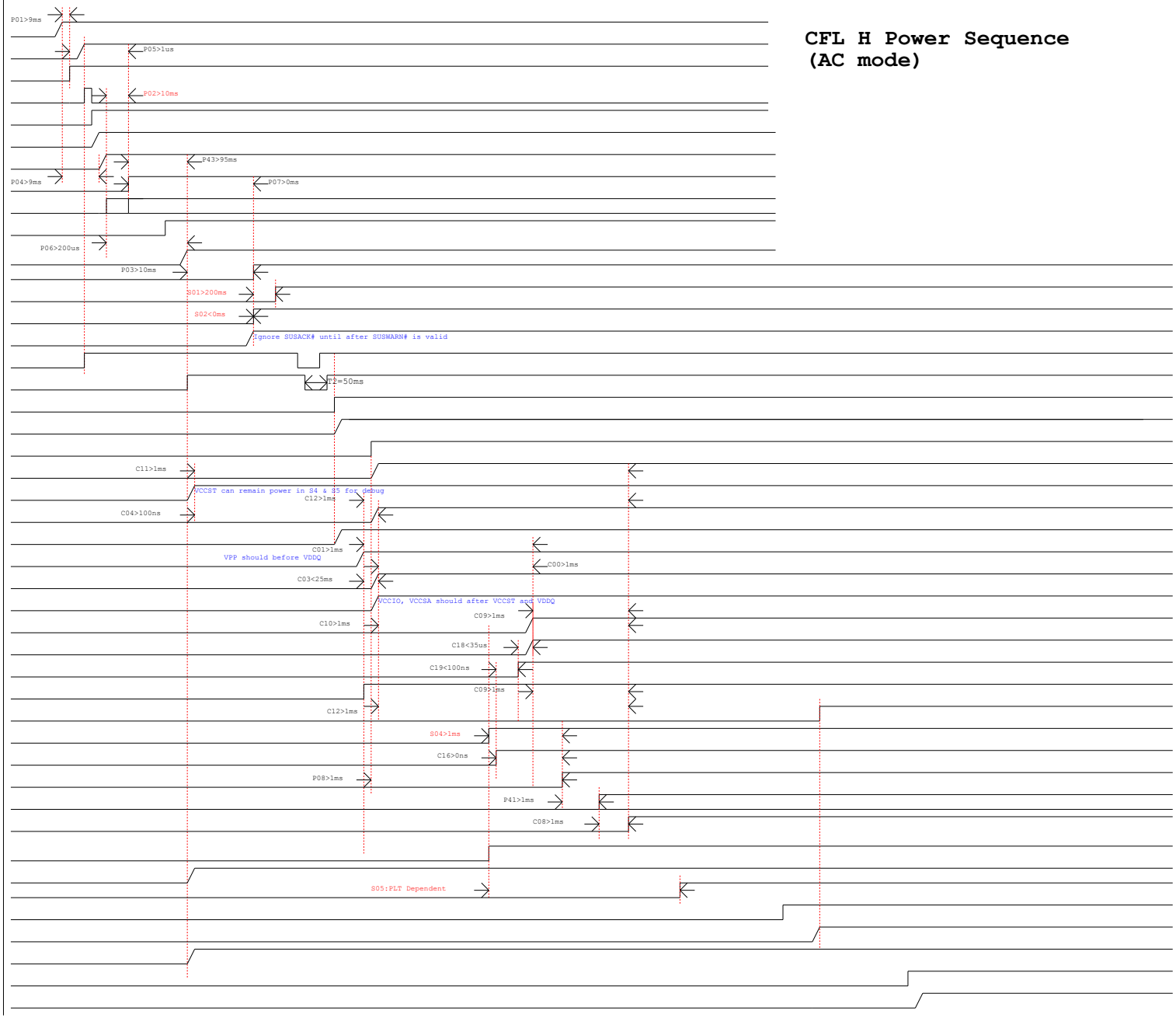
ASUS	Project Name: GA401	Rev: R1.0
Title : PW_FLOWCHART		
Size: Custom	Dept.: NB Power team	Engineer: CS Lin
Date: Tuesday, February 11, 2020	Sheet 99 of 104	

AC-IN Mode

CFL H Power Sequence (AC mode)

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(SUSB_EC#) +1.0V_VCCST, VCCPLL
(SUSB_EC#) +VCCIO, (+12VS) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



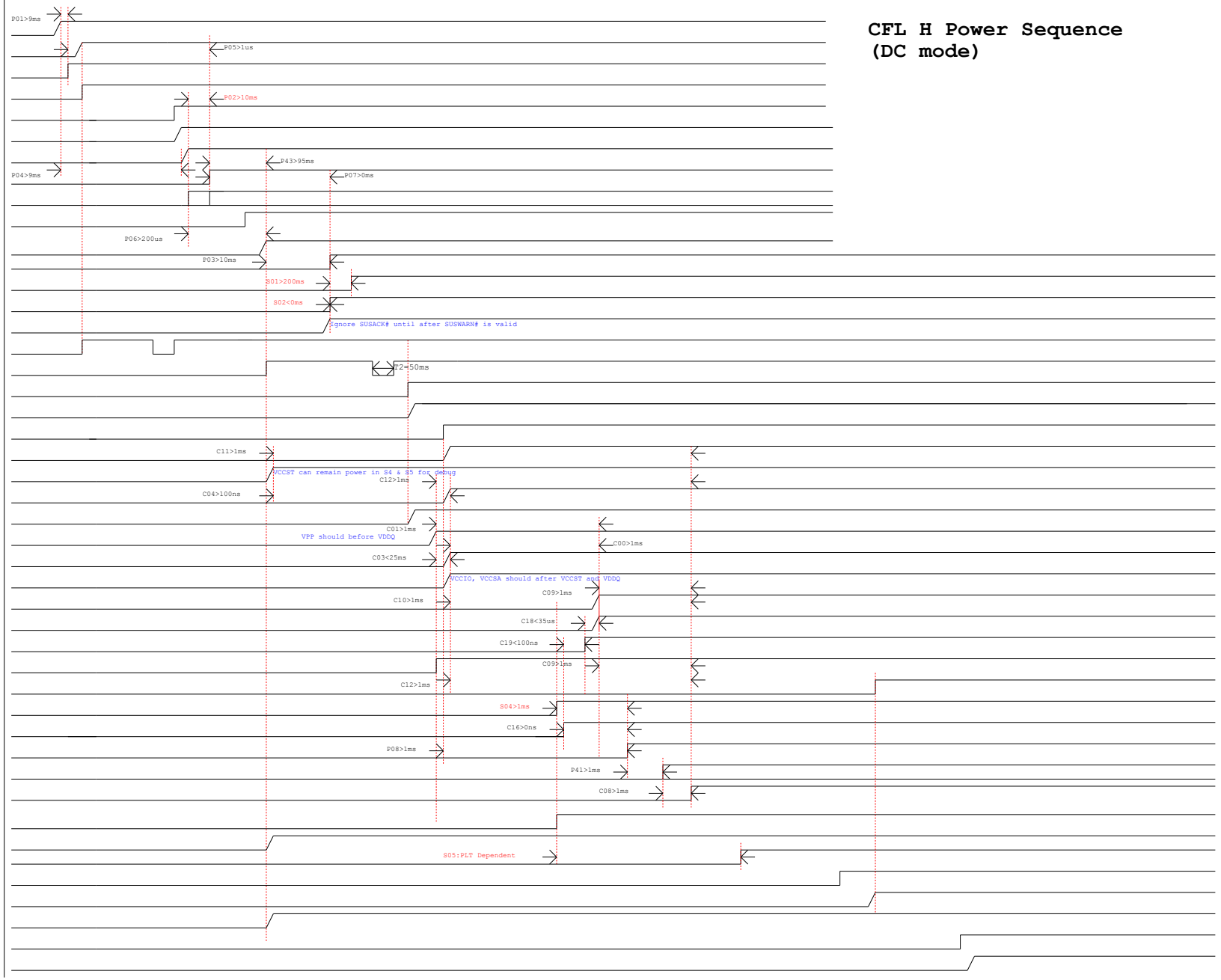
ASUS	Project Name: GA401		Rev: 1.0
Title : Power On Timing--AC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Tuesday, February 11, 2020	Sheet 100 of 104		

CFL H Power Sequence (DC mode)

DC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(VSUS_ON) +1.0V_VCCST,VCCPLL (VCCST_PWRGD)
(+VCCIO) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



ASUS	Project Name: GA401		Rev: 1.0
Title : Power On Timing--DC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: NB1 RD2 EE1	
Date: Tuesday, February 11, 2020	Sheet 101 of 104		

Rev	Date	Description
1.0	2017.03.03	P21 Remove CN
	2017.03.04	Q5602, Q5601 change for DXF Limitation
	2017.03.10	+1V9_MAIN, +3VS_NV Follow G753 Power sequence setting
	2017.03.11	R7821 Follow GL702 GPU Power seq
	2017.03.11	+PEX_VDD GPU Sequence update
	2017.03.14	PCE8104, PCE8107, PCE8106 update Cap for DXF Limit
	2017.03.14	GX501VIK Remove useless nut in P67
	2017.03.15	J5301 Connector list update
	2017.03.15	H6716, H6706, H6724, H6723 Screw Hole update
	2017.03.16	J5602 change LID SW for Angle Simulation
	2017.03.17	EMI Reserve C5606, C5607 Cap
	2017.03.17	RM3002, L4512, L4513, L4504, L4515, L4505 SWAP for Layout
1.1	2017.03.21	P30, P37, P39 AMP Change SNL04M25555
	2017.03.21	EMI Reserve P30 C77360 Cap and P69 Caps and Spring
	2017.03.23	AMP Change Remove P37 MUTE CONTROL schematic
	2017.03.23	AMP Change Reserve Q3701
	2017.03.27	P71 +PBVDDQ Discharge setting Follow G753 Power sequence setting
	2017.03.29	P12 Remove TBT Power Low Switch for Layout
1.2	2017.03.30	Change Cap C7105, C7101 for thermal request
	2017.03.30	Thermal Request for H6728
	2017.04.05	EMI Reserve Cap and Spring in P69
	2017.04.06	Reserve C2601 for +VCCPGPP_EF Ripple
	2017.04.07	25.00MHZ Cap C1126, C1124 change for Vendor Suggest
	2017.04.07	27MHz Cap C7811, C7801 change for Vendor Suggest
2.0	2017.04.11	P48 Reserve 0 ohm for SDA and SCL
	2017.04.17	P71 Add Caps for NVVDD Ripple
	2017.04.18	Q5704 Chnage MOS for DXF Limitation
	2017.04.20	P71 Add Caps for NVVDD Ripple
	2017.04.21	P67 Screw Hole H6705 update
	2017.04.21	P71 Add Caps for NVVDD Ripple C71119~C71122
	2017.04.25	P71 C7122, C7123, C7127, C7135, C7143, C7144, C7156, C7164, C7166,, C7186, C7187 change to 100UF
	2017.04.25	P70 C7007, C7002 change to 4.7UF
	2017.04.25	P70 C7020, C7024 change to 22UF
	2017.05.02	EMI Reserve C6948, C6949, C6950, C6951, C6952, C6953, C6954 and remove U6913
	2017.05.02	H6711, H6712 change screw hole type fot EMI Solution
	2017.05.03	Remove J4502 Pin 36 GND fot Factory Issue
	2017.05.05	P88, P58 Remove VCCST_PWRGD signal
	2017.05.05	P79, P45 Remove eDP Lan2 and Lan3 Signal
	2017.08.10	P31 R3121,R3122 change to unmount

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

ASUSTeK COMPUTER

Title : Revision History

Engineer: EE

Size: D | Project Name: GA401 | Rev: 1.0

Date: Tuesday, February 11, 2020 | Sheet 102 of 106

GM531GX R1.0 SKU Table

			CPU	Power	DIMM	VRAM			
Option	PCB	SKU							
60NB0H10-MB1030	R1.0	GM531GX SKU1	/I7-7700HQ	/230W	TBD	VBG_Micron			
60NB0H10-MB2000	R1.0	GM531GX SKU2	/I5-7300HQ	/230W	TBD	VBG_Samsung			

ASUSTeK COMPUTER	Title :	GM531GX SKU Table R1.0		
	Engineer:	EE		
Size: C	Project Name: GA401			Rev: 1.0
Date: Tuesday, February 13, 2018	Sheet	103	of	104

9. Card Reader: AU6435--02G630002400 (Page42)

10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)

1. P.01-30 reference FX505DY, P.31-104 reference GX502_(WW39_20180927C)
2. Net connection_(WW39_20180928A)
20181004
P.03
P.07
P.30 Copy FX505DY P.30
P.32 Modify Reset circuit
P.34 Modify LAN connector
P.35 Modify N-KEY IT8291E to IT8299E
P.36 線路
P.37 Modiffy Headpohne, Mic, ESS
P.39 Remove Mute control
P.40 Modify circuit
P.41 Modify circuit & 螺孔, 0 ohm先keep
P.45 Add Mic and HDR circuit
P.48 Keep SL4802
P.49 Modify circuit
P.50

ASUS	Title : GM531GX_SKU Table_R1.0		
ASUSTeK COMPUTER	Engineer: EE		
Size: C	Project Name: GA401		Rev: 1.0
Date: Tuesday, February 11, 2020	Sheet 104 of 104		

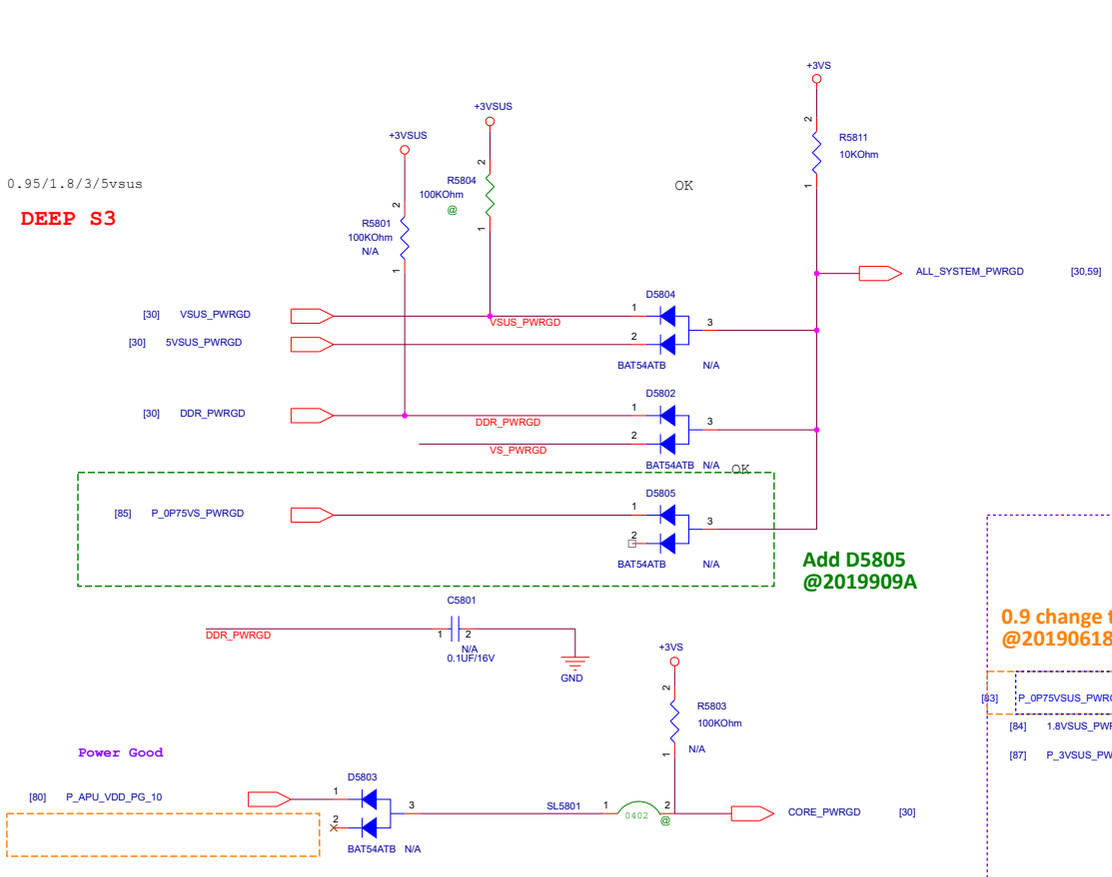
9. Card Reader: AU6435--02G630002400 (Page42)

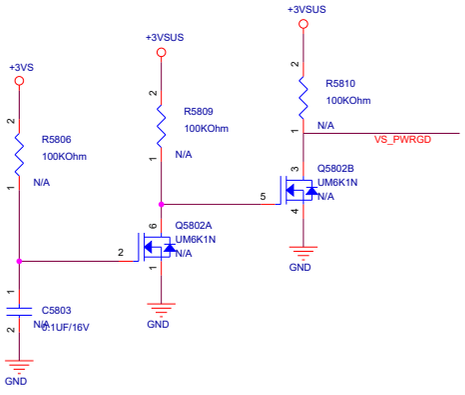
10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

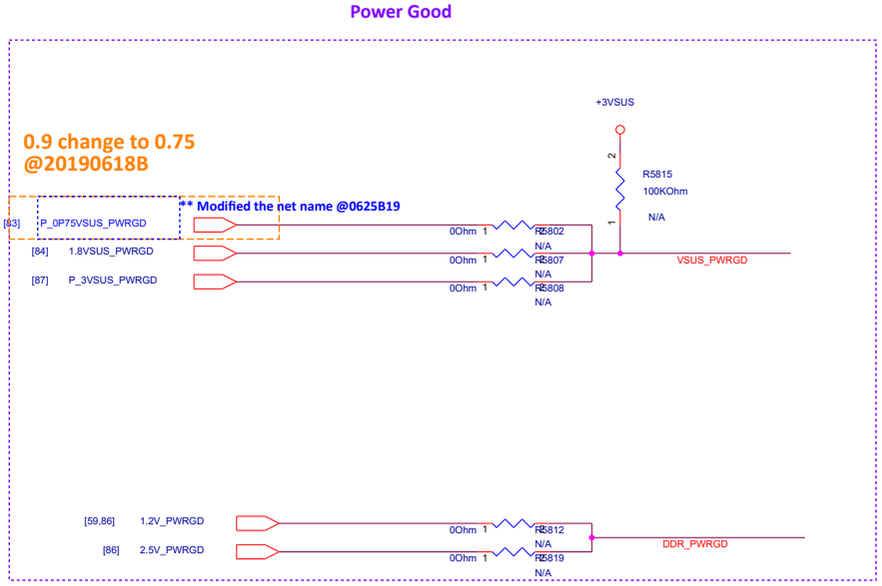
11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)

POWER GOOD DETECTER







Remove AMD GPU PWRGD
@20181009K

Project Name: GA401		Rev: R1.0
Title : POWER GOOD DETECTER		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: RD2 EE3
Date: Tuesday, February 11, 2020	Sheet 58 of 104	

EMI1 SPRING (4.7H) 13060-00570000*1

EMI2 SPRING (2.6H) *3
13NB0I50M01011

U6906 U6910 change to 13040-00440000(SMT Gasket H=2.5mm)
@20190213A

Modify @20181122A(EMI req.)

D5906 GASKET_1P 13040-00440000 /EMI — GND

D5910 GASKET_1P 13040-00440000 /EMI — GND

D5907 GASKET_1P 13040-00440000 /EMI — GND

D5908 GASKET_1P 13040-00440000 /EMI — GND

D5909 GASKET_1P 13040-00440000 /EMI — GND

EMI request @20181026A

AC_BAT_SYS

C5910 0.1UF/25V
C5911 0.1UF/25V
C5906 0.1UF/25V
C5934 0.1UF/25V
C5941 0.1UF/25V
C5944 0.1UF/25V
GND

+3VA

D5901 AZ5325-01F @ — GND

D5902 AZ5325-01F — GND

D5903 AZ5325-01F — GND

P_SMB0_CLK [28,30,60,89,90]
P_SMB0_DAT [28,30,60,89,90]

將U6904, U6908(改裸銅), U6905(改裸銅) 移除
@20181122C

2017/04/05 EMI

AC_BAT_SYS

C5945 0.1UF/25V
C5946 0.1UF/25V
C5947 0.1UF/25V
GND

AC_BAT_SYS

C5942 0.1UF/25V @
C5943 0.1UF/25V @
C5904 0.1UF/25V
C5905 0.1UF/25V
C5907 0.1UF/25V
C5908 0.1UF/25V
C5909 0.1UF/25V
GND

4/2 for EMI

G_PWR_SRC_NVVDD

C5901 0.1UF/25V
GND

G_PWR_SRC_NVVDD

C5902 2.2UF/25V
C5903 2.2UF/25V
GND

TOP side

2016/07/27 EMI

+NVVDD

C5922 10PF/50V @
C5923 10PF/50V @
C5924 10PF/50V @
GND

AC_BAT_SYS

C5925 0.1UF/25V
C5926 0.1UF/25V
C5927 0.1UF/25V @
C5928 0.1UF/25V
C5929 0.1UF/25V
C5930 0.1UF/25V
C5932 0.1UF/25V
C5933 0.1UF/25V
C5935 0.1UF/25V
C5936 0.1UF/25V @
C5937 0.1UF/25V
GND

[58,86] 1.2V_PWRGD

C5931 100PF/50V
GND

GX501VI 1.1H

[30,58] ALL_SYSTEM_PWRGD

C5938 100PF/50V @
GND

Delete@ 20181015K

[7,32,41,53,70] BUF_PLT_RST#

C5940 100PF/50V
GND

2016/11/09 EMI

+5VS_PWR

C5954 10PF/50V @
GND

<Core Design> 2017.05.02 EMI Reserve

ASUSTeK COMPUTER

Title : OTH_EMI

Engineer: EE

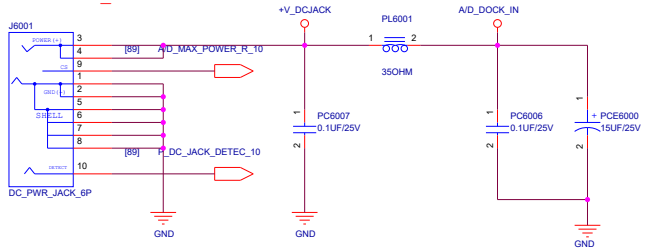
Size	Project Name	Rev
B	GA401	1.0

Date: Tuesday, February 11, 2020 Sheet 59 of 104

DC-IN Connector

DC Jack使用請詢用River_Hsu

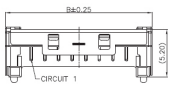
New 6 Phi 4 Pin DC_Jack

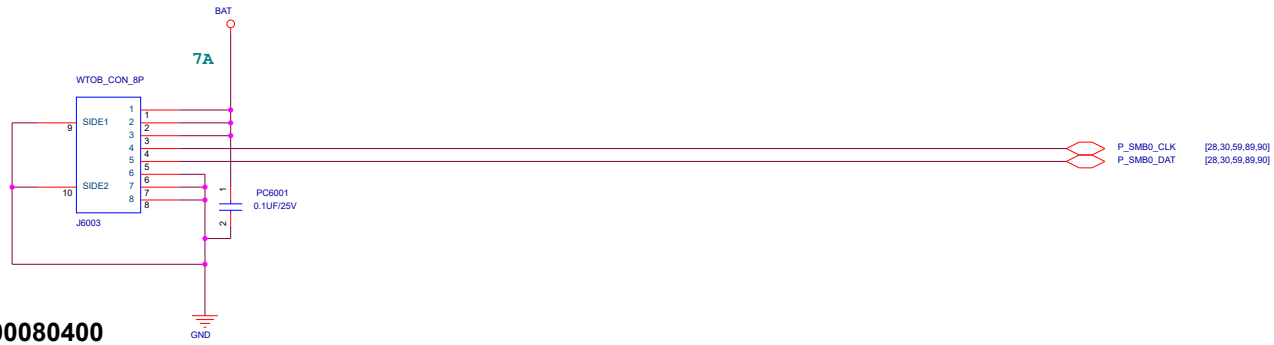


CHIP Cap (H=2.1)

	3.4CH	1.55CH
J6001	12033-00020200	12033-00020300

Battery Connector





12017-00080400

Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

ASUS	Project Name: GA502IV		Rev: R1.0
Title : DC & BAT IN			
Size: A3	Dept.: NB_Power team	Engineer: CS Lin	
Date: Tuesday, February 11, 2020	Sheet 60 of 104		

<Core Design>

Title : BT_Bluetooth

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
C	**GA401**	1.0

Date:	Tuesday, February 11, 2020	Sheet	61	of	104

<Variant Name>

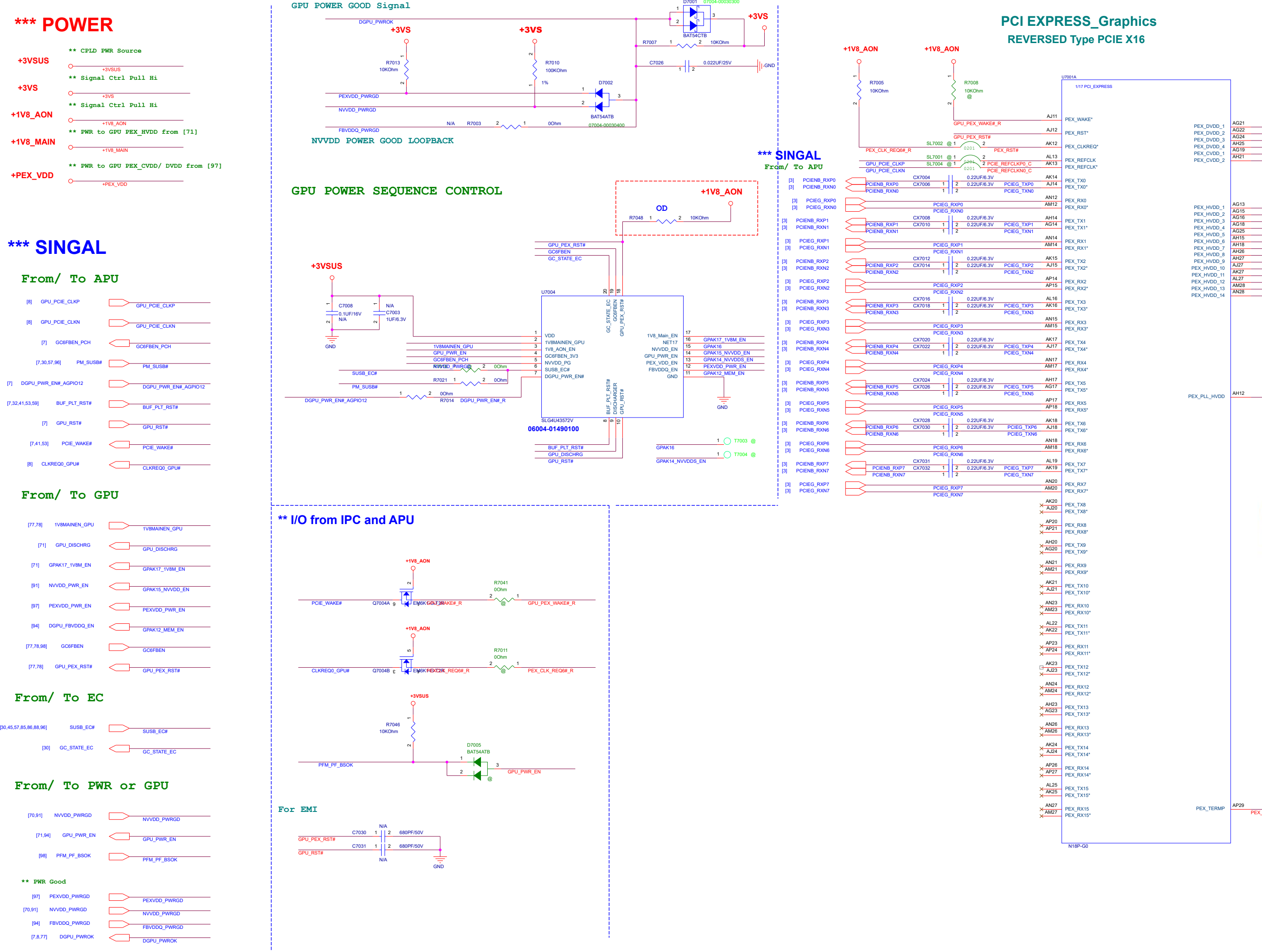
Title : I/O board Audio/USB

ASUSTeK COMPUTER

Engineer: Wendell_Lo

Size	Project Name	Rev
C	GA401	1.0

Date:	Tuesday, February 11, 2020	Sheet	62	of	104



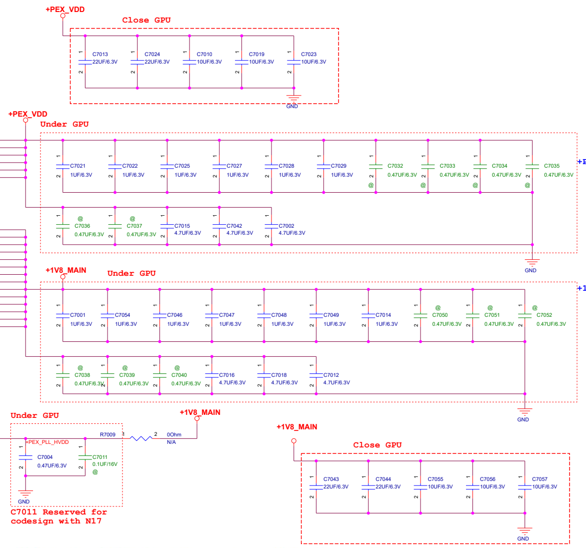


Table 5.11 GB4D-128 Package: Power Rail Filtering (Continued)

Rail (GPU Ball)	Balls	Voltage	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	14 x 0.47uF (0201W X6S) 3 x 4.7uF (0603 X6S) - - - - - - - - - - - - - - - - - Alternate solution: 7 x 1uF (0402 or 0201W, X6S) [3] 3 x 4.7uF (0603 X6S)	3 x 10uF (0805 X6S) 2 x 22uF (0805 X6S)
PEX_DVDD	6	1.0V	12 x 0.47uF (0201W X6S) 3 x 4.7uF (0603 X6S) - - - - - - - - - - - - - - - - - Alternate solution: 6 x 1uF (0402 or 0201W, X6S) [3] 3 x 4.7uF (0603 X6S)	3 x 10uF (0805 X6S) 2 x 22uF (0805 X6S)

ASUS
Project Name: G512LI
Rev: 2.0
Title : GPU_PCIE I/F
Size: Custom
Dept.: ASUSTeK COMPUTER
Engineer: Gaming RD
Date: Tuesday, February 11, 2020
Sheet 70 of 103

*** POWER

*** SINGAL

MEMORY: GPU FB Partition A

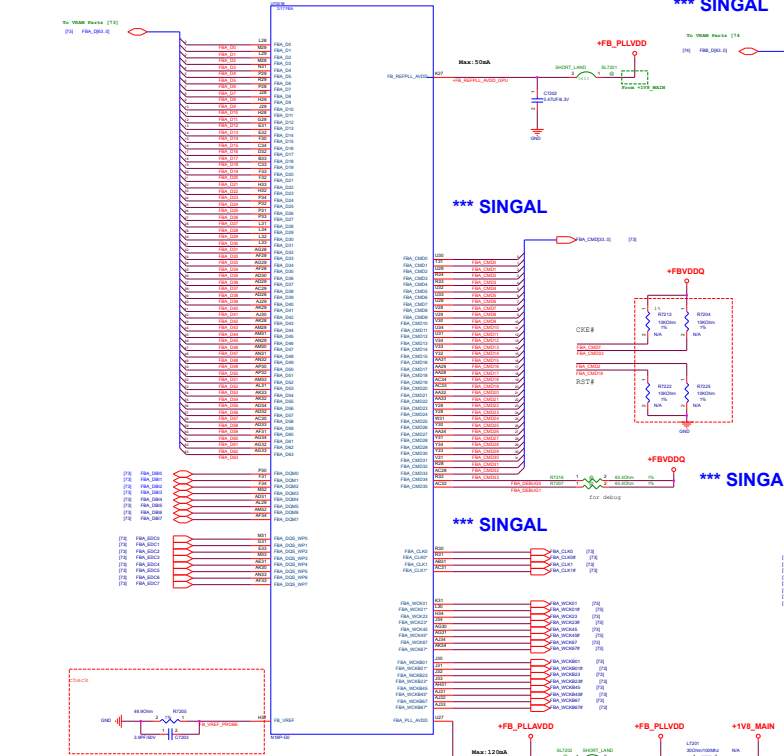
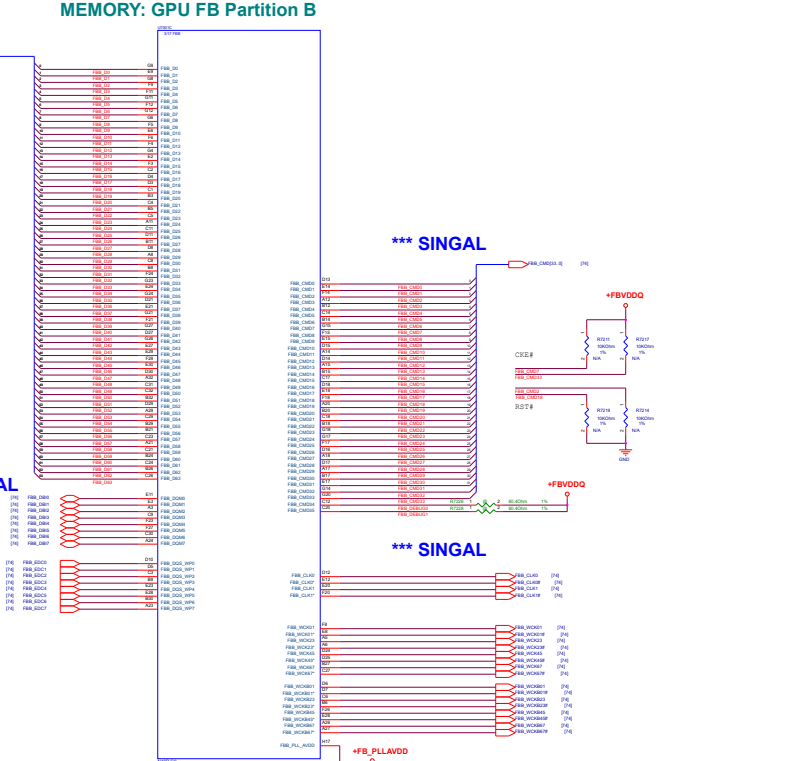


Table 15. N17-GB4C-128 and N18/GB4D-128 FB BOM Differences

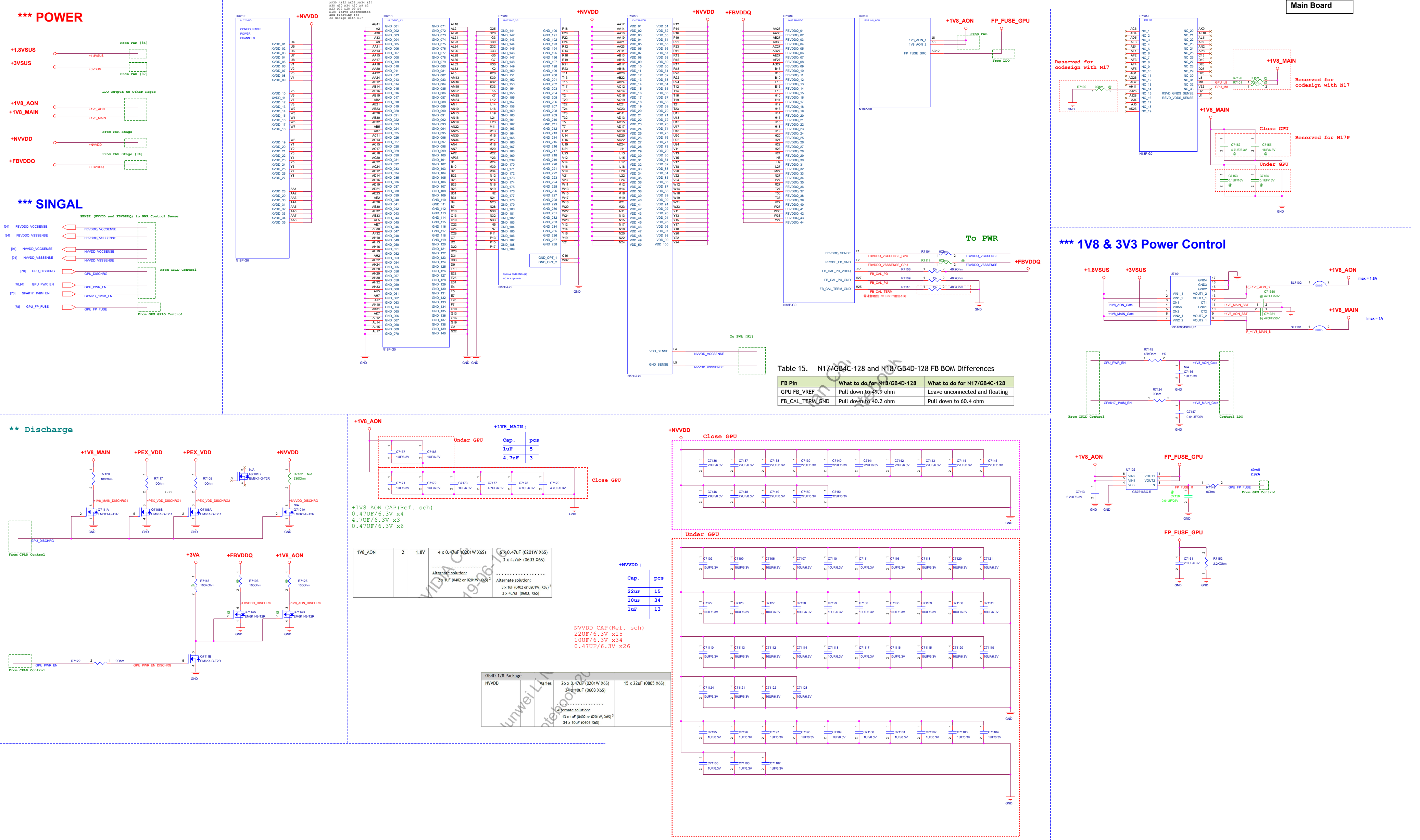
FB Pin	What to do for N18/GB4D-128	What to do for N17/GB4C-128
GPU FB_VREF	Pull down to 49.9 ohm	Leave unconnected and floating
FB_CAL_TERM_GND	Pull down to 40.2 ohm	Pull down to 60.4 ohm

*** SINGAL

MEMORY: GPU FB Partition B



ASUS	Project Name: G512LI		Rev: 30.0
Title : GPU_FRAME BUFFER			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, February 11, 2020	Sheet 73 of 103		



+1V8_AON CAP(Ref. sch)
0.47UF/6.3V x4
4.7UF/6.3V x3
0.47UF/6.3V x6

NVVDD CAP(Ref. sch)
22UF/6.3V x15
10UF/6.3V x34
0.47UF/6.3V x26

+1V8_MAIN : Cap.	pcs
1uF	5
4.7uF	3

+NVVDD : Cap.	pcs
22uF	15
10uF	34
1uF	13

1V8_AON	2	1.8V	4 x 0.47uF (0201W X6S) Alternate solution: 2 x 1uF (0402 or 0201W, X6S) [3]	6 x 0.47uF (0201W X6S) 3 x 4.7uF (0603 X6S) Alternate solution: 3 x 1uF (0402 or 0201W, X6S) [3] 3 x 4.7uF (0603, X6S)

GB4D-128 Package				
NVVDD		Varies	26 x 0.47uF (0201W X6S) 34 x 10uF (0603 X6S) Alternate solution: 13 x 1uF (0402 or 0201W, X6S) [3] 34 x 10uF (0603 X6S)	15 x 22uF (0805 X6S)

Table 15. N17/GB4C-128 and N18/GB4D-128 FB BOM Differences

FB Pin	What to do for N18/GB4D-128	What to do for N17/GB4C-128
GPU FB_VREF	Pull down to 49.9 ohm	Leave unconnected and floating
FB_CAL_TERM_GND	Pull down to 40.2 ohm	Pull down to 60.4 ohm

*** POWER

MEM_VPP

MEM_VPP
From +1VS_AON
[17]

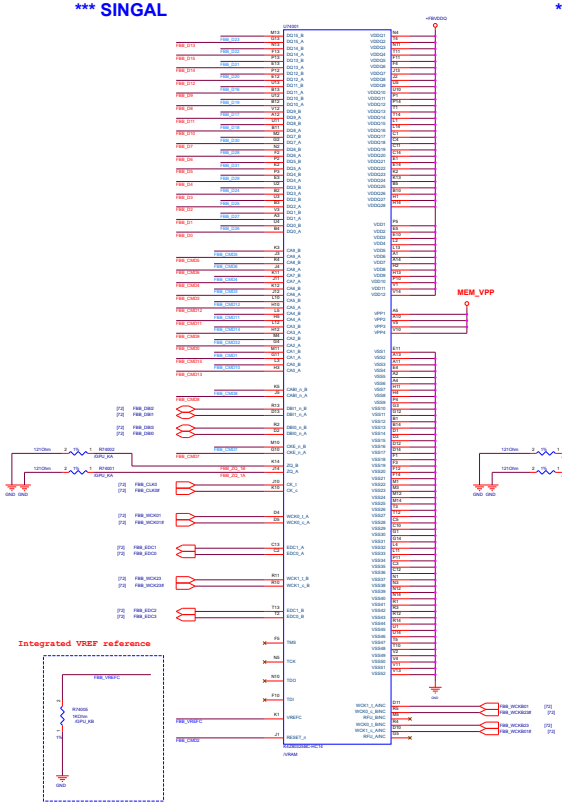
[72] FBB_DQ[31..0]
[72] FBB_CMD[33..0]

40 OHm_NET
FBB Partition 31..0

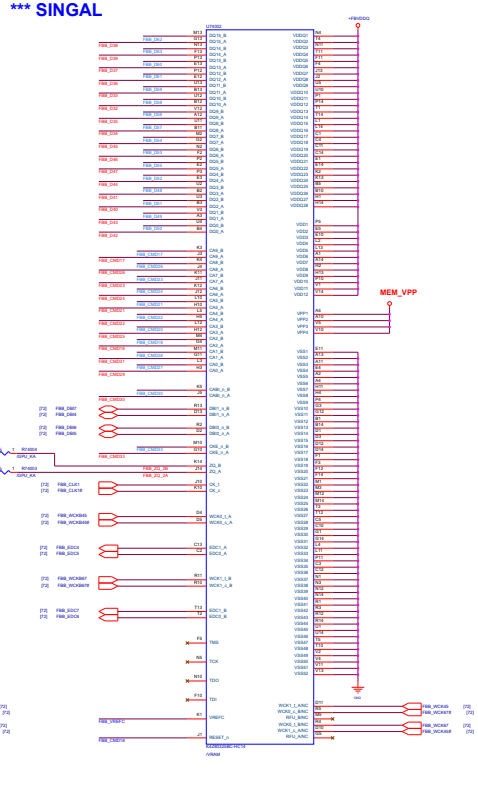
[72] FBB_DQ[63..32]

40 OHm_NET
FBB Partition 64..32

*** SINGAL



*** SINGAL



ASUS	Project Name: G512LI		Rev: R1.0
Title : VRAM_Channel_A			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, February 11, 2020	Sheet 72 of 100		

<Variant Name>

Title: <Title>		
Size: Custom	Document Number: 5G512LI	Rev: R1.0
Date: Tuesday, February 11, 2020	Sheet 72 of 100	

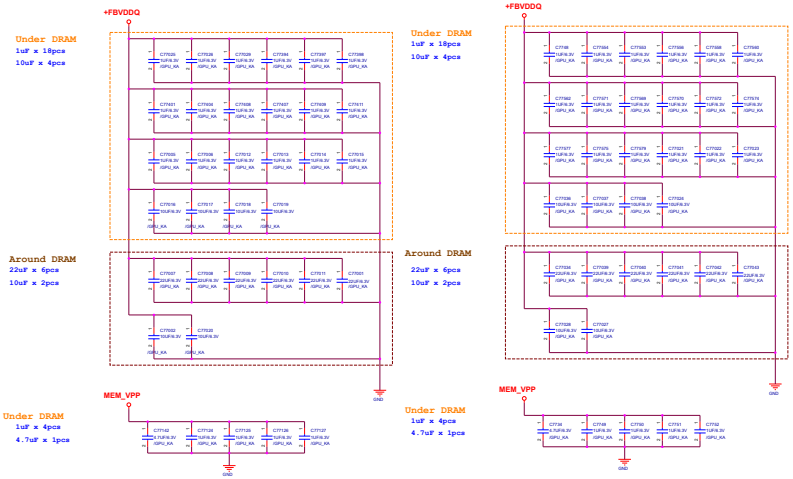
*** POWER

+FBVDDQ

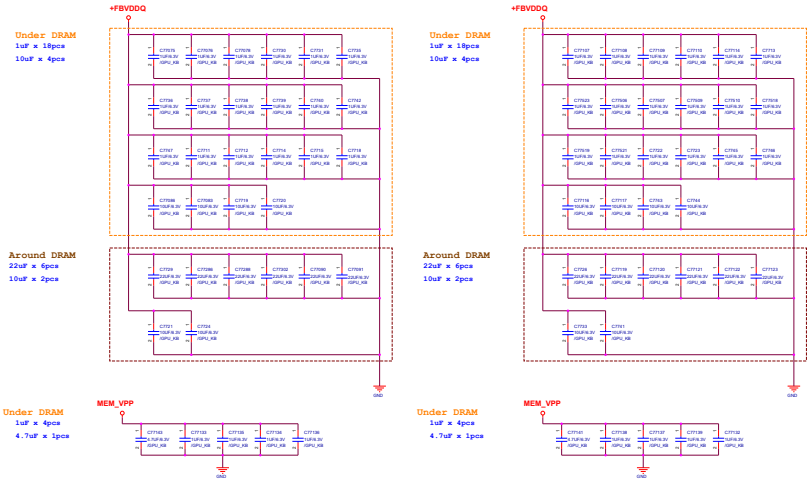
+1V8_AON

FBVDDQ/VPP (VRAM)

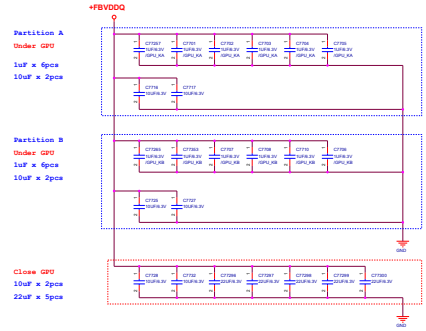
Channel A



Channel B



FBVDDQ (GPU)



FBVDDQ GPU side (Ref sch)
A ch:
0.47uF x12
10uF x2
B ch:
0.47uF x12
10uF x2
Near GPU
10uF x2
22uF x5

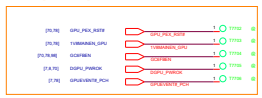
FBVDDQ VRAM side (Ref sch) per VRAM
Close VRAM:
0.47uF x36
10uF x4
0.47uF x8
Around DRAM
22uF x6
10uF x2

FBVDDQ (GPU side)[1]	1.35V 1.5V	24 x 0.47uF (0201W X6S) 4 x 10uF (0603 X6S) . . . . . . Alternate solution: 12 x 1uF (0402 or 0201W, X6S)[3] 4 x 10uF (0603 X6S)	2 x 10uF (0603 X6S)[2] 5 x 22uF (0603 X6S)

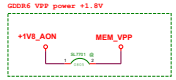
Table 8.12 DRAM-Side Decoupling

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type, [Size NOTE 1]	Quantity	Placement
VDD/VDDQ Rail			
0.47 uF NOTE 2	X6S [0201W]	36	Under or very close to DRAM
10 uF	X6S [0603]	4	
10 uF	X6S [0603]	2	Around DRAM
22 uF	X6S [0603]	6	
VPP Rail			
0.47 uF NOTE 3	X6S [0201W]	4	Under or very close to DRAM
4.7 uF	X6S [0603]	1	

For power sequence measurement



GDDR6 VPP power +1.8V

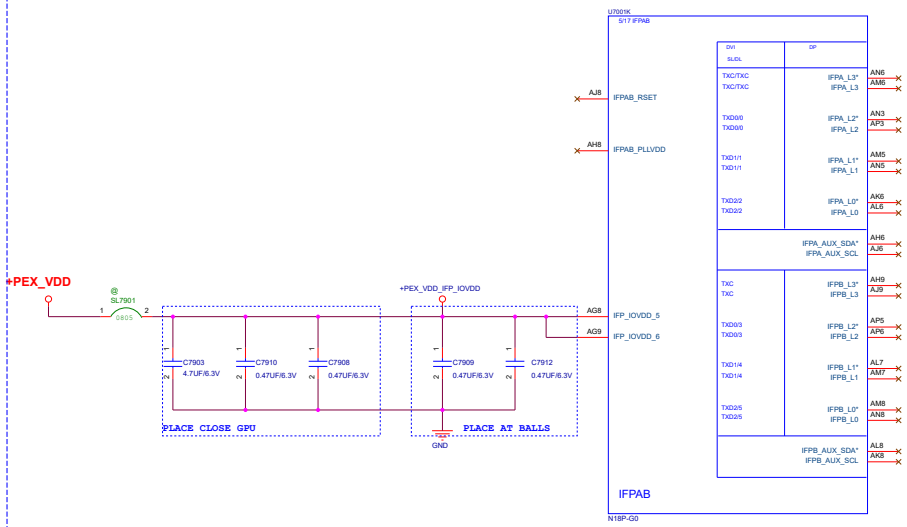


ASUS	Project Name: G512LI	Rev: X1.0
Title: VRM		
Size: A0	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Tuesday, February 11, 2020	Sheet: 27 of 100	

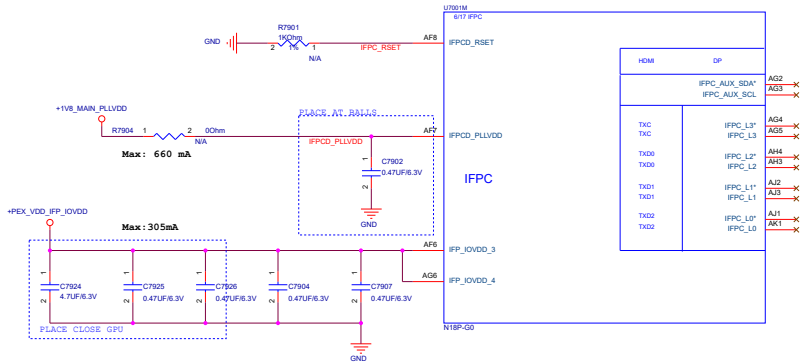
*** POWER

+PEX_VDD

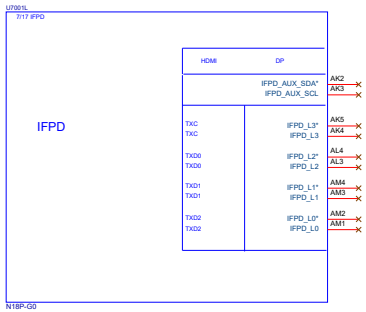
*** SINGAL



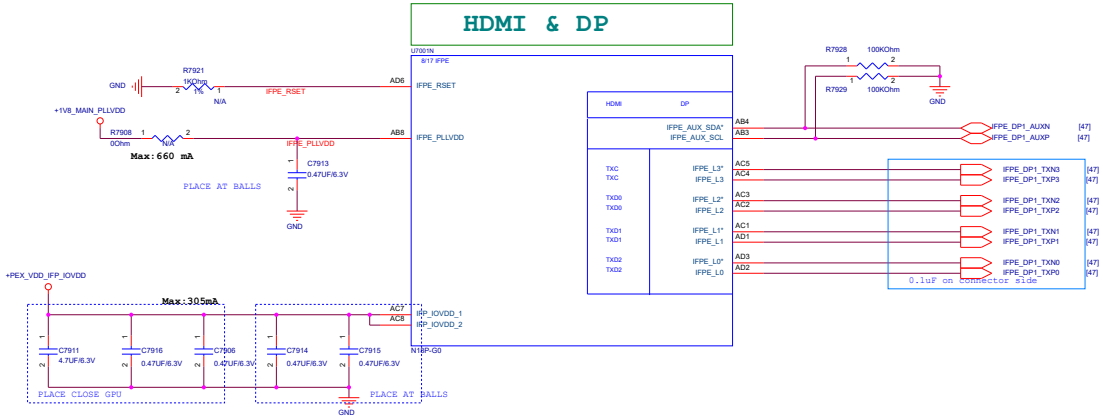
DP(Type-C)



EDP(4Lane Panel)



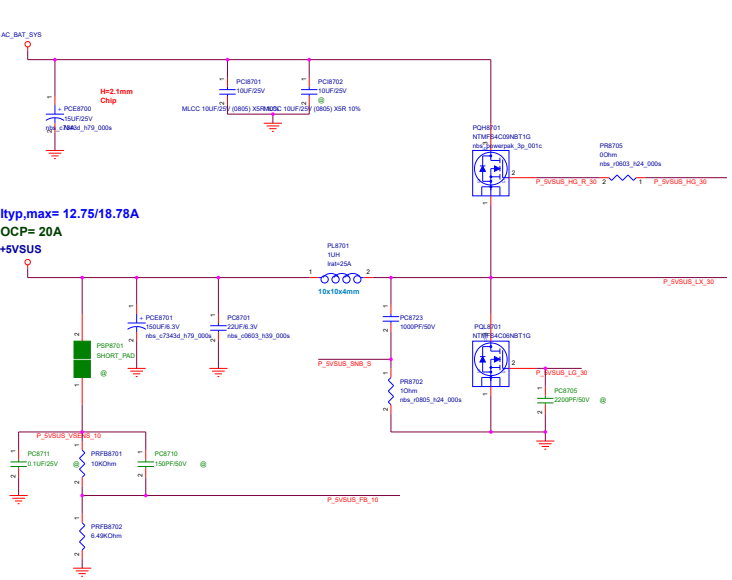
HDMI & DP

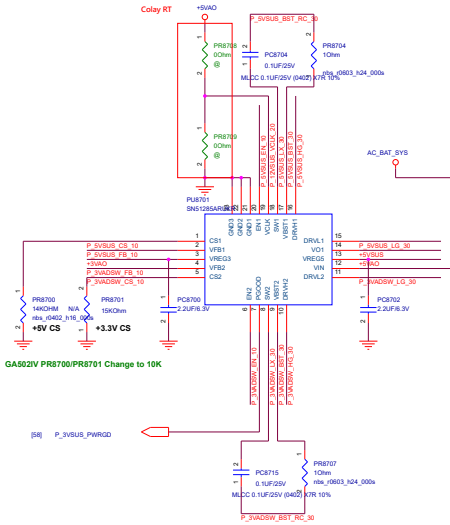


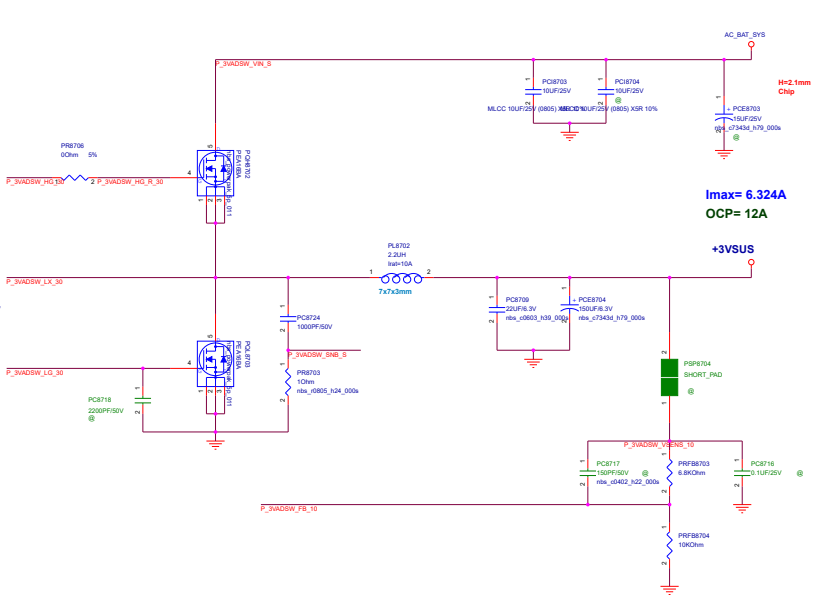
IFPAB_PLLVDD IFPCD_PLLVDD IFPE_PLLVDD	1 1 1	1.8V	3 x 0.47uF (0201W X6S, one per ball) --- Alternate solution: 3 x 1uF (0402 or 0201W, X6S, one per ball)	1 x 4.7uF (0603 X6S) 1 x 22uF (0805 X6S) 1 x 30Ω bead (0603 max ESR 0.01 Ω)
IFP_IOVDD	6	1.0V	6 x 0.47uF (0201W X6S) --- Alternate solution: 6 x 1uF (0402 or 0201W, X6S)	6 x 0.47uF (0201W X6S) 3 x 4.7uF (0603 X6S) --- Alternate solution: 3 x 1uF (0402 or 0201W, X6S) 3 x 4.7uF (0603, X6S)

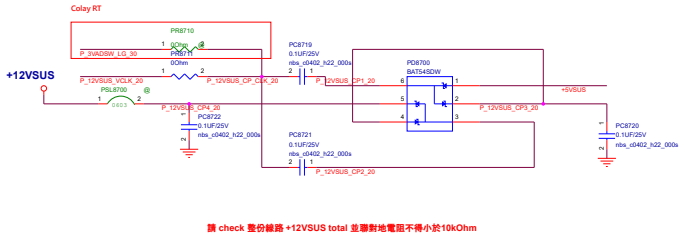
ASUS	Project Name: G512LI		Rev: 2.0
Title : GPU_DP/EDP/HDMI			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Tuesday, February 11, 2020	Sheet 79 of 103		

+3VA_DSW / +5VSUS [System Power]

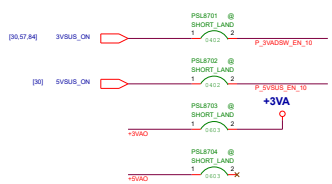








請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

PT870* 請放置 PU8700旁;並請放置Trace 上!

<Variant Name>

ASUS	Project Name: Coffelake-H	Rev: R1.0
Title : PW_+3VA_DSW/+5VSUS		
Size: A2	Dept.: NB Power team	Engineer: Joe
Date: Tuesday, February 11, 2020	Sheet 87 of 104	

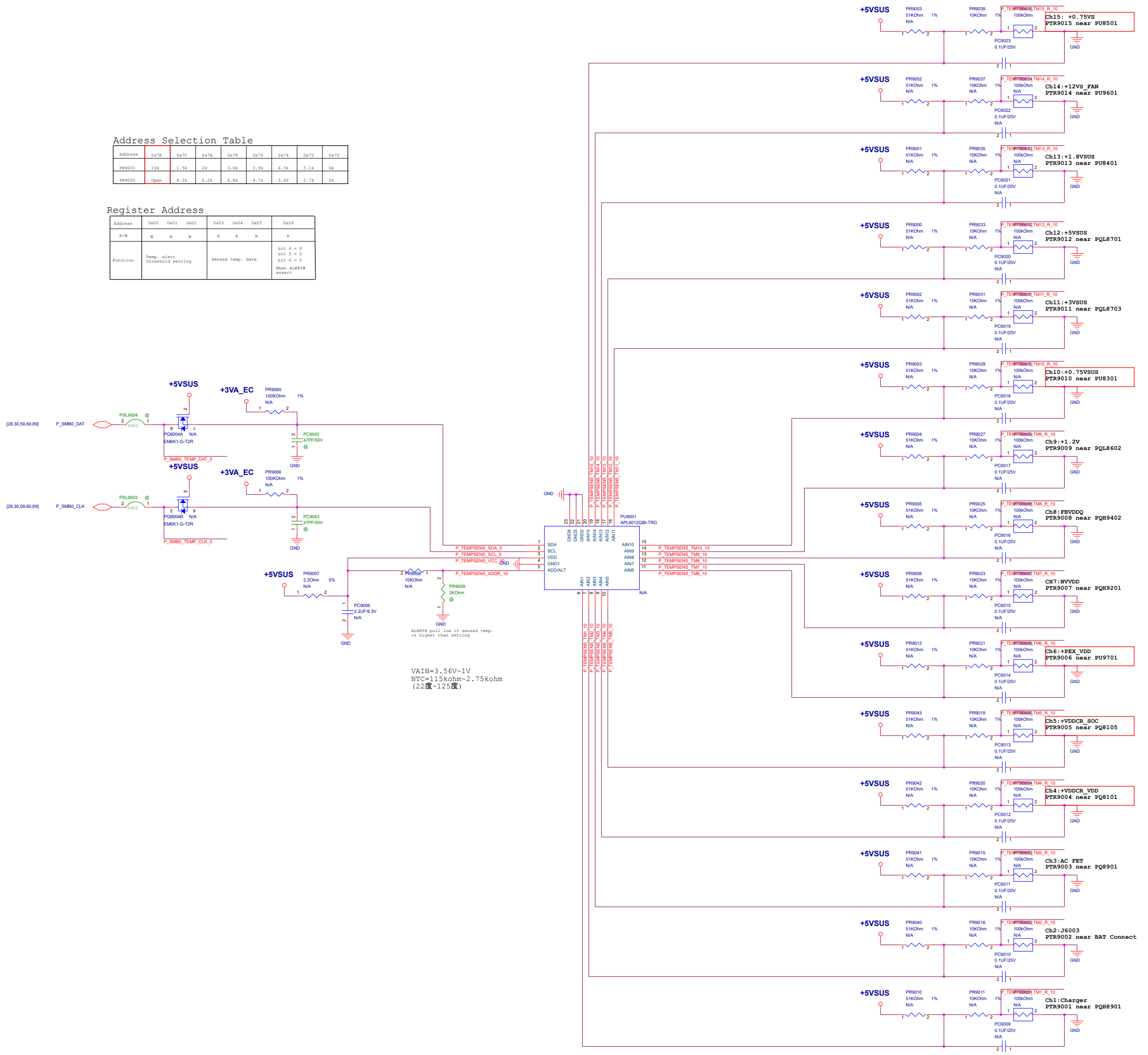
P90_PROTECTION

Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

Address	0x00 0x01 0x02	0x03 0x04 0x05	0x06
R/W	W W W	R R R	R
Function	Temp. alert threshold setting	Sensed temp. data	bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert



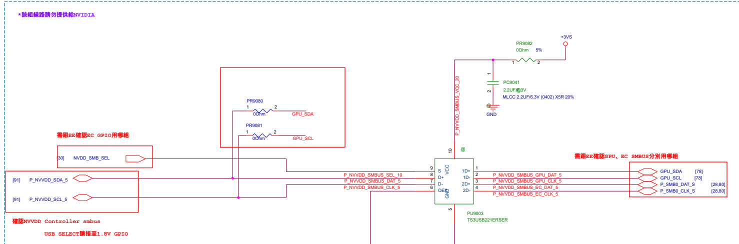
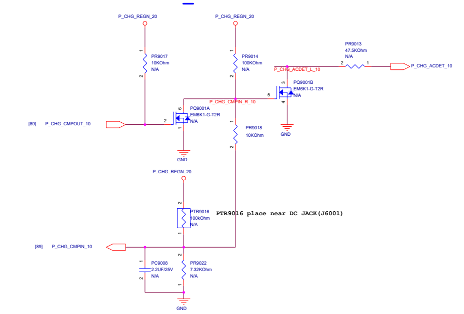


Table 2. TRUTH TABLE

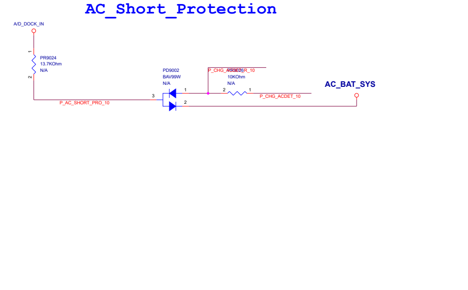
S	OE	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

單獨下地

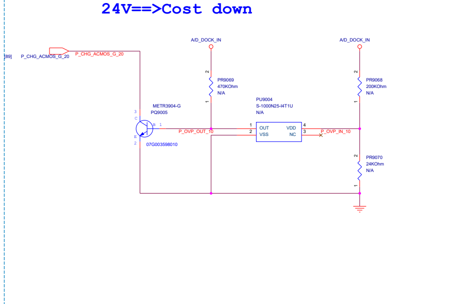
DC JACK_Protection



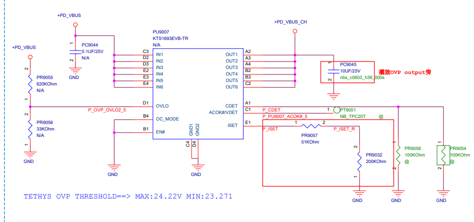
AC_Short_Protection



OVP Protection circuit 24V==>Cost down



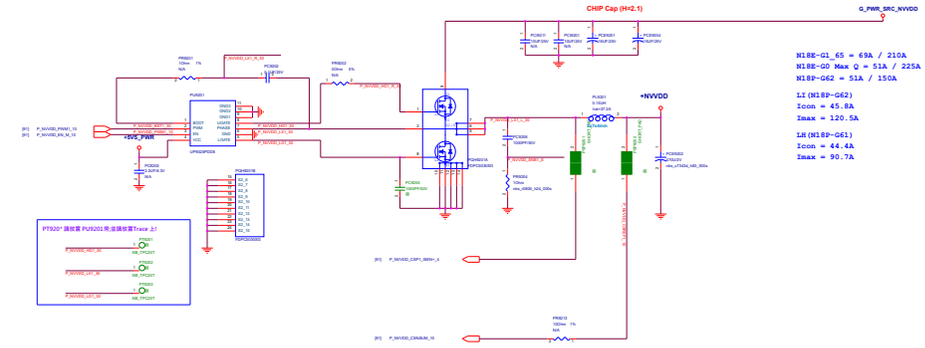
OVP for type C input (Slave Charger)



<Variant Name>

Project Name: GA502IV			Rev: R1.0
Title : PW_PROTECTION			
Size: A1	Dept.: NB Power Team	Engineer: CS Lin	
Date: Tuesday, February 11, 2020		Sheet 90 of 104	

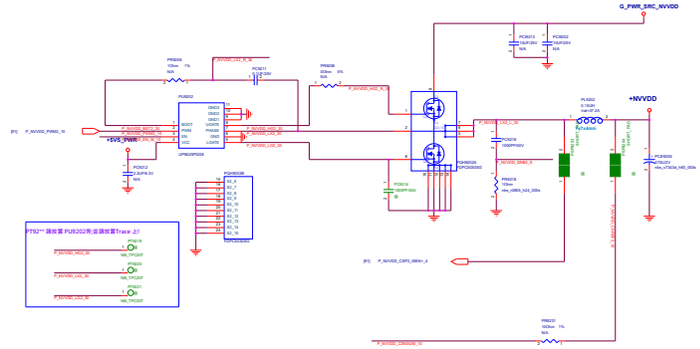
+NVVDD [For DGPU]

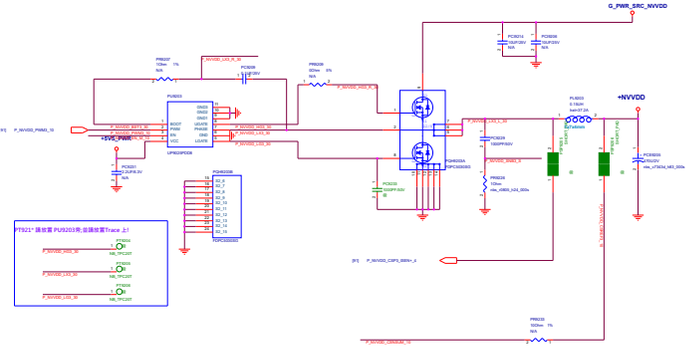


N18E-G1_65 = 69A / 210A
N18E-G0 Max Q = 51A / 225A
N18P-G62 = 51A / 150A

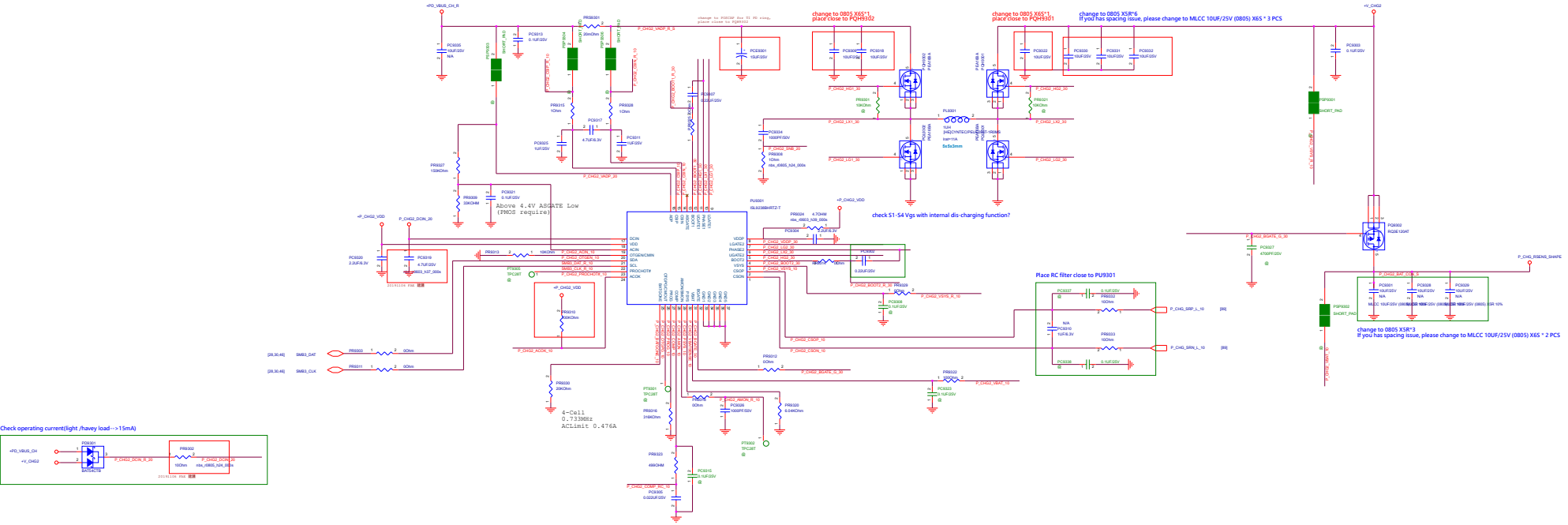
LI(N18P-G62)
Icon = 45.8A
Imax = 120.5A

LH(N18P-G61)
Icon = 44.4A
Imax = 90.7A





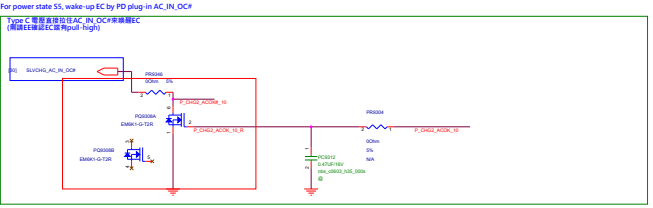
Charger ISL9238 (NVDC)

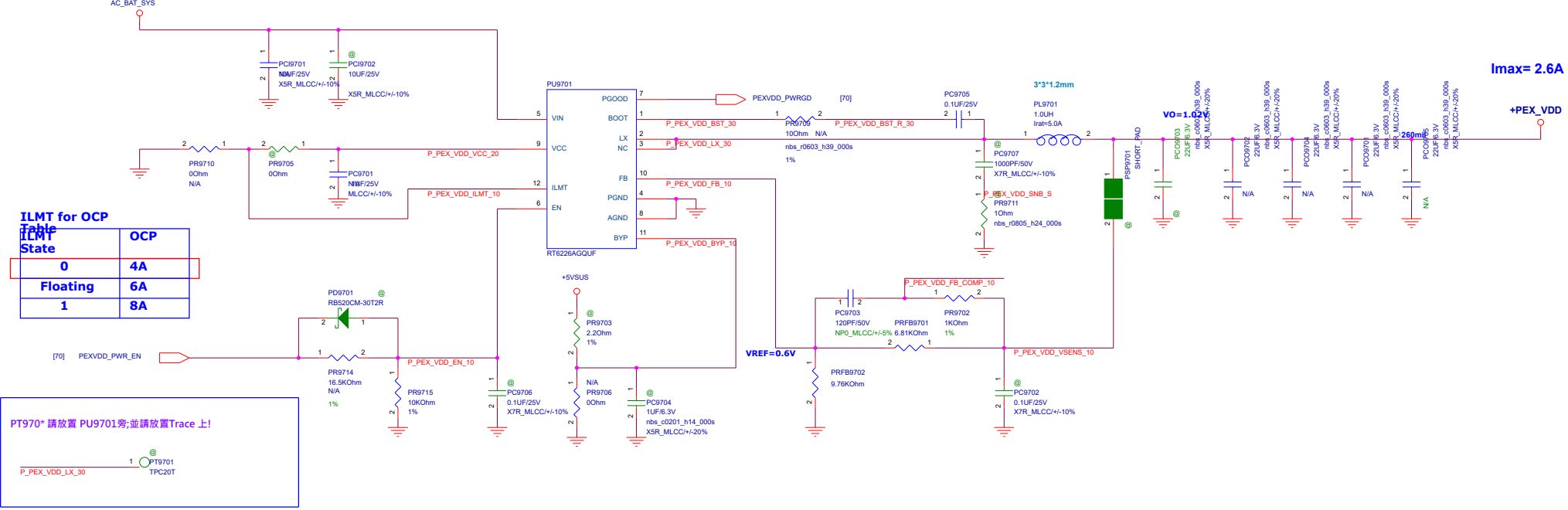


Check operating current(light /havey load-->15mA)

For power state S5, wake-up EC by PD plug-in AC_IN_OC#

Type C電壓直接拉住AC_IN_OC#來喚醒EC
(前提EC腳是EC採用pull -high)





ILMT for OCP

Table

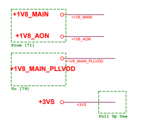
ILMT State	OCP
0	4A
Floating	6A
1	8A

PT970* 請放置 PU9701旁;並請放置Trace 上!

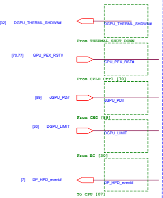
<Variant Name>

ASUS	Project Name: GA502IV	Rev: R1.0
Title : PW_+PEX_VDD		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Tuesday, February 11, 2020	Sheet 97 of 104	

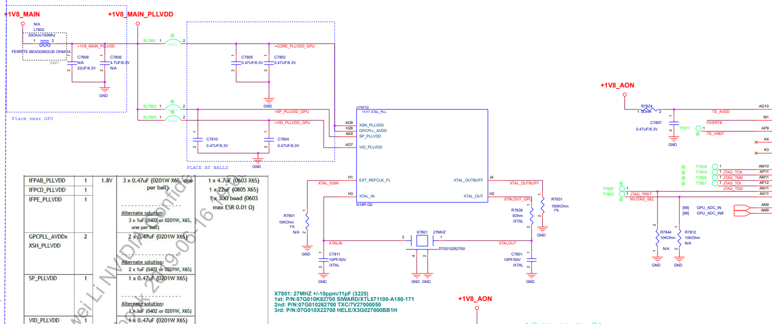
*** POWER



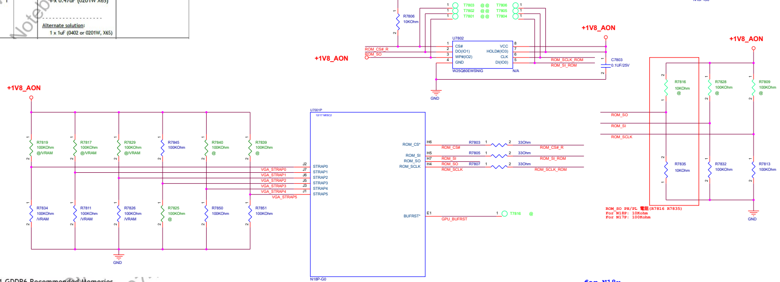
*** SINGAL



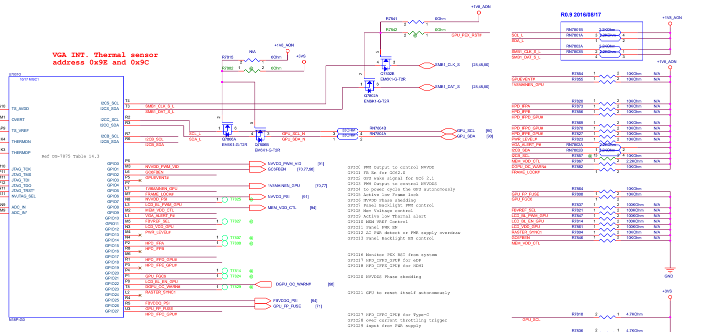
IFPAB_PLLVDD	1	1.8V	3 x 0.47uF (0201W X6S, one per ball) Alternate solution: 3 x 1uF (0402 or 0201W, X6S, one per ball)	1 x 4.7uF (0603 X6S) 1 x 22uF (0805 X6S) 1 x 30Ω bead (0603 max ESR 0.01 Ω)
IFPCD_PLLVDD	1			
IFPE_PLLVDD	1			
GPCPLL_AVDDx XSN_PLLVDD	2		2 x 0.47uF (0201W X6S) Alternate solution: 2 x 1uF (0402 or 0201W, X6S)	
SP_PLLVDD	1		1 x 0.47uF (0201W X6S) Alternate solution: 1 x 1uF (0402 or 0201W, X6S)	
VID_PLLVDD	1		1 x 0.47uF (0201W X6S) Alternate solution: 1 x 1uF (0402 or 0201W, X6S)	



STRAP PIN



VGA INT. Thermal sensor address 0x9E and 0x9C



Level Option	Physical Configuration	
	Pull-Up to 1.8V via resistor (see Note 1). (Notebook designs also see Note 2.)	Pull-Down to GND via resistor Note 1
1.8V ("HIGH") Level	Populate	No Stuff
0.9V ("MIDDLE") Level	Populate	Populate
GND ("LOW") Level	No Stuff	Populate

Note 1: Resistor should be 100K Ohms. 5% tolerance is acceptable.
Note 2: Notebook graphics circuit designs should pull up to the 1V8_AON rail rather than to 1V8_MAIN.

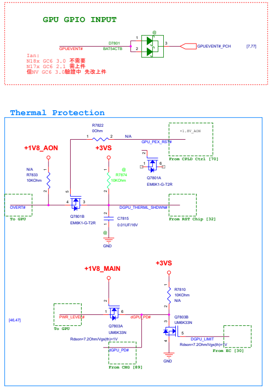
Assorted Configuration Straps

1. SMB_ALT_ADDR Enable: "0" signal GPU setting I2CS address 0x9E, "1" Dual GPU setting I2CS address add 0x9C, used when a second GPU
2. DEVID_SEL: G-sync function→"0"normal GPU ID, "1" support G-sync GPU ID
3. PCIE_CFG: PCIE Swing→"0" PCIE Swing default, "1" PCEI swing reduce
4. VGA_DEVICE: Graphics circuit→"0" MS-Hybrid, "1" Discrete

Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

GPU GPIO INPUT

Thermal Protection



Level shift

HPD Invert

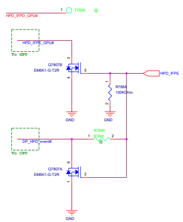


Table 5. N18P-G62/G61 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V and 1.25V[3]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	Yes, TBD[2, 4]	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	Yes, TBD[2, 5]	Full	Production candidate

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

for N18x

Total Display Links (HDMI, DP or DVI)					See This Row of Table 5.4
	Total Enabled for Audio (HDMI, DP or DVI)				
		Is eDP Supported on:			
		IFPA or IFPB?	IFPC or IFPD?	IFPE or IFPF?	
4	4	--	--	--	15
4	3	yes	--	--	14
4	3	--	yes	--	13
4	3	--	--	yes	11
3	3	--	--	--	14
3	2	yes	--	--	12
3	2	--	yes	--	12
3	2	--	--	yes	10
2	2	--	--	--	12
2	1	yes	--	--	8
2	1	--	yes	--	8
2	1	--	--	yes	8
1	1	--	--	--	8
1	0	yes	--	--	0
1	0	--	yes	--	0
1	0	--	--	yes	0

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

for N17x

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0

Total Display Links (HDMI, DP or DVI)					See This Row of Table 5.4
	Total Enabled for Audio (HDMI, DP or DVI)				
		Is eDP Supported on:			
		IFPA or IFPB?	IFPC or IFPD?	IFPE or IFPF?	
4	4	--	--	--	15
4	3	yes	--	--	14
4	3	--	yes	--	13
4	3	--	--	yes	11
3	3	--	--	--	14
3	2	yes	--	--	12
3	2	--	yes	--	12
3	2	--	--	yes	10
2	2	--	--	--	12
2	1	yes	--	--	8
2	1	--	yes	--	8
2	1	--	--	yes	8
1	1	--	--	--	8
1	0	yes	--	--	0
1	0	--	yes	--	0
1	0	--	--	yes	0

Table 15.1 GPIO Descriptions for GB4D-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	No PU/PD
GPIO1	GC6: GC6_FB_EN	I/O	FB Enable for GC6 2.1	10 kΩ pull-down
GPIO2	GC6:GPU_EVENT	I/O	GPU wake signal for GC6 2.1	10 kΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	UNUSED	O		
GPIO4	GC6: 1V8_MAIN_EN	I	GPU power sequencing for GC6 2.1	10 kΩ pull-up to 1V8_AON
GPIO5	FRAME_LOCK*	O	Active low Frame Lock	10 kΩ pull-up to 1V8_AON
GPIO6	NVVDD_PSI*		Phase Shedding (see Section 15.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	LCD Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT*	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	10K Pull Up
GPIO13	UNUSED			
GPIO14	HPD_IFPA*	I	Hot Plug Detect for IFPA	10K Pull Up to 1V8_AON
GPIO15	HPD_IFPB*	I	Hot Plug	10K Pull Up to 1V8_AON
GPIO16	UNUSED			
GPIO17	HPD_IFPD*	I	Hot Plug Detect for IFPD	10K Pull Up to 1V8_AON
GPIO18	HPD_IFPE*	I	Hot Plug Detect for IFPE	10K Pull Up to 1V8_AON
GPIO19	UNUSED	O		
GPIO20	GC6:NB_GC6	I/O		10K Pull Down
GPIO21	LCD_BLEN	O	LCD Panel Backlight enable	100K Pull Down
GPIO22	INA_HT* / ADC_MUX_SEL			2.2K Pull Up See circuit
GPIO23	Reserved			100K Pull Down
GPIO24	UNUSED	I		
GPIO25	FBVDD_PSI*			PU/PD with series resistor depending on PSI topology
GPIO26	FP_FUSE			10K Pull Down
GPIO27	HPD_IFPC*	I	Hot plug detect for IFPC	10K Pull Up to 1V8_AON

Project Name: G512LI
Title: GPU_CLOCK/STRAP/GPIO
Dept.: ASUSTeK COMPUTER Engineer: Gaming RD
Date: Tuesday, February 11, 2020