COMPAL CONFIDENTIAL

MODEL NAME : ***PAL61***

PCB NO : ***LA-6561P (DA80000JO10)***

DAZ NO : ***DAZ0FI00100***

BOM P/N : ***43193131L01,46193131L03.***

GPIO MAP: E3 Master GPIO Map10102010.xlsx

E3 MACALLAN 15.6" SG

rPGA Sandy Bridge +
FCBGA PCH Cougar Point-M

2011-01-12

REV : 1.0(A00)

@ : Nopop Component

CONN@ : Connector Component

MB Type	BOM P/N	
TPM EN/ TCM DIS	43193131L01 (R1)	1@ 3@
TPM DIS/ TCM EN	43193131L02 (R1)	2@ 4@
TPM DIS/ TCM DIS	43193131L03 (R1)	2@ 3@

MB PCB

Part Number	Description
DA80000I700	PCB 0FI LA-6561P REV0 M/B DSC

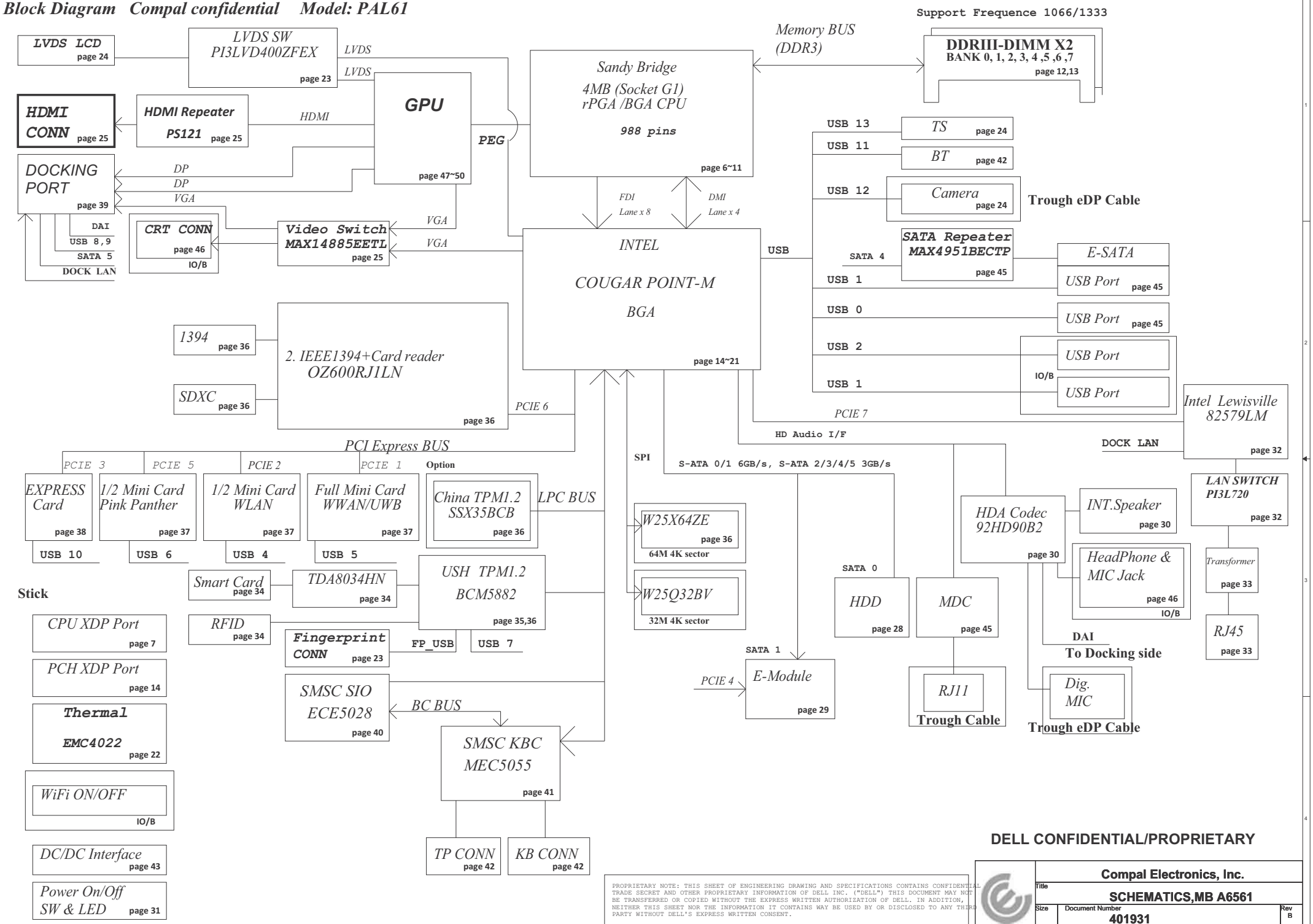
Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 Sheet 1 of 77

Block Diagram Compal confidential Model: PAL61



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 2 of 77

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

Layer No.	Name	Dielectric Constant	Enginner proposal (Unit : mil) Material		Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask		0.6	0.50
			Add Plating		1.3	1.40
1	Top		Copper foil		0.5oz	0.70
			Prepreg	1080LRC	2.80	2.67
2	GND		Copper foil		0.5oz	0.70
			Core	3mil H/1	3.00	3.00
3	Sig1		Copper foil		1.0oz	1.30
			Prepreg	7628HRC*2	17.06	15.10
4	Sig2		Copper foil		1.0oz	1.30
			Core	3mil 1/1	3.00	3.00
5	VCC		Copper foil		1.0oz	1.30
			Prepreg	7628HRC*2	17.06	15.76
6	Sig 3		Copper foil		1.0oz	1.30
			Core	3mil H/1	3.00	3.00
7	GND		Copper foil		0.5oz	0.70
			Prepreg	1080LRC	2.80	2.67
8	Bottom		Copper foil		0.5oz	0.70
			Add Plating		1.3	1.40
			SolderMask		0.6	0.50
Overall Thickness (1.45 mm ± 10%)						57.00
						1.4478

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

DSC DP/HDMI Port	Connetion
Port C	Dock DP port 2
Port D	Dock DP port 1
Port E	MB HDMI Conn

	USB PORT#	DESTINATION
PCH	0	JUSB1 (Ext Right Side)
	1	JESA1 (Ext Right Side)
	2	IO Board- JUSB1 (Ext Left Side)
	3	IO Board- JUSB2 (Ext Left Side)
	4	WLAN
	5	WWAN
	6	JMINI3(Pink Panther)
	7	USH->BIO
	8	DOCKING
	9	DOCKING
	10	Express card
	11	Bluetooth
	12	Camera
	13	LCD Touch

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	MINI CARD-3 (Pink Panther)
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

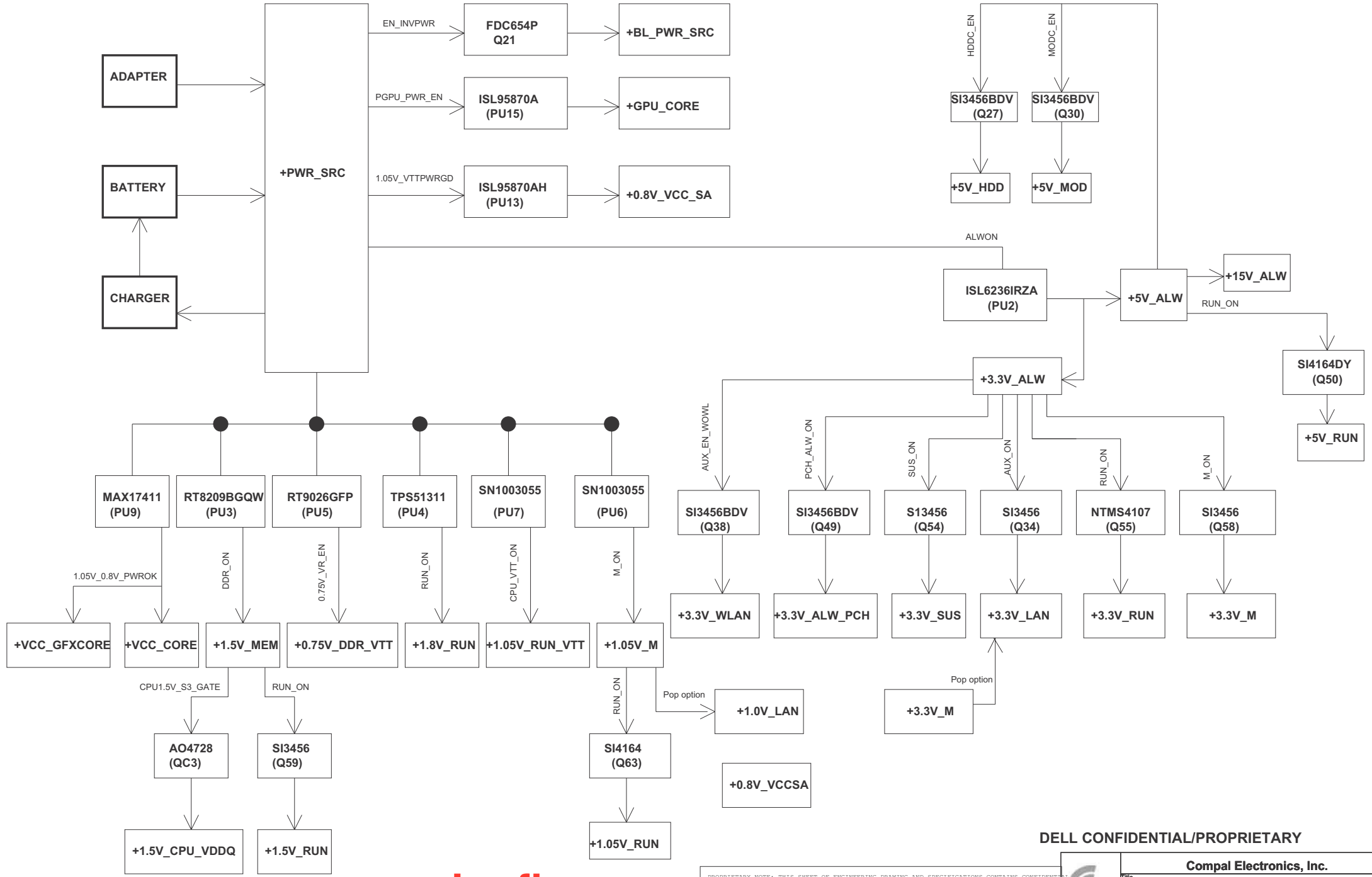
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

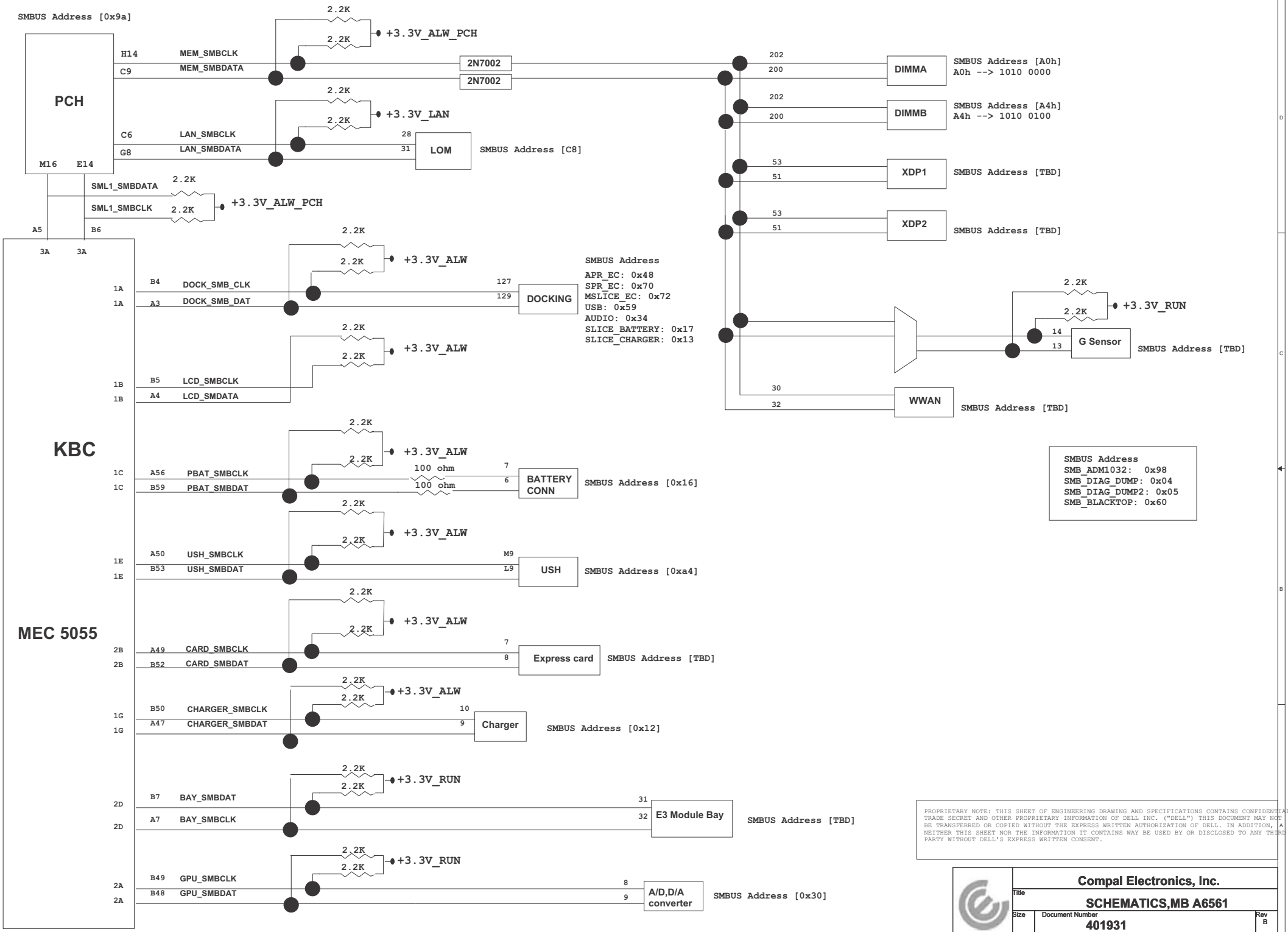
Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 3 of 77



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	SCHEMATICS,MB A6561
Size	Document Number 401931 Rev B
Date: Thursday, January 13, 2011	Sheet 4 of 77

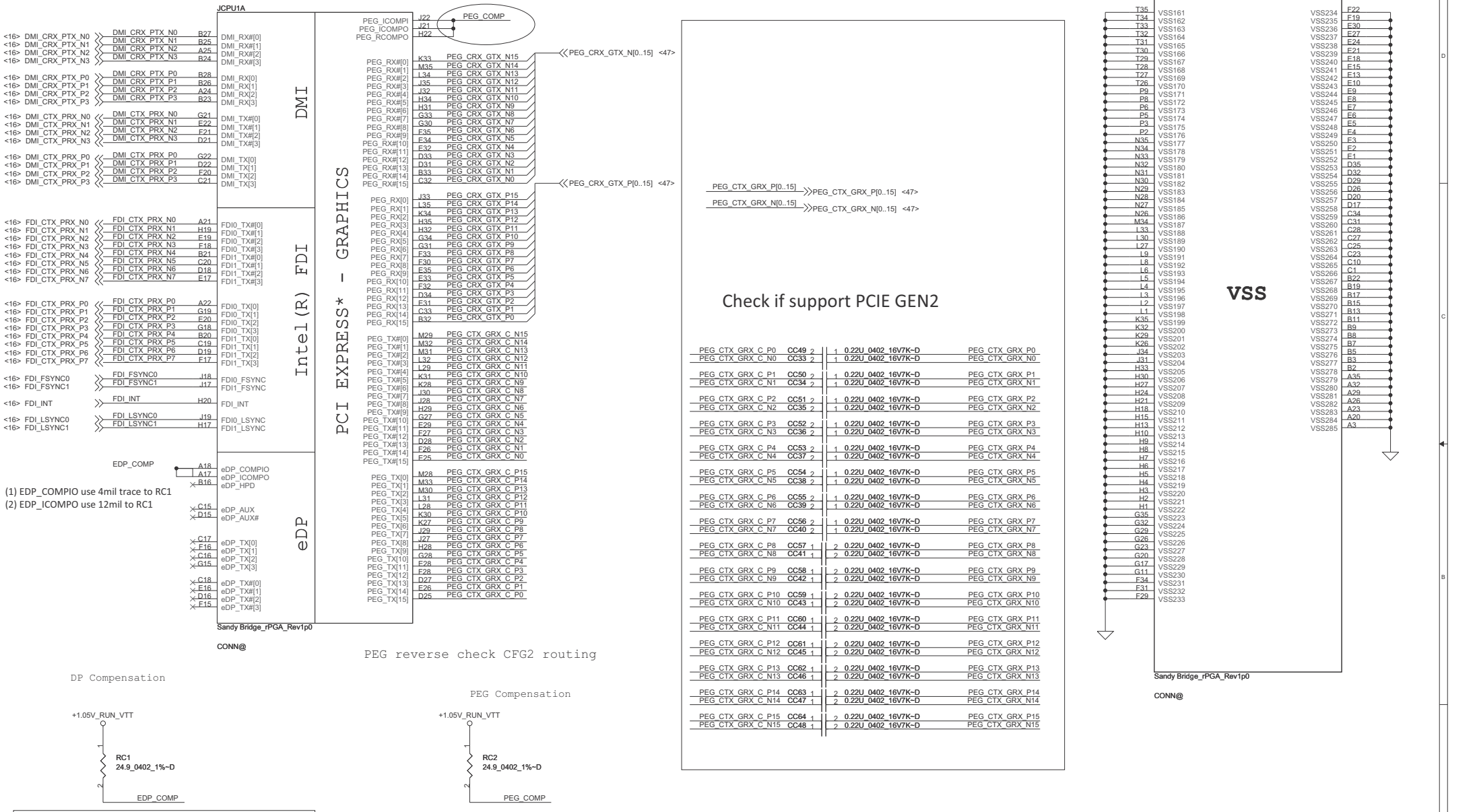


Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 5 of 77



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 6 of 77

Follow DG Rev0.71 SM_DRAMPWROK topology

+1.5V_CPU_VDDQ
+3.3V_ALW_PCH
CC156 1 2 0.1U_0402_16V4Z~D
UC2
<40,41> RUNPWROK
+3.3V_ALW_PCH
RC18 200_0402_5%~D
<16> PM_DRAM_PWRGD
74AHC1G09GW_TSSOP5~D
RUNPWROK_AND
RC12 200_0402_5%~D
RC28 130_0402_5%~D PM_DRAM_PWRGD_CPU
RC64 39_0402_5%~D
<11,43> RUN_ON_CPU1.5VS3#
QC1 SSM3K7002FU_SC70-3~D

+3.3V_ALW_PCH
@RC124 1K_0402_5%~D
SYS_PWROK_XDP
+1.05V_RUN_VTT
CC65 0.1U_0402_16V4Z~D
CC96 0.1U_0402_16V4Z~D
Place near JXDP1

The resistor for HOOK2 should beplaced such that the stub is very small on CFG0 net

+1.05V_RUN_VTT
@RC126 56_0402_5%~D H_THERMTRIP#
@RC128 49.9_0402_1%~D H_CATERR#
RC44 62_0402_5%~D H_PROCHOT#

JCPU1B_CONN@

MISC
C26 PROC_SELECT#
<40> CPU_DETECT# AN34 SKTOCC#

THERMAL
H_CATERR# AL33 CATERR#
<41> PECI_EC AN33 PECI
<41,59> H_PROCHOT# RC57 H_PROCHOT#_R 56_0402_5%~D AL32 PROCHOT#
<22> H_THERMTRIP# @RC129 H_THERMTRIP#_R 0_0402_5%~D AN32 THERMTRIP#

place RC129 near CPU

PWR MANAGEMENT
<16> H_PM_SYNC H_PM_SYNC AM34 PM_SYNC
<18> H_CPUPWRGD @RC25 VCCPWRGOOD_0_R 0_0402_5%~D AP33 UNCOREPWRGOOD
PM_DRAM_PWRGD_CPU V8 SM_DRAMPWROK
PCH_PLTRST#_R AR33 RESET#

CLOCKS
BCLK A28 CPU_DMI
BCLK# A27 CPU_DMI# @RC13 @RC15 0_0402_5%~D CLK_CPU_DMI <15> CLK_CPU_DMI# <15>
DPLL_REF_CLK A16 CPU_DPLL
DPLL_REF_CLK# A15 CPU_DPLL# @RC100 @RC101 0_0402_5%~D CLK_CPU_DPLL <15> CLK_CPU_DPLL# <15>

DDR3 MISC
SM_DRAMRST# R8 DDR3_DRAMRST#_CPU
Max 500mils
SM_RCOMP[0] AK1 SM_RCOMP0
SM_RCOMP[1] A5 SM_RCOMP1
SM_RCOMP[2] A4 SM_RCOMP2

JTAG & BPM
PRDY# AP29 XDP_PRDY#
PREQ# AP27 XDP_PREQ#
TCK AR26 XDP_TCK
TMS AR27 XDP_TMS
TRST# AP30 XDP_TRST#
TDI AR28 XDP_TDI_R
TDO AP26 XDP_TDO_R
DBR# AL35 XDP_DBRESET#_R @RC26 0_0402_5%~D XDP_DBRESET# XDP_DBRESET# <14,16>
BPM#[0] AT28 XDP_OBS0_R @RC30 XDP_OBS0
BPM#[1] AR29 XDP_OBS1_R @RC31 XDP_OBS1
BPM#[2] AR30 XDP_OBS2_R @RC33 XDP_OBS2
BPM#[3] AT30 XDP_OBS3_R @RC34 XDP_OBS3
BPM#[4] AP32 XDP_OBS4_R @RC36 XDP_OBS4
BPM#[5] AR31 XDP_OBS5_R @RC37 XDP_OBS5
BPM#[6] AT31 XDP_OBS6_R @RC38 XDP_OBS6
BPM#[7] AR32 XDP_OBS7_R @RC39 XDP_OBS7
0_0402_5%~D

Sandy Bridge_rPGA_Rev1p0

For ESD concern, please put near CPU

JXDP1
SAMTE_BSH-030-01-L-D-A
CONN@

XDP_PREQ#	3	GND0	GND1 2
XDP_PRDY#	5	OBSFN_A0	OBSFN_C0 4
	7	OBSFN_A1	OBSFN_C1 6
	9	GND2	GND3 8
XDP_OBS0	11	OBSDATA_A0	OBSDATA_C0 10
XDP_OBS1	13	OBSDATA_A1	OBSDATA_C1 12
	15	GND4	GND5 14
XDP_OBS2	17	OBSDATA_A2	OBSDATA_C2 16
XDP_OBS3	19	OBSDATA_A3	OBSDATA_C3 18
	21	GND6	GND7 20
CFG10	23	OBSFN_B0	OBSFN_D0 22
CFG11	25	OBSFN_B1	OBSFN_D1 24
	27	GND8	GND9 26
XDP_OBS4	29	OBSDATA_B0	OBSDATA_D0 28
XDP_OBS5	31	OBSDATA_B1	OBSDATA_D1 30
	33	GND10	GND11 32
XDP_OBS6	35	OBSDATA_B2	OBSDATA_D2 34
XDP_OBS7	37	OBSDATA_B3	OBSDATA_D3 36
	39	GND12	GND13 38
	41	PWRGOOD/HOOK0	ITPCLK/HOOK4 40
	43	HOOK1	ITPCLK#/HOOK5 42
	45	VCC_OBS_AB	VCC_OBS_CD 44
	47	HOOK2	RESET#/HOOK6 46
	49	HOOK3	DBR#/HOOK7 48
	51	GND14	GND15 50
	53	SDA	TD0 52
	55	SCL	TRST# 54
XDP_TCLK	57	TCK1	TDI 56
	59	TCK0	TMS 58
		GND16	GND17 60

CFG16	4	CFG16 <9>
CFG17	6	CFG17 <9>
CFG0	10	CFG0 <9>
CFG1	12	CFG1 <9>
CFG2	16	CFG2 <9>
CFG3	18	CFG3 <9>
CFG8	22	CFG8 <9>
CFG9	24	CFG9 <9>
CFG4	28	CFG4 <9>
CFG5	30	CFG5 <9>
CFG6	34	CFG6 <9>
CFG7	36	CFG7 <9>
CLK_XDP	40	
CLK_XDP#	42	
XDP_RST#_R	46	
XDP_DBRESET#	48	
XDP_TDO	52	
XDP_TRST#	54	
XDP_TDI	56	
XDP_TMS	58	
	60	

H_CPUPWRGD 1 RC51 2 1K_0402_5%~D H_CPUPWRGD_XDP
<14,16> SIO_PWRBTN#_R @ RC6 CFD_PWRBTN#_XDP
CFG0 1 RC7 2 1K_0402_5%~D XDP_HOOK2
<16,40> SYS_PWROK @RC9 SYS_PWROK_XDP
<12,13,14,15,28,37> DDR_XDP_WAN_SMBDAT RC125 0_0402_5%~D DDR_XDP_WAN_SMBDAT_R1
<12,13,14,15,28,37> DDR_XDP_WAN_SMBCLK RC127 0_0402_5%~D DDR_XDP_WAN_SMBCLK_R1
XDP_TCLK

XDP_RST#_R RC8 1K_0402_5%~D PLTRST_XDP# <17>

CLK_XDP @RH107 0_0402_5%~D CLK_CPU_ITP <15>
CLK_XDP# @RH106 0_0402_5%~D CLK_CPU_ITP# <15>
<9> CLK_XDP_ITP @RH109 0_0402_5%~D
<9> CLK_XDP_ITP# @RH108 0_0402_5%~D

@RC48 0_0402_5%~D
QC2 BSS138W-7-F_SOT323-3~D
DDR3_DRAMRST# <12>
RC50 4.99K_0402_1%~D
DDR_HVREF_RST
CC177 0.047U_0402_16V4Z~D
<15> DDR_HVREF_RST_PCH @RC46 0_0402_5%~D
<41> DDR_HVREF_RST_GATE @RC47 0_0402_5%~D

PU/PD for JTAG signals
+3.3V_RUN
XDP_DBRESET# RC19 1K_0402_5%~D
+1.05V_RUN_VTT
XDP_TMS RC27 51_0402_1%~D
XDP_TDI_R RC29 51_0402_1%~D
XDP_PREQ# @RC32 51_0402_1%~D
XDP_TDO RC35 51_0402_1%~D
XDP_TCLK RC40 51_0402_1%~D
XDP_TRST# RC41 51_0402_1%~D

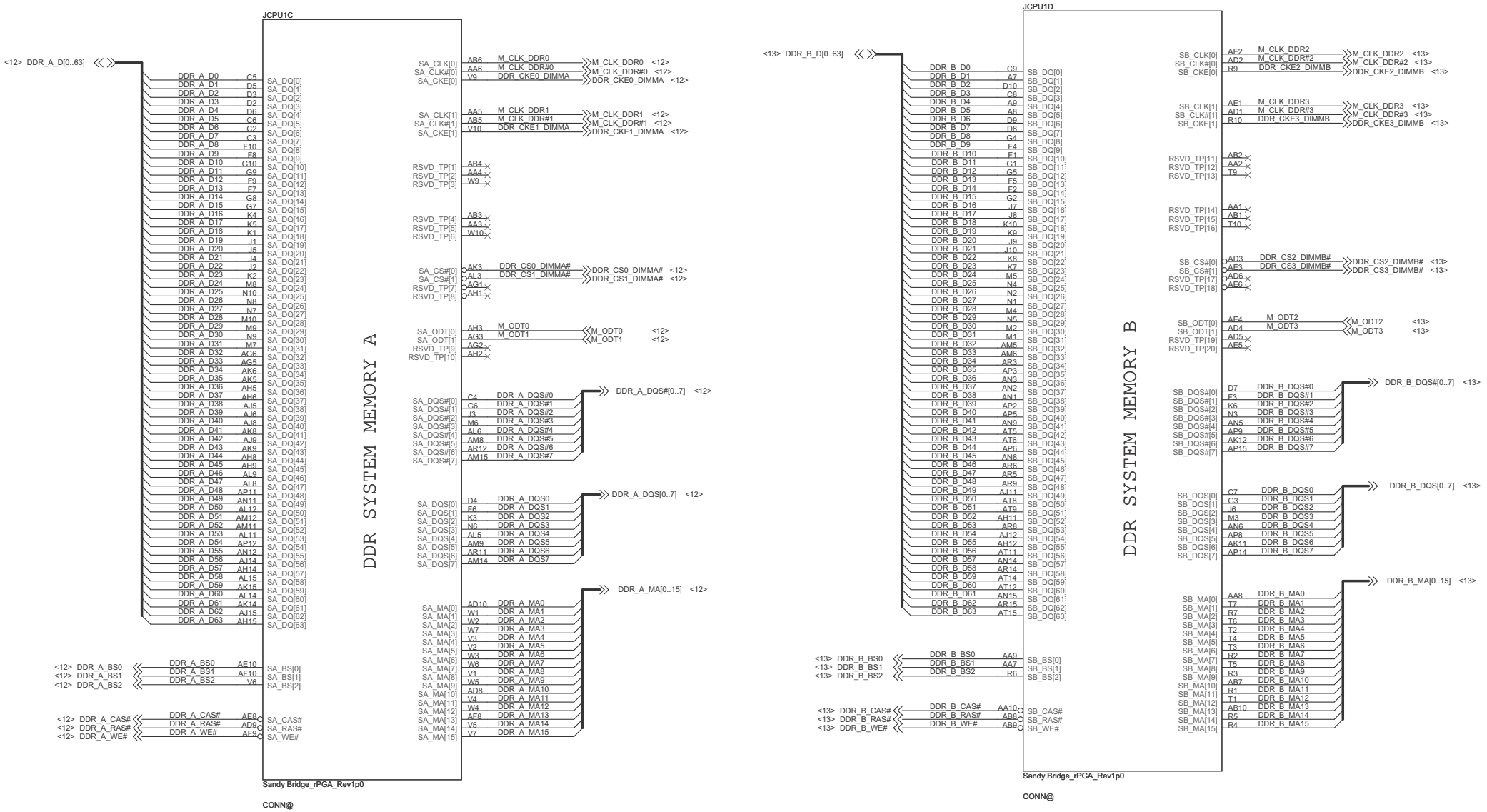
XDP_TDI_R @RC23 0_0402_5%~D XDP_TDI
XDP_TDO_R @ RC24 0_0402_5%~D XDP_TDO

Buffered reset to CPU
+3.3V_RUN
+1.05V_RUN_VTT
CC140 0.1U_0402_16V4Z~D
RC4 75_0402_1%~D
UC1
<14,17> PCH_PLTRST#
SN74LVC1G07DCKR_SC70-5~D
PCH_PLTRST#_BUF
RC10 43_0402_5%~D PCH_PLTRST#_R
Open drain buffer

VCCPWRGOOD_0_R
RC130 10K_0402_5%~D
Avoid stub in the PWRGD path while placing resistors RC25 & RC130

SM_RCOMP2
SM_RCOMP1
SM_RCOMP0
RC42 140_0402_1%~D
RC43 25.5_0402_1%~D
RC45 200_0402_1%~D

Compal Electronics, Inc.
Title: SCHEMATICS,MB A6561
Size: Document Number: 401931 Rev: B
Date: Thursday, January 13, 2011 Sheet 7 of 77



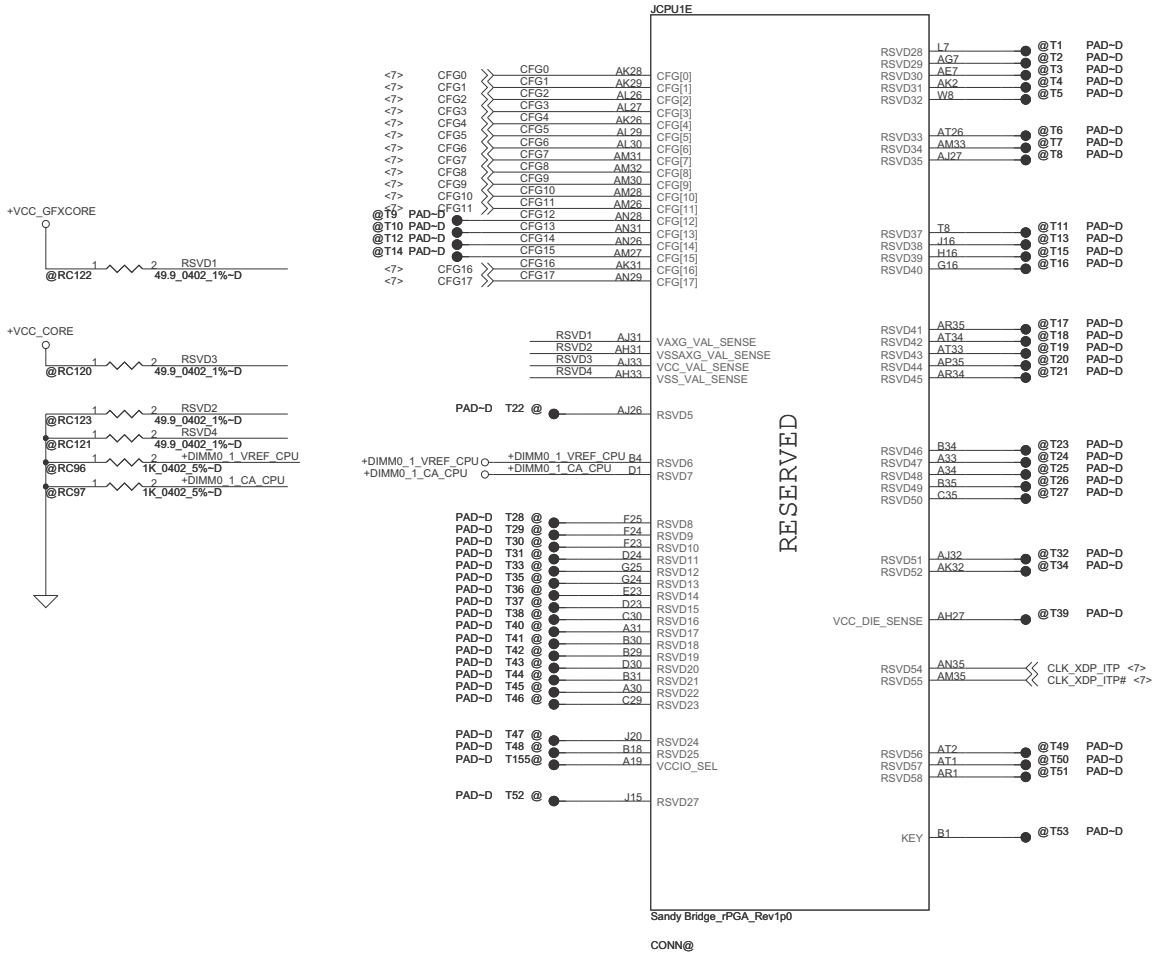
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

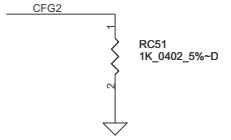
Title: **SCHEMATICS,MB A6561**

Size | Document Number: **401931** | Rev: **B**

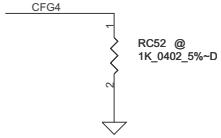
Date: Thursday, January 13, 2011 | Sheet 8 of 77



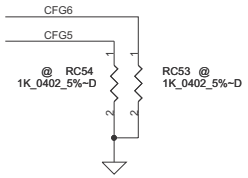
CFG Straps for Processor



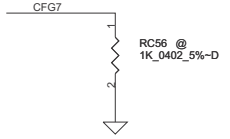
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

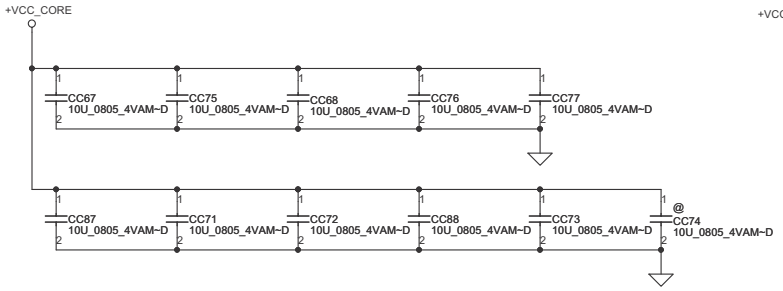


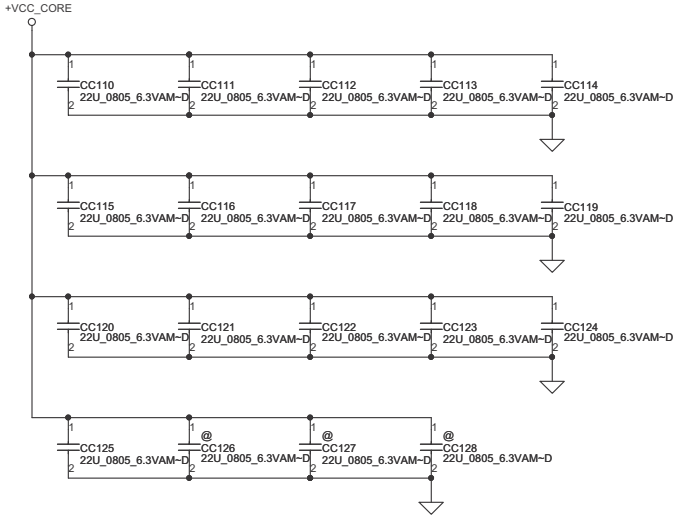
PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

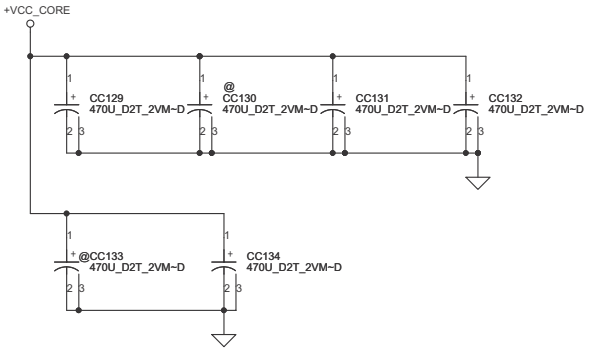


PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

POWER



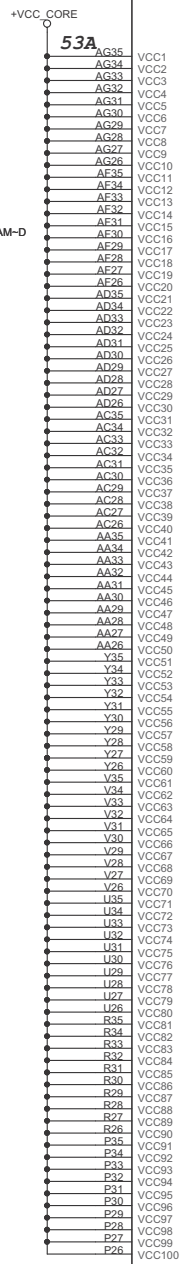




JCPU1F

Sandy Bridge_rPGA_Rev1p0

CONN@

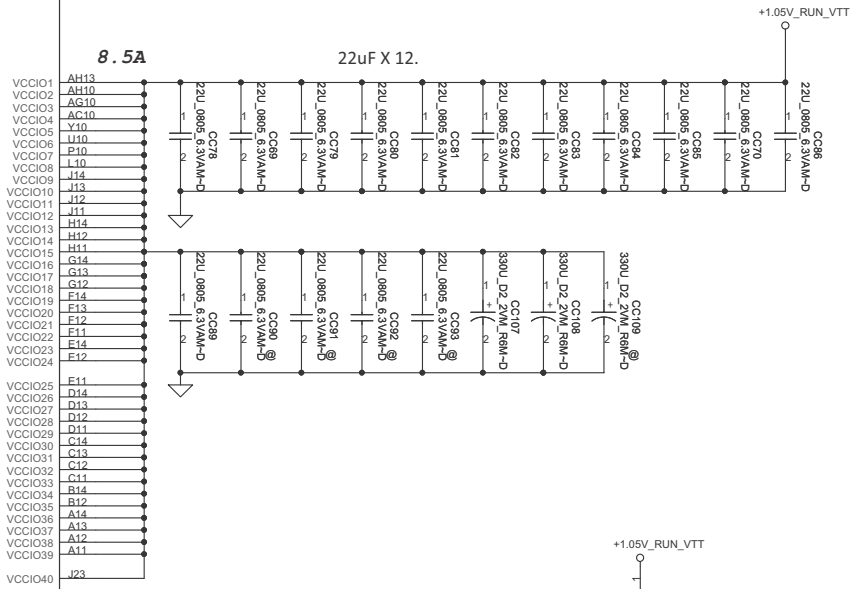


CORE SUPPLY

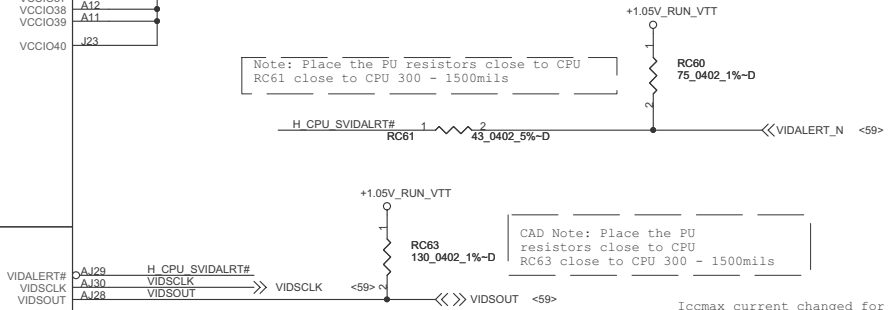
PEG AND DDR

8.5A

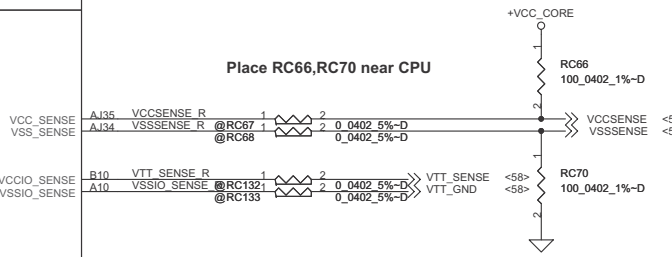
22uF X 12.



SVID



SENSE LINES



Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05	8.5
VAXG	0.0-1.1	26
VCCPLL	1.8	3
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 ★

★ Description

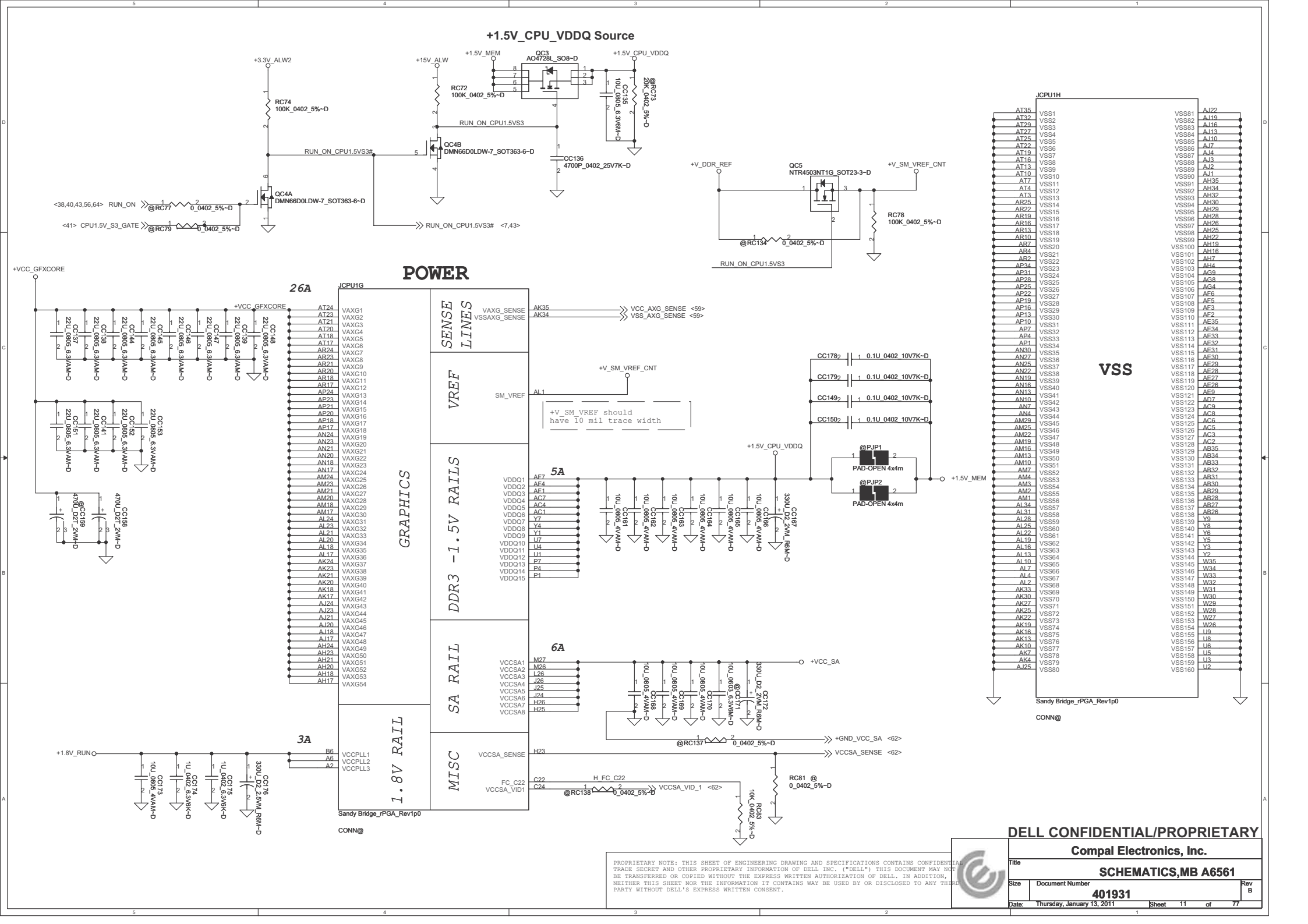
5A to Mem controller(+1.5V_CPU_VDDQ)
5-6A to 2 DIMMs/channel
2-5A to +1.5V_RUN & +0.75V_DDR_VTT

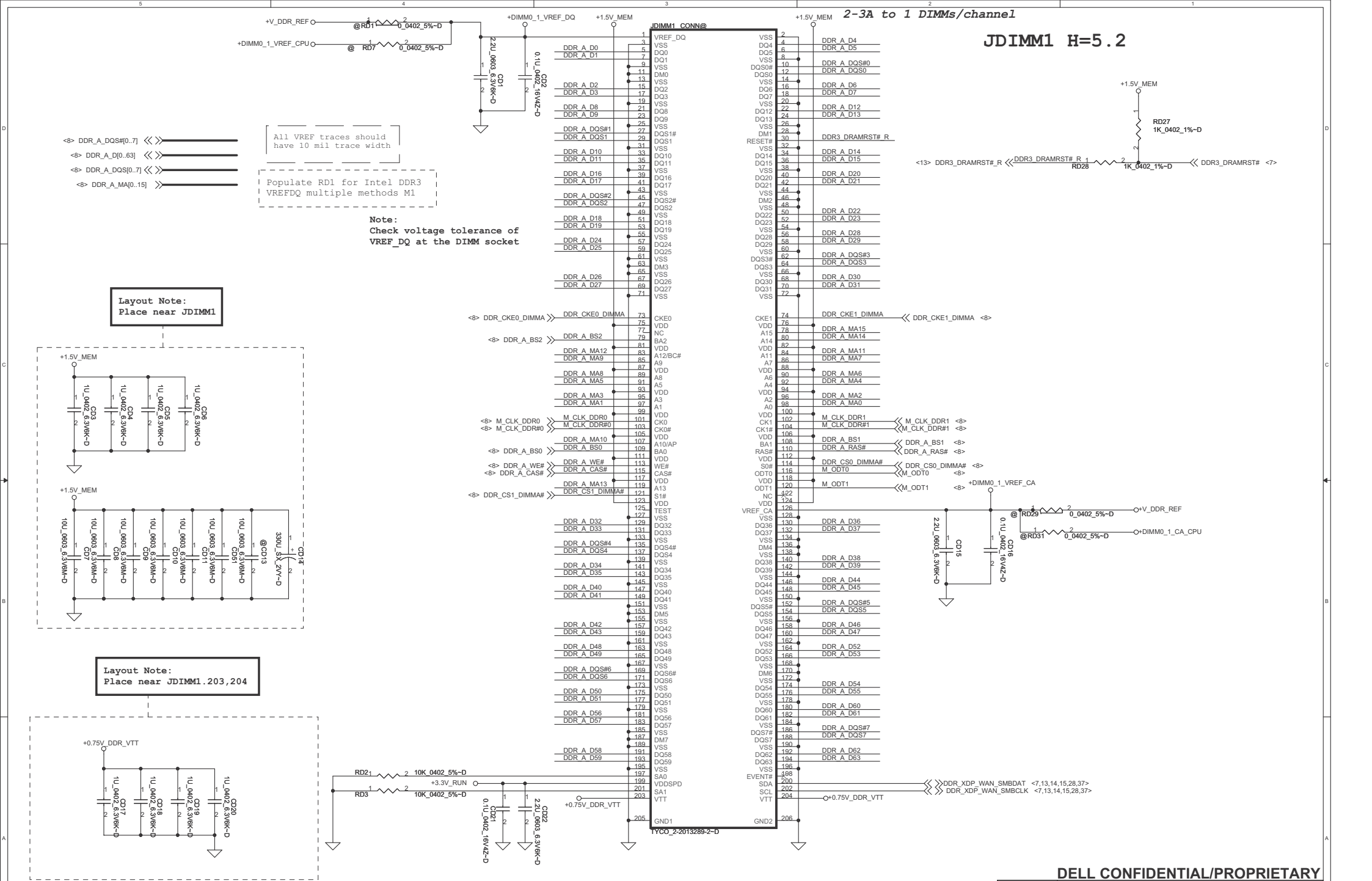
Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 10 of 77


+1.5V_CPU_VDDQ Source
POWER
JCPU1G
JCPU1H
VSS
GRAPHICS
DDR3 -1.5V RAILS
SA RAIL
1.8V RAIL
MISC
SENSE LINES
VREF
+V_SM_VREF should have 10 mil trace width
Sandy Bridge_rPGA_Rev1p0
CONN@
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
SCHEMATICS,MB A6561
401931
Thursday, January 13, 2011
Sheet 11 of 77



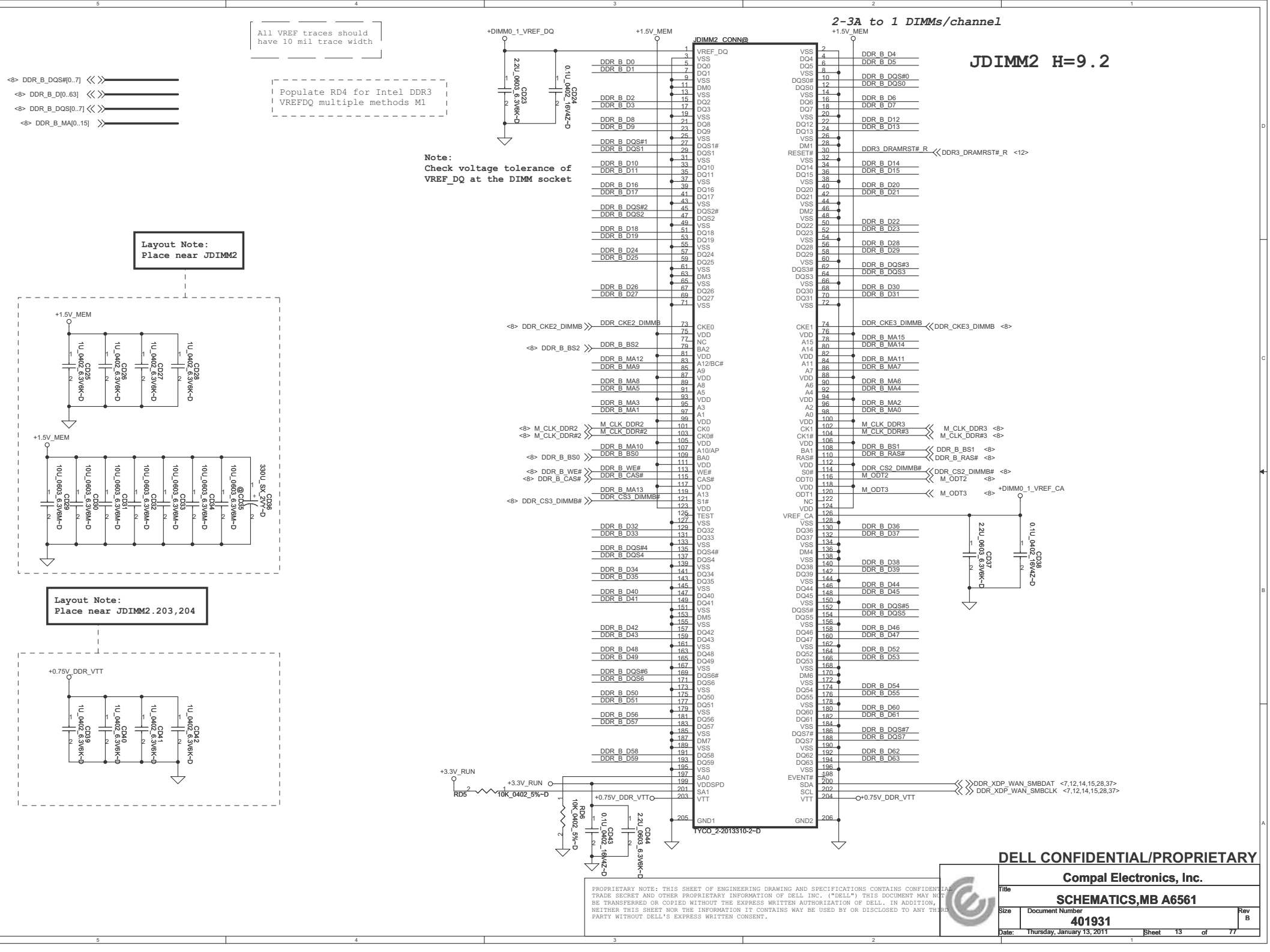
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size: | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 12 of 77



CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

PCH_AZ_SYNC is sampled at the rising edge of RSMRST# pin. So signal should be PU to the ALWAYS rail.

On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low

INTVRMEN- Integrated SUS 1.1V VRM Enable
* High - Enable Internal VRs
Low - Enable External VRs

CMOS place near DIMM

SPI_MOSI (PCH_SPI_DO)
High: Enable Intel Anti-Theft Technology
Left floating: Disable Intel Anti-Theft Technology

BBS_BIT0 - BIOS BOOT STRAP BIT 0

No Reboot Strap
SPKR: Low = Default; High = No Reboot

200 MIL SO8
64Mb Flash ROM
X76@ U52
W25Q64BVSSIG_SO8~D

200 MIL SO8
16Mb Flash ROM
X76@ U53
W25Q16BVSSIG_SO8~D

HRS_FH12-16S-0P5SH(55)~D

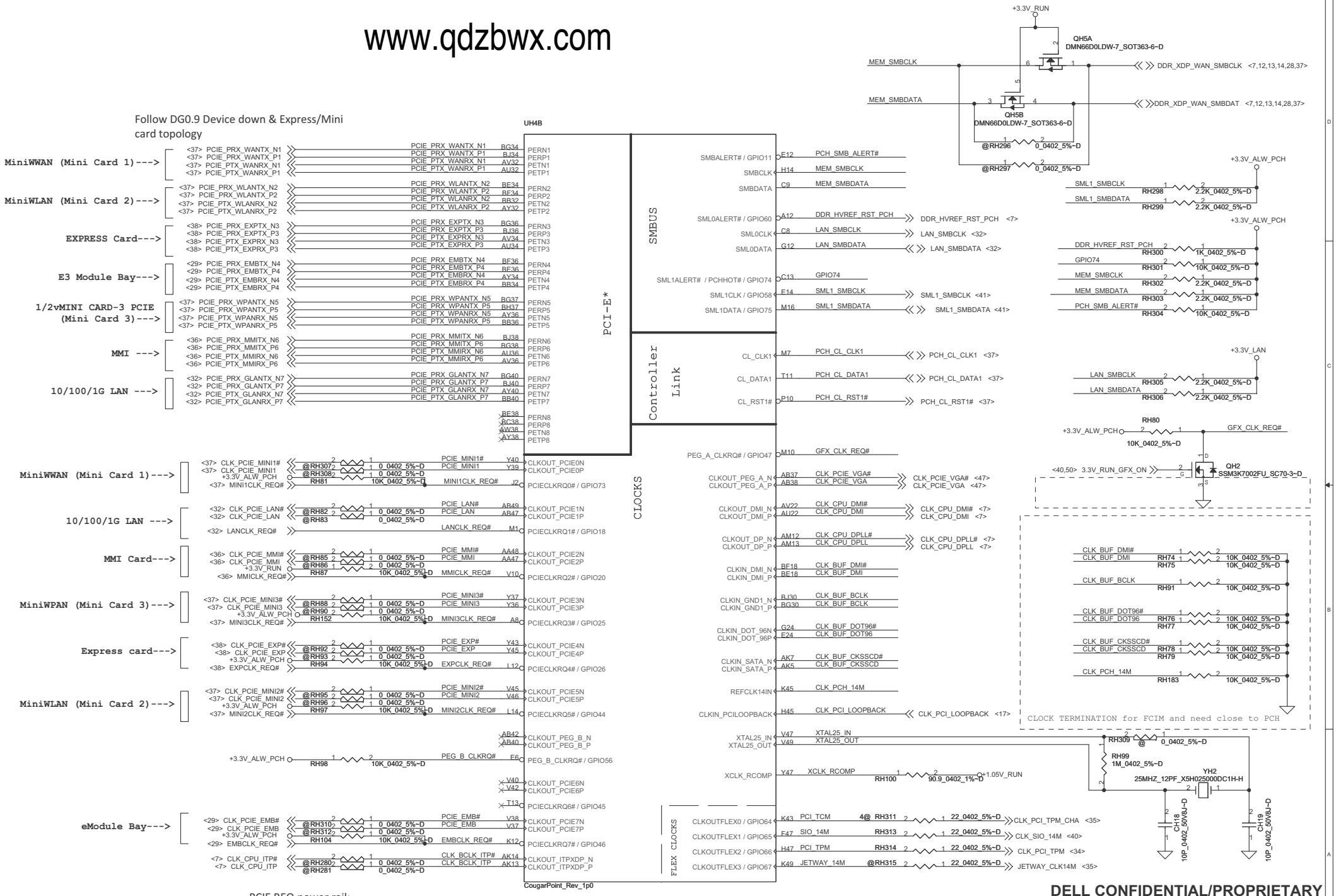
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size: | Document Number: 401931 | Rev: B

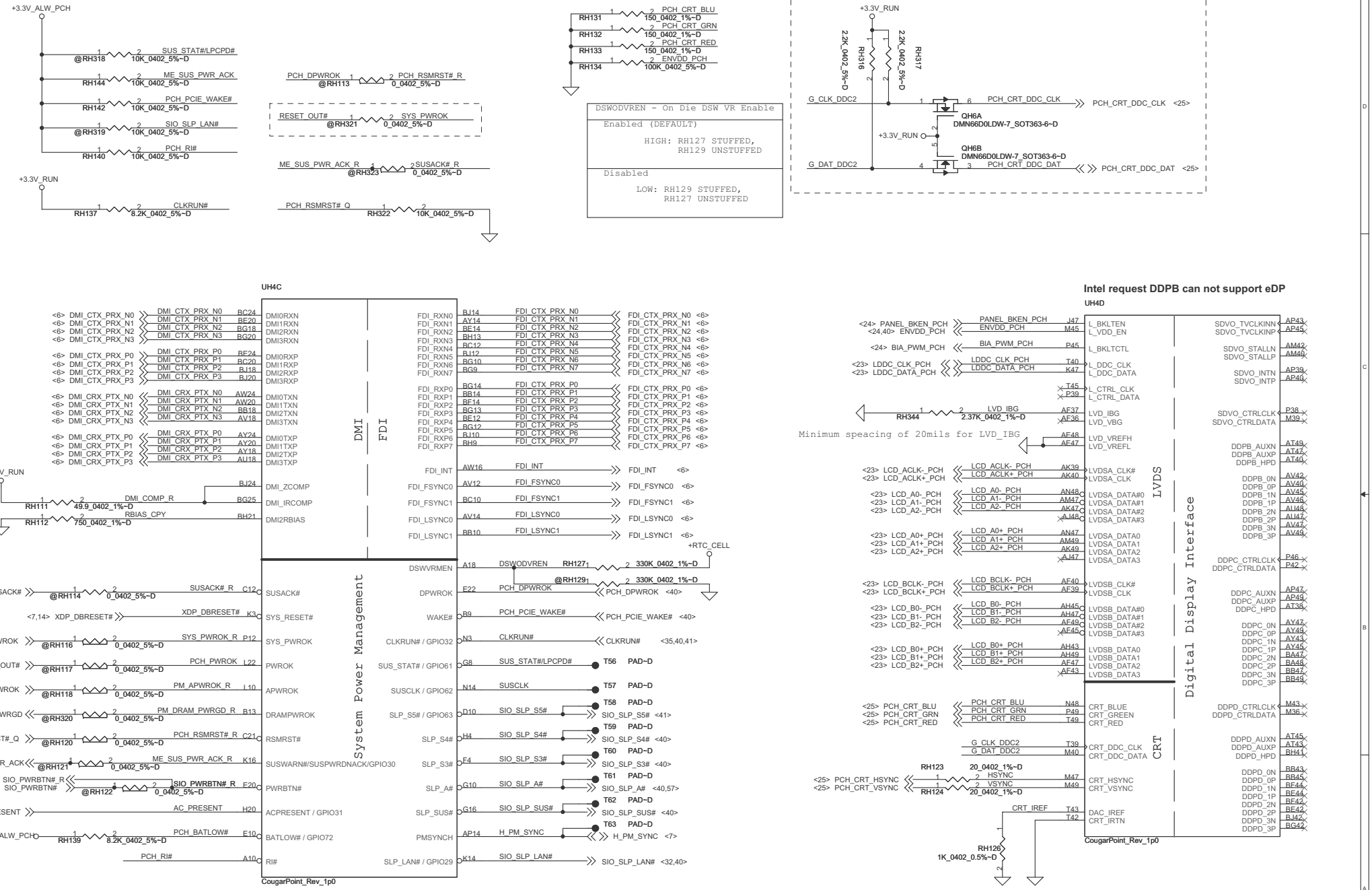
Date: Thursday, January 13, 2011 | Sheet 14 of 77



PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	SCHEMATICS,MB A6561
Size	Document Number: 401931 — Rev: B
Date: Thursday, January 13, 2011	Sheet 15 of 77

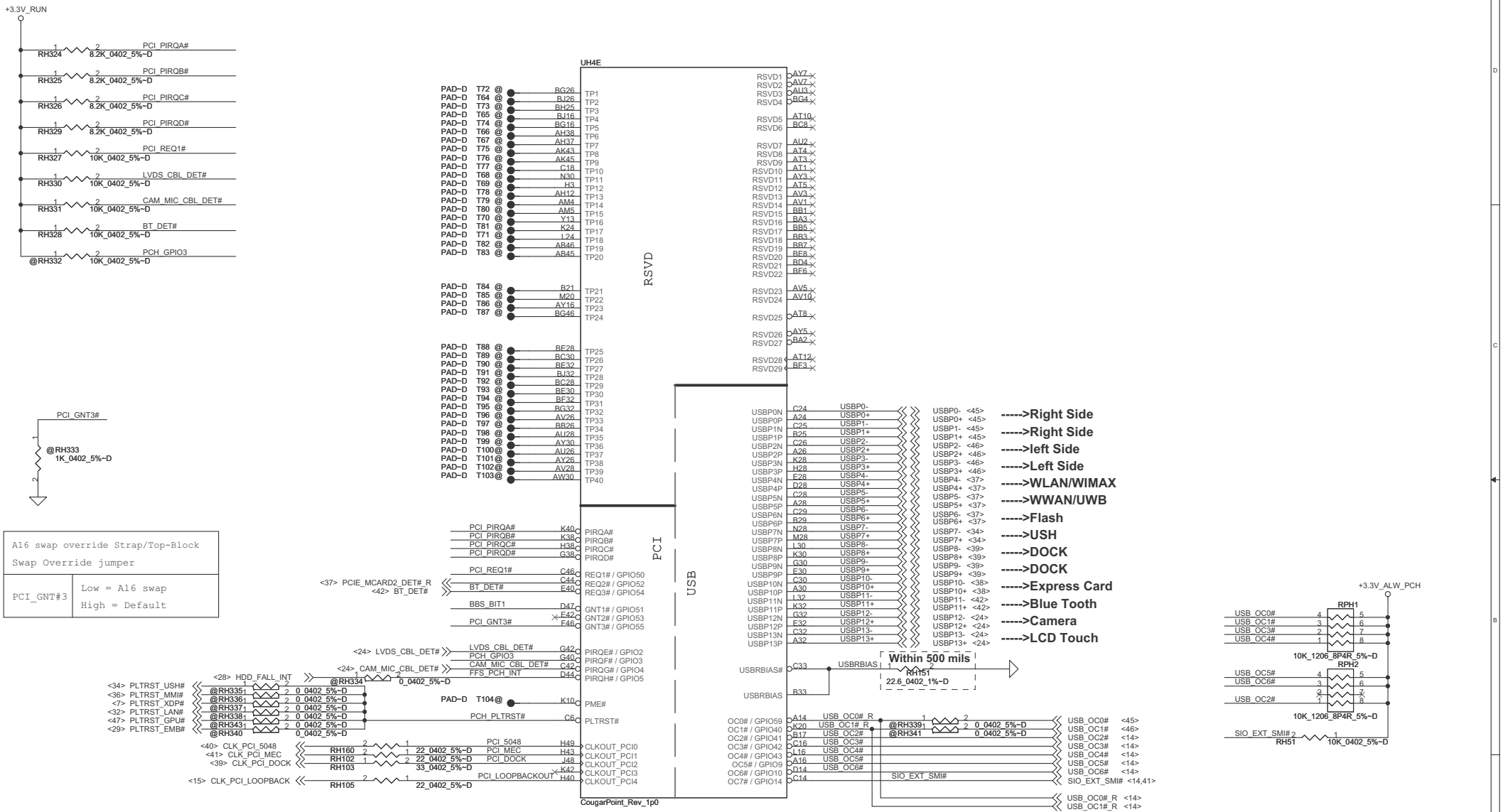


Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 16 of 77



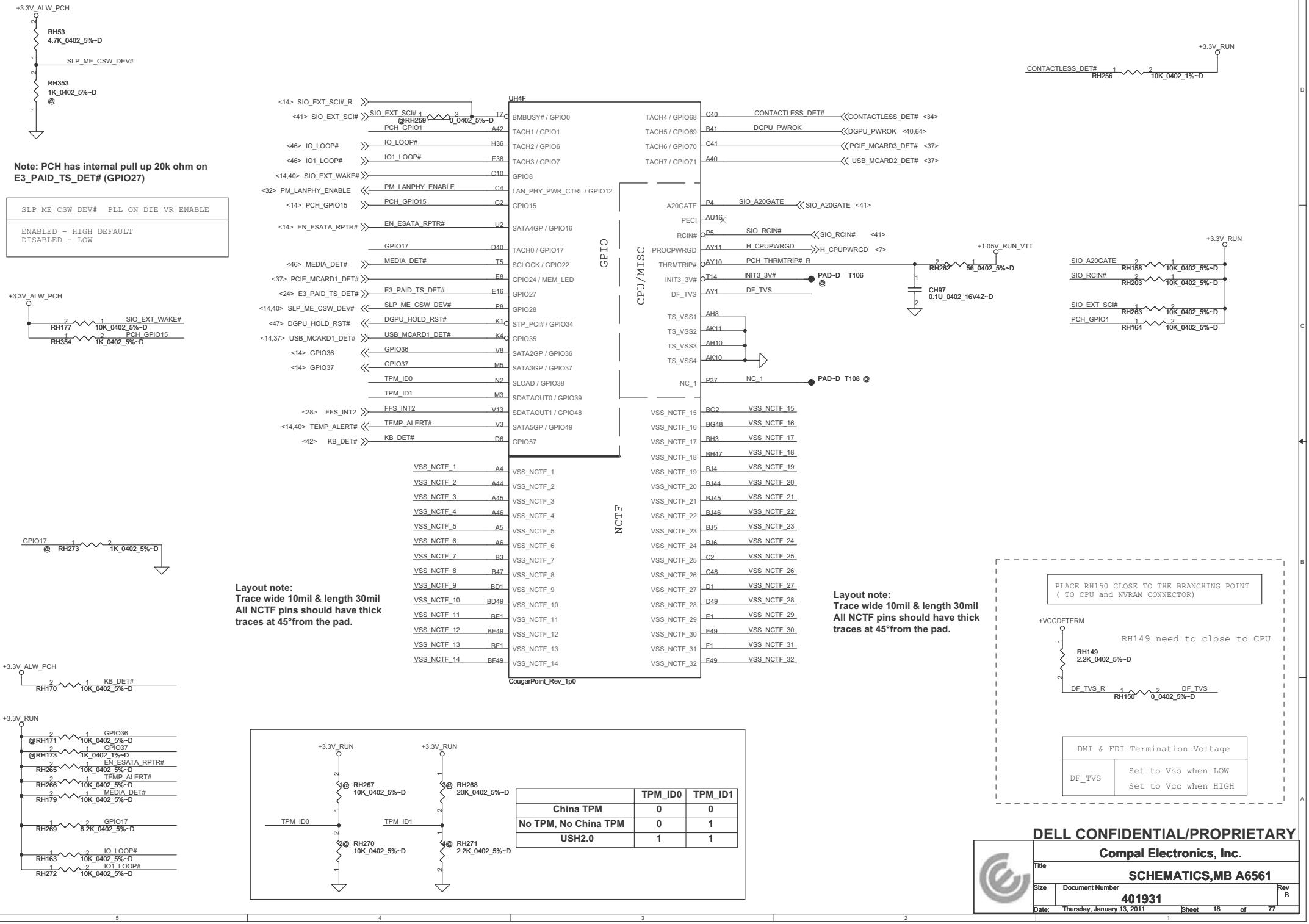
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

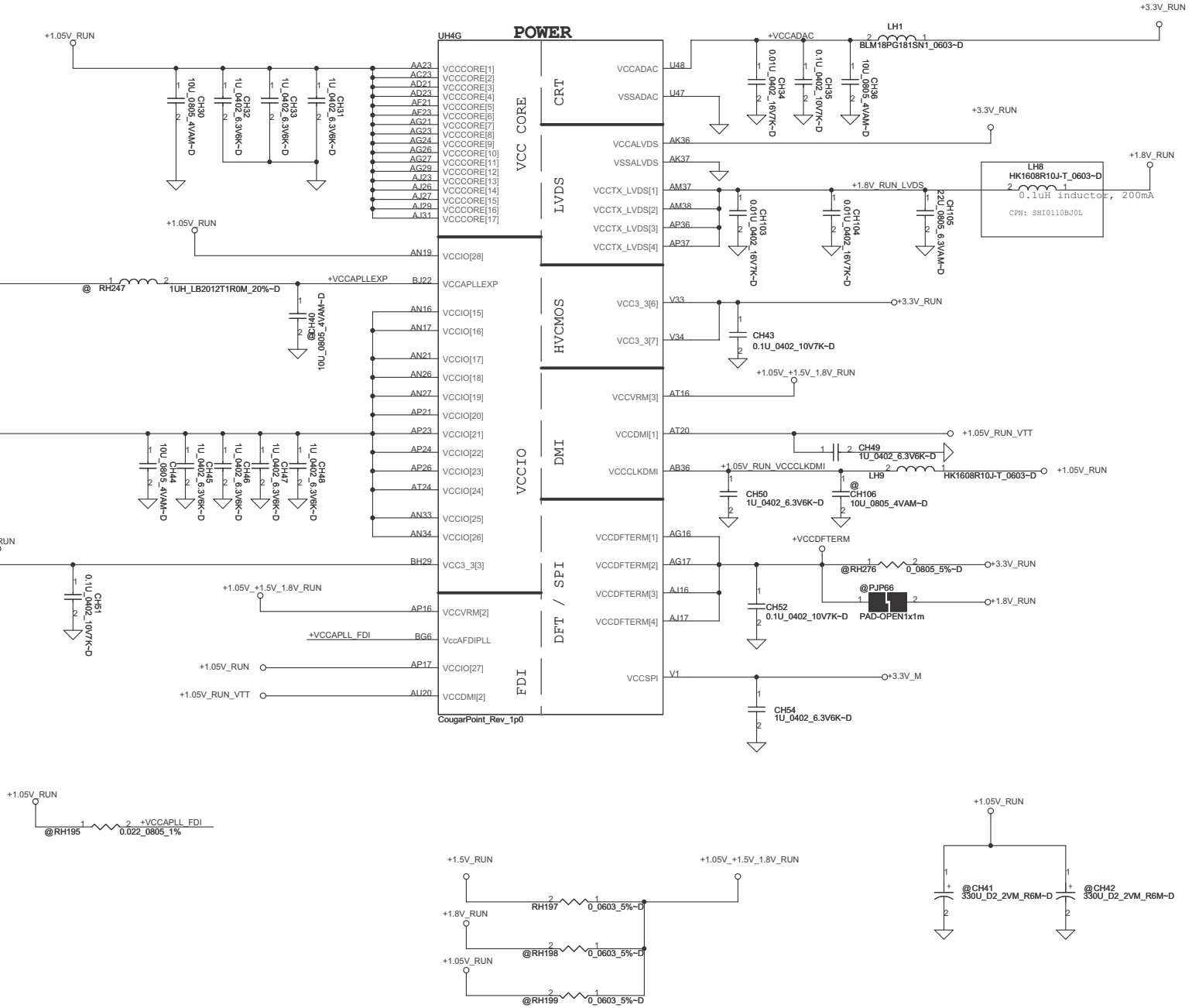
Date: Thursday, January 13, 2011 | Sheet 17 of 77



	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
USH2.0	1	1

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	SCHEMATICS,MB A6561
Size	Document Number: 401931 — Rev: B
Date: Thursday, January 13, 2011	Sheet 18 of 77



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.020
VccDSW3_3	3.3	0.003
VccpDFTERM	1.8	0.19
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.119
VccSusHDA	3.3	0.01
VccVRM	1.8 / 1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06
VccAPLLEXP	1.05	0.05

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 19 of 77

Note: C225 - STUFFED ONLY FOR CPT INTERPOSER;
UNSTUFF FOR CPT

POWER

UH4J

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | CPU | MISC | RTC | HDA

CougarPoint_Rev_1p0

+1.05V_RUN
@RH200 0.022_0805_1% +VCCACLK
AD49 VCCACLK
+3.3V_ALW_PCH
+3.3V_ALW2
@RH201 0_0402_5%~D
@RH253 0_0402_5%~D
CH55 0.1U_0402_10V7K~D
T16 VCCDSW3_3 +VCCDSW3_3
+PCH_VCCDSW V12 DCPSUSBYP
+1.05V_RUN
@ LH3 10UH_LBR2012T100M_20%~D
@ CH57 0.1U_0402_10V7K~D
T38 VCC3_3[5] +3.3V_RUN_VCC_CLKF33
@ CH58 10U_0805_6.3V6M~D
BH23 VCCAPLLDMI2 +VCCAPLL_CPY_PCH
+1.05V_RUN
AL29 VCCIO[14]
+VCCSUS1 AL24 DCPSUS[3]
@CH61 1U_0402_6.3V6K~D
AA19 VCCASW[1]
AA21 VCCASW[2]
AA24 VCCASW[3]
AA26 VCCASW[4]
AA27 VCCASW[5]
AA29 VCCASW[6]
AA31 VCCASW[7]
AC26 VCCASW[8]
AC27 VCCASW[9]
AC29 VCCASW[10]
AC31 VCCASW[11]
AD29 VCCASW[12]
AD31 VCCASW[13]
W21 VCCASW[14]
W23 VCCASW[15]
W24 VCCASW[16]
W26 VCCASW[17]
W29 VCCASW[18]
W31 VCCASW[19]
W33 VCCASW[20]
CH64 22U_0805_6.3V6M~D
CH65 22U_0805_6.3V6M~D
+1.05V_M
CH67 1U_0402_6.3V6K~D
CH68 1U_0402_6.3V6K~D
CH69 1U_0402_6.3V6K~D
+3.3V_RUN
@RH215 0.022_0805_1%
LH4 10UH_LBR2012T100M_20%~D
+3.3V_RUN_VCC_CLKF33
@ CH73 10U_0805_6.3V6M~D
CH74 1U_0402_6.3V6K~D
+VCCRTCEXT N16 DCPRTC
CH78 0.1U_0402_10V7K~D
+1.05V_+1.5V_1.8V_RUN
Y49 VCCVRM[4]
+1.05V_RUN
+1.05V_RUN_VCCA_A_DPL BD47 VCCADPLLA
+1.05V_RUN_VCCA_B_DPL BF47 VCCADPLLB
CH79 1U_0402_6.3V6K~D
AF17 VCCIO[7]
AF33 VCCDIFFCLKN[1]
AF34 VCCDIFFCLKN[2]
AG34 VCCDIFFCLKN[3]
CH81 1U_0402_6.3V6K~D
AG33 VCCSSC
CH96 1U_0402_6.3V6K~D
+1.05V_M
@RH248 0.022_0805_1% +1.05V_M_VCCSUS
+VCCSST V16 DCPSST
+1.05V_M_VCCSUS
T17 DCPSUS[1]
V19 DCPSUS[2]
CH84 0.1U_0402_10V7K~D
CH83 @ 1U_0402_6.3V6K~D
+1.05V_RUN_VTT
BJ8 V_PROC_IO
CH85 4.7U_0603_6.3V6K~D
CH86 0.1U_0402_10V7K~D
CH87 0.1U_0402_10V7K~D
+RTC_CELL
A22 VCCRTC
CH88 0.1U_0402_10V7K~D
CH89 0.1U_0402_10V7K~D
CH90 1U_0402_6.3V6K~D
LH6 10UH_LBR2012T100M_20%~D
+1.05V_RUN
LH7 10UH_LBR2012T100M_20%~D
+1.05V_RUN_VCCA_A_DPL
+1.05V_RUN_VCCA_B_DPL
220U_B2_2.5VM_R35M~D
CH84 CH82 CH85 CH83
1U_0402_6.3V6K~D
+1.05V_RUN_VCCA_A_DPL
@RH279 0_0805_5%~D
+1.05V_RUN_VCCA_B_DPL

VCCIO[29] N26
VCCIO[30] P26
VCCIO[31] P28
VCCIO[32] T27
VCCIO[33] T29
CH56 1U_0402_6.3V6K~D
+1.05V_RUN
VCCSUS3_3[7] T23
VCCSUS3_3[8] T24
VCCSUS3_3[9] V23
VCCSUS3_3[10] V24
VCCSUS3_3[6] P24
+3.3V_ALW_PCH
CH59 0.1U_0402_10V7K~D
CH60 0.1U_0402_10V7K~D
VCCIO[34] T26
+1.05V_RUN
V5REF_SUS M26 +PCH_V5REF_SUS
DCPSUS[4] AN23 +VCCA_USBSUS
VCCSUS3_3[1] AN24
CH66 0.1U_0402_10V7K~D
V5REF P34 +PCH_V5REF_RUN
VCCSUS3_3[2] N20
VCCSUS3_3[3] N22
VCCSUS3_3[4] P20
VCCSUS3_3[5] P22
CH70 1U_0603_10V6K~D
+3.3V_RUN
VCC3_3[1] AA16
VCC3_3[8] W16
CH72 0.1U_0402_10V7K~D
VCC3_3[4] T34
CH75 0.1U_0402_10V7K~D
VCC3_3[2] AJ2
VCCIO[5] AF13
VCCIO[12] AH13
VCCIO[13] AH14
VCCIO[6] AF14
CH76 0.1U_0402_10V7K~D
CH77 1U_0402_6.3V6K~D
VCCAPLLSATA AK1 +VCCSATAPLL
VCCVRM[1] AF11
+1.05V_+1.5V_1.8V_RUN
LH5 @ 10UH_LBR2012T100M_20%~D
CH80 @ 10U_0805_6.3V6M~D
VCCIO[2] AC16
VCCIO[3] AC17
VCCIO[4] AD17
CH82 1U_0402_6.3V6K~D
VCCASW[22] T21
VCCASW[23] V21
VCCASW[21] T19
VCCSUSHDA P32
CH91 0.1U_0402_10V7K~D

+5V_ALW
+5V_ALW_PCH
PJP68 PAD-OPEN1x1m
@QH4 SSM3K7002FU_SC70-3~D
<43> ALW_ENABLE
CH98 @ 0.1U_0402_10V7K~D
@RH278 20K_0402_5%~D
+5V_ALW_PCH
+3.3V_ALW_PCH
RH208 10_0402_5%~D
DH2 RB751S40T1_SOD523-2~D
+PCH_V5REF_SUS
CH63 0.1U_0402_10V7K~D
CRB 0.7 RH208,RH213 trace width 20mil.
+5V_RUN
+3.3V_RUN
RH213 10_0402_5%~D
DH3 RB751S40T1_SOD523-2~D
+PCH_V5REF_RUN
CH71 1U_0603_10V6K~D
+VCCA_USBSUS
@CH62 1U_0402_6.3V6K~D

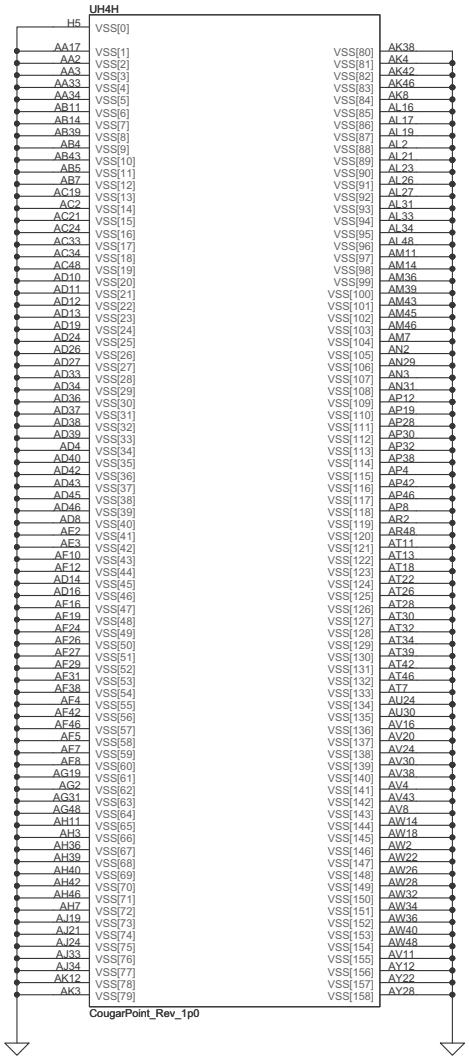
DELL CONFIDENTIAL/PROPRIETARY

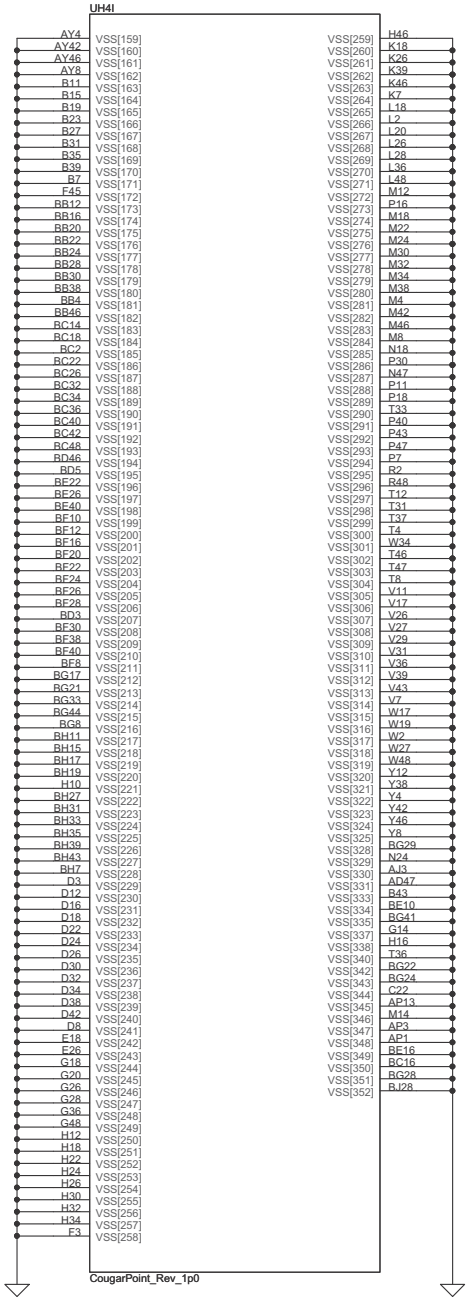
Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size: | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 20 of 77





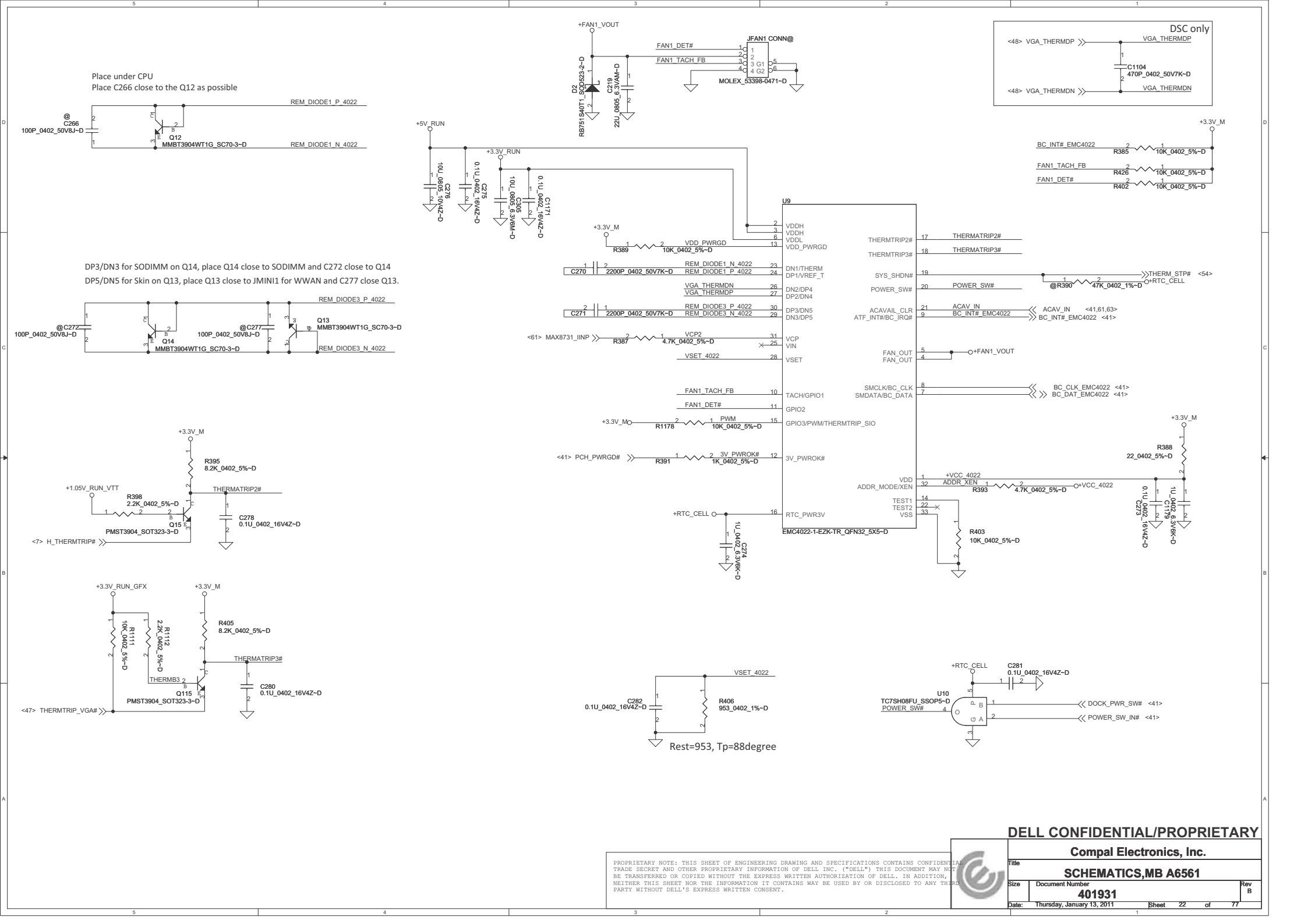
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: **SCHEMATICS,MB A6561**

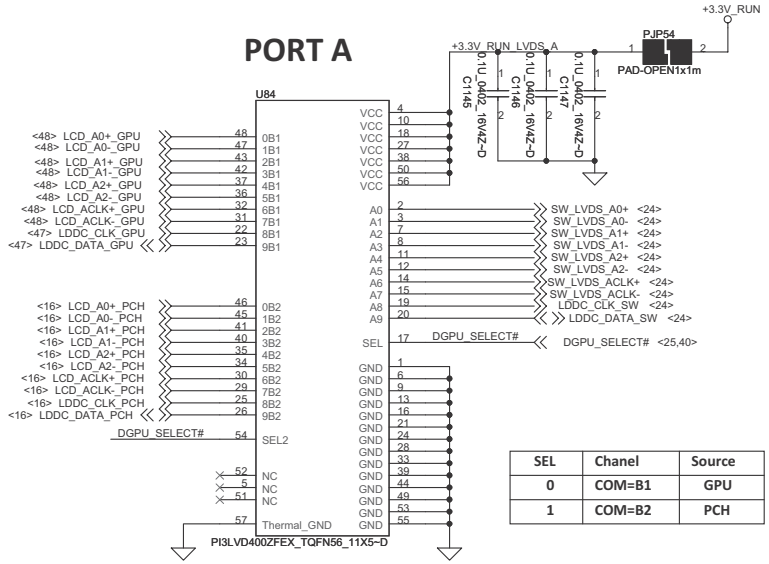
Size | Document Number: **401931** | Rev: B

Date: Thursday, January 13, 2011 | Sheet 21 of 77


Place under CPU
Place C266 close to the Q12 as possible
@C266 100P_0402_50V8J~D
Q12 MMBT3904WT1G_SC70-3~D
REM_DIODE1_P_4022
REM_DIODE1_N_4022
DP3/DN3 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
DP5/DN5 for Skin on Q13, place Q13 close to JMINI1 for WWAN and C277 close to Q13.
@C272 100P_0402_50V8J~D
Q14 MMBT3904WT1G_SC70-3~D
@C277 100P_0402_50V8J~D
Q13 MMBT3904WT1G_SC70-3~D
REM_DIODE3_P_4022
REM_DIODE3_N_4022
+FAN1_VOUT
D2 RB751S40T1_SOD523-2~D
C219 22U_0805_6.3V6M~D
FAN1_DET#
FAN1_TACH_FB
JFAN1 CONN@
MOLEX_53398-0471~D
DSC only
<48> VGA_THERMDP
<48> VGA_THERMDN
C1104 470P_0402_50V7K~D
+5V_RUN
+3.3V_RUN
C276 10U_0805_10V4Z~D
C275 0.1U_0402_16V4Z~D
C305 10U_0805_6.3V6M~D
C1171 0.1U_0402_16V4Z~D
+3.3V_M
BC_INT#_EMC4022
FAN1_TACH_FB
FAN1_DET#
R385 10K_0402_5%~D
R426 10K_0402_5%~D
R402 10K_0402_5%~D
U9
EMC4022-1-EZK-TR_QFN32_5X5~D
VDDH
VDDL
VDD_PWRGD
R389 10K_0402_5%~D
DN1/THERM
DP1/VREF_T
DN2/DP4
DP2/DN4
DP3/DN5
DN3/DP5
C270 2200P_0402_50V7K~D
C271 2200P_0402_50V7K~D
REM_DIODE1_N_4022
REM_DIODE1_P_4022
VGA_THERMDN
VGA_THERMDP
REM_DIODE3_P_4022
REM_DIODE3_N_4022
VCP2
VCP
VIN
VSET
VSET_4022
<61> MAX8731_IINP
R387 4.7K_0402_5%~D
THERMTRIP2#
THERMTRIP3#
SYS_SHDN#
POWER_SW#
ACAVAIL_CLR
ATF_INT#/BC_IRQ#
ACAV_IN
BC_INT#_EMC4022
THERM_STP#
+RTC_CELL
@R390 47K_0402_1%~D
FAN_OUT
+FAN1_VOUT
SMCLK/BC_CLK
SMDATA/BC_DATA
BC_CLK_EMC4022
BC_DAT_EMC4022
TACH/GPIO1
GPIO2
GPIO3/PWM/THERMTRIP_SIO
PWM
R1178 10K_0402_5%~D
3V_PWROK#
<41> PCH_PWRGD#
R391 1K_0402_5%~D
RTC_PWR3V
C274 1U_0402_6.3V6K~D
VDD
ADDR_MODE/XEN
+VCC_4022
ADDR_XEN
R393 4.7K_0402_5%~D
TEST1
TEST2
VSS
R403 10K_0402_5%~D
R388 22_0402_5%~D
C273 0.1U_0402_16V4Z~D
C1176 1U_0402_6.3V6K~D
+1.05V_RUN_VTT
R395 8.2K_0402_5%~D
R398 2.2K_0402_5%~D
Q15 PMST3904_SOT323-3~D
C278 0.1U_0402_16V4Z~D
<7> H_THERMTRIP#
+3.3V_RUN_GFX
R1111 10K_0402_5%~D
R1112 2.2K_0402_5%~D
R405 8.2K_0402_5%~D
THERMB3
Q115 PMST3904_SOT323-3~D
C280 0.1U_0402_16V4Z~D
<47> THERMTRIP_VGA#
C282 0.1U_0402_16V4Z~D
R406 953_0402_1%~D
Rest=953, Tp=88degree
C281 0.1U_0402_16V4Z~D
U10 TC7SH08FU_SSOP5~D
POWER_SW#
DOCK_PWR_SW# <41>
POWER_SW_IN# <41>
DELL CONFIDENTIAL/PROPRIETARY
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
Compal Electronics, Inc.
Title
SCHEMATICS,MB A6561
Size
Document Number
401931
Rev B
Date: Thursday, January 13, 2011
Sheet 22 of 77

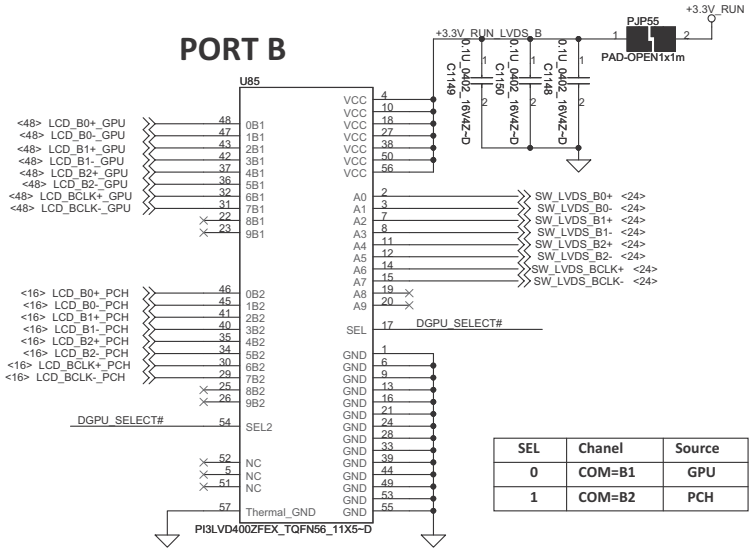
LVDS SW

PORT A

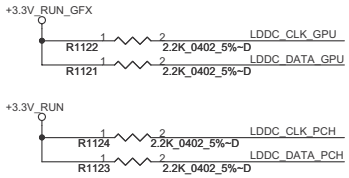


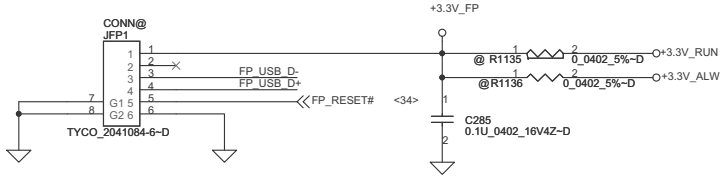
SEL	Chanel	Source
0	COM=B1	GPU
1	COM=B2	PCH

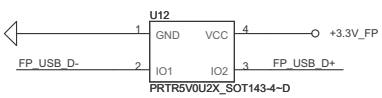
PORT B

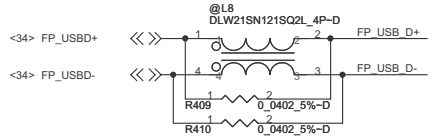


SEL	Chanel	Source
0	COM=B1	GPU
1	COM=B2	PCH









Fingerprint CONN.

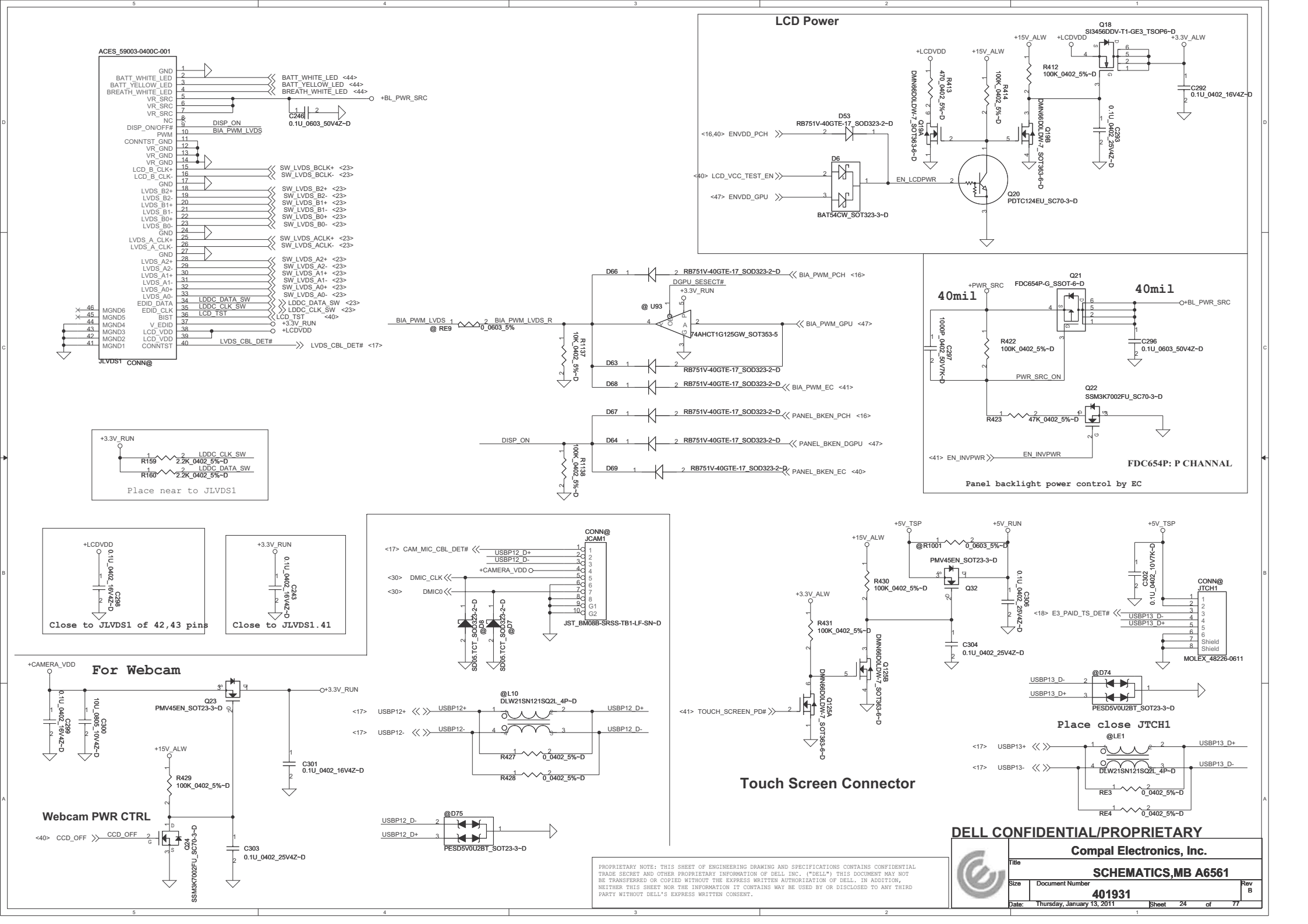
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 23 of 77



Compal Electronics, Inc.

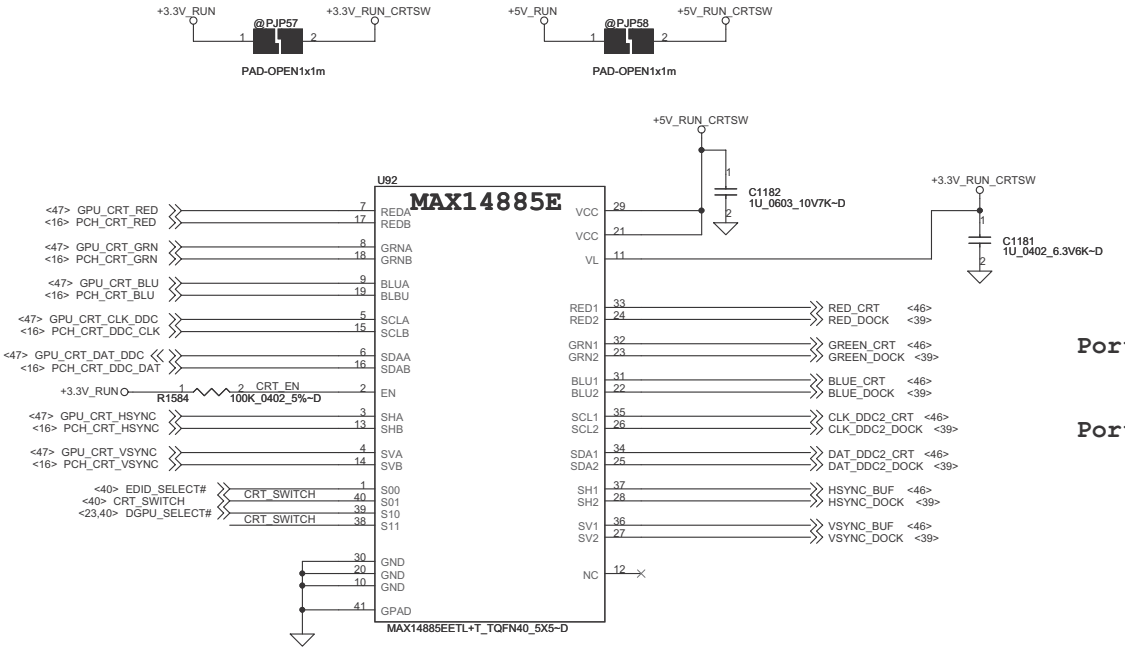
Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 24 of 77

Channel A --> GPU

Channel B --> PCH



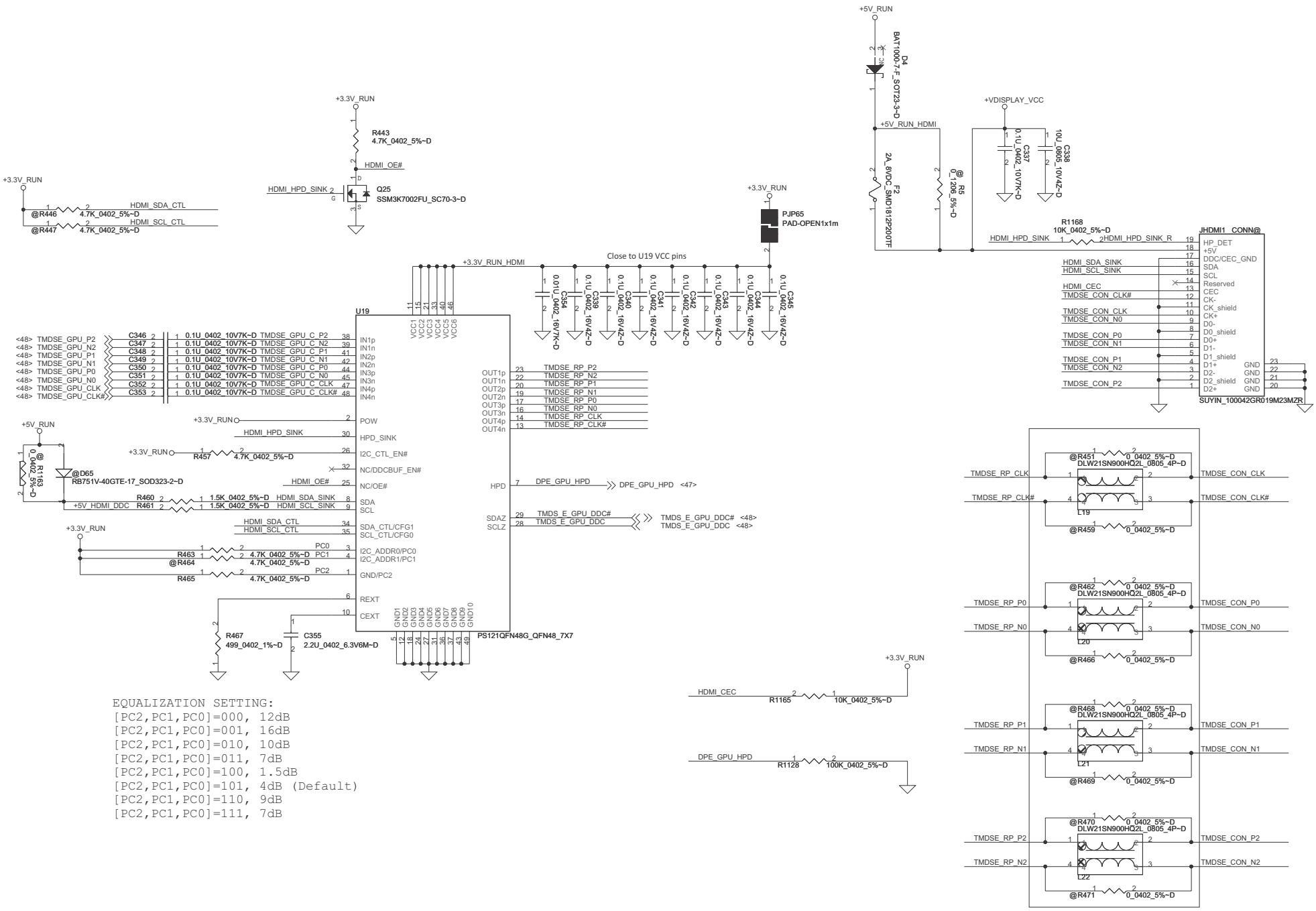
S01/S11	CRT_SWITCH	0	0	1	1
S10	DGPU_SELECT#	0	1	0	1
S00	EDID_SELECT#	0	1	0	1
		A --> Port 1	B --> Port 1	A --> Port 2	B --> Port 2

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 25 of 77



EQUALIZATION SETTING:
[PC2,PC1,PC0]=000, 12dB
[PC2,PC1,PC0]=001, 16dB
[PC2,PC1,PC0]=010, 10dB
[PC2,PC1,PC0]=011, 7dB
[PC2,PC1,PC0]=100, 1.5dB
[PC2,PC1,PC0]=101, 4dB (Default)
[PC2,PC1,PC0]=110, 9dB
[PC2,PC1,PC0]=111, 7dB

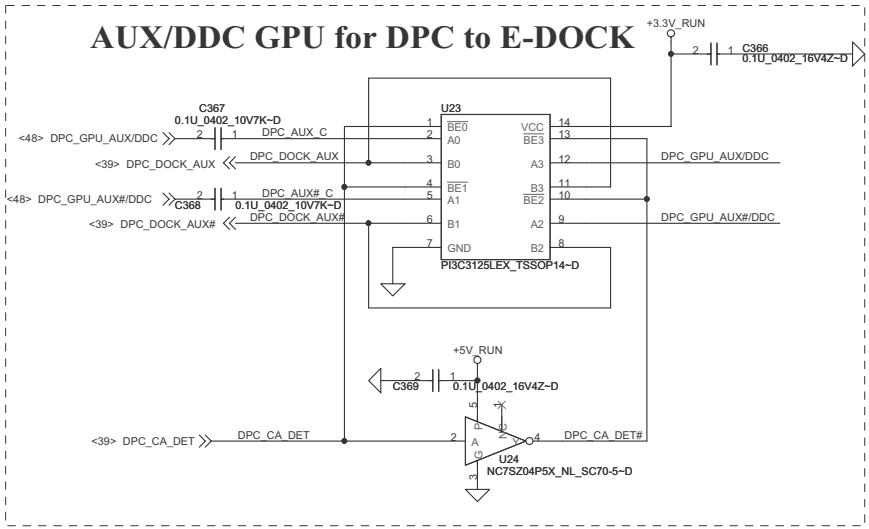
DELL CONFIDENTIAL/PROPRIETARY

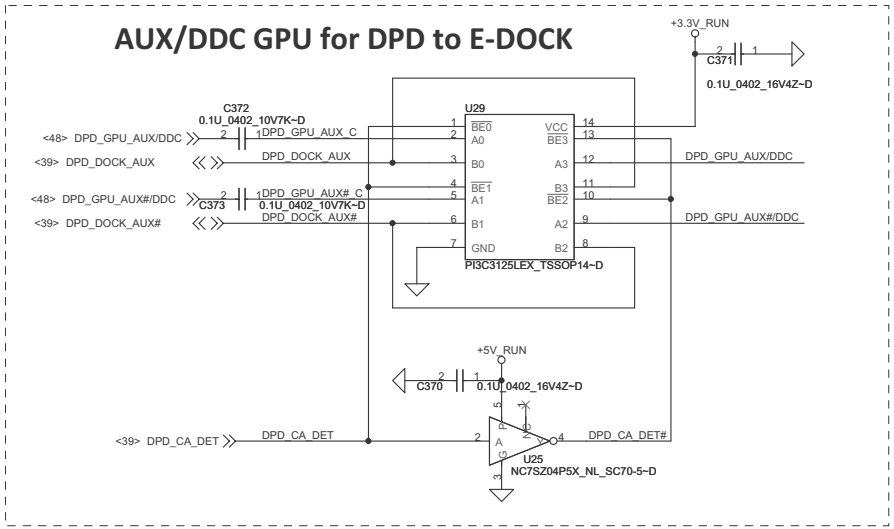
Compal Electronics, Inc.

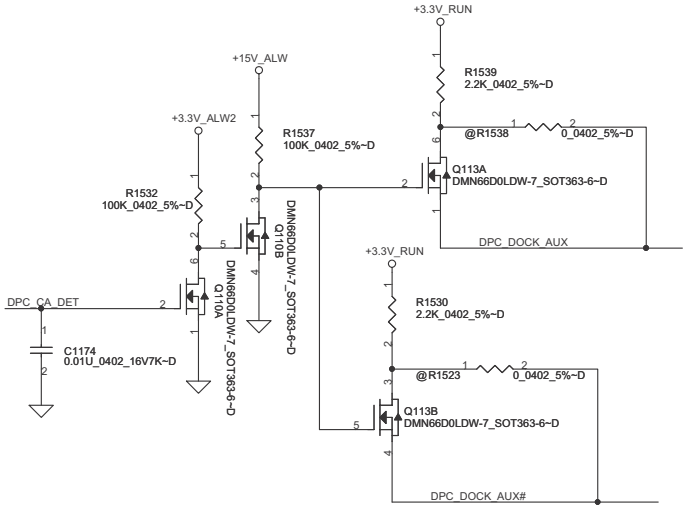
Title: SCHEMATICS,MB A6561

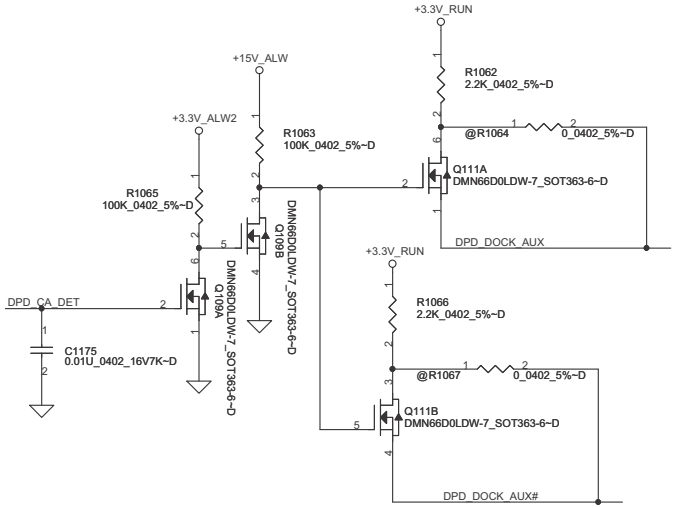
Size: | Document Number: 401931 | Rev: B

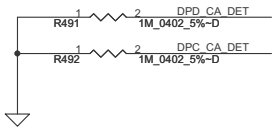
Date: Thursday, January 13, 2011 | Sheet 26 of 77











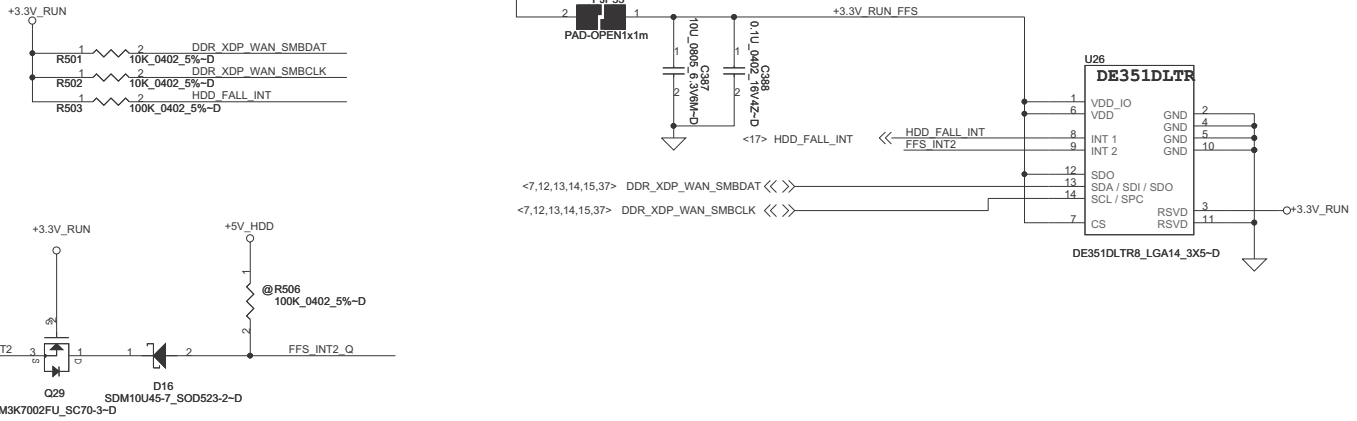
Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

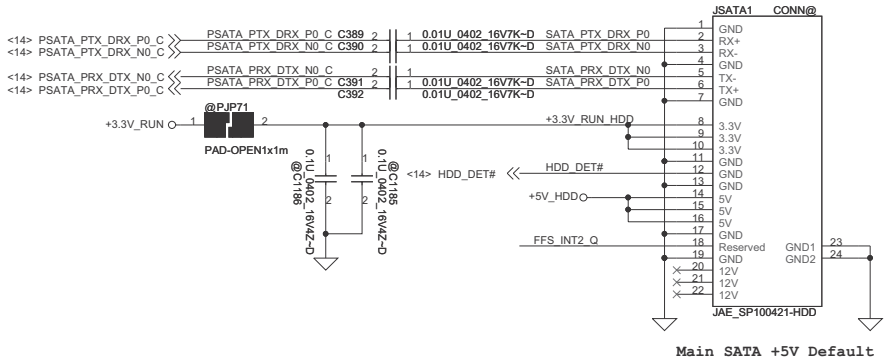
Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 27 of 77

Free Fall Sensor

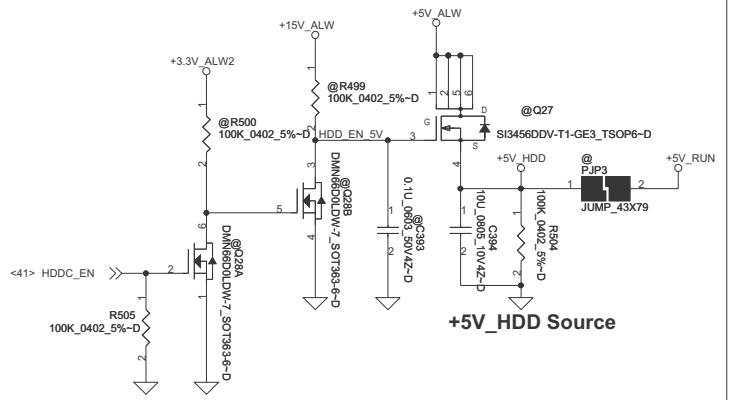


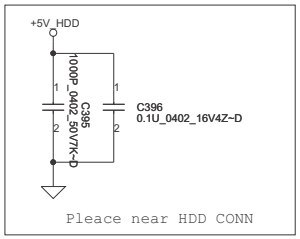
For HDD Temp.



Main SATA +5V Default

HDD PWR

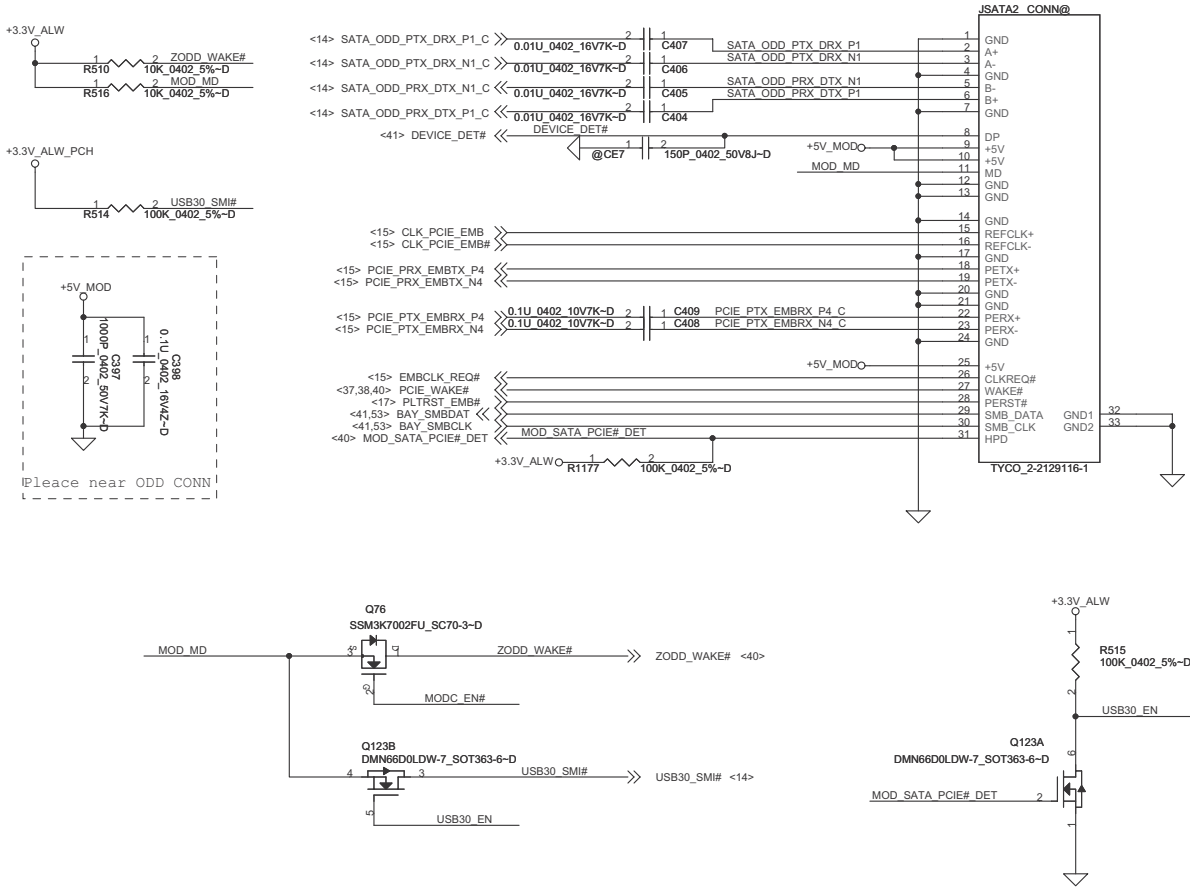


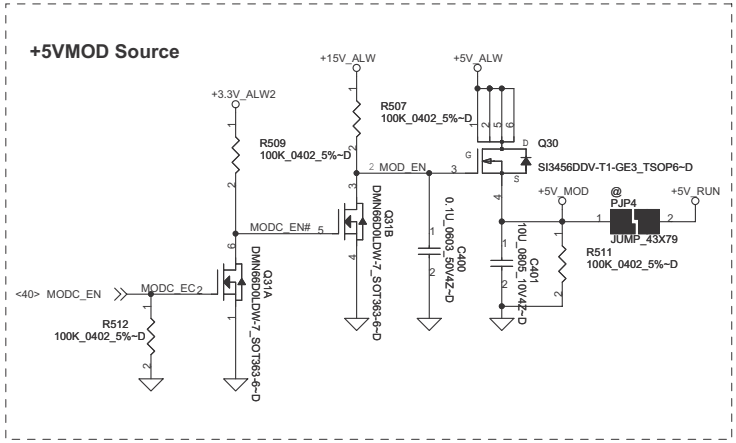


DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	SCHEMATICS,MB A6561
Size	Document Number 401931 Rev B
Date: Thursday, January 13, 2011	Sheet 28 of 77

For ODD





DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	SCHEMATICS,MB A6561
Size	Document Number: 401931 — Rev: B
Date: Thursday, January 13, 2011	Sheet 29 of 77

Internal Speakers Header

DVDD_IO should match with HDA Bus level

15 mils trace

INT_SPK_L+ L91 BLM18BD121SN1D_2P~D INT_SPKL_L+
INT_SPK_L- L92 BLM18BD121SN1D_2P~D INT_SPKR_L-
INT_SPK_R+ L93 BLM18BD121SN1D_2P~D INT_SPKR_R+
INT_SPK_R- L94 BLM18BD121SN1D_2P~D INT_SPKR_R-

JSPK1 CONN@ (GND GND) TYCO_2-1775765-4

@DE2 PESD5V0U2BT_SOT23-3-D
@DE1 PESD5V0U2BT_SOT23-3-D

+3.3V_RUN_DVDD

C984 0.1U_0402_16V4Z~D
C982 1U_0603_10V6K~D
C983 0.1U_0402_16V4Z~D
C954 10U_0805_10V6K~D

Place C994, C952~C957 close to Codec

U72 92HD90B2X5NLGXYAX8_QFN48_7X7~D

DVDD_CORE
DVDD_IO
DVDD
BITCLK
SDATA_OUT
SYNC
SDATA_IN
RESET#
I2S_MCLK
I2S_SCLK
I2S_DOUT
I2S_LRCLK
I2S_DIN
No Connect
No Connect
EAPD
DVSS
PVSS
GND
AVDD1
AVDD2
PVDD
PVDD
SENSE_A
SENSE_B
PORTA_L
PORTA_R
VrefOut_A
PORTB_L
PORTB_R
PORTD_+L
PORTD_-L
PORTD_+R
PORTD_-R
MONO_OUT
PC_BEEP
DMIC_CLK/GPIO 1
DMIC_0/GPIO 2
DMIC1/GPIO0/SPDIFOUT1
SPDIFOUT0//GPIO3/Aux_Out
CAP+
CAP-
VREFFILT
CAP2
V-
Vreg
AVSS1
AVSS
AVSS

<14> PCH_AZ_CODEC_BITCLK — PCH_AZ_CODEC_BITCLK
<14> PCH_AZ_CODEC_SDOUT — PCH_AZ_CODEC_SDOUT
<14> PCH_AZ_CODEC_SYNC — Place R1096 close to codec
<14> PCH_AZ_CODEC_SDIN0 — R1096 33_0402_5%~D — PCH_AZ_SDIN0_R
<14> PCH_AZ_CODEC_RST# — PCH_AZ_CODEC_RST#

I2S_MCLK — RE13 0_0402_5%~D — I2S_MCLK_R
I2S_BCLK — RE10 0_0402_5%~D — I2S_BCLK_R
I2S_DO — R1097 33_0402_5%~D
I2S_LRCLK
I2S_DI#
Place R1097 close to codec

<40> AUD_NB_MUTE# — +3.3V_RUN — R1099 10K_0402_5%~D

+VDDA_AVDD — C955 10U_0805_10V6K~D; C956 1U_0603_10V6K~D; C957 0.1U_0402_16V4Z~D
place close to pin27 — place close to pin38
L77 BLM21PG600SN1D_0805~D — +5V_RUN
C1172 1U_0603_10V6K~D; C1173 0.1U_0402_16V4Z~D
+5V_RUN — R1095 0_0805_5%~D
+VREFOUT_R — C1180 1U_0603_10V6K~D

+VDDA_PVDD
C958 10U_0805_10V6K~D; C959 0.1U_0402_16V4Z~D; C960 10U_0805_10V6K~D; C961 0.1U_0402_16V4Z~D

AUD_SENSE_A
AUD_SENSE_B

MIC_IN_L — C1163 1U_0402_6.3V6K~D — MIC_IN_R <46>
+VREFOUT — +VREFOUT_R
AUD_HP_OUT_L — R1143 2.2K_0402_5%~D — AUD_HP_OUT_L <46>
AUD_HP_OUT_R — AUD_HP_OUT_R <46>

MIC_IN_L and MIC_IN_RR must symmetric in layout
R161 pop 0-ohm for Combo Jack, pop 1UF for E2 backup circuit
MIC_IN_RR — R161 0_0402_5%~D — MIC_IN_R
+VREFOUT_R — D70 RB751V-40GTE-17_SOD323-2~D

INT_SPK_L+
INT_SPK_L-
INT_SPK_R+
INT_SPK_R-

AUD_PC_BEEP — C1105 0.1U_0402_16V4Z~D — SPKR_R — R1119 100K_0402_5%~D — SPKR <14>
C1106 0.1U_0402_16V4Z~D — BEEP_R — R1120 100K_0402_5%~D — BEEP <41>

DMIC_CLK_L — LE2 BLM18BB221SN1D_2P~D — DMIC_CLK <24> DMIC0 <24>

@R1141 10K_0402_5%~D
@R1142 10K_0402_5%~D

680P_0402_50V7K~D: C973, C974, C975, C976

Place C962 close to Codec
C962 4.7U_0603_10V6K~D

Place C963~C966 close to Codec
C963 4.7U_0603_10V6K~D; C964 4.7U_0603_10V6K~D; C965 1U_0603_10V6K~D; C966 10U_0805_10V6K~D

+3.3V_RUN — @PJP60 — +3.3V_RUN_DVDD
PAD-OPEN1x1m

Close to U72 pin5
PCH_AZ_CODEC_SDOUT — @R1077 47_0402_5%~D — @C978 0.1U_0402_10V7K~D

Close to U72 pin6
PCH_AZ_CODEC_BITCLK — @R1076 10_0402_5%~D — @C977 10P_0402_50V8J~D

BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

Place closely to Pin 13.

+VDDA_AVDD — R1083 2.49K_0402_1%~D — AUD_SENSE_A
+3.3V_RUN — @R352 39.2K_0402_1%~D — @R1088 100K_0402_5%~D
R1086 20K_0402_1%~D — C980 100P_0402_50V7K~D
+3.3V_RUN — R1087 100K_0402_5%~D
<46> AUD_MIC_SWITCH — Q107A DMN66D0LDW-7_SOT363-6~D — Q107B DMN66D0LDW-7_SOT363-6~D — AUD_HP_NB_SENSE <40,46>
@C967 0.1U_0402_16V4Z~D

Add for solve pop noise and detect issue

place at AGND and DGND plane
@C981 100P_0402_50V8J~D
@C982 100P_0402_50V8J~D
@C983 100P_0402_50V8J~D

place at Codec bottom side
@PJP62
PAD-OPEN1x1m

Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Dock Audio
PORT D	Internal SPK

Place closely to Pin 14

+VDDA_AVDD — R1078 2.49K_0402_1%~D — AUD_SENSE_B
+3.3V_RUN — R1079 39.2K_0402_1%~D — R1081 100K_0402_5%~D
R1080 20K_0402_1%~D — C979 100P_0402_50V7K~D
+3.3V_RUN — R1082 100K_0402_5%~D
<40> DOCK_HP_DET — Q106A DMN66D0LDW-7_SOT363-6~D — Q106B DMN66D0LDW-7_SOT363-6~D — DOCK_MIC_DET <40>

+3.3V_RUN — C1103 0.1U_0402_10V7K~D

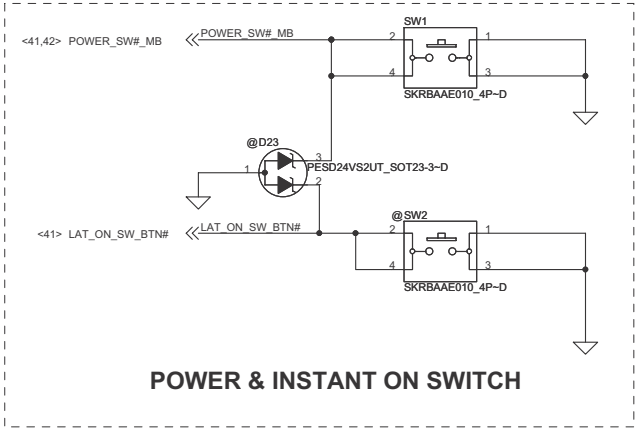
U73 CD74HC366M96_SO16~D

I2S_BCLK — 1A — 1Y# — @D54 DA204U_SOT323-3~D — DAI_BCLK# <39>
I2S_LRCLK — 2A — 2Y# — @D55 DA204U_SOT323-3~D — DAI_LRCK# <39>
I2S_DO — 3A — 3Y# — @D56 DA204U_SOT323-3~D — DAI_DO# <39>
I2S_MCLK — 4A — 4Y# — @D57 DA204U_SOT323-3~D — DAI_12MHZ# <39>
5A — 5Y#
I2S_DI# — 6A — 6Y#
<40> EN_I2S_NB_CODEC# — OE1# — OE2# — GND
R1540 1K_0402_5%~D

+3.3V_RUN — @D58 DA204U_SOT323-3~D — DAI_DI <39>

DELL CONFIDENTIAL/PROPRIETARY

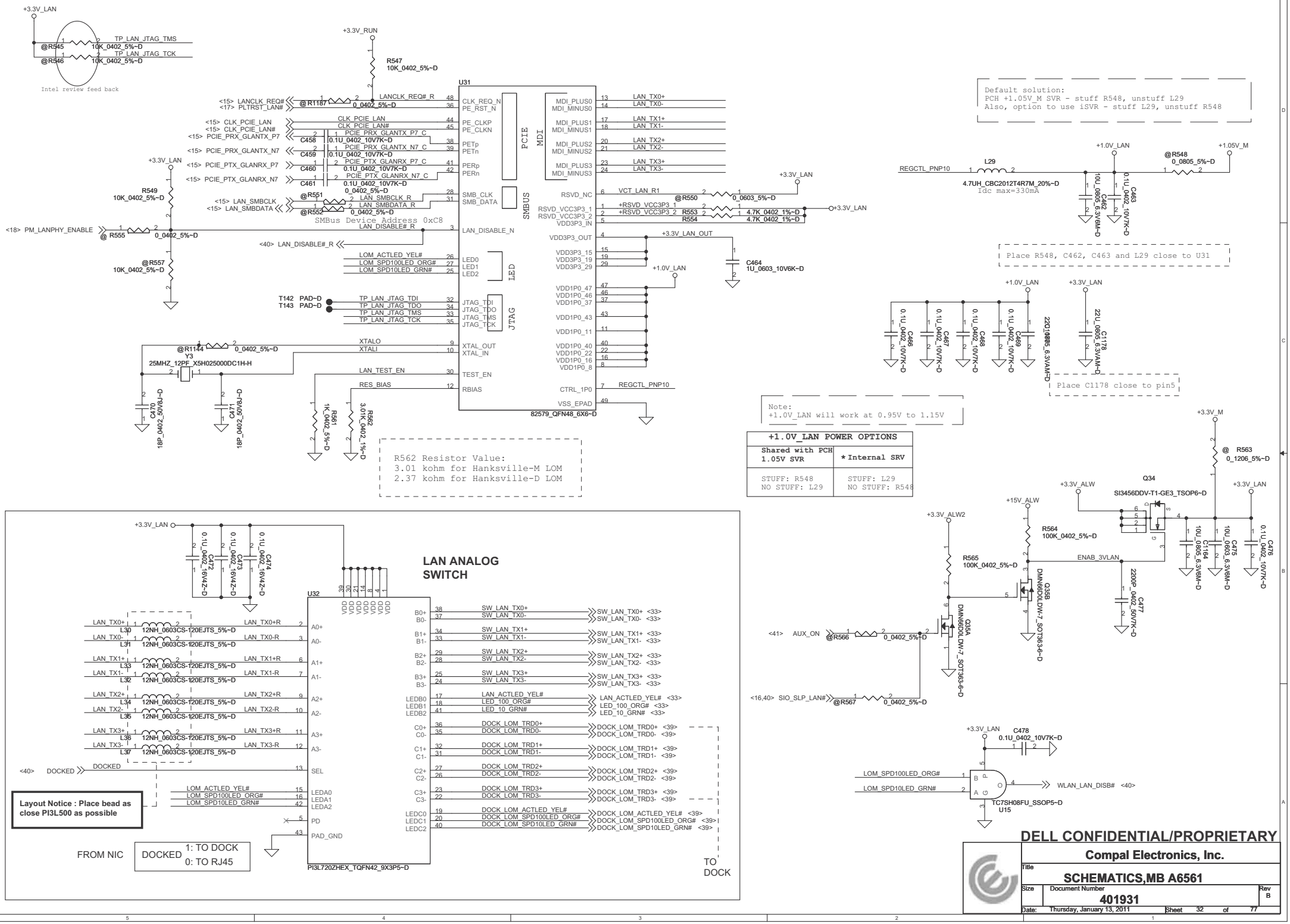
Compal Electronics, Inc.
Title: SCHEMATICS,MB A6561
Size: Document Number: 401931 Rev: B
Date: Thursday, January 13, 2011 Sheet 30 of 77



POWER & INSTANT ON SWITCH

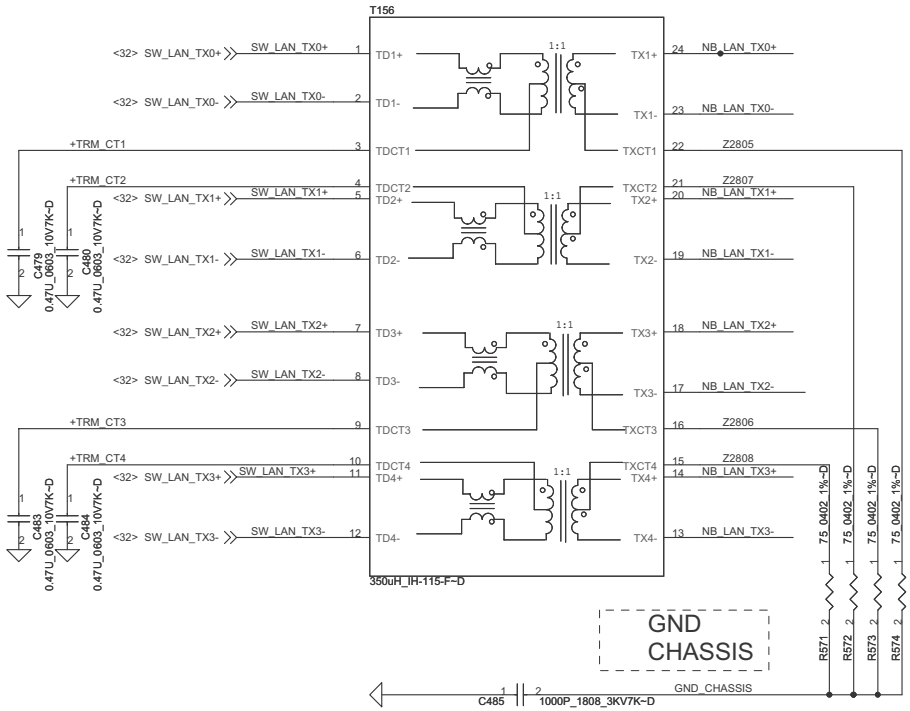
DELL CONFIDENTIAL/PROPRIETARY

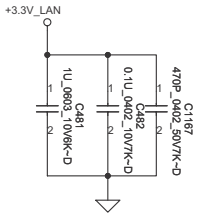
Compal Electronics, Inc.	
Title	SCHEMATICS,MB A6561
Size	Document Number: 401931 — Rev: B
Date: Thursday, January 13, 2011	Sheet 31 of 77



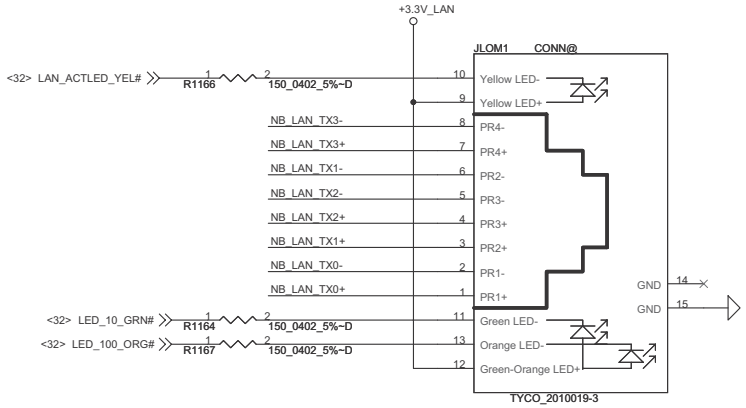
DELL CONFIDENTIAL/PROPRIETARY

	Compal Electronics, Inc.	
	Title: SCHEMATICS,MB A6561	
Size	Document Number: 401931	Rev: B
Date: Thursday, January 13, 2011	Sheet 32 of 77	





+3.3V_LAN:20mils

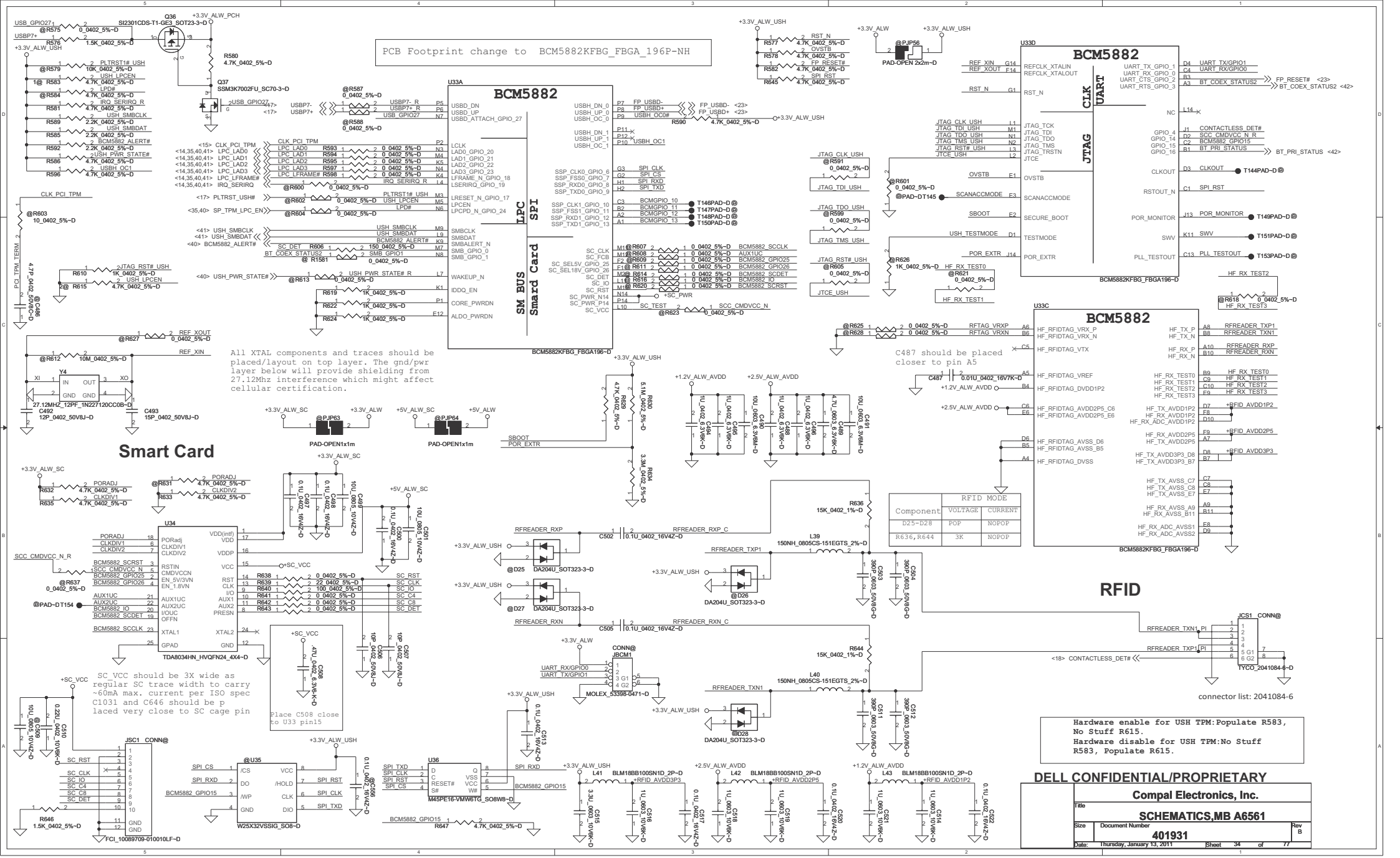


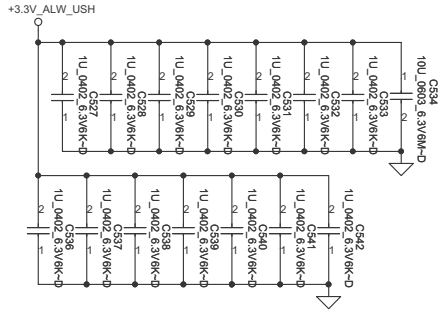
Compal Electronics, Inc.

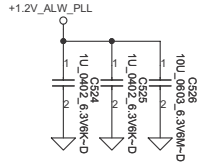
Title: SCHEMATICS,MB A6561

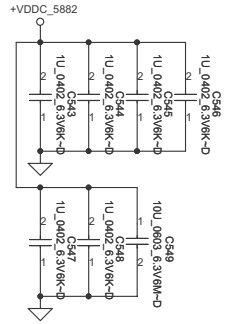
Size | Document Number: 401931 | Rev: B

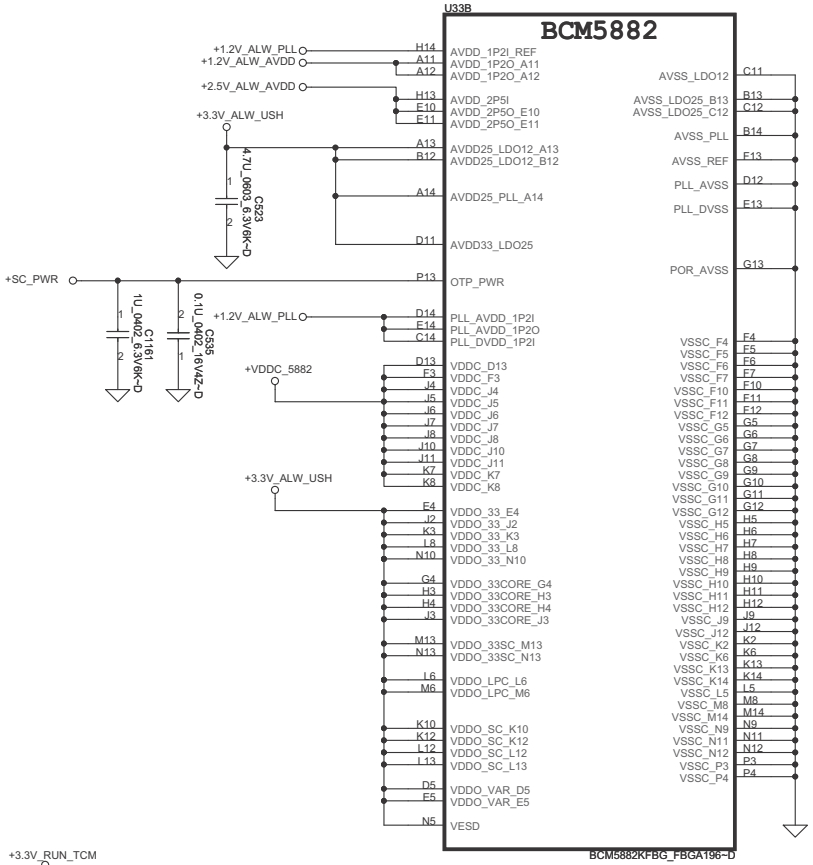
Date: Thursday, January 13, 2011 | Sheet 33 of 77


PCB Footprint change to BCM5882KFBG_FBGA_196P-NH
BCM5882
BCM5882KFBG_FBGA196-D
BCM5882KFBG_FBGA196~D
U33A
U33C
U33D
LPC
SPI
SM BUS
Smard Card
CLK
UART
JTAG
Smart Card
RFID
All XTAL components and traces should be placed/layout on top layer. The gnd/pwr layer below will provide shielding from 27.12Mhz interference which might affect cellular certification.
C487 should be placed closer to pin A5
SC_VCC should be 3X wide as regular SC trace width to carry ~60mA max. current per ISO spec C1031 and C646 should be p laced very close to SC cage pin
Place C508 close to U33 pin15
Hardware enable for USH TPM:Populate R583, No Stuff R615.
Hardware disable for USH TPM:No Stuff R583, Populate R615.
RFID MODE
Component | VOLTAGE | CURRENT
D25-D28 | POP | NOPOP
R636,R644 | 3K | NOPOP
TDA8034HN_HVQFN24_4X4~D
W25X32VSSIG_SO8~D
M45PE16-VMW6TG_SO8W8~D
FCI_10089709-010010LF~D
TYCO_2041084-6~D
MOLEX_53398-0471~D
connector list: 2041084-6
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
SCHEMATICS,MB A6561
401931
Rev B
Thursday, January 13, 2011
Sheet 34 of 77



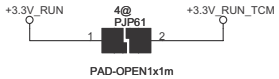


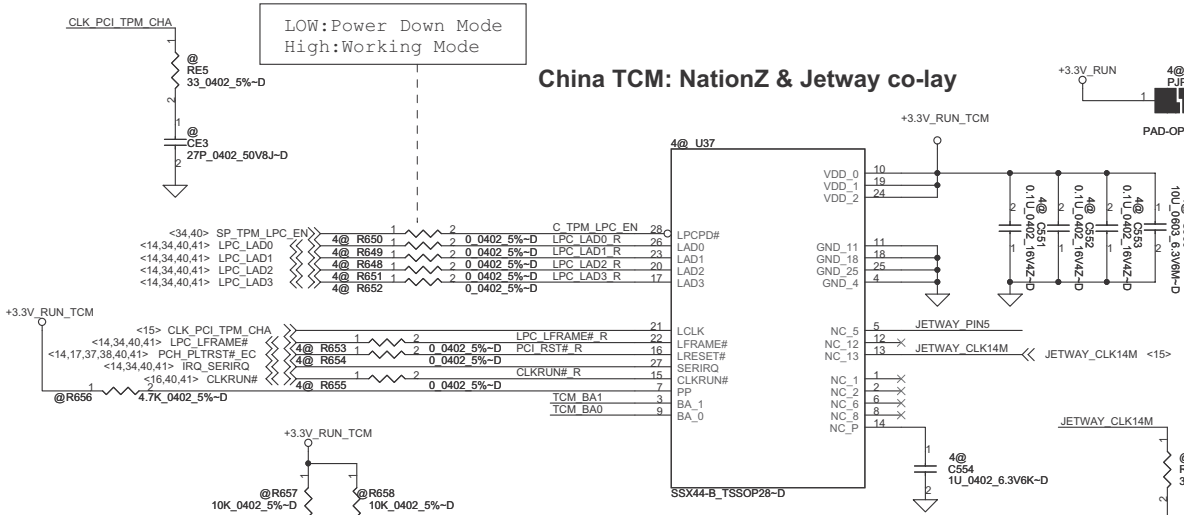




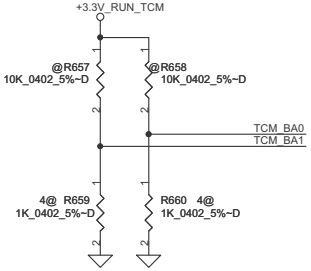
LOW:Power Down Mode
High:Working Mode

China TCM: NationZ & Jetway co-lay

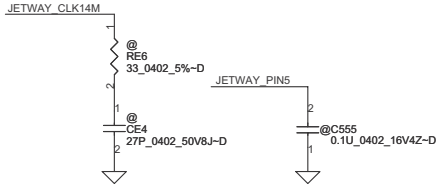




USH BCM5882 and China TCM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 4@	POP	@	@
USH_LPCEN	PU R583	@	POP	@
	PD R615	POP	@	@
SIO 5028 ->SP_TPM_LPC_EN	PU R772	@	@	@
PCH GPIO39 ->TPM_ID1	PU RH268	@	POP	POP
	PD RH271	POP	@	@
PCH GPIO38 ->TPM_ID0	PU RH267	@	POP	@
	PD RH270	POP	@	POP



TCM Vender	POP
NationZ	R660, R659, C554, C550
Jetway	C555, RH315



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

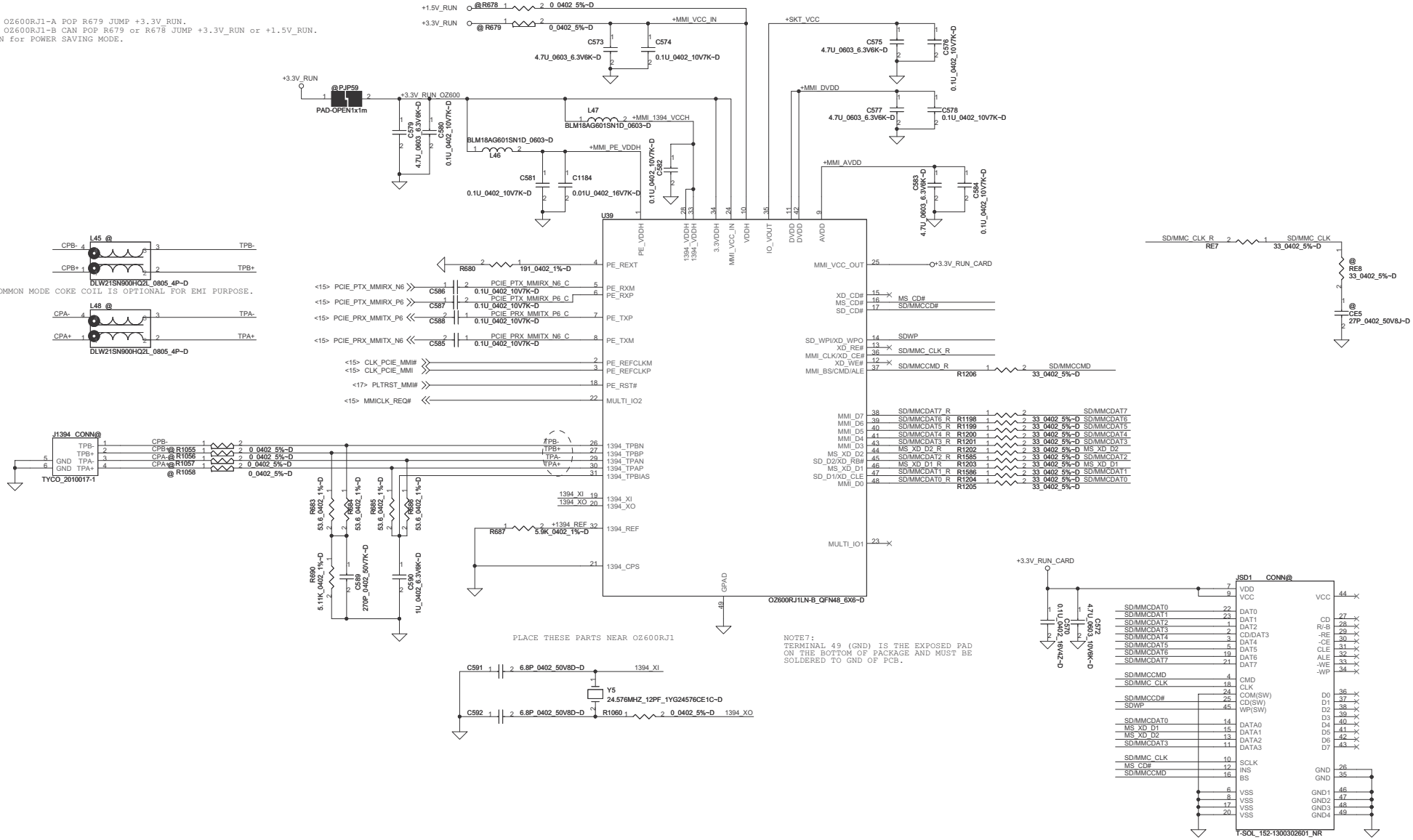
Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 35 of 77

NOTE1:
THESE 1394 SIGNALS ARE HIGH SPEED
DIFFERENTIAL PAIRS AND MUST BE KEPT EQUAL
LENGTH WITH A DIFFERENTIAL IMPEDANCE (Z0)
OF 110 OHMS.

NOTE2:
If used OZ600RJ1-A R680 need change to 5.1K ohm_1%.
If used OZ600RJ1-B R680 need change to 191 ohm _1%.

NOTE3:
If used OZ600RJ1-A POP R679 JUMP +3.3V_RUN.
If used OZ600RJ1-B CAN POP R679 or R678 JUMP +3.3V_RUN or +1.5V_RUN.
1.5V_RUN for POWER SAVING MODE.



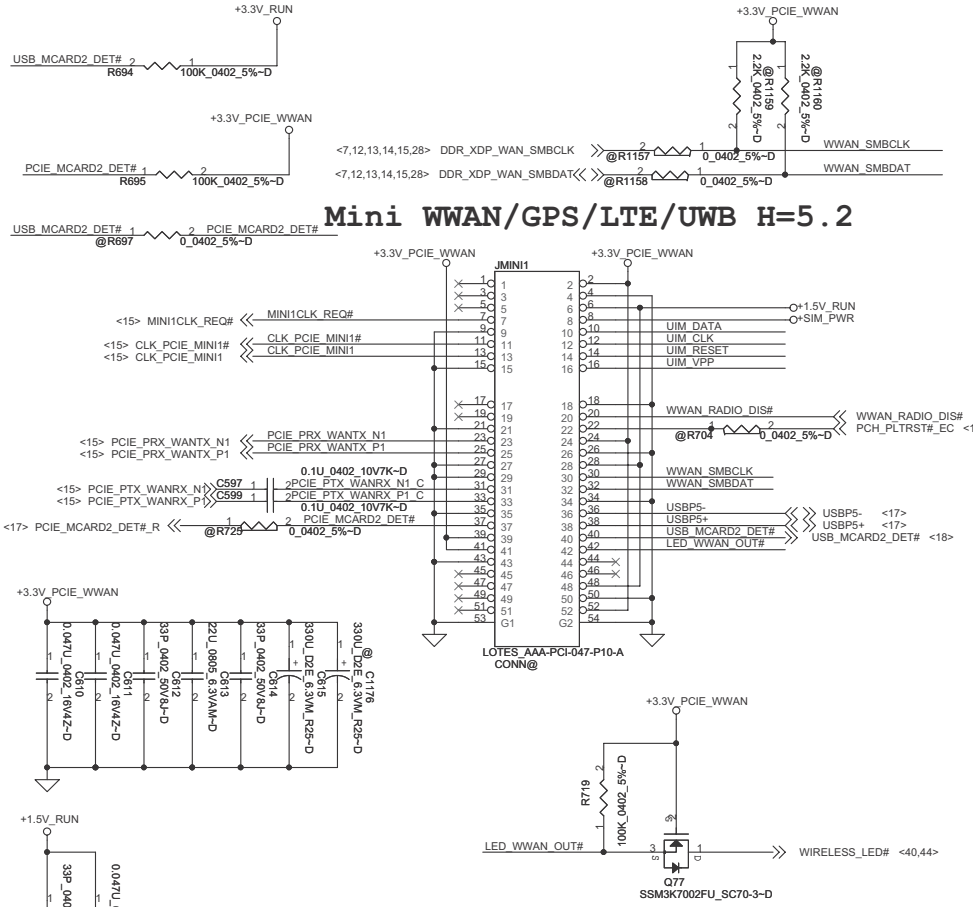
Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

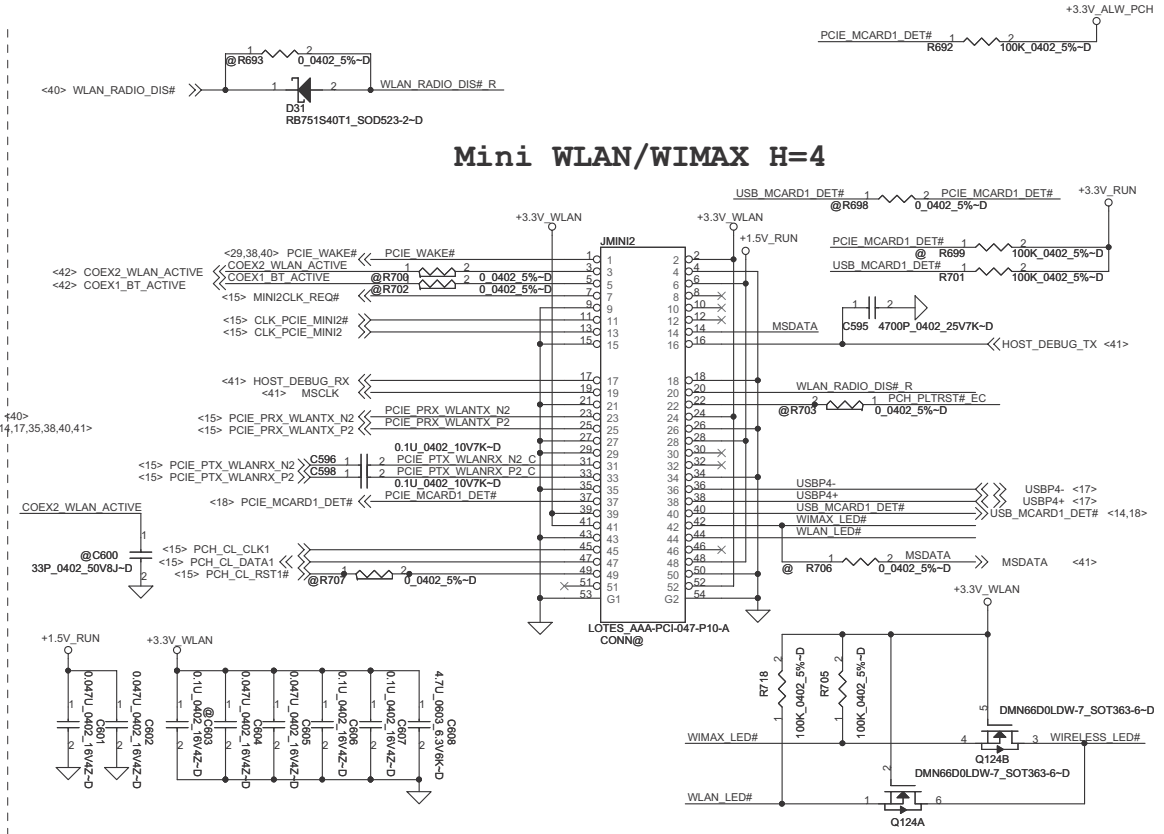
Size: Document Number: 401931 Rev: B

Date: Thursday, January 13, 2011 Sheet 36 of 77

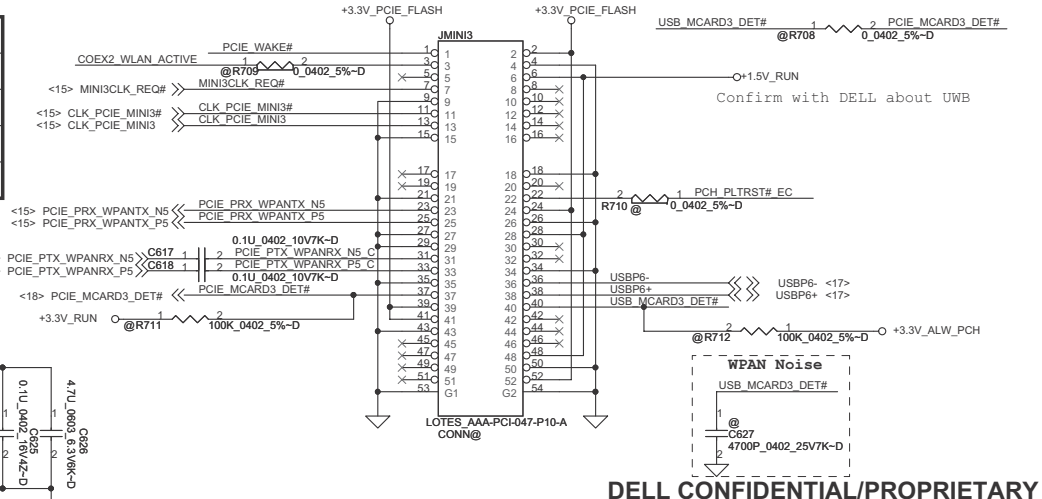
Mini WWAN/GPS/LTE/UWB H=5.2



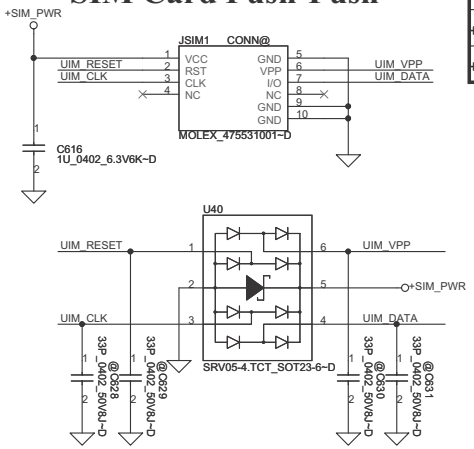
Mini WLAN/WIMAX H=4



1/2 Minicard Flash Card H=4



SIM Card Push-Push



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA

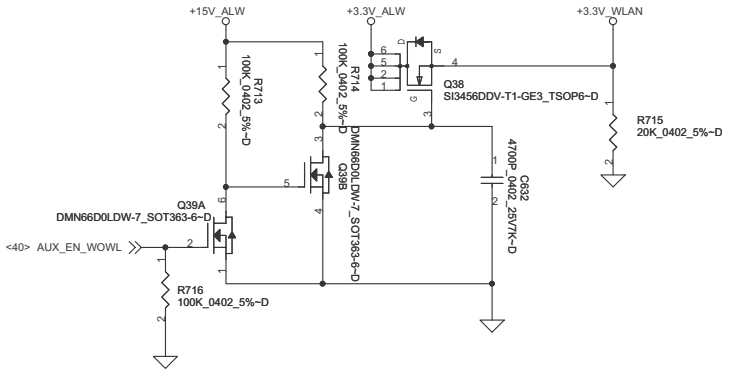
Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

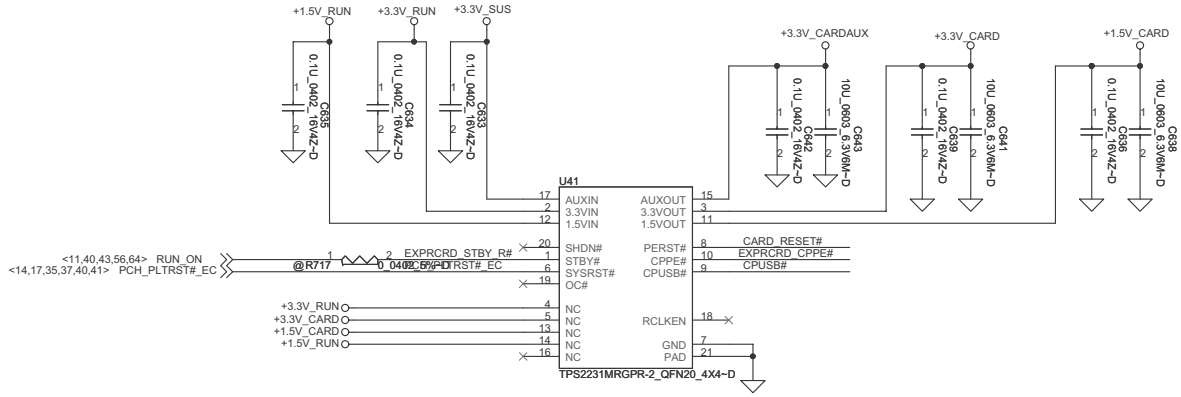
Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 37 of 77

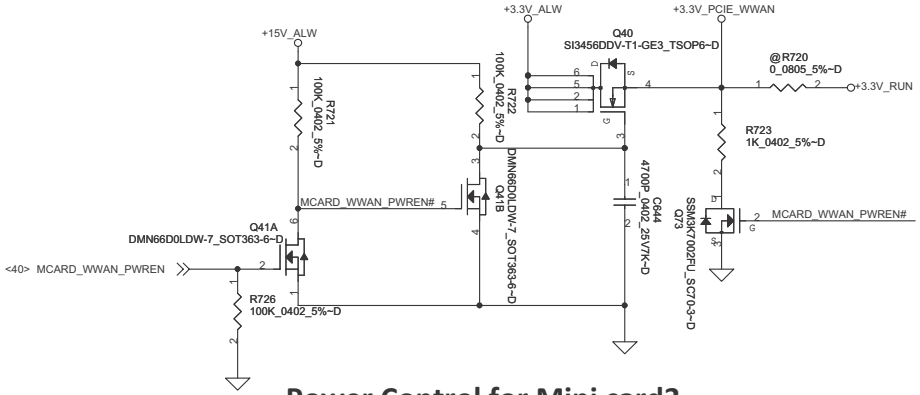
Power Control for Mini card1



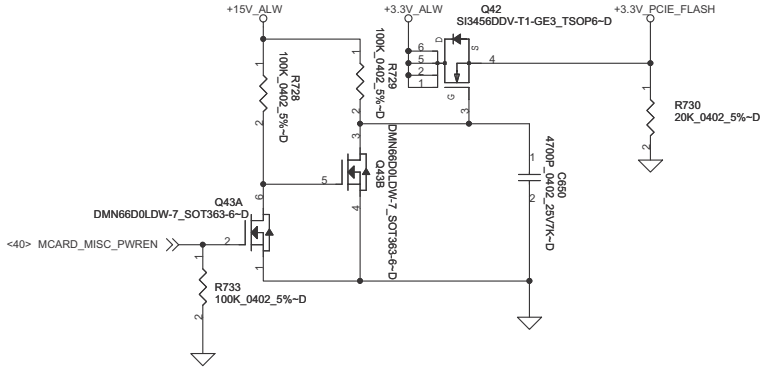
Express Card PWR S/W



Power Control for Mini card2

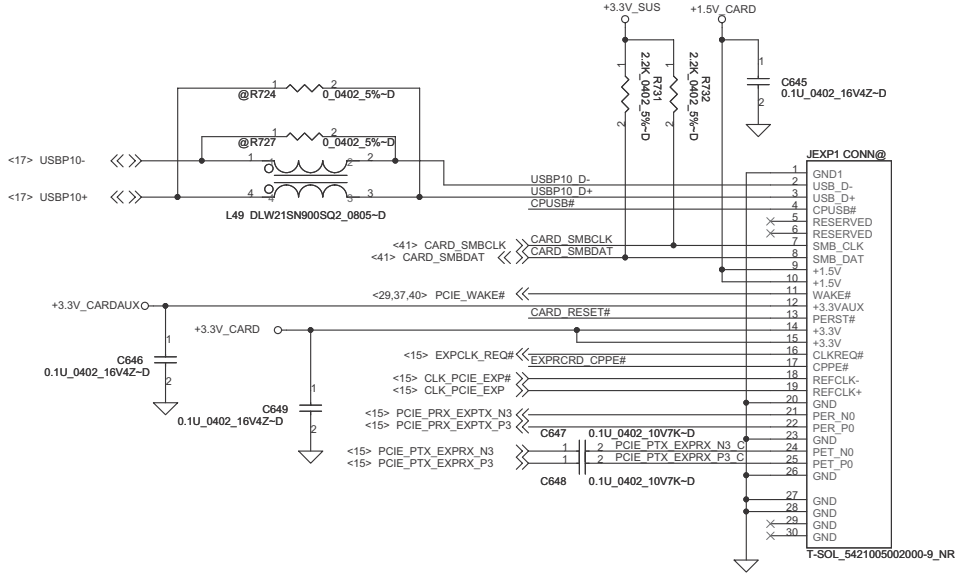


Power Control for Mini card3



Express Card BTB Conn.

+1.5V_CARD: Max. 650mA, Average 500mA
+3.3V_CARD: Max. 1300mA, Average 1000mA

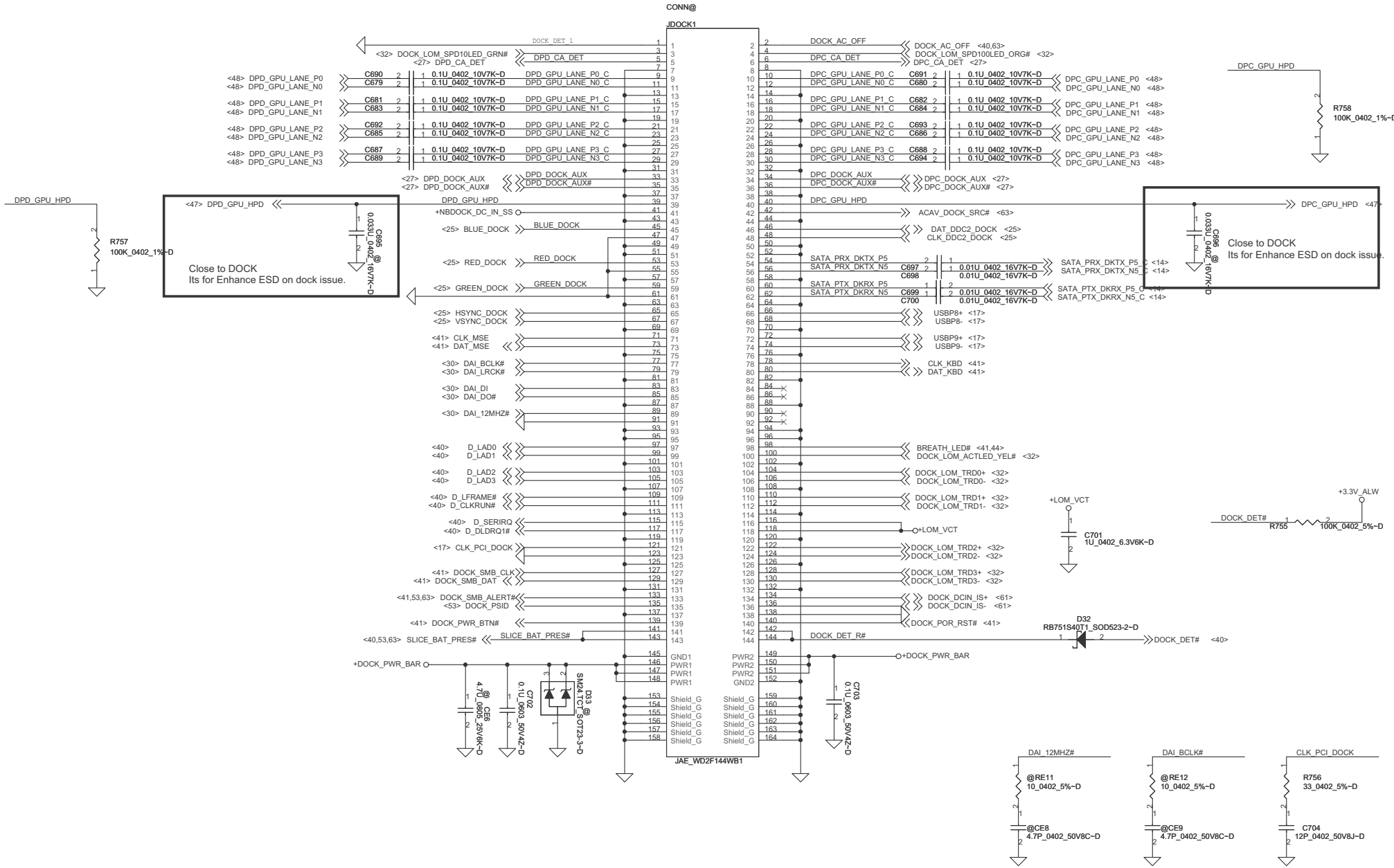


Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 38 of 77

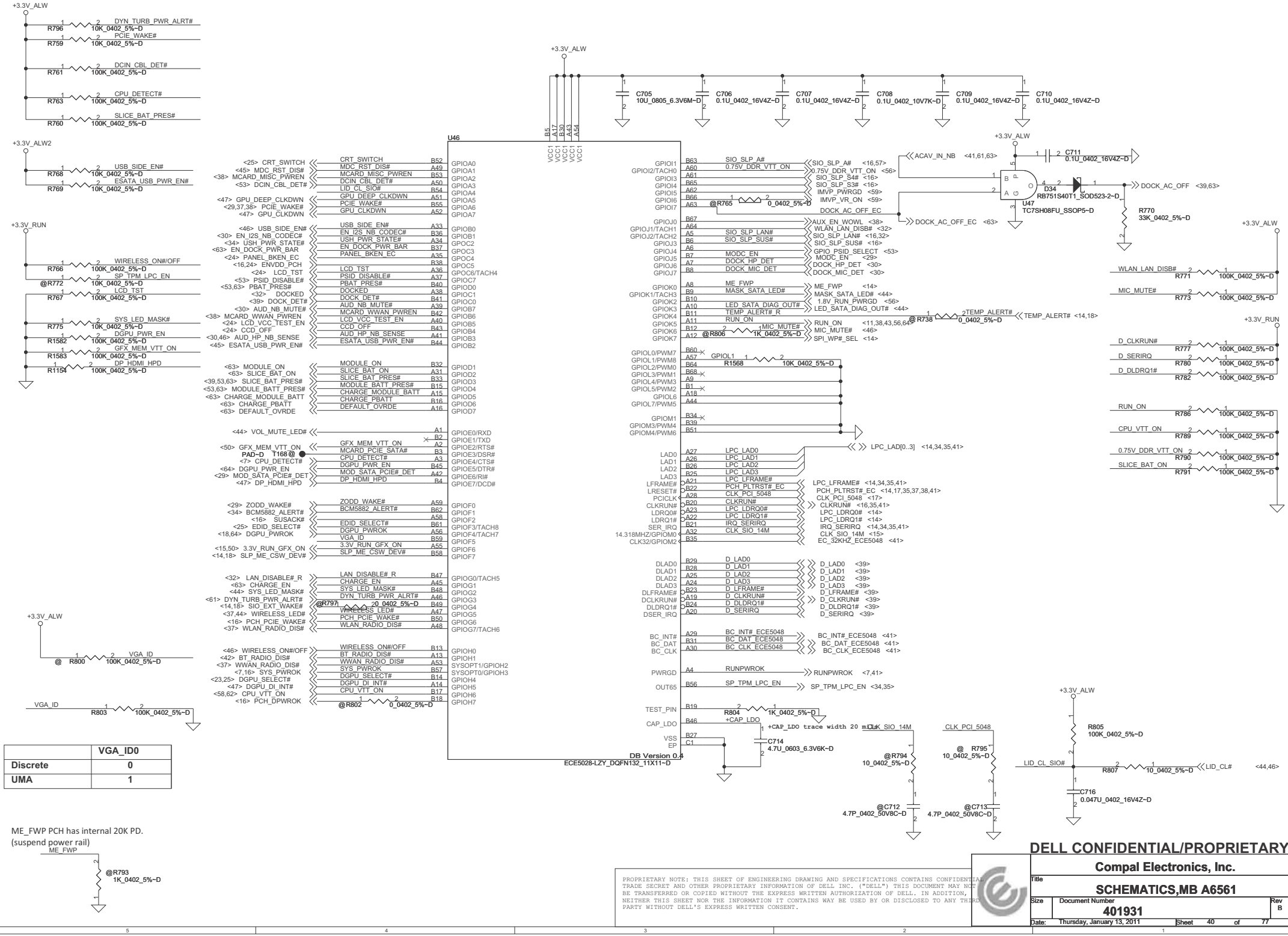


Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 39 of 77



	VGA_ID0
Discrete	0
UMA	1

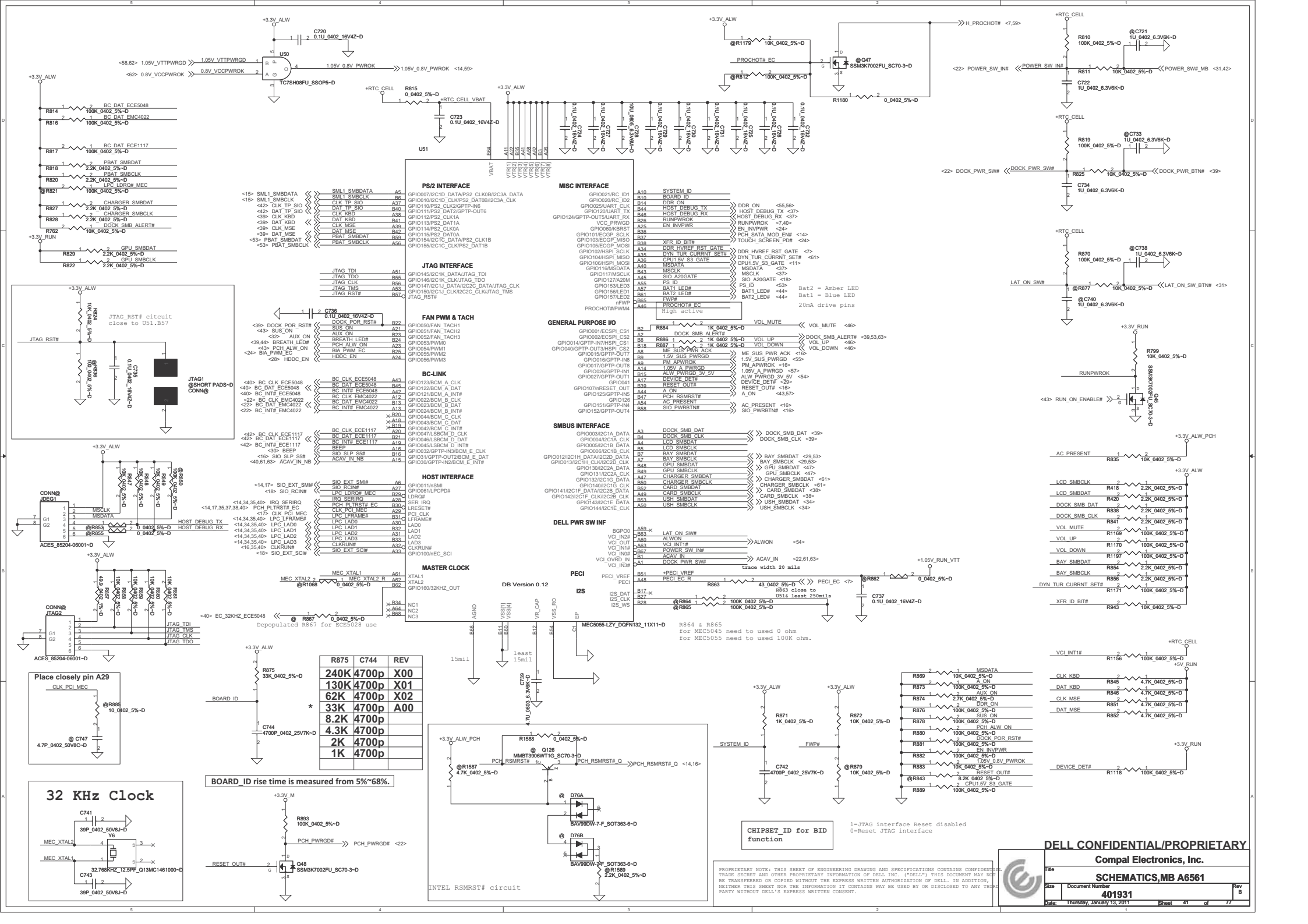
ME_FWP PCH has internal 20K PD.
(suspend power rail)

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

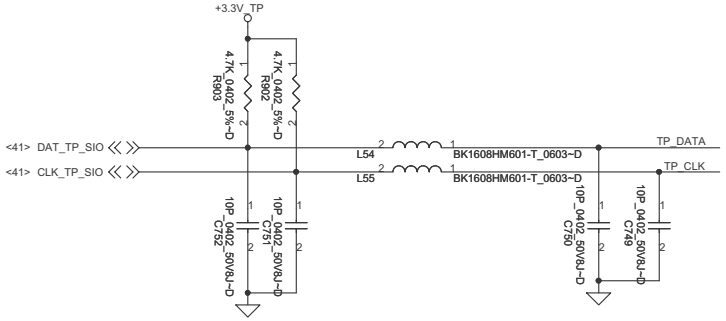
Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 40 of 77

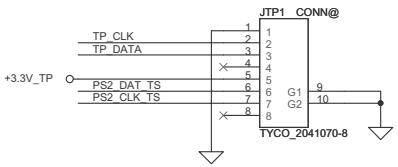


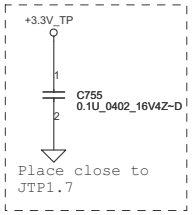
R875	C744	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	A00
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

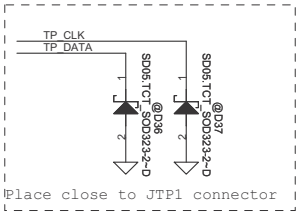
Touch Pad



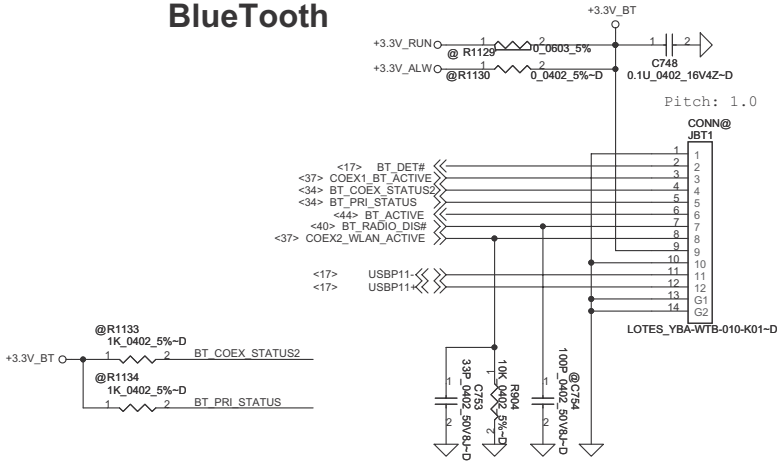
Pitch: 0.5



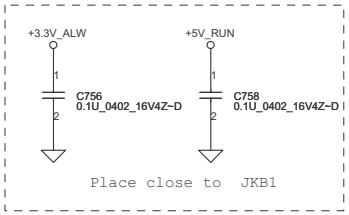




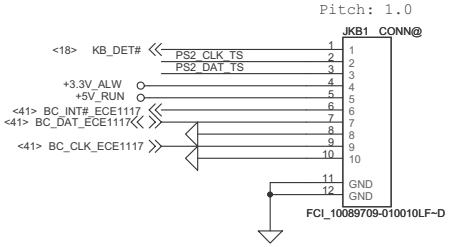
BlueTooth



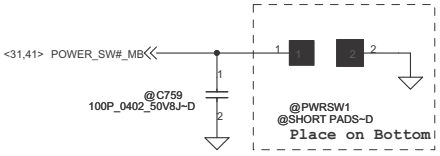
Keyboard



Pitch: 1.0

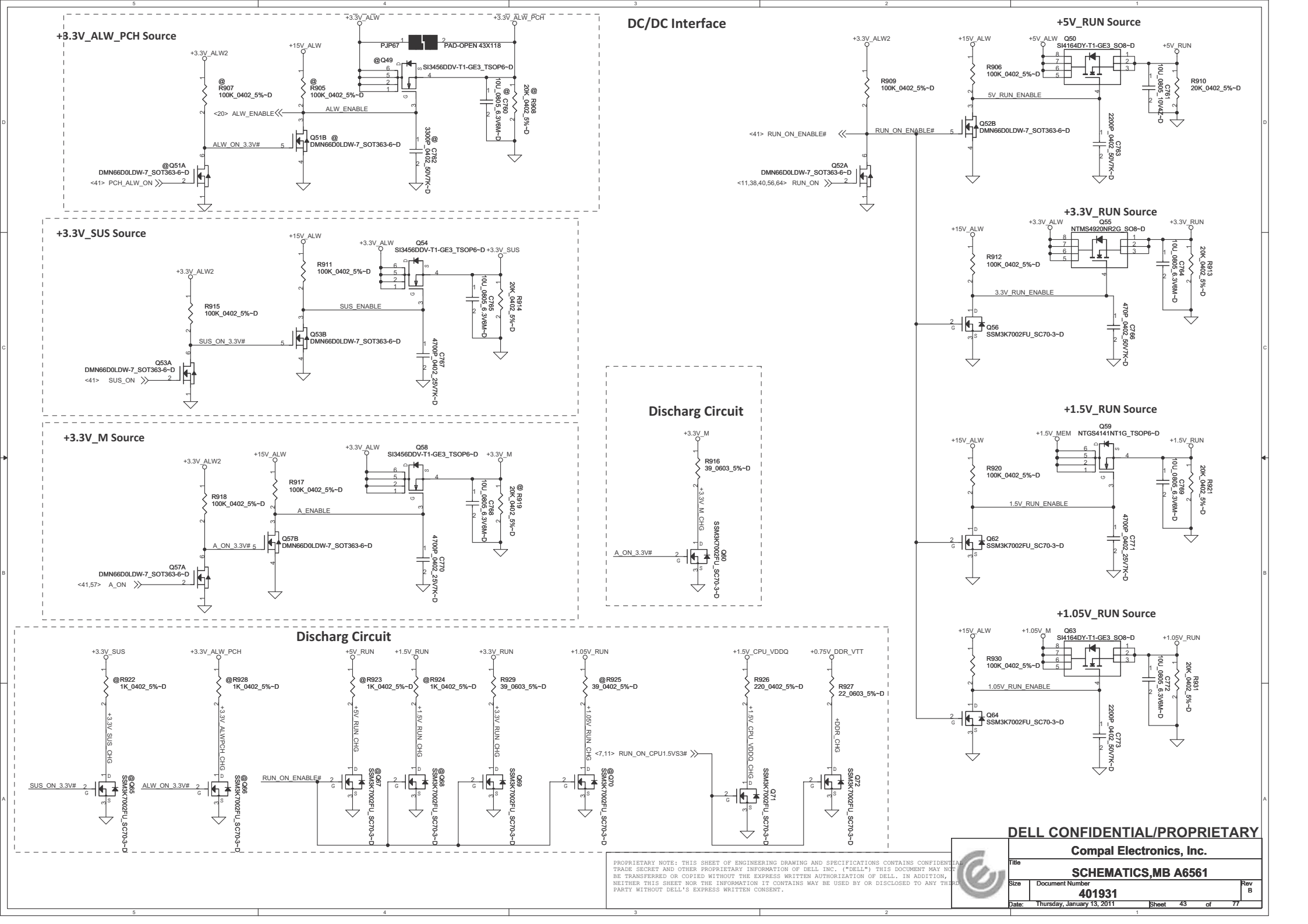


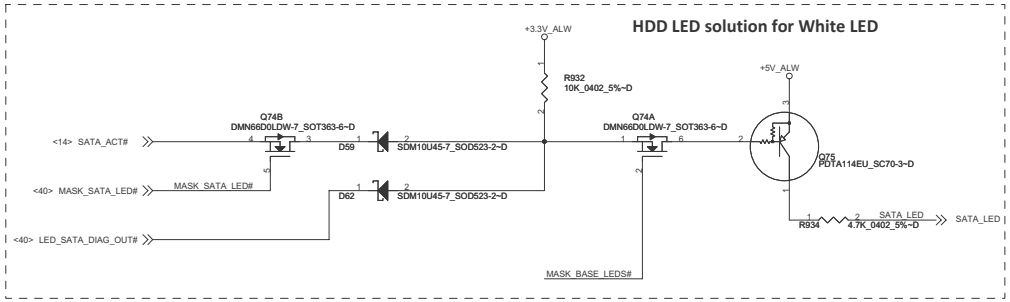
Power Switch for debug

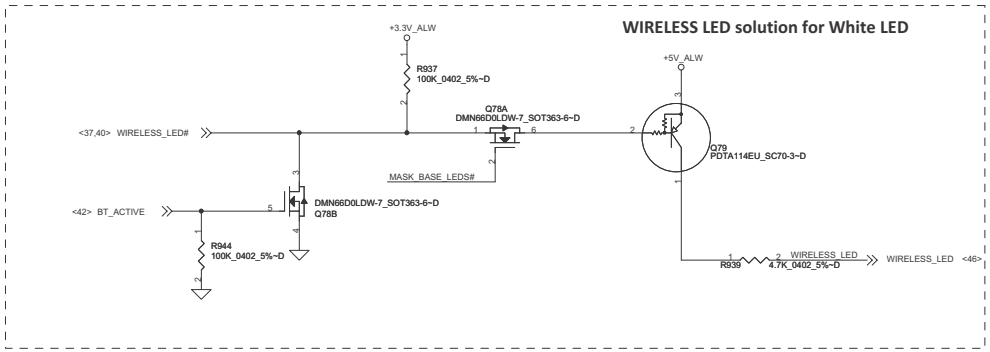


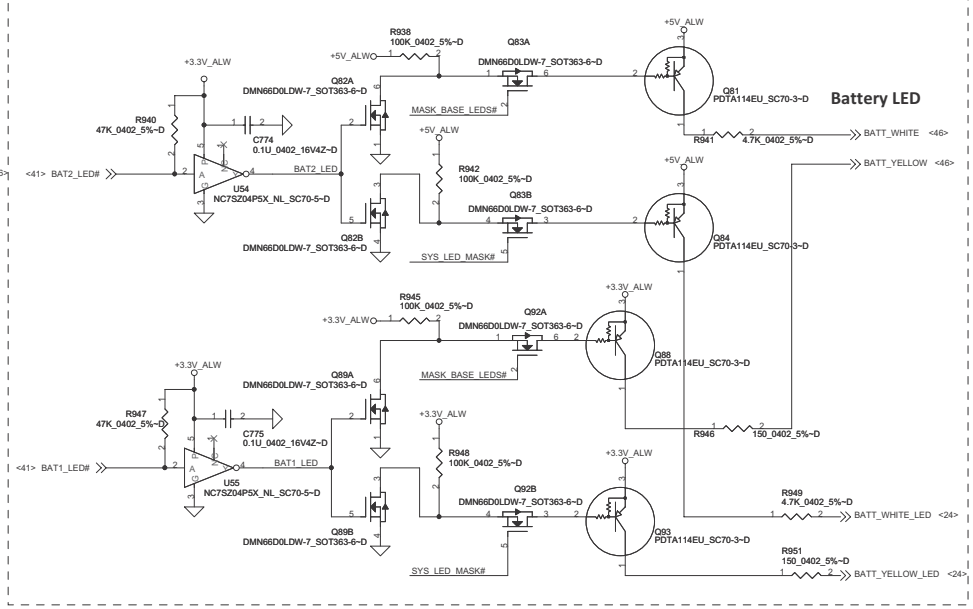
DELL CONFIDENTIAL/PROPRIETARY

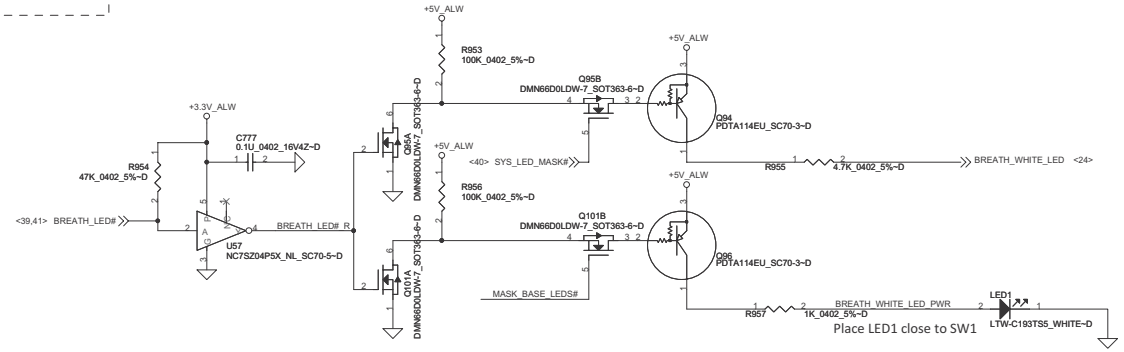
Compal Electronics, Inc.	
Title	SCHEMATICS,MB A6561
Size	Document Number 401931 Rev B
Date: Thursday, January 13, 2011	Sheet 42 of 77

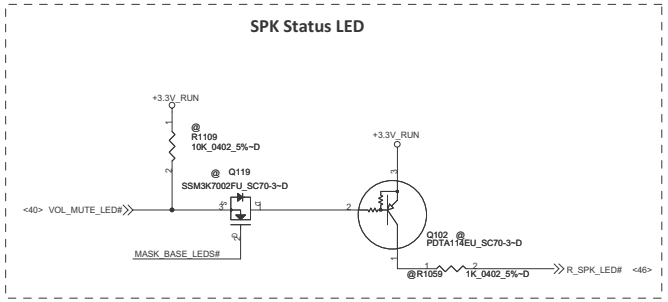

DC/DC Interface
+8.3V_ALW_PCH Source
+3.3V_SUS Source
+3.3V_M Source
Discharg Circuit
Discharg Circuit
+5V_RUN Source
+3.3V_RUN Source
+1.5V_RUN Source
+1.05V_RUN Source
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
SCHEMATICS,MB A6561
401931
Thursday, January 13, 2011
43 of 77

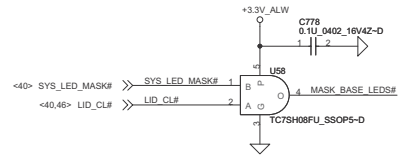


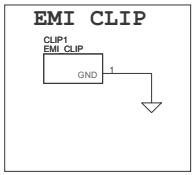


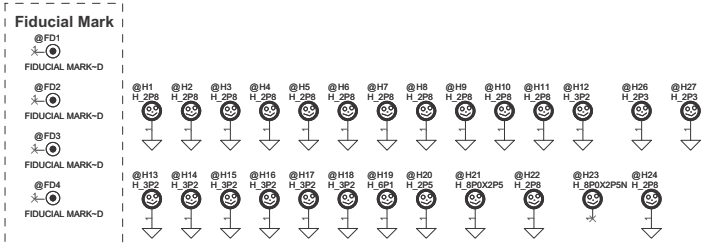












LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

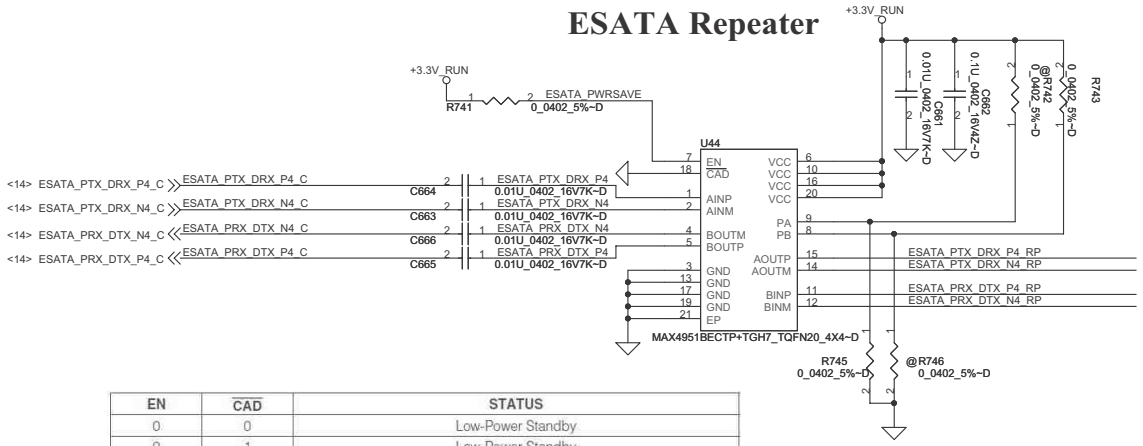
Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 44 of 77

ESATA Repeater

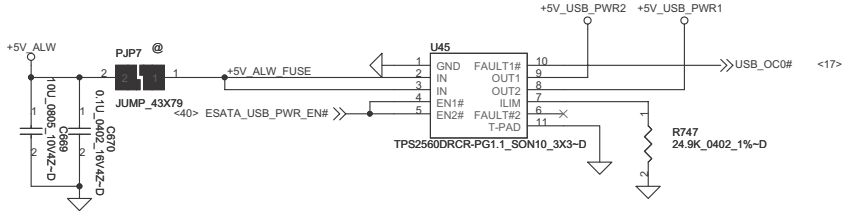


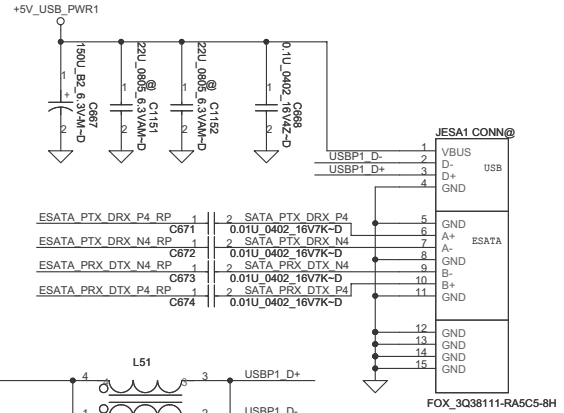
EN	$\overline{CAD}$	STATUS
0	0	Low-Power Standby
0	1	Low-Power Standby
1	0	Active
1	1	Low-Power Standby

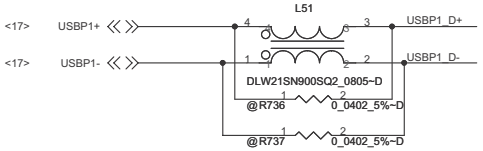
EN	PA	PB	CHANNEL A	CHANNEL B
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Preemphasis	Standard SATA
1	0	1	Standard SATA	Preemphasis
1	1	1	Preemphasis	Preemphasis

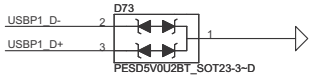
Note: *PA, PB, EN are internally pulled down to GND by 330kΩ resistors. $\overline{CAD}$ is internally pulled up to V_{CC} by a 330kΩ resistor.*

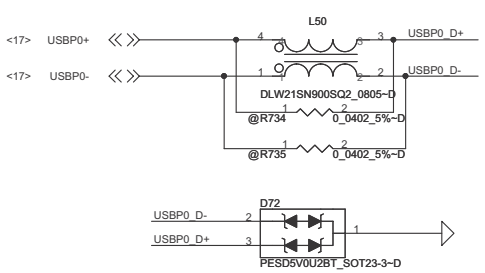
X = Don't care.

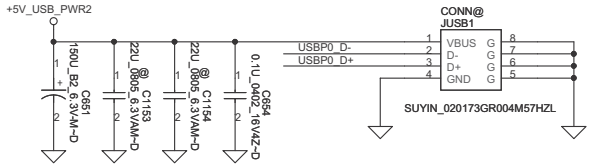




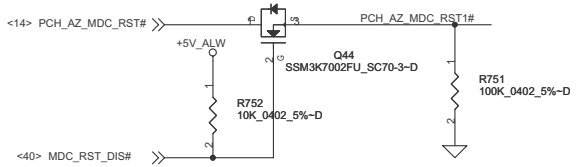


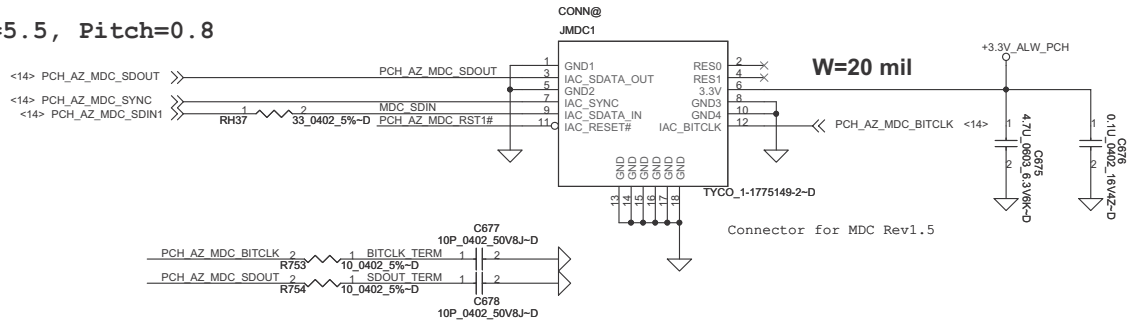






MDC CONN. H=5.5, Pitch=0.8





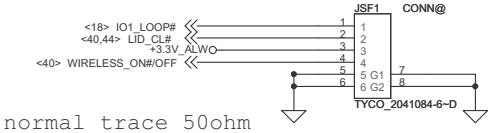
Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 45 of 77

power 20mil

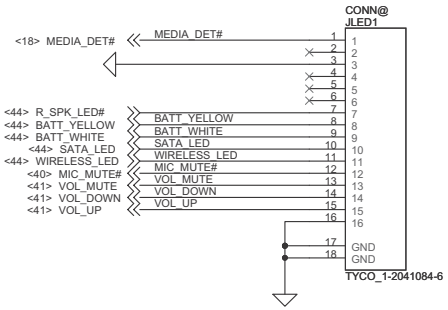


normal trace 50ohm

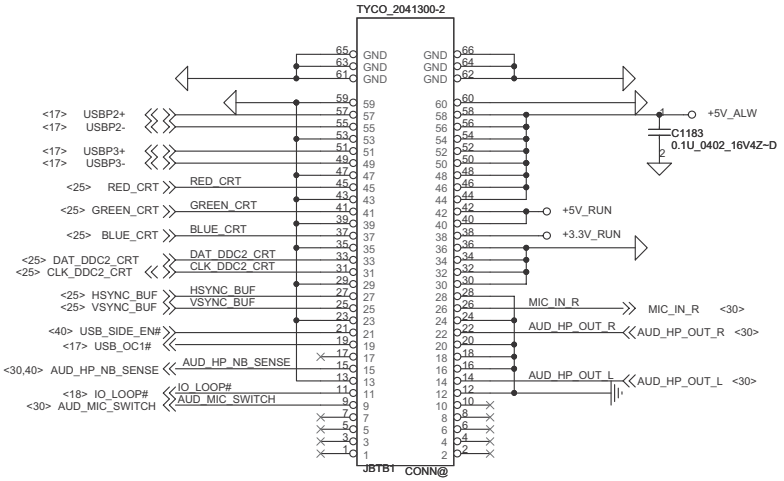
SNIFFER /Hall SENSOR IO BOARD

MEDIA BOARD

Defult on,
WIRELESS_ON/OFF#:
LOW: ON
HIGH: OFF

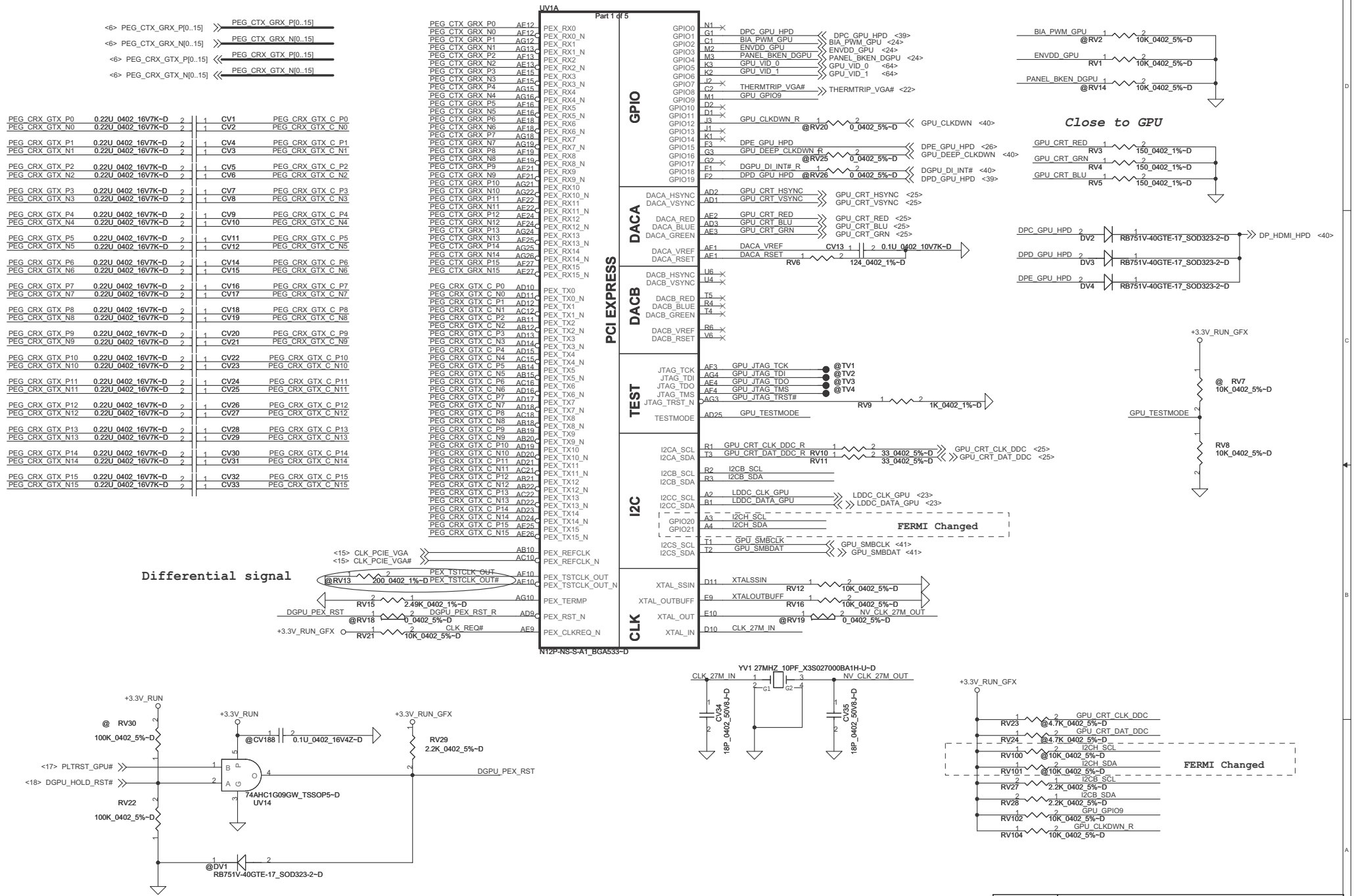


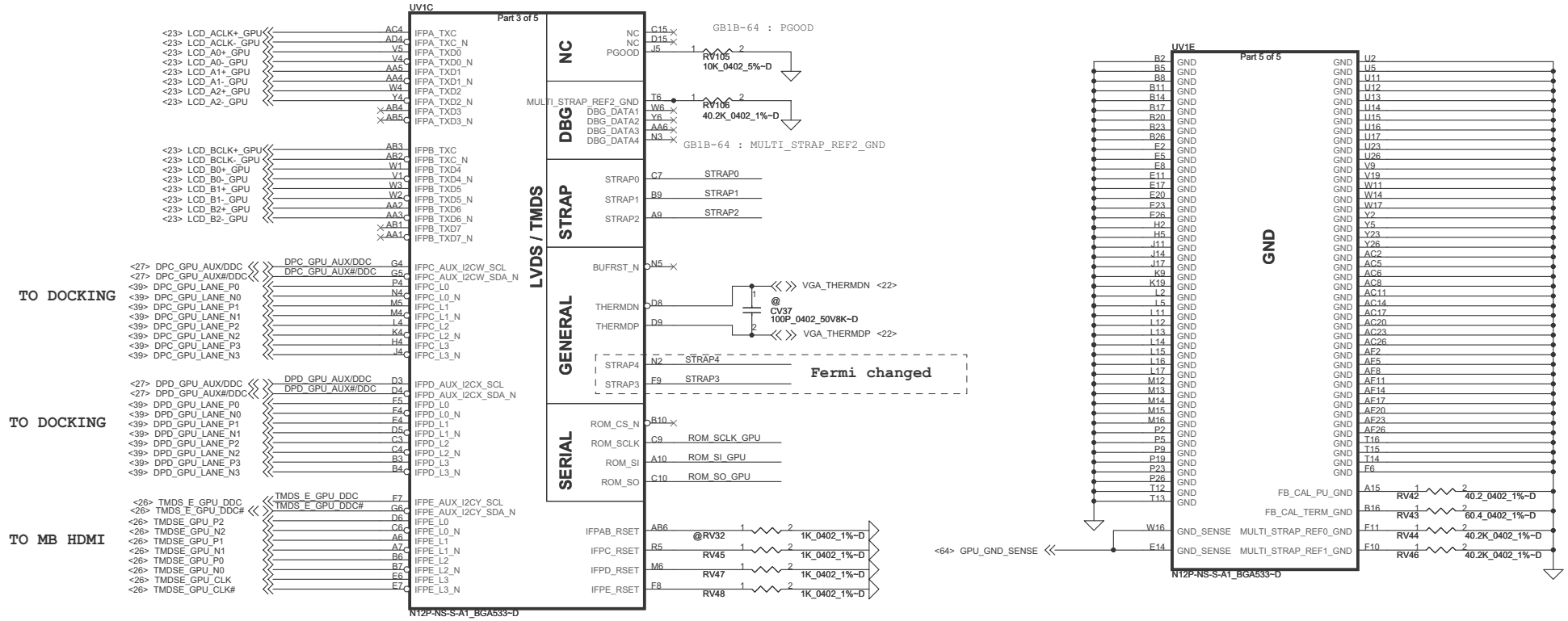
USBx2 /CRT/ AUDIO JACK IO BOARD

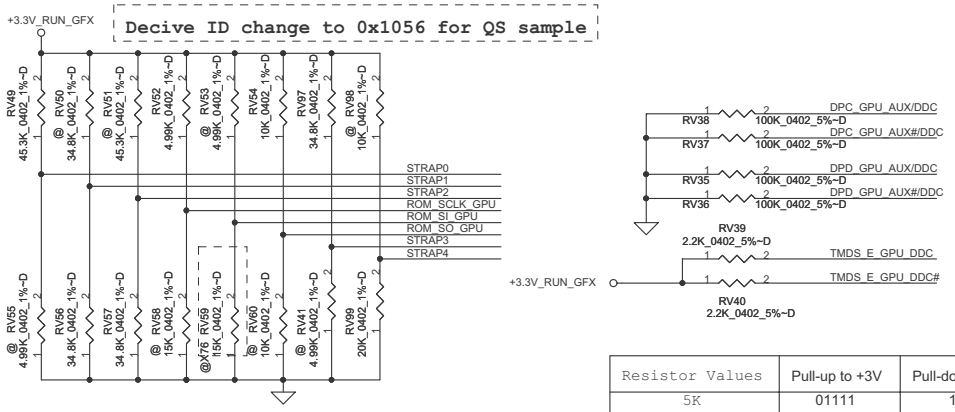


DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	SCHEMATICS,MB A6561
Size	Document Number 401931 Rev B
Date: Thursday, January 13, 2011	Sheet 46 of 77







set to multi-level straps

Resistor Values	Pull-up to +3V	Pull-down to Gnd
5K	01111	11111
10K	01110	11110
15K	01011	11011
20K	01001	11001
25K	00111	10111
30K	00110	10110
35K	00011	10011
45K	00000	100000

ROM_SCLK	PCIDEVID_EXT, SUB_VENDOR, SLOT_CLK, PEX_PLL_EN
ROM_SI	RAM_CFG[3:0]
ROM_SO	XCLK_417, FB_0_BAR_SIZE, ALT_ADOOR, VGA_DEVICE

** Hynix 64Mx16 DDR3 part stuff RV59=15K
Samsung 64Mx16 DDR3 part stuff RV59=20K

Hynix 128Mx16 DDR3 part stuff RV59=35K
Samsung 128Mx16 DDR3 part stuff RV59=45.3K

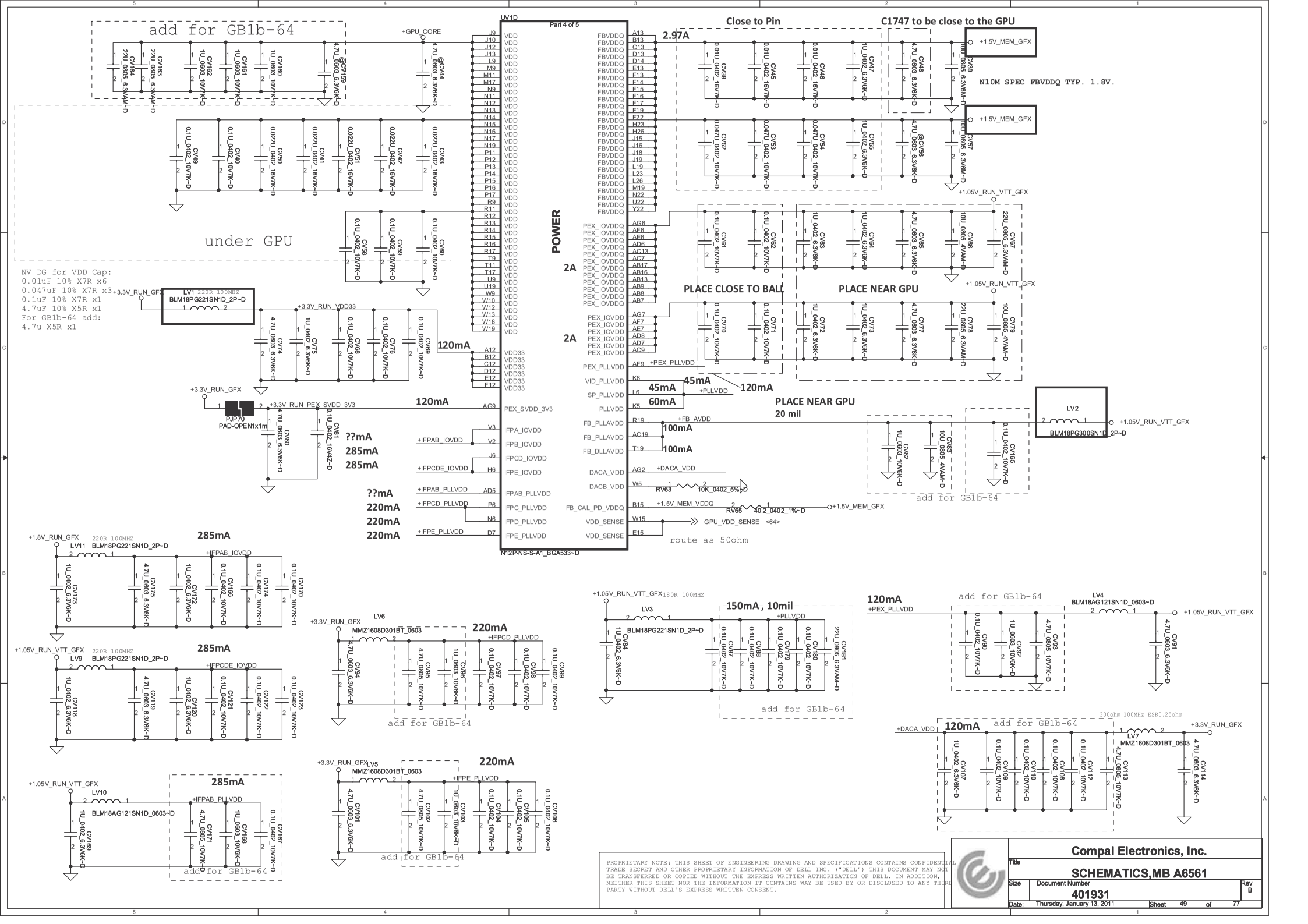
STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 48 of 77


add for GB1b-64
under GPU
POWER
Part 4 of 5
UV1D
N12P-NS-S-A1_BGA533~D
Close to Pin
C1747 to be close to the GPU
2.97A
N10M SPEC FBVDDQ TYP. 1.8V.
+1.5V_MEM_GFX
+1.05V_RUN_VTT_GFX
+GPU_CORE
+3.3V_RUN_GFX
+3.3V_RUN_VDD33
+3.3V_RUN_PEX_SVDD_3V3
+PEX_PLLVDD
+PLLVDD
+FB_AVDD
+DACA_VDD
+1.5V_MEM_VDDQ
GPU_VDD_SENSE <64>
route as 50ohm
PLACE CLOSE TO BALL
PLACE NEAR GPU
PLACE NEAR GPU
20 mil
2A
2A
120mA
45mA
45mA
60mA
120mA
100mA
100mA
??mA
285mA
285mA
??mA
220mA
220mA
220mA
285mA
285mA
285mA
220mA
220mA
150mA, 10mil
120mA
120mA
NV DG for VDD Cap:
0.01uF 10% X7R x6
0.047uF 10% X7R x3
0.1uF 10% X7R x1
4.7uF 10% X5R x1
For GB1b-64 add:
4.7u X5R x1
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
Compal Electronics, Inc.
SCHEMATICS,MB A6561
401931
Rev B
Thursday, January 13, 2011
Sheet 49 of 77

FBAD[0..63] FBAD[0..63] <51,52>
FBA_CMD[0..30] FBA_CMD[0..30] <51,52>
DQMA#[0..7] DQMA#[0..7] <51,52>
DQSA_RN[0..7] DQSA_RN[0..7] <51,52>
DQSA_WP[0..7] DQSA_WP[0..7] <51,52>

FBA_CMD3 — RV66 10K_0402_5%~D — CKE_1
FBA_CMD19 — RV68 10K_0402_5%~D — ODT_2
FBA_CMD0 — RV71 10K_0402_5%~D — ODT_1
FBA_CMD16 — RV72 10K_0402_5%~D — CKE_2
FBA_CMD20 — RV75 10K_0402_5%~D — RST

+1.5V_MEM_GFX — 1:1K_0402_1%~D @RV77 — +FB_VREF — 1:1K_0402_1%~D @RV78 — @CV128 0.01U_0402_25V7K~D — 16mil

UV1B
Part 2 of 5
MEMORY INTERFACE
N12P-NS-S-A1_BGA533~D

FBAD0	D22	FBA_D0	FBA_CMD0	G24	FBA_CMD0
FBAD1	E24	FBA_D1	FBA_CMD1	F27	FBA_CMD1
FBAD2	E22	FBA_D2	FBA_CMD2	F25	FBA_CMD2
FBAD3	D24	FBA_D3	FBA_CMD3	F26	FBA_CMD3
FBAD4	D26	FBA_D4	FBA_CMD4	G26	FBA_CMD4
FBAD5	D27	FBA_D5	FBA_CMD5	G27	FBA_CMD5
FBAD6	C27	FBA_D6	FBA_CMD6	G25	FBA_CMD6
FBAD7	B27	FBA_D7	FBA_CMD7	J25	FBA_CMD7
FBAD8	A21	FBA_D8	FBA_CMD8	J24	FBA_CMD8
FBAD9	B21	FBA_D9	FBA_CMD9	H24	FBA_CMD9
FBAD10	C21	FBA_D10	FBA_CMD10	H22	FBA_CMD10
FBAD11	C19	FBA_D11	FBA_CMD11	J26	FBA_CMD11
FBAD12	C18	FBA_D12	FBA_CMD12	G22	FBA_CMD12
FBAD13	D18	FBA_D13	FBA_CMD13	G23	FBA_CMD13
FBAD14	B18	FBA_D14	FBA_CMD14	J22	FBA_CMD14
FBAD15	C16	FBA_D15	FBA_CMD15	J27	FBA_CMD15
FBAD16	F21	FBA_D16	FBA_CMD16	M24	FBA_CMD16
FBAD17	F21	FBA_D17	FBA_CMD17	L24	FBA_CMD17
FBAD18	D20	FBA_D18	FBA_CMD18	J23	FBA_CMD18
FBAD19	F20	FBA_D19	FBA_CMD19	K23	FBA_CMD19
FBAD20	D17	FBA_D20	FBA_CMD20	K22	FBA_CMD20
FBAD21	F18	FBA_D21	FBA_CMD21	M23	FBA_CMD21
FBAD22	D16	FBA_D22	FBA_CMD22	K24	FBA_CMD22
FBAD23	E16	FBA_D23	FBA_CMD23	M27	FBA_CMD23
FBAD24	A22	FBA_D24	FBA_CMD24	N27	FBA_CMD24
FBAD25	C24	FBA_D25	FBA_CMD25	M26	FBA_CMD25
FBAD26	D21	FBA_D26	FBA_CMD26	K26	FBA_CMD26
FBAD27	B22	FBA_D27	FBA_CMD27	K27	FBA_CMD27
FBAD28	C22	FBA_D28	FBA_CMD28	K25	FBA_CMD28
FBAD29	A25	FBA_D29	FBA_CMD29	M25	FBA_CMD29
FBAD30	B25	FBA_D30	FBA_CMD30	L22	FBA_CMD30
FBAD31	A26	FBA_D31			
FBAD32	U24	FBA_D32	FBA_DQM0	C26	DQMA#0
FBAD33	V24	FBA_D33	FBA_DQM1	B19	DQMA#1
FBAD34	V23	FBA_D34	FBA_DQM2	D19	DQMA#2
FBAD35	R24	FBA_D35	FBA_DQM3	D23	DQMA#3
FBAD36	T23	FBA_D36	FBA_DQM4	T24	DQMA#4
FBAD37	R23	FBA_D37	FBA_DQM5	AA23	DQMA#5
FBAD38	P24	FBA_D38	FBA_DQM6	AB27	DQMA#6
FBAD39	P22	FBA_D39	FBA_DQM7	T26	DQMA#7
FBAD40	AC24	FBA_D40			
FBAD41	AB23	FBA_D41	FBA_DQS_RN0	D25	DQSA_RN0
FBAD42	AB24	FBA_D42	FBA_DQS_RN1	A18	DQSA_RN1
FBAD43	W24	FBA_D43	FBA_DQS_RN2	E18	DQSA_RN2
FBAD44	AA22	FBA_D44	FBA_DQS_RN3	B24	DQSA_RN3
FBAD45	W23	FBA_D45	FBA_DQS_RN4	R22	DQSA_RN4
FBAD46	W22	FBA_D46	FBA_DQS_RN5	Y24	DQSA_RN5
FBAD47	V22	FBA_D47	FBA_DQS_RN6	AA27	DQSA_RN6
FBAD48	AA25	FBA_D48	FBA_DQS_RN7	R27	DQSA_RN7
FBAD49	W27	FBA_D49			
FBAD50	W26	FBA_D50	FBA_DQS_WP0	C25	DQSA_WP0
FBAD51	W25	FBA_D51	FBA_DQS_WP1	A19	DQSA_WP1
FBAD52	AB25	FBA_D52	FBA_DQS_WP2	E19	DQSA_WP2
FBAD53	AB26	FBA_D53	FBA_DQS_WP3	A24	DQSA_WP3
FBAD54	AD26	FBA_D54	FBA_DQS_WP4	T22	DQSA_WP4
FBAD55	AD27	FBA_D55	FBA_DQS_WP5	AA24	DQSA_WP5
FBAD56	V25	FBA_D56	FBA_DQS_WP6	AA26	DQSA_WP6
FBAD57	R25	FBA_D57	FBA_DQS_WP7	T27	DQSA_WP7
FBAD58	V26	FBA_D58			
FBAD59	V27	FBA_D59	FB_VREF	A16	+FB_VREF
FBAD60	R26	FBA_D60			
FBAD61	T25	FBA_D61	FBA_CLK0	F24	CLKA0 <51>
FBAD62	N25	FBA_D62	FBA_CLK0_N	E23	CLKA0# <51>
FBAD63	N26	FBA_D63			
			FBA_CLK1	N24	CLKA1 <52>
			FBA_CLK1_N	N23	CLKA1# <52>
			FBA_DEBUG	M22	RV76 10K_0402_5%~D +1.5V_MEM_GFX

PAD~D TV6@
PAD~D TV5@

Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

+1.8V_RUN_GFX Source

+1.8V_RUN — QV7 PMV45EN_SOT23-3~D — +1.8V_RUN_GFX
1.05V_RUN_VTT_GFX#_EN — RV95 0_0402_5%~D — 1.05V_RUN_VTT_GFX#_EN_R
CV187 10U_0805_6.3V6M~D
RV96 20K_0402_5%~D

+3.3V_RUN_GFX Source

+3.3V_ALW2 — RV92 100K_0402_5%~D
+15V_ALW — RV91 100K_0402_5%~D
+3.3V_ALW — QV5 SI3456BDV-T1-E3_TSOP6~D — +3.3V_RUN_GFX
3.3V_RUN_GFX_EN
3.3V_RUN_GFX_ON# — QV6B DMN66D0LDW-7_SOT363-6~D
QV6A DMN66D0LDW-7_SOT363-6~D
<15,40> 3.3V_RUN_GFX_ON
CV186 3300P_0402_50V7K~D
CV185 10U_0805_6.3V6M~D
RV90 20K_0402_5%~D

+1.5V_MEM_GFX Source

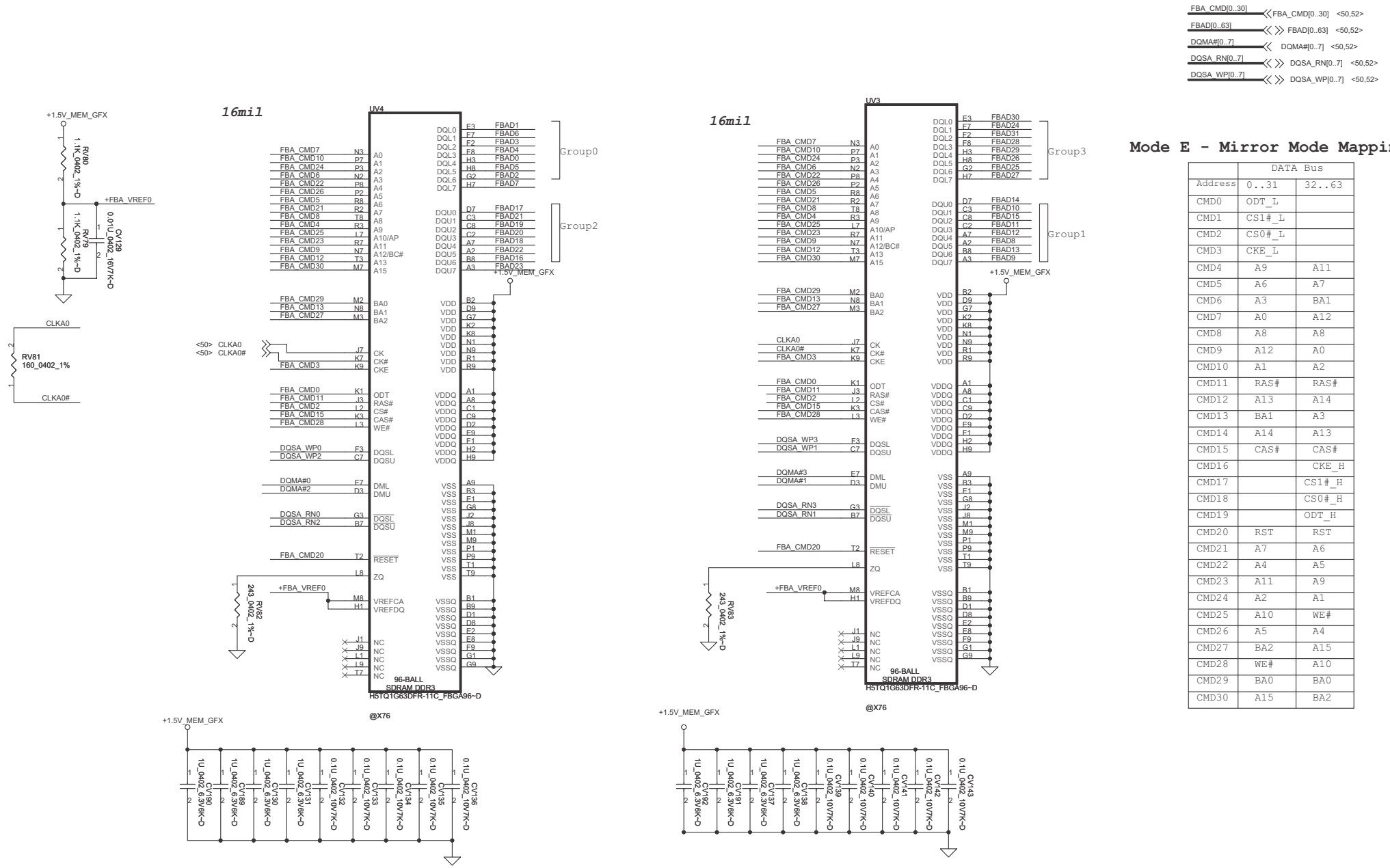
+3.3V_ALW2 — RV69 100K_0402_5%~D
+15V_ALW — RV87 100K_0402_5%~D
+1.5V_MEM — QV1 SI4164DY-T1-GE3_SO8~D — +1.5V_MEM_GFX
GFX_MEM_VTT_EN
GFX_MEM_VTT_ON# — QV2B DMN66D0LDW-7_SOT363-6~D
<40> GFX_MEM_VTT_ON — QV2A DMN66D0LDW-7_SOT363-6~D
CV125 2200P_0402_50V7K~D
CV124 10U_0805_6.3V6M~D
RV70 20K_0402_5%~D

+1.05V_RUN_VTT_GFX Source

+15V_ALW — RV73 100K_0402_5%~D
+1.05V_M — QV3 SI4164DY-T1-GE3_SO8~D — +1.05V_RUN_VTT_GFX
1.05V_RUN_VTT_GFX#_EN — QV4 SSM3K7002FU_SC70-3~D
CV127 2200P_0402_50V7K~D
CV126 10U_0805_6.3V6M~D
RV74 20K_0402_5%~D

Compal Electronics, Inc.
Title: SCHEMATICS,MB A6561
Size: Document Number: 401931 Rev: B
Date: Thursday, January 13, 2011 Sheet 50 of 77

Memory Partition A - Lower 32 bits

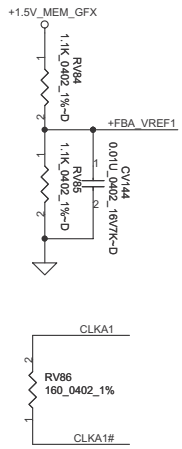


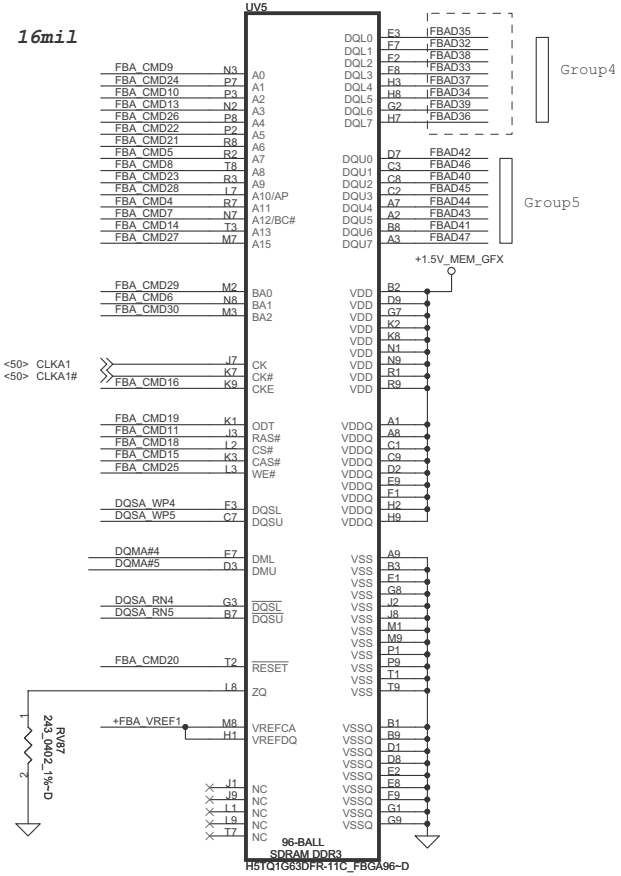
Mode E - Mirror Mode Mapping

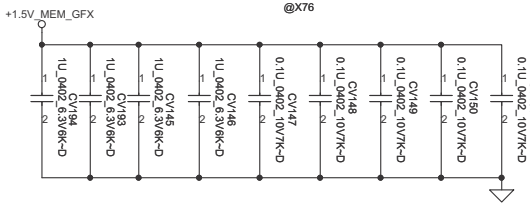
	DATA Bus	
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2

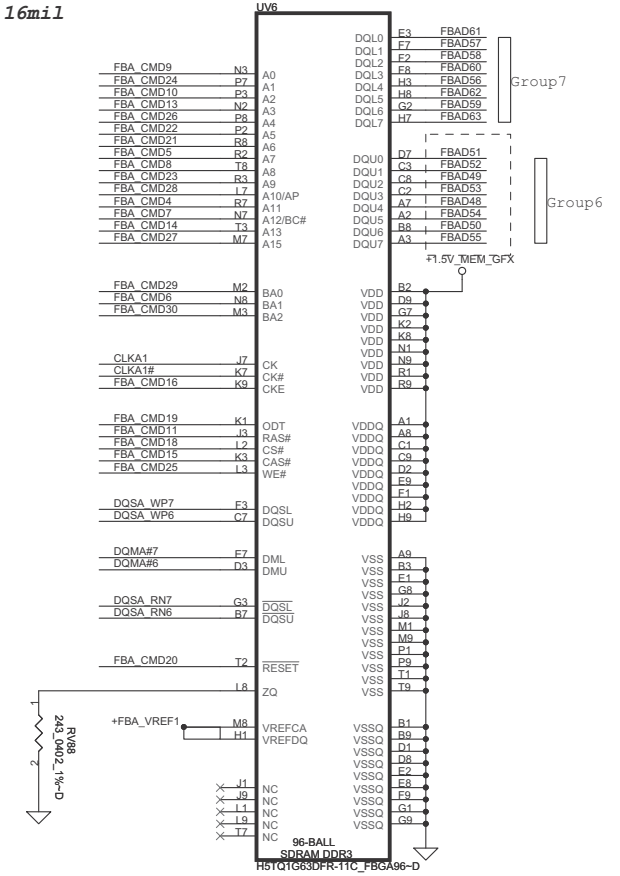
Compal Electronics, Inc.
Title: SCHEMATICS,MB A6561
Size: Document Number: 401931 Rev: B
Date: Thursday, January 13, 2011 Sheet 51 of 77

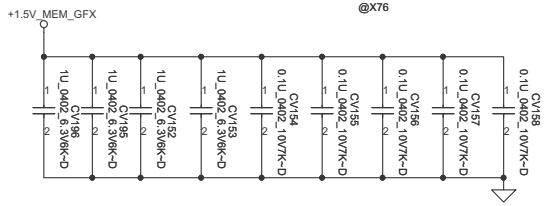
Memory Partition A - Upper 32 bits







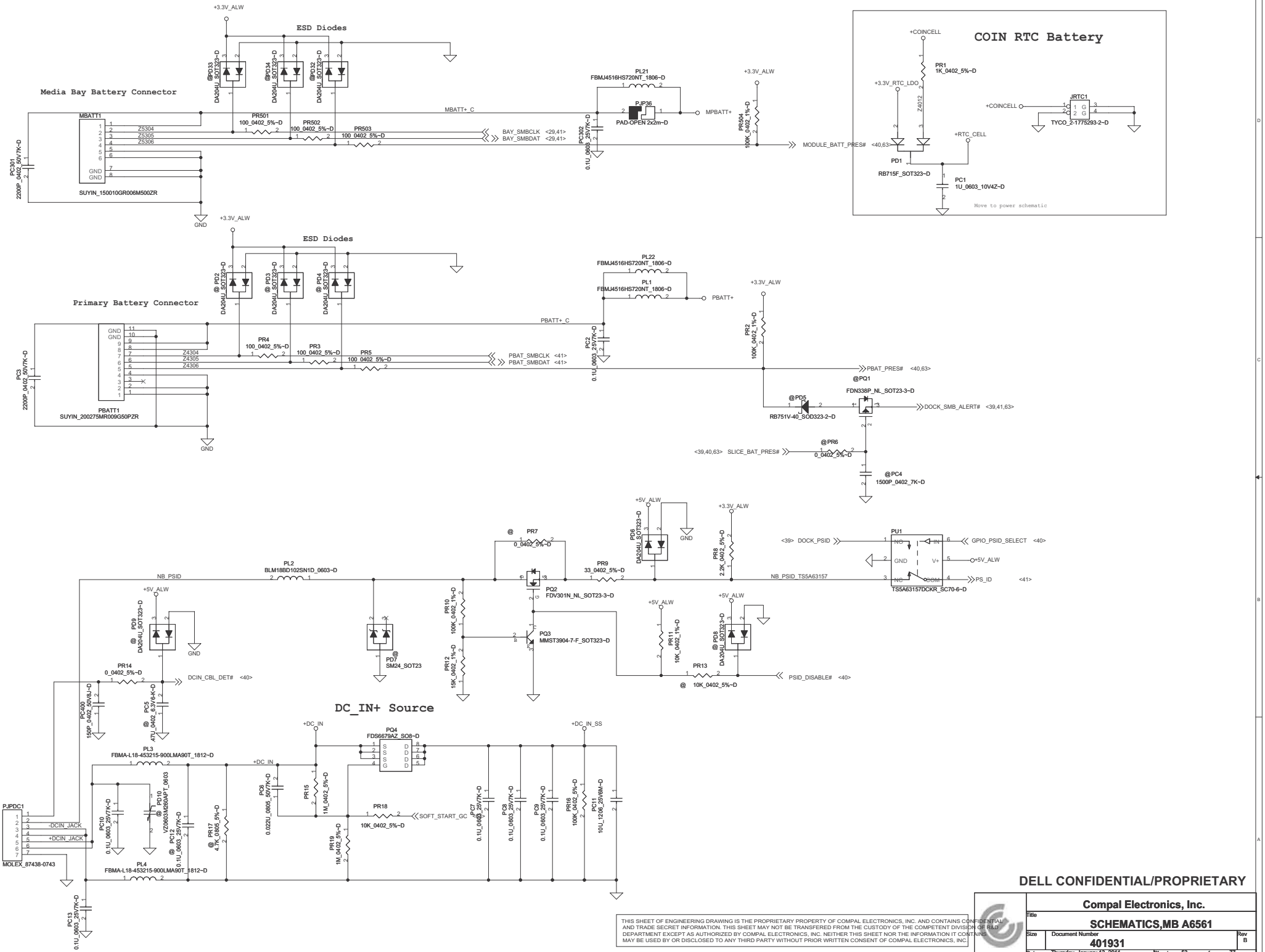




FBAD[0..63] FBAD[0..63] <50,51>
FBA_CMD[0..30] FBA_CMD[0..30] <50,51>
DQMA#[0..7] DQMA#[0..7] <50,51>
DQSA_RN[0..7] DQSA_RN[0..7] <50,51>
DQSA_WP[0..7] DQSA_WP[0..7] <50,51>

Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	SCHEMATICS,MB A6561
Size	Document Number: 401931
Rev	B
Date:	Thursday, January 13, 2011
Sheet	53 of 77

+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP/ +3.3V_RTC_LDO

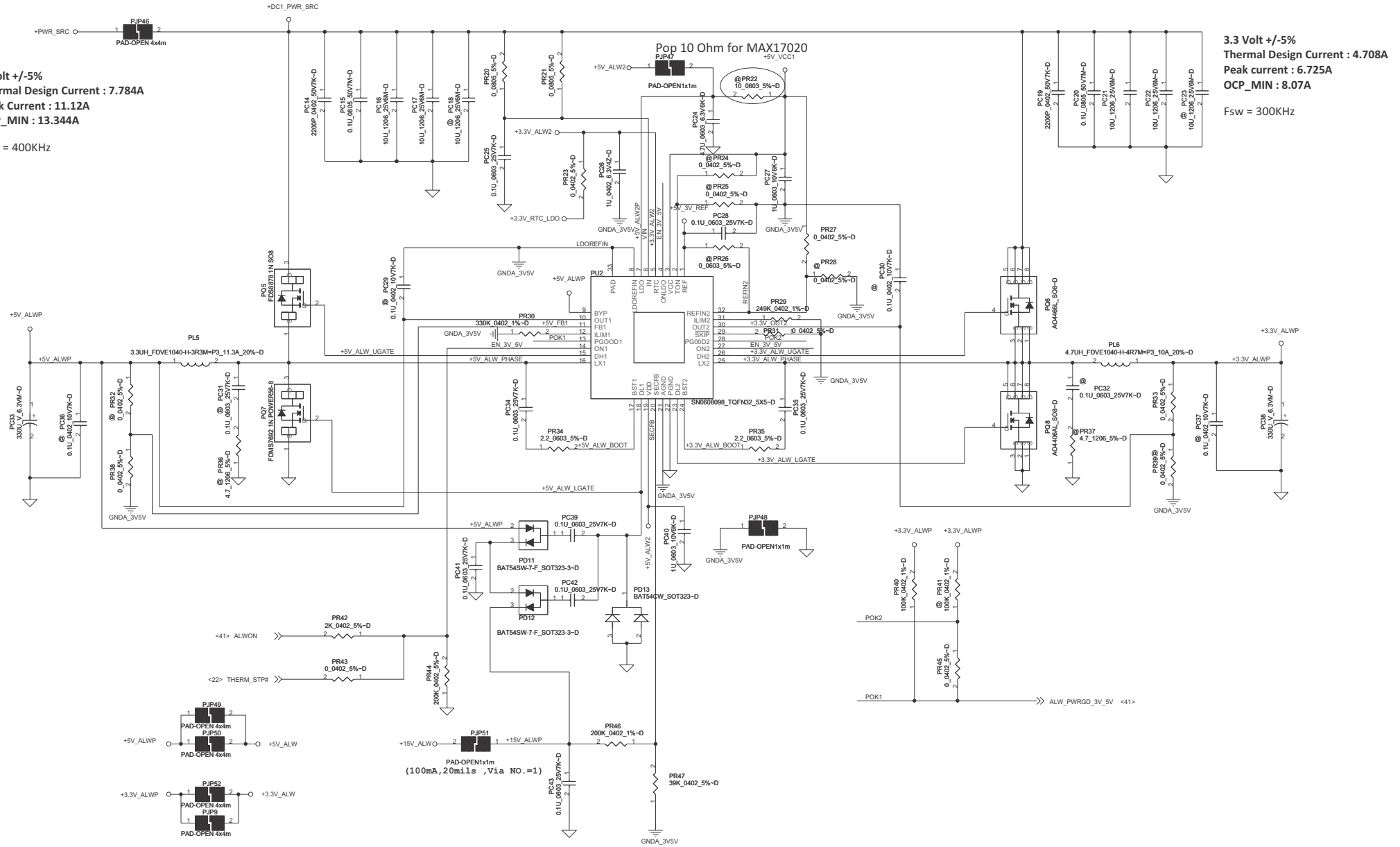
5 Volt +/-5%
Thermal Design Current : 7.784A
Peak Current : 11.12A
OCP_MIN : 13.344A

Fsw = 400KHz

3.3 Volt +/-5%
Thermal Design Current : 4.708A
Peak current : 6.725A
OCP_MIN : 8.07A

Fsw = 300KHz

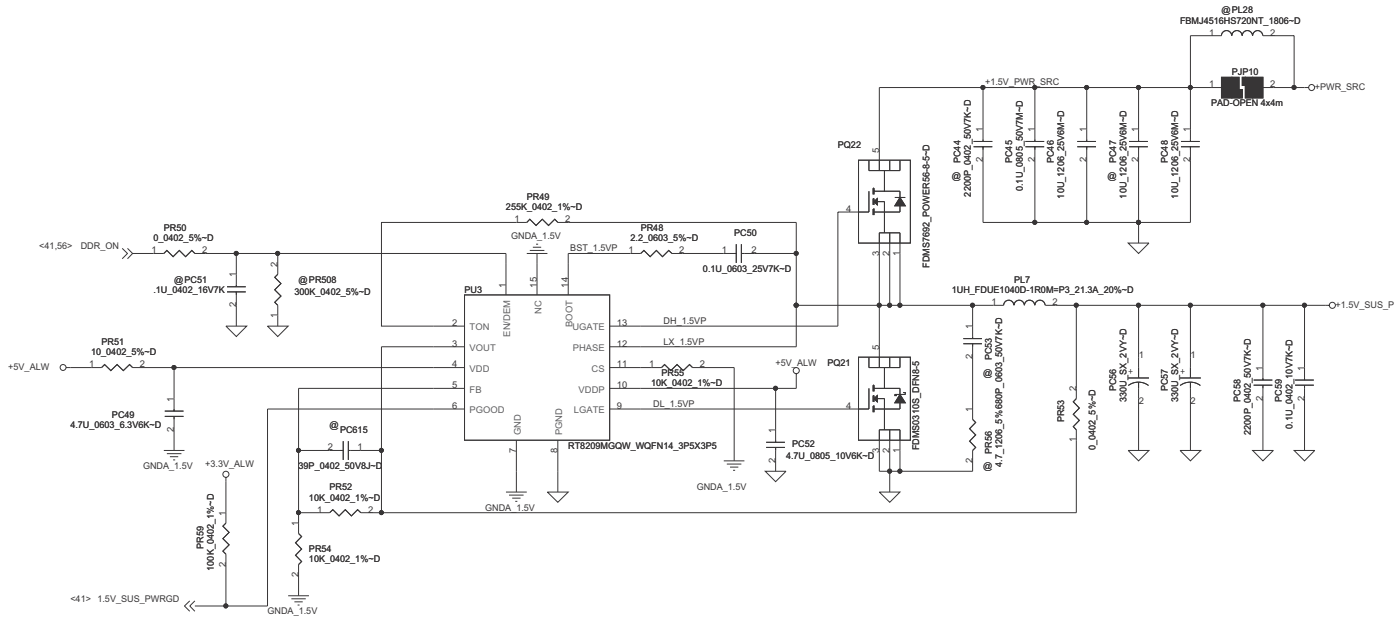
Pop 10 Ohm for MAX17020

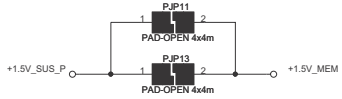


Compal Electronics, Inc.		
Title: SCHEMATICS,MB A6561		
Size	Document Number: 401931	Rev: B
Date: Thursday, January 13, 2011	Sheet 54 of 77	

+1.5V_SUS_P(RT8209B)

1.5 Volt +/-5%
Thermal Design Current: 12.259A
Peak current: 17.513A
OCP_MIN:21.016A



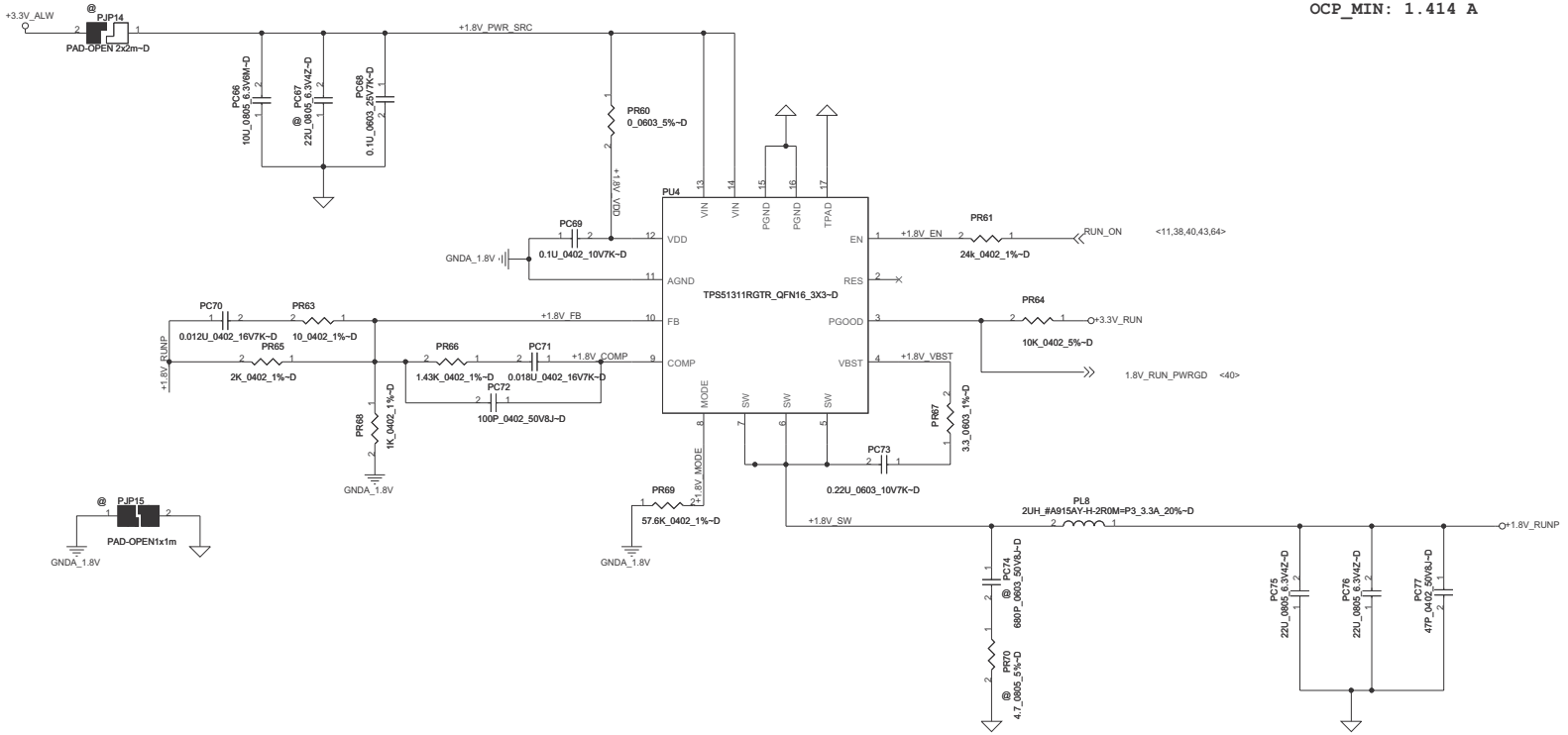


Compal Electronics, Inc.

Title	SCHEMATICS,MB A6561	
Size	Document Number 401931	Rev B
Date: Thursday, January 13, 2011	Sheet 55 of 77	

+1.8V_RUNP

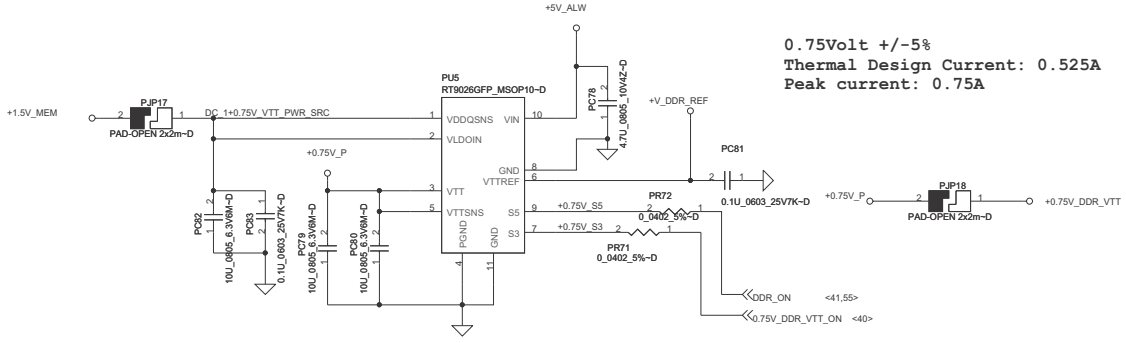
1.8 Volt +/-5%
Thermal Design Current: 0.824 A
Peak current: 1.178 A
OCP_MIN: 1.414 A

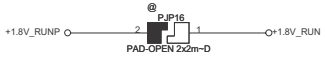


+0.75V_DDR_VTT

DDR3 Termination

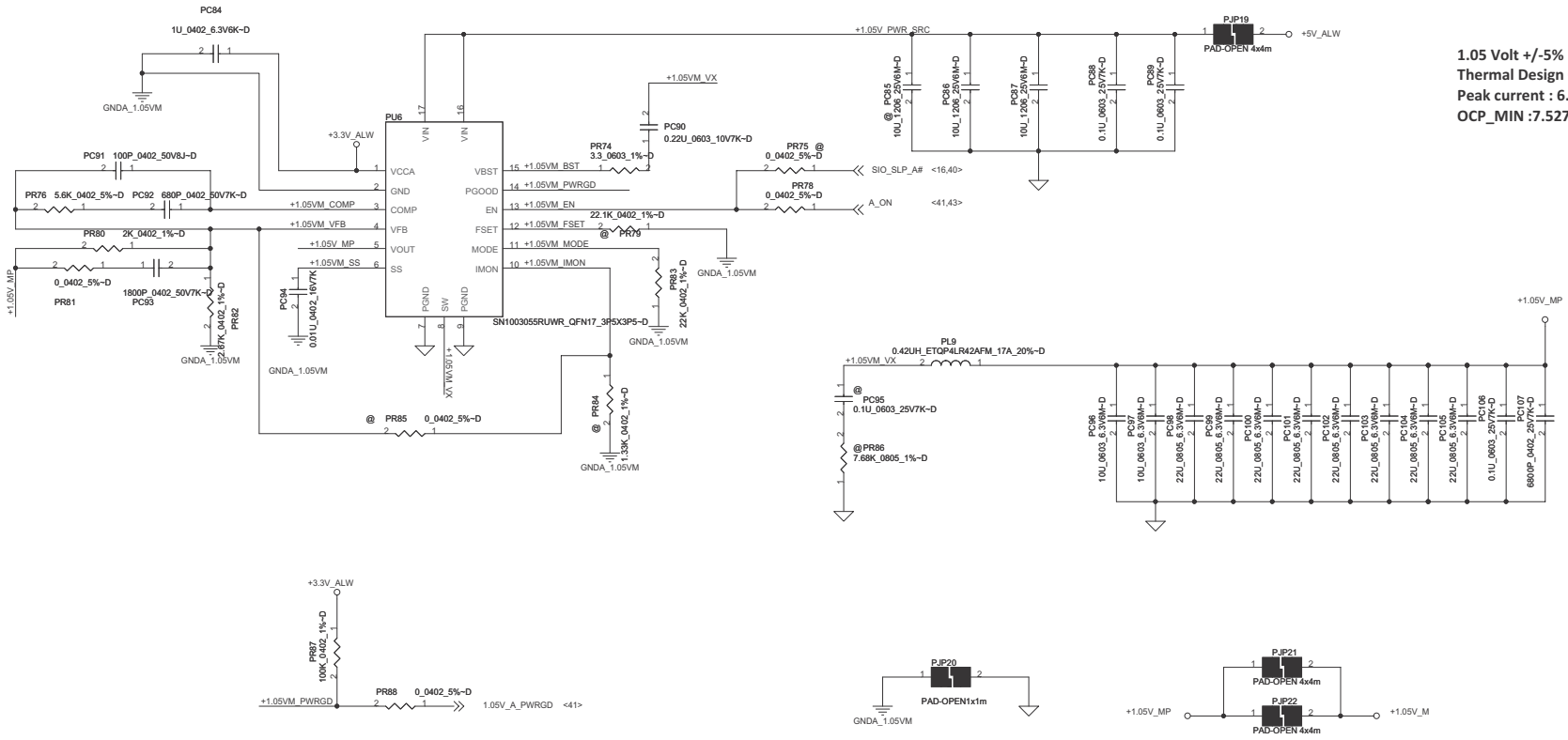
0.75Volt +/-5%
Thermal Design Current: 0.525A
Peak current: 0.75A





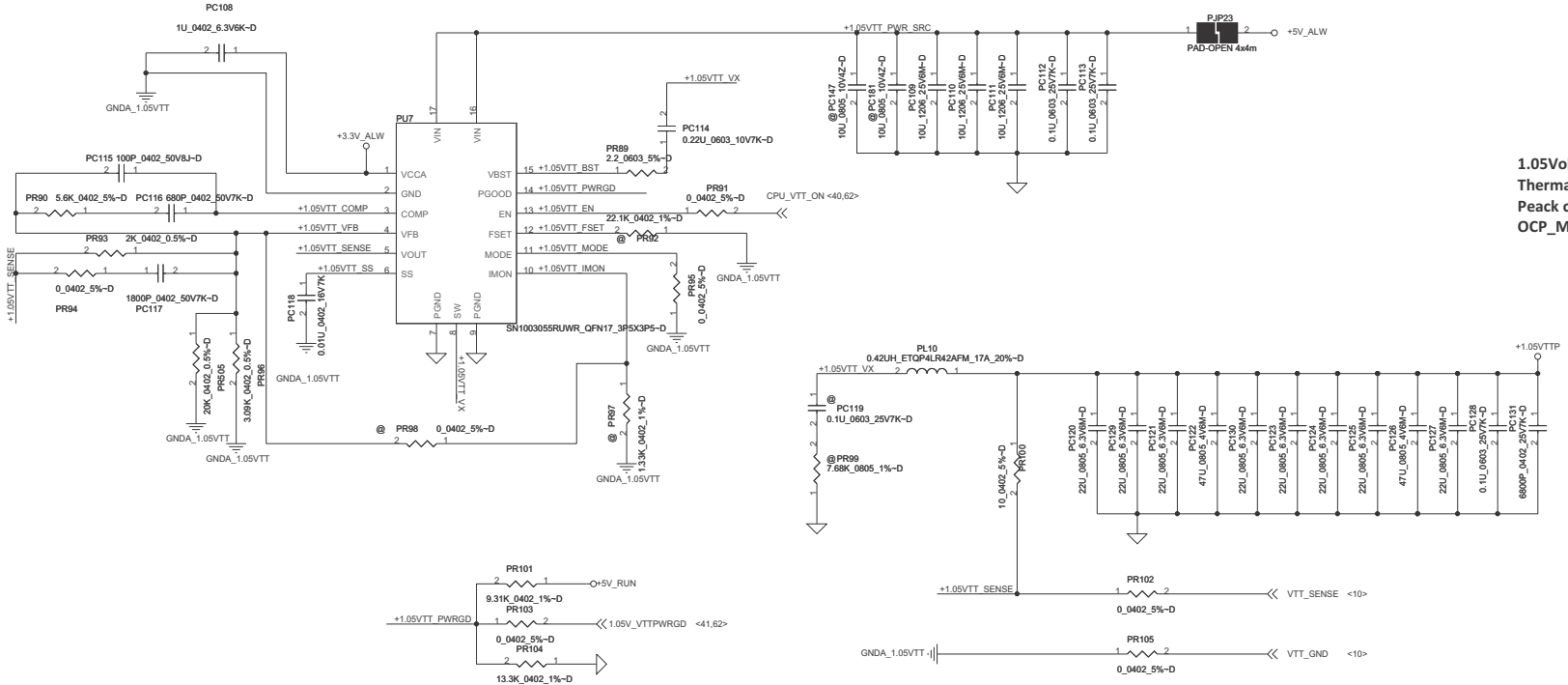
VOUT=1.8V
L=3.3uF
Fsw=290KHz
D=0.092
Input Ripple Current=TDC*(D*(1-D))^0.5=0.884A
Output Ripple Current=1.707A
Output Ripple Voltage=1.707*15m=20.5mV

+1.05V_M



1.05 Volt +/-5%
Thermal Design Current : 4.391A
Peak current : 6.273A
OCP_MIN :7.527A

Compal Electronics, Inc.		
Title: SCHEMATICS,MB A6561		
Size	Document Number: 401931	Rev: B
Date: Thursday, January 13, 2011	Sheet 57 of 77	



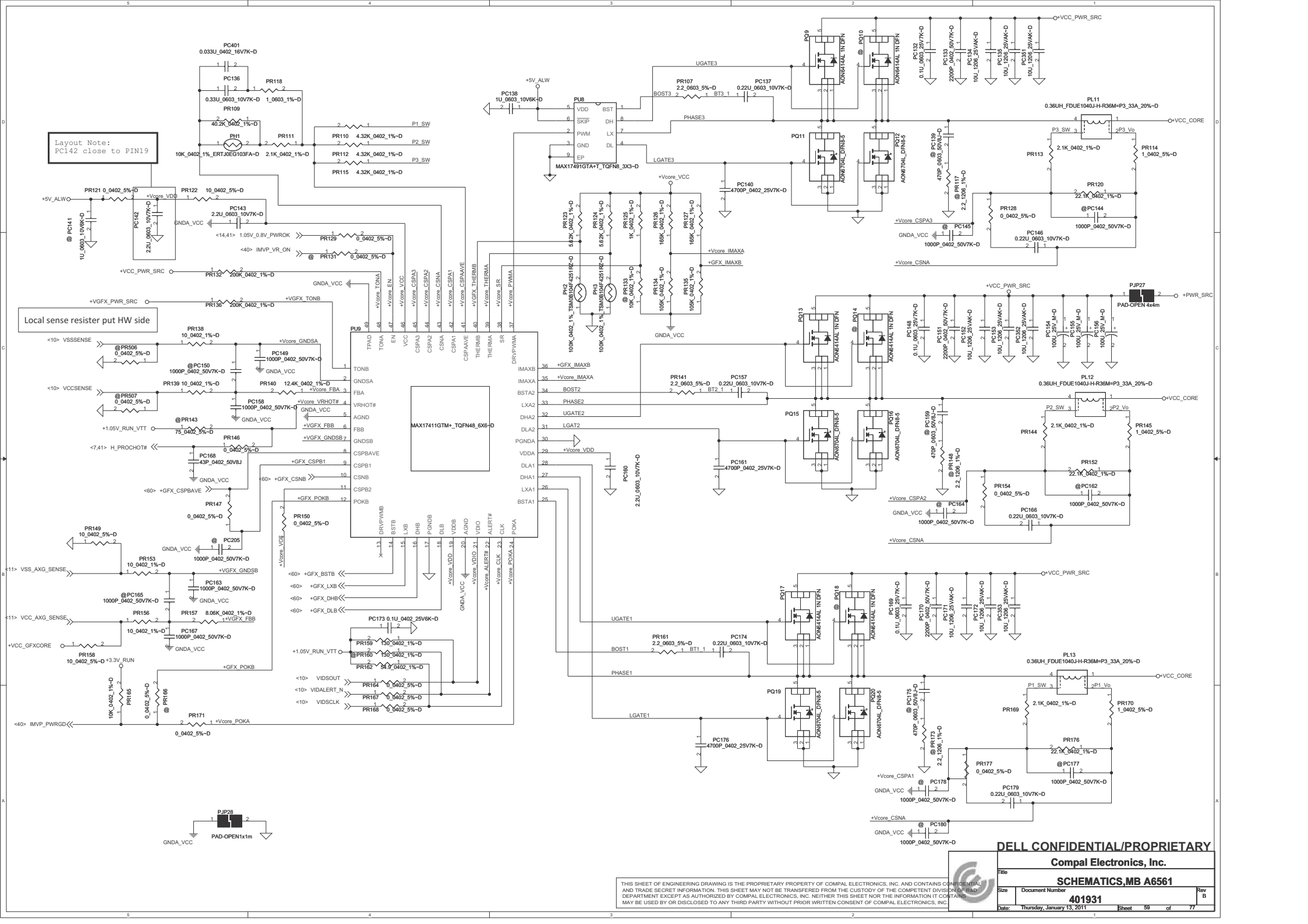
1.05Volt +/-5%
Thermal Design Current : 5.98A
Peack current : 8.543A
OCP_MIN : 10.251A

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

Size | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 58 of 77

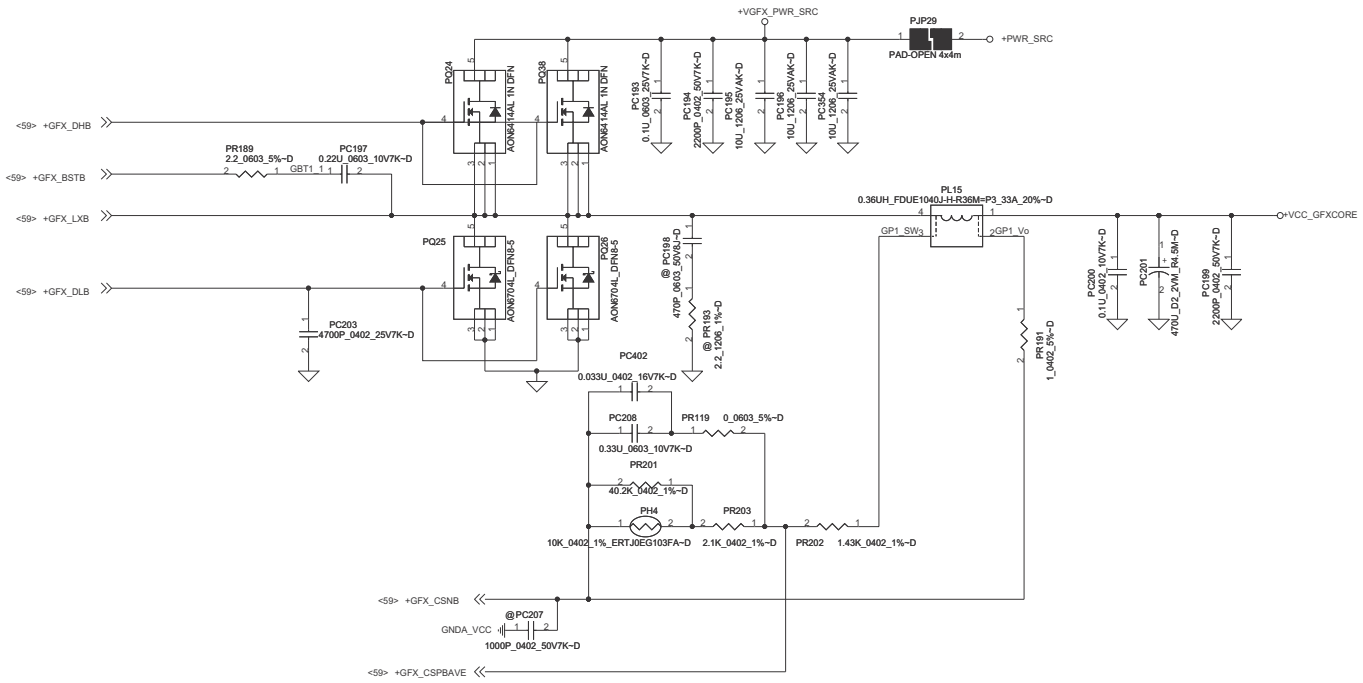


Compal Electronics, Inc.

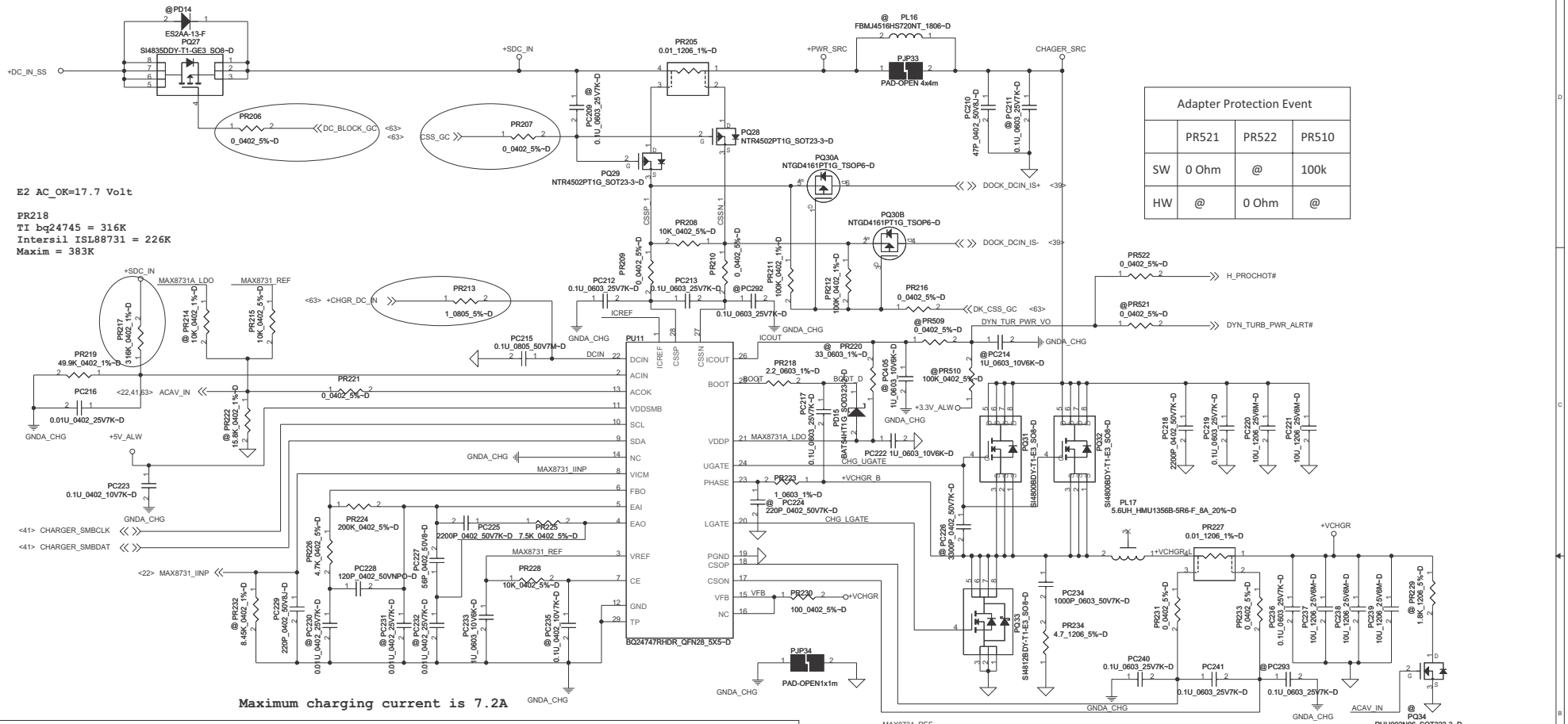
Title: SCHEMATICS,MB A6561

Size: | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 59 of 77

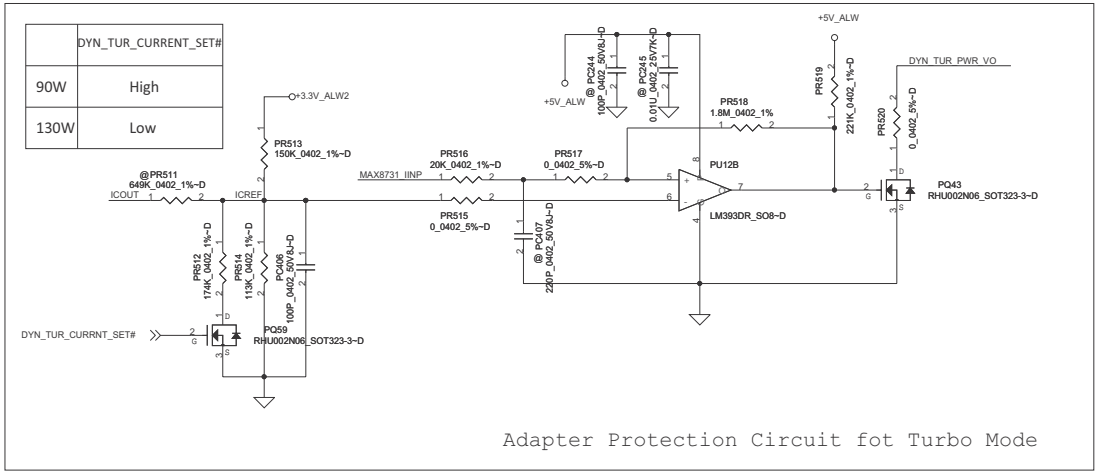


Compal Electronics, Inc.		
Title: SCHEMATICS,MB A6561		
Size	Document Number: 401931	Rev: B
Date: Thursday, January 13, 2011	Sheet 60 of 77	



Adapter Protection Event			
	PR521	PR522	PR510
SW	0 Ohm	@	100k
HW	@	0 Ohm	@

	DYN_TUR_CURRENT_SET#
90W	High
130W	Low



Adapter Protection Circuit fot Turbo Mode

DELL CONFIDENTIAL/PROPRIETARY

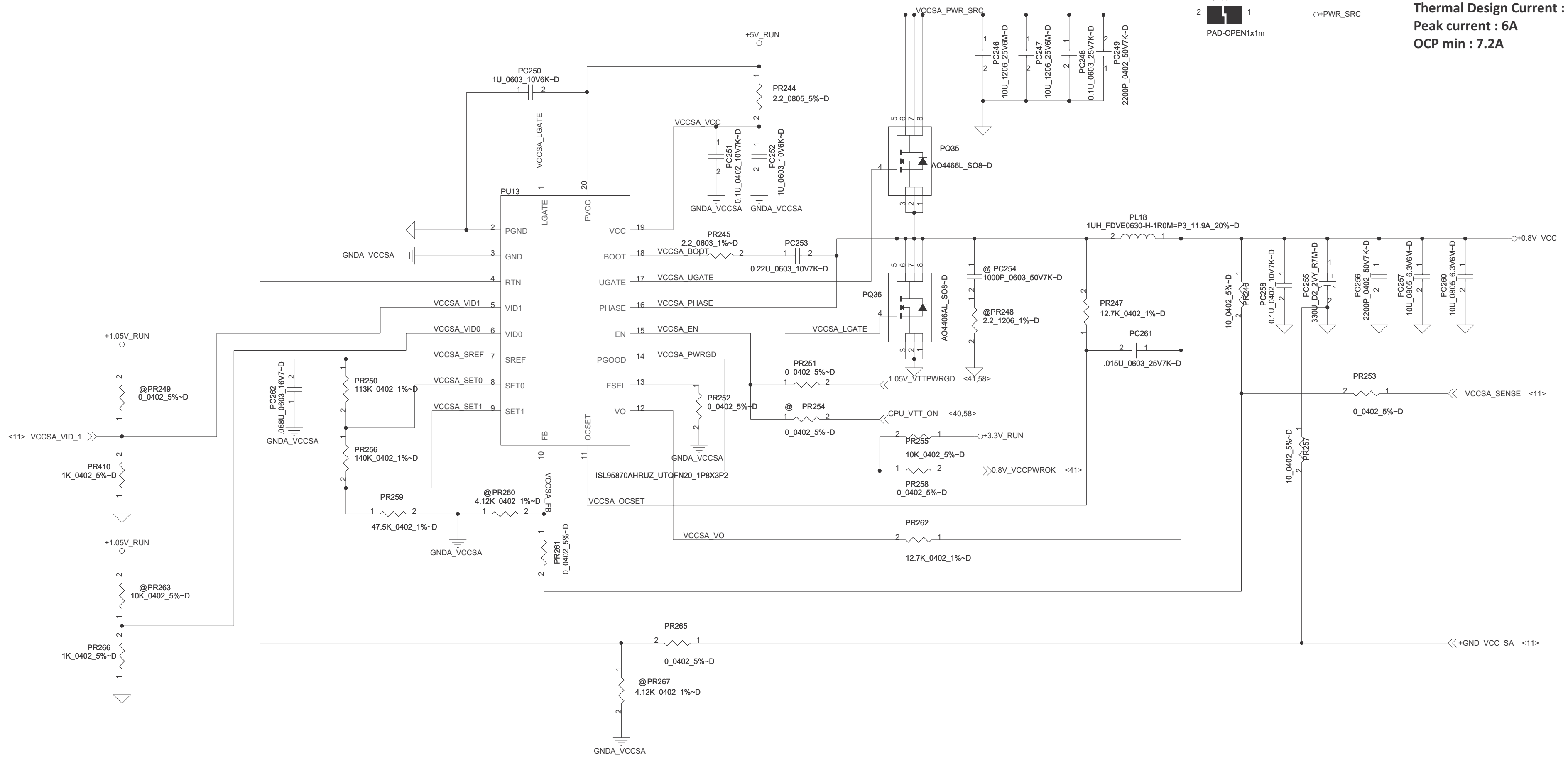
Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

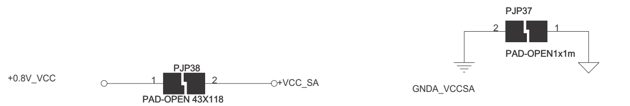
Size: | Document Number: 401931 | Rev: B

Date: Thursday, January 13, 2011 | Sheet 61 of 77

VCC_SA
Thermal Design Current : 4.2A
Peak current : 6A
OCP min : 7.2A



VCCSA_PWR_SRC
PJP35
PAD-OPEN1x1m
+PWR_SRC
PC246 10U_1206_25V6M~D
PC247 10U_1206_25V6M~D
PC248 0.1U_0603_25V7K~D
PC249 2200P_0402_50V7K~D
+5V_RUN
PR244 2.2_0805_5%~D
PC250 1U_0603_10V6K~D
VCCSA_VCC
PC251 0.1U_0402_10V7K~D
PC252 1U_0603_10V6K~D
GNDA_VCCSA
PQ35 AO4466L_SO8~D
PU13
PGND
GND
RTN
VID1
VID0
SREF
SET0
SET1
LGATE
PVCC
VCC
BOOT
UGATE
PHASE
EN
PGOOD
FSEL
VO
FB
OCSET
VCCSA_LGATE
VCCSA_BOOT
VCCSA_UGATE
VCCSA_PHASE
VCCSA_EN
VCCSA_PWRGD
VCCSA_VID1
VCCSA_VID0
VCCSA_SREF
VCCSA_SET0
VCCSA_SET1
PR245 2.2_0603_1%~D
PC253 0.22U_0603_10V7K~D
PL18 1UH_FDVE0630-H-1R0M=P3_11.9A_20%~D
+0.8V_VCC
PQ36 AO4406AL_SO8~D
@ PC254 1000P_0603_50V7K~D
@PR248 2.2_1206_1%~D
PR247 12.7K_0402_1%~D
PC261 .015U_0603_25V7K~D
PR246 10_0402_5%~D
PC258 0.1U_0402_10V7K~D
PC255 330U_D2_2V_Y_R7M~D
PC256 2200P_0402_50V7K~D
PC257 10U_0805_6.3V6M~D
PC260 10U_0805_6.3V6M~D
PR251 0_0402_5%~D
1.05V_VTTPWRGD <41,58>
@ PR254 0_0402_5%~D
CPU_VTT_ON <40,58>
PR252 0_0402_5%~D
PR255 10K_0402_5%~D
+3.3V_RUN
PR258 0_0402_5%~D
0.8V_VCCPWROK <41>
PR253 0_0402_5%~D
VCCSA_SENSE <11>
PR257 10_0402_5%~D
ISL95870AHRUZ_UTQFN20_1P8X3P2
VCCSA_OCSET
VCCSA_FB
VCCSA_VO
PR262 12.7K_0402_1%~D
PC262 .068U_0603_16V7~D
PR250 113K_0402_1%~D
PR256 140K_0402_1%~D
PR259 47.5K_0402_1%~D
@PR260 4.12K_0402_1%~D
PR261 0_0402_5%~D
+1.05V_RUN
@PR249 0_0402_5%~D
<11> VCCSA_VID_1
PR410 1K_0402_5%~D
@PR263 10K_0402_5%~D
PR266 1K_0402_5%~D
PR265 0_0402_5%~D
+GND_VCC_SA <11>
@PR267 4.12K_0402_1%~D



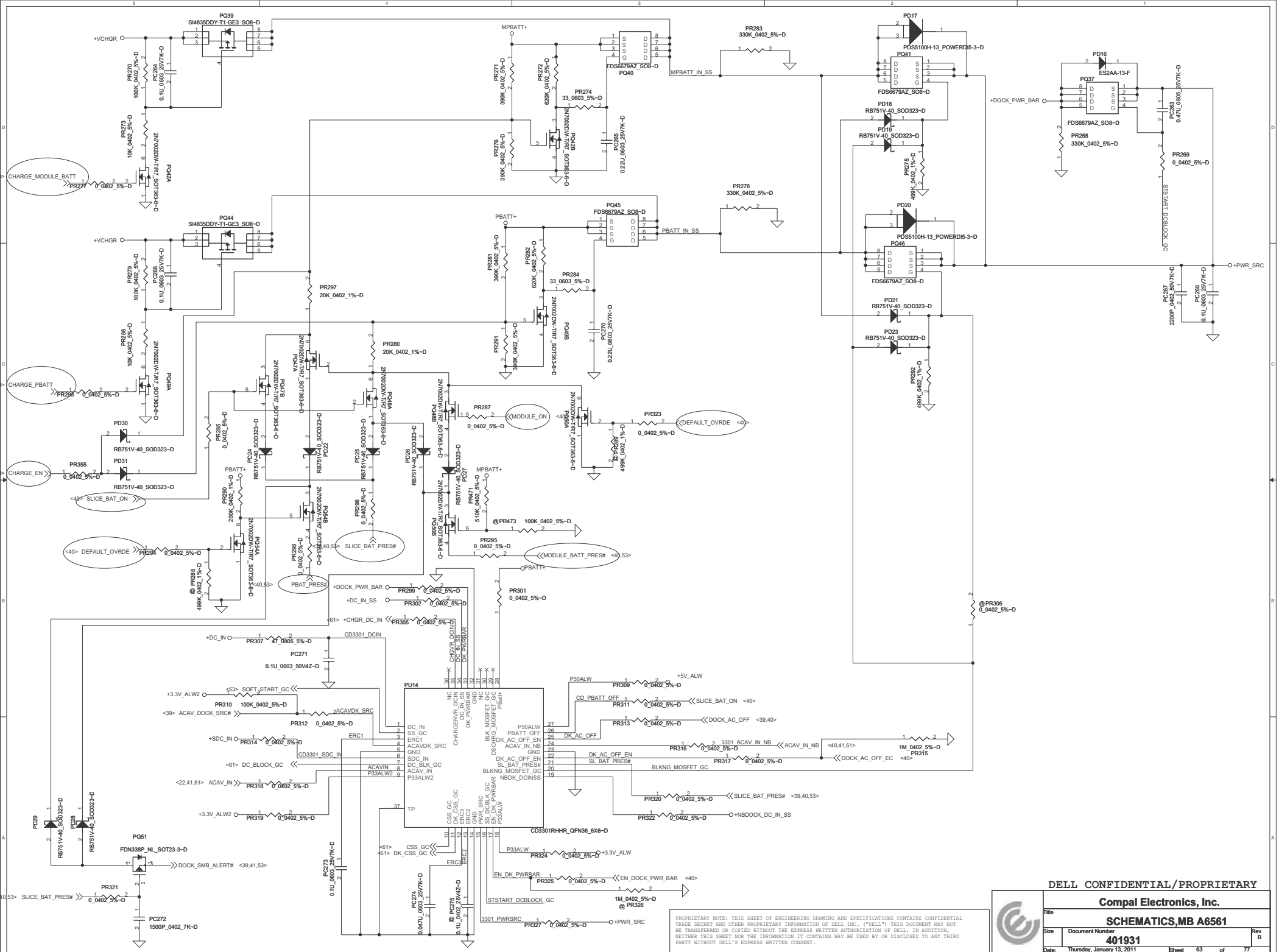
	0.9V	0.8V
VCCSA_VID_1	0	1

output voltage adjustable network

Compal Electronics, Inc.

Title: SCHEMATICS,MB A6561

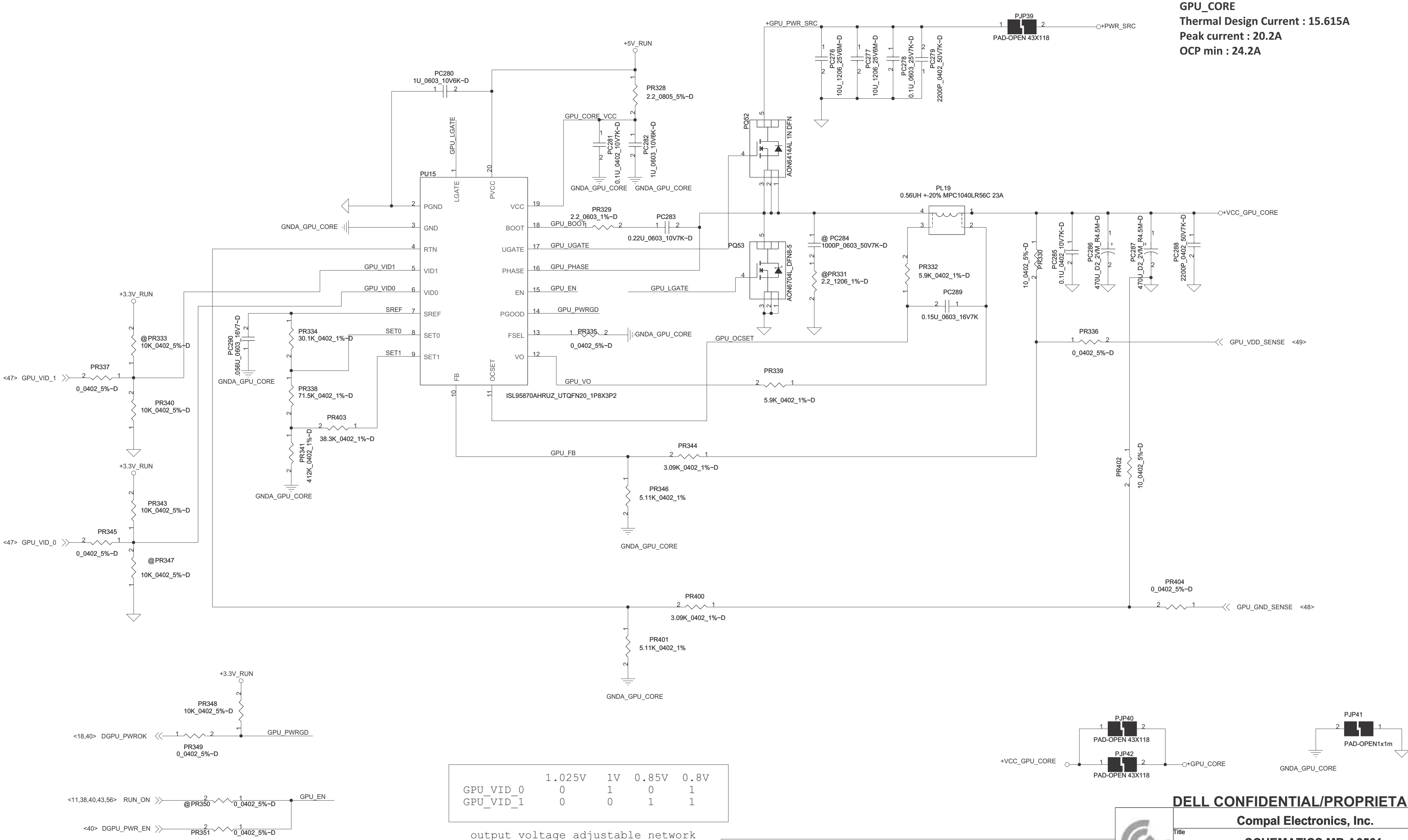
Size | Document Number: 401931 | Rev: B



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	SCHEMATICS,MB A6561
Size	Document Number: 401931
Rev	B
Date:	Thursday, January 13, 2011
Sheet	63 of 77

GPU_CORE
Thermal Design Current : 15.615A
Peak current : 20.2A
OCP min : 24.2A



	1.025V	1V	0.85V	0.8V
GPU_VID_0	0	1	0	1
GPU_VID_1	0	0	1	1

output voltage adjustable network

Compal Electronics, Inc.

Title: **SCHEMATICS,MB A6561**

Size | Document Number: **401931** | Rev: B

Date: Thursday, January 13, 2011 | Sheet 64 of 77

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	7	HW	6/15/2010	COMPAL	Boot issue	Change QC1 control from SUS_ON to RUN_ON_CPU1.5VS3#	X01
2	11	HW	6/15/2010	COMPAL	Modify net name	Change +0.8V_VCC_SA to +VCC_SA	X01
3	22,28,32,40 41,43,11,20 50,38	HW	6/15/2010	COMPAL	Follow PPM recommendation to change material	Change capacitors from 10uF_0805_10V Y5V to 10uF_0805_6.3V_X5R: C305,C387,C462,C705,C728,C760,C764,C765,C768,C769, C772,CC135,CH58,CH73,CH80,CV124,CV126,CV185,CV187 Change capacitors from 10uF_0805_6.3V to 10uF_0603_6.3V: C475,C638,C641,C643 Change resistors to 0402 size: RC134, RH201,RH253,RH208,RH213 Delete RH192 and add PJP66	X01
4	14	HW	6/15/2010	COMPAL	De-pop PCH XDP	De-pop RH1,RH3~RH10,RH12~RH21,RH24,RH283~RH285,CH1	X01
5	14	HW	6/15/2010	COMPAL	Change HDA_SYNC topology	Add QH7 and RH37	X01
6	29	HW	6/15/2010	COMPAL	Change ODD connector from 13 pin to 31 pin	1. Change ODD connector to 31 pin, 2. Remove T157~T167,T169, U87~U89,C1168~C1170,R1181,R508. 3. Add Q123, Q76,R516,R514. 4. Change R510,R1177 power rail to +3.3V_ALW.	X01 X01
8	18	HW	6/17/2010	INTEL	Follow Intel Design Guide Rev1.0	Change RH149 to 1k and RH150 to 4.7k	X01
9	22	HW	6/17/2010	COMPAL	Change EMC4002 to EMC4022	Change U9 to EMC4022, remove R392,R394 R866,R404,C279,R866, Reserve C277	X01
10	25	HW	6/17/2010	COMPAL	Change CRT SW to MAX14885	Change CRT SW to MAX14885 and add C1181,C1182,R1581,remove C325~C336	X01
11	26	HW	6/17/2010	COMPAL	Safety request	Add no stuff D4 and co-lay with F2, change F2 to 2A_8V	X01
12	45	HW	6/17/2010	COMPAL	Change E-SATA repeater to MAX4951BE	Chagne U44 to MAX4591BE and Reserve R1189~R1196 for bypass repeater	X01
13	30	HW	6/17/2010	COMPAL	Change Codec to ZB version.	Change U72 to ZB version as 92HD90B2X5NLGXZBX8 and stuff C962	X01
14	41	HW	6/17/2010	COMPAL	Board ID	Change R875 to 130K	X01
15	34	HW	6/17/2010	COMPAL	Change SI2301BDS to C version	Change Q36 to SI2301CDS	X01
16	34	HW	6/17/2010	BRCOM	Change RFID capacitors for more popular	Change C502,C505 from 1uF to 0.1uF	X01
17	18	HW	6/17/2010	COMPAL	Remove touch screen PAID pull down circuit	Remove RH241	X01
18	47	HW	6/17/2010	COMPAL	BIOS request	Reserve RV29, De-pop DV1, RV29 and pop U14	X01
19	46	HW	6/17/2010	COMPAL	ME request	Change the JBTB1 to TYCO_2041300-2 connector	X01
20	23	HW	6/17/2010	COMPAL	LVDS SW change to PI3LVD400ZFEX	1.Change U84, U85 to PI3LVD400ZFEX 2.Remove Q209,Q210, U91,U90	X01
21	41	HW	6/17/2010	COMPAL	Change BAY_SMBDAT and BAY_SMBCLK pull-up resistors to +3.3V_ALW	Change R854, R856 pull up power rail to +3.3V_ALW	X01

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
22	11,14,41	HW	6/18/2010	COMPAL	EOL concern	Change CC176 to SGA00005H0L, change YH1, Y6 to SJ132P7KW1L	X01
23	42	HW	6/18/2010	COMPAL	Change connector	Change JKB1 to same as JSC1 Change JLED1 to TYCO_1-2041084-6	X01
24	42	HW	6/18/2010	COMPAL	Change TP pin definition	Reverse TP pin definition for PT	X01
25	40,41	HW	6/18/2010	COMPAL	Add series resistor and pull up resistors on MIC_MUTE#, VOL_MUTE,VOL_UP,VOL_DOWN	Add R773,R806,R884,R886,R887,R1169,R1170,R1197	X01
26	24,44	HW	6/18/2010	COMPAL	Correct net name for LED signal	Modify signal name BREATH_BLUE_LED to BREATH_WHITE_LED and BREATH_BLUE_LED_SNIFF to BREATH_WHITE_LED_SNIFF	X01
27	40,47	HW	6/21/2010	NVIDIA	Add HPD circuit to inform system for NV request	Add DV2,DV3,DV4,R1154 and use ECE5028 GPIOE7/DCD# as HPD signal to inform system	X01
28	32	HW	6/21/2010	INTEL	Remove useless resistors	Remove R556, R558, R559, R560 and short the pin1 and pin2 together	X01
29	24,28,30, 32,38,43,50	HW	6/22/2010	COMPAL	Change part for Halogen free	Change Q18,Q27,Q30,Q34,Q38,Q40,Q42,Q49,Q54,Q58,QV5 to HF part	X01
30	10	HW	6/22/2010	COMPAL	To have better return path	De-pop CC130 and pop CC134	X01
31	43	HW	6/23/2010	COMPAL	Solution +1.5V_RUN voltage drop issue	Change Q59 from SI3456BDV to NTGS4141NT1G	X01
32	14	HW	6/23/2010	COMPAL	Add serial damping on SPI_CS0#,SPI_CS1# to avoid SPI EA fail issue	Add serial damping resistor R935 47 ohm on SPI_CS0#, R936 22ohm on SPI_CS1#	X01
33	24	HW	6/25/2010	COMPAL	PT panel change touch screen pin definition	Change JTS1 pin definition for new TS pin define	X01
34	43	HW	6/25/2010	COMPAL	NTMS4107NR2G EOL	Change Q55 to NTMS4920NR2G	X01
35	14	HW	6/25/2010	COMPAL	Follow Intel XDP design	Change RH43,RH44,RH45 to 200 ohm	X01
36	24	HW	6/25/2010	COMPAL	Change LVDS connector to 40 pin	Change JLVDS1 to 40 pin as ACES_59003-0400C-001	X01
37	14,41,29	HW	7/1/2010	COMPAL	Modify Module Bay circuit	1.Remove R1181,R1182,R1189. 2.Change BAY_SMBUS, DEVICE_DET# pull up power rail from +3.3V_RUN to +3.3V_ALW. 3.Change net name ODD_DET# to PCH_SATA_MOD_EN#. 4.Add Q123,Q76,R513,R514,R515 for USB_SMI# circuit. 5.De-pop C627,R712	X01
38	24	HW	7/1/2010	COMPAL	Stuff PWM pull down resistor for PT solution	Pop R1137	X01
39	7	HW	7/1/2010	COMPAL	For support XDP device	De-pop RC9	X01
40	15,18, 40,41	HW	7/1/2010	COMPAL	Base on GPIO map to modify	1. Move SLP_ME_CSW_DEV# from GPIO45 to GPIO28, add MCARD_PCIE_SATA# on 5028 GPIOE3. 2. Remove RH238, change RH80 from 1k to 10k. 3. Change SLICE_BAT_PRES# pull up power rail from +3.3V_ALW2 to +3.3V_ALW. 4. Add R889	X01
41	24	HW	7/1/2010	COMPAL	PWM function	Remove R1139,R1140 and add D68,D69	X01
42	11	HW	7/1/2010	COMPAL	VCCSA VID circuit	Change VCCSA_VID_0 to VCCSA_VID_1 and pop RC138	X01

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
43	22	HW	7/2/2010	COMPAL	Modify thermal diode for thermal request	Remove C268,C269, use DP1/DN1 for CPU,DP2/DN2 for GPU, DP3/DN3 for DIMM, DN5/DP5 for WWAM	X01
44	15,14,47	HW	7/8/2010	COMPAL	Meet Crystal EA chnage caps value.	1. CH18, CH19 change to 10P_0402_50V8J~D 2. CH2, CH3 change to 15P_0402_50V8J~D 3. CV34, CV35 change to 12P_0402_50V8J~D	X01 X01
45	47	HW	7/8/2010	COMPAL	U14 power pin add 0.1uF bypass cap.	Add CV188 0.1uF CAP at U14.5 pin	X01
46	36	HW	7/12/2010	COMPAL	O2 suggest 1. add the damping resistors 33ohm on the (SD/MMCDAT0-7 and SD/MMCCMD) 2. change the resistor RE7 on the SD/MMC_CLK to 33ohm. 3. OZ600RJ1N rev.B PE_REXT change resistor	1. Add R1198~R1206 33 ohm 2. RE7 change to 33 ohm 3. R680 chnage to 191 ohm	X01 X01
47	45,29	HW	7/12/2010	COMPAL	EMC request 1.Add 90 ohm common mode choke L50,L51 at USBP0+/- and USBP1+/- for USB R/W noise 2. Reserve 150pF bypass capacitor at ODD DEVICE_DET# 3.Add 220ohm Bead at DMIC_CLK for DMIC noise 4.Add 0 ohm at BIA_PWM_LVDS check UMA mode whether have PCI noise	1. L51,L50 change to POP, R734~R737 change to De POP. 2. Reserve CH7 150P 3. add LE2 220 ohm bead instead of R1106. 4. add RE9 0 ohm at BIA_PWM_LVDS	X01
48	24,45	HW	7/13/2010	COMPAL	PPM recommendation to change material	1.C300, C669 from 10U 16V Y5V 1206 change to 10U 10V Z Y5V 0805	X01
49	41	HW	7/13/2010	COMPAL	SMSC request 1.I2S_CLK, I2S_WS pull down resistors depopulated	R864 and R865 can be depopulated	X01
50	33	HW	7/15/2010	COMPAL	Hi-Pot EA Fail	JLOM1.14 change to NC, JLOM1.15 change to GND net,Remove C1165,C1166	X01
51	37,44	HW	7/15/2010	COMPAL	Modify LED circuit	Remove R1578,R1579,R1580,D42,D60,D61, add Q77,Q124,R705,R718,R719	X01
52	26	HW	7/15/2010	COMPAL	Meet HDMI EA, EMI	1.L19,L20,L21,L22 change to Populated 2.R470,R471,R468,R469,R462,R466,R451,R459 change to Depopulated	X01
53	37	HW	7/15/2010	COMPAL	MINI card CONN from H9.9 change to H9	JMINI1,JMINI2,JMINI3 change to LOTES_AAA-PCI-047-P10-A	X01
54	44	HW	7/15/2010	DELL	1.Remove MIC MUTE LED circuit, 2.Reserve SPK MUTE LED circuit	1.Remove the R1108,Q119,R1061,Q105 parts as MIC mute circuit 2.Reserve the R1109,Q119,Q102,R1059 parts as SPK mute circuit, Change Q119 to SSM3K7002FU	X01
55	14,17,18 40,41	HW	7/16/2010	COMPAL	Follow GPIO MAP	1.Remove R1567~R1577. 2.U46.B64,A9,A18,A44,B39,B51 connect to GND direct. 3.R796 Net rename to DYN_TURB_PWR_ALRT# then change to 10K value and pull up to +3.3V_ALW power rail. 4.Add GPIO DYN_TUR_CURRNT_SET# TO U51.A35 and add R1171 10k pull up. 5.SIO_EXT_SMI# GPIO form PCH.GPIO1 change to PCH.GPIO14 and add RH51 10kohm Pull up 6.RH164 change to PCH_GPIO1 net. and remove RH254	X01
56	33	HW	7/19/2010	COMPAL	ME change reuqest	JLOM1 change to TYCO_2010019-3	X01

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
57	36	HW	7/19/2010	COMPAL	OZ600RJ1 from A change to B version	U39 change to OZ600RJ1LN-B_QFN48	X01
58	20,43	HW	7/19/2010	COMPAL	Cost reduction as +3.3V_ALW_PCH and +5V_ALW_PCH power control circuit	1.Add PJP68 bypass JUMP for +5V_ALW to +5V_ALW_PCH 2.QH4,CH98,RH278 change to NON-POP 3.Add PJP67 bypass JUMP for +3.3V_ALW to +3.3V_ALW_PCH 4.Q51,R907,R905,C762,C760,R908,Q49 change to NON-POP	X01
59	24	HW	7/20/2010	COMPAL	Add BIA_PWM_GPU to control BIA_PWM_LVDS	D63 change to POP	X01
60	24	HW	7/20/2010	COMPAL	Meet LCD power sequence spec	R413 change to 470 ohm	X01
61	24	HW	7/20/2010	COMPAL	Corrent Touch screen pin define	Modify JTS1 pin define	X01
62	29	HW	7/20/2010	COMPAL	Q107 change to one channel	Q107 change to SSM3K7002FU_SC70-3~D	X01
63	47	HW	7/20/2010	NV	Follow NV request	Add @RV103,RV104, @RV20,@RV25,@RV26	X01
64	17,30,39	HW	7/20/2010	COMPAL	EMC team request	1.I2S_12MHZ add @RE13 2.I2S_BCLK add @RE10. 3.CLK_PCI_DOCK, RH103 change to 33ohm, R756 change to 33 ohm, C704 change to 12pf 4.DAI_BCLK# add@RE12,@CE9 5.DAI_12MHZ# add @RE11,@CE8	X01
65	26	HW	7/21/2010	COMPAL	Safety team request	Modify HDMI power circuit about D4,F2,R5 parts	X01
66	37	HW	7/21/2010	COMPAL	DF398754 Debug reserve	Reserve R725 0 ohm both PCIE_MCARD2_DET#R to PCIE_MCARD2_DET#	X01
67	36	HW	7/21/2010	COMPAL	Meet 1394 EA SPEC	R683,R684,R685,R686 from 56.2 change to 53.6 ohm	X01
68	36	HW	7/21/2010	COMPAL	Add MS card function	Modify U39 and JSD1 circuit	X01
69	30	HW	7/22/2010	COMPAL	EMI snubber and change Audio net name	1.Change net name from I2S_12MHZ to I2S_MCLK 2.Reserve R1587~R1590 part at INT_SPK bus	X01
70	41	HW	7/22/2010	COMPAL	New GPIO MAP	1.Pull up R943 to +3.3V_ALW on XFR_ID_BIT# of ECE5055-GPIO105 2.R712,R711,C627 change to de-pop	X01
71	40	HW	7/23/2010	COMPAL	TEMP_ALERT# Add 0 ohm jump between EC to PCH	Add R738 ohm at TEMP_ALERT#	X01
72	24,42	HW	7/24/2010	COMPAL	Follow GPIO map to add touch screen power down control circuit	Add TOUCH_SCREEN_PD#, Q125,Q32,R430,R431,C304,C306, and change JTCH1 pin 1,pin2 from +5V_RUN to +5V_TSP	X01
73	24	HW	7/26/2010	COMPAL	Reserve a 0 ohm option between +5V_RUN and +5V_TSP	Reserve R1001 0 ohm 0603 between +5V_RUN and +5V_TSP	X01
74	44	HW	7/26/2010	COMPAL	Due to BT_ACTIVE was folating pin, so, add 100 Kohm pull down	Add R944 100K ohm for BT_ACTIVE pull down	X01
75	49	HW	7/28/2010	NV	Follow NV suggestion to modify BOM	De-pop CV184, and change CV183 to 1uF,CV182 to 4.7uF, CV109 to 470pF,CV110 to 4700pF, LV8 to 100nH	X01

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
76	24	HW	9/06/2010	COMPAL	In order to use the HF part.	Q21 change SB000009K0L to SB000009K1L	X02
77	14,18	HW	9/06/2010	Intel	Follow Intel request	Add RH52 and RH53.	X02
~~78~~	~~38,45~~	~~HW~~	~~9/15/2010~~	~~COMPAL~~	~~For the part consist issue.~~	~~L49,L50,L51 change SM01002080L to SM070001E0L~~	~~X02~~
79	45	HW	9/17/2010	COMPAL	Remove Bypass ESATA Repeater schematic, because Gen1 EA fail when Bypass ESATA Repeater.	Remove R1189~R1196.	X02
80	15,36	HW	9/17/2010	H.ELE.	YH2's CL value can't match cd & cg value. Y5's value too low that frequency shift of PCB board.	CH18 & CH19 change from 10P to 22P, C591 & C592 change from 10P to 6.8P.	X02
81	47,48,49 50,51,52	HW	9/21/2010	DELL	Macallan DIS performance request.	UV change from N12M to N12P.	X02
82	30	HW	9/23/2010	IDT	MIC detect issue.	U72 change version from SA00003ZZ1L(ZB) to SA00003ZZ2L(YA).	X02
83	47	HW	9/23/2010	COMPAL	De-pop pull up resistors	De-pop RV23,RV24	X02
84	18	HW	9/23/2010	Intel	Follow Intel design guide Rev1.2	Change RH149 to 2.2k and RH150 to 0 ohm	X02
85	32	HW	9/23/2011	Intel	Intel request	U31 change version from WG82579LM QMWM A2 to WG82579LM QNGP C0.	X02
86	15,32	HW	9/24/2011	H.ELE.	modify item 80 YH2's CL value can't match cd & cg value.	CH18 & CH19 change from 22P to 10P and YH2 change from CL=18pF to CL=12pF. C470 & C471 change from 33P to 18P and Y3 change from CL=18pF to CL=12pF.	X02
87	34	HW	9/24/2011	Broadcom	Broadcom request	Add decouping cap C556 for U35 on layout.	X02
88	24	HW	9/24/2011	COMPAL	The PWM can not function correct.	R1137 change from 100K to 10K.	X02
89	41	HW	9/24/2011	EPSON	The frequency skew of Y6 is too big in Normal temperature.	C741 & C743 change from 33P to 39P,	X02
90	36	HW	9/25/2011	COMPAL	Correct the 53.6 ohm into L end part number.	Change the R683,R684,R685,R686 to SD00000HE8L	X02
91	46	HW	9/25/2011	COMPAL	Add bypass cap at IO board connector of MB side.	Add bypass cap C1183 at +5V_ALW.	X02
92	38	HW	9/25/2011	COMPAL	Correct the Express Card PWR S/W into L end part number.	Change the U41 to SA00001SL2L.	X02
							X03

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
93	47,48,49 ,51,52	HW	9/27/2010	NVIDIA	NVIDIA request.	1. CV160~CV162 change to 1uF 2. Change CV41/42/43/50/51 to 0.022u 3. Change CV40/58/59/60 to 0.1u 4. No stuff CV58/44 on DSC 5. Change CV181 to 22uF_0805 6. Change +SP_PLLVDD to +PLLVDD and remove CV182,CV183,CV184,CV115,LV8 7. Change LV3 to SM01000BE0L 8. Change CV34/35 to 18pF 9. Reserve 1x1mm jumper and contact to PEX_SVDD_3V3. 10. CV90 placement under GPU 11. Change CV80 to 4.7u. 12. Add 2pcs of 1uF per VRAM 13. Change RV81,RV86 to 160_1% 14. Add 10K pull-down to UV1.J5 15. Add 40.2K_1% pull down on UV1.T6	X02
94	36	HW	9/28/2010	O2Micro	O2Micro request.	1. Move C582 to +MMI_1394_VCCH and close to either one pin 28 or pin 33. 2. Move C581 to +MMI_PE_VDDH and close to pin1. 3. Add a 0.01uF capacitor on +MMI_PE_VDDH and close to pin1.	X02
95	30,31	HW	9/30/2010	IDT	To solve pop noise and detect issue	Add U6,Q33,Q46,D70,D71,R425,R33,R38,R424,R161,R352,R1088,C967,C307,C308 Q107 change from SB00000960L(3pin) to SB00000DH0L(6pin)	X02
96	30	HW	9/30/2010	COMPAL	EMC request	Add bypass cap C1185~C1188	X02
97	14,09	HW	10/04/2010	Intel	Following Intel DG ver1.5	1. Add RH31 pull down resister. 2. RC96,RC97 no stuff	X02
98	34	HW	10/04/2010	Broadcom	Broadcom request(enhancement current amount)	L39 & L40 change from SHI00005Y0L(0603 size) to SHI0000CH0L(0805 size rate current is 400mA).	X02
99	11	HW	10/04/2010	COMPAL	Change QC5 VGS MAX rating from 12V to 20V	Change QC5 from SB52302028L to SB00000HK0L	X02
100	24,26,47	HW	10/04/2010	COMPAL	Change RB751V to HF part	Change D53,D63~D69,DV1~DV4 to SCS00004L0L	X02
101	7,18,41	HW	10/04/2010	COMPAL	For cost saving	Remove RH159,RH261	X02
102	30	HW	10/06/2010	COMPAL	1. Sync-up with Macallan 14" 2. EMC request	1. Remove R1587~R1590, C1185~C1188, change R1183~R1186 to L91~L94 2. Change Audio signal's diode from 4 of 2pins(SD05.TCT) to 2 of 3pins (PESD5V0U2BT SCA00000T0L)	X03
103	38	HW	10/06/2010	COMPAL	In order to enable Express Card PWR S/W 2nd source vendor "GMT" to act.	Add connection of pin4,pin5,pin13 and pin14 to power net.	X03
104	26	HW	10/06/2010	COMPAL	Follow safety request	Pop F2 and de-pop R5	X03
105	53,14	HW	10/06/2010	COMPAL	Remove PAID function of RTC	1. JRTC1 change from 3pin to 2pin(SP02000CA0L) and remove detect pin 2. UH4.C36 & RH355.2 rename from RTC_DET# to PCH_GPIO33	X03

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
106	29	HW	10/06/2010	COMPAL	For power saving	Increase JSATA2 detect pin R1177 from 1k to 100kohm	X03
107	46	HW	10/07/2010	COMPAL	For NB board space consider.	Remove page46 two block MIC detect schematic to IO/B.	X03
108	28	HW	10/07/2010	COMPAL	For cost saving	De-pop the R505,Q28,R500,R499,C393,C394,R504 parts.	X03
109	32	HW	10/07/2010	COMPAL	Based on IEEE Return Loss EA fail	L30~L37 change from SHI00004O0L(22NH) to SHI00005I0L(12NH)	X03
110	28	HW	10/07/2010	COMPAL	Based on support SSD HDD	Add +3.3V_RUN on JSATA1 pin8,pin9,pin10	X03
111	47	HW	10/07/2010	COMPAL	solve systen can't boot in UMA only mode.	correct from U14 to UV14 and change the PN to SA00003Y00L. pop RV29.	X03
112	30,32,40 42	HW	10/07/2010	COMPAL	GPIO MAP update at 1-Oct-10	1. Add U15, C478 that defect RJ45 cable insert or not if plug in then close WLAN power. 2. 5048 GPIOB7 rename from AUD_NB_MUTE to AUD_NB_MUTE#	X03
113	18,30	HW	10/08/2010	COMPAL	Remove PAID function of speaker	1. JSPK1 change from 6pin to 4pin(LTCX002V50L) that remove detect pin 2. UH4.D40 & RH269.2 rename from SPEAKER_DET# to GPIO17	X03
114	48,49	HW	10/08/2010	nVIDIA	Follow nVIDIA suggest	1.Move CV74 to contact +3.3V_RUN_VDD33 not +3.3V_RUN_GFX 2.RV41 change to 4.99K 1% and RV99 change to 20K 1%.	X03
115	44	HW	10/11/2010	COMPAL	LED brightness test result	change R957 to 1K, R955, R941, R949, R939, R934 to 4.7K	X03
116	41	HW	10/11/2010	COMPAL	BORAD_ID	change R875 to 62K.	X03
117	17	HW	10/11/2010	Intel	Follow Intel check list Rev1.2	Add @RH332	X03
118	31,41	HW	10/12/2010	DELL	DELL DM Dennis has confirmed.	No stuff “Latitude On” button of SW2,R877,C740	X03
119	24,45	HW	10/13/2010	COMPAL	EMC request(for cost saving)	1.UE1,UE2,U13,U86 change from PRTR5V0U2X(SOT143-4)(4pin)to PESD5V0U2BT(SOT23-3)(3pin) SCA00000T0L. 2.Diode for UE1,UE2 shall be added, not reserved. 3.Rename UE1 to D73,UE2 to D72,U86 to D74,U13 to D75	X03
120	28	HW	10/13/2010	COMPAL	Follow 14"	PJP71 size change to 1X1	X03
121	7	HW	10/14/2010	COMPAL	UC1.4 is OD pin,so remove pull down R.	Remove RC11	X03
122	22,47,48 49	HW	10/14/2010	nVIDIA	Follow nVIDIA suggest	1.Change R1111 to 10K for power saving. 2.No stuff of CV188,RV50,CV159 and stuff of RV56,RV41,RV99,CV58 3.Change RV51 to 45.3K, CV109 & CV110 to 0.1uF	X03
123	30	HW	10/14/2010	COMPAL	Audio team Paul’s agree the EMI solution.	Stuff of C973~C976	X03
124	28	HW	10/15/2010	COMPAL	MikeCC suggest	Stuff of R505,C394,R504	X03
125	14,18	HW	10/19/2010	COMPAL	Follow Intel debug port DG	Connect PCH_GPIO15 to PCH XDP_FN16	X03
~~126~~	~~30~~	~~HW~~	~~10/19/2010~~	~~COMPAL~~	~~Change Mic detect to external detect~~	~~Remove R161 and add C1165~~	~~X03~~
127	51,52	HW	10/25/2010	DELL	DELL request	Change VRAM from 128Mx16 to 64Mx16	X03

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
128	30	HW	11/10/2010	COMPAL	Modify Mic detect circuit	1.Move C1180 to +VREFOUT_R 2.No stuff C967,R352,R1088	X04
129	14~21	HW	11/10/2010	COMPAL	Change PCH stepping	Change UH4 to B2 stepping	X04
130	18	HW	11/16/2010	COMPAL	Follow check list Rev1.0	Change RH177 from 1k to 10k	X04
131	15	HW	11/16/2010	COMPAL	To fix ME issue (transition fail S3/Moff->S3/M3)	De-pop RH296,RH297; pop QH5,RH302,RH303	X04
132	47	HW	11/19/2010	NV	Solve HDMI audio issue	De-pop RV41, change RV97 to 34.8K and stuff it	X04
133	47	HW	11/19/2010	NV	Chagne Device ID to 0x1056	De-pop RV51,change RV57 to 34.8k and stuff De-pop RV60, change RV54 to 10k and stuff it, change RV52 to 4.99k	X04
134	47,48, 49,50	HW	11/19/2010	NV	Change GPU to QS sample	Change UV1 to N12P-NS-S-A1	X04
135	28	HW	11/19/2010	Intel	Follow Intel CRB design	Change R501,R502 to 10k	X04
136	38	HW	11/19/2010	COMPAL	To fix soldering issue	Change express card connector JEXP1 to TAISOL 5-421005002000-9	X04
137	45	HW	11/19/2010	COMPAL	To fix pericom ESATA Repeater that PA internal pull high.	Stuff R745 that channel A from preemphasis to standard SATA of Pericom.	X04
138	47	HW	11/26/2010	COMPAL	Correct the DGPU_HOLD_RST# behavior.	Reserve Pull-up resistor RV30 to DGPU_HOLD_RST#,but de-pop RV30.	X05
~~139~~	~~14~~	~~HW~~	~~11/26/2010~~	~~COMPAL~~	Remove Resistor between +3.3V_ALW_PCH_JTAG and +3.3V_ALW_PCH.	~~Remove RH288.~~	~~X05~~
140	41	HW	12/06/2010	COMPAL	Follow INTEL DG1.5 RSMRST# timing cicuit	Just add RSMRST# circuit for backup. but de-pop.	X05
141	18	HW	12/07/2010	COMPAL	GPIO17 for interior MIC and exterior MIC detect function.	Reserve pull-down resistor RH273 to GPIO17,but De-pop RH273.	X05
142	41	HW	01/07/2011	COMPAL	BOARD ID.	Change R875 from 62k to 33k.	A00
143	35	HW	01/07/2011	COMPAL	PWM and backlight timing issue.	Reserve 74AHC125 circuit for BIA_PWM_GPU, but de-pop.	A00
144	35	HW	01/07/2011	COMPAL	Modify TPM/TCM configuration table.	Update USH BCM5882 and China TCM Z8H172T Option table.	A00
145	ALL	HW	01/11/2011	COMPAL	For cost saving	Change 119pcs 0402 0 ohm resistors and 3pcs 0603 0 ohm footprint to new footprint which is short pin1 and pin2 .	A00

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	54	+3V/+5V	7/5	Compal	+3.3V phase node over Mosfet Vds rating	Change PQ6 from SI4128 to AO4466L. Change PQ8 from SI4134 to AO4712L.	
2	62	0.8V_VCCSA	7/5	Intersil	VCCSA spike issue	Remove PR264 and add PR410 connect PR249.1 to do PD. Remove VCCSA_VID_0 net to connect PR249.1 and change net name to VCCSA_VID_1 Change PR250 from 34K to 113K Change PR256 from 0 to 140K Change PR261 and 265 from 2.49K to 0 ohm. Change PD resister PR266 and PR410 to 1K. Depop PR249, PR260 and PR267 Change PR259 from 274K to 47.5K	
3	53	+DCIN	7/19	Compal	Add 150pF bypass capacitor for PCI noise	Add PC400 to connect PR14.1 and gnd	
4	55	+1.5V_SUS	7/19	Compal	Vendor will not support this part	Change PC56 and PC57 to 330U/9m/2V (SGA20331E0L) from 330U/9m/2.5V (SGA19331D1L)	
5	53	+DCIN	7/19	Compal	PL3 and PL4 current rating is not enough for 130W adapter	Change PL3 and PL4 to FBMA-L18-453215-900LMA90T (SM01002078L) from FBMJ4516HS720NT(SM010009C8L)	
6	53	+DCIN	7/19	Compal	PL1 current rating is not enough for 9cell (3.0Ah 1C) discharge current	Change PL1 to FBMJ4516HS720NT(SM010009C8L) from FBMA-L18-453215-900LMA90T (SM01002078L) Add PL22 FBMJ4516HS720NT(SM010009C8L) Take off PJP45	
7	53	+DCIN	7/19	Compal	PR16 down size to 0402 from 0805	Change PR16 to 100k/0402 (SD02810038L) from 100k/0805 (SD01510038L)	
8	54	+3V/+5V	7/19	Compal	PC24 down size to 0603 from 0805	Change PC24 to 4.7u/6.3V/0603 (SE107475K8L) from 4.7u/6.3V/0805 (SE093475K8L)	
9	55	+1.5V_SUS	7/19	Richtek	Reserve 300K PD to avoid VR turn on when EN/DEM is floating.	Add PR508 to do PD from PU3 pin1	
10	61	Charger	7/19	Compal	solve leakage issue	Change PD14 to ES2AA-13-F (SC100005A0L) from SBR3A40SA-13_SMA2 (SC100003J00)	
11	63	Selector	7/19	Compal	solve leakage issue	Change PD16 to ES2AA-13-F (SC100005A0L) from SBR3A40SA-13_SMA2 (SC100003J00)	
12	58	+1.05V_VTT	7/19	Compal	Remove PC147 for ME Interfere	Remove PC147	
13	62	0.8V_VCCSA	7/19	Compal	VCCSA phase node over Mosfet Vds rating	Change PQ35 from SI4128 to AO4466L. Change PQ36 from SI4172 to AO4712L.	
~~14~~	~~59~~	~~VCORE~~	~~7/19~~	~~MAXIN~~	~~Fine tuning VCORE Load Line~~	~~Change PR140 to 11.8k(SD03411828L) from 12.6k(SD00000AJ8L)~~	
15	59	VCORE	7/19	MAXIN	Reserve 33nF cap parallel with PC136 to fine tuning VCORE transient	Add PC401 33nF/16V/X7R/0402(SE076333K8L)	
~~16~~	~~59~~	~~VCORE~~	~~7/19~~	~~MAXIN~~	~~Fine tuning VGFX Load Line~~	~~Change PR157 to 8.2k(SD00000418L) from 8.66k(SD03486618L)~~	
17	60	VGFX	7/19	MAXIN	Add 33nF cap parallel with PC208 to fine tuning VGFX transient	Add PC402 33nF/16V/X7R/0402(SE076333K8L)	

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
18	61	Charger	7/21	Compal	Reserve adapter protection circuit for turbo mode	Change PU11 pin1 net name to ICREF from GNDA_CHG Change PU11 pin26 net name to ICOUT from VCC Reserve PR511,PR512,PR513,PR514,PC406,PQ59,PR515,PR516.PR517,PC407 PC244,PC245,PR518,PR519,PR520.PQ43,PC405,PR509,PR510	X01
19	61	Charger	7/21	Compal	PQ27 body diode can handle surge current when adapter plug in so depop PD14	Depop PD14 SBR3A40SA (SC100003J00)	X01
20	59	VCORE	7/23	MAXIN	For Pass2 VCORE & VGFX OCP setup	Change PR126 & PR127 to 165K from 150K Change PR134 & PR135 to 105K from 100K	X01
21	59/~~60~~	VCORE/~~VGFX~~	7/23	MAXIN	Setting change for ICC version change	Change PR118 to 1 ohm from 2 ohm ~~Change PR119 to 1 ohm from 2 ohm~~	X01
22	61	Charger	7/28	TI	Pop adapter protection componment for turbo mode with TI solution	Pop PR513 100k (SD03410038L) Pop PR514 78.7k (SD03478728L) Pop PR512 115k (SD03411538L) Pop PR511 1.87M () Pop PQ59 RHU002N06 (SB50206008L) Pop PR510 100K (SD02810038L) Pop PC406 100P (SE071101J8L)	
23	57	+1.05VM	10/18	TI	Fine tune OCP setting	Change PR83 to 22k (SD03422028L) from 10k (SD03410028L)	
24	63	Selector	10/18	Compal	Change parts to HF parts	Change PQ39 and PQ44 SI4835DDY-T1-GE3 (SB00000FF1L) from SI4835DDY-T1-E3 (SB00000FF0L)	
25	61	charger	10/18	Compal	Fine tune adapter protection circuit to reserve H_PROCHOT#	Depop PR814	
26	57	+1.05VM	10/18	Compal	22u/1206/6.3V COS issue	Change PC98 ~ PC105 to 22u/0805 (SE00000110L) from 22u/1206 (SE077226M8L)	
27	58	+1.05VTT	10/18	Compal	22u/1206/6.3V COS issue	Change PC123 ~ PC125, PC121, PC127, PC120, PC129 and PC130 to 22u/0805 (SE00000110L) from 22u/1206 (SE077226M8L) Change PC122 and PC126 to 47u/0805 (SE00000G60L) from 22u/1206 (SE077226M8L)	
28	53	DCIN	10/18	Compal	6 ~ 7mA leakage current in slice	Change PR2 and PR504 to 100K (SD02810038L) from 10K (SD03410028L)	
29	64	GPU_Core	10/18	nVidia	Fix output voltage to 0.9V for nVidia ES sample	Depop PR337 and PR345 0 Ohm (SD02800008L) Depop PR347 10K (SD02810028L) Pop PR343 10K (SD02810028L)	
30	64	GPU_Core	10/18	Compal	Change OCP setting for new nVidia chip	Change PR332 and PR339 to 5.9k (SD03459018L) from 4.22k (SD03442218L)	
31	62	VCCSA	10/18	Compal	Fine tune VCCSA OCP setting for 2nd and 3rd source choke	Change PR247 and PR262 to 12.7k (SD03412728L) from 11.5k (SD03411528L)	
32	64	GPU_Core	11/11	nVidia	Change VID setting for new nVidia chip. Defult set 1V.	Depop PR347 10K (SD02810028L) Pop PR343 10K (SD02810028L) Change PR344 and PR400 to 3.09k (SD00000J38L) from 3.57k (SD03435718L) Change PR341 to 412k (SD00000678L) from 402k (SD034402380) Change PR403 to 38.3k (SD03438328L) from 200k (SD03420038L) Change PR338 to 71.5k (SD03471528L) from 0 Ohm (SD02800008L) Change PR334 to 30.1k () from 23.7k (SD03423728L)	

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
33	63	Selector	11/11	Compal	Fine tune main and media battery switching to slice battery transient time	Change PC270 and PC265 to 0.22uF (SE000005Z8L) from 1uF (SE00000698L)	
~~34~~	~~61~~	~~Charger~~	~~11/11~~	~~Compal~~	~~Change adapter protection circuit trip point. (Adapter rated current + 0.75A)~~	~~Change PR512 to 107k (SD03410738L) from 115K (SD03411538L)~~ ~~Change PR511 to 649K (SD03464938L) from 1.87M (SD00000WN0L)~~ ~~Change PR514 to 80.6K (SD03480628L) from 78.7k (SD03478728L)~~	
35	61	Charger	11/11	Compal	Change adapter protection event to HW from SW	Pop PR522 0 Ohm (SD02800008L) Depop PR521 0 Ohm (SD02800008L) Depop PR510 100k Ohm (SD02810038L)	
36	60	VGFX_core	12/08	Compal	Fine tune the GFX initial voltage to solve offset	Change PR119 to 0 ohm (SD01300008L) from 1 ohm (SD014100B8L)	
37	59	VCORE	12/08	Compal	Fine tuning VCORE Load Line	Change PR140 to 12.4k(SD00000AJ8L) from 11.8k(SD03411828L)	
38	61	Charger	12/10	Compal	H_PROCHOT# can not pull high issue with external circuit at DC mode	Change PR513.1 net nam to +3.3V_ALW2 from MAX8731_REF Change PQ59.3, PR514.2 and PC406.2 net nam to PGND from GAND_CHG	
39	61	Charger	12/10	Compal	H_PROCHOT# pull low level can not meet Intel SPEC with TI solution at AC mode	Depop PR511 (SD03464938L) Change PR512 to 174k (SD03417438L) from 107k (SD03410738L) Change PR513 to 150k (SD03415038L) from 100k (SD03410038L) Change PR514 to 113k (SD03411338L) from 80.6K (SD03480628L) Pop PR515, PR517,PR520 0 Ohm (SD02800008L) Pop PQ43 RHU002N06 (SB50206008L) Pop PR519 221K (SD00000HX8L) Pop PR518 1.8M (SD00000K180) Pop PR516 20K (SD03420028L) Depop PR509 (SD02800008L)	
40	59	VCORE	12/10	Compal	Fine tune the GFX Load Line	Change PR157 to 8.06K ohm (SD03480618L) from 8.2K ohm (SD00000418L)	

Compal Electronics, Inc.
Title: SCHEMATICS,MB A6561
Size | Document Number: 401931 | Rev: B
Date: Thursday, January 13, 2011 | Sheet 77 of 77