# Compal LA-C293P

## B/N series AMD
## Carrizo/Carrizo-L
## DIS M/B Schematics Document

### AMD Exo Pro

**REV：1.0**

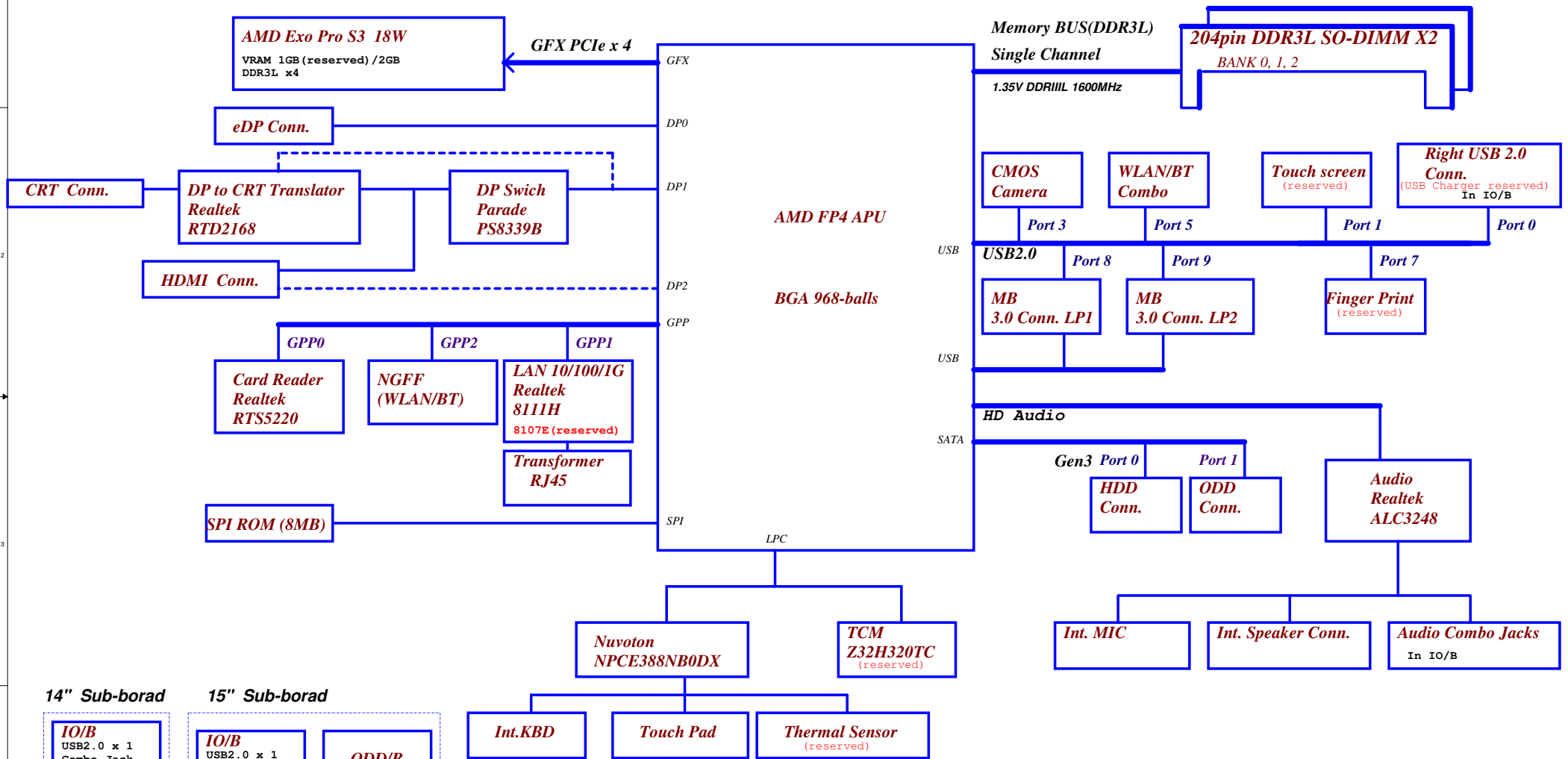
**2015-03-06**



| Compal Electronics, Inc. | | | |
|---|---|---|---|
| Title: Cover Page | | | |
| Size: C | Document Number: LA-C293P | | Rev: 1.0 |
| Date: Monday, March 09, 2015 | Sheet 1 of 48 | | |

Carrizo only

# AMD Carrizo/Carrizo-L




**14" Sub-borad**

- IO/B
  USB2.0 x 1
  Combo Jack
  Novo button
- LED/B
- 14" Power/B

**15" Sub-borad**

- IO/B
  USB2.0 x 1
  Combo Jack
  Novo button
- ODD/B
- LED/B
- Battery/B
- 15" Power/B

| | | | |
|---|---|---|---|
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Title: BLOCK DIAGRAMS

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## Voltage Rails

| Power Plane | Description | S0 | S3 | S5 |
|---|---|---|---|---|
| VIN | Adapter power supply (19V) | ON | ON | ON |
| B+ | AC or battery power rail for power circuit. | ON | ON | ON |
| +APU_CORE | Core voltage for APU | ON | OFF | OFF |
| +APU_CORE_NB | Voltage for On-die VGA of APU | ON | OFF | OFF |
| +VGA_CORE | 0.95-1.2V switched power rail | ON | OFF | OFF |
| +3VALW | 3.3V always on power rail | ON | ON | OFF |
| +3VS | 3.3V switched power rail | ON | OFF | OFF |
| +1.8VALW | 1.8V always on power rail | ON | ON | ON* |
| +1.8VS | 1.8V switched power rail | ON | OFF | OFF |
| +0.95VALW | 0.95V always on power rail | ON | OFF | OFF |
| +0.95VS | 0.95V switched power rail | ON | OFF | OFF |
| +1.35V | 1.35V power rail for APU and DDR | ON | ON | OFF |
| +1.5VS | 1.5V switched power rail | ON | OFF | OFF |
| +3VGS | 3.3V switched power rail for VGA | ON | OFF | OFF |
| +1.8VGS | 1.8V switched power rail for VGA | ON | OFF | OFF |
| +1.35VGS | 1.35V switched power rail for VGA | ON | OFF | OFF |
| +0.95VGS | 0.95V switched power rail for VGA | ON | OFF | OFF |
| +5VALW | 5V always on power rail | ON | ON | ON |
| +5VS | 5V switched power rail | ON | OFF | OFF |
| +RTC_APU | RTC power | ON | ON | ON |
| +0.675VS | 0.675V switched power rail for DDR terminator | ON | OFF | OFF |

## USB OC MAPPING

| OC# | USB Port | |
|---|---|---|
| 0 | USB2 port0 | |
| 1 | USB2 port6,7 | USB3 port2,3 |
| 2 | | |
| | | |

| STATE \ SIGNAL | SLP_S3# | SLP_S5# | +VALW | +V | +VS | Clock |
|---|---|---|---|---|---|---|
| Full ON | HIGH | HIGH | ON | ON | ON | ON |
| S3 (Suspend to RAM) | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | ON | OFF | OFF | OFF |

## SMBUS Control

| | SOURC | | | | | | |
|---|---|---|---|---|---|---|---|
| EC_SMB_CK1<br>EC_SMB_DA1 | EC 388N<br>+3VLP | X | V<br>+3VLP | X | X | X | X |
| APU_SCLK0<br>APU_SDATA0 | APU<br>+3VS | X | X | V<br>+3VS | X | X | X |
| EC_SMB_CK2<br>EC_SMB_DA2 | EC 388N<br>+3VS | V<br>+3VS | X | X | X | V<br>+3VS | V<br>+3VS |

## APU PCIE PORT LIST

| Port | Device |
|---|---|
| | |
| 1 | LAN |
| 2 | WLAN |
| 3 | |

## BOM Structure Table

| BOM Structure | BTO Item |
|---|---|
| 45@ | for HDMI Logo |
| 14@ | for 14" componect |
| 15@ | for 15" componect |
| PX_CZL@ | GFX GEN2 caps for PX CZL |
| PX_CZ@ | GFX GEN3 caps for PX CZ |
| CZ@ | For CZ APU BOM |
| CZL@ | For CZL APU BOM |
| A8@ | |
| A6@ | |
| A4@ | |
| | |
| E1@ | |
| UMA@ | UMA part |
| | |
| EXO@ | |
| MESO@ | |
| CMOS@ | |
| HDMI@ | |
| 8107E_LDO@ | |
| 8107E_SW@ | |
| 8111H_LDO@ | |
| 8111H_SW@ | |
| TS@ | Touch Screen |
| ZODD@ | Zero Power ODD part |
| NOZODD@ | Non-Zero Power ODD part |
| CHG@ | USB Charger function |
| NOCHG@ | Non-USB Charger function |
| FHD@ | Full HD Panel |
| CRT@ | CRT BOM |
| USB3@ | USB 3.0 |
| EX_THM@ | External Thermal sensor |
| NOTCM@ | NOTCM componets |
| TCM@ | TCM componets |
| ME@ | ME part |
| EMIP@ | EMI pop component |
| EMIU@ | EMI Un pop component |
| ESDP@ | ESD pop component |
| ESDU@ | ESD Un pop component |
| @ | Unpop |

## USB Port Table

| USB 2.0 | USB 3.0 | | Port | 3 External USB Port |
|---|---|---|---|---|
| EHCI | | | 0 | RIGHT USB |
| | | | 1 | Touch Screen |
| | | | 2 | Finger Print |
| | | | 3 | Camera |
| | | | 4 | |
| | | | 5 | WLAN/BT Combo |
| | XHCI | 2 | 6 | LEFT USB3.0 |
| | | 3 | 7 | LEFT USB3.0 |

## EC SM Bus1 address

| Device | Address | HEX |
|---|---|---|
| Smart Battery | 0001 011X b | 16H |
| | | |
| | | |
| | | |

## EC SM Bus2 address

| Device | Address | HEX |
|---|---|---|
| Thermal Sensor | 1001 101X b | 9AH |
| SB-TSI (APU) | 1001 100X b | 98H |
| | | |
| VGA Internal Thermal | 1000 001X b | 82H |
| | | |

## APU SM Bus address

| Device | Address | HEX |
|---|---|---|
| DDR DIMM2 | 1010 000Xb | A0H |
| DDR DIMM1 | 1010 001Xb | A2H |



| | | | |
|---|---|---|---|
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Title: NOTES LIST

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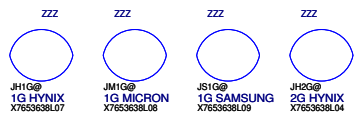
## EXO Pro VRAM STRAP

| | | Vendor<br>UV5, UV6, UV7, UV8 | ID | PS_3[3] | PS_3[2] | PS_3[1] | X76@<br>R_pu<br>RV21 | X76@<br>R_pd<br>RV24 |
|---|---|---|---|---|---|---|---|---|
| 1GBytes | ZZZ09<br>JH1G@ | Hynix 2048Mbits<br>SA00006H400<br>128Mx16 H5TC2G63FFR-11C | 0 | 0 | 0 | 0 | NC | 4.75K |
| 1GBytes | ZZZ10<br>JM1G@ | Micron 2048Mbits<br>SA000067500<br>128Mx16 MT41J128M16JT-093G:K | 1 | 0 | 0 | 1 | 8.45K | 2K |
| 1GBytes | ZZZ11<br>JS1G@ | Samsung 2048Mbits<br>SA000068U40<br>128Mx16 K4W2G1646Q-BC1A | 2 | 0 | 1 | 0 | 4.53K | 2K |
| 2GBytes | ZZZ12<br>JH2G@ | Hynix 4096Mbits<br>SA00006E800<br>256Mx16 H5TC4G63AFR-11C | 3 | 0 | 1 | 1 | 6.98K | 4.99K |
| 2GBytes | ZZZ13<br>JS2G@ | Samsung 4096Mbits<br>SA000076P00<br>256Mx16 K4W4G1646D-BC1A | 4 | 1 | 0 | 0 | 4.53K | 4.99K |
| 2GBytes | ZZZ14<br>JM2G@ | Micron 4096Mbits<br>SA000077K00<br>256Mx16 MT41J256M16HA-093G:E | 5 | 1 | 0 | 1 | 3.24K | 5.62K |
| 2GBytes | ZZZ08<br>JM2G2@ | Micron 4096Mbits<br>SA000065D00<br>256Mx16 MT41K256M16HA-107G:E | 6 | 1 | 1 | 0 | 3.4K | 10K |
| 1GBytes | ZZZ16<br>JM1G2@ | Micron 2048Mbits<br>SA00005XB00<br>128Mx16 MT41K128M16JT-107G:K | 7 | 1 | 1 | 1 | 4.75K | NC |




| R_pu (Ω) | R_pd (Ω) | Bits [3:1] |
|---|---|---|
| NC | 4750 | 000 |
| 8450 | 2000 | 001 |
| 4530 | 2000 | 010 |
| 6980 | 4990 | 011 |
| 4530 | 4990 | 100 |
| 3240 | 5620 | 101 |
| 3400 | 10000 | 110 |
| 4750 | NC | 111 |

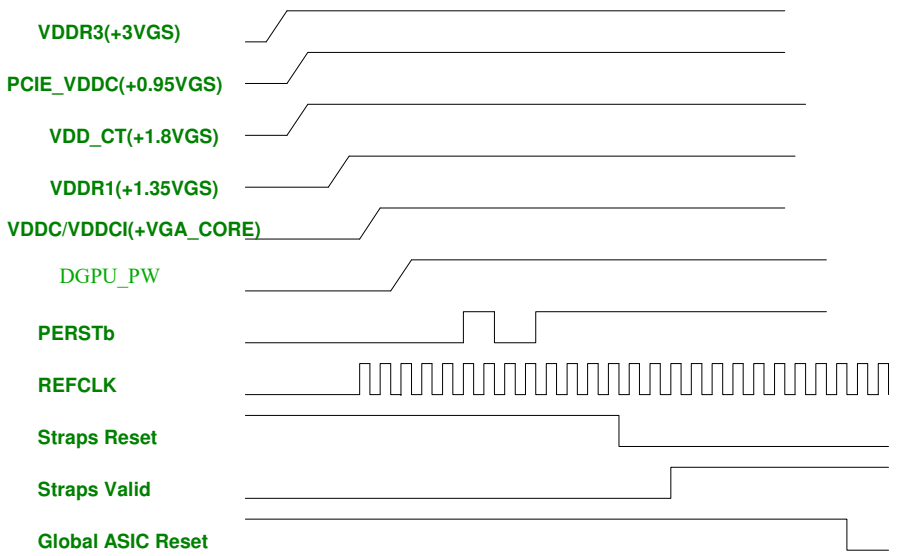
**Note:** 0402 1% resistors are required.

## DGPU_PW

## Power-Up/Down Sequence

"EXO" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
- It is recommended that the 3.3-V rail ramp up frist.
- It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2ms from the start of VDDC ramping up.
- The power rails that are shared with other components on the system should be gated for the dGPU so that when dGPU is powered down (for example AMD PowerXpressTM idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≦ 50mV/us)
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

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|---|---|---|---|
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| Issued Date | 2015/03/06 | Deciphered Date 2016/03/06 | Title: VGA Notes List |
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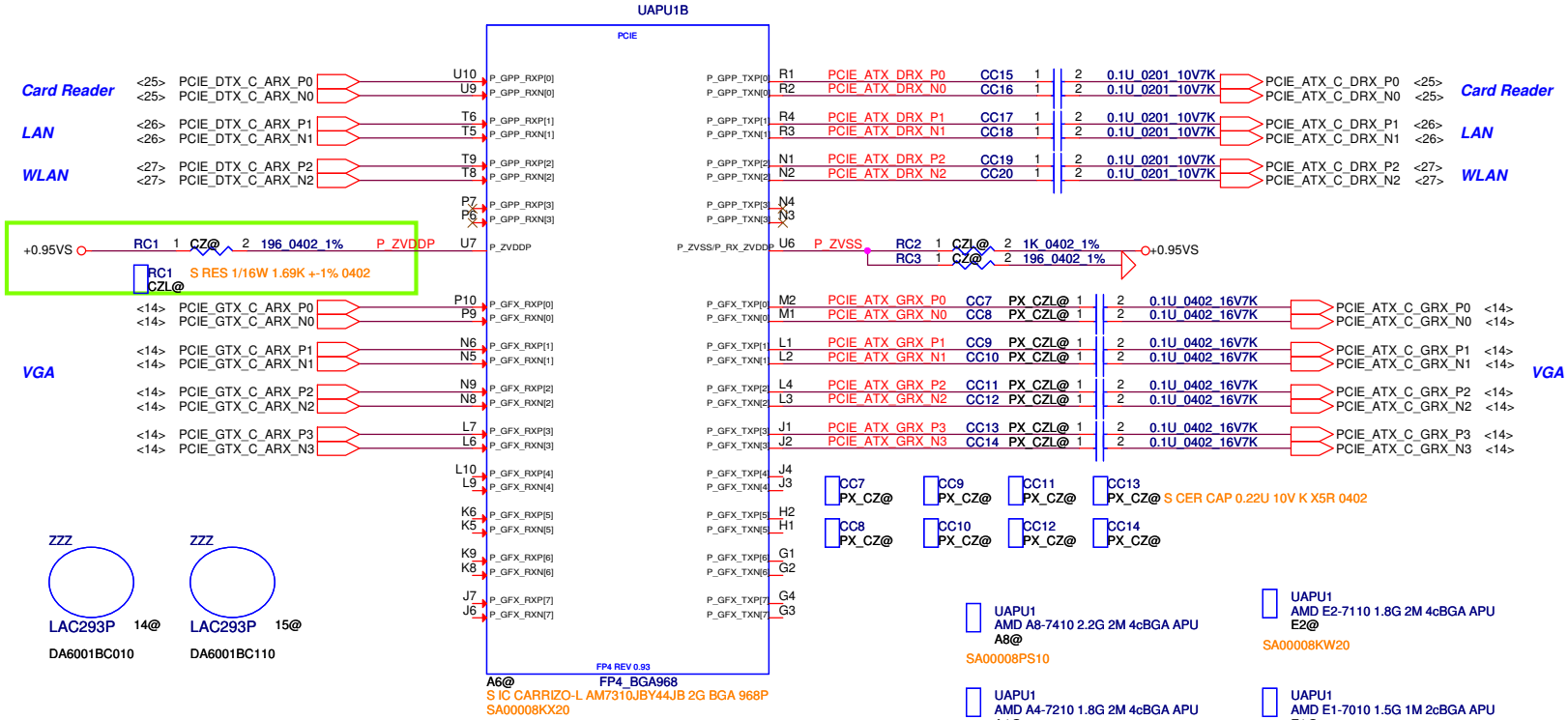


Carrizo:
PCIe GPP: Four x1 Gen2
PCIe Discrete Graphics Port: PCI Gen3 x8

Carrizo-L:
PCIe GPP: Four x1 Gen2
PCIe Discrete Graphics Port: PCI Gen2 x4

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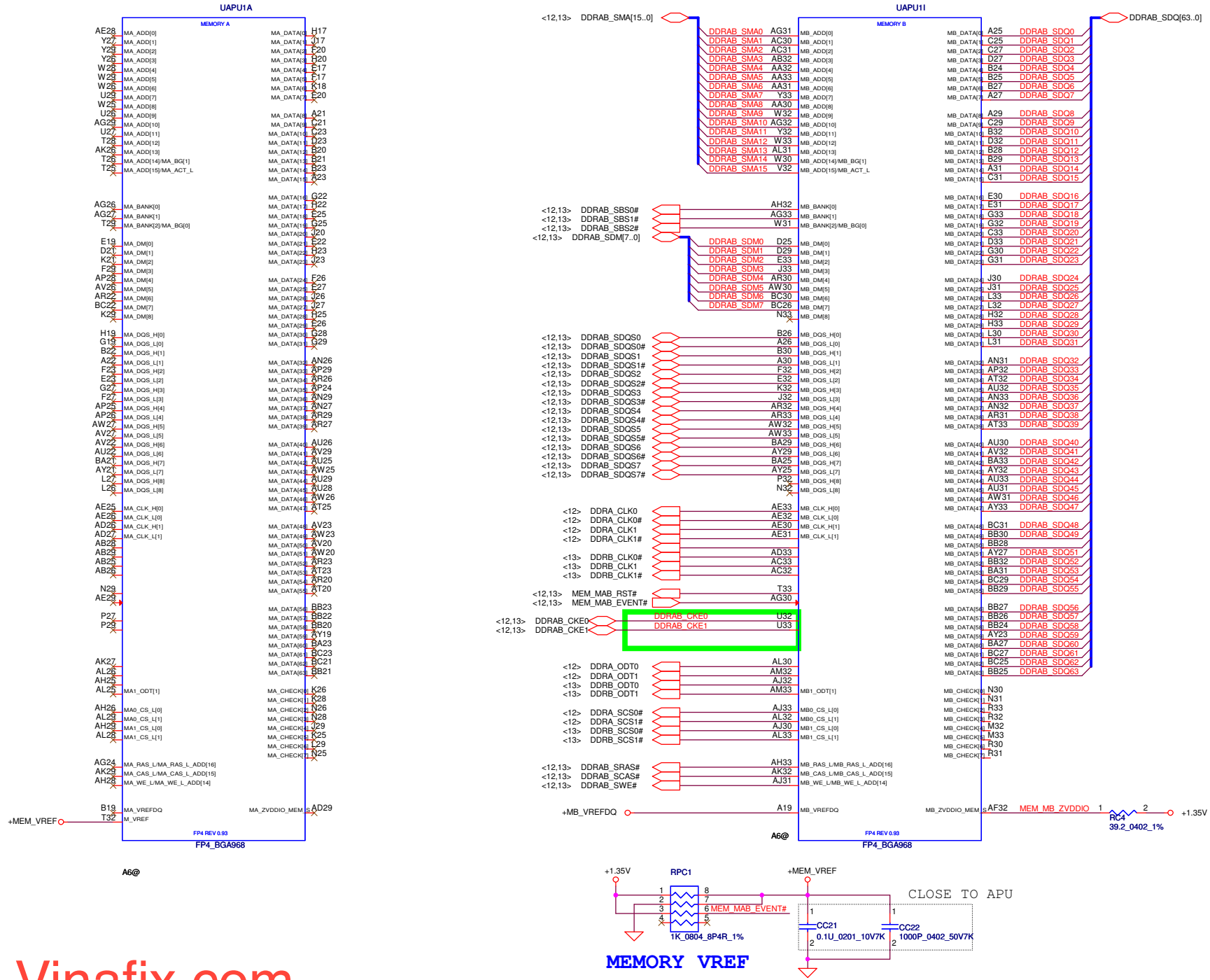




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Title: FP4 MEMORY INTERFACE

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DP2 is not supported by
Carrizo-L
DP2: HDMI
DP1: CRT Translator
DP0: eDP

For SIC, SID, ALERT_L, PROCHOT_L
Carrizo: Each are pulled up to VDD_18
Carrizo-L: Each are pulled up to VDD_33

**HDMI for CZ only**

**DP-to-CRT Translator or DP Switch**

UAPU1C
DISPLAYSVI2JTAG/TEST
FP4 REV 0.93
FP4_BGA968

Place resistor(0ohm) for SVT in PWR side

For DP_VARY_BL, DP_BLON, DP_DIGON
Carrizo: VDD_18 level at the APU
Carrizo-L: VDD_33 level at the APU

For DP_STEREOSYNC/TEST36
Carrizo: Pulled up to VDD_18
Carrizo-L: Pulled up to VDD_33

CZ
CZ-L

HDT+
JHDT1 @
SAMTE_ASP-136446-07-B

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |



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Title: FP4 DISP/MISC/HDT

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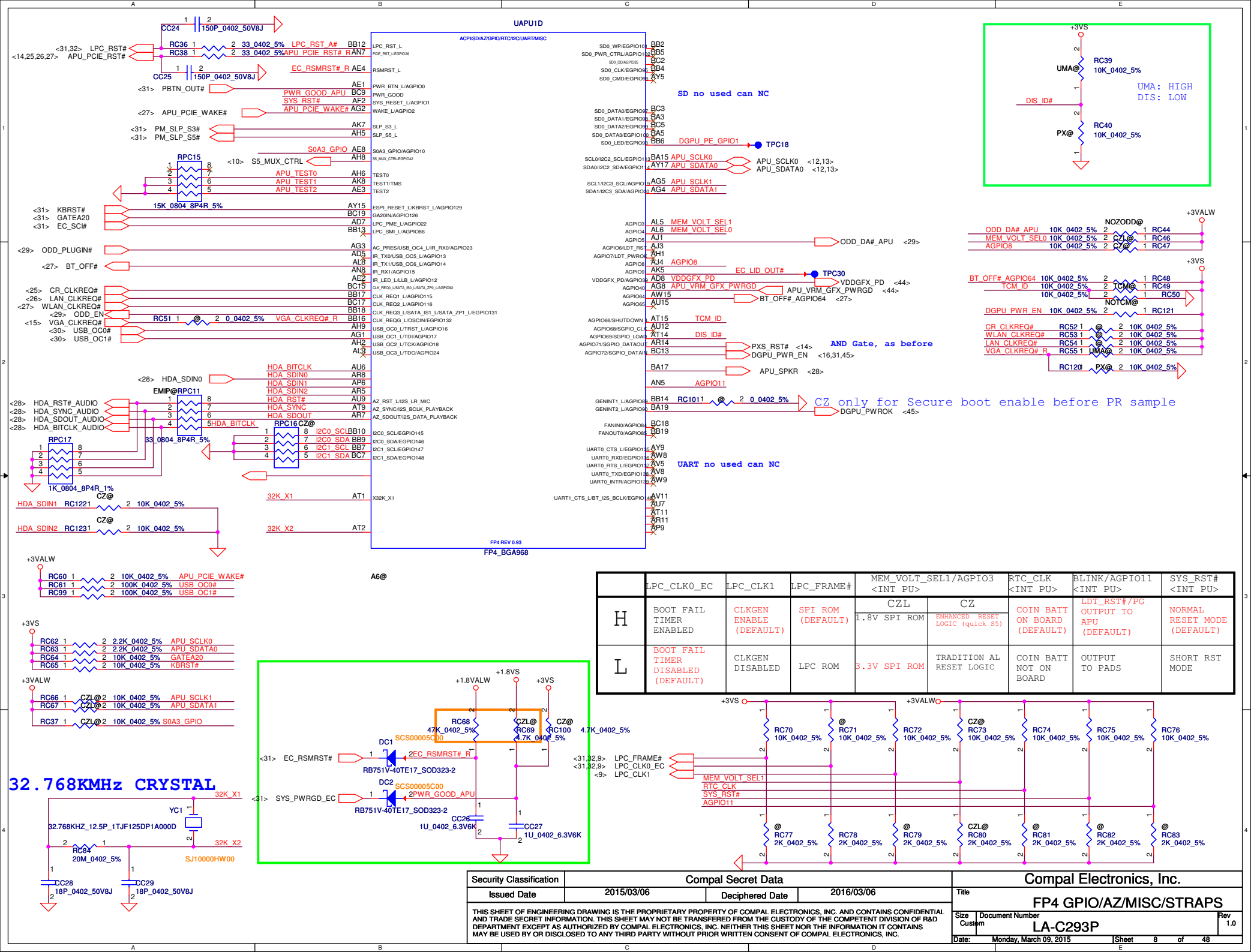


| | LPC_CLK0_EC | LPC_CLK1 | LPC_FRAME# | MEM_VOLT_SEL1/AGPIO3 <INT PU> | | RTC_CLK <INT PU> | BLINK/AGPIO11 <INT PU> | SYS_RST# <INT PU> |
|---|---|---|---|---|---|---|---|---|
| | | | | CZL | CZ | | | |
| H | BOOT FAIL TIMER ENABLED | CLKGEN ENABLE (DEFAULT) | SPI ROM (DEFAULT) | 1.8V SPI ROM | ENHANCED RESET LOGIC (quick S5) | COIN BATT ON BOARD (DEFAULT) | LDT_RST#/PG OUTPUT TO APU (DEFAULT) | NORMAL RESET MODE (DEFAULT) |
| L | BOOT FAIL TIMER DISABLED (DEFAULT) | CLKGEN DISABLED | LPC ROM | 3.3V SPI ROM | TRADITION AL RESET LOGIC | COIN BATT NOT ON BOARD | OUTPUT TO PADS | SHORT RST MODE |

| | | | |
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Title: FP4 GPIO/AZ/MISC/STRAPS

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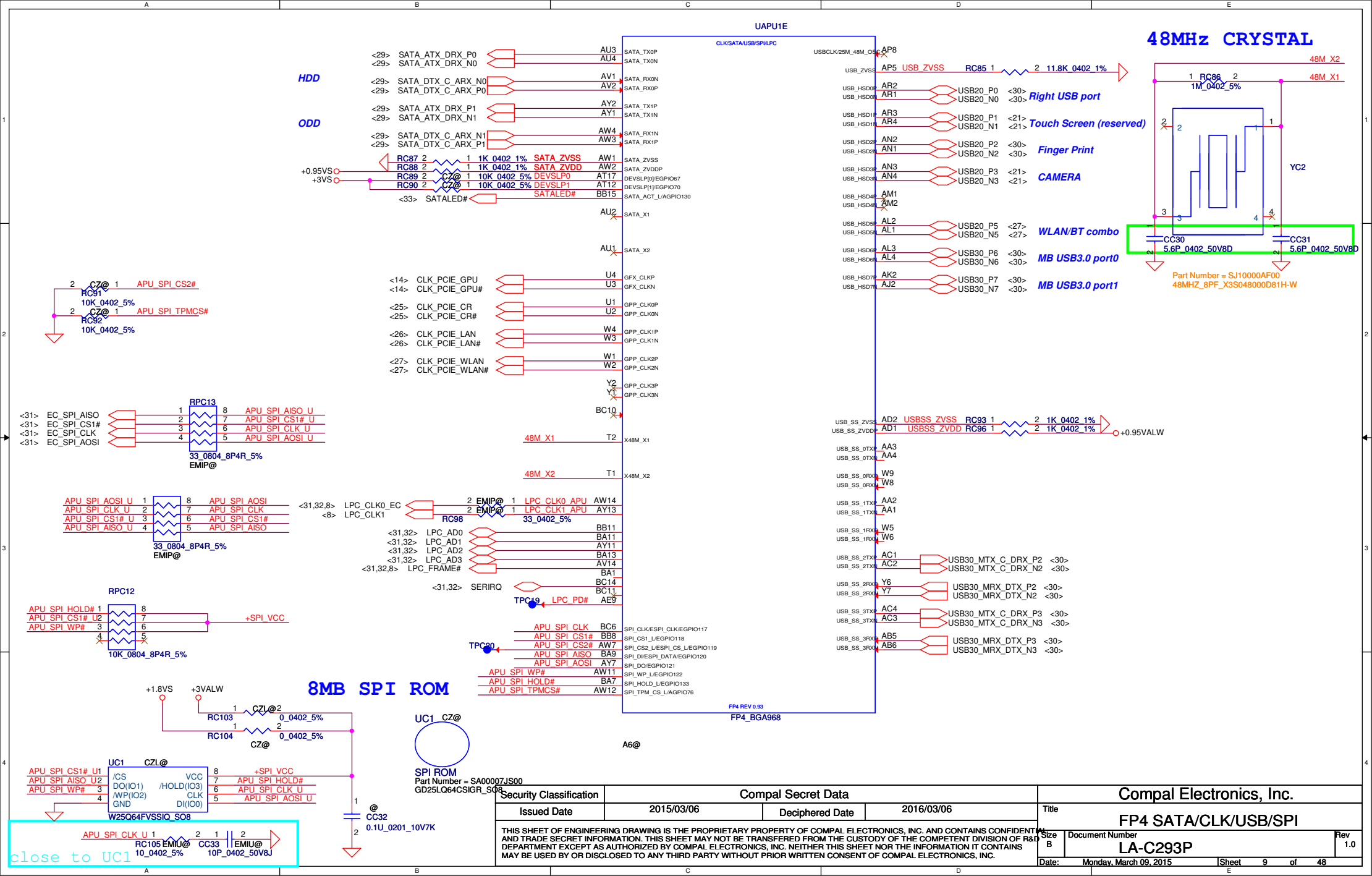


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Title: FP4 SATA/CLK/USB/SPI

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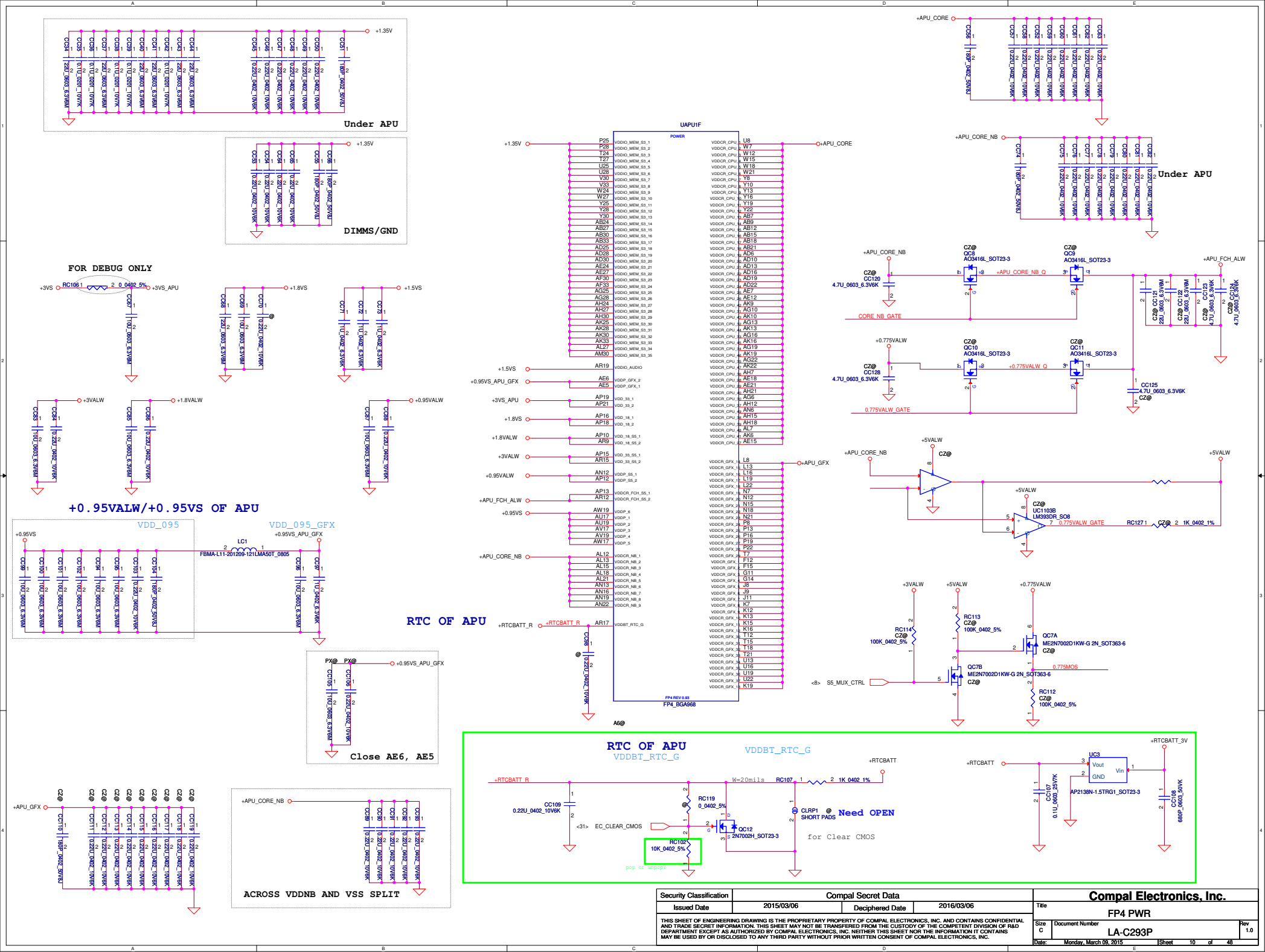
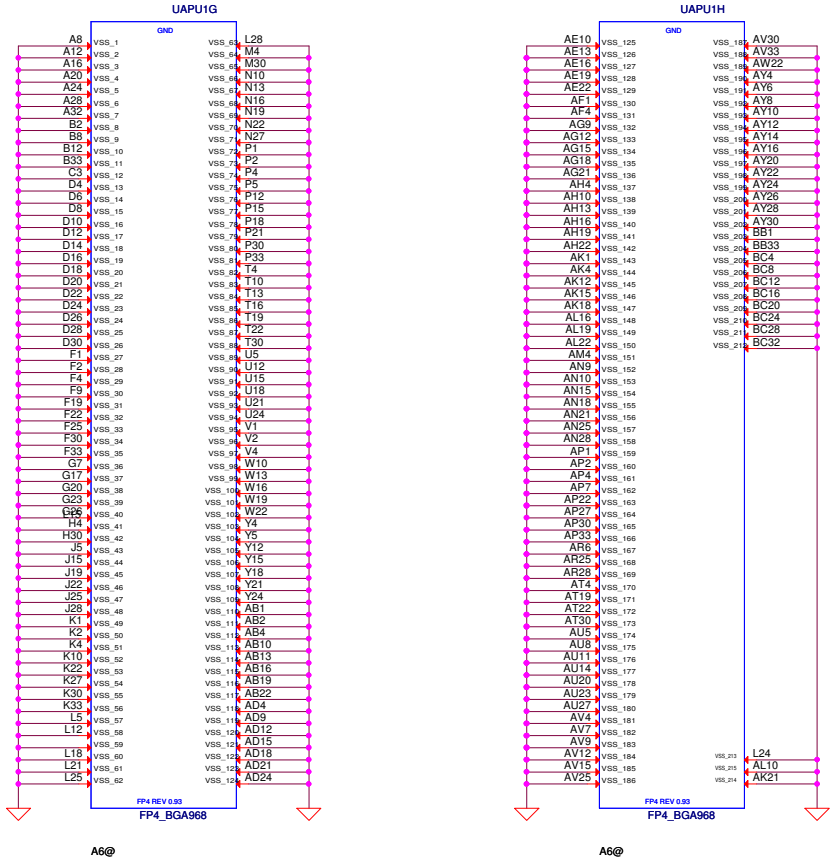
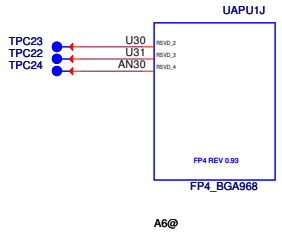

Under APU
DIMMS/GND
FOR DEBUG ONLY
+0.95VALW/+0.95VS OF APU
VDD_095
VDD_095_GFX
Close AE6, AE5
ACROSS VDDNB AND VSS SPLIT
UAPU1F
FP4_BGA968
RTC OF APU
VDDBT_RTC_G
Need OPEN
for Clear CMOS
Under APU
CORE_NB GATE
0.775VALW_GATE
Compal Electronics, Inc.
FP4 PWR
LA-C293P
Monday, March 09, 2015







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Title: FP4 GND

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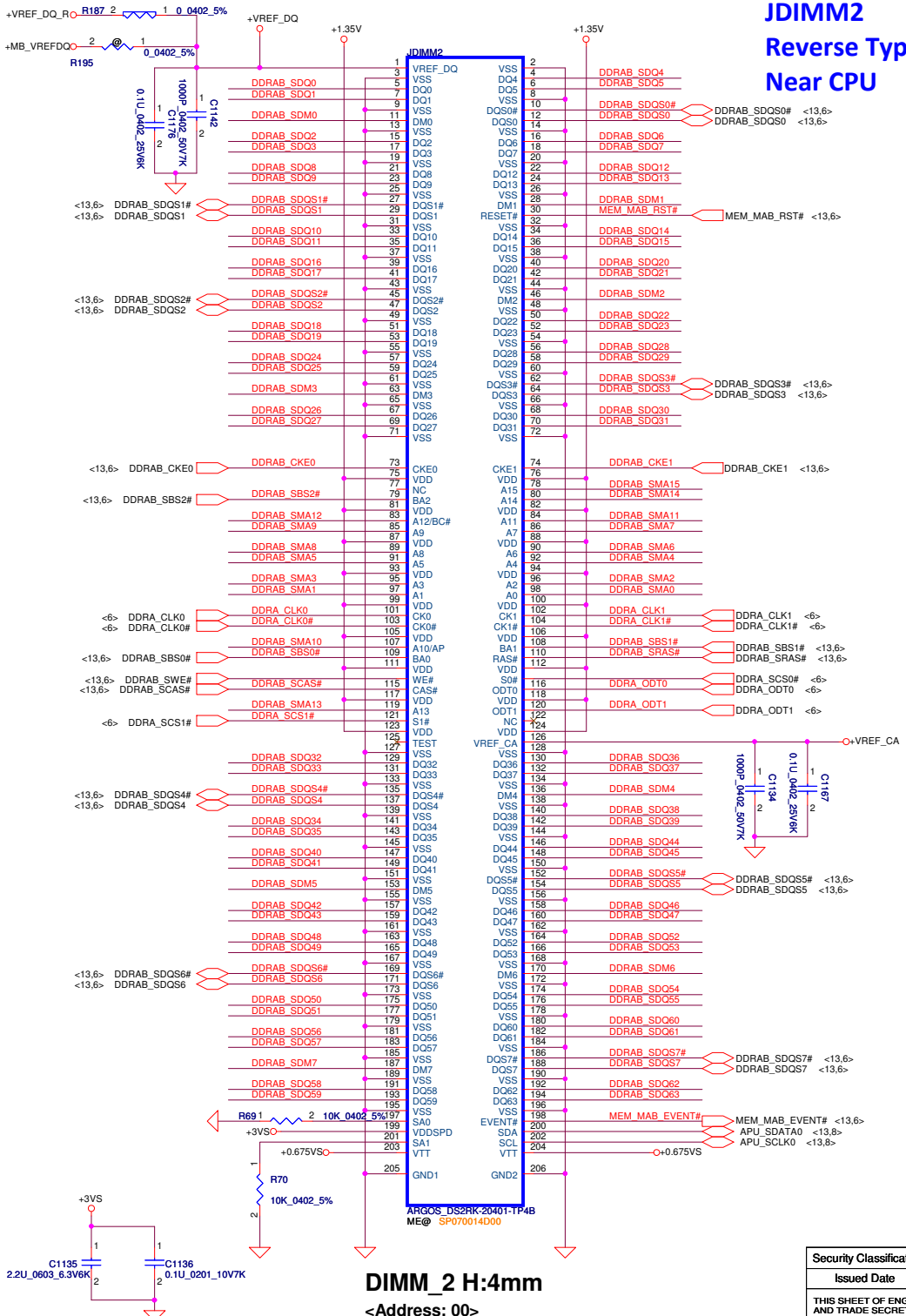
# JDIMM2
# Reverse Type
# Near CPU




## DIMM_2 H:4mm

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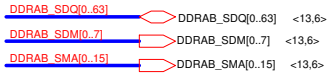
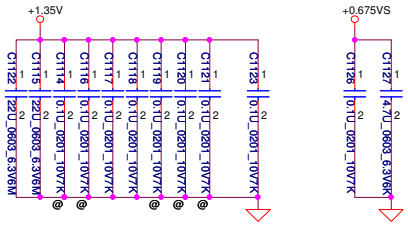
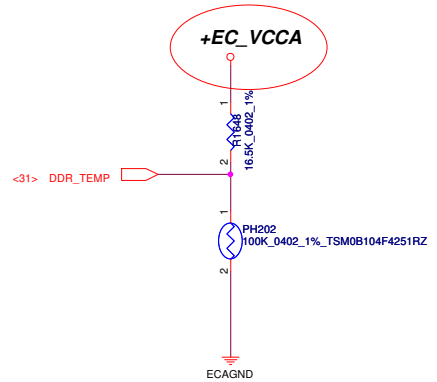
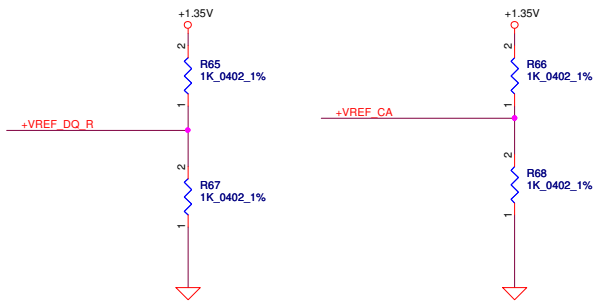



## +1.35V/+0.675VS OF DIMM2




## VREF for DIMM1,DIMM2

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Title: DDR3 SODIMM-I Socket

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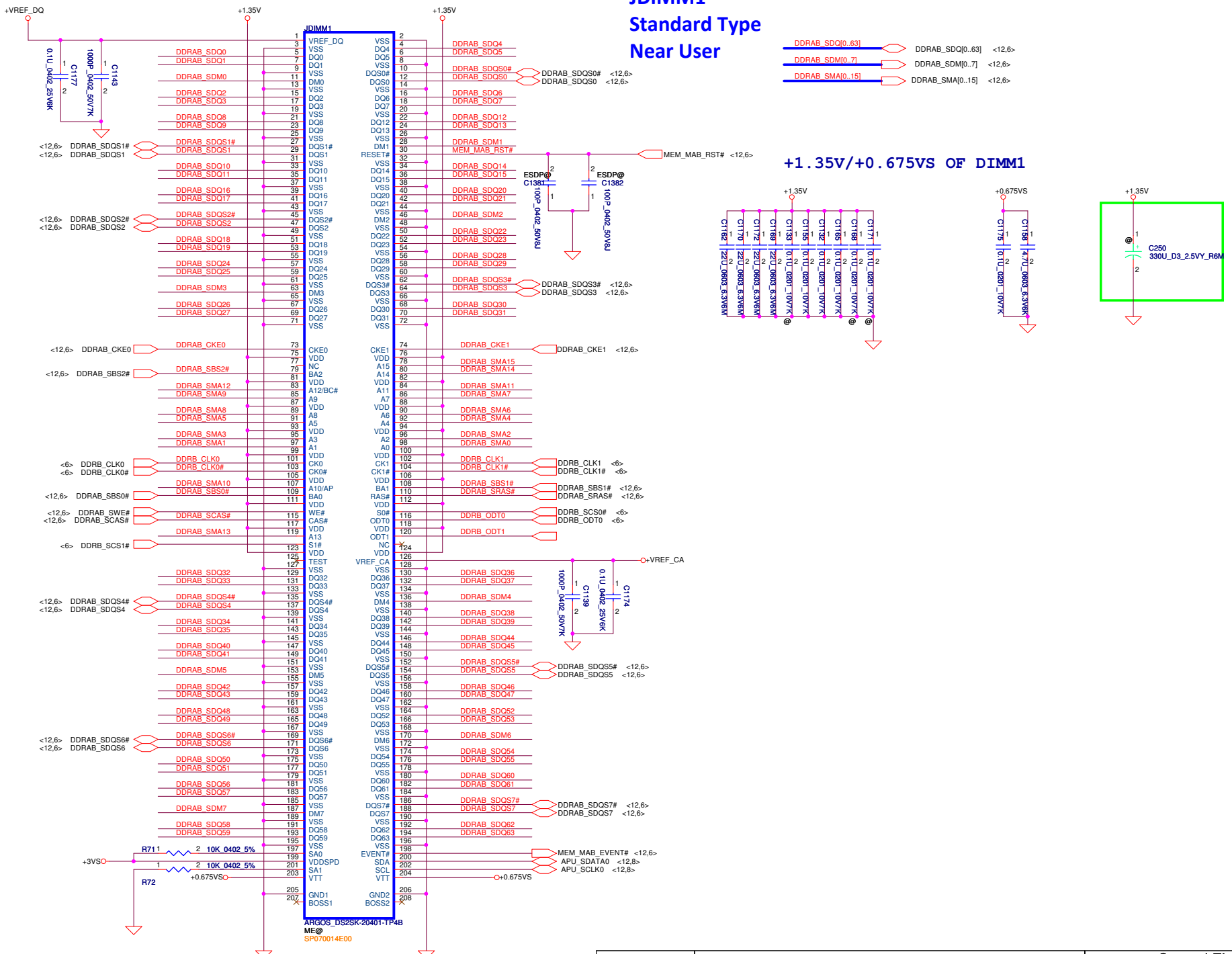
# JDIMM1
# Standard Type
# Near User




## DIMM_1 H:4mm

**<Address: 01>**

| | | | |
|---|---|---|---|
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Title: DDR3 SODIMM-II Socket

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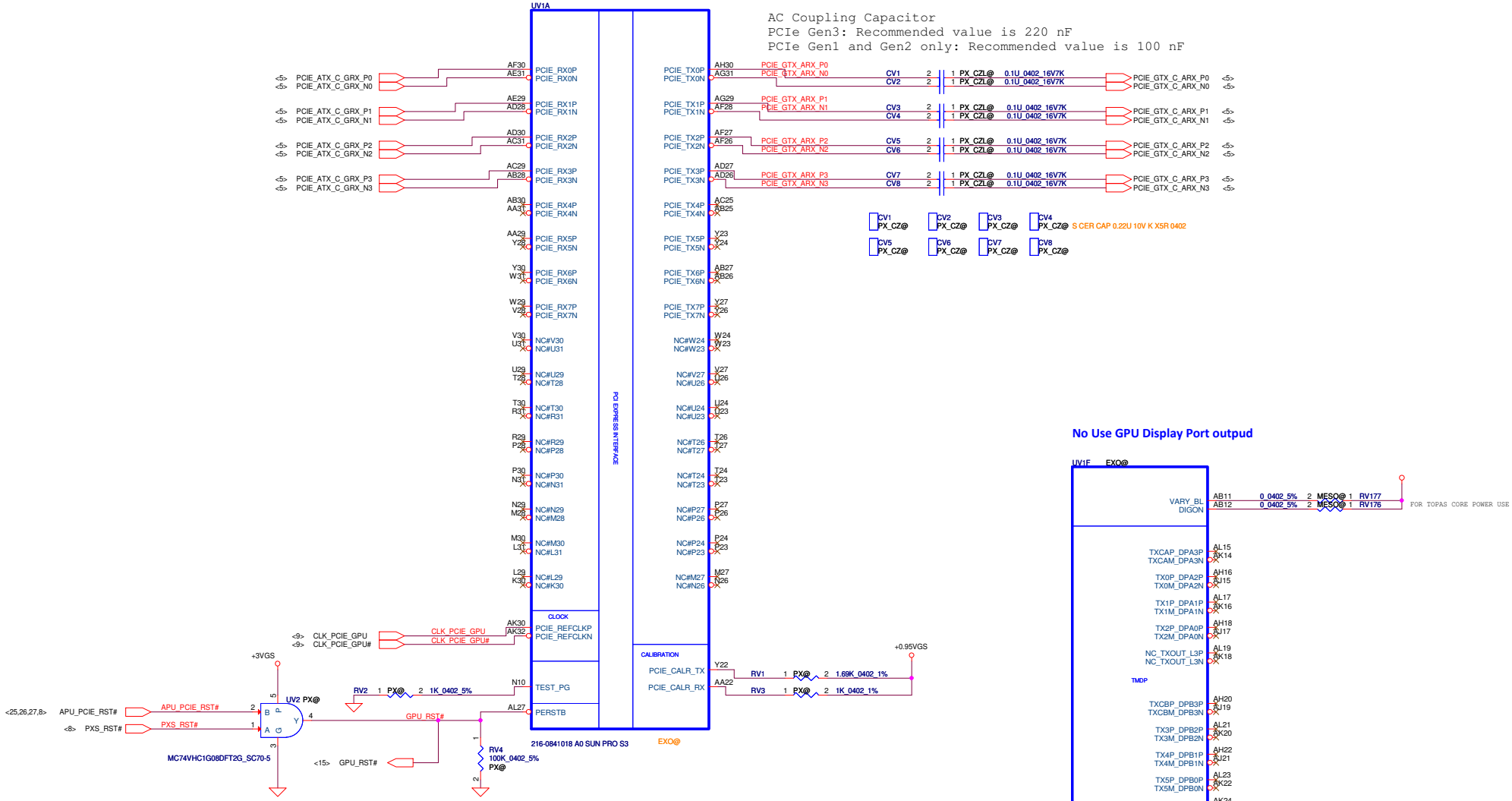


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Title: EXO/MESO(1/5)_PCIE/DP

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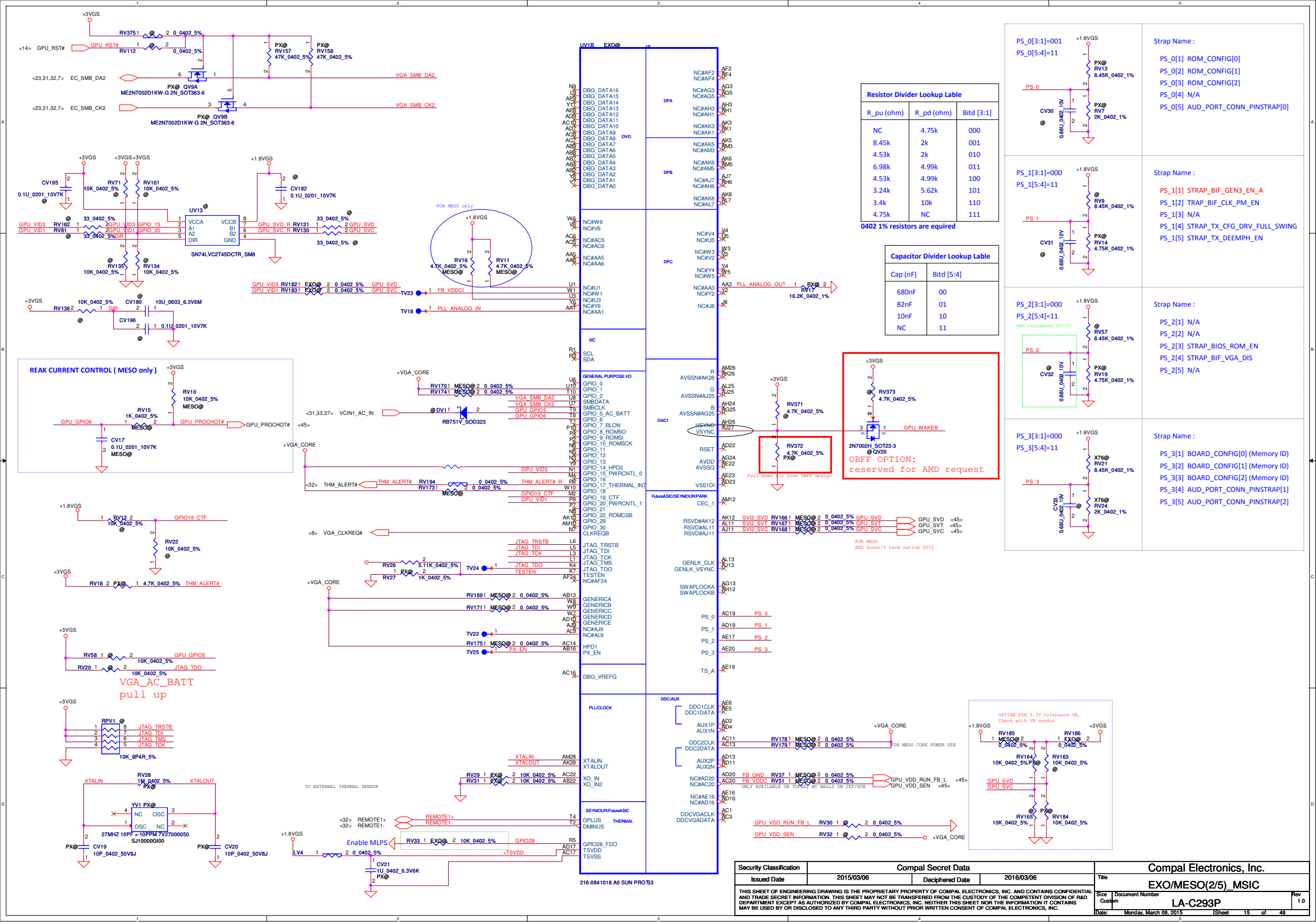
Resistor Divider Lookup Lable
R_pu (ohm) | R_pd (ohm) | Bitd [3:1]
NC | 4.75k | 000
8.45k | 2k | 001
4.53k | 2k | 010
6.98k | 4.99k | 011
4.53k | 4.99k | 100
3.24k | 5.62k | 101
3.4k | 10k | 110
4.75k | NC | 111
0402 1% resistors are equired
Capacitor Divider Lookup Lable
Cap (nF) | Bitd [5:4]
680nF | 00
82nF | 01
10nF | 10
NC | 11
PS_0[3:1]=001
PS_0[5:4]=11
Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]
PS_1[3:1]=000
PS_1[5:4]=11
Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN
PS_2[3:1]=000
PS_2[5:4]=11
AMD recommend 09/25
Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A
PS_3[3:1]=000
PS_3[5:4]=11
Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]
REAK CURRENT CONTROL ( MESO only )
VGA_AC_BATT
pull up
OBFF OPTION:
reserved for AMD request
Enable MLPS
FOR MESO only
TO EXTERNAL THERMAL SENSOR
OPTIAN FOR 3.3V tolerance VR,
Check with VR vendor
Security Classification
Compal Secret Data
Issued Date
2015/03/06
Deciphered Date
2016/03/06
Compal Electronics, Inc.
EXO/MESO(2/5)_MSIC
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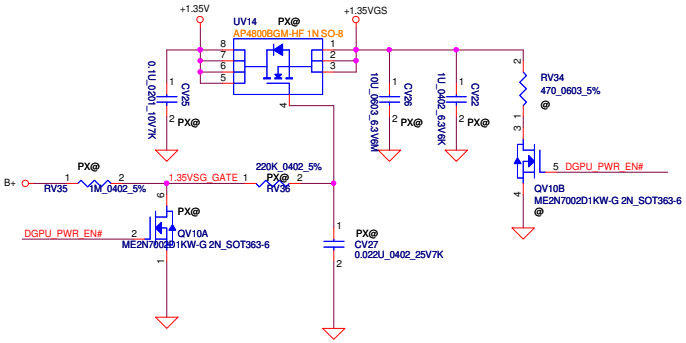
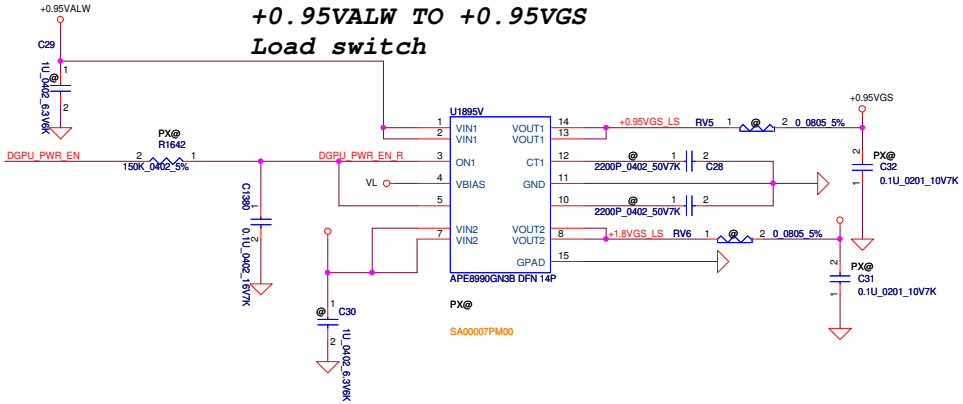
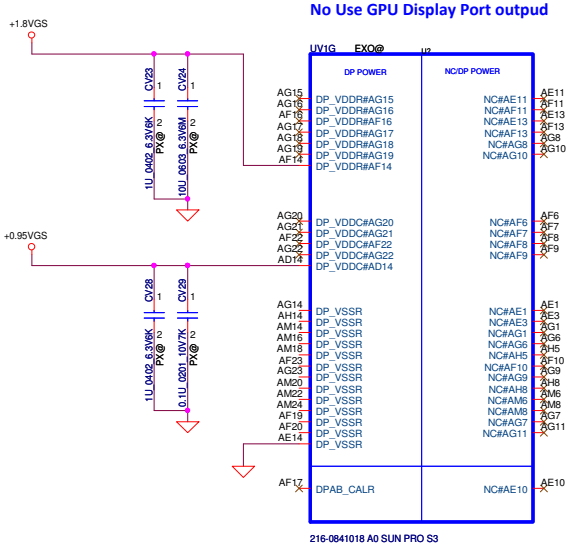
## +1.35VS to +1.35VGS

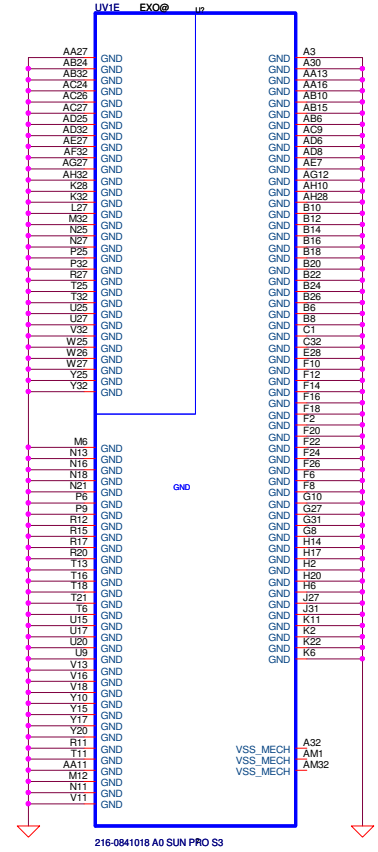



## +1.8VALW TO +1.8VGS
## +0.95VALW TO +0.95VGS
## Load switch

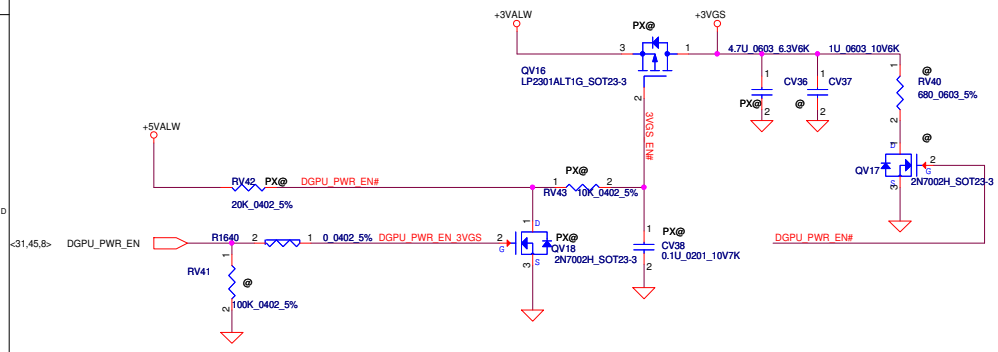


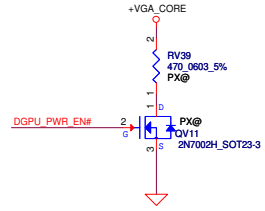

## No Use GPU Display Port outpud

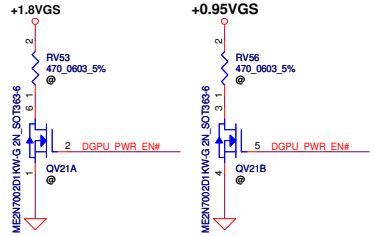



## +3VS to +3VGS




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
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Compal Electronics, Inc.

Title: EXO/MESO(3/5)_PWR/GND

Size: Custom | Document Number: LA-C293P | Rev: 1.0

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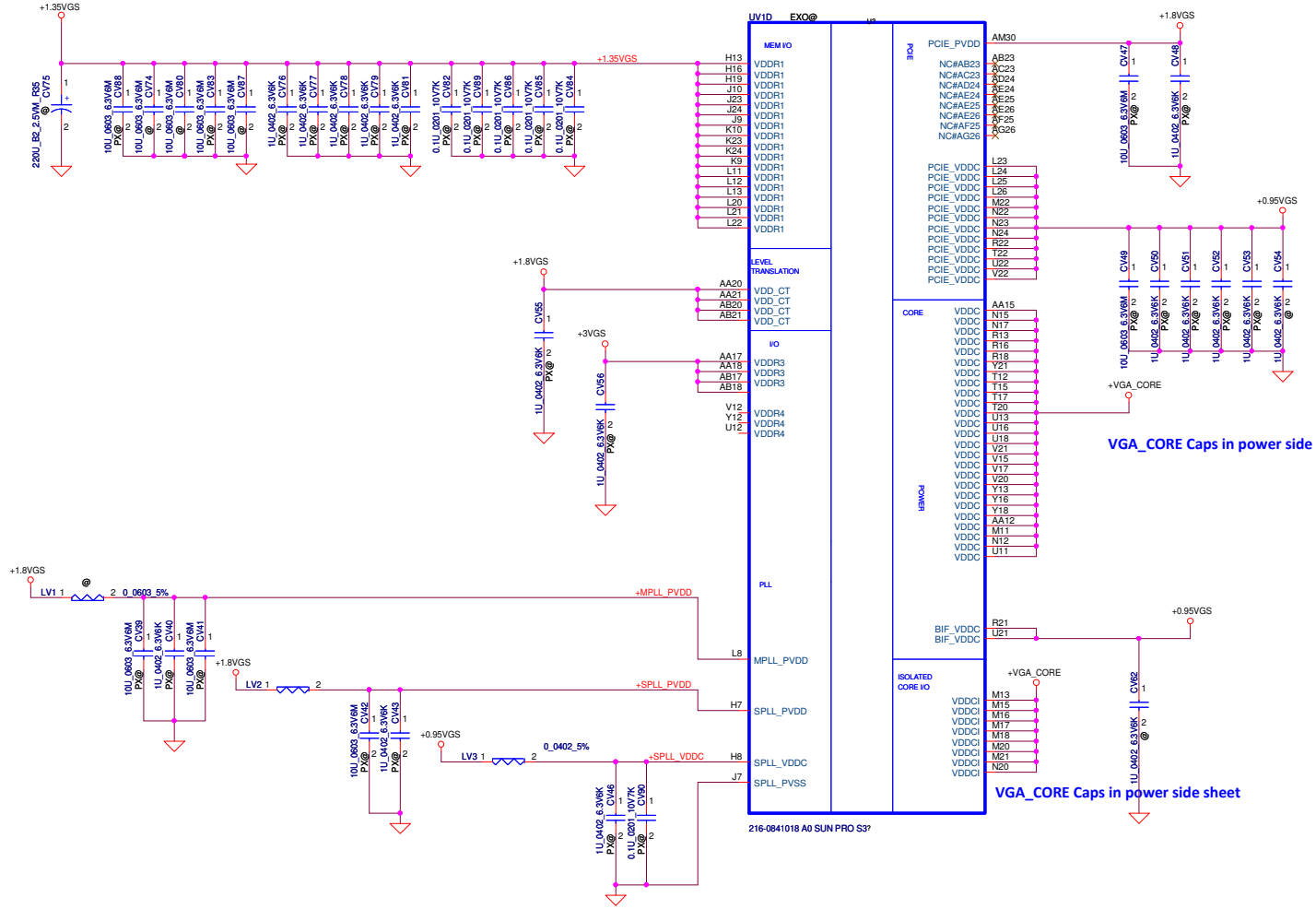


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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |



Compal Electronics, Inc.

Title: EXO/MESO(4/5)_PWR

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|---|---|---|
| Custom | LA-C293P | 1.0 |

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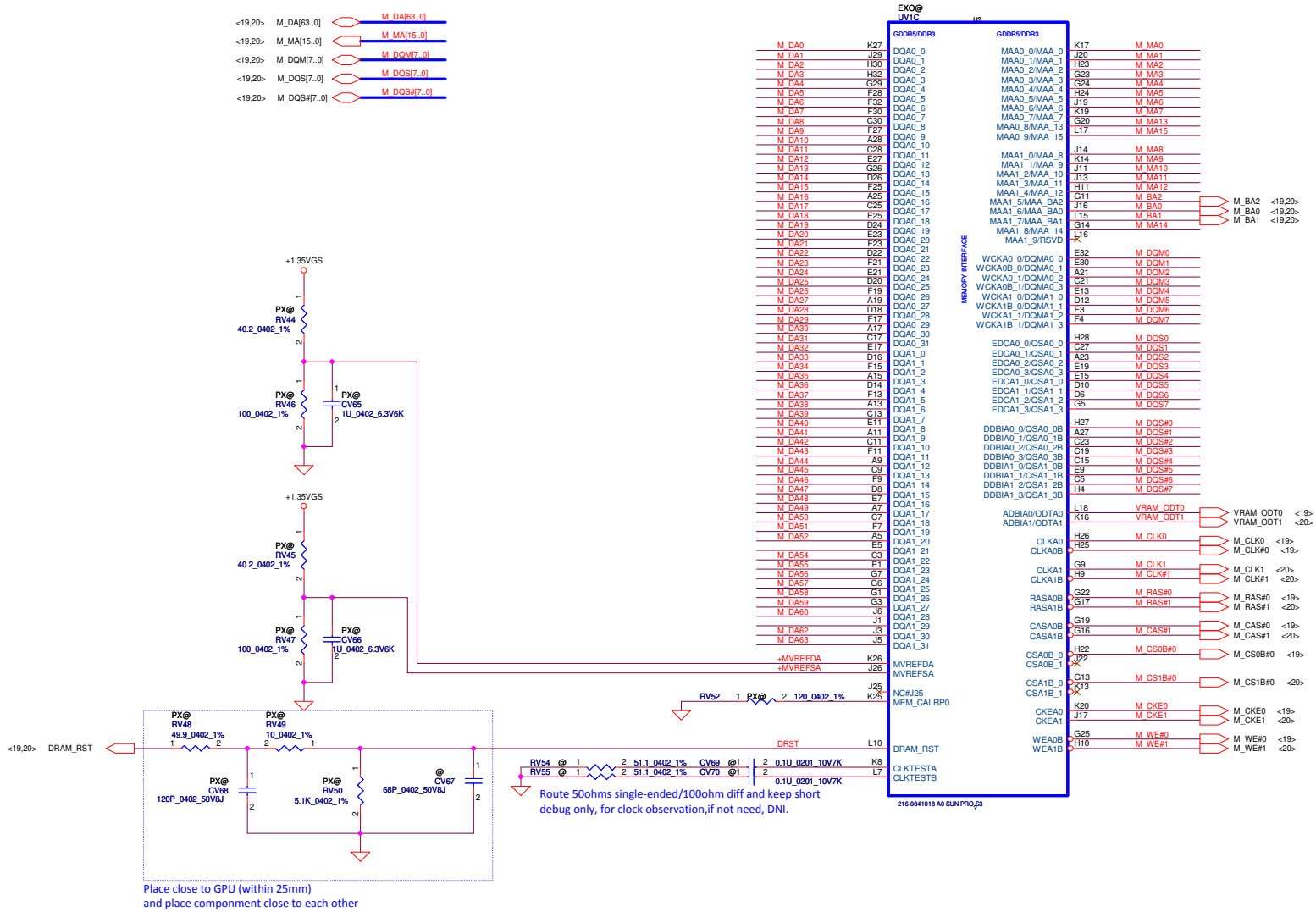


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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |



Compal Electronics, Inc.

Title: EXO/MESO(5/5)_MEM

| Size | Document Number | Rev |
|---|---|---|
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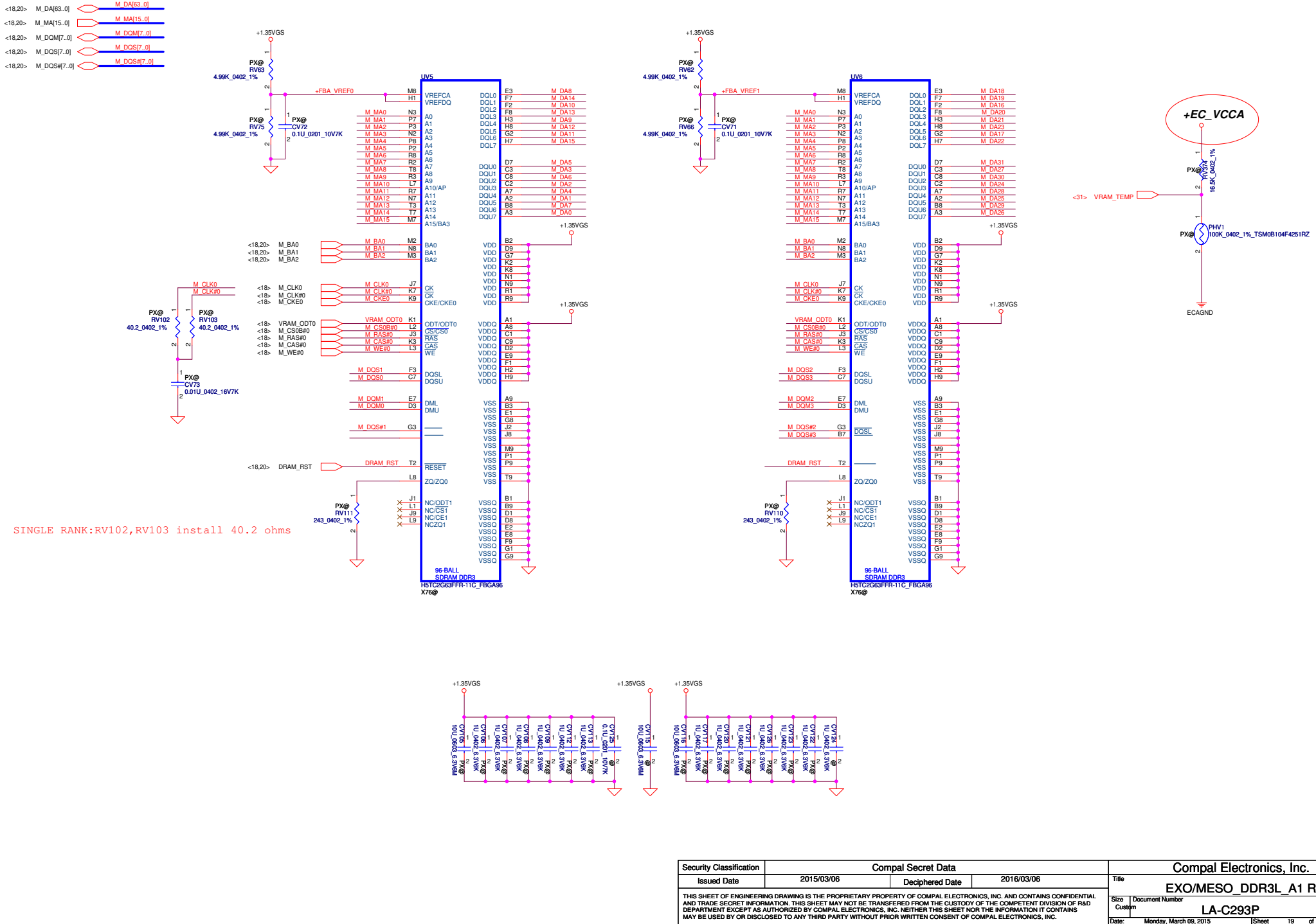
# DDR3L Memory Channel Rank 0:A0




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |



Compal Electronics, Inc.

Title: EXO/MESO_DDR3L_A1 Rank 0

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-C293P | 1.0 |

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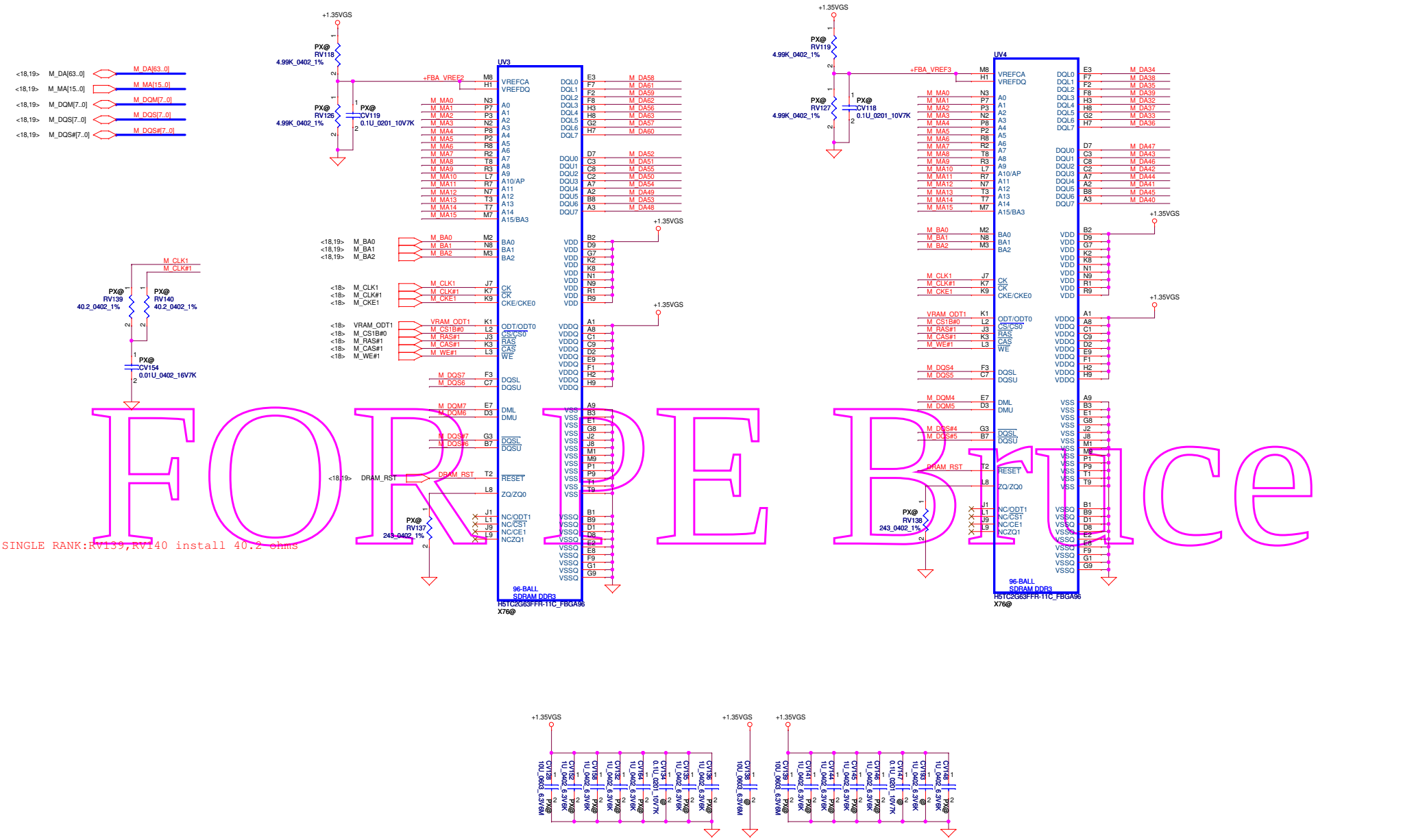
# DDR3L Memory Channel Rank 0:A1



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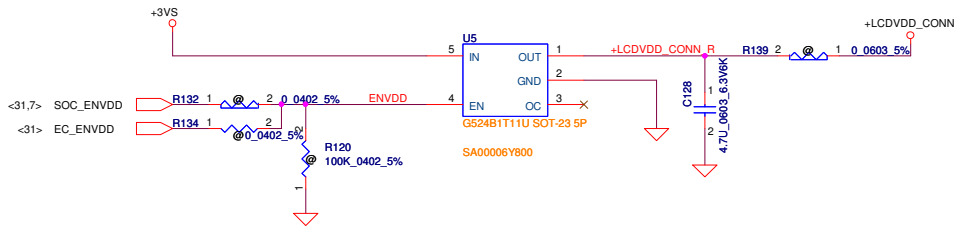
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |

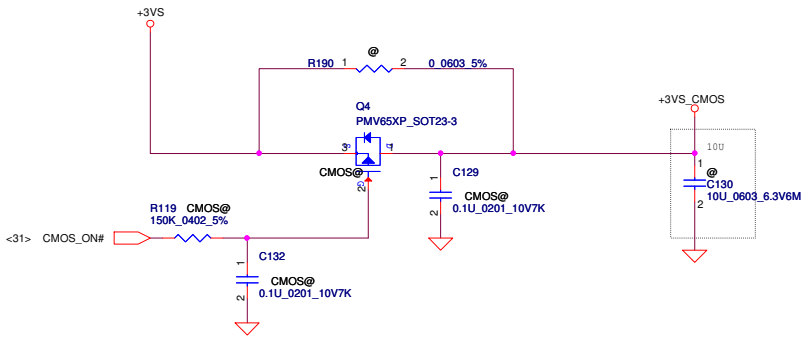


| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | EXO/MESO_DDR3L_A2 Rank 0 | | |
| Size: Custom | Document Number: LA-C293P | | Rev: 1.0 |
| Date: Monday, March 09, 2015 | Sheet 20 of 48 | | |

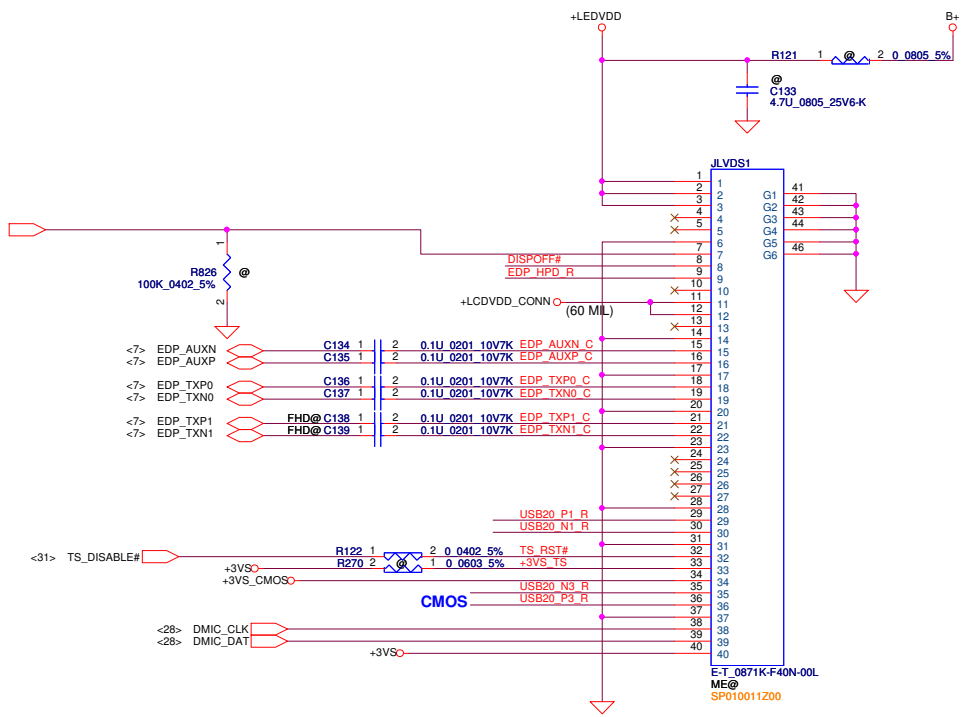
## LCD POWER CIRCUIT

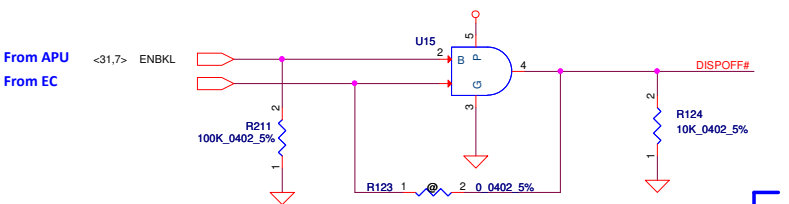


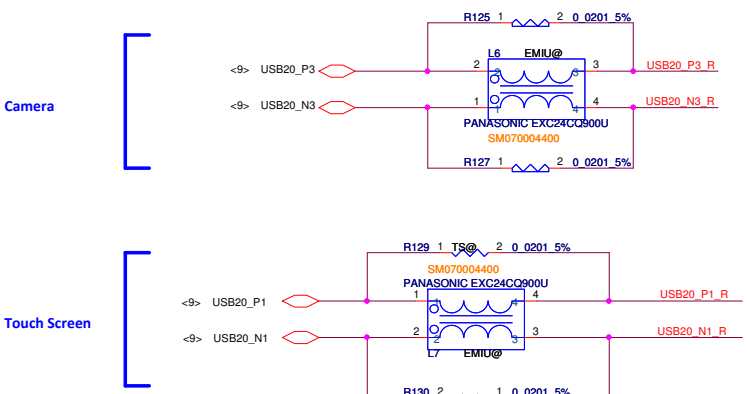

## CMOS Camera




## VGA LCD/PANEL BD. Conn.

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|---|---|---|---|
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Title: EDP CONN / Camera

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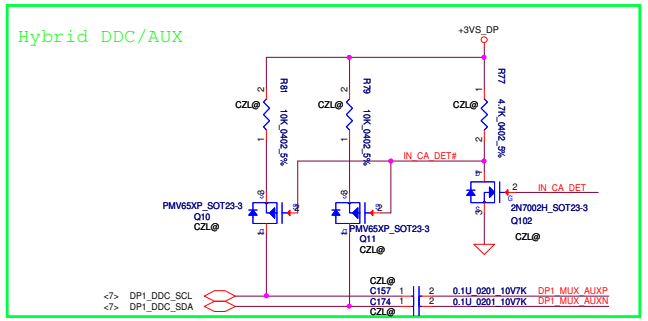



| TMDS_DDCBUF | Function |
|---|---|
| H | DDC active buffer |
| M | DDC pass through with 40 kohm pull up resistor |
| L | DDC pass through |

| TMDS_RT | Function |
|---|---|
| H | Open drain driver with termination resistors |
| L | Standard open drain driver |

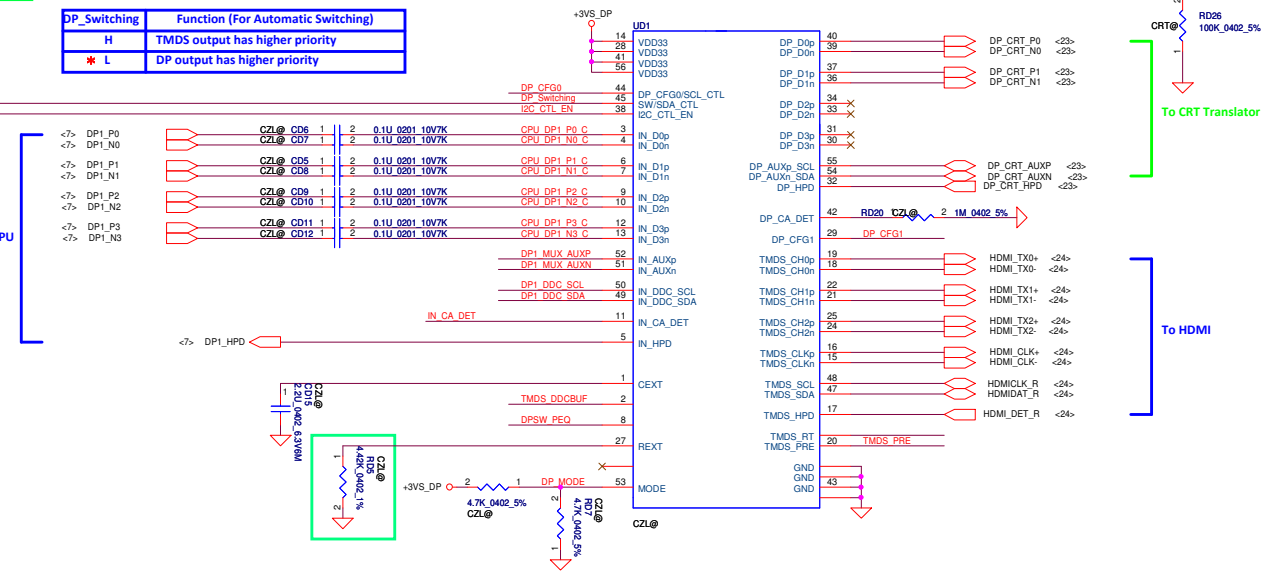
| TMDS_PRE | |
|---|---|
| H | 1.5dB pre-emphasis |
| M | 3.0dB pre-emphasis |
| L | no pre-emphasis |

| DPSW_PEQ | Function |
|---|---|
| H | HEQ, compensate channel loss up to 15dB @ HBR2 |
| M | LLEQ, compensate channel loss up to 5dB @ HBR2 |
| L | default, LEQ, compensate channel loss up to 12dB @ HBR2 |

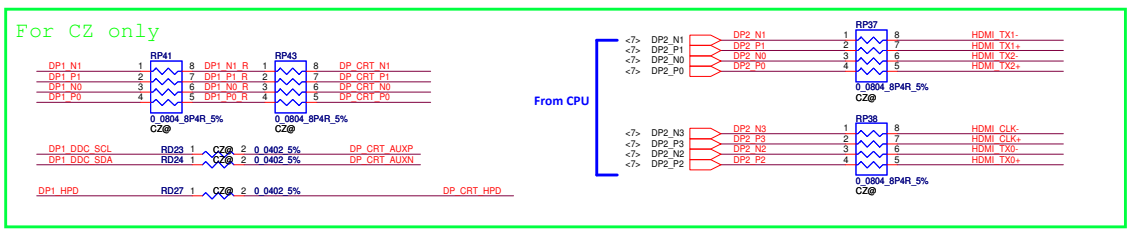
| DP_CFG0 | Function |
|---|---|
| H | automatic EQ disable & AUX interception enable |
| M | automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing |
| L | default, automatic EQ enable & AUX interception enable |

| DP_CFG1 | Function |
|---|---|
| H | auto test enable & input offset cancellation enable |
| M | auto test disable & input offset cancellation disable |
| L | default, auto test disable & input offset cancellation enable |

| DP_Switching | Function (For Automatic Switching) |
|---|---|
| H | TMDS output has higher priority |
| * L | DP output has higher priority |




| DP_MODE | Function |
|---|---|
| H | Automatic Switching Mode, HDMI ID disable |
| *M (VDD33/2 | Automatic Switching Mode, HDMI ID enable |
| L | Control Switching Mode, HDMI ID disable |




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
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Compal Electronics, Inc.

Title: DP Switch

| Size | Document Number | Rev |
|---|---|---|
| C | LA-C293P | 1.0 |

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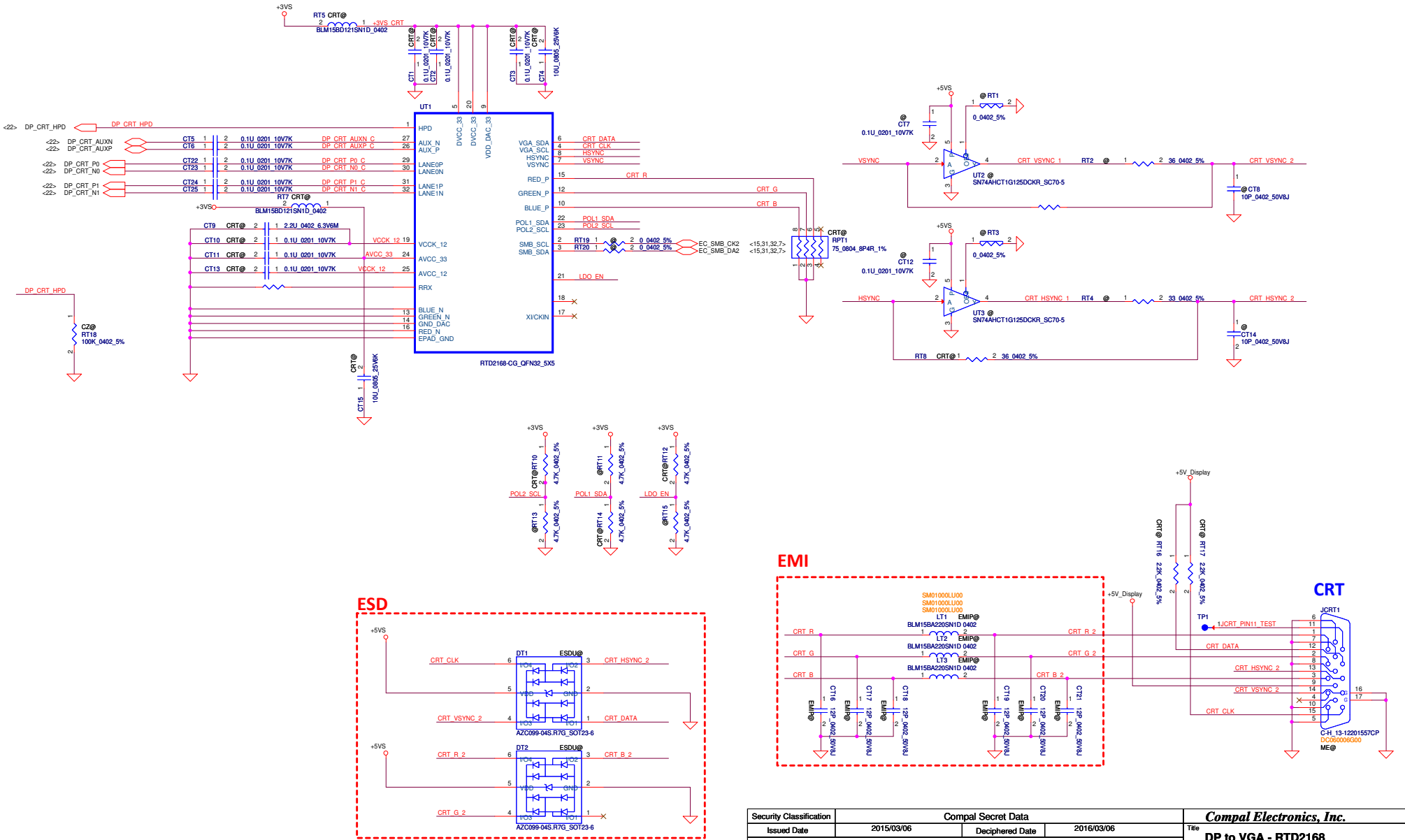
UT1
RTD2168-CG_QFN32_5X5
BLM15BD121SN1D_0402
AZC099-04S.R7G_SOT23-6
SN74AHCT1G125DCKR_SC70-5
75_0804_8P4R_1%
BLM15BA220SN1D 0402
SM01000LU00
C-H_13-12201557CP
DC080006G00
ME@
EMI
ESD
CRT
DP to VGA - RTD2168
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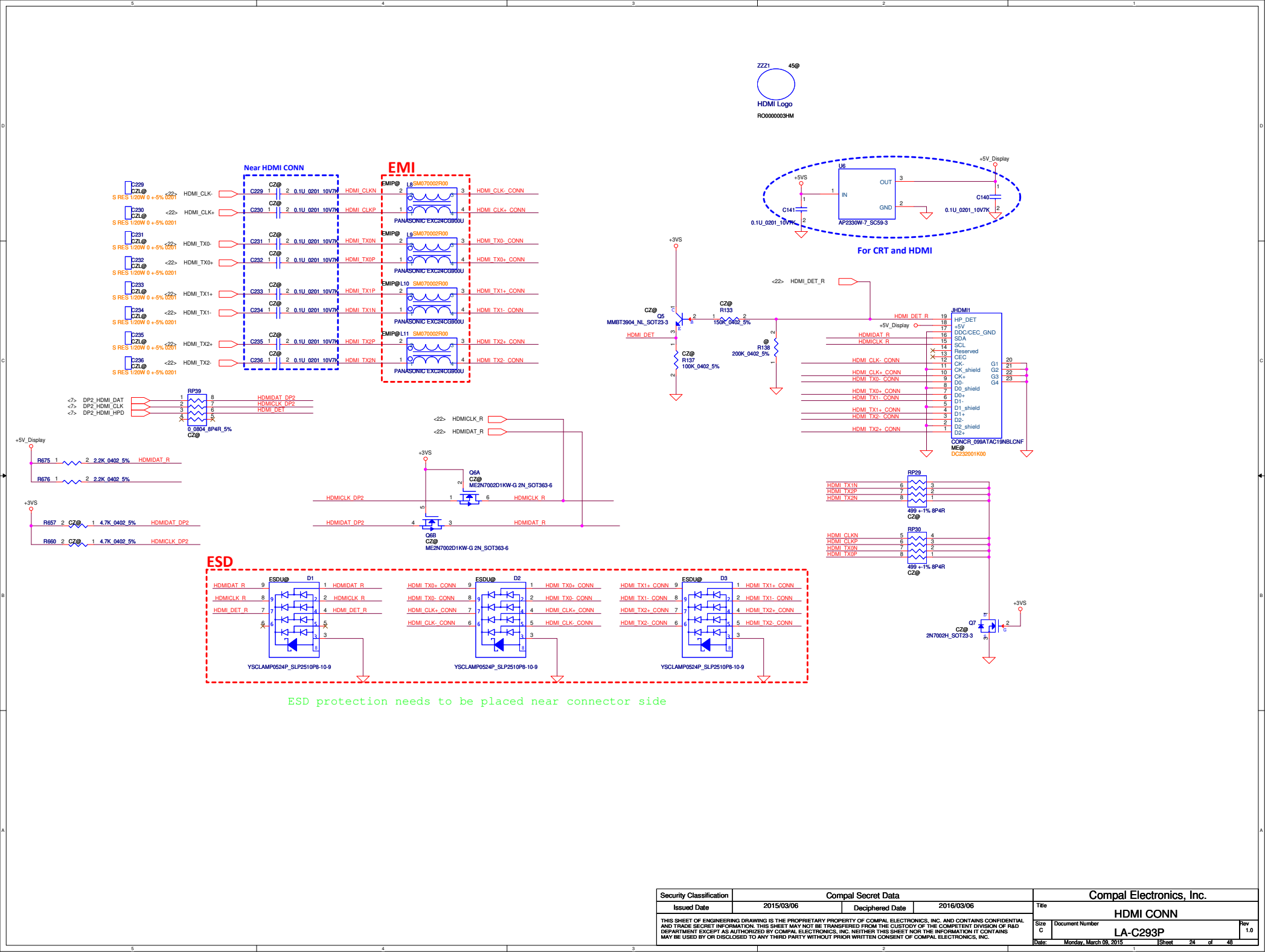


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| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | HDMI CONN | | |
| Size C | Document Number LA-C293P | | Rev 1.0 |
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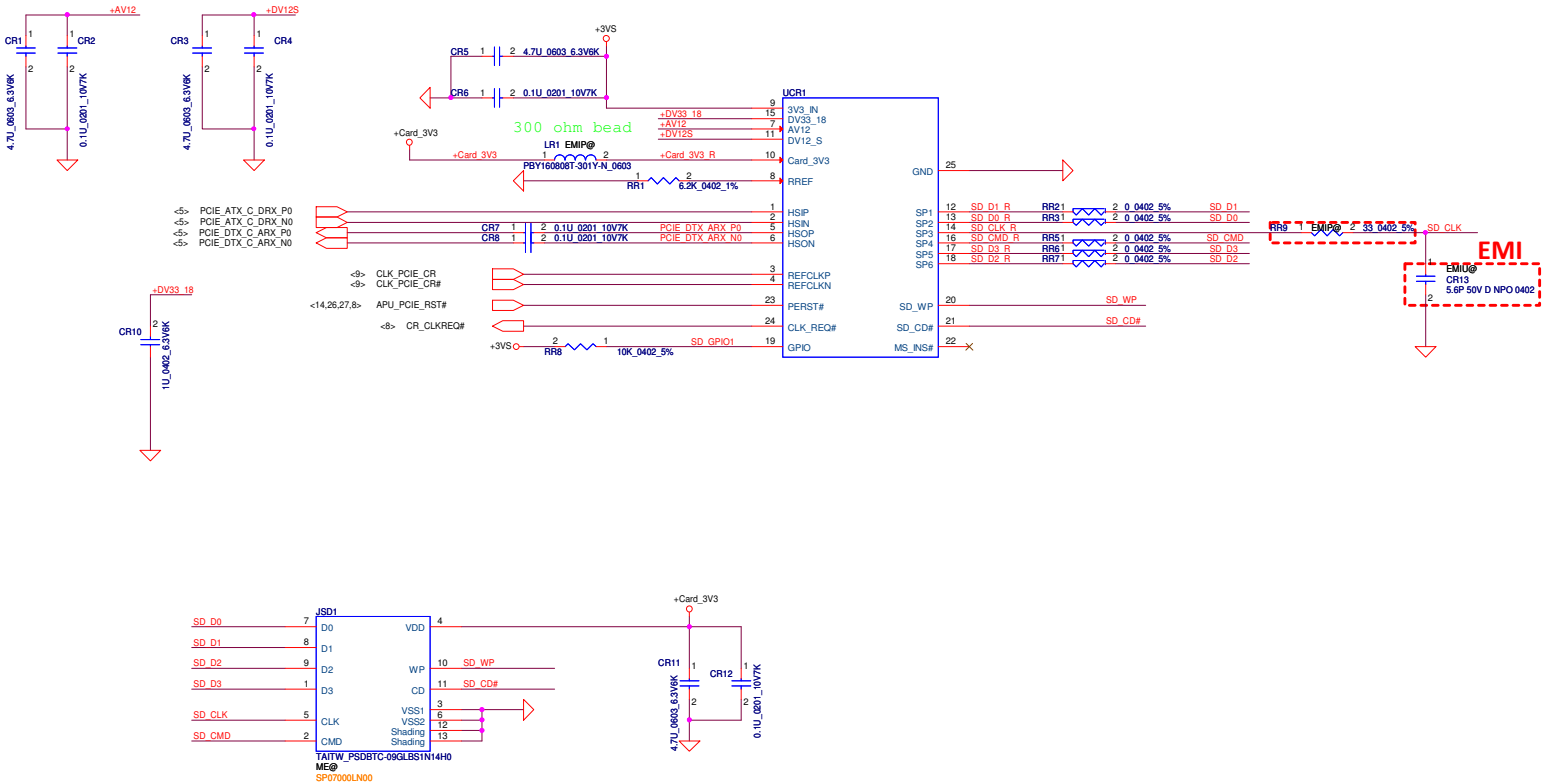


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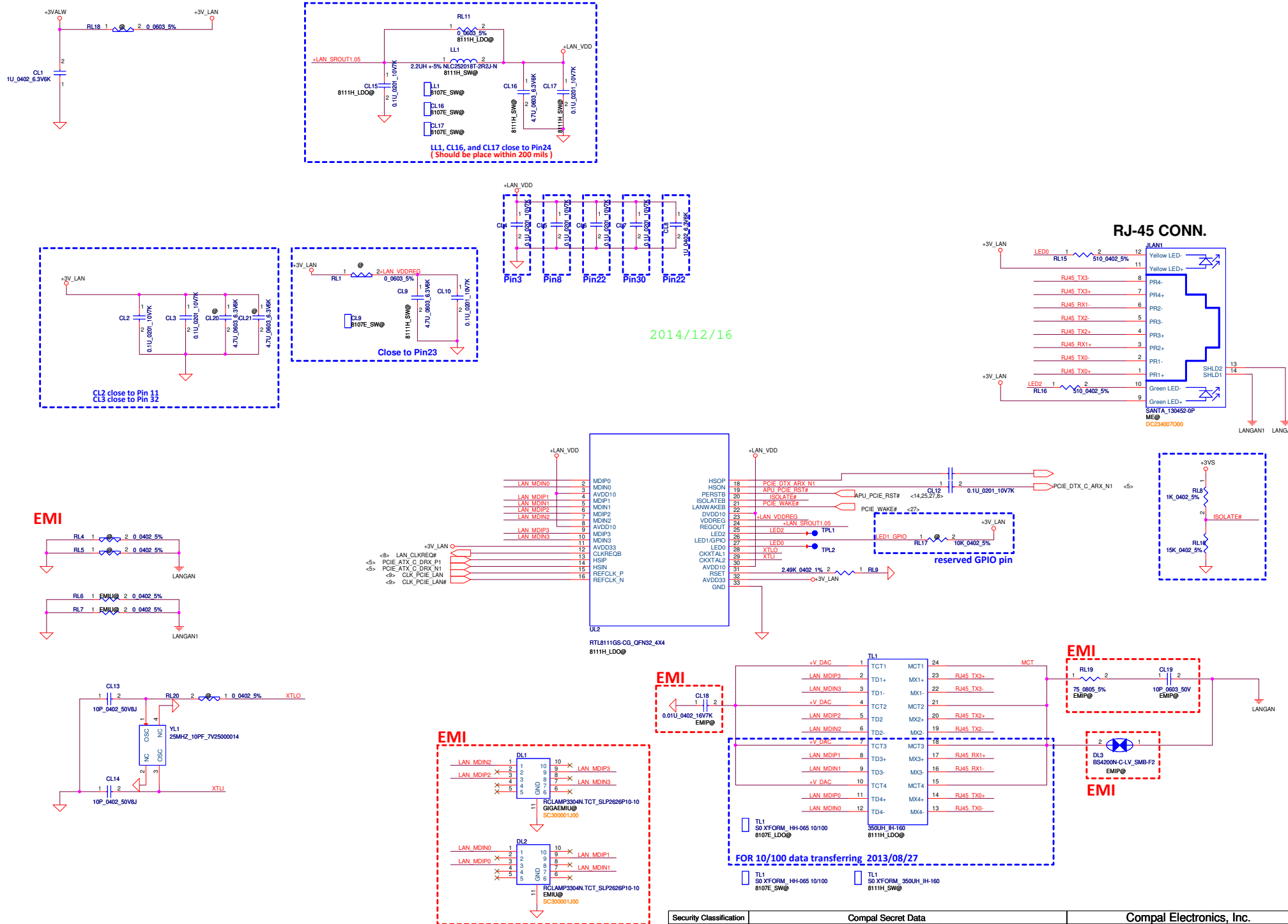
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: Card Reader RTS5220 | | | |
| Size: C | Document Number: LA-C293P | | Rev: 1.0 |
| Date: Monday, March 09, 2015 | | Sheet 25 of 48 | |

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |



Compal Electronics, Inc.

Title: LAN_RTL8111H/RTL8107E

| Size | Document Number | Rev |
|---|---|---|
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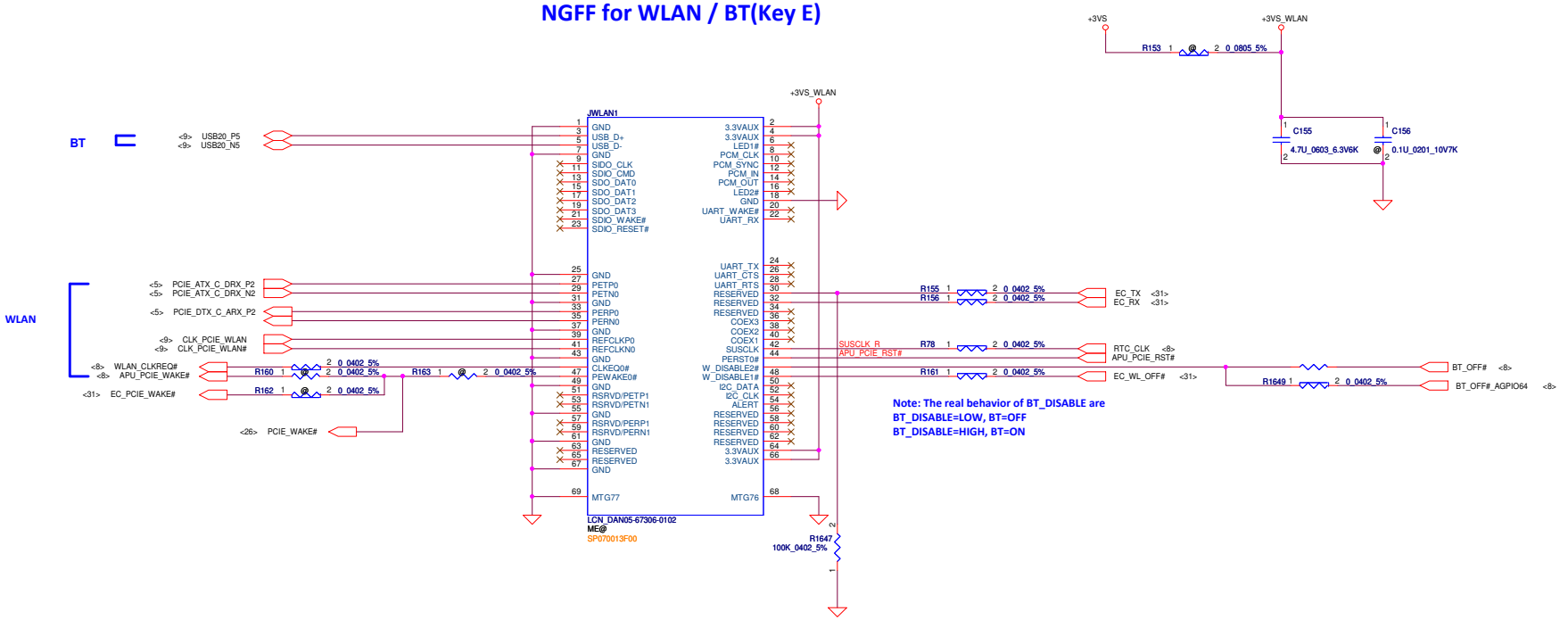
# NGFF for WLAN / BT(Key E)




**Note: The real behavior of BT_DISABLE are**
**BT_DISABLE=LOW, BT=OFF**
**BT_DISABLE=HIGH, BT=ON**

| | | | |
|---|---|---|---|
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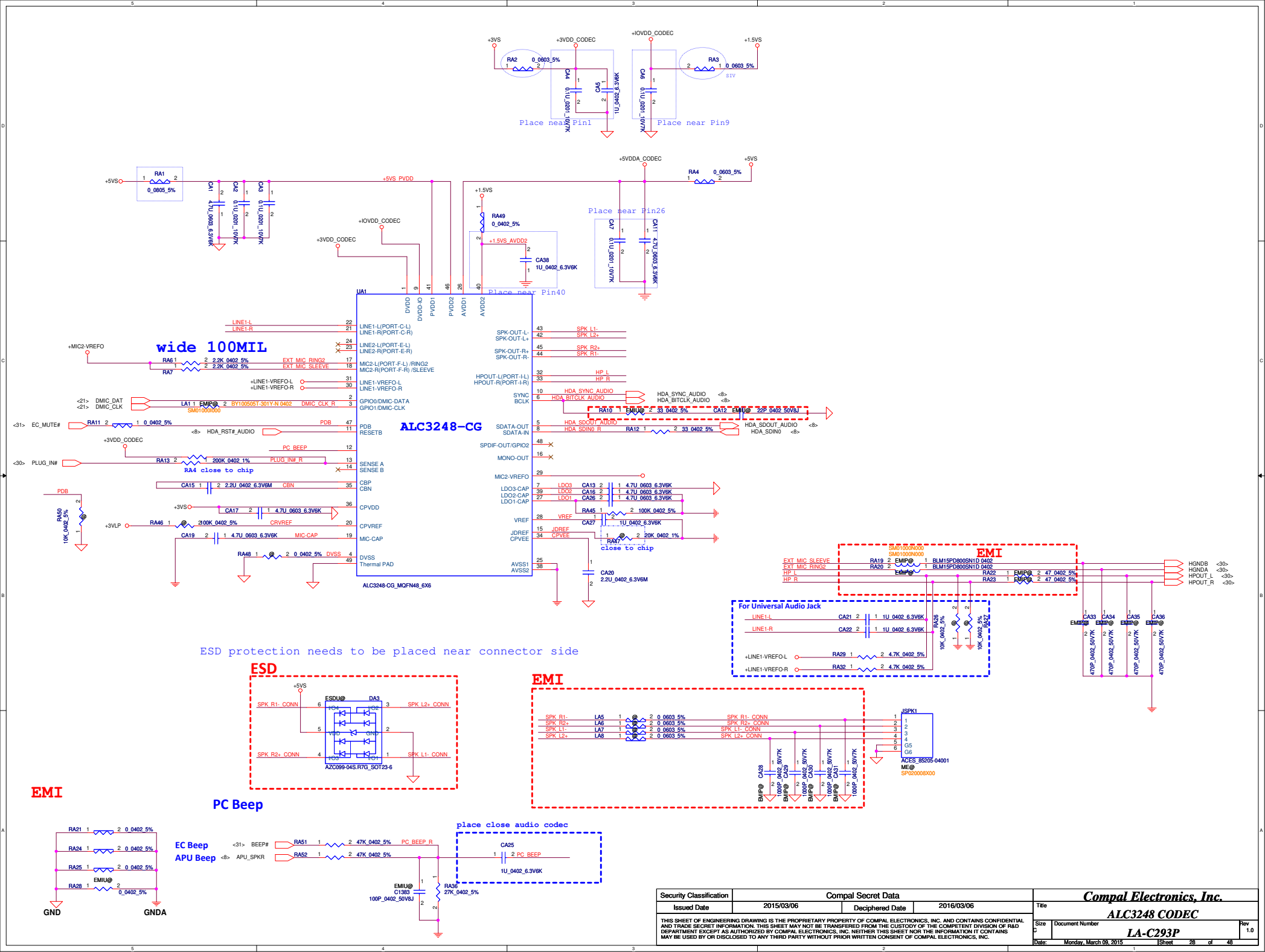
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | NGFF WLAN/BT | | |
| Size C | Document Number LA-C293P | | Rev 1.0 |
| Date: Monday, March 09, 2015 | Sheet 27 of 48 | | |

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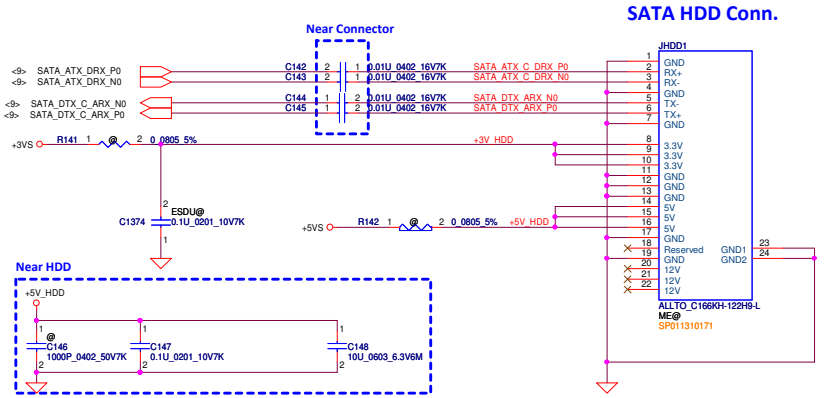
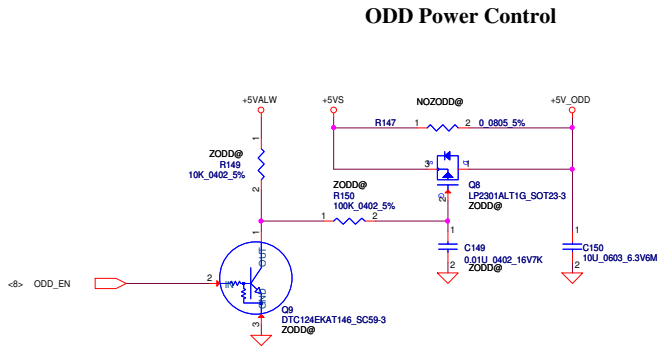
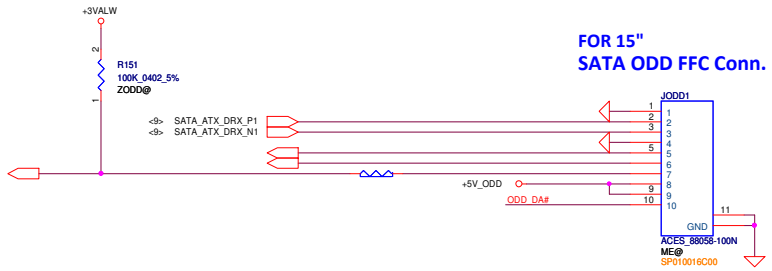
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: ALC3248 CODEC | | | |
| Size: C | Document Number: LA-C293P | | Rev: 1.0 |
| Date: Monday, March 09, 2015 | Sheet: 28 | of: 48 | |

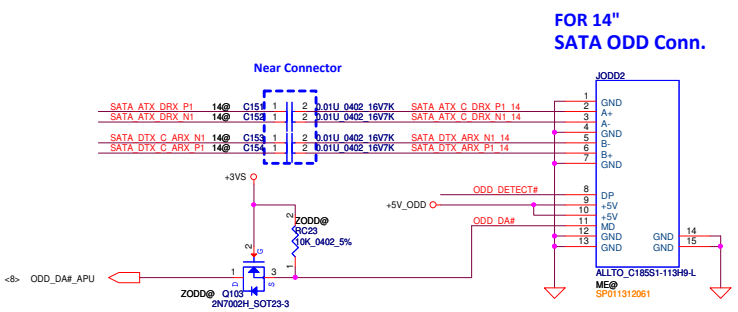
# HDD




# ODD

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|---|---|---|---|
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| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |
| Title | HDD/ODD | | |
| Size C | Document Number LA-C293P | | Rev 1.0 |
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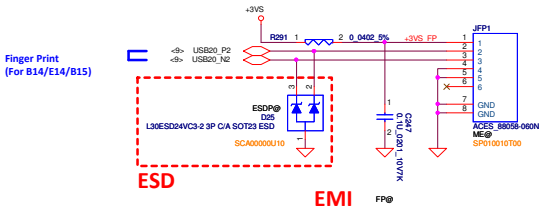
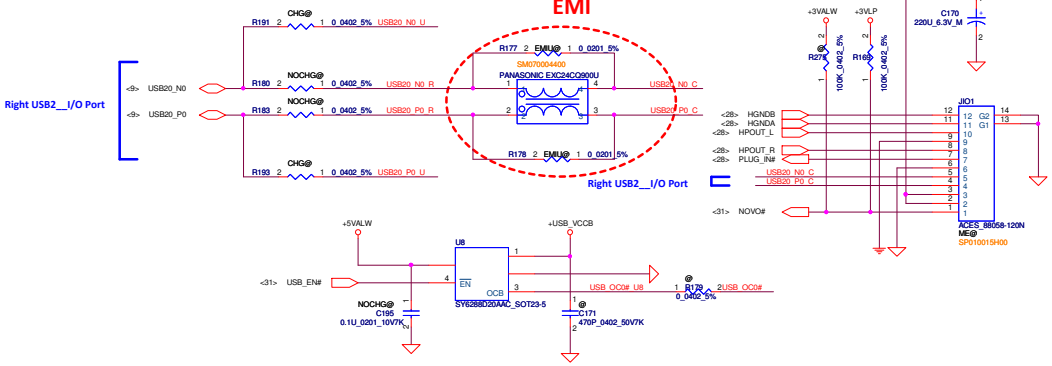
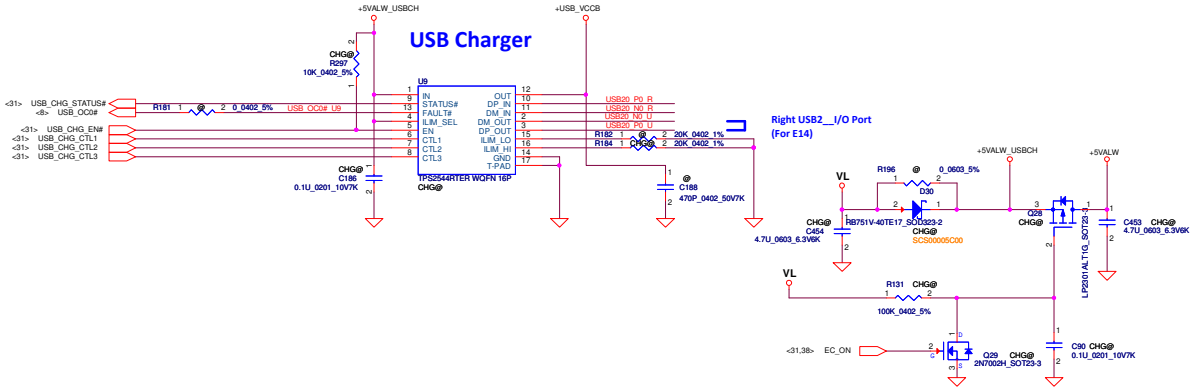
# Finger Print

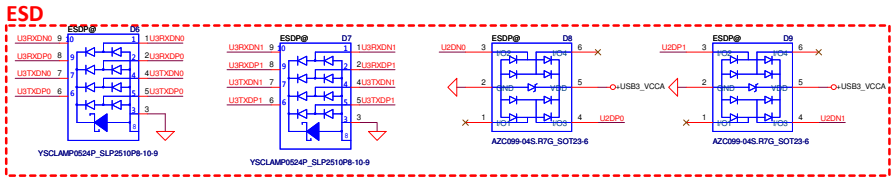



# USB2.0_Port



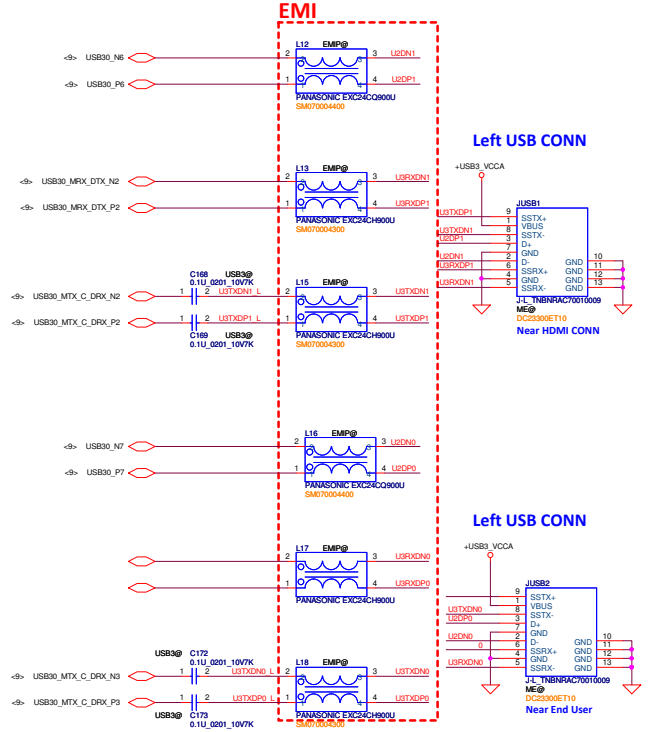




# ESD

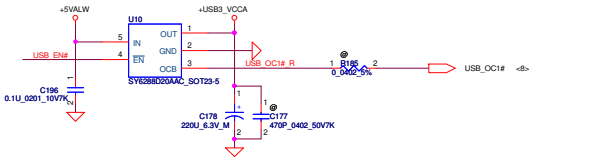



ESD protection needs to be placed near connector side

# USB3.0_Port




Place TX AC coupling Cap (C843~C850). Close to connector

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|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |
| | | | Title: USB Port/FP |
| Size: Custom | Document Number: LA-C293P | | Rev: 1.0 |
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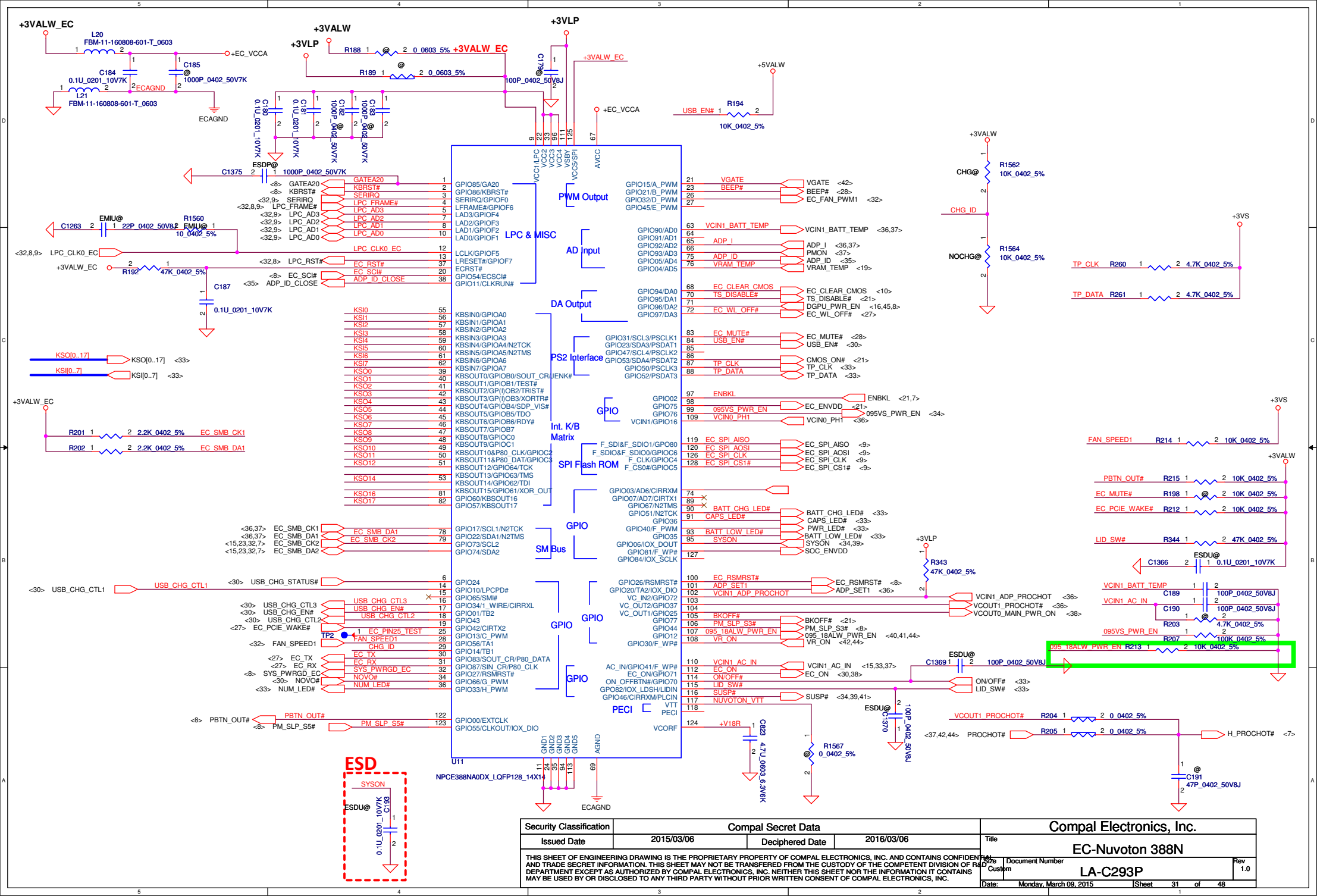


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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |

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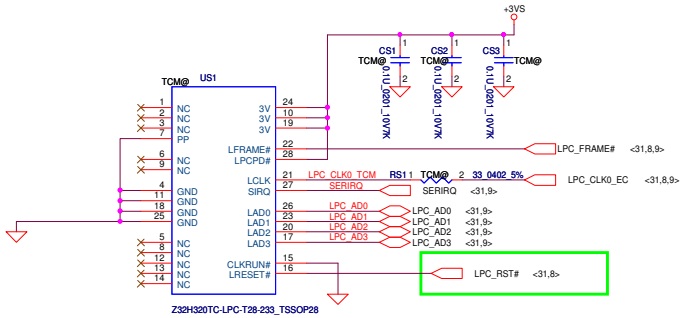
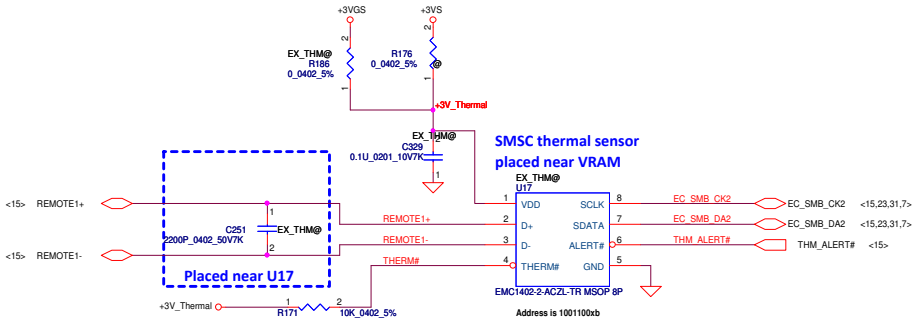
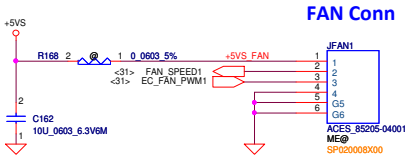
## TCM

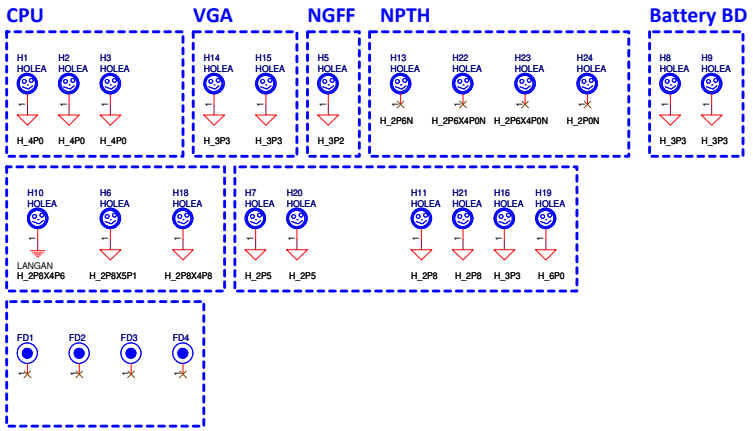



## 2 Channel Thermal Sensor




## FAN Conn

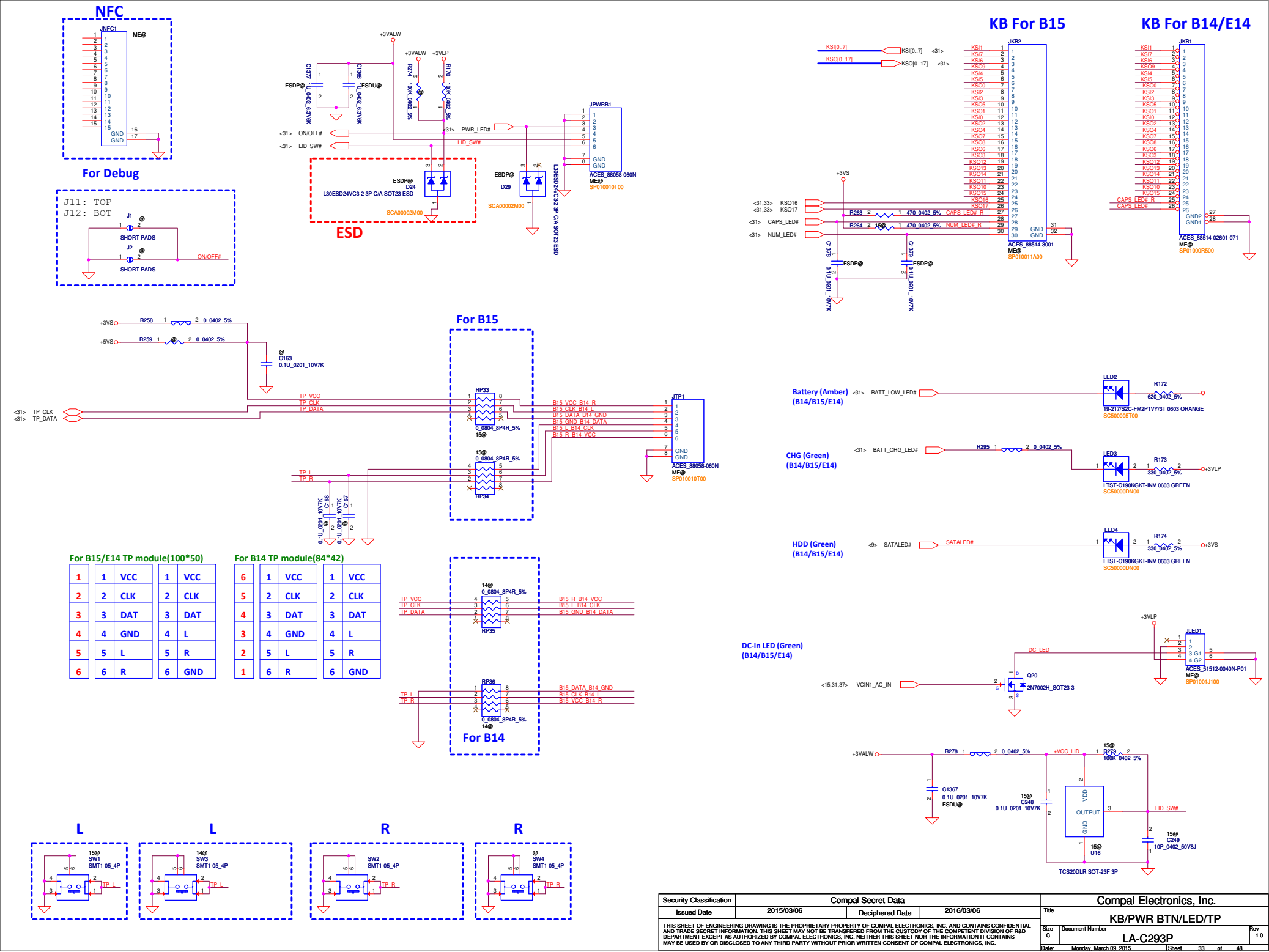



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | EMC1403-2/FAN/Screw Hole/TCM | | |
| Size C | Document Number LA-C293P | | Rev 1.0 |
| Date: Monday, March 09, 2015 | | Sheet 32 of 48 | |

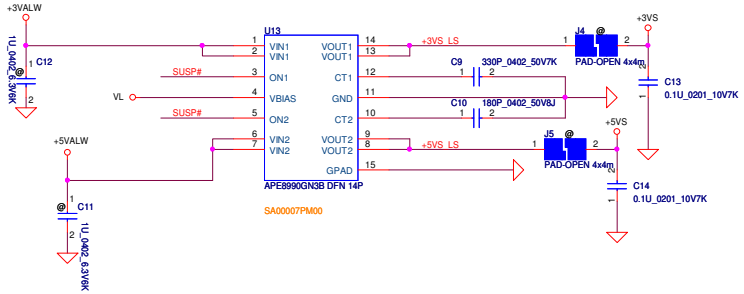



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |

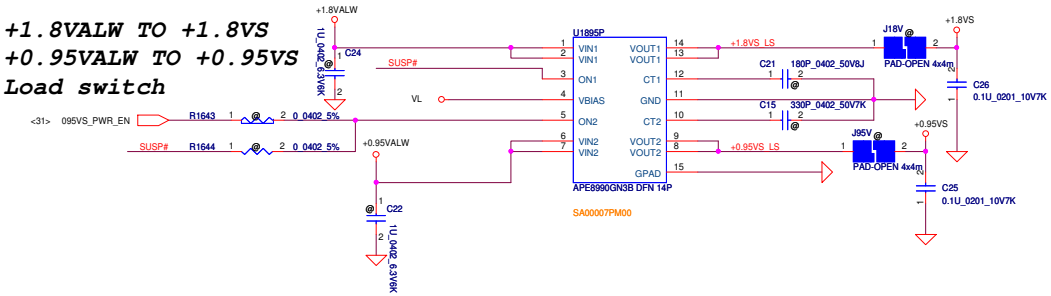


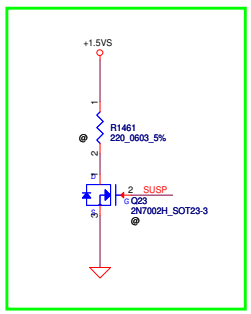
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | KB/PWR BTN/LED/TP | | |
| Size C | Document Number LA-C293P | | Rev 1.0 |
| Date: Monday, March 09, 2015 | Sheet 33 of 48 | | |

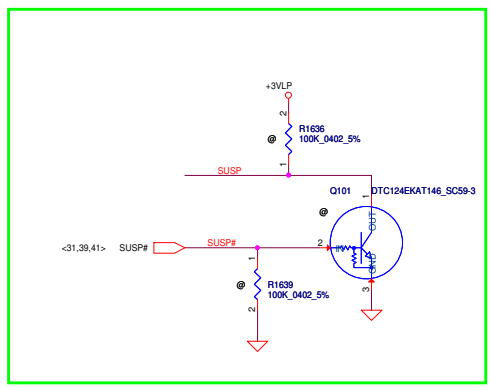
*+5VALW TO +5VS*
*+3VALW TO +3VS*
*Load switch*

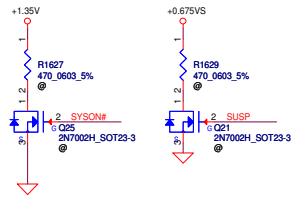


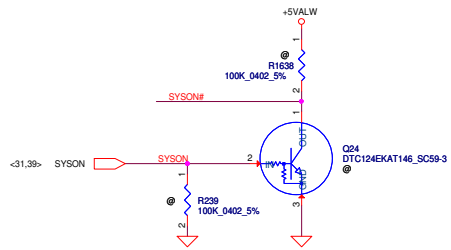

*+1.8VALW TO +1.8VS*
*+0.95VALW TO +0.95VS*
*Load switch*




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |

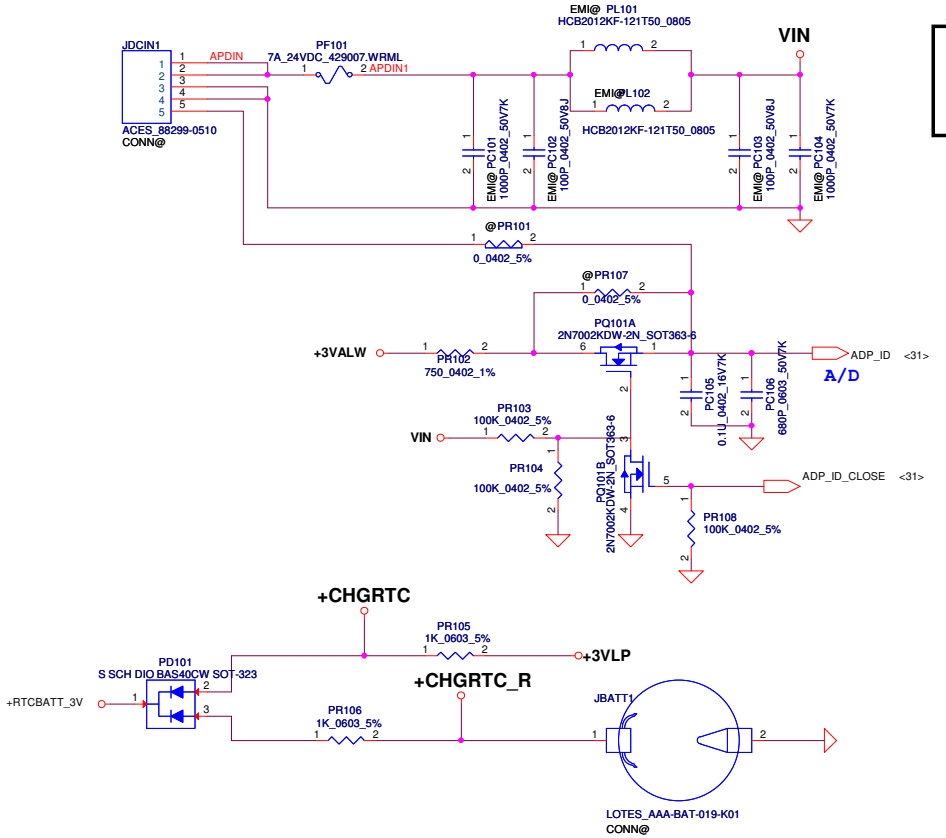


Compal Electronics, Inc.

Title: DC Interface

| Size | Document Number | Rev |
|---|---|---|
| C | LA-C293P | 1.0 |

Date: Monday, March 09, 2015 Sheet 34 of 48




**RTC Battery**

**ADP_ID**

| | | |
|---|---|---|
| AC Adapter | 90W | 65W |
| R(K ohm) | open | 10 |
| ADP_ID(V) | 3.3 | 1.65 |
| Detection voltage | >2.64 | 1.32~1.98 |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |

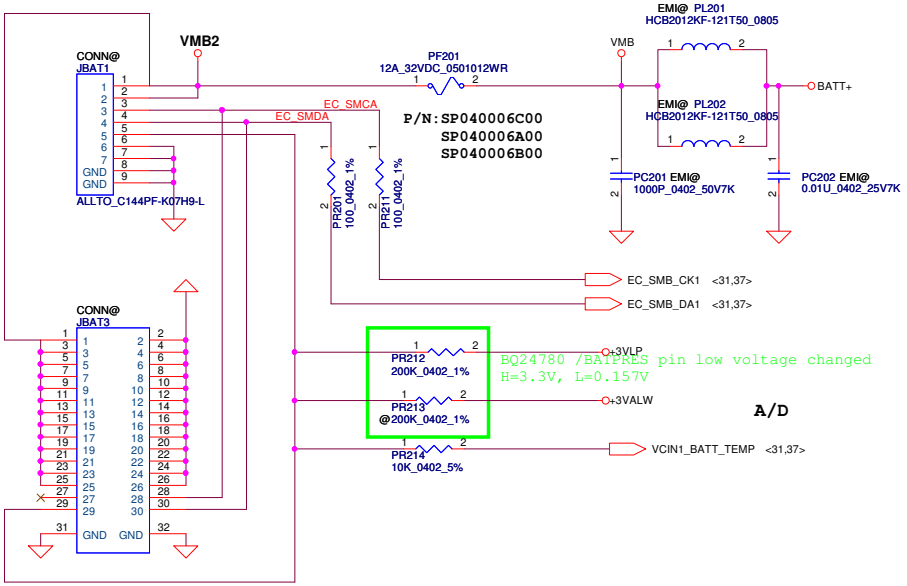


Compal Electronics, Inc.

Title: PWR- DCIN / Vin Detector

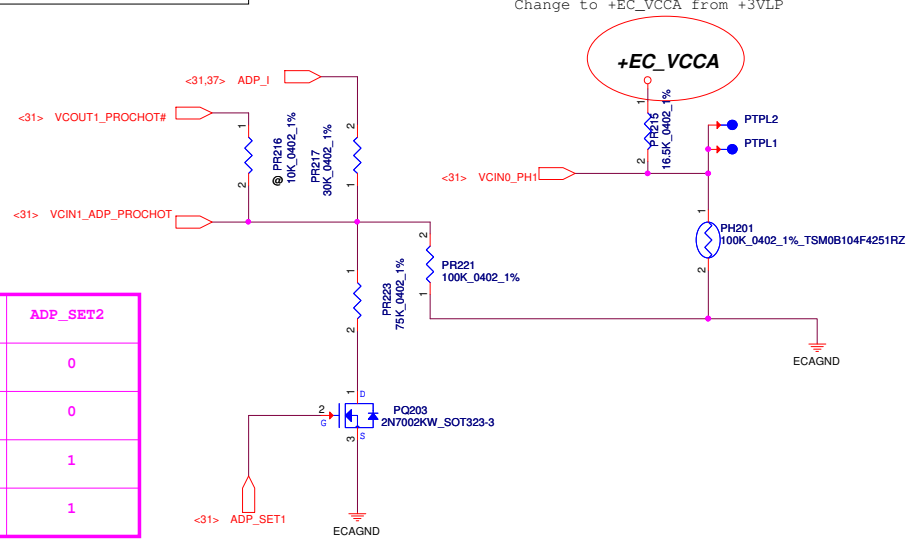
Size: Custom | Document Number: LA-C293P | Rev: 1.0

Date: Monday, March 09, 2015 | Sheet 35 of 48




***PH201 under CPU botten side :***
***CPU thermal protection at 93 +-3 degree C***
***Recovery at 56 +-3 degree C***

20120314
Change to +EC_VCCA from +3VLP

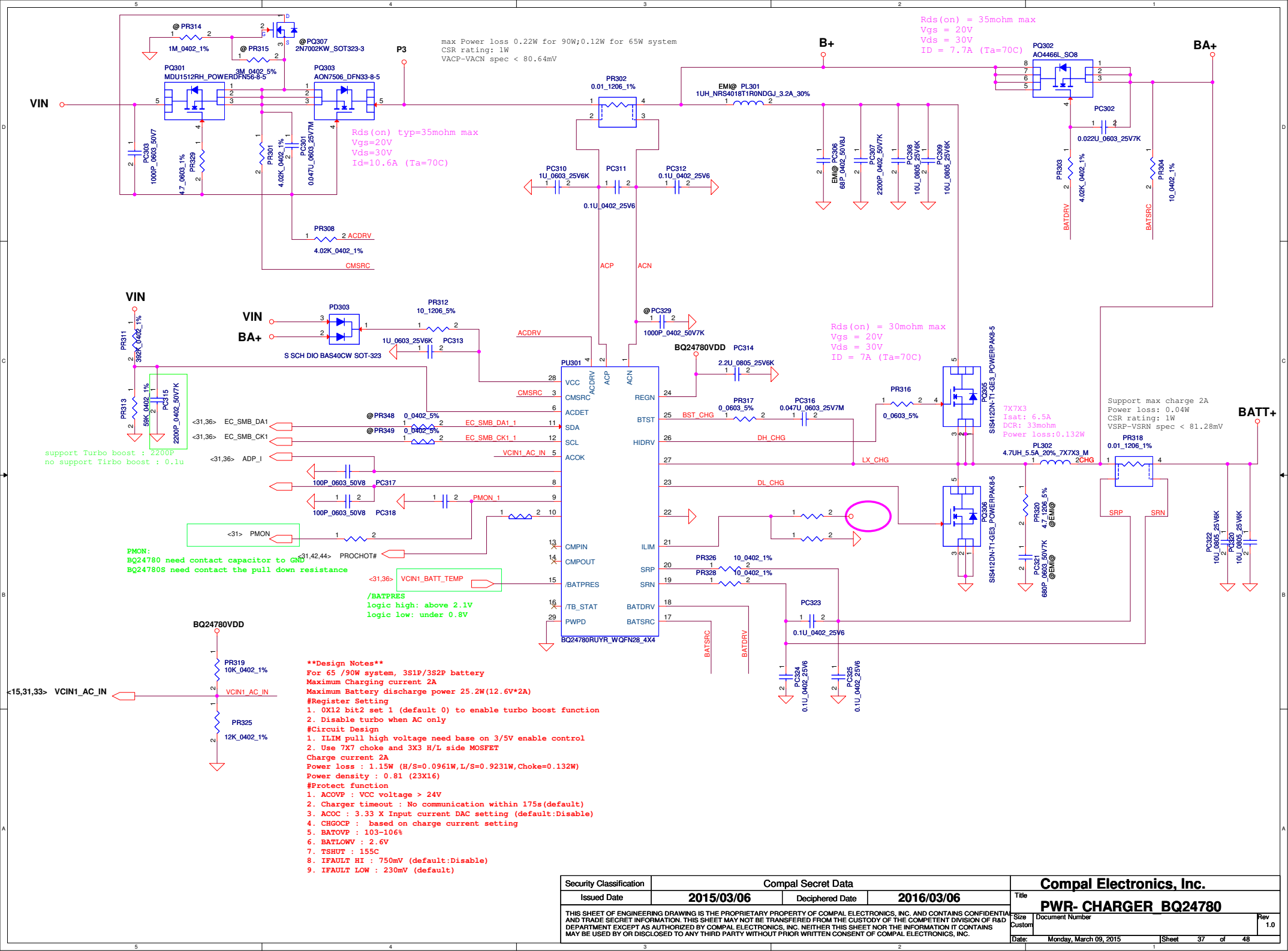



| | | ADP_SET2 |
|---|---|---|
| 45W adapter | 0 | 0 |
| 65W adapter | 1 | 0 |
| 90W adapter | 0 | 1 |
| 135W adapter | 1 | 1 |

***135W: 150W active and 135W recovery***
***90W : 120W active and 90W recovery***
***65W : 85W active and 65W recovery***
***45W : 65W active and 45W recovery***



| Compal Electronics, Inc. | | | |
|---|---|---|---|
| Title | PWR- BATTERY CONN/OTP | | |
| Size: Custom | Document Number: LA-C293P | | Rev: 1.0 |
| Date: Monday, March 09, 2015 | Sheet 36 of 48 | | |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |



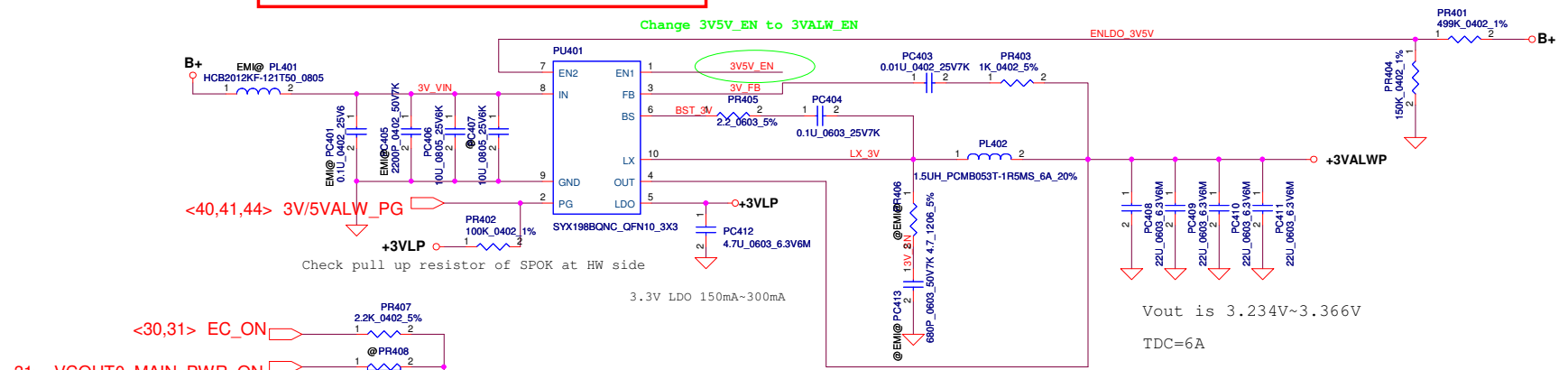
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | PWR- CHARGER_BQ24780 | | |
| Size: Custom | Document Number | | Rev: 1.0 |
| Date: Monday, March 09, 2015 | Sheet 37 of 48 | | |

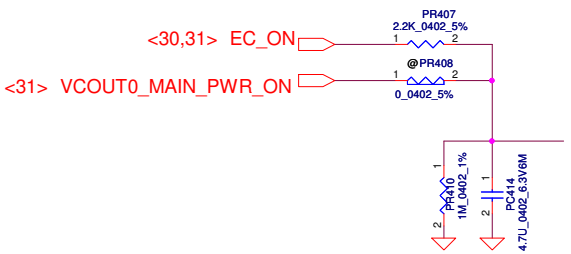
Module model information

SY8208B_V2.mdd

EN1 and EN2 dont't floating

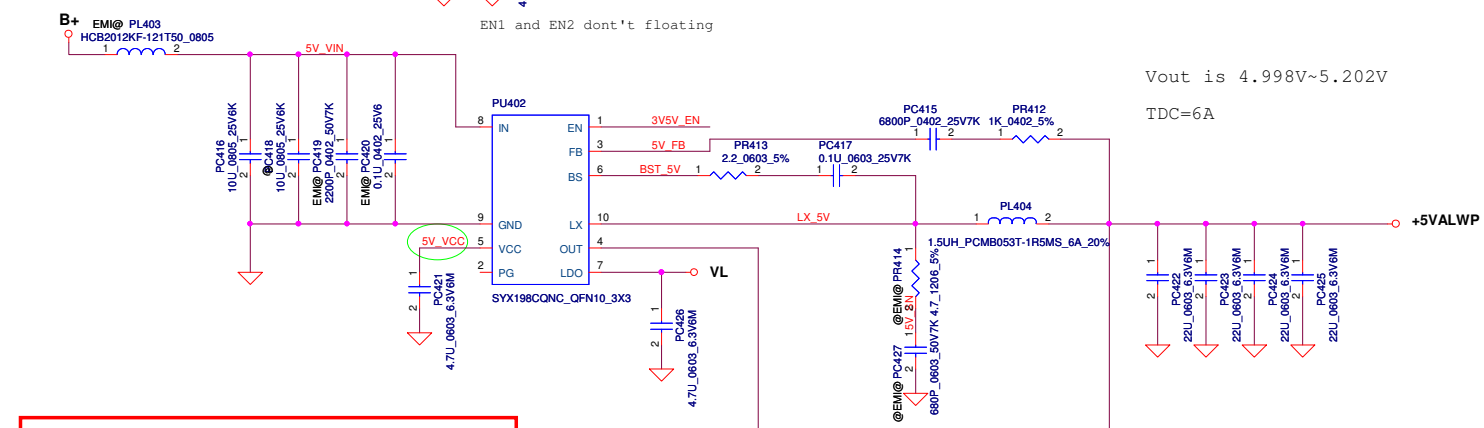
Change 3V5V_EN to 3VALW_EN





EN1 and EN2 dont't floating





5V LDO 150mA~300mA

Module model information

SY8208C_V2.mdd

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |



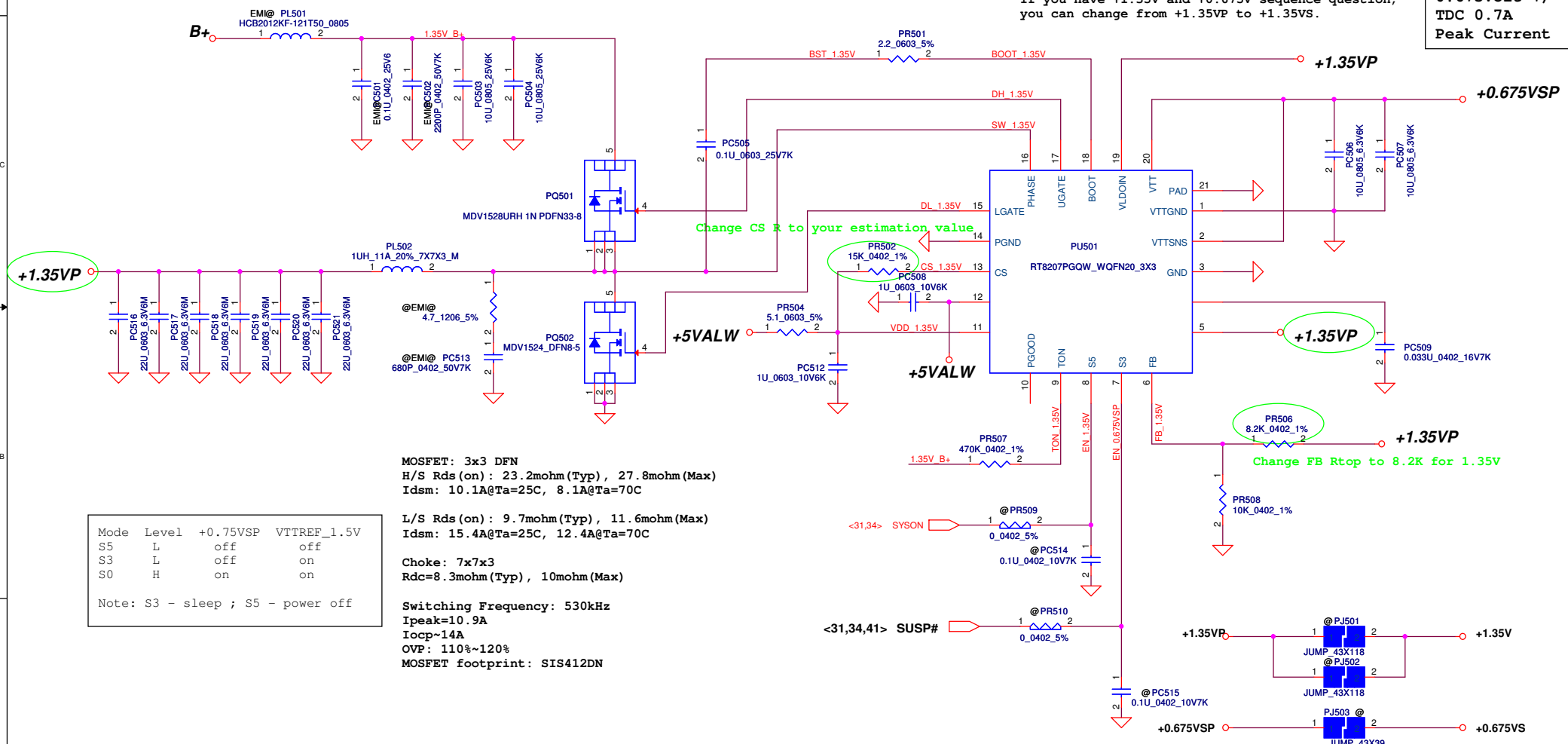
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | PWR- 3VALW/5VALW-SY8208B/C | | |
| Size | Custom | Document Number | LA-C293P |
| Rev | 1.0 | | |
| Date: | Monday, March 09, 2015 | Sheet | 38 of 48 |

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A




MOSFET: 3x3 DFN
H/S Rds(on): 23.2mohm(Typ), 27.8mohm(Max)
Idsm: 10.1A@Ta=25C, 8.1A@Ta=70C

L/S Rds(on): 9.7mohm(Typ), 11.6mohm(Max)
Idsm: 15.4A@Ta=25C, 12.4A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 530kHz
Ipeak=10.9A
Iocp~14A
OVP: 110%~120%
MOSFET footprint: SIS412DN

| Mode | Level | +0.75VSP | VTTREF_1.5V |
|---|---|---|---|
| S5 | L | off | off |
| S3 | L | off | on |
| S0 | H | on | on |

Note: S3 - sleep ; S5 - power off

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |



Compal Electronics, Inc.

Title: PWR-+1.35VP/ +0.675VS

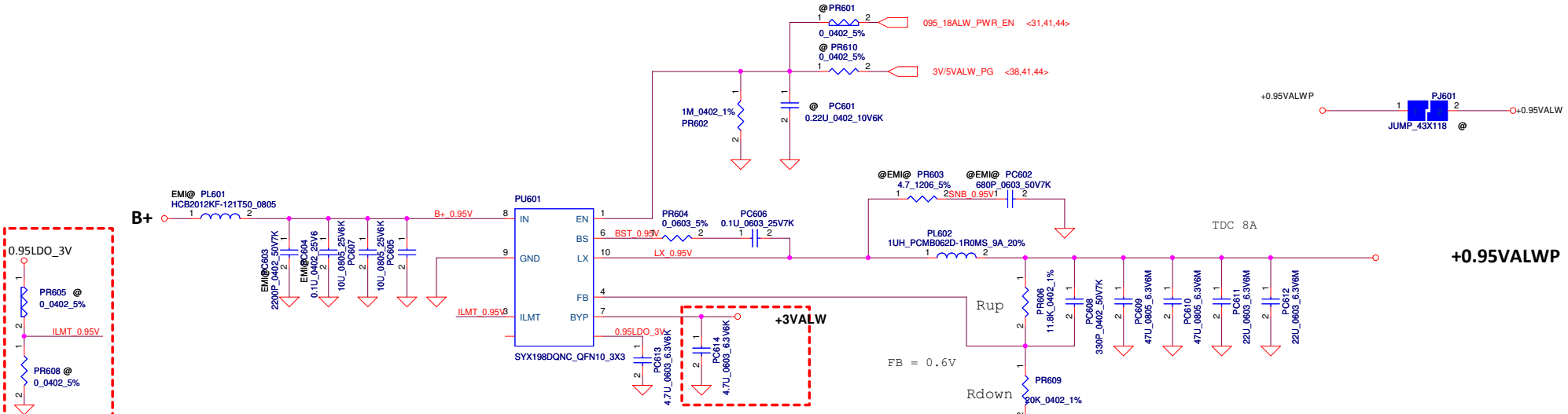
Size: Custom | Document Number: LA-C293P | Rev: 1.0

Date: Monday, March 09, 2015 | Sheet 39 of 48

Module model information

SY8208D_V2.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2




The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

**VFB=0.6V**
**Vout=0.6V* (1+Rup/Rdown)**

**Vout=0.95V**

| | | | |
|---|---|---|---|
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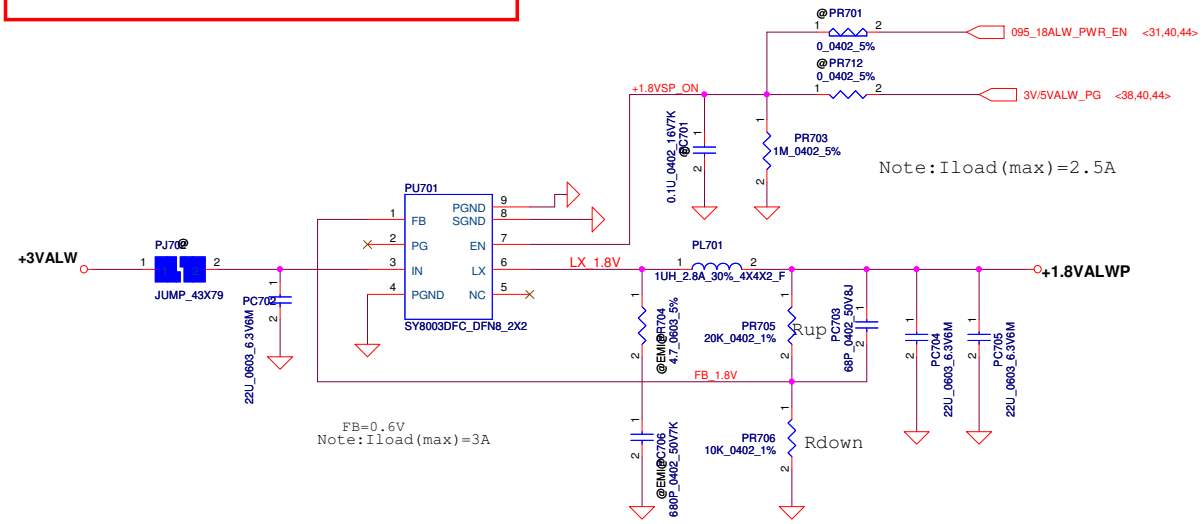
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | PWR- +0.95VALW | | |
| Size: Custom | Document Number: LA-C293P | | Rev: 1.0 |
| Date: Monday, March 09, 2015 | Sheet 40 of 48 | | |

Module model information

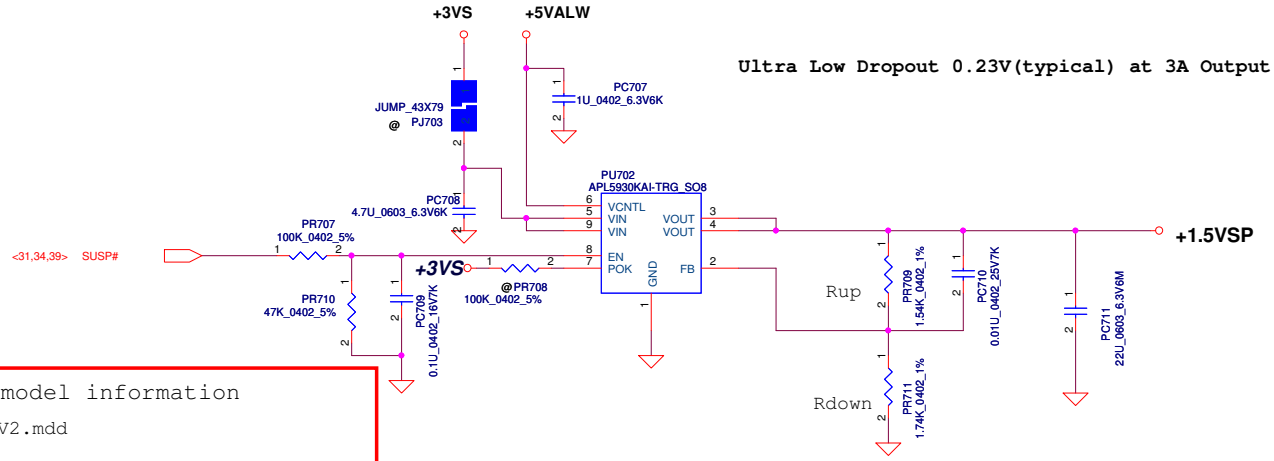
SY8003_V2.mdd



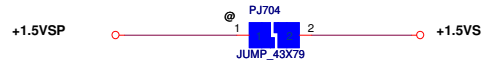


**Note:**
**When design Vin=5V, please stuff snubber to prevent Vin damage**

**Vout=0.6V* (1+Rup/Rdown)**




**Ultra Low Dropout 0.23V(typical) at 3A Output Current**




**Vout=0.8V* (1+Rup/Rdown)**

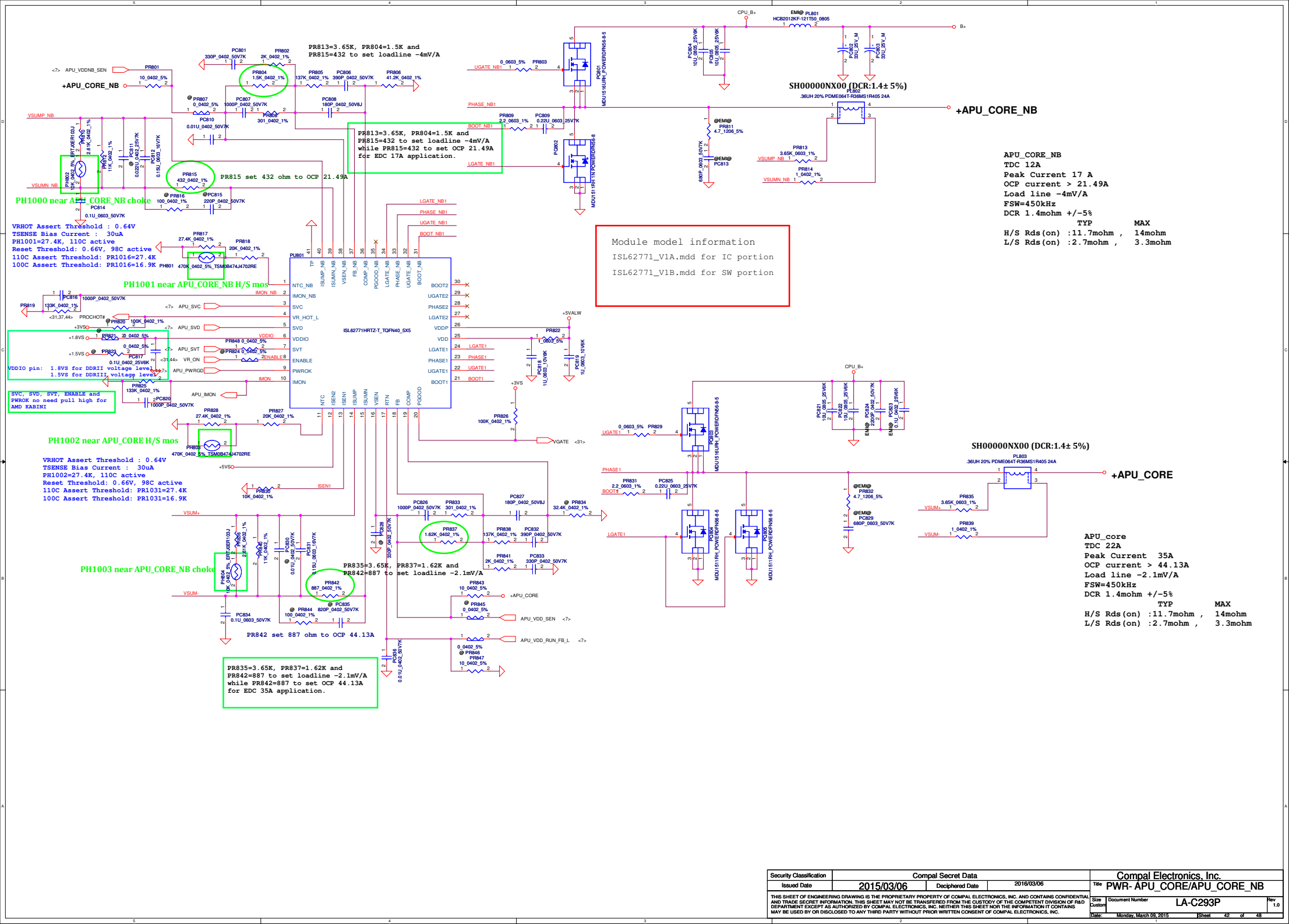
Module model information

APL5930_V2.mdd

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | PWR- +1.8VALW/ +1.5VS | | |
| Size: Custom | Document Number: LA-C293P | | Rev: 1.0 |
| Date: Monday, March 09, 2015 | Sheet 41 of 48 | | |

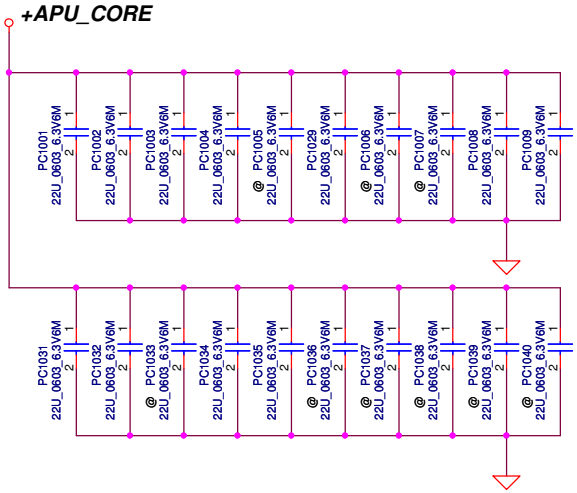



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2015/03/06 | Deciphered Date 2016/03/06 | Title PWR- APU_CORE/APU_CORE_NB |

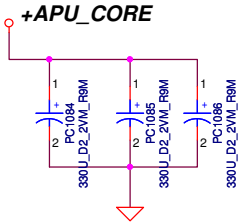


| | | | |
|---|---|---|---|
| Size Custom | Document Number LA-C293P | | Rev 1.0 |
| Date: Monday, March 09, 2015 | Sheet 42 of 48 | | |

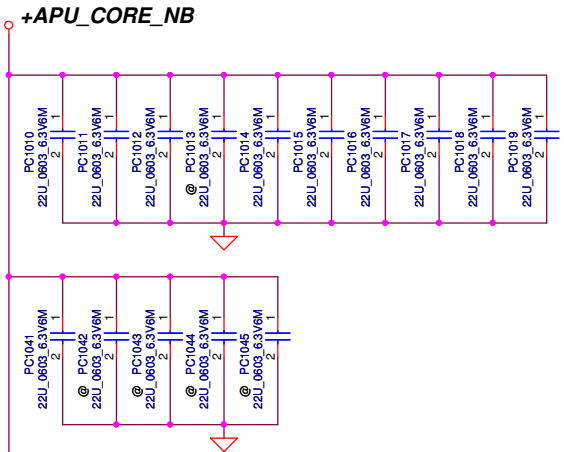
# +APU_CORE




APU_CORE
330uF*3
22uF*20

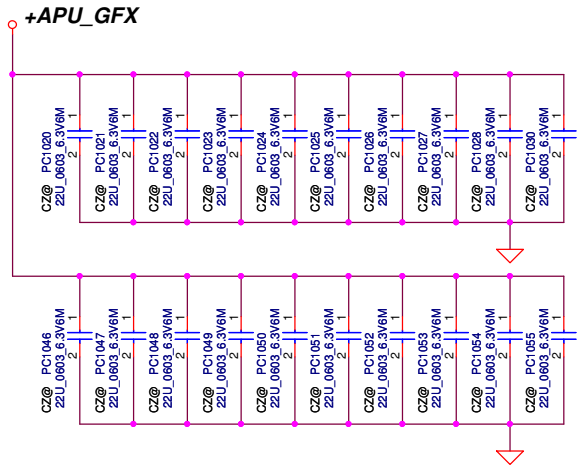



# +APU_CORE_NB

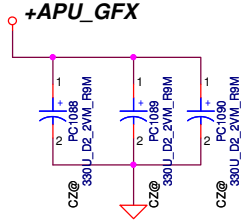



APU_CORENB
330uF*1
22uF*15


# +APU_GFX




APU_CORE
330uF*3
22uF*20

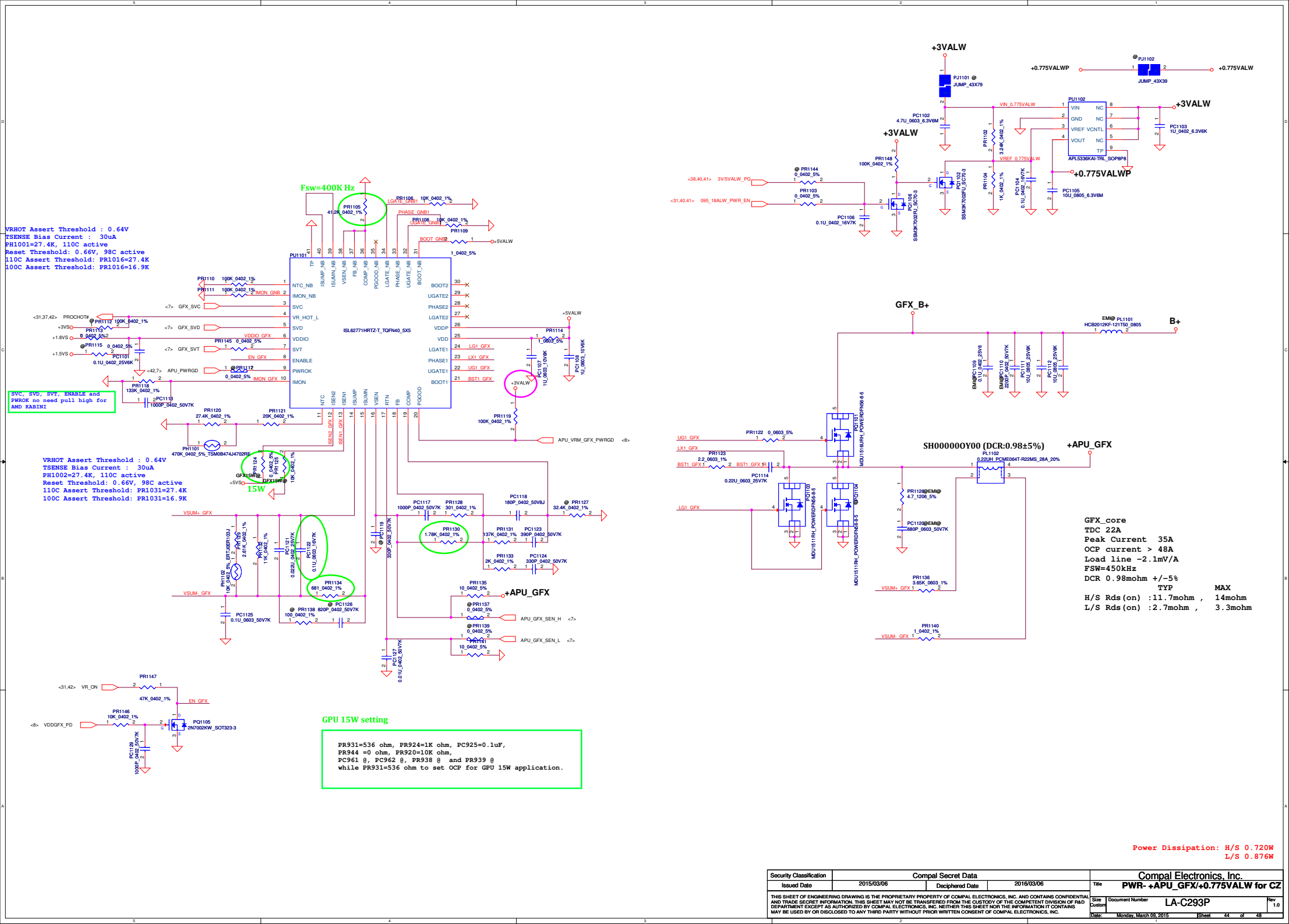



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |



**Compal Electronics, Inc.**

| | | |
|---|---|---|
| Title | +APU_CORE Cap | |
| Size: Custom | Document Number: LA-C293P | Rev: 1.0 |
| Date: Monday, March 09, 2015 | Sheet 43 of 48 | |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2015/03/06 | Deciphered Date 2016/03/06 | Title PWR- +APU_GFX/+0.775VALW for CZ |



| | | | |
|---|---|---|---|
| Size Custom | Document Number LA-C293P | | Rev 1.0 |
| Date: Monday, March 09, 2015 | Sheet 44 of 48 | | |

Module model information

ISL62771_V1A.mdd for IC portion

ISL62771_V1B.mdd for SW portion

+VGA_CORE
AMD EXO PRO
TDC 28A
OCP > 38.55A

VRHOT Assert Threshold : 0.64V
TSENSE Bias Current : 30uA
PH1001=27.4K, 110C active
Reset Threshold: 0.66V, 98C active
110C Assert Threshold: PR1016=27.4K
100C Assert Threshold: PR1016=16.9K

PR912 for MESO
PR914 for EXO pro

SVC, SVD, SVT, ENABLE and PWROK no need pull high for AMD KABINI

VRHOT Assert Threshold : 0.64V
TSENSE Bias Current : 30uA
PH1002=27.4K, 110C active
Reset Threshold: 0.66V, 98C active
110C Assert Threshold: PR1031=27.4K
100C Assert Threshold: PR1031=16.9K

Fsw=400K Hz

ISL62771HRTZ-T_TQFN40_5X5

SH000000Y00 (DCR:0.98±5%)

1/7 change to H=6 CAP_SF000002000

AON6932A_DFN5X6-8-7

GPU 15W setting

PR931=536 ohm, PR924=1K ohm, PC925=0.1uF,
PR944 =0 ohm, PR920=10K ohm,
PC961 @, PC962 @, PR938 @ and PR939 @
while PR931=536 ohm to set OCP for GPU 15W application.

Power Dissipation: H/S 0.720W
L/S 0.876W

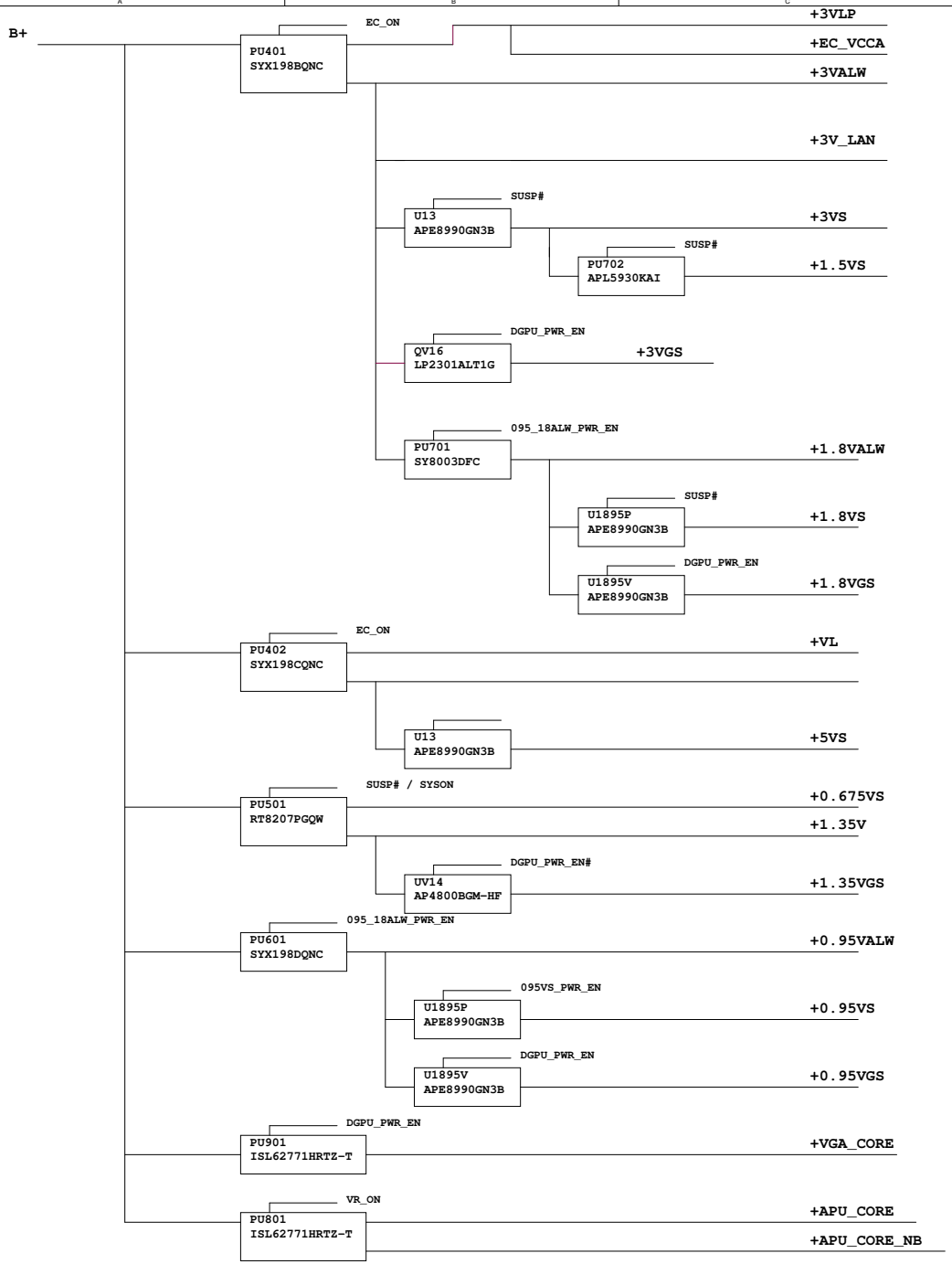
+VGA_CORE



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | PWR- +VGA_CORE | | |
| Size: Custom | Document Number: LA-C293P | | Rev: 1.0 |
| Date: Monday, March 09, 2015 | Sheet 45 of 48 | | |




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |

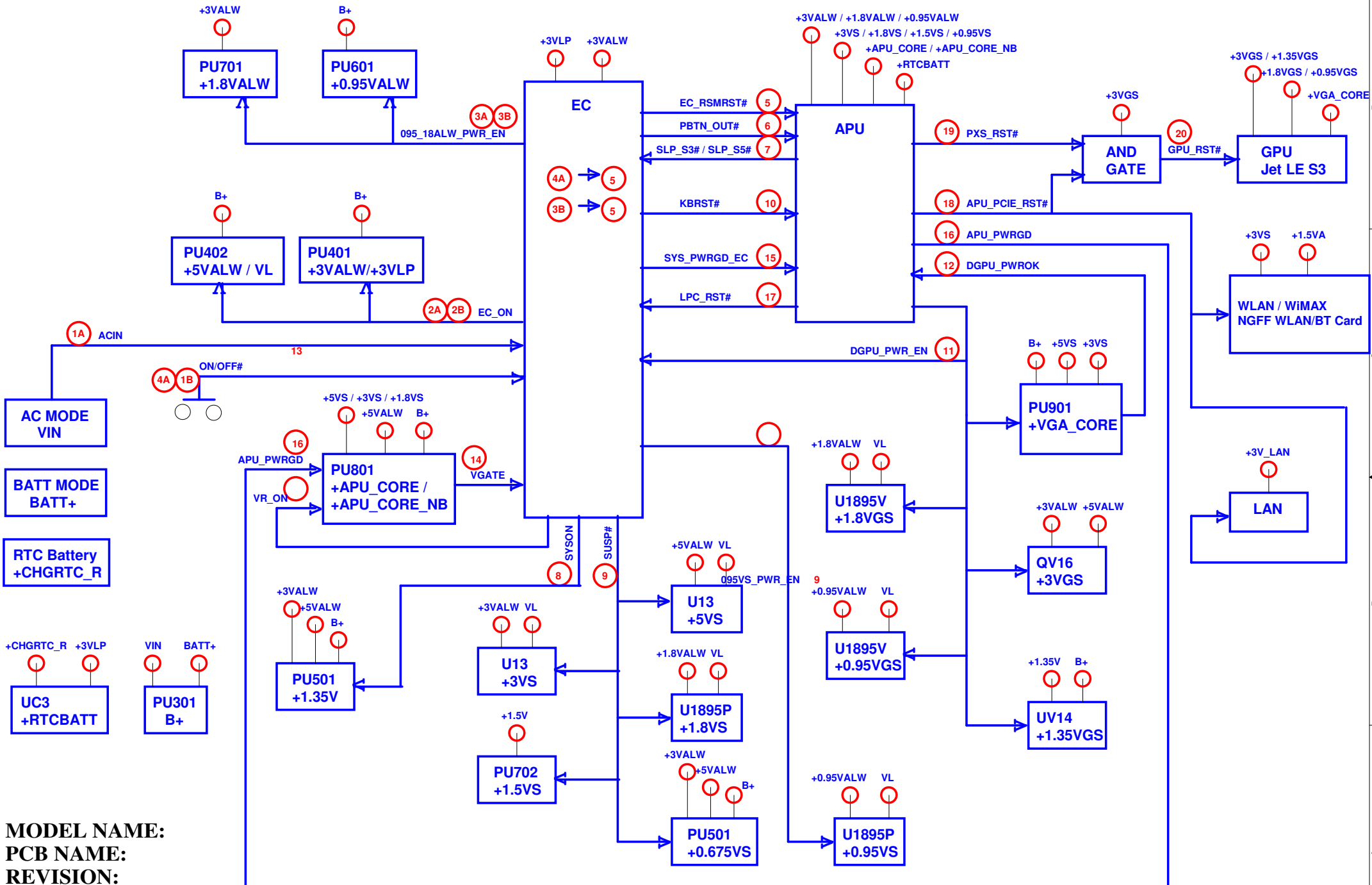


Compal Electronics, Inc.

Title: Power Map

Size: Custom | Document Number: LA-C293P | Rev: 1.0

Date: Monday, March 09, 2015 | Sheet 46 of 48




**MODEL NAME:**
**PCB NAME:**
**REVISION:**
**DATE:** *2014/11/18*

# COMPAL CONFIDENTIAL

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2015/03/06 | Deciphered Date | 2016/03/06 |



Compal Electronics, Inc.

Title: Power Sequence Block

Size: Custom | Document Number: LA-C293P | Rev: 1.0

Date: Monday, March 09, 2015 | Sheet 47 of 48