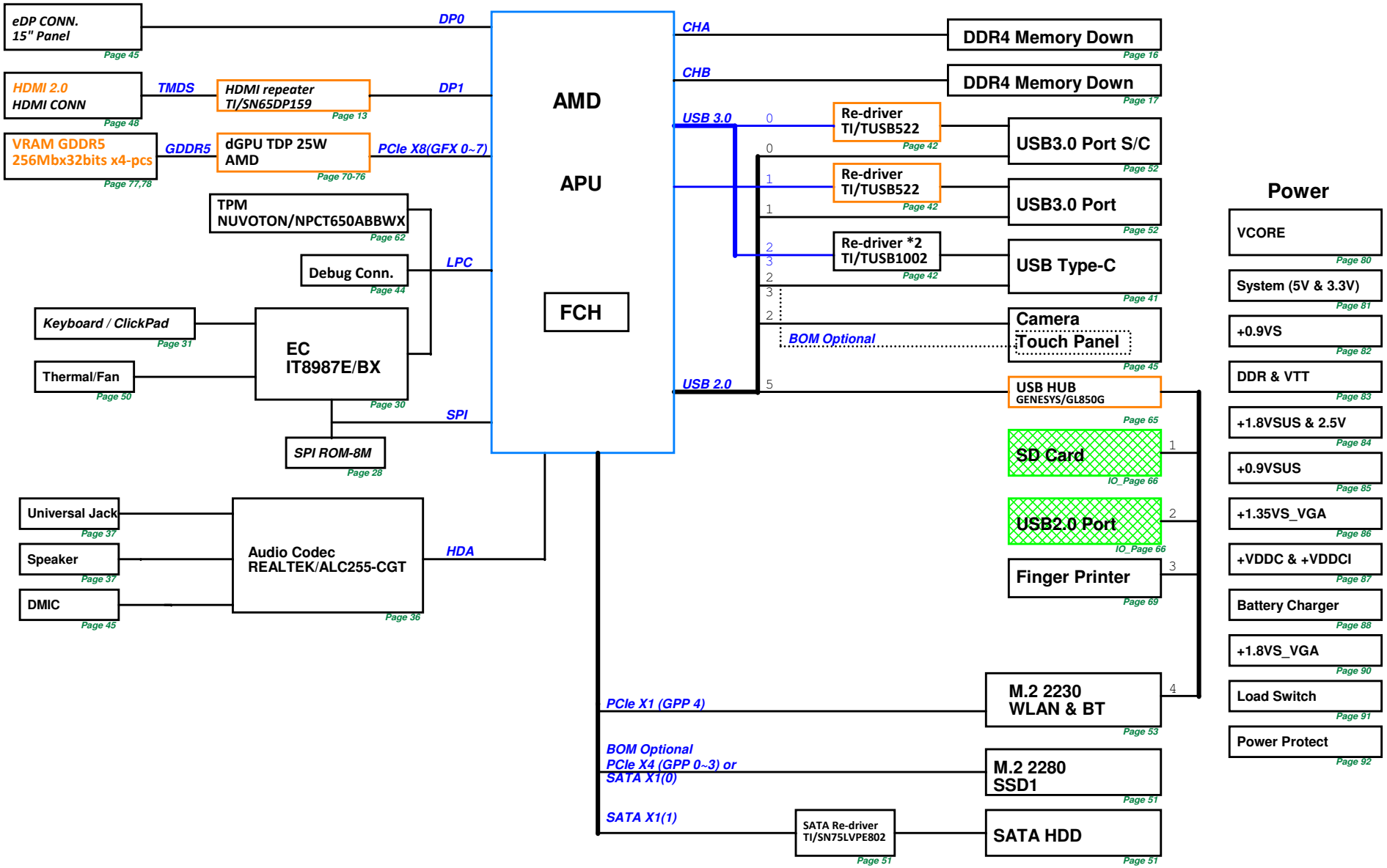
BK5EA_AMD Block Diagram



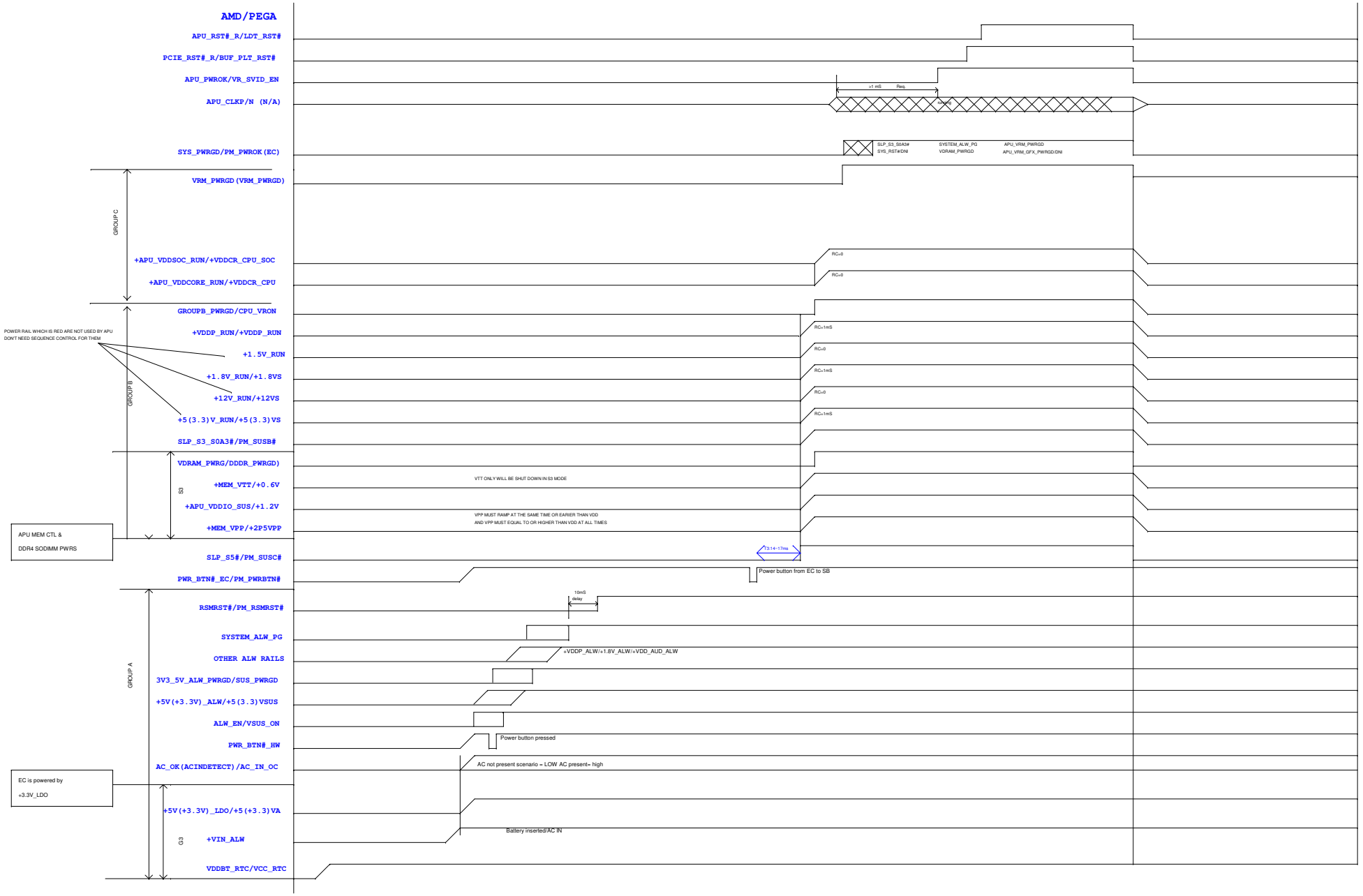
PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON Title : Block Diagram

3G1-HW3 RD Engineer: Jack_Lee

Size	Project Name	Rev
C	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 1 of 94



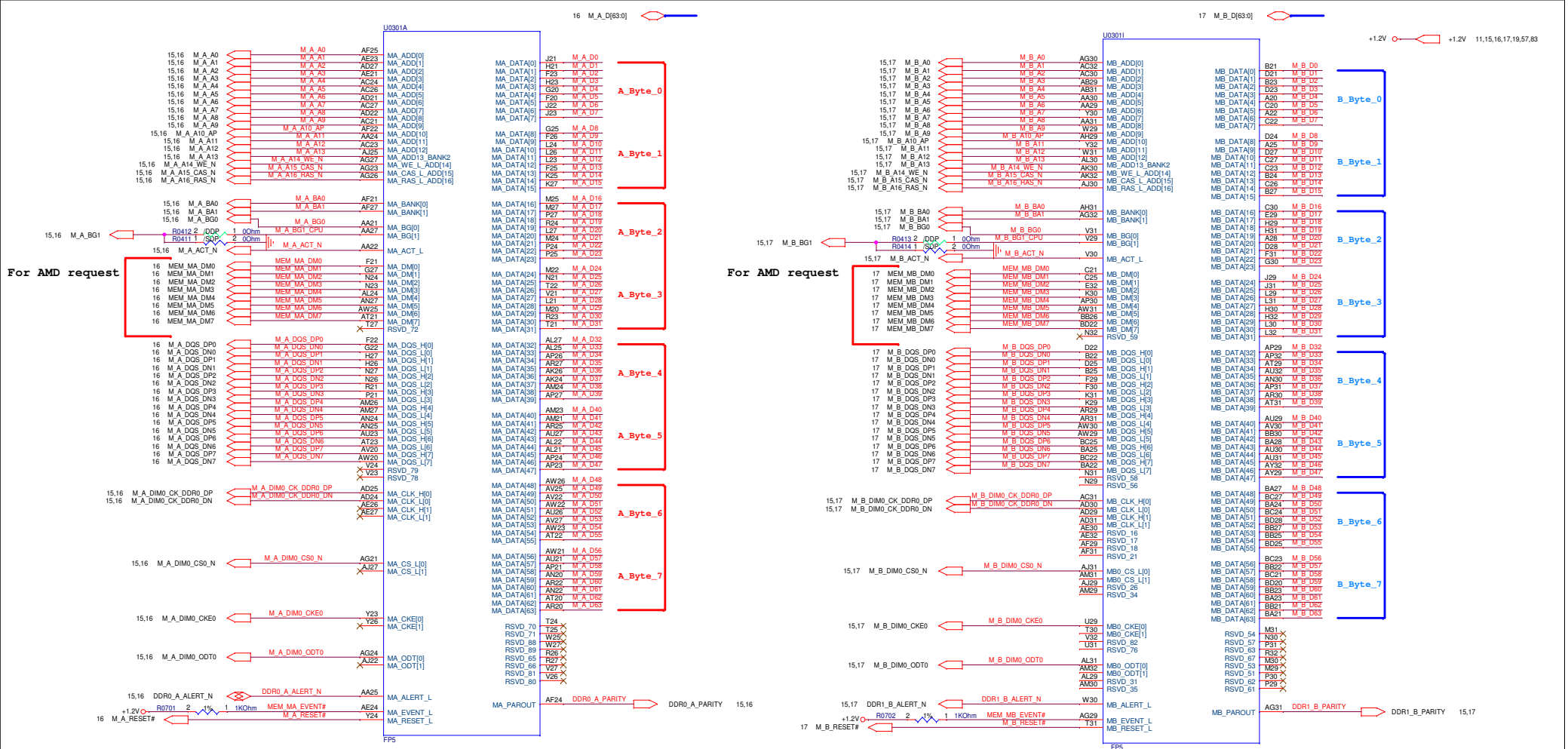
PEGATRON Title : Option

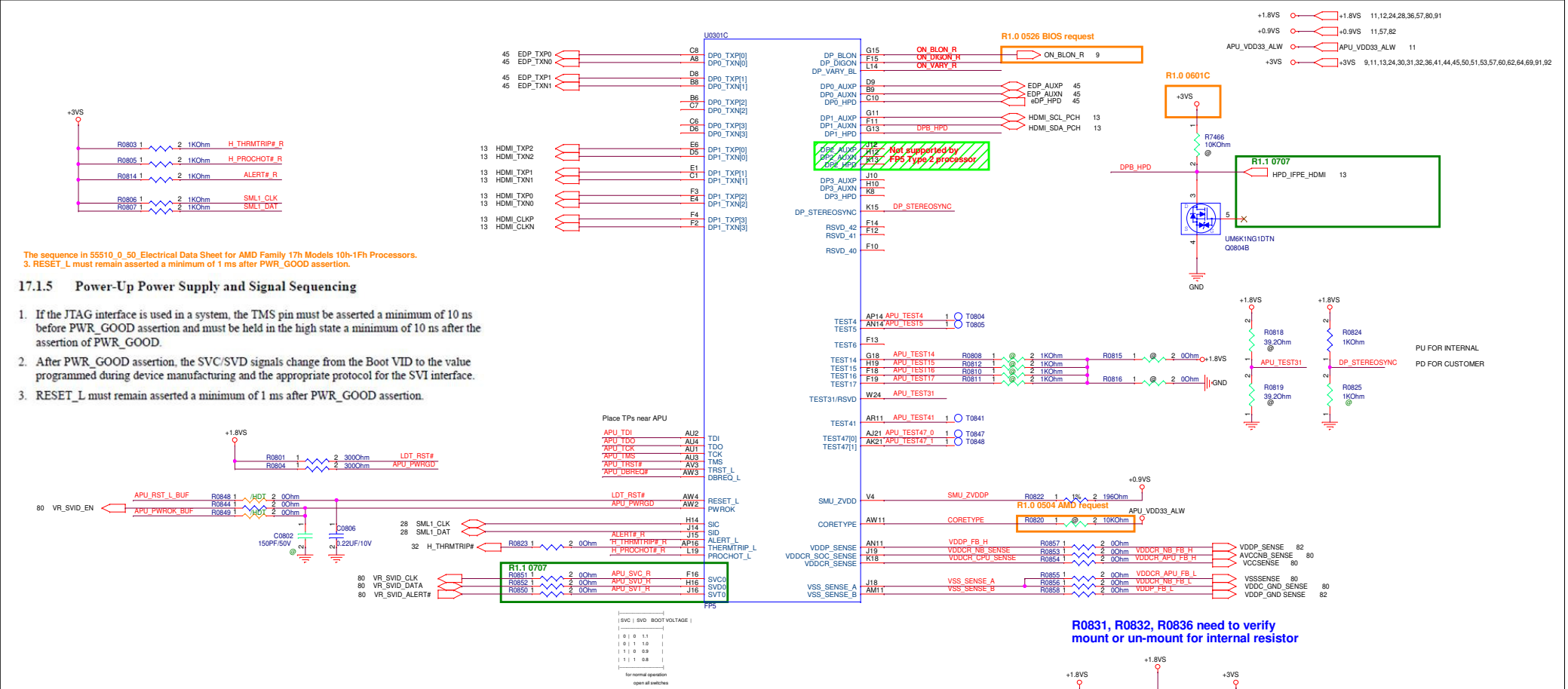
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD Engineer: Jack_Lee

Size	Project Name	Rev
C	BK5BA	1.1

Date: Friday, March 09, 2018 Sheet 2 of 94


16 M_A_D[63:0]
U0301A
For AMD request
A_Byte_0
A_Byte_1
A_Byte_2
A_Byte_3
A_Byte_4
A_Byte_5
A_Byte_6
A_Byte_7
FP5
17 M_B_D[63:0]
U0301I
+1.2V
+1.2V 11,15,16,17,19,57,83
For AMD request
B_Byte_0
B_Byte_1
B_Byte_2
B_Byte_3
B_Byte_4
B_Byte_5
B_Byte_6
B_Byte_7
FP5



The sequence in 55510_0_50_Electrical Data Sheet for AMD Family 17h Models 10h-1Fh Processors.
3. RESET_L must remain asserted a minimum of 1 ms after PWR_GOOD assertion.

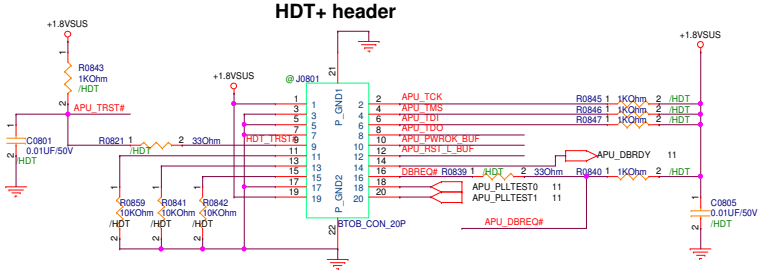
17.1.5 Power-Up Power Supply and Signal Sequencing

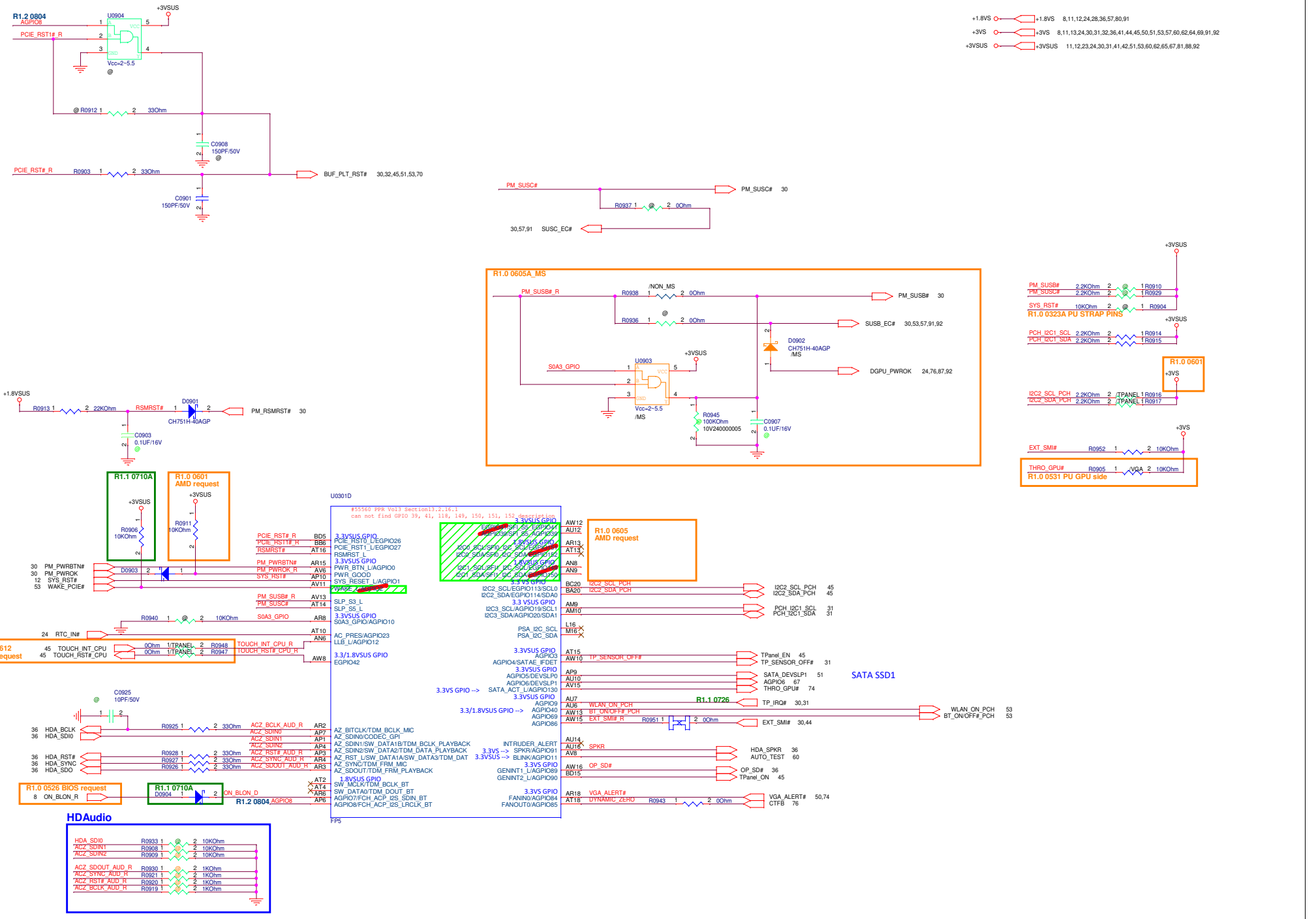
1. If the JTAG interface is used in a system, the TMS pin must be asserted a minimum of 10 ns before PWR_GOOD assertion and must be held in the high state a minimum of 10 ns after the assertion of PWR_GOOD.
2. After PWR_GOOD assertion, the SVC/SVD signals change from the Boot VID to the value programmed during device manufacturing and the appropriate protocol for the SVI interface.
3. RESET_L must remain asserted a minimum of 1 ms after PWR_GOOD assertion.

R0831, R0832, R0836 need to verify mount or un-mount for internal resistor

J0801 Only for EE Verify use

HDT+ header





<Variant Name>

PEGATRON Title: QEVENT_GPIO_SD_AZ

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD Engineer: Jack_Lee

Size	Project Name	Rev
C	BK5BA	1.1

Date: Friday, March 09, 2018 Sheet 9 of 107

TDC 22A/ EDC 35A

U0301F

+VDDCR_CPU_SOC

+VDDCR_CPU

+1.2V

3A

APU_VDDIO_AZ

APU_VDD_33

APU_VDD_18

APU_VDD18_ALW

APU_VDD33_ALW

APU_VDDP_ALW

+0.9VS

+VCC_RTC

FP5

All BU(on bottom side under SOC)

2017/09/05 Power team request
Part number:1AV300000045

DECOUPLING BETWEEN PROCESSOR AND DIMMs
ACROSS VDDIO AND VSS SPLIT

+1.8VSUS

R1.0 0605

0.2A

0.5A

1.5A

0.8A

BO(Bottom side outside SOC)

BU

Q1102
PJA3411

Q1103
BC856BS
07V020000007

R1115 100KOhm

R1114 100KOhm

U0301K

U0301G

U0301H

+5VSUS

APU_PLLTEST0

APU_PLLTEST1

APU_DBRDY

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : PWR & DECOUPLING

BG1-HW3 RD

Engineer: Jack_Lee

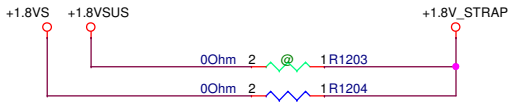
Size C | Project Name BK5BA | Rev 1.1

Date: Friday, March 09, 2018 | Sheet 11 of 107

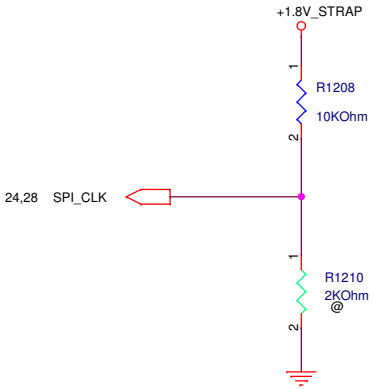
+1.8VSUS → +1.8VSUS 8,9,11,24,28,80,84,87

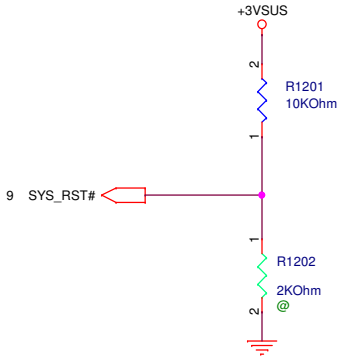
+1.8VS → +1.8VS 8,11,24,28,36,57,80,91

+3VSUS → +3VSUS 9,11,23,24,30,31,41,42,51,53,60,62,65,67,81,88,92



STRAP PINS





STRAP	FUNCTION	DEFINITION
SPI_CLK		1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RST#		1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE

<Variant Name>

PEGATRON Title : STRAPS, SOCKET, HS

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD Engineer: Jack_Lee

Size	Project Name	Rev
B	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 12 of 107

[I2C_EN_PIN = 0] pin strap mode			
Net / Level	H	L	NC
PRE_SEL	Reserved	-2 dB	0 dB
EQ_SEL_A0	Fixed at 14 dB	Fixed at 7.5 dB	Adaptive EQ
SLEW_CTL	fastest data rate	5 ps slow	10 ps slow
HDMI_SEL#_TEST_A1	DVI	HDMI	N/A

+3VS +3VS 8,9,11,24,30,31,32,36,41,44,45,50,51,53,57,60,62,64,69,91,92

[DP159 DDC on]
mount R1306 / R1307 / R1312 / R1313 / R7227 / R7228,
unmount R1308 / R1309 / R1310 / R1311 / R7225 / R7226 / Q7205 / Q7206.

[DP159 DDC snoop only] bypass I2C clock strength
unmount R1306 / R1307 / R1312 / R1313 / R7227 / R7228,
mount R1308 / R1309 / R1310 / R1311 / R7225 / R7226 / Q7205 / Q7206.

[I2C_EN_PIN = 1] I2C control mode
unmount R1320, mount R1319 / R1328 / R1329 / R1332 / R1333,

[I2C_EN_PIN = 0] pin strap mode
mount R1320, unmount R1319 / R1328 / R1329 / R1332 / R1333,
3-level setting (H / L / NC): PRE_SEL / EQ_SEL_A0 /SLEW_CTL
2-level setting (H / L): HDMI_SEL#_TEST_A1

+3VS R1304 1 2 0Ohm +3VS_HDMI 50mA
C1315 10UF/6.3V C1314 0.1UF/6.3V C1316 0.1UF/6.3V GND

VDD_1P2V 325mA
For DP159, VDD is 1V to 1.27V, normally use 1.1V.
C1301 0.1UF/6.3V C1303 0.1UF/6.3V C1304 0.1UF/6.3V C1302 10UF/6.3V C1319 0.1UF/6.3V C1317 0.01UF/16V C1313 0.1UF/6.3V @C1322 10UF/6.3V GND

+3VS_HDMI
R1312 1 @1% 2 47KOhm HDMID_DDI2_AUXN R1311 1 @ 2 0Ohm
R1313 1 @1% 2 47KOhm HDMID_DDI2_AUXP R1310 1 @ 2 0Ohm
R1319 1 @1% 2 64.9KOhm I2C_EN_PIN R1320 1 1% 2 64.9KOhm
R1322 1 @1% 2 64.9KOhm PRE_SEL R1323 1 @1% 2 64.9KOhm
R1324 1 @1% 2 64.9KOhm EQ_SEL_A0 R1325 1 @1% 2 64.9KOhm
R1330 1 @1% 2 64.9KOhm SLEW_CTL R1331 1 @1% 2 64.9KOhm
R1326 1 @1% 2 64.9KOhm HDMI_SEL#_TEST_A1 R1327 1 1% 2 64.9KOhm
GND

8 HDMI_TXP2 C1309 1 2 0.1UF/6.3V HDMID_DDI2_DATA2_P
8 HDMI_TXN2 C1305 1 2 0.1UF/6.3V HDMID_DDI2_DATA2_N
8 HPD_IFPE_HDMI R1303 1 2 1KOhm 1% HPD_IFPE_HDMI_R
8 HDMI_TXP1 C1312 1 2 0.1UF/6.3V HDMID_DDI2_DATA1_P
8 HDMI_TXN1 C1307 1 2 0.1UF/6.3V HDMID_DDI2_DATA1_N
8 HDMI_TXP0 C1311 1 2 0.1UF/6.3V HDMID_DDI2_DATA0_P
8 HDMI_TXN0 C1306 1 2 0.1UF/6.3V HDMID_DDI2_DATA0_N
I2C_EN_PIN
8 HDMI_CLKP C1308 1 2 0.1UF/6.3V HDMID_DDI2_DATA3_P
8 HDMI_CLKN C1310 1 2 0.1UF/6.3V HDMID_DDI2_DATA3_N

R1.1 0707
28,30,50,74 SMB1_CLK
28,30,50,74 SMB1_DAT
+3VS_HDMI VDD_1P2V
R1332 1 @ 2 0Ohm SMB1_CLK_HDMI
R1333 1 @ 2 0Ohm SMB1_DAT_HDMI
PRE_SEL
EQ_SEL_A0
VSADJ
GND R1321 1 1% 2 6.98KOhm

U1301A
GND_3 41
VDD_4 40
SDA_SRC 39
SCL_SRC 38
VCC_2 37
OE 36
GND_2 35
SLEW 34
SDA_SNK 33
SCL_SNK 32
VDD_3 31
OUT_D2n/p_2 30
OUT_D2n/p_1 29
HPD_SNK 28
OUT_D1n/p_2 27
OUT_D1n/p_1 26
OUT_D0n/p_2 25
OUT_D0n/p_1 24
A1/EQ2 23
OUT_CLKn/p_2 22
OUT_CLKn/p_1 21
IN_D2p/n_1 1
IN_D2p/n_2 2
HPD_SRC 3
IN_D1p/n_1 4
IN_D1p/n_2 5
IN_D0p/n_1 6
IN_D0p/n_2 7
I2C_EN 8
IN_CLKp/n_1 9
IN_CLKp/n_2 10
VCC_1 11
VDD_1 12
SCL_CTL/SWAP 13
SDA_CTL/PRE 14
GND_1 15
TERM 16
A0/EQ1 17
VSADJ 18
NC 19
VDD_2 20
TDP158RSBR
HDMID_DDI2_AUXN
HDMID_DDI2_AUXP
OE
SLEW_CTL
HDMI_SEL#_TEST_A1
VDD_1P2V
GND

R1306 1 2 0Ohm
R1307 1 2 0Ohm
+3VS_HDMI
C1318 1 2 0.1UF/6.3V GND
R1308 1 @ 2 0Ohm
R1309 1 @ 2 0Ohm
HDMI_CTRLDATA_C 48
HDMI_CTRCLK_C 48
HDMI_TMDSD_DATA2_P 48
HDMI_TMDSD_DATA2_N 48
HDMI_HOTPLUG_DET 48
HDMI_TMDSD_DATA1_P 48
HDMI_TMDSD_DATA1_N 48
HDMI_TMDSD_DATA0_P 48
HDMI_TMDSD_DATA0_N 48
HDMI_TMDSD_CLK_P 48
HDMI_TMDSD_CLK_N 48

R1.1 0707
2KOhm R1329 +3VS_HDMI
2KOhm R1328
HDMI_SDA_PCH 8
HDMI_SCL_PCH 8

+5VS +3VS
R1337 4.7Ohm SR1301 NB_R0402_20MIL_SMALL
R1336 1 2 10KOhm
U1302
POK 1
VEN 2
VIN 3
VPP 4
GND2 9
GND1 8
ADJ 7
VO 6
NC 5
G9661-25ADJF11U
C1323 1UF/6.3V 1AT200000068
C1325 10UF/6.3V
R1334 23.7KOhm
R1335 47KOhm
VDD_1P2V
C1324 10UF/6.3V

U1301B
GND_4 42
GND_5 43
GND_6 44
GND_7 45
GND_8 46
GND_9 47
GND_10 48
GND_11 49
GND_12 50
TDP158RSBR
GND

PEGATRON
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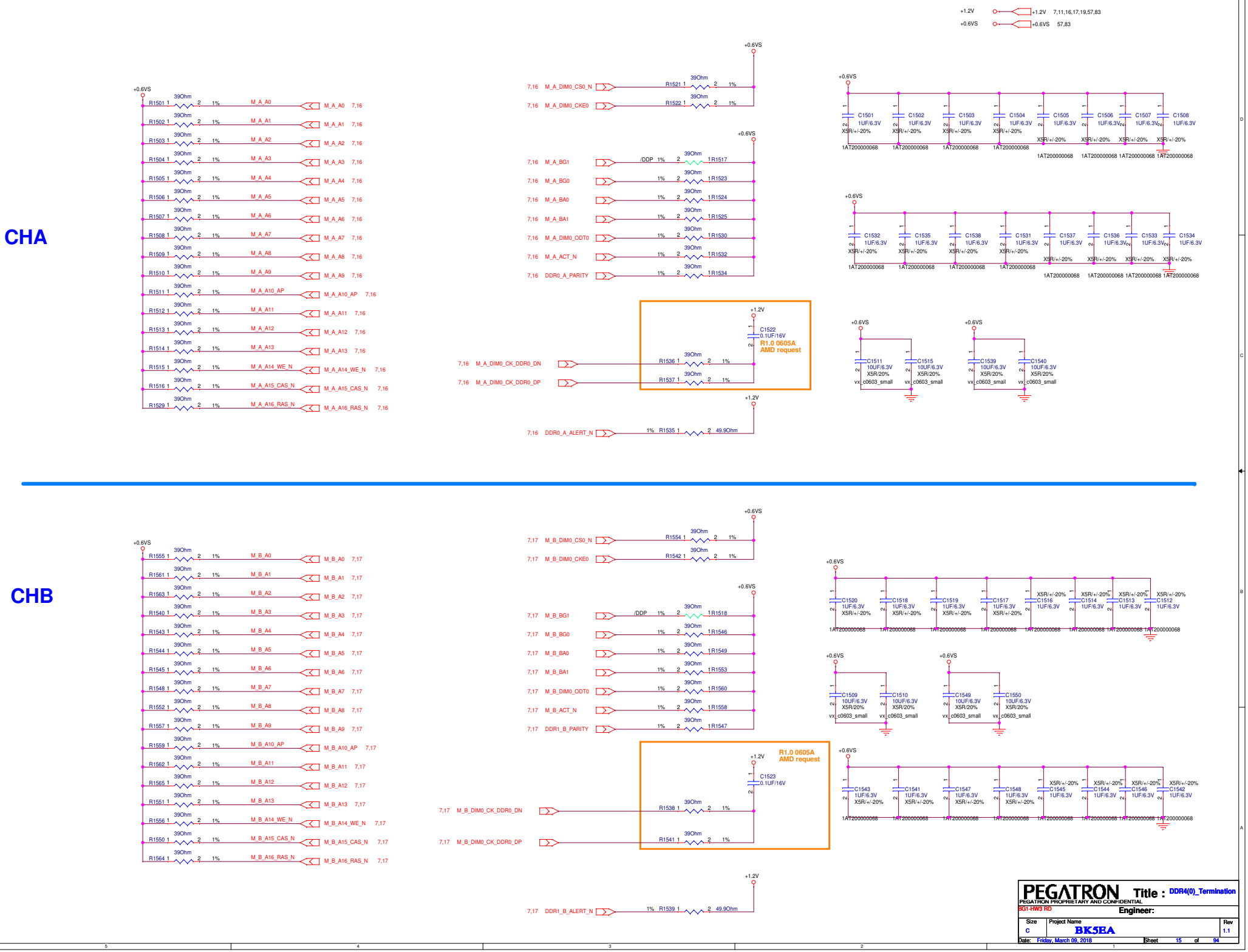
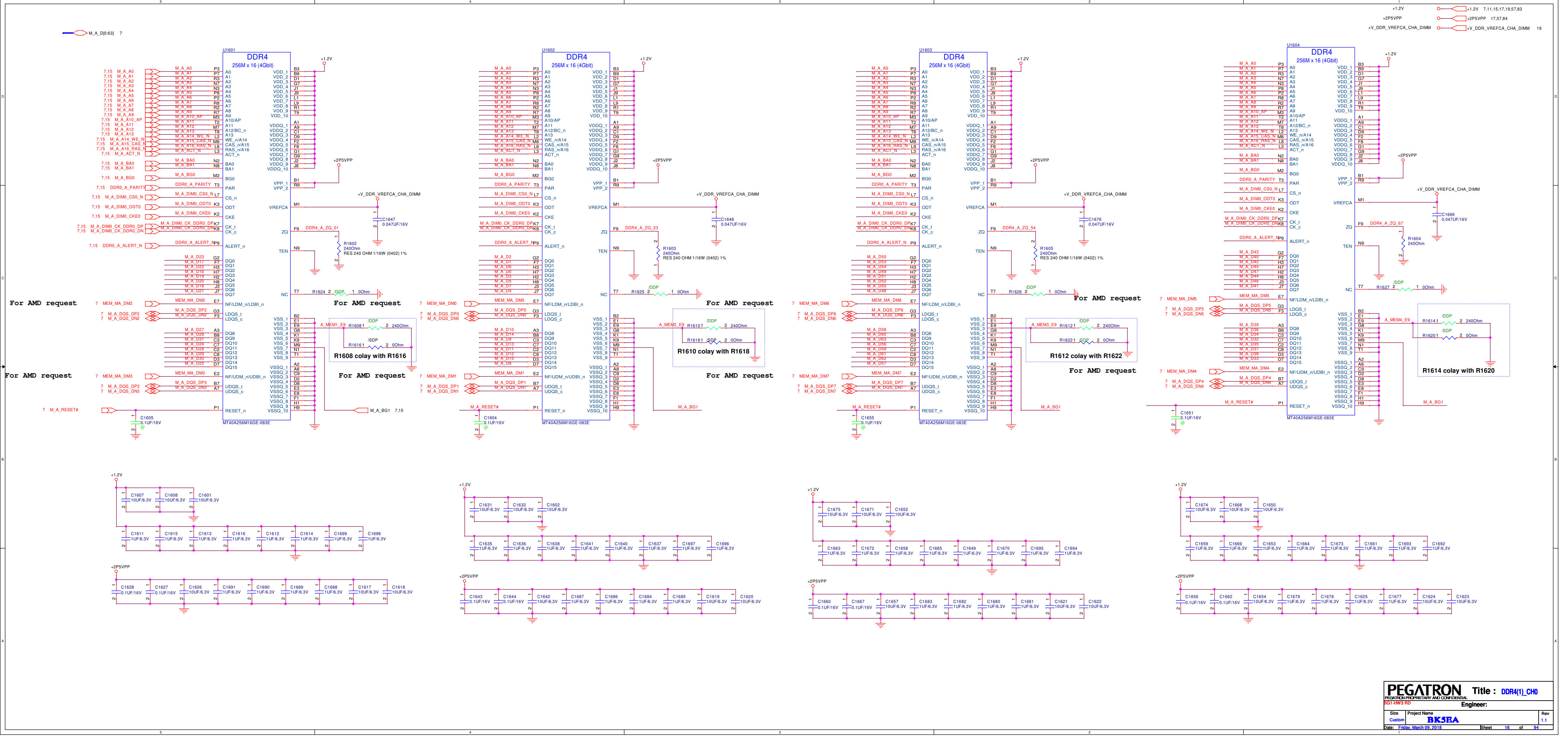
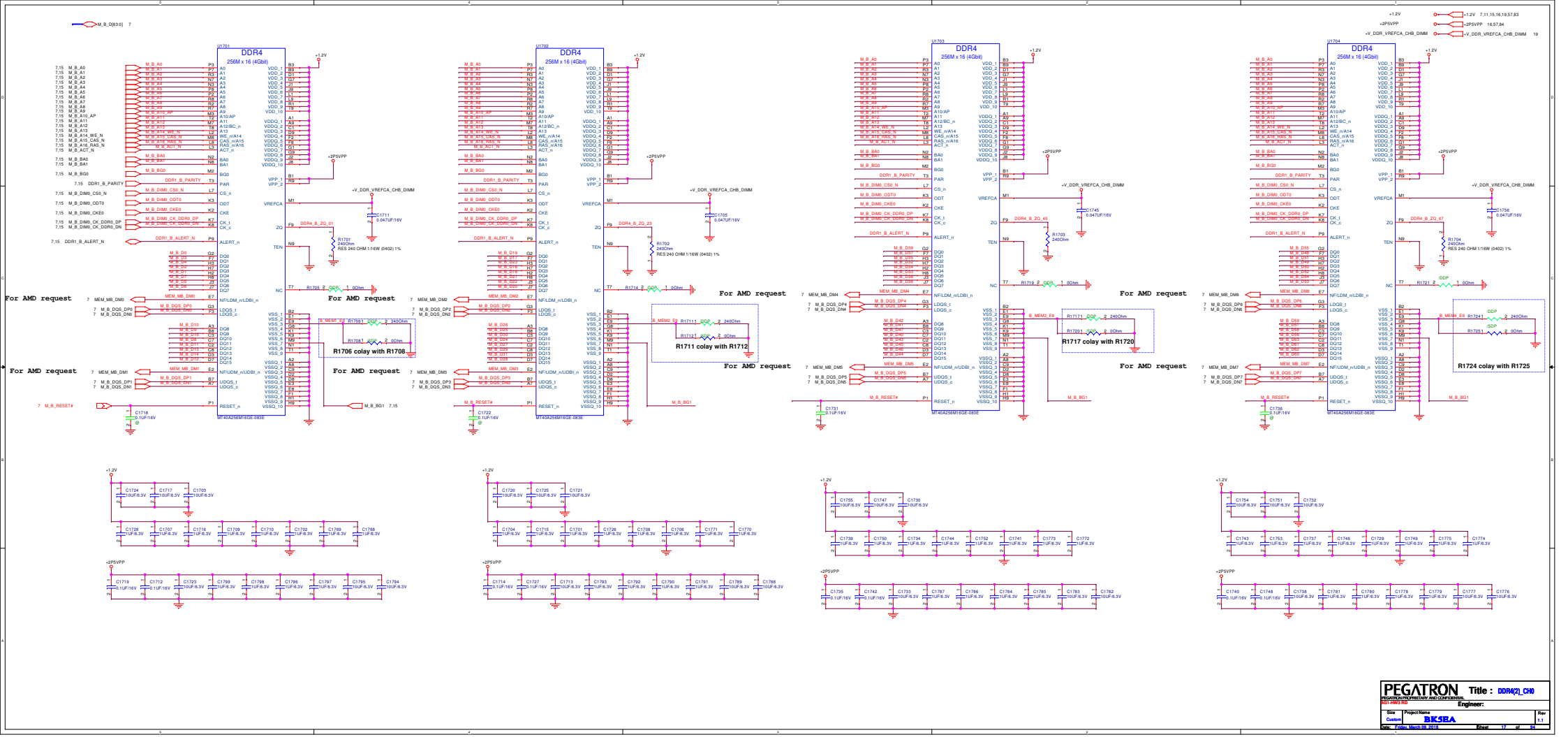
BG1-HW3 RD
Title : THUNDERBOLT_HDMI redriver
Engineer:
Size B | Project Name BK5EA | Rev 1.1
Date: Friday, March 09, 2018 | Sheet 13 of 94


CHA
CHB
+1.2V
+0.6VS
+1.2V 7,11,16,17,19,57,83
+0.6VS 57,83
39Ohm
1%
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10_AP M_A_A11 M_A_A12 M_A_A13 M_A_A14_WE_N M_A_A15_CAS_N M_A_A16_RAS_N
M_A_DIM0_CS0_N
M_A_DIM0_CKE0
M_A_BG1
M_A_BG0
M_A_BA0
M_A_BA1
M_A_DIM0_ODT0
M_A_ACT_N
DDR0_A_PARITY
M_A_DIM0_CK_DDR0_DN
M_A_DIM0_CK_DDR0_DP
DDR0_A_ALERT_N
/DDP
C1522 0.1UF/16V
R1.0 0605A
AMD request
49.9Ohm
C1501 C1502 C1503 C1504 C1505 C1506 C1507 C1508 1UF/6.3V X5R/+/-20%
C1532 C1535 C1538 C1531 C1537 C1536 C1533 C1534 1UF/6.3V X5R/+/-20%
C1511 C1515 10UF/6.3V X5R/20% vx_c0603_small
C1539 C1540 10UF/6.3V X5R/20% vx_c0603_small
1AT200000068
M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10_AP M_B_A11 M_B_A12 M_B_A13 M_B_A14_WE_N M_B_A15_CAS_N M_B_A16_RAS_N
M_B_DIM0_CS0_N
M_B_DIM0_CKE0
M_B_BG1
M_B_BG0
M_B_BA0
M_B_BA1
M_B_DIM0_ODT0
M_B_ACT_N
DDR1_B_PARITY
M_B_DIM0_CK_DDR0_DN
M_B_DIM0_CK_DDR0_DP
DDR1_B_ALERT_N
C1523 0.1UF/16V
R1.0 0605A
AMD request
49.9Ohm
C1520 C1518 C1519 C1517 C1516 C1514 C1513 C1512 1UF/6.3V X5R/+/-20%
C1543 C1541 C1547 C1548 C1545 C1544 C1546 C1542 1UF/6.3V X5R/+/-20%
C1509 C1510 10UF/6.3V X5R/20% vx_c0603_small
C1549 C1550 10UF/6.3V X5R/20% vx_c0603_small
1AT200000068
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : DDR4(0)_Termination
3G1-HW3 RD
Engineer:
Size C
Project Name BK5BA
Rev 1.1
Date: Friday, March 09, 2018
Sheet 15 of 94



DDR4
256M x 16 (4Gbit)
U1601
U1602
U1603
U1604
MT40A256M16GE-083E
For AMD request
R1608 colay with R1616
R1610 colay with R1618
R1612 colay with R1622
R1614 colay with R1620
+1.2V
+2P5VPP
+V_DDR_VREFCA_CHA_DIMM
M_A_D[0:63]
M_A_RESET#
M_A_BG1
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : DDR4(1)_CH0
RG1-HW3 RD
Engineer:
Size
Custom
Project Name
BK5RA
Rev
1.1
Date: Friday, March 09, 2018
Sheet 16 of 94


DDR4
256M x 16 (4Gbit)
U1701
U1702
U1703
U1704
+1.2V
+2P5VPP
+V_DDR_VREFCA_CHB_DIMM
For AMD request
R1706 colay with R1708
R1711 colay with R1712
R1717 colay with R1720
R1724 colay with R1725
MT40A256M16GE-083E

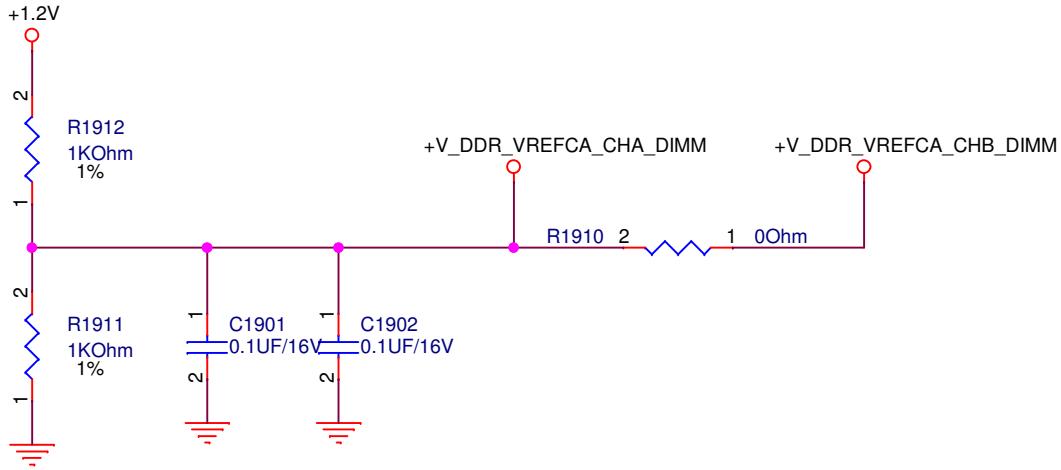
PEGATRON
Title : DDR4[2]_CH0
Engineer:
Size
Custom
Project Name
BK5EA
Rev
1.1
Date: Friday, March 09, 2018
Sheet 17 of 34

Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 18 of 94

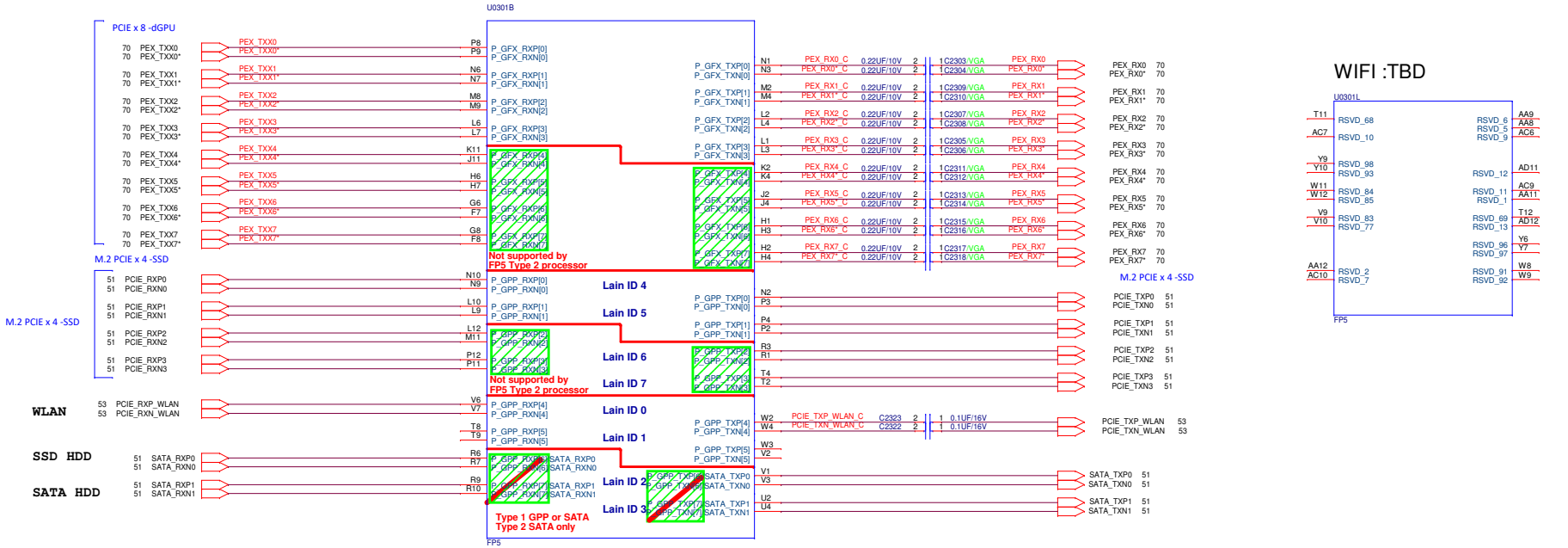
+1.2V — +1.2V — 7,11,15,16,17,57,83

+V_DDR_VREFCA_CHB_DIMM — +V_DDR_VREFCA_CHB_DIMM — 17

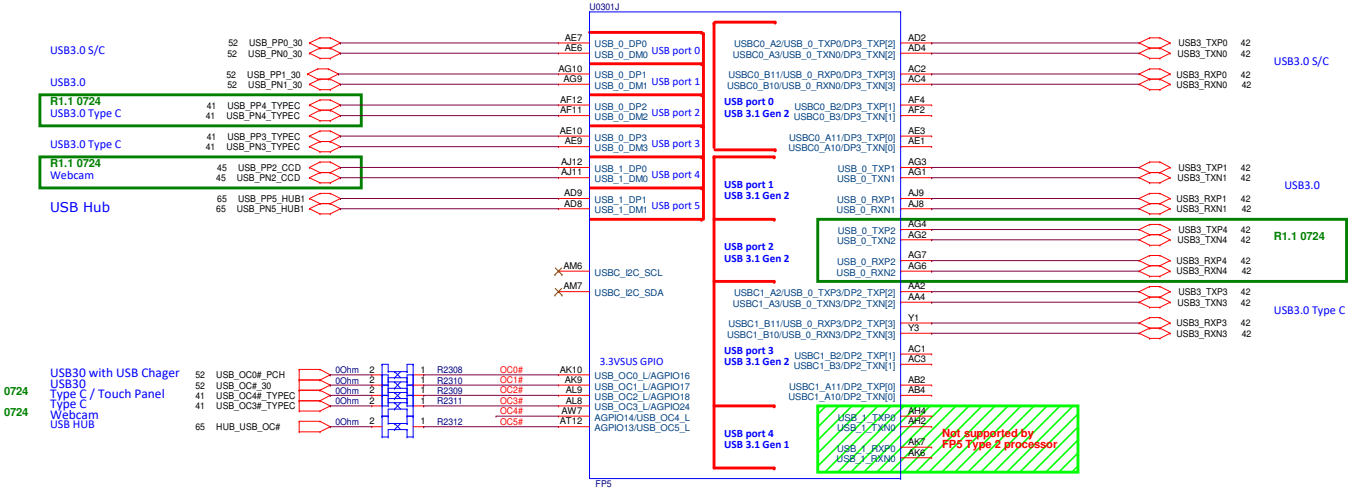
+V_DDR_VREFCA_CHA_DIMM — +V_DDR_VREFCA_CHA_DIMM — 16



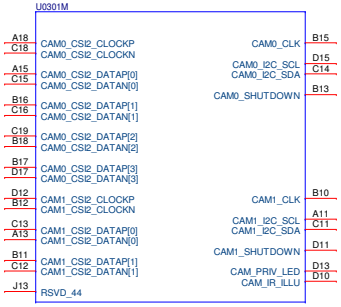
PEGATRON	Title : DDR4(3)_CA/DQ Voltage	
BG1-HW3 RD	Engineer: Jack_Lee	
Size: A	Project Name: BK5EA	Rev: 1.1
Date: Friday, March 09, 2018	Sheet 19 of 94	

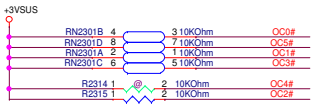


WIFI :TBD

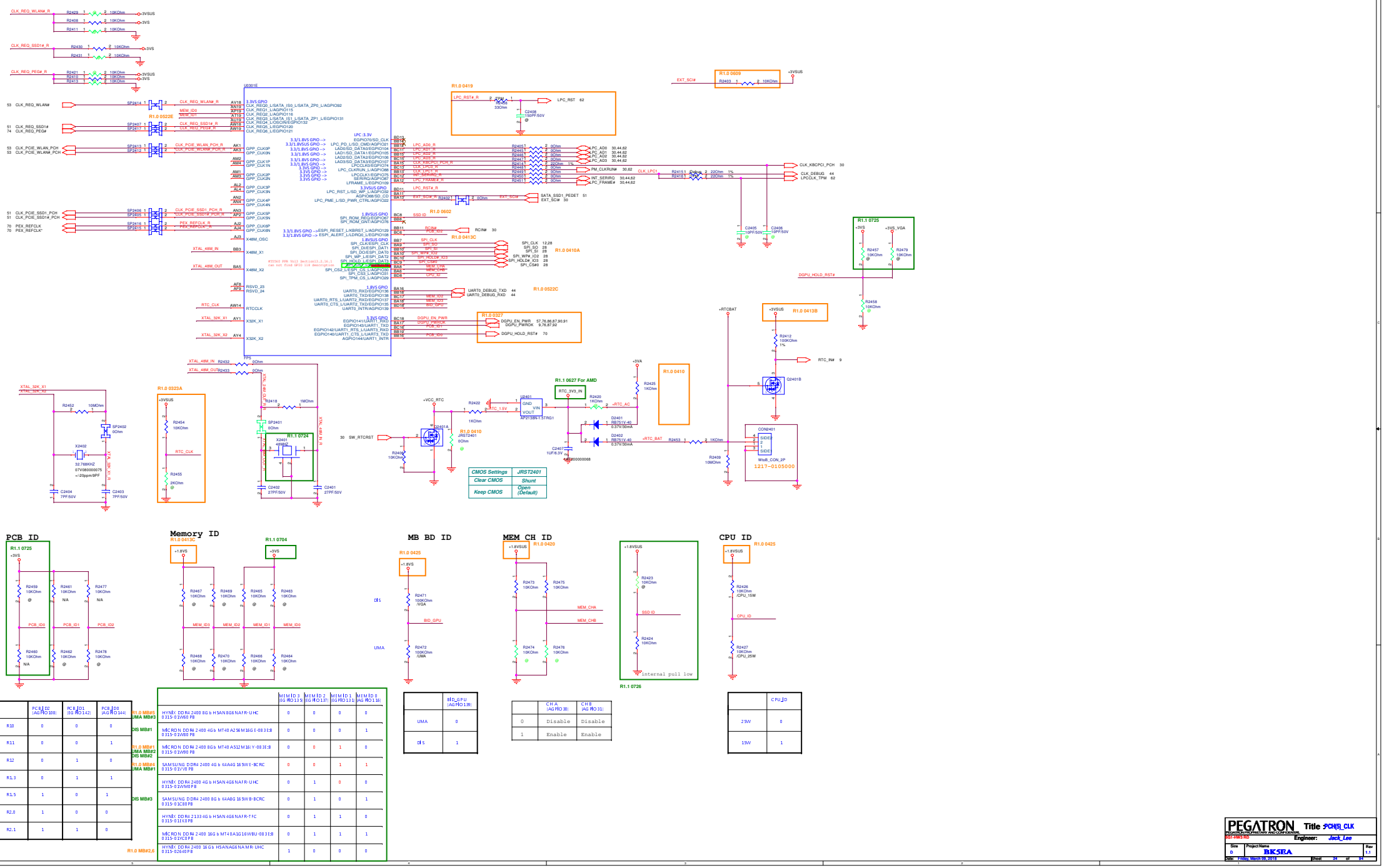


CAMERA





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : PCH(4)_USB/PCIE/SATA
BG1-HW3 RD
Engineer: Jack_Lee
Size: C
Project Name: BK5BA
Rev: 1.1
Date: Friday, March 09, 2018
Sheet 23 of 94



	PCB_ID2 (AGPIO108)	PCB_ID1 (EGPIO142)	PCB_ID0 (AGPIO144)
R1.0 MB#5 UMA MB#3			
R1.0 MB#1 DIS MB#1			
R1.0 MB#1 UMA MB#2 DIS MB#2			
R1.0 MB#4 UMA MB#1			
R1.3	0	1	1
R1.5	1	0	1
DIS MB#3			
R2.0	1	0	0
R2.1	1	1	0

	MEM_ID 3 (EGPIO139)	MEM_ID 2 (EGPIO137)	MEM_ID 1 (EGPIO131)	MEM_ID 0 (AGPIO116)
HYNIX DDR4 2400 8G b H5AN8G6NAFR-UHC 0315-01UV00 PB	0	0	0	0
MICRON DDR4 2400 4Gb MT40A256M16GE-083E:B 0315-01UV00 PB	0	0	0	1
MICRON DDR4 2400 8Gb MT40A512M16JY-083E:B 0315-01UV00 PB	0	0	1	0
SAMSUNG DDR4 2400 4G b K4A4G165WE-BCRC 0315-01UV0 PB	0	0	1	1
HYNIX DDR4 2400 4G b H5AN4G6NAFR-UHC 0315-01VM0 PB	0	1	0	0
SAMSUNG DDR4 2400 8G b K4A8G165WB-BCRC 0315-01UC0 PB	0	1	0	1
HYNIX DDR4 2133 4G b H5AN4G6NAFR-TFC 0315-01UC0 PB	0	1	1	0
MICRON DDR4 2400 16G b MT40A1G16WBU-083E:B 0315-01UC0 PB	0	1	1	1
R1.0 MB#2,6 HYNIX DDR4 2400 16Gb H5ANAG6NAMR-UHC 0315-02640 PB	1	0	0	0

	BID_GPU (AGPIO139)
UMA	0
dIS	1

	CHA (AGPIO130)	CHB (AGPIO131)
0	Disable	Disable
1	Enable	Enable

	CPU_ID
25W	0
15W	1

PEGATRON
Title: PCH(5)_CLK
Engineer: Jack_Lee
Size: D
Project Name: BKSEA
Rev: 1.1
Date: Friday, March 09, 2018
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Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 27 of 94

+1.8V_SPI +1.8V_SPI 30,44

R1.0 0411B Change ROM to 1.8VSUS

55mA

+1.8VSUS R2802 1 2 0Ohm +1.8V_SPI

+1.8VS R2830 1 2 0Ohm

+1.8V_SPI

C2801 0.1UF/16V

R1.0 0410A R2813 1KOhm

R2820 1 2 1KOhm

+1.8V_SPI

R2811 1KOhm

R1.0 0410A R2812 3.3KOhm

R1.0 0323A Change ROM to 1.8V

24 SPI_WP#_IO2 R2805 1 2 33Ohm

24 SPI_SO R2806 1 2 33Ohm

24 SPI_CS#0 R2807 1 2 33Ohm

30,44 F_CS#_EC R2808 1 2 33Ohm

30,44 F_SDIO_EC R2809 1 2 33Ohm

SPI1_CS#0 SPI1_SO SPI1_WP#

U2801

1	CS#	VCC	8
2	SO/SIO1	RESET#/SIO3	7
3	WP#/SIO2	SCLK	6
4	GND	SI/SIO0	5

MX25U6435FM2I-10G

05V000000039

SPI1_HOLD# SPI1_CLK SPI1_SI

R2814 1 2 33Ohm SPI_HOLD#_IO3 24

R2815 1 2 33Ohm SPI_CLK 12,24

R2816 1 2 33Ohm SPI_SI 24

R2818 1 2 33Ohm F_SCK_EC 30,44

R2819 1 2 33Ohm F_SDI_EC 30,44

R2821 1 2 3KOhm +1.8V_SPI R1.0 0327

PCH SMBus

+12VSUS

R1.1 0725

13,30,50,74 SMB1_CLK

13,30,50,74 SMB1_DAT

Q2802A UM6K1NG1DTN Rdson=13Ohm/Vgs(th)=1.5V

Q2802B UM6K1NG1DTN

SML1_CLK 8

SML1_DAT 8

EC

GPU

PCH

PEGATRON Title : PCH(9)_SPI_SMB

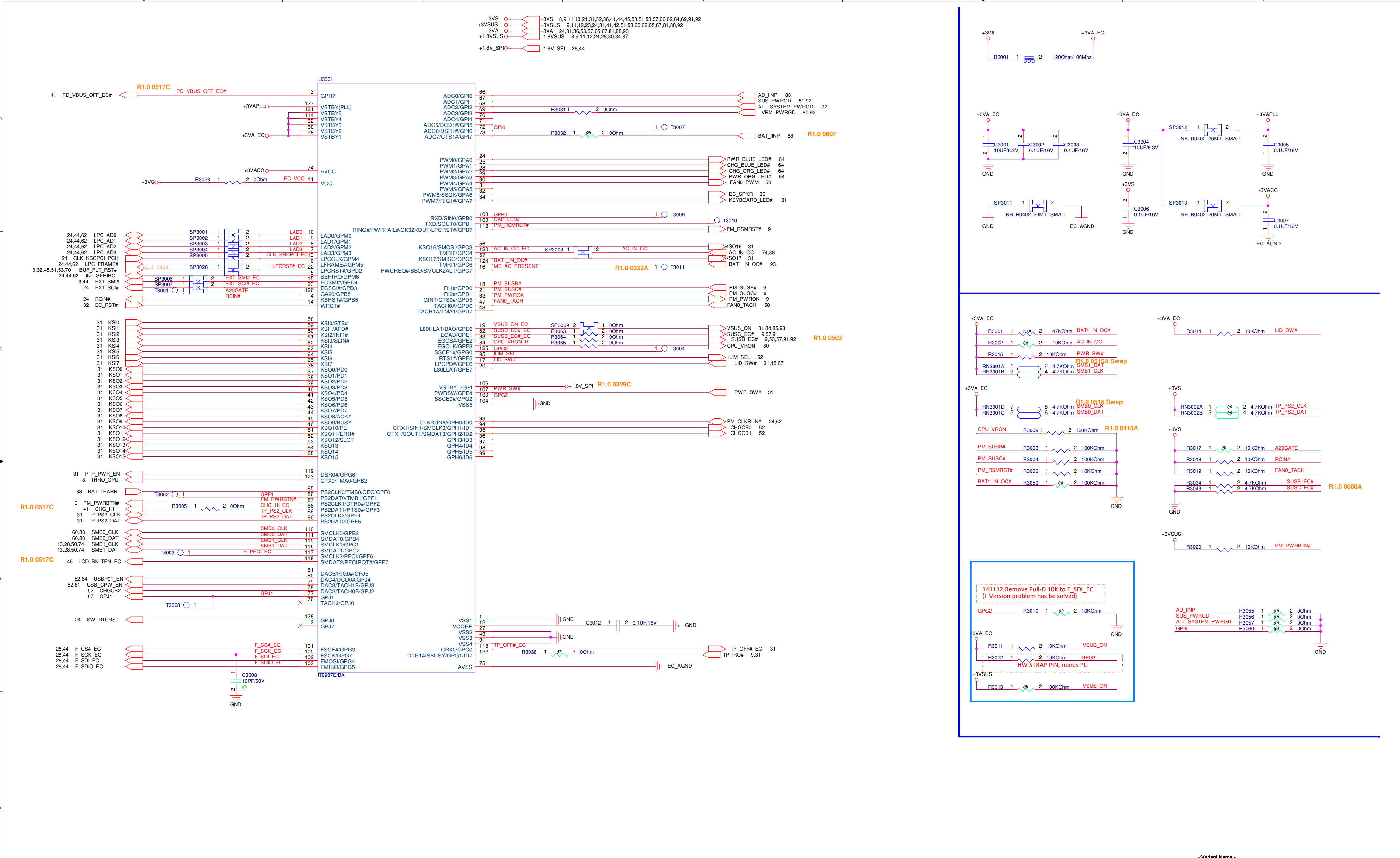
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD Engineer: Jack_Lee

Size Custom | Project Name BK5EA | Rev 1.1

Date: Friday, March 09, 2018 | Sheet 28 of 94

Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 29 of 94



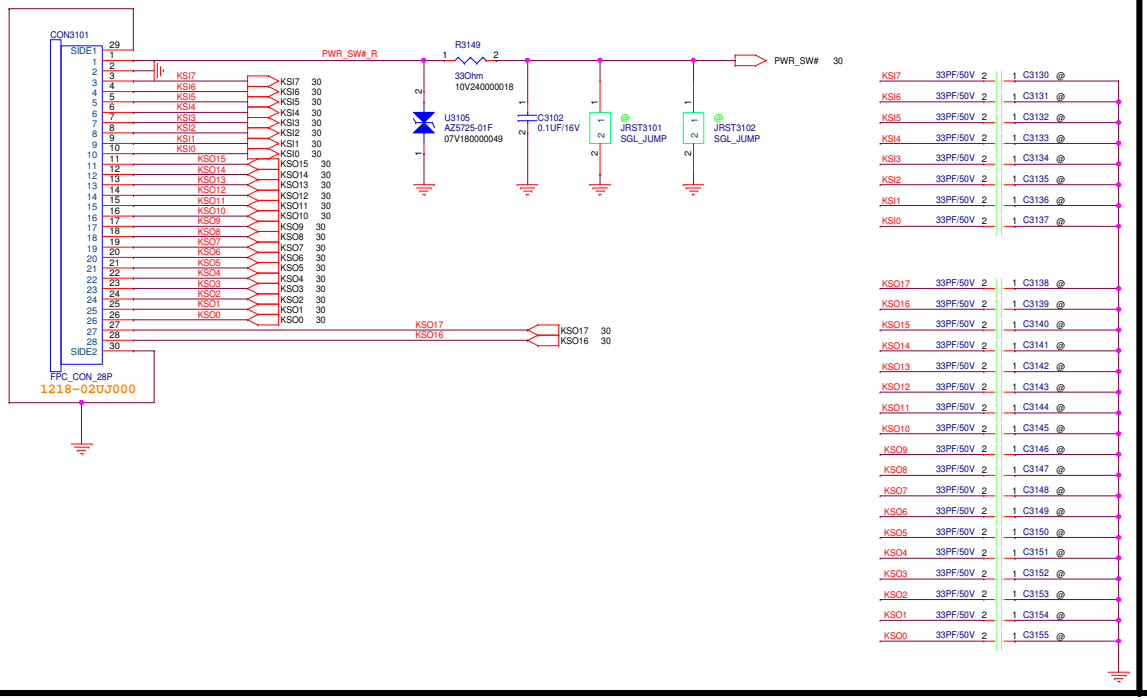
U3001
IT8587E/BX
R1.0 0517C
PD_VBUS_OFF_EC#
GPH7
VSTBY(PLL)
VSTBY5
VSTBY4
VSTBY3
VSTBY2
VSTBY1
AVCC
VCC
+3VAPLL
+3VA_EC
+3VACC
+3VS
EC_VCC
ADC0/GPI0
ADC1/GPI1
ADC2/GPI2
ADC3/GPI3
ADC4/GPI4
ADC5/DCD1#/GPI5
ADC6/DSR1#/GPI6
ADC7/CTS1#/GPI7
AD_IINP
SUS_PWRGD
ALL_SYSTEM_PWRGD
VRM_PWRGD
BAT_IINP
R1.0 0607
PWM0/GPA0
PWM1/GPA1
PWM2/GPA2
PWM3/GPA3
PWM4/GPA4
PWM5/GPA5
PWM6/SSCK/GPA6
PWM7/RIG1#/GPA7
PWR_BLUE_LED#
CHG_BLUE_LED#
CHG_ORG_LED#
PWR_ORG_LED#
FAN0_PWM
EC_SPKR
KEYBOARD_LED#
RXD/SIN0/GPB0
TXD/SOUT0/GPB1
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7
PM_RSMRST#
LAD0/GPM0
LAD1/GPM1
LAD2/GPM2
LAD3/GPM3
LPCCLK/GPM4
LFRAME#/GPM5
LPCRST#/GPD2
SERIRQ/GPM6
ECSMI#/GPD4
ECSCI#/GPD3
GA20/GPB5
KBRST#/GPB6
WRST#
KSO16/SMOSI/GPC3
TMRI0/GPC4
KSO17/SMISO/GPC5
TMRI1/GPC6
PWUREQ#/BBO/SMCLK2ALT/GPC7
AC_IN_OC
BAT1_IN_OC#
ME_AC_PRESENT
R1.0 0322A
RI1#/GPD0
RI2#/GPD1
GINT/CTS0#/GPD5
TACH0A/GPD6
TACH1A/TMA1/GPD7
PM_SUSB#
PM_SUSC#
PM_PWROK
FAN0_TACH
L80HLAT/BAO/GPE0
EGAD/GPE1
EGCS#/GPE2
EGCLK/GPE3
SSCE1#/GPG0
RTS1#/GPE5
LPCPD#/GPE6
L80LLAT/GPE7
VSUS_ON
SUSC_EC#
SUSB_EC#
CPU_VRON
ILIM_SEL
LID_SW#
R1.0 0503
VSTBY_FSPI
PWRSW/GPE4
SSCE0#/GPG2
VSS5
PWR_SW#
R1.0 0329C
+1.8V_SPI
CLKRUN#/GPH0/ID0
CRX1/SIN1/SMCLK3/GPH1/ID1
CTX1/SOUT1/SMDAT3/GPH2/ID2
GPH3/ID3
GPH4/ID4
GPH5/ID5
GPH6/ID6
PM_CLKRUN#
CHGCB0
CHGCB1
KSI0/STB#
KSO0/PD0
KSO15
DSR0#/GPG6
CTX0/TMA0/GPB2
PTP_PWR_EN
THRO_CPU
BAT_LEARN
PS2CLK0/TMB0/CEC/GPF0
PS2DAT0/TMB1/GPF1
PS2CLK1/DTR0#/GPF2
PS2DAT1/RTS0#/GPF3
PS2CLK2/GPF4
PS2DAT2/GPF5
PM_PWRBTN#
CHG_HI
TP_PS2_CLK
TP_PS2_DAT
SMCLK0/GPB3
SMDAT0/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
SMCLK2/PECI/GPF6
SMDAT2/PECIRQT#/GPF7
SMB0_CLK
SMB0_DAT
SMB1_CLK
SMB1_DAT
H_PECI_EC
LCD_BKLTEN_EC
DAC5/RIG0#/GPJ5
DAC4/DCD0#/GPJ4
DAC3/TACH1B/GPJ3
DAC2/TACH0B/GPJ2
GPJ1
TACH2/GPJ0
USBP01_EN
USB_CPW_EN
CHGCB2
SW_RTCRST
GPJ6
GPJ7
FSCE#/GPG3
FSCK/GPG7
FMOSI/GPG4
FMISO/GPG5
F_CS#_EC
F_SCK_EC
F_SDI_EC
F_SDIO_EC
VSS1
VCORE
VSS2
VSS3
VSS4
CRX0/GPC0
DTR1#/SBUSY/GPG1/ID7
AVSS
TP_OFF#_EC
TP_IRQ#
EC_AGND
GND
C3008 10PF/50V
C3012 0.1UF/16V
B3001 120Ohm/100Mhz
C3001 10UF/6.3V
C3002 0.1UF/16V
C3003 0.1UF/16V
C3004 10UF/6.3V
C3005 0.1UF/16V
C3006 0.1UF/16V
C3007 0.1UF/16V
SP3011 NB_R0402_20MIL_SMALL
SP3012 NB_R0402_20MIL_SMALL
SP3013 NB_R0402_20MIL_SMALL
R1.0 0515A Swap
R1.0 0516 Swap
R1.0 0410A
R1.0 0608A
141112 Remove Pull-D 10K to F_SDI_EC
(F Version problem has be solved)
HW STRAP PIN, needs PU
+3VSUS
+1.8VSUS

<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

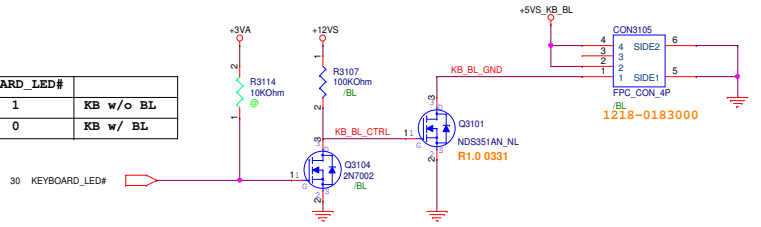
BG1-HW3 RD

Title :	EC_IT8587E/FX
Engineer:	Jack_Lee
Size	Custom
Project Name	BK5EA
Rev	1.1
Date:	Friday, March 09, 2018
Sheet	30 of 94

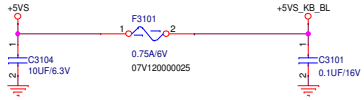


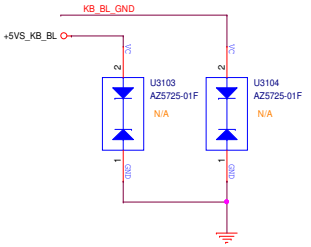
Keyboard Backlight

KEYBOARD_LED#	
1	KB w/o BL
0	KB w/ BL



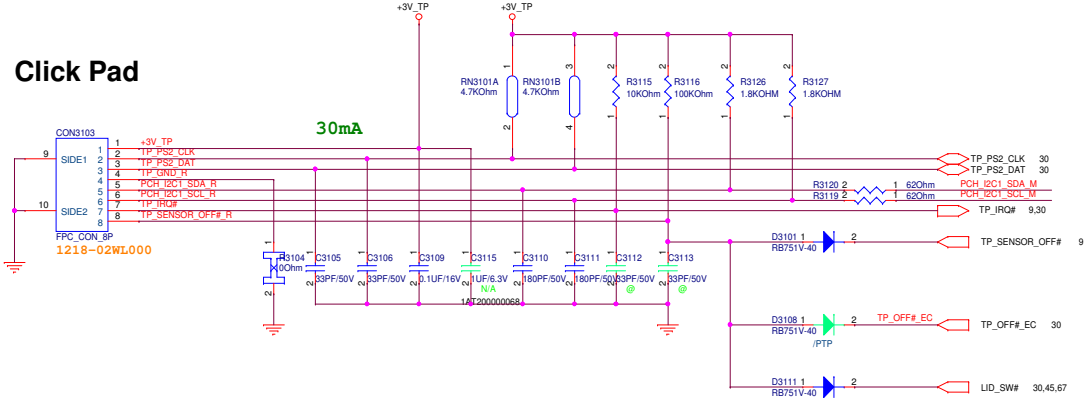
+5VS_KB_BL trace >20mils

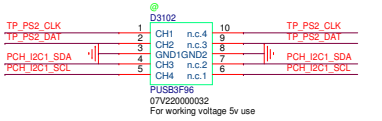


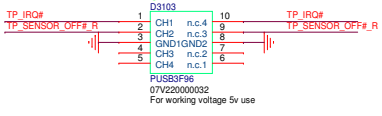


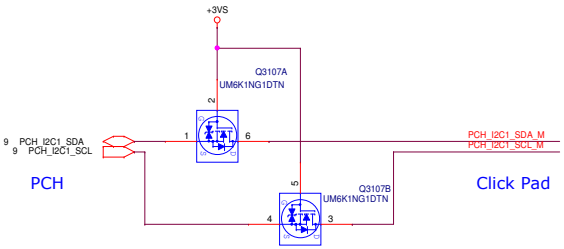
Click Pad

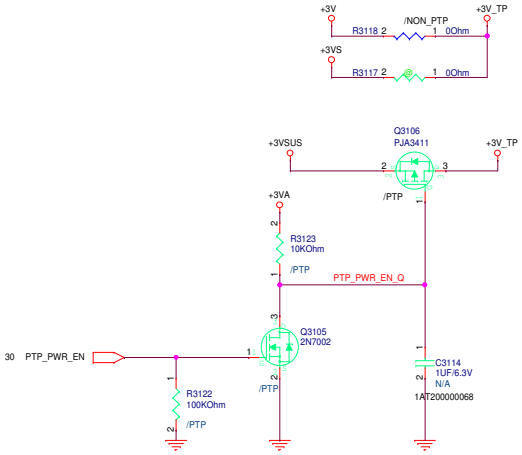
30mA



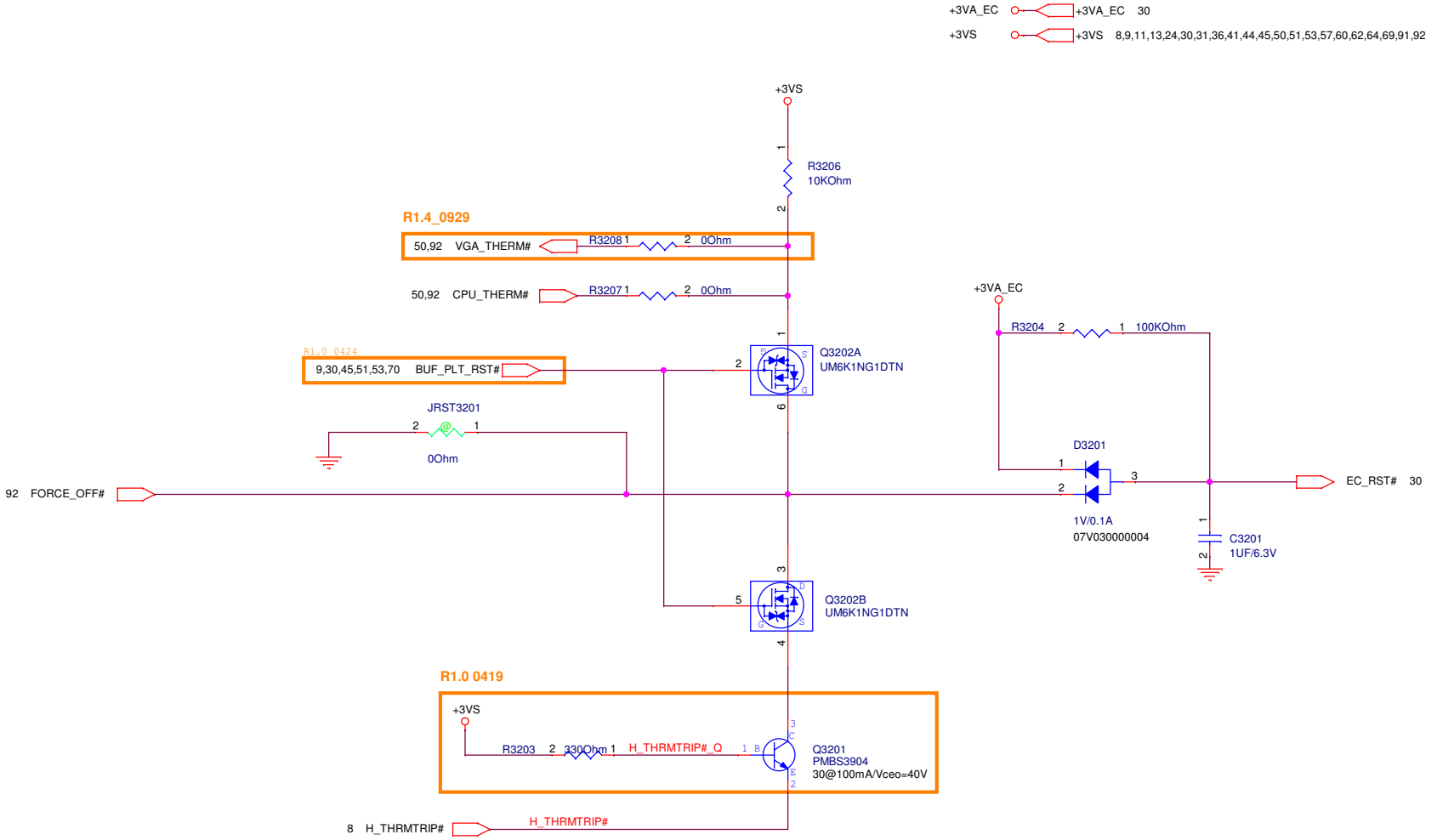








PEGATRON	Title :	KB_TP
BG1-HW3 RD	Engineer:	Jack_Lee
Size: C	Project Name: BK5BA	Rev: 1.1
Date: Friday, March 09, 2018	Sheet 31 of 94	



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD

Title : RST_Reset Circuit

Engineer: Jack_Lee

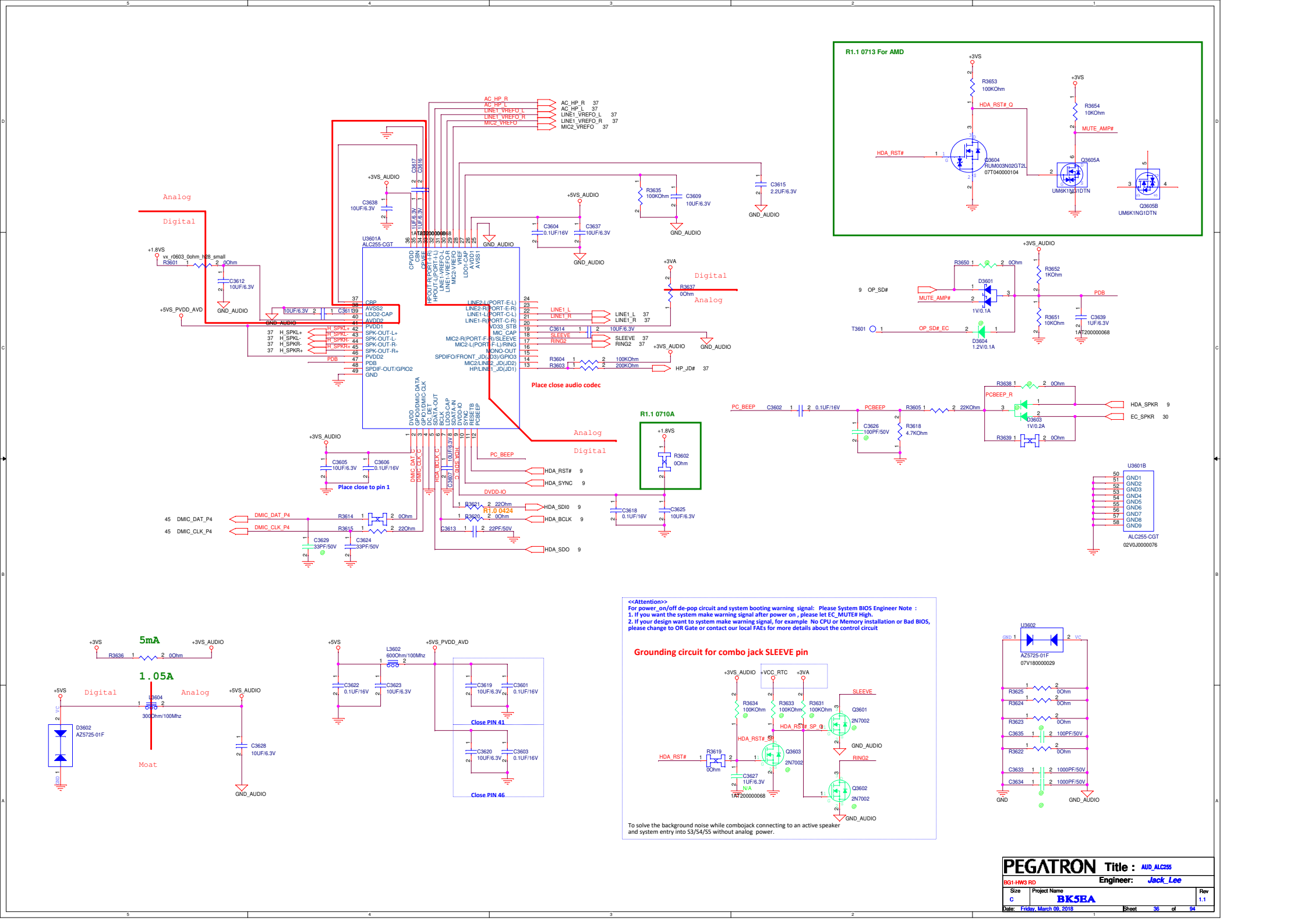
Size	Project Name	Rev
B	BK5EA	1.1

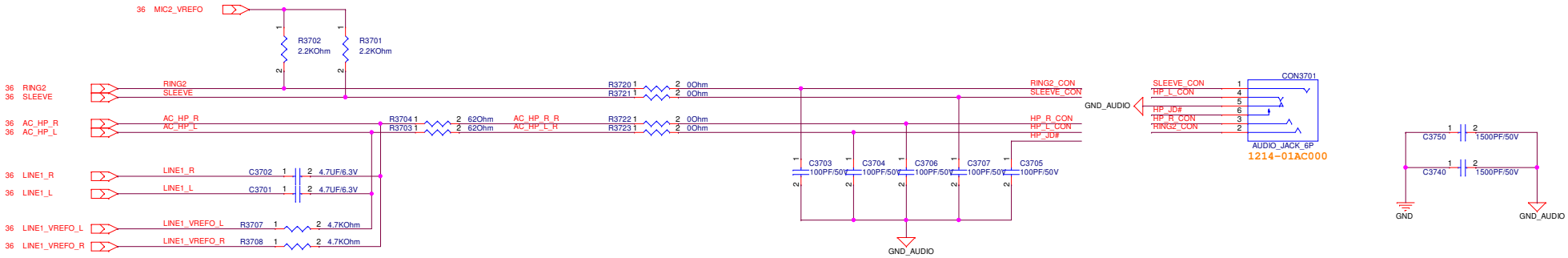
Date: Friday, March 09, 2018 Sheet 32 of 94

Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 33 of 94

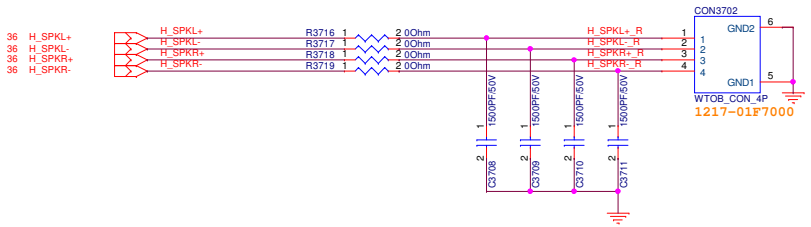
Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 34 of 94

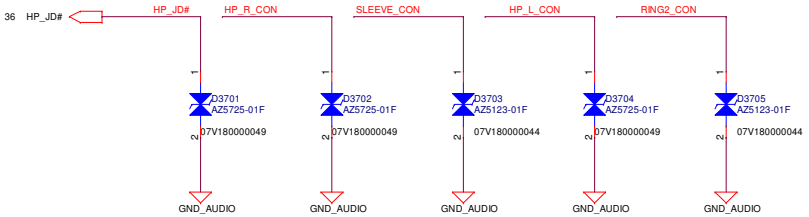
Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 35 of 94


R1.1 0713 For AMD
Analog
Digital
U3601A
ALC255-CGT
Place close audio codec
Place close to pin 1
R1.1 0710A
R1.0 0424
Close PIN 41
Close PIN 46
5mA
1.05A
Moat
<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High.
2. If your design want to system make warning signal, for example No CPU or Memory installation or Bad BIOS, please change to OR Gate or contact our local FAEs for more details about the control circuit
Grounding circuit for combo jack SLEEVE pin
To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.
U3601B
ALC255-CGT
02V0J0000076
PEGATRON
Title : AUD_ALC255
Engineer: Jack_Lee
BG1-HW3 RD
Size C
Project Name BK5BA
Rev 1.1
Date: Friday, March 09, 2018
Sheet 36 of 94



Internal Speaker





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD

Title : AUD_HP/DMIC/SPK
Engineer: Jack_Lee

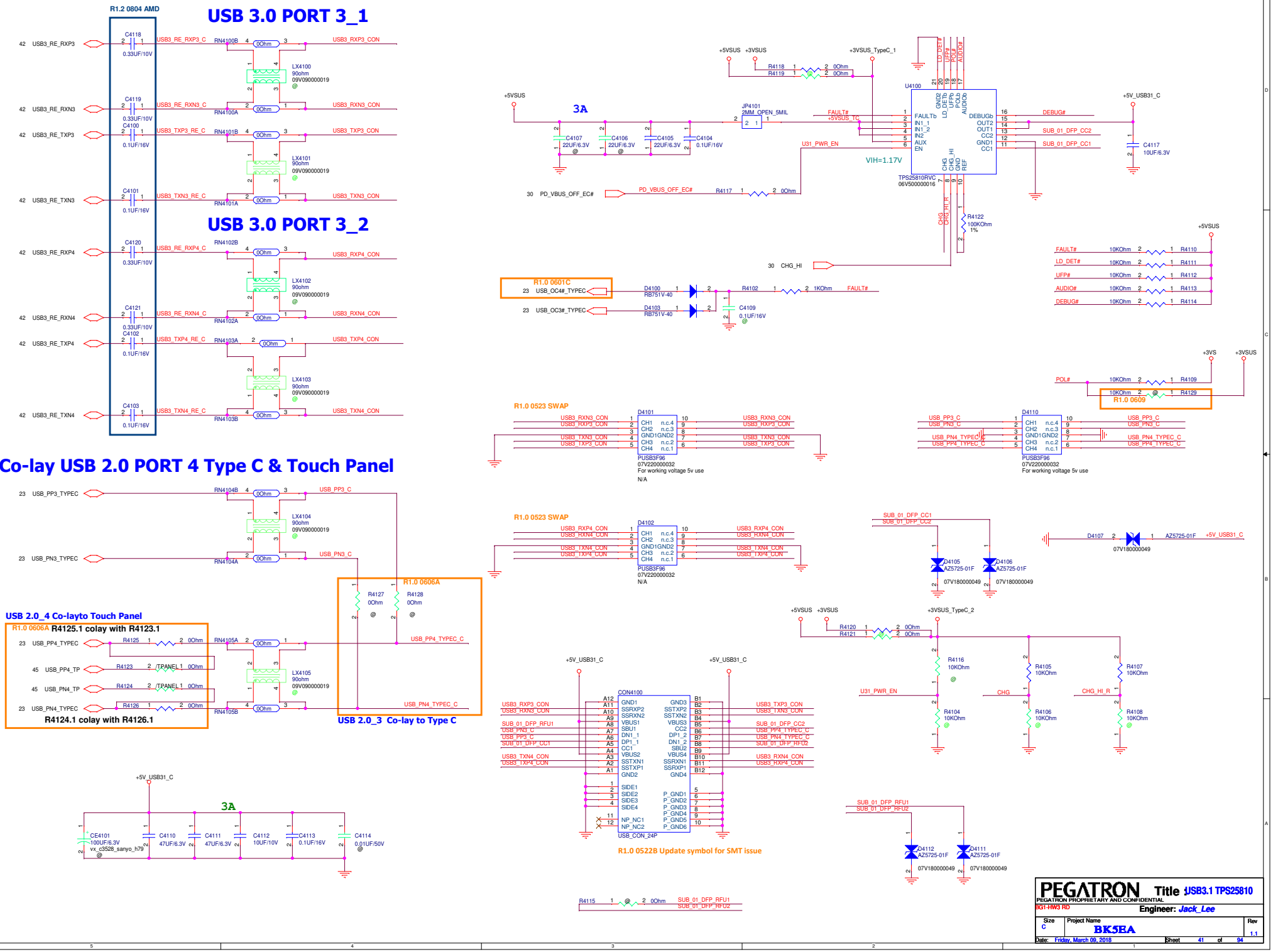
Size	Project Name	Rev
Custom	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 37 of 94

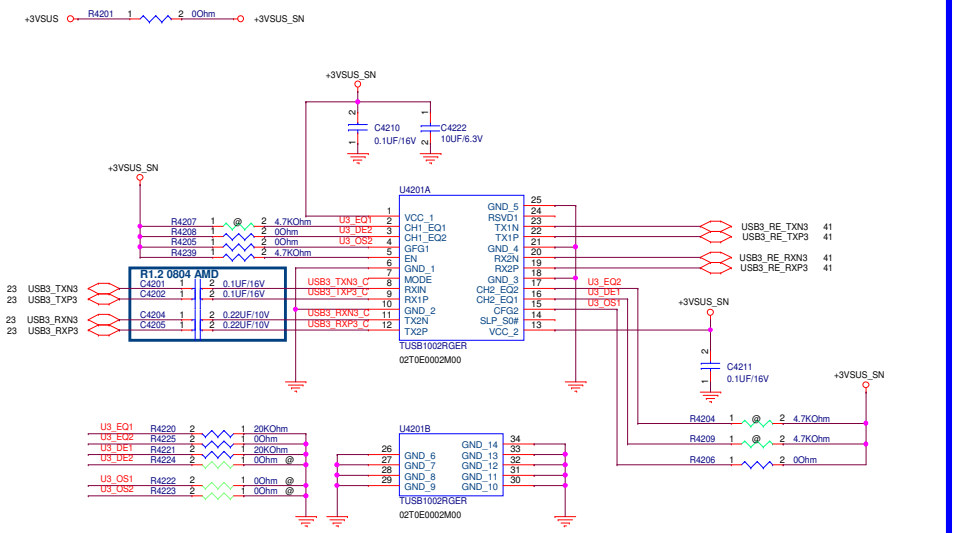
Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 38 of 94

Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 39 of 94

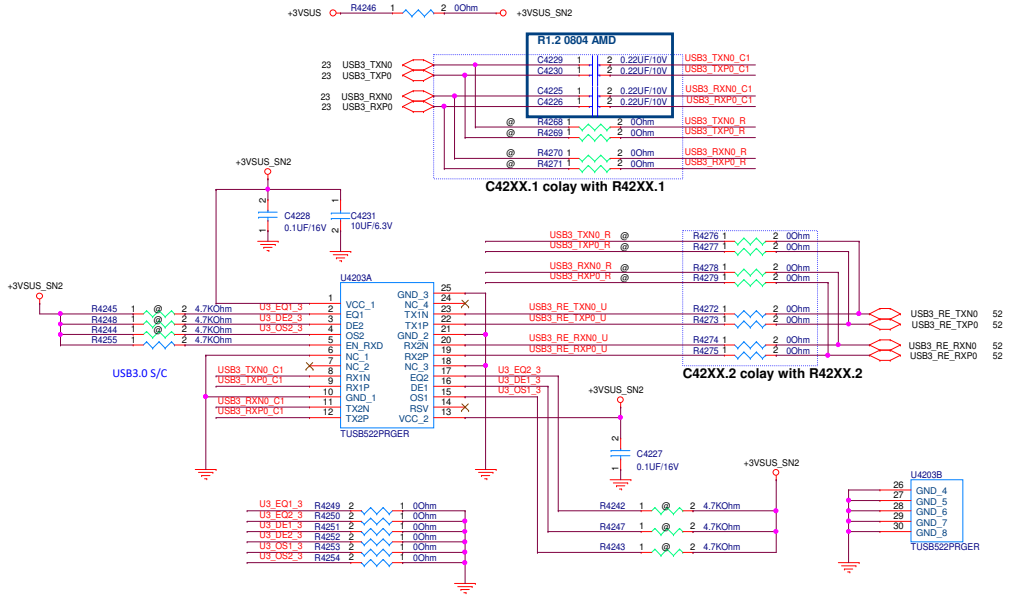
Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 40 of 94


R1.2 0804 AMD
USB 3.0 PORT 3_1
USB 3.0 PORT 3_2
Co-lay USB 2.0 PORT 4 Type C & Touch Panel
USB 2.0_4 Co-layto Touch Panel
R1.0 0606A R4125.1 colay with R4123.1
R4124.1 colay with R4126.1
USB 2.0_3 Co-lay to Type C
R1.0 0606A
R1.0 0523 SWAP
R1.0 0601C
R1.0 0609
R1.0 0522B Update symbol for SMT issue
3A
PEGATRON
Title :USB3.1 TPS25810
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Jack_Lee
Project Name
BK5BA
Rev
1.1
Date: Friday, March 09, 2018
Sheet 41 of 94

Type-C Port 3 (Gen 2)



USB 3.0 PORT 0 S/C (Gen 1)



Type C Port 4 (Gen 2)

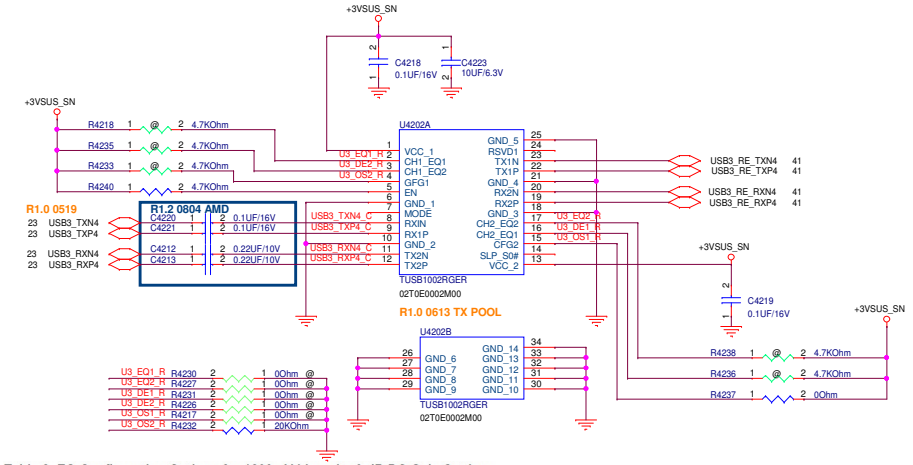


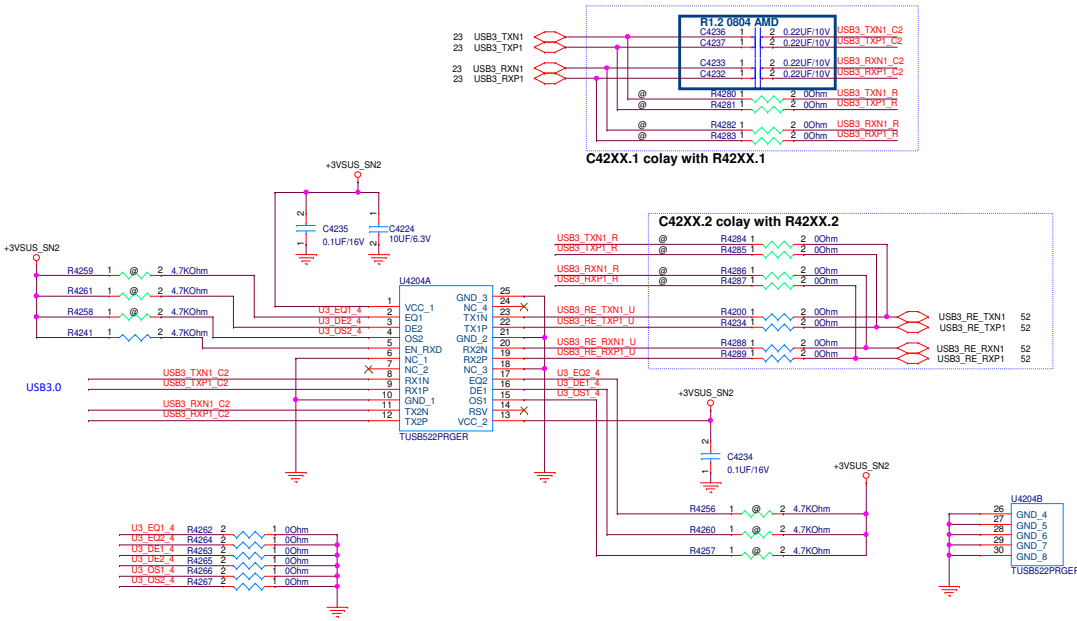
Table 2. EQ Configuration Options for 1200mV Linearity 0 dB DC Gain Setting

EQ SETTING #	CHx_EQ2 PIN LEVEL	CHx_EQ1 PIN LEVEL	EQ GAIN at 2.5GHz / 5 GHz (dB)
1	0	0	1.9 / 5.5
2	0	R	2.8 / 7.1
3	0	F	3.5 / 8.2
4	0	1	4.4 / 9.3
5	R	0	5.0 / 10.2
6	R	R	5.8 / 11.1
7	R	F	6.4 / 11.8
8	R	1	7.1 / 12.6
9	F	0	7.6 / 13.1
10	F	R	8.2 / 13.8
11	F	F	8.7 / 14.3
12	F	1	9.2 / 14.8
13	1	0	9.6 / 15.2
14	1	R	10.1 / 15.6

Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 KΩ 5% to V_{CC}. Option 2: Tie directly to V_{CC}.

USB 3.0 PORT 1 (Gen 1)



PEGATRON Title : USB3 repeater

PEGATRON PROPRIETARY AND CONFIDENTIAL

3G1-HW3 RD

Engineer: Jack_Lee

Size	Project Name	Rev
C	BK5BA	1.1

Date: Friday, March 09, 2018 Sheet 42 of 94

PEGATRON
CONFIDENTIAL-PROPRIETARY AND CONFIDENTIAL

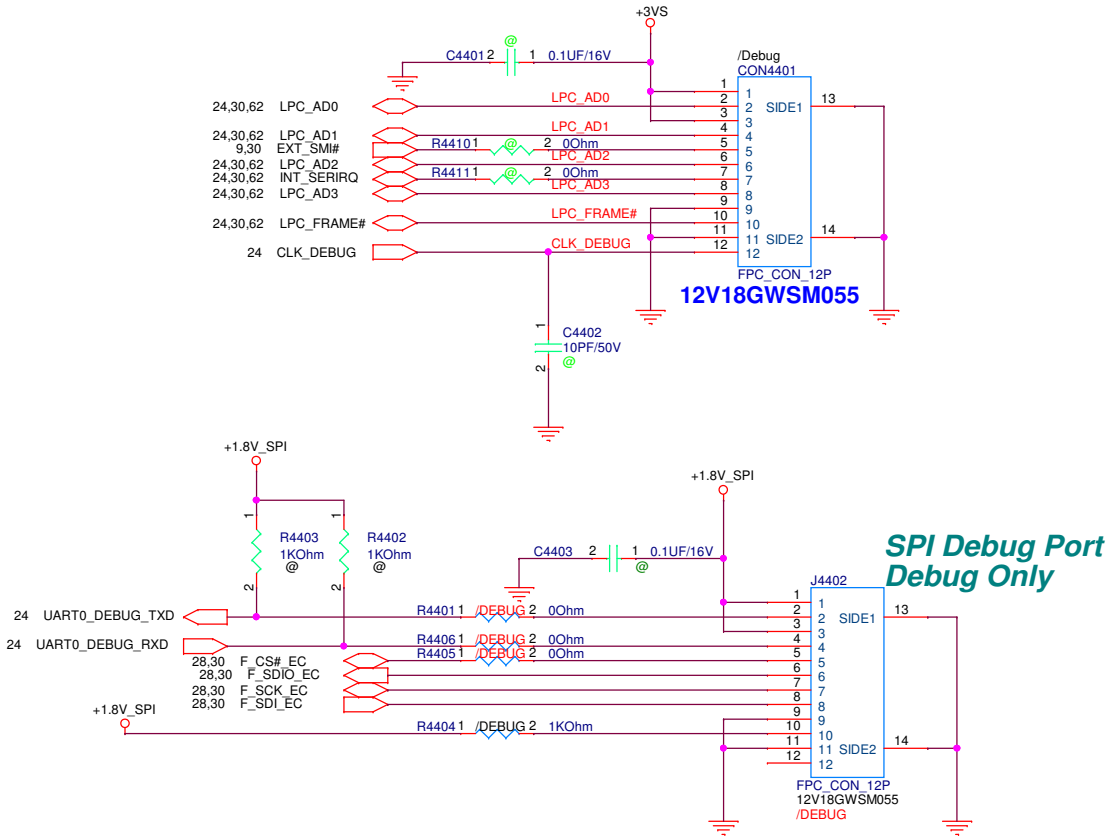
Title : USB3 repeater

DO-HW3 RD

Engineer: Jack_Lee

Size	Project Name	Rev
D	BKSEA	1.1

Date: Friday, March 09, 2018 Sheet 43 of 94



PEGATRON Title : DEBUG CONN.

PEGATRON PROPRIETARY AND CONFIDENTIAL

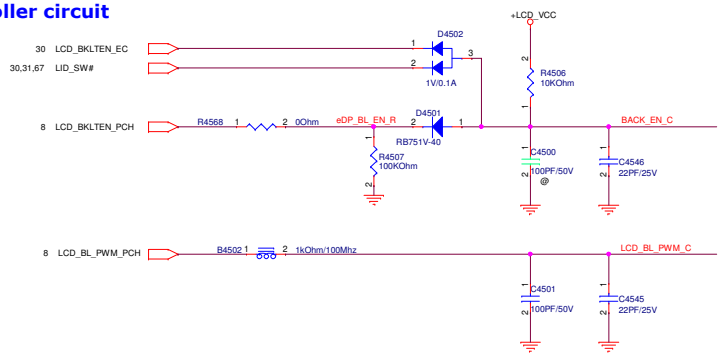
BG1-HW3 RD

Engineer: Jack_Lee

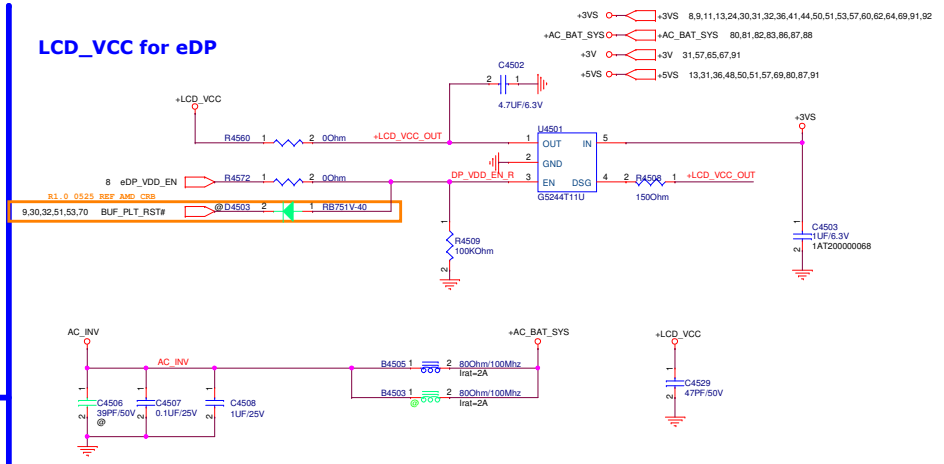
Size	Project Name	Rev
B	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 44 of 94

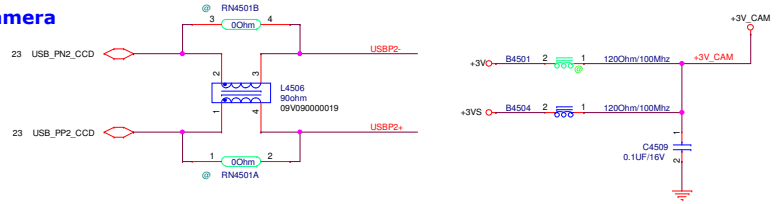
Controller circuit



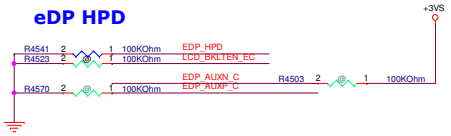
LCD_VCC for eDP



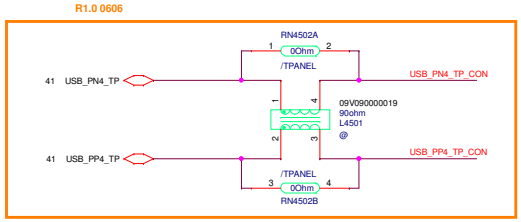
Camera

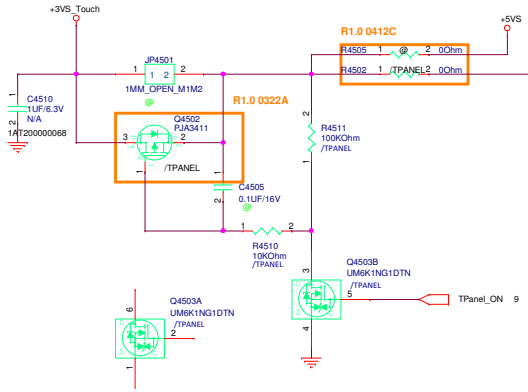


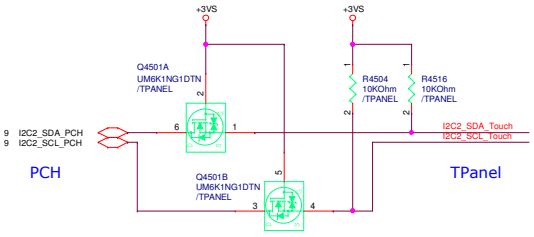
eDP HPD

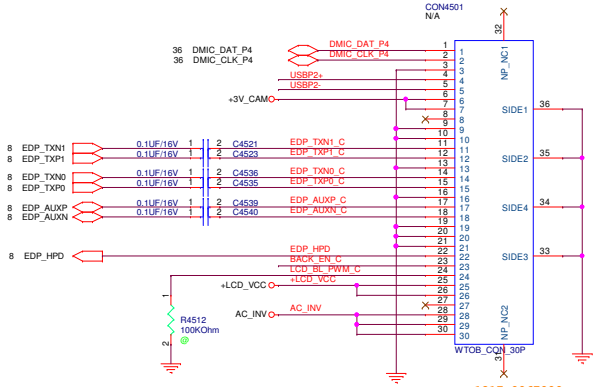


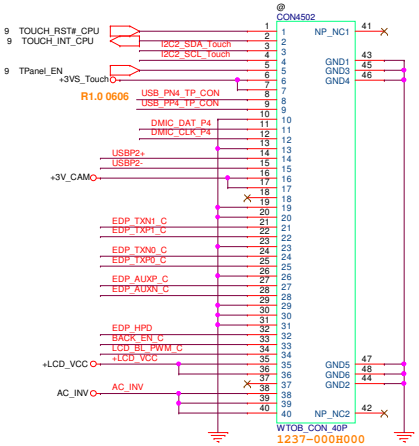
Touch panel











PEGATRON
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Title : LVDS Out

BG1-HW3 RD

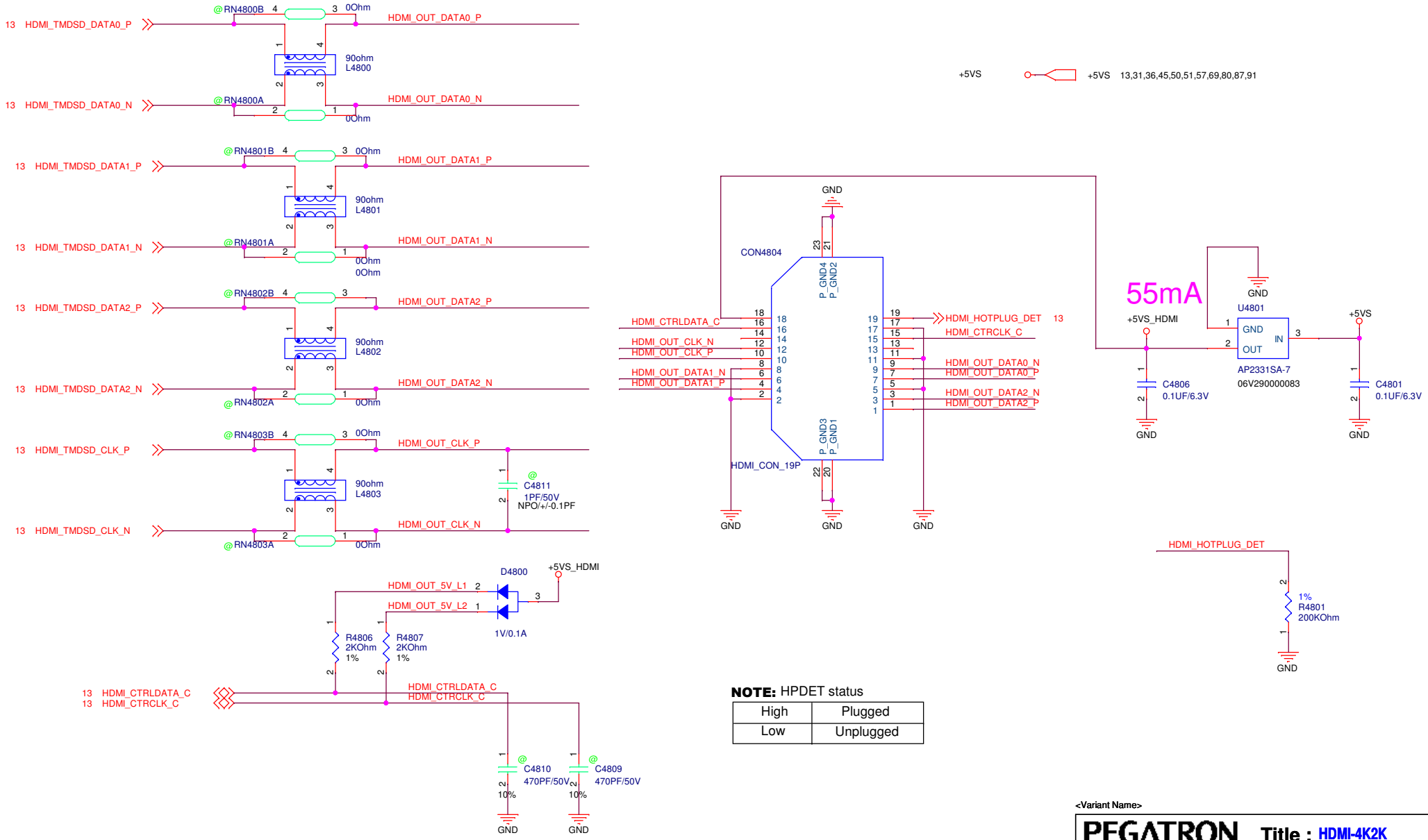
Engineer: Jack_Lee

Size	Project Name	Rev
Custom	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 45 of 94

Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 46 of 94

Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 47 of 94



NOTE: HPDET status

High	Plugged
Low	Unplugged

<Variant Name>

PEGATRON Title : HDMI-4K2K

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD Engineer: Jack_Lee

Size	Project Name	Rev
B	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 48 of 94

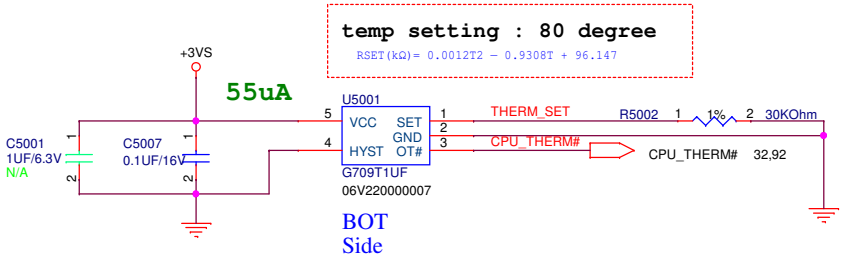
<Variant Name>

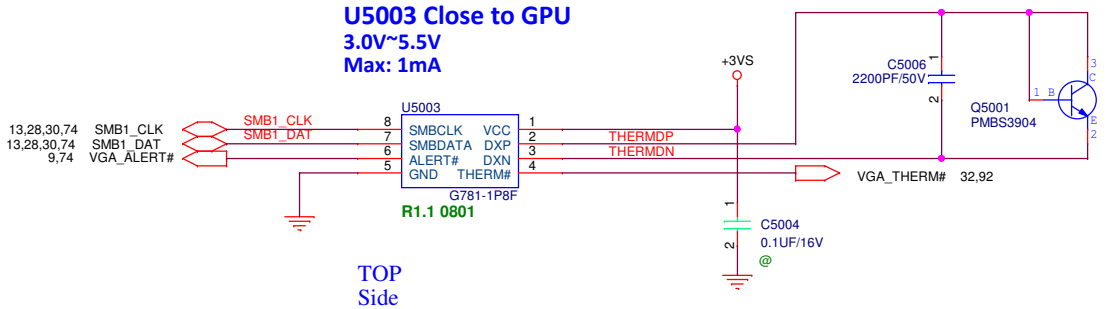
PEGATRON Title : eMMC

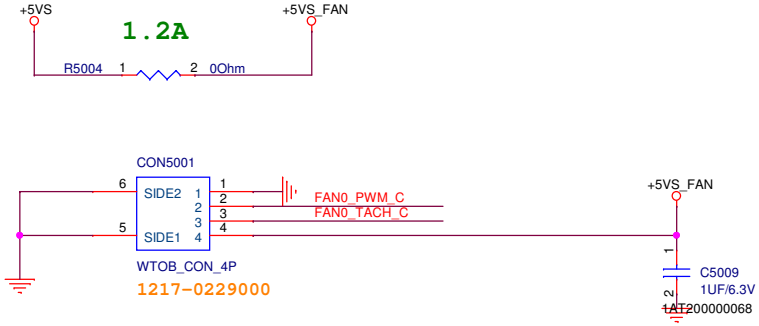
BG1-HW3 RD Engineer: Jack_Lee

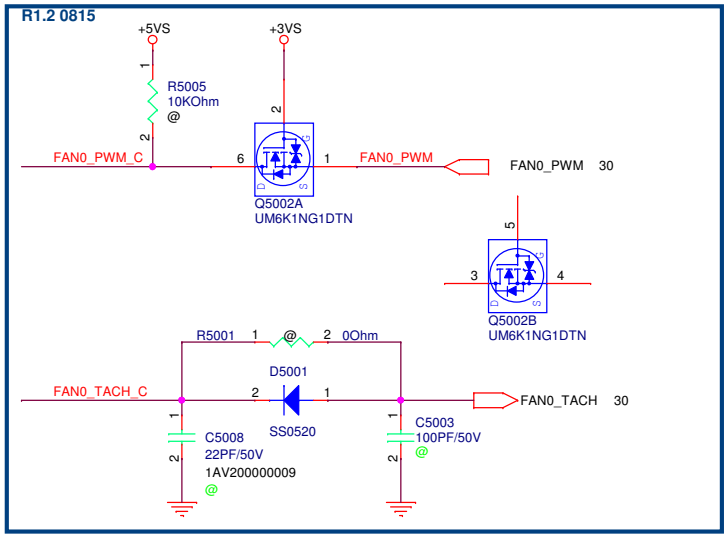
Size	Project Name	Rev
C	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 49 of 94









PEGATRON

Title : Thermal_Fan

BG1-HW3 RD

Engineer: Jack_Lee

Size	Project Name	Rev
B	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 50 of 94

SATA re-driver

R1.1 0718 Remove /NON_SATA_RD

+3VS 8,9,11,13,24,30,31,32,36,41,44,45,50,53,57,60,62,64,69,91,92
+5VS 13,31,36,45,48,50,57,69,80,87,91
+3VSUS 9,11,12,23,24,30,31,41,42,53,60,62,65,67,81,88,92

+3VS +3VS_HDD R5136 2 /HDD 1 0Ohm

+3VS_HDD C5146 0.1UF/16V /HDD C5164 0.1UF/16V /HDD

U5101A SN75LVPE802RTJR /HDD

SATA_TXP1	C5132	SATA_TXP1_C	SATA_HDD_TXP0_CON_C
SATA_TXN1	C5124	SATA_TXN1_C	SATA_HDD_TXN0_CON_C
SATA_RXN1	C5125	SATA_RXN1_C	SATA_HDD_RXN0_CON_C
SATA_RXP1	C5131	SATA_RXP1_C	SATA_HDD_RXP0_CON_C

/HDD C5127 0.01UF/16V SATA_HDD_TXP0_CON
/HDD C5129 0.01UF/16V SATA_HDD_TXN0_CON
/HDD C5133 0.01UF/16V SATA_HDD_RXN0_CON
/HDD C5135 0.01UF/16V SATA_HDD_RXP0_CON

U5101B SN75LVPE802RTJR /HDD

+5VS +5VS_HDD R5180 1 /HDD 2 0Ohm

CON5102 FPC_CON_10P /HDD 1218-02VQ000

SATA_HDD_TXP0_CON SATA_HDD_TXN0_CON SATA_HDD_RXN0_CON SATA_HDD_RXP0_CON

R5179 1 /HDD 2 0Ohm +5VS_HDD

C5103 0.1UF/16V /HDD C5139 10UF/6.3V /HDD C5140 10UF/6.3V /HDD

Equalizer control

EQ1 / EQ2	Channel 1 / Channel 2
NC	0 dB (Default)
H	7 dB
L	15 dB

Internally biased to VCC / 2 with >200-Ωk pullup or ulldown.
When 3-state pins are left as NC, board leakage at the pin pad must be <1 µA; otherwise, drive to VCC / 2 to assert mid-level

De-Emphasis setting

DE1 / DE2	Channel 1 / Channel 2
NC	-4 dB (Default)
H	0 dB
L	-2 dB

De-Emphasis width control

DEW1 or DEW2	Channel 1	Channel 2
H	De-emphasis pulse duration, Long (Default)	
L	De-emphasis pulse duration, Short	

Device enable

EN	Device
H	Device enabled (Default)
L	Device in standby mode

C1_EQ1 R5116 2 1 4.7KOhm +3VS
R5115 1 2 4.7KOhm R1.1 0720 Follow BUSEA setting
C1_EQ2 R5182 2 1 4.7KOhm +3VS
R5113 1 /HDD 2 4.7KOhm

R5117 2 1 4.7KOhm C1_DE1 R5118 2 /HDD 1 4.7KOhm +3VS
R5119 2 1 4.7KOhm C1_DE2 R5120 2 /HDD 1 4.7KOhm

R5121 2 1 4.7KOhm C1_DEW1 R5138 2 /HDD 1 4.7KOhm +3VS
R5123 2 1 4.7KOhm C1_DEW2 R5137 2 /HDD 1 4.7KOhm

C1_EN R5124 2 1 4.7KOhm +3VS

Co-lay Type 1 & 2

PCIE_RXP0	PCIE_SSD	R5144	PCIE_RXP0_R	
PCIE_RXN0	PCIE_SSD	R5145	PCIE_RXN0_R	
SATA_RXP0	SATA_SSD	R5149		
SATA_RXN0	SATA_SSD	R5148		
PCIE_TXN0	PCIE_SSD	R5146	PCIE_TXN0_R	
PCIE_TXP0	PCIE_SSD	R5147	PCIE_TXP0_R	
SATA_TXP0	SATA_SSD	R5150		
SATA_TXN0	SATA_SSD	R5151		

All 0Ohm

SSD

R1.0 0601A

CON5101 NGFF_67P

PCIE_RXN3	PCIE_RXP3			
PCIE_TXN3	PCIE_TXP3	/SSD C5165	/SSD C5166	PCIE_TXN3_C PCIE_TXP3_C
PCIE_RXN2	PCIE_RXP2			
PCIE_TXN2	PCIE_TXP2	/SSD C5167	/SSD C5168	PCIE_TXN2_C PCIE_TXP2_C
PCIE_RXN1	PCIE_RXP1			
PCIE_TXN1	PCIE_TXP1	/SSD C5169	/SSD C5170	PCIE_TXN1_C PCIE_TXP1_C
PCIE_RXN0_R	PCIE_RXP0_R			
PCIE_TXN0_R	PCIE_TXP0_R	/SSD C5171	/SSD C5172	PCIE_TXN0_C PCIE_TXP0_C

All 0.22UF/10V

CLK_PCIE_SSD1#_PCH
CLK_PCIE_SSD1_PCH

+3VS_SSD1 C5156 0.1UF/16V /SSD C5155 0.1UF/16V /SSD C5154 22UF/6.3V /SSD
R5103 1 /SSD 2 0Ohm +3VS
R5181 1 /SSD 2 0Ohm

SATA_DEVSLP1_R R5102 1 /SSD 2 0Ohm SATA_DEVSLP1 9

R1.0 0525

SSD1_PERST# /SSD R5122 1 2 0Ohm BUF_PLT_RST# 9,30,32,45,53,70
CLK_REQ_SSD1# 24

T5102 1 M.2_SSD1_PEDET T5101

+3VS_SSD1 C5159 0.1UF/16V /SSD C5158 0.1UF/16V /SSD C5157 22UF/6.3V /SSD

1244-00EW000

RF requirement

+3VS_SSD1 C5152 10PF/50V @

R1.0 0523D

+3VS_SSD1 R5105 10KOhm /SSD
+3VS C5108 0.1UF/6.3V @
+3VSUS R5104 10KOhm @
M.2_SSD1_PEDET U5102 SN74AUP1G04DCKR @
SATA_SSD1_PEDET 24
R5106 1 2 0Ohm R1.1 0725

PEGATRON
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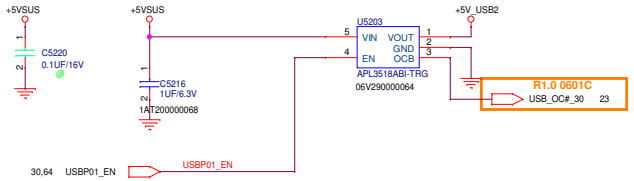
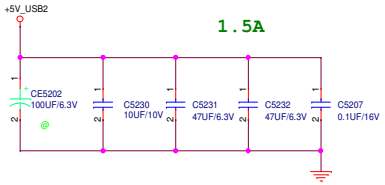
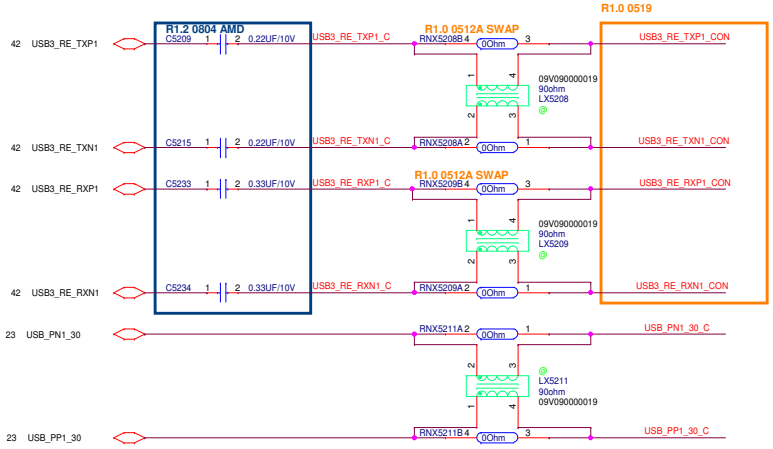
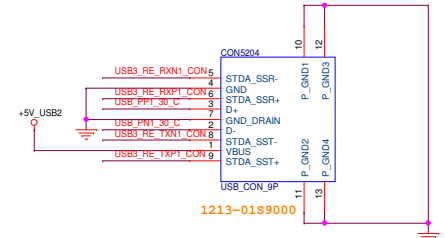
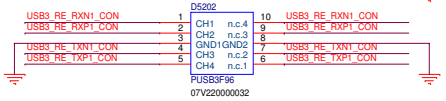
Title: SATA SSD_HDD
BGT-HW3 RD
Engineer: Jack_Lee
Size: Custom
Project Name: BK5EA
Rev: 1.1
Date: Friday, March 09, 2018
Sheet 51 of 94

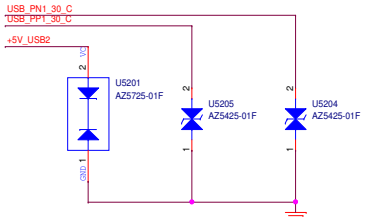






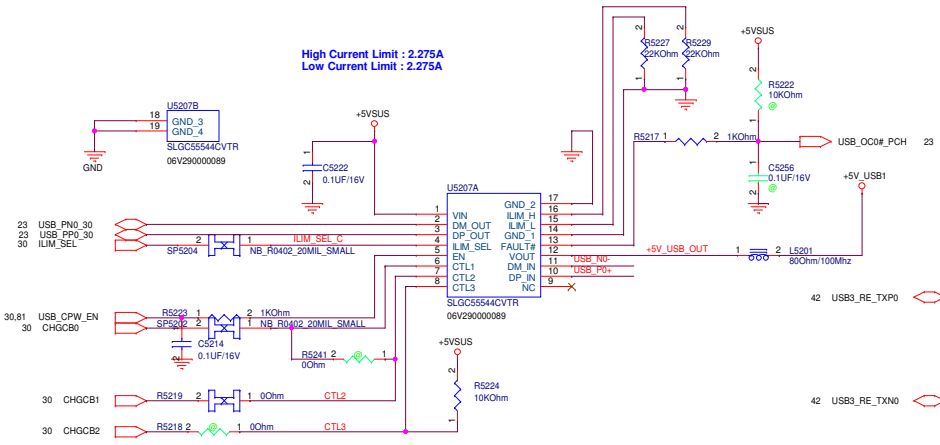


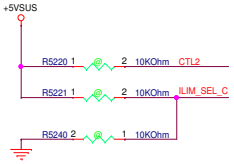




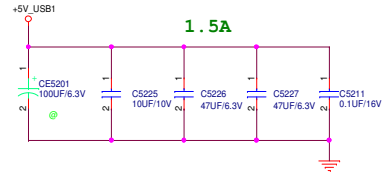
USB 3.0 ports x 1 with Sleep & Charge Left_Down

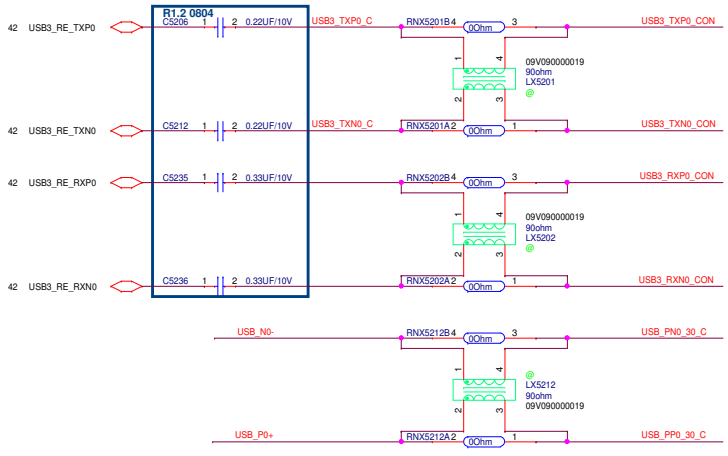
Device	Pega No.	VX No.
SLGC55544CVTR	0629-00TJ000	06V290000089 (Default)

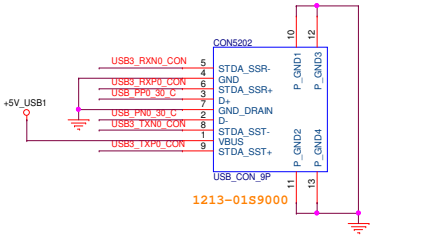


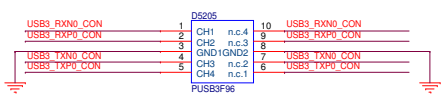


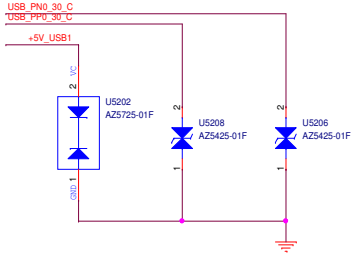
System Global Power State	TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP (Standard Downstream)	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode, no mouse wake	0	0	1	0	ILIM_HI
S3	Dedicated Charging Port Auto mode,	0	1	1	X	ILIM_HI
S3	SDP, keyboard/ mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO









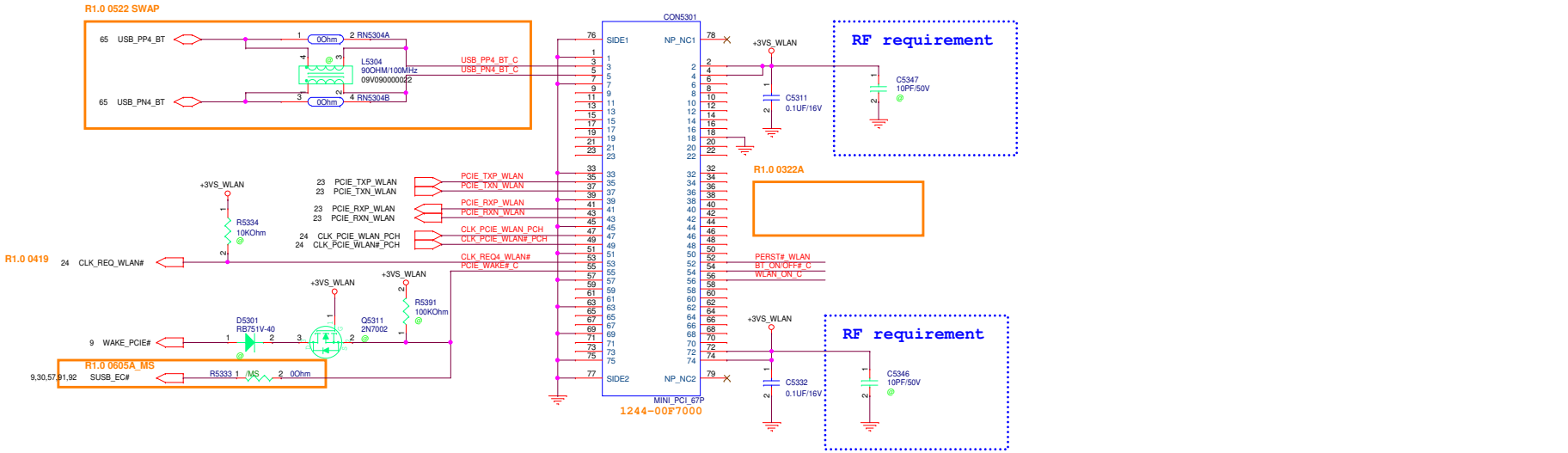


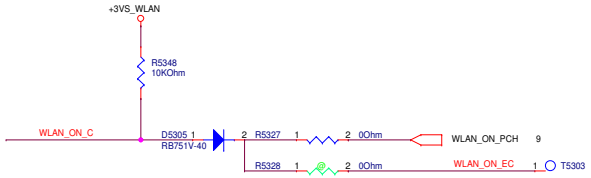
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
3G1-HW3 RD

Title: USB3.0_Charge IC
Engineer: Jack_Lee

Size	Project Name	Rev
C	BK5BA	1.1

Date: Friday, March 09, 2018 Sheet 52 of 94

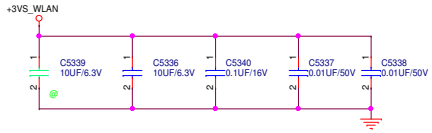


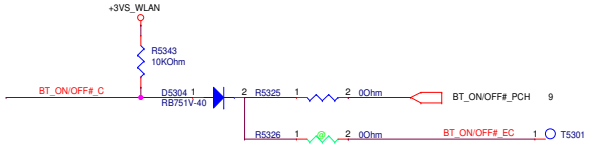


+3V_WLAN_WP1 bypass capactor:

Place 0.1UF near pin 2,4

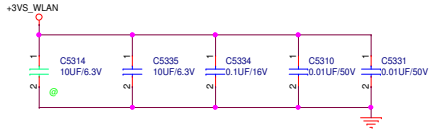
Place 10UF near +3V_WLAN_WP1 source side.

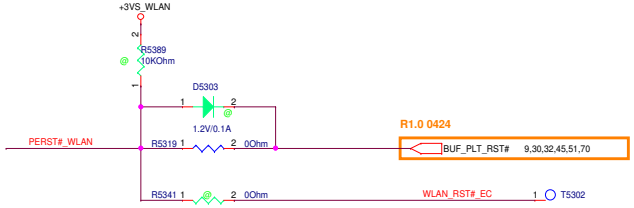


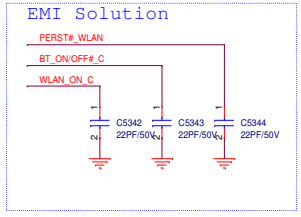


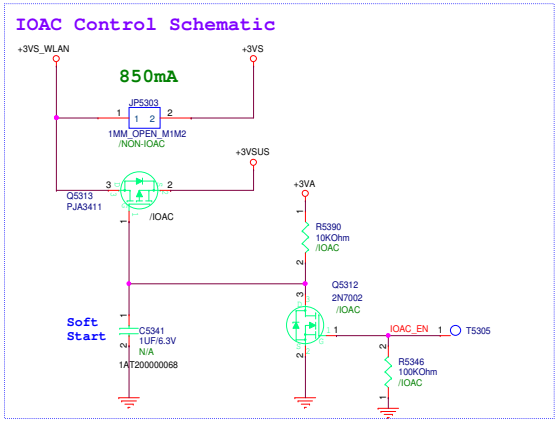
Place 0.1UF near pin 72,74.

Place 10UF near +3V_WLAN_WP1 source side.









PEGATRON Title : PCIE_WLAN_BT

PEGATRON PROPRIETARY AND CONFIDENTIAL

3G1-HW3 RD

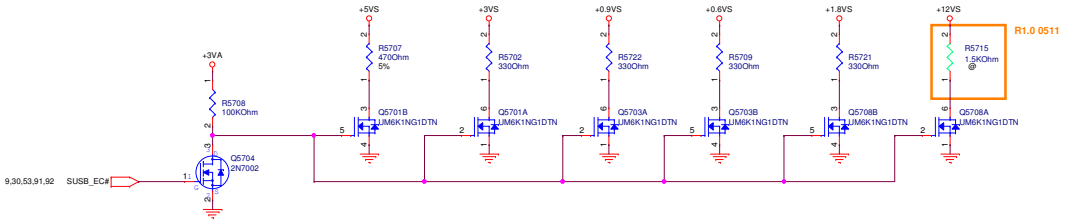
Engineer: Jack_Lee

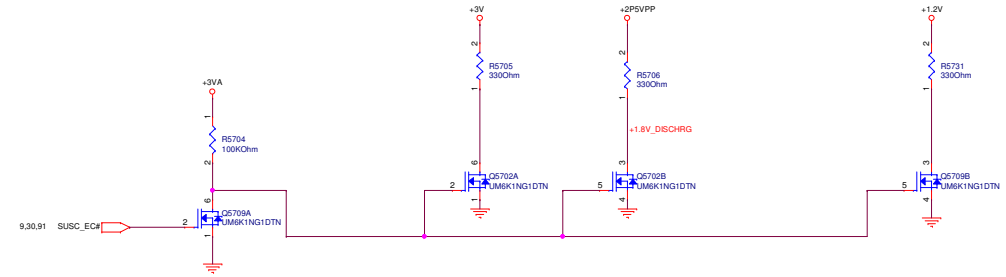
Size	Project Name	Rev
C	BK5BA	1.1

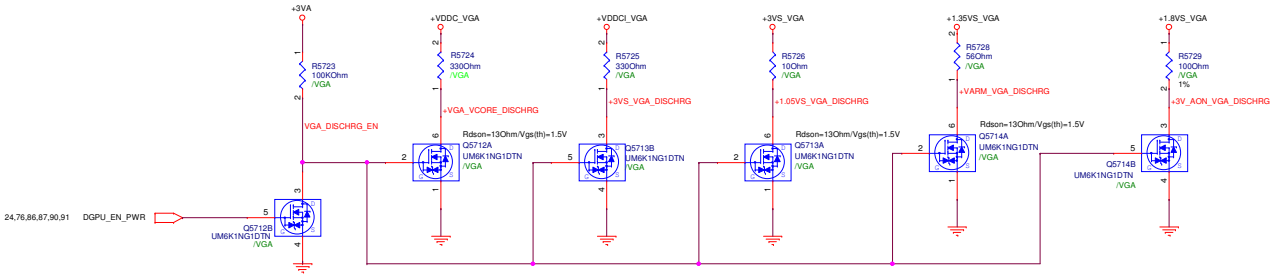
Date: Friday, March 09, 2018 Sheet 53 of 94

Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 54 of 94

Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 55 of 94







+3VA +3VA 24,30,31,36,53,65,67,81,88,93
+5VS +5VS 13,31,36,45,48,50,51,69,80,87,91
+3VS +3VS 8,9,11,13,24,30,31,32,36,41,44,45,50,51,53,60,62,64,69,91,92
+0.6VS +0.6VS 15,83
+0.9VS +0.9VS 8,11,82 R1.0 0322A
+1.8VS +1.8VS 8,11,12,24,28,36,80,91
+12VS +12VS 31,91

+3V +3V 31,45,65,67,91

+2P5VPP +2P5VPP 16,17,84
+1.2V +1.2V 7,11,15,16,17,19,83

PEGATRON Title : DISCHARGE
PEGATRON PROPRIETARY AND CONFIDENTIAL
BGT-HW3 RD Engineer: Jack_Lee

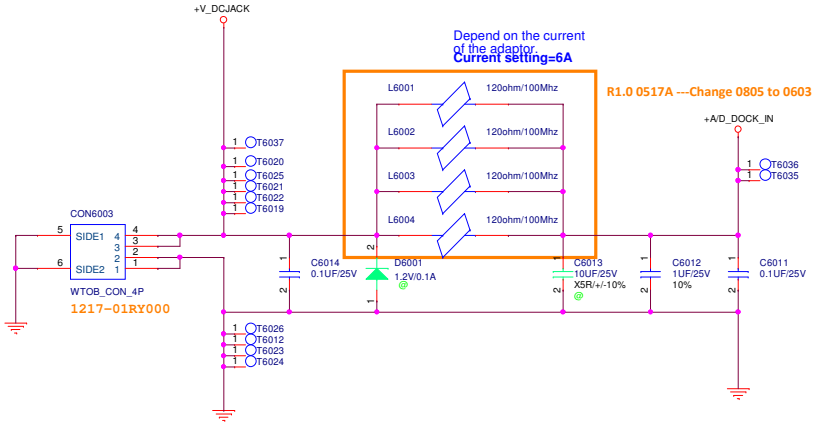
Size	Project Name	Rev
Custom	BK5EA	1.1

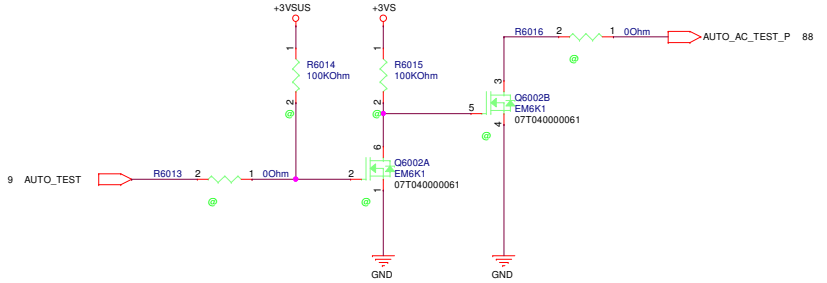
Date: Friday, March 09, 2018 Sheet 57 of 94

Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 58 of 94

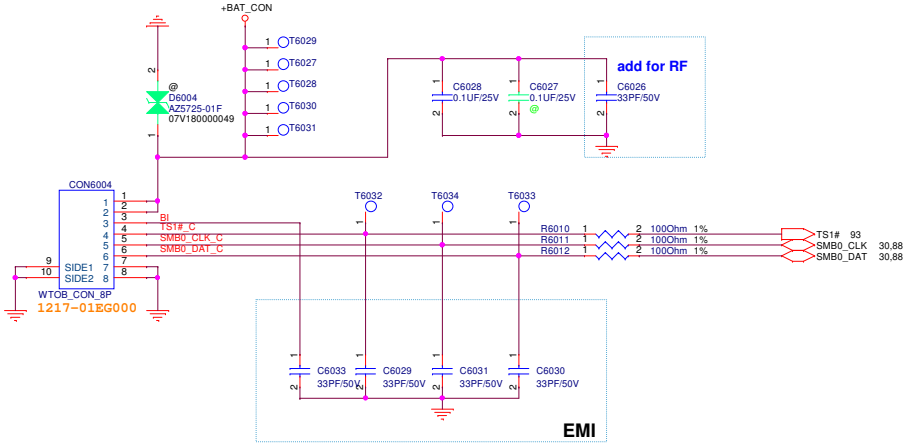
Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 59 of 94

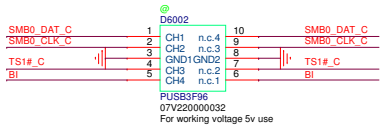
DC Jack WTB CONN

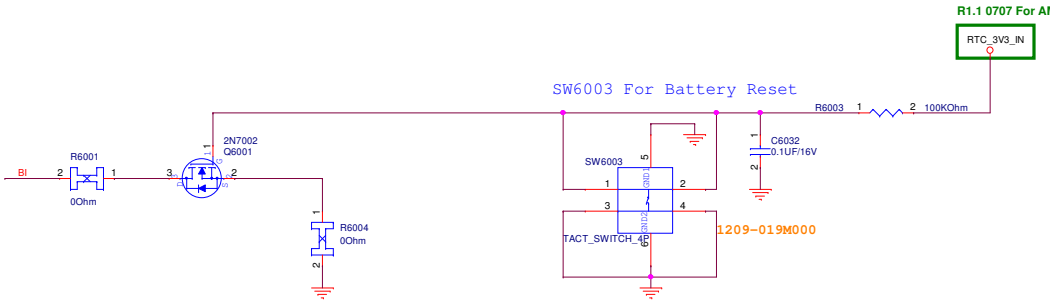




Battery Connector

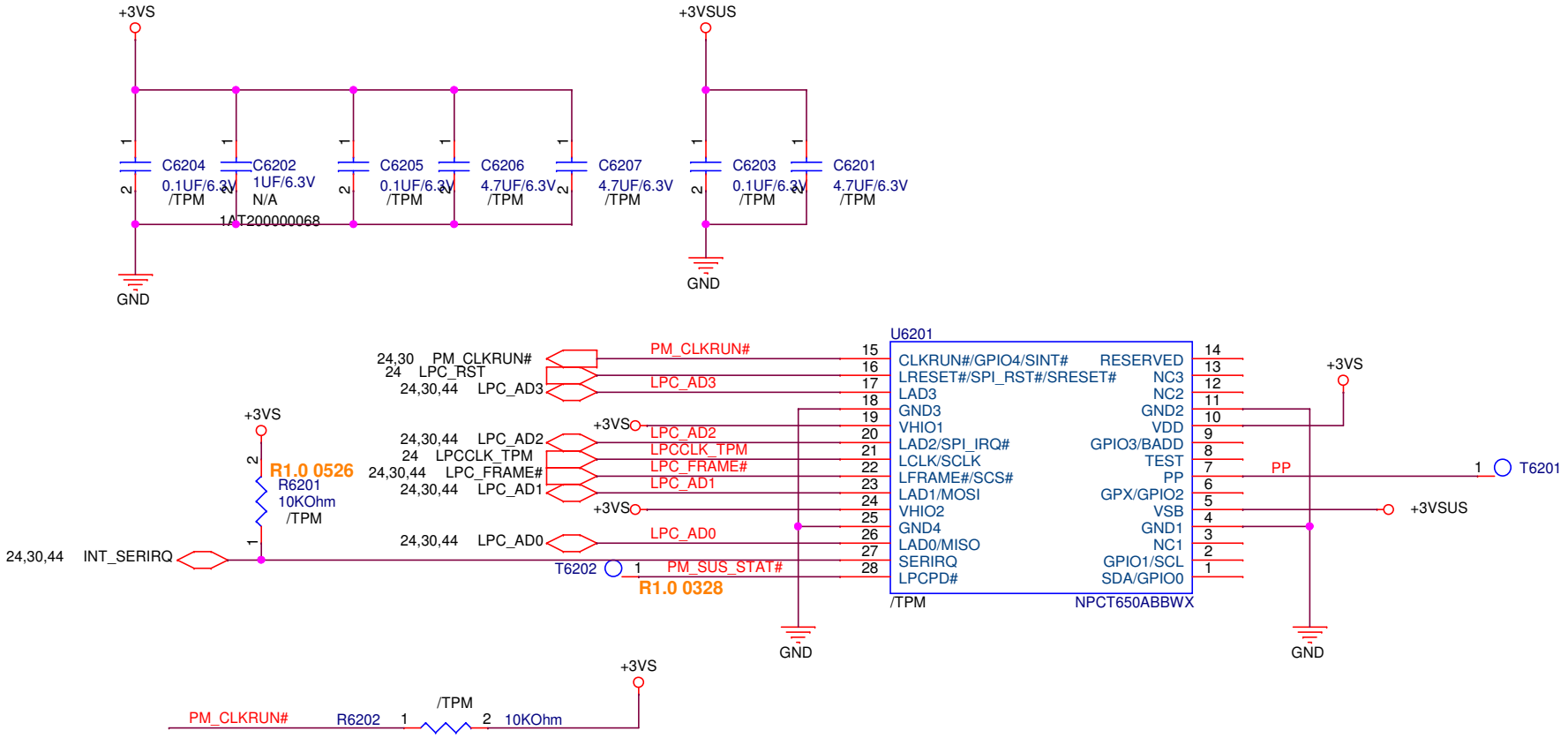






PEGATRON	Title : DC_BAT_CONN		
BG1-HW3 RD	Engineer: Jack_Lee		
Size: Custom	Project Name: BK5EA		Rev: 1.1
Date: Friday, March 09, 2018	Sheet 60 of 94		

Title	<Title>
Size: A	Document Number: BK5EA
Rev: 1.1	
Date: Friday, March 09, 2018	Sheet 61 of 94



PEGATRON	Title : TPM NPCT650	
BG1-HW3 RD	Engineer: Jack_Lee	
Size: Custom	Project Name: BK5EA	Rev: 1.1
Date: Friday, March 09, 2018	Sheet 62 of 94	

<Variant Name>

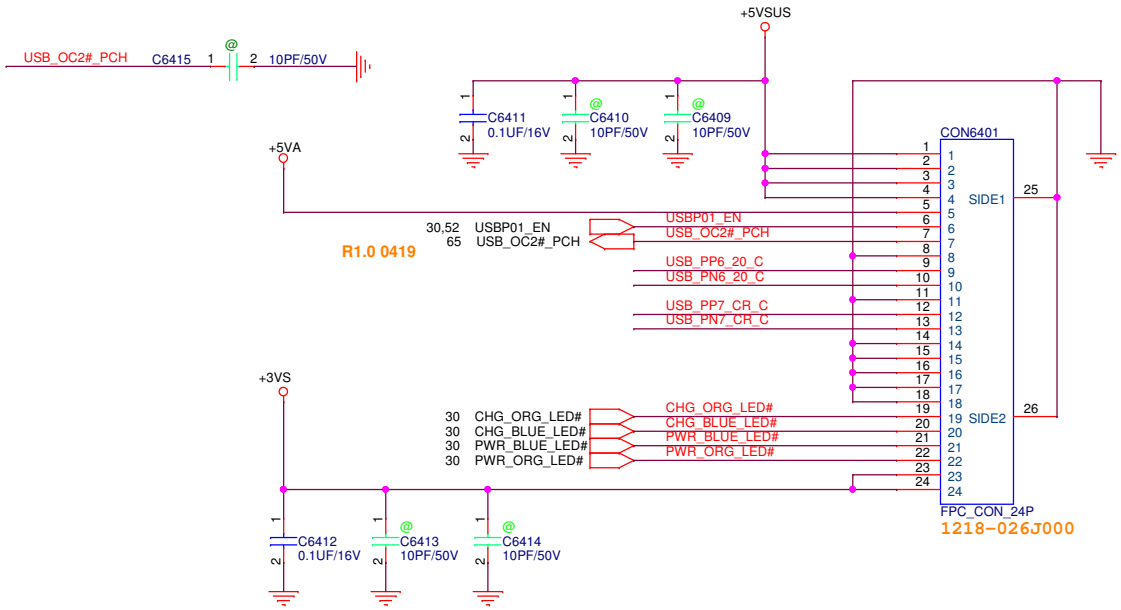
PEGATRON

Title : USB 2.0 Hub

Engineer: Jack_Lee

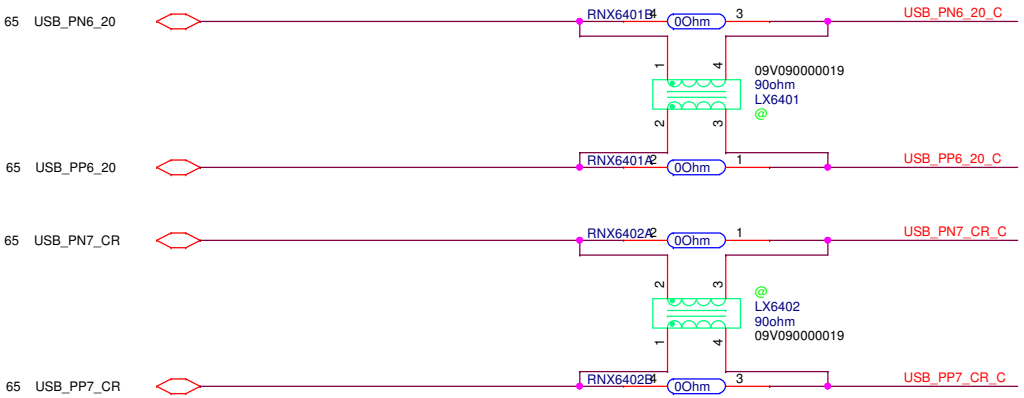
Size	Project Name	Rev
A	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 63 of 94



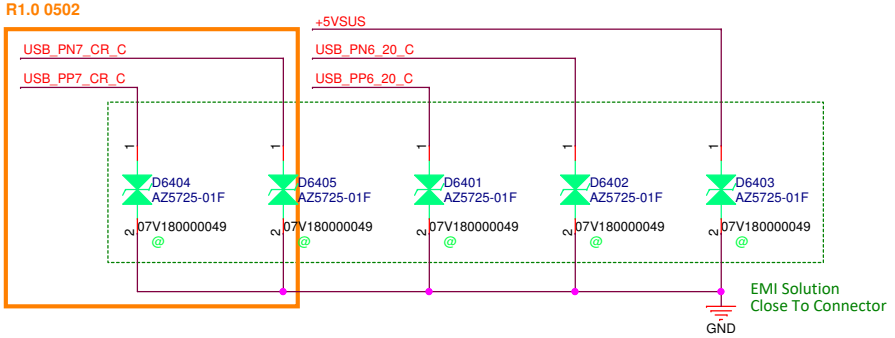
DB Connector Pin Define(MB Side)

1	+5VSUS
2	+5VSUS
3	+5VSUS
4	+5VSUS
5	+5VA
6	USB_EN
7	USB_OC
8	GND_IO
9	USB_PP1_20
10	USB_PN1_20
11	GND_IO
12	USB_PP2_20
13	USB_PN2_20
14	GND_IO
15	GND_IO
16	GND_IO
17	GND_IO
18	GND_IO
19	CHG_ORG_LED#
20	CHG_BLUE_LED#
21	PWR_BLUE_LED#
22	PWR_ORG_LED#
23	+3VS
24	+3VS



R1.0 0512A SWAP

R1.0 0502



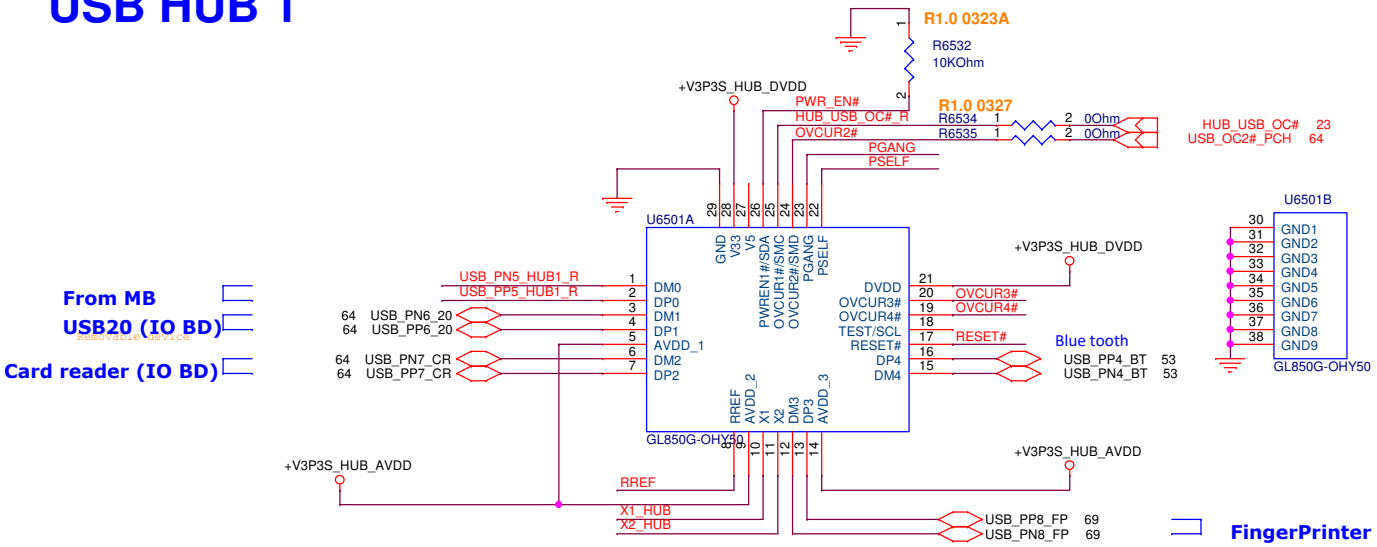
PEGATRON Title : IO Board

BG1-HW3 RD Engineer: Jack_Lee

Size	Project Name	Rev
B	BK5EA	1.1

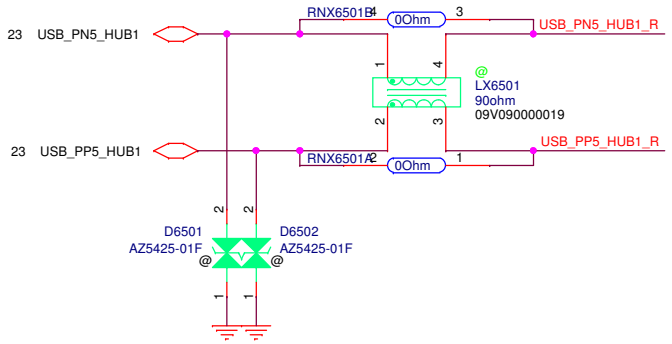
Date: Friday, March 09, 2018 Sheet 64 of 94

USB HUB 1

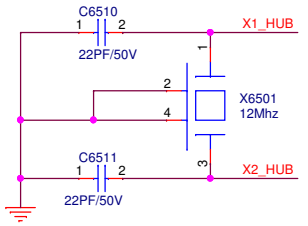


From MB
USB20 (IO BD)
Card reader (IO BD)

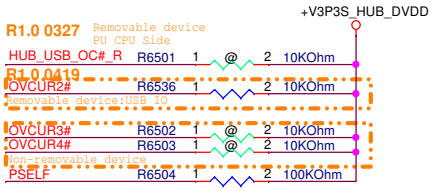
CHOKE



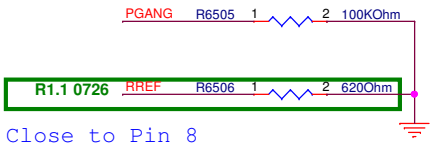
Crystal



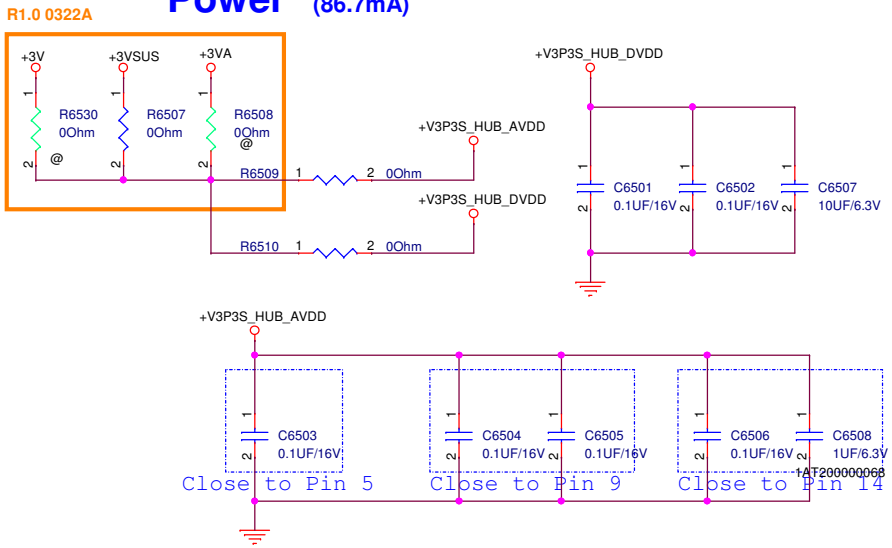
Pull-High

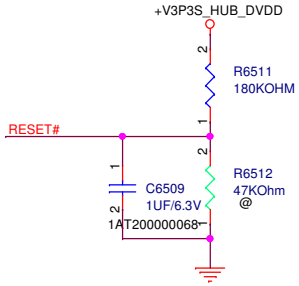


Pull-Low



Power (86.7mA)





<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : USB Hub

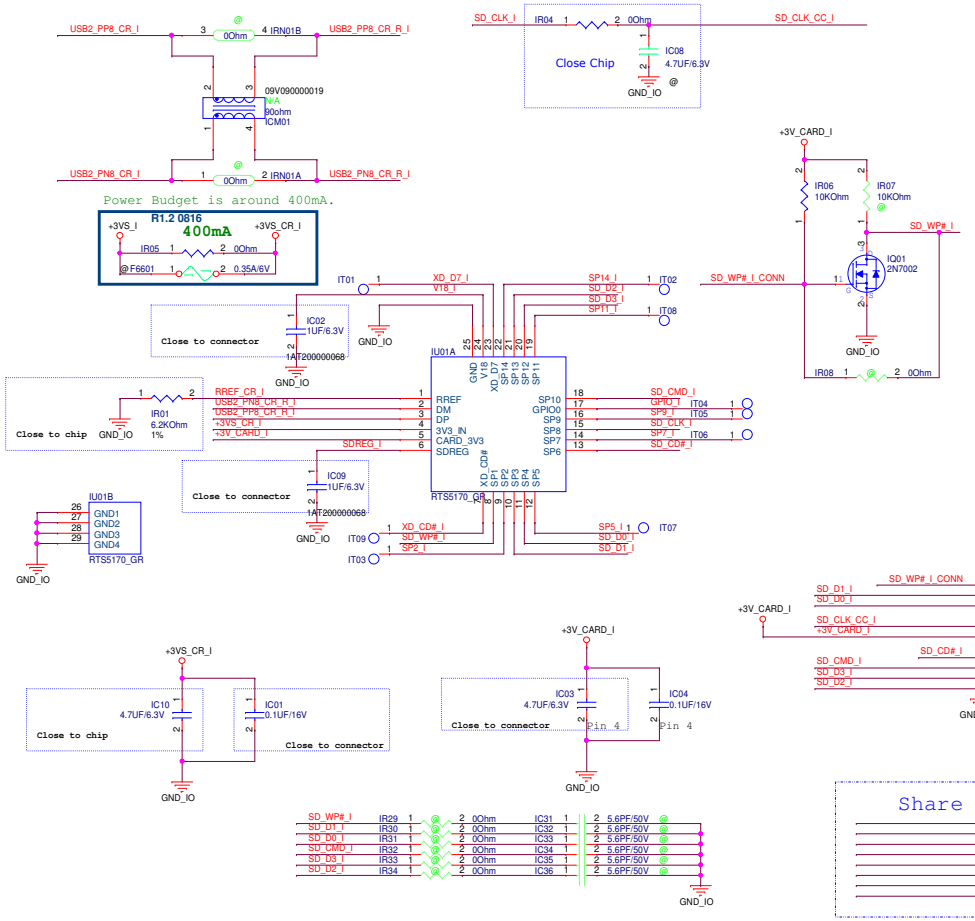
Engineer: Jack_Lee

Size	Project Name	Rev
B	BK5EA	1.1

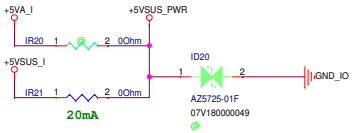
Date: Friday, March 09, 2018 Sheet 65 of 94

66 IO Board

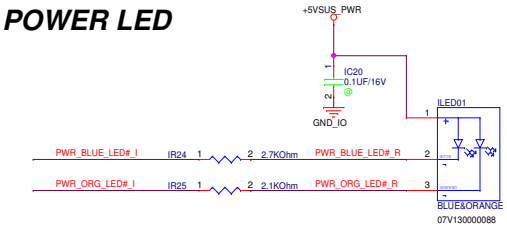
Card Reader



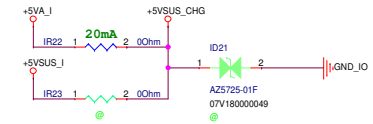
POWER LED



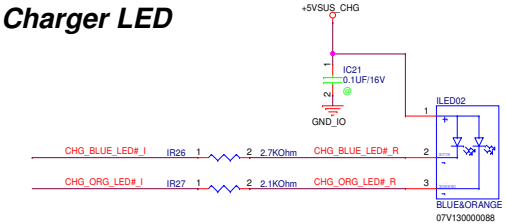
POWER LED

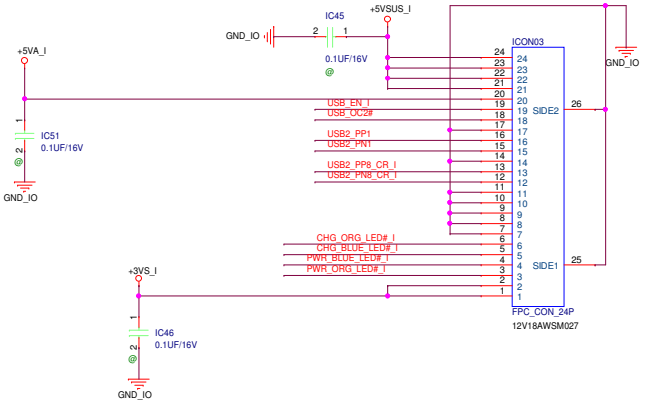


Charger LED

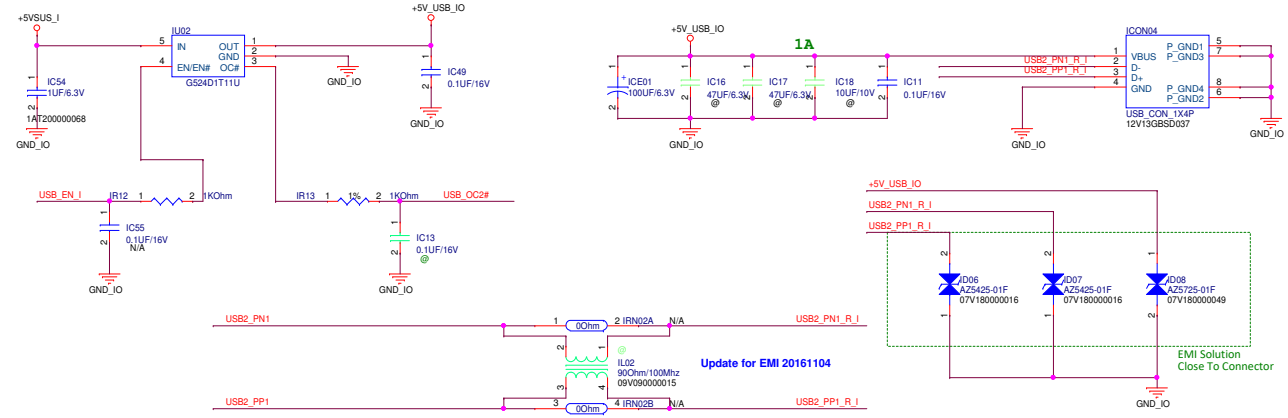


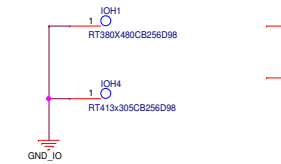
Charger LED



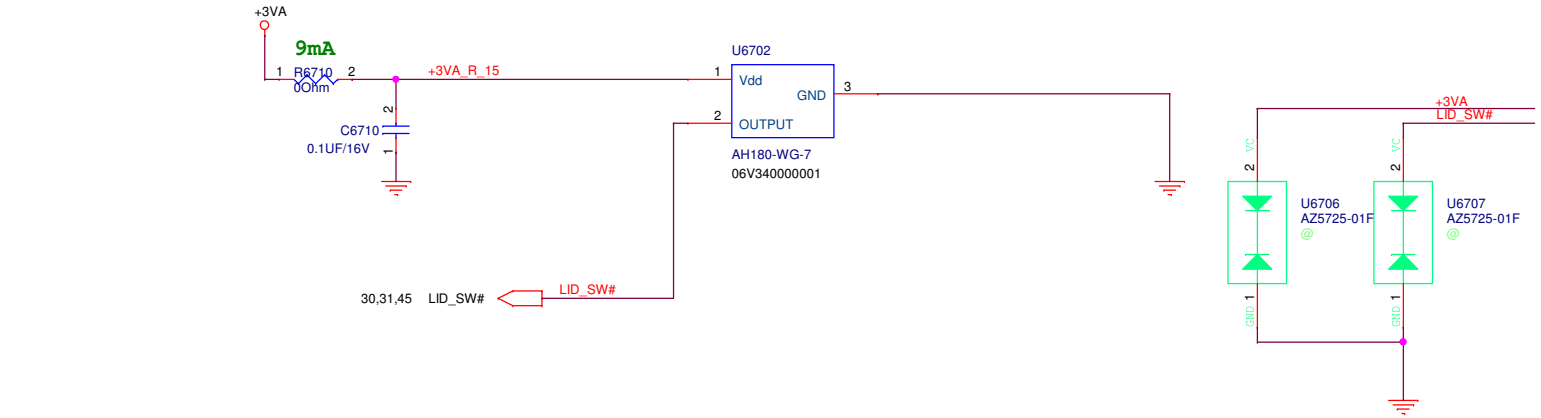


USB 2.0





PEGATRON PROPRIETARY AND CONFIDENTIAL	Title : IO Board	
BG1-HW3 RD	Engineer: Jack_Lee	
Size: C	Project Name: BK5BA	Rev: 1.1
Date: Friday, March 09, 2018	Sheet 66 of 94	



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Sensor Board

BG1-HW3 RD

Engineer: Jack_Lee

Size	Project Name	Rev
B	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 67 of 94

68 ME Hole

IOPORT SHIELDING(Screw G)

H6879
RT315X287D94

2017.3.27
R1.3---For ME

H6884
RT226x276B114D98

2017.4.26
R1.4---For BL

2.5X3.0 NPTH(Screw H)

H6825
O118X98DO118X98N

6mm NPTH(Screw E,K)

H6876
HOLE_NPTH

CPU NUT(Screw A1)*4

H6801 H6802 H6803 H6804
CT217B136ID106
1308-00NA000

SSD (Screw NUT)

H6880
CT217B140D110
N/A
1308-00LG000

2.5 NPTH(Screw P)

H6821
C98D98N
temp_5262_gh15

GPU NUT(Screw B1)*2

H6805 H6806
CT217B136ID106
/VGA
1308-00NA000

Audio Jack (screw J)

H6878
R335X394D118

2017.3.28
R1.3---For ME

(Screw C)

H6836
P_GND
NP_NC2 ... NP_NC31
NP_NC32 ... NP_NC61
S394D118

H6837
P_GND
NP_NC2 ... NP_NC31
NP_NC32 ... NP_NC61
S394D118

Main Shielding NUT*2

H6829
CT217B140D110
N/A
1308-00LG000

H6834
CT217B140D110
N/A
1308-00LG000

Main shielding (Screw D,L)

H6881
GND NP_NC
D98N_D110

H6882
GND NP_NC
D110_DO118X98N

Screw support metal(Screw I)*2

H6838
NP_NC
SUPPORT_METAL_3P
N/A
13N1-20M0201

H6839
NP_NC
SUPPORT_METAL_3P
N/A
13N1-20M0201

T6801
TPC50T_68

CPU Clip(BOT)*20

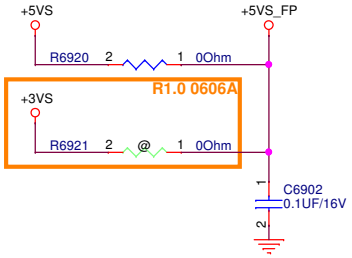
R1.0 0614 For ME

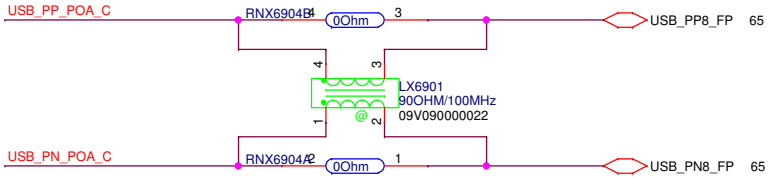
H6851 H6852 H6853 H6854
H6855 H6856 H6857 H6858
H6859 H6860 H6861 H6862
H6883 H6864 H6865 H6866
H6867 H6868 H6869 H6870
1000300037

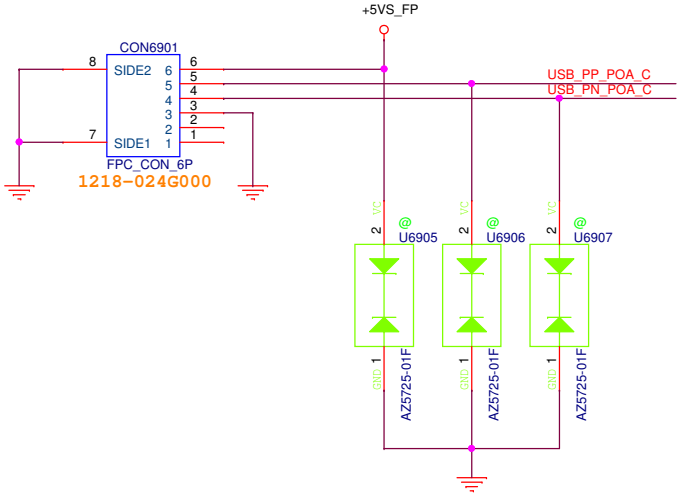
IO Clip(TOP)*4

H6871 H6872 H6873 H6874
MA090-002M110P

PEGATRON Title : ME Hole
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD
Engineer: Jack_Lee
Size: C | Project Name: BK5EA | Rev: 1.1
Date: Friday, March 09, 2018 | Sheet 68 of 94







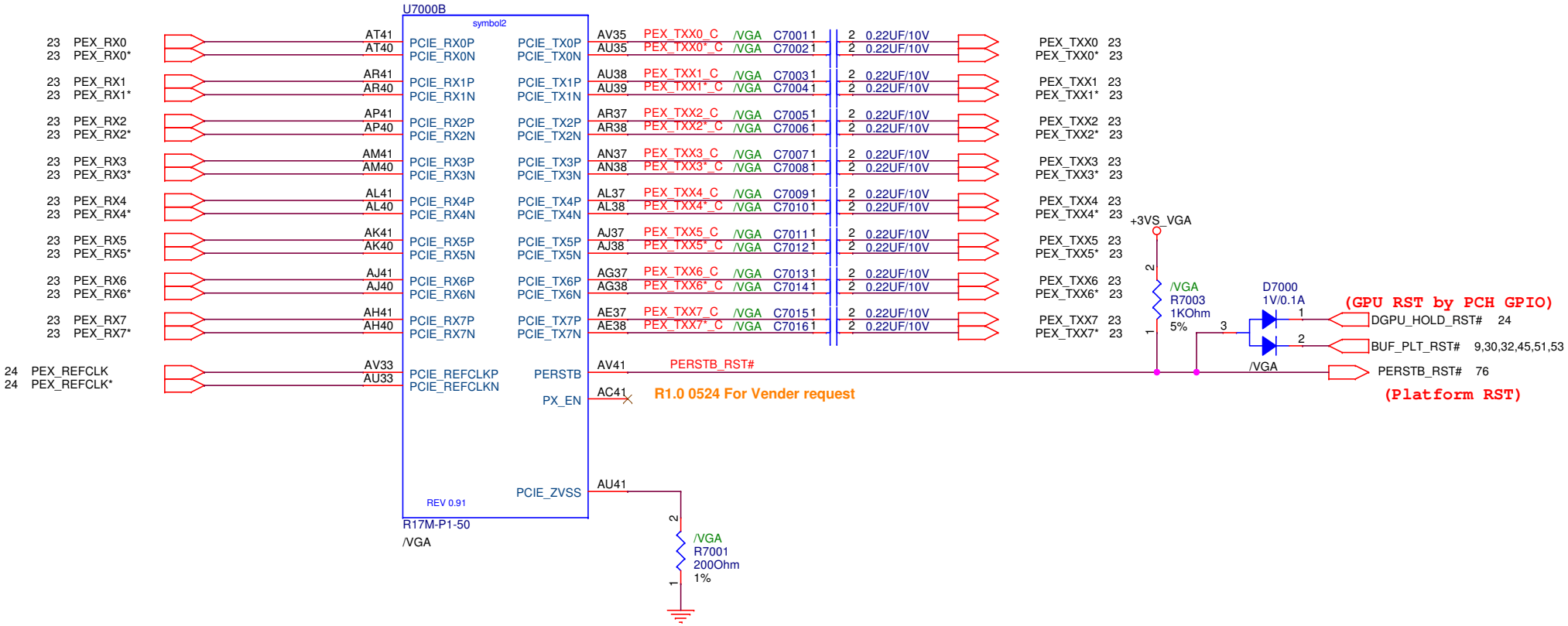
Pin	Definition
1	+PP_VCC
2	USBP
3	USBN
4	GND
5	NC
6	NC

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD

Title : Finger printer
Engineer: Jack_Lee

Size	Project Name	Rev
B	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 69 of 94



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : GPU-PCIE

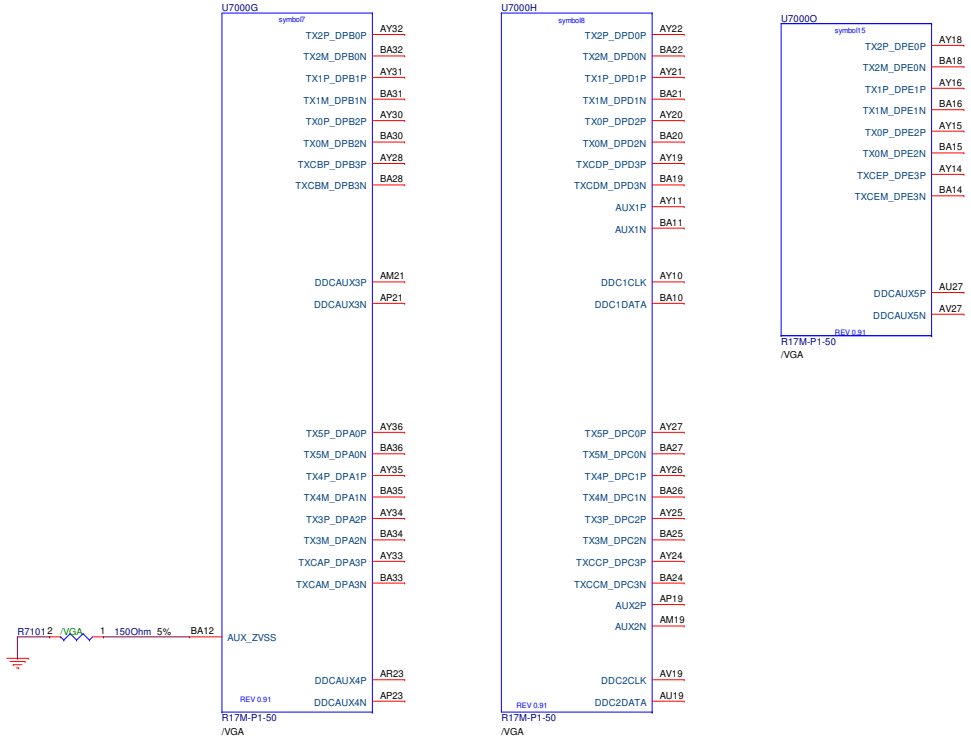
BG1-HW3 RD

Engineer: Jack_Lee

Size	Project Name	Rev
Custom	BK5EA	1.1

Date:

Sheet 70 of 96



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

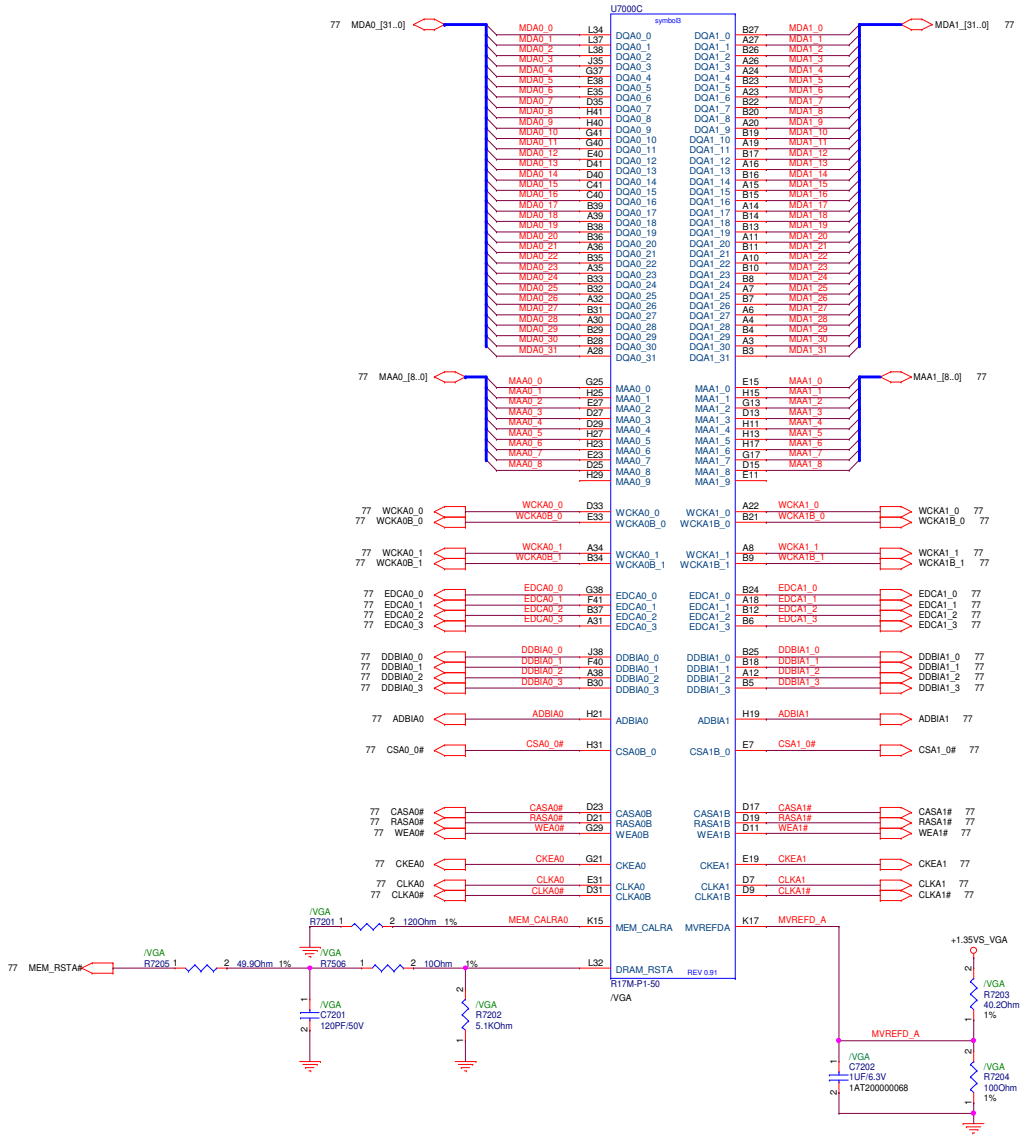
Title : GPU-DISPLAY

Engineer: Jack_Lee

BG1-HW3 RD

Size	Project Name	Rev
Custom	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 71 of 96



PEGATRON Title : GPU-MEM_CTRL_CHA

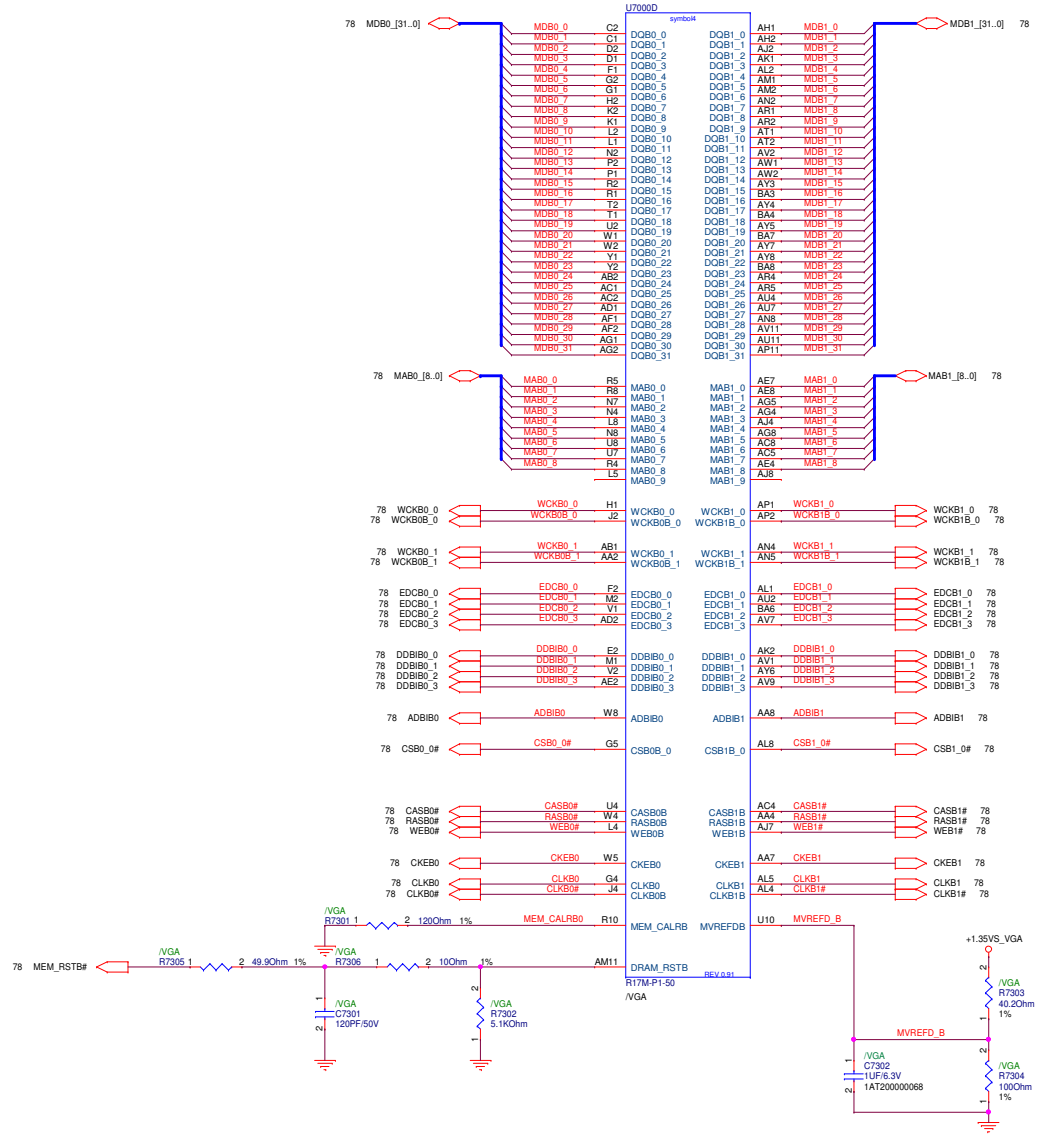
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Jack_Lee

BG1-HW3 RD

Size	Project Name	Rev
C	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 72 of 96



PEGATRON PROPRIETARY AND CONFIDENTIAL

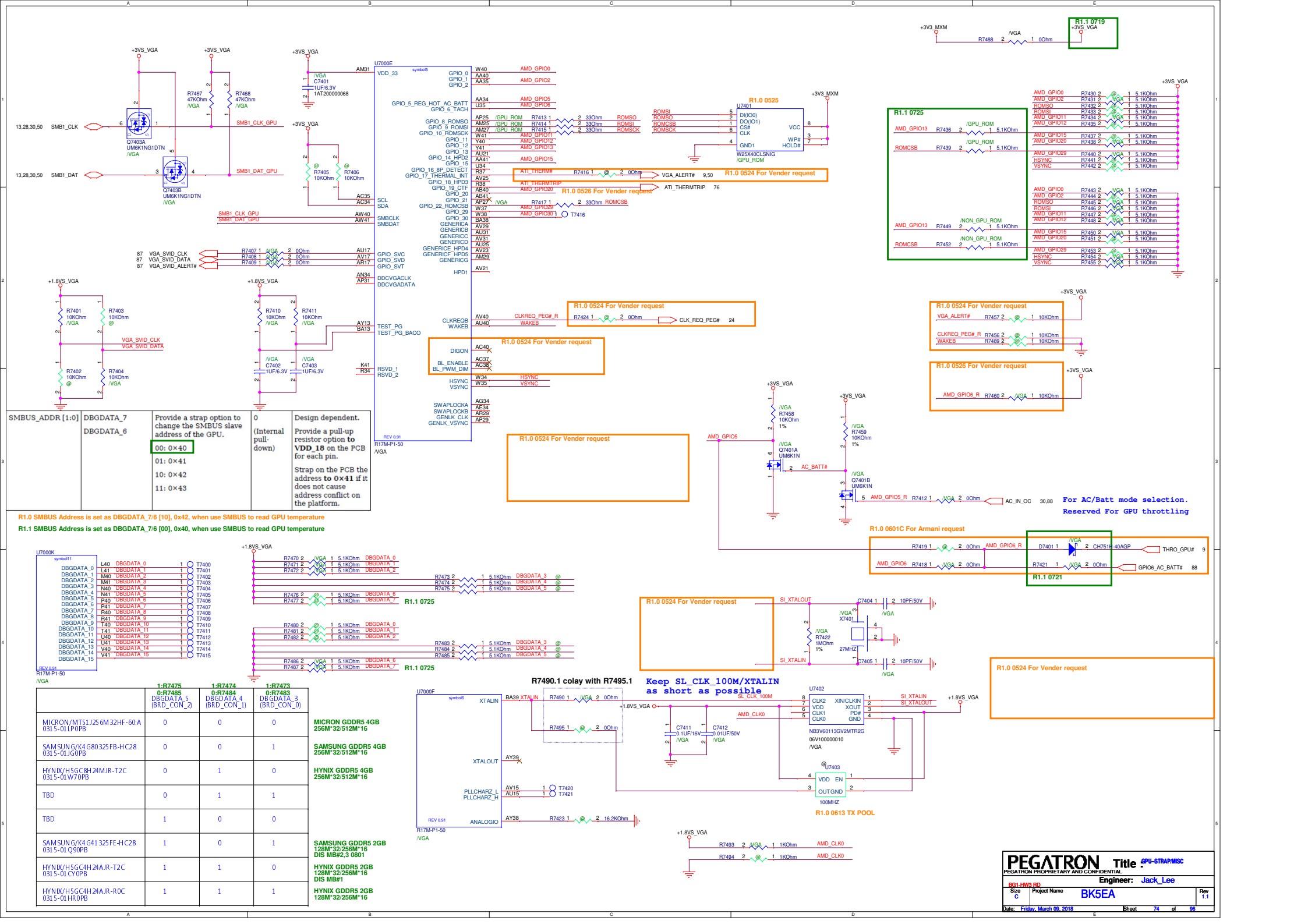
Title : GPU-MEM_CTRL_CHB

Engineer: Jack_Lee

BG1-HW3 RD

Size	Project Name	Rev
C	BK5EA	1.1

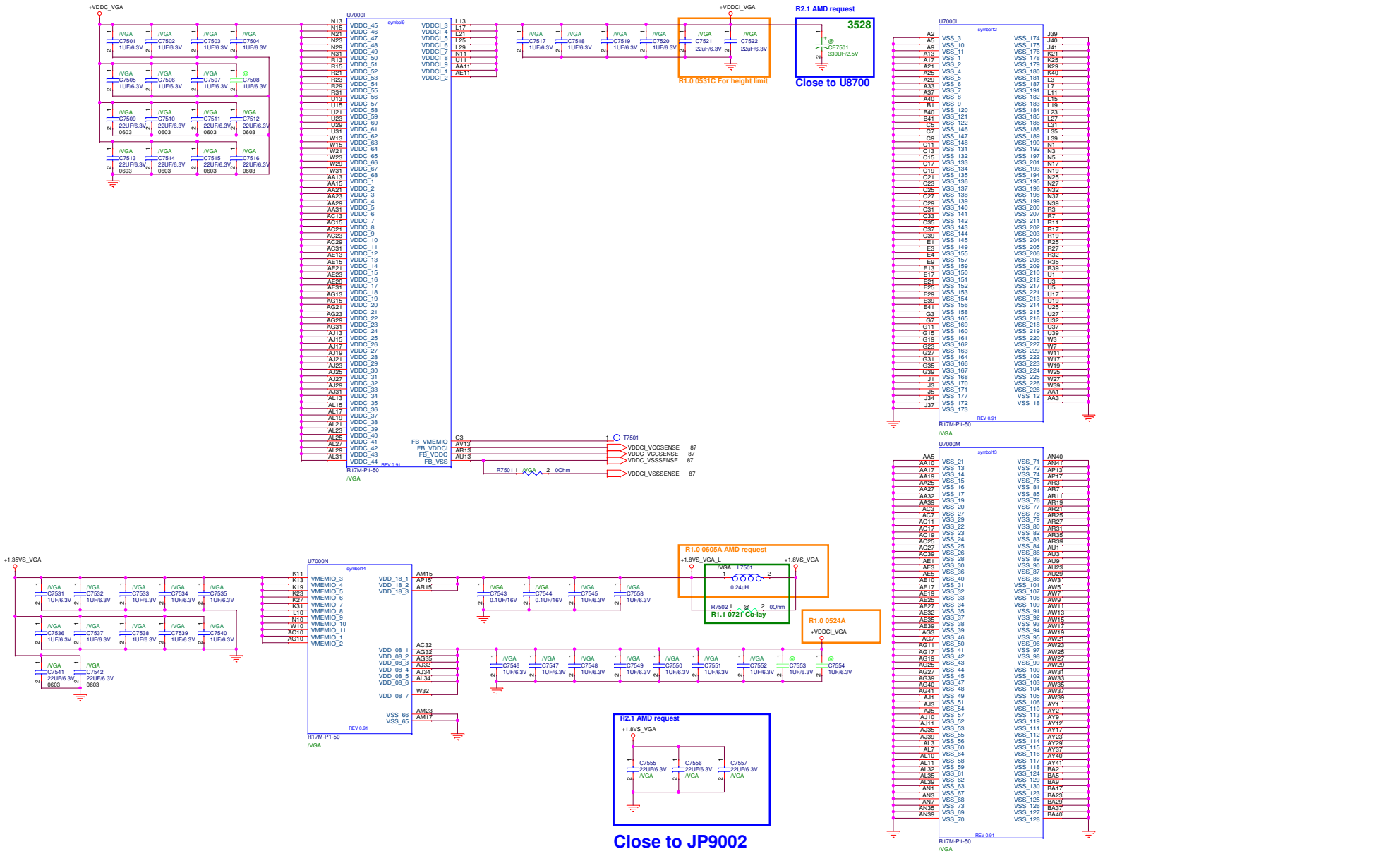
Date: Friday, March 09, 2018 Sheet 73 of 96



SMBUS_ADDR [1:0]	DBGDATA_7 DBGDATA_6	Provide a strap option to change the SMBUS slave address of the GPU. 00: 0×40 01: 0×41 10: 0×42 11: 0×43	0 (Internal pull-down)	Design dependent. Provide a pull-up resistor option to **VDD_18** on the PCB for each pin. Strap on the PCB the address to **0×41** if it does not cause address conflict on the platform.

	1:R7475 0:R7485 DBGDATA_5 (BRD_CON_2)	1:R7474 0:R7484 DBGDATA_4 (BRD_CON_1)	1:R7473 0:R7483 DBGDATA_3 (BRD_CON_0)	
MICRON/MT51J256M32HF-60:A 0315-01LP0PB	0	0	0	MICRON GDDR5 4GB 256M*32/512M*16
SAMSUNG/K4G80325FB-HC28 0315-01JG0PB	0	0	1	SAMSUNG GDDR5 4GB 256M*32/512M*16
HYNIX/H5GC8H24MJR-T2C 0315-01W70PB	0	1	0	HYNIX GDDR5 4GB 256M*32/512M*16
TBD	0	1	1	
TBD	1	0	0	
SAMSUNG/K4G41325FE-HC28 0315-01Q90PB	1	0	1	SAMSUNG GDDR5 2GB 128M*32/256M*16 DIS MB#2,3 0801
HYNIX/H5GC4H24AJR-T2C 0315-01CY0PB	1	1	0	HYNIX GDDR5 2GB 128M*32/256M*16 DIS MB#1
HYNIX/H5GC4H24AJR-R0C 0315-01HR0PB	1	1	1	HYNIX GDDR5 2GB 128M*32/256M*16

PEGATRON Title : GPU-STRAP/MISC
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Jack_Lee
BG1-HW3 RD
Size C | Project Name BK5EA | Rev 1.1
Date: Friday, March 09, 2018 | Sheet 74 of 96


+VDDC_VGA
U7000I
symbol9
VDDC_45
VDDC_46
VDDC_47
VDDC_48
VDDC_49
VDDC_50
VDDC_51
VDDC_52
VDDC_53
VDDC_54
VDDC_55
VDDC_56
VDDC_57
VDDC_58
VDDC_59
VDDC_60
VDDC_61
VDDC_62
VDDC_63
VDDC_64
VDDC_65
VDDC_66
VDDC_67
VDDC_68
VDDC_1
VDDC_2
VDDC_3
VDDC_4
VDDC_5
VDDC_6
VDDC_7
VDDC_8
VDDC_9
VDDC_10
VDDC_11
VDDC_12
VDDC_13
VDDC_14
VDDC_15
VDDC_16
VDDC_17
VDDC_18
VDDC_19
VDDC_20
VDDC_21
VDDC_22
VDDC_23
VDDC_24
VDDC_25
VDDC_26
VDDC_27
VDDC_28
VDDC_29
VDDC_30
VDDC_31
VDDC_32
VDDC_33
VDDC_34
VDDC_35
VDDC_36
VDDC_37
VDDC_38
VDDC_39
VDDC_40
VDDC_41
VDDC_42
VDDC_43
VDDC_44
REV 0.91
R17M-P1-50
/VGA
VDDCI_3
VDDCI_4
VDDCI_5
VDDCI_6
VDDCI_7
VDDCI_8
VDDCI_9
VDDCI_1
VDDCI_2
+VDDCI_VGA
R1.0 0531C For height limit
R2.1 AMD request
3528
Close to U8700
FB_VMEMIO
FB_VDDCI
FB_VDDC
FB_VSS
T7501
VDDCI_VCCSENSE
VDDC_VCCSENSE
VDDC_VSSSENSE
VDDCI_VSSSENSE
R7501 0Ohm
U7000L
symbol12
VSS_3
VSS_10
VSS_11
VSS_1
VSS_2
VSS_4
VSS_5
VSS_6
VSS_7
VSS_8
VSS_9
VSS_120
VSS_121
VSS_122
VSS_146
VSS_147
VSS_148
VSS_131
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VSS_225
VSS_226
VSS_228
VSS_12
VSS_18
U7000M
symbol13
VSS_21
VSS_13
VSS_14
VSS_15
VSS_16
VSS_17
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VSS_27
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VSS_33
VSS_34
VSS_35
VSS_37
VSS_38
VSS_39
VSS_46
VSS_50
VSS_41
VSS_42
VSS_43
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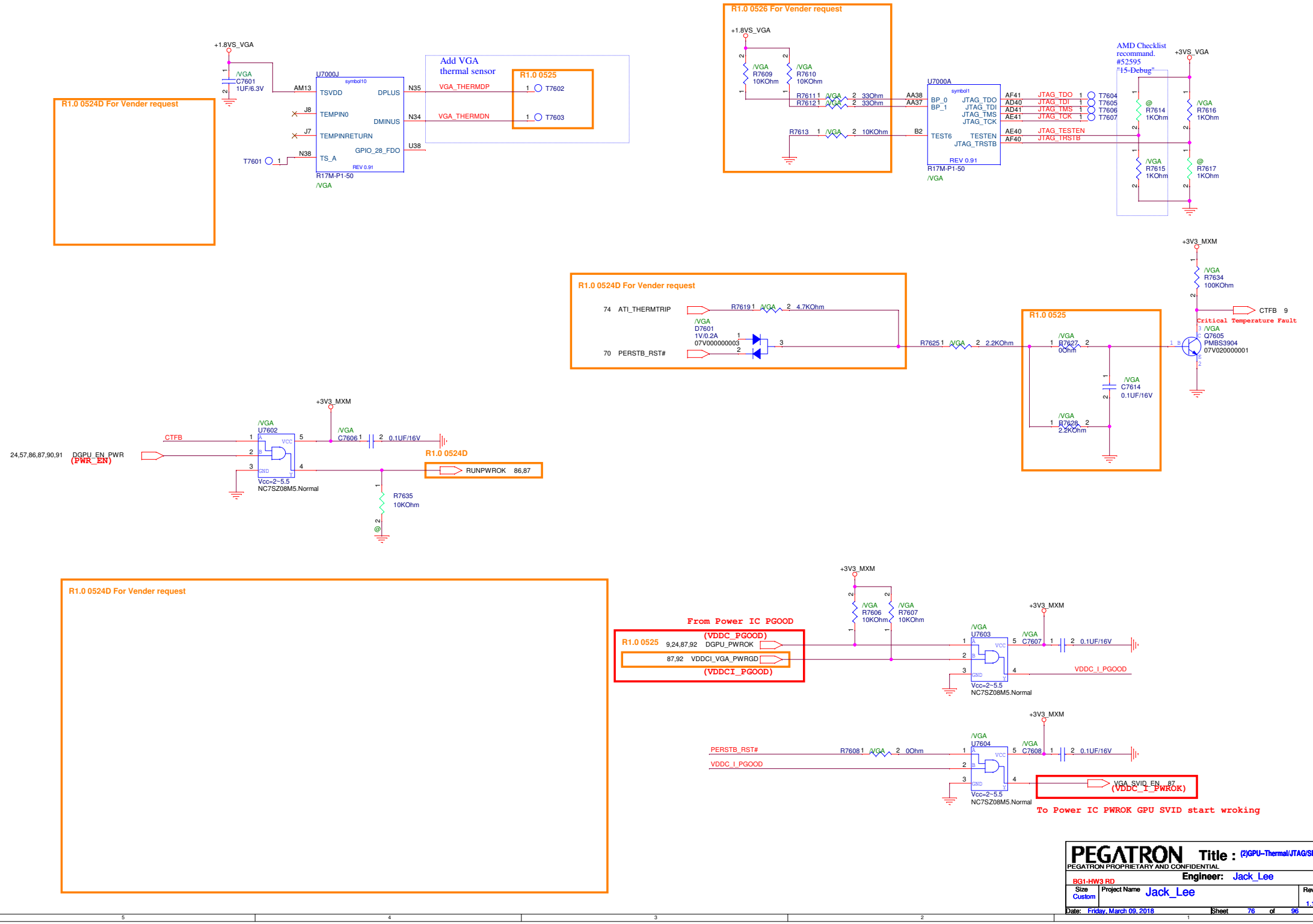
VSS_117
VSS_118
VSS_124
VSS_129
VSS_130
VSS_123
VSS_125
VSS_126
VSS_127
VSS_128
+1.35VS_VGA
U7000N
symbol14
VMEMIO_3
VMEMIO_4
VMEMIO_5
VMEMIO_6
VMEMIO_7
VMEMIO_8
VMEMIO_9
VMEMIO_10
VMEMIO_11
VMEMIO_1
VMEMIO_2
VDD_18_1
VDD_18_2
VDD_18_3
VDD_08_1
VDD_08_2
VDD_08_3
VDD_08_4
VDD_08_5
VDD_08_6
VDD_08_7
VSS_66
VSS_65
R1.0 0605A AMD request
+1.8VS_VGA_L
+1.8VS_VGA
L7501
0.24uH
R7502 0Ohm
R1.1 0721 Co-lay
R1.0 0524A
+VDDCI_VGA
R2.1 AMD request
+1.8VS_VGA
Close to JP9002


R1.0 0524D For Vender request
+1.8VS_VGA
/VGA
C7601
1UF/6.3V
U7000J
symbol10
TSVDD
DPLUS
TEMPIN0
DMINUS
TEMPINRETURN
GPIO_28_FDO
TS_A
REV 0.91
R17M-P1-50
/VGA
AM13
J8
J7
N38
T7601
N35
N34
U38
Add VGA
thermal sensor
VGA_THERMDP
VGA_THERMDN
R1.0 0525
T7602
T7603
R1.0 0526 For Vender request
R7609
10KOhm
R7610
10KOhm
R7611
R7612
33Ohm
R7613
AA38
AA37
B2
U7000A
BP_0
BP_1
TEST6
JTAG_TDO
JTAG_TDI
JTAG_TMS
JTAG_TCK
TESTEN
JTAG_TRSTB
AF41
AD40
AD41
AE41
AE40
AF40
T7604
T7605
T7606
T7607
AMD Checklist
recommand.
#52595
"15-Debug"
+3VS_VGA
R7614
1KOhm
R7616
1KOhm
R7615
1KOhm
R7617
1KOhm
R1.0 0524D For Vender request
74 ATI_THERMTRIP
70 PERSTB_RST#
R7619
4.7KOhm
D7601
1V/0.2A
07V000000003
R7625
2.2KOhm
R1.0 0525
R7627
0Ohm
R7628
2.2KOhm
C7614
0.1UF/16V
+3V3_MXM
R7634
100KOhm
CTFB 9
Critical Temperature Fault
Q7605
PMBS3904
07V020000001
24,57,86,87,90,91 DGPU_EN_PWR
(PWR_EN)
CTFB
U7602
VCC
GND
Vcc=2~5.5
NC7SZ08M5.Normal
C7606
0.1UF/16V
R1.0 0524D
RUNPWROK 86,87
R7635
10KOhm
R1.0 0524D For Vender request
From Power IC PGOOD
(VDDC_PGOOD)
R1.0 0525
9,24,87,92 DGPU_PWROK
87,92 VDDCI_VGA_PWRGD
(VDDCI_PGOOD)
R7606
10KOhm
R7607
10KOhm
U7603
C7607
0.1UF/16V
VDDC_I_PGOOD
PERSTB_RST#
VDDC_I_PGOOD
R7608
0Ohm
U7604
C7608
0.1UF/16V
VGA_SVID_EN 87
(VDDC_I_PWROK)
To Power IC PWROK GPU SVID start wroking
PEGATRON
Title : (2)GPU--Thermal/JTAG/SEQ
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD
Engineer: Jack_Lee
Size Custom
Project Name Jack_Lee
Rev 1.1
Date: Friday, March 09, 2018
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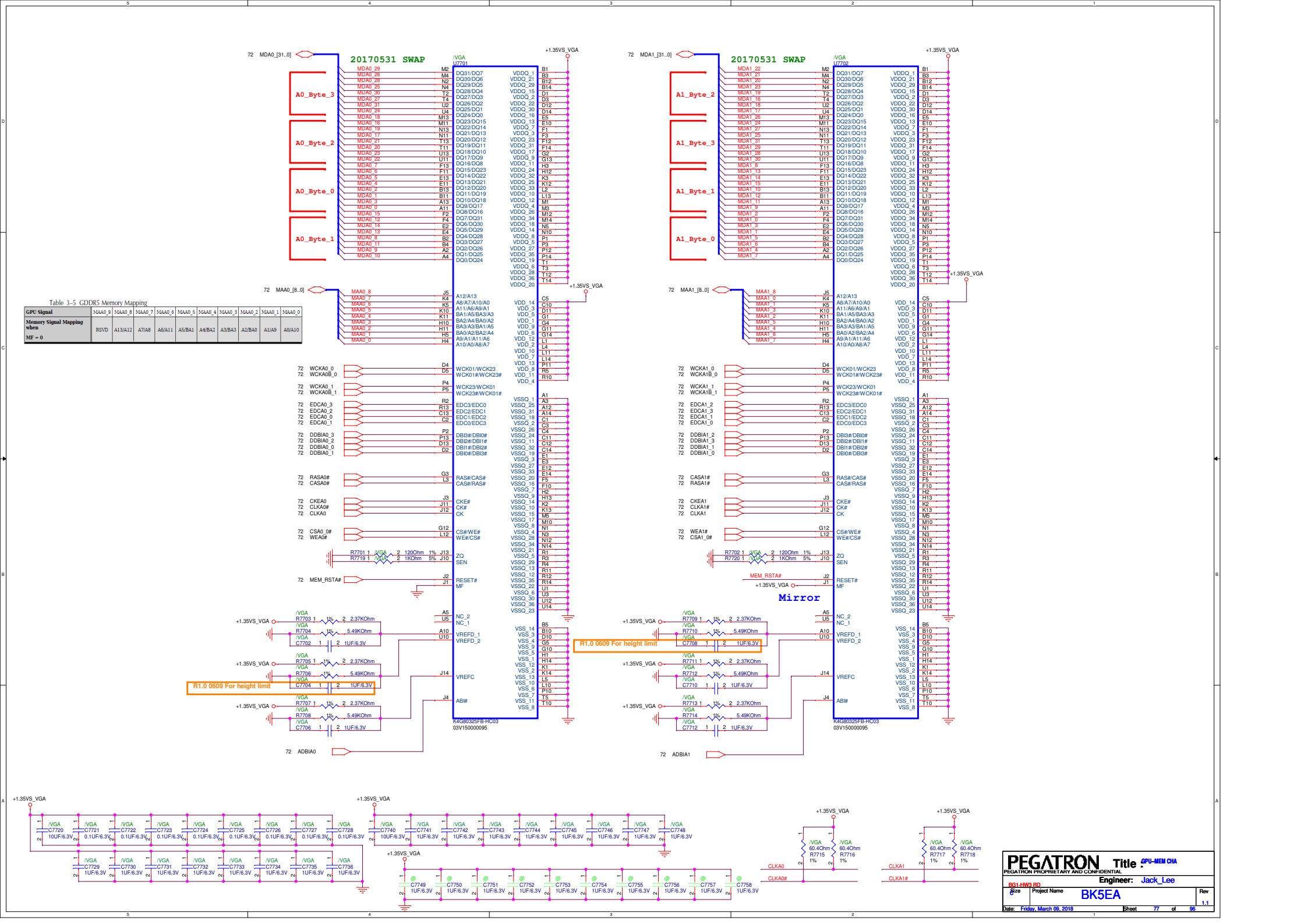


Table 3–5 GDDR5 Memory Mapping

GPU Signal	MAA0_9	MAA0_8	MAA0_7	MAA0_6	MAA0_5	MAA0_4	MAA0_3	MAA0_2	MAA0_1	MAA0_0
Memory Signal Mapping when MF = 0	RSVD	A13/A12	A7/A8	A6/A11	A5/BA1	A4/BA2	A3/BA3	A2/BA0	A1/A9	A0/A10

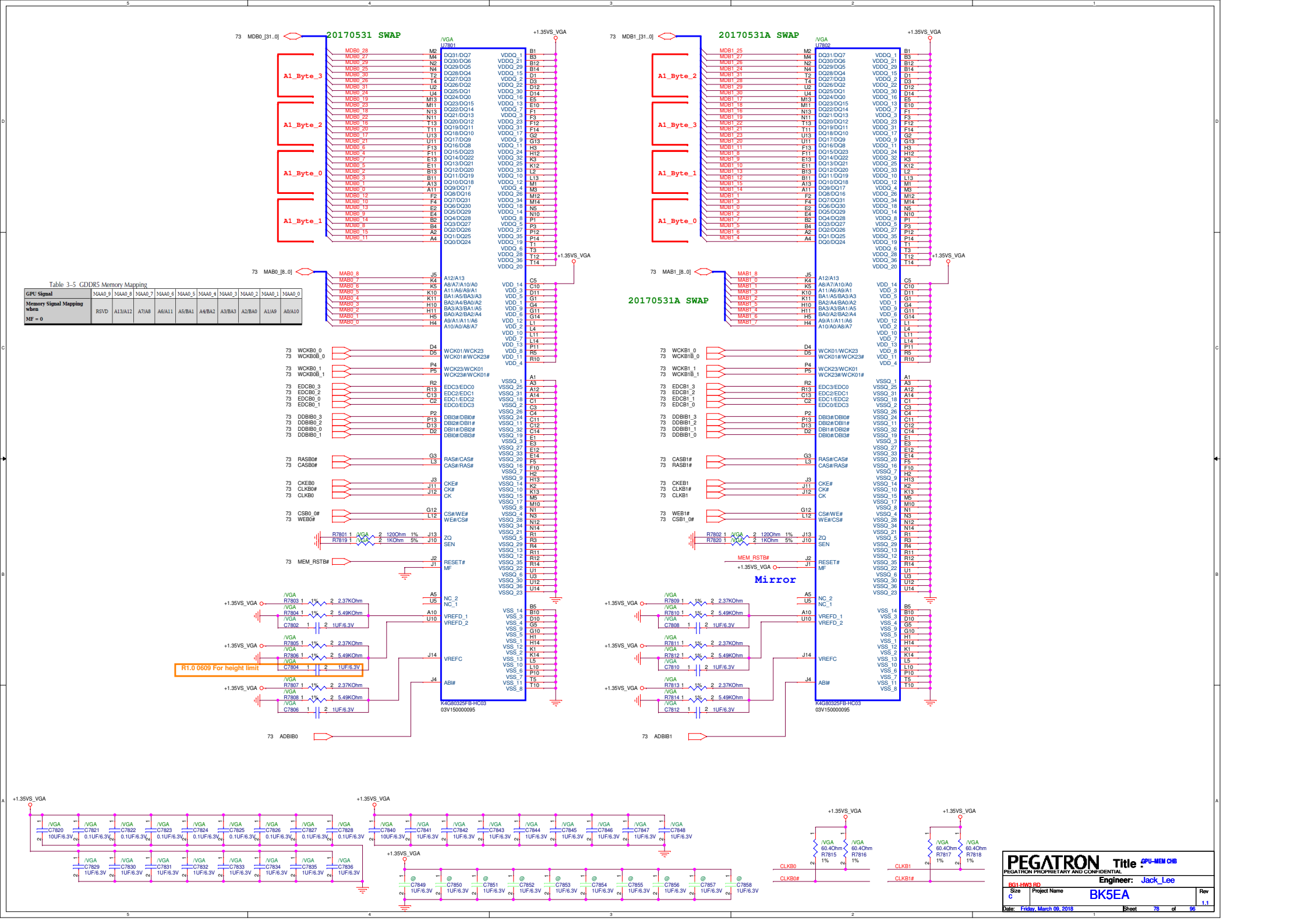


Table 3–5 GDDR5 Memory Mapping

GPU Signal	MAA0_9	MAA0_8	MAA0_7	MAA0_6	MAA0_5	MAA0_4	MAA0_3	MAA0_2	MAA0_1	MAA0_0
Memory Signal Mapping when MF = 0	RSVD	A13/A12	A7/A8	A6/A11	A5/BA1	A4/BA2	A3/BA3	A2/BA0	A1/A9	A0/A10

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: GPU-POWER FLOW

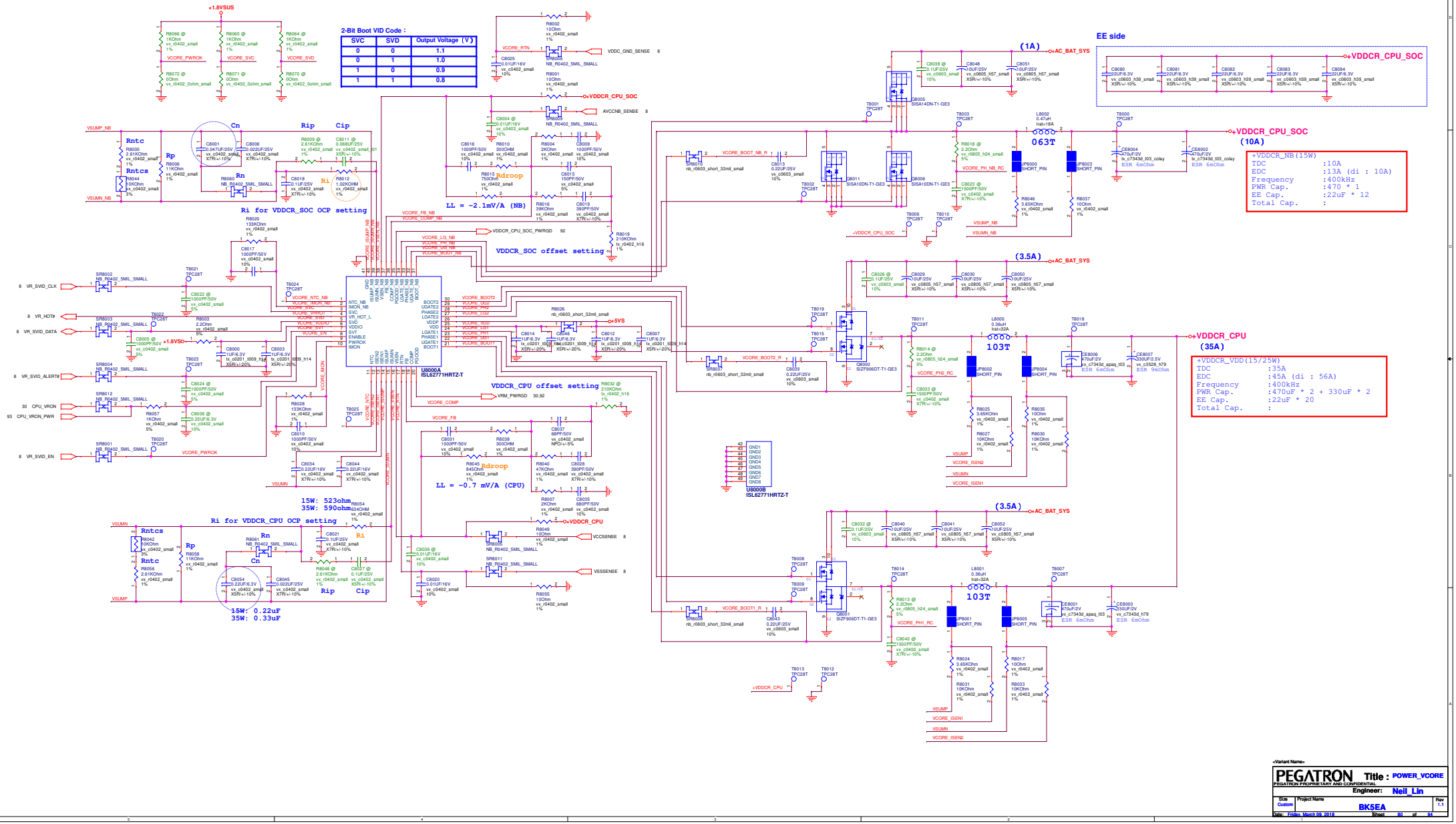
Engineer: Jack_Lee

BG1-HW3 RD

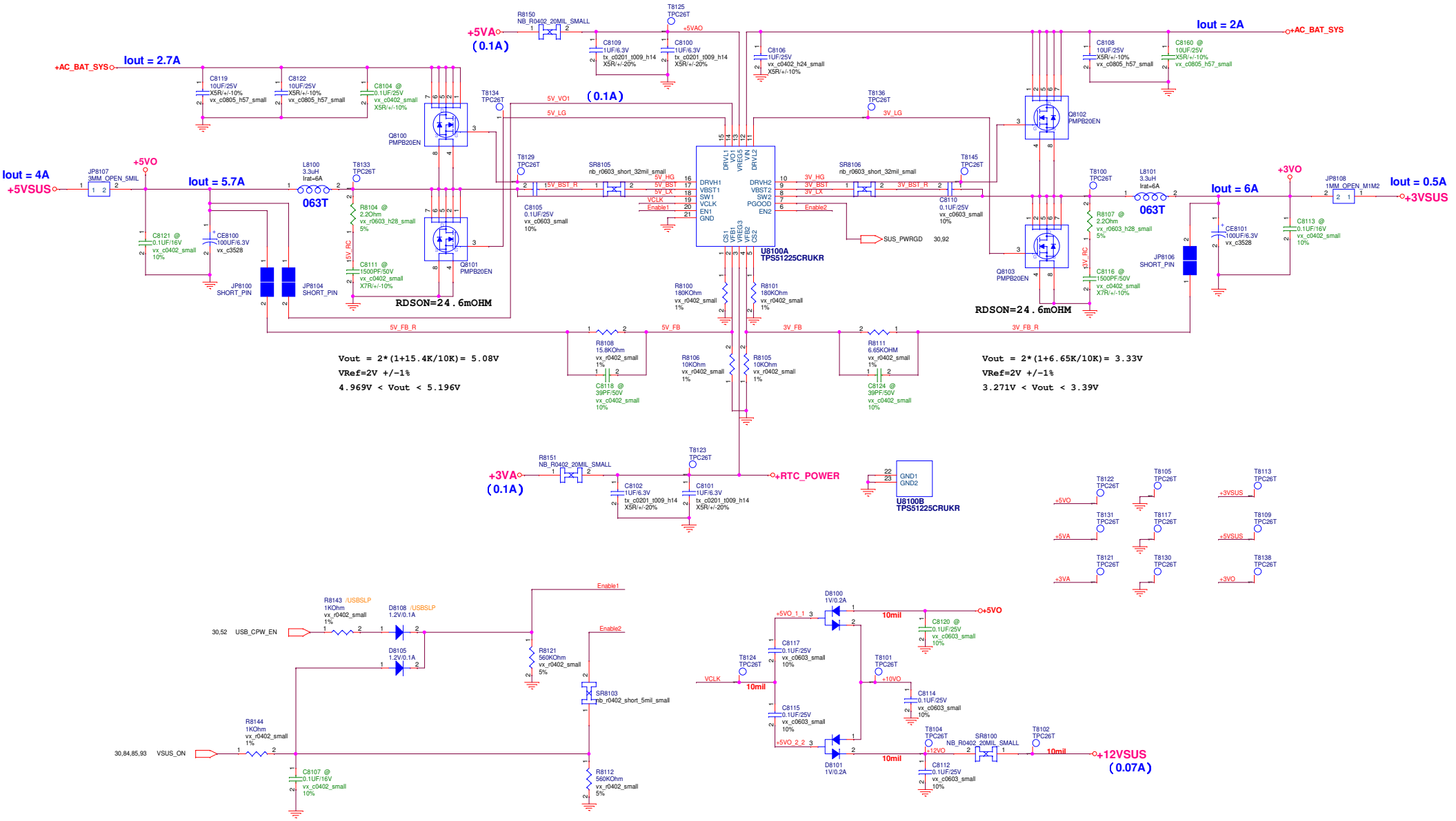
Size	Project Name	Rev
C	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 79 of 96

15W/25W VCORE POWER SUPPLY



5VO & 3VO POWER SUPPLY



<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

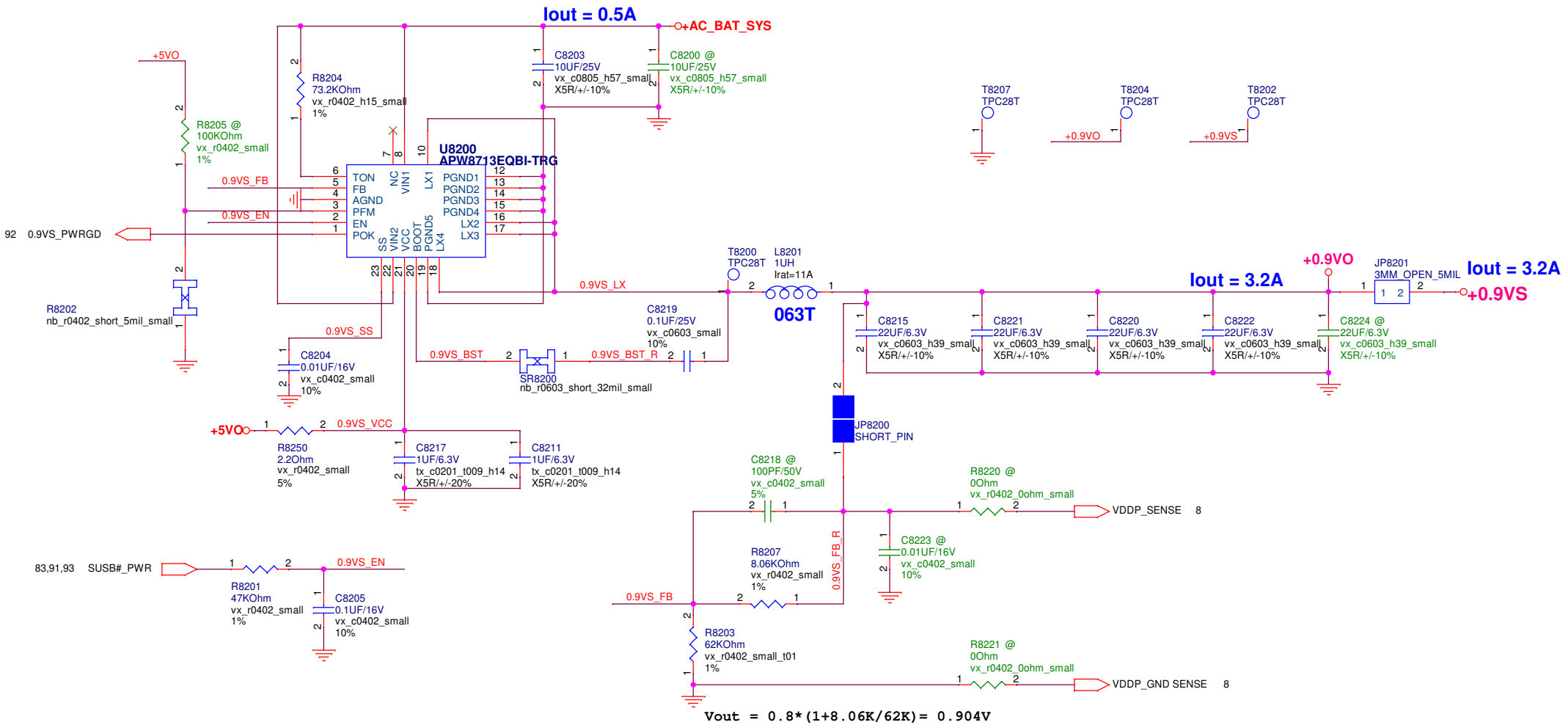
Title : POWER_SYSTEM

Engineer: Neil_Lin

Size	Project Name	Rev
Custom	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 61 of 94

0.9VS POWER SUPPLY



<Variant Name>

PEGATRON Title : +0.9VS

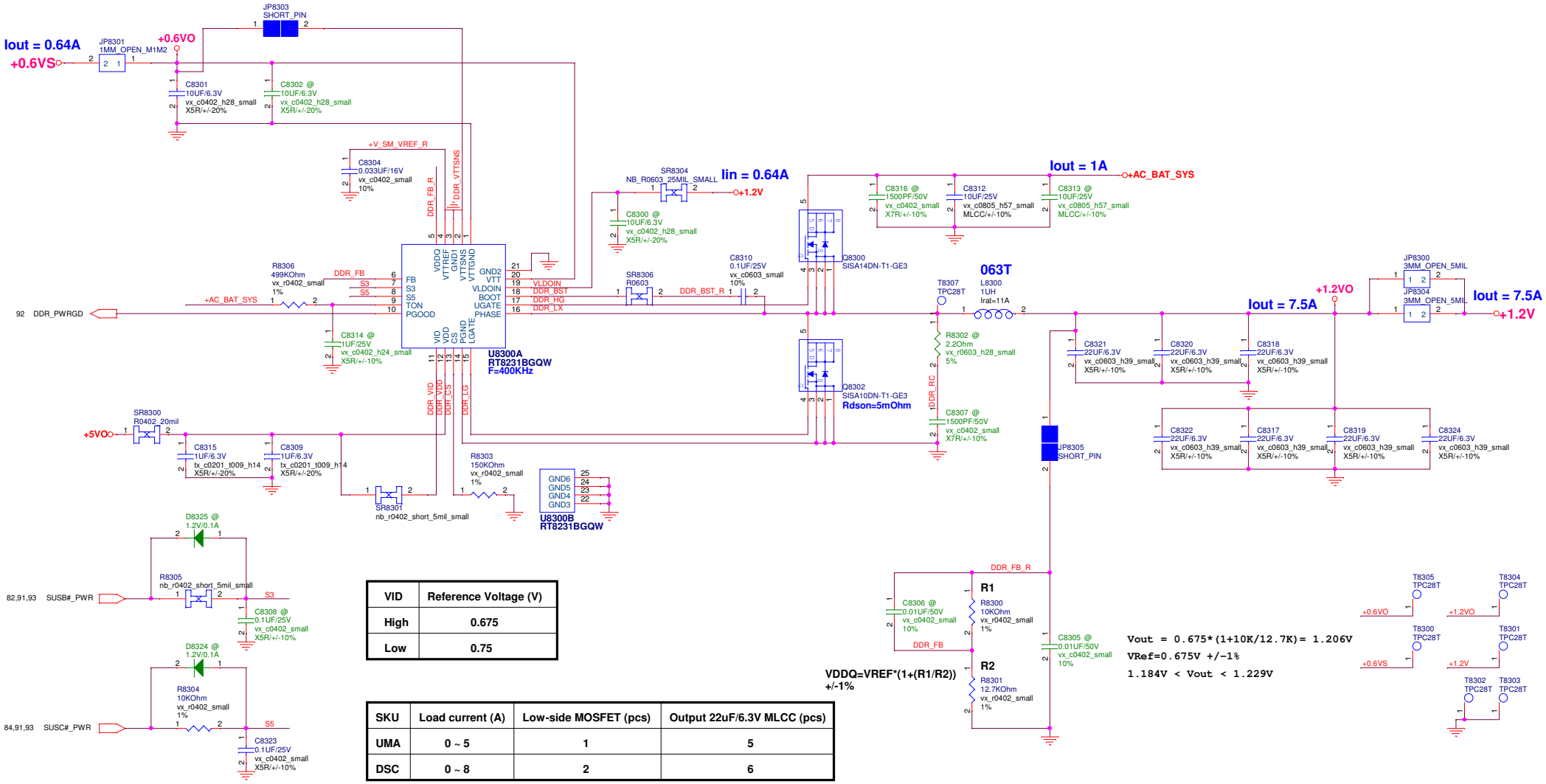
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Neil_Lin

Size	Project Name	Rev
Custom	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 82 of 94

DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	5
DSC	0 ~ 8	2	6

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

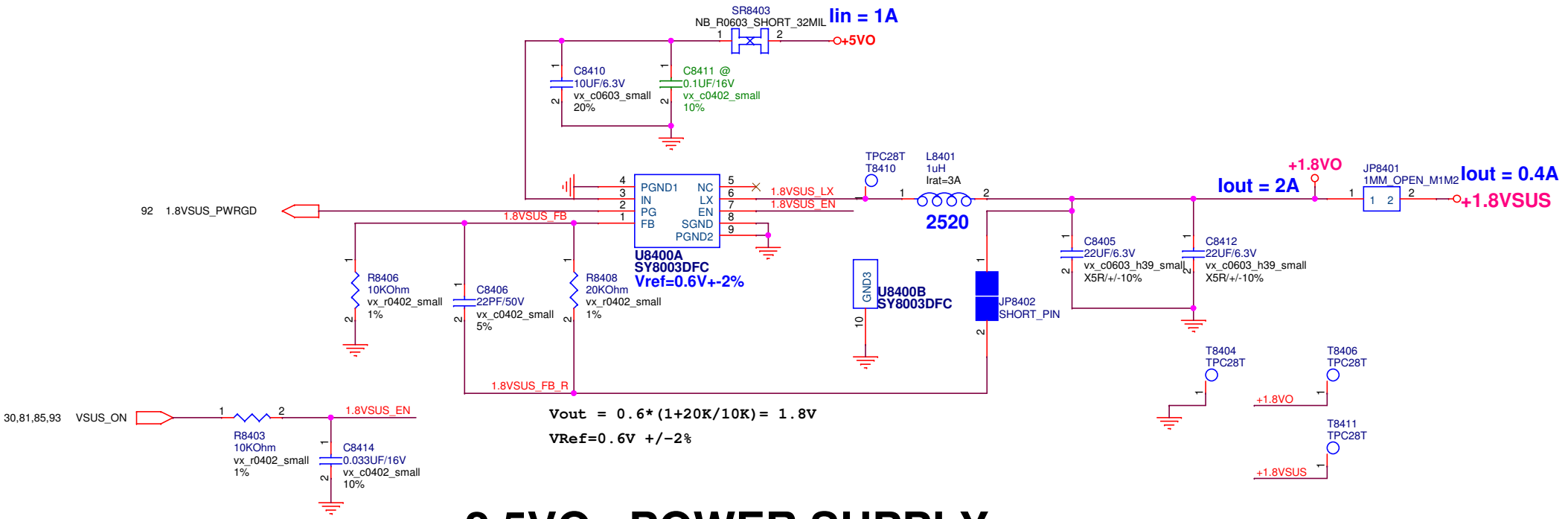
Title : POWER_DDR & VTT

Engineer: Neil_Lin

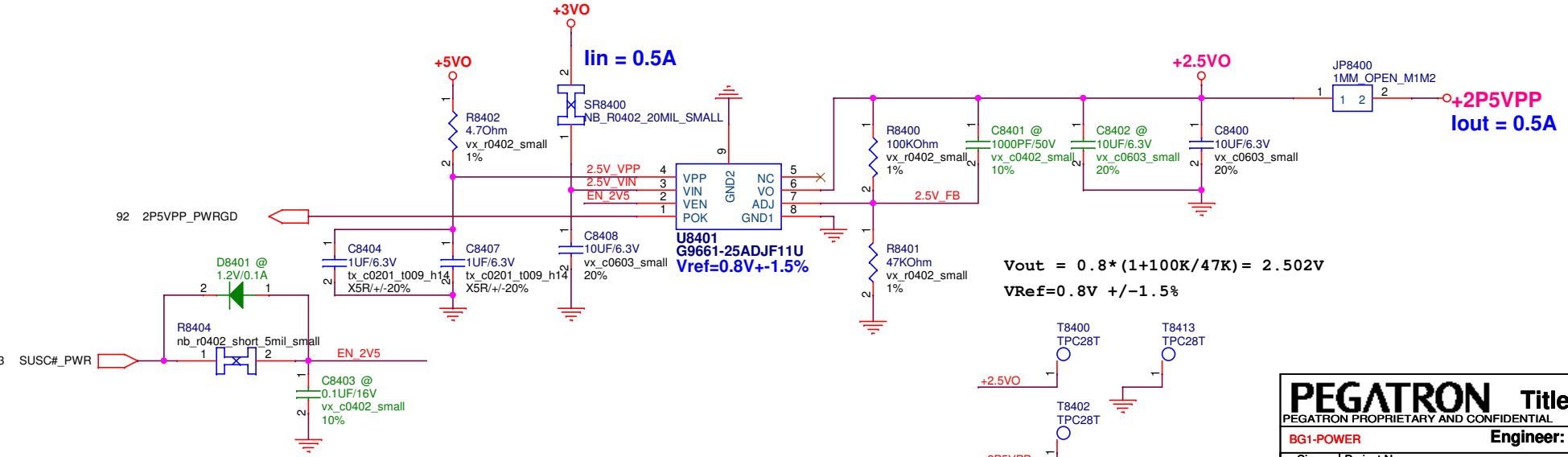
Size	Project Name	Rev
Custom	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 83 of 94

1.8VSUS POWER SUPPLY



2.5VO POWER SUPPLY



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_+1.8VSUS_2.5V

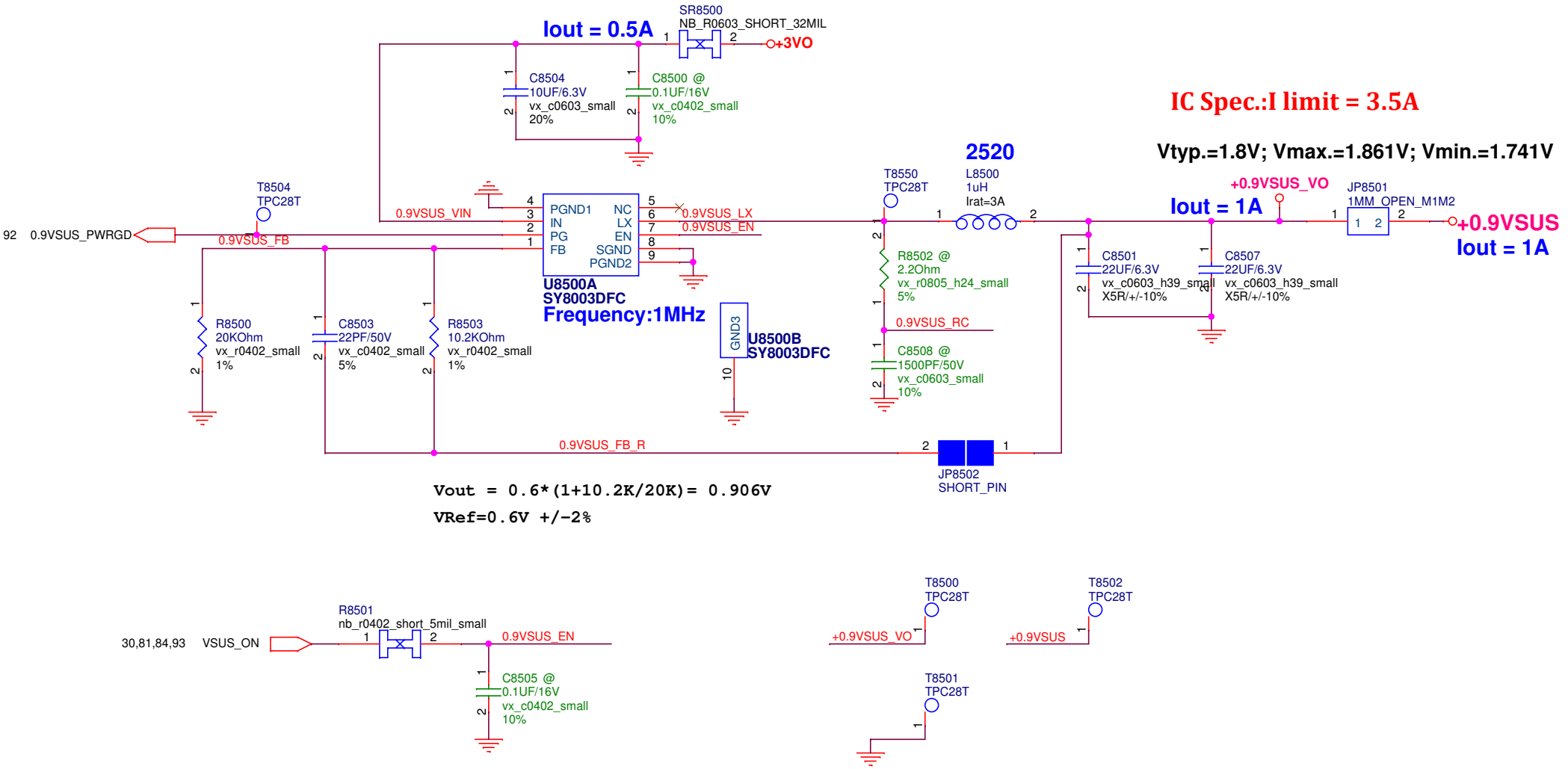
BG1-POWER

Engineer: Neil_Lin

Size	Project Name	Rev
Custom	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 84 of 94

0.9VSUS POWER SUPPLY



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

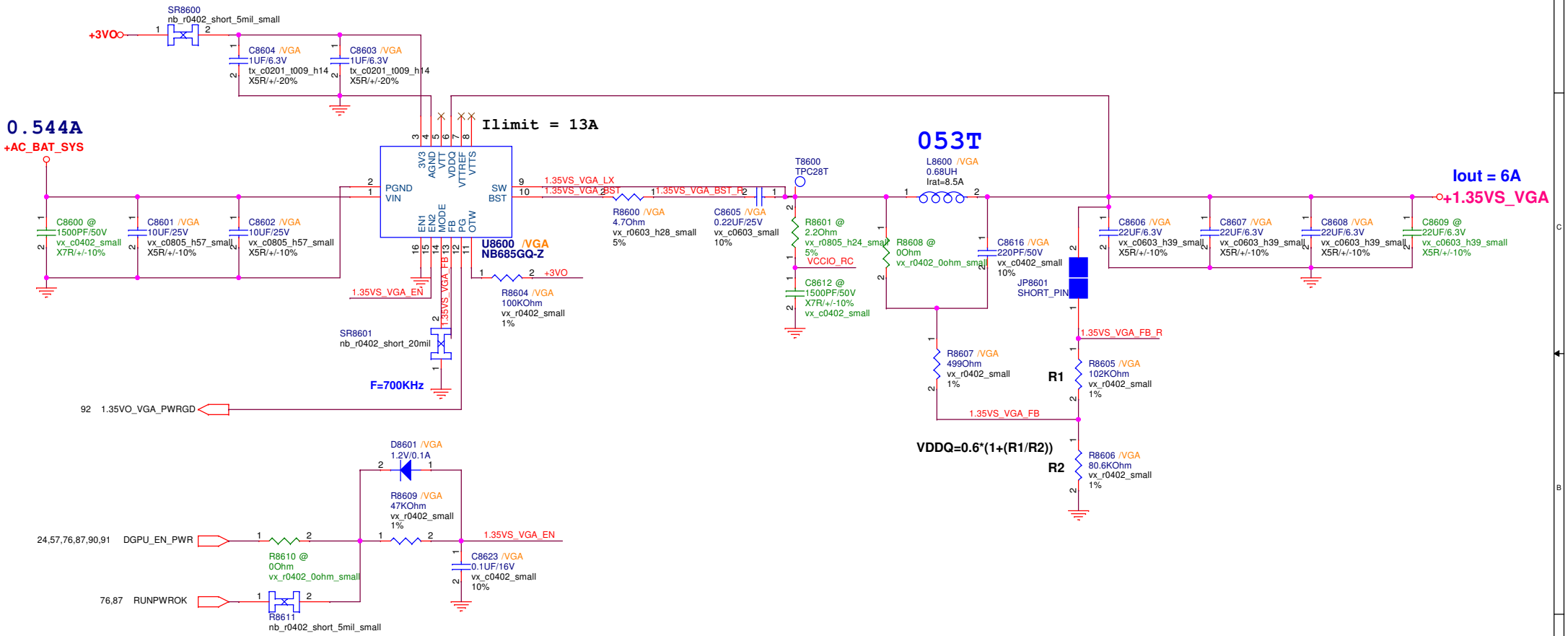
Title : POWER_0.9VSUS

Engineer: Neil_Lin

Size	Project Name	Rev
Custom	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 85 of 94

1.35VS_VGA POWER SUPPLY



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

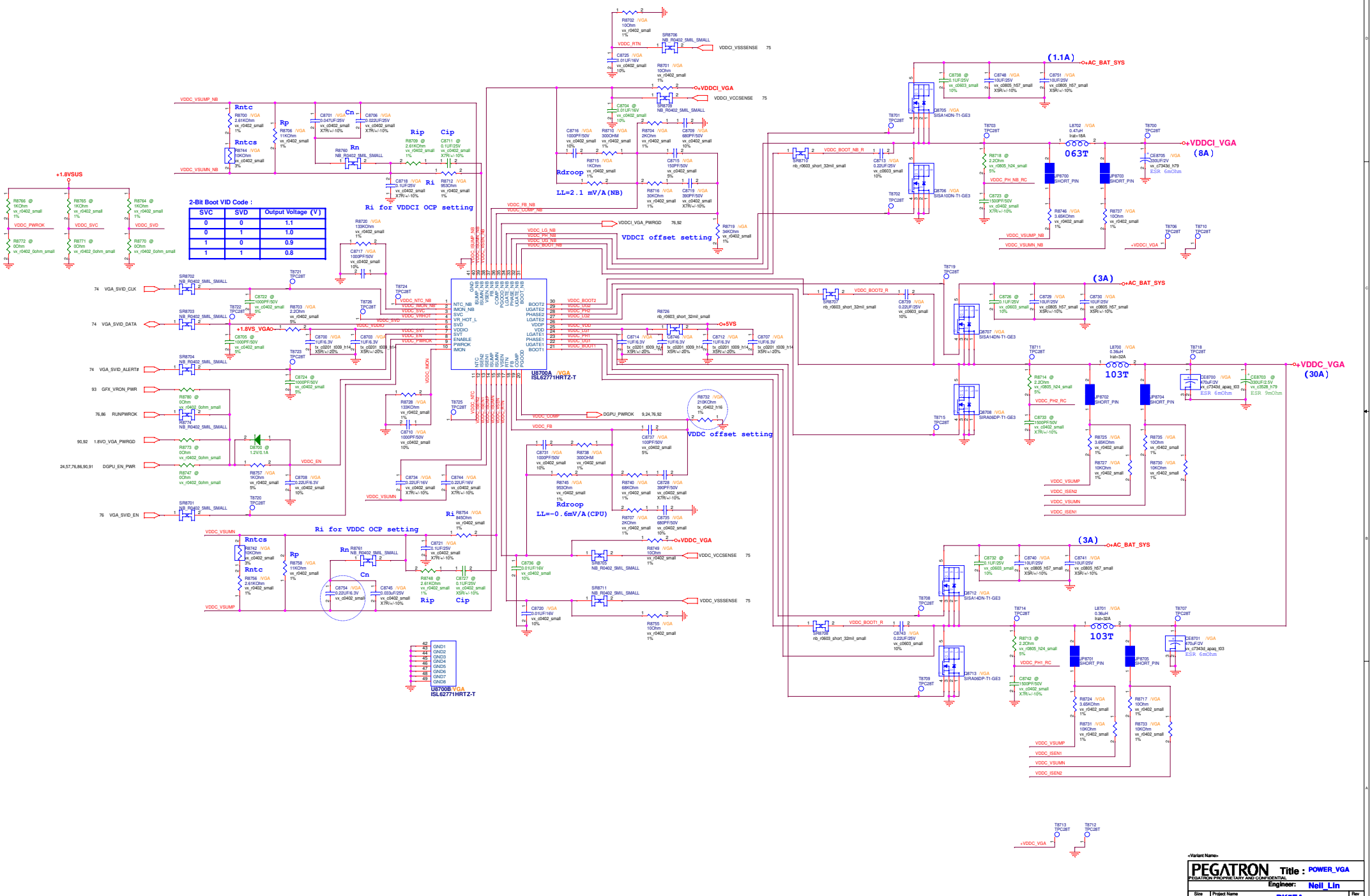
Title : POWER_1.35VS_VGA

Engineer: Neil_Lin

Size	Project Name	Rev
Custom	BK5EA	1.1

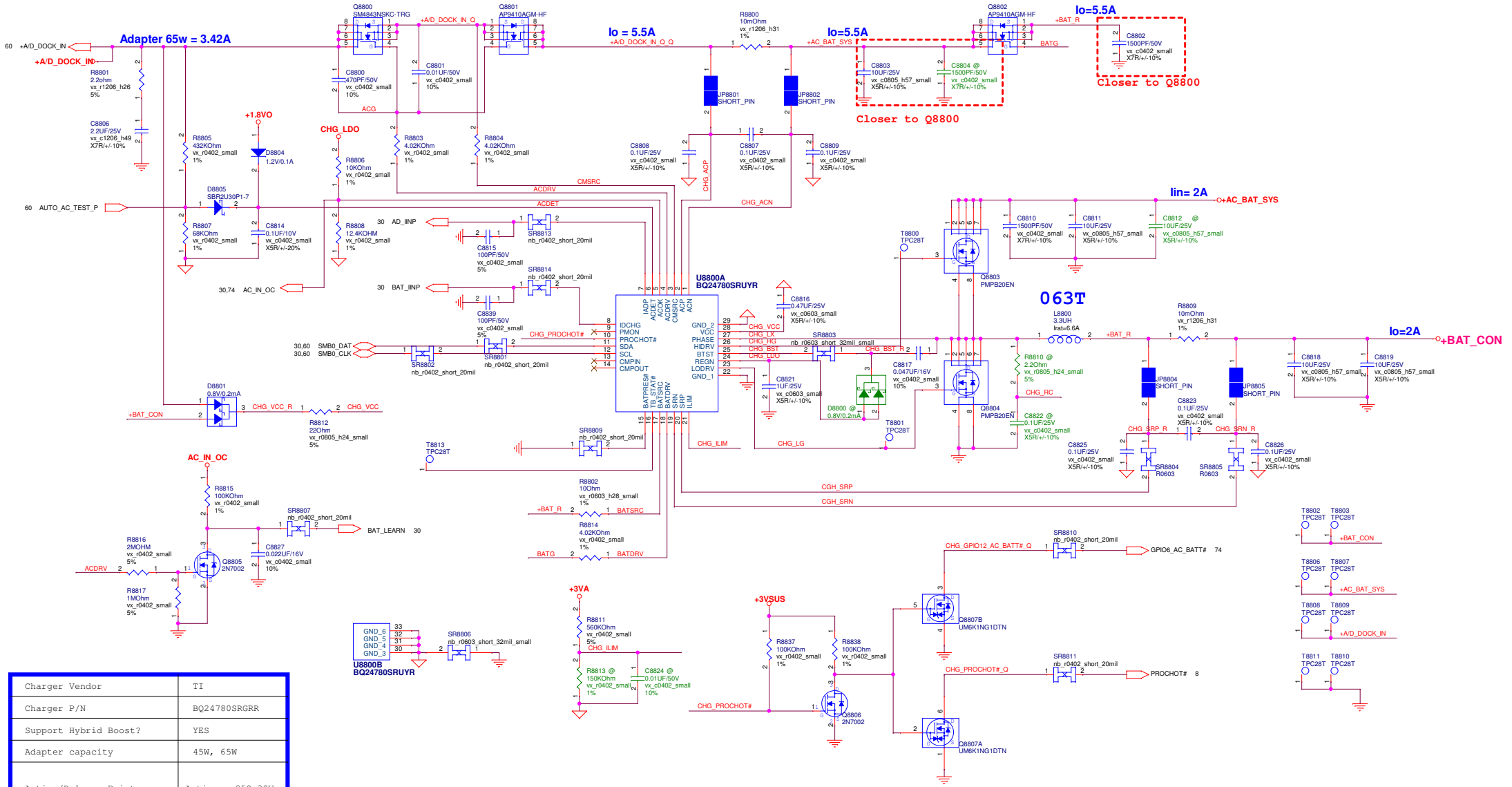
Date: Friday, March 09, 2018 Sheet 86 of 94

VGA POWER SUPPLY



<Variant Name>
PEGATRON Title : POWER_VGA
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Neil_Lin
Size: Custom | Project Name: BK5EA | Rev: 1.1
Date: Friday, March 09, 2018 | Sheet 87 of 94

BATTERY CHARGER



Charger Vendor	TI
Charger P/N	BQ24780SRGRR
Support Hybrid Boost?	YES
Adapter capacity	45W, 65W
Active/Release Point (Hybrid Boost)	Active - 250.38W Release - 217.62W
Enable condition Disable condition	RSOC>40% RSOC<30%

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

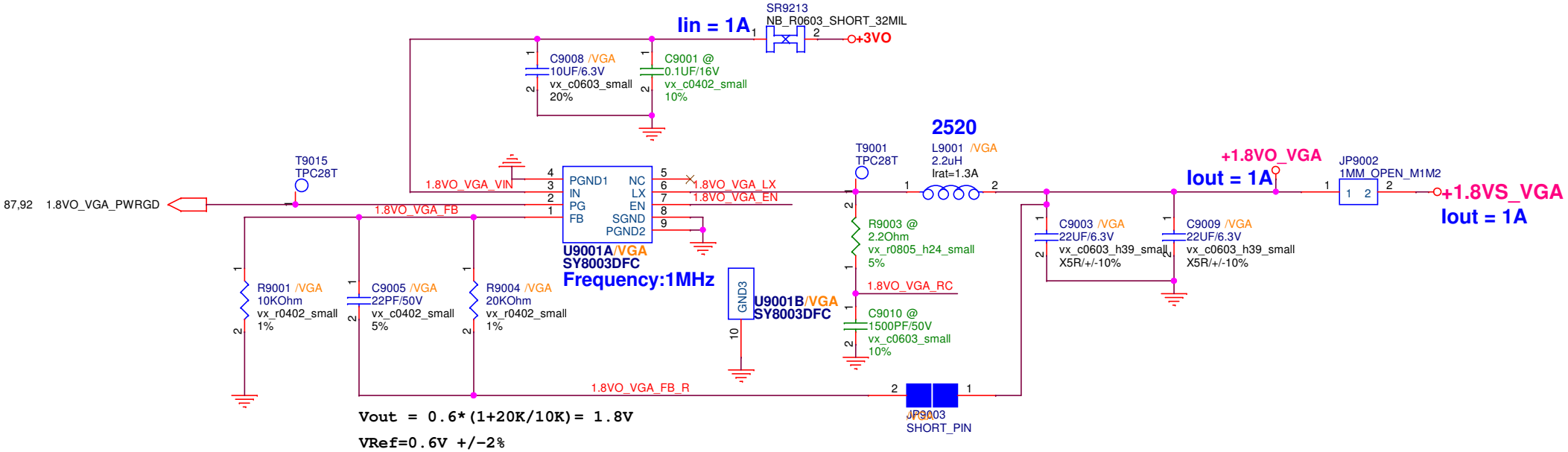
Title : POWER_CHARGER

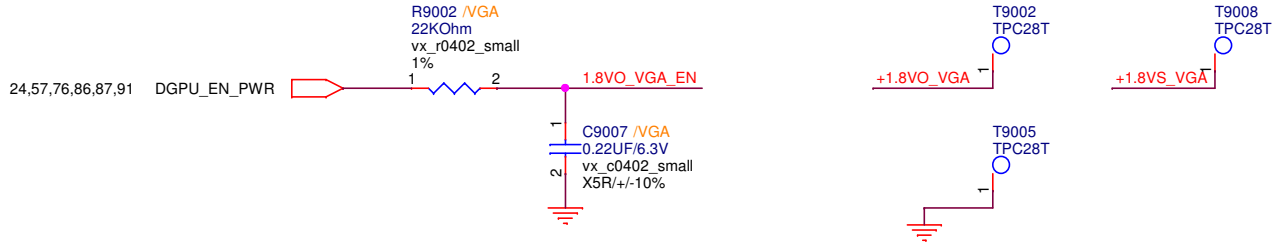
Engineer: Neil_Lin

Size	Project Name	Rev
Custom	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 88 of 94

+1.8VO_VGA POWER SUPPLY





<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

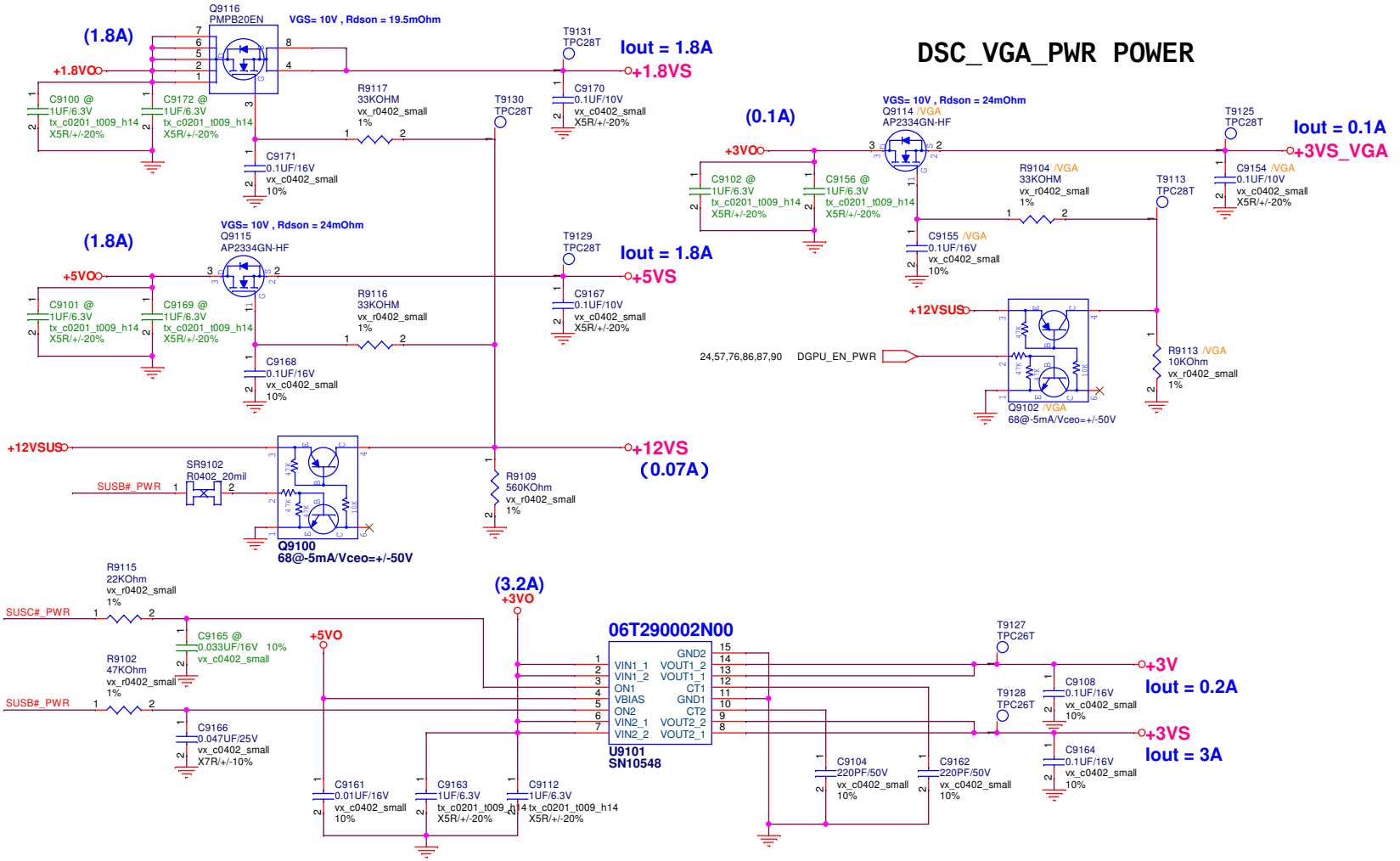
Title : POWER_1.8VS_VGA

Engineer: Neil_Lin

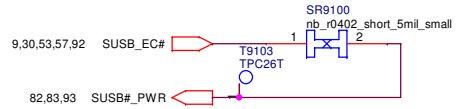
Size	Project Name	Rev
Custom	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 90 of 94

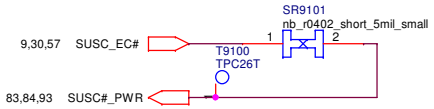
LOAD SWITCH



SUSB#_PWR POWER Control



SUSC#_PWR POWER Control



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_LOAD SWITCH

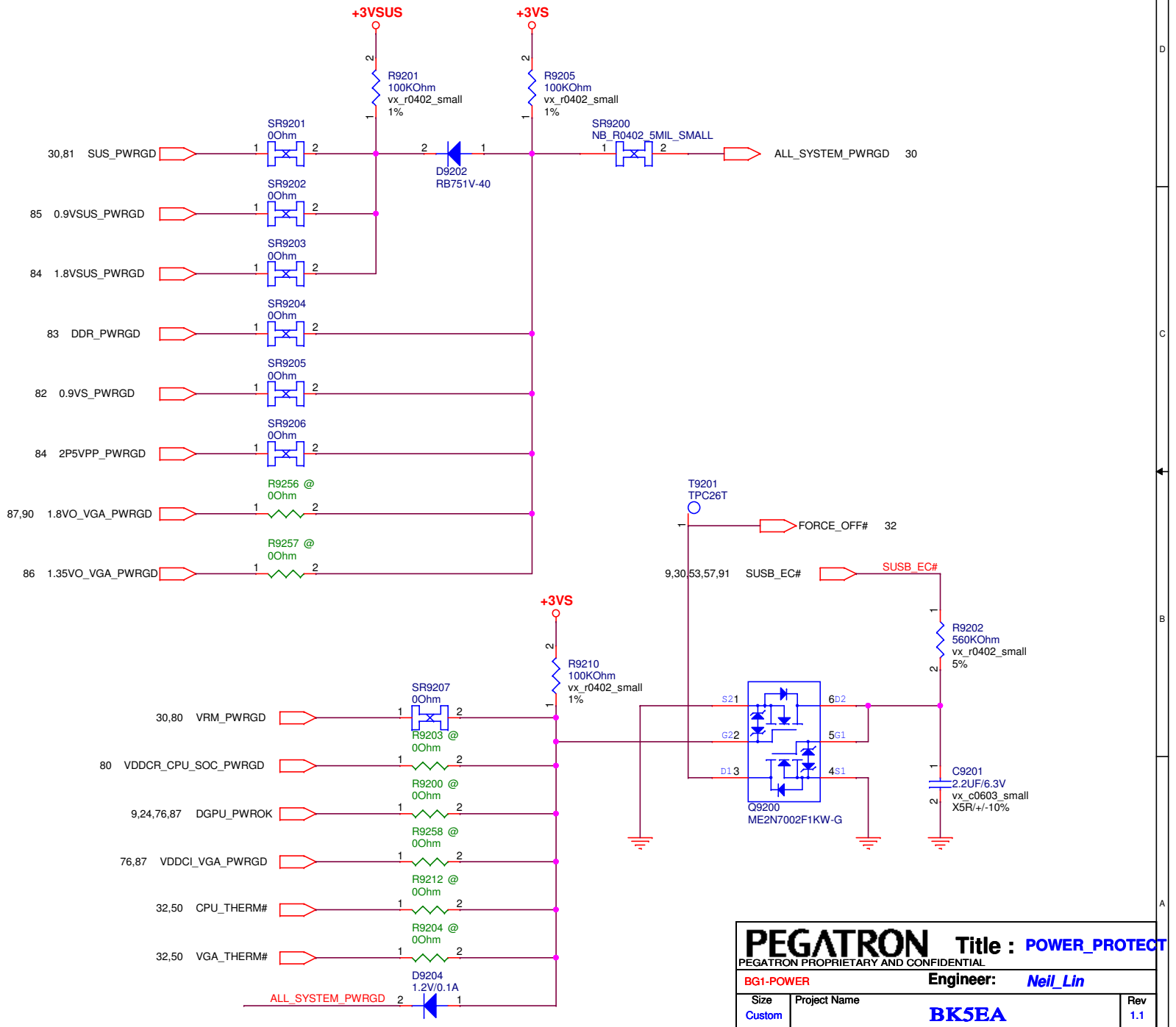
Engineer: Neil_Lin

BG1-POWER

Size	Project Name	Rev
Custom	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 91 of 94

POWER GOOD DETECTER



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_PROTECT

BG1-POWER

Engineer: Neil_Lin

Size	Project Name	Rev
Custom	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 92 of 94

+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,86,87,88

+BAT_CON → +BAT_CON 60,88

+RTC_POWER → +RTC_POWER 81

+5VA → +5VA 64,81

+3VA → +3VA 24,30,31,36,53,57,65,67,81,88

+5VO → +5VO 81,82,83,84,91

+3VO → +3VO 81,84,85,86,90,91

+2.5VO → +2.5VO 84

+1.8VO → +1.8VO 84,88,91

+1.8VO_VGA → +1.8VO_VGA 90

+1.2VO → +1.2VO 83

+0.9VO → +0.9VO 82

+0.9VSUS_VO → +0.9VSUS_VO 85

+0.6VO → +0.6VO 83

+12VSUS → +12VSUS 28,81,91

+5VSUS → +5VSUS 11,41,52,64,81

+3VSUS → +3VSUS 9,11,12,23,24,30,31,41,42,51,53,60,62,65,67,81,88,92

+1.8VSUS → +1.8VSUS 8,9,11,12,24,28,80,84,87

+0.9VSUS → +0.9VSUS 11,85

+12VS → +12VS 31,57,91

+5VS → +5VS 13,31,36,45,48,50,51,57,69,80,87,91

+3VS → +3VS 8,9,11,13,24,30,31,32,36,41,44,45,50,51,53,57,60,62,64,69,91,92

+1.8VS → +1.8VS 8,11,12,24,28,36,57,80,91

+0.6VS → +0.6VS 15,57,83

+3V → +3V 31,45,57,65,67,91

+1.2V → +1.2V 7,11,15,16,17,19,57,83

+2P5VPP → +2P5VPP 16,17,57,84

+1.8VS_VGA → +1.8VS_VGA 57,74,75,76,87,90

+1.35VS_VGA → +1.35VS_VGA 57,72,73,75,77,78,86

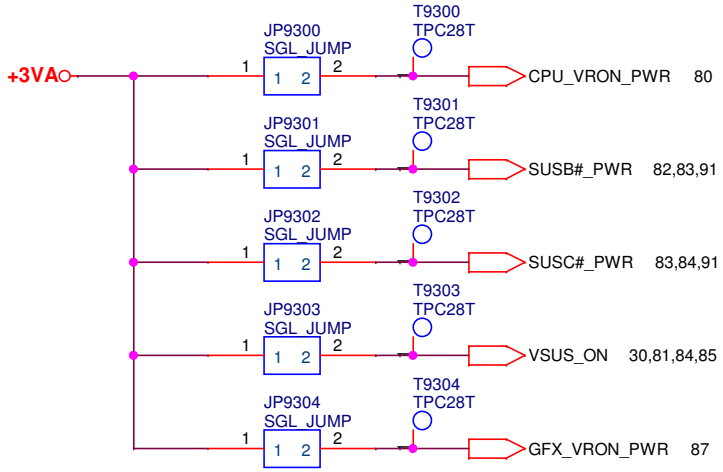
+VDDCI_VGA → +VDDCI_VGA 57,75,87

+VDDC_VGA → +VDDC_VGA 57,75,87

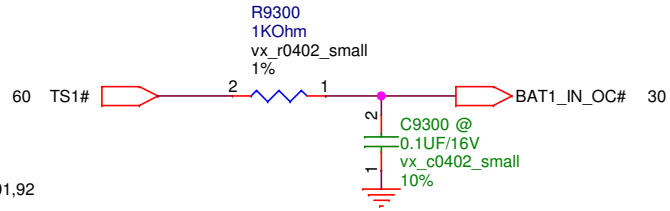
+VDDCR_CPU_SOC → +VDDCR_CPU_SOC 11,80

+VDDCR_CPU → +VDDCR_CPU 11,80

FOR POWER TEST



BATTERY IN DETECT



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

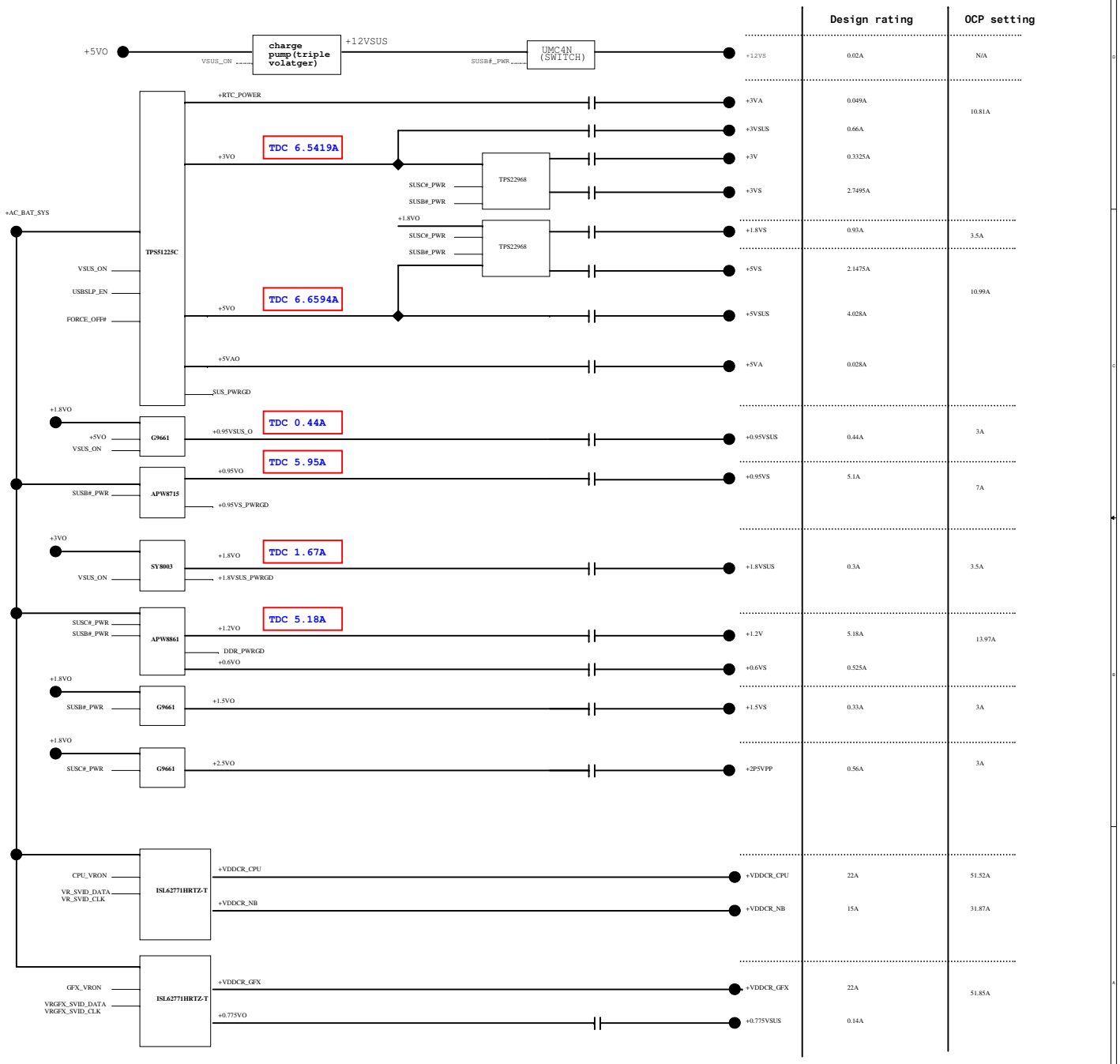
Title : POWER_SIGNAL

BG1-POWER

Engineer: Neil_Lin

Size	Project Name	Rev
Custom	BK5EA	1.1

Date: Friday, March 09, 2018 Sheet 93 of 94



PEGATRON
Title : POWER_SIGNAL
BG1-POWER
Engineer: Neil_Lin
Size: Custom
Project Name: BK5EA
Rev: 1.1
Date: Friday, March 09, 2018
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