LCFC Confidential

EG521/EG522 MB Schematics Document

Kabylake-U42 with DDR4 + Nvidia N17S-G1

2017-04-20

REV:0.2

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	Cover Page	
Size: Custom	Document Number: EG521	Rev: 0.2
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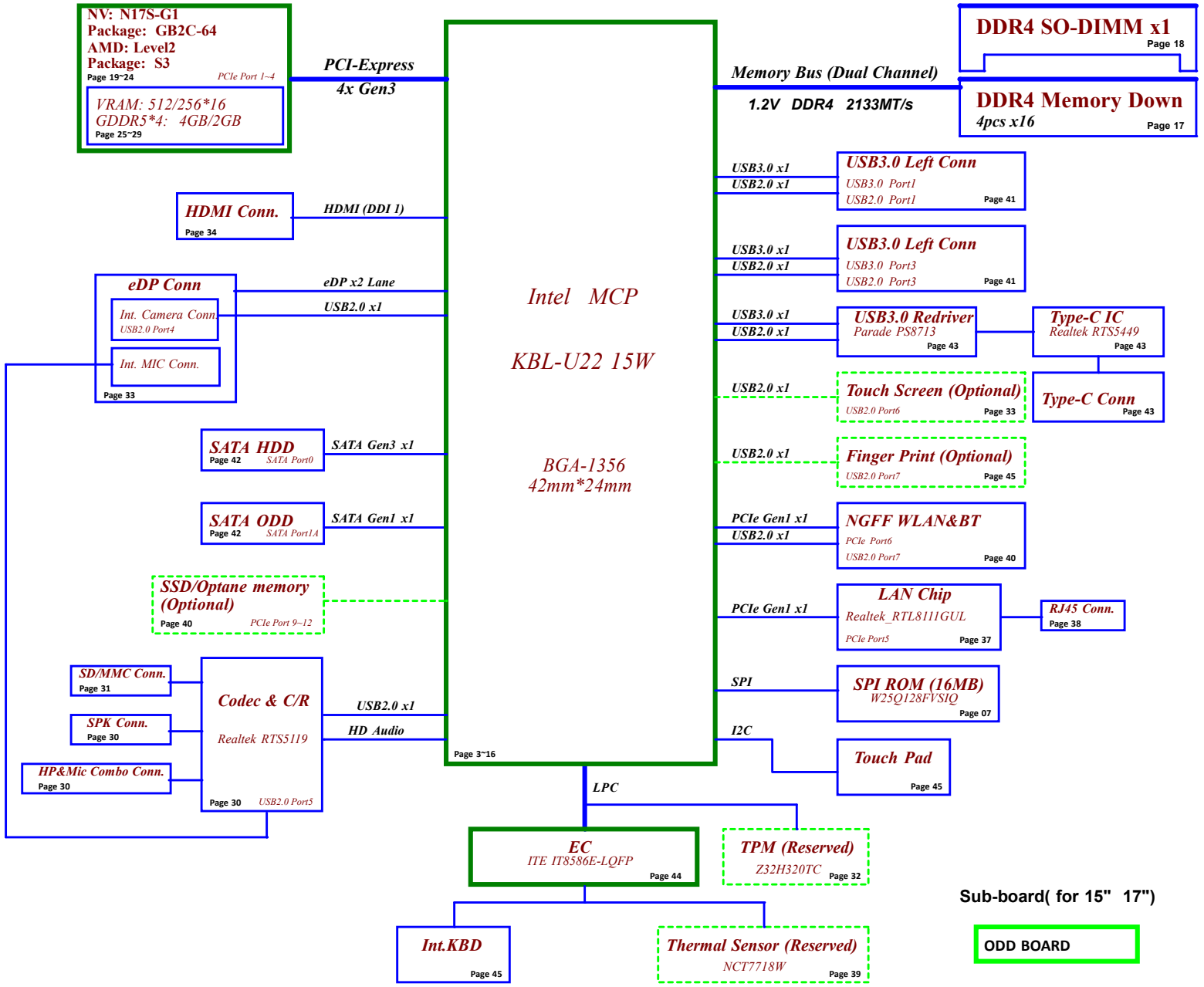

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Block Diagram**

Size	Document Number	Rev
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE / SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT		Function
USB3.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	Finger Print
	5	Cardreader
	6	Touch Panel
	7	Bluetooth
	8	Camera
	9	NC
	10	NC
PCIE	1~4 X4 PCIE	DGPU
	5	LAN
	6	WLAN
	7	SATA HDD
	8	SATA ODD
	9~12 X4 PCIE	Optane Memory
SATA	0	HDD
	1A	ODD
	1B	used as PCIE
	2	used as PCIE

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
14or15@	For 14" or 15" part
14or17@	For 14" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
NTS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
PX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek_SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAN rank part
DUALRANK@	For dual VRAN rank part
TS@	For touch screen part
TPM@	For TPM part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

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Title: **Notes List**

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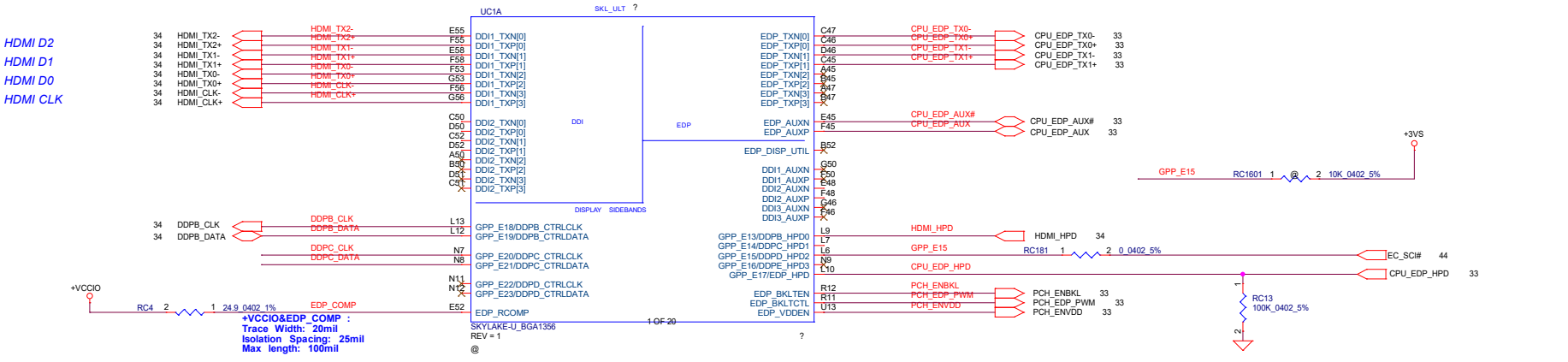
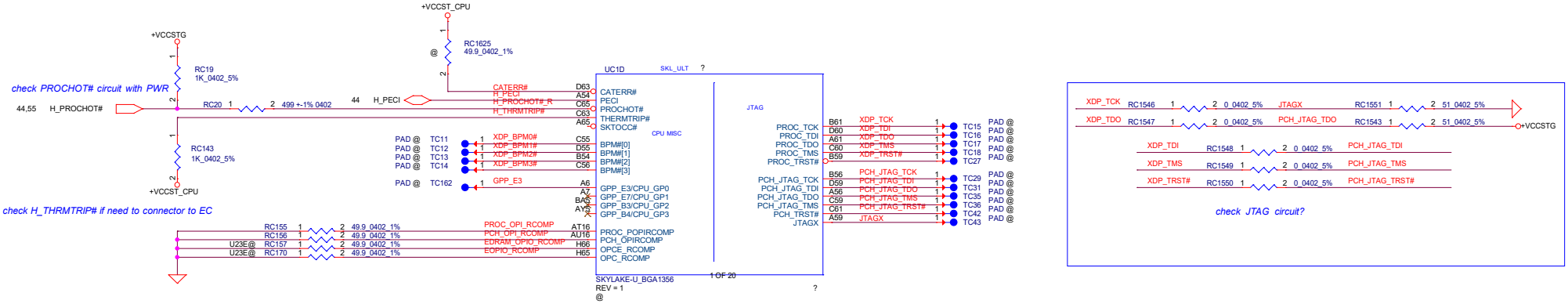
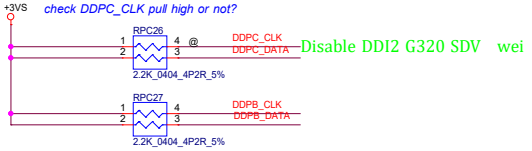




DDP*_CTRLDATA strapping sampled on the rising edge of PWROK

Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC



Disable DDI2 G320 SDV wei

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Title: **MCP (DDI,EDP)**

Size	Document Number	Rev
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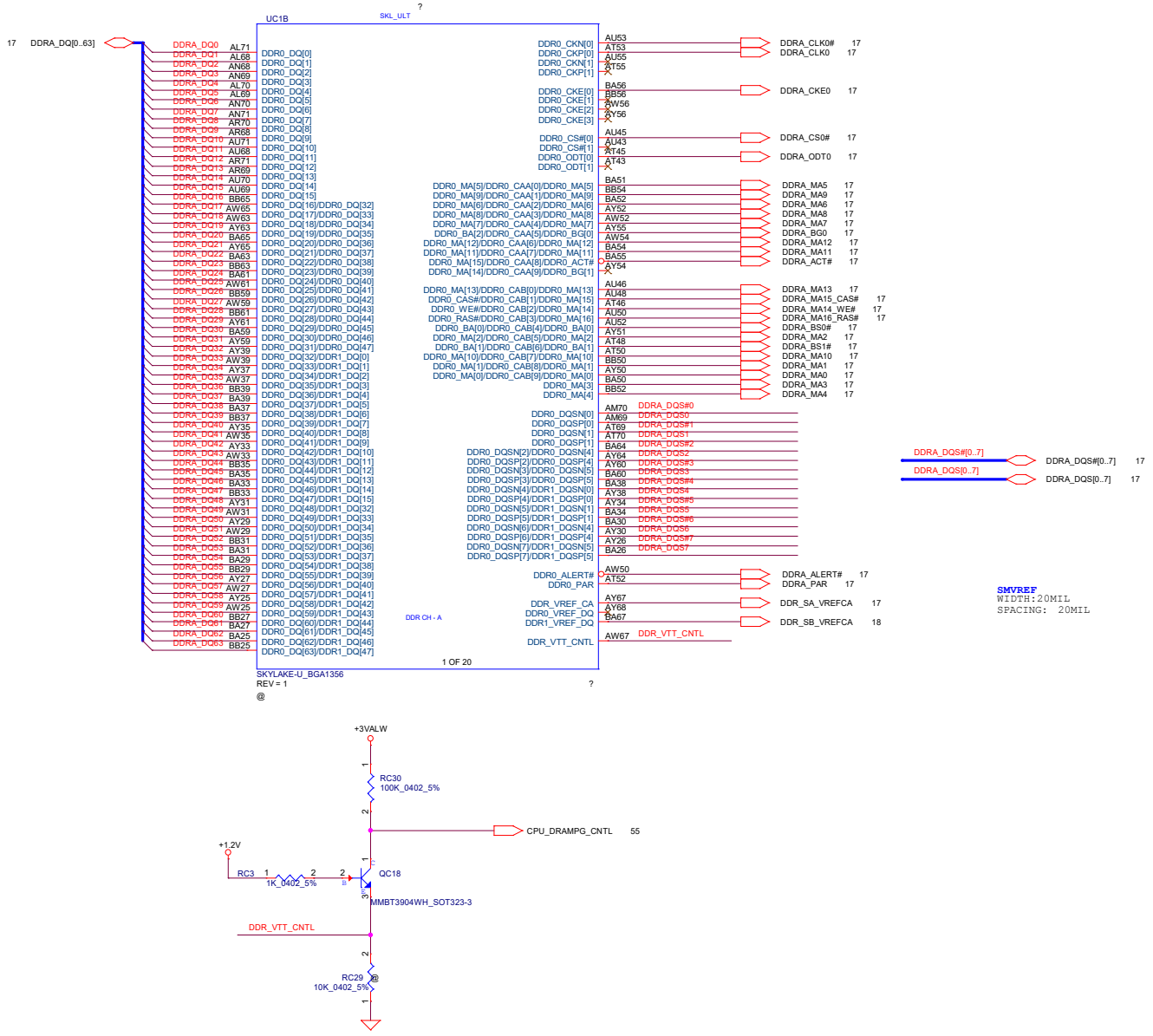

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (DDR4)**

Size	Document Number	Rev
Custom	EG521	0.2
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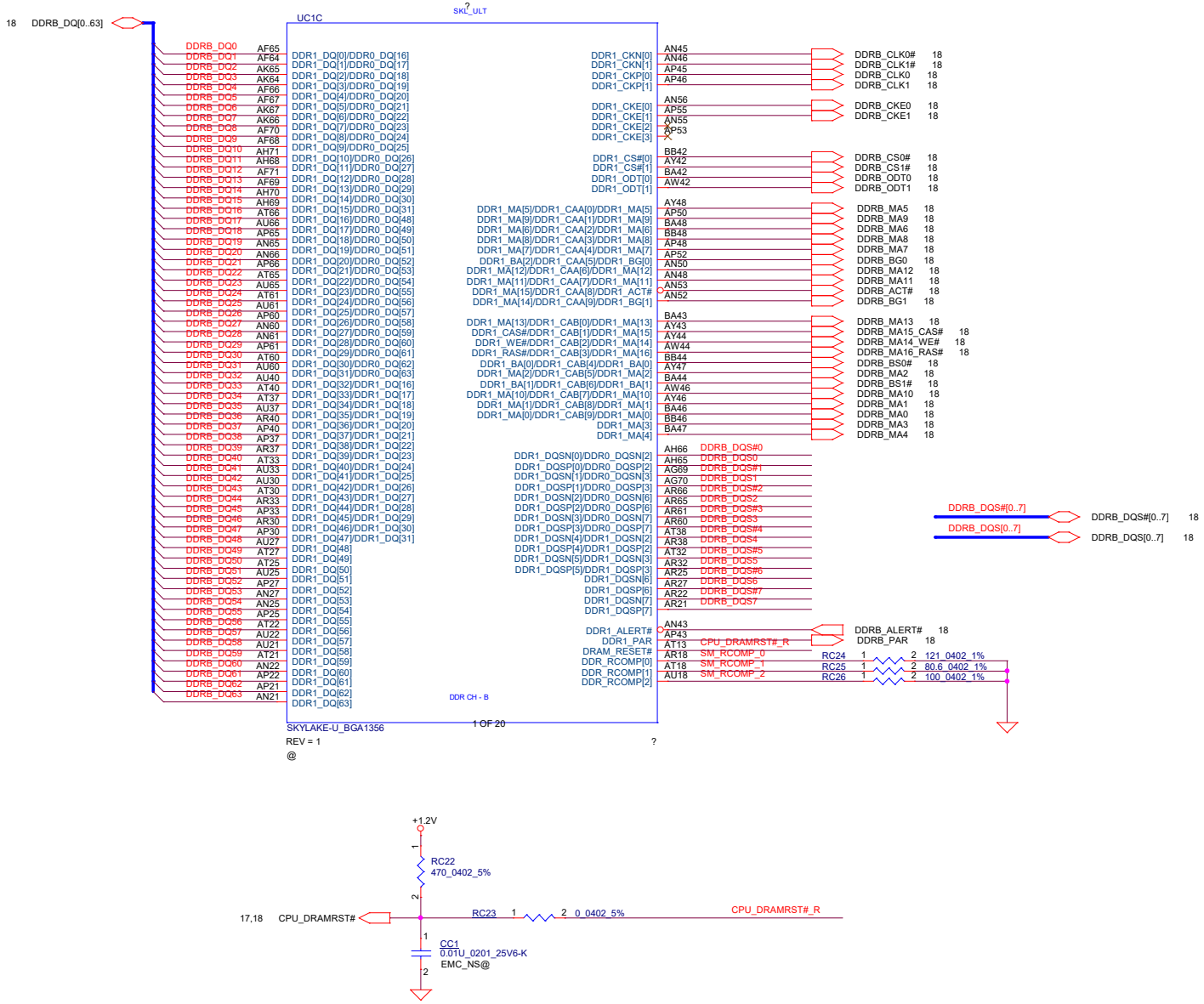

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Title: MCP (DDR4)

Size	Document Number	Rev
Custom	EG521	0.2

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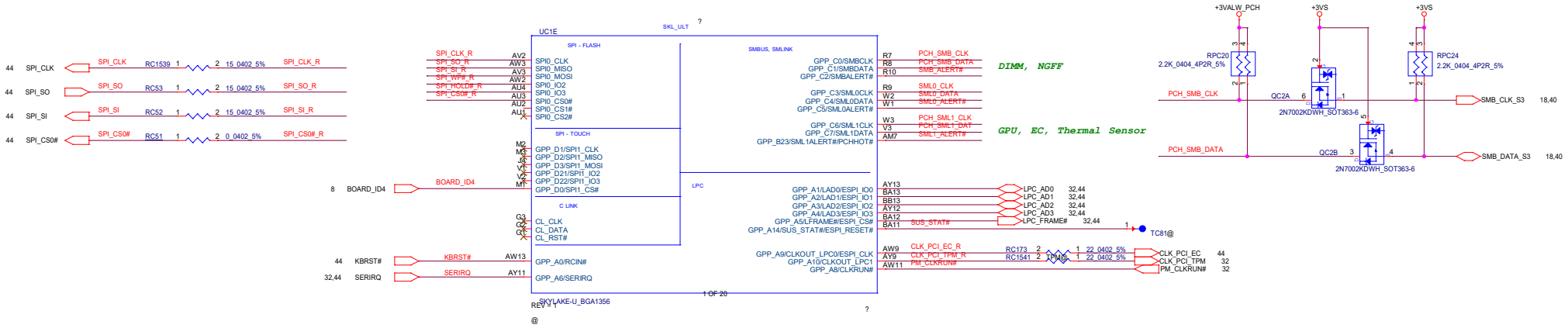

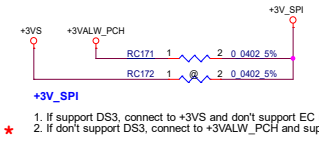

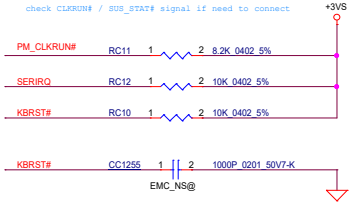

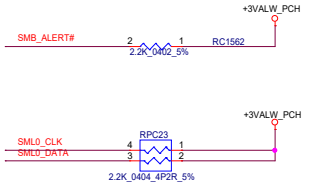

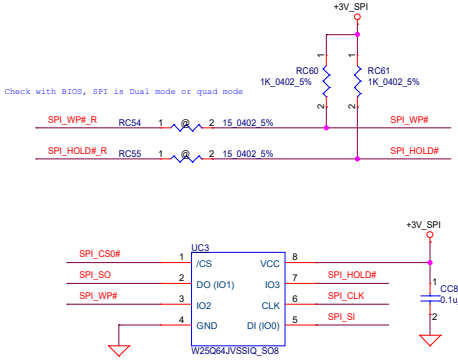

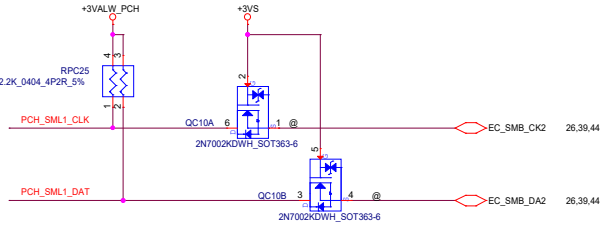

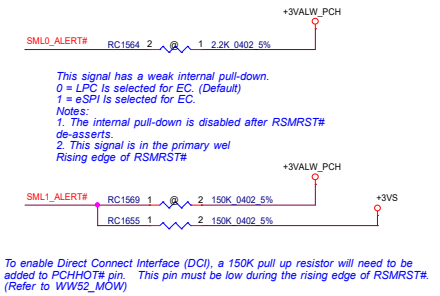

Security Classification	LC Future Center Secret Data		
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Title	MCP (MISC,JTAG,SPI,LPC,SMB,EC)	
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@DIS For NV and AMD GPU SKU

+3VS

RC1559 2 DIS@ 1 10K_0402_5% PXS_PWREN_R
RC1641 1 @ 2 10K_0402_5% PXS_RST#_R
Reserve for GPU sequence
RC1557 1 DIS@ 2 10K_0402_5% PXS_RST#_R
CC1259 1 DIS@ 2 0.01U_0201_10V6K PXS_RST#
DGPU_PWROK

1K_0402_5% 2 DIS@ 1 RC7 → PXS_PWREN 23
0_0402_5% 2 DIS@ 1 RC8 → PXS_RST# 26
DGPU_PWROK → DGPU_PWROK 23,58

@OPT&GC6 Only for NV GPU SKU

+3VS

RC1629 1 GC6@ 2 10K_0402_5% FB_GC6_EN_R → FB_GC6_EN_R 26
RC1630 1 GC6@ 2 10K_0402_5% GPU_EVENT# → GPU_EVENT# 26
RC1637 1 @ 2 10K_0402_5% FB_GC6_EN_R
RC1638 1 @ 2 10K_0402_5% GPU_EVENT#

@UMA SKU

RC1558 1 UMA@ 2 10K_0402_5% DGPU_PWROK

+3VS

RC1615 2 @ 10K_0402_5%
RC1613 2 15@ 10K_0402_5%
RC1611 2 @ 10K_0402_5%
RC1609 2 DIS@ 10K_0402_5%
RC1608 2 PX@ 1 10K_0402_5%
RC1606 2 @ 10K_0402_5%

BOARD_ID0
BOARD_ID1
BOARD_ID2
BOARD_ID3
BOARD_ID4
BOARD_ID5

9 BOARD_ID2
7 BOARD_ID4

RC1616 2 @ 10K_0402_5%
RC1614 2 14@ 10K_0402_5%
RC1612 2 @ 10K_0402_5%
RC1610 2 UMA@ 10K_0402_5%
RC1607 2 OPT@ 1 10K_0402_5%
RC123 2 @ 10K_0402_5%

Board ID	Description		Stuff R
Board_ID[0:1]	00	14"	RC1616 RC1614
	01	15"	RC1616 RC1613
	10	17"	RC1615 RC1614
	11	Reserved	RC1615 RC1613
Board_ID2	0	Reserved	RC1612
	1	Reserved	RC1611
Board_ID3	0	UMA	RC1610
	1	DIS	RC1609
Board_ID4	0	NV GPU	RC1607
	1	AMD GPU	RC1608
Board_ID5	0	Reserved	RC123
	1	Reserved	RC1606

+3VS

RPC28 1 2 4 3 2.2K_0404_4P2R_5%
PCH_I2C_SDA0
PCH_I2C_SCL0
RC1658 2 1 10K_0402_5% PCH_TP_INT#

10/25 SIT For I2C T/P Function wei

+3VS

RC1595 2 @ 1 10K_0402_5% PCH_CMOS_ON#
RC1596 2 1 10K_0402_5% PCH_WLAN_OFF#
RC1597 2 1 10K_0402_5% PCH_BT_OFF#
double check if need the pull up resisor

+3VALW_PCH +3VS

RC1600 1 @ 2 1K_0402_5%
RC47 1 @ 2 1K_0402_5% HDA_SDOUT

★ HDA_SDO This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.

UC1F — SKL_ULT — LPSS / ISH — SKYLAKE-U_BGA1356 REV = 1 — 1 OF 20

LPSS:
AN8 GPP_B15/GSPI0_CS#
AP7 GPP_B16/GSPI0_CLK
AP8 GPP_B17/GSPI0_MISO
AR7 GPP_B18/GSPI0_MOSI
AM5 GPP_B19/GSPI1_CS#
AN7 GPP_B20/GSPI1_CLK
AP5 GPP_B21/GSPI1_MISO
AN5 GPP_B22/GSPI1_MOSI
AB1 GPP_C8/UART0_RXD
AB2 GPP_C9/UART0_TXD
W4 GPP_C10/UART0_RTS#
AB3 GPP_C11/UART0_CTS#
AD1 GPP_C20/UART2_RXD
AD2 GPP_C21/UART2_TXD
AD3 GPP_C22/UART2_RTS#
AD4 GPP_C23/UART2_CTS#
U7 GPP_C16/I2C0_SDA
U6 GPP_C17/I2C0_SCL
U8 GPP_C18/I2C1_SDA
U9 GPP_C19/I2C1_SCL
AH9 GPP_F4/I2C2_SDA
AH10 GPP_F5/I2C2_SCL
AH11 GPP_F6/I2C3_SDA
AH12 GPP_F7/I2C3_SCL
AF11 GPP_F8/I2C4_SDA
AF12 GPP_F9/I2C4_SCL

ISH:
P2 GPP_D9
P3 GPP_D10
P4 GPP_D11
P1 GPP_D12
M4 GPP_D5/ISH_I2C0_SDA
N3 GPP_D6/ISH_I2C0_SCL
N1 GPP_D7/ISH_I2C1_SDA
N2 GPP_D8/ISH_I2C1_SCL
AD11 GPP_F10/I2C5_SDA/ISH_I2C2_SDA
AD12 GPP_F11/I2C5_SCL/ISH_I2C2_SCL
U1 GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA
U2 GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL
U3 GPP_D15/ISH_UART0_RTS#
U4 GPP_D16/ISH_UART0_CTS#/SML0BALERT#
AC1 GPP_C12/UART1_RXD/ISH_UART1_RXD
AC2 GPP_C13/UART1_TXD/ISH_UART1_TXD
AC3 GPP_C14/UART1_RTS#/ISH_UART1_RTS#
AB4 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
AY8 GPP_A18/ISH_GP0
BA8 GPP_A19/ISH_GP1
BB7 GPP_A20/ISH_GP2
BA7 GPP_A21/ISH_GP3
AY7 GPP_A22/ISH_GP4
AW7 GPP_A23/ISH_GP5
R13 GPP_A12/BM_BUSY#/ISH_GP6

BOARD_ID0
BOARD_ID1
BOARD_ID3
BOARD_ID6
BOARD_ID5
BOARD_ID7
BOARD_ID8
GPU_EVENT# @1 → TC205 → PCH_TP_INT# 45

TC206 1 @ PXS_PWREN_R
TC207 1 @ PXS_RST#_R
TC208 1 @ DGPU_PWROK
TC204 1 @ FB_GC6_EN_R

+3VS
RC1561 1 @ 2 2.2K_0402_5% GPP_B18
33 PCH_CMOS_ON#
RC1563 1 @ 2 2.2K_0402_5% GPP_B22
40 UART_RX_DEBUG
40 UART_TX_DEBUG
45 TP_I2C_SDA0 RC1656 1 2 0_0402_5% PCH_I2C_SDA0
45 TP_I2C_SCL0 RC1657 1 2 0_0402_5% PCH_I2C_SCL0
40 PCH_WLAN_OFF# PCH_WLAN_OFF#
40 PCH_BT_OFF# PCH_BT_OFF#

@DIMM_ONLY@ @DIMM_ONLY@ @520Z@ @ @

+3VS

RC1651 2 @ 10K_0402_5%
RC1652 2 @ 10K_0402_5%
RC1653 2 @ 10K_0402_5%
RC1654 2 @ 10K_0402_5%
RC1655 2 @ 10K_0402_5%

BOARD_ID6
BOARD_ID7
BOARD_ID8
BOARD_ID9
BOARD_ID10

RC1624 2 @ 10K_0402_5%
RC1625 2 @ 10K_0402_5%
RC1626 2 @ 10K_0402_5%
RC1627 2 @ 10K_0402_5%
RC1628 2 @ 10K_0402_5%

@ @ 320G@ @ @

Board ID	Description		Stuff R
Board_ID [6,7]	00	Samsung 8Gb 2400 MT/s	RC1634 RC1635
	01	Hynix 8Gb 2400 MT/s	RC1634 RC1632
	10	Micron 8Gb 2400 MT/s	RC1631 RC1635
	11	SO-DIMM Only	RC1631 RC1632
Board_ID8	0	320G	RC1636
	1	520Z	RC1633
Board_ID9	0	Reserved	RC1640
	1	Reserved	RC1639
Board_ID10	0	Reserved	RC1652
	1	Reserved	RC1651

For EMI

HDA_SDIN0
CC7 10P_0201_50V8F EMC_NS@

30 HDA_SYNC_AUDIO RC43 1 2 33_0402_5% HDA_SYNC
30 HDA_BITCLK_AUDIO RC42 1 2 33_0402_5% HDA_BCLK
HDA_SDOUT
HDA_SDIN0
30 HDA_SDIN0
30 HDA_RST_AUDIO# RC44 1 2 33_0402_5% HDA_RST#

30 HDA_SDOUT_AUDIO
44 ME_FLASH
RC45 1 2 33_0402_5%
RC46 1 2 0_0402_5%
HDA_SDOUT

UC1G — SKL_ULT — AUDIO / SDIO/SDXC — SKYLAKE-U_BGA1356 REV = 1 — 1 OF 20

AUDIO:
BA22 HDA_SYNC/I2S0_SFRM
AY22 HDA_BLK/I2S0_SCLK
BB22 HDA_SDO/I2S0_TXD
BA21 HDA_SDI0/I2S0_RXD
AY21 HDA_SDI1/I2S1_RXD
AW22 HDA_RST#/I2S1_SCLK
J6 GPP_D23/I2S_MCLK
AY20 I2S1_SFRM
AW20 I2S1_TXD
AK7 GPP_F1/I2S2_SFRM
AK8 GPP_F0/I2S2_SCLK
AK9 GPP_F2/I2S2_TXD
AK10 GPP_F3/I2S2_RXD
H5 GPP_D19/DMIC_CLK0
D7 GPP_D20/DMIC_DATA0
D8 GPP_D17/DMIC_CLK1
C8 GPP_D18/DMIC_DATA1
AW5 GPP_B14/SPKR

SDIO/SDXC:
AB11 GPP_G0/SD_CMD
AB13 GPP_G1/SD_DATA0
AB12 GPP_G2/SD_DATA1
W12 GPP_G3/SD_DATA2
W11 GPP_G4/SD_DATA3
W10 GPP_G5/SD_CD#
W8 GPP_G6/SD_CLK
W7 GPP_G7/SD_WP
BA9 GPP_A17/SD_PWR_EN#/ISH_GP7
BB9 GPP_A16/SD_1P8_SEL
AB7 SD_RCOMP
AF13 GPP_F23

BOARD_ID10
BOARD_ID9
SD_RCOMP → RC49 200_0402_1%

+3VS
RC14 1 @ 2 2.2K_0402_5% PCH_BEEP
30 PCH_BEEP

Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable " Top Swap" mode. (Default) ★ 1 = Enable " Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0_MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable " No Reboot" mode. (Default) ★ 1 = Enable " No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1_MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) ★ 1 = LPC	0	Rising edge of PCH_PWROK

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Title: MCP (LPSS,ISH,AUDIO,SDI

Size	Document Number	Rev
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@DIS For NV and AMD GPU SKU

20 PCIE_CRX_GTX_N[0..3]
20 PCIE_CRX_GTX_P[0..3]
20 PCIE_CTX_C_GRX_N[0..3]
20 PCIE_CTX_C_GRX_P[0..3]

DGPU

PCIE_CTX_C_GRX_N0	0.22U 0201 6.3V6-K	DIS@ 1	2 CC16	PCIE_CRX_GTX_N0	H13	PCIE1_RXN/USB3_5_RXN
PCIE_CTX_C_GRX_P0	0.22U 0201 6.3V6-K	DIS@ 1	2 CC14	PCIE_CRX_GTX_P0	G13	PCIE1_RXP/USB3_5_RXP
				PCIE_CTX_GRX_N0	B17	PCIE1_TXN/USB3_5_TXN
				PCIE_CTX_GRX_P0	A17	PCIE1_TXP/USB3_5_TXP
PCIE_CTX_C_GRX_N1	0.22U 0201 6.3V6-K	DIS@ 1	2 CC15	PCIE_CRX_GTX_N1	G11	PCIE2_RXN/USB3_6_RXN
PCIE_CTX_C_GRX_P1	0.22U 0201 6.3V6-K	DIS@ 1	2 CC17	PCIE_CRX_GTX_P1	F11	PCIE2_RXP/USB3_6_RXP
				PCIE_CTX_GRX_N1	D16	PCIE2_TXN/USB3_6_TXN
				PCIE_CTX_GRX_P1	C16	PCIE2_TXP/USB3_6_TXP
PCIE_CTX_C_GRX_N2	0.22U 0201 6.3V6-K	DIS@ 1	2 CC18	PCIE_CRX_GTX_N2	H16	PCIE3_RXN
PCIE_CTX_C_GRX_P2	0.22U 0201 6.3V6-K	DIS@ 1	2 CC19	PCIE_CRX_GTX_P2	G16	PCIE3_RXP
				PCIE_CTX_GRX_N2	D17	PCIE3_TXN
				PCIE_CTX_GRX_P2	C17	PCIE3_TXP
PCIE_CTX_C_GRX_N3	0.22U 0201 6.3V6-K	DIS@ 1	2 CC20	PCIE_CRX_GTX_N3	G15	PCIE4_RXN
PCIE_CTX_C_GRX_P3	0.22U 0201 6.3V6-K	DIS@ 1	2 CC21	PCIE_CRX_GTX_P3	F15	PCIE4_RXP
				PCIE_CTX_GRX_N3	B19	PCIE4_TXN
				PCIE_CTX_GRX_P3	A19	PCIE4_TXP

LAN

37 PCIE_PRX_DTX_N5			PCIE_PRX_DTX_N5	F16	PCIE5_RXN	
37 PCIE_PRX_DTX_P5			PCIE_PRX_DTX_P5	E16	PCIE5_RXP	
37 PCIE_PTX_C_DRX_N5	CC1262 1	2 0.1u 0201 10V6K	PCIE_PTX_DRX_N5	C19	PCIE5_TXN	
37 PCIE_PTX_C_DRX_P5	CC1261 1	2 0.1u 0201 10V6K	PCIE_PTX_DRX_P5	D19	PCIE5_TXP	

WLAN

40 PCIE_PRX_DTX_N6			PCIE_PRX_DTX_N6	G18	PCIE6_RXN	
40 PCIE_PRX_DTX_P6			PCIE_PRX_DTX_P6	F18	PCIE6_RXP	
40 PCIE_PTX_C_DRX_N6	CC1264 1	2 0.1u 0201 10V6K	PCIE_PTX_DRX_N6	D20	PCIE6_TXN	
40 PCIE_PTX_C_DRX_P6	CC1263 1	2 0.1u 0201 10V6K	PCIE_PTX_DRX_P6	C20	PCIE6_TXP	

SATA HDD

42 SATA_PRX_DTX_N0		SATA_PRX_DTX_N0	F20	PCIE7_RXN/SATA0_RXN	
42 SATA_PRX_DTX_P0		SATA_PRX_DTX_P0	E20	PCIE7_RXP/SATA0_RXP	
42 SATA_PTX_DRX_N0		SATA_PTX_DRX_N0	B21	PCIE7_TXN/SATA0_TXN	
42 SATA_PTX_DRX_P0		SATA_PTX_DRX_P0	A21	PCIE7_TXP/SATA0_TXP	

SATA ODD

42 SATA_PRX_DTX_N1		SATA_PRX_DTX_N1	G21	PCIE8_RXN/SATA1A_RXN	
42 SATA_PRX_DTX_P1		SATA_PRX_DTX_P1	F21	PCIE8_RXP/SATA1A_RXP	
42 SATA_PTX_DRX_N1		SATA_PTX_DRX_N1	D21	PCIE8_TXN/SATA1A_TXN	
42 SATA_PTX_DRX_P1		SATA_PTX_DRX_P1	C21	PCIE8_TXP/SATA1A_TXP	

Optane Memory

40 PCIE_PRX_DTX_N9		PCIE_PRX_DTX_N9	E22	PCIE9_RXN	
40 PCIE_PRX_DTX_P9		PCIE_PRX_DTX_P9	E23	PCIE9_RXP	
40 PCIE_PTX_C_DRX_N9	CC22 1	2 0.22U 0201 6.3V6-K	PCIE_PTX_DRX_N9	B23	PCIE9_TXN	
40 PCIE_PTX_C_DRX_P9	CC23 1	2 0.22U 0201 6.3V6-K	PCIE_PTX_DRX_P9	A23	PCIE9_TXP	
40 PCIE_PRX_DTX_N10			PCIE_PRX_DTX_N10	F25	PCIE10_RXN	
40 PCIE_PRX_DTX_P10			PCIE_PRX_DTX_P10	E25	PCIE10_RXP	
40 PCIE_PTX_C_DRX_N10	CC1266 1	2 0.22U 0201 6.3V6-K	PCIE_PTX_DRX_N10	D23	PCIE10_TXN	
40 PCIE_PTX_C_DRX_P10	CC1265 1	2 0.22U 0201 6.3V6-K	PCIE_PTX_DRX_P10	C23	PCIE10_TXP	
	RC119 1	2 100_0402_1%	PCIE_RCOMPN	F5	PCIE_RCOMPN	
			PCIE_RCOMPP	E5	PCIE_RCOMPP	

PCIE_RCOMPN and PCIE_RCOMPP Trace Width: 12-15mil Differential between RCOMPP/RCOMPN

PAD@ TC20 1 XDP_PRDY# D56
PAD@ TC19 1 XDP_PRE0# D61
PIRQA# BB11

PROC_PRDY#
PROC_PREQ#
GPP_A7/PIRQA#

40 PCIE_PRX_DTX_N11		PCIE_PRX_DTX_N11	E28	PCIE11_RXN/SATA1B_RXN	
40 PCIE_PRX_DTX_P11		PCIE_PRX_DTX_P11	E27	PCIE11_RXP/SATA1B_RXP	
40 PCIE_PTX_C_DRX_N11	CC1267 1	2 0.22U 0201 6.3V6-K	PCIE_PTX_DRX_N11	D24	PCIE11_TXN/SATA1B_TXN	
40 PCIE_PTX_C_DRX_P11	CC1268 1	2 0.22U 0201 6.3V6-K	PCIE_PTX_DRX_P11	C24	PCIE11_TXP/SATA1B_TXP	
40 PCIE_PRX_DTX_N12			PCIE_PRX_DTX_N12	E30	PCIE12_RXN/SATA2_RXN	
40 PCIE_PRX_DTX_P12			PCIE_PRX_DTX_P12	F30	PCIE12_RXP/SATA2_RXP	
40 PCIE_PTX_C_DRX_N12	CC1269 1	2 0.22U 0201 6.3V6-K	PCIE_PTX_DRX_N12	A25	PCIE12_TXN/SATA2_TXN	
40 PCIE_PTX_C_DRX_P12	CC1270 1	2 0.22U 0201 6.3V6-K	PCIE_PTX_DRX_P12	B25	PCIE12_TXP/SATA2_TXP	

UC1H — SKL_ULT — PCIE/USB3/SATA

SKYLAKE-U_BGA1356
REV = 1
@
1 OF 20

SSIC / USB3

USB3_1_RXN	H8	USB30_RX_N1	USB30_RX_N1	41
USB3_1_RXP	G8	USB30_RX_P1	USB30_RX_P1	41
USB3_1_TXN	C13	USB30_TX_N1	USB30_TX_N1	41
USB3_1_TXP	D13	USB30_TX_P1	USB30_TX_P1	41
	J6	USB30_RX_N2		
USB3_2_RXN/SSIC_1_RXN	H6	USB30_RX_P2	USB30_RX_N2	43
USB3_2_RXP/SSIC_1_RXP	B13	USB30_TX_N2	USB30_RX_P2	43
USB3_2_TXN/SSIC_1_TXN	A13	USB30_TX_P2	USB30_TX_N2	43
USB3_2_TXP/SSIC_1_TXP	J10	USB30_RX_N3	USB30_TX_P2	43
USB3_3_RXN/SSIC_2_RXN	H10	USB30_RX_P3	USB30_RX_N3	41
USB3_3_RXP/SSIC_2_RXP	B15	USB30_TX_N3	USB30_RX_P3	41
USB3_3_TXN/SSIC_2_TXN	A15	USB30_TX_P3	USB30_TX_N3	41
USB3_3_TXP/SSIC_2_TXP			USB30_TX_P3	41
USB3_4_RXN	E10			
USB3_4_RXP	C10			
USB3_4_TXN	C15			
USB3_4_TXP	D15			

LEFT USB3.0
Type-C
LEFT USB3.0

USB2

USB2N_1	AB9	USB20_N1	USB20_N1	41
USB2P_1	AB10	USB20_P1	USB20_P1	41
USB2N_2	AD6	USB20_N2	USB20_N2	43
USB2P_2	AD7	USB20_P2	USB20_P2	43
USB2N_3	AH3	USB20_N3	USB20_N3	41
USB2P_3	AJ3	USB20_P3	USB20_P3	41
USB2N_4	AD9	USB20_N4	USB20_N4	45
USB2P_4	AD10	USB20_P4	USB20_P4	45
USB2N_5	AJ1	USB20_N5	USB20_N5	30
USB2P_5	AJ2	USB20_P5	USB20_P5	30
USB2N_6	AF6	USB20_N6	USB20_N6	33
USB2P_6	AF7	USB20_P6	USB20_P6	33
USB2N_7	AH1	USB20_N7	USB20_N7	40
USB2P_7	AH2	USB20_P7	USB20_P7	40
USB2N_8	AF8	USB20_N8	USB20_N8	33
USB2P_8	AF9	USB20_P8	USB20_P8	33
USB2N_9	AG1			
USB2P_9	AG2			
USB2N_10	AH7			
USB2P_10	AH8			

LEFT USB3.0
Type-C
LEFT USB3.0
Finger Print
Card reader
Touch panel
BT
Camera

USB2_COMP	AB6	USB2_COMP	RC118 2	1 113_0402_1%
USB2_ID	AG3	USB2_ID	RC1626 1	2 0_0402_5%
USB2_VBUSSENSE	AG4	USB2_VBUSSENSE	RC1627 1	2 1K_0402_5%

USBRBIAS
Width 20Mil
Space 15Mil
Length 500Mil

GPP_E9/USB2_OC0#	A9	USB_OC0#	
GPP_E10/USB2_OC1#	C9	USB_OC1#	USB_OC1# 41
GPP_E11/USB2_OC2#	D9	USB_OC2#	
GPP_E12/USB2_OC3#	B9	USB_OC3#	

GPP_E4/DEVSLP0	J1	GPP_E4	
GPP_E5/DEVSLP1	J2	GPP_E5	1 @PAD TC202
GPP_E6/DEVSLP2	J3		

RC1628 1 — 2 0_0402_5% — EC_SMI# 44

2016/05/03: Implement as Power Button function for Windows RedStone support

GPP_E0/SATAXPCIE0/SATAGP0	H2	SATA0GP	
GPP_E1/SATAXPCIE1/SATAGP1	H3	ODD_DETECT#	
GPP_E2/SATAXPCIE2/SATAGP2	G4	SATA2GP	
GPP_E8/SATALED#	H1	BOARD_ID2	BOARD_ID2 8

+3VS
RPC2: 1 ODD_DETECT# 8; 2 SATA0GP 7; 3 SATA2GP 6; 4 PIRQA# 5
10K_0804_8P4R_5%

+3VALW_PCH
RPC17: USB_OC0# 8; USB_OC1# 7; USB_OC3# 6; USB_OC2# 5; 1 2 3 4
10K_0804_8P4R_5%

+3VS
GPP_E4 RC1617 2 @ 1 10K_0402_5%
USB_OC2# RC1654 1 2 0_0402_5% TYPE_C_OCP# 43

8/24 Reserve TYPE_C_OCP# to CPU USB_OC2# wei

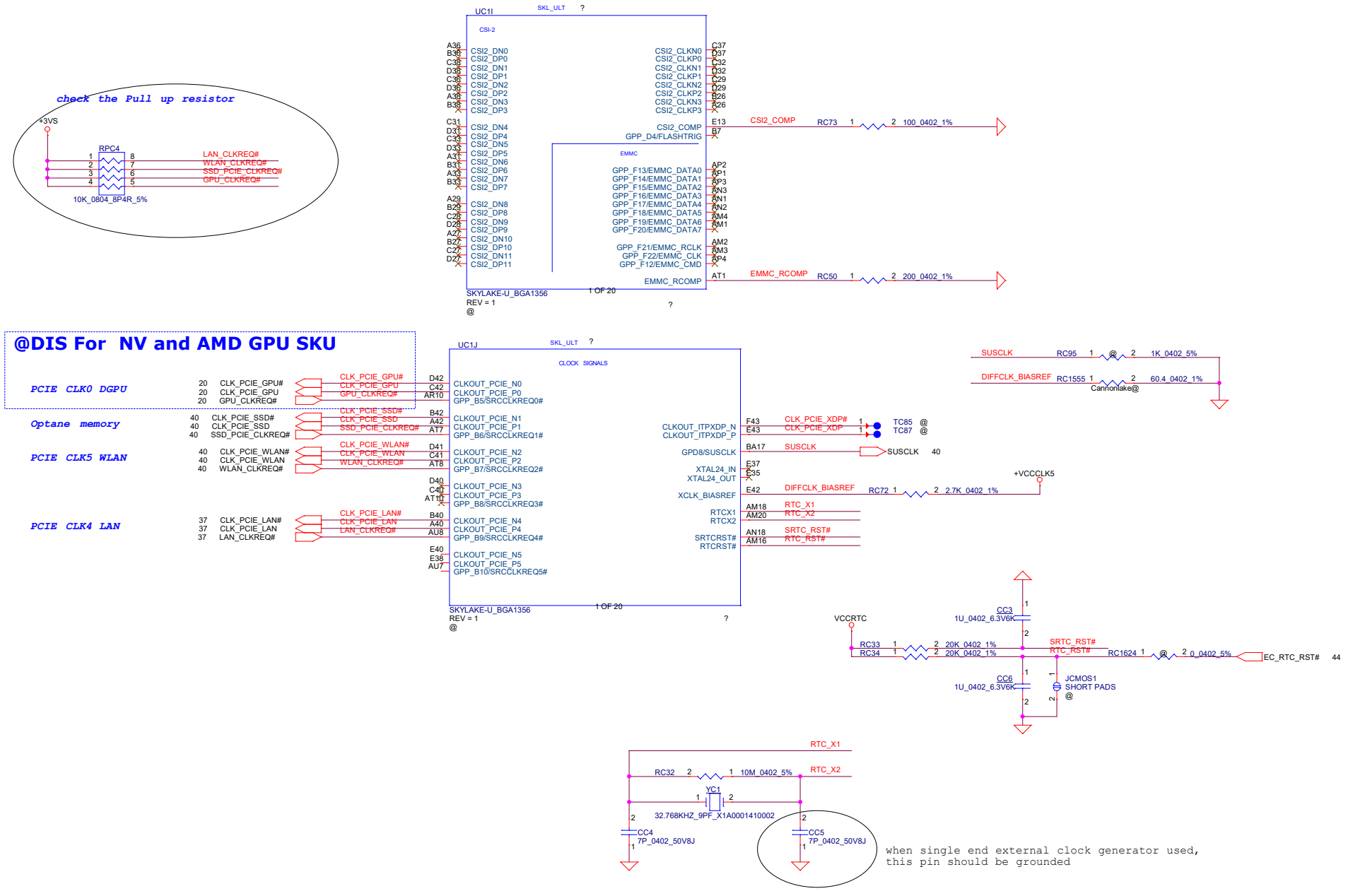
SATA2GP RC189 1 2 0_0402_5% SSD_DET# 40

Add SSD_DET# for Optane memory wei

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (PCIE,SATA,USB3,US

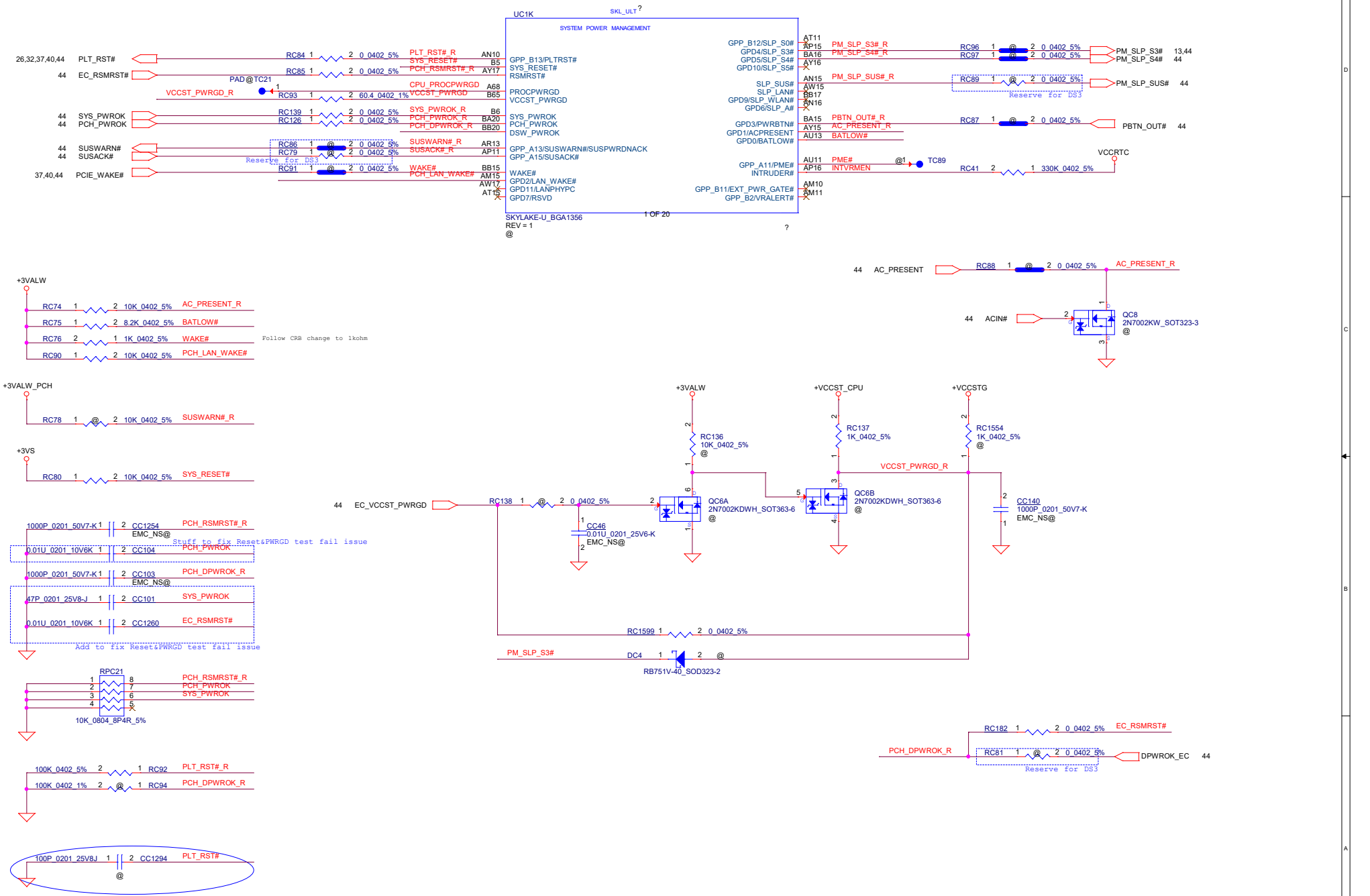
Size: Custom	Document Number: EG521	Rev: 0.2
Date: Tuesday, April 25, 2017	Sheet 9 of 60	



Title: MCP (CSI2,EMMC,CLOCK)

Size	Document Number	Rev
Custom	EG521	0.2

Date: Tuesday, April 25, 2017 Sheet 10 of 60



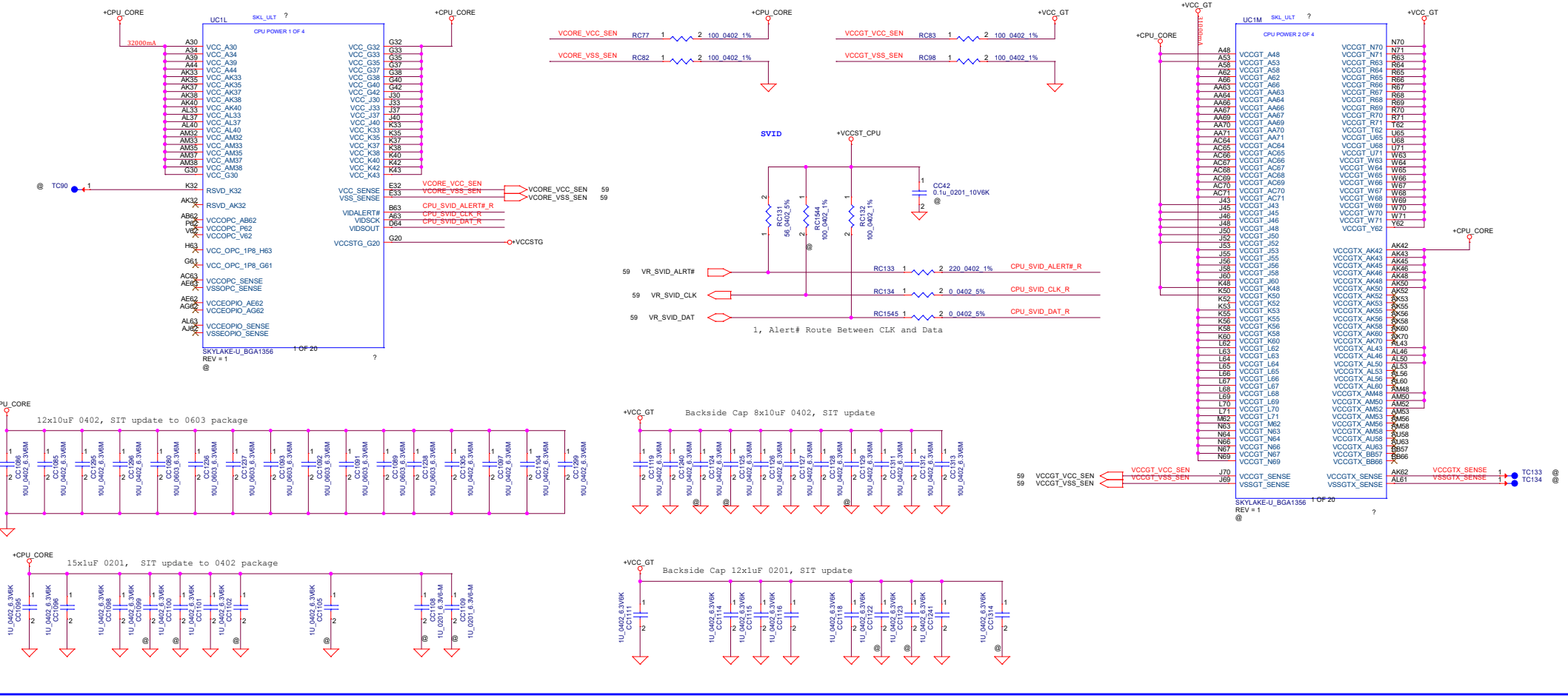
10/25 SIT Add to fix PLT_RST# glitch issue wei

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (SYSTEM PWR MANAGEMENT)

Size	Document Number	Rev
Custom	EG521	0.2

Date: Tuesday, April 25, 2017 Sheet 11 of 60

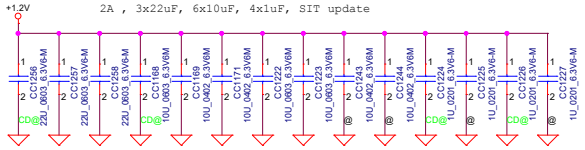


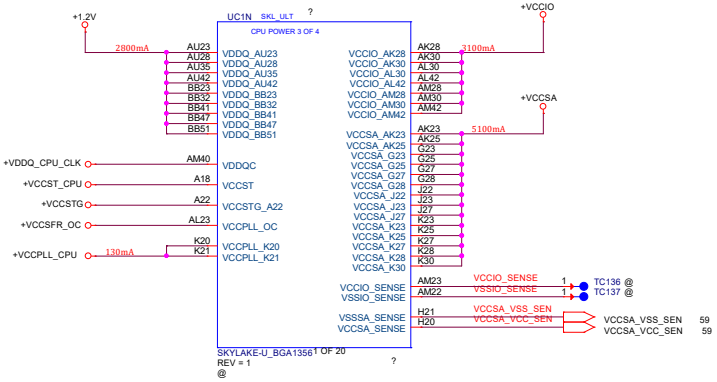
Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

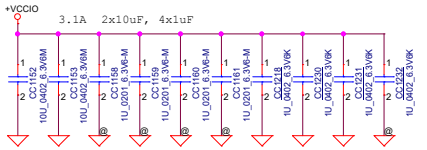
Title: **MCP (CPU PWR1)**

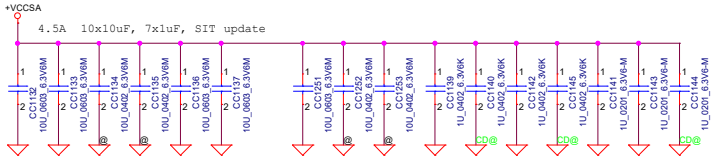
Size	Document Number	Rev
Custom	EG521	0.2

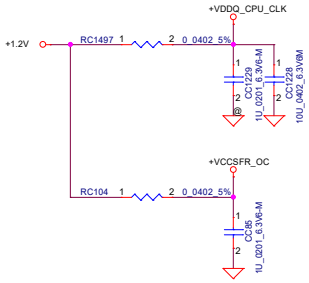
Date: Tuesday, April 25, 2017 | Sheet 12 of 60

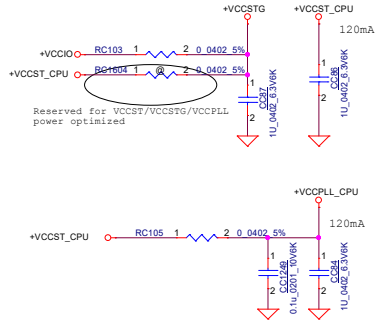


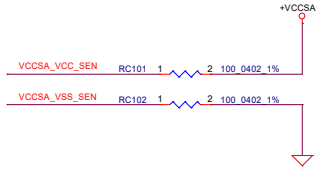


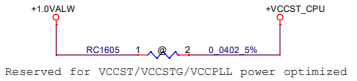


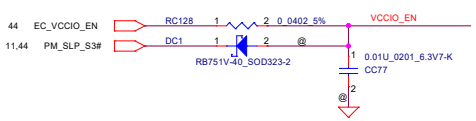


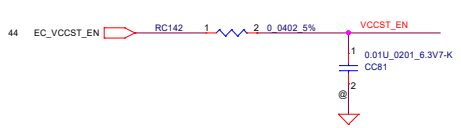


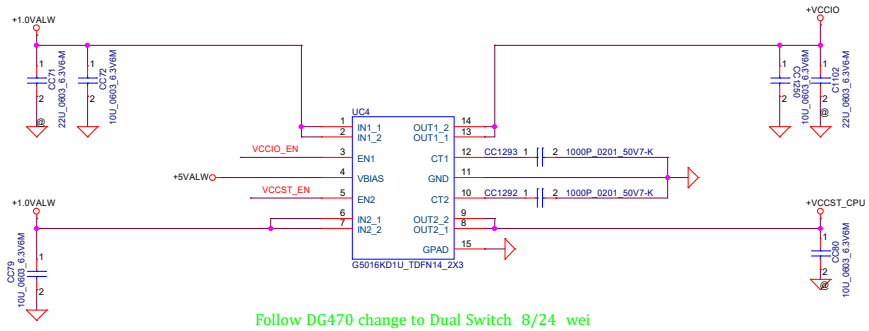












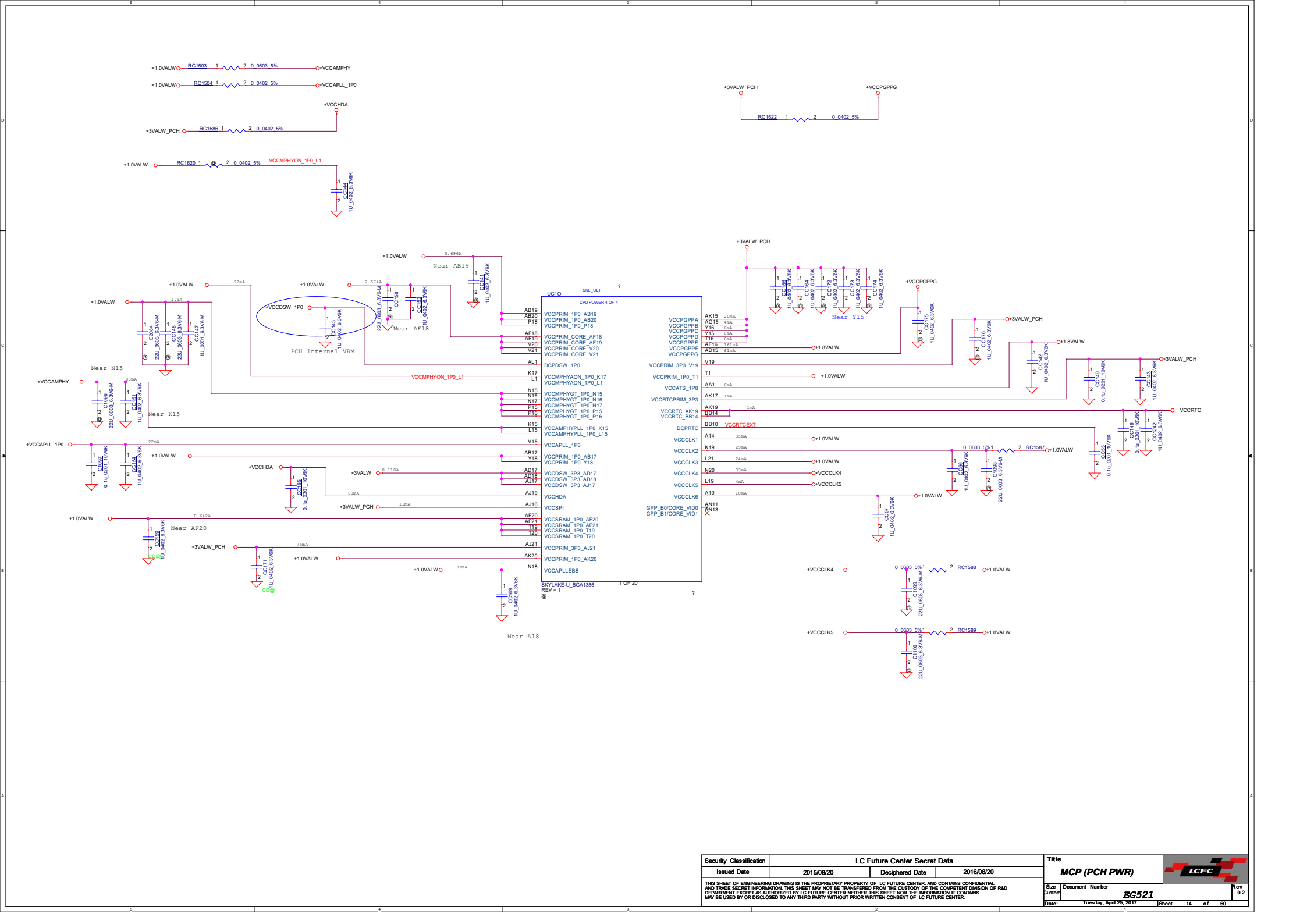
Follow DG470 change to Dual Switch 8/24 wei

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (CPU PWR2)

Size: Custom | Document Number: EG521 | Rev: 0.2

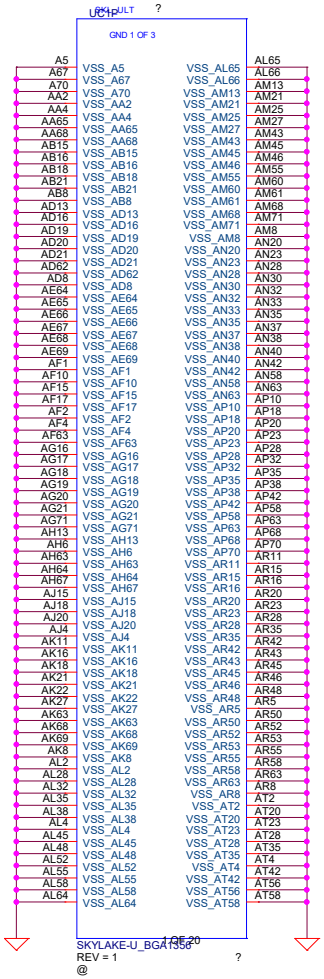
Date: Tuesday, April 25, 2017 | Sheet 13 of 60

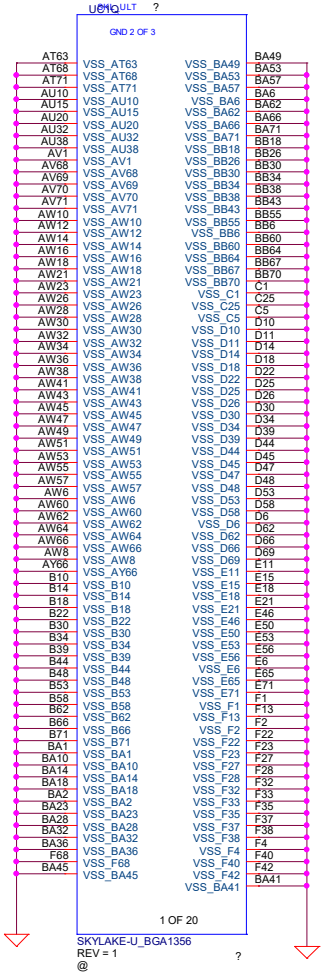


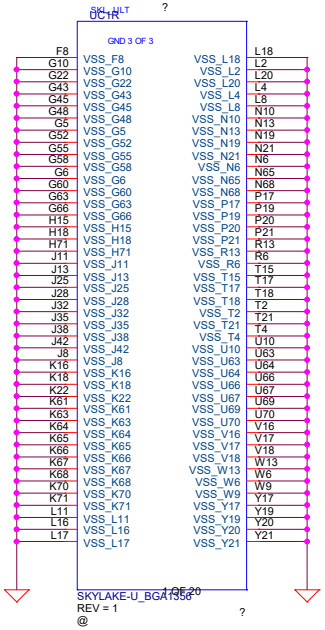
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (PCH PWR)**

Size: Custom	Document Number: EG521	Rev: 0.2
Date: Tuesday, April 25, 2017	Sheet 14 of 60	





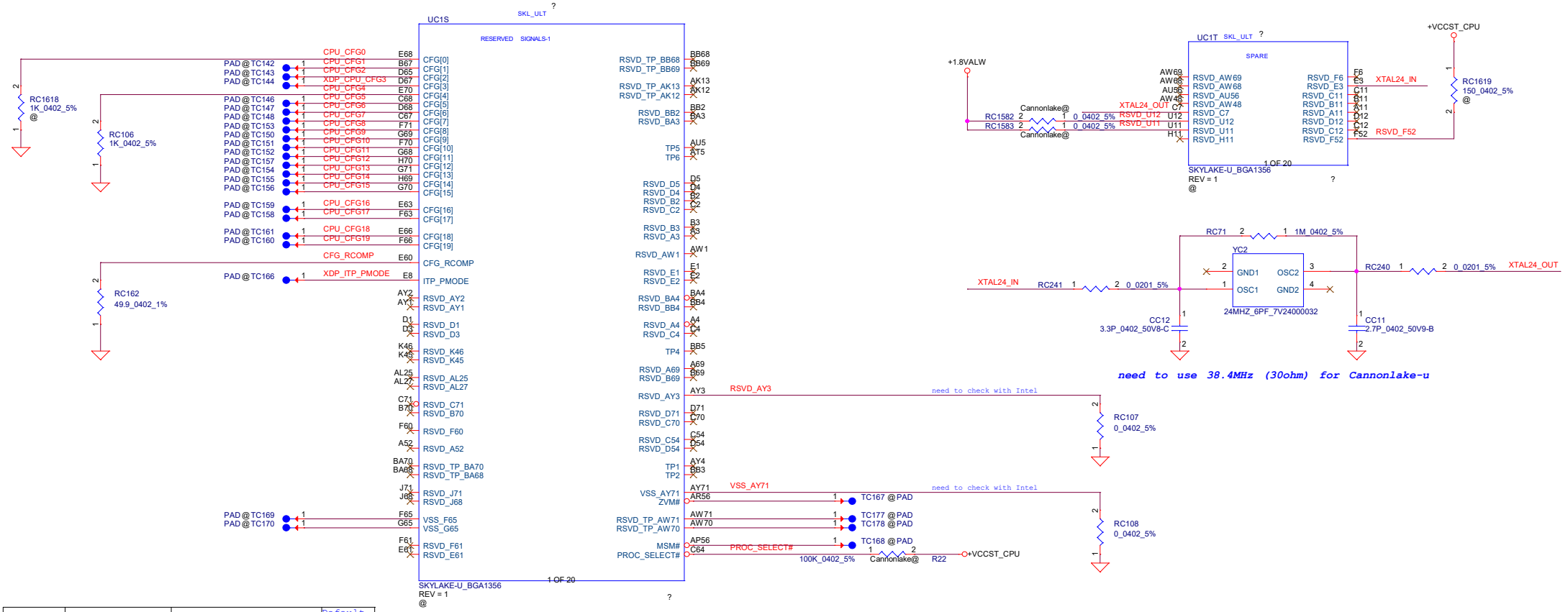


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (VSS)**

Size	Document Number	Rev
Custom	EG521	0.2

Date: Tuesday, April 25, 2017 Sheet 15 of 60



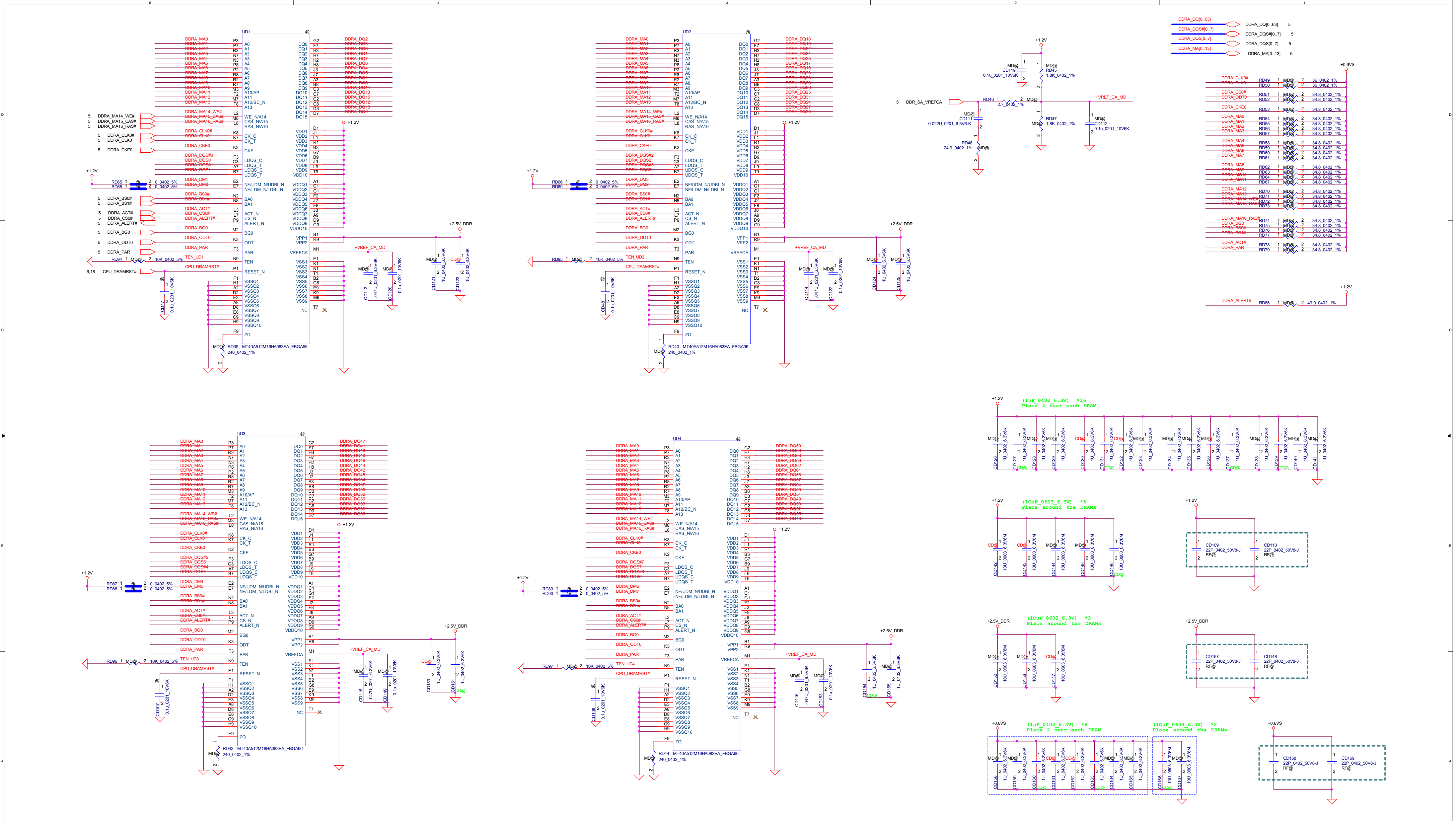
Pin Name	Strap Description	Configuration	Default Value
CFG[4]	Display Port Presence strap	– 1 = eDP Disabled – 0 = eDP Enabled ★	1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (CFG,RESERVED)

Size	Document Number	Rev
Custom	EG521	0.2

Date: Tuesday, April 25, 2017 Sheet 16 of 60



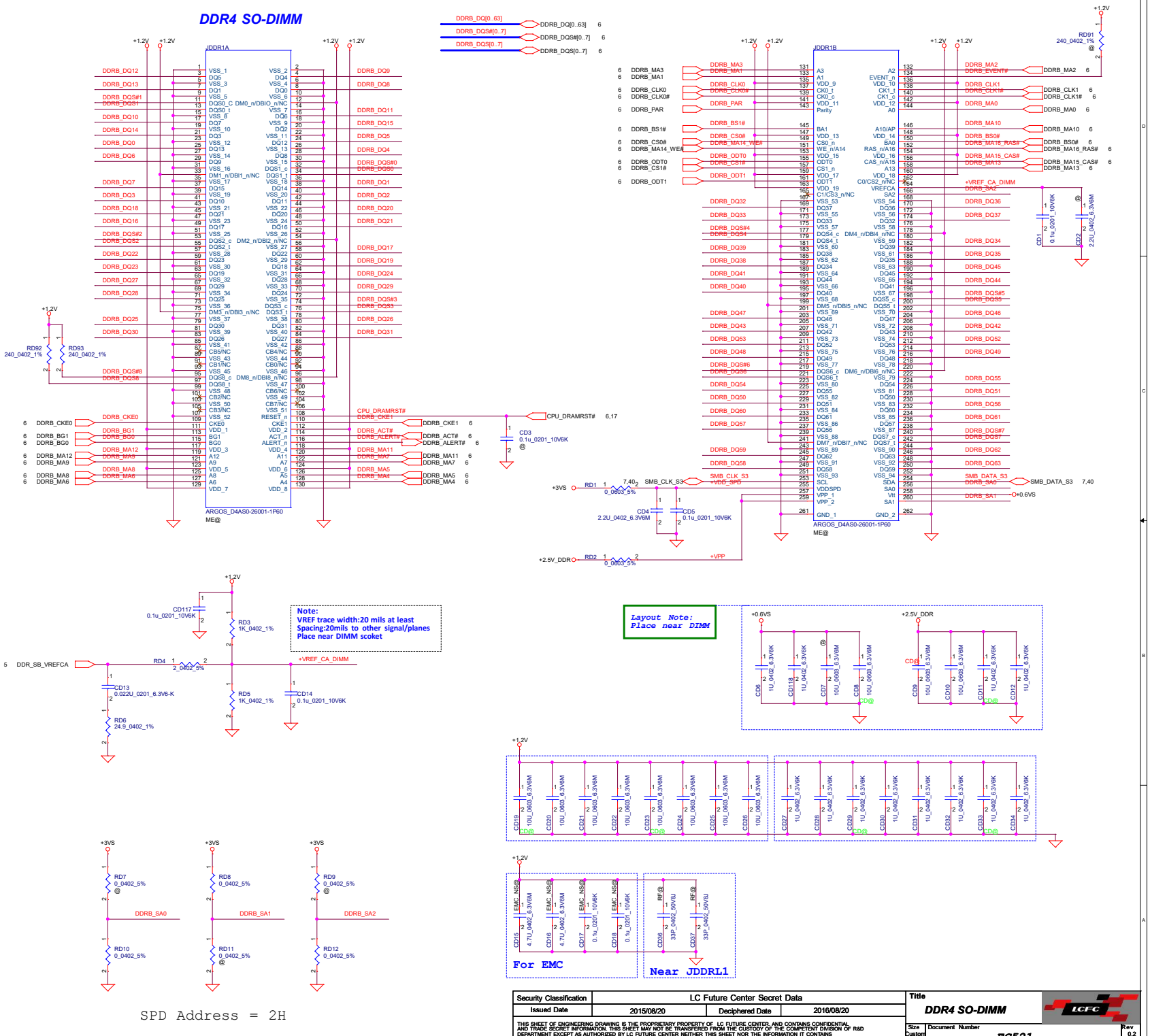
Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

Title: **DDR4 Memory Down**

Size: Custom | Document Number: EG523 | Rev: 0.2

Date: Tuesday, April 25, 2017 |

DDR4 SO-DIMM



Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM scoket

Layout Note: Place near DIMM

SPD Address = 2H

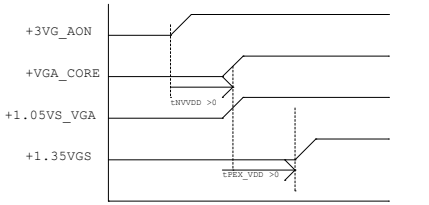
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	DDR4 SO-DIMM		
Size: Custom	Document Number: EG521		Rev: 0.2
Date: Tuesday, April 25, 2017	Sheet 18 of 60		

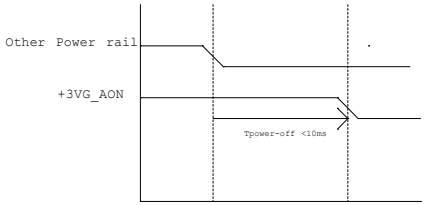
N16x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

N15V-GM Power Sequence



1. all power rail ramp up time should be larger than 40us-4ms



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

Products	GPU (W)	Mem (W)	Min Core Clk (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	(1.05V) (6) (mA)	(1.05V) (6) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

N16x Multi-level Straps

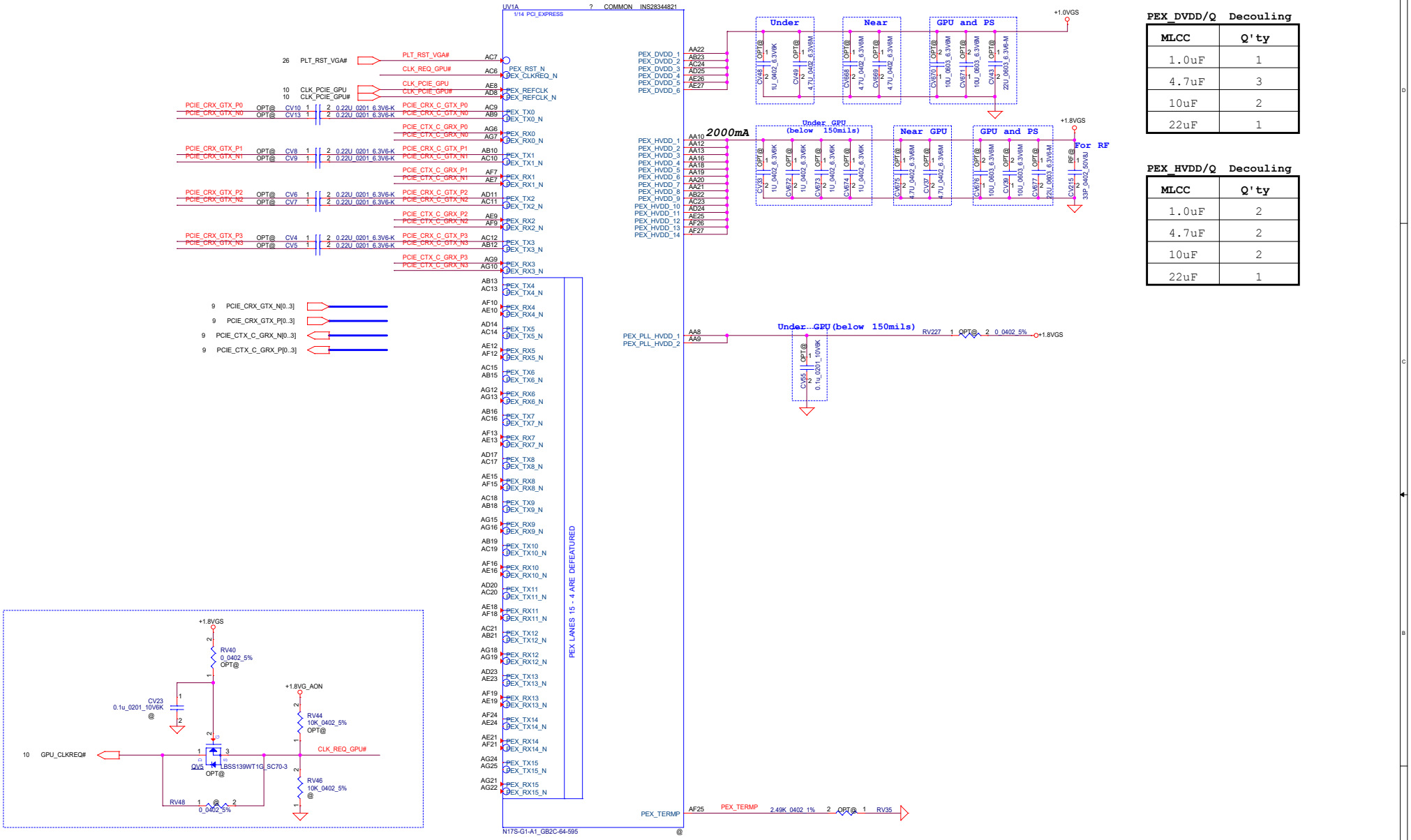
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: *VGA Notes List*

Size	Document Number	Rev
C	EG521	0.2

Date: Tuesday, April 25, 2017 Sheet 19 of 60



PEX_DVDD/Q Decouling

MLCC	Q'ty
1.0uF	1
4.7uF	3
10uF	2
22uF	1

PEX_HVDD/Q Decouling

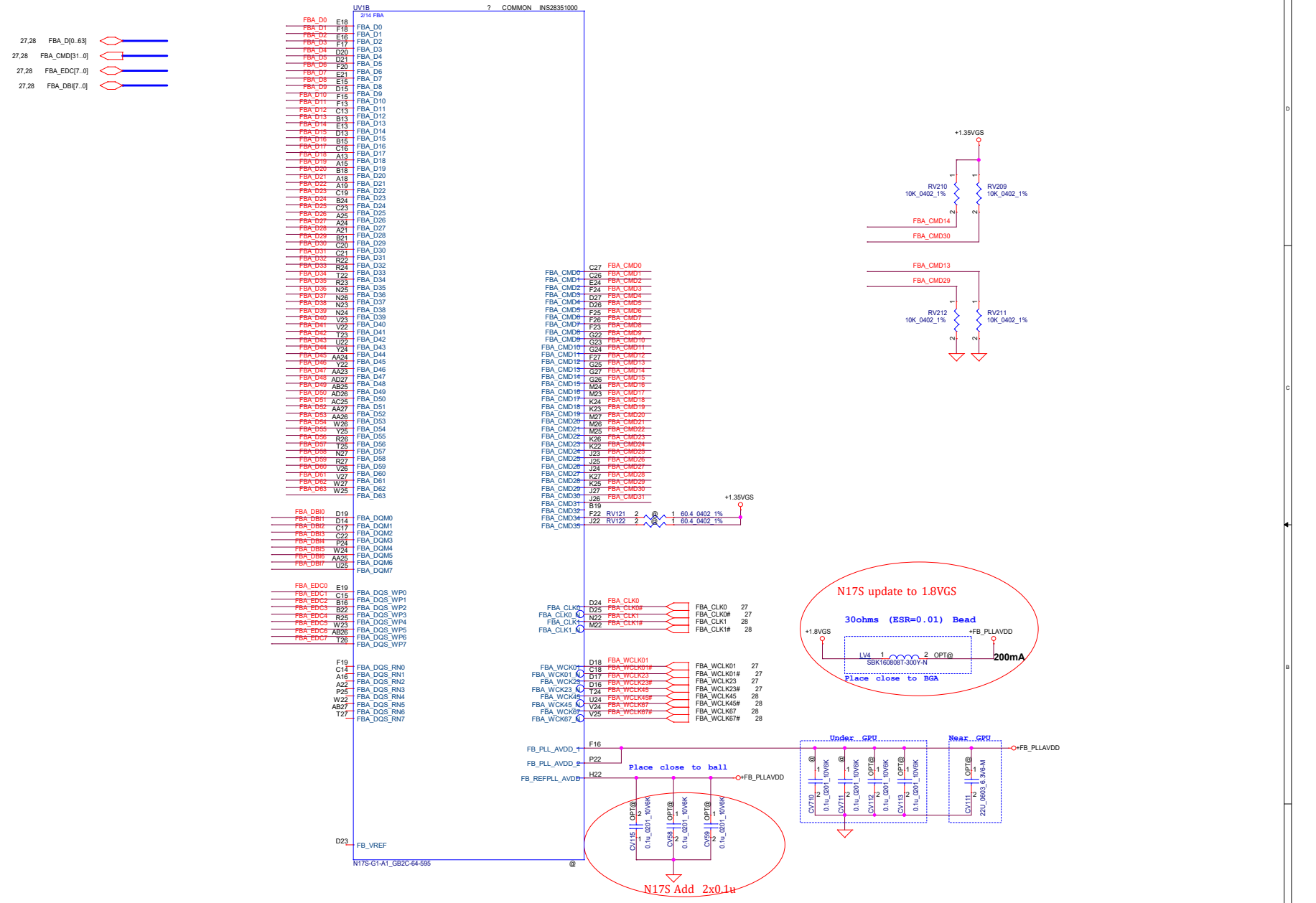
MLCC	Q'ty
1.0uF	2
4.7uF	2
10uF	2
22uF	1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **N17S_PCIE Interface**

Size	Document Number	Rev
C	EG521	0.2

Date: Tuesday, April 25, 2017 | Sheet 20 of 60

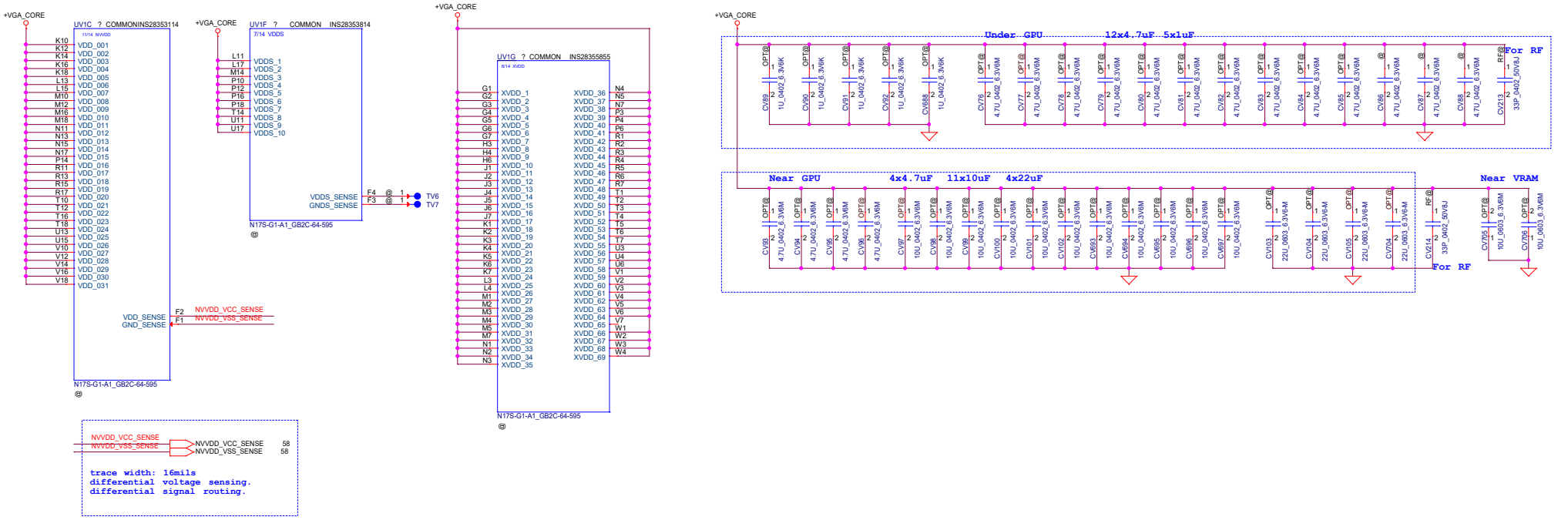


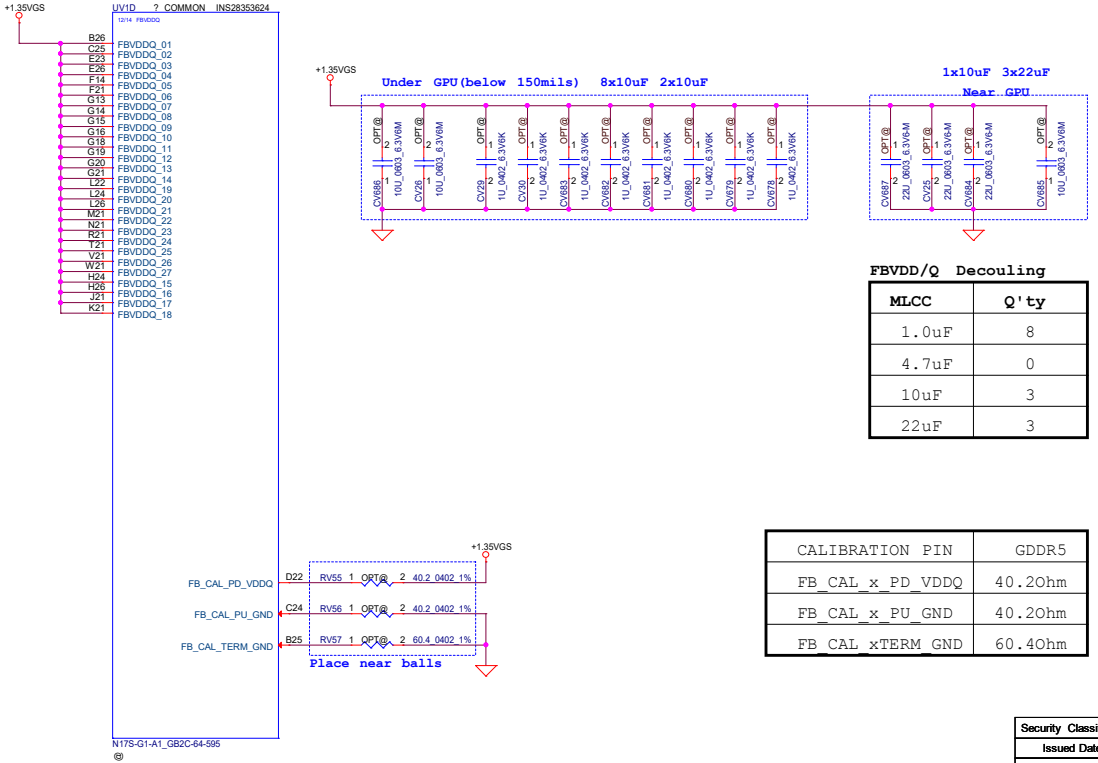
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **N17S_MEM Interface**

Size	Document Number	Rev
C	EG521	0.2

Date: Tuesday, April 25, 2017 Sheet 21 of 60





FBVDD/Q Decouling

MLCC	Q'ty
1.0uF	8
4.7uF	0
10uF	3
22uF	3

CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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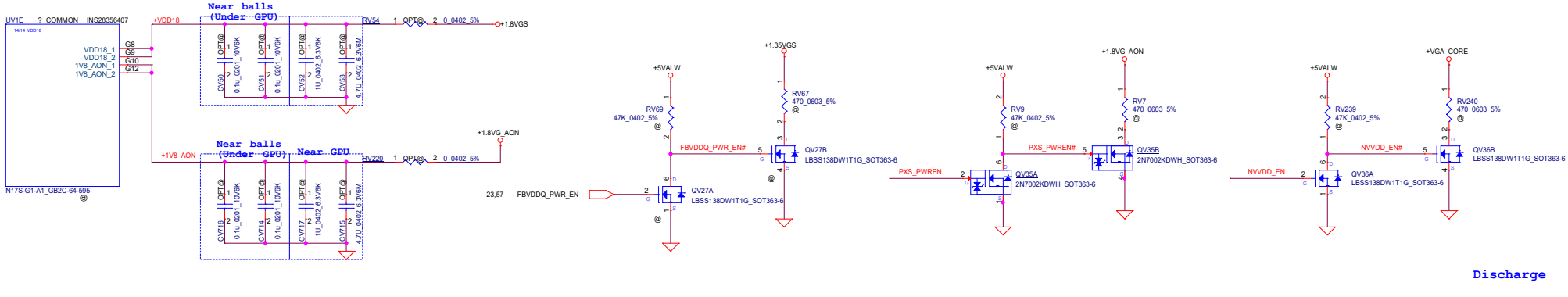
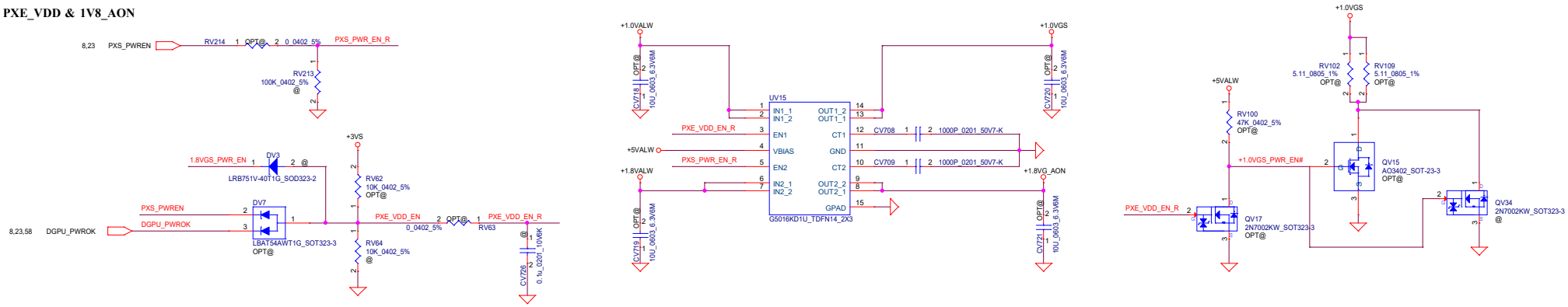
Title: N17S_+VGA_CORE,FBVDDQ

Size	Document Number	Rev
C	EG521	0.2

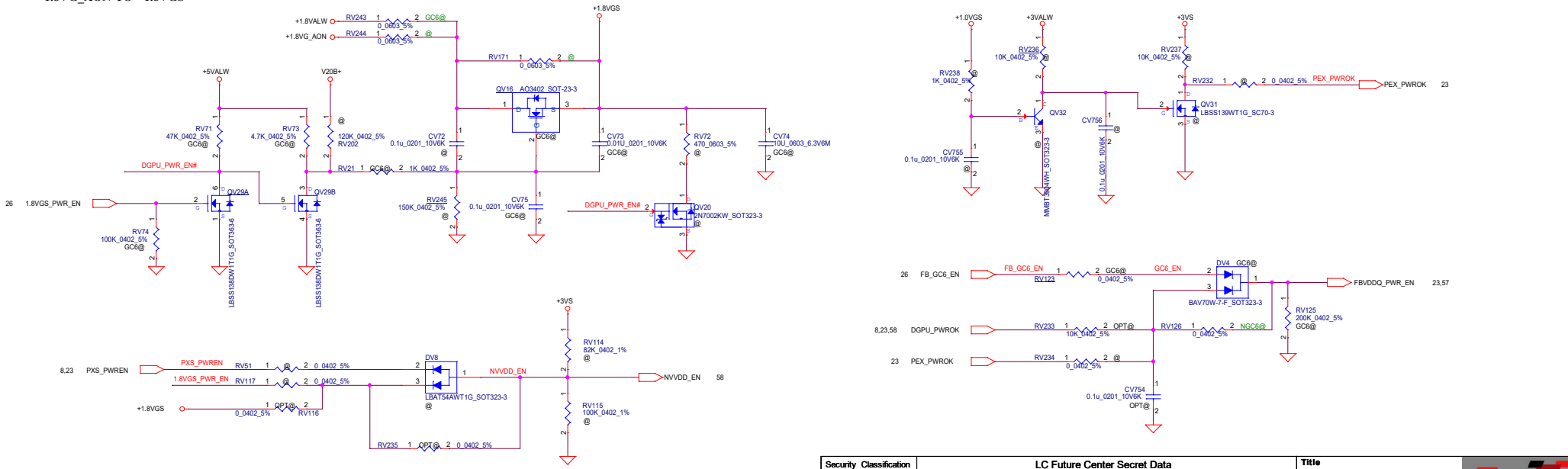
Date: Tuesday, April 25, 2017 Sheet 22 of 60



PXE_VDD & 1V8_AON

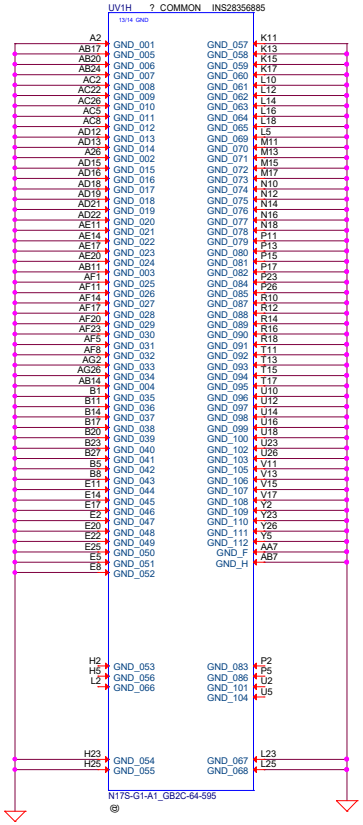


+1.8VG_AON TO +1.8VGS



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	N17S_AON/MAIN PWR		
Size	Document Number		Rev
C	EG521		0.2
Date:	Tuesday, April 25, 2017	Sheet	23 of 60

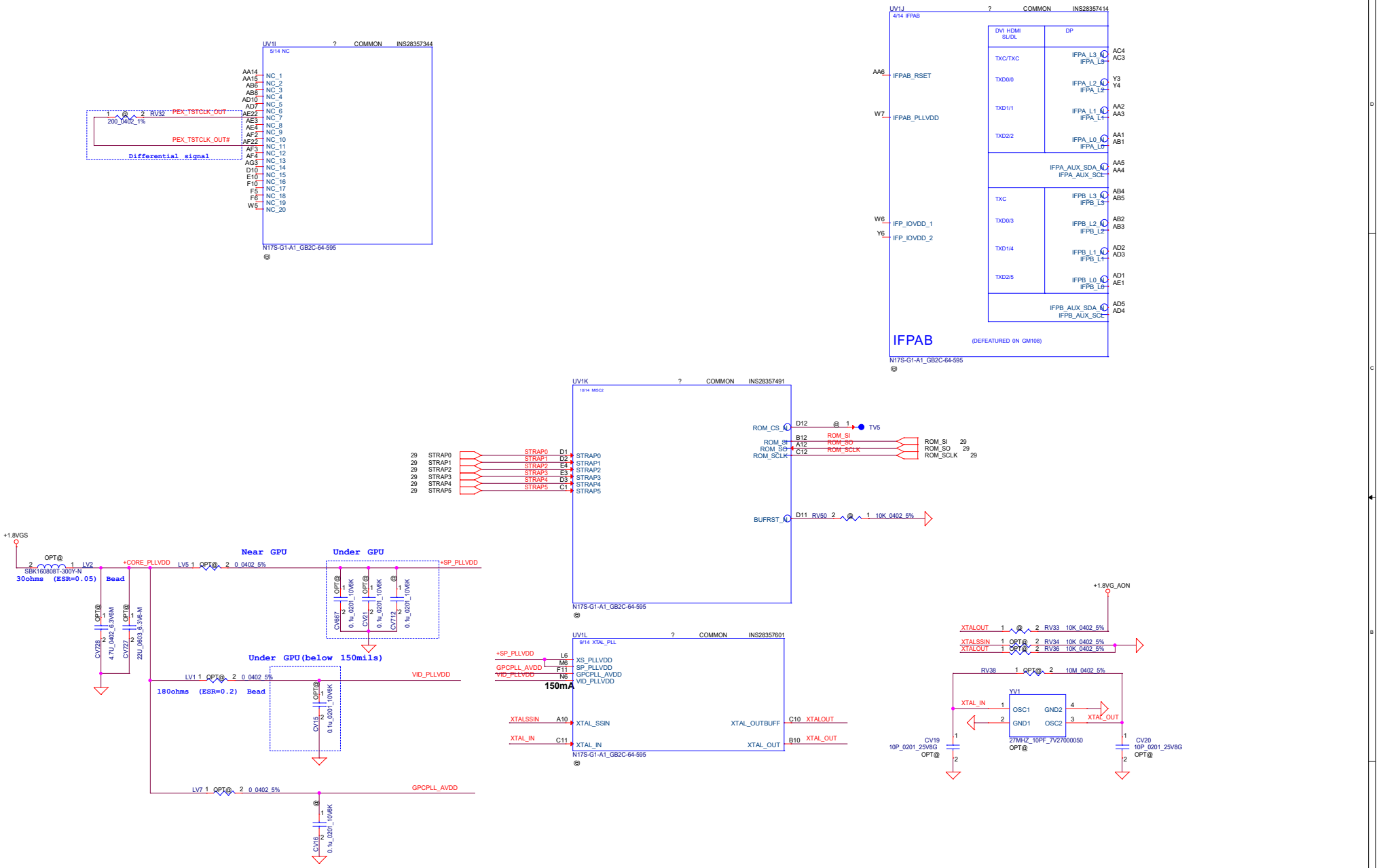


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **N17S_GND**

Size	Document Number	Rev
C	EG521	0.2

Date: Tuesday, April 25, 2017 | Sheet 24 of 60

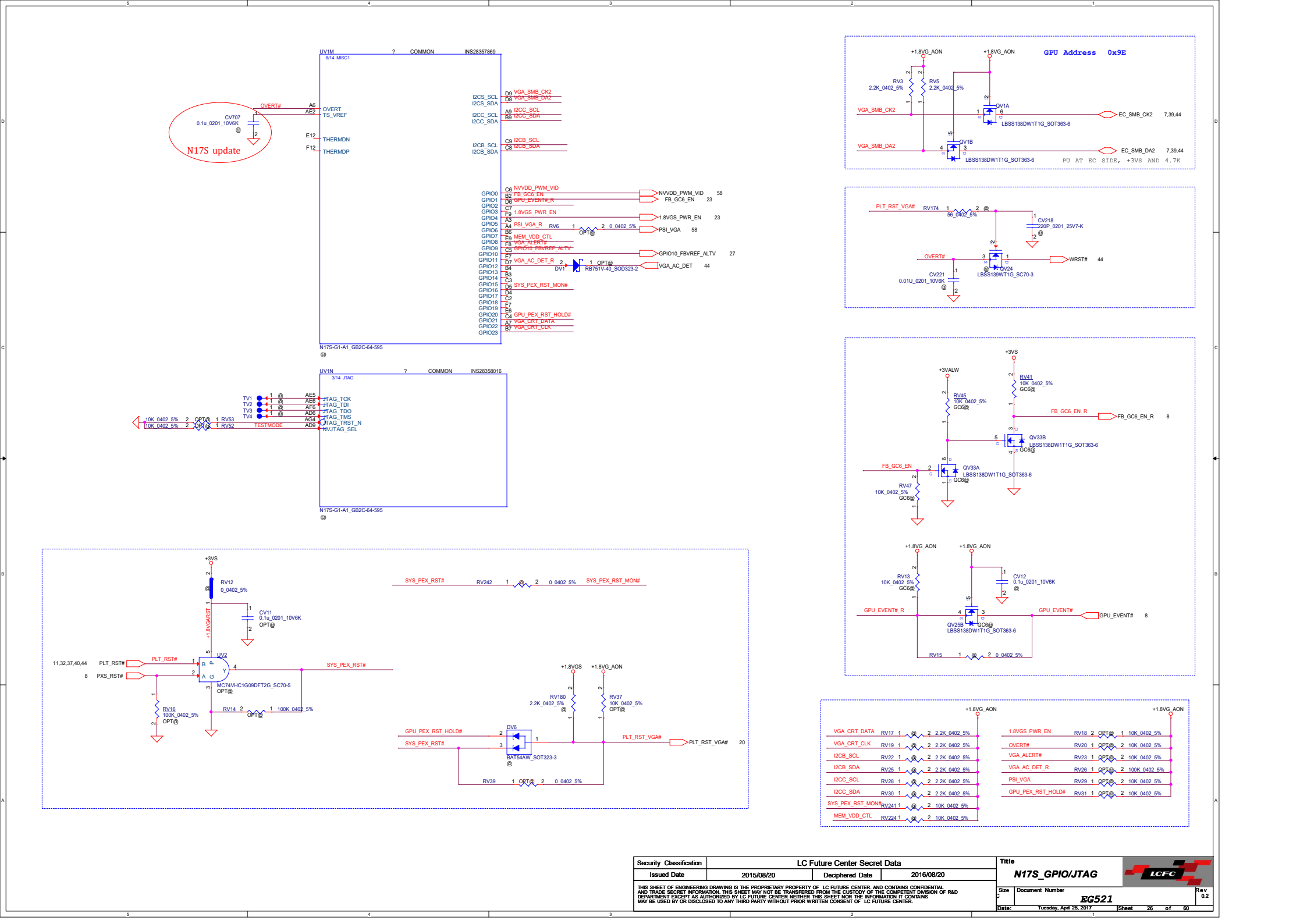


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: N17S_STRAP/DP/HDMI

Size	Document Number	Rev
C	EG521	0.2

Date: Tuesday, April 25, 2017 Sheet 25 of 60



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: N17S_GPIO/JTAG

Size	Document Number	Rev
C	EG521	0.2

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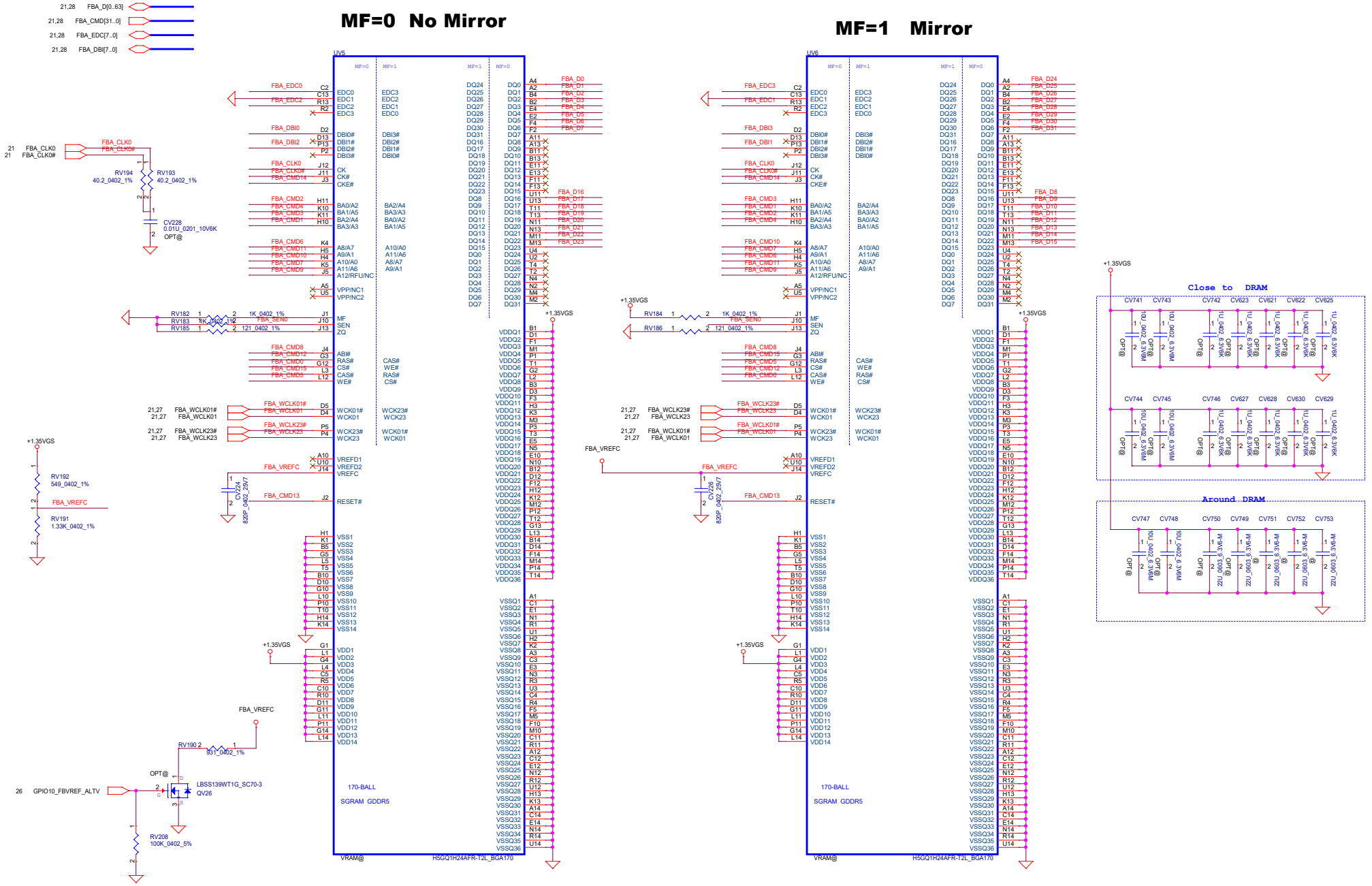
Lower 32 bits



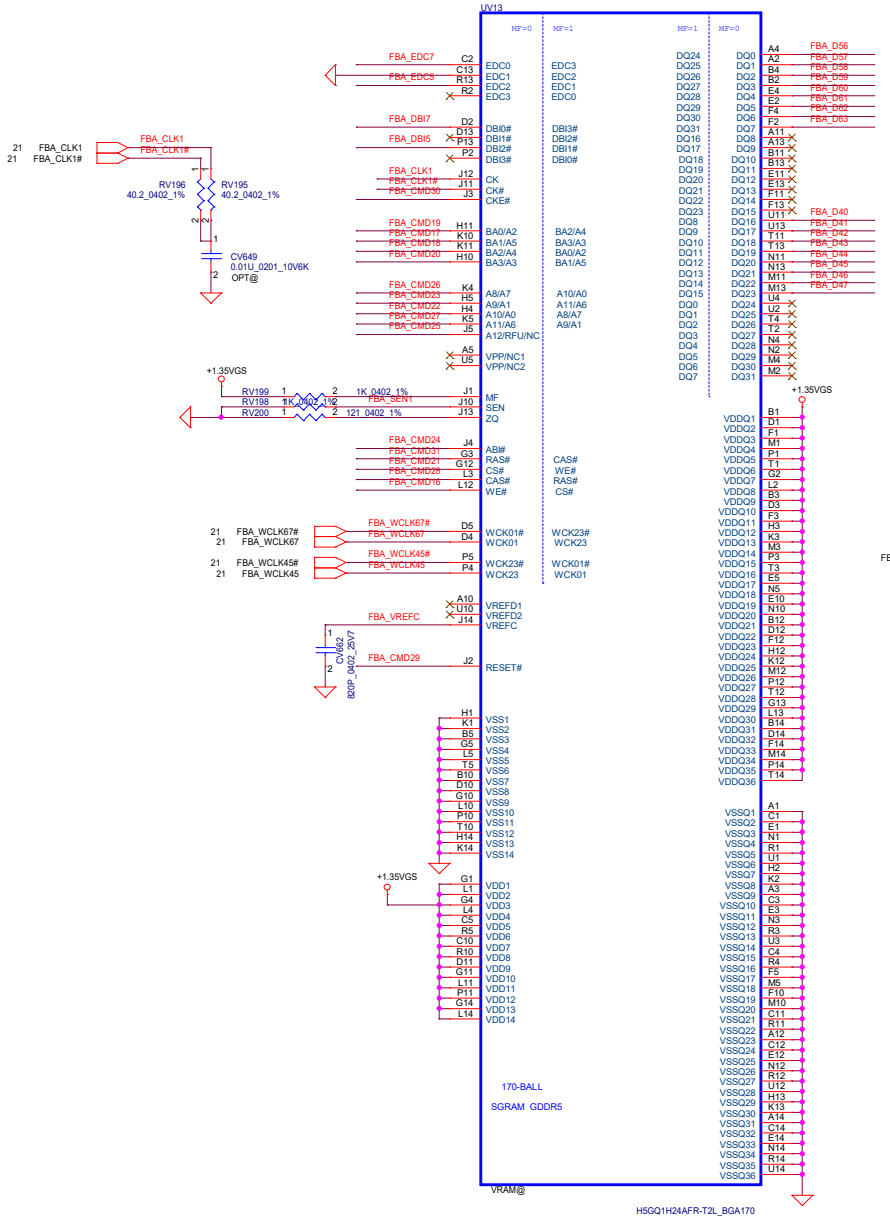
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	N17S_GDDR5_Rank0_[31:0]		
Size C	Document Number EG521		Rev 0.2
Date: Tuesday, April 25, 2017	Sheet 27 of 60		

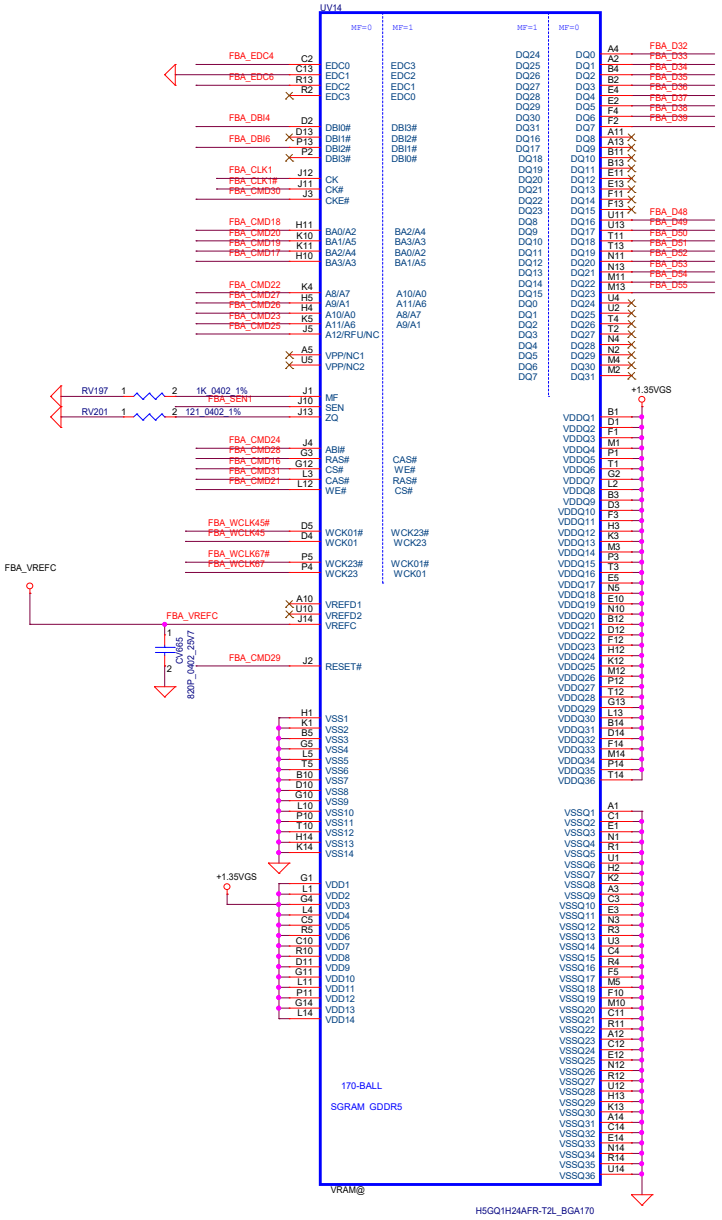
upper 32 bits

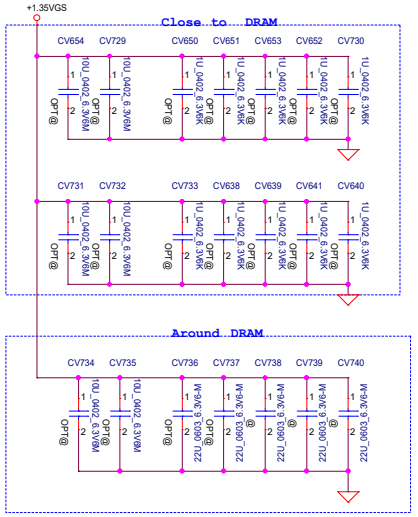
21,27 FBA_D[0..63]
21,27 FBA_CMD[31..0]
21,27 FBA_EDC[7..0]
21,27 FBA_DBI[7..0]

MF=1 Mirror



MF=0 No Mirror





Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: N17S_GDDR5_Rank0_[64:32]

Size	Document Number	Rev
C	EG521	0.2

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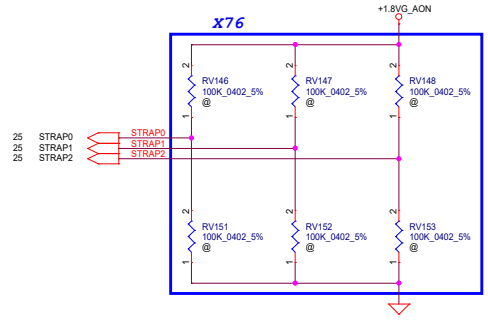
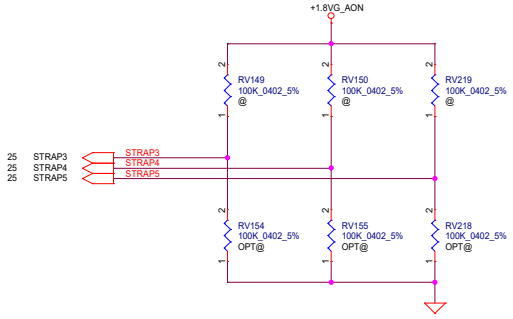


GPU	FB Memory (GDDR5)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-HC28	0(0x0000)	L	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1(0x0001)	L	L	H
	Hynix 8Gb	H5GC8H24MJR-R0C	2(0x0010)	L	H	L
4Gb	Samsung 4Gb	K4G41325FE-HC28	7(0x0111)	H	H	H
	Hynix 4Gb	H5GC4H24AJR-R0C	6(0x0110)	H	H	L
	Micron 4Gb	EDW4032BABG-70-F	8(0x1000)	L	L	M



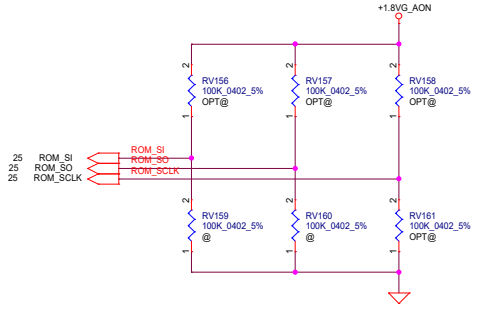
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE



ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
H	H	M	0000

1:ENABLE 0:DISABLE

SOR0/1/2/3 DISABLE

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Title: N16X_MISC

Size	Document Number	Rev
C	EG521	0.2

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Digital power for HDA link

8/29 Add +1.8VS Circuit for Audio wei

Analog power for mixers, & IO ports

Power supply for full-bridge left/Right channel

Power for card reader controller

Analog power for DACs, ADCs

Digital power for digital I/O circuit

Power for combo jack depop circuit at system shutdown mode

To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.

11/8 SIT Vendor suggestion form 47 ohm change to 51om wei

11/8 SIT Cost down to 0ohm wei

8/16 Update Audio Jack P/N SP011509163 wei

Audio Jack

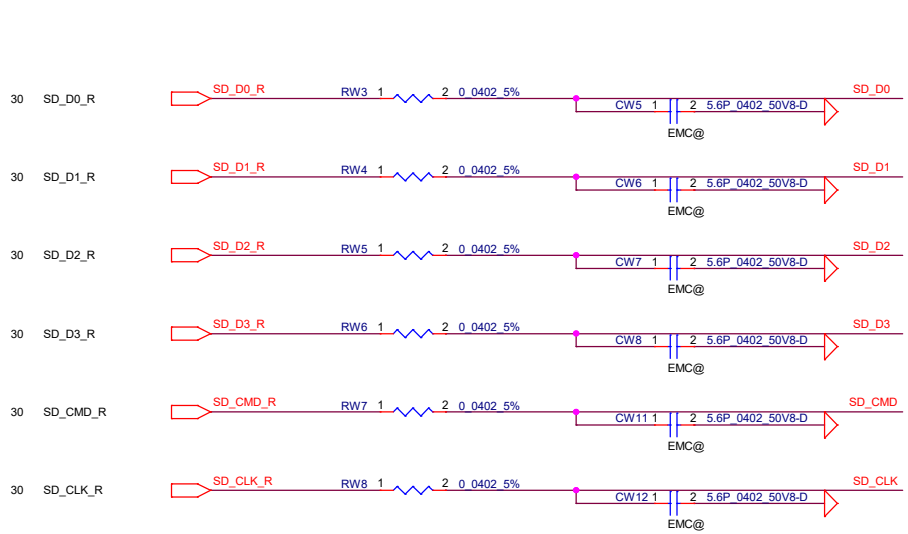
8/16 Update Audio Jack P/N DC021608101 wei

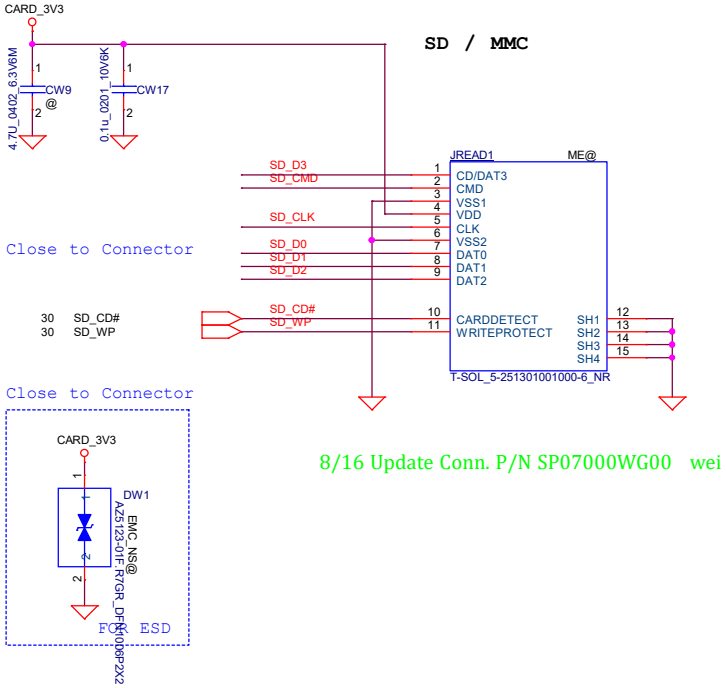
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Codec & CR_RTS5199

Size: C | Document Number: EG521 | Rev: 0.2

Date: Tuesday, April 25, 2017 | Sheet 30 of 60

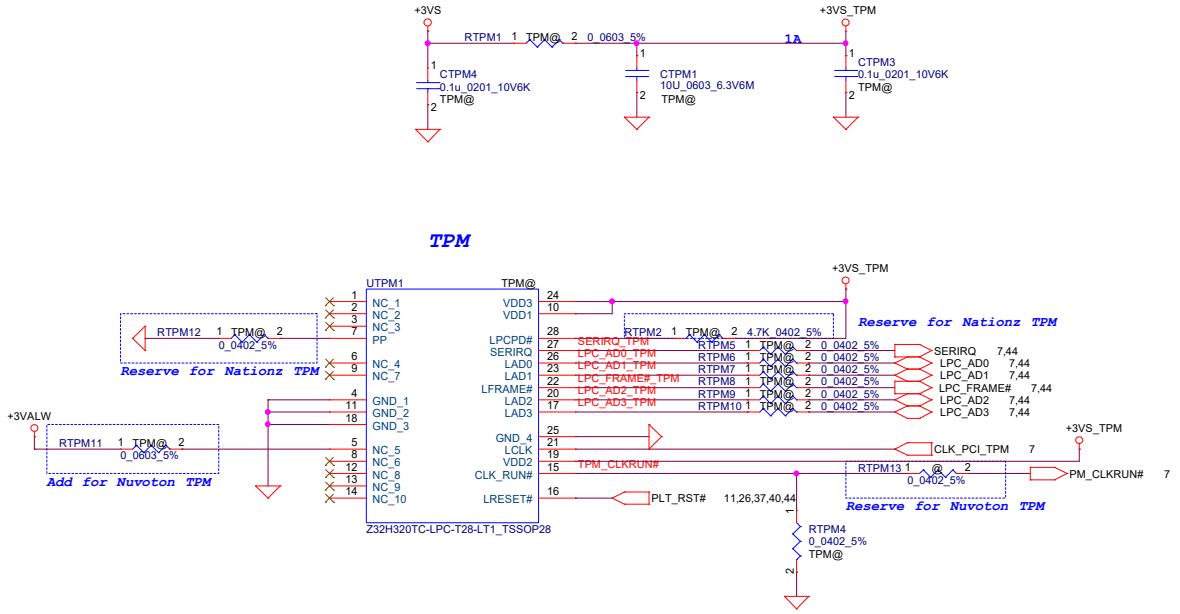




Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Cardreader**

Size: Custom	Document Number: EG521	Rev: 0.2
Date: Tuesday, April 25, 2017	Sheet 31 of 60	



	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: TPM

Size	Document Number	Rev
Custom	EG521	0.2

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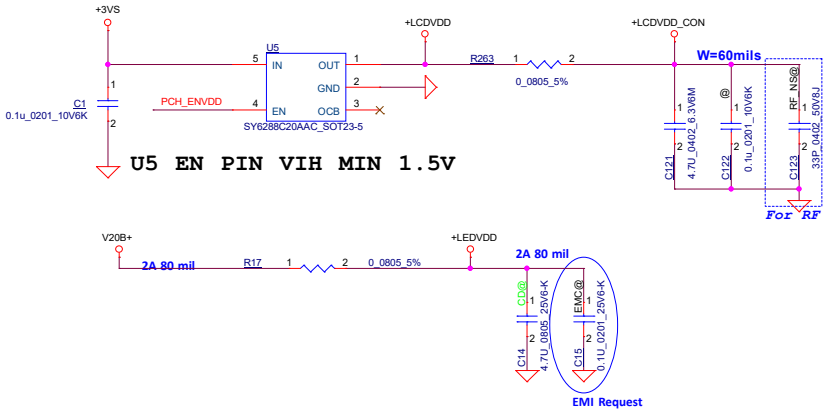
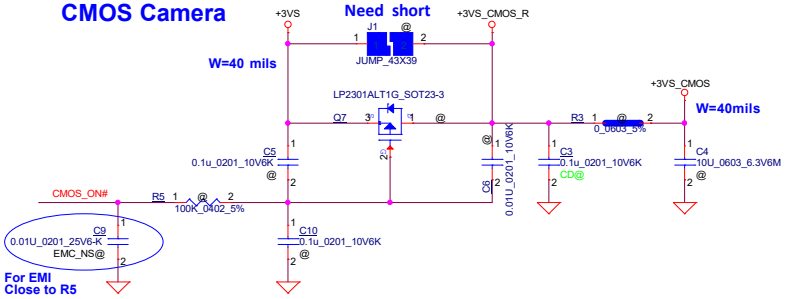
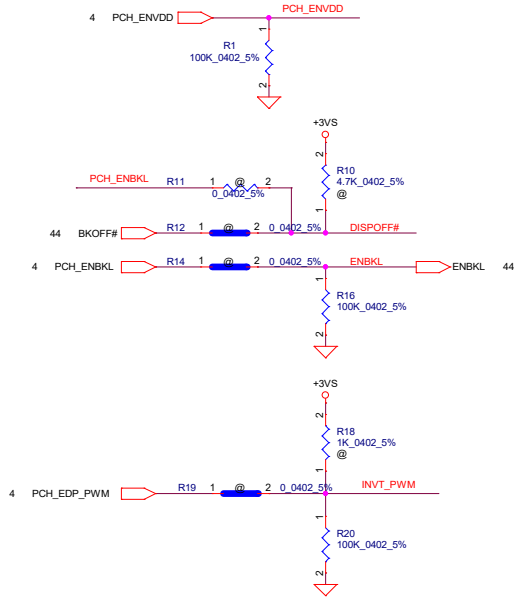
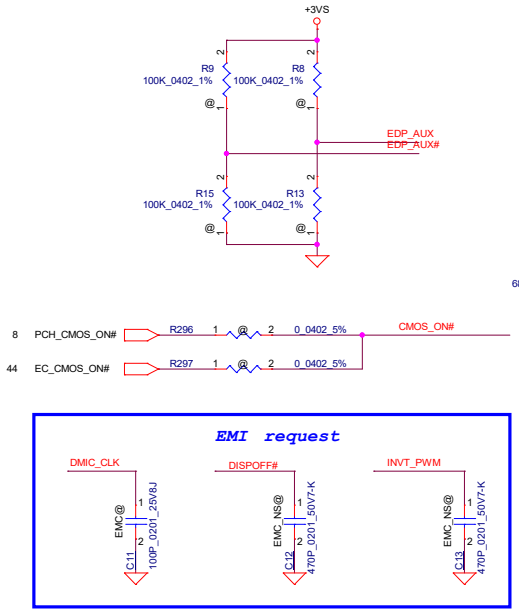
LCD POWER CIRCUIT

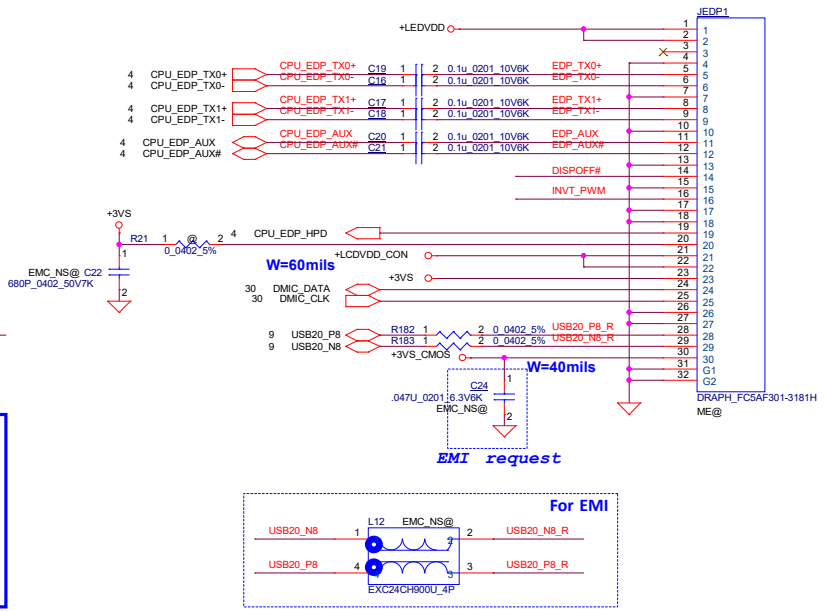


CMOS Camera

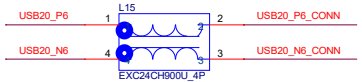




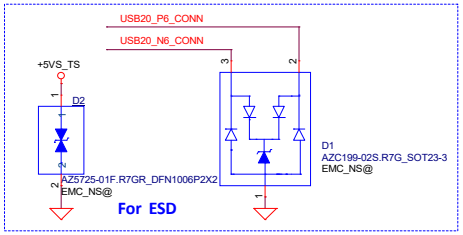


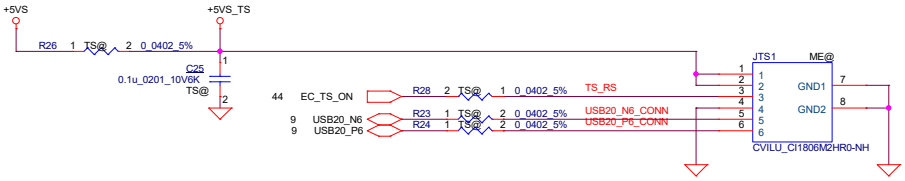


Touch Screen



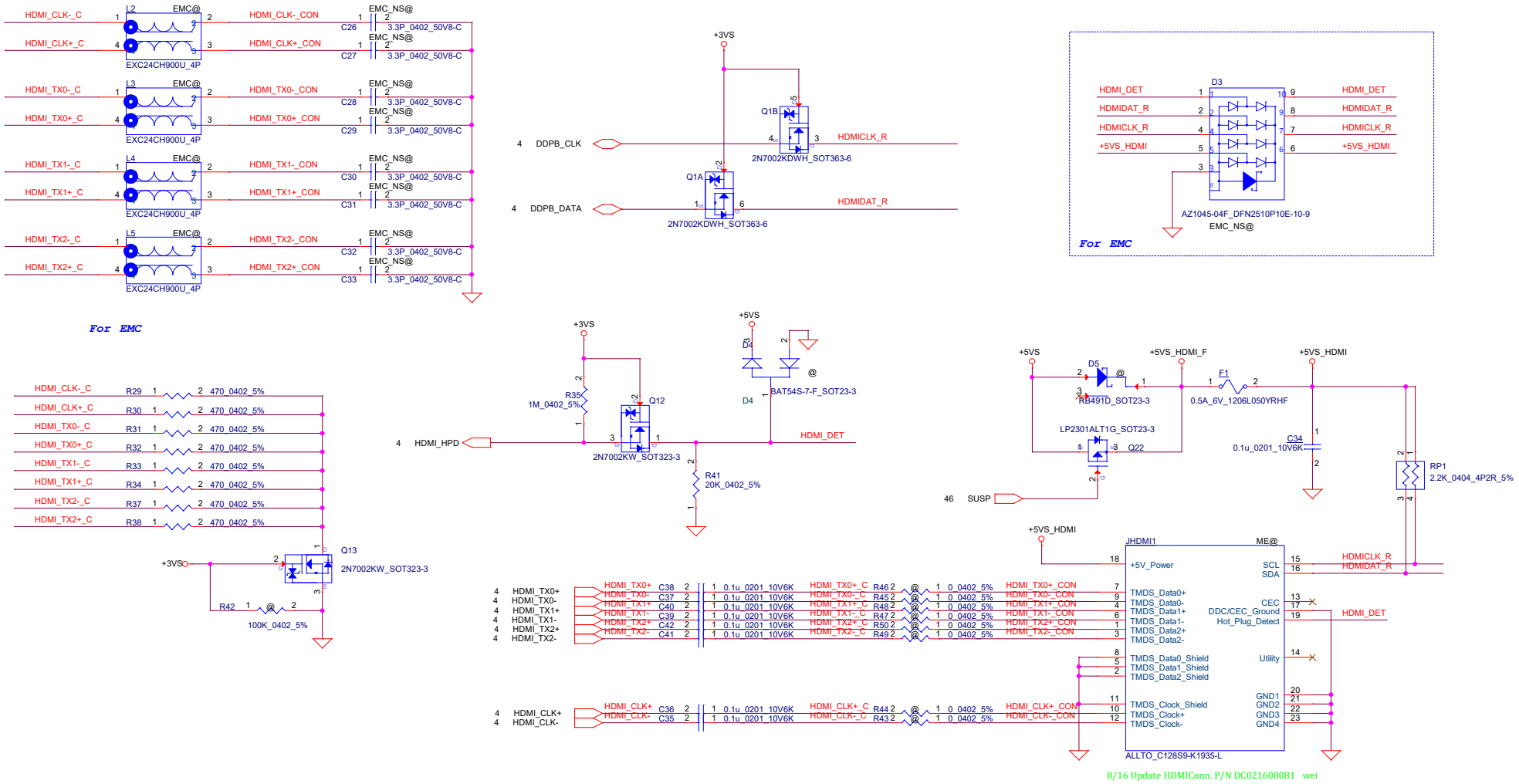
For EMI





Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	eDP/CMOS/Touch screen		
Size: Custom	Document Number: EG521		Rev: 0.2
Date: Tuesday, April 25, 2017	Sheet 33 of 60		



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **HDMI_CONN**

Size	Document Number	Rev
Custom	EG521	0.2

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

P35-Blank

Size	Document Number	Rev
Custom	***EG521***	0.2

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

Blank

Size	Document Number	Rev
Custom	*EG521*	0.2

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+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms < spec < 10.0ms

Need short

width : 40 mils

JUMP_43X79

LP2301ALT1G_SOT23-3

Close to Pin11 Close to Pin32 Close to Pin11 Close to Pin32

manual change the Codec PN to RTL8111GUL-CG

RTL8111GUL-CG QFN 32P
8111GUL@

CL10 close to Pin18
CL11 close to Pin17

For RTL8111GUL(SWR mode, reserved)
For RTL8111H (LDO mode)

Close to Pin3, 8, 22, 30

Close to Pin22(Reserved)

Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

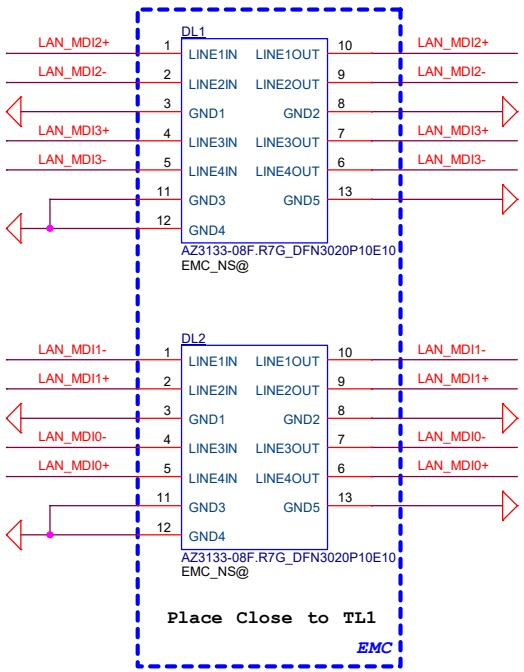
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

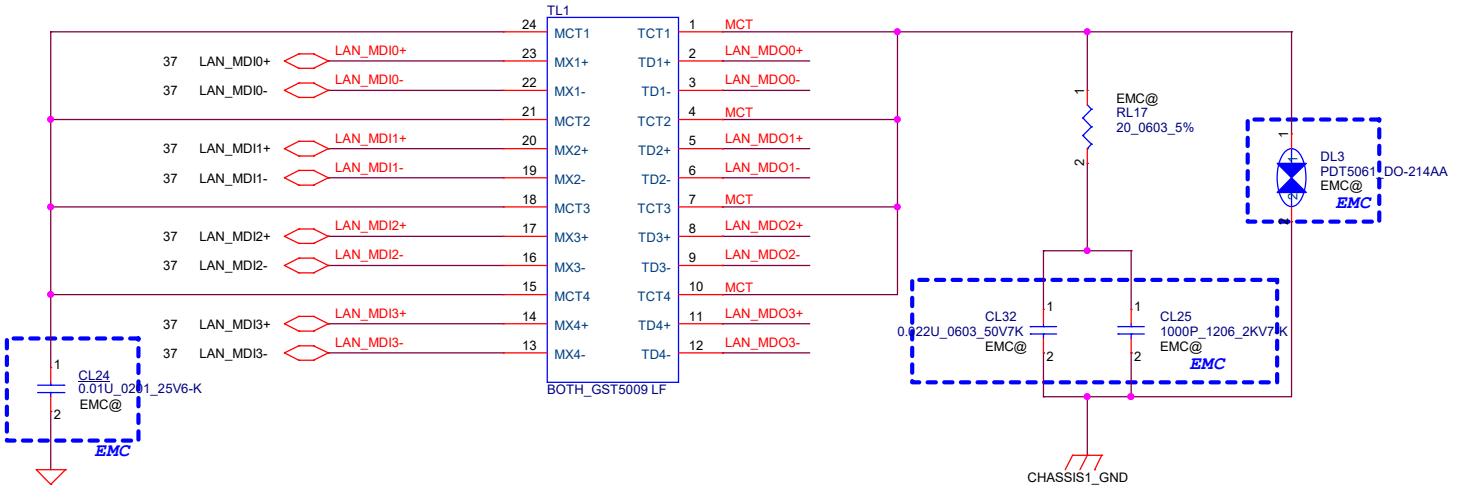
Title: LAN_RTL8111H_CG

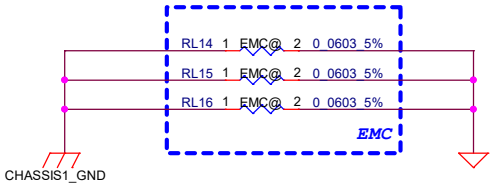
Size: Custom | Document Number: EG521 | Rev: 0.2

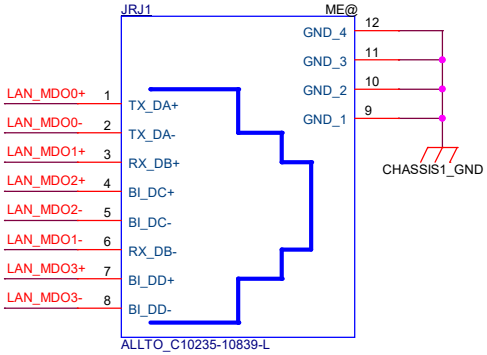
Date: Tuesday, April 25, 2017 | Sheet 37 of 60

DL1/DL2
1'S PN:SC300003M00







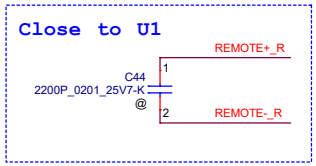


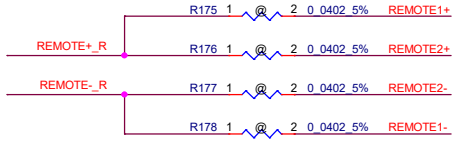
8/16 Update RJ45 P/N DC021608091 wei

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

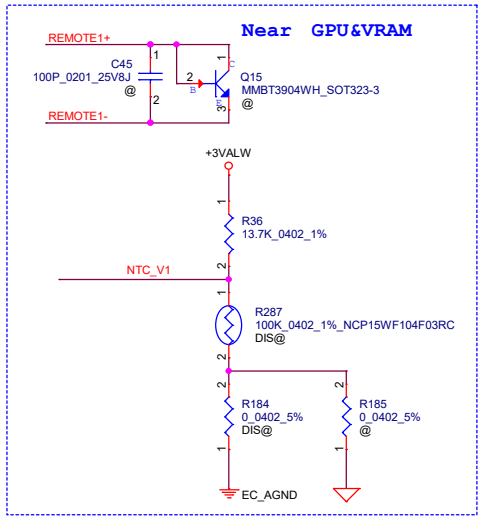
Title: LAN_Transformer

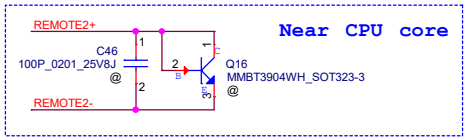
Size	Document Number	Rev
B	EG521	0.2
Date: Tuesday, April 25, 2017	Sheet 38 of 60	

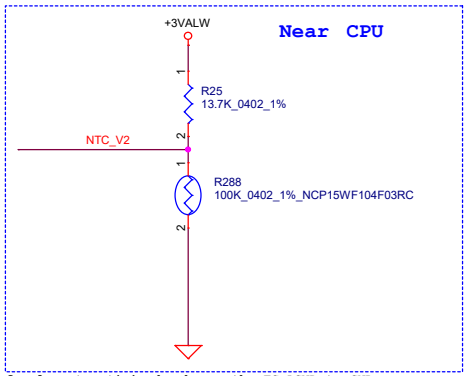




REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

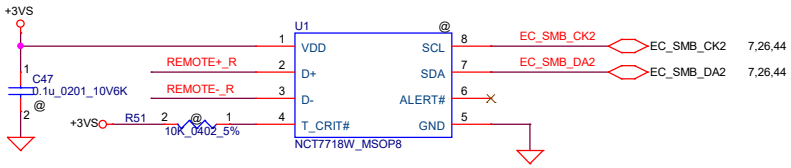






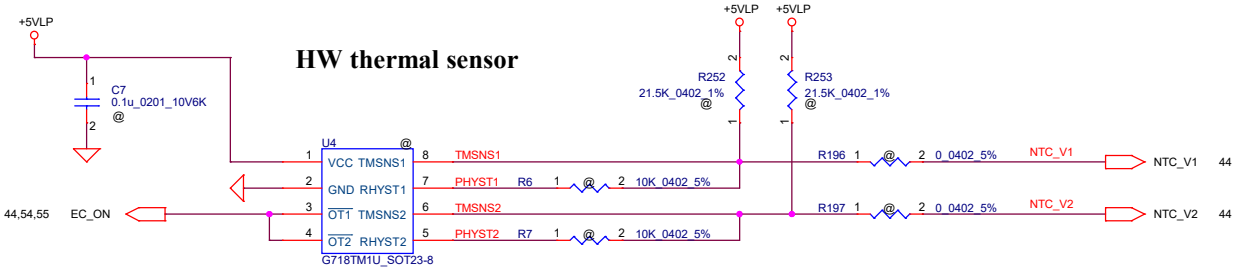
for layout optimized, change the EC_AGND to GND

SMSC thermal sensor placed near DIMM



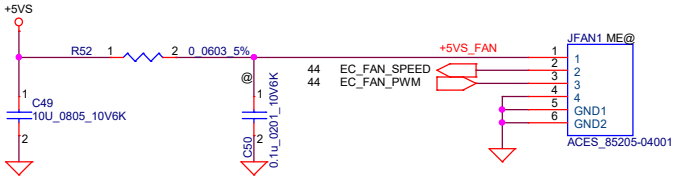
Address 1001_101xb

HW thermal sensor



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

FAN Conn



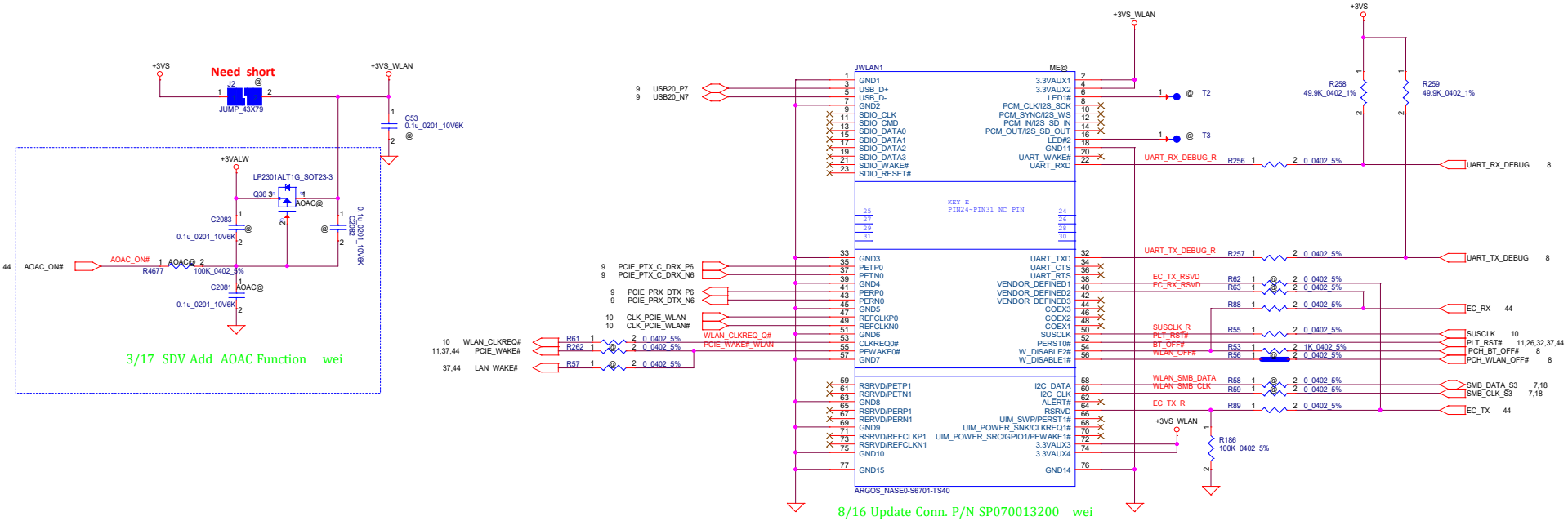
Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title: *Thermal sensor/FAN CONN*

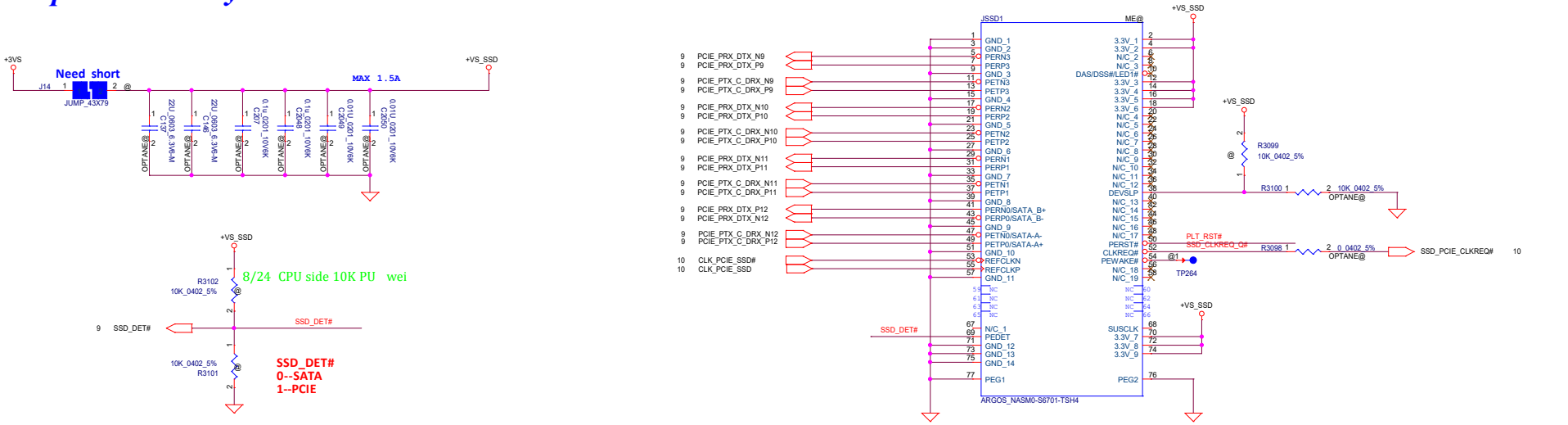
Size	Document Number	Rev
Custom	*EG521*	0.2

Date: Tuesday, April 25, 2017 Sheet 39 of 60

Mini-Express Card(WLAN/WiMAX)



Optane Memory



Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

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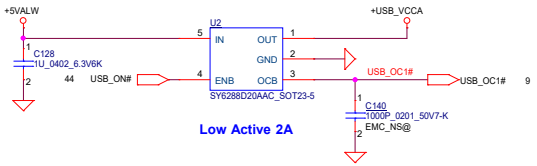
Title: NGFF WLAN&SSD

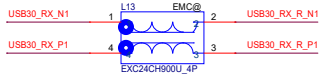
Size	Document Number	Rev
C	EG523	0.2

Date: Tuesday, April 25, 2017 Sheet 40 of 60

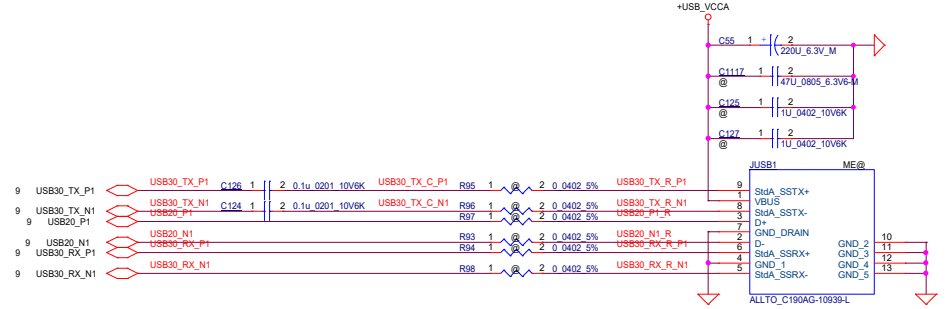
LEFT SIDE USB3.0 PORT x2



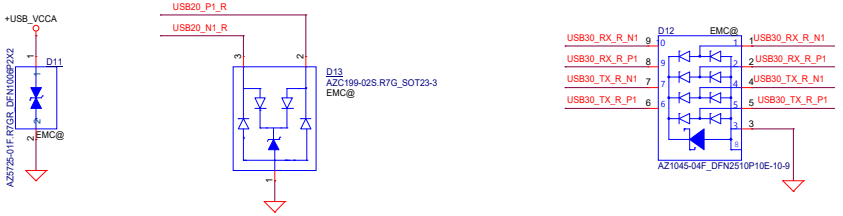
Low Active 2A



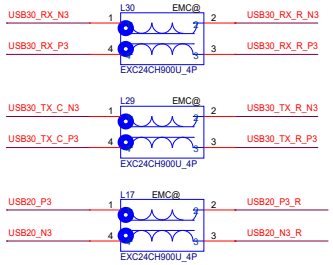
EMC

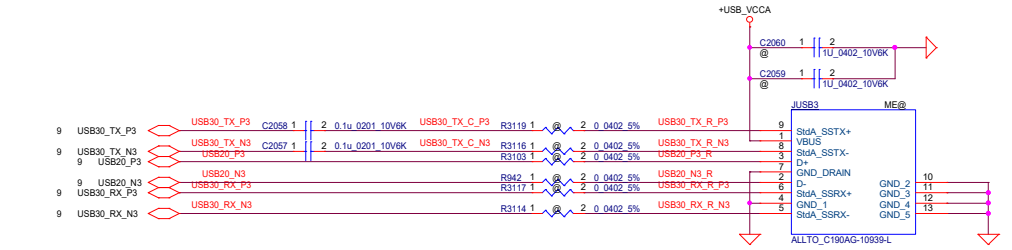


09/05 Update USBConn. P/N DC021609011 wei



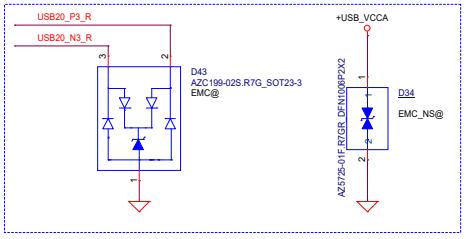
EMC

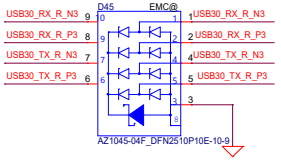




09/05 Update USBConn. P/N DC021609011 wei

FOR ESD Close to Connector

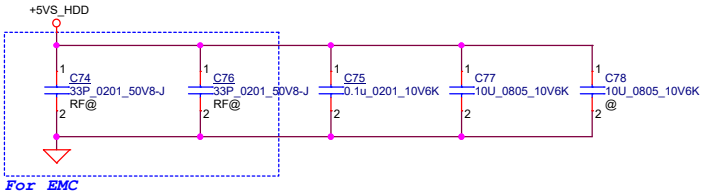


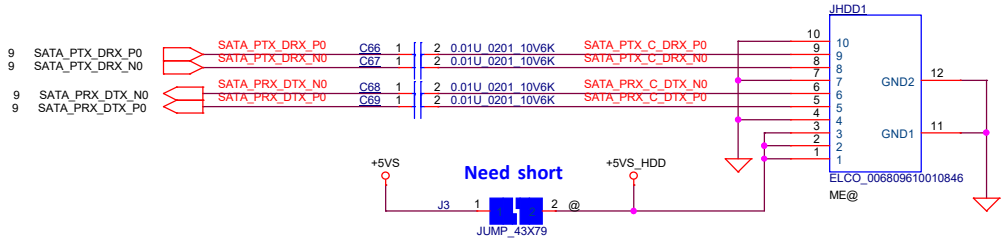


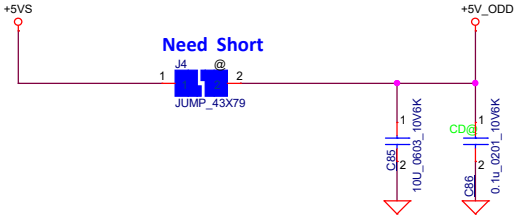
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	USB3.0 PORT (LEFT)		
Size C	Document Number EG521		Rev 0.2
Date: Tuesday, April 25, 2017		Sheet 41 of 60	

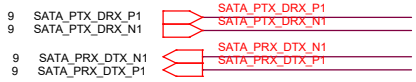
SATA HDD Conn.



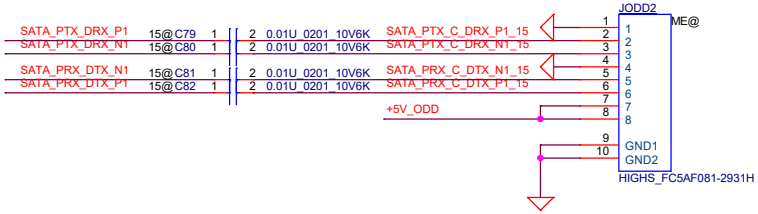




FOR 14"
SATA ODD Conn.



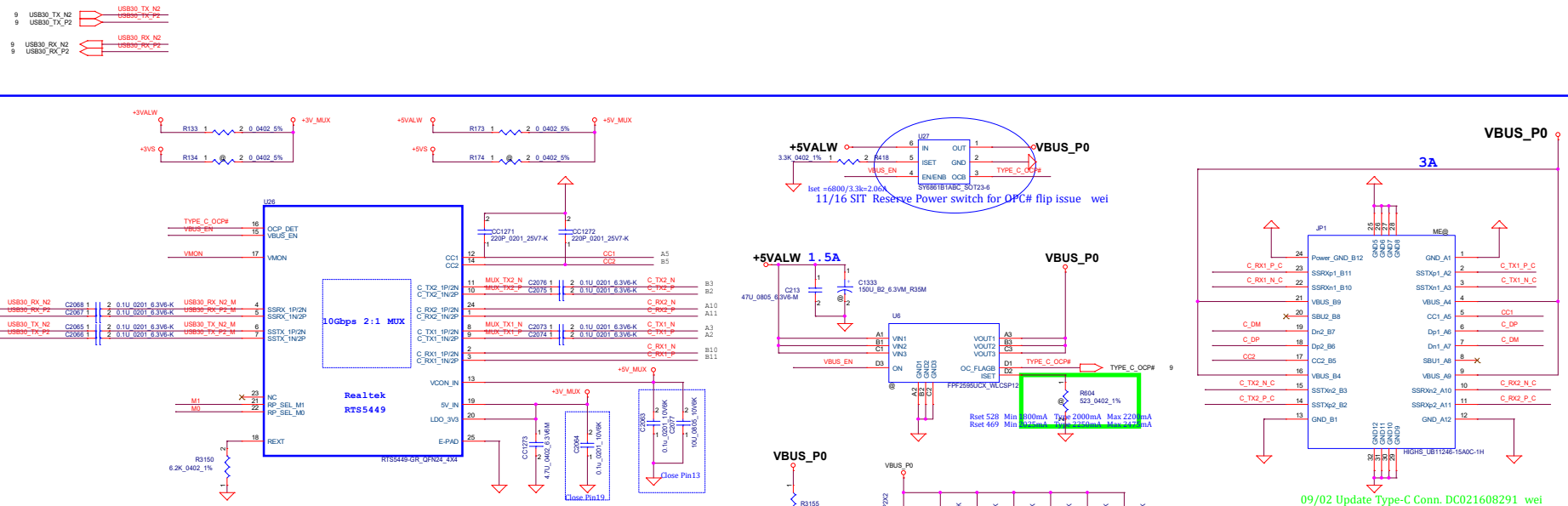
FOR 15" 17"
SATA ODD FFC Conn



8/16 Update Conn. P/N SP01001YV00 wei

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	HDD/ODD CONN		
Size: Custom	Document Number: EG521		Rev: 0.2
Date: Tuesday, April 25, 2017	Sheet 42 of 60		



Rp configuration

Rp:1.5A (now)

	M1	M0	Note
Rp:900mA	0	1	R3144/R3142 mount
Rp:1.5A	1	0	R3139/R3143 mount
Rp:3.0A	1	1	R3139/R3142 mount

For C_VBUS power switch enable pin

Power switch enable pin	Note
Low Active	R3146 mount
High Active	R3141 mount

For C_VBUS power switch OCP pin

PH at CPU side 09/06 wei

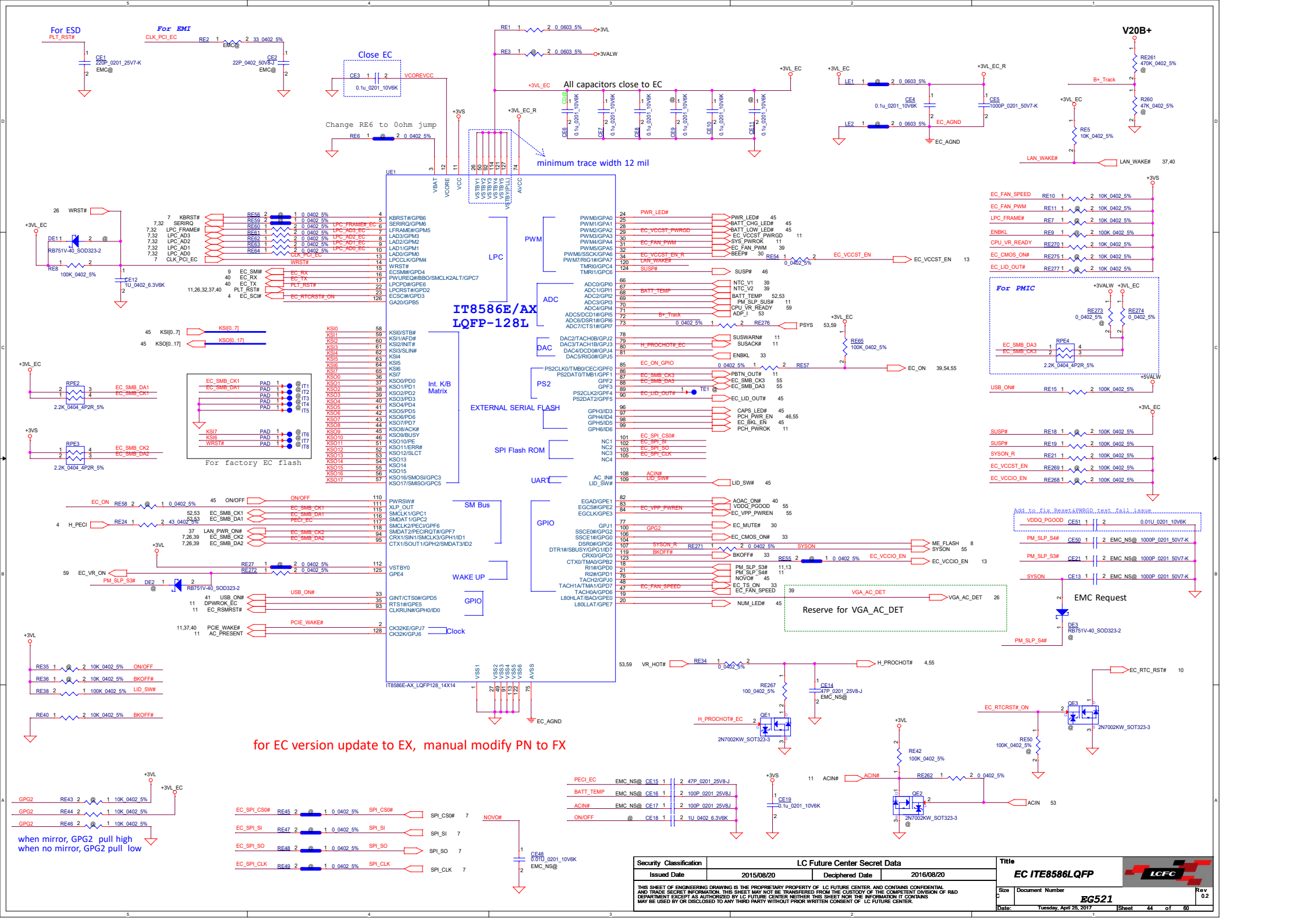
Power switch OCP pin	Note
Low Active	R3147 mount
High Active	R3140 mount

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: 3D Camera

Size: Custom | Document Number: EG521 | Rev: 0.2

Date: Tuesday, April 25, 2017 | Sheet 43 of 60


V20B+
IT8586E/AX
LQFP-128L
IT8586E-AX_LQFP128_14X14
Close EC
All capacitors close to EC
Change RE6 to 0ohm jump
minimum trace width 12 mil
For ESD
For EMI
For PMIC
For factory EC flash
Reserve for VGA_AC_DET
EMC Request
for EC version update to EX, manual modify PN to FX
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2016/08/20
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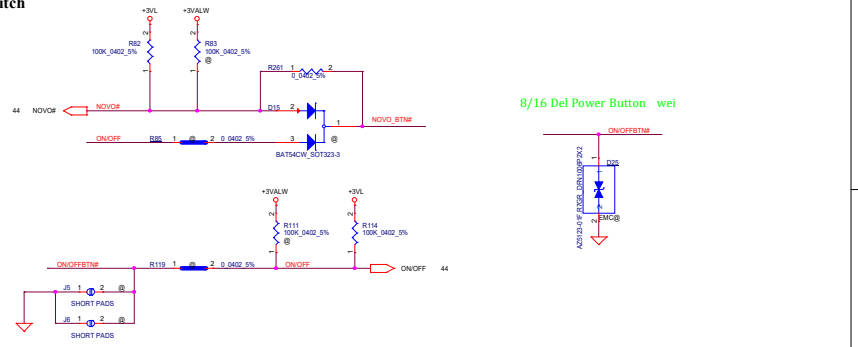
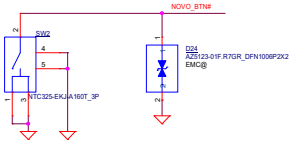
Title
EC ITE8586LQFP
Size
C
Document Number
EG521
Rev
0.2
Date:
Tuesday, April 25, 2017
Sheet
44
of
60

ON/OFF switch



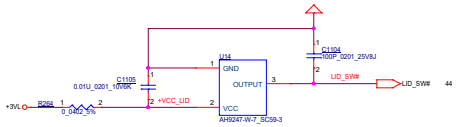
8/16 Del Power Button wei

Novo button

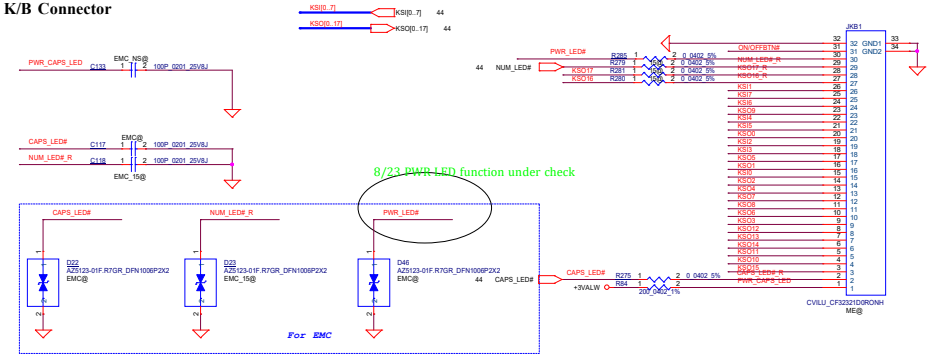


8/31 Update the P/N SN100008W00 wei

LID switch

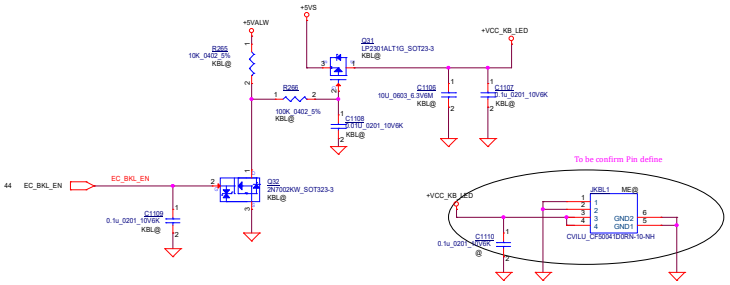


K/B Connector



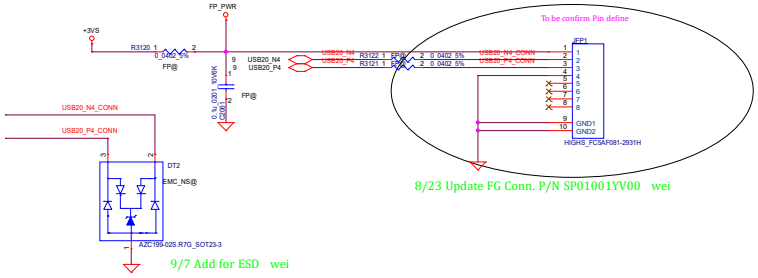
8/23 PWR LED function under check

KB Backlight Connector



8/31 Update KBL Conn. P/N SP011608241 wei

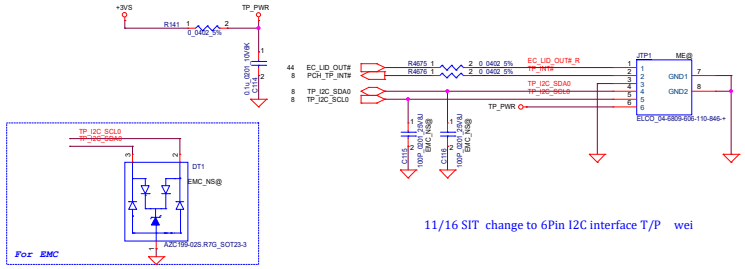
Finger Print Connector



8/23 Update FG Conn. P/N SP01001YV00 wei

9/7 Add for ESD wei

TP/B Connector



11/16 SIT change to 6Pin I2C interface T/P wei

PWR_LED Change to M/B (310->320) 08/17

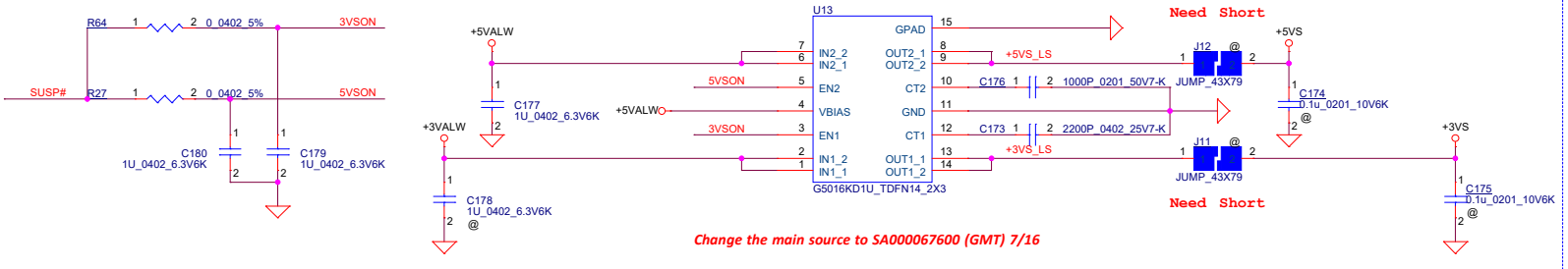
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	KBD/PWR/IO/LED/TP Conn.		
Size: Custom	Document Number: EG521		Rev: 0.2
Date: Tuesday, April 25, 2017	Sheet 45 of 60		

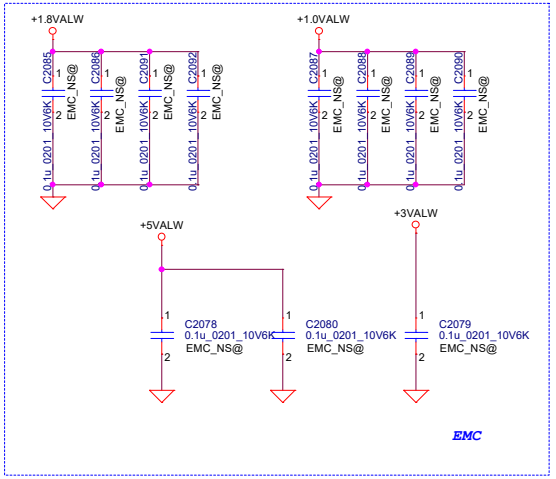
Load Switch
+5VALW To +5VS
+3VALW To +3VS

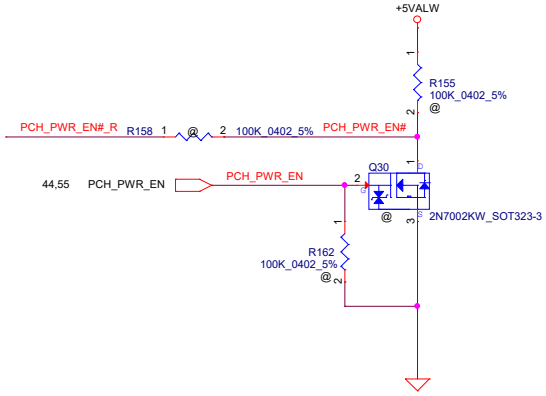
+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

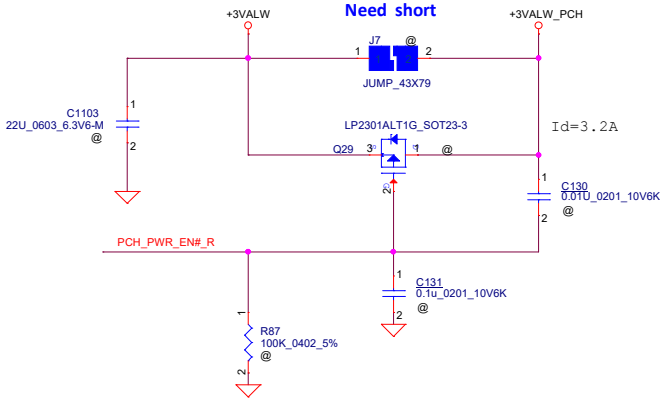
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

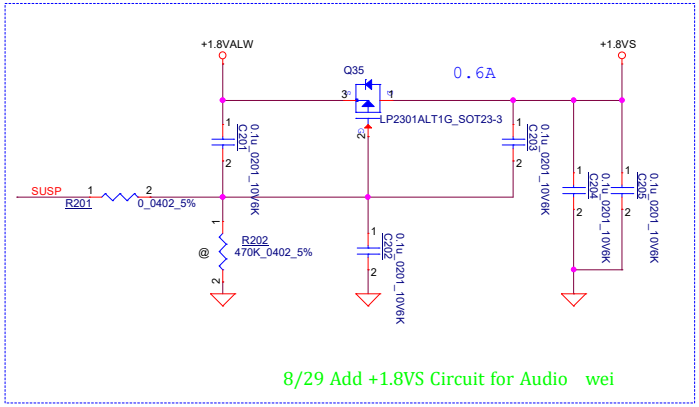


Change the main source to SA000067600 (GMT) 7/16

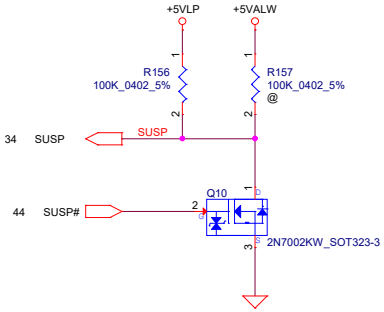




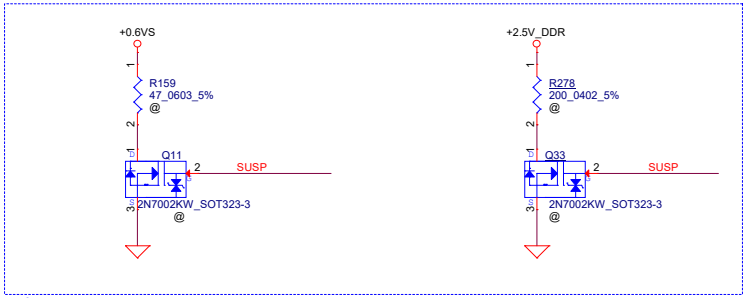




8/29 Add +1.8VS Circuit for Audio wei



For DisCharge

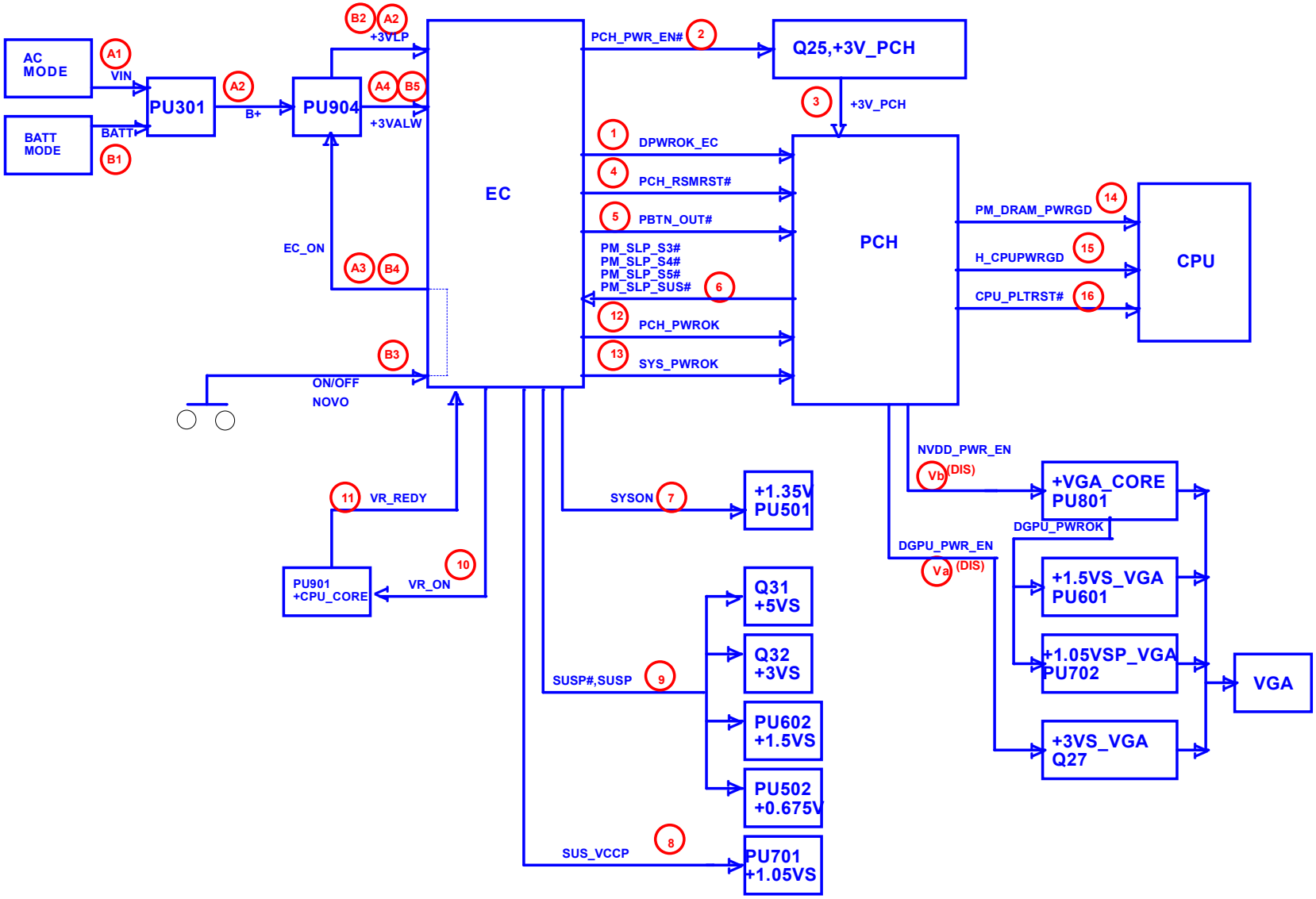


08/29: Need double check enable signal and the resistance

Title: **DC V TO VS INTERFACE**

Size	Document Number	Rev
Custom	EG521	0.2

Date: Tuesday, April 25, 2017 Sheet 46 of 60



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: *Power sequence block*

Size: Custom	Document Number: EG521	Rev: 0.2
Date: Tuesday, April 25, 2017	Sheet 47 of 60	

Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/30	Deciphered Date	2016/08/30

Title

Virtual symbol

Size	Document Number	Rev
A1	*EG521*	1.0

Date: Tuesday, April 18, 2017 Sheet 45 of 45

CPU Thermal Holex3

H1 HOLEA — pad_c6p0d4p0
H2 HOLEA — pad_c6p0d4p0
H3 HOLEA — pad_c6p0d4p0

GPU Thermal Holex2

H4 HOLEA — pad_c7p0d3p3
H5 HOLEA — pad_c7p0d3p3

Close to RJ45

H6 HOLEA — CHASSIS1_GND, pad_ct7p0b8p0d3p0

Close to Audio jack

H7 HOLEA — pad_ct7p0b8p0d3p0

PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

DC-IN x2

H10 HOLEA — pad_ct5p5d2p5

WLAN Standoff

H11 HOLEA — pad_ct7p0b6p0d3p3
H12 HOLEA — pad_ct7p0d3p0
H13 HOLEA — pad_ct7p0d3p0
H15 HOLEA — pad_ct5p0d2p5
H16 HOLEA — pad_cb5p5d2p5

H17 HOLEA — pad_o2p6x2p9d2p6x2p9n
H18 HOLEA — PAD_CT7P0D3P0
H19 HOLEA — PAD_CT7P0D3P0
H20 HOLEA — pad_c3p3d3p3n
H22 HOLEA — PAD_C2P6D2P6N

USB3.0 Shielding

SH1 ME@ — SPRING_FINGER_6.2X1.64
SH2 ME@ — SPRING_FINGER_6.2X1.64
SH3 ME@ — SPRING_FINGER_6.2X1.64
SH4 ME@ — SPRING_FINGER_6.2X1.64
SH5 ME@ — SPRING_FINGER_6.2X1.64
SH6 ME@ — SPRING_FINGER_6.2X1.64

DDR4 Shielding

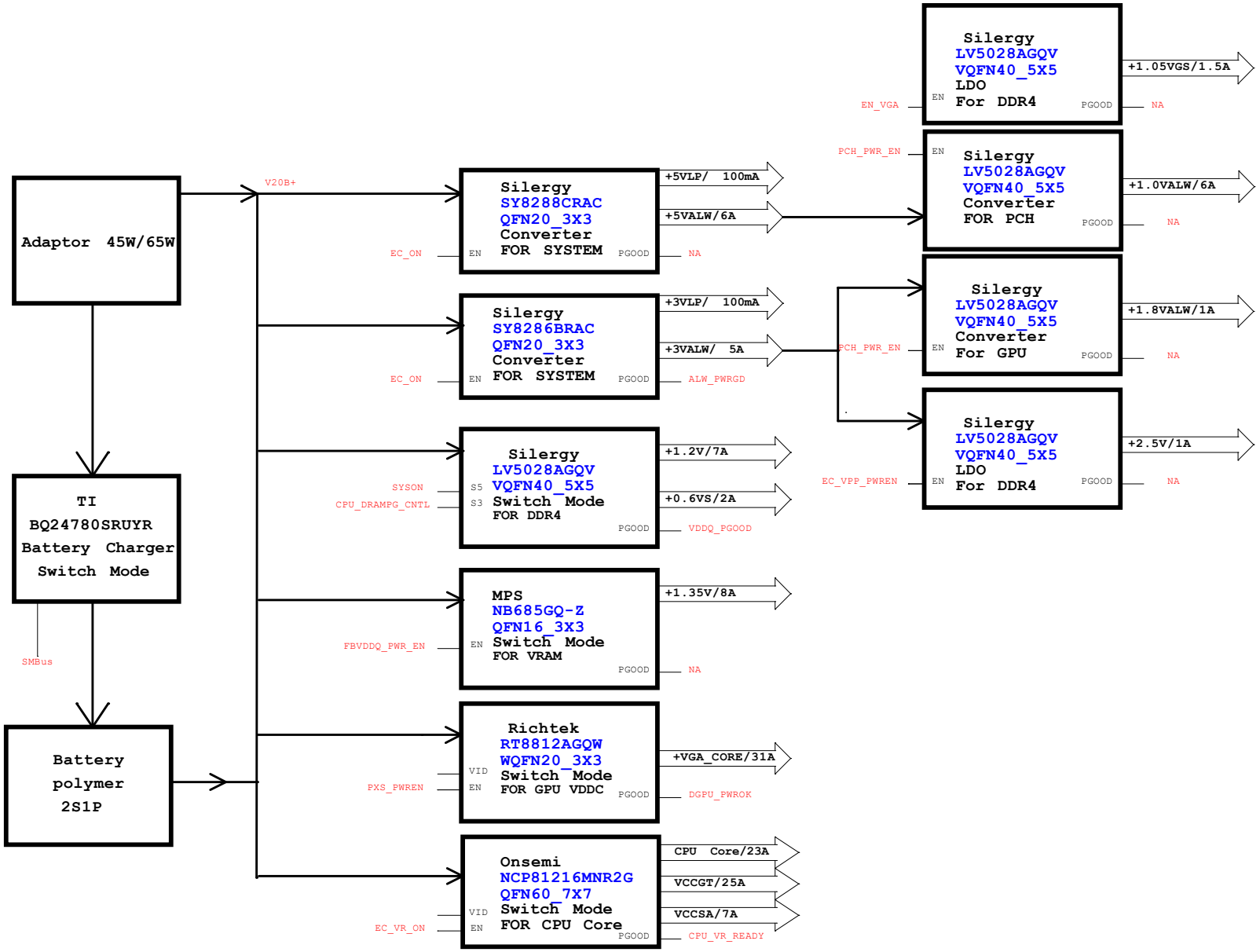
SH12 ME@ — SPRING_FINGER_6.2X1.64
SH7 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH8 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH14 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH13 ME@ — SPRING_FINGER_6.2X1.64
SH9 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH10 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH11 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Hole

Size	Document Number	Rev
B	EG521	0.2

Date: Tuesday, April 25, 2017 Sheet 49 of 60

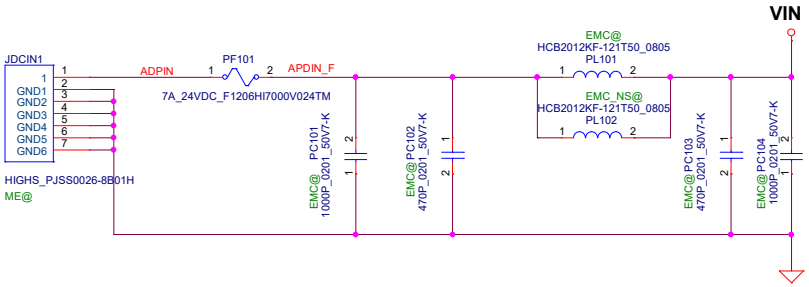


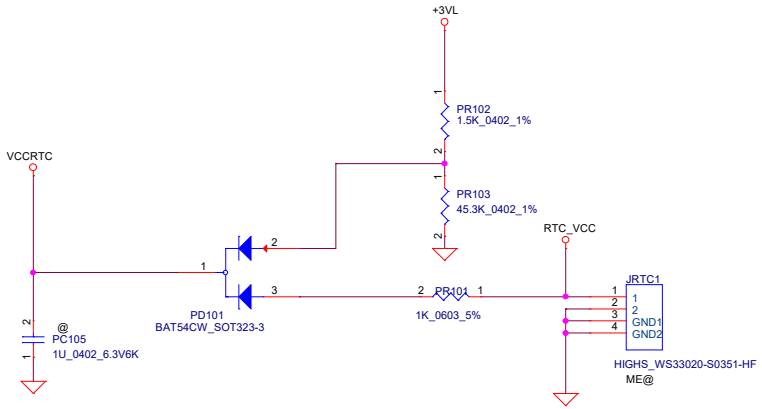
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR-Power Diagram

Size	Document Number	Rev
Custom	CG411	0.1

Date: Tuesday, April 25, 2017 Sheet 50 of 60





RTC_VCC 20MIL
+3VL 20MIL
VCCRTC 20MIL

No charge RTC with 35mm cable

RTC Battery for GCM BOM
(2nd source and quoted price)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR-DCIN / RTC charger

Size: Custom	Document Number: CG411	Rev: 0.1
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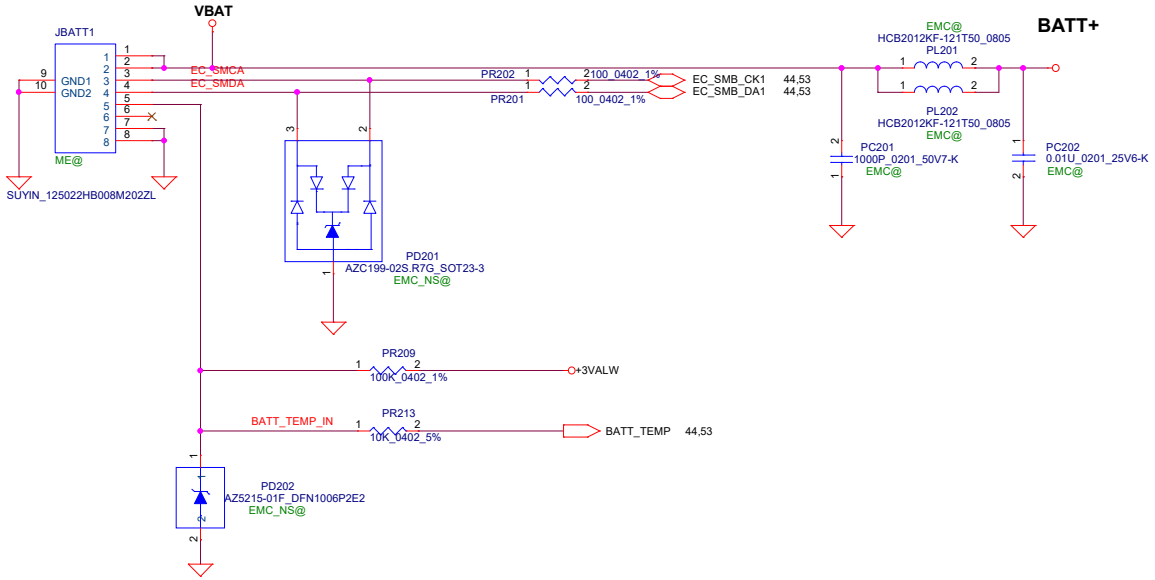

2S1P polymer battery voltage level: +6V ~ 8.4 V

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR-BATTERY CONN/OTP

Size	Document Number	Rev
Custom	CG411	0.1

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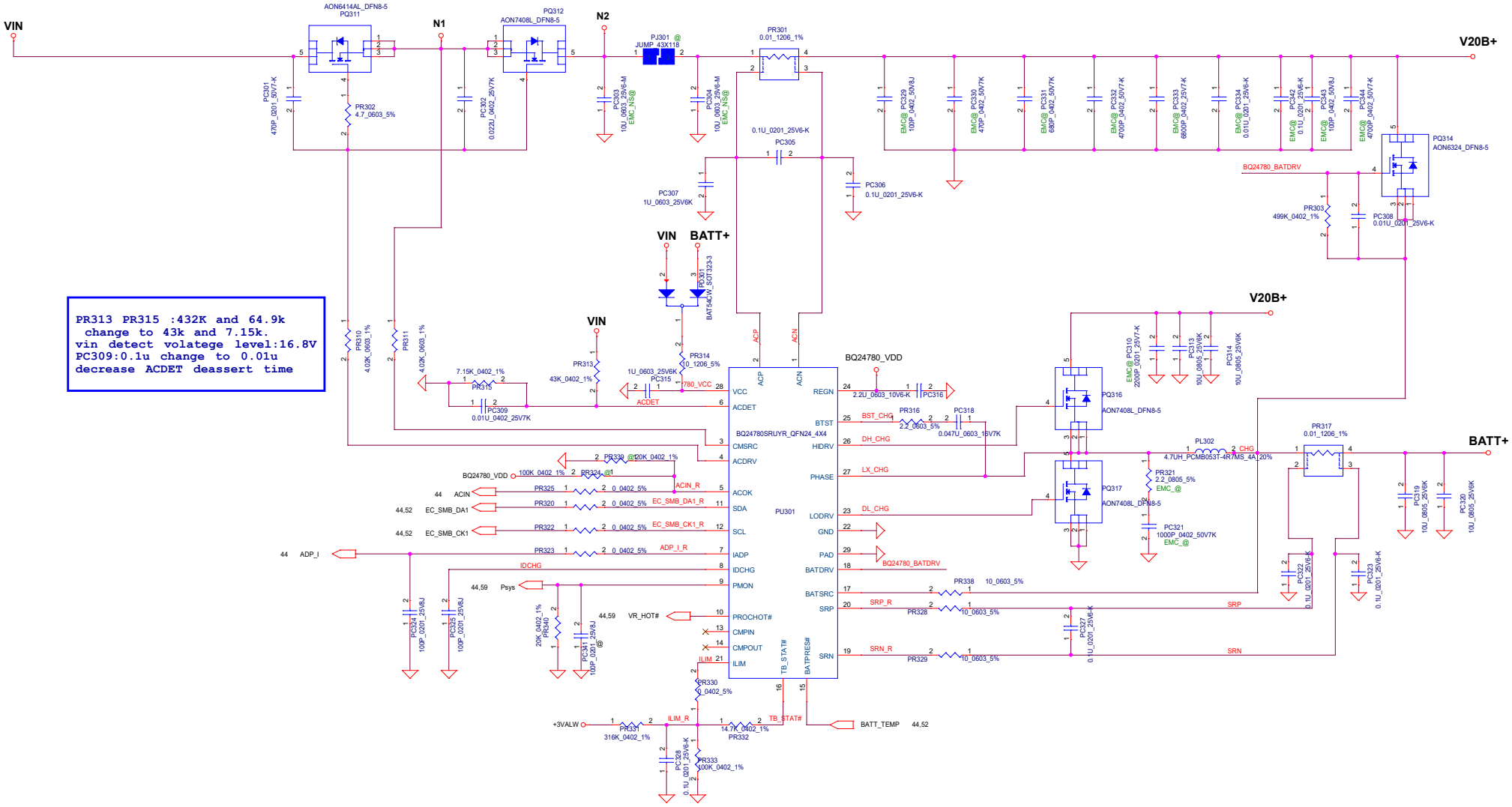
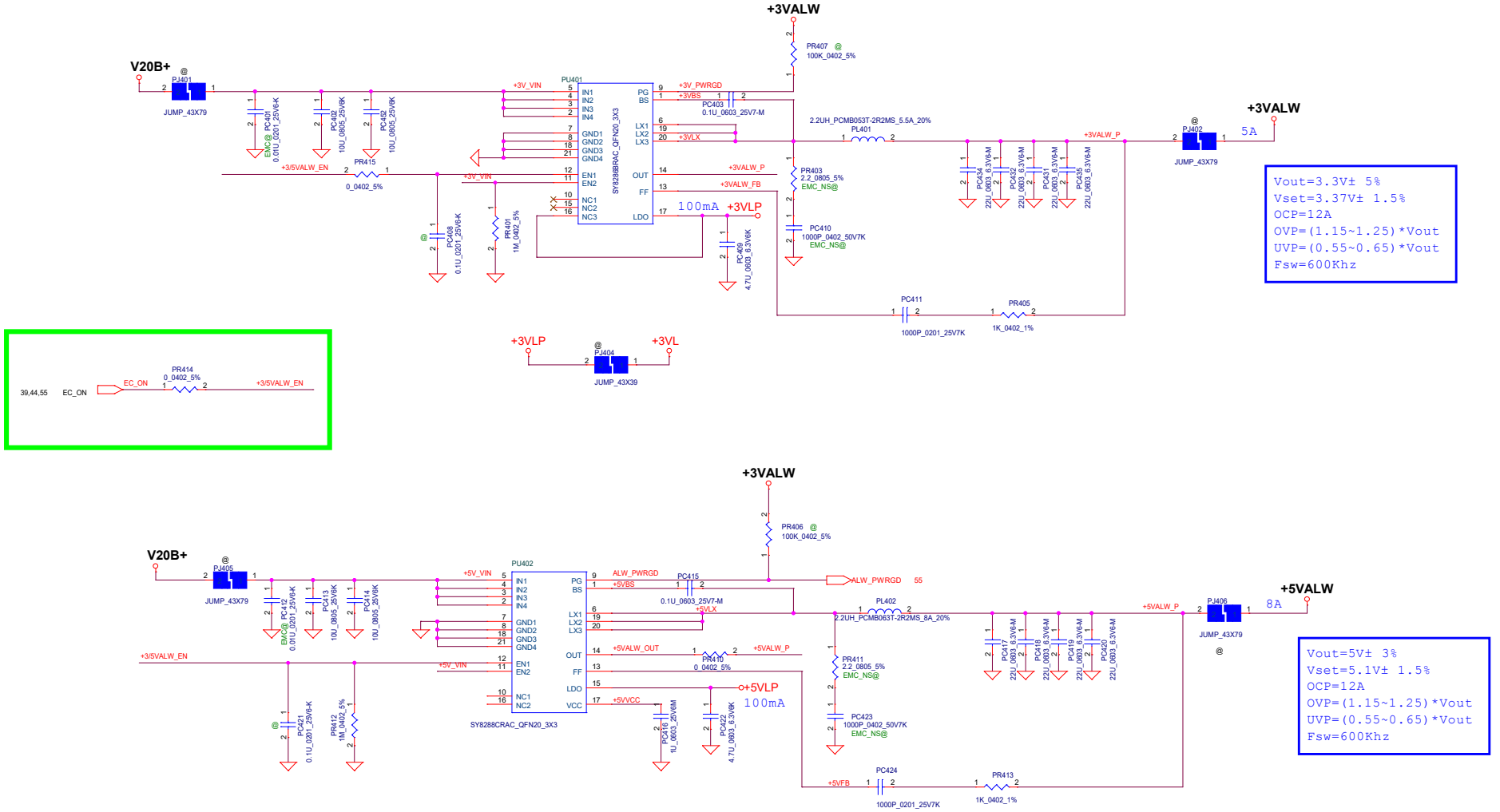


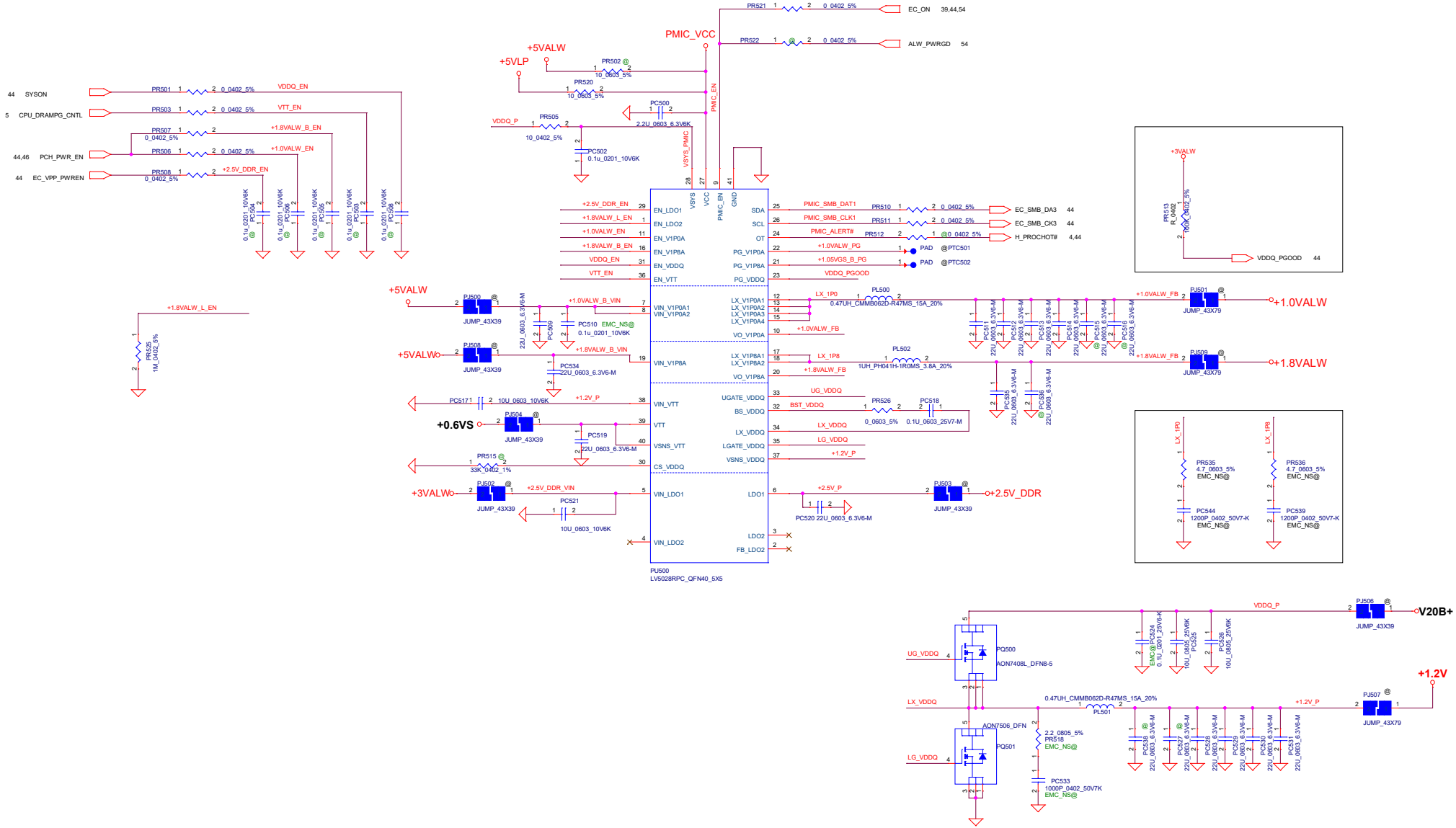
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	PWR-CHARGER		
Size	Document Number		Rev
C	CG411		0.1
Date:	Tuesday, April 25, 2017	Sheet	53 of 60



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	PWR_3VALW/5VALW		
Size	Document Number		Rev
C	CG411		0.1
Date:	Tuesday, April 25, 2017	Sheet	54 of 60



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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: PWR PMIC-DDR4/1.0ALW/1.8ALW

Size	Document Number	Rev
A2	CG411	0.1

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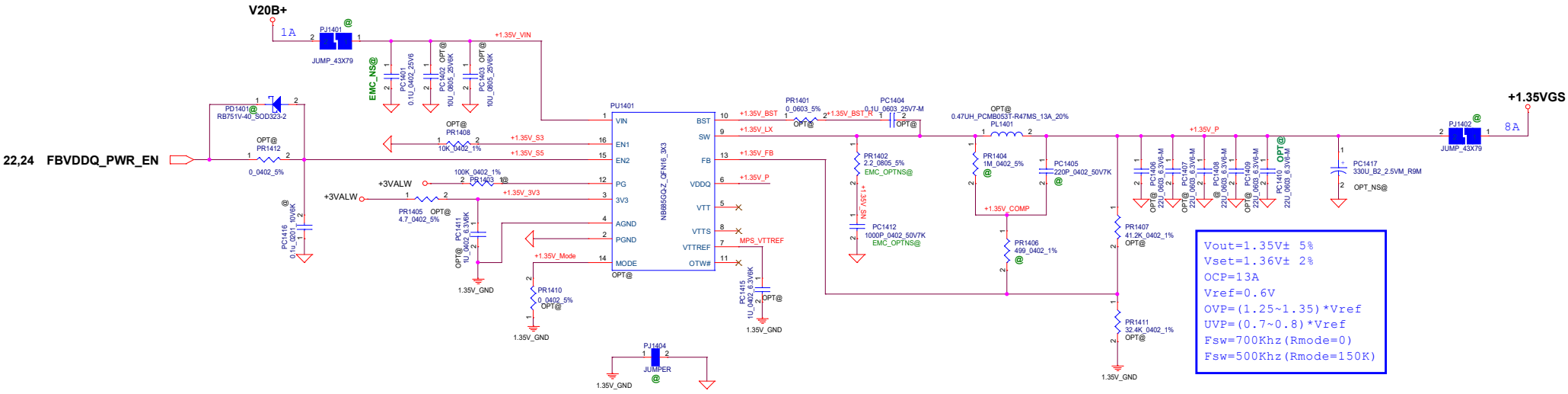
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

PWR

Size	Document Number	Rev
Custom	CG411	0.1

Date: Tuesday, April 25, 2017 Sheet 56 of 60



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR-+1.05VGS/+1.35V_VRAM

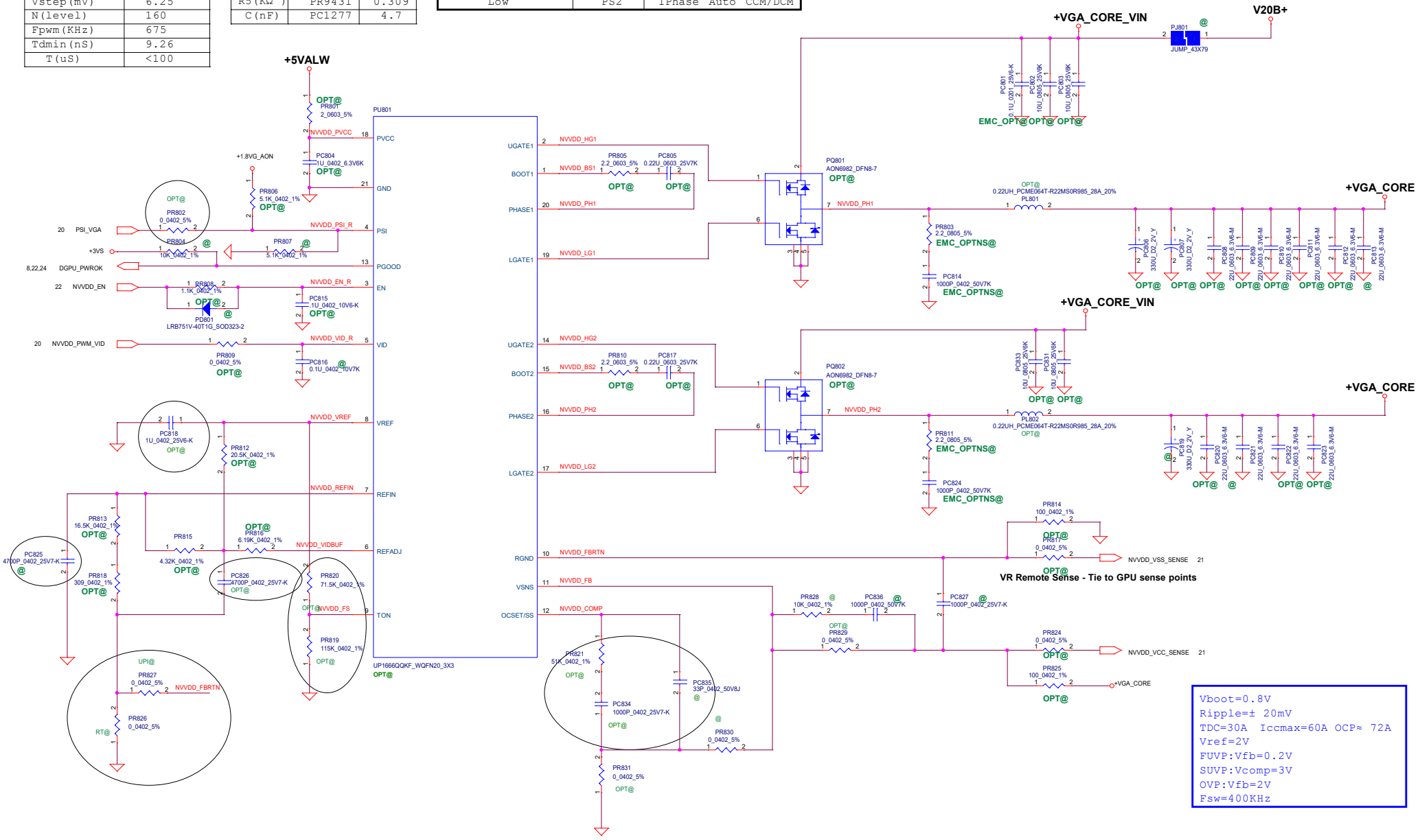
Size	Document Number	Rev
C	CG411	0.1

Date: Tuesday, April 25, 2017 Sheet 57 of 60

PWM-VID Specification	
	Config
Vmin(V)	0.3
Vmax(V)	1.3
Vboot(V)	0.8
Vstep(mV)	6.25
N(level)	160
Fpwm(KHz)	675
Tdmin(nS)	9.26
T(uS)	<100

Component	Value	
R1(KΩ)	PR9440	6.19
R2(KΩ)	PR9434	20.5
R3(KΩ)	PR9436	4.32
R4(KΩ)	PR9437	16.5
R5(KΩ)	PR9431	0.309
C(nF)	PC1277	4.7

PSI Level	Power Mode	Phase Configuration
Connected to PVCC	PSH	2Phase Auto CCM/DCM
High	PS0	2Phase FCCM
Intermediate	PS1	2Phase Auto CCM
Low	PS2	1Phase Auto CCM/DCM



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR-VGA_CORE

Size	Document Number	Rev
C	CG411	0.1

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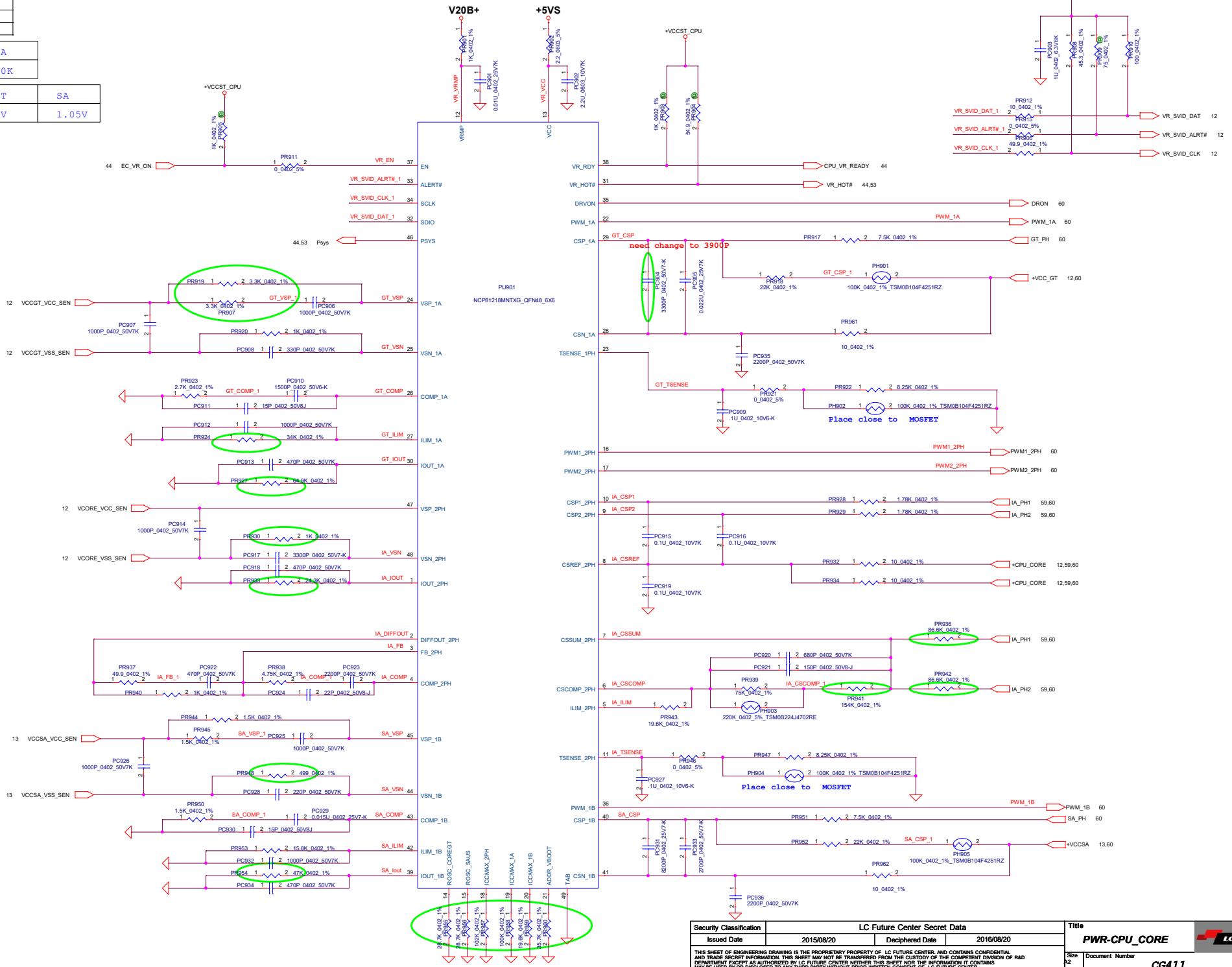
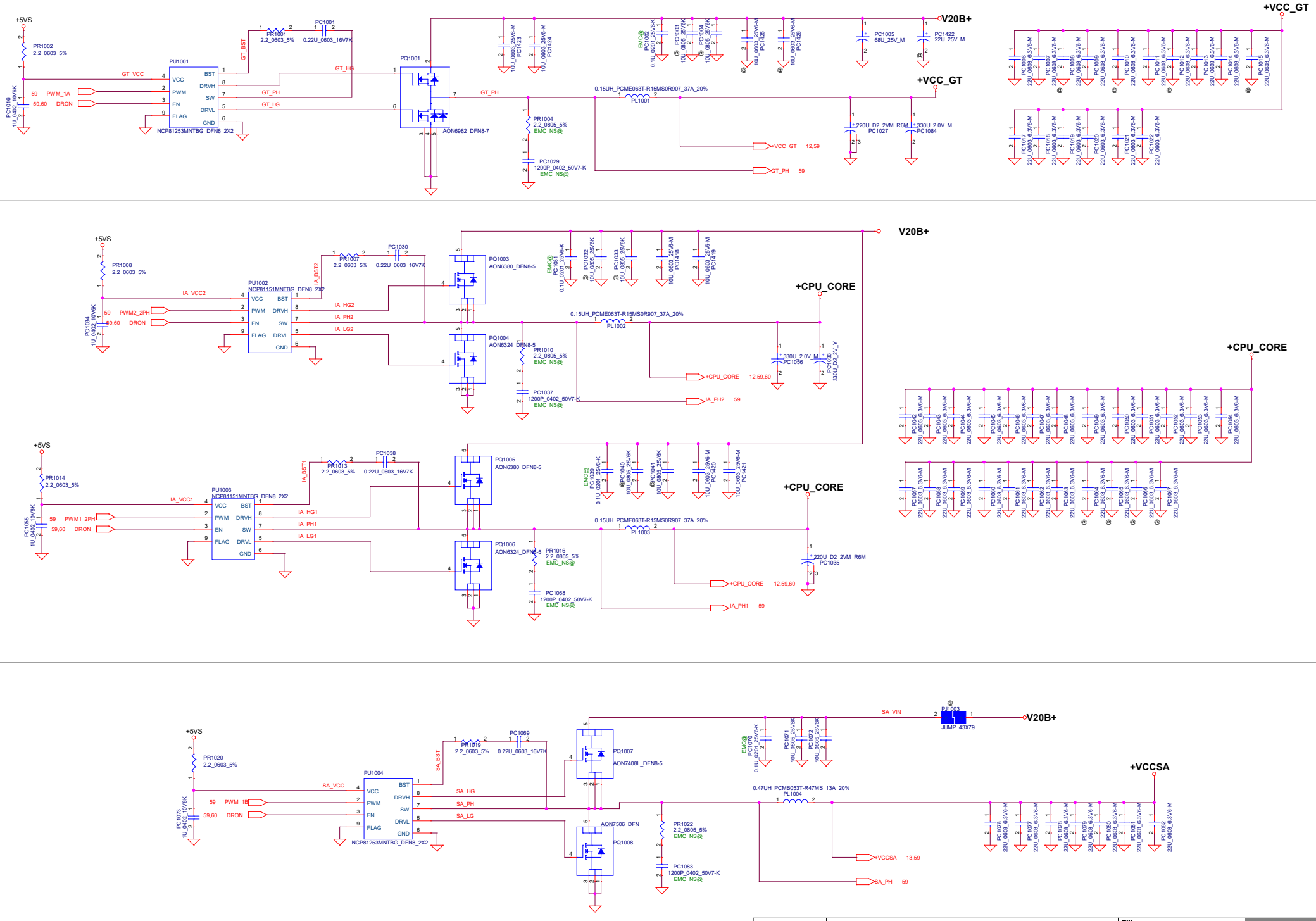
SVID Specification	
	Config
Vmin(V)	0
Vmax(V)	1.52
Vstep(mV)	5

RFsw	Core/GT	SA
28.7K	550K	550K

RVboot	Core	GT	SA
35.7K	0V	0V	1.05V





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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: PWR-CPU_CORE

LCFC

Size: A2 | Document Number: CG411 | Rev: 0.1

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