DW70 CALPELLA N11P-GE1 Schematics

uFCPGA Mobile Arrandale/Clarksfield

Intel Ibex Peak-M

2009-02-03

REV : -1

DY : Nopop Component
UMA : Pop when schematic is UMA
DIS : Pop when schematic is DIS
ARD : Pop when schematic is Arrandale
CFD : Pop when schematic is Clarksfield

CFD DIS

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Title: *Cover Page*

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Winery CALPELLA Block Diagram

PCB LAYER

L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

Project code : 91.4RU01.001
Part Number : 48.4RU06.0SA
PCB P/N : 09290
Revision : -1

Clock Generator
SLG8SP585 7

VRAM(gDDR3)
64Mbx16x8 (1GB)
84,85,89,90

VRAM

Nvidia
N11P-GE1(40nm)
80,81,82,83

100MHz/
2.5Gbps
PCIe x 16
Bandwidth
:8GB

Intel CPU
Arrandale
Clarksfield
8,9,10,11,12,13,14

DDRIII Channel A
Arrandale 800/1066MHz
Clarksfield 1066/1333MHz

DDRIII DM1 18
Arrandale 1066MHz
Clarksfield 1333MHz

DDRIII Channel B
Arrandale 800/1066MHz
Clarksfield 1066/1333MHz

DDRIII DM2 19
Arrandale 1066MHz
Clarksfield 1333MHz

HDMI 57
CRT 55
LCD 54

HDMI
RGB CRT
LVDS

Switchable

(Dual Channel)

DMIx4
FDI

Intel
PCH

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
20,21,22,23,24,25,26,27,28

PCIE x 1
10/100/1000LOM
RTL8111DL
RJ45 CONN
(On LAN board)

Power SW
TPS2231R
New Card
(On I/O board)

PCIE
100MHz
2.5Gbps

PCIE x 1 USB 2.0 x 1

Mini-Card
802.11a/b/g/n 64

Left Side:
USB x 2
63

USB 2.0
480Mbps

SM Bus
400KHz

Free fall sensor 40

Right Side:
USB x 2
(On LAN board)

CAMERA
(Option) 73

Bluetooth
(On Audio board)

Biometric 78

1394 Connector
(8 in 1)SD/MMC
MS/MS Pro/xD
(On I/O board)

CardReader
1394
RICOH
R5U230

PCIE
100MHz
2.5Gbps

Digital Mic Array
(Option)

HD AUDIO
CODEC
OP AMP
IDT
92HD79

HD AUDIO

MIC IN
HP OUT
(On Audio board)

2CH SPEAKER

LPC Bus
33MHz

DEBUG BOARD
GOLDEN FINGER 70

KBC
NUVOTON
NPCE781BA0DX 37

SPI
SM Bus

Thermal
& Fan
EMC2102 39,58

Capacity Board

SATA, USB
SATA
SPI

USB,ESATA
Multi-Port x1
63

ODD
HDD 59

Flash ROM
4MB

Flash ROM
256kB 62

Touch
PAD 68

Int.
KB 68

CFD DIS

CPU DC/DC
ISL62883 47,48

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC
RT8205BGQW 46

INPUTS	OUTPUTS
+PWR_SRC	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC
TPS51116 50

INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC
ADP3211 53

INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

SYSTEM DC/DC
TPS51218 86

INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

CHARGER
BQ24745 45

INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC
TPS51218 49

INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM DC/DC
TPS51117 52

INPUTS	OUTPUTS
+PWR_SRC	+1.05V_PCH

LDO
APL5930 51

INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

LDO
RT9025 87

INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN_GPU

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Title: Block Diagram

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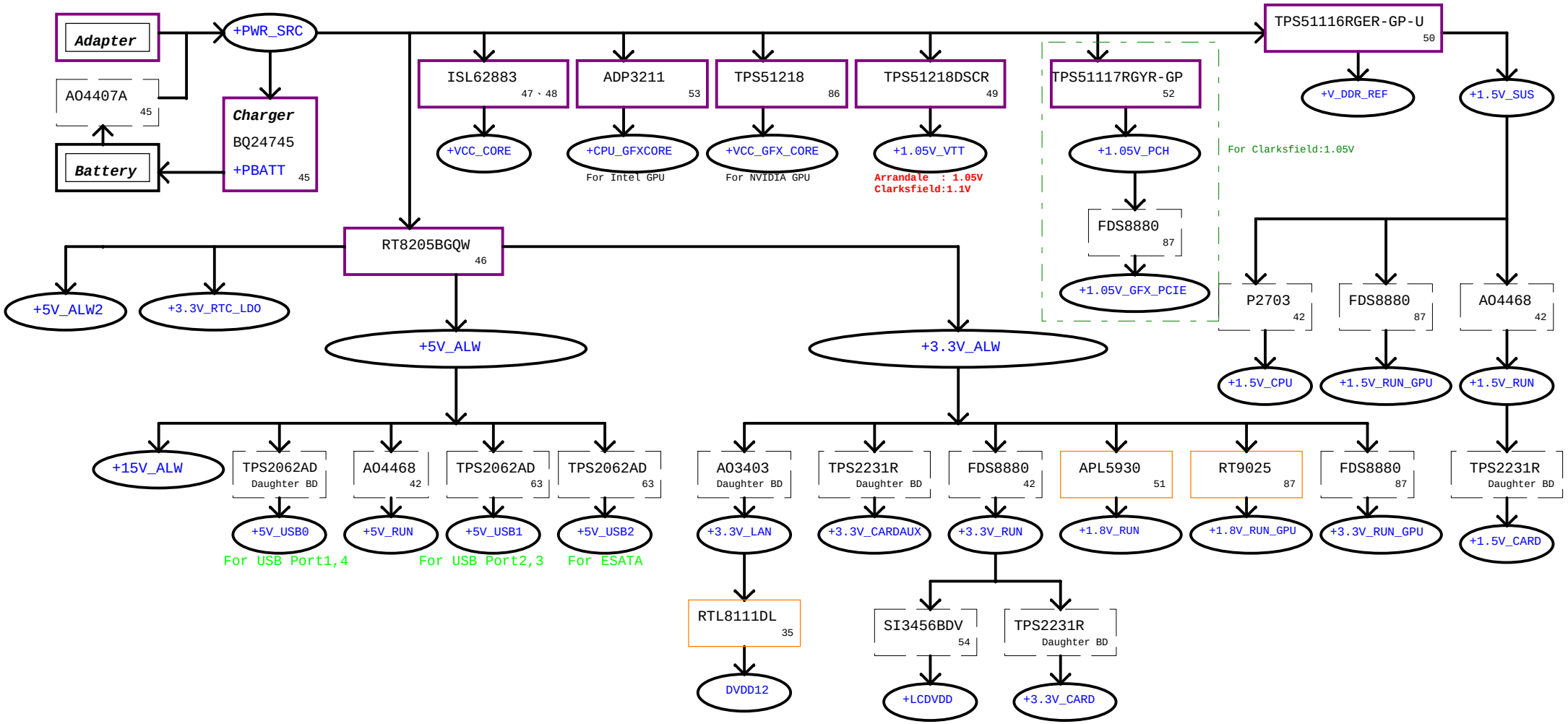

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Title: **Power Block Diagram**

Size: Custom | Document Number: **Vostro Calpella** | Rev: -1

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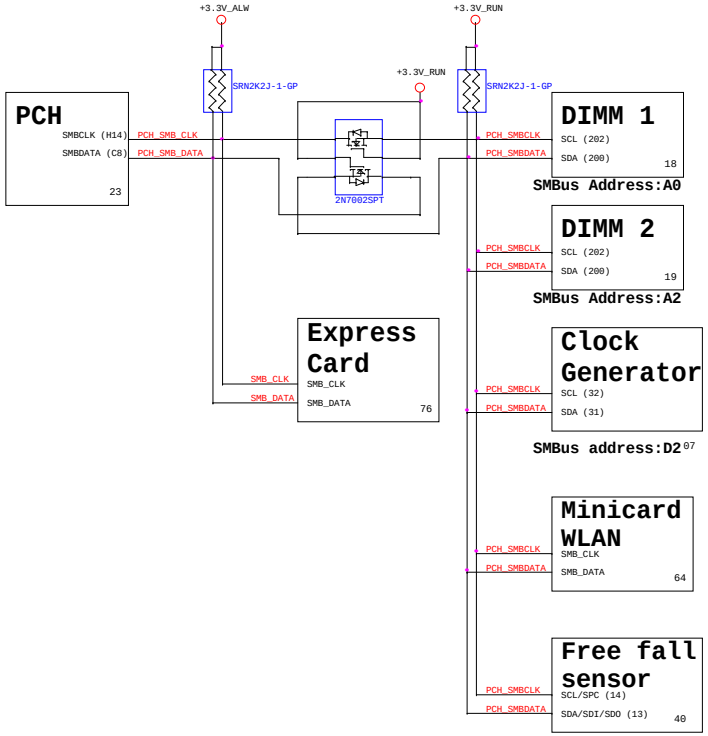
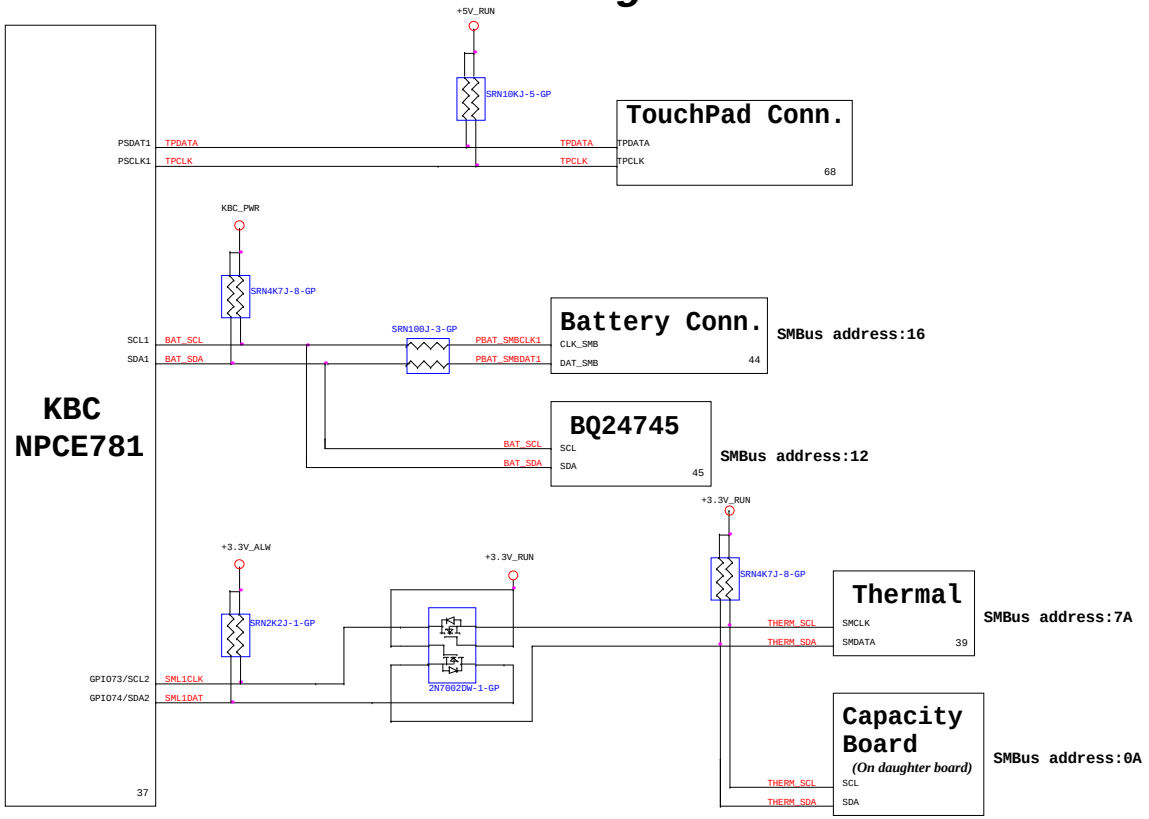
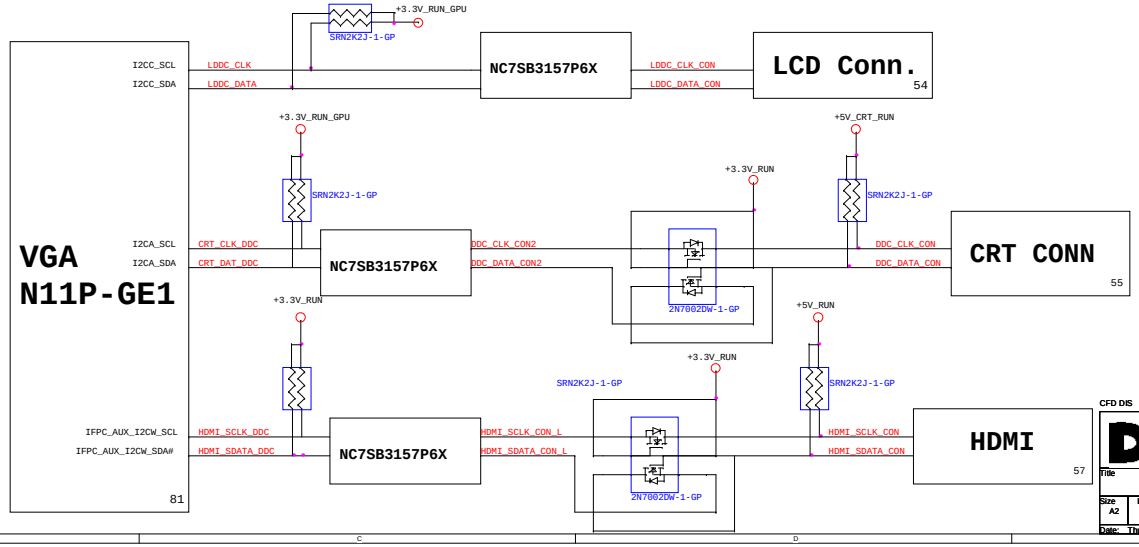
PCH SMBus Block Diagram



KBC SMBus Block Diagram



VGA SMBus Block Diagram



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Title: SMBUS Block Diagram

Size	Document Number	Rev
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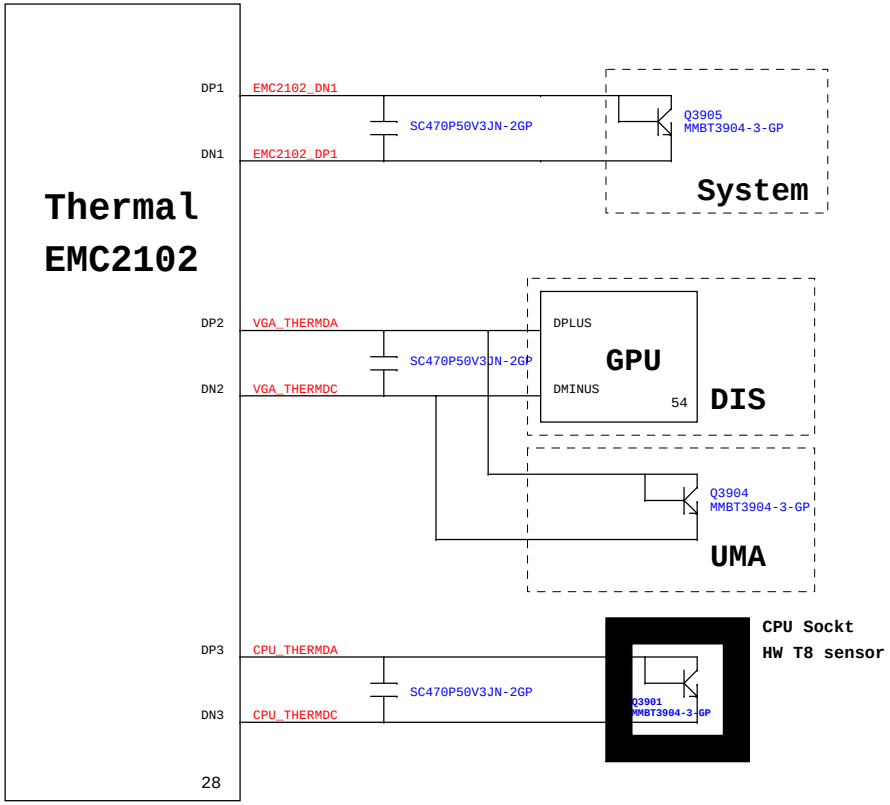
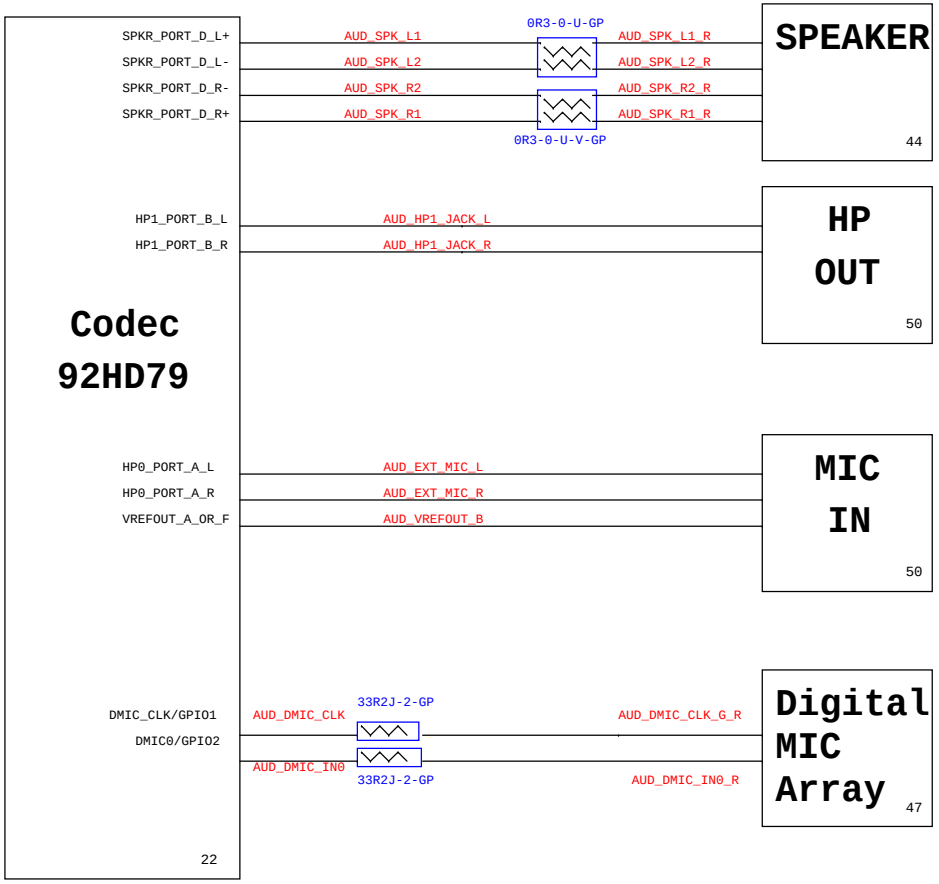
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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PCH Strapping

Calpella Schematic Checklist Rev.1_6

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** Note: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ; do not stuff resistor.
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled** **Note:** CRB uses a 330-kΩ resistor.
GNT0#, GNT1#	**Default (SPI):** Leave both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	**Enable Intel Anti-Theft Technology:**Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Intel Anti-Theft Technology:**Left floating, no pull-down required.
NV_ALE	**Enable Intel Anti-Theft Technology:**Connect to +NVRAM_Vccq with 8.2-kΩ weak pull-up resistor.[CRB has it pulled up with 1-kΩ no-stuff resistor] **Disable Intel Anti-Theft Technology:**Leave floating. (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0)-** Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. **High (1)--**Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. CRB recommends 1-kΩ pull-down for FD Override. **Note:** There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	**Low (0)-**Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality **High (1)--**Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality **Note:** This is an unmuxed signal. This signal has a weak internal pull-down of 20 KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kΩ pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	**Default = Do not connect (floating). Internal pull-up.** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev.1_6

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**

PCIE Routing

LANE1	NC
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	Card reader
LANE5	New Card

USB Table

USB	
Pair	Device
0	USB1 > LAN BOARD
1	USB4 > LAN BOARD
2	USB2 > M/B
3	USB3 > M/B
4	USB for ESATA
5	RESERVED
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BLUETOOTH
9	Touch Panel
10	Biometric
11	CAMERA
12	New Card
13	WLAN

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Title: Table of Content

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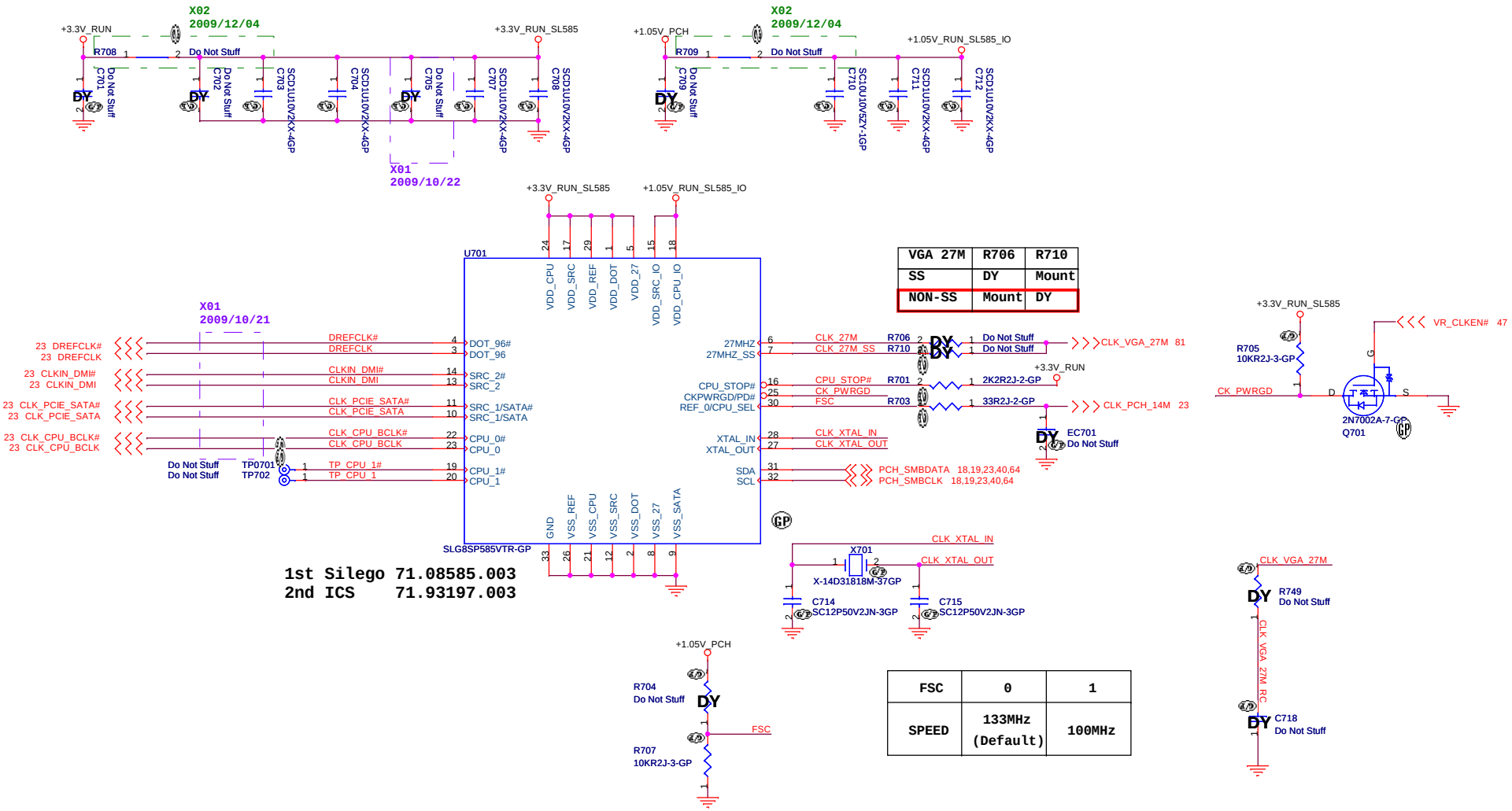

VGA 27M	R706	R710
SS	DY	Mount
NON-SS	Mount	DY

FSC	0	1
SPEED	133MHz (Default)	100MHz

1st Silego 71.08585.003
2nd ICS 71.93197.003

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Title: Clock Generator SLG8SP585

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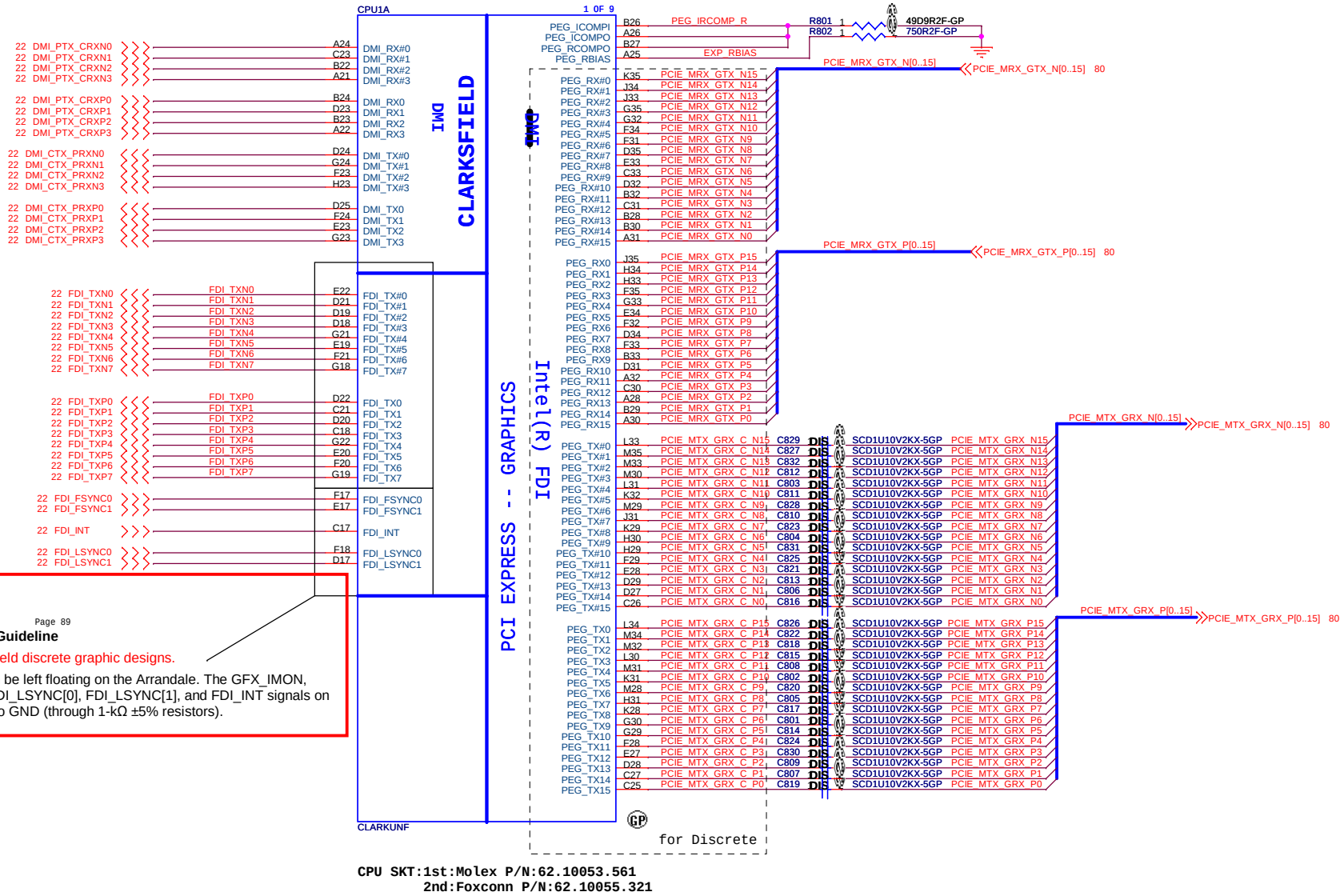

Calpella Platform Design Guide
Revision 1.6

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2.4 Arrandale Graphics Disable Guideline

It applies to Arrandale and Clarksfield discrete graphic designs.

FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

CPU SKT:1st:Molex P/N:62.10053.561
2nd:Foxconn P/N:62.10055.321

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Title: **CPU (PCIE/DMI/FDI)**

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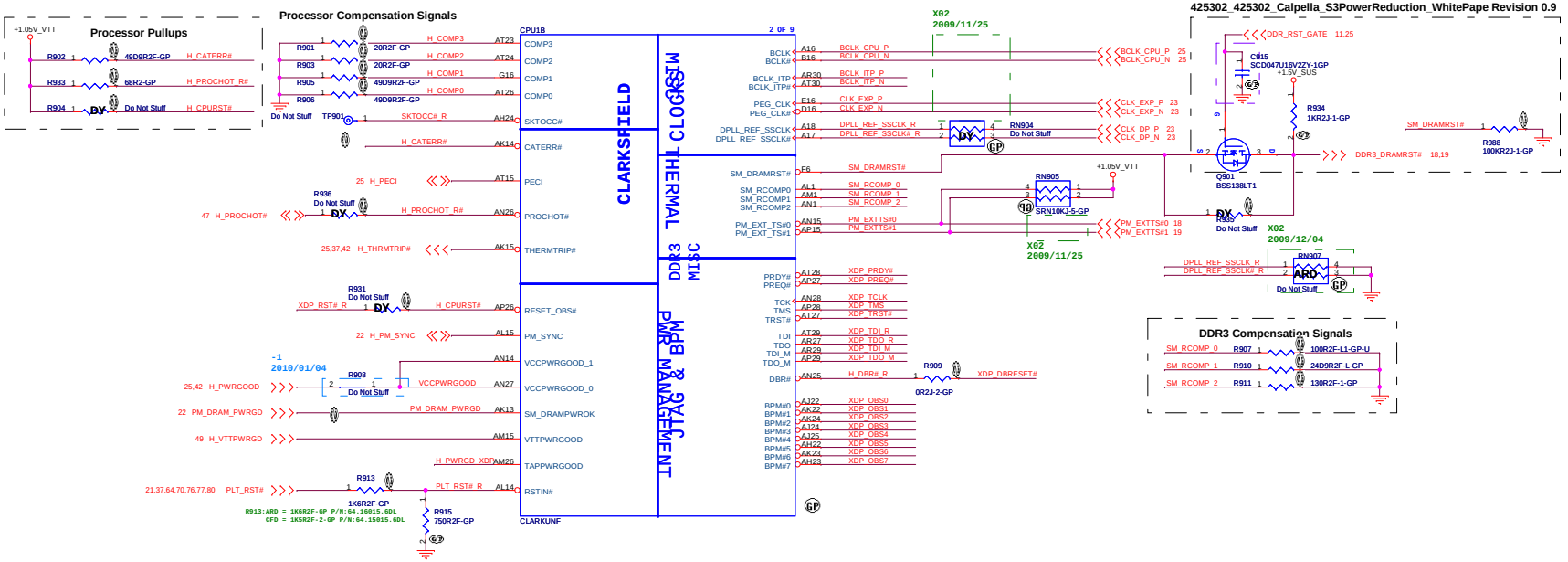
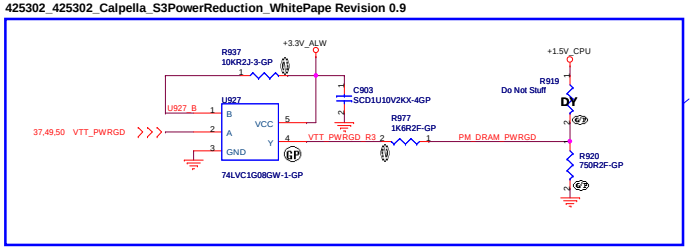




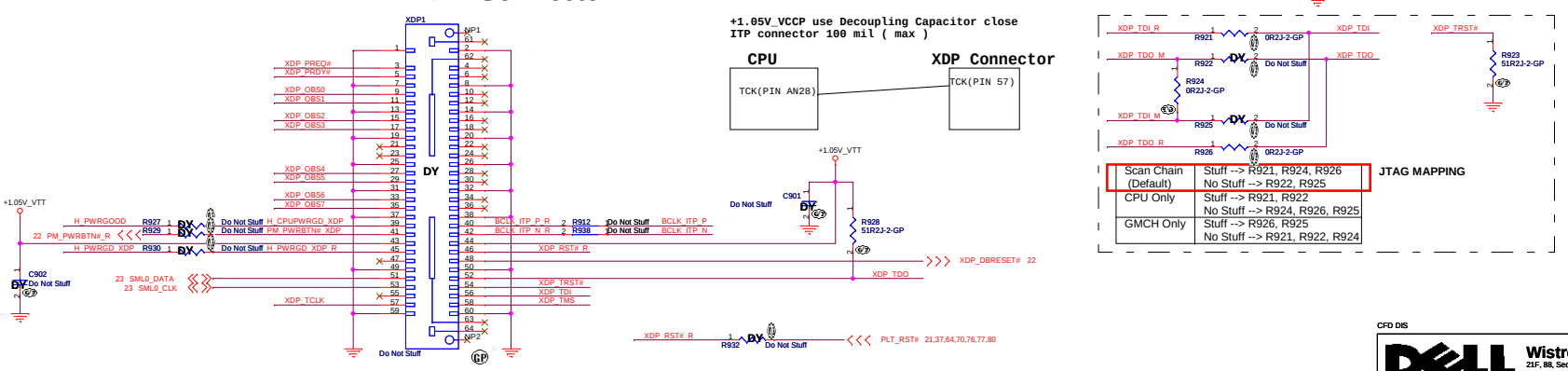
Normal

	R919	R920	R977
AUB	1.27k	3k 64.30015.6DL	1.6k(DY)
CFD	1.1k	3k 64.30015.6DL	1.5k(DY)

S3 Power Reduction circuit

	R919	R920	R977
AUB	1.1k(DY)	0.75k 64.75005.6DL	1.6k
CFD	1.1k(DY)	0.75k 64.75005.6DL	1.5k

XDP Connector



JTAG MAPPING	
Scan Chain (Default)	Stuff --> R921, R924, R926 No Stuff --> R922, R925
CPU Only	Stuff --> R921, R922 No Stuff --> R924, R926, R925
GMCH Only	Stuff --> R926, R925 No Stuff --> R921, R922, R924

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Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
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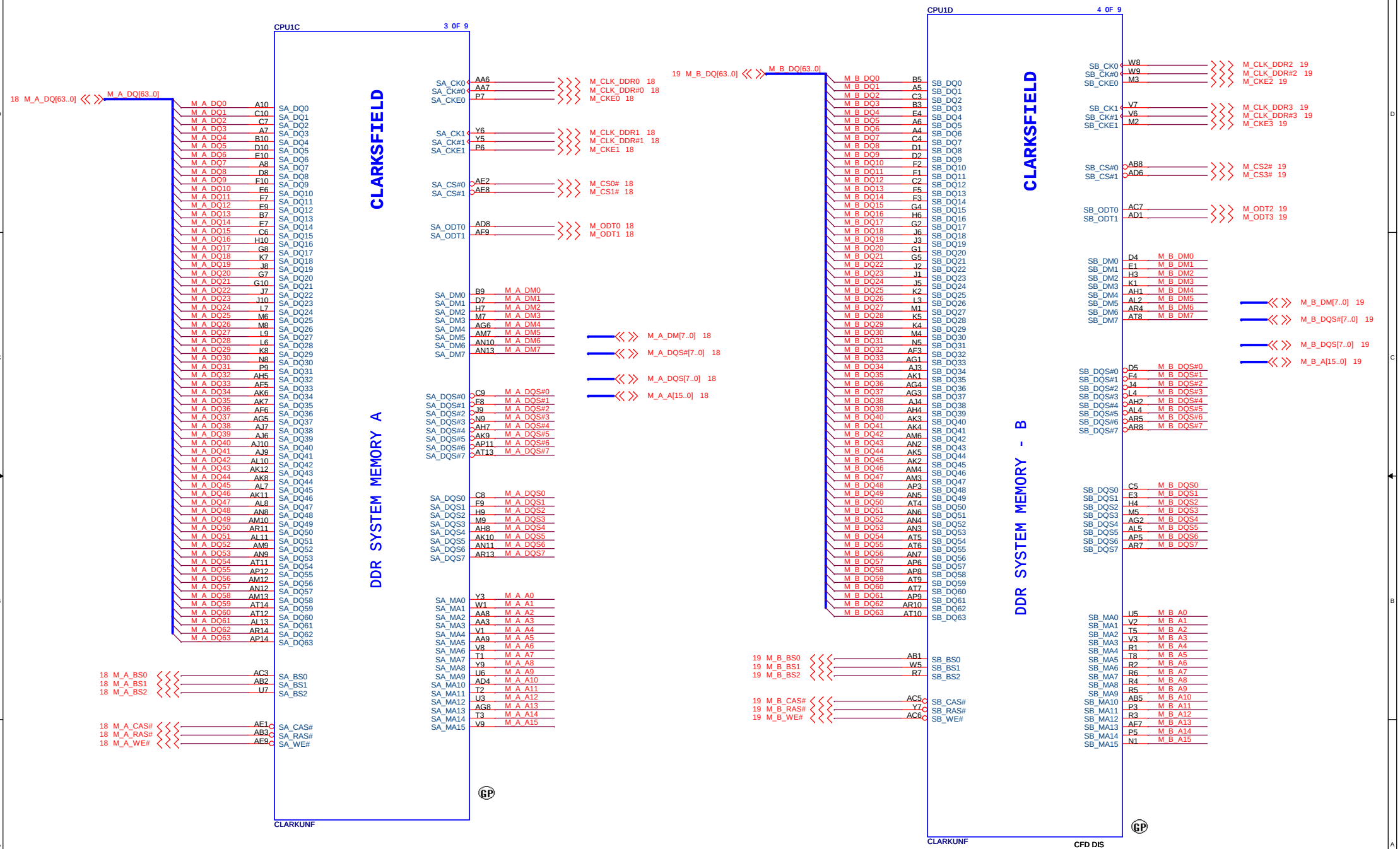

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Title: CPU (DDR)

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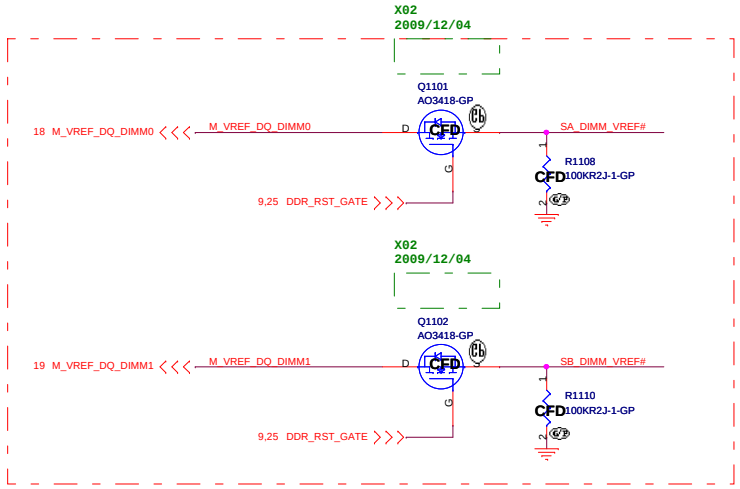
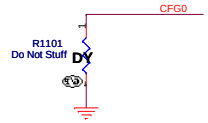
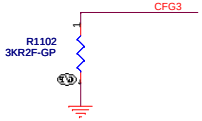


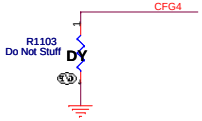


PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

DIS改5%



CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

Calpella Platform Design Guide
Revision 1.6

4.8.3.1 LVDS Switching

Switchable GFX, just like integrated GFX only, to enable LVDS it is required that the OEM set the LDVS (L_DDC_DATA) strap to present (pulled up) and the eDP strap (CFG[4]) to disabled (not pulled down).

4.8.3.2 eDP Switching

eDP for Switchable GFX can only be driven out of Port D of PCH. To configure Port D for embedded DP it is required to set the DDPD_CTRLDATA strap high to 3.3V Core rail through 2.2 kΩ ±5% resistor, LVDS (L_DDC_DATA) strap as no connect and the eDP strap CFG[4] as no connect.

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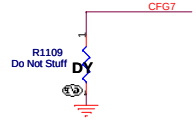
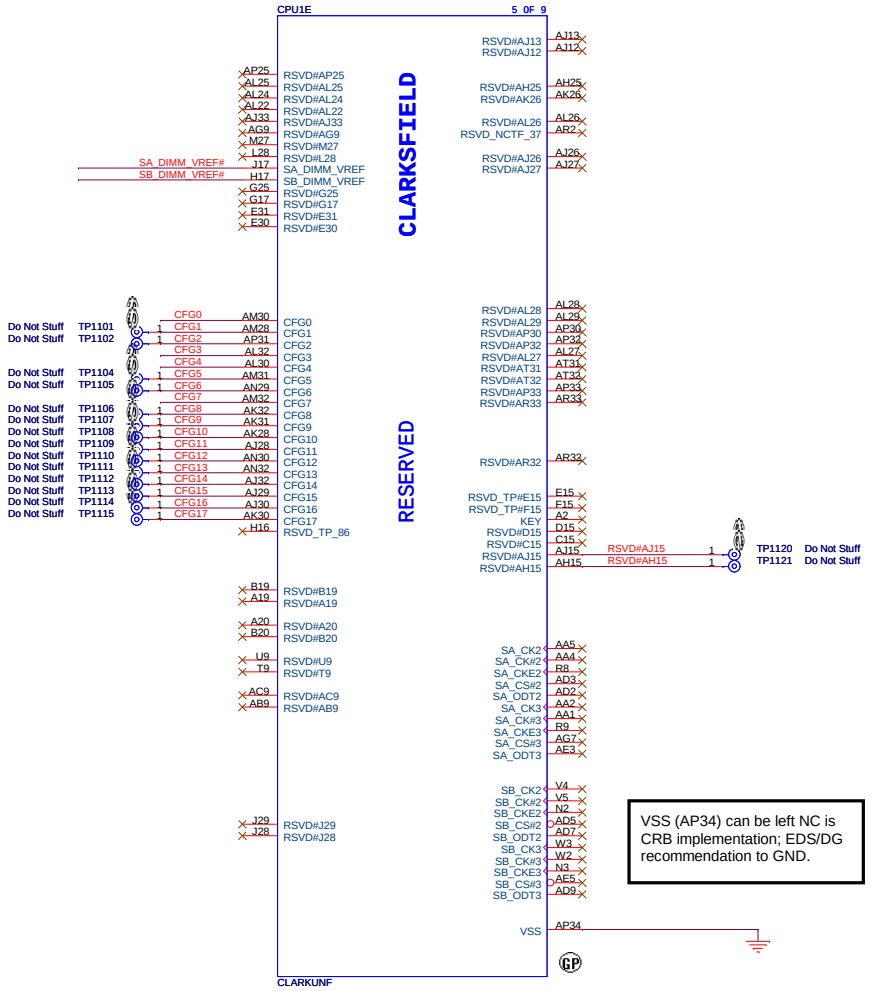


CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

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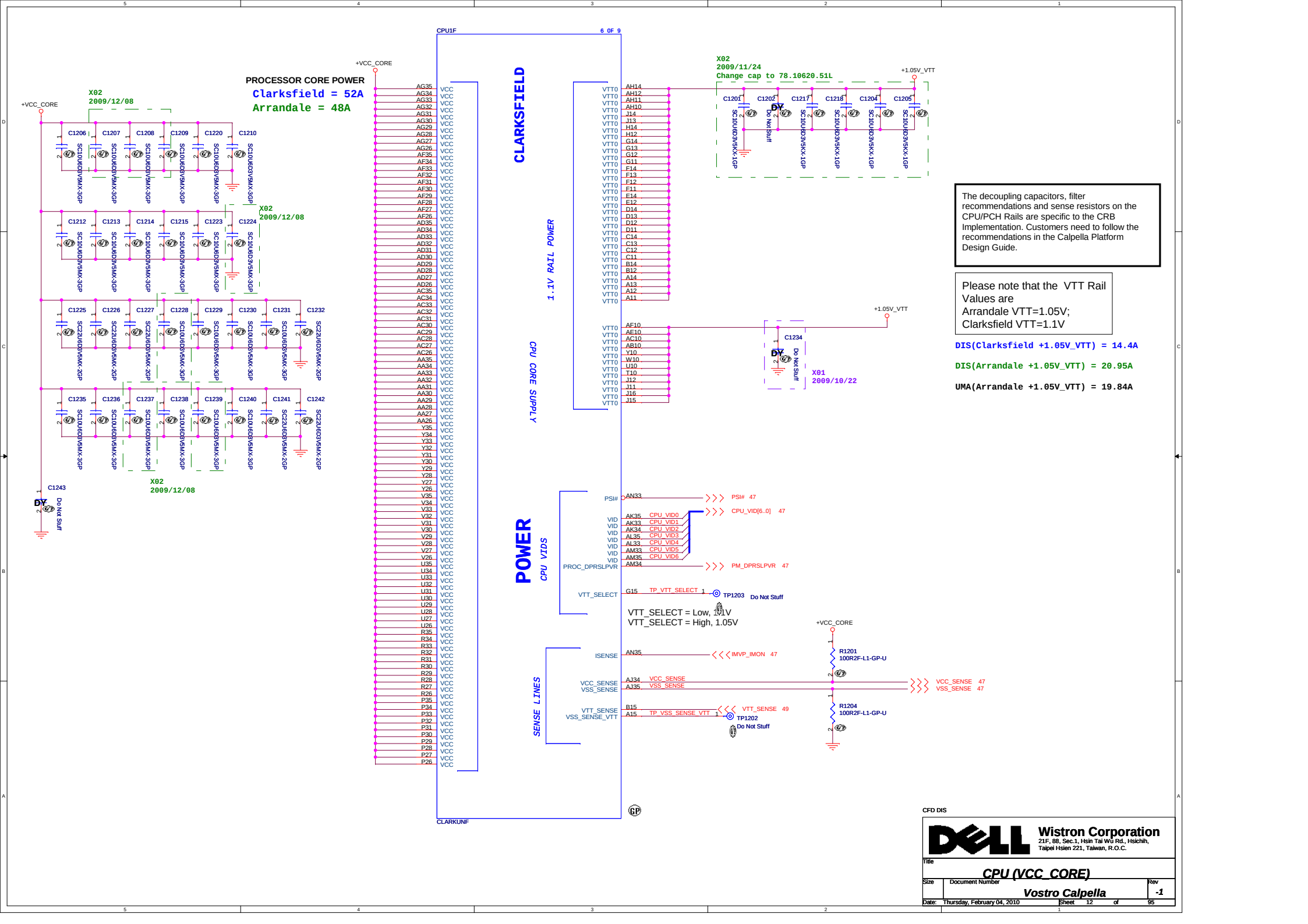

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Title	CPU (VCC_CORE)	
Size	Document Number: Vostro Calpella	Rev: -1
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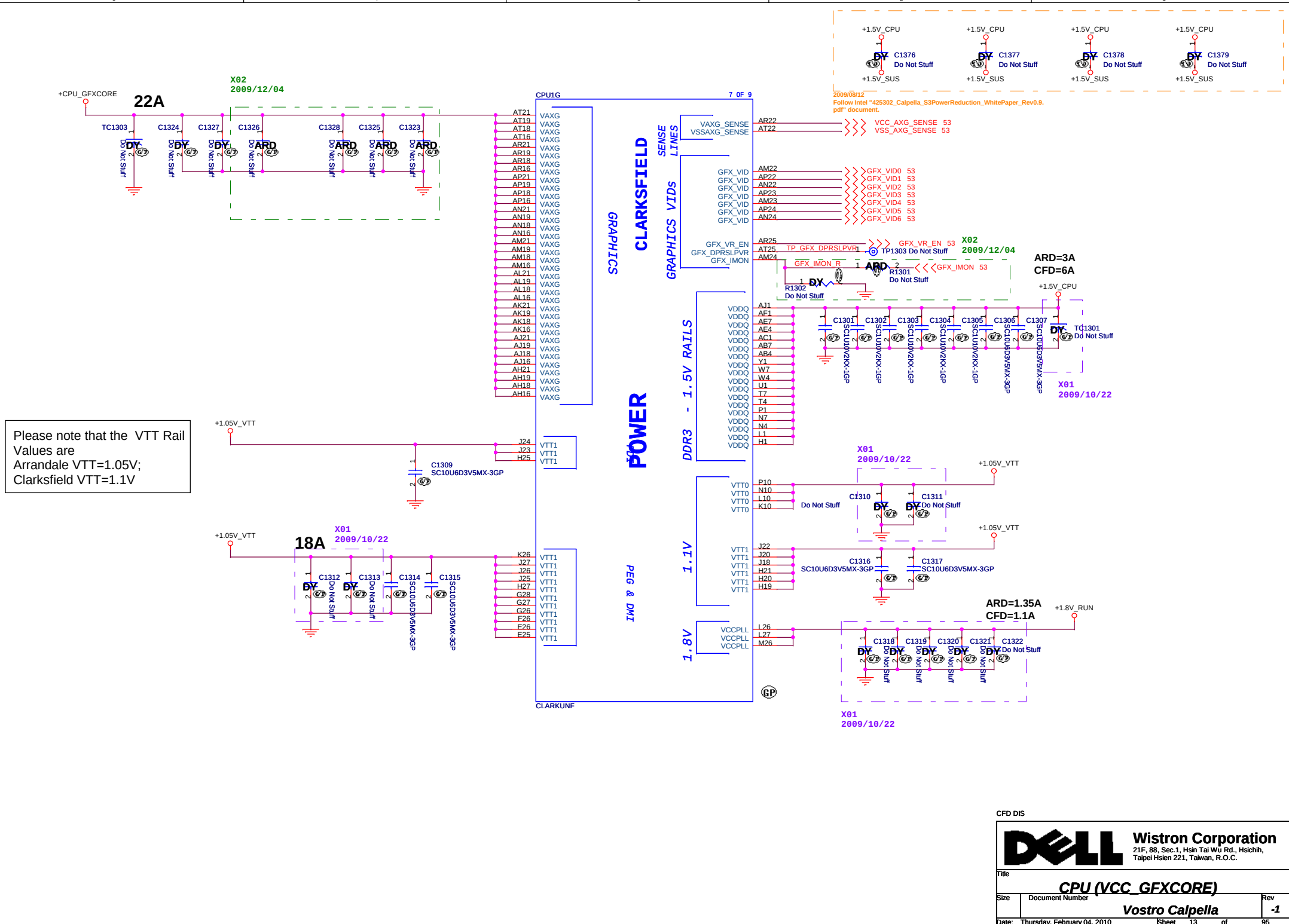

Please note that the VTT Rail Values are
Arrandale VTT=1.05V;
Clarksfield VTT=1.1V

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Title: CPU (VCC_GFXCORE)

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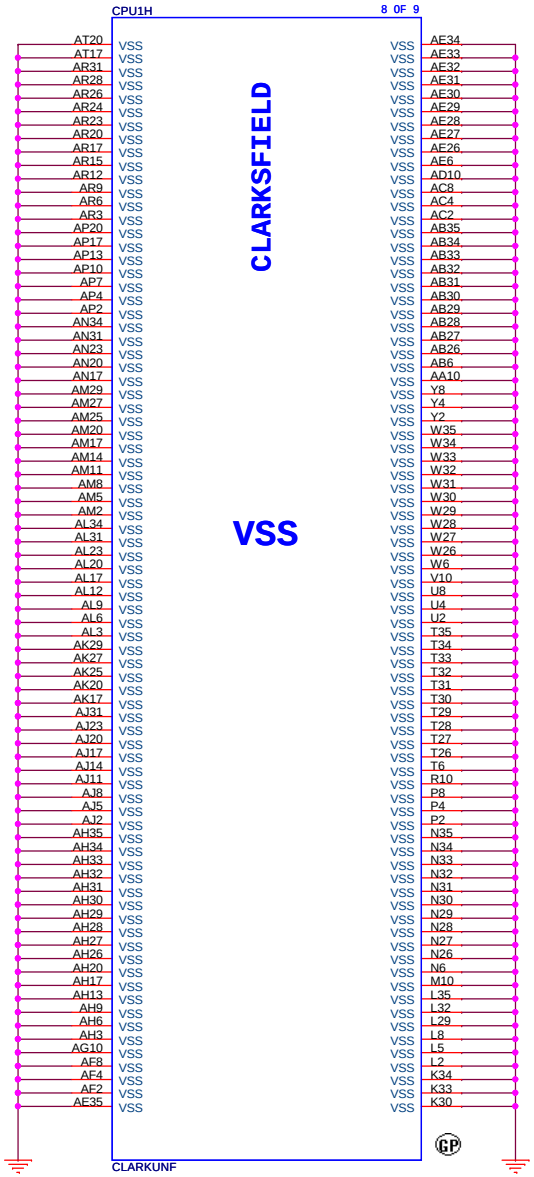

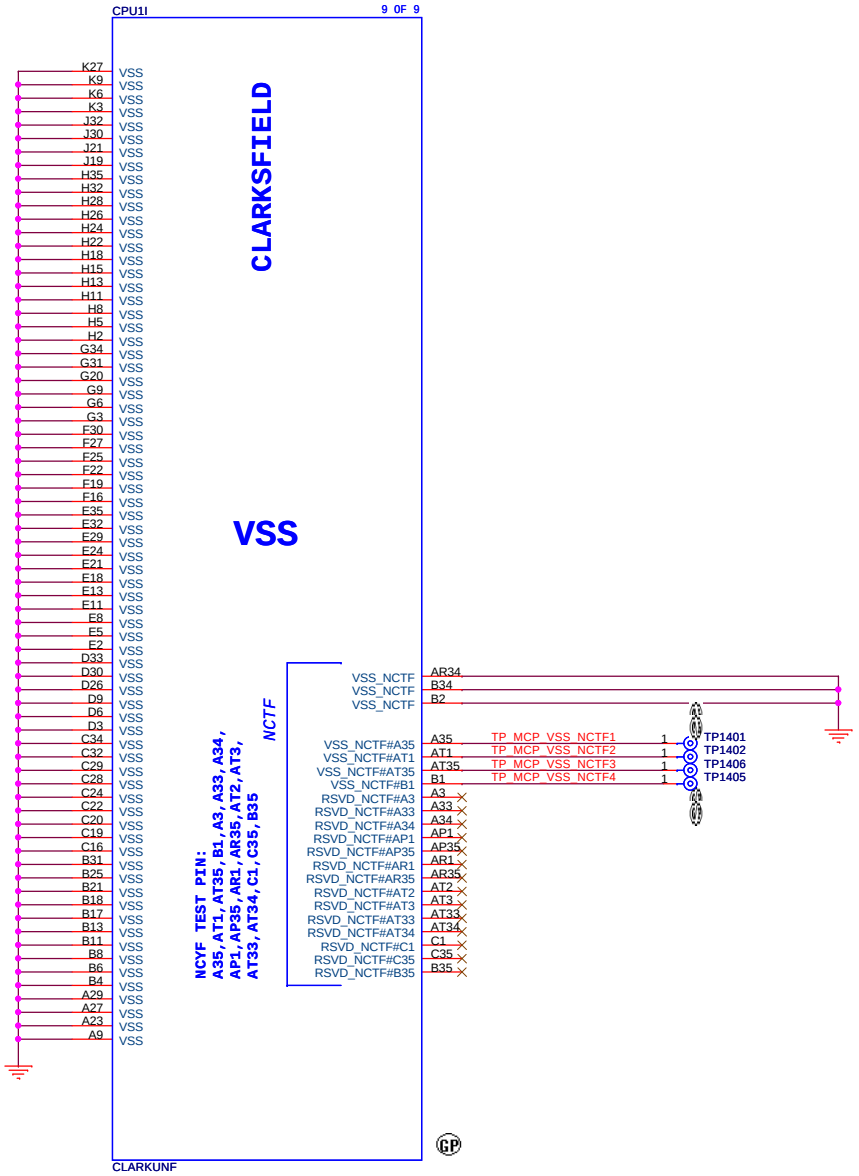

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Title

(Reserve)

Size	Document Number	Rev
A3	*Vostro Calpella*	*-1*

Date: Thursday, February 04, 2010 Sheet 17 of 95

SSID = MEMORY

10 M_A_DQS#[7..0]
10 M_A_DQ[63..0]
10 M_A_DM[7..0]
10 M_A_DQS[7..0]
10 M_A_A[15..0]

Layout Note:
Place near DM1

+1.5V_SUS

X01
2009/10/22

C1803 Do Not Stuff
C1804 SC10U6D3V5MX-3GP
C1812 Do Not Stuff
C1802 SC10U6D3V5MX-3GP
C1811 Do Not Stuff
C1816 SC10U6D3V5MX-3GP
TC1803 ST330U2D5VBM-1-GP

Layout Note:
Put close to VTT1,VTT2.

+0.75V_DDR_VTT

C1814 SC1U10V2KX-1GP
C1813 SC1U10V2KX-1GP
C1815 SC1U10V2KX-1GP
C1801 SC1U10V2KX-1GP
C1823 SC10U6D3V5MX-3GP

+1.5V_SUS

C1872 SCD1U10V2KX-4GP
C1873 SCD1U10V2KX-4GP
C1874 SCD1U10V2KX-4GP
C1875 SCD1U10V2KX-4GP

2009/08/12
Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9.pdf" document.

+V_DDR_REF

-1
2010/01/04
R1803 0R2J-2-GP
C1817 SCD1U16V2KX-3GP
C1805 SC2D2U10V3KX-1GP
C1808 Do Not Stuff
X01
2009/10/20
M_VREF_DQ_DIMM0 11

+V_DDR_REF
C1810 SCD1U16V2KX-3GP
C1809 SC2D2U10V3KX-1GP
M_VREF_DQ_DIMM0

+0.75V_DDR_VTT

DM1

M_A_A0	98	A0	
M_A_A1	97	A1	
M_A_A2	96	A2	
M_A_A3	95	A3	
M_A_A4	92	A4	
M_A_A5	91	A5	
M_A_A6	90	A6	
M_A_A7	86	A7	
M_A_A8	89	A8	
M_A_A9	85	A9	
M_A_A10	107	A10/AP	
M_A_A11	84	A11	
M_A_A12	83	A12	
M_A_A13	119	A13	
M_A_A14	80	A14	
M_A_A15	78	A15	
M_A_BS2	79	A16/BA2	10 M_A_BS2
M_A_BS0	109	BA0	10 M_A_BS0
M_A_BS1	108	BA1	10 M_A_BS1
M_A_DQ0	5	DQ0	
M_A_DQ1	7	DQ1	
M_A_DQ2	15	DQ2	
M_A_DQ3	17	DQ3	
M_A_DQ4	4	DQ4	
M_A_DQ5	6	DQ5	
M_A_DQ6	16	DQ6	
M_A_DQ7	18	DQ7	
M_A_DQ8	21	DQ8	
M_A_DQ9	23	DQ9	
M_A_DQ10	33	DQ10	
M_A_DQ11	35	DQ11	
M_A_DQ12	22	DQ12	
M_A_DQ13	24	DQ13	
M_A_DQ14	34	DQ14	
M_A_DQ15	36	DQ15	
M_A_DQ16	39	DQ16	
M_A_DQ17	41	DQ17	
M_A_DQ18	51	DQ18	
M_A_DQ19	53	DQ19	
M_A_DQ20	40	DQ20	
M_A_DQ21	42	DQ21	
M_A_DQ22	50	DQ22	
M_A_DQ23	52	DQ23	
M_A_DQ24	57	DQ24	
M_A_DQ25	59	DQ25	
M_A_DQ26	67	DQ26	
M_A_DQ27	69	DQ27	
M_A_DQ28	56	DQ28	
M_A_DQ29	58	DQ29	
M_A_DQ30	68	DQ30	
M_A_DQ31	70	DQ31	
M_A_DQ32	129	DQ32	
M_A_DQ33	131	DQ33	
M_A_DQ34	141	DQ34	
M_A_DQ35	143	DQ35	
M_A_DQ36	130	DQ36	
M_A_DQ37	132	DQ37	
M_A_DQ38	140	DQ38	
M_A_DQ39	142	DQ39	
M_A_DQ40	147	DQ40	
M_A_DQ41	149	DQ41	
M_A_DQ42	157	DQ42	
M_A_DQ43	159	DQ43	
M_A_DQ44	146	DQ44	
M_A_DQ45	148	DQ45	
M_A_DQ46	158	DQ46	
M_A_DQ47	160	DQ47	
M_A_DQ48	163	DQ48	
M_A_DQ49	165	DQ49	
M_A_DQ50	175	DQ50	
M_A_DQ51	177	DQ51	
M_A_DQ52	164	DQ52	
M_A_DQ53	166	DQ53	
M_A_DQ54	174	DQ54	
M_A_DQ55	176	DQ55	
M_A_DQ56	181	DQ56	
M_A_DQ57	183	DQ57	
M_A_DQ58	191	DQ58	
M_A_DQ59	193	DQ59	
M_A_DQ60	180	DQ60	
M_A_DQ61	182	DQ61	
M_A_DQ62	192	DQ62	
M_A_DQ63	194	DQ63	
M_A_DQS#0	10	DQS0#	
M_A_DQS#1	27	DQS1#	
M_A_DQS#2	45	DQS2#	
M_A_DQS#3	62	DQS3#	
M_A_DQS#4	135	DQS4#	
M_A_DQS#5	152	DQS5#	
M_A_DQS#6	169	DQS6#	
M_A_DQS#7	186	DQS7#	
M_A_DQS0	12	DQS0	
M_A_DQS1	29	DQS1	
M_A_DQS2	47	DQS2	
M_A_DQS3	64	DQS3	
M_A_DQS4	137	DQS4	
M_A_DQS5	154	DQS5	
M_A_DQS6	171	DQS6	
M_A_DQS7	188	DQS7	
M_ODT0	116	ODT0	10 M_ODT0
M_ODT1	120	ODT1	10 M_ODT1
	126	VREF_CA	
	1	VREF_DQ	
	30	RESET#	9,19 DDR3_DRAMRST#
	203	VTT1	
	204	VTT2	

NP1	NP1	
NP2	NP2	
RAS#	110	M_A_RAS# 10
WE#	113	M_A_WE# 10
CAS#	115	M_A_CAS# 10
CS0#	114	M_CS0# 10
CS1#	121	M_CS1# 10
CKE0	73	M_CKE0 10
CKE1	74	M_CKE1 10
CK0	101	M_CLK_DDR0 / M_CLK_DDR0 10
CK0#	103	M_CLK_DDR#0 / M_CLK_DDR#0 10
CK1	102	M_CLK_DDR1 / M_CLK_DDR1 10
CK1#	104	M_CLK_DDR#1 / M_CLK_DDR#1 10
DM0	11	M_A_DM0
DM1	28	M_A_DM1
DM2	46	M_A_DM2
DM3	63	M_A_DM3
DM4	136	M_A_DM4
DM5	153	M_A_DM5
DM6	170	M_A_DM6
DM7	187	M_A_DM7
SDA	200	PCH_SMBDATA 7,19,23,40,64
SCL	202	PCH_SMBCLK 7,19,23,40,64
EVENT#	198	PM_EXTTS#0 9
VDDSPD	199	
SA0	197	SA0_DM1
SA1	201	SA1_DM1
NC#1	77	
NC#2	122	
NC#/TEST	125	
VDD1	75	
VDD2	76	
VDD3	81	
VDD4	82	
VDD5	87	
VDD6	88	
VDD7	93	
VDD8	94	
VDD9	99	
VDD10	100	
VDD11	105	
VDD12	106	
VDD13	111	
VDD14	112	
VDD15	117	
VDD16	118	
VDD17	123	
VDD18	124	
VSS	2	
VSS	3	
VSS	8	
VSS	9	
VSS	13	
VSS	14	
VSS	19	
VSS	20	
VSS	25	
VSS	26	
VSS	31	
VSS	32	
VSS	37	
VSS	38	
VSS	43	
VSS	44	
VSS	48	
VSS	49	
VSS	54	
VSS	55	
VSS	60	
VSS	61	
VSS	65	
VSS	66	
VSS	71	
VSS	72	
VSS	127	
VSS	128	
VSS	133	
VSS	134	
VSS	138	
VSS	139	
VSS	144	
VSS	145	
VSS	150	
VSS	151	
VSS	155	
VSS	156	
VSS	161	
VSS	162	
VSS	167	
VSS	168	
VSS	172	
VSS	173	
VSS	178	
VSS	179	
VSS	184	
VSS	185	
VSS	189	
VSS	190	
VSS	195	
VSS	196	
VSS	205	
VSS	206	

Height 5.2mm

DDR3-204P-25-GP
62.10017.K11

+1.5V_SUS

+3.3V_RUN
C1806 SCD1U16V2KX-3GP
C1807 Do Not Stuff

SA0_DM1
SA1_DM1
R1802 10KR2J-3-GP
R1801 10KR2J-3-GP

SMBUS address:A0

Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4

put near connector
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
C1821 Do Not Stuff
C1819 Do Not Stuff
C1820 Do Not Stuff
C1818 Do Not Stuff

CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII-SODIMM SLOT1
Size: Custom
Document Number: Vostro Calpella
Rev: -1
Date: Thursday, February 04, 2010
Sheet 18 of 95

SSID = MEMORY

10 M_B_DQS#[7..0]
10 M_B_DQ[63..0]
10 M_B_DM[7..0]
10 M_B_DQS[7..0]
10 M_B_A[15..0]

Layout Note:
Place near DM2

X01
2009/10/22

+1.5V_SUS

C1919 SCD1U06D3V5MX-3GP
C1905 SCD1U06D3V5MX-3GP Do Not Stuff
C1911 SCD1U06D3V5MX-3GP
C1916 SCD1U06D3V5MX-3GP Do Not Stuff
C1913 SCD1U06D3V5MX-3GP
C1920 SCD1U06D3V5MX-3GP Do Not Stuff
TC1903 Do Not Stuff

Layout Note:
Put close to VTT1,VTT2.

+0.75V_DDR_VTT

C1908 SCD1U10V2KX-1GP
C1917 SCD1U10V2KX-1GP
C1909 SCD1U10V2KX-1GP
C1918 SCD1U10V2KX-1GP

+1.5V_SUS

C1976 SCD1U10V2KX-4GP
C1977 SCD1U10V2KX-4GP
C1978 SCD1U10V2KX-4GP
C1979 SCD1U10V2KX-4GP

2009/08/12
Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9. pdf" document.

+V_DDR_REF

-1
2010/01/04

R1905 0R2J-2-GP
C1910 SCD1U16V2KX-3GP
C1912 SC2D2U10V3KX-1GP
C1915 Do Not Stuff
M_VREF_DQ_DIMM1 11

X01
2009/10/20

+V_DDR_REF

C1907 SCD1U16V2KX-3GP
C1914 SC2D2U10V3KX-1GP

M_VREF_DQ_DIMM1

9,18 DDR3_DRAMRST#

+0.75V_DDR_VTT

10 M_ODT2
10 M_ODT3

DM2

M_B_A0	98	A0	
M_B_A1	97	A1	
M_B_A2	96	A2	
M_B_A3	95	A3	
M_B_A4	92	A4	
M_B_A5	91	A5	
M_B_A6	90	A6	
M_B_A7	86	A7	
M_B_A8	89	A8	
M_B_A9	85	A9	
M_B_A10	107	A10/AP	
M_B_A11	84	A11	
M_B_A12	83	A12	
M_B_A13	119	A13	
M_B_A14	80	A14	
M_B_A15	78	A15	
M_B_BS2	79	A16/BA2	
M_B_BS0	109	BA0	
M_B_BS1	108	BA1	
M_B_DQ0	5	DQ0	
M_B_DQ1	7	DQ1	
M_B_DQ2	15	DQ2	
M_B_DQ3	17	DQ3	
M_B_DQ4	4	DQ4	
M_B_DQ5	6	DQ5	
M_B_DQ6	16	DQ6	
M_B_DQ7	18	DQ7	
M_B_DQ8	21	DQ8	
M_B_DQ9	23	DQ9	
M_B_DQ10	33	DQ10	
M_B_DQ11	35	DQ11	
M_B_DQ12	22	DQ12	
M_B_DQ13	24	DQ13	
M_B_DQ14	34	DQ14	
M_B_DQ15	36	DQ15	
M_B_DQ16	39	DQ16	
M_B_DQ17	41	DQ17	
M_B_DQ18	51	DQ18	
M_B_DQ19	53	DQ19	
M_B_DQ20	40	DQ20	
M_B_DQ21	42	DQ21	
M_B_DQ22	50	DQ22	
M_B_DQ23	52	DQ23	
M_B_DQ24	57	DQ24	
M_B_DQ25	59	DQ25	
M_B_DQ26	67	DQ26	
M_B_DQ27	69	DQ27	
M_B_DQ28	56	DQ28	
M_B_DQ29	58	DQ29	
M_B_DQ30	68	DQ30	
M_B_DQ31	70	DQ31	
M_B_DQ32	129	DQ32	
M_B_DQ33	131	DQ33	
M_B_DQ34	141	DQ34	
M_B_DQ35	143	DQ35	
M_B_DQ36	130	DQ36	
M_B_DQ37	132	DQ37	
M_B_DQ38	140	DQ38	
M_B_DQ39	142	DQ39	
M_B_DQ40	147	DQ40	
M_B_DQ41	149	DQ41	
M_B_DQ42	157	DQ42	
M_B_DQ43	159	DQ43	
M_B_DQ44	146	DQ44	
M_B_DQ45	148	DQ45	
M_B_DQ46	158	DQ46	
M_B_DQ47	160	DQ47	
M_B_DQ48	163	DQ48	
M_B_DQ49	165	DQ49	
M_B_DQ50	175	DQ50	
M_B_DQ51	177	DQ51	
M_B_DQ52	164	DQ52	
M_B_DQ53	166	DQ53	
M_B_DQ54	174	DQ54	
M_B_DQ55	176	DQ55	
M_B_DQ56	181	DQ56	
M_B_DQ57	183	DQ57	
M_B_DQ58	191	DQ58	
M_B_DQ59	193	DQ59	
M_B_DQ60	180	DQ60	
M_B_DQ61	182	DQ61	
M_B_DQ62	192	DQ62	
M_B_DQ63	194	DQ63	
M_B_DQS#0	10	DQS0#	
M_B_DQS#1	27	DQS1#	
M_B_DQS#2	45	DQS2#	
M_B_DQS#3	62	DQS3#	
M_B_DQS#4	135	DQS4#	
M_B_DQS#5	152	DQS5#	
M_B_DQS#6	169	DQS6#	
M_B_DQS#7	186	DQS7#	
M_B_DQS0	12	DQS0	
M_B_DQS1	29	DQS1	
M_B_DQS2	47	DQS2	
M_B_DQS3	64	DQS3	
M_B_DQS4	137	DQS4	
M_B_DQS5	154	DQS5	
M_B_DQS6	171	DQS6	
M_B_DQS7	188	DQS7	
M_ODT2	116	ODT0	
M_ODT3	120	ODT1	
	126	VREF_CA	
	1	VREF_DQ	
	30	RESET#	
	203	VTT1	
	204	VTT2	

NP1		NP1	
NP2		NP2	
RAS#	110	M_B_RAS# 10	
WE#	113	M_B_WE# 10	
CAS#	115	M_B_CAS# 10	
CS0#	114	M_CS2# 10	
CS1#	121	M_CS3# 10	
CKE0	73	M_CKE2 10	
CKE1	74	M_CKE3 10	
CK0	101	M_CLK_DDR2	M_CLK_DDR2 10
CK0#	103	M_CLK_DDR#2	M_CLK_DDR#2 10
CK1	102	M_CLK_DDR3	M_CLK_DDR3 10
CK1#	104	M_CLK_DDR#3	M_CLK_DDR#3 10
DM0	11	M_B_DM0	
DM1	28	M_B_DM1	
DM2	46	M_B_DM2	
DM3	63	M_B_DM3	
DM4	136	M_B_DM4	
DM5	153	M_B_DM5	
DM6	170	M_B_DM6	
DM7	187	M_B_DM7	
SDA	200	PCH_SMBDATA	PCH_SMBDATA 7,18,23,40,64
SCL	202	PCH_SMBCLK	PCH_SMBCLK 7,18,23,40,64
EVENT#	198	PM_EXTTS#1 9	
VDDSPD	199		
SA0	197	SA0_DM2	
SA1	201	SA1_DM2	
NC#1	77		
NC#2	122		
NC#/TEST	125		
VDD1	75		
VDD2	76		
VDD3	81		
VDD4	82		
VDD5	87		
VDD6	88		
VDD7	93		
VDD8	94		
VDD9	99		
VDD10	100		
VDD11	105		
VDD12	106		
VDD13	111		
VDD14	112		
VDD15	117		
VDD16	118		
VDD17	123		
VDD18	124		
VSS	2		
VSS	3		
VSS	8		
VSS	9		
VSS	13		
VSS	14		
VSS	19		
VSS	20		
VSS	25		
VSS	26		
VSS	31		
VSS	32		
VSS	37		
VSS	38		
VSS	43		
VSS	44		
VSS	48		
VSS	49		
VSS	54		
VSS	55		
VSS	60		
VSS	61		
VSS	65		
VSS	66		
VSS	71		
VSS	72		
VSS	127		
VSS	128		
VSS	133		
VSS	134		
VSS	138		
VSS	139		
VSS	144		
VSS	145		
VSS	150		
VSS	151		
VSS	155		
VSS	156		
VSS	161		
VSS	162		
VSS	167		
VSS	168		
VSS	172		
VSS	173		
VSS	178		
VSS	179		
VSS	184		
VSS	185		
VSS	189		
VSS	190		
VSS	195		
VSS	196		
VSS	205		
VSS	206		

Height 9.2mm

DDR3-204P-24-GP
62.10017.K01

+3.3V_RUN

R1903 Do Not Stuff
R1904 10KR2J-3-GP
SA1_DM2
SA0_DM2
R1901 10KR2J-3-GP
R1902 Do Not Stuff

SMBUS address:A4

+3.3V_RUN

C1906 SCD1U16V2KX-3GP
C1921 Do Not Stuff

put near connector

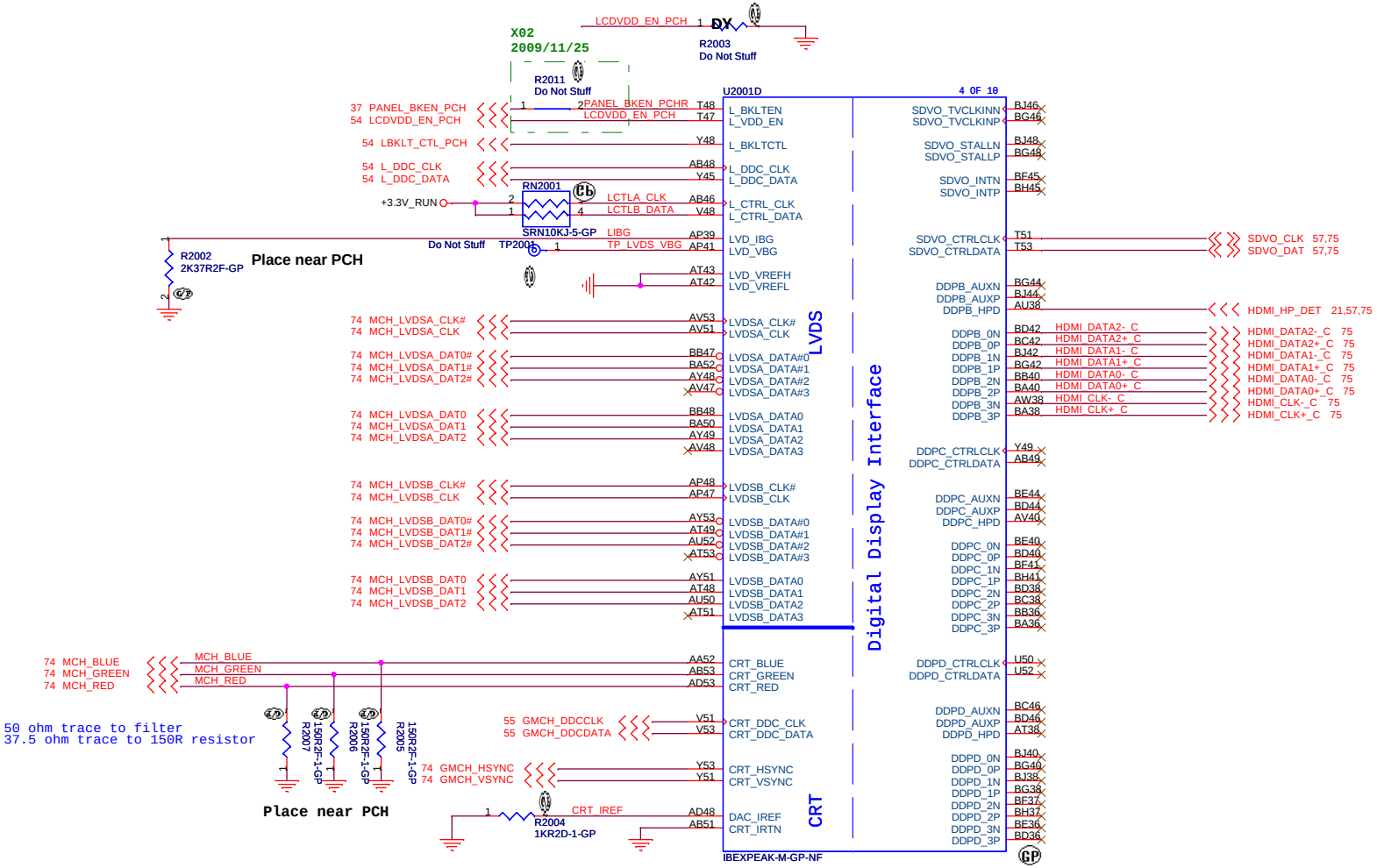
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3

C1901 Do Not Stuff
C1904 Do Not Stuff
C1902 Do Not Stuff
C1903 Do Not Stuff

CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII-SODIMM SLOT2
Size: Custom
Document Number: Vostro Calpella
Rev: -1
Date: Thursday, February 04, 2010
Sheet 19 of 95



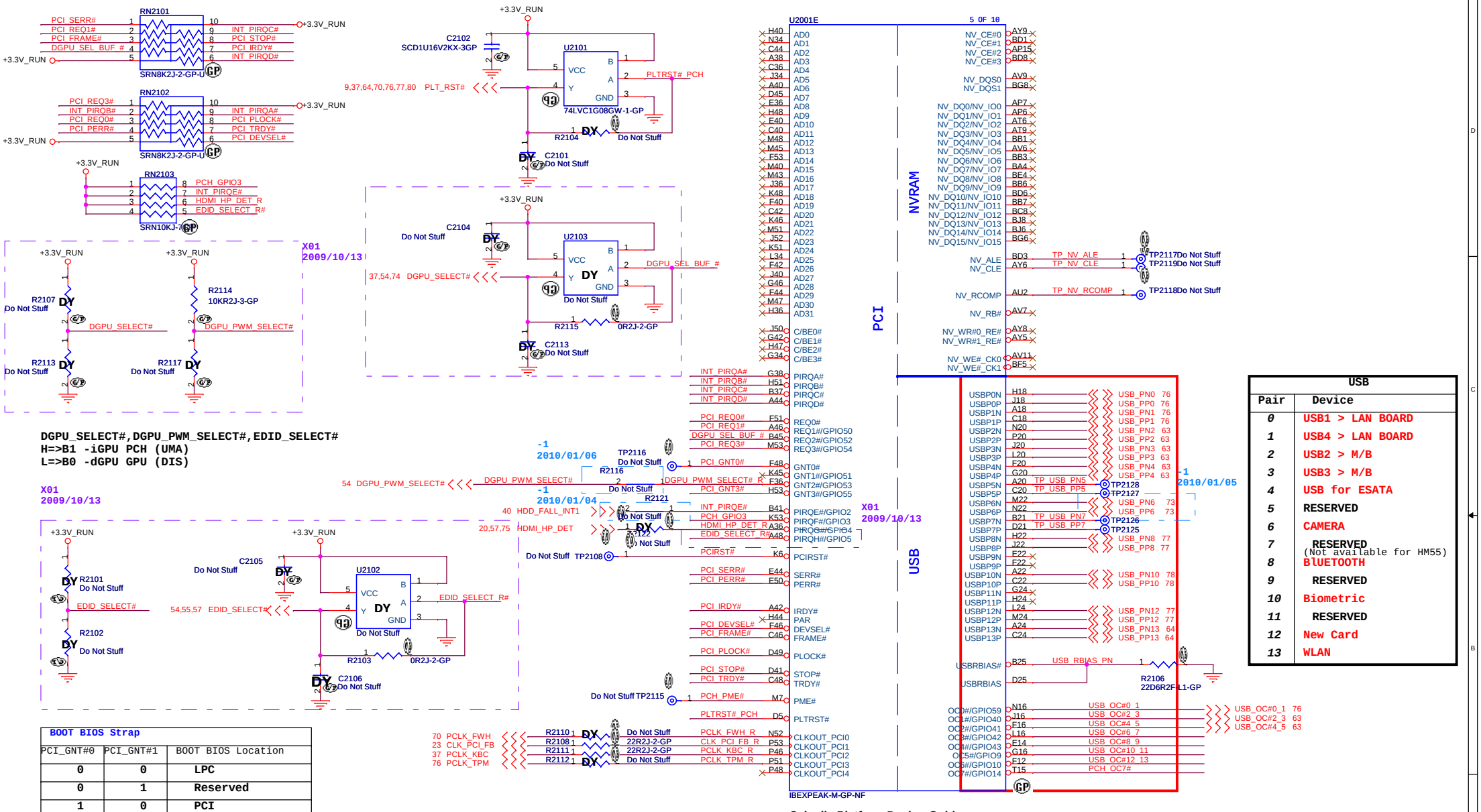
CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size | Document Number: Vostro Calpella | Rev: -1

Date: Thursday, February 04, 2010 | Sheet 20 of 95



Calpella Platform Design Guide
Revision 1.6

Table 111. Overcurrent Pin Example Configuration

These OC7# pins are not used for USB overcurrent protection and should be configured as GPIOs. The unused USB ports can be left as no connect.

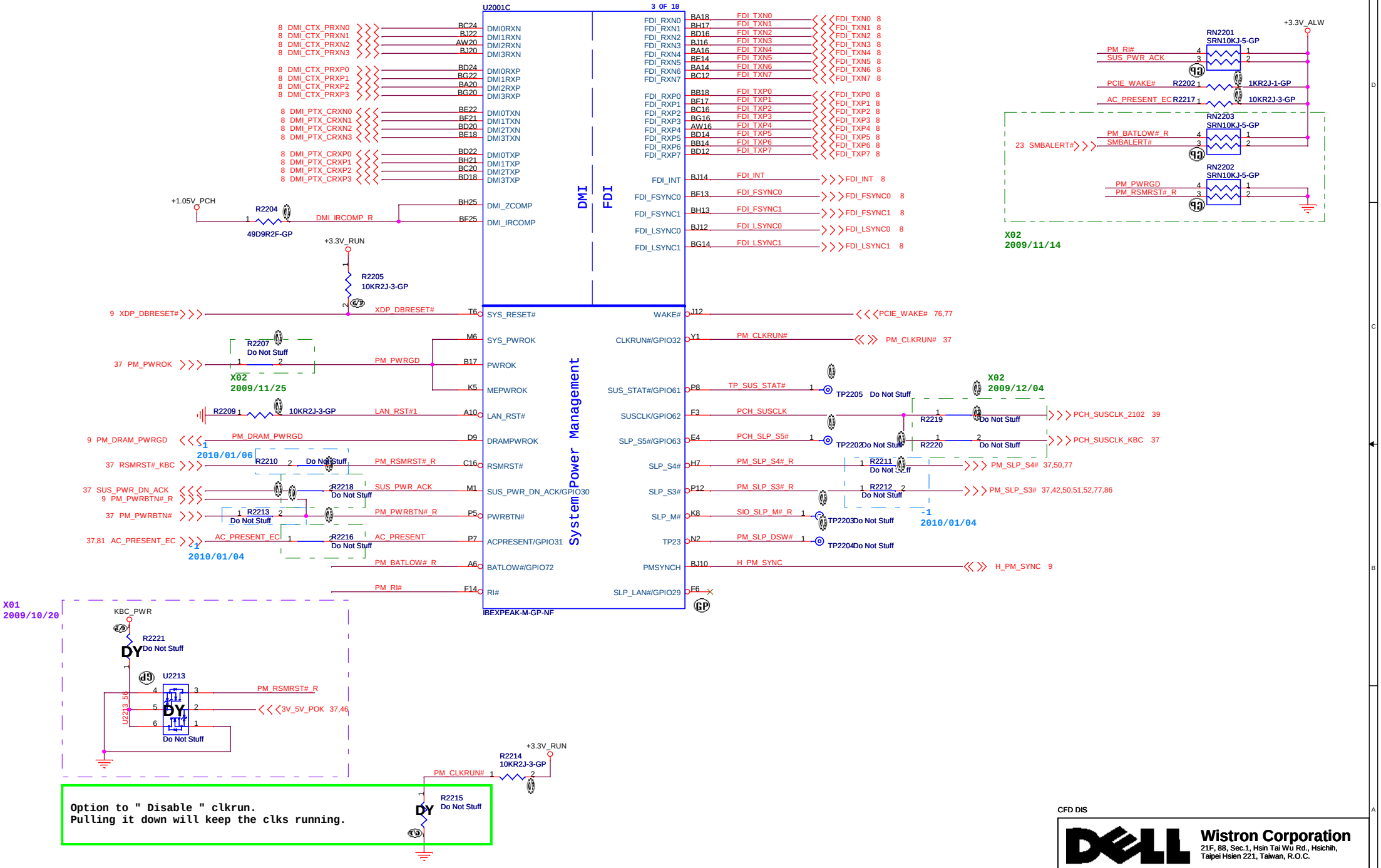
CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

Size | Document Number: Vostro Calpella | Rev: -1

Date: Thursday, February 04, 2010 | Sheet 21 of 95



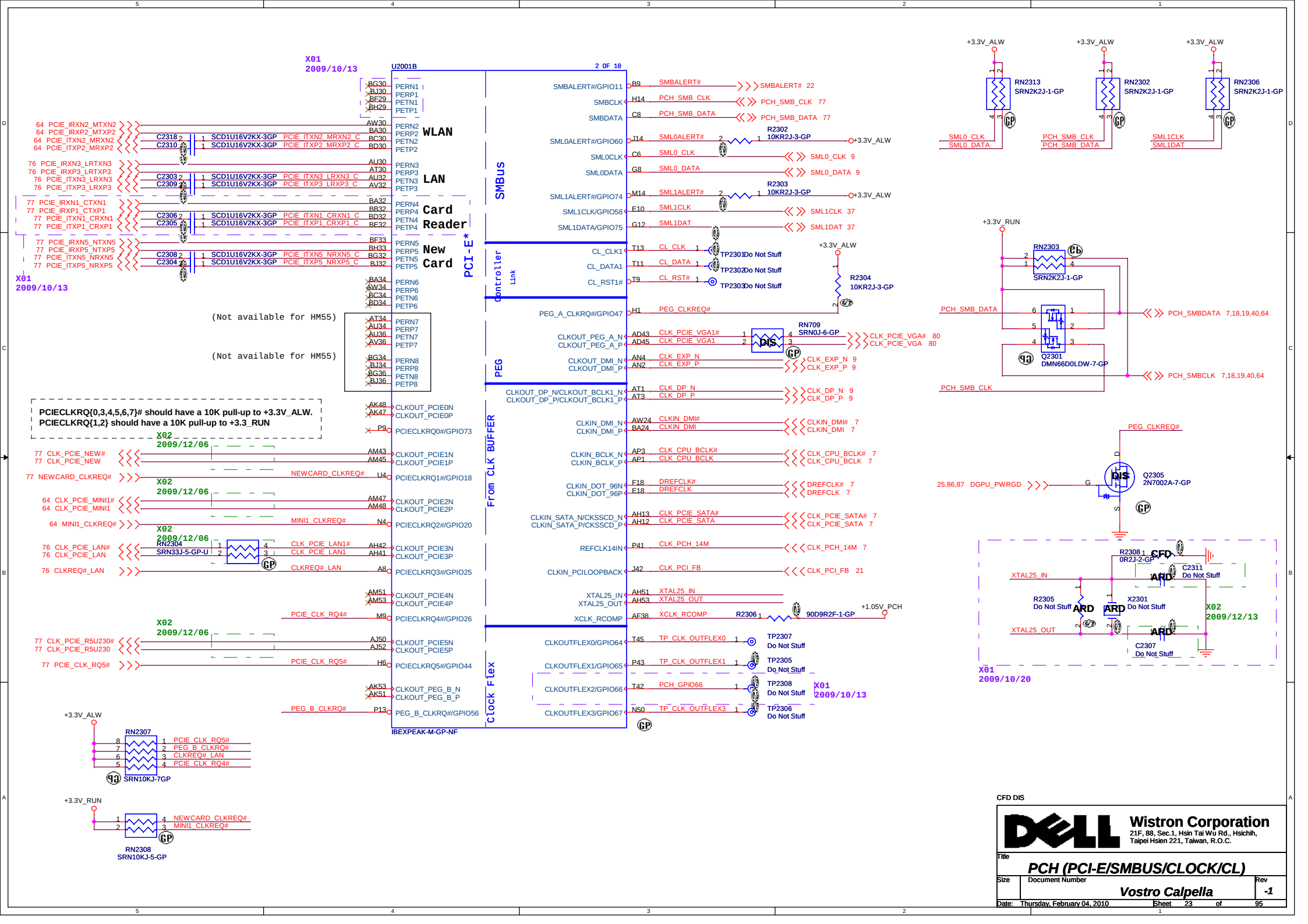
CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**

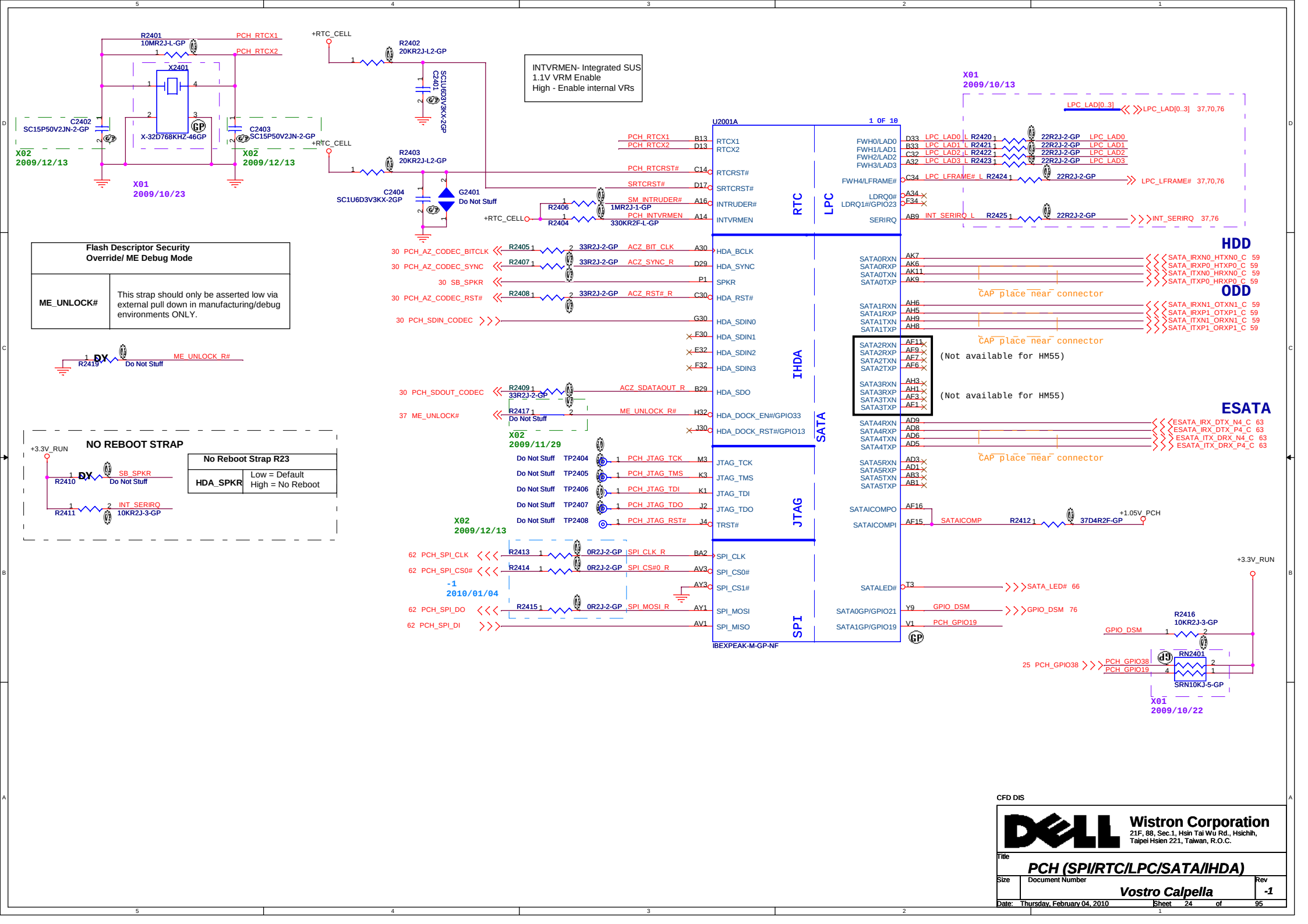
Size	Document Number	Rev
	Vostro Calpella	-1

Date: Thursday, February 04, 2010 Sheet 22 of 95



Title	PCH (PCI-E/SMBUS/CLOCK/CL)
Size	
Document Number	Vostro Calpella
Rev	-1
Date:	Thursday, February 04, 2010
Sheet	23 of 95

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


R2401 10MR2J-L-GP
PCH_RTCX1
PCH_RTCX2
X2401
X-32D768KHZ-46GP
C2402 SC15P50V2JN-2-GP
C2403 SC15P50V2JN-2-GP
X02 2009/12/13
X01 2009/10/23
+RTC_CELL
R2402 20KR2J-L-GP
C2401 SC1U6D3V3KX-2GP
R2403 20KR2J-L-GP
C2404 SC1U6D3V3KX-2GP
G2401 Do Not Stuff
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs
U2001A
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
PCH_RTCRST#
SRTCRST#
SM_INTRUDER#
PCH_INTVRMEN
R2406 1MR2J-1-GP
R2404 330KR2F-L-GP
LPC_LAD[0..3]
LPC_LFRAME#
INT_SERIRQ
HDD
ODD
ESATA
CAP place near connector
(Not available for HM55)
IBEXPEAK-M-GP-NF
Flash Descriptor Security Override/ ME Debug Mode
ME_UNLOCK#
This strap should only be asserted low via external pull down in manufacturing/debug environments ONLY.
R2419 DY Do Not Stuff
NO REBOOT STRAP
No Reboot Strap R23
HDA_SPKR
Low = Default
High = No Reboot
R2410 DY SB_SPKR Do Not Stuff
R2411 INT_SERIRQ 10KR2J-3-GP
X02 2009/11/29
X02 2009/12/13
-1 2010/01/04
X01 2009/10/13
X01 2009/10/22
+3.3V_RUN
+1.05V_PCH
R2412 37D4R2F-GP
R2416 10KR2J-3-GP
RN2401 SRN10KJ-5-GP
CFD DIS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
PCH (SPI/RTC/LPC/SATA/IHDA)
Vostro Calpella
-1
Thursday, February 04, 2010
Sheet 24 of 95

X01
2009/10/13

X02
2009/12/04

X01
2009/10/12

U2001F

6 OF 10

IBEXPEAK-M-GP-NF

PCH_GPIO38 PULL HIGH AT THE PAGE 24.

Placed Within 2" from PCH

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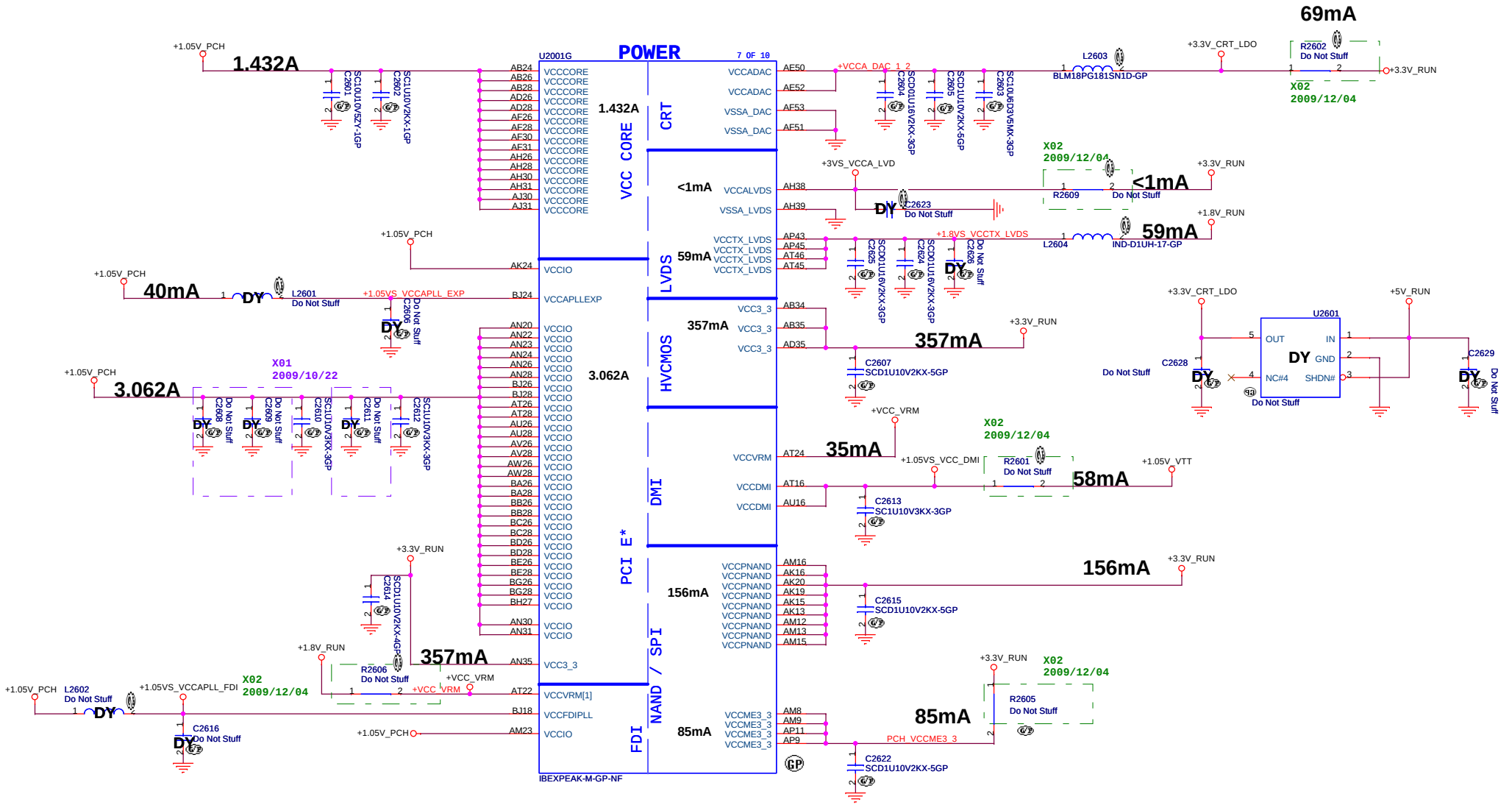
Title: PCH (GPIO/CPU)

Size | Document Number: Vostro Calpella | Rev: -1

Date: Thursday, February 04, 2010 | Sheet 25 of 95


POWER
7 OF 10
U2001G
IBEXPEAK-M-GP-NF
VCC CORE
1.432A
CRT
<1mA
LVDS
59mA
HVCMOS
357mA
3.062A
PCI E*
DMI
35mA
58mA
NAND / SPI
156mA
FDI
85mA
69mA
+1.05V_PCH
+3.3V_CRT_LDO
+3.3V_RUN
+1.8V_RUN
+5V_RUN
+1.05V_VTT
+VCC_VRM
+1.05VS_VCCAPLL_FDI
+1.05VS_VCCAPLL_EXP
+1.05VS_VCC_DMI
+3VS_VCCA_LVD
+1.8VS_VCCTX_LVDS
+VCCA_DAC_1_2
PCH_VCCME3_3
X01
2009/10/22
X02
2009/12/04
Do Not Stuff
DY
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Taipei Hsien 221, Taiwan, R.O.C.
CFD DIS
PCH (POWER1)
Vostro Calpella
-1
Thursday, February 04, 2010
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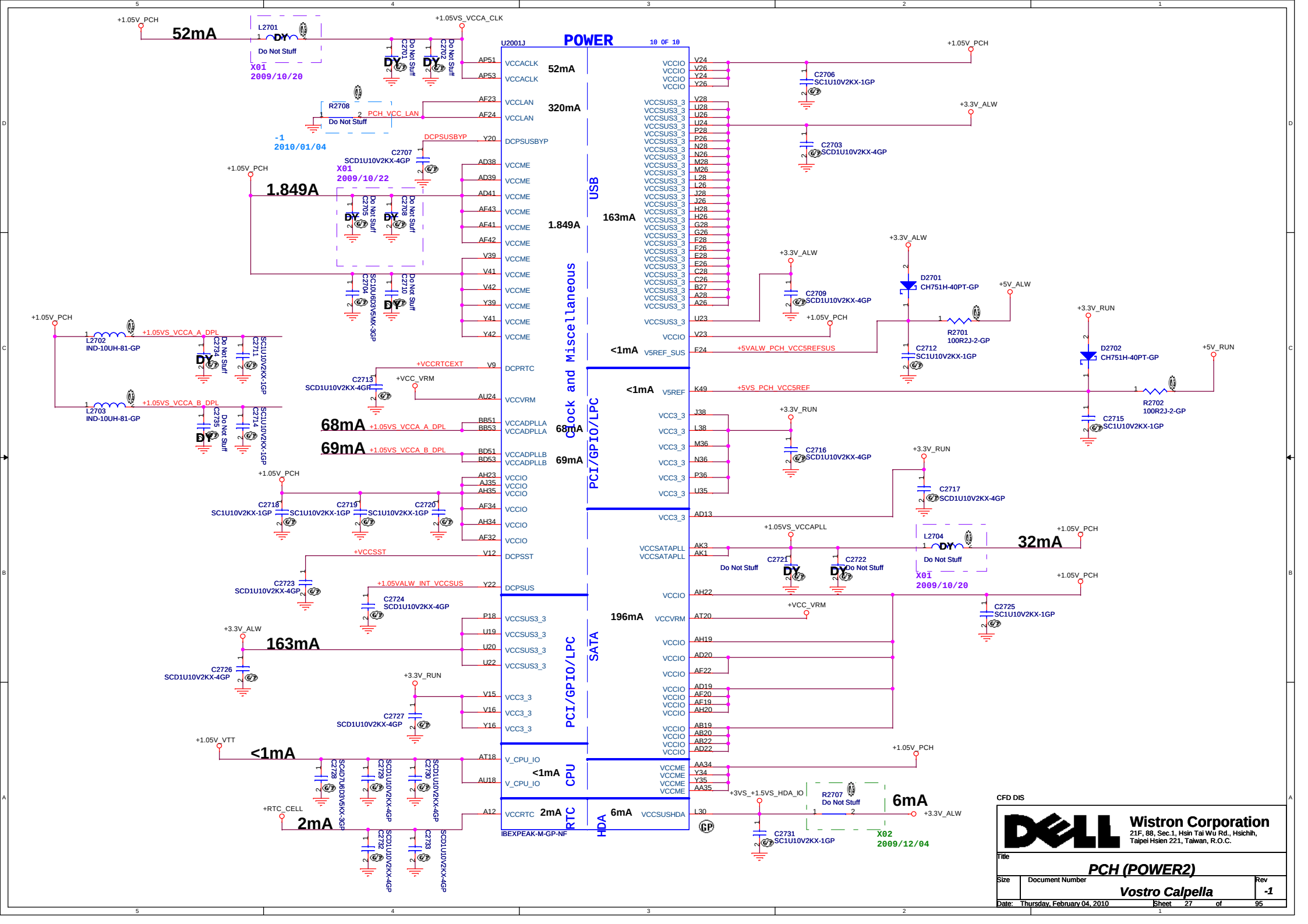

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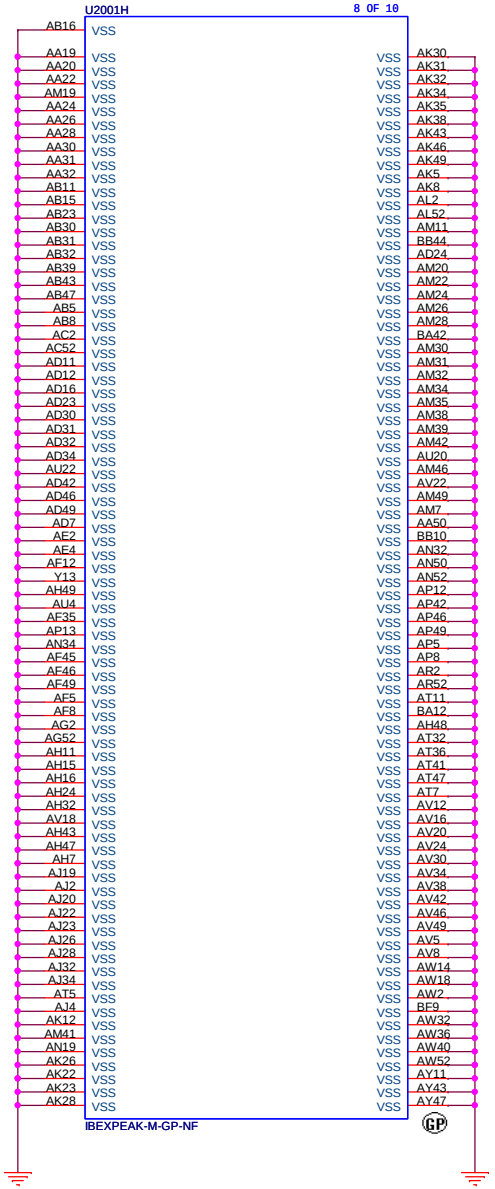
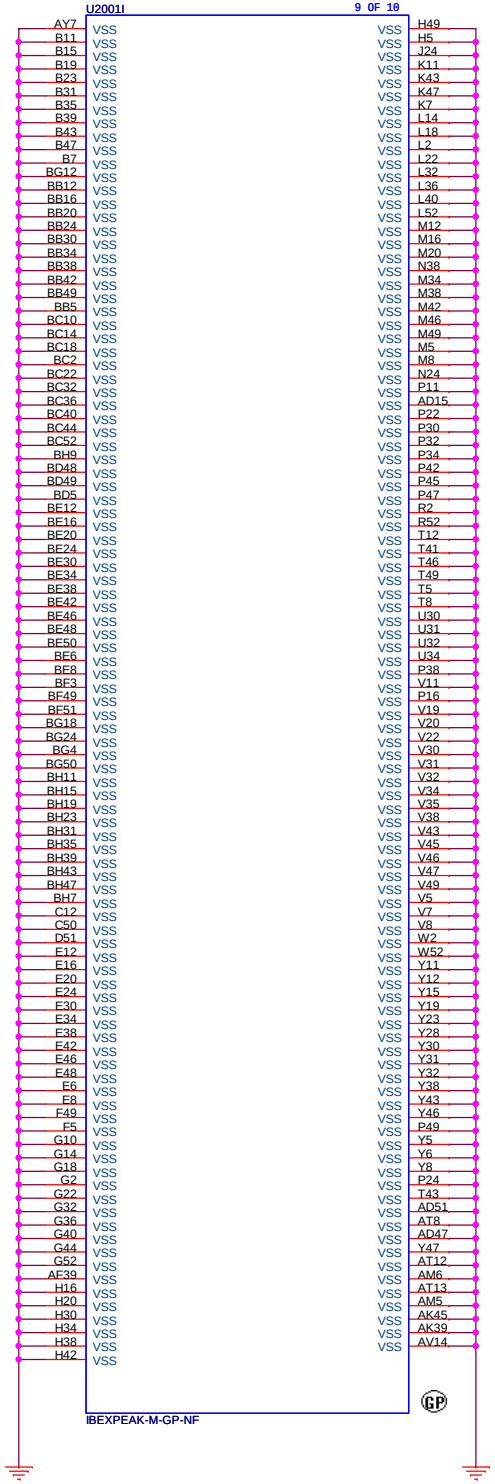
Title: PCH (POWER2)

Size	Document Number	Rev
	Vostro Calpella	-1

Date: Thursday, February 04, 2010 Sheet 27 of 95





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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size	Document Number	Rev
	Vostro Calpella	*-1*

Date: Thursday, February 04, 2010 Sheet 28 of 95

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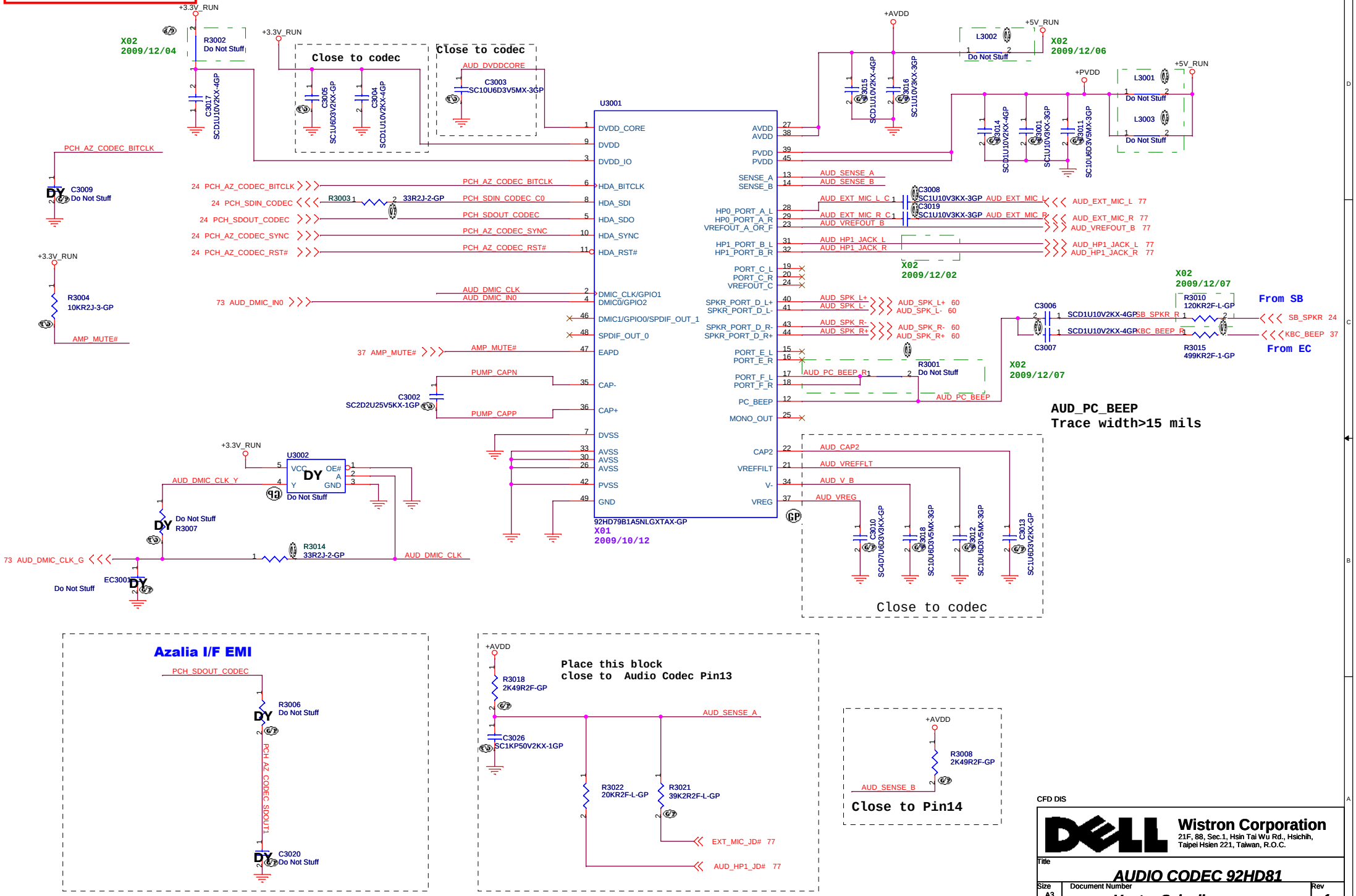
Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*-1*

Date: Thursday, February 04, 2010 Sheet 29 of 95

SSID = AUDIO



CFD DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CODEC 92HD81**

Size	Document Number	Rev
A3	Vostro Calpella	-1

Date: Thursday, February 04, 2010 Sheet 30 of 95

(Blank)

CFD DIS

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Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*-1*

Date: Thursday, February 04, 2010 Sheet 31 of 95

(Blank)

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Title

Reserve

Size	Document Number	Rev
A3	***Vostro Calpella***	*-1*

Date: Thursday, February 04, 2010 Sheet 32 of 95

(Blank)

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Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*-1*

Date: Thursday, February 04, 2010 Sheet 33 of 95

(Blank)

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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*-1*

Date: Thursday, February 04, 2010 Sheet 34 of 95

(Blank)

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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
A3	*Vostro Calpella*	*-1*

Date: Thursday, February 04, 2010 Sheet 35 of 95

CFD DIS

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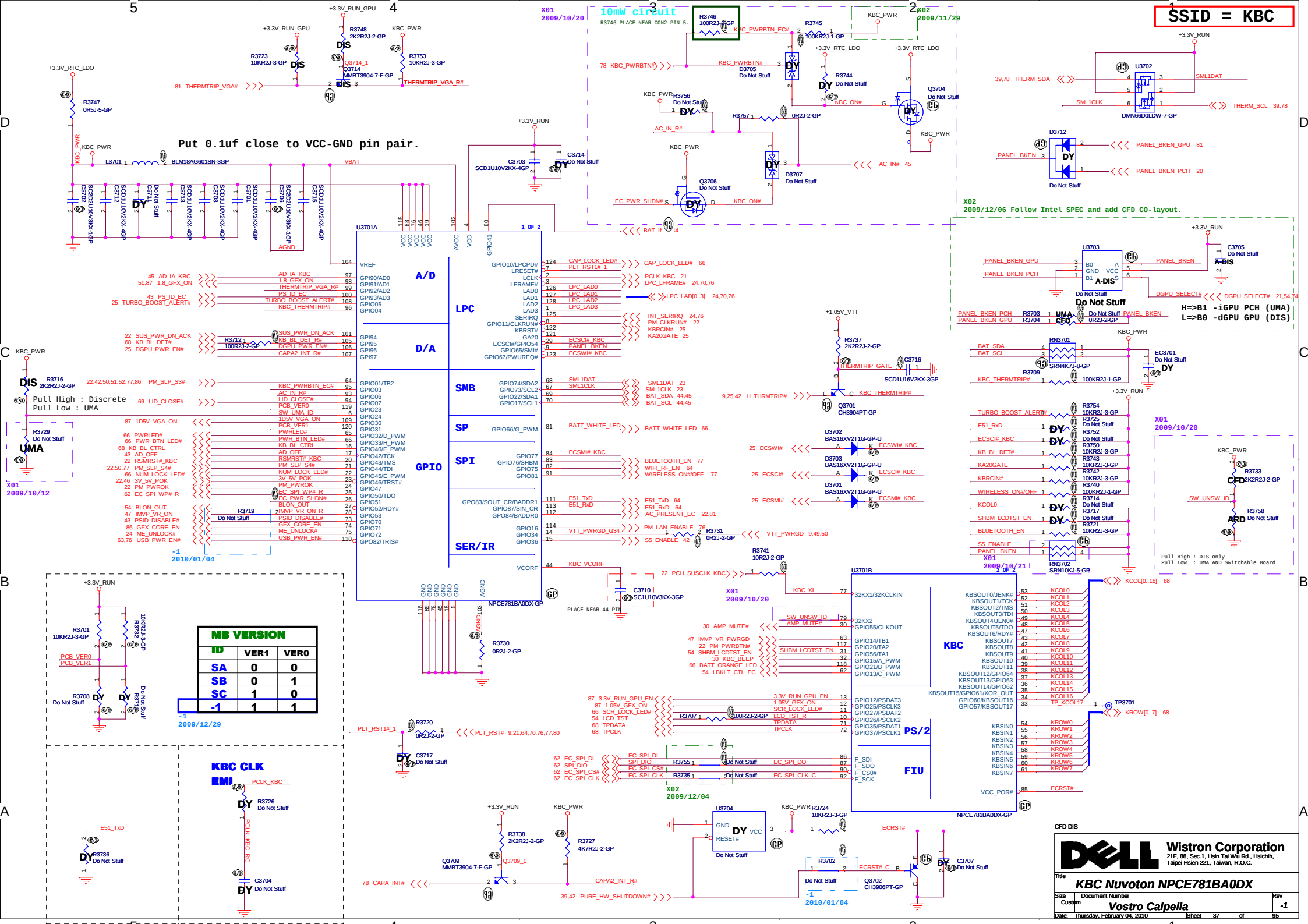
Taipei Hsien 221, Taiwan, R.O.C.

Title

TPM

Size	Document Number	Rev
Custom	***Vostro Calpella***	***-1***

Date: Thursday, February 04, 2010 Sheet 36 of 95


SSID = KBC
10mW circuit
R3746 PLACE NEAR CON2 PIN 5.
X01 2009/10/20
X02 2009/11/29
X02 2009/12/06 Follow Intel SPEC and add CFD CO-layout.
Put 0.1uf close to VCC-GND pin pair.
U3701A
1 OF 2
A/D
LPC
D/A
GPIO
SMB
SP
SPI
SER/IR
U3701B
2 OF 2
KBC
PS/2
FIU
NPCE781BA0DX-GP
Pull High : Discrete
Pull Low : UMA
UMA
Do Not Stuff
MB VERSION
ID | VER1 | VER0
SA | 0 | 0
SB | 0 | 1
SC | 1 | 0
-1 | 1 | 1
2009/12/29
KBC CLK EMI
Pull High : DIS only
Pull Low : UMA AND Switchable Board
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)
CFD DIS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC Nuvoton NPCE781BA0DX
Size Custom
Document Number
Vostro Calpella
Rev -1
Date: Thursday, February 04, 2010
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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*-1*

Date: Thursday, February 04, 2010 Sheet 38 of 95

SSID = Thermal

1. CPU System Sensor

Q3905 must be near CPU
C3912 must be near Q3905
C3914 must be near EMC2102

Q3905 PMBS3904-1-GP
C3912 DY Do Not Stuff
C3914 SC470P50V3JN-2GP

Layout notice:
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

2. GPU Sensor (DIS)

C3906 must be near EMC2102

RN3903 SRN0J-6-GP
81 VGA_THERMDC
81 VGA_THERMDA
X02
2009/12/02
C3906 SC470P50V3JN-2GP

C3913 must be near Q3904

CH2_TDC
RN3904 Do Not Stuff
Q3904 Do Not Stuff
C3913 Do Not Stuff
UMA
CH2_TDA

Layout notice :
Both VGA_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing.

C3901 must be near Q3901

Q3901 MMBT3904-3-GP
C3901 DY Do Not Stuff
C3903 SC470P50V3JN-2GP
C3903 must be near EMC2102

3.HW T8 sensor

Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

32K suspend clock output

Q3902 2N7002A-7-GP
22 PCH_SUSCLK_2102
CLK_32K_R
R3913 10R2J-2-GP
CLK_32K
C3911 DY Do Not Stuff
RUN_POWER_ON 42

+5V_RUN
25mil
C3910 SC4D7U6D3V5KX-3GP
C3909 SCD1U16V2KX-3GP

+3.3V_RUN
R3907 10KR2J-3-GP
R3912 Do Not Stuff
D3901 B0530WS-7-F-GP
+5V_RUN
R3901 DY Do Not Stuff

EMC2102_FAN_TACH
EMC2102_FAN_TACH_1
EMC2102_FAN_TACH_1 58
EMC2102_FAN_DRIVE
EMC2102_FAN_DRIVE 58
25mil

RN3901 SRN4K7J-8-GP
+3.3V_RUN
THERM_SCL 37,78
THERM_SDA 37,78

+3.3V_RUN
R3908 49D9R2F-GP
EMC2102_VDD_3D3
C3905 SCD1U16V2KX-3GP

U3901 EMC2102

29	28	27	26	25	24	23	22	1	2	3	4	5	6	7
GND	TACH	VDD_5Va	FANa	FANb	VDD_5Vb	SMCLK	SMDATA	VDD_3V	DN1	DP1	DN2	DP2	DN3	DP3

8	9	10	11	12	13	14	21	20	19	18	17	16	15	
NC#8	SHDN_SEL	FAN_MODE	TRIP_SET	SYS_SHDN#	THERMTRIP#	POWER_OK#	NC#21	GND	ALERT#	CLK_IN	CLK_SEL	RESET#	NC#15	EMC2102-DZK-GP

TP3903 Do Not Stuff
TP3904 Do Not Stuff
R3906 10KR2J-3-GP
+3.3V_RUN
CLK_32K
EMC2102_CLK_SEL
TP_EM2102_RESET#
TP_ALERT#

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

R3903 DY Do Not Stuff
EMC2102_SHDN
R3916 DY Do Not Stuff
EMC2102_FAN_mode
R3914 10KR2J-3-GP

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

EMC2102_PWROK
EMC2102_THERMTRIP#
RN3902 SRN10KJ-5-GP
+3.3V_RUN

+3.3V_RUN
R3910 10KR2J-3-GP
SYS_SHDN#
SHDN
Q3903 2N7002A-7-GP
KBC_PWR
R3917 10KR2J-3-GP
PURE_HW_SHUTDOWN# 37,42
V_DEGREE

+3.3V_RUN
C3902 SCD1U16V2KX-3GP
R3902 10KR2F-2-GP
C3904 SCD1U16V2KX-3GP
R3904 2K37R2F-GP

TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)
T8 shutdown is set 88 deg-C.

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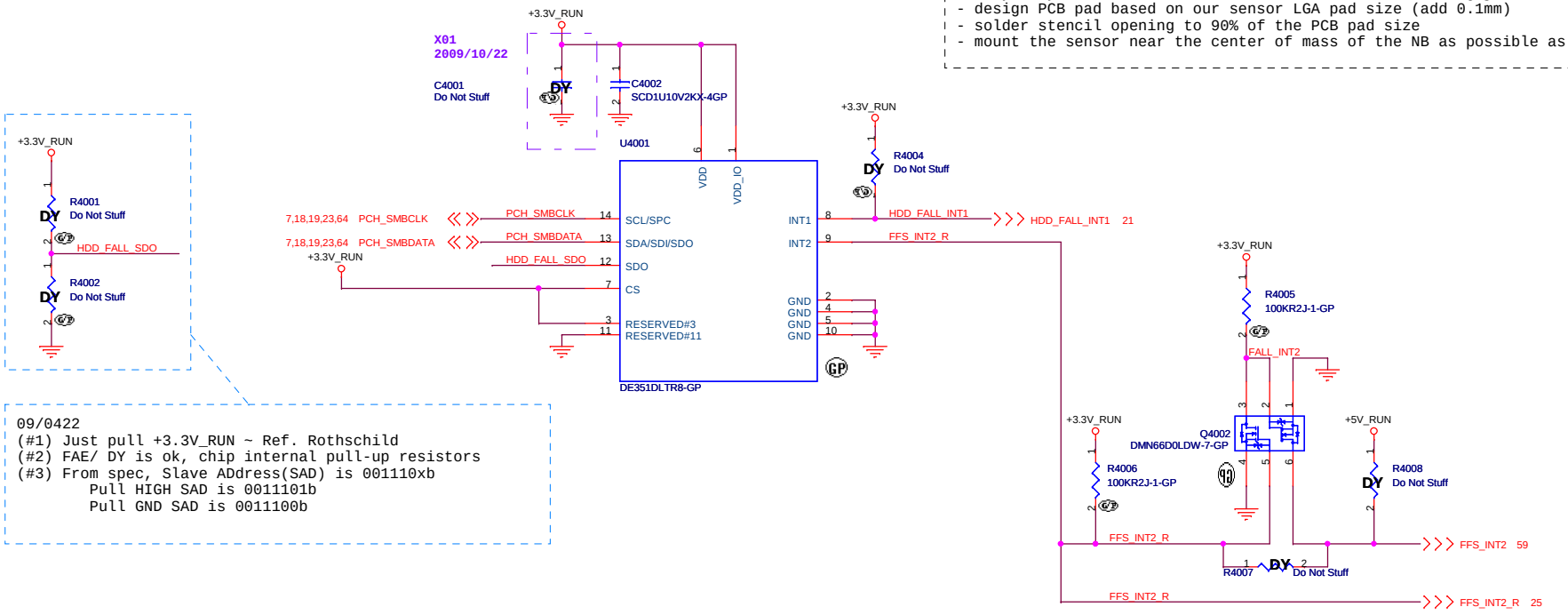
Title: Thermal/Fan Controllor EMC2102
Size: Custom
Document Number: Vostro Calpella
Rev: -1
Date: Thursday, February 04, 2010
Sheet 39 of 95

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave ADdress(SAD) is 001110xb
Pull HIGH SAD is 0011101b
Pull GND SAD is 0011100b

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

CFD DIS

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Title: Free Fall Sensor

Size: Custom | Document Number: Vostro Calpella | Rev: -1

Date: Thursday, February 04, 2010 | Sheet 40 of 95

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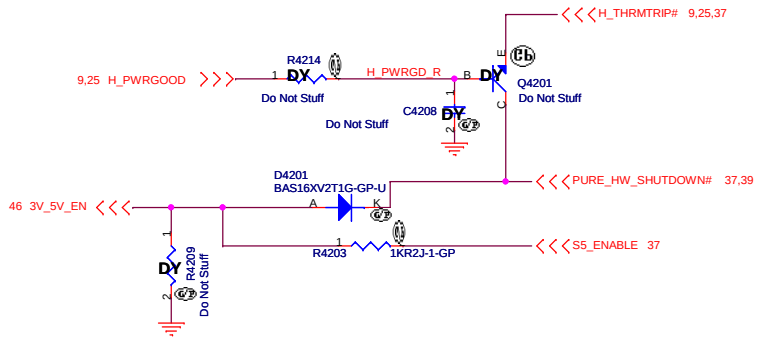
Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*-1*

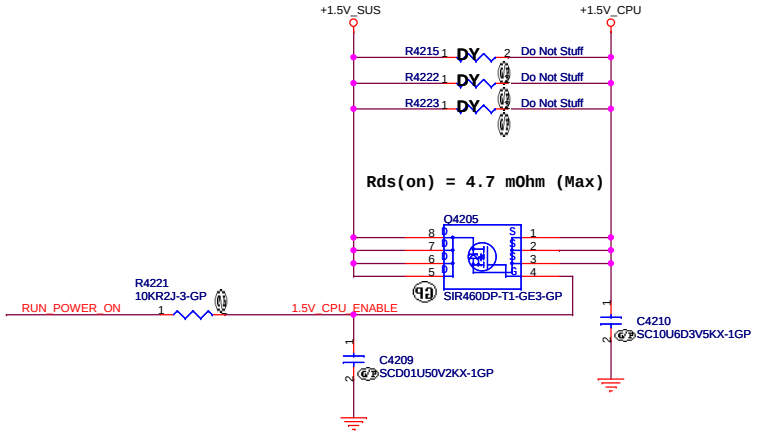
Date: Thursday, February 04, 2010 Sheet 41 of 95

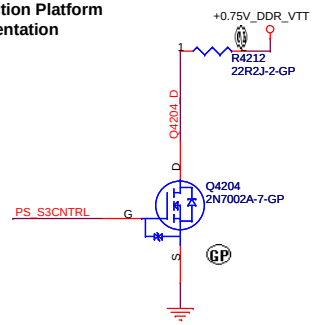
SSID = Reset.Suspend

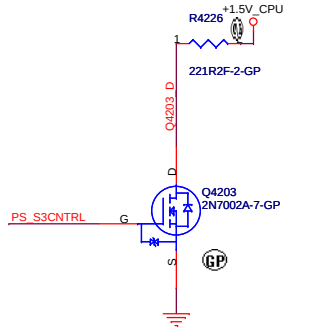


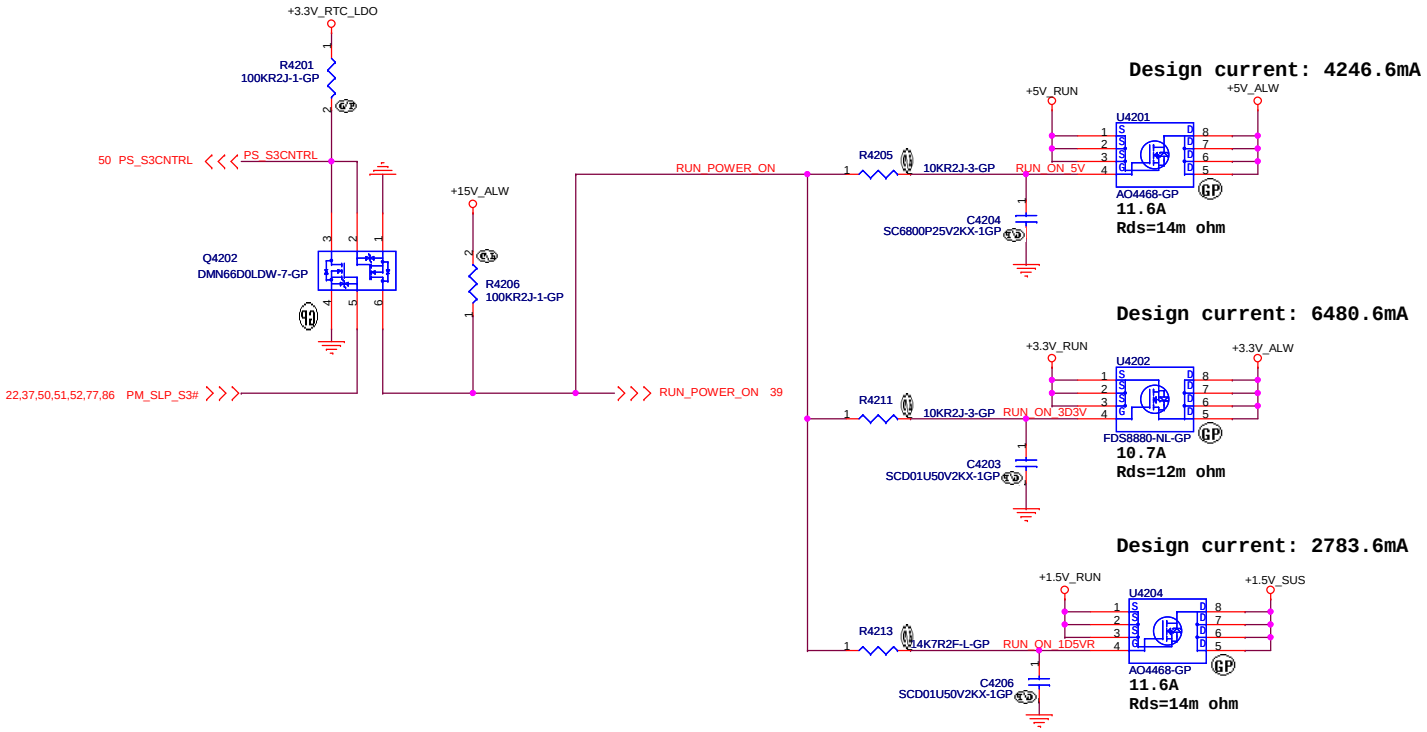
+1.5V_CPU:

Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details









CFD DIS

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Title: ***Power Plane Enable***

Size	Document Number	Rev
Custom	***Vostro Calpella***	-1

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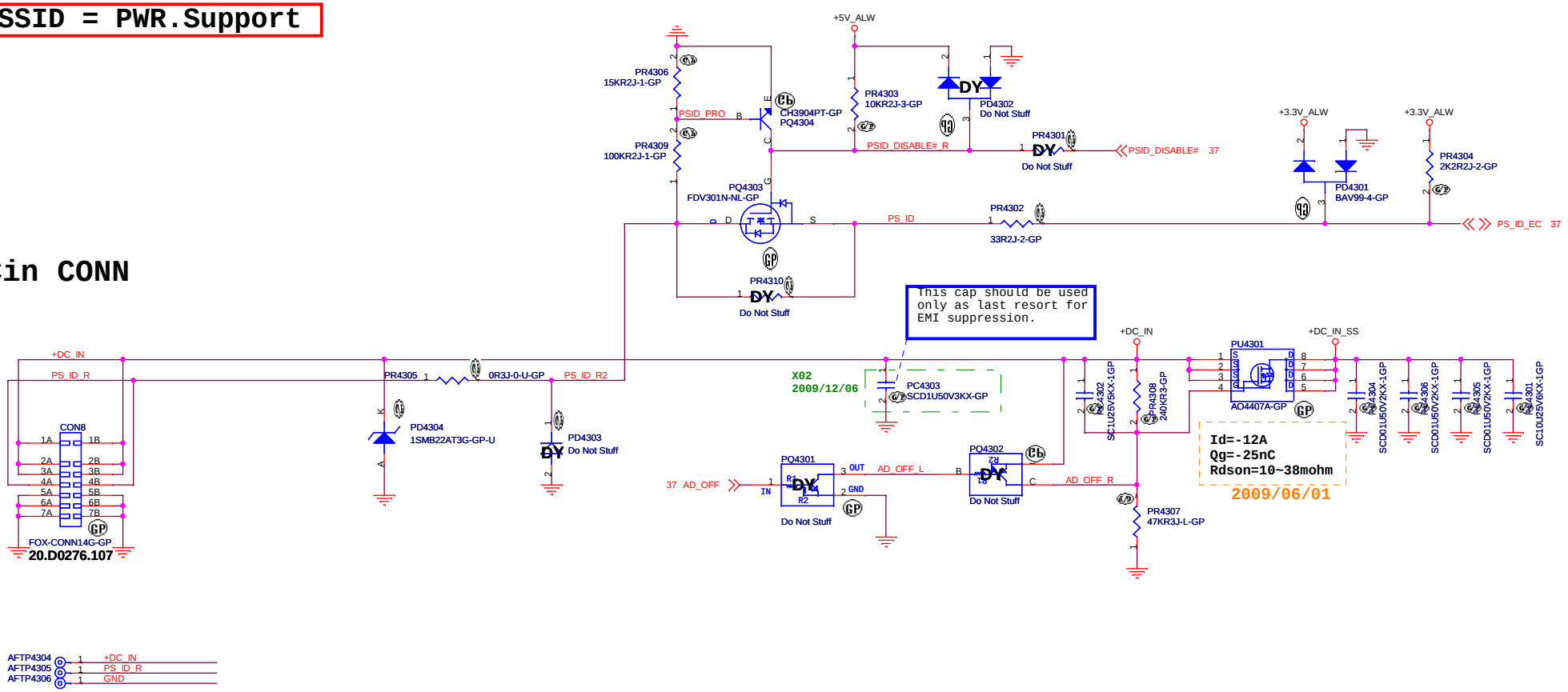
SSID = PWR.Support

DCin CONN



CFD DIS

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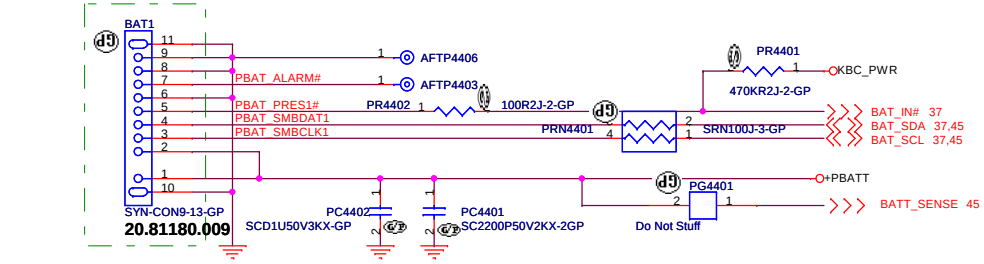
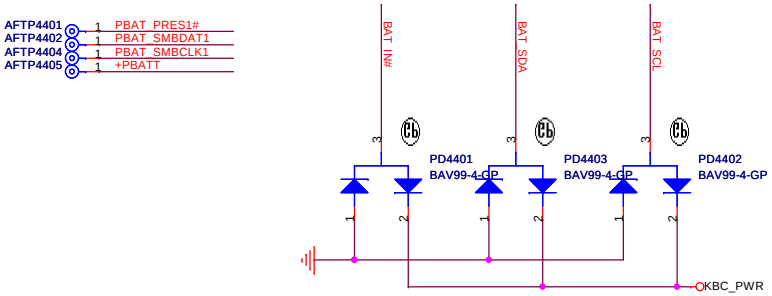
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC IN	
Size: Custom	Document Number: Vostro Montevina Discrete	Rev: -1
Date: Thursday, February 04, 2010	Sheet 43 of 95	

Batt Connecter

X02
2009/12/06





CFD DIS

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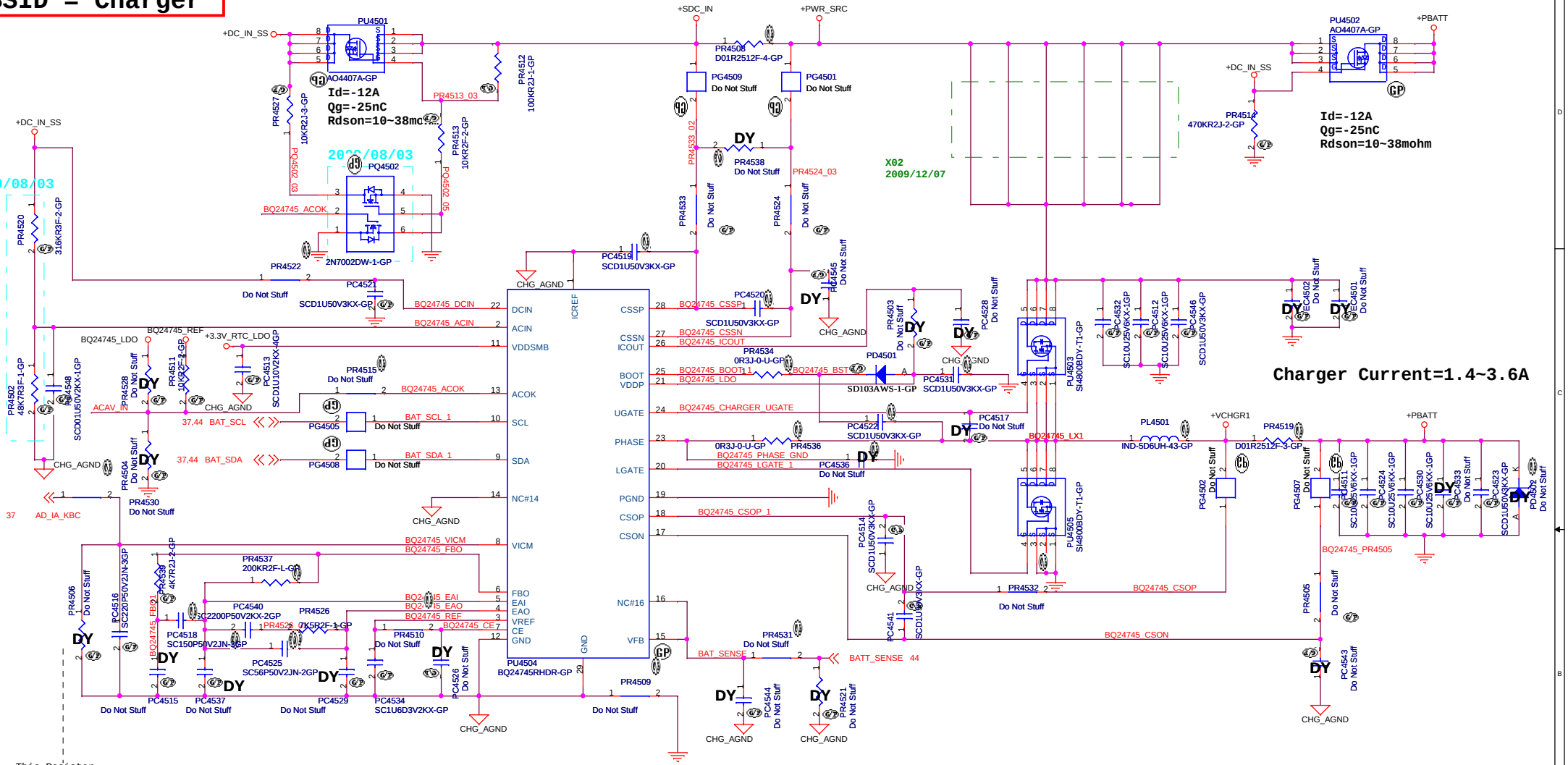
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT CONN	
Size: A3	Document Number: Vostro Montevina Discrete	Rev: -1
Date: Thursday, February 04, 2010	Sheet 44 of 95	

SSID = Charger



CFD DIS

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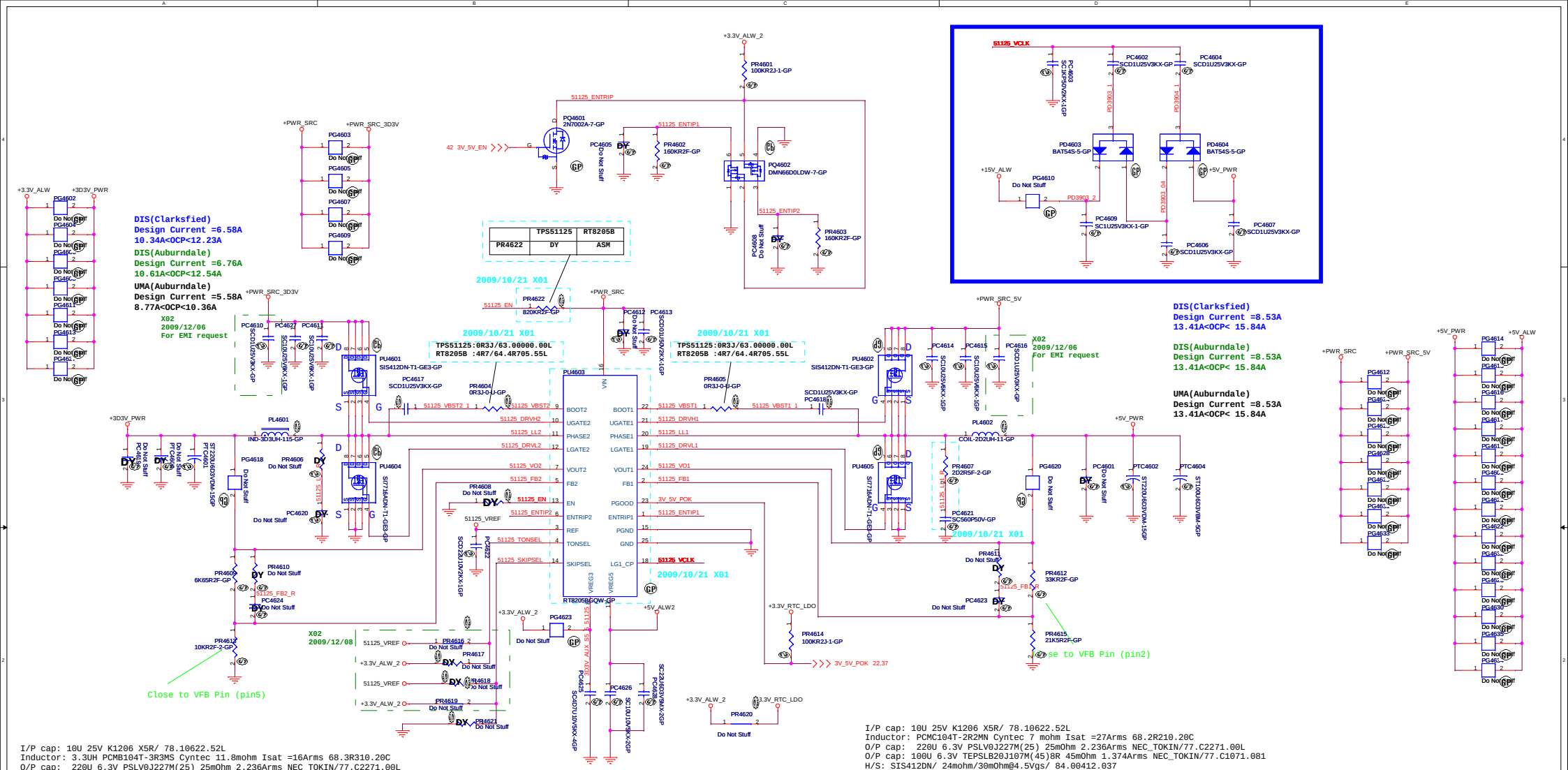
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

Size: Custom | Document Number: DW Calpella | Rev: -1

Date: Thursday, February 04, 2010 | Sheet 45 of 95



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cyntec 11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: PCMC104T-2R2MN Cyntec 7 mohm Isat =27Arms 68.2R210.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

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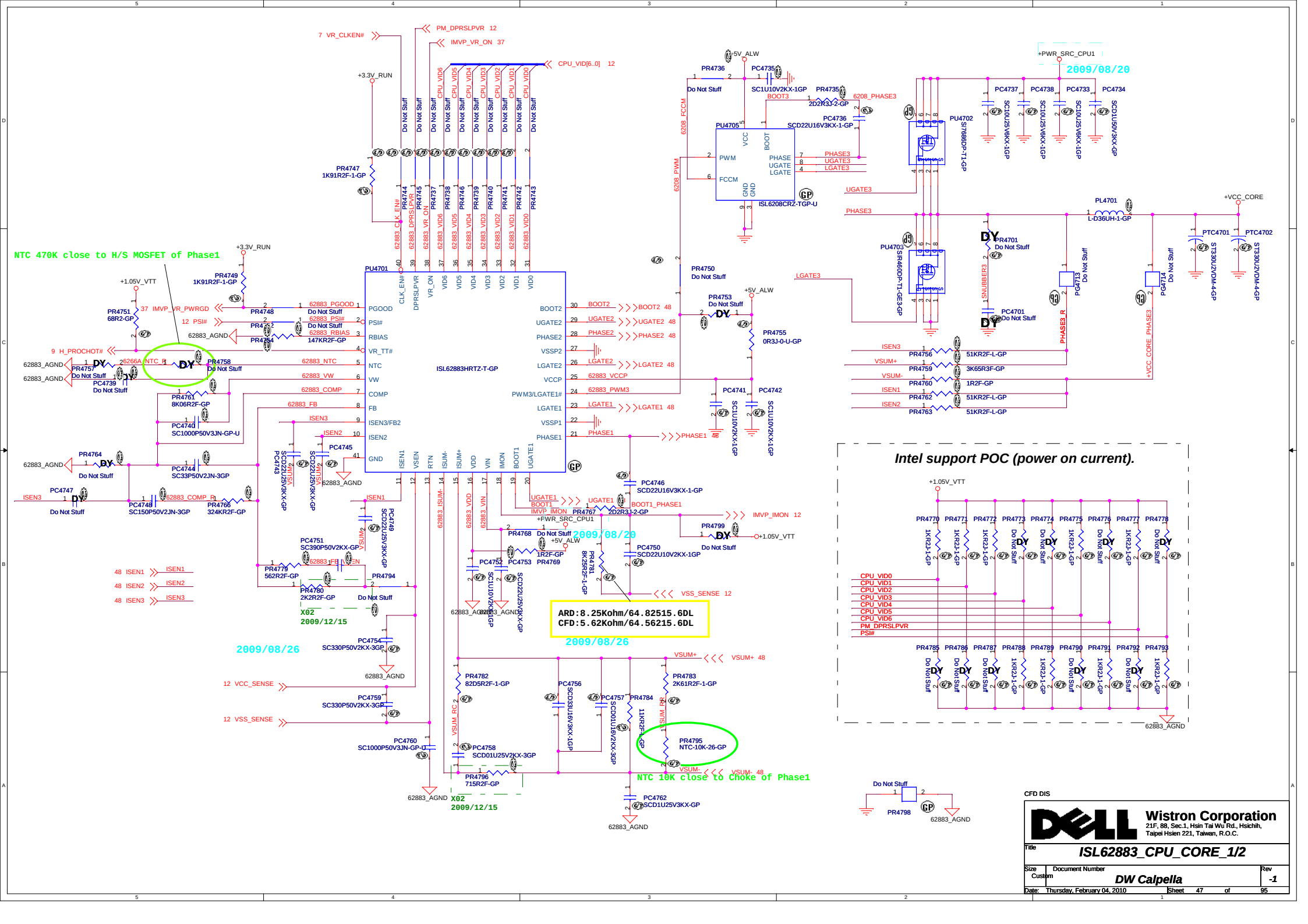
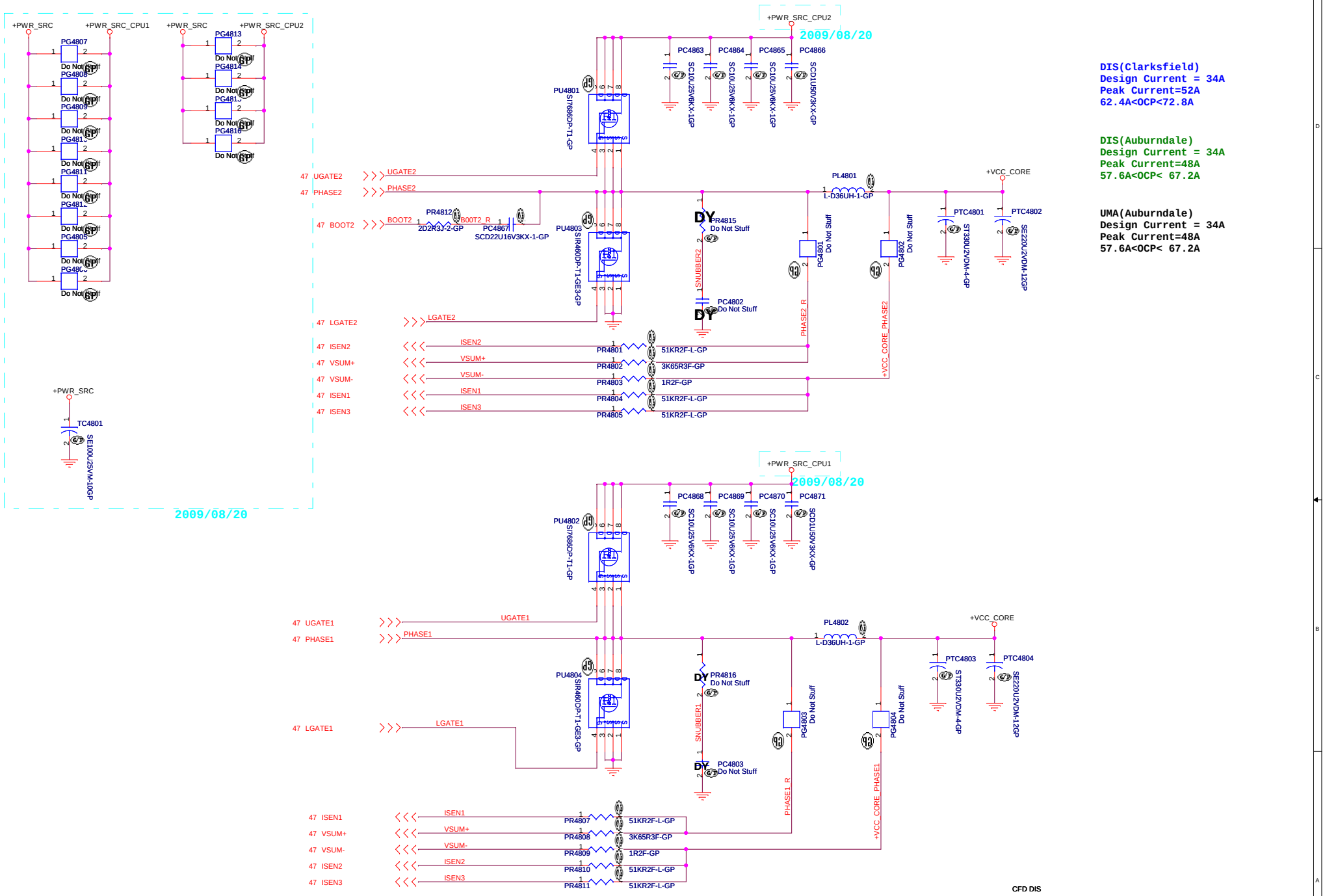
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8205B_5V/3D3V

Size: Custom | Document Number: DW Calpella | Rev: -1

Date: Thursday, February 04, 2010 | Sheet 46 of 95


NTC 470K close to H/S MOSFET of Phase1
PU4701
ISL62883HRTZ-T-GP
PU4705
ISL6208CRZ-TGP-U
PU4702
PU4703
SI7686DP-T1-GP
SIR460DP-T1-GE3-GP
PL4701
L-D36UH-1-GP
+PWR_SRC_CPU1
2009/08/20
+VCC_CORE
Intel support POC (power on current).
ARD:8.25Kohm/64.82515.6DL
CFD:5.62Kohm/64.56215.6DL
2009/08/26
X02
2009/12/15
NTC 10K close to Choke of Phase1
CFD DIS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL62883_CPU_CORE_1/2
DW Calpella
-1
Thursday, February 04, 2010
47
95



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
O/P cap: 220U 2V EEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Freq=300KHz@PER PHASE

CFD DIS

Wistron Corporation
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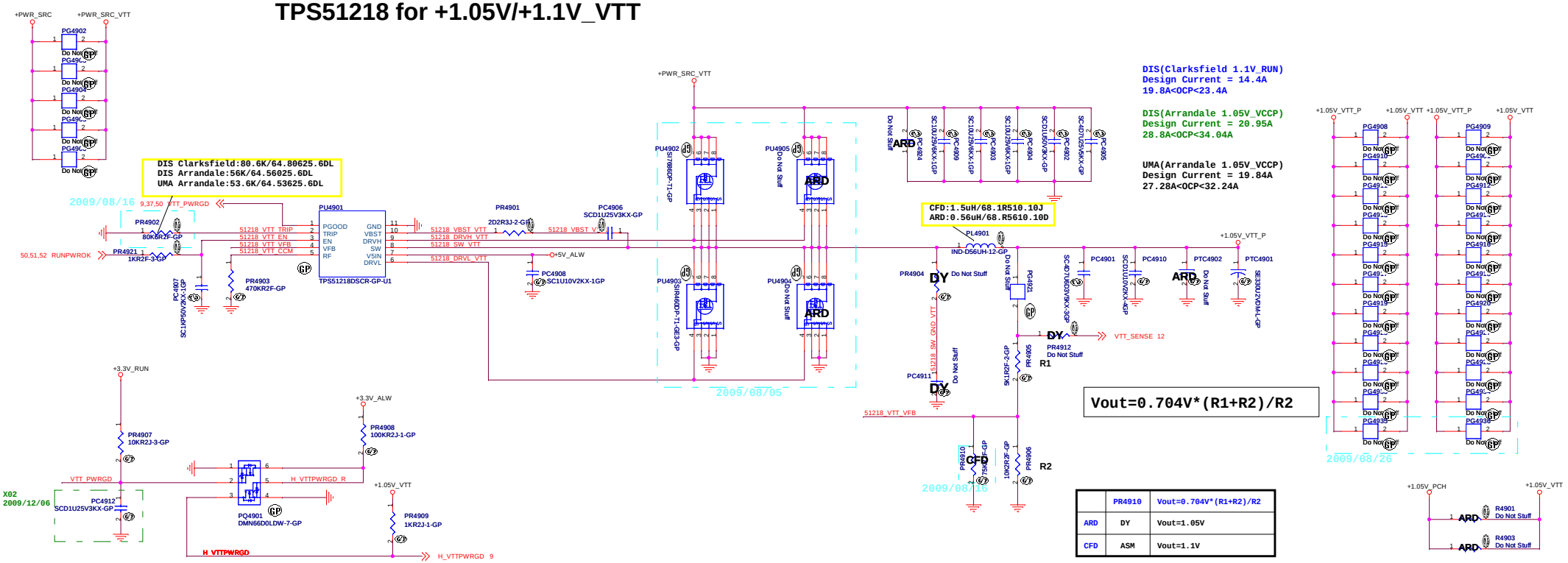
Taipei Hsien 221, Taiwan, R.O.C.

Title	ISL62883_CPU_CORE_2/2	
Size: Custom	Document Number: DW Calpella	Rev: -1
Date: Thursday, February 04, 2010	Sheet 48 of 95	

TPS51218 for +1.05V/+1.1V_VTT



	PR4910	Vout=0.704V*(R1+R2)/R2
ARD	DY	Vout=1.05V
CFD	ASM	Vout=1.1V

Frequency setting

470K	-->290KHz
200K	-->340KHz
100K	-->380KHz
39K	-->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
Inductor: 1.5uH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat=33Arms 68.1R510.10J
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

CFD DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218_+1.05V_VTT

Size	Document Number	Rev
Custom	DJ1 Discrete	-1

Date: Thursday, February 04, 2010 Sheet 49 of 95

SSID = PWR.Plane.Regulator_1p5v0p75v

DIS Clarksfield:11.5K/64.11525.6DL
DIS Arrandale:9.76K/64.97615.6DL
UMA Arrandale:6.65K/64.66515.6DL

2009/08/16

425302_425302_Calpella_S3PowerReduction_WhitePape Revision 0.9

TPS51116RGER-GP-U

X02
2009/11/25

Design Current = 0.7A

2009/08/05

DIS(Clarksfied)
Design Current = 14.52A
22.82A<OCP<26.97A

DIS(Auburndale)
Design Current = 12.42A
19.52A<OCP<23.07A

UMA(Auburndale)
Design Current = 8.51A
13.37A<OCP<15.8A

DIS:1.0uH/68.1R01A.20A
UMA:1.5uH/68.1R510.10J

DIS:EEFSX0D331ER/79.33719.L01
UMA:EEFCX0D221R/79.22719.20L

X02
2009/12/08

Close to VFB Pin (pin5)

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.0uH PCMC104T-1R0MN Cyntec DCR:3.5mohm Isat=40Arms 68.1R01A.20A
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz

CFD DIS

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Taipei Hsien 221, Taiwan, R.O.C.

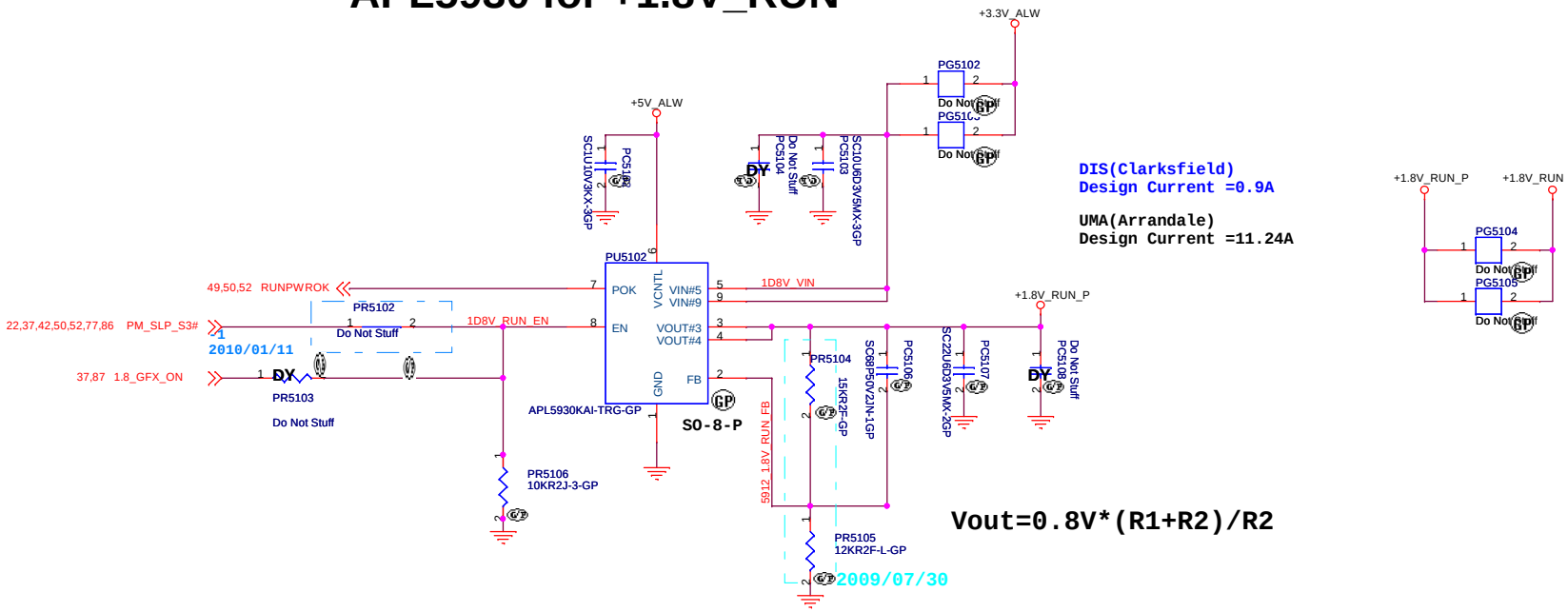
Title: TPS51116_+1.5V_SUS

Size	Document Number	Rev
Custom	DW Calpella	-1

Date: Thursday, February 04, 2010 Sheet 50 of 95

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



CFD DIS

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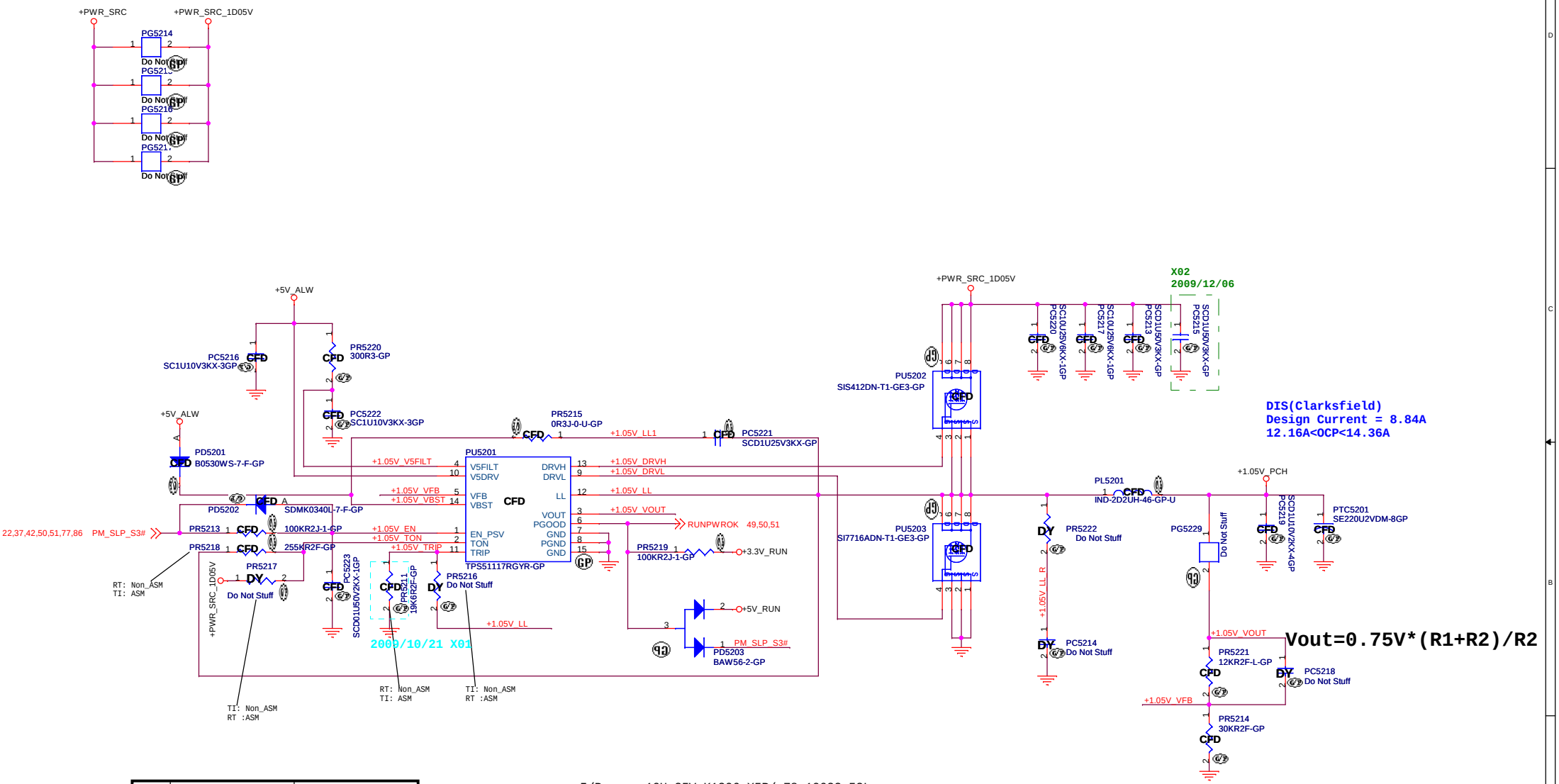
Taipei Hsien 221, Taiwan, R.O.C.

Title	*APL5930 +1.8V_RUN*	
Size: A3	Document Number: *DW Calpella*	Rev: *-1*
Date: Thursday, February 04, 2010	Sheet 51 of 95	

SSID = PWR.Plane.Regulator_1p05v



	ASM	Non_ASM
TI	PR5218, PR5211	PR5217, PR5216
RT	PR5217, PR5216	PR5218, PR5211

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor:2.2UH PCMC063T-2R2MN Cyntec DCR:20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037
Switching freq-->320KHz

CFD DIS

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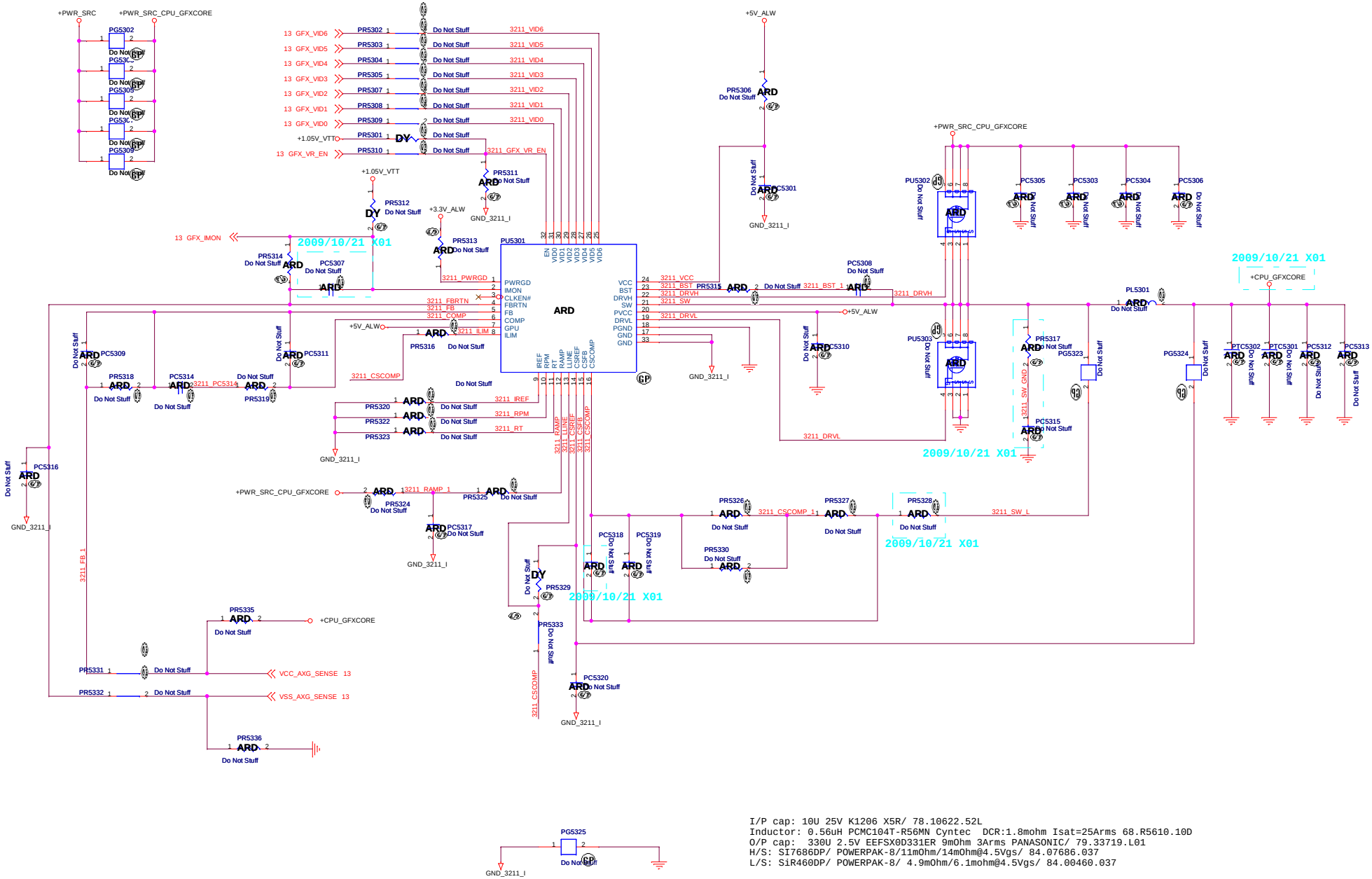
Title	DC to DC 1.05V	
Size: A3	Document Number: DW Calpella (Clarksfield)	Rev: -1
Date: Thursday, February 04, 2010	Sheet 52 of 95	

SSID = CPU.GFX.Regulator



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

CFD DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP3211 CPU_GFXCORE

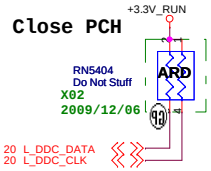
Size	Document Number	Rev
Custom	DW Calpella UMA	-1

Date: Thursday, February 04, 2010 Sheet 53 of 95

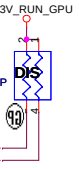
SSID = VIDEO

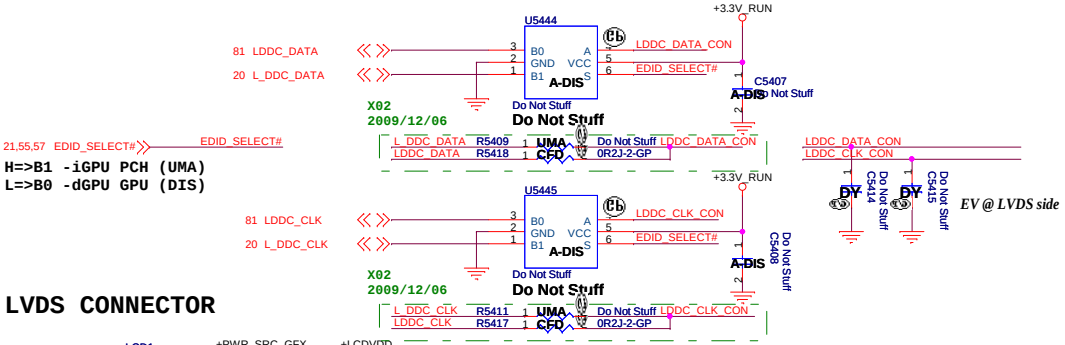
UMA/DIS LVDS DDC CLK/DAT select circuit

Close PCH

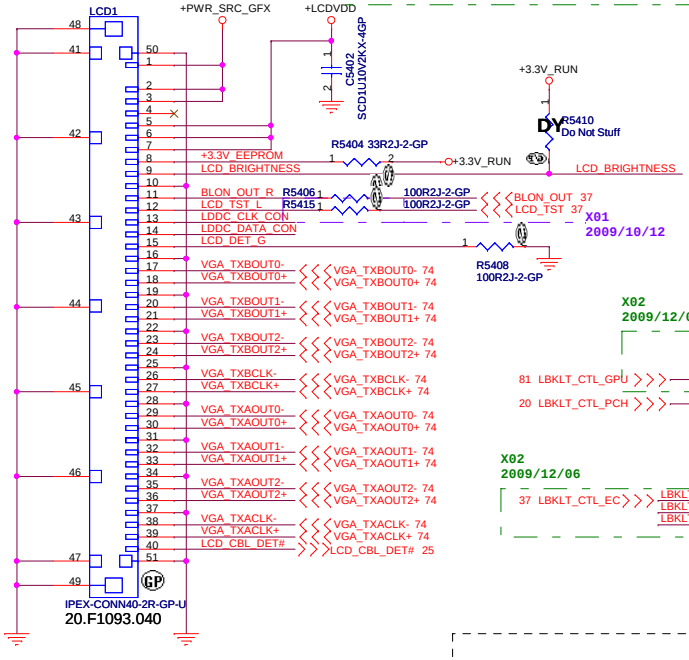


Close GPU

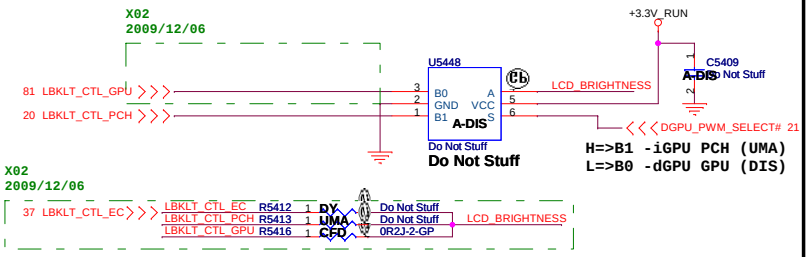


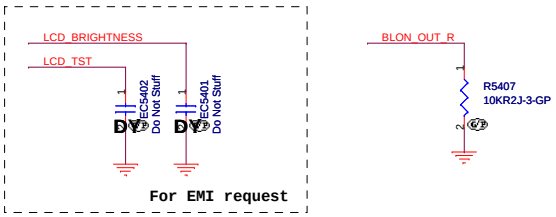


LVDS CONNECTOR



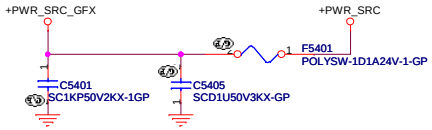
UMA/DIS LVDS PWM select circuit





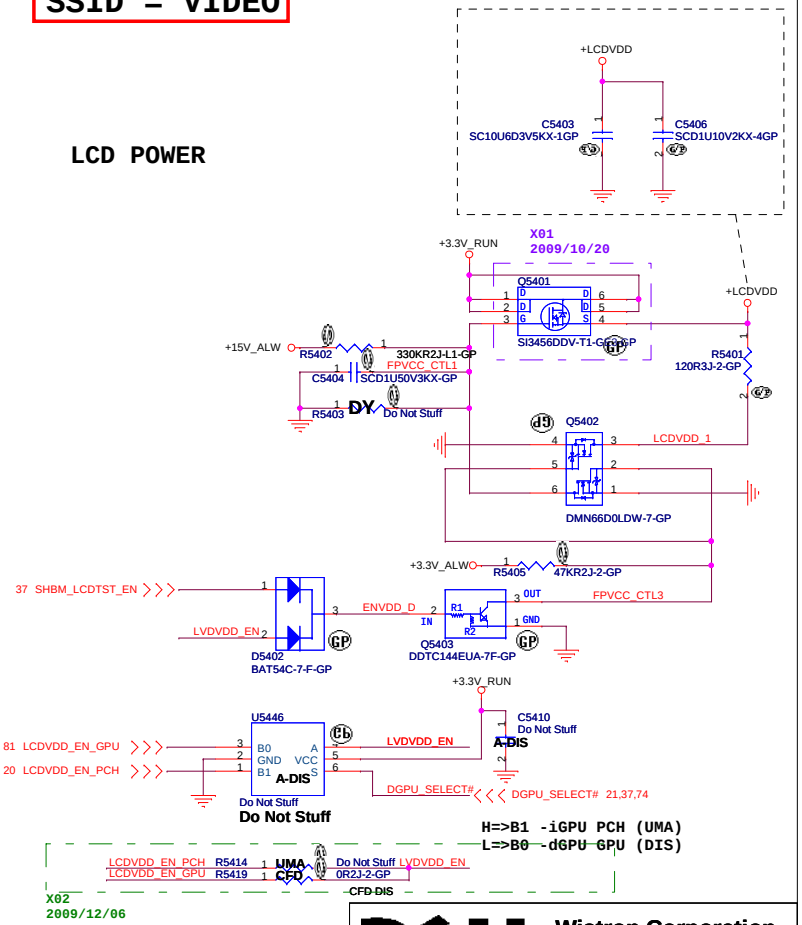
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



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Title: LCD/Inverter Connector

Size	Document Number	Rev
Custom	Vostro Calpella	-1

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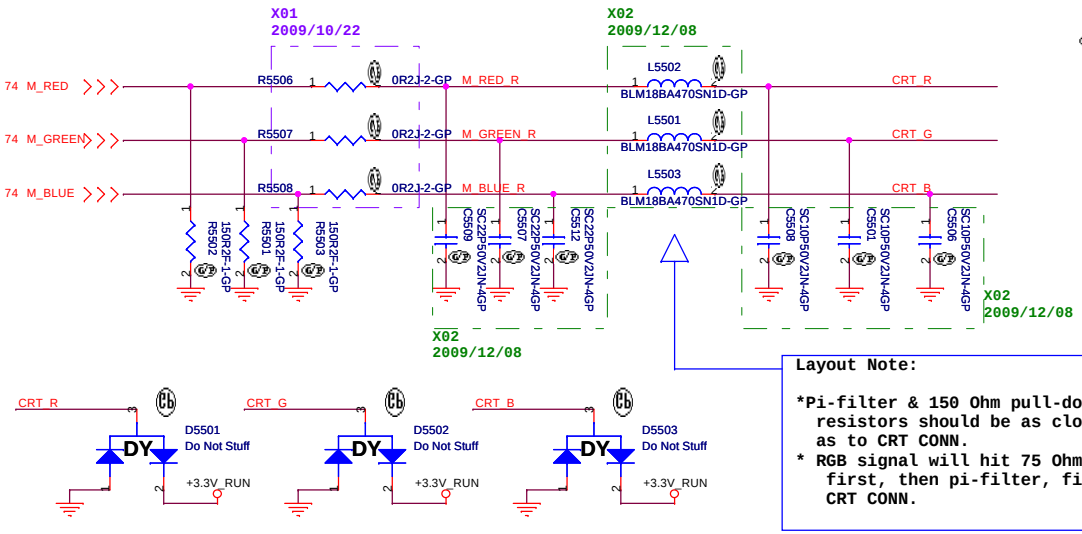
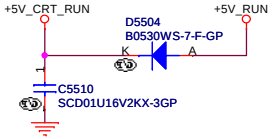
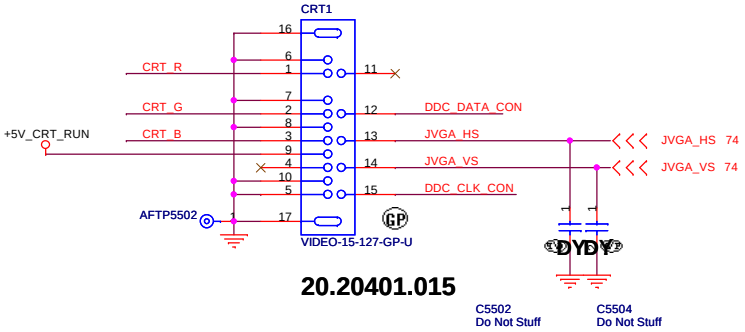
SSID = VIDEO

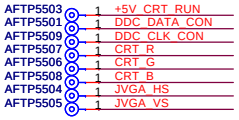


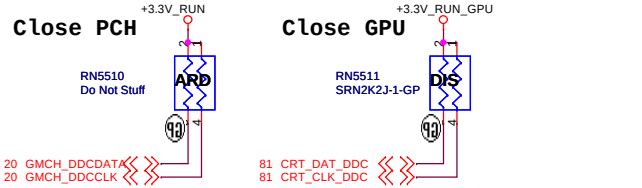




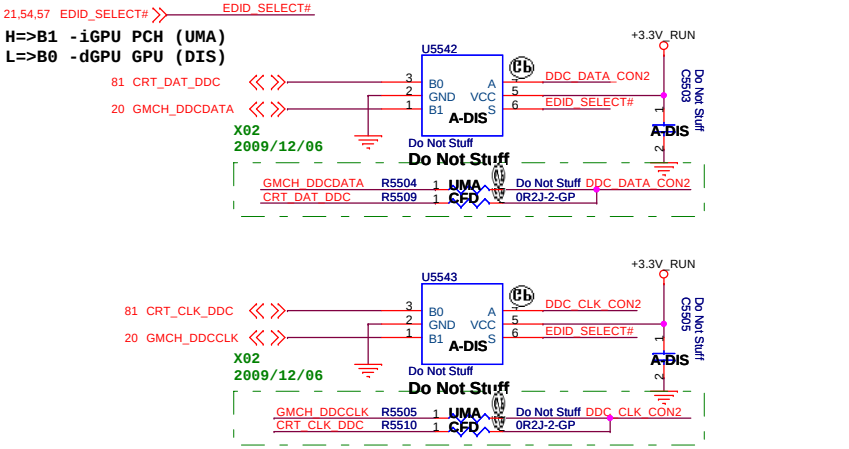
Layout Note:

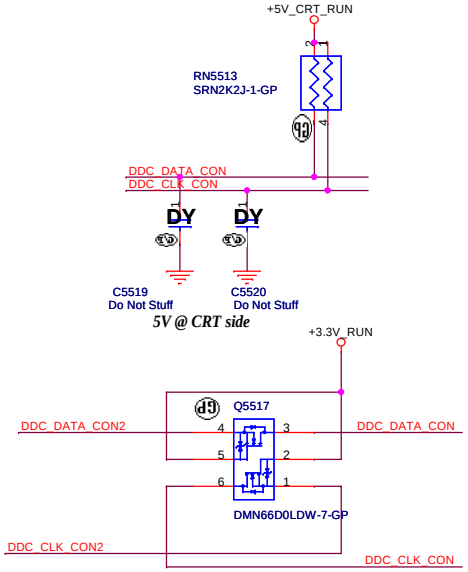
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.





UMA/DIS CRT DDC CLK/DAT select circuit





CFD DIS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **CRT Connector**		
Size: A3	Document Number: **Vostro Calpella**	Rev: **-1**
Date: Thursday, February 04, 2010	Sheet 55 of 95	

(Blank)

CFD DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title

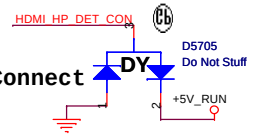
(Reserve)

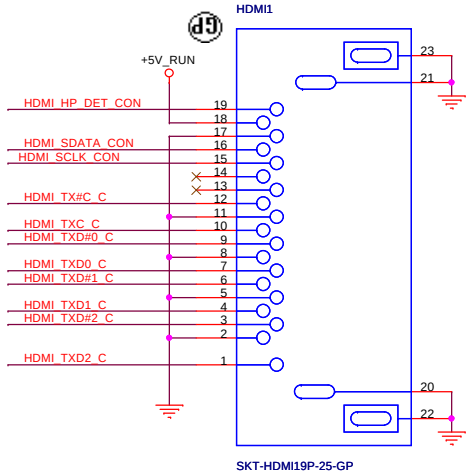
Size	Document Number	Rev
Custom	*Vostro Calpella*	*-1*

Date: Thursday, February 04, 2010 Sheet 56 of 95

X02
2009/12/02

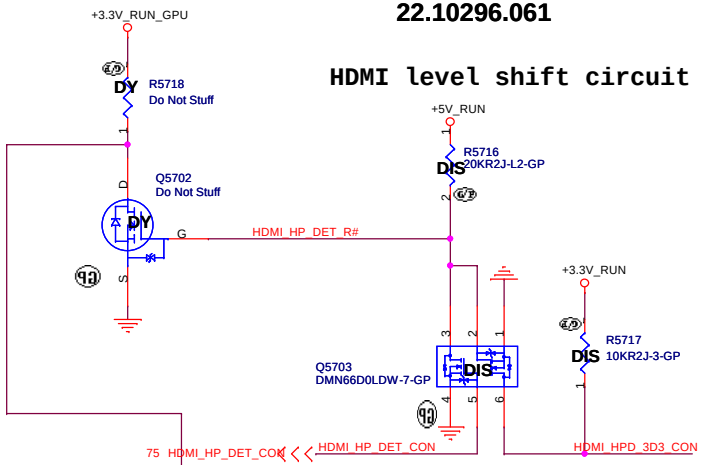
Close HDMI Connect



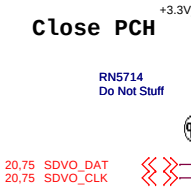


22.10296.061

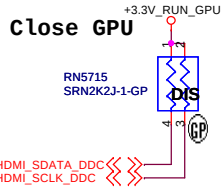
HDMI level shift circuit



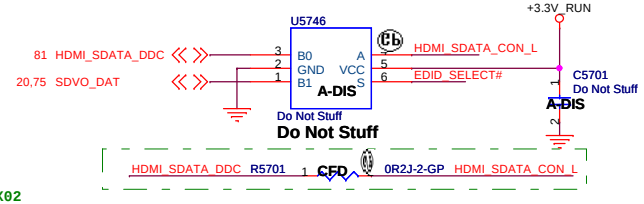
Close PCH



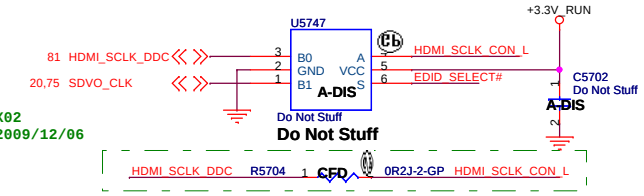
Close GPU



UMA/DIS HDMI DDC CLK/DAT select circuit



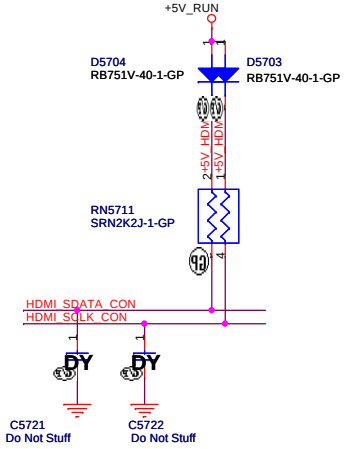
X02
2009/12/06



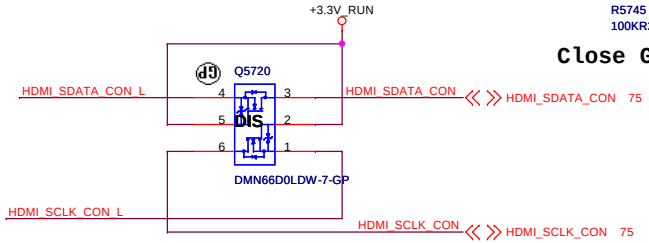
X02
2009/12/06

21,54,55 EDID_SELECT# EDID_SELECT#

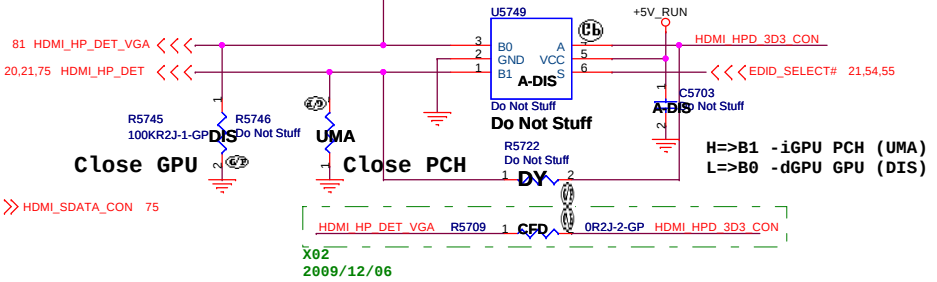
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)



5V @ HDMI side



UMA/DIS HDMI Detection select circuit



Close GPU

Close PCH

H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

X02
2009/12/06

CFD DIS

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Title: HDMI Connector		
Size: A3	Document Number: Vostro Calpella	Rev: -1
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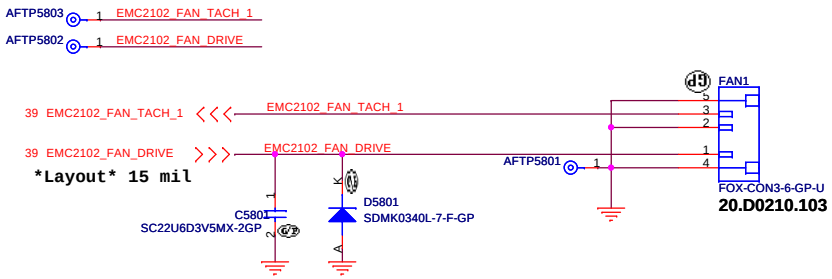
SSID = Thermal

Fan Connector



CFD DIS

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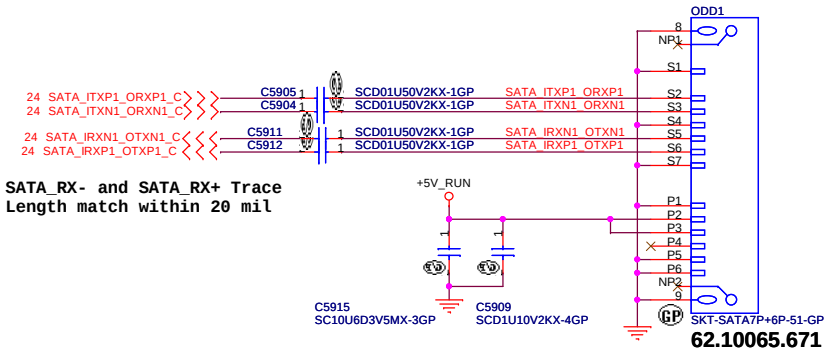
Taipei Hsien 221, Taiwan, R.O.C.

Title	***58_FAN***	
Size: A3	Document Number: ***Vostro Calpella***	Rev: ***-1***
Date: Thursday, February 04, 2010	Sheet 58 of 95	

SSID = SATA

ODD Connector



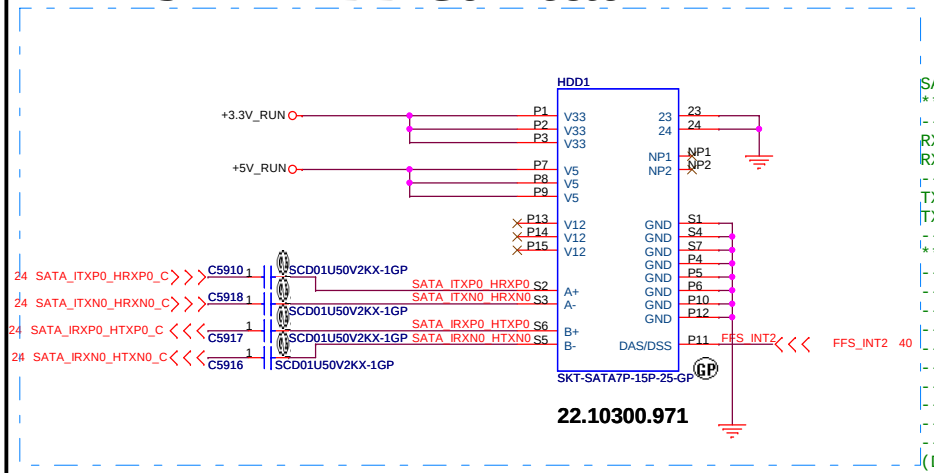
62.10065.671

SATA_RX- and SATA_RX+ Trace Length match within 20 mil

SSID = SATA

SATA HDD Connector

-1
2010/01/07

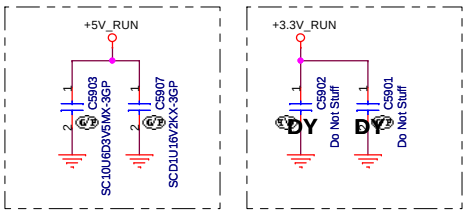


22.10300.971

```
SATA HDD Interface comment
*****************************
--- GND
RX+
RX-
--- GND
TX-
TX+
--- GND
*****************************
------------ 3.3V
------------ 3.3V
------------ 3.3V
--- GND
--- GND / Dell Detected Pin
--- GND
------------ 5V
------------ 5V
------------ 5V
--- GND
(Dell: FFS_INT for supported HDD)
--- GND
------------ 12V
------------ 12V
------------ 12V
*****************************
```

Close to CONN 5V power pin

Close to CONN 3.3V power pin



CFD DIS

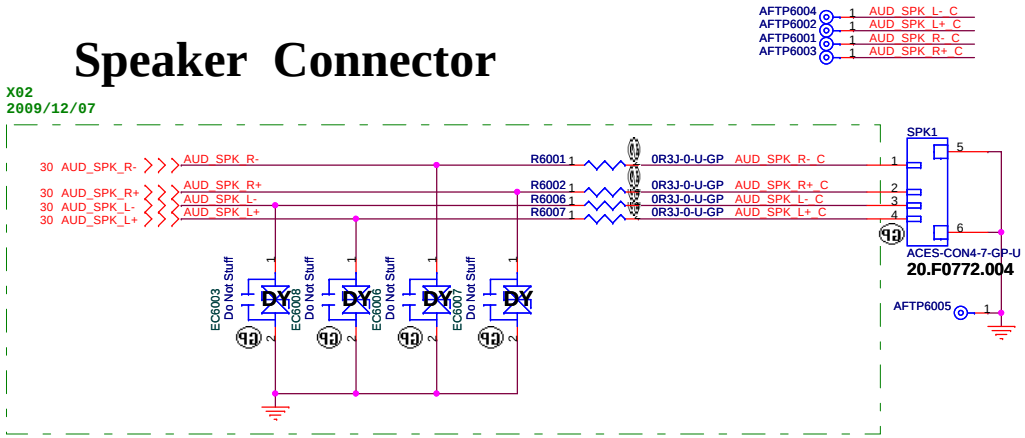
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD/ODD Connector		
Size: A3	Document Number: Vostro Calpella	Rev: -1
Date: Thursday, February 04, 2010	Sheet 59 of 95	

SSID = AUDIO

Speaker Connector

X02
2009/12/07



CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Speaker/HP/MIC Jack***	
Size: A3	Document Number: ***Vostro Calpella***	Rev: ***-1***
Date: Thursday, February 04, 2010	Sheet 60 of 95	

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CFD DIS

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

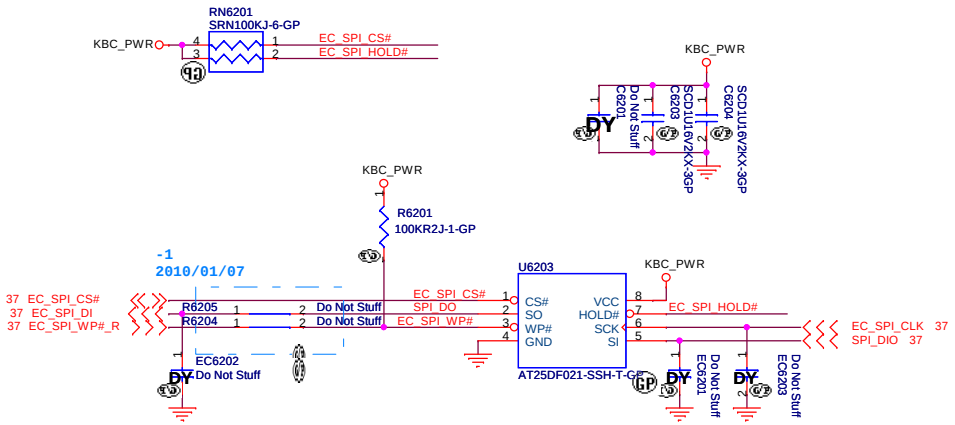
(Reserve)

Size	Document Number	Rev
A3	*Vostro Calpella*	*-1*

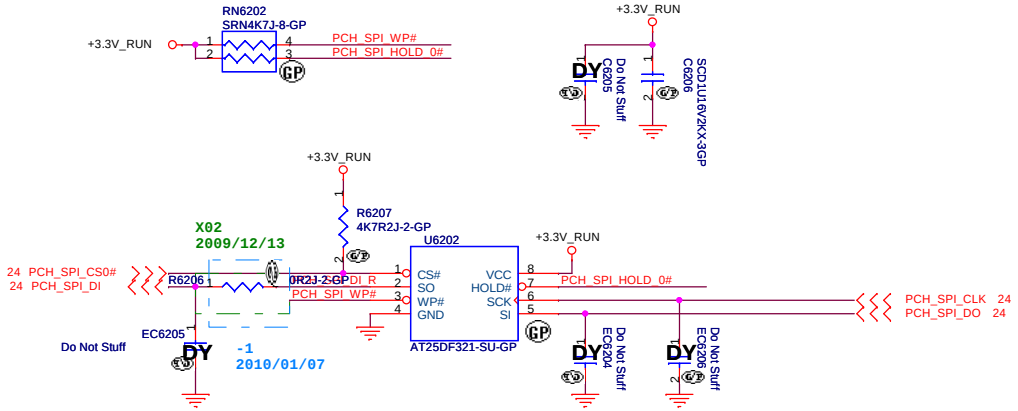
Date: Thursday, February 04, 2010 Sheet 61 of 95

SSID = Flash.ROM

SPI FLASH ROM (256K Bytes) for KBC

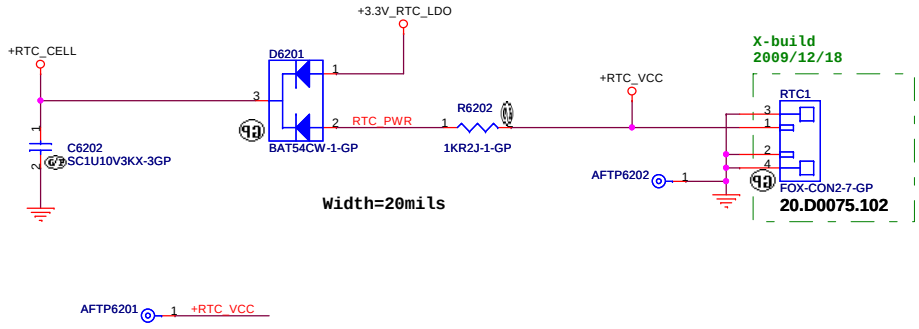


SPI FLASH ROM (4M Bytes) for PCH



SSID = RBATT

RTC Connector



CFD DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

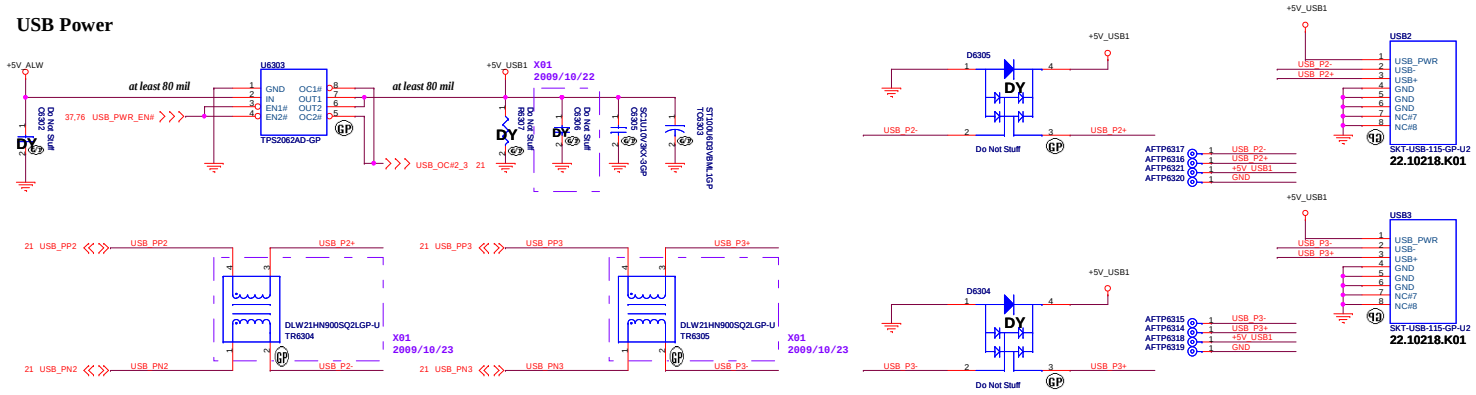
Title: EEPROM/RTC Connector

Size	Document Number	Rev
A3	Vostro Calpella	-1

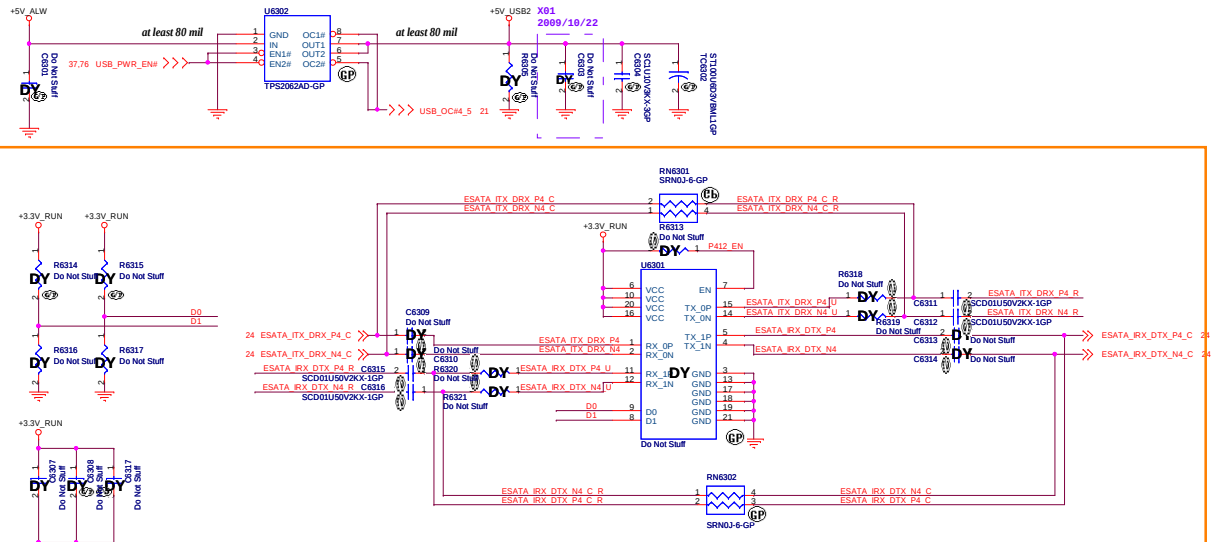
Date: Thursday, February 04, 2010 Sheet 62 of 95

SSID = USB

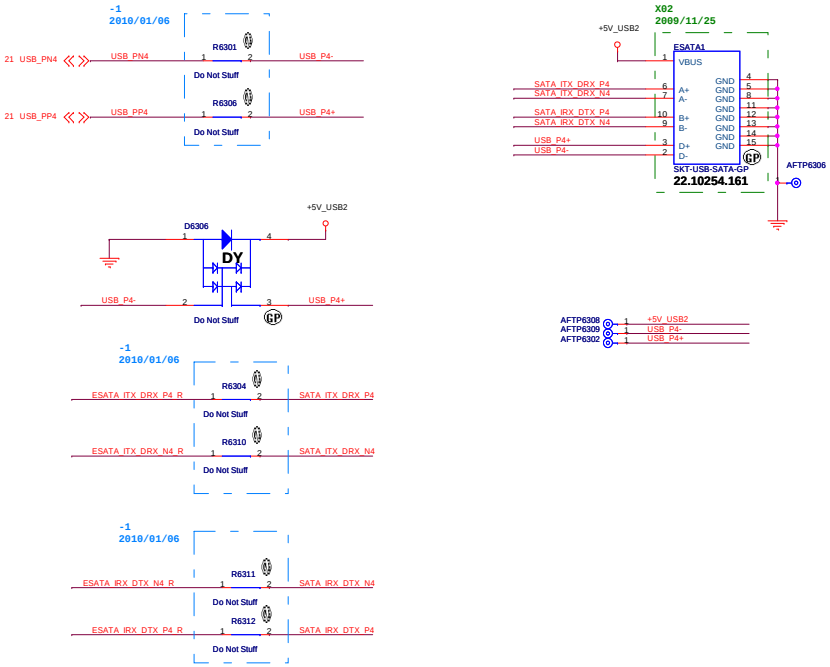
USB Power



ESATA Power



	If you added U6301(SN75LVCP412RTJR-GP). You need to BOM change
ASM	R6313, R6314, R6315, R6318, R6319, R6320, R6321 C6309, C6310, C6313, C6314, C6307, C6308, C6317
DY	RN6301, RN6302



CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

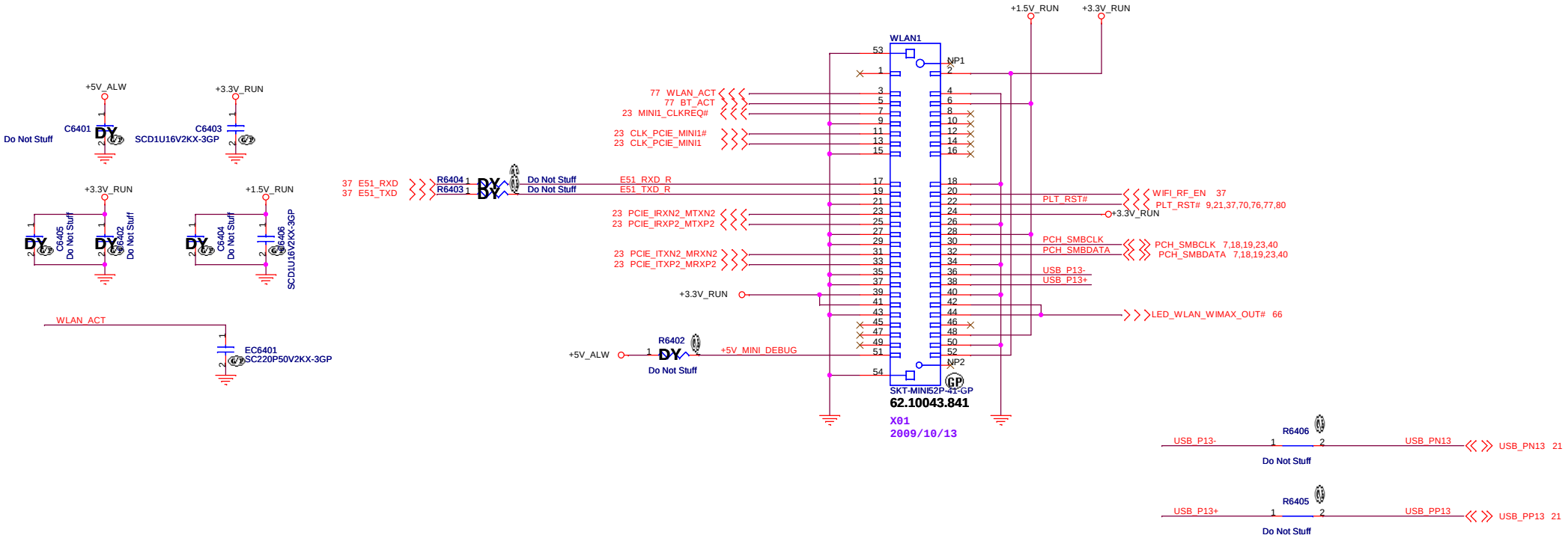
Title: *USB /ESATA Port*

Size	Document Number	Rev
A2	*Vostro Calpella*	-1

Date: Thursday, February 04, 2010 Sheet 63 of 95

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINICARD(WLAN)/ITP CONN***

Size	Document Number	Rev
A3	*Vostro Calpella*	*-1*

Date: Thursday, February 04, 2010 Sheet 64 of 95

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CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *WWAN Connector*

Size: A3 | Document Number: *Vostro Calpella* | Rev: *-1*

Date: Thursday, February 04, 2010 | Sheet 65 of 95

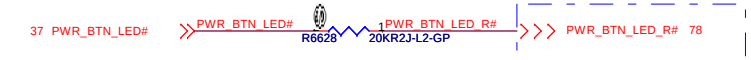
For LED & Capacity board:

LED Type	Color	Power rail
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN WIMAX LED	White	RUN

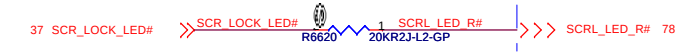
For IO board:

LED Type	Color	Power rail
PWR LED2	White(Multi-color)	ALW
BATTERY LED2	Amber(Multi-color)	ALW
	White(Multi-color)	ALW

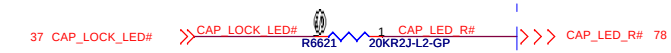
PWR BTN LED



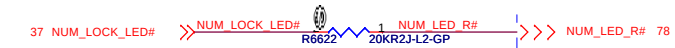
SCRLK LED



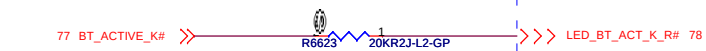
CAPS LED



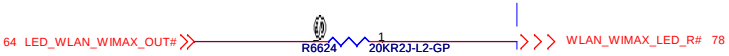
NUM LED



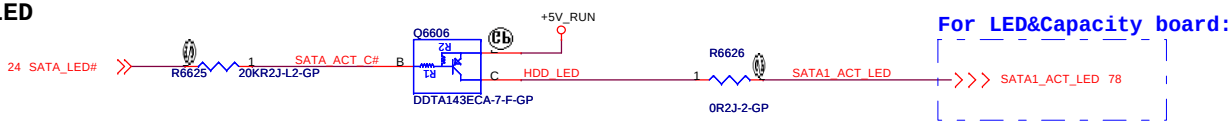
Bluetooth LED



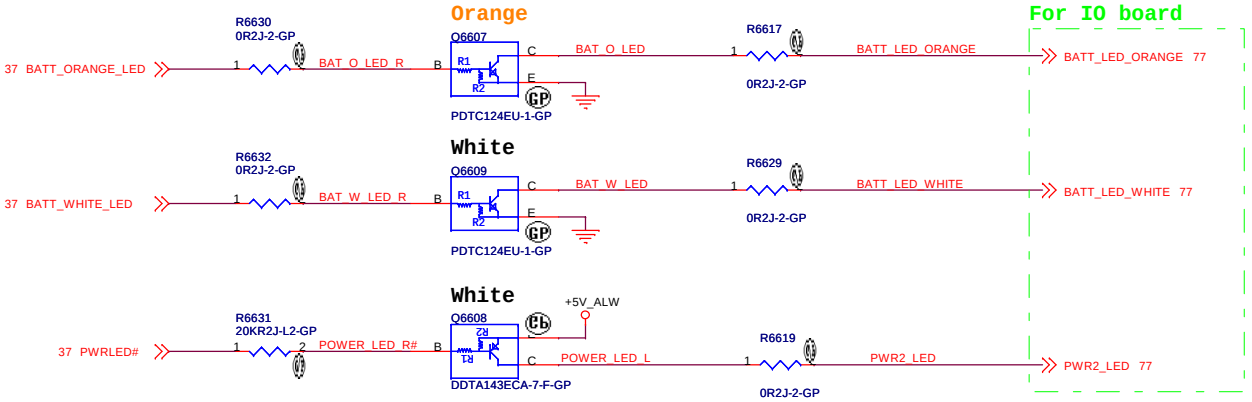
WLAN LED



HD LED



Power & Battery LED



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LED*

Size	Document Number	Rev
A3	*Vostro Calpella*	*-1*

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CFD DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title

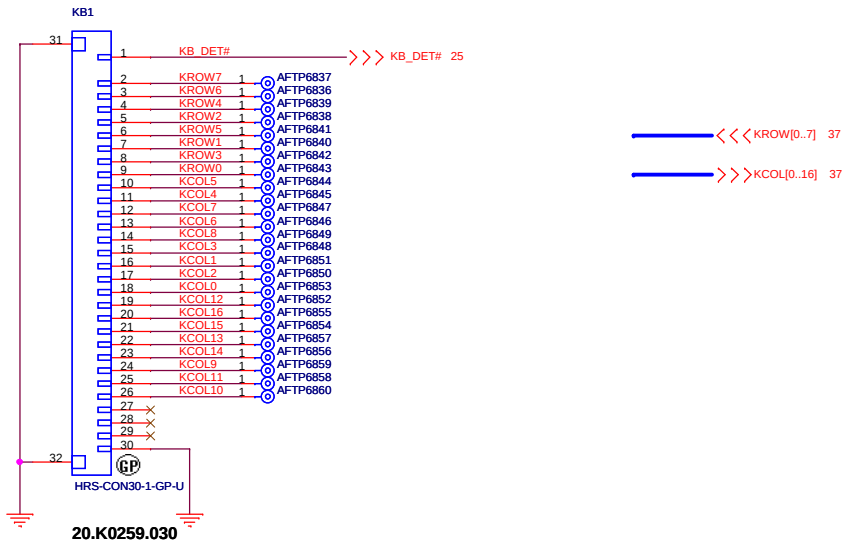
(Reserve)

Size	Document Number	Rev
A2	*Vostro Calpella*	*-1*

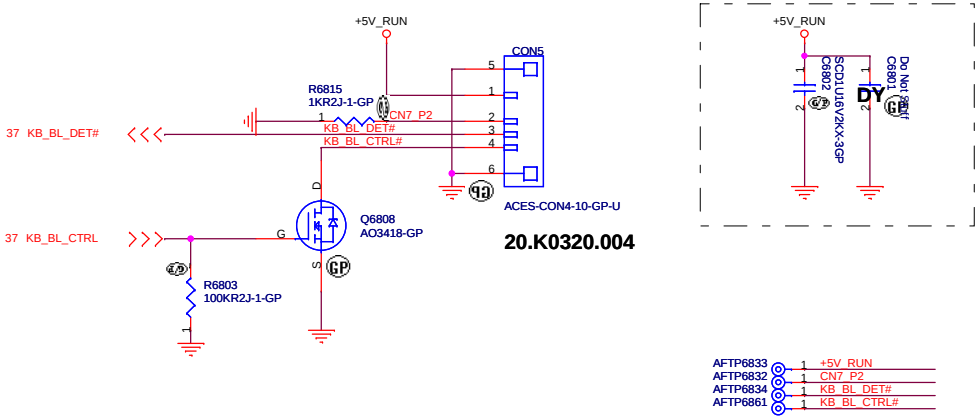
Date: Thursday, February 04, 2010 Sheet 67 of 95

SSID = KBC

Internal KeyBoard Connector

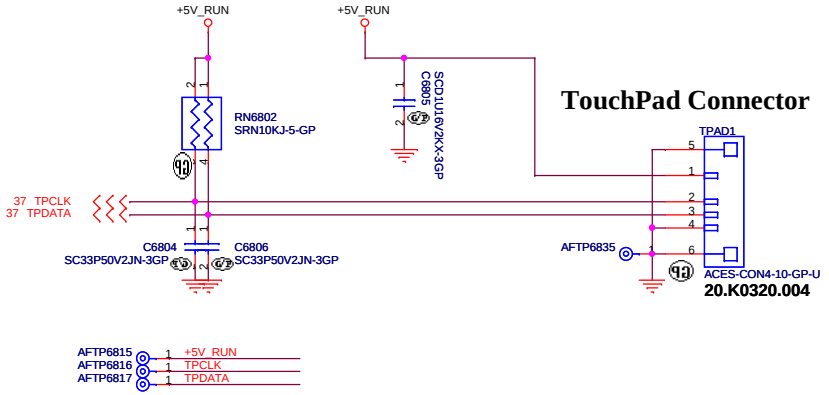


KB Backlight CONN



SSID = Touch.Pad

TouchPad Connector



CFD DIS

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Keyboard/Touch Pad

Size: Custom | Document Number: Vostro Calpella | Rev: -1

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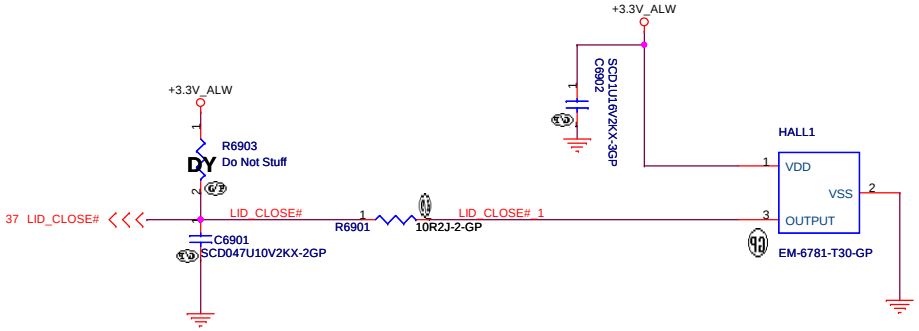
Hall Sensor Connector

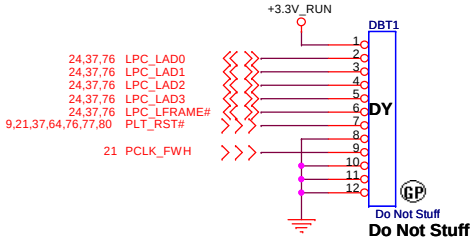


CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Hall sensor*		
Size: A3	Document Number: *Vostro Calpella*	Rev: *-1*
Date: Thursday, February 04, 2010	Sheet 69 of 95	

GOLDEN FINGER FOR DEBUG BOARD



Do Not Stuff

X01
2009/10/20
Change DBT1 to 20.F0866.010/

CFD DIS

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Title	***Debug port***	
Size: A3	Document Number: ***Vostro Calpella***	Rev: ***-1***
Date: Thursday, February 04, 2010	Sheet 70 of 95	

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CFD DIS

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Title: *PX Swith-2*

Size: A3 | Document Number: *Vostro Calpella* | Rev: *-1*

Date: Thursday, February 04, 2010 | Sheet 71 of 95

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CFD DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title

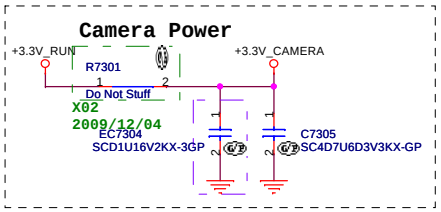
Braidwood

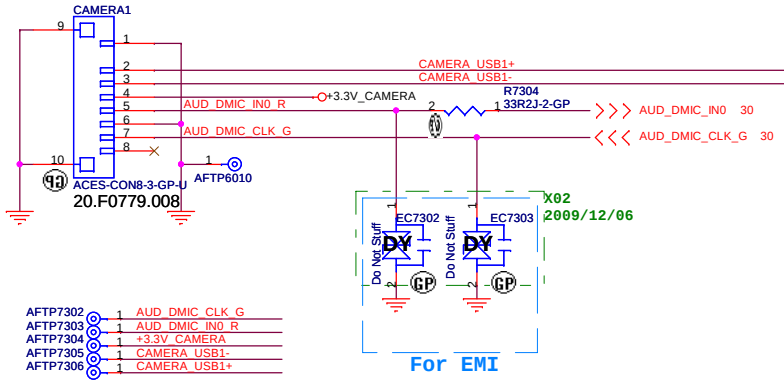
Size	Document Number	Rev
A3	***Vostro Calpella***	*-1*

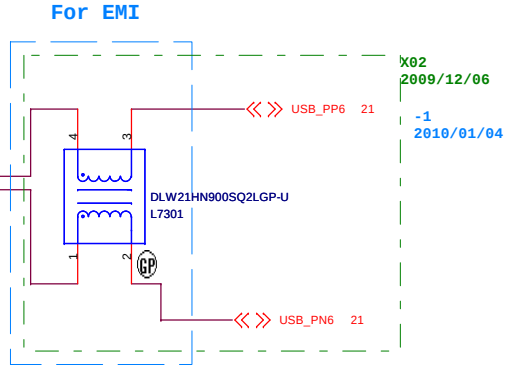
Date: Thursday, February 04, 2010 Sheet 72 of 95

SSID = User.Interface

Camera Connector







CFD DIS

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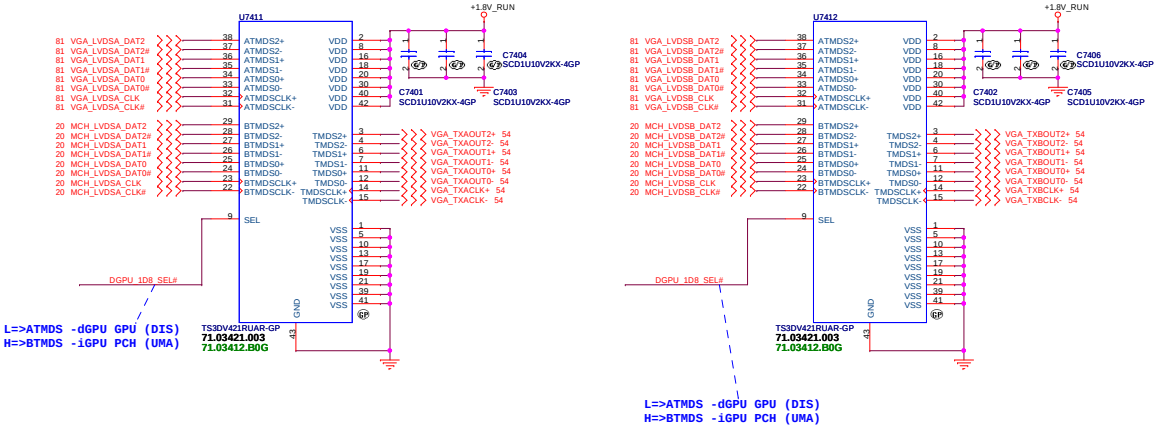
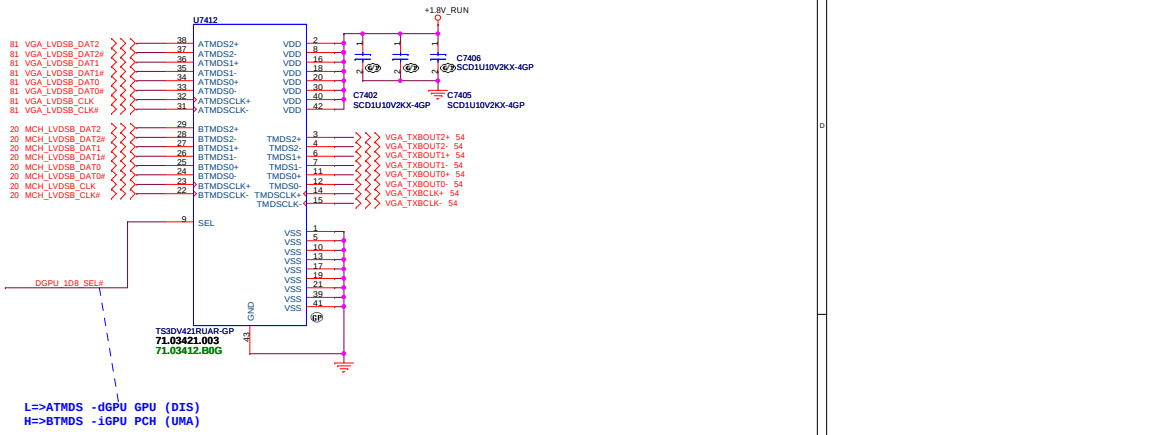
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Camera Connector*		
Size: A3	Document Number: *Vostro Calpella*	Rev: *-1*
Date: Thursday, February 04, 2010	Sheet 73 of 95	

UMA/DIS LVDS signal select circuit





FUNCTION TABLE

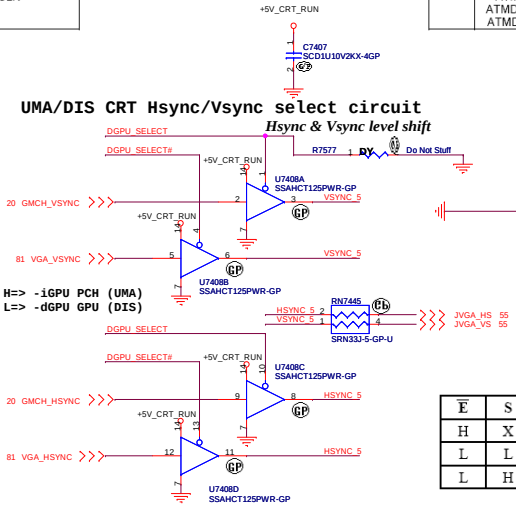
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

FUNCTION TABLE

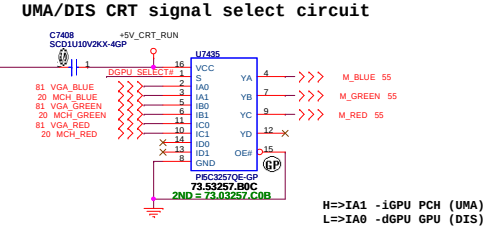
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

UMA/DIS CRT Hsync/Vsync select circuit

Hsync & Vsync level shift

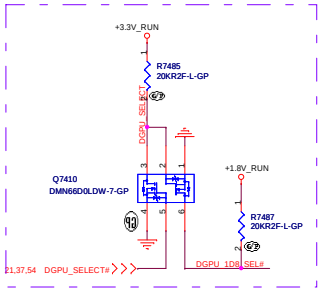


UMA/DIS CRT signal select circuit



$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

X01
2009/10/20



CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *PX Swith-1*

Size: Custom | Document Number: *Vostro Calpella* | Rev: -1

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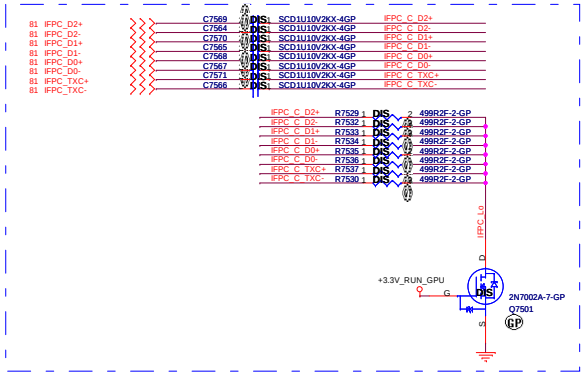
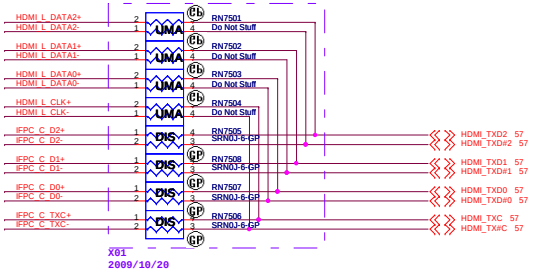
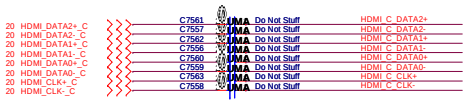
Close to connector



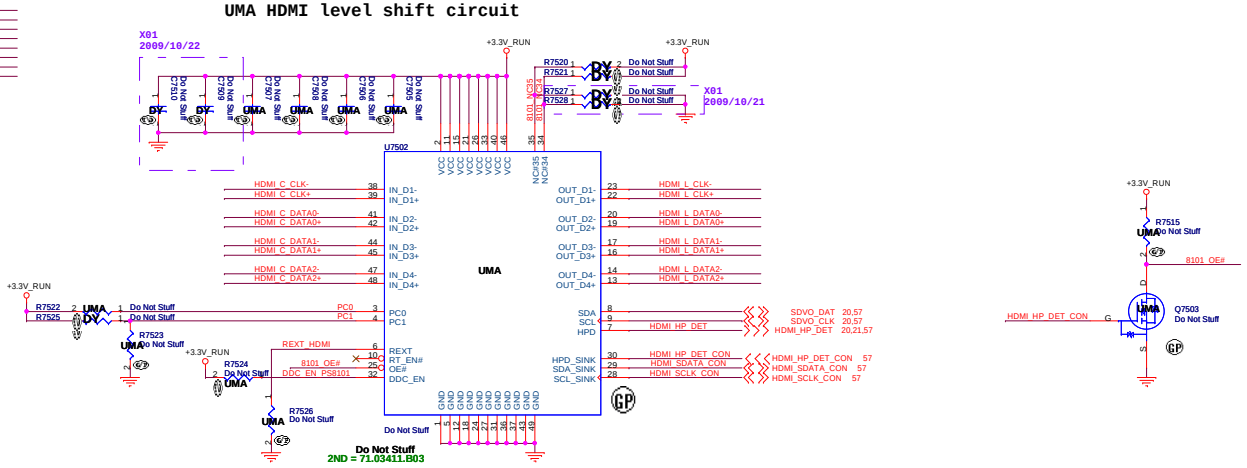
UMA/DIS HDMI signal select circuit



Close to PCH



UMA HDMI level shift circuit



CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserve)*

Size: A2 | Document Number: *Vostro Calpella* | Rev: -1

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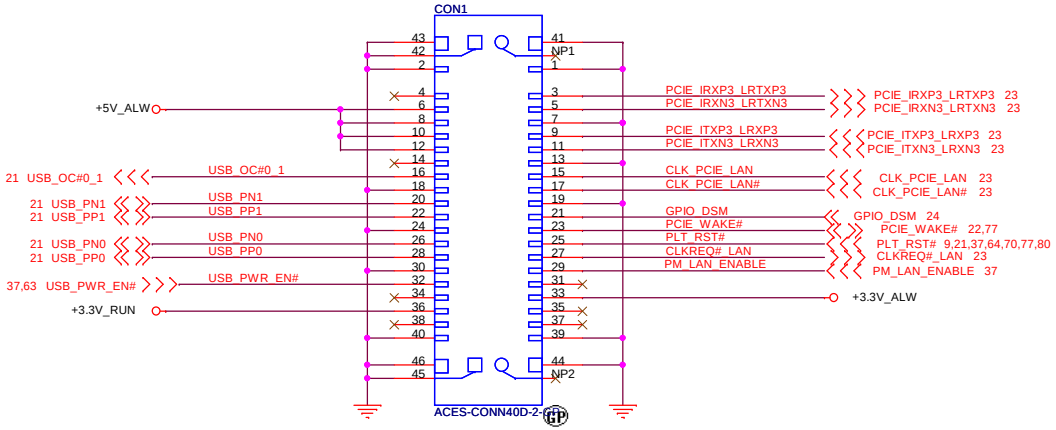
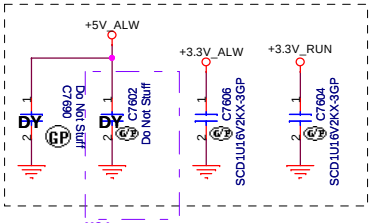
LAN baord CON

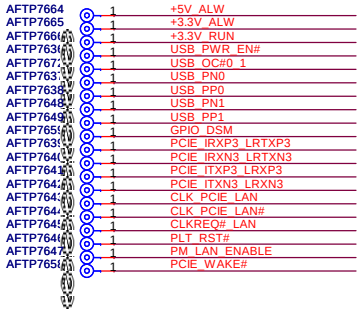


20.F1009.040

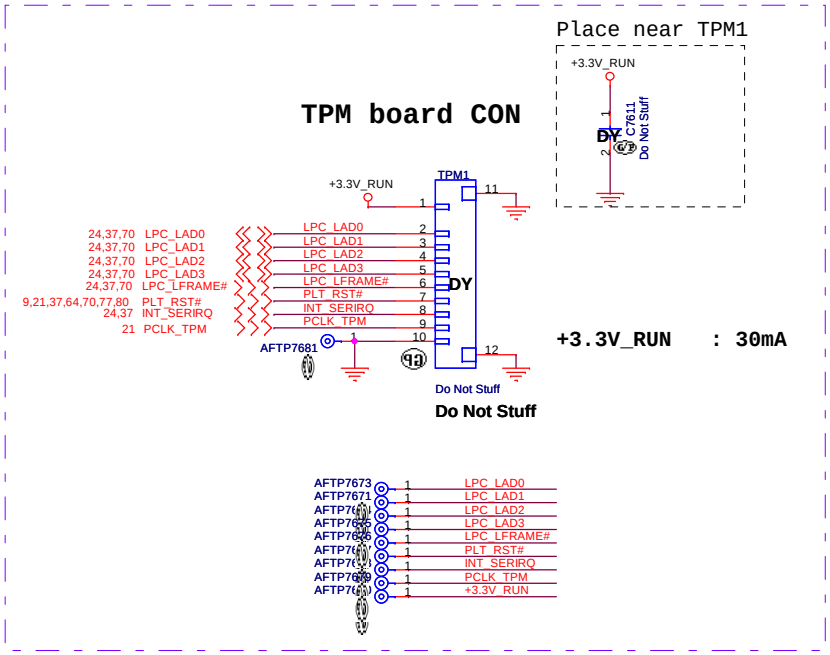
Place near CON1



X01
2009/10/22



TPM board CON



X01
2009/10/15
Add TPM function.

CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN Board Connector	
Size: A3	Document Number: Vostro Calpella	Rev: -1
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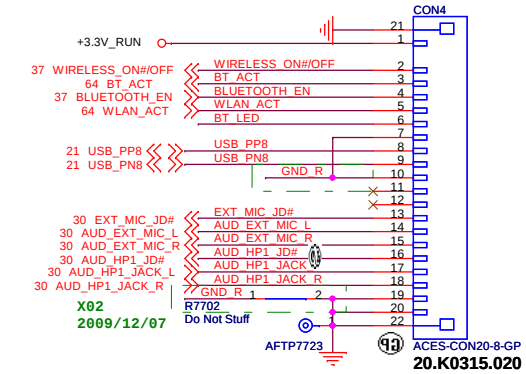
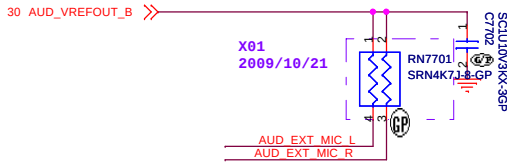
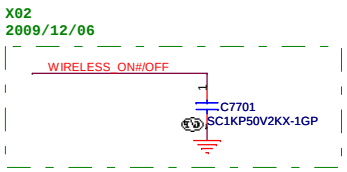
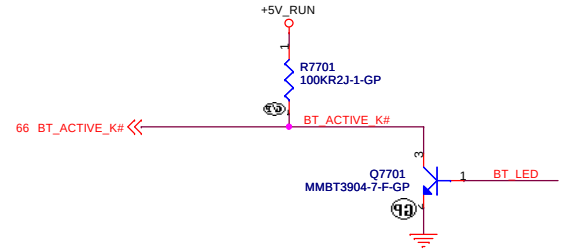
SSID = User.Interface

Audio board CON

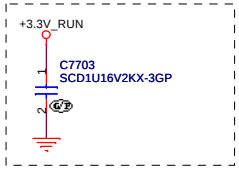




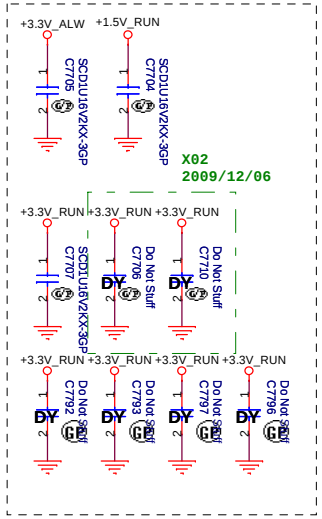




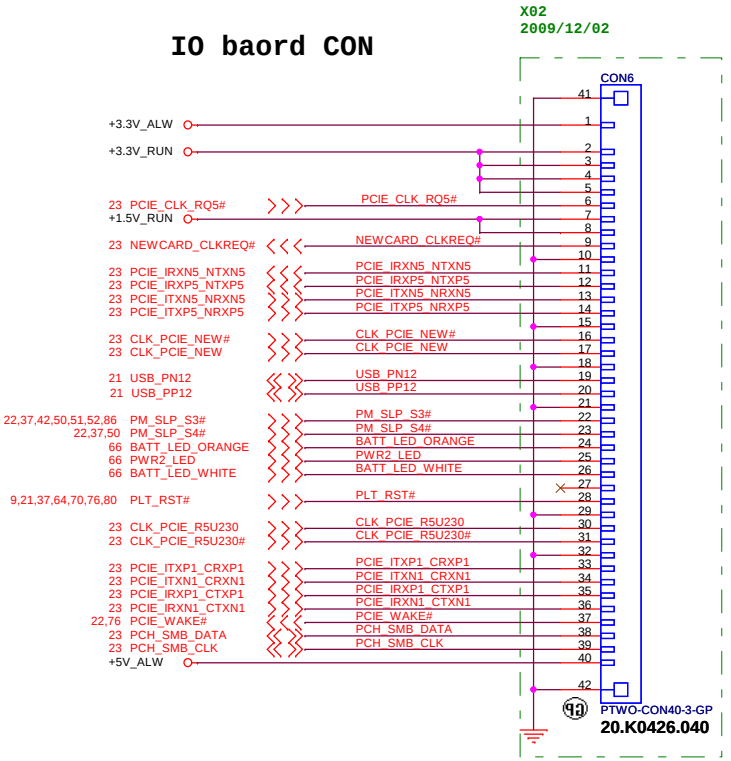
Place near CON4



Place near CON6



IO baord CON



AFTP7706 1 +3.3V_RUN
AFTP7709 1 WIRELESS_ON#/OFF

AFTP7702 1 WLAN_ACT
AFTP7703 1 BLUETOOTH_EN
AFTP7704 1 BT_LED
AFTP7705 1 BT_ACT
AFTP7707 1 USB_PP8
AFTP7708 1 USB_PN8

AFTP7713 1 EXT_MIC_JD#
AFTP7714 1 AUD_EXT_MIC_L
AFTP7715 1 AUD_EXT_MIC_R
AFTP7716 1 AUD_HP1_JD#
AFTP7717 1 AUD_VREFOUT_B
AFTP7718 1 AUD_HP1_JACK_L
AFTP7719 1 AUD_HP1_JACK_R

AFTP7786 1 PCIE_CLK_RQ5#
AFTP7758 1 +3.3V_ALW
AFTP7757 1 +3.3V_RUN
AFTP7760 1 +1.5V_RUN
AFTP7762 1 USB_PN12
AFTP7759 1 USB_PP12
AFTP7761 1 PCIE_IRXN5_NTXN5
AFTP7765 1 PCIE_IRXP5_NTXP5
AFTP7764 1 PCIE_ITXN5_NRXN5
AFTP7763 1 PCIE_ITXP5_NRXP5
AFTP7771 1 CLK_PCIE_NEW#
AFTP7770 1 CLK_PCIE_NEW
AFTP7766 1 PCIE_WAKE#
AFTP7769 1 NEWCARD_CLKREQ#
AFTP7768 1 PCH_SMB_CLK
AFTP7767 1 PCH_SMB_DATA
AFTP7777 1 PM_SLP_S3#
AFTP7776 1 PM_SLP_S4#
AFTP7774 1 BATT_LED_WHITE
AFTP7773 1 BATT_LED_ORANGE
AFTP7772 1 PWR2_LED
AFTP7775 1 CLK_PCIE_R5U230
AFTP7780 1 CLK_PCIE_R5U230#
AFTP7779 1 PCIE_ITXP1_CRXP1
AFTP7778 1 PCIE_ITXN1_CRXN1
AFTP7783 1 PCIE_IRXP1_CTXP1
AFTP7782 1 PCIE_IRXN1_CTXN1
AFTP7781 1 PLT_RST#

CFD DIS

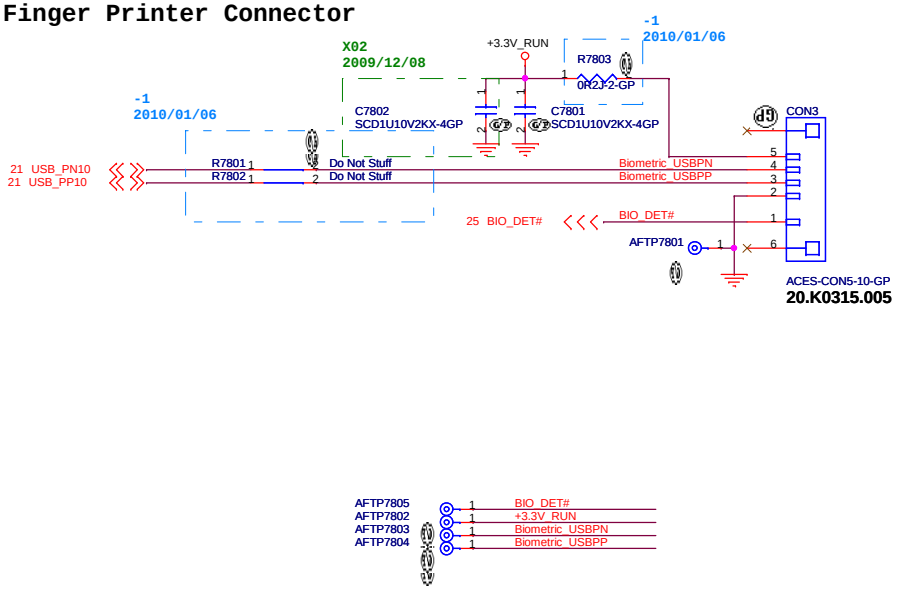
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board/Audio Board Connector

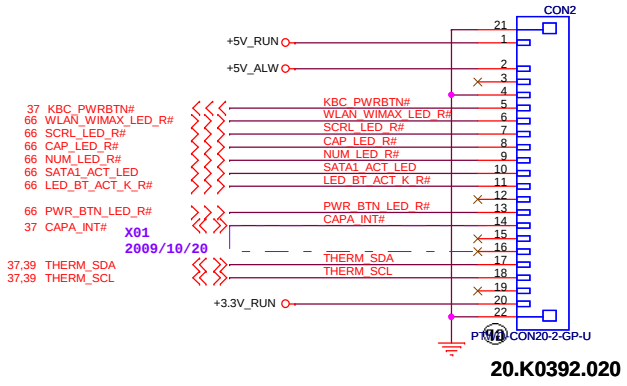
Size	Document Number	Rev
A3	Vostro Calpella	-1

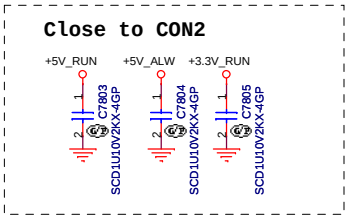
Date: Thursday, February 04, 2010 Sheet 77 of 95

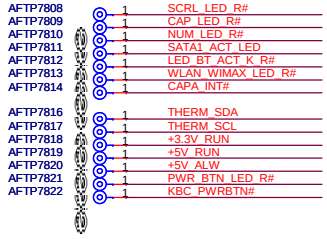
Finger Printer Connector



LED&Capacity board CONN







CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Finger Printer***

Size: Custom | Document Number: ***Vostro Calpella*** | Rev: ***-1***

Date: Thursday, February 04, 2010 | Sheet 78 of 95

SSID = Mechanical

BOSS:

WLAN

BOSS2
STF256R89H178-GP
34.4B417.001

Thermal

BOSS3
STF237R117H83-3-GP
34.4CK01.201

Thermal

BOSS5
STF237R117H83-3-GP
34.4CK01.201

X02
2009/12/06

For CPU HOLE:

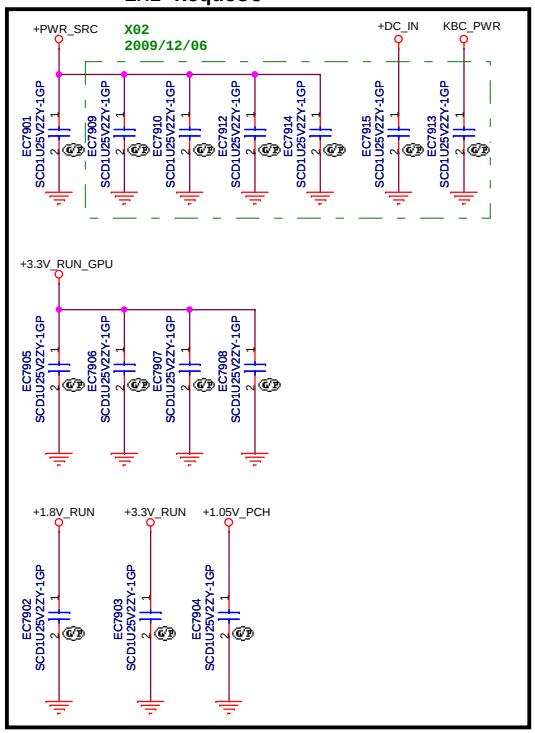
H13 Do Not Stuff — Do Not Stuff
H14 Do Not Stuff — Do Not Stuff
H15 Do Not Stuff — Do Not Stuff

H16 Do Not Stuff — Do Not Stuff

HOLE:

H1 Do Not Stuff — Do Not Stuff
H2 Do Not Stuff — Do Not Stuff
H3 Do Not Stuff — Do Not Stuff
H4 Do Not Stuff — Do Not Stuff
H17 Do Not Stuff — Do Not Stuff
H5 Do Not Stuff — Do Not Stuff
H6 Do Not Stuff — Do Not Stuff
H8 Do Not Stuff — Do Not Stuff
H10 Do Not Stuff — Do Not Stuff
H12 Do Not Stuff — Do Not Stuff

EMI Request



CFD DIS

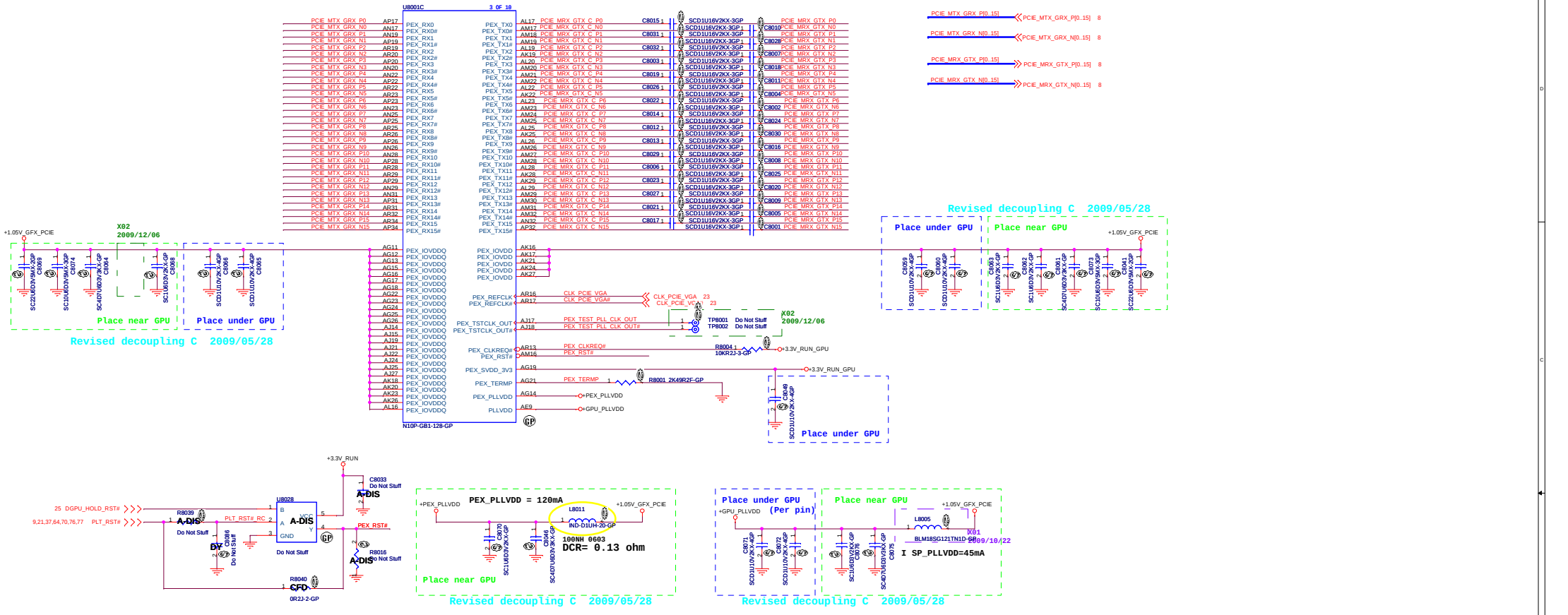
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Miscellaneous Components

Size: Custom | Document Number: Vostro Calpella | Rev: -1

Date: Thursday, February 04, 2010 | Sheet 79 of 95

SSID = VIDEO



CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *VGA-PCIE/LVDS(1/4)*

Size	Document Number	Rev
A2	*Vostro Calpella*	-1

Date: Thursday, February 04, 2010 Sheet 80 of 95

SSID = VIDEO

X02
2009/11/25

X01
2009/10/13

U8001F
6 OF 10
N10P-GB1-128-GP

+DACA_VDD = 120mA

Place near GPU
Place under GPU
16mil
Spec 300 ohm,
ESR<0.25 ohm

Revised decoupling C 2009/05/28

Added CLK GEN 27M select circuit 2009/06/15
Added R8132 (DY) 2009/06/17

CLK GEN 27M select:

VGA 27M	R8123	R8131	R8125	R8132
SS	DY	POP	DY	POP
NON-SS	POP	DY	POP	DY

Main 82.30034.651

X02
2009/12/13

Place near GPU
Place under GPU
I SP_PLLVDD=45mA

Revised decoupling C 2009/05/28

U8001E
5 OF 10
N10P-GB1-128-GP

+IFPAB_IOVDD

Place near GPU
Place under GPU near IFPA_IOVDD
Place under GPU near IFPB_IOVDD

IFPAB_IOVDD = 220mA

Revised decoupling C 2009/05/28

+IFPC_IOVDD

IFPAB_IOVDD = 285mA

Place near GPU
Place under GPU

Revised decoupling C 2009/05/28

Unused IFP Interfaces setting 2009/06/03

+IFPAB_PLLVDD

Revised decoupling C 2009/05/28

IFPAB_PLLVDD = 220mA

Place near GPU

+IFPC_PLLVDD

IFPAB_PLLVDD = 220mA

Spec 300 ohm,
ESR<0.25 ohm

Place near GPU
Place under GPU

Revised decoupling C 2009/05/28

CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-LVDS/CRT/DP PORT

Size: A2 | Document Number: Vostro Calpella | Rev: -1

Date: Thursday, February 04, 2010 | Sheet 81 of 95

SSID = VIDEO

+VCC_GFX_CORE = 31.66A

FBVDD/Q = 2.24A

Revised decoupling C 2009/05/28

Revised decoupling C 2009/05/28

X02
2009/12/02

Layout notice:
VDD_SENSE need check layout SPEC.

CFD DIS

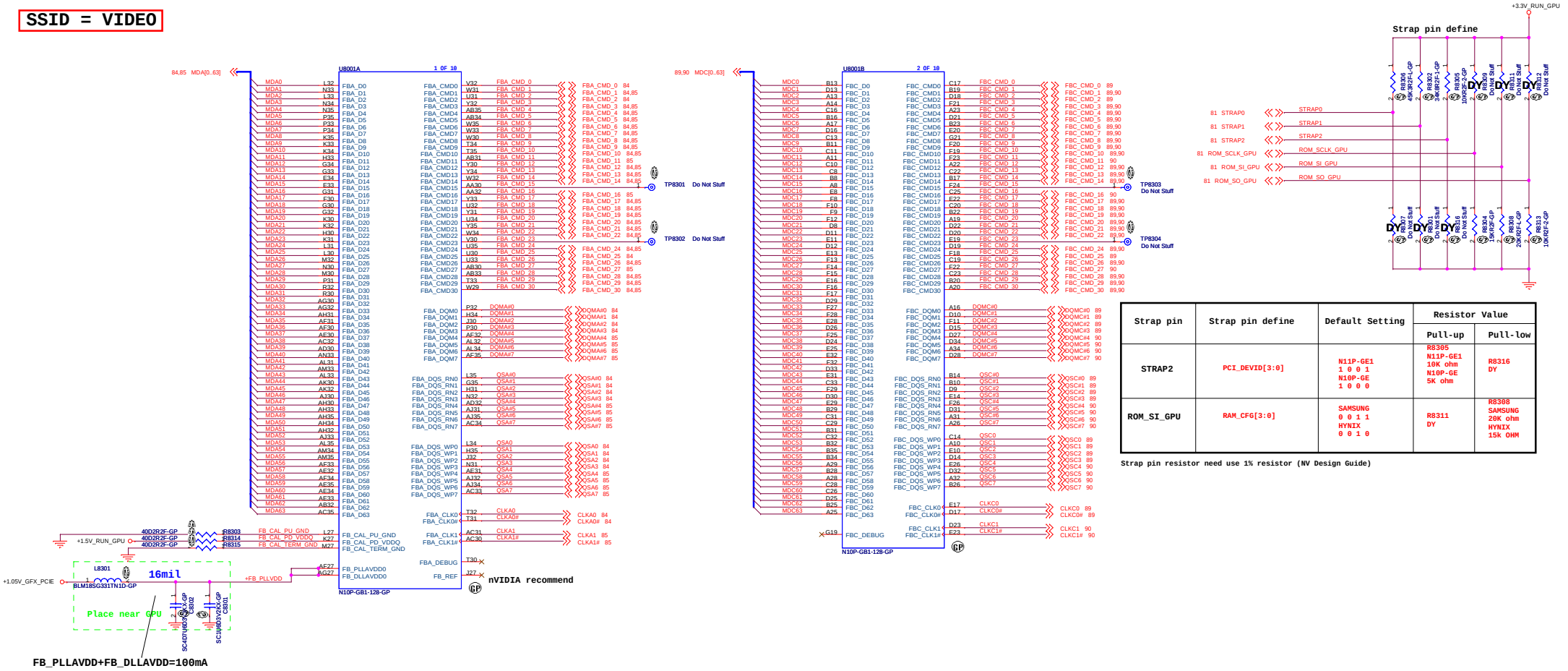
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-POWER/GND(3/4)

Size: A2 | Document Number: Vostro Calpella | Rev: -1

Date: Thursday, February 04, 2010 | Sheet 82 of 95

SSID = VIDEO



Strap pin	Strap pin define	Default Setting	Resistor Value	
			Pull-up	Pull-low
STRAP2	PCI_DEVID[3:0]	N11P-GE1 1 0 0 1 N10P-GE 1 0 0 0	R8305 N11P-GE1 10K ohm N10P-GE 5K ohm	R8316 DY
ROM_SI_GPU	RAM_CFG[3:0]	SAMSUNG 0 0 1 1 HYNIX 0 0 1 0	R8311 DY	R8308 SAMSUNG 20K ohm HYNIX 15K OHM

Strap pin resistor need use 1% resistor (NV Design Guide)

CFD DIS

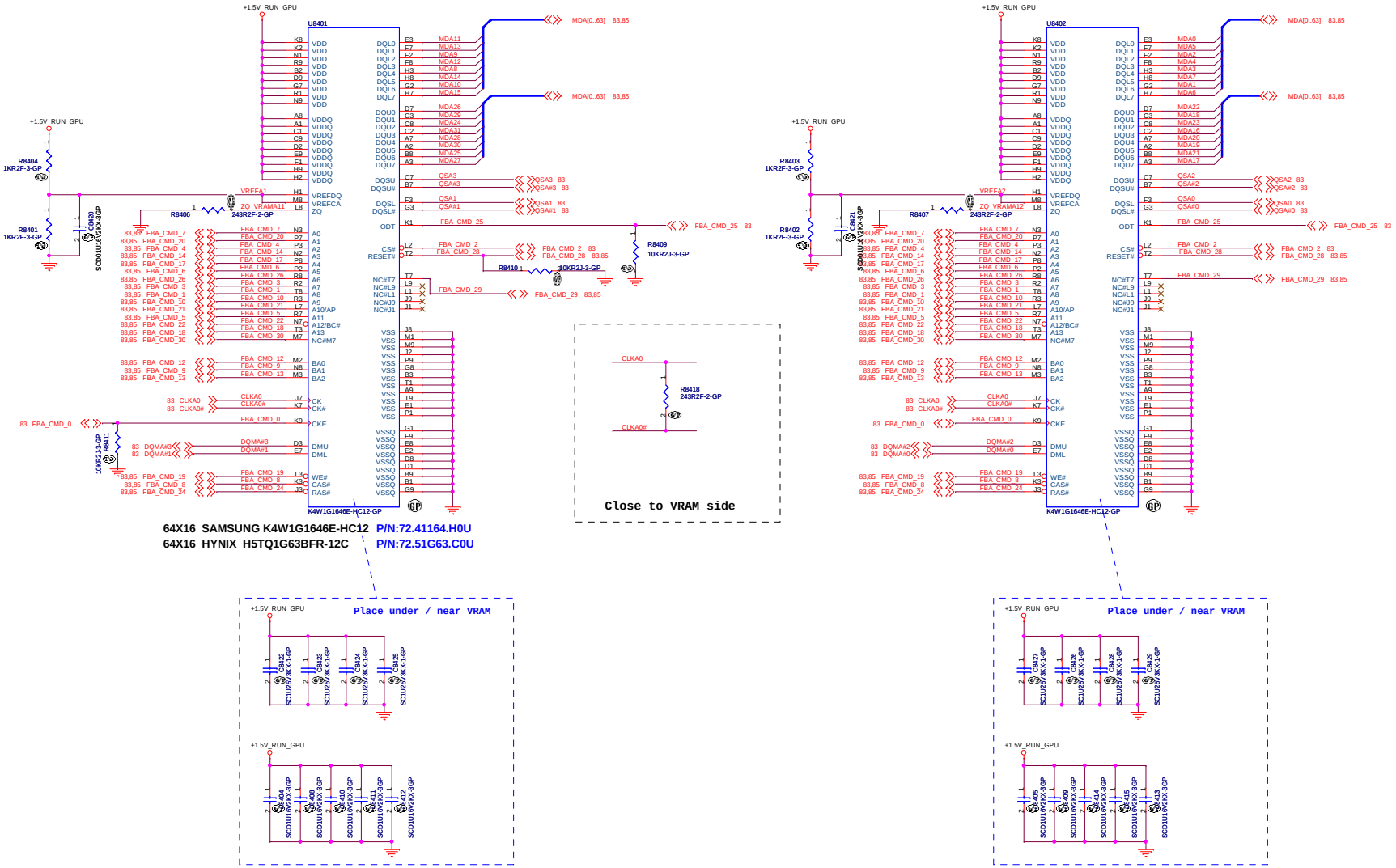
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-MEMORY(5/5)

Size	Document Number	Rev
A2	Vostro Calpella	-1

Date: Thursday, February 04, 2010 Sheet 83 of 95

SSID = VIDEO



CFD DIS

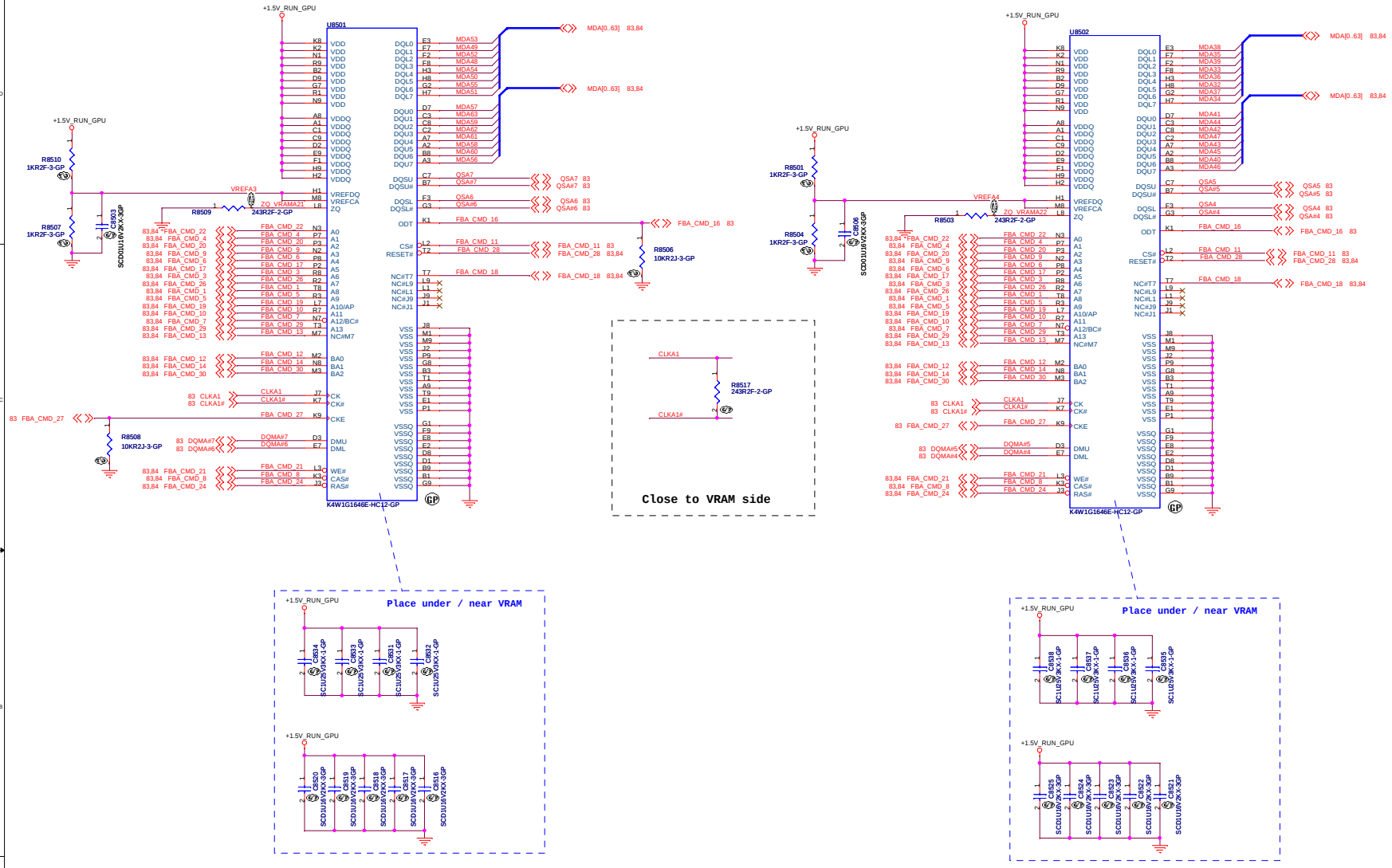
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM(1/2)**

Size	Document Number	Rev
A2	*Vostro Calpella*	-1

Date: Thursday, February 04, 2010 Sheet 84 of 95

SSID = VIDEO

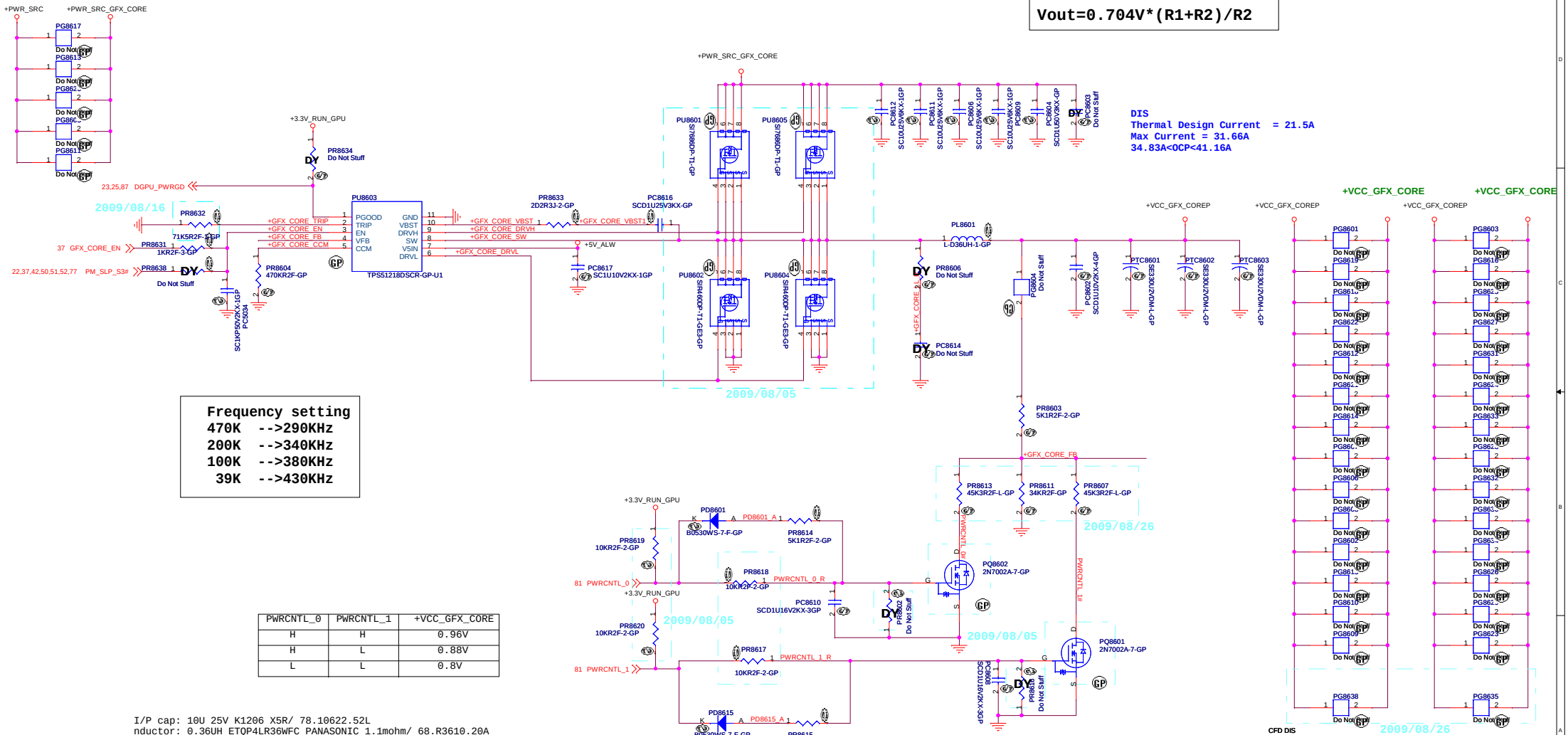


CFD DIS

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM		
Size: A2	Document Number: Vostro Calpella	Rev: -1
Date: Thursday, February 04, 2010	Sheet 85 of 95	

SSID = PWR.Plane.Regulator_GFX

Vout=0.704V*(R1+R2)/R2



DIS
Thermal Design Current = 21.5A
Max Current = 31.66A
34.83A<OCP<41.16A

Frequency setting
470K --> 290KHz
200K --> 340KHz
100K --> 380KHz
39K --> 430KHz

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	0.96V
H	L	0.88V
L	L	0.8V

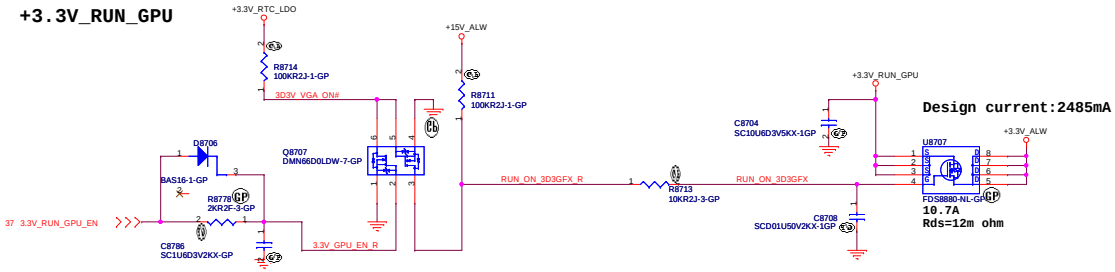
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
nductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->350KHz

CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

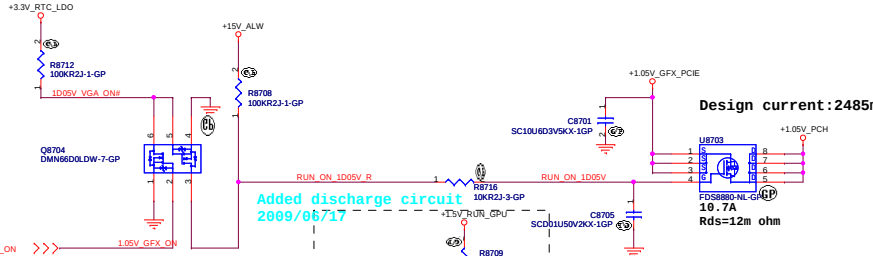
Title: TPS51218 +VCC_GFX_CORE
Size: Custom | Document Number: DW Calpella (Discrete) | Rev: -1
Date: Thursday, February 04, 2010 | Sheet 86 of 95

+3.3V_RUN_GPU

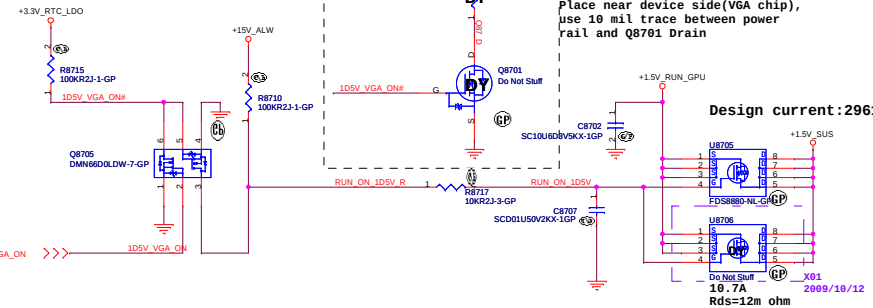


Added +1.05V_GFX_PCIE, +1.5V_RUN_GPU power switch 2009/05/25

+1.05V_GFX_PCIE:

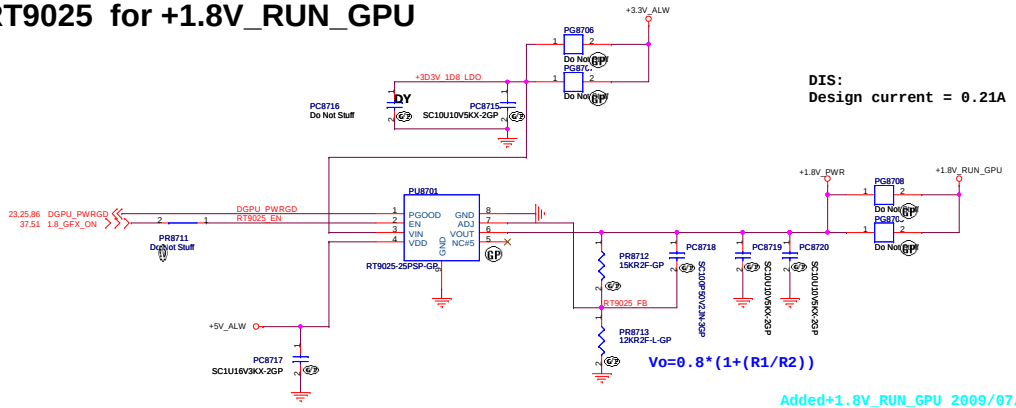


+1.5V_RUN_GPU:



+1.8V_RUN_GPU

RT9025 for +1.8V_RUN_GPU



Added+1.8V_RUN_GPU 2009/07/17

CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO 1.8V

Size: Custom | Document Number: Vostro Calpella | Rev: -1

Date: Thursday, February 04, 2010 | Sheet 87 of 95

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	20	2009/10/23	EMI		CRT RGB signal serics 0 ohm resistor at PCH side for EMI request.	SB
2	55	2009/10/22	EMI		CRT RGB signal serics 0 ohm resistor at connector side for EMI request.	SB
3	63	2009/10/23	EMI		Add USB2 and USB3 common choke for EMI request.	SB
4	73	2009/10/23	EMI		Add 0.1UF on EC7304 for EMI request	SB
5	43	2009/12/06	EMI		Add 0.1UF on PC4303 for EMI request	SC
6	46	2009/12/06	EMI		Add 0.1UF on PC4610 and PC4616 for EMI request	SC
7	49	2009/12/06	EMI		Add 0.1UF on PC4912 for EMI request	SC
8	52	2009/12/06	EMI		Add 0.1UF on PC5215 for EMI request	SC
9	73	2009/12/06	EMI		Add VARISTOR on EC7302 and EC7303 for EMI request.	SC
10	73	2009/12/06	EMI		Add camera USB port 11 common choke for EMI request.	SC
11	77	2009/12/06	EMI		Add 1000PF on WIRELESS_ON#/OFF for EMI request	SC
12	78	2009/12/08	EMI		Add 0.1UF on C7802 for EMI request	SC
13	79	2009/12/08	EMI		Add 0.1UF on +PWR_SRC, +DC_IN and KBC_PWR for EMI request	SC
14	23	2009/12/06	EMI		Change RN2304 from 0 ohm to 33 ohm for EMI request.	SC
15	55	2009/12/06	EMI		1. Change C5501, C5506 and C5508 from 8PF to 10PF for EMI request. 2. Change L5501, L5502 and L5503 from 22 ohm to 60 ohm for EMI request. 3. Change C5507, C5509 and C5512 from 8PF to 22PF for EMI request.	SC
16						
17						
18						
19						
20						
21						
22						

CFD DIS

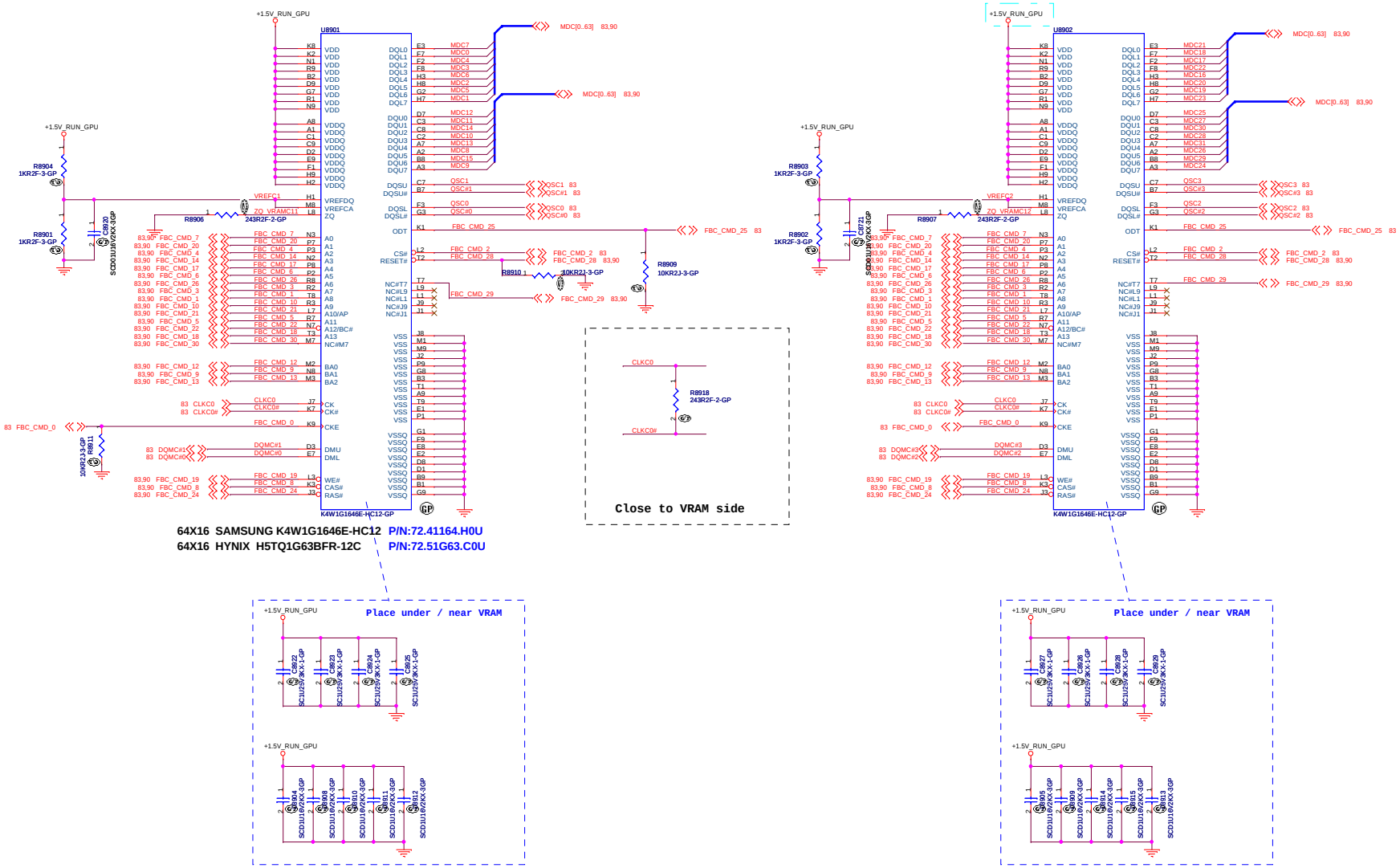
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change List-EMI

Size: Custom | Document Number: Vostro Calpella | Rev: -1

Date: Thursday, February 04, 2010 | Sheet 88 of 95

SSID = VIDEO



CFD DIS

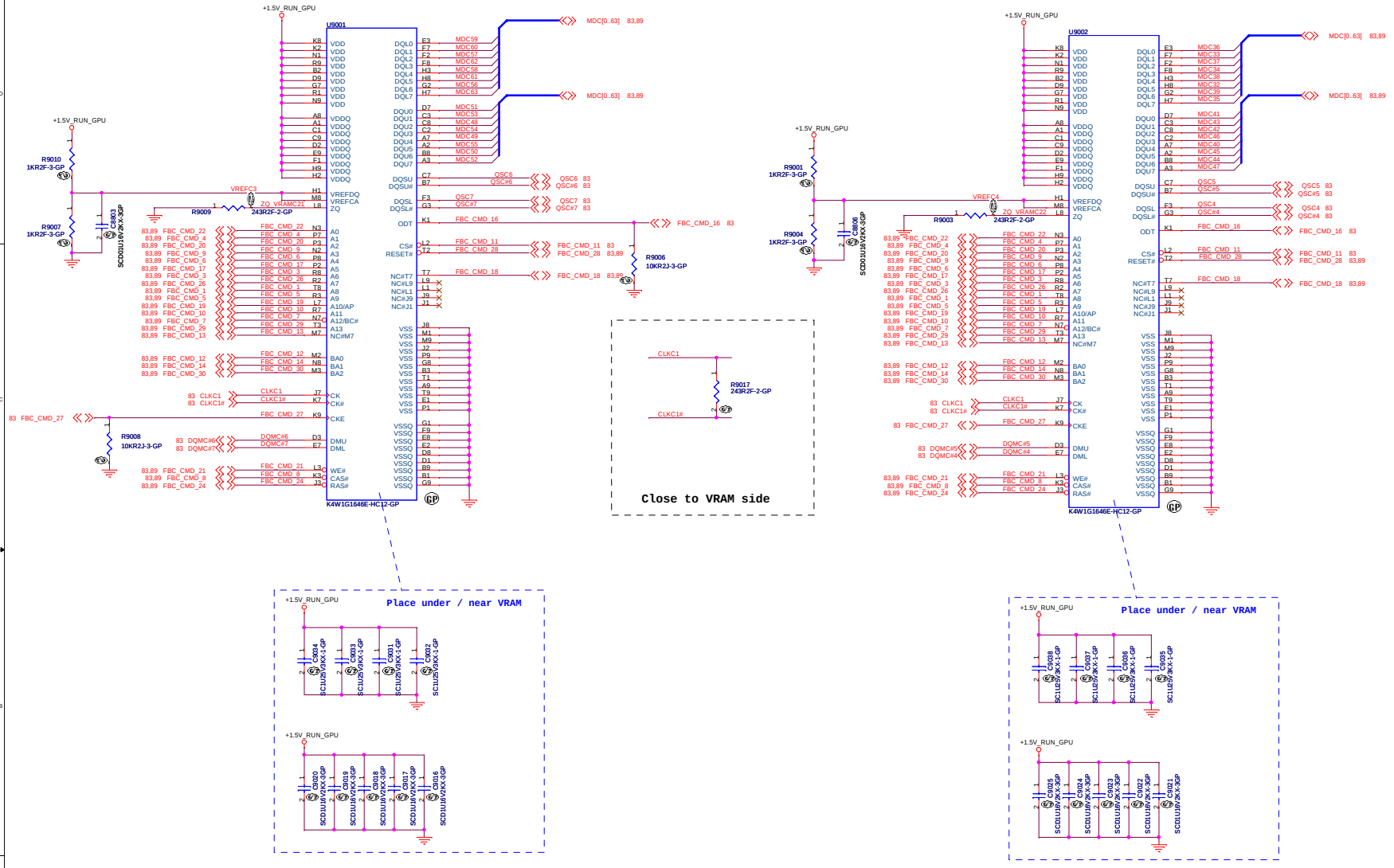
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM(1/2)**

Size	Document Number	Rev
A2	Vostro Calpella	-1

Date: Thursday, February 04, 2010 Sheet 89 of 95

SSID = VIDEO



CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
VRAM		
Size: A2	Document Number: Vostro Calpella	Rev: -1
Date: Thursday, February 04, 2010	Sheet 90 of 95	

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	46	2009/10/21	Power Team		Change PU4603 from TPS51125 to RT8205B.	SB
2	46	2009/10/21	Power Team		Net 51125_EN connect PR4622 to +PWR_SRC for RT8205B.	SB
3	46	2009/10/21	Power Team		PR4604 and PR4605 add 4.7ohm for RT8205B.	SB
4	46	2009/10/21	Power Team		Mount PR4607 and PC4621.	SB
5	52	2009/10/21	Power Team		Chagne PR5211 to 19.6K ohm for OCP seting.	SB
6	53	2009/10/21	Power Team		PR5328 change to 60.4Kohm for load line.	SB
7	53	2009/10/21	Power Team		PC5318 change to 560pF for transient response.	SB
8	53	2009/10/21	Power Team		PC5307 change to 68nF for Intel spec.	SB
9	53	2009/10/21	Power Team		Remove Ouput Gap PG5301 PG5304 PG5306 PG5308 PG5310~PG5318 and PG5321.	SB
10	53	2009/10/21	Power Team		Mount PR5317 and PC5315	SB
11	46	2009/12/11	Power Team		POP PR4619 and Dummy PR4618 to improve +15V_Pump Power On issue.	SC
12	47	2009/12/11	Power Team		PR4796 change from 768ohm to 715ohm (64.71505.6DL).	SC
13	47	2009/12/11	Power Team		PR4780 change from 2.37Kohm to 2.2Kohm(64.22015.6DL).	SC
14						
15						
16						
17						
18						
19						
20						
21						
22						
23						

CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change List-Power*

Size: Custom | Document Number: *Vostro Calpella* | Rev: -1

Date: Thursday, February 04, 2010 | Sheet 91 of 95

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	25	2009/10/12	EE		Change DGPU_PRSNT# from pull high to pull low for DIS.	SB
2	30	2009/10/12	EE		Change CODEC from 91HD81 to 92HD79.	SB
3	37	2009/10/12	EE		Add R3729 pull low resistor for SW_UMA_ID for UMA.	SB
4	37	2009/10/12	EE		Dummy R3708 and mount R3701 for board ID change.	SB
5	54	2009/10/12	EE		Add R5415 100 ohm resistor for KBC ESD.	SB
6	68	2009/10/12	EE		Remove Keyboard EMI cap.	SB
7	37	2009/10/12	EE		Added Switchable Detection circuit Pull Low for UMA and ARD DIS. Pull High for CFD.	SB
8	78	2009/10/12	ME		Change CON3(Finger Printer CONN) to 20.K0315.005.	SB
9	68	2009/10/12	ME		Change TPAD1(Touch PAD CONN) to 20.K0320.004.	SB
10	79	2009/10/12	ME		Change H11 to BOSS5 (PN:34.4CK01.001) for DIS.	SB
11	23	2009/10/13	EE		Added 25M Crystal for DCI (DisplayClock_Integration). For UMA and ARD DIS.	SB
12	25	2009/10/13	EE		Swapped Q2515 C,E Pin ,For correct.	SB
13	64	2009/10/13	ME		Change WLAN connector to 62.10043.841.	SB
14	24	2009/10/13	EE		Add 22 ohm resistances at LPC BUS.	SB
15	81	2009/10/13	EE		Connect AC_PRESENT_EC to GPU GPIO12.	SB
16	27	2009/10/20	EE		Change L2701 , L2704 for update component.	
17	21,23	2009/10/20	EE		Changed EDID_SELECT# pin from PCH_GPIO66 to PCH_GPIO5 for fixed gitch.	SB
18	54	2009/10/20	EE		Change Q5401 from 84.03456.C3D to 84.03456.D3D.	SB
19	18,19	2009/10/20	EE		Add 4.7UF at DIMM1 and DIMM2 VREF voltage for noise over SPEC.	SB
20	22	2009/10/20	EE		Added 3V_5V_POK to control resume reset sequence prevent RTC data loss	SB
21	37	2009/10/20	EE		Update 10mW circuit.	SB
22	24	2009/10/23	EE		Change X2401 form 82.30001.691 to 82.30001.861.	SB

CFD DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change List-EE 01*

Size: Custom | Document Number: *Vostro Calpella* | Rev: -1

Date: Thursday, February 04, 2010 | Sheet 92 of 95

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
23	70	2009/10/20	EE		Change Debug board connector to 20.D0183.110.	SB
24	74	2009/10/20	EE		Change DGPU_SELECT# level shift circuit to dual MOS.	SB
25	76	2009/10/20	EE		Dummy connector TPM1 and resistor R2112.	SB
26	37,78	2009/10/20	EE		Removed CAPA_RST# from Capacity board..	SB
27	9,42 ,50	2009/10/21	EE		Add Intel S3 power reduction circuit.	SB
28	7	2009/10/21	EE		Removed RN701,RN702,RN703,RN704 for ICS,Silego has integrated 33ohm series resistors.	SB
29	9	2009/10/21	EE		Change RN907 to 1K ohm for update component.	SB
30	80,81	2009/10/23	EE		Change L8005 and L8110 to 68.00143.221. For +1.05V_GFX_PCIE drop over SPEC.	SB
31	7,9 20,22 23,24 25,26 27,30 37,57 73,81	2009/12/04	EE		Change 0 ohm to short pad. R708,R709,RN901,RN903,RN906,R2011,R2207,R2219 R2220,RN2311,RN2305,RN2310,R2417,R2506,R2602 R2609,R2601,R2605R2606,R2707,R3002,L3001,L3002 L3003,R3755,R3735,R5708,R5703,R5707,R5706,R5702 R5705,R5711,R5712,R7301,R8135,R8136	SC
32	23	2009/12/06	EE		Remove R3017 and R3019.	SC
33	37	2009/11/14	EE		Change board ID to SC.	SC
34	37	2009/12/06	EE		Add MUX for PANEL_BKEN.	SC
35	44	2009/12/06	ME		Change BAT1 to 20.81180.009.	SC
36	60	2009/12/07	ME		Change speaker pin define for ME request.	SC
37	77	2009/12/02	ME		Change CON6 to 20.K0426.040.	SC
38	79	2009/12/06	ME		Change BOSS3 and BOSS5 to 34.4CK01.201.	SC
39	80	2009/12/06	EE		Delete C8067.	SC

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
40	9,22 24,27 37,62	2010/01/04	EE		Change 0 ohm to short pad. R908,R2121,R2211,R2212,R2213,R2413,R2414,R2415,R2708,R3719,R6205,R6204,R6206,	-1
41	21	2010/01/04	EE		Change camera usb port 11 to port 6 Remove USB Port 9 TP(TP2131,TP2132)	-1
42	37	2010/01/06	EE		reserve Reset IC(U3704) and DUMMY	-1
43	78	2010/01/06	EE		Add 0 ohm (R7803)	-1
44	21,22 37,78	2010/01/06	EE		Change 0 ohm to short pad. R2116,R2210,R3702,R7801,R7802	-1
45	63	2010/01/06	EE		U6301 DUMMY	-1
46	78	2010/01/06	EE		Del EL7801	-1
47	20	2010/01/06	EE		DEL R2012、R2013、R2014 For PCH SIDE	-1
48	63,64	2010/01/06	EE		Change 0 ohm to short pad. R6306,R6301,R6304,R6310,R6311,R6312,R6406,R6405	-1
49	63,73	2010/01/06	EE		Del TR6301,TR6302,TR6303,L6401 and R6302,R6303,R6308,R6309,R7303,R7302	-1
50	21	2010/01/06	EE		Remove USB Port 11TP (TP2129,TP2130)	-1
51	59	2010/01/07	EE		Change SMD TYPE(62.10065.B81) to DIP TYPE(22.10300.971) for SATA HDD Connector	-1
52	45,46 47,50 53,87	2010/01/07	EE		Change 0 ohm to short pad. PR4505,PR4509,PR4510,PR4515,PR4522,PR4524,PR4530,PR4531,PR4532,PR4533 PR4616,PR4619,PR4620,PR4736~PR4746,PR4748,PR4750,PR4752,PR4768,PR4794 PR5002,PR5015,PR5302,PR5303,PR5304,PR5305,PR5307,PR5308,PR5309,PR5310,PR5331,PR5332,PR5333,PR8711,R6	-1
53	62,24 37	2010/01/07	EE		Change Short Pad to 0 ohm R6206,R2413,R2414,R2415 Change 0 ohm to Short Pad R3755,R3735	-1
54	59	2010/01/11	EE		change 2.2k ohm to short pad (PR5102) and add PR5106 to GND	-1
						-1
39	80	2009/12/06	EE		Delete C8067.	SC

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
55	73	2010/01/12	EE		Remove EC7302 and EC7303	-1

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