Table of Contents

Intel Skylake-U Platform

Skylake-U CPU (TDP 15W) SoC

Project Information

Phase: EVT

PCB AND SILKSCREEN COLOR		
Program Phase	Color of PCB	Silkscreen
EVT	RED	YELLOW
DVT	LIGHT BLUE	YELLOW
PVT/MVB / PRODUCTION	GREEN	WHITE

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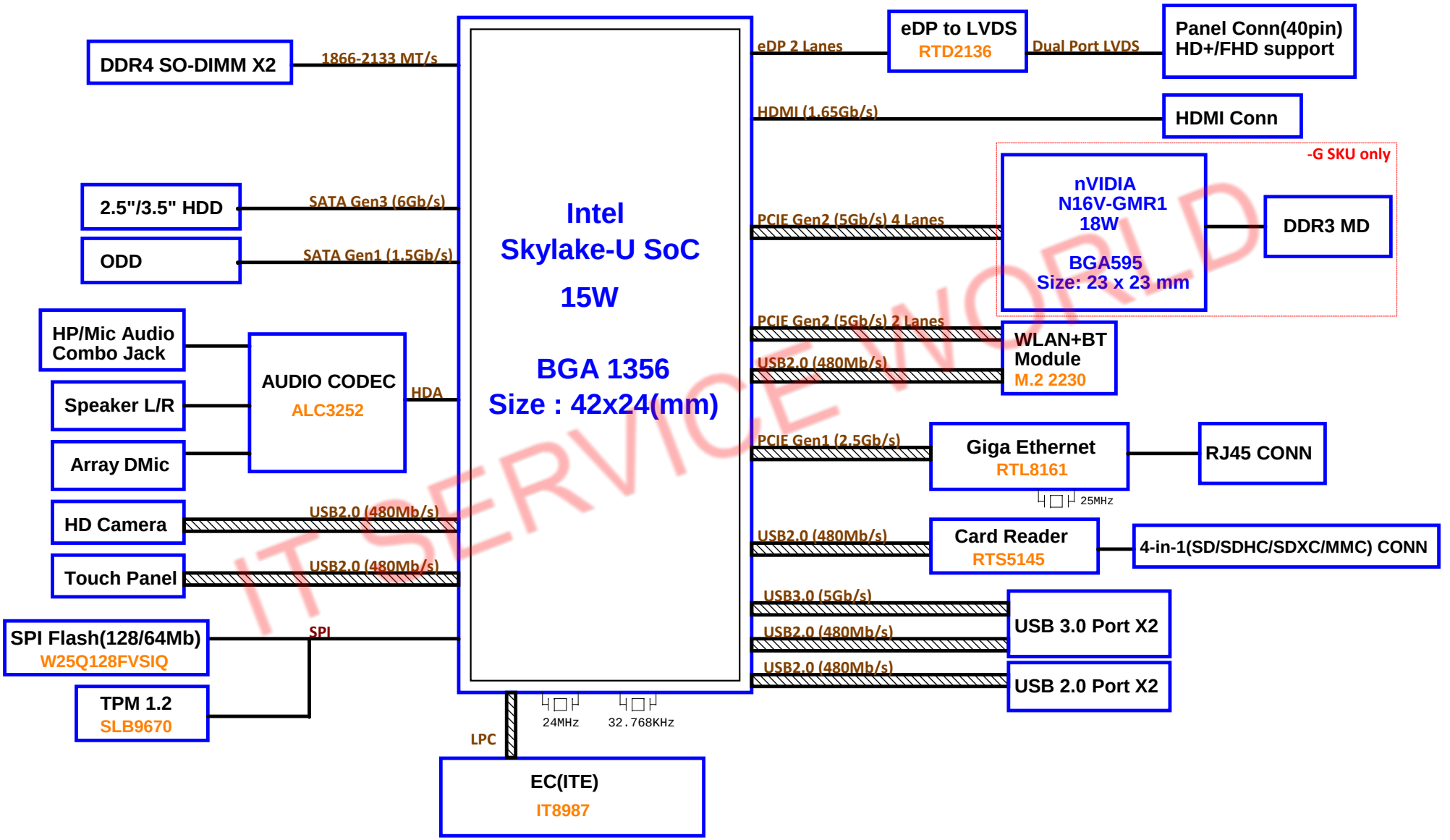
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	Front Page	1A

Date: Thursday, December 17, 2015 Sheet 1 of 58

Intel Skylake-U Platform Block Diagram (Hawaii-G/-U)



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PROJECT: HP-Hawaii
Size: Custom | Document Number: Block Diagram | Rev: 1A
Date: Thursday, December 17, 2015 | Sheet 2 of 58

[5,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[5,7,17,46,48] +VCCIO
[5,6,7,10,43,46] +VCCSTPLL

HDMI

U21A SKL_ULT ?

[22] IN_D2# → IN_D2# E55 DDI1_TXN[0]
[22] IN_D2 → IN_D2 F55 DDI1_TXP[0]
[22] IN_D1# → IN_D1# E58 DDI1_TXN[1]
[22] IN_D1 → IN_D1 F58 DDI1_TXP[1]
[22] IN_D0# → IN_D0# F53 DDI1_TXN[2]
[22] IN_D0 → IN_D0 G53 DDI1_TXP[2]
[22] IN_CLK# → IN_CLK# F56 DDI1_TXN[3]
[22] IN_CLK → IN_CLK G56 DDI1_TXP[3]

C50 DDI2_TXN[0]
D50 DDI2_TXP[0]
C52 DDI2_TXN[1]
D52 DDI2_TXP[1]
A50 DDI2_TXN[2]
B50 DDI2_TXP[2]
D51 DDI2_TXN[3]
C51 DDI2_TXP[3]

DDI

EDP_TXN[0] C47 → INT_EDP_TXN0 → INT_EDP_TXN0 [20]
EDP_TXP[0] C46 → INT_EDP_TXP0 → INT_EDP_TXP0 [20]
EDP_TXN[1] D46 → INT_EDP_TXN1 → INT_EDP_TXN1 [20]
EDP_TXP[1] C45 → INT_EDP_TXP1 → INT_EDP_TXP1 [20]
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP

EDP_AUXN E45 → INT_EDP_AUXN → INT_EDP_AUXN [20]
EDP_AUXP F45 → INT_EDP_AUXP → INT_EDP_AUXP [20]

EDP_DISP_UTIL B52

DISPLAY SIDEBANDS

[22] SDVO_CLK → L13 GPP_E18/DDPB_CTRLCLK
[22] SDVO_DATA → L12 GPP_E19/DDPB_CTRLDATA

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN G48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP F46

+3V → R208 2.2K_4 → N7 GPP_E20/DDPC_CTRLCLK
N8 GPP_E21/DDPC_CTRLDATA

TP22 → N11 GPP_E22/DDPD_CTRLCLK
N12 GPP_E23/DDPD_CTRLDATA

+VCCIO → R116 24.9/F_4 → EDP_RCOMP E52 EDP_RCOMP

GPP_E13/DDPB_HPD0 L9 → PCH_HDMI_HPD → PCH_HDMI_HPD [22]
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 N9
GPP_E16/DDPE_HPD3 L10 → EDP_HPD → EDP_HPD [20]
GPP_E17/EDP_HPD

EDP_BKLTEN R12 → PCH_LVDS_BLON → PCH_EDP_BLON [21]
EDP_BKLTCTL R11 → PCH_DPST_PWM → PCH_DPST_PWM [20]
EDP_VDDEN U13 → PCH_LCDVCC_EN → PCH_LCDVCC_EN [21]

SKL_ULT
REV = 1

1 OF 20

?

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

+3V → R505 *10K_4 → EDP_HPD → R504 100K_4

U21D SKL_ULT ?

TP45 → CATERR# D63 CATERR#
[29] EC_PECI → EC_PECI A54 PECI
[29,43,47] H_PROCHOT# → R408 499/F_4 → PROCHOT# C65 PROCHOT#
PM_THRMTRIP# C63 THERMTRIP#
A65 SKTOCC#

CPU MISC

[17] XDP_BPM0 → C55 BPM#[0]
[17] XDP_BPM1 → D55 BPM#[1]
B54 BPM#[2]
C56 BPM#[3]

A6 GPP_E3/CPU_GP0
A7 GPP_E7/CPU_GP1
BA5 GPP_B3/CPU_GP2
AY5 GPP_B4/CPU_GP3

[26] RF_OFF → RF_OFF

R170 49.9/F_4 → PROC_POPIRCOMP AT16 PROC_POPIRCOMP
R164 49.9/F_4 → PCH_OPI_RCOMP AU16 PCH_OPIRCOMP
R79 49.9/F_4 → EDRAM_OPIO_RCOMP H66 OPCE_RCOMP
R80 49.9/F_4 → EOPIO_RCOMP H65 OPC_RCOMP

JTAG

PROC_TCK B61 → XDP_TCK0 → XDP_TCK0 [17]
PROC_TDI A61 → XDP_TDI_CPU → XDP_TDI_CPU [17]
PROC_TDO C60 → XDP_TDO_CPU → XDP_TDO_CPU [17]
PROC_TMS B59 → XDP_TMS_CPU → XDP_TMS_CPU [17]
PROC_TRST# → XDP_TRST#_CPU → XDP_TRST#_CPU [17]

PCH_JTAG_TCK B56 → JTAG_TCK_PCH → JTAG_TCK_PCH [17]
PCH_JTAG_TDI D59 → JTAG_TDI_PCH → JTAG_TDI_PCH [17]
PCH_JTAG_TDO A56 → JTAG_TDO_PCH → JTAG_TDO_PCH [17]
PCH_JTAG_TMS C59 → JTAG_TMS_PCH → JTAG_TMS_PCH [17]
PCH_TRST# C61 → XDP_TRST#_CPU
JTAGX A59 → JTAGX_PCH → JTAGX_PCH [17]

SKL_ULT
REV = 1

4 OF 20

+VCCSTPLL → PM_THRMTRIP# R422 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL . 470 OHM IS FOR I/P

PLACE NEAR CPU

+VCCIO
XDP_TMS_CPU R435 *51_4
XDP_TDI_CPU R436 *51_4
XDP_TDO_CPU R427 *51_4

+VCCSTPLL
H_PROCHOT# R406 1K_4
XDP_TCK0 R430 51_4
XDP_TRST#_CPU R439 51_4

EC-PV-01

+VCCIO → R428 *0/S_4
R431 *51_4 → JTAGX_PCH
R440 51_4 → JTAG_TMS_PCH
R444 51_4 → JTAG_TDI_PCH
R448 51_4 → JTAG_TDO_PCH
R443 51_4 → JTAG_TCK_PCH

Close to Chipset

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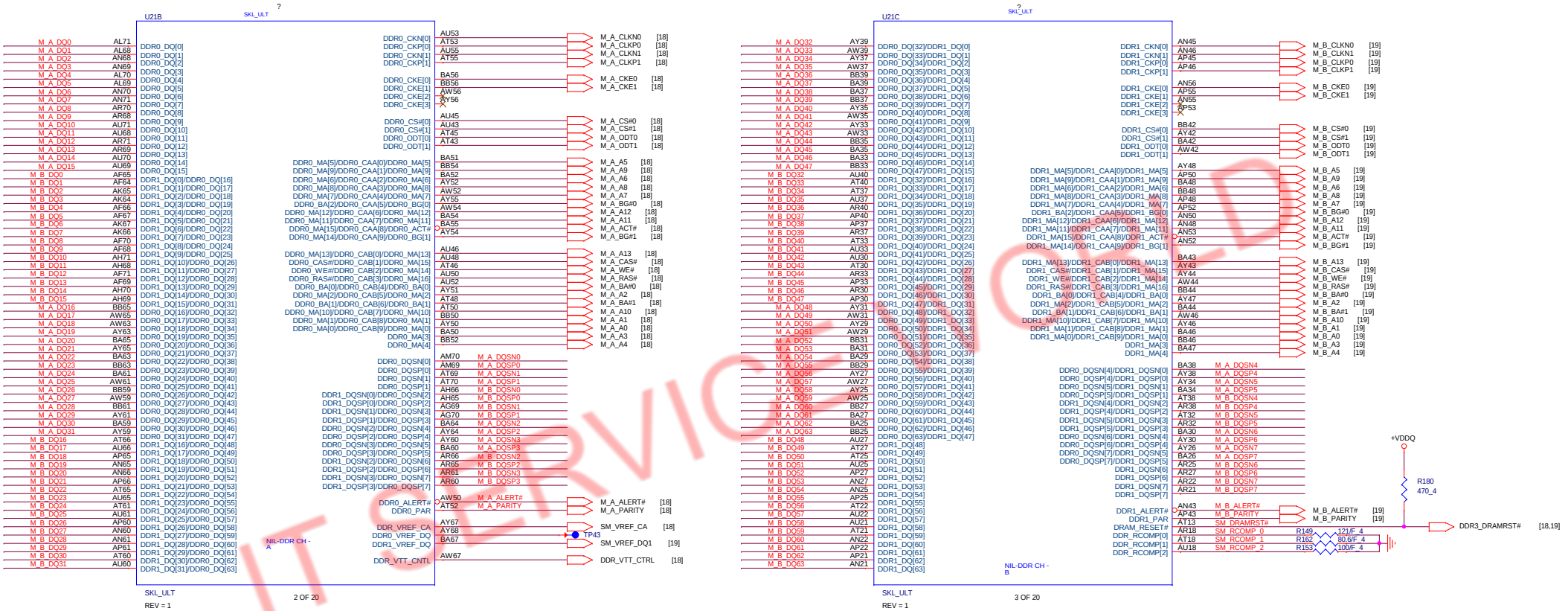
Size	Document Number	Rev
Custom	SKL CPU eDP/DDI/MISC	1A

Date: Wednesday, March 09, 2016 Sheet 3 of 58

SkyLake ULT Processor (DDR4 IL)



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Size	Document Number	Rev
Custom	SKL CPU DDR	1A

Date: Wednesday, March 09, 2016 Sheet 4 of 58

[11,12,13,15,16,17,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52] +3V_S5
[3,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[21,23,27,28,32,39,40,41,43,45,46,47,48,52] +5V_S5
[3,7,17,46,48] +VCCIO
[3,6,7,10,43,46] +VCCSTPLL
[14,16] +3V_RTC_2

U21K SKL_ULT ?
SYSTEM POWER MANAGEMENT

[24,26,29,31,33] PLTRST# → PLTRST# → AN10 GPP_B13/PLTRST#
[17] SYS_RESET# → SYS_RESET# → B5 SYS_RESET#
[17,29] RSMRST# → R485 *0/S_4 → RSMRST#_R → AY17 RSMRST#
R403 *10K_4 → PROCPWRGD → A68 PROCPWRGD
H_VCCST_PWRGD → B65 VCCST_PWRGD
EC-PV-01
[17,29] HWPG → R484 *0/S_4 → SYS_PWROK → B6 SYS_PWROK
DPWROK → BA20 PCH_PWROK
BB20 DSW_PWROK
[29] EC_SUSPWRACK → *0_4 R580 → SUSWARN# → AR13 GPP_A13/SUSWARN#/SUSPWRDNACK
[29] EC_SUSACK# → *0_4 R192 → SUSACK# → AP11 GPP_A15/SUSACK#
[24,26] PCIE_WAKE# → PCIE_WAKE# → BB15 WAKE#
TP23 → PCIE_LAN_WAKE# → AM15 GPD2/LAN_WAKE#
TP58 → LAN_DIS# → AW17 GPD11/LANPHYPC
TP18 → AT15 GPD7/RSVD

GPP_B12/SLP_S0# AT11 PM_SLP_S0# → PM_SLP_S0# [17,29]
GPD4/SLP_S3# AP15 → SUSB# [17,29]
GPD5/SLP_S4# BA16 → SUSC# [17,29]
GPD10/SLP_S5# AY16 → SLP_S5# [17,29]
SLP_SUS# AN15 → PM_SLP_SUS# [29]
SLP_LAN# AW15 SLP_LAN# → TP62
GPD9/SLP_WLAN# BB17 SLP_WLAN# → TP60
GPD6/SLP_A# AN16 → SLP_A# [17] → TP31
GPD3/PWRBTN# BA15 DNBSWON# → DNBSWON# [17,29]
GPD1/ACPRESENT AY15 AC_PRESENT_EC → AC_PRESENT_EC [29]
GPD0/BATLOW# AU13 PM_BATLOW_N_EC → TP27
GPP_A11/PME# AU11
INTRUDER# AP16 INTRUDER# R R177 1M_4 → +3V_RTC_2
AM10 EXT_PWR_GATE#
GPP_B11/EXT_PWR_GATE# AM11
GPP_B2/VRALERT# A2

SKL_ULT
REV = 1
11 OF 20
?

RSMRST# → EC5 *220P/50V_4
SYS_RESET# → C554 *220P/50V_4
PLTRST# → C549 *220P/50V_4

[29] EC_DPWROK → EC_DPWROK R538 *0/S_4 → RSMRST# R483 *0_4 → DPWROK
EC-PV-01

PCH Pull-high/low(CLG)

+3V_S5
SUSWARN# R189 *10K_4
SUSACK# R191 *10K_4
PM_BATLOW_N_EC R181 10K_4

+3V_S5
PCIE_WAKE# R493 1K_4
AC_PRESENT_EC R490 10K_4
PCIE_LAN_WAKE# R187 10K_4
EXT_PWR_GATE# R186 *20K/F_4

+3V
SYS_RESET# R500 10K_4
PLTRST# R222 *10K/F_4
R223 100K/F_4
RSMRST# R487 10K_4
DPWROK R481 *100K/F_4

Close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

+VCCIO +VCCSTPLL
R401 1K_4
R405 *1K_4
HWPG D141 2 RB500V-40 H_VCCST_PWRGD_R R404 60.4_4 H_VCCST_PWRGD
C512 *10P/50V_4

+VCCIO +5V_S5 +3V_S5
R478 15K_4
R479 100K_4
R476 10K_4
HWPG
+1.0V_PWRGD_G2 2 Q31 2N7002K
R475 100K_4
+1.0V_PWRGD_G1 2 Q32 METR3904-G
C530 0.1U/16V_4
R480 100K_4

System PWR_OK(CLG)

SYS_PWROK
EC-PV-01
R496 *0/S_4
EC_PWROK → EC_PWROK [29]
C552 *0.1U/16V_4
R497 100K/F_4

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Size	Document Number	Rev
Custom	SKL CPU Power Management	1A

Date: Wednesday, March 09, 2016 Sheet 5 of 58

[32,43,44] +VCC_CORE
[7] +VCCSTG
[3,5,7,10,43,46] +VCCSTPLL

+VCC_CORE

C270 10U/6.3V_4 C265 22U/6.3V_6 C229 22U/6.3V_6 C267 22U/6.3V_6 C225 22U/6.3V_6 C226 22U/6.3V_6 C266 22U/6.3V_6 C269 22U/6.3V_6
C233 10U/6.3V_4 C246 10U/6.3V_4 C268 10U/6.3V_4 C236 10U/6.3V_4 C256 10U/6.3V_4 C241 10U/6.3V_4 C258 10U/6.3V_4
C227 22U/6.3V_6 C264 22U/6.3V_6 C245 22U/6.3V_6 C228 22U/6.3V_6 C223 22U/6.3V_6 C230 22U/6.3V_6

Under CPU

U21L SKL_ULT ?
CPU POWER 1 OF 4
33A

A30	VCC_A30	VCC_G32	G32
A34	VCC_A34	VCC_G33	G33
A39	VCC_A39	VCC_G35	G35
A44	VCC_A44	VCC_G37	G37
AK33	VCC_AK33	VCC_G38	G38
AK35	VCC_AK35	VCC_G40	G40
AK37	VCC_AK37	VCC_G42	G42
AK38	VCC_AK38	VCC_J30	J30
AK40	VCC_AK40	VCC_J33	J33
AL33	VCC_AL33	VCC_J37	J37
AL37	VCC_AL37	VCC_J40	J40
AL40	VCC_AL40	VCC_K33	K33
AM32	VCC_AM32	VCC_K35	K35
AM33	VCC_AM33	VCC_K37	K37
AM35	VCC_AM35	VCC_K38	K38
AM37	VCC_AM37	VCC_K40	K40
AM38	VCC_AM38	VCC_K42	K42
G30	VCC_G30	VCC_K43	K43
K32	RSVD_K32	VCC_SENSE	E32
AK32	RSVD_AK32	VSS_SENSE	E33
AB62	VCCOPC_AB62	VIDALERT#	B63
P62	VCCOPC_P62	VIDSCK	A63
V62	VCCOPC_V62	VIDSOUT	D64
H63	VCC_OPC_1P8_H63	VCCSTG_G20	G20
G61	VCC_OPC_1P8_G61		
AC63	VCCOPC_SENSE		
AE63	VSSOPC_SENSE		
AE62	VCCEOPIO		
AG62	VCCEOPIO		
AL63	VCCEOPIO_SENSE		
AJ62	VSSEOPIO_SENSE		

SKL_ULT
REV = 1
12 OF 20
?

+VCC_CORE

C276 1U/6.3V_4 C249 1U/6.3V_4 C232 1U/6.3V_4 C247 1U/6.3V_4 C274 1U/6.3V_4 C261 1U/6.3V_4 C248 1U/6.3V_4
C240 1U/6.3V_4 C252 1U/6.3V_4 C251 1U/6.3V_4 C250 1U/6.3V_4 C271 1U/6.3V_4 C272 1U/6.3V_4 C259 1U/6.3V_4 C221 1U/6.3V_4

Under CPU

R129 100/F_4
R132 100/F_4
+VCC_CORE
VCC_SENSE [43]
VSS_SENSE [43]

100- ±1% pull-up to VCC near processor.

H_CPU_SVIDALRT#
VR_SVID_CLK_R
H_CPU_SVIDDAT
+VCCSTG

Close CPU

+VCC_CORE
C501 47U/6.3V_8 C237 47U/6.3V_8 C211 47U/6.3V_8 C75 47U/6.3V_8 C502 47U/6.3V_8 C239 47U/6.3V_8 C506 47U/6.3V_8 C217 47U/6.3V_8
+VCC_CORE
C243 10U/6.3V_4 C523 10U/6.3V_4 C521 10U/6.3V_4 C244 10U/6.3V_4 C519 10U/6.3V_4 C522 10U/6.3V_4 C524 10U/6.3V_4 C520 10U/6.3V_4

+VCC_CORE
C510 *1U/6.3V_4
C505 *22U/6.3V_6
C508 *1U/6.3V_4
C503 *22U/6.3V_6
RF RESERVE

Layout note: need routing together and ALERT need between CLK and DATA.

CLOSE TO CPU
PLACE THE PU RESISTORS

+VCCSTPLL
R418 56.2/F_4
H_CPU_SVIDALRT# R417 220/F_4 VR_SVID_ALERT# [43]
C513 *0.1U/16V_4

SVID ALERT

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE

+VCCSTPLL
R424 *54.9/F_4
VR_SVID_CLK_R EC-PV-01 R423 *0/S_4 VR_SVID_CLK [43]

SVID CLK

CLOSE TO CPU
PLACE THE PU RESISTORS

+VCCSTPLL
R412 100/F_4
H_CPU_SVIDDAT EC-PV-01 R413 *0/S_4 VR_SVID_DATA [43]

SVID DATA

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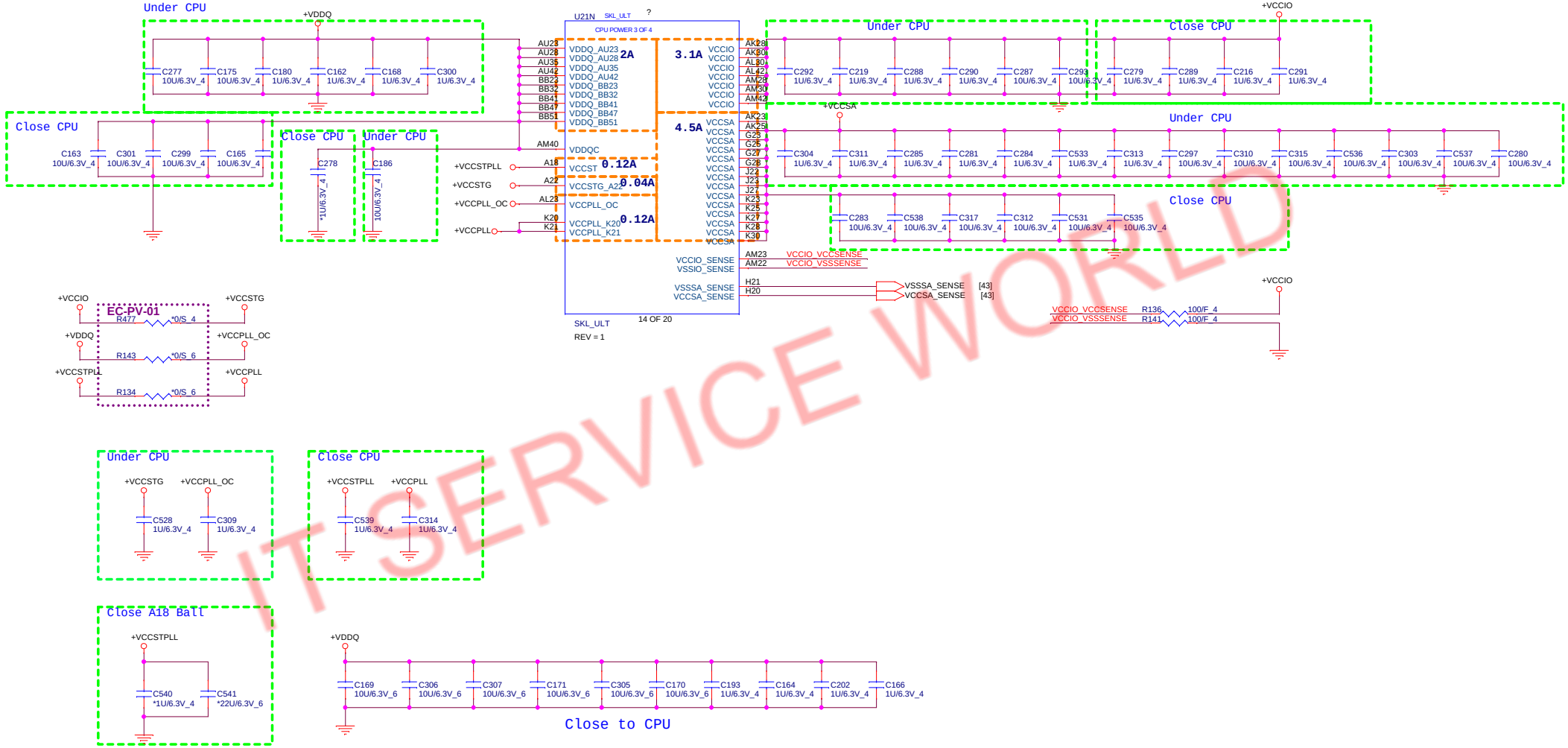
Size	Document Number	Rev
Custom	SKL CPU Power	1A
Date: Wednesday, March 09, 2016	Sheet 6 of 58	

[3,5,17,46,48] +VCCIO
[43,45] +VCCSA
[4,18,19,32,40] +VDDQ
[3,5,6,10,43,46] +VCCSTPLL
[6] +VCCSTG



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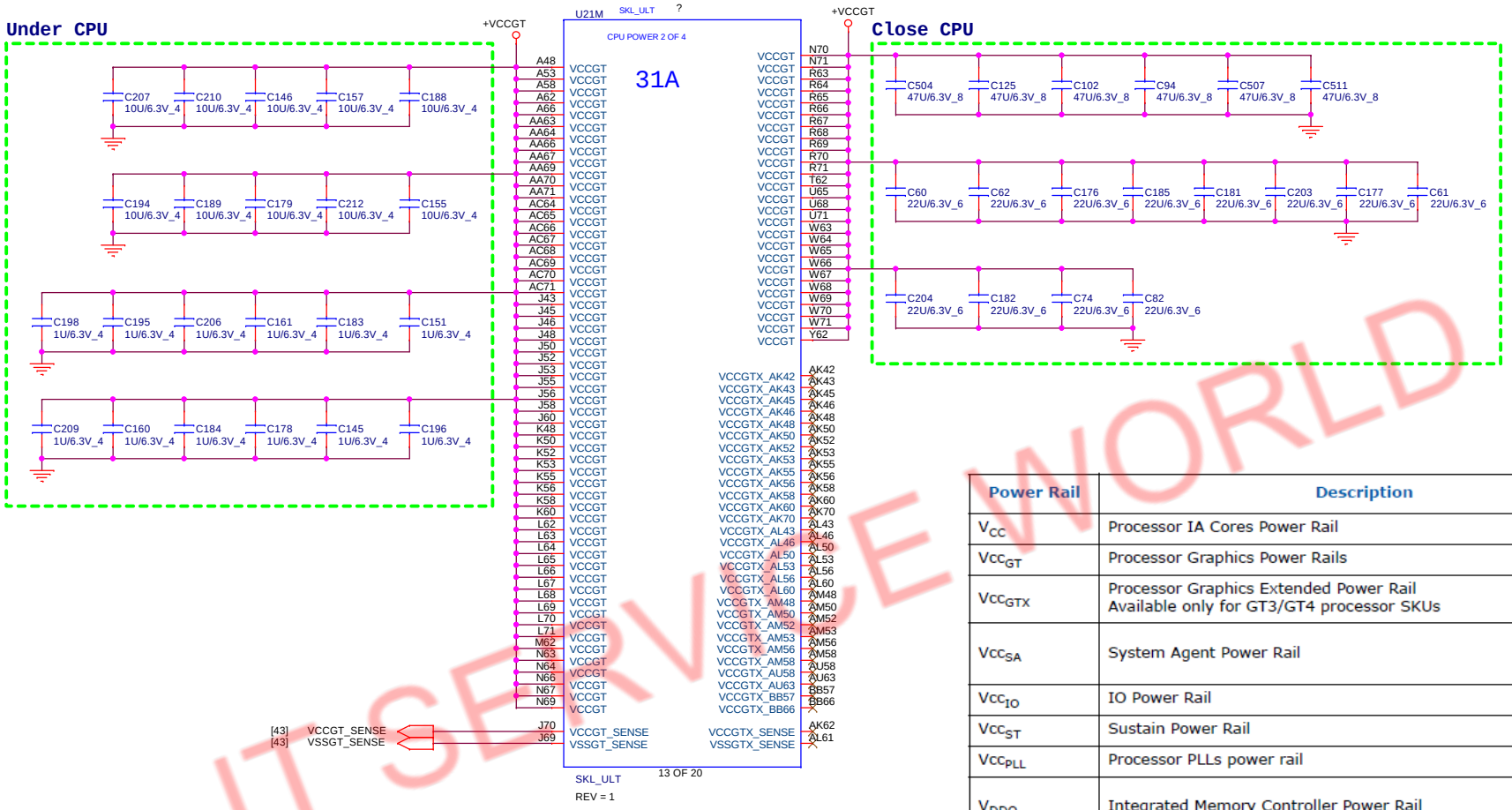
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU Power	1A

Date: Wednesday, March 09, 2016 Sheet 7 of 58



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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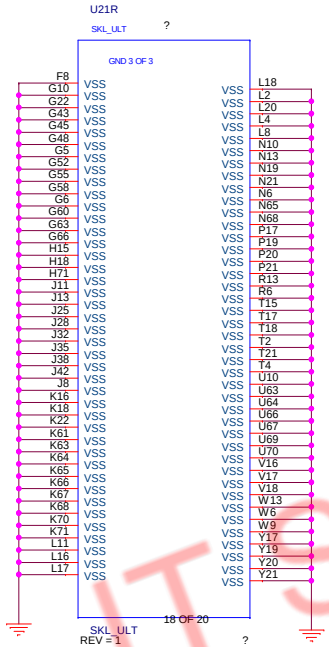
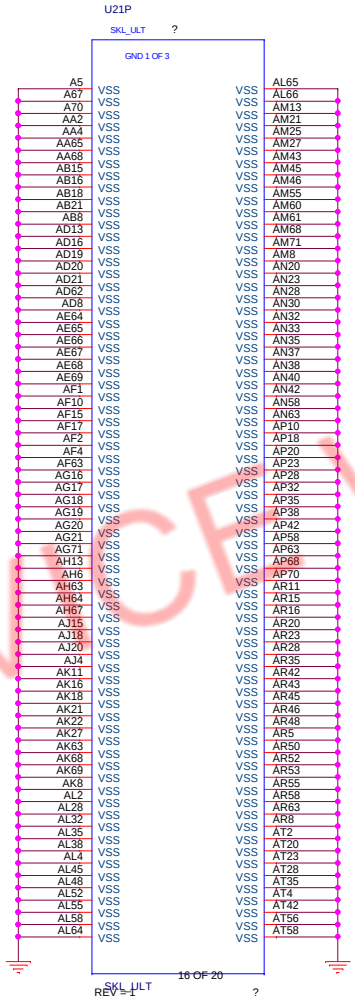
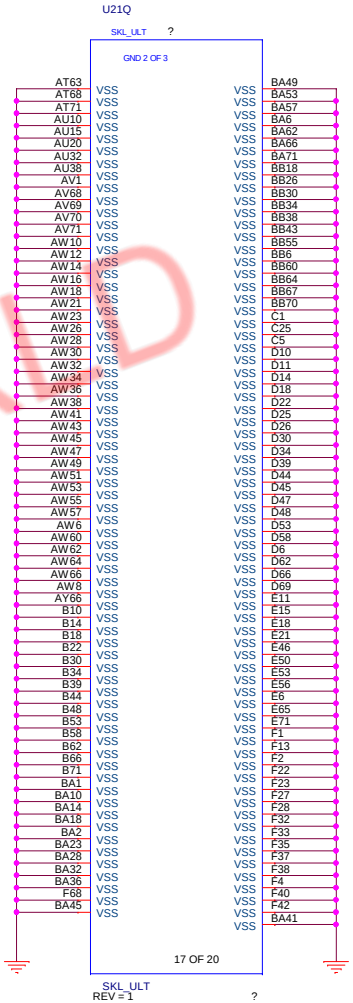
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU Power	1A
Date: Wednesday, March 09, 2016	Sheet 8 of 58	







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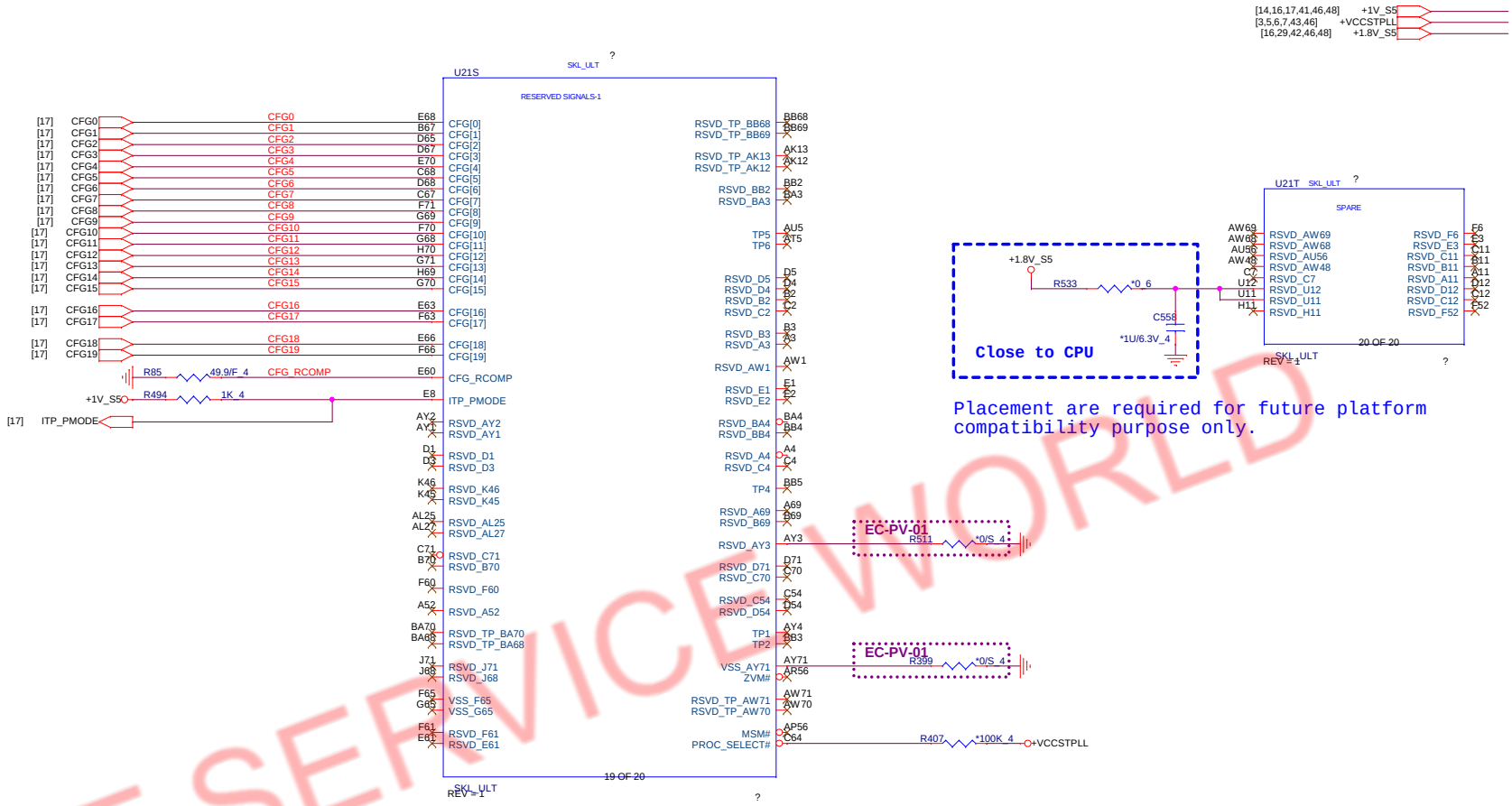
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU GND	1A

Date: Wednesday, March 09, 2016 Sheet 9 of 58



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R400 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R402 1K_4

HP Restricted Secret

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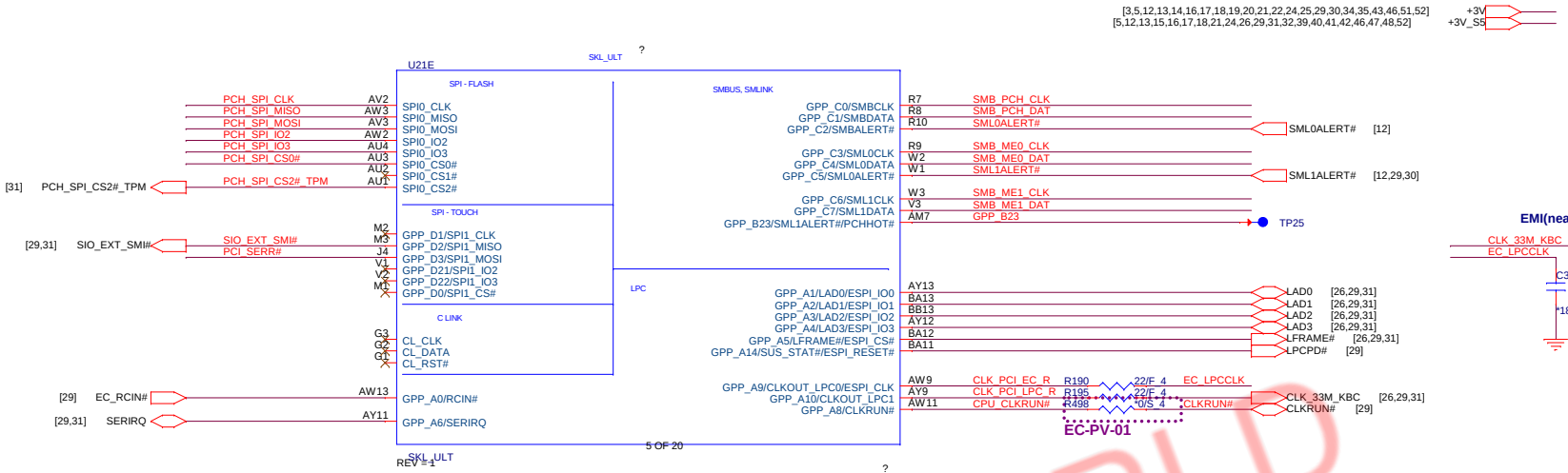
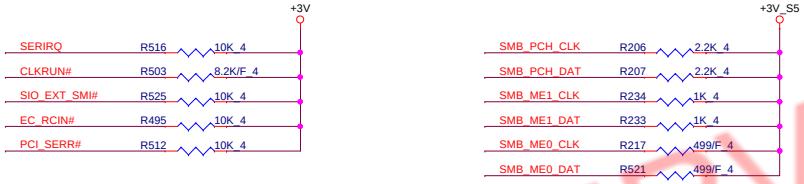
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU RSVD	1A

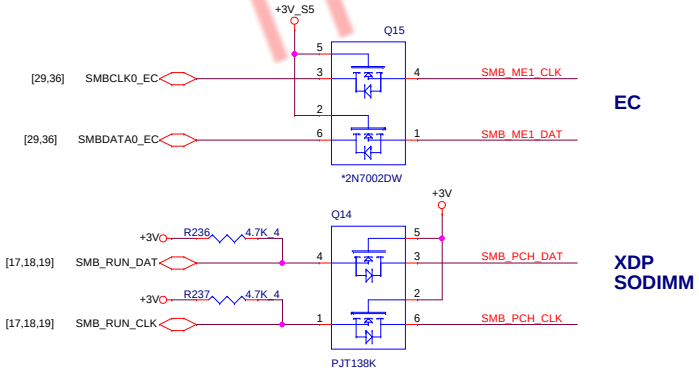
Date: Wednesday, March 09, 2016 Sheet 10 of 58



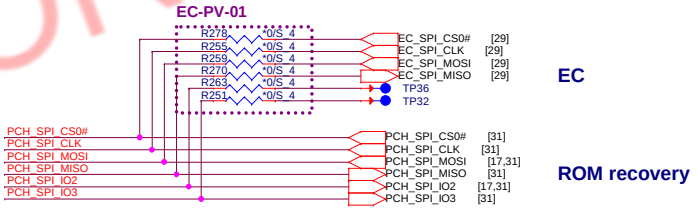
GPIO Pull UP

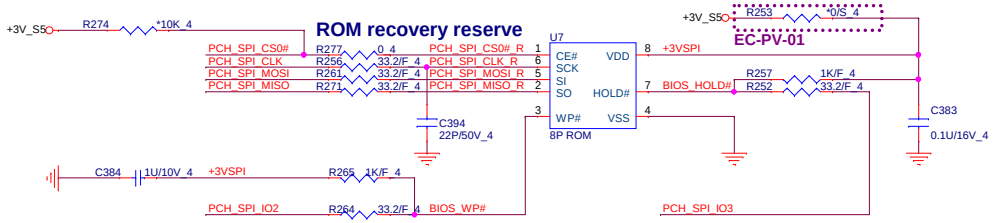


SMBus/Pull-up(CLG)



PCH SPI ROM(CLG)





Vender	Size	P/N
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GD	8MB	AKE2EZN0Q00 (GD25B64CSIGR)
Socket		DFHS08FS023

HP Restricted Secret

Quanta Computer Inc.
PROJECT: HP-Hawaii

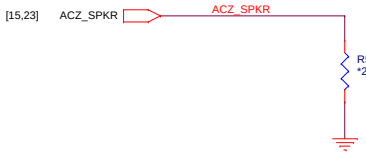
Size	Document Number	Rev
Custom	SKL CPU SPI/LPC/SMB	1A

Date: Tuesday, March 15, 2016 Sheet 11 of 58

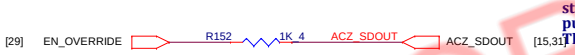
[3,5,11,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V

Functional Strap Definitions

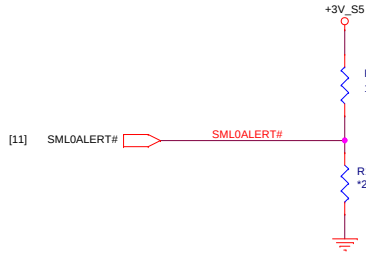
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



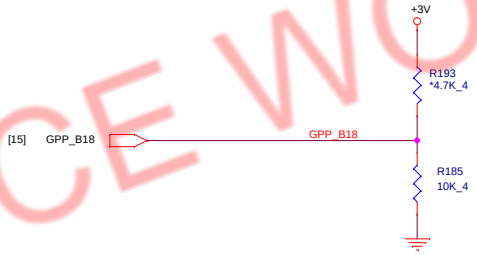
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
This function is useful when running ITP/XDP.



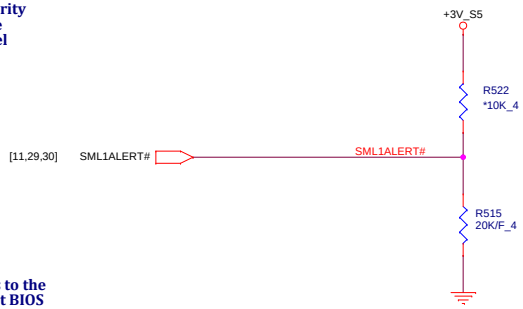
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system reboot feature).
This function is useful when running ITP/XDP.

No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC

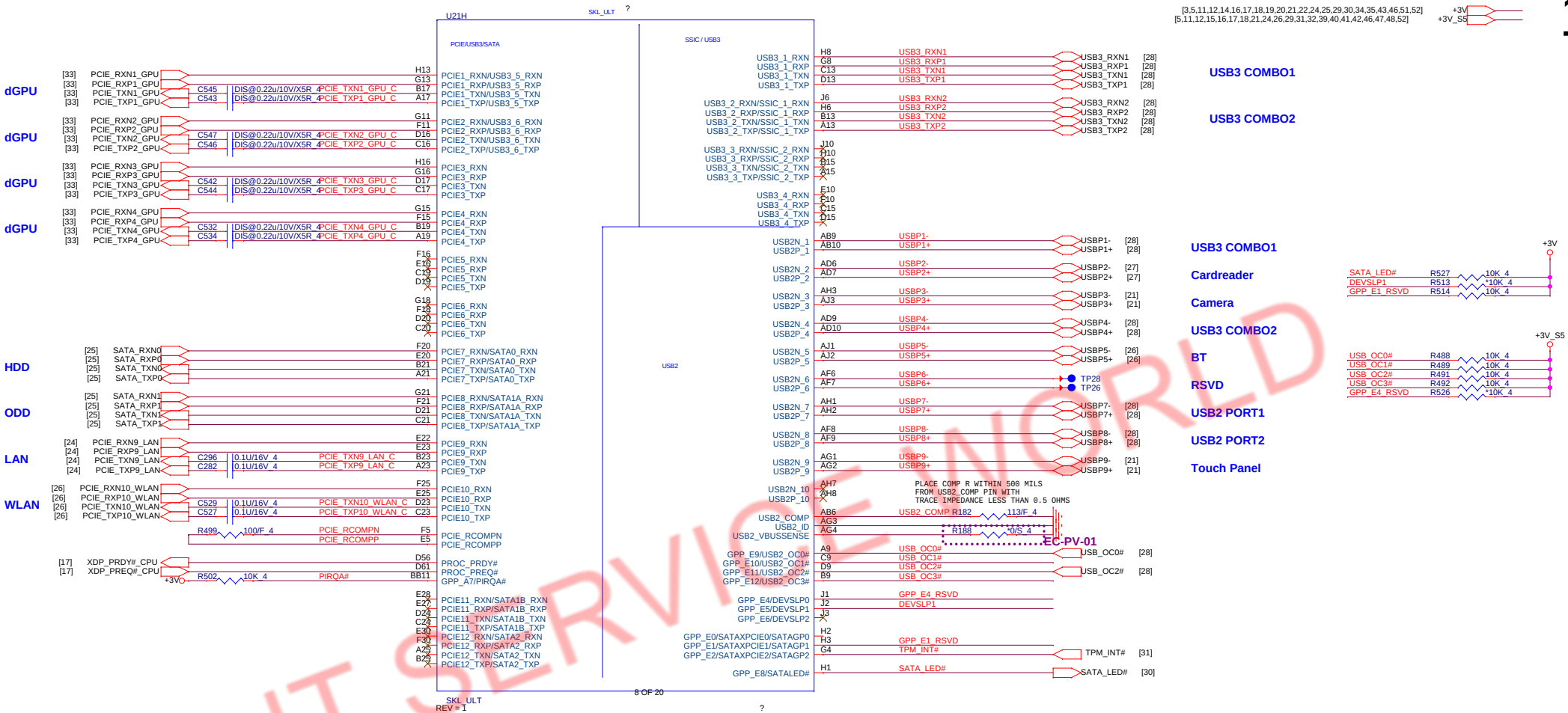


No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU Strap	1A

Date: Wednesday, March 09, 2016 Sheet 12 of 58



PCI-E Port Mapping Table

PCI-E	Function	CLK REQ	Function
PORT-1	dGPU	PORT-0	dGPU
PORT-2	dGPU	PORT-1	
PORT-3	dGPU	PORT-2	WLAN
PORT-4	dGPU	PORT-3	LAN
PORT-5		PORT-4	
PORT-6		PORT-5	
PORT-7	HDD		
PORT-8	ODD		
PORT-9	LAN		
PORT-10	WLAN		
PORT-11			
PORT-12			

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3 COMBO1
PORT-2	USB3 COMBO2
PORT-3	NC
PORT-4	NC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB3 COMBO1
PORT-2	Cardreader
PORT-3	Camera
PORT-4	USB3 COMBO2
PORT-5	BT
PORT-6	NC
PORT-7	USB2 PORT1
PORT-8	USB2 PORT2
PORT-9	Touch Panel
PORT-10	NC

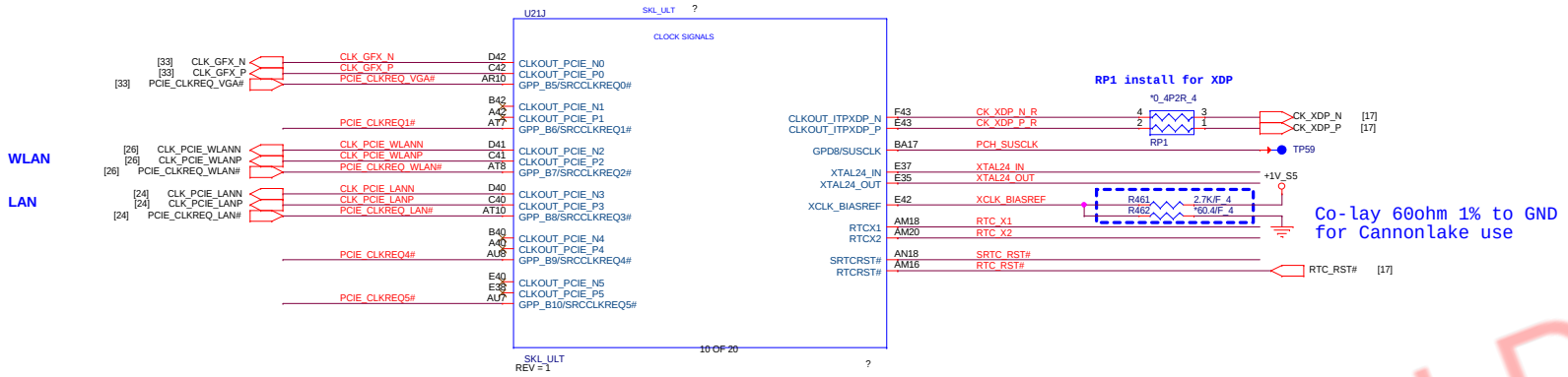
Quanta Computer Inc.

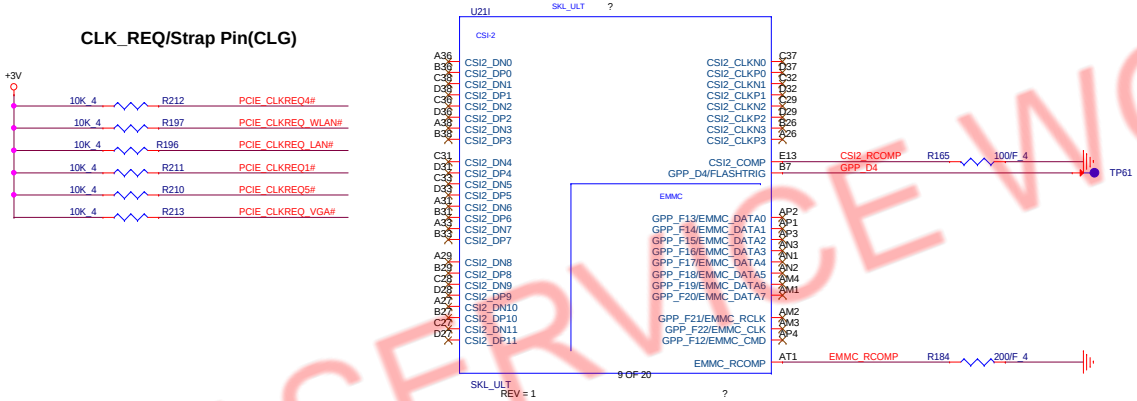
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU PCIE/USB/SATA	1A

Date: Wednesday, March 09, 2016 Sheet 13 of 58

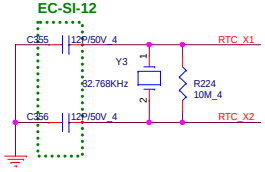
[5,16] +3V_RTC_2
[3,5,11,12,13,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[10,16,17,41,46,48] +1V_S5





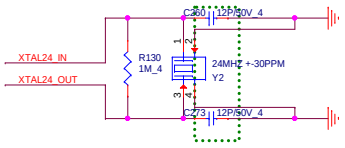
RTC Clock 32.768KHz

EC-SI-12



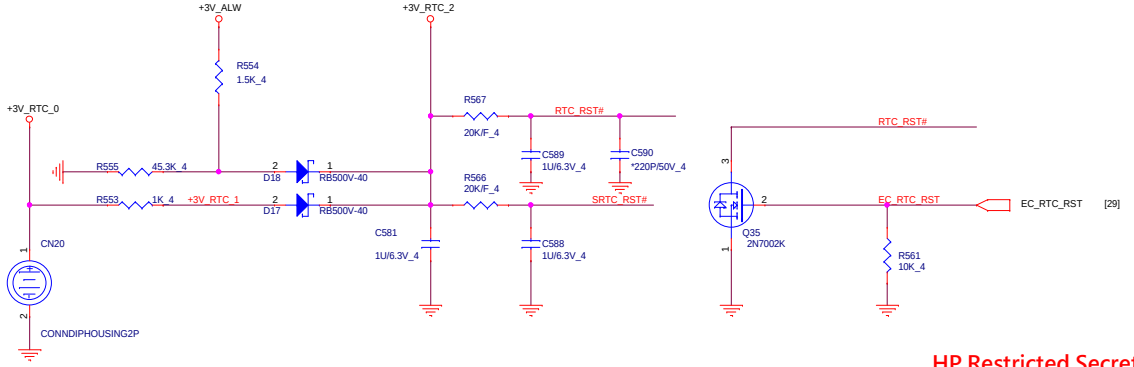
External Crystal

EC-SI-12



RTC Circuitry(RTC)

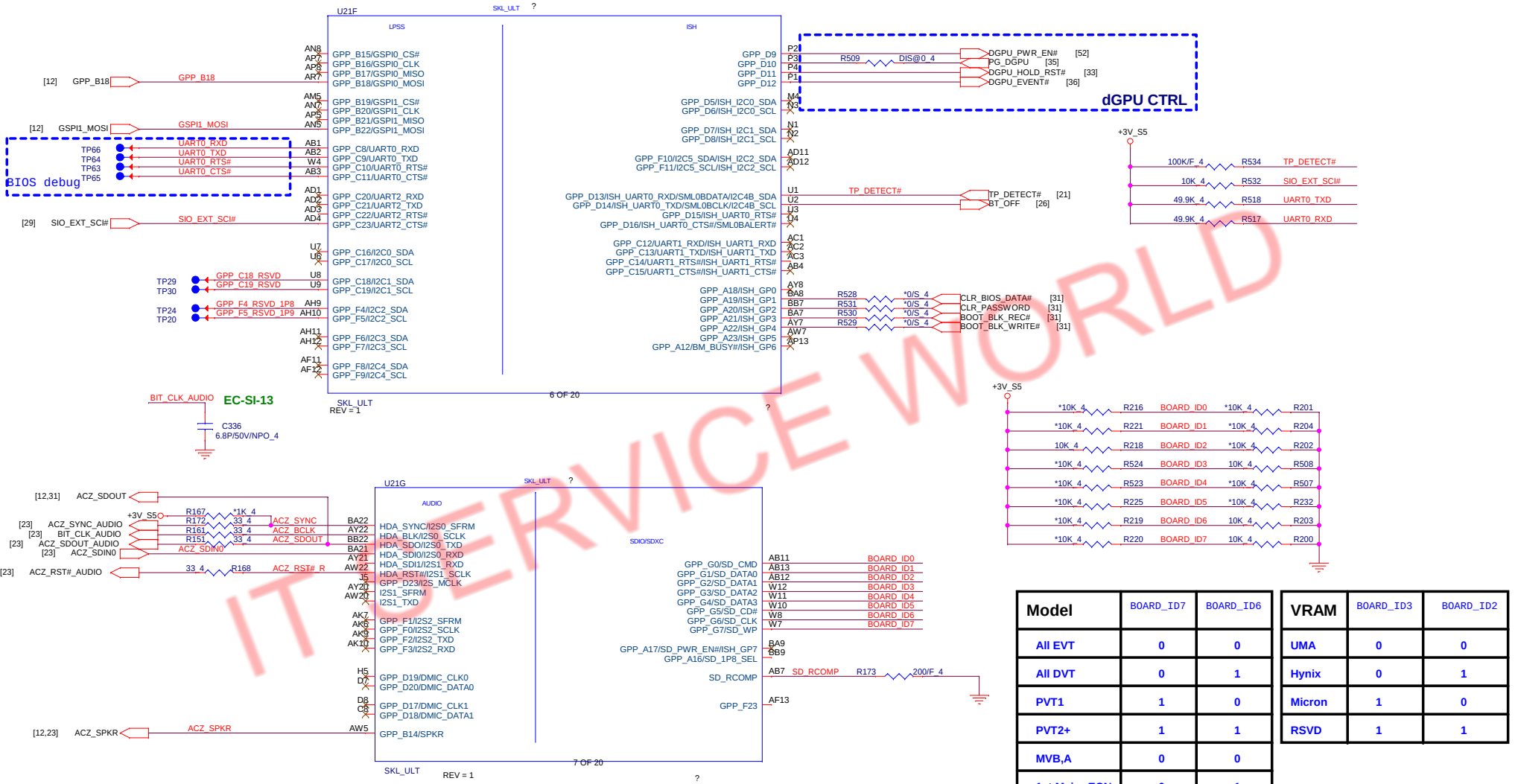
RTC Power trace width 20mils.



HP Restricted Secret

Quanta Computer Inc.		
PROJECT: HP-Hawaii		
Size: Custom	Document Number: SKL CPU CLK/eMMC	Rev: 1A
Date: Tuesday, March 15, 2016	Sheet 14 of 58	

[5,11,12,13,16,17,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52]
[3,5,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52]
+3V_S5
+3V



Model	BOARD_ID7	BOARD_ID6
All EVT	0	0
All DVT	0	1
PVT1	1	0
PVT2+	1	1
MVB,A	0	0
1st Major ECN	0	1
2nd Major ECN	1	0
3rd Major ECN	1	1

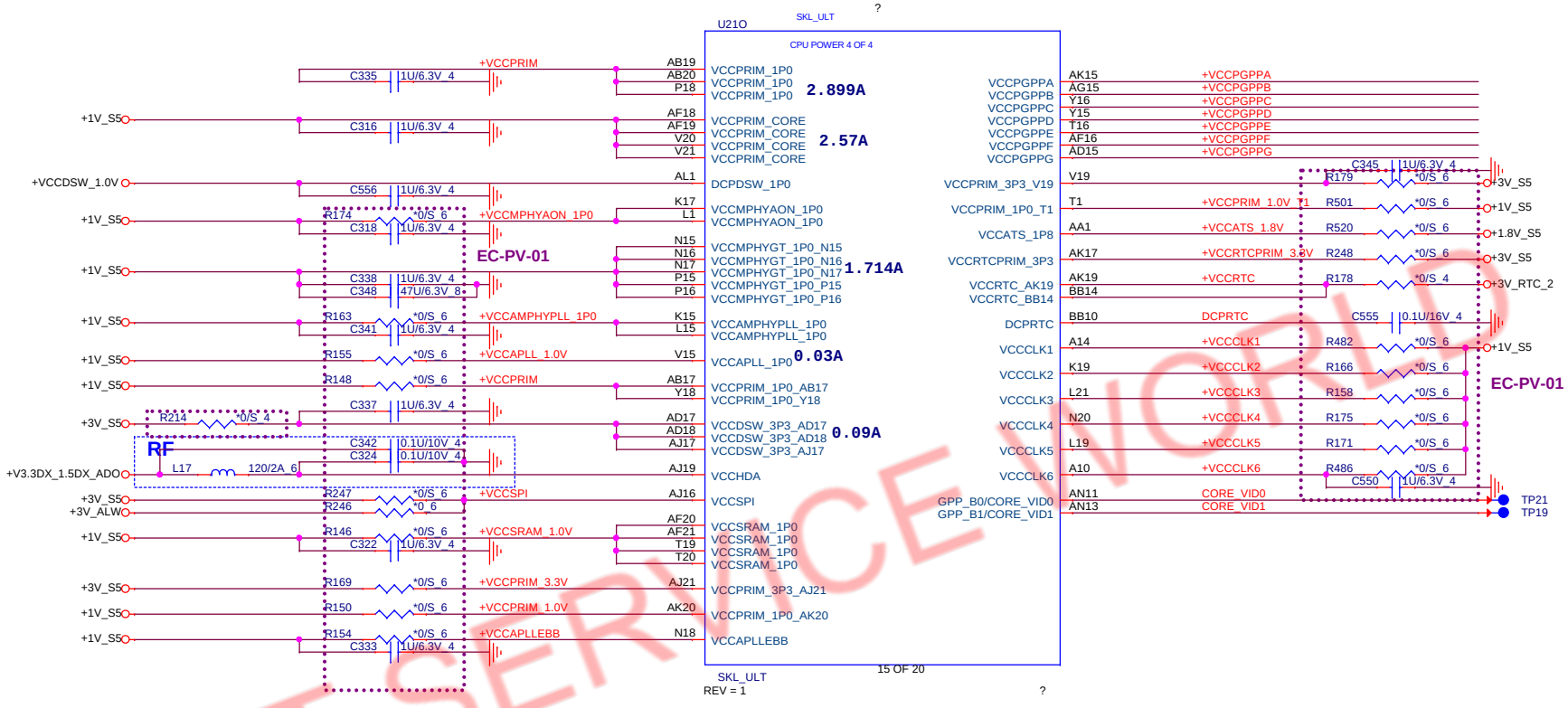
VRAM	BOARD_ID3	BOARD_ID2
UMA	0	0
Hynix	0	1
Micron	1	0
RSVD	1	1

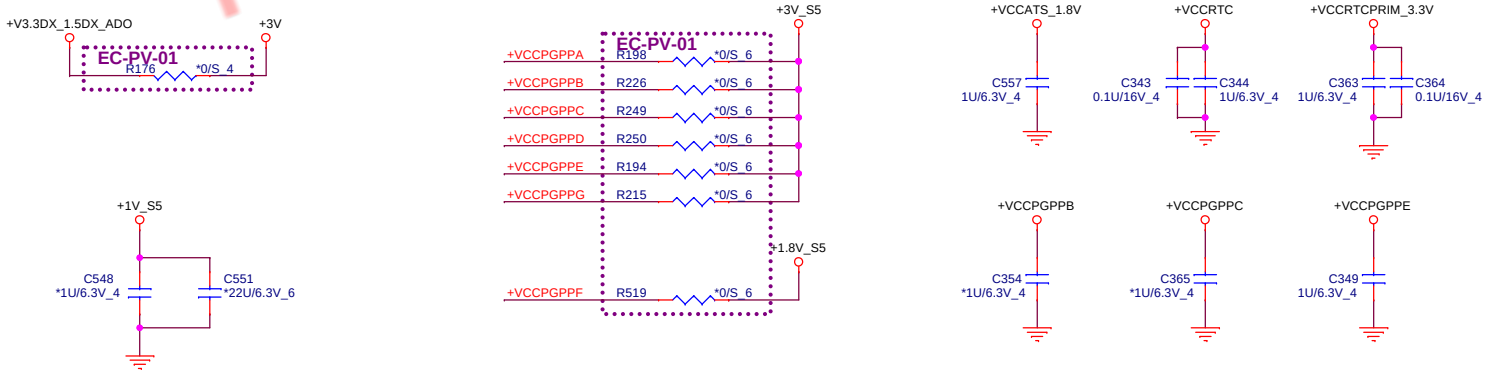
Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU HDA/GPIO	1A

Date: Thursday, March 10, 2016 Sheet 15 of 58

[10,14,17,41,46,48] +1V_S5
[10,29,42,46,48] +1.8V_S5
[5,11,12,13,15,17,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52] +3V_S5
[5,14] +3V_RTC_2
[3,5,11,12,13,14,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V





HP Restricted Secret

Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU Power (PCH)	1A

Date: Wednesday, March 09, 2016 Sheet 16 of 58

[3,5,11,12,13,14,16,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[10,14,16,41,46,48] +1V_S5
[3,5,7,46,48] +VCCIO
[5,11,12,13,15,16,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52] +3V_S5

CPU XDP

CN1

*Samtec BSH-030-01

EC-PV-01

APS

CN2

*50501-0180N-001

U19

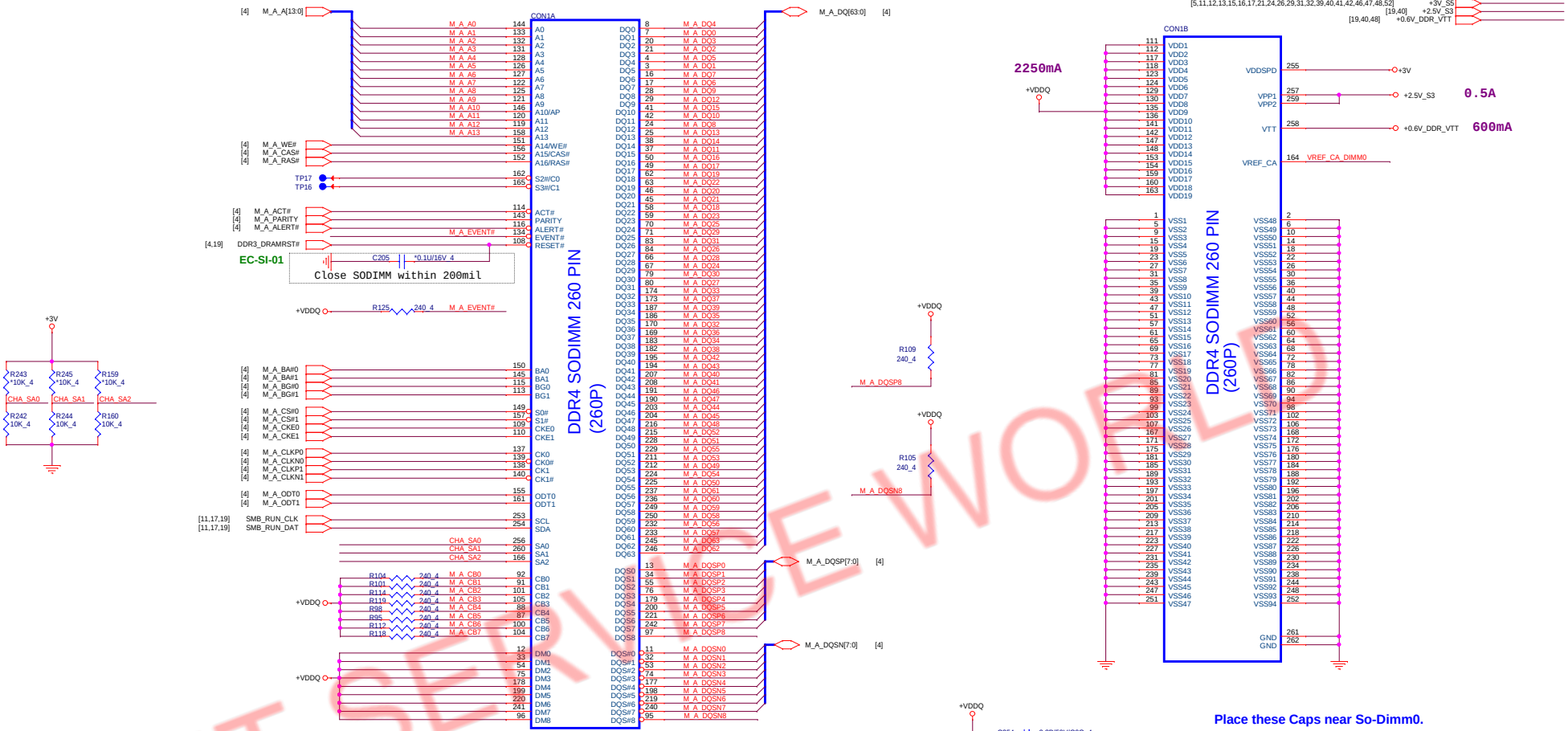
*SN74CBTLV3126RGYR

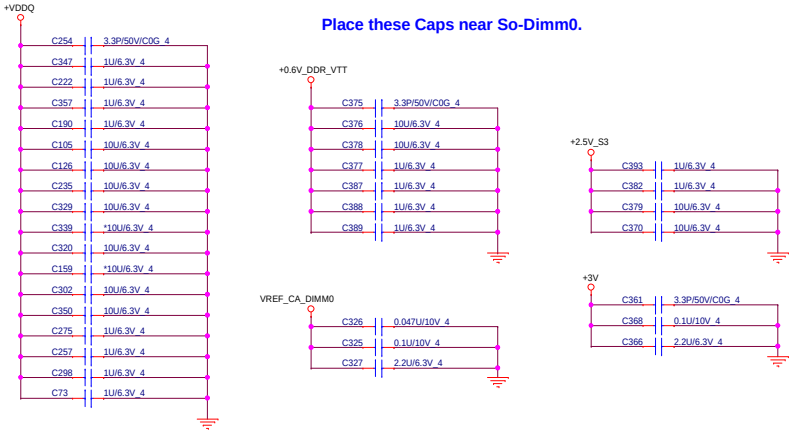
Quanta Computer Inc.

PROJECT: HP-Hawaii

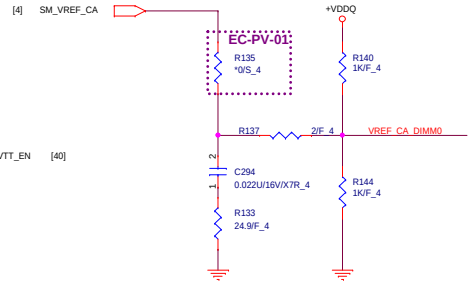
Size	Document Number	Rev
Custom	SKL CPU XDP/APS	1A

Date: Wednesday, March 09, 2016 Sheet 17 of 58

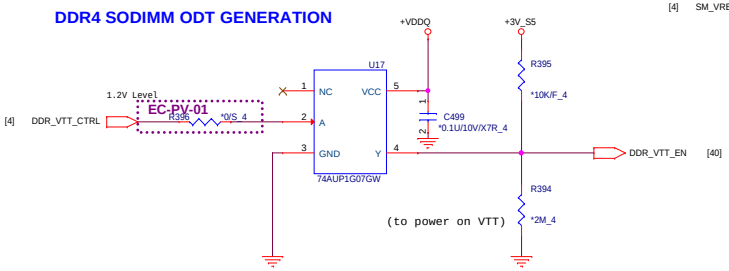




VREF CA DIMM0 Solution



DDR4 SODIMM ODT GENERATION

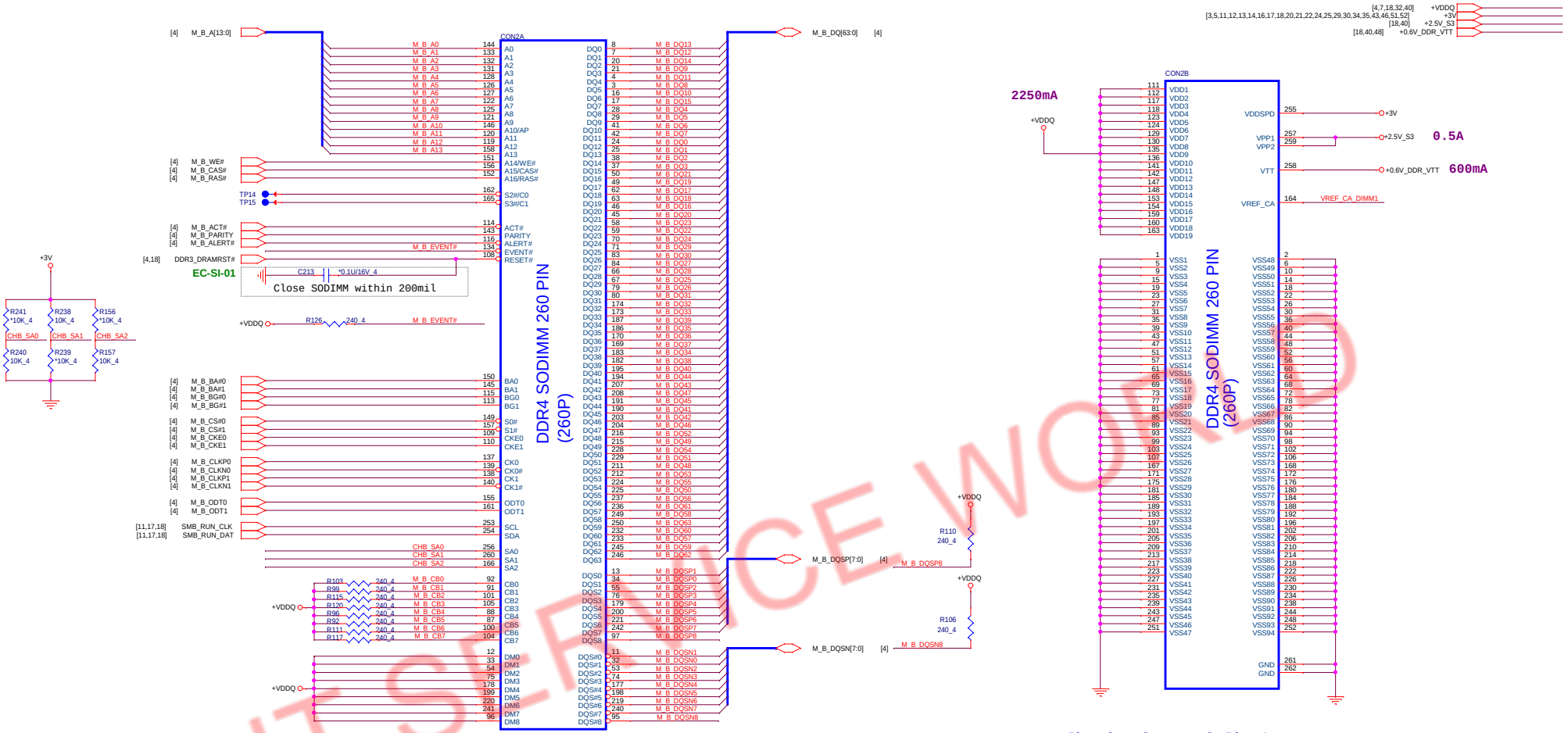


Quanta Computer Inc.

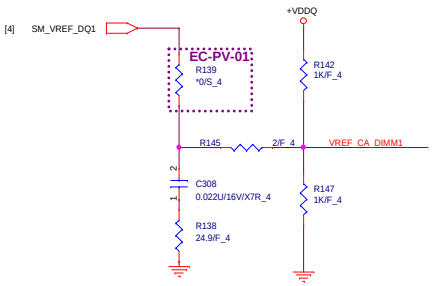
PROJECT: HP-Hawaii

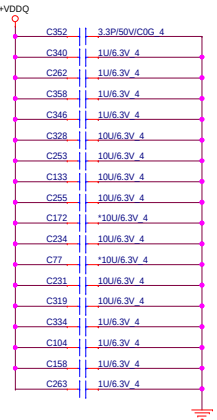
Size	Document Number	Rev
Custom	DDR4 SODIMM H=8	1A

Date: Tuesday, February 02, 2016 Sheet 18 of 58

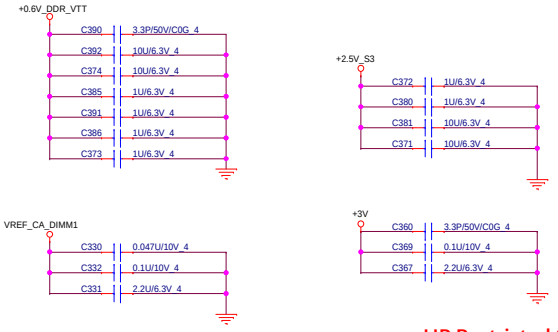


VREF CA DIMM1 Solution





Place these Caps near So-Dimm1



HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	DDR4 SODIMM H=4	1A

Date: Thursday, January 28, 2016 Sheet 19 of 58

eDP to LVDS (RTD2136N-CG)

[3,5,11,12,13,14,16,17,18,19,21,22,24,25,29,30,34,35,43,46,51,52] +3V

Trace width of DVCC33 >40mils

+3V — L13 PBY160808T-600Y-N — DVCC33
C25 10U/6.3V/X5R_6
C18 0.1U/10V/X5R_4

+3V — L14 PBY160808T-600Y-N — AVCC33
C38 10U/6.3V/X5R_6
C33 0.1U/10V/X5R_4
C32 0.1U/10V/X5R_4 CLOSE to PIN5

SWR_V12
C23 0.1U/10V/X5R_4 CLOSE to PIN43

DP input signals

[3] EDP_HPD — R26 1K/F_4
R31 *100K/F_4
eDP_HPD with pull down 100K-ohm on PCH side.

[3] INT_EDP_AUXN — C473 0.1U/10V/X5R_4
[3] INT_EDP_AUXP — C472 0.1U/10V/X5R_4

[3] INT_EDP_TXP0 — C471 0.1U/10V/X5R_4
[3] INT_EDP_TXN0 — C470 0.1U/10V/X5R_4
[3] INT_EDP_TXP1 — C469 0.1U/10V/X5R_4
[3] INT_EDP_TXN1 — C468 0.1U/10V/X5R_4

C31 0.1U/10V/X5R_4
R387 12K/F_6
CLOSE to PIN11

U15 RTD2136N-CG(QFN)

RTD2136N

2136_BKLT_EN
EDID_DAT
EDID_CLK
SDA
SCL
eDP_HPD_R
TEST_MODE
2136_AUXN
2136_AUXP
AVCC33
DPD_TXP0_C
DPD_TXN0_C
DPD_TXP1_C
DPD_TXN1_C
SWR_V12
DP_REXT

ODD_CH
LVDS_TX_ON0 [21]
LVDS_TX_OP0 [21]
LVDS_TX_ON1 [21]
LVDS_TX_OP1 [21]
LVDS_TX_ON2 [21]
LVDS_TX_OP2 [21]
LVDS_TXCLK_ON [21]
LVDS_TXCLK_OP [21]
LVDS_TX_ON3 [21]
LVDS_TX_OP3 [21]

EVEN_CH
LVDS_TX_EN0 [21]
LVDS_TX_EP0 [21]
LVDS_TX_EN1 [21]
LVDS_TX_EP1 [21]
LVDS_TX_EN2 [21]
LVDS_TX_EP2 [21]
LVDS_TXCLK_EN [21]
LVDS_TXCLK_EP [21]
LVDS_TX_EN3 [21]
LVDS_TX_EP3 [21]

ISP_SCL
ISP_SDA
SWR_V12
PCH_DPST_PWM
2136_LVDS_PWREN
2136_VADJ

Trace width of SWR_V12 and SWR_LX >60mils
L9/C536/C113 close to Pin17 within 200mils
SWR_V12 — L12 *0/S_8_SWR_LX
C27 0.1U/10V/X5R_4
C29 22U/6.3V/X5R_6

Trace width of DVCC33 >40mils
DVCC33
C21 0.1U/10V/X5R_4
C14 22U/6.3V/X5R_6

C5023/C5024 close to Pin18 within 200mils

DVCC33
C22 0.1U/10V/X5R_4
CLOSE to PIN22

SWR MODE /LDO MODE

	4.7-uH	0 Olm
SWR_182mW	Connect	NC
LDO_357mW	NC	Connect

GPIO & TESTing signals

[50] 2136_VADJ
[21] 2136_LVDS_PWREN
[21] 2136_BKLT_EN
[3] PCH_DPST_PWM
TEST_MODE
2136_VADJ
2136_LVDS_PWREN
2136_BKLT_EN
PCH_DPST_PWM
R386 100K/F_4
R365 100K/F_4
2136_VADJ
C465 100P/50V/NPO_4
R368 100K/F_4

In System Programing

slave address=0xA8

DVCC33 DVCC33
R381 4.7K/F_4
R373 4.7K/F_4
[29] LVDS_SCL — R379 *0/S_4 — ISP_SCL
[29] LVDS_SDA — R372 *0/S_4 — ISP_SDA
EC-PV-01

RTD2136N: Mode Selestion		MODE_CFG0 (PIN47)	
		0	1
MODE_CFG1(PIN48)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

Program EEPROM (F/W.EDID)

slave address=0xA8

DVCC33 DVCC33
R384 *4.7K/F_4
R385 4.7K/F_4
SCL
SDA
MODE_CFG1(PIN48) MODE_CFG0 (PIN47)

DVCC33
C475 *0.1U/10V/X5R_4
Pin_45 EDID_DAT — R371 *0/S_4 — FW_ROM_SDA
Pin_46 EDID_CLK — R378 *0/S_4 — FW_ROM_SCL
EC-PV-01
U16 *M24C64
VCC WP SDA A2 SCL A1 GND A0

The Program EEPROM must be 2 byte addressing device

DDC

DVCC33 DVCC33
R377 4.7K/F_4
R370 *4.7K/F_4
Pin_46
EDID_CLK
EDID_DAT
Pin_45
SCL
R376 *4.7K/F_4
R369 4.7K/F_4
R383 4.7K/F_4

Reserve pull down for EPMODE

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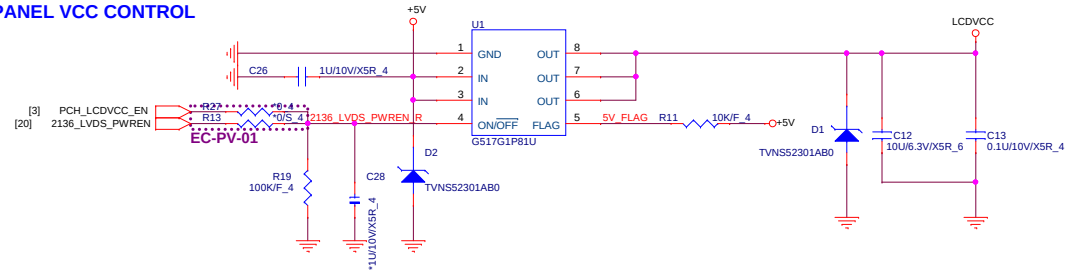
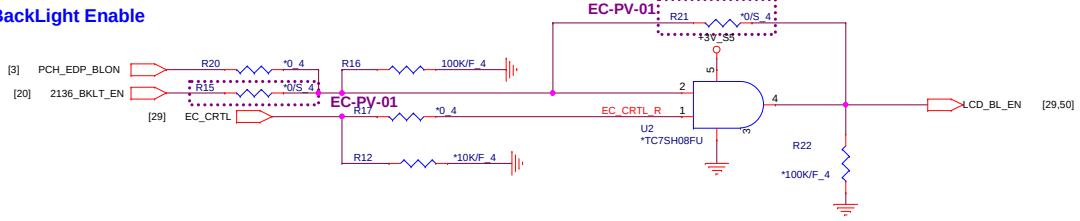
Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	eDP to LVDS converter	1A
Date: Thursday, January 28, 2016	Sheet 20 of 58	

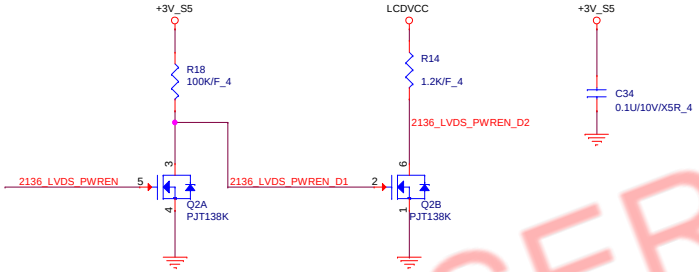
PANEL VCC CONTROL



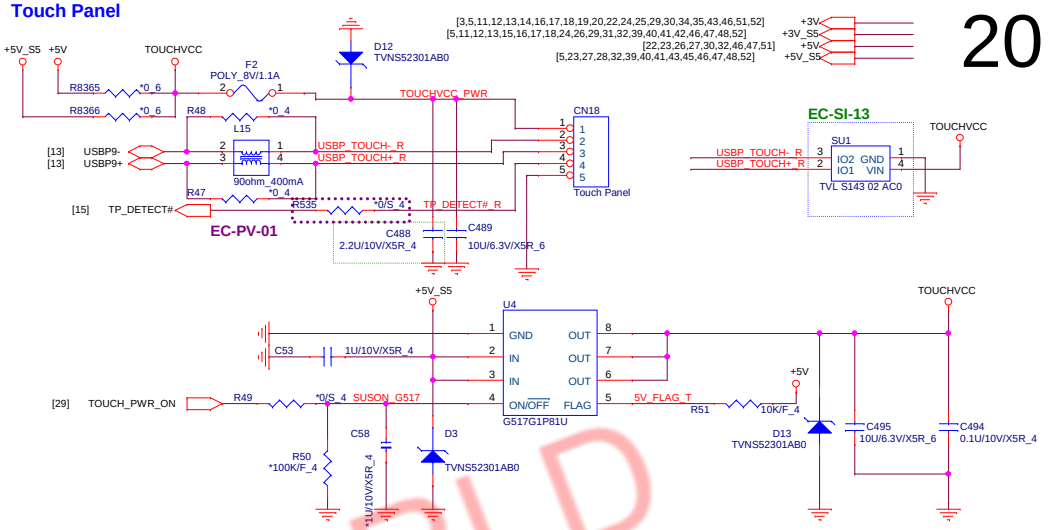
BackLight Enable



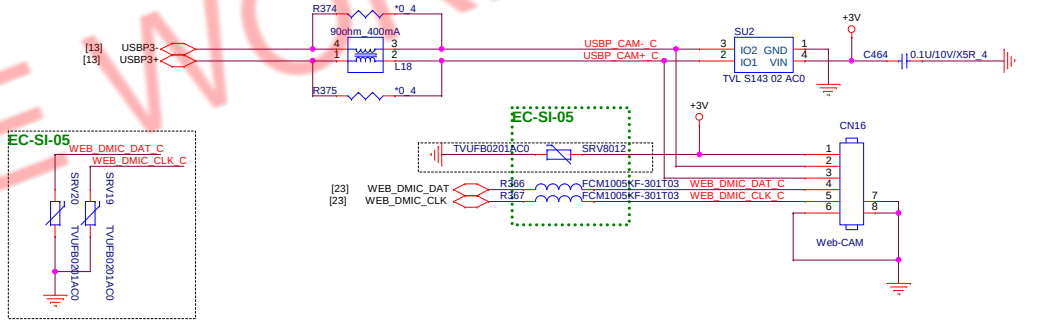
LCDVCC Discharge Circuit

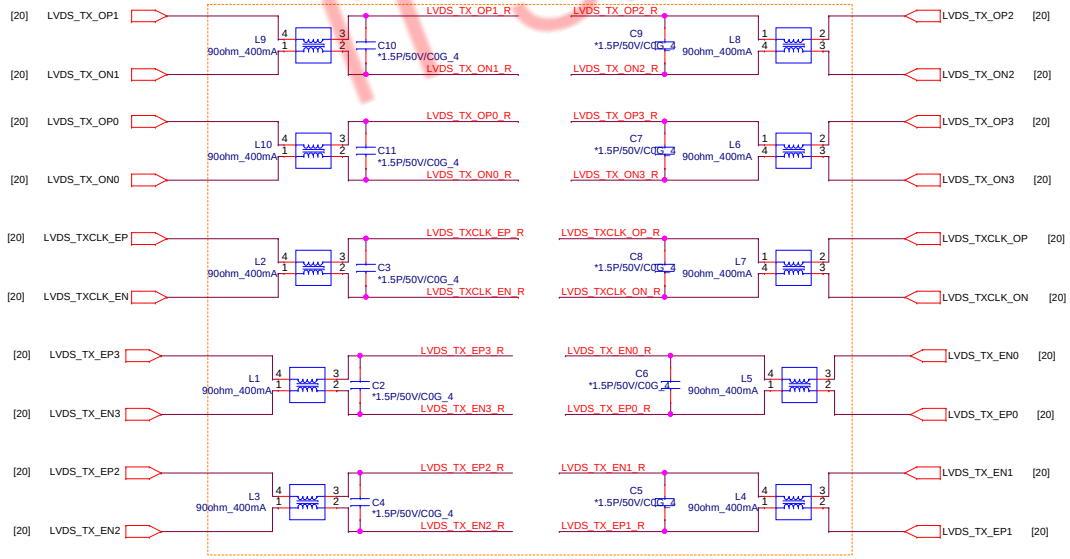


Touch Panel

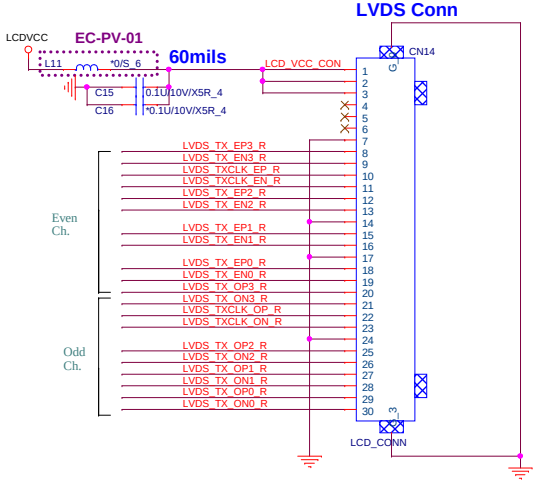


CCD CONN





LVDS Conn



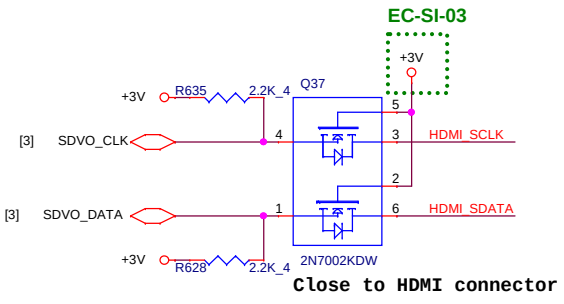
Quanta Computer Inc.
PROJECT: HP-Hawaii

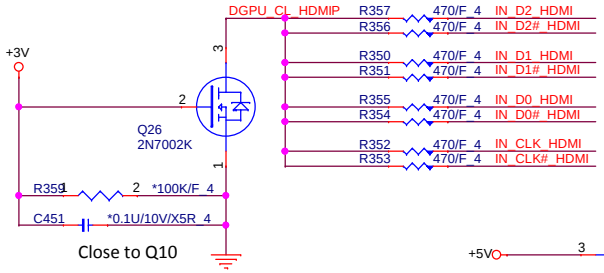
Size	Document Number	Rev
Custom	LVDS CONN/DDC/Touch Panel	1A
Date: Thursday, March 17, 2016	Sheet 21 of 58	

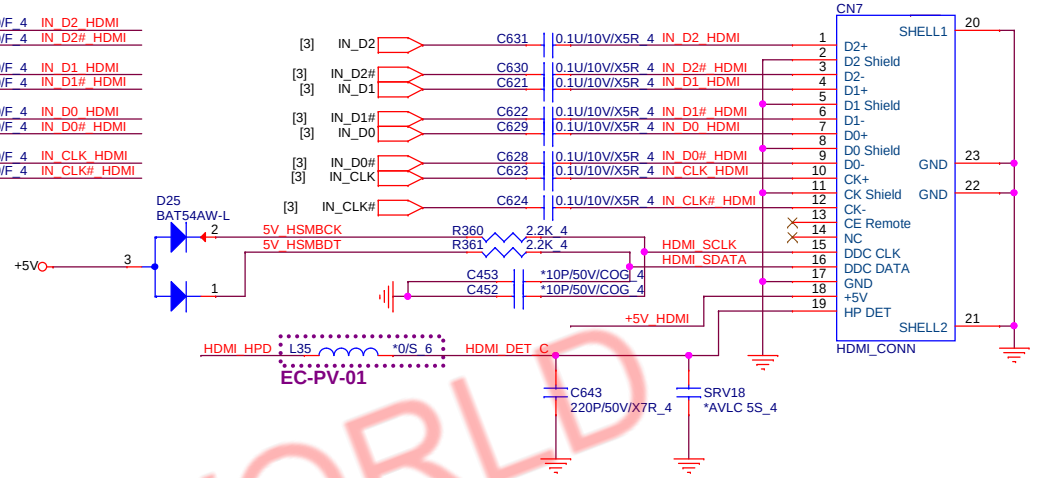
HDMI CONN

[3,5,11,12,13,14,16,17,18,19,20,21,24,25,29,30,34,35,43,46,51,52]
[21,23,26,27,30,32,46,47,51]
+3V
+5V

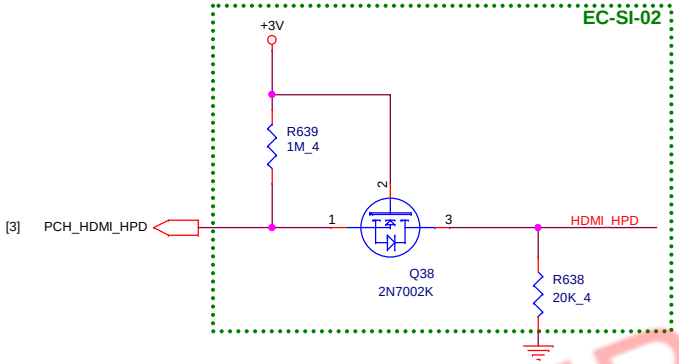
EC-SI-03



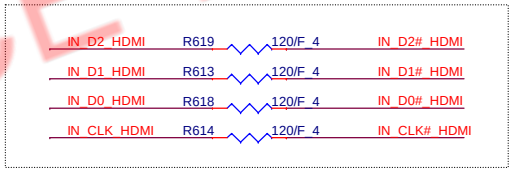


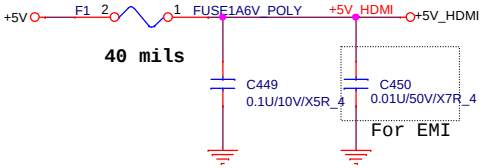


EC-SI-02

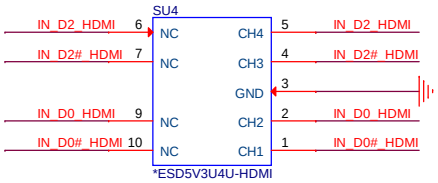


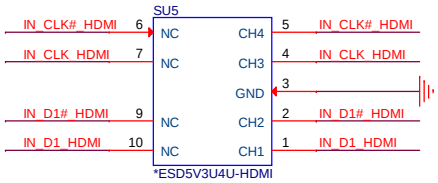
For EMI

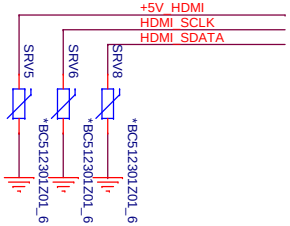




For ESD







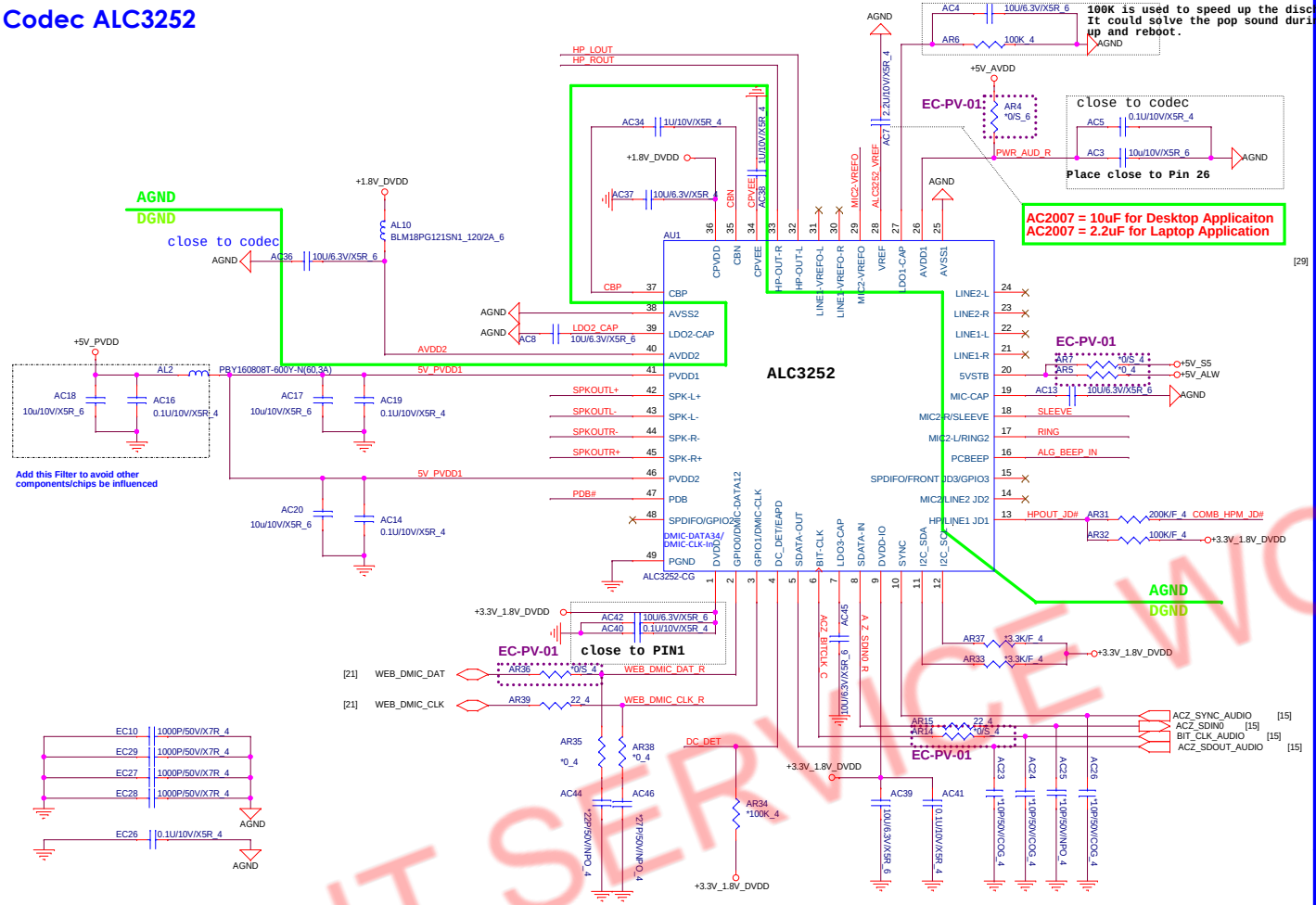
Layout note:Place close to HDMI Conn

HP Restricted Secret

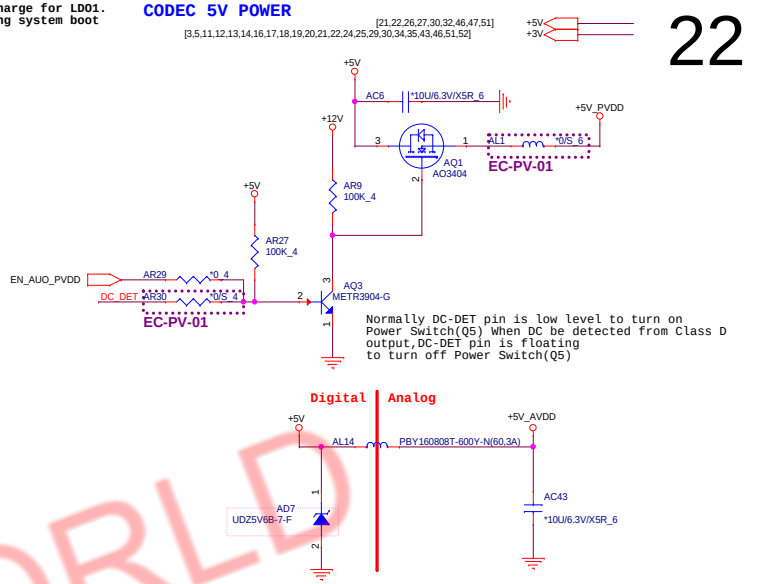
Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	HDMI	1A
Date: Monday, February 15, 2016	Sheet 22 of 58	

Codec ALC3252

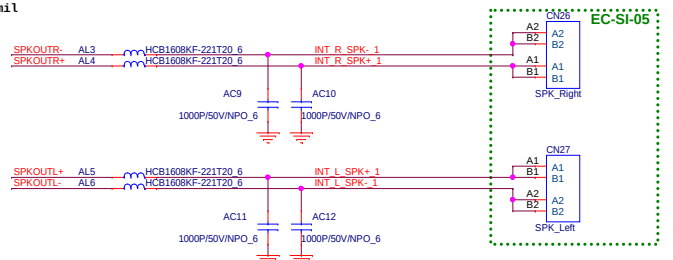


CODEC 5V POWER

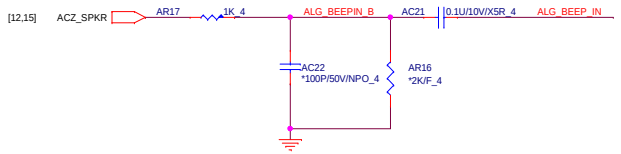


Internal Speaker (2W, 4 ohm)

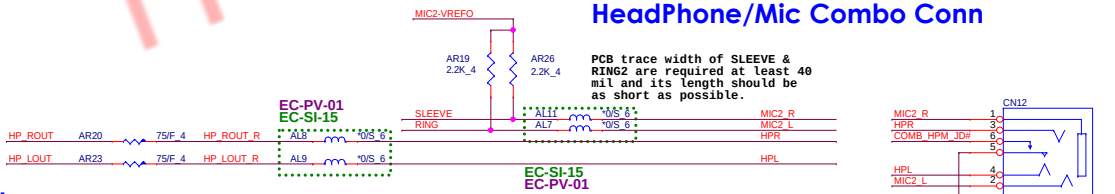
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
4 ohm : 40mil
8 ohm : 20mil



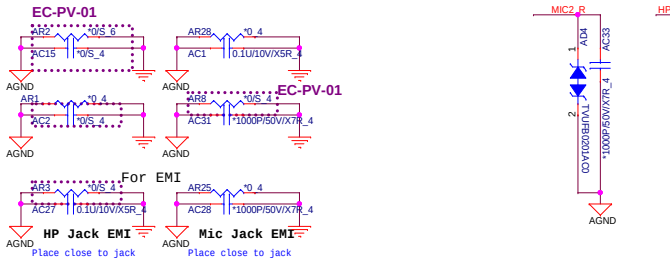
PC BEEP

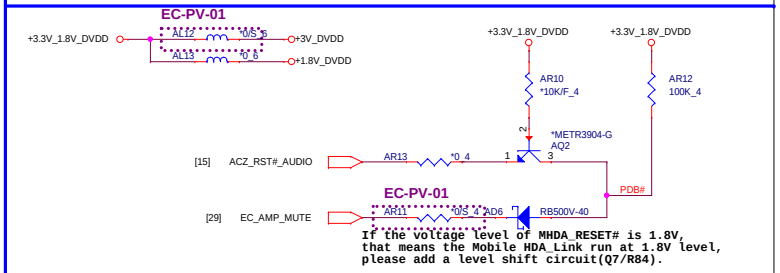


HeadPhone/Mic Combo Conn



CODEC Return Path





HP Restricted Secret

Quanta Computer Inc.
PROJECT: HP-Hawaii
Size: Custom | Document Number: Audio CODEC | Rev: 1A
Date: Tuesday, March 22, 2016 | Sheet 23 of 58

R2248 value should be 2.49K (1%) for all application.

RTL8161GSH-CG

3V_LAN

EC-PV-01

EVDD10/AVDD33_REG trace width >40mils

Close to Pin32

Close to Pin11

Close to Pin23

EVDD10/N780946/REGOUT trace width >60mils

Close to PIN3, 8, 22, 30

C367,C368 Close to PIN22

X'tal 25MHz

LAN Conn

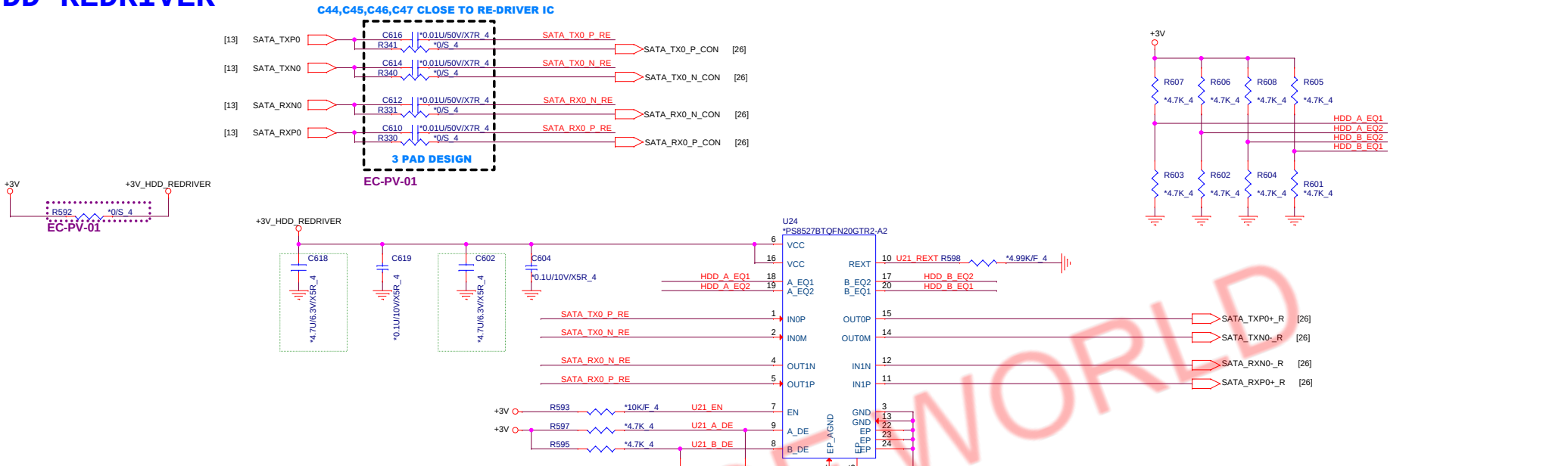
Quanta Computer Inc.

PROJECT: HP-Hawaii

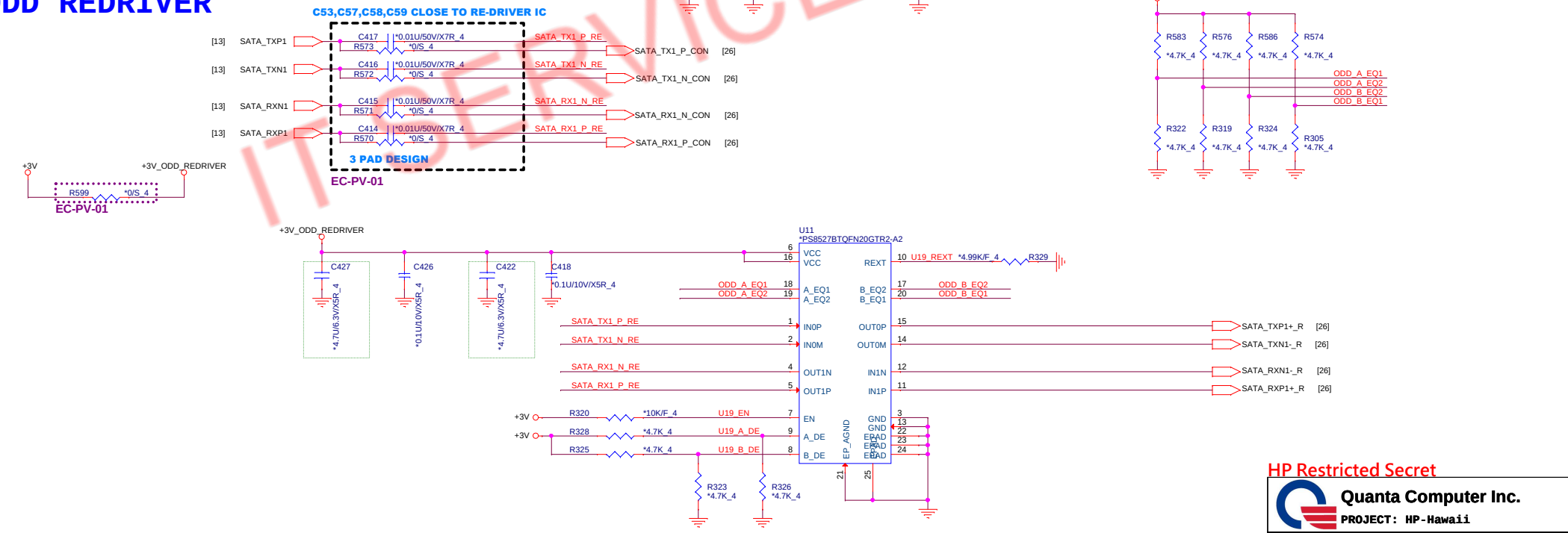
Size: Custom | Document Number: LAN/RJ45 | Rev: 1A

Date: Wednesday, March 09, 2016 | Sheet 24 of 58

HDD REDRIVER



ODD REDRIVER



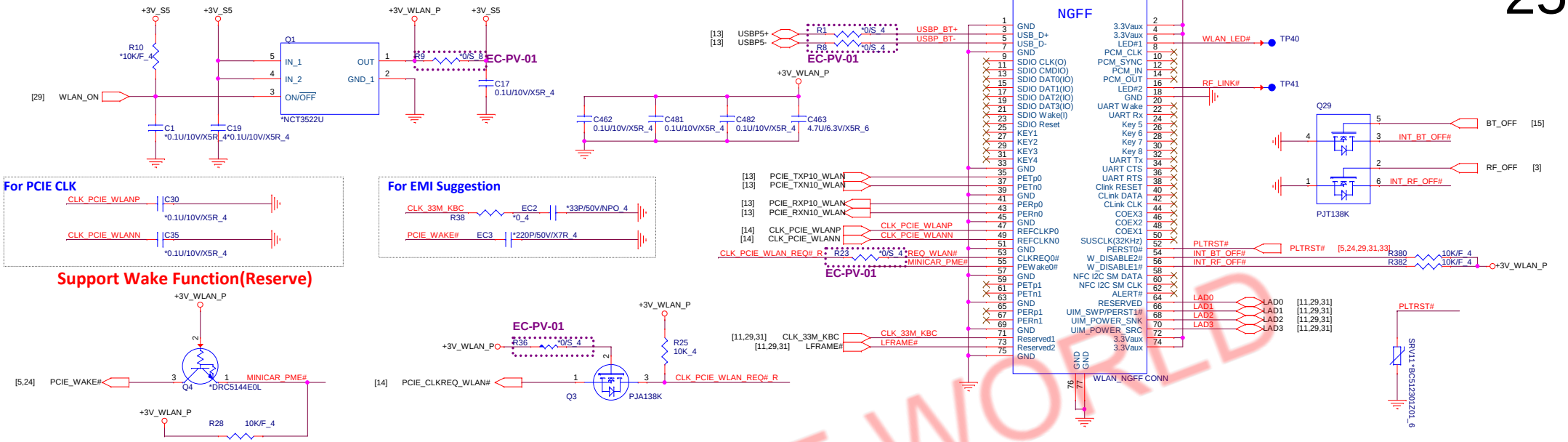
[3,5,11,12,13,14,16,17,18,19,20,21,22,24,29,30,34,35,43,46,51,52] +3V

Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SATA Re-driver	1A

Date: Wednesday, January 27, 2016 Sheet 25 of 58

Mini Card WLAN/BT(Option) PCIe M.2_power(S5)

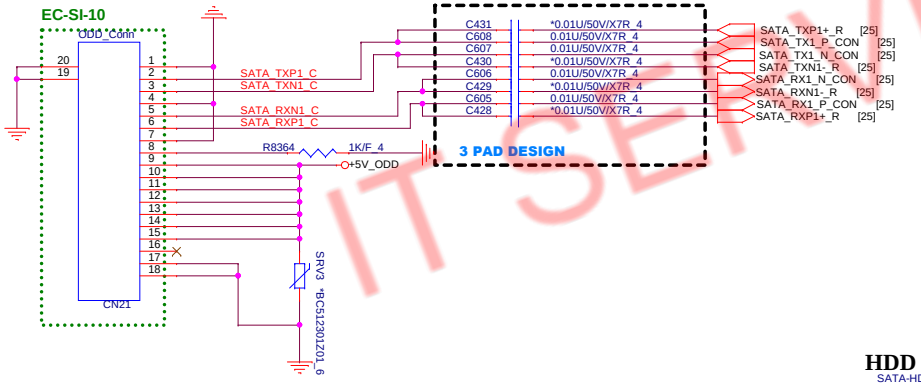


For PCIE CLK

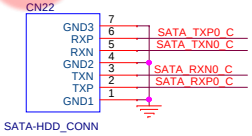
For EMI Suggestion

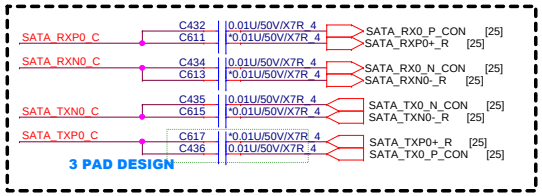
Support Wake Function(Reserve)

ODD

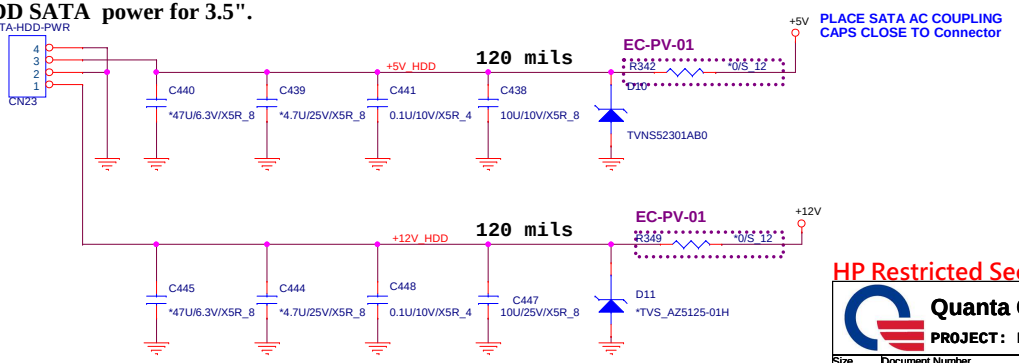


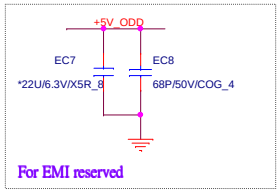
HDD SATA signal for 3.5".

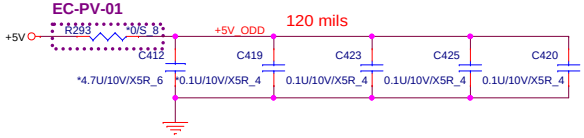




HDD SATA power for 3.5".







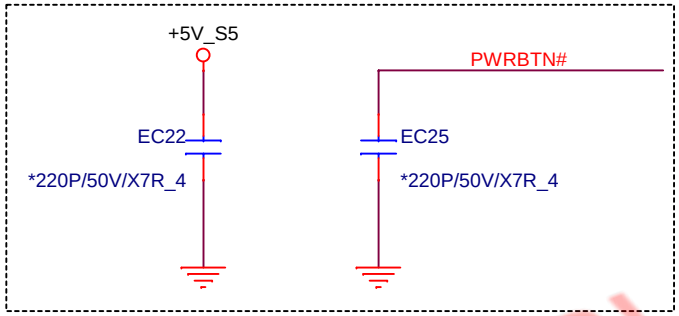
[21,22,23,27,30,32,46,47,51] +5V
[3,5,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[5,11,12,13,15,16,17,18,21,24,29,31,32,39,40,41,42,46,47,48,52] +3V_S5

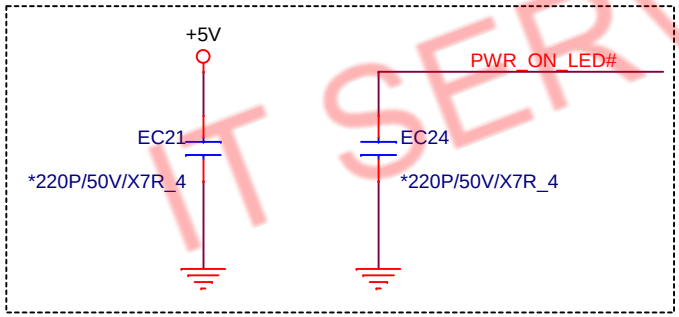
HP Restricted Secret

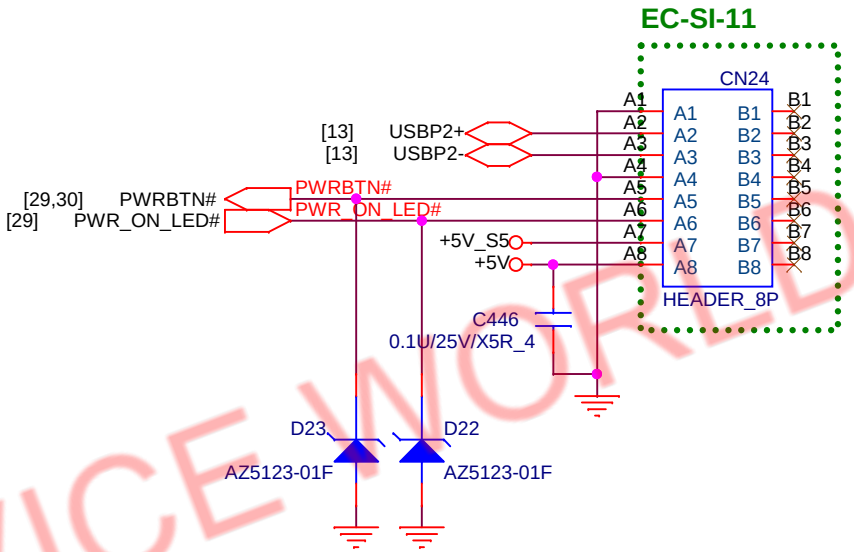
Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	WLAN/HDD/ODD	1A
Date: Tuesday, March 22, 2016	Sheet 26 of 58	

Card reader/Power button conn





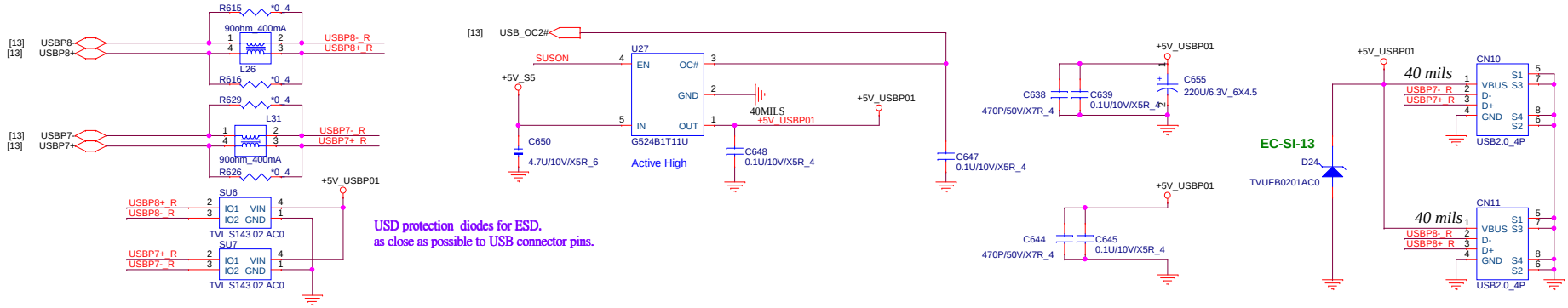


Quanta Computer Inc.

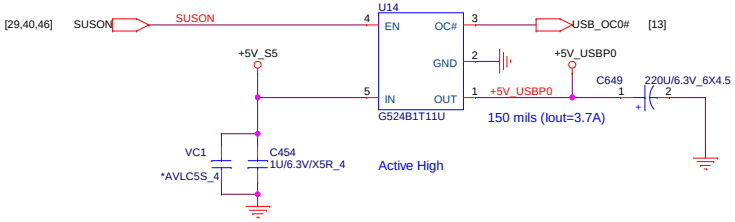
PROJECT: HP-Hawaii

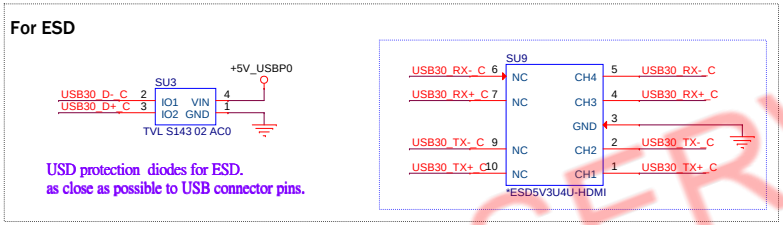
Size	Document Number	Rev
A	Card reader/PWR BTN CONN	1A
Date: Tuesday, March 08, 2016	Sheet 27 of 58	

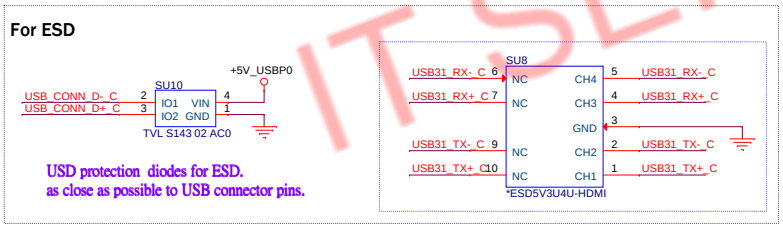
USB 2.0

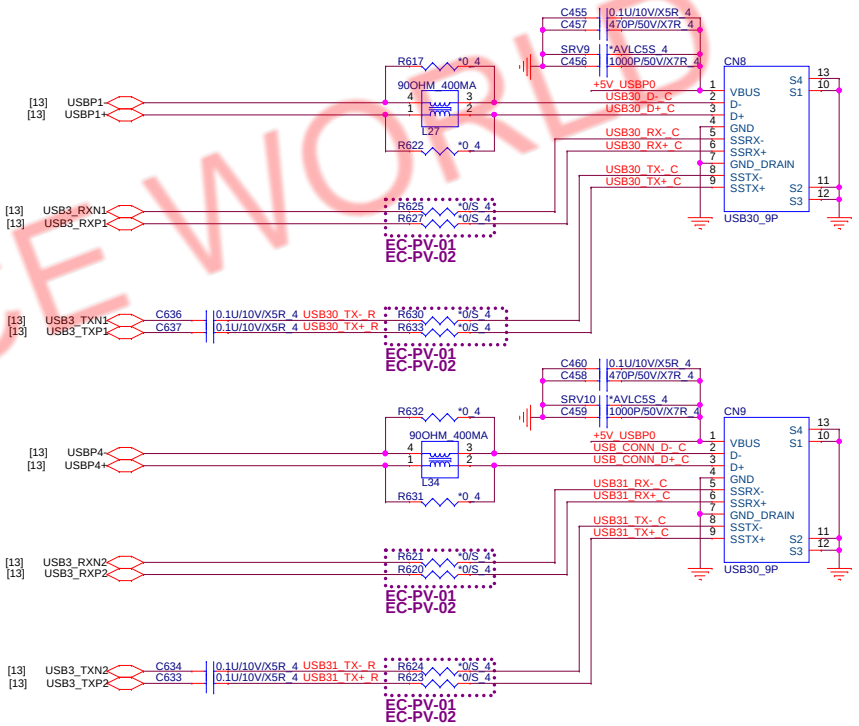


USB 2.0/3.0 Combo









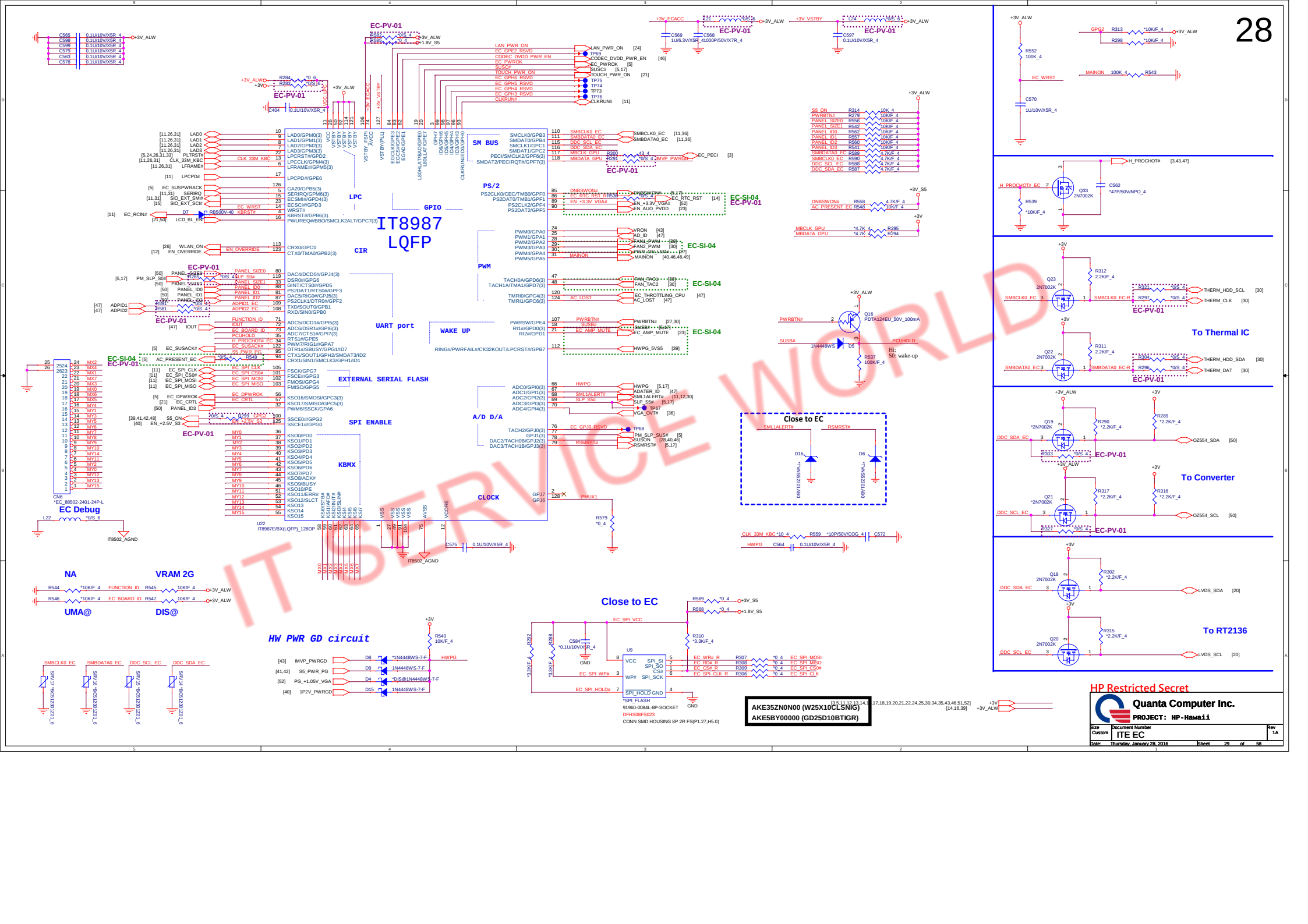
[5,21,23,27,32,39,40,41,43,45,46,47,48,52] +5V_S5

HP Restricted Secret

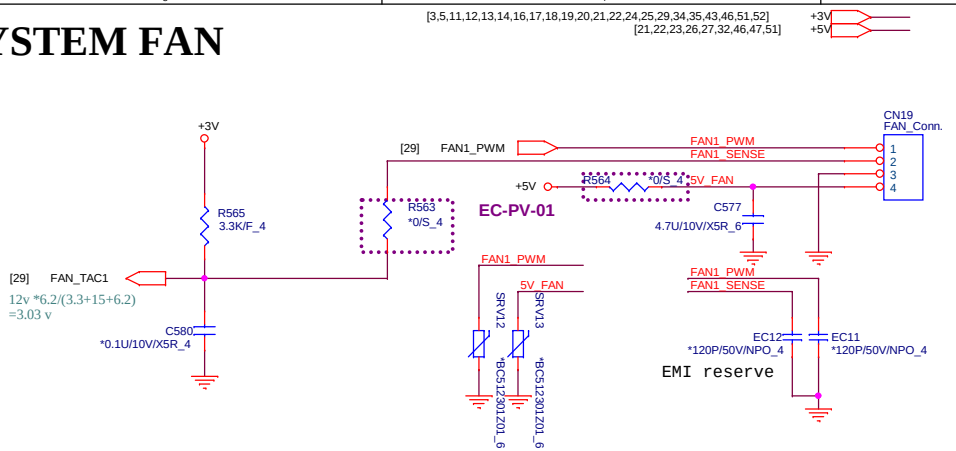
Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	USB2.0/USB3.0/Hole/EMI	1A

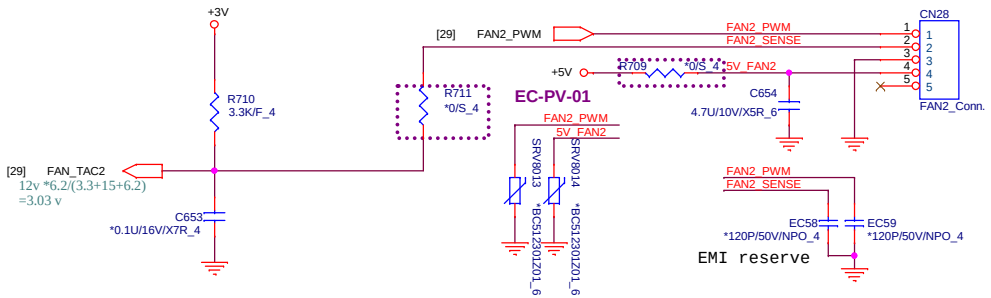
Date: Tuesday, January 26, 2016 Sheet 28 of 58


28
IT8987
LQFP
EC-PV-01
EC-SI-04
LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
A/D D/A
KBMX
CLOCK
EC Debug
Close to EC
HW PWR GD circuit
NA
VRAM 2G
UMA@
DIS@
To Thermal IC
To Converter
To RT2136
HP Restricted Secret
Quanta Computer Inc.
PROJECT: HP-Hawaii
ITE EC
Thursday, January 28, 2016
AKE35ZN00N00 (W25X10CLSNIG)
AKE5BY00000 (GD25D10BTIGR)
IT SERVICE WORLD

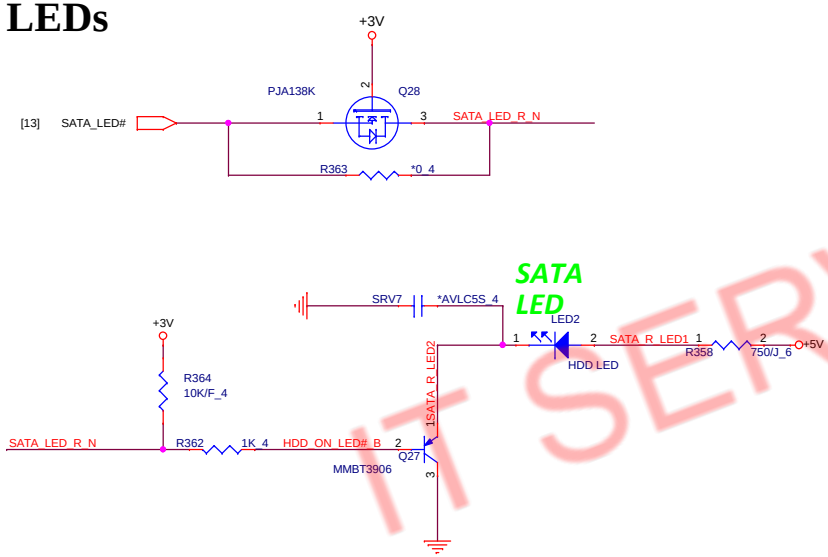
SYSTEM FAN

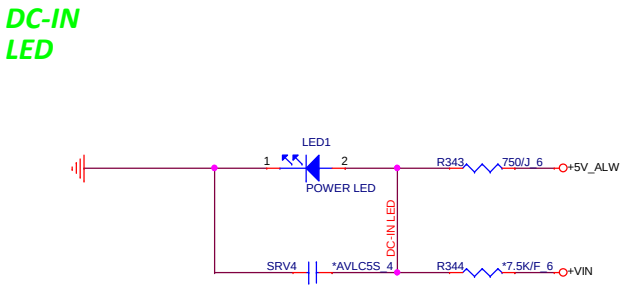


2nd SYSTEM FAN (RSVD)

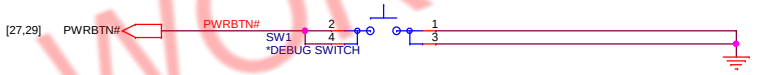


LEDs

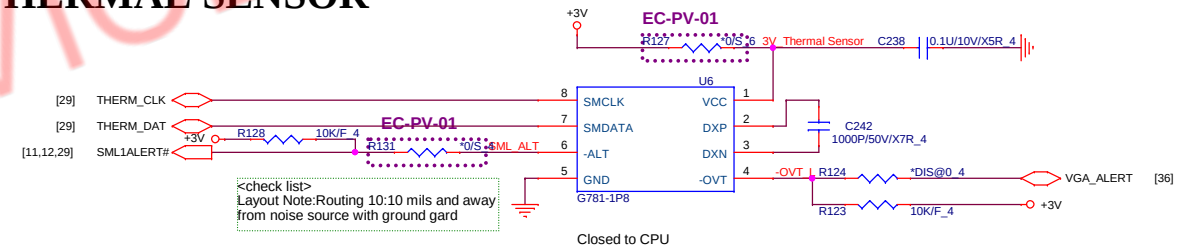




SW1 For Debug.MP will remove it.



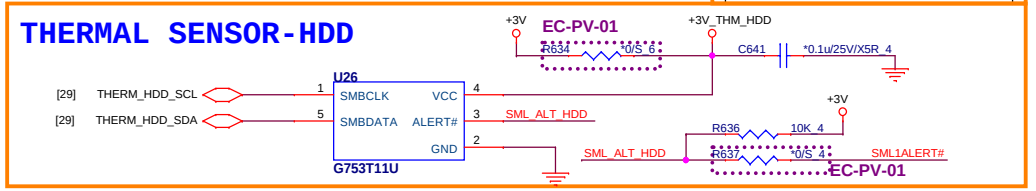
THERMAL SENSOR



THERMAL SENSOR-HDD

Ambient

Slave Adress						
A6	A5	A4	A3	A2	A1	A0
1	0	0	1	0	0	0



HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	Thermal/Fan/LED	1A

Date: Wednesday, March 09, 2016 Sheet 30 of 58

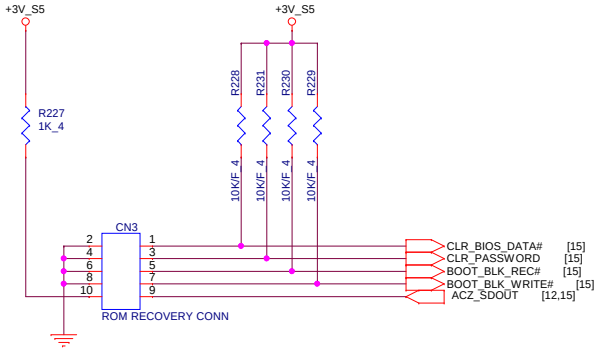
[5,11,12,13,15,16,17,18,21,24,26,29,32,39,40,41,42,46,47,48,52]
[3,5,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52]
+3V_S5
+3V

CLR_CMOS

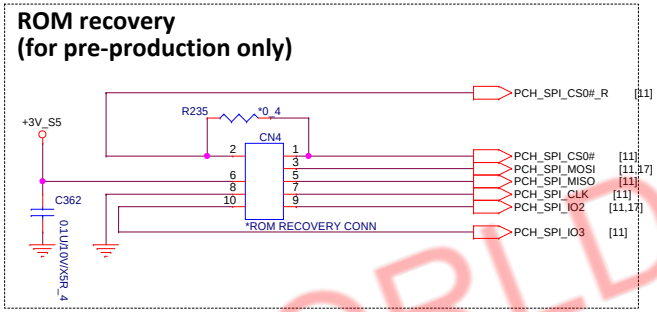
Jumper	Pre-production	Production
BOOT_BLK_Recovery	X	X
BOOT_BLK_Enable	O	X

Jumper	Type
Pop	CLR_BIOS_DAT
Pop	CLR_PASSWD
Pop	BOOT_BLK_Recovery
Pop	BOOT_BLK_Enable

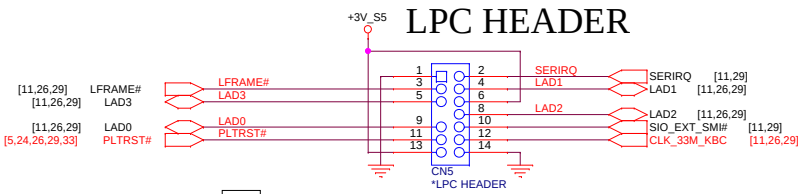
ON Chip select:Default:iinsatall (PROTO only)
CONN MINI JUMPER 2P FS (P2.0,H5.0)



ROM recovery (for pre-production only)

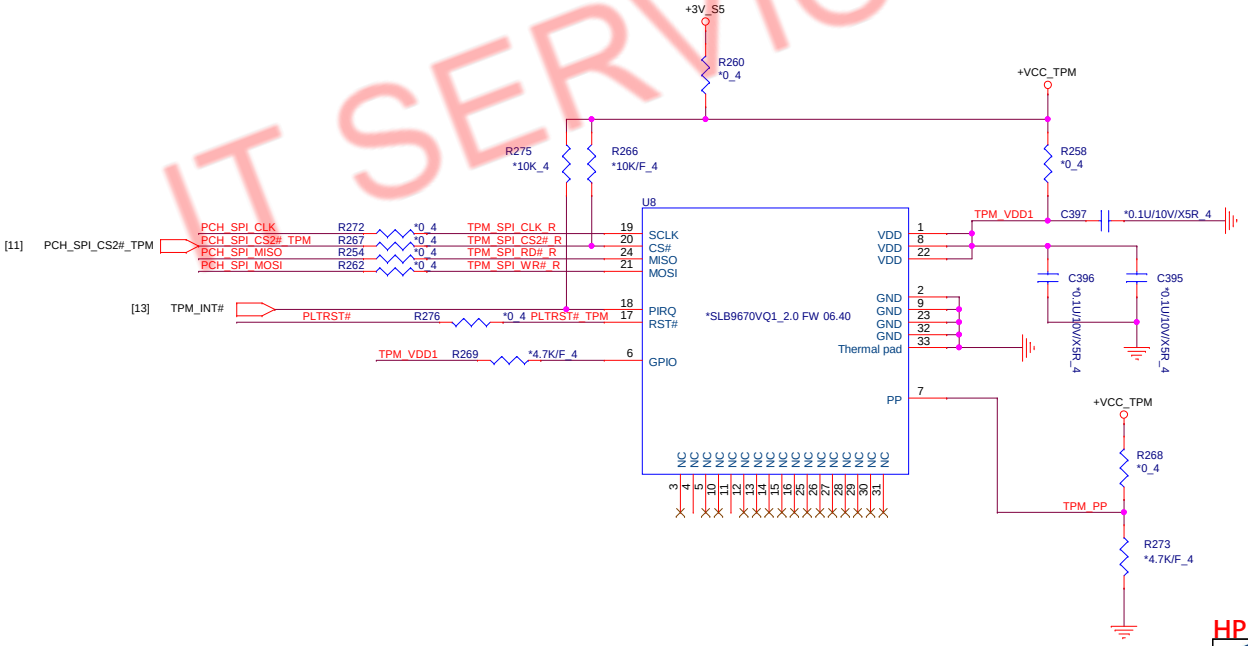


LPC HEADER



CLR_PASSWORD Default:install
CONN MINI JUMPER 2P FS (P2.0,H5.0)

TPM (1.2 or 2.0)



Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	Jumper/LPC Header	1A
Date: Friday, December 18, 2015	Sheet 31 of 58	

RF/EMI Suggestion

[4,7,18,19,40] +VDDQ
[6,43,44] +VCC_CORE
[30,39,40,41,43,44,45,46,47,48,49,50,51,52] +VIN

+VIN: C603 *8P/50V/COG_4, C57 *0.1U/10V/X5R_4, C500 0.1U/10V/X5R_4, C585 *0.1U/10V/X5R_4, C466 0.1U/10V/X5R_4
+VCC_CORE: C509 *10U/6.3V/X5R_6, C63 *10U/6.3V/X5R_6, C224 *8P/50V/COG_4, C218 *8P/50V/COG_4
+5V: C433 *0.1U/10V/X5R_4, C24 *0.1U/10V/X5R_4, C652 *0.1U/10V/X5R_4, C601 *0.1U/10V/X5R_4, C437 *0.1U/10V/X5R_4
+VIN: C50 0.1U/10V/X5R_4, C600 *0.1U/10V/X5R_4, C467 *0.1U/10V/X5R_4, C399 0.1U/10V/X5R_4
+VCC_CORE: C84 *0.1U/10V/X5R_4, C92 *0.1U/10V/X5R_4, C96 *0.1U/10V/X5R_4, C100 *0.1U/10V/X5R_4
+5V_S5: C461 *0.1U/10V/X5R_4, C651 *0.1U/10V/X5R_4, C55 *0.1U/10V/X5R_4, C559 *0.1U/10V/X5R_4, C442 *0.1U/10V/X5R_4
+VIN: C574 *0.1U/10V/X5R_4, C398 *0.1U/10V/X5R_4, C560 0.1U/10V/X5R_4, C553 *0.1U/10V/X5R_4, C402 *0.1U/10V/X5R_4
+VDDQ: C71 *8P/50V/COG_4, C149 *8P/50V/COG_4, C109 *8P/50V/COG_4, C64 *8P/50V/COG_4, C323 *8P/50V/COG_4, C359 *8P/50V/COG_4, C321 *8P/50V/COG_4
+5V_S5: C37 *0.1U/10V/X5R_4, C561 *0.1U/10V/X5R_4

AR18 *0/S_4 — AGND
AR24 *0/S_4 — AGND
AR22 *0/S_4 — LANGND
AR21 *0/S_4 — LANGND
EC-PV-01

+3V_S5: C20 *0.1U/10V/X5R_4, C525 *0.1U/10V/X5R_4, C526 *0.1U/10V/X5R_4, C401 *0.1U/10V/X5R_4, C400 *0.1U/10V/X5R_4

Holes

outline
H2 *HG-C276D134P2-OPP-BSW
H15 *HG-C276D134P2-OPP-BSW
H18 *HG-C276D134P2-OPP-BSW
H17 *HG-C276D134P2-OPP-BSW
H14 *HG-C276D134P2-OPP-BSW

WLAN x1 (need to mount nut)
H3 H-TC276BC126D126PT

CPU x4 (need to mount nut)
H7 H-TC177BC102D102P2
H8 H-TC177BC102D102P2
H13 H-TC177BC102I122D102P2
H12 H-TC177BC102I122D102P2

Orientation x2
H16 *HG-C315D185P2-OPP-BSW
H4 *HG-C315D185P2-OPP-BSW

H1 O-OPP-BSW-1

GPU x2 (need to mount nut)
H10 H-TC177BC102D102P2
H6 H-TC177BC102D102P2

FAN x3 (need to mount nut)
H11 H-TC315BC169D169PT
H9 H-TC315BC169D169PT
H5 H-TC315BC169D169PT

PAD1 GASKET-RE118X157NP
PAD2 GASKET-RE118X157NP
PAD3 GASKET-RE118X157NP

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Quanta Computer Inc.
PROJECT: HP-Hawaii

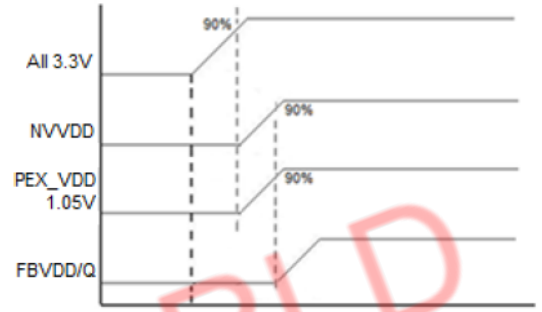
Size	Document Number	Rev
Custom	EMI/RF/Holes	1A
Date: Thursday, March 17, 2016	Sheet 32 of 58	

[34,35,52] +1.05V_VGA
[35,36,37,51,52] +3.3V_VGA

PEX_IOVDD + PEX_IOVDDQ = 1.042A

PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA

PEX_PLLVDD = 130mA

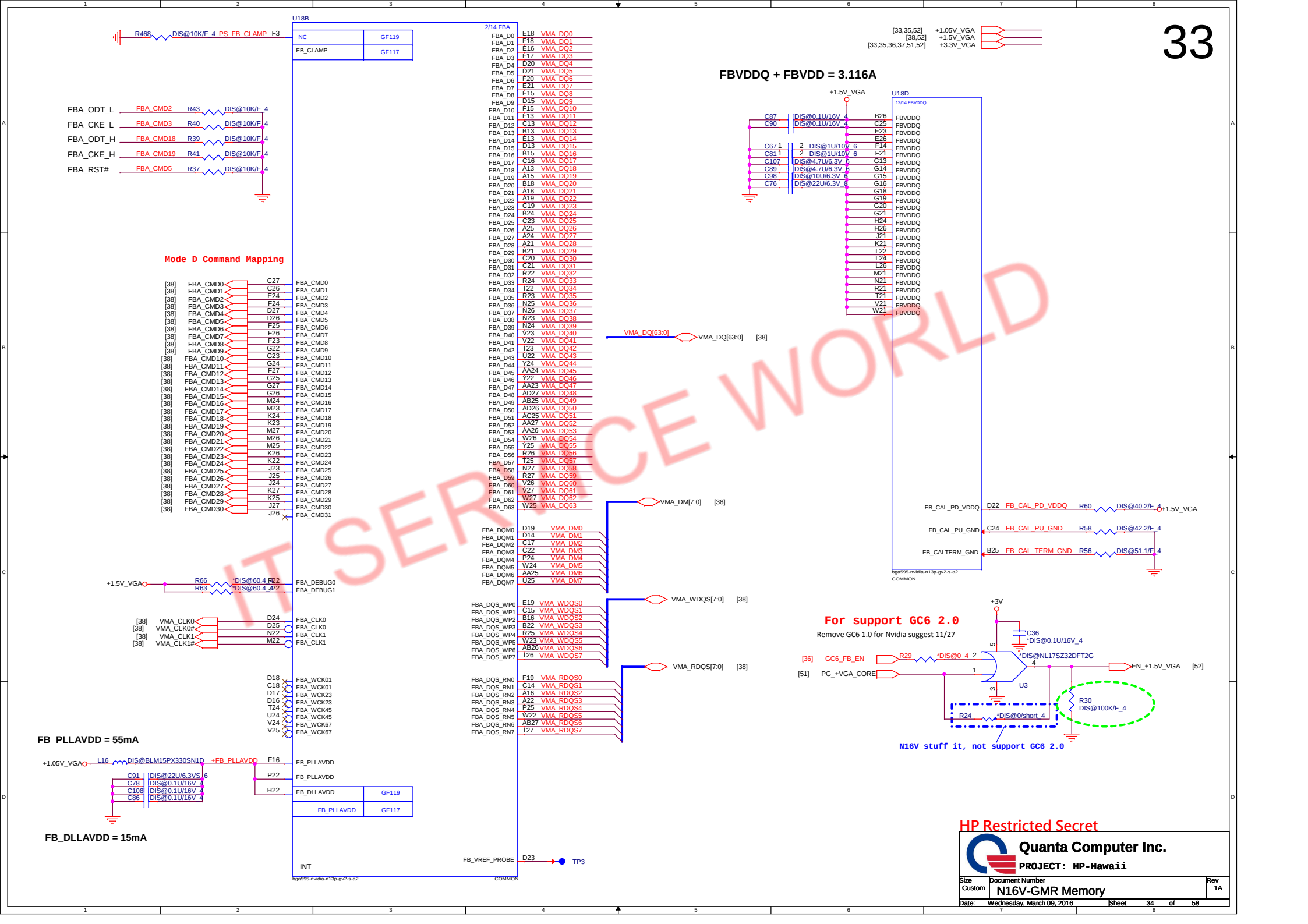


HP Restricted Secret

Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	N16V-GMR PCIE	1A

Date: Wednesday, March 09, 2016 Sheet 33 of 58

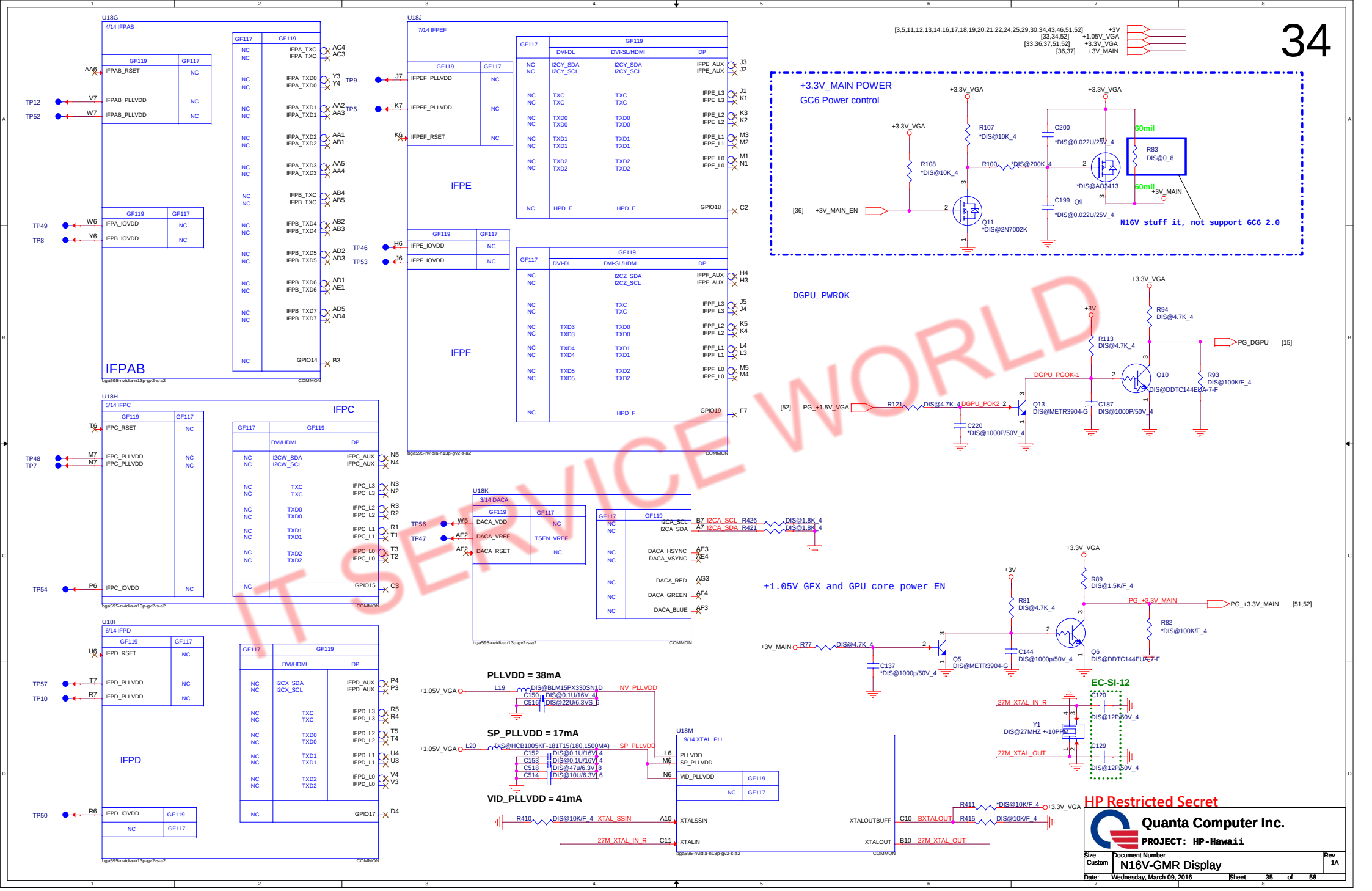


Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	N16V-GMR Memory	1A

Date: Wednesday, March 09, 2016 Sheet 34 of 58

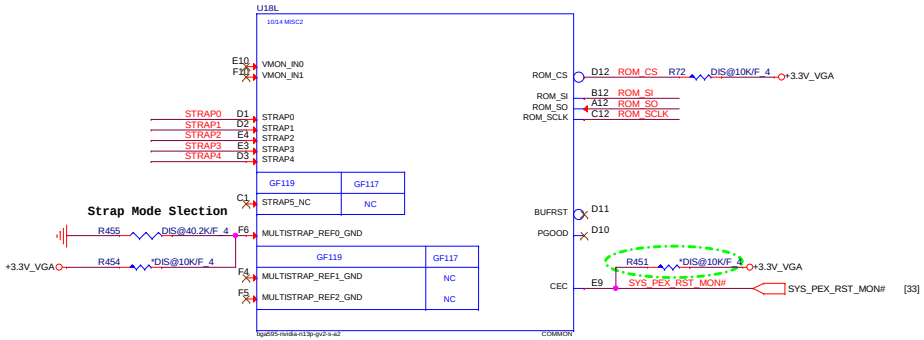


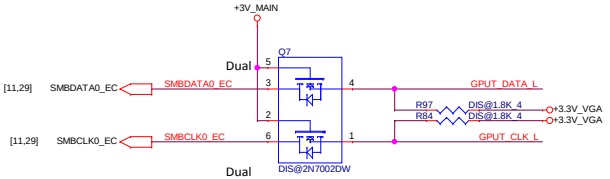
HP Restricted Secret

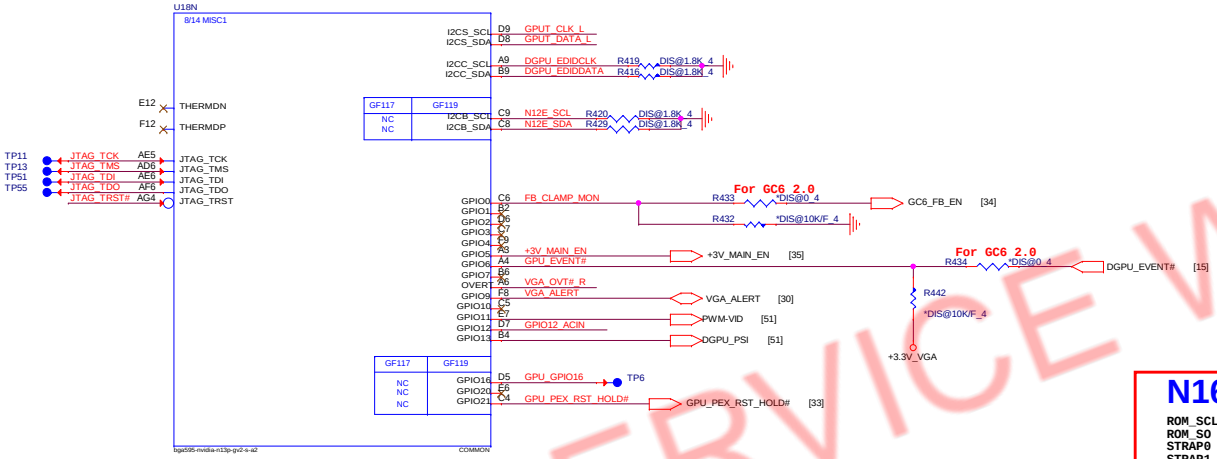
Quanta Computer Inc.
PROJECT: HP-Hawaii

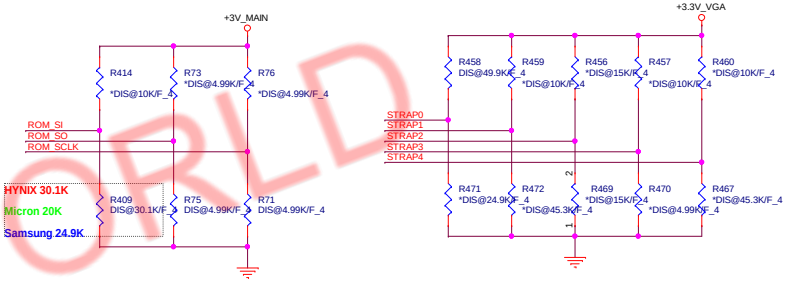
Size	Document Number	Rev
Custom	N16V-GMR Display	1A

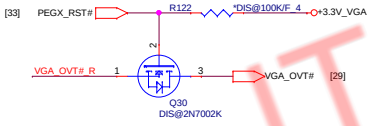
Date: Wednesday, March 09, 2016 Sheet 35 of 58

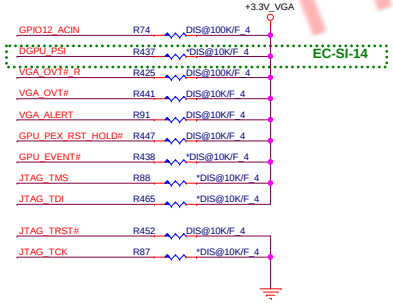












GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVT#	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

N16V-GMR1 DID=0x134F

GB2B-64

```
ROM_SCLK = Stuff 4.99K pull down
ROM_SO   = Stuff 4.99K pull down
STRAP0   = Stuff 49.9K pull up
STRAP1   = NC
STRAP2   = NC
STRAP3   = NC
STRAP4   = NC
ROM_SI   = VRAM Configuration follow below table
```

Logical Strap Bit Mapping

	PU-VDD	PD	QCI P/N
4.99K	1000	0000	CS24992FB26
10K	1001	0001	CS31002FB26
15K	1010	0010	CS31502FB24
20K	1011	0011	CS32002FB29
24.9K	1100	0100	CS32492FB16
30.1K	1101	0101	CS33012FB18
34.8K	1110	0110	CS33482FB06
45.3K	1111	0111	CS34532FB18

ROM_SI

RAMCFG [3:0]	DESCRIPTION 1.5V DDR3	Vendor	Vendor P/N	ROM_SI	STN B/S	Configuration
	256Mx16					
0011	DDR3 256Mx16, 64bit, 4Gb,1000MHz	Micron	MT41J256M16LY-091G:N	PD 20K ohm	AKD59GSTL02	Single Rank or
1001	DDR3 256Mx16, 64bit, 4Gb,1000MHz	HYNIX	H5TC4G63CFR-N0C	PD 30.1K ohm	AKD5PZDTW03	Single Rank stuffing
1000	DDR3 256Mx16, 64bit, 4Gb,1000MHz	Samsung	K4W4G1646E-BC1A	PD 24.9K ohm	AKD5PGDT502	for Dual Rank

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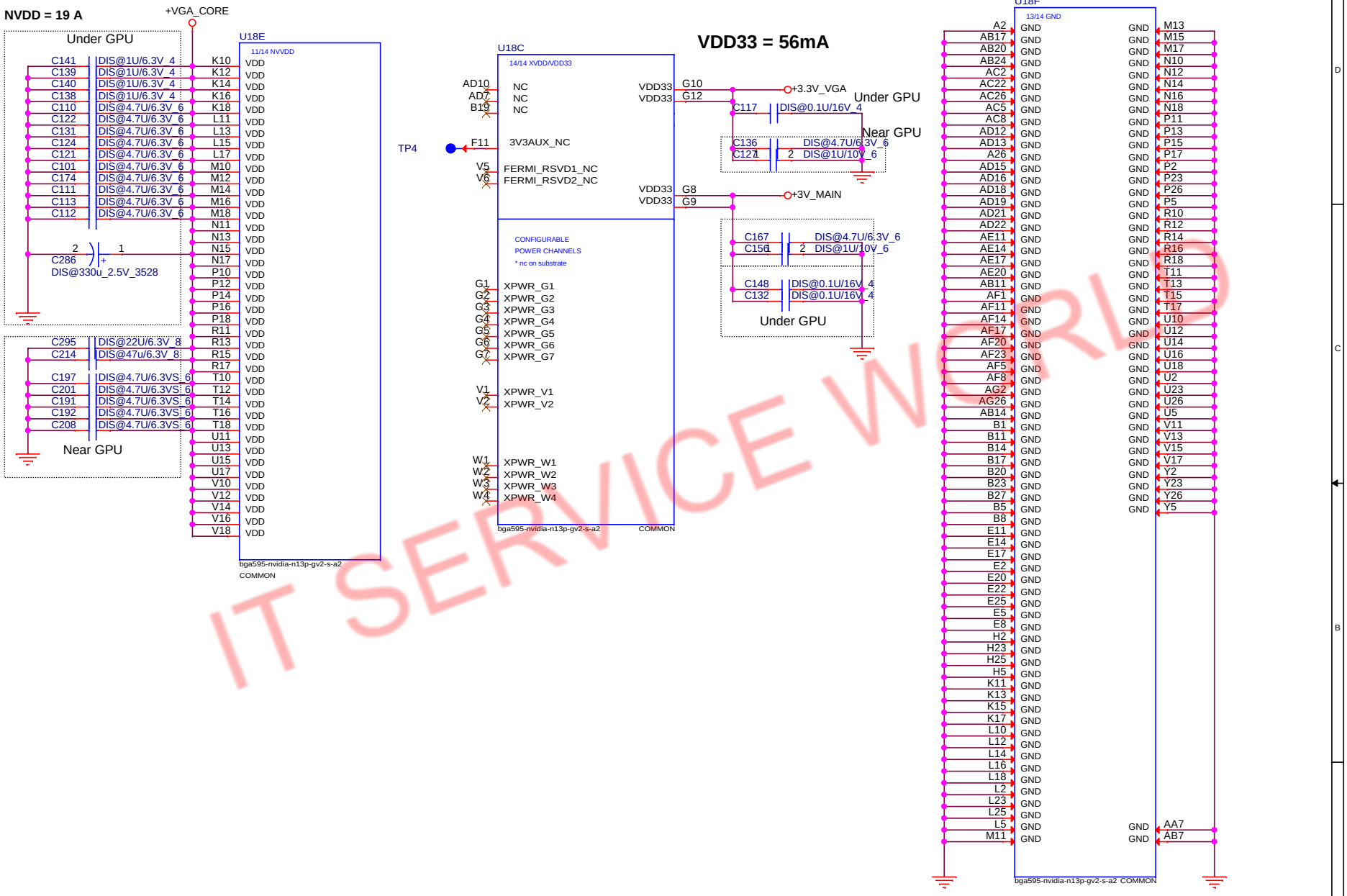
Quanta Computer Inc.

PROJECT: HP-Hawaii

Size: Custom | Document Number: N16V-GMR GPIO/Strap | Rev: 1A

Date: Monday, March 21, 2016 | Sheet 36 of 58



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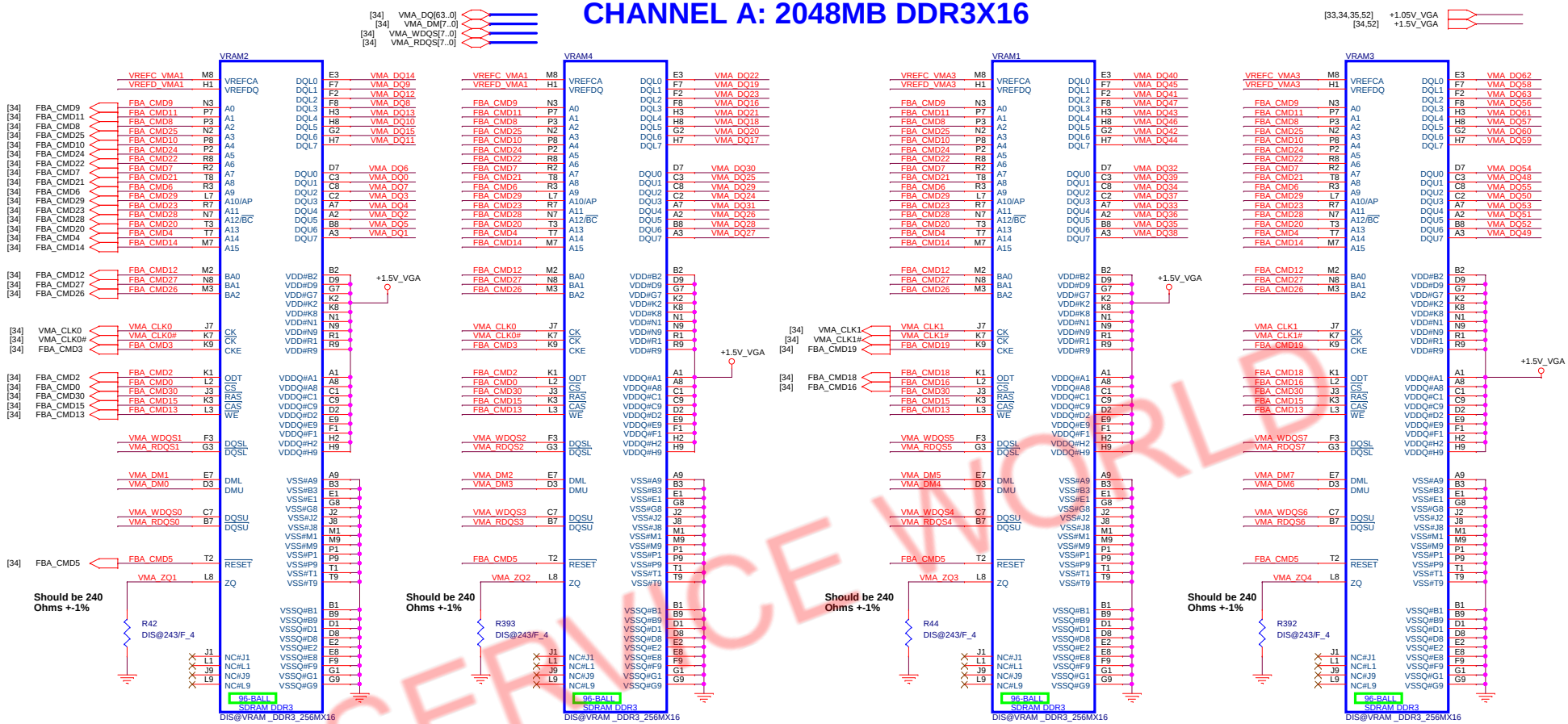
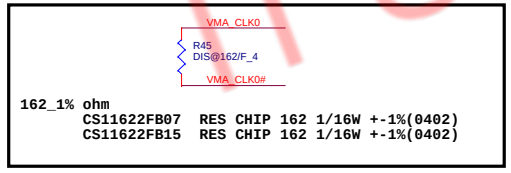
PROJECT: HP-Hawaii

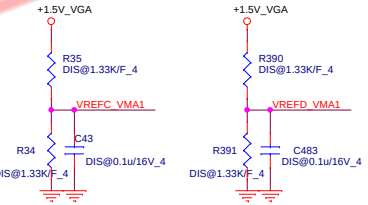
Size	Document Number	Rev
Custom	N16V-GMR Power/GND	1A

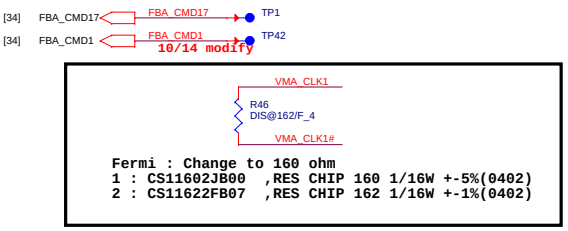
Date: Wednesday, March 09, 2016 Sheet 37 of 58

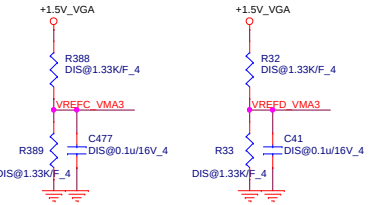
CHANNEL A: 2048MB DDR3X16

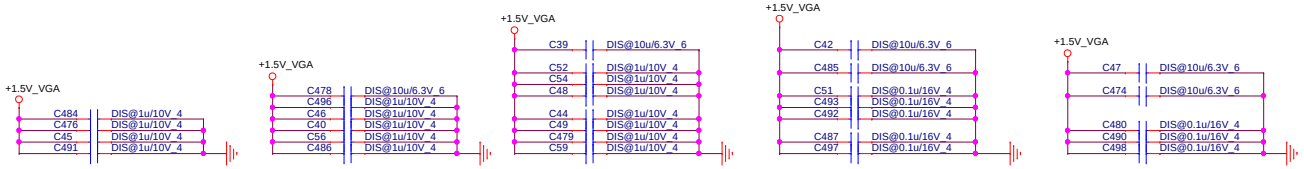










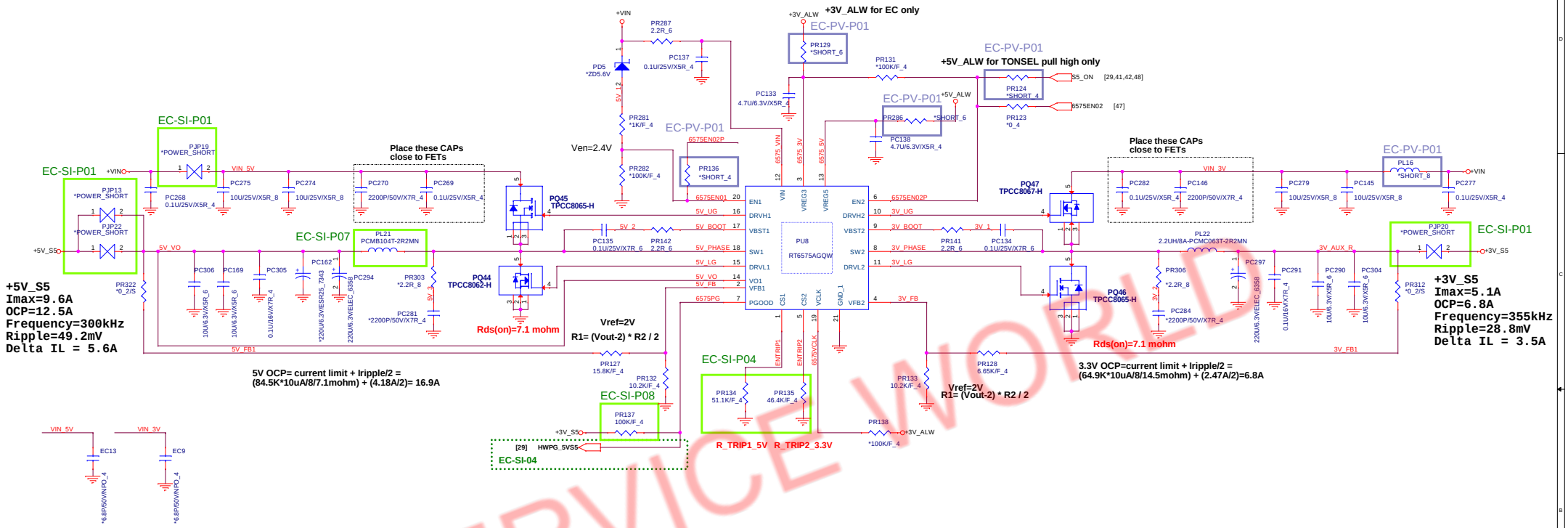


Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	N16V-GMR DDR3 VRAM	1A

Date: Wednesday, March 09, 2016 Sheet 38 of 58



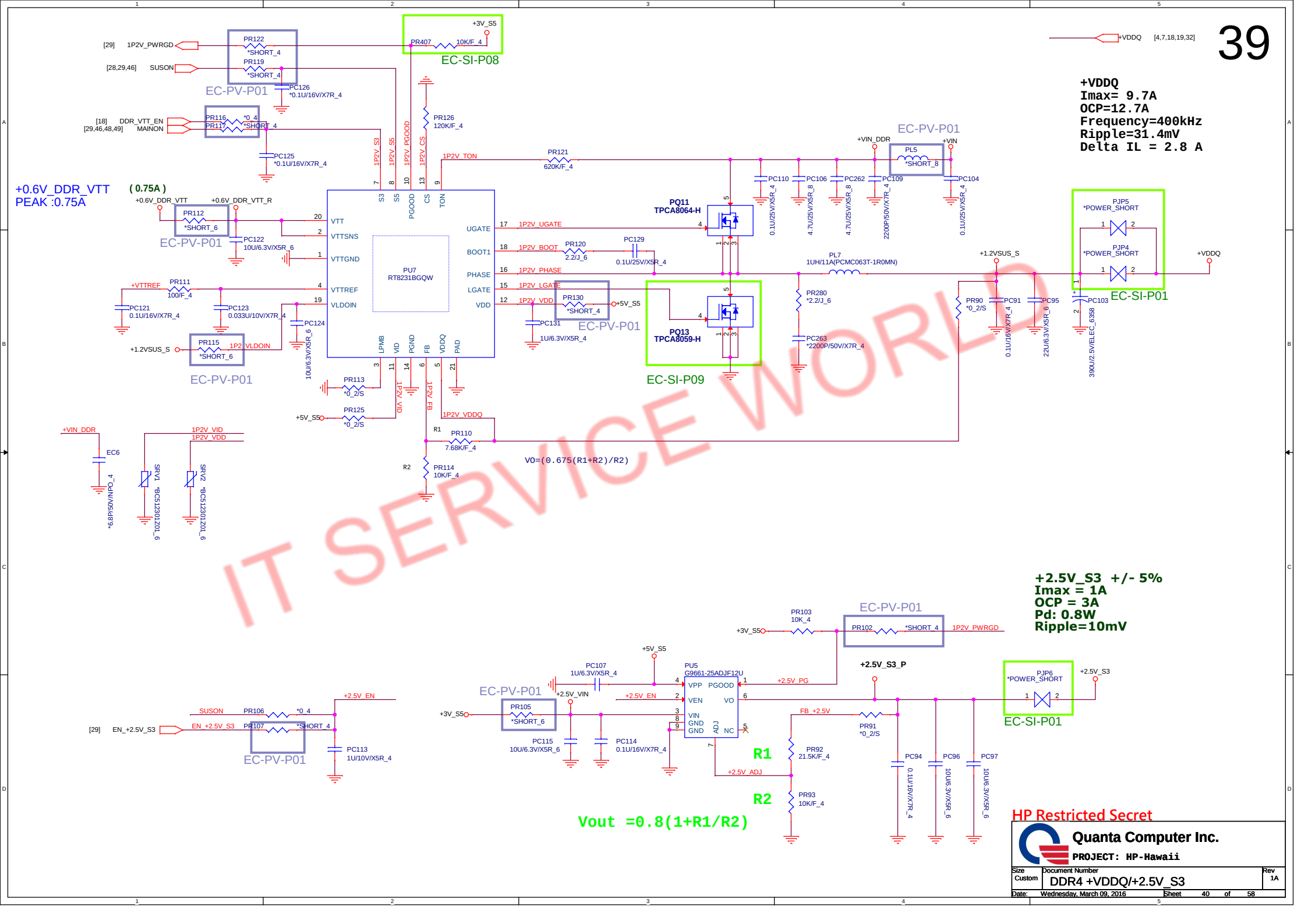
L/S Mosfet parameter

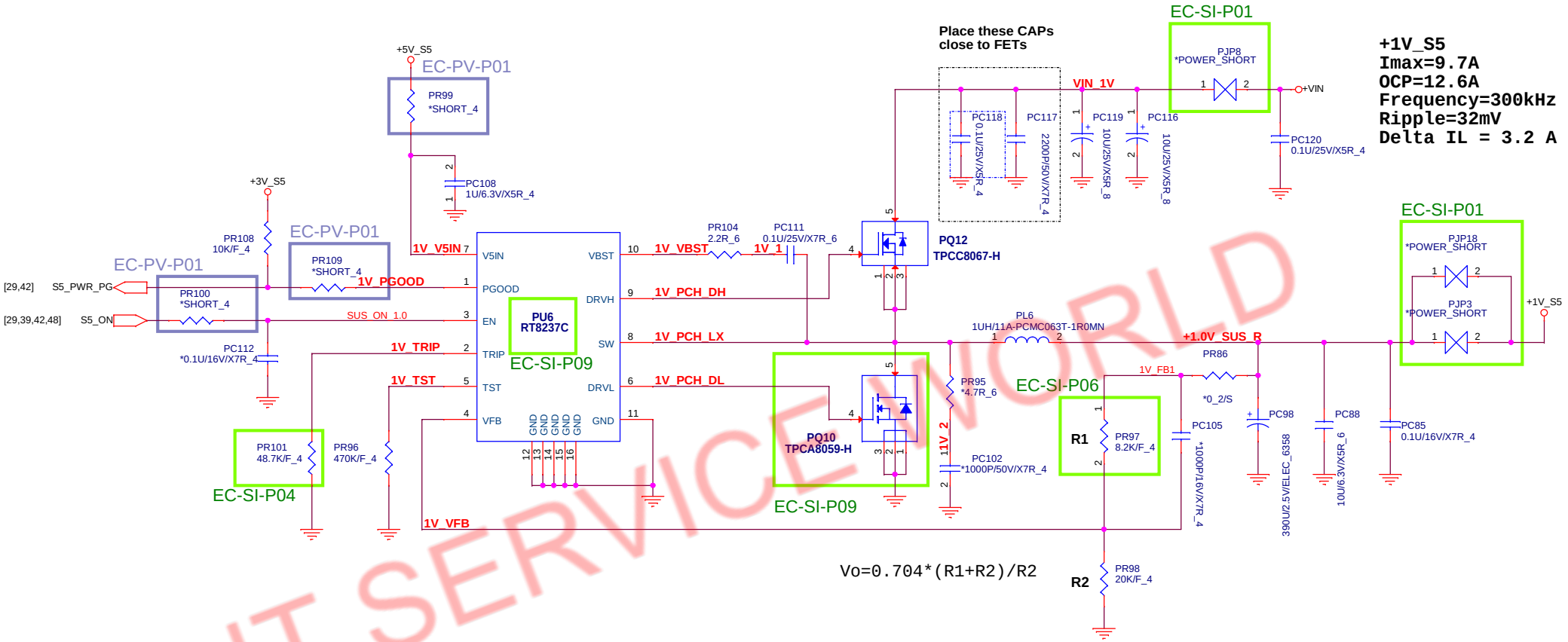
MOSFET	Package	ID (Ta=25C)	Rds_on_max
TPCC8067-H	DFN3x3	9A	26m
TPCC8062-H	DFN3x3	27A	7.1m

Power On sequencing

EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

Quanta Computer Inc.
PROJECT: HP-Hawaii
Size: Custom | Document Number: System +3V_S5/+5V_S5 | Rev: 1A
Date: Wednesday, March 09, 2016 | Sheet 39 of 58


+VDDQ [4,7,18,19,32]
+VDDQ
Imax= 9.7A
OCP=12.7A
Frequency=400kHz
Ripple=31.4mV
Delta IL = 2.8 A
+0.6V_DDR_VTT (0.75A)
PEAK :0.75A
PU7 RT8231BGQW
PQ11 TPCA8064-H
PQ13 TPCA8059-H
PU5 G9661-25ADJF12U
EC-PV-P01
EC-SI-P08
EC-SI-P09
EC-SI-P01
VO=(0.675(R1+R2)/R2)
+2.5V_S3 +/- 5%
Imax = 1A
OCP = 3A
Pd: 0.8W
Ripple=10mV
R1
R2
Vout =0.8(1+R1/R2)
IT SERVICE WORLD
HP Restricted Secret
Quanta Computer Inc.
PROJECT: HP-Hawaii
DDR4 +VDDQ/+2.5V_S3
Wednesday, March 09, 2016
Sheet 40 of 58



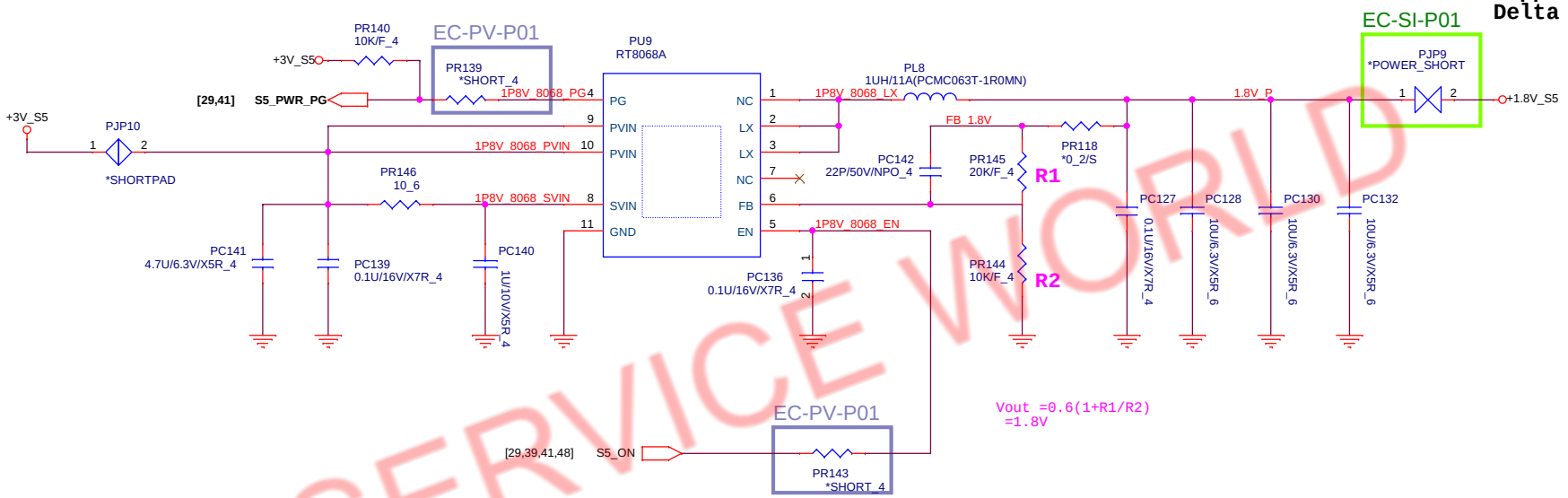
Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
B	+1V_S5	1A

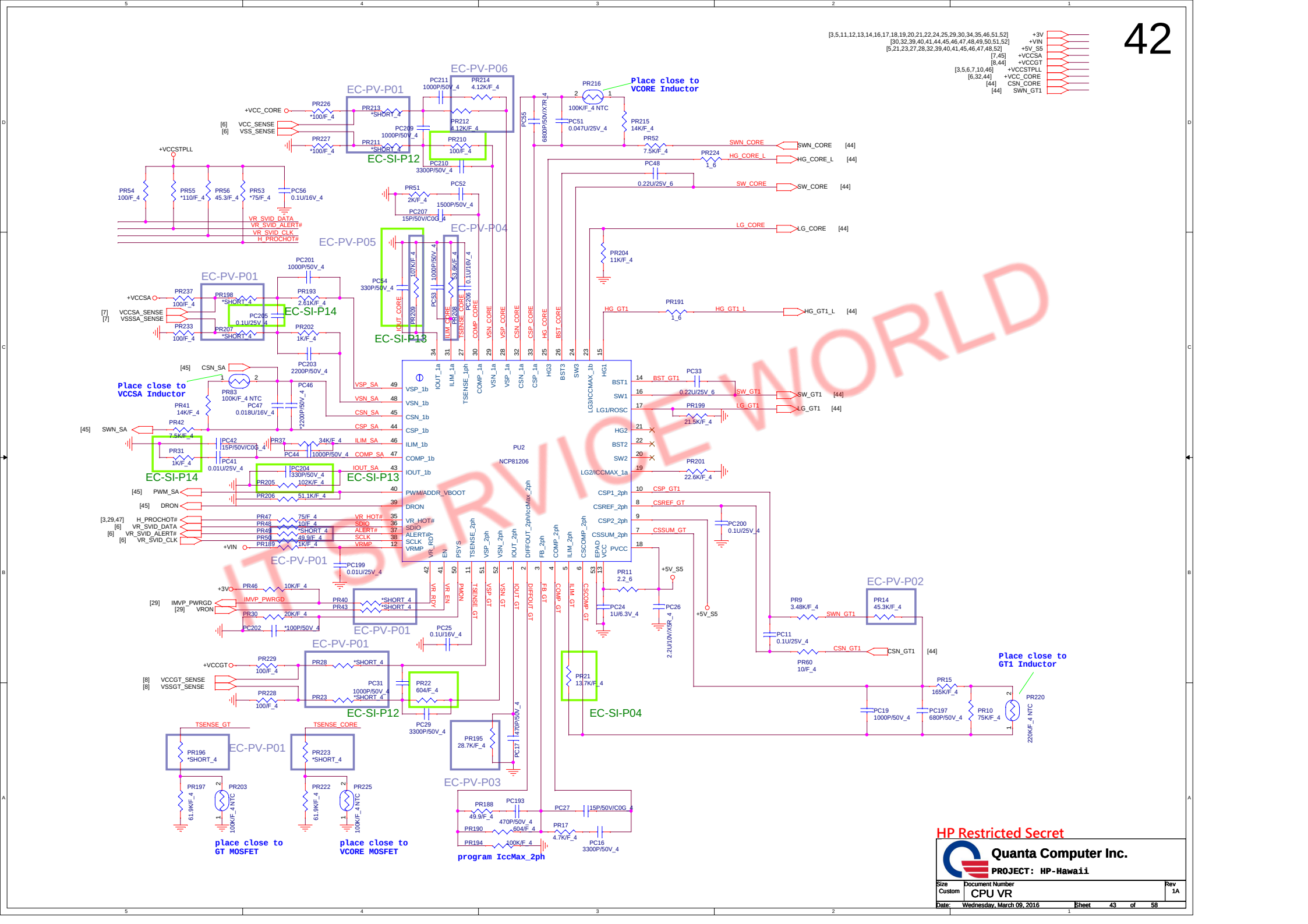
Date: Wednesday, March 09, 2016 Sheet 41 of 58

V1P8A (RT8068A)

+1.8V_S5
Imax=1.2A
OCP=4A
Frequency=1MHz
Ripple=12mV
Delta IL = 0.8A



Quanta Computer Inc.		
PROJECT: HP-Hawaii		
Size: B	Document Number: +1.8V_S5	Rev: 1A
Date: Wednesday, March 09, 2016	Sheet 42 of 58	



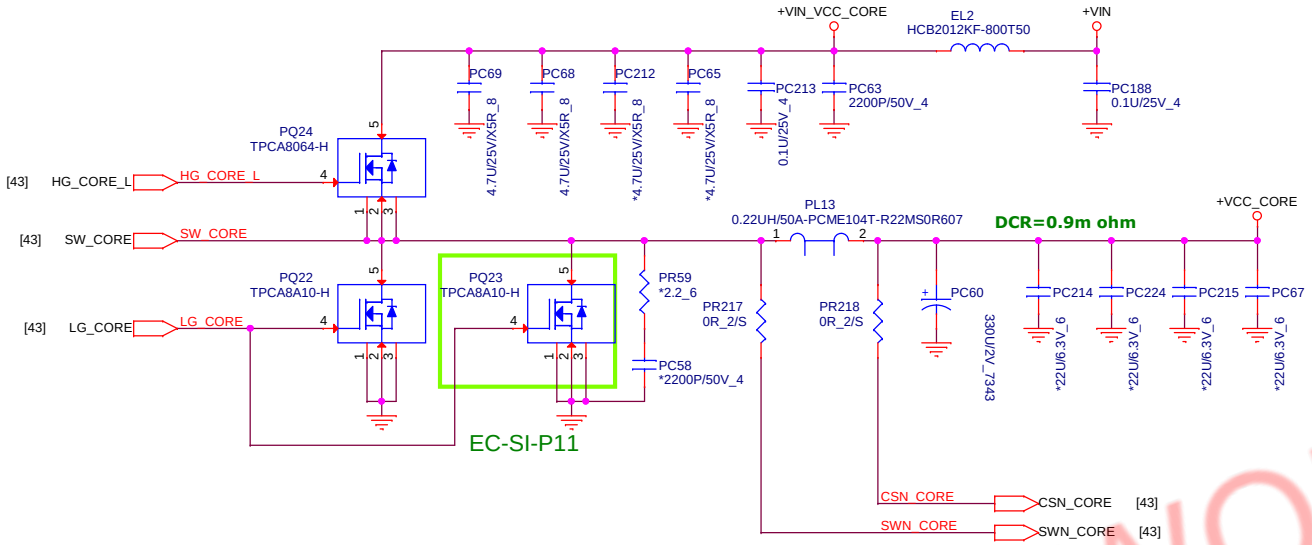
Quanta Computer Inc.

PROJECT: HP-Hawaii

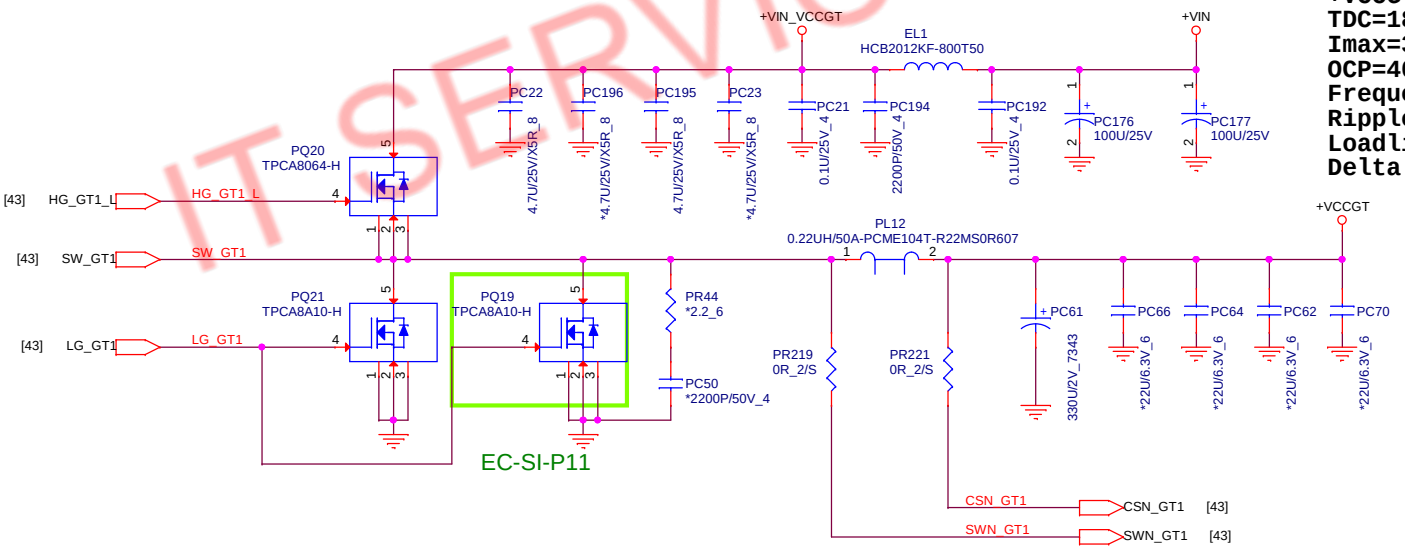
Size	Document Number	Rev
Custom	CPU VR	1A

Date: Wednesday, March 09, 2016 Sheet 43 of 58

+VCC_CORE
TDC=21A
Imax=29A
OCP=36A
Frequency=450kHz
Ripple=13mV
Loadline: -2.4m ohm
Delta IL = 9.6A



+VCCGT
TDC=18A
Imax=31A
OCP=40A
Frequency=450kHz
Ripple=13mV
Loadline: -3.1m ohm
Delta IL = 9.6A



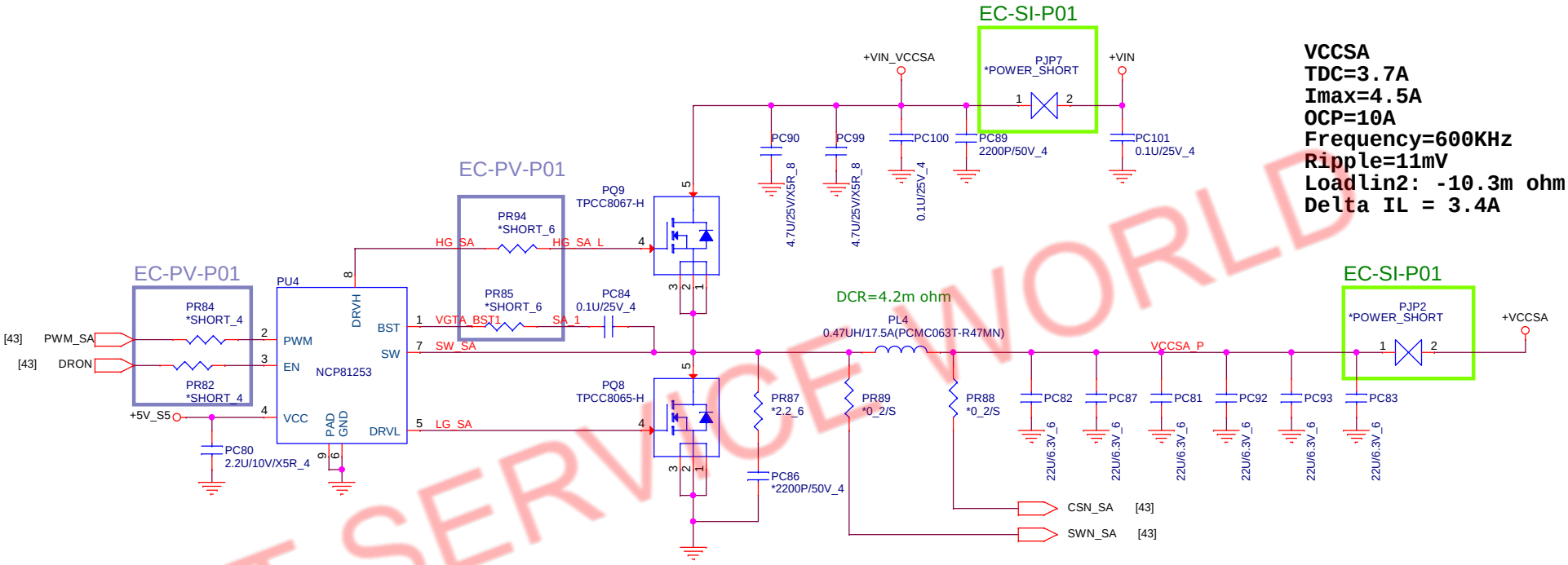
Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
B	CPU +VCC_CORE/+VCCGT	1A

Date: Wednesday, March 09, 2016 Sheet 44 of 58

[30,32,39,40,41,43,44,46,47,48,49,50,51,52] +VIN
[5,21,23,27,28,32,39,40,41,43,46,47,48,52] +5V_S5
[7,43] +VCCSA

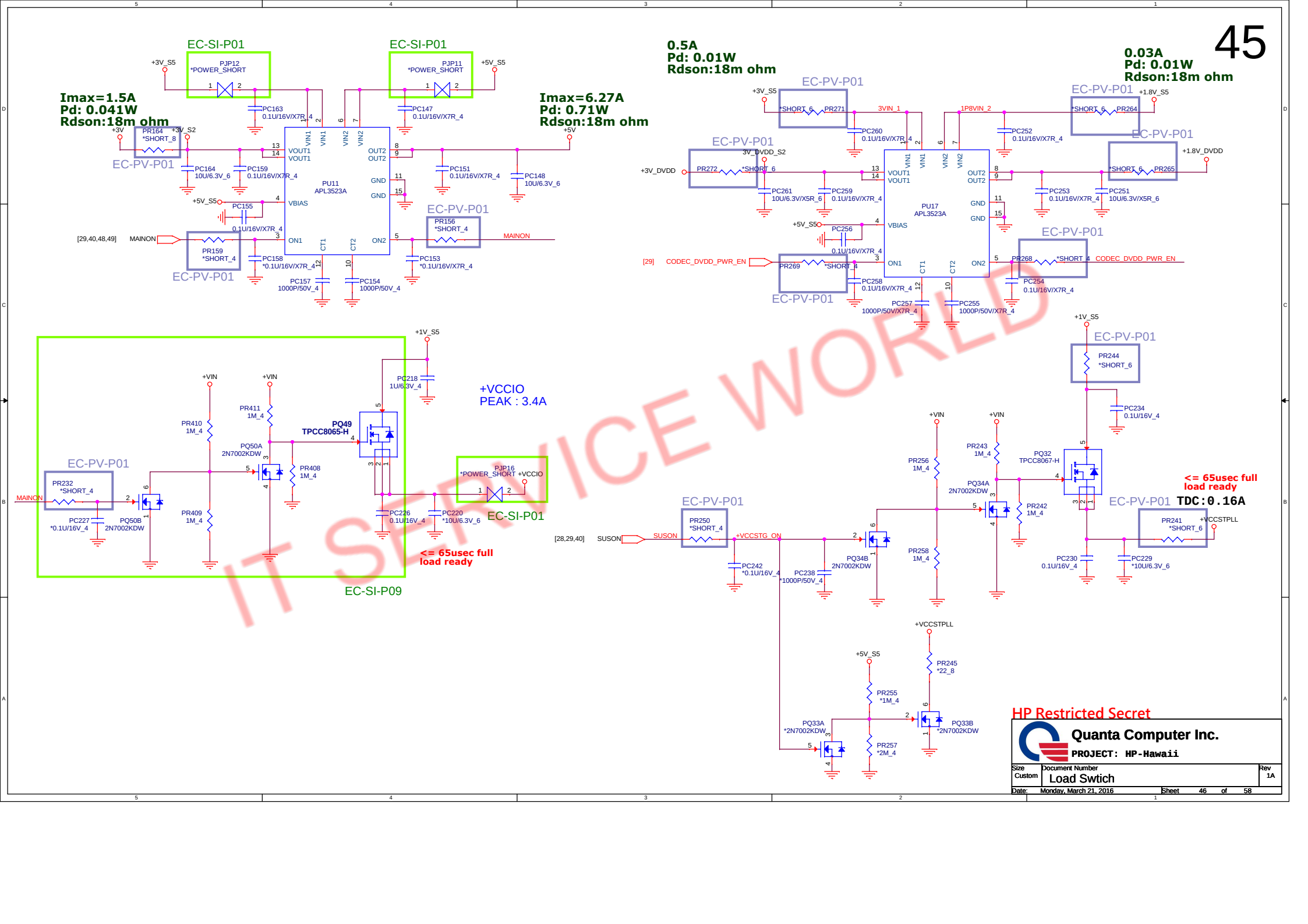
VCCSA



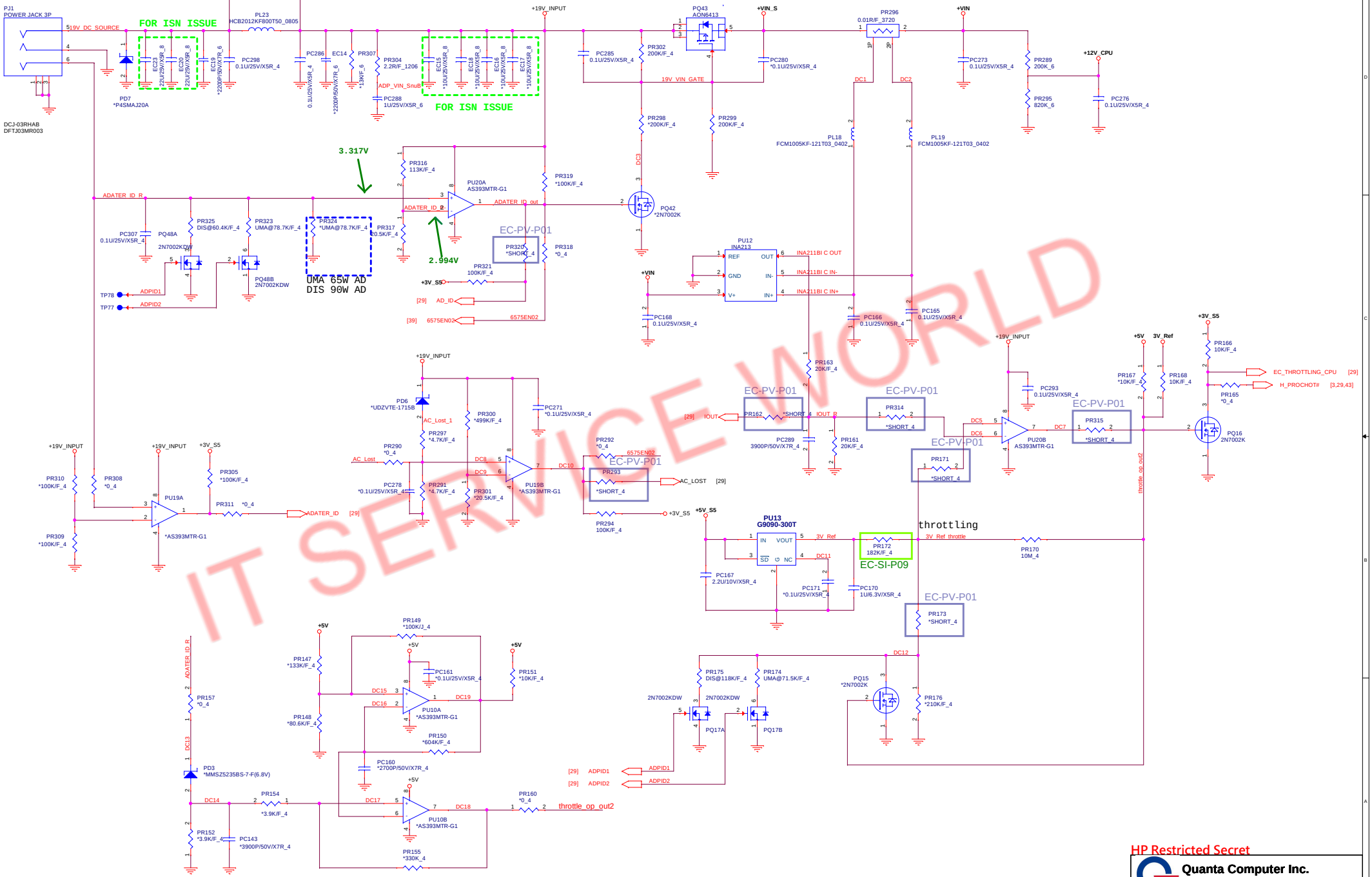
VCCSA
TDC=3.7A
Imax=4.5A
OCP=10A
Frequency=600KHz
Ripple=11mV
Loadlin2: -10.3m ohm
Delta IL = 3.4A

Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	CPU +VCCSA	1A
Date: Wednesday, March 09, 2016	Sheet 45 of 58	



Id=16A
Qg=41~58nC
Rdson=6.9~8.5mOHM

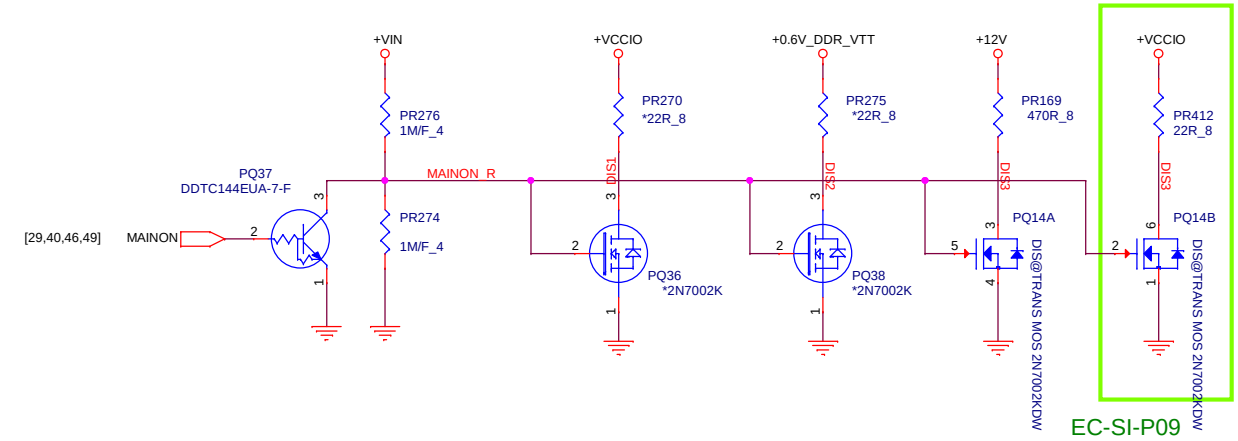


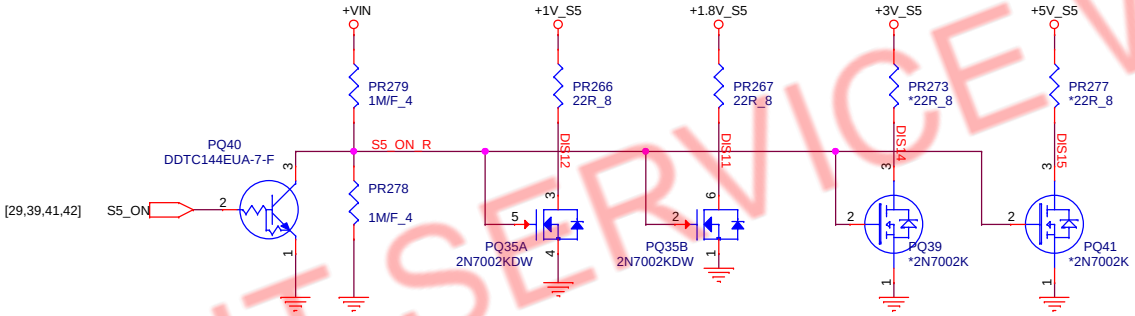
Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	DC IN	1A

Date: Wednesday, March 09, 2016 Sheet 47 of 56

DISCHARGE





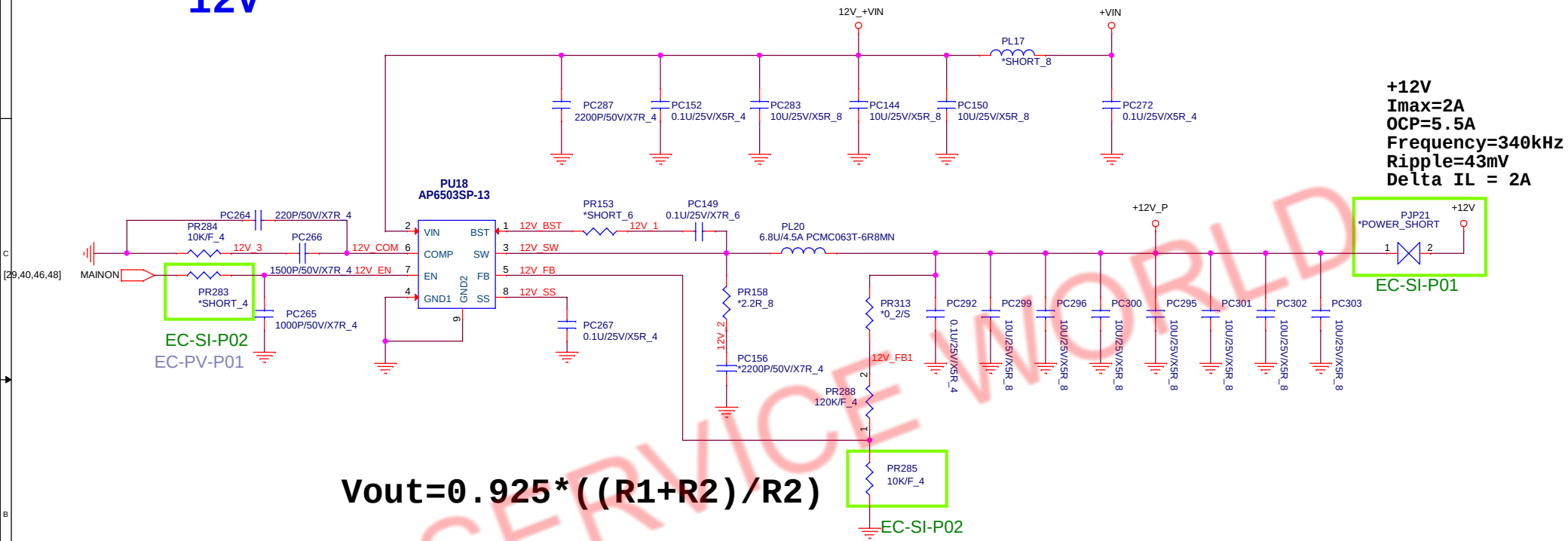
Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
B	Discharge	1A

Date: Wednesday, March 09, 2016 Sheet 48 of 58

12V



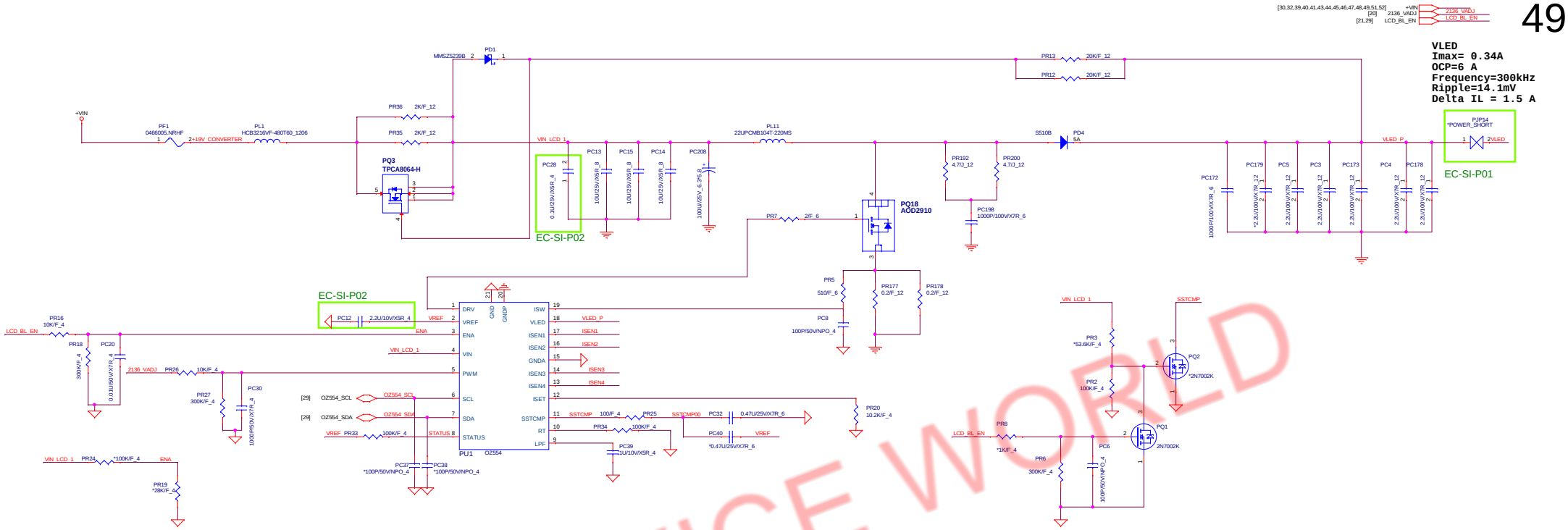
+12V
Imax=2A
OCP=5.5A
Frequency=340kHz
Ripple=43mV
Delta IL = 2A

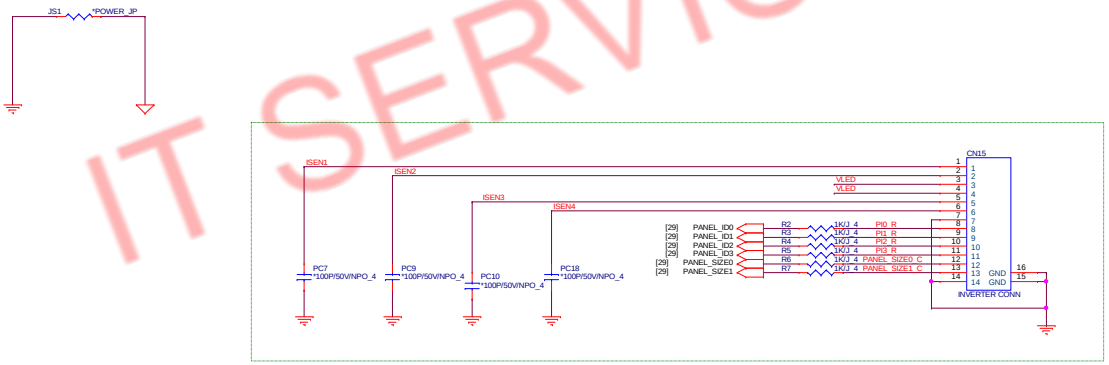
Vout=0.925*((R1+R2)/R2)

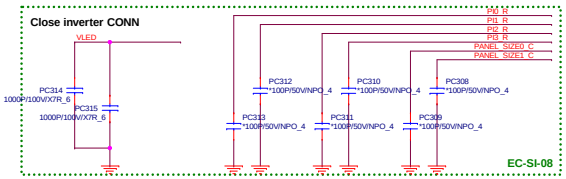
Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
B	+12V	1A

Date: Wednesday, March 09, 2016 Sheet 49 of 58







PANEL_SIZE Table

PANEL_Size[1:0]	Size
00	19.5/9.53"
01	21.5"
10	23.6"/23.8"
11	Reserve

19.45" /19.53" PANEL_ID Table

PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M200HJJ-L20 FHD
1101	AUO M195RTN01.0 HD+
1100	LGD LM195WD1-TLA1 HD+
1010	Reserve

21.5" PANEL_ID Table

PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M215HJK-L3B FHD eDP
1101	SDC LTM215HL01 FHD
1100	LGD LM215WF3-SLN1 FHD
1011	Reserve

23.6" /23.8" PANEL_ID Table

PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M236HJK-L5B FHD eDP
1101	AUO M238HAN01.0 FHD
1100	LGD LM238WF1-SLE1 FHD
1011	SDC LTM238HL02 FHD
1010	Reserve

Panel_ID[3:0] = 1111 & Panel_Size[1:0] = 11 is reserved for cabling detection by "No connection".

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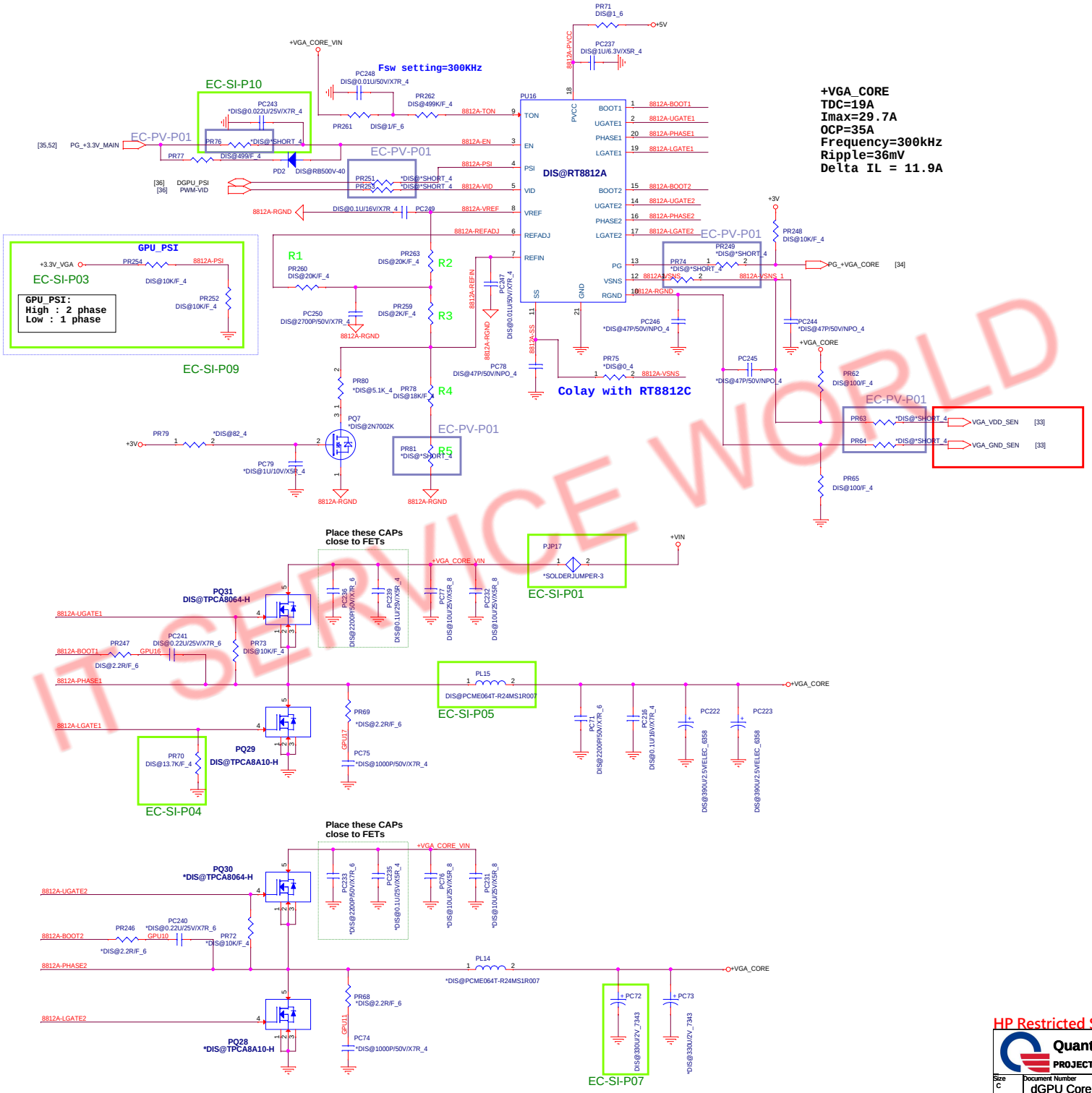
PROJECT: HP-Hawaii
Size: Custom | Document Number: OZ554 | Rev: 1A
Date: Thursday, March 17, 2016 | Sheet 50 of 58



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PROJECT: HP-Hawaii

Size	Document Number	Rev
C	dGPU Core	1A

Date: Wednesday, March 09, 2016 Sheet 51 of 58

VGA POWER

51

AO6402A
Rdson=24m ohm
Imax=0.2A
Pd: 0.01W

+1.05V_VGA
Imax=1.5A
OCP=4A
Frequency=1MHz
Ripple=12mV
Delta IL = 0.8A

+1.5V_VGA
Imax=4.7A
OCP=8A
Frequency=500KHz
Ripple=22mV
Delta IL = 2.8A

+1.05V VGA

V0=0.6*(R1+R2)/R2

VREF=0.604V

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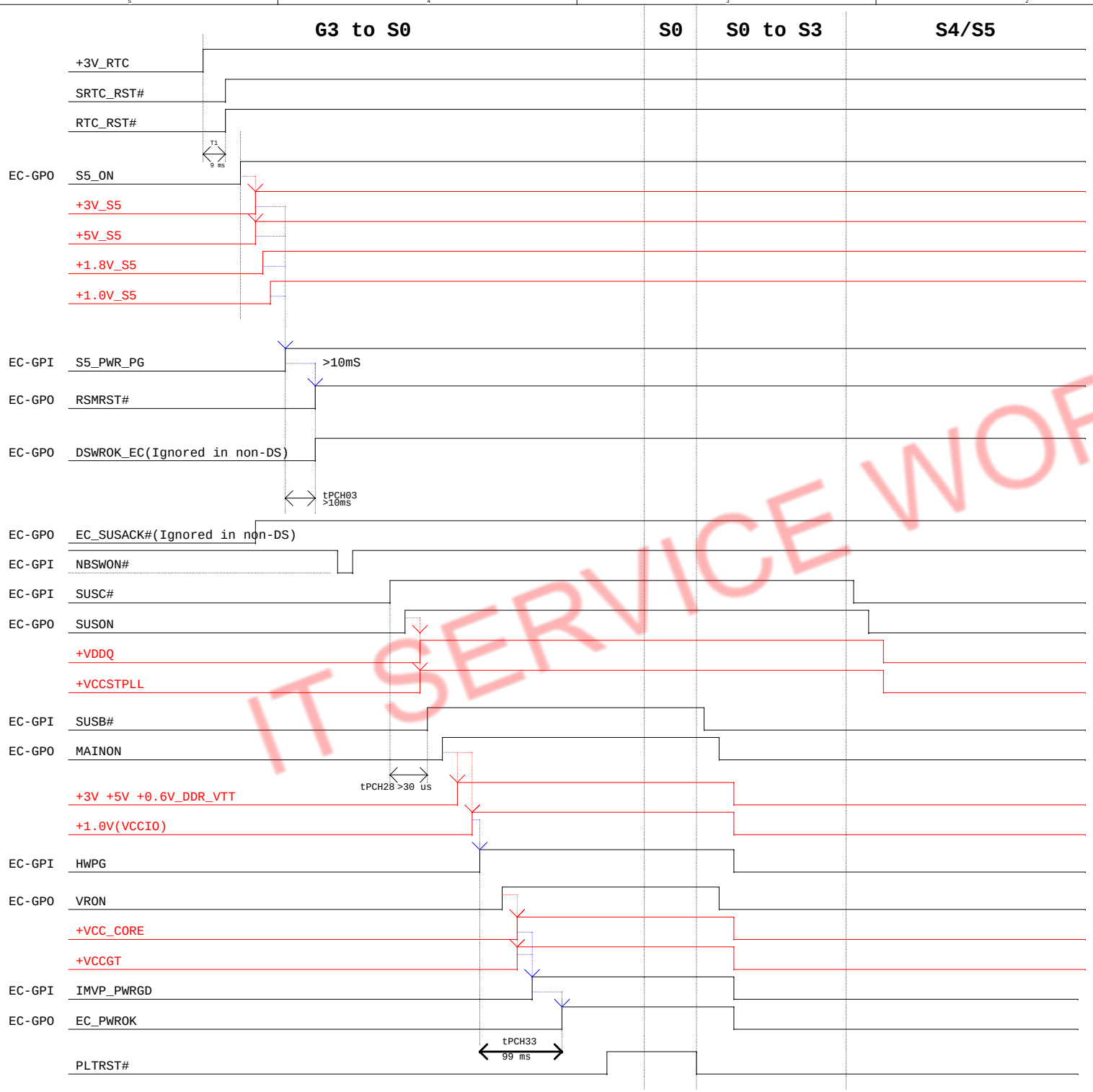
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	dGPU +1.05V/+1.5V	1A

Date: Wednesday, March 09, 2016 Sheet 52 of 58



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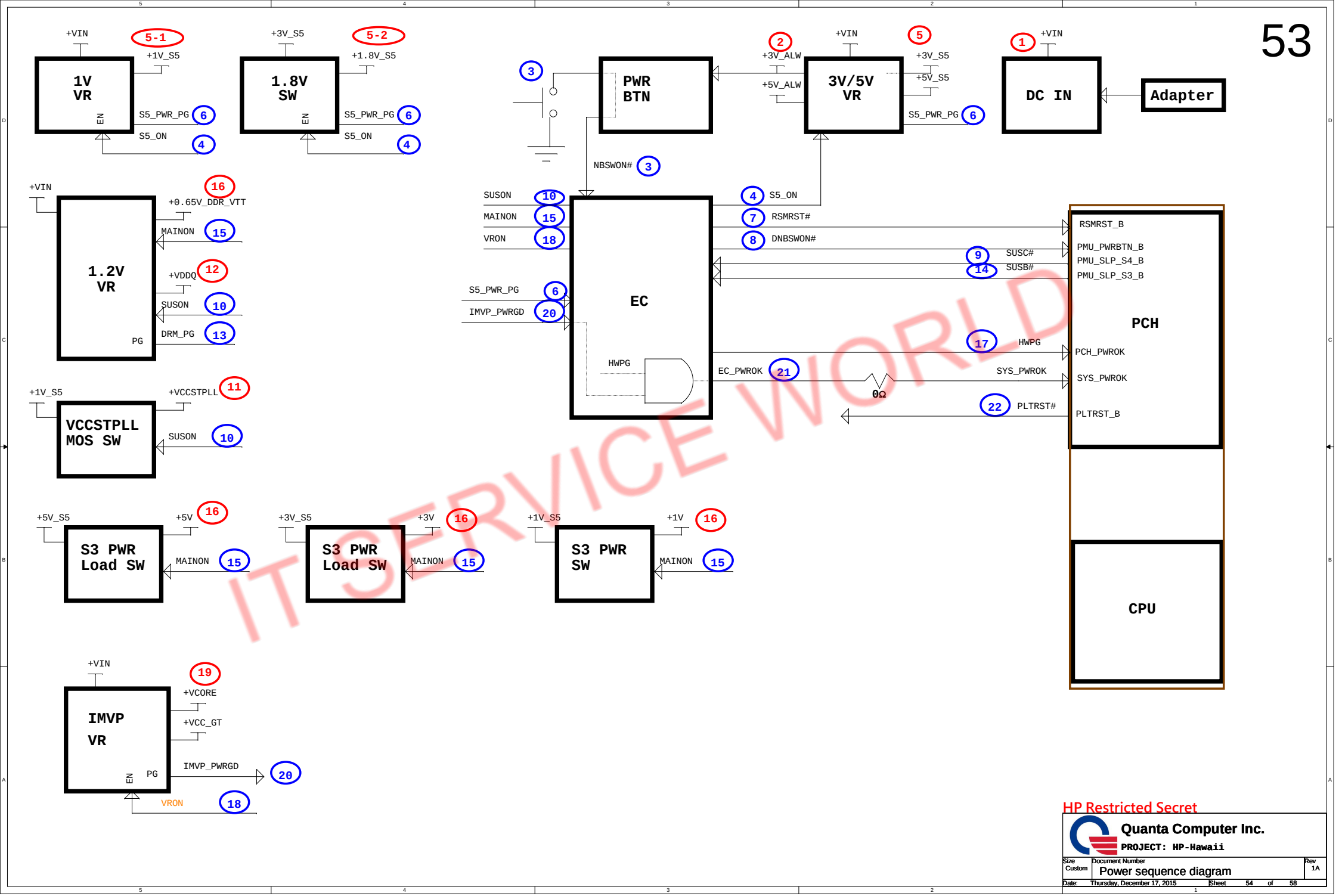
PROJECT: HP-Hawaii

Size	Document Number	Rev
C	Power Sequence	1A

Date: Thursday, December 17, 2015 Sheet 53 of 58



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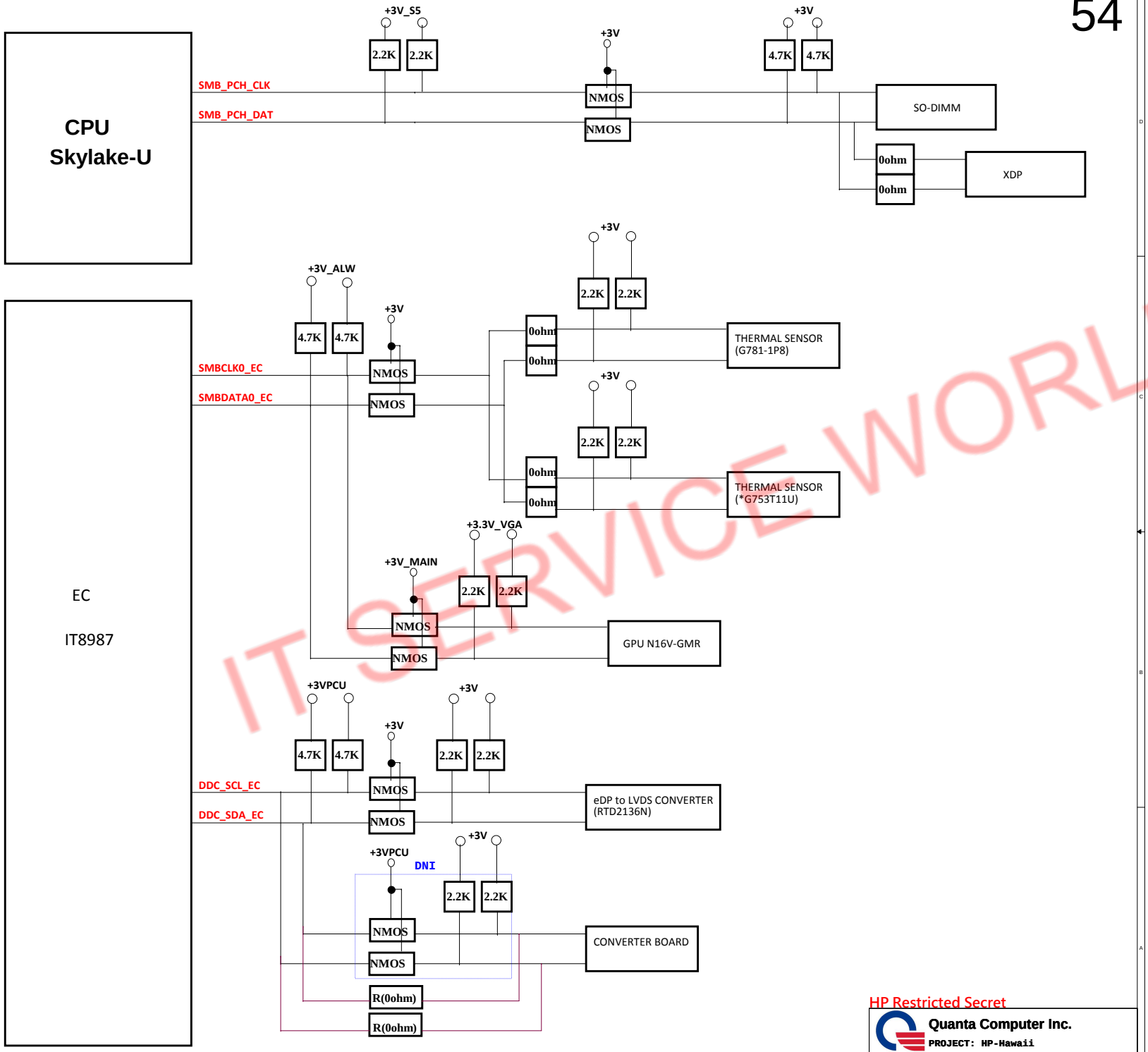
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	Power sequence diagram	1A

Date: Thursday, December 17, 2015 Sheet 54 of 58



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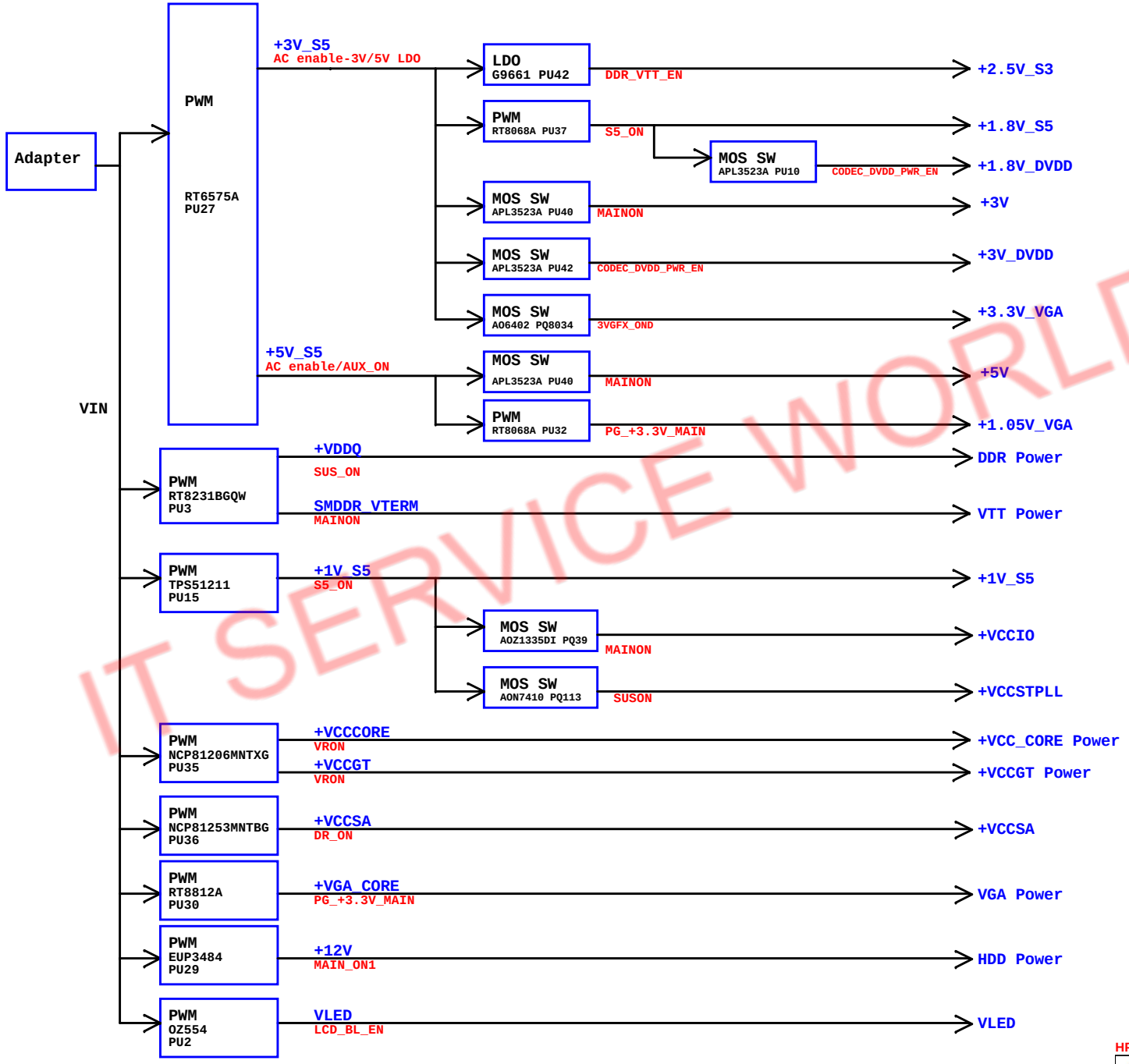
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SMBUS map	1A

Date: Thursday, December 17, 2015 Sheet 55 of 58

Power Delivery Map



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PROJECT: HP-Hawaii
Size C | Document Number: Power Delivery Map | Rev 1A
Date: Thursday, January 28, 2016 | Sheet 56 of 58

N91 EE Schematic DB to SI Change List

EC#	Page	Description	Part Affected
EC-SI-01	17,18	Unstuff C205/C213 for DDR4 Issue	C205,C213
EC-SI-02	21	Change HDMI HPD signal from low active to high active	Q38,R638,R639
EC-SI-03	21	Modify Q37 MOSFET gate power source from +5V to +3V	Q37
EC-SI-04	28	Swap EC GPIO for reserving 2nd fan control	
EC-SI-05	22	Separate L/R channels for spkeaker connector	CN26,CN27
EC-SI-06	20	Add ESD protection for CCD	
EC-SI-07	29	Reserve 2nd FAN	
EC-SI-08	49	Reserve 100pF for CN15 (EMI suggestion)	
EC-SI-09	31	Add 2 GND pad for EMI	
EC-SI-10	25	Change ODD connector	CN21
EC-SI-11	26	Change connector of card reader daughter board	CN24
EC-SI-12	13,34	Change load cap for 32.768K/24M/27M due to vendor suggest	
EC-SI-13	All	Stuff EMC/ESD/RF materials	
EC-SI-14	35	Unstuff R437 for correct PSI setting	R437
EC-SI-15	22	Change AL7/AL8/AL9/AL11 as 0ohm from Realtek suggest	AL7,AL8,AL9,AL11

N91 EE Schematic SI to PV Change List

EC#	Page	Description	Part Affected
EC-PV-01	All	Change 0ohm resistor to be short pad	
EC-PV-02	27	Remove reserved CMC of USB3.0	L28,L29,L30,L33

N91 Power Schematic DB to SI Change List

EC#	Page	Description	Part Affected
EC-SI-P01	38~51	Change default open to default short	PJP1~PJP22
EC-SI-P02	48,49,51	Downsize components	PR283, PR285, PC12, PC28, PC184, PC185, PC174, PL3
EC-SI-P03	50, 51	Correct connection	
EC-SI-P04	38,40,42,50	Fine tune OCP function	PR134, PR135, PR101, PR21, PR70
EC-SI-P05	50	Change choke for transient	PL15
EC-SI-P06	40,51	Fine tune offset voltage	PR97, PR186
EC-SI-P07	38, 50	Change components for ripple voltage	PL21, PC72
EC-SI-P08	38,39	Add components for PG function	PR137, PR122
EC-SI-P09	39,40,45~47,50,51	Change components for common part using	PU6, PQ10, PQ13, PQ14, PQ49, PQ50, PR408~PR412, PR254, PR252, PQ4, PQ5, PQ26, PR172
EC-SI-P10	50	Fine tune soft start	PR76, PC243
EC-SI-P11	43	Add components for Efficiency	PQ19, PQ23
EC-SI-P12	42	Fine tune DVID setting	PR210, PR22
EC-SI-P13	42	Fine tune Iout function	PR205, PR209, PC54, PC204
EC-SI-P14	42	Fine tune compensation	PR31, PC205

N91 EE Schematic SI to PV Change List

EC#	Page	Description	Part Affected
EC-PV-P01	All	Change 0ohm resistor to short pad	
EC-PV-P02	42	Fine tune +VCCGT load line	PR14
EC-PV-P03	42	Fine tune +VCCGT Iout function	PR195
EC-PV-P04	42	Fine tune Vcore OCP	PR208
EC-PV-P05	42	Fine tune Vcore Iout function	PR209
EC-PV-P06	42	Fine tune Vcore Loadline	PR212,PR214