MS-7680 Ver: 7.1 m-ATX : 243.84 X 228mm

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(H61)

OnBoard Chipset:

HD Audio Codec:RTL887 Co-lay 892
LAN:RTL 8111E 10/100/1000 , Co-lay 8105E 10/100
SIO:FIN71869AD
Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 3

PWM:

Controller:VRD12 UT501 3Phase
CPU+GPU: UP6282 MOSFET Driver
CPU VTT: IP6103
CPU SA : OP+MOS
DDR: UP6103
PCH: OP+MOS

ACPI:

UPI

Other:

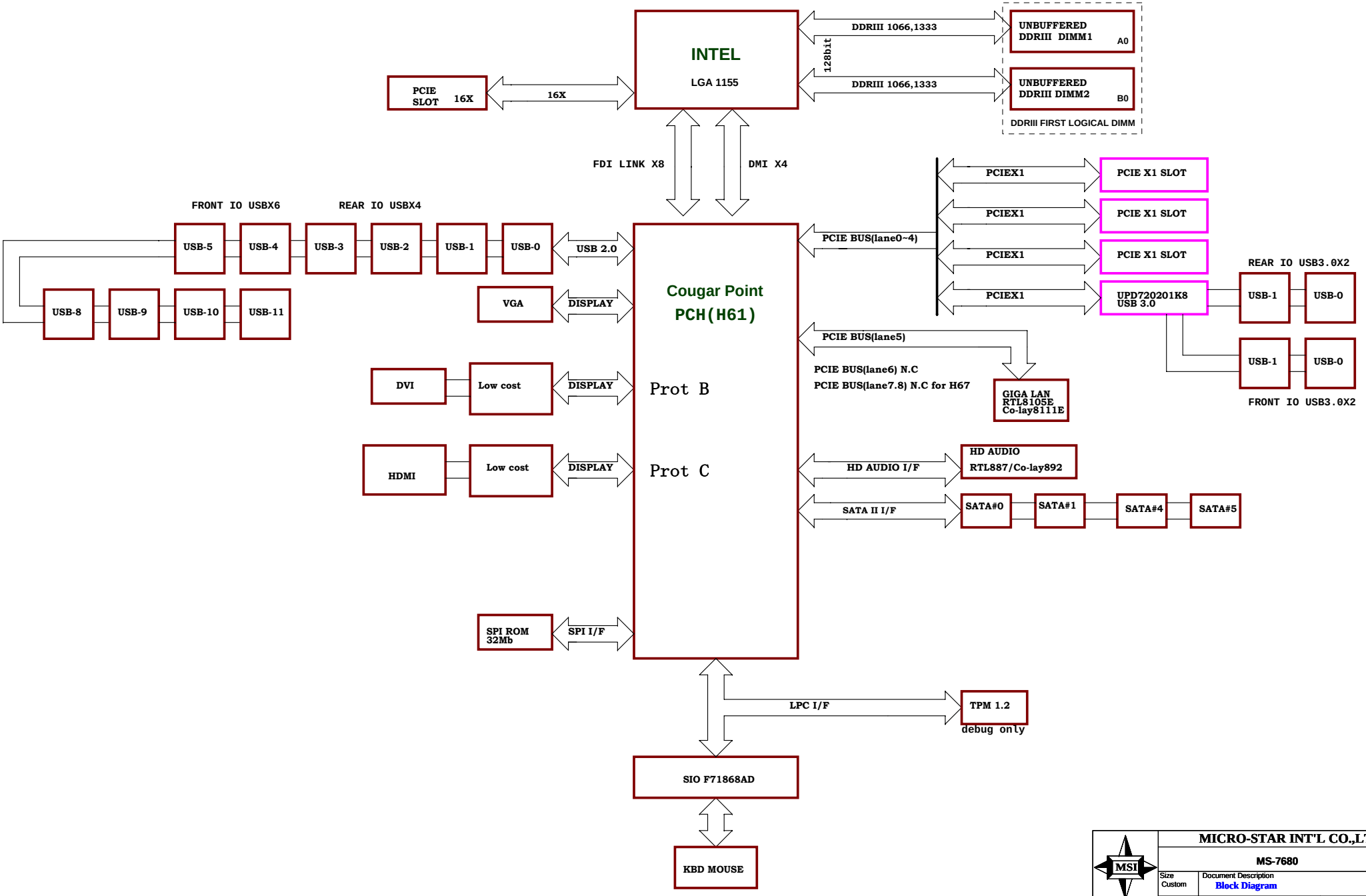
SATA2.0 x4 (PCH)
USB2.0 RearX4 Front x6
USB3.0 RearX2 FrontX2
D-SUB/DVI/HDMI *1
TPM Header *1(debug only)
on BOARD BUZZER

MICRO-STAR INT'L CO.,LTD

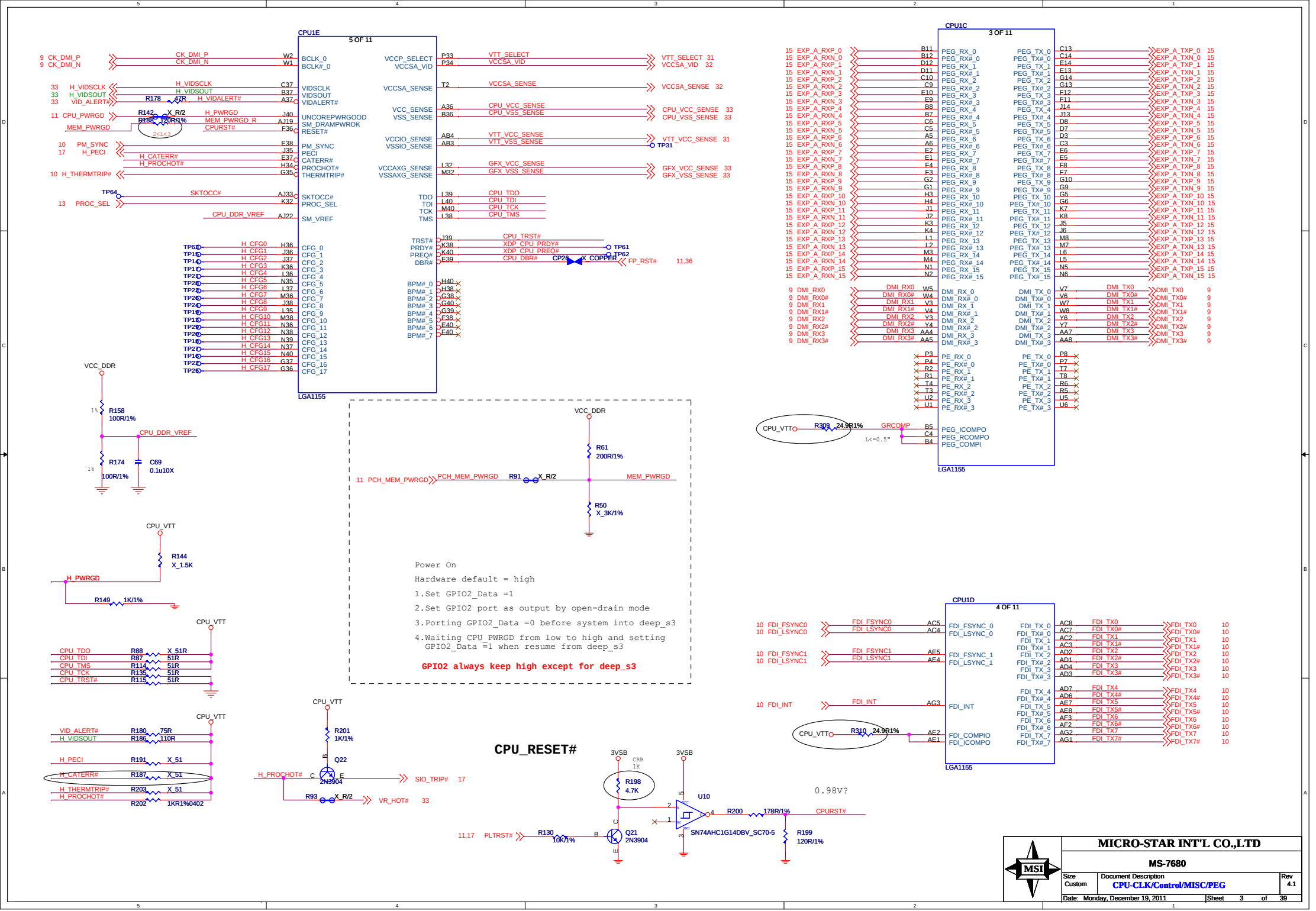
MS-7680

Size	Document Description	Rev
Custom	Cover Sheet	7.0

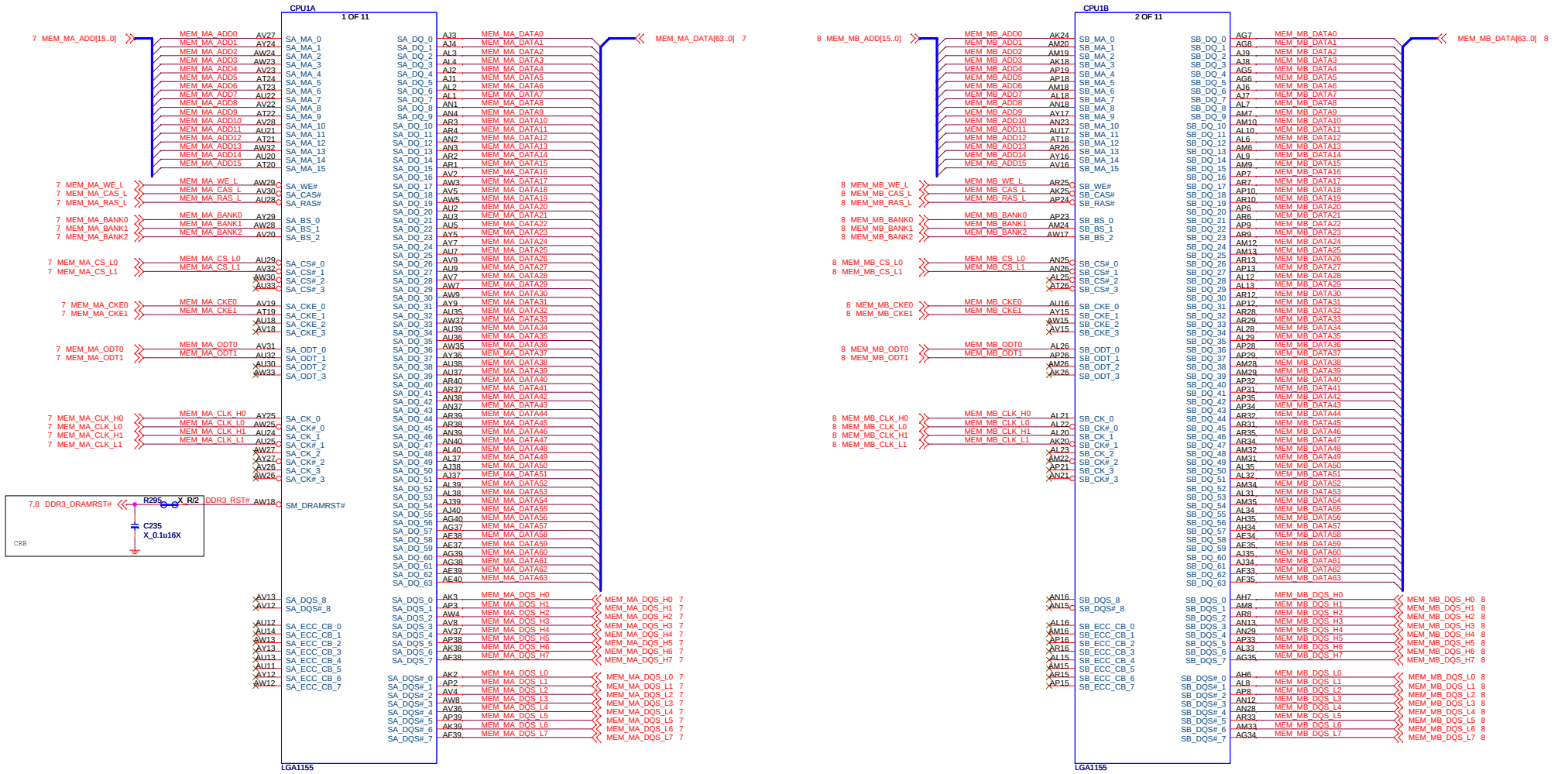
Date: Thursday, January 12, 2012 Sheet 1 of 39



MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size: Custom	Document Description: Block Diagram	Rev: 7.0
Date: Monday, December 19, 2011	Sheet 2 of 39	



MICRO-STAR INT'L CO.,LTD	
MS-7680	
Size: Custom	Document Description: CPU-CLK/Control/MISC/PEG
Rev: 4.1	
Date: Monday, December 19, 2011	Sheet 3 of 39



MSI	MICRO-STAR INT'L CO.,LTD		
	MS-7680		
Size: Custom	Document Description: CPU-Memory		Rev: 4.1
Date: Monday, December 19, 2011		Sheet 4 of 39	

(1.05V / 1.00V)

(0.925V / 0.85V)

VCCP: 112A
CPU_VTT: 8.2A
CPU_SA: 8.8A
VCC_DDR: 4.5A
VCC1_8: 1.6A

+CPU_GFX Decoupling

CPU SOCKET CAVITY CAPS

Backside

+1.5V_DDR3-Decoupling

2011.11.14 modify

CPU SOCKET CAVITY CAPS

Backside

Backside

+CPU_VTT Decoupling

CPU SOCKET CAVITY CAPS

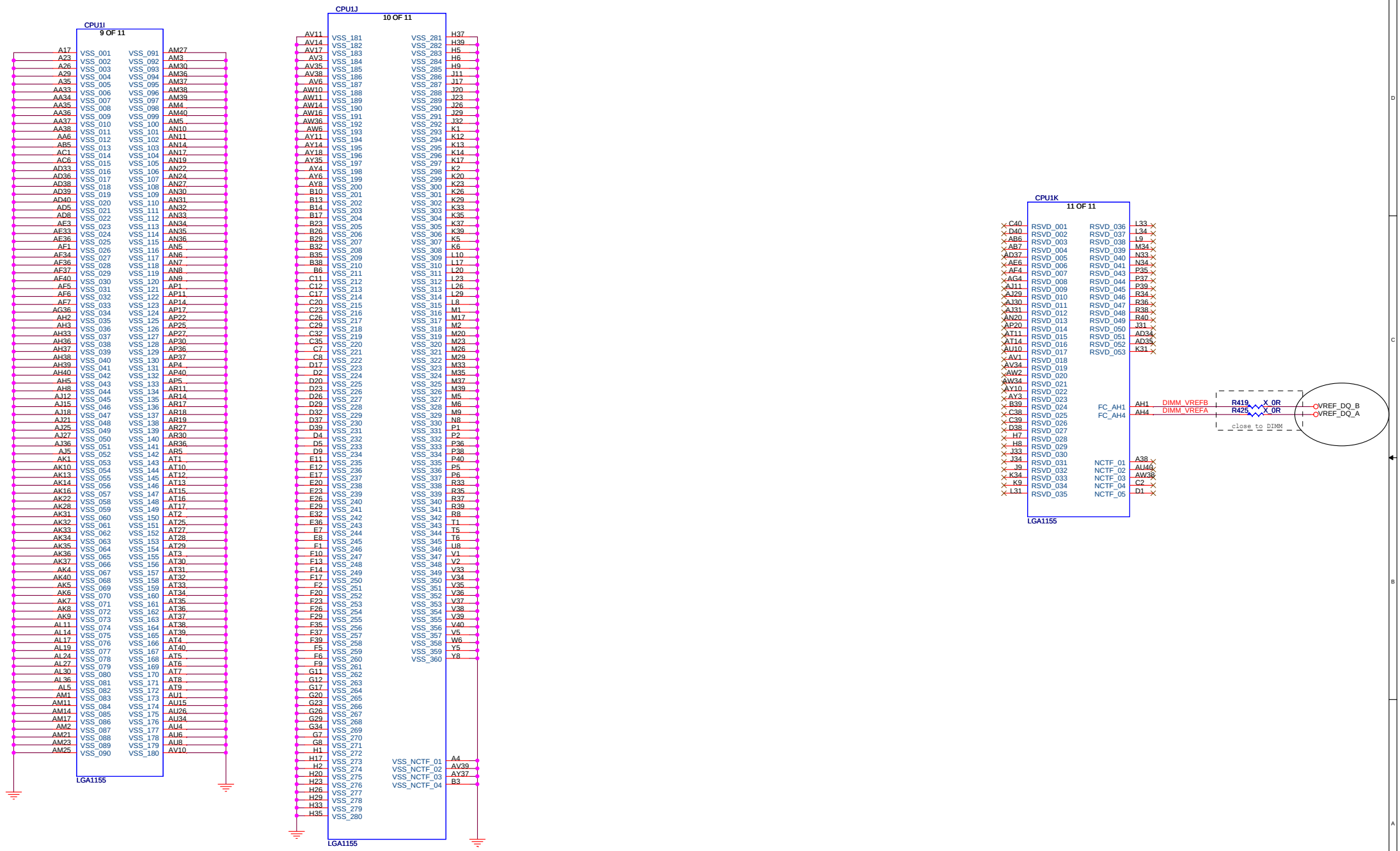
Backside

+CPU_VCCP-Decoupling

PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY

Backside

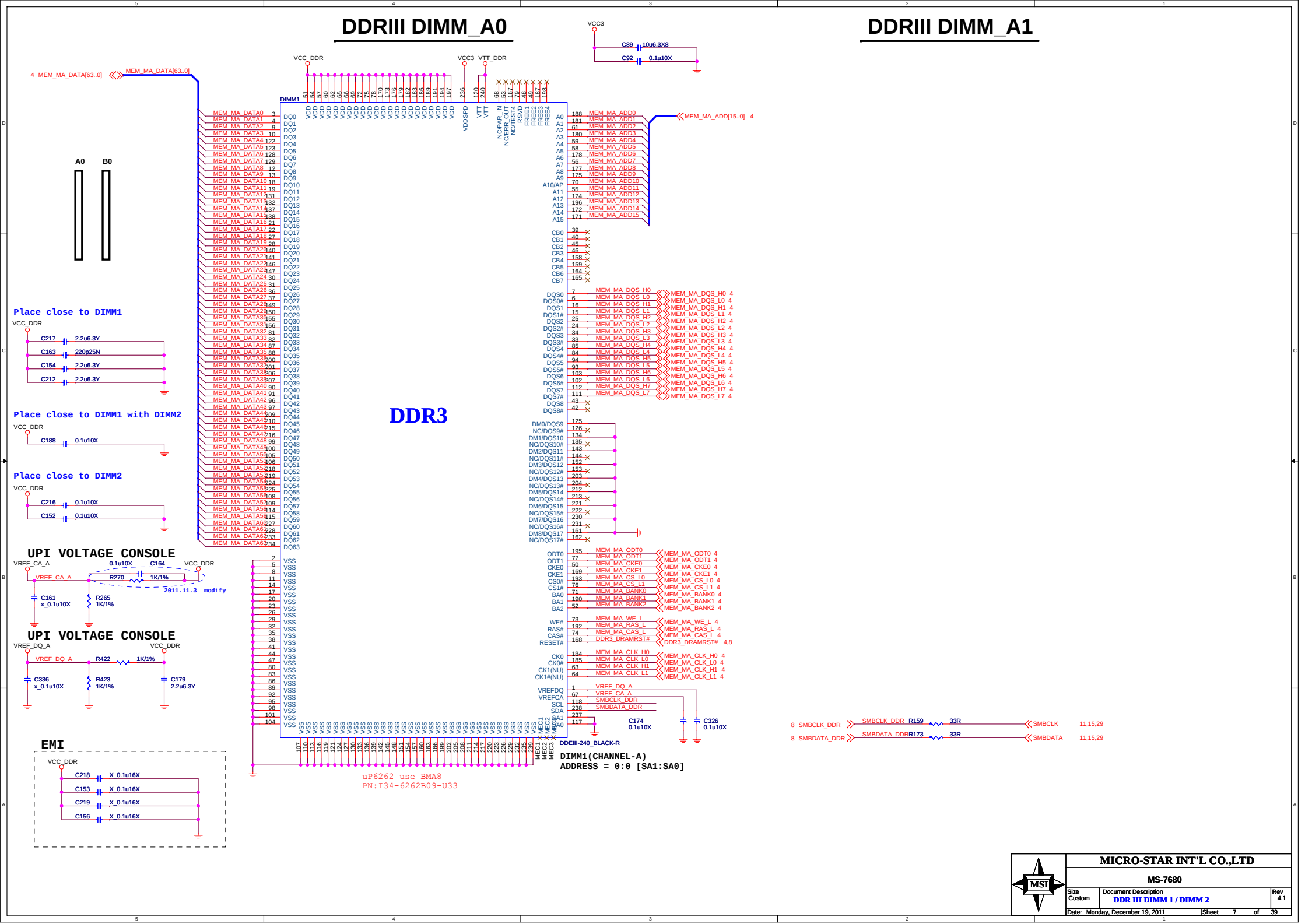
MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size: Custom	Document Description: CPU-Power	Rev: 4.1
Date: Monday, January 09, 2012	Sheet 5 of 39	



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7680	
Size: Custom	Document Description: CPU-GND	Rev: 4.1
Date: Monday, December 19, 2011	Sheet 6 of 39	

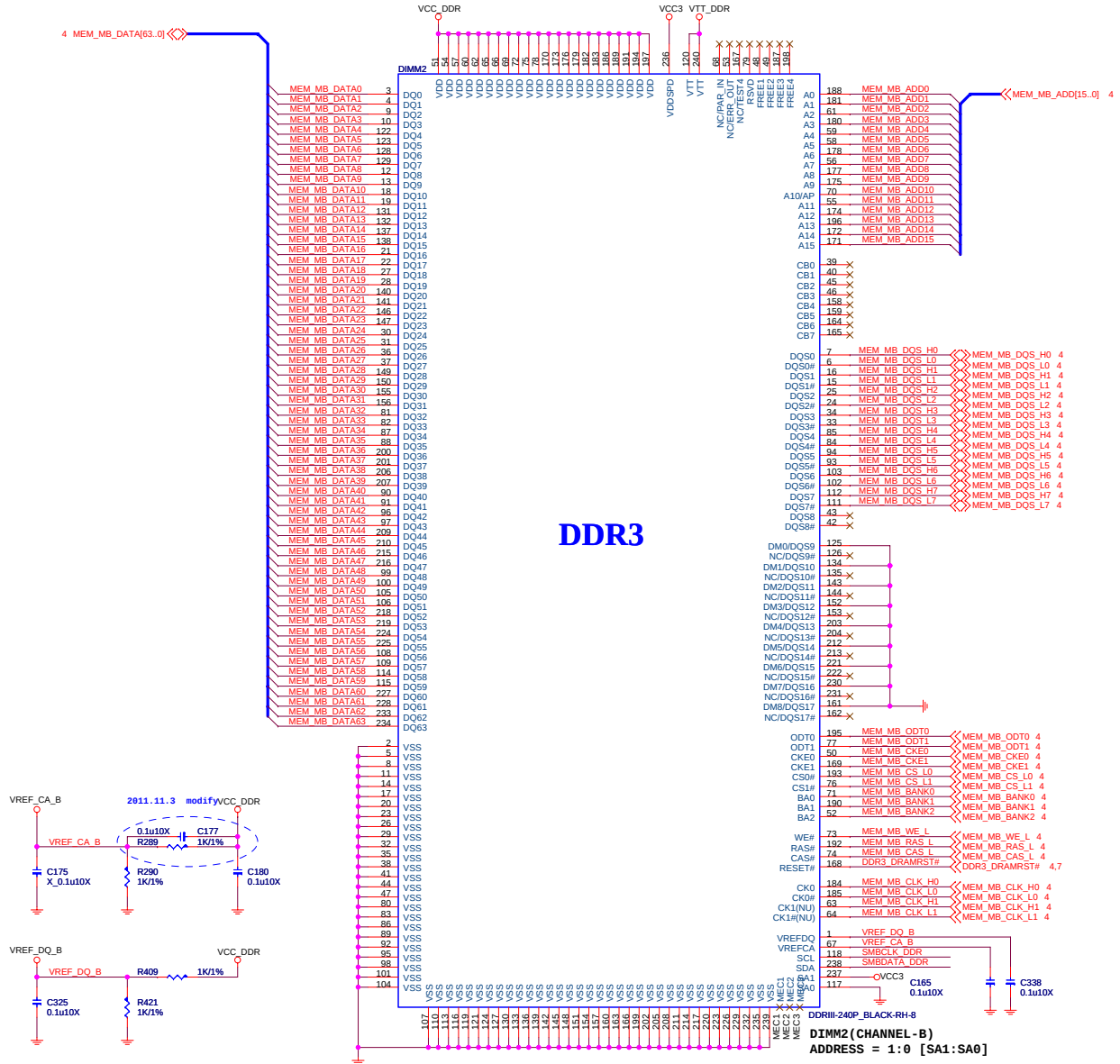
DDRIII DIMM_A0

DDRIII DIMM_A1

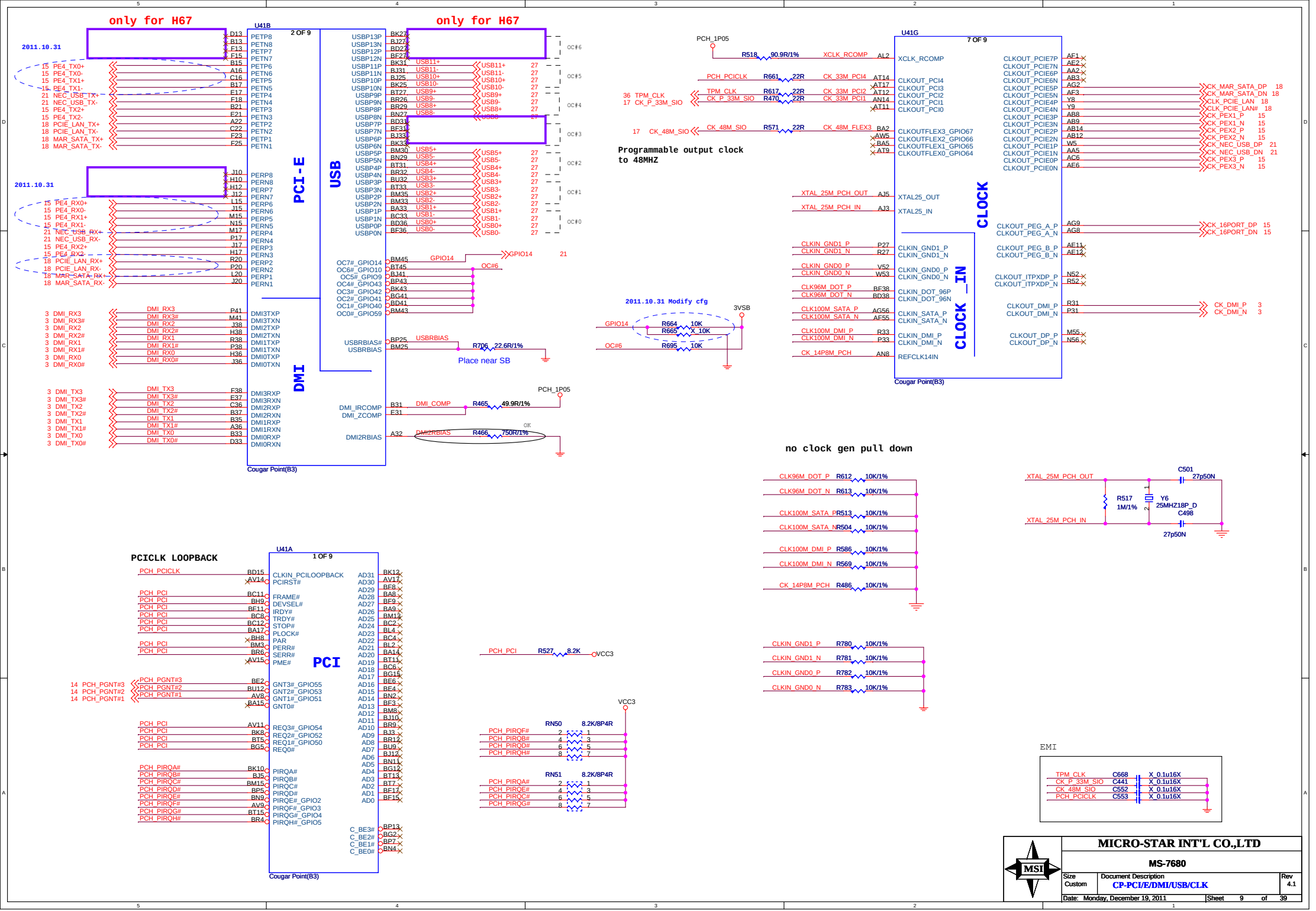


MICRO-STAR INT'L CO.,LTD	
MS-7680	
Size: Custom	Document Description: DDR III DIMM 1 / DIMM 2
Rev: 4.1	
Date: Monday, December 19, 2011	Sheet 7 of 39

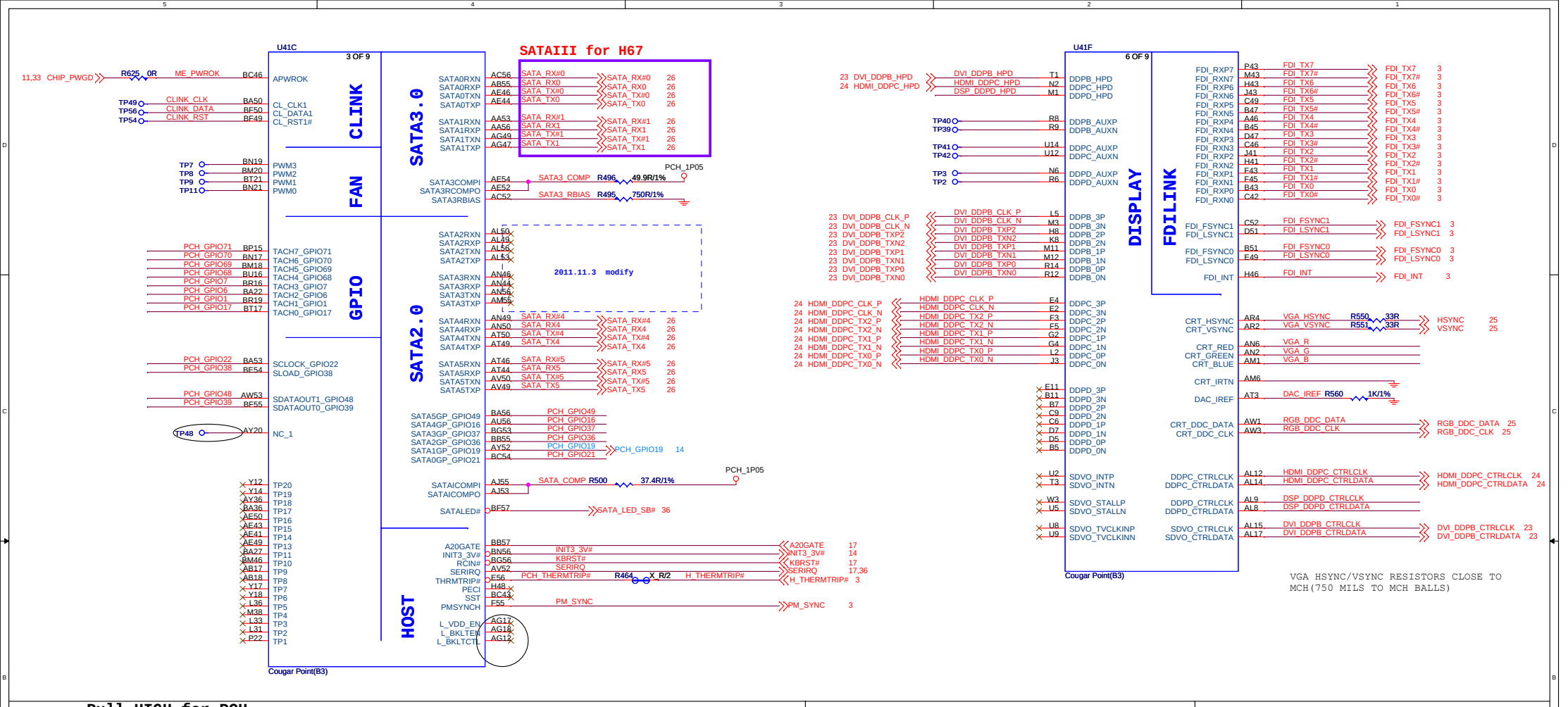
DDRIII DIMM_B0

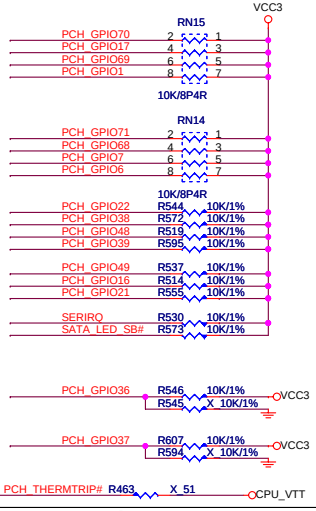


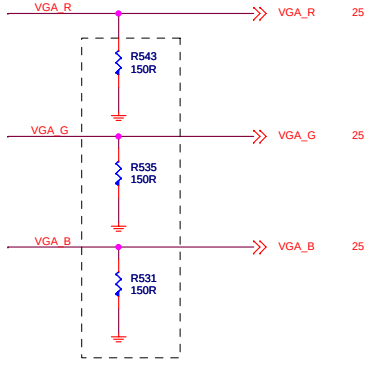
MICRO-STAR INT'L CO.,LTD	
MS-7680	
Size: Custom	Document Description: DDR III DIMM 3 / DIMM 4
Rev: 4.1	
Date: Monday, December 19, 2011	Sheet 8 of 39

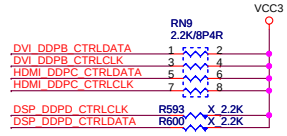


MICRO-STAR INT'L CO.,LTD	
MS-7680	
Size: Custom	Document Description: CP-PCI/E/DMI/USB/CLK
Rev: 4.1	
Date: Monday, December 19, 2011	Sheet 9 of 39



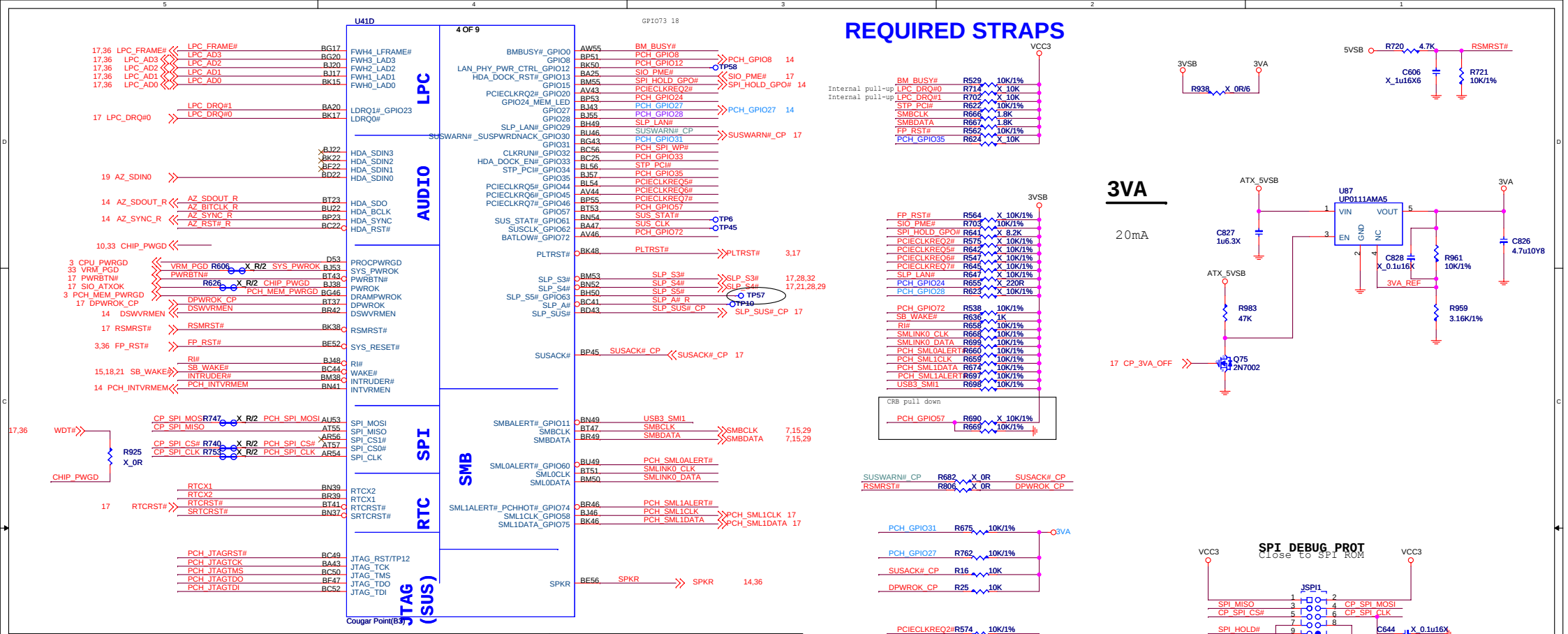






MICRO-STAR INT'L CO.,LTD	
MS-7680	
Size: Custom	Document Description: CP-SATA/HOST/FAN/GPIO/VGA
Rev: 4.1	
Date: Monday, December 19, 2011	Sheet 10 of 39

REQUIRED STRAPS



PCIECLKREQ can't find 0/1/3/4

3VA

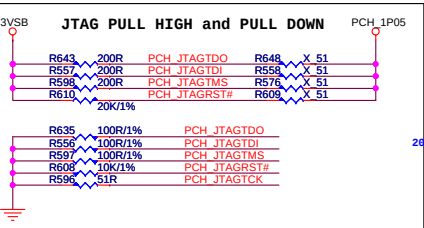
20mA

SPI DEBUG PROT

Close to SPI ROM

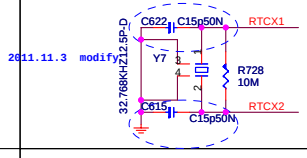
Part Number:N31-2051451-H06

JTAG PULL HIGH and PULL DOWN

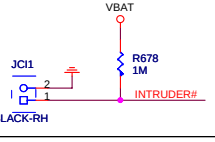


RTC Block

Close to PCH

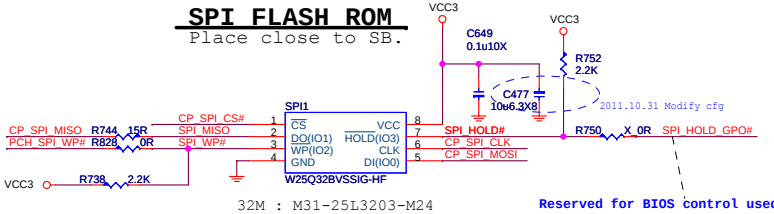


Chassis Intrusion



SPI FLASH ROM

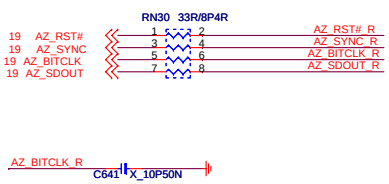
Place close to SB.



32M : M31-25L3203-M24

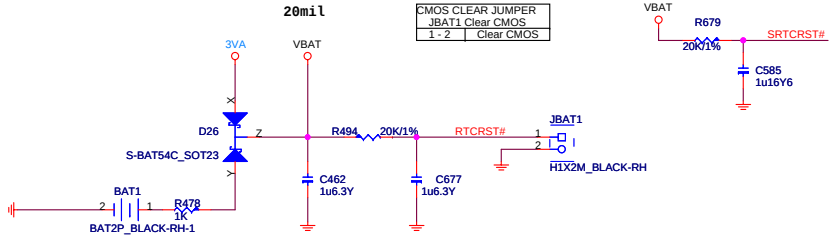
Reserved for BIOS control used

33 Ohm series near PCH



RTC and CLR_CMOS

Clear CMOS



N91-01F0151-H06

MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size: Custom	Document Description: CP-SMB/LPC/AUDIO/RTC	Rev: 4.1
Date: Monday, December 19, 2011	Sheet 11 of 39	

Reserved for BIOS control used

Change to 10UH if
VCCA_DPLLA/VCCA_DPLLB
has noise issue.

PCH_1P05

R460 X_0/8 VCCAFDIPLL
C415 10u6.3X8

R526 X_0R VCCACLK
NO THIS PIN

R461 X_0/8 VCCAPLLDMI2
C417 10u6.3X8
C426 1u6.3X

R567 0R/8 VCCCLKDMI
C550 10u6.3X8
C551 1u6.3X

R475 0R/8 VCCA_DPLLA
EC46 100u16SO
C460 X_22u6.3X8
C472 1u6.3X

R515 0R/8 VCCA_DPLLB
EC47 100u16SO
C474 X_22u6.3X8
C475 1u6.3X

PCH_1P05

DMI PLL FILTER

L23 X_L1U_500mA_0805 VCCAPLLEXP
C420 X_10u6.3X8
C427 1u6.3X

SATA PLL FILTER

L24 X_L10U_100mA_0805 VCCAPLLSATA
C459 X_10u6.3X8
C464 1u6.3X

PCH_1P05

U41H
8 OF 9
Cougar Point(B3)

CPU_VTT D55 V_PROC_IO
CPU_VTT B56 V_PROC_IO_NCTF
B41 VCCDMI_02
E41 VCCDMI_01
C429 1u6.3X
VCCAPLLDMI2 A19 VCCAPLLDMI2
VCCCLKDMI AJ20 VCCCLKDMI
5VREF BF1 V5REF
5VREF_SUS BT25 V5REF_SUS
+3.3V_DAC AT1 VCCADAC
VCCACLK AL5 VCCACLK
VCCA_DPLLA AB1 VCCADPLLA
VCCA_DPLLB AC2 VCCADPLLB
VCCAPLLSATA U56 VCCAPLLSATA
VCCAPLLEXP B53 VCCAPLLEXP
VCCAFDIPLL C54 VCCAFDIPLL
3VSB AV28 VCCSUSHDA
VCC3 AN52 VCCSPI
VCC1_8 CP24 X_COPPER R2 VCCVRM_04
R54 VCCVRM_03
R56 VCCVRM_02
AJ1 VCCVRM_01
C428 1u6.3X DCPSUS A39 DCPSUS_03
TP44 AT41 DCPSUS_02
TP43 AA32 DCPSUS_01
C583 0.1u10X DCPRTC BR54 DCPRTC
BT56 DCPRTC_NCTF
TP51 AV41 DCPSUSBYP
C521 0.1u10X DCPSST BA46 DCPSST
VBAT BU42 VCCRTC
AV40 VCCDSW3_3
3VA C720 X_0.1u10X
PCH_1P05 AG15 VCCDIFFCLKN_03
AE17 VCCDIFFCLKN_02
AE15 VCCDIFFCLKN_01
PCH_1P05 CP7 X_COPPER VCCSSC
VCCNAND
VCC1_8 CP23 X_COPPER
C457 X_0.1u10X

Backside

PCH_1P05: 7.66A
CPU_VTT: 0.058A
VCC1_8: 0.159A
VCC3: 0.697A
3VSB: 0.11A
5VREF: 0.001A
5VREF_SUS: 0.001A

POWER

PCH_1P05
VCCCORE_022 AR34
VCCCORE_021 AR32
VCCCORE_020 AN34
VCCCORE_019 AN32
VCCCORE_018 AL34
VCCCORE_017 AL32
VCCCORE_016 AJ36
VCCCORE_015 AJ34
VCCCORE_014 AJ32
VCCCORE_013 AG34
VCCCORE_012 AG32
VCCCORE_011 AE36
VCCCORE_010 AE34
VCCCORE_009 AE32
VCCCORE_008 AE30
VCCCORE_007 AE28
VCCCORE_006 AE24
VCCCORE_005 AC32
VCCCORE_004 AC30
VCCCORE_003 AC28
VCCCORE_002 AC26
VCCCORE_001 AC24

VCCASW_023 AU36
VCCASW_022 AU30
VCCASW_021 AR38
VCCASW_020 AR36
VCCASW_019 AR30
VCCASW_018 AR28
VCCASW_017 AR26
VCCASW_016 AR24
VCCASW_015 AN28
VCCASW_014 AN26
VCCASW_013 AN24
VCCASW_012 AN22
VCCASW_011 AL28
VCCASW_010 AL24
VCCASW_009 AJ28
VCCASW_008 AJ26
VCCASW_007 AJ24
VCCASW_006 AG28
VCCASW_005 AG26
VCCASW_004 AG24
VCCASW_003 AU34
VCCASW_002 AV36
VCCASW_001 AU32

3VSB

VCC3

5VREF & 5VREF_SUS Sequencing Circuit

VCC3 Q76 2N3904 C569 1u6.3X
VCC5 R637 10R 5VREF C568 0.1u10X

3VSB Q81 2N3904 C604 0.1u10X
5VSB R715 100R/1% 5VREF_SUS C600 0.1u10X

VCC3 CP5 X_COPPER +3.3V_DAC
Near ball AF1
C538 0.1u10X
3VSB C592 C598 0.1u10X
0.1u10X

PCH decoupling cap

PCH_1P05
C401 0.1u10X
C434 0.1u10X
C439 1u10Y6
C404 10u6.3X8
C418 10u6.3X8
C419 10u6.3X8
C458 4.7u10X8
C406 0.1u10X

VBAT
C603 0.1u10X
C609 1u10Y6

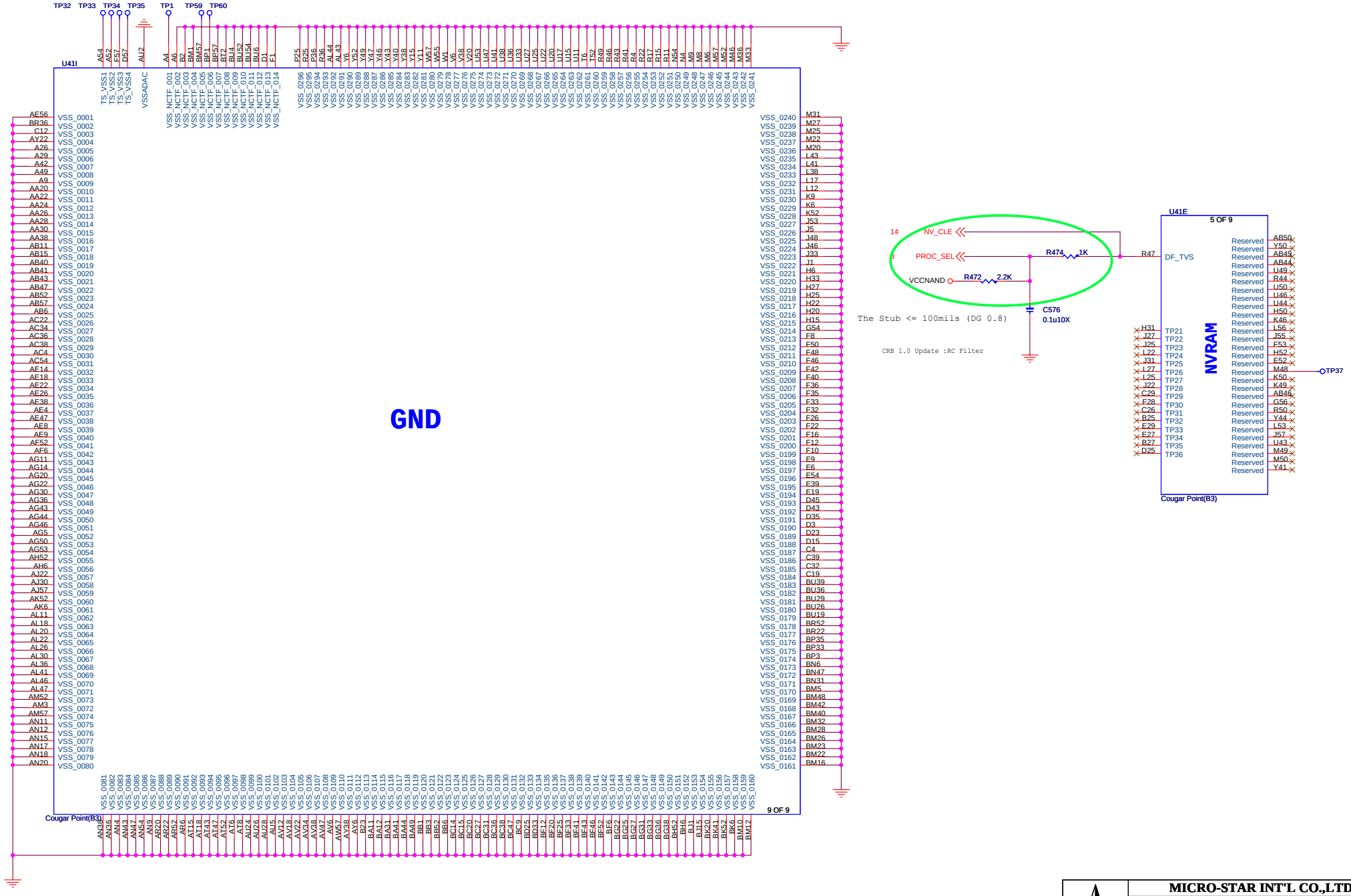
VCC3
C479 0.1u10X
C580 X_0.1u10X
C489 X_0.1u10X
C431 X_0.1u10X
C542 0.1u10X

CPU_VTT
C413 4.7u10X8
C423 0.1u10X
C430 0.1u10X

Backside

PCH_1P05
C712 X_1u10Y6
C716 X_1u10Y6
C717 X_10u6.3X8
C715 X_1u10Y6
C713 X_0.1u10X
C719 X_0.1u10X
C718 X_0.1u10X
C714 X_0.1u10X

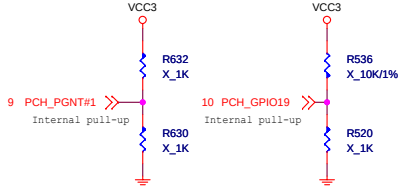
MICRO-STAR INT'L CO.,LTD
MS-7680
Size: Custom
Document Description: CP-POWER
Rev: 4.1
Date: Monday, January 09, 2012
Sheet 12 of 39

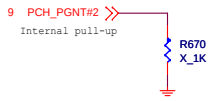


MICRO-STAR INT'L CO.,LTD			
MS-7680			
Size: Custom	Document Description: CP-GND/NVRAM		Rev: 4.1
Date: Monday, December 19, 2011		Sheet 13 of 39	

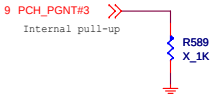
PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

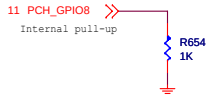




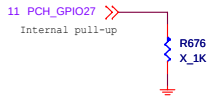
DMI AC/DC MODE
0 : AC
1 : DC *



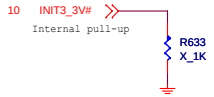
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

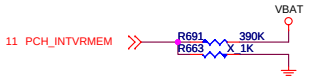


GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INT3_3V#
0 : ??????????????
1 : ??????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

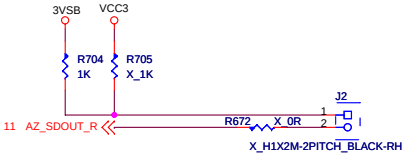


INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltageregulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

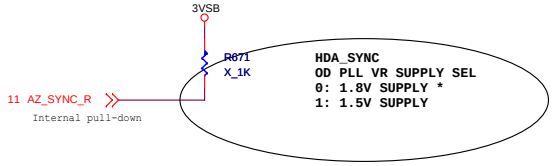
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.



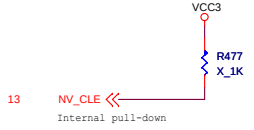
HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high

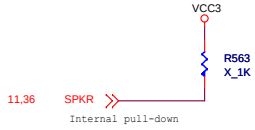


HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

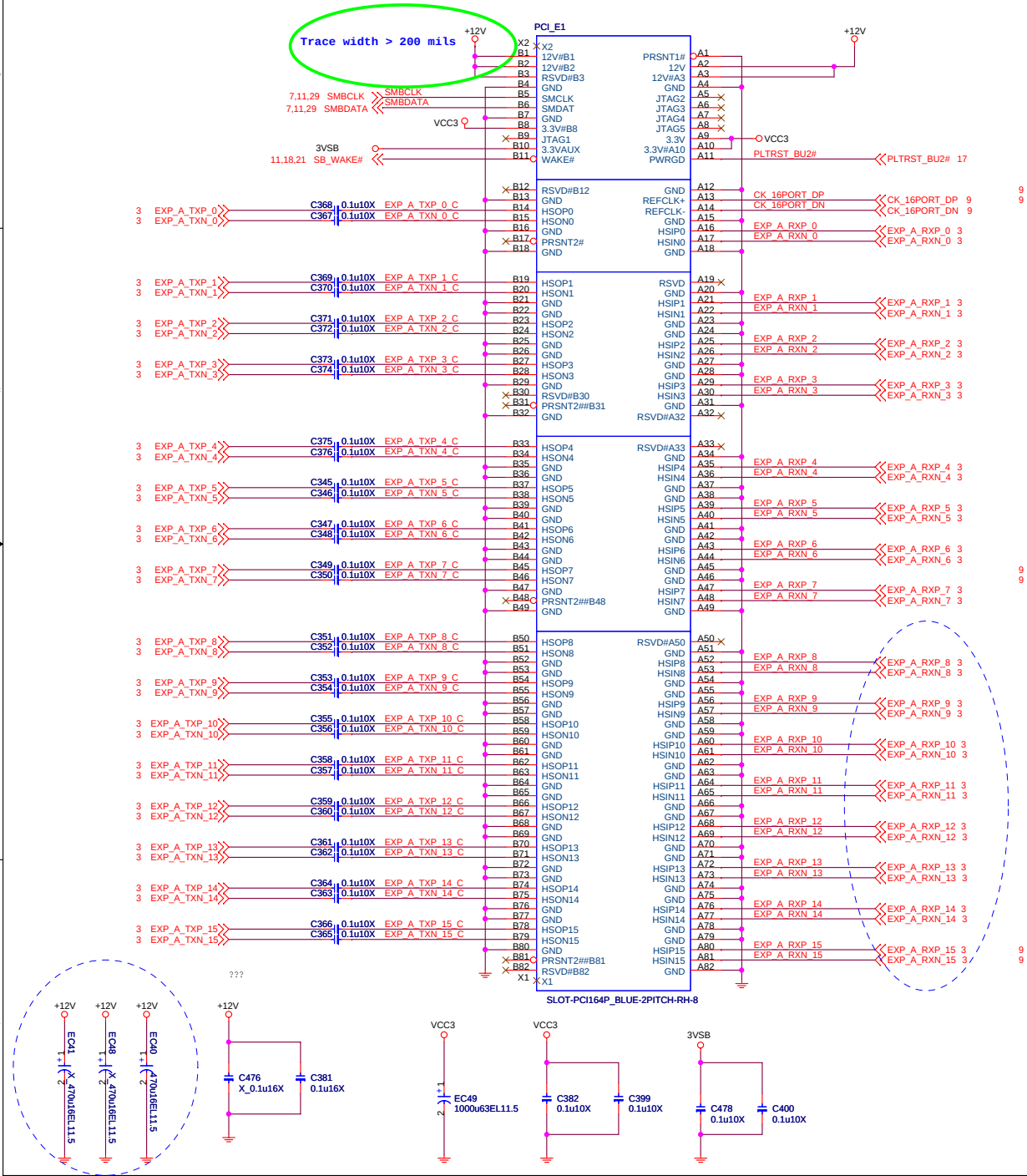
MICRO-STAR INT'L CO.,LTD

MS-7680

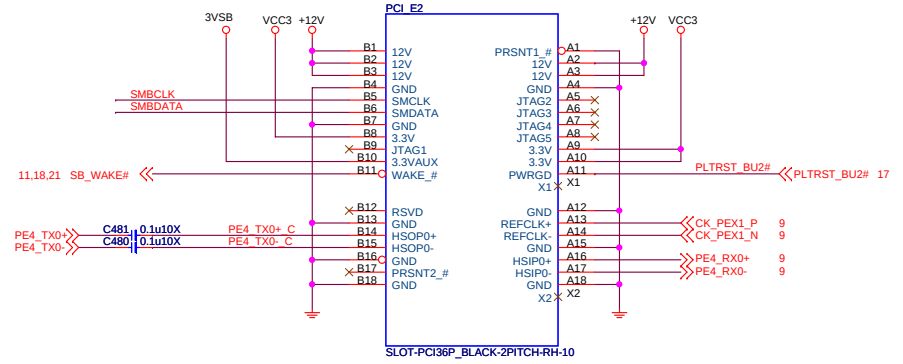
Size	Document Description	Rev
Custom	CP-Strap	4.1

Date: Monday, December 19, 2011 Sheet 14 of 39

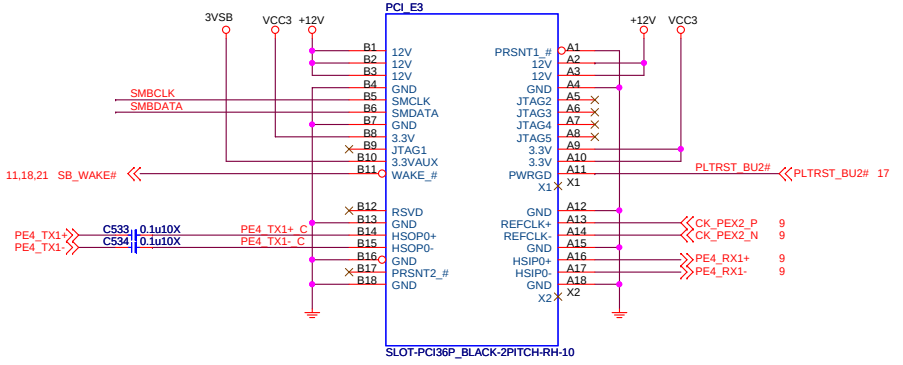
PCI_Express X16 Slot



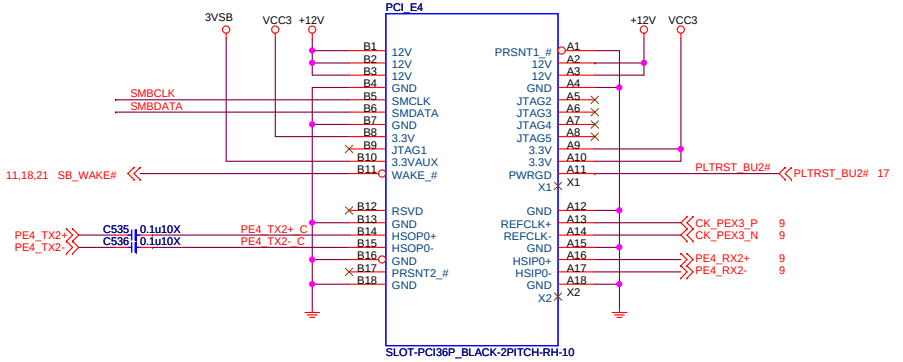
PCI EXPRESS x1-PORT



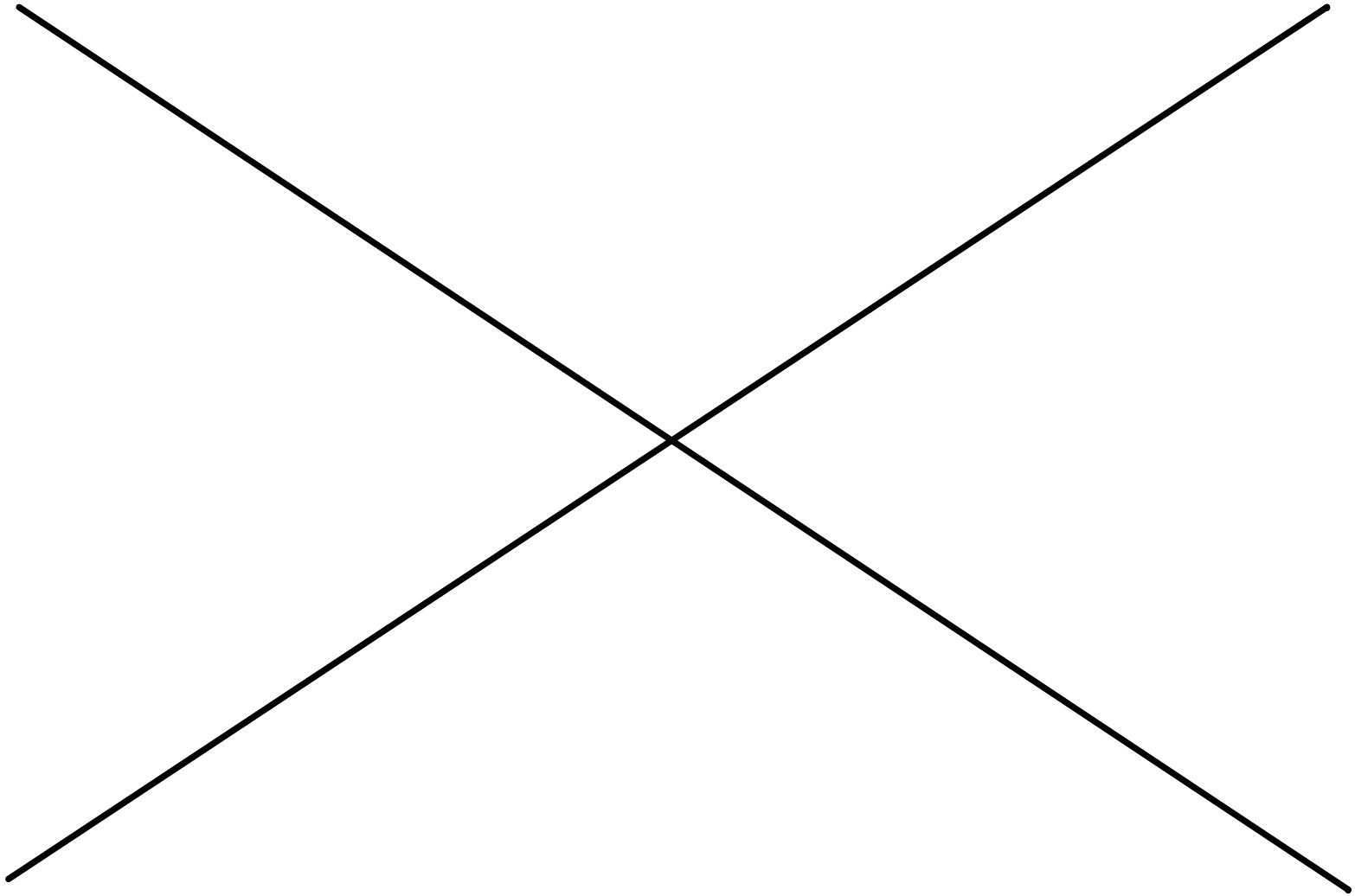
PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT



MICRO-STAR INT'L CO.,LTD	
MS-7680	
Size: Custom	Document Description: PCIE x16 /x1/x1
Rev: 4.1	
Date: Monday, December 19, 2011	Sheet 15 of 39

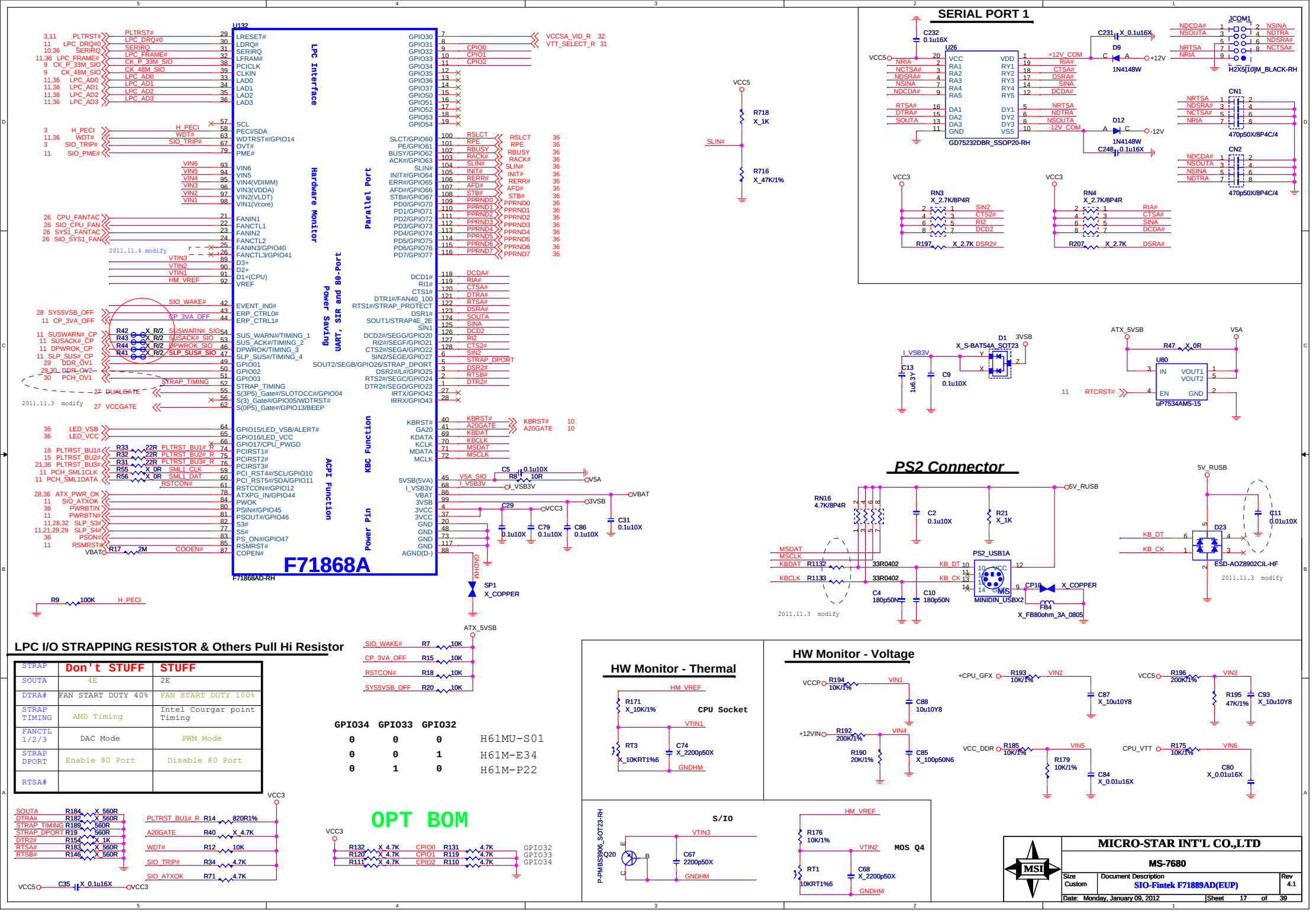


MICRO-STAR INT'L CO.,LTD

MS-7680

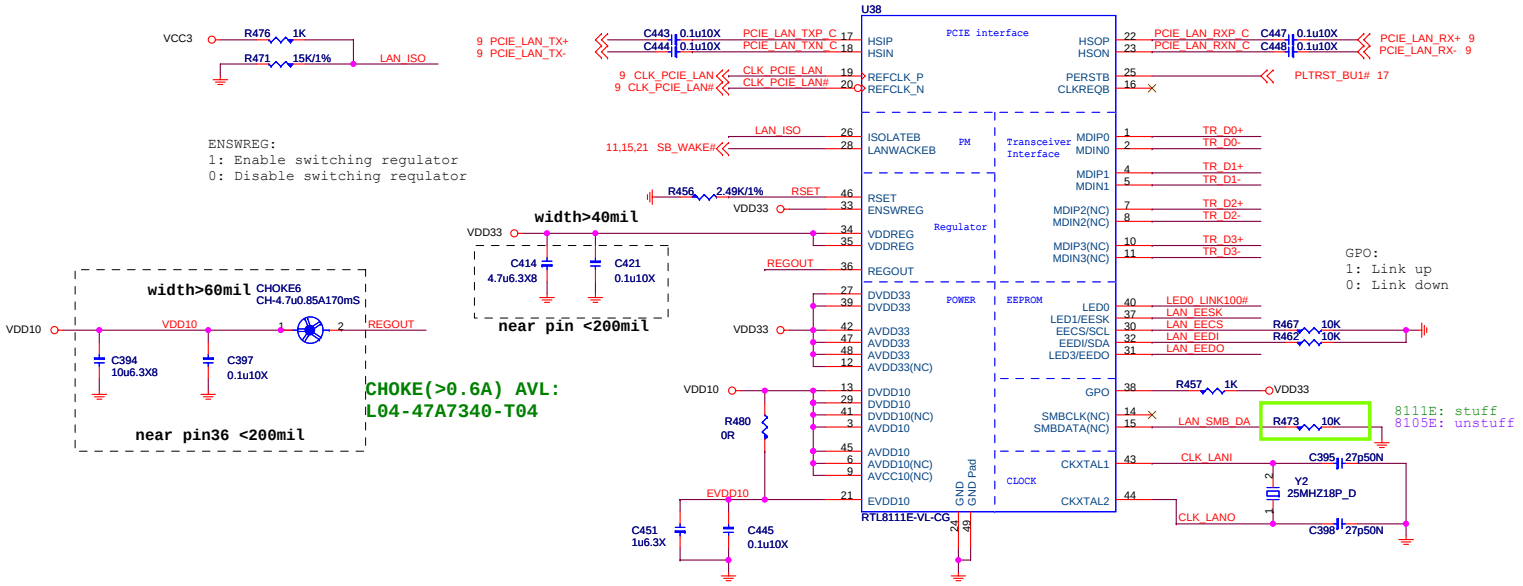
Size	Document Description	Rev
Custom	PCIx1 Slots	4.1

Date: Monday, December 19, 2011 | Sheet 16 of 39


SERIAL PORT 1
F71868A
F71868AD-RH
LPC Interface
Hardware Monitor
Parallel Port
Power Saving
UART, SIR and 80-Port
KBC Function
ACPI Function
Power Pin
PS2 Connector
LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor
STRAP
Don't STUFF
STUFF
SOUTA
4E
2E
DTRA#
FAN START DUTY 40%
FAN START DUTY 100%
STRAP TIMING
AMD Timing
Intel Courgar point Timing
FANCTL 1/2/3
DAC Mode
PWM Mode
STRAP DPORT
Enable 80 Port
Disable 80 Port
RTSA#
GPIO34 GPIO33 GPIO32
0 0 0 H61MU-S01
0 0 1 H61M-E34
0 1 0 H61M-P22
OPT BOM
HW Monitor - Thermal
CPU Socket
HW Monitor - Voltage
S/IO
MOS Q4
MICRO-STAR INT'L CO.,LTD
MS-7680
SIO-Fintek F71889AD(EUP)
Rev 4.1
Monday, January 09, 2012
Sheet 17 of 39

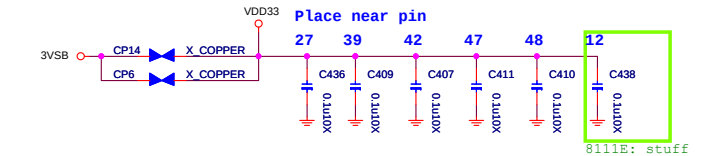
RTL8111E Giga LAN

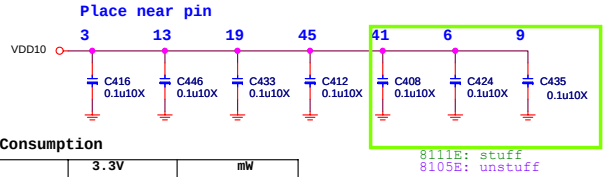
RTL8105E 10/100M LAN

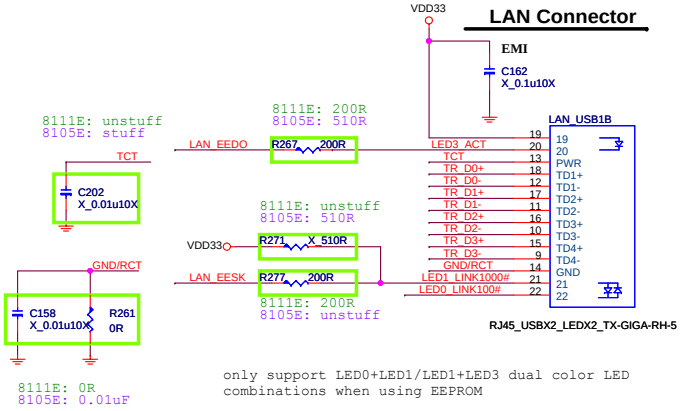


Pin49: 9 via from top layer to GND layer and make the via at the center of IC.

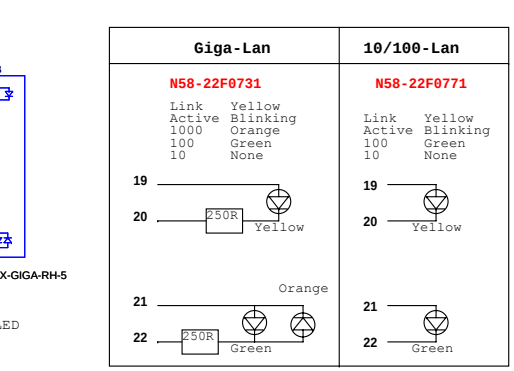
3.3v Power on rise time : 1~100ms. MAX: 163mA

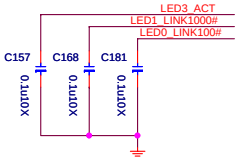






Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Yellow Active Blinking 1000 Orange 100 Green 10 None	Link Yellow Active Blinking 100 Green 10 None





8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

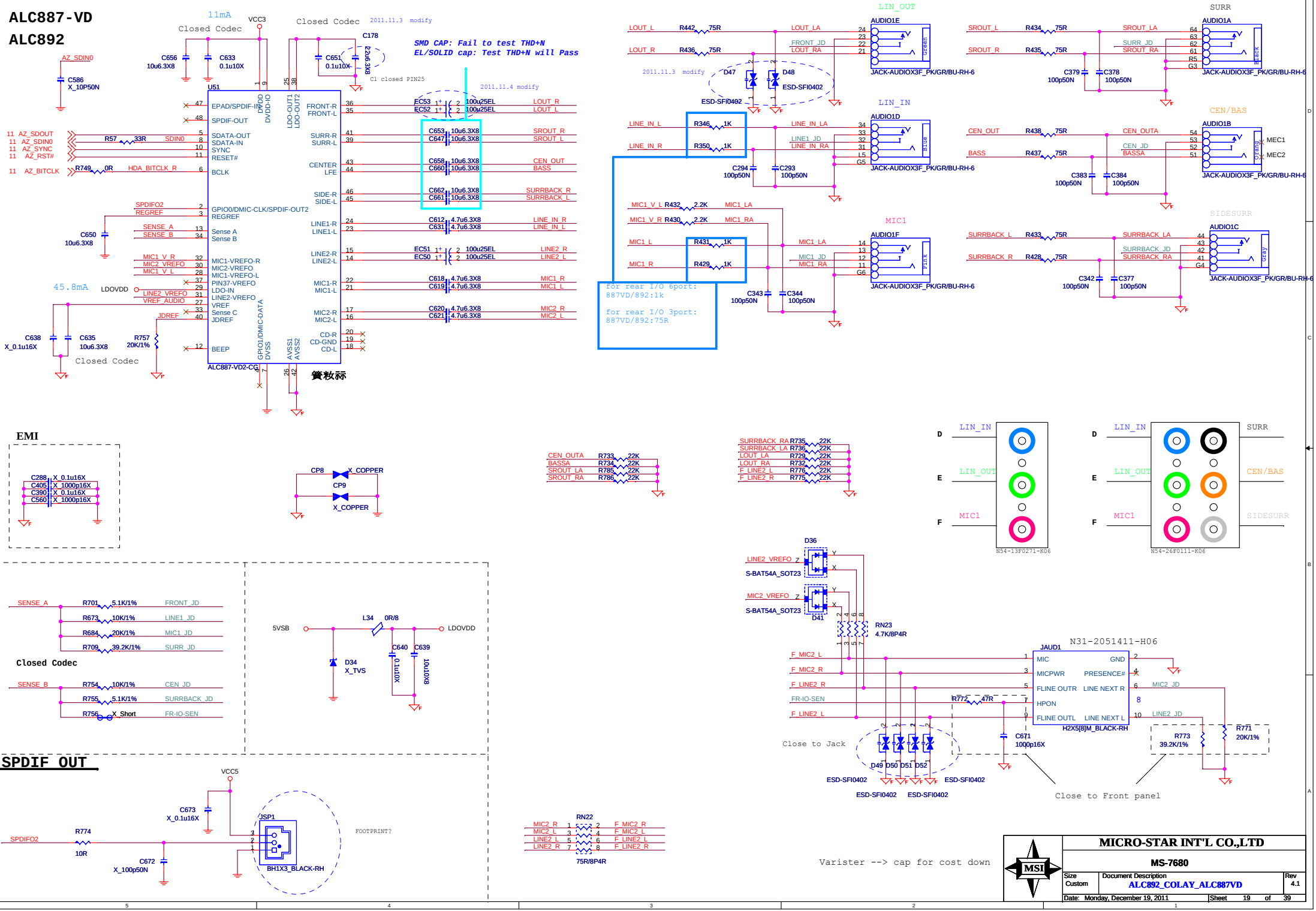
MICRO-STAR INT'L CO.,LTD

MS-7680

Size	Document Description	Rev
Custom	LAN - RTL8111E / 8105E	4.1

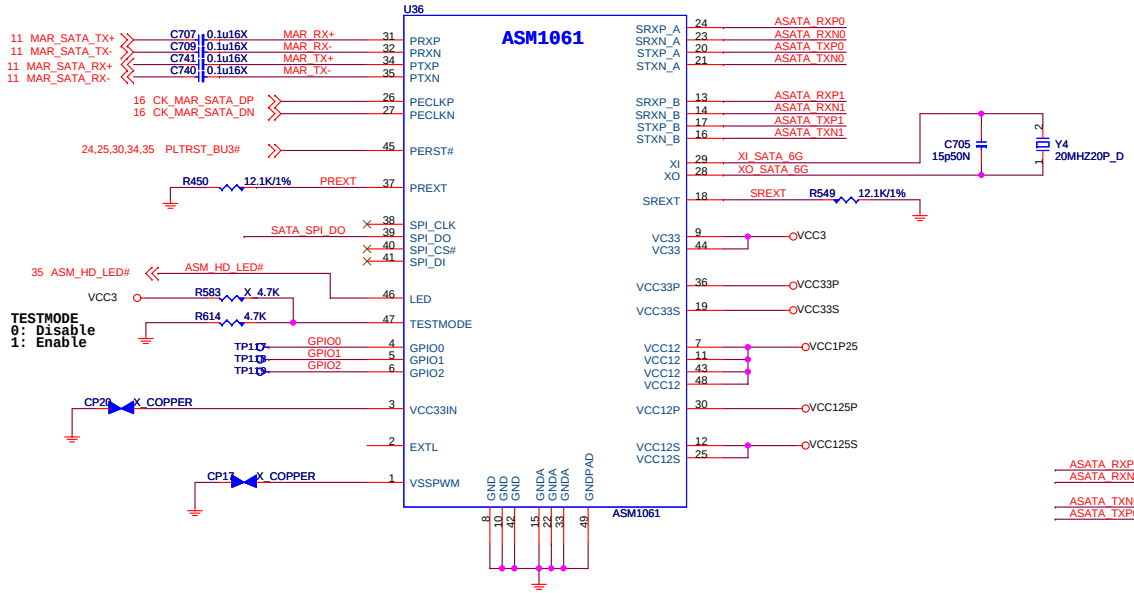
Date: Monday, December 19, 2011 Sheet 18 of 39

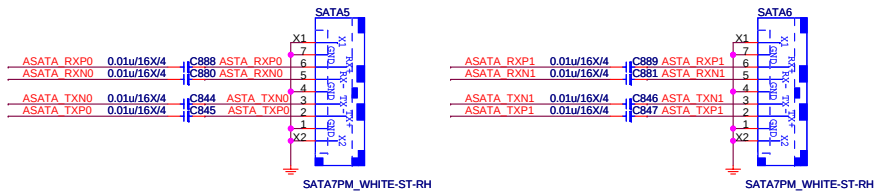
ALC887-VD
ALC892



ASM1061 SATA6G

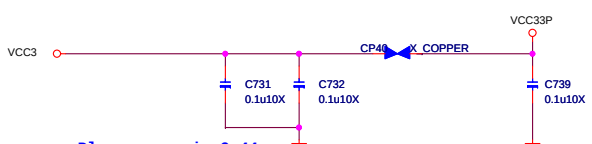
SATA 6G

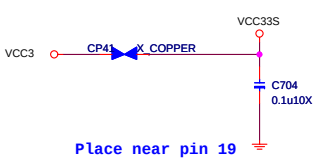


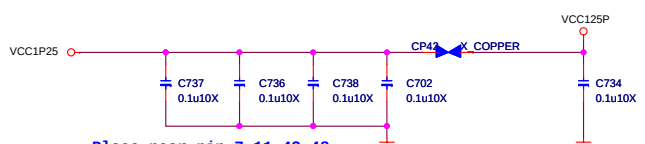


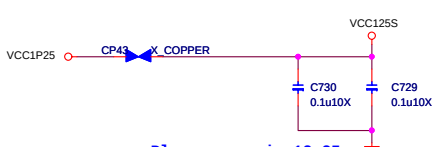
ASM1061 POWER Consumption

	3.3V	1.2V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47

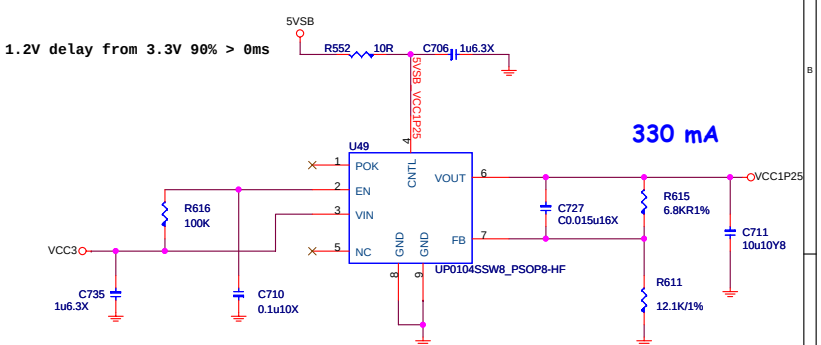


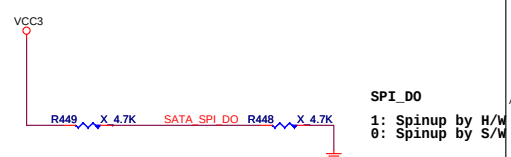






1.2V delay from 3.3V 90% > 0ms



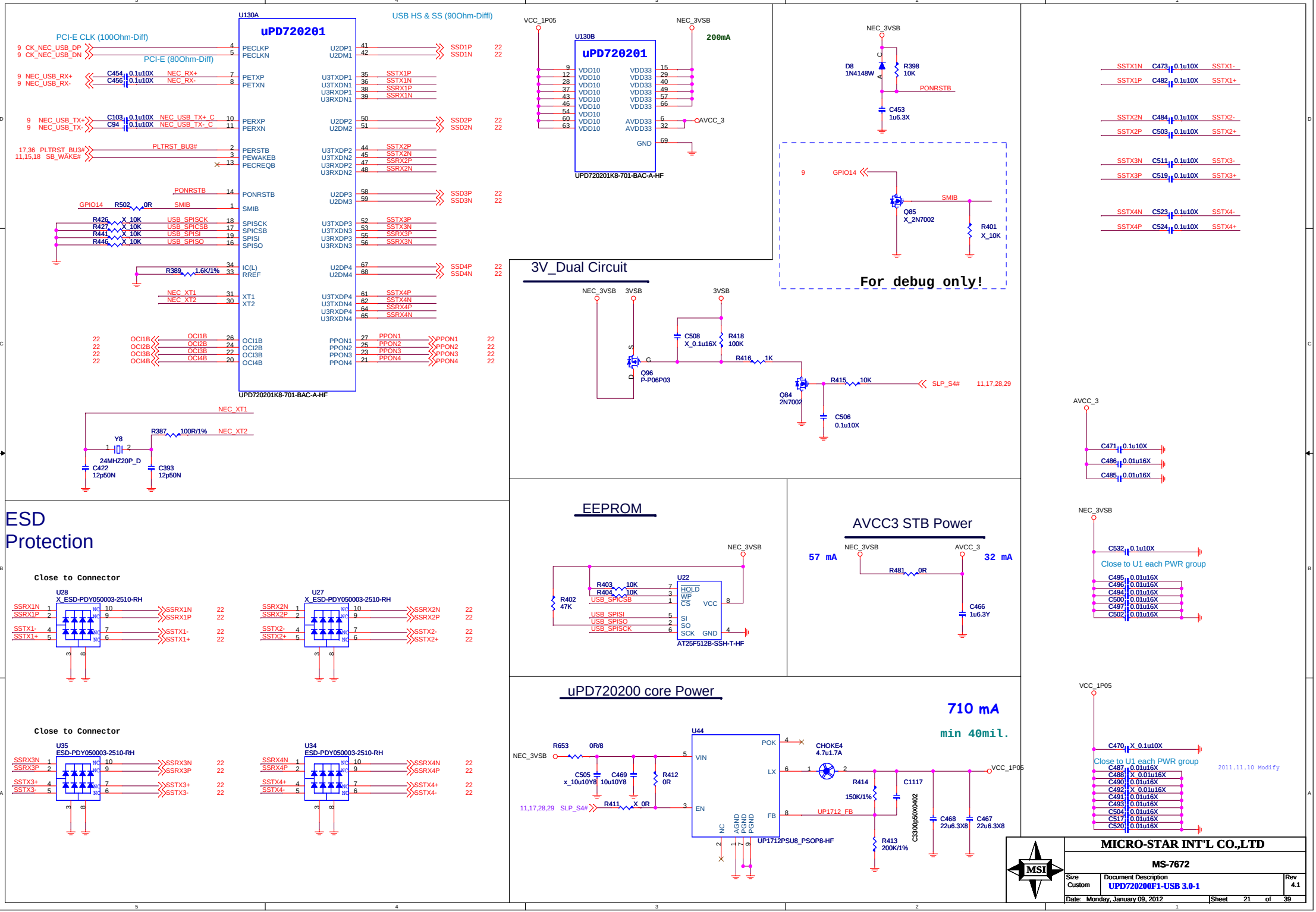


MICRO-STAR INT'L CO.,LTD

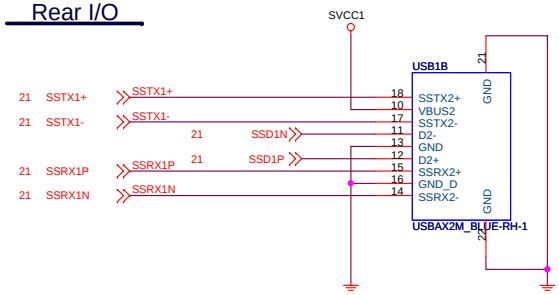
MS-7681

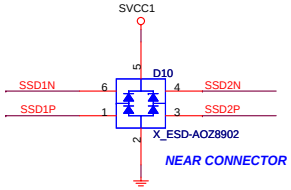
Size	Document Description	Rev
Custom	ASM1061 SATA6G	10

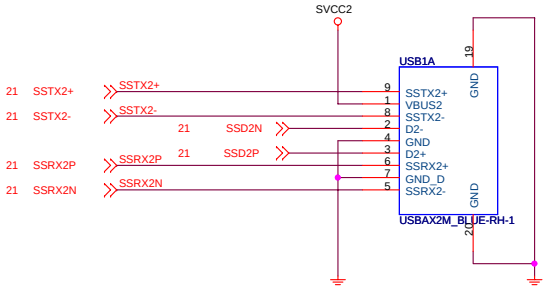
Date: Monday, January 09, 2012 Sheet 20 of 52

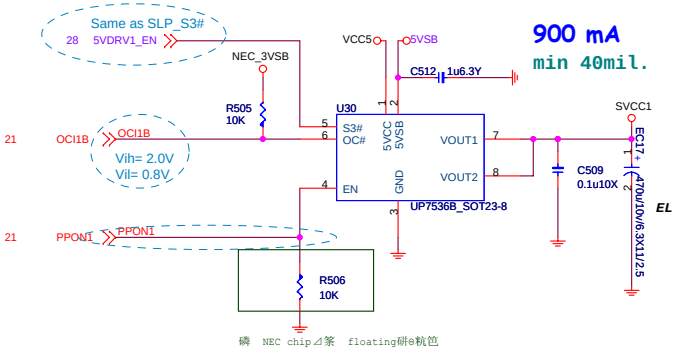

U130A
uPD720201
USB HS & SS (90Ohm-Diffl)
PCI-E CLK (100Ohm-Diff)
PCI-E (80Ohm-Diff)
UPD720201K8-701-BAC-A-HF
U130B
uPD720201
UPD720201K8-701-BAC-A-HF
VCC_1P05
NEC_3VSB
200mA
AVCC_3
GND
D8
1N4148W
R398
10K
PONRSTB
C453
1u6.3X
GPIO14
SMIB
Q85
X_2N7002
R401
X_10K
For debug only!
3V_Dual Circuit
3VSB
C508
X_0.1u16X
R418
100K
R416
1K
Q96
P-P06P03
R415
10K
SLP_S4#
11,17,28,29
Q84
2N7002
C506
0.1u10X
EEPROM
R402
47K
R403
10K
R404
10K
USB_SPICSB
USB_SPISI
USB_SPISO
USB_SPISCK
U22
HOLD
WP
CS
VCC
SI
SO
SCK
GND
AT25F512B-SSH-T-HF
AVCC3 STB Power
57 mA
32 mA
R481
0R
C466
1u6.3Y
uPD720200 core Power
710 mA
min 40mil.
U44
R653
0R/8
C505
x_10u10Y8
C469
10u10Y8
R412
0R
R411
X_0R
POK
VIN
LX
EN
FB
NC
AGND
PGND
PGND
CHOKE4
4.7u1.7A
R414
150K/1%
C1117
C3300p50X0402
UP1712_FB
R413
200K/1%
C468
22u6.3X8
C467
22u6.3X8
UP1712PSU8_PSOP8-HF
VCC_1P05
C470
X_0.1u10X
Close to U1 each PWR group
2011.11.10 Modify
C471
0.1u10X
C486
0.01u16X
C485
0.01u16X
C532
0.1u10X
C495
0.01u16X
C496
0.01u16X
C494
0.01u16X
C500
0.01u16X
C497
0.01u16X
C502
0.01u16X
C487
0.01u16X
C488
X_0.01u16X
C490
0.01u16X
C492
X_0.01u16X
C491
0.01u16X
C493
0.01u16X
C504
0.01u16X
C517
0.01u16X
C520
0.01u16X
SSTX1N
C473
0.1u10X
SSTX1-
SSTX1P
C482
0.1u10X
SSTX1+
SSTX2N
C484
0.1u10X
SSTX2-
SSTX2P
C503
0.1u10X
SSTX2+
SSTX3N
C511
0.1u10X
SSTX3-
SSTX3P
C519
0.1u10X
SSTX3+
SSTX4N
C523
0.1u10X
SSTX4-
SSTX4P
C524
0.1u10X
SSTX4+
AVCC_3
NEC_3VSB
Close to U1 each PWR group
ESD
Protection
Close to Connector
U28
X_ESD-PDY050003-2510-RH
U27
X_ESD-PDY050003-2510-RH
Close to Connector
U35
ESD-PDY050003-2510-RH
U34
ESD-PDY050003-2510-RH
MICRO-STAR INT'L CO.,LTD
MS-7672
Size
Custom
Document Description
UPD720200F1-USB 3.0-1
Rev
4.1
Date: Monday, January 09, 2012
Sheet 21 of 39

Rear I/O

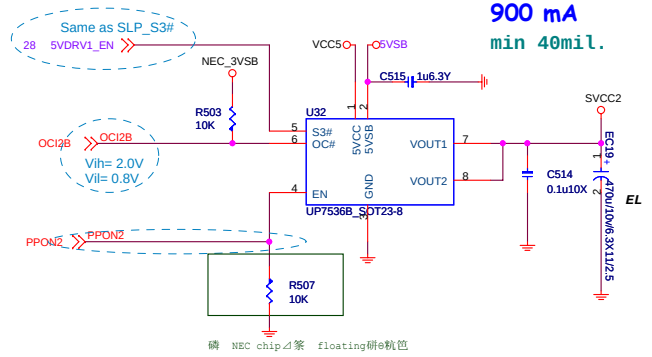


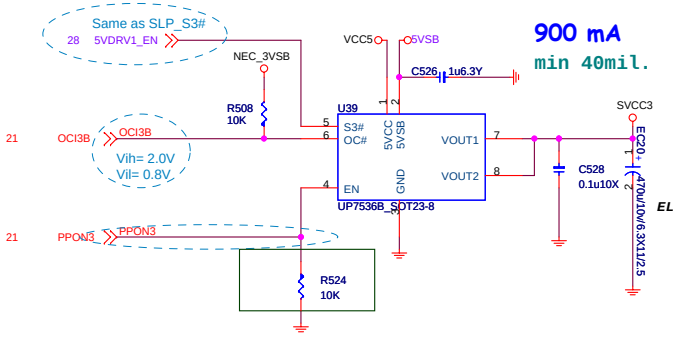


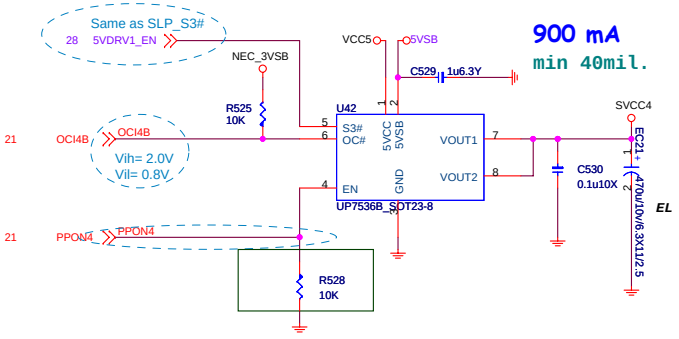


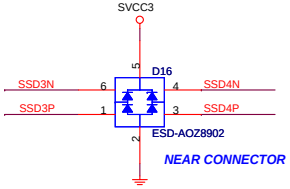


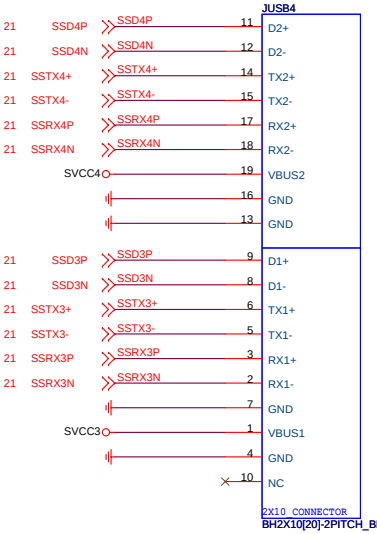
All power sources of uPD720200 are supplied, PPONx is enable.
PPONx is low when OCIx going to low.











MICRO-STAR INT'L CO.,LTD

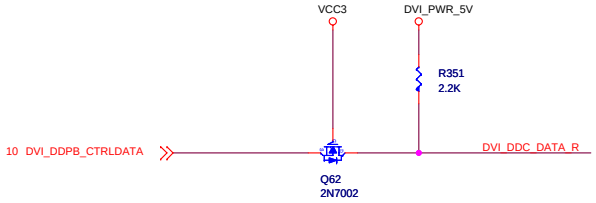
MS-7672

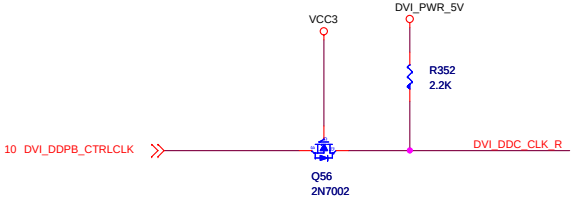
Size	Document Description	Rev
Custom	USB 3.0 Power & Connector	4.1

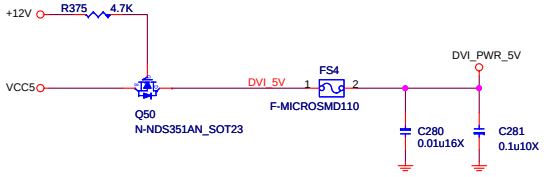
Date: Monday, December 19, 2011 Sheet 22 of 39

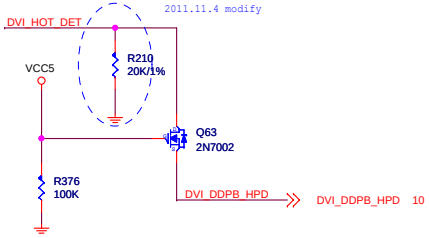
DVI level shifter

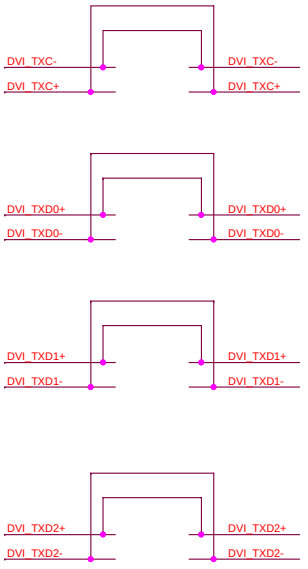
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

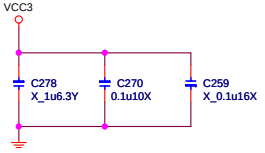


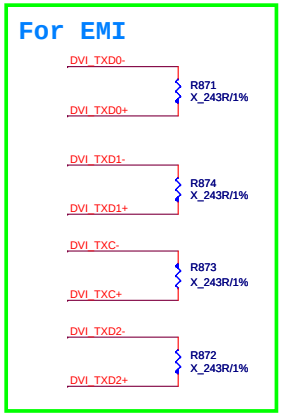


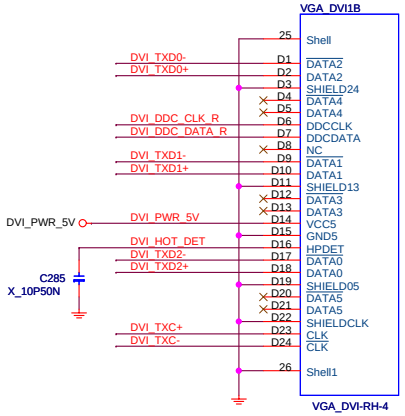


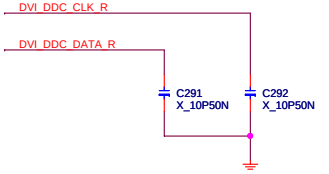












MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size: Custom	Document Description: DVI transfer	Rev: 4.1
Date: Monday, December 19, 2011	Sheet 23 of 39	

HDMI level shifter

HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

10 HDMI_DDPC_CLK_P	HDMI_DDPC_CLK_P	C140	0.1u10X	HDMI_TXC+	R509	680R	HDMI_MOS_CLKP
10 HDMI_DDPC_CLK_N	HDMI_DDPC_CLK_N	C142	0.1u10X	HDMI_TXC-	R522	680R	HDMI_MOS_CLKN
10 HDMI_DDPC_TX2_P	HDMI_DDPC_TX2_P	C134	0.1u10X	HDMI_TXD2+	R510	680R	HDMI_MOS_D2P
10 HDMI_DDPC_TX2_N	HDMI_DDPC_TX2_N	C132	0.1u10X	HDMI_TXD2-	R511	680R	HDMI_MOS_D2N
10 HDMI_DDPC_TX1_P	HDMI_DDPC_TX1_P	C136	0.1u10X	HDMI_TXD1+	R516	680R	HDMI_MOS_D1P
10 HDMI_DDPC_TX1_N	HDMI_DDPC_TX1_N	C137	0.1u10X	HDMI_TXD1-	R521	680R	HDMI_MOS_D1N
10 HDMI_DDPC_TX0_P	HDMI_DDPC_TX0_P	C123	0.1u10X	HDMI_TXD0+	R523	680R	HDMI_MOS_D0P
10 HDMI_DDPC_TX0_N	HDMI_DDPC_TX0_N	C119	0.1u10X	HDMI_TXD0-	R512	680R	HDMI_MOS_D0N

HDMI_TXC- → HDMI_TXC-
HDMI_TXC+ → HDMI_TXC+

HDMI_TXD2+ → HDMI_TXD2+
HDMI_TXD2- → HDMI_TXD2-

HDMI_TXD1+ → HDMI_TXD1+
HDMI_TXD1- → HDMI_TXD1-

HDMI_TXD0+ → HDMI_TXD0+
HDMI_TXD0- → HDMI_TXD0-

VCC3
Q31 2N7002D: G2 ← HDMI_MOS_CLKN, D1 ← G1, D2 → HDMI_MOS_CLKP, S2, S1
VCC3
Q36 2N7002D: G2 ← HDMI_MOS_D2N, D1 ← G1, D2 → HDMI_MOS_D2P, S2, S1
VCC3
Q38 2N7002D: G2 ← HDMI_MOS_D1N, D1 ← G1, D2 → HDMI_MOS_D1P, S2, S1
VCC3
Q43 2N7002D: G2 ← HDMI_MOS_D0N, D1 ← G1, D2 → HDMI_MOS_D0P, S2, S1

HDMI1 CONN-HDMI19P_BLACK-RH-11

HDMI_TXD0+	1	SHELL1	21
	2	D2+	
HDMI_TXD0-	3	D2 Shield	
HDMI_TXD1+	4	D2-	
	5	D1+	
HDMI_TXD1-	6	D1 Shield	
HDMI_TXD2+	7	D1-	
	8	D0+	
HDMI_TXD2-	9	D0 Shield	
HDMI_TXC+	10	D0-	
	11	CK+	
HDMI_TXC-	12	CK Shield	
	13	CK-	
	14	CE Remote	
HDMI_DDC_CLK_R	15	NC	
HDMI_DDC_DATA_R	16	DDC CLK	
	17	DDC DATA	
HDMI_PWR_5V	18	GND	
HDMI_HOT_DET	19	+5V	
		HP DET	
		SHELL2	20

MEC1

+12V → R209 4.7K → Q29 N-NDS351AN_SOT23 (VCC5) → HDMI_5V → FS2 F-MICROSMD110 → HDMI_PWR_5V

HDMI_PWR_5V
C108 0.01u16X
C111 0.1u10X

2011.11.03 modify

VCC3
R236 1M
Q30 2N7002
10 HDMI_DDPC_HPD
HDMI_HOT_DET
R204 20K/1%

VCC3
C124 0.1u10X
C139 1u6.3Y
C118 0.1u16X
C129 0.01u16X

HDMI_PWR_5V
R354 2.2K
VCC3
R353 2.2K
Q17 2N7002D: G2 ← HDMI_DDC_DATA_R, D1 ← G1, D2 → HDMI_DDC_CLK_R, S2 → HDMI_DDPC_CTRLCLK 10, S1
10 HDMI_DDPC_CTRLDATA

EMI

HDMI_TXC- / HDMI_TXC+ — R235 X_180R/1%
HDMI_TXD1- / HDMI_TXD1+ — R233 X_180R/1%
HDMI_TXD2- / HDMI_TXD2+ — R231 X_180R/1%
HDMI_TXD0- / HDMI_TXD0+ — R225 X_180R/1%

EMI

HDMI_DDC_CLK_R	C555	X_0.1u16X
HDMI_DDC_DATA_R	C556	X_0.1u16X
HDMI_HOT_DET	C562	X_0.1u16X

MICRO-STAR INT'L CO.,LTD

MS-7680

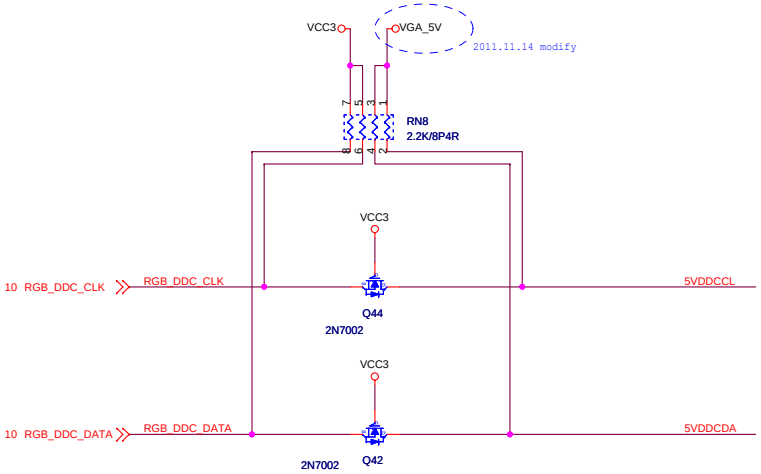
Size	Document Description	Rev
Custom	HDMI	4.1

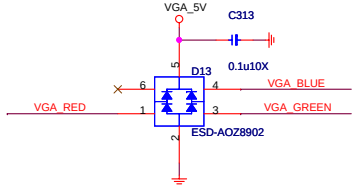
Date: Monday, December 19, 2011 Sheet 24 of 39

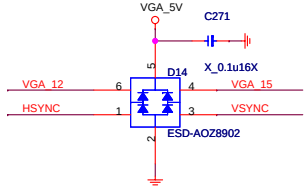
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

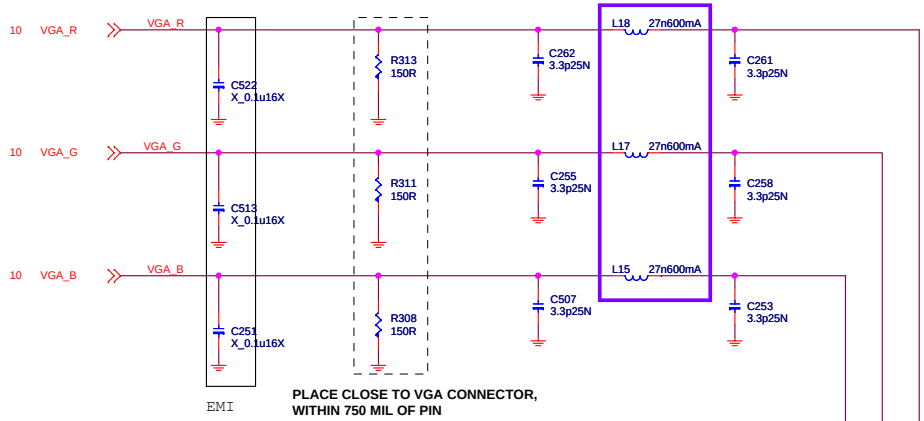
Level shift

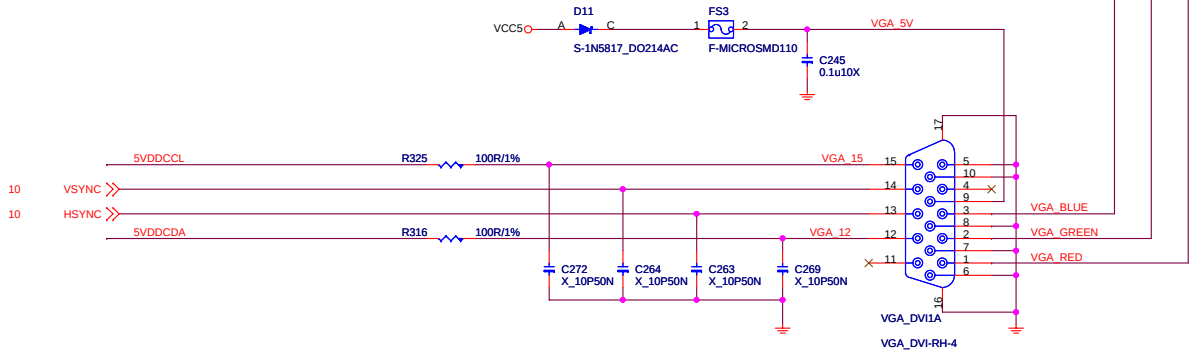






Change to L, don't use FB
Try to pass VESA v1.2

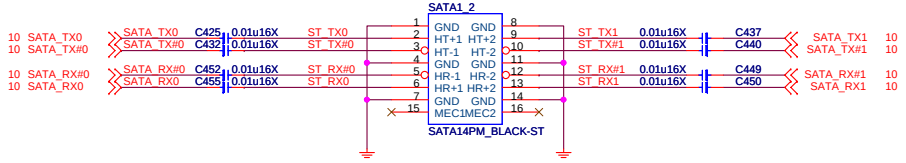


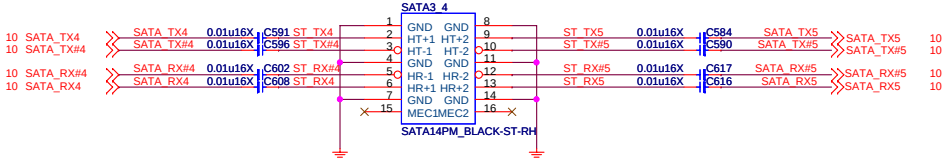


MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size: Custom	Document Description: VGA	Rev: 4.1
Date: Monday, December 19, 2011	Sheet 25 of 39	

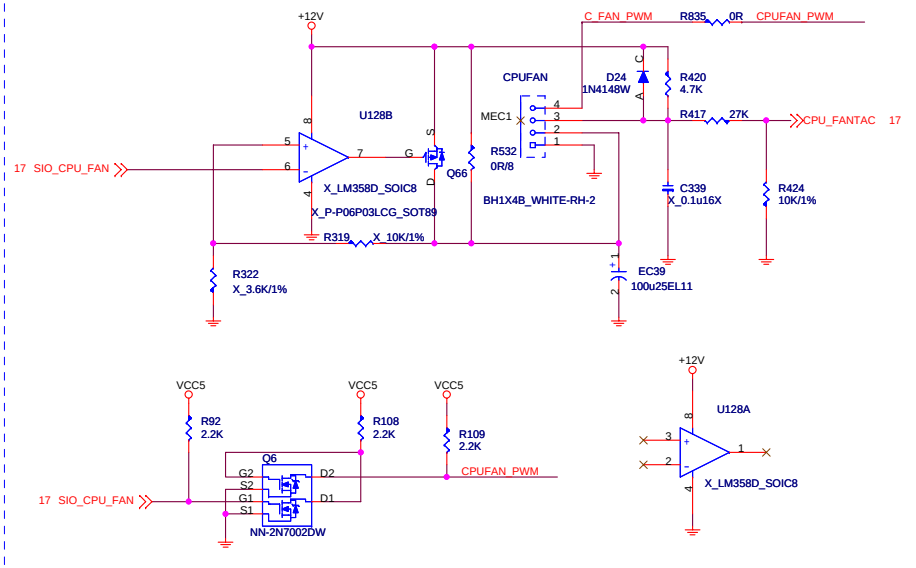
SATA 6G PORT 0,1

H61 PORT 0/1 Support 3G
H67 PORT 0/1 Support 6G

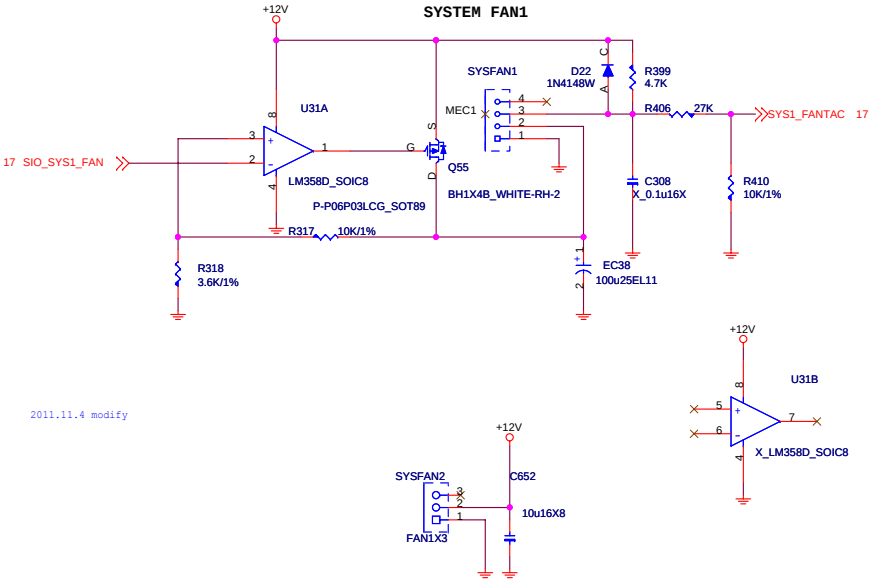




CPU FAN-COUNTROL CIRCUIT

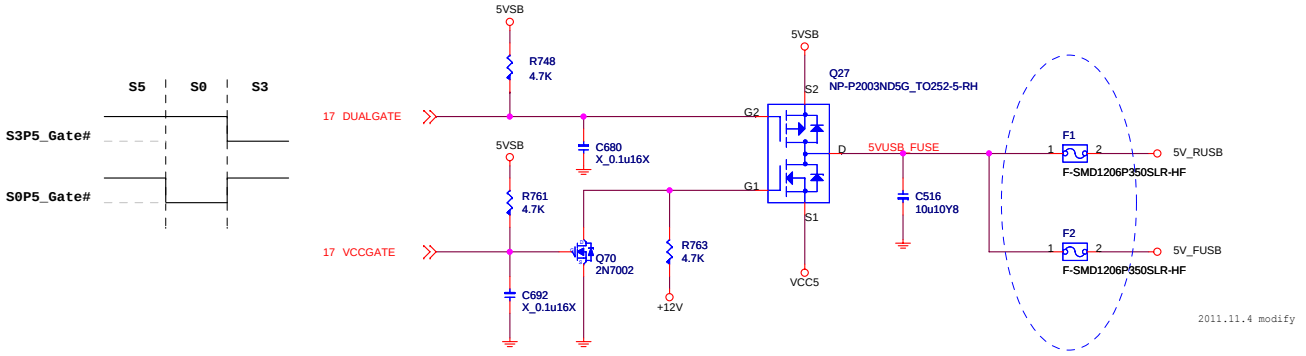


SYSTEM FAN-COUNTROL CIRCUIT



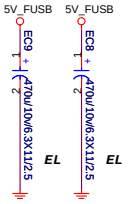
MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size: Custom	Document Description: SATA / FAN Control	Rev: 4.1
Date: Monday, January 09, 2012	Sheet 26 of 39	

5V_RUSB Switch



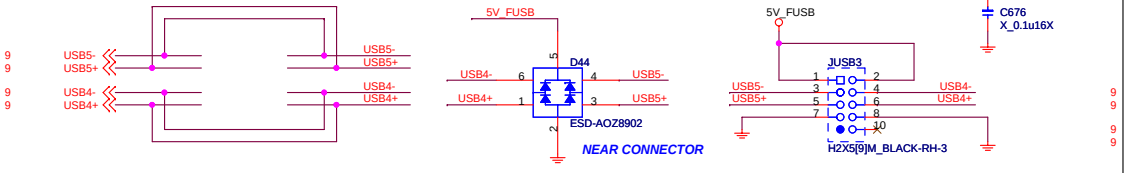
Front USB Connector

NEAR USB Front CONNECTOR

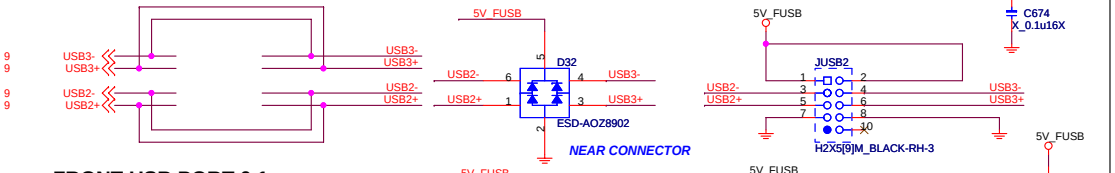


For H61 6,7,12,13 Port should be remove

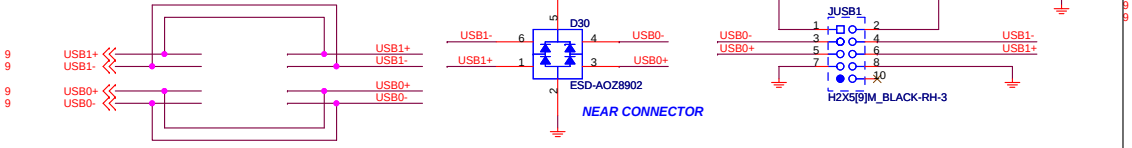
FRONT USB PORT 4,5



FRONT USB PORT 2,3

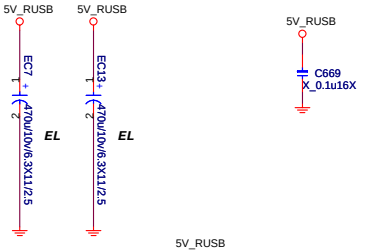


FRONT USB PORT 0,1

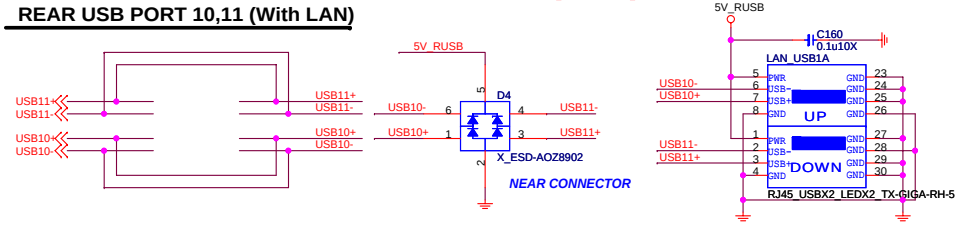


Rear USB Connector

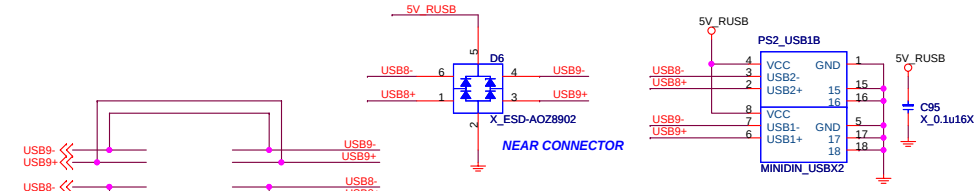
NEAR USB REAR CONNECTOR



REAR USB PORT 10,11 (With LAN)

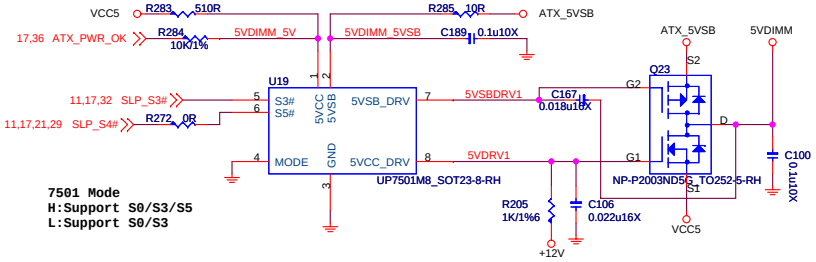


REAR USB PORT 8,9 (With PS2)

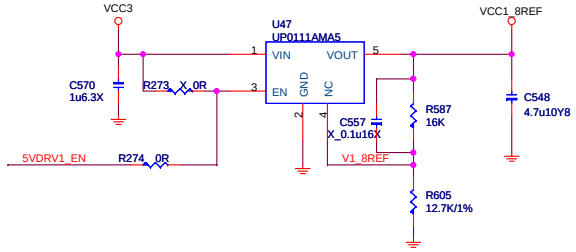


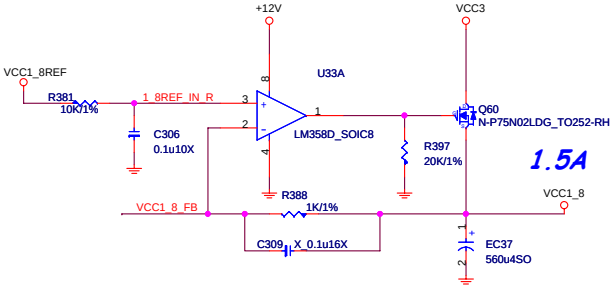
MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size: Custom	Document Description: USB Connector	Rev: 4.1
Date: Monday, December 19, 2011	Sheet 27 of 39	

5VDIMM FOR DDR

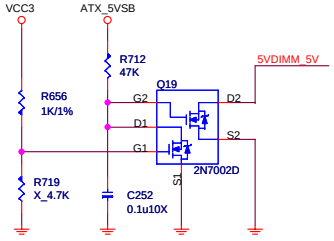


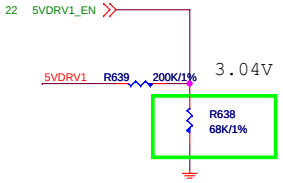
VCC1_8REF





USB MODE

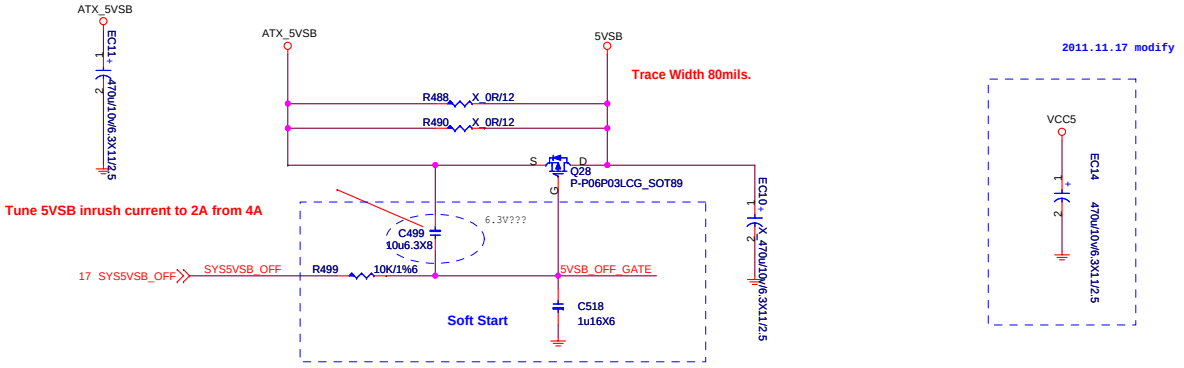




56K-->68K.

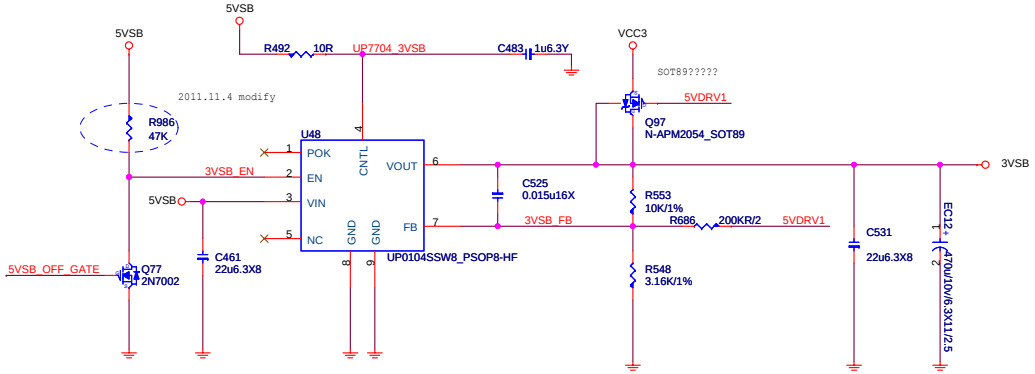
Patch coolermaster 700w power sequence

5VSB Power Switch



3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



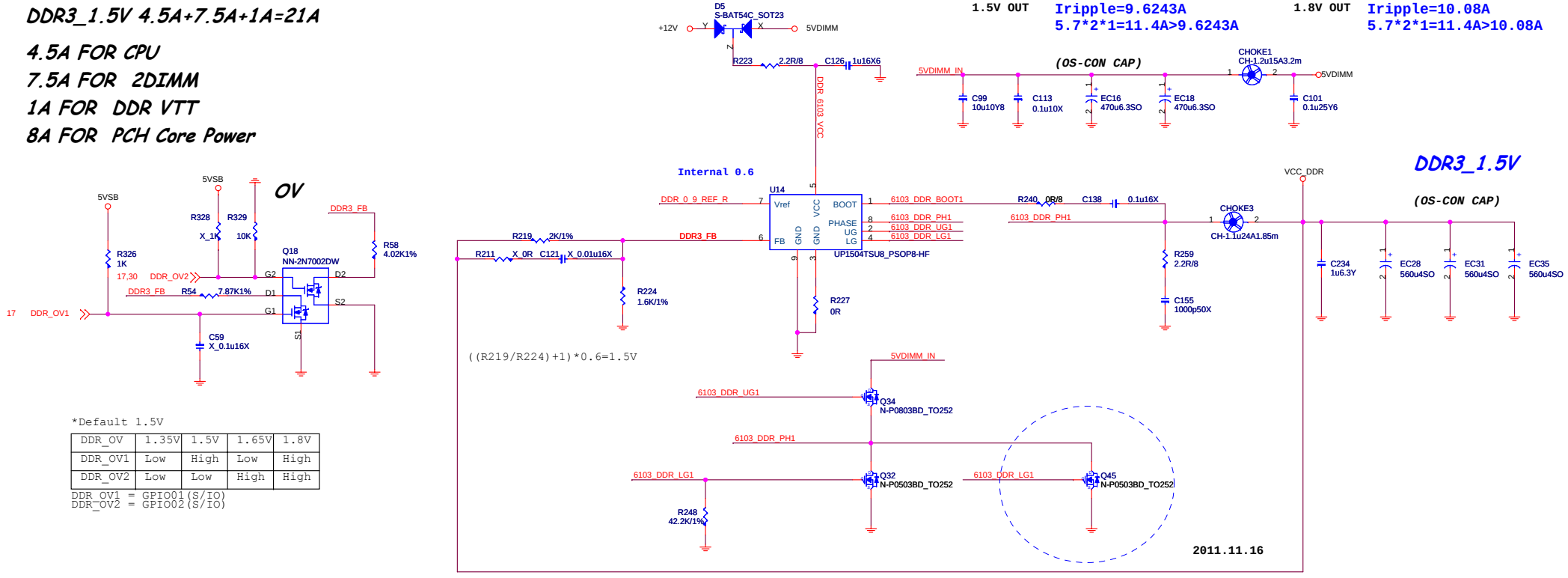
MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size: Custom	Document Description: ACPI controller UPI	Rev: 4.1
Date: Monday, January 09, 2012	Sheet 28 of 39	

DDR3_1.5V 4.5A+7.5A+1A=21A

4.5A FOR CPU
7.5A FOR 2DIMM
1A FOR DDR VTT
8A FOR PCH Core Power

1.5V OUT Iripple=9.6243A
5.7*2*1=11.4A>9.6243A

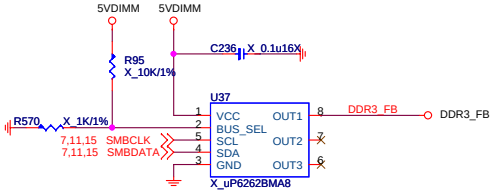
1.8V OUT Iripple=10.08A
5.7*2*1=11.4A>10.08A



*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01(S/IO)
DDR_OV2 = GPIO02(S/IO)

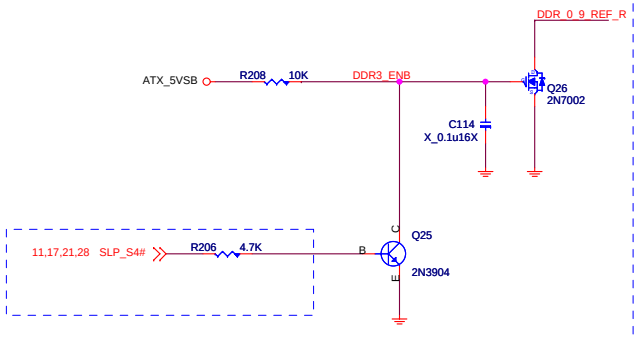


UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

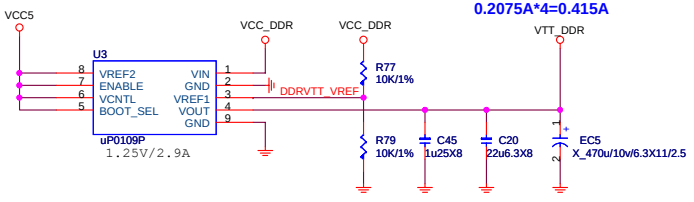
P.S. Only for meet Intel power down sequence.



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

0.2075A*4=0.415A



MICRO-STAR INT'L CO.,LTD

MS-7680

Size	Document Description	Rev
Custom	DDR Power - uP6103 1-Phase	4.1

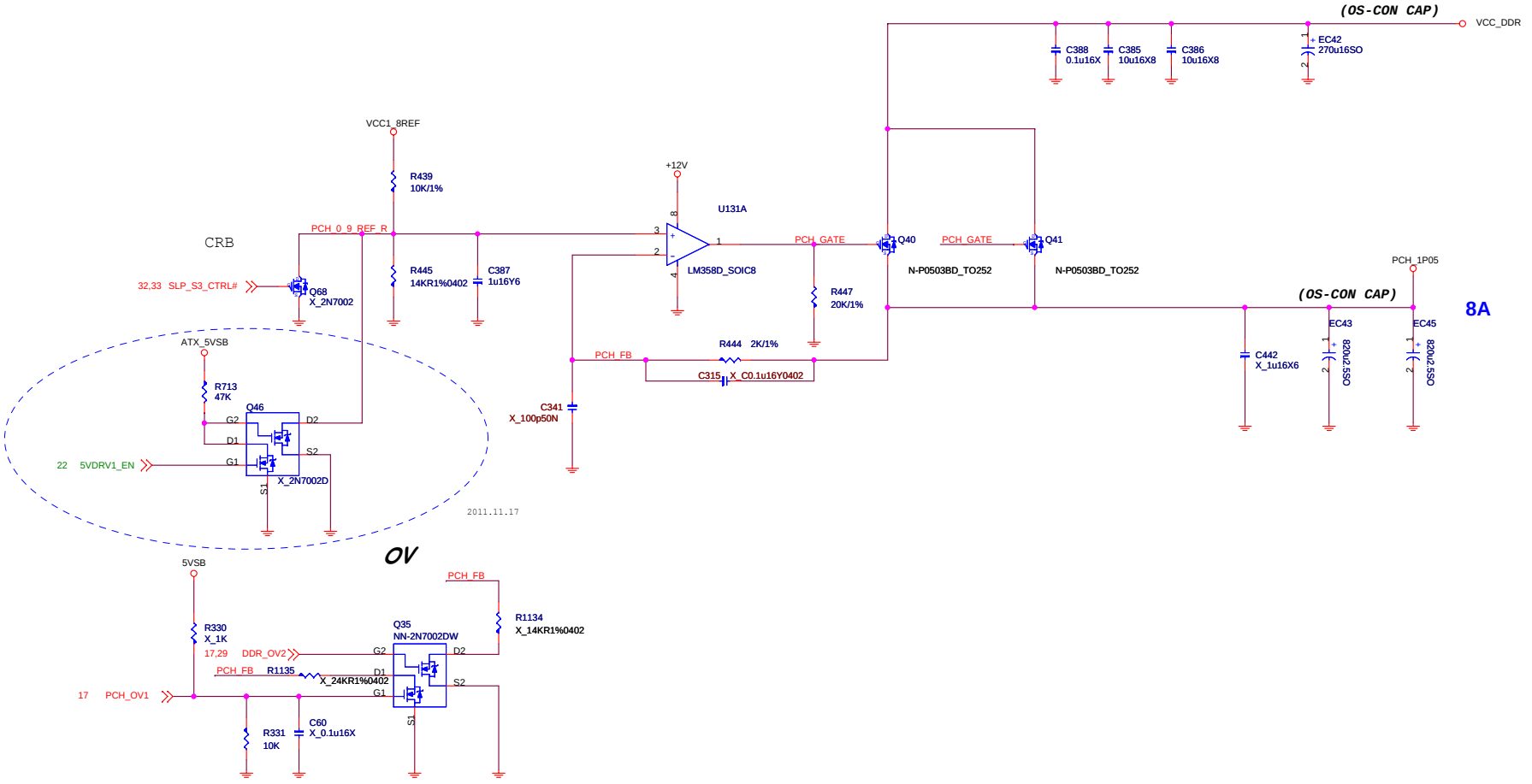
Date: Monday, December 19, 2011 Sheet 29 of 39

PCH Power:1.05V

PCH Core 6.2A+1.8A=8A

6.2A FOR PCH

1.8A FOR ME CORE



*Default 1.05V

DDR_OV	1.05	1.2V	1.35V	
DDR_OV2	Low	High	High	
PCH_OV1	Low	Low	High	

MICRO-STAR INT'L CO.,LTD

MS-7680

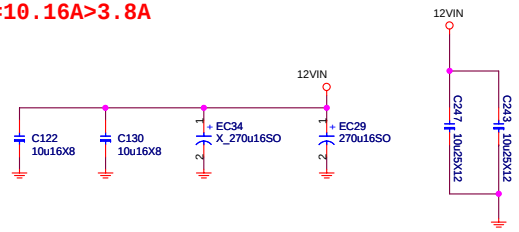
Size: Custom | Document Description: PCH Power - uP6103 1-Phase | Rev: 4.1

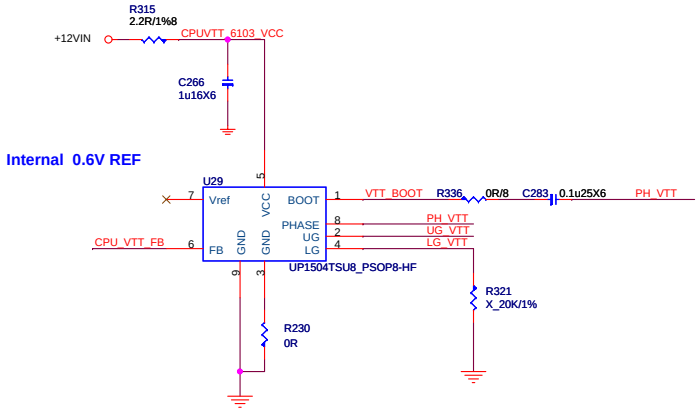
Date: Monday, December 19, 2011 | Sheet 30 of 39

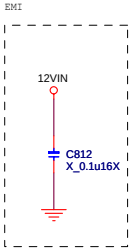
CPU_VTT:1.05/1.00

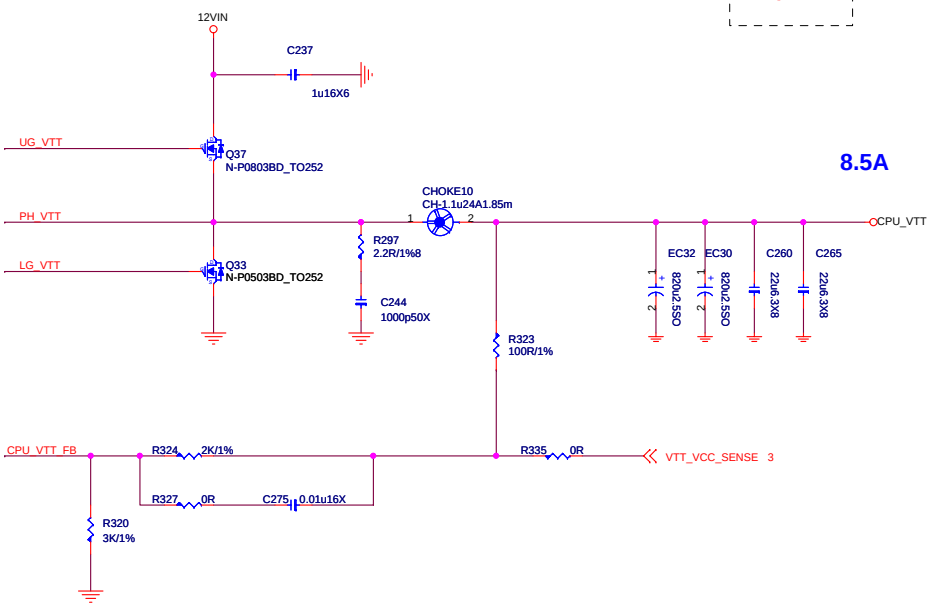
CPU VTT 8.5A + SA Core =8.8A =17.3A

Iripple=1.92(vtt)+1.88(sa)
5.08*2=10.16A>3.8A



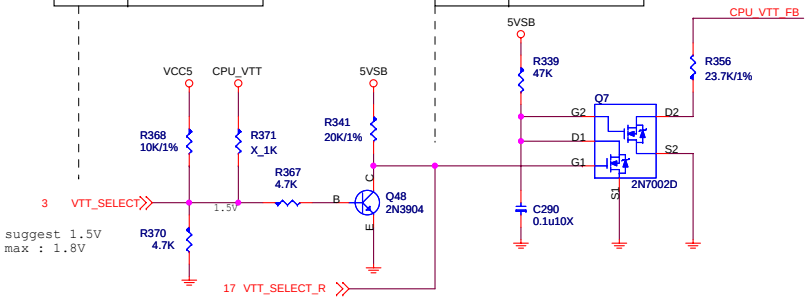






VTT_SELECT	
Low	1.0V
High	1.05V

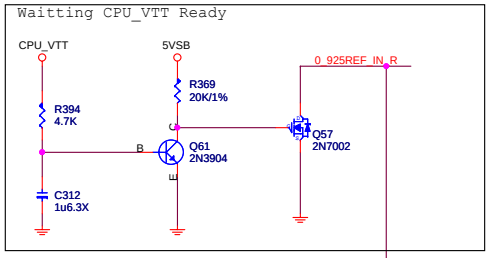
VTT_SELECT Table	
Low	1.05V
High	1.0V

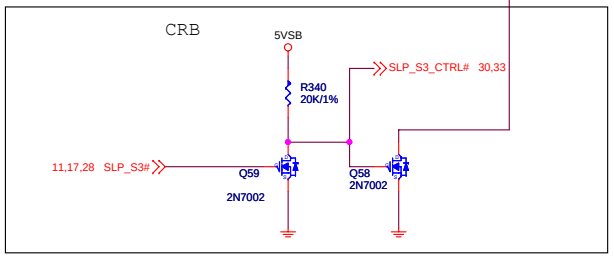


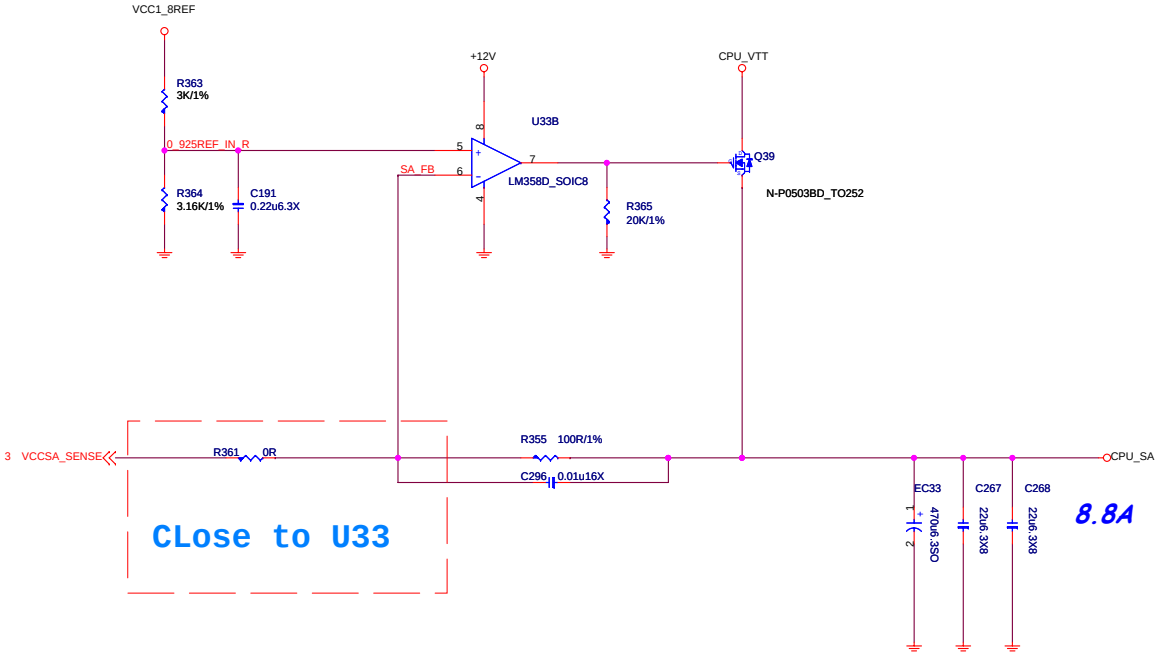
MICRO-STAR INT'L CO.,LTD			
MS-7680			
Size: Custom	Document Description: CPU_VTT - uP6103- 1-Phase		Rev: 4.1
Date: Monday, December 19, 2011		Sheet 31 of 39	

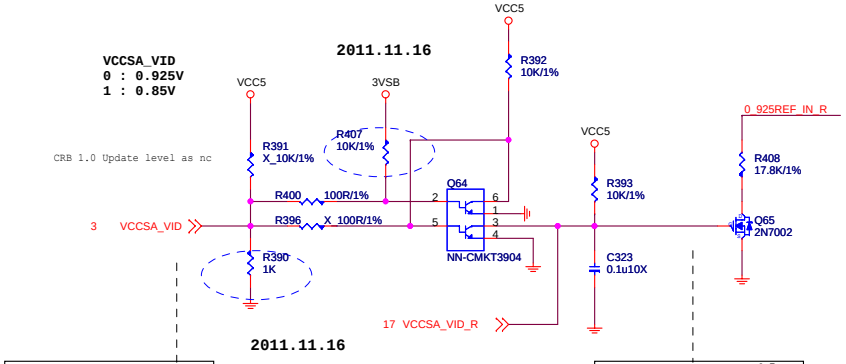
CPU_SA:0.925/0.85

SA Core =8.8A







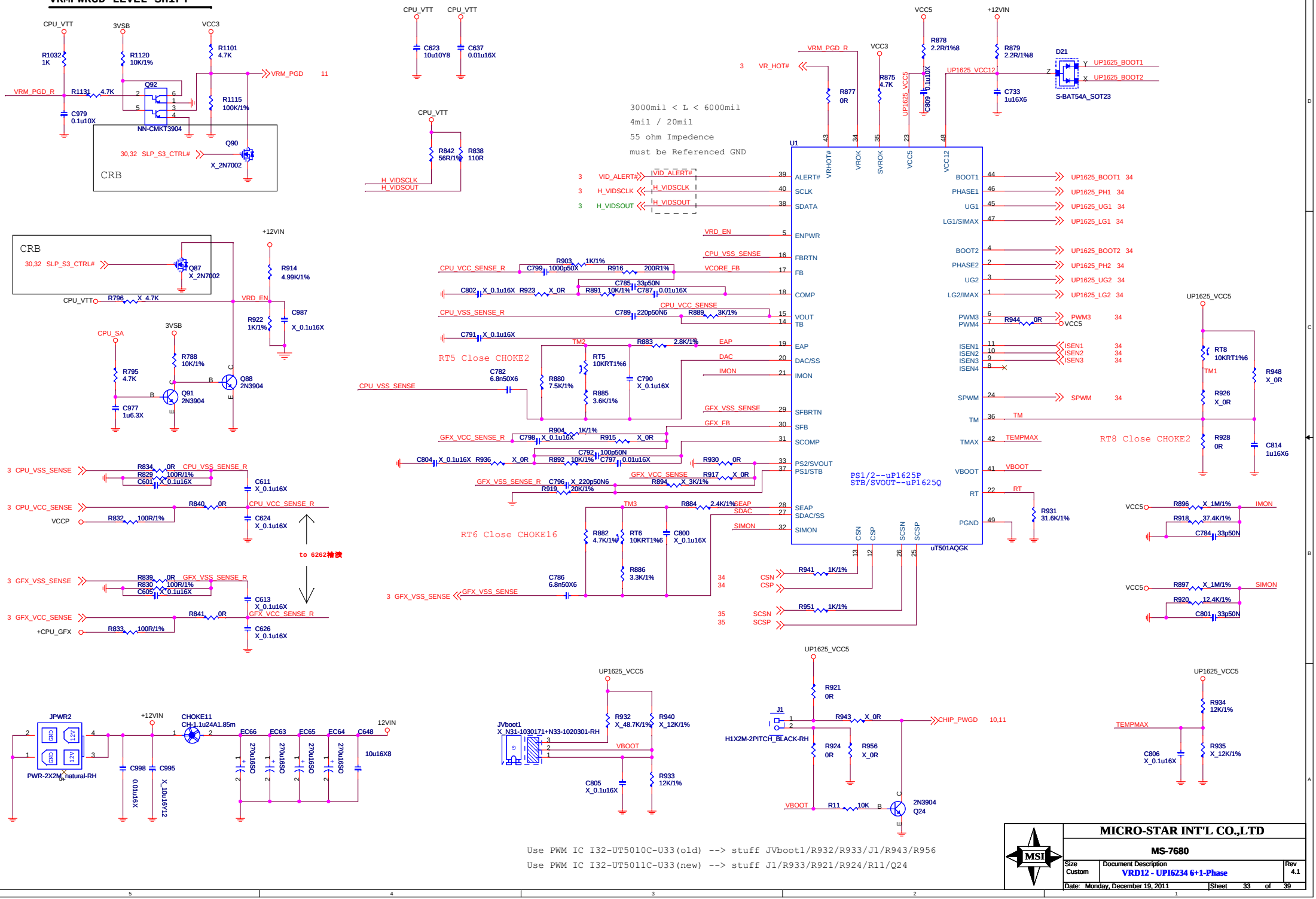


VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V

MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size: Custom	Document Description: CPU_SA - uP6103 1-Phase	Rev: 4.1
Date: Monday, January 09, 2012	Sheet 32 of 39	

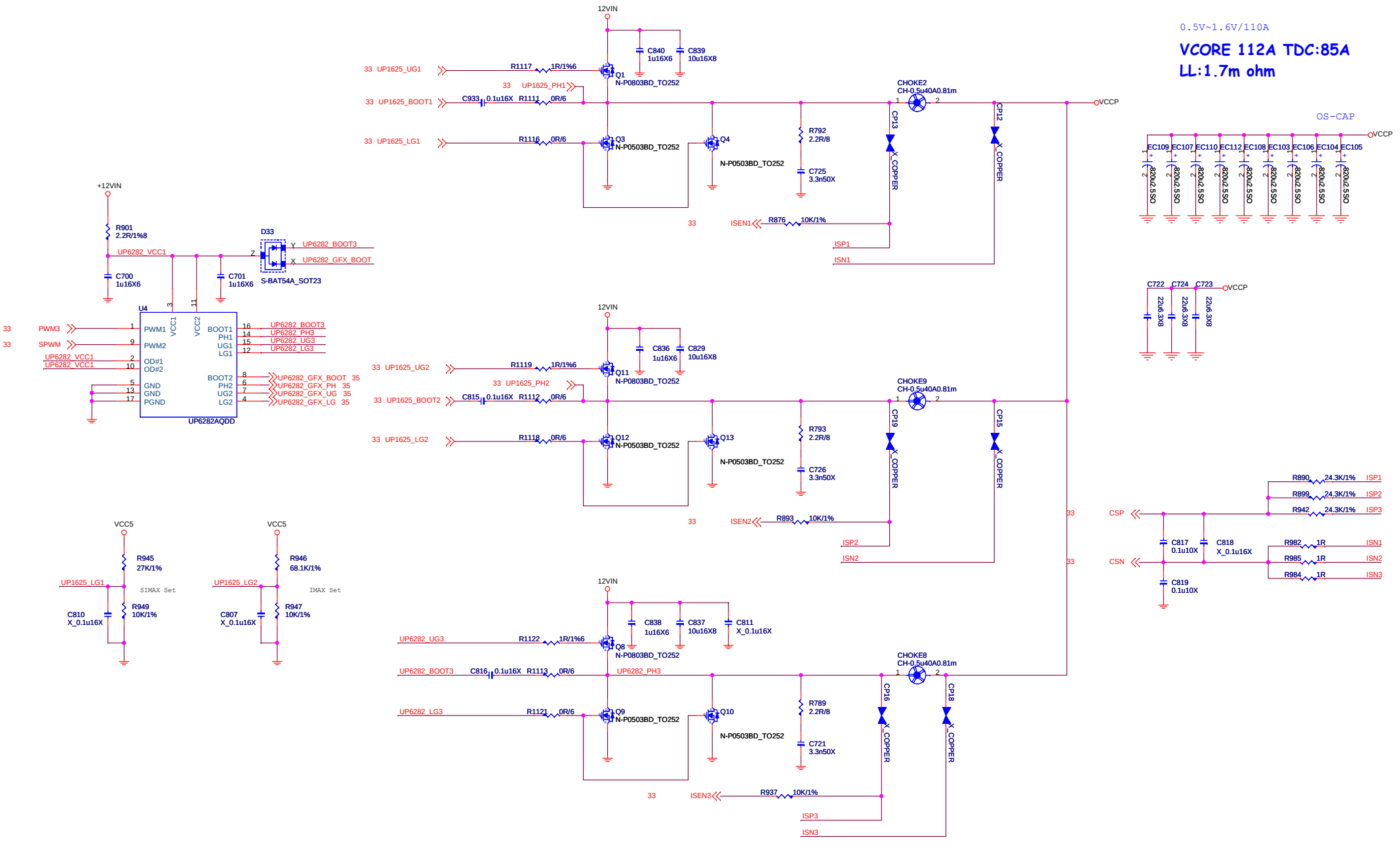
VRMPWRGD LEVEL SHIFT



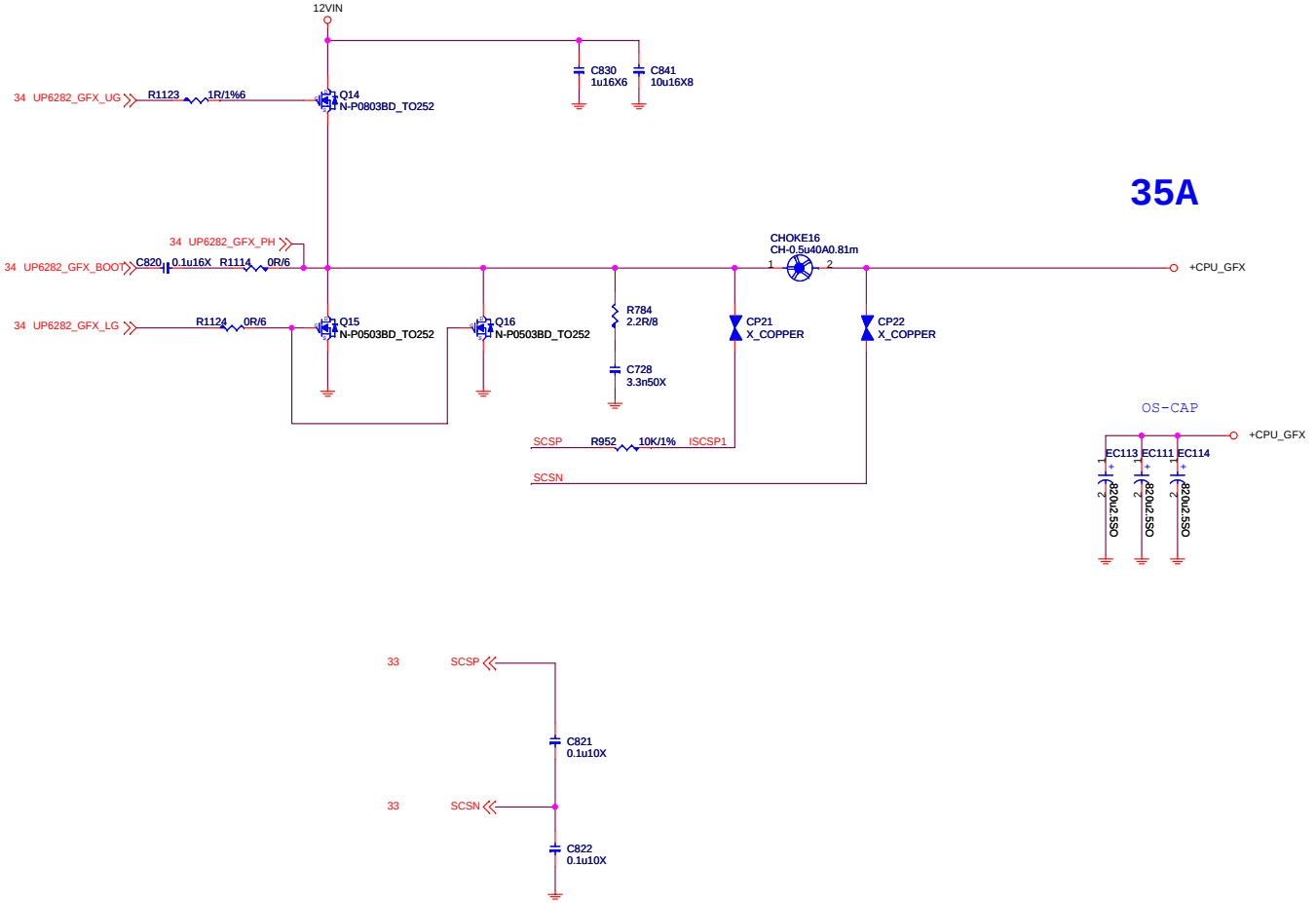
MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size: Custom	Document Description: VRD12 - UPI6234 6+1-Phase	Rev: 4.1
Date: Monday, December 19, 2011	Sheet 33 of 39	

0.5V~1.6V/110A

VCORE 112A TDC:85A
LL:1.7m ohm

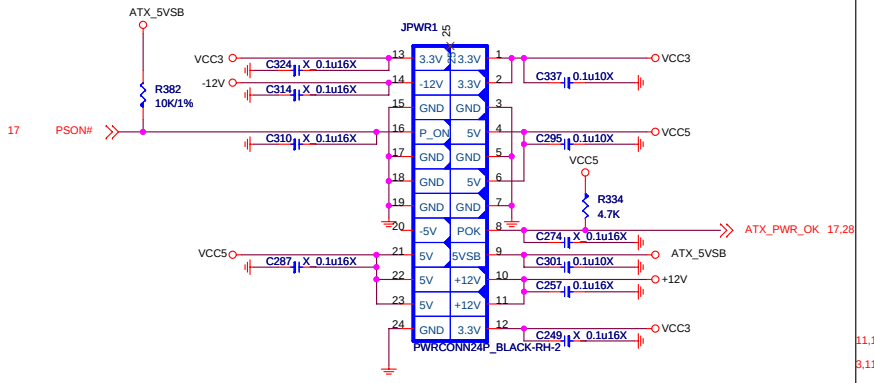


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7680	
Size: Custom	Document Description: UP6234 6-Phase CPU	Rev: 4.1
Date: Monday, December 19, 2011	Sheet 34 of 39	

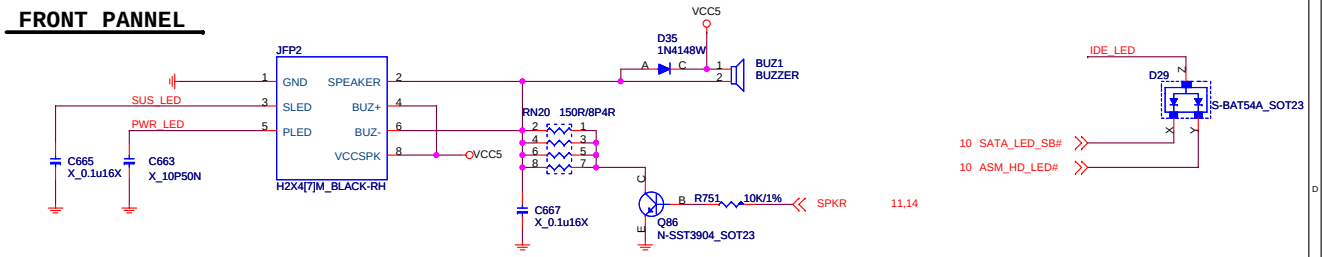


MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size: Custom	Document Description: UP6234 1-Phase GPU	Rev: 4.1
Date: Monday, December 19, 2011	Sheet 35 of 39	

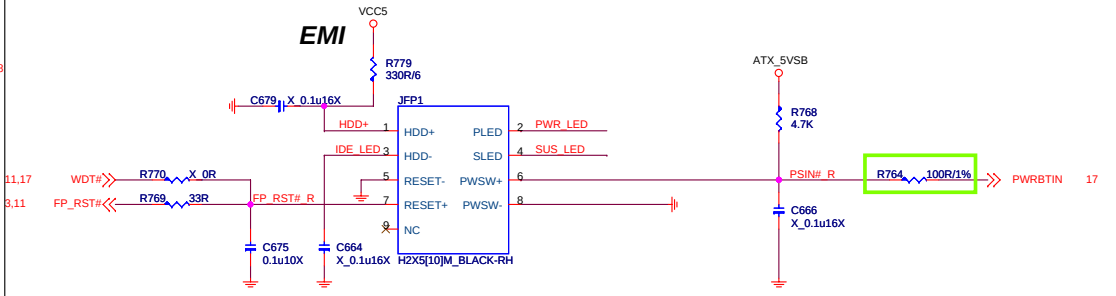
ATX POWER CONNECTOR



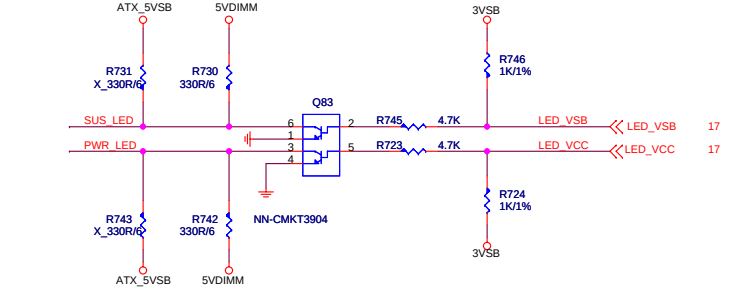
FRONT PANNEL



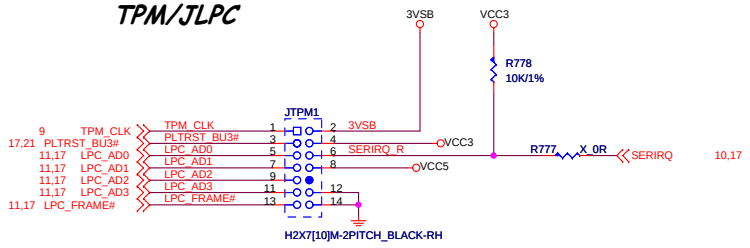
EMI



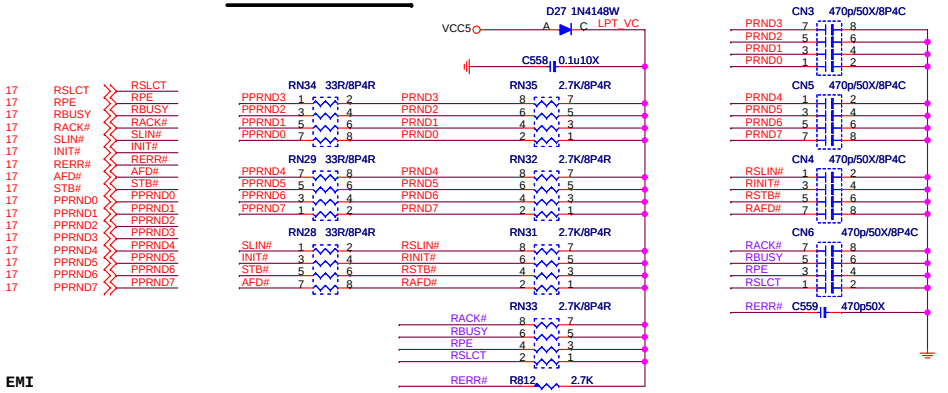
LED (for Fintek 71869)



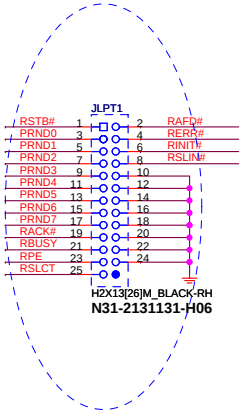
TPM/JLPC



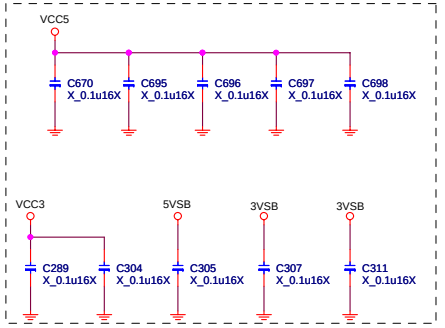
PARALLAL PORT



modify footprint!



EMI



MICRO-STAR INT'L CO.,LTD

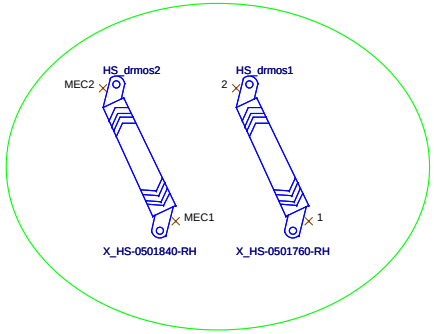
MS-7680

Size: Custom | Document Description: ATX PWR-Connector & Front Panel & EMI | Rev: 4.1

Date: Monday, December 19, 2011 | Sheet 36 of 39

MS-7680-7.0

OPT	Configure	BOM	Function



AUDIO CON OPT.

AUDIO10
AUDIO
PK/GR/BU/GY/OR/BL

EL/OS OPT.

EC200	EC201	EC202	EC203
EC	EC	EC	EC
270uF16OS	100u16SO	470u6.3SO	100u25EL

LABEL

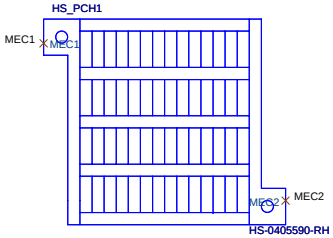
LA10
Label
601-7680-210
LABEL

HDMI_LA1
Label
HDMI
HDMI LABEL

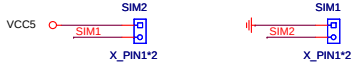
LA1
AMI_BIOS LABLE
BIOS_LABLE

HDMI_RLA1
Real Label
HDMI
HDMI_RLA

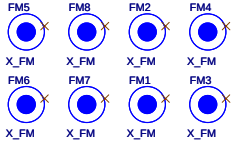
PCH XDP PWRGD/RESET



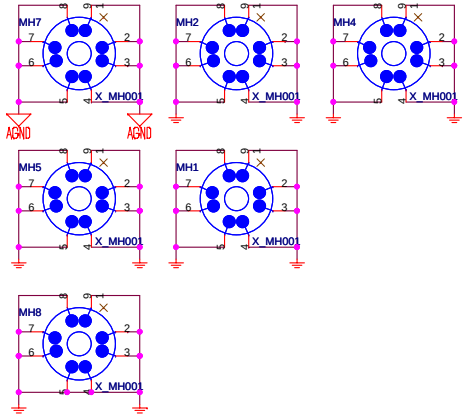
Simulation



Optical Fiducial Marks-120



Mounting Holes



PCB1
7680-7.0

BAT1_X1
BAT-BCR2032P-RH

RUB1
USB
X_Rubber

RUB2
USB
X_Rubber

CPU_H1
CPU
E21-7557050-L06

THX1
Label
THX
X_THX LABEL

PK0-0768041-G37,花Lo,23,脚 吹邹紅(MSIS),4,Coffee
PK0-0768041-E36,EsE,23,脚 吹邹紅(MSIS),4,Coffee

MICRO-STAR INT'L CO.,LTD

MS-7680

Size	Document Description	Rev
Custom	XDP / Manual Parts	4.1

Date: Monday, December 19, 2011 Sheet 37 of 39