Lenovo M920z/M828z Schematic Rev:1.0 Model Name:IQ370SV RVP10

Reference	Description
CB	0.1UF_0402
CP	0.01UF_0402
CM	1UF_0603

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Document Number : <Doc>		
Prepared by : KERRY HUANG		
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Block Diagram - M920z/M828z

M=0 M=1

GDDR5 CHA 8Gb(256MX32) | GDDR5 CHA 8Gb(256MX32)

*SAMSUNG-K4G80325FB-HC28
*MICRON-MT51J256M32HF-70:A

DQ 0~31 1500MHZ | DQ 32~64 1500MHZ

M920z : SSID 17AA SVID 3122

M828z : SSID 17AA SVID 3131

AMD GPU GB2b-64 R17M-M1-70 (25W)

PCI Express 3.0 X8

Intel CFL-S 6+2 Processor 65W LGA1151

Voltage: VCCCORE VCCGT VCCSA

VCCCORE: IMVP8 4 Phase

VCCGTS: IMVP8 2 Phase

VCCSA: 1 Phase

eDP: RTD2526-CG SCALAR → LVDS CONN

DDI3: PS8330B DP REPEATER → DP Switch TS3DV642 → DP CONN

DDR4 2400/2666 → CHA SO-DIMM

DDR4 2400/2666 → CHB SO-DIMM

Voltage: 0.6V, 1.2V

DMI X4(Gen 3)

Intel 300 CNP-H PCH

Q370 for M920z,B360 for M828z

TDP<= 6W

Voltage: V3.3A,V1.0A,VCCDSW_3p3

Clock: 32.768K/14/33/48/96/100MHz

SATA HDD*1 — SATA3.0

SATA ODD*1 — SATA3.0

M.2 Socket Slot M KEY — PCIE P21~24:x4

M.2 Socket Slot E KEY — CNVi, PCIE P7:x1, USB2.0 P14

FP HEADER — USB2.0 P12

USB3.1 Gen1 → SIDE USB CONN P7 *ONLY FOR M920z

USB3.1 Gen2 → SIDE USB CONN P1

USB3.1 Gen1 → USB TYPE-C(P2)

USB3.1 Gen1 → Rear USB CONN*4Ports(P3~P6)

USB2.0 P8 → Web Camera

USB2.0 P9 → Multi-Touch Connector

*ONLY FOR M920z

USB2.0 P10 → RTS5170-GR | Card Reader

SPI → SPI Flash ROM (16M+8M FOR M920z,16+4M FOR M828z)

SPI → TPM

Voltage:3.3VAUX

HDA → Audio Codec ALC233-VB2-CG

Voltage:3.3V,5V

Clock: 24MHz

LPC → IT8738E SIO

Voltage:3.3V, 3.3VAUX

Clock: 24MHz

COM CONN*1(Rear)

FAN Header*1

SPI(1MB)*1

PCI Express 2.0

RJ45 CONN *1 — Intel JACKSONVILLE LM for M920z ,LV for M828z

Voltage:3.3VAUX, 1.2VAUX, 1.8VAUX

Clock: 25MHz/100MHz

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TITLE: M920z/M828z BLOCK DIAGRAM		REV: V1.0
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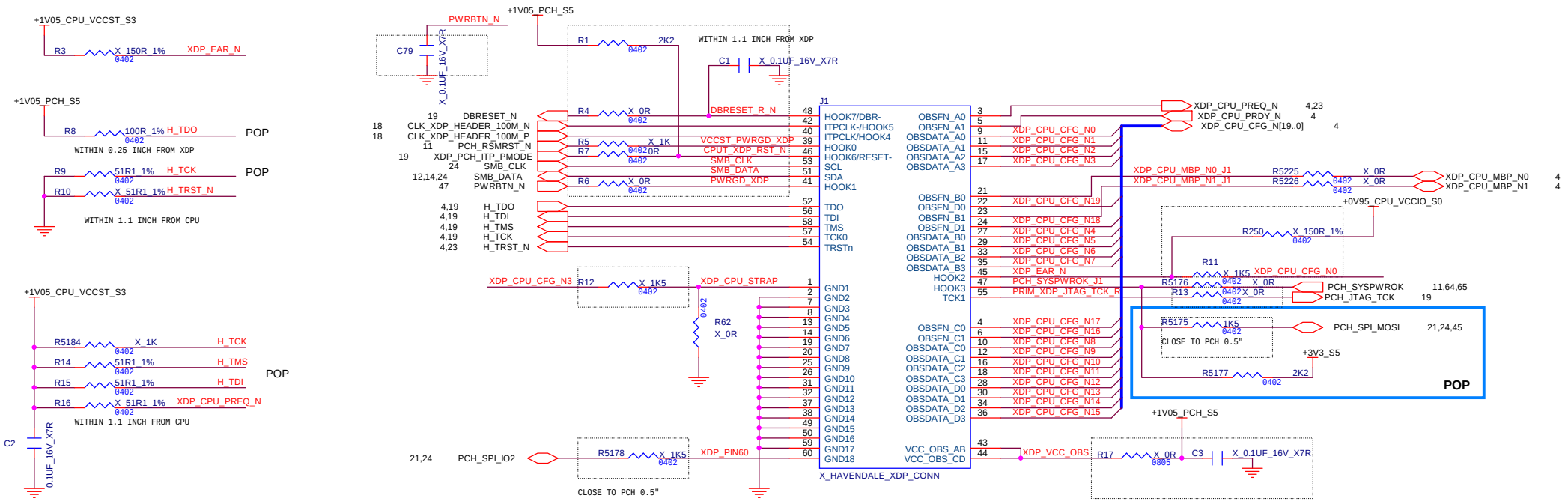
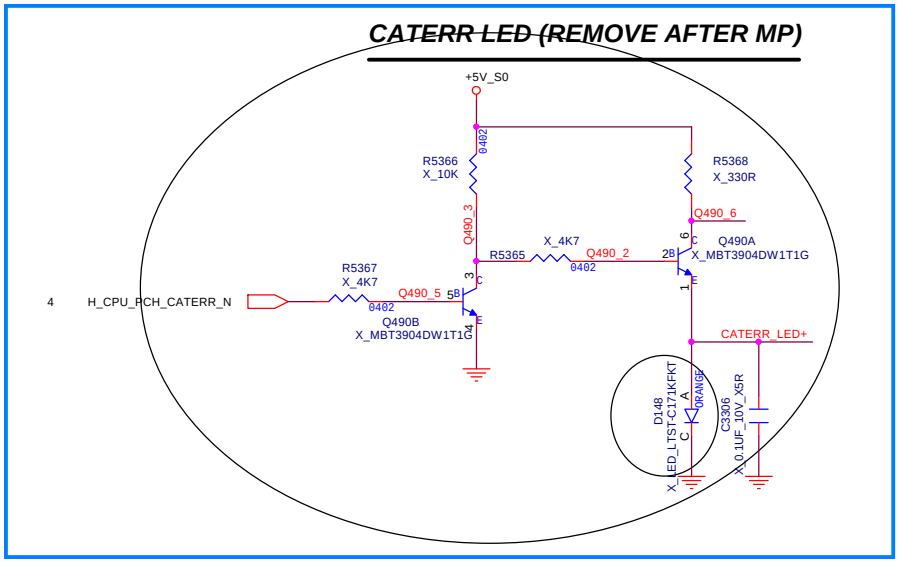
CPU DEBUG CONN





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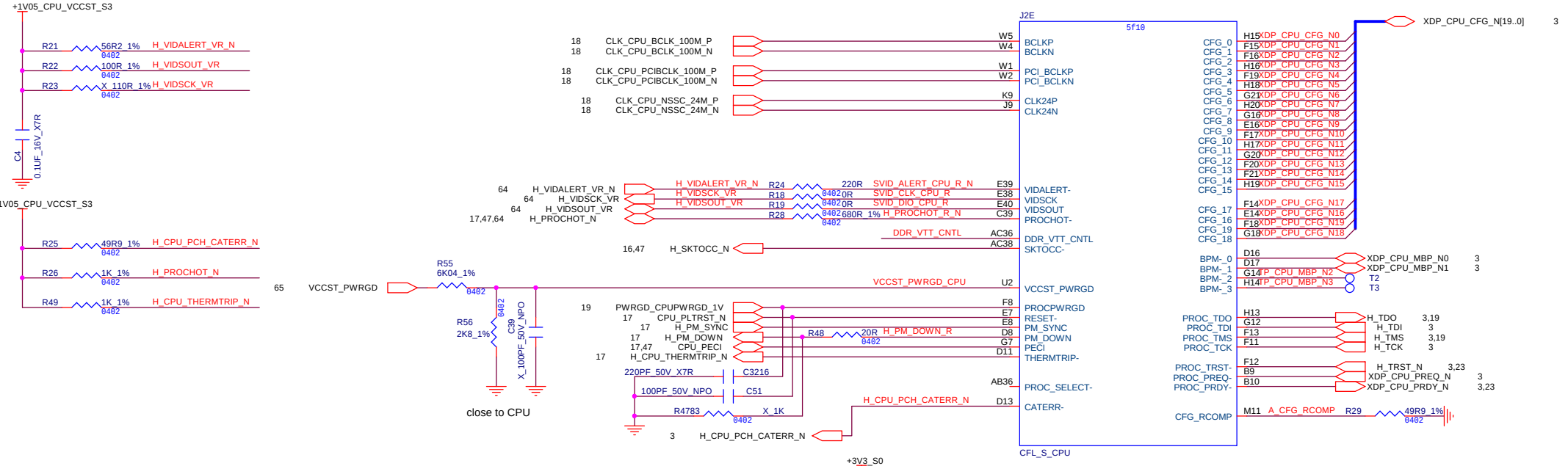
TITLE: M920z/M828z XDP DEBUG PORT			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, March 06, 2018		PAGE: 3 of 99



CFG CONFIG TABLE

CFG	HIGH	LOW	STRAP DESCRIPTION
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG_LAN_REVERSAL
3	ENABLE	DISABLE	PHYSICAL_DEBUG_ENABLE
4	DISABLE	ENABLE	eDP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8	DISABLE	ENABLE	CFG UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVATE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI_AC_COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYNC	PMSYNC ASYNC MODE
14	RESERVE		
15	RESERVE		
ALL PINS HAVE INTERNAL PULL-UPS			

PCI-E CONFIG TABLE

CFG 6	CFG 5	PCI-E CONFIG
0	0	X8 X4 X4
0	1	RESERVED
1	0	X8 X8
1	1	X16

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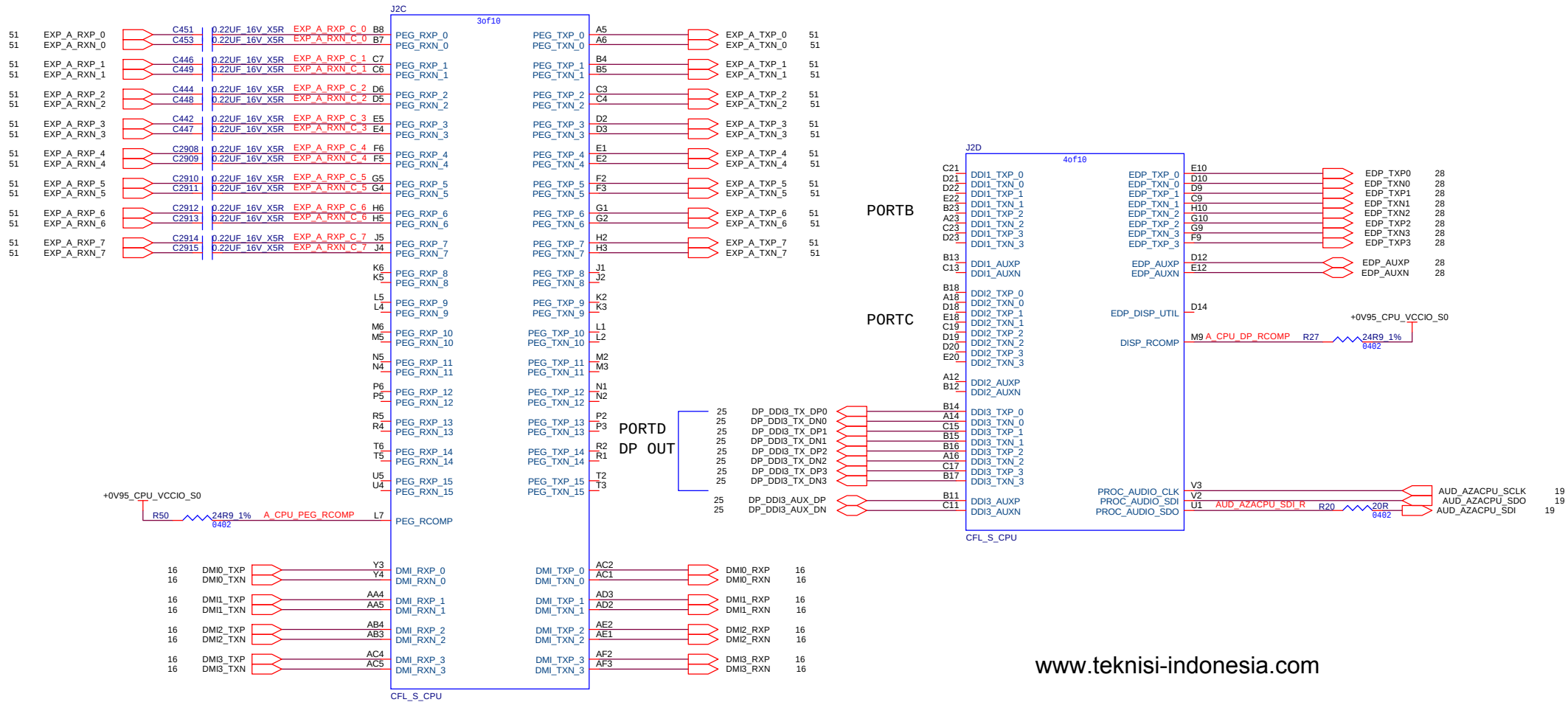

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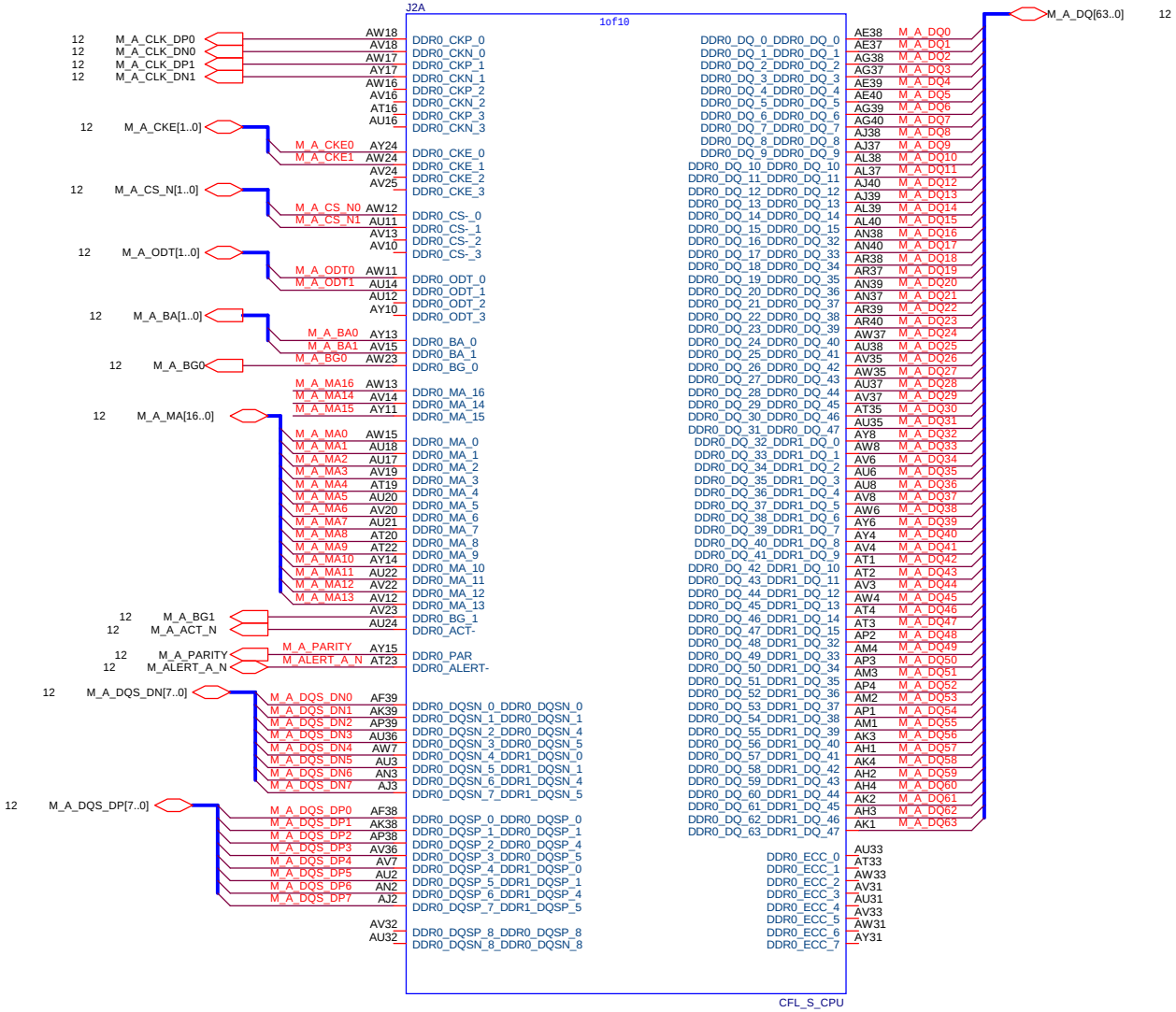
NOTE CMD SIGNALS FOR DIFFERENT MEMORY TECHNOLOGIES:
LEFT TO RIGHT: DDR3L/LPDDR3/DDR4



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Document Number : <Doc>			
Prepared by : KERRY HUANG			
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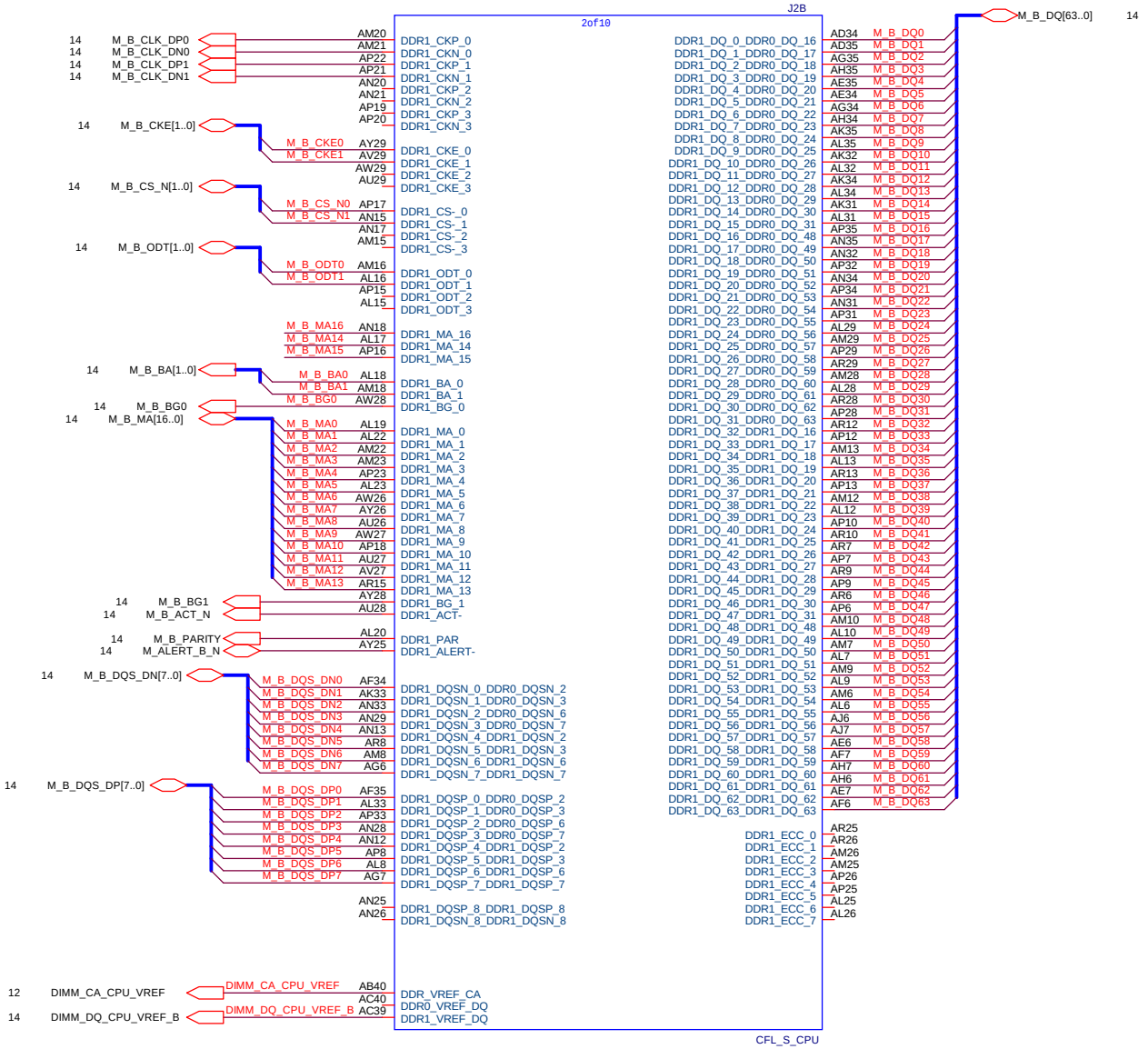
NOTE CMD SIGNALS FOR DIFFERENT MEMORY TECHNOLOGIES:
LEFT TO RIGHT: DDR4/DDR3L/LPDDR3/



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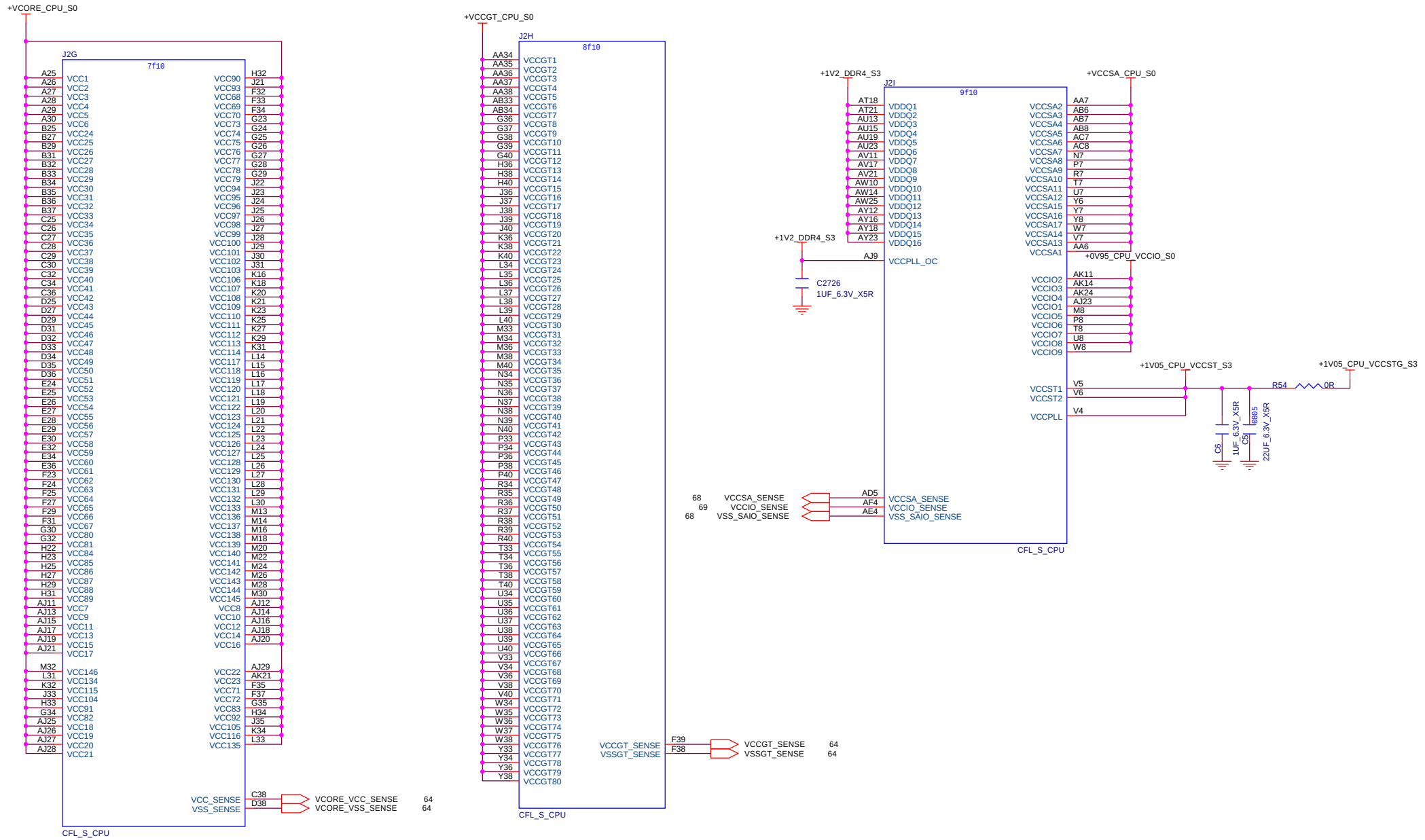
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 7 of 99



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Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Tuesday, March 06, 2018
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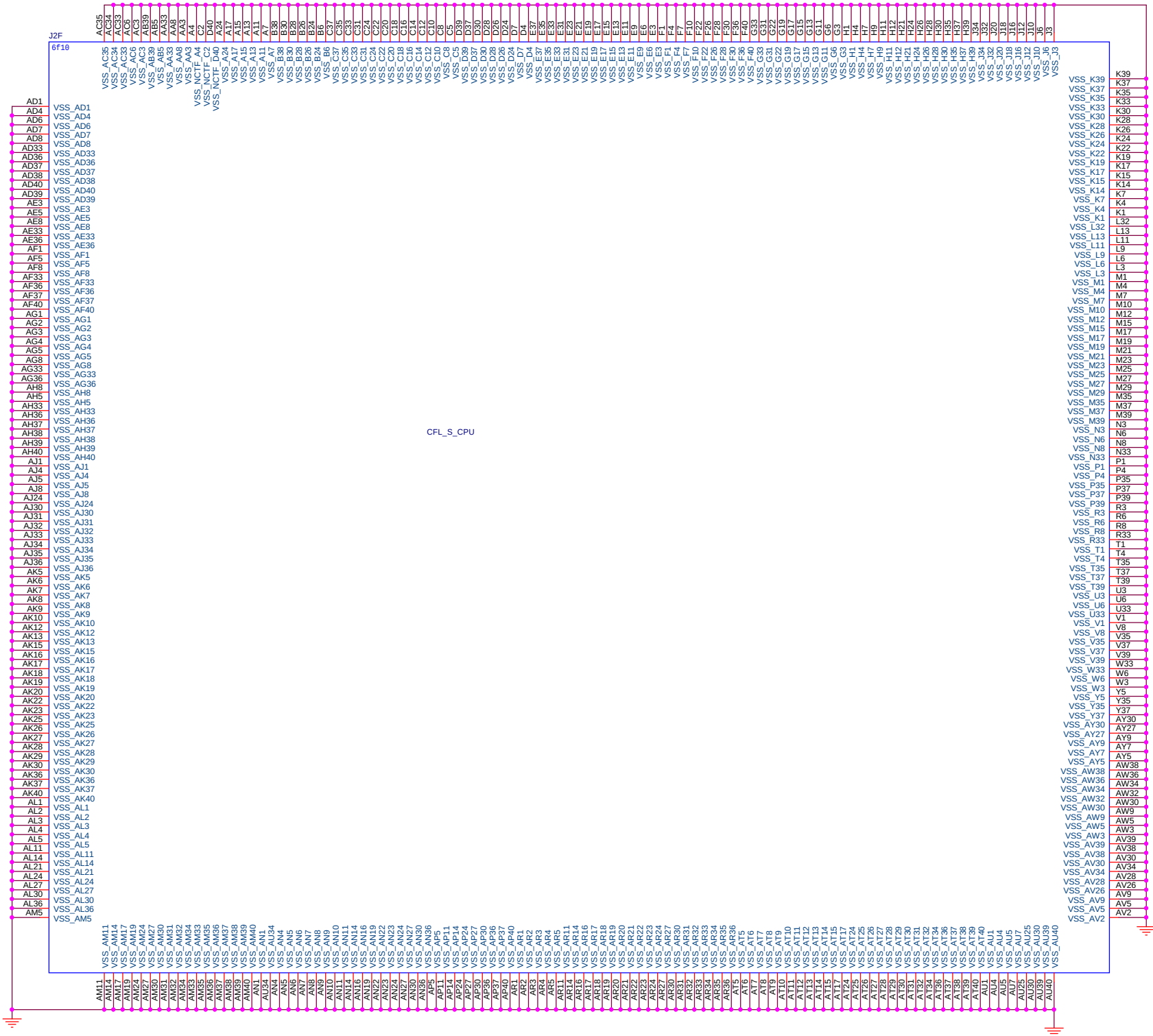

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Document Number : <Doc>	
Prepared by : KERRY HUANG	
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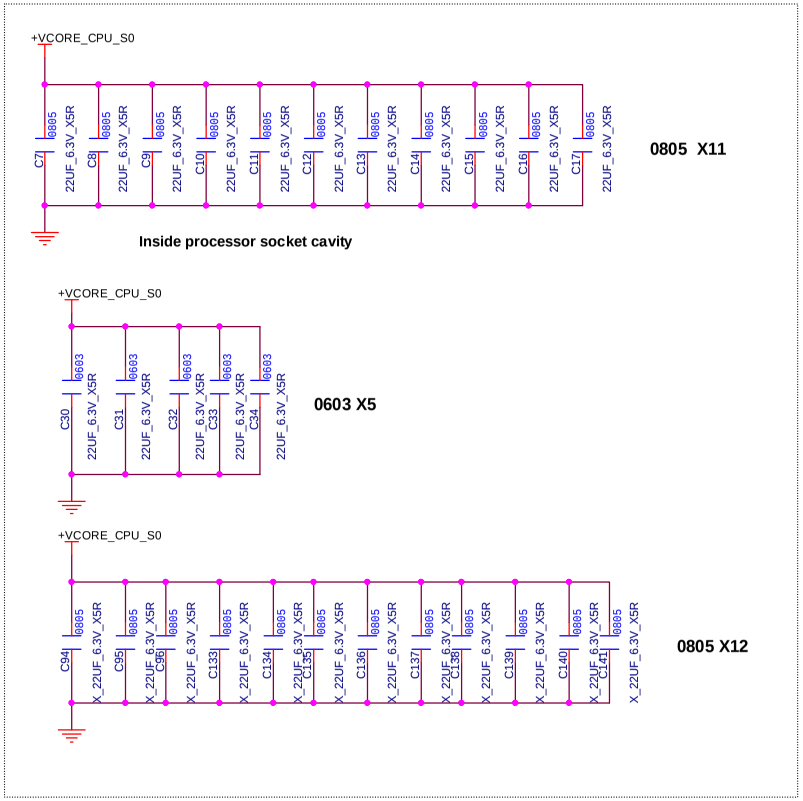
CPU DECOUPLING



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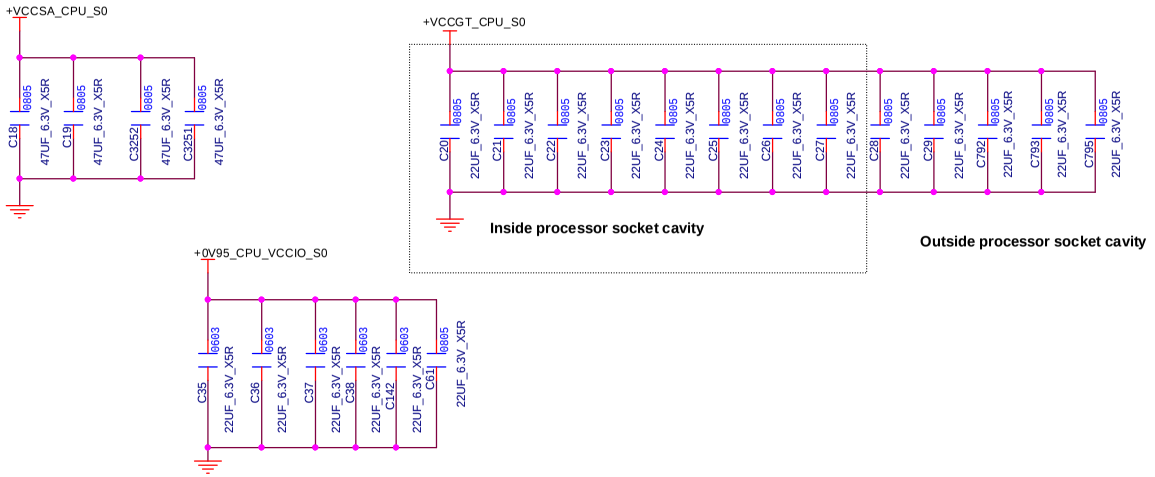

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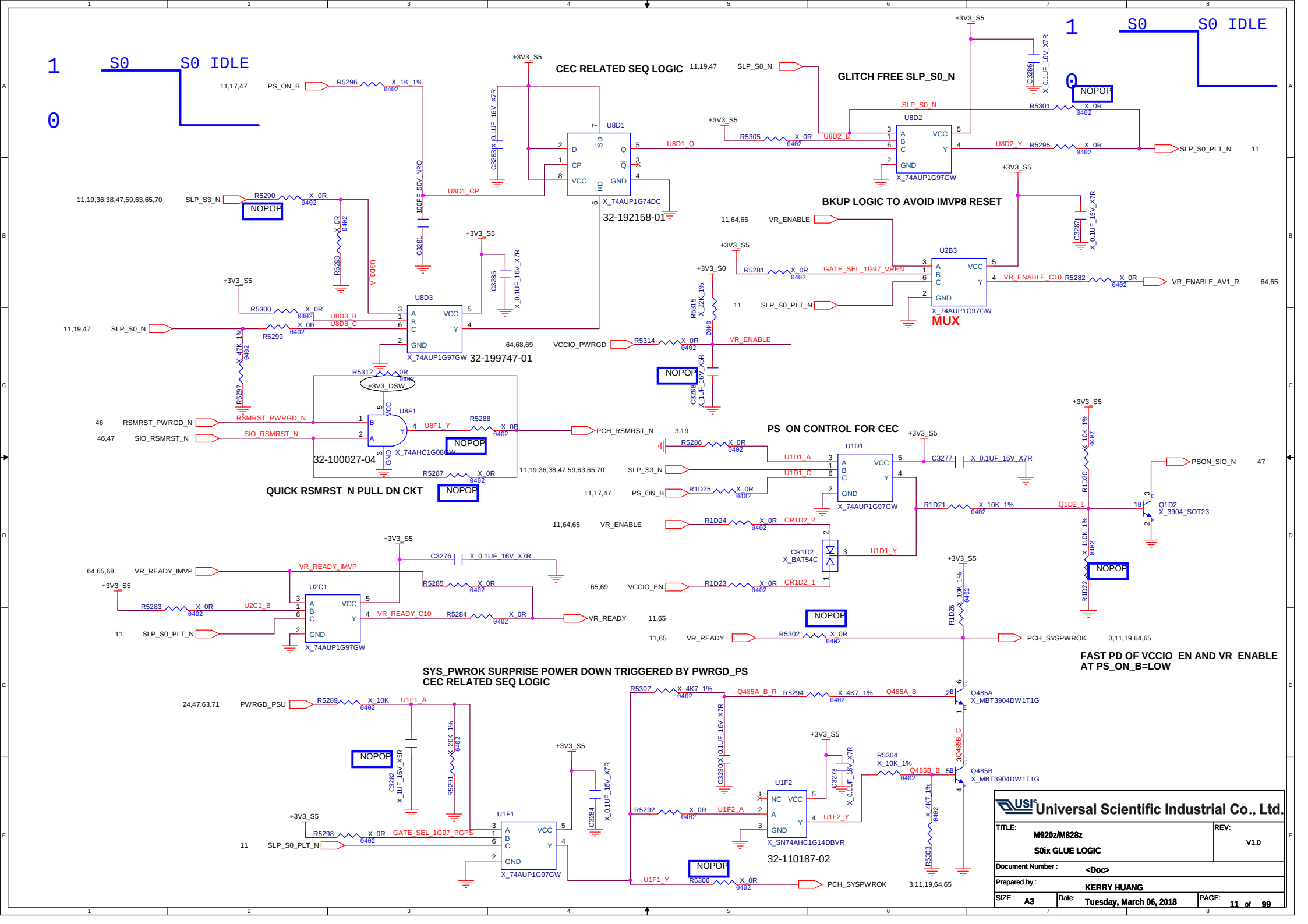
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 10 of 99


1 S0 S0 IDLE
0
1 S0 S0 IDLE
0
CEC RELATED SEQ LOGIC
GLITCH FREE SLP_S0_N
BKUP LOGIC TO AVOID IMVP8 RESET
MUX
QUICK RSMRST_N PULL DN CKT
PS_ON CONTROL FOR CEC
SYS_PWROK SURPRISE POWER DOWN TRIGGERED BY PWRGD_PS
CEC RELATED SEQ LOGIC
FAST PD OF VCCIO_EN AND VR_ENABLE AT PS_ON_B=LOW
NOPOP
32-192158-01
32-199747-01
32-100027-04
32-110187-02
PS_ON_B
SLP_S3_N
SLP_S0_N
SLP_S0_PLT_N
VR_ENABLE
VR_ENABLE_AV1_R
VR_READY_IMVP
VR_READY
VCCIO_EN
VCCIO_PWRGD
PWRGD_PSU
RSMRST_PWRGD_N
SIO_RSMRST_N
PCH_RSMRST_N
PCH_SYSPWROK
PSON_SIO_N
GATE_SEL_1G97_VREN
GATE_SEL_1G97_PGPS
U8D1
U8D2
U8D3
U2B3
U2C1
U1D1
U1F1
U1F2
U8F1
Q485A
Q485B
Q1D2
X_74AUP1G97GW
X_74AUP1G74DC
X_74AHC1G08GW
X_SN74AHC1G14DBVR
X_MBT3904DW1T1G
X_3904_SOT23
CR1D2
X_BAT54C
+3V3_S5
+3V3_S0
+3V3_DSW
Universal Scientific Industrial Co., Ltd.
TITLE: M920z/M828z
S0ix GLUE LOGIC
REV: V1.0
Document Number : <Doc>
Prepared by : KERRY HUANG
SIZE : A3
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DDR4 SO-DIMM CHANNEL A

CHANNEL A
ADDRESS:0XA0 000

DIMM1

CAD Note:
all signal should have
10 mil trace width

Data bit swapping within a byte lane

FOR ECC

FOR ECC

J3A

1of2

DDR4SODIMM260_RVS_ADDR0206-P023 BLACK

4.0H

M_A_DQ[63..0] 6

M_A_MA[16..0] 6

M_A_PARITY 6
M_A_ALERT_A_N 6
M_A_ACT_N 6
M_A_BG0 6
M_A_BG1 6
M_A_CLK_DP0 6
M_A_CLK_DN0 6
M_A_CLK_DP1 6
M_A_CLK_DN1 6
M_RESET_N 14,19
M_A_CS_N[1..0] 6
M_A_CKE[1..0] 6
M_A_BA[1..0] 6
SMB_DATA 3,14,24
SMB_CLK 24

CAD NOTE:
PLACE RESISTORS
CLOSE TO CH_A DIMMS
ON DIMM_VREF_A

PLACE NEAR DIMM AREA

NC
For Intel MOW

Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z DDR4 SO-DIMM CHANNEL A	REV: V1.0
Document Number : <Doc>	
Prepared by : KERRY HUANG	
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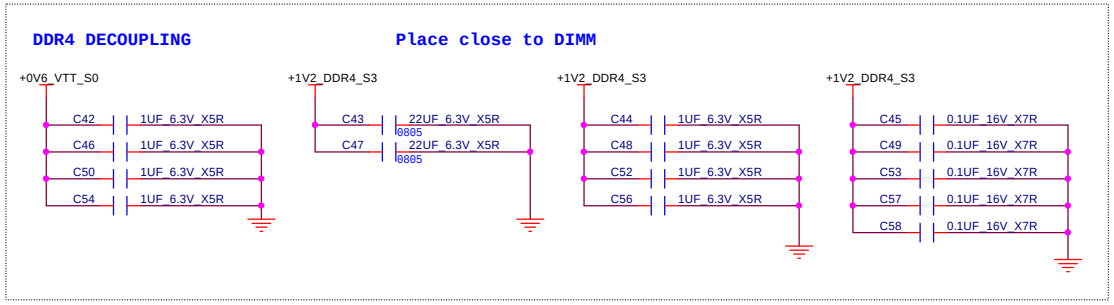
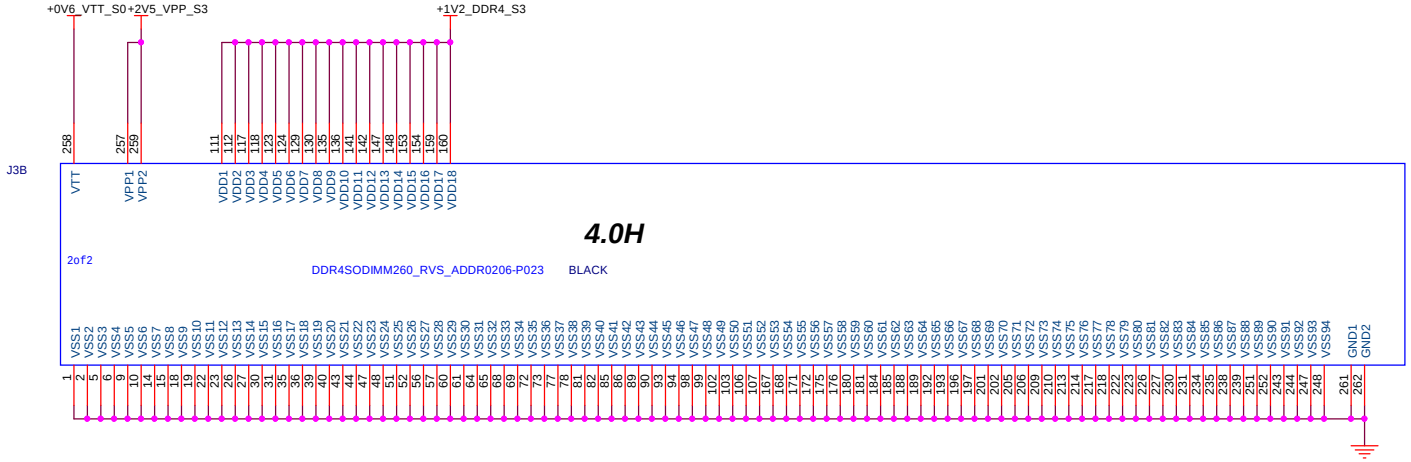
DDR4 SO-DIMM CHANNEL A





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TITLE: M920z/M828z DDR4 SO-DIMM CHANNEL A POWER		REV: V1.0
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DDR4 SO-DIMM CHANNEL B

CHANNEL B
ADDRESS:0XA4 010

DIMM2

CAD Note:
all signal should have
10 mil trace width

M_B_DQS_DP7
M_B_DQS_DN7
M_B_DQS_DP6
M_B_DQS_DN6
M_B_DQS_DP5
M_B_DQS_DN5
M_B_DQS_DP4
M_B_DQS_DN4
M_B_DQS_DP3
M_B_DQS_DN3
M_B_DQS_DP2
M_B_DQS_DN2
M_B_DQS_DP1
M_B_DQS_DN1
M_B_DQS_DP0
M_B_DQS_DN0
M_B_ODT1
M_B_ODT0

+1V2_DDR4_S3
R69 240R 1% 0402
M_B_TS_EVENT_N

FOR ECC

Data bit swapping within a byte lane

M_B_DQ[63..0]

FOR ECC
+1V2_DDR4_S3

J4A
1of2

DDR4SODIMM260_RVS_ADDR0070-P037 BLACK **8.0H**

+1V2_DDR4_S3
+3V3_S0
R70 0R
CB6

M_B_PARITY
M_ALERT_B_N
M_B_ACT_N
M_B_BG0
M_B_BG1
M_B_CLK_DP0
M_B_CLK_DN0
M_B_CLK_DP1
M_B_CLK_DN1
M_RESET_N 12,19
M_B_CS_N[1..0]
M_B_CKE[1..0]
M_B_BA[1..0]
SMB_DATA 3,12,24
SMB_CLK 24

M_B_MA[16..0]

CAD NOTE:
PLACE RESISTORS
CLOSE TO CH_B DIMMS
ON DIMM_VREF_B

+1V2_DDR4_S3
R60 1K_1%
R64 1K_1%
C2725 1UF_6.3V_X5R

DIMM_DQ_CPU_VREF_B
R66 2R_1% 0402
DIMM_CA_VREF_B
C41 0.022UF_16V_X7R
DIMM_CA_CPU_VREF_RC_B
R68 24R9_1%
C2176 4.7UF_6.3V_X5R 0603
CB5 1UF_10V_X5R 0603
C786 1UF_6.3V_X5R
C800 1UF_6.3V_X5R
PLACE NEAR DIMM AREA

M_RESET_N
C59 X_220PF_50V_NPO
NC
For Intel MOW

Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z DDR4 SO-DIMM CHANNEL B	REV: V1.0
Document Number : <Doc>	
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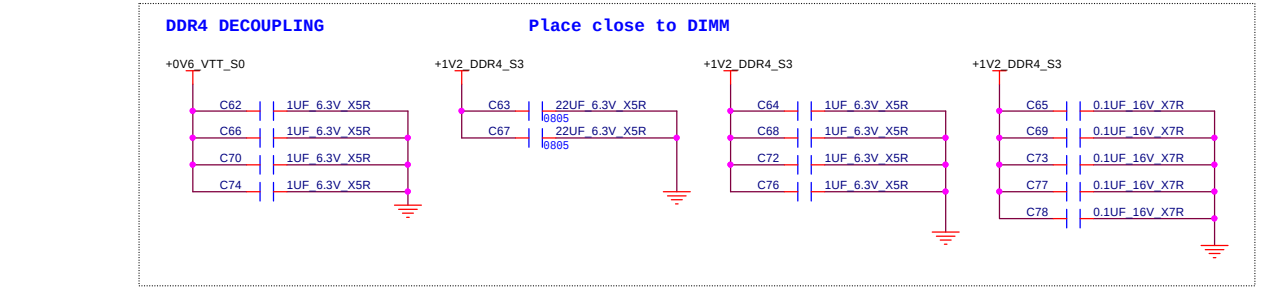
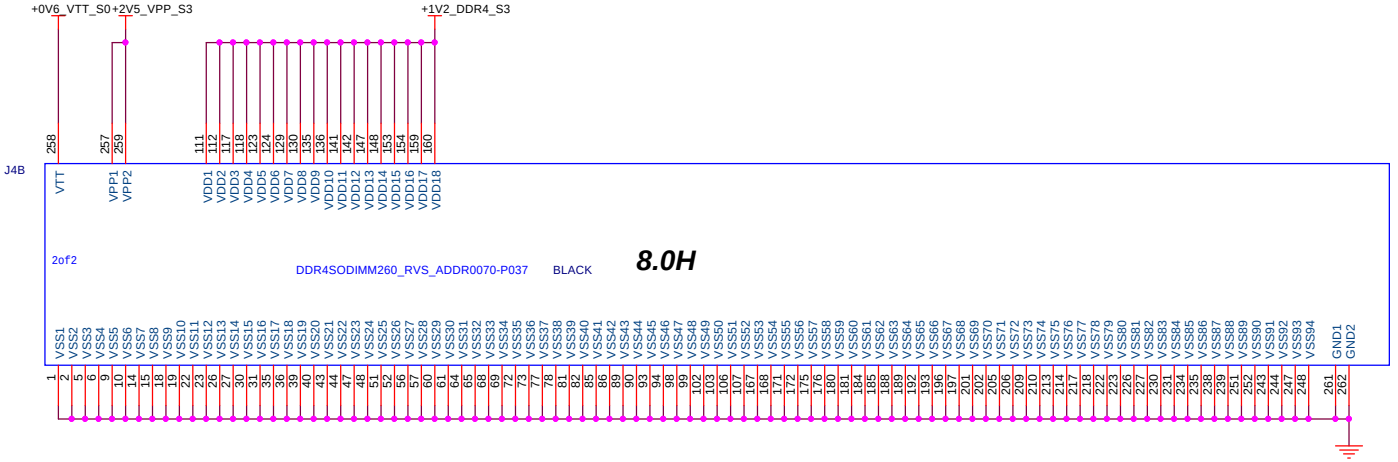
DDR4 SO-DIMM CHANNEL B





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Document Number : <Doc>		
Prepared by : KERRY HUANG		
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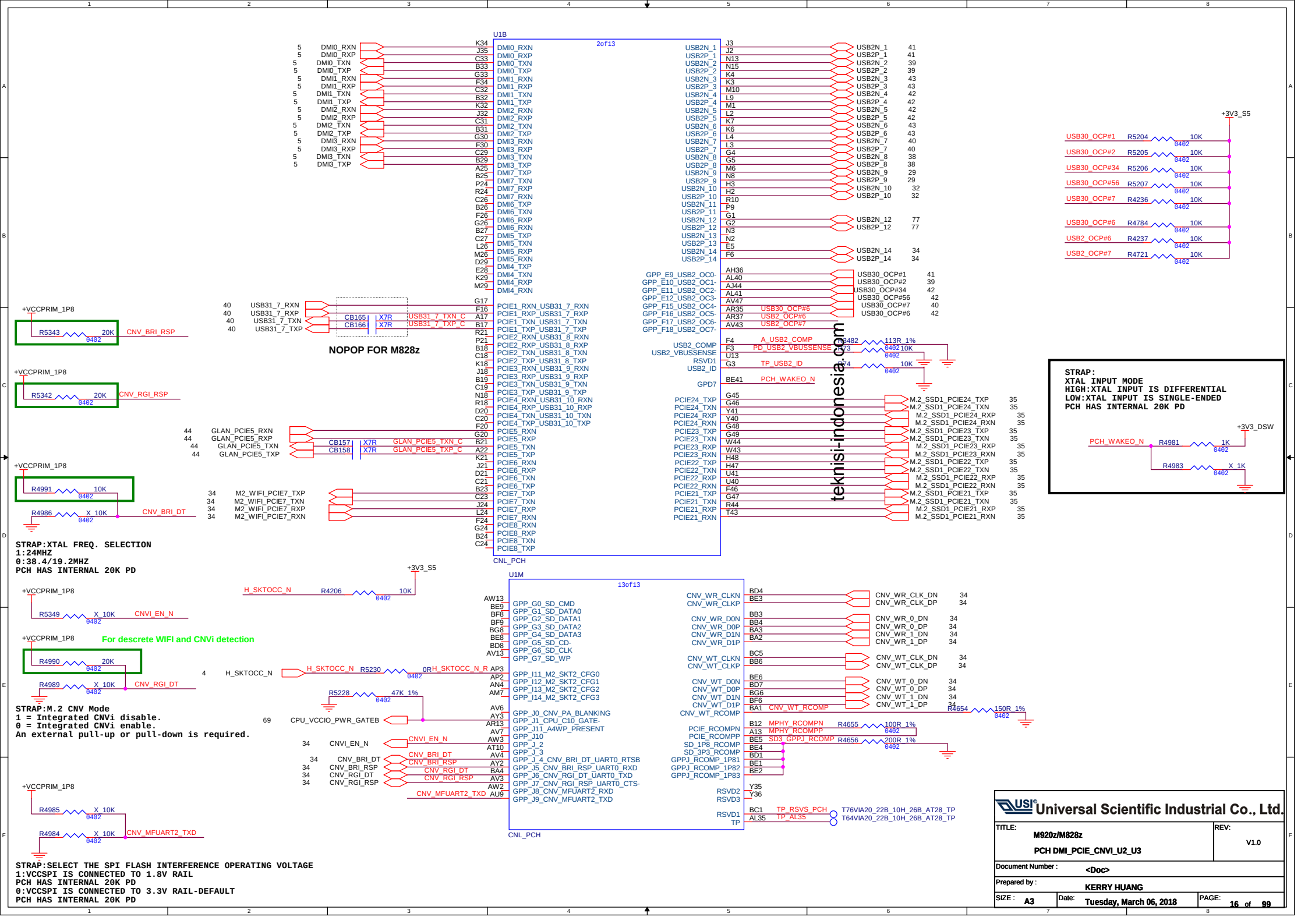
U1B
2of13
CNL_PCH
NOPOP FOR M828z
STRAP:
XTAL INPUT MODE
HIGH:XTAL INPUT IS DIFFERENTIAL
LOW:XTAL INPUT IS SINGLE-ENDED
PCH HAS INTERNAL 20K PD
STRAP:XTAL FREQ. SELECTION
1:24MHZ
0:38.4/19.2MHZ
PCH HAS INTERNAL 20K PD
STRAP:M.2 CNV Mode
1 = Integrated CNVi disable.
0 = Integrated CNVi enable.
An external pull-up or pull-down is required.
For descrete WIFI and CNVi detection
STRAP:SELECT THE SPI FLASH INTERFERENCE OPERATING VOLTAGE
1:VCCSPI IS CONNECTED TO 1.8V RAIL
PCH HAS INTERNAL 20K PD
0:VCCSPI IS CONNECTED TO 3.3V RAIL-DEFAULT
PCH HAS INTERNAL 20K PD
U1M
13of13
CNL_PCH
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Universal Scientific Industrial Co., Ltd.
TITLE: M920z/M828z
PCH DMI_PCIE_CNVI_U2_U3
REV: V1.0
Document Number : <Doc>
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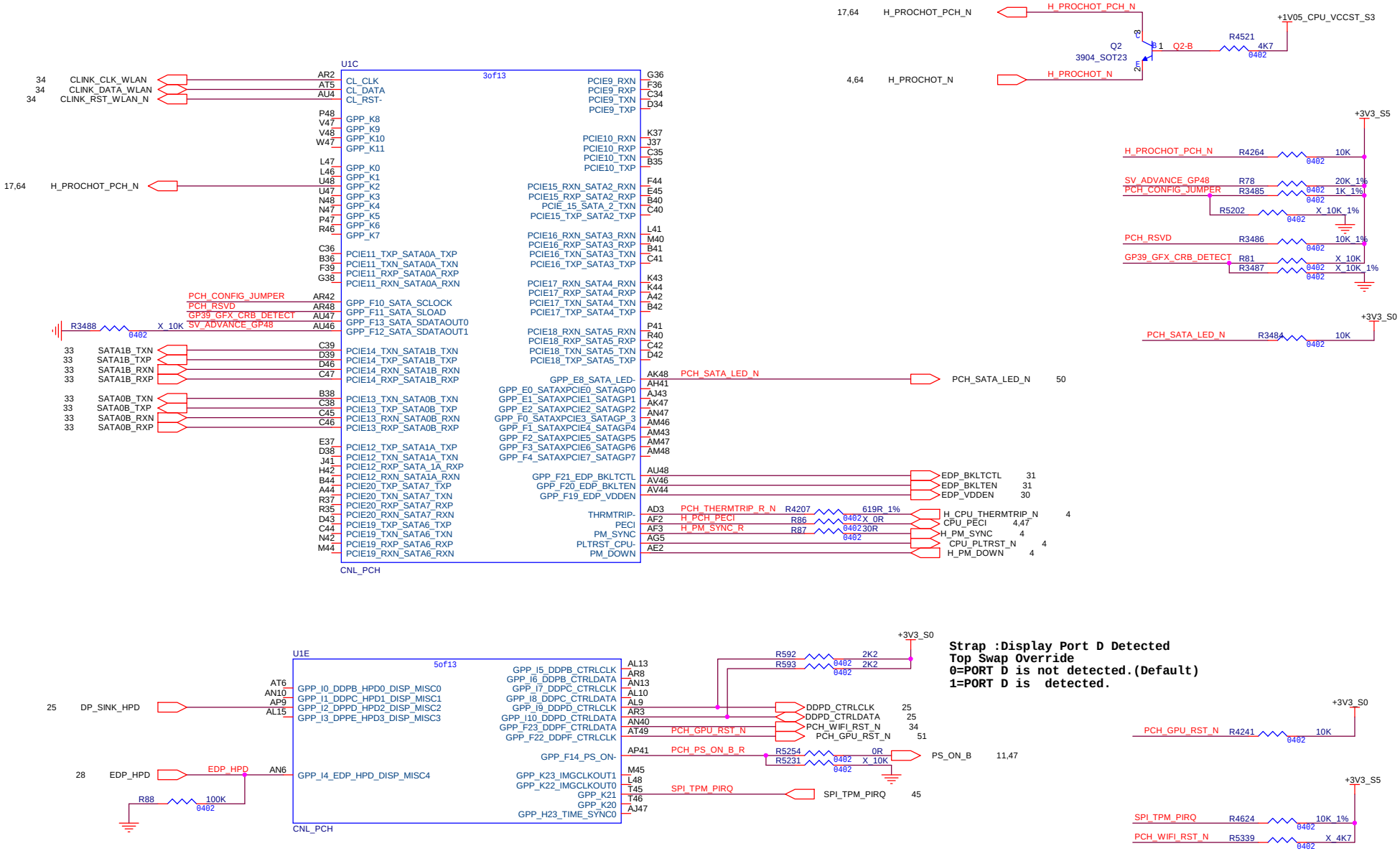

Universal Scientific Industrial Co., Ltd.		
TITLE: M920z/M828z PCH PCIE_SATA_DDC_CLINK		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
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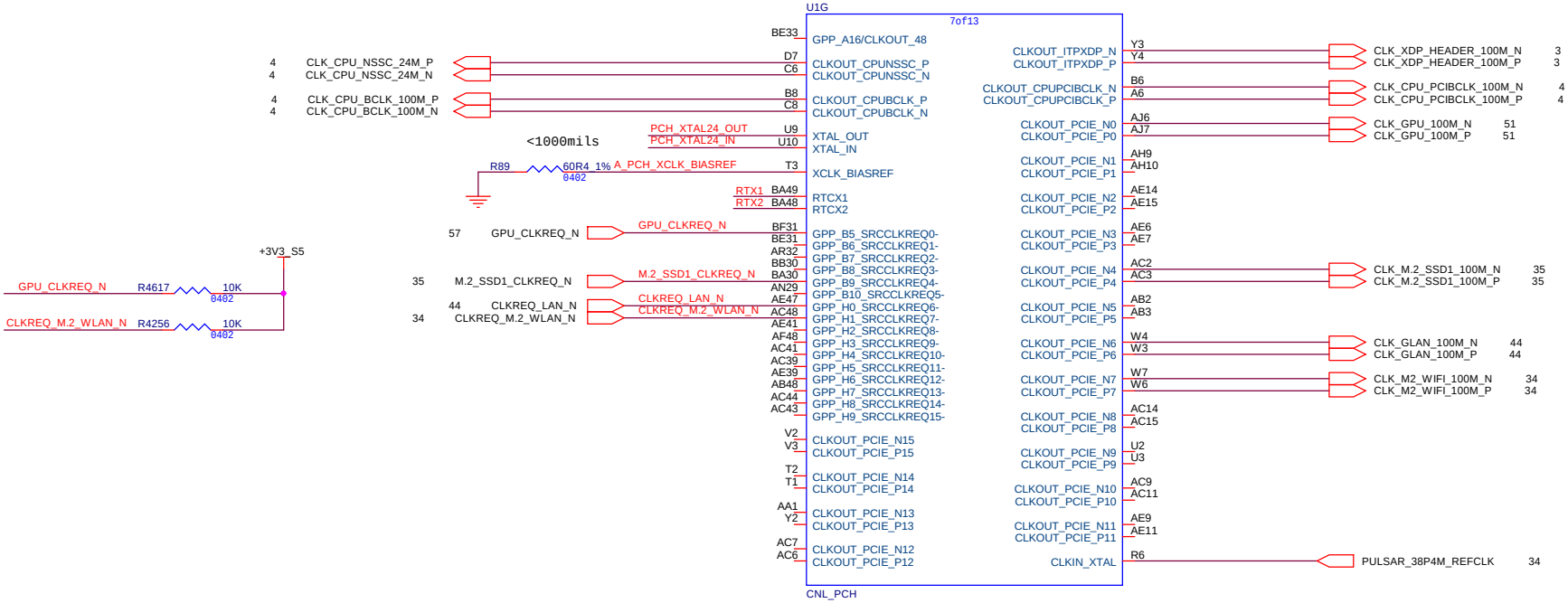
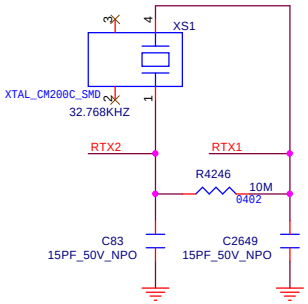
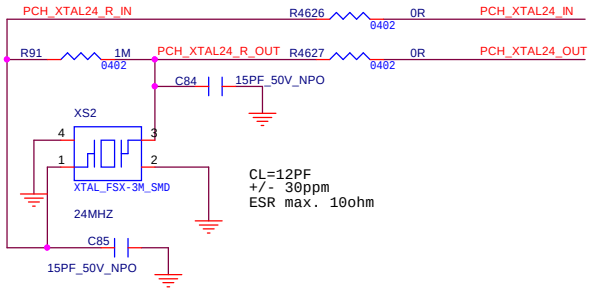
PCH CLOCK



RTC SOURCE

10PPM 12.5PF





Universal Scientific Industrial Co., Ltd.		
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Document Number : <Doc>		
Prepared by : KERRY HUANG		
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CLOSE TO PCH

CLOSE TO DIMM

STUFF R130 FOR NON SUPPORT HANDSHAKE MECHANISM.

U1D

CNL_PCH

1.8V level

For MS debug

Strap :
DCI ENABLE STRAP ENABLED IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD

To enable Direct Connect Interface (DCI)

Strap :
Top Swap Override
0=Disable "Top Swap" mode.((W/ WEAK PD)
1=Enable "Top Swap" mode.

Strap :
TLS Confi-dentiality
0:Disable(W/ WEAK PD)
1:Enable

Strap :
eSPI or LPC
0:LPC is selected for EC (W/ WEAK PD)
1:eSPI is selected for EC

Warning: If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' as well (SAFS is disabled)

ME DISABLE HEADER

Strap :Flash Descriptor Security Override

FLASH SECURITY OVERRIDE

HIGH:Disable ME in Manufacturing Mode

PLACE CLOSE TO PCH WITHIN 1.1INCH

Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z PCH HDA_SMB_MISC.	REV: V1.0
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Prepared by : KERRY HUANG	
SIZE : A3	Date: Tuesday, March 06, 2018
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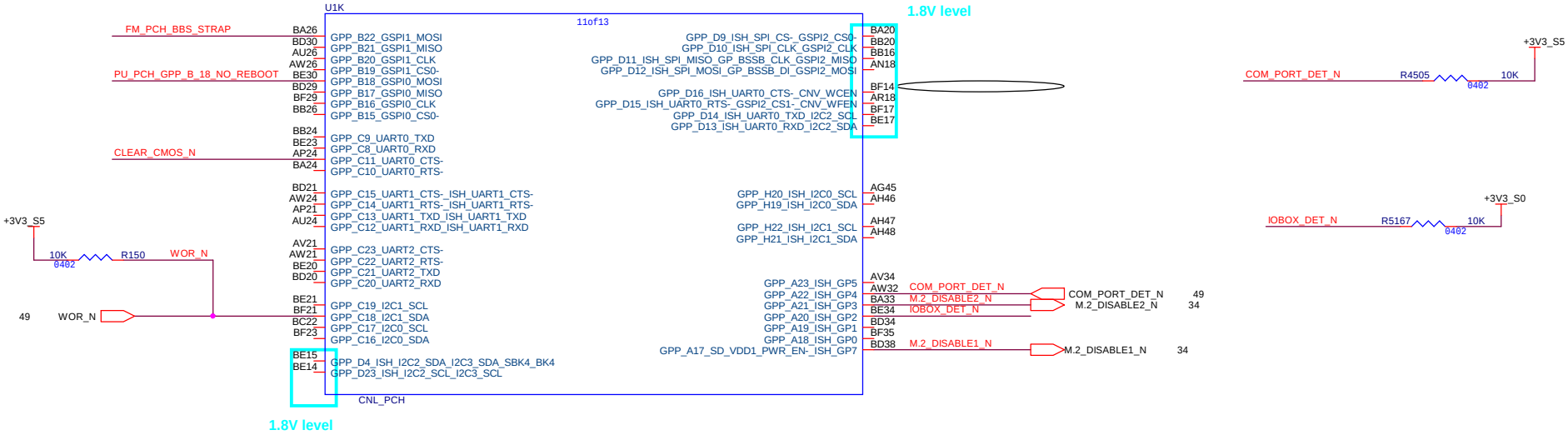
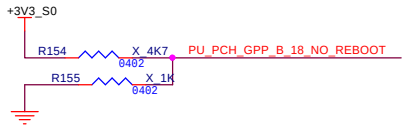
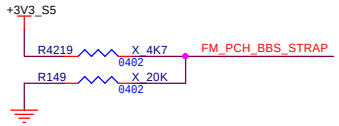


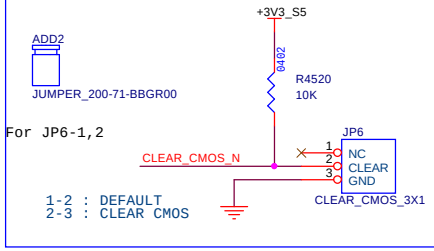
Strap :
No Reboot
0=Disable "No Reboot" mode(W/ WEAK PD)
1=Enable "No Reboot" mode



Strap :
Boot BIOS Strap Bit 10 BBS
0:SPI (W/ WEAK PD)
1:LPC



CLEAR CMOS



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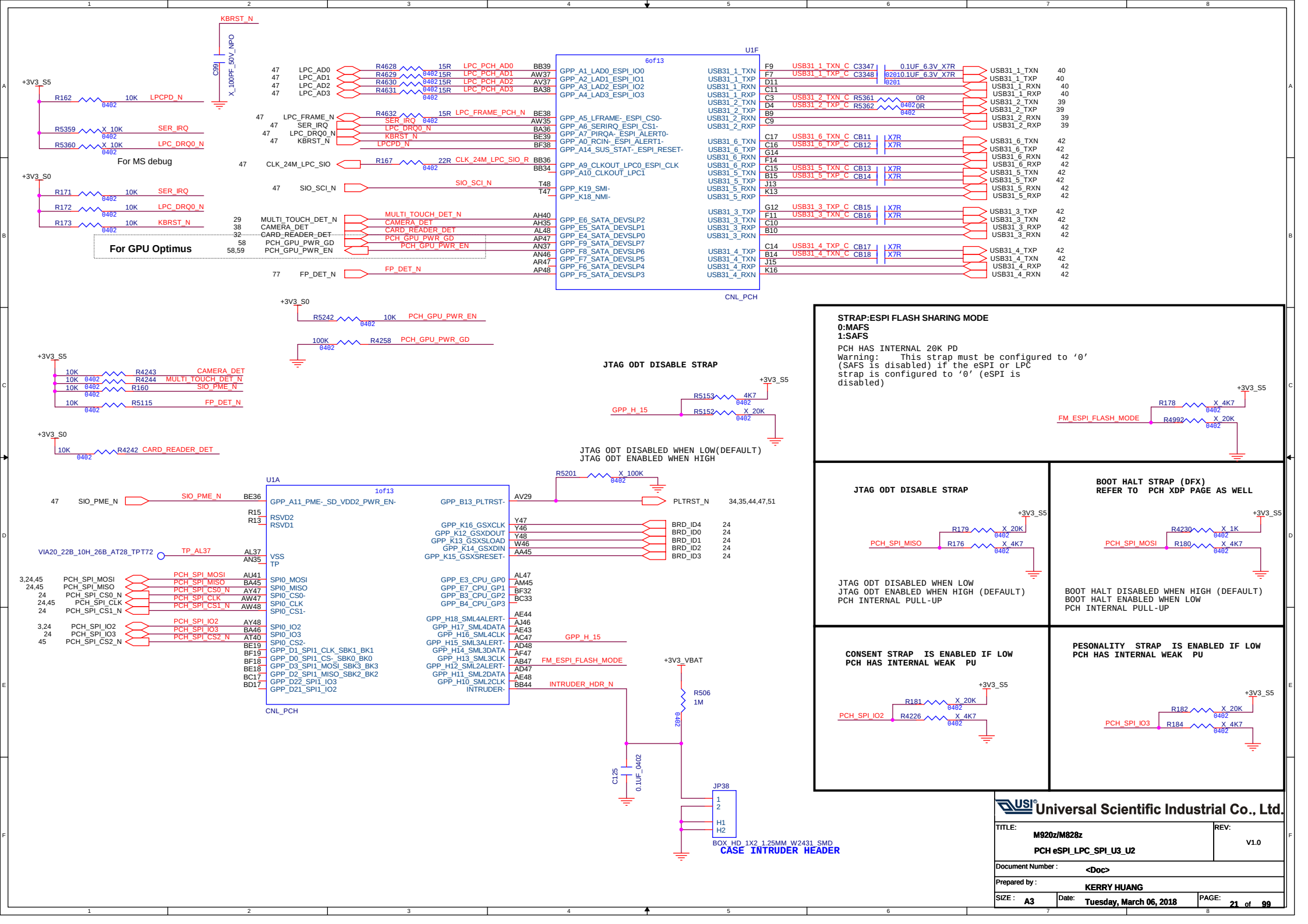
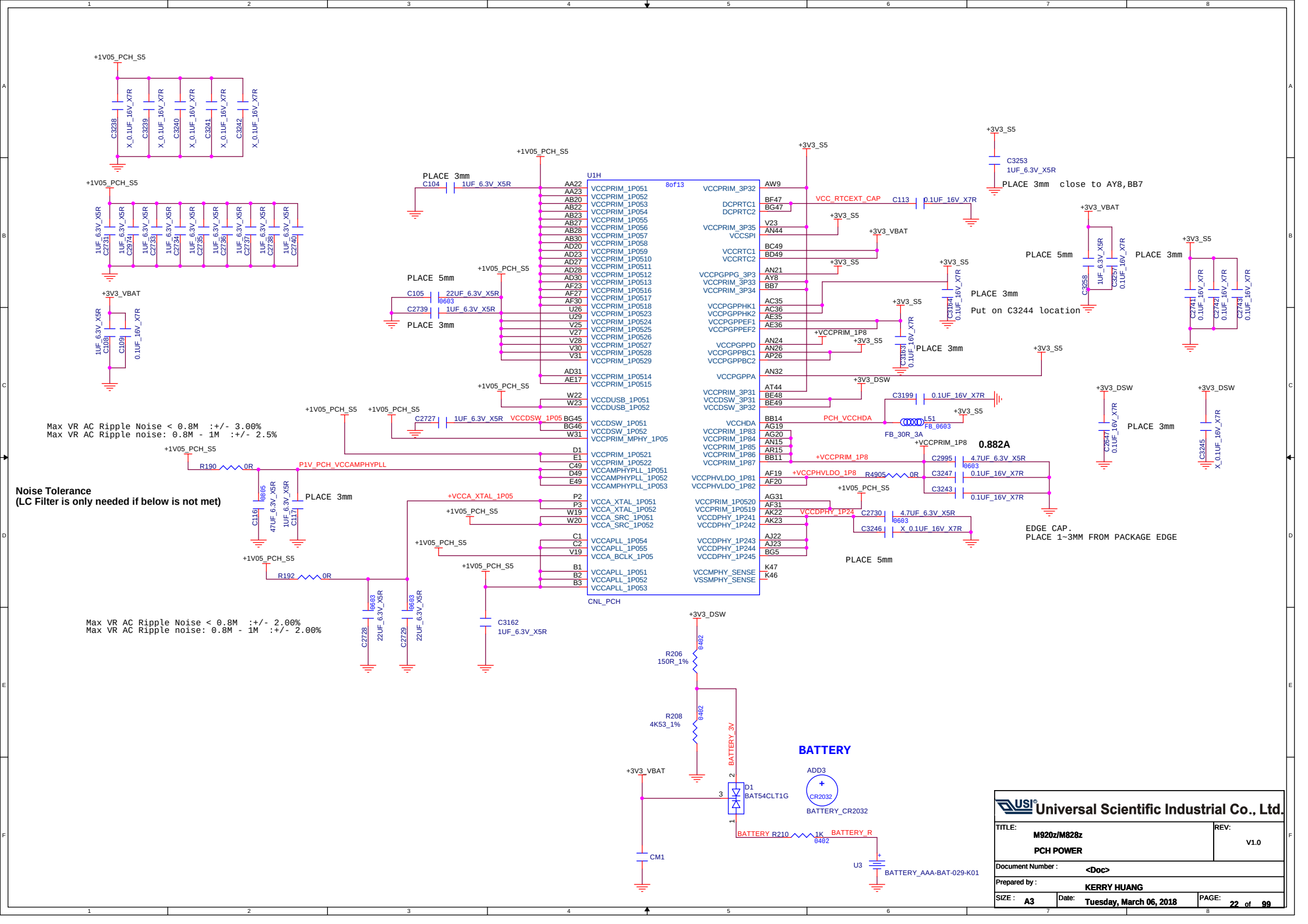
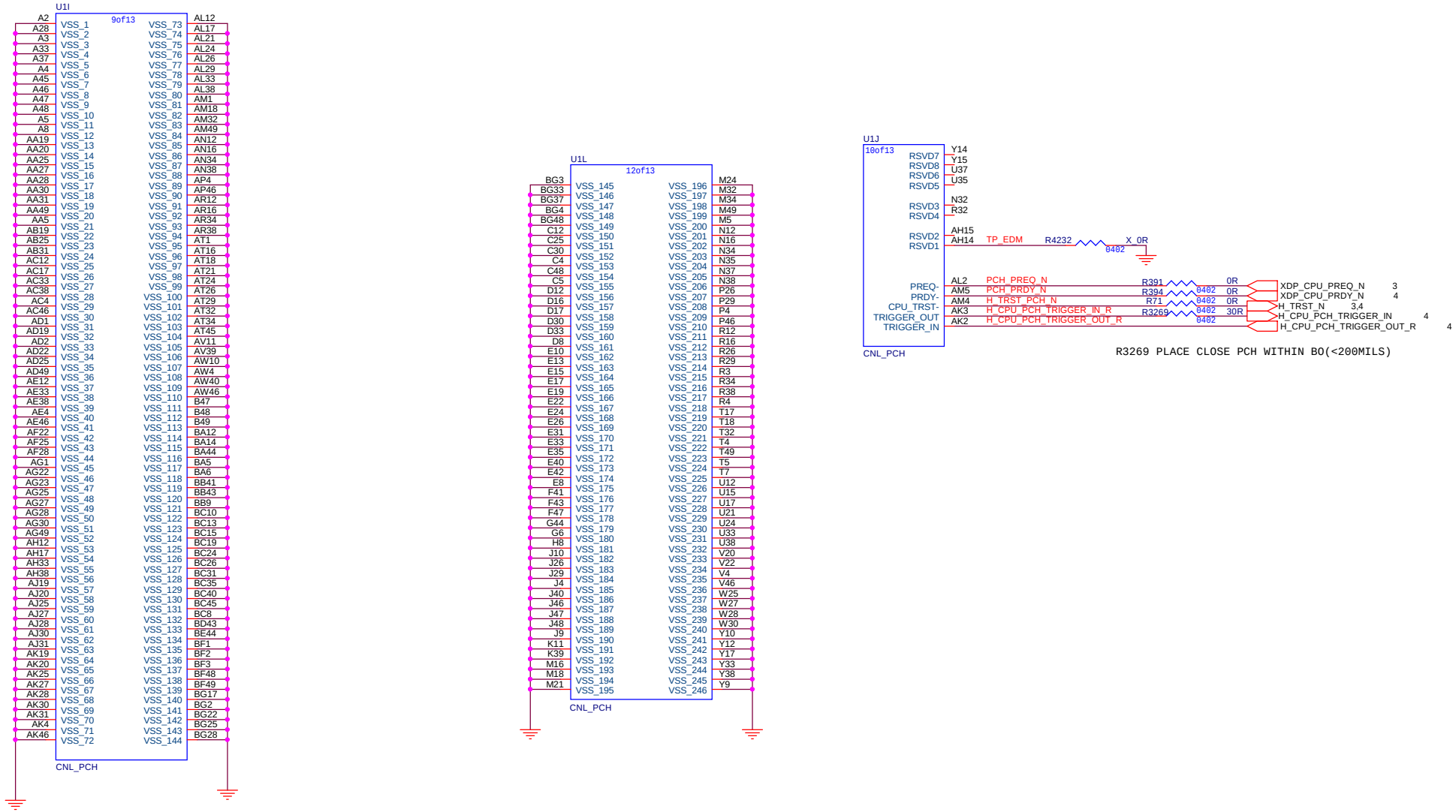
TITLE: M920z/M828z PCH GPIO_CLRCMOS		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 20 of 99


KBRST_N
C99
X_100PF_50V_NPO
+3V3_S5
R162 10K LPCPD_N
R5359 X_10K SER_IRQ
R5360 X_10K LPC_DRQ0_N
For MS debug
+3V3_S0
R171 10K SER_IRQ
R172 10K LPC_DRQ0_N
R173 10K KBRST_N
For GPU Optimus
47 LPC_AD0
47 LPC_AD1
47 LPC_AD2
47 LPC_AD3
R4628 15R LPC_PCH_AD0
R4629 15R LPC_PCH_AD1
R4630 15R LPC_PCH_AD2
R4631 15R LPC_PCH_AD3
47 LPC_FRAME_N
47 SER_IRQ
47 LPC_DRQ0_N
47 KBRST_N
R4632 15R LPC_FRAME_PCH_N
SER_IRQ
LPC_DRQ0_N
KBRST_N
LPCPD_N
47 CLK_24M_LPC_SIO
R167 22R CLK_24M_LPC_SIO_R
47 SIO_SCI_N
SIO_SCI_N
29 MULTI_TOUCH_DET_N
38 CAMERA_DET
32 CARD_READER_DET
58 PCH_GPU_PWR_GD
58,59 PCH_GPU_PWR_EN
77 FP_DET_N
MULTI_TOUCH_DET_N
CAMERA_DET
CARD_READER_DET
PCH_GPU_PWR_GD
PCH_GPU_PWR_EN
FP_DET_N
U1F
6of13
GPP_A1_LAD0_ESPI_IO0
GPP_A2_LAD1_ESPI_IO1
GPP_A3_LAD2_ESPI_IO2
GPP_A4_LAD3_ESPI_IO3
GPP_A5_LFRAME-_ESPI_CS0-
GPP_A6_SERIRQ_ESPI_CS1-
GPP_A7_PIRQA-_ESPI_ALERT0-
GPP_A0_RCIN-_ESPI_ALERT1-
GPP_A14_SUS_STAT-_ESPI_RESET-
GPP_A9_CLKOUT_LPC0_ESPI_CLK
GPP_A10_CLKOUT_LPC1
GPP_K19_SMI-
GPP_K18_NMI-
GPP_E6_SATA_DEVSLP2
GPP_E5_SATA_DEVSLP1
GPP_E4_SATA_DEVSLP0
GPP_F9_SATA_DEVSLP7
GPP_F8_SATA_DEVSLP6
GPP_F7_SATA_DEVSLP5
GPP_F6_SATA_DEVSLP4
GPP_F5_SATA_DEVSLP3
BB39
AW37
AV37
BA38
BE38
AW35
BA36
BE39
BF38
BB36
BB34
T48
T47
AH40
AH35
AL48
AP47
AN37
AN46
AR47
AP48
USB31_1_TXN
USB31_1_TXP
USB31_1_RXN
USB31_1_RXP
USB31_2_TXN
USB31_2_TXP
USB31_2_RXN
USB31_2_RXP
USB31_6_TXN
USB31_6_TXP
USB31_6_RXN
USB31_6_RXP
USB31_5_TXN
USB31_5_TXP
USB31_5_RXN
USB31_5_RXP
USB31_3_TXP
USB31_3_TXN
USB31_3_RXP
USB31_3_RXN
USB31_4_TXP
USB31_4_TXN
USB31_4_RXP
USB31_4_RXN
CNL_PCH
F9 USB31_1_TXN_C C3347 0.1UF_6.3V_X7R
F7 USB31_1_TXP_C C3348 0201 0.1UF_6.3V_X7R
D11
C11
C3 USB31_2_TXN_C R5361 0R
D4 USB31_2_TXP_C R5362 0402 0R
B9
C9
C17 USB31_6_TXN_C CB11 X7R
C16 USB31_6_TXP_C CB12 X7R
G14
F14
C15 USB31_5_TXN_C CB13 X7R
B15 USB31_5_TXP_C CB14 X7R
J13
K13
G12 USB31_3_TXP_C CB15 X7R
F11 USB31_3_TXN_C CB16 X7R
C10
B10
C14 USB31_4_TXP_C CB17 X7R
B14 USB31_4_TXN_C CB18 X7R
J15
K16
USB31_1_TXN 40
USB31_1_TXP 40
USB31_1_RXN 40
USB31_1_RXP 40
USB31_2_TXN 39
USB31_2_TXP 39
USB31_2_RXN 39
USB31_2_RXP 39
USB31_6_TXN 42
USB31_6_TXP 42
USB31_6_RXN 42
USB31_6_RXP 42
USB31_5_TXN 42
USB31_5_TXP 42
USB31_5_RXN 42
USB31_5_RXP 42
USB31_3_TXP 42
USB31_3_TXN 42
USB31_3_RXP 42
USB31_3_RXN 42
USB31_4_TXP 42
USB31_4_TXN 42
USB31_4_RXP 42
USB31_4_RXN 42
+3V3_S0
R5242 10K PCH_GPU_PWR_EN
100K R4258 PCH_GPU_PWR_GD
+3V3_S5
10K R4243 CAMERA_DET
10K R4244 MULTI_TOUCH_DET_N
10K R160 SIO_PME_N
10K R5115 FP_DET_N
+3V3_S0
10K R4242 CARD_READER_DET
JTAG ODT DISABLE STRAP
+3V3_S5
R5153 4K7
GPP_H_15
R5152 X_20K
JTAG ODT DISABLED WHEN LOW(DEFAULT)
JTAG ODT ENABLED WHEN HIGH
U1A
1of13
47 SIO_PME_N
SIO_PME_N
BE36
GPP_A11_PME-_SD_VDD2_PWR_EN-
R15 RSVD2
R13 RSVD1
VIA20_22B_10H_26B_AT28_TPT72
TP_AL37
AL37 VSS
AN35 TP
3,24,45 PCH_SPI_MOSI
24,45 PCH_SPI_MISO
24 PCH_SPI_CS0_N
24,45 PCH_SPI_CLK
24 PCH_SPI_CS1_N
3,24 PCH_SPI_IO2
24 PCH_SPI_IO3
45 PCH_SPI_CS2_N
AU41 SPI0_MOSI
BA45 SPI0_MISO
AY47 SPI0_CS0-
AW47 SPI0_CLK
AW48 SPI0_CS1-
AY48 SPI0_IO2
BA46 SPI0_IO3
AT40 SPI0_CS2-
BE19 GPP_D1_SPI1_CLK_SBK1_BK1
BF19 GPP_D0_SPI1_CS-_SBK0_BK0
BF18 GPP_D3_SPI1_MOSI_SBK3_BK3
BE18 GPP_D2_SPI1_MISO_SBK2_BK2
BC17 GPP_D22_SPI1_IO3
BD17 GPP_D21_SPI1_IO2
CNL_PCH
R5201 X_100K
AV29 GPP_B13_PLTRST-
PLTRST_N 34,35,44,47,51
Y47 GPP_K16_GSXCLK
Y46 GPP_K12_GSXDOUT
Y48 GPP_K13_GSXSLOAD
W46 GPP_K14_GSXDIN
AA45 GPP_K15_GSXSRESET-
BRD_ID4 24
BRD_ID0 24
BRD_ID1 24
BRD_ID2 24
BRD_ID3 24
AL47 GPP_E3_CPU_GP0
AM45 GPP_E7_CPU_GP1
BF32 GPP_B3_CPU_GP2
BC33 GPP_B4_CPU_GP3
AE44 GPP_H18_SML4ALERT-
AJ46 GPP_H17_SML4DATA
AE43 GPP_H16_SML4CLK
AC47 GPP_H15_SML3ALERT-
AD48 GPP_H14_SML3DATA
AF47 GPP_H13_SML3CLK
AB47 GPP_H12_SML2ALERT-
AD47 GPP_H11_SML2DATA
AE48 GPP_H10_SML2CLK
BB44 INTRUDER-
GPP_H_15
FM_ESPI_FLASH_MODE
INTRUDER_HDR_N
+3V3_VBAT
R506 1M
20mil
C125 0.1UF_0402
JP38
1
2
H1
H2
BOX_HD_1X2_1.25MM_W2431_SMD
CASE INTRUDER HEADER
STRAP:ESPI FLASH SHARING MODE
0:MAFS
1:SAFS
PCH HAS INTERNAL 20K PD
Warning: This strap must be configured to '0'
(SAFS is disabled) if the eSPI or LPC
strap is configured to '0' (eSPI is
disabled)
+3V3_S5
R178 X_4K7
FM_ESPI_FLASH_MODE
R4992 X_20K
JTAG ODT DISABLE STRAP
+3V3_S5
R179 X_20K
PCH_SPI_MISO
R176 X_4K7
JTAG ODT DISABLED WHEN LOW
JTAG ODT ENABLED WHEN HIGH (DEFAULT)
PCH INTERNAL PULL-UP
BOOT HALT STRAP (DFX)
REFER TO PCH XDP PAGE AS WELL
+3V3_S5
R4230 X_1K
PCH_SPI_MOSI
R180 X_4K7
BOOT HALT DISABLED WHEN HIGH (DEFAULT)
BOOT HALT ENABLED WHEN LOW
PCH INTERNAL PULL-UP
CONSENT STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU
+3V3_S5
R181 X_20K
PCH_SPI_IO2
R4226 X_4K7
PESONALITY STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU
+3V3_S5
R182 X_20K
PCH_SPI_IO3
R184 X_4K7
Universal Scientific Industrial Co., Ltd.
TITLE: M920z/M828z
PCH eSPI_LPC_SPI_U3_U2
REV: V1.0
Document Number : <Doc>
Prepared by : KERRY HUANG
SIZE : A3
Date: Tuesday, March 06, 2018
PAGE: 21 of 99

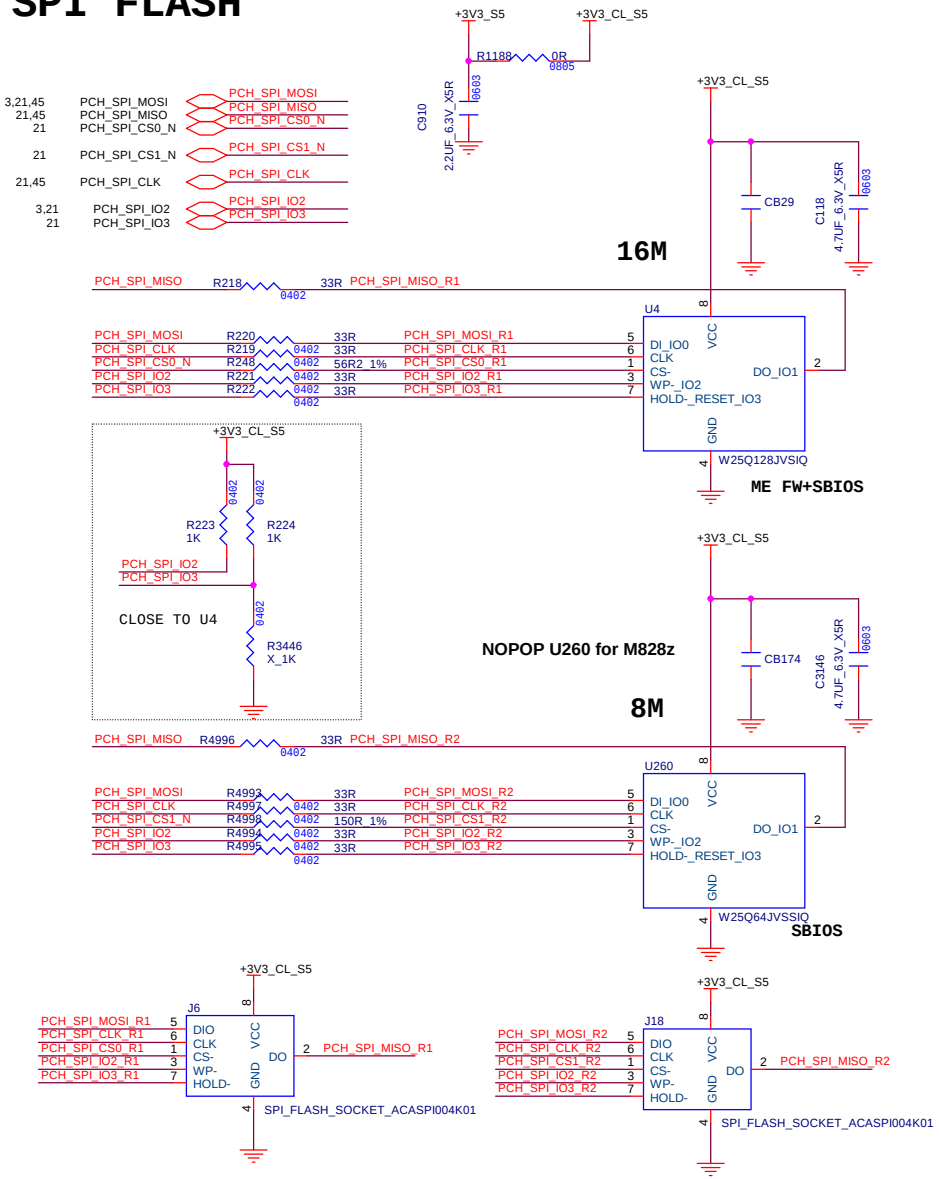


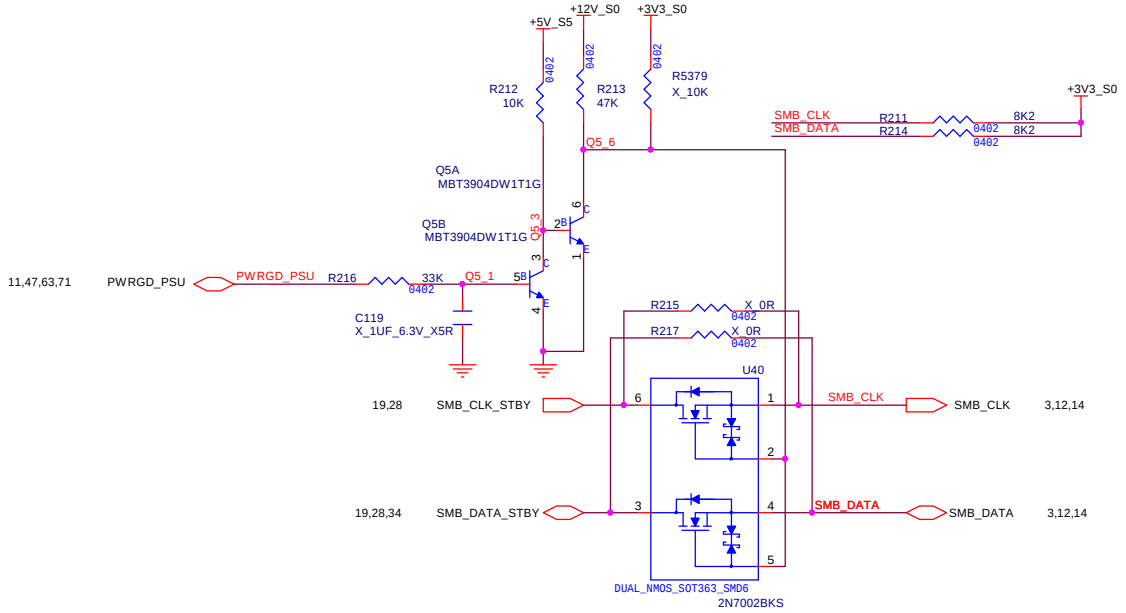
Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z PCH POWER			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 22 of 99	



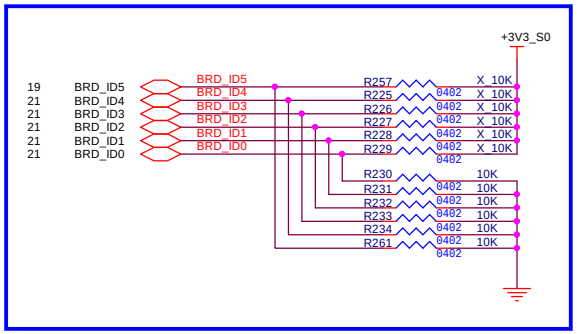
Universal Scientific Industrial Co., Ltd.		
TITLE: M920z/M828z PCH GND		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 23 of 99

SPI FLASH





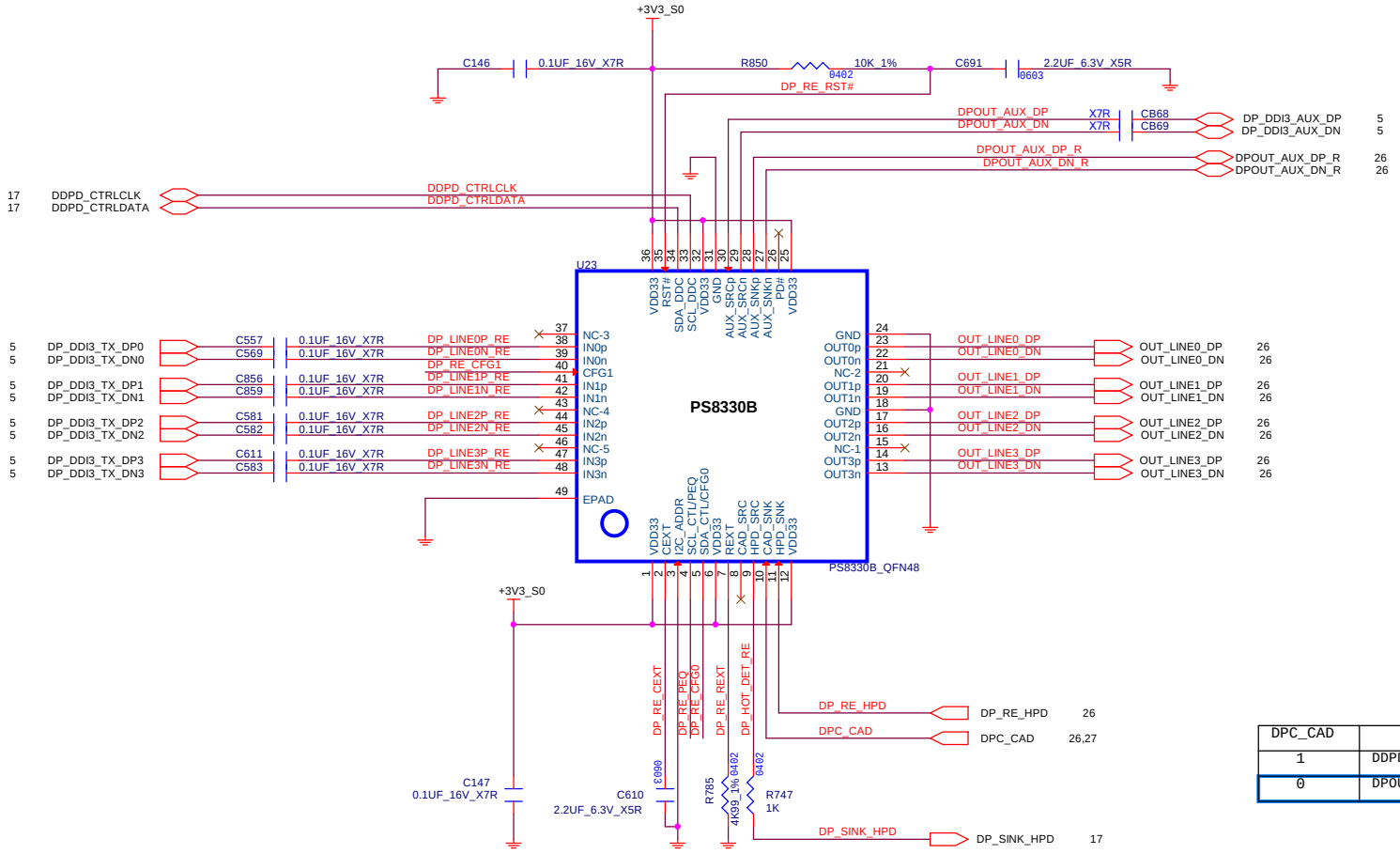
BOARD ID



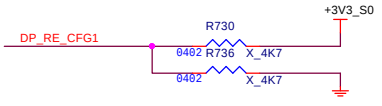
BOARD ID MAP	ID5	ID4	ID3	ID2	ID1	ID0	
M920Z W/GPU	0	0	0	0	0	0	default
M920Z W/O GPU	0	0	0	0	0	1	
M828Z W/GPU	0	0	0	0	1	0	
	0	0	1	0	1	1	
	0	0	1	1	0	0	
	0	0	1	1	0	1	
	0	0	1	1	1	0	

Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z SPI & SMBUS & BOARD ID			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, March 06, 2018		PAGE: 24 of 99

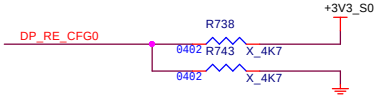
DisplayPort Repeater



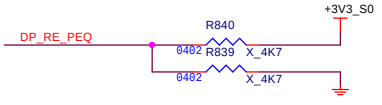
DPC_CAD	OA	OD	
1	DDPD_CTRLDATA	DDPD_CTRLCLK	HDMI
0	DPOUT_AUX_DN	DPOUT_AUX_DP	DP



Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
In Pin Control Mode,
H: default, auto CTS test disable & input offset cancellation enable
L: auto CTS test enable & input offset cancellation enable
M: auto CTS test disable & input offset cancellation disable



CFG0: Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.
CFG0 =
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing



PEQ: programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.
PEQ =
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2

Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z DisplayPort Repeater	REV: V1.0
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Tuesday, March 06, 2018
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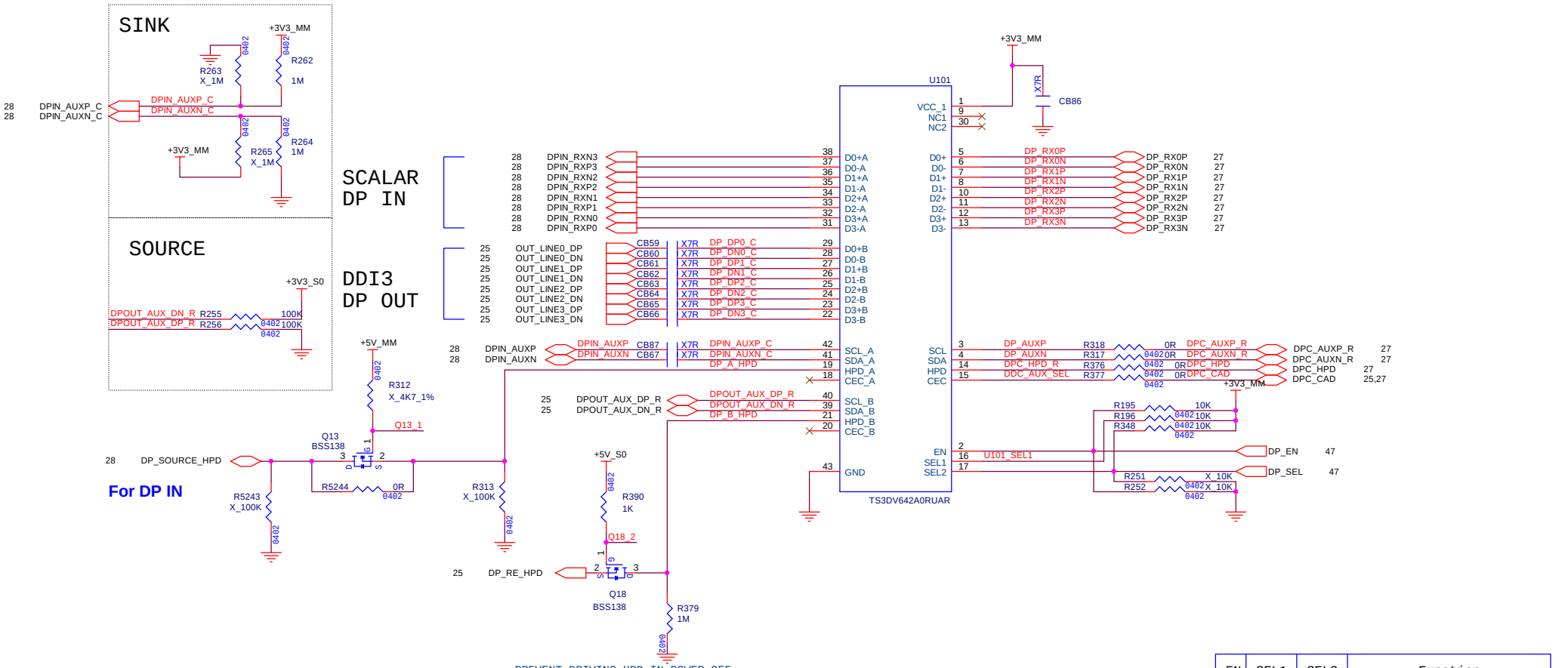
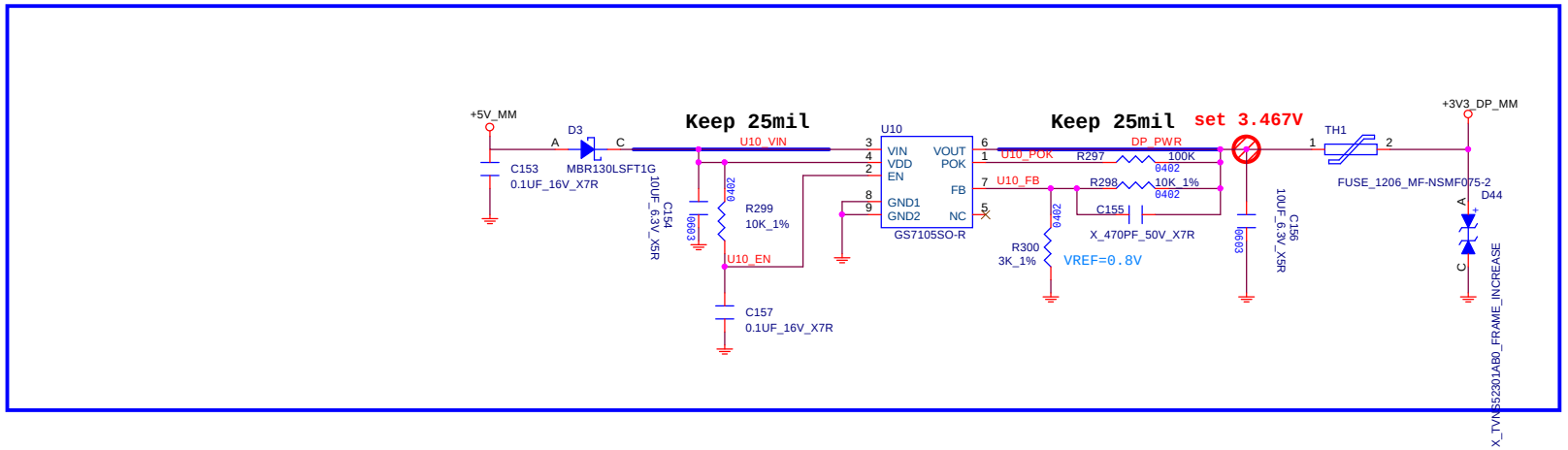


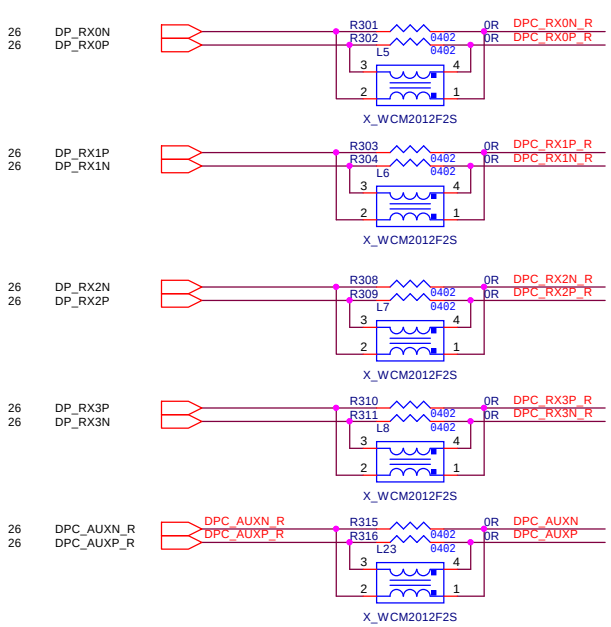
EN	SEL1	SEL2	Function
L	X	X	All I/O = High Impedance
H	H	L	DISPLAY PORT IN
H	H	H	DISPLAY PORT OUT

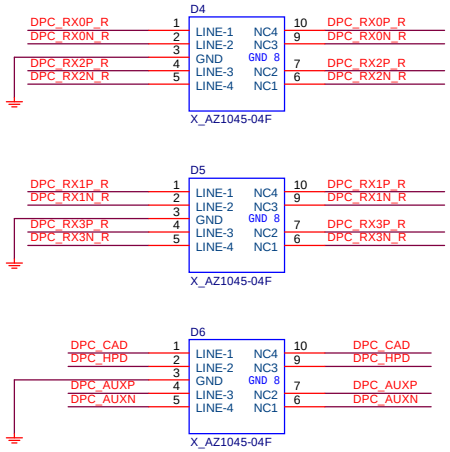
Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z DP MUX/CONN	REV: V1.0
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Tuesday, March 06, 2018
PAGE: 26 of 99	

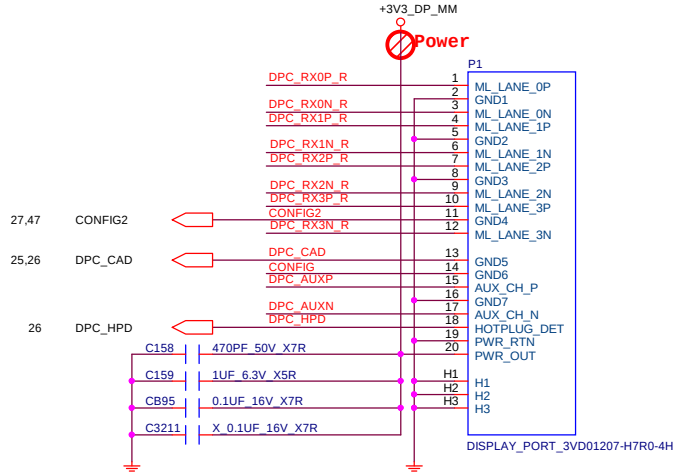


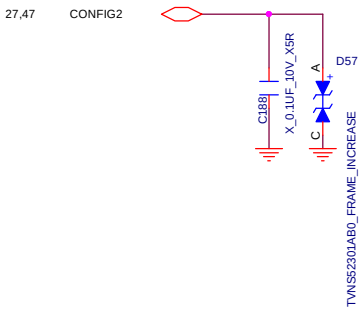
Parameter	Value
Output voltage	3.3V
Maximum output current	0.5A
IC current limit	3.5A
Max. PD(theoretically)	0.85W
Rja	75 °C/W
Enable condition	"+5V_MM" ON

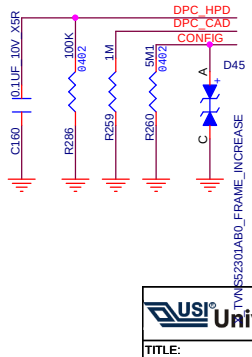
DISPLAY PORT











Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z DP PORT			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, March 06, 2018		PAGE: 27 of 99

598mA

Close to U148

240mA

1.0V/0.3A

RTD2526 only 1 pair LVDS CLK

LVDS OUTPUT

SCALAR FW

U148

RTD2526A-CG

Parameter	Value
Output voltage	1.0V
Maximum output current	0.3A
IC current limit	1.6A
Max. PD(theoretically)	0.63W
Rja	75 °C/W
Enable condition	"+3V_MM" ON

DP IN

External DP IN

CPU eDP IN

CL=12pF ,20PPM

MONITOR MODE SW TO EC

For debug

NVRAM

I2C address=0xA0 for Scalar

EEPROM

NO F/W

LCD Panel Converter

For cable detection

FROM PCH
SMBUS_ISP H: Simutaneous Mode
SMBUS_ISP L: Isolate Mode

Close to Pin 10

Close to Pin 20

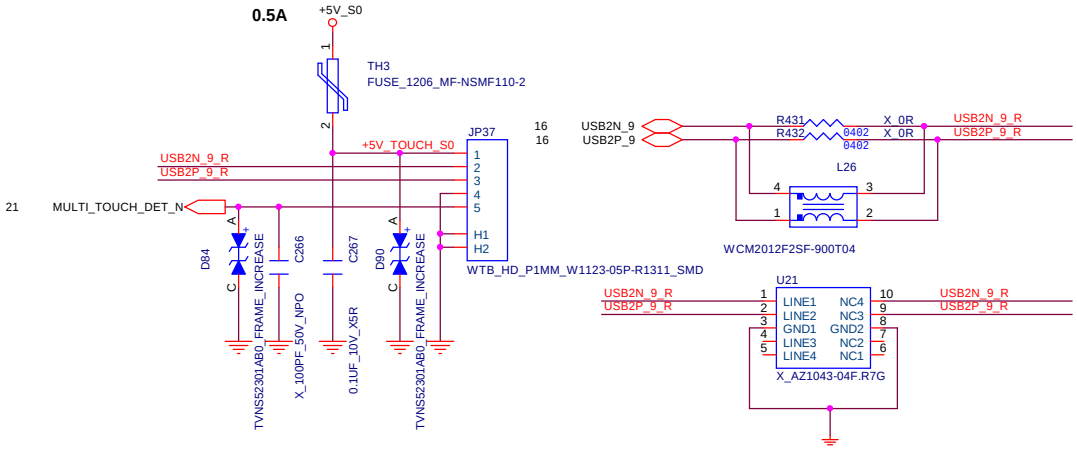
PREVENT DRIVING HPD IN POWER OFF

Universal Scientific Industrial Co., Ltd.

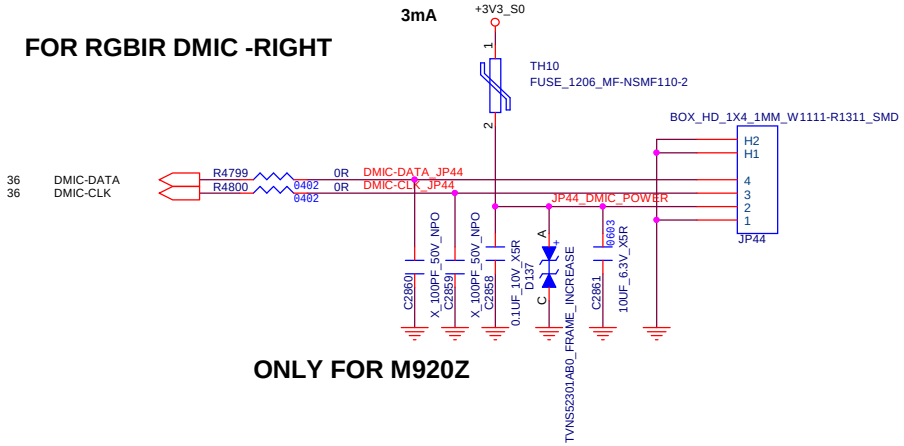
TITLE:	M920z/M828z LCD SCALAR RTD2526-CG
REV:	V1.0
Document Number :	<Doc>
Prepared by :	KERRY HUANG
SIZE : A2	Date: Tuesday, March 06, 2018
PAGE:	28 of 99

Multi-Touch

ONLY FOR M920Z

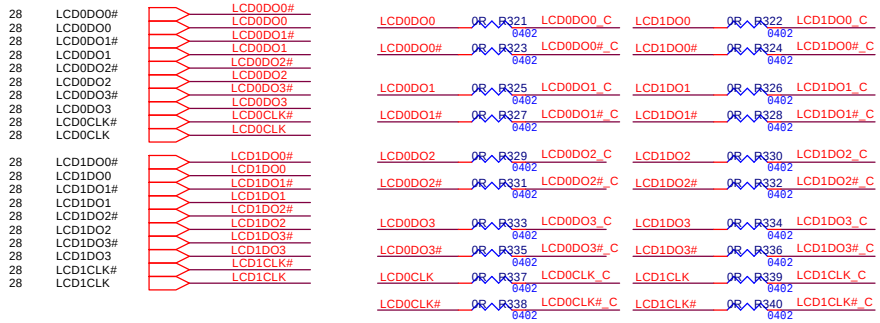


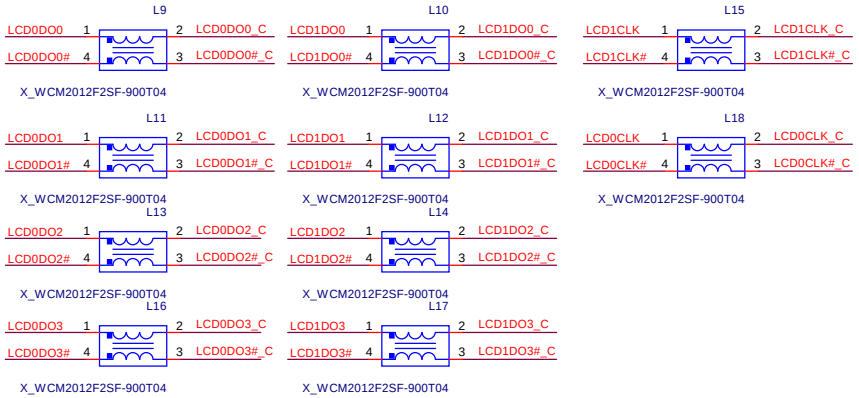
FOR RGBIR DMIC -RIGHT

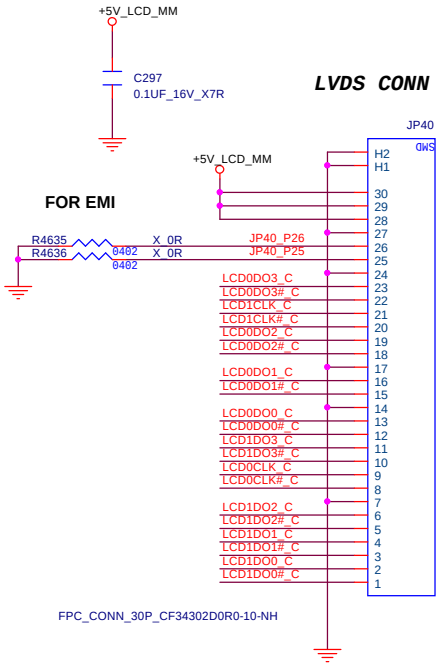


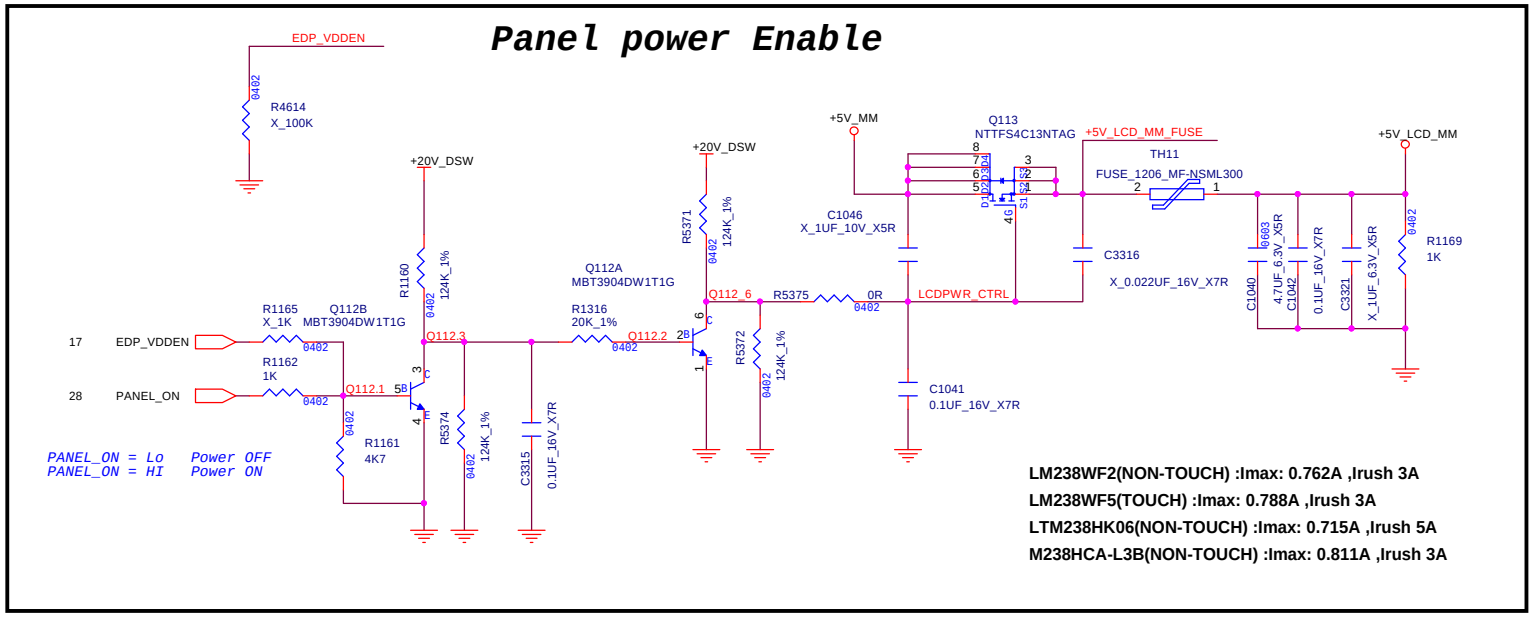
ONLY FOR M920Z

Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z DMIC_TOUCH HD			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 29 of 99	



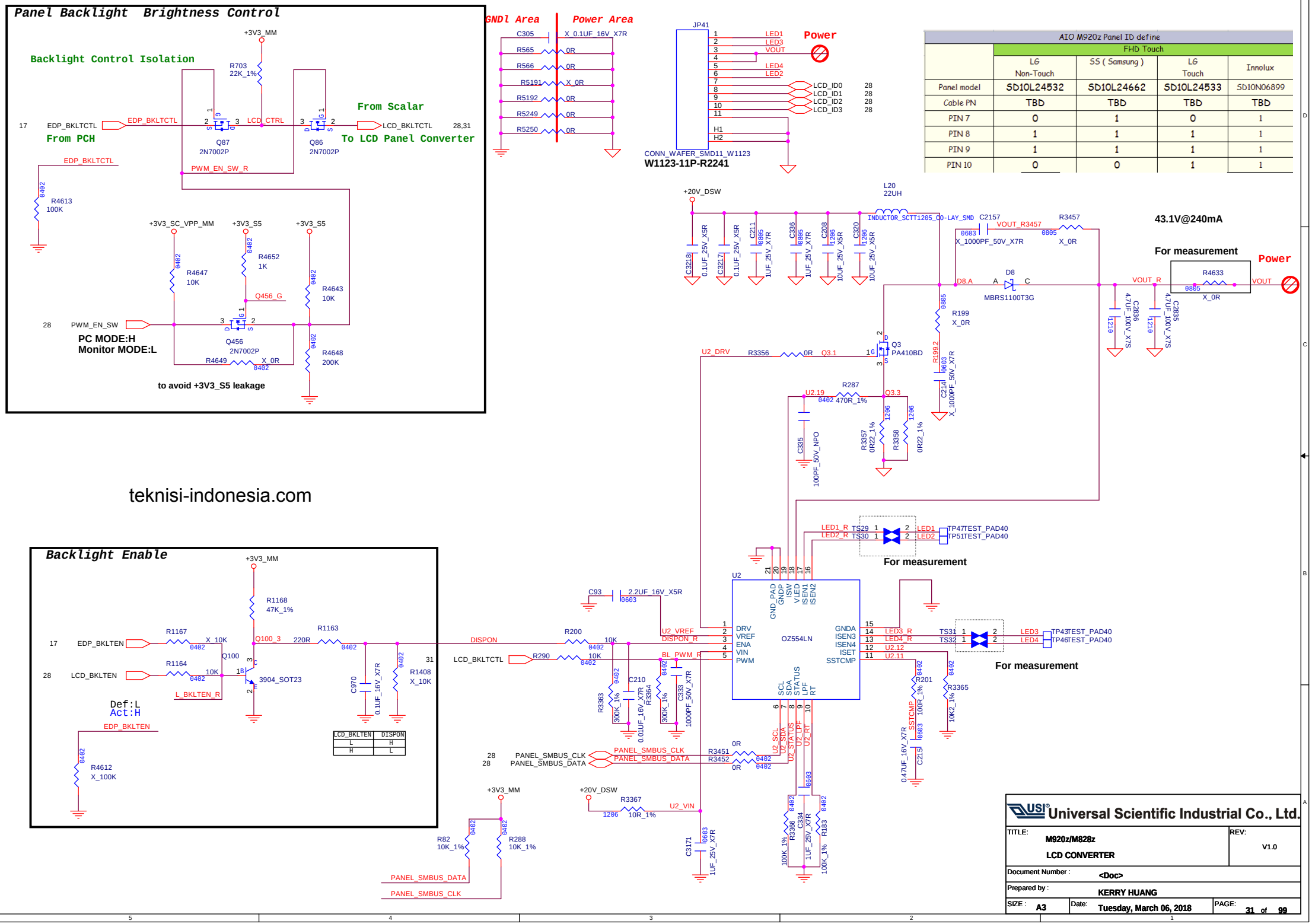






Universal Scientific Industrial Co., Ltd.

TITLE: M920z/M828z LVDS CONN		REV: V1.0	
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 30 of 99	


Panel Backlight Brightness Control
Backlight Control Isolation
+3V3_MM
R703
22K_1%
17
EDP_BKLTCTL
From PCH
EDP_BKLTCTL
LCD_CTRL
Q87
2N7002P
Q86
2N7002P
From Scalar
LCD_BKLTCTL
28,31
To LCD Panel Converter
PWM_EN_SW_R
R4613
100K
+3V3_SC_VPP_MM
+3V3_S5
+3V3_S5
R4647
10K
R4652
1K
Q456_G
R4643
10K
28
PWM_EN_SW
PC MODE:H
Monitor MODE:L
Q456
2N7002P
R4649
X_0R
R4648
200K
to avoid +3V3_S5 leakage
GNDl Area
Power Area
C305
X_0.1UF_16V_X7R
R565
R566
R5191
R5192
R5249
R5250
0R
X_0R
JP41
LED1
LED3
VOUT
LED4
LED2
LCD_ID0
LCD_ID1
LCD_ID2
LCD_ID3
H1
H2
Power
CONN_WAFER_SMD11_W1123
W1123-11P-R2241
AIO M920z Panel ID define
FHD Touch
LG Non-Touch
SS (Samsung)
LG Touch
Innolux
Panel model
SD10L24532
SD10L24662
SD10L24533
SD10N06899
Cable PN
TBD
PIN 7
PIN 8
PIN 9
PIN 10
+20V_DSW
L20
22UH
INDUCTOR_SCTT1205_CO-LAY_SMD
C2157
X_1000PF_50V_X7R
VOUT_R3457
R3457
X_0R
43.1V@240mA
For measurement
Power
D8
MBRS1100T3G
R4633
X_0R
VOUT
R199
X_0R
Q3
PA410BD
U2_DRV
R3356
Q3.1
R287
470R_1%
Q3.3
C335
100PF_50V_NPO
R3357
R3358
0R22_1%
C2836
C2835
4.7UF_100V_X7S
LED1_R
LED2_R
TS29
TS30
TP47TEST_PAD40
TP51TEST_PAD40
For measurement
U2
OZ554LN
DRV
VREF
ENA
VIN
PWM
GNDA
ISEN3
ISEN4
ISET
SSTCMP
SCL
SDA
STATUS
LPF
RT
LED3_R
LED4_R
TS31
TS32
TP43TEST_PAD40
TP46TEST_PAD40
LED3
LED4
For measurement
C93
2.2UF_16V_X5R
U2_VREF
DISPON_R
BL_PWM_R
R200
10K
R290
R201
R3365
10K2_1%
100R_1%
C215
0.47UF_16V_X7R
R3363
300K_1%
C210
0.01UF_16V_X7R
R3364
C333
1000PF_50V_X7R
PANEL_SMBUS_CLK
PANEL_SMBUS_DATA
R3451
R3452
0R
U2_SCL
U2_SDA
U2_STATUS
U2_LPF
U2_RT
U2_VIN
R3367
10R_1%
C3171
1UF_25V_X7R
R3366
C334
R183
100K_1%
Backlight Enable
+3V3_MM
R1168
47K_1%
17
EDP_BKLTEN
R1167
X_10K
Q100_3
220R
R1163
28
LCD_BKLTEN
R1164
10K
Q100
3904_SOT23
L_BKLTEN_R
Def:L
Act:H
EDP_BKLTEN
R4612
X_100K
C970
0.1UF_16V_X7R
R1408
X_10K
31
LCD_BKLTCTL
DISPON
LCD_BKLTEN
DISPON
L
H
H
L
R82
10K_1%
R288
10K_1%
PANEL_SMBUS_DATA
PANEL_SMBUS_CLK
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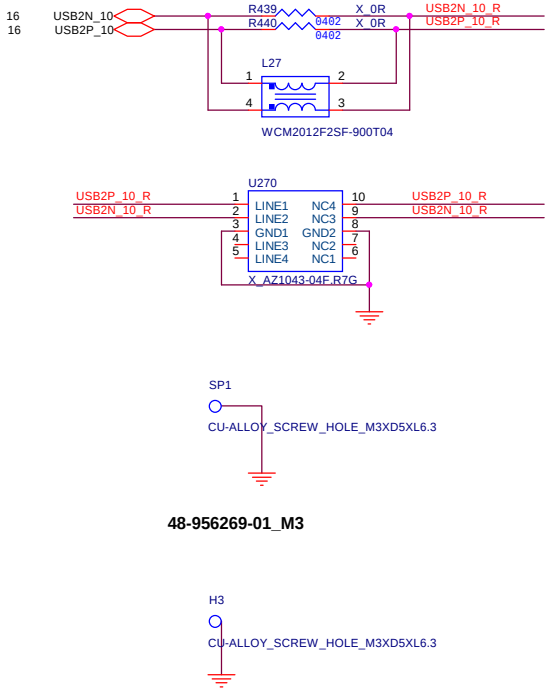
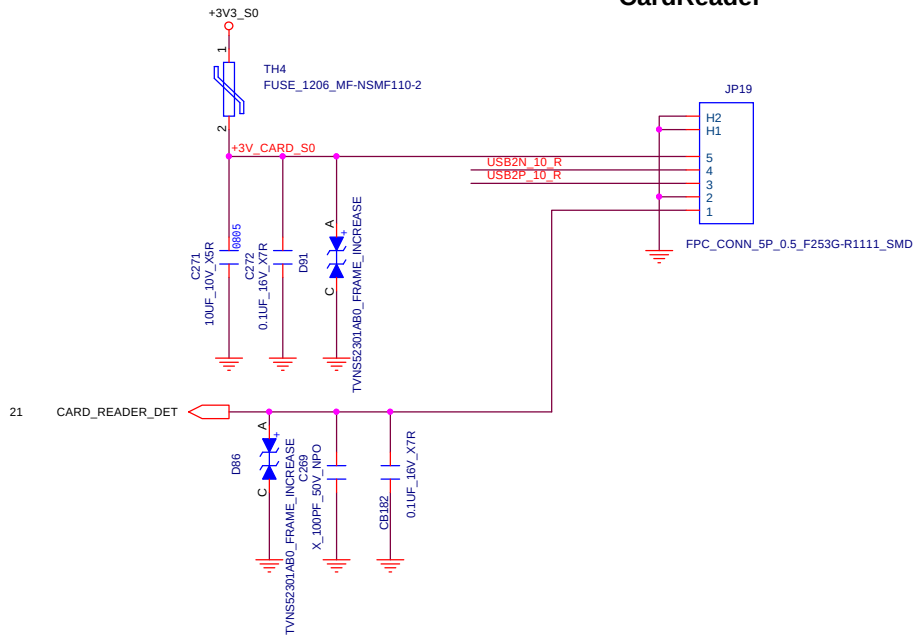
Universal Scientific Industrial Co., Ltd.
TITLE:
M920z/M828z
LCD CONVERTER
REV:
V1.0
Document Number :
<Doc>
Prepared by :
KERRY HUANG
SIZE :
A3
Date:
Tuesday, March 06, 2018
PAGE:
31 of 99

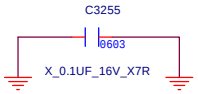
CardReader



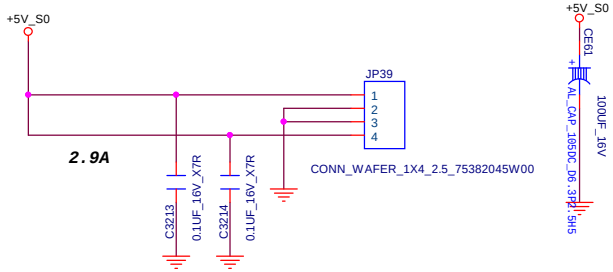


Universal Scientific Industrial Co., Ltd.		
TITLE: M920z/M828z CARD READER HD		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 32 of 99

SATA CONN
SATA 3.0

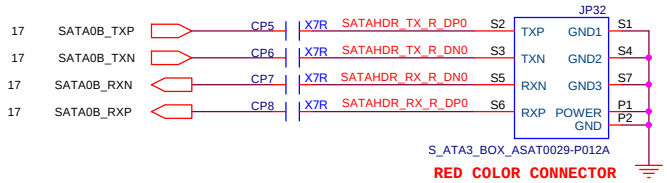


Power Connector



SATA1 Gen3

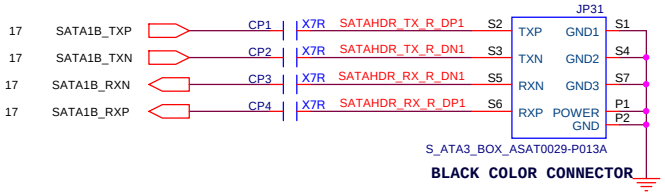
HDD



RED COLOR CONNECTOR

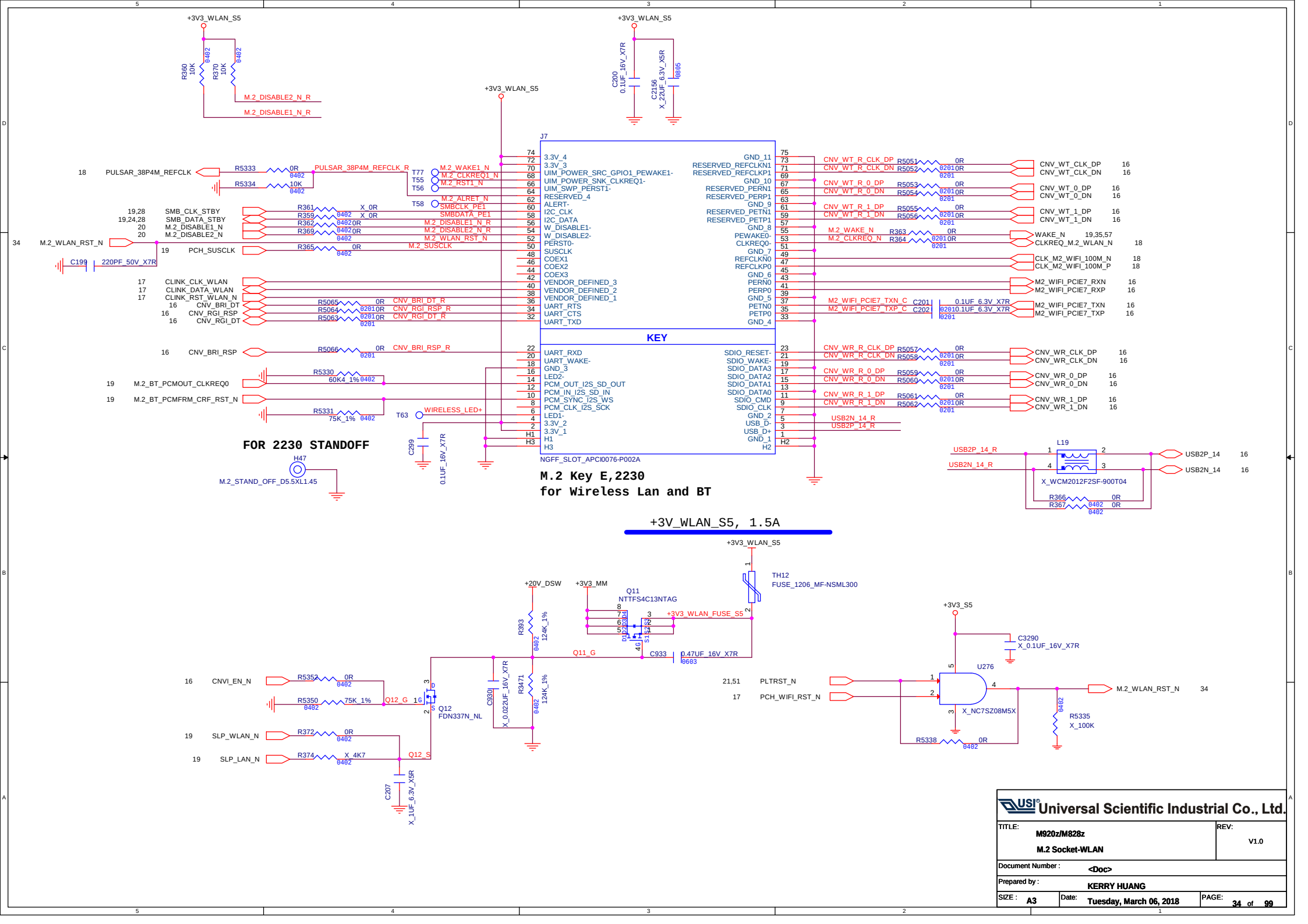
SATA2 Gen3

ODD



BLACK COLOR CONNECTOR

Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z SATA 3.0 CONN			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 33 of 99	


+3V3_WLAN_S5
R360 10K 0402
R370 10K 0402
M.2_DISABLE2_N_R
M.2_DISABLE1_N_R
C200 0.1UF_16V_X7R
C2156 X_22UF_6.3V_X5R 0805
J7
3.3V_4
3.3V_3
UIM_POWER_SRC_GPIO1_PEWAKE1-
UIM_POWER_SNK_CLKREQ1-
UIM_SWP_PERST1-
RESERVED_4
ALERT-
I2C_CLK
I2C_DATA
W_DISABLE1-
W_DISABLE2-
PERST0-
SUSCLK
COEX1
COEX2
COEX3
VENDOR_DEFINED_3
VENDOR_DEFINED_2
VENDOR_DEFINED_1
UART_RTS
UART_CTS
UART_TXD
UART_RXD
UART_WAKE-
GND_3
LED2-
PCM_OUT_I2S_SD_OUT
PCM_IN_I2S_SD_IN
PCM_SYNC_I2S_WS
PCM_CLK_I2S_SCK
LED1-
3.3V_2
3.3V_1
H1
H3
GND_11
RESERVED_REFCLKN1
RESERVED_REFCLKP1
GND_10
RESERVED_PERN1
RESERVED_PERP1
GND_9
RESERVED_PETN1
RESERVED_PETP1
GND_8
PEWAKE0-
CLKREQ0-
GND_7
REFCLKN0
REFCLKP0
GND_6
PERN0
PERP0
GND_5
PETN0
PETP0
GND_4
SDIO_RESET-
SDIO_WAKE-
SDIO_DATA3
SDIO_DATA2
SDIO_DATA1
SDIO_DATA0
SDIO_CMD
SDIO_CLK
GND_2
USB_D-
USB_D+
GND_1
H2
KEY
NGFF_SLOT_APCI0076-P002A
M.2 Key E,2230
for Wireless Lan and BT
PULSAR_38P4M_REFCLK
R5333 0R 0402
R5334 10K 0402
PULSAR_38P4M_REFCLK_R
M.2_WAKE1_N
M.2_CLKREQ1_N
M.2_RST1_N
M.2_ALERT_N
SMBCLK_PE1
SMBDATA_PE1
M.2_DISABLE1_N_R
M.2_DISABLE2_N_R
M.2_WLAN_RST_N
M.2_SUSCLK
SMB_CLK_STBY
SMB_DATA_STBY
M.2_DISABLE1_N
M.2_DISABLE2_N
PCH_SUSCLK
M.2_WLAN_RST_N
C199 220PF_50V_X7R
CLINK_CLK_WLAN
CLINK_DATA_WLAN
CLINK_RST_WLAN_N
CNV_BRI_DT
CNV_RGI_RSP
CNV_RGI_DT
CNV_BRI_DT_R
CNV_RGI_RSP_R
CNV_RGI_DT_R
CNV_BRI_RSP
CNV_BRI_RSP_R
R5330 60K4_1% 0402
R5331 75K_1% 0402
M.2_BT_PCMOUT_CLKREQ0
M.2_BT_PCMFRM_CRF_RST_N
WIRELESS_LED+
C299 0.1UF_16V_X7R
FOR 2230 STANDOFF
H47
M.2_STAND_OFF_D5.5XL1.45
CNV_WT_R_CLK_DP
CNV_WT_R_CLK_DN
CNV_WT_R_0_DP
CNV_WT_R_0_DN
CNV_WT_R_1_DP
CNV_WT_R_1_DN
M.2_WAKE_N
M.2_CLKREQ_N
M2_WIFI_PCIE7_TXN_C
M2_WIFI_PCIE7_TXP_C
C201 0.1UF_6.3V_X7R
C202 0.1UF_6.3V_X7R
CNV_WT_CLK_DP
CNV_WT_CLK_DN
CNV_WT_0_DP
CNV_WT_0_DN
CNV_WT_1_DP
CNV_WT_1_DN
WAKE_N
CLKREQ_M.2_WLAN_N
CLK_M2_WIFI_100M_N
CLK_M2_WIFI_100M_P
M2_WIFI_PCIE7_RXN
M2_WIFI_PCIE7_RXP
M2_WIFI_PCIE7_TXN
M2_WIFI_PCIE7_TXP
CNV_WR_R_CLK_DP
CNV_WR_R_CLK_DN
CNV_WR_R_0_DP
CNV_WR_R_0_DN
CNV_WR_R_1_DP
CNV_WR_R_1_DN
CNV_WR_CLK_DP
CNV_WR_CLK_DN
CNV_WR_0_DP
CNV_WR_0_DN
CNV_WR_1_DP
CNV_WR_1_DN
USB2N_14_R
USB2P_14_R
L19
X_WCM2012F2SF-900T04
R366 0R 0402
R367 0R 0402
USB2P_14
USB2N_14
+3V_WLAN_S5, 1.5A
TH12
FUSE_1206_MF-NSML300
+3V_WLAN_FUSE_S5
+20V_DSW
+3V_MM
Q11
NTTFS4C13NTAG
R393 124K_1% 0402
Q11_G
C933 0.47UF_16V_X7R 0603
CNVI_EN_N
R5352 0R 0402
R5350 75K_1% 0402
Q12_G
Q12
FDN337N_NL
C930 X_0.022UF_16V_X7R
R3471 124K_1% 0402
SLP_WLAN_N
SLP_LAN_N
R372 0R 0402
R374 X_4K7 0402
Q12_S
C207 X_1UF_6.3V_X5R
PLTRST_N
PCH_WIFI_RST_N
+3V3_S5
C3290 X_0.1UF_16V_X7R
U276
X_NC7SZ08M5X
R5335 X_100K 0402
R5338 0R 0402
Universal Scientific Industrial Co., Ltd.
TITLE: M920z/M828z
M.2 Socket-WLAN
REV: V1.0
Document Number : <Doc>
Prepared by : KERRY HUANG
SIZE : A3
Date: Tuesday, March 06, 2018
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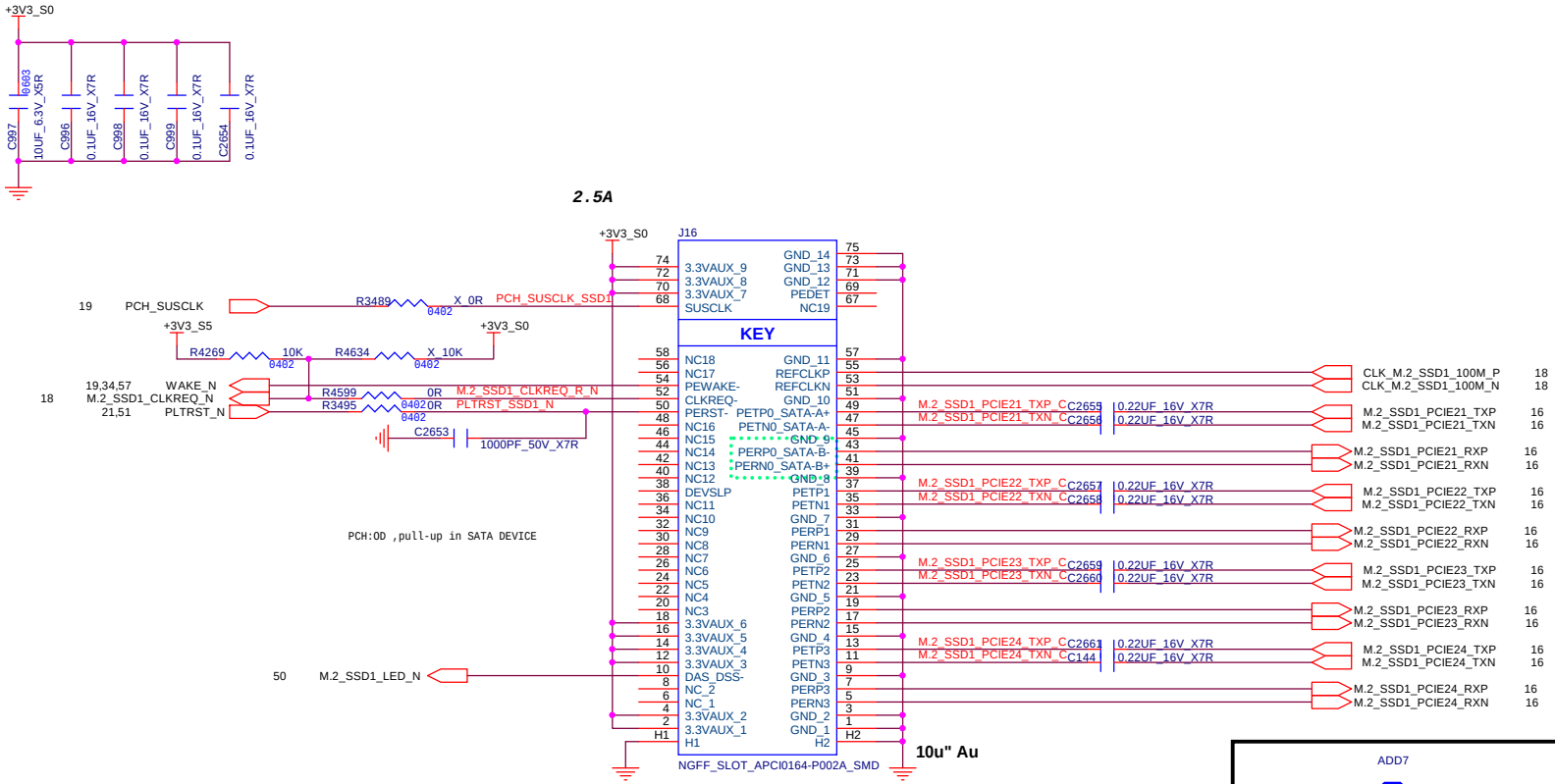
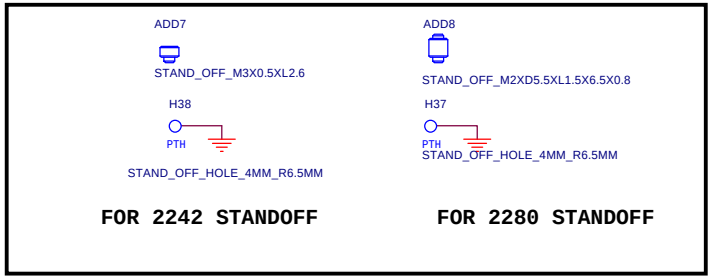
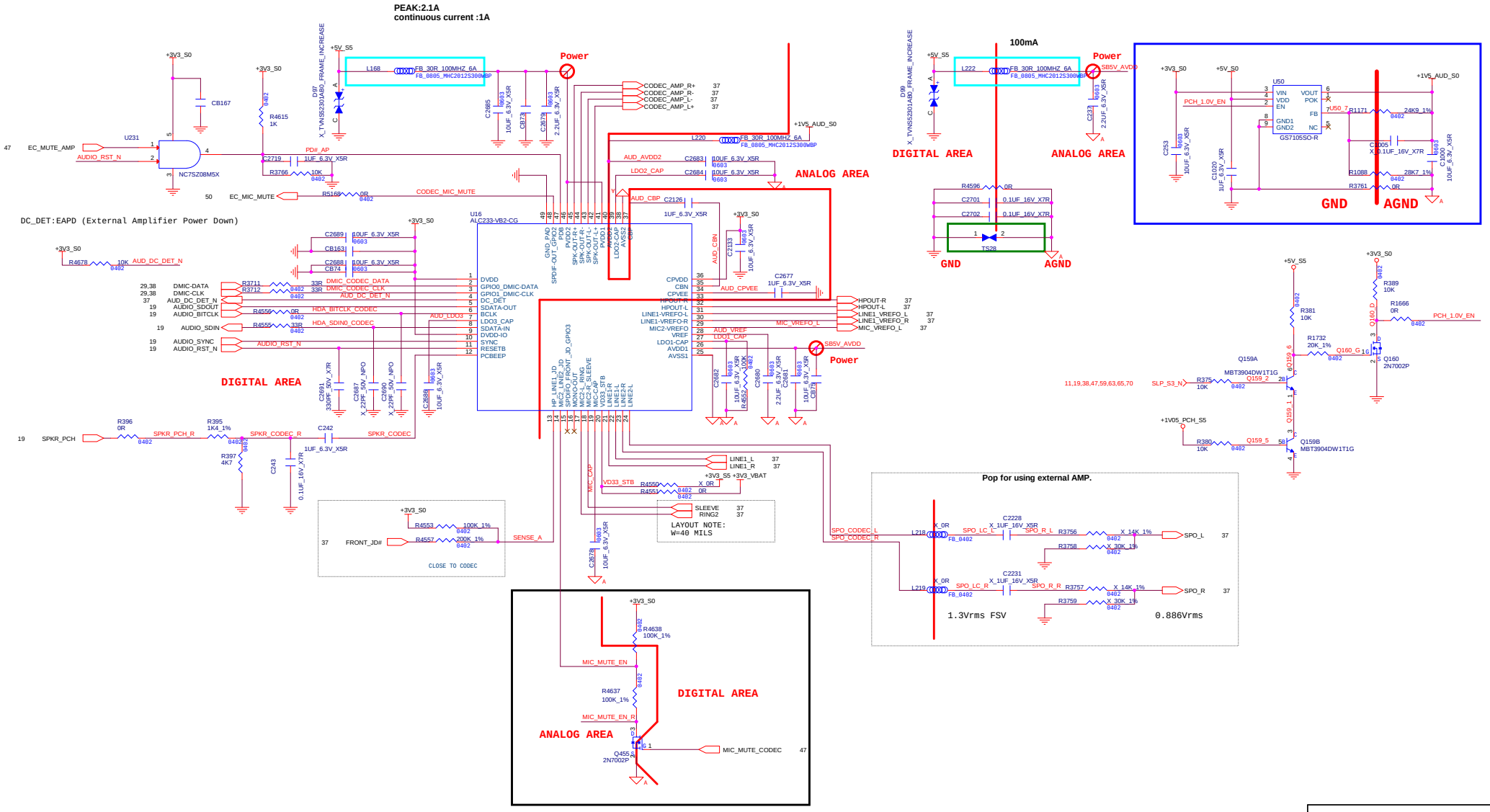


NGFF KEY M SLOT1 BLACK
TYPE 2280 H=8.5mm

NOTE: set 4 X1 from FITC for M.2 RX testing

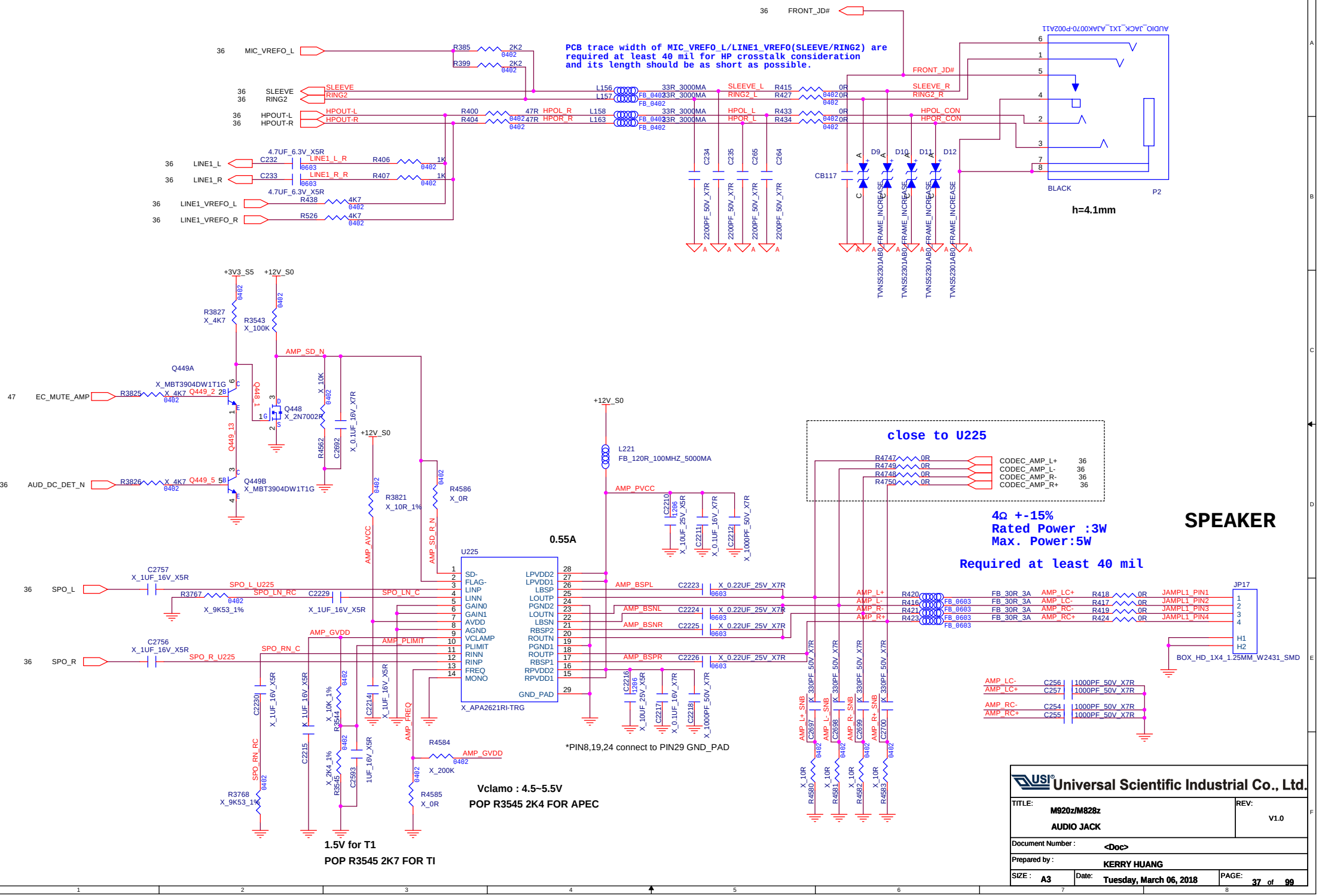


Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z M.2 SOCKET-SSD			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Thursday, March 22, 2018		PAGE: 35 of 99



Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z AUDIO CODEC ALC233	REV: V1.0
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : Custom	Date: Tuesday, March 06, 2018
PAGE: 36 of 99	

Combo Audio Jacks



Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z AUDIO JACK	REV: V1.0
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Tuesday, March 06, 2018
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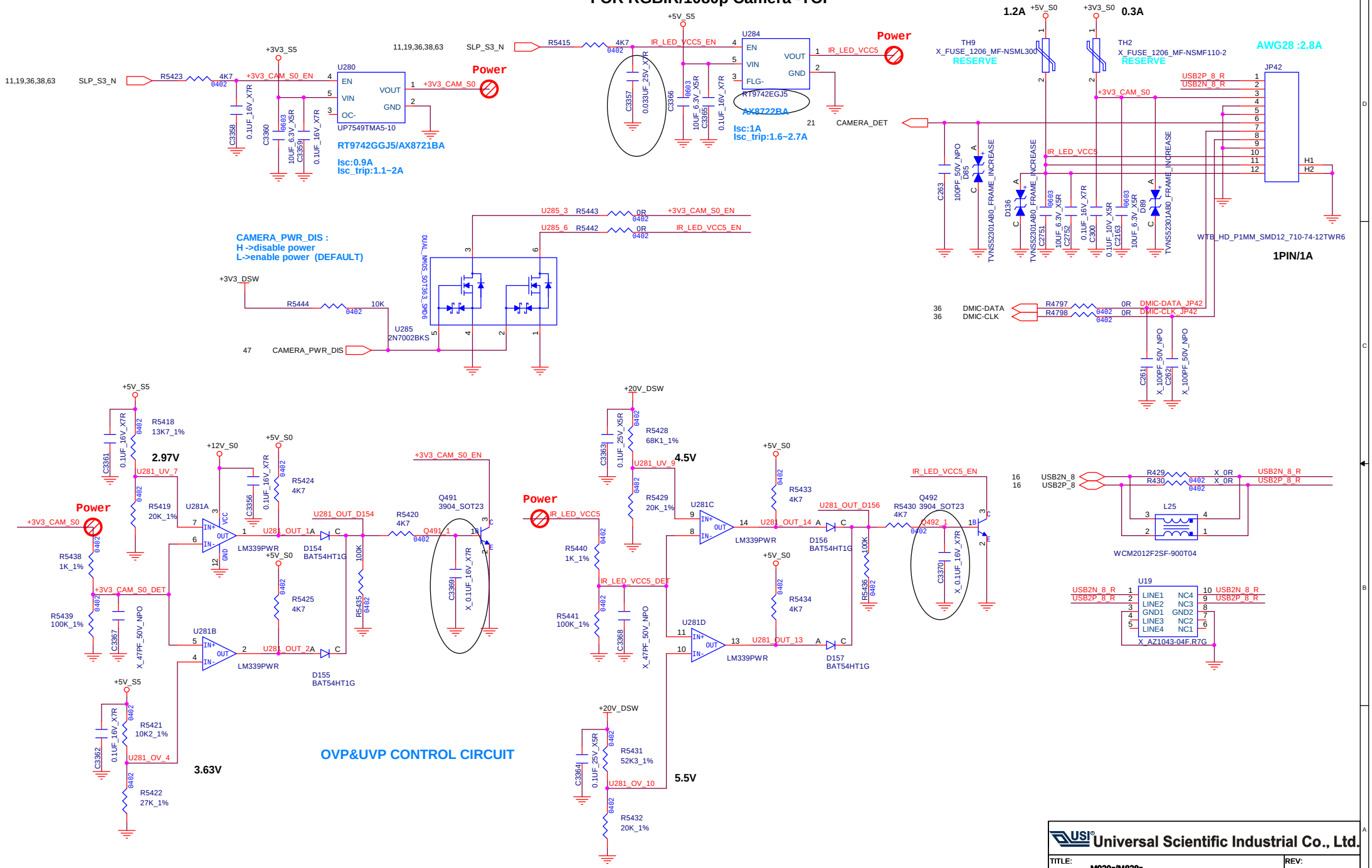
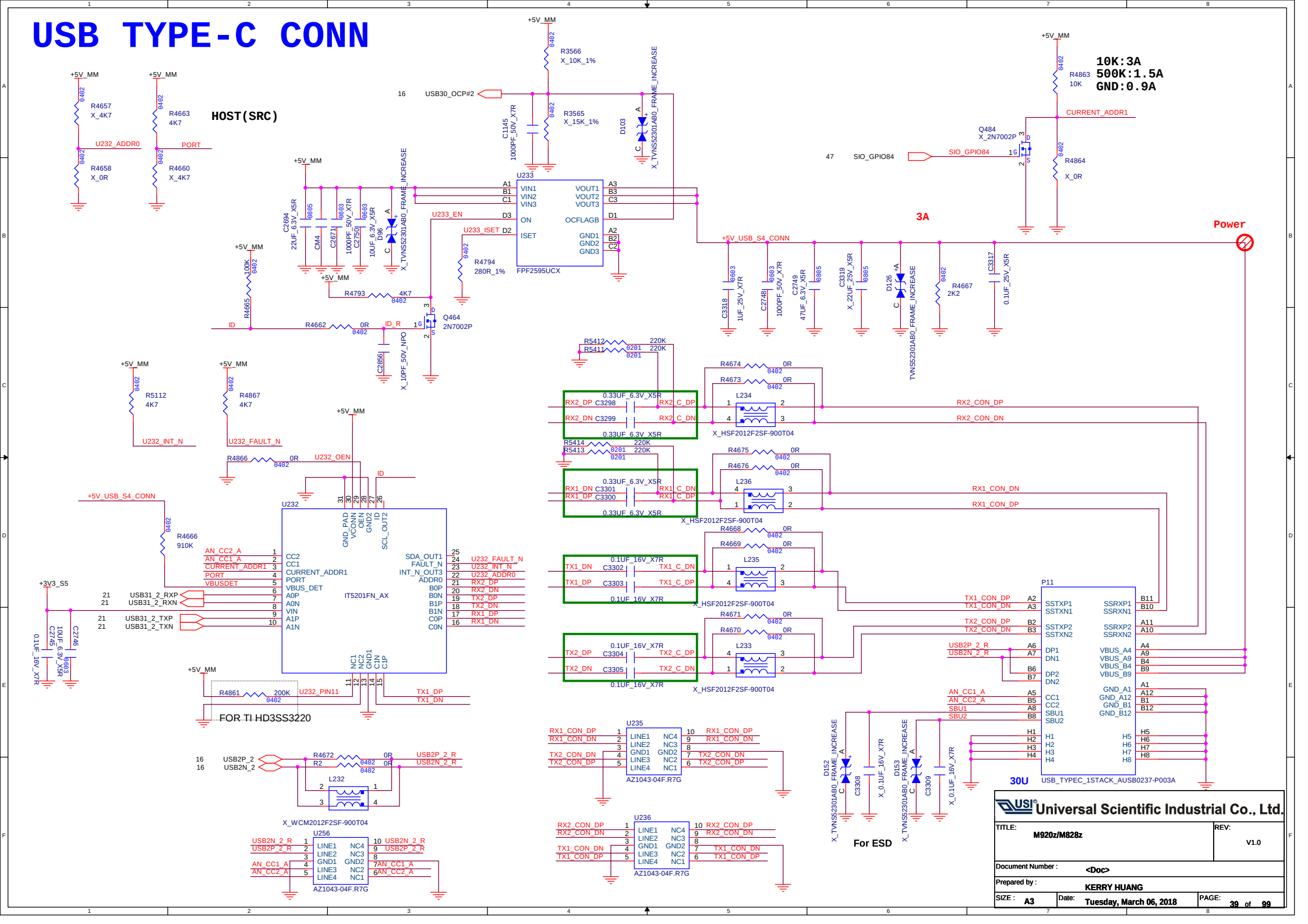
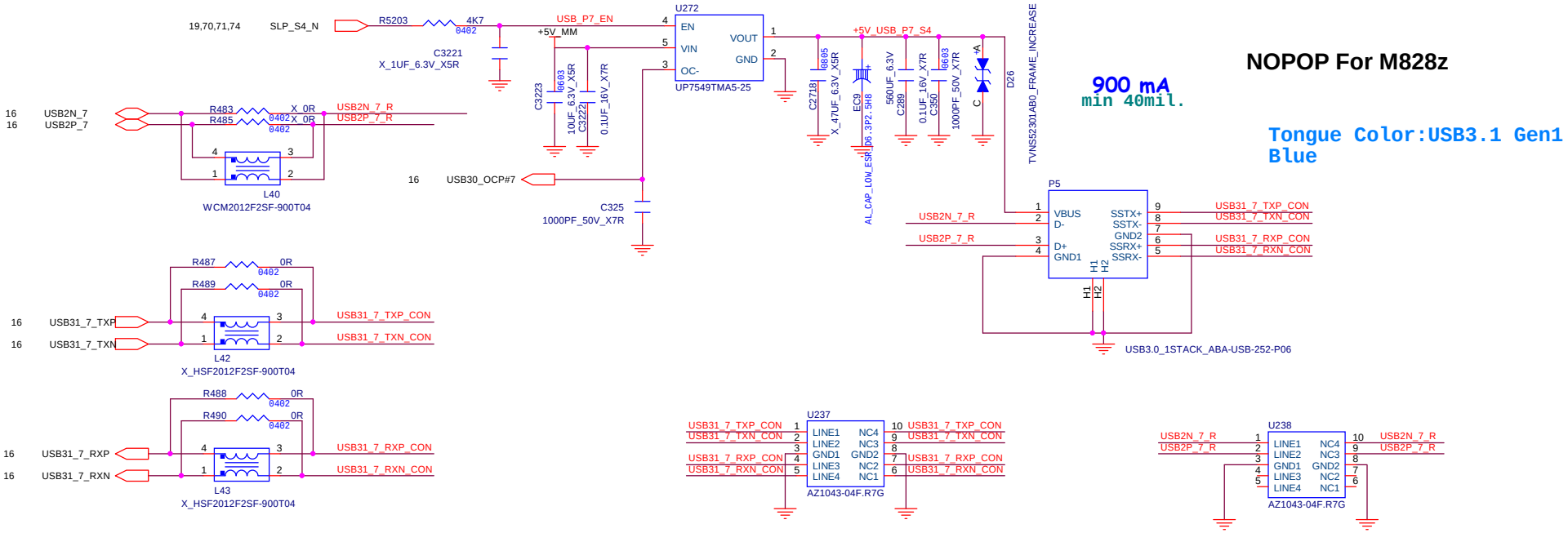
FOR RGBIR/1080p Camera -TOP

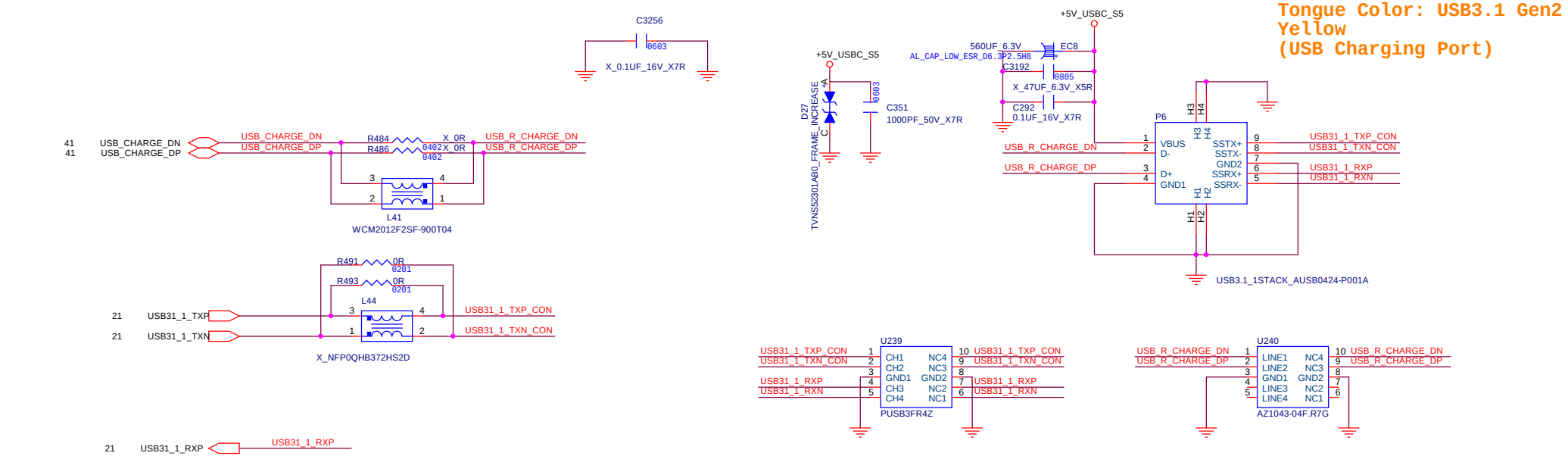


Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z RGBIR_DMIC_TOUCH_HD			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, April 10, 2018		PAGE: 38 of 99

USB TYPE-C CONN



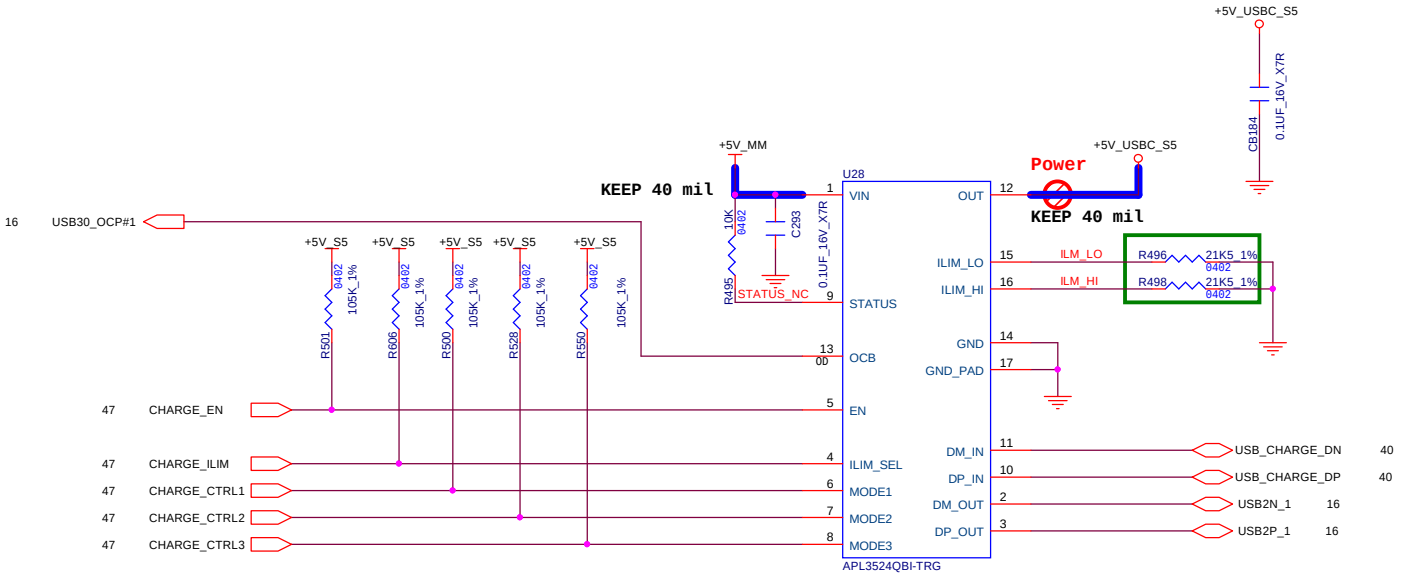




Universal Scientific Industrial Co., Ltd.

TITLE: M920z/M828z SIDE USB3.1 PORTX2		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 40 of 99

USB CHARGING PORT CONTROLLER & POWER SWITCH WITH LOAD DETECTION

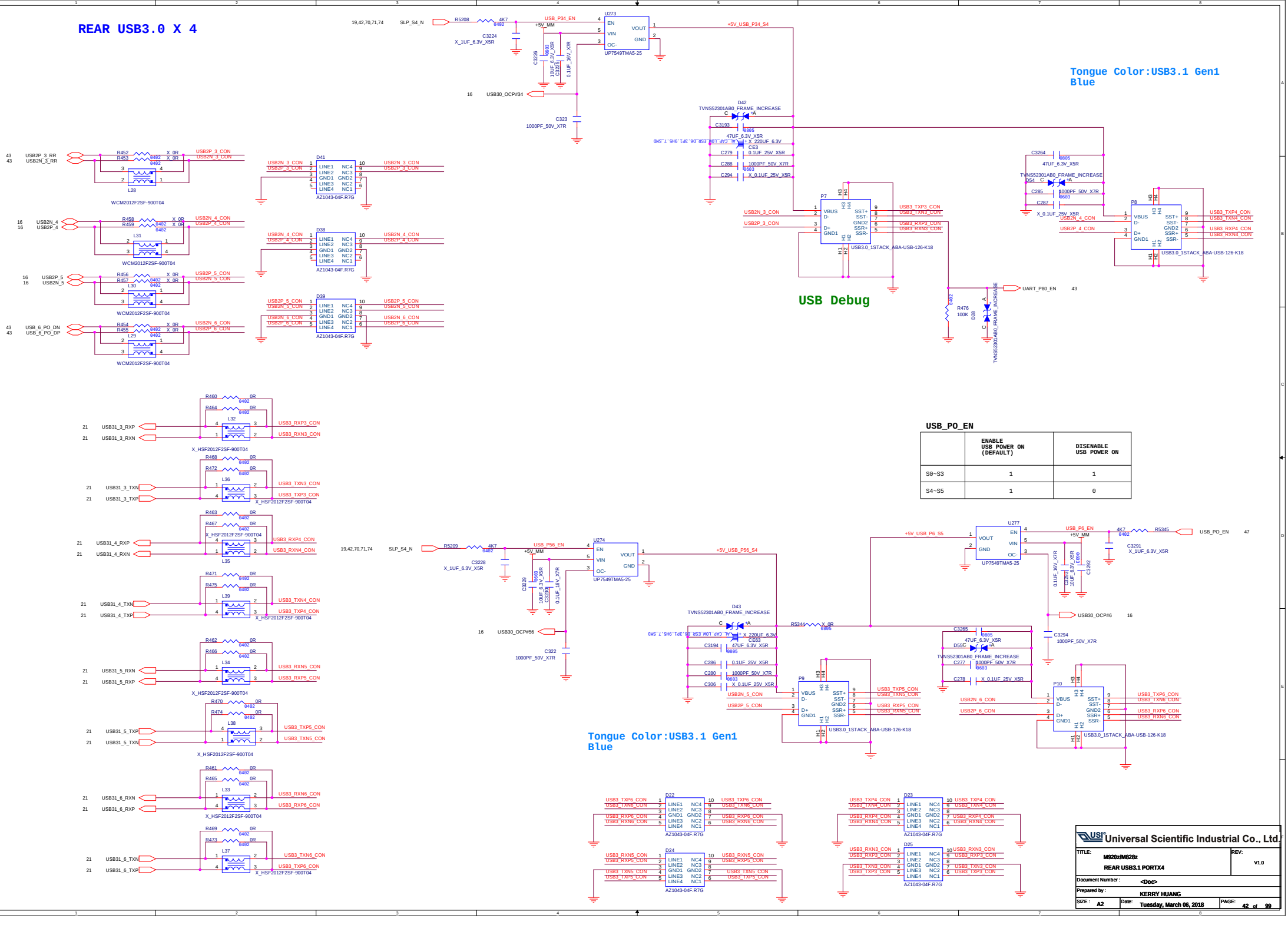


TI/SN1702001RTER

Control Signal			Model Select				
			CNTL1	CNTL2	CNTL3	ILIM_SEL	EN
Charge EN	S0	CDP	1	1	1	1 -ILIM_HI	1
	S3	DCP	0	1	1	0 -ILIM_HI	1
	S4/S5	DCP	0	0	1	1 -ILIM_HI	1
Charge DIS	S0	SDP	0	1	0	0 -ILIM_LO	1
	S3	SDP	0	1	0	0 -ILIM_LO	1
	S4/S5	SDP	Shunt Down				0
Logic			AND (EN_GPIO,SLP_S3#)	AND (OR(EN_GPIO#,MODE),SLP_S4#)	EN_GPIO	AND (SLP_S3#, SLP_S4)	OR (EN_GPIO,SLP_S4#)

Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z USB CHARGING			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, April 10, 2018		PAGE: 41 of 99

REAR USB3.0 X 4

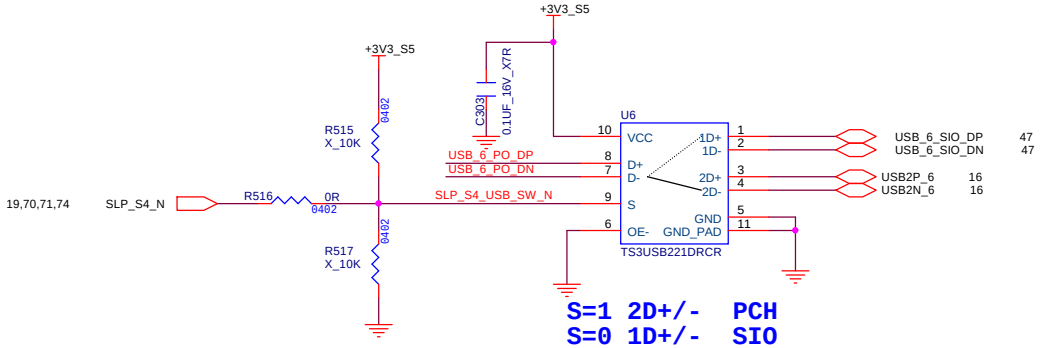


USB_PO_EN

	ENABLE USB POWER ON (DEFAULT)	DISENABLE USB POWER ON
S0~S3	1	1
S4~S5	1	0

Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z REAR USB3.1 PORTX4	REV: V1.0
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A2	Date: Tuesday, March 06, 2018 PAGE: 42 of 99

USB POWER ON
(Key ALT+P to power on system)



S=1 2D+/- PCH
S=0 1D+/- SIO

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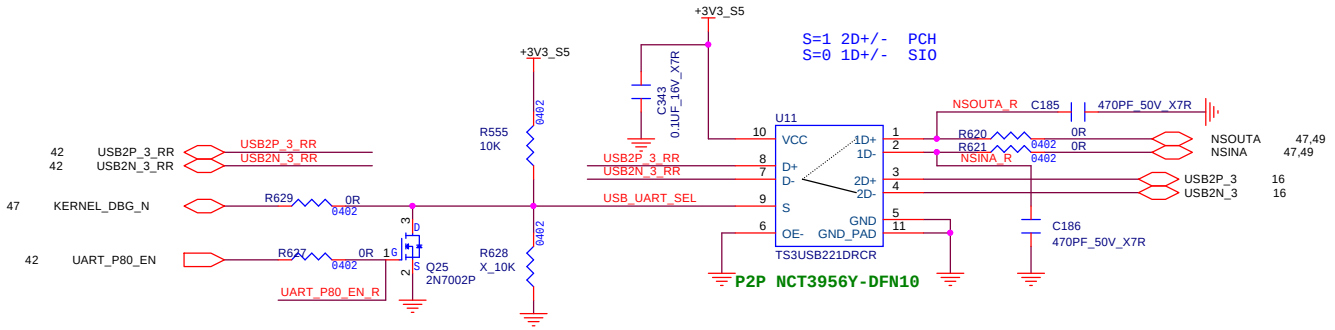
OE#	S	Funtion
H	X	Disable
L	L	D(+/-) to 1D(+/-)
L	H (Default)	D(+/-) to 2D(+/-)

POP FOR NO USB POWER ON

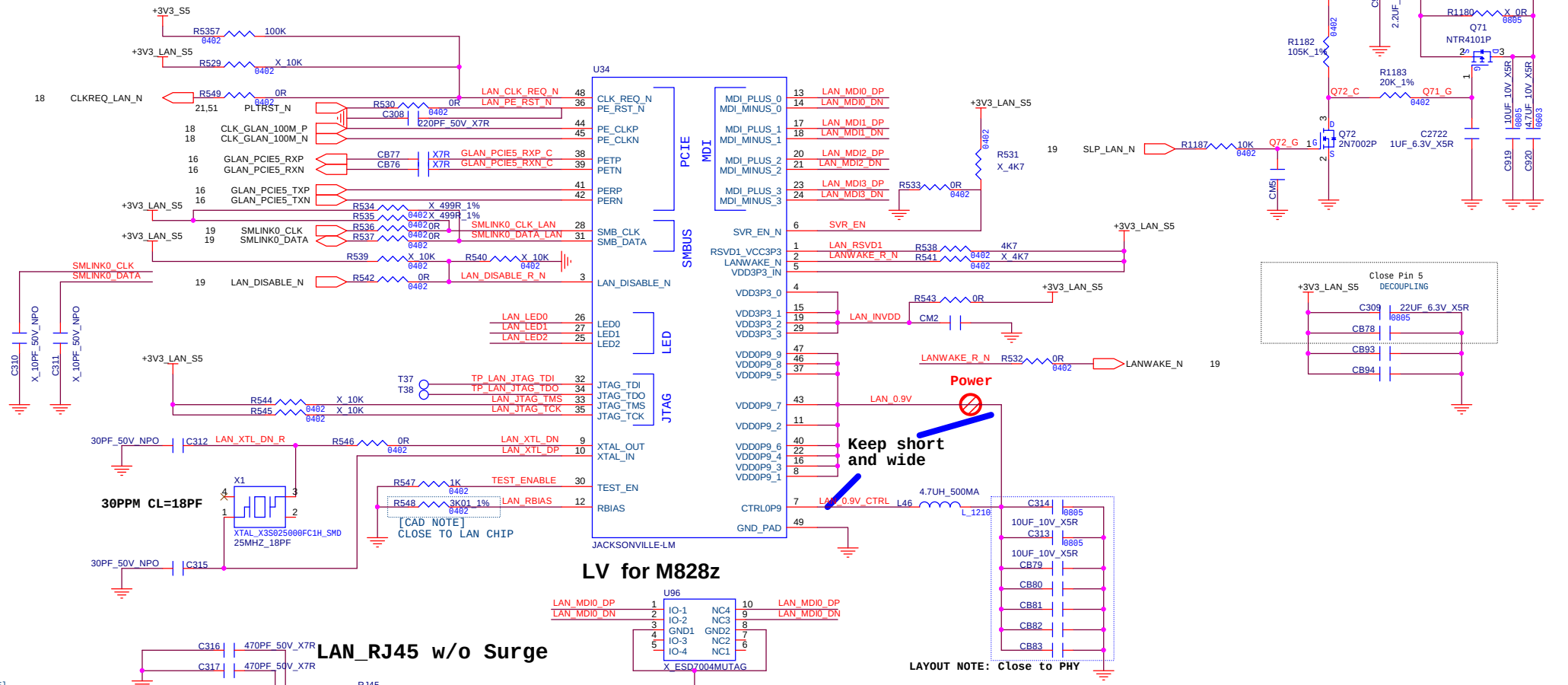
USB Debug



UARTA_P80_EN	POST 80
L	DISABLE
H	ENABLE

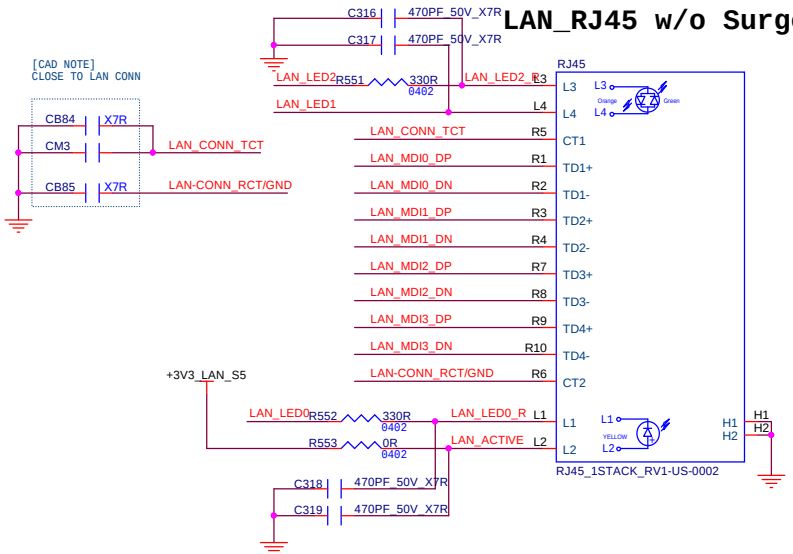
Universal Scientific Industrial Co., Ltd.		
TITLE: M920z/M828z USB Debug		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 43 of 99

ETHERNET

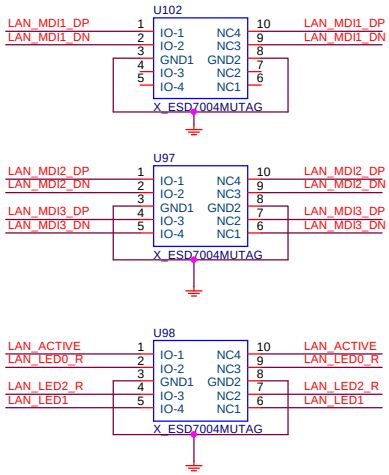


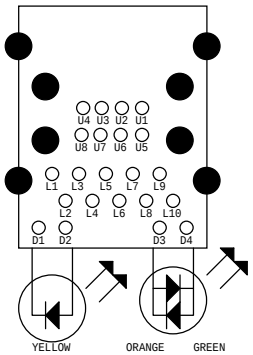
LV for M828z

LAN_RJ45 w/o Surge



ESD Reserve





WOL	Status	Yellow	Green	Orange
Don't care	No Link	●	●	●
Off	S3/S4/S5	●	●	●
On	10Mb Inactive	●	●	●
On	10Mb Active	●	B	●
On	100Mb Inactive	●	●	●
On	100Mb Active	●	B	●
On	1Gb Inactive	●	●	●
On	1Gb Active	●	B	●

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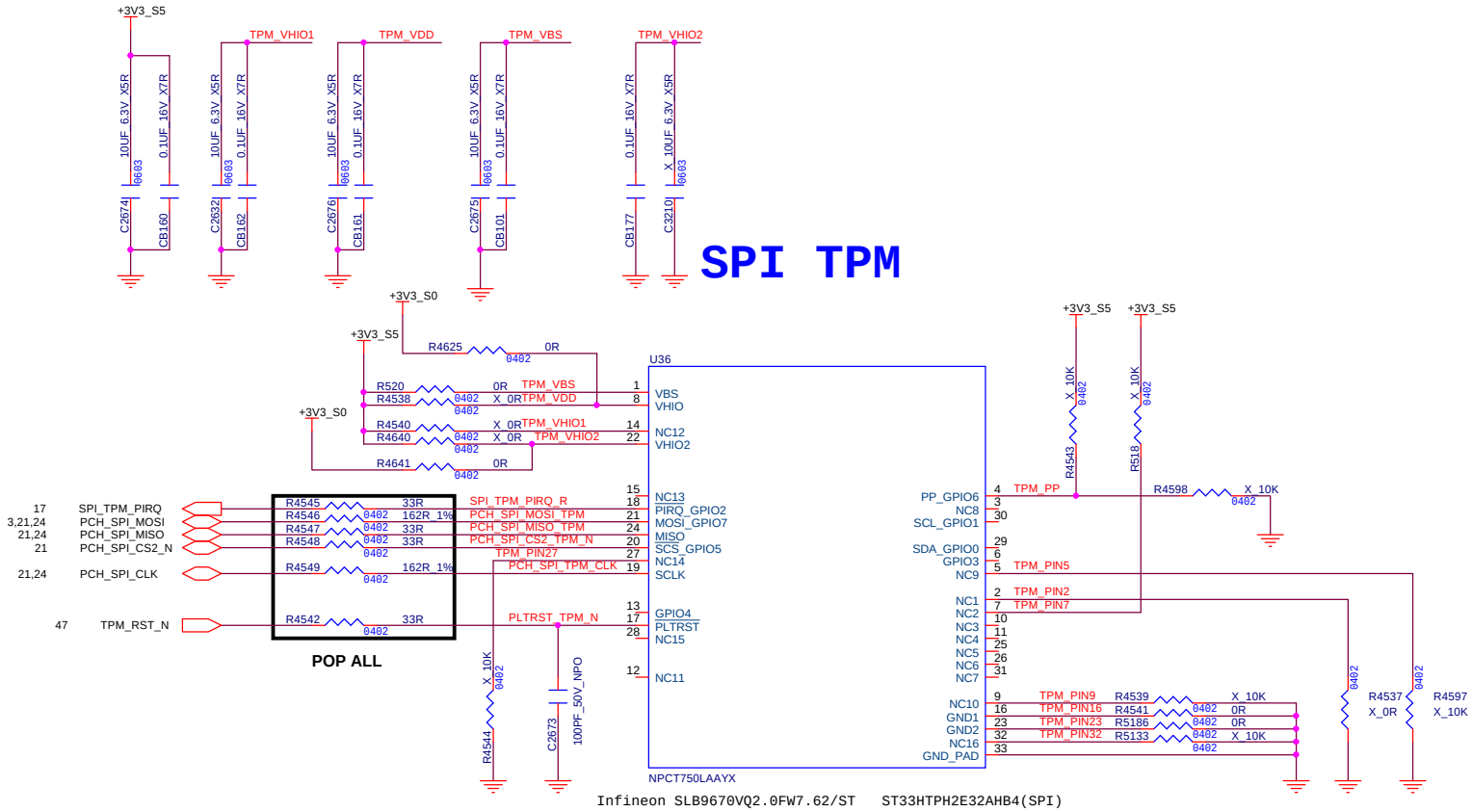
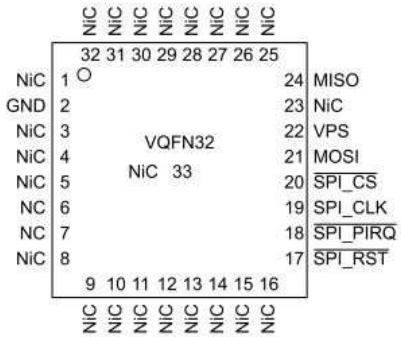
TITLE: M920z/M828z LAN JACKSONVILLE		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 44 of 99



Infineon SLB9670VQ2.0FW7.62/ST ST33HTPH2E32AHB4(SPI)

ST33HTPH2E32AAE6

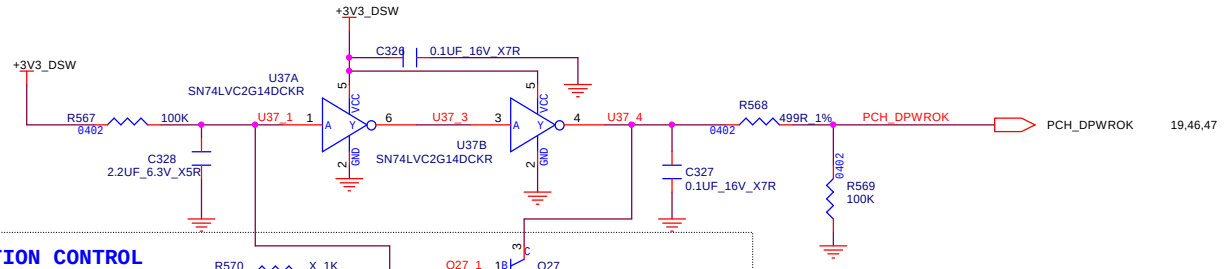


	STUFF	EMPTY
NPCT750LAAYX	R520,R4541,R4625,R4641,C2673	R518,R4543,R4537,R4597,R4598,R4539,R5133,R4640,R4540, R4538,R4544
ST33HTPH2E32AHB4	R4537,R5133,R4640,C2673,C3210	R4625,R520,R4543,R518,R4538,R4539,R4540,R4541,R4544 ,C2632,CB162,C2676,CB161,C2675,CB101,R4597,R4598,R4641,R5186,R5133
SLB9670VQ2.0FW7.62	R4538,R4640,R4545,R4546,R4547,R4548 ,R4549,R4542,R5133,R4539,R4537	R520,R4625,R4540,R4641,R4544,R4541,R518,R4597,R4543,R4598

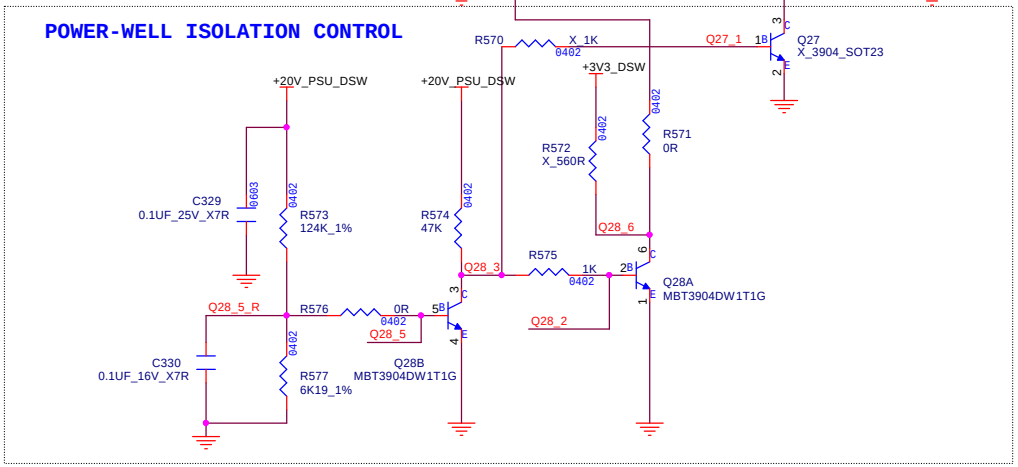
Universal Scientific Industrial Co., Ltd.

TITLE: M920z/M828z TPM		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 45 of 99

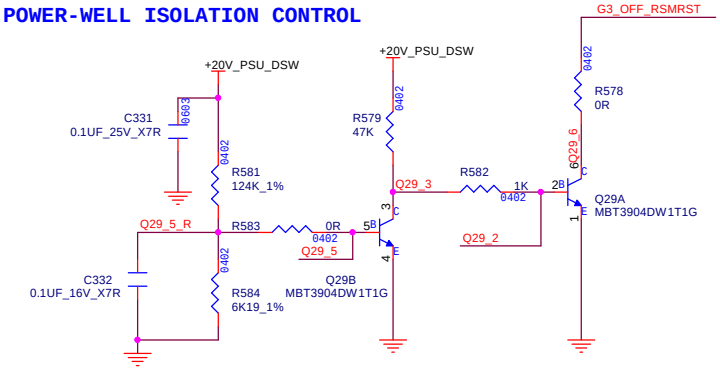
DPWROK LOGIC

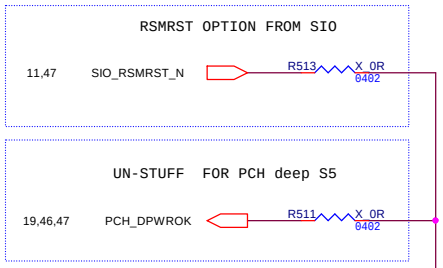


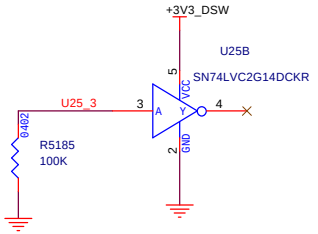
POWER-WELL ISOLATION CONTROL



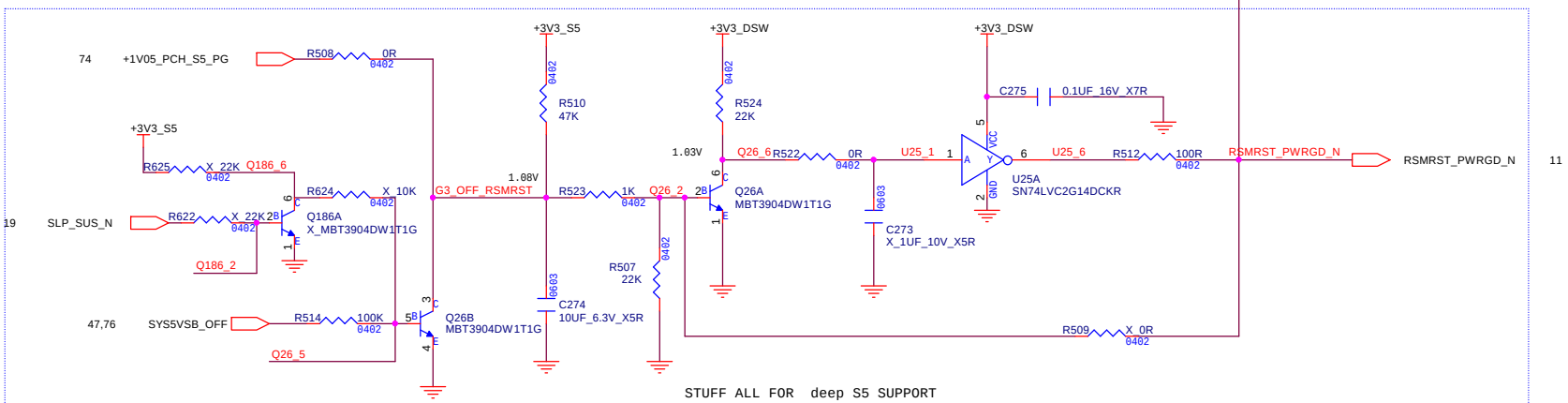
POWER-WELL ISOLATION CONTROL



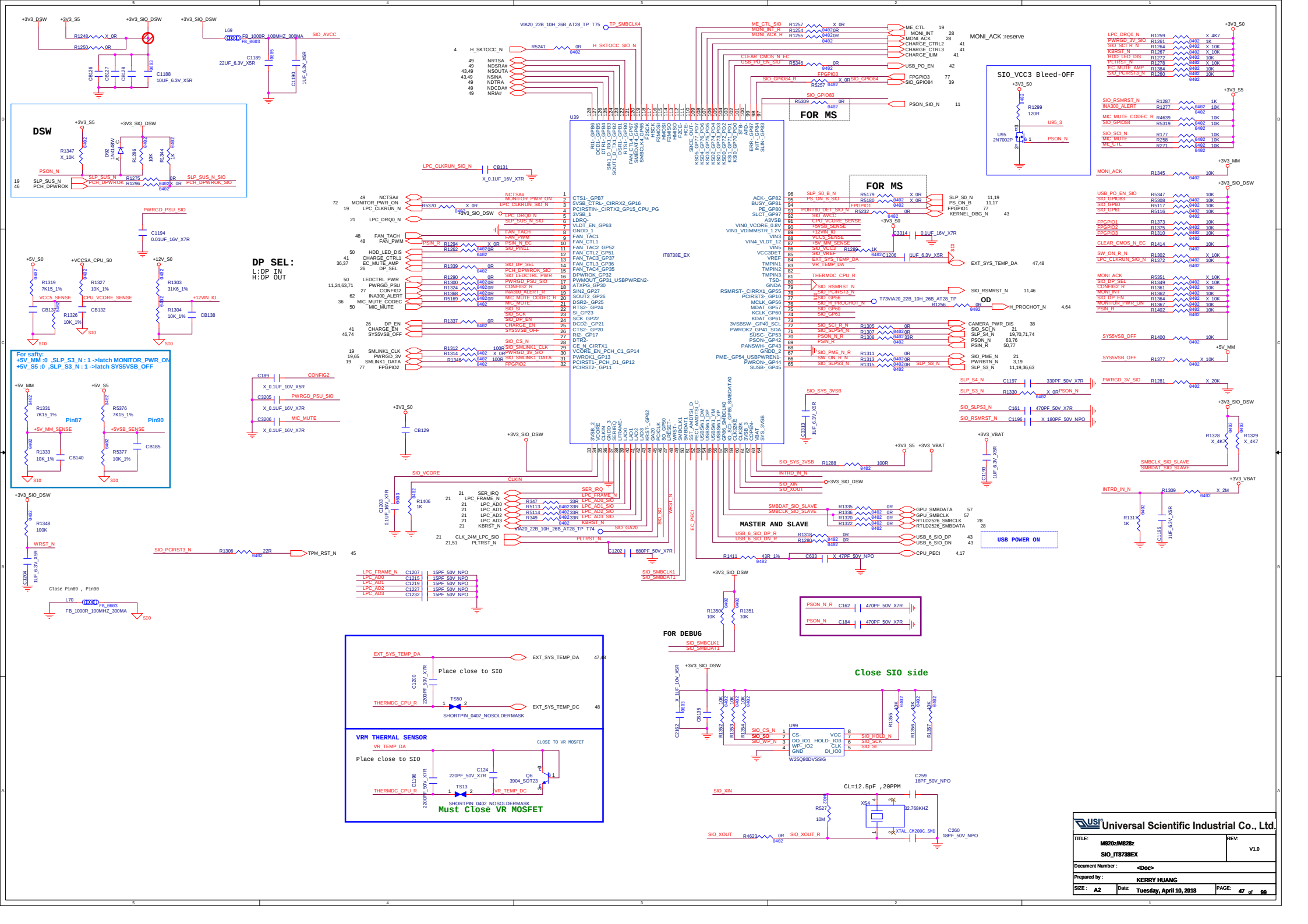


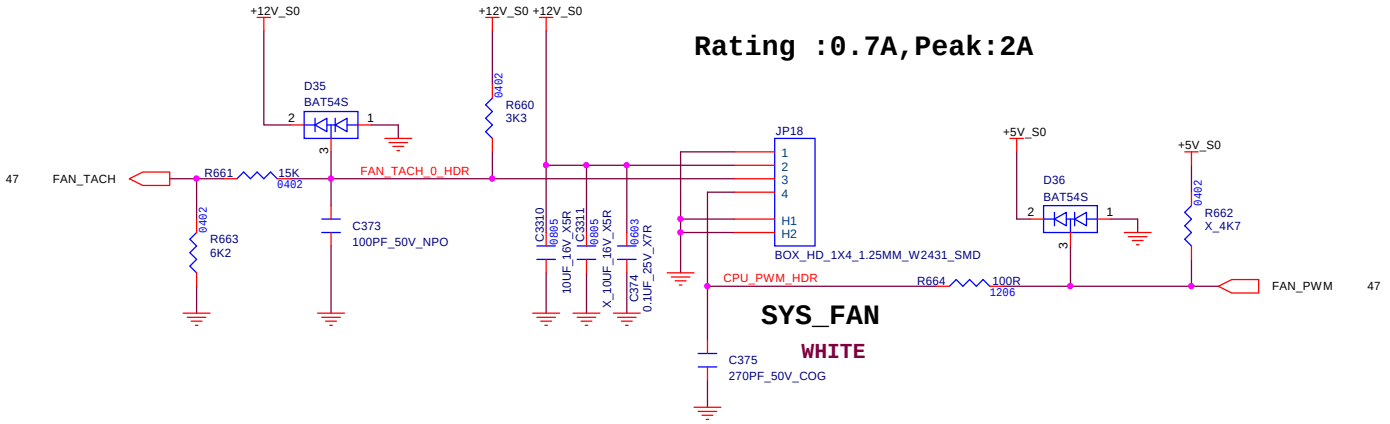


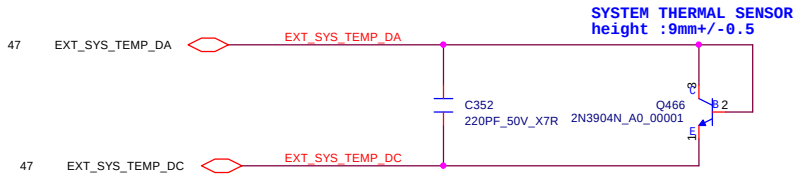
RSMRST LOGIC

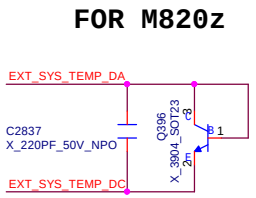


Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z RSMRST LOGIC			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, March 06, 2018		PAGE: 46 of 99


DSW
DP SEL:
L:DP IN
H:DP OUT
For safty:
+5V_MM :0 ,SLP_S3_N : 1 ->latch MONITOR_PWR_ON
+5V_S5 :0 ,SLP_S3_N : 1 ->latch SYS5VSB_OFF
FOR MS
MONI_ACK :reserve
SIO_VCC3 Bleed-OFF
FOR MS
OD
MASTER AND SLAVE
USB POWER ON
FOR DEBUG
Close SIO side
Place close to SIO
VRM THERMAL SENSOR
Place close to SIO
CLOSE TO VR MOSFET
Must Close VR MOSFET
Close Pin89 , Pin90
Universal Scientific Industrial Co., Ltd.
TITLE: M920z/M828z
SIO_IT8738EX
REV: V1.0
Document Number : <Doc>
Prepared by : KERRY HUANG
SIZE : A2
Date: Tuesday, April 10, 2018
PAGE: 47 of 99

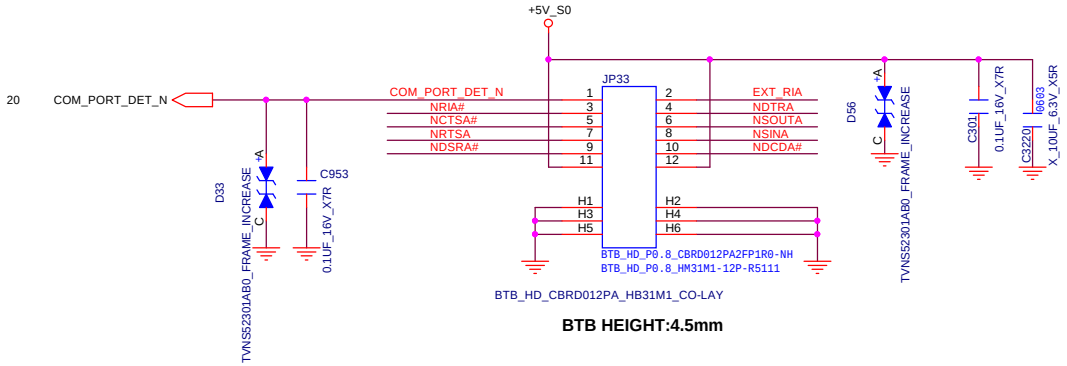




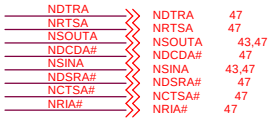


Universal Scientific Industrial Co., Ltd.		
TITLE: M920z/M828z THERMAL_FAN		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 48 of 99

SERIAL PORT 1

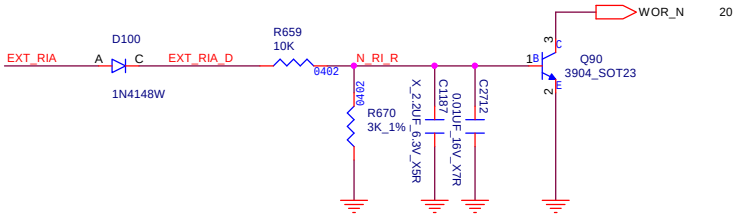


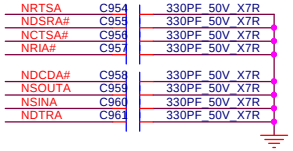
BTB HEIGHT:4.5mm



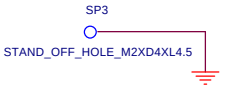
Wake On Modem Header

	N_RI	RI#
Active	+12V_S0	Low
Normal	-12V	High





COM PCB 1.6mm



48-956282-01_Q4_1p45X4p5X1p5XM2.pdf

Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z COM	REV: V1.0
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Tuesday, March 06, 2018
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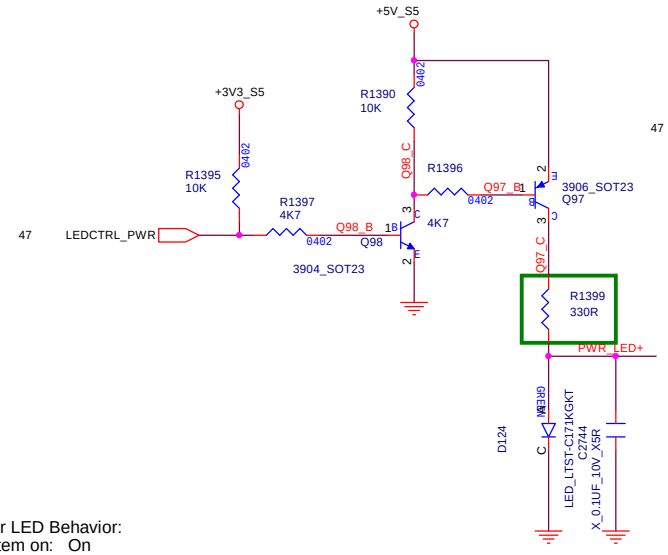
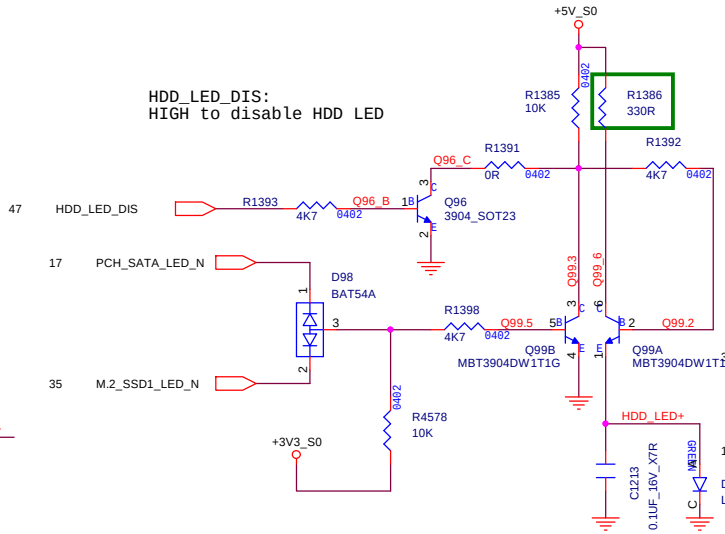
Power LED



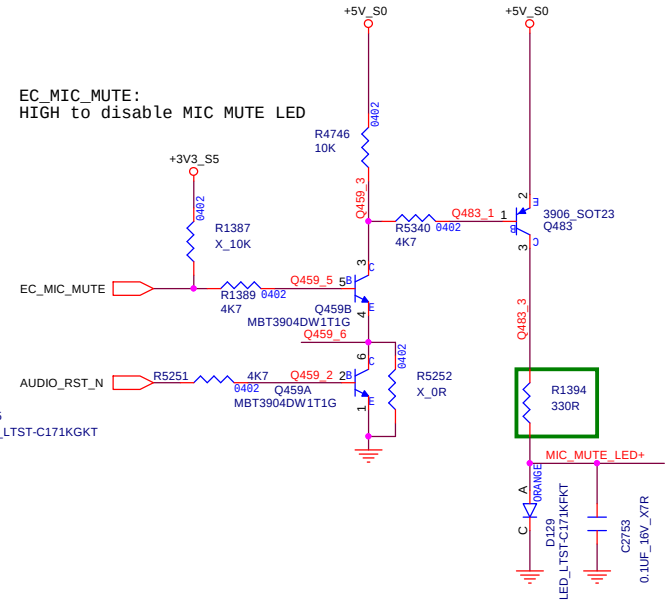
Power LED Behavior:
- System on: On
- System in Standby
  Gradual 1s On, Gradual 1s OFF, 3s OFF
- Initial Connection of Power (e.g. via AC adaptor or AC-in) Blink 3 Times (0.25 s On/ 0.25 s Off , repeat x 3)
- System entering hibernation Blink (0.25 s On/ 0.25 s Off)
- System off OFF

HDD LED



HDD LED Behavior: Blink when HDD active

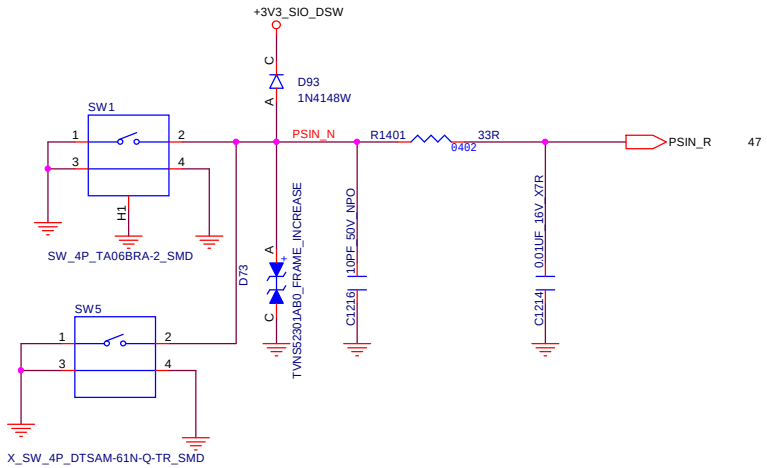
MIC MUTE LED



Mic mute LED Behavior:
ON when muted; OFF when un-muted
S3/S4/S5 will be off
Will keep last state when next reboot or re-power on
The shipping default for Mic mute led is off (after preload in MFG, Mic mute is off)

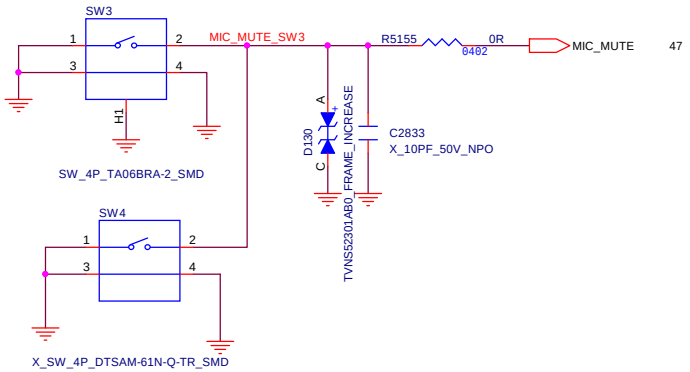
ORANGE

POWER button



46-005323-01

MIC MUTE button



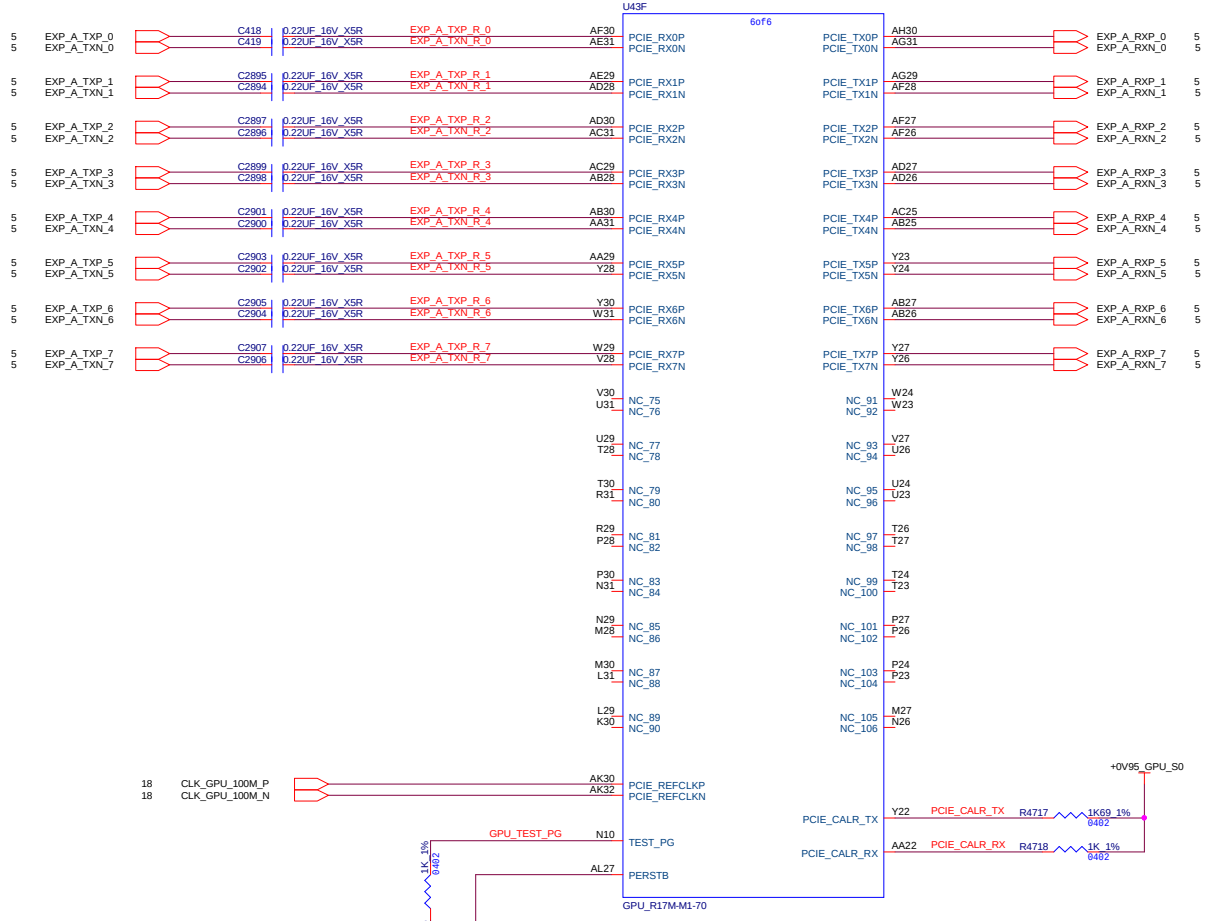
46-005323-01

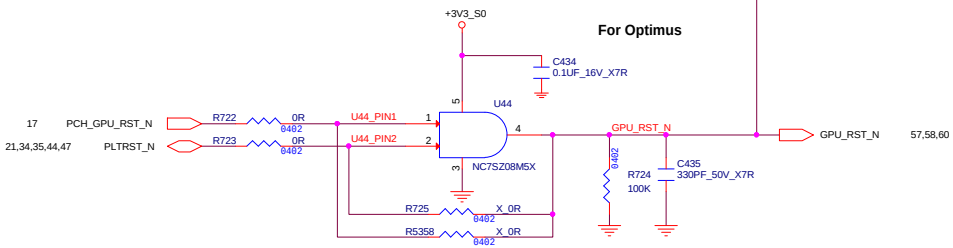
Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z FUNCTION BUTTON			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, March 06, 2018		PAGE: 50 of 99

FOR GPU
HEAT PIPE SCREW HOLES

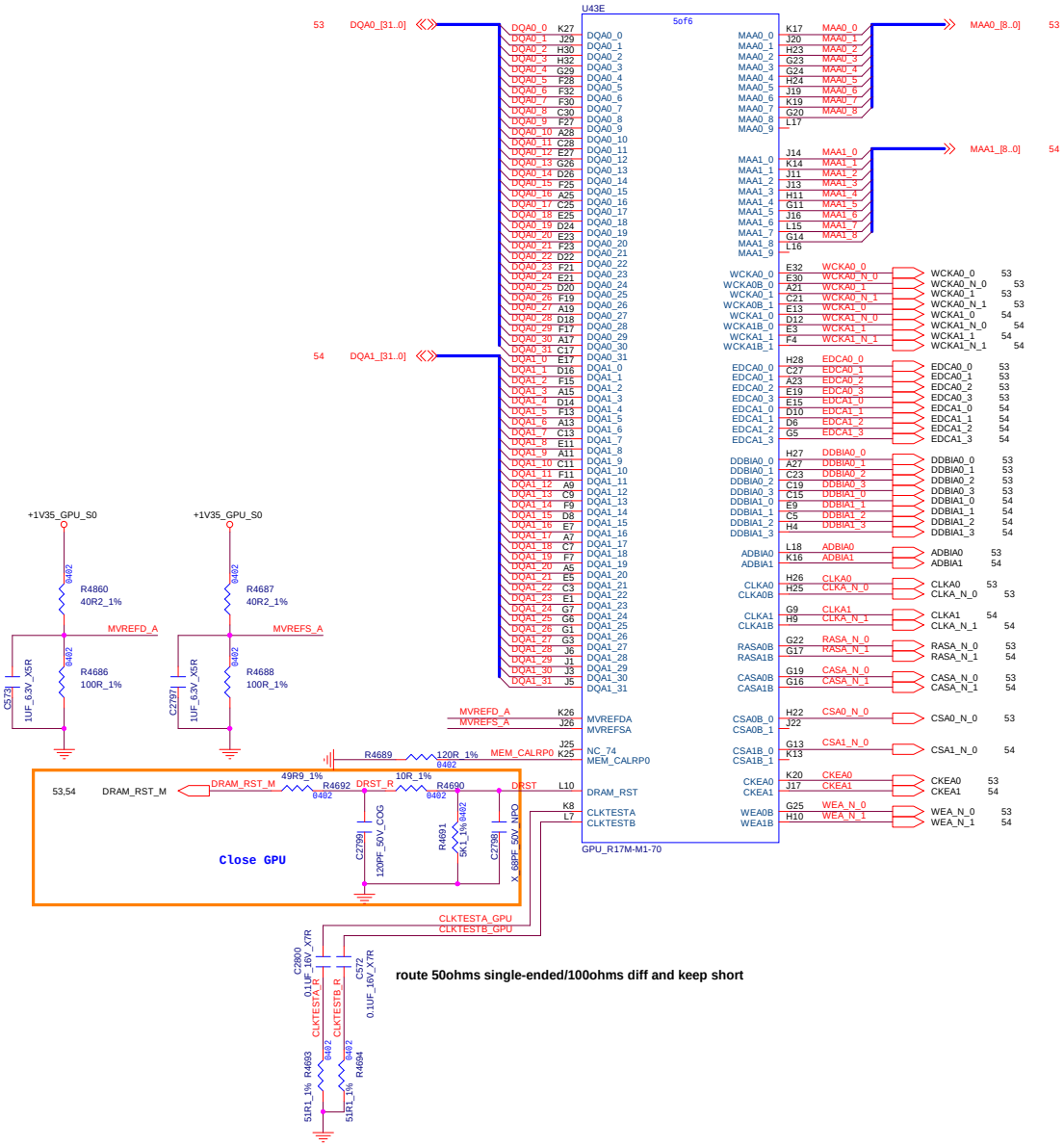
H12 SCREW_HOLE_M2X2.5X1.5

H14 SCREW_HOLE_M2X2.5X1.5





Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z R17M PCIE	REV: V1.0
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : Custom	Date: Tuesday, March 06, 2018
PAGE: 51 of 99	

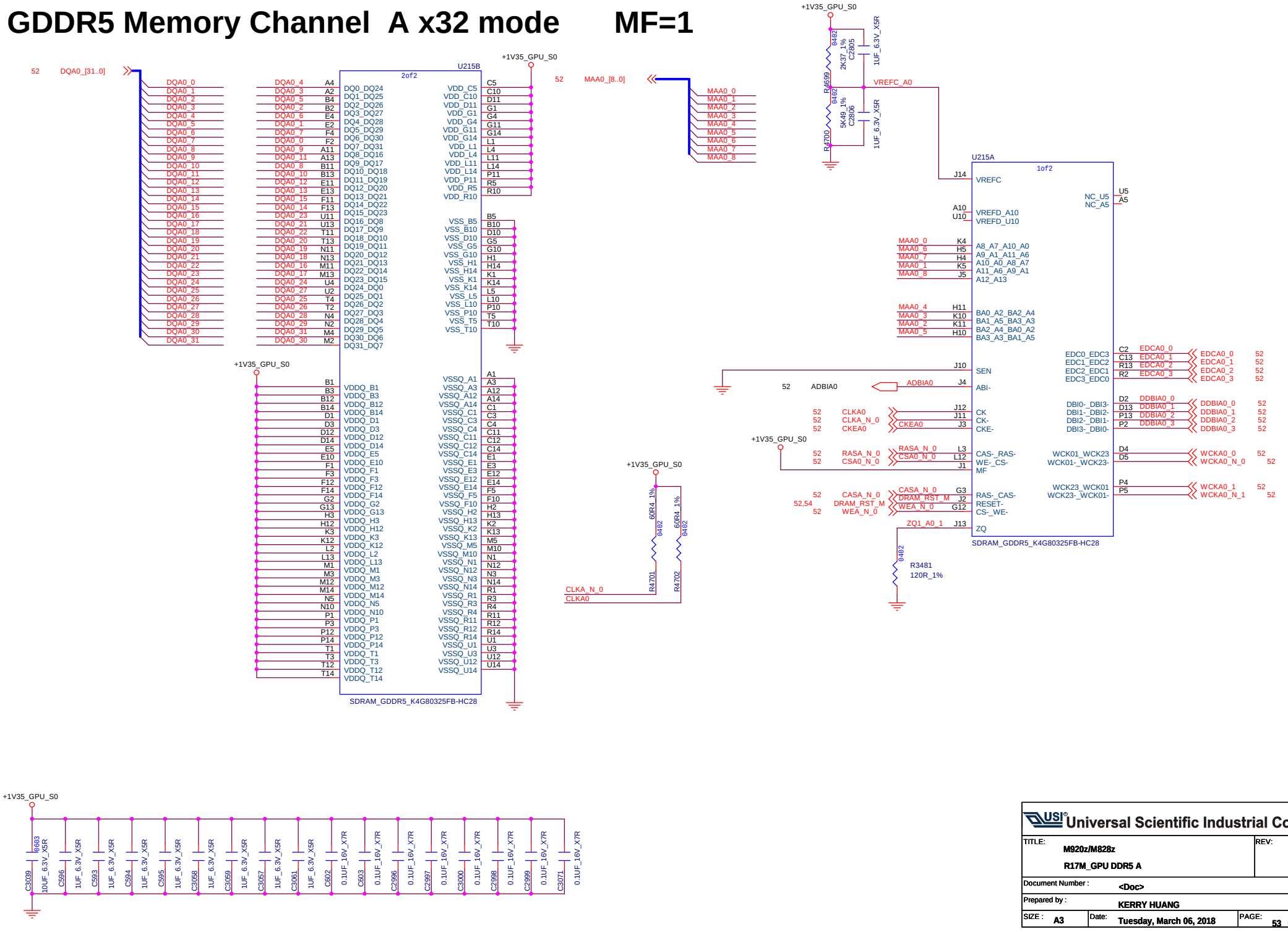


GDDR5 CMD MAPPING TABLE

<0..31>	<32..63>	MEMORY
12	28	RAS
15	31	CAS
5	21	WE
0	16	CS
8	24	ABI
10	26	A0_A10
11	27	A1_A9
2	18	A2_BA0
1	17	A3_BA3
3	19	A4_BA2
4	20	A5_BA1
7	23	A6_A11
6	22	A7_A8
9	25	A12_RFU
14	30	CKE
13	29	RESET

Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z R17M_MEMORY			REV: V1.0
Document Number :			
Prepared by : KERRY HUANG			
SIZE : Custom	Date: Tuesday, March 06, 2018		PAGE: 52 of 99

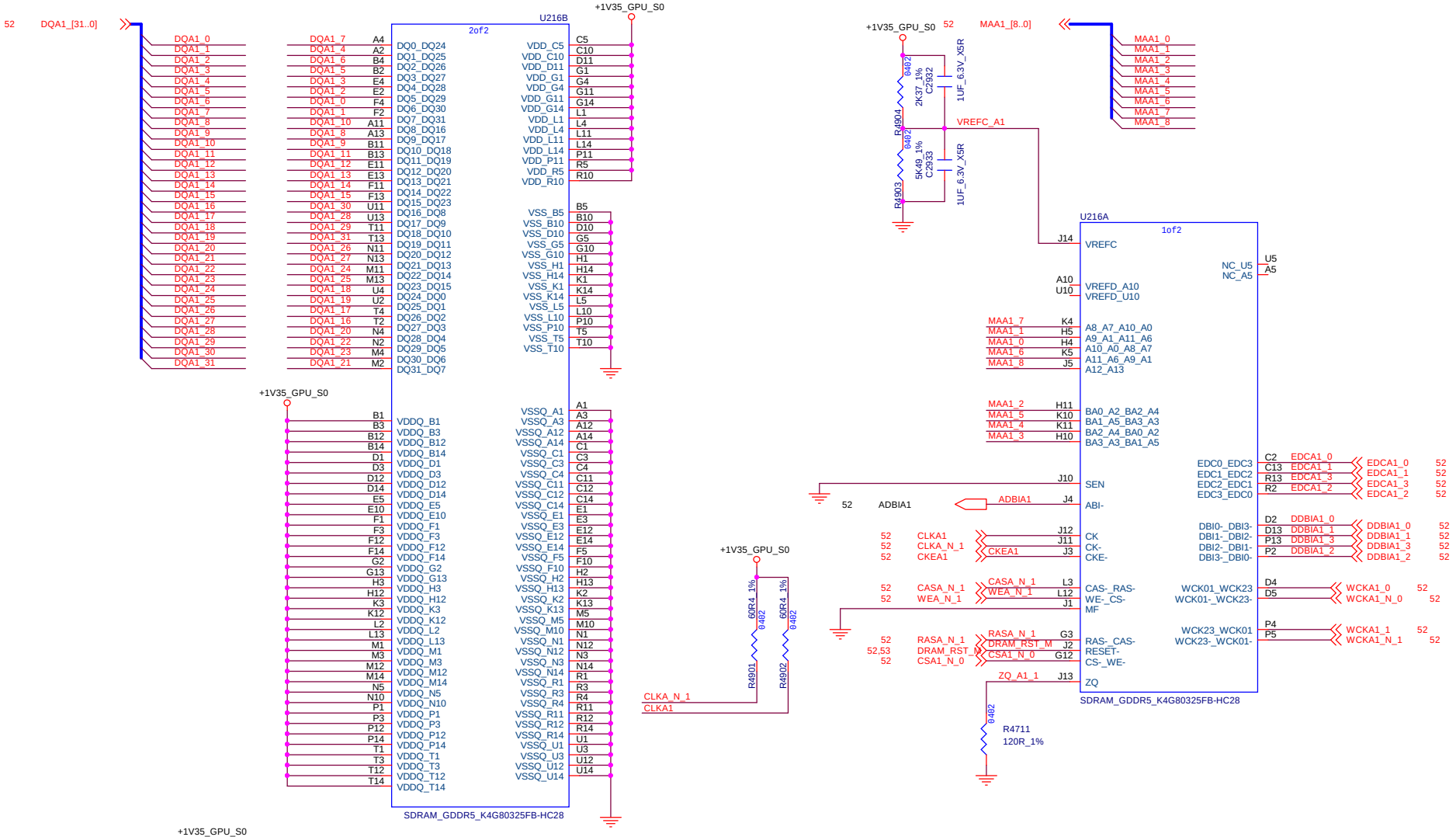
GDDR5 Memory Channel A x32 mode MF=1

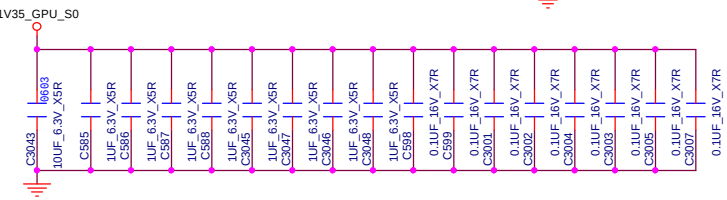


Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z R17M_GPU DDR5 A			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 53 of 99	

GDDR5 Memory Channel B x32 mode

MF=0





Universal Scientific Industrial Co., Ltd.			
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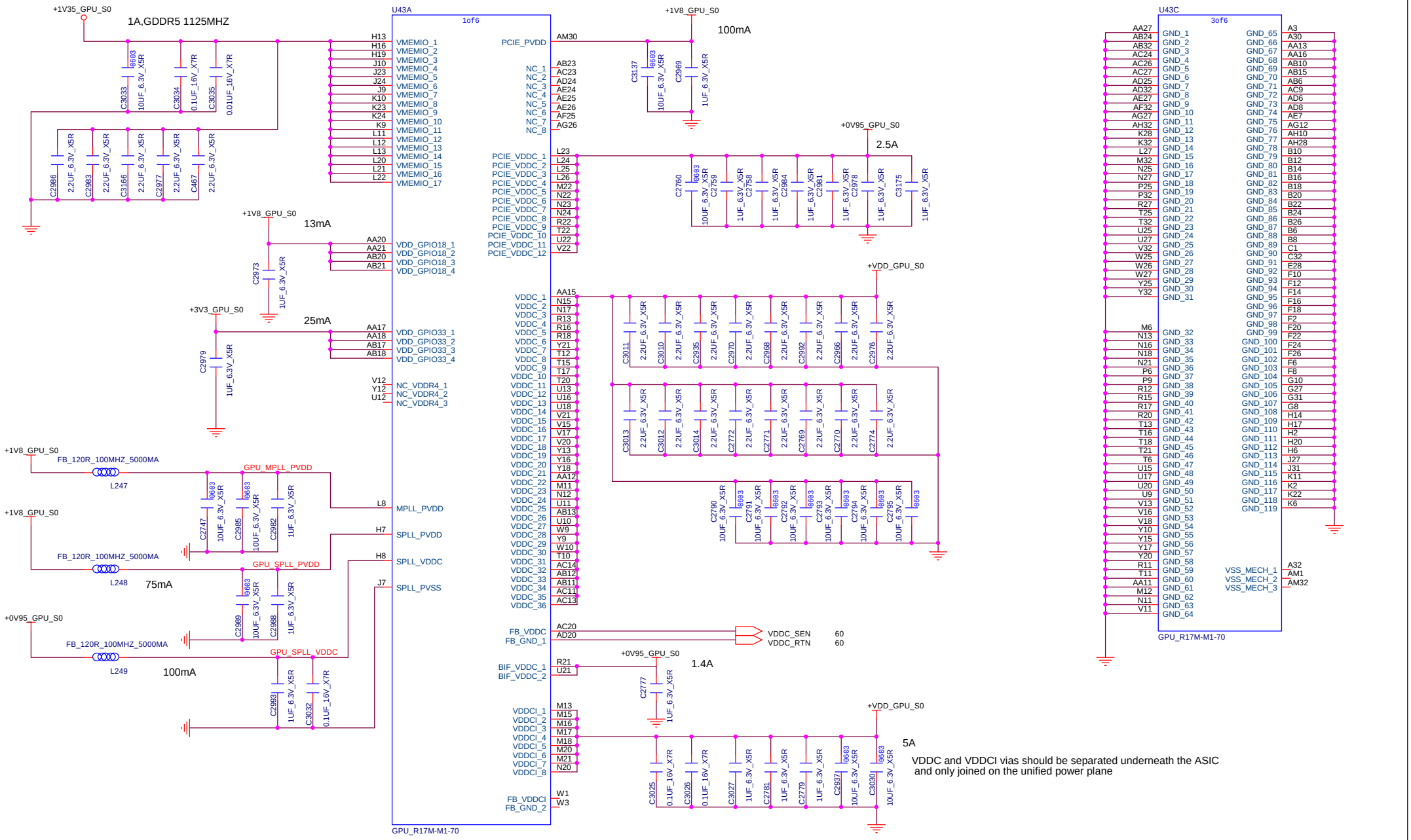
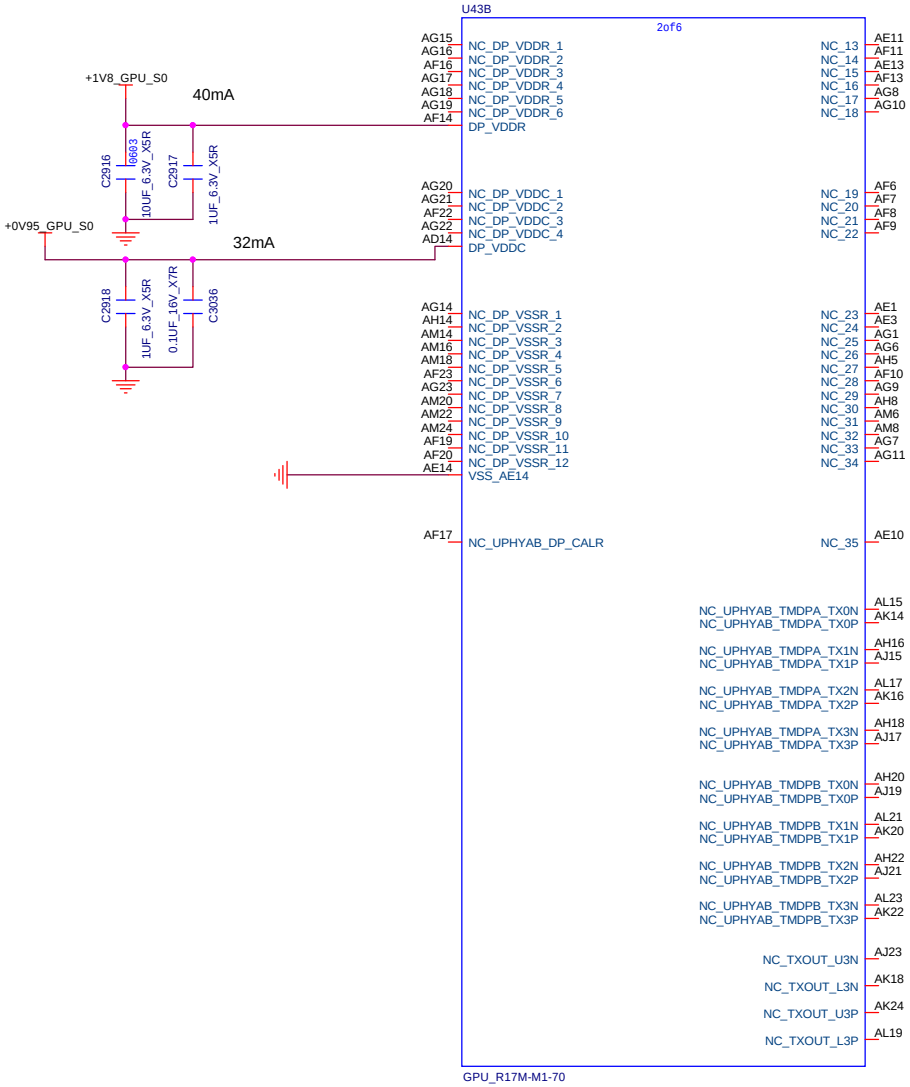
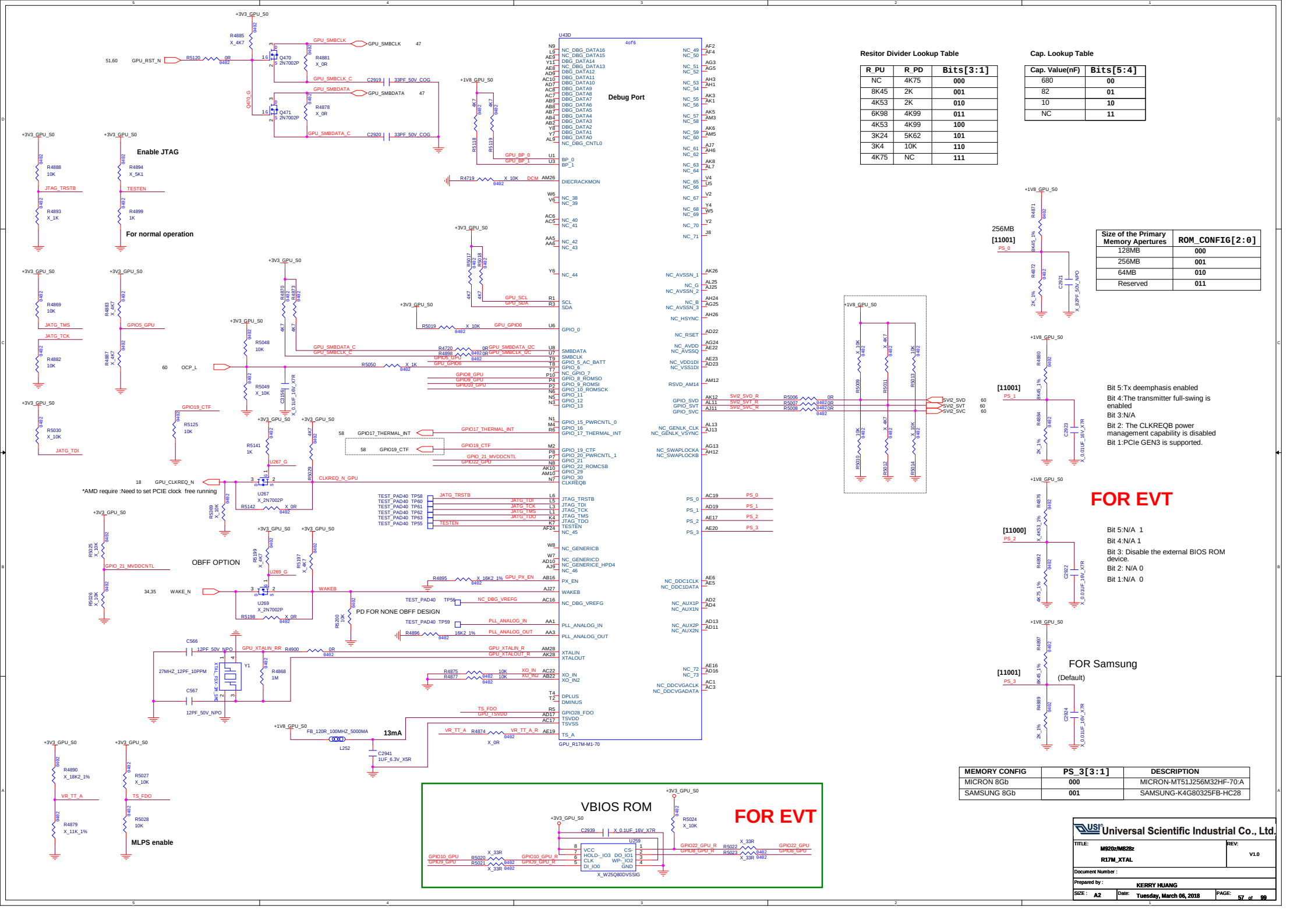
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, March 06, 2018		PAGE: 54 of 99



Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z R17M_POWER	REV: V1.0
Document Number :	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Tuesday, March 06, 2018
PAGE: 55 of 99	



Universal Scientific Industrial Co., Ltd.		
TITLE: M920z/M828z R17M_IFP/DAC		REV: V1.0
Document Number :		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 56 of 99



Resitor Divider Lookup Table

R_PU	R_PD	Bits[3:1]
NC	4K75	000
8K45	2K	001
4K53	2K	010
6K98	4K99	011
4K53	4K99	100
3K24	5K62	101
3K4	10K	110
4K75	NC	111

Cap. Lookup Table

Cap. Value(nF)	Bits[5:4]
680	00
82	01
10	10
NC	11

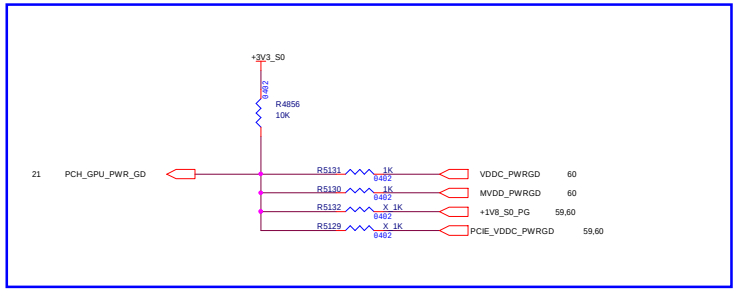
Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128MB	000
256MB	001
64MB	010
Reserved	011

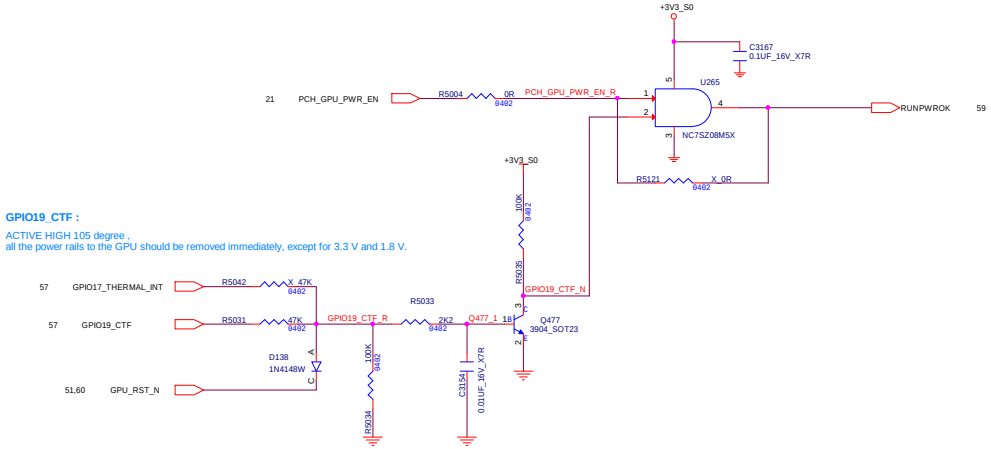
Bit 5:Tx deemphasis enabled
Bit 4:The transmitter full-swing is enabled
Bit 3:N/A
Bit 2: The CLKREQB power management capability is disabled
Bit 1:PCIe GEN3 is supported.

Bit 5:N/A 1
Bit 4:N/A 1
Bit 3: Disable the external BIOS ROM device.
Bit 2: N/A 0
Bit 1:N/A 0

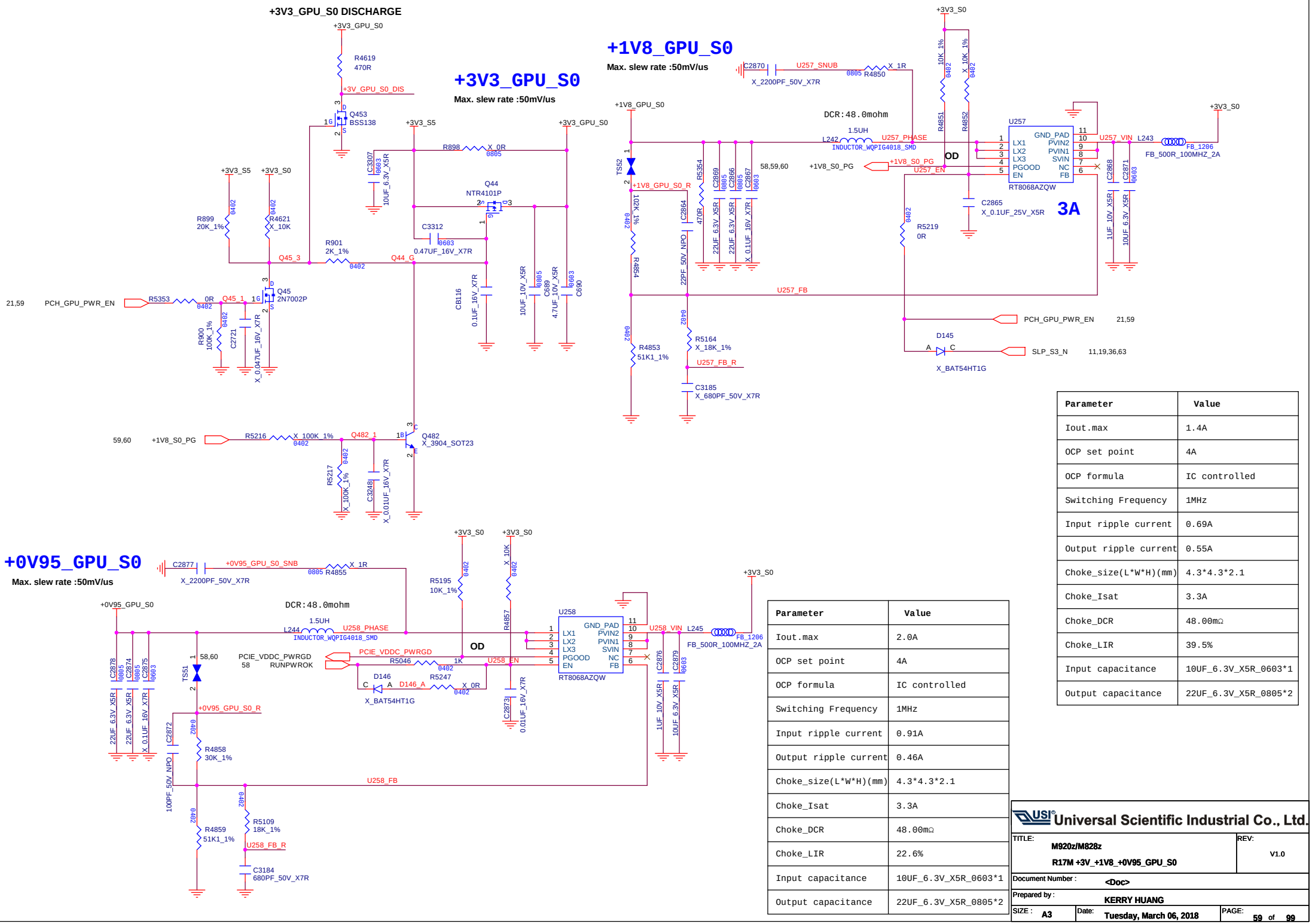
MEMORY CONFIG	PS_3[3:1]	DESCRIPTION
MICRON 8Gb	000	MICRON-MT51J256M32HF-70:A
SAMSUNG 8Gb	001	SAMSUNG-K4G80325FB-HC28

Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M820z R17M_XTAL	REV: V1.0
Document Number :	
Prepared by : KERRY HUANG	
SIZE : A2	Date: Tuesday, March 06, 2018 PAGE: 57 of 99





Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M826z R17M TIMING CONTROL LOGIC			REV: V1.0
Document Number :			
Prepared by : KERRY HUANG			
SIZE : A2	Date: Tuesday, March 06, 2018	PAGE: 58 of 99	

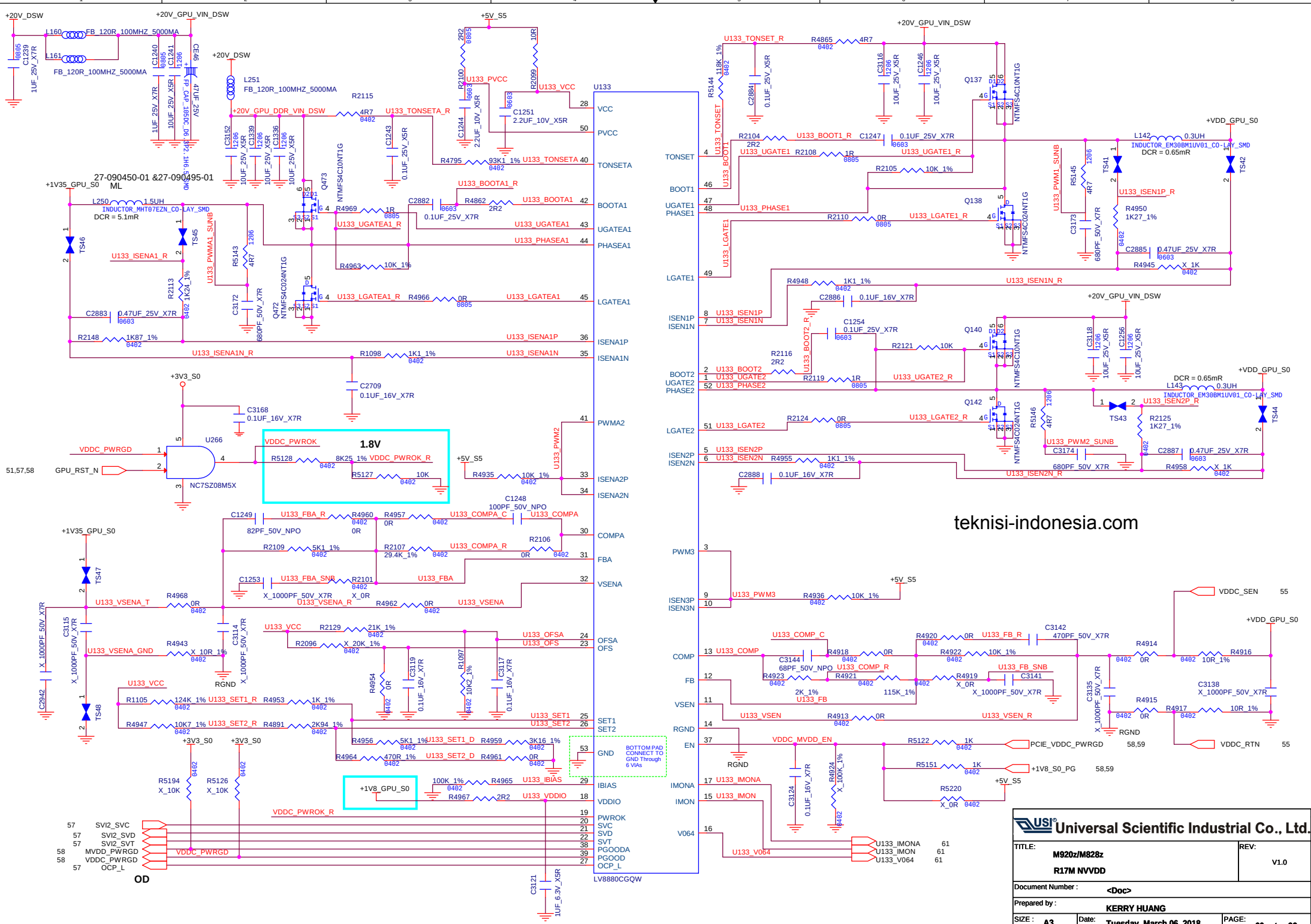


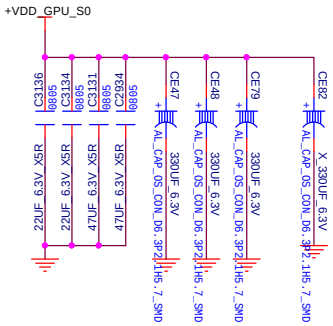
Parameter	Value
Iout.max	1.4A
OCP set point	4A
OCP formula	IC controlled
Switching Frequency	1MHz
Input ripple current	0.69A
Output ripple current	0.55A
Choke_size(L*W*H)(mm)	4.3*4.3*2.1
Choke_Isat	3.3A
Choke_DCR	48.00mΩ
Choke_LIR	39.5%
Input capacitance	10UF_6.3V_X5R_0603*1
Output capacitance	22UF_6.3V_X5R_0805*2

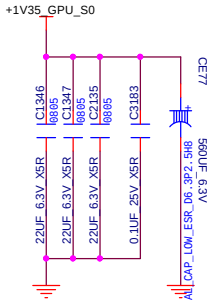
Parameter	Value
Iout.max	2.0A
OCP set point	4A
OCP formula	IC controlled
Switching Frequency	1MHz
Input ripple current	0.91A
Output ripple current	0.46A
Choke_size(L*W*H)(mm)	4.3*4.3*2.1
Choke_Isat	3.3A
Choke_DCR	48.00mΩ
Choke_LIR	22.6%
Input capacitance	10UF_6.3V_X5R_0603*1
Output capacitance	22UF_6.3V_X5R_0805*2

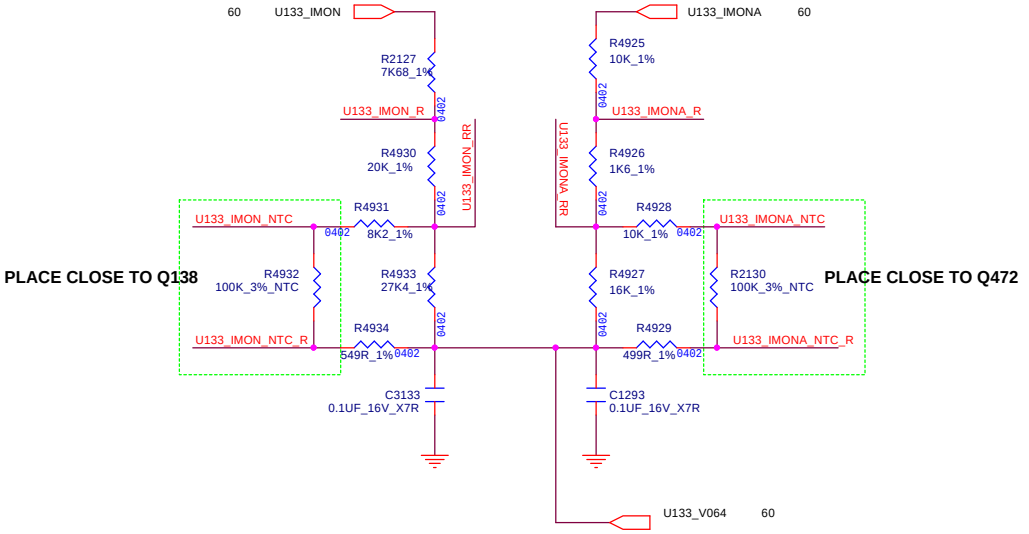
Universal Scientific Industrial Co., Ltd.

TITLE: M920z/M828z R17M +3V_+1V8_+0V95_GPU_S0		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 59 of 99


+20V_DSW
+20V_GPU_VIN_DSW
+5V_S5
+20V_GPU_DDR_VIN_DSW
27-090450-01 &27-090495-01
ML
+1V35_GPU_S0
+3V3_S0
+1V8_GPU_S0
+VDD_GPU_S0
1.8V
VDDC_PWROK
VDDC_PWROK_R
GPU_RST_N
NC7SZ08M5X
U133
LV8880CGQW
VCC
PVCC
TONSETA
BOOTA1
UGATEA1
PHASEA1
LGATEA1
ISENA1P
ISENA1N
PWMA2
ISENA2P
ISENA2N
COMPA
FBA
VSENA
OFSA
SET1
SET2
GND
IBIAS
VDDIO
PWROK
SVC
SVD
SVT
PGOODA
PGOOD
OCP_L
TONSET
BOOT1
UGATE1
PHASE1
LGATE1
ISEN1P
ISEN1N
BOOT2
UGATE2
PHASE2
LGATE2
ISEN2P
ISEN2N
PWM3
ISEN3P
ISEN3N
COMP
FB
VSEN
RGND
EN
IMONA
IMON
V064
BOTTOM PAD CONNECT TO GND Through 6 VIAs
OD
SVI2_SVC
SVI2_SVD
SVI2_SVT
MVDD_PWRGD
VDDC_PWRGD
OCP_L
PCIE_VDDC_PWRGD
+1V8_S0_PG
VDDC_SEN
VDDC_RTN
teknisi-indonesia.com
Universal Scientific Industrial Co., Ltd.
TITLE: M920z/M828z
R17M NVVDD
REV: V1.0
Document Number : <Doc>
Prepared by : KERRY HUANG
SIZE : A3
Date: Tuesday, March 06, 2018
PAGE: 60 of 99







+VDD_GPU_S0

Parameter	Value
Iout.max	42A Per-phase : 21A
OCP set point	63A Per-phase : 31.5A
OCP formula	I_L = (3.19375-0.64)/DCR*(Rcsx/RIMON)
Switching Frequency	350kHz
Input ripple current	5.03A
Output ripple current	10.9A
Choke_size(L*W*H)(mm)	11.5*8.05*5.5
Choke_Isat	63A
Choke_DCR	0.65mΩ
Choke_LIR	51.9%
Input capacitance	10UF_25V_X5R_1206*4
Output capacitance (Near GPU side)	330UF_6.3V*4 22UF_6.3V_X5R_0805*2

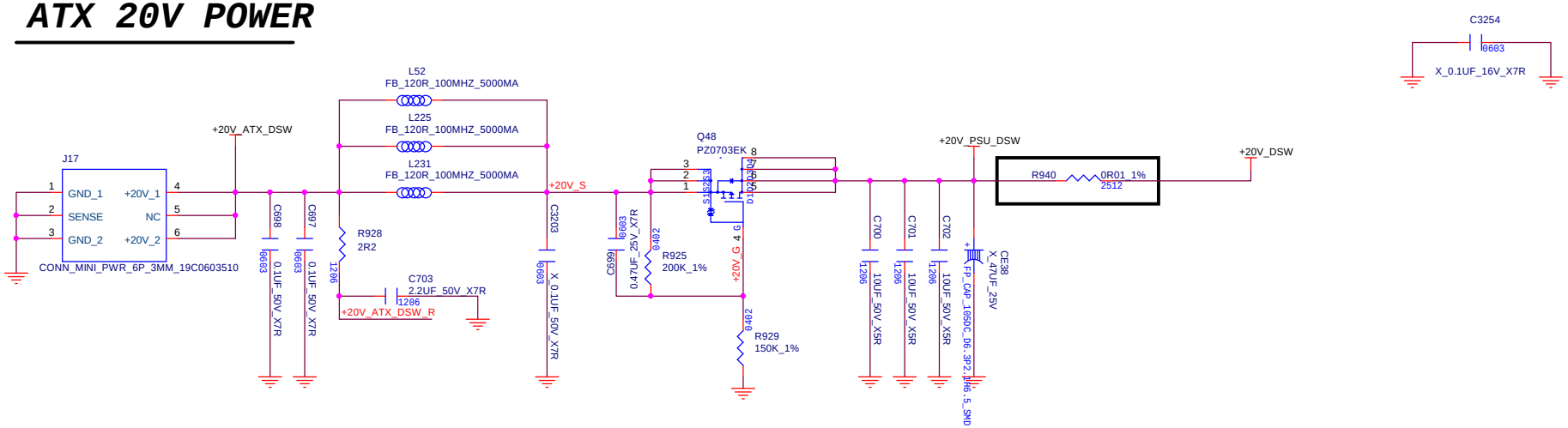
+1V35_GPU_S0

Parameter	Value
Iout.max	5A
OCP set point	11.0A
OCP formula	I_L = (3.19375-0.64)/DCR*(Rcsx/RIMONA)
Switching Frequency	450kHz
Input ripple current	1.26A
Output ripple current	1.865A
Choke_size(L*W*H)(mm)	7.0*8.3*5.0
Choke_Isat	11A
Choke_DCR	5.1mΩ
Choke_LIR	37.3%
Input capacitance	10UF_25V_X5R_1206*2
Output capacitance (Near GPU side)	330UF_6.3V*1 22UF_6.3V_X5R_0805*3

Universal Scientific Industrial Co., Ltd.

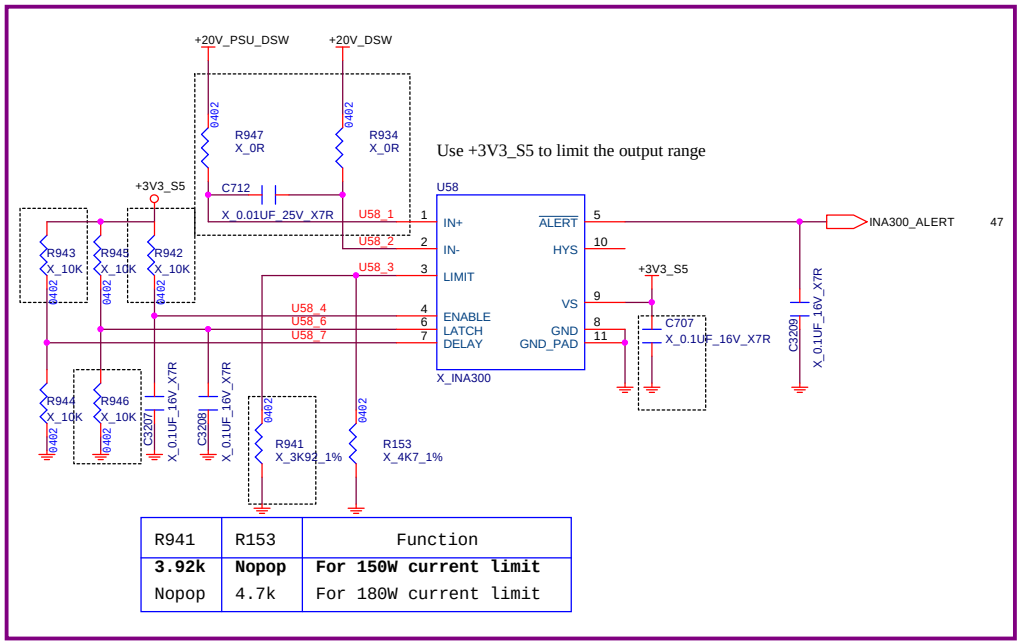
TITLE: M920z/M828z R17M OUTPUT		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 61 of 99

ATX 20V POWER



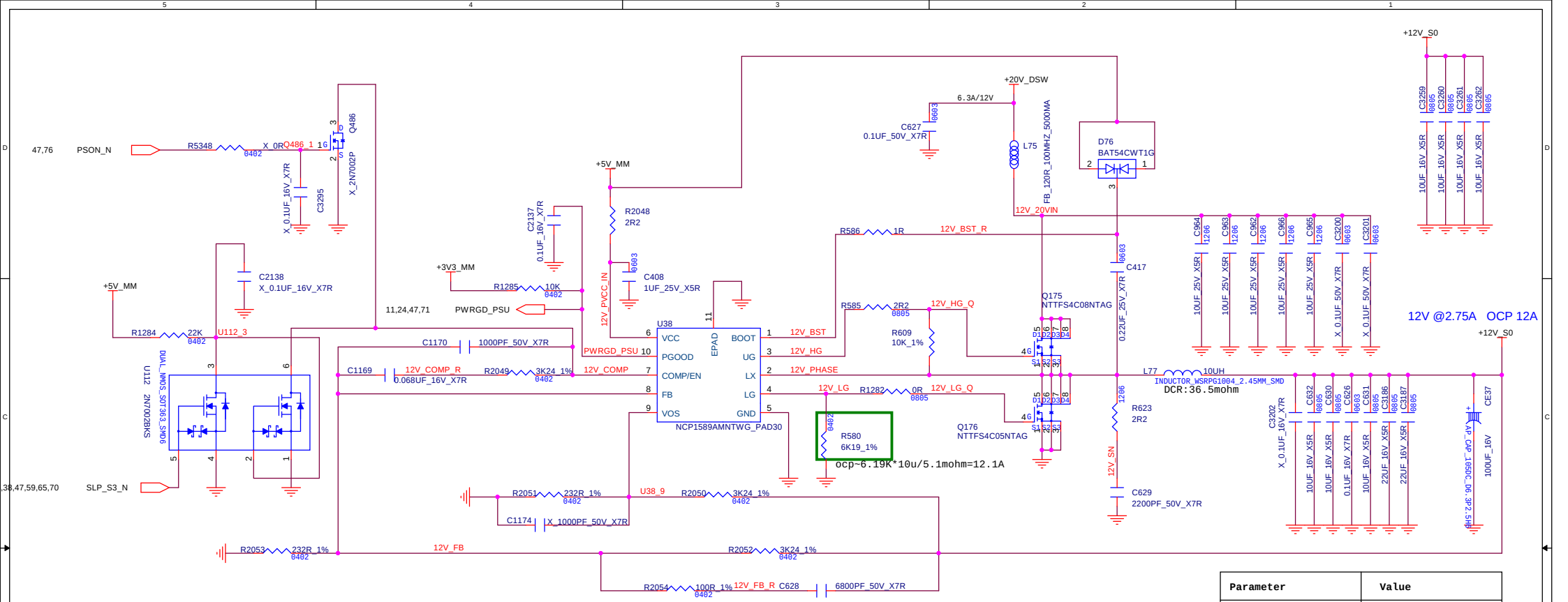
POWER METER (INA300)

For M920 UMA,M828z



R941	R153	Function
3.92k	**Nopop**	**For 150W current limit**
Nopop	4.7k	For 180W current limit

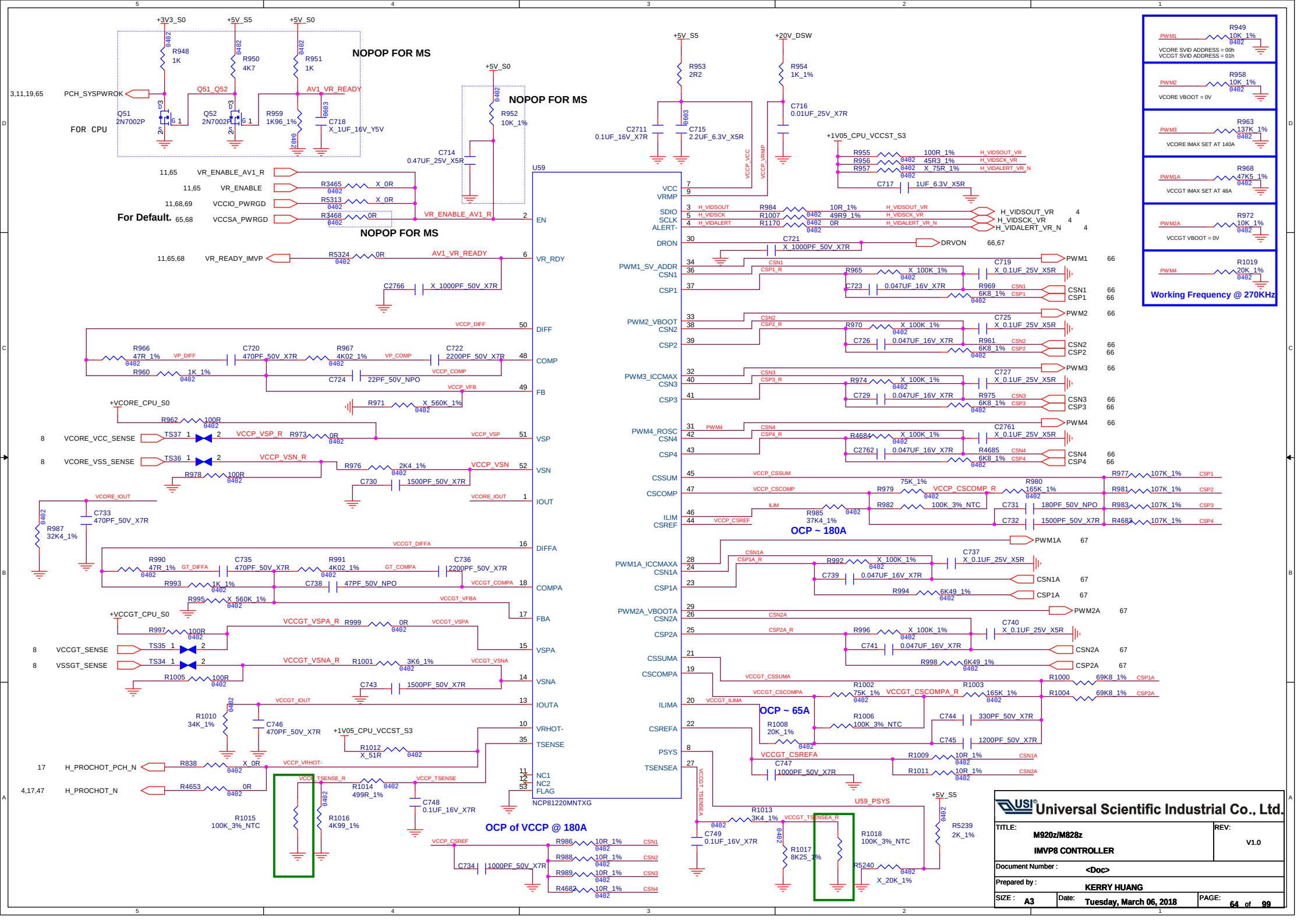
Universal Scientific Industrial Co., Ltd.		
TITLE: M920z/M828z DC IN		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 62 of 99

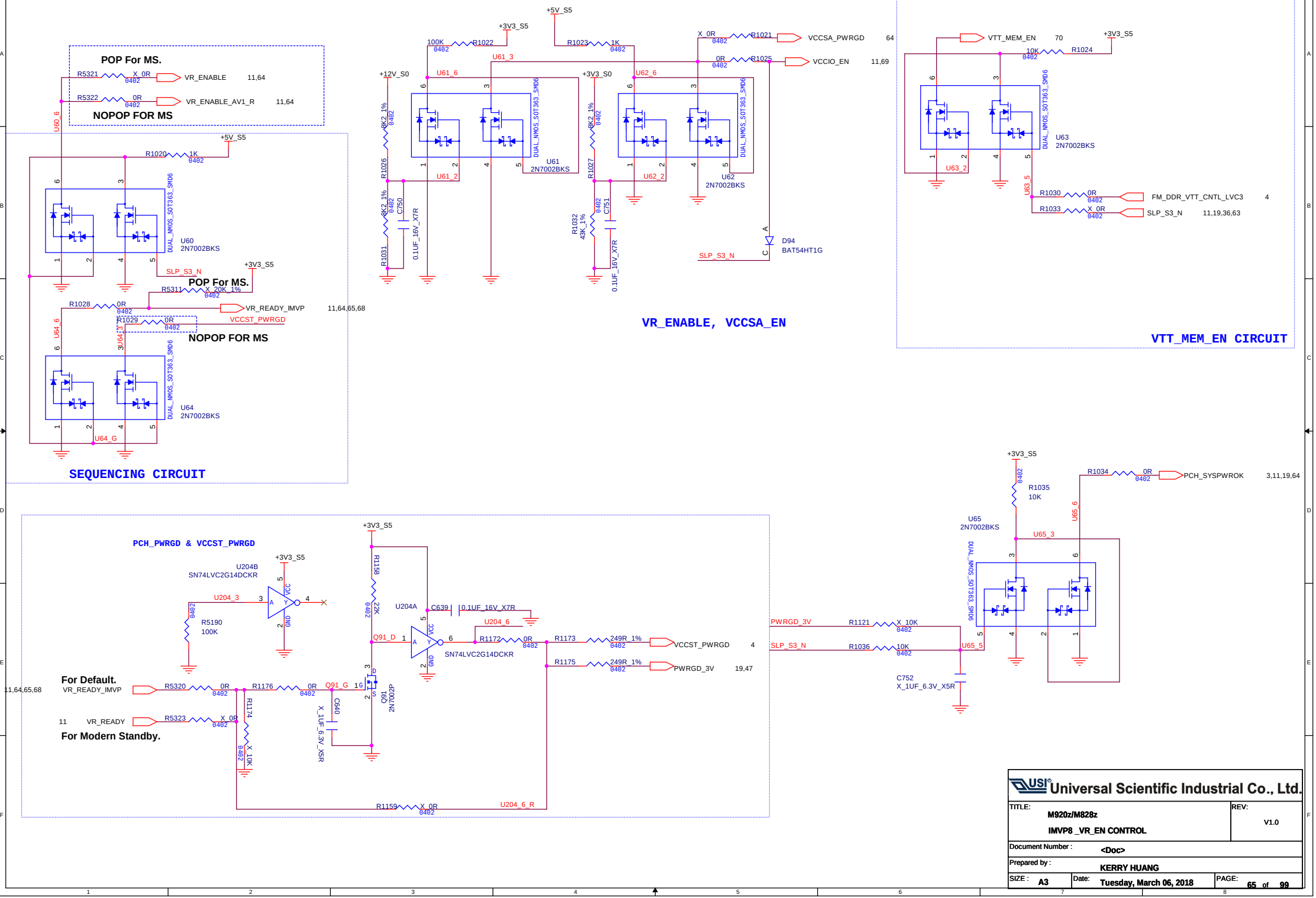


Parameter	Value
Iout.max	2.7A@Ipeak =4.1A
OCP set point	12.1A
OCP formula	ROCSET*10uA/Rds_on
Switching Frequency	300kHz
Input ripple current	1.81A
Output ripple current	1.6A
Choke_size(L*W*H)(mm)	11.5*10.3*4.2
Choke_Isat	12A
Choke_DCR	36.5mΩ
Choke_LIR	43.2%
Input capacitance	10UF_25V_X5R_1206*5
Output capacitance	270UF_16V*1 10UF_16V_X5R_0805*3

Universal Scientific Industrial Co., Ltd.

TITLE: M920z/M828z 20V TO 12V		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 63 of 99


NOPOP FOR MS
FOR CPU
PCH_SYSPWROK
Q51_Q52
AV1_VR_READY
Q51 2N7002P
Q52 2N7002P
R948 1K
R950 4K7
R951 1K
R959 1K96_1%
C718 X_1UF_16V_Y5V
R952 10K_1%
C714 0.47UF_25V_X5R
For Default.
VR_ENABLE_AV1_R
VR_ENABLE
VCCIO_PWRGD
VCCSA_PWRGD
R3465 X_0R
R5313 X_0R
R3468 0R
U59
EN
VR_RDY
DIFF
COMP
FB
VSP
VSN
IOUT
DIFFA
COMPA
FBA
VSPA
VSNA
IOUTA
VRHOT-
TSENSE
NC1
NC2
FLAG
NCP81220MNTXG
R5324 0R
C2766 X_1000PF_50V_X7R
R966 47R_1%
C720 470PF_50V_X7R
R967 4K02_1%
C722 2200PF_50V_X7R
R960 1K_1%
C724 22PF_50V_NPO
R971 X_560K_1%
R962 100R
R973 0R
R976 2K4_1%
R978 100R
C730 1500PF_50V_X7R
R987 32K4_1%
C733 470PF_50V_X7R
R990 47R_1%
C735 470PF_50V_X7R
R991 4K02_1%
C736 2200PF_50V_X7R
R993 1K_1%
C738 47PF_50V_NPO
R995 X_560K_1%
R997 100R
R999 0R
R1001 3K6_1%
R1005 100R
C743 1500PF_50V_X7R
R1010 34K_1%
C746 470PF_50V_X7R
R1012 X_51R
R838 X_0R
R4653 0R
R1014 499R_1%
C748 0.1UF_16V_X7R
R1015 100K_3%_NTC
R1016 4K99_1%
OCP of VCCP @ 180A
R986 10R_1%
R988 10R_1%
R989 10R_1%
R4682 10R_1%
C734 1000PF_50V_X7R
+5V_S5
+20V_DSW
R953 2R2
R954 1K_1%
C716 0.01UF_25V_X7R
C2711 0.1UF_16V_X7R
C715 2.2UF_6.3V_X5R
+1V05_CPU_VCCST_S3
R955 100R_1%
R956 45R3_1%
R957 X_75R_1%
C717 1UF_6.3V_X5R
R984 10R_1%
R1007 49R9_1%
R1170 0R
C721 X_1000PF_50V_X7R
DRVON
PWM1_SV_ADDR
PWM2_VBOOT
PWM3_ICCMAX
PWM4_ROSC
CSSUM
CSCOMP
ILIM
CSREF
R965 X_100K_1%
C723 0.047UF_16V_X7R
R969 6K8_1%
C719 X_0.1UF_25V_X5R
R970 X_100K_1%
C726 0.047UF_16V_X7R
R961 6K8_1%
C725 X_0.1UF_25V_X5R
R974 X_100K_1%
C729 0.047UF_16V_X7R
R975 6K8_1%
C727 X_0.1UF_25V_X5R
R4684 X_100K_1%
C2762 0.047UF_16V_X7R
R4685 6K8_1%
C2761 X_0.1UF_25V_X5R
R979 75K_1%
R980 165K_1%
R982 100K_3%_NTC
R985 37K4_1%
C731 180PF_50V_NPO
C732 1500PF_50V_X7R
R977 107K_1%
R981 107K_1%
R983 107K_1%
R4683 107K_1%
OCP ~ 180A
PWM1A_ICCMAXA
CSP1A
CSP2A
CSSUMA
CSCOMPA
ILIMA
CSREFA
PSYS
TSENSEA
R992 X_100K_1%
C739 0.047UF_16V_X7R
R994 6K49_1%
C737 X_0.1UF_25V_X5R
R996 X_100K_1%
C741 0.047UF_16V_X7R
R998 6K49_1%
C740 X_0.1UF_25V_X5R
R1002 75K_1%
R1003 165K_1%
R1000 69K8_1%
R1004 69K8_1%
R1006 100K_3%_NTC
R1008 20K_1%
C744 330PF_50V_X7R
C745 1200PF_50V_X7R
C747 1000PF_50V_X7R
R1009 10R_1%
R1011 10R_1%
OCP ~ 65A
R1013 3K4_1%
C749 0.1UF_16V_X7R
R1017 8K25_1%
R1018 100K_3%_NTC
R5240 X_20K_1%
R5239 2K_1%
R949 10K_1%
VCORE SVID ADDRESS = 00h
VCCGT SVID ADDRESS = 01h
R958 10K_1%
VCORE VBOOT = 0V
R963 137K_1%
VCORE IMAX SET AT 140A
R968 47K5_1%
VCCGT IMAX SET AT 48A
R972 10K_1%
VCCGT VBOOT = 0V
R1019 20K_1%
Working Frequency @ 270KHz
Universal Scientific Industrial Co., Ltd.
TITLE: M920z/M828z
IMVP8 CONTROLLER
REV: V1.0
Document Number : <Doc>
Prepared by : KERRY HUANG
SIZE : A3
Date: Tuesday, March 06, 2018
PAGE: 64 of 99



Universal Scientific Industrial Co., Ltd.		
TITLE: M920z/M828z IMVP8 _VR_EN CONTROL		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 65 of 99

W=20 MILS

X5R/X7R base on thermal test result

X5R/X7R base on thermal test result

Parameter	Value
Iout.max	133A
OCP set point	172A
OCP formula	Formula
Switching Frequency	360kHz
Input ripple current	4.95A
Output ripple current	10.83A
Choke_size(L*W*H)(mm)	11.5*10.3*4.2
Choke_Isat	60A
Choke_DCR	1.2mΩ
Choke_LIR	35.3%
CPU Load Line	2.1mΩ
Input capacitance	47UF_25V*3 10UF_25V_X5R_1206*5 4.7UF_25V_X5R_0805*3
Output capacitance	560UF_2.5V*5 22UF_6.3V_X5R_0805*3

Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z VCORE OUTPUT DRIVEVE	REV: V1.0
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Tuesday, July 10, 2018
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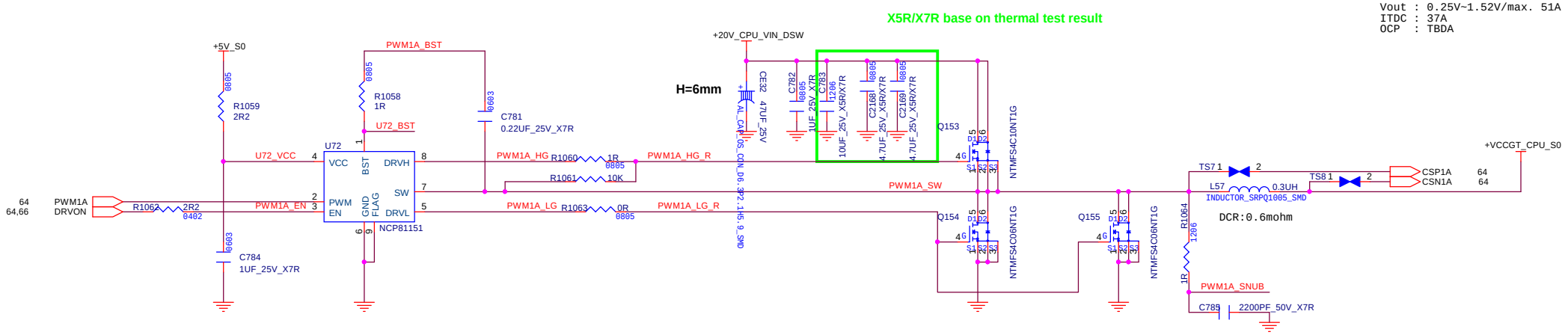
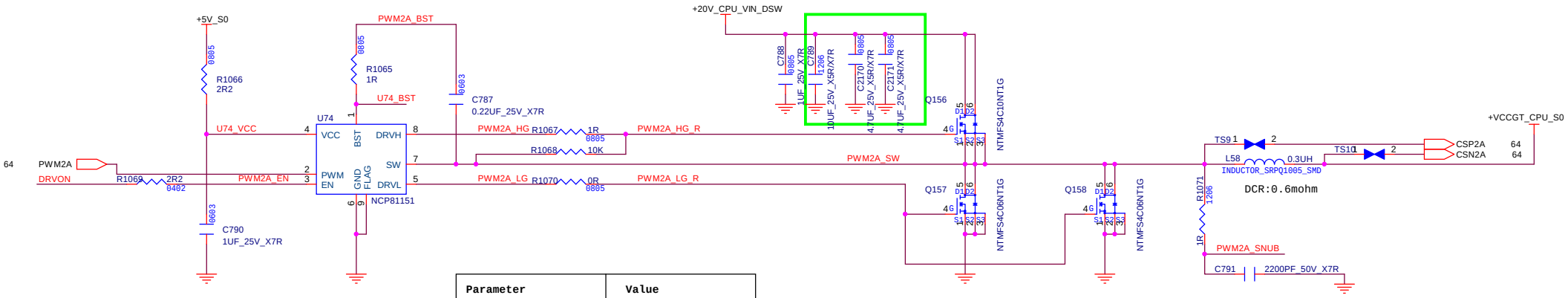
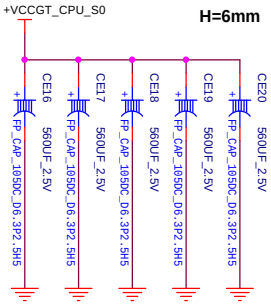
+VCCGT_CPU_S0

Vin : 20V
Vout : 0.25V~1.52V/max. 51A
ITDC : 37A
OCP : TBDA



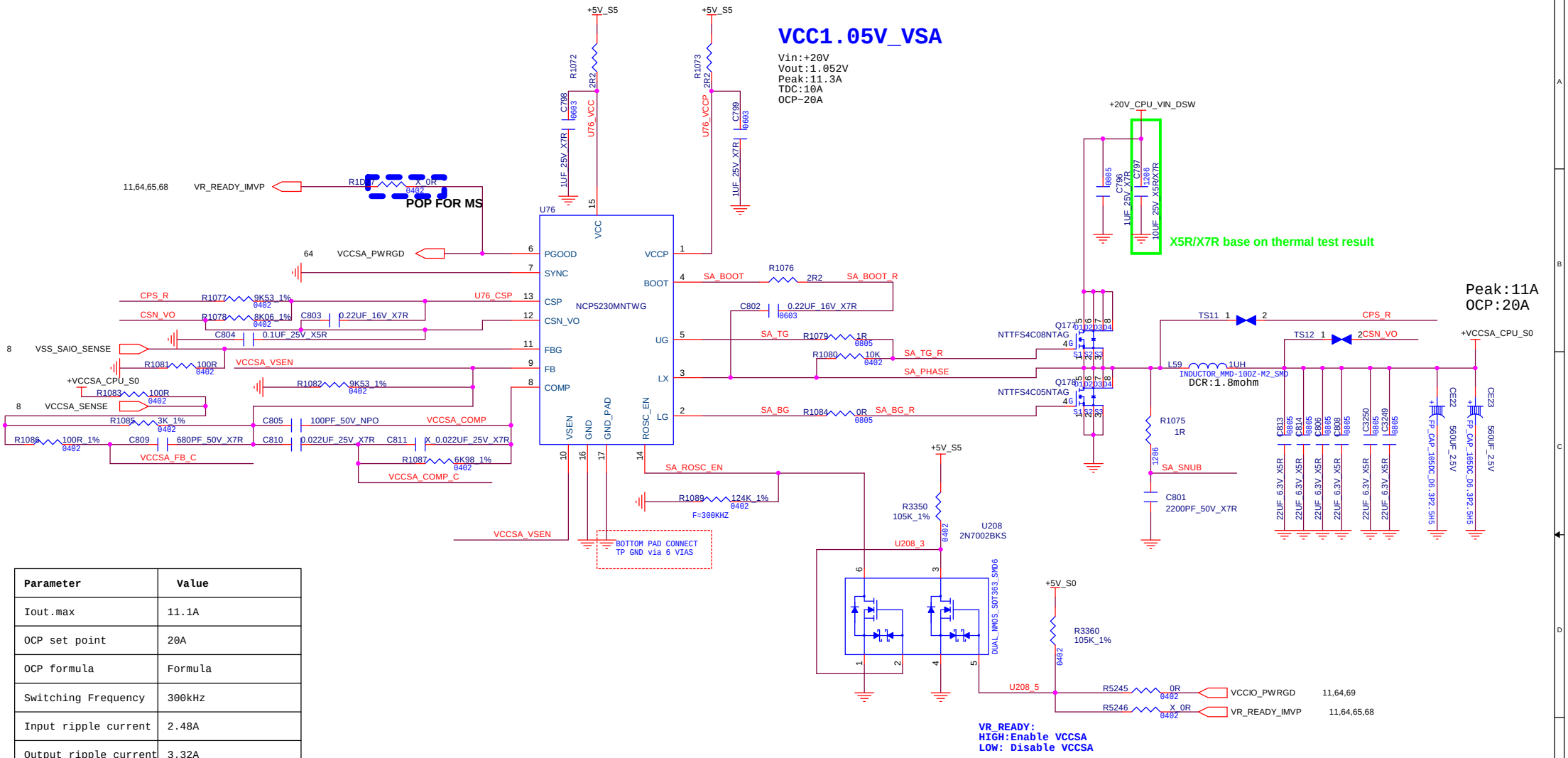




Parameter	Value
Iout.max	45A
OCP set point	77A
OCP formula	Formula
Switching Frequency	360kHz
Input ripple current	5.96A
Output ripple current	13.0A
Choke_size(L*W*H)(mm)	10.5*6.8*5.0
Choke_Isat	60
Choke_DCR	1.05mΩ
Choke_LIR	37.2%
CPU GT Load Line	3.1mΩ
Input capacitance	4.7UF_25V_X5R_0805*4 10UF_25V_X5R_1206*2
Output capacitance	560UF_2.5V*5 22UF_6.3V_X5R_0805*3

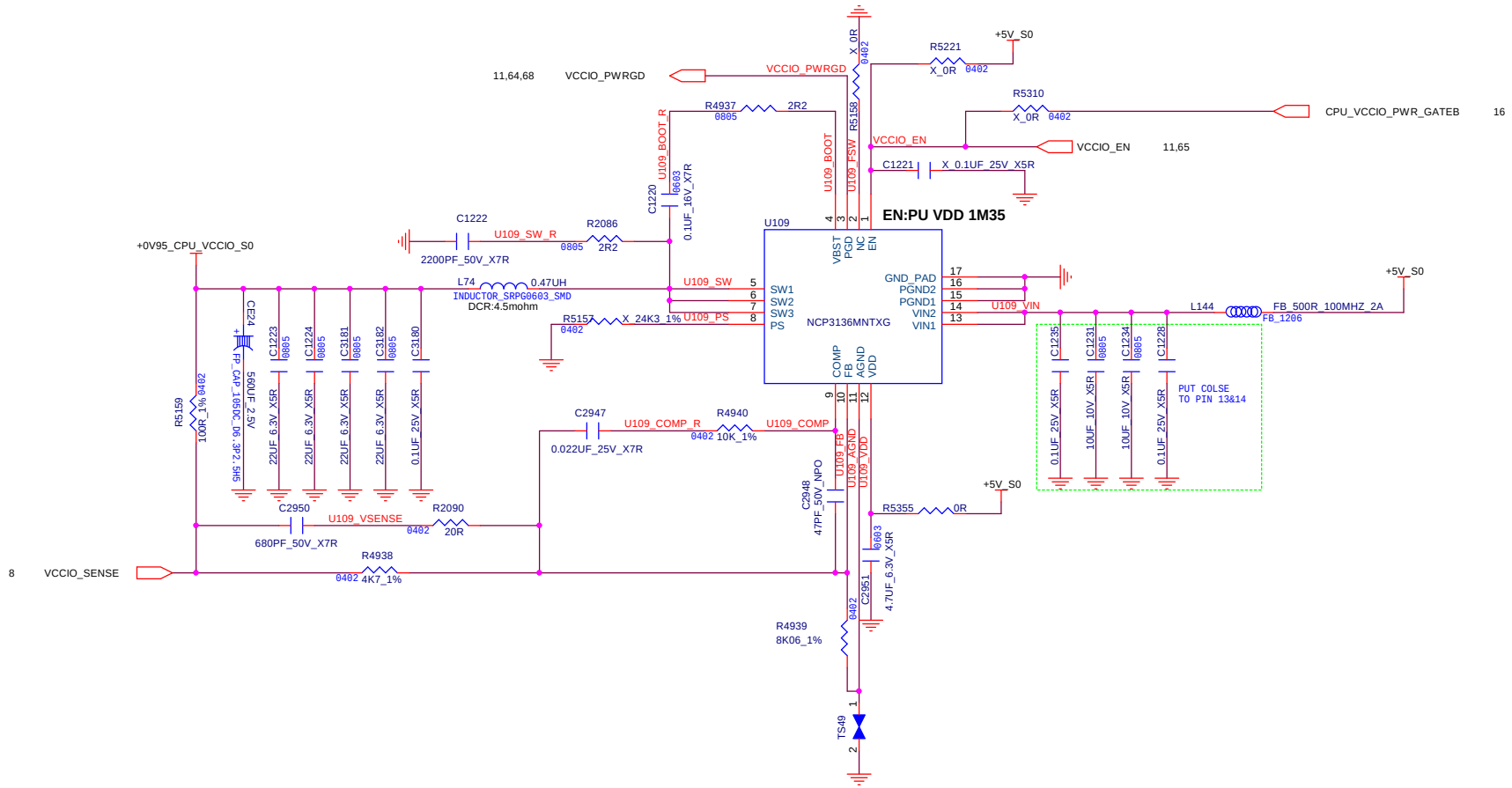
Universal Scientific Industrial Co., Ltd.

TITLE: M920z/M828z VCCGT OUTPUT DRIVE		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, July 10, 2018	PAGE: 67 of 99



Parameter	Value
Iout.max	11.1A
OCP set point	20A
OCP formula	Formula
Switching Frequency	300kHz
Input ripple current	2.48A
Output ripple current	3.32A
Choke_size(L*W*H)(mm)	11.5*10*4
Choke_Isat	27A
Choke_DCR	2.0mΩ
Choke_LIR	29.9%
Input capacitance	10UF_25V_X5R_1206*1
Output capacitance	560UF_2.5V*1 22UF_6.3V_X5R_0805*4

Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z VCCSA OUTPUT DRIVE	REV: V1.0
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Tuesday, July 10, 2018
PAGE: 68 of 99	



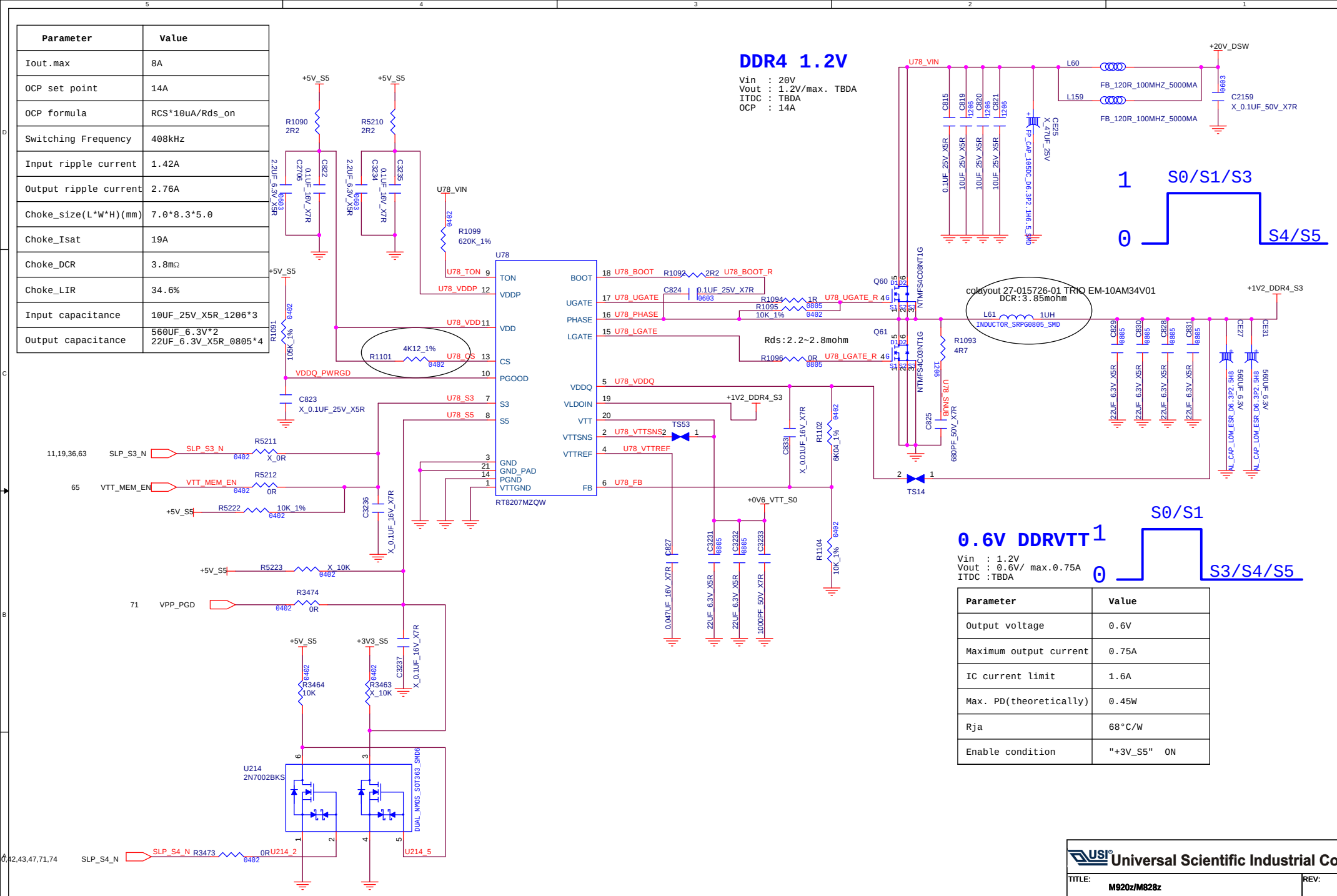
Parameter	Value
Iout.max	6.4A
OCP set point	7.6A
OCP formula	IC controlled
Switching Frequency	1.1MHz
Input ripple current	2.51A
Output ripple current	1.49A
Choke_size(L*W*H)(mm)	7.3*6.8*2.8
Choke_Isat	17.5A
Choke_DCR	4.50mΩ
Choke_LIR	23.3%
Input capacitance	10UF_10V_X5R_0805*2
Output capacitance	560UF_2.5V*1 22UF_6.3V_X5R_0805*4

Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z VCCIO			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, March 06, 2018		PAGE: 69 of 99

Parameter	Value
Iout.max	8A
OCP set point	14A
OCP formula	RCS*10uA/Rds_on
Switching Frequency	408kHz
Input ripple current	1.42A
Output ripple current	2.76A
Choke_size(L*W*H)(mm)	7.0*8.3*5.0
Choke_Isat	19A
Choke_DCR	3.8mΩ
Choke_LIR	34.6%
Input capacitance	10UF_25V_X5R_1206*3
Output capacitance	560UF_6.3V*2 22UF_6.3V_X5R_0805*4

DDR4 1.2V

Vin : 20V
Vout : 1.2V/max. TBDA
ITDC : TBDA
OCP : 14A



0.6V DDRVTT

Vin : 1.2V
Vout : 0.6V/ max.0.75A
ITDC :TBDA

1 S0/S1
0 S3/S4/S5

Parameter	Value
Output voltage	0.6V
Maximum output current	0.75A
IC current limit	1.6A
Max. PD(theoretically)	0.45W
Rja	68°C/W
Enable condition	"+3V_S5" ON

Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z System DDR4 VR	REV: V1.0
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Tuesday, March 06, 2018
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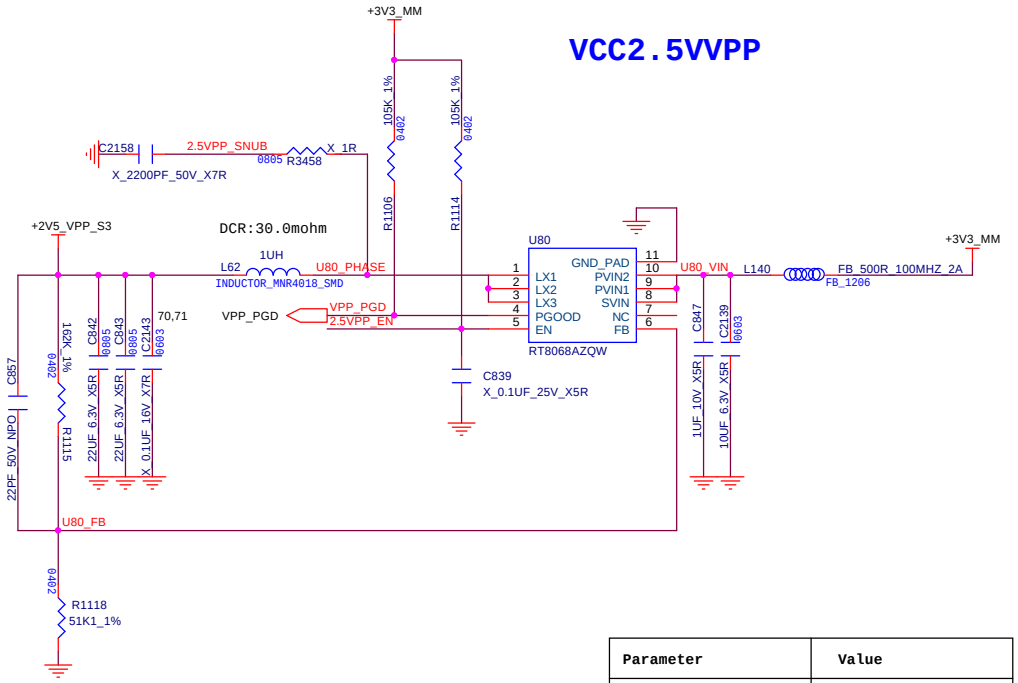
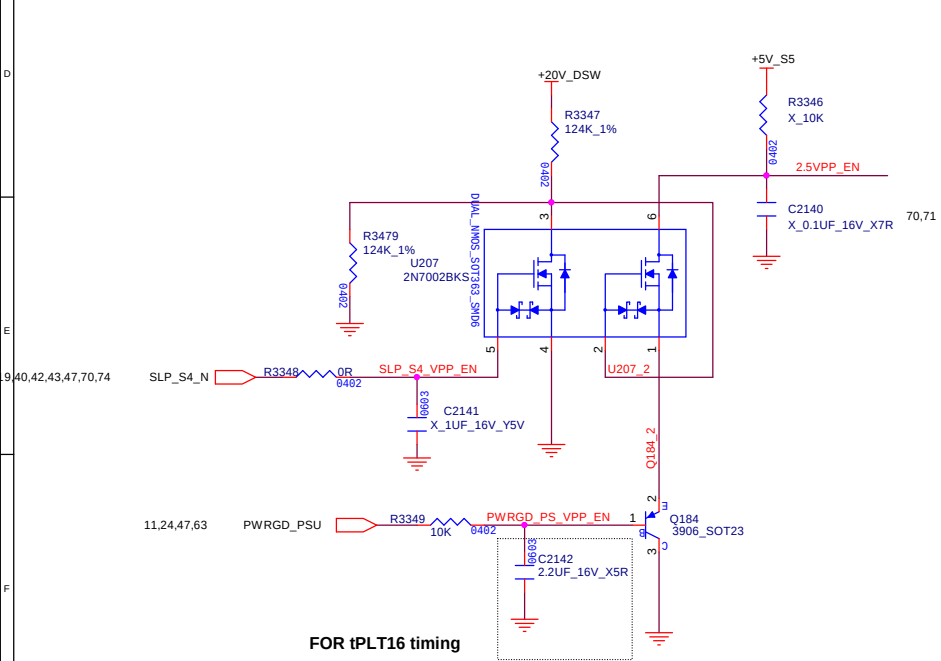
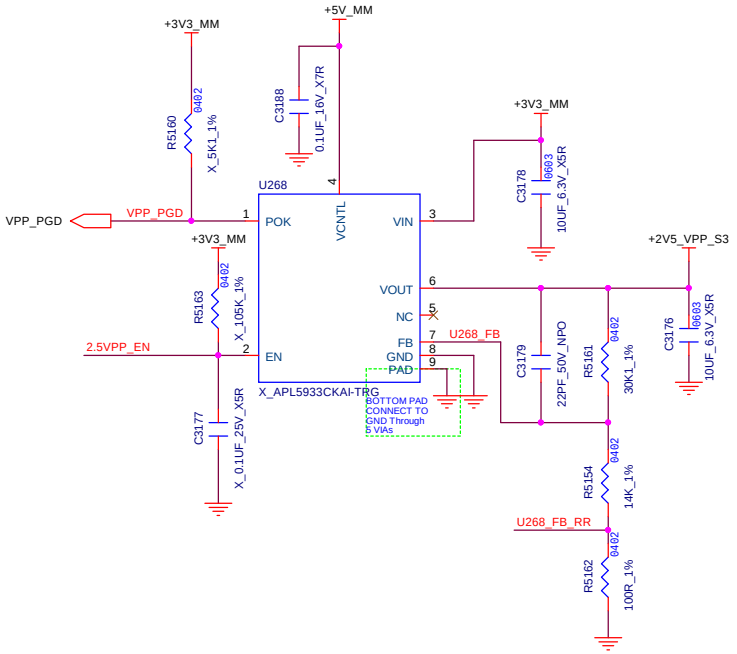
VCC2.5VPP



Parameter	Value
Iout.max	2.24A
OCP set point	4A
OCP formula	IC controlled
Switching Frequency	1MHz
Input ripple current	0.72A
Output ripple current	0.40A
Choke_size(L*W*H)(mm)	4.0*4.0*1.8
Choke_Isat	4.5A
Choke_DCR	30.00mΩ
Choke_LIR	27.1%
Input capacitance	10UF_6.3V_X5R_0603*1
Output capacitance	22UF_6.3V_X5R_0805*2





Universal Scientific Industrial Co., Ltd.		
TITLE: M920z/M828z VCC2.5V_VPP		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 71 of 99

Enable	Disable
EN1,EN2 > 1.4 V	EN1,EN2 < 0.4 V

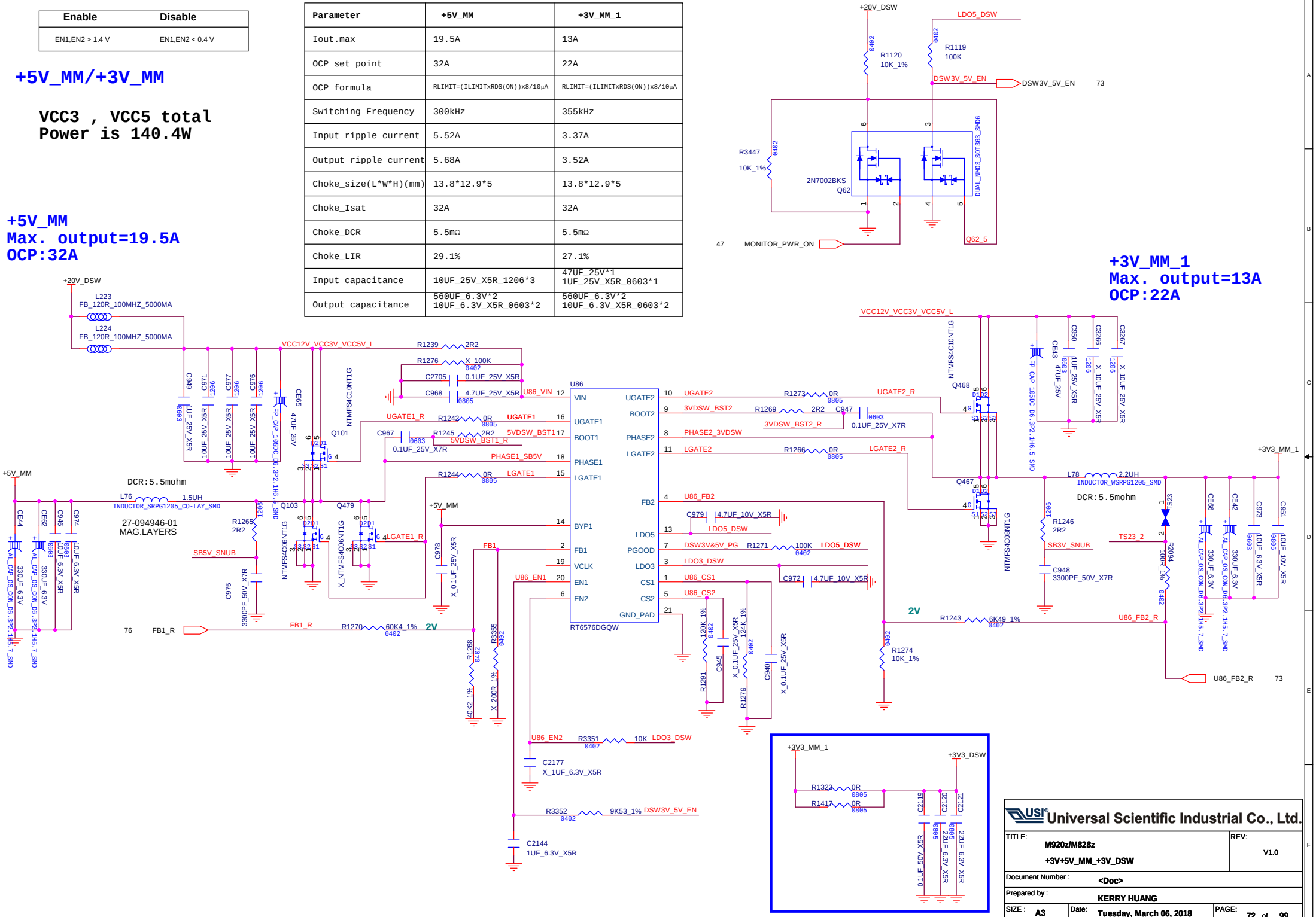
+5V_MM/+3V_MM

VCC3 , VCC5 total Power is 140.4W

Parameter	+5V_MM	+3V_MM_1
Iout.max	19.5A	13A
OCP set point	32A	22A
OCP formula	RLIMIT=(ILIMITxRDS(ON))x8/10μA	RLIMIT=(ILIMITxRDS(ON))x8/10μA
Switching Frequency	300kHz	355kHz
Input ripple current	5.52A	3.37A
Output ripple current	5.68A	3.52A
Choke_size(L*W*H)(mm)	13.8*12.9*5	13.8*12.9*5
Choke_Isat	32A	32A
Choke_DCR	5.5mΩ	5.5mΩ
Choke_LIR	29.1%	27.1%
Input capacitance	10UF_25V_X5R_1206*3	47UF_25V*1 1UF_25V_X5R_0603*1
Output capacitance	560UF_6.3V*2 10UF_6.3V_X5R_0603*2	560UF_6.3V*2 10UF_6.3V_X5R_0603*2

+5V_MM
Max. output=19.5A
OCP:32A

+3V_MM_1
Max. output=13A
OCP:22A



Universal Scientific Industrial Co., Ltd.	
TITLE: M920z/M828z +3V+5V_MM_+3V_DSW	REV: V1.0
Document Number : <Doc>	
Prepared by : KERRY HUANG	
SIZE : A3	Date: Tuesday, March 06, 2018
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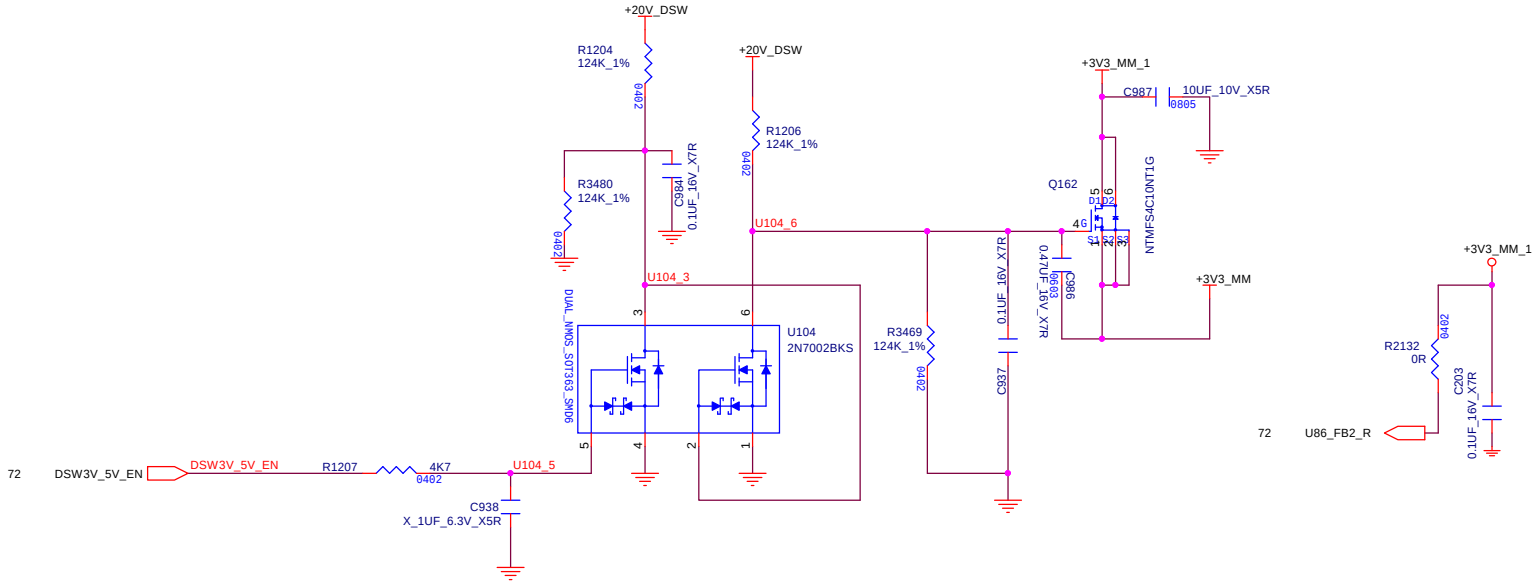
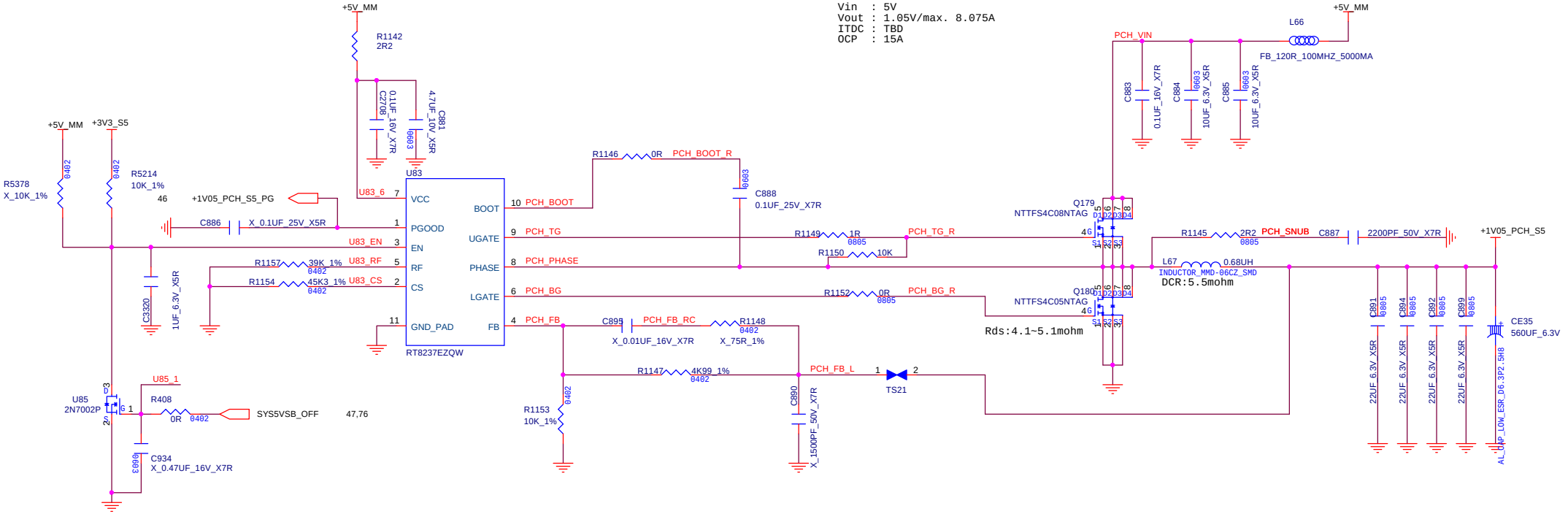
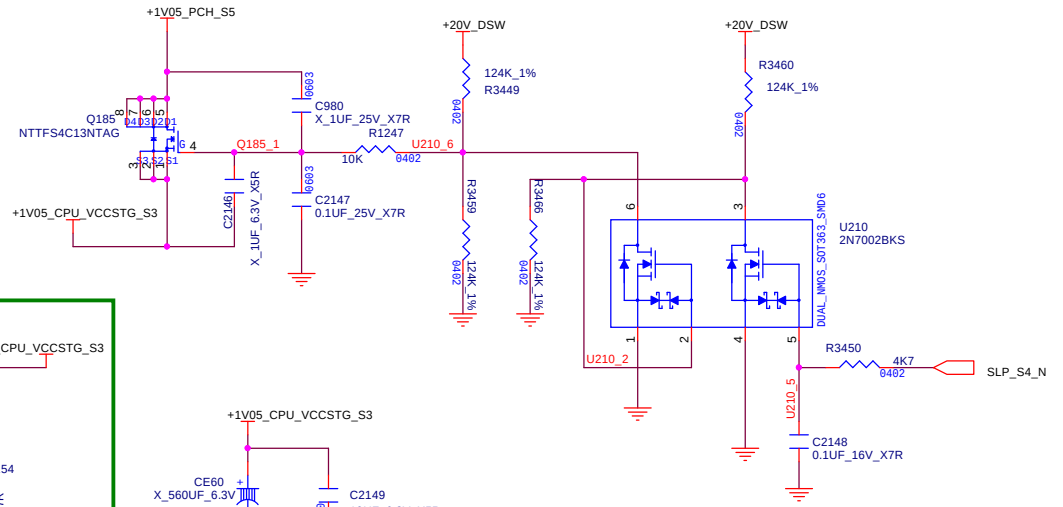


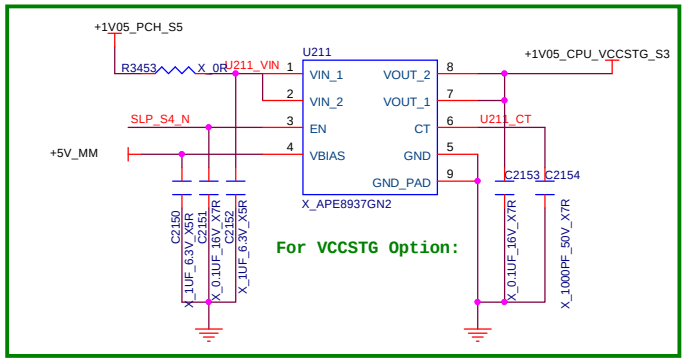
Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z +3V3_MM			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, March 06, 2018		PAGE: 73 of 99

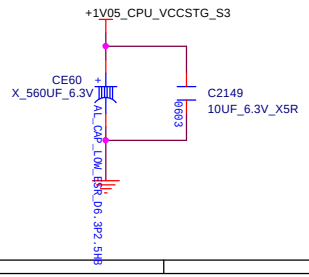
+1V05_PCH_S5

Vin : 5V
Vout : 1.05V/max. 8.075A
ITDC : TBD
OCP : 15A









Parameter	Value
Iout.max	8.075A
OCP set point	15A
OCP formula	Iocp=10uA*Rcs/(8*Rdson) +Iripple/2
Switching Frequency	430kHz
Input ripple current	3.29A
Output ripple current	2.83A
Choke_size(L*W*H)(mm)	7.2*6.7*3.0
Choke_Isat	25A
Choke_DCR	5.5mΩ
Choke_LIR	35.1%
Input capacitance	10UF_6.3V_X5R_0603*2
Output capacitance	560UF_2.5V*1 22UF_6.3V_X5R_0805*4

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TITLE: M920z/M828z V1P05_PCH			REV: V1.0
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TITLE: M920z/M828z BLANK		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
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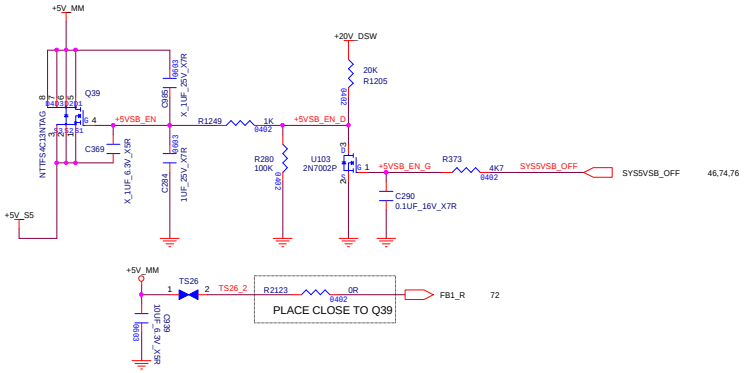
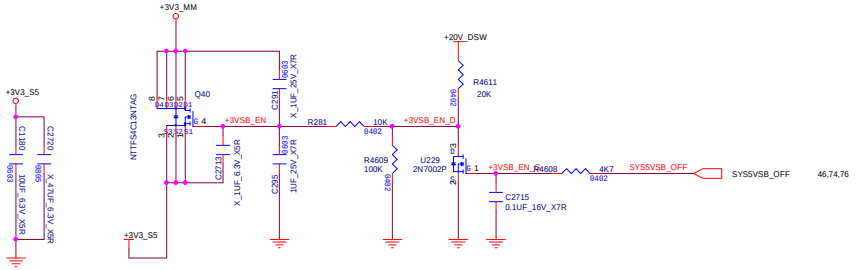
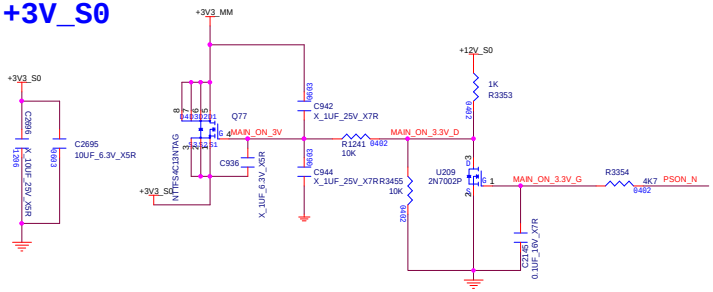
STAND BY POWER CONTROL





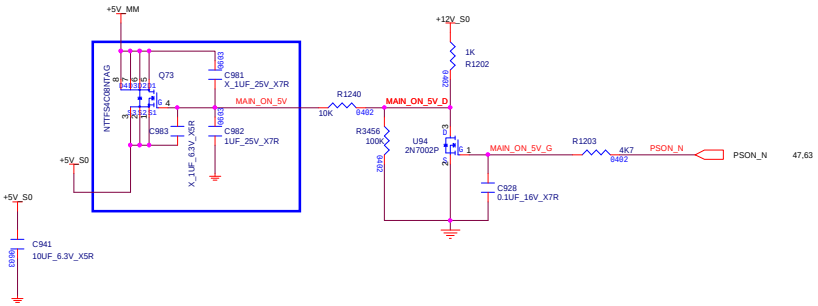
SYSTEM POWER CONTROL

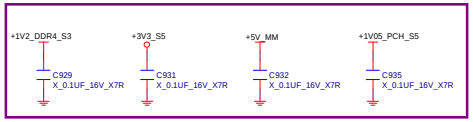
+3V_S0



+5V_S0

Layout:
Closed to JP32,L77,U13





For EMC

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TITLE: M920z/M828z VCC3/5V			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
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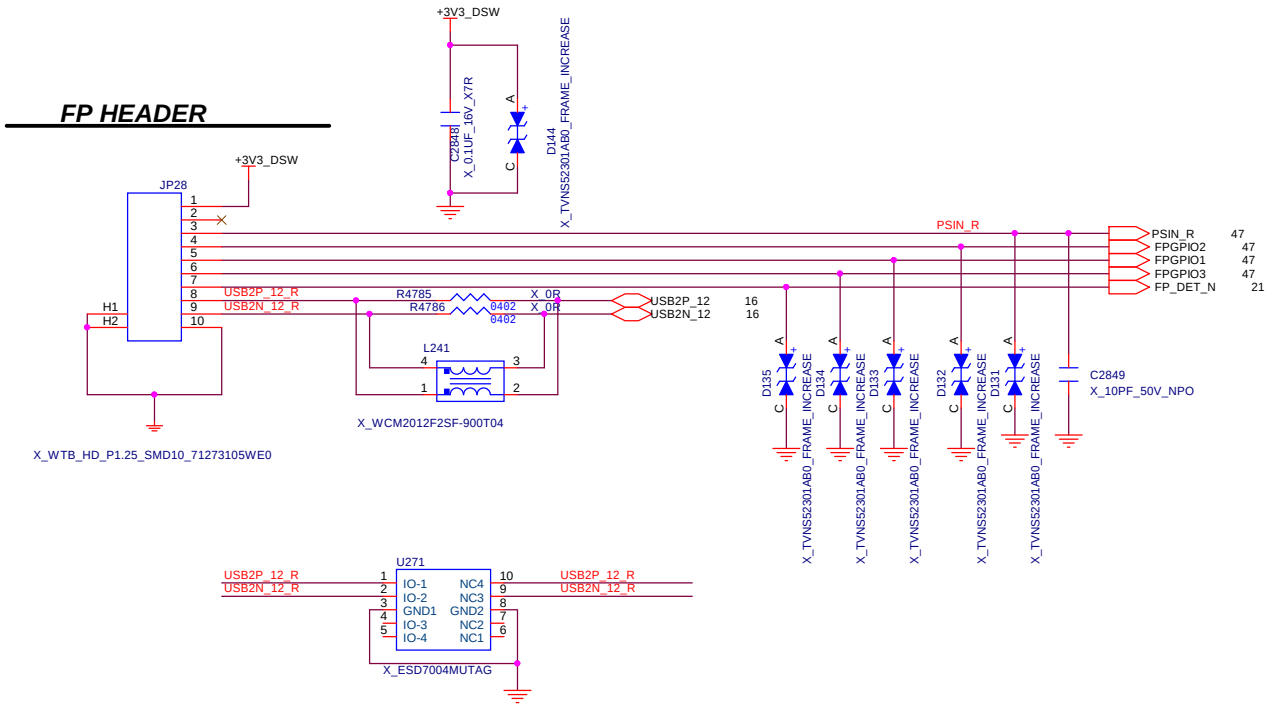

Universal Scientific Industrial Co., Ltd.		
TITLE: M920z/M828z FP HD_USB2.0 HD		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
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M920z : V
M828z : X

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
USB3.1# 1-GEN2	USB3.1# 2-GEN2	USB3.1# 3-GEN1	USB3.1# 4-GEN1	USB3.1# 5-GEN1	USB3.1# 6-GEN1	USB3.0# 7	USB3.0# 8	USB3.0# 9	USB3.0#10	PCIe #5	PCIe #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16	PCIe #17	PCIe #18	PCIe #19	PCIe #20
						PCIe #1	PCIe #2	PCIe #3	PCIe #4	GbE				GbE		SATA #0a	SATA #1a	SATA #0b	SATA #1b	SATA #2	SATA #3	SATA #4	SATA #5		
						X4				X4				X4				X4				X4			
						X2		X2		X2		X2		X2		X2		X2		X2		X2		X2	
						No Remapping								Intel PCIe Storage Device #1								Intel PCIe Storage Device #2			

27	28	29	30
PCIe #21	PCIe #22	PCIe #23	PCIe #24
X4			
X2		X2	
Intel PCIe Storage Device #3			

Flexible IO Assign

*B250: ONLY FLEX. IO 27~30 SUPPORT Optane

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TITLE: M920z/M828z Flexible IO		REV: V1.0
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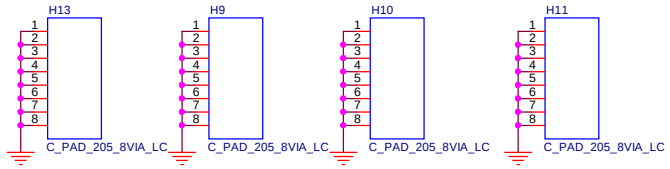
PCB SIZE: TOLERANCE +/-0.20 mm

HEAT PIPE SCREW HOLES

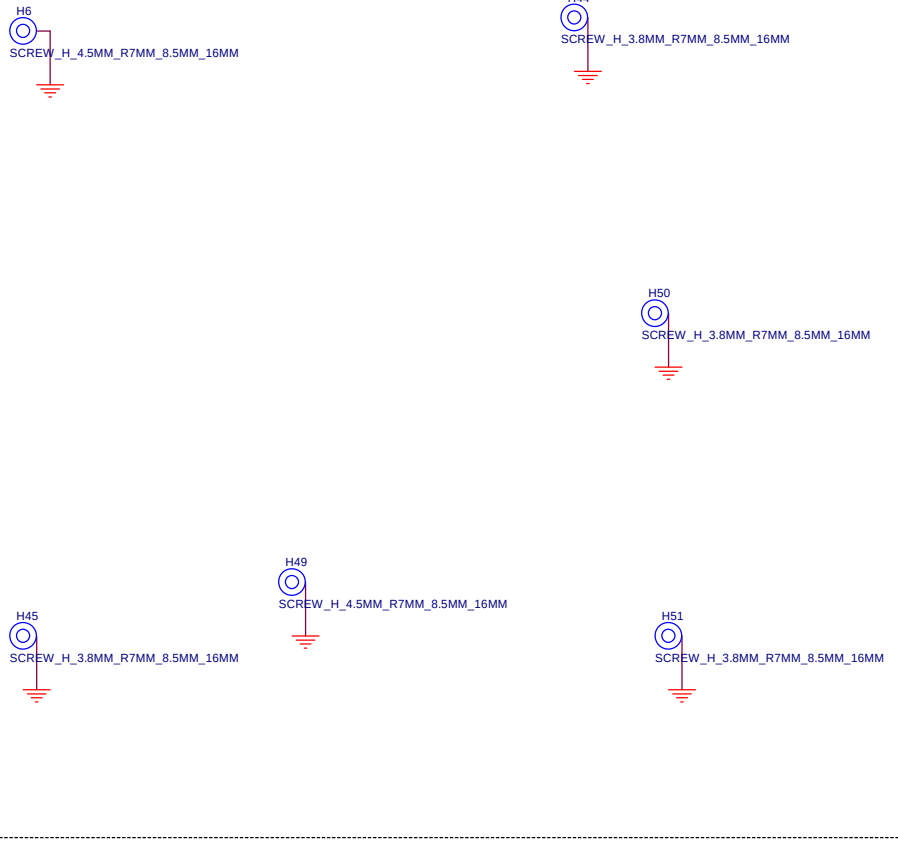


FOR CPU

CPU SOCKET

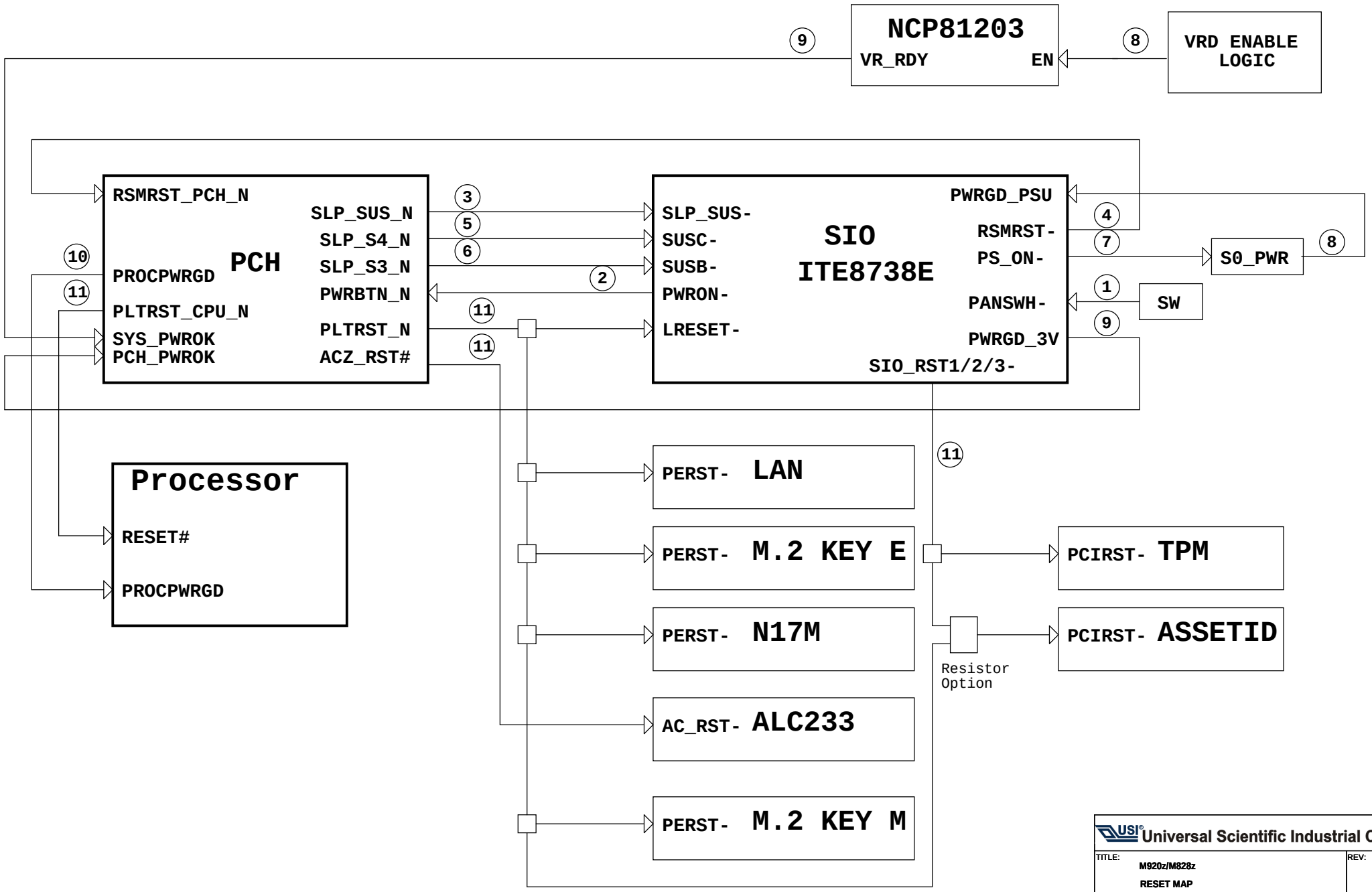
PCH Heatsink

SCREW HOLES



Universal Scientific Industrial Co., Ltd.			
TITLE: M920z/M828z HOLE_HEATSINK			REV: V1.0
Document Number : <Doc>			
Prepared by : KERRY HUANG			
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 79 of 99	

RESET MAP



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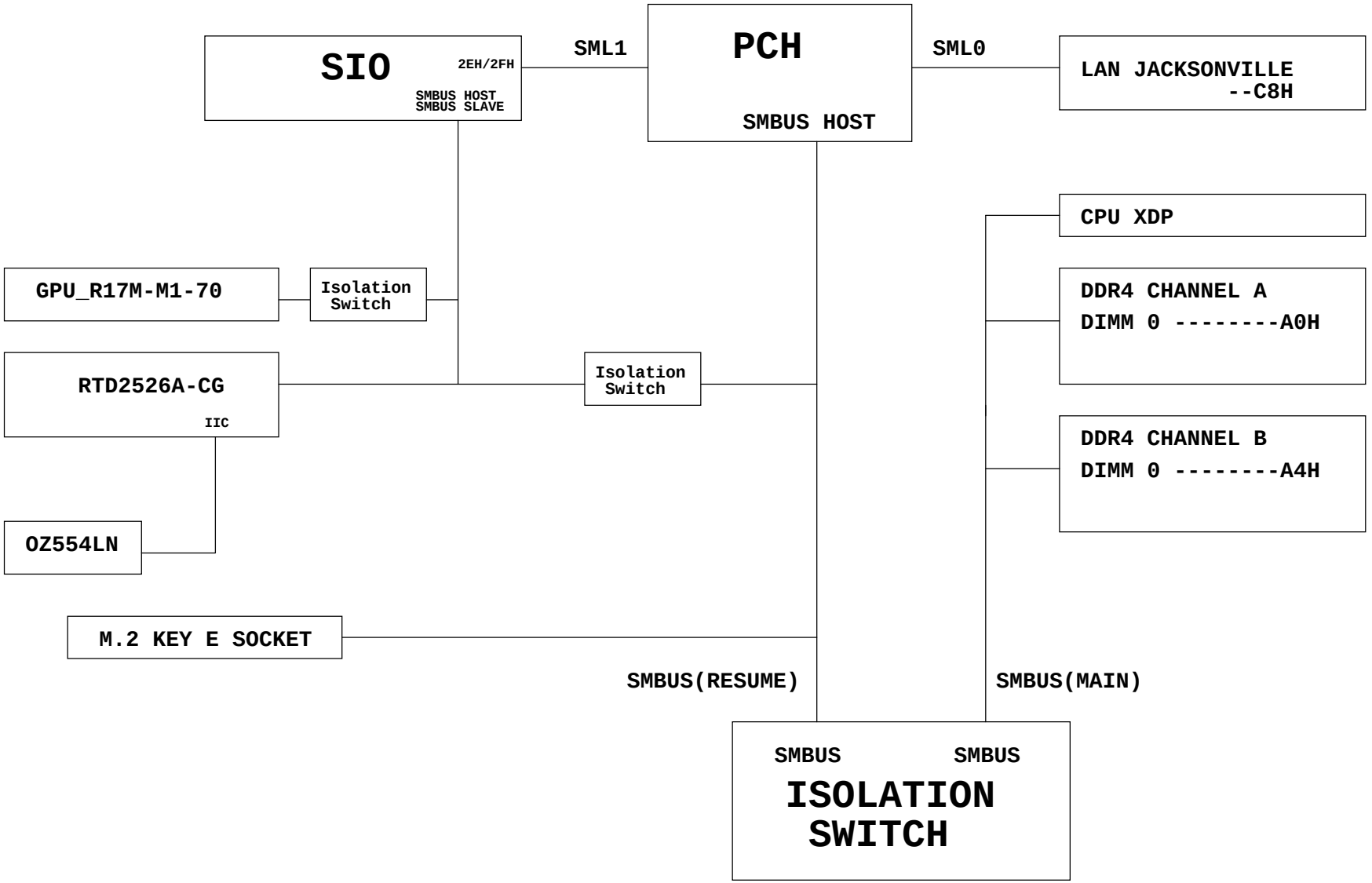
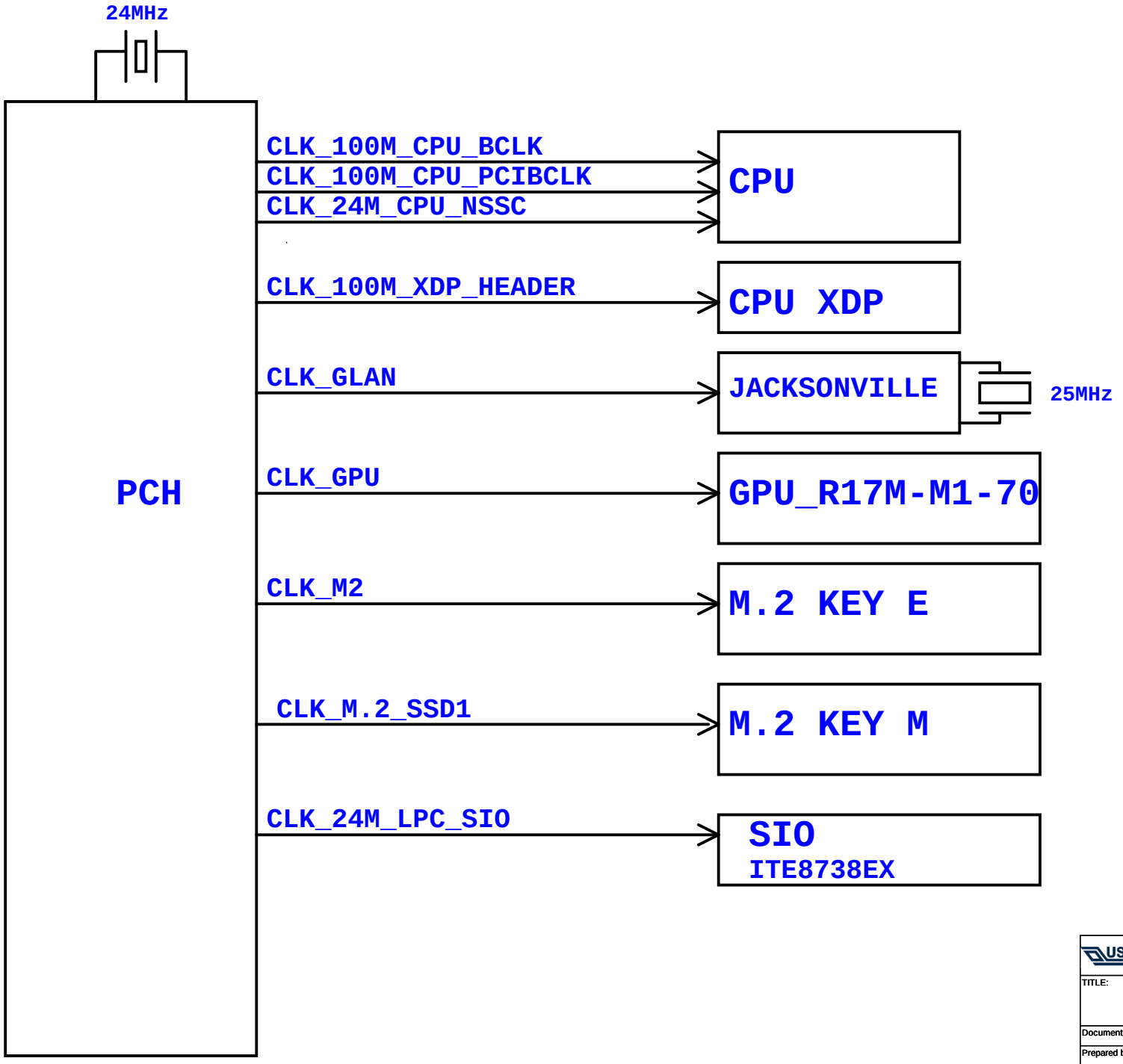
TITLE: M920z/M828z RESET MAP		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 80 of 99

SMBUS MAP



Universal Scientific Industrial Co., Ltd.		
TITLE: M920z/M828z SMBUS MAP		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 81 of 99

CLOCKS DIAGRAM



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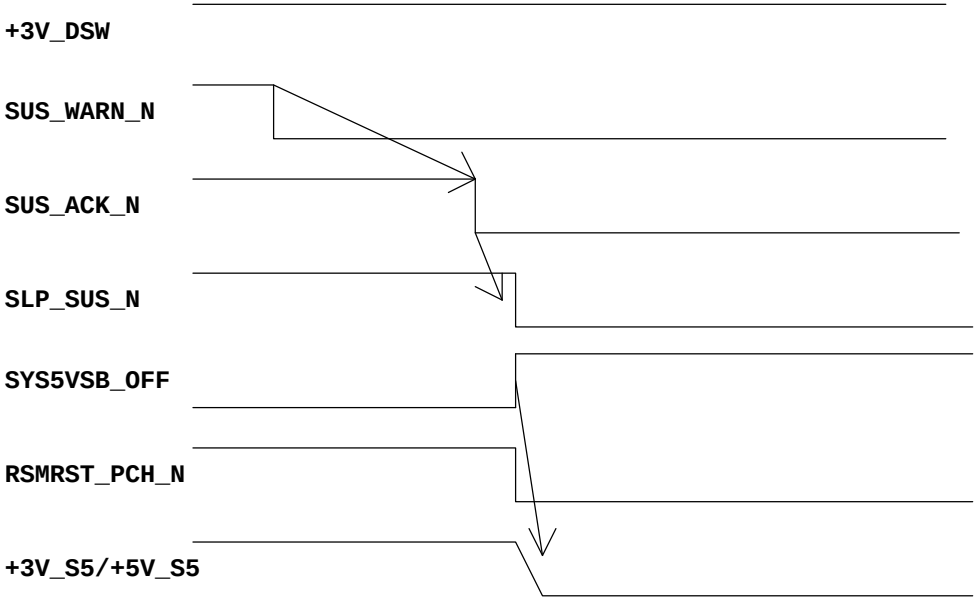
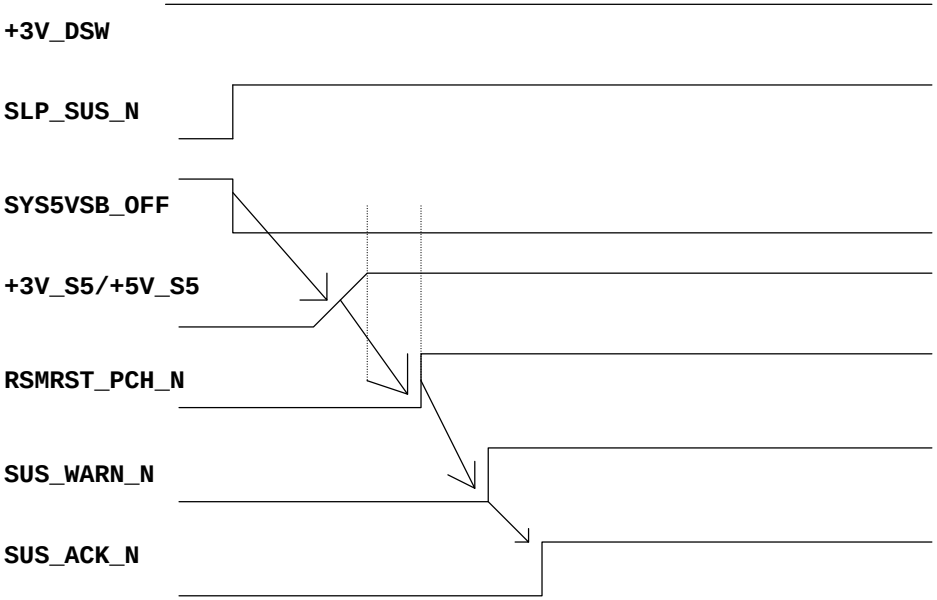
TITLE: M920z/M828z CLOCK DISTRIBUTION		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 82 of 99

Enter DSW State timing diagram



Exit DSW State timing diagram



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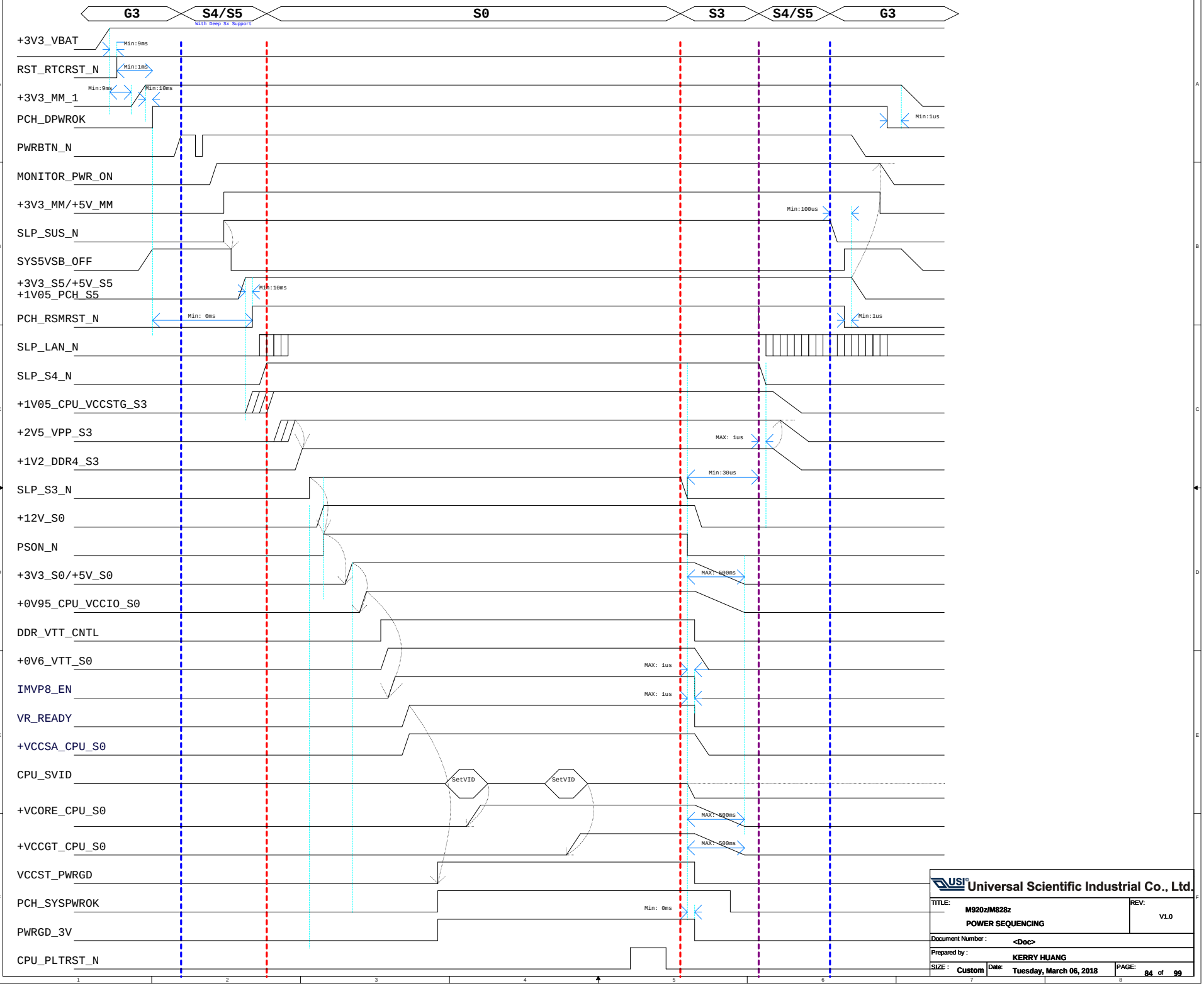
TITLE: M920z/M828z DSW SEQUENCING		REV: V1.0
Document Number : <Doc>		
Prepared by : KERRY HUANG		
SIZE : A3	Date: Tuesday, March 06, 2018	PAGE: 83 of 99



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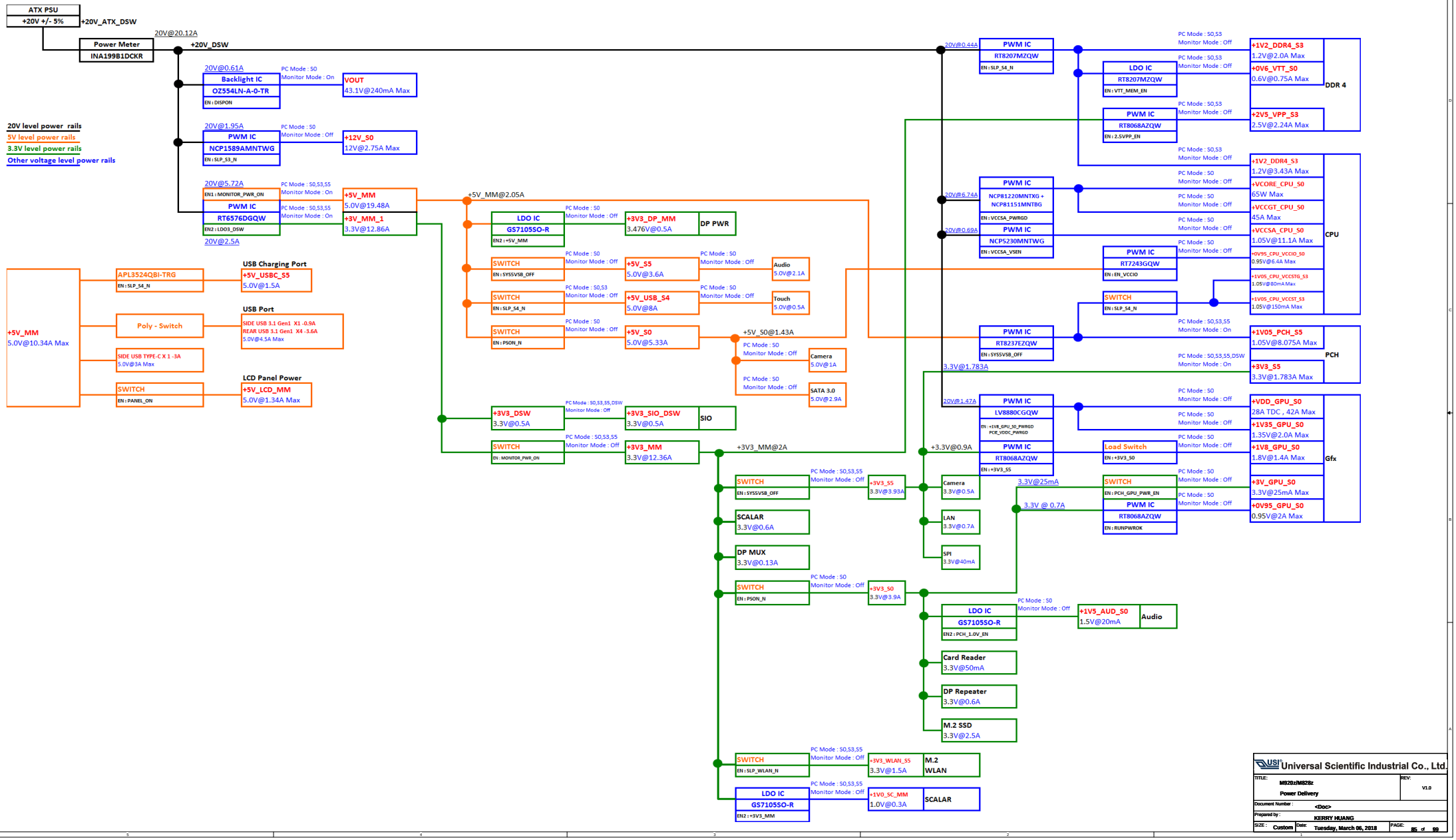
TITLE:	M920z/M828z POWER SEQUENCING	REV: V1.0
Document Number :	<Doc>	
Prepared by :	KERRY HUANG	
SIZE : Custom	Date: Tuesday, March 06, 2018	PAGE: 84 of 99


ATX PSU
+20V +/- 5%
+20V_ATX_DSW
Power Meter
INA199B1DCKR
20V@20.12A
+20V_DSW
20V level power rails
5V level power rails
3.3V level power rails
Other voltage level power rails
20V@0.61A
Backlight IC
OZ554LN-A-0-TR
EN : DISPON
PC Mode : S0
Monitor Mode : On
VOUT
43.1V@240mA Max
20V@1.95A
PWM IC
NCP1589AMNTWG
EN : SLP_S3_N
PC Mode : S0
Monitor Mode : Off
+12V_S0
12V@2.75A Max
20V@5.72A
EN1 : MONITOR_PWR_ON
PWM IC
RT6576DGQW
EN2 : LDO3_DSW
PC Mode : S0,S3,S5
Monitor Mode : On
PC Mode : S0,S3,S5
Monitor Mode : On
+5V_MM
5.0V@19.48A
+3V_MM_1
3.3V@12.86A
20V@2.5A
+5V_MM@2.05A
LDO IC
GS7105SO-R
EN2 : +5V_MM
PC Mode : S0
Monitor Mode : Off
+3V3_DP_MM
3.476V@0.5A
DP PWR
SWITCH
EN : SYSSVSB_OFF
+5V_S5
5.0V@3.6A
Audio
5.0V@2.1A
SWITCH
EN : SLP_S4_N
PC Mode : S0,S3
Monitor Mode : Off
+5V_USB_S4
5.0V@8A
Touch
5.0V@0.5A
SWITCH
EN : PSON_N
+5V_S0
5.0V@5.33A
+5V_S0@1.43A
Camera
5.0V@1A
SATA 3.0
5.0V@2.9A
+5V_MM
5.0V@10.34A Max
APL3524QBI-TRG
EN : SLP_S4_N
+5V_USBC_S5
5.0V@1.5A
USB Charging Port
Poly - Switch
SIDE USB 3.1 Gen1 X1 -0.9A
REAR USB 3.1 Gen1 X4 -3.6A
5.0V@4.5A Max
USB Port
SIDE USB TYPE-C X 1 -3A
5.0V@3A Max
SWITCH
EN : PANEL_ON
+5V_LCD_MM
5.0V@1.34A Max
LCD Panel Power
+3V3_DSW
3.3V@0.5A
PC Mode : S0,S3,S5,DSW
Monitor Mode : Off
+3V3_SIO_DSW
3.3V@0.5A
SIO
SWITCH
EN : MONITOR_PWR_ON
PC Mode : S0,S3,S5
Monitor Mode : Off
+3V3_MM
3.3V@12.36A
+3V3_MM@2A
SWITCH
EN : SYSSVSB_OFF
PC Mode : S0,S3,S5
Monitor Mode : Off
+3V3_S5
3.3V@3.93A
SCALAR
3.3V@0.6A
DP MUX
3.3V@0.13A
SWITCH
EN : PSON_N
PC Mode : S0
Monitor Mode : Off
+3V3_S0
3.3V@3.9A
SWITCH
EN : SLP_WLAN_N
PC Mode : S0,S3,S5
Monitor Mode : Off
+3V3_WLAN_S5
3.3V@1.5A
M.2
WLAN
LDO IC
GS7105SO-R
EN2 : +3V3_MM
PC Mode : S0,S3,S5
Monitor Mode : Off
+1V0_SC_MM
1.0V@0.3A
SCALAR
20V@0.44A
PWM IC
RT8207MZQW
EN : SLP_S4_N
LDO IC
RT8207MZQW
EN : VTT_MEM_EN
PC Mode : S0,S3
Monitor Mode : Off
+1V2_DDR4_S3
1.2V@2.0A Max
+0V6_VTT_S0
0.6V@0.75A Max
DDR 4
PWM IC
RT8068AZQW
EN : 2.5VPP_EN
+2V5_VPP_S3
2.5V@2.24A Max
20V@6.74A
PWM IC
NCP81220MNTXG +
NCP81151MNTBG
EN : VCCSA_PWRGD
20V@0.69A
PWM IC
NCP5230MNTWG
EN : VCCSA_VSEN
PC Mode : S0
Monitor Mode : Off
+1V2_DDR4_S3
1.2V@3.43A Max
+VCORE_CPU_S0
65W Max
+VCCGT_CPU_S0
45A Max
+VCCSA_CPU_S0
1.05V@11.1A Max
+0V95_CPU_VCCIO_S0
0.95V@6.4A Max
+1V05_CPU_VCCSTG_S3
1.05V@80mA Max
+1V05_CPU_VCCST_S3
1.05V@150mA Max
CPU
PWM IC
RT7243GQW
EN : EN_VCCIO
SWITCH
EN : SLP_S4_N
20V@1.47A
PWM IC
LV8880CGQW
EN : +1V8_GPU_S0_PWRGD
PCIE_VDDC_PWRGD
PWM IC
RT8068AZQW
EN : +3V3_S5
PC Mode : S0,S3,S5
Monitor Mode : On
+1V05_PCH_S5
1.05V@8.075A Max
PCH
PC Mode : S0,S3,S5,DSW
Monitor Mode : On
+3V3_S5
3.3V@1.783A Max
3.3V@1.783A
+3.3V@0.9A
PC Mode : S0
Monitor Mode : Off
+VDD_GPU_S0
28A TDC , 42A Max
+1V35_GPU_S0
1.35V@2.0A Max
+1V8_GPU_S0
1.8V@1.4A Max
+3V_GPU_S0
3.3V@25mA Max
+0V95_GPU_S0
0.95V@2A Max
Gfx
Load Switch
EN : +3V3_S0
SWITCH
EN : PCH_GPU_PWR_EN
PWM IC
RT8068AZQW
EN : RUNPWROK
3.3V@25mA
3.3V @ 0.7A
Camera
3.3V@0.5A
LAN
3.3V@0.7A
SPI
3.3V@40mA
LDO IC
GS7105SO-R
EN2 : PCH_1.0V_EN
PC Mode : S0
Monitor Mode : Off
+1V5_AUD_S0
1.5V@20mA
Audio
Card Reader
3.3V@50mA
DP Repeater
3.3V@0.6A
M.2 SSD
3.3V@2.5A
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TITLE:
M920z/M828z
Power Delivery
REV:
V1.0
Document Number :
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Prepared by :
KERRY HUANG
SIZE :
Custom
Date:
Tuesday, March 06, 2018
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Name	Power Rail	Internal Pull-Up/ Pull-	De-Glitch Input	De-Glitch Output	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Default	NMI or SMI Capable	M920 Usage
Group A GPIO - Primary Power Well (1.8V or 3.3V)													
GPP_A0	VCCPGPPA	None	No	Yes	RCIN#	in			ESPI_RESET#	out	Native F1/GP-In	None	KBRST_N
GPP_A1	VCCPGPPA	None	No	Yes	LAD0	inout			ESPI_IO0	inout	Native F1	None	LPC_AD0
GPP_A2	VCCPGPPA	None	No	Yes	LAD1	inout			ESPI_IO1	inout	Native F1	None	LPC_AD1
GPP_A3	VCCPGPPA	None	No	Yes	LAD2	inout			ESPI_IO2	inout	Native F1	None	LPC_AD2
GPP_A4	VCCPGPPA	None	No	Yes	LAD3	inout			ESPI_IO3	inout	Native F1	None	LPC_AD3
GPP_A5	VCCPGPPA	None	No	Yes	LFRAME#	out			ESPI_CS0#	out	Native F1	None	LPC_FRAME_N
GPP_A6	VCCPGPPA	None	No	Yes	SERIRQ	inout			ESPI_CS1#	out	Native F1	None	SER_IRQ
GPP_A7	VCCPGPPA	None	No	Yes	PIRQA#	iod			ESPI_ALERT0#	in	Native F1	None	LPC_DRQ0_N
GPP_A8	VCCPGPPA	None	No	Yes	CLKRUN#	iod					Native F1/ GP-In	None	LPC_CLKRUN_N (Unused)
GPP_A9	VCCPGPPA	None	No	Yes	CLKOUT_LPC0	out			ESPI_CLK	out	Native F1	None	CLK_24M_LPC_SIO
GPP_A10	VCCPGPPA	None	No	Yes	CLKOUT_LPC1	out					Native F1/ GP-In	None	(No Use)
GPP_A11	VCCPGPPA	None	No	Yes	PME#	iod	SD_VDD2_P-WR_EN#	out			Native F1/ GP-In	None	SIO_PME_N
GPP_A12	VCCPGPPA	None	No	Yes	BM_BUSY#	in	ISH_GP6	inout	SX_EX-IT_HOLDOF F#	in	GP-In	None	(No Use)
GPP_A13	VCCPGPPA	None	No	Yes	SUSWARN# / SUSPWRDNA CK	out					Native F1/GP-In	None	SUS_WARN_N
GPP_A14	VCCPGPPA	None	No	Yes	SUS_STAT#	out			ESPI_RESE T#	out	Native F1	None	LPCPD_N
GPP_A15	VCCPGPPA	None	No	Yes	SUSACK#	in					Native F1	None	SUS_ACK_N
GPP_A16	VCCPGPPA	None	No	Yes	CLKOUT_48	out					Native F1/ GP-In	None	(No Use)
GPP_A17	VCCPGPPA	None	No	Yes	SD_VDD1_P WR_EN#	out	ISH_GP7	inout			GP-Out	None	M.2_DISABLE1_N
GPP_A18	VCCPGPPA	None	No	Yes	ISH_GP0	inout					GP-In	None	(No Use)
GPP_A19	VCCPGPPA	None	No	Yes	ISH_GP1	inout					GP-In	None	(No Use)
GPP_A20	VCCPGPPA	None	No	Yes	ISH_GP2	inout					GP-In	None	IOBOX_DET_N
GPP_A21	VCCPGPPA	None	No	Yes	ISH_GP3	inout					GP-In	None	M.2_DISABLE2_N
GPP_A22	VCCPGPPA	None	No	Yes	ISH_GP4	inout					GP-In	None	COM_PORT_DET_N
GPP_A23	VCCPGPPA	None	No	Yes	ISH_GP5	inout					GP-In	None	(No Use)

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TITLE: M920z/M828z CNL-PCH GPIO Table 1		REV: V1.0
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Group B GPIO - Primary Power Well (1.8V or 3.3V)														
GPP_B0	VCCPGPPBC	None	No	Yes	GSPI0_CS1#	out					GP-Out	None	SMBUS_ISP
GPP_B1	VCCPGPPBC	None	No	Yes	GSPI1_CS1#	out	TIME_SYNC1	inout			GP-In	None	(No Use)
GPP_B2	VCCPGPPBC	None	No	Yes	VRALERT#	in					GP-In	None	(No Use)
GPP_B3	VCCPGPPBC	None	No	Yes	CPU_GP2	in					GP-In	None	(No Use)
GPP_B4	VCCPGPPBC	None	No	Yes	CPU_GP3	in					GP-In	None	(No Use)
GPP_B5	VCCPGPPBC	None	No	Yes	SRCCLKREQ0#	iod					GP-In	None	GPU_CLKREQ_N
GPP_B6	VCCPGPPBC	None	No	Yes	SRCCLKREQ1#	iod					GP-In	None	(No Use)
GPP_B7	VCCPGPPBC	None	No	Yes	SRCCLKREQ2#	iod					GP-In	None	(No Use)
GPP_B8	VCCPGPPBC	None	No	Yes	SRCCLKREQ3#	iod					GP-In	None	(No Use)
GPP_B9	VCCPGPPBC	None	No	Yes	SRCCLKREQ4#	iod					GP-In	None	M.2_SSD1_CLKREQ_N
GPP_B10	VCCPGPPBC	None	No	Yes	SRCCLKREQ5#	iod					GP-In	None	(No Use)
GPP_B11	VCCPGPPBC	None	No	Yes	I2S_MCLK	out					GP-In	None	(No Use)
GPP_B12	VCCPGPPBC	None	No	Yes	SLP_S0#	out					Native F1	None	SLP_S0_N
GPP_B13	VCCPGPPBC	None	No	Yes	PLTRST#	out					Native F1	None	PLTRST_N
GPP_B14	VCCPGPPBC	20K_PD	No	No	SPKR	out					GP-Out	NMI SMI	SPKR_PCH (STRAP)
GPP_B15	VCCPGPPBC	None	No	Yes	GSPI0_CS0#	out					GP-In	None	(No Use)
GPP_B16	VCCPGPPBC	None	No	Yes	GSPI0_CLK	out					GP-In	None	(No Use)
GPP_B17	VCCPGPPBC	None	No	Yes	GSPI0_MISO	in					GP-In	None	(No Use)
GPP_B18	VCCPGPPBC	20K_PD	No	No	GSPI0_MOSI	out					GP-Out	None	PU_PCH_GPP_B_18_NO_BOOT (STRAP)
GPP_B19	VCCPGPPBC	None	No	Yes	GSPI1_CS#	out					GP-In	None	(No Use)
GPP_B20	VCCPGPPBC	None	No	Yes	GSPI1_CLK	out					GP-In	NMI SMI	(No Use)
GPP_B21	VCCPGPPBC	None	No	Yes	GSPI1_MISO	in					GP-In	None	(No Use)
GPP_B22	VCCPGPPBC	20K_PD	No	No	GSPI1_MOSI	out					GP-Out	None	FM_PCH_BBS_STRAP (STRAP)
GPP_B23	VCCPGPPBC	20K_PD	Yes	No	SML1ALERT#	iod	PCHHOT#	od			GP-Out	NMI SMI	SMLINK1_ALERT_N (STRAP)

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Group C GPIO - Primary Power Well (1.8V or 3.3V)														
GPP_C0	VCCPGPPBC	None	Yes	Yes	SMBCLK	iod					Native F1	None	SMB_CLK_STBY_R	
GPP_C1	VCCPGPPBC	None	Yes	Yes	SMBDATA	iod					Native F1	None	SMB_DATA_STBY_R	
GPP_C2	VCCPGPPBC	20K_PD	Yes	No	SMBALERT#	iod					GP-Out	None	FM_PCH_TLS_STRAP (STRAP)	GPO-HIGH
GPP_C3	VCCPGPPBC	None	Yes	Yes	SML0CLK	iod					Native F1	None	SMLINK0_CLK	
GPP_C4	VCCPGPPBC	None	Yes	Yes	SML0DATA	iod					Native F1	None	SMLINK0_DATA	
GPP_C5	VCCPGPPBC	20K_PD	Yes	No	SML0ALERT#	iod					GP-Out	None	SMLINK0_ALERT_N (STRAP)	GPO-HIGH
GPP_C6	VCCPGPPBC	None	Yes	Yes	SML1CLK	iod					GP-In	None	SMLINK1_CLK	
GPP_C7	VCCPGPPBC	None	Yes	Yes	SML1DATA	iod					GP-In	None	SMLINK1_DATA	
GPP_C8	VCCPGPPBC	None	No	Yes	UART0_RXD	in					GP-In	None	CLEAR_CMOS_N	
GPP_C9	VCCPGPPBC	None	No	Yes	UART0_TXD	out					GP-In	None	(No Use)	
GPP_C10	VCCPGPPBC	None	No	Yes	UART0_RTS#	out					GP-In	None	(No Use)	
GPP_C11	VCCPGPPBC	None	No	Yes	UART0_CTS#	in					GP-In	None	(No Use)	
GPP_C12	VCCPGPPBC	None	No	Yes	UART1_RXD	in	ISH_UART1_RXD	in			GP-In	None	(No Use)	
GPP_C13	VCCPGPPBC	None	No	Yes	UART1_TXD	out	ISH_UART1_TXD	out			GP-In	None	(No Use)	
GPP_C14	VCCPGPPBC	None	No	Yes	UART1_RTS#	out	ISH_UART1_RTS#	out			GP-In	None	(No Use)	
GPP_C15	VCCPGPPBC	None	No	Yes	UART1_CTS#	in	ISH_UART1_CTS#	in			GP-In	None	(No Use)	
GPP_C16	VCCPGPPBC	None	Yes	Yes	I2C0_SDA	iod					GP-In	None	(No Use)	
GPP_C17	VCCPGPPBC	None	Yes	Yes	I2C0_SCL	iod					GP-In	None	(No Use)	
GPP_C18	VCCPGPPBC	None	Yes	Yes	I2C1_SDA	iod					GP-In	None	WOR_N	
GPP_C19	VCCPGPPBC	None	Yes	Yes	I2C1_SCL	iod					GP-In	None	(No Use)	
GPP_C20	VCCPGPPBC	None	No	Yes	UART2_RXD	in					GP-In	None	(No Use)	
GPP_C21	VCCPGPPBC	None	No	Yes	UART2_TXD	out					GP-In	None	(No Use)	
GPP_C22	VCCPGPPBC	None	No	Yes	UART2_RTS#	out					GP-In	NMI SMI	(No Use)	
GPP_C23	VCCPGPPBC	None	No	Yes	UART2_CTS#	in					GP-In	NMI SMI	(No Use)	

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Group D GPIO in Primary Power Well (1.8V or 3.3V) -use 1.8V													
GPP_D0	VCCPGPPD	None	No	Yes	SPI1_CS#						GP-In	NMI SMI	(No Use)
GPP_D1	VCCPGPPD	None	No	Yes	SPI1_CLK						GP-In	NMI SMI	(No Use)
GPP_D2	VCCPGPPD	None	No	Yes	SPI1_MISO						GP-In	NMI SMI	(No Use)
GPP_D3	VCCPGPPD	None	No	Yes	SPI1_MOSI						GP-In	NMI SMI	(No Use)
GPP_D4	VCCPGPPD	None	Yes	Yes	ISH_I2C2_SDA		I2C3_SDA	iod			GP-In	NMI SMI	(No Use)
GPP_D5	VCCPGPPD	None	No	Yes	I2S2_SFRM	inout	CNV_RF_RESET#	out			Native F3	None	CNV_RF_RESET#
GPP_D6	VCCPGPPD	None	No	Yes	I2S2_TXD	out	MODEM_-CLKREQ	out			Native F3	None	MODEM_-CLKREQ
GPP_D7	VCCPGPPD	None	No	Yes	I2S2_RXD	in					GP-In	None	(No Use)
GPP_D8	VCCPGPPD	None	No	Yes	I2S2_SCLK	inout					GP-In	None	(No Use)
GPP_D9	VCCPGPPD	None	No	Yes	ISH_SPI_CS#	out					GP-In	None	(No Use)
GPP_D10	VCCPGPPD	None	No	Yes	ISH_SPI_CLK	out					GP-In	None	(No Use)
GPP_D11	VCCPGPPD	None	No	Yes	ISH_SPI_MISO	in	GP_BSSB_CLK	in			Native F2	None	(No Use)
GPP_D12	VCCPGPPD	None	No	Yes	ISH_SPI_MOSI	out	GP_BSSB_D	in			Native F2	None	(No Use)
GPP_D13	VCCPGPPD	None	No	Yes	ISH_UART0_RXD	in					GP-In	None	(No Use)
GPP_D14	VCCPGPPD	None	No	Yes	ISH_UART0_TXD	out					GP-In	None	(No Use)
GPP_D15	VCCPGPPD	None	No	Yes	ISH_UART0_RTS#	out	GSPI2_CS1#	out			GP-In	None	(No Use)
GPP_D16	VCCPGPPD	None	No	Yes	ISH_UART0_CTS#	in					GP-In	None	(No Use)
GPP_D17	VCCPGPPD	None	No	Yes	DMIC_CLK1	out	SNDW3_CLK	inout			GP-In	None	(No Use)
GPP_D18	VCCPGPPD	None	No	Yes	DMIC_DATA1	in	SNDW3_DATA	inout			GP-In	None	(No Use)
GPP_D19	VCCPGPPD	None	No	Yes	DMIC_CLK0	out	SNDW4_CLK	inout			GP-In	None	(No Use)
GPP_D20	VCCPGPPD	None	No	Yes	DMIC_DATA0	in	SNDW4_DATA	inout			GP-In	None	(No Use)
GPP_D21	VCCPGPPD	None	No	Yes	SPI1_IO2	inout					GP-In	None	(No Use)
GPP_D22	VCCPGPPD	None	No	Yes	SPI1_IO3	inout					GP-In	None	(No Use)
GPP_D23	VCCPGPPD	None	Yes	Yes	ISH_I2C2_SCL	iod	I2C3_SCL	iod			GP-In	None	(No Use)

Group E GPIO - Primary Power Well (1.8V or 3.3V)													
GPP_E0	VCCPGPPEF	None	No	Yes	SATAXPCIE0	in	SATAGP0	in			Native F1/ GP-In	NMI SMI	(No Use)
GPP_E1	VCCPGPPEF	None	No	Yes	SATAXPCIE1	in	SATAGP1	in			Native F1/ GP-In	NMI SMI	(No Use)
GPP_E2	VCCPGPPEF	None	No	Yes	SATAXPCIE2	in	SATAGP2	in			Native F1/ GP-In	NMI SMI	(No Use)
GPP_E3	VCCPGPPEF	None	No	Yes	CPU_GP0	in					GP-In	NMI SMI	(No Use)
GPP_E4	VCCPGPPEF	None	No	Yes	SATA_DEVSLP0	od					GP-In	NMI SMI	CARD_READER_DET
GPP_E5	VCCPGPPEF	None	No	Yes	SATA_DEVSLP1	od					GP-In	NMI SMI	CAMERA_DET
GPP_E6	VCCPGPPEF	None	No	Yes	SATA_DEVSLP2	od					GP-In	NMI SMI	MULTI_TOUCH_DET
GPP_E7	VCCPGPPEF	None	No	Yes	CPU_GP1	in					GP-In	NMI SMI	(No Use)
GPP_E8	VCCPGPPEF	None	No	Yes	SATA_LED#	od					GP-In	NMI SMI	PCH_SATA_LED_N
GPP_E9	VCCPGPPEF	20K_PD	No	Yes	USB_OC0#	in					GP-In	None	USB30_OCP#1
GPP_E10	VCCPGPPEF	20K_PD	No	Yes	USB_OC1#	in					GP-In	None	USB30_OCP#2
GPP_E11	VCCPGPPEF	20K_PD	No	Yes	USB_OC2#	in					GP-In	None	USB30_OCP#34
GPP_E12	VCCPGPPEF	20K_PD	No	Yes	USB_OC3#	in					GP-In	None	USB30_OCP#56

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Group F GPIO - Primary Power Well (1.8V or 3.3V)													
GPP_F0	VCCPGPPEF	None	No	Yes	SATAXPCIE3	in	SATAGP3				Native F1/ GP-In	None	(No Use)
GPP_F1	VCCPGPPEF	None	No	Yes	SATAXPCIE4	in	SATAGP4				Native F1/ GP-In	None	(No Use)
GPP_F2	VCCPGPPEF	None	No	Yes	SATAXPCIE5	in	SATAGP5				Native F1/ GP-In	None	(No Use)
GPP_F3	VCCPGPPEF	None	No	Yes	SATAXPCIE6	in	SATAGP6				Native F1/ GP-In	None	(No Use)
GPP_F4	VCCPGPPEF	None	No	Yes	SATAXPCIE7	in	SATAGP7				Native F1/ GP-In	None	(No Use)
GPP_F5	VCCPGPPEF	None	No	Yes	SATA_DEVSLP3	od					GP-In	None	FP_DET_N
GPP_F6	VCCPGPPEF	None	No	Yes	SATA_DEVSLP4	od					GP-In	None	SSD1_SATA_DEVSLP
GPP_F7	VCCPGPPEF	None	No	Yes	SATA_DEVSLP5	od					GP-In	None	(No Use)
GPP_F8	VCCPGPPEF	None	No	Yes	SATA_DEVSLP6	od					GP-Out	None	PCH_GPU_PWR_EN
GPP_F9	VCCPGPPEF	None	No	Yes	SATA_DEVSLP7	od					GP-In	None	PCH_GPU_PWR_GD
GPP_F10	VCCPGPPEF	None	No	Yes	SATA_SCLOCK	od					GP-In	None	PCH_CONFIG_JUMPER(No Use)
GPP_F11	VCCPGPPEF	None	No	Yes	SATA_SLOAD	od					GP-In	None	PCH_RSVD(No Use)
GPP_F12	VCCPGPPEF	None	No	Yes	SATA_SDATAOUT1	od					GP-In	None	SV_ADVANCE_GP48(No Use)
GPP_F13	VCCPGPPEF	None	No	Yes	SATA_SDATAOUT2	od					GP-In	None	GP39_GFX_CRB_DETECT(No Use)
GPP_F14	VCCPGPPEF	None	No	Yes	None		PS_ON#	out			GP-In	None	H_SKTOCC_N
GPP_F15	VCCPGPPEF	None	No	Yes	USB_OC4#	in					GP-In	None	USB30_OCP#7
GPP_F16	VCCPGPPEF	None	No	Yes	USB_OC5#	in					GP-In	None	USB2_OCP#5(No Use)
GPP_F17	VCCPGPPEF	None	No	Yes	USB_OC6#	in					GP-In	None	USB2_OCP#6 (No Use)
GPP_F18	VCCPGPPEF	None	No	Yes	USB_OC7#	in					GP-In	None	USB2_OCP#7(No Use)
GPP_F19	VCCPGPPEF	None	No	Yes	eDP_VDDEN	out					GP-Out	None	EDP_VDDEN
GPP_F20	VCCPGPPEF	None	No	Yes	eDP_BKLTEN	out					GP-Out	None	EDP_BKLTEN
GPP_F21	VCCPGPPEF	None	No	Yes	eDP_BKLTCTL	out					GP-Out	None	BKLTCTL
GPP_F22	VCCPGPPEF	None	No	Yes	DDPF_C-TRLCLK	iod					GP-Out	None	PCH_GPU_RST_N
GPP_F23	VCCPGPPEF	None	No	No	DDPF_C-TRLDATA	iod					GP-Out	None	(No Use)

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Group G GPIO - Primary Power Well (1.8V or 3.3V)														
GPP_G0	VCCPGPPG_3P3 or VCCPRIM_1P8	None	No	Yes	SD_CMD	inout					GP-In	SMI	(No Use)
GPP_G1	VCCPGPPG_3P3 or VCCPRIM_1P8	None	No	Yes	SD_DATA0	inout					GP-In	SMI	(No Use)
GPP_G2	VCCPGPPG_3P3 or VCCPRIM_1P8	None	No	Yes	SD_DATA1	inout					GP-In	SMI	(No Use)
GPP_G3	VCCPGPPG_3P3 or VCCPRIM_1P8	None	No	Yes	SD_DATA2	inout					GP-In	SMI	(No Use)
GPP_G4	VCCPGPPG_3P3 or VCCPRIM_1P8	None	No	Yes	SD_DATA3	inout					GP-In	SMI	(No Use)
GPP_G5	VCCPGPPG_3P3 or VCCPRIM_1P8	None	No	Yes	SD_CD#	in					GP-In	SMI	(No Use)
GPP_G6	VCCPGPPG_3P3 or VCCPRIM_1P8	None	No	Yes	SD_CLK	out					GP-In	SMI	(No Use)
GPP_G7	VCCPGPPG_3P3 or VCCPRIM_1P8	None	No	Yes	SD_WP	in					GP-In	SMI	(No Use)

Group H GPIO - Primary Power Well (1.8V or 3.3V)													
GPP_H0	VCCPGPPHK	None	No	Yes	SRCCLKREQ6#	iod					GP-In	None	(No Use)
GPP_H1	VCCPGPPHK	None	No	Yes	SRCCLKREQ7#	iod					GP-In	None	CLKREQ_LAN_N
GPP_H2	VCCPGPPHK	None	No	Yes	SRCCLKREQ8#	iod					GP-In	None	CLKREQ_M.2_WLAN_N
GPP_H3	VCCPGPPHK	None	No	Yes	SRCCLKREQ9#	iod					GP-In	None	(No Use)
GPP_H4	VCCPGPPHK	None	No	Yes	SRCCLKREQ10#	iod					GP-In	None	(No Use)
GPP_H5	VCCPGPPHK	None	No	Yes	SRCCLKREQ11#	iod					GP-In	None	(No Use)
GPP_H6	VCCPGPPHK	None	No	Yes	SRCCLKREQ12#	iod					GP-In	None	(No Use)
GPP_H7	VCCPGPPHK	None	No	Yes	SRCCLKREQ13#	iod					GP-In	None	(No Use)
GPP_H8	VCCPGPPHK	None	No	Yes	SRCCLKREQ14#	iod					GP-In	None	(No Use)
GPP_H9	VCCPGPPHK	None	No	Yes	SRCCLKREQ15#	iod					GP-In	None	(No Use)
GPP_H10	VCCPGPPHK	None	Yes	Yes	SML2CLK	iod					GP-In	None	(No Use)
GPP_H11	VCCPGPPHK	None	Yes	Yes	SML2DATA	iod					GP-In	None	(No Use)
GPP_H12	VCCPGPPHK	20K_PD	Yes	No	SML2ALERT#	iod					GP-Out	None	FM_ESPI_FLASH_MODE (STRAP)
GPP_H13	VCCPGPPHK	None	Yes	Yes	SML3CLK	iod					GP-In	None	(No Use)
GPP_H14	VCCPGPPHK	None	Yes	Yes	SML3DATA	iod					GP-In	None	(No Use)
GPP_H15	VCCPGPPHK	None	Yes	Yes	SML3ALERT#	iod					GP-In	None	(No Use)
GPP_H16	VCCPGPPHK	None	Yes	Yes	SML4CLK	iod					GP-In	None	(No Use)
GPP_H17	VCCPGPPHK	None	Yes	Yes	SML4DATA	iod					GP-In	None	(No Use)
GPP_H18	VCCPGPPHK	None	Yes	Yes	SML4ALERT#	iod					GP-In	None	(No Use)
GPP_H19	VCCPGPPHK	None	Yes	Yes	ISH_I2C0_SDA	iod					GP-In	None	(No Use)
GPP_H20	VCCPGPPHK	None	Yes	Yes	ISH_I2C0_SCL	iod					GP-In	None	(No Use)
GPP_H21	VCCPGPPHK	None	Yes	Yes	ISH_I2C1_SDA	iod					GP-In	None	(No Use)
GPP_H22	VCCPGPPHK	None	Yes	Yes	ISH_I2C1_SCL	iod					GP-In	None	(No Use)
GPP_H23	VCCPGPPHK	None	No	Yes	TIME_SYNC0	inout					GP-In	None	(No Use)

Group I GPIO - Primary Power Well (3.3V Only)													
GPP_I0	VCCPRIM_3P3	None	No	Yes	DDPB_HPD0	in					GP-In	NMI SMI	(No Use)
GPP_I1	VCCPRIM_3P3	None	No	Yes	DDPB_HPD1	in					GP-In	NMI SMI	(No Use)
GPP_I2	VCCPRIM_3P3	None	No	Yes	DDPB_HPD2	in					GP-In	NMI SMI	DP_SINK_HPD
GPP_I3	VCCPRIM_3P3	None	No	Yes	DDPB_HPD3	in					GP-In	NMI SMI	(No Use)
GPP_I4	VCCPRIM_3P3	None	No	Yes	EDP_HPD	in					GP-In	None	EDP_HPD
GPP_I5	VCCPRIM_3P3	None	Yes	Yes	DDPB_CTRLCLK	iod					GP-In	None	(No Use)
GPP_I6	VCCPRIM_3P3	20K PD	Yes	No	DDPB_CTRLDATA	iod					GP-Out	None	(No Use)
GPP_I7	VCCPRIM_3P3	None	Yes	Yes	DDPC_CTRLCLK	iod					GP-In	None	(No Use)
GPP_I8	VCCPRIM_3P3	20K PD	Yes	No	DDPC_CTRLDATA	iod					GP-Out	None	(No Use)
GPP_I9	VCCPRIM_3P3	None	Yes	Yes	DDPD_CTRLCLK	iod					GP-In	None	DDPD_CTRLCLK
GPP_I10	VCCPRIM_3P3	20K PD	Yes	No	DDPD_CTRLDATA	iod					GP-Out	None	DDPD_CTRLDATA
GPP_I11	VCCPRIM_3P3	20K PD	Yes	No	M2_SKT2_CFG0	in					GP-In	None	H_SKTOCC_N
GPP_I12	VCCPRIM_3P3	20K PD	Yes	No	M2_SKT2_CFG1	in					GP-In	None	(No Use)
GPP_I13	VCCPRIM_3P3	20K PD	Yes	No	M2_SKT2_CFG2	in					GP-In	None	(No Use)
GPP_I14	VCCPRIM_3P3	20K PD	Yes	No	M2_SKT2_CFG3	in					GP-In	None	(No Use)

Group J GPIO - Primary Power Well (1.8V Only)													
GPP_J0	VCCPRIM_1P8	None	No	No	CNV_PA_BLANKING	in					GP-In	NMI SMI	(No Use)
GPP_J1	VCCPRIM_1P8	None	No	No			CPU_VC-CIO_P-WR_GATE#	out			Native F2	NMI SMI	(No Use)
GPP_J2	VCCPRIM_1P8	None	No	No							GP-In	NMI SMI	CNVI_EN_N
GPP_J3	VCCPRIM_1P8	None	No	No							GP-In	NMI SMI	(No Use)
GPP_J4	VCCPRIM_1P8	None	No	No	CNV_BRI_DT	out	UART0B_RTS#	out			Native F1	None	CNV_BRI_DT(STRAP)
GPP_J5	VCCPRIM_1P8	None	No	Yes	CNV_BRI_RSP	in	UART0B_RXD	in			Native F1	None	CNV_BRI_RSP(STRAP)
GPP_J6	VCCPRIM_1P8	20K PD	No	No	CNV_RGI_DT	out	UART0B_TXD	out			Native F1	None	(No Use)
GPP_J7	VCCPRIM_1P8	None	No	Yes	CNV_RGI_RSP	in	UART0B_CTS#	in			Native F1	None	(No Use)
GPP_J8	VCCPRIM_1P8	20K PD	No	Yes	CNV_M-FUART2_RXD	in					GP-In	None	(No Use)
GPP_J9	VCCPRIM_1P8	None	No	No	CNV_M-FUART2_TXD	out					GP-Out	None	CNV_MFUART2_TXD(STRAP)
GPP_J10	VCCPRIM_1P8	20K PD	No	Yes							GP-In	None	(No Use)
GPP_J11	VCCPRIM_1P8	20K PD	No	Yes	A4WP_PRESENT	in					Native F1	None	(No Use)

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Group K GPIO - Primary Power Well (1.8V or 3.3V)													
GPP_K0	VCCPGPPHK	None	Yes	Yes							GP-In	None	(No Use)
GPP_K1	VCCPGPPHK	None	Yes	Yes							GP-In	None	(No Use)
GPP_K2	VCCPGPPHK	None	Yes	Yes							GP-In	None	H_PROCHOT_PCH_N
GPP_K3	VCCPGPPHK	None	Yes	Yes							GP-In	None	(No Use)
GPP_K4	VCCPGPPHK	None	Yes	Yes							GP-In	None	(No Use)
GPP_K5	VCCPGPPHK	None	Yes	Yes							GP-In	None	(No Use)
GPP_K6	VCCPGPPHK	None	Yes	Yes							GP-In	None	(No Use)
GPP_K7	VCCPGPPHK	None	Yes	Yes							GP-In	None	(No Use)
GPP_K8	VCCPGPPHK	None	No	Yes	Reserved	od					Native F1	None	(No Use)
GPP_K9	VCCPGPPHK	None	No	Yes	Reserved	od					Native F1	None	(No Use)
GPP_K10	VCCPGPPHK	None	No	Yes	Reserved	od					Native F1	None	(No Use)
GPP_K11	VCCPGPPHK	None	No	Yes	Reserved	od					Native F1	None	(No Use)
GPP_K12	VCCPGPPHK	20K_PD	No	No	GSXDOUT	out					GP-In	None	BRD_ID0
GPP_K13	VCCPGPPHK	None	No	Yes	GSXSLOAD	out					GP-In	None	BRD_ID1
GPP_K14	VCCPGPPHK	None	No	Yes	GSXDIN	in					GP-In	None	BRD_ID2
GPP_K15	VCCPGPPHK	None	No	Yes	GSXSRESET#	out					GP-In	None	BRD_ID3
GPP_K16	VCCPGPPHK	None	No	Yes	GSXCLK	out					GP-In	None	BRD_ID4
GPP_K17	VCCPGPPHK	None	No	Yes	ADR_COM-PLETE	out					GP-In	None	BRD_ID5
GPP_K18	VCCPGPPHK	None	No	Yes	NMI#	od					GP-In	None	(No Use)
GPP_K19	VCCPGPPHK	None	No	Yes	SMI#	od					GP-In	None	SIO_SCI_N
GPP_K20	VCCPGPPHK	None	No	Yes	Reserved	out					Native F1	None	SPI_TPM_PIRQ
GPP_K21	VCCPGPPHK	None	No	Yes	Reserved	out					Native F1	None	(No Use)
GPP_K22	VCCPGPPHK	None	No	Yes	IMGCLKOUT0	out					GP-In	None	(No Use)
GPP_K23	VCCPGPPHK	None	No	Yes	IMGCLKOUT1	out					GP-In	None	(No Use)

GPIO in Deep Sleep Power Well (3.3V Only)													
GPD0	VCCDSW_3P3	None	No	Yes	BATLOW#	in					Native F1	None	PU_PCH_GPD_0_BATLOW_N (No Use)
GPD1	VCCDSW_3P3	None	No	Yes	ACPRESENT	in					Native F1	None	ACPRESENT(No Use)
GPD2	VCCDSW_3P3	None	No	Yes	LAN_WAKE#	in					Native F1	None	LANWAKE_N
GPD3	VCCDSW_3P3	None	Yes	Yes	PWRBTN#	in					Native F1	None	PWRBTN_N
GPD4	VCCDSW_3P3	None	No	Yes	SLP_S3#	out					Native F1	None	SLP_S3_N
GPD5	VCCDSW_3P3	None	No	Yes	SLP_S4#	out					Native F1	None	SLP_S4_N
GPD6	VCCDSW_3P3	None	No	Yes	SLP_A#	out					Native F1/ GP-In	None	(No Use)
GPD7	VCCDSW_3P3	None	No	No							GP-Out	None	PCH_WAKEO_N(STRAP)(No Use)
GPD8	VCCDSW_3P3	None	No	Yes	SUSCLK	out					Native F1	None	PCH_SUSCLK
GPD9	VCCDSW_3P3	None	No	Yes	SLP_WLAN#	out					Native F1	None	SLP_WLAN_N
GPD10	VCCDSW_3P3	None	No	Yes	SLP_S5#	out					Native F1/ GP-In	None	SLP_S5_N (TP)(No Use)
GPD11	VCCDSW_3P3	None	No	Yes	LANPHYPC	out					Native F1	None	LAN_DISABLE_N

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TITLE: M920z/M828z CNL-PCH GPIO Table 8		REV: V1.0
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Signal	Usage	When Sampled	Internal PU/PD	Definition		M920z Setting
				Set To	Description	
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	Weak PD	0	Disable "Top Swap" mode (Default)	0 (No external PD)
				1	Enable "Top Swap" mode	
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	Weak PD	0	Disable "No Reboot" mode	0 (PD R116 1K)
				1	Enable "No Reboot" mode	
SMBALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	Weak PD	0	Disable Intel ME Crypto Transport Layer	1 (PU R499 4K7)
				1	Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality)	
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	Weak PD	0	SPI	0 (No external PD)
				1	LPC	
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	Weak PD	0	LPC Is selected for EC	0 (No external PD)
				1	eSPI Is selected for EC	
SPI0_MOSI	BOOT HALT	Rising edge of RSMRST#	Weak PU	0	ENABLE	1 (No external PU)
				1	DISABLED	
GPP_H15 / SML3ALERT#	JTAG ODT	Rising edge of PCH_PWROK		0	ODT DISABLE	1 (PU R5153 4K7)
				1	ODT ENABLE	
SPI0_MISO	JTAG ODT	Rising edge of PCH_PWROK	Weak PU	0	ODT DISABLE	1 (no external PD)
				1	ODT ENABLE	
GPP_B23 / SML1ALERT# /	Intel® DCI-OOB	Rising edge of RSMRST#	Weak PD	0	Disable Intel® DCI-OOB (Default)	1 (PU R97 4K7)
				1	Enable Intel® DCI-OOB	
SPI0_IO2	Reserved(CONSENT)	Rising edge of RSMRST#	Weak PU	0	ENABLE	1 (PU R223 1K)
				1	DISABLE	
SPI0_IO3	PESONALITY	Rising edge of RSMRST#	Weak PU	0	ENABLE	1 (PU R224 1K)
				1	DISABLE	
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	Weak PD	0	Enable security measures defined in the Flash Descriptor	0 (No external PD)
				1	Disable Flash Descriptor Security (override)	
GPP_H12 / SML2ALERT#	eSPI Flash Sharing Mode	Rising edge of RSMRST#	Weak PD	0	MAFS	0 (No external PD)
				1	SAFS	
DDPB_CTRLDATA / GPP_I6	Display Port B Detected	Rising edge of PCH_PWROK	Weak PD	0	Port B is not detected	0 (No external PD)
				1	Port B is detected	
DDPC_CTRLDATA / GPP_I8	Display Port C Detected	Rising edge of PCH_PWROK	Weak PD	0	Port C is not detected	0 (No external PD)
				1	Port C is detected	
DDPD_CTRLDATA / GPP_I10	Display Port D Detected	Rising edge of PCH_PWROK	Weak PD	0	Port D is not detected	1 (PU R593 2K2)
				1	Port D is detected	
GPP_F23	Display Port F Detected	Rising edge of PCH_PWROK	Weak PD	0	Port D is not detected	0 (No external PD)
				1	Port D is detected	
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	Weak PD	0	38.4 XTAL frequency selected. (Default)	1 (PU R4991 10K)
				1	24MHz XTAL frequency selected.	
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#		0	Integrated CNVi enable.	1 (PU R4990 10K)
				1	Integrated CNVi disable	
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	Weak PD	0	VCCSPI is connected to 3.3V rail	0 (No external PD)
				1	VCCSPI is connected to 1.8V rail	
GPD7	Reserved	Rising edge of DSW_PWROK	Weak PD	0	XTAL INPUT IS SINGLE-ENDED	1 (PU R4981 1K)
				1	XTAL IMPUT IS DIFFERENTIAL	

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TITLE: M920z/M828z CNL-PCH Strapping		REV: V1.0
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PIN No.	GPIO	IN/OUT	M920z/M828z Usage	Behavior
2	GP16	OUT	MONITOR_PWR_ON	Turn off MONITOR_PWR_ON的條件: SLP_SUS = low 且 System = _SYSTEM_S5 且 DP_SEL = high ,+5V_MM(pin87) :0 SLP_S3_N : 1 ->latch MONITOR_PWR_ON, release 條件 : press power button (For safty) Turn on MONITOR_PWR_ON的條件: 1.Monitor_Btn to power on monitor mode 2.DPIN for DP auto detect 3.Press power button to power on system (System = _SYSTEM_S0)
6	GP63	IN	SLP_SUS_N_SIO	S0~S5 :high ,deep sleep : low
10	GP52	IN	PSIN_R	no action
11	GP51	OUT	HDD_LED_DIS	no action ,default :low , by BIOS setup menu
12	GP37	OUT	CHARGE_CTRL1	follow usb charge control table
13	GP36	OUT	EC_MUTE_AMP	no action ,default high
14	GP35	OUT	DP_SEL	scalar inform EC to switch monitor mode or PC mode via I2C,H:DP OUT L:DP IN
16	GP31	OUT	LEDCTRL_PWR	Power LED Behavior: - System on: On - System in Standby Gradual 1s On, Gradual 1s OFF, 3s OFF - Initial Connection of Power (e.g. via AC adaptor or AC-in) Blink 3 Times (0.25 s On/ 0.25 s Off , repeat x 3) - System entering hibernation Blink (0.25 s On/ 0.25 s Off) - System off OFF
18	GP27	IN	CONFIG2	default :high ,cable is plugged ->low
19	GP26	IN	INA300_ALERT	Power meter IC ALERT to EC ,only for M828z
20	GP25	OUT	MIC_MUTE_CODEC	H->L,L->H when MIC MUTE BUTTON trigger
21	GP24	IN	MIC_MUTE	from MIC MUTE button
24	GP21	OUT	DP_EN	no action ,default :high
25	GP20	OUT	CHARGE_EN	follow usb charge control table
26	GP17	OUT	SYS5VSB_OFF	follow SLPSUS(SLP_SUS_N) behavior and invert ,+5V_S5(pin90 ,SLP_S5_N : 1 ->latch SYS5VSB_OFF release 條件 : press power button(For safty)
31	GP12	IN	FPGPIO1	no action
32	GP11	IN	FPGPIO1	no action
66	GP44	OUT	PWRBTN_N	follow PANSW behavior
70	GP42	OUT	PSON_N	follow SUSB(SLP_S3_N) behavior and invert ,
76	GP57	OUT(OD)	SIO_H_PROCHOT_N	follow OBP flow chart,only for M920z w/o GPU and M828z w/GPU.
77	GP56	OUT	DP_PWR_SEL	no action
93	GP97	IN	KERNEL_DBG_N	For port80 Pnp
94	GP80	IN	NA	NA
95	GP81	IN	PS_ON_B	TBD (for Modern standby)
96	GP82	IN	SLP_S0_N	TBD (for Modern standby)
97	GP83	IN	PSON_SIO_N	TBD (for Modern standby)
98	GP84	OUT	SIO_GPIO84	TBD (for USB type-C 0.9A /3A option)
99	GP87	IN	FPGPIO3	no action
102	GP70	OUT	USB_PO_EN	set default enable ,follow note4 table
103	GP71	OUT	CLEAR_CMOS_EC	TBD
104	GP72	OUT	CHARGE_ILIM	follow usb charge control table
105	GP73	OUT	CHARGE_CTRL3	follow usb charge control table
106	GP74	OUT	CHARGE_CTRL2	follow usb charge control table
107	GP75	OUT	MONI_ACK	NA
108	GP76	IN	MONI_INT	Scalar notify EC
109	GP76	OUT	ME_CTL	TBD
120	GP66	IN	H_SKTOCC_N	gate GP42_ PSON_N

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TITLE: M920z/M828z SIO GPIO Table 1	REV: V1.0
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RTD2526A-CG SCALER GPIO TABLE

PIN #	Signal Name	Description	Voltage	IN/OUT	M920 Usage	Default	Behavior
21	GPIO_1	MCU_GPIO	5V tolerance when power-off	OUT	EDP_HPD	LOW	scaler拉high
22	GPIO_2	MCU_GPIO	5V tolerance when power-off	OUT	DP_SOURCE_HPD	LOW	scaler拉high
34	GPIO_PWM0_MCK_CLKO	MCU GPIO/PWM/I2S/CLKO	5V tolerance when power-off	--	(No Use)		
35	GPIO_PWM1_SCK_IRQB	MCU GPIO/PWM/I2S/IRQB	5V tolerance when power-off	--	(No Use)		
36	GPIO_PWM2_WS	MCU GPIO/PWM/I2S	5V tolerance when power-off	--	(No Use)		
37	GPIO_PWM3_IICSCL0_RXD_SD0_SPDIF0	MCU GPIO/PWM/IIC BUS/UART/I2S/SPDIF	5V tolerance when power-off	--	PANEL_SMBUS_CLK		
38	GPIO_IICSDA0_TXD	MCU GPIO/PWM/IIC BUS/UART/I2S/	5V tolerance when power-off	--	PANEL_SMBUS_DATA		
39	GPIO_3	MCU_GPIO	5V tolerance when power-off	--	(No Use)		
42	A-ADC0_GPIO	5bits MCU ADC Input/MCU GPIO	3.3 V tolerance when using ADC Input; 5V Tolerance power on when using GPIO	OUT	PWM_EN_SW	HIGH	PC MODE:H Monitor MODE:L
43	A-ADC1_GPIO	5bits MCU ADC Input/MCU GPIO	3.3 V tolerance when using ADC Input; 5V Tolerance power on when using GPIO	--	(No Use)		
44	A-ADC2_GPIO	5bits MCU ADC Input/MCU GPIO	3.3 V tolerance when using ADC Input; 5V Tolerance power on when using GPIO	OUT	SYSTEM_EEPROM_WP	HIGH	WP_ENABLE:H WP_DISABLE:L
45	A-ADC3_GPIO	5bits MCU ADC Input/MCU GPIO	3.3 V tolerance when using ADC Input; 5V Tolerance power on when using GPIO	--	(No Use)		
46	GPIO_PWM1	MCU GPIO/PWM	5V tolerance when power-off	--	(No Use)		
47	GPIO_IICSCL1_IICSCL_AUX	CU GPIO/IIC BUS/IIC over AUX	5V tolerance when power-off	Native	EESCL		
48	GPIO_IICSDA1_IICSDA_AUX	MCU GPIO/IIC BUS/IIC over AUX	5V tolerance when power-off	Native	EESDA		
49	GPIO_DDCSCLVGA_RXD	MCU GPIO/VGA IIC BUS/UART	5V tolerance when power-off	--	(No Use)		
50	GPIO_DDCSDAVGA_TXD	MCU GPIO/VGA IIC BUS/UART	5V tolerance when power-off	--	(No Use)		
52	GPIO_PWM0	MCU GPIO/PWM	5V tolerance when power-off	OUT	LCD_BKLTCTL	PWM0 (OD)	scaler pwm output
53	GPIO_PWM3_1	CU GPIO/PWM	5V tolerance when power-off	IN/OUT	MONI_INT		
55	GPIO_PWM0_I2S_MCK_LINE_INL	MCU GPIO/PWM/I2S/LINE-IN	3.3V Tolerance	IN	MONI_ACK		
56	GPIO_I2S_SCK_LINE_INR	MCU GPIO/I2S/LINE-IN	3.3V Tolerance	--	(No Use)		
57	GPIO_I2S_WS_AUDIO_REF	MCU GPIO/I2S/ Audio Reference Resistance	3.3V Tolerance	--	(No Use)		
58	GPIO_I2S_SD0_SPDIF0_SOUTL	MCU GPIO/I2S/SPDIF/Speaker Out	3.3V Tolerance	--	(No Use)		
59	GPIO_SOUTR	MCU GPIO/Speaker Out	3.3V Tolerance	IN	LCD_ID3		
60	GPIO_IICSCL2_RXD_HOUTL	MCU GPIO/IIC BUS/UART/ Head Phone Out	3.3V Tolerance	--	(No Use)		
61	GPIO_IICSDA2_TXD_HOUTR	MCU GPIO/IIC BUS/UART/ Head Phone Out	3.3V Tolerance	--	(No Use)		
63	GPIO_PWM0_PWM3_INT1_T2_IHS	MCU GPIO/PWM/MCU EXINT1/ DVI Control Signal/HIS	5V tolerance even when power-off	OUT	LCD_BKLTE	HIGH	BACKLIGHT ON:L BACKLIGHT OFF:H
64	GPIO_PWM2_INT0_IENA_CLKO	MCU GPIO/PWM/MCU EXINT0/DVI Control Signal/IENA/CLKO	5V tolerance even when power-off	OUT	PANEL_ON	LOW	PANEL ON:H PANEL OFF:L
65	GPIO_4	MCU GPIO	5V tolerance even when power-off	--	--		
67	GPIO/TXO3+_8b	MCU GPIO	3.3V Tolerance	Native	LCD1DO3		
68	GPIO/TXO3-_8b	MCU GPIO	3.3V Tolerance	Native	LCD1DO3#		

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TITLE: M920z/M828z Scalar GPIO Table 1			REV: V1.0
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70	GPIO/TXO2-_8b	MCU GPIO	3.3V Tolerance	Native	LCD1DO2#		
71	GPIO/TXO1+_8b	MCU GPIO	3.3V Tolerance	Native	LCD1DO1		
72	GPIO/TXO1-_8b	MCU GPIO	3.3V Tolerance	Native	LCD1DO1#		
73	GPIO/TXO0+_8b	MCU GPIO	3.3V Tolerance	Native	LCD1DO0		
74	GPIO/TXO0-_8b	MCU GPIO	3.3V Tolerance	Native	LCD1DO0#		
90	GPIO_5	MCU GPIO	5V tolerance even when power-off	--	--		
91	GPIO_6	MCU GPIO	5V tolerance even when power-off	--	--		
92	GPIO_PWM3_2	GPIO_PWM3_2	5V tolerance even when power-off	--	--		
93	GPIO_PWM2_1	GPIO_PWM2_1	5V tolerance even when power-off	--	--		
94	GPIO_PWM1_1	GPIO_PWM1_1	5V tolerance even when power-off	--	--		
96	GPIO_FLASH_WP_INT0	GPIO_FLASH_WP_INT0	5V tolerance even when power-off	OUT	FLASH_WP	LOW	WRITE_PROTECT_ ENABLE:L
97	GPIO_INT1_IVS	GPIO_INT1_IVS	5V tolerance even when power-off (GPIO OD)	IN	LCD_ID0		
98	GPIO_T0_DENA	GPIO_T0_DENA	5V tolerance even when power-off	IN	LCD_ID1		
99	GPIO_PWM2_PWM3_T1_DHS	GPIO_PWM2_PWM3_T1_DHS	5V tolerance even when power-off	IN	LCD_ID2		
100	VGADDC2_SCL_GPIO_PWM_IN_AUX_D2_DCLK_T2EX	VGADDC2_SCL_GPIO_PWM_IN_AUX_D2_DCLK_T2EX	5V tolerance even when power-off	IN/OUT	RTLD2526_SMBCLK		
101	VGADDC2_SDA_GPIO_PWM_OUT_AUX_D1_DVS	VGADDC2_SDA_GPIO_PWM_OUT_AUX_D1_DVS	3.3V tolerance	IN/OUT	RTLD2526_SMBDATA		
102	GPIO_7	GPIO_7	3.3V tolerance	--	(No Use)		
108	GPIO_8	GPIO_8	3.3V tolerance	--	(No Use)		
110	GPIO_DDCSCL0_AUXP0	GPIO_DDCSCL0_AUXP0	3.3V tolerance	Native	DPIN_AUXP		
111	GPIO_DDCSDA0_AUXN0	GPIO_DDCSDA0_AUXN0	3.3V tolerance	Native	DPIN_AUXN		
112	GPIO_DDCSCL1_AUXP1	GPIO_DDCSCL1_AUXP1	3.3V tolerance	Native	EDP_AUXp		
113	GPIO_DDCSDA1_AUXN1	GPIO_DDCSDA1_AUXN1	3.3V tolerance	Native	EDP_AUXN		
114	GPIO_PWM2_2	GPIO_PWM2_2	3.3V tolerance	--	(No Use)		
115	GPIO_PWM1_2	GPIO_PWM1_2	3.3V tolerance	--	(No Use)		

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TITLE: M920z/M828z Scalar GPIO Table 2	REV: V1.0
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V0.1 to V0.2 CHAGNE LIST

page03:pop R14,15 51R1_1% to fix +1V05_CPU_VCCST_S3 leakage
page04:pop C3216 220pF to fix PWRGD_CPUPWRGD_1V no-monotonic,overshoot,undershoot
page04:pop R28 680R_1% to fix H_PROCHOT_R_N falling no-monotonic
page11 : reserve modern standby circuit for supporting MS.
page12 : pop C60 68pF to fix falling no-monotonic
page16:add CNVi for supporting Cnvi Intel WIFI module
page 18:change C84 C85 from18pF to 15pF for ppm fine tune
page19:nopop R140,R143 51R to fix +1V05_CPU_VCCST_S3 leakage
page19:pop R4600 33R to fix PWRGD_CPUPWRGD_1V no-monotonic,overshoot,undershoot
page 22:chagne R206 from 1K5_1% to 150R and R208 from 45.3K to 4.53K for fix VCCRTC drop fail.
page 24:remove second flash socket due to space issue for supporting Cnvi Intel WIFI module
page 28:connect DPIN_AUXP_C/DPIN_AUXN_C to pin34/35 for DP IN cable detection
page 28:change scalar SMBUS debug test point to pin49/50 for realtek requiremtn to avoid SMBUS conflict
page 28:change C1290 C1291 from12pF to 15pF for ppm fine tune
page 29:remove IO BOX header due to space issue for supporting Cnvi Intel WIFI module
page 33:remove R4796 0R to increase +5V_S0 power plane for SATA power
page 34:add CNVi net and change power control for supporting Cnvi Intel WIFI module
page 34:change C201 C202 to 0.1uF 0201 for supporting CNVi and routing.
page 34:pop C199 220pF to fix M.2_WLAN_RST_N no-monotonic
page 36:remove L168 ,L222 short net .Lenovo update smokeless critera
page 38:change DMIC header pin pitch from 1.25mm to 1mm for AVC requirement
page 39:reserve Q484 2N7002 to control tyep-c support current via EC for Lenovo requirement
page 39:pop R4667 4K7 to fix VBUS falling time fail.
page 42:add USB power on circuit for Lenovo requirement
page 43:add USB power on MUX IC for Lenovo requirement
page 44:pop C308 220pF to fix LAN_PE_RST_N no-monotonic
page 47:reserve MS control logic via EC for cost down
page 47:change MONI_ACK PU from +3V3_SIO_DSW to +3V3_mm to fix +3V3_MM leakage in deep sleep mode
page 47:pop R1260 10K to fix TPM no found issue
page 47:pop R1318 R1280 0R for support USB PO.
page 48:change FAN header from RA to vertical for AVC requirement and cable routing
page 58 : nopop R5132 and R5129 1k to fix no power on +VDD_GPU_S0 and +1V35_GPU_S0
page 59 : add D145 1N4148 for timing fine-tune
page 59 : C2872 change from 22uF to 100pF for stability fine-tuning for +0V95_GPU_S0
page 59 : pop CB116 0.1uF to fix +3V3_GPU_S0 slew rate .
page 59 : change R899. to 1K for fine-tuning +3V3_GPU_S0 power sequence.
page 60:change R2113 from 270R to 1.24K and R2148 from 5.11K to 1.87K for RC time constant setting of +1V35_GPU_S0.
page 60:use lower DCR L250 and change R5143 from 1R to 4.7R and C3172 from 2200pF to 680pF to Increase power conversion efficiency of +1V35_GPU_S0.
page 60:change R4950/R2125 from 787R to 1.27K for RC time constant setting of +VDD_GPU_S0.
page 60:use lower DCR L142/L143 and change R5145/R5146 from 1R to 4.7R and C3173/C3174 from 2200pF to 680pF to Increase power conversion efficiency of +VDD_GPU_S0.
page 60:change R4921 from 165K to 115K and R4923 from 2.37K to 2K for LL setting of +VDD_GPU_S0.
page 61 :change R4925 from 0R to 10K,R4926 from 220R to 1.6K,R4927 from 9.53K to 16K,R4928 from 16.9K to 10K,R4929 from 110R to 499R for OCP fine-tuning of +1V35_GPU_S0.
page 61 :change R2127 from 18K to 7.68K,R4930 from 4.87K to 20K,R4931 from 10K to 8.2K,R4933 from 25.5K to 27.4K,R4934 from 390R to 549R for OCP fine-tuning of +VDD_GPU_S0.
page 61 :change CE77 from 330uF to 560uF for fine-tuning of +1V35_GPU_S0 power noise.
page 62 :change C699 from 0.22uF to 0.47uF to fix Vmax. fail.
page 63 : nopop U112 and add Q486 2N7002 for MS to turn off VCC power rails via EC
page 64:change C731 from 100pF to 180pF,C744 from 220pF to 330pF,R1000 from 71.5K to 69.8K,R1004 from 71.5K to 69.8K
for loadline fine-tuning for +VCORE_CPU_S0 & +VCCGT_CPU_S0
page 64:pop R5239 2K and nopop R5240 for disable psys function.
page 64 :change R1014 from 3.24K to 499R,R1016 from 8.25K to 4.99K for fine-tuning VRHOT#.
page 68:change C809 from 330pF to 680pF for stability fine-tuning for +VCCSA_CPU_S0.
page 69:C2950 change from 1000pF to 680pF,C2948 from 100pF to 47pF for stability fine-tuning of +0V95_CPU_VCCIO_S0.
page 70:use lower DCR L61,lower Rds Q60/Q61 and change R1093 from 1R to 4.7R,C825 from 2200pF to 680pF to Increase power conversion efficiency of +1V2_DDR4_S3.
page 70:change R1101 from 9.53K to 2.8K for OCP fine-tuning of +1V2_DDR4_S3.
page 72 : nonpop R2095 to fix +5V_MM jitter issue
page 74 : pop C2147 0.1UF_25V_X7R for fine-tuning power sequence of 1V05_CPU_VCCSTG_S3.
page 76 : pop C982 1UF_25V_X7R for fine-tuning power sequence of +5V_S0.
page 79:change H3 for screw hole to stand off (for CR) for AVC requirement .Strain gauge PASS

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V0.2 to V0.3 CHAGNE LIST

page3:remove J1 XDP connector
page3:add CATERR LED for debug
page19:move WOR_N from GPP_D18 to GPP_C18 due to GPP_D power rail changed to 1.8V level
page20:move WOR_N from GPP_D18 to GPP_C18 due to GPP_D power rail changed to 1.8V level
page20:remove net KERNEL_DBG_N in PCH side ,EC F/W can control by itself.
page21:remove CB7 ,CB8 0402 and add C3347 C3348 0201 for better USB3.1 Gen2 RX margin
page21:change CB9 ,CB10 from 0.1uF to R5361 R5362 0R for tyep-c device compatible.
page22:change U1.AN24 power rail from +3V3_S5 to +VCCPRIM_1P8 for CNVi
page24:change R248 33R->56R2_1% ,R4998 33R->150R_1% to fix overshoot fail
page24:add J18 SPI SOCKET
page30:change panel power enable circuit and add TH11 FUSE to fix combustion fail
page30:change C1040 10uF to 4.7uF,add R1169 1K,nopop C1046 1uF to fix Innolux panel rising and falling time fail.
page34:add TH13 FUSE to fix combustion fail
page34:change stand-off into 階梯式 to fasten device easy for Lenovo requirement
page35:change stand-off into 階梯式 to fasten device easy for Lenovo requirement
page39:change C3298,C3299,C3301,C3300 from 0.1uF to 0.33uF and R5147,R5148,R5150,R5149 from 0R to C3302,C3303,C3304,C33050.1uF for type-c device compatible.
page39:reserve D152 ,D153,C3308,C3309 for ESD
page39:change P11 from 15U to 30U for Lenovo USB TYPE-C spec. requirement
page40: remove reserve L45 CMC ,R492 R494 0R for better JTOL.
page43:change U1 pin 10 and R515 PU voltage from +3V_S5 to +3v3_S5 due to typo.
page44:nopop R529 10K and pop R5357 100K to avoid to trigger CLKREQ_N when LAN is disabled.
page47:add C3313 1UF to fix +3V3_MM_1 -5% GB fail
page48:remove CE1 and add C3310 10UF for Cap. life
page50:reserve SW4,SW5 for second source
page57:nopop R5197,pop R5200 4K7 due to none OBFF design
page57:change R5120 left net from PLTRST_N to GPU_RST_N to fix DP out no display issue
page57:nopop R5042 47K confirmed from AMD if unused
page57:nopop R5049 ,C3156,R5050 due to GPIO_6 no support OCP_L
page59:add R901 0R->2K,R899 1K->20K ,pop C3312 0.47UF to fix +3V3_GPU_S0 slew rate fail
page59:nopop Q482,R5216,R5217,C3248 ,D145 for GPU timing fine-tune
page59:add C3307 10UF to fix +3V3_GPU_S0 drop
page60:change L250 footprint from TRIO to MAG.LAYERS for avoiding components interference
page63:nopop Q485 ,R5348 and pop U112,R1284,C2138 to fix "enter and exit S3 quickly fail issue"
page64:change R5239 PU from +5V_S0 to +5V_S5 for MS.
page64:change R1019 from 33k2 to 20k to fix L57 thermal test fail.
page66:change CE67 from 2000hr to 5000hr for cap. life.
page68:change R3350 PU from +5V_S0 to +5V_S5 and R3360 PU from +3V3_S0 to +5V_S0 to fix +VCCSA_CPU_S0 glitch
page69:change R4939 from 7K87_1% to 8K06_1% to fine-tune nominal value for +0V95_CPU_VCCIO_S0
page69:add CE24 560uF to fix tranient Vpeak fail
page70:change L61 footprint from TRIO to MAG.LAYERS for avoiding components interference
page70:change R1101 from 2k8_1% to 4k12_1% to fix inrush current fail
page74:change R5214 PU high from +5V_MM to +3V3_S5 and add C3320 1UF for MOW WW43 update VBUS sequence timing

V0.3 to V1.0 CHAGNE LIST

page38:nopop C3369 ,C3370 and change C3357 from 0.1uF to 0.033uF for timing fine-tune to avoid protection too late

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