MS-7388 VER:1.0

CPU:

AMD M2 Athlon 64/Athlon 64 FX AM2R2

System Chipset:

AMD RD780/RX780

ATI SB600

On Board Chipset:

FINTEK Super I/O -- F71882
LAN -- RTL8111B/RTL8111C
HD Codec --ALC888&883
BIOS -- SPI ROM 8M
1394 -- VT6308
ESATA-SIL3531

Main Memory:

DDR II X 4 (Max 8GB)

Expansion Slots:

PCI-E X 1 *2(RX780)
PCI-E X 16 *1(RX780)

PCI-E X 1 *1(FOR RD780)
PCI-E X 16 *2(FOR RD780)

PCI 2.2 Slot X 2

PWM:

Controller--Intersil ISL6323 4 Phase
Vcore 3 Phase (MOS HIGHX2 LOWX2)
Vnb 1 Phase (MOS HIGHX1 LOWX2)

Clock Generator:

Controller--ICS9LPRS477

111111
222222
X_manual part

Title	Cover Sheet
Rev	1.0
Document Number	MS-7388
Last Revision Date:	Tuesday, August 07, 2007
Sheet	1 of 39

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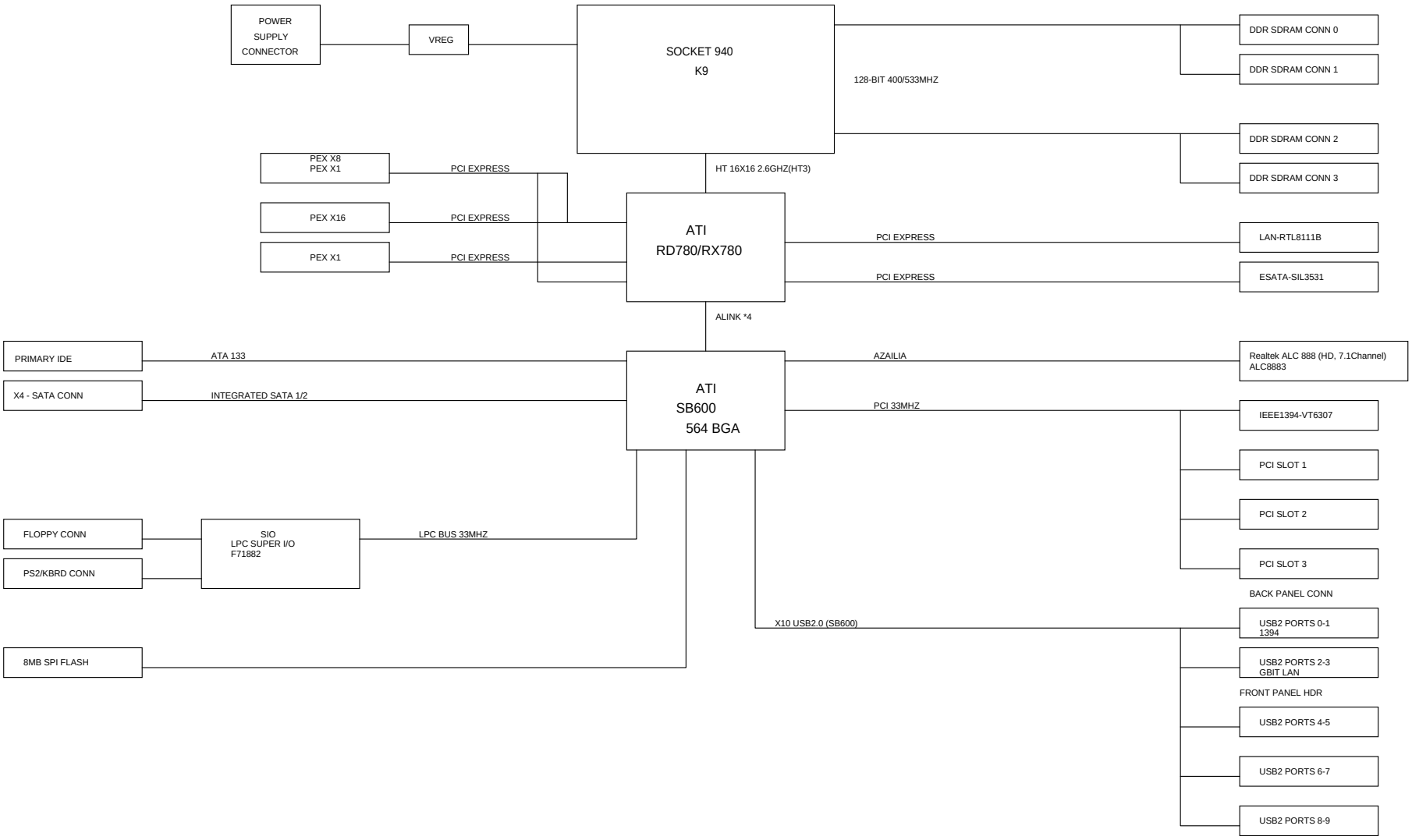
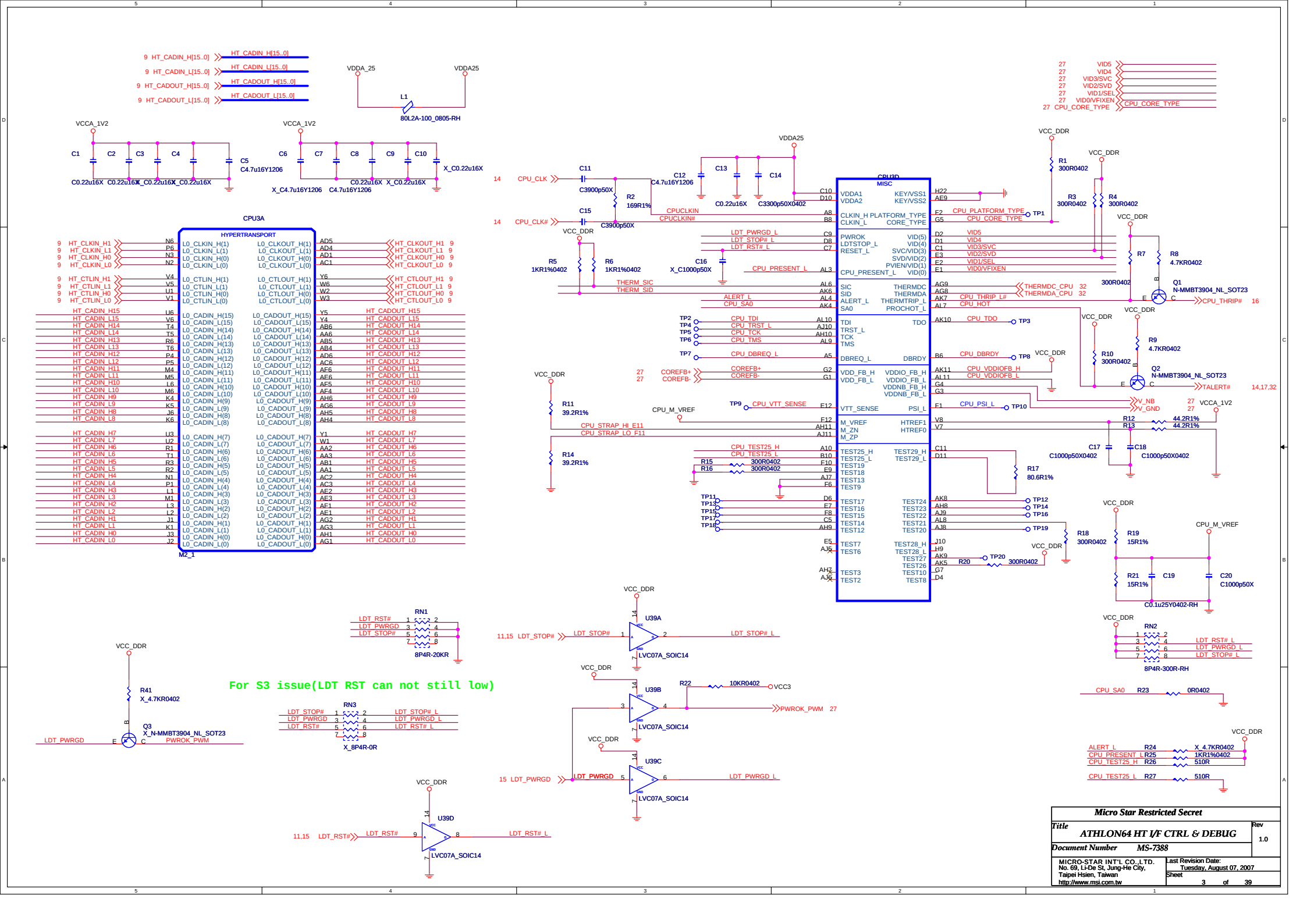
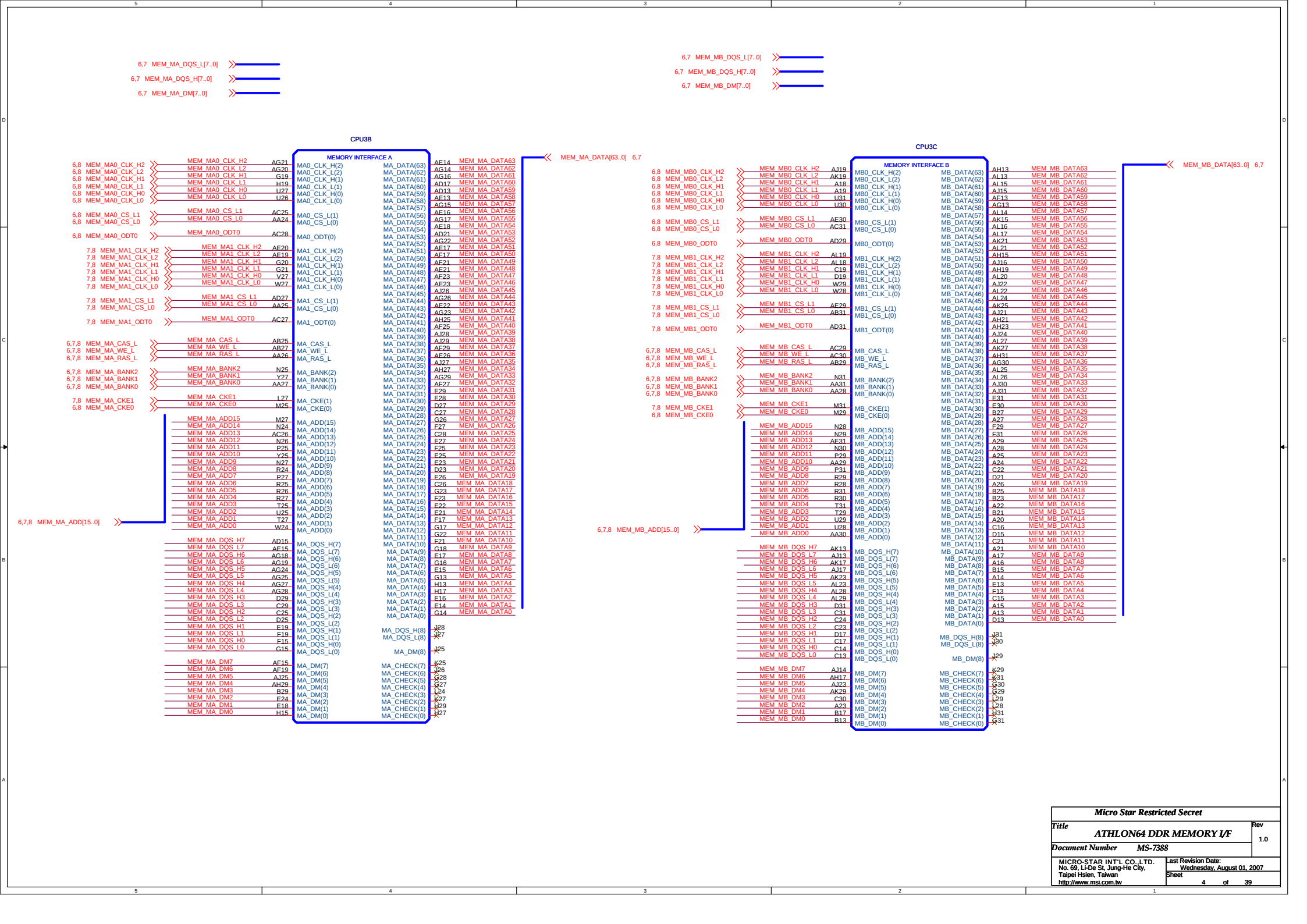
BLOCK DIAGRAM



Micro Star Restricted Secret		
Title	*Block Diagram*	Rev 1.0
Document Number	*MS-7388*	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, July 31, 2007	
	Sheet 2 of 39	


HT_CADIN_H[15..0]
HT_CADIN_L[15..0]
HT_CADOUT_H[15..0]
HT_CADOUT_L[15..0]
VDDA_25
VDDA25
L1
80L2A-100_0805-RH
VCCA_1V2
C1
C2
C3
C4
C5
C4.7u16Y1206
C0.22u16X
C6
C7
C8
C9
C10
X_C0.22u16X
X_C4.7u16Y1206
CPU3A
HYPERTRANSPORT
L0_CLKIN_H(1)
L0_CLKIN_L(1)
L0_CLKIN_H(0)
L0_CLKIN_L(0)
L0_CLKOUT_H(1)
L0_CLKOUT_L(1)
L0_CLKOUT_H(0)
L0_CLKOUT_L(0)
L0_CTLIN_H(1)
L0_CTLIN_L(1)
L0_CTLIN_H(0)
L0_CTLIN_L(0)
L0_CTLOUT_H(1)
L0_CTLOUT_L(1)
L0_CTLOUT_H(0)
L0_CTLOUT_L(0)
L0_CADIN_H(15)
L0_CADIN_L(15)
L0_CADIN_H(14)
L0_CADIN_L(14)
L0_CADIN_H(13)
L0_CADIN_L(13)
L0_CADIN_H(12)
L0_CADIN_L(12)
L0_CADIN_H(11)
L0_CADIN_L(11)
L0_CADIN_H(10)
L0_CADIN_L(10)
L0_CADIN_H(9)
L0_CADIN_L(9)
L0_CADIN_H(8)
L0_CADIN_L(8)
L0_CADIN_H(7)
L0_CADIN_L(7)
L0_CADIN_H(6)
L0_CADIN_L(6)
L0_CADIN_H(5)
L0_CADIN_L(5)
L0_CADIN_H(4)
L0_CADIN_L(4)
L0_CADIN_H(3)
L0_CADIN_L(3)
L0_CADIN_H(2)
L0_CADIN_L(2)
L0_CADIN_H(1)
L0_CADIN_L(1)
L0_CADIN_H(0)
L0_CADIN_L(0)
L0_CADOUT_H(15)
L0_CADOUT_L(15)
L0_CADOUT_H(14)
L0_CADOUT_L(14)
L0_CADOUT_H(13)
L0_CADOUT_L(13)
L0_CADOUT_H(12)
L0_CADOUT_L(12)
L0_CADOUT_H(11)
L0_CADOUT_L(11)
L0_CADOUT_H(10)
L0_CADOUT_L(10)
L0_CADOUT_H(9)
L0_CADOUT_L(9)
L0_CADOUT_H(8)
L0_CADOUT_L(8)
L0_CADOUT_H(7)
L0_CADOUT_L(7)
L0_CADOUT_H(6)
L0_CADOUT_L(6)
L0_CADOUT_H(5)
L0_CADOUT_L(5)
L0_CADOUT_H(4)
L0_CADOUT_L(4)
L0_CADOUT_H(3)
L0_CADOUT_L(3)
L0_CADOUT_H(2)
L0_CADOUT_L(2)
L0_CADOUT_H(1)
L0_CADOUT_L(1)
L0_CADOUT_H(0)
L0_CADOUT_L(0)
M2_1
CPU3D
MISC
CPU_CLK
CPU_CLK#
C11
C12
C13
C14
C15
C16
C3900p50X
C4.7u16Y1206
C0.22u16X
C3300p50X0402
R2
169R1%
CPUCLKIN
CPUCLKIN#
LDT_PWRGD_L
LDT_STOP#_L
LDT_RST#_L
CPU_PRESENT_L
X_C1000p50X
R5
1KR1%0402
R6
1KR1%0402
THERM_SIC
THERM_SID
ALERT_L
CPU_SA0
VDDA1
VDDA2
CLKIN_H
CLKIN_L
PROCHOT_L
TDI
TRST_L
TCK
TMS
TDO
DBREQ_L
DBRDY
VDD_FB_H
VDD_FB_L
VDDIO_FB_H
VDDIO_FB_L
VDDNB_FB_H
VDDNB_FB_L
VTT_SENSE
PSI_L
M_VREF
M_ZN
M_ZP
HTREF1
HTREF0
TEST25_H
TEST25_L
TEST19
TEST18
TEST13
TEST9
TEST29_H
TEST29_L
TEST17
TEST16
TEST15
TEST14
TEST12
TEST24
TEST23
TEST22
TEST21
TEST20
TEST7
TEST6
TEST28_H
TEST28_L
TEST27
TEST26
TEST10
TEST8
TEST3
TEST2
PWROK
LDTSTOP_L
RESET_L
CPU_PRESENT_L
VID(5)
VID(4)
SVC/VID(3)
SVD/VID(2)
PVIEN/VID(1)
VID(0)
SIC
SID
ALERT_L
SA0
THERMDC
THERMDA
THERMTRIP_L
PROCHOT_L
KEY/VSS1
KEY/VSS2
PLATFORM_TYPE
CORE_TYPE
CPU_PLATFORM_TYPE
CPU_CORE_TYPE
VID5
VID4
VID3/SVC
VID2/SVD
VID1/SEL
VID0/VFIXEN
THERMDC_CPU
THERMDA_CPU
CPU_THRIP_L#
CPU_HOT
CPU_THRIP#
CPU_TDI
CPU_TRST_L
CPU_TCK
CPU_TMS
CPU_TDO
CPU_DBREQ_L
CPU_DBRDY
CPU_VDDIOFB_H
CPU_VDDIOFB_L
V_NB
V_GND
CPU_PSI_L
CPU_VTT_SENSE
CPU_M_VREF
CPU_STRAP_HI_E11
CPU_STRAP_LO_F11
COREFB+
COREFB-
CPU_TEST25_H
CPU_TEST25_L
TALERT#
R1
300R0402
R3
300R0402
R4
300R0402
R7
4.7KR0402
R8
4.7KR0402
R9
4.7KR0402
R10
300R0402
Q1
N-MMBT3904_NL_SOT23
Q2
N-MMBT3904_NL_SOT23
R11
39.2R1%
R14
39.2R1%
R15
300R0402
R16
300R0402
R12
44.2R1%
R13
44.2R1%
R17
80.6R1%
R18
300R0402
R19
15R1%
R21
15R1%
C17
C1000p50X0402
C18
C1000p50X0402
C19
C20
C1000p50X
C0.1u25Y0402-RH
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TP17
TP18
TP19
TP20
RN1
LDT_RST#
LDT_PWRGD
LDT_STOP#
8P4R-20KR
RN2
LDT_RST# L
LDT_PWRGD_L
LDT_STOP# L
8P4R-300R-RH
RN3
X_8P4R-0R
U39A
U39B
U39C
U39D
LVC07A_SOIC14
R22
10KR0402
VCC3
PWROK_PWM
R23
0R0402
R24
X_4.7KR0402
R25
1KR1%0402
R26
510R
R27
510R
R41
X_4.7KR0402
Q3
X_N-MMBT3904_NL_SOT23
R20
300R0402
For S3 issue(LDT RST can not still low)
VCC_DDR
VCCA_1V2
Micro Star Restricted Secret
Title
ATHLON64 HT I/F CTRL & DEBUG
Rev
1.0
Document Number
MS-7388
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date:
Tuesday, August 07, 2007
Sheet
3 of 39


6,7 MEM_MA_DQS_L[7..0]
6,7 MEM_MA_DQS_H[7..0]
6,7 MEM_MA_DM[7..0]
6,7 MEM_MB_DQS_L[7..0]
6,7 MEM_MB_DQS_H[7..0]
6,7 MEM_MB_DM[7..0]
CPU3B
MEMORY INTERFACE A
MEM_MA_DATA[63..0] 6,7
CPU3C
MEMORY INTERFACE B
MEM_MB_DATA[63..0] 6,7
6,7,8 MEM_MA_ADD[15..0]
6,7,8 MEM_MB_ADD[15..0]
Micro Star Restricted Secret
Title
ATHLON64 DDR MEMORY I/F
Rev
1.0
Document Number
MS-7388
MICRO-STAR INT'L CO.,LTD.
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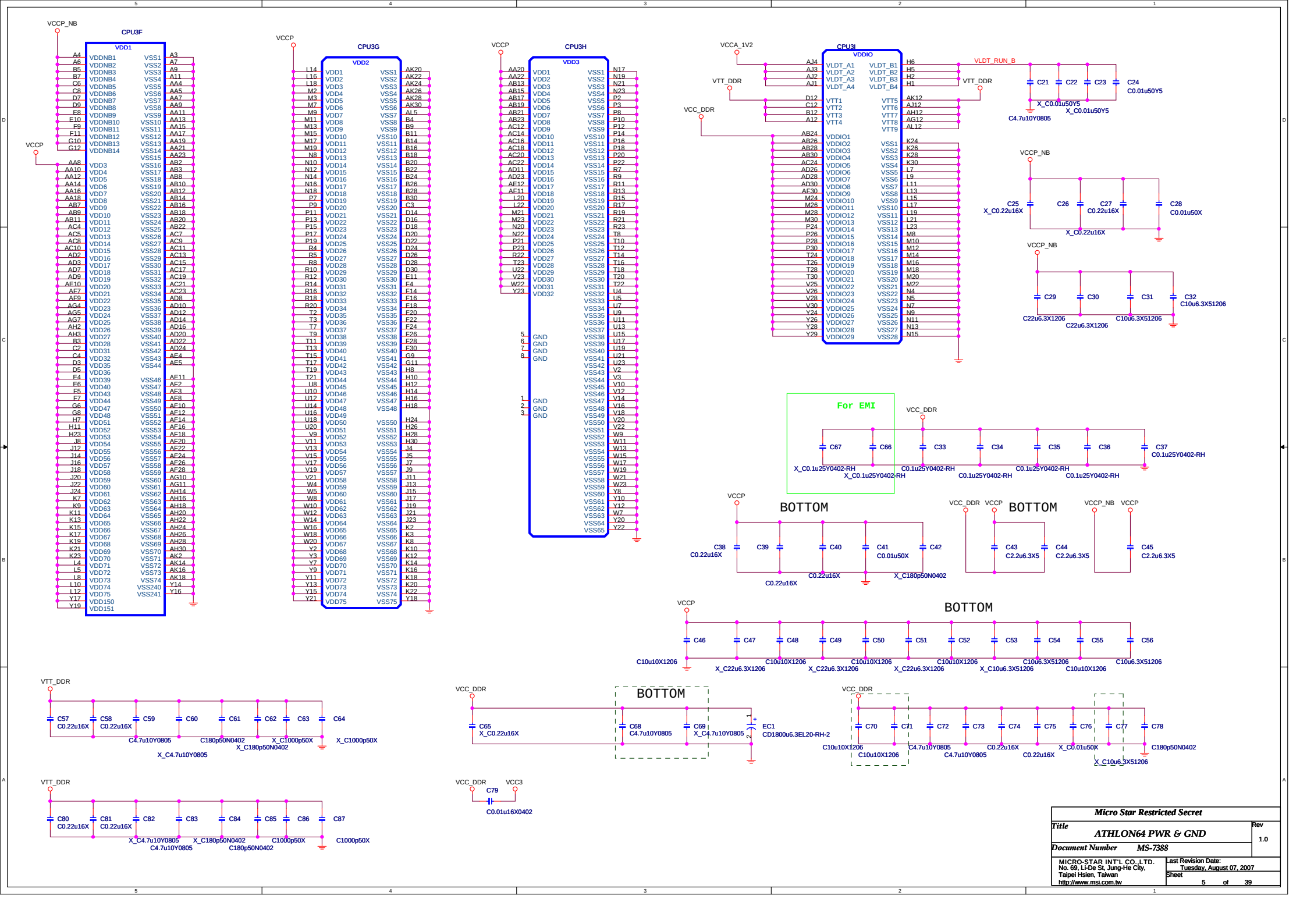
Sheet
4 of 39


CPU3F
VDD1
CPU3G
VDD2
CPU3H
VDD3
CPU3I
VDDIO
VCCP_NB
VCCP
VCC_DDR
VTT_DDR
VCCA_1V2
VLDT_RUN_B
For EMI
BOTTOM
BOTTOM
BOTTOM
Micro Star Restricted Secret
Title
ATHLON64 PWR & GND
Rev
1.0
Document Number
MS-7388
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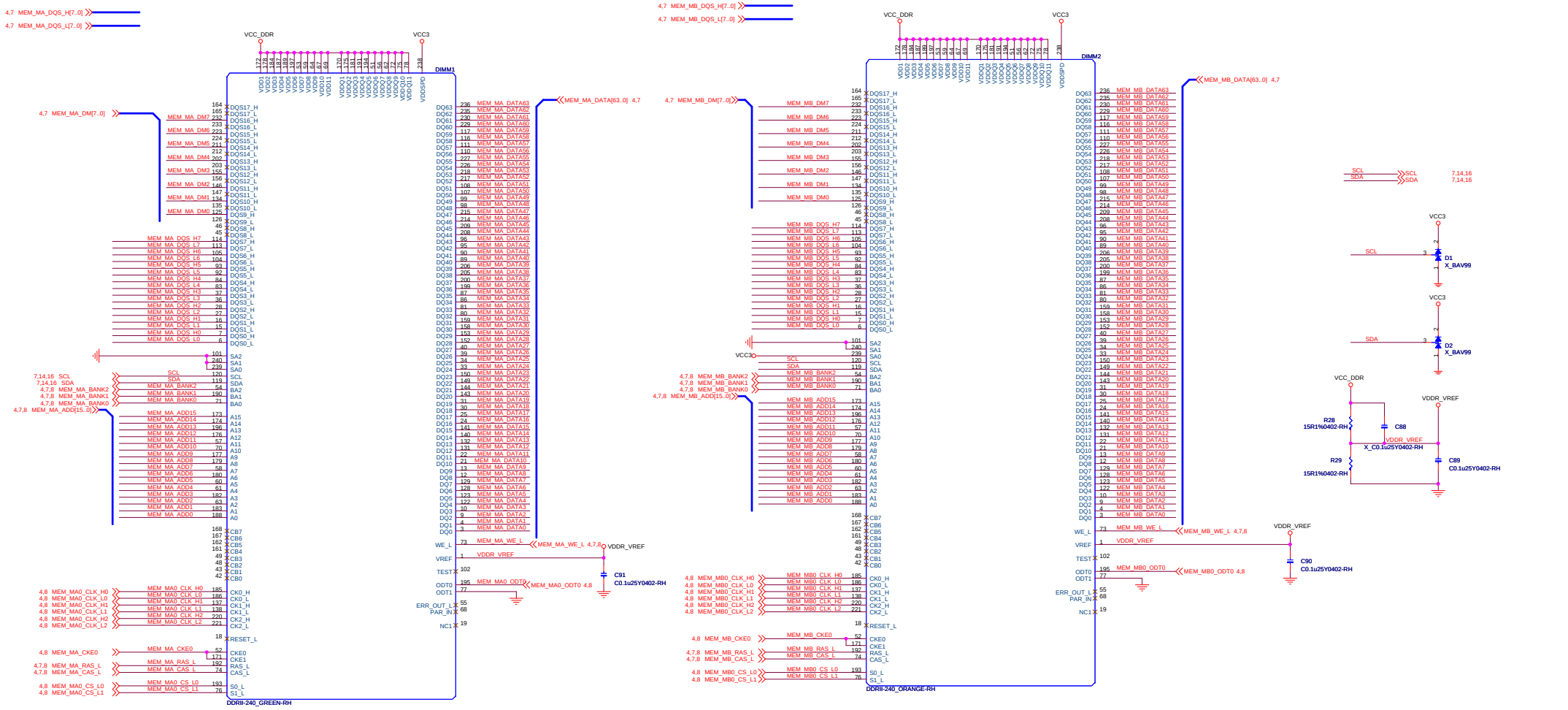
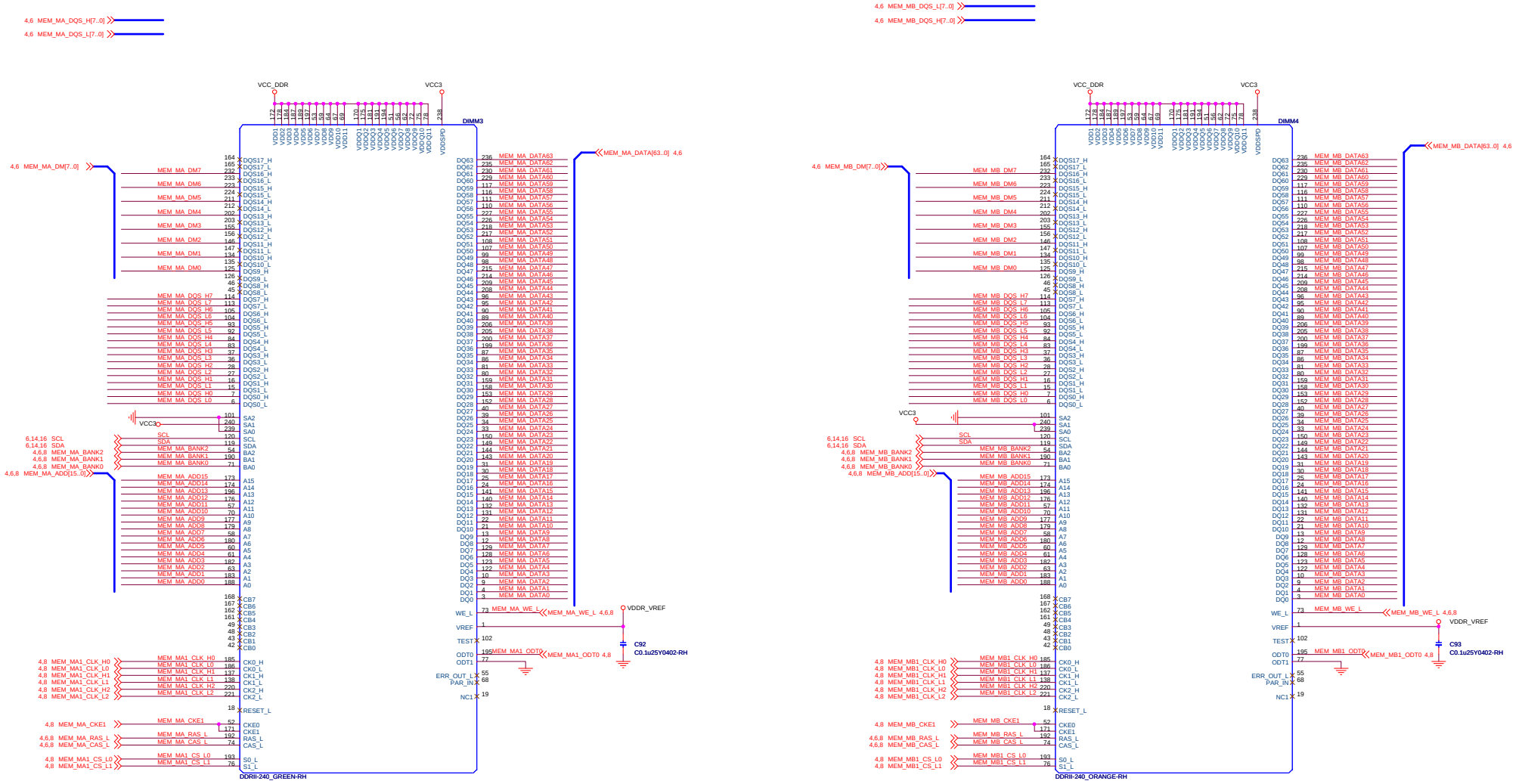
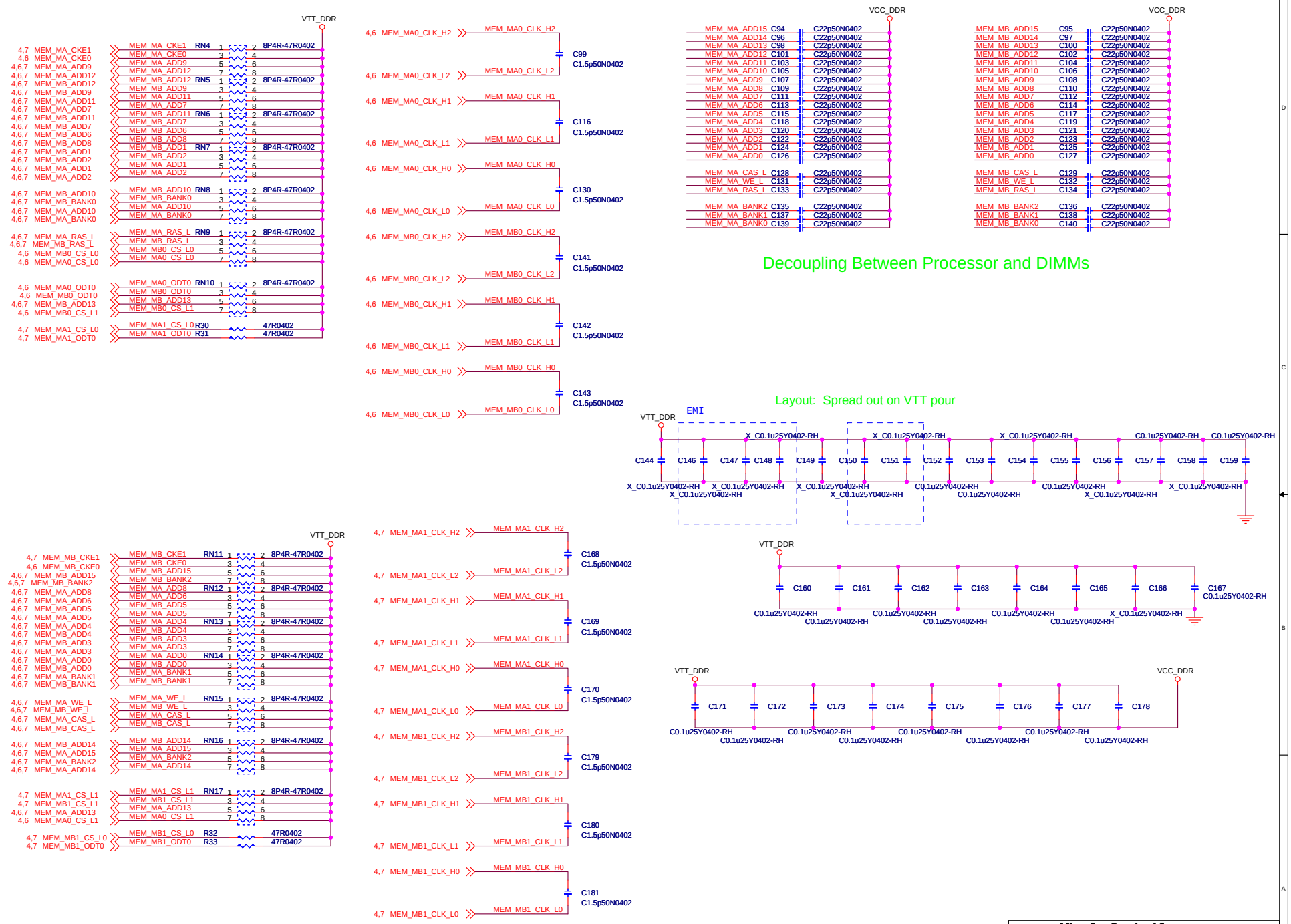
Last Revision Date:
Tuesday, August 07, 2007
Sheet
5 of 39



Micro Star Restricted Secret	
Title: FIRST LOGICAL DDR DIMM	Rev: 1.0
Document Number: MS-7388	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, August 01, 2007
	Sheet 6 of 39



Micro Star Restricted Secret		
Title	**SECOND LOGICAL DDR DIMM**	Rev 1.0
Document Number	*MS-7388*	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, August 01, 2007	Sheet 7 of 39



Micro Star Restricted Secret		
Title: DDR Terminatior		Rev: 1.0
Document Number: MS-7388		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, August 01, 2007	Sheet 8 of 39

3 HT_CADIN_H[15..0] → HT_CADIN_H[15..0]

3 HT_CADIN_L[15..0] → HT_CADIN_L[15..0]

3 HT_CADOUT_H[15..0] → HT_CADOUT_H[15..0]

3 HT_CADOUT_L[15..0] → HT_CADOUT_L[15..0]

U40A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

HT_CADOUT_H0	Y25	HT_RXCAD0P	HT_TXCAD0P	D24	HT_CADIN_H0
HT_CADOUT_L0	Y24	HT_RXCAD0N	HT_TXCAD0N	D25	HT_CADIN_L0
HT_CADOUT_H1	V22	HT_RXCAD1P	HT_TXCAD1P	E24	HT_CADIN_H1
HT_CADOUT_L1	V23	HT_RXCAD1N	HT_TXCAD1N	E25	HT_CADIN_L1
HT_CADOUT_H2	V25	HT_RXCAD2P	HT_TXCAD2P	F24	HT_CADIN_H2
HT_CADOUT_L2	V24	HT_RXCAD2N	HT_TXCAD2N	F25	HT_CADIN_L2
HT_CADOUT_H3	U24	HT_RXCAD3P	HT_TXCAD3P	F23	HT_CADIN_H3
HT_CADOUT_L3	U25	HT_RXCAD3N	HT_TXCAD3N	F22	HT_CADIN_L3
HT_CADOUT_H4	T25	HT_RXCAD4P	HT_TXCAD4P	H23	HT_CADIN_H4
HT_CADOUT_L4	T24	HT_RXCAD4N	HT_TXCAD4N	H22	HT_CADIN_L4
HT_CADOUT_H5	P22	HT_RXCAD5P	HT_TXCAD5P	J25	HT_CADIN_H5
HT_CADOUT_L5	P23	HT_RXCAD5N	HT_TXCAD5N	J24	HT_CADIN_L5
HT_CADOUT_H6	P25	HT_RXCAD6P	HT_TXCAD6P	K24	HT_CADIN_H6
HT_CADOUT_L6	P24	HT_RXCAD6N	HT_TXCAD6N	K25	HT_CADIN_L6
HT_CADOUT_H7	N24	HT_RXCAD7P	HT_TXCAD7P	K23	HT_CADIN_H7
HT_CADOUT_L7	N25	HT_RXCAD7N	HT_TXCAD7N	K22	HT_CADIN_L7
HT_CADOUT_H8	AC24	HT_RXCAD8P	HT_TXCAD8P	F21	HT_CADIN_H8
HT_CADOUT_L8	AC25	HT_RXCAD8N	HT_TXCAD8N	G21	HT_CADIN_L8
HT_CADOUT_H9	AB25	HT_RXCAD9P	HT_TXCAD9P	G20	HT_CADIN_H9
HT_CADOUT_L9	AB24	HT_RXCAD9N	HT_TXCAD9N	H21	HT_CADIN_L9
HT_CADOUT_H10	AA24	HT_RXCAD10P	HT_TXCAD10P	J20	HT_CADIN_H10
HT_CADOUT_L10	AA25	HT_RXCAD10N	HT_TXCAD10N	J21	HT_CADIN_L10
HT_CADOUT_H11	Y22	HT_RXCAD11P	HT_TXCAD11P	J18	HT_CADIN_H11
HT_CADOUT_L11	Y23	HT_RXCAD11N	HT_TXCAD11N	K17	HT_CADIN_L11
HT_CADOUT_H12	W21	HT_RXCAD12P	HT_TXCAD12P	L19	HT_CADIN_H12
HT_CADOUT_L12	W20	HT_RXCAD12N	HT_TXCAD12N	J19	HT_CADIN_L12
HT_CADOUT_H13	V21	HT_RXCAD13P	HT_TXCAD13P	M19	HT_CADIN_H13
HT_CADOUT_L13	V20	HT_RXCAD13N	HT_TXCAD13N	L18	HT_CADIN_L13
HT_CADOUT_H14	U20	HT_RXCAD14P	HT_TXCAD14P	M21	HT_CADIN_H14
HT_CADOUT_L14	U21	HT_RXCAD14N	HT_TXCAD14N	P21	HT_CADIN_L14
HT_CADOUT_H15	U19	HT_RXCAD15P	HT_TXCAD15P	P18	HT_CADIN_H15
HT_CADOUT_L15	U18	HT_RXCAD15N	HT_TXCAD15N	M18	HT_CADIN_L15
3 HT_CLKOUT_H0	T22	HT_RXCLK0P	HT_TXCLK0P	H24	HT_CLKIN_H0 3
3 HT_CLKOUT_L0	T23	HT_RXCLK0N	HT_TXCLK0N	H25	HT_CLKIN_L0 3
3 HT_CLKOUT_H1	AB23	HT_RXCLK1P	HT_TXCLK1P	L21	HT_CLKIN_H1 3
3 HT_CLKOUT_L1	AA22	HT_RXCLK1N	HT_TXCLK1N	L20	HT_CLKIN_L1 3
3 HT_CTLOUT_H0	M22	HT_RXCTL0P	HT_TXCTL0P	M24	HT_CTLIN_H0 3
3 HT_CTLOUT_L0	M23	HT_RXCTL0N	HT_TXCTL0N	M25	HT_CTLIN_L0 3
3 HT_CTLOUT_H1	R21	HT_RXCTL1P	HT_TXCTL1P	P19	HT_CTLIN_H1 3
3 HT_CTLOUT_L1	R20	HT_RXCTL1N	HT_TXCTL1N	R18	HT_CTLIN_L1 3
R34 HT_RXCALP	C23	HT_RXCALP	HT_TXCALP	B24	HT_TXCALP R35
HT_RXCALN	A24	HT_RXCALN	HT_TXCALN	B25	HT_TXCALN
1.21KR1%0402					1.21KR1%0402

RS780(RX780)

RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780/RS780
HT_RXCALP	49.9R (GND)	1.21K
HT_RXCALN	49.9R (VDDHT)	
HT_TXCALP HT_TXCALN	100R	1.21K

REF

RD780

X_RD780

Micro Star Restricted Secret

Title RD780/RX780-HT LINK I/F	Rev 1.0
Document Number MS-7388	
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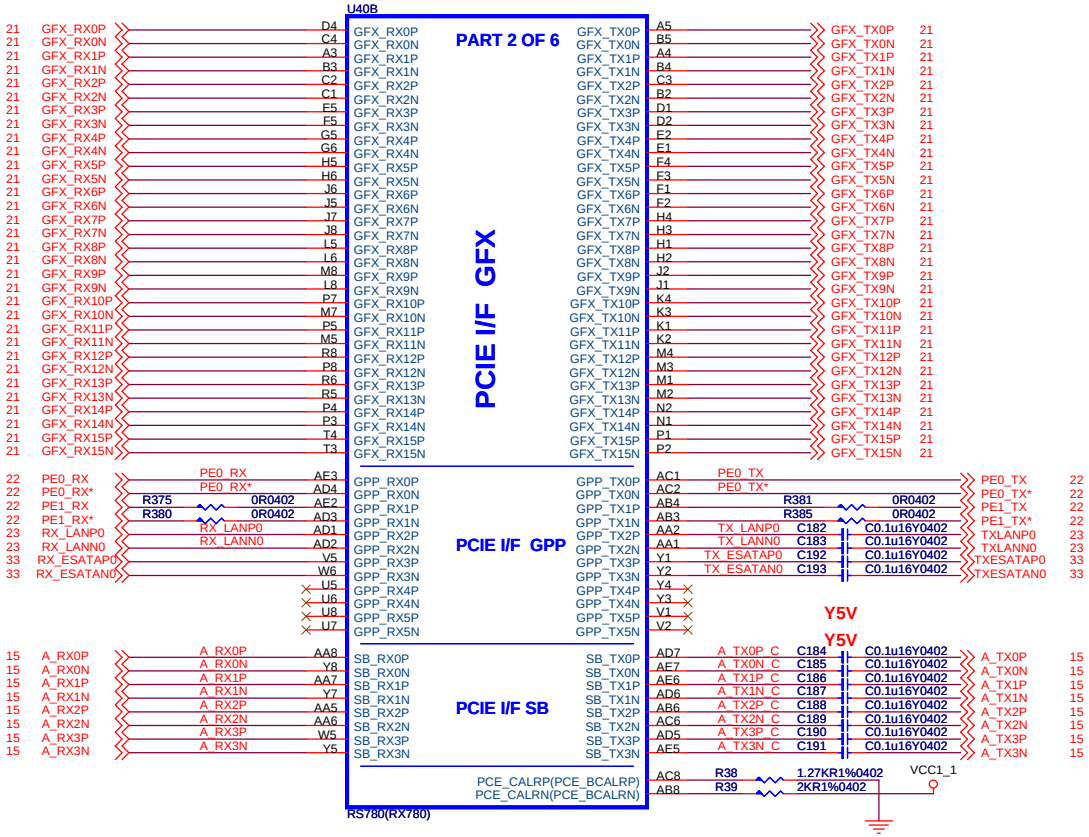

RX740/RS740/RS780 difference table (PCIE LINK)

	RS740	RX740/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

Micro Star Restricted Secret

Title *RD780/RX780-HT LINK I/F*	Rev 1.0
Document Number *MS-7388*	

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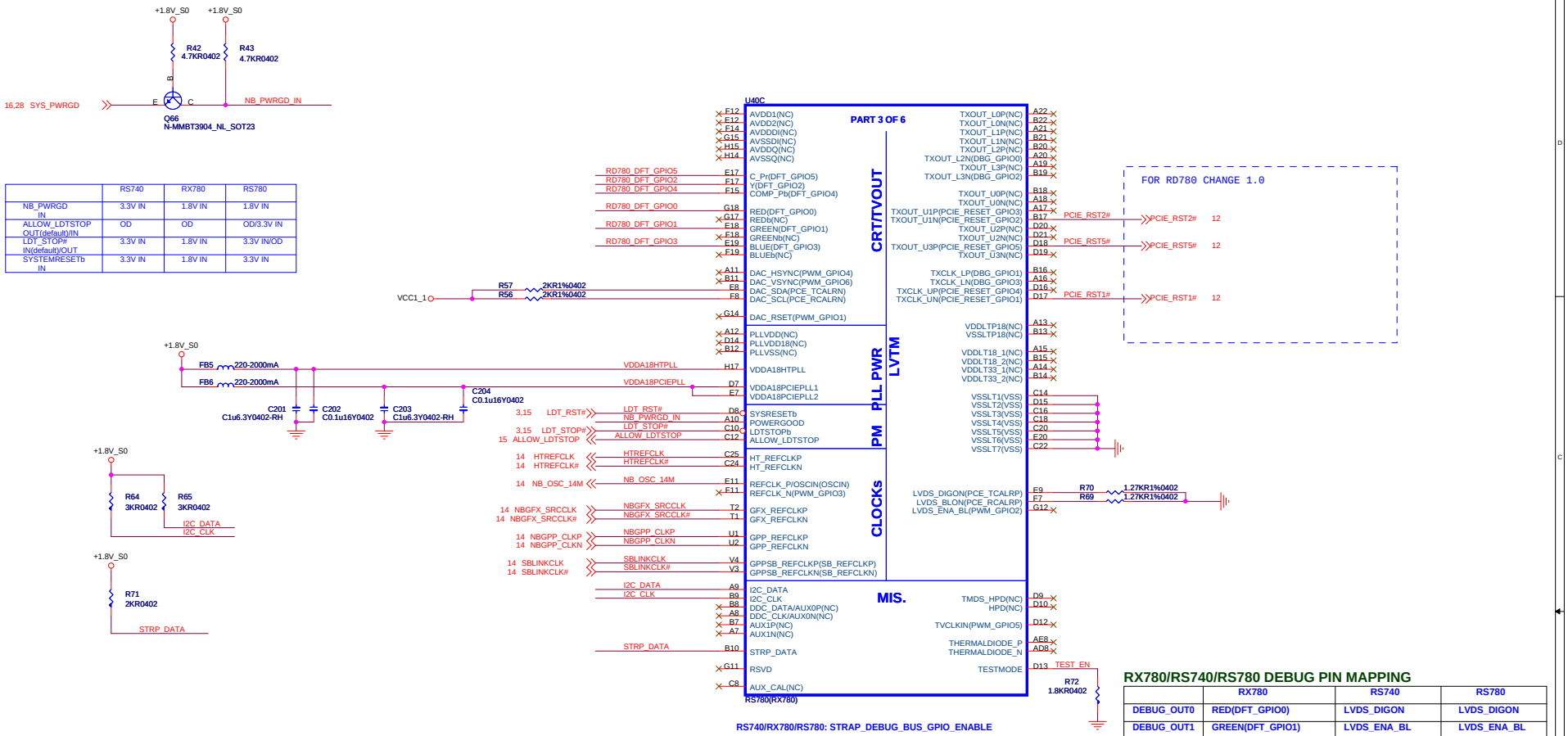
Last Revision Date: Wednesday, August 01, 2007
Sheet 10 of 39



	RS740	RX780	RS780
NB_PWRGD IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OD	OD	OD/3.3V IN
LDT_STOP# IN(default)/OUT	3.3V IN	1.8V IN	3.3V IN/OD
SYSTEMRESETb IN	3.3V IN	1.8V IN	3.3V IN

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

```
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740); Enable (RX780/RS780)
0 : Enable  (RS740); Disable(RX780/RS780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

```
111: 1-1-1-1-1-1   Mode L   default
110: 1-1-1-1-1-1   Mode L
101: 2-0-2-0-2-0   Mode C2
100: 2-0-2-0-1-1   Mode K
011: 2-0-1-1-1-1   Mode E
010: 1-1-1-1-1-1   Mode L
001: 4-0-0-0-1-1   Mode C
000: 4-0-0-0-2-0   Mode B
```

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#
```

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

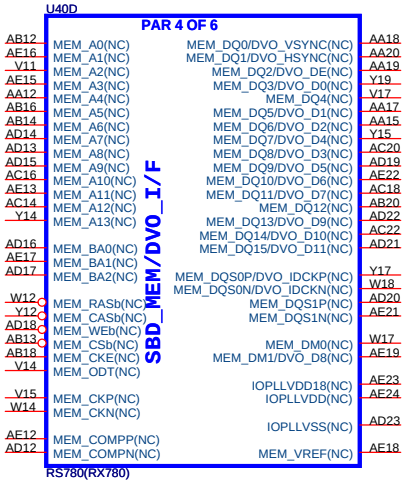
```
Enables Test debug bus
using PCIE bus
1.  Disable (can be enabled
     thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register
          setting only
RS740: Not supported
```

RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

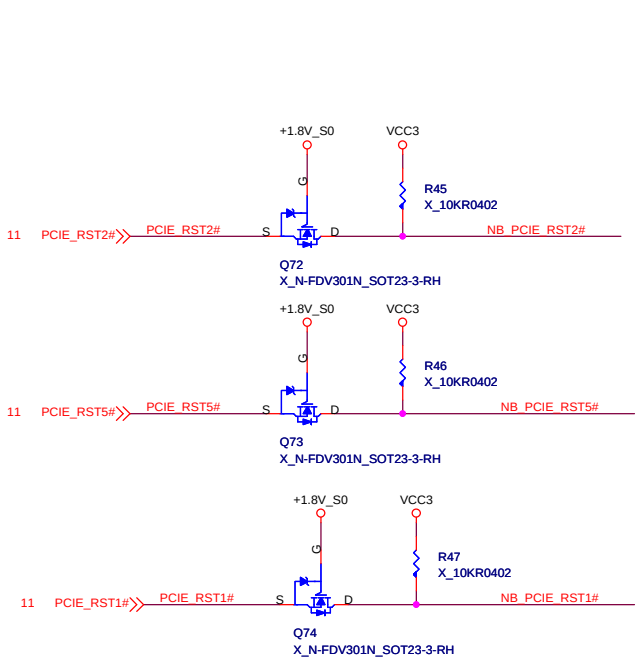
Micro Star Restricted Secret

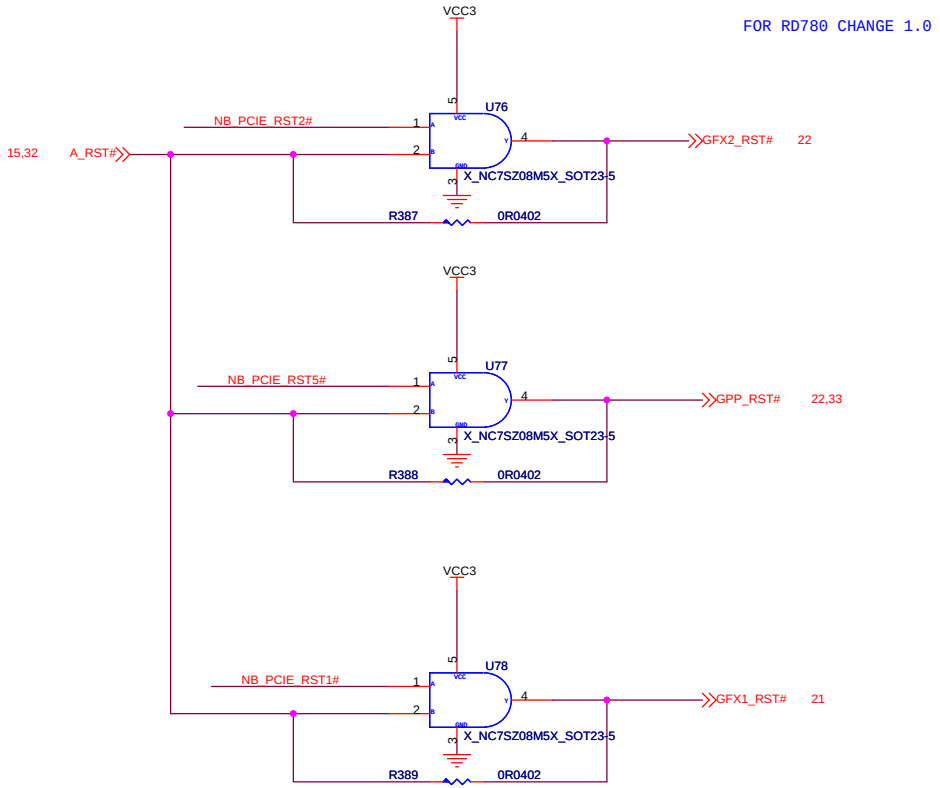
Title	RD780/RX780-HT LINK I/F
Rev	1.0
Document Number	MS-7388
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 07, 2007
	Sheet 11 of 39



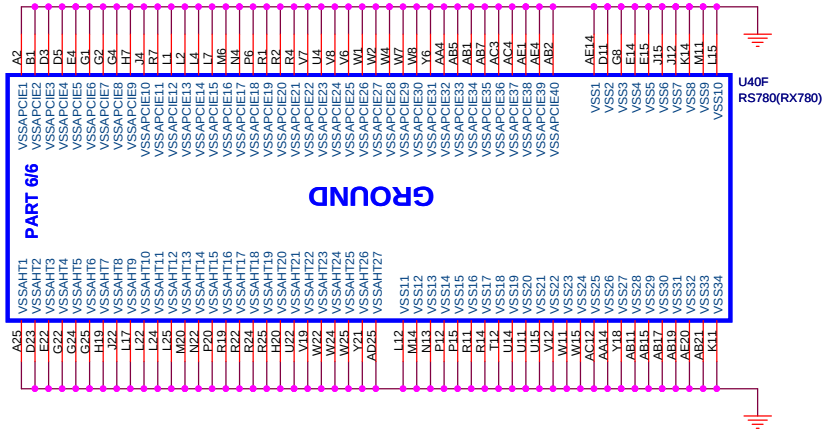
Note: If the Side-port memory interface is **not** used, make sure that:

- The memory interface IO power (VDD_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVDD18 is connected to 1.8 V and IOPLLVDD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT_GPIO0 is **not** connected to the GND.



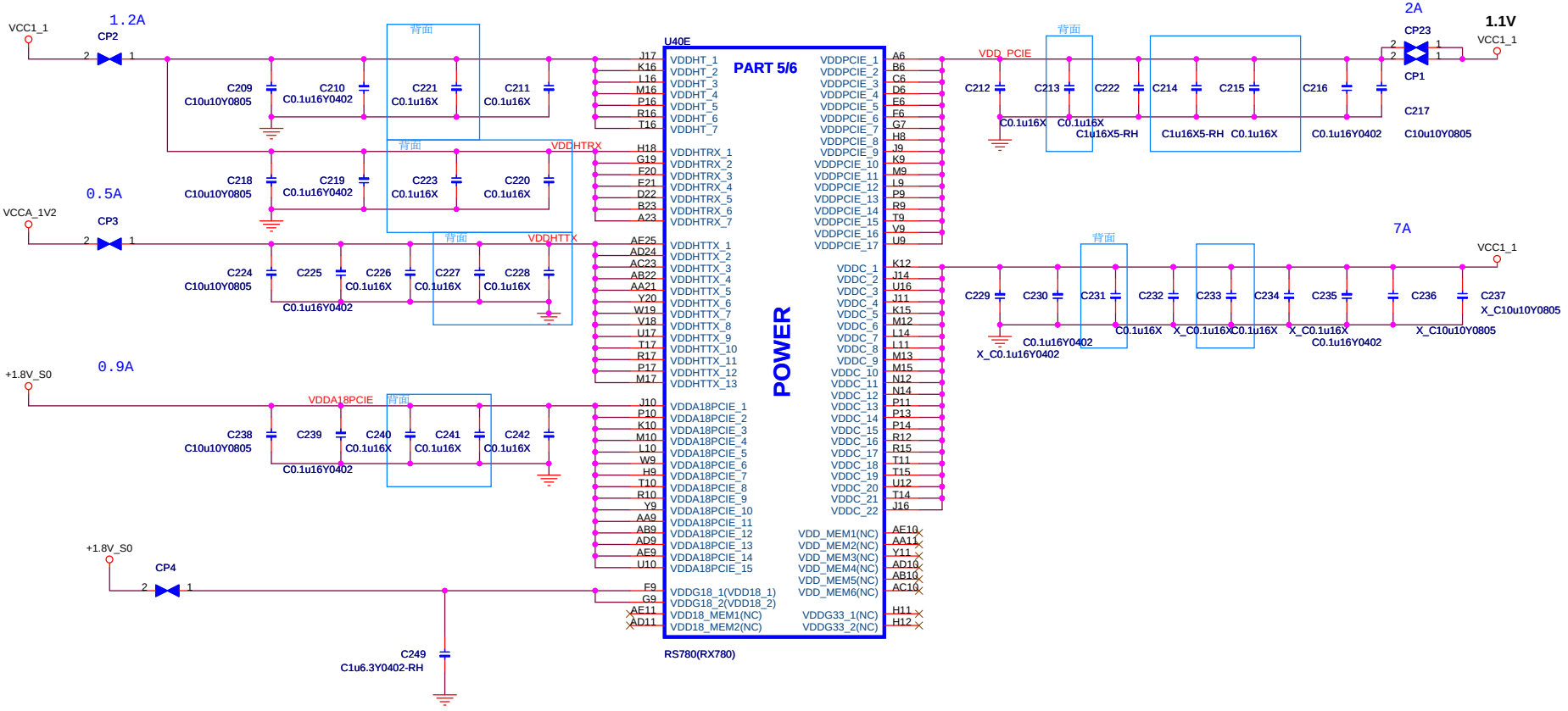


Micro Star Restricted Secret	
Title *RD780/RX780-HT LINK I/F*	Rev 1.0
Document Number *MS-7388*	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 07, 2007
	Sheet 12 of 39

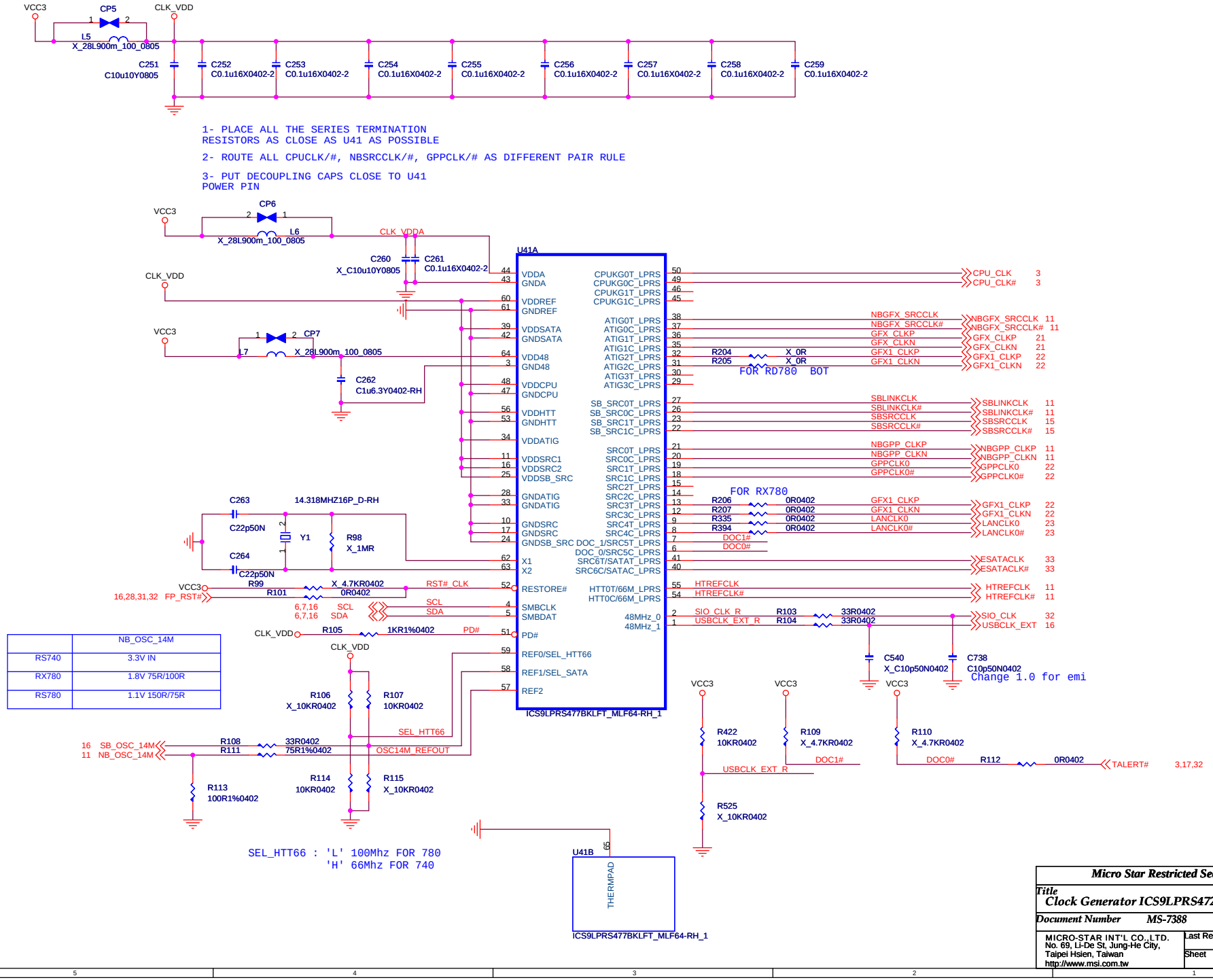


RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



Micro Star Restricted Secret	
Title: RD780/RX780-HT LINK I/F	Rev: 1.0
Document Number: MS-7388	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 07, 2007
	Sheet 13 of 39



	NB_OSC_14M
RS740	3.3V IN
RX780	1.8V 75R/100R
RS780	1.1V 150R/75R

Micro Star Restricted Secret

Title	Clock Generator ICS9LPRS472/RTM870T-691
Rev	1.0
Document Number	MS-7388
Last Revision Date:	Tuesday, August 07, 2007
Sheet	14 of 39

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Taipei Hsien, Taiwan
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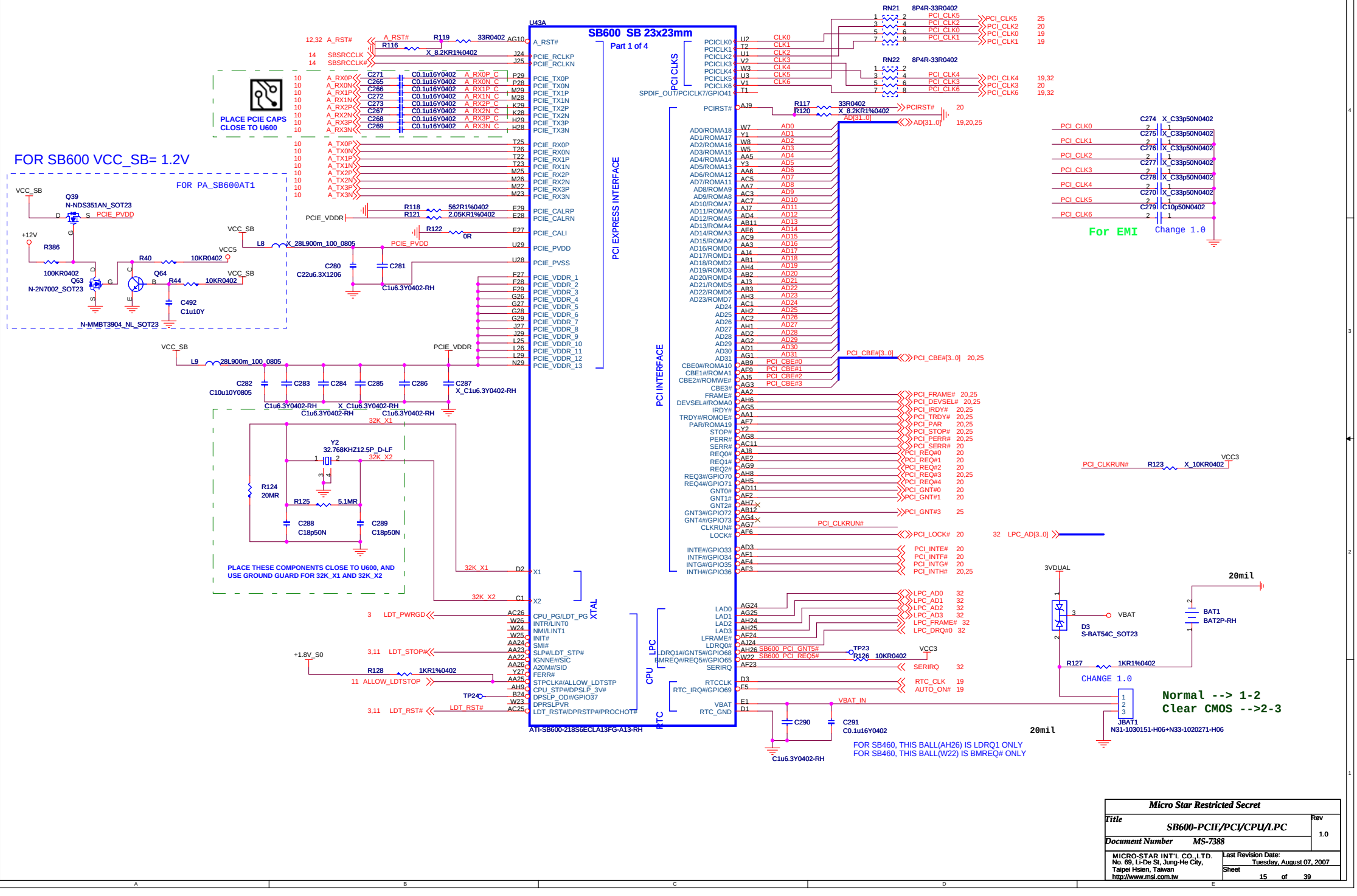
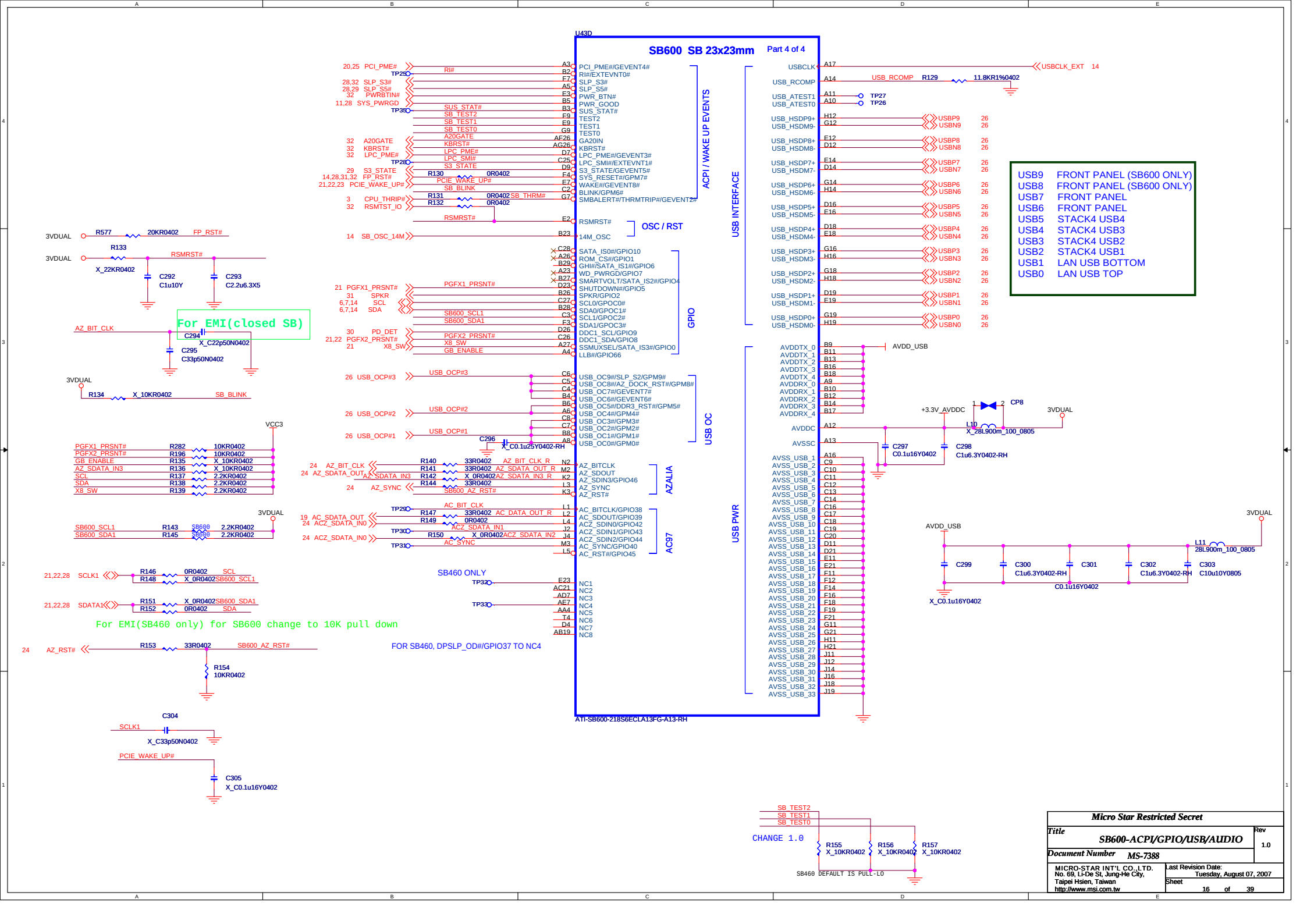

FOR SB600 VCC_SB= 1.2V
FOR PA_SB600AT1
PLACE PCIE CAPS CLOSE TO U600
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
U43A
SB600 SB 23x23mm
Part 1 of 4
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
CPU
LPC
RTC
ATI-SB600-218S6ECLA13FG-A13-RH
For EMI
Change 1.0
CHANGE 1.0
Normal --> 1-2
Clear CMOS -->2-3
FOR SB460, THIS BALL(AH26) IS LDRQ1 ONLY
FOR SB460, THIS BALL(W22) IS BMREQ# ONLY
Micro Star Restricted Secret
SB600-PCIE/PCI/CPU/LPC
MS-7388
1.0
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
Tuesday, August 07, 2007
15 of 39


U43D
SB600 SB 23x23mm Part 4 of 4
ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN
KBRST#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
RSMRST#
14M_OSC
SATA_IS0#/GPIO10
ROM_CS#/GPIO1
GHI#/SATA_IS1#/GPIO6
WD_PWRGD/GPIO7
SMARTVOLT/SATA_IS2#/GPIO4
SHUTDOWN#/GPIO5
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
SSMUXSEL/SATA_IS3#/GPIO0
LLB#/GPIO66
USB_OC9#/SLP_S2/GPM9#
USB_OC8#/AZ_DOCK_RST#/GPM8#
USB_OC7#/GEVENT7#
USB_OC6#/GEVENT6#
USB_OC5#/DDR3_RST#/GPM5#
USB_OC4#/GPM4#
USB_OC3#/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AC_BITCLK/GPIO38
AC_SDOUT/GPIO39
ACZ_SDIN0/GPIO42
ACZ_SDIN1/GPIO43
ACZ_SDIN2/GPIO44
AC_SYNC/GPIO40
AC_RST#/GPIO45
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
ATI-SB600-218S6ECLA13FG-A13-RH
USBCLK
USB_RCOMP
USB_ATEST1
USB_ATEST0
USB_HSDP9+
USB_HSDM9-
USB_HSDP8+
USB_HSDM8-
USB_HSDP7+
USB_HSDM7-
USB_HSDP6+
USB_HSDM6-
USB_HSDP5+
USB_HSDM5-
USB_HSDP4+
USB_HSDM4-
USB_HSDP3+
USB_HSDM3-
USB_HSDP2+
USB_HSDM2-
USB_HSDP1+
USB_HSDM1-
USB_HSDP0+
USB_HSDM0-
AVDDTX_0
AVDDTX_1
AVDDTX_2
AVDDTX_3
AVDDTX_4
AVDDRX_0
AVDDRX_1
AVDDRX_2
AVDDRX_3
AVDDRX_4
AVDDC
AVSSC
AVSS_USB_1
AVSS_USB_2
AVSS_USB_3
AVSS_USB_4
AVSS_USB_5
AVSS_USB_6
AVSS_USB_7
AVSS_USB_8
AVSS_USB_9
AVSS_USB_10
AVSS_USB_11
AVSS_USB_12
AVSS_USB_13
AVSS_USB_14
AVSS_USB_15
AVSS_USB_16
AVSS_USB_17
AVSS_USB_18
AVSS_USB_19
AVSS_USB_20
AVSS_USB_21
AVSS_USB_22
AVSS_USB_23
AVSS_USB_24
AVSS_USB_25
AVSS_USB_26
AVSS_USB_27
AVSS_USB_28
AVSS_USB_29
AVSS_USB_30
AVSS_USB_31
AVSS_USB_32
AVSS_USB_33
USB9 FRONT PANEL (SB600 ONLY)
USB8 FRONT PANEL (SB600 ONLY)
USB7 FRONT PANEL
USB6 FRONT PANEL
USB5 STACK4 USB4
USB4 STACK4 USB3
USB3 STACK4 USB2
USB2 STACK4 USB1
USB1 LAN USB BOTTOM
USB0 LAN USB TOP
For EMI(closed SB)
For EMI(SB460 only) for SB600 change to 10K pull down
SB460 ONLY
FOR SB460, DPSLP_OD#/GPIO37 TO NC4
CHANGE 1.0
SB460 DEFAULT IS PULL-LO
Micro Star Restricted Secret
Title
SB600-ACPI/GPIO/USB/AUDIO
Rev
1.0
Document Number
MS-7388
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date:
Tuesday, August 07, 2007
Sheet
16 of 39

FOR SB600

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

SB600 SB 23x23mm
Part 2 of 4

SERIAL ATA

SERIAL ATA POWER

ATA 66/100

SPI ROM

HW MONITOR

PLACE R665 CLOSE TO U600 BALL

R674 IS 1K 1% FOR XTAL, 4.99K 1% FOR INTERNAL CLK

C658 CLOSE TO THE BALL OF U600

C659 & C660 CLOSE TO THE BALLS OF U600

Only for SB600

NS_VIA CONNECTS HWM_AGND TO GND

背面

ATI-SB600-218S6ECLA13FG-A13-RH

SST SPI ROM

W25X80VSSIG-RH

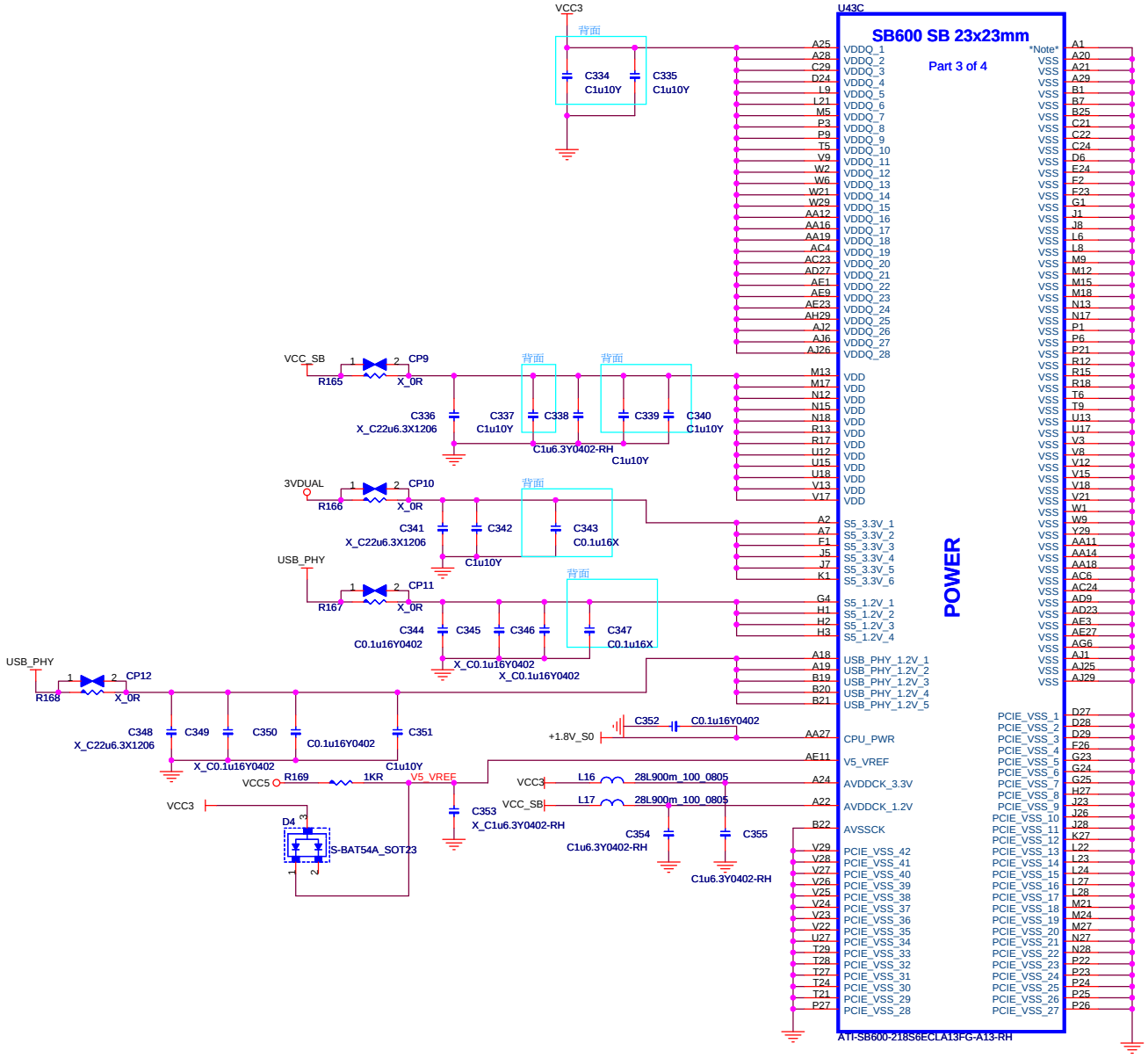
SPI FLASH MEMORY

SPI DEBUG PORT
Place close to SPI ROM

H2X5[1]M-2PITCH_BLACK-RH

Part Number : N31-2051451-H06

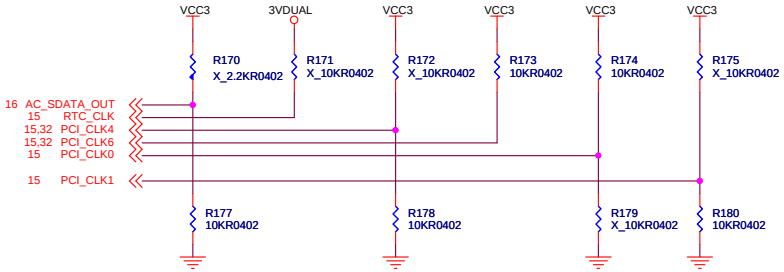
Micro Star Restricted Secret	
Title	SB600-SATA/IDE/HWM/SPI
Rev	1.0
Document Number	MS-7388
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Thursday, August 02, 2007
	Sheet 17 of 39



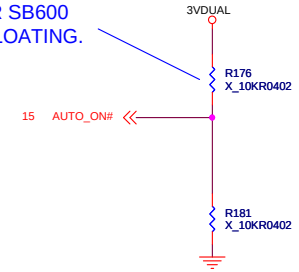
Micro Star Restricted Secret		
Title	*SB600-POWER & DECOUPLING*	Rev 1.0
Document Number	*MS-7388*	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Thursday, August 02, 2007 Sheet 18 of 39	

REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT, 15K PU FOR RTC_CLK, EXTERNAL PU/PD IS NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE REQUIRED



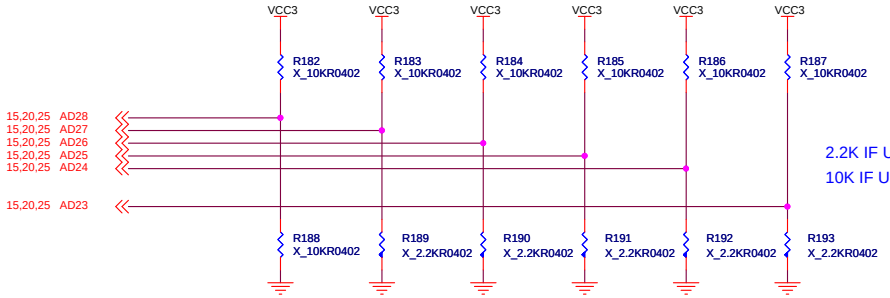
NOTE: R PU RESISTOR FOR RTC_IRQ# IS REQUIRED FOR SB600 TO KEEP THE INPUT FROM FLOATING.



					SB600	
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM DEFAULT L, H = LPC ROM L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



2.2K IF USED FOR SB600.
10K IF USED FOR SB460.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB600 ONLY

SB600 ONLY

FOR SB460, PCI_AD23 IS RESERVED

Title	SB600-STRAPS
Rev	1.0
Document Number	MS-7388

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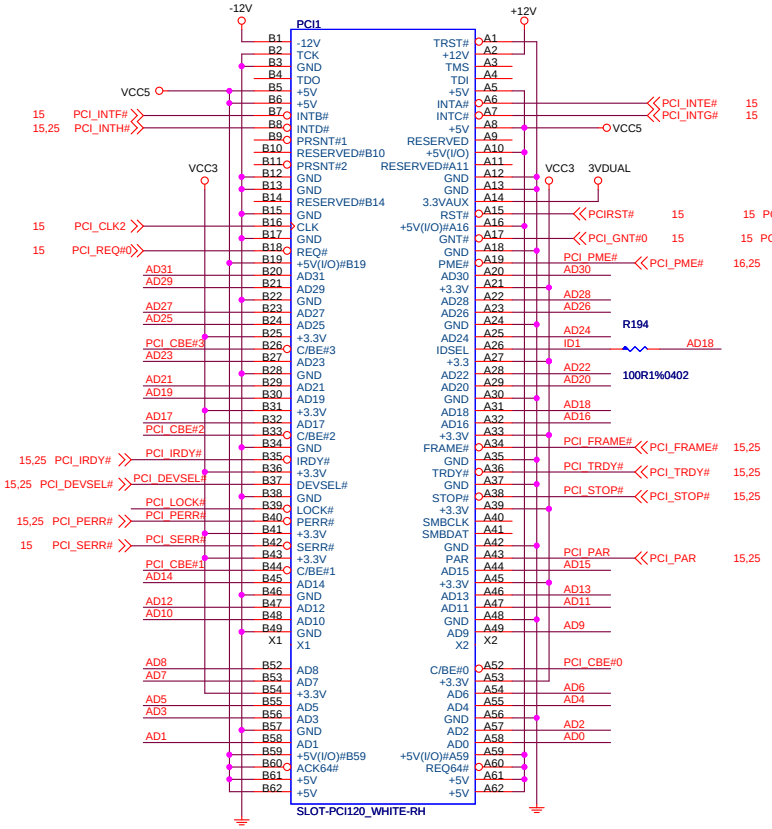
http://www.msi.com.tw

Last Revision Date: Wednesday, August 01, 2007

15,19,25 AD[31..0] AD[31..0]

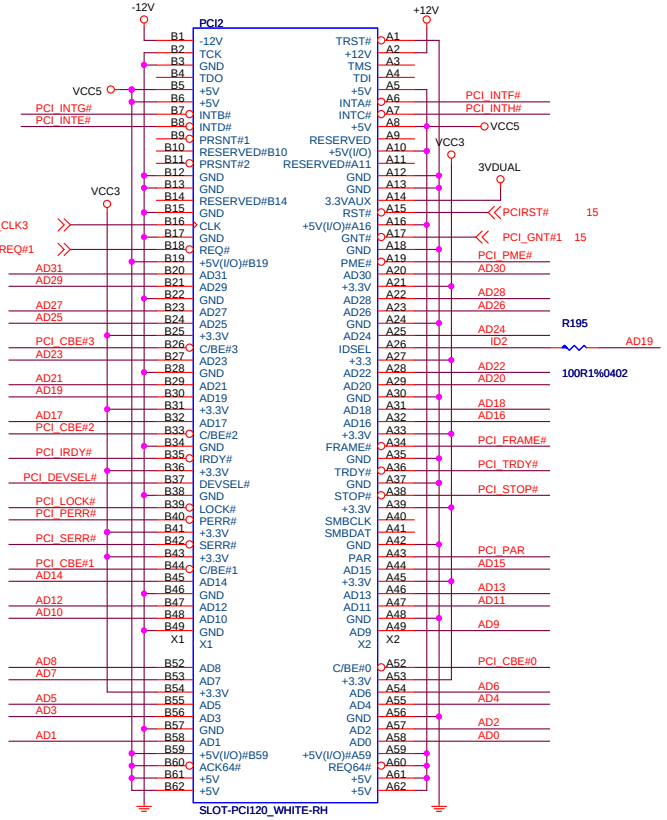
15,25 PCI_CBE#[3..0] PCI_CBE#[3..0]

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



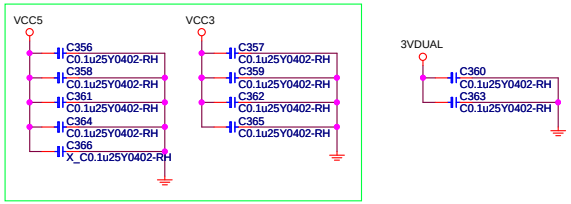
IDSEL = AD18
MASTER = PCI_REQ#0
PCI_GNT#0

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



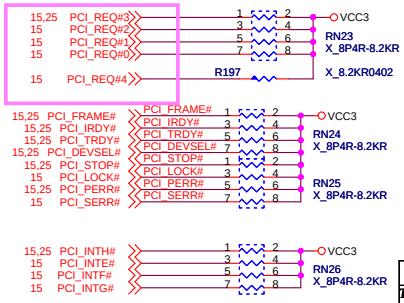
IDSEL = AD19
MASTER = PCI_REQ#1
PCI_GNT#1

PCI SLOT DECOUPLING CAPACITORS



For EMI

PCI PULL-UP / DOWN RESISTORS



Micro Star Restricted Secret

Title	PCI Slot 1,2 & PCI Extender	Rev 1.0
Document Number	MS-7388	

MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw

Last Revision Date: Wednesday, August 01, 2007

Sheet 20 of 39

PCI EXPRESS_16

Trace width > 100 mils

PCI_EX1

PCI EXPRESS X16 POART

X_CD270u16SO-RH-2

FOR RX780 ONLY EC3

EC2 X_CD470u16EL11.5

EC3 CD470u16EL11.5

C399 C0.1u25Y0402-RH

C401 C0.1u25Y0402-RH

EC4 CD1000u63EL11.5-RH-1

C402 C0.1u25Y0402-RH

C404 C0.1u25Y0402-RH

C400 C0.1u25Y0402-RH

C403 C0.1u25Y0402-RH

For EMI

RN40 RN44 RN47 RN48 RN45 RN46 RN49 RN50

8P4R-0R

FOR RX780

FOR RD780

CHANGE 1.0

R198 X_4.7KR0402

R199 X_4.7KR0402

R390 X_0R0402

R393 X_0R0402

R391 X_0R0402

Q8 X_N-FDV301N_SOT23-3-RH

X8_SW low for X16

U45 U46 U47 U48

X_PI2PCIE2412ZHE_TQFN42-RH

GND

Micro Star Restricted Secret

Title	PCI-E X16 , X1 Slot
Rev	1.0
Document Number	MS-7388
Last Revision Date	Wednesday, August 08, 2007
Sheet	21 of 39

MICRO-STAR INT'L CO.,LTD.
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http://www.msi.com.tw

PCI EXPRESS_16

FOR RX780 PCI-EX1

Trace width > 100 mils

PCI_EX2

Near Connector

R201 X_10KR0402

R202 X_0R0402

REF2

SLOT

X_PCI EXPRESS X16 POART

PCI EXPRESS X16 POART

PCI-Express x1 SLOT 1

PCI_EX3

Near Connector

R203 X_10KR0402

PCIE X1

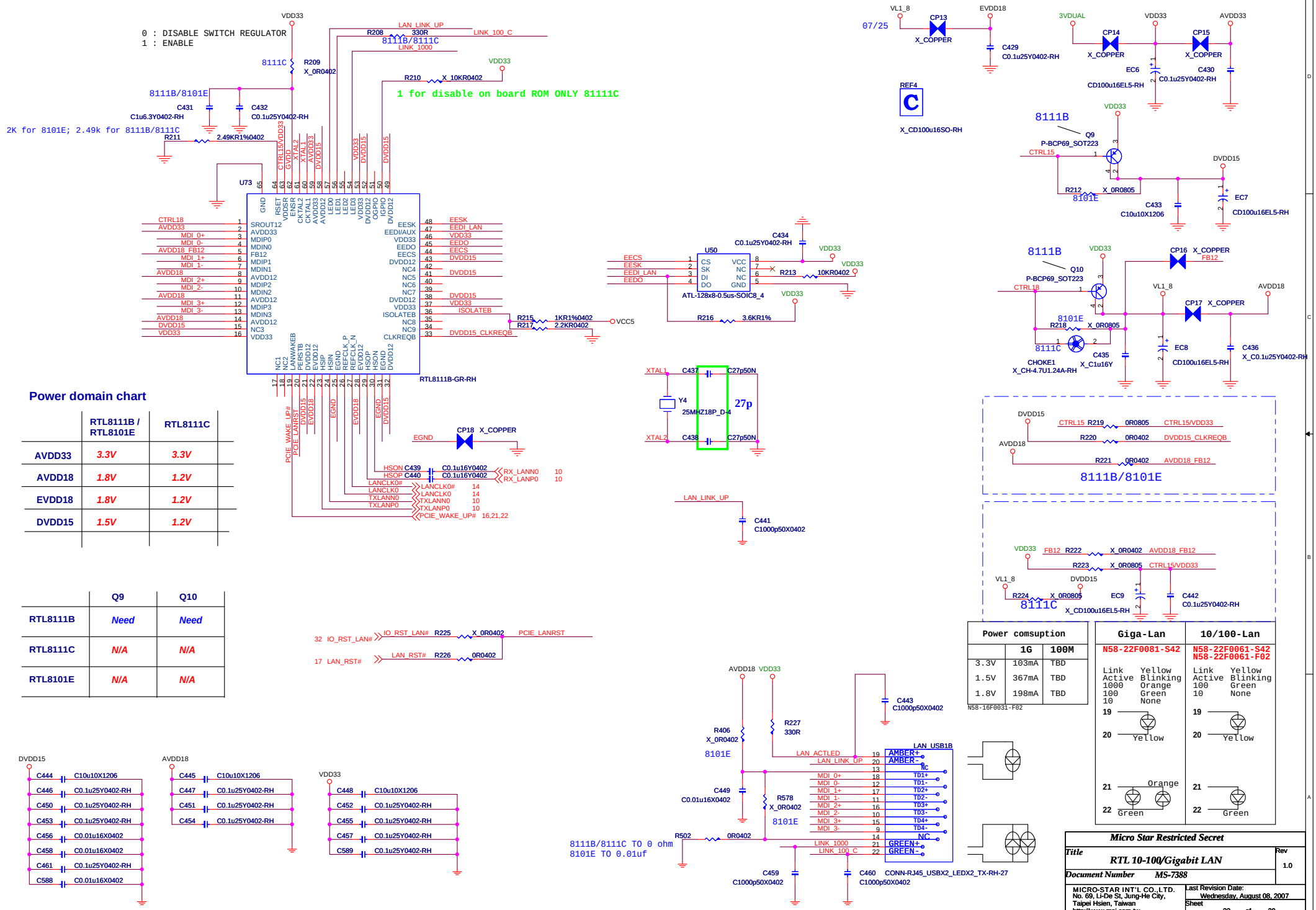
RN51

8P4R-0R

FOR RX780

For EMI

Micro Star Restricted Secret	
Title: PCI-E X16 Slot 3 , 4	Rev: 1.0
Document Number: MS-7388	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, August 01, 2007
	Sheet 22 of 39


0 : DISABLE SWITCH REGULATOR
1 : ENABLE
1 for disable on board ROM ONLY 81111C
2K for 8101E; 2.49k for 8111B/8111C
8111B/8101E
8111C
8111B
RTL8111B-GR-RH
ATL-128x8-0.5us-SOIC8_4
25MHZ18P_D-4
CHOKE1
X_CH-4.7U1.24A-RH
LAN_USB1B
CONN-RJ45_USBX2_LEDX2_TX-RH-27
8111B/8111C TO 0 ohm
8101E TO 0.01uf
07/25
REF4
X_CD100u16SO-RH
Power domain chart
RTL8111B / RTL8101E
RTL8111C
AVDD33 3.3V 3.3V
AVDD18 1.8V 1.2V
EVDD18 1.8V 1.2V
DVDD15 1.5V 1.2V
Q9
Q10
RTL8111B Need Need
RTL8111C N/A N/A
RTL8101E N/A N/A
Power comsuption
1G
100M
3.3V 103mA TBD
1.5V 367mA TBD
1.8V 198mA TBD
N58-16F0031-F02
Giga-Lan
N58-22F0081-S42
10/100-Lan
N58-22F0061-S42
N58-22F0061-F02
Link Active 1000 100 10
Yellow Blinking Orange Green None
Micro Star Restricted Secret
Title
RTL 10-100/Gigabit LAN
Rev
1.0
Document Number
MS-7388
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
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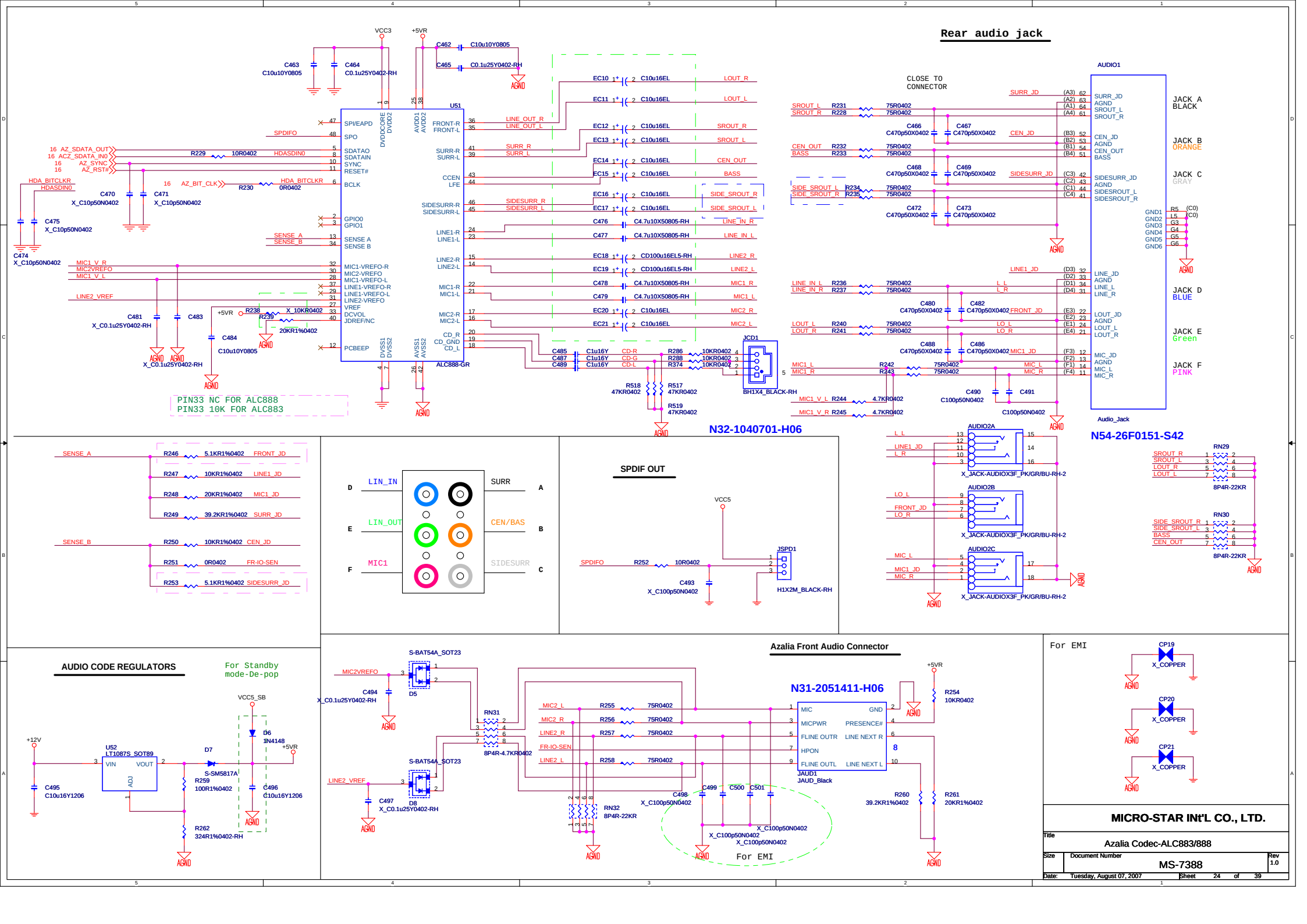
http://www.msi.com.tw
Last Revision Date:
Wednesday, August 08, 2007
Sheet
23
of
39


Rear audio jack
CLOSE TO CONNECTOR
AUDIO1
JACK A BLACK
JACK B ORANGE
JACK C GRAY
JACK D BLUE
JACK E Green
JACK F PINK
Audio_Jack
U51
ALC888-GR
N32-1040701-H06
N54-26F0151-S42
PIN33 NC FOR ALC888
PIN33 10K FOR ALC883
SPDIF OUT
JSPD1
H1X2M_BLACK-RH
JCD1
BH1X4_BLACK-RH
AUDIO2A
AUDIO2B
AUDIO2C
X_JACK-AUDIOX3F_PK/GR/BU-RH-2
RN29
RN30
8P4R-22KR
AUDIO CODE REGULATORS
For Standby mode-De-pop
U52
LT1087S_SOT89
S-SM5817A
Azalia Front Audio Connector
N31-2051411-H06
JAUD1
JAUD_Black
For EMI
CP19
CP20
CP21
X_COPPER
MICRO-STAR INt'L CO., LTD.
Azalia Codec-ALC883/888
MS-7388
Rev 1.0
Tuesday, August 07, 2007
Sheet 24 of 39

1394a OHCI Link Layer Controller

VT6308P/VT6308S

IDSEL = AD16
MASTER = PCI_REQ#3
PCI_GNT#3

ENABLE I2C EEPROM : R271 STUFF
DISABLE I2C EEPROM : R271 EMPTY

ENABLE EXTERAL EEPROM : R273 EMPTY
DISABLE EXTRRAL EEPROM : R273 STUFF

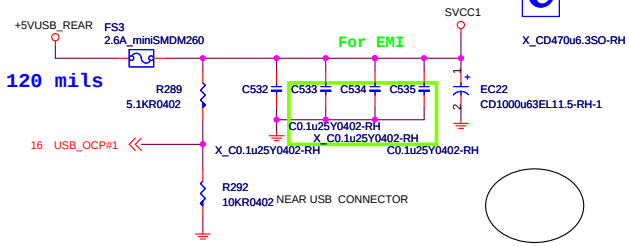
NEAR CHIP

NEAR CHIP

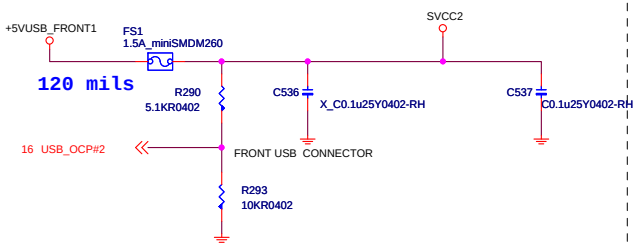
For Intel 1394 pinheader

Micro Star Restricted Secret	
Title: 1394a Link Layer Controller	Rev: 1.0
Document Number: MS-7388	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 07, 2007
	Sheet 25 of 39

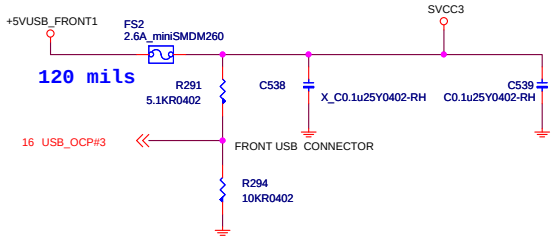
POWER CIRCUIT FOR USB PORT 0,1



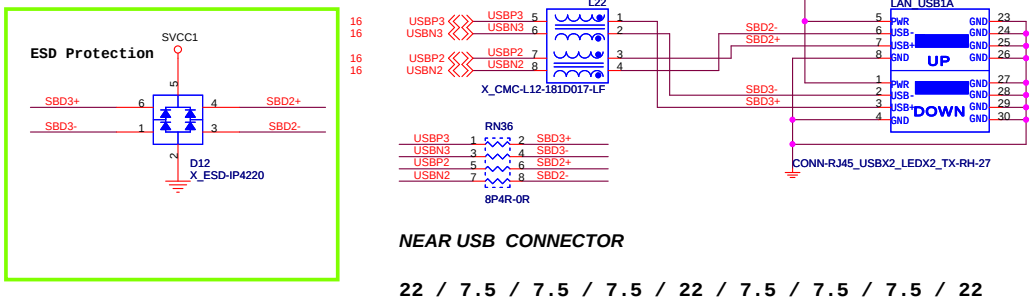
POWER CIRCUIT FOR USB PORT 4,5



POWER CIRCUIT FOR USB PORT 6.7.8.9



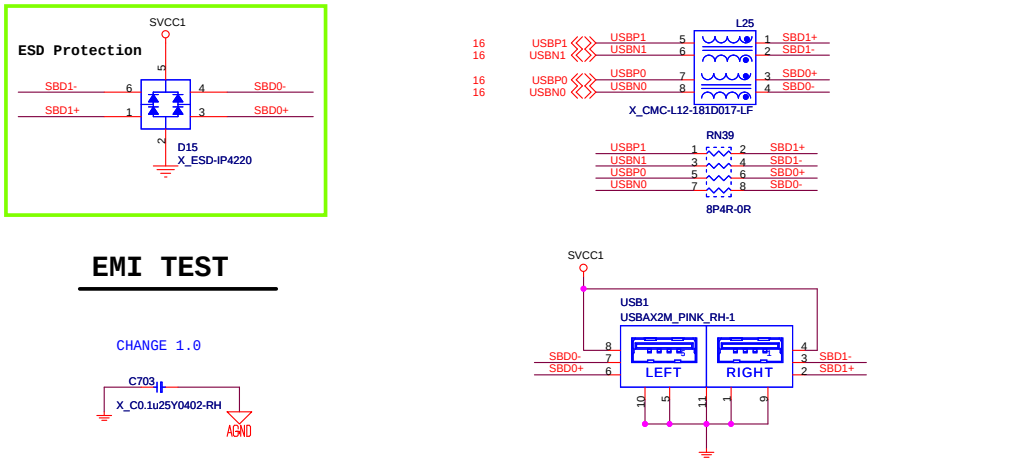
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

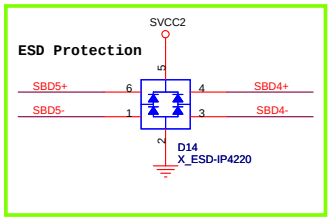
REAR PANEL USB CONNECTOR FOR USB PORT 0,1

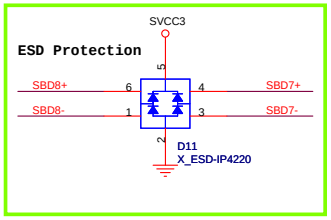


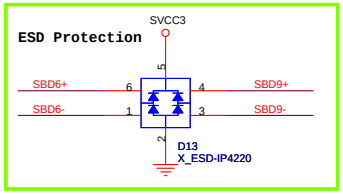
EMI TEST

CHANGE 1.0

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

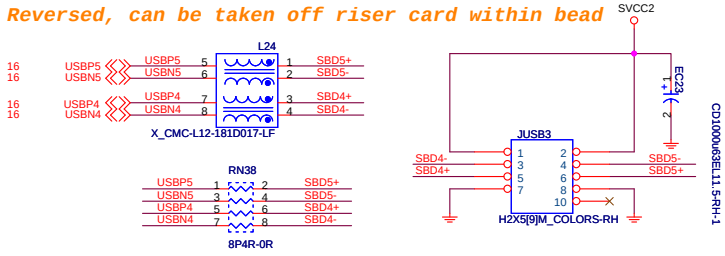




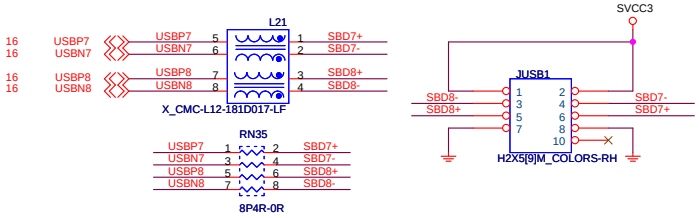


FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

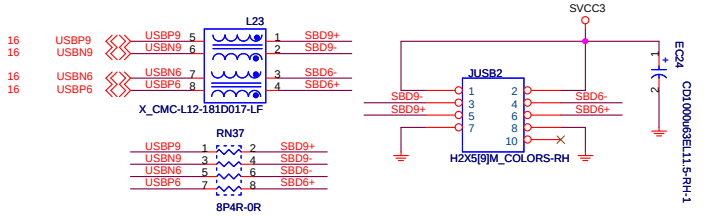
Reversed, can be taken off riser card within bead



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

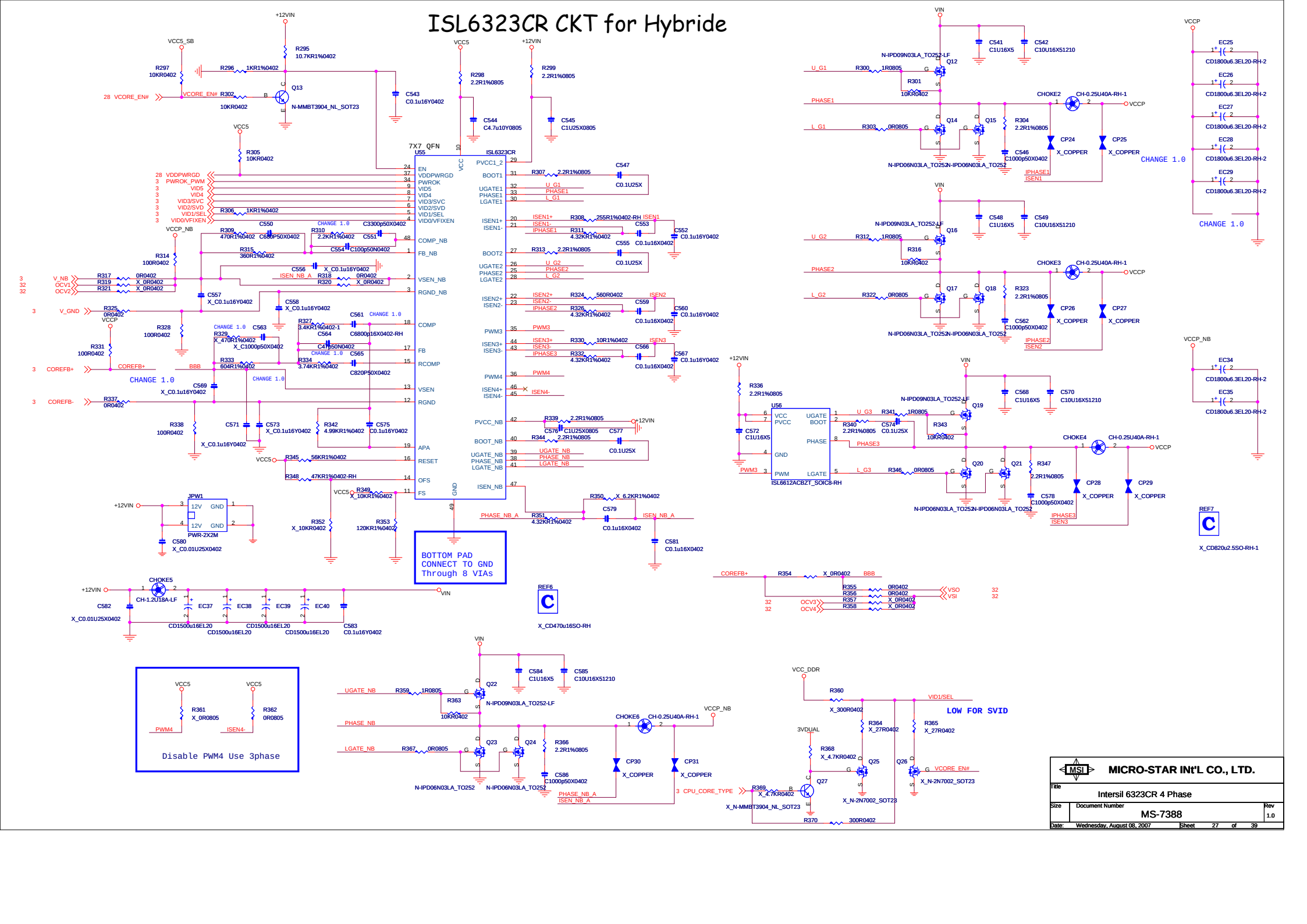


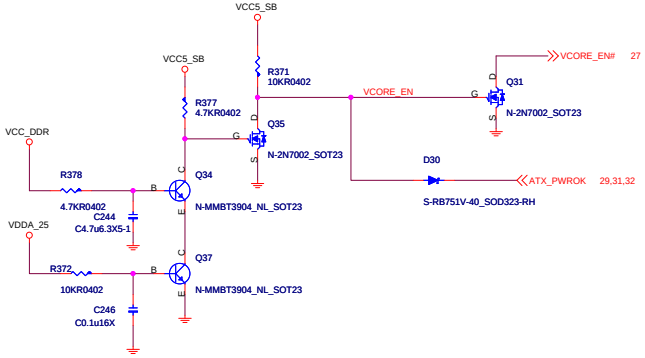
FRONT PANEL USB CONNECTOR FOR USB PORT8,9

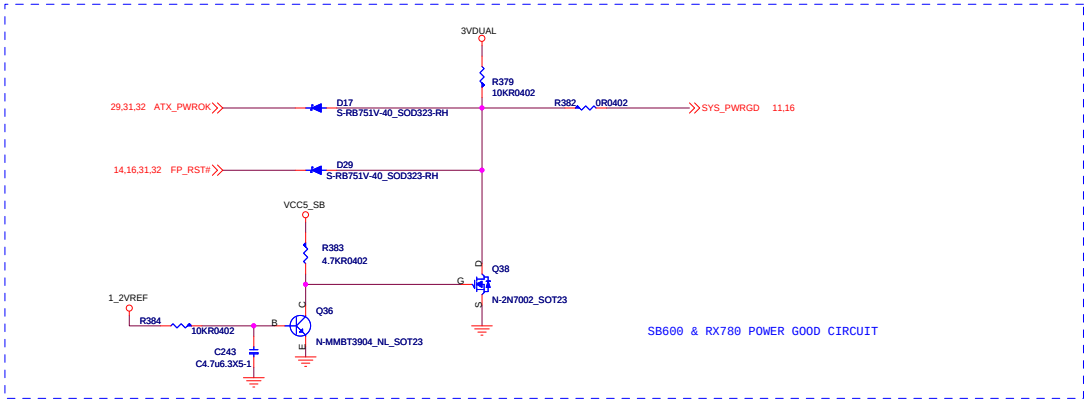


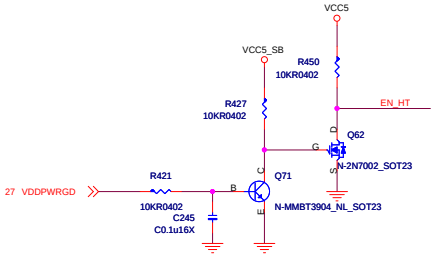
<OrgAddr1> MSI	MICRO-STAR INt'L CO., LTD.	
Title	USB CONNECTORS	
Size	Document Number MS-7388	Rev 1.0
Date: Wednesday, August 01, 2007	Sheet 26 of 39	

ISL6323CR CKT for Hybride

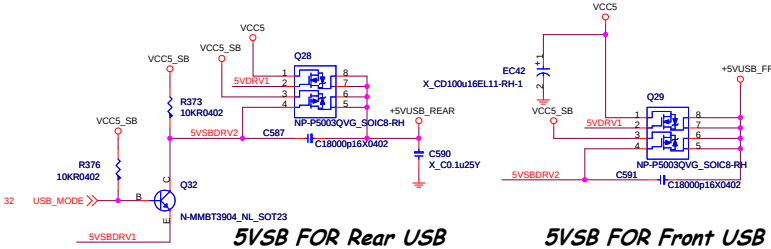






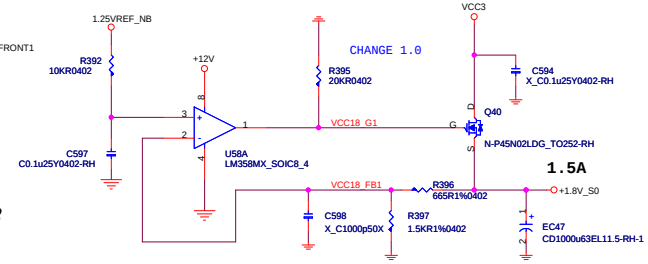


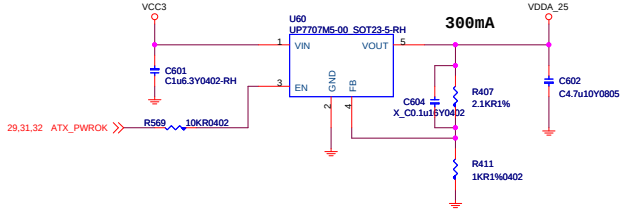
ATHLON64 POWER GOOD & ENABLES CIRCUIT



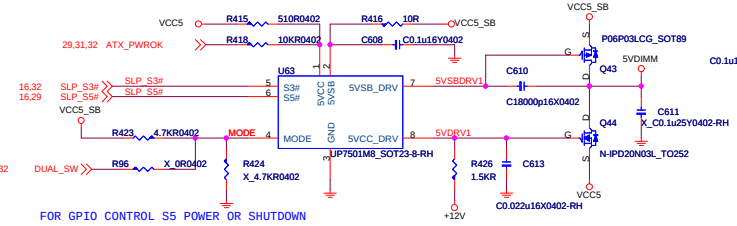
5VSB FOR Rear USB

5VSB FOR Front USB



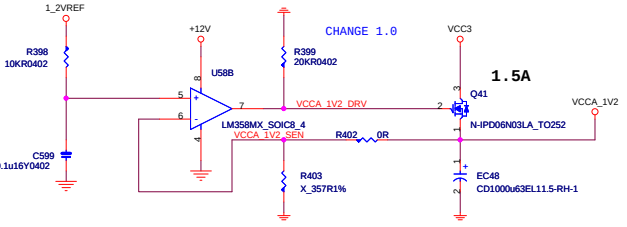


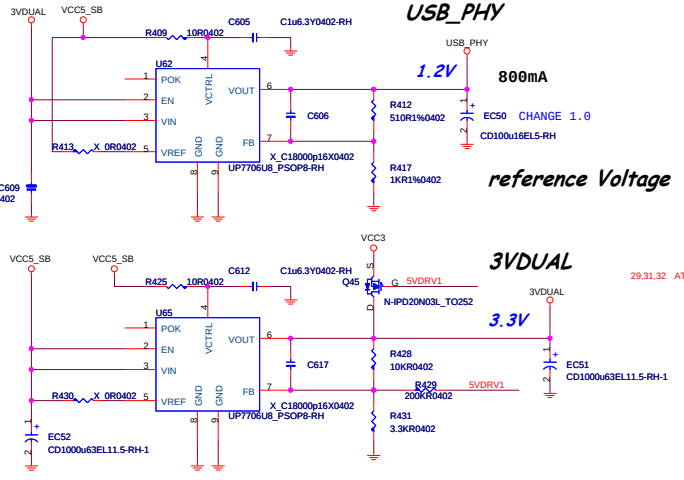
5VDIMM FOR DDR

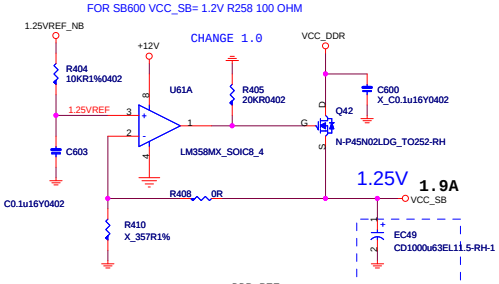


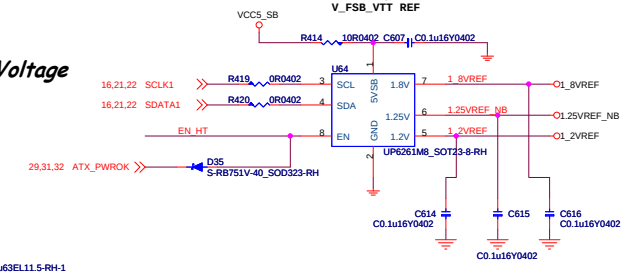
FOR GPIO CONTROL S5 POWER OR SHUTDOWN

S5	S3	MODE	5VDUAL	REMARK
1	1	X	VCC5	S0/S1/S2
1	0	X	VCC5_SB	S3
0	X	1	VCC5_SB	S4/S5
0	X	0	SHUTDOWM	S4/S5





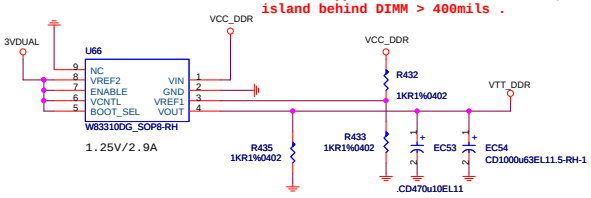




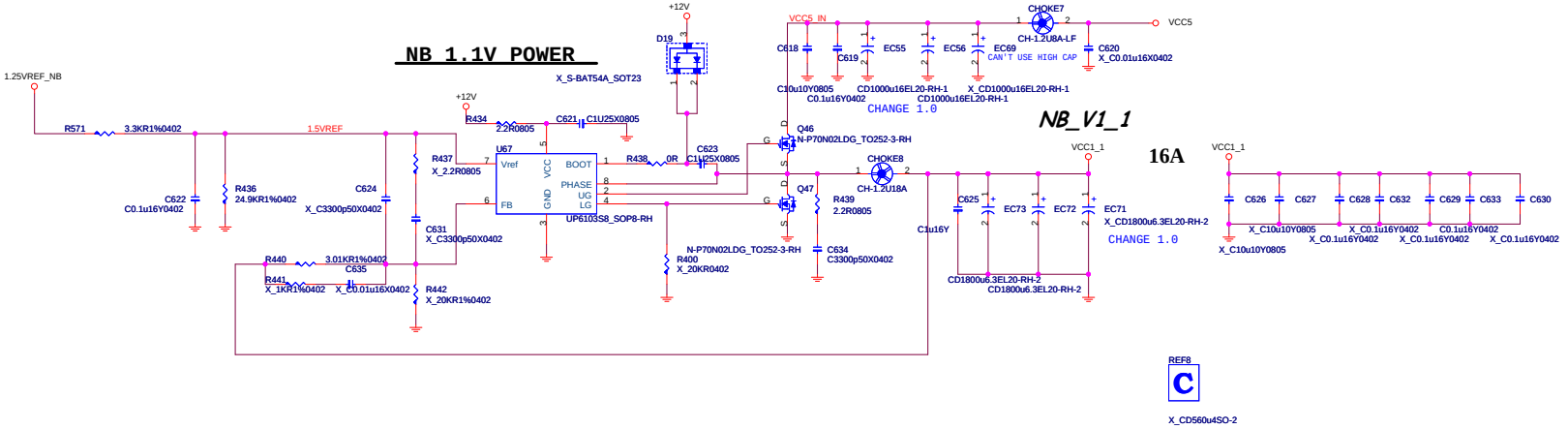
Micro Star Restricted Secret		
Title: ACPI BY UPI		Rev: 1.0
Document Number: MS-7388		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 07, 2007	Sheet 28 of 39

DDR VTT Power

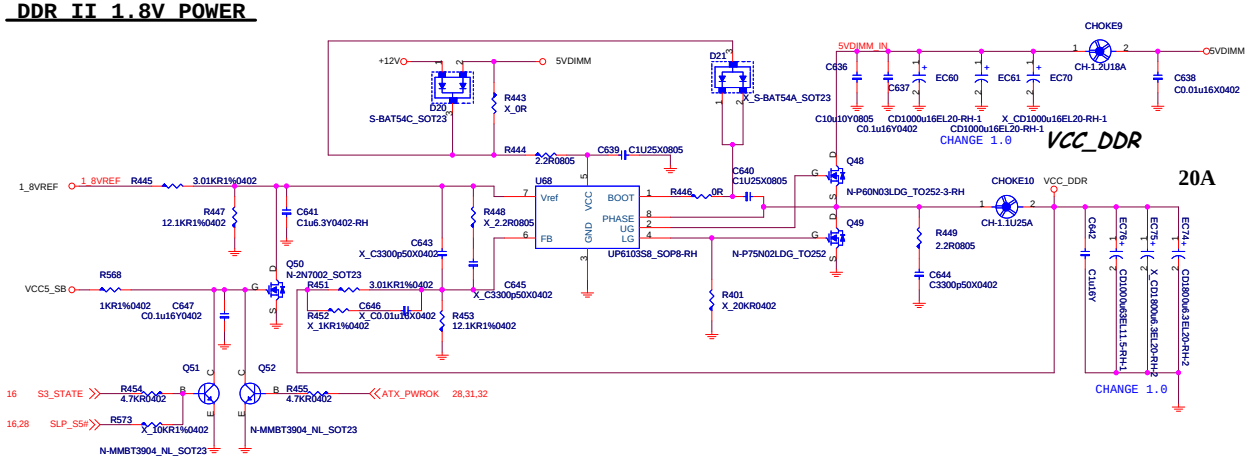
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



NB 1.1V POWER

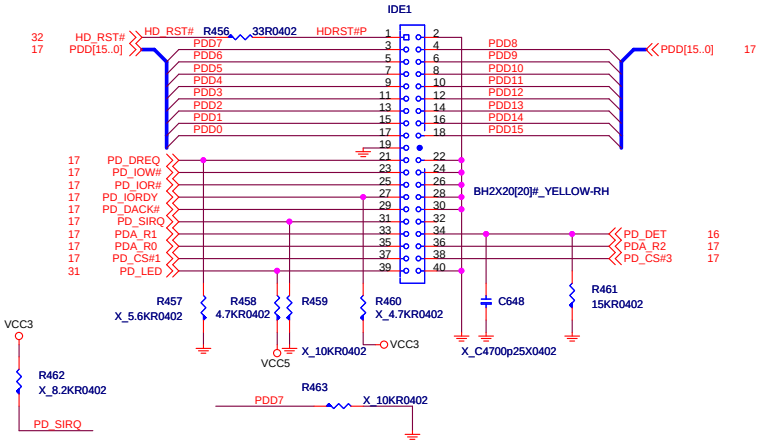


DDR II 1.8V POWER

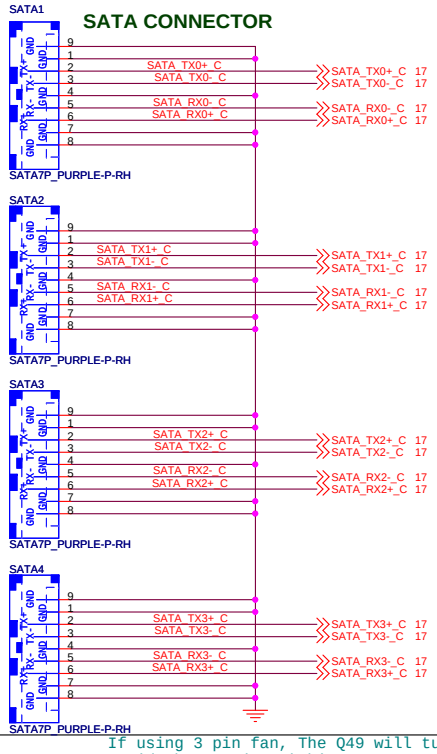


Micro Star Restricted Secret	
Title: VCC_DDR&VCC1_5	Rev: 1.0
Document Number: MS-7388	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 07, 2007
	Sheet 29 of 39

IDE 1



SATA CONNECTOR

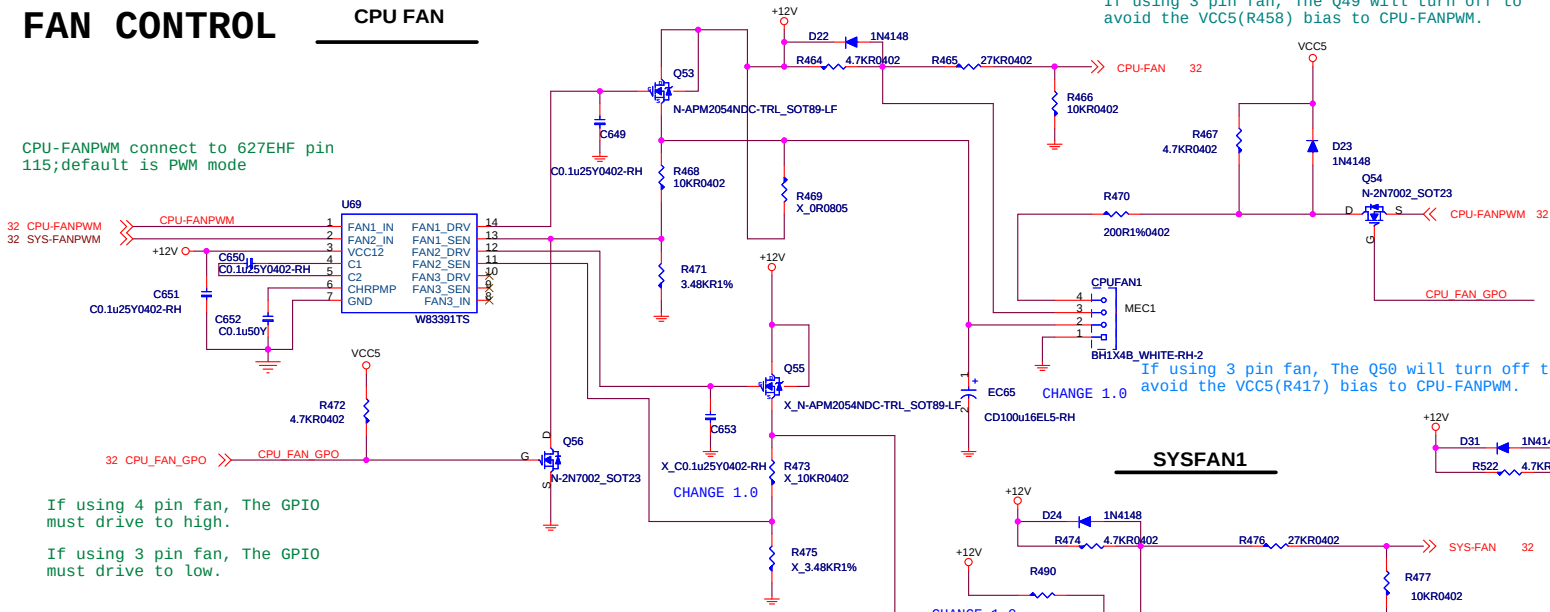


FAN CONTROL

CPU FAN

CPU-FANPWM connect to 627EHF pin 115;default is PWM mode

If using 3 pin fan, The Q49 will turn off to avoid the VCC5(R458) bias to CPU-FANPWM.



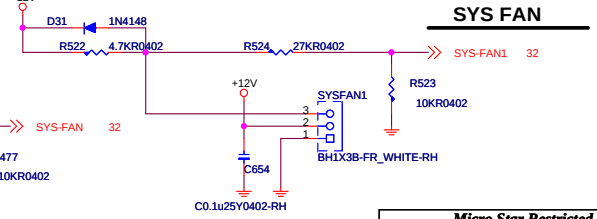
If using 3 pin fan, The Q50 will turn off to avoid the VCC5(R417) bias to CPU-FANPWM.

If using 4 pin fan, The GPIO must drive to high.

If using 3 pin fan, The GPIO must drive to low.

SYSFAN1

SYS FAN



Micro Star Restricted Secret	
Title: IDE Conn/FAN/LPT/SATA	Rev: 1.0
Document Number: MS-7388	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 07, 2007
	Sheet 30 of 39

ATX connector / Front Panel

Intel Front Panel

ESD Protect

C655 X_C180p50N0402

D25 S-BAT54A_SOT23

D28 S-BAT54A_SOT23

SATA_ACT# 17
PD_LED 30
ESATA_LED 33

3VDUAL

PLED1
PLED2

C658 X_C0.1u25Y0402-RH
C659 X_C0.1u25Y0402-RH

EMI

For MSI / Intel Front Panel

VCC5

C657 X_C0.1u25Y0402-RH

R480 33R0402

HDD+
HDD-
RESET-
RESET+
NC
PLED
SLED
PWSW+
PWSW-

JFP1

PLED1
PLED2
PWR_LED
SUS_LED
PWSW+
PWSW-

R479 X_1KR1%0402
R481 0R0402
R482 4.7KR0402
R483 33R0402
R484 100R1%0402
R485 X_10KR0402

14,16,28,32 FP_RST#

C664 C0.1u25Y0402-RH
C665 X_C0.1u25Y0402-RH
C666 X_C0.1u25Y0402-RH

EMI

Near Super I/O

PSIN

EMI solution

VCC3
C669 X_C0.1u16Y0402

VCC5
C670 X_C0.1u25Y0402-RH

VCC5
C671 C0.1u25Y0402-RH

JFP2

GND
SLED
PLED
SPEAKER
BUZ+
BUZ-
VCCSPK

H2X4[7]M_COLOR-RH

CHANGE 1.0

32 ALARM
16 SPKR

R486 100R0805
R487 2.2KR0402

Q57 N-MMBT3904_NL_SOT23

C674 C0.1u25Y0402-RH

PS2 KEYBOARD & MOUSE CONNECTOR

SVCC1

RN41 8P4R-4.7KR0402

EC67 X_CD100u16EL5-RH
C656 X_C0.1u25Y0402-RH

R478 X_1KR1%0402

JKBMS1

MSDATA MSDAT#
MSCLK MSCLK#
KBDATA KBDAT#
KBCLK KBCLK#

FB8 300-600mA
FB9 300-600mA
FB10 300-600mA
FB11 300-600mA

MS
KB

C660 C180p50N0402
C663 C180p50N0402
C661 C180p50N0402
C662 C180p50N0402

CONN-KB_MS-RH

SERIAL PORT 1

U70

VCC
RIN1
RIN2
RIN3
RIN4
RIN5
ROUT1
ROUT2
ROUT3
ROUT4
ROUT5
V+
V-
DIN1
DIN2
DIN3
GND
DOUT1
DOUT2
DOUT3

NRIA#
NCTSA#
NDSRA#
NSINA
NDCDA#
RIA#
CTSA#
DSRA#
SINA
DCDA#
RTSA#
DTRA#
SOUTA
NRTSA
NDTRA
NSOUTA

75232S-SSOP20

+12VCOM
-12VCOM
D26 1N4148
D27 1N4148
C667 X_C0.1u25Y0402-RH
C673 X_C0.1u25Y0402-RH

COM1 CONN-COM

CN1 8p4C-330p50N
CN2 8p4C-330p50N

ATX Connector

ATXPWR1

3.3V
-12V
GND
P_ON
5V
POK
5VSB
+12V

ATX_PSON#
ATX_PWROK 28,29,32

C686 X_C0.1u25Y0402-RH
C687 C1000p50X0402
C691 C1000p50X0402
C688 C0.1u25Y0402-RH
C689 C0.1u25Y0402-RH
EC68 CD1000u63EL11.5-RH-1
R488 10KR0402
C700 C0.1u25Y0402-RH
C707 X_C0.1u25Y0402-RH
C701 C0.1u25Y0402-RH
C702 C0.1u25Y0402-RH

VCC3
VCC5
VCC5_SB
+12V

PWRCONN24P_CREAM-RH-1

+1.8V_S0
3VDUAL

C675 X_C0.1u16Y0402
C676 X_C0.1u16Y0402
C690 C0.1u16Y0402
C692 X_C0.1u16Y0402

CP32
CP33
CP34
CP35
CP36

EMI solution

VCCP
C677 X_C0.1u16Y0402

VCC5
C679 X_C0.1u16Y0402
C680 X_C0.1u16Y0402
C681 X_C0.1u16Y0402
C682 X_C0.1u16Y0402
C683 X_C0.1u16Y0402
C684 X_C0.1u16Y0402
C685 X_C0.1u16Y0402

VCC3
C695 X_C0.1u16Y0402
C696 X_C0.1u16Y0402
C697 X_C0.1u16Y0402
C698 X_C0.1u16Y0402
C699 X_C0.1u16Y0402

C693 X_C0.1u25Y0402-RH
C694 X_C0.1u25Y0402-RH

Micro Star Restricted Secret

Title	ATX connector / Front Panel/KB
Rev	1.0
Document Number	MS-7388

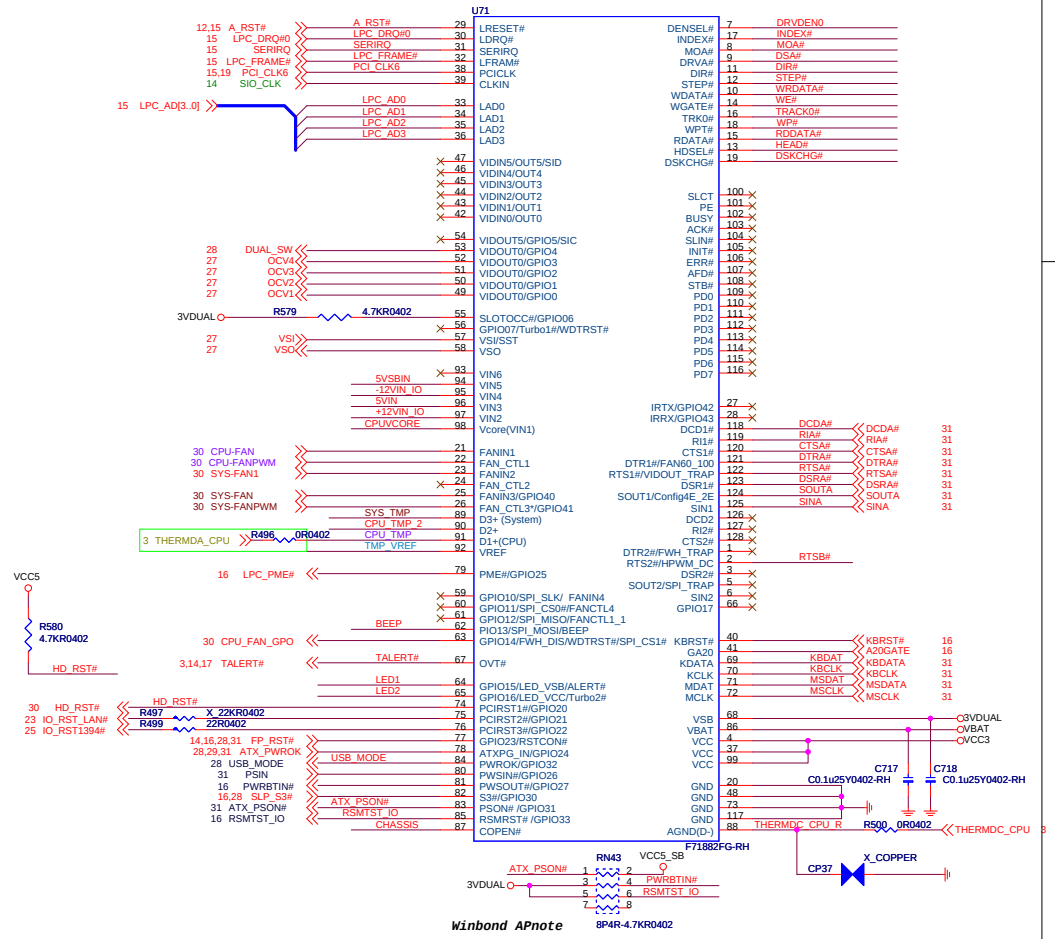
MICRO-STAR INT'L CO.,LTD.
No. 69, Li-De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw

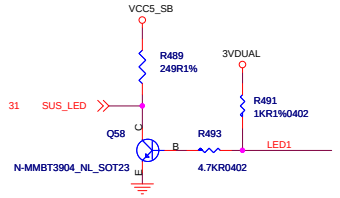
Last Revision Date: Tuesday, August 07, 2007

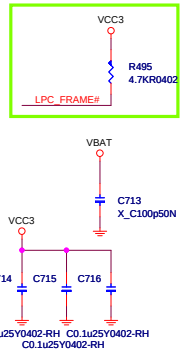
Sheet 31 of 39

Super I/O

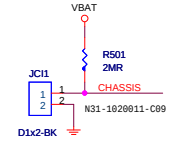
LPC SUPER I/O F71882



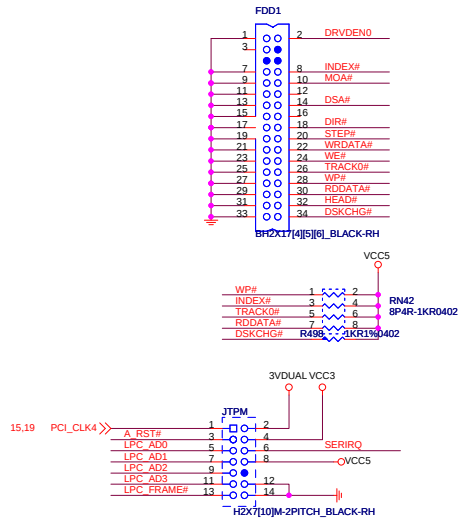




Chasiss Intrusion



FLOPPY CONNECTOR



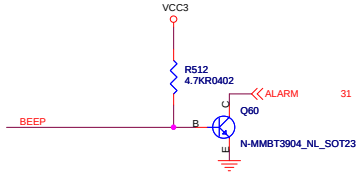
LPC I/O STRAPPING RESISTOR

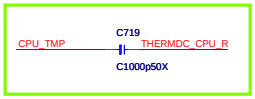
	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT PIN42-47=VIDIN	PIN49-54=GPIO PIN42-47=VIDIN/OUT
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%

BEEP

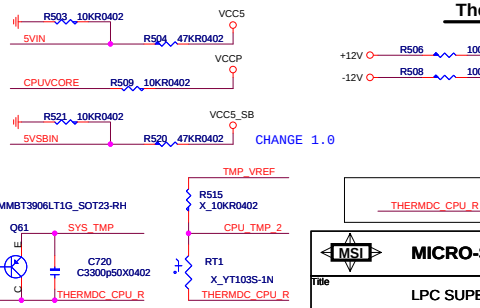
Ver C:Pop R32 and R27 and Q2. non-pop R31

Ver G,H:Pop R27 and R31. non-pop R32 and Q2





Thermal Resistor



NOTE: LOCATE CLOSE STATUS PANEL

Winbond APnote

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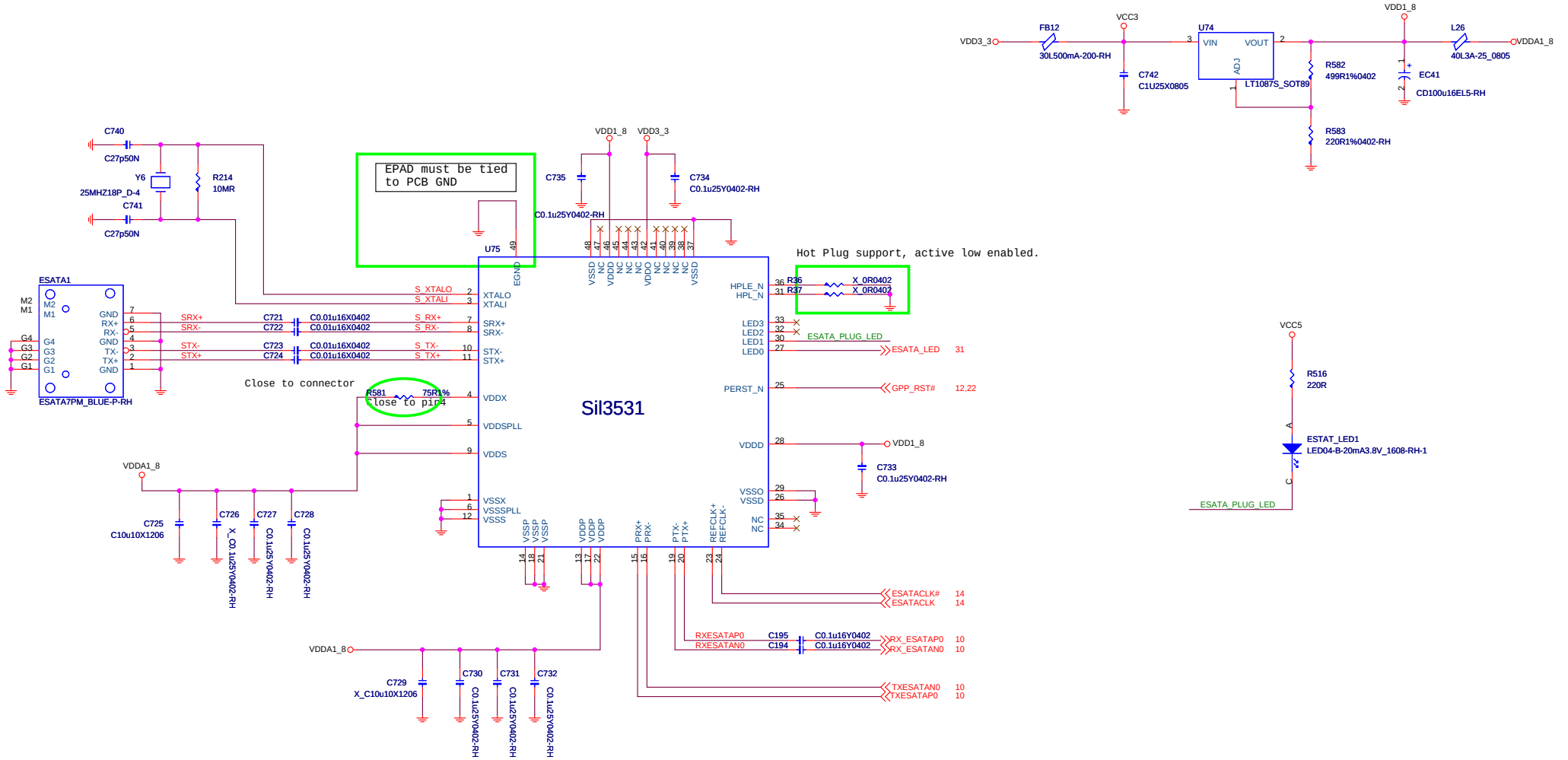
Size: | Document Number: MS-7388 | Rev: 1.0

Date: Tuesday, August 07, 2007 | Sheet 32 of 39

PCIE to SATA Bridge --Silicon Image SiI3531



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Title: Sil3531 PCIE to ESATA	Rev: 1.0
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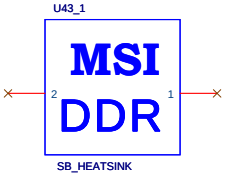
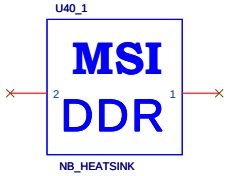
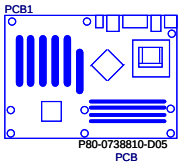
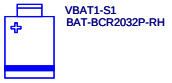
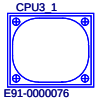
	Sheet 33 of 39



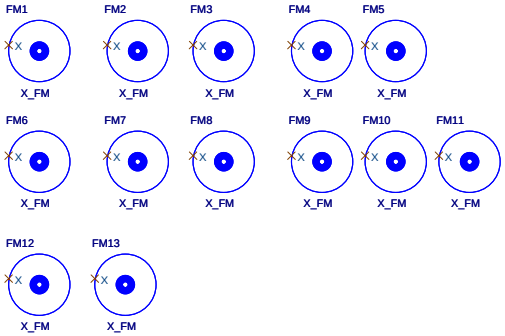




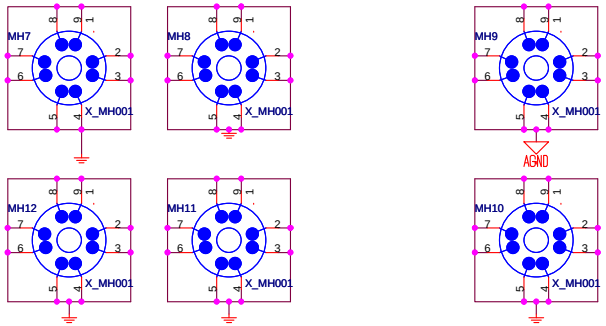




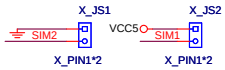
Optics Orientation Holes



Mounting Holes



Simulation



Model option table

Model type	Function	BOM Config	ERP BOM No.
MS-7388	RX780+SB600+1_PCI-EX16+2_PCI-EX1 RD780+SB600+2_PCI-EX16+1_PCI-EX1+1394	Cfg-7388-RX780 Cfg-7388-RD780	

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	Sheet 34 of 39	

Micro Star Restricted Secret	
Title *GPIO SPEC*	Rev 1.0
Document Number *MS-7388*	
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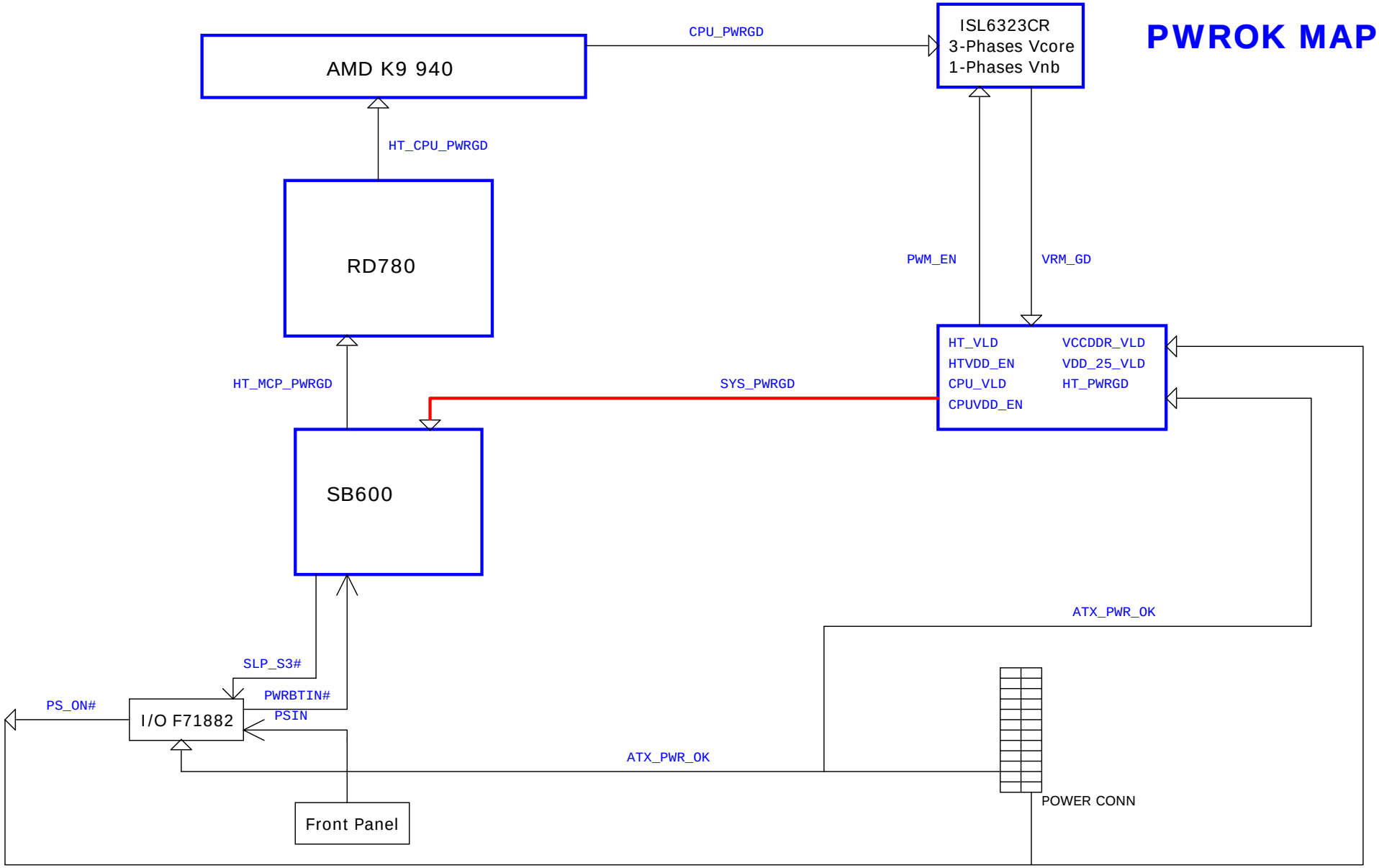
PWROK MAP



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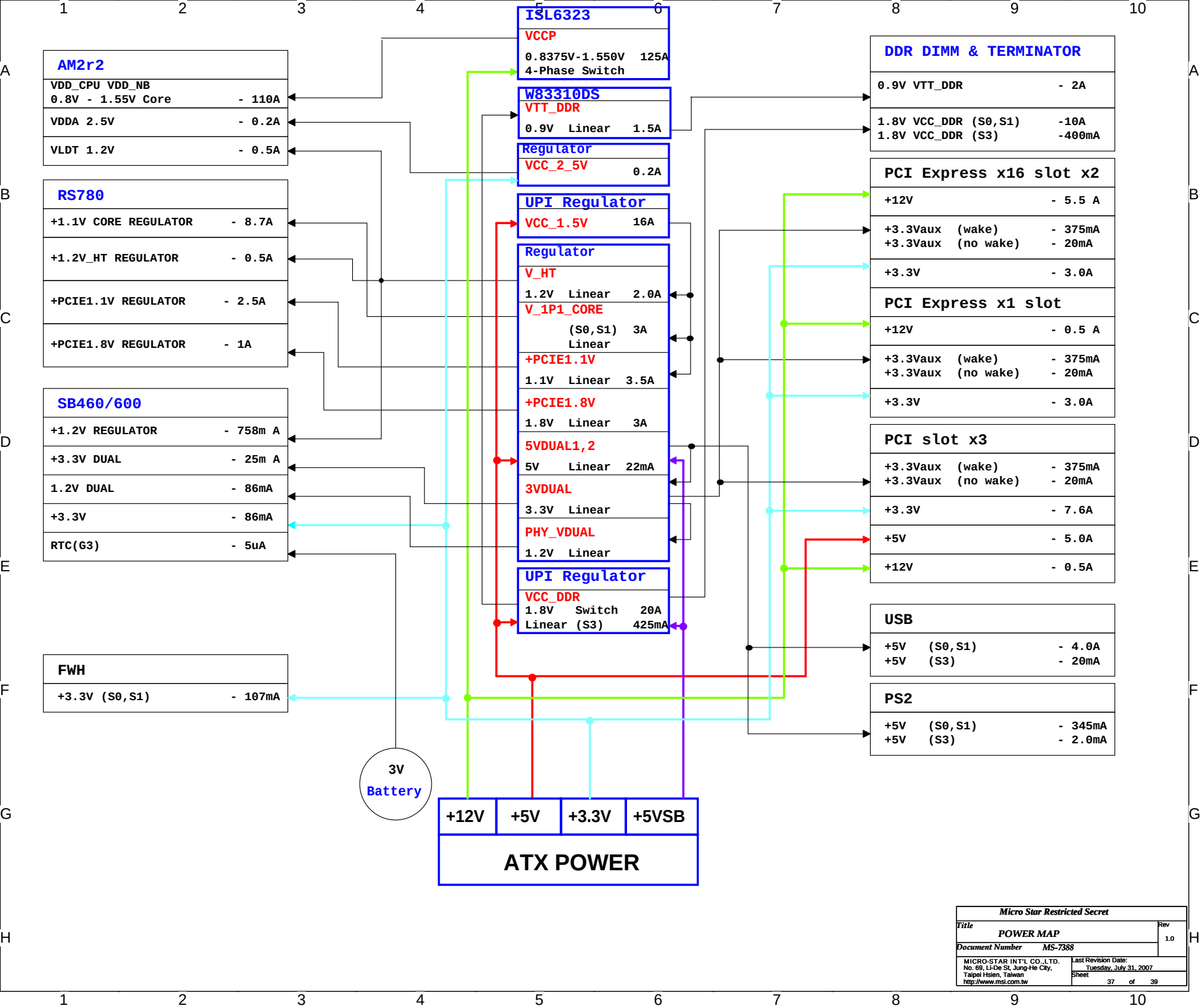
Title	PWROK MAP	
Size	Document Number: MS-7388	Rev: 1.0
Date: Tuesday, July 31, 2007	Sheet 36 of 39	



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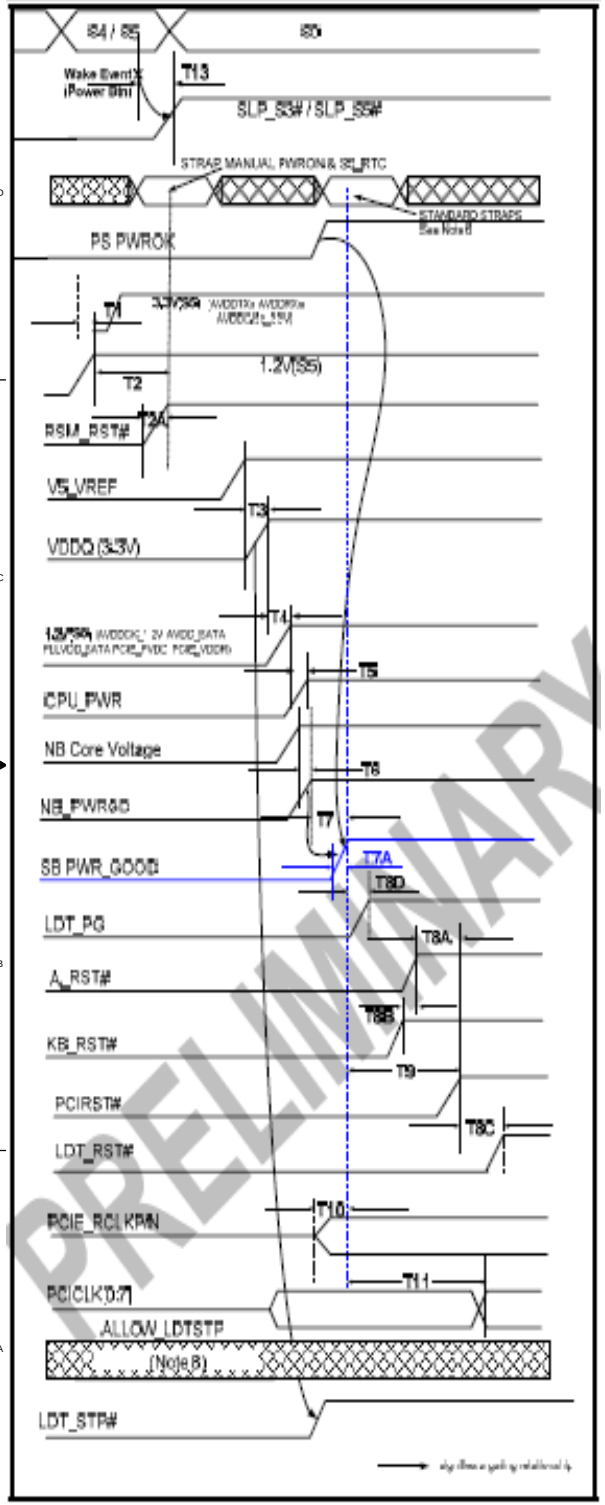
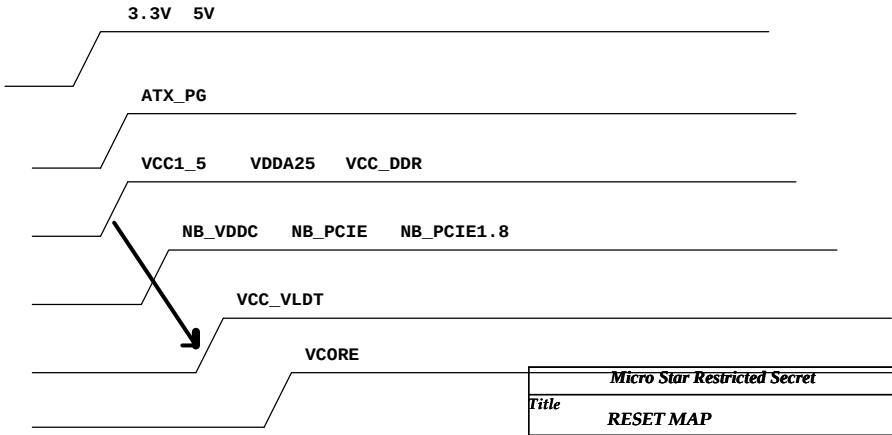
Last Revision Date: Tuesday, July 31, 2007

Sheet 37 of 39





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Title *RESET MAP*	Rev 1.0
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Last Revision Date: Tuesday, July 31, 2007

Sheet 38 of 39

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VER : 1.0 MODIFY

1.C46,48,50,52,55,71,70 -->10uF/ X5R/1206....page 5

2.Add reset R45~R47..Q72~Q74..U76~U78..R387~R389 RX780 A_RST#....RD780 NB_RST#.....page 12

3.Change GFX_CLK to ATIG_CLK and add R204~R207 to GFX1_CLK GPP_CLK colay...and add R335.R394 to LAN damping resister for emi and chage CLK gen.477.....page 14

4.Add Q39.Q63.Q64.R386.R40.R44.C492..PCIE_PVDD delay VCC_SB 3us~5ms ..ATI.AP.NOTE....page15

5.Add R390.R391.R393 and change PCIE X 16 or 8 control single to PFGX2_PRSNT#....page21

6.Change EC10~EC17.EC20~21 footprint OS-CON and JSPD1 change to 2pin....page24

7.Del CP23 and add C703 for EMI audio precision....page 26

8.Change the over voltage cpu R354.and del EC30....page27

9.Change R310 3.4K-->2.2K C564 33pF-->47pF C561 1000pF-->6800pF R333 698-->604 R348 56K-->47K R353 100K-->120K R311,326,332,351 3.9K-->4.32K R308 100-->255 R324 100-->560 R330 100-->10
Q14,15,17,18,20,21-->D03-06N030B-I14 R329 470-->NC C563 1000pF-->NC....page27

10. Change EC50 footprint for os-con cap and C244.C243 change 4.7u....page28

11.Change EC65.EC66 footprint for os-con and add D31.R522~R524 that SYS_FAN speed monitor....page 30

12.Change R486 220-->100 speaker speak too small....page 31

13. Add R520.R521 +5VSB monitor....page 32

14.R36.R37 empty no support esata chip hot plut.becuae it's on board not card....page33

15.Add CP23 VDD_PCIE power.... page13

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Document Number	*MS-7388*	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, August 01, 2007	
	Sheet 39 of 39	