MODEL NAME : *FDQ50 / FDC55*

PCB NO : *LA-J191P DAC0000X000*

MB *LA-J191P DAC0000X000*
FB *LS-H821P DA60027F00S*
KB *LS-H822P DA4002TR00S*

EDP w/TS *LF-H821P DA30001AF00*
EDP w/o TS *LF-H824P DA30001AD00*
CCD *LF-H822P DA30001AC00*
LED *LF-F825P DA30001AE00*
KBC *LF-H82AP DA30001BD00*
IO *LF-H823P DA30001AB00*

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Schematic Document

Fiorana CML CometLake H

2019-11-22
Rev: DVT2.1 0.4(X03)

@
@EMC@
CONN@
TP@
3PHASEI5@
4PHASE62@
4PHASE82@
BreakDown@
EMC@
RF@
UMA@
DIS@
EMI@
DAR@
CNV@
N18PG62@
N19PQ1@
N19PQ3Q@
N19PQVRAMS@
N19PQVRAMH@
N19PQVRAMM@
NVPRO@
VPRO@
UMAP@
UMAX@
XDP@
QTJ0@
QTJ1@
QTJ2@

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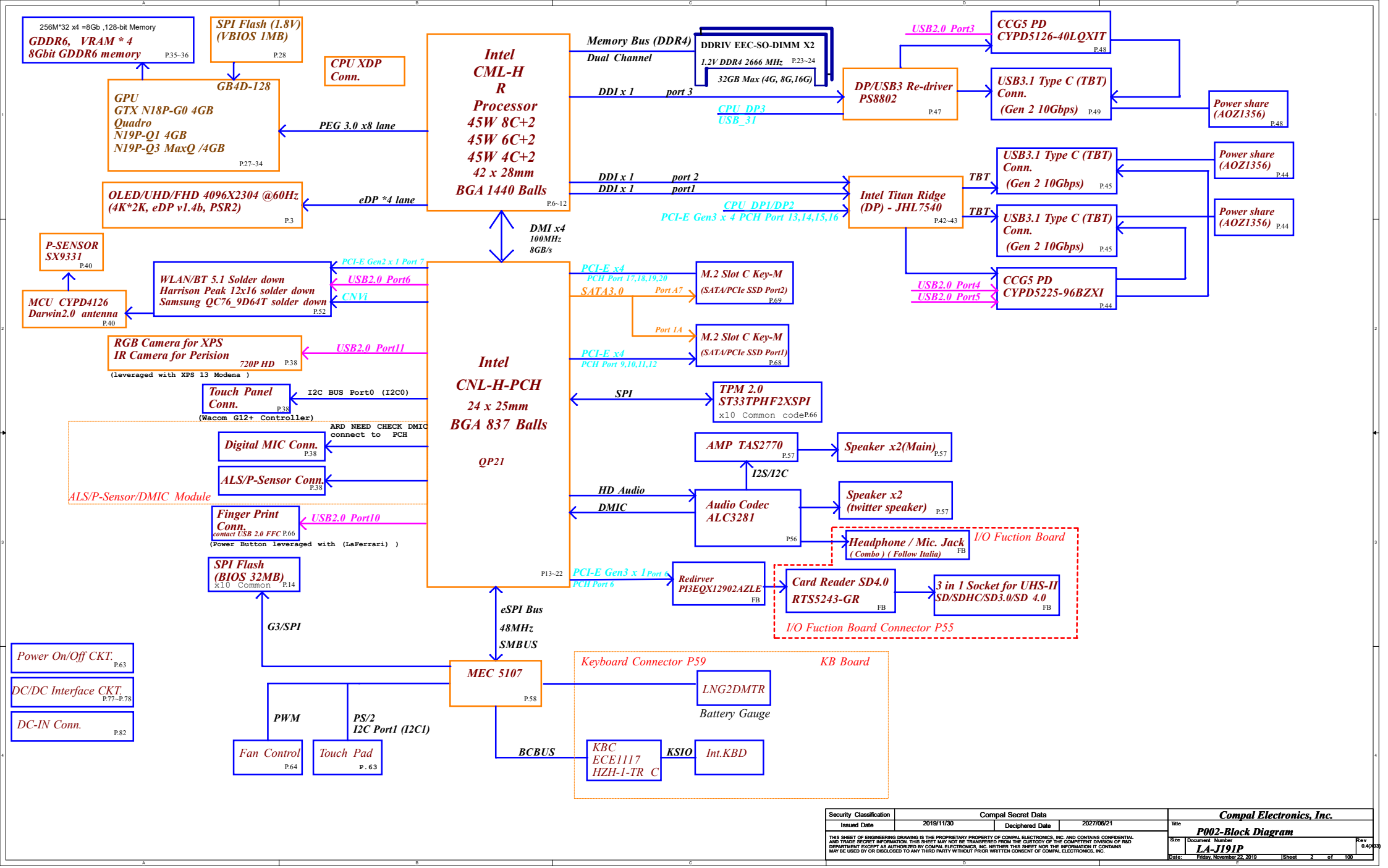
Title: *P001-Cover Page*

Size: | Document Number: *LA-J191P* | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 1 of 100



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Compal Electronics, Inc.

Title: **P002-Block Diagram**

Size	Document Number	Rev
	LA-J191P	0.4(003)

Date: Friday, November 22, 2019 | Sheet 2 of 100

RE67	CE51	REV	PHASE
240K	4700p		PRE EVT
130K	4700p	X00	EVT
62K	4700p	X00	DVT1
33K	4700p	X01	DVT1.1
8.2K	4700p	X02	DVT2
4.3K	4700p	X03	DVT2.1
2K	4700p		
1K	4700p	A00	PVT

USB3.1	DESTINATION
1	USB3.0 PS8802
2	None
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	None
2	None
3	Type-C Conn 1 (Left Side)
4	Type-C Conn 1 (Right Side)
5	Type-C Conn 2 (Right Side)
6	None
7	None
8	None
9	None
10	Finger Print
11	RGB CAMERA
14	NGFF-1 WLAN + BT

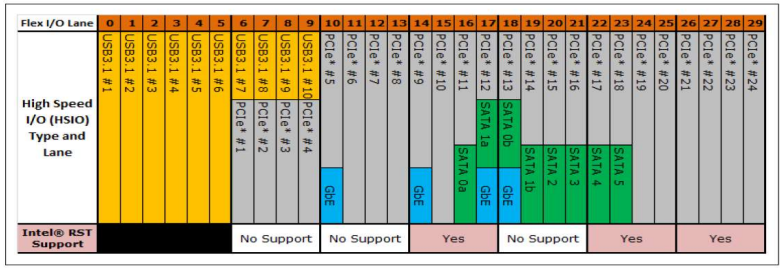
USB OC#	DESTINATION
0	
1	
2	
3	Type-C Conn 1 (Left Side)
4	Type-C Conn 1 (Right Side)
5	Type-C Conn 2 (Right Side)
6	
7	

PCI EXPRESS	DESTINATION	USB3.0	DESTINATION
Lane 1	Titan Ridge	7	None
Lane 2		8	None
Lane 3		9	None
Lane 4		10	None
Lane 5	None		
Lane 6	CNVi WLAN + BT		
Lane 7	CARD READER		
Lane 8	None		
Lane 9	SSD		
Lane 10	SSD	SATA	DESTINATION
Lane 11	SSD	0A	N/A
Lane 12	SSD	1A	SSD
Lane 13	None	0B	N/A
Lane 14	None	1B	N/A
Lane 15	None	A2	N/A
Lane 16	None	A3	N/A
Lane 17	SSD_2	A4	SSD
Lane 18	SSD_2	A5	N/A
Lane 19	SSD_2		
Lane 20	SSD_2		

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	NGFF-2 SSD2	11	None
2	None	12	None
3	NGFF-2 SSD1	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-1 WLAN		
7	GPU		
8	None		
9	None		

DDI	DESTINATION
1	Titan Ridge
2	Titan Ridge
3	DP/USB3 PS8802

LPC	DESTINATION
ESPI/LPC0	MEC5107
LPC1	DEBUG PORT



The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
– A maximum of 16 PCIe* Ports (or devices) can be enabled
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 - GbE (0 or 1)
– PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
– A maximum of 6 SATA Ports (or devices) can be enabled
– SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
– SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
– A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
– A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (Intel® Rapid Storage Technology) PCIe* storage devices
– x2 and x4 PCIe* NVMe SSD
– x2 Intel® Optane™ Memory Device
– See the " PCI Express* (PCIe*) " chapter for the PCH PCIe* Controllers,configuration, and lanes that can be used for Intel® Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool.

Symbol Note :
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: means Digital Ground
: means Analog Ground

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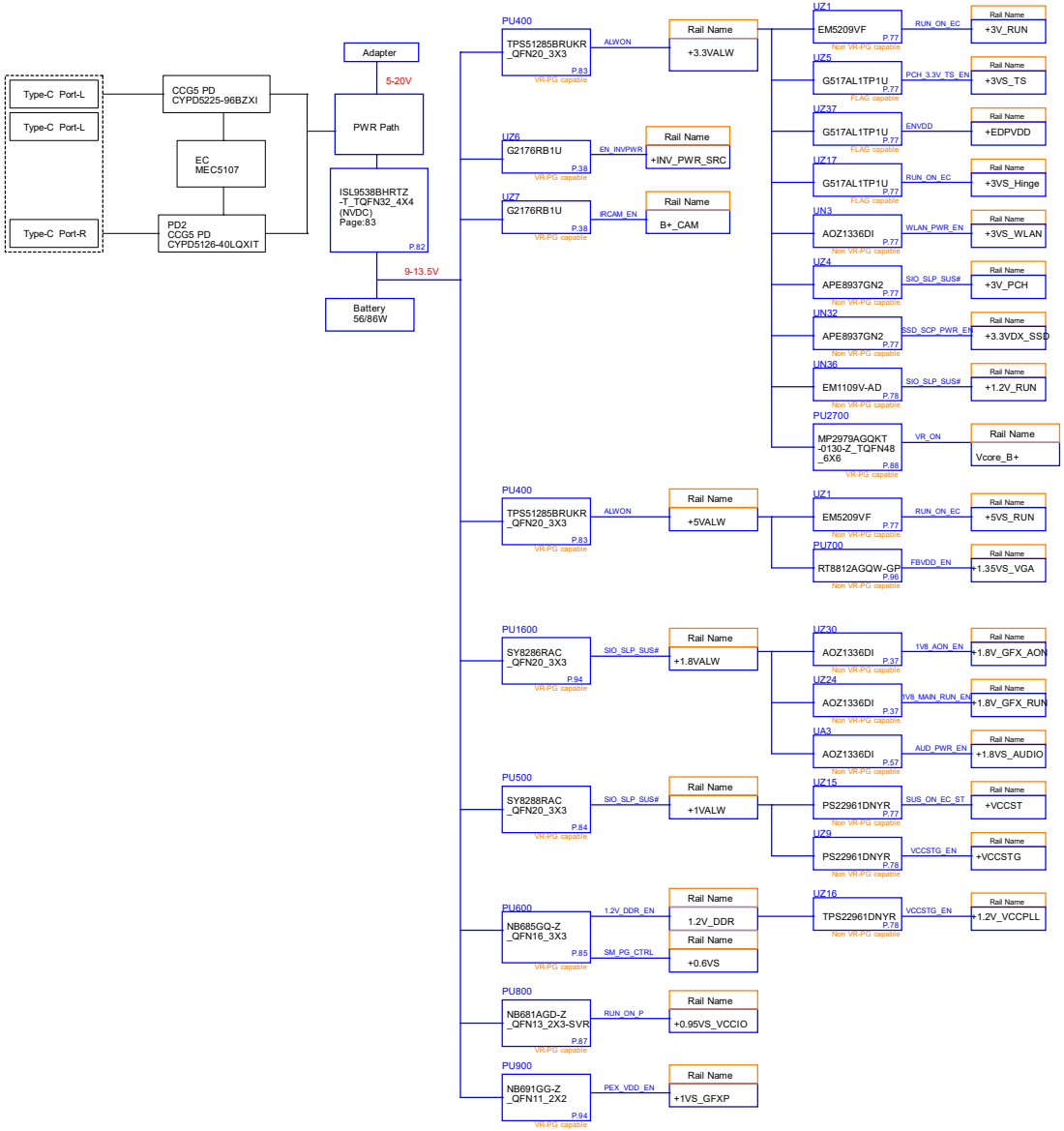
Title: P003-Notes List

Size	Document Number	Rev
	LA-J191P	0.4(X03)

Date: Friday, November 22, 2019 Sheet 3 of 100



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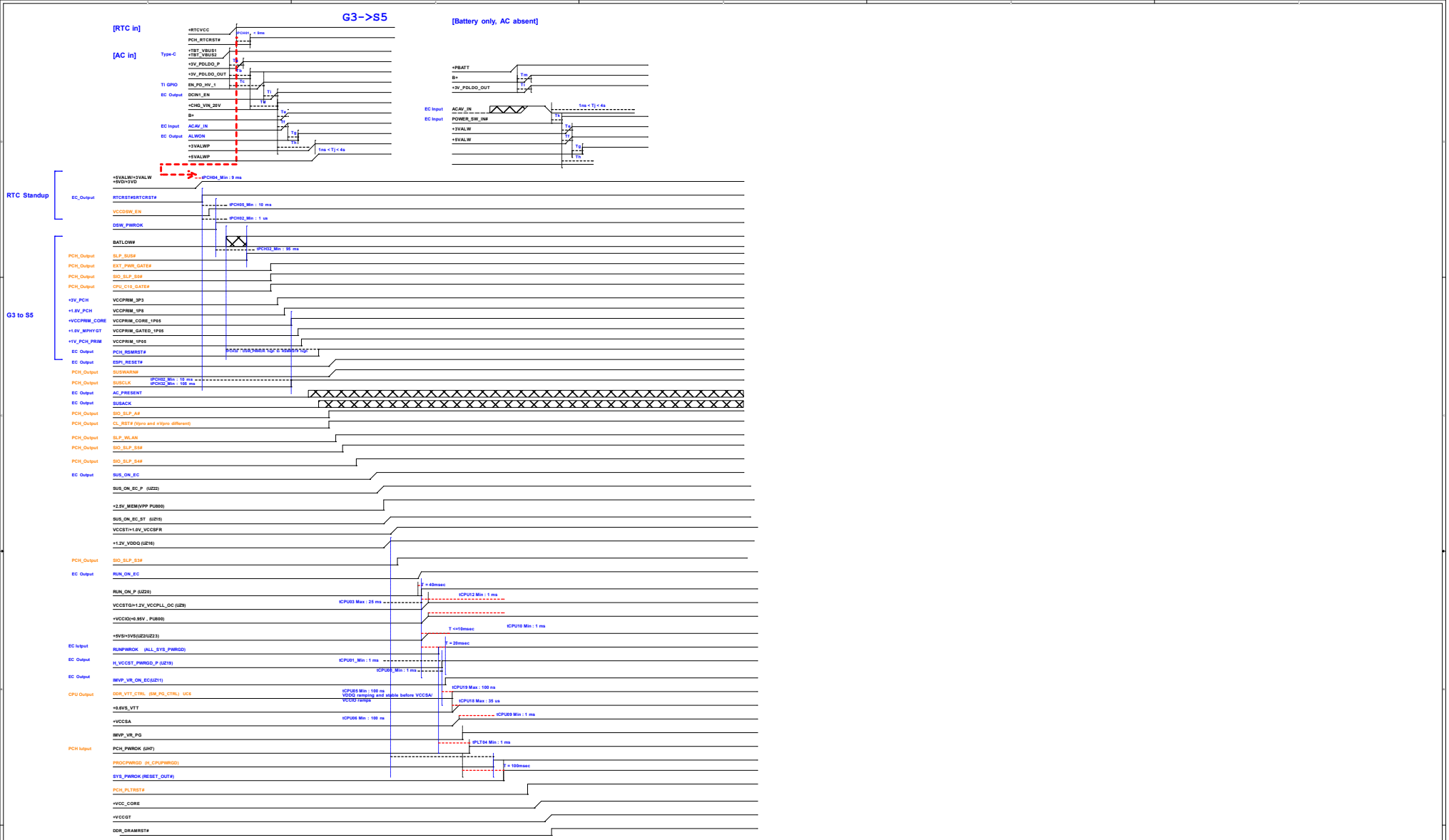
Title: PDM - Power MAP

Size: Document Number: LA-J191P Rev: 0.4

Date: Sunday, December 24, 2017 Sheet: 4 of 51



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Issued Date	2018/11/30	Deciphered Date 2019/12/31	Title P865-Power Sequence

To Titan Ridge Port1

DP/USB3 Re-driver PS8802

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Issued Date	2019/11/30	Deciphered Date	2027/06/21

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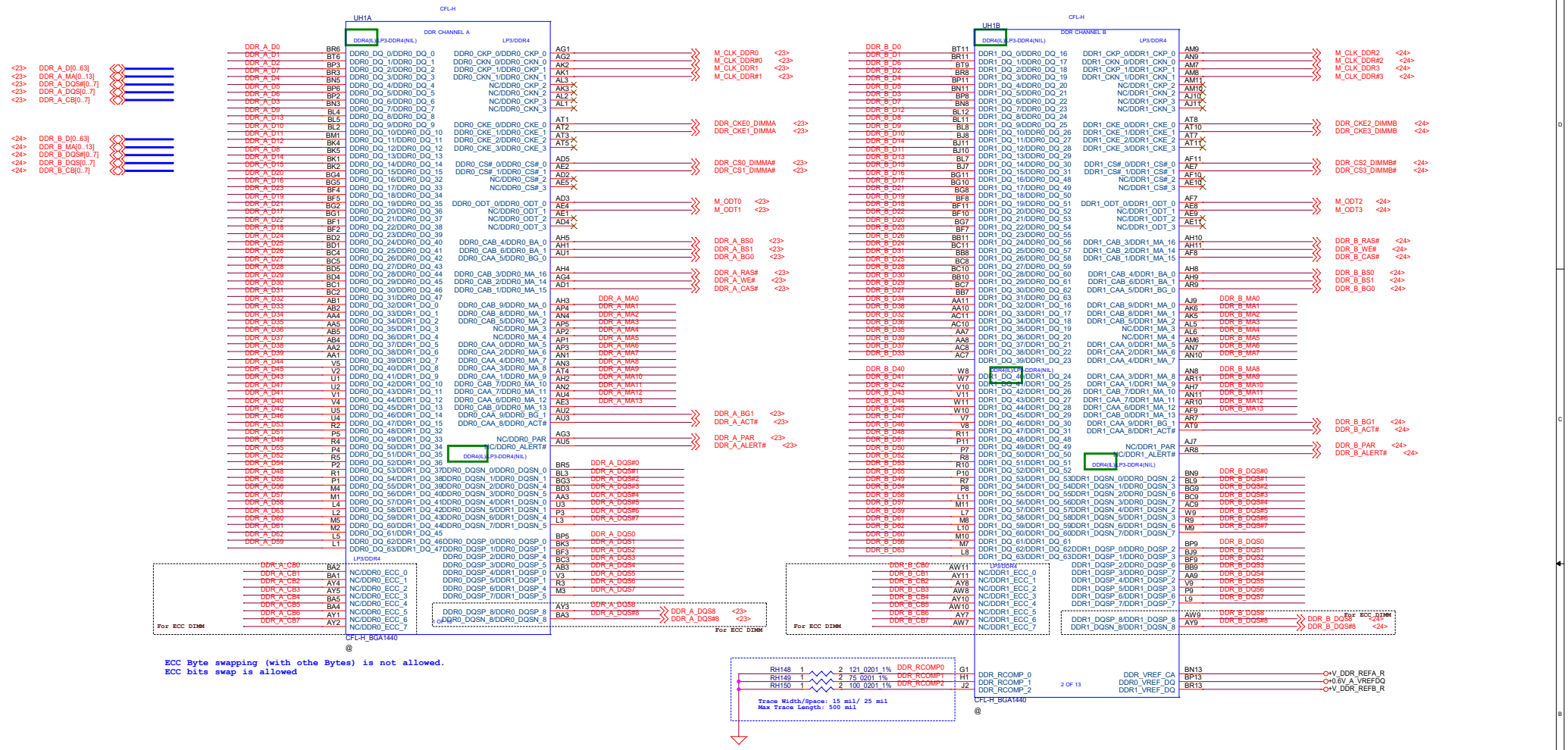
Compal Electronics, Inc.

Title: P006-CPU(1/7) DMI,PEG,DDI,EDP

Size	Document Number	Rev
C		0.4(003)

Date: Friday, November 22, 2019 | Sheet 6 of 100

Interleave



ECC Byte swapping (with othe Bytes) is not allowed.
ECC bits swap is allowed

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Issued Date	2019/11/30	Deciphered Date	2027/06/21

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Title: *P007-CPU(2/7) DDR4*

Size	Document Number	Rev
C		0.4(X03)

Date: Friday, November 22, 2019 | Sheet 7 of 100

CFG Straps for Processor

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG2 PEG LANE REVERSAL
NORMAL:1
LANE REVERSER :0

- 00 = 1 x8, 2 x4 PCI Express*
- 01 = reserved
- 10 = 2 x8 PCI Express*
- 11 = 1 x16 PCI Express*

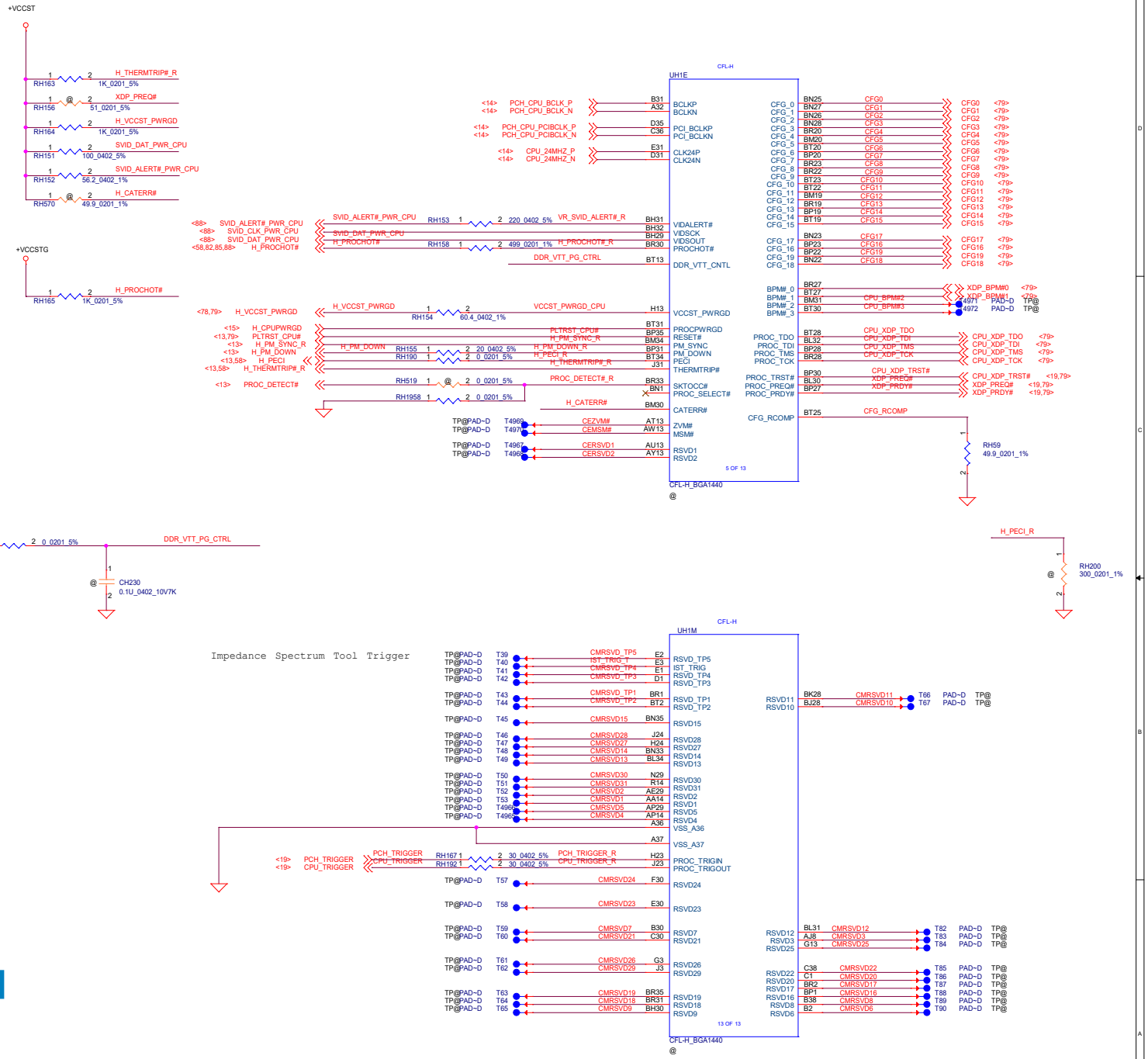
PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

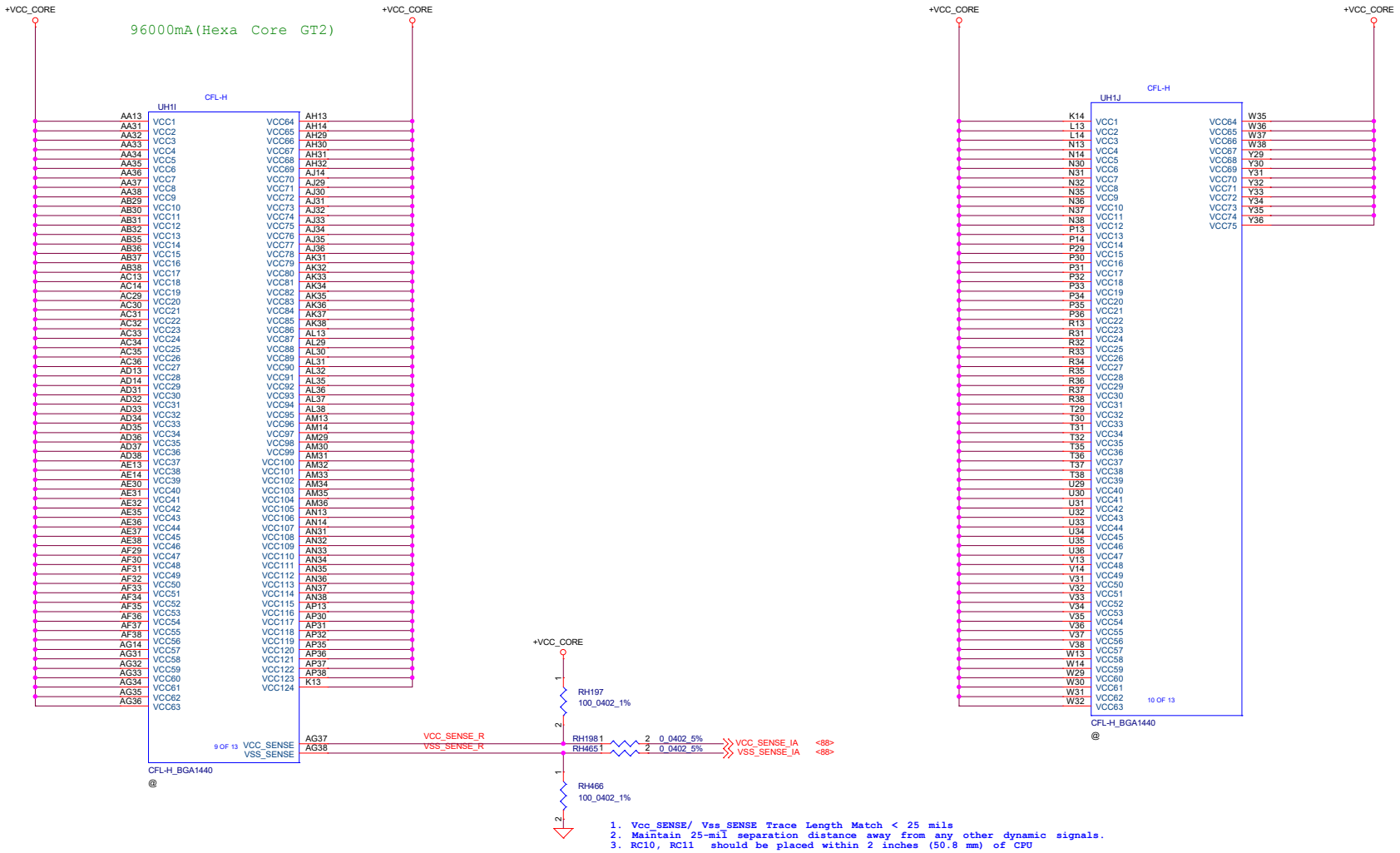
Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals			Lanes													
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 **Reversed**	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 **Reversed**	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:
1. For CFG bus details, refer to Section 6.4.
2. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
3. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   - Connect lane 0 of 1st device to lane 0.
   - Connect lane 0 of 2nd device to lane 8.
   - Connect lane 0 of 3rd device to lane 12.

   For example:
   a. When using 1x8 + 2x4, the 8 lane device should use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device should use lanes 0:3, and other 2 lanes device should use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device should use lanes 0:3, two lane device should use lanes 8:9, one lane device should use lane 12.
4. for reversal lanes, for example:
   When using 1x8, the 8 lane device should use lanes 8:15, so lane 15 will be connected to lane 0 of the Device.
5. For Basin Falls platform use 1x8+2x4 Bifurcation





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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Title: ***P009-CPU(4/7) PWR,VCore,RSVD***

Size	Document Number	Rev
Custom		0.4(003)

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570805_CFL_EDS_Vol1_Rev0.7
+VCC_SA
Max: 11100mA

+VCC_SA

570805_CFL_EDS_Vol1_Rev0.7
+1.2V_VDDQ_CPU
Max: 3300mA

+VDDQ_DDR

+1.2V_DDR

P_JP1604
PAD-OPEN 3x3m
JUMP@

571483_CFL_H_RVP_CRB_TDK_Rev0p5
+1.05VS_VCCSTG: 1uF * 1

CFL-H
UH1L

J30	VCCSA1	VDDQ1	AA6
K29	VCCSA2	VDDQ2	AE12
K30	VCCSA3	VDDQ3	AF5
K31	VCCSA4	VDDQ4	AF6
K32	VCCSA5	VDDQ5	AG5
K33	VCCSA6	VDDQ6	AG9
K34	VCCSA7	VDDQ7	AJ12
K35	VCCSA8	VDDQ8	AL11
L31	VCCSA9	VDDQ9	AP6
L32	VCCSA10	VDDQ10	AP7
L35	VCCSA11	VDDQ11	AR12
L36	VCCSA12	VDDQ12	AR6
L37	VCCSA13	VDDQ13	AT12
L38	VCCSA14	VDDQ14	AW6
M29	VCCSA15	VDDQ15	AY6
M30	VCCSA16	VDDQ16	J5
M31	VCCSA17	VDDQ17	J6
M32	VCCSA18	VDDQ18	K12
M33	VCCSA19	VDDQ19	K6
M34	VCCSA20	VDDQ20	L12
M35	VCCSA21	VDDQ21	L6
M36	VCCSA22	VDDQ22	R6
		VDDQ23	T6
		VDDQ24	W6
		VDDQ25	Y12

570805_CFL_EDS_Vol1_Rev0.7
+VCC_IO
Max: 6400mA

+VCCIO

AG12	VCCIO1		
G15	VCCIO2		
G17	VCCIO3		
G19	VCCIO4	VCCPLL_OC1	BH13
G21	VCCIO5	VCCPLL_OC2	BJ13
H15	VCCIO6	VCCPLL_OC3	G11
H16	VCCIO7	VCCST	H30
H17	VCCIO8	VCCSTG2	H29
H19	VCCIO9		G30
H20	VCCIO10	VCCSTG1	
H21	VCCIO11		H28
H26	VCCIO12	VCCPLL1	J28
H27	VCCIO13	VCCPLL2	
J15	VCCIO14		
J16	VCCIO15		
J17	VCCIO16		
J19	VCCIO17		
J20	VCCIO18	VCCSA_SENSE	M38
J21	VCCIO19	VSSSA_SENSE	M37
J26	VCCIO20		
J27	VCCIO21	VCCIO_SENSE	H14
		12 OF 13 VSSIO_SENSE	J14

CFL-H_BGA1440
@

570805_CFL_EDS_Vol1_Rev0.7
+1.2V_VCCPLL_OC
Max: 130mA

+1.2V_VCCPLL_OC

+VCCST
Max: 60mA

+VCCSTG
Max: 20mA

+VCCST
Max: 150mA

VCCSA_SENSE_R
VSSSA_SENSE_R

RH201 100_0402_1%
RH202 0_0402_5%
RH470 0_0402_5%
RH469 100_0402_1%

+VCC_SA
VCC_SENSE_SA <88>
VSS_SENSE_SA <88>

VCCIO_SENSE <87>
VSSIO_SENSE <87>

1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC15, RC16 should be placed within 2 inches (50.8 mm) of CPU

+VCCSTG
1U_0201_6.3V6M CH105
1U_0201_6.3V6M CH106

+VCCST
10U_0402_6.3V6M CH107
10U_0402_6.3V6M CH108
1U_0201_6.3V6M CH109
10U_0402_6.3V6M CH110

+1.2V_VCCPLL_OC
1U_0201_6.3V6M CH336
1U_0201_6.3V6M CH337

+VCCST
1U_0402_10V6K CH334

+VCCST
470U_D6L_2VM_R15M CH335

close CPU ball H28,J28

Board Edge cap

+VCC_SA
22U_0603_6.3V6M CH134
22U_0603_6.3V6M CH135

+VCC_SA
10U_0402_6.3V6M CH111
10U_0402_6.3V6M CH112
10U_0402_6.3V6M CH113
10U_0402_6.3V6M CH114
10U_0402_6.3V6M CH115
10U_0402_6.3V6M CH116
10U_0402_6.3V6M CH117

+VCC_SA
1U_0201_6.3V6M CH133

Backside cap

+VCCIO
10U_0402_6.3V6M CH102
10U_0402_6.3V6M CH103
10U_0402_6.3V6M CH104

Backside cap

+VDDQ_DDR
22U_0603_6.3V6M CH129
22U_0603_6.3V6M CH130
22U_0603_6.3V6M CH131
22U_0603_6.3V6M CH132

+VDDQ_DDR
10U_0402_6.3V6M CH118
10U_0402_6.3V6M CH121
10U_0402_6.3V6M CH124
10U_0402_6.3V6M CH120
10U_0402_6.3V6M CH119
10U_0402_6.3V6M CH122
10U_0402_6.3V6M CH123
10U_0402_6.3V6M CH125
10U_0402_6.3V6M CH126
10U_0402_6.3V6M CH127
10U_0402_6.3V6M CH128

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Issued Date	2019/11/30	Deciphered Date	2027/06/21

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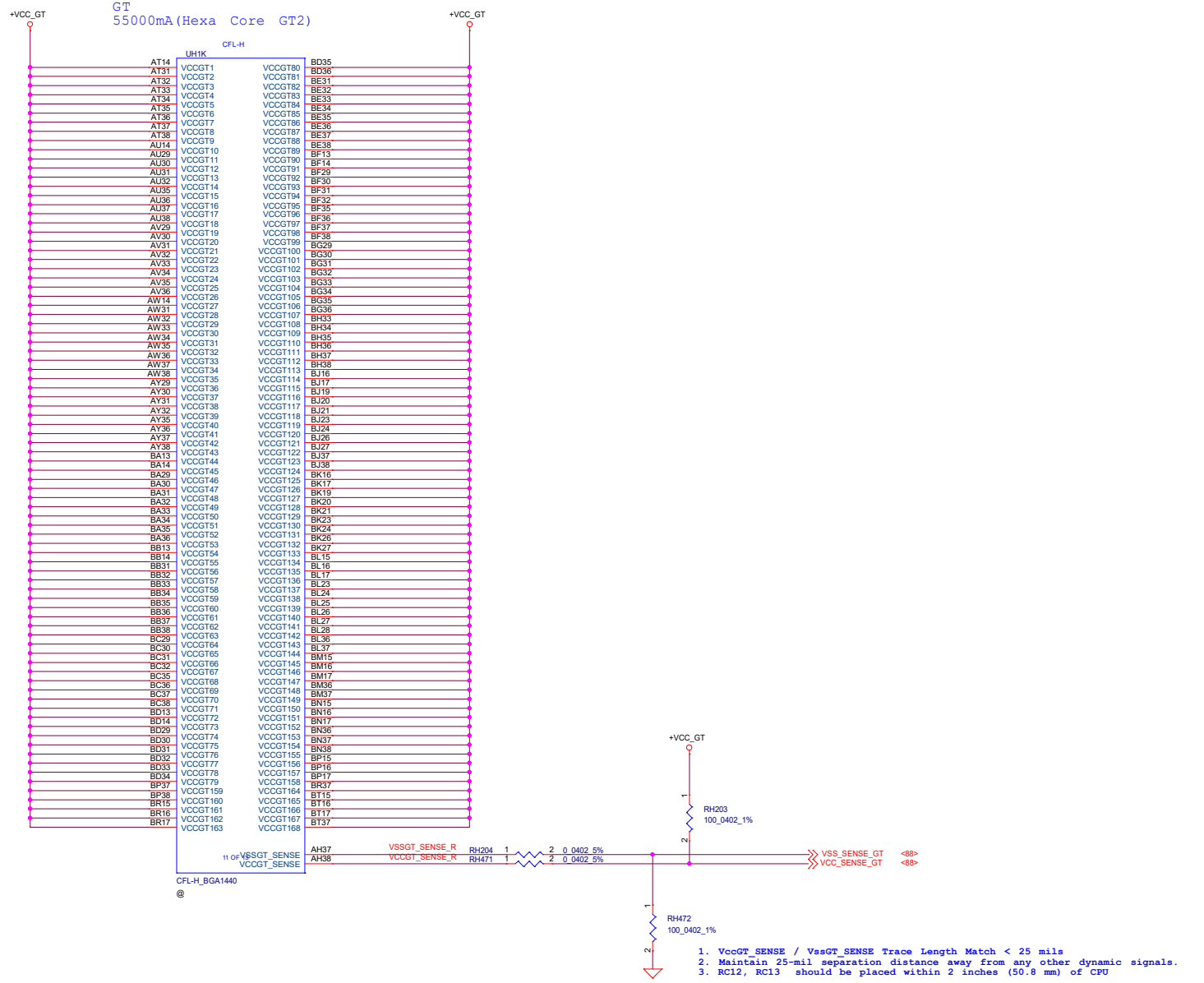
Title: P010-CPU(5/7) PWR,VDDR,VSA,VIO

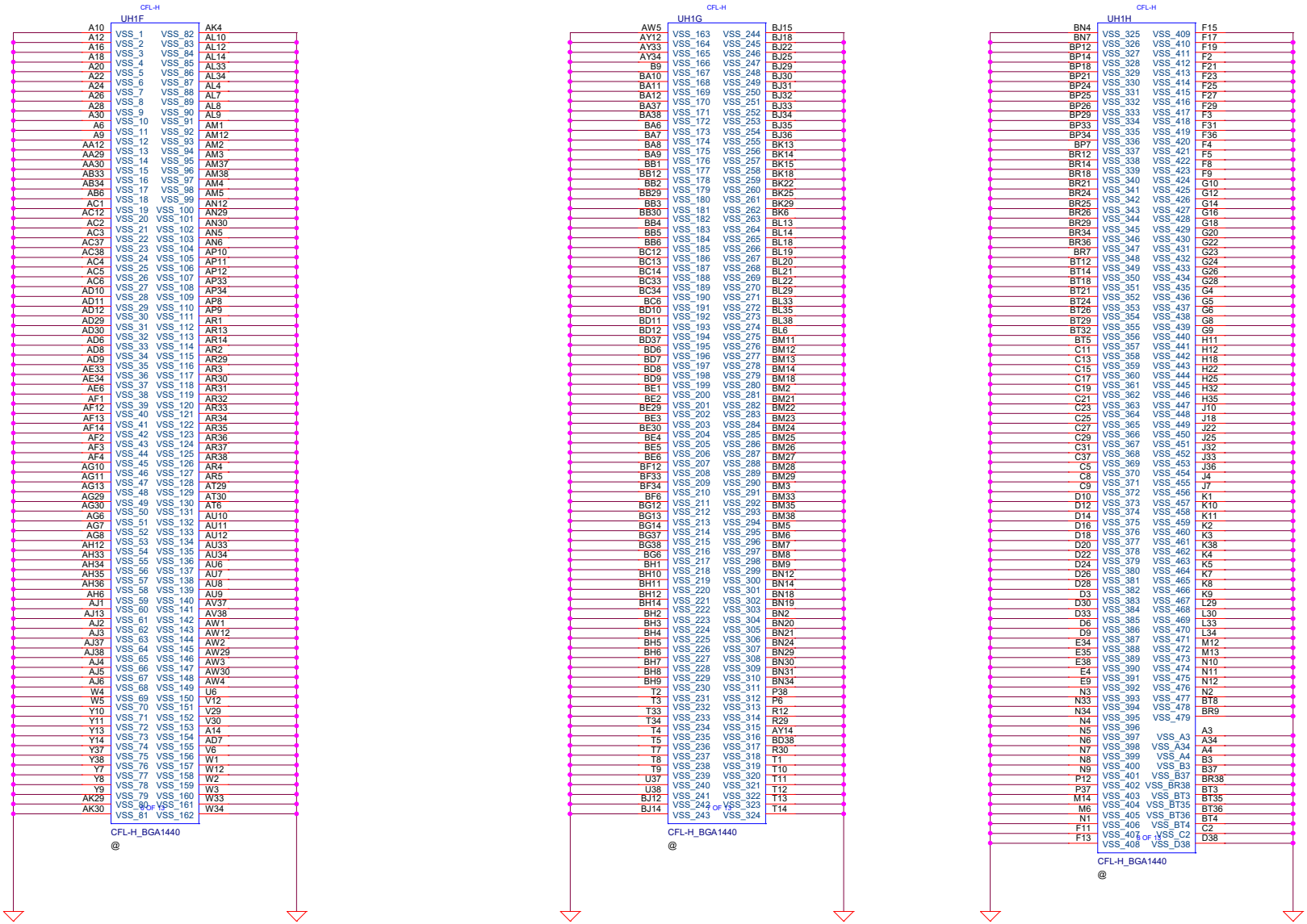
Size	Document Number	Rev
Custom		0.4(X03)

Date: Friday, November 22, 2019 Sheet 10 of 100



Security Classification	Compal Secret Data	Compal Electronics, Inc.	
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Title	P011-CPU(6/7) PWR,VGT	
Size: Custom	Document Number	Rev: 0.4(X03)
Date: Friday, November 22, 2019	Sheet 11 of 100	



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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P012-CPU(7/7) VSS**

Size	Document Number	Rev
Custom		0.4(X03)

Date: Friday, November 22, 2019 Sheet 12 of 100

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

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Issued Date	2019/11/30	Deciphered Date	2027/06/21

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Title: P013-PCH (1/7)SATA,DDC,PCIE,CNV

Size	Document Number	Rev
	LA-J191P	0.4(003)

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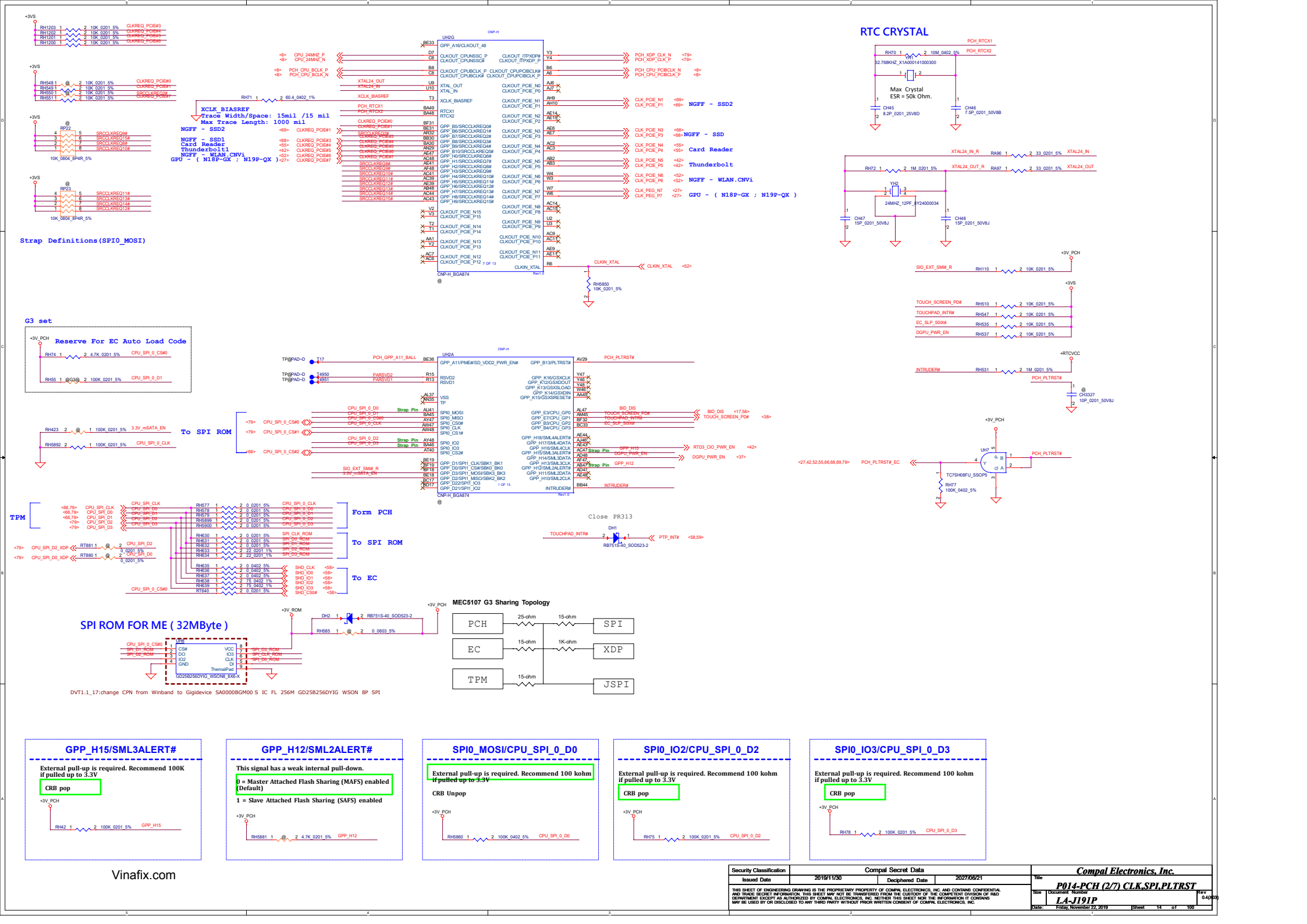

GPP_H15/SML3ALERT#

External pull-up is required. Recommend 100K if pulled up to 3.3V

CRB pop

GPP_H12/SML2ALERT#

This signal has a weak internal pull-down.

0 = Master Attached Flash Sharing (MAFS) enabled (Default)

1 = Slave Attached Flash Sharing (SAFS) enabled

SPI0_MOSI/CPU_SPI_0_D0

External pull-up is required. Recommend 100 kohm if pulled up to 3.3V

CRB Unpop

SPI0_IO2/CPU_SPI_0_D2

External pull-up is required. Recommend 100 kohm if pulled up to 3.3V

CRB pop

SPI0_IO3/CPU_SPI_0_D3

External pull-up is required. Recommend 100 kohm if pulled up to 3.3V

CRB pop

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Compal Electronics, Inc.			
Title	P014-PCH (2/7) CLK,SPI,PLTRST		
Size	Document Number		Rev
	LA-J191P		0.4(003)
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HDA_SDO / I2S0_TXD

ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE
1=Disable ME Protect (ME can be updated) 0=Enable ME Protect (ME cannot be updated)

RP14~RP15 close to PCH

<56> HDA_SYNC_AUDIO — RH266 1 2 33 0201 1% — HDA_SYNC
<56> HDA_SDOUT_AUDIO — RH267 1 2 33 0201 1% — HDA_SDOUT
<56> HDA_BITCLK_AUDIO — RH268 1 2 33 0201 1% — HDA_BITCLK

<52> PCM_CLK — RH1205 1 DAR@ 2 33 0201 1% — PCM_CLK_CPU
<52> PCM_OUT — RH1206 1 DAR@ 2 33 0201 1% — PCM_OUT_CPU
<52> PCM_IN — RH1207 1 DAR@ 2 33 0201 1% — PCM_IN_CPU
<52> PCM_SYNC — RH1208 1 DAR@ 2 33 0201 1% — PCM_SYNC_CPU

+RTCVCC — RH83 1 2 20K 0201 5% — PCH_SRTCRST#
CH52 1U 0201 6.3V6M

+RTCVCC — RH84 1 2 20K 0201 5% — PCH_RTCRST#
CH53 1U 0201 6.3V6M
close to BOT
CLRP1 SHORT PADS

+3V_PCH
RH458 1 2 1K 0201 5% MEM_SMBCLK
RH459 1 2 1K 0201 5% MEM_SMBDATA
RH460 1 2 1K 0201 5% SML1_SMBCLK
RH461 1 2 1K 0201 5% SML1_SMBDAT
RH501 1 2 1K 0201 1% SML0_SMBCLK
RH502 1 2 1K 0201 1% SML0_SMBDATA
RH557 2 1 10K 0201 5% KB_DET#

+3VS
RH463 1 2 1K 0201 5% PCH_SMBCLK
RH462 1 2 1K 0201 5% PCH_SMBDATA
RH516 1 DIS@ 2 10K 0201 5% DGPU_PWROK
RH599 1 2 10K 0201 5% IMVP_VR_PG
RH91 1 @ 2 100K 0201 5% SYS_PWROK

RH6907 1 UMA@ 2 10K 0201 5% DGPU_PWROK
RH5841 1 2 100K 0201 5% PCH_RSMRST#_AND

DVT2.1_08:EC read DGPU always high that thermal PL4 error,so it's should control by BOM optoin
Add RH6907(UMA@) ,change RH516 to DIS@

RH401 1 DS3@ 2 100K 0201 5% PCH_DPWROK_R
RH899 1 2 1M 0201 5% SIO_SLP_SUS#
CH899 1 @ 2 0.1U 0201 10V6K SIO_SLP_SUS#

RH1152 1 2 100K 0201 5% SIO_SLP_A#
RZ1150 1 2 100K 0201 5% SIO_SLP_S3#
RZ1151 1 2 100K 0201 5% SIO_SLP_S4#

75K 0201 1% RH114 CNV_RF_RESET#
75K 0201 1% RH728 CLKREQ_CNV#
DVT2_12 :change RH728 from SD000016T00 to SD000010380 follow intel design guide

Close to PCH

RH146 1 2 30 0201 1% — AUD_AZA_CPU_SDO_R
RH147 1 2 30 0201 1% — AUD_AZA_CPU_SDI_R
<6> AUD_AZA_CPU_SDO
<6> AUD_AZA_CPU_SDI_R
<6> AUD_AZA_CPU_SCLK

TP@PAD~D T121 — PCH_GPP_D7_BALL

<52> CLKREQ_CNV#
<52> CNV_RF_RESET#
<38> PCH_DMIC_DAT_R — RA102 1 2 0 0402 5% — PCH_DMIC_DAT
<38> PCH_DMIC_CLK_R — RA103 1 2 0 0402 5% — PCH_DMIC_CLK
<27,37,58,96> DGPU_PWROK
<69> KB_DET#

DVT1.1_41 :RA102,RA103 change from 33 ohm to 0 ohm for solve mic noise

<64,79> PCH_RTCRST# — PCH_RTCRST# — PCH_SRTCRST#

<58> PCH_DPWROK_EC — RH309 1 DS3@ 2 0 0402 5% — PCH_DPWROK_R

<42> SML0_ALERT#_TR — Strap Pin — PCH_SMB_ALERT#
<42> SML0_SMBCLK — Strap Pin — MEM_SMBCLK
<42> SML0_SMBDATA — Strap Pin — MEM_SMBDATA
<58> SML1_SMBCLK — Strap Pin — SML1_SMBCLK
<58> SML1_SMBDAT — Strap Pin — SML1_SMBDAT

PCH to DDR, XDP, FFS

+3VS
QH4A
MEM_SMBCLK — PCH_SMBCLK — PCH_SMBCLK <23,24,79>
PMDXB600UNE_DFN1010B-6
MEM_SMBDATA — PCH_SMBDATA — PCH_SMBDATA <23,24,79>
QH4B
PMDXB600UNE_DFN1010B-6

UH2D — CNP-H

HDA_BITCLK	BD11	HDA_BCLK/I2S0_SCLK	
HDA_SDIN0_AUDIO	BE11	HDA_SDI0/I2S0_RXD	
HDA_SDOUT	BF12	HDA_SDO/I2S0_TXD	Strap Pin
HDA_SYNC	BG13	HDA_SYNC/I2S0_SFRM	
PCM_CLK_CPU	BE10	HDA_RST#/I2S1_SCLK	
PCM_OUT_CPU	BF10	HDA_SDI1/I2S1_RXD	
PCM_IN_CPU	BE12	I2S1_TXD/SNDW2_DATA	
PCM_SYNC_CPU	BD12	I2S1_SFRM/SNDW2_CLK	
AUD_AZA_CPU_SDO_R	AM2	HDACPU_SDO	
AUD_AZA_CPU_SDI_R	AN3	HDACPU_SDI	
AUD_AZA_CPU_SCLK_R	AM3	HDACPU_SCLK	
PCH_GPP_D7_BALL	AV18	GPP_D8/I2S2_SCLK	
	AW18	GPP_D7/I2S2_RXD	
	BA17	GPP_D6/I2S2_TXD/MODEM_CLKREQ	
	BE16	GPP_D5/I2S2_SFRM/CNV_RF_RESET#	
	BF15	GPP_D20/DMIC_DATA0/SNDW4_DATA	
	BD16	GPP_D19/DMIC_CLK0/SNDW4_CLK	
DGPU_PWROK	AV16	GPP_D18/DMIC_DATA1/SNDW3_DATA	
KB_DET#	AW15	GPP_D17/DMIC_CLK1/SNDW3_CLK	
PCH_RTCRST#	BE47	RTCRST#	
PCH_SRTCRST#	BD46	SRTCRST#	
PCH_PWROK	AY42	PCH_PWROK	
PCH_RSMRST#_AND	BA47	RSMRST#	
PCH_DPWROK_R	AW41	DSW_PWROK	
PCH_SMB_ALERT#	BE25	GPP_C2/SMBALERT#	Strap Pin
MEM_SMBCLK	BE26	GPP_C0/SMBCLK	
MEM_SMBDATA	BF26	GPP_C1/SMBDATA	
SML0_ALERT#_TR	BF24	GPP_C5/SML0ALERT#	Strap Pin
SML0_SMBCLK	BF25	GPP_C3/SML0CLK	
SML0_SMBDATA	BE24	GPP_C4/SML0DATA	
GPP_B23	BD33	GPP_B23/SML1ALERT#/PCHHOT#	Strap Pin
SML1_SMBCLK	BF27	GPP_C6/SML1CLK	
SML1_SMBDAT	BE27	GPP_C7/SML1DATA	
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		@	Rev1.0

	BF36	GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF#	
CLKRUN#	AV32	GPP_A8/CLKRUN#	
PM_LANPHY_ENABLE	BF41	GPD11/LANPHYPC	
SIO_SLP_WLAN#	BD42	GPD9/SLP_WLAN#	
VRALERT#	BB46	DRAM_RESET#	
	BE32	GPP_B2/VRALERT#	
	BE29	GPP_B1/GSPI1_CS1#/TIME_SYNC1	
TS_I2C_RST#	R47	GPP_B0/GSPI0_CS1#	
I2C2_IRQ_TS	AP29	GPP_K17/ADR_COMPLETE	
SYS_PWROK	AU3	GPP_B11/I2S_MCLK	
PCH_PCIE_WAKE#	BB47	SYS_PWROK	
SIO_SLP_A#	BE40	WAKE#	
PCH_SLP_LAN#	BF40	GPD6/SLP_A#	
	BC28	SLP_LAN#	
	BF42	GPP_B12/SLP_S0#	
SIO_SLP_S4#	BE42	GPD4/SLP_S3#	
	BC42	GPD5/SLP_S4#	
		GPD10/SLP_S5#	
PCH_BATLOW#	BE45	GPD8/SUSCLK	
SUSACK#_R	BF44	GPD0/BATLOW#	
ME_SUS_PWR_ACK_R	BE35	GPP_A15/SUSACK#	
	BC37	GPP_A13/SUSWARN#/SUSPWRDNACK	
LAN_WAKE#	BG44	GPD2/LAN_WAKE#	
AC_PRESENT	BG42	GPD1/ACPRESENT	
SIO_SLP_SUS#_L	BD39	SLP_SUS#	
	BF46	GPD3/PWRBTN#	
SYS_RESET#	AU2	SYS_RESET#	
SPKR	AW29	GPP_B14/SPKR	Strap Pin
	AE3	CPUPWRGD	
PCH_ITP_PMODE	AL3	ITP_PMODE	
PCH_JTAGX	AH4	PCH_JTAGX	
PCH_JTAG_TMS	AJ4	PCH_JTAG_TMS	
PCH_JTAG_TDO	AH3	PCH_JTAG_TDO	
PCH_JTAG_TDI	AH2	PCH_JTAG_TDI	
PCH_JTAG_TCK	AJ3	PCH_JTAG_TCK	

T6020 PAD~D — 0 0201 5% 2 — 1 RH5872 — SUSCLK <52>
SIO_SLP_SUS#_L 0 0201 5% 2 — 1 RH587 — SIO_SLP_SUS# <58>

Strap Definitions(ITP_PMODE)

<88,99> IMVP_VR_PG — IMVP_VR_PG — UH14 — PCH_PWROK
<58> RUNPWROK
TC7SH08FU_SSOP5
RH529 100K 0201 5%

DVT2_11:Power sequence fix & Aligne schematic to Olympic
Add NeT name "EN_1.8_PRIM","EN_1.0VA"
Add CH54(SE000000QL10),RH702(SD043470180)
Add RH701(SD043000980),CH55(SE000000QL10) but un-pop

+3VALW
UZ123
<15,58> PCH_RSMRST#_EC_R
<15,50,83> ALW_PWRGD_3V_5V
ALW_PWRGD_3V_5V — PCH_RSMRST#_AND
TC7SH08FU_SSOP5~D
RH215 1 2 0 0201 5% PCH_DPWROK_R

RSMRST circuit

RH215	
POP	NO Support Deep sleep
DE-POP	Support Deep sleep

@RH701 0 0201 5%
<17> VCCDSW_EN_GPIO
<58> VCCDSW_EN — RH6905 1 2 0 0201 5%
<15,50,83> ALW_PWRGD_3V_5V — RH6906 1 2 0 0201 5%
<15,58> PCH_RSMRST#_EC_R — R5873 1 @ 2 200K 0201 1% — PCH_RSMRST#_G
CA252 470P 0201 25V7K
QT14 2N7002KW_SOT323-3

DVT2_11 : Change CA252 from 330P to 470P to fix WDT sequence
PCH_PRIM_EN is low intervel time = 40 ms
R5873 change to unpop,EC can internal pull down
DVT2_10 : Change QT14 from SB000005T00 to SB000009Q80 follow Olympic schematic

EC WDT reset circuit

0 0201 5% 2@DS3@ 1 RH699 — SIO_SLP_SUS#
PCH_PRIM_EN <77,78>
RH700 1 2 0 0201 5% — EN_1.8V_PRIM <95>
CH55 1U 0402 10V6K
RH702 1 2 4.7K 0201 5% — EN_1.0VA <84>
CH54 1U 0402 10V6K

Reserve for EMI
EMC@ CH50 1 2 8.2P 0201 25V8D — HDA_BITCLK
RF@ CH51 1 2 2P 0201 25V8B — HDA_SDOUT
EMC@ CD3325 1 2 2P 0201 25V8B — HDA_SYNC
EMC@ CD3324 1 2 2P 0201 25V8B — HDA_SDIN0_AUDIO

+3V_PCH
PM_LANPHY_ENABLE — RH5842 1 @ 2 10K 0201 5%
PCH_PCIE_WAKE# — RH453 1 2 1K 0201 5%
PCH_BATLOW# — RH515 1 2 8.2K 0201 1%
AC_PRESENT — RH533 1 2 8.2K 0201 1%
LAN_WAKE# — RH545 1 2 10K 0201 5%
VRALERT# — RH5837 2 @ 1 4.7K 0201 5%

+3V_PCH
ME_SUS_PWR_ACK_R — RH506 1 @ 2 1M 0201 5%
SYS_RESET# — RH571 1 2 8.2K 0201 1%

+3VS
CLKRUN# — RH85 1 @ 2 8.2K 0201 1%

Strap Definitions(GPP_B14 / SPKR)

+3V_PCH
SPKR — 4.7K 0201 5% 2 @ 1 RH82

Top Swap Override (internal PD)	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Strap Definitions(GPP_C2 /SMBALERT#)

+3V_PCH
PCH_SMB_ALERT# — 4.7K 0201 5% 2 @ 1 RH505

TLS CONFIDENTIALITY	
HIGH	vPRO
LOW(DEFAULT)	non-vPRO

Strap Definitions(GPP_C5 /SML0ALERT#)

+3V_PCH
SML0_ALERT#_TR — 4.7K 0201 5% 2 — 1 RH503

EC interface	
HIGH	ESPI
LOW(DEFAULT)	LPC

Strap Definitions(GPP_B23 /SML1ALERT# /PCHHOT#)

+3V_PCH
GPP_B23 — 150K 0201 5% 2 — 1 RH504

PCHHOT# (IntelR DCI-OOB)	
HIGH	Enable
LOW(DEFAULT)	Disable

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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

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Title: P015-PCH (3/7) PM,HDA,SMB,JTAG

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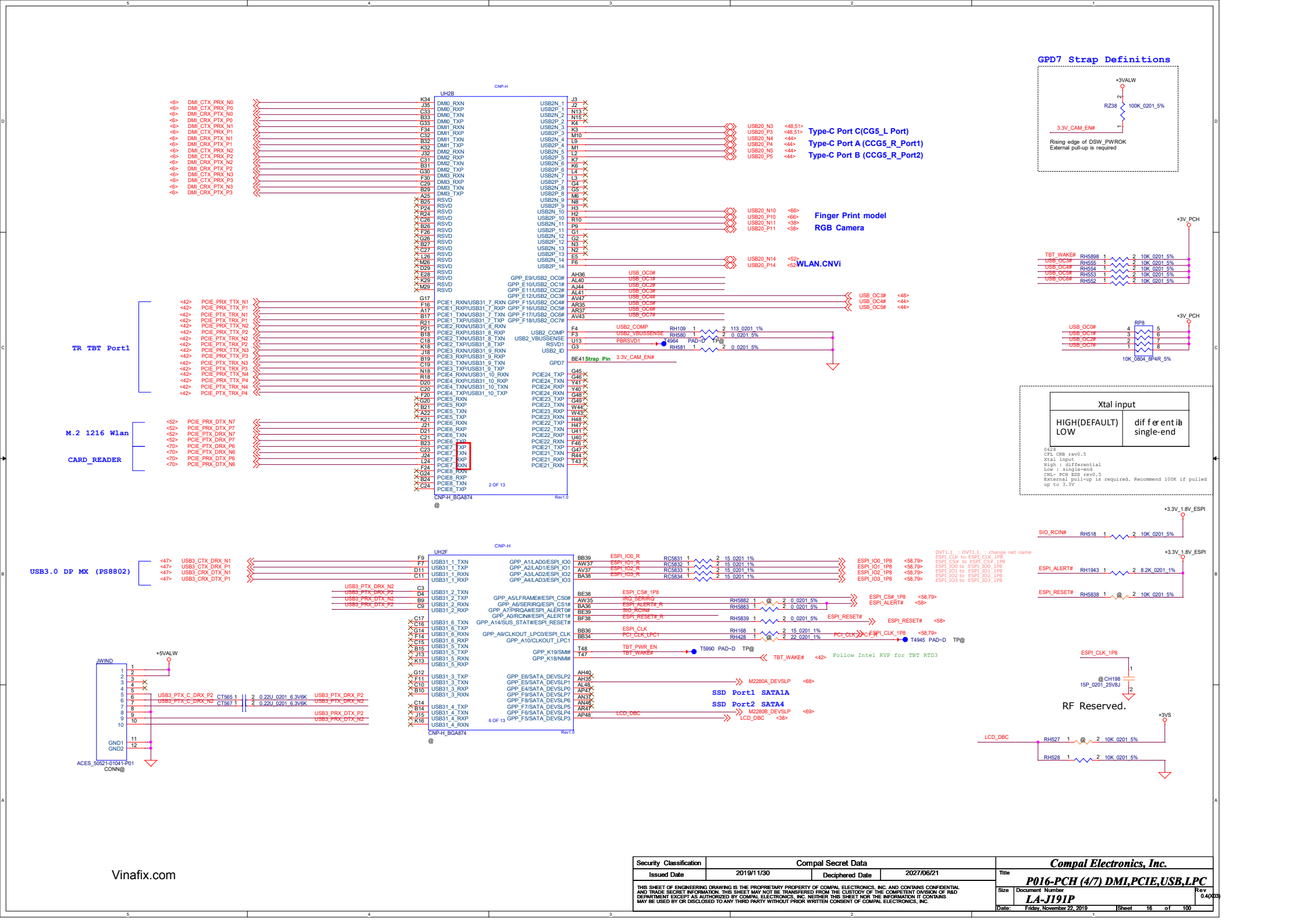
GPD7 Strap Definitions
+3VALW
RZ38 100K_0201_5%
3.3V_CAM_EN#
Rising edge of DSW_PWROK
External pull-up is required
UH2B
CNP-H
DMI0_RXN DMI0_RXP DMI0_TXN DMI0_TXP DMI1_RXN DMI1_RXP DMI1_TXN DMI1_TXP DMI2_RXN DMI2_RXP DMI2_TXN DMI2_TXP DMI3_RXN DMI3_RXP DMI3_TXN DMI3_TXP
USB2N_1 USB2P_1 USB2N_2 USB2P_2 USB2N_3 USB2P_3 USB2N_4 USB2P_4 USB2N_5 USB2P_5 USB2N_6 USB2P_6 USB2N_7 USB2P_7 USB2N_8 USB2P_8 USB2N_9 USB2P_9 USB2N_10 USB2P_10 USB2N_11 USB2P_11 USB2N_12 USB2P_12 USB2N_13 USB2P_13 USB2N_14 USB2P_14
USB20_N3 USB20_P3 USB20_N4 USB20_P4 USB20_N5 USB20_P5
Type-C Port C(CG5_L Port)
Type-C Port A (CCG5_R_Port1)
Type-C Port B (CCG5_R_Port2)
USB20_N10 USB20_P10 USB20_N11 USB20_P11
Finger Print model
RGB Camera
USB20_N14 USB20_P14
WLAN.CNVi
RSVD
GPP_E9/USB2_OC0# GPP_E10/USB2_OC1# GPP_E11/USB2_OC2# GPP_E12/USB2_OC3# GPP_F15/USB2_OC4# GPP_F16/USB2_OC5# GPP_F17/USB2_OC6# GPP_F18/USB2_OC7#
USB_OC0# USB_OC1# USB_OC2# USB_OC3# USB_OC4# USB_OC5# USB_OC6# USB_OC7#
USB_OC3# USB_OC4# USB_OC5#
TR TBT Port1
PCIE_PRX_TTX_N1 PCIE_PRX_TTX_P1 PCIE_PRX_TTX_N1 PCIE_PTX_TRX_P1 PCIE_PTX_TTX_N2 PCIE_PTX_TRX_P2 PCIE_PTX_TRX_N2 PCIE_PRX_TTX_P2 PCIE_PTX_TRX_N3 PCIE_PRX_TTX_P3 PCIE_PRX_TTX_N3 PCIE_PTX_TRX_P3 PCIE_PTX_TRX_N4 PCIE_PRX_TTX_P4 PCIE_PTX_TRX_N4 PCIE_PTX_TRX_P4
PCIE1_RXN/USB31_7_RXN PCIE1_RXP/USB31_7_RXP PCIE1_TXN/USB31_7_TXN PCIE1_TXP/USB31_7_TXP PCIE2_RXN/USB31_8_RXN PCIE2_RXP/USB31_8_RXP PCIE2_TXN/USB31_8_TXN PCIE2_TXP/USB31_8_TXP PCIE3_RXN/USB31_9_RXN PCIE3_RXP/USB31_9_RXP PCIE3_TXN/USB31_9_TXN PCIE3_TXP/USB31_9_TXP PCIE4_RXN/USB31_10_RXN PCIE4_RXP/USB31_10_RXP PCIE4_TXN/USB31_10_TXN PCIE4_TXP/USB31_10_TXP PCIE5_RXN PCIE5_RXP PCIE5_TXN PCIE5_TXP PCIE6_RXN PCIE6_RXP PCIE6_TXN PCIE6_TXP PCIE7_TXP PCIE7_TXN PCIE7_RXP PCIE7_RXN PCIE8_RXN PCIE8_RXP PCIE8_TXN PCIE8_TXP
USB2_COMP USB2_VBUSSENSE RSVD1 USB2_ID GPD7
PCIE24_TXP PCIE24_TXN PCIE24_RXP PCIE24_RXN PCIE23_TXP PCIE23_TXN PCIE23_RXP PCIE23_RXN PCIE22_TXP PCIE22_TXN PCIE22_RXP PCIE22_RXN PCIE21_TXN PCIE21_RXP PCIE21_RXN
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Rev1.0
USB2_COMP RH109 113_0201_1%
USB2_VBUSSENSE RH580 0_0201_5%
PBRSVD1 T4964 PAD-D TP@ RH581 0_0201_5%
BE41 Strap Pin 3.3V_CAM_EN#
+3V_PCH
TBT_WAKE# RH5898 10K_0201_5%
USB_OC3# RH555 10K_0201_5%
USB_OC4# RH554 10K_0201_5%
USB_OC5# RH553 10K_0201_5%
USB_OC6# RH552 10K_0201_5%
RP8
USB_OC0# USB_OC1# USB_OC2# USB_OC7#
10K_0804_8P4R_5%
Xtal input
HIGH(DEFAULT) dif f er ent ib
LOW single-end
0628
CFL CRB rev0.5
Xtal input
High : differential
Low : single-end
CNL- PCH EDS rev0.5
External pull-up is required. Recommend 100K if pulled up to 3.3V
M.2 1216 Wlan
CARD_READER
PCIE_PRX_DTX_N7 PCIE_PRX_DTX_P7 PCIE_PTX_DRX_N7 PCIE_PTX_DRX_P7 PCIE_PTX_DRX_N6 PCIE_PRX_DTX_P6 PCIE_PRX_DTX_N6
USB3.0 DP MX (PS8802)
USB3_CTX_DRX_N1 USB3_CTX_DRX_P1 USB3_CRX_DTX_N1 USB3_CRX_DTX_P1
USB3_PTX_DRX_N2 USB3_PTX_DRX_P2 USB3_PRX_DTX_N2 USB3_PRX_DTX_P2
UH2F
CNP-H
USB31_1_TXN USB31_1_TXP USB31_1_RXN USB31_1_RXP USB31_2_TXN USB31_2_TXP USB31_2_RXN USB31_2_RXP USB31_6_TXN USB31_6_TXP USB31_6_RXN USB31_6_RXP USB31_5_TXN USB31_5_TXP USB31_5_RXN USB31_5_RXP USB31_3_TXP USB31_3_TXN USB31_3_RXP USB31_3_RXN USB31_4_TXP USB31_4_TXN USB31_4_RXP USB31_4_RXN
GPP_A1/LAD0/ESPI_IO0 GPP_A2/LAD1/ESPI_IO1 GPP_A3/LAD2/ESPI_IO2 GPP_A4/LAD3/ESPI_IO3 GPP_A5/LFRAME#/ESPI_CS0# GPP_A6/SERIRQ/ESPI_CS1# GPP_A7/PIRQA#/ESPI_ALERT0# GPP_A0/RCIN#/ESPI_ALERT1# GPP_A14/SUS_STAT#/ESPI_RESET# GPP_A9/CLKOUT_LPC0/ESPI_CLK GPP_A10/CLKOUT_LPC1 GPP_K19/SMI# GPP_K18/NMI# GPP_E6/SATA_DEVSLP2 GPP_E5/SATA_DEVSLP1 GPP_E4/SATA_DEVSLP0 GPP_F9/SATA_DEVSLP7 GPP_F8/SATA_DEVSLP6 GPP_F7/SATA_DEVSLP5 GPP_F6/SATA_DEVSLP4 GPP_F5/SATA_DEVSLP3
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CNP-H_BGA874
Rev1.0
ESPI_IO0_R ESPI_IO1_R ESPI_IO2_R ESPI_IO3_R
RC5831 RC5832 RC5833 RC5834 15_0201_1%
ESPI_IO0_1P8 ESPI_IO1_1P8 ESPI_IO2_1P8 ESPI_IO3_1P8
DVT1.1_ : DVT1.1_ : change net name
ESPI_CLK to ESPI_CLK_1P8
ESPI_CS# to ESPI_CS#_1P8
ESPI_IO0 to ESPI_IO0_1P8
ESPI_IO1 to ESPI_IO1_1P8
ESPI_IO2 to ESPI_IO2_1P8
ESPI_IO3 to ESPI_IO3_1P8
ESPI_CS#_1P8 IRQ_SERIRQ ESPI_ALERT#_R SIO_RCIN# ESPI_RESET#_R ESPI_CLK PCI_CLK_LPC1
RH5882 RH5883 RH5839 RH168 RH428 0_0201_5% 15_0201_1% 22_0201_1%
ESPI_CS#_1P8 ESPI_ALERT# ESPI_RESET# ESPI_CLK_1P8 PCI_CLK2_LPC_R
T4945 PAD-D TP@
TBT_PWR_EN TBT_WAKE#
T5990 PAD-D TP@
TBT_WAKE# <42>
Follow Intel RVP for TBT RTD3
M2280A_DEVSLP <68>
SSD Port1 SATA1A
SSD Port2 SATA4
LCD_DBC
M2280B_DEVSLP <69>
LCD_DBC <38>
+3.3V_1.8V_ESPI
SIO_RCIN# RH518 10K_0201_5%
ESPI_ALERT# RH1943 8.2K_0201_1%
ESPI_RESET# RH5838 10K_0201_5%
ESPI_CLK_1P8
@CH198 15P_0201_25V8J
RF Reserved.
+3VS
LCD_DBC
RH527 10K_0201_5%
RH528 10K_0201_5%
JWIND
+5VALW
USB3_PTX_C_DRX_P2 USB3_PTX_C_DRX_N2
CT565 CT567 0.22U_0201_6.3V6K
USB3_PTX_DRX_P2 USB3_PTX_DRX_N2
USB3_PRX_DTX_P2 USB3_PRX_DTX_N2
GND1 GND2
ACES_50521-01041-P01
CONN@
Vinafix.com
Security Classification Compal Secret Data
Issued Date 2019/11/30 Deciphered Date 2027/06/21
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Title P016-PCH (4/7) DMI,PCIE,USB,LPC
Size Document Number LA-J191P Rev 0.4(003)
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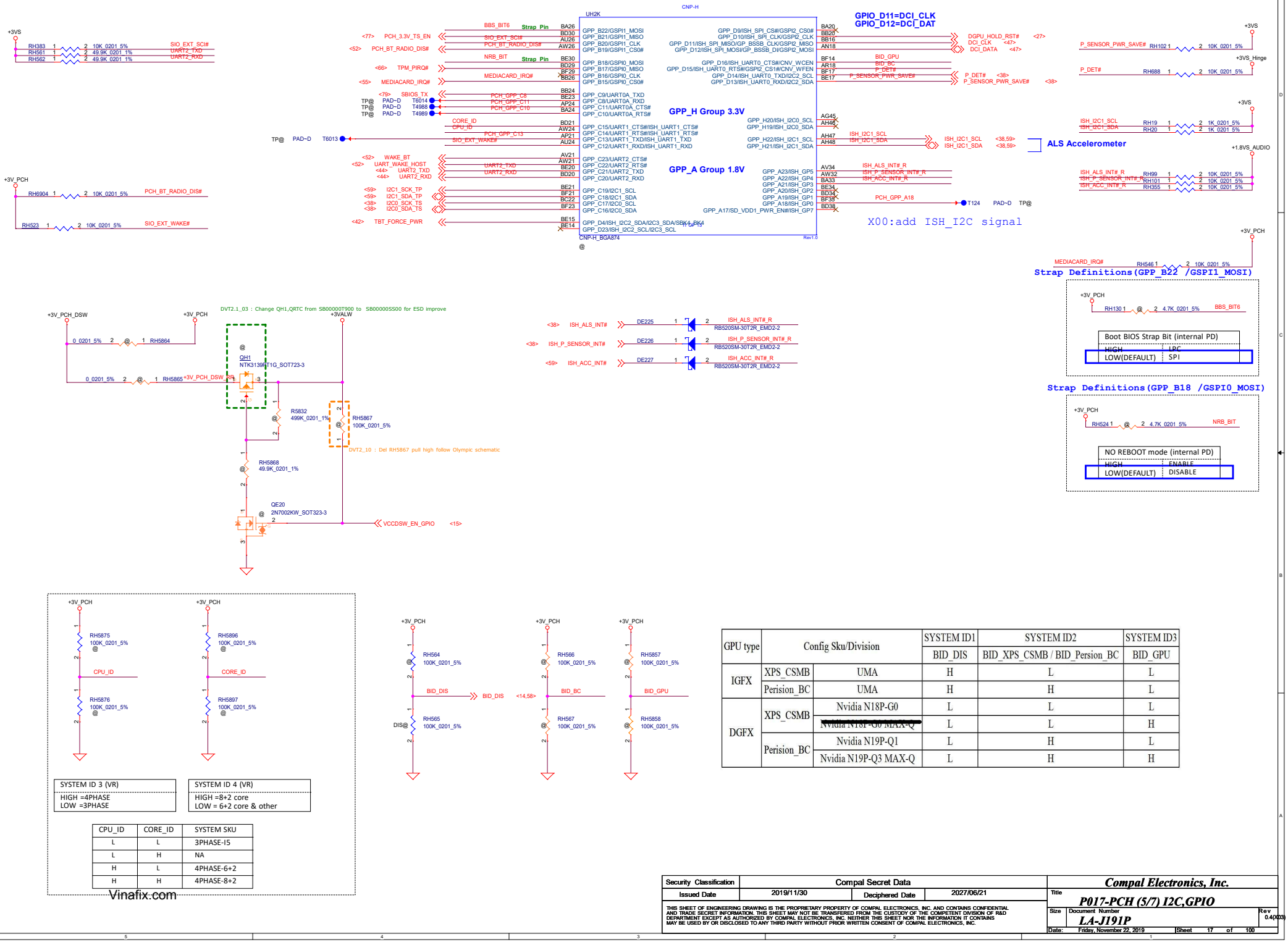

CPU_ID	CORE_ID	SYSTEM SKU
L	L	3PHASE-I5
L	H	NA
H	L	4PHASE-6+2
H	H	4PHASE-8+2

GPU type	Config Sku/Division		SYSTEM ID1	SYSTEM ID2	SYSTEM ID3
			BID_DIS	BID_XPS_CSMB / BID_Persion_BC	BID_GPU
IGFX	XPS_CSMB	UMA	H	L	L
	Perision_BC	UMA	H	H	L
DGFX	XPS_CSMB	Nvidia N18P-G0	L	L	L
		~~Nvidia N18P-G0 MAX-Q~~	L	L	H
	Perision_BC	Nvidia N19P-Q1	L	H	L
		Nvidia N19P-Q3 MAX-Q	L	H	H

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Issued Date	2019/11/30	Deciphered Date	2027/06/21

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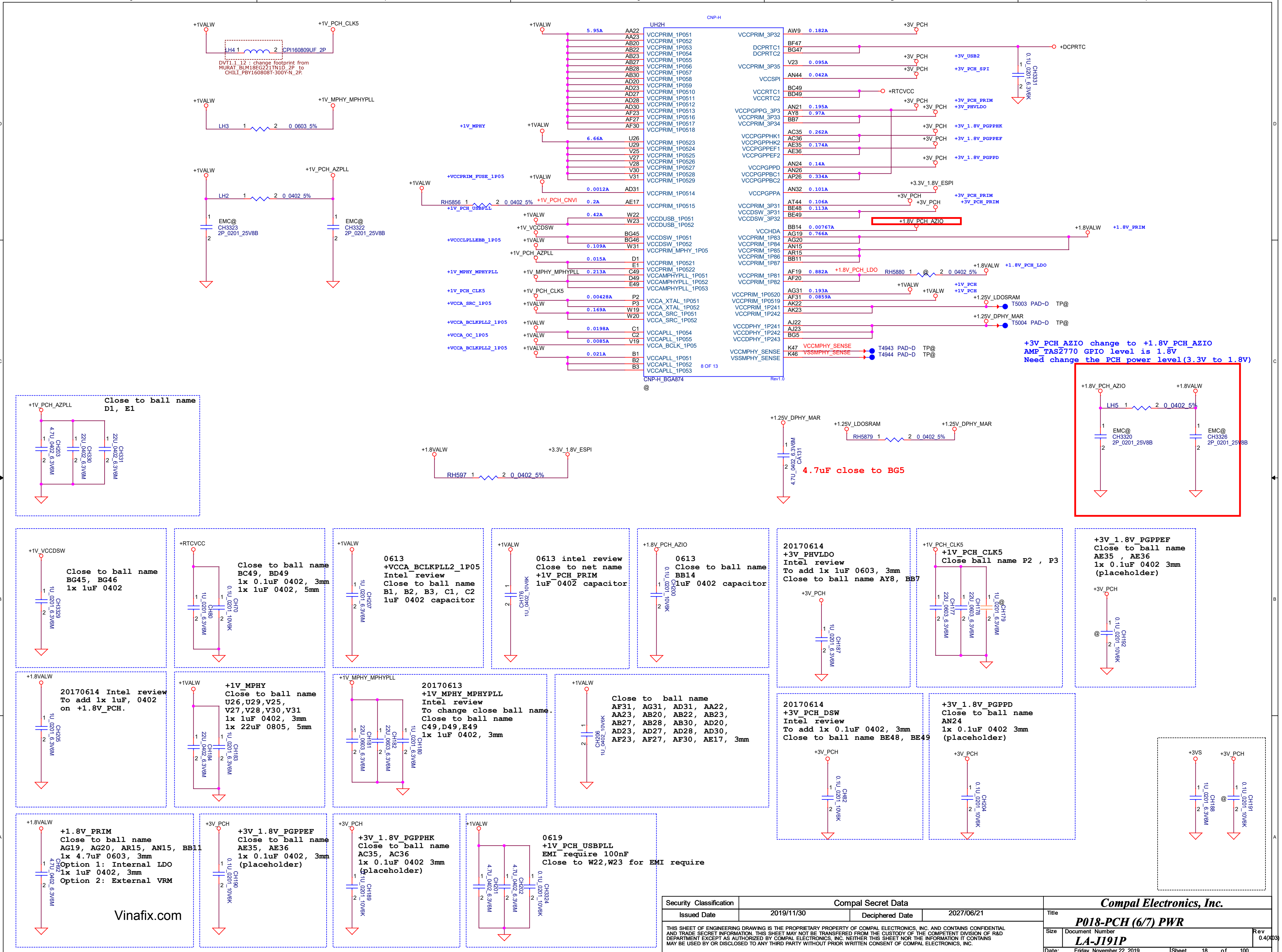
Compal Electronics, Inc.

Title: **P017-PCH (5/7) I2C,GPIO**

Size	Document Number	Rev
	LA-J191P	0.4(003)

Date: Friday, November 22, 2019 | Sheet 17 of 100



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Issued Date	2019/11/30	Deciphered Date	2027/06/21

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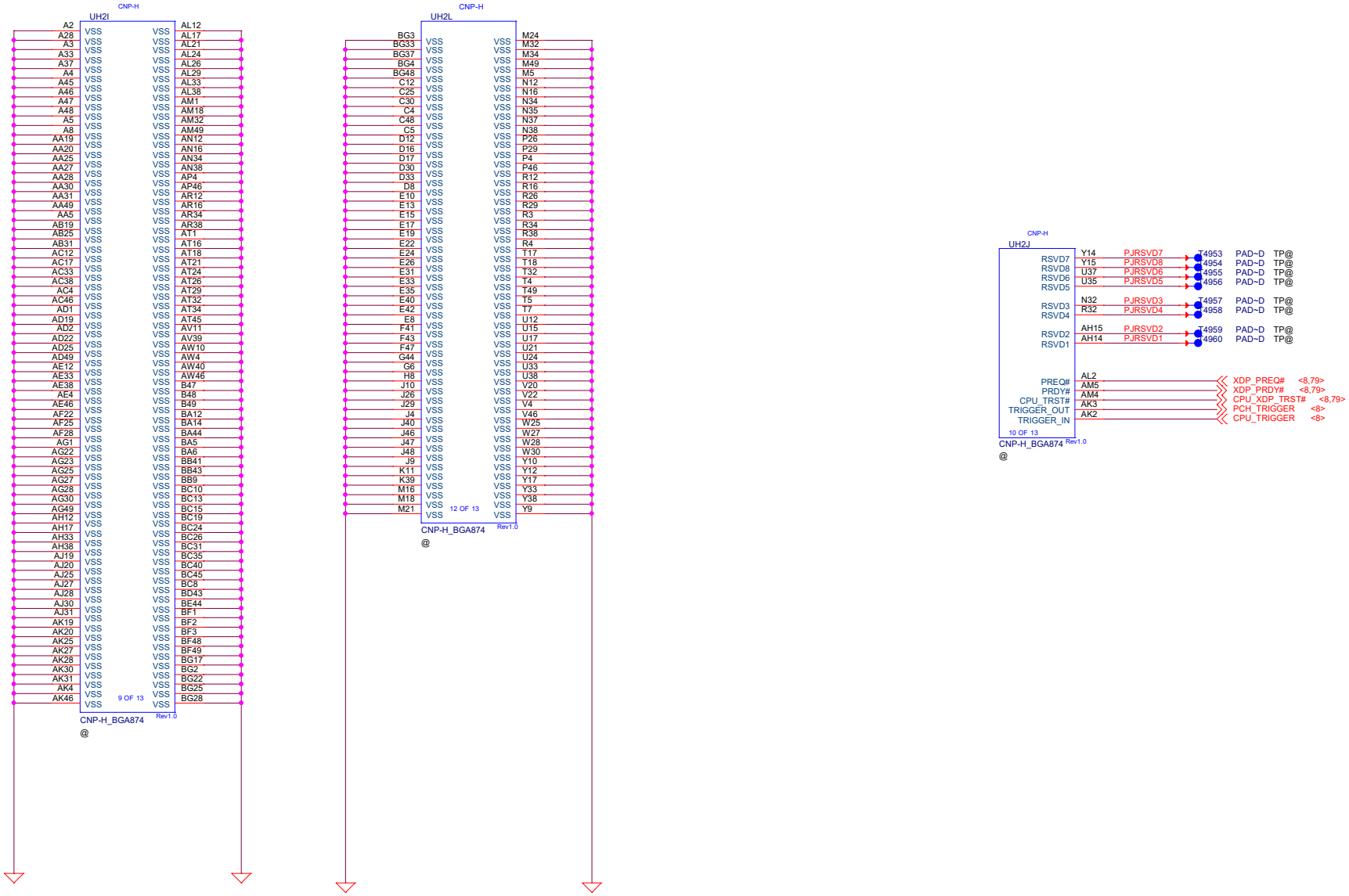
Compal Electronics, Inc.

Title: **P018-PCH (6/7) PWR**

Size	Document Number	Rev
	LA-J191P	0.4(X03)

Date: Friday, November 22, 2019 Sheet 18 of 100



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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P019-PCH (7/7) VSS**

Size	Document Number	Rev
	LA-J191P	0.4(X03)

Date: Friday, November 22, 2019 Sheet 19 of 100

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

Compal Electronics, Inc.		
Title: P020-Reserve		
Size	Document Number: LA-J191P	Rev: 0.4(X03)
Date: Friday, November 22, 2019	Sheet 20 of 100	

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

Compal Electronics, Inc.		
Title: P021-Reserve		
Size	Document Number: LA-J191P	Rev: 0.4(X03)
Date: Friday, November 22, 2019	Sheet 21 of 100	

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

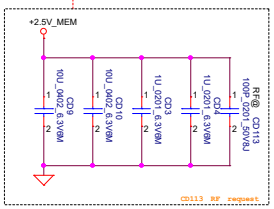
Compal Electronics, Inc.		
Title: P022-Reserve		
Size	Document Number: LA-J191P	Rev: 0.4(X03)
Date: Friday, November 22, 2019	Sheet 22 of 100	

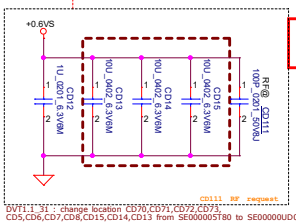
Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

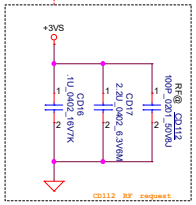
Layout Note:
Place near JDIMM1.255

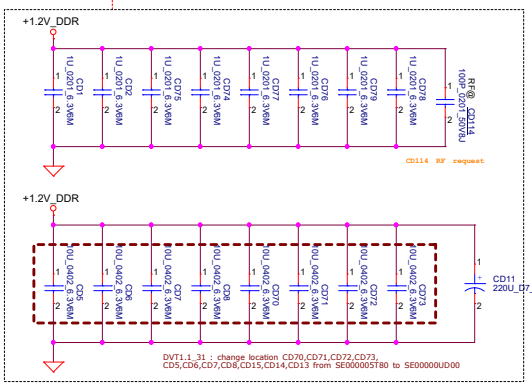
Layout Note:
Place near JDIMM1



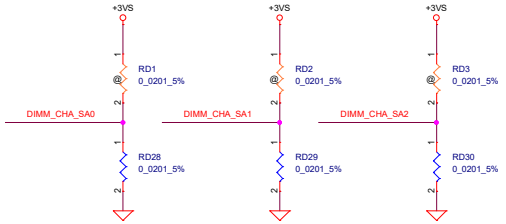


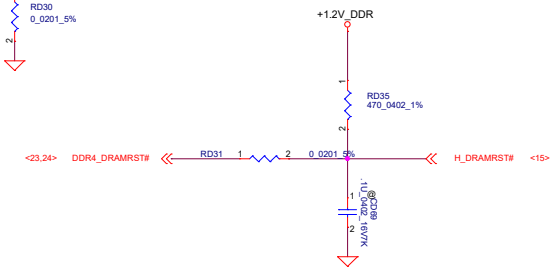
DVT1.1_31 : change location CD70,CD71,CD72,CD73,
CD5,CD6,CD7,CD8,CD15,CD14,CD13 from SE000005T80 to SE000000UD00



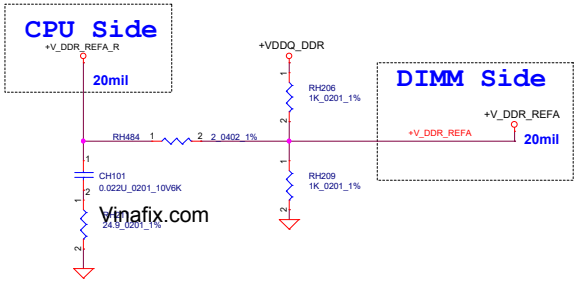


DVT1.1_31 : change location CD70,CD71,CD72,CD73,
CD5,CD6,CD7,CD8,CD15,CD14,CD13 from SE000005T80 to SE000000UD00





VREF traces should be at least 20 mils wide with 20 mils spacing to other signals



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Compal Electronics, Inc.

Title: P023-DDR4 DIMMA

Size: | Document Number: LA-J191P | Rev: 0.4(003)

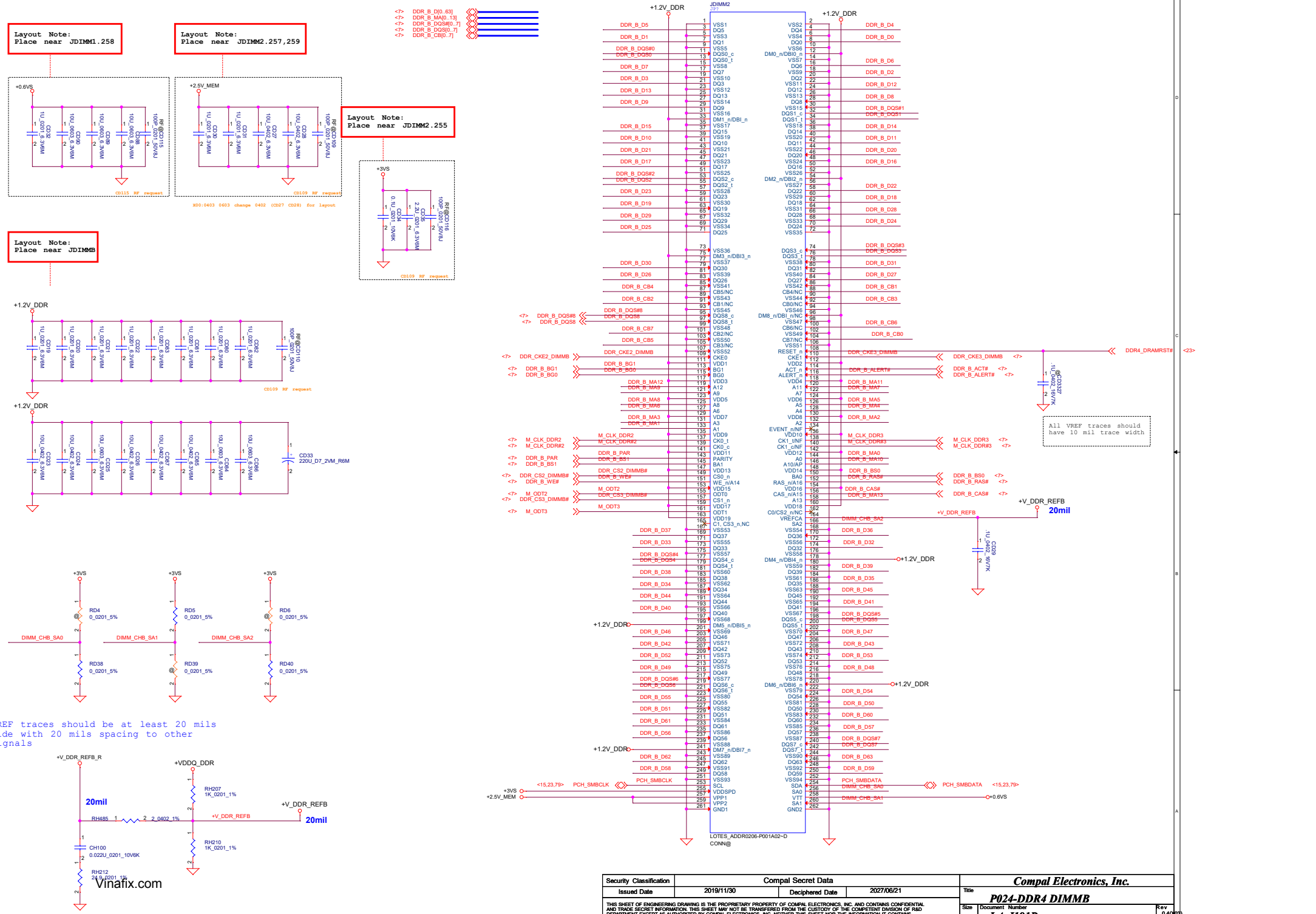
Date: Friday, November 22, 2019 | Sheet 23 of 100

Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.255

Layout Note:
Place near JDIMMB



Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Compal Electronics, Inc.			
Title	P024-DDR4 DIMMB		
Size	Document Number		Rev
	LA-J191P		0.4(003)
Date:	Friday, November 22, 2019	Sheet	24 of 100

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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

Compal Electronics, Inc.

Title: *P025-Reserve*

Size | Document Number: *LA-J191P* | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 25 of 100

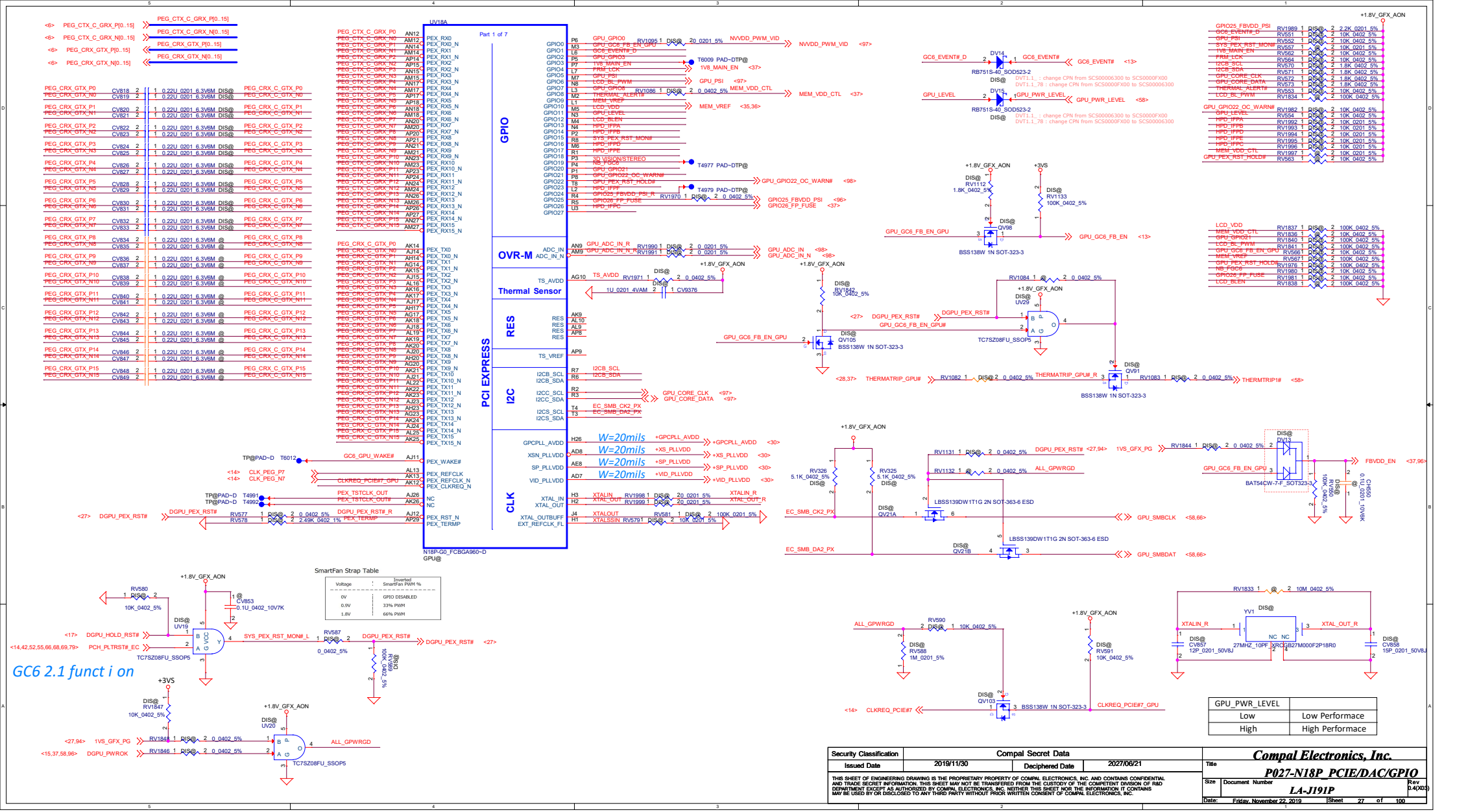
Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

Compal Electronics, Inc.

Title: *P026-Reserve*

Size | Document Number: *LA-J191P* | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 26 of 100



Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

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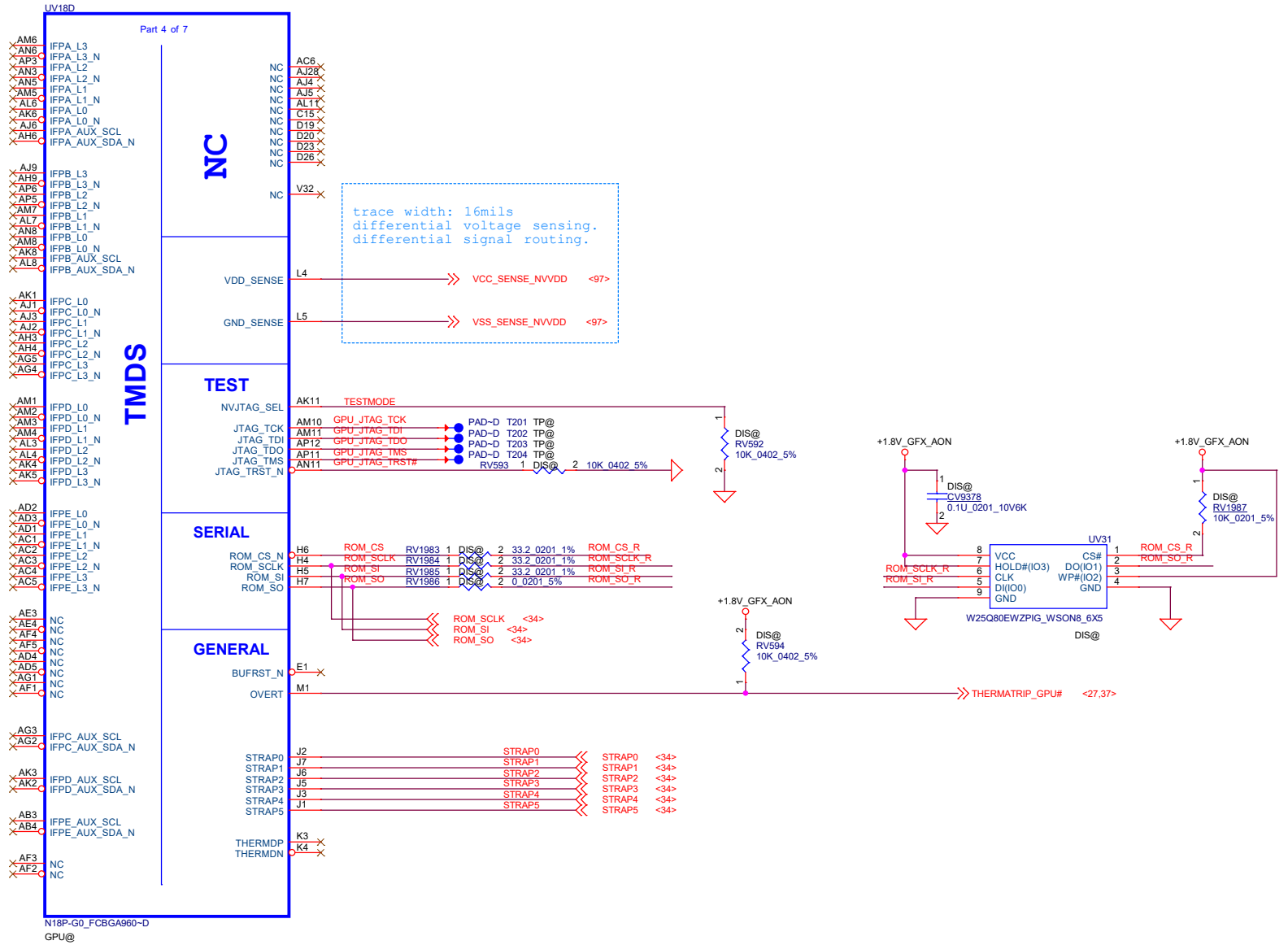
Compal Electronics, Inc.

Title: P027-N18P_PCIE/DAC/GPIO

Size: | Document Number: LA-J191P | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 27 of 100



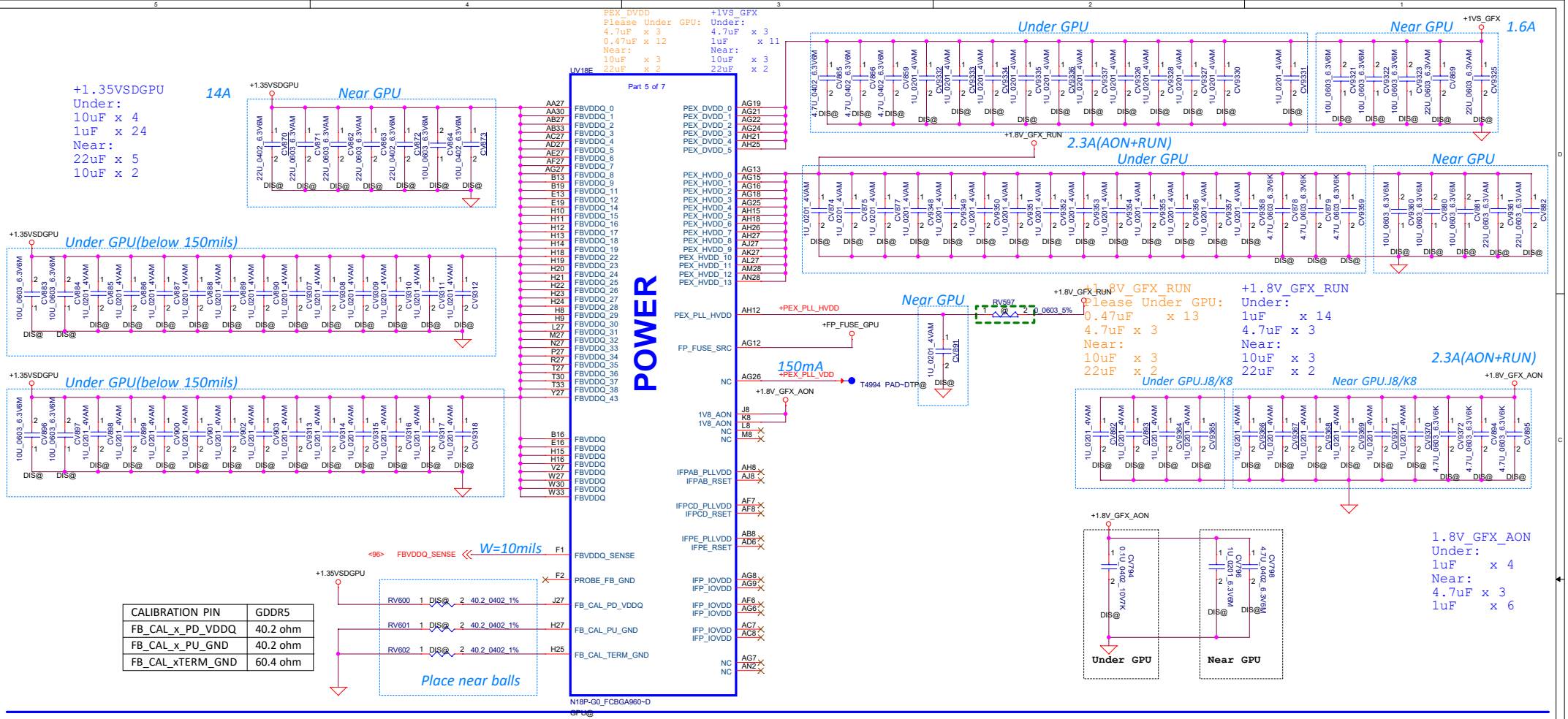
Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P028-N18P_eDP/HDMI/mDP**

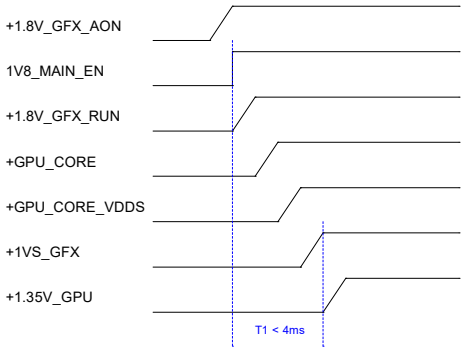
Size	Document Number	Rev
	LA-J191P	0.4(X03)

Date: Friday, November 22, 2019 | Sheet 28 of 100



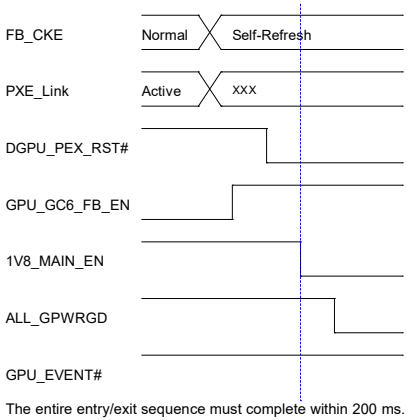
CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2 ohm
FB_CAL_x_PU_GND	40.2 ohm
FB_CAL_xTERM_GND	60.4 ohm

GPU Power Up Sequence



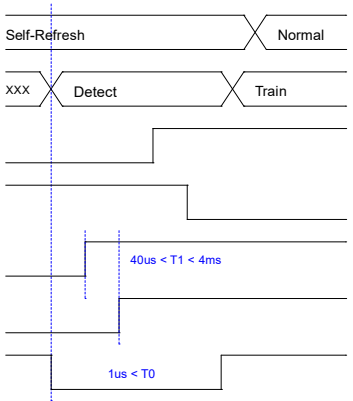
The ramp time for any rail must be more than 40us and less than 2ms.

GPU GC6 Entry Sequence

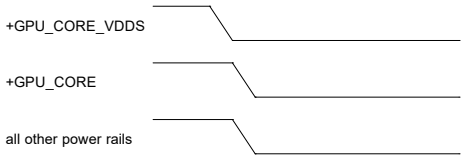


The entire entry/exit sequence must complete within 200 ms.

GPU GC6 Exit Sequence



GPU Power Down Sequence



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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P029-N18P_Power

Size: | Document Number: LA-J191P | Rev: 0.4(0.03)

Date: Friday, November 22, 2019 | Sheet 29 of 100

+1.8V_PLLVDD
Under:
1uF x 4
Near:
4.7uF x 1
22uF x 1
30Ω x 1

Under
<27> +XS_PLLVDD
RV575 0_0402_5%
1U_0201_4VAM CV851 DIS@
+1.8V_PLLVDD

<27> +GPCPLL_AVDD
RV574 0_0402_5%
1U_0201_4VAM CV1091 DIS@
4.7U_0402_6.3VAM CV1050 DIS@
22U_0603_6.3VAM CV850 DIS@
+1.8V_PLLVDD
Under Near GPU

Under
<27> +VID_PLLVDD
RV582 0_0402_5%
1U_0201_4VAM CV854 DIS@
+1.8V_PLLVDD

Under
<27> +SP_PLLVDD
RV576 0_0402_5%
1U_0201_4VAM CV852 DIS@
+1.8V_PLLVDD

Near
+1.8V_PLLVDD
LV23 PBY160808T-300Y-N_2P
+1.8V_GFX_RUN
30 ohm
(ESR=0.03) Bead
CV865 10U_0402_6.3V6M DIS@
CV866 220U_D2_2VY_R9M DIS@

47A +GPU_CORE
UV18G
Part 7 of 7
POWER
VDD_1 AA14
VDD_4 AA21
VDD_6 AB13
VDD_7 AB15
VDD_8 AB17
VDD_9 AB18
VDD_10 AB20
VDD_11 AB22
VDD_12 AC12
VDD_14 AC16
VDD_15 AC19
VDD_17 AC23
VDD_18 M12
VDD_20 M16
VDD_21 M19
VDD_23 M23
VDD_24 N13
VDD_25 N15
VDD_26 N17
VDD_27 N18
VDD_28 N20
VDD_29 N22
VDD_31 P14
VDD_34 P21
VDD_36 R13
VDD_37 R15
VDD_38 R17
VDD_39 R18
VDD_40 R20
VDD_41 R22
VDD_42 T12
VDD_44 T16
VDD_45 T19
VDD_47 T23
VDD_48 U13
VDD_49 U15
VDD_51 U18
VDD_52 U20
VDD_53 U22
VDD_54 V13
VDD_55 V15
VDD_72 AA12
VDD_73 AA16
VDD_74 AA19
VDD_75 AA23
VDD_76 AC14
VDD_77 AC21
VDD_78 M14
VDD_79 M21
VDD_80 P12
VDD_81 P16
VDD_82 P19
VDD_83 P23
VDD_84 T14
VDD_85 T21
VDD_86 U17
VDD_87 V18
VDD_88 W14
VDD_89 W21
VDD_90 AB11
VDD_91 AB24
VDD_92 AD11
VDD_93 AD13
VDD_94 AD15
VDD_95 AD17
VDD_96 AD18
VDD_97 AD20
VDD_98 AD22
VDD_95 AD24
VDD_96 L11
VDD_97 L13
VDD_98 L15
VDD_99 L17
VDD_100 L18
VDD_101 L20
VDD_102 L22
VDD_103 L24
VDD_104 N11
VDD_105 N24
VDD_56 V17
VDD_58 V20
VDD_59 V22
VDD_60 W12
VDD_62 W16
VDD_63 W19
VDD_65 W23
VDD_66 Y13
VDD_67 Y15
VDD_68 Y17
VDD_69 Y18
VDD_70 Y20
VDD_71 Y22
RSVD_VDDS_SENSE U1
RSVD_GNDS_SENSE U2
W=10mils
VDDS_SENSE_VGA T6010 PAD~D@
GNDS_SENSE_VGA T6011 PAD~D@
XVDD_4 U4
XVDD_5 U5
XVDD_6 U6
XVDD_7 U7
XVDD_8 U8
XVDD_9 V1
XVDD_10 V2
XVDD_11 V3
XVDD_12 V4
XVDD_13 V5
XVDD_14 V6
XVDD_15 V7
XVDD_16 V8
XVDD_17 W2
XVDD_18 W3
XVDD_19 W4
XVDD_20 W5
XVDD_21 W7
XVDD_22 W8
XVDD_20 Y1
XVDD_21 Y2
XVDD_22 Y3
XVDD_23 Y4
XVDD_24 Y5
XVDD_25 Y6
XVDD_26 Y7
XVDD_27 Y8
XVDD_28 AA1
XVDD_29 AA2
XVDD_30 AA3
XVDD_31 AA4
XVDD_32 AA5
XVDD_33 AA6
XVDD_34 AA7
XVDD_35 AA8
VDD_106 R11
VDD_107 R24
VDD_108 U11
VDD_109 U24
VDD_110 V11
VDD_111 V24
VDD_112 Y11
VDD_113 Y24
N18P-G0_FCBGA960-D
GPU@

UV18F
Part 6 of 7
GND
GND_0 A2
GND_1 AA17
GND_2 AA18
GND_3 AA20
GND_4 AA22
GND_5 AB12
GND_6 AB14
GND_7 AB16
GND_8 AB19
GND_9 AB2
GND_10 AB21
GND_11 A33
GND_12 AB23
GND_13 AB28
GND_14 AB30
GND_15 AB32
GND_16 AB5
GND_17 AB7
GND_18 AC13
GND_19 AC15
GND_20 AC17
GND_21 AC18
GND_22 AA13
GND_23 AC20
GND_24 AC22
GND_25 AE2
GND_26 AE28
GND_27 AE30
GND_28 AE32
GND_29 AE33
GND_30 AE5
GND_31 AE7
GND_32 AH10
GND_33 AA15
GND_34 AH13
GND_35 AH16
GND_36 AH19
GND_37 AH2
GND_38 AH22
GND_39 AH24
GND_40 AH28
GND_41 AH29
GND_42 AH30
GND_43 AH32
GND_44 AH33
GND_45 AH5
GND_46 AH7
GND_47 AJ7
GND_48 AK10
GND_49 AK7
GND_50 AL12
GND_51 AL14
GND_52 AL15
GND_53 AL17
GND_54 AL18
GND_55 AL2
GND_56 AL20
GND_57 AL21
GND_58 AL23
GND_59 AL24
GND_60 AL26
GND_61 AL28
GND_62 AL30
GND_63 AL32
GND_64 AL33
GND_65 AL5
GND_66 AM13
GND_67 AM16
GND_68 AM19
GND_69 AM22
GND_70 AM25
GND_71 AN1
GND_72 AN10
GND_73 AN13
GND_74 AN16
GND_75 AN19
GND_76 AN22
GND_77 AN25
GND_78 AN30
GND_79 AN34
GND_80 AN4
GND_81 AN7
GND_82 AP2
GND_83 AP33
GND_84 B1
GND_85 B10
GND_86 B22
GND_87 B25
GND_88 B28
GND_89 B31
GND_90 B34
GND_91 B4
GND_92 B7
GND_93 C10
GND_94 C13
GND_95 C19
GND_96 C22
GND_97 C25
GND_98 C28
GND_99 C7
GND_214 L21
GND_215 L23
GND_216 M11
GND_217 M24
GND_218 P11
GND_219 T11
GND_220 T24
GND_221 W11
GND_222 W24
GND_223 P24
GND_100 D2
GND_101 D31
GND_102 D33
GND_103 E10
GND_104 E22
GND_105 E26
GND_106 E5
GND_107 E7
GND_108 F28
GND_109 F7
GND_110 G10
GND_111 G13
GND_112 G16
GND_113 G19
GND_114 G2
GND_115 G22
GND_116 G25
GND_117 G28
GND_118 G3
GND_119 G30
GND_120 G32
GND_121 G33
GND_122 G5
GND_123 G7
GND_124 K2
GND_125 K28
GND_126 K30
GND_127 K32
GND_128 K33
GND_129 K5
GND_130 K7
GND_131 M13
GND_132 M15
GND_133 M17
GND_134 M18
GND_135 M20
GND_136 M22
GND_137 N12
GND_138 N14
GND_139 N16
GND_140 N19
GND_141 N2
GND_142 N21
GND_143 N23
GND_144 N26
GND_145 N30
GND_146 N32
GND_147 N33
GND_148 N5
GND_149 N7
GND_150 P13
GND_151 P15
GND_152 P17
GND_153 P18
GND_154 P20
GND_155 P22
GND_156 R12
GND_157 R14
GND_158 R16
GND_159 R19
GND_160 R21
GND_161 R23
GND_162 T13
GND_163 T15
GND_164 T17
GND_165 T18
GND_166 T2
GND_167 T20
GND_168 T22
GND_169 AG11
GND_170 T28
GND_171 T32
GND_172 T5
GND_173 T7
GND_174 U12
GND_175 U14
GND_176 U16
GND_177 U19
GND_178 U21
GND_179 U23
GND_180 V12
GND_181 V14
GND_182 V16
GND_183 V19
GND_184 V21
GND_185 Y23
GND_186 W13
GND_187 W15
GND_188 W17
GND_189 W18
GND_190 W20
GND_191 W22
GND_192 W28
GND_193 Y12
GND_194 Y14
GND_195 Y16
GND_196 Y19
GND_197 Y21
GND_198 Y23
GND_200 AA11
GND_201 AA24
GND_202 AC11
GND_203 AC24
GND_204 AD12
GND_205 AD14
GND_206 AD16
GND_207 AD19
GND_208 AD21
GND_209 AD23
GND_210 L12
GND_211 L14
GND_212 L16
GND_213 L19
NC AH11
GND_OPT C16
GND_OPT W32
N18P-G0_FCBGA960-D
GPU@
@ RV1973 0_0402_5%

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Issued Date	2019/11/30	Deciphered Date	2027/06/21

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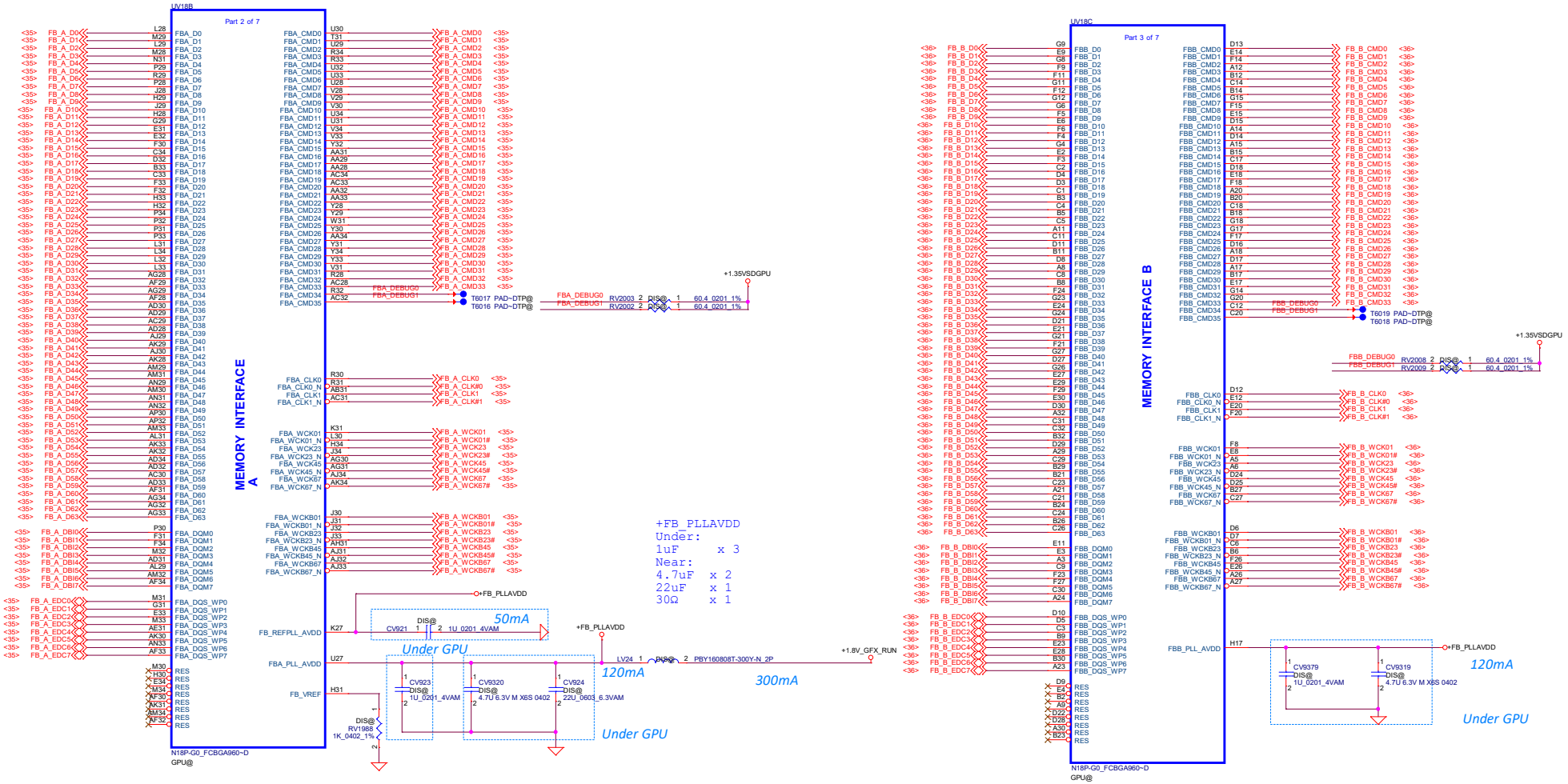
Title: P030-N18P VGA CORE/GND
Size: Document Number: LA-J191P
Rev: 0.4(X03)
Date: Friday, November 22, 2019 Sheet 30 of 100



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Compal Electronics, Inc.

Title: **P031-N18P_MEM Interface**

Size: | Document Number: **LA-J191P** | Rev: 0.4(203)

Date: Friday, November 22, 2019 | Sheet 31 of 100

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Issued Date	2019/11/30	Deciphered Date	2018/05/08

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Title: *P032-Reserve*

Size | Document Number: *LA-J191P* | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 32 of 100

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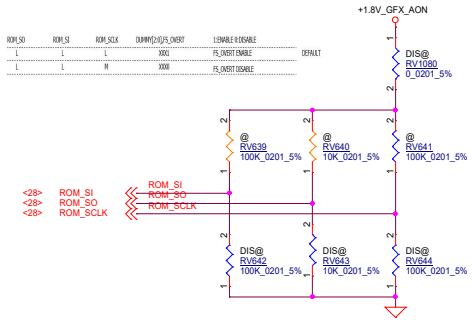
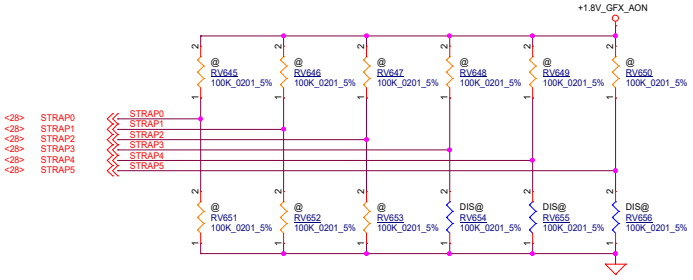
Title	P033-Reserve	
Size A	Document Number LA-J191P	Rev 0.4(X03)
Date: Friday, November 22, 2019	Sheet 33 of 100	





SMB_ALT_ADDR	State
Low	Single GPU
High	Dual GPU

DEVID_SEL	State
Low	Original Device ID
High	Re-brand Device ID

PCIE_CFG	State
Low	Normal signal swing
High	Reduce the signal amplitude

VGA_DEVICE	State
Low	3D Device
High	VGA Device

Table 5.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	SAMSUNG
L	L	H	1 (0x0001)	MICRON
L	H	L	2 (0x0002)	HYNIX

Table 4. N19P-Q3/Q1 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Notes:
1. For N19P-Q3/Q1, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCLK: TBD

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

Berlinetta MLK			
Straps	(N17P-Q1)		(N17P-G0)
Net NAME	state	State	defind
ROM_SCLK	PD 5K	"M"	SOR_EXPOSED(LSB)
ROM_SI	Base on memory RVL.	"H"	SOR_EXPOSED
ROM_SO	PD 5K	"H"	SOR_EXPOSED(MSB)
STRAP0	PU 49.9K		RAMCFG(LSB)
STRAP1	Do not stuff		RAMCFG
STRAP2	Do not stuff		RAMCFG(MSB)
STRAP3	Do not stuff	"L"	SMB_ALT_ADDR(0), DEVIE_SEL(0)
STRAP4	Do not stuff	"L"	PCIE_CFG(0), VGA_DEVICE(0)
STRAP5	Unused	"L"	

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Title	P034-N18P_MISC		
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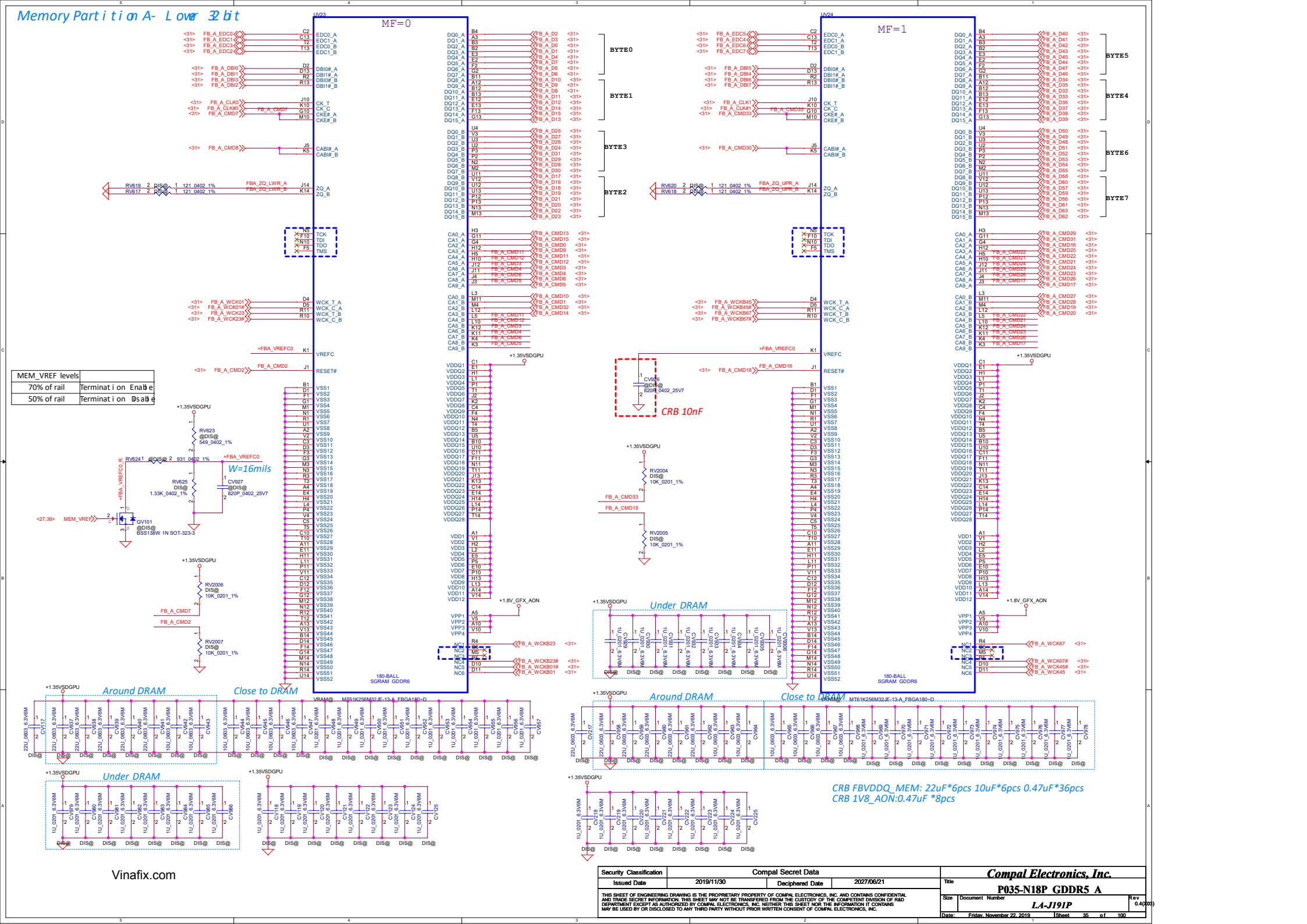
Memory Partition A- Lower 32bit



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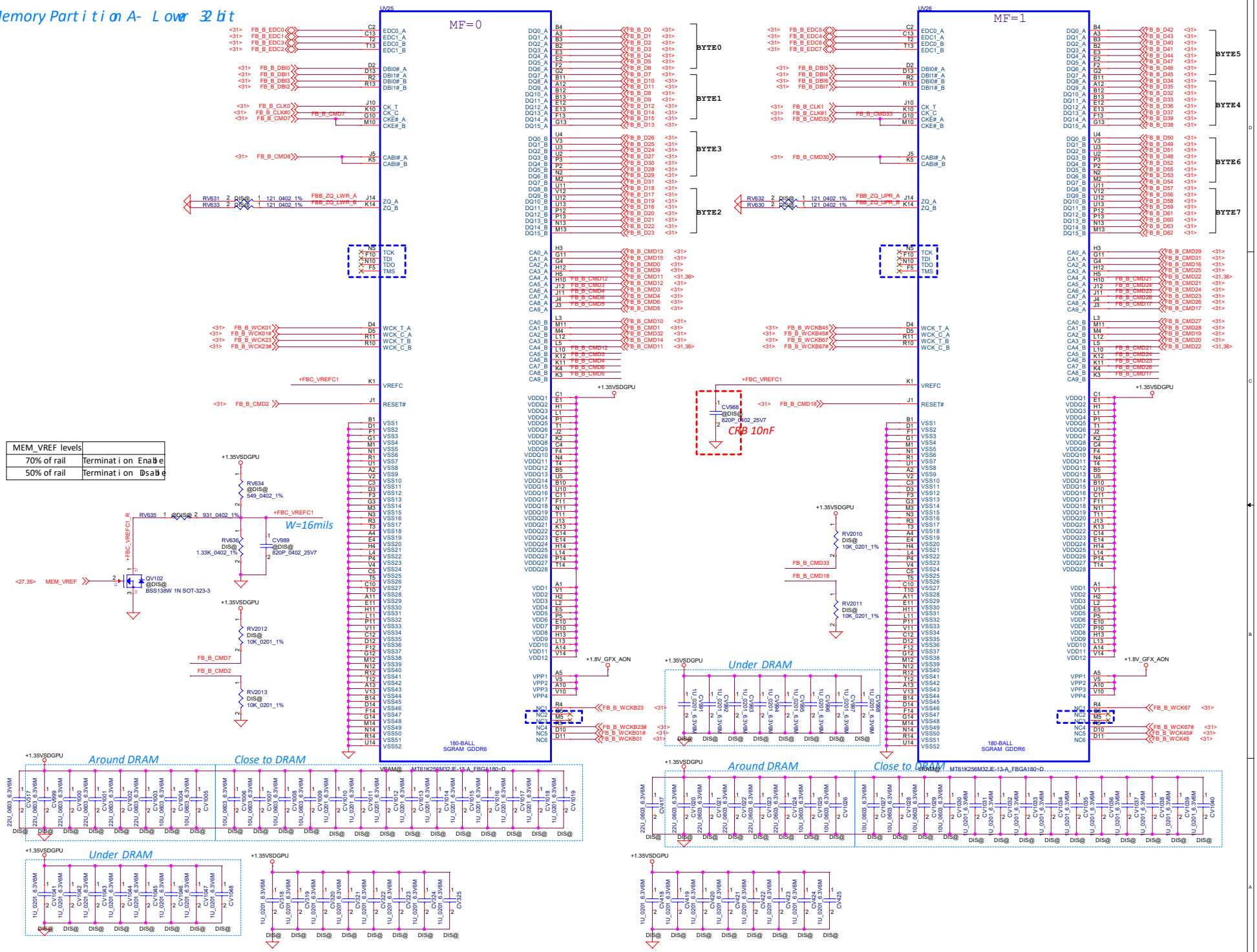
Compal Electronics, Inc.

Title: P035-N18P_GDDR5_A

Size: | Document Number: LA-J191P | Rev: 0.4(2005)

Date: Friday, November 22, 2019 | Sheet 35 of 100

Memory Partition A- Lower 32 bit



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	P036-N18P_GDDR5_B
Size	Document Number: LA-J191P
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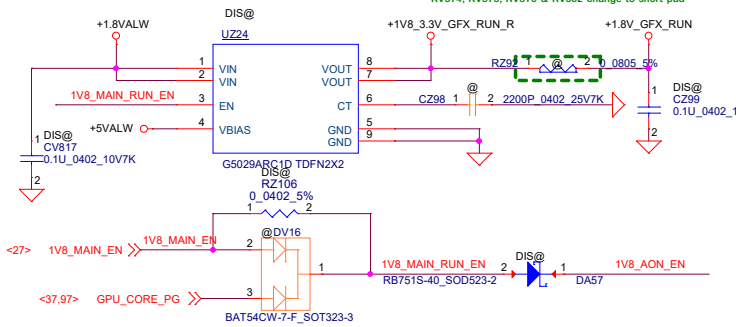
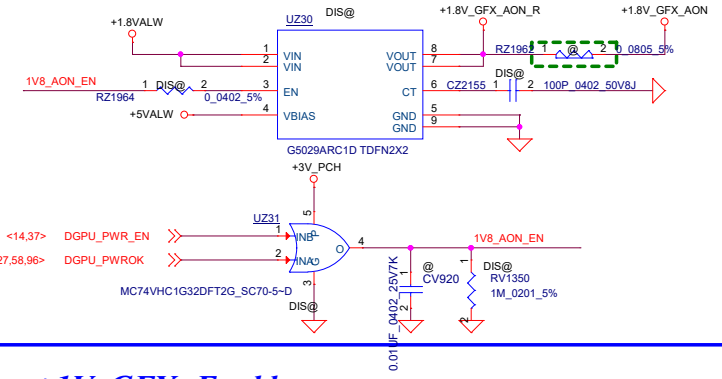
+1.8V_3.3V_GFX_RUN

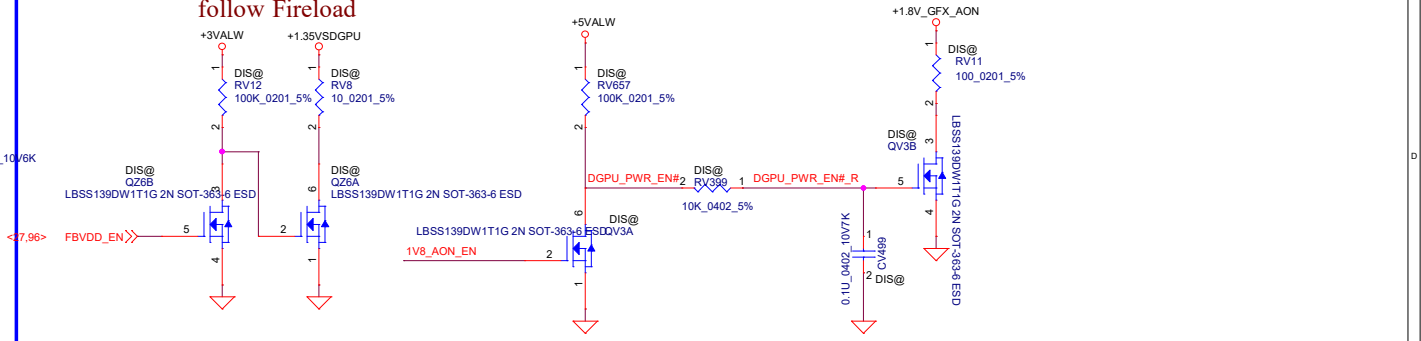


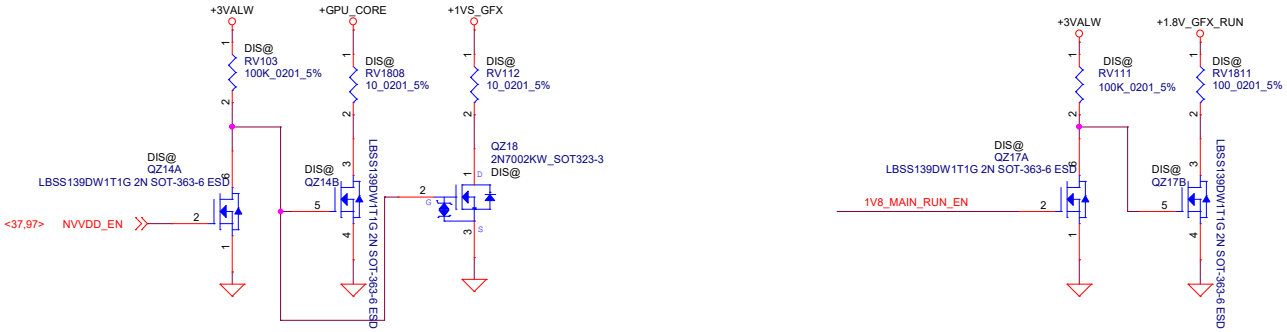
+1.8VALW to +1.8V_3.3V_GFX_AON



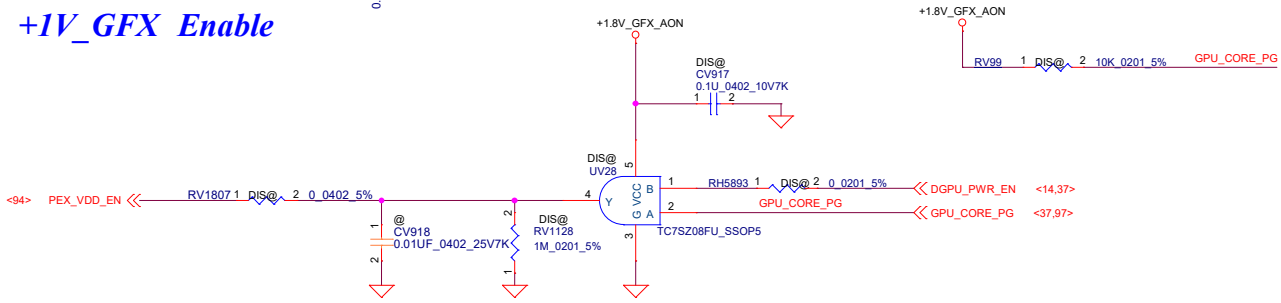
Discharge

follow Fireload

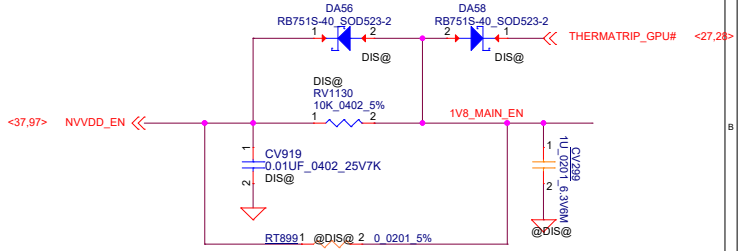




+1V_GFX Enable

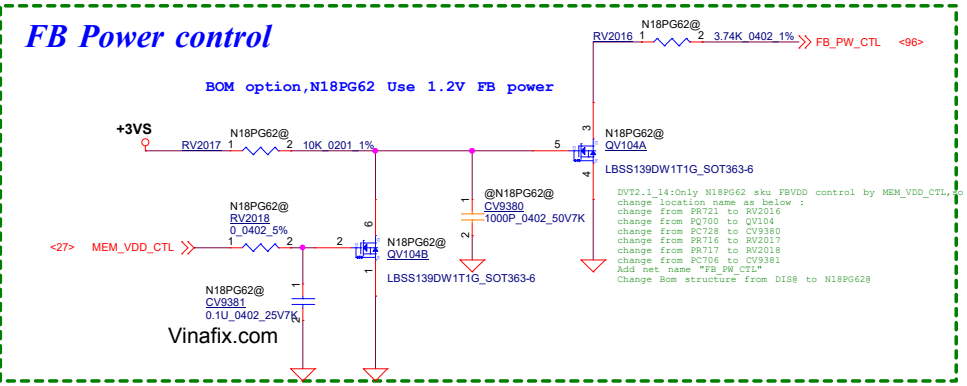


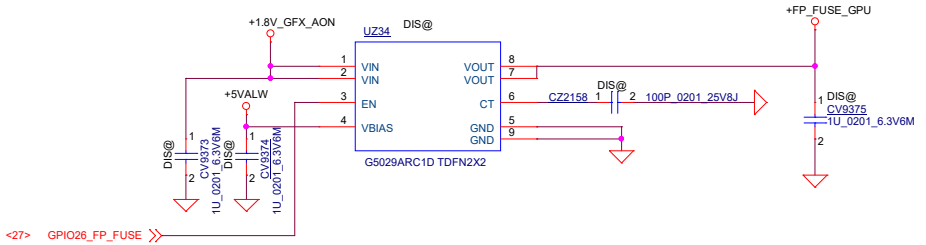
NVVDD Enable



FB Power control

BOM option,N18PG62 Use 1.2V FB power





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Compal Electronics, Inc.

Title: **P037-DC/DC-VGA**

Size	Document Number	Rev
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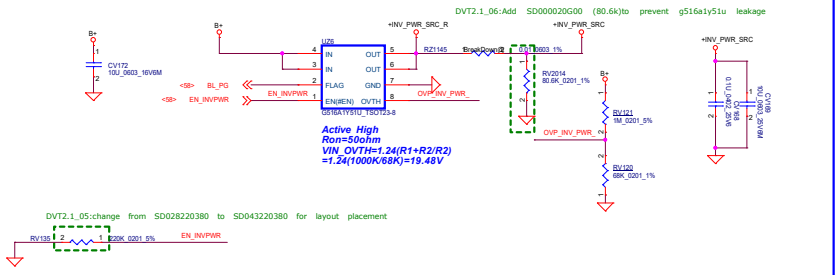
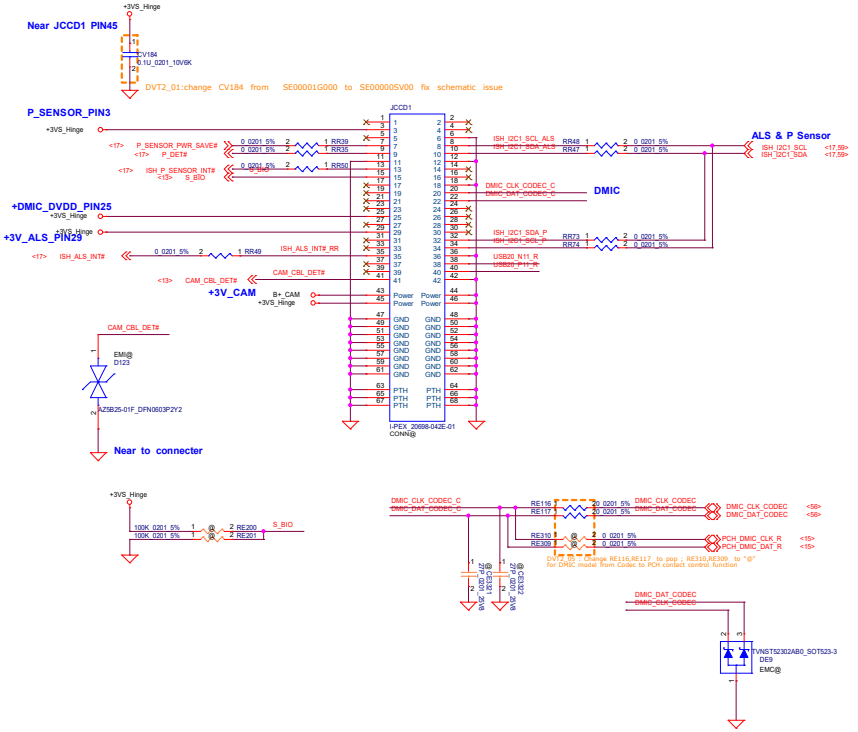
LCD backlight PWR CTRL



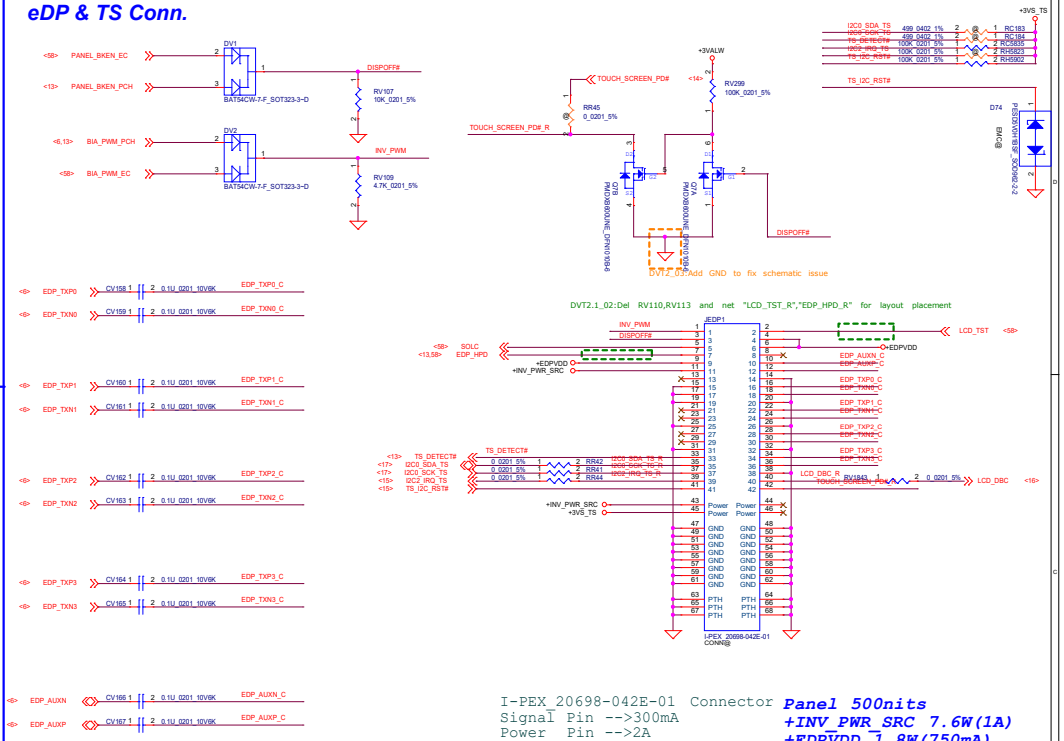
ALS+ IR CCD+ DMIC

Chicony: IR LED MAX:1000mA(12.6V) Estimate-->1400mA(9V)
Power Consumption for Camera (RGB / IR)=200mA(3.3v)

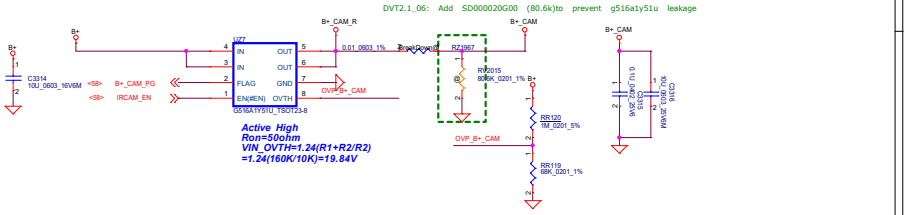
LITEON: IR LED 800mA(B+ Peak power)
Power Consumption for Camera (RGB / IR)=254mA(3.3v)
RGB Cam:143.5mA IR Cam:110.6mA
pin define:20pin



eDP & TS Conn.



IR Digital Camera



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Title	P038-eDP/CCD/TS
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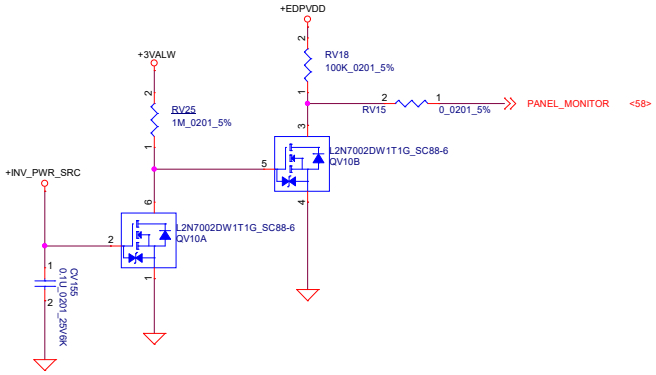
+INV_PWR_SRC & +EDPVDD monitor



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Compal Electronics, Inc.

Title: **P039-DP to HDMI Converter PS175**

Size	Document Number	Rev
Custom	LA-J191P	0.4(X03)

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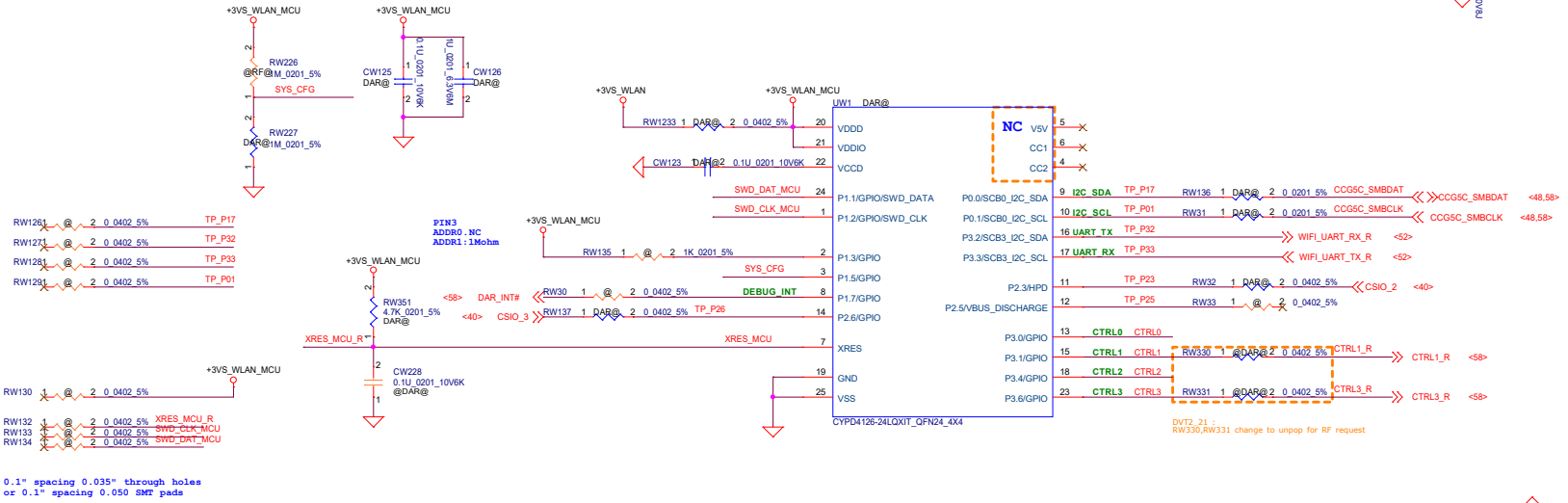
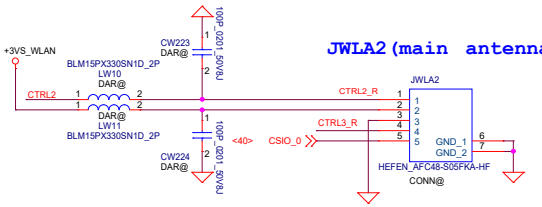
Darwin 2.0

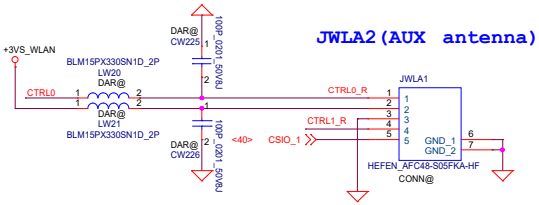
I2C ADDR	I2C Slave Address
NC	0x72 (default)
Pull up 3.3V	0x34



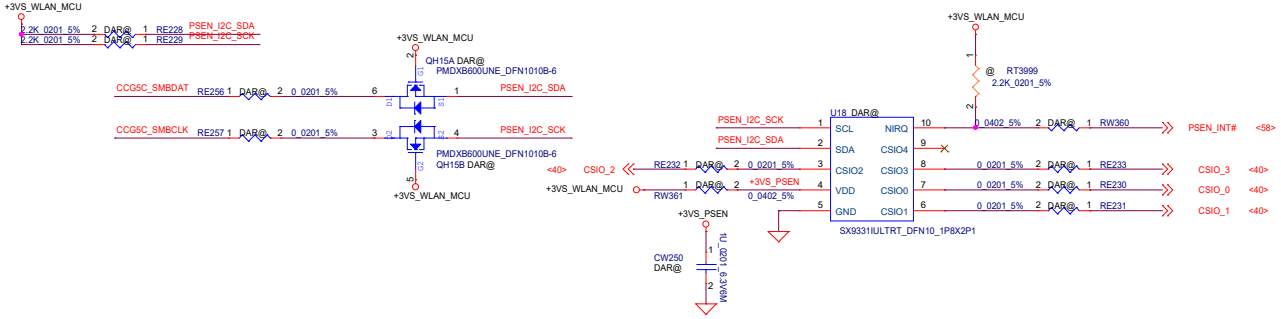
JWLA2 (main antenna)



JWLA2 (AUX antenna)



P-sensor



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Title: **P040-HDMI Connector**

Size	Document Number	Rev
C	LA-J191P	0.4(003)

Date: Friday, November 22, 2019 Sheet 40 of 100

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **P058-EC MEC 5105**

Size	Document Number	Rev
C		

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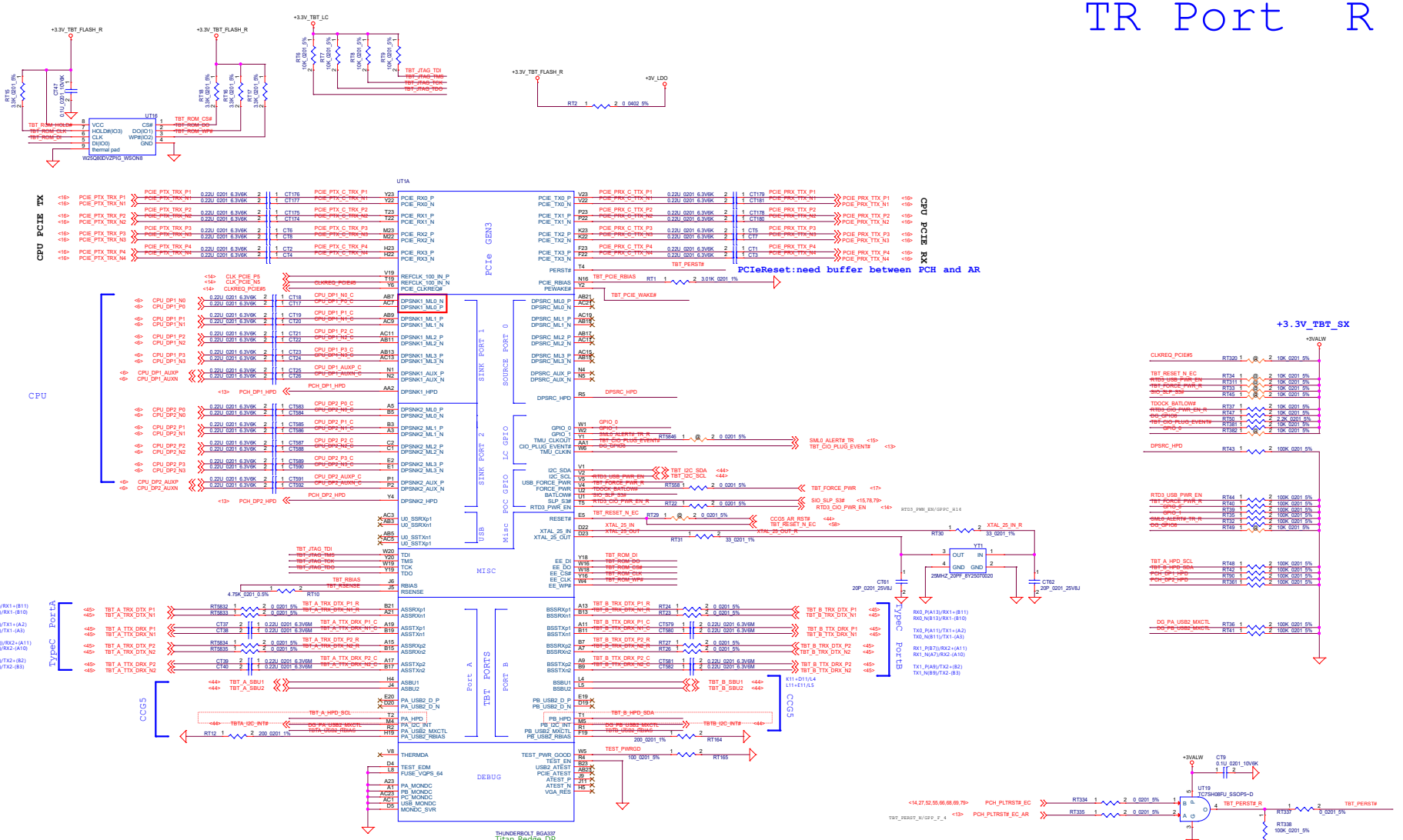
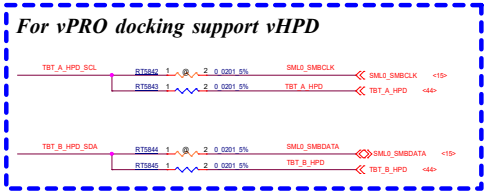
TR Port R



For vPRO docking support vHPD



RTD3 GPIO refer by Intel RVP

GPIO	intel RVP	Fiorano
TBT_PERST_N	GPP_F_4_SATAXPCIE	PCH_PLTRST#_EC_AR/GPP_F4
TBT_Wake_N	GPP_K_18_NMIB	TBT_WAKE#/GPP_K18
RTD3_PWN_EN	GPP_H_16_SML4_CLK	RTD3_CIO_PWR_EN/GPP_H16

FUNCTION TABLE

IN	NC TO COM COM TO NC	NO TO COM COM TO NO
L	ON	OFF
H	OFF	ON

IN	NC	NO
L	COM	X
H	X	COM

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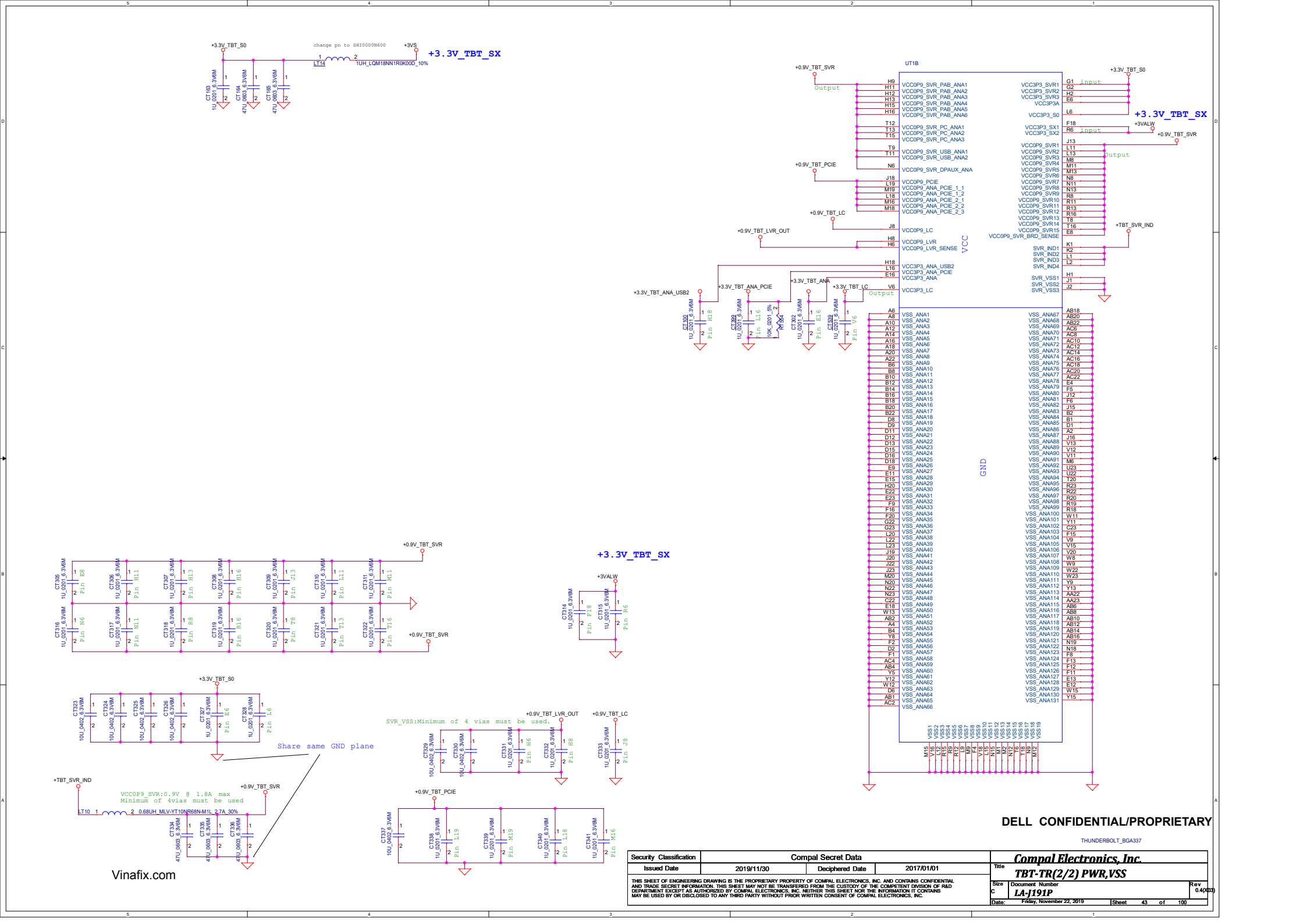
			Size: Custom; Document Number: LA-J191P; Rev: 0.4(A03)
			Date: Friday, November 22, 2019; Sheet 42 of 100


+3.3V_TBT_S0
change pn to SHI0000N600
+3VS
+3.3V_TBT_SX
LT14
1UH_LQM18NN1R0K00D_10%
CT163 1U_0201_6.3V6M
CT164 47U_0603_6.3V6M
CT165 47U_0603_6.3V6M
UT1B
+0.9V_TBT_SVR
Output
VCC0P9_SVR_PAB_ANA1
VCC0P9_SVR_PAB_ANA2
VCC0P9_SVR_PAB_ANA3
VCC0P9_SVR_PAB_ANA4
VCC0P9_SVR_PAB_ANA5
VCC0P9_SVR_PAB_ANA6
VCC0P9_SVR_PC_ANA1
VCC0P9_SVR_PC_ANA2
VCC0P9_SVR_PC_ANA3
VCC0P9_SVR_USB_ANA1
VCC0P9_SVR_USB_ANA2
VCC0P9_SVR_DPAUX_ANA
+0.9V_TBT_PCIE
VCC0P9_PCIE
VCC0P9_ANA_PCIE_1_1
VCC0P9_ANA_PCIE_1_2
VCC0P9_ANA_PCIE_2_1
VCC0P9_ANA_PCIE_2_2
VCC0P9_ANA_PCIE_2_3
+0.9V_TBT_LC
VCC0P9_LC
+0.9V_TBT_LVR_OUT
VCC0P9_LVR
VCC0P9_LVR_SENSE
VCC
VCC3P3_ANA_USB2
VCC3P3_ANA_PCIE
VCC3P3_ANA
VCC3P3_LC
+3.3V_TBT_S0
input
VCC3P3_SVR1
VCC3P3_SVR2
VCC3P3_SVR3
VCC3P3A
VCC3P3_S0
+3.3V_TBT_SX
+3VALW
VCC3P3_SX1
VCC3P3_SX2
+0.9V_TBT_SVR
VCC0P9_SVR1
VCC0P9_SVR2
VCC0P9_SVR3
VCC0P9_SVR4
VCC0P9_SVR5
VCC0P9_SVR6
VCC0P9_SVR7
VCC0P9_SVR8
VCC0P9_SVR9
VCC0P9_SVR10
VCC0P9_SVR11
VCC0P9_SVR12
VCC0P9_SVR13
VCC0P9_SVR14
VCC0P9_SVR15
VCC0P9_SVR_BRD_SENSE
+TBT_SVR_IND
SVR_IND1
SVR_IND2
SVR_IND3
SVR_IND4
SVR_VSS1
SVR_VSS2
SVR_VSS3
+3.3V_TBT_ANA_USB2
+3.3V_TBT_ANA_PCIE
+3.3V_TBT_ANA
+3.3V_TBT_LC
CT106 1U_0201_6.3V6M
CT309 1U_0201_6.3V6M
10K_0201_5%
CT302 1U_0201_6.3V6M
CT539 1U_0201_6.3V6M
GND
VSS_ANA1
VSS_ANA2
VSS_ANA3
VSS_ANA4
VSS_ANA5
VSS_ANA6
VSS_ANA7
VSS_ANA8
VSS_ANA9
VSS_ANA10
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VSS_ANA88
VSS_ANA89
VSS_ANA90
VSS_ANA91
VSS_ANA92
VSS_ANA93
VSS_ANA94
VSS_ANA95
VSS_ANA96
VSS_ANA97
VSS_ANA98
VSS_ANA99
VSS_ANA100
VSS_ANA101
VSS_ANA102
VSS_ANA103
VSS_ANA104
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VSS_ANA123
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VSS_ANA128
VSS_ANA129
VSS_ANA130
VSS_ANA131
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
VSS14
VSS15
VSS16
VSS17
VSS18
VSS19
+0.9V_TBT_SVR
CT305 1U_0201_6.3V6M
CT306 1U_0201_6.3V6M
CT307 1U_0201_6.3V6M
CT308 1U_0201_6.3V6M
CT309 1U_0201_6.3V6M
CT310 1U_0201_6.3V6M
CT311 1U_0201_6.3V6M
CT316 1U_0201_6.3V6M
CT317 1U_0201_6.3V6M
CT318 1U_0201_6.3V6M
CT319 1U_0201_6.3V6M
CT320 1U_0201_6.3V6M
CT321 1U_0201_6.3V6M
CT322 1U_0201_6.3V6M
+0.9V_TBT_SVR
+3.3V_TBT_SX
+3VALW
CT314 1U_0201_6.3V6M
CT315 1U_0201_6.3V6M
+3.3V_TBT_S0
CT323 10U_0402_6.3V6M
CT324 10U_0402_6.3V6M
CT325 10U_0402_6.3V6M
CT326 10U_0402_6.3V6M
CT327 1U_0201_6.3V6M
CT328 1U_0201_6.3V6M
Share same GND plane
SVR_VSS:Minimum of 4 vias must be used.
+0.9V_TBT_LVR_OUT
+0.9V_TBT_LC
CT329 10U_0402_6.3V6M
CT330 10U_0402_6.3V6M
CT331 1U_0201_6.3V6M
CT332 1U_0201_6.3V6M
CT333 1U_0201_6.3V6M
+TBT_SVR_IND
+0.9V_TBT_SVR
VCC0P9_SVR:0.9V @ 1.8A max
Minimum of 4vias must be used
LT10 0.68UH_MLV-YT10NR68N-M1L 2.7A_30%
CT334 47U_0603_6.3V6M
CT335 47U_0603_6.3V6M
CT336 47U_0603_6.3V6M
+0.9V_TBT_PCIE
CT337 10U_0402_6.3V6M
CT338 1U_0201_6.3V6M
CT339 1U_0201_6.3V6M
CT340 1U_0201_6.3V6M
CT341 1U_0201_6.3V6M
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THUNDERBOLT_BGA337
Security Classification
Compal Secret Data
Issued Date
2019/11/30
Deciphered Date
2017/01/01
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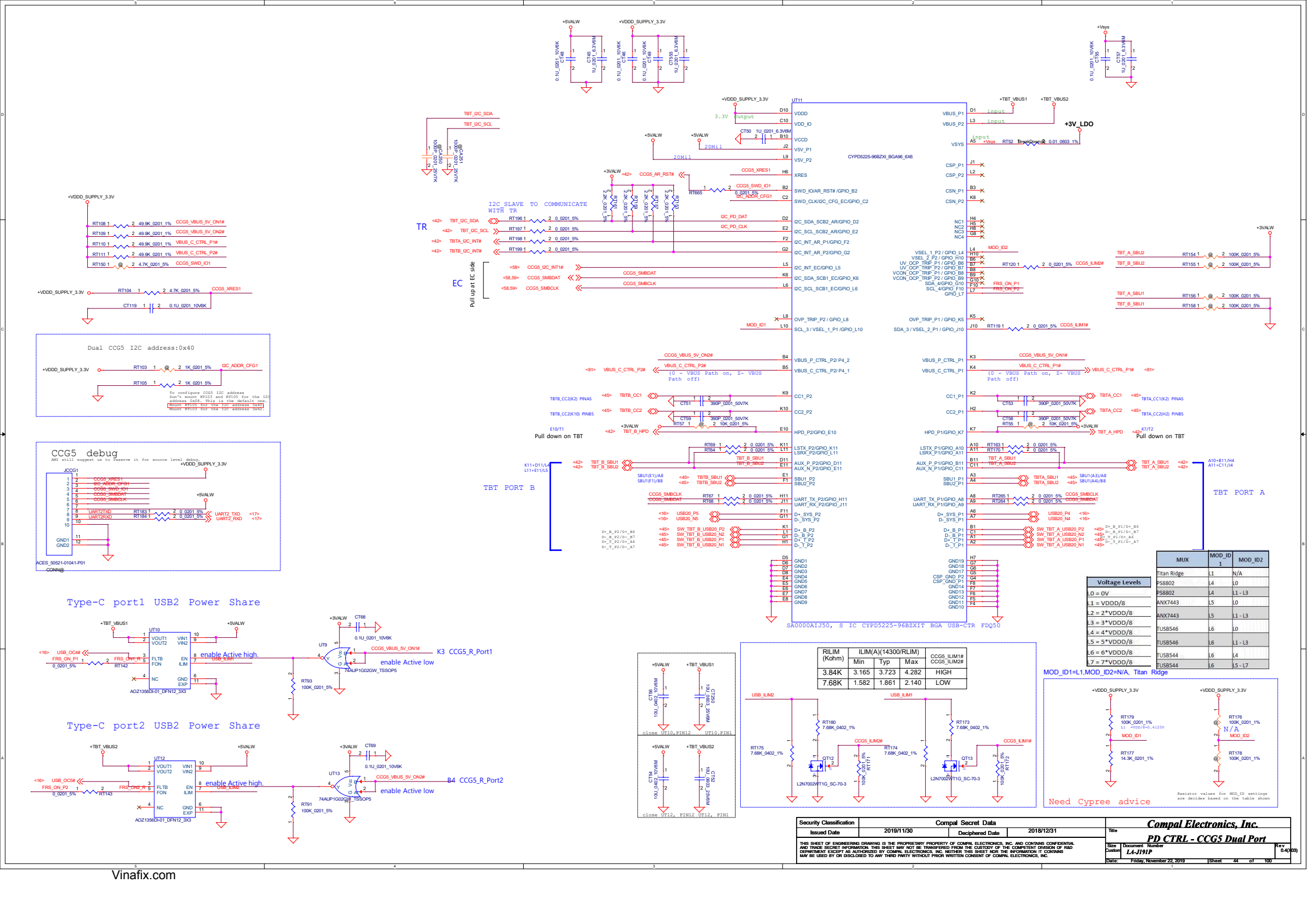
Compal Electronics, Inc.
Title
TBT-TR(2/2) PWR,VSS
Size
C
Document Number
LA-J191P
Rev
0.4(003)
Date:
Friday, November 22, 2019
Sheet
43
of
100



MUX	MOD_ID 1	MOD_ID2
Titan Ridge	L1	N/A
PS8802	L4	L0
PS8802	L4	L1 - L3
ANX7443	L5	L0
ANX7443	L5	L1 - L3
TUSB546	L6	L0
TUSB546	L6	L1 - L3
TUSB544	L6	L4
TUSB544	L6	L5 - L7

RILIM (Kohm)	ILIM(A)(14300/RILM)			CCG5_ILIM1# CCG5_ILIM2#
	Min	Typ	Max	
3.84K	3.165	3.723	4.282	HIGH
7.68K	1.582	1.861	2.140	LOW

Voltage Levels
L0 = 0V
L1 = VDDD/8
L2 = 2*VDDD/8
L3 = 3*VDDD/8
L4 = 4*VDDD/8
L5 = 5*VDDD/8
L6 = 6*VDDD/8
L7 = 7*VDDD/8

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/12/31

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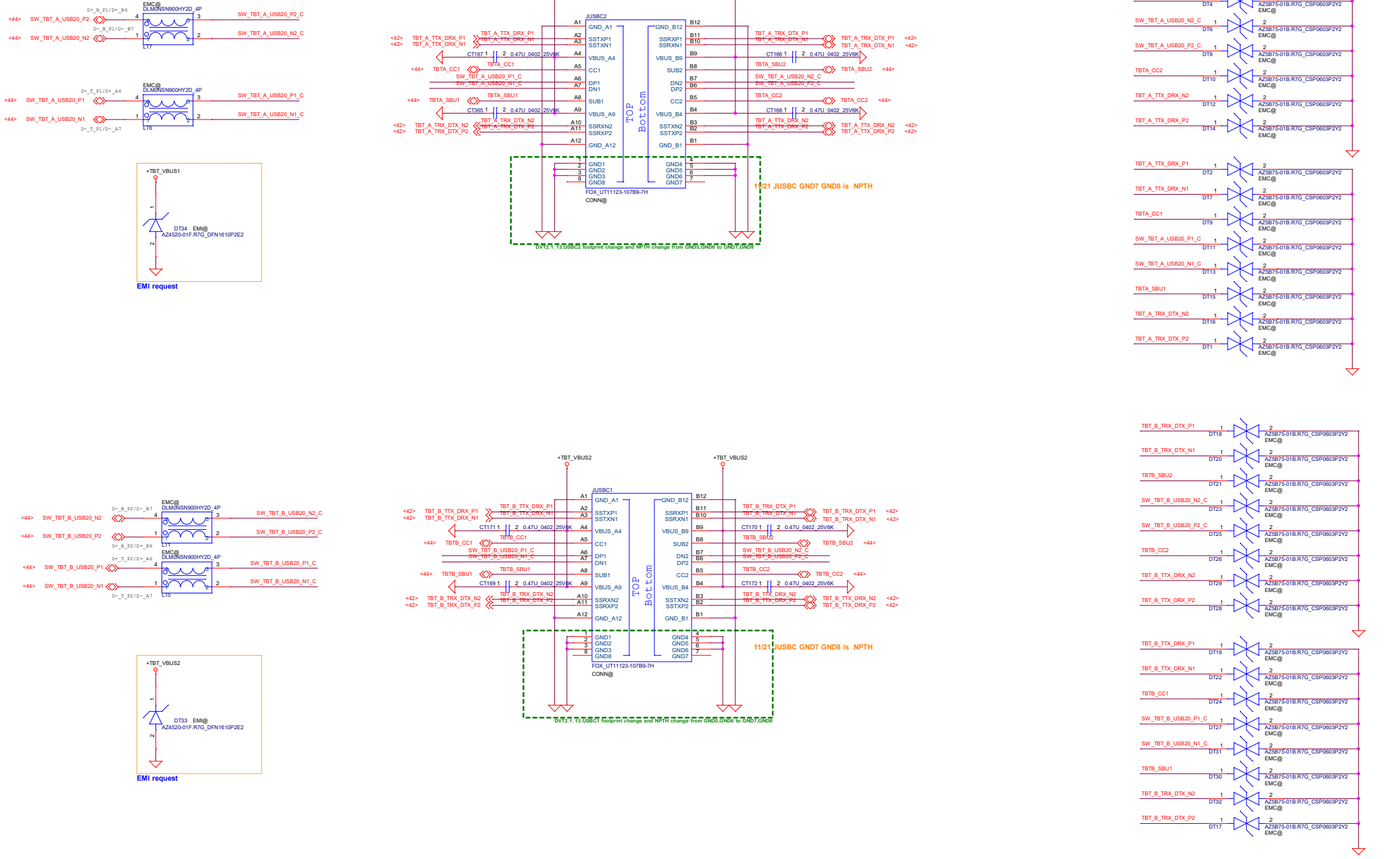
Size	Document Number		Rev
Custom	L4-J191P		0.4(003)
Date:	Friday, November 22, 2019	Sheet 44 of 100	



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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

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Compal Electronics, Inc.

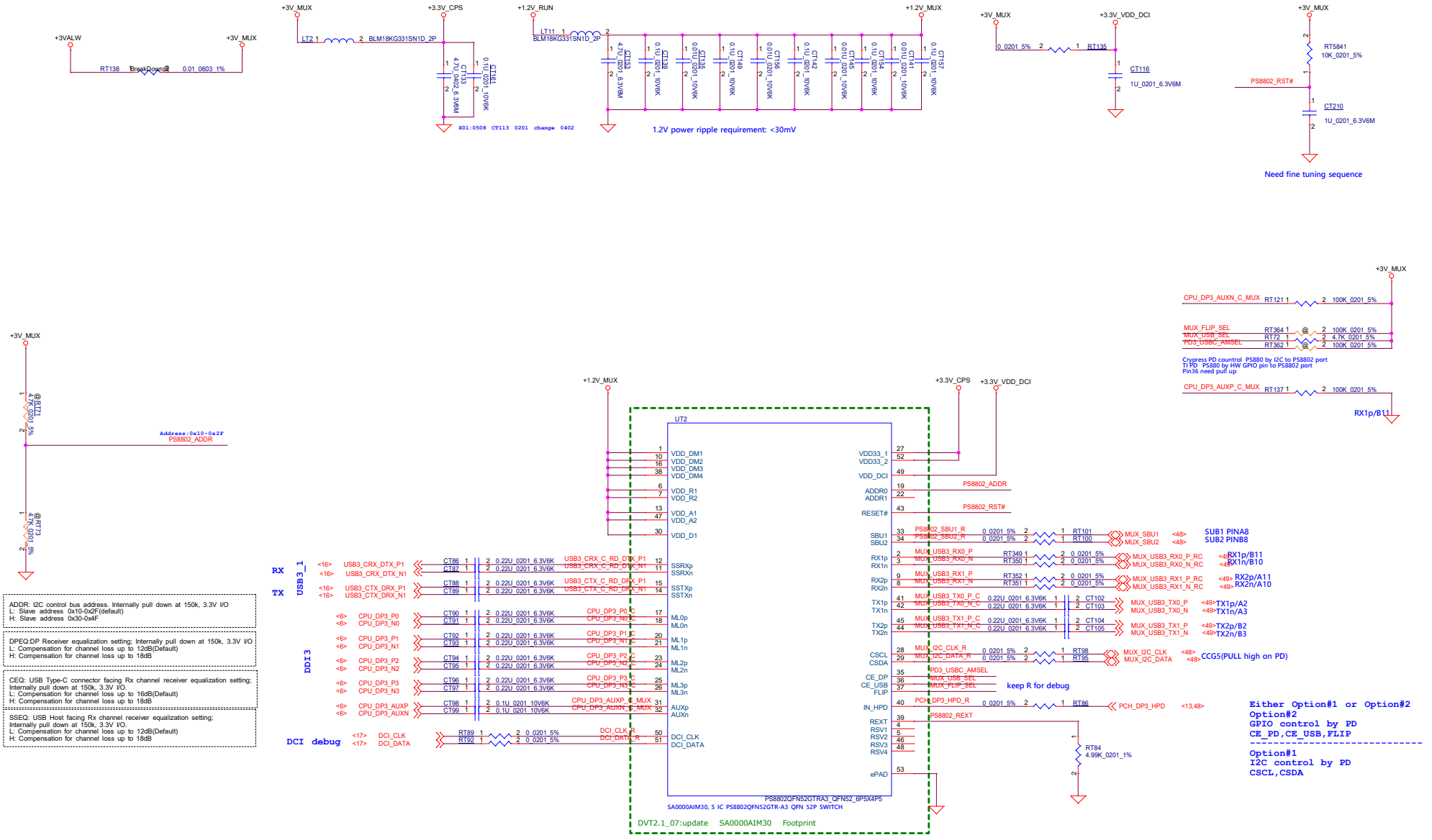
Title: P045-PD USB TYPE-C CONN.

Size	Document Number	Rev
Custom	LA-J191P	0.4(D03)

Date: Friday, November 22, 2019 Sheet 45 of 100

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: TBT-TR(1/2) DP, PCIE			
Size: Custom	Document Number: LA-J191P		Rev: 0.4(03)
Date: Friday, November 22, 2019	Sheet 46 of 100		



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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2017/01/01

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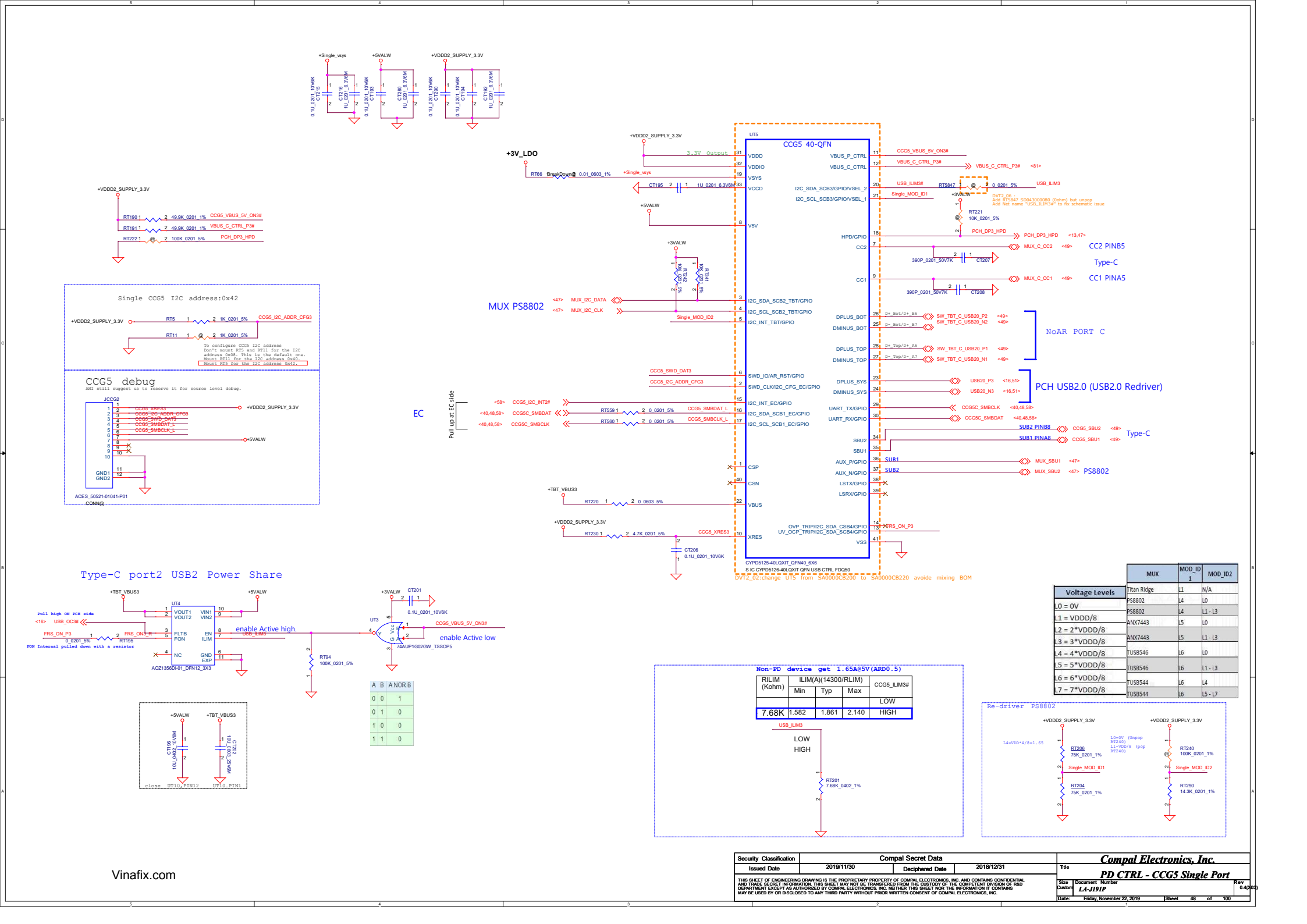
Compal Electronics, Inc.

Title: TBT-TR(2/2) PWR,VSS

Size: Custom | Document Number: LA-J191P | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 47 of 100



RILIM (Kohm)	ILIM(A)(14300/RLIM) Min	Typ	Max	CCG5_ILIM3#
				LOW
7.68K	1.582	1.861	2.140	HIGH

MUX	MOD_ID1	MOD_ID2
Titan Ridge	L1	N/A
PS8802	L4	L0
PS8802	L4	L1 - L3
ANX7443	L5	L0
ANX7443	L5	L1 - L3
TUSB546	L6	L0
TUSB546	L6	L1 - L3
TUSB544	L6	L4
TUSB544	L6	L5 - L7

Voltage Levels
L0 = 0V
L1 = VDDD/8
L2 = 2*VDDD/8
L3 = 3*VDDD/8
L4 = 4*VDDD/8
L5 = 5*VDDD/8
L6 = 6*VDDD/8
L7 = 7*VDDD/8

A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/12/31

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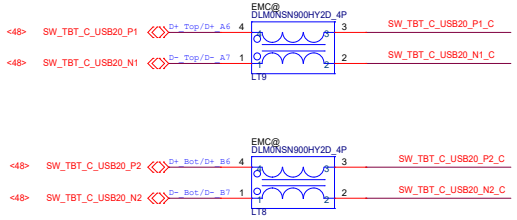
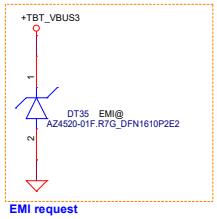
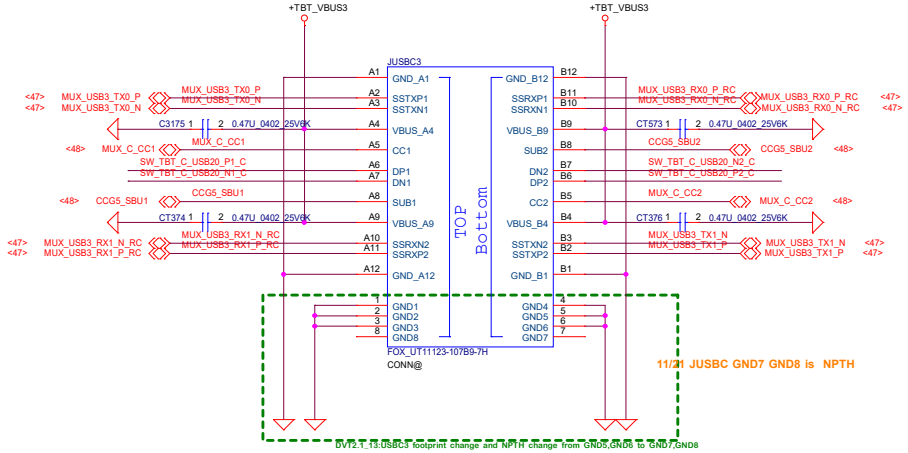
Compal Electronics, Inc.

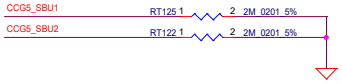
Title: PD CTRL - CCG5 Single Port

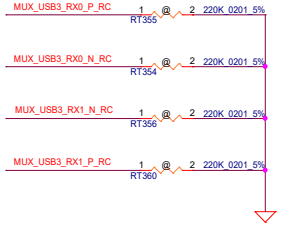
Size	Document Number	Rev
Custom	LA-J191P	0.4(D03)
Date: Friday, November 22, 2019	Sheet 48 of 100	

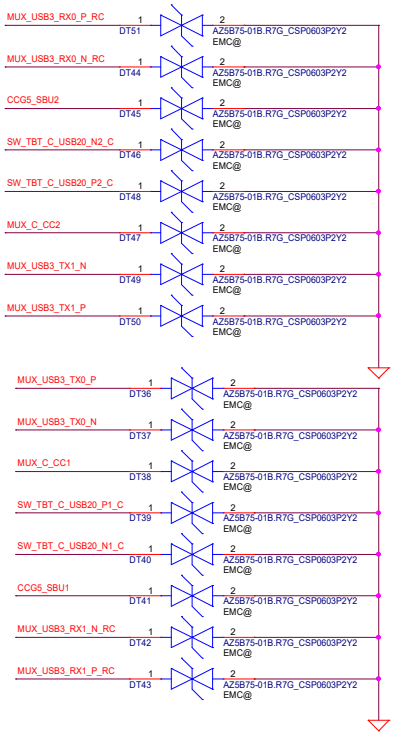




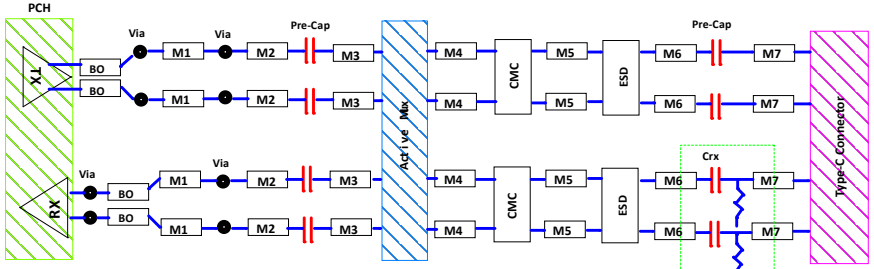








CNL/CFL Type-C External (Back Panel) Topology with Active Mux



Notes

Crx Cap Value: 297nF to 363nF including tolerance

Rb Resistor Value: 220kΩ ± 5%

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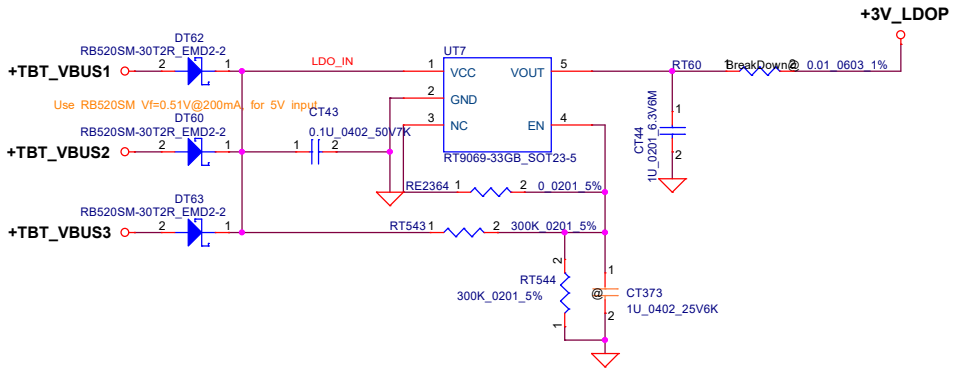
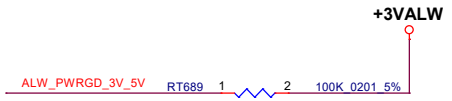
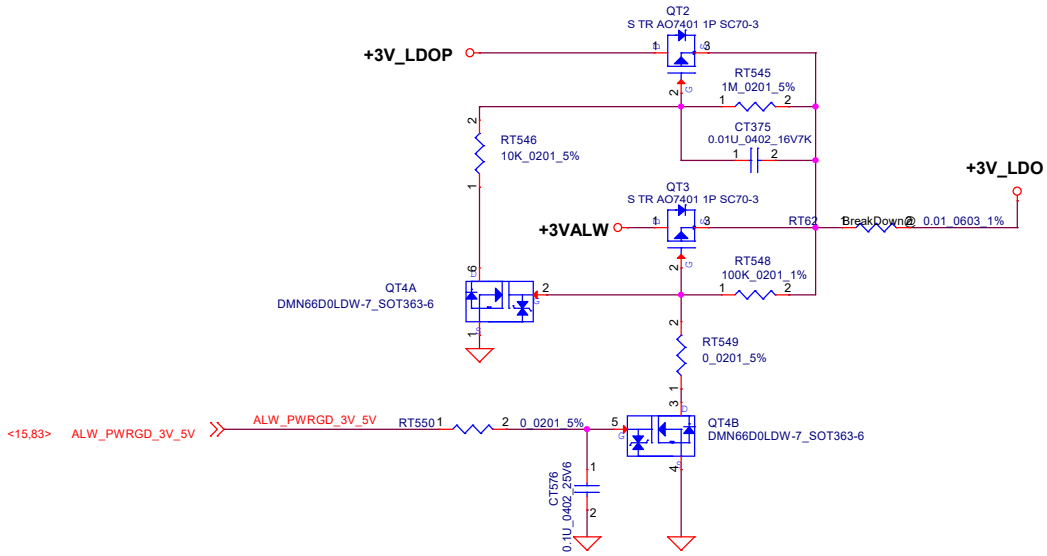
Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

Compal Electronics, Inc.			
Title: P049-Reserve			
Size	Document Number: LA-J191P		Rev: 0.4(X03)
Date: Friday, November 22, 2019	Sheet 49 of 100		

3V LDO







Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

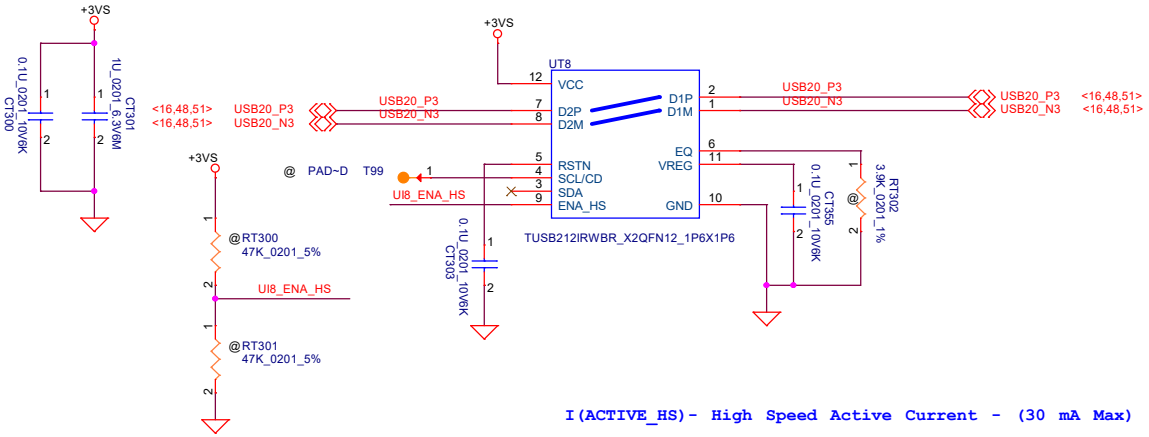
Compal Electronics, Inc.

Title: P050-Reserve

Size | Document Number: LA-J191P | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 50 of 100

USB2.0 Re-driver for TypeC NoTBT port



I(ACTIVE_HS)- High Speed Active Current - (30 mA Max)

Table 1. DC Boost Settings

DC BOOST SETTING VIA PIN STRAP	
DC_BOOST	DC Boost Setting (mV)
V_{IL}	40
V_{IM}	60
V_{IH}	80

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

Compal Electronics, Inc.

Title: P051-Reserve

Size | Document Number: LA-J191P | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 51 of 100

M.2 Slot-A Key-A (WLAN + BT)

Level Shift Circuit (Killer9560 GPIO 1.8V)

CNVi&Darwin2.0 BOM opt i on

CNVi&Darwin2.0 BOM opt i on

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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

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Compal Electronics, Inc.

Title: P052-NGFF-WLAN/BT

Size: Custom | Document Number: LA-J191P | Rev: 0.4(003)

Date: Friday, November 22, 2019 | Sheet 52 of 100

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

Compal Electronics, Inc.		
Title: P053-Reserve		
Size	Document Number: LA-J191P	Rev: 0.4(X03)
Date: Friday, November 22, 2019	Sheet 53 of 100	

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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

Compal Electronics, Inc.

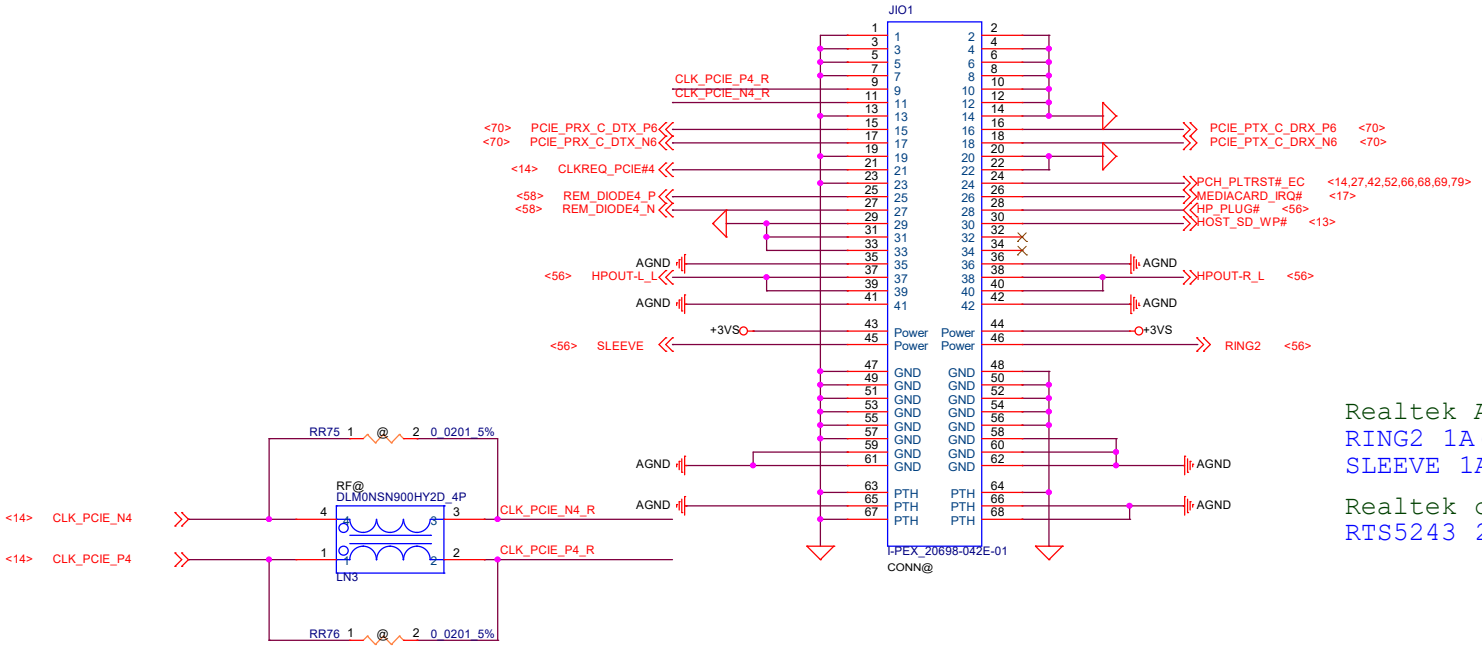
Title: *P054-Reserve*

Size | Document Number: *LA-J191P* | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 54 of 100

Audio Jack + CardReader(RT35243)

I-PEX_20698-042E-01 Connector
Signal Pin -->300mA
Power Pin -->2A



Realtek Audio jack
RING2 1A(40mil)
SLEEVE 1A(40mil)

Realtek codec inner class D(By Clark feedback)
RTS5243 2A+2.375mA

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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

Compal Electronics, Inc.

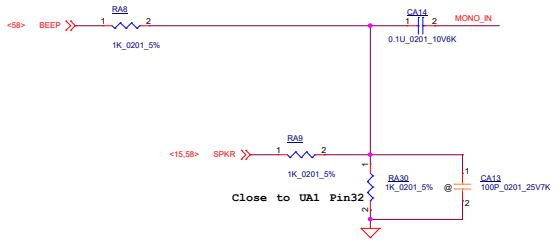
Title: P055-Reserve

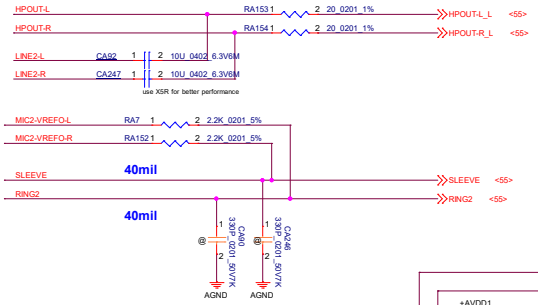
Size: | Document Number: LA-J191P | Rev: 0.4(X03)

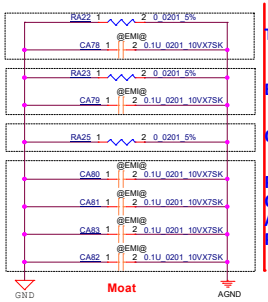
Date: Friday, November 22, 2019 | Sheet 55 of 100

Beep sound

RC filter for PWM square to sine-wave

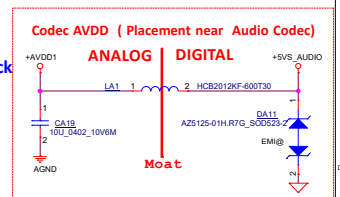






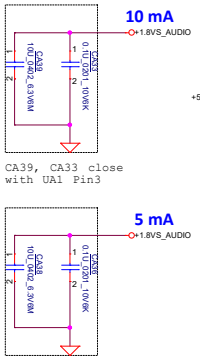
TOP
BOT
Close Audio jack
Close Codec
Place on Codec to Audio Jack Path

Don't short this pad to USB digital ground, and should be far away from any power traces.

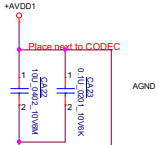


In order to prevent the built-in LDO damaged from over-voltage on +5VD or Standby power line, we suggested using this Voltage suppressing device.

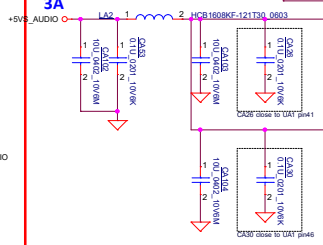
3.3V level change 1.8V

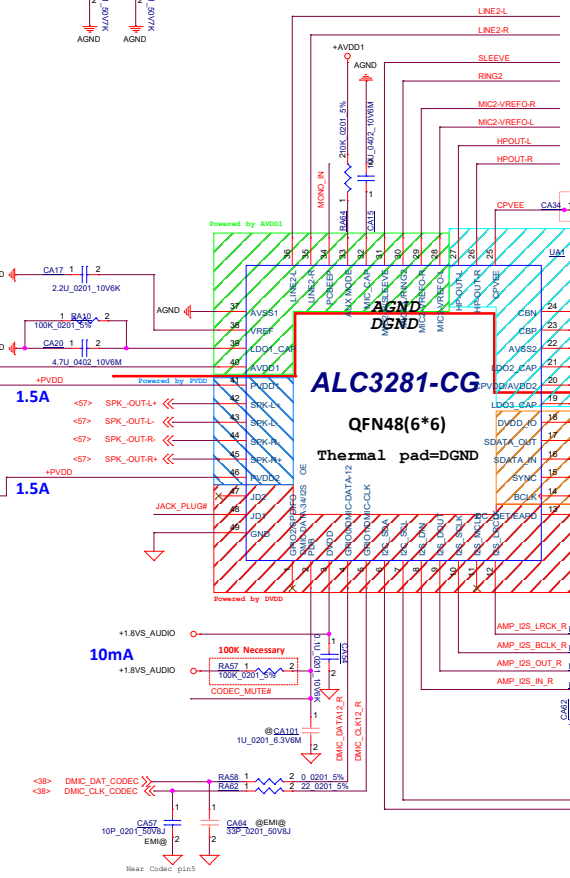


200 mA

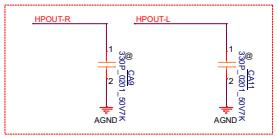


3A

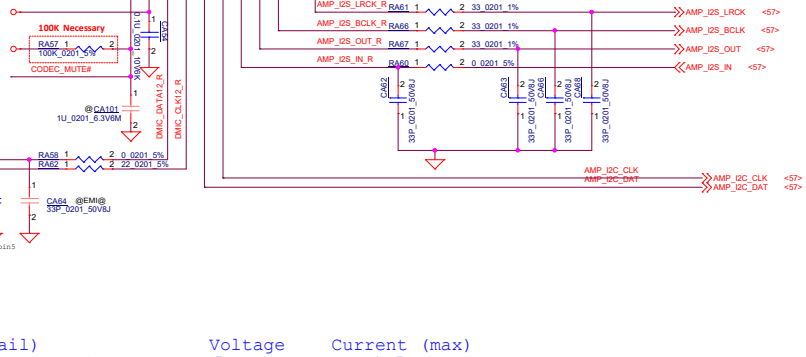


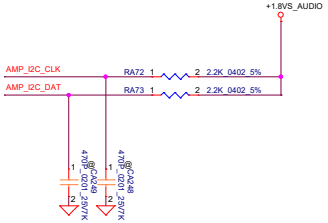


Place near UA1 pin26/27

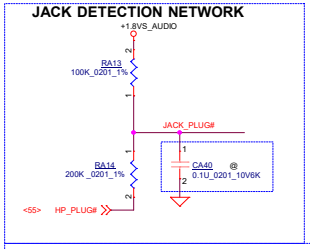


10mA

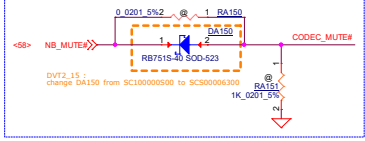




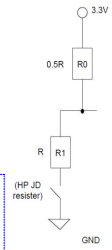
JACK DETECTION NETWORK



Internal pull high to +DVDD



R0 is 100K ohm.



(Power Rail)	Voltage	Current (max)
PVDD1(+5VS_AUDIO)	5V	>1.5A
PVDD2(+5VS_AUDIO)	5V	>1.5A
AVDD1(+5VS_AUDIO)	5V	200mA
AVDD2+CPVDD(+1.8VS_AUDIO)	1.8V	50mA
DVDD(+1.8VS_AUDIO)	1.8V/3.3V	10mA
DVDD-IO(+1.8VS_AUDIO)	1.8V/3.3V	5mA

Realtek codec inner class D 2W/4ohm speaker estimation
(By Clark feedback)

Vinafix.com

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2013/10/28

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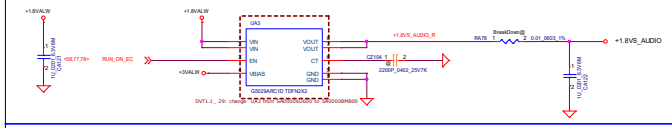
Compal Electronics, Inc.

Title: P056 - Audio ALC3281

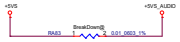
Size: | Document Number: LA-J191P | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 56 of 100

+1.8VALW To +1.8VS_AUDIO

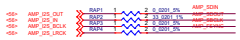


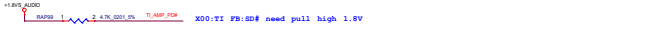
+5VS To +5VS_AUDIO

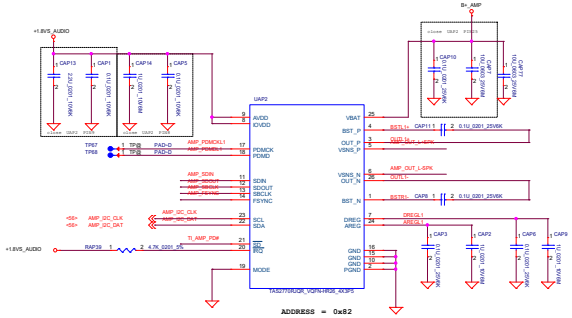


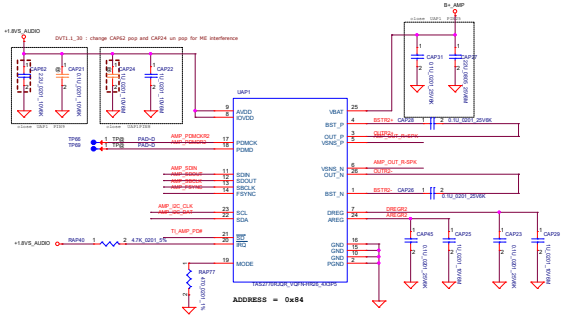
SMART AMP TAS2770

TAS2770 moment I =(15.4W/0.85)/12.6V=1.43A(Single)
B+_AMP Continuous power I=(2W/0.85)/12.6V = 0.17A
+1.8VS_AUDIO=12.6mA

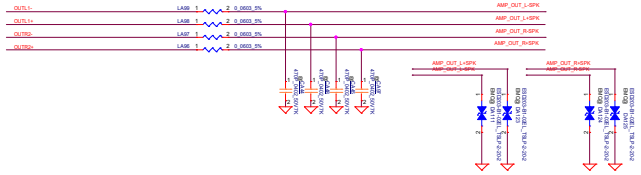




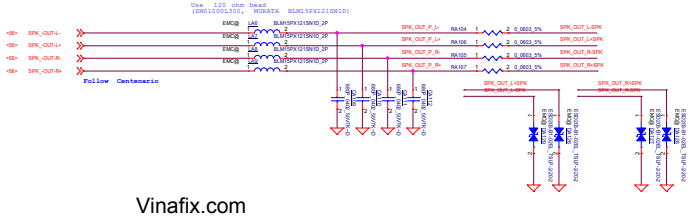


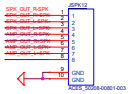


TI AMP Speaker Conn.

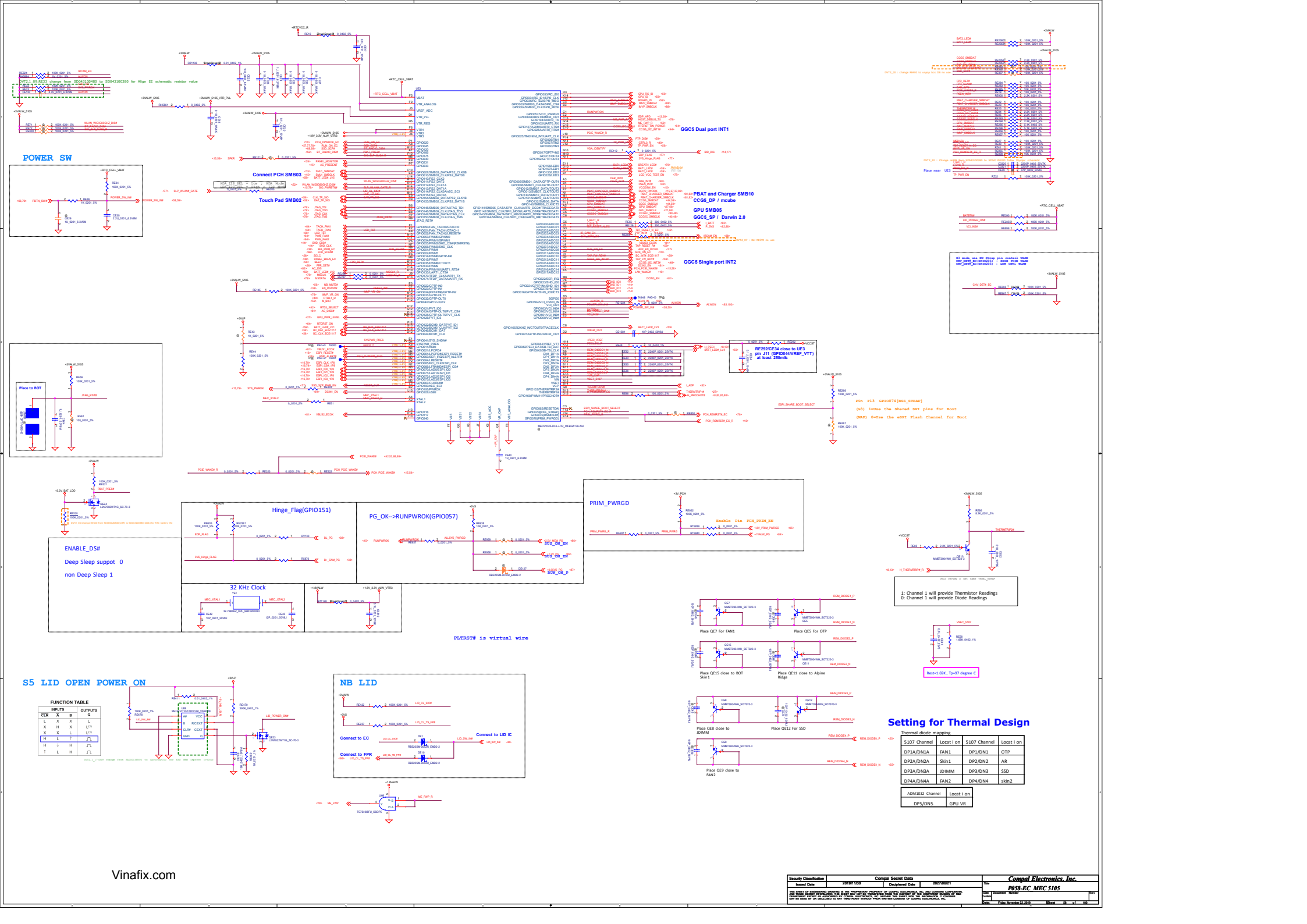


Realtek Codec Speaker Conn.





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/11/30	Deciphered Date	2027/08/21
			Title: P057-Audio Jack/SmartAMP/DB Board
			Size: Document Number: LA-J191P Rev: 0.4(0A)
			Date: Friday, November 29, 2019 Sheet 37 of 105



INPUTS			OUTPUTS
CLR	X	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

Thermal diode mapping			
5107 Channel	Locat i on	5107 Channel	Locat i on
DP1A/DN1A	FAN1	DP1/DN1	OTP
DP2A/DN2A	Skin1	DP2/DN2	AR
DP3A/DN3A	JDIMM	DP3/DN3	SSD
DP4A/DN4A	FAN2	DP4/DN4	skin2

ADM1032 Channel	Locat i on
DP5/DN5	GPU VR

Security Classification	Compal Secret Data		
Issued Date	2019/01/30	Deciphered Date	2020/08/21

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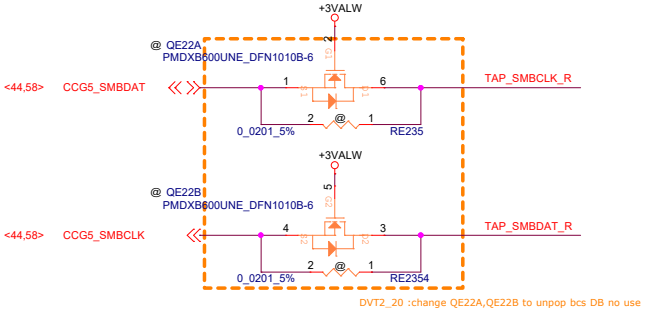
Compal Electronics, Inc.

Title: P05B-EC MEC 5105

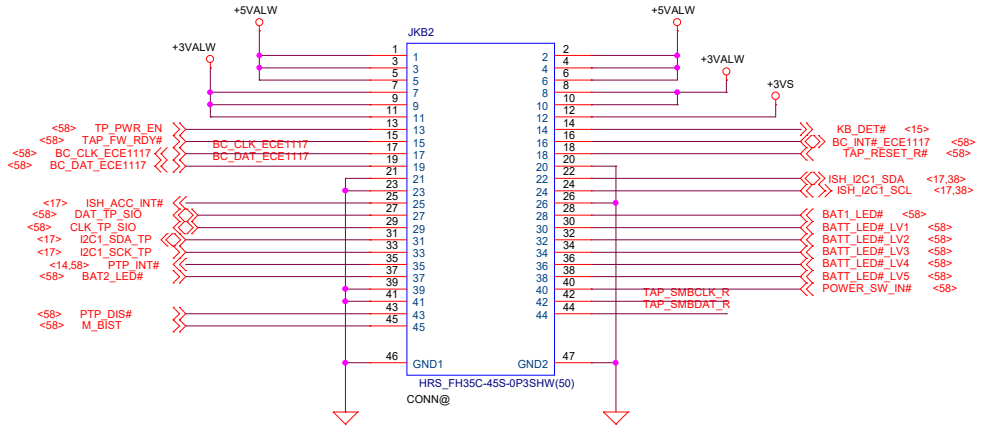
Size: C | Document Number: | Rev:

Date: Friday, November 29, 2019 | Sheet 38 of 56

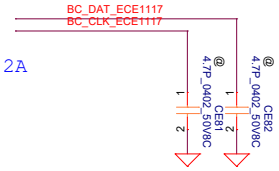
Keyboard Controller board + TAP Sensor



DVT2_20 :change QE22A,QE22B to unpop bcs DB no use



HRS_FH35C-45S-0P3SHW(50) series withstand current 0.2A
Latch-up current at Top = 25 0C 200mA
+5VALW=1.2A +3VALW=1A



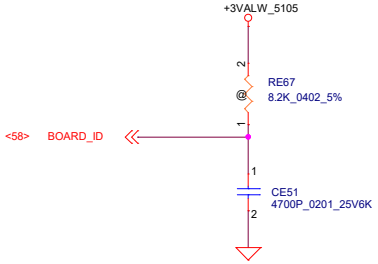
EC Strap

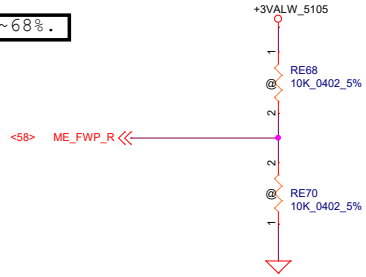
RE67	CE51	REV	PHASE
240K	4700p	M00	PRE EVT
130K	4700p	X00	EVT
62K	4700p	X00	DVT1
33K	4700p	X01	DVT1.1
8.2K	4700p	X02	DVT2
4.3K	4700p	X03	DVT2.1
2K	4700p		
1K	4700p	A00	PVT

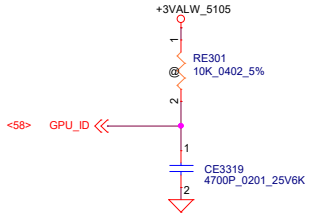
RE301	CE3319	CONFIG
240K	4700p	
130K	4700p	UMA
62K	4700p	N18P-G0
33K	4700p	
8.2K	4700p	N19P-Q1
4.3K	4700p	N19P-Q3 MAXQ
2K	4700p	
1K	4700p	

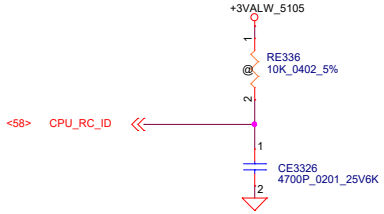
RE336	CE3326	CONFIG
240K	4700p	
130K	4700p	3PHASE-I5
62K	4700p	
33K	4700p	
8.2K	4700p	4PHASE-6+2
4.3K	4700p	
2K	4700p	
1K	4700p	4PHASE-8+2

BOARD_ID rise time is measured from 5%~68%.









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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

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Compal Electronics, Inc.

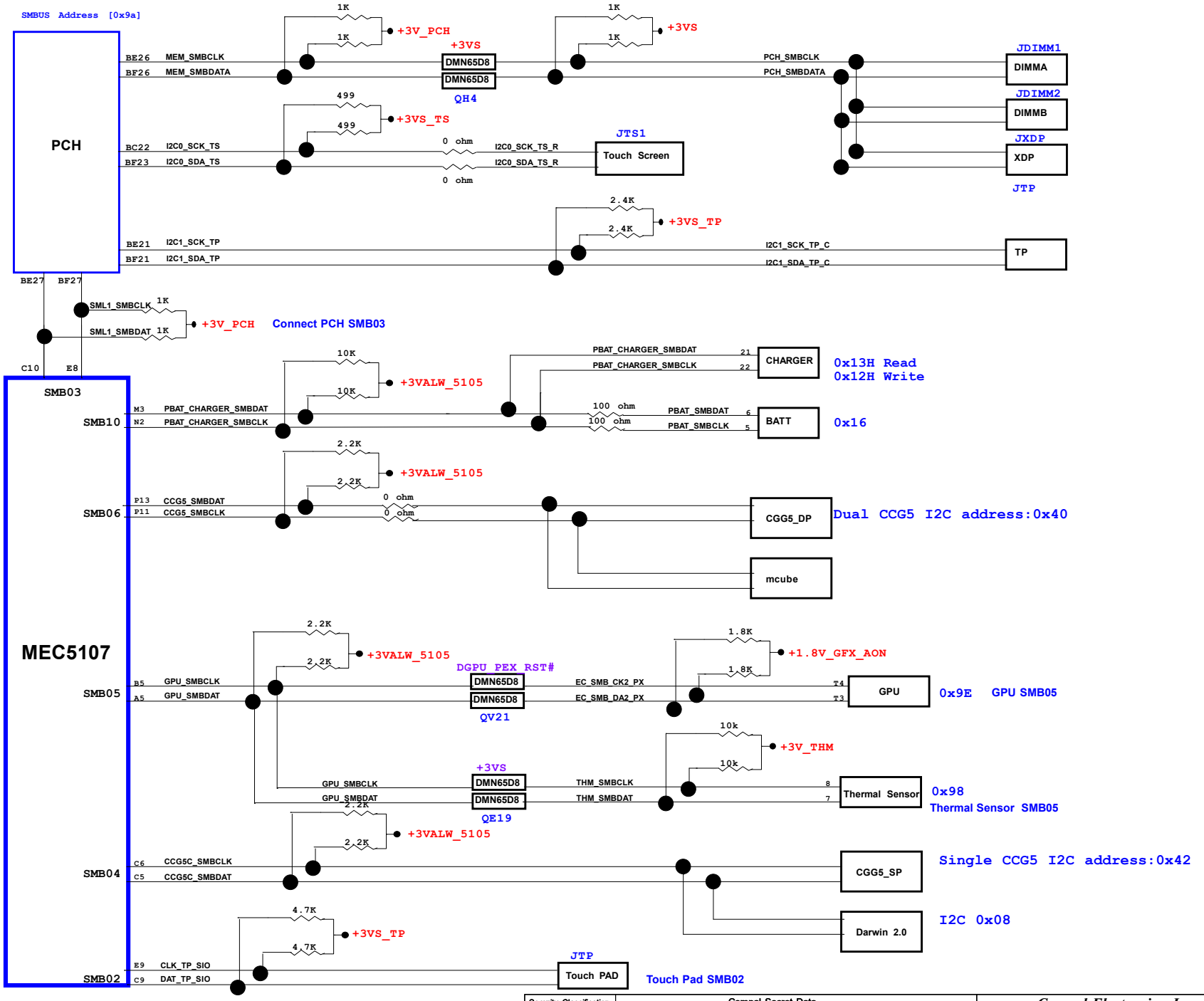
Title: P059-KBC Board

Size | Document Number: LA-J191P | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 59 of 100

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

Compal Electronics, Inc.		
Title: P060-Reserve		
Size	Document Number: LA-J191P	Rev: 0.4(X03)
Date: Friday, November 22, 2019	Sheet 60 of 100	



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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P061-SMBus block diagram

Size: Custom | Document Number | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 61 of 100

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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

Compal Electronics, Inc.

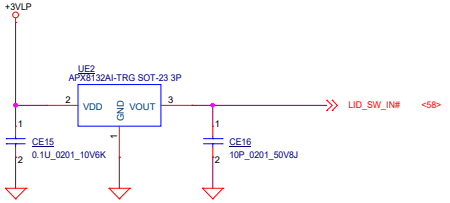
Title: *P062-Reserve*

Size | Document Number: *LA-J191P* | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 62 of 100

Power Button and LED

Lid Switch



Touch pad

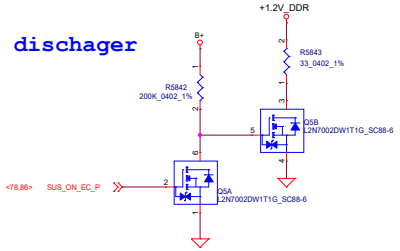
Fingerprint Reader CONN

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

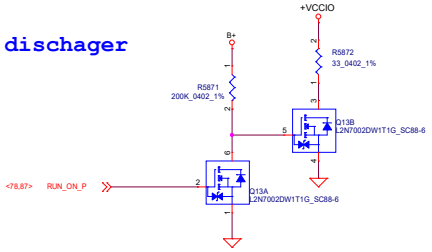
Compal Electronics, Inc.

Title	P063-BAT LED/TP/SW	
Size C	Document Number LA-J191P	Rev 0.4(003)
Date: Friday, November 22, 2019	Sheet 63 of 100	

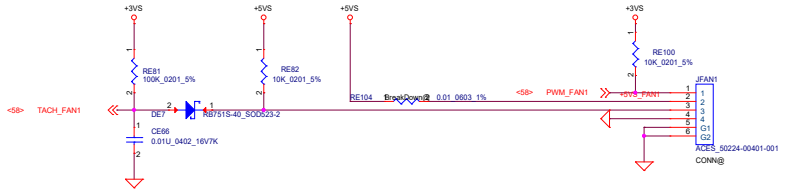
1.2V DDR dischager

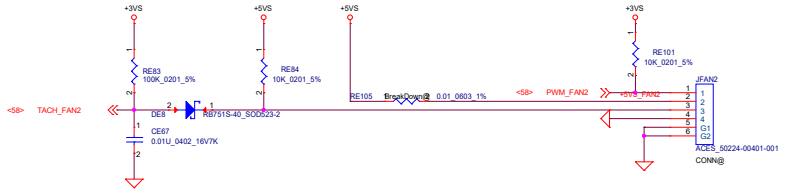


VCCIO dischager

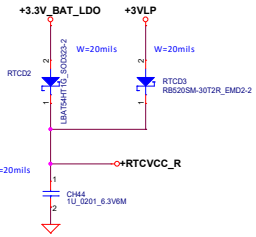


PWM FAN

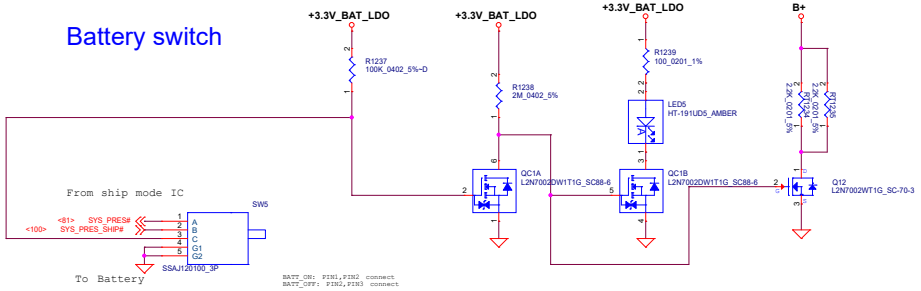




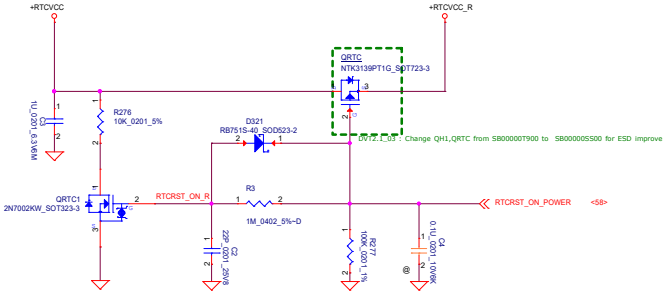
RTC Battery With Charge Function



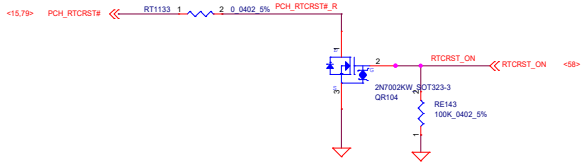
Battery switch



Default: OD EC drives GPIOs to LOW to turn ON power to VCCRTC.



follow Intel Keep old RTC X9&X8 RTC discharge schematic



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Issued Date	2019/11/30	Deciphered Date	2027/06/21

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Compal Electronics, Inc.

Title: P064-LId/RTC/FAN

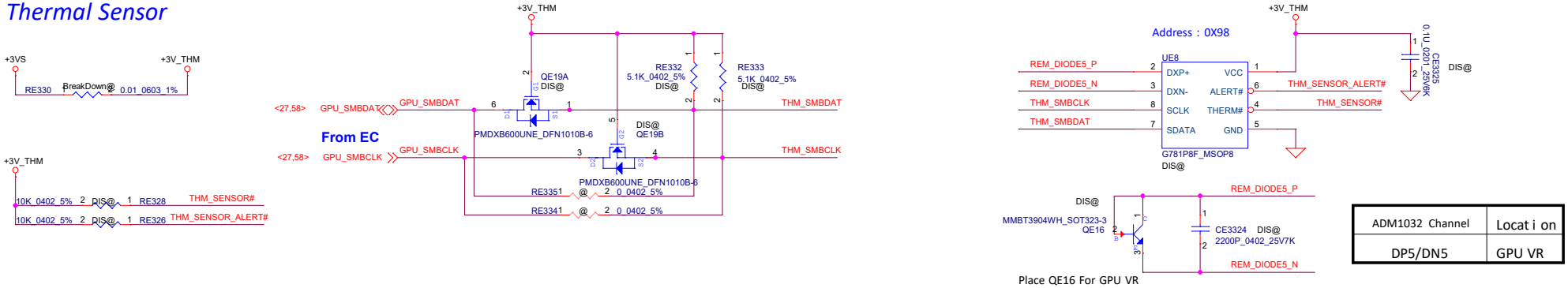
Size: LA-J191P | Document Number | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 64 of 100

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

Compal Electronics, Inc.		
Title: P065-Reserve		
Size	Document Number: LA-J191P	Rev: 0.4(X03)
Date: Friday, November 22, 2019	Sheet 65 of 100	

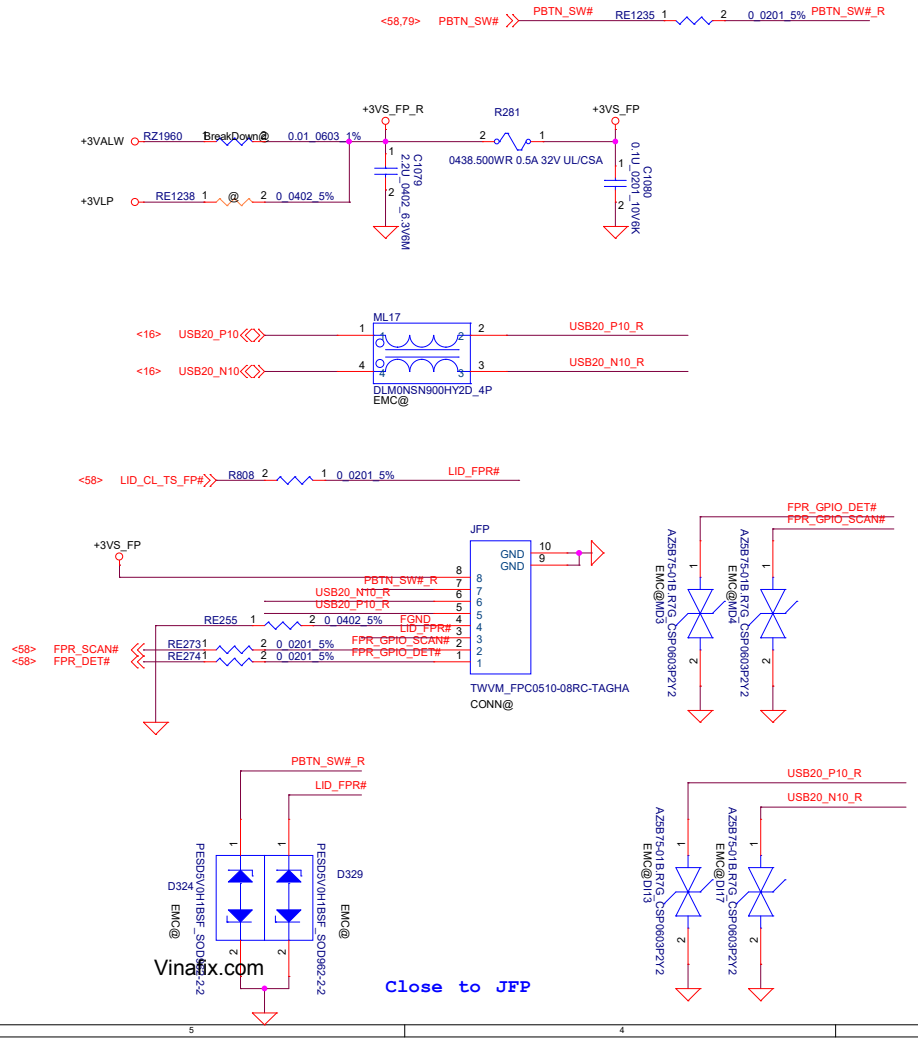
Thermal Sensor



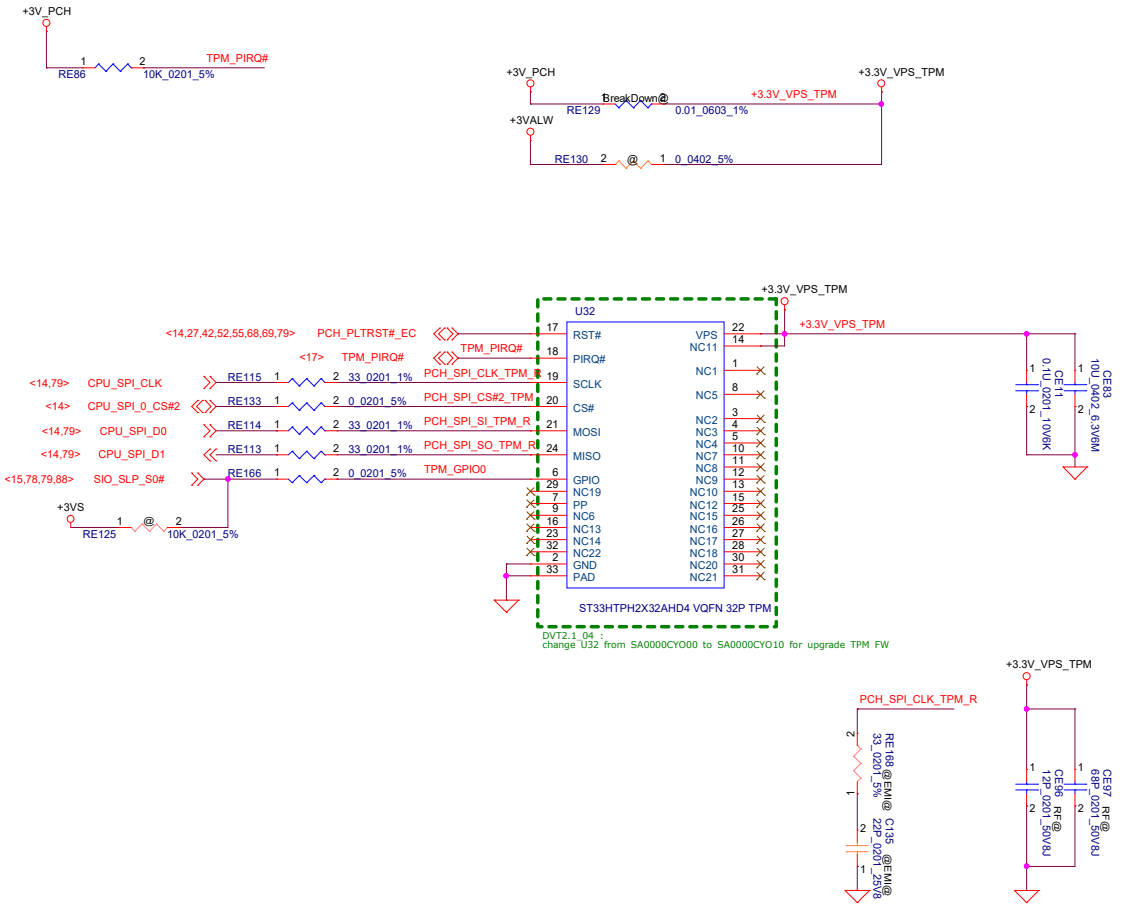
ADM1032 Channel	Location
DP5/DN5	GPU VR

Finger Print circuit

(Fingerprint Reader)
Current capability: 3.3V 150mA



ST TPM



Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P066-TPM/FP/THM Senso**

Size	Document Number	Rev
Custom	LA-J191P	0.4(X03)

Date: Friday, November 22, 2019 Sheet 66 of 100

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

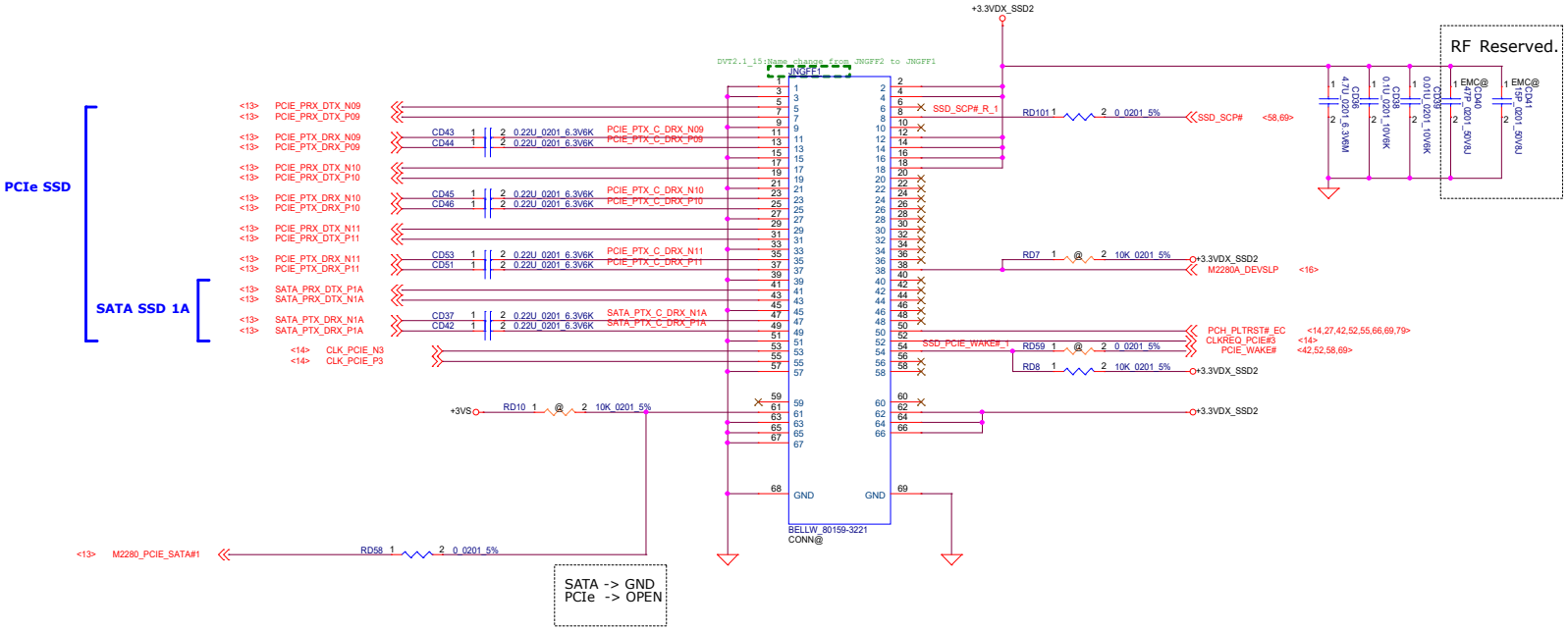
Compal Electronics, Inc.

Title: **P067-HDD / FFS**

Size	Document Number	Rev
C	LA-J191P	0.4(X03)

Date: Friday, November 22, 2019 | Sheet 67 of 100

M.2 Slot-C Key-M (SSD)



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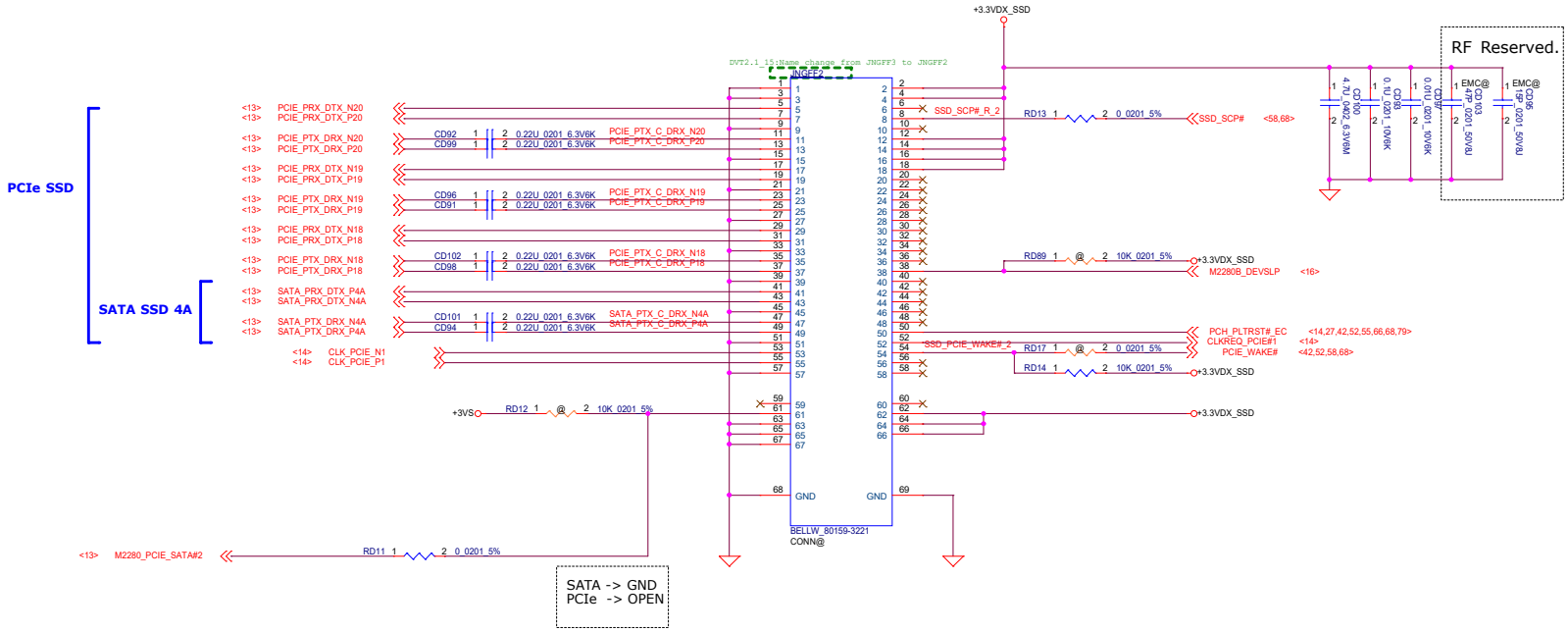
Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Compal Electronics, Inc.			
Title: P068-NGFF-SSD			
Size: C	Document Number: LA-J191P		Rev: 0.4(003)
Date: Friday, November 22, 2019	Sheet 68 of 100		

M.2 Slot-C Key-M (SSD)



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Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

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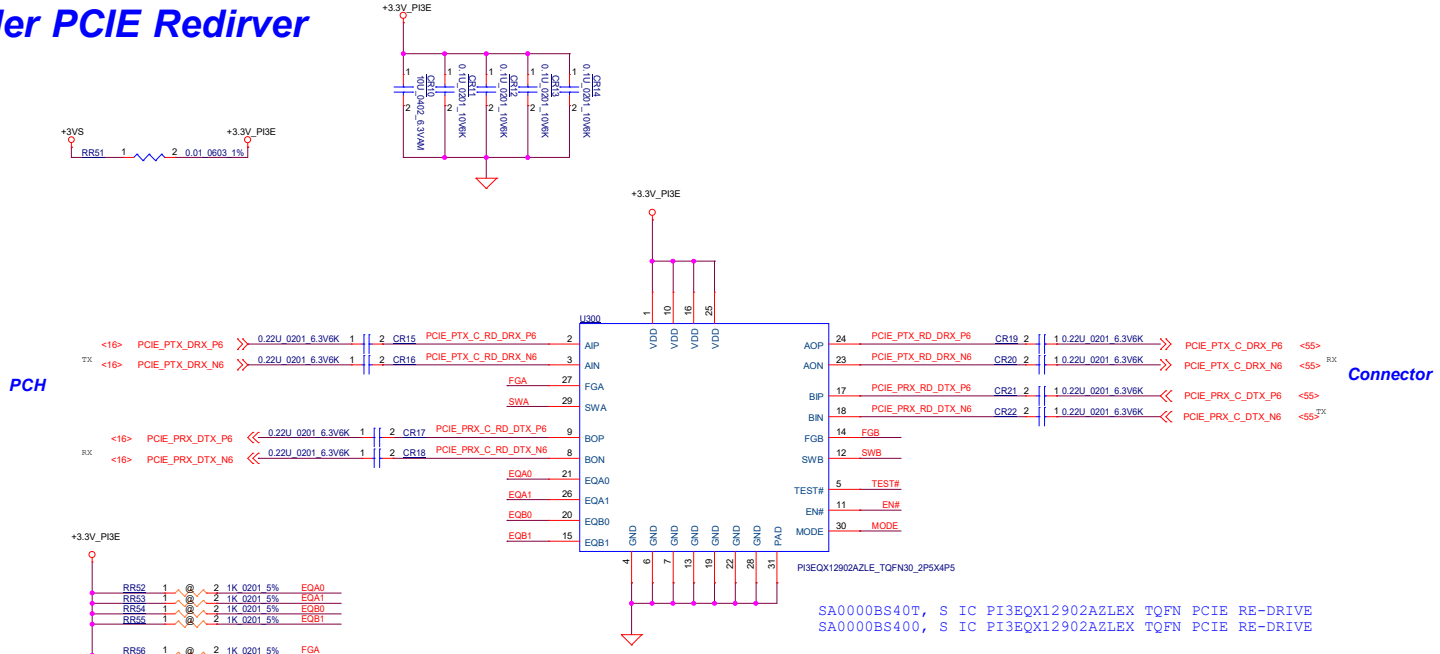
Compal Electronics, Inc.

Title: **P069-Reserve**

Size	Document Number	Rev
	LA-J191P	0.4(X03)

Date: Friday, November 22, 2019 | Sheet 69 of 100

Card reader PCIE Redirver



PCH

Connector

SA0000BS40T, S IC PI3EQX12902AZLEX TQFN PCIE RE-DRIVE
SA0000BS400, S IC PI3EQX12902AZLEX TQFN PCIE RE-DRIVE

Operation MODE pin.
" High" - For PCIe applicatios
" Low" - For SATA applicatio

Test mode Enable pin. With internal 300kΩ pull-up resistor.
"High" - Test mode disabled.
"Low" - Test mode enabled.

Channel Enable pin. With internal 300kΩ pull down resistor.
" High" - Channel is in power down mod
" Low" - Channel is in normal operatio

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P070-Card Reader**

Size	Document Number	Rev
		0.4(003)

Date: Friday, November 22, 2019 | Sheet 70 of 100

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P058-EC_MEC 5105**

Size	Document Number	Rev
Custom		

Date: Friday, November 22, 2019 | Sheet 71 of 100

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: ***P072-USB3.1 retimer***

Size	Document Number	Rev
Custom		0.4(X03)

Date: Friday, November 22, 2019 Sheet 72 of 100

Place close to JUSB1

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P073-USB3.1/USB2.0 conn**

Size	Document Number	Rev
	LA-J191P	0.4(X03)

Date: Friday, November 22, 2019 Sheet 73 of 100

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

Compal Electronics, Inc.		
Title: P074-Reserve		
Size	Document Number: LA-J191P	Rev: 0.4(X03)
Date: Friday, November 22, 2019	Sheet 74 of 100	

DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/05/08

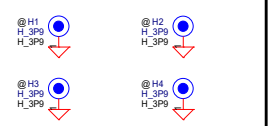
Compal Electronics, Inc.

Title: *P075-Reserve*

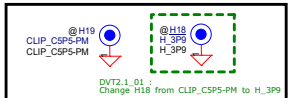
Size | Document Number: *LA-J191P* | Rev: 0.4(X03)

Date: Friday, November 22, 2019 | Sheet 75 of 100

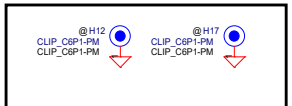
Screw Hole



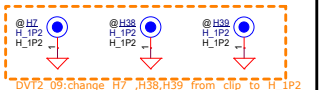
H1~H4: 3.9mm
CPU x 4



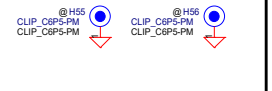
H18~H19: 5.5mm
FAN x 2



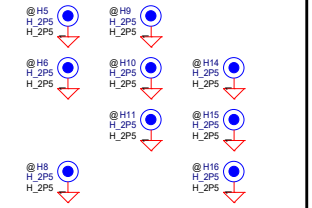
H12 H17: 6.1mm
NGFF x 2



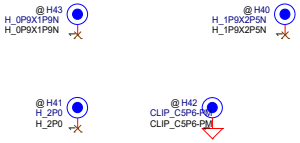
H17 H38 H39 :1.2mm
eDP&TS x 3

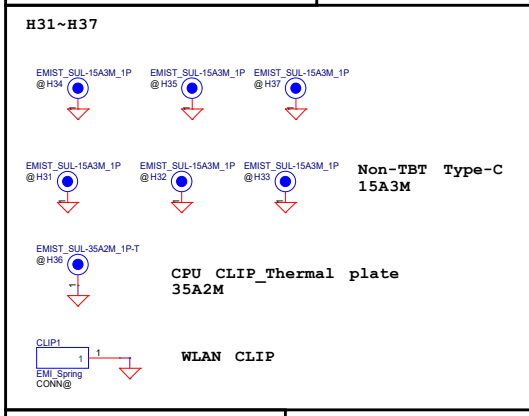


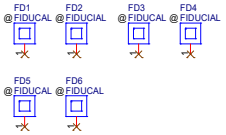
H55 H56: 6.5mm
PCH x 2



H5,H6,H8,H9,H10,H11,
H14,H15,H16: 2.5mm
other x 9







H13: 2.6mm
TOP side WLAN NGFF

Vinafix.com

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

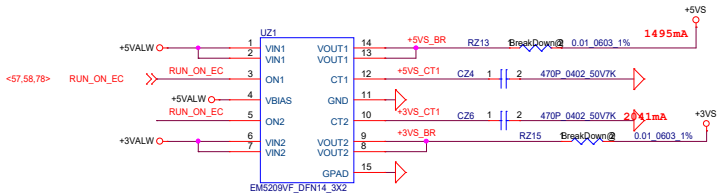
Compal Electronics, Inc.

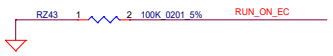
Title: P076-Screws

Size	Document Number	Rev
		0.4(X03)

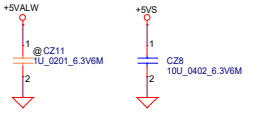
Date: Friday, November 22, 2019 Sheet 76 of 100

+5VALW to +5VS
+3VALW to +3VS

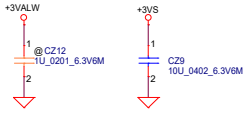




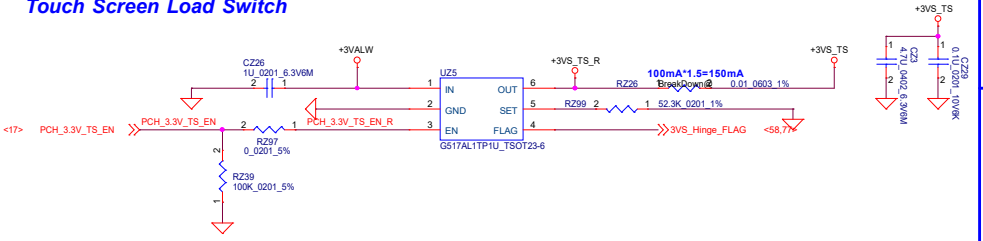
Close UZ1



Close UZ1

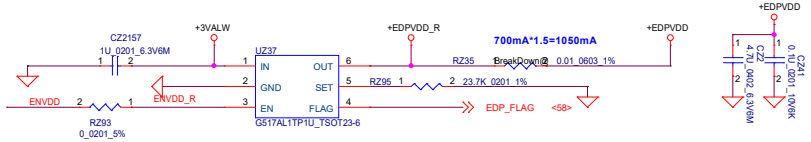


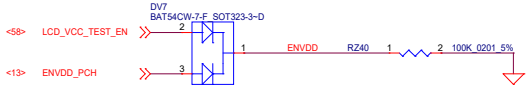
Touch Screen Load Switch



Ron=70m ohm
Current Limit =25K/52.3K=0.478A

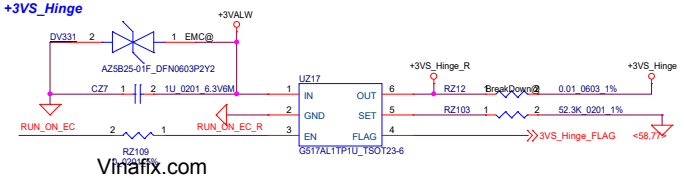
eDP Load Switch

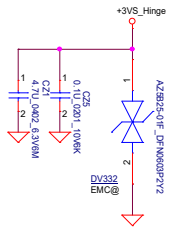




Ron=70m ohm
Current Limit =25K/23.7K=1.055A

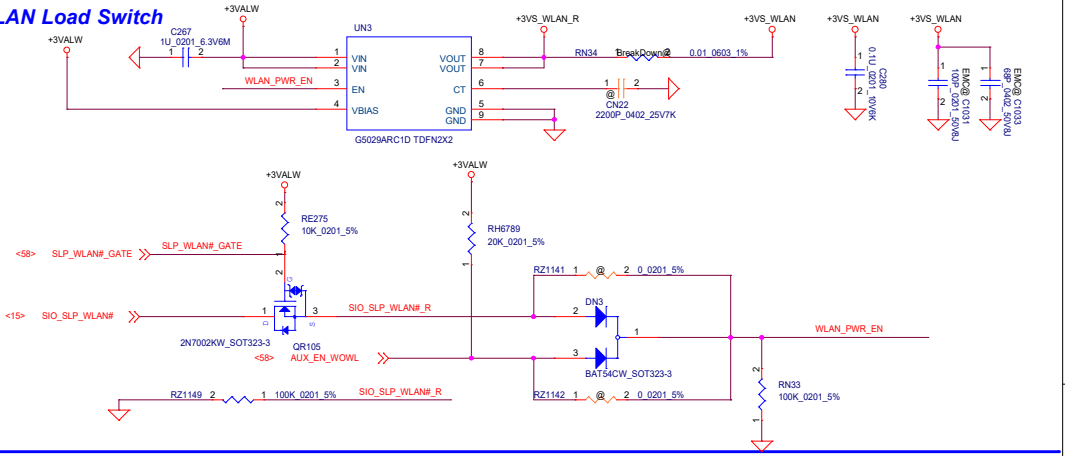
+3VALW to +3VS_Hinge



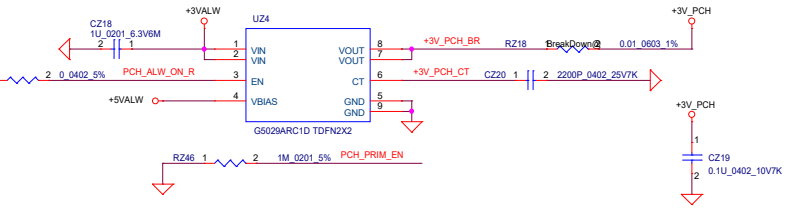


Ron=70m ohm
Current Limit =25K/52.3K=0.478A

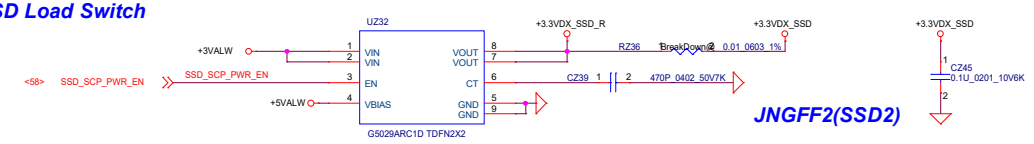
WLAN Load Switch

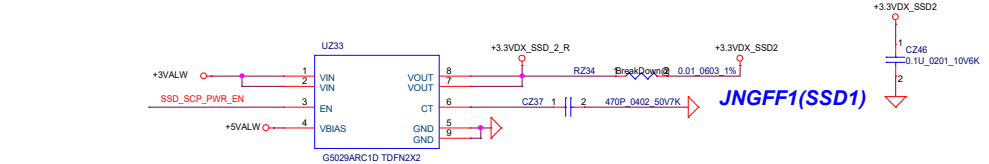


+3VALW to +3V_PCH

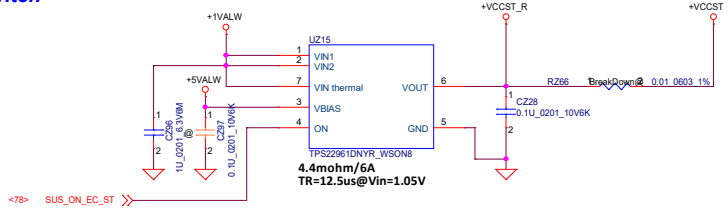


SSD Load Switch





+VCCST Load Switch



Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P077-DC/DC SYSTEM

Size	Document Number	Rev
	LA-J191P	0.4(003)

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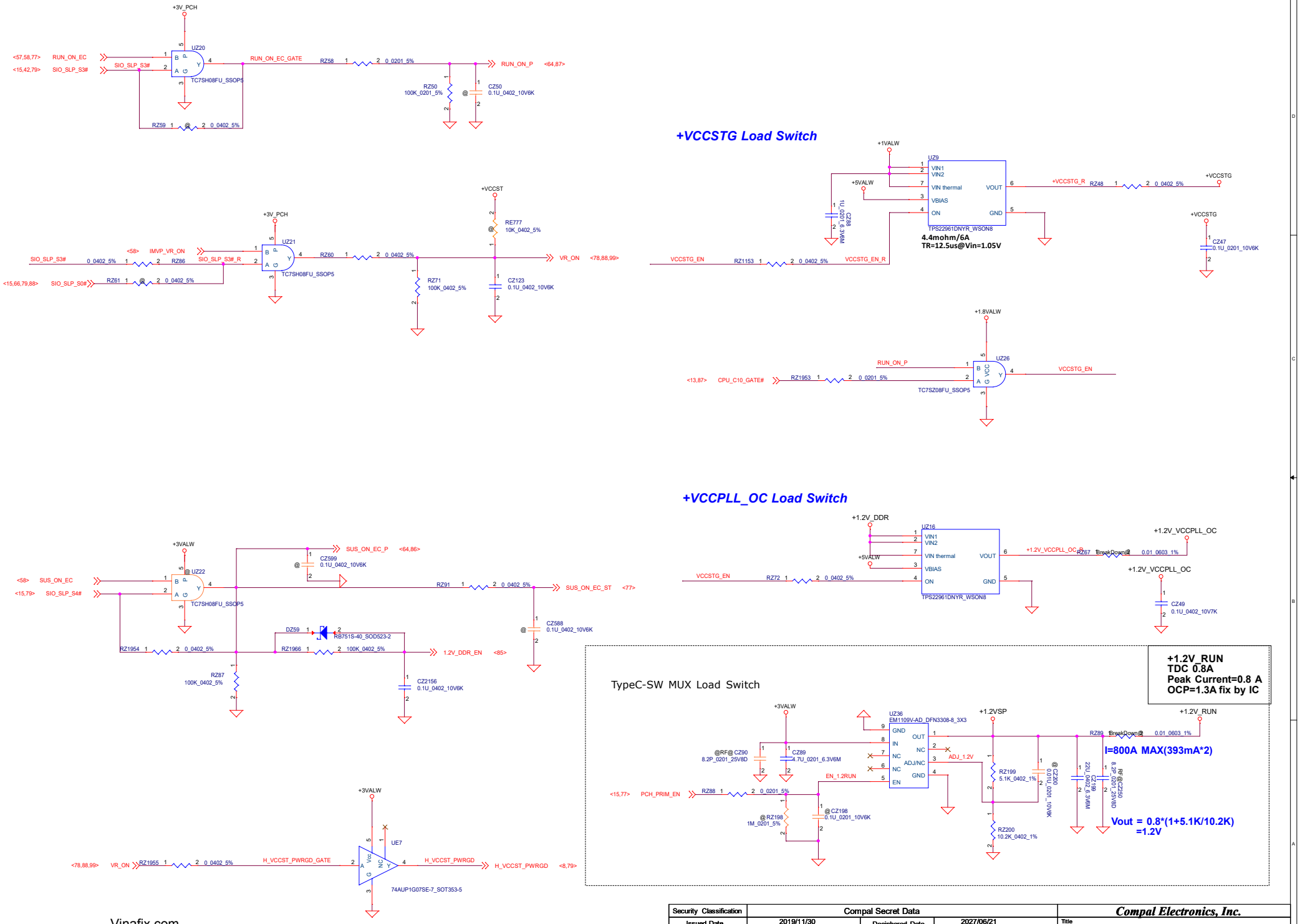

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2027/06/21

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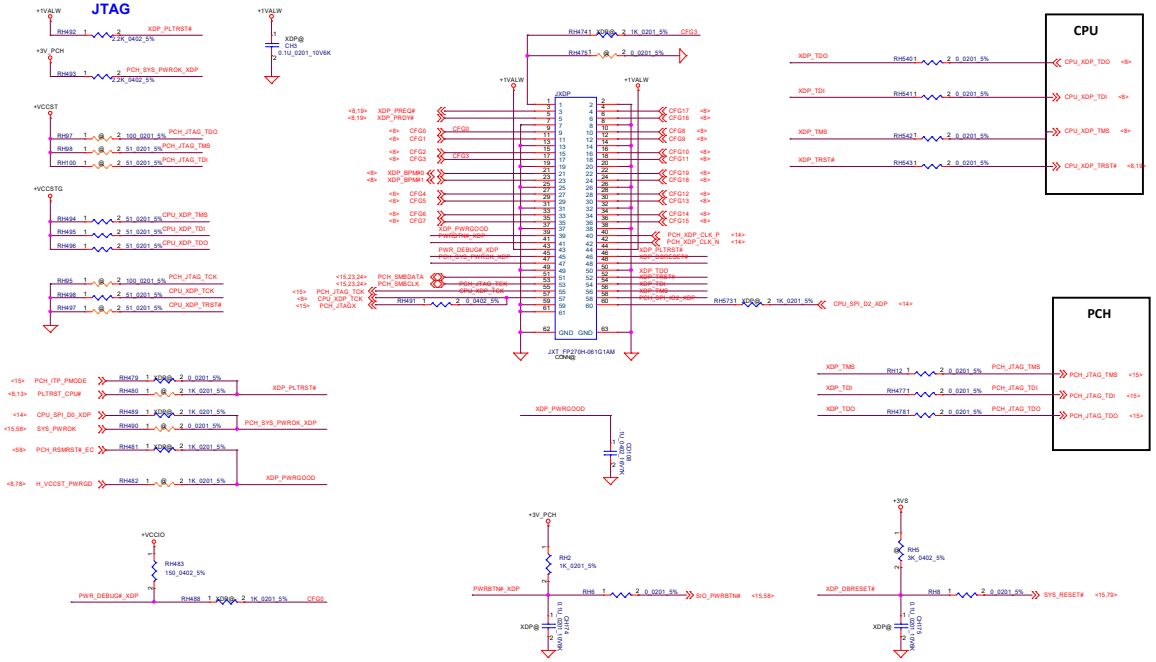
Compal Electronics, Inc.

Title: P078-DC/DC/S0iX/CS

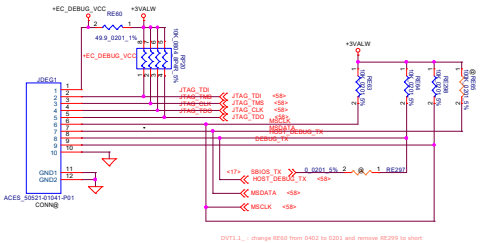
Size	Document Number	Rev
	LA-J191P	0.4(003)

Date: Friday, November 22, 2019 | Sheet 78 of 100

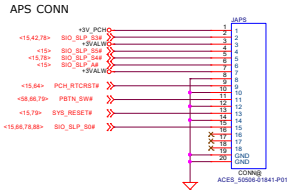
JXDP



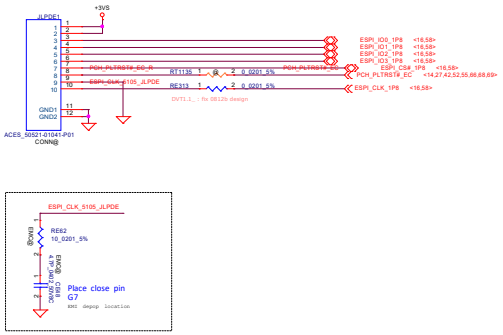
JDEG



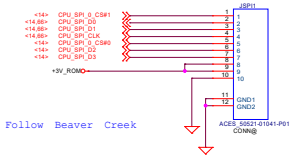
JAPS



JLPDE



JSPI

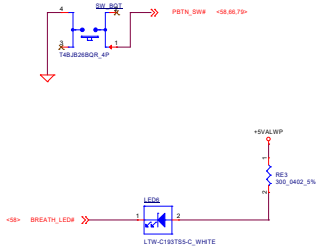


FLASH DESCRIPTOR SECURITY OVERRIDE

Strap Definitions(HDA_SDO /I2S0_TXD)

GPP_R2/HDA_SDO (Internal 20 K Pull Down)
0 = ENABLE (DEFAULT)
1 = DISABLE (ME can update)

Debug Power Button BOT side



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/11/30	Deciphered Date 2027/06/21	Title: P079-XDP/APS/SPI/LPDE...Debug
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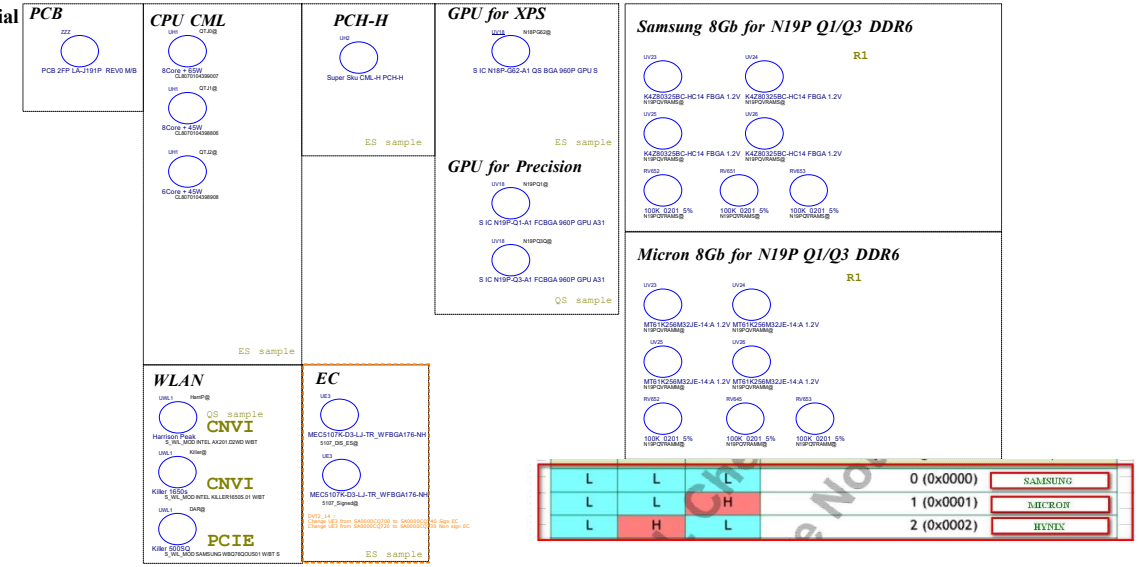
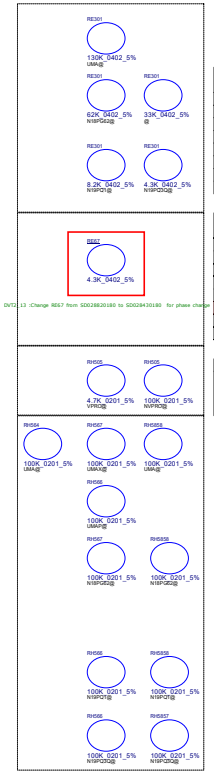
			Date: Friday, November 22, 2019 Sheet 79 of 100

Compal Confidential

Project Code :
File Name :

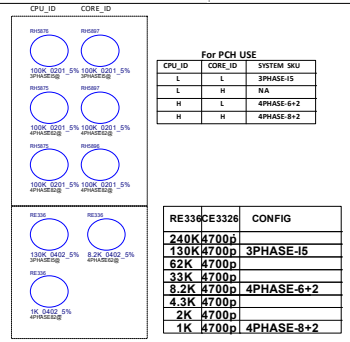




RE301	CE3319	CONFIG
240K	4700p	
130K	4700p	UMA
62K	4700p	N18P-G62
33K	4700p	NA
8.2K	4700p	N19P-Q1
4.3K	4700p	N19P-Q3 MAXQ
2K	4700p	
1K	4700p	

RE67	CE51	REV	PHASE
240K	4700p	M00	PRE EVT
130K	4700p	X00	EVT
62K	4700p	X00	DVT1
33K	4700p	X01	DVT1.1
8.2K	4700p	X02	DVT2
4.3K	4700p	X03	DVT2.1
2K	4700p		
1K	4700p	A00	PVT

TLS CONFIDENTIALITY
HIGH(4.7K)
LOW(DEFAULT)(100K)
BIOS 20k internal pull-down



CPU_ID	CORE_ID	SYSTEM SKU
L	L	3PHASE-I5
L	H	NA
H	L	4PHASE-6+2
H	H	4PHASE-8+2

For PCH USE

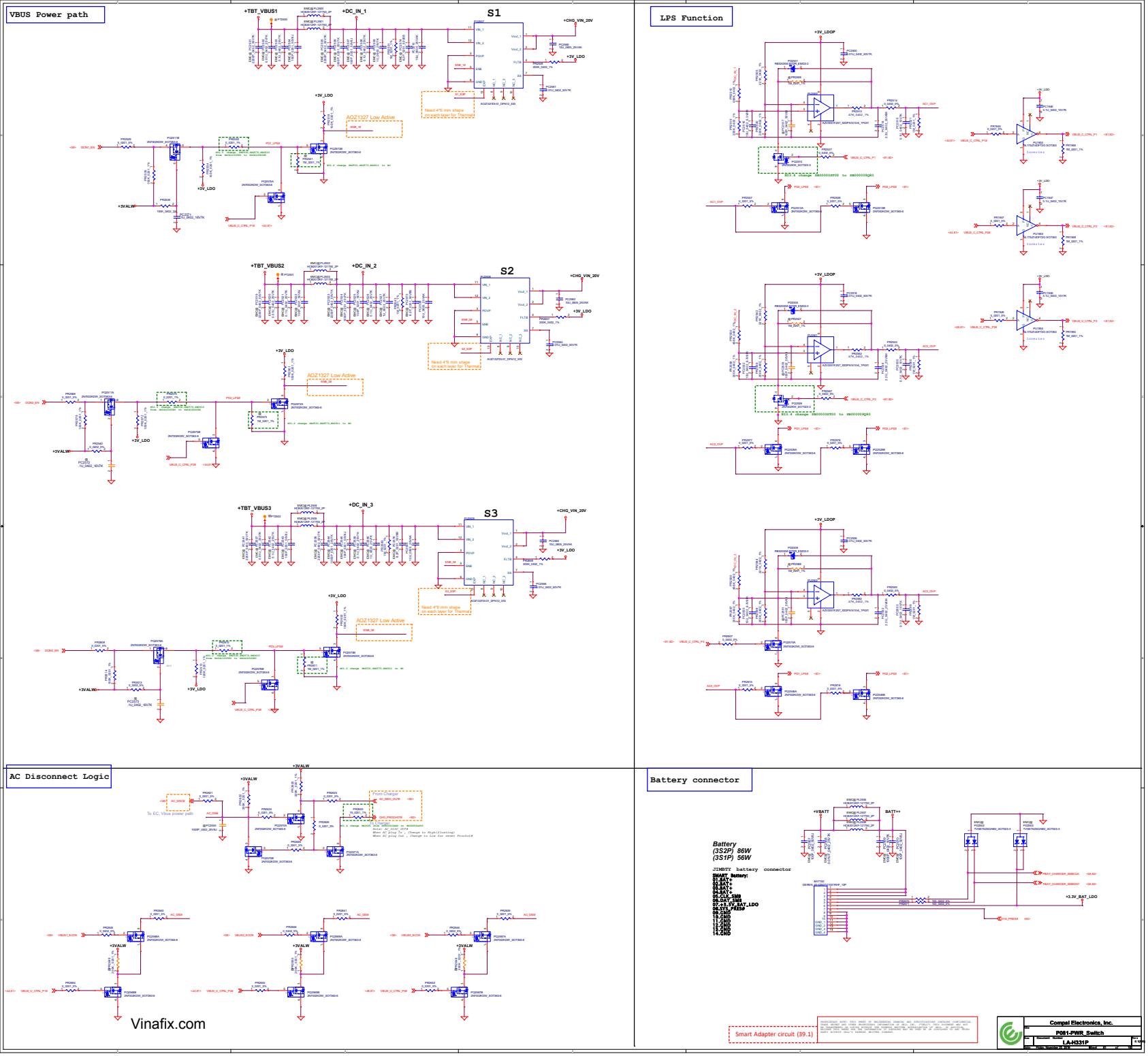
RE336	CE3326	CONFIG
240K	4700p	
130K	4700p	3PHASE-I5
62K	4700p	
33K	4700p	
8.2K	4700p	4PHASE-6+2
4.3K	4700p	
2K	4700p	
1K	4700p	4PHASE-8+2

GPU type	Config Sku/Division		SYSTEM ID1	SYSTEM ID2	SYSTEM ID3
			BID_DIS	BID_XPS_CSMB / BID_Persion_BC	BID_GPU
IGFX	XPS_CSMB	UMA	H	L	L
	Persion_BC	UMA	H	H	L
DGFX	XPS_CSMB	Nvidia N18P-G0	L	L	L
		Nvidia N18P-G0 MAX-Q	L	L	H
	Persion_BC	Nvidia N19P-Q1	L	H	L
		Nvidia N19P-Q3 MAX-Q	L	H	H

DRAM Option	DRAM Config Option MEM_CONFIG0 MEM_CONFIG1 MEM_CONFIG2 MEM_CONFIG3 MEM_CONFIG4	DRAM SDP / DDP Option	R_COMP	X76
SDP MICRON 8G/2400				X7674531L07
SDP HYNIX 8G/2400				X7674531L09
SDP SAMSUNG 8G/2400				X7674531L08
DDP MICRON 16G/2400				X7674531L10
DDP HYNIX 16G/2400				X7674531L15
DDP SAMSUNG 16G/2400				X7674531L11

Security Classification	Compal Secret Data		
Issued Date	2019/11/30	Deciphered Date	2018/12/31

Compal Electronics, Inc.			
Title: P080-BOM Option			
Size	Document Number: LA-J191P		Rev: 0.4(X0)
Date: Friday, November 22, 2019	Sheet 80 of 100		


VBUS Power path
+TBT_VBUS1
+DC_IN_1
S1
+CHG_VIN_20V
+3V_LDO
AOZ1327 Low Active
+3VALW
+TBT_VBUS2
+DC_IN_2
S2
+TBT_VBUS3
+DC_IN_3
S3
LPS Function
+3V_LDOP
AC Disconnect Logic
+3VALW
Battery connector
+VBATT
BATT++
Battery
(3S2P) 86W
(3S1P) 56W
JIMBTY battery connector
SMART_Battery:
01.BAT+
02.BAT+
03.BAT+
04.BAT+
05.BAT_SMB
06.BAT_SMB
07.+3.3V_BAT_LDO
08.SYS_PRESP
09.GND
10.GND
11.GND
12.GND
13.GND
14.GND
+3V_BAT_LDO
Smart Adapter circuit (39.1)
Compal Electronics, Inc.
P081-PWR_Switch
LA-H331P
Vinafix.com

SH00000NW00

Part Number	L0 Inductance (μH) @ (0A)	Rdc (mΩ) Typical	Rdc (mΩ) Maximum	Heat Rating Current DC Amps. Idc (A.) Typical	Saturation Current DC Amps. Isat (A.) Typical
PCMB053T-1R0MS	1.0	13.0	14.0	7.0	11.0

+CHG_VIN_20V = 5~20V
B+ = 9~13.4V (3S battery)
Support 130W
Freq =700k Hz

+CHG_VIN_20V
+PWR_SRC_AC
+CHG_SRC_20V
PR1900 0.01_1206_1%
EMC@ PL1900 1UH_PCMB053T-1R0MS_7A_20%
PD1904 SMF4L22A_SOD123FL2
TVS diode
Low Noise X5R SE00000X210 *7 Place on TOP Side
Low Noise X6S SE00001BM10 *7 Place on BOT side near H/S MOSFET
B+
X6S low noise SE00001BM10 *5
97Whr/(3*3.7)*1.5=12.8A
12.8*12.8*5m=0.82W
+VBATT
X6S low noise SE00001BM10 *2
PU1900 ISL9538CHRTZ-T_TQFN32_4X4
X01.16 change PR1907 from 2.2_1206_5%(SD011220B80) to 10_1206_5%(SD011100A80)
X01.17 change PC1926 from 2.2U_25V_X5R(SE00000WP00) to 4.7U_25V_X6S(SE00001CJ00)
X01.1 pop PC1935 and change from SE00000GB80 to SE000013H00
For battery 60% stop charge in factory. (Manufacture mode)
X02.8 change to non pop due to no use
+3V_LDO
PU1901 TC7SH08FU_SSOP5

SH00000CN00

PART NUMBER	INDUCTANCE Lo(μH) ±20% @0A	Q Min	Rdc (mΩ) Typ.	Rdc (mΩ) Max	HEAT RATING CURRENT(Idc) DC AMPS[1]	SATURATION CURRENT(Isat) DC AMPS[2]
MMD-10DZ-1R0M-X1	1.0	24	2.9	3.3	18	36

Compal Electronics, Inc.
P082-PWR_CHARGER(ISL88738)
Document Number: LA-H331P
Rev: 0.1(XXX)
Date: Friday, November 22, 2019 Sheet 82 of 100

SH00001ST00
Package: 11.5x 10 x 3

Part number	Inductance ±20%@0A (μH)	Rdc(mΩ) Typ.	Rdc(mΩ) Max.	Heat rating current (Idc)[1] DC amps (A)	Saturation current (Isat)[2] DC amps (A)	Rs @1Mhz (Ω)Max
MMD-10CZN1R5M-R1L	1.5	6.5	7.5	16.0	20.0	0.21

SH00000SD00
Package: 10.3 x 11.2 x 3.0

Part Number	L0 Inductance (μH) @ (0A)	R_{dc} (mΩ) Typical	R_{dc} (mΩ) Maximum	Heat Rating Current DC Amps. Idc (A) Typical	Saturation Current DC Amps. Isat (A) Typical
PCMB103T-2R2MS	2.2	8.0	9.0	13.0	16.0

B+
EMC@PL403 HCB2012KF-121T50_2P
EMC@PL402 HCB2012KF-121T50_2P
13.5VB_35V
X5R low noise
SE00000X210 *1
@EMC@ PC457 8.2P_0201_50V8B
PC420 100U_D_20VM_R55M
EMC@ PC403 15P_0402_50V8J
EMC@ PC404 0.1U_0402_25V6
EMC@ PC405 2200P_0402_50V7K
PC406 10U_0603-H1.2_25V6M
SH00001ST00
SH00001TW00
L_10X10X3_M
PQ400 AON6380_DFN5X6-8-5
PR400 0_0402_5%
PC400 10U_0402_10V6M
@PC401 100P_0402_50V8J
@PC402 100P_0402_50V8J
PR401 69.8K_0402_1%
PR402 160K_0402_1%
PR403 102K_0402_1%
PR404 102K_0402_1%
PR405 12K_0402_1%
PR406 12K_0402_1%
FB_3V
FB_5V
PR408 0_0402_5%
PR407 0_0402_5%
@PR428 100K_0402_5%
ALW_PWRGD_3V_5V
<15,50>
<58,83,100>
ALWON
PU400 TPS51285BRUKR_QFN20_3X3
CS2 VFB2 VREG3 VFB1 CS1
EN2 PGOOD SW2 VBST2 DRVH2
TP EN1 VCLK SW1 VBST1 DRVH1
DRVL2 VIN VREG5 VO1 DRVL1
PR409 0_0402_5%
PR410 200_0402_1%
PQ401 AON6380_DFN5X6-8-5
13.5VB_35V
XR low noise
SE00000X210 *1
+3VLP
+3VALWP
+5VALWP
PL400 1.5UH_MMD-10CZN1R5M-R1L_16A_20%
PL401 2.2UH_PCMB103T-2R2MS_13A_20%
PC410 0.1U_0402_25V7K
PR411 2.2_0805_1%
PC411 0.1U_0402_25V7K
PR412 2.2_0805_1%
BST_3V_R
BST_3V
BST_5V
BST_5V_R
LX_3V
LX_5V
UG_3V
UG_5V
LG_3V
LG_5V
PQ402 AON6314_N_DFN56-8-5
PQ403 AON6354_N_DFN56-8-5
PC2969 150U_B2_6.3VM_R35M
PC412 150U_B2_6.3VM_R35M
EMC@ PR413 4.7_1206_5%
SNUB_3V
EMC@ PC414 680P_0402_50V7K
@PC415 1U_0402_16V7K
PR415 0_0402_5%
PC418 0.1U_0402_25V6
PC419 4.7U_0603_6.3V6M
@PC416 .1U_0402_16V7K
EMC@ PR414 4.7_1206_5%
SNUB_5V
EMC@ PC417 680P_0402_50V7K
PC456 150U_B2_6.3VM_R35M
PC413 150U_B2_6.3VM_R35M
@EMC@ PC458 8.2P_0201_50V8B
EMC@ PC407 0.1U_0402_25V6
EMC@ PC408 2200P_0402_50V7K
PC409 10U_0603-H1.2_25V6M

R4=(Vo-2)/2*R5
Valtage setting: Vo=3.37V

R1=(Vo-2)/2*R2
Valtage setting: Vo=5.14V

+3VALWP JUMP@ PJP402 PAD-OPEN 4x4m +3VALW
+5VALWP JUMP@ PJP403 PAD-OPEN 4x4m +5VALW

3.3VALWP
3.3V +/-5%
TDC 10.83A
Peak Current 14.72A
OCP current 19.2 A
Freq 475k Hz

5VALWP
5.1V +/-5%
TDC 8.19A
Peak Current 11.33A
OCP current 19.2A
Freq 400k Hz

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3V/5V controller(35.1), Support component(35.2)

Compal Electronics, Inc.
Title: P083-PWR_3.3VALWP/5VALWP
Size: Document Number: LA-H331P
Rev: 0.1(X00)
Date: Friday, November 22, 2019
Sheet 83 of 100

SH00000PJ00
Package: : 6.6 x 7.3 x 3.0

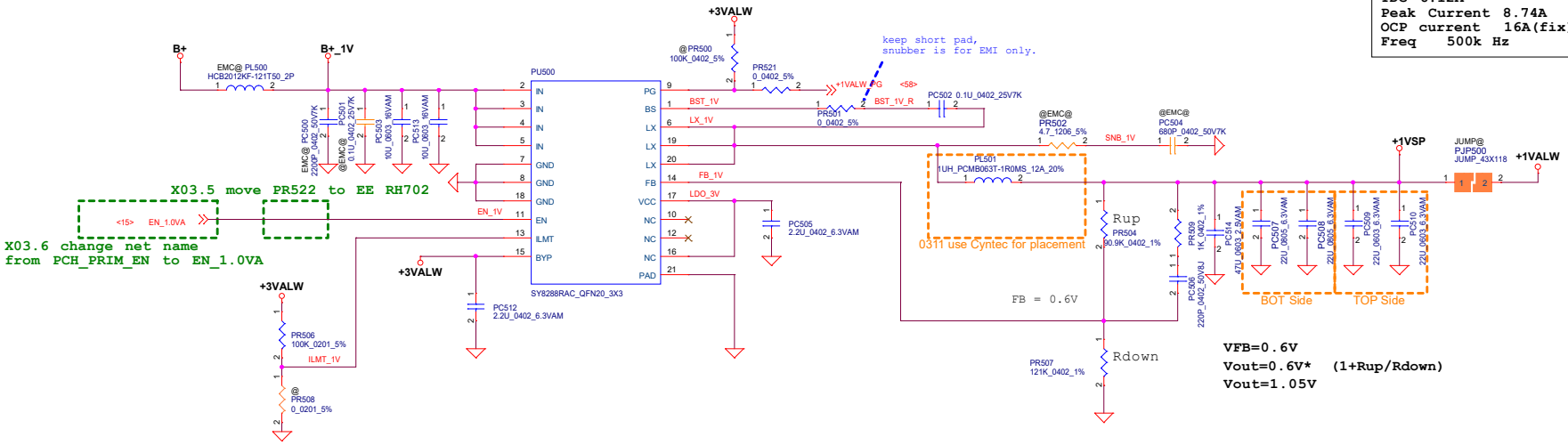
Part Number	L0 Inductance (µH) @ (0A)	R_{dc} (mΩ)		Heat Rating Current DC Amps. Idc (A)	Saturation Current DC Amps. Isat (A)
		Typical	Maximum	Typical	Typical
PCMB063T-1R0MS	1.0	6.7	7.4	12.0	15.0

EN :H>0.8V ; L<0.4V

EN pin don't floating

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

+1VSP
1.05V +/-5%
TDC 6.12A
Peak Current 8.74A
OCP current 16A(fix)
Freq 500k Hz



PWR.Plane.Regulator(35.5), Support component(35.6)

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P084-PWR_PCH_1V(SY8288RAC)

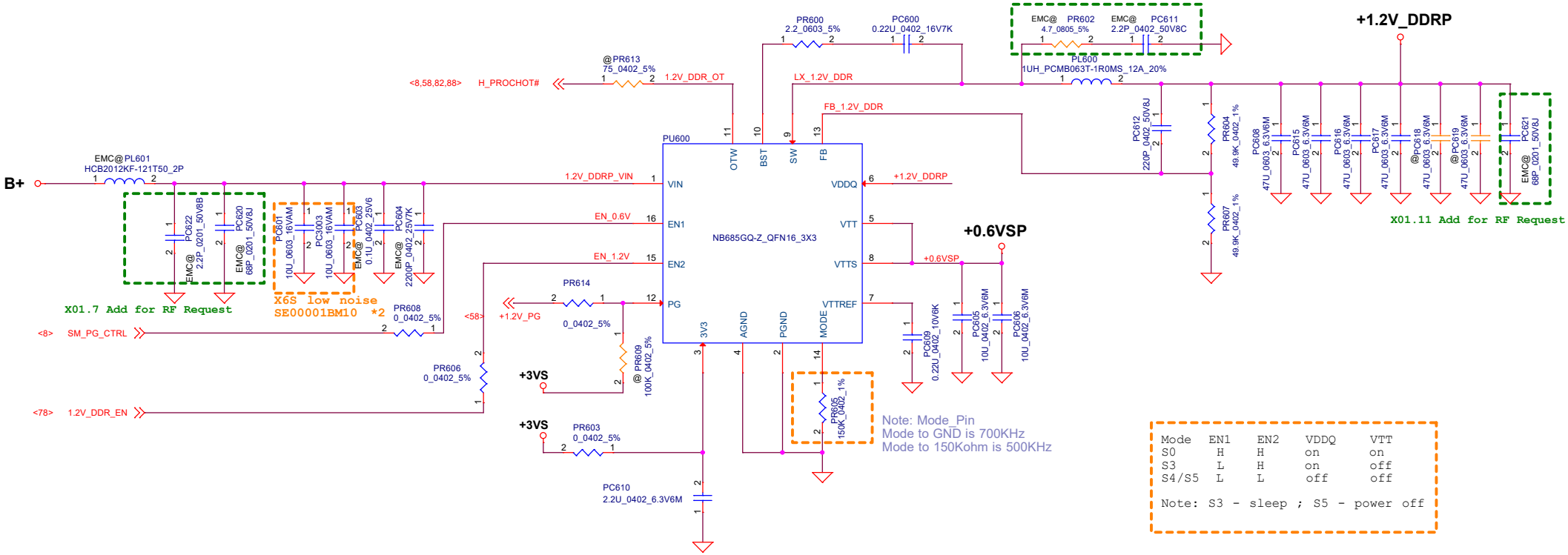
Size	Document Number	Rev
	LA-H331P	0.1(000)

Date: Friday, November 22, 2019 Sheet 84 of 100

SH00000PJ00
Package: : 6.6 x 7.3 x 3.0

Part Number	L0 Inductance (µH) @ (0A)	R_{dc} (mΩ)		Heat Rating Current DC Amps. Idc (A)	Saturation Current DC Amps. Isat (A)
		Typical	Maximum	Typical	Typical
PCMB063T-1R0MS	1.0	6.7	7.4	12.0	15.0

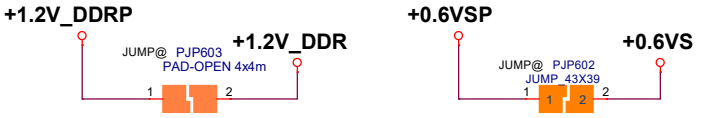
X01.8 change for RF Request



Note: Mode_Pin
Mode to GND is 700KHz
Mode to 150Kohm is 500KHz

Mode	EN1	EN2	VDDQ	VTT
S0	H	H	on	on
S3	L	H	on	off
S4/S5	L	L	off	off

Note: S3 - sleep ; S5 - power off



+1.2V_MEN_P
1.2V +/- 5%
TDC 7.16A
Peak Current 10.23A
OCP current 13A (TYP.)
Freq 500k Hz

+0.6VSP
0.6V +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.5A

DDR controller(35.3), Support component(35.4)

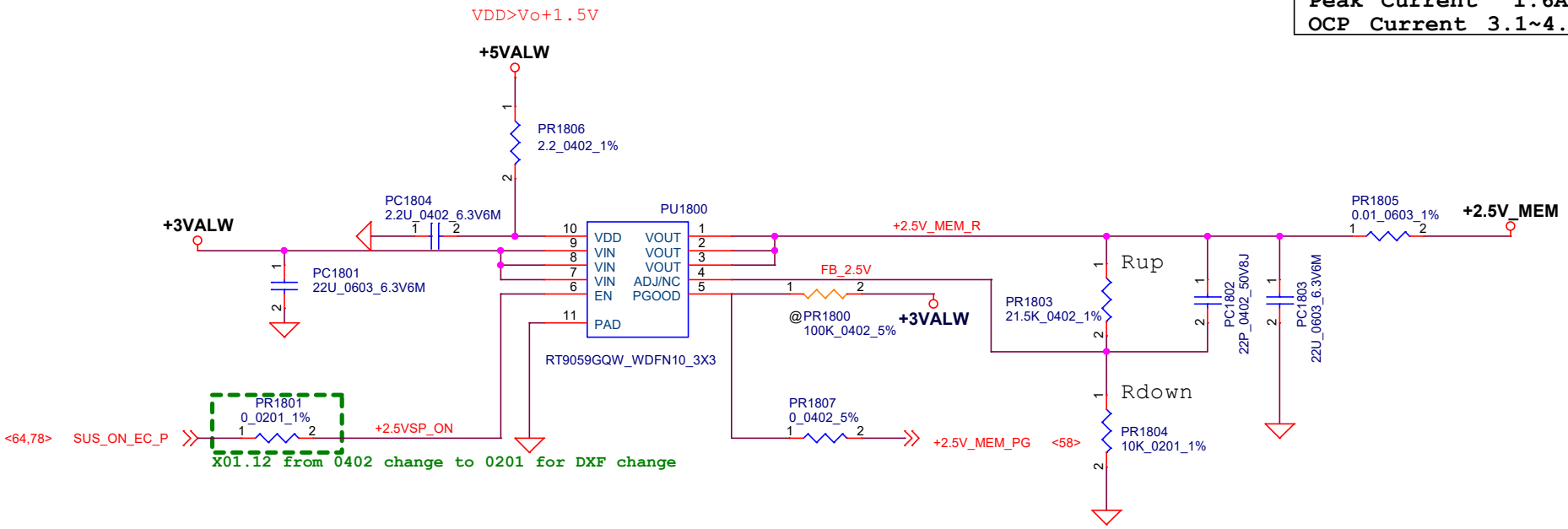
Compal Electronics, Inc.

Title: PWR_+1.2V_DDR/+0.6V

Size | Document Number: LA-F211P/LA-F212P | Rev: 1.0(A00)

Date: Friday, November 22, 2019 | Sheet 85 of 100

+2.5V_MEM
2.5V +/-5%
TDC 1.6A
Peak Current 1.6A
OCP Current 3.1~4.6A



2.5V_MEM controller(35.11), Support component(35.12)

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P086-PWR_+2.5V_MEM(RT9059GSP)**

Size | Document Number: **LA-H331P** | Rev: 0.1(X00)

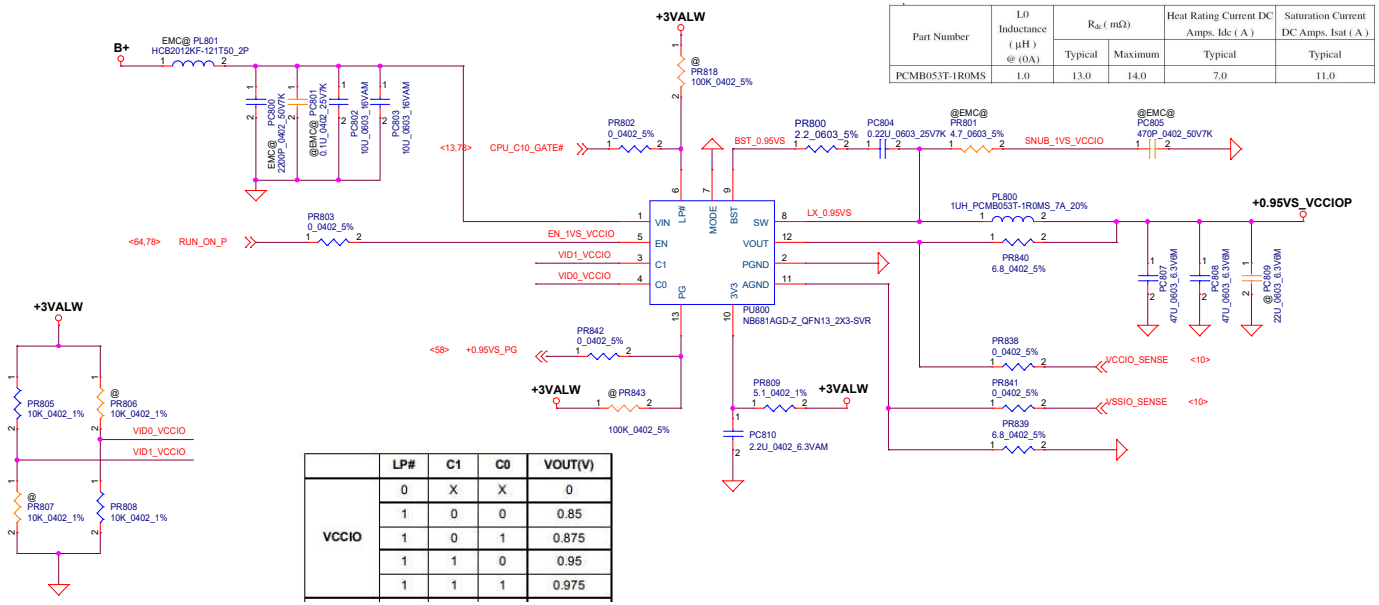
Date: Friday, November 22, 2019 | Sheet 86 of 100

Vin=9~13.5V

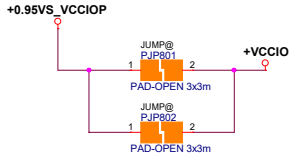
SH00000NW00
Package: 4.9 x 5.2 x 3.0

Part Number	L0 Inductance (μH) @ (0A)	R_{dc} (mΩ) Typical	R_{dc} (mΩ) Maximum	Heat Rating Current DC Amps. Idc (A) Typical	Saturation Current DC Amps. Isat (A) Typical
PCMB053T-1R0MS	1.0	13.0	14.0	7.0	11.0

+0.95VS_VCCIOP
0.95V +/-5%
TDC 4.48A
Peak Current 6.4A
OCP Current 7.65A Fix by IC
Freq 750k Hz



	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975



PWR Plane Regulator_VCCIO(35.37), Support component(35.38)

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

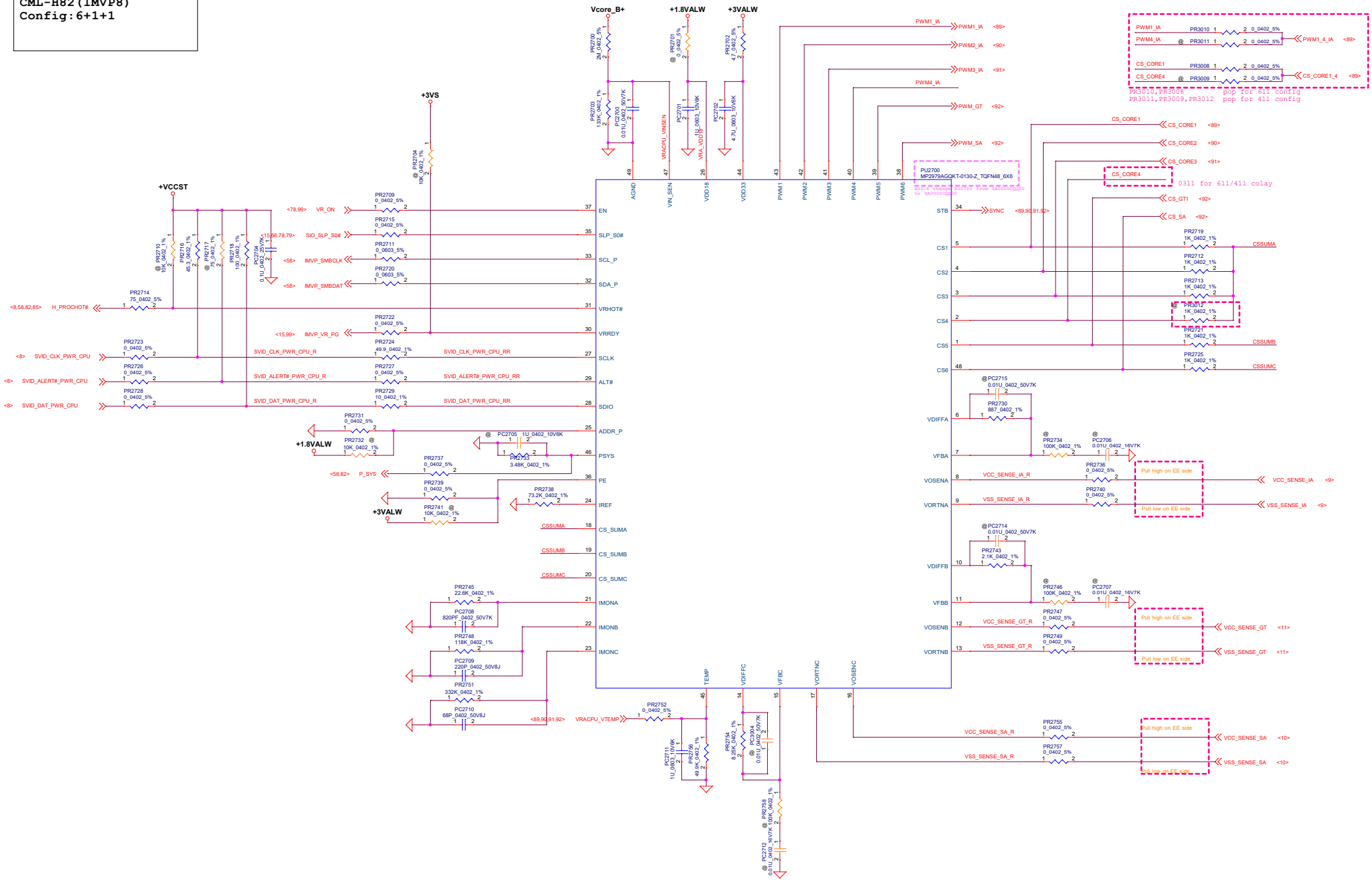
Compal Electronics, Inc.

Title: **P087-PWR_VCCIO(NB681A)**

Size | Document Number: **LA-H331P** | Rev: 0.1(X00)

Date: Friday, November 22, 2019 | Sheet 87 of 100

CML-H82(IMVP8)
Config:6+1+1



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CPU control PWM IC(36.1), Support component(36.3)

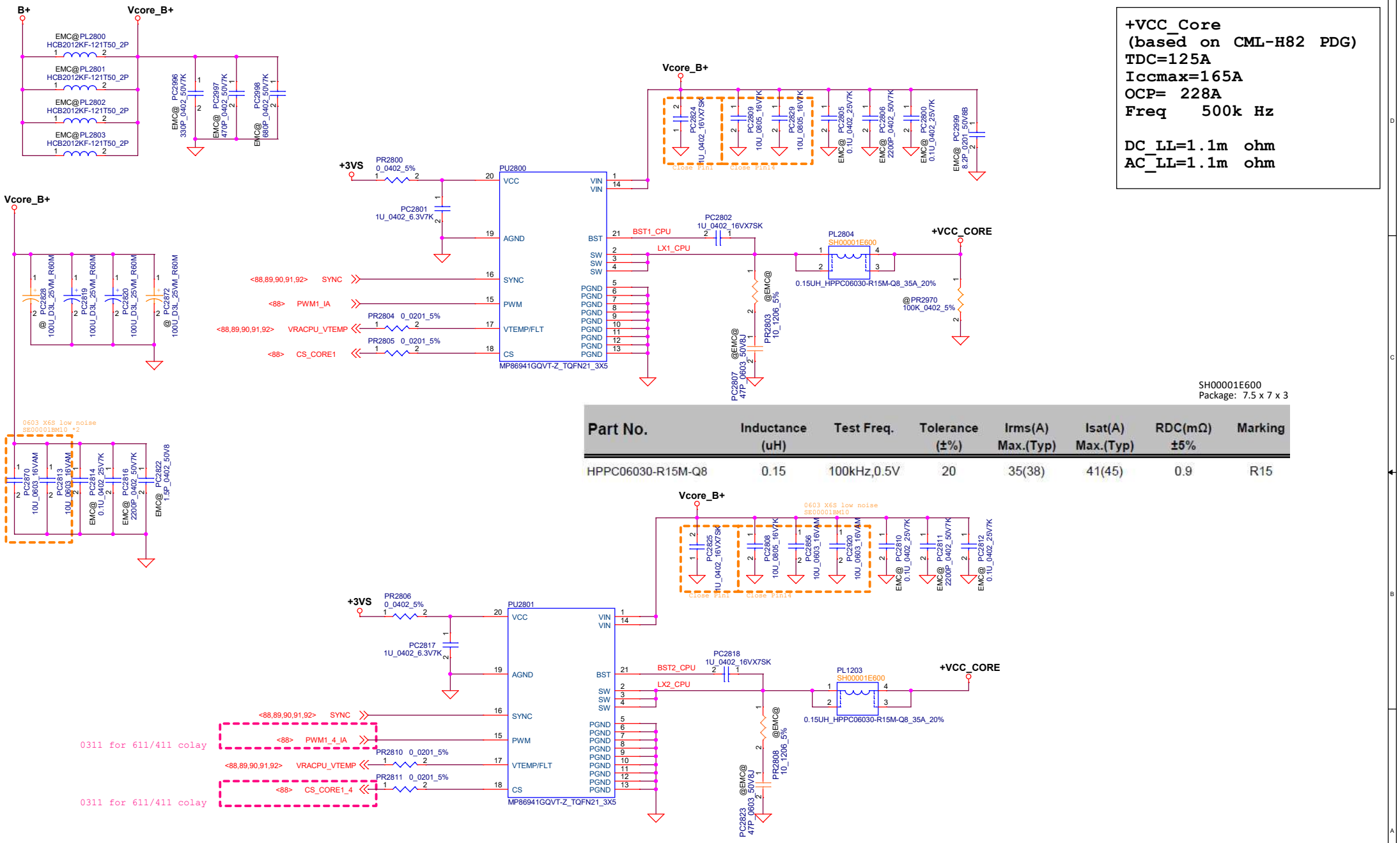
Compal Electronics, Inc.

Title: P088-PWR_+VCORE_MP2949

Size: Document Number: LA-H331P

Rev: 0.1(000)

Date: Friday, November 22, 2019 Sheet 88 of 100



SH00001E600
Package: 7.5 x 7 x 3

Part No.	Inductance (uH)	Test Freq.	Tolerance (±%)	Irms(A) Max.(Typ)	Isat(A) Max.(Typ)	RDC(mΩ) ±5%	Marking
HPPC06030-R15M-Q8	0.15	100kHz,0.5V	20	35(38)	41(45)	0.9	R15

CPU Drivers(36.2), Support component(36.3)

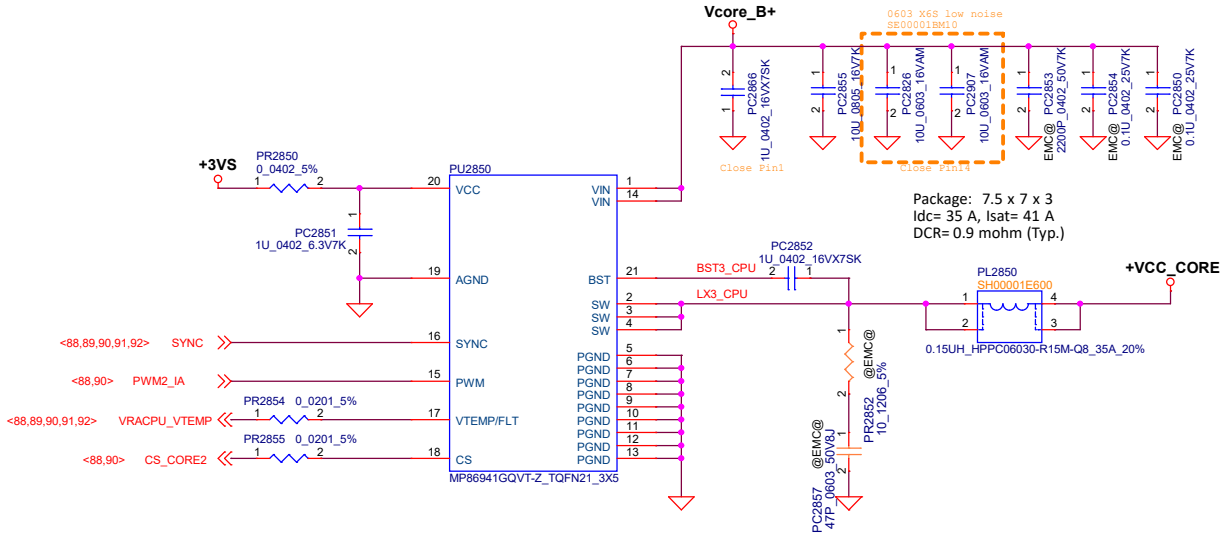
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

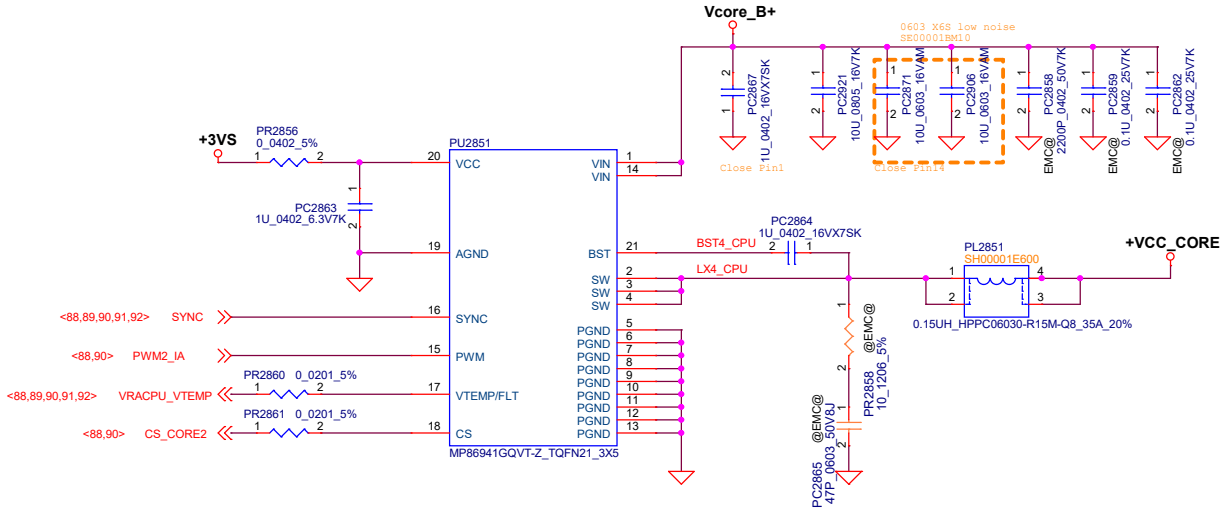
Compal Electronics, Inc.

Title: P089-PWR +VCC_CORE Phase1&2

Size | Document Number: LA-H331P | Rev: 0.1(X00)

Date: Friday, November 22, 2019 | Sheet 89 of 100





CPU Drivers(36.2), Support component(36.3)

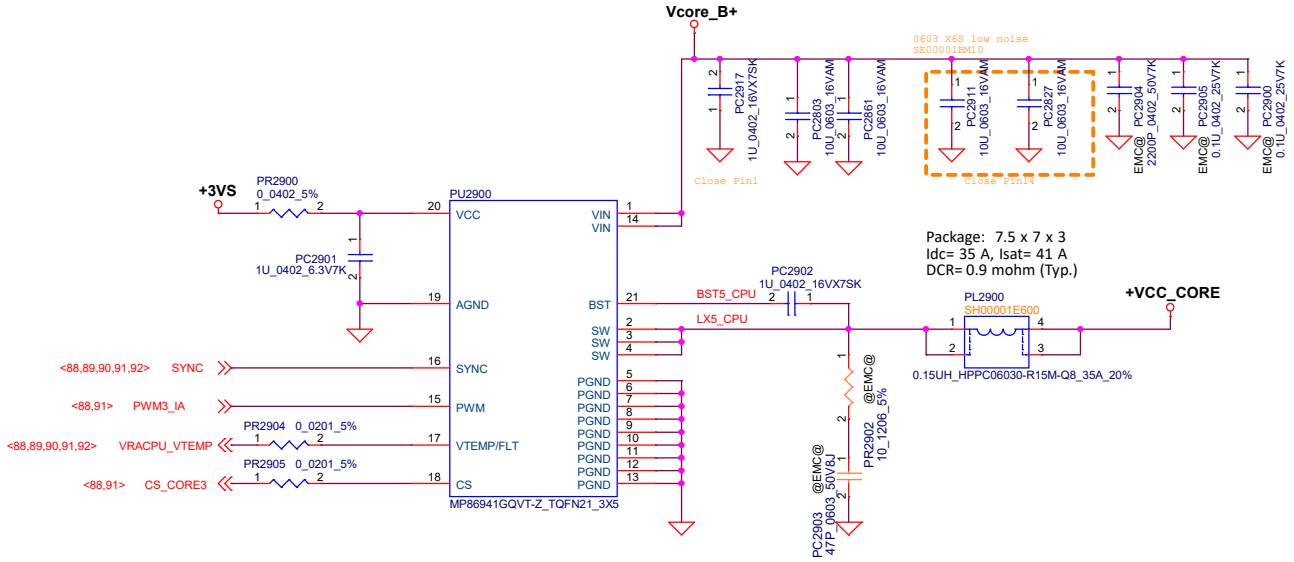
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

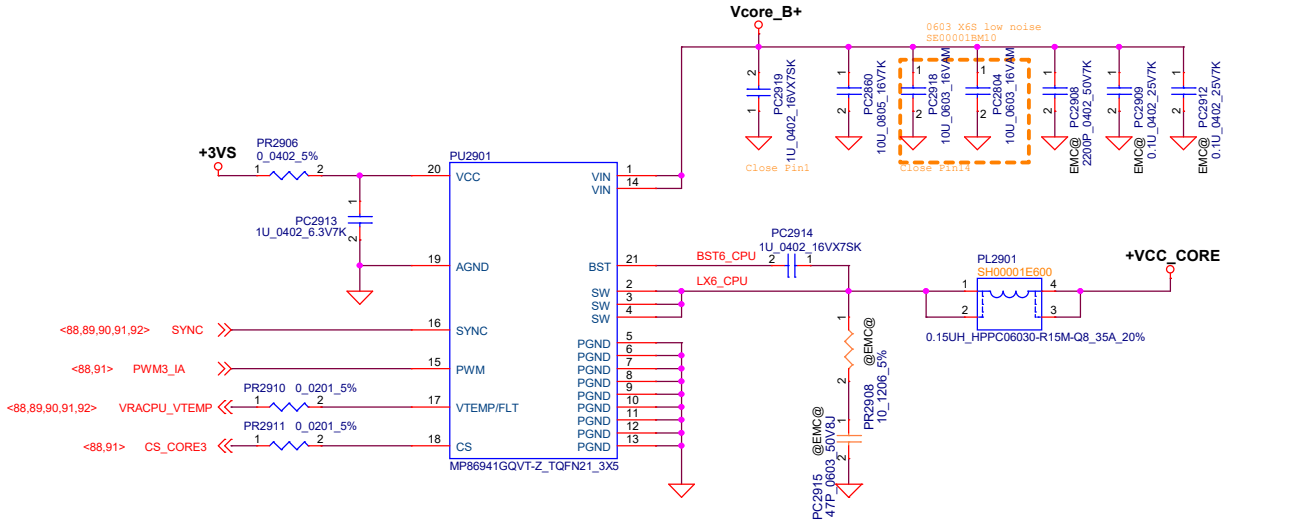
Compal Electronics, Inc.

Title: P090-PWR +VCC_CORE Phase3&4

Size | Document Number: LA-H331P | Rev: 0.1(100)

Date: Friday, November 22, 2019 | Sheet 90 of 100





CPU Drivers(36.2), Support component(36.3)

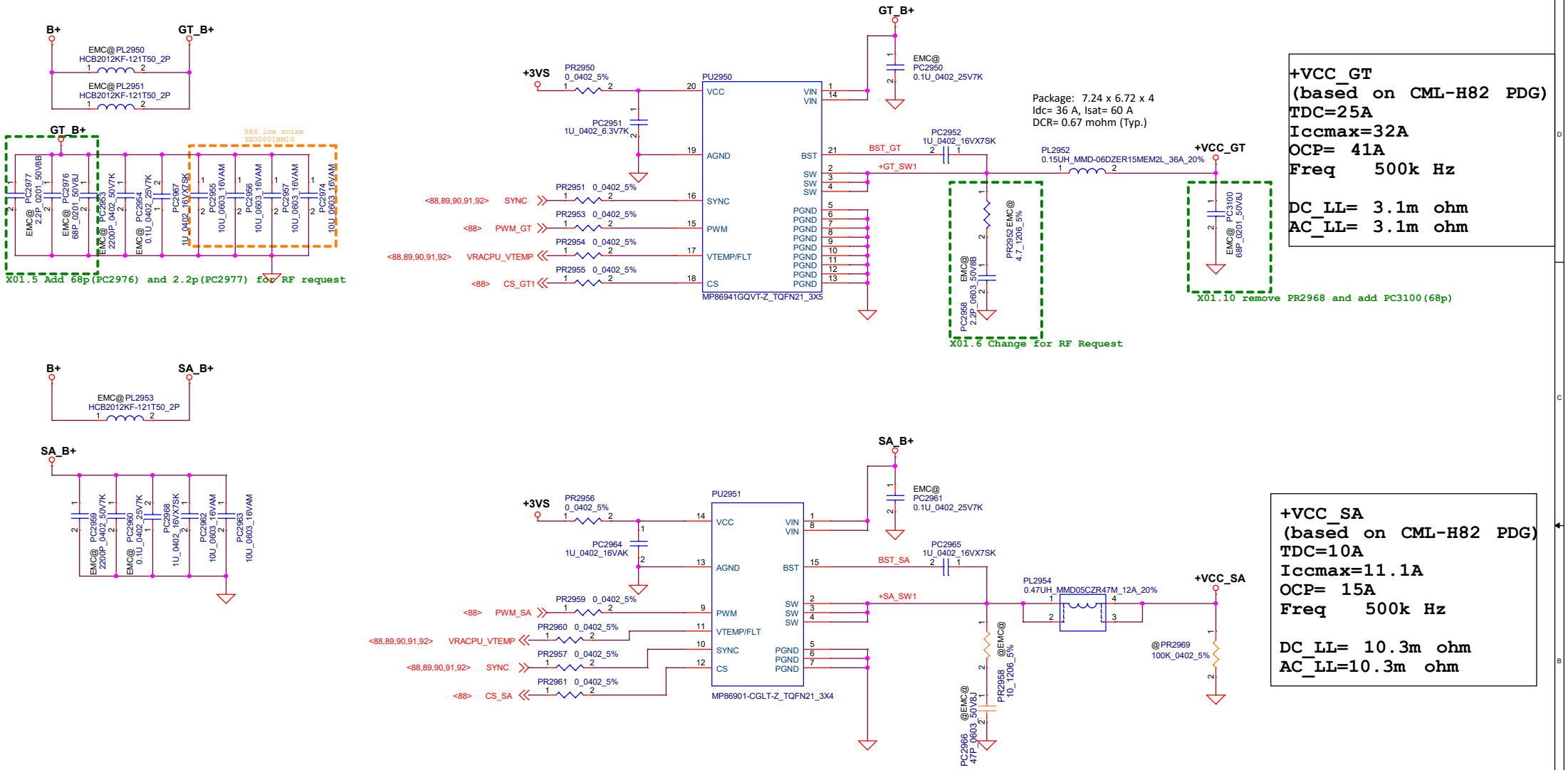
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: P091-PWR +VCC_CORE_Phase3&4

Size | Document Number: LA-H331P | Rev: 0.1(X00)

Date: Friday, November 22, 2019 | Sheet 91 of 100



SH000015M00
Package: 5.7 x 5.4 x 3.0

PART NUMBER	INDUCTANCE Lo(μH)±20% @0A	R_{dc} (mΩ) ±5%	HEAT RATING CURRENT(Idc) DC AMPS[1]	SATURATION CURRENT(Isat) DC AMPS[2]
MMD-05CZ-R47MEV1L	0.47	6.2	12.2	16

CPU Drivers(36.2), Support component(36.3)

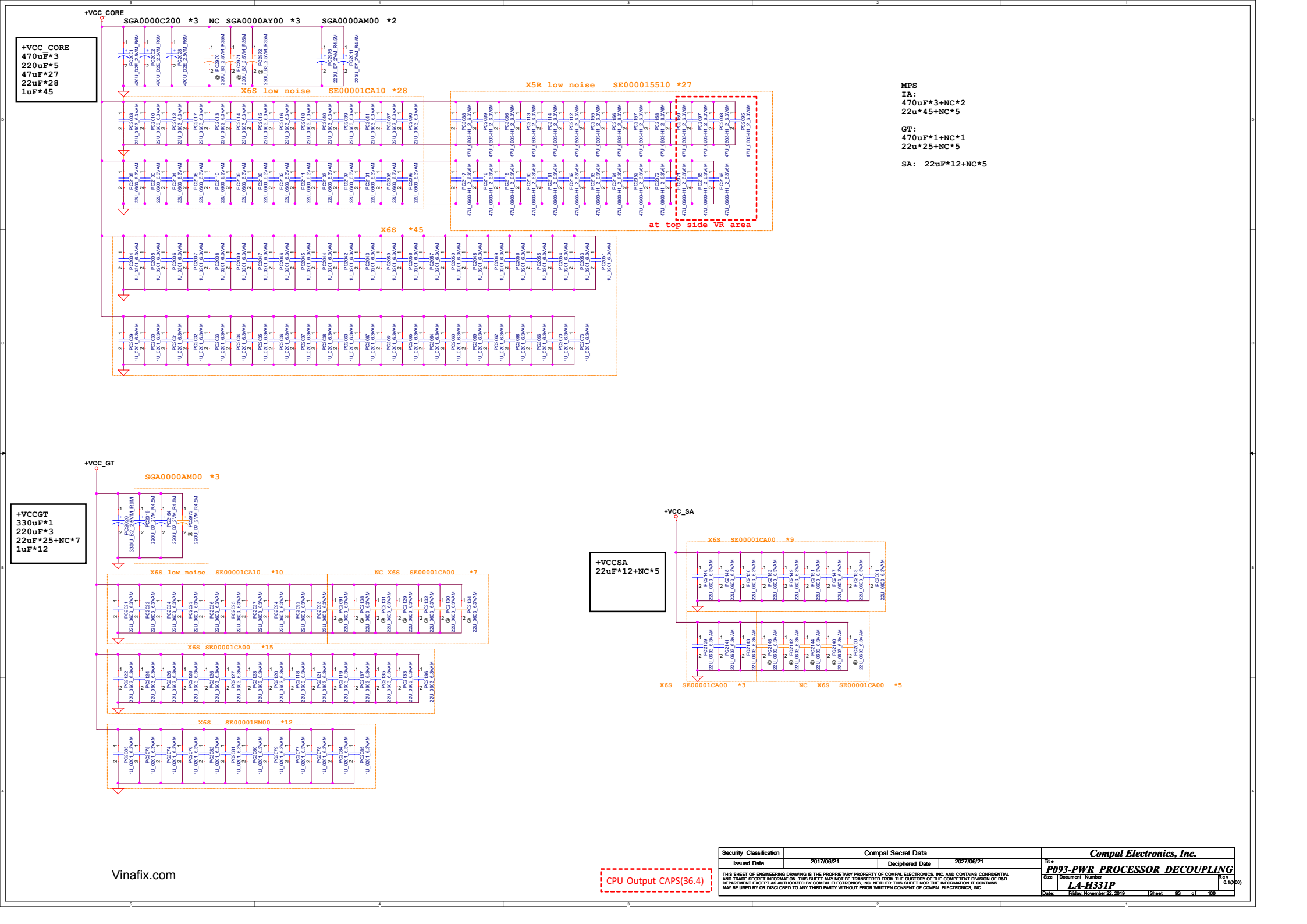
Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: P092-PWR +VCC_GT/+VCC_SA

Size | Document Number: LA-H331P | Rev: 0.1(X00)

Date: Friday, November 22, 2019 | Sheet 92 of 100



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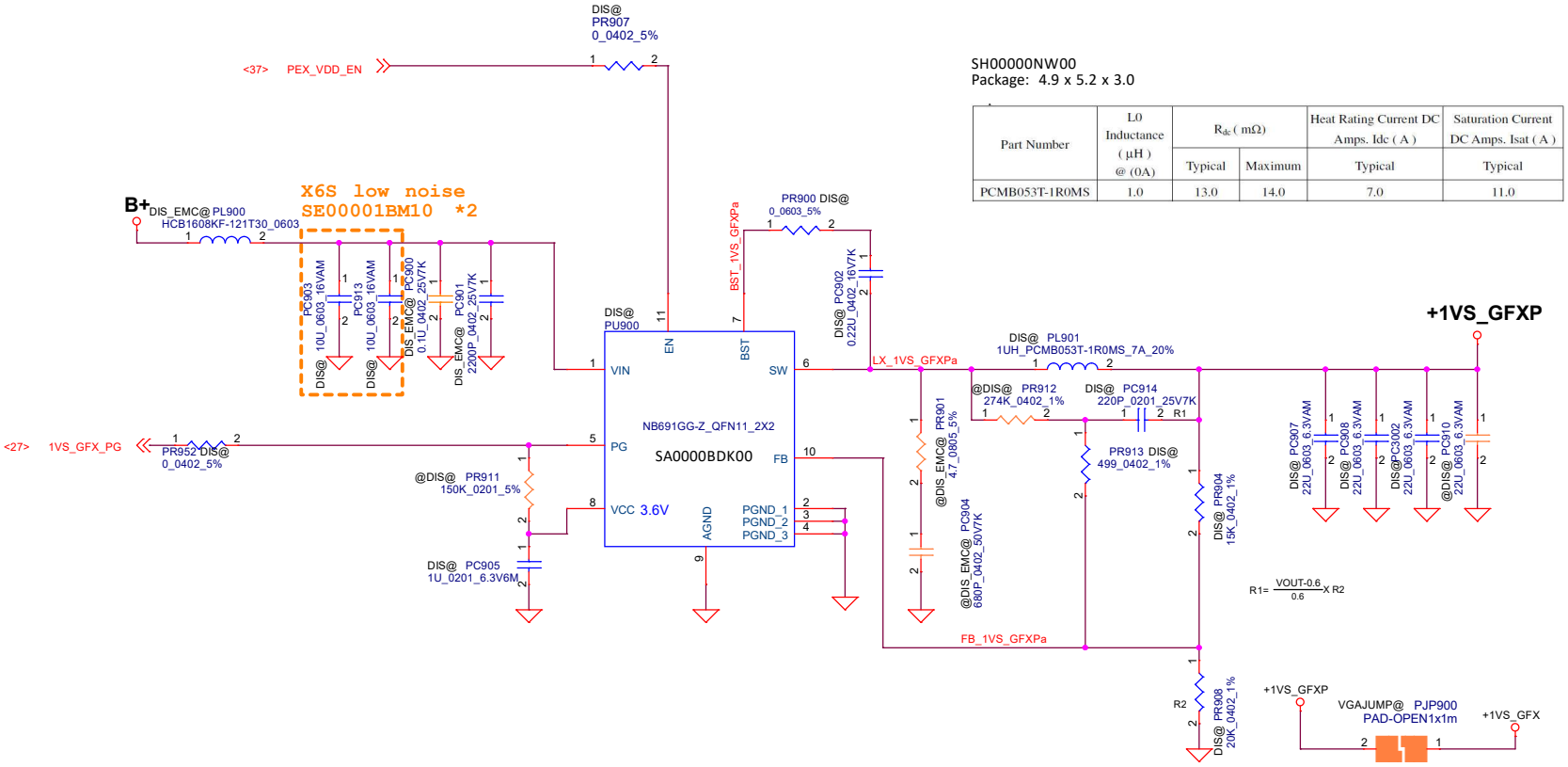
CPU Output CAPS(36.4)

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.	
Title	P093-PWR PROCESSOR DECOUPLING
Size / Document Number	LA-H331P
Rev	0.1(000)
Date: Friday, November 22, 2019	Sheet 93 of 100

for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU

+1.0VSP/1.05VSP
1.05V +/-5% (TBD)
TDC 1.6A
Peak Current 1.6A
OCP current 7.5A(typ.)
Freq 750k Hz



Vinafix.com

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.

Title: P094-PWR_+1VS_GFX(NB691GG-Z)

Size: | Document Number: LA-H331P | Rev: 0.1(X00)

Date: Friday, November 22, 2019 | Sheet 94 of 100

EN :H>0.8V ; L<0.4V

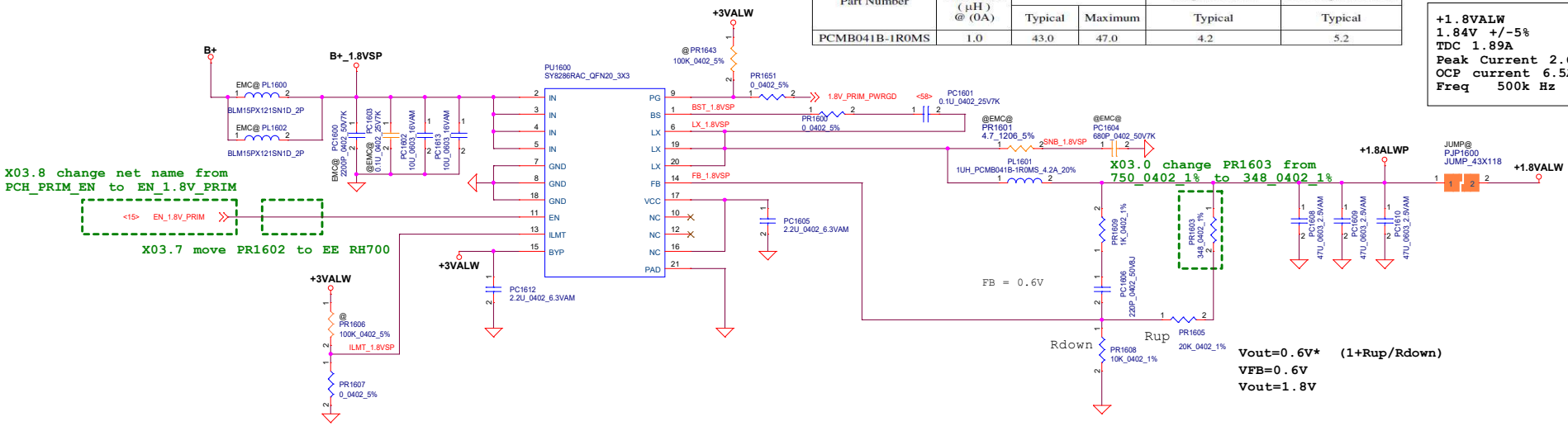
EN pin don't floating

The current limit is set to 6.5A, 9.5A or 12.5A when this pin is pull low, floating or pull high

SH00000PB00
Package: 4.4 x 4.2 x 1.0

Part Number	L0 Inductance (μH) @ (0A)	R_{dc} (mΩ)		Heat Rating Current DC Amps. Idc (A)	Saturation Current DC Amps. Isat (A)
		Typical	Maximum	Typical	Typical
PCMB041B-1R0MS	1.0	43.0	47.0	4.2	5.2

+1.8VALW
1.84V +/-5%
TDC 1.89A
Peak Current 2.68A
OCP current 6.5A(fix)
Freq 500k Hz



Vinafix.com

PWR Plane Regulator_1.8V(35.13), Support component(35.14)

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P095-PWR +1.8ALWP(SY8286RAC)

Size	Document Number	Rev
C	LA-H331P	0.1(000)

Date: Friday, November 22, 2019 Sheet 95 of 100

for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU

1.35VS_VGAP
1.25V +/-5% (N19P-Q1 GDDR6)
1.2V +/-5% (N18P-G62 GDDR6)

TDC=16.7A
Ipeak=33.2A
OCP=47A
Freq=500kHz

X01.15 change PU700 from SA0000CVF10 to SA0000CVF20

PSI: 1.2V full CCM
0.9V auto phase
0.6V one phase CCM/DCM

0.897v

X03.11 add FB_PW_CTL net name

X03.10 move some conponment to EE page

SH00001GX00
SH00001G400

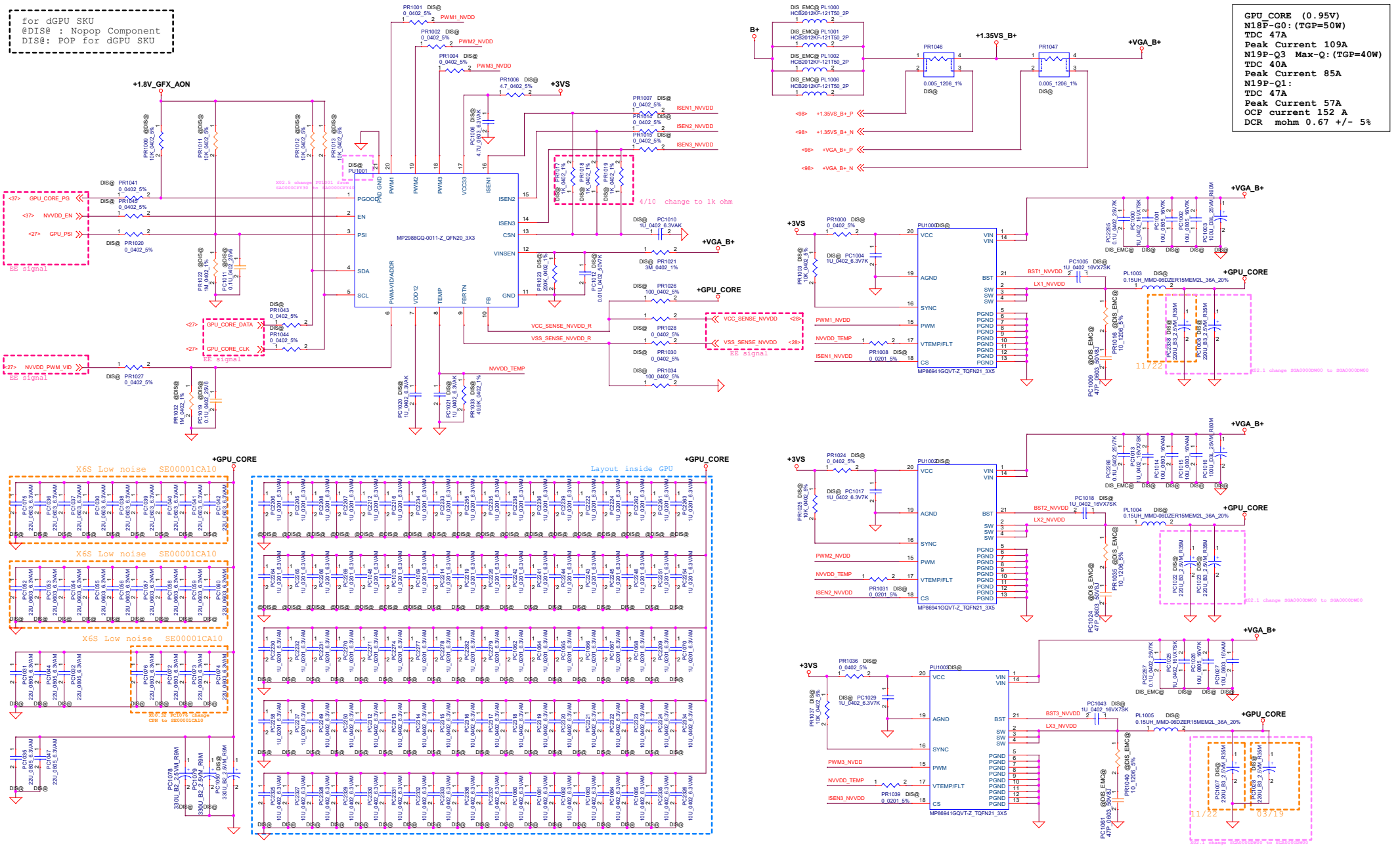
VRAM Control PWM IC(43.5), Support component(43.6)

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title	P096-PWR +1.35VRAM(MP2988)		
Size	Document Number		Rev
	LA-H331P		0.1(X00)
Date:	Friday, November 22, 2019	Sheet	96 of 100

for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU

GPU_CORE (0.95V)
N18P-G0:(TGP=50W)
TDC 47A
Peak Current 109A
N19P-Q3 Max-Q:(TGP=40W)
TDC 40A
Peak Current 85A
N19P-Q1:
TDC 47A
Peak Current 57A
OCP current 152 A
DCR mohm 0.67 +/- 5%



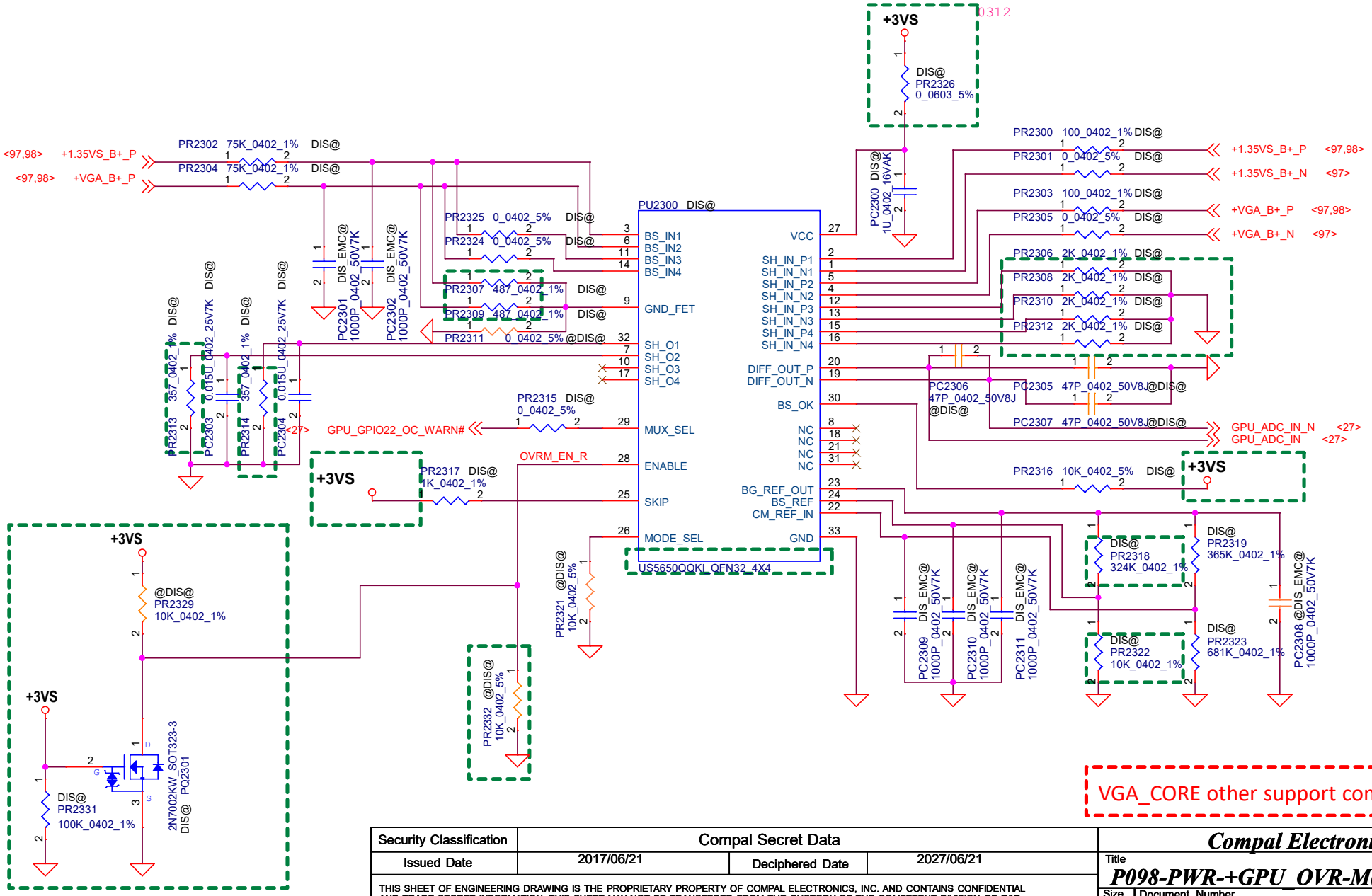
GPU_CORE
330uF*3
220uF*5
22uF*30
10uF*34
1uF*56 (15NC)

SH00001TX00
Package: 6.8 x 6.4 x 4
Idc= 36 A, Isat= 60 A
DCR= 0.67 mohm (Typ.)

Part number	Inductance ±20%@0A (μH)	Rdc(mΩ) ±5%	Heat rating current (Idc)¹ DC amps (A)	Saturation current (Isat)² DC amps (A)	Rs @1Mhz (Ω)Max
MMD-06DZER15MEM2L	0.15	0.67	36.0	60.0	0.034

VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

Compal Electronics, Inc.
Title: P097-PWR-+GPU_CORE(MP2988)
Size: Document Number: LA-H331P
Rev: 0.1(000)
Date: Friday, November 22, 2019 Sheet 97 of 100



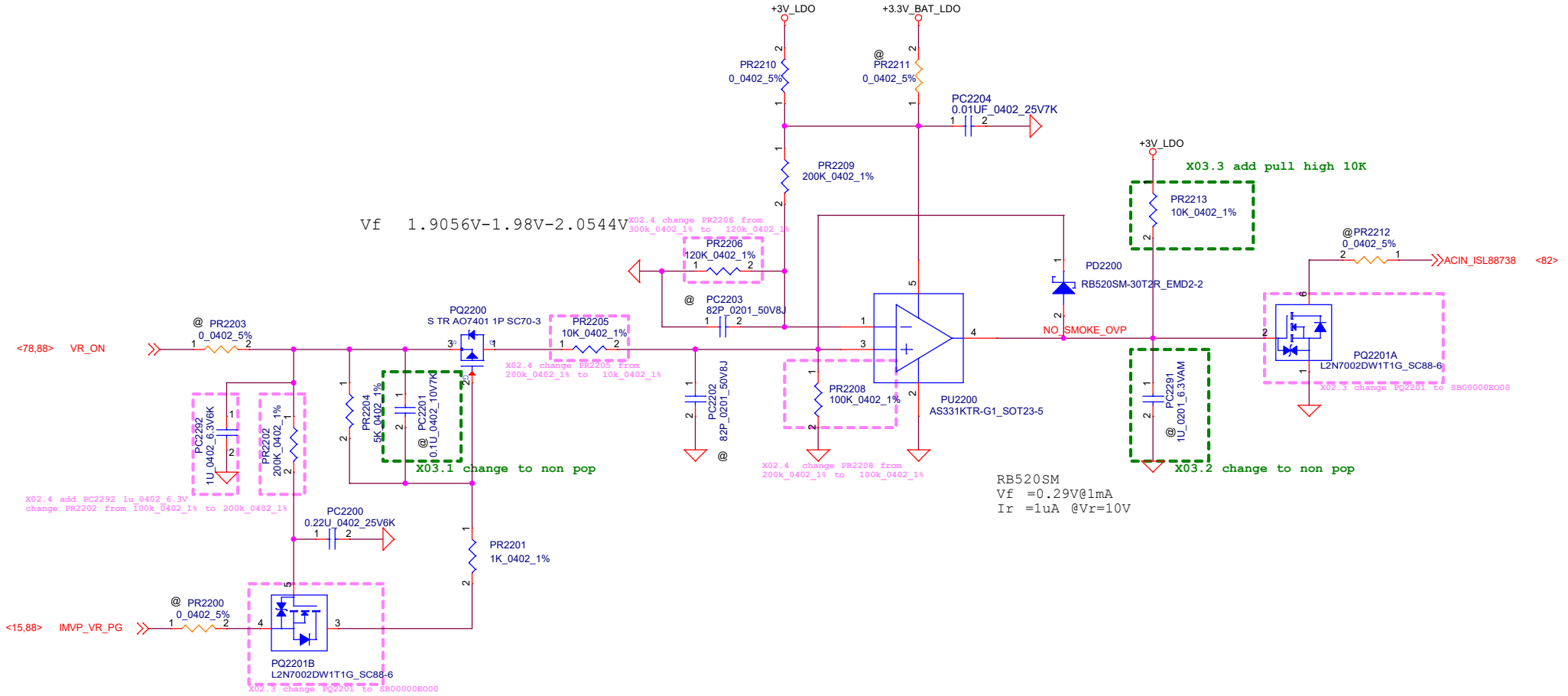
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P098-PWR-+GPU_OVR-M(US5650QQKI)**

Size	Document Number	Rev
	LA-H331P	0.1(X00)

Date: Friday, November 22, 2019 | Sheet 98 of 100



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

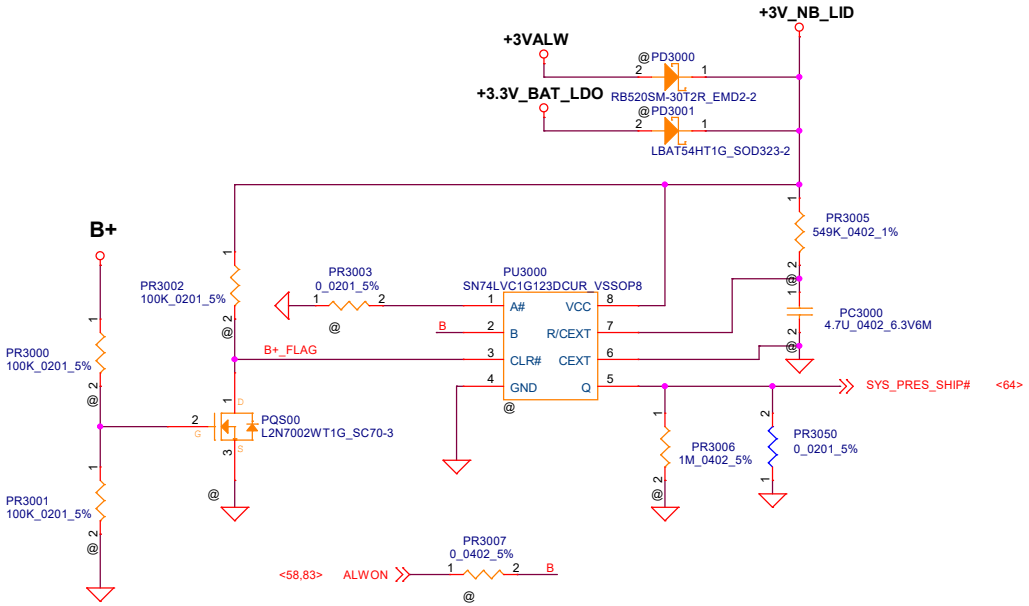
Compal Electronics, Inc.

Title: **P099-PWR_SMOKELESS**

Size	Document Number	Rev
	LA-H331P	0.1(X00)

Date: Friday, November 22, 2019 | Sheet 99 of 100

PD3001
mail source: SCS00008A00
second source: SCS00003M00



FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.

Title: PWR_SHIP_MODE

Size | Document Number: LA-G172P | Rev: 0.1(M00)

Date: Friday, November 22, 2019 | Sheet 100 of 100