MS-7680 Ver: 2.3 m-ATX : 245 X 215mm

三個BOM:

1.H67 Full Spec(全固)
2.H61 Full Spec(全固)
3.H61 common Spec(半固)

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(H61,Co-lay H67)

OnBoard Chipset:

HD Audio Codec:RTL887 Co-lay 892
LAN:RTL 8111E 10/100/1000 , Co-lay 8105E 10/100
SIO:FIN71869AD
Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2
PCI Slot * 1

PWM:

Controller:VRD12 UP1625 3Phase
CPU+GPU: UP6282 MOSFET Driver
CPU VTT: IP6103
CPU SA : OP+MOS
DDR: UP6103
PCH: UP6103

ACPI:

UPI

Other:

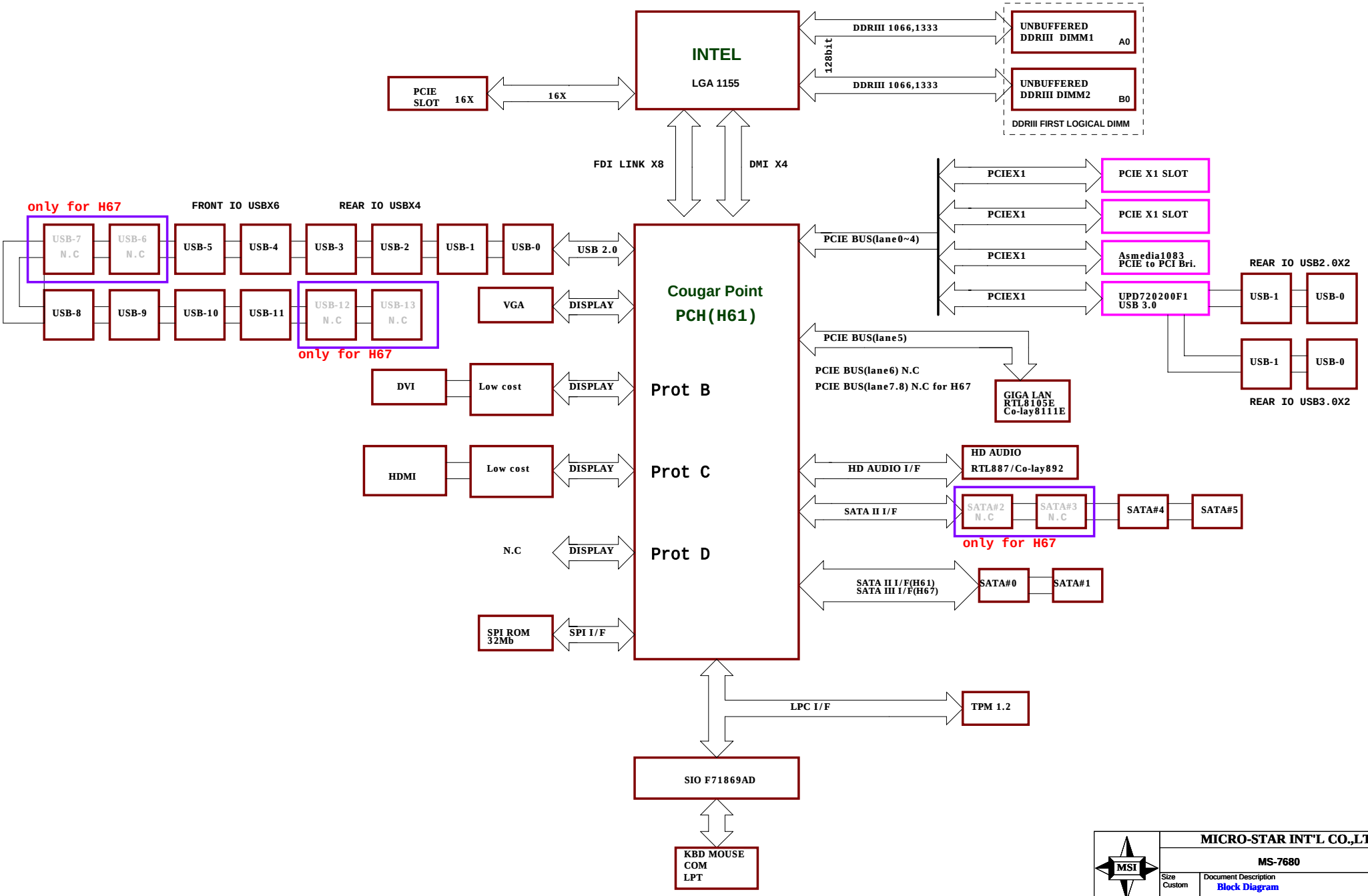
SATA3.0 x2 + SATA2.0 x4 (PCH)
USB2.0 RearX4 Front x6
USB3.0 RearX2
D-SUB/DVI/HDMI *1
TPM Header *1
COM Header *1
LPT Header *1
on BOARD BUZZER

MICRO-STAR INT'L CO.,LTD

MS-7680

Size	Document Description	Rev
Custom	Cover Sheet	2.3

Date: Thursday, June 02, 2011 Sheet 1 of 39

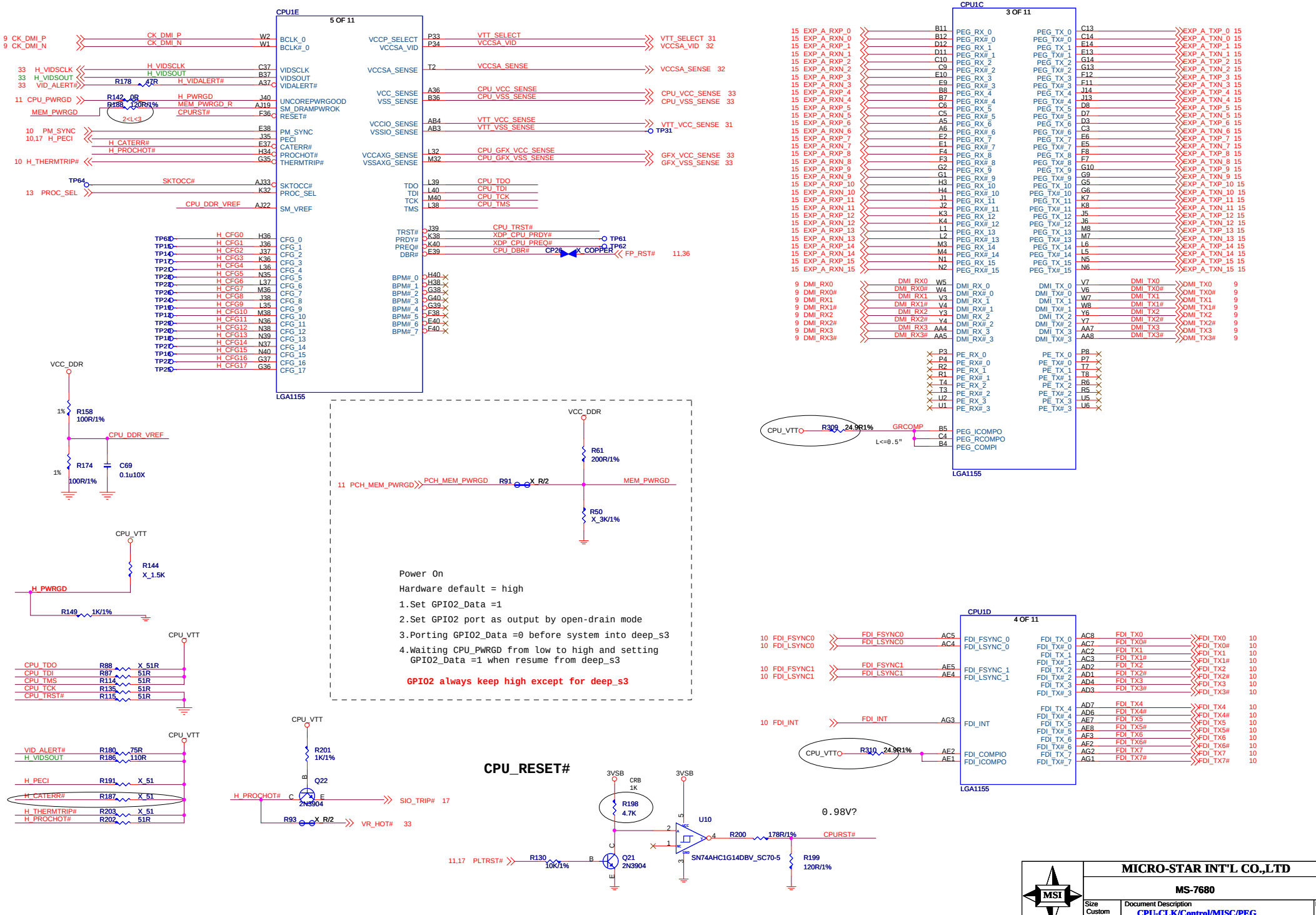


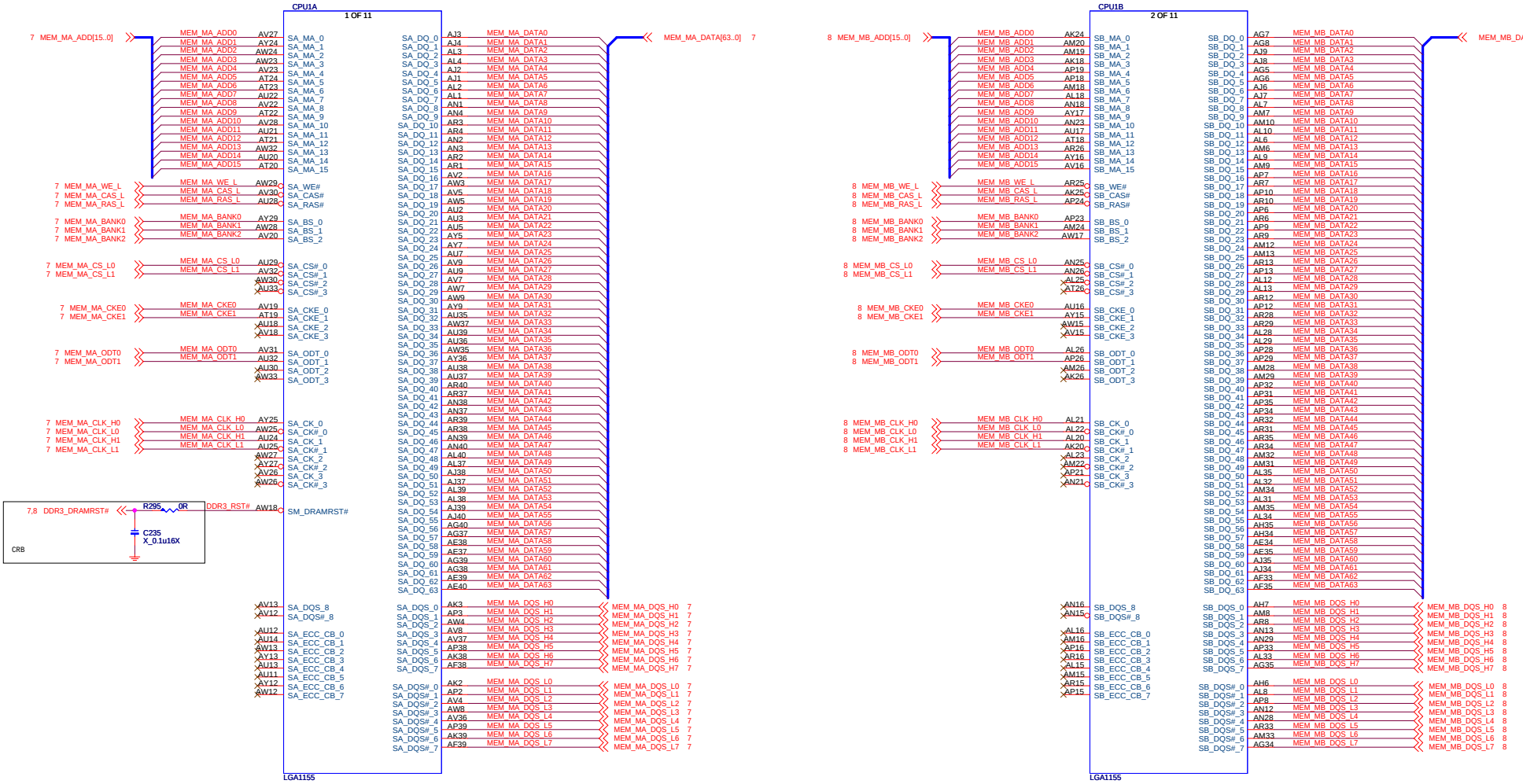
MICRO-STAR INT'L CO.,LTD

MS-7680

Size	Document Description	Rev
Custom	Block Diagram	2.3

Date: Thursday, June 02, 2011 Sheet 2 of 39


CPU1E
5 OF 11
LGA1155
CPU1C
3 OF 11
LGA1155
CPU1D
4 OF 11
LGA1155
CK_DMI_P
CK_DMI_N
H_VIDSCLK
H_VIDSOUT
VID_ALERT#
H_VIDALERT#
CPU_PWRGD
H_PWRGD
MEM_PWRGD
MEM_PWRGD_R
CPURST#
PM_SYNC
H_PECI
H_CATERR#
H_PROCHOT#
H_THERMTRIP#
SKTOCC#
PROC_SEL
CPU_DDR_VREF
VTT_SELECT
VCCSA_VID
VCCSA_SENSE
CPU_VCC_SENSE
CPU_VSS_SENSE
VTT_VCC_SENSE
CPU_GFX_VCC_SENSE
CPU_GFX_VSS_SENSE
CPU_TDO
CPU_TDI
CPU_TCK
CPU_TMS
CPU_TRST#
XDP_CPU_PRDY#
XDP_CPU_PREQ#
CPU_DBR#
FP_RST#
PCH_MEM_PWRGD
VCC_DDR
CPU_VTT
R158 100R/1%
R174 100R/1%
C69 0.1u10X
R144 X_1.5K
R149 1K/1%
R61 200R/1%
R50 X_3K/1%
R91 X_R/2
R309 24.9R1%
R310 24.9R1%
GRCOMP
L<=0.5"
PEG_ICOMPO
PEG_RCOMPO
PEG_COMPI
FDI_FSYNC0
FDI_LSYNC0
FDI_FSYNC1
FDI_LSYNC1
FDI_INT
FDI_COMPIO
FDI_ICOMPO
CPU_TDO R88 X_51R
CPU_TDI R87 51R
CPU_TMS R114 51R
CPU_TCK R135 51R
CPU_TRST# R115 51R
VID_ALERT# R180 75R
H_VIDSOUT R186 110R
H_PECI R191 X_51
H_CATERR# R187 X_51
H_THERMTRIP# R203 X_51
H_PROCHOT# R202 51R
R201 1K/1%
Q22
2N3904
R93 X_R/2
SIO_TRIP# 17
VR_HOT# 33
Power On
Hardware default = high
1.Set GPIO2_Data =1
2.Set GPIO2 port as output by open-drain mode
3.Porting GPIO2_Data =0 before system into deep_s3
4.Waiting CPU_PWRGD from low to high and setting GPIO2_Data =1 when resume from deep_s3
GPIO2 always keep high except for deep_s3
CPU_RESET#
3VSB
R198 4.7K
U10
SN74AHC1G14DBV_SC70-5
R200 178R/1%
CPURST#
R130 10K/1%
Q21 2N3904
R199 120R/1%
PLTRST#
0.98V?
MICRO-STAR INT'L CO.,LTD
MS-7680
Size Custom
Document Description
CPU-CLK/Control/MISC/PEG
Rev 2.3
Date: Friday, June 17, 2011
Sheet 3 of 39



MICRO-STAR INT'L CO.,LTD

MS-7680

Size	Document Description	Rev
Custom	CPU-Memory	2.3

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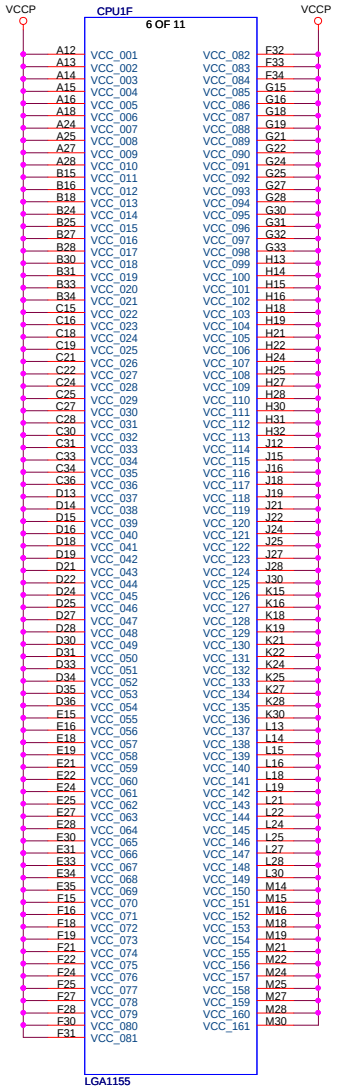
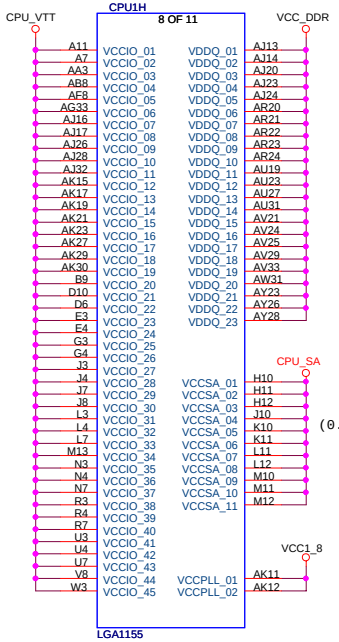
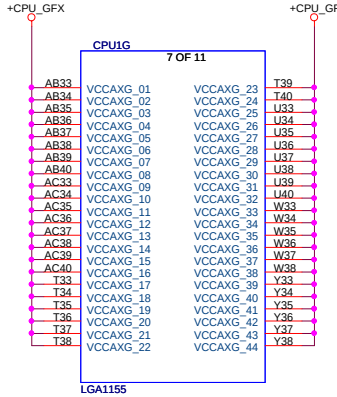
(1.05V / 1.00V)



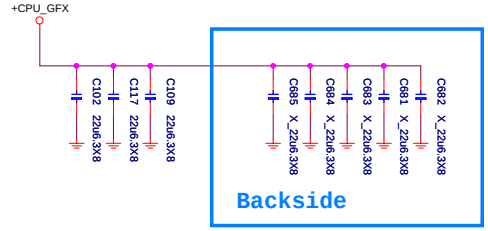


(0.925V / 0.85V)



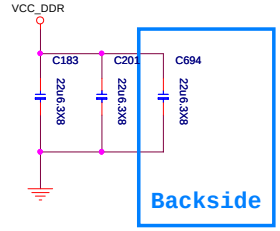
VCCP: 112A
CPU_VTT: 8.2A
CPU_SA: 8.8A
VCC_DDR: 4.5A
VCC1_8: 1.6A

+CPU_GFX Decoupling

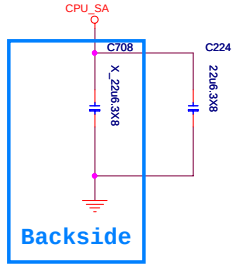


CPU SOCKET CAVITY CAPS

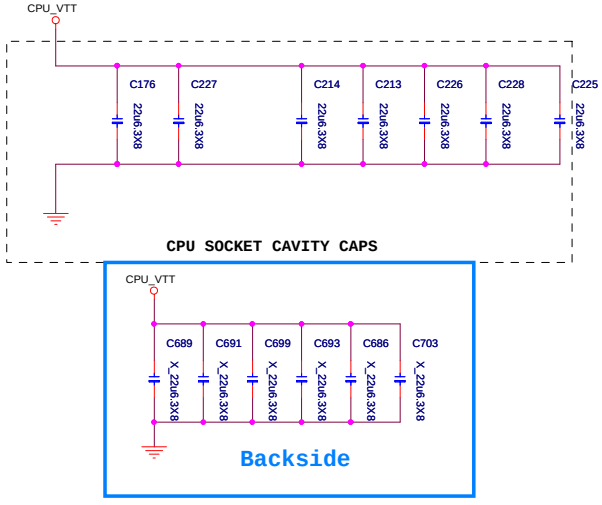
+1.5V_DDR3-Decoupling



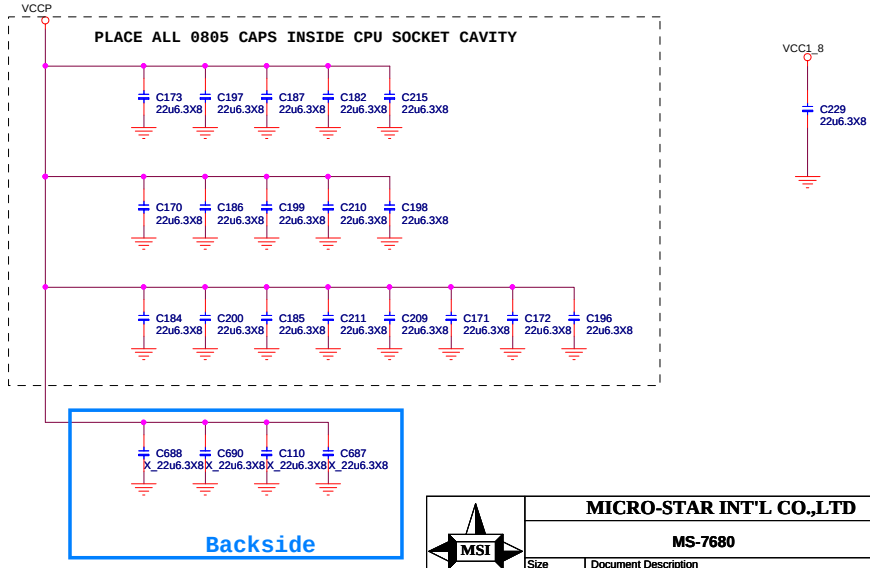
CPU SOCKET CAVITY CAPS



+CPU_VTT Decoupling



+CPU_VCCP-Decoupling



MICRO-STAR INT'L CO.,LTD

MS-7680

Size	Document Description	Rev
Custom	CPU-Power	2.3

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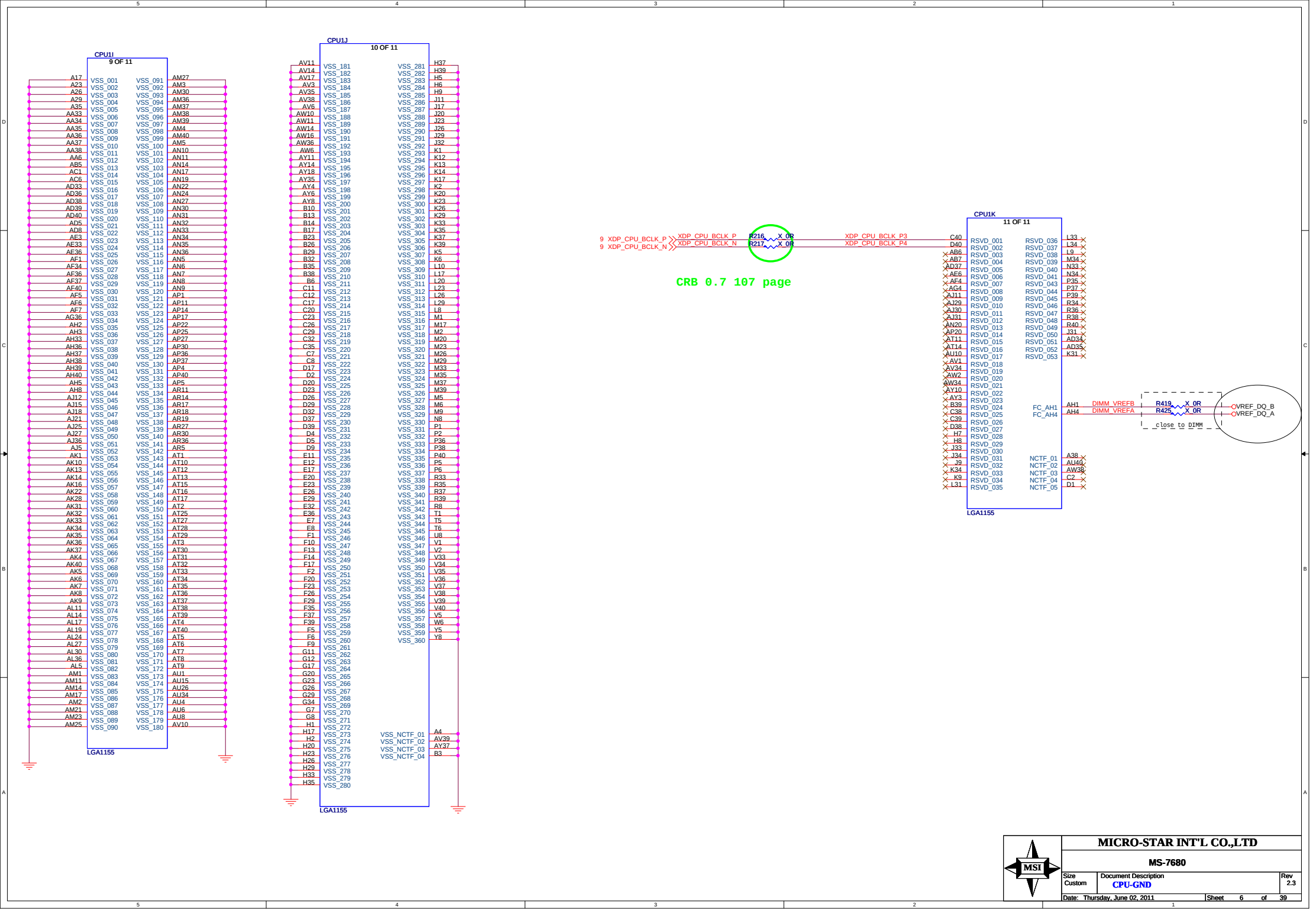


MICRO-STAR INT'L CO.,LTD	
MS-7680	
Size: Custom	Document Description: CPU-GND
Rev: 2.3	
Date: Thursday, June 02, 2011	Sheet 6 of 39

DDRIII DIMM_A0

DDRIII DIMM_A1

A0 B0

Place close to DIMM1

VCC_DDR
C217 2.2u6.3Y
C163 220p25N
C154 2.2u6.3Y
C212 2.2u6.3Y

Place close to DIMM1 with DIMM2

VCC_DDR
C188 0.1u10X

Place close to DIMM2

VCC_DDR
C216 0.1u10X
C152 0.1u10X

UPI VOLTAGE CONSOLE

VREF_CA_A VCC_DDR
VREF_CA_A R270 1K/1%
C161 0.1u10X
R265 1K/1%

UPI VOLTAGE CONSOLE

VREF_DQ_A VCC_DDR
VREF_DQ_A R422 1K/1%
C336 0.1u10X
R423 1K/1%
C179 2.2u6.3Y

EMI

VCC_DDR
C218 X_0.1u16X
C153 X_0.1u16X
C219 X_0.1u16X
C156 X_0.1u16X

4 MEM_MA_DATA[63..0] MEM_MA_DATA[63..0]

VCC_DDR VCC3 VTT_DDR

VCC3
C89 10u6.3X8
C92 0.1u10X

DIMM1

DDR3

MEM_MA_DATA0 3
MEM_MA_DATA1 4
MEM_MA_DATA2 9
MEM_MA_DATA3 10
MEM_MA_DATA4 122
MEM_MA_DATA5 123
MEM_MA_DATA6 128
MEM_MA_DATA7 129
MEM_MA_DATA8 12
MEM_MA_DATA9 13
MEM_MA_DATA10 18
MEM_MA_DATA11 19
MEM_MA_DATA12 131
MEM_MA_DATA13 132
MEM_MA_DATA14 137
MEM_MA_DATA15 138
MEM_MA_DATA16 21
MEM_MA_DATA17 22
MEM_MA_DATA18 27
MEM_MA_DATA19 28
MEM_MA_DATA20 140
MEM_MA_DATA21 141
MEM_MA_DATA22 146
MEM_MA_DATA23 147
MEM_MA_DATA24 30
MEM_MA_DATA25 31
MEM_MA_DATA26 36
MEM_MA_DATA27 37
MEM_MA_DATA28 149
MEM_MA_DATA29 150
MEM_MA_DATA30 155
MEM_MA_DATA31 156
MEM_MA_DATA32 81
MEM_MA_DATA33 82
MEM_MA_DATA34 87
MEM_MA_DATA35 88
MEM_MA_DATA36 200
MEM_MA_DATA37 201
MEM_MA_DATA38 206
MEM_MA_DATA39 207
MEM_MA_DATA40 90
MEM_MA_DATA41 91
MEM_MA_DATA42 96
MEM_MA_DATA43 97
MEM_MA_DATA44 209
MEM_MA_DATA45 210
MEM_MA_DATA46 215
MEM_MA_DATA47 216
MEM_MA_DATA48 99
MEM_MA_DATA49 100
MEM_MA_DATA50 105
MEM_MA_DATA51 106
MEM_MA_DATA52 218
MEM_MA_DATA53 219
MEM_MA_DATA54 224
MEM_MA_DATA55 225
MEM_MA_DATA56 108
MEM_MA_DATA57 109
MEM_MA_DATA58 114
MEM_MA_DATA59 115
MEM_MA_DATA60 227
MEM_MA_DATA61 228
MEM_MA_DATA62 233
MEM_MA_DATA63 234

MEM_MA_ADD[15..0] 4

MEM_MA_ADD0 188
MEM_MA_ADD1 181
MEM_MA_ADD2 61
MEM_MA_ADD3 180
MEM_MA_ADD4 59
MEM_MA_ADD5 58
MEM_MA_ADD6 178
MEM_MA_ADD7 56
MEM_MA_ADD8 177
MEM_MA_ADD9 175
MEM_MA_ADD10 70
MEM_MA_ADD11 55
MEM_MA_ADD12 174
MEM_MA_ADD13 196
MEM_MA_ADD14 172
MEM_MA_ADD15 171

CB0 39
CB1 40
CB2 45
CB3 46
CB4 158
CB5 159
CB6 164
CB7 165

MEM_MA_DQS_H0 7
MEM_MA_DQS_L0 6
MEM_MA_DQS_H1 16
MEM_MA_DQS_L1 15
MEM_MA_DQS_H2 25
MEM_MA_DQS_L2 24
MEM_MA_DQS_H3 34
MEM_MA_DQS_L3 33
MEM_MA_DQS_H4 85
MEM_MA_DQS_L4 84
MEM_MA_DQS_H5 94
MEM_MA_DQS_L5 93
MEM_MA_DQS_H6 103
MEM_MA_DQS_L6 102
MEM_MA_DQS_H7 112
MEM_MA_DQS_L7 111
DQS8 43
DQS8# 42

MEM_MA_DQS_H0 4
MEM_MA_DQS_L0 4
MEM_MA_DQS_H1 4
MEM_MA_DQS_L1 4
MEM_MA_DQS_H2 4
MEM_MA_DQS_L2 4
MEM_MA_DQS_H3 4
MEM_MA_DQS_L3 4
MEM_MA_DQS_H4 4
MEM_MA_DQS_L4 4
MEM_MA_DQS_H5 4
MEM_MA_DQS_L5 4
MEM_MA_DQS_H6 4
MEM_MA_DQS_L6 4
MEM_MA_DQS_H7 4
MEM_MA_DQS_L7 4

DM0/DQS9 125
NC/DQS9# 126
DM1/DQS10 134
NC/DQS10# 135
DM2/DQS11 143
NC/DQS11# 144
DM3/DQS12 152
NC/DQS12# 153
DM4/DQS13 203
NC/DQS13# 204
DM5/DQS14 212
NC/DQS14# 213
DM6/DQS15 221
NC/DQS15# 222
DM7/DQS16 230
NC/DQS16# 231
DM8/DQS17 161
NC/DQS17# 162

MEM_MA_ODT0 195
MEM_MA_ODT1 77
MEM_MA_CKE0 50
MEM_MA_CKE1 169
MEM_MA_CS_L0 193
MEM_MA_CS_L1 76
MEM_MA_BANK0 71
MEM_MA_BANK1 190
MEM_MA_BANK2 52

MEM_MA_ODT0 4
MEM_MA_ODT1 4
MEM_MA_CKE0 4
MEM_MA_CKE1 4
MEM_MA_CS_L0 4
MEM_MA_CS_L1 4
MEM_MA_BANK0 4
MEM_MA_BANK1 4
MEM_MA_BANK2 4

MEM_MA_WE_L 73
MEM_MA_RAS_L 192
MEM_MA_CAS_L 74
DDR3_DRAMRST# 168

MEM_MA_WE_L 4
MEM_MA_RAS_L 4
MEM_MA_CAS_L 4
DDR3_DRAMRST# 4,8

MEM_MA_CLK_H0 184
MEM_MA_CLK_L0 185
MEM_MA_CLK_H1 63
MEM_MA_CLK_L1 64

MEM_MA_CLK_H0 4
MEM_MA_CLK_L0 4
MEM_MA_CLK_H1 4
MEM_MA_CLK_L1 4

VREF_DQ_A 1
VREF_CA_A 67
SMBCLK_DDR 118
SMBDATA_DDR 238

C174 0.1u10X
C326 0.1u10X

DDRIII-240P_BLACK-RH-8

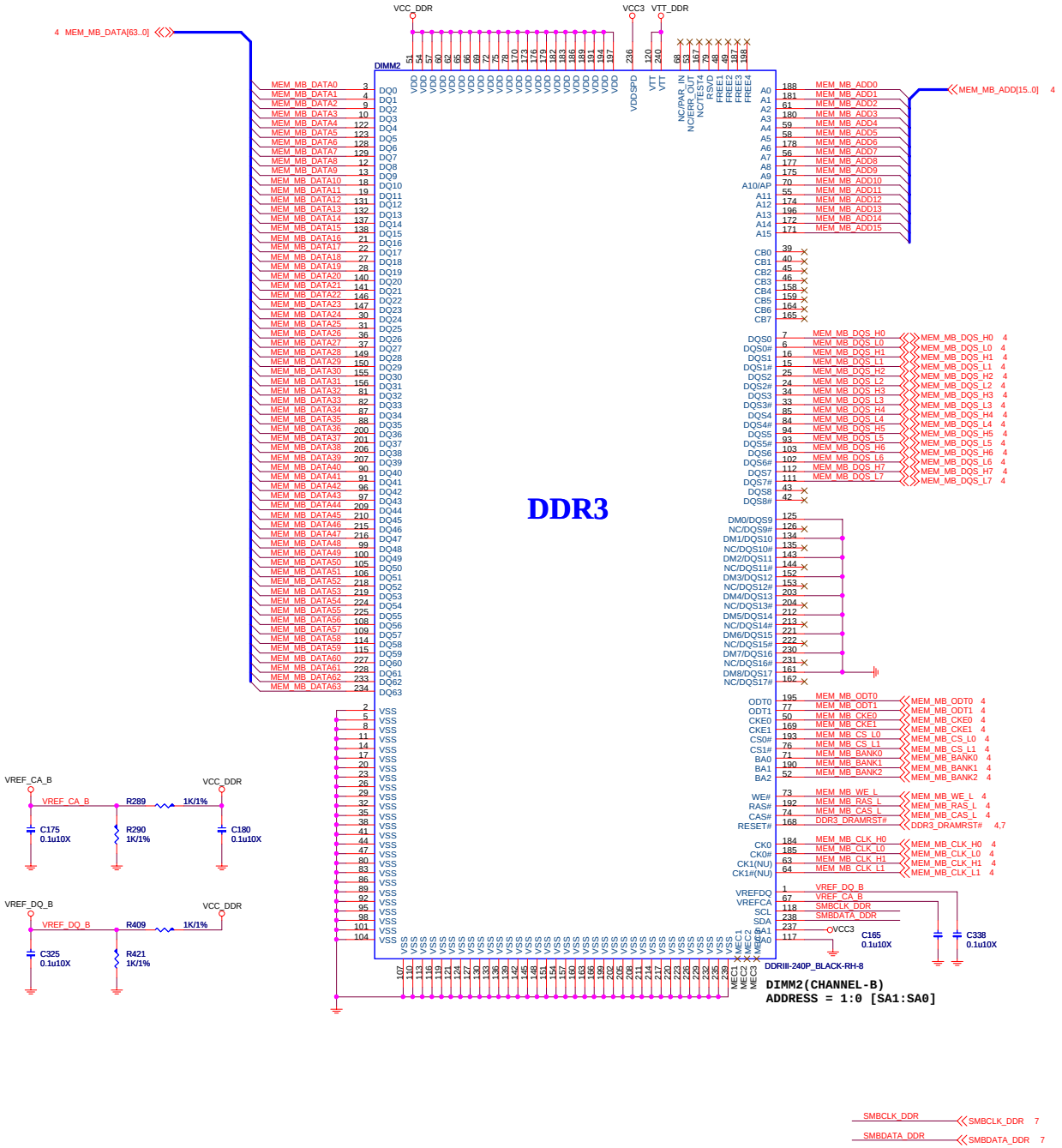
DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

uP6262 use BMA8
PN:I34-6262B09-U33

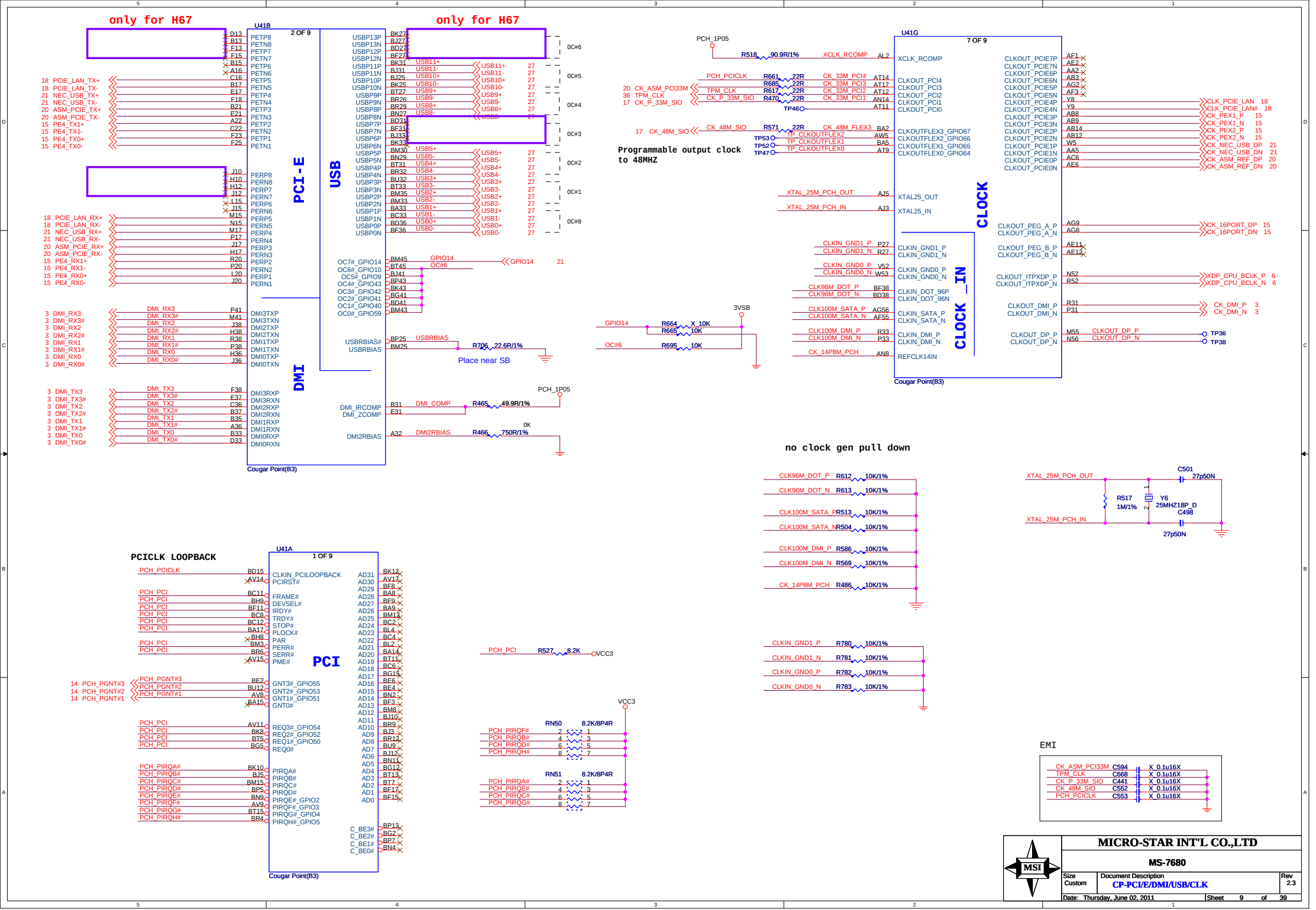
8 SMBCLK_DDR SMBCLK_DDR R159 33R SMBCLK 11,15,29
8 SMBDATA_DDR SMBDATA_DDR R173 33R SMBDATA 11,15,29

MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size: Custom	Document Description: DDR III DIMM 1 / DIMM 2	Rev: 2.3
Date: Thursday, June 02, 2011	Sheet 7 of 39	

DDRIII DIMM_B0



MICRO-STAR INT'L CO.,LTD	
MS-7680	
Size: Custom	Document Description: DDR III DIMM 3 / DIMM 4
Rev: 2.3	
Date: Thursday, June 02, 2011	Sheet 8 of 39


only for H67
only for H67
U41B
2 OF 9
PCI-E
USB
DMI
Cougar Point(B3)
Place near SB
Programmable output clock to 48MHZ
U41G
7 OF 9
CLOCK
CLOCK_IN
Cougar Point(B3)
no clock gen pull down
PCICLK LOOPBACK
U41A
1 OF 9
PCI
Cougar Point(B3)
EMI
MICRO-STAR INT'L CO.,LTD
MS-7680
CP-PCI/E/DMI/USB/CLK
Size Custom
Rev 2.3
Date: Thursday, June 02, 2011
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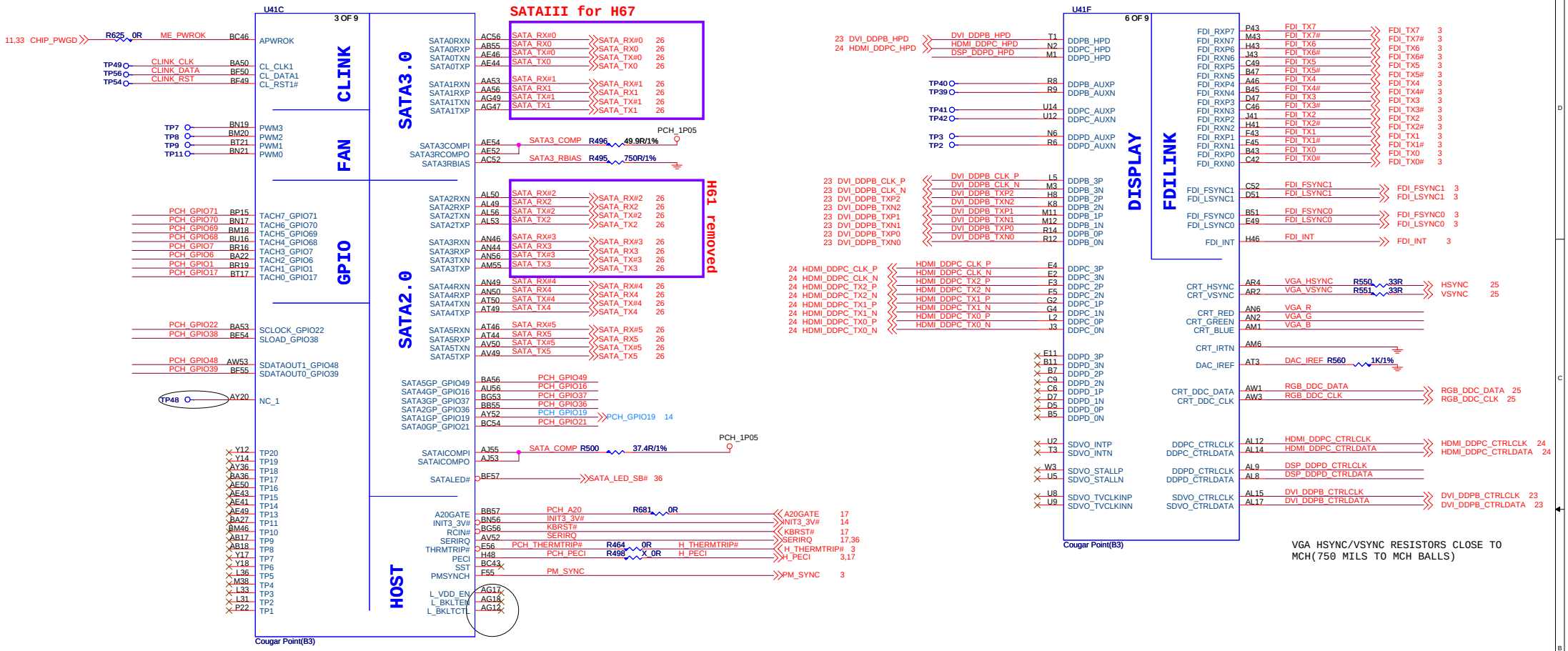

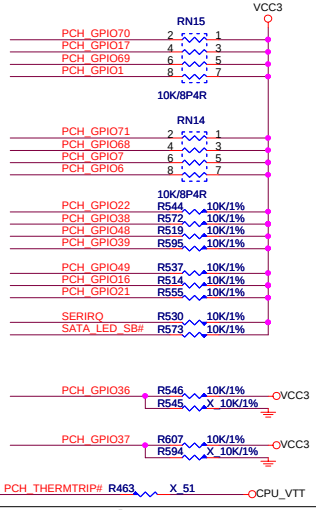

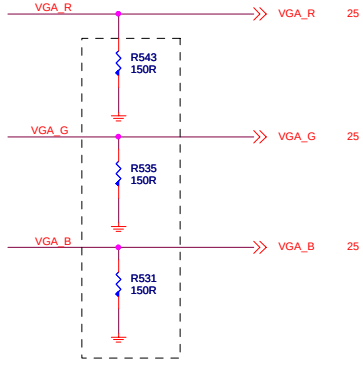

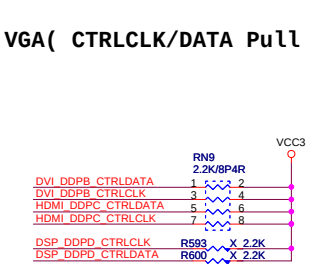

MICRO-STAR INT'L CO.,LTD

MS-7680

Size	Document Description	Rev
Custom	CP-SATA/HOST/FAN/GPIO/VGA	2.3

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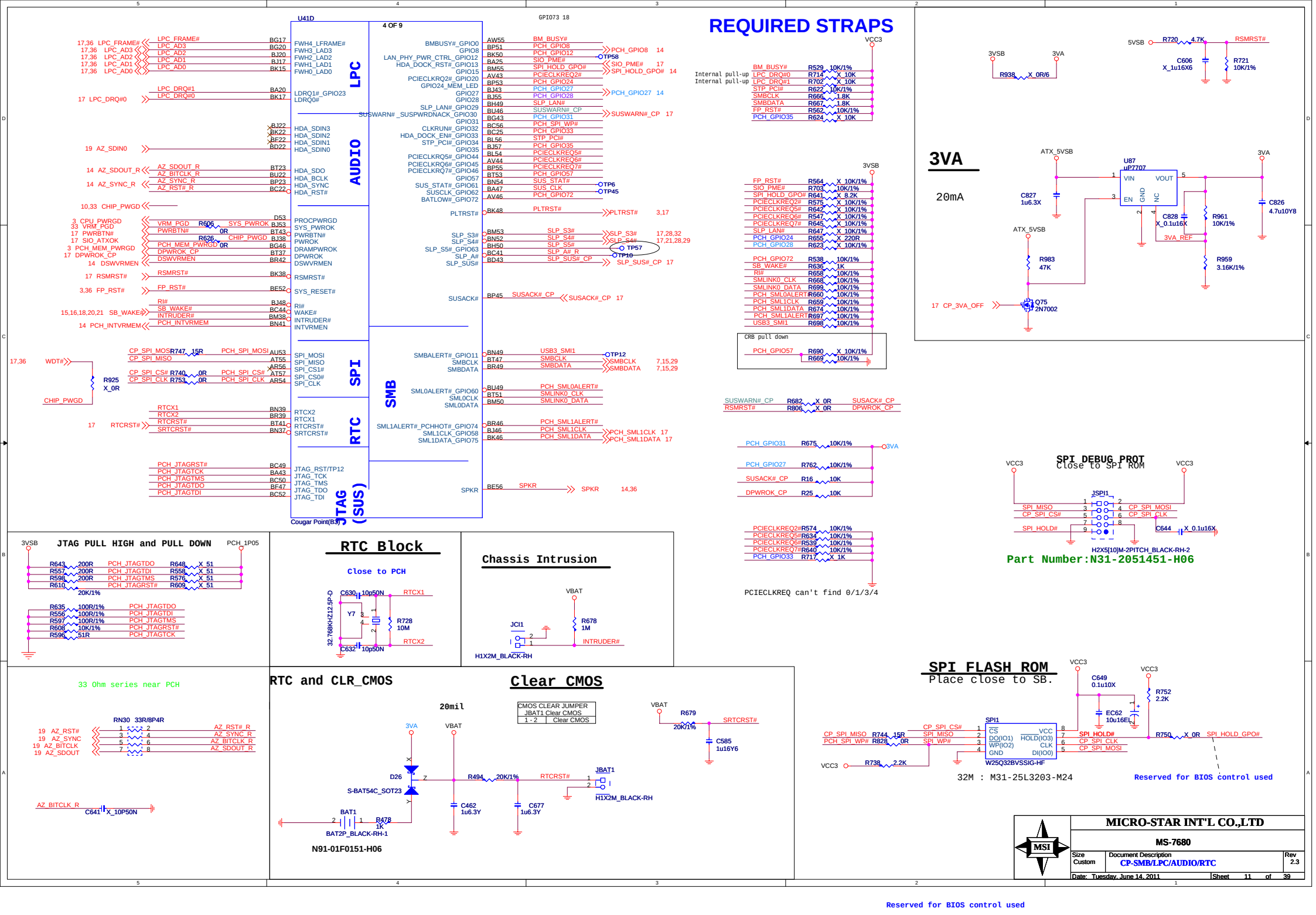
REQUIRED STRAPS
3VA
20mA
SPI DEBUG PROT
Close to SPI ROM
Part Number:N31-2051451-H06
JTAG PULL HIGH and PULL DOWN
RTC Block
Close to PCH
Chassis Intrusion
SPI FLASH ROM
Place close to SB.
32M : M31-25L3203-M24
Reserved for BIOS control used
RTC and CLR_CMOS
Clear CMOS
20mil
33 Ohm series near PCH
N91-01F0151-H06
MICRO-STAR INT'L CO.,LTD
MS-7680
CP-SMB/LPC/AUDIO/RTC
Date: Tuesday, June 14, 2011
Sheet 11 of 39

Change to 10UH if
VCCA_DPLLA/VCCA_DPLLB
has noise issue.

PCH_1P05

R460 X_0/8 VCCAFDIPLL
C415 10u6.3X8

R526 X_0R VCCACLK
NO THIS PIN

R461 X_0/8 VCCAPLLDMI2
C417 10u6.3X8
C426 1u6.3X

R567 0R/8 VCCCLKDMI
C550 10u6.3X8
C551 1u6.3X

R475 0R/8 VCCA_DPLLA
EC46 X_100u16SO
C460 10u6.3X8
C472 1u6.3X

R515 0R/8 VCCA_DPLLB
EC47 X_100u16SO
C474 10u6.3X8
C475 1u6.3X

PCH_1P05

DMI PLL FILTER
L23 X_L1U_500mA_0805
VCCAPLLEXP
C420 X_10u6.3X8
C427 1u6.3X

SATA PLL FILTER
L24 X_L10U_100mA_0805
VCCAPLLSATA
C459 X_10u6.3X8
C464 1u6.3X

PCH_1P05: 7.66A
CPU_VTT: 0.058A
VCC1_8: 0.159A
VCC3: 0.697A
3VSB: 0.11A
5VREF: 0.001A
5VREF_SUS: 0.001A

PCH_1P05

U41H
8 OF 9
Cougar Point(B3)

CPU_VTT
D55 V_PROC_IO
B56 V_PROC_IO_NCTF

CPU_VTT
B41 VCCDMI_02
E41 VCCDMI_01

C429 1u6.3X
VCCAPLLDMI2 A19 VCCAPLLDMI2
VCCCLKDMI AJ20 VCCCLKDMI

5VREF BF1 V5REF
5VREF_SUS BT25 V5REF_SUS

+3.3V_DAC
AT1 VCCADAC
VCCACLK AL5 VCCACLK

VCCA_DPLLA AB1 VCCADPLLA
VCCA_DPLLB AC2 VCCADPLLB

VCCAPLLSATA U56 VCCAPLLSATA

VCCAPLLEXP B53 VCCAPLLEXP

VCCAFDIPLL C54 VCCAFDIPLL

3VSB AV28 VCCSUSHDA

VCC3 AN52 VCCSPI

VCC1_8 CP24 X_COPPER
R2 VCCVRM_04
R54 VCCVRM_03
R56 VCCVRM_02
AJ1 VCCVRM_01

C428 1u6.3X DCPSUS A39 DCPSUS_03
TP44 AT41 DCPSUS_02
TP43 AA32 DCPSUS_01

C583 0.1u10X DCPRTC BR54 DCPRTC
BT56 DCPRTC_NCTF

TP51 AV41 DCPSUSBYP

C521 0.1u10X DCPSST BA46 DCPSST

VBAT BU42 VCCRTC
AV40 VCCDSW3_3

3VA
C720 X_0.1u10X
Backside

PCH_1P05
AG15 VCCDIFFCLKN_03
AE17 VCCDIFFCLKN_02
AE15 VCCDIFFCLKN_01

PCH_1P05 CP7 X_COPPER VCCSSC
VCCSSC_02 AE20
VCCSSC_01 AC20

VCCDFTERM T57
VCCDFTERM T55
VCCNAND

VCC3_3_10 AV20
VCC3_3_09 AU20
VCC3_3_08 AU22
VCC3_3_07 AN38
VCC3_3_06 AL38
VCC3_3_05 BD20
VCC3_3_04 BD17
VCC3_3_03 BC17
VCC3_3_02 AE57
VCC3_3_01
VCC3

VCCSUS3_3_011 BT35
VCCSUS3_3_010 AU38
VCCSUS3_3_009 AT40
VCCSUS3_3_008 BA35
VCCSUS3_3_007 BK36
VCCSUS3_3_006 BJ36
VCCSUS3_3_005 AY33
VCCSUS3_3_004 AY31
VCCSUS3_3_003 AV32
VCCSUS3_3_002 AV30
VCCSUS3_3_001 U31
3VSB

VCC1_8 CP23 X_COPPER VCCNAND
C457 X_0.1u10X

PCH_1P05
VCCCORE_022 AR34
VCCCORE_021 AR32
VCCCORE_020 AN34
VCCCORE_019 AN32
VCCCORE_018 AL34
VCCCORE_017 AL32
VCCCORE_016 AJ36
VCCCORE_015 AJ34
VCCCORE_014 AJ32
VCCCORE_013 AG34
VCCCORE_012 AG32
VCCCORE_011 AE36
VCCCORE_010 AE34
VCCCORE_009 AE32
VCCCORE_008 AE30
VCCCORE_007 AE28
VCCCORE_006 AE24
VCCCORE_005 AC32
VCCCORE_004 AC30
VCCCORE_003 AC28
VCCCORE_002 AC26
VCCCORE_001 AC24

VCCASW_023 AU36
VCCASW_022 AU30
VCCASW_021 AR38
VCCASW_020 AR36
VCCASW_019 AR30
VCCASW_018 AR28
VCCASW_017 AR26
VCCASW_016 AR24
VCCASW_015 AN28
VCCASW_014 AN26
VCCASW_013 AN24
VCCASW_012 AN22
VCCASW_011 AL28
VCCASW_010 AL24
VCCASW_009 AJ28
VCCASW_008 AJ26
VCCASW_007 AJ24
VCCASW_006 AG28
VCCASW_005 AG26
VCCASW_004 AG24
VCCASW_003 AU34
VCCASW_002 AV36
VCCASW_001 AU32

POWER

5VREF & 5VREF_SUS Sequencing Circuit

VCC3 Q76 2N3904
C569 1u6.3X
VCC5 R637 10R 5VREF
C568 0.1u10X

3VSB Q81 2N3904
C604 0.1u10X
5VSB R715 100R/1% 5VREF_SUS
C600 0.1u10X

VCC3 +3.3V_DAC
CP5 X_COPPER
Near ball AF1
C538 0.1u10X

3VSB
C592 C598 0.1u10X
0.1u10X

PCH decoupling cap

PCH_1P05
C401 0.1u10X
C434 0.1u10X
C439 1u10Y6
C404 10u6.3X8
C418 10u6.3X8
C419 10u6.3X8
C458 4.7u10X8
C406 0.1u10X

VBAT
C603 0.1u10X
C609 1u10Y6

VCC3
C479 0.1u10X
C580 X_0.1u10X
C489 X_0.1u10X
C431 X_0.1u10X
C542 0.1u10X
C597 4.7u10X8
C589 1u10Y6

CPU_VTT
C413 4.7u10X8
C423 0.1u10X
C430 0.1u10X

Backside
PCH_1P05
C712 X_1u10Y6
C716 X_1u10Y6
C717 X_10u6.3X8
C715 X_1u10Y6
C713 X_0.1u10X
C719 X_0.1u10X
C718 X_0.1u10X
C714 X_0.1u10X

MICRO-STAR INT'L CO.,LTD
MS-7680
Size Custom
Document Description CP-POWER
Rev 2.3
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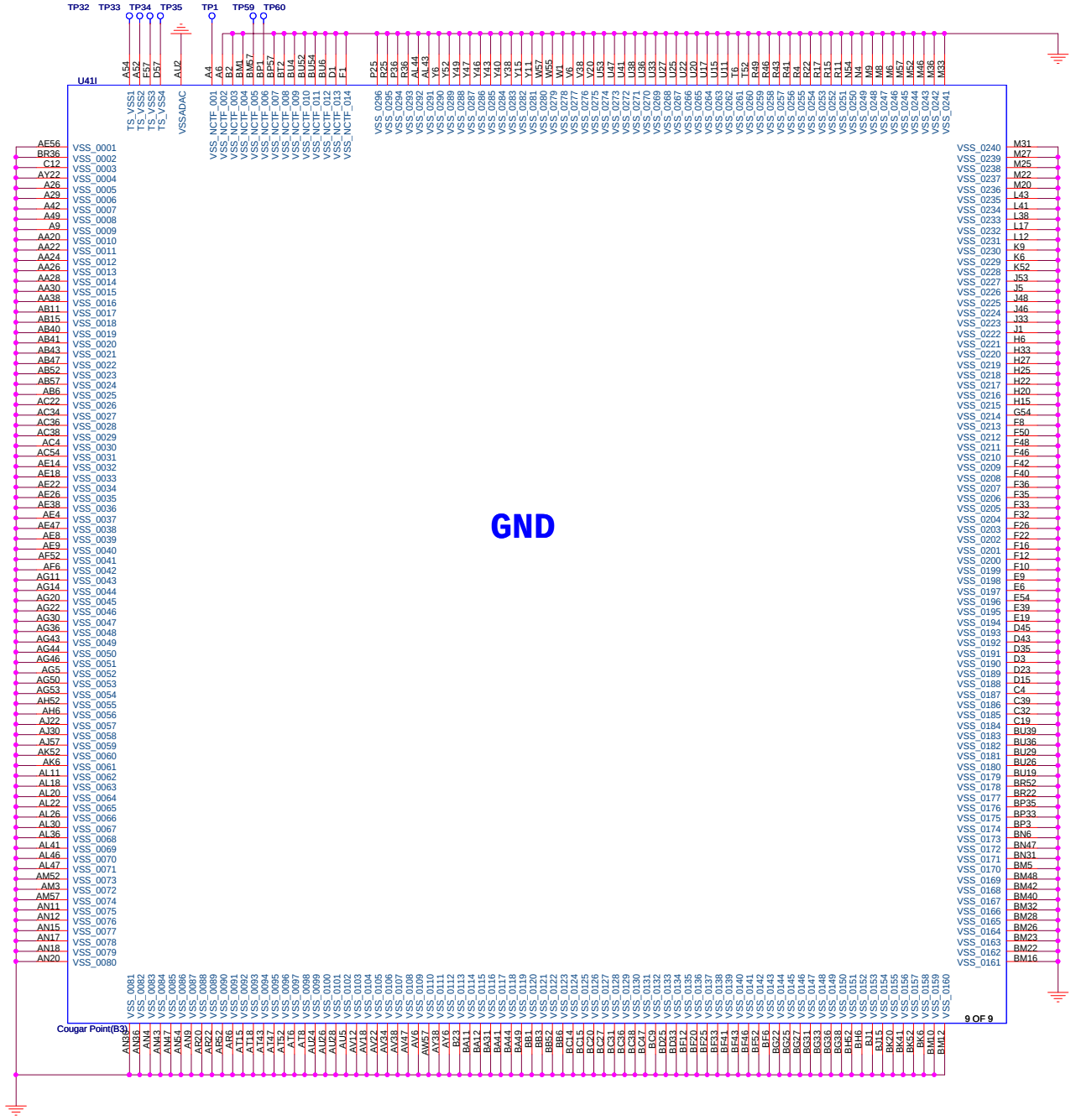
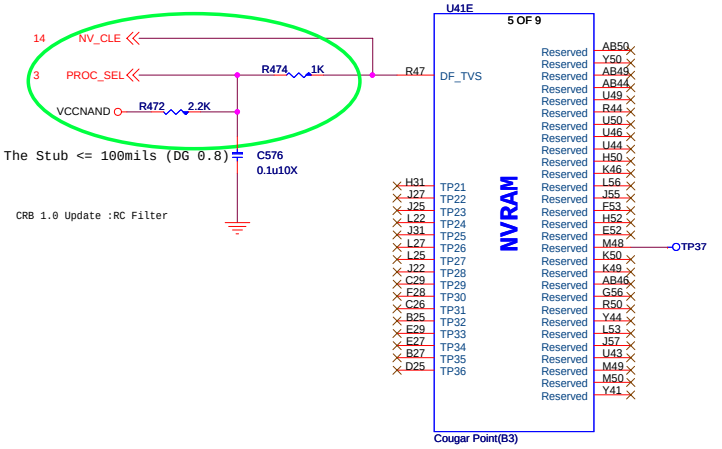
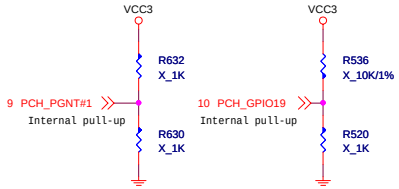


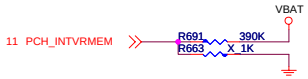


MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size: Custom	Document Description: CP-GND/NVRAM	Rev: 2.3
Date: Thursday, June 02, 2011	Sheet 13 of 39	

PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



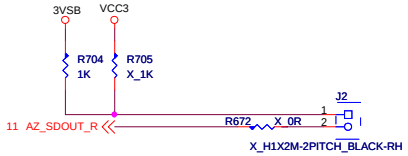


INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltageregulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

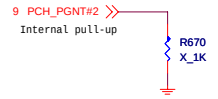
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.

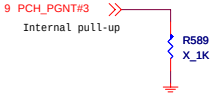


HDA_SDO
Disable ME in Manufacturing Mode when pull LOW ????

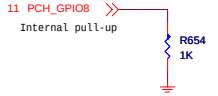
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



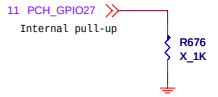
DMI AC/DC MODE
0 : AC
1 : DC *



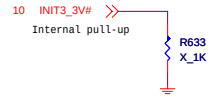
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

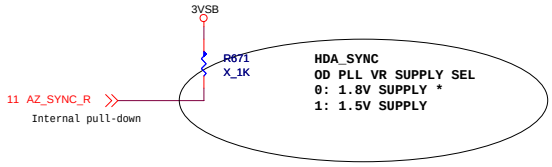


GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up

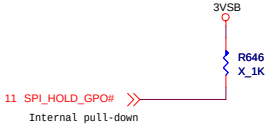


INT3_3V#
0 : ????????????????
1 : ???????????????? *

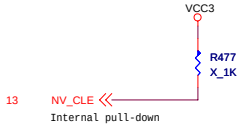
1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



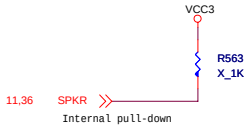
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY



GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

MICRO-STAR INT'L CO.,LTD

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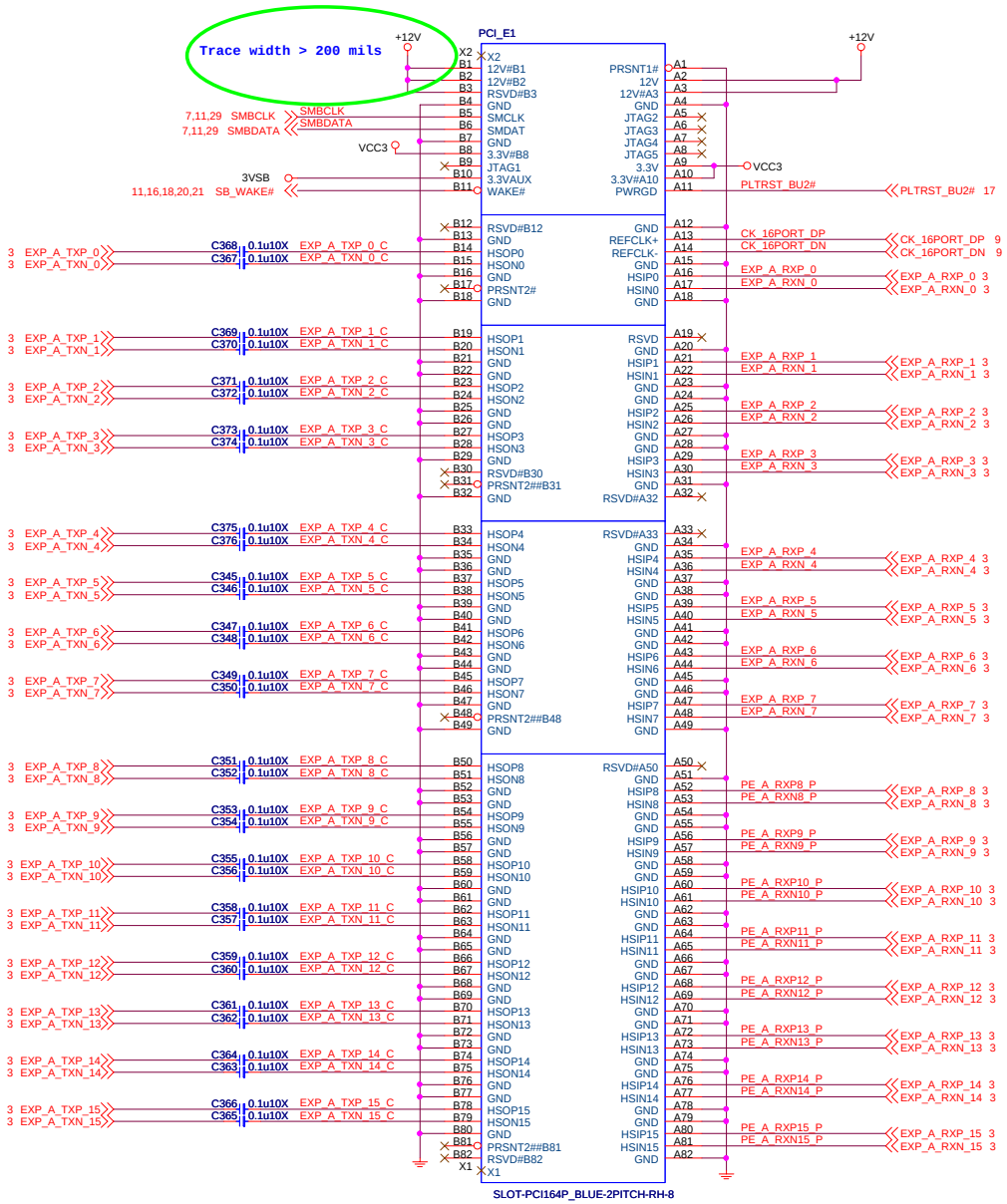
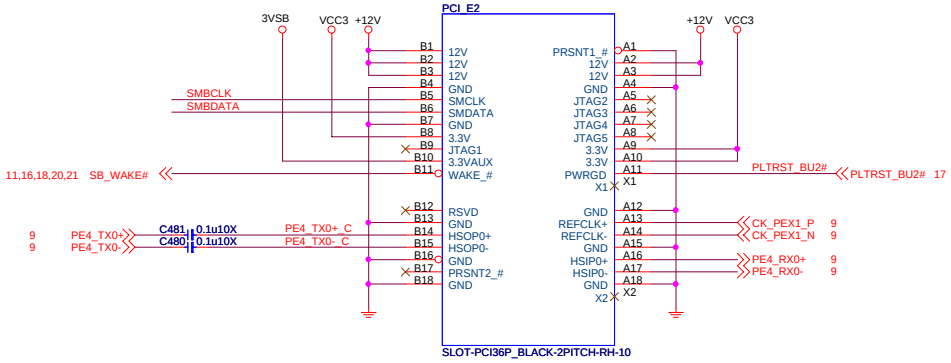
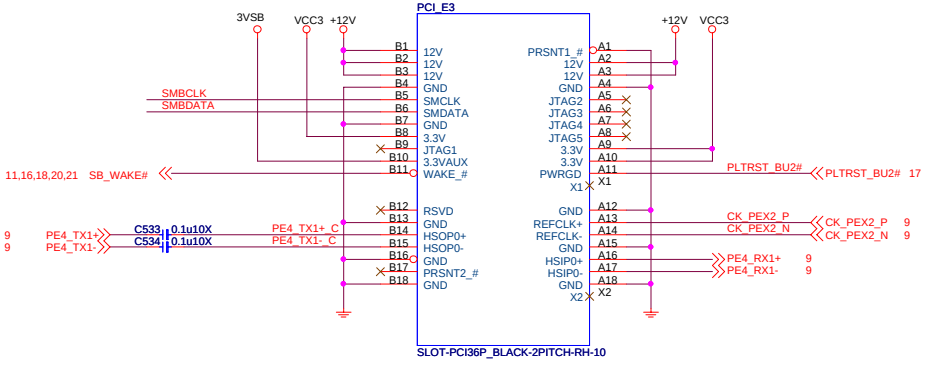
PCI_Express X16 Slot

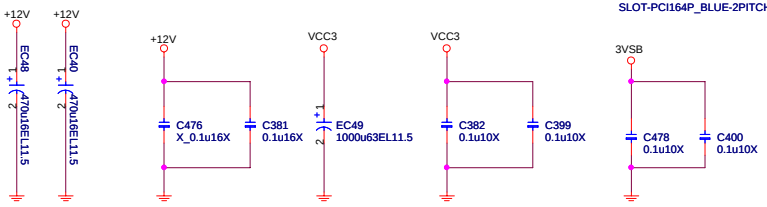


PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT





MICRO-STAR INT'L CO.,LTD	
MS-7680	
Size: Custom	Document Description: PCIE x16 /x1/x1 — Rev: 2.3
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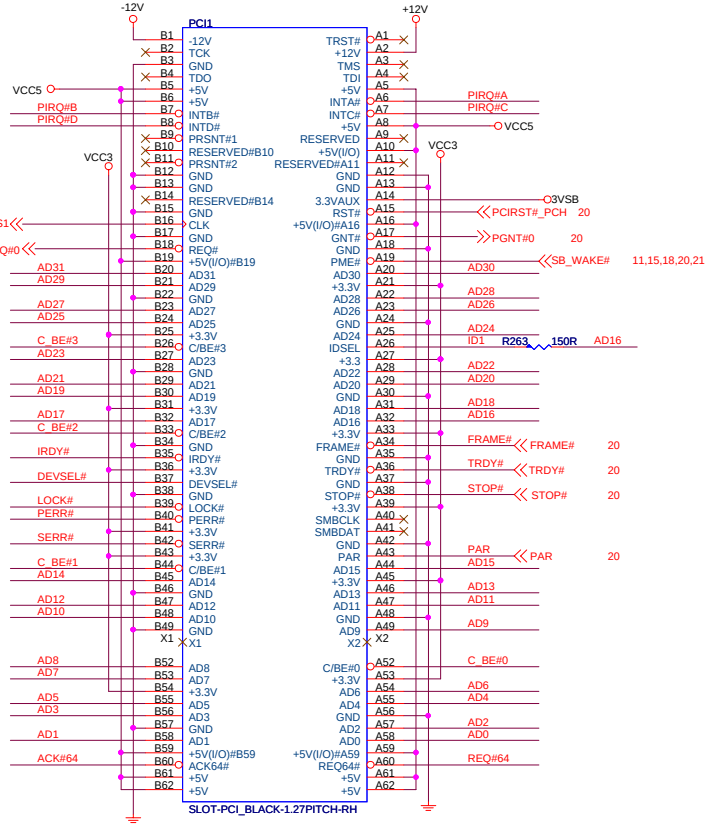
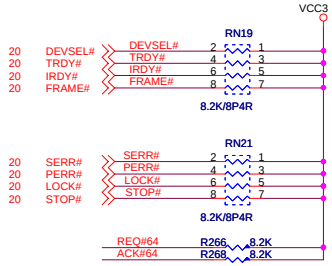
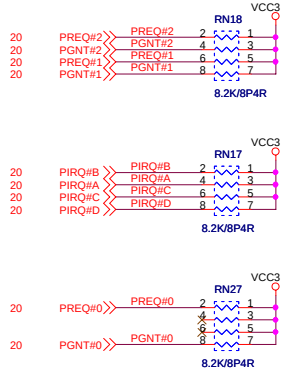
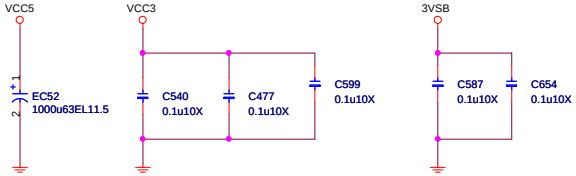


PCI PULL-UP / DOWN RESISTORS







MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size: Custom	Document Description: PCIx1 Slots	Rev: 2.3
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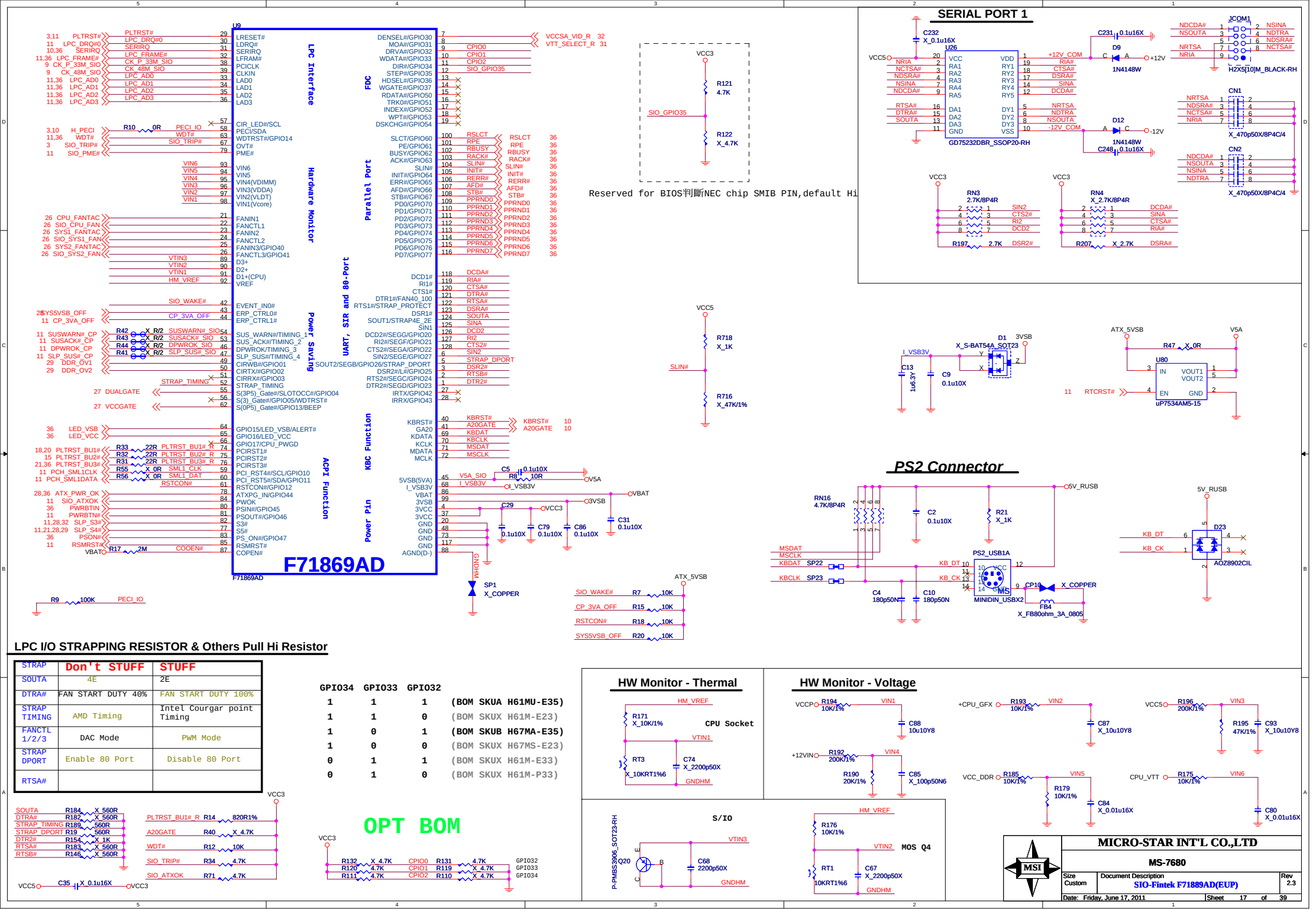
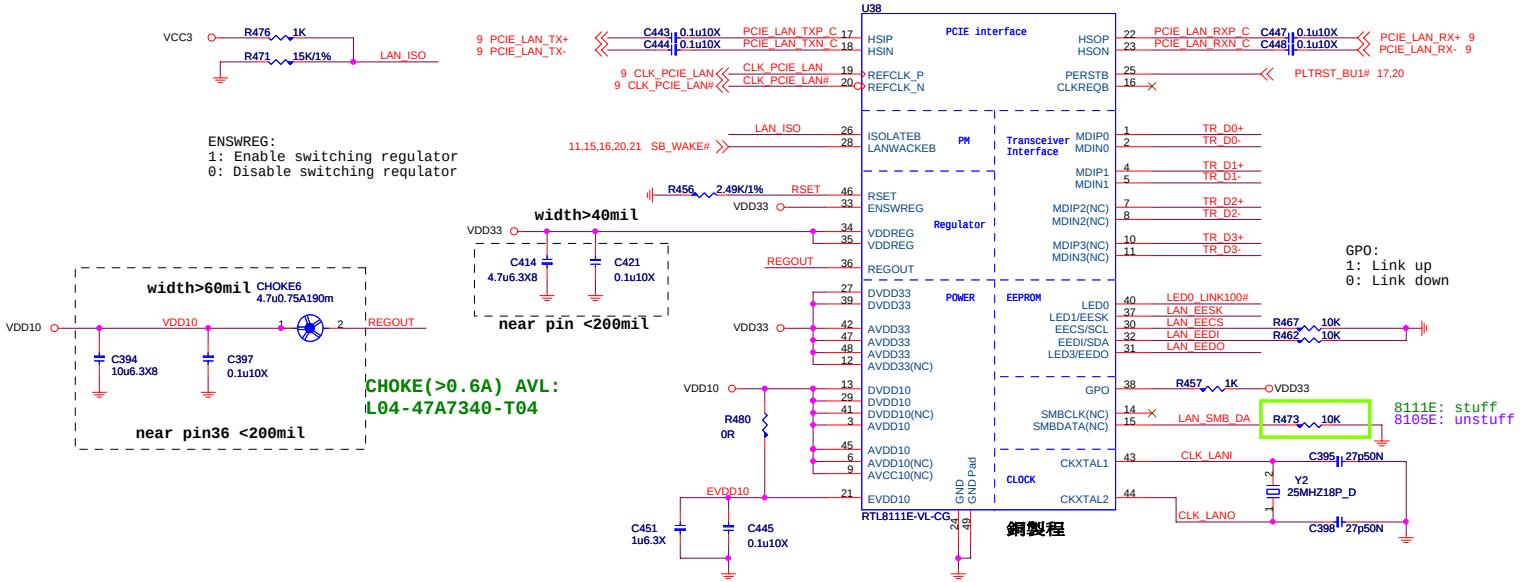


STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Courgar point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT	Enable 80 Port	Disable 80 Port
RTSA#		

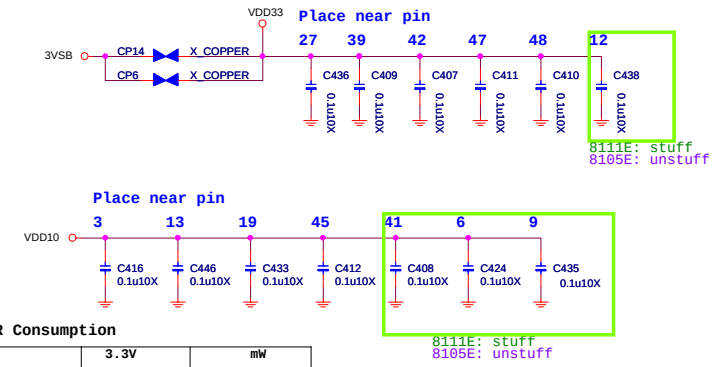
GPIO34	GPIO33	GPIO32	
1	1	1	(BOM SKUA H61MU-E35)
1	1	0	(BOM SKUX H61M-E23)
1	0	1	(BOM SKUB H67MA-E35)
1	0	0	(BOM SKUX H67MS-E23)
0	1	1	(BOM SKUX H61M-E33)
0	1	0	(BOM SKUX H61M-P33)

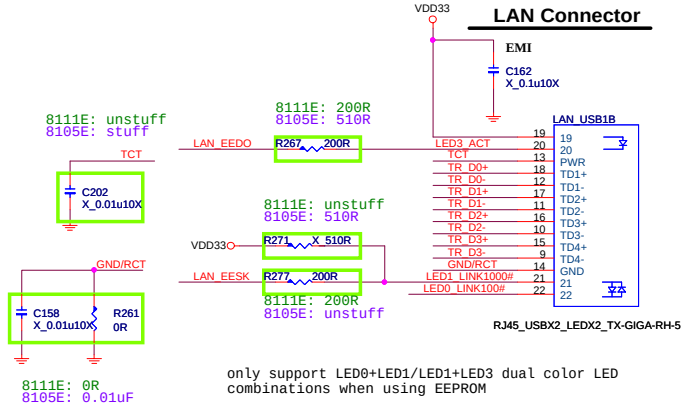
RTL8111E Giga LAN

RTL8105E 10/100M LAN

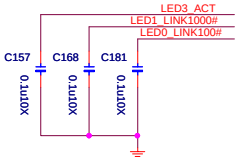


3.3v Power on rise time : 1~100ms. MAX: 163mA





Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Yellow Active Blinking 1000 Orange 100 Green 10 None	Link Yellow Active Blinking 100 Green 10 None
19 — 250R — Yellow 20	19 — Yellow 20
Orange 21 22 — 250R — Green	21 22 — Green



8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

MICRO-STAR INT'L CO.,LTD

MS-7680

Size: Custom | Document Description: LAN - RTL8111E / 8105E | Rev: 2.3

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ALC887-VD
ALC892

11mA

Closed Codec

VCC3

用SMD CAP 手動量測會FAIL在THD+N
用EL-CAP or SOLID cap,才會pass

C1 closed PIN25

U51

ALC887-VD2-CG

銅製程

45.8mA

LDOVDD

Closed Codec

LIN_OUT

SURR

LIN_IN

CEN/BAS

MIC1

SIDESURR

for rear I/O 6port:
887VD/892:1k

for rear I/O 3port:
887VD/892:75R

JACK-AUDIOX3F_PK/GR/BU-RH-6

當串接電容有極性時，需上對地電阻

N54-13F0271-K06

N54-26F0111-K06

EMI

Closed Codec

SPDIF OUT

N31-2051411-H06

JAUD1

H2X5[8]M_BLACK-RH

Close to Jack

Varister --> cap for cost down

Close to Front panel

MICRO-STAR INT'L CO.,LTD

MS-7680

Size: Custom

Document Description: ALC892_COLAY_ALC887VD

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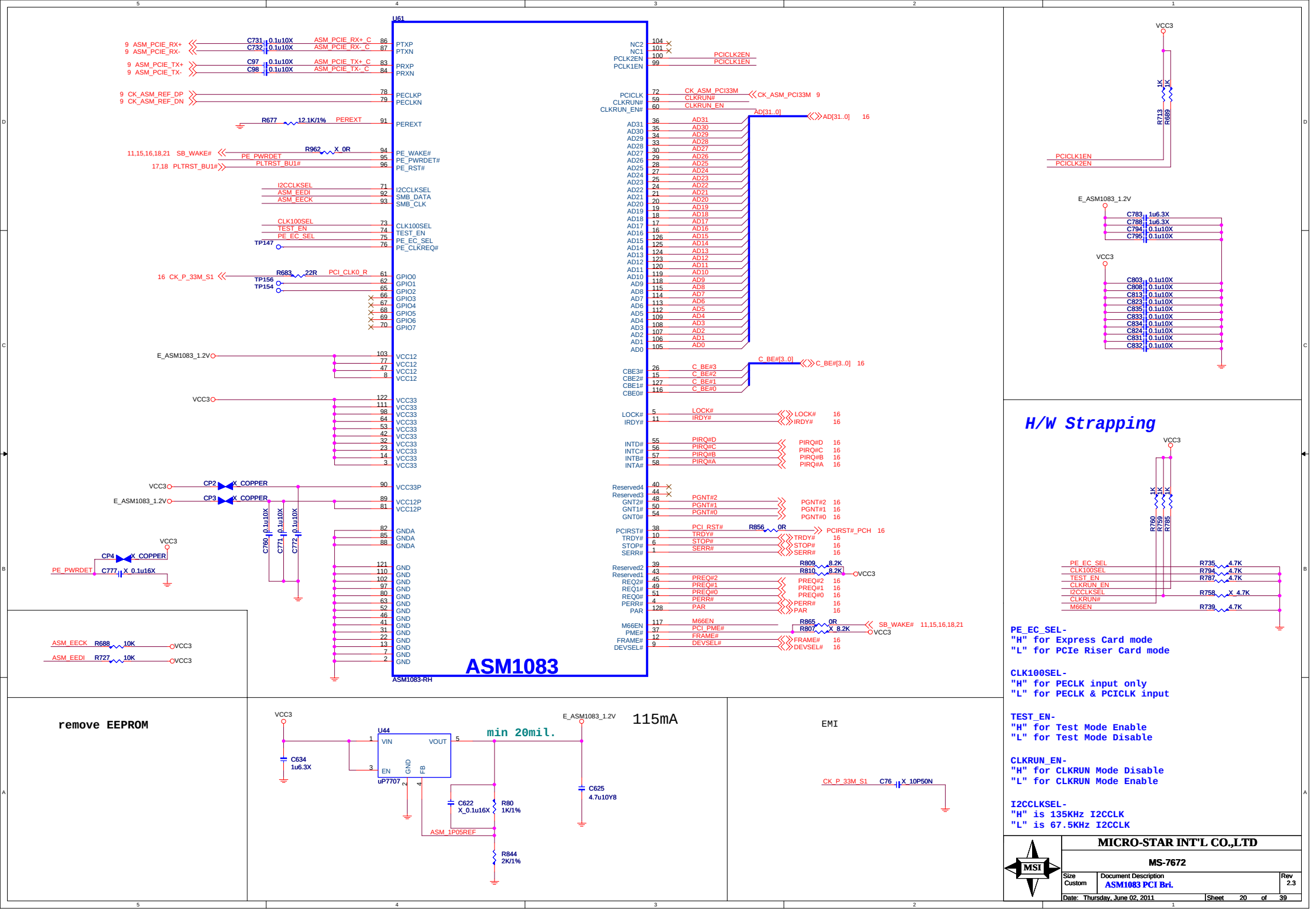
U61
ASM1083
ASM1083-RH
PTXP
PTXN
PRXP
PRXN
PECLKP
PECLKN
PEREXT
PE_WAKE#
PE_PWRDET#
PE_RST#
I2CCLKSEL
SMB_DATA
SMB_CLK
CLK100SEL
TEST_EN
PE_EC_SEL
PE_CLKREQ#
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
VCC12
VCC33
VCC33P
VCC12P
GNDA
GND
PCICLK2EN
PCICLK1EN
CK_ASM_PCI33M
CLKRUN#
CLKRUN_EN
AD[31..0]
C_BE#[3..0]
LOCK#
IRDY#
PIRQ#D
PIRQ#C
PIRQ#B
PIRQ#A
PGNT#2
PGNT#1
PGNT#0
PCI_RST#
PCIRST#_PCH
TRDY#
STOP#
SERR#
PREQ#2
PREQ#1
PREQ#0
PERR#
PAR
M66EN
PCI_PME#
FRAME#
DEVSEL#
SB_WAKE#
E_ASM1083_1.2V
VCC3
ASM_EECK
ASM_EEDI
remove EEPROM
U44
uP7707
VIN
VOUT
EN
GND
FB
min 20mil.
115mA
EMI
CK_P_33M_S1
H/W Strapping
PE_EC_SEL
CLK100SEL
TEST_EN
CLKRUN_EN
I2CCLKSEL
CLKRUN#
M66EN
PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode
CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input
TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable
CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable
I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK
MICRO-STAR INT'L CO.,LTD
MS-7672
Size
Custom
Document Description
ASM1083 PCI Bri.
Rev
2.3
Date: Thursday, June 02, 2011
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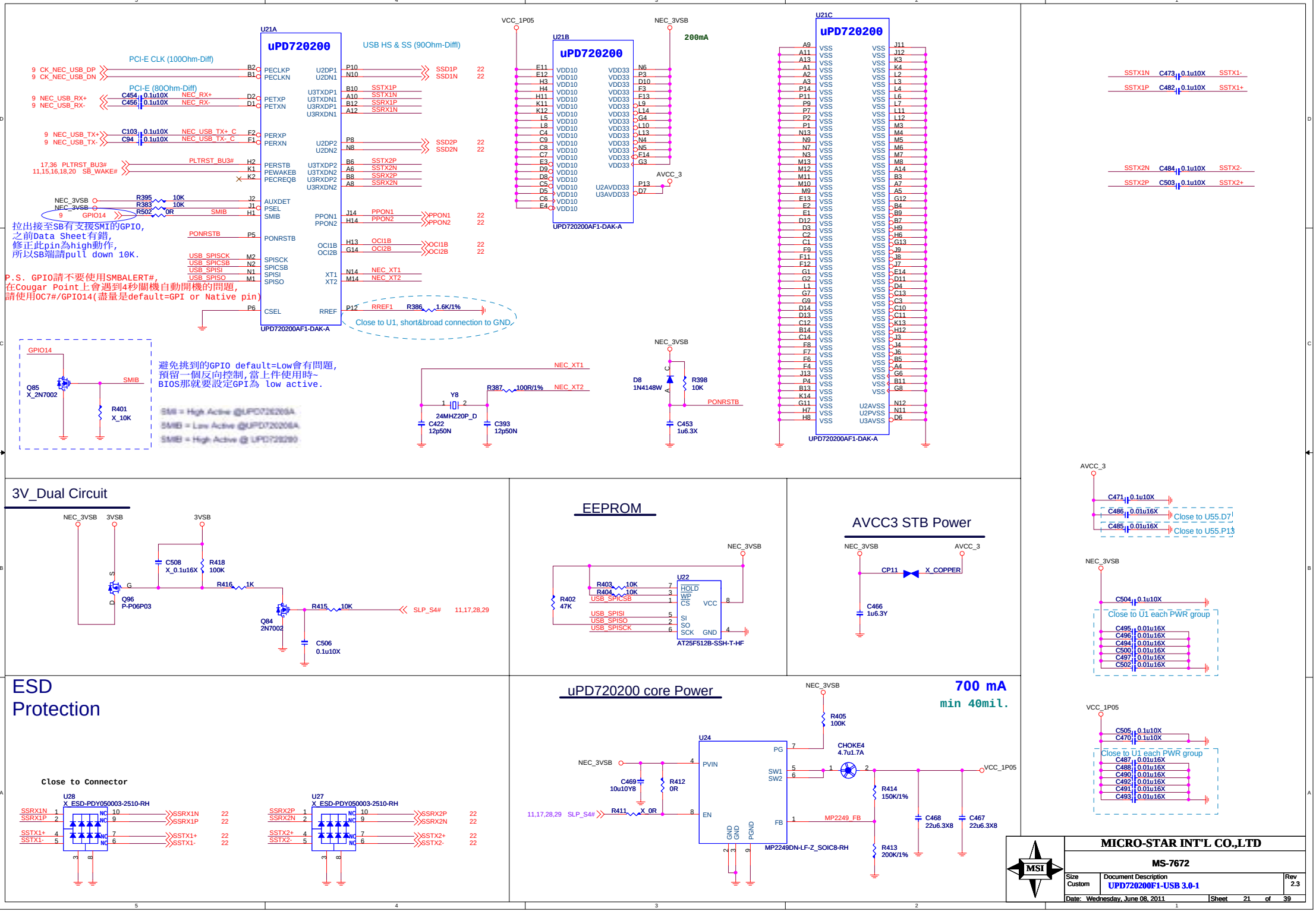
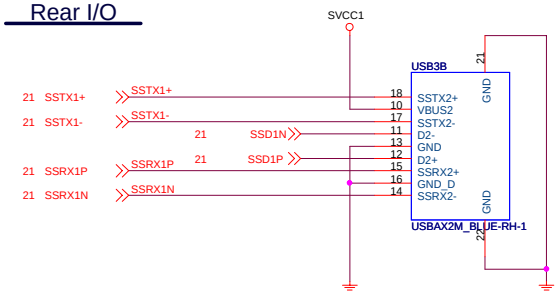
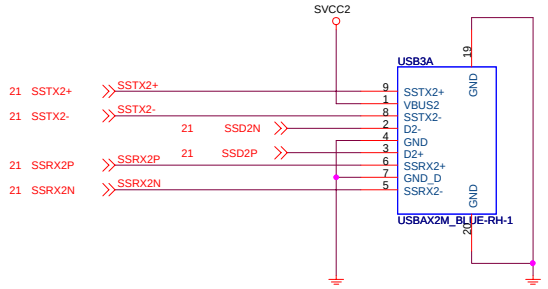
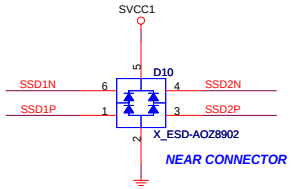
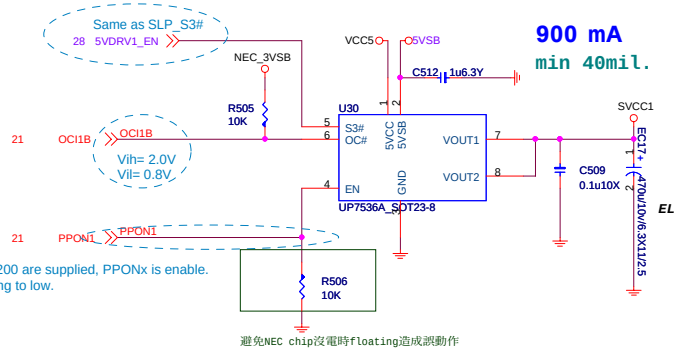

uPD720200
USB HS & SS (90Ohm-Diff)
PCI-E CLK (100Ohm-Diff)
PCI-E (80Ohm-Diff)
拉出接至SB有支援SMI的GPIO,
之前Data Sheet有錯,
修正此pin為high動作,
所以SB端請pull down 10K.
P.S. GPIO請不要使用SMBALERT#,
在Cougar Point上會遇到4秒關機自動開機的問題,
請使用OC7#/GPIO14(盡量是default=GPI or Native pin)
Close to U1, short&broad connection to GND
避免挑到的GPIO default=Low會有問題,
預留一個反向控制,當上件使用時~
BIOS那就要設定GPI為 low active.
200mA
3V_Dual Circuit
EEPROM
AVCC3 STB Power
ESD
Protection
Close to Connector
uPD720200 core Power
700 mA
min 40mil.
MICRO-STAR INT'L CO.,LTD
MS-7672
UPD720200F1-USB 3.0-1
Wednesday, June 08, 2011

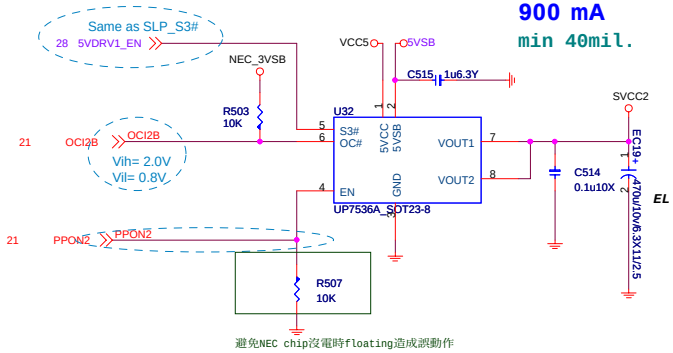
Rear I/O











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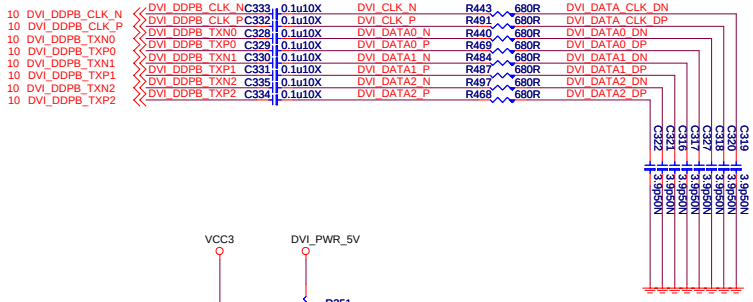
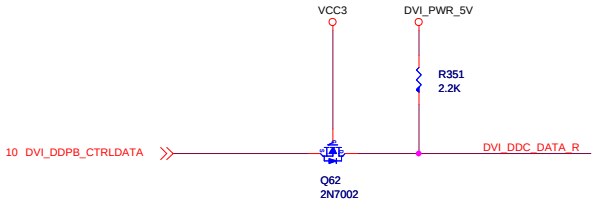
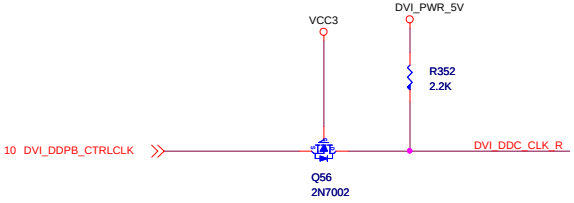
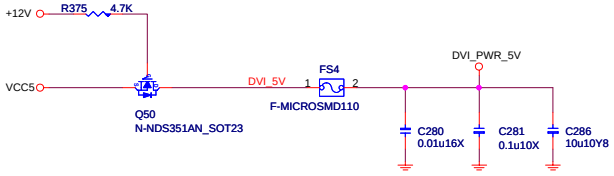
DVI level shifter

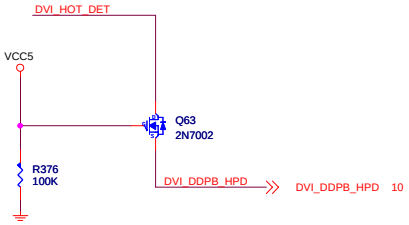
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

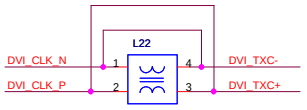


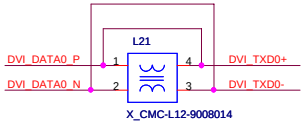


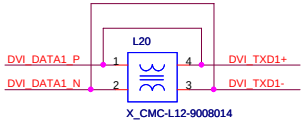


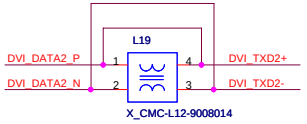


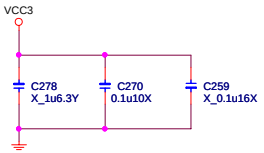


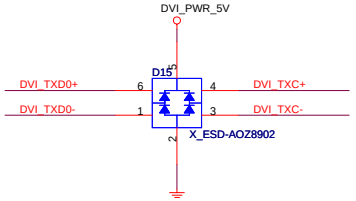


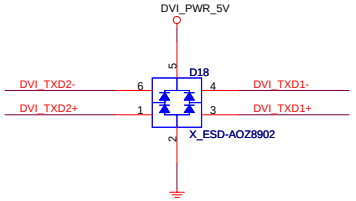


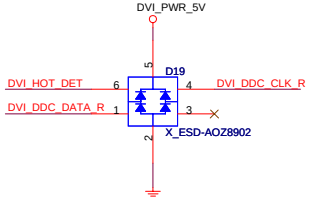


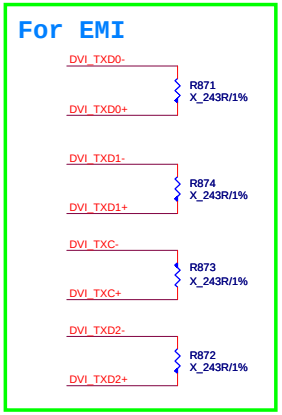


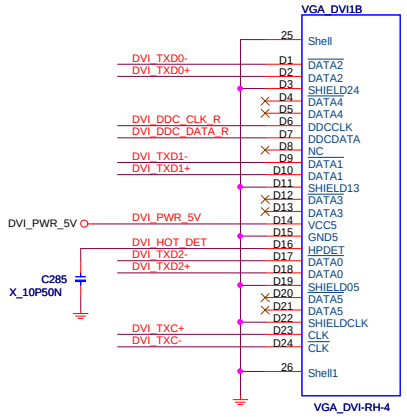


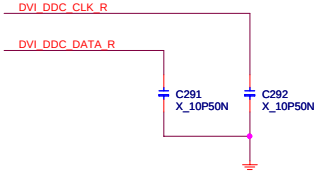












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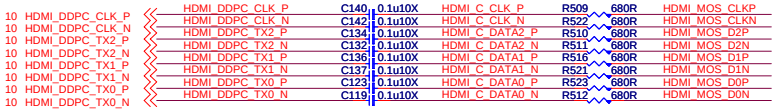
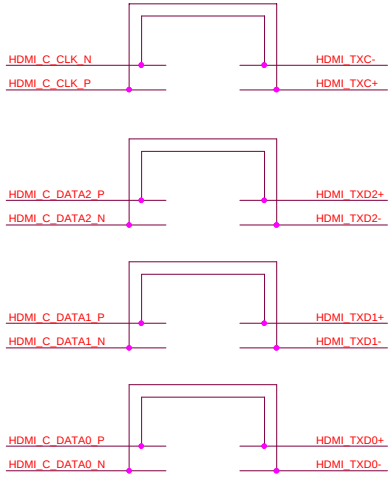
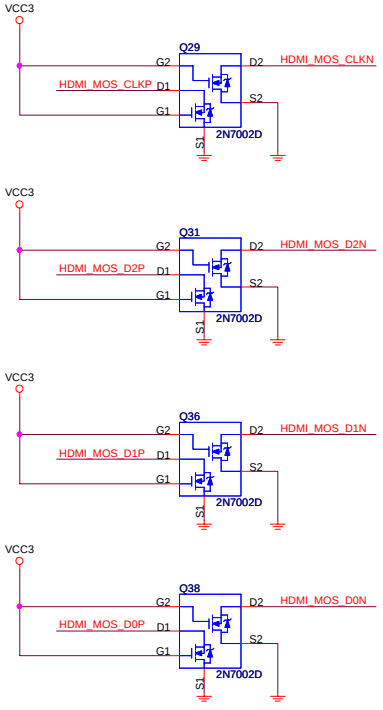
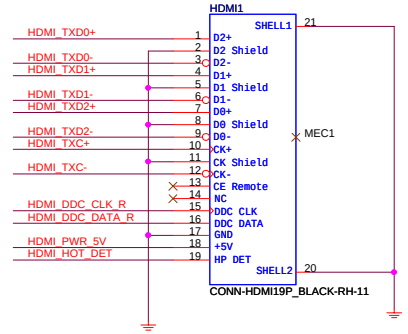
HDMI level shifter

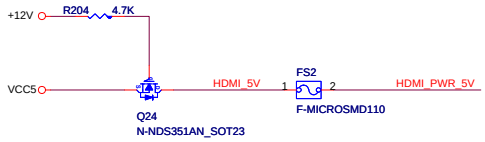
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

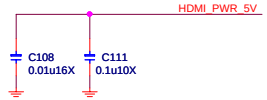


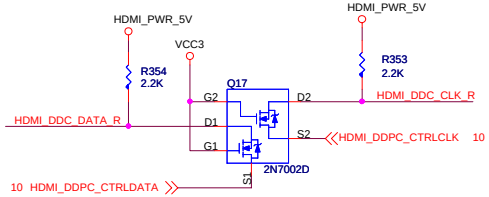


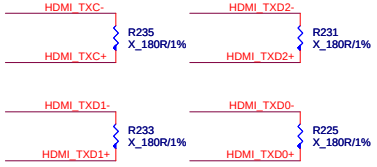












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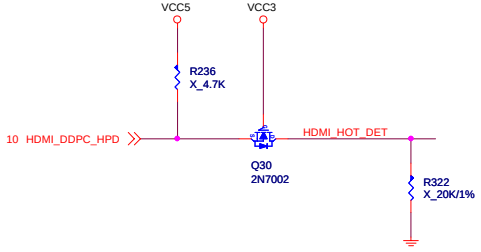

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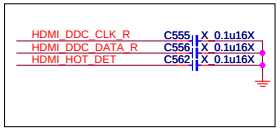

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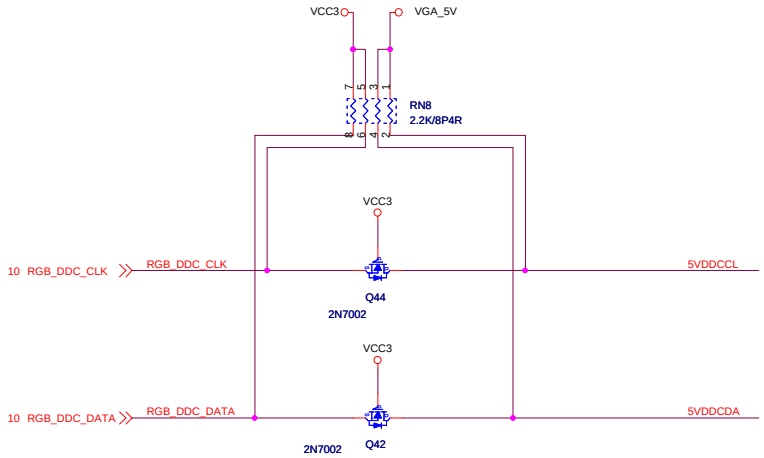
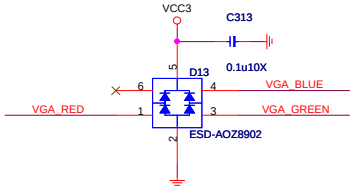
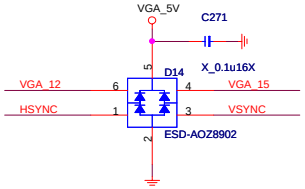
D-Sub

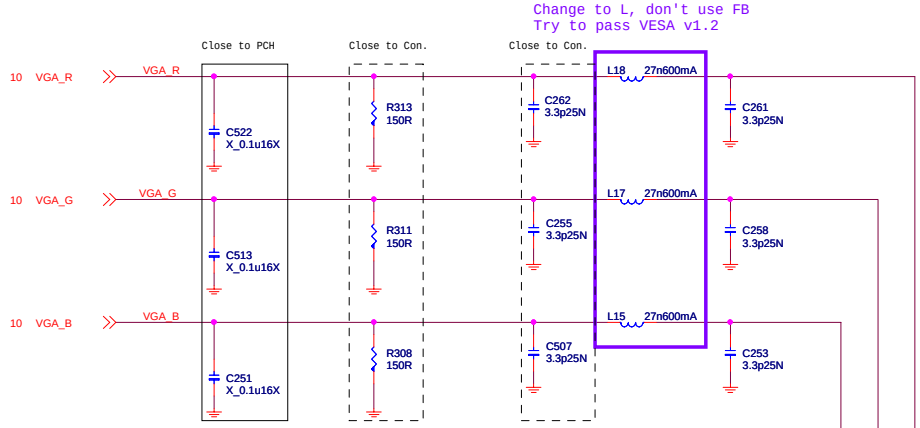
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

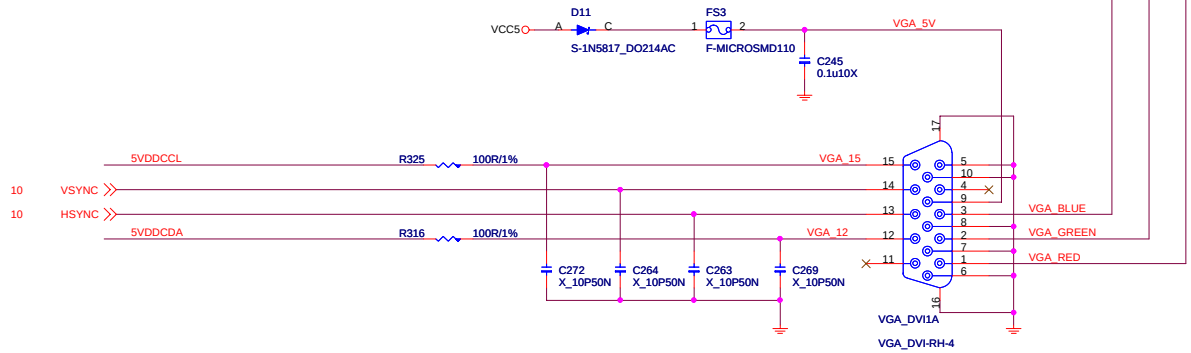
Level shift











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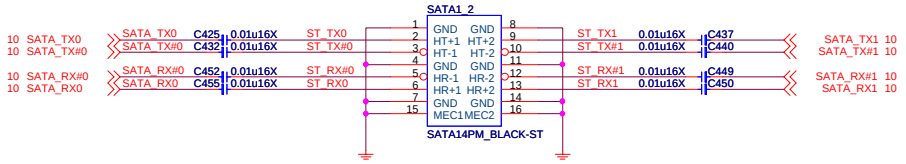
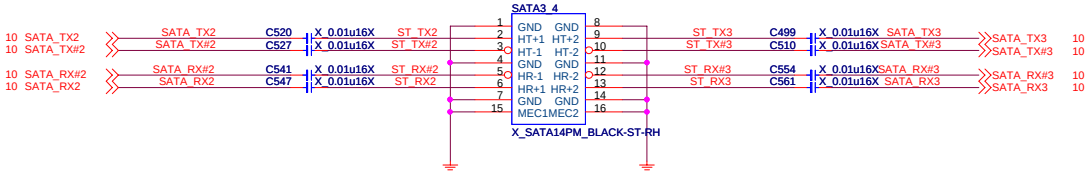
SATA 6G PORT 0,1

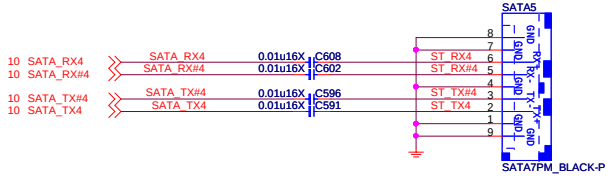
H61 PORT 0/1 Support 3G
H67 PORT 0/1 Support 6G

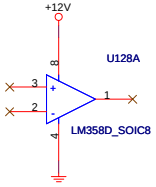


SATA 3G PORT 2,3

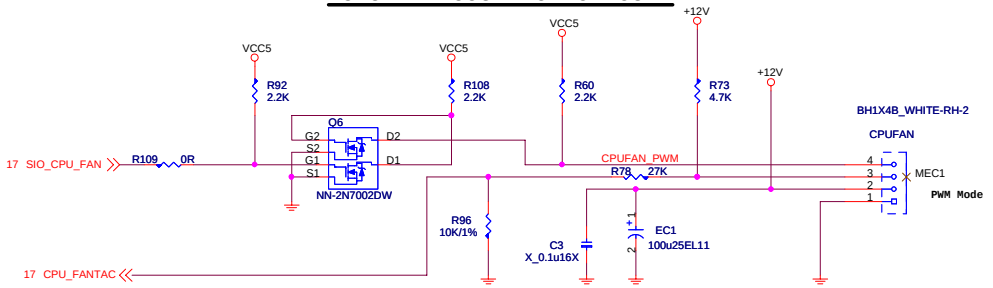


For H61,SATA3&4 removed

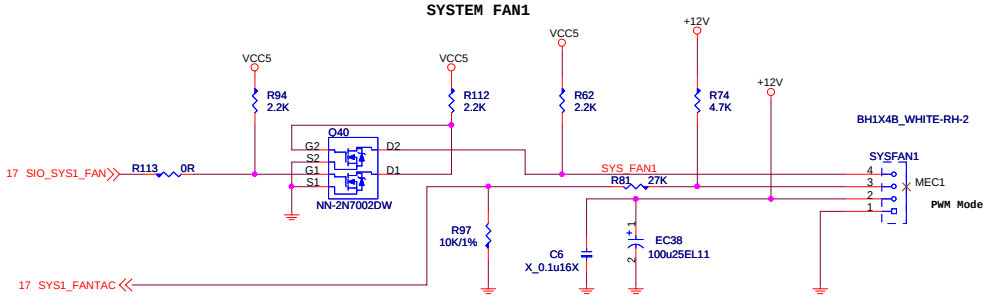




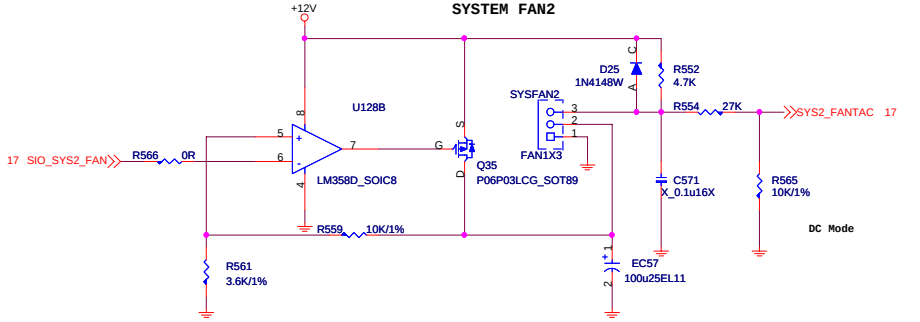
CPU FAN-COUNTROL CIRCUIT



SYSTEM FAN-COUNTROL CIRCUIT



SYSTEM FAN2



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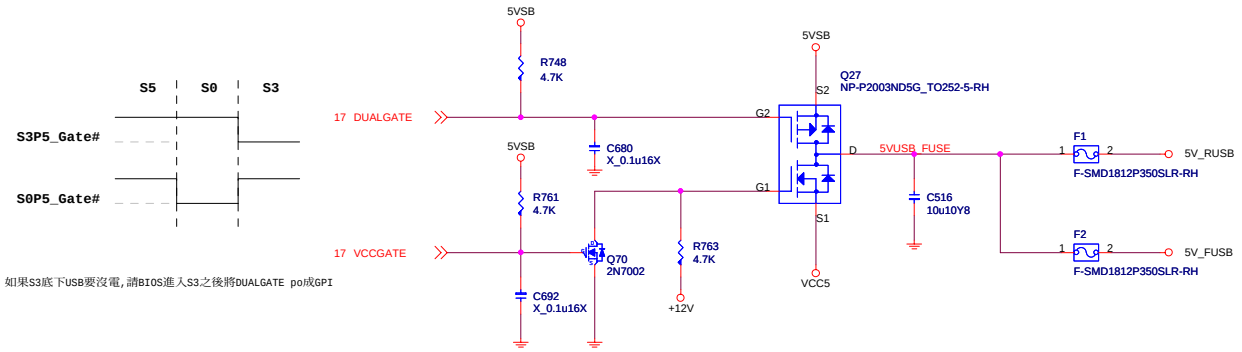
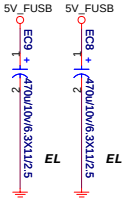
5V_RUSB Switch



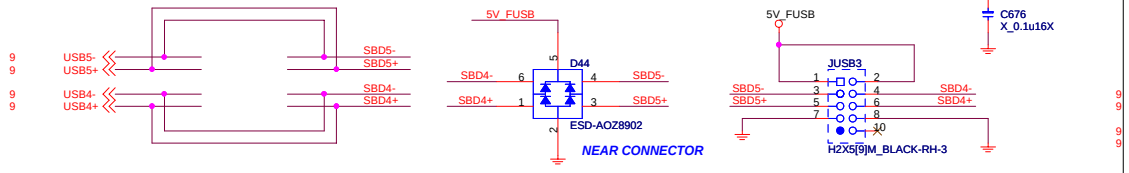
Front USB Connector

NEAR USB Front CONNECTOR

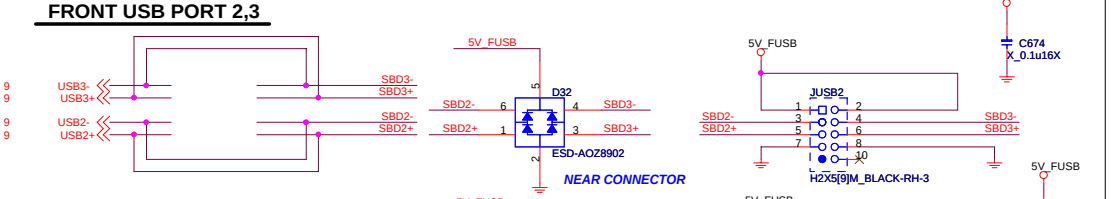


For H61 6,7,12,13 Port should be remove

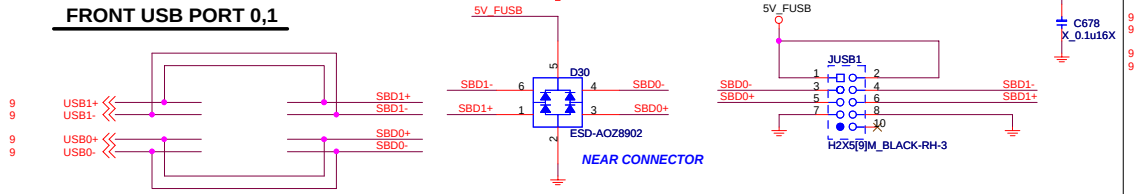
FRONT USB PORT 4,5



FRONT USB PORT 2,3

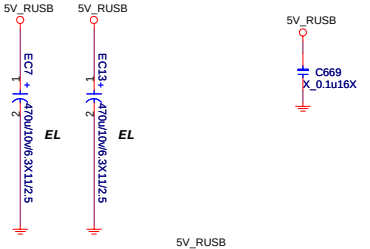


FRONT USB PORT 0,1

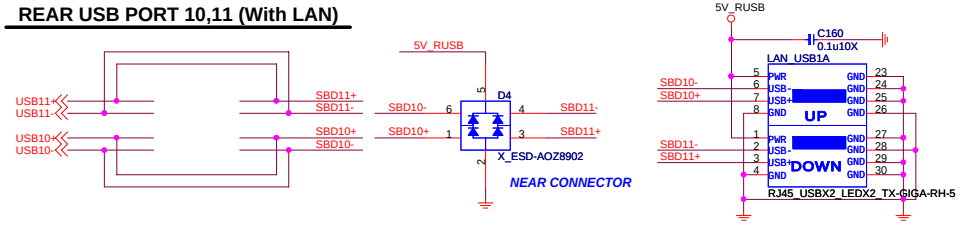


Rear USB Connector

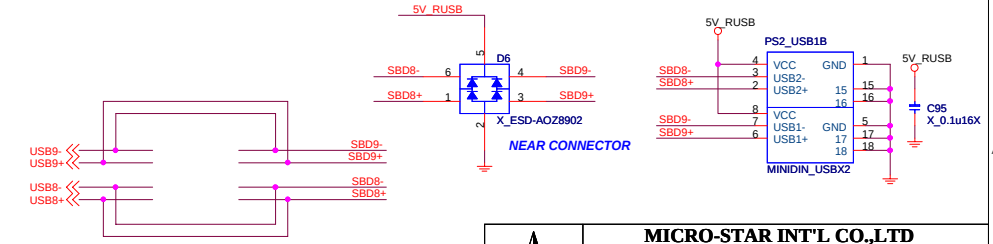
NEAR USB REAR CONNECTOR



REAR USB PORT 10,11 (With LAN)



REAR USB PORT 8,9 (With PS2)



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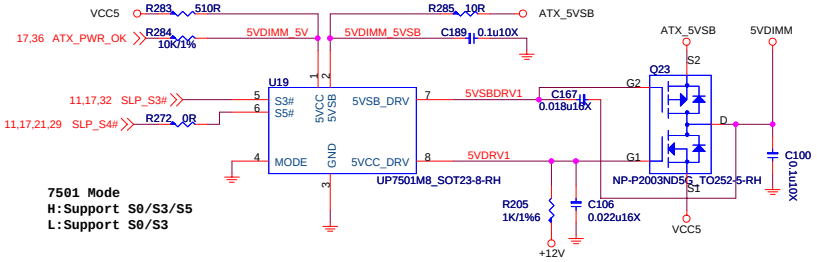
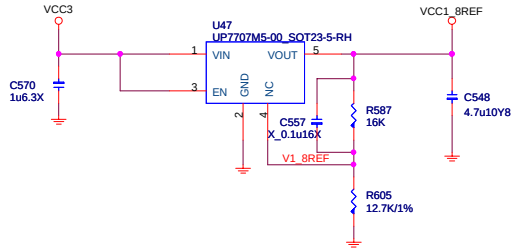
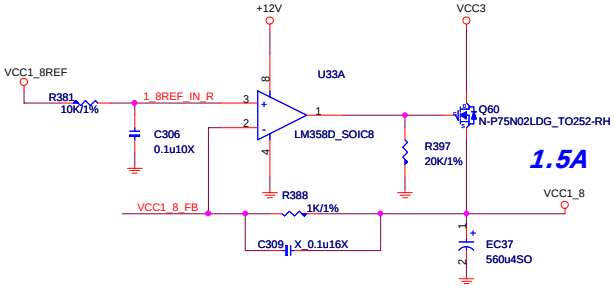
5VDIMM FOR DDR



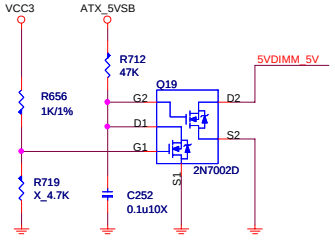
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

VCC1_8REF

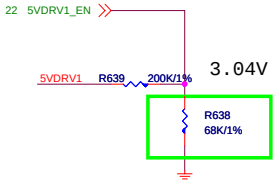




USB MODE

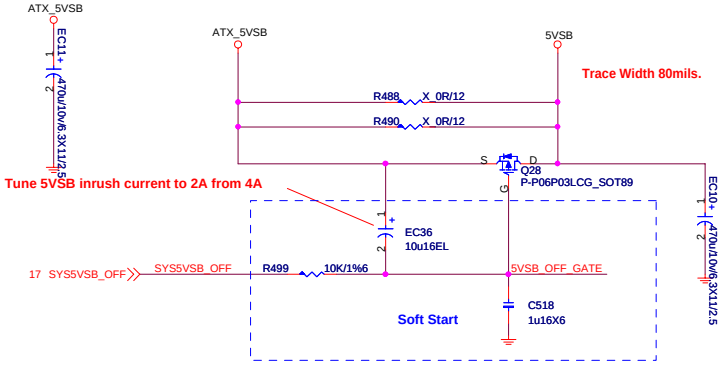


Patch coolermaster 700w power sequence



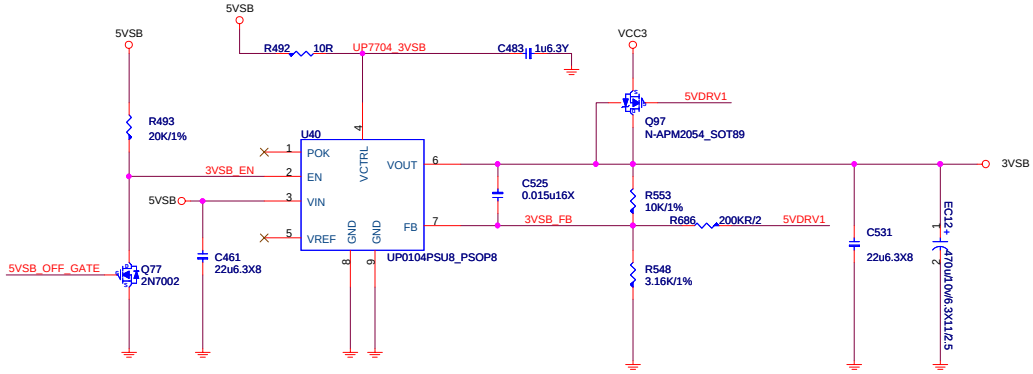
56K-->68K縮少料件

5VSB Power Switch



3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



MICRO-STAR INT'L CO.,LTD		
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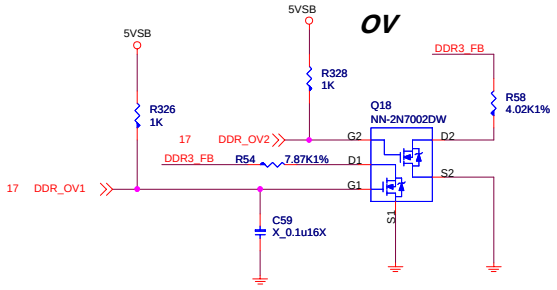
DDR3_1.5V 4.5A+7.5A+1A=13A

4.5A FOR CPU

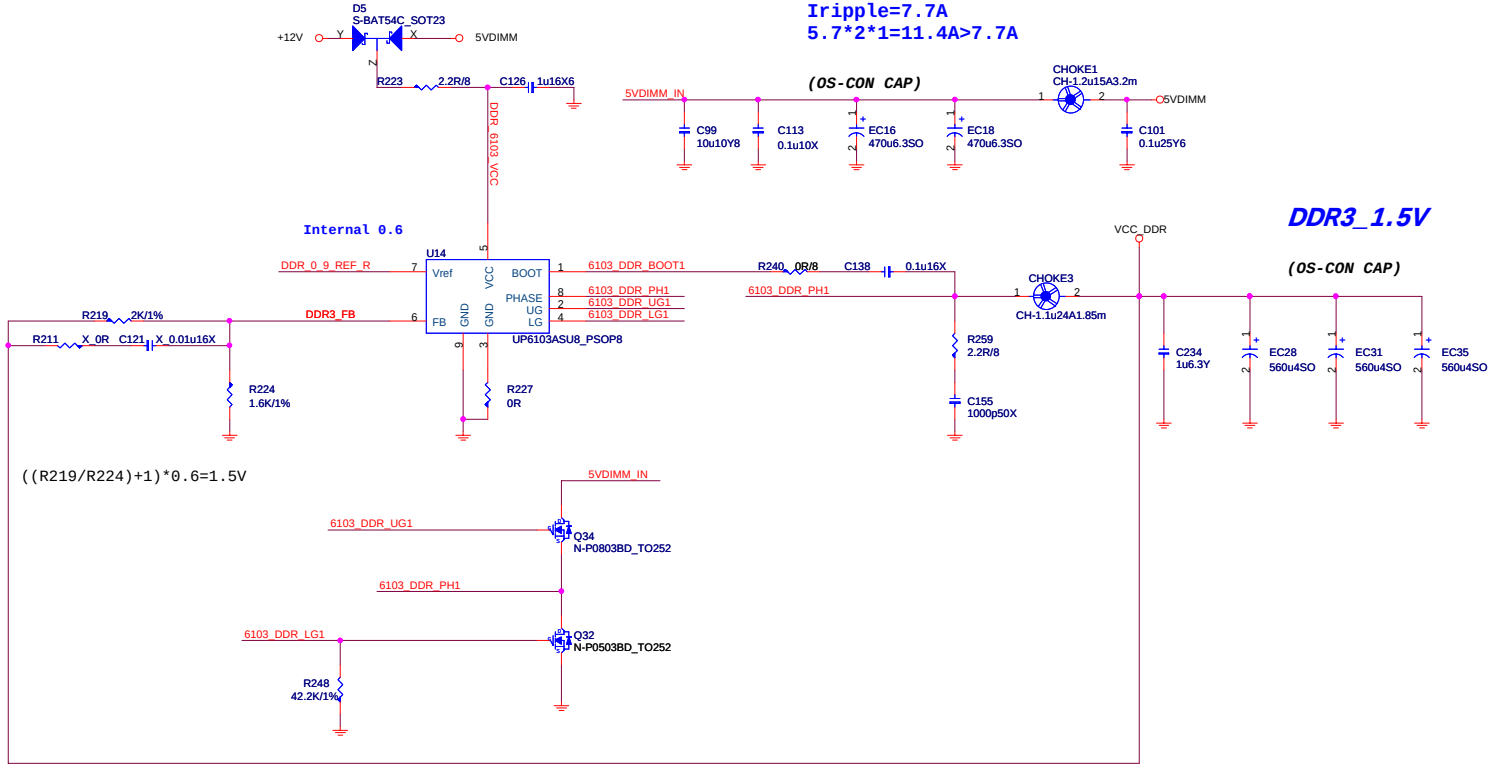
7.5A FOR 2DIMM

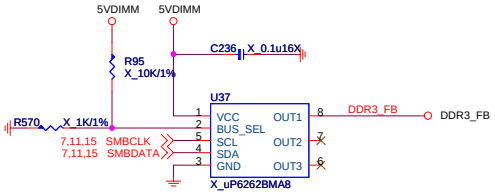
1A FOR DDR VTT

Iripple=7.7A
5.7*2*1=11.4A>7.7A



DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High



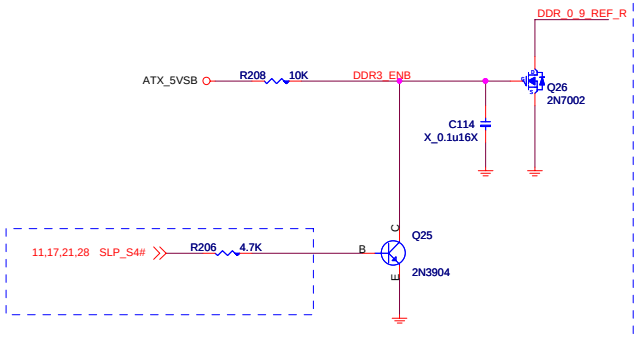


UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN

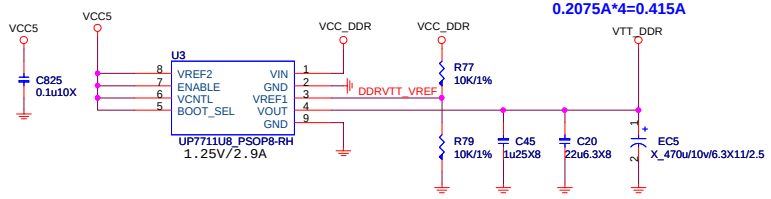
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

P.S. Only for meet Intel power down sequence.



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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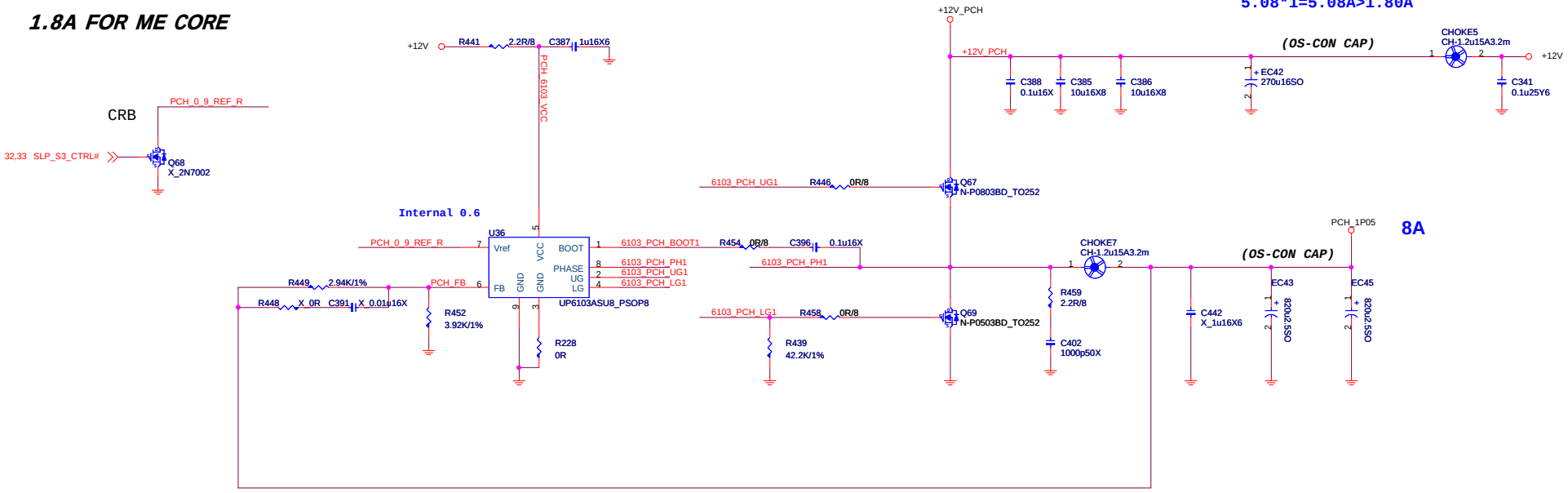
PCH Power:1.05V

PCH Core 6.2A+1.8A=8A

6.2A FOR PCH

1.8A FOR ME CORE

Iripple=1.80A
5.08*1=5.08A>1.80A



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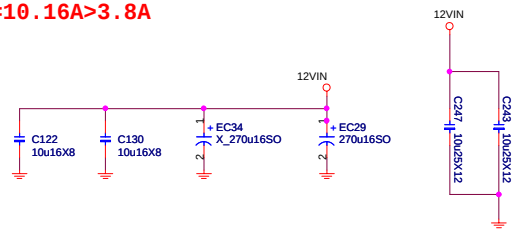
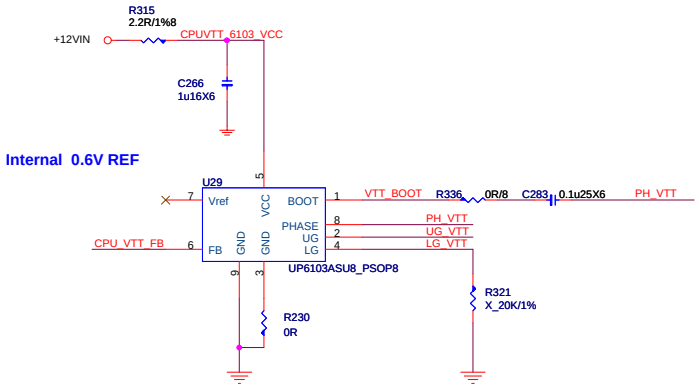
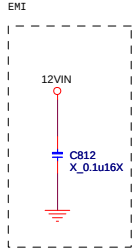
CPU_VTT:1.05/1.00

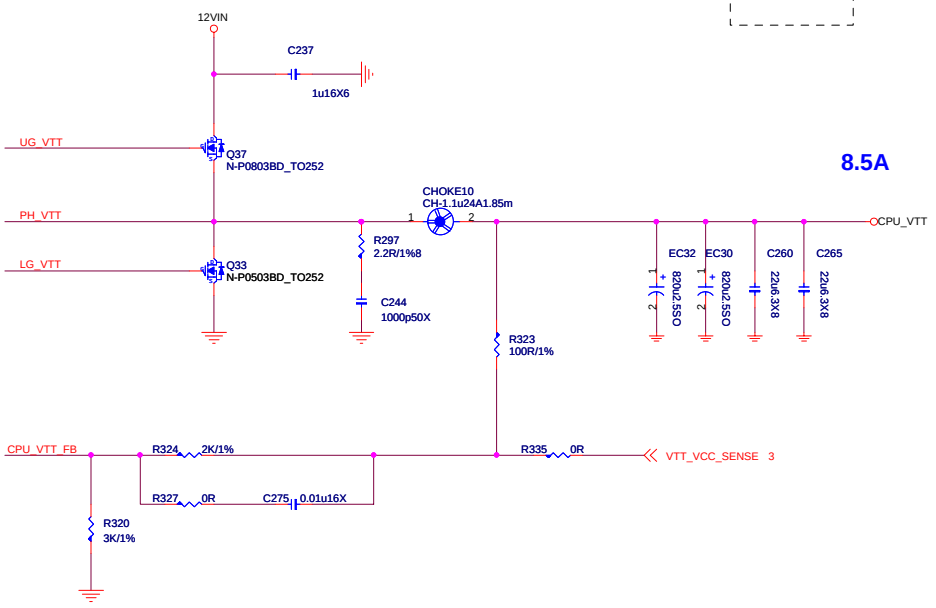
CPU VTT 8.5A + SA Core =8.8A =17.3A

Iripple=1.92(vtt)+1.88(sa)
5.08*2=10.16A>3.8A



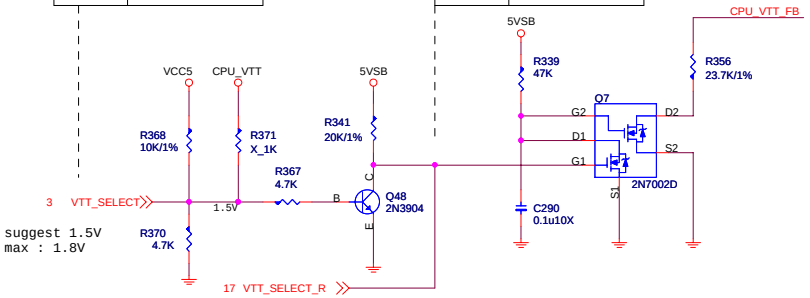






VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V



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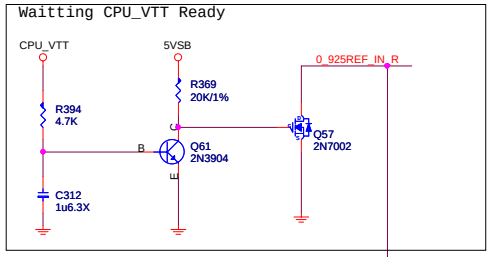
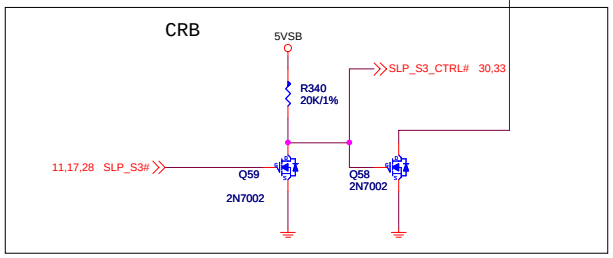
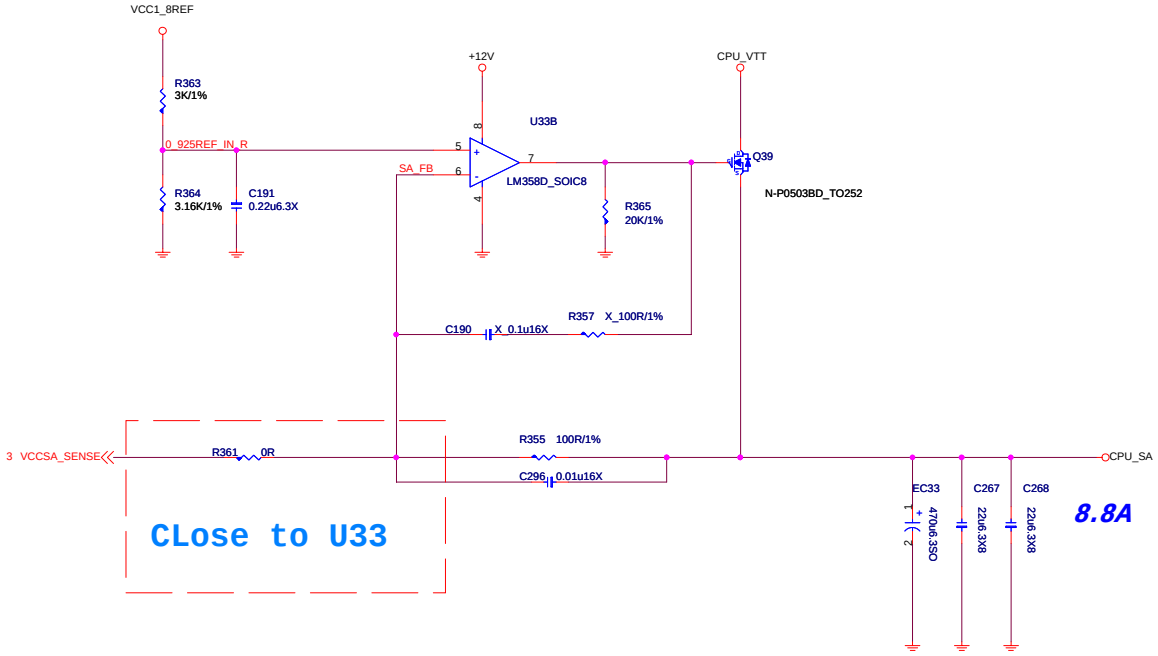
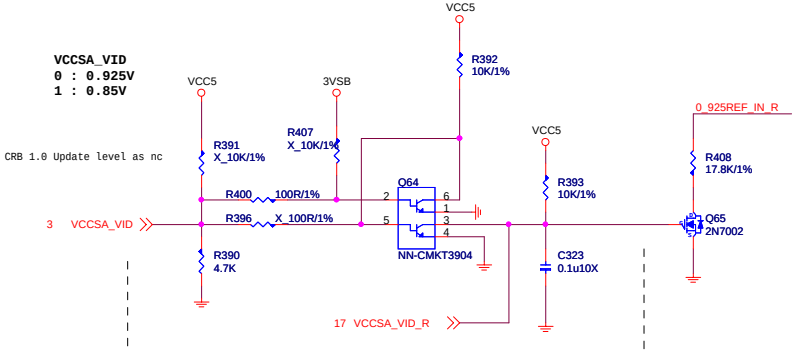
CPU_SA:0.925/0.85

SA Core =8.8A









VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V

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VRMPWRGD LEVEL SHIFT

3000mil < L < 6000mil
4mil / 20mil
55 ohm Impedence
must be Referenced GND

RT5 Close CHOKE2

RT6 Close CHOKE16

RT8 Close CHOKE2

PS1/2--uP1625P
STB/SV0UT--uP1625Q

uT501AQGK

to 6262短腿

CRB

Use PWM IC I32-UT5010C-U33(old) --> stuff JVboot1/R932/R933/J1/R943/R956
Use PWM IC I32-UT5011C-U33(new) --> stuff J1/R933/R921/R924/R417/Q89

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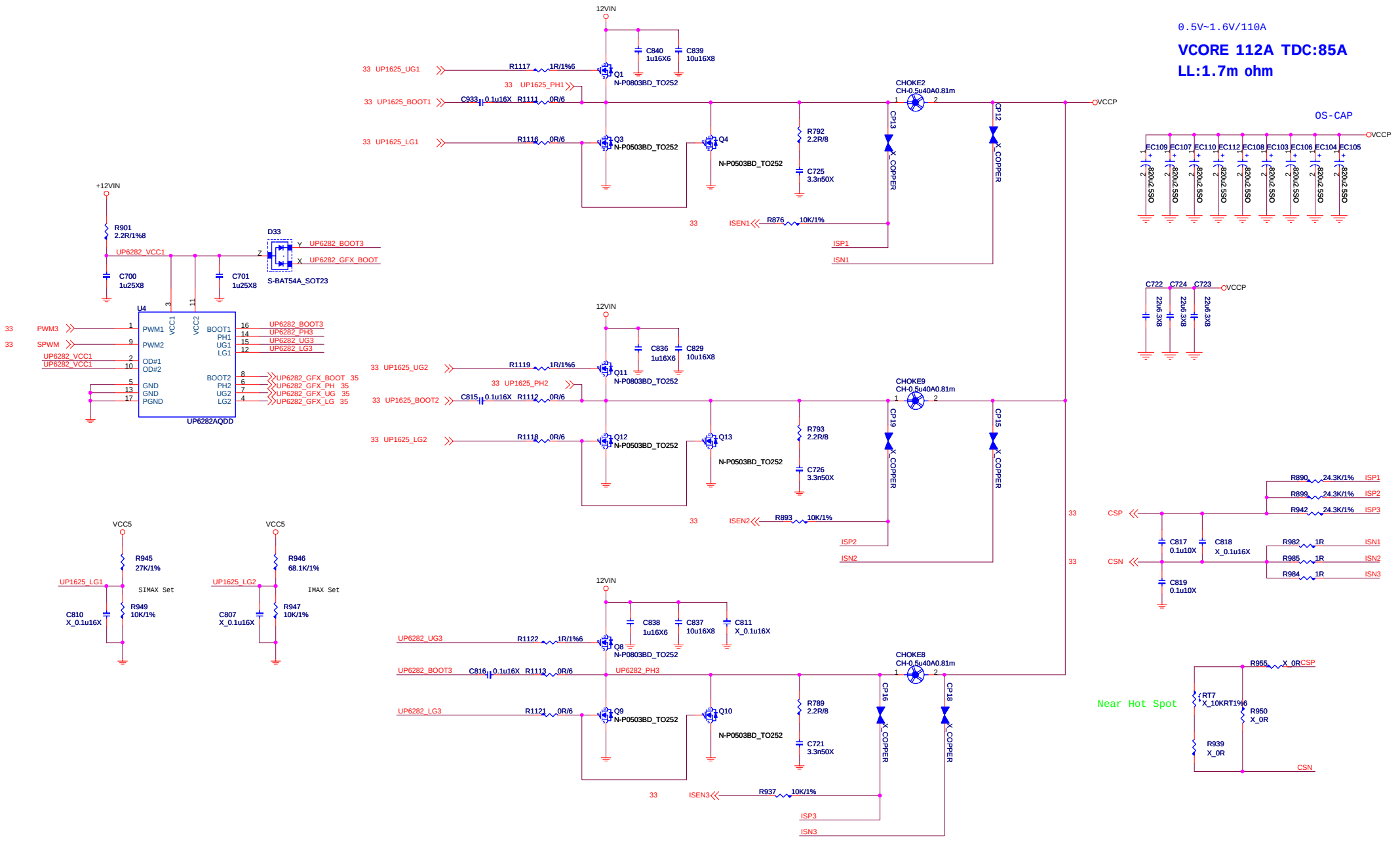
0.5V~1.6V/110A

VCORE 112A TDC:85A

LL:1.7m ohm



MSI	MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: UP6234 6-Phase CPU	Rev: 2.3
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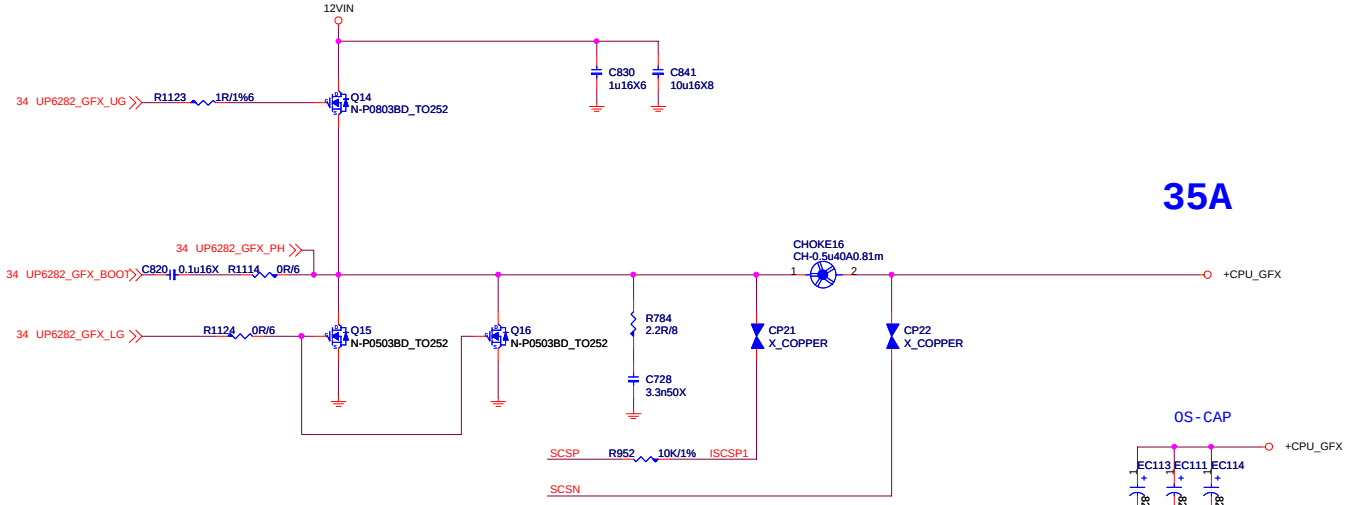

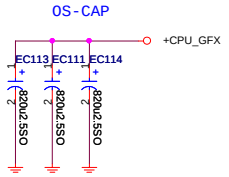

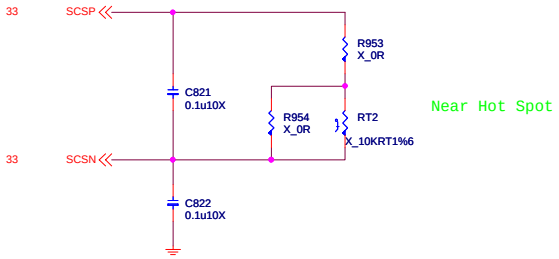

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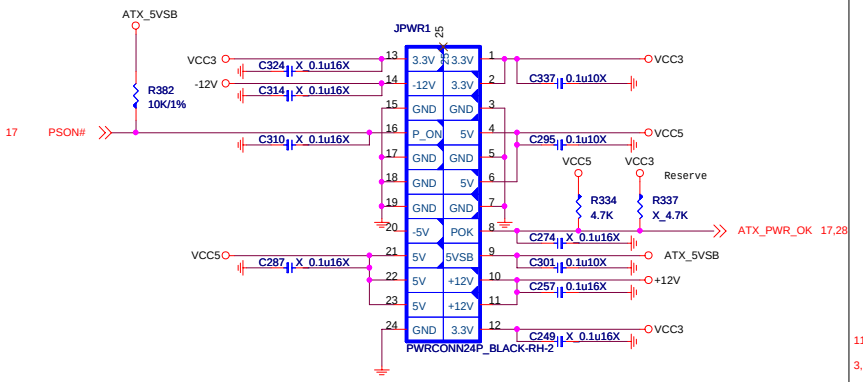
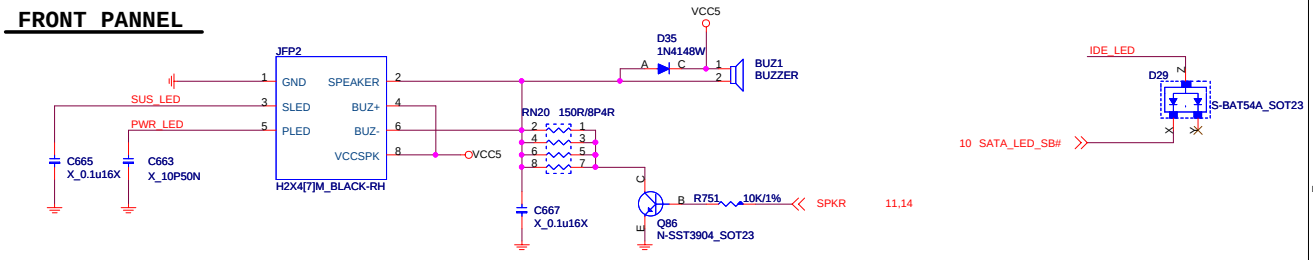
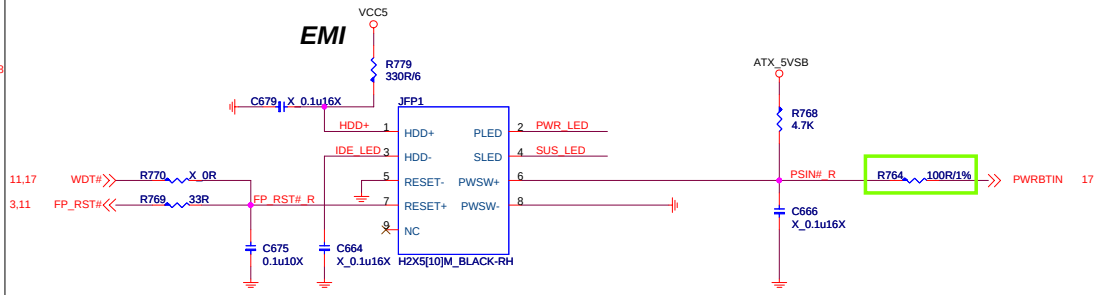
ATX POWER CONNECTOR



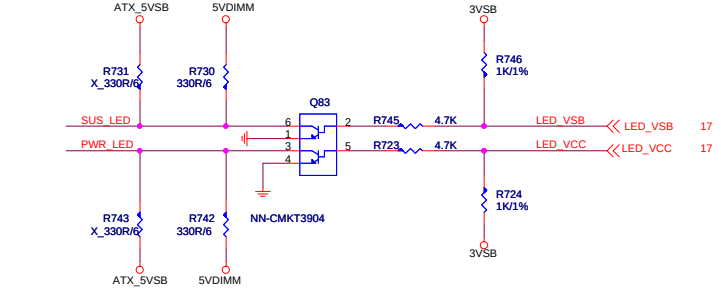
FRONT PANNEL



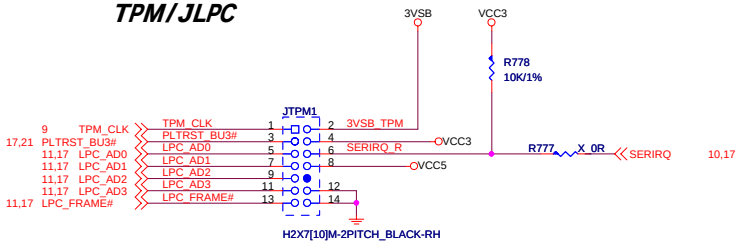
EMI



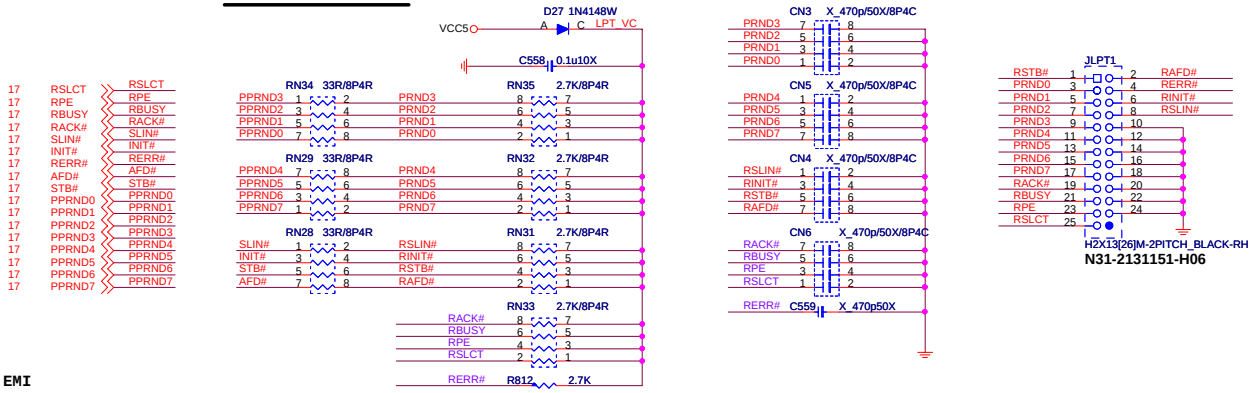
LED (for Fintek 71869)



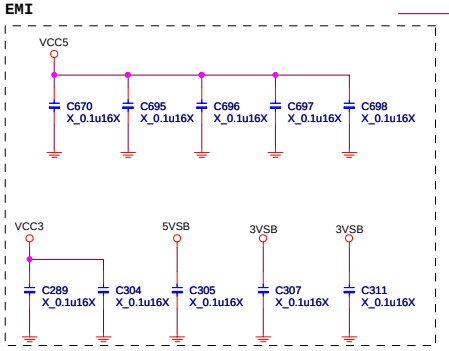
TPM/JLPC



PARALLAL PORT



EMI



MICRO-STAR INT'L CO.,LTD

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PCB1

7680-23

PK9-0768023-G37,精成,23,寶安恩斯邁廠(MSIS),4,Coffee
PK9-0768023-E48,競華,23,寶安恩斯邁廠(MSIS),4,Coffee

	OPT	Configure	BOM	Function
先轉BOM	A	CFG-H61MU_E35	601-7680-17S	MS-7680 23 OPT:A H61MU-E35 (B3) Intel H61 B3 +2*DDR3+1*PCIe16, 2*PCIe1,1*PCI+DVI/D-sub/HDMI+4*SATAII+2*USB3+10*USB2+HD8Ch Audio+Gblan,EuP,RoHS
先轉BOM	B	CFG-H67MA-E35	601-7680-18S	MS-7680 23 OPT:B H67MA-E35 (B3) Intel H67 B3+2DDR3+1PCIe16,2PCIe1, 1PCI+DVI/D-sub/HDMI+4*SATAII+2SATAIII+2*USB3+10*USB2+HD8Ch Audio+Gb lan,EuP,RoHS

H67 OPT.

U100
CPT H67
Cougar point H67(B3)

SATA10_11
SATA CON.
SATA14PM_BEIGE-ST-RH

AUDIO CON OPT.

AUDIO10
AUDIO
PK/GR/BU/GY/OR/BL

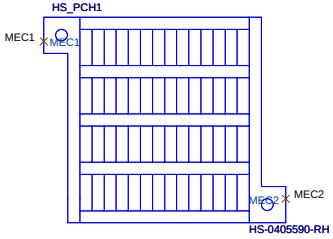
EL/OS OPT.

EC200 EC — 270uF16OS
EC201 EC — 100u16SO
EC202 EC — 470u6.3SO
EC203 EC — 100u25EL

LABEL OPT.

LA10 Label H61MU-E35. LABEL
LA11 Label H67MA-E35. LABEL
LA12 Label H67MS-E23. LABEL
LA13 Label H61M-P33 . LABEL
LA14 Label H61M-E33 . LABEL

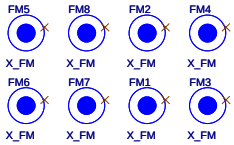
PCH XDP PWRGD/RESET



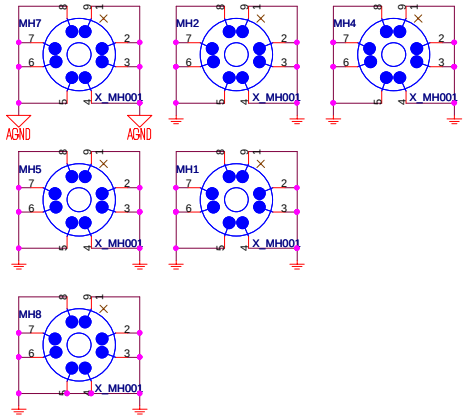
HS-0405590-RH

Simulation

Optical Fiducial Marks-120



Mounting Holes



BAT1_X1
BAT-BCR2032P-RH

RUB1 USB Rubber
RUB2 USB Rubber

CPU_H1
CPU 鍵座
E21-7557050-L06

LA1 Label H61M-E23. LABEL
HDMI_LA1 Label HDMI HDMI LABEL
THX1 Label THX X_THX LABEL

MICRO-STAR INT'L CO.,LTD

MS-7680

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