PCB Number: 14058-2
ECO# number : 776481

BOM Configuration
(R):Unmount
(G):GPU
(U):UMA
(X):Debug used
(T):Touch

PAGE	TITLE	Quantity
01	Cover Page	
02	Block Diagram	
03	CPU_DDRA_DDRB	
04	CPU_CFG/CLOCK	
05	CPU_PCIE	
06	CPU_ (VSS)	
07	CPU_(VCC_CORE/TP)	
08	CPU_(DDI/EDP)	
09	CPU_(POWER CAP1)	
10	CPU_(POWER CAP2)	
11	Reserved	
12	DDR3_SODIMM1	
13	DDR3_SODIMM2	
14	Reserved	
15	PCH(SPI/SMBUS/Audio/JTAG)	
16	PCH_(Clock)	
17	PCH (PCIE/SATA/USB)	
18	PCH (USB3.0/GPIO/HPD)	
19	PCH (GPIO)	
20	PCH_(Stap Pin)	
21	PCH_(Power)	
22	PCH_(Vss/TP)	
23	PCH_(Reserved)	
24	SIO_ITE8739	
25	Flash ROM/RTC	
26	FAN CIRCUITS/HOLE	
27	AUDIO ALC3661	
28	AMP TPA3131	
29	MIC/SPEAKER/AUDIO JACK	
30	Reserved	
31	LAN_RTL8111HSD	
32	RJ45+TRANSFORMER	
33	READER CONN	
34	USB2.0 CONN	
35	USB3.0 CONN	
36	Reserved	
37	Reserved	
38	WEBCAM	
39	Reserved	
40	Power enable & sequence	
41	DCIN	
42	Run PWR/USB/ DSWPWR	
43	CHARGER	
44	VCORE & V_GT(NCP81203)	
45	VCORE OUTPUT (NCP81151)	
46	V_GT OUTPUT(NCP81151)	
47	VCCSA(RT8237)	
48	VCCIO(RT8237)	
49	5V & 3.3V(RT8243A)	
50	DDR_PWR (RT8207M)	
51	PCH_1D0V(RT8237)	
52	1D8V(RT9025)	
53	12V(RT8289)	
54	Reserved	
55	Scalar	
56	HDMI OUT	
57	HDMI IN	
58	PANEL CONTROL	

PAGE	TITLE	Quantity
59	OZ554A LED Converter	
60	HDD/ODD	
61	NGFF CONN	
62	TOUCH	
63	Reserved	
64	LED BOARD/POWER BUTTON	
65	Reserved	
66	Reserved	
67	FFS	
68	DEBUG CONNECTOR	
69	Reserved	
70	Reserved	
71	Reserved	
72	Reserved	
73	Reserved	
74	Reserved	
75	Reserved	
76	GPU(1/5) PEG	
77	GPU(2/5)DIGITALOUT	
78	GPU(3/5):VRAM I/F	
79	GPU(4/5):GPIO/STRAP	
80	080_GPU(5/5):PWR/GND	
81	VRAM 1,2(1/2)	
82	VRAM 3,4(2/2)	
83	VRAM5,6(3/4)	
84	VRAM7,8(4/4)	
85	Reserved	
86	PWR_GPU_LDO	
87	Reserved	
88	PWR_GPU_CORE	
89	Reserved	
90	Reserved	
91	Reserved	
92	Reserved	
93	Reserved	
94	Reserved	
95	Reserved	
96	Reserved	
97	Reserved	
98	Reserved	
99	CPU_XDP	
100	Reserved	
101	Reserved	
102	POWER Sequence	
103	POWER BLOCK DIAGRAM	
104	POWER GOOD & RESET DIAGRAM	
105	CLOCK DIAGRAM	

<Variant Name>

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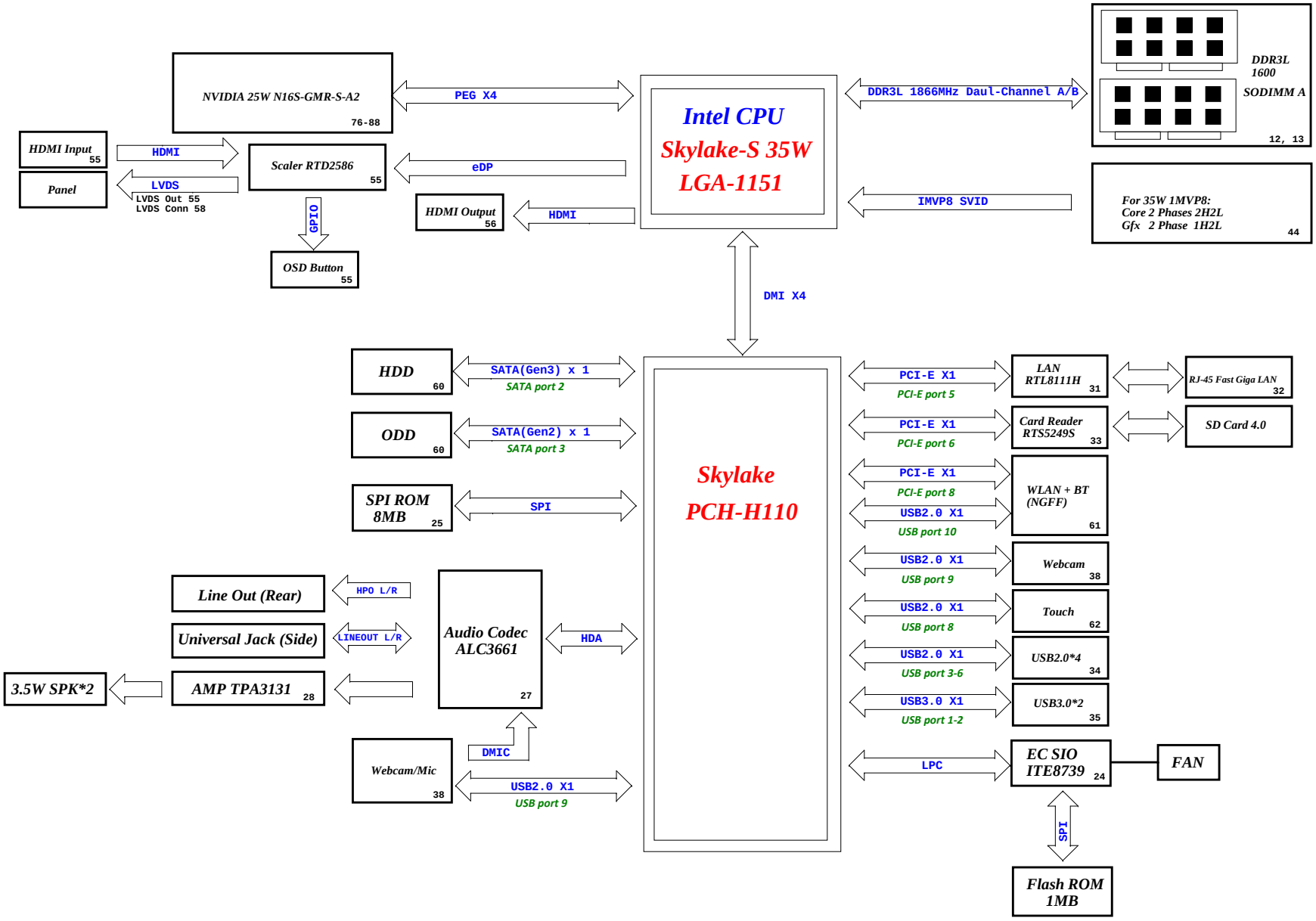
Title: 001_Cover Page

Size | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 1 of 107

Project code:3PD025010001
ECO# Number: 776481
PCB Number: 14058
Revision:A01

COLORADO MLK Skylake-S Block Diagram



CHARGER BQ24727RGRR-1-GP 43

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT8243AZQW-GP 49

INPUTS	OUTPUTS
DCBATOUT	V_3P3_A V_5P0_A

CPU Core Power NCP81203MNTXG-SI2-GP 44,45

INPUTS	OUTPUTS
DCBATOUT	V_CPU_CORE

GFX Core Power NCP81172MNTXG-GP-U 88

INPUTS	OUTPUTS
DCBATOUT	+V_GPU_CORE

DDR3L SUS TPS51716RUKR-GP 50

INPUTS	OUTPUTS
DCBATOUT	V_SM V_SM_VTT

CPU GT POWER NCP81203MNTXG-SI2-GP 44,46

INPUTS	OUTPUTS
DCBATOUT	V_CPU_GT

CPU 1.05V NCP5230MNTWG 47

INPUTS	OUTPUTS
DCBATOUT	V_CPU_SA

CPU 0.95V RT8237CZQW-2-GP 48

INPUTS	OUTPUTS
DCBATOUT	V_CPU_IO

PCH 1.0V S-1339D15-M5001-GP 51

INPUTS	OUTPUTS
DCBATOUT	V1P0_PCH_S5

FAN 12V RT8289GSP-GP 53

INPUTS	OUTPUTS
DCBATOUT	12V_S0

GPU 1.35V APW8713QBI-GP 86

INPUTS	OUTPUTS
DCBATOUT	+V_1P35_VGA

System switchs

INPUTS	OUTPUTS
V_5P0_A	SB5V
V_3P3_A	SB3V
V_5P0_A	VCC
V_3P3_A	VCC3
V_SM	+V_1P05_VGA

PCB LAYER

L1:Top
L2:GND
L3:Signal
L4:Signal
L5:GND
L6:Bottom

<Variant Name>

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Title: 002_Block Diagram

Size	Document Number	Rev
Custom	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 2 of 107

DDR DATA

12 M_DATA_A[0..63]
13 M_DATA_B[0..63]

12 M_DQS_A_DP[0..7]
12 M_DQS_A_DN[0..7]

13 M_DQS_B_DP[0..7]
13 M_DQS_B_DN[0..7]

DDR CMD/ADD

12 M_MAA_A[0..15]
13 M_MAA_B[0..15]

12 M_WE_A_N
12 M_CAS_A_N
12 M_RAS_A_N
12 M_SBS_A0
12 M_SBS_A1
12 M_SBS_A2

13 M_WE_B_N
13 M_CAS_B_N
13 M_RAS_B_N
13 M_SBS_B0
13 M_SBS_B1
13 M_SBS_B2

DDR CTRL

12 M_SCS_A_N0
12 M_SCS_A_N1

12 M_SCKE_A0
12 M_SCKE_A1

12 M_ODT_A0
12 M_ODT_A1

13 M_SCS_B_N0
13 M_SCS_B_N1

13 M_SCKE_B0
13 M_SCKE_B1

13 M_ODT_B0
13 M_ODT_B1

DDR CLOCK

12 CK_M_DDR0_A_DP
12 CK_M_DDR0_A_DN
12 CK_M_DDR1_A_DP
12 CK_M_DDR1_A_DN

13 CK_M_DDR0_B_DP
13 CK_M_DDR0_B_DN
13 CK_M_DDR1_B_DP
13 CK_M_DDR1_B_DN

DDR OTHERS

12 DIMM_DQ_CPU_VREF_A
13 DIMM_DQ_CPU_VREF_B
12 DIMM_CA_VREF_A
13 DIMM_CA_VREF_B

06/24 Allen modify

CPU1A — SKYLAKE — 1 OF 12 — LGA1151

DDR0_DQ0 … DDR0_DQ63 (AE38, AE37, AG38, AG37, AE39, AE40, AG39, AG40, AJ38, AJ37, AL38, AL37, AJ40, AJ39, AL39, AL40, AN39, AN40, AR39, AR40, AN37, AN38, AR37, AR38, AM40, AM39, AW37, AU38, AV35, AV36, AW39, AW40, AV37, AT36, AU36, AU35, AW38, AW36, AT35, AT34, AV34, AV33, AT32, AT33, AV32, AV31, AW34, AW33, AP32, AP33, AM34, AM33, AP31, AP30, AM31, AM30, AR31, AR30, AM29, AM28, AR29, AR28, AK31, AK30, AM27, AM26, AK29, AK28, AM25, AM24)

DDR0_CKP0 (AW18) CK_M_DDR0_A_DP
DDR0_CKN0 (AV18) CK_M_DDR0_A_DN
DDR0_CKP1 (AW17) CK_M_DDR1_A_DP
DDR0_CKN1 (AT17) CK_M_DDR1_A_DN
DDR0_CKP2 (AW16)
DDR0_CKN2 (AV16)
DDR0_CKP3 (AT16)
DDR0_CKN3 (AU16)

DDR0_CKE0 (AY24) M_SCKE_A0
DDR0_CKE1 (AW24) M_SCKE_A1
DDR0_CKE2 (AV24)
DDR0_CKE3 (AV25)

DDR0_CS#0 (AW12) M_SCS_A_N0
DDR0_CS#1 (AU11) M_SCS_A_N1
DDR0_CS#2 (AV12)
DDR0_CS#3 (AV30)

DDR0_ODT0 (AW11) M_ODT_A0
DDR0_ODT1 (AU14) M_ODT_A1
DDR0_ODT2 (AU13)
DDR0_ODT3 (AT13)

DDR0_BA0/DDR0_CAB4/DDR0_BA0 (AY13) M_SBS_A0
DDR0_BA1/DDR0_CAB5/DDR0_BA1 (AV15) M_SBS_A1
DDR0_BA2/DDR0_CAA5/DDR0_BG0 (AW23) M_SBS_A2

DDR0_RAS#/DDR0_CAB3/DDR0_MA16 (AW13) M_RAS_A_N
DDR0_WE#/DDR0_CAB2/DDR0_MA14 (AV14) M_WE_A_N
DDR0_CAS#/DDR0_CAB1/DDR0_MA15 (AY11) M_CAS_A_N

DDR0_MA0/DDR0_CAB9/DDR0_MA0 (AW15) M_MAA_A0
DDR0_MA1/DDR0_CAB8/DDR0_MA1 (AU18) M_MAA_A1
DDR0_MA2/DDR0_CAB7/DDR0_MA2 (AU17) M_MAA_A2
DDR0_MA3 (AT19) M_MAA_A3
DDR0_MA4 (AU20) M_MAA_A4
DDR0_MA5/DDR0_CAA0/DDR0_MA5 (AV20) M_MAA_A5
DDR0_MA6/DDR0_CAA2/DDR0_MA6 (AU21) M_MAA_A6
DDR0_MA7/DDR0_CAA4/DDR0_MA7 (AT22) M_MAA_A7
DDR0_MA8/DDR0_CAA3/DDR0_MA8 (AT20) M_MAA_A8
DDR0_MA9/DDR0_CAA1/DDR0_MA9 (AY14) M_MAA_A9
DDR0_MA10/DDR0_CAB7/DDR0_MA10 (AU22) M_MAA_A10
DDR0_MA11/DDR0_CAA7/DDR0_MA11 (AV22) M_MAA_A11
DDR0_MA12/DDR0_CAA6/DDR0_MA12 (AV17) M_MAA_A12
DDR0_MA13/DDR0_CAB6/DDR0_MA13 (AV23) M_MAA_A13
DDR0_MA14/DDR0_CAA9/DDR0_BG1 (AU24) M_MAA_A14
DDR0_MA15/DDR0_CAA8/DDR0_ACT# (AP22) M_MAA_A15

DDR0_PAR (AY15) TP_DDR0_PAR
DDR0_ALERT# (AT23) DDR0_ALERT#
R1 1 2 0R0402-PAD
TP1 TPAD28

THIS IS FOR RVP10 ONLY
Short PAD ,if Layout placement inpact

NOTE CMD SIGNALS FOR DIFFERENT MEMORY TECHINOLOGIES:
LEFT TO RIGHT: DDR3L/LPDDR3/DDR4

06/24 Allen modify

DDR0_DQSN0 (AC39) M_DQS_A_DN0
DDR0_DQSN1 (AP39) M_DQS_A_DN1
DDR0_DQSN2/DDR0_DQSN4 (AU39) M_DQS_A_DN2
DDR0_DQSN3/DDR0_DQSN5 (AW7) M_DQS_A_DN3
DDR0_DQSN4/DDR1_DQSN0 (AU3) M_DQS_A_DN4
DDR0_DQSN5/DDR1_DQSN1 (AN3) M_DQS_A_DN5
DDR0_DQSN6/DDR1_DQSN4 (AJ3) M_DQS_A_DN6
DDR0_DQSN7/DDR1_DQSN5 M_DQS_A_DN7

DDR0_DQSP0 (AC38) M_DQS_A_DP0
DDR0_DQSP1 (AP38) M_DQS_A_DP1
DDR0_DQSP2/DDR0_DQSP4 (AV39) M_DQS_A_DP2
DDR0_DQSP3/DDR0_DQSP5 (AV7) M_DQS_A_DP3
DDR0_DQSP4/DDR1_DQSP0 (AU2) M_DQS_A_DP4
DDR0_DQSP5/DDR1_DQSP1 (AN2) M_DQS_A_DP5
DDR0_DQSP6/DDR1_DQSP4 (AJ2) M_DQS_A_DP6
DDR0_DQSP7/DDR1_DQSP5 M_DQS_A_DP7

DDR0_DQSP8 (AV32) TP_DDR0_DQSP8
DDR0_DQSN8 (AU32) TP_DDR0_DQSN8
TP3 TPAD28
TP4 TPAD28

DDR0_ECC0 (AY33)
DDR0_ECC1 (AW33)
DDR0_ECC2 (AY31)
DDR0_ECC3 (AU31)
DDR0_ECC4 (AY28)
DDR0_ECC5 (AW31)
DDR0_ECC6 (AY30)
DDR0_ECC7 (A)

Can be left as no connects if no support ECC.

DDR CHANNEL A

SKYLAKE-1

06/24 Allen modify

CPU1B — SKYLAKE — 2 OF 12 — LGA1151

DDR1_DQ0/DDR0_DQ16 … DDR1_DQ63/DDR0_DQ48 (AD34, AD35, AD39, AD38, AE36, AE35, AE34, AE33, AK36, AK35, AL36, AL35, AK34, AK33, AK32, AK31, AN34, AN33, AP34, AP33, AN31, AN30, AP29, AP28, AN29, AN28, AL32, AL31, AL30, AL29, AK27, AK26, AL27, AL26, AJ27, AJ26, AG27, AG26, AG29, AG28, AE29, AE28, AE31, AE30, AG31, AG30, AJ31, AJ30, AJ29, AJ28, AG34, AG33, AG36, AG35, AJ34, AJ33, AJ36, AJ35)

DDR1_CKP0 (AM26) CK_M_DDR0_B_DP
DDR1_CKN0 (AM27) CK_M_DDR0_B_DN
DDR1_CKP1 (AP27) CK_M_DDR1_B_DP
DDR1_CKN1 (AP26) CK_M_DDR1_B_DN
DDR1_CKP2 (AN26)
DDR1_CKN2 (AN25)
DDR1_CKP3 (AP25)
DDR1_CKN3 (AP24)

DDR1_CKE0 (AY29) M_SCKE_B0
DDR1_CKE1 (AV29) M_SCKE_B1
DDR1_CKE2 (AW28)
DDR1_CKE3 (AU28)

DDR1_CS#0 (AP17) M_SCS_B_N0
DDR1_CS#1 (AN17) M_SCS_B_N1
DDR1_CS#2 (AN15)
DDR1_CS#3 (AM15)

DDR1_ODT0 (AM16) M_ODT_B0
DDR1_ODT1 (AL16) M_ODT_B1
DDR1_ODT2 (AP15)
DDR1_ODT3 (AL15)

DDR1_RAS#/DDR1_CAB3/DDR1_MA16 (AN19) M_RAS_B_N
DDR1_WE#/DDR1_CAB2/DDR1_MA14 (AL17) M_WE_B_N
DDR1_CAS#/DDR1_CAB1/DDR1_MA15 (AP18) M_CAS_B_N

DDR1_BA0/DDR1_CAB4/DDR1_BA0 (AL18) M_SBS_B0
DDR1_BA1/DDR1_CAB6/DDR1_BA1 (AM18) M_SBS_B1
DDR1_BA2/DDR1_CAA5/DDR1_BG0 (AW28) M_SBS_B2

DDR1_MA0/DDR1_CAB9/DDR1_MA0 (AL19) M_MAA_B0
DDR1_MA1/DDR1_CAB8/DDR1_MA1 (AL22) M_MAA_B1
DDR1_MA2/DDR1_CAB5/DDR1_MA2 (AM22) M_MAA_B2
DDR1_MA3 (AP22) M_MAA_B3
DDR1_MA4 (AL21) M_MAA_B4
DDR1_MA5/DDR1_CAA0/DDR1_MA5 (AW26) M_MAA_B5
DDR1_MA6/DDR1_CAA2/DDR1_MA6 (AY26) M_MAA_B6
DDR1_MA7/DDR1_CAA4/DDR1_MA7 (AU26) M_MAA_B7
DDR1_MA8/DDR1_CAA3/DDR1_MA8 (AW27) M_MAA_B8
DDR1_MA9/DDR1_CAA1/DDR1_MA9 (AP16) M_MAA_B9
DDR1_MA10/DDR1_CAB7/DDR1_MA10 (AU27) M_MAA_B10
DDR1_MA11/DDR1_CAA7/DDR1_MA11 (AV27) M_MAA_B11
DDR1_MA12/DDR1_CAA6/DDR1_MA12 (AR15) M_MAA_B12
DDR1_MA13/DDR1_CAB0/DDR1_MA13 (AY25) M_MAA_B13
DDR1_MA14/DDR1_CAA9/DDR1_BG1 (AU25) M_MAA_B14
DDR1_MA15/DDR1_CAA8/DDR1_ACT# (AL20) M_MAA_B15

DDR1_PAR (AY24) TP_DDR1_PAR
DDR1_ALERT# (AY25) DDR1_ALERT#
R2 1 2 0R0402-PAD
TP2 TPAD28

THIS IS FOR RVP10 ONLY
Short PAD ,if Layout placement inpact

NOTE CMD SIGNALS FOR DIFFERENT MEMORY TECHINOLOGIES:
LEFT TO RIGHT: DDR3L/LPDDR3/DDR4

06/24 Allen modify

DDR1_DQSN0/DDR0_DQSN2 (AF34) M_DQS_B_DN0
DDR1_DQSN1/DDR0_DQSN3 (AK37) M_DQS_B_DN1
DDR1_DQSN2/DDR0_DQSN6 (AN35) M_DQS_B_DN2
DDR1_DQSN3/DDR0_DQSN7 (AN24) M_DQS_B_DN3
DDR1_DQSN4/DDR1_DQSN2 (AR35) M_DQS_B_DN4
DDR1_DQSN5/DDR1_DQSN3 (AM35) M_DQS_B_DN5
DDR1_DQSN6 (AD37) M_DQS_B_DN6
DDR1_DQSN7 M_DQS_B_DN7

DDR1_DQSP0/DDR0_DQSP2 (AF35) M_DQS_B_DP0
DDR1_DQSP1/DDR0_DQSP3 (AL33) M_DQS_B_DP1
DDR1_DQSP2/DDR0_DQSP6 (AP37) M_DQS_B_DP2
DDR1_DQSP3/DDR0_DQSP7 (AN22) M_DQS_B_DP3
DDR1_DQSP4/DDR1_DQSP2 (AN37) M_DQS_B_DP4
DDR1_DQSP5/DDR1_DQSP3 (AP21) M_DQS_B_DP5
DDR1_DQSP6 (AL37) M_DQS_B_DP6
DDR1_DQSP7 (AG17) M_DQS_B_DP7

DDR1_DQSP8 (AN20) TP_DDR1_DQSP8
DDR1_DQSN8 (AN21) TP_DDR1_DQSN8
TP5 TPAD28
TP6 TPAD28

DDR1_ECC0 (AF25)
DDR1_ECC1 (AM24)
DDR1_ECC2 (AP23)
DDR1_ECC3 (AP24)
DDR1_ECC4 (AF23)
DDR1_ECC5 (AL25)
DDR1_ECC6 (AL26)
DDR1_ECC7 (A)

Can be left as no connects if no support ECC.

DDR CHANNEL B

SKYLAKE-1

DDR_VREF_CA (AB40)
DDR0_VREF_DQ (AC40)
DDR1_VREF_DQ (AC39)
DIMM_CA_CPU_VREF_A
DIMM_DQ_CPU_VREF_A
DIMM_DQ_CPU_VREF_B

C2 SCD1U16V2KX-3DLGP
C1 SCD1U16V2KX-3DLGP

DIMM_CA_CPU_VREF_A
R3 1 2 2R2F-GP
DIMM_CA_VREF_A
C3 SCD022U16V2KX-3DLGP
DIMM_CA_CPU_VREF_RC
R4 1 2 2R2F-GP
DIMM_CA_VREF_B
R5 240/8R2F-L-GP

All types of DIMMs are DDR3L

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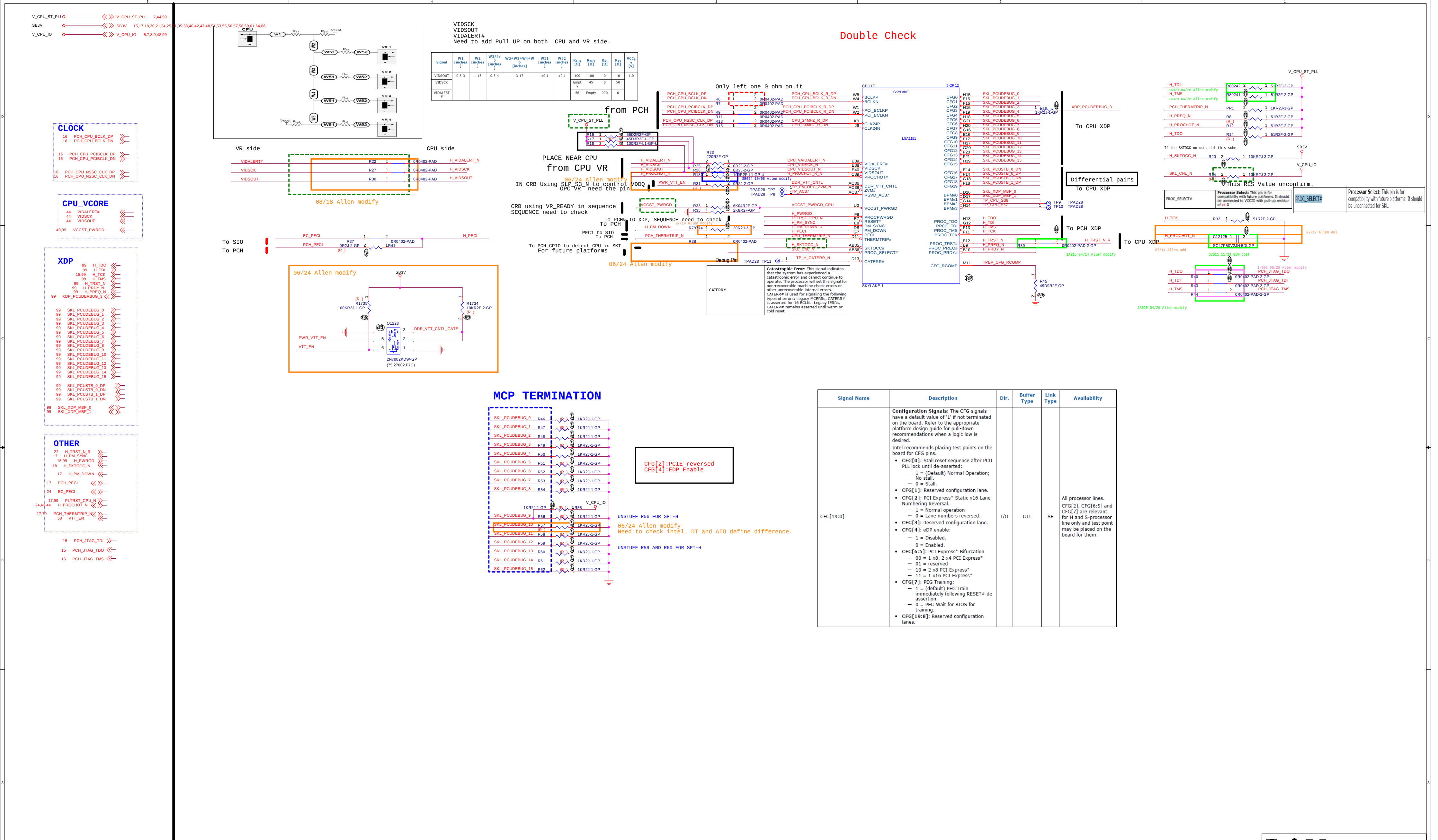
Title: 003_CPU_DDRA_DDR8

Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 3 of 107



Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

CATERR#	**Catastrophic Error:** This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this signal for non-recoverable machine check errors or other unrecoverable internal errors. CATERR# is used for signaling the following types of errors: Legacy MCERRs, CATERR# is asserted for 16 BCLKs. Legacy IERRs, CATERR# remains asserted until warm or cold reset.

PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be connected to VCCIO with pull-up resistor of xx Ω
PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for SKL.

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]**: Reserved configuration lane. • **CFG[4]**: eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]**: PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]**: Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

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Title		
004_CPU_CFG/CLOCK		
Size: D	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 4 of 107	

V_CPU_IO — V_CPU_IO 4,7,8,9,40,99

Already SWAP

CHECK PCIEX8 swap ?????

DMI

17 DMI_IT_MR_DP[0..3]
17 DMI_IT_MR_DN[0..3]
17 DMI_MT_IR_DP[0..3]
17 DMI_MT_IR_DN[0..3]

76 PEG_RXN[7..0]
PEG_RXN7 PEG_RXN6 PEG_RXN5 PEG_RXN4 PEG_RXN3 PEG_RXN2 PEG_RXN1 PEG_RXN0

76 PEG_RXP[7..0]
PEG_RXP7 PEG_RXP6 PEG_RXP5 PEG_RXP4 PEG_RXP3 PEG_RXP2 PEG_RXP1 PEG_RXP0

CPU1C 3 OF 12
SKYLAKE
LGA1151

B8 PEG_RXP0	B7 PEG_RXN0	A5 PEG_TXP0	A6 PEG_TXN0
C7 PEG_RXP1	C6 PEG_RXN1	B4 PEG_TXP1	B5 PEG_TXN1
D6 PEG_RXP2	D5 PEG_RXN2	C3 PEG_TXP2	C4 PEG_TXN2
E5 PEG_RXP3	E4 PEG_RXN3	D2 PEG_TXP3	D3 PEG_TXN3
F6 PEG_RXP4	F5 PEG_RXN4	E1 PEG_TXP4	E2 PEG_TXN4
G5 PEG_RXP5	G4 PEG_RXN5	F2 PEG_TXP5	F3 PEG_TXN5
H6 PEG_RXP6	H5 PEG_RXN6	G1 PEG_TXP6	G2 PEG_TXN6
J5 PEG_RXP7	J4 PEG_RXN7	H2 PEG_TXP7	H3 PEG_TXN7
K6 PEG_RXP8	K5 PEG_RXN8	J1 PEG_TXP8	J2 PEG_TXN8
L5 PEG_RXP9	L4 PEG_RXN9	K2 PEG_TXP9	K3 PEG_TXN9
M6 PEG_RXP10	M5 PEG_RXN10	L1 PEG_TXP10	L2 PEG_TXN10
N5 PEG_RXP11	N4 PEG_RXN11	M2 PEG_TXP11	M3 PEG_TXN11
P6 PEG_RXP12	P5 PEG_RXN12	N1 PEG_TXP12	N2 PEG_TXN12
R5 PEG_RXP13	R4 PEG_RXN13	P2 PEG_TXP13	P3 PEG_TXN13
T6 PEG_RXP14	T5 PEG_RXN14	R2 PEG_TXP14	R1 PEG_TXN14
U5 PEG_RXP15	U4 PEG_RXN15	T2 PEG_TXP15	T3 PEG_TXN15

PEG_RXP7 PEG_RXN7 — PEG_C_TXP7 PEG_C_TXN7
PEG_RXP6 PEG_RXN6 — PEG_C_TXP6 PEG_C_TXN6
PEG_RXP5 PEG_RXN5 — PEG_C_TXP5 PEG_C_TXN5
PEG_RXP4 PEG_RXN4 — PEG_C_TXP4 PEG_C_TXN4
PEG_RXP3 PEG_RXN3 — PEG_C_TXP3 PEG_C_TXN3
PEG_RXP2 PEG_RXN2 — PEG_C_TXP2 PEG_C_TXN2
PEG_RXP1 PEG_RXN1 — PEG_C_TXP1 PEG_C_TXN1
PEG_RXP0 PEG_RXN0 — PEG_C_TXP0 PEG_C_TXN0

V_CPU_IO
R63 24D9R2F-L-GP
PEG_COMP L7
PEG_RCOMP

DMI_IT_MR_DP0 Y3	DMI_IT_MR_DN0 Y4	DMI_RXP0 DMI_RXN0	DMI_TXP0 AC2 DMI_TXN0 AC1 DMI_MT_IR_DP0 DMI_MT_IR_DN0
DMI_IT_MR_DP1 AA4	DMI_IT_MR_DN1 AA5	DMI_RXP1 DMI_RXN1	DMI_TXP1 AD3 DMI_TXN1 AD2 DMI_MT_IR_DP1 DMI_MT_IR_DN1
DMI_IT_MR_DP2 AB4	DMI_IT_MR_DN2 AB3	DMI_RXP2 DMI_RXN2	DMI_TXP2 AE2 DMI_TXN2 AE1 DMI_MT_IR_DP2 DMI_MT_IR_DN2
DMI_IT_MR_DP3 AC4	DMI_IT_MR_DN3 AC5	DMI_RXP3 DMI_RXN3	DMI_TXP3 AF2 DMI_TXN3 AF3 DMI_MT_IR_DP3 DMI_MT_IR_DN3

SKYLAKE-1

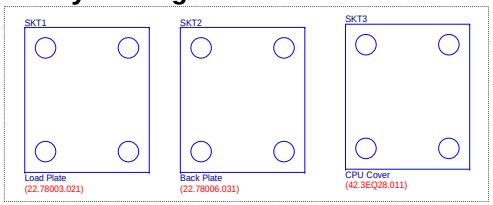
06/24 Allen add

PEG_TXN[7..0] 76
PEG_C_TXN7 (G_) C11898 1 — 1 SCD22U10V2KX-2-GP PEG_TXN7
PEG_C_TXN6 (G_) C11899 1 — 1 SCD22U10V2KX-2-GP PEG_TXN6
PEG_C_TXN5 (G_) C11900 1 — 1 SCD22U10V2KX-2-GP PEG_TXN5
PEG_C_TXN4 (G_) C11902 1 — 1 SCD22U10V2KX-2-GP PEG_TXN4
PEG_C_TXN3 (G_) C11904 1 — 1 SCD22U10V2KX-2-GP PEG_TXN3
PEG_C_TXN2 (G_) C11905 1 — 1 SCD22U10V2KX-2-GP PEG_TXN2
PEG_C_TXN1 (G_) C11907 1 — 1 SCD22U10V2KX-2-GP PEG_TXN1
PEG_C_TXN0 (G_) C11908 1 — 1 SCD22U10V2KX-2-GP PEG_TXN0

PEG_TXP[7..0] 76
PEG_C_TXP7 (G_) C12138 1 — 1 SCD22U10V2KX-2-GP PEG_TXP7
PEG_C_TXP6 (G_) C12139 1 — 1 SCD22U10V2KX-2-GP PEG_TXP6
PEG_C_TXP5 (G_) C12140 1 — 1 SCD22U10V2KX-2-GP PEG_TXP5
PEG_C_TXP4 (G_) C12141 1 — 1 SCD22U10V2KX-2-GP PEG_TXP4
PEG_C_TXP3 (G_) C12142 1 — 1 SCD22U10V2KX-2-GP PEG_TXP3
PEG_C_TXP2 (G_) C12143 1 — 1 SCD22U10V2KX-2-GP PEG_TXP2
PEG_C_TXP1 (G_) C12144 1 — 1 SCD22U10V2KX-2-GP PEG_TXP1
PEG_C_TXP0 (G_) C12145 1 — 1 SCD22U10V2KX-2-GP PEG_TXP0

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

Sandy Bridge Socket



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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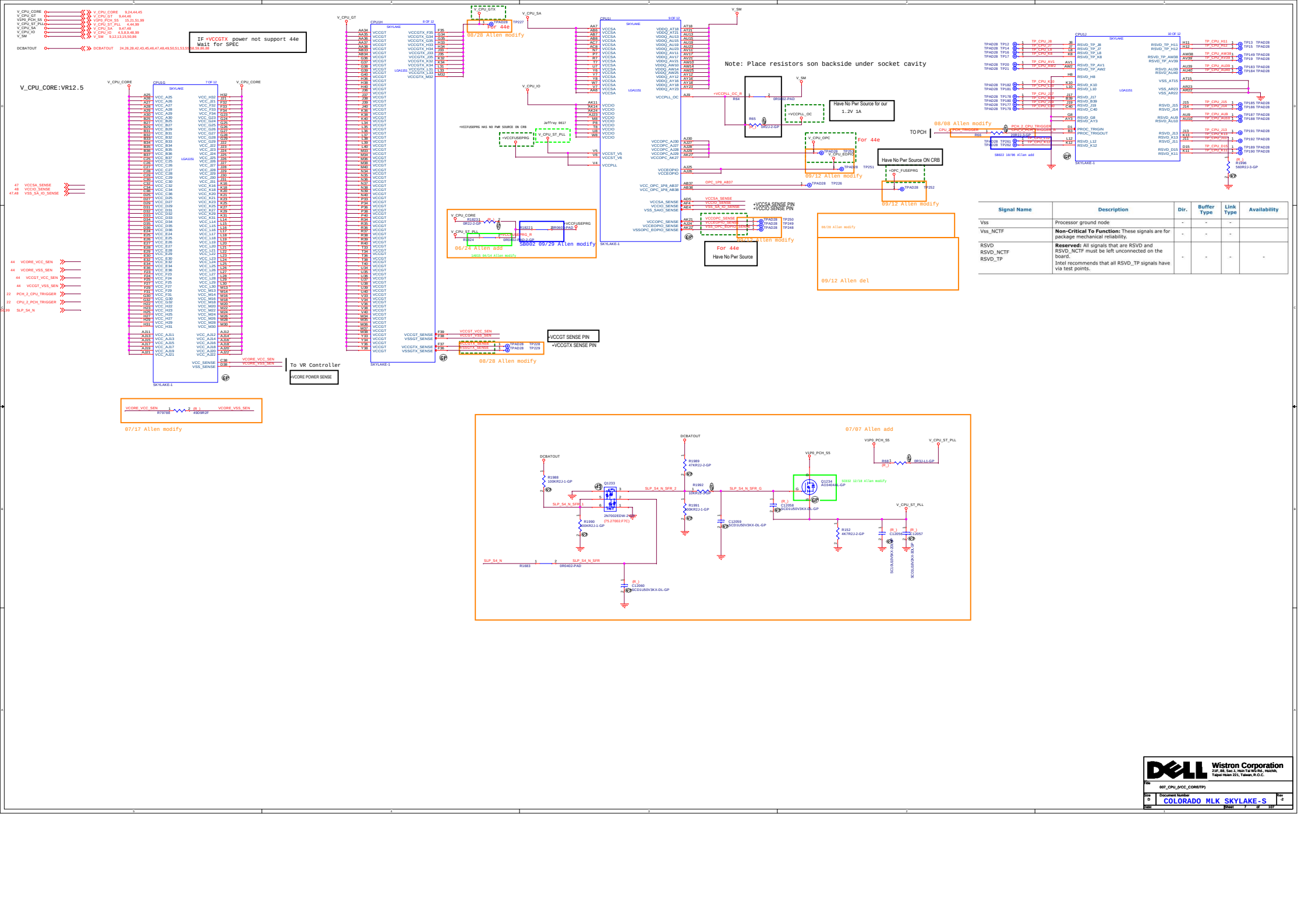
Title: 005_CPU_PCIE
Size: C
Document Number: COLORADO MLK SKYLAKE-S
Rev: -2
Date:
Sheet 5 of 107

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	006_CPU_(VSS)
Size: C	Document Number: COLORADO MLK SKYLAKE-S
Rev: -2	
Date:	Sheet 6 of 107



Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
Vss	Processor ground node	-	-	-	
Vss_NCTF	**Non-Critical To Function:** These signals are for package mechanical reliability.	-	-	-	
RSVD RSVD_NCTF RSVD_TP	**Reserved:** All signals that are RSVD and RSVD_NCTF must be left unconnected on the board. Intel recommends that all RSVD_TP signals have via test points.	-	-	-	-

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: 007_CPU_(VCC_CORE/TP)			
Size: D	Document Number: COLORADO MLK SKYLAKE-S		Rev: -2
Date:	Sheet 7 of 107		

V_CPU_IO → V_CPU_IO 4,5,7,9,48,99

HDMI PORT B

56 DDSP_B_TX_DN_0
56 DDSP_B_TX_DP_0
56 DDSP_B_TX_DN_1
56 DDSP_B_TX_DP_1
56 DDSP_B_TX_DN_2
56 DDSP_B_TX_DP_2
56 DDSP_B_TX_DN_3
56 DDSP_B_TX_DP_3

eDISPLAY PORT E

55 DPD_LANE0P
55 DPD_LANE0N
55 DPD_LANE1P
55 DPD_LANE1N
55 DPD_LANE2P
55 DPD_LANE2N
55 DPD_LANE3P
55 DPD_LANE3N
55 DPD_AUXN
55 DPD_AUXP

AUDIO

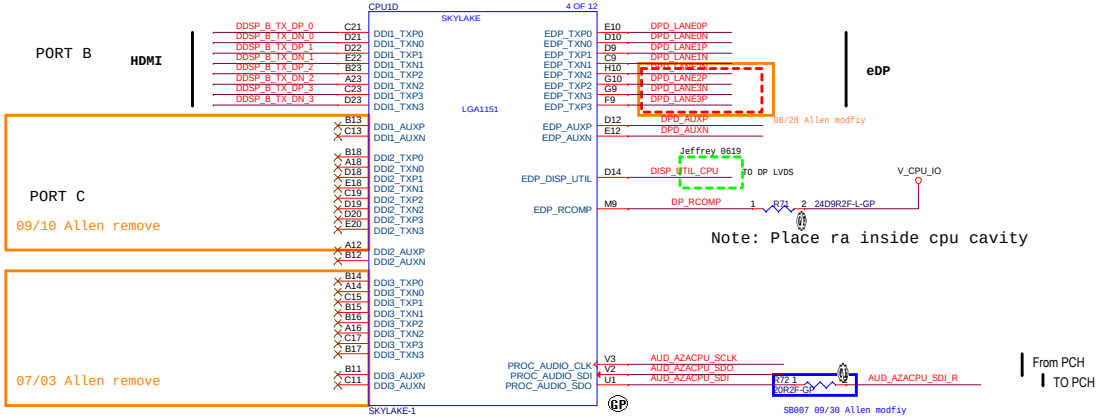
15 AUD_AZACPU_SCLK
15 AUD_AZACPU_SDO
15 AUD_AZACPU_SDI_R
55 DISP_UTIL_CPU

- H/S-processor line processors supports eDP and up to 3 DDI supporting DP/HDMI.

In CRB,
DDI1 for DP
DDI2 dor HDMI
DDI3 for DP HDMI combo
DDI4 for eDP

x4 eDP
Or
x2 eDP + x2 DP

DDI B
(X4 DP/HDMI)
DDI C
(X4 DP/HDMI)
DDI D
(X4 DP/HDMI)



<Variant Name>

Wistron Corporation
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Title: 008_CPU_(DDI/EDP)

Size: C | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 8 of 107

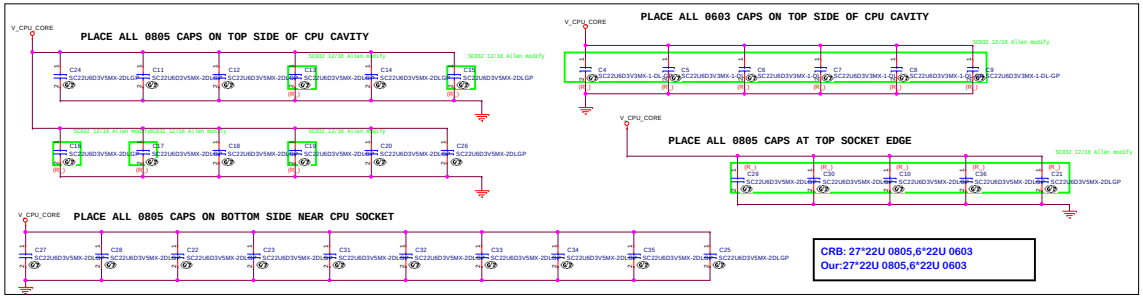
V_CPU_CORE — V_CPU_CORE 7,24,44,45

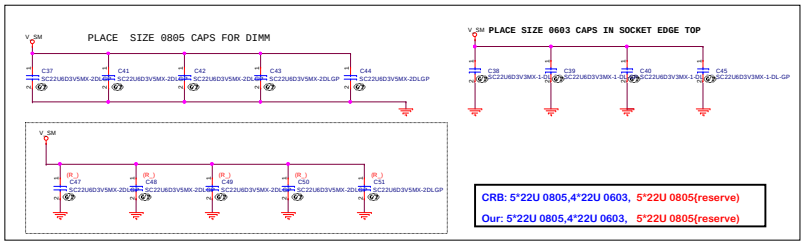
V_SM — V_SM 7,12,13,15,50,86

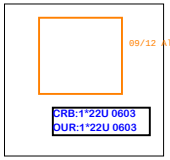
V_CPU_GT — V_CPU_GT 7,44,46

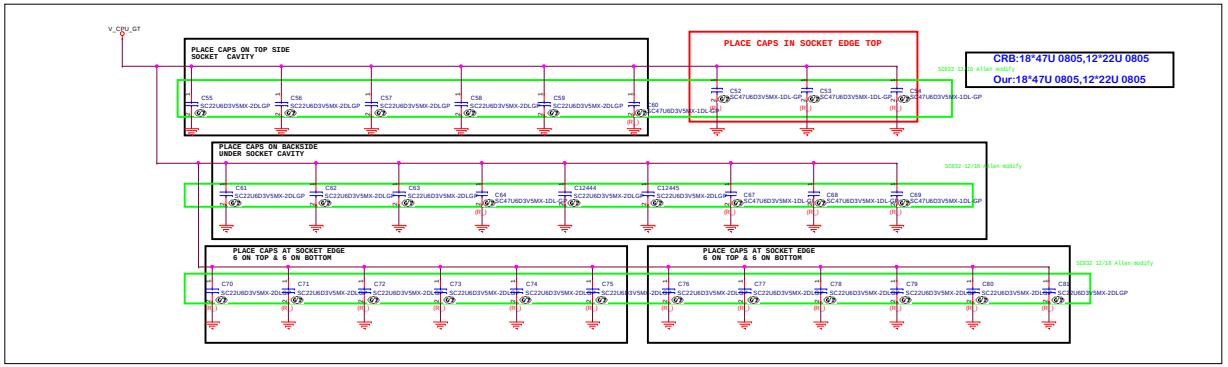
V_CPU_SA — V_CPU_SA 7,47,48

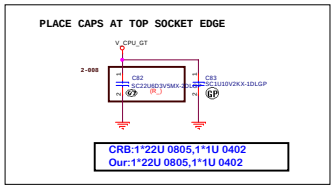
V_CPU_IO — V_CPU_IO 4,5,7,8,48,99

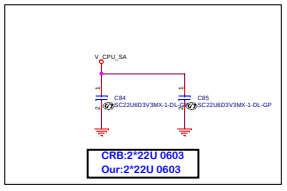


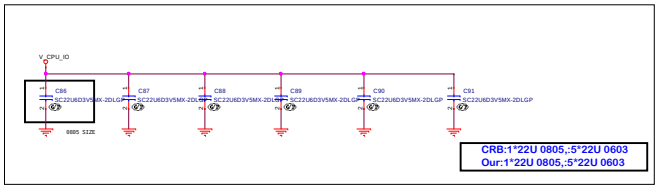












Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 009_CPU_(POWER CAP1)

Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 9 of 107

For 44e

GTTX
CRB:4*22U 0603,10*47U 0805

For 44e

V_CPU_OPC
CRB:6*22U 0603

For 44e

V_CPU_EOPIO
CRB:7*22U 0603

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 010_CPU_(POWER CAP2)

Size: A | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 10 of 107

<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
D	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 11 of 107

V_SM
V_SM_VTT
VCC3

DDR DATA

3 M_DATA_A[0..63]
3 M_DQS_A_DP[0..7]
3 M_DQS_A_DN[0..7]

DDR CMD/ADD

3 M_MAA_A[0..15]

3 M_WE_A_N
3 M_CAS_A_N
3 M_RAS_A_N

3 M_SBS_A0
3 M_SBS_A1
3 M_SBS_A2

DDR CTRL

3 M_SCS_A_N0
3 M_SCS_A_N1
3 M_SCKE_A0
3 M_SCKE_A1
3 M_ODT_A0
3 M_ODT_A1

DDR CLOCK

3 CK_M_DDR0_A_DP
3 CK_M_DDR0_A_DN
3 CK_M_DDR1_A_DP
3 CK_M_DDR1_A_DN

DDR OTHERS

13,15,55,67,79,99 SMB_DATA_MAIN
13,15,55,67,79,99 SMB_CLK_MAIN

13,55 DDR3_DRAMRST_N
3 DIMM_DQ_CPU_VREF_A
3 DIMM_CA_VREF_A

DIMM1

Reverse Connector
H=4mm

DIMM1

DDR3-204P-252-GP-U
(062.10011.0001)

TS4_DIMM0_1

Thermal EVENT

TS4_DIMM0_1
R73 10KR2J-3-GP
VCC3

SA0_DIM0
SA1_DIM0
R74 10KR2J-3-GP
R75 10KR2J-3-GP

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

DIMM VREF DQ A (To DIMM/CPU)

R76 1KR2F-3-GP
C106 SCD1U16V2KX-3DLGP
DIMM_DQ_R_VREF_A
R77 0R0402-PAD
DIMM_DQ_R_VREF_A
R78 1KR2F-3-GP
C107
C108
Joey_SB_9788
DIMM_DQ_CPU_VREF_A
R79 3K2F-GP
C111 SCD022U16V2KX-3DLGP
DIMM_DQ_CPU_VREF_A_1
R80 240R2F-L-GP

DIMM VREF CA A (To DIMM)

R82 1KR2F-3-GP
C113 SCD1U16V2KX-3DLGP
DIMM_CA_VREF_A_1
R83 0R0402-PAD
DIMM_CA_VREF_A
R84 1KR2F-3-GP
C114
C115

VCC3
C104 SCD1U16V2KX-3DLGP
C105 SCD1U16V2KX-3DLGP
V_SM_VTT
C109 SC4D7U6D3V3KX-DLGP
C110 SCD1U16V2KX-3DLGP

DDR3_DRAMRST_N
RB1 0R0402-PAD-2-GP
DDR3_DRAMRST_N_A_1
C112 SCD1U10V2KX-5DLGP
V_SM_VTT

V_SM
C92 C93 C94 C95 C96 C97 SC4D7U6D3V3KX-DLGP C98 SC4D7U6D3V3KX-DLGP C99 SC4D7U6D3V3KX-DLGP
SCD1U16V2KX-3DLGP

V_SM
C100
C101 SC4D7U6D3V3KX-DLGP
C102 SC4D7U6D3V3KX-DLGP
C103 SC4D7U6D3V3KX-DLGP
SCD1U16V2KX-3DLGP

Place Near Power Pin

Net	CAP	AMOUNT
+VDDQ	1uf 0402 X5R	4
+VDDQ	0.1uf 0402 X5R	5
+VDDQ_VTT	0.1uf 0402 X5R	1
+VDDQ_VTT	4.7uf 0603 X5R	1

<Variant Name>

Wistron Corporation
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File: 012_DDR3_SODIMM1

Size: A1 | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 12 of 100

Joey_SA_0415

VCC3 — VCC3 — 12,16,16,17,18,20,21,24,25,26,27,28,31,33,38,41,42,44,47,48,50,52,53,55,56,58,60,62,64,65,66,68,69,70,71,72,73,74,75,76,77,78,79,80,81,82,83,84,85,86,87,88,89,90,91,92,93,94,95,96,97,98,99,100

V_SM_VTT — V_SM_VTT — 12,50

V_SM — V_SM — 7,9,12,15,50,86

DDR DATA

3 M_DATA_B[0..63]
3 M_DQS_B_DP[0..7]
3 M_DQS_B_DN[0..7]

DDR CMD/ADD

3 M_MAA_B[0..15]
3 M_WE_B_N
3 M_CAS_B_N
3 M_RAS_B_N
3 M_SBS_B0
3 M_SBS_B1
3 M_SBS_B2

DDR CTRL

3 M_SCS_B_N0
3 M_SCS_B_N1
3 M_SCKE_B0
3 M_SCKE_B1
3 M_ODT_B0
3 M_ODT_B1

DDR CLOCK

3 CK_M_DDR0_B_DP
3 CK_M_DDR0_B_DN
3 CK_M_DDR1_B_DP
3 CK_M_DDR1_B_DN

DDR OTHERS

12,15 DDR3_DRAMRST_N
12,15,55,67,79,99 SMB_DATA_MAIN
12,15,55,67,79,99 SMB_CLK_MAIN

3 DIMM_CA_VREF_B
3 DIMM_DQ_CPU_VREF_B

DIMM2

Reverse Connector

H=8mm

DIMM2

M_MAA_B0 98 A0
M_MAA_B1 97 A1
M_MAA_B2 96 A2
M_MAA_B3 95 A3
M_MAA_B4 92 A4
M_MAA_B5 91 A5
M_MAA_B6 90 A6
M_MAA_B7 86 A7
M_MAA_B8 89 A8
M_MAA_B9 85 A9
M_MAA_B10 107 A10/AP
M_MAA_B11 84 A11
M_MAA_B12 83 A12
M_MAA_B13 119 A13
M_MAA_B14 80 A14
M_MAA_B15 78 A15
M_SBS_B2 79 A16/BA2

M_SBS_B0 109 BA0
M_SBS_B1 108 BA1

NP1 NP1
NP2 NP2

110 RAS# M_RAS_B_N
113 WE# M_WE_B_N
115 CAS# M_CAS_B_N

114 CS0# M_SCS_B_N0
121 CS1# M_SCS_B_N1

73 CKE0 M_SCKE_B0
74 CKE1 M_SCKE_B1

101 CK0 CK_M_DDR0_B_DP
103 CK0# CK_M_DDR0_B_DN

102 CK1 CK_M_DDR1_B_DP
104 CK1# CK_M_DDR1_B_DN

11 DM0
28 DM1
46 DM2
63 DM3
136 DM4
153 DM5
170 DM6
187 DM7

200 SDA SMB_DATA_MAIN
202 SCL SMB_CLK_MAIN

198 EVENT# TS#_DIMM0_1 12

199 VDDSPD VCC3

197 SA0 SA0_DIM1
201 SA1 SA1_DIM1

77 NC#1
122 NC#2
125 NC#/TEST

M_DATA_B0 5 DQ0
M_DATA_B1 7 DQ1
M_DATA_B2 15 DQ2
M_DATA_B3 17 DQ3
M_DATA_B4 4 DQ4
M_DATA_B5 6 DQ5
M_DATA_B6 16 DQ6
M_DATA_B7 18 DQ7
M_DATA_B8 21 DQ8
M_DATA_B9 23 DQ9
M_DATA_B10 33 DQ10
M_DATA_B11 35 DQ11
M_DATA_B12 22 DQ12
M_DATA_B13 24 DQ13
M_DATA_B14 34 DQ14
M_DATA_B15 36 DQ15
M_DATA_B16 39 DQ16
M_DATA_B17 41 DQ17
M_DATA_B18 51 DQ18
M_DATA_B19 53 DQ19
M_DATA_B20 40 DQ20
M_DATA_B21 42 DQ21
M_DATA_B22 50 DQ22
M_DATA_B23 52 DQ23
M_DATA_B24 57 DQ24
M_DATA_B25 59 DQ25
M_DATA_B26 67 DQ26
M_DATA_B27 69 DQ27
M_DATA_B28 56 DQ28
M_DATA_B29 58 DQ29
M_DATA_B30 68 DQ30
M_DATA_B31 70 DQ31
M_DATA_B32 129 DQ32
M_DATA_B33 131 DQ33
M_DATA_B34 141 DQ34
M_DATA_B35 143 DQ35
M_DATA_B36 130 DQ36
M_DATA_B37 132 DQ37
M_DATA_B38 140 DQ38
M_DATA_B39 142 DQ39
M_DATA_B40 147 DQ40
M_DATA_B41 149 DQ41
M_DATA_B42 157 DQ42
M_DATA_B43 159 DQ43
M_DATA_B44 146 DQ44
M_DATA_B45 148 DQ45
M_DATA_B46 158 DQ46
M_DATA_B47 160 DQ47
M_DATA_B48 163 DQ48
M_DATA_B49 165 DQ49
M_DATA_B50 175 DQ50
M_DATA_B51 177 DQ51
M_DATA_B52 164 DQ52
M_DATA_B53 166 DQ53
M_DATA_B54 174 DQ54
M_DATA_B55 176 DQ55
M_DATA_B56 181 DQ56
M_DATA_B57 183 DQ57
M_DATA_B58 191 DQ58
M_DATA_B59 193 DQ59
M_DATA_B60 180 DQ60
M_DATA_B61 182 DQ61
M_DATA_B62 192 DQ62
M_DATA_B63 194 DQ63

M_DQS_B_DN0 10 DQS0#
M_DQS_B_DN1 27 DQS1#
M_DQS_B_DN2 45 DQS2#
M_DQS_B_DN3 62 DQS3#
M_DQS_B_DN4 135 DQS4#
M_DQS_B_DN5 152 DQS5#
M_DQS_B_DN6 169 DQS6#
M_DQS_B_DN7 186 DQS7#

M_DQS_B_DP0 12 DQS0
M_DQS_B_DP1 29 DQS1
M_DQS_B_DP2 47 DQS2
M_DQS_B_DP3 64 DQS3
M_DQS_B_DP4 137 DQS4
M_DQS_B_DP5 154 DQS5
M_DQS_B_DP6 171 DQS6
M_DQS_B_DP7 188 DQS7

M_ODT_B0 116 ODT0
M_ODT_B1 120 ODT1

DIMM_CA_VREF_B 126 VREF_CA
DIMM_DQ_R_VREF_B 1 VREF_DQ

DDR3_DRAMRST_N_B_1 30 RESET#

203 VTT1
204 VTT2

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

VSS 2,3,8,9,13,14,19,20,25,26,31,32,37,38,43,44,48,49,54,55,60,61,65,66,71,72,127,128,133,134,139,144,145,150,151,155,156,161,162,167,168,172,173,178,179,184,185,189,190,195,196,205,206

SKT_DDR_204P_SMD

DDR3-204P-278-GP

(062.10011.00F1)

DDR3_DRAMRST_N — 1 R92 2 — 0R0402-PAD-2-GP — DDR3_DRAMRST_N_B_1

(R_) C136 V_SM_VTT — SCD1U10V2KX-5DLGP

TS#_DIMM0_1 — 12

TS#_DIMM0_1(EVENT#)must be connected to EC.(PH)

V_SM

C116 SCD1U16V2KX-3DLGP
C117 SCD1U16V2KX-3DLGP
C118 SCD1U16V2KX-3DLGP
C119 SCD1U16V2KX-3DLGP
C120 SCD1U16V2KX-3DLGP
C121 SC4D7U6D3V3KX-DLGP
C122 SC4D7U6D3V3KX-DLGP
C123 SC4D7U6D3V3KX-DLGP

V_SM

C124 SCD1U16V2KX-3DLGP
C125 SC4D7U6D3V3KX-DLGP
C126 SC4D7U6D3V3KX-DLGP
C127 SC4D7U6D3V3KX-DLGP

VCC3

R85 10KR2J-3-GP
R86 10KR2J-3-GP

SA1_DIM1
SA0_DIM1

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

VCC3

(R_) C128 SCD1U16V2KX-3DLGP
(R_) C129 SCD1U16V2KX-3DLGP

V_SM_VTT

C130 SC4D7U6D3V3KX-DLGP
C131 SCD1U16V2KX-3DLGP

DIMM VREF DQ B (To DIMM/CPU)

V_SM

R87 1KR2F-3-GP
(R_) C132 SCD1U16V2KX-3DLGP

DIMM_DQ_VREF_B — R88 0R0402-PAD — DIMM_DQ_R_VREF_B

R89 1KR2F-3-GP

C133 SCD1U16V2KX-3DLGP
C134 SCD1U16V2KX-3DLGP

DIMM_DQ_CPU_VREF_B — R90 2R2F-GP

C135 SCD022U16V2KX-3DLGP

DIMM_DQ_CPU_VREF_B_1

R91 24D9R2F-L-GP

DIMM VREF CA B (To DIMM)

V_SM

R93 1KR2F-3-GP
(R_) C12148 SCD1U16V2KX-3DLGP

DIMM_CA_VREF_B_L — R94 0R0402-PAD — DIMM_CA_VREF_B

R95 1KR2F-3-GP

C138 SCD1U16V2KX-3DLGP
C139 SCD1U16V2KX-3DLGP

Joey_SB_0708

<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title 013_DDR3_SODIMM2

Size C | Document Number COLORADO MLK SKYLAKE-S | Rev -2

Date: | Sheet 13 of 107

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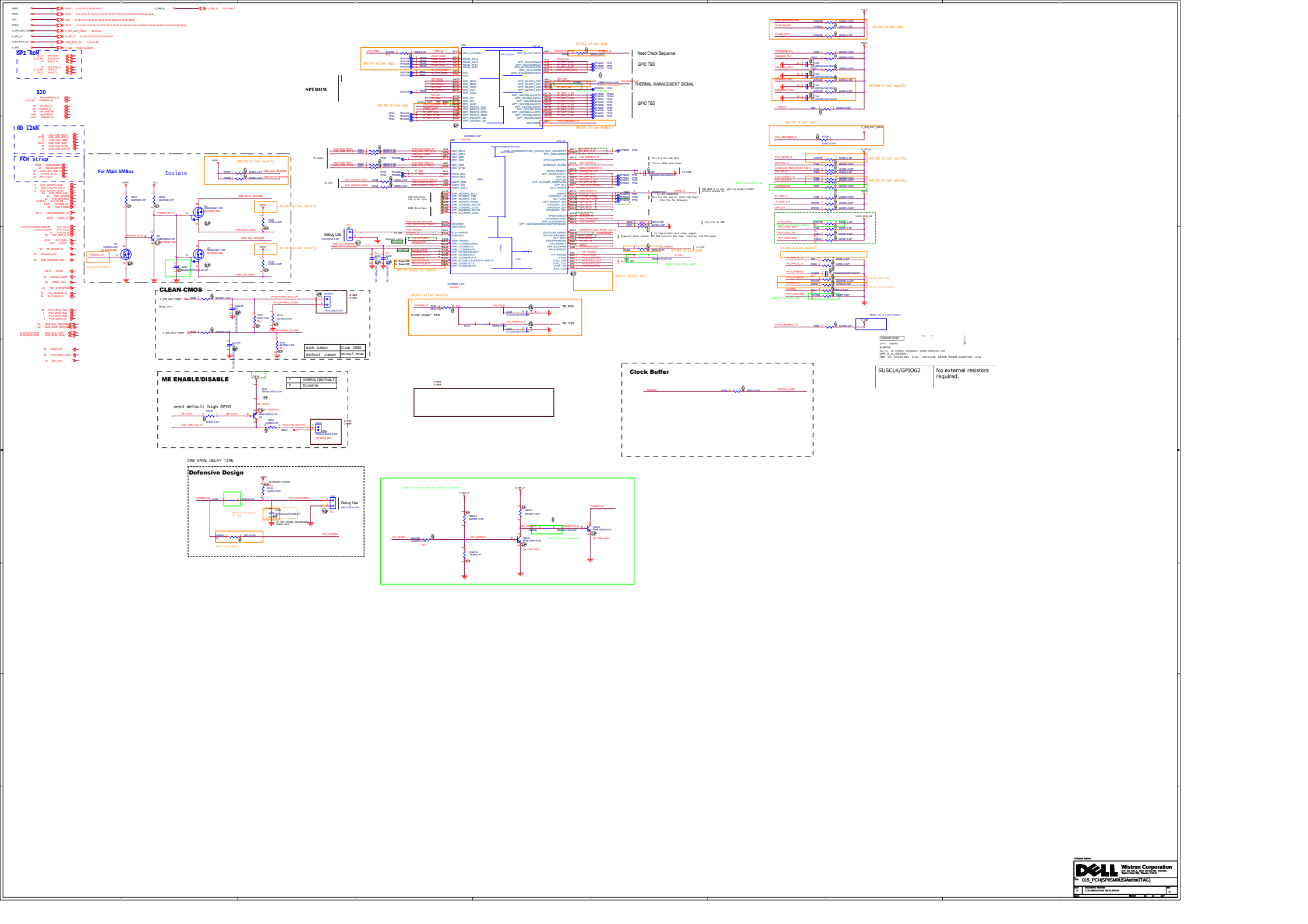
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 14 of 107


SPI ROM
SIO
HD LINK
PCH strap
For Main SMBus
Ioslate
CLEAN CMOS
With Jumper
Clear CMOS
Without Jumper
Normal Mode
ME ENABLE/DISABLE
L
NORMAL (DEFAULT)
H
Disable
need default high GPIO
CRB HAVE DELAY TIME
Defensive Design
Debug Use
From Power BIM
TO PCH
TO SIO
Clock Buffer
SUSCLK/GPIO62
No external resistors required.
Need Check Sequence
GPIO TBD
THERMAL MANAGEMENT SIGNAL
GPIO TBD
Wistron Corporation
015_PCH(SPI/SMBUS/Audio/JTAG)

+V1P0A_VCCF24_1P0

VCC3

Need to check Intel

CARDREADER

NGFF_REQ

LAN_REQ

NGFF REQ

The 10-kΩ pull-up should be on the rail that the corresponding SRCCLKRQ[15:0] pin resides in.

PCI Express devices or add-in cards that do NOT support clock request should terminate the SRCCLKRQ[15:0]# pins on the PCH with 10 kΩ ±10% external pull-up resistor.

PCIEX16_PRSNT2_R2_N

BD32

GPP_H2/SRCCLKREQ8#

FROM CPU

To SIO

TO CPU XDP

TO CPU

CLK OUT TO NGFF_PCIE0

CLK OUT TO PCIEx1 for LAN

CLK OUT TO Cardreader

06/26 Allen modify

CLK OUT TO X16 Graphic

ASTRO TEAM USE X'TAL

06/24 Allen modify

NOTE:The 1Mohm Damping Resistor
Use 0603 and Can't change to 0402!

When support FCIM need to stuff.

WHEN USING 25MHZ EXTERNAL REFERENCE FROM SINAI CMV:

REMOVE R383, X2, C322

REPLACE C321 WITH 50OHM RES 0402 PACKAGE

XTAL_IN should be pulled to GND via a 0-Ω resistor by default. Intel reliability concerns

<Variant Name>

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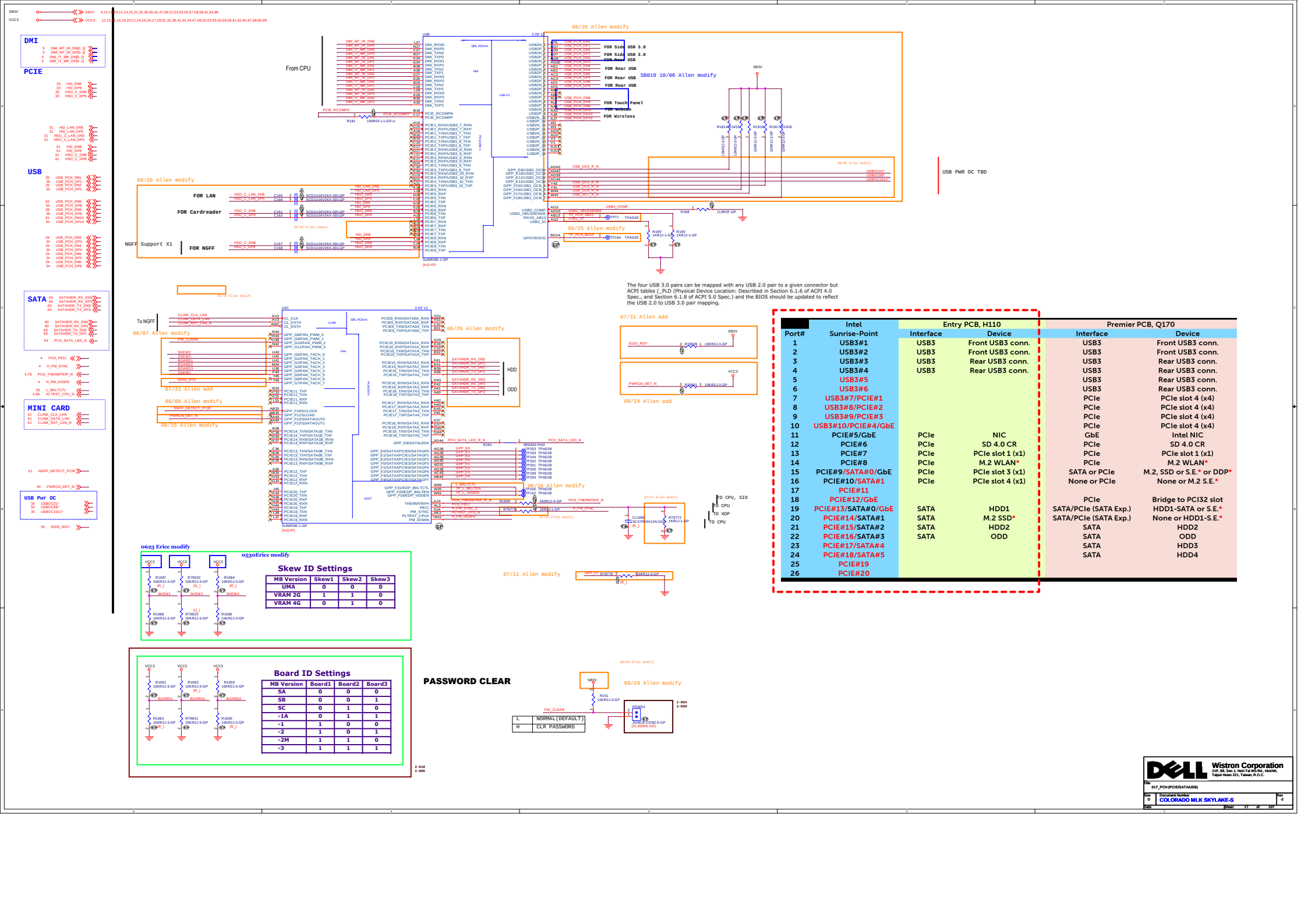
Title: 016_PCH_(Clock)

Size: | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 16 of 107



Skew ID Settings			
MB Version	Skew1	Skew2	Skew3
UMA	0	0	0
VRAM 2G	1	1	0
VRAM 4G	0	1	0

Board ID Settings			
MB Version	Board1	Board2	Board3
SA	0	0	0
SB	0	0	1
SC	0	1	0
-1A	0	1	1
-1	1	0	0
-2	1	0	1
-2M	1	1	0
-3	1	1	1

L	NORMAL(DEFAULT)
H	CLR PASSWORD

	Intel	Entry PCB, H110		Premier PCB, Q170	
Port#	Sunrise-Point	Interface	Device	Interface	Device
1	USB3#1	USB3	Front USB3 conn.	USB3	Front USB3 conn.
2	USB3#2	USB3	Front USB3 conn.	USB3	Front USB3 conn.
3	USB3#3	USB3	Rear USB3 conn.	USB3	Rear USB3 conn.
4	USB3#4	USB3	Rear USB3 conn.	USB3	Rear USB3 conn.
5	USB3#5			USB3	Rear USB3 conn.
6	USB3#6			USB3	Rear USB3 conn.
7	USB3#7/PCIE#1			PCIe	PCIe slot 4 (x4)
8	USB3#8/PCIE#2			PCIe	PCIe slot 4 (x4)
9	USB3#9/PCIE#3			PCIe	PCIe slot 4 (x4)
10	USB3#10/PCIE#4/GbE			PCIe	PCIe slot 4 (x4)
11	PCIE#5/GbE	PCIe	NIC	GbE	Intel NIC
12	PCIE#6	PCIe	SD 4.0 CR	PCIe	SD 4.0 CR
13	PCIE#7	PCIe	PCIe slot 1 (x1)	PCIe	PCIe slot 1 (x1)
14	PCIE#8	PCIe	M.2 WLAN*	PCIe	M.2 WLAN*
15	PCIE#9/SATA#0/GbE	PCIe	PCIe slot 3 (x1)	SATA or PCIe	M.2, SSD or S.E.* or DDP*
16	PCIE#10/SATA#1	PCIe	PCIe slot 4 (x1)	None or PCIe	None or M.2 S.E.*
17	PCIE#11				
18	PCIE#12/GbE			PCIe	Bridge to PCI32 slot
19	PCIE#13/SATA#0/GbE	SATA	HDD1	SATA/PCIe (SATA Exp.)	HDD1-SATA or S.E.*
20	PCIE#14/SATA#1	SATA	M.2 SSD*	SATA/PCIe (SATA Exp.)	None or HDD1-S.E.*
21	PCIE#15/SATA#2	SATA	HDD2	SATA	HDD2
22	PCIE#16/SATA#3	SATA	ODD	SATA	ODD
23	PCIE#17/SATA#4			SATA	HDD3
24	PCIE#18/SATA#5			SATA	HDD4
25	PCIE#19				
26	PCIE#20				

SB3V

VCC3

SB3V 4,15,17,20,21,24,25,31,35,38,40,42,47,48,51,53,55,56,57,58,59,61,84,86

VCC3 12,13,15,16,17,20,21,24,25,26,27,28,31,33,38,41,42,44,47,48,50,53,55,56,58,59,61,62,64,67,68,86,99

35 USB3_RX1_DN

35 USB3_RX1_DP

35 USB3_TX1_C_DN

35 USB3_TX1_C_DP

35 USB3_RX2_DN

35 USB3_RX2_DP

35 USB3_TX2_C_DN

35 USB3_TX2_C_DP

HDMI PORTB

56 DDPB_CTRL_CLK

56 DDPB_CTRL_DATA

56 DDSP_B_HPD

EDP PORT

55 EDP_4_HPD

4 H_SKTOCC_N

24,68 L_AD0

24,68 L_AD1

24,68 L_AD2

24,68 L_AD3

24 KBRST_N

24,68 L_FRAME_N

24 SER_IRQ_LT

24,67 FFS_INT1

67 FFS_INT2

24 CK_24M_SIO

24,68 LPC_CLK

20 DDPC_CTRL_DATA

20 DDPC_CTRL_DATA

61 NGFF_DETECT_USB

26,53 FAN_CTRL_POWER

61 NGFF_BT_DISABLE

55 OS_MODE_SEL

55 BIOS_REQ

06/26 Allen modify

FOR Side USB 3.0

FOR Side USB 3.0

Unused

SATA Device Sleep control pin

06/26 Allen modify

06/26 Allen modify

SID Need both 49R/J and 33R/J for LPC CLK

06/26 Allen modify

06/08 Allen modify

HDMI no ADI

HDMI

EDP

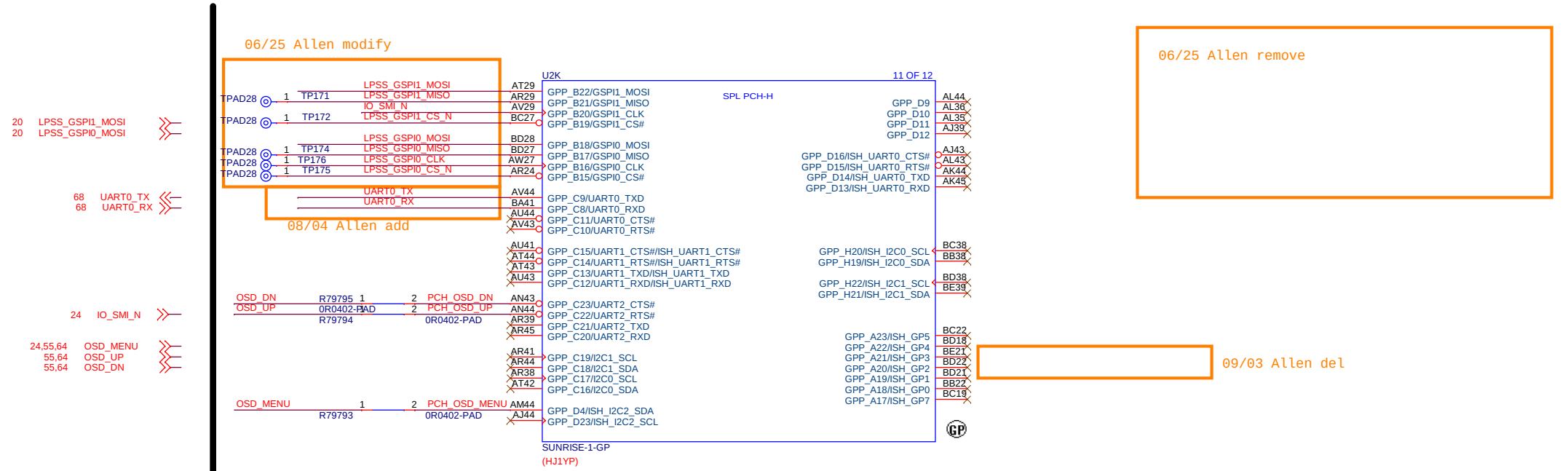
09/03 Allen modify

09/03 Allen modify

09/03 Allen modify

09/03 Allen modify

Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: 018_PCH (USB3.0/GPIO/HPD)			
Size: D	Document Number: COLORADO MLK SKYLAKE-S		Rev: -2
Date:	Sheet 18 of 107		



20.4 Terminating Unused GSPI Signals

GSPI signals are multiplexed with GPIOs and default to GPIO functionality. If GSPI interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

§ §

19.3 Terminating Unused UART Signals

UART signals are multiplexed with GPIOs and default to GPIO functionality (as input). If UART interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

18.4 Terminating Unused I^2C Signals

I^2C signals are multiplexed with GPIOs and default to GPIO functionality (as input). If I^2C interfaces are not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

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Title: 019_PCH (GPIO)
Size: B
Document Number: COLORADO MLK SKYLAKE-S
Rev: -2
Date:
Sheet 19 of 107

Check GPIO require to Pull Up or Pull down

Signal	Usage	When Sampled	Comment
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC). ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

CRB "0"

CRB "1"

08/08 Allen modify

CRB to Header,but Unmount

CONSENT STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

PESONALITY STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

Signal	Usage	When Sampled	Comment
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). **Bit 6 — Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** Is selected for EC. (Default) 1 = **eSPI** Is selected for EC. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SPI0_MOSI	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SML1ALERT# / PCHHOT# / GPP_B23	Reserved	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

Signal	Usage	When Sampled	Comment
HDA_SDO	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Asserting HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. 3. This signal is in the primary well.
DDPB_CTRLDATA / GPP_I6	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_I8	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPD_CTRLDATA / GPP_I10	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GPP_H12	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Note:*** The pull-down resistor is disabled after RSMRST# de-asserts

06/25 Allen modify

ESPI FLASH SHARING MODE
0: MASTER ATTACHED FLASH SHARING
1:SLAVE ATTACEHD FLASH SHARING
PCH HAS INTERNAL WEAK PD

EXI BOOT STALL BYPASS IS ENABLE
IF SAMPLED HIGH PCH HAS INTERNAL WEAK PD

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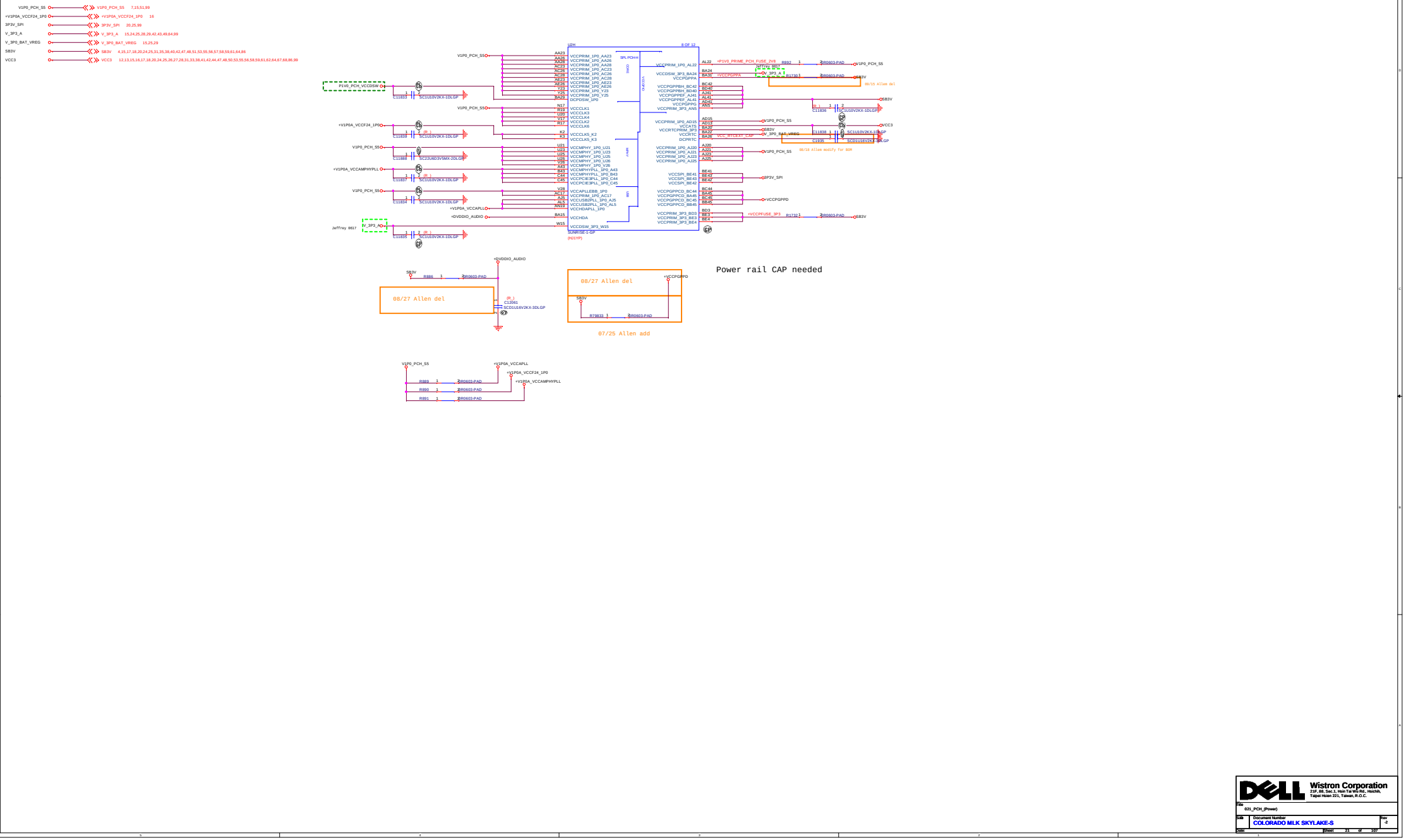
020_PCH_(Strap Pin)

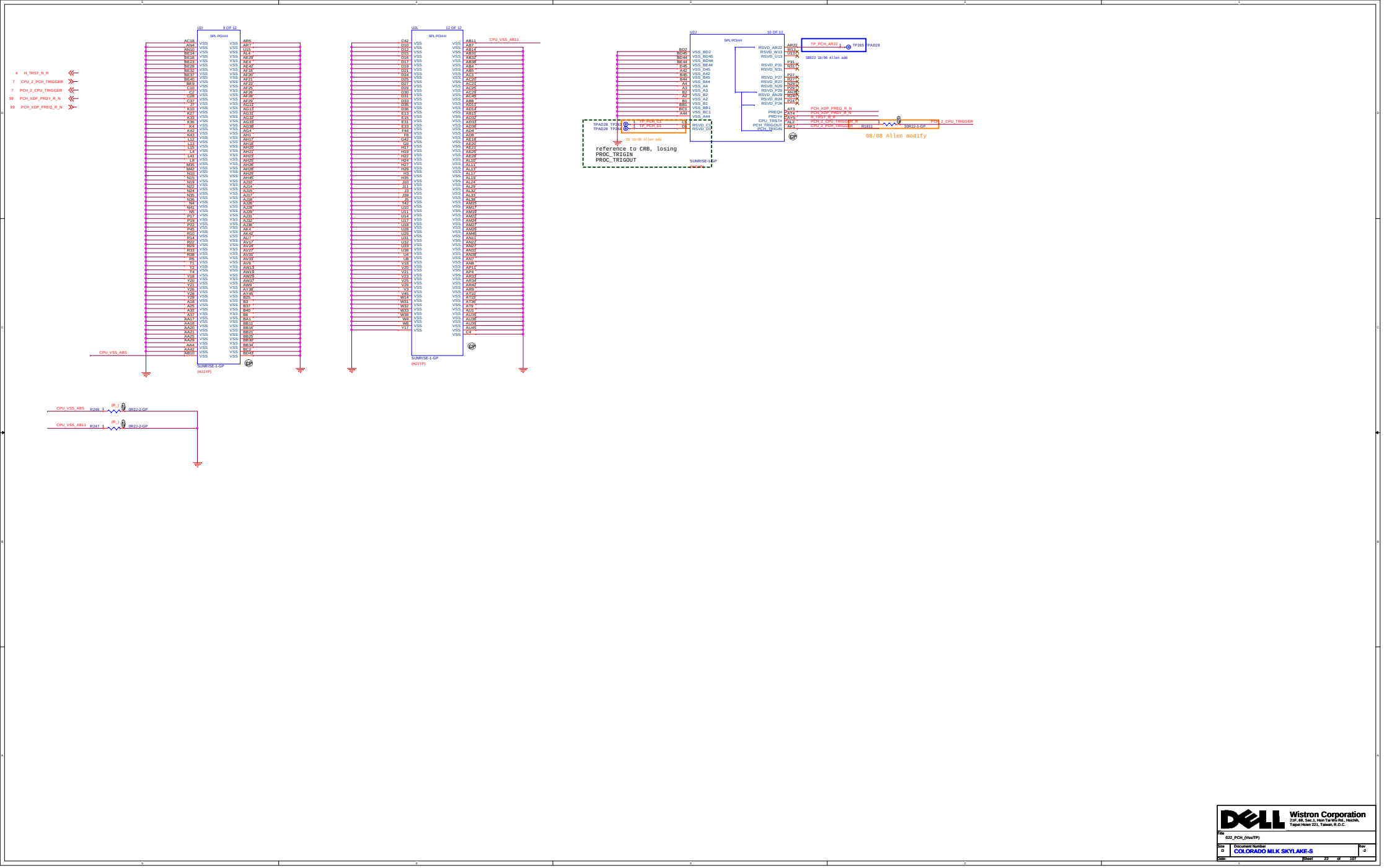
Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 39 of 107



Wistron Corporation
2/F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	021_PCH_(Power)	
Size	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 21 of 107	



Wistron Corporation	Title: 022_PCH_(Vss/TP)	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	Size: D	Document Number: COLORADO MLK SKYLAKE-S
	Date:	Sheet 22 of 107

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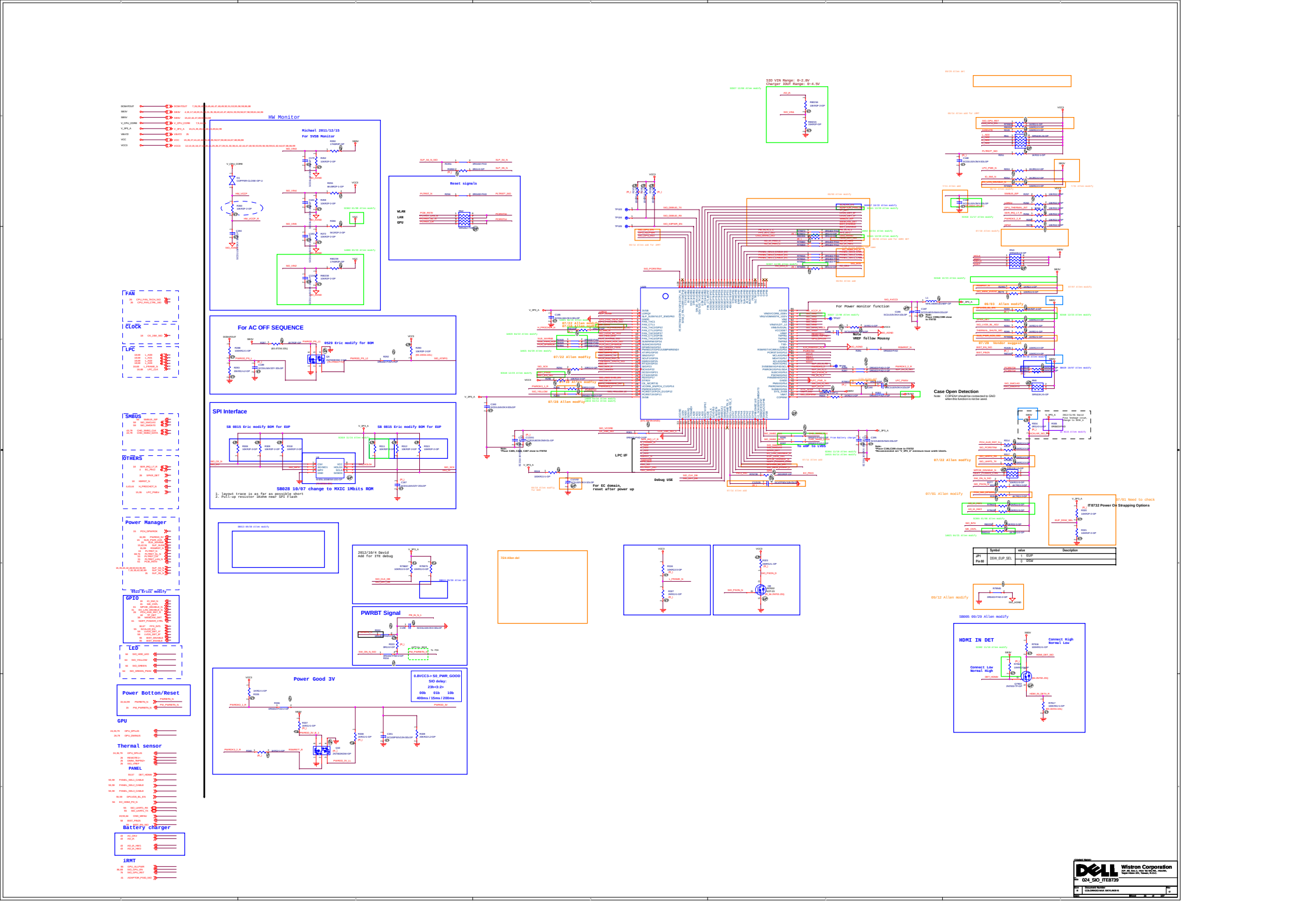
Taipei Hsien 221, Taiwan, R.O.C.

Title
023_PCH_(Reserved)

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	-2

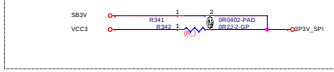
Date: Sheet 23 of 107


HW Monitor
Michael 2011/12/15
For SVSB Monitor
Reset signals
WLAN
LAN
GPU
For AC OFF SEQUENCE
SB 0815 Eric modify for BOM
SPI Interface
SB 0815 Eric modify BOM for EUP
SB828 10/07 change to MXIC 1Mbits ROM
1. layout trace is as far as possible short
2. Pull-up resistor 1Kohm near SPI Flash
Power Good 3V
0.8VCC3-> S0_PWR_GOOD
SIO delay:
23h<3:2>
00b 01b 10b
40ms / 15ms / 200ms
PWRBT Signal
2012/10/4 David
Add for ITE debug
SIO VIN Range: 0~2.8V
Charger IOUT Range: 0~4.5V
For Power monitor function
VBAT follow Moussy
VBEF follow Moussy
Case Open Detection
Note: CQH2H should be connected to GND when this function is not be used.
LPC I/F
Debug USE
For EC domain, reset after power up
IT8732 Power On Strapping Options
HDMI IN DET
Connect High Normal Low
Connect Low Normal High
FAN
CLOCK
LPC
SMBUS
OTHERS
Power Manager
GPIO
LED
Power Botton/Reset
GPU
Thermal sensor
PANEL
Battery charger
iRMT
07/22 Allen modify
07/28 Allen modify
07/01 Allen modify
09/03 Allen modify
07/29 Vender suggest
07/22 Allen modify
07/01 Need to check
09/12 Allen modify
SB805 09/29 Allen modify
Wistron Corporation
Document Number
024_SIO_ITE8739
COLORADO14E_BAYLAKE-S

3P3V_SPI 20,21,99
SB3V 4,15,17,18,20,21,24,31,35,38,40,42,47,48,51,53,55,56,57,58,59,61,84,86
VCC3 12,13,15,16,17,18,20,21,24,26,27,28,31,33,38,41,42,44,47,48,50,53,55,56,58,59,61,62,64,67,68,86,99
V_3P3_A 15,21,24,28,29,41,43,49,64,99
VBAT2 24
V_3P0_BAT_VREG 15,21,99

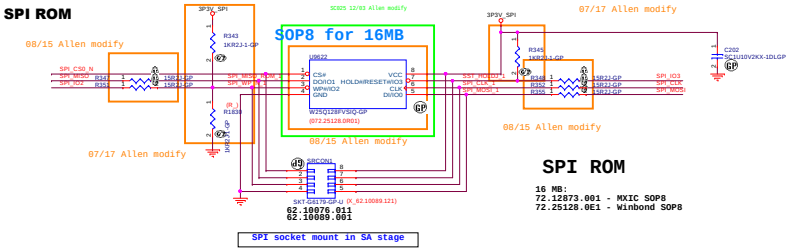
15 SPI_CS0_N
15,20 SPI_MISO
5,10,99 SPI_IO2
15,20 SPI_IO3
15 SPI_CLK
15,20,99 SPI_MOSI

+V3P3A_V1P8A_PCH_SPI



SPI ROM

08/15 Allen modify



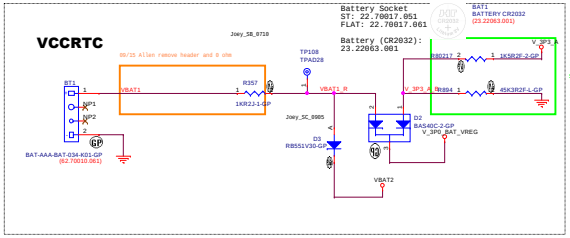
SPI socket mount in SA stage

SPI ROM

16 MB:
72.12873.001 - MXIC SOP8
72.25128.0E1 - Winbond SOP8

08/15 Allen modify for cost

VCCRTC



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Taipei Hsien 221, Taiwan, R.O.C.

Title: 025_Flash ROM/RTC
Size: D
Document Number: COLORADO MLK SKYLAKE-S
Rev: -X
Date:
Sheet 25 of 107

DCBATOUT
VCC
VCC3
12V_S0

SIO FAN CONTROL

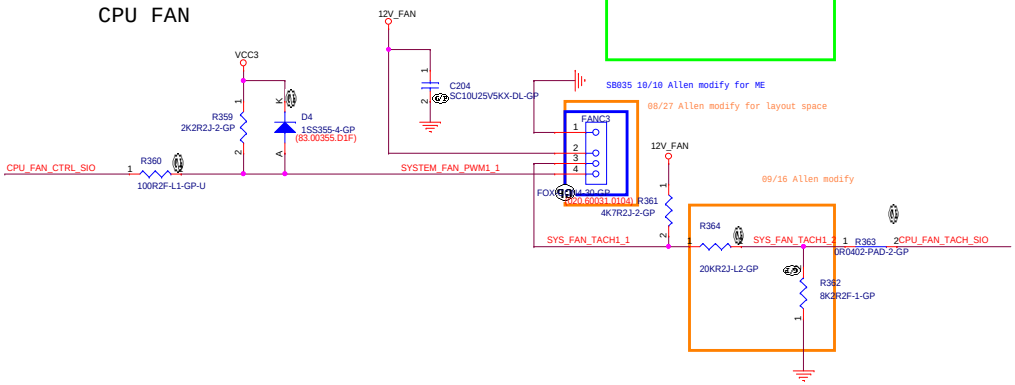
24 CPU_FAN_CTRL_SIO
24 CPU_FAN_TACH_SIO

From SIO

18,53 FAN_CTRL_POWER

4 PINS FAN CONTROL

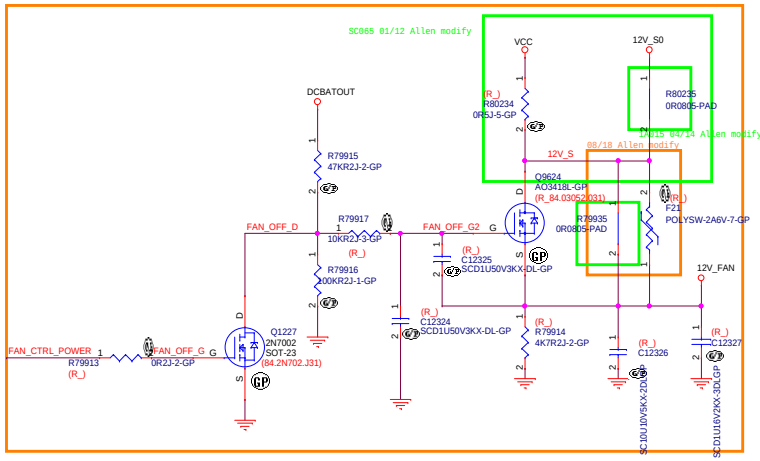
CPU FAN



07/29 Allen modify for down size

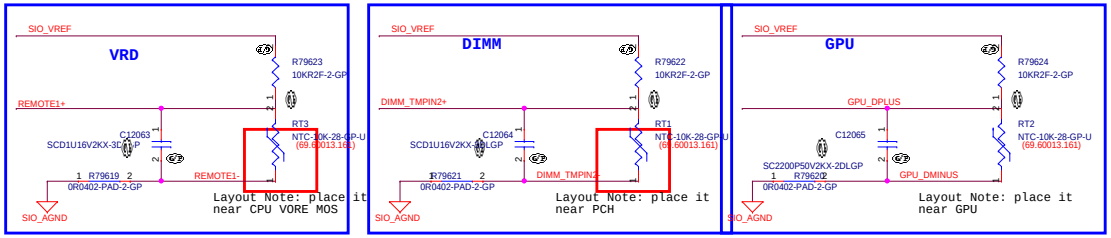
SC065 01/12 Allen del

08/12 Allen add



THERMAL DIODES

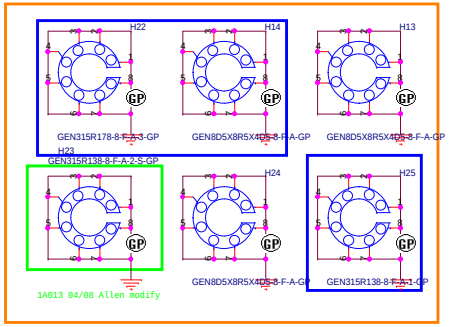
24 SIO_VREF
24 REMOTE1+
24 DIMM_TMPIN2+
24,79 GPU_DPLUS
79 GPU_DMINUS

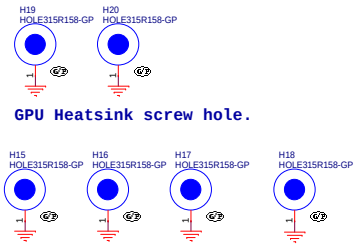


09/02 Allen modify for ME

SB021 10/06 Allen modify

A





SB006 09/30 Allen modify

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title 026_FAN CIRCUITS/HOLE

Size C | Document Number COLORADO MLK SKYLAKE-S | Rev -2

Date: | Sheet 26 of 107

V_SP0_A
VCC
VCC3
HD_LINK
AUD_LINK_SDIN
AUD_LINK_SDO
AUD_LINK_BCLK
AUD_LINK_SYNC
AUD_LINK_RST_N
AUD_DMIC_CLK
AUD_DMIC_DATA
PORTC_SPK_R
PORTC_SPK_L
SPKR
EAPD_DEPOP
To AMP
To Mute AMP
BUZZER_SPKR_R
To PCH
MIC2-L
MIC2-R
LINEOUT-L
LINEOUT-R
HPOUT-L
HPOUT-R
MIC2-VREFO-L
MIC2-VREFO-R
LINE2-VREFO
HPOUT-JD
LINEOUT-JD
SLEEVE
RING2
SPDIF_IC
PC_MONITOR_SW
PC_MONITOR_SW
SEL L:A1(PC) H:A2(MONITOR)
7/24 Allen add
08/25 Allen modify
PCB trace width of
RING2 & SLEEVE at least 40 mil
ANALOG
DIGITAL
Moat
PCH PWR have no 1.5v
Digital Power from 3V
DIGITAL
ANALOG
Moat
In order to prevent the built-in LDO damaged from over-voltage on +5VSYS or Standby power line, we suggested using this Voltage suppressing device.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
027_AUDIO ALC3661
COLORADO MLK SKYLAKE-S

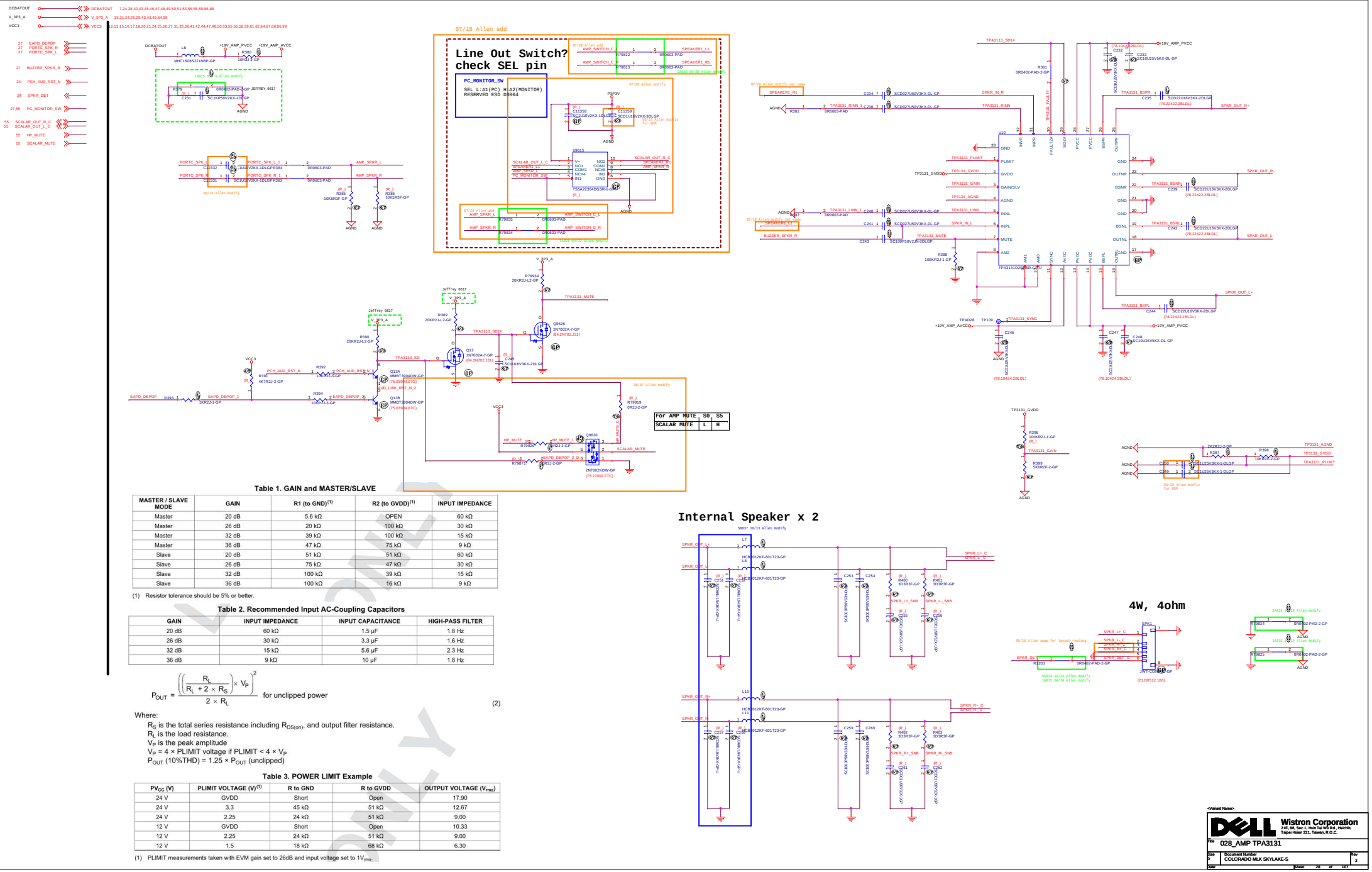


Table 1. GAIN and MASTER/SLAVE

MASTER / SLAVE MODE	GAIN	R1 (to GND)(1)	R2 (to GVDD)(1)	INPUT IMPEDANCE
Master	20 dB	5.6 kΩ	OPEN	60 kΩ
Master	26 dB	20 kΩ	100 kΩ	30 kΩ
Master	32 dB	39 kΩ	100 kΩ	15 kΩ
Master	36 dB	47 kΩ	75 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	26 dB	75 kΩ	47 kΩ	30 kΩ
Slave	32 dB	100 kΩ	39 kΩ	15 kΩ
Slave	36 dB	100 kΩ	16 kΩ	9 kΩ

(1) Resistor tolerance should be 5% or better.

Table 2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	60 kΩ	1.5 µF	1.8 Hz
26 dB	30 kΩ	3.3 µF	1.6 Hz
32 dB	15 kΩ	5.6 µF	2.3 Hz
36 dB	9 kΩ	10 µF	1.8 Hz

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power} \qquad (2)$$

Where:

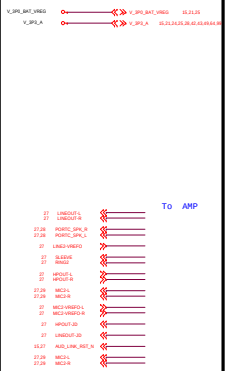
R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
R_L is the load resistance.
V_P is the peak amplitude
$V_P = 4 \times$ PLIMIT voltage if PLIMIT $< 4 \times V_P$
P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)

Table 3. POWER LIMIT Example

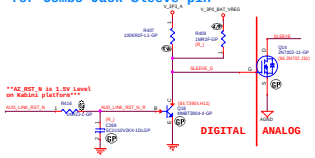
PV_{CC} (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	OUTPUT VOLTAGE (V_{rms})
24 V	GVDD	Short	Open	17.90
24 V	3.3	45 kΩ	51 kΩ	12.67
24 V	2.25	24 kΩ	51 kΩ	9.00
12 V	GVDD	Short	Open	10.33
12 V	2.25	24 kΩ	51 kΩ	9.00
12 V	1.5	18 kΩ	68 kΩ	6.30

(1) PLIMIT measurements taken with EVM gain set to 26dB and input voltage set to 1V_{rms}.

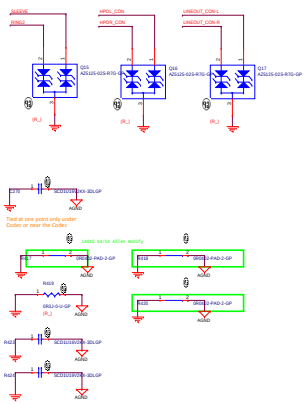
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: 028_AMP TPA3131
Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2
Date: | Sheet 28 of 107

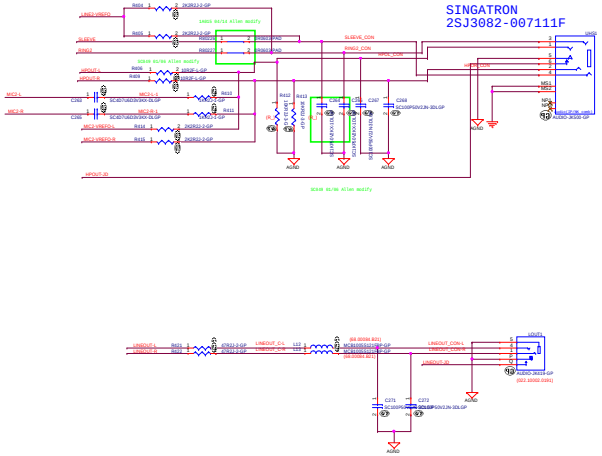


Grounding Circuit for Combo Jack Sleeve pin

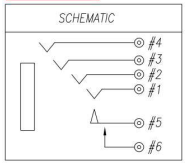


To solve the background noise while combo jack connecting to an active speaker and system entry into S3/S4/S5 without analog power.





Pin Define:
Pin1:HP_L
Pin2:HP_R
Pin3:Ring2
Pin4:Sleeve
Pin5:AGND
Pin6:JD
Pin7:GND
Pin8:GND



Pin Define:
Pin1:HP_L
Pin2:HP_R
Pin3:Ring2
Pin4:Sleeve
Pin5:AGND
Pin6:JD
Pin7:GND
Pin8:GND

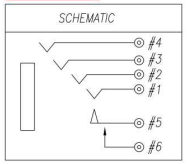
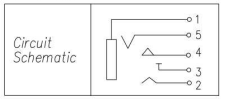
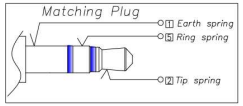


TABLE A:Circuit





4-pin 3.5mm Headset Connector Pinout

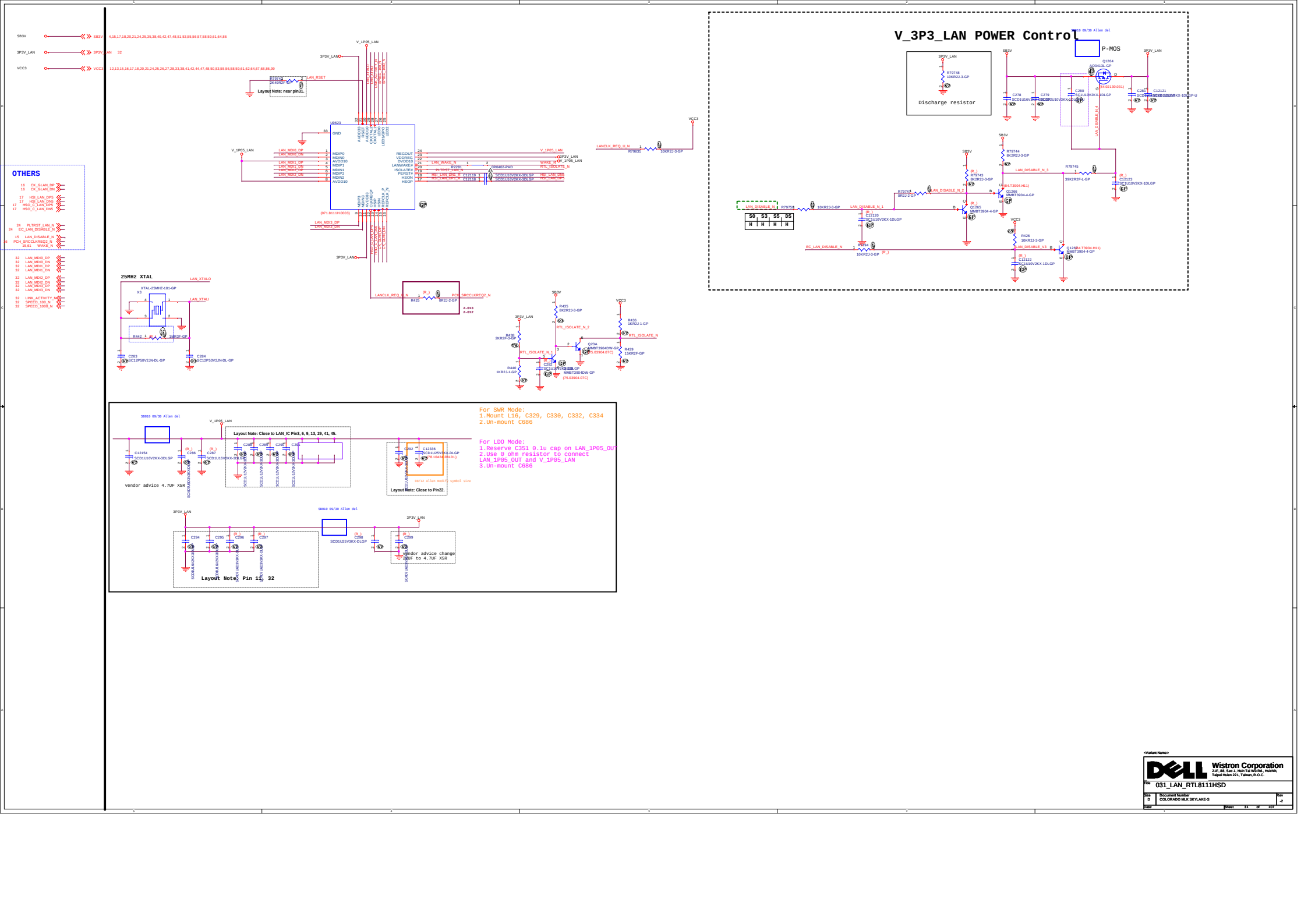
Nokia, Lenovo mobile		
Pin Number	**Pin Name**	**Description**
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	**Microphone**
4	Sleeve	**Ground / Common**

iPhone, Samsung, Blackberry, HTC		
Pin Number	**Pin Name**	**Description**
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	**Ground / Common**
4	Sleeve	**Microphone**

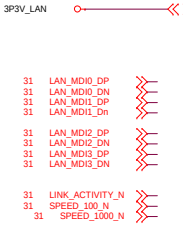
Wistron Corporation
Size: 029_MIC/SPEAKER/AUDIO JACK
Document Number: COLGRADO MLK SKYLAKE-S
Rev: -2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

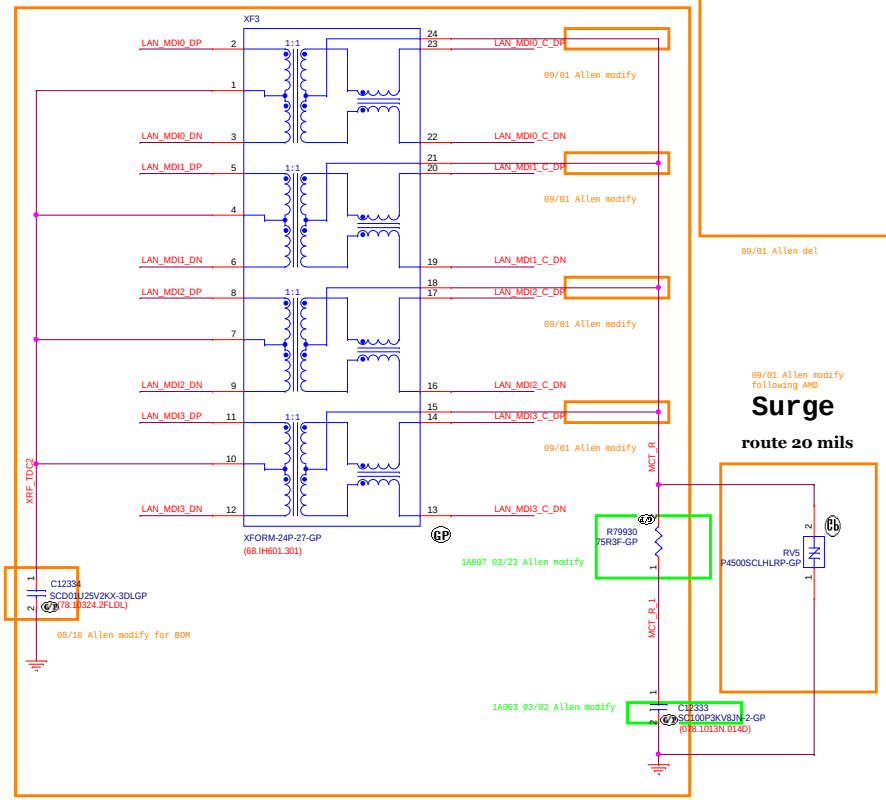
Title		
Size: A	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 30 of 107	


V_3P3_LAN POWER Control
P-MOS
Discharge resistor
25MHz XTAL
Layout Note: near pin31.
Layout Note: Close to LAN_IC Pin3, 6, 9, 13, 29, 41, 45.
vendor advice 4.7UF X5R
Layout Note: Close to Pin22.
Layout Note: Pin 11, 32
vendor advice change 22UF to 4.7UF X5R
For SWR Mode:
1.Mount L16, C329, C330, C332, C334
2.Un-mount C686
For LDO Mode:
1.Reserve C351 0.1u cap on LAN_1P05_OUT
2.Use 0 ohm resistor to connect LAN_1P05_OUT and V_1P05_LAN
3.Un-mount C686
OTHERS
Wistron Corporation
2UF, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
031_LAN_RTL8111HSD
COLORADO MLK SKYLAKE-S

0702 Eric modify from Dogfish



Transformer



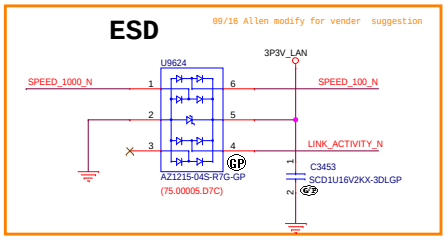
09/01 Allen del

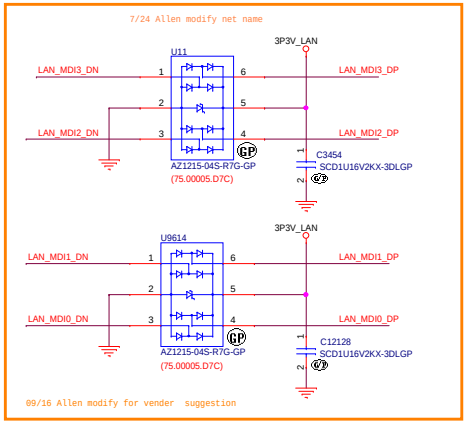
09/01 Allen modify following AMD

Surge

route 20 mils

ESD





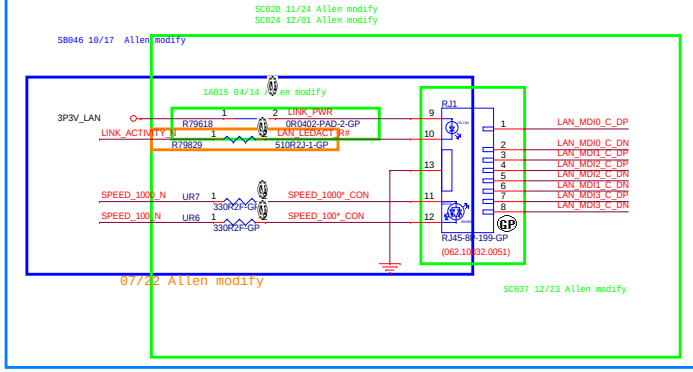
Transformer

0703 eric modify connector

	Giga	100	10
Link	Orange	Green	Green
Act	Yellow Blink	Yellow Blink	Yellow Blink

Connector

RJ45



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 032_RJ45+TRANSFORMER

Size	Document Number	Rev
C	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 32 of 107

VCC3 VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,38,41,42,44,47,48,50,53,55,56,58,59,61,62,64,67,68,86,99

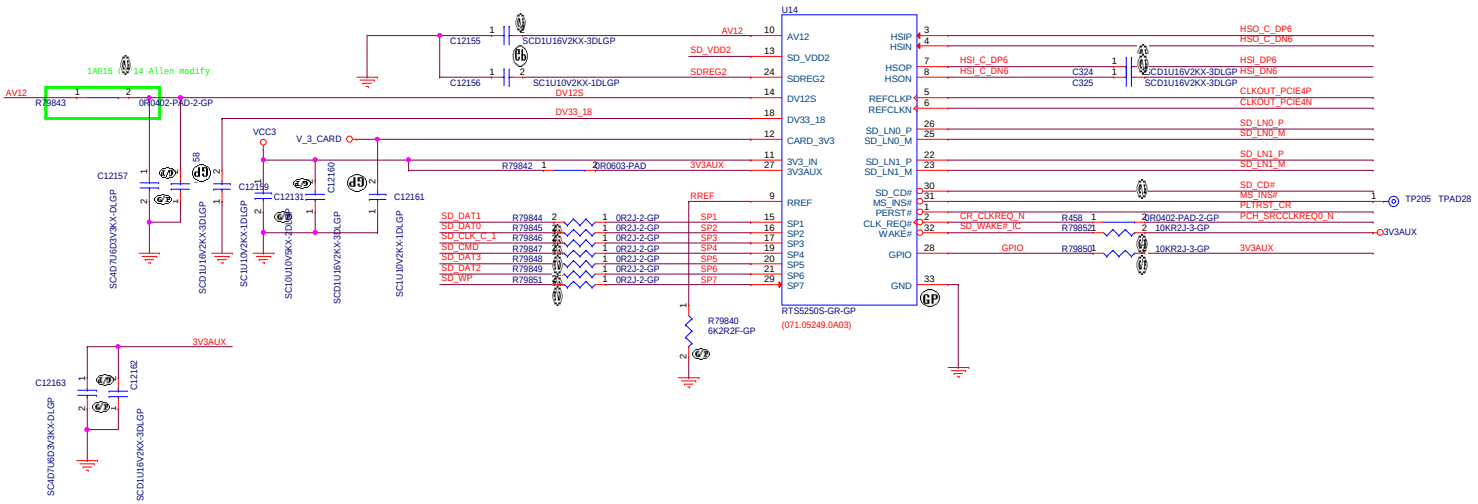
Card Reader

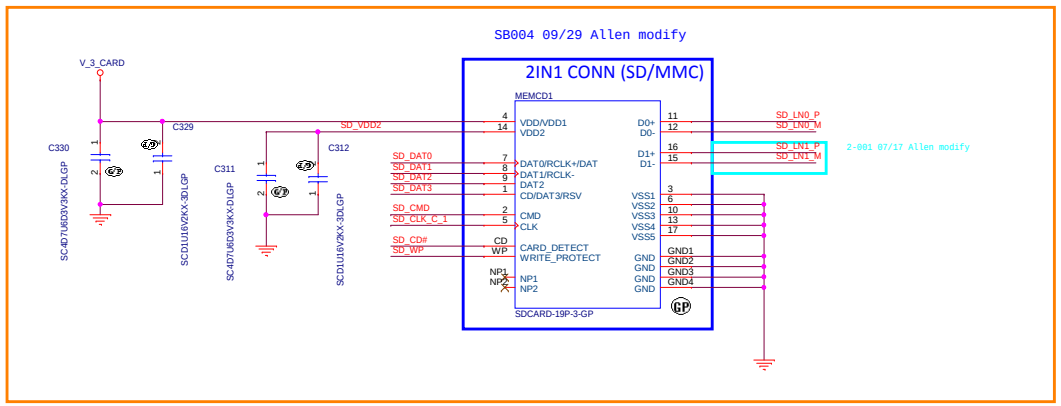
17 HSI_DN6
17 HSI_DP6
17 HSO_C_DN6
17 HSO_C_DP6

16 PCH_SRCCLKREQ0_N
24 PLTRST_CR

16 CLKOUT_PCIE4N
16 CLKOUT_PCIE4P

15 SD_WAKE#_IC





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title 033_READER CONN

Size C | Document Number COLORADO MLK SKYLAKE-S | Rev -2

Date: | Sheet 33 of 107

VCC5_USB

VCC5_USB

35,42,62

USB

17 USB_PCH_DN3
17 USB_PCH_DP3
17 USB_PCH_DN4
17 USB_PCH_DP4

17 USBOC89*

17 USB_PCH_DN5
17 USB_PCH_DP5
17 USB_PCH_DN6
17 USB_PCH_DP6

17 USBOC01*

07/24 Allen modify for down size

USB_Power...Rear1

SB050 10/20 Allen modify

F18
POLYSW-2A6V-7-GP

VCC5_USB

R462
1KR2J-1-GP
(R_)

C334
(R_)
SC1KP50V2KX-1DLGP

R463
10KR2J-3-GP

USBOC89*

R464
15KR2F-GP

USBVCC89

C331
(R_)
SC1U10V5KX-2DLGP

C332
(R_)
SC1U16V2KX-3DLGP

C333
(R_)
SC1U10V5KX-2DLGP

USB_Power...Rear2

SB050 10/20 Allen modify

F19
POLYSW-2A6V-7-GP

07/24 Allen modify for down size

VCC5_USB

R466
1KR2J-1-GP
(R_)

C338
(R_)
SC1KP50V2KX-1DLGP

R467
10KR2J-3-GP

USBOC01*

R469
15KR2F-GP

TC2
FU00U16VM-47-GP
(009.10710.0021)
08/20 Allen modify for BOM

USBVCC1011

C12329
(R_)
SC1U10V5KX-2DLGP

C356
(R_)
SC1U16V2KX-3DLGP

C12330
(R_)
SC1U10V5KX-2DLGP

R465
(R_)
0R2J-2-GP

R468
(R_)
0R2J-2-GP

Rear USB1

SB003 09/29 Allen modify for Dell ID
SB031 10/07 Allen modify for Dell ID

USB1

USBVCC1011
USBP3N_EXT
USBP3P_EXT

SM10USB6-127-GP
(022.10005.01K1)

USB2

USBVCC89
USBP4N_EXT
USBP4P_EXT

SM10USB6-127-GP
(022.10005.01K1)

Rear USB2

USB3

USBVCC1011
USBP5N_EXT
USBP5P_EXT

SM10USB6-127-GP
(022.10005.01K1)

USB4

USBVCC89
USBP6N_EXT
USBP6P_EXT

SM10USB6-127-GP
(022.10005.01K1)

ESD

D10

USBP3P_EXT
USBP4P_EXT
USBVCC89

C340
SCD1U16V2KX-3DLGP

USBP3N_EXT
USBP4N_EXT
(075.02304.007C)

IP4223CZ6-1-GP

D11

USBP5N_EXT
USBP6N_EXT
USBVCC1011

C341
SCD1U16V2KX-3DLGP

USBP5P_EXT
USBP6P_EXT
(075.02304.007C)

IP4223CZ6-1-GP

TR3

USB_PCH_DN3
USB_PCH_DP3
USBP3N_EXT
USBP3P_EXT

MCM10128900FBP-GP-U
(068.01012.2011)

TR4

USB_PCH_DP4
USB_PCH_DN4
USBP4P_EXT
USBP4N_EXT

MCM10128900FBP-GP-U
(068.01012.2011)

TR5

USB_PCH_DN5
USB_PCH_DP5
USBP5N_EXT
USBP5P_EXT

MCM10128900FBP-GP-U
(068.01012.2011)

TR6

USB_PCH_DN6
USB_PCH_DP6
USBP6N_EXT
USBP6P_EXT

MCM10128900FBP-GP-U
(068.01012.2011)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 034_USB2.0 CONN

Size: C
Document Number: COLORADO MLK SKYLAKE-S
Rev: -2

Date:
Sheet 34 of 107

VCCS_USB
SB3V

USB 3.0

18 USB3_RX1_DN
18 USB3_RX1_DP
18 USB3_TX1_C_DN
18 USB3_TX1_C_DP
18 USB3_RX2_DN
18 USB3_RX2_DP
18 USB3_TX2_C_DN
18 USB3_TX2_C_DP
17 USB_PCH_DN1
17 USB_PCH_DP1
17 USB_PCH_DN2
17 USB_PCH_DP2
17 USBOC1011*
15 CHAR_EN
15 PCH_CHAR_CTL3
7,15,24,42,50,99 SLP_S4_N
7,15,24,40,42,48,50,53,55,99 SLP_S3_N

USB_Power...Side1

F14 POLYSW-2A6V-7-GP
R471 1KR2J-1-GP
R470 10KR2J-3-GP
R472 15KR2F-GP
C12164 SC1KP50V2KX-1DLGP
TC3 SCD1U16V2KX-3DLGP
TC4 SE001607A47-GP
C342 SCD1U16V2KX-3DLGP
C343 SCD1U16V2KX-3DLGP
C344 SCD1U16V2KX-3DLGP
C345 SCD1U16V2KX-3DLGP
USBOC1011*
USBVCC01
VCCS_USB

Side USB 3.0

SSUSB1
SSUSB2
USBVCC01
USBP1N_EXT
USBP1P_EXT
USBP2N_EXT
USBP2P_EXT
SIDE_USB3_RX1-
SIDE_USB3_RX1+
SIDE_USB3_TX1-
SIDE_USB3_TX1+
SIDE_USB3_RX2-
SIDE_USB3_RX2+
SIDE_USB3_TX2-
SIDE_USB3_TX2+
SKT-USB11-112-GP-U
(022.10005.0J01)

EMI

USB3_TX1_C_DN
USB3_TX1_C_DP
USB3_TX1_EMI_DN
USB3_TX1_EMI_DP
USB3_TX2_C_DN
USB3_TX2_C_DP
USB3_TX2_EMI_DN
USB3_TX2_EMI_DP
C347 C348 C349 C350
SCD1U16V2KX-3DLGP

L17 L18 L19 L20
FILTER-4P-123-GP
(66.R0036.04L)

ESD

U15 U16
AZ1045-04F.R7G-GP

D9
IP4223CZ6-1-GP
C339 SCD1U16V2KX-3DLGP
(075.02304.007C)

TR1 TR2
MCM1012B900FBP-GP-U
(068.01012.2011)
USB_PCH_DP1
USB_PCH_DN1
USBDN2_CHAR
USBDP2_CHAR

SB051 10/20 Allen modify

Charger IC - TI TPS2546

TPS2546RTER-GP
U625
R455 10KR2J-3-GP
R457 33K9F-GP
R80049 20K9F-L-GP
R452 0R2J-2-GP
C314 SCD1U16V2KX-3DLGP
TP72 TPAD24
CHAR_EN
CHAR_ILIM_SEL
CHAR_ILIM_HI
CHAR_ILIM_LO
CHAR_CTL1
CHAR_CTL2
CHAR_CTL3
CHAR_ILIM_SEL
R451 0R2J-2-GP
R453 0R2J-2-GP
R454 0R2J-2-GP
R456 0R2J-2-GP
SLP_S3_N
SLP_S4_N
PCH_CHAR_CTL3

Current limit for ILIM_HI (CDP/DCP mode)= 2510 mA
Current limit for ILIM_LO (SDP mode) = 1525 mA

To PCH GPIO41

To PCH

To connector

CTL1 SLP_S3#	CTL2 SLP_S4#	CTL3 GPIO41	ILIM_SEL GPIO41	Mode	State
0	0	0	0	Turn off power switch & discharge VBUS	S4/S5
0	0	1	1	DCP	S4/S5
0	1	0	0	SDP	S3
0	1	1	1	DCP with HID auto detect USB data pass through	S3
1	1	0	0	SDP	S0
1	1	1	1	CDP	S0

DVT1

R80052 R80050 R80053 R80051 0R0402-PAD
USB_PCH_DP2_M
USB_PCH_DN2_M
USBDP2_CHAR
USBDN2_CHAR

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 035_USB3.0 CONN

Size: Custom | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 35 of 107

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Size: A4	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 36 of 107	

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
Custom	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 37 of 107

SB3V SB3V 4,15,17,18,20,21,24,25,31,35,40,42,47,48,51,53,55,56,57,58,59,61,64,86

VCC3 VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,41,42,44,47,48,50,53,55,56,58,59,61,62,64,67,68,86,99

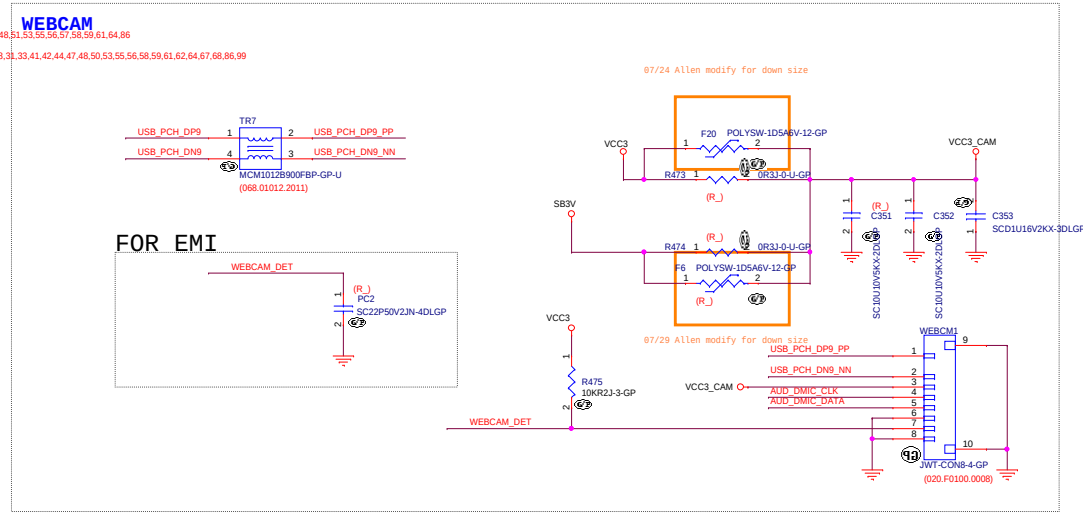
WEBCAM

17 USB_PCH_DN9
17 USB_PCH_DP9

27 AUD_DMIC_CLK
27 AUD_DMIC_DATA

24 WEBCAM_DET

WEBCAM



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title 038_WEBCAM

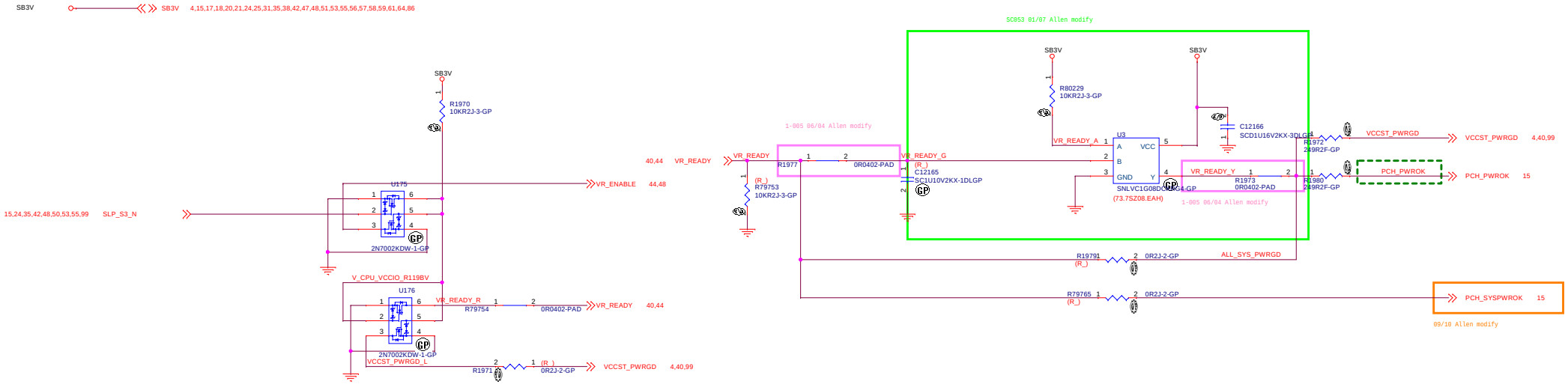
Size C | Document Number COLORADO MLK SKYLAKE-S | Rev -2

Date: | Sheet 38 of 107

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Size: A	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 39 of 107	



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 040_Power enable & sequence

Size	Document Number	Rev
Custom	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 40 of 107

VCC
VCC3

VCC 15,24,26,27,42,44,45,46,55,56,57,58,60,64,67,68,86,88

VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,42,44,47,48,50,53,55,56,58,59,61,62,64,67,68,86,99

For layout top and bottom the same

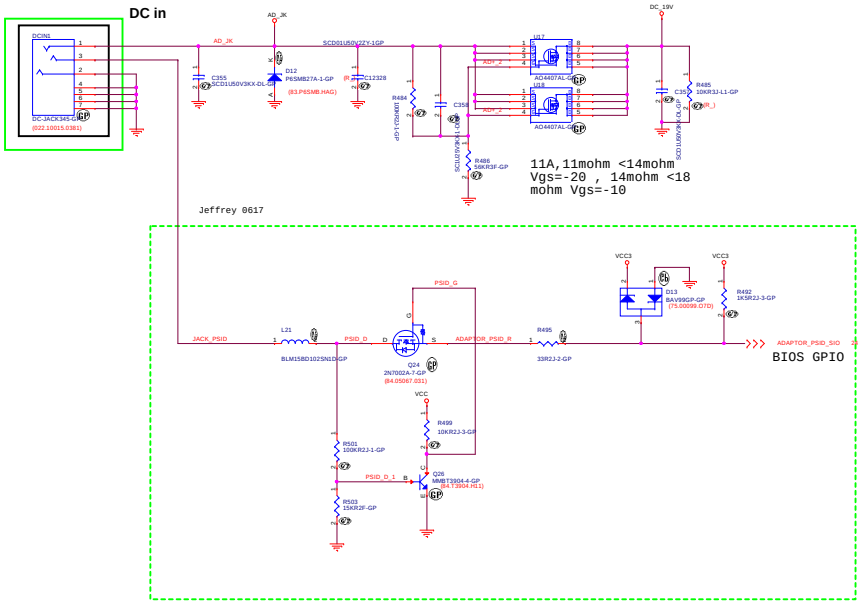
U33 R981 R982 R983

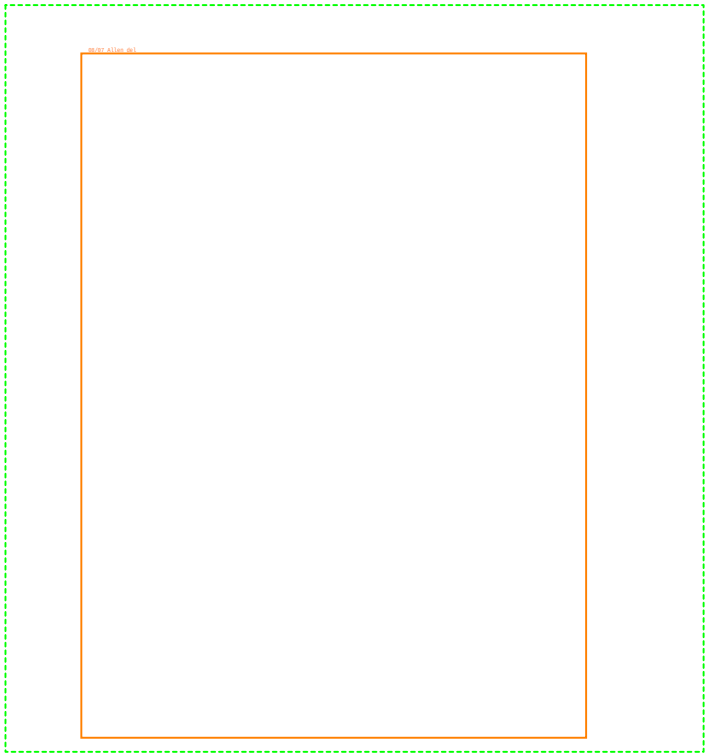
R1718

SC820 11/24 Allen modify

Adaptor in to generate DCBATOUT

DC in





<Variant Name>

Wistron Corporation
2/F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

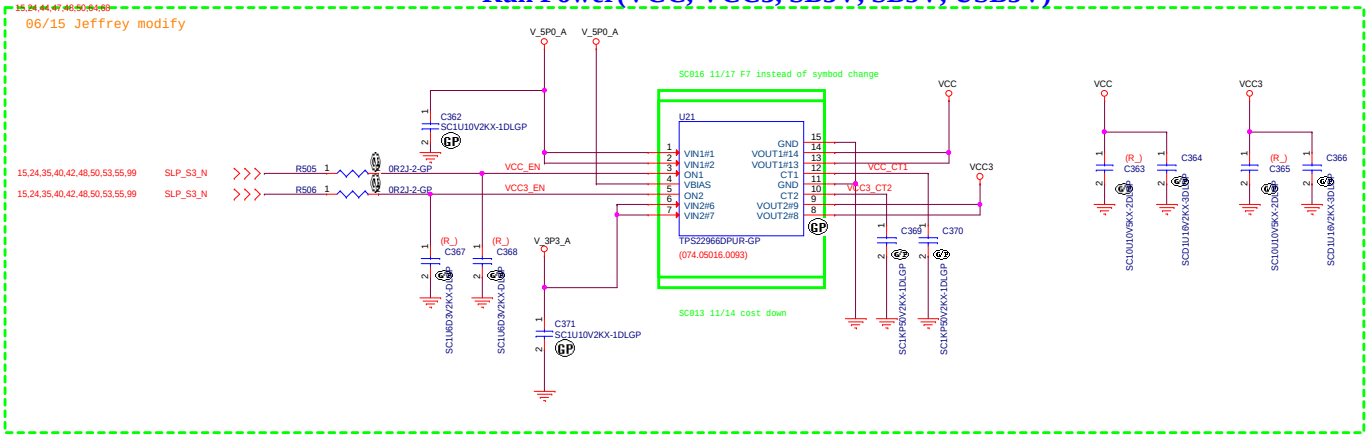
Title: 041_DCIN

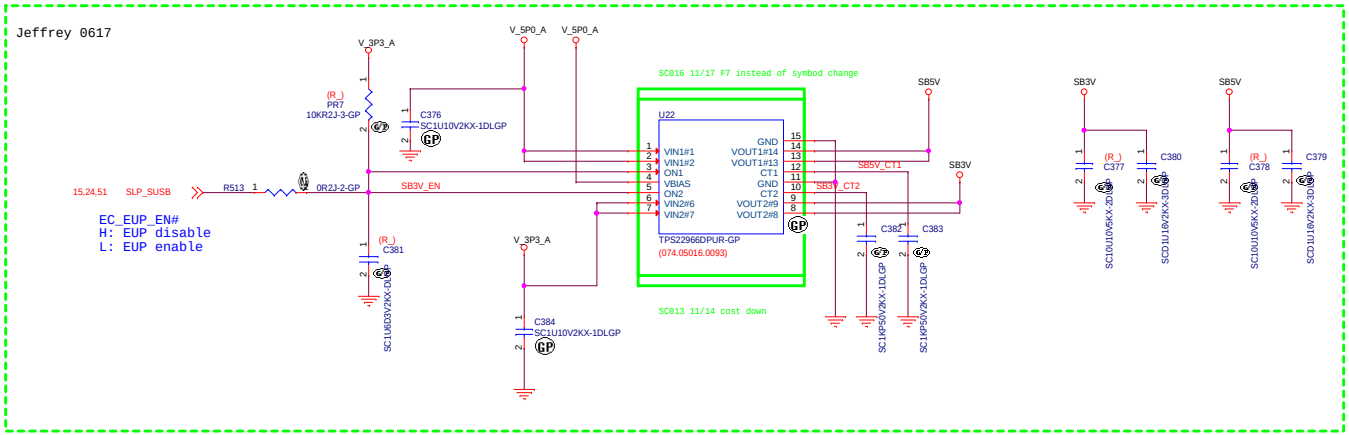
Size	Document Number	Rev
D	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 41 of 107

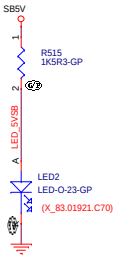
DCBATOUT — DCBATOUT 7,24,26,28,43,45,46,47,48,49,50,51,53,55,58,59,86,88
V_3P3_A — V_3P3_A 15,21,24,25,28,29,43,49,64,99
V_5P0_A — V_5P0_A 15,27,49,51
VCC — VCC 15,24,26,27,41,44,45,46,55,56,57,58,60,64,67,68,86,88
VCC3 — VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,44,47,48,50,53,55,56,58,59,61,62,64,67,68,86,99
VCC5_USB — VCC5_USB 34,35,62
SB3V — SB3V 4,15,17,18,20,21,24,25,31,35,38,40,47,48,51,53,55,56,57,58,59,61,64,86
SB5V — SB5V 15,24,44,47,48,50,51,53

Run Power(VCC, VCC3, SB3V, SB5V, USB5V)

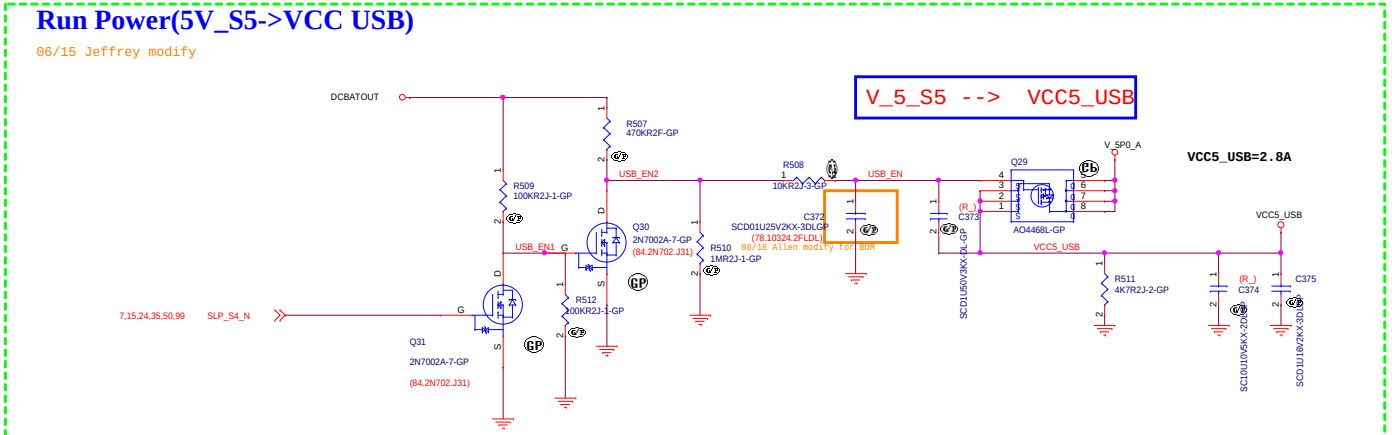




VCC5SB LED



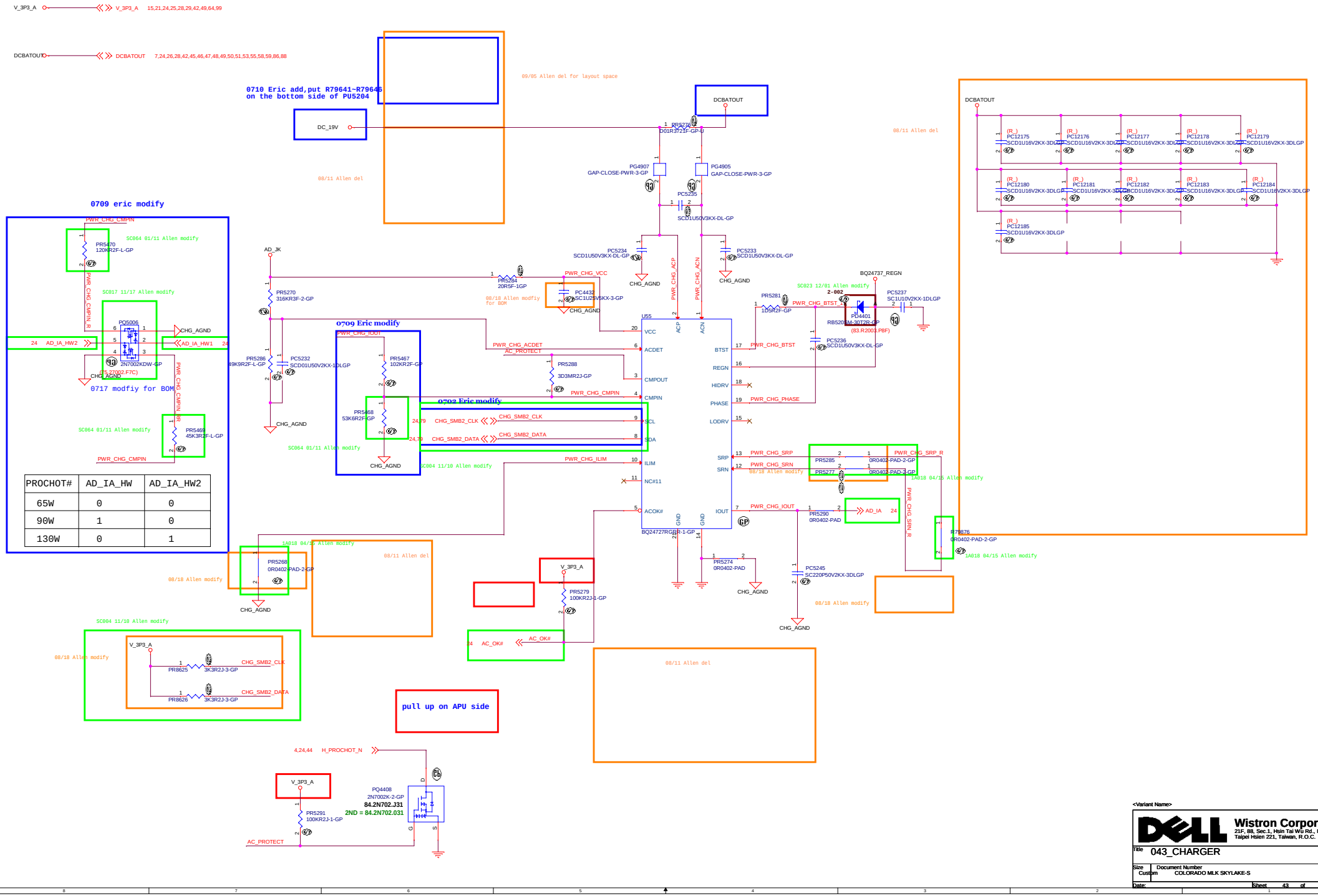
Run Power(5V_S5->VCC USB)



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	042_Run PWR/USB/DSWPWR	
Size C	Document Number COLORADO MLK SKYLAKE-S	Rev -2
Date:	Sheet 42 of 107	



<Variant Name>

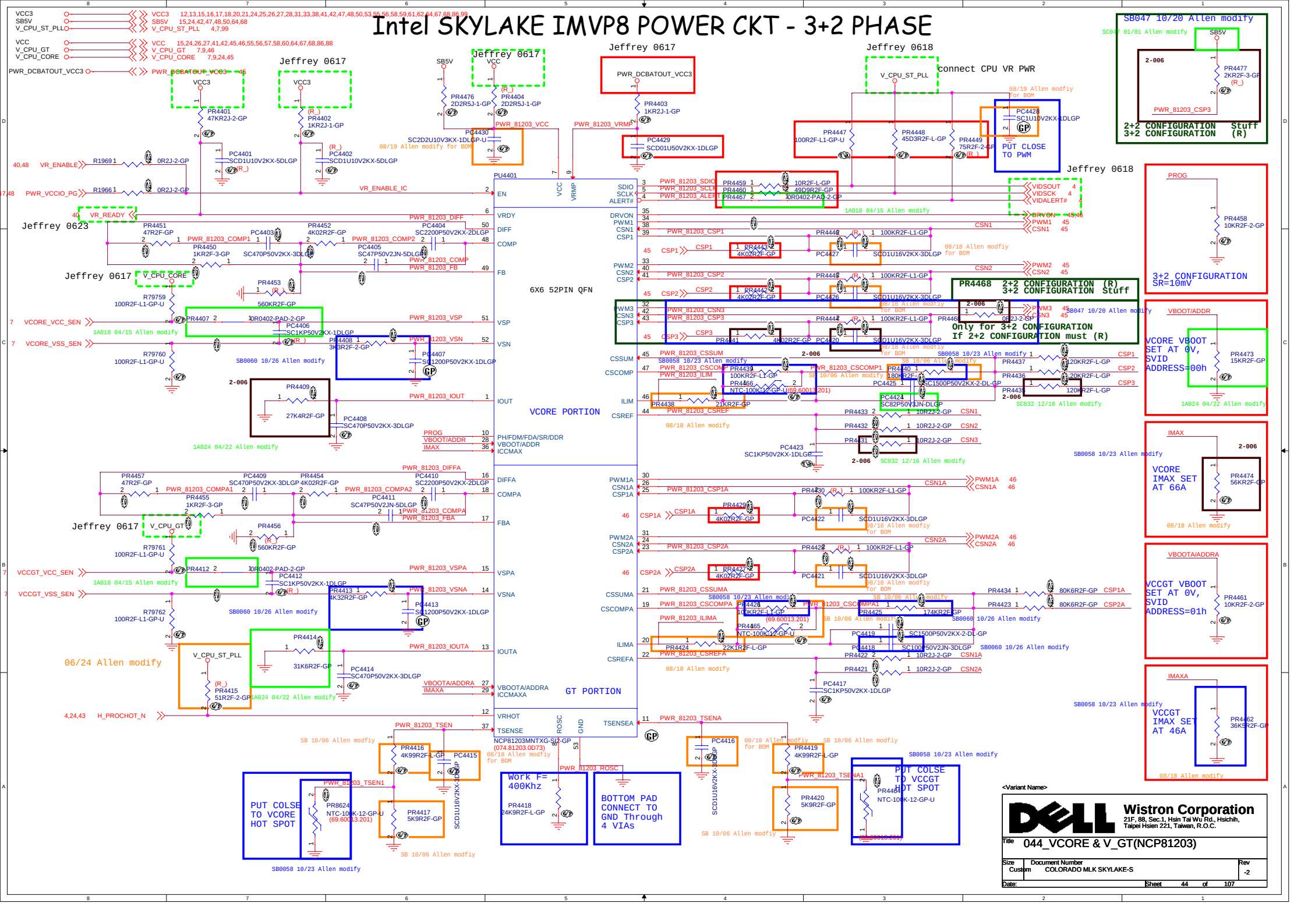
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

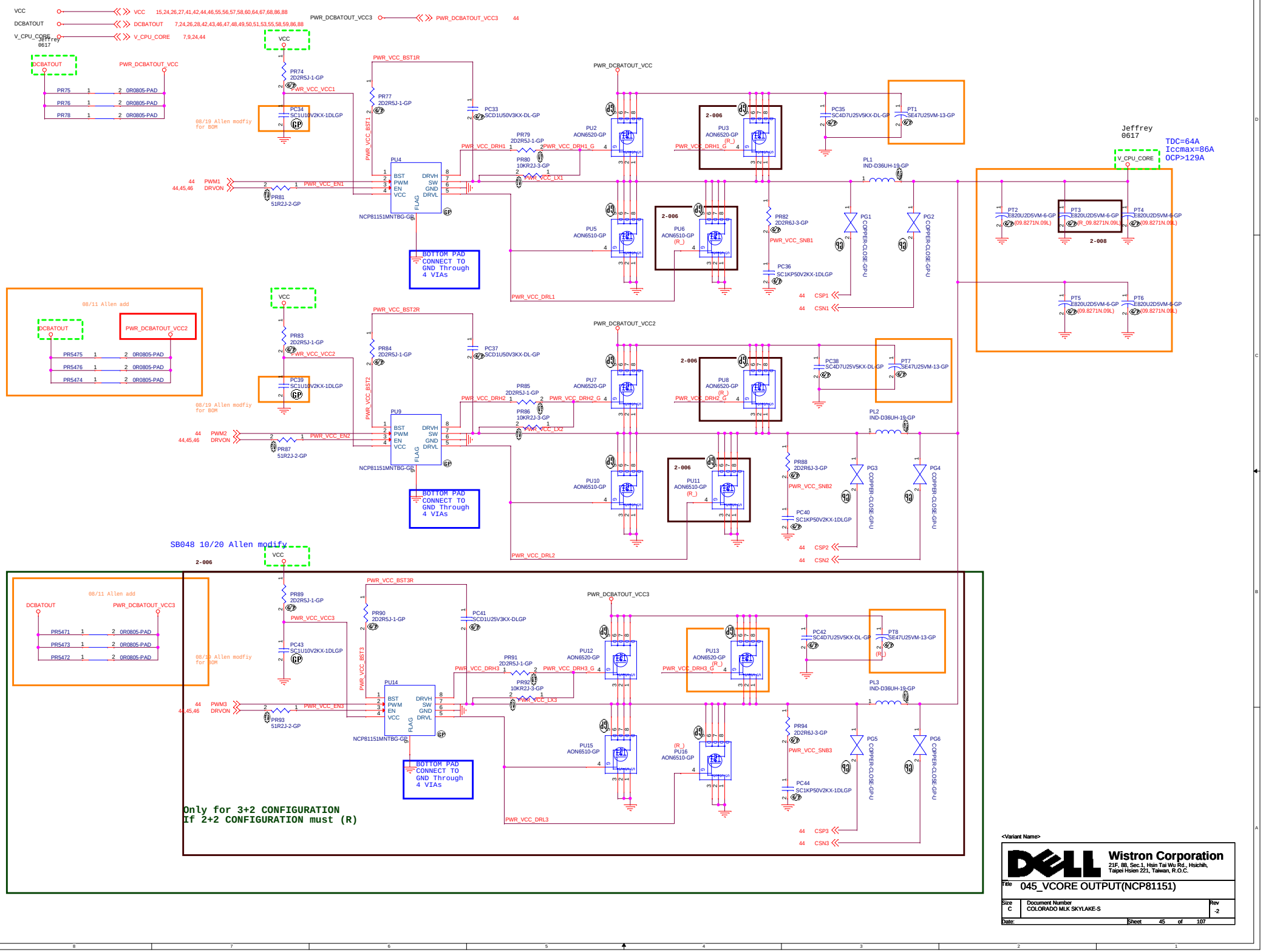
Title: 043_CHARGER

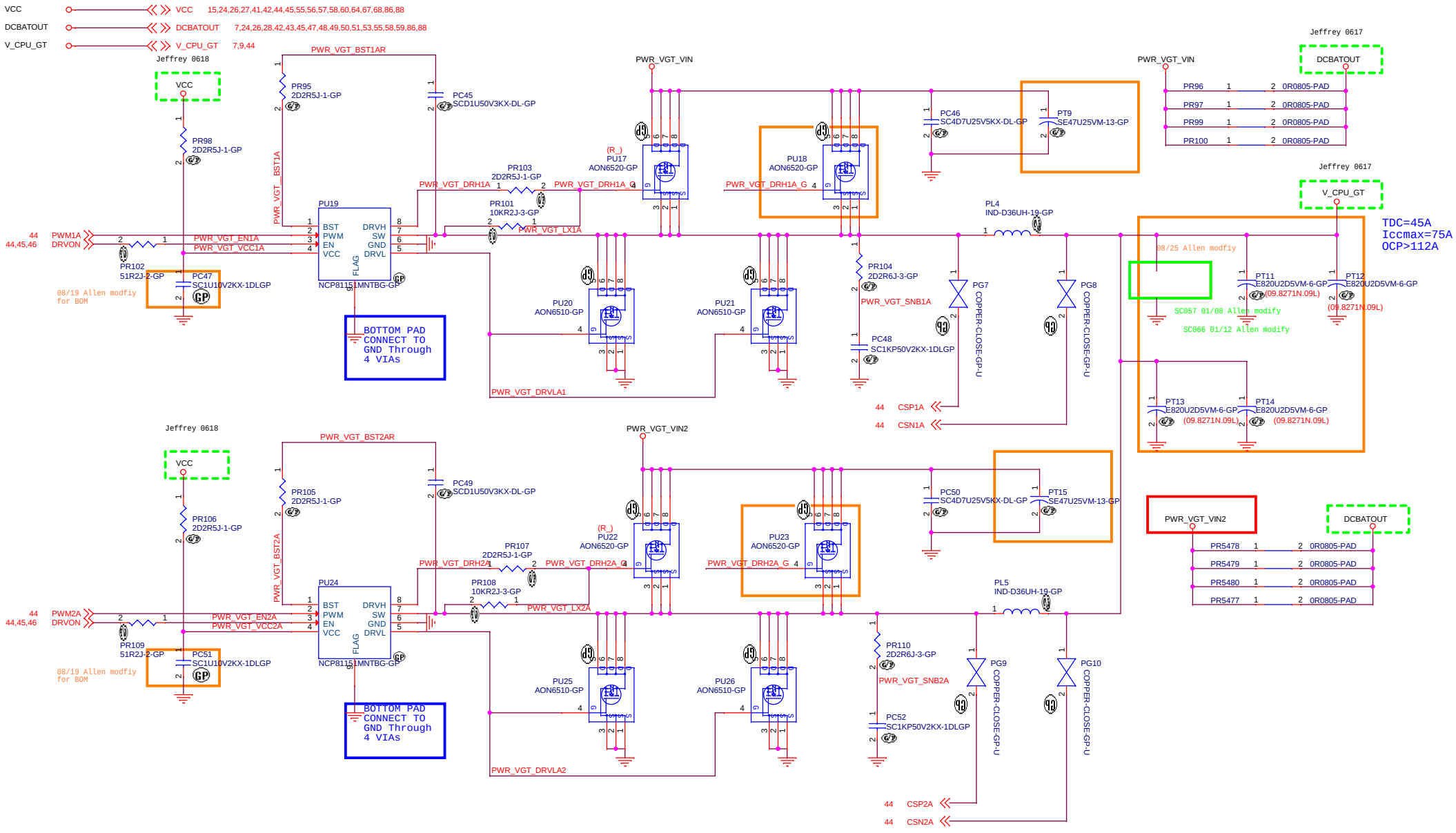
Size	Document Number	Rev
Custom	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 43 of 107

Intel SKYLAKE IMVP8 POWER CKT - 3+2 PHASE



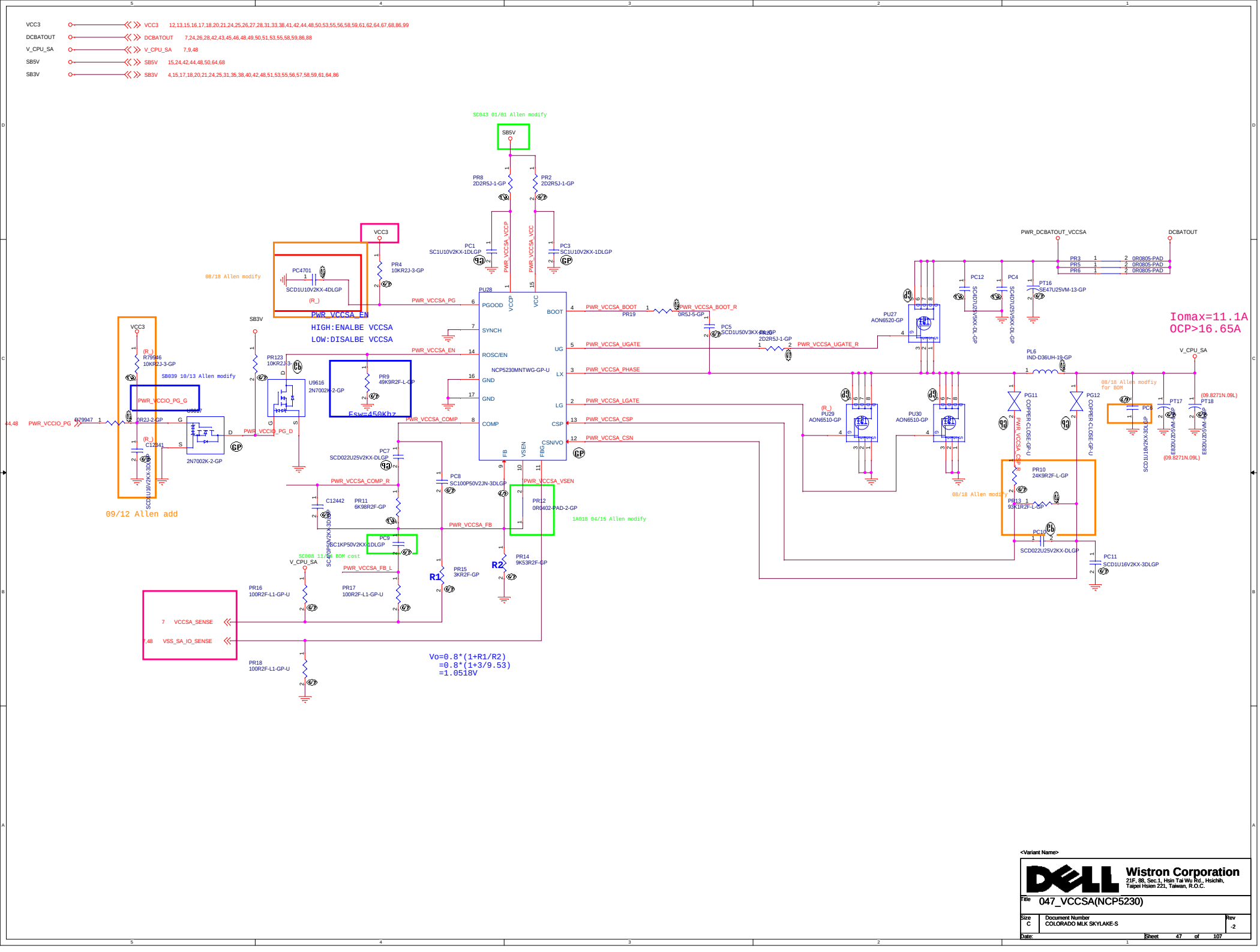

VCC
DCBATOUT
V_CPU_CORE
PWR_DCBATOUT_VCC3
Jeffrey
0617
PWR_DCBATOUT_VCC
PWR_DCBATOUT_VCC2
PWR_DCBATOUT_VCC3
PR74 2D2R5J-1-GP
PR75 0R0805-PAD
PR76 0R0805-PAD
PR78 0R0805-PAD
PC34 SC1U10V2KX-1DLGP
08/19 Allen modfiy for BOM
PR77 2D2R5J-1-GP
PC33 SCD1U50V3KX-DL-GP
PR79 2D2R5J-1-GP
PR80 10KR2J-3-GP
PU4
NCP81151MNTBG-GP
PWM1
DRVON
PR81 51R2J-2-GP
BOTTOM PAD CONNECT TO GND Through 4 VIAs
PU2 AON6520-GP
PU3 AON6520-GP (R_)
PU5 AON6510-GP
PU6 AON6510-GP (R_)
PC35 SC4D7U25V5KX-DL-GP
PT1 SE47U25VM-13-GP
PL1 IND-D36UH-19-GP
PR82 2D2R6J-3-GP
PC36 SC1KP50V2KX-1DLGP
PG1 COPPER-CLOSE-GPU
PG2 COPPER-CLOSE-GPU
PT2 E820U2D5VM-6-GP (09.8271N.09L)
PT3 E820U2D5VM-6-GP (R_09.8271N.09L)
PT4 E820U2D5VM-6-GP (09.8271N.09L)
PT5 E820U2D5VM-6-GP (09.8271N.09L)
PT6 E820U2D5VM-6-GP (09.8271N.09L)
TDC=64A
Iccmax=86A
OCP>129A
V_CPU_CORE
CSP1
CSN1
08/11 Allen add
PR5475 0R0805-PAD
PR5476 0R0805-PAD
PR5474 0R0805-PAD
PR83 2D2R5J-1-GP
PC39 SC1U10V2KX-1DLGP
PR84 2D2R5J-1-GP
PC37 SCD1U50V3KX-DL-GP
PR85 2D2R5J-1-GP
PR86 10KR2J-3-GP
PU9
NCP81151MNTBG-GP
PWM2
DRVON
PR87 51R2J-2-GP
BOTTOM PAD CONNECT TO GND Through 4 VIAs
PU7 AON6520-GP
PU8 AON6520-GP (R_)
PU10 AON6510-GP
PU11 AON6510-GP (R_)
PC38 SC4D7U25V5KX-DL-GP
PT7 SE47U25VM-13-GP
PL2 IND-D36UH-19-GP
PR88 2D2R6J-3-GP
PC40 SC1KP50V2KX-1DLGP
PG3 COPPER-CLOSE-GPU
PG4 COPPER-CLOSE-GPU
CSP2
CSN2
SB048 10/20 Allen modfiy
2-006
08/11 Allen add
PR5471 0R0805-PAD
PR5473 0R0805-PAD
PR5472 0R0805-PAD
PR89 2D2R5J-1-GP
PC43 SC1U10V2KX-1DLGP
PR90 2D2R5J-1-GP
PC41 SCD1U25V3KX-DLGP
PR91 2D2R5J-1-GP
PR92 10KR2J-3-GP
PU14
NCP81151MNTBG-GP
PWM3
DRVON
PR93 51R2J-2-GP
BOTTOM PAD CONNECT TO GND Through 4 VIAs
PU12 AON6520-GP
PU13 AON6520-GP (R_)
PU15 AON6510-GP
PU16 AON6510-GP (R_)
PC42 SC4D7U25V5KX-DL-GP
PT8 SE47U25VM-13-GP (R_)
PL3 IND-D36UH-19-GP
PR94 2D2R6J-3-GP
PC44 SC1KP50V2KX-1DLGP
PG5 COPPER-CLOSE-GPU
PG6 COPPER-CLOSE-GPU
CSP3
CSN3
Only for 3+2 CONFIGURATION
If 2+2 CONFIGURATION must (R)
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title 045_VCORE OUTPUT(NCP81151)
Size C
Document Number COLORADO MLK SKYLAKE-S
Rev -2
Date:
Sheet 45 of 107



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	046_V_GT OUTPUT(NCP81151)	
Size: Custom	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 46 of 107	



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	047_VCCSA(NCP5230)	
Size C	Document Number COLORADO MLK SKYLAKE-S	Rev -2
Date:	Sheet 47 of 107	

VCC3 — VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,42,44,47,50,53,55,56,58,59,61,62,64,67,68,86,99

DCBATOUT — DCBATOUT 7,24,26,28,42,43,45,46,47,49,50,51,53,55,58,59,86,88

V_CPU_IO — V_CPU_IO 4,5,7,8,9,99

SB5V — SB5V 15,24,42,44,47,50,64,68

SB3V — SB3V 4,15,17,18,20,21,24,25,31,35,38,40,42,47,51,53,55,56,57,58,59,61,64,86

V_CPU_SA — V_CPU_SA 7,9,47

Jeffrey 0617

VCC3

PR135 10KR2J-3-GP

44,47 PWR_VCCIO_PG

PWR_VCCIO_PG

PC4431 SC1KP50V2KX-1DLGP

PR136 75KR2F-GP

PWR_VCCIO_CS

PWR_VCCIO_EN

PWR_VCCIO_FB

PWR_VCCIO_RF

PC64 SC1KP50V2KX-1DLGP

PR143 470KR2F-GP

PU32

PGOOD
CS
EN
FB
RF
GND
BOOT
UGATE
PHASE
VCC
LGATE

RT8237CZQW-2-GP

PWR_VCCIO_BOOT

PWR_VCCIO_UGATE

PWR_VCCIO_PHASE

PWR_VCCIO_LGATE

PR139 2D2R3-1-U-GP

PWR_VCCIO_BOOT_R

PC62 SCD1U50V2KX-DL-GP

OSB5V

PC63 SC1U10V2KX-1DLGP

SC043 01/01 Allen modify

Jeffrey 0617

PU31 AON7410-GP

PU33 AON7506-GP

PC61 SC4D7U25V5KX-DL-GP

PC117 SC4D7U25V5KX-DL-GP

PWR_DCBATOUT_VCCIO

PR133 0R0805-PAD

PR134 0R0805-PAD

PL7 IND-1D5UH-53-GP

PR145 2D2R5J-1-GP

PWR_VCCIO_SW

08/11 Allen modify

PR4801 100R2F-L1-GP-U

PC66 SCD1U16V2KX-3DLGP

PT20 EB20U2D5VM-1GP

(09.8271N.09L)

08/18 Allen modify for BOM

Jeffrey 0617

DCBATOUT

Iomaax=5.4A
OCP>8.1A

PWR_VCCIO

PC65 SC1KP50V2KX-1DLGP

Jeffrey 0617

V_CPU_IO

PR137 0R0805-PAD

PR138 0R0805-PAD

PR140 0R0805-PAD

PR141 0R0805-PAD

PR142 0R0805-PAD

PR144 0R0805-PAD

PWR_VCCIO

V_CPU_SA

R1985 0R6J-L-GP

R1986 0R6J-L-GP

07/07 Allen Add

SC052 1/7 Allen modify

VCC3

R1961 10KR2J-3-GP

VCC3

R1964 10KR2J-3-GP

SB3V

R1963 100KR2J-1-GP

PWR_VCCIO_EN_R

R1968 0R2J-2-GP PWR_VCCIO_EN

R1967 0R2J-2-GP VR_ENABLE

VR_ENABLE 40,44

U173

PWR_VCCIO_EN_G1

PWR_VCCIO_EN_G2

2N7002KDW-1-GP

C12055 SCD1U16V2KX-3DLGP

08/18 Allen modfiy for BOM

SC052 1/7 Allen modify

15,24,35,40,42,50,53,55,99 SLP_S3_N

R80228 2KR2F-3-GP PWR_VCCIO_EN_G1

1A006 03/20 Allen modify

Vout = 0.704*(1+R1/R2)
= 0.704*(1+11.8/33)
= 0.9557V

PWR_VCCIO_FB_R

PR4802 VCCIO_SENSE 0R0402-PAD-2-GP

VCCIO_SENSE 7

1A018 04/15 Allen modify

07/08 Power modify

PR146 11K8R2F-GP

R1

PC67 SC18P50V2JN-1DLGP

PWR_VCCIO_FB

PR147 33KR2F-GP

R2

08/11 Allen modify

PR4803 VSS_SA_IO_SENSE 0R0402-PAD-2-GP

VSS_SA_IO_SENSE 7,47

1A018 04/15 Allen modify

07/08 Power modify

R79948 100R2F-L1-GP-U

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title 048_VCCIO(RT8237)

Size A3 | Document Number COLORADO MLK SKYLAKE-S | Rev -2

Date: | Sheet 48 of 107

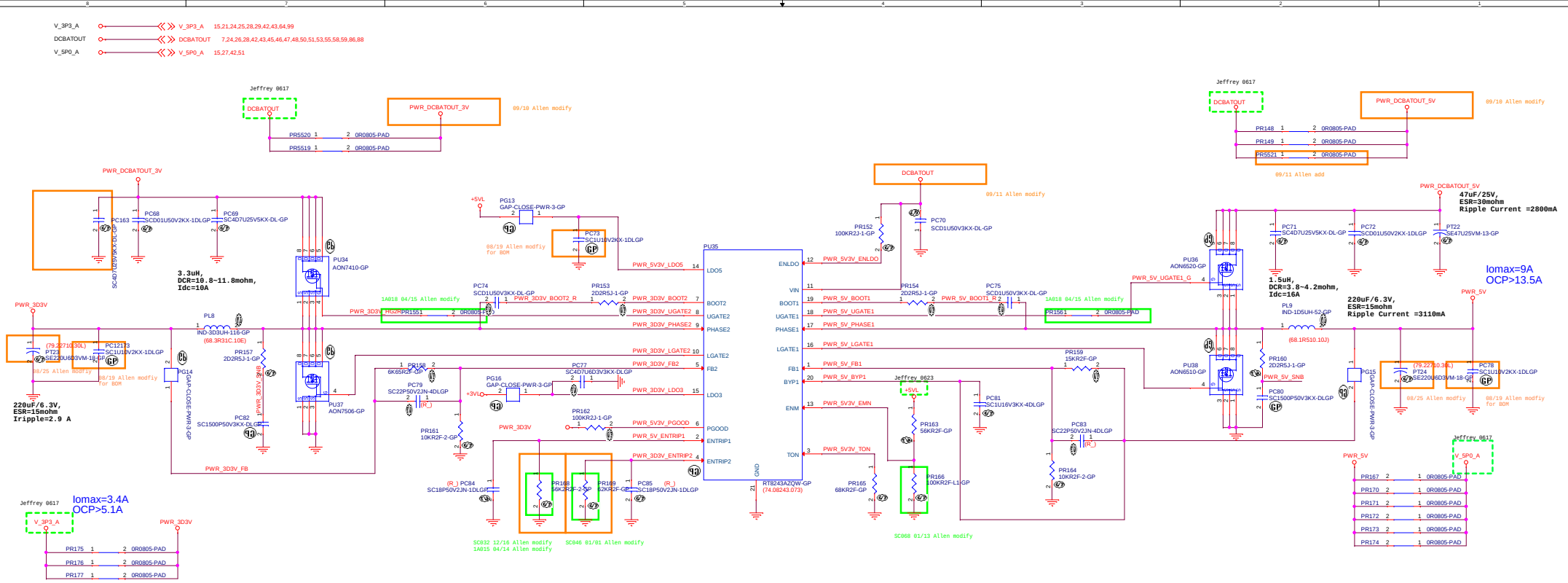


Table 2. Power Up Sequencing(RT8243A)

ENLDO(V)	SECFB	ENTRIP1	ENTRIP2	LDO5(V)	LDO3(V)	SMPS1	SMPS2
LOW	LOW	X	X	Off	Off	Off	Off
>1.6V =>High	LOW	X	X	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	Off	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	On	On	On	Off	On
>1.6V =>High	>2.3V =>High	On=>PD	On=>PD	On	On	On	On
>1.6V =>High	>2.3V =>High	On	Off	On	On	On	On

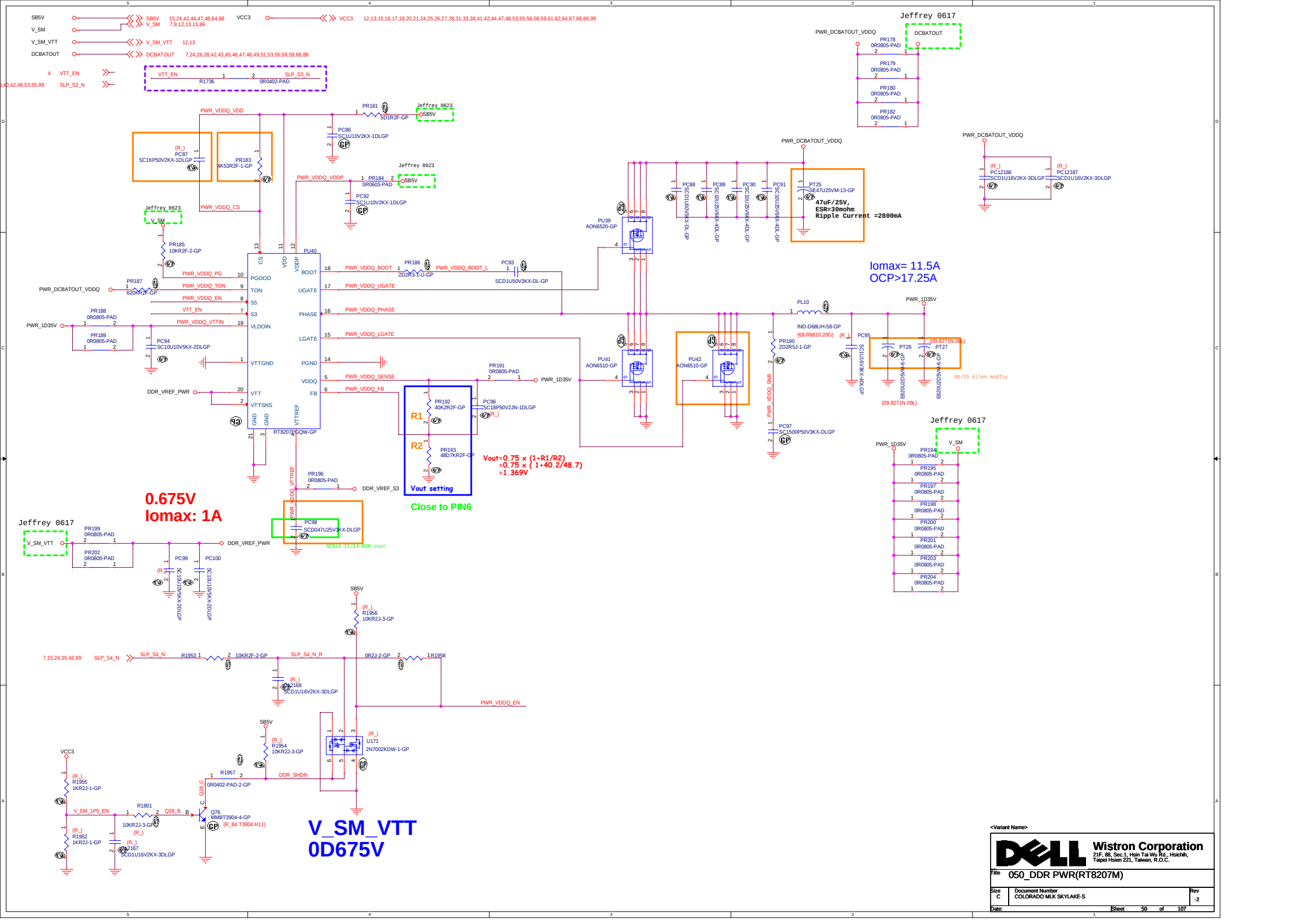
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 049_5V & 3.3V(RT8243A)

Size	Document Number	Rev
Custom	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 49 of 107



<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

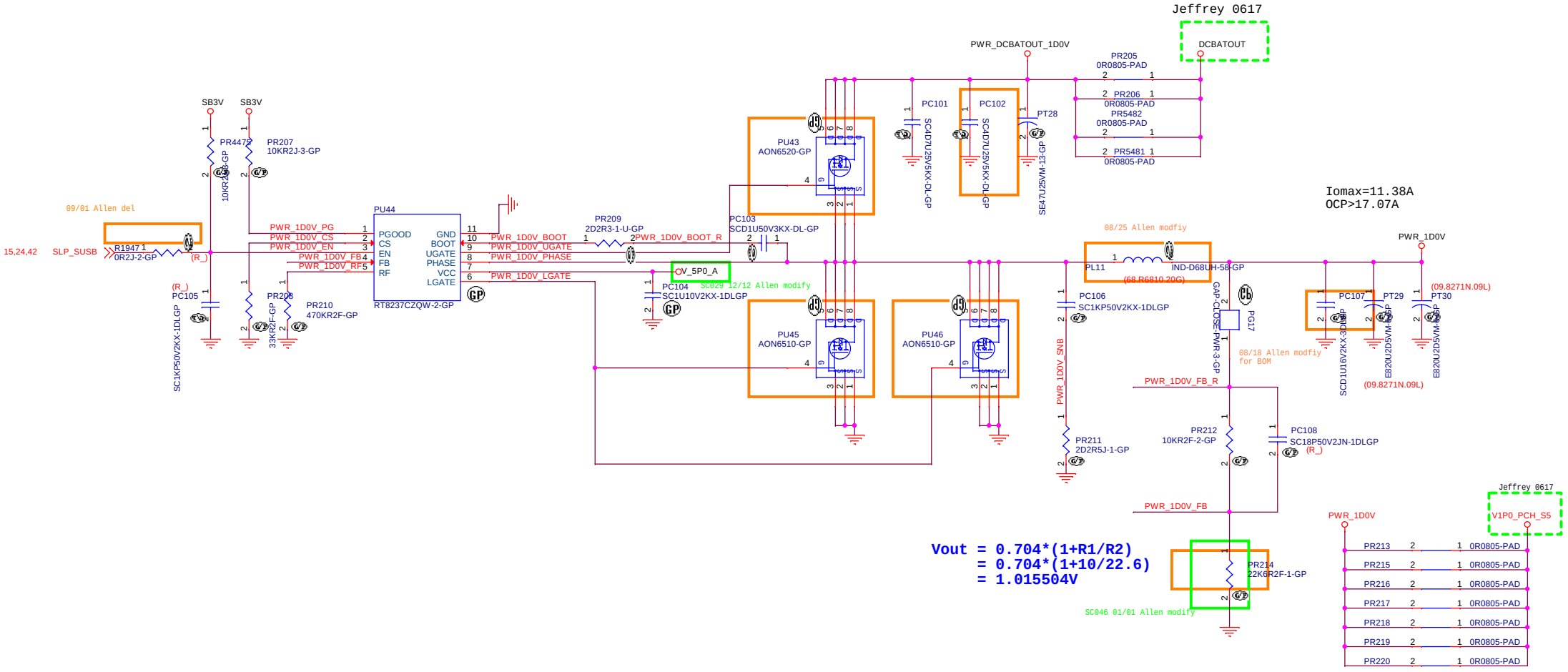
Title	050_DDR PWR(RT8207M)	
Size C	Document Number COLORADO MLK SKYLAKE-S	Rev -2
Date:	Sheet 50 of 107	

SB3V — SB3V 4,15,17,18,20,21,24,25,31,35,38,40,42,47,48,53,55,56,57,58,59,61,64,86

DCBATOUT — DCBATOUT 7,24,26,28,42,43,45,46,47,48,49,50,53,55,58,59,86,88

V1P0_PCH_S5 — V1P0_PCH_S5 7,15,21,99

V_5P0_A — V_5P0_A 15,27,42,49



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	051_PCH 1D0V(RT8237)	
Size A3	Document Number COLORADO MLK SKYLAKE-S	Rev -2
Date:	Sheet 51 of 107	

08/27 Allen del

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

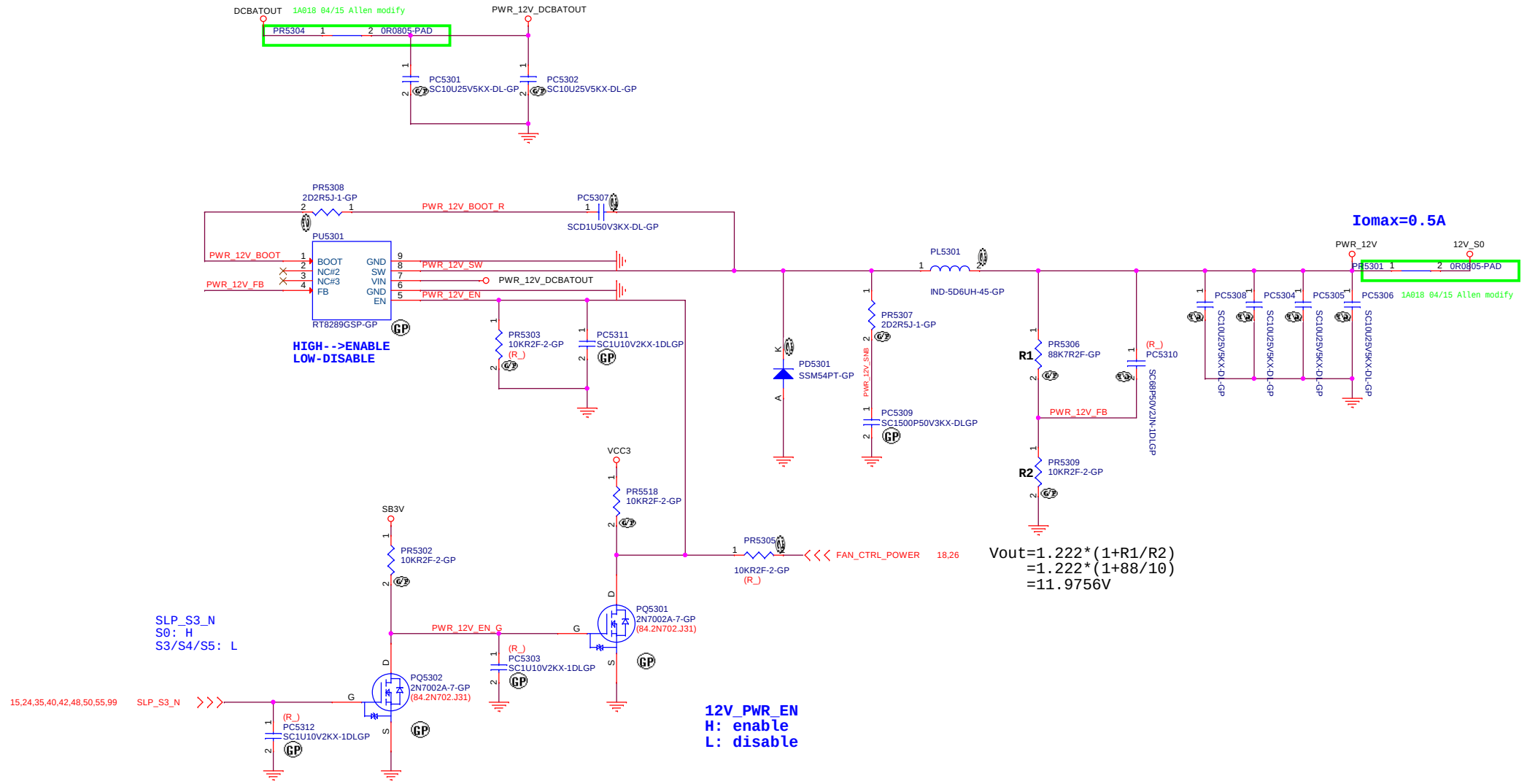
Size	Document Number	Rev
A3	COLORADO MLK SKYLAKE-S	-2

DCBATOUT
12V_S0

DCBATOUT 7,24,26,28,42,43,45,46,47,48,49,50,51,55,58,59,86,88
12V_S0 26

VCC3
SB3V

VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,42,44,47,48,50,55,56,58,59,61,62,64,67,68,86,99
SB3V 4,15,17,18,20,21,24,25,31,35,38,40,42,47,48,51,55,56,57,58,59,61,64,86



En Threshold	Logic Low Voltage	V_{IL}		--	--	0.4	V
	Logic High Voltage	V_{IH}		1.4	--	5.5	V

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title 053_12V(RT8289)

Size	Document Number	Rev
A3	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 53 of 107

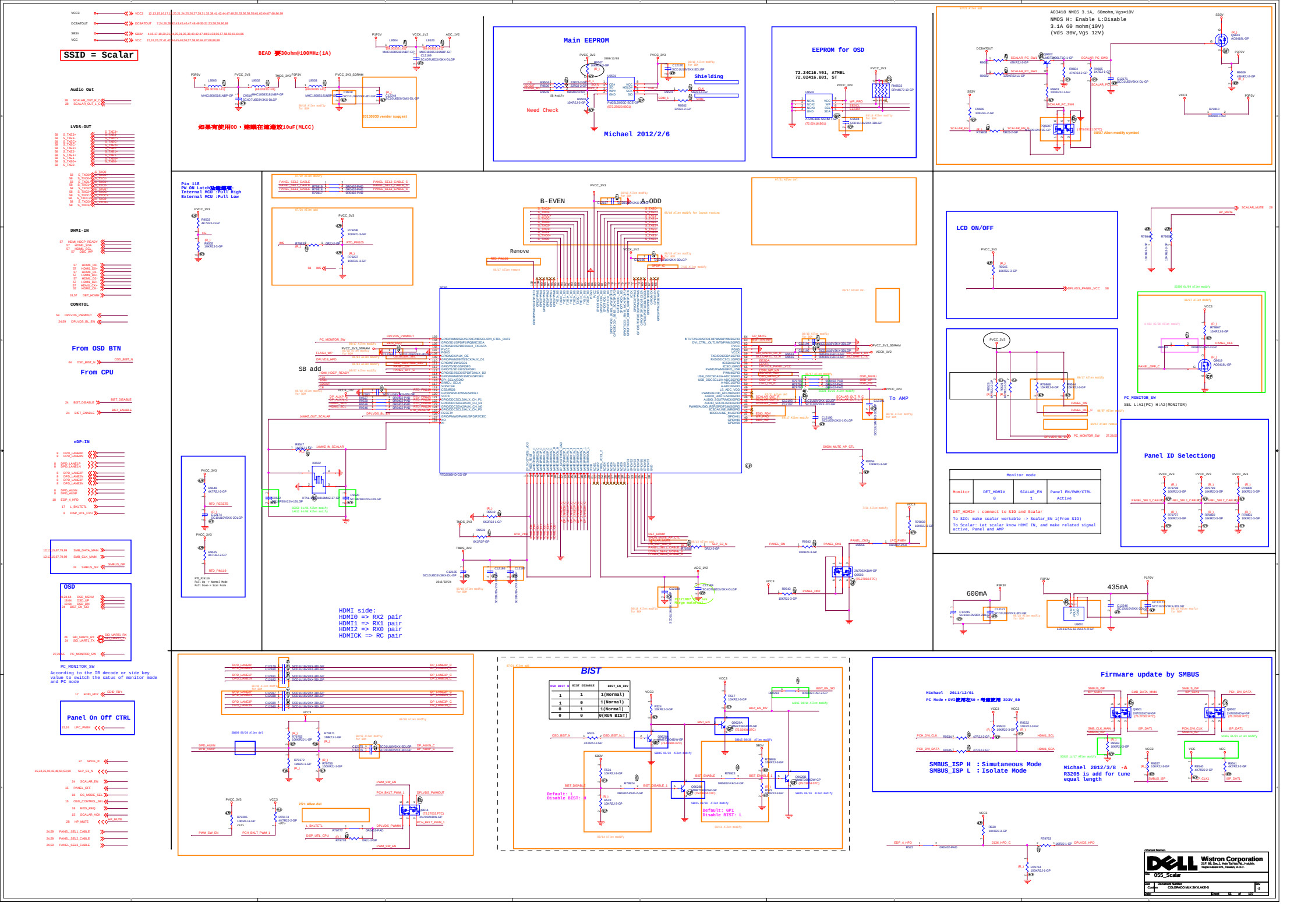
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
Custom	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 54 of 107


SSID = Scalar
Audio Out
LVDS-OUT
DHMI-IN
CONRTOL
From OSD BTN
From CPU
eDP-IN
OSD
PC_MONITOR_SW
According to the IR decode or side key value to switch the satus of monitor mode and PC mode
Panel On Off CTRL
BEAD 要30ohm@100MHz(1A)
如果有使用OD，建議在這邊放10uF(MLCC)
Main EEPROM
Need Check
Michael 2012/2/6
Shielding
EEPROM for OSD
72.24C16.Y01, ATMEL
72.02416.B01, ST
AO3418 NMOS 3.1A, 60mohm,Vgs=10V
NMOS H: Enable L:Disable
3.1A 60 mohm(10V)
(Vds 30V,Vgs 12V)
B-EVEN
A-ODD
Remove
SB add
Pin 118
PW ON Latch功能選擇
Internal MCU :Pull high
External MCU :Pull Low
LCD ON/OFF
To AMP
PC_MONITOR_SW
SEL L:A1(PC) H:A2(MONITOR)
Monitor mode
Monitor | DET_HDMI# 0 | SCALAR_EN 1 | Panel EN/PWM/CTRL Active
DET_HDMI# : connect to SIO and Scalar
To SIO: make scalar workable -> Scalar_EN 1(From SIO)
To Scalar: Let scalar know HDMI IN, and make related signal active, Panel and AMP
Panel ID Selectiong
600mA
435mA
HDMI side:
HDMI0 => RX2 pair
HDMI1 => RX1 pair
HDMI2 => RX0 pair
HDMICK => RC pair
BIST
Firmware update by SMBUS
Michael 2011/12/01
PC Mode + 3V3使用在S0 + 考慮使用 3D3V_S0
SMBUS_ISP H : Simutaneous Mode
SMBUS_ISP L : Isolate Mode
Michael 2012/3/8 -A
R3205 is add for tune equal length
Wistron Corporation
055_Scalar
COLORADO MLK SKYLAKE-S

VCC3
SB3V
VCC

12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,42,44,47,48,50,53,55,58,59,61,62,64,67,68,86,99
4,15,17,18,20,21,24,25,31,35,38,40,42,47,48,51,53,55,57,58,59,61,64,86
15,24,26,27,41,42,44,45,46,55,57,58,60,64,67,68,86,88

HDMI

8 DDSP_B_TX_DP_0
8 DDSP_B_TX_DN_0
8 DDSP_B_TX_DP_1
8 DDSP_B_TX_DN_1
8 DDSP_B_TX_DP_2
8 DDSP_B_TX_DN_2
8 DDSP_B_TX_DP_3
8 DDSP_B_TX_DN_3
18 DDPB_CTRL_CLK
18 DDPB_CTRL_DATA
18 DDSP_B_HPD
24 EC_HDMI_PD_N

09/17 Allen modify

HDMI

08/12 Allen modify

VCC
F7 POLYSW-1DS46V-12-GP
V_5P0_HDMI_CONN
L25
0R0805-PAD
08/18 Allen modify for BOM
C13199
C419
SCD1U16V2KX-2DLGP
V_5P0_HDMI_CONN
HDMI1
+5V_POWER
HDMI_LANE2_DP
HDMI_LANE2_DN
HDMI_LANE1_DP
HDMI_LANE1_DN
HDMI_LANE0_DP
HDMI_LANE0_DN
HDMI_LANE3_DP
HDMI_LANE3_DN
TMDS_DATA0+
TMDS_DATA0-
TMDS_DATA1+
TMDS_DATA1-
TMDS_DATA2+
TMDS_DATA2-
TMDS_DATA0_SHIELD
TMDS_DATA1_SHIELD
TMDS_DATA2_SHIELD
TMDS_CLOCK_SHIELD
TMDS_CLOCK+
TMDS_CLOCK-
SCL
SDA
CEC
DDC/CEC_GROUND
HOT_PLUG_DETECT
RESERVED#14
GND
HDMI (A_Type)
SKT-HDMI22-12-GP
(062.10012.0191)
DDPB_CTRL_CLK_CONN
DDPB_CTRL_DATA_CONN
DDSP_B_HPD_CONN

ESD

U26 (R_)
U28 (R_)
U29 (R_)
LINE_1
LINE_2
LINE_3
LINE_4
NC#6
NC#7
NC#9
NC#10
GND
AZ1045-04F-R7G-GP

Reserved for HDMI re-Driver

V_1P5

08/11 Allen modify
U119
INPUT
OUTPUT
ADJ/GND
AZ1117CR-ADJTRG1-GP
(074.01117.0038)
C3367
SC10U10V5KX-2DLGP
C3366
SCD1U16V2KX-3DLGP
R2081
180R3F-GP
R2
R1
R1592
36R3F-GP
1117 ADJ
Vout = 1.25*(1+R1/R2)

mount if use
R1594 CFG
R2087 DCIN_EN
R1593 EQ
R1596 SET
R1598 DDCBUF
R2088 PRE
R2089
R2090
R2091
R2092
4K7R2F-GP
(R_)

U118
VDD33
VDDRX
VDDTX
VDDTA
IN_D0P
IN_D0N
IN_D1P
IN_D1N
IN_D2P
IN_D2N
IN_CKP
IN_CKN
SCL_SRC
SDA_SRC
HPD_SRC
HPD_SNK
REXT
OUT_D0P
OUT_D0N
OUT_D1P
OUT_D1N
OUT_D2P
OUT_D2N
OUT_CKP
OUT_CKN
I2C_CTL_EN
EQ/I2C_ADDR0
CFG/I2C_ADDR1
PRE
SET
PDn
DCIN_EN
DDCBUF/SDA_CTL
SCL_SNK
SDA_SNK
GND
PS8407ATQFN40SGTR2-A1-GP
(71.08201.G03)
2-007
R2082
4K99R2F-L-GP
HDMI_DATA_IC_P0
HDMI_DATA_IC_N0
HDMI_DATA_IC_P1
HDMI_DATA_IC_N1
HDMI_DATA_IC_P2
HDMI_DATA_IC_N2
HDMI_DATA_IC_P3
HDMI_DATA_IC_N3
SCD1U10V2KX-4DLGP
(81.10421.2F1.DL)
0702 Eric modify

D23
1SS355-6-GP
(83.01355.D1F)
SC001 10/30 Allen modify
VCC5_DDC_HDMI
R2083
2K2R2J-2-GP
R2084
2K2R2J-2-GP
SC003 11/18 Allen modify
SC007 10/07 Allen modify
C12400
SCD01U16V2KX-3DLGP
0702 Eric modify

TR16
TR17
TR18
TR19
FILTER-4P-120-GP
(068.MCF11.0001)
0702 Eric modify

0702 Eric modify

SB3V
R2091
10KR2J-3-GP
EC_HDMI_PD_N
PD_N
Q1249
2N7002A-7-GP
(R_84.2N702.J31)

SC007 11/14 BOM cost

V_1P5_HDMI
VCC3
C12207
C12206
C12205
C12204
C12203
C12202
C12201
C12200
SCD01U50V2KX-1DLGP
SCD1U16V2KX-3DLGP
Near Pin 19
Near Pin 20, 31
Near Pin 12, 40
Near Pin 11, 37

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 056_HDMI OUT

Size	Document Number	Rev
D	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 56 of 107

SB3V — SB3V 4,15,17,18,20,21,24,25,31,35,38,40,42,47,48,51,53,55,56,58,59,61,64,86

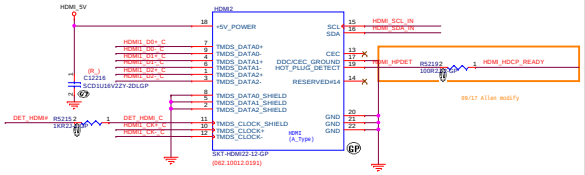
VCC — VCC 15,24,26,27,41,42,44,45,46,55,56,58,60,64,67,68,86,88

HDMI

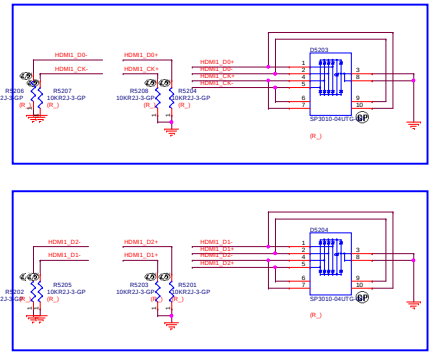
55 HDMI1_D2+
55 HDMI1_D2-
55 HDMI1_D1+
55 HDMI1_D1-
55 HDMI1_D0+
55 HDMI1_D0-
55 HDMI1_CK+
55 HDMI1_CK-
24,55 DET_HDMI#
55 DDC_WP
55 HDMI1_SDA
55 HDMI1_SCL
55 HDMI_HDCP_READY

HDMI-IN

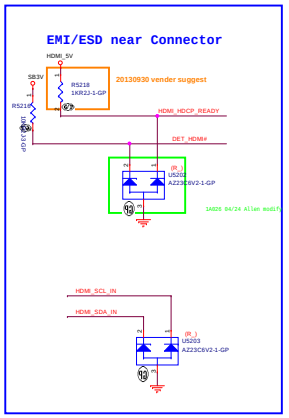
Connector



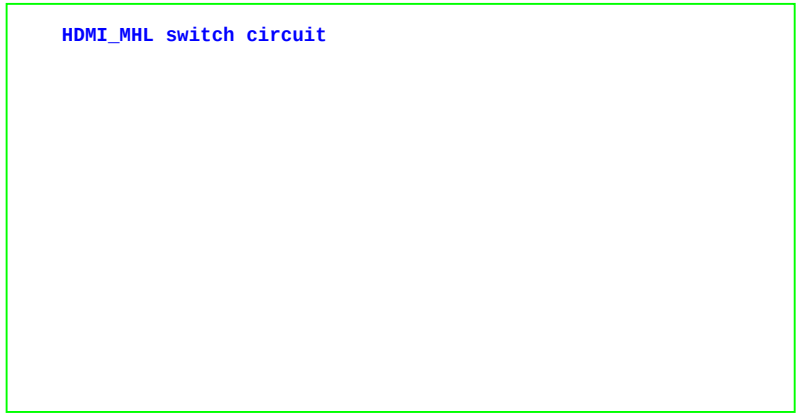
EMI/ESD near Connector

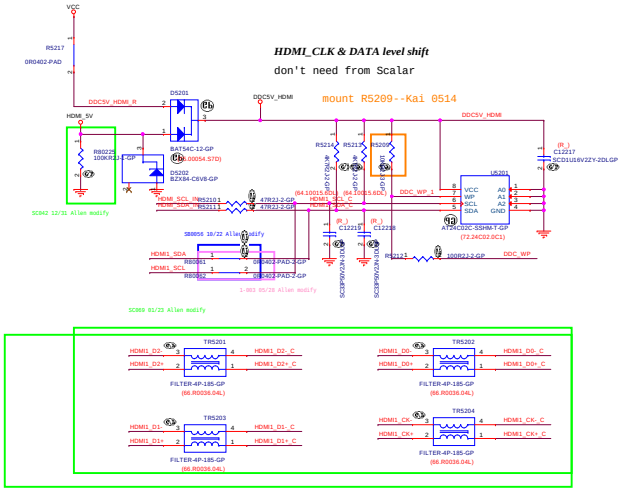


EMI/ESD near Connector



HDMI_MHL switch circuit





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 057_HDMI IN

Size	Document Number	Rev
D	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 57 of 107

SB3V — SB3V 4,15,17,18,20,21,24,25,31,35,38,40,42,47,48,51,53,55,56,57,59,61,64,86

VCC — VCC 15,24,26,27,41,42,43,45,46,55,56,57,60,64,67,68,86,88

VCC3 — VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,42,44,47,48,50,53,55,56,59,61,62,64,67,68,86,99

DCBATOUT — DCBATOUT 7,24,26,28,43,45,46,47,48,49,50,51,53,55,59,86,88

From RTD2136S to LVDS

55 S_TXE3+ — S_TXE3+
55 S_TXE3- — S_TXE3-
55 S_TXEC+ — S_TXEC+
55 S_TXEC- — S_TXEC-
55 S_TXE2+ — S_TXE2+
55 S_TXE2- — S_TXE2-
55 S_TXE1+ — S_TXE1+
55 S_TXE1- — S_TXE1-
55 S_TXE0+ — S_TXE0+
55 S_TXE0- — S_TXE0-

55 S_TXO0+ — S_TXO0+
55 S_TXO0- — S_TXO0-
55 S_TXO1+ — S_TXO1+
55 S_TXO1- — S_TXO1-
55 S_TXO2+ — S_TXO2+
55 S_TXO2- — S_TXO2-
55 S_TXOC+ — S_TXOC+
55 S_TXOC- — S_TXOC-
55 S_TXO3+ — S_TXO3+
55 S_TXO3- — S_TXO3-

GPIO

24 LVDS_DET_A*
24 LVDS_DET_B*
55 DPLVDS_PANEL_VCC — DPLVDS_PANEL_VCC
55 IMS

From RTD2136R

0624 Eric modify

S_TXO0+ / S_TXO0-
S_TXO1+ / S_TXO1-
S_TXO2+ / S_TXO2-
S_TXO3+ / S_TXO3-
S_TXOC+ / S_TXOC-
S_TXE0+ / S_TXE0-
S_TXE1+ / S_TXE1-
S_TXE2+ / S_TXE2-
S_TXE3+ / S_TXE3-
S_TXEC+ / S_TXEC-

09/11 Allen modify

LVDS1

ACES-CON60J-GP — LVDS1

S_TXO0- S_TXO0+ S_TXO1- S_TXO1+ S_TXO2- S_TXO2+ LVDS_PU_24 S_TXOC- S_TXOC+ S_TXO3- S_TXO3+ S_TXE0- S_TXE0+ S_TXE1- S_TXE1+ S_TXE2- S_TXE2+ S_TXEC- S_TXEC+ LVDS_PU_6 LVDS_PU_3 IMS

R79728 10KR2F-3-GP — VCC5_PANEL
R79730 10KR2F-3-GP — SB3V
LVDS_DET_A*
SC040 12/23 Allen modify
SC051 01/06 Allen modify
Q664B AO3413L-GP (84.02130.031) — VCC5_PANEL
R78718 100R2F-L1-GP-U
R11852 1KR2F-3-GP — VCC5_PANEL
7/31 Allen add
VCC5_PANEL
LVDS_DET_B_C*
C12220 C12221 C12222 SCCU1U105ZX0GBGS
R79811 0R2J-2-GP
Q103 2N7002A-7-GP (84.2N702.231)
R79732 10KR2J-3-GP — SB3V
LVDS_DET_B*
C12223 SCCU1U105ZX0GBGS

SC058 01/08 Allen modify

VCC5_PANEL
R80230 10KR2J-3-GP
BIST_PIN25_G
Q9650 2N7002A-7-GP (84.2N702.231)
BIST_PIN25
IMS for LG Interlace Mode Selection function

DCBATOUT
R79738 100KR2J-1-GP
R79727 470KR2F-GP
C12113 SC4D7U10V3KX-DL-GP
Q1261 2N7002A-7-GP (84.2N702.231)
PANEL_ON_3
R19 1MR2J-1-GP
C12134 SC101U25V2KX-3DL-GP
09/18 Allen modify for BOM
PANEL_ON_4
R79376 10KR2J-3-GP
Q1283 MMBT3904-4-GP-R (84.T3904.H11)
PANEL_ON_2
R42 10KR2J-3-GP
R79737 10KR2J-3-GP (R_)
VCC3
DPLVDS_PANEL_VCC
R79736 22R2J-2-GP
PANEL_ON_1
High: Enable
Low: Disable
Low: Enable
High: Disable

VCC
ADR4525J-GP
Main: 84.R5482.B3D
Alt: 84.08655.B3D
L62 HCB2012KF-600T30-GP (68.00335.121)
V_5_LCD1
V_5_LCD2
High: Enable
Low: Disable
R79735 330R1K-L-GP
PANEL_ON_5
Q1262 2N7002A-7-GP (84.2N702.231)

07/24 Allen modify for down size
VCC5_PANEL
F17 POLYSW-2A6V-7-GP
SB000 09/30 Allen del

<Variant Name>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 058_PANEL CONTROL

Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 58 of 107

DCBATOUT
VCC3
SB3V

24,55 PANEL_SEL1_CABLE
24,55 PANEL_SEL2_CABLE
24,55 PANEL_SEL3_CABLE

55 DPLVDS_PWMOUT
24,55 DPLVDS_BL_EN

24 SIO_SMCLK0
24 SIO_SMDAT0

0703 Eric modify

1st source: 83.3R010.C8M
2rd source: 83.3R010.A8M

07/24 Allen modify for down size

SB030 Allen modify for F7 BOM

1st source: 084.04286.0037
2rd source: 084.PA010.0037

0630 Eric Modify

23.8"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Vout
LG	1	0	0	3,4 Vout 1,2,3 RTN
BOE	1	1	0	3,4 Vout 1,2,3 RTN
AUO	1	0	1	3,4 Vout 1,2,3,4 RTN

23.8"Panel Model	PANEL_SEL1	PANEL_SEL2	PANEL_SEL3	Vout
LG	0	1	1	3,4 Vout 1,6 RTN
BOE	0	0	1	3,4 Vout 1,5,6 RTN
AUO	0	1	0	3,4 Vout 1,2,3,4 RTN

2-011

to EC SMBUS

closed to chip and cut AGND and DGND

7/21 Allen del

0703 Eric modify

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 059_OZ554A LED CONVERTER

Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 59 of 107

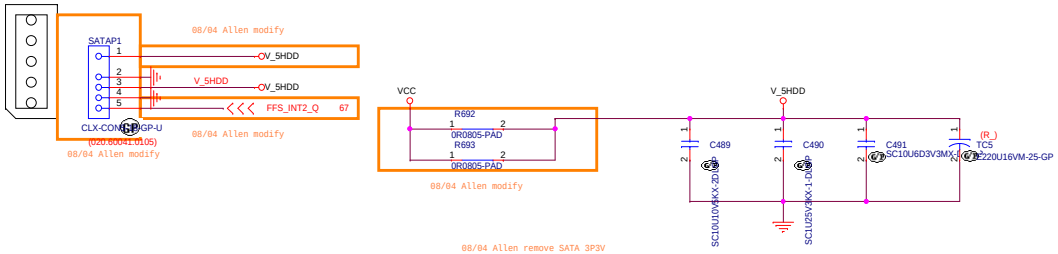
VCC — VCC 15,24,26,27,41,42,44,45,46,55,56,57,58,64,67,68,86,88

SATA

17 SATAHDR_RX_DP2
17 SATAHDR_RX_DN2
17 SATAHDR_TX_DN2
17 SATAHDR_TX_DP2
17 SATAHDR_RX_DP3
17 SATAHDR_RX_DN3
17 SATAHDR_TX_DN3
17 SATAHDR_TX_DP3

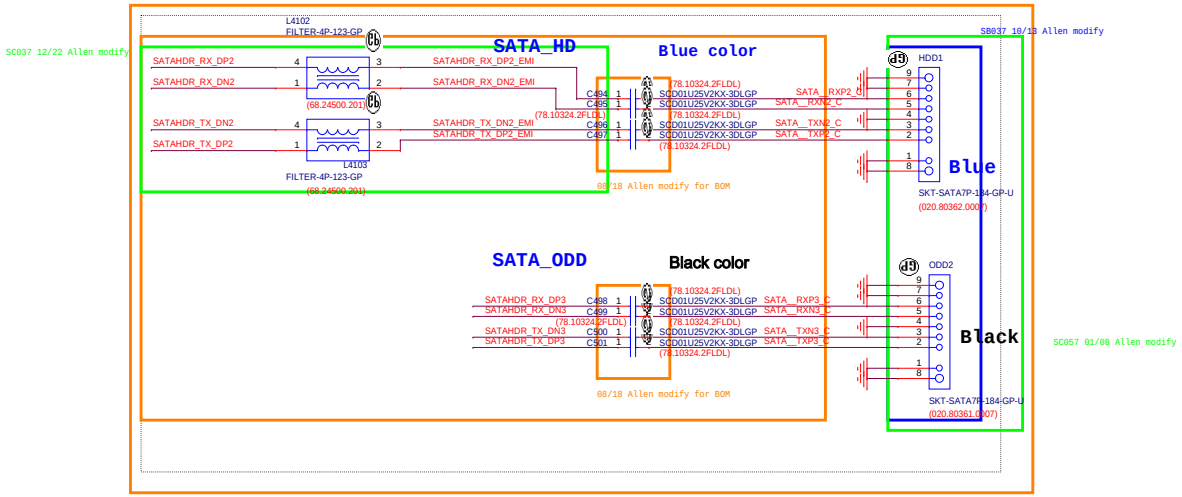
SATA

Layout: Please put them together



08/11 Allen modfiy SATA connector

06/26 Allen modify net name



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 060_HDD/ODD

Size: C | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 60 of 107

NGFF(A Key)

H:4.2mm

09/10 Allen remove

09/10 Allen remove

09/10 Allen remove

SB017 10/02 Allen modify

V_3P3_PCIVAUX DUAL

P-MOS

Discharge resistor

MINI CARD STAND OFF

Table 19. MLDIR Pin Termination

Display-Capability on Display-M.2 Card	Example	MLDIR Pin Termination on Display-M.2 Card
DisplayPort Sink	Card is a wireless display transmitter	Terminated directly to GND
DisplayPort Source	Card is a wireless display receiver	Terminated directly to +3.3V
DisplayPort Sink or Source	Card is configurable as either a wireless display transmitter or receiver	Hi-Z (single input load)

S0	S3	S5	DS
H	H	L	L

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 061_NGFF CONN

Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 61 of 107

VCC3 VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,42,44,47,48,50,53,55,56,58,59,61,64,67,68,86,99

VCC5_USB VCC5_USB 34,35,42

USB TOUCH PANEL

17 USB_PCH_DN8
17 USB_PCH_DP8
24 TP_DET GPIO

TOUCH PANEL

SB 09/30 Allen modify

VCC5_USB — F12 POLYSW-1D5A6V-12-GP (T_) — USBVCCTP

C520 SC10U10V5KX-2DLGP

TR13
USB_PCH_DP8 → USB_PCH_DP8_PP
USB_PCH_DN8 → USB_PCH_DN8_NN
MCM1012B900FBP-GP-U
(T_068.01012.2011)

FOR EMI

USB_PCH_DP8_PP
USB_PCH_DN8_NN
(R_) C522 SC10P50V2JN-4GS
(R_) C523 SC10P50V2JN-4GS

VCC3 — R738 10KR2J-3-GP — TP_DET

USBVCCTP

USB_PCH_DP8_PP
USB_PCH_DN8_NN

TOUCH2
ENT-CON5-GP

SB031 10/07 Allen modfiy symbol

SB014 09/30 Allen modify SMD for layout space

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 062_TOUCH

Size: C | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

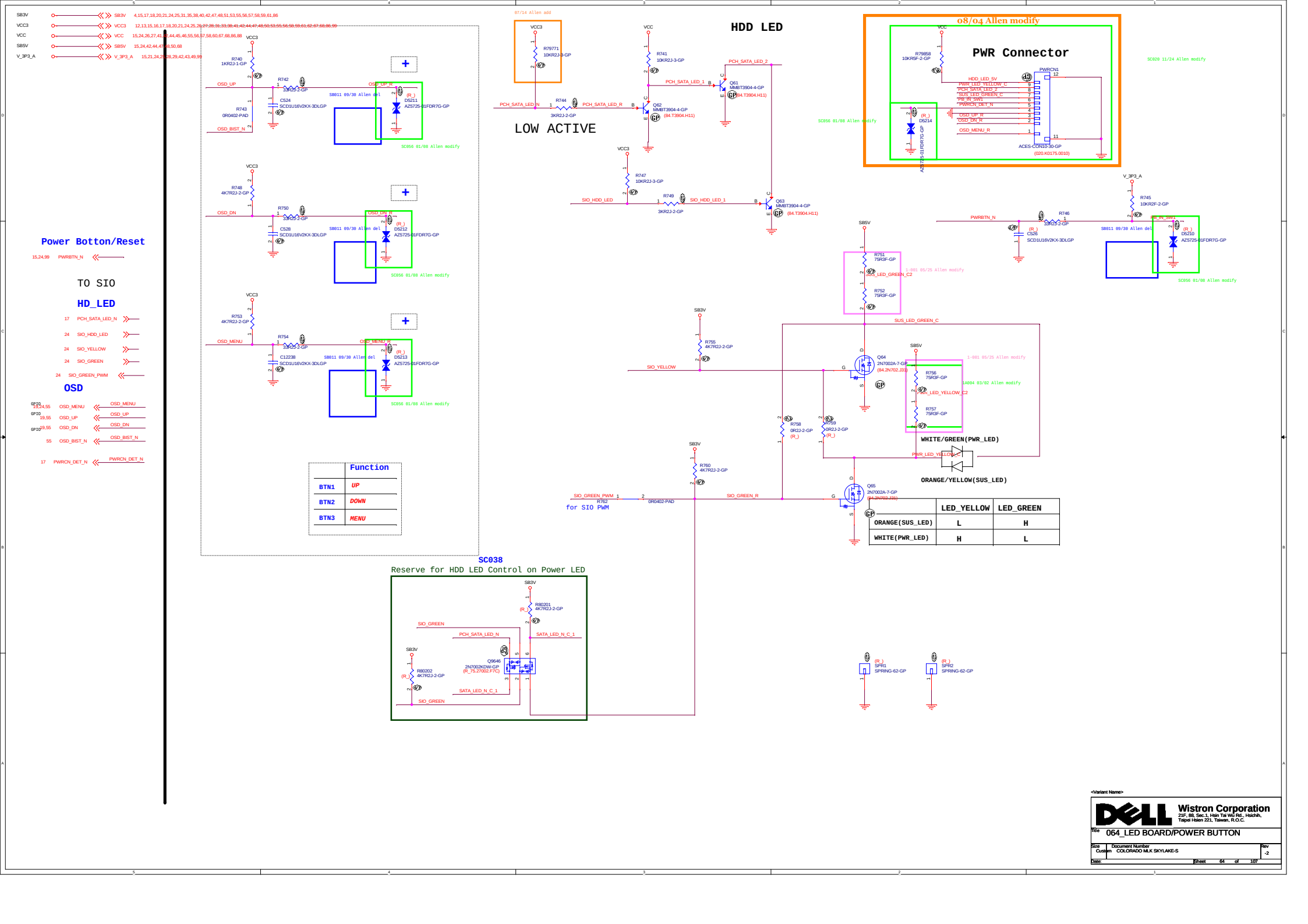
Date: | Sheet 62 of 107

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	-2
Date:	Sheet 63 of 107	


SB3V
VCC3
VCC
SB5V
V_3P3_A
HDD LED
LOW ACTIVE
08/04 Allen modify
PWR Connector
Power Botton/Reset
PWRBTN_N
TO SIO
HD_LED
PCH_SATA_LED_N
SIO_HDD_LED
SIO_YELLOW
SIO_GREEN_PWM
OSD
OSD_MENU
OSD_UP
OSD_DN
OSD_BIST_N
PWRCN_DET_N
Function
BTN1 UP
BTN2 DOWN
BTN3 MENU
WHITE/GREEN(PWR_LED)
ORANGE/YELLOW(SUS_LED)
for SIO PWM
LED_YELLOW
LED_GREEN
ORANGE(SUS_LED) L H
WHITE(PWR_LED) H L
SC038
Reserve for HDD LED Control on Power LED
Wistron Corporation
064_LED BOARD/POWER BUTTON
COLORADO MLK SKYLAKE-S

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 65 of 107

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A3	COLORADO MLK SKYLAKE-S	-2

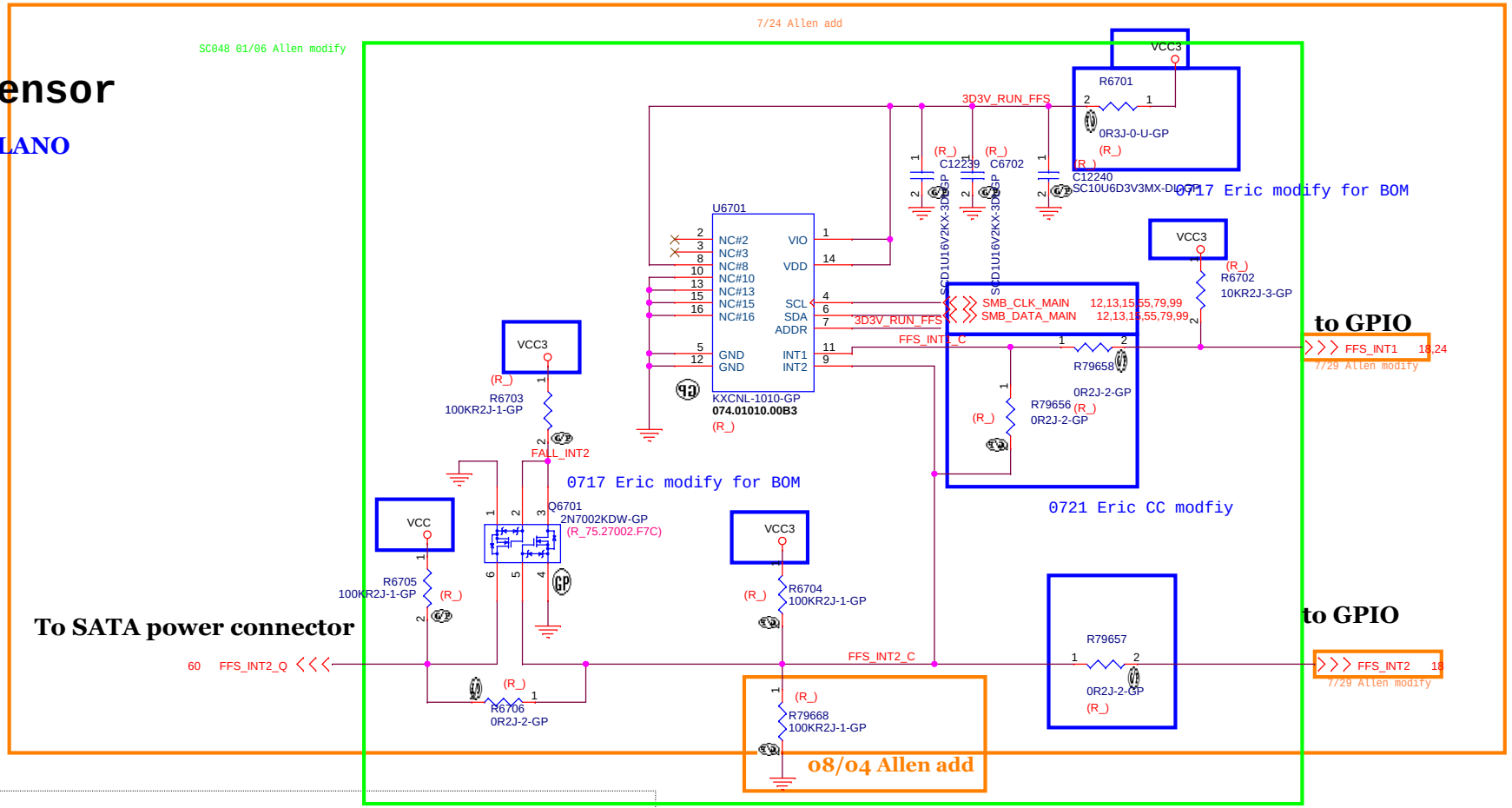
Date: Sheet 66 of 107

VCC — VCC 15,24,26,27,41,42,44,45,46,55,56,57,58,60,64,68,86,88

VCC3 — VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,42,44,47,48,50,53,55,56,58,59,61,62,64,68,86,99

Free Fall Sensor

0716 modfiy from PLANO



Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Variant Name>

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Title: 067_FFS		
Size: B	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 67 of 107	

SSID = DEBUG PORT

VCC — VCC — 15,24,26,27,41,42,44,45,46,55,56,57,58,60,64,67,86,88

VCC3 — VCC3 — 12,13,15,16,17,18,20,21,23,25,26,27,28,31,33,38,41,42,44,47,48,50,53,55,56,58,59,61,62,64,67,86,99

SB5V — SB5V — 15,24,42,44,47,48,50,64

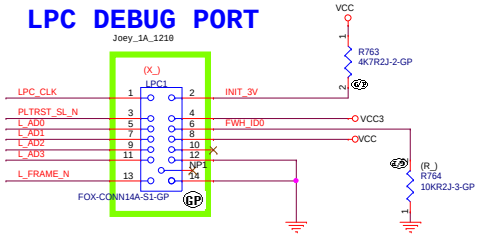
LPC DEBUG PORT

18,24 L_AD0
18,24 L_AD1
18,24 L_AD2
18,24 L_AD3
18,24 L_FRAME_N
18,24 LPC_CLK
24,76 PLTRST_SL_N

19 UART0_TX
19 UART0_RX

LPC DEBUG PORT

Joey_1A_1210

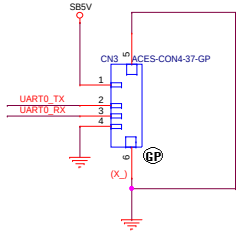


Pin height 2.3mm

Follow Eagle

08/04 Allen add

Pin height 2.3mm



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Title: 068_DEBUG CONNECTOR

Size: C | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 68 of 107

<Variant Name>

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Title

Size	Document Number	Rev
A	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 69 of 107

<Variant Name>

Reserved

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Title

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	SA

Date: Sheet 70 of 107

<Variant Name>

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Title

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 71 of 107

<Variant Name>

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Title: Reserved

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 73 of 107

<Variant Name>

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Title

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Title Reserved

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 75 of 107

+V_1P05_VGA +V_1P05_VGA 78,79,86

+V_3P3_VGA +V_3P3_VGA 79,80,86,88

PCIEX4

5 PEG_TXP[7..0]
5 PEG_TXN[7..0]

5 PEG_RXP[7..0]
5 PEG_RXN[7..0]

16,76 CK_PE_100M_16PORT_DP
16,76 CK_PE_100M_16PORT_DN

24,68,76 PLTRST_SL_N

79 PEX_RST_GPU

+V_3P3_VGA

R591 10KR2J-3-GP (G_)

PEX_CLKREQ

AMD_RST#_L — R1212 0R0402-PAD-2-GP — PEX_RST_GPU

100MHz 16,76 CK_PE_100M_16PORT_DP 16,76 CK_PE_100M_16PORT_DN

GPU1A 1 OF 14
1/14 PCI_EXPRESS

PEG_RXP0 / PEG_RXN0	C122641 / C122651 SCD22U10V2KX-2-GP	PEG_C_RXP0 / PEG_C_RXN0
PEG_RXP1 / PEG_RXN1	C122661 / C122671 SCD22U10V2KX-2-GP	PEG_C_RXP1 / PEG_C_RXN1
PEG_RXP2 / PEG_RXN2	C122681 / C122691 SCD22U10V2KX-2-GP	PEG_C_RXP2 / PEG_C_RXN2
PEG_RXP3 / PEG_RXN3	C122701 / C122711 SCD22U10V2KX-2-GP	PEG_C_RXP3 / PEG_C_RXN3
PEG_RXP4 / PEG_RXN4	C122721 / C122731 SCD22U10V2KX-2-GP	PEG_C_RXP4 / PEG_C_RXN4
PEG_RXP5 / PEG_RXN5	C122741 / C122751 SCD22U10V2KX-2-GP	PEG_C_RXP5 / PEG_C_RXN5
PEG_RXP6 / PEG_RXN6	C122761 / C122771 SCD22U10V2KX-2-GP	PEG_C_RXP6 / PEG_C_RXN6
PEG_RXP7 / PEG_RXN7	C122781 / C122791 SCD22U10V2KX-2-GP	PEG_C_RXP7 / PEG_C_RXN7

PEG_TXP0 / PEG_TXN0	AG6 / AG7	PEX_RX0 / PEX_RX0#
PEG_TXP1 / PEG_TXN1	AF7 / AE7	PEX_RX1 / PEX_RX1#
PEG_TXP2 / PEG_TXN2	AE9 / AF9	PEX_RX2 / PEX_RX2#
PEG_TXP3 / PEG_TXN3	AG9 / AG10	PEX_RX3 / PEX_RX3#
PEG_TXP4 / PEG_TXN4	AF10 / AE10	PEX_RX4 / PEX_RX4#
PEG_TXP5 / PEG_TXN5	AE12 / AF12	PEX_RX5 / PEX_RX5#
PEG_TXP6 / PEG_TXN6	AG12 / AG13	PEX_RX6 / PEX_RX6#
PEG_TXP7 / PEG_TXN7	AF13 / AE13	PEX_RX7 / PEX_RX7#

AB6	PEX_WAKE#
AC7	PEX_RST#
AC6	PEX_CLKREQ#
AE8 / AD8	PEX_REFCLK / PEX_REFCLK#
AC9 / AB9	PEX_TX0 / PEX_TX0#
AB10 / AC10	PEX_TX1 / PEX_TX1#
AD11 / AC11	PEX_TX2 / PEX_TX2#
AC12 / AB12	PEX_TX3 / PEX_TX3#
AB13 / AC13	PEX_TX4 / PEX_TX4#
AD14 / AC14	PEX_TX5 / PEX_TX5#
AC15 / AB15	PEX_TX6 / PEX_TX6#
AB16 / AC16	PEX_TX7 / PEX_TX7#
AD17 / AC17	PEX_TX8 / PEX_TX8#
AE15 / AF15	PEX_RX8 / PEX_RX8#
AC18 / AB18	PEX_TX9 / PEX_TX9#
AG15 / AG16	PEX_RX9 / PEX_RX9#
AB19 / AC19	PEX_TX10 / PEX_TX10#
AF16 / AE16	PEX_RX10 / PEX_RX10#
AD20 / AC20	PEX_TX11 / PEX_TX11#
AE18 / AF18	PEX_RX11 / PEX_RX11#
AC21 / AB21	PEX_TX12 / PEX_TX12#
AG18 / AG19	PEX_RX12 / PEX_RX12#
AD23 / AE23	PEX_TX13 / PEX_TX13#
AF19 / AE19	PEX_RX13 / PEX_RX13#
AF24 / AE24	PEX_TX14 / PEX_TX14#
AF21 / AF21	PEX_RX14 / PEX_RX14#
AG24 / AG25	PEX_TX15 / PEX_TX15#
AG21 / AG22	PEX_RX15 / PEX_RX15#

NC FOR GM108

NC FOR GF117/GK208/GM108

GP

N16S-GM-S-A2-GP
(G_071.0N16S.0G0U)

AA22 / AB23 / AC24 / AD25 / AE26 / AE27	PEX_IOVDD_1 / PEX_IOVDD_2 / PEX_IOVDD_3 / PEX_IOVDD_4 / PEX_IOVDD_5 / PEX_IOVDD_6
AA10 / AA12 / AA13 / AA16 / AA18 / AA19 / AA20 / AA21 / AB22 / AC23 / AD24 / AE25 / AF26 / AF27	PEX_IOVDDQ_1 / PEX_IOVDDQ_2 / PEX_IOVDDQ_3 / PEX_IOVDDQ_4 / PEX_IOVDDQ_5 / PEX_IOVDDQ_6 / PEX_IOVDDQ_7 / PEX_IOVDDQ_8 / PEX_IOVDDQ_9 / PEX_IOVDDQ_10 / PEX_IOVDDQ_11 / PEX_IOVDDQ_12 / PEX_IOVDDQ_13 / PEX_IOVDDQ_14

+V_1P05_VGA

C445 SCD1U10V2KX-1DLGP; C434 SCD1U10V2KX-1DLGP; C437 SC4D7U6D3V3KX-DLGP; C412 SC10U6D3V3MX-DL-GP; C413 SC10U6D3V3MX-DL-GP; C417 SC10U6D3V5MX-2DLGP; C420 SC10U6D3V5MX-2DLGP

+V_1P05_VGA

C442 SCD1U10V2KX-1DLGP; C441 SCD1U10V2KX-1DLGP; C433 SC4D7U6D3V3KX-DLGP; C12376 SC10U6D3V3MX-DL-GP; C421 SC10U6D3V5MX-2DLGP; C429 SC10U6D3V5MX-2DLGP; C426 SC10U6D3V5MX-2DLGP

NC FOR GF119

PEX_PLL_HVDD_1 AA8
PEX_PLL_HVDD_2 AA9
PEX_SVDD_3V3 AB8

+V_3P3_VGA

C440 SCD1U16V2KX-3DLGP; C443 SC4D7U6D3V3KX-DLGP; C438 SC4D7U6D3V3KX-DLGP

VDD_SENSE F2 PWR_VGA_CORE_SENCE+ → PWR_VGA_CORE_SENCE+ 88

GND_SENSE F1 PWR_VGA_CORE_SENCE- → PWR_VGA_CORE_SENCE- 88

PEX_TSTCLK_OUT AF22 PEX_TSTCLK_OUT
PEX_TSTCLK_OUT# AE22 PEX_TSTCLK_OUT# — R193 200R2F-L-GP

PEX_PLLVDD_1 AA14
PEX_PLLVDD_2 AA15
PEX_PLLVDD_GPU

+V_1P05_VGA

L9524 (G_68.00217.161) MCB1608S121IBP-GP

C444 SC1U16V2KX-3DLGP; C435 SCD1U25V2KX-1DLGP; C427 SC4D7U25V5KX-DLGP; C430 SC4D7U25V5KX-DLGP; C428 SC1U25V3KX-1DLGP

100MHZ 120mohm

TESTMODE AD9 GPU_TESTMODE — R192 10KR2J-3-GP

PEX_TERMP AF25 PEX_TERMP — R79978 2K49R2F-GP

SB042 10/17 Allen modify

08/14 Allen add for iRMT

SC005 11/11 Allen modify

R80059 0R2J-2-GP +V_3P3_VGA

24 SIO_GPU_RST
24,68,76 PLTRST_SL_N

U9521 NL17SZ08DFT2G-GP

AMD_RST#_L

R80060 100KR2F-L1-GP

SB0055 10/22 Allen modify

<Variant Name>

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Title 076_GPU(1/5) PEG

Size C | Document Number COLORADO MLK SKYLAKE-S | Rev -2

Date: | Sheet 76 of 107

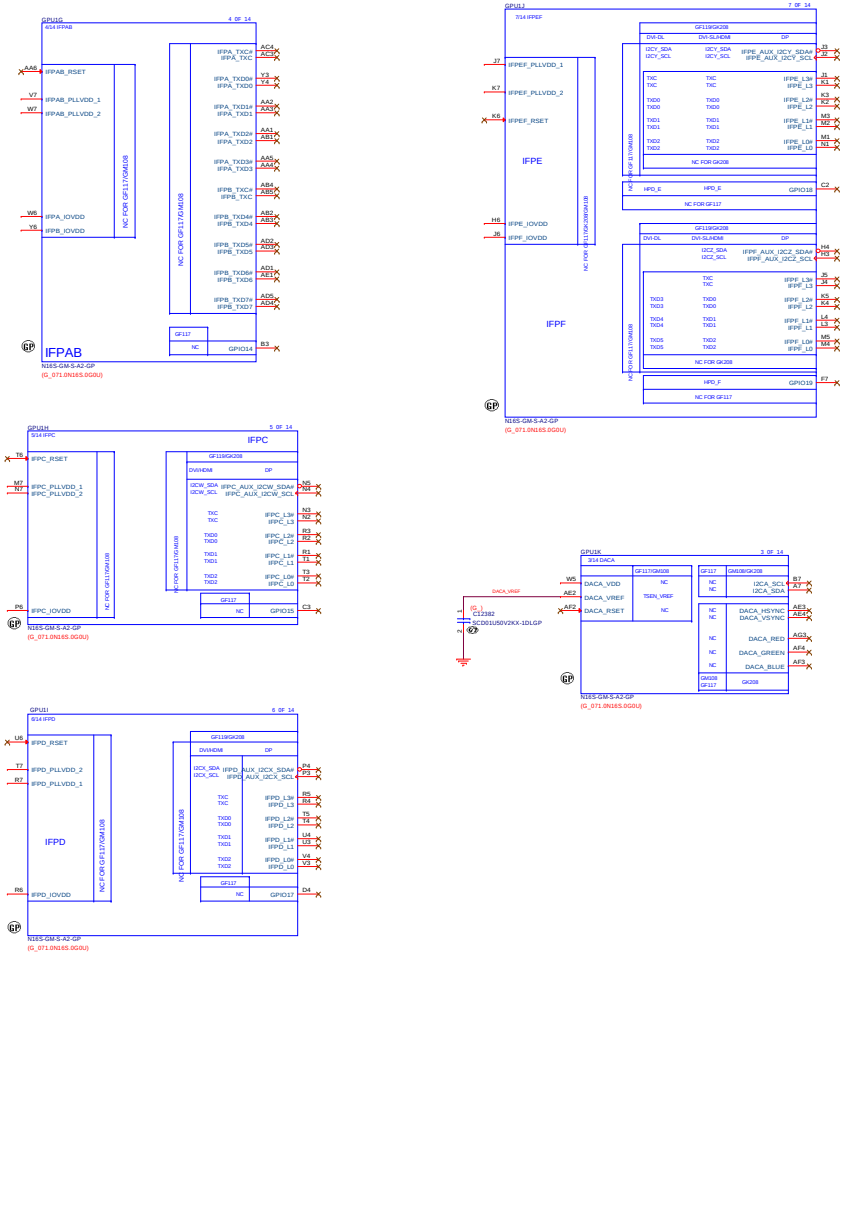
1U Under GPU

4.7U NEAR TO GPU

10U mid TO GPU

Michael 2011/12/12

Add two 1uF Caps according to the NV Comment



Title: 077_GPU(2/5)DIGITALOUT

Size	Document Number	Rev
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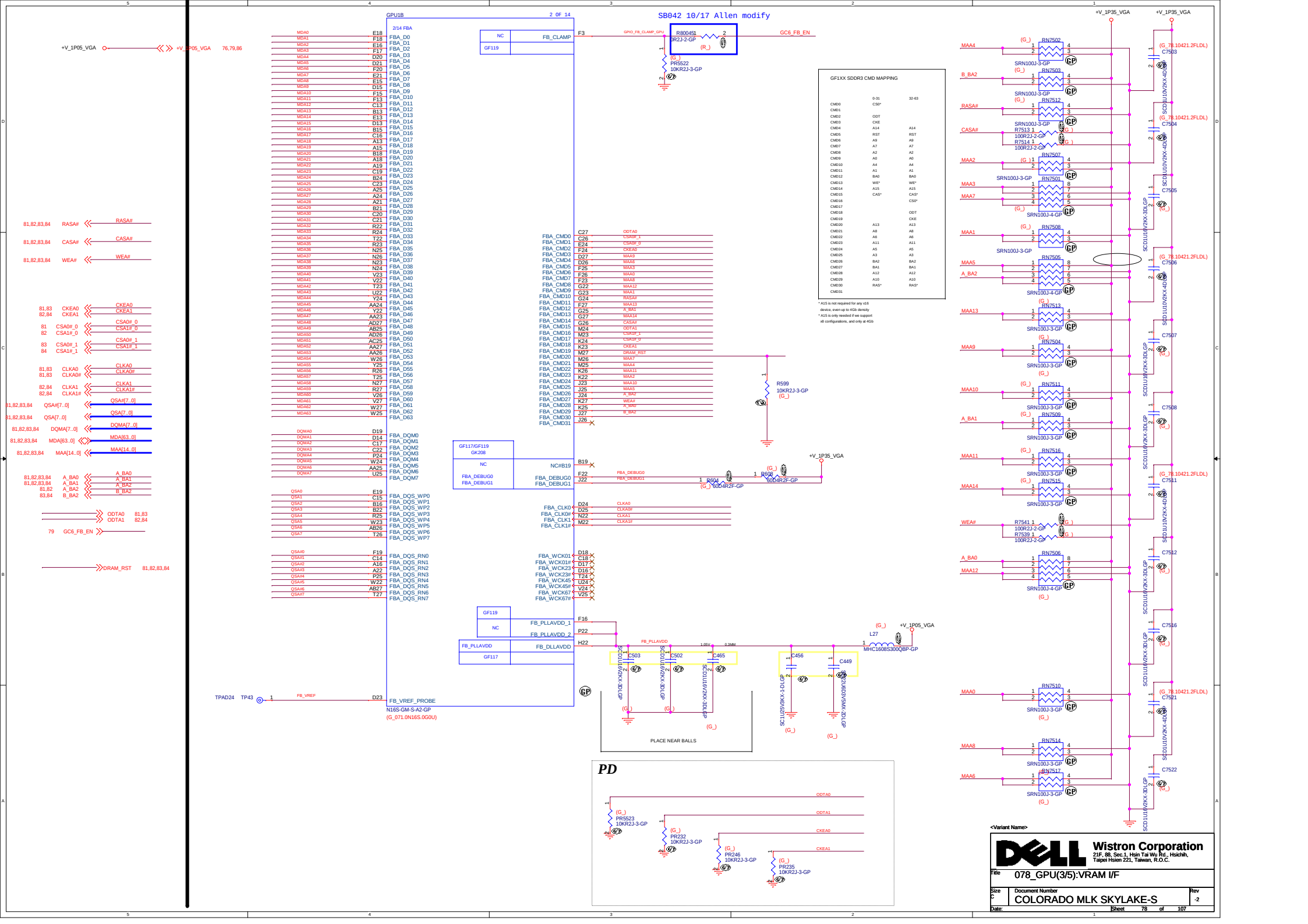
Date: Sheet 77 of 107


GPU1B
2 OF 14
SB042 10/17 Allen modify
2/14 FBA
FBA_D0
FBA_D1
FBA_D2
FBA_D3
FBA_D4
FBA_D5
FBA_D6
FBA_D7
FBA_D8
FBA_D9
FBA_D10
FBA_D11
FBA_D12
FBA_D13
FBA_D14
FBA_D15
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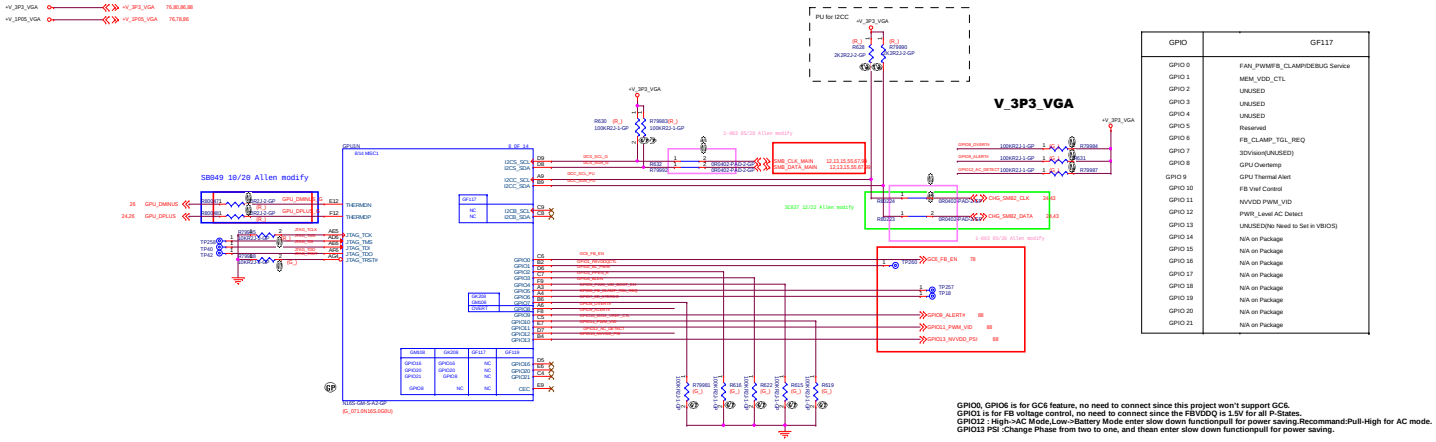
FBA_D56
FBA_D57
FBA_D58
FBA_D59
FBA_D60
FBA_D61
FBA_D62
FBA_D63
FBA_DQM0
FBA_DQM1
FBA_DQM2
FBA_DQM3
FBA_DQM4
FBA_DQM5
FBA_DQM6
FBA_DQM7
FBA_DQS_WP0
FBA_DQS_WP1
FBA_DQS_WP2
FBA_DQS_WP3
FBA_DQS_WP4
FBA_DQS_WP5
FBA_DQS_WP6
FBA_DQS_WP7
FBA_DQS_RN0
FBA_DQS_RN1
FBA_DQS_RN2
FBA_DQS_RN3
FBA_DQS_RN4
FBA_DQS_RN5
FBA_DQS_RN6
FBA_DQS_RN7
FB_VREF_PROBE
N16S-GM-S-A2-GP
(G_071.0N16S.0G0U)
FB_CLAMP
GPIO_FB_CLAMP_GPU
R800451
10KR2J-2-GP
GC6_FB_EN
PR5522
10KR2J-3-GP
GF117/GF119
GK208
NC
NC#B19
FBA_DEBUG0
FBA_DEBUG1
R604
60D4R2F-GP
R608
60D4R2F-GP
+V_1P35_VGA
R599
10KR2J-3-GP
FBA_CLK0
FBA_CLK0#
FBA_CLK1
FBA_CLK1#
FBA_WCK01
FBA_WCK01#
FBA_WCK23
FBA_WCK23#
FBA_WCK45
FBA_WCK45#
FBA_WCK67
FBA_WCK67#
FB_PLLAVDD_1
FB_PLLAVDD_2
FB_PLLAVDD
FB_DLLAVDD
GF117
GF119
C503
C502
C465
C456
C449
L27
MHC1608S300QBP-GP
+V_1P05_VGA
PLACE NEAR BALLS
PD
PR5523
10KR2J-3-GP
PR232
10KR2J-3-GP
PR246
10KR2J-3-GP
PR235
10KR2J-3-GP
ODTA0
ODTA1
CKEA0
CKEA1
GF1XX SDDR3 CMD MAPPING
* A15 is not required for any x16 device, even up to 4Gb density
* A15 is only needed if we support x8 configurations, and only at 4Gb
RN7502
RN7503
RN7512
RN7507
RN7501
RN7508
RN7505
RN7513
RN7504
RN7511
RN7509
RN7516
RN7515
RN7506
RN7510
RN7514
RN7517
SRN100J-3-GP
SRN100J-4-GP
R7513
R7514
R7541
R7539
100R2J-2-GP
C7503
C7504
C7505
C7506
C7507
C7508
C7511
C7512
C7516
C7521
C7522
SCD1U16V2KX-4DLGP
SCD1U16V2KX-3DLGP
(G_78.10421.2FLDL)
MAA4
B_BA2
RASA#
CASA#
MAA2
MAA3
MAA7
MAA1
MAA5
A_BA2
MAA13
MAA9
MAA10
A_BA1
MAA11
MAA14
WEA#
A_BA0
MAA12
MAA0
MAA8
MAA6
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
078_GPU(3/5):VRAM I/F
Size
C
Document Number
COLORADO MLK SKYLAKE-S
Rev
-2
Date:
Sheet 78 of 107



GPIO	GF117
GPIO 0	FAN_PWMFB_CLAMPDEBUG Service
GPIO 1	MEM_VDD_CTL
GPIO 2	UNUSED
GPIO 3	UNUSED
GPIO 4	UNUSED
GPIO 5	Reserved
GPIO 6	FB_CLAMP_TGL_REQ
GPIO 7	3DVision(UNUSED)
GPIO 8	GPU Overtemp
GPIO 9	GPU Thermal Alert
GPIO 10	FB Vref Control
GPIO 11	NVVDD PWM_VID
GPIO 12	PWR_Level AC Detect
GPIO 13	UNUSED(No Need to Set in VBIOS)
GPIO 14	N/A on Package
GPIO 15	N/A on Package
GPIO 16	N/A on Package
GPIO 17	N/A on Package
GPIO 18	N/A on Package
GPIO 19	N/A on Package
GPIO 20	N/A on Package
GPIO 21	N/A on Package

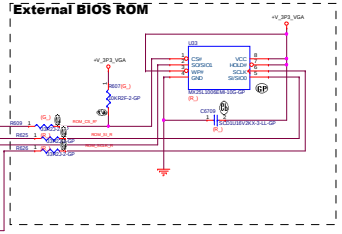
GPIO0, GPIO6 is for GC6 feature, no need to connect since this project won't support GC6.
GPIO1 is for FB voltage control, no need to connect since the FBVDDQ is 1.5V for all P-States.
GPIO12 : High->AC Mode,Low->Battery Mode enter slow down functionpull for power saving.Recommand:Pull-High for AC mode.
GPIO13 PSI :Change Phase from two to one, and thean enter slow down functionpull for power saving.

Table 12-1. GB2-64 GPIO Description

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	Reserved			
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	Pull-up/pull-down to set the FBVDD/Q boot voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 kΩ pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	100 kΩ pull-down
GPIO4	LCD_BLEH	O	Panel Backlight Enable	100 kΩ pull-down
GPIO5	Reserved			
GPIO6	Reserved			
GPIO7	3DVision	O	3D Vision L/R signal	100 kΩ pull-down
GPIO8	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up
GPIO9	THERM_ALERT	I/O	Thermal Alert, Open Drain	10 kΩ pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL		AC power detect or power supply overdraw input	100 kΩ pull-up
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	Reserved			
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IPFB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	Reserved			

STRAP

External BIOS ROM



STRAP PIN MODE TABLE	
PIN NAME	BINARY BRINGUP
STRAP0	3GIO_PADCFG_LUT_ADR0
STRAP1	3GIO_PADCFG_LUT_ADR1
STRAP2	3GIO_PADCFG_LUT_ADR2
STRAP3	3GIO_PADCFG_LUT_ADR3
STRAP4	PCI_MAX_SPEED
ROM_SCLK	SMB_ALT_ADDR
ROM_SI	SUB_VENDOR
ROM_SO	VGA_DEVICE

NOTE 2: See table 1 for the correct value/location of the strap resistor for the desired modes

NOTE 3: Bring-up SKU(s) have jumper configurable subvendor and DEVID_4 settings see the ROM_SCLK STRAP

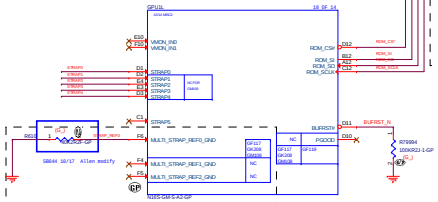


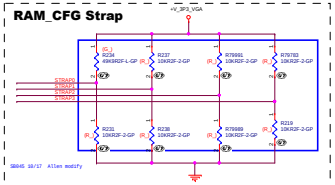
Table 119. Device Specific Strap Mode Selection

	N14M-GE/-GL	Other N14x GPUs
Multi_Strap_Ref2_GND (Only on GB2-64 package)	No Connect	N/A
Multi_Strap_Ref1_GND (Only on GB2-64 package)	No Connect	N/A
Multi_Strap_Ref0_GND	No Connect	40.2k 1% to GND
Strap Mode Selected	Bidirect	Multi-Level

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

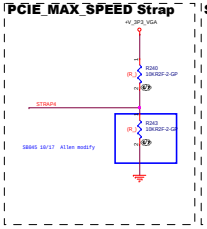
Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

RAM_CFG Strap

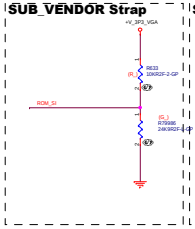


RMA_CFG [3:0]
Samsung - K4W2G1646E-BC11 (1000MHz) [0101]
Micron - MT41J128M16JT-093G:K (1000MHz) [0001]

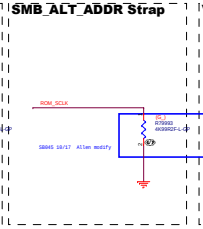
PCIE_MAX_SPEED Strap



SUB_VENDOR Strap



SMB_ALT_ADDR Strap



VGA_DEVICE Strap

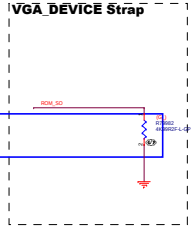


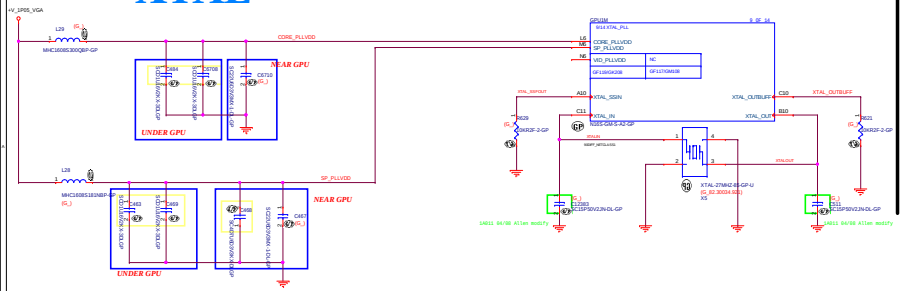
Table 4. H16S-GM/-GT/-LP DDR3L Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
DDR3L	1.35V/ 1.35V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC2G63FFR-11C	F-die	0x9	900	H/A	Production ready
				Micron	MT41J128M16JT-093G:K	K-die	0xA	900	1322	Production ready
				Samsung	K4W2G1646Q-BC1A	Q-die	0xB	900	H/A	Production ready
		256Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x3	900	H/A	Production ready
				Micron	MT41J256M16HA-093G:E	E-die	0x4	900	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	H/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0x1	900	H/A	Post production ready
				Hynix	H5TC4G63CFR-H0C	C-die	0x2	900	H/A	Post production ready
			Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x3	900	H/A	Production ready
				Micron	MT41J256M16HA-093G:E	E-die	0x4	900	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	H/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0x7	900	H/A	Post production ready
				Hynix	H5TC4G63CFR-H0C	C-die	0xE	900	H/A	Post production ready

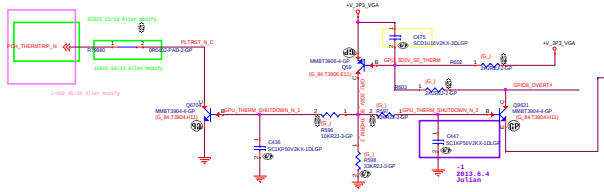
Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

XTAL

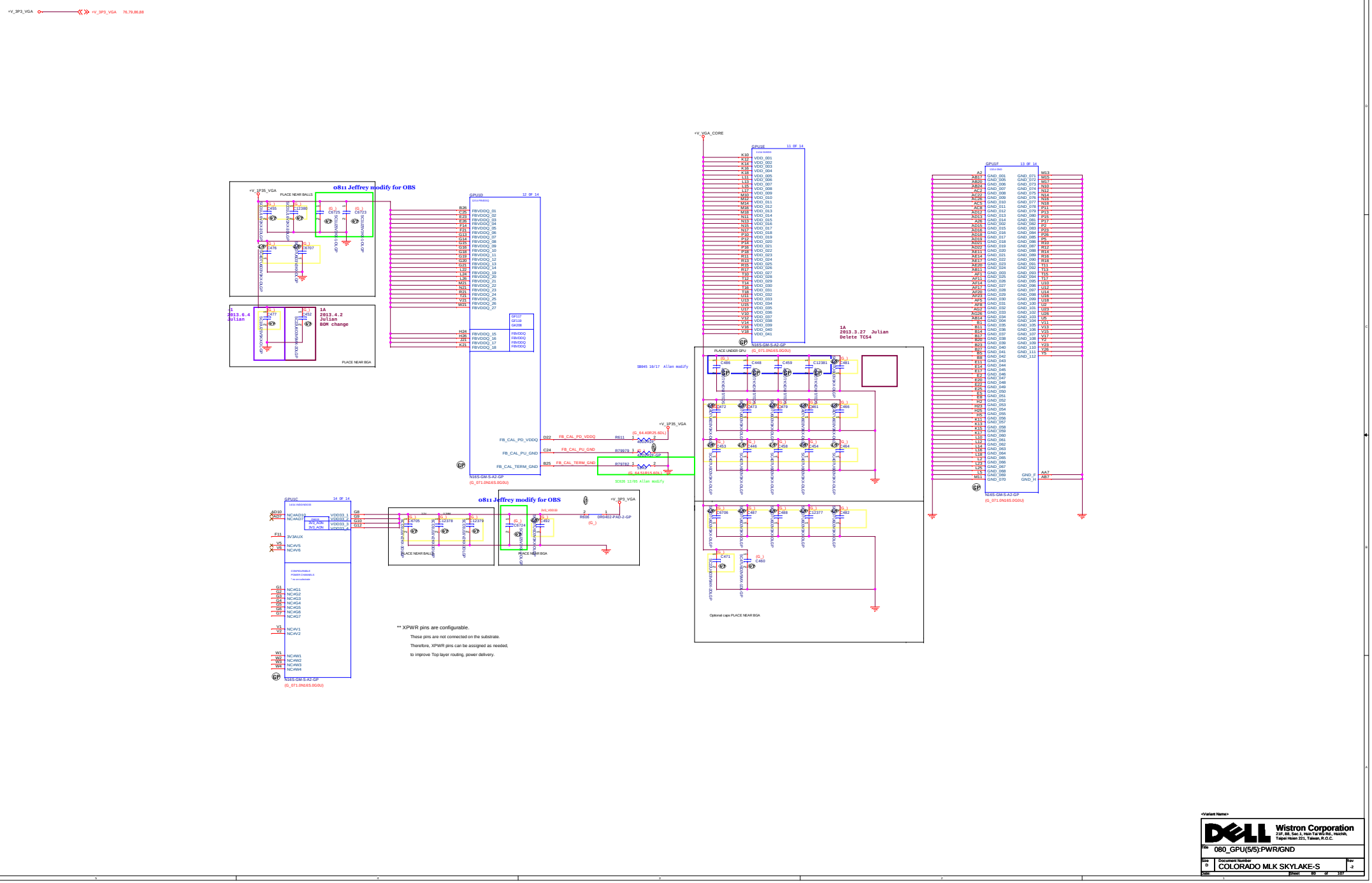


THERMAL PROTECTION



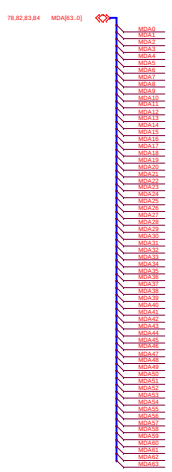
079_GPU(4/5):GPIO/STRAP

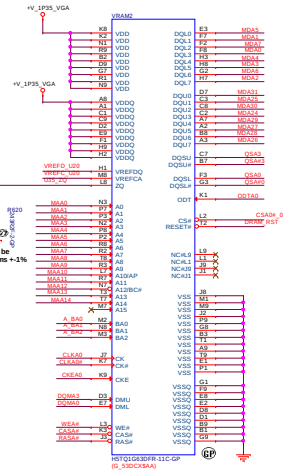
COLORADO MLK SKYLAKE-S

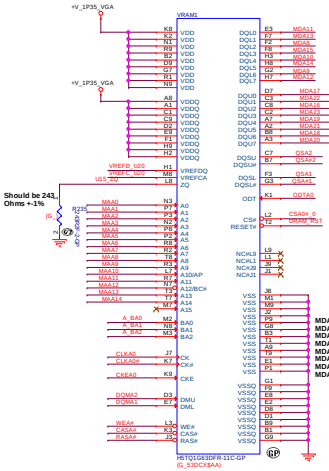

+V_3P3_VGA
+V_3P3_VGA 76,79,86,88
+V_VGA_CORE
GPU1E 11 OF 14
GPU1F 13 OF 14
GPU1D 12 OF 14
GPU1C 14 OF 14
+V_1P35_VGA
PLACE NEAR BALLS
PLACE NEAR BGA
PLACE UNDER GPU
o811 Jeffrey modify for OBS
1A
2013.6.4
Julian
1A
2013.4.2
Julian
BOM change
1A
2013.3.27 Julian
Delete TCS4
SB045 10/17 Allen modify
SC826 12/05 Allen modify
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
N16S-GM-S-A2-GP
(G_071.0N16S.0GGU)
Optional caps PLACE NEAR BGA
** XPWR pins are configurable.
These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
080_GPU(5/5):PWR/GND
Size
D
Document Number
COLORADO MLK SKYLAKE-S
Rev
-2
Date:
Sheet 80 of 107

CHANNEL A:1GB DDR3

72.42164.G0U	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Samsung- K4W2G1646E-BC11
0B41791AA	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Hynix- H5TQ2G63DFR-11C







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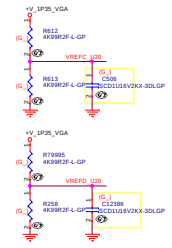
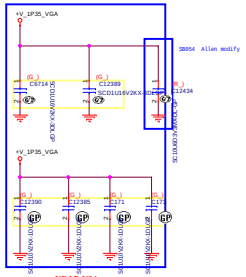
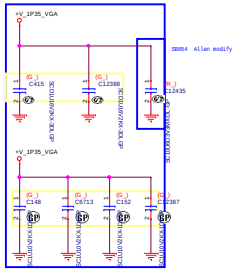
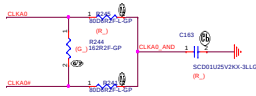






FBCLK Termination place on VRAM side



<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

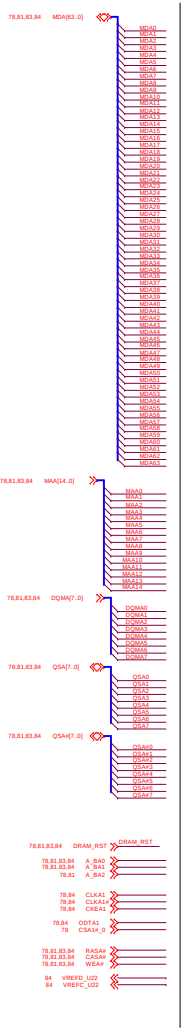
Title: 081_VRAM 1,2 (1/4)

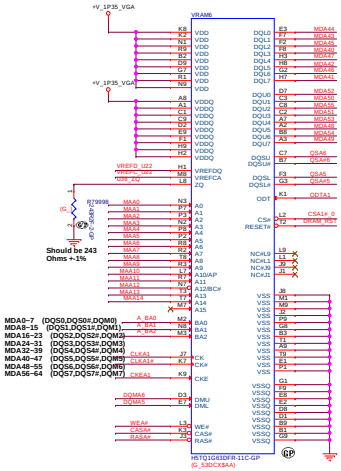
Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

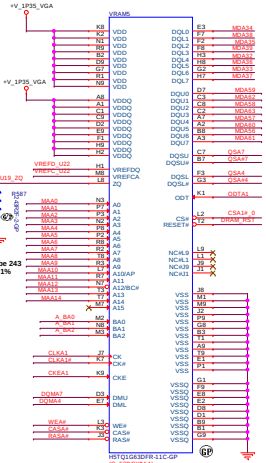
Date: | Sheet 81 of 107

CHANNEL A:1GB DDR3

72.42164.G0U	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Samsung- K4W2G1646E-BC11
0B41791AA	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Hynix- H5TQ2G63DFR-11C







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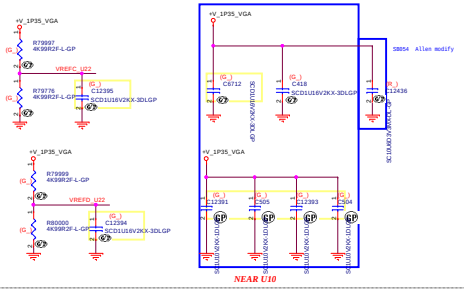
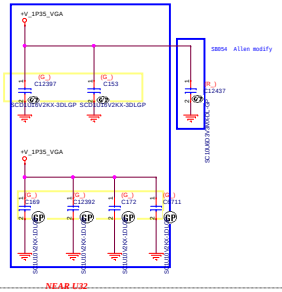
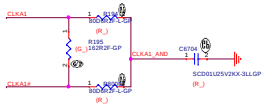




FBCLK Termination place on VRAM side



<Variant Name>
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

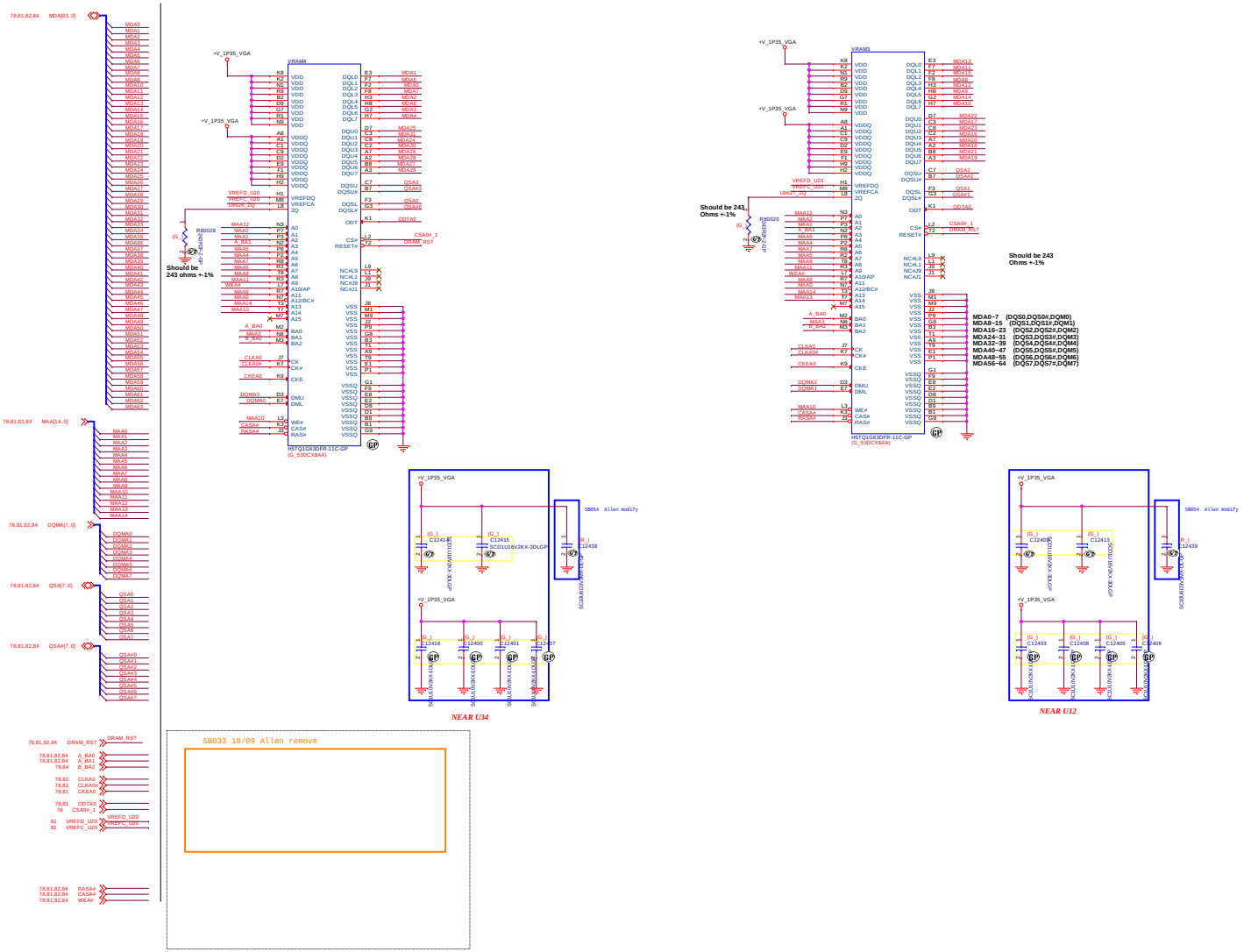
Title: 082_VRAM 3,4 (2/4)

Size	Document Number	Rev
D	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 82 of 107

CHANNEL A:1GB DDR3

72.42164.G0U	2Gb	DDR3	128M*16 900MHz SDRAM FBGA96P	Samsung- K4W2G1646E-BC11
0B41791AA	2Gb	DDR3	128M*16 900MHz SDRAM FBGA96P	Hynix- H5TQ2G63DFR-11C



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

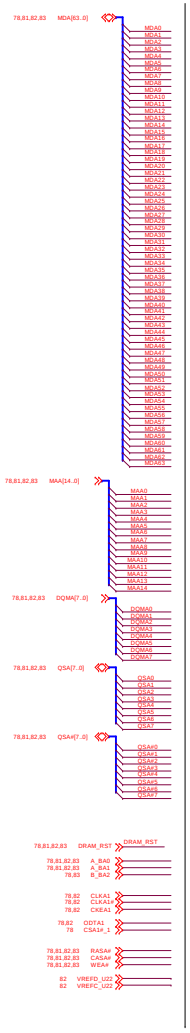
Title: 083_VRAM 5,6 (2/4)

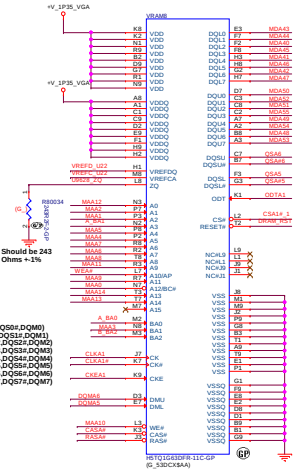
Size	Document Number	Rev
D	COLORADO MLK SKYLAKE-S	-2

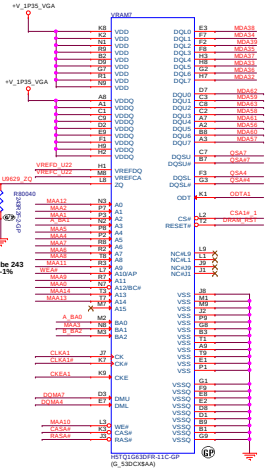
Date: Sheet 83 of 107

CHANNEL A:1GB DDR3

72.42164.G0U	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Samsung- K4W2G1646E-BC11
0B41791AA	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Hynix- H5TQ2G63DFR-11C







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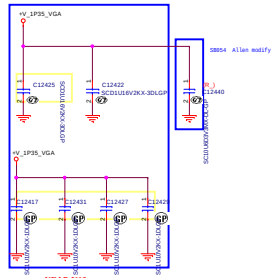
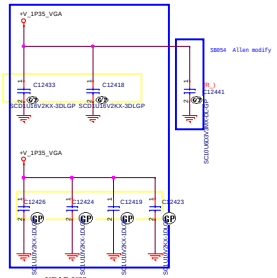




FBCLK Termination place on VRAM side

SB033 10/09 Allen remove

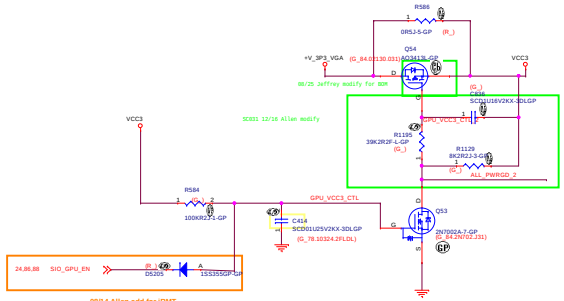
<Variant Name>

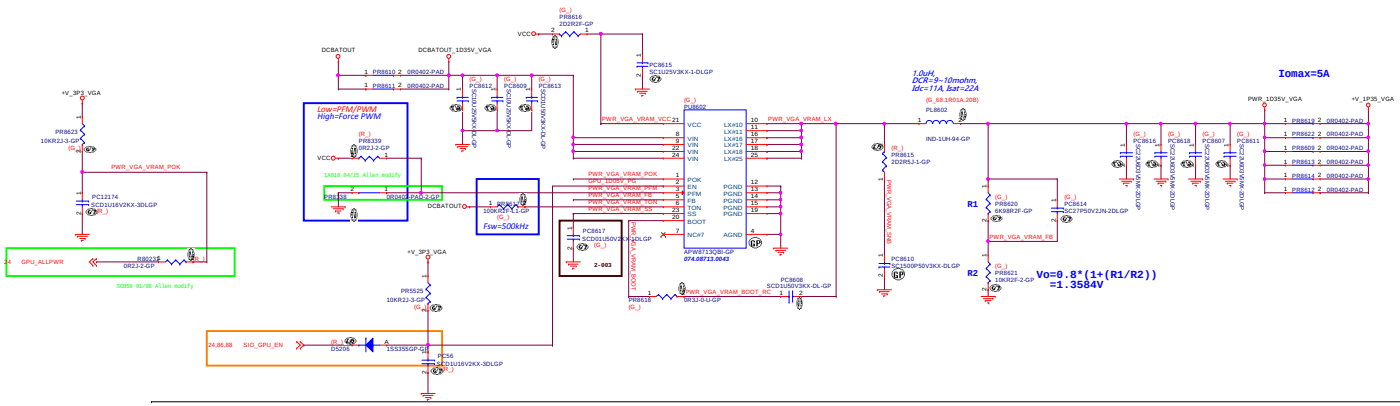
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Size: Custom	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 85 of 107	

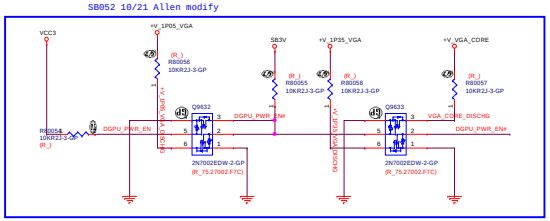
+V_3P3_VGA
+V_1P05_VGA
VCC3
VCC
DCBATOUT
V_SM
SB3V

3D3V_S0 to 3D3V_DELAY Transfer

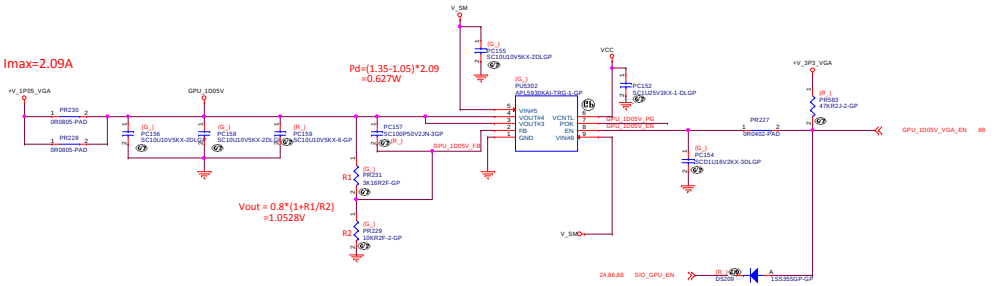




SB052 10/21 Allen modify



GPU 1.05V



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: 086_PWR_GPU_LDO

Size	Document Number	Rev
D	COLORADO MLK SKYLAKE-S	-2

Date: | Sheet 86 of 107

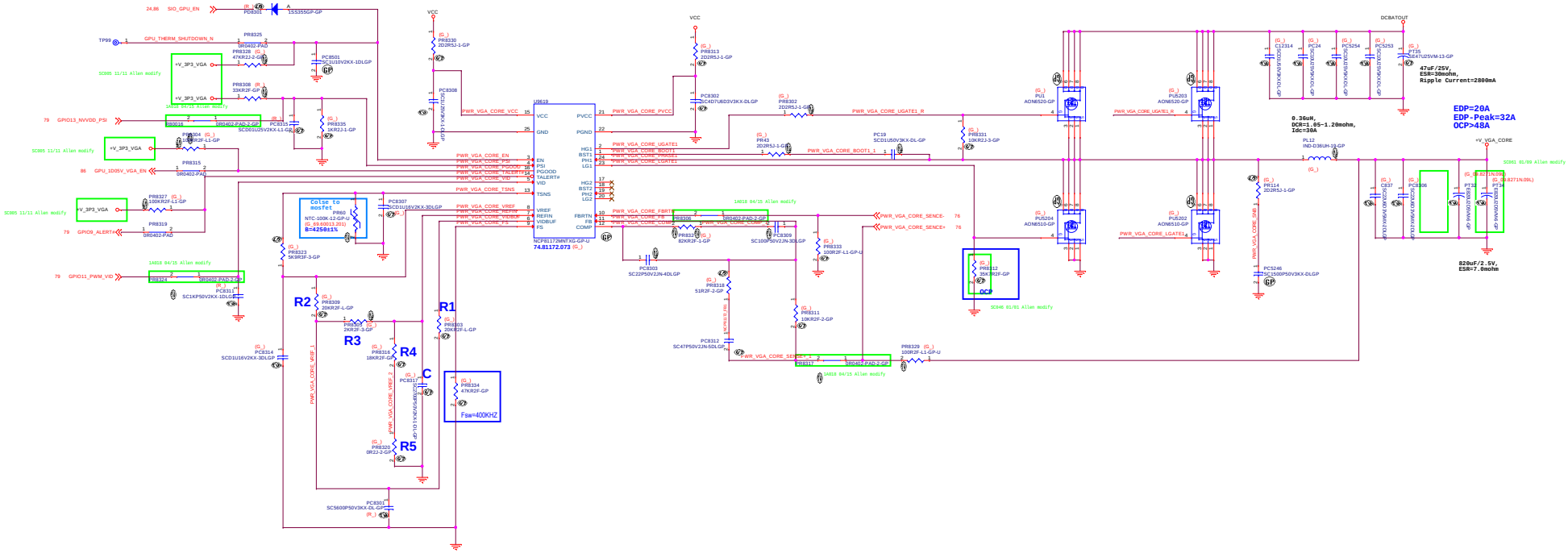
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
Custom	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 87 of 107



		Config A	Config B
R1 (1%)	KΩ	39	20
R2 (1%)	KΩ	39	20
R3 (1%)	KΩ	1.5	2
R4 (1%)	KΩ	30	18
R5 (1%)	KΩ	1.5	0
C	nF	1.5	2.7

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 088_PWR_GPU_CORE

Size: D | Document Number: COLORADO MLK SKYLAKE-S | Rev: -2

Date: | Sheet 88 of 107

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
D	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 89 of 107

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title		
Size: A3	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 90 of 107	

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A3	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 91 of 107

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Size	Document Number	Rev
C	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 92 of 107

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	-2
Date:	Sheet 93 of 107	

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Size: A4	Document Number: COLORADO MLK SKYLAKE-S	Rev: -2
Date:	Sheet 94 of 107	

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 95 of 107

(Blanking)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 96 of 107

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 97 of 107

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 98 of 107

V1P0_PCH_S5 — V1P0_PCH_S5 7,15,21,51
V_3P3_A — V_3P3_A 15,21,24,25,28,29,42,43,49,84
V_CPU_IO — V_CPU_IO 4,5,7,8,9,48

VCC3 — VCC3 12,13,15,16,17,18,20,21,24,25,26,27,28,31,33,38,41,42,44,47,48,50,53,55,56,58,59,61,62,64,67,68,86
V_CPU_ST_PLL — V_CPU_ST_PLL 4,7,44
3P3V_SPI — 3P3V_SPI 20,21,25

XDP for CPU

4 H_TDO
4 H_TDI
4 H_TMS
4,15 H_TCK
4 H_TRST_N
4 H_PREQ_N
4 H_PRDY_N

4,15 H_PWRGD
4,40 VCCST_PWRGD
15,20,25 SPI_MOSI
4 SKL_PCUDEBUG_0
4 SKL_PCUDEBUG_1
4 SKL_PCUDEBUG_2
4 SKL_PCUDEBUG_3
4 SKL_PCUDEBUG_4
4 SKL_PCUDEBUG_5
4 SKL_PCUDEBUG_6
4 SKL_PCUDEBUG_7
4 SKL_PCUDEBUG_8
4 SKL_PCUDEBUG_9
4 SKL_PCUDEBUG_10
4 SKL_PCUDEBUG_11
4 SKL_PCUDEBUG_12
4 SKL_PCUDEBUG_13
4 SKL_PCUDEBUG_14
4 SKL_PCUDEBUG_15
4 XDP_PCUDERBUG_3
4 SKL_XDP_MBP_0
4 SKL_XDP_MBP_1

4 SKL_PCUSTB_0_DN
4 SKL_PCUSTB_0_DP
4 SKL_PCUSTB_1_DN
4 SKL_PCUSTB_1_DP
12,13,15,55,67,79 SMB_DATA_MAIN
12,13,15,55,67,79 SMB_CLK_MAIN
16 CK_100M_CPU_XDP_DN
16 CK_100M_CPU_XDP_DP
4,17 PLTRST_CPU_N
15,20,25 SPI_IO2

APS CONNECTOR

15,24,35,40,42,48,50,53,55 SLP_S3_N
7,15,24,35,42,55 SLP_S4_N
15 PCH_SLP_A_N
15,24,64,99 PWRBTN_N

XDP for PCH

15 PCH_JTAG_TCK
15,24,64,99 PWRBTN_N
15,24 RSMRST_N
15,24 PWRGD_3V
15 FP_RST_N
15 ITP_PMODE
22 PCH_XDP_PRDY_R_N
22 PCH_XDP_PREQ_R_N

1A015 04/14 Allen modify
PCH_XDP_PREQ_R_N — R1773 — 0R0402-PAD-2-GP — H_PREQ_N
PCH_XDP_PRDY_R_N — R1774 — 0R0402-PAD-2-GP — H_PRDY_N
3P3V_SPI — R79874 — 2K2R2J-2-GP — SPI_MOSI (08/06 Allen modify)
PWRGD_3V — R1776 — 1KR2F-3-GP — XDP_VR_READY
R1774 — 0R0402-PAD-2-GP
C12241 — SCD1U16V2KX-3DLGP
06/25 Need to check sequence

RSMRST_N — R1778 — 1KR2F-3-GP
H_PWRGD — R1775 — 1KR2F-3-GP — XDP_PWRGD
VCCST_PWRGD — R1777 — 1KR2F-3-GP
1A016 04/14 Allen modify
V_CPU_ST_PLL
H_TDO — R79769 — 51R2F-2-GP
V1P0_PCH_S5 — R117761 — 150R2J-2-GP
PLTRST_CPU_N — R117713 — 1KR2J-1-GP
ITP_PMODE — R1770 — 0R0402-PAD-2-GP — H_RSTOUT_XDP_N
VCC3 — R178623 — 1KR2F-3-GP — FP_RST_N
C12242 — SCD1U16V2KX-3DLGP (X_)
V_3P3_A — R179231 — 1KR2F-3-GP
PWRBTN_N — R1792 — 0R0402-PAD-2-GP — XDP_PLTRST_N
C12243 — SCD1U16V2KX-3DLGP (R_)
V_CPU_IO — R176921 — 150R2F-1-GP
SKL_PCUDEBUG_0 — R176623 — 1KR2F-3-GP — XDP_PWR_DEBUG
PCH_JTAG_TCK — R1764 — 0R0402-PAD-2-GP — PRIM_XDP_JTAG_TCK_R
SPI_IO2 — R1812 — 0R0402-PAD-2-GP — XDP_PRDY
06/25 Allen modify

XDP for CPU

SB025 10/06 Allen modify
XDPC1 — MK1
TP135 TPAD28 — R178211 — 0R2J-2-GP — XDP_PCUDERBUG_3
H_PREQ_N
H_PRDY_N
TP136 TPAD28
TP137 TPAD28
SKL_PCUDEBUG_3

SKL_PCUDEBUG_0
SKL_PCUDEBUG_1
SKL_PCUDEBUG_2
SKL_XDP_MBP_0
SKL_XDP_MBP_1
SKL_PCUDEBUG_4
SKL_PCUDEBUG_5
SKL_PCUDEBUG_6
SKL_PCUDEBUG_7
XDP_PWRGD
XDP_PLTRST_N
XDP_PWR_DEBUG
XDP_VR_READY
SMB_DATA_MAIN
SMB_CLK_MAIN
PRIM_XDP_JTAG_TCK_R
H_TCK

SKL_PCUSTB_0_DP
SKL_PCUSTB_0_DN
SKL_PCUDEBUG_8
SKL_PCUDEBUG_9
SKL_PCUDEBUG_10
SKL_PCUDEBUG_11
V1P0_CPU_XDP_S5
SKL_PCUSTB_1_DP
SKL_PCUSTB_1_DN
SKL_PCUDEBUG_12
SKL_PCUDEBUG_13
SKL_PCUDEBUG_14
SKL_PCUDEBUG_15
CK_100M_CPU_XDP_DP
CK_100M_CPU_XDP_DN
H_RSTOUT_XDP_N
FP_RST_N
H_TDO
H_TRST_N
H_TDI
H_TMS
XDP_PRDY
SM_DMC_CONN_GP1 (X_)
MH2

V1P0_CPU_XDP_S5 — R17148 — 0R0603-PAD — V1P0_PCH_S5
R17149 — 0R0603-PAD

06/25 Allen modify
R1780 — 0R2J-2-GP (R_)
06/24 Allen modify
H_TRST_N — R1789 — 51R2J-2-GP (R_)
1A016 04/14 Allen modify

APS CONNECTOR

08/27 Allen modify for layout space

SLP_S4_N — R1784 — 0R0402-PAD-2-GP — SLP_S4_N_CN — TP221 TPAD28
PCH_SLP_A_N — R1786 — 0R0402-PAD-2-GP — SLP_A#_CN — TP222 TPAD28
SLP_S3_N — R1785 — 0R0402-PAD-2-GP — SLP_S3_N_CN — TP223 TPAD28
PWRBTN_N — R1787 — 0R0402-PAD-2-GP — PWRBTN_N_CN — TP224 TPAD28
FP_RST_N — R1783 — 0R0402-PAD-2-GP — FP_RST_PCH_N_CN — TP225 TPAD28

All parts can be placed at back side

XDP for PCH

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Title: 099_XDP
Size: D
Document Number: COLORADO MLK SKYLAKE-S
Rev: -2
Date:
Sheet 99 of 107

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Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 100 of 107

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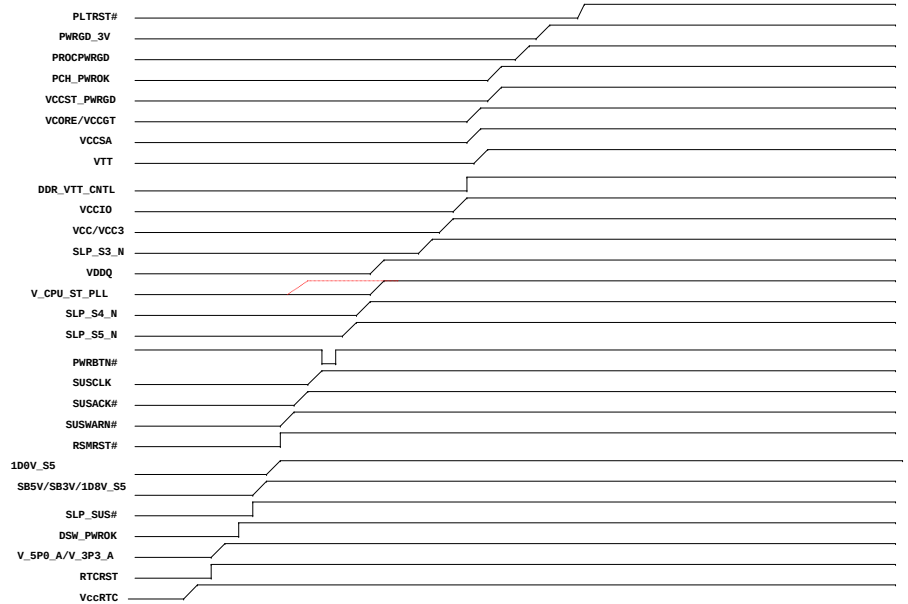
Title

Size	Document Number	Rev
A4	COLORADO MLK SKYLAKE-S	-2
Date:	Sheet 101 of 107	

POWER ON SEQUENCE



3.3V-->NVVDD&PEX_VDD(+V_VGA_CORE&+V_1P05_VGA)-->FBVDD/Q(+V_1P5_VGA)

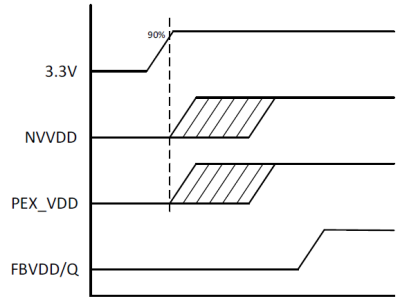


Figure 3-7. Example of Power-Up Sequencing Order

CRB	+V3_BAT (0) → RTCRST# (1) → AC_IN (2) → +V5DSW (3) → +V3p3DSW, BACKFEED_CUT_N (4) → DPWROK, SMC_RST# (5)
	BAT (0) → RTCRST# (1) → AC_IN (2) → 19V (3) → V_5P0_A, V_3P3_A (4) → DPWROK (5)
CRB	SLP_SUS# (6) → +V5DUAL, +V1P8A, +V5A, +V3p3A, BACKFEED_CUT_N, LATCHED_BACKFEED_CUT (7) → +VCCST_VCCSFR, +V1P0A (8) → RSMRST#_PWRGD (9) → RSMRST# (10)
	SLP_SUS# (6) → SB5V, SB3V, V_1P8_A (7) → V_CPU_ST_PLL, +V1P0A (8) → RSMRST# (9) → SUSWARN# (10) → SUSACK# (11)
CRB	SUSWARN# (11) → SUSACK# (12) → PWRBTN (13) → SLP_S5, SLP_S4, SLP_S3 (15) → +VCCST_VCCSFR, +VCCST_VCCPLL, +VPP(DDR4) (16)
	PWRBTN (12) → SLP_S5, SLP_S4, SLP_S3 (13) → V_SM, +VCCST_VCCSFR (14) → VCC, VCC3 (15) → VCCIO_EN (16)
CRB	FPGA_VDDQ_EN (17) → PS_ON_N, +VDDQ, +VDDQ_VTT (18) → +V12S, +V5S, +V3p3S, +V12S_CPU (19) → VCCIO_EN, PWRGD_VCCPLL_OC, VDDQ_PWRGD_ISOLATE (20) → +VCCIO (21)
	V_CPU_IO (17) → DDR_VTT_CNTL (18) → +VDDQ_VTT (19) → VCCIO_PWRGD (20) → V_CPU_GT/V_CPU_CORE, V_CPU_SA (21)
CRB	VCCIO_PWRGD (22) → +VCCSA (23) → VR_READY (24) → ALL_SYS_PWRGD (25)
	VR_READY (22) → ALL_SYS_PWRGD (23) → PWRGD_3V (24)
CRB	SYSPWROK (26) → PLTRST#, PLTRST_CPU# (27)
	PLTRST#, PLTRST_CPU# (25)

Noter:
If +VCCST_VCCSFR is only in S0, power can be controlled by slp _s4.

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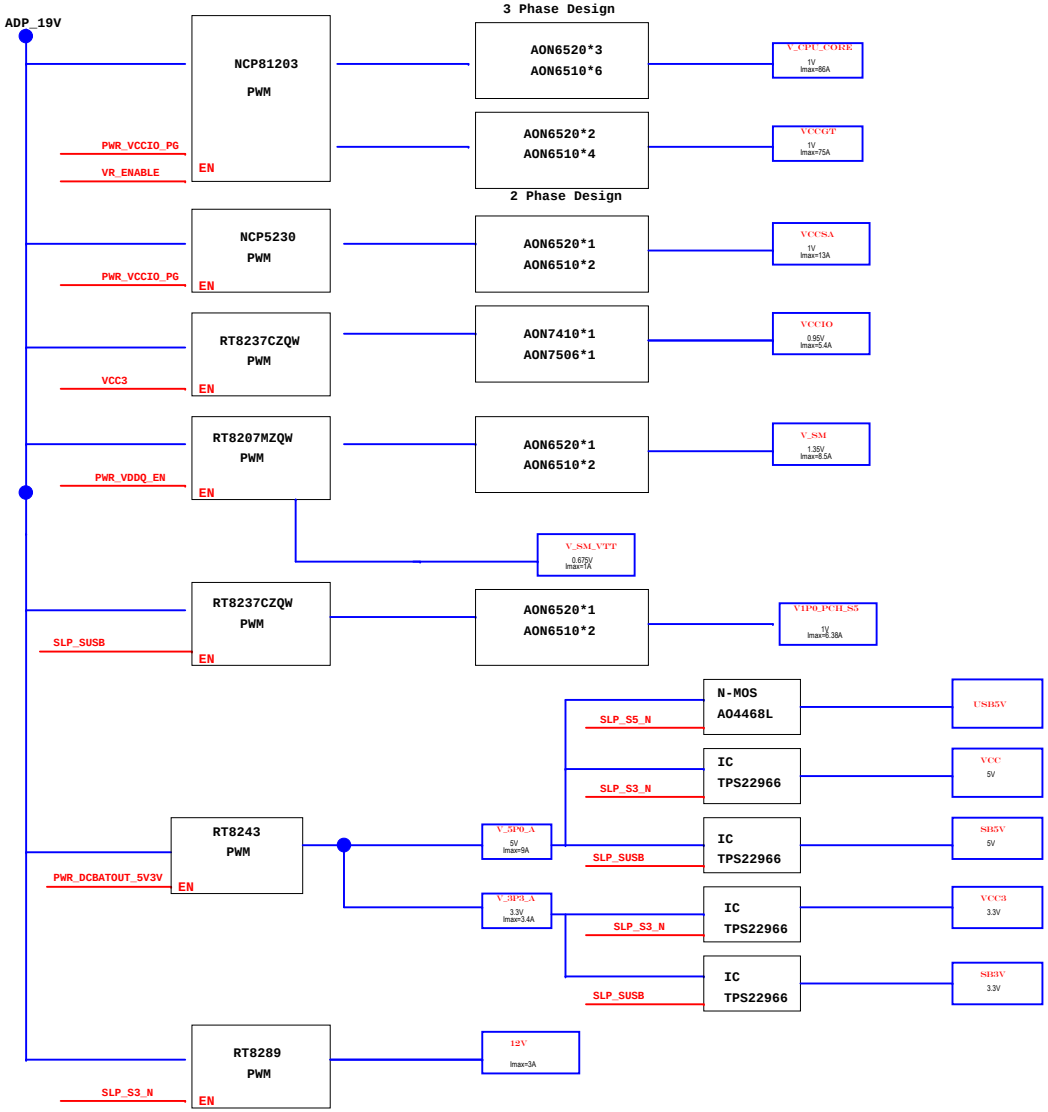
Size	Document Number	Rev
D	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 102 of 107

AC/DC ADAPTER

POWER: ADP-90WB
INPUT: 100-240V(1.5A)
OUTPUT: 19.5V(4.62A)



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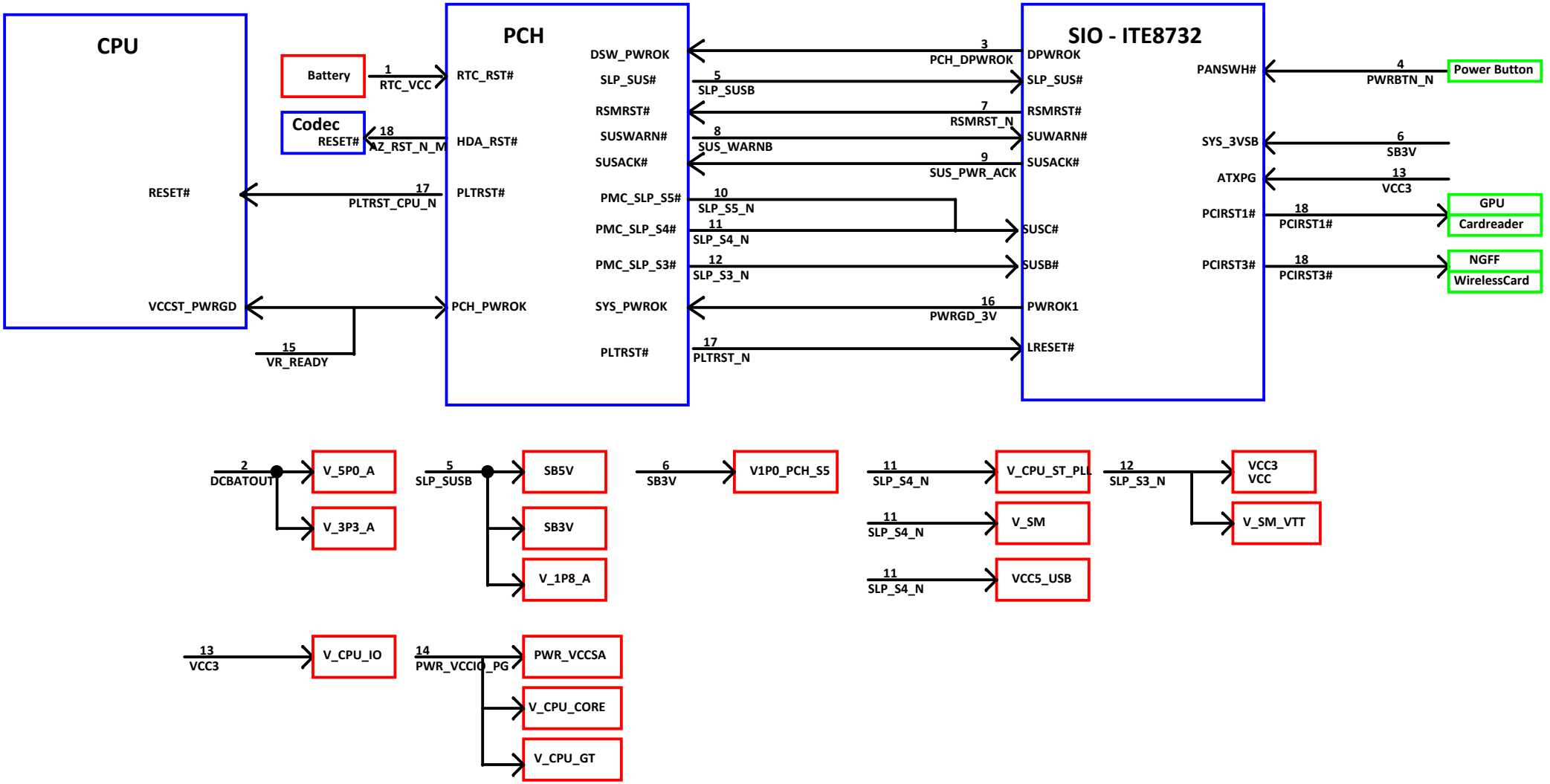
Title: 103_POWER BLOCK DIAGRAM

Size	Document Number	Rev
D	COLORADO MLK SKYLAKE-S	-2

Date: Sheet 103 of 107



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Title: 104_POWER GOOD & RESET DIAGRAM

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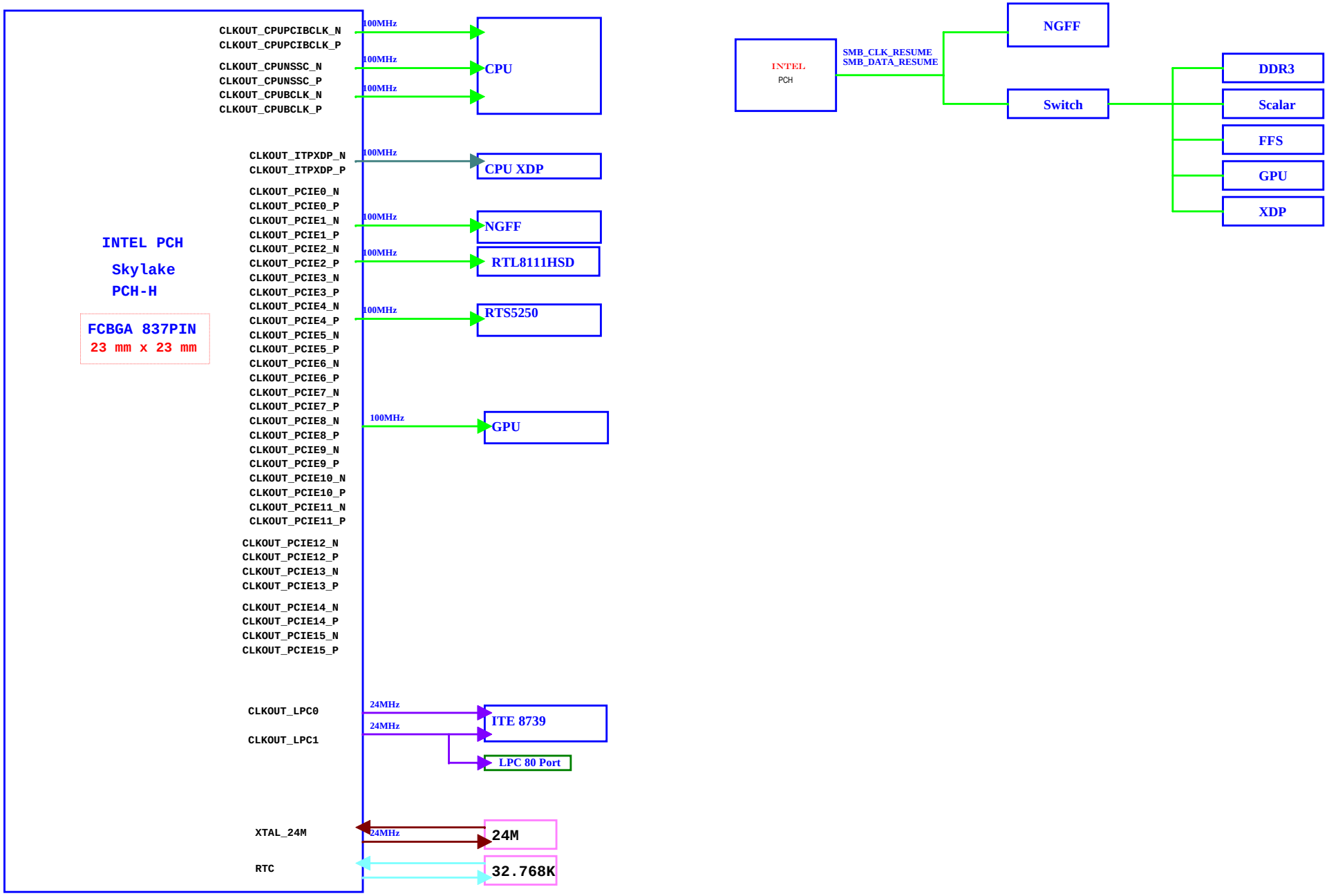
Date: | Sheet 104 of 107



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Title: 105_CLOCK DIAGRAM

Size	Document Number	Rev
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Date: Sheet 105 of 107

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Size: A	Document Number: COLORADO MLK SKYLAKE-S
Rev: -2	
Date:	Sheet 106 of 107

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Title	
Size: A	Document Number: COLORADO MLK SKYLAKE-S
Rev: -2	
Date:	Sheet 107 of 107