Compal Confidential

FLMS0

DIS M/B Schematic Document

Intel Ice Lake-U Processor with DDR4 Memory Down

2019-08-22

LA-J551P

REV :0.2

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Title: Cover Page			
Size: Custom	Document Number: LA-LJ551PR02		Rev: 0.2
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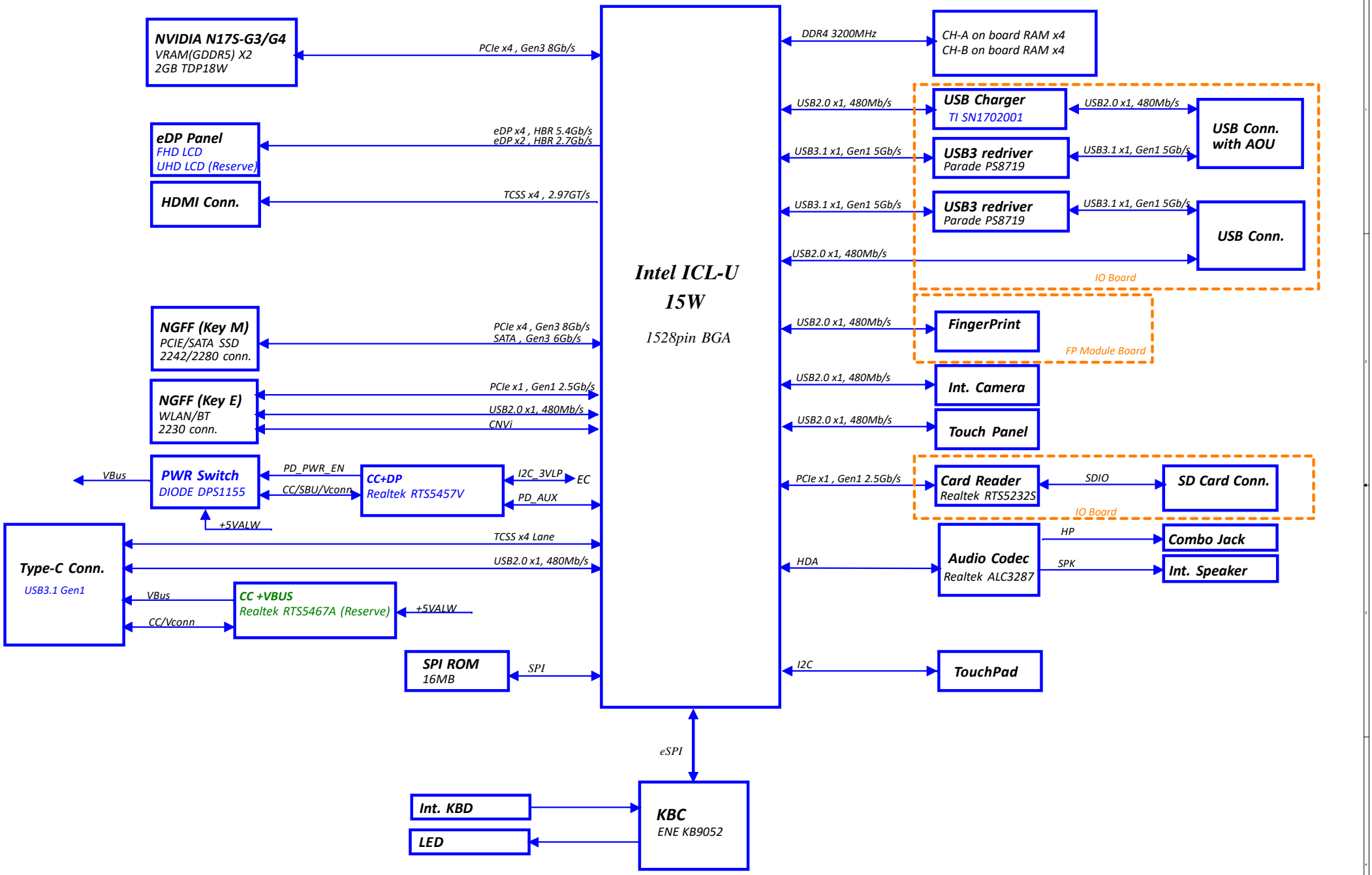

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Voltage Rails

power plane / State	+12.6VB	+5VALW +3VALW +1.8VALW	+1.2V +2.5V	+5VS +3VS +1.8VS +0.6VS +1.05V_VCCST +1.05VS_VCCSTG +VCCIN +VCCIN_AUX +1.8VS_DGPU +1.8VS_DGPU_AON +VGA_CORE +1.0VS_DGPU +1.35VS_VRAM
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
GPU N17S-G0/G2	DIS@
	UMA@
Debug	DCI@
Memory Down - SDP Package	SDP@
	SDP_CHB@
Memory Down - DDP Package	DDP@
	DDP_CHB@
Only CHB Memory Down	CHB@
Intel CNVi	CNVi@
Keyboard BackLight	KBL@
EMI Category	EMI@
ESD Category	ESD@
RF Category	RF@
Normal FP Device	FP@
SLIM_FP	SLIM_FP@
+12V FAN CAP	
+5V FAN CAP	
CPU MIC (Reserve)	Arrary_MIC@
	Single_MIC@
Modern standby	S0ix@
	NOS0ix@
Project select	
DDR4 Memory Down CHB	CHB@
GPU GC6 Mode	GC6@
	NOGC6@
Touch Screen Power	TS@
EC9052Q C Version	EC9052_C@
Option Bypass USB Charger	
	NON_AOU@
RMT tool test	RMT@
CPU select	QSQS_R1@
	QSQP_R1@
	QSQV_R1@
	QSVV_R1@
	QSQW_R1@

Item	BOM Structure
DGPU chip select	N17S_G0_R1@
	N17S_G0_R3@
	N17S_G2_R1@
	N17S_G2_R3@
VRAM chip select	VRAM_M2G_R1@
	VRAM_M2G_R3@
	VRAM_H2G_R1@
	VRAM_H2G_R3@
	VRAM_S2G_R1@
	VRAM_S2G_R3@

USB 2.0 Port Table

Port	External USB Port
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	Touch Screen
5	
6	Camera
7	Fingrt Print
8	
9	
10	NGFF WLAN+BT

TCP Port Table

Port	Lane
0	TYPE C (PD + CC)
1	HDMI
2	
3	

USB 3.0 Port Table

Port	
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	
4	
5	
6	

PCIE Port Table

Port	Lane	
1		
2		
3		
4	0	
5	0	
6	1	GPU
7	2	
8	3	
9	1	CardReader
10	0	NGFF WLAN+BT
11		
12	0	
13	3	
14	2	SSD
15	1	
16	0	

SATA Port Table

Port	
0	
1A	
1B	SSD

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x 16h
Charger (ISL88739A)	0001 001x 12h

EC SM Bus2 address

Device	Address
Thermal Sensor (F75305M)	1001_101xb 9Ah
Thermal Sensor (F75397M)	1001_100xb 98h

PCH SM Bus address

Device	Address
DDR_JDIMM1 Touch Pad	1010 010x A4h

GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111x 9Eh

SMBUS Control Table

	SOURCE	SOC	BATT	CHARGER	KB9052	SODIMM	Thermal Sensor	DGPU
EC_SMB_CK1 EC_SMB_DA1	KB9052 +3VL	X	V +3VALW	V +19V_VIN	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB9052	V +3VS	X	X	X	X	V +3VS	V +3VS
EC_SMB_CK4 EC_SMB_DA4	KB9052 +3VS	X	X	X	X	X	X	X
SOC_SMBCLK SOC_SMBDATA	SOC +3VS	X	X	X	X	V +3VS	X	X
SOC_SML0CLK SOC_SML0DATA	SOC +3VS	X	X	X	X	X	X	X

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

VRAM

ZZZ11 X76_H2G@ — X76 HYNIX 2GB — X7684838L11

ZZZ12 X76_S2G@ — X76 SAMSUNG 2GB — X7684838L12

ZZZ13 X76_M2G@ — X76 MICRON 2GB — X7684838L13

ICL-U CPU

UC1 QSQS_R1@ — I7-1065G7 — SA0000CT610

UC1 QSQP_R1@ — I5-1034G1 — SA0000CUQ10

UC1 QSQV_R1@ — I5-1035G1 — SA0000CTB10

UC1 QSVV_R1@ — I3-1005G1 — SA0000CVQ10

UC1 QSQW_R1@ — I3-1005G1 — SA0000CTD10

DGPU

R1	UV1 SA0000CC940 N17S_G0_R1@ N17S-G0	UV1 SA0000CCB30 N17S_G2_R1@ N17S-G2
R3	UV1 SA0000CC910 N17S_G0_R3@ N17S-G0	UV1 SA0000CCB10 N17S_G2_R3@ N17S-G2

VRAM

	Micron	Hynix	Samsung
R1	UV21 SA00009T30 VRAM_M2G_R1@ MT51J256M32HF-80	UV21 SA0000C1710 VRAM_H2G@_R1@ H5GC8H24AJR-R2C	UV21 SA00009TA50 VRAM_S2G@_R1@ H5GC8H24AJR-R2C
	UV22 SA00009T30 VRAM_M2G_R1@ MT51J256M32HF-80	UV22 SA0000C1710 VRAM_H2G@_R1@ H5GC8H24AJR-R2C	UV22 SA00009TA50 VRAM_S2G@_R1@ H5GC8H24AJR-R2C
R3	UV21 SA00009T50 VRAM_M2G_R3@ MT51J256M32HF-80	UV21 SA0000C1730 VRAM_H2G@_R3@ H5GC8H24AJR-R2C	UV21 SA0000C1730 VRAM_S2G@_R3@ H5GC8H24AJR-R2C
	UV22 SA00009T60 VRAM_M2G_R3@ MT51J256M32HF-80	UV22 SA0000C1730 VRAM_H2G@_R3@ H5GC8H24AJR-R2C	UV22 SA0000C1730 VRAM_S2G@_R3@ H5GC8H24AJR-R2C

ON BOARD RAM X76

ZZZ7 X76_H16G_2CH_2666@ — X76 HYNIX 16GB DUAL — X7684838L07

ZZZ3 X76_S16G_2CH_2666@ — X76 SAMSUNG 16GB DUAL — X7684838L05

ZZZ10 X76_M4G_1CH_3200@ — X76 MICRON 4GB SINGEL — X7684838L10

ZZZ6 X76_H4G_1CH_2666@ — X76 HYNIX 4GB SINGEL — X7684838L04

ZZZ2 X76_S4G_1CH_2666@ — X76 SAMSUNG 4GB SINGEL — X7684838L02

ZZ9 X76_M8G_2CH_3200@ — X76 MICRON 8GB DUAL — X7684838L09

ZZZ5 X76_H8G_2CH_2666@ — X76 HYNIX 8GB DUAL — X7684838L03

ZZZ1 X76_S8G_2CH_2666@ — X76 SAMSUNG 8GB DUAL — X7684838L01

PCB PN

ZZZ — PCB FL535 LA-H105P — DA80001LE00

X4E

ZZZ14 X4E_DIS@ — X4E S550- ICL DIS — X4EAJY38L01

ZZZ15 X4E_UMA@ — X4E S550- ICL UMA — X4EAJY38L02

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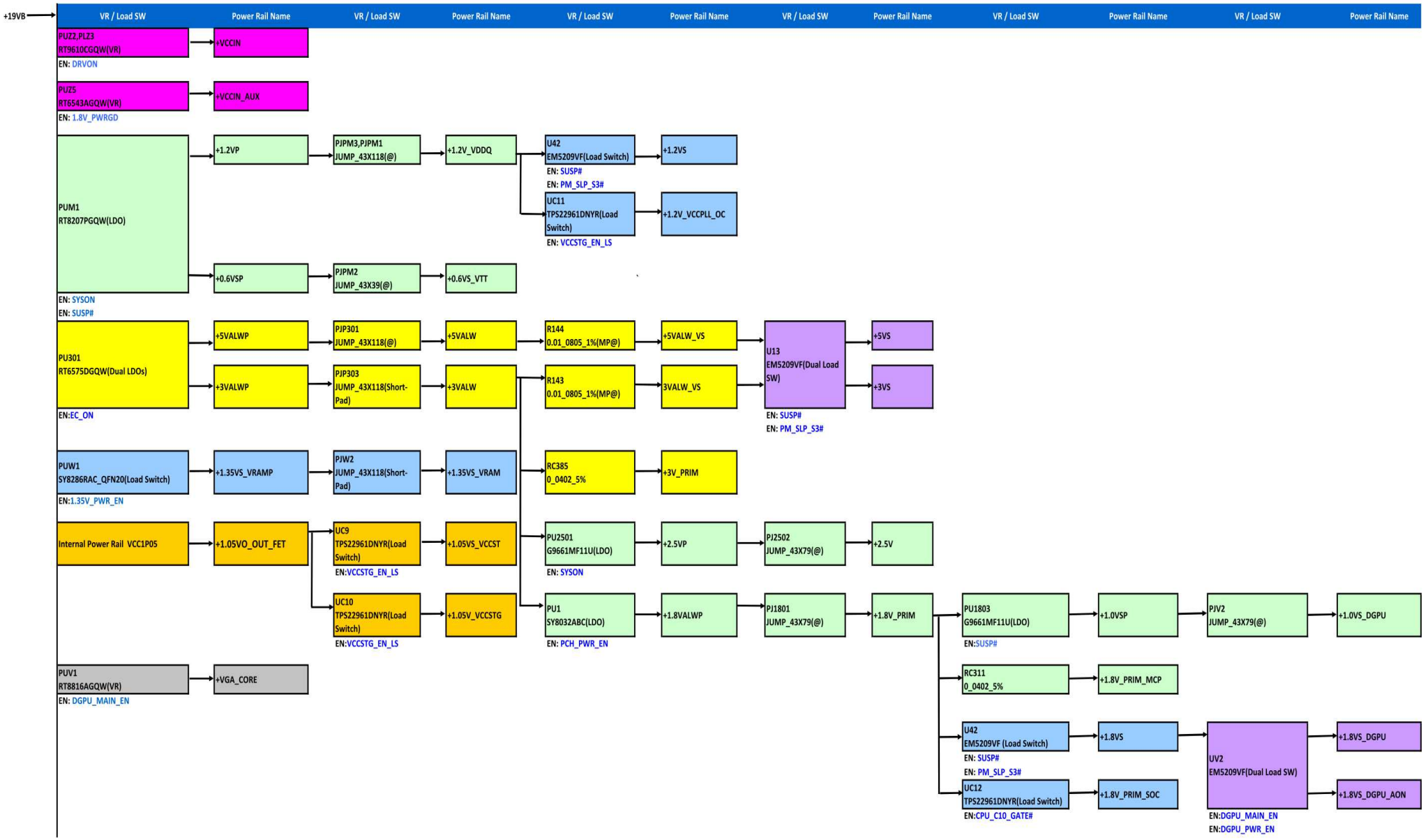
[DQA04-Power Map_ICL-U4+2_DDR4_Volume_S0ix]



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Title: Power MAP			
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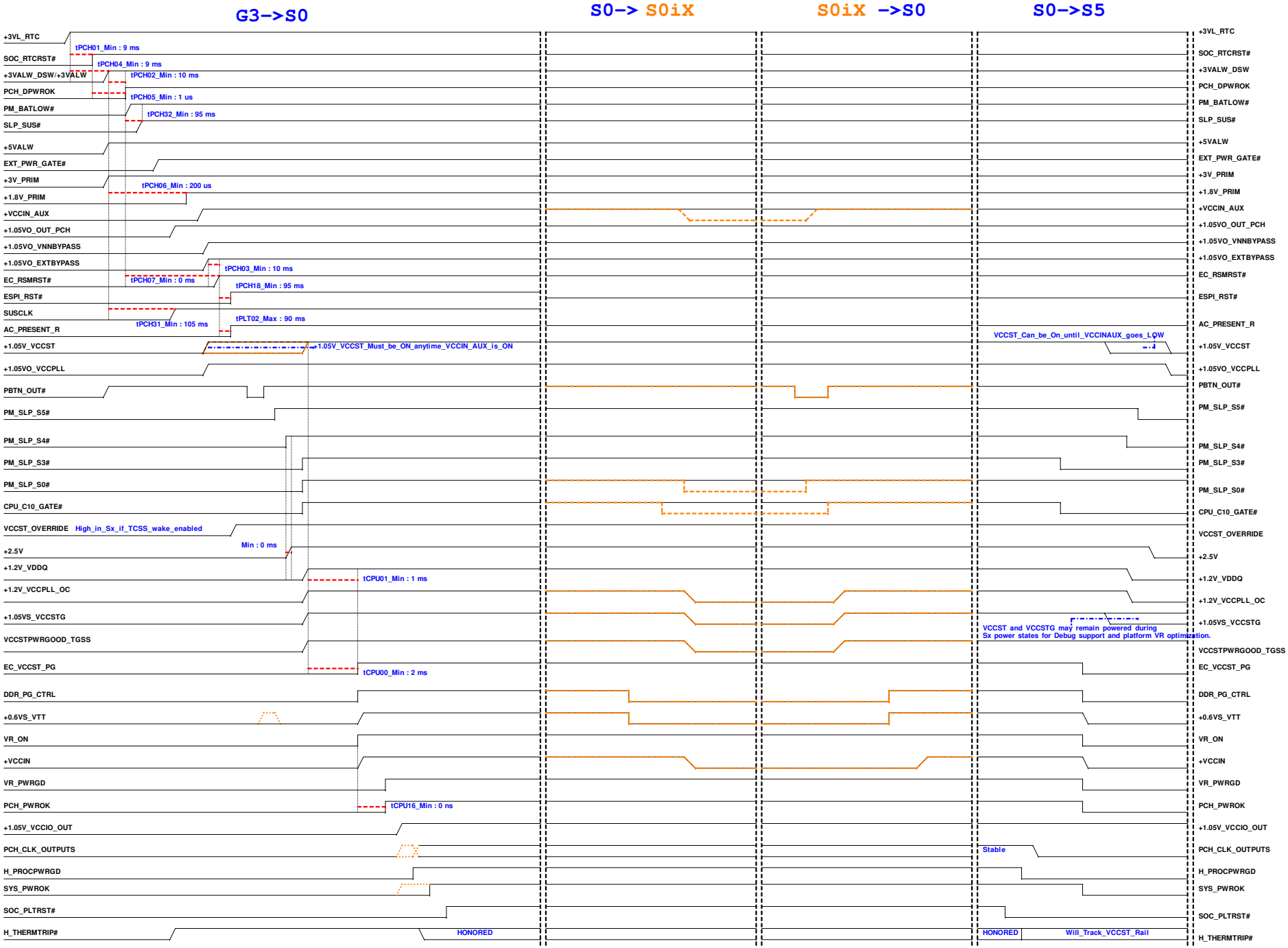
[DQA04-PWR Sequence_ICL-U4+2_DDR4_Volume_S0iX]



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Title: Power Sequence

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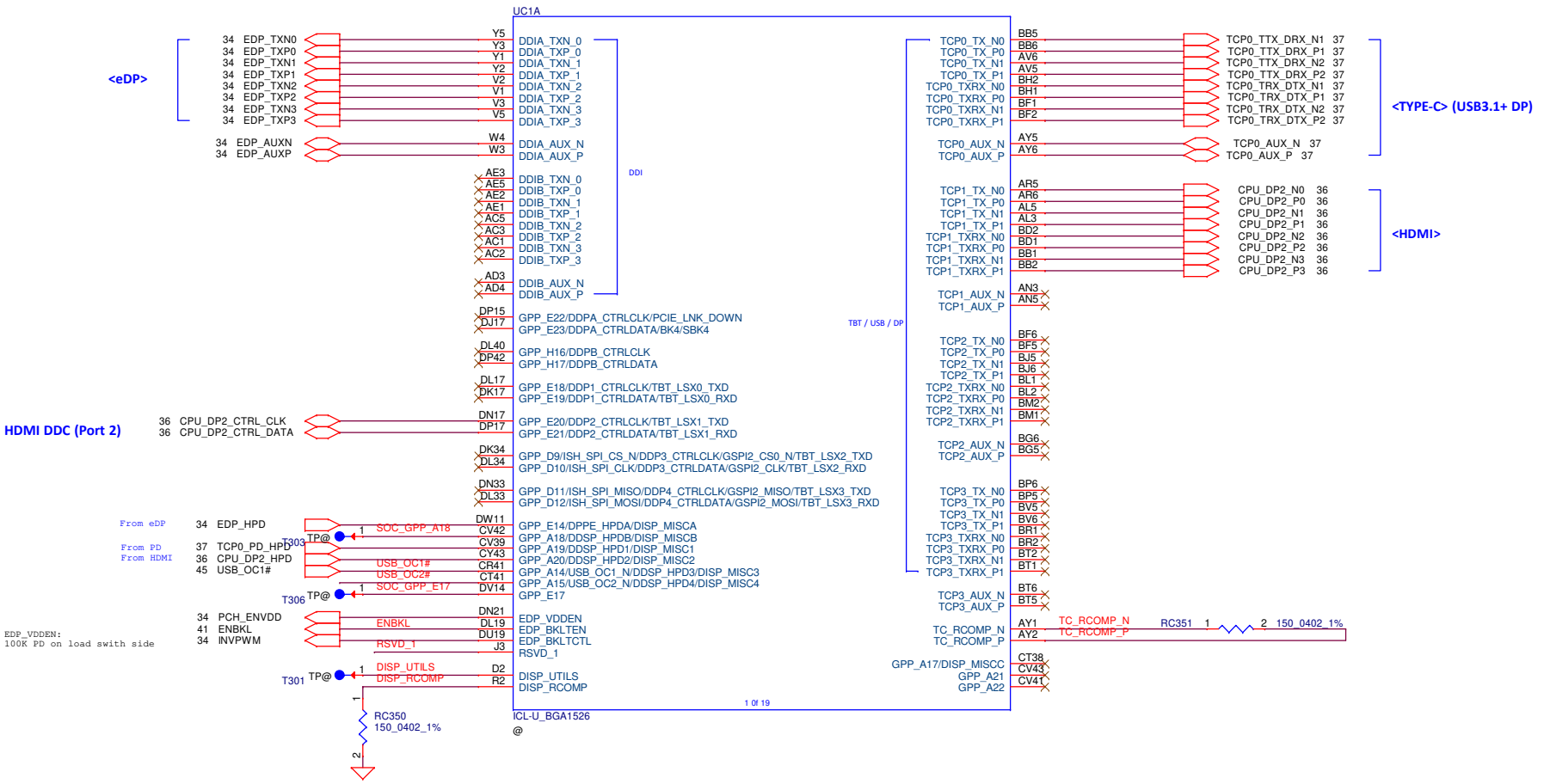

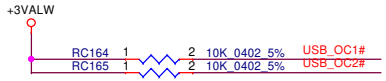

RSVD_1:
Follow 573129_ICL_U_DDR4_SODIMM_HW_SCH_RN

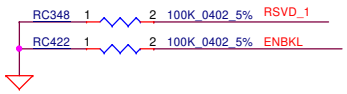

Table 5-11. USB3/USB2 Port Pairing for USB Type-C Connectors

	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

To make split xDCI controller working functionally for different USB-C connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C connectors, but it is not strictly required.

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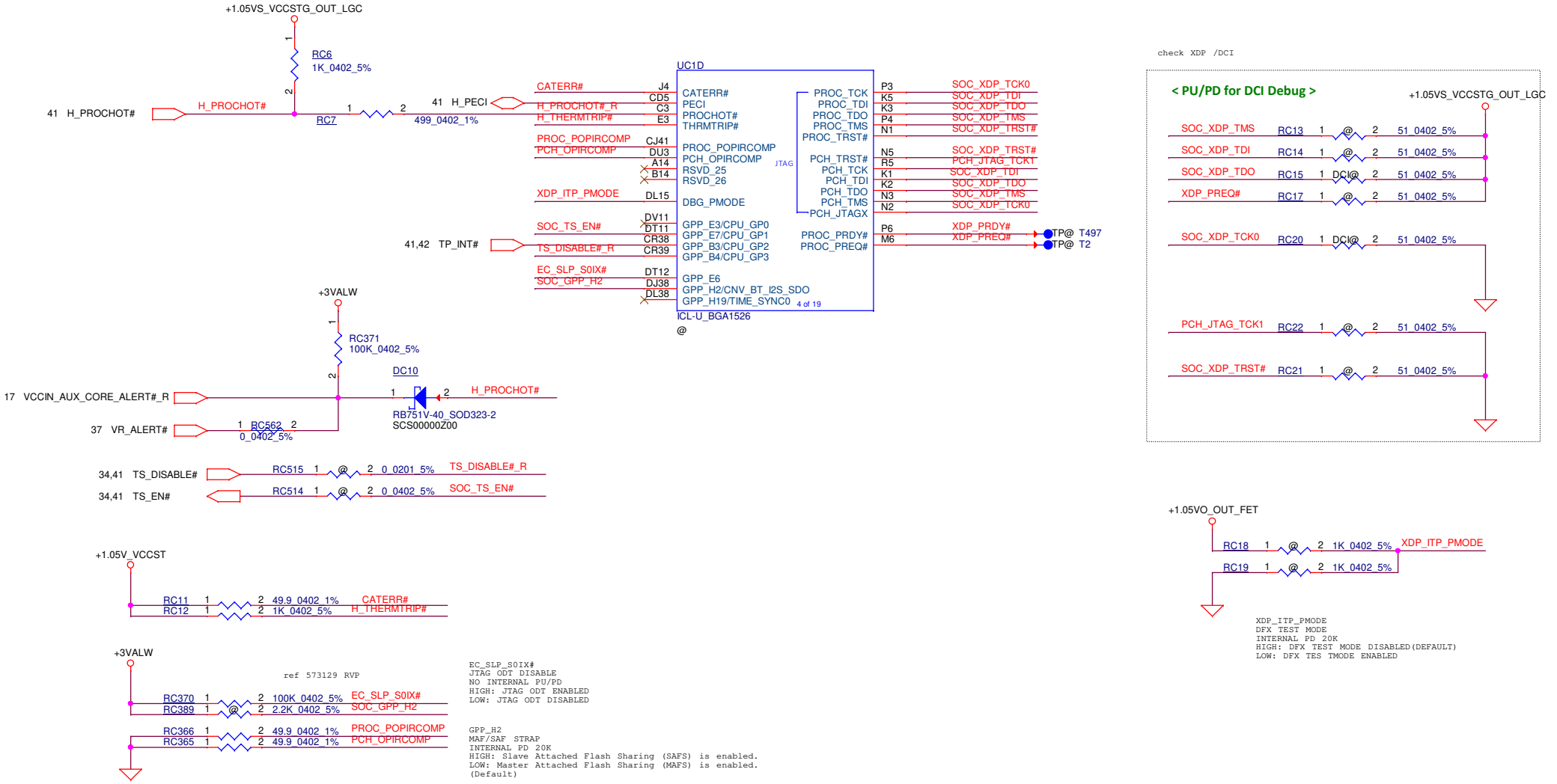

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Title	ICL-U(1/14)DDI,MSIC,XDP		
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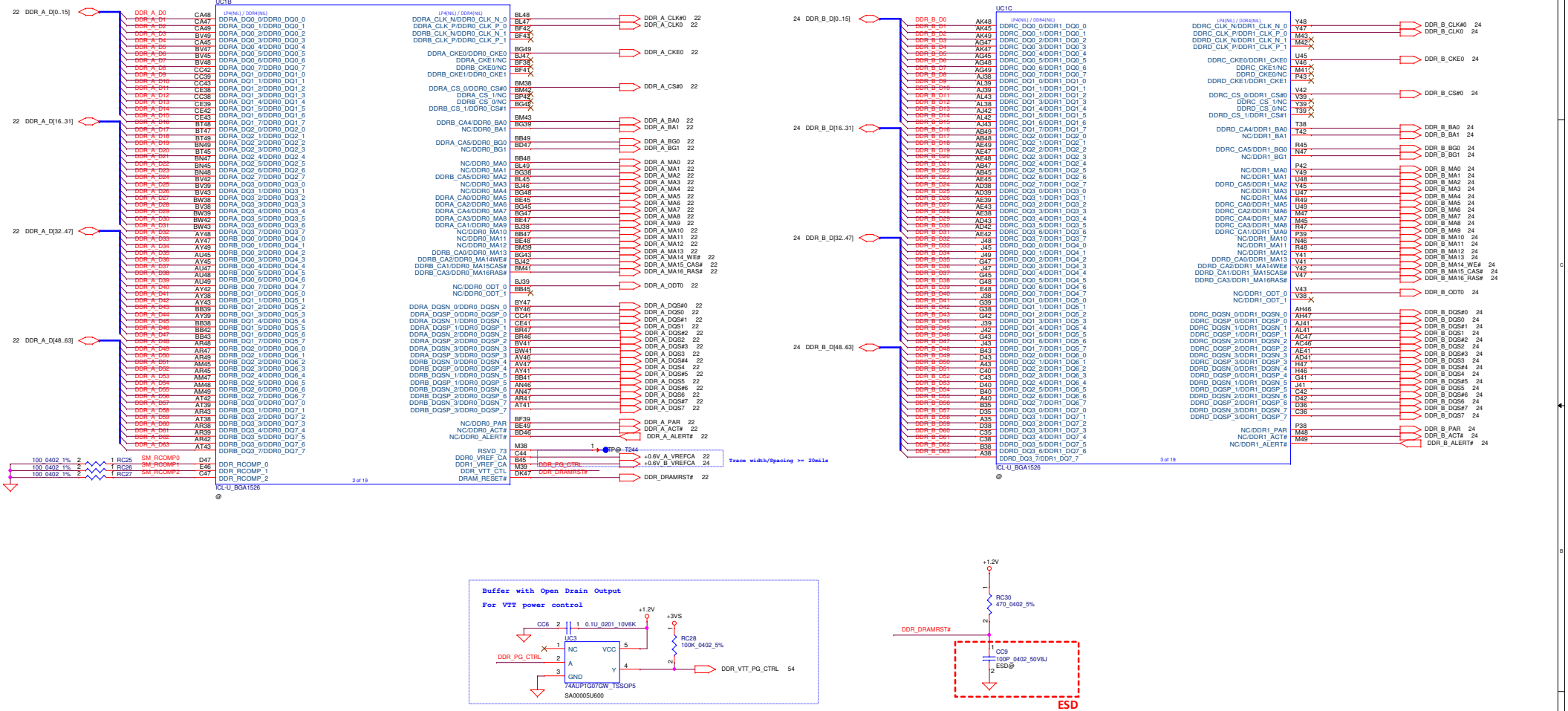
Follow Intel DDR4 NIL

DDR4: Refer to 575034_ICL_U42_DDR4_T3_6L_Core_Schematics_Rev0p7



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Title: **ICL-U(3/14)DDR4**

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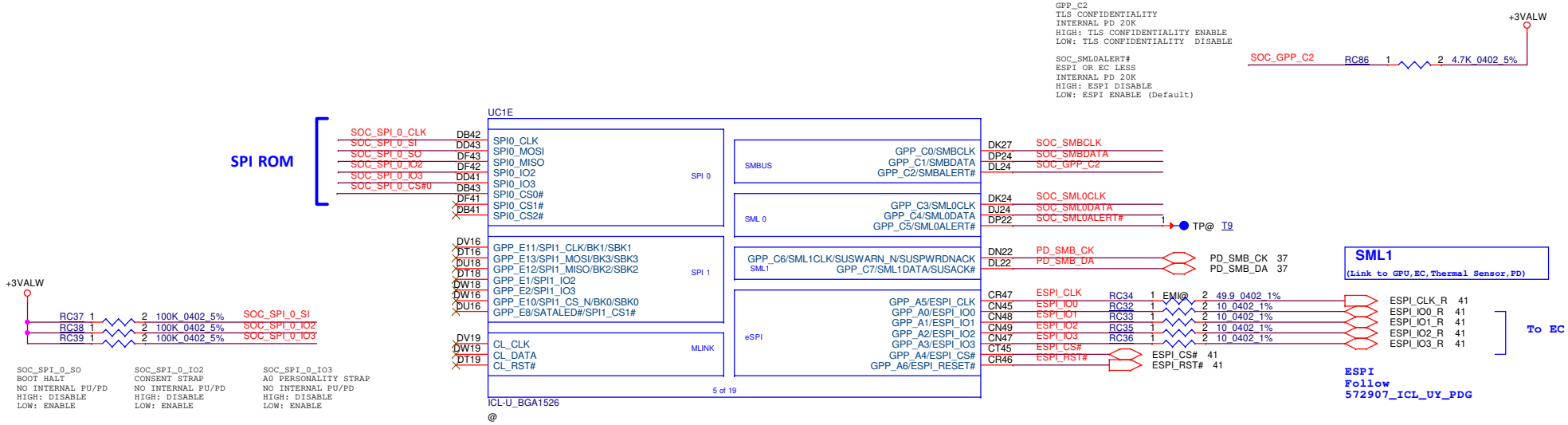
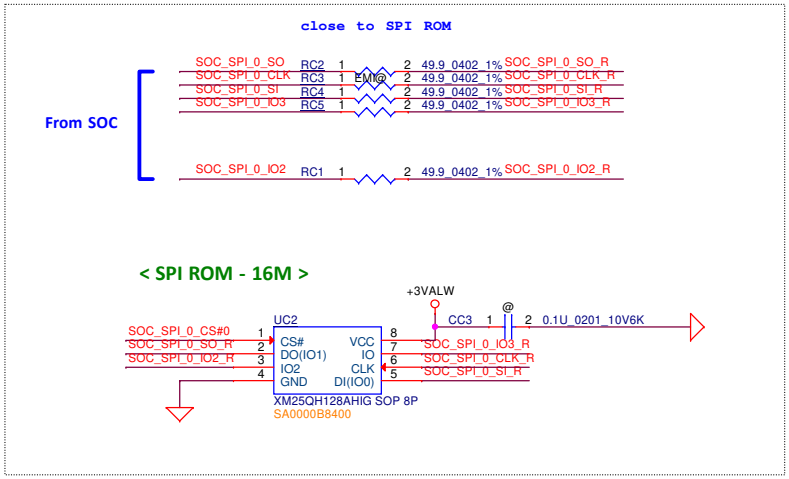
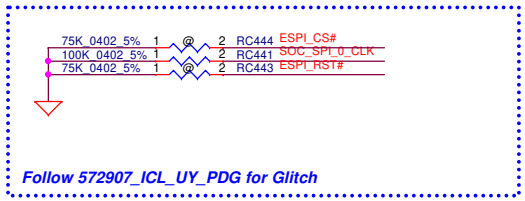
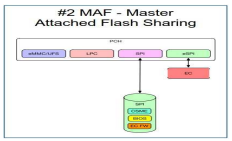


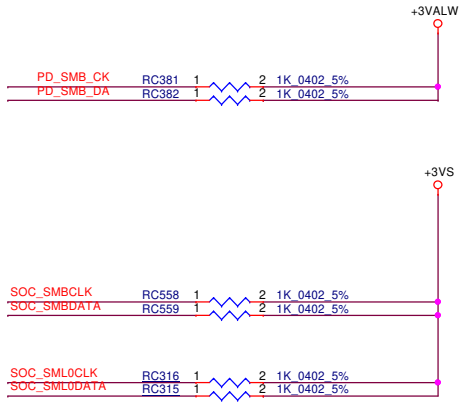
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.







MAF - Master Attached Flash
Single SPI Flash attached to SPI Bus
EC FW access through eSPI Bus



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Title: **ICL-U(3/12)SPI,ESPI,SMB,LPC**

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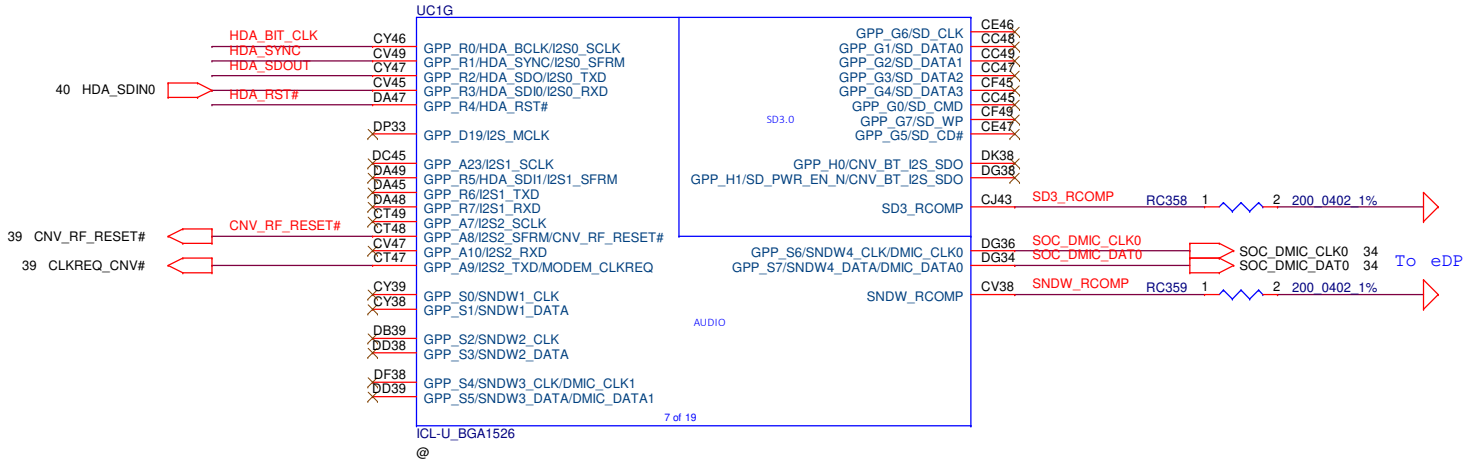

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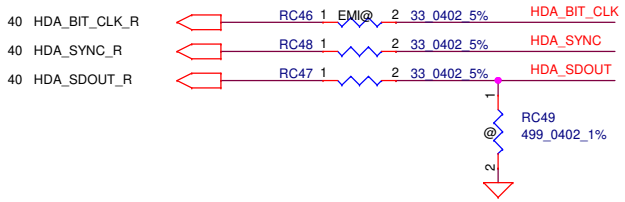

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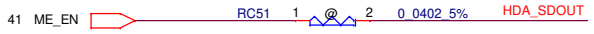

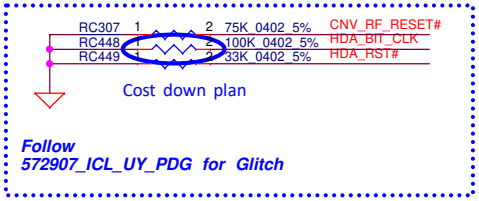

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Title: **ICL-U(4/12)HDA,SD**

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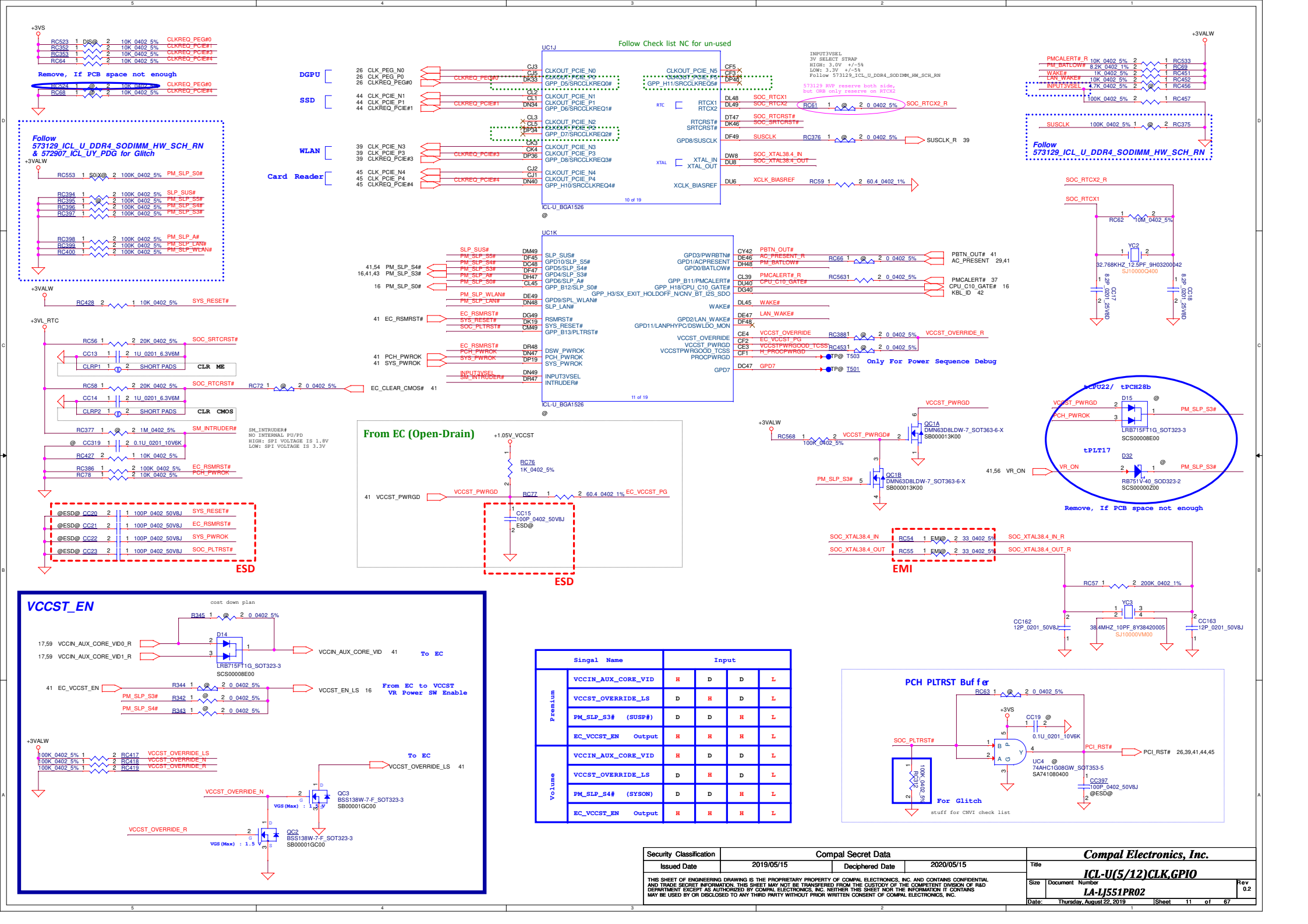

	Singal Name	Input			
Premium	VCCIN_AUX_CORE_VID	H	D	D	L
	VCCST_OVERRIDE_LS	D	H	D	L
	PM_SLP_S3# (SUSP#)	D	D	H	L
	EC_VCCST_EN Output	H	H	H	L
Volume	VCCIN_AUX_CORE_VID	H	D	D	L
	VCCST_OVERRIDE_LS	D	H	D	L
	PM_SLP_S4# (SYSON)	D	D	H	L
	EC_VCCST_EN Output	H	H	H	L

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Title	ICL-U(5/12)CLK,GPIO		
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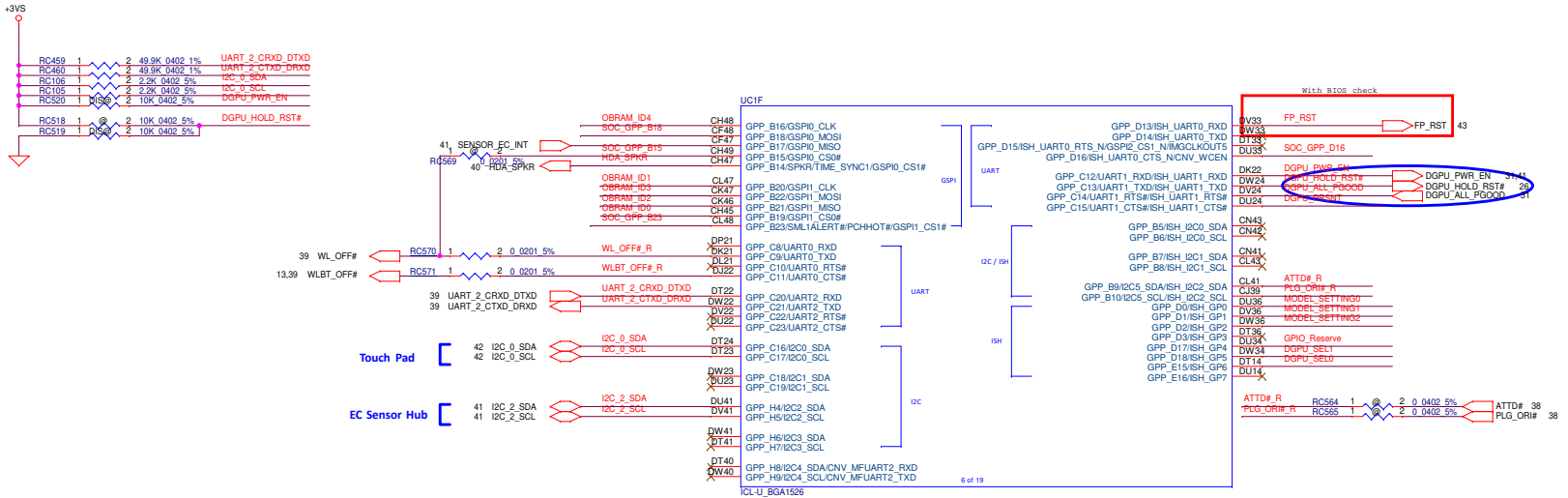
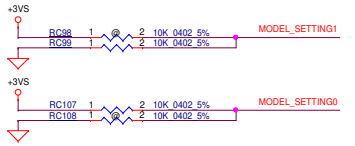
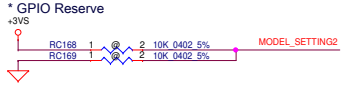


Function	MODEL_SETTING1 (GPP_D1)	MODEL_SETTING0 (GPP_D0)
S550	0	1

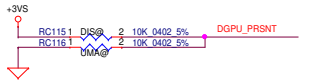


Function	MODEL_SETTING2 (GPP_D2)
Arrary MIC	1
Single MIC	0

* GPIO Reserve

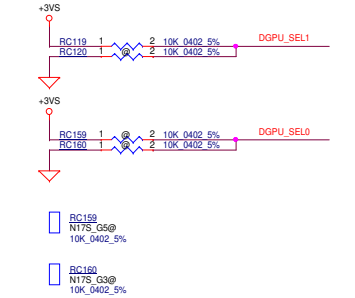


DGPU Select

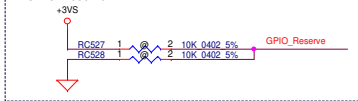


Function	DGPU_SEL1 (GPP_D18)	DGPU_SEL0 (GPP_D15)
N17S-G0	0	0
N17S-G2	0	1
N17S-G3	1	0
N17S-G5	1	1

* N17S-G0/G2 only for SDV phase

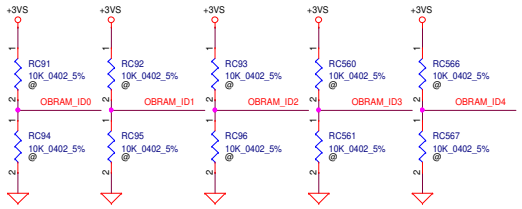


GPIO Reserve

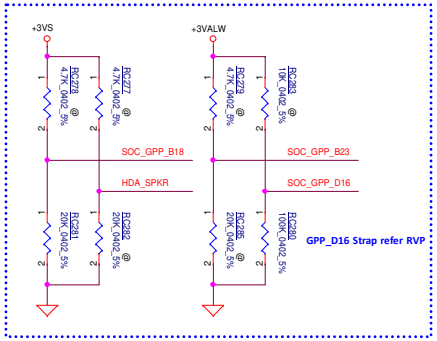


Place the same side(TOP/BOT) with on board RAM IC

Capacity	Description	Part Number	Used Channel	OBRAM_ID4	OBRAM_ID3	OBRAM_ID2	OBRAM_ID1	OBRAM_ID0	X'76 Number	DDR4 System total size
8Gb-2666	SS D4 K4A8G165WC-BCTD SDP	SA0000B6F00	1	0	0	0	0	0	X7684838L02	4GB
	HY D4 H5AN8G6NCJR-VKC SDP	A0000BMN00	1	0	0	0	0	1	X7684838L04	
16Gb-2666	SS D4 K4AAG165WA-BCTD SDP	SA0000CNO00	1	0	0	0	1	0	X7684838L06	8GB
	HY D4 H5ANAG6NCMR-VKC DDP	SA0000BZJ00	1	0	0	0	1	1	X7684838L08	
8Gb-3200	SS D4 K4A8G165WC-BCWE SDP	SA0000CZ500	1	0	0	1	0	0	TBD	4GB
	HY D4 H5AN8G6NCJR-XNC SDP	SA0000CZ300	1	0	0	1	0	1	TBD	
	MC D4 MT40A512M16TB-062E:J SDP	SA0000CMS00	1	0	0	1	1	0	X7684838L10	
16Gb-3200	SS D4 K4AAG165WA-BCWE SDP	SA0000CZ200	1	0	0	1	1	1	TBD	8GB
	HY D4 H5ANAG6NCJR-XNC DDP	SA0000CZ100	1	0	1	0	0	0	TBD	
	MC D4 MT40A1G16RC-062E:B SDP	SA0000CSR00	1	0	1	0	0	1	TBD	
	MC D4 MT40A1G16KD-062E:E SDP	TBD	1	0	1	0	1	0	TBD	
8Gb-2666	SS D4 K4A8G165WC-BCTD SDP	SA0000B6F00	2	1	0	0	0	0	X7684838L01	8GB
	HY D4 H5AN8G6NCJR-VKC SDP	A0000BMN00	2	1	0	0	0	1	X7684838L03	
16Gb-2666	SS D4 K4AAG165WA-BCTD SDP	SA0000CNO00	2	1	0	0	1	0	X7684838L05	16GB
	HY D4 H5ANAG6NCMR-VKC DDP	SA0000BZJ00	2	1	0	0	1	1	X7684838L07	
8Gb-3200	SS D4 K4A8G165WC-BCWE SDP	SA0000CZ500	2	1	0	1	0	0	TBD	8GB
	HY D4 H5AN8G6NCJR-XNC SDP	SA0000CZ300	2	1	0	1	0	1	TBD	
	MC D4 MT40A512M16TB-062E:J SDP	SA0000CMS00	2	1	0	1	1	0	X7684838L09	
16Gb-3200	SS D4 K4AAG165WA-BCWE SDP	SA0000CZ200	2	1	0	1	1	1	TBD	16GB
	HY D4 H5ANAG6NCJR-XNC DDP	SA0000CZ100	2	1	1	0	0	0	TBD	
	MC D4 MT40A1G16RC-062E:B SDP	SA0000CSR00	2	1	1	0	0	1	TBD	
	MC D4 MT40A1G16KD-062E:E SDP	TBD	2	1	1	0	1	0	TBD	



Strap Pin



GPP_B18
No Reboot
INTERNAL PD 20K
HIGH: No Reboot
LOW: Reboot Enable (Default)

SPKR
TOP SWAP OVERRIDE
INTERNAL PD 20K
HIGH: Top swap enable
LOW: Disable (Default)

GPP_B23
CPUNSSC CLOCK FREQ
INTERNAL PD 20K
HIGH: 19.2 MHz (form internal divider)
LOW: 38.4 MHz (direct form crystal) (Default)

GPP_D16
MFR_MODE_DET_STRAP
Follow 573129_ICL_U_DDR4_SODIMM_HW_SCH_RN_1P0

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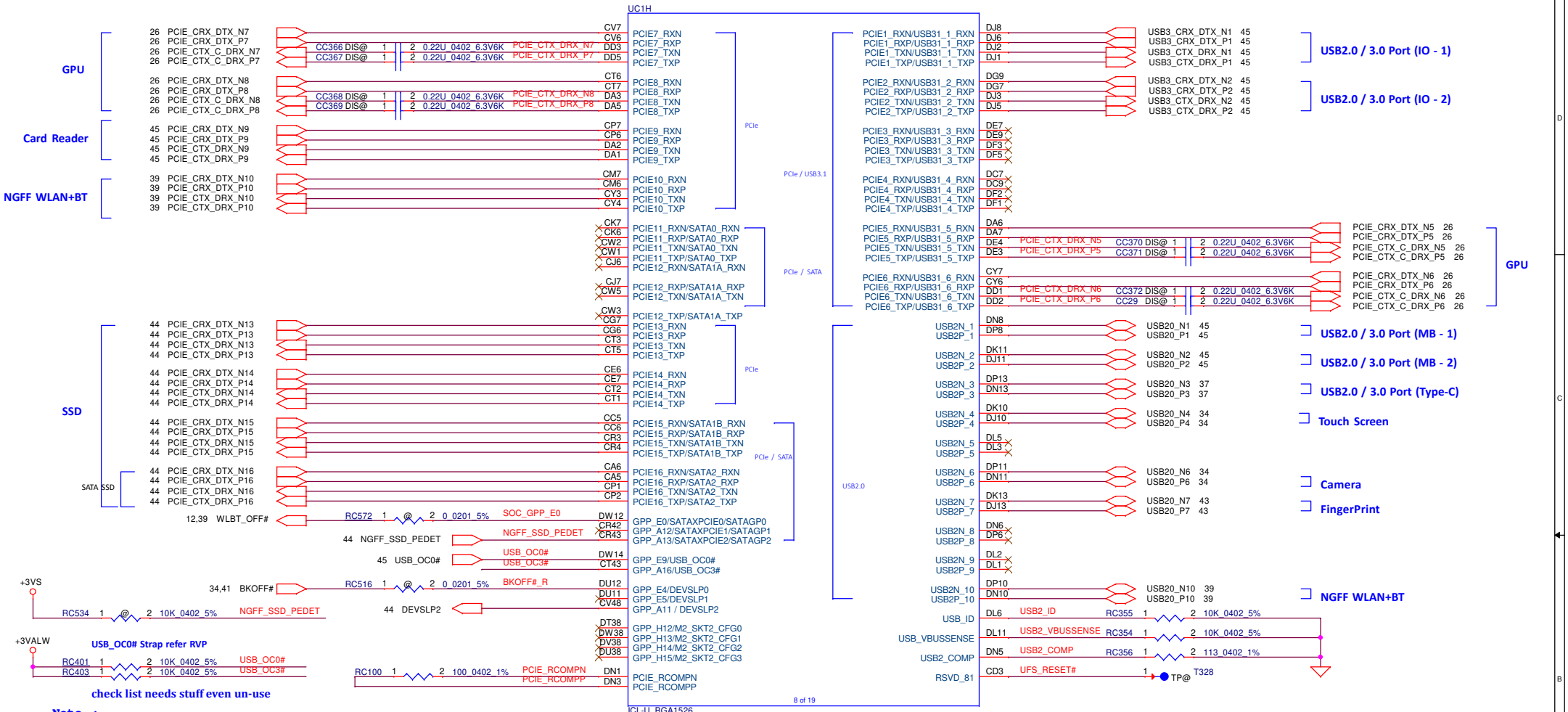

Note :
Please reference PCH EDS Tabel 1-2

Table 1-2. PCH HSIO Details

Flex I/O Lane	SKU		
	Premium U	Premium Y	Base U
0	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1
1	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1
2	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1
3	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1
4	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	PCIe*
5	USB3.1 Gen1/Gen2, PCIe*	USB3.1 Gen1/Gen2, PCIe*	PCIe*
6	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
7	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
8	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
9	PCIe*	PCIe*	PCIe*
10	PCIe*, SATA	PCIe*, SATA	PCIe*, SATA
11	PCIe*, SATA	PCIe*, SATA	PCIe*, SATA
12	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
13	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
14	PCIe*, SATA	NA	PCIe*
15	PCIe*, SATA	NA	PCIe*

Table 6-24. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[1]	None[2]	None[3]

Notes:
1. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
2. For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
3. For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

From Max reply mail

CHIPSET SKU	Max Number of USB 2.0 Ports	USB 2.0 Port # 1	USB 2.0 Port # 2	USB 2.0 Port # 3	USB 2.0 Port # 4	USB 2.0 Port # 5	USB 2.0 Port # 6	USB 2.0 Port # 7	USB 2.0 Port # 8	USB 2.0 Port # 9	USB 2.0 P10 / Integrated Intel® Wireless-AC
PREM-U	10										
MAINSTREAM BASE_U	8										

Port Disabled | Port Enabled | Port Enabled for Intel® Wireless-AC only

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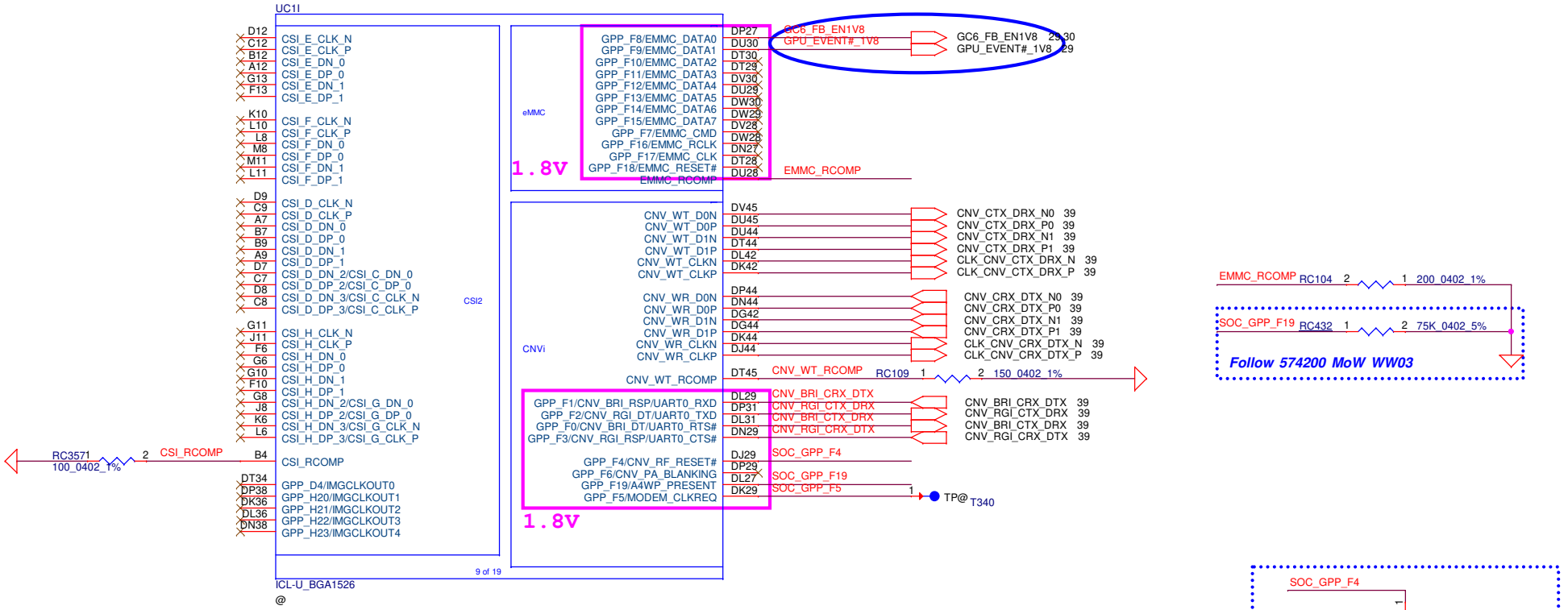

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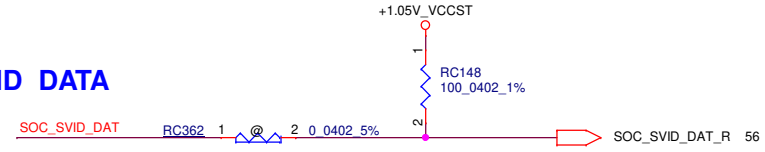
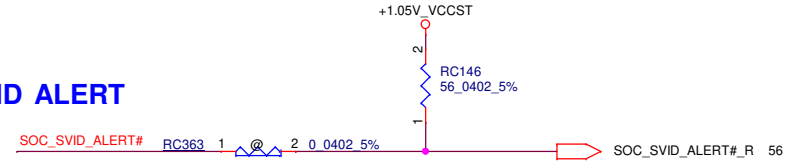
SVID DATA



SVID ALERT



SVID CLOCK

5.5.10 SVID Topology

Figure 5-54. Routing Illustration for SVID Topology

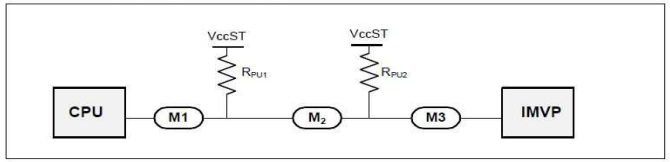
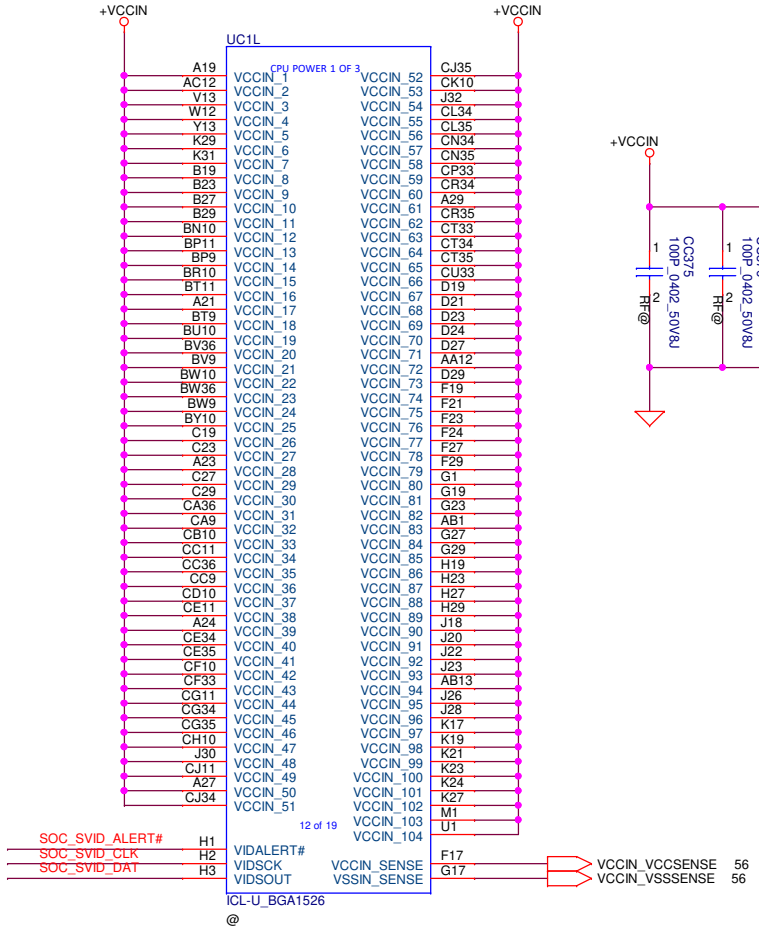
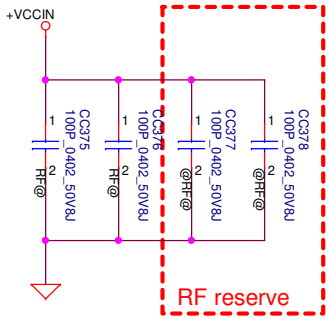


Figure above demonstrates Routing Illustration for SVID Topology, each trace from CPU to VR represents 3 signals: VIDSOUT, VIDSCK, VIDSALERT#.

Table 5-75. SVID Routing Guidelines

Segment	Tline Type	Reference	Via Count	Max Length, mm	
				Segment	Total
M1	MS/SL/DSL	VSS		75	530
M2	MS/SL/DSL	VSS		380	
M3	MS/SL/DSL	VSS		75	
Topology Guidelines					
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#				
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω				
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω				
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty				
Platform resistors tolerances	± 5%				
Route ordering	When routing at minimum spacing route Alert between Data and Clock				





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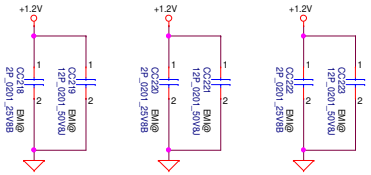
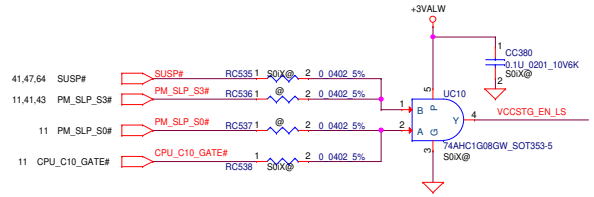
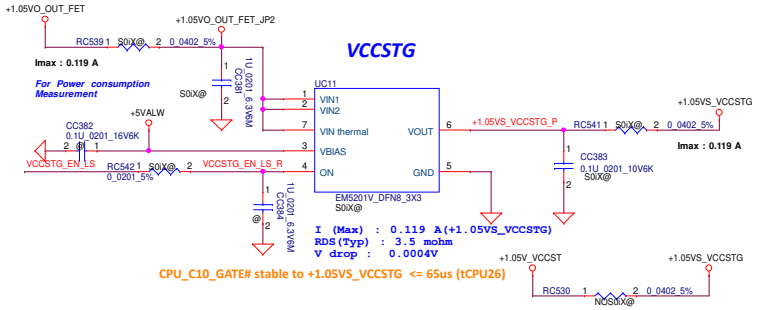
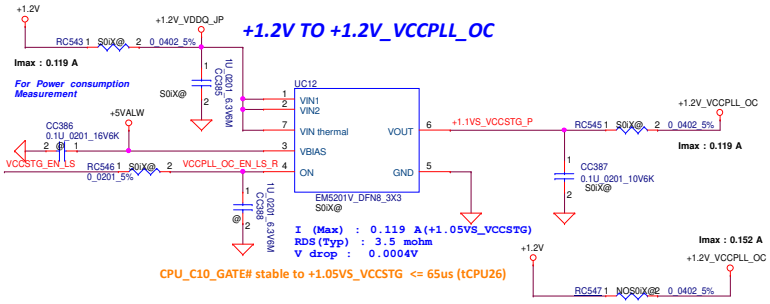
EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 3 (EMI@)
2pF* 3 (EMI@)

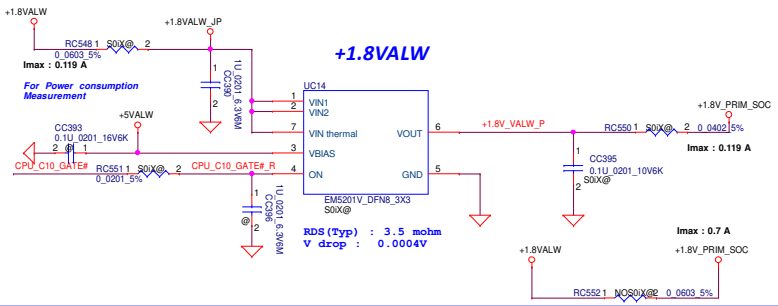


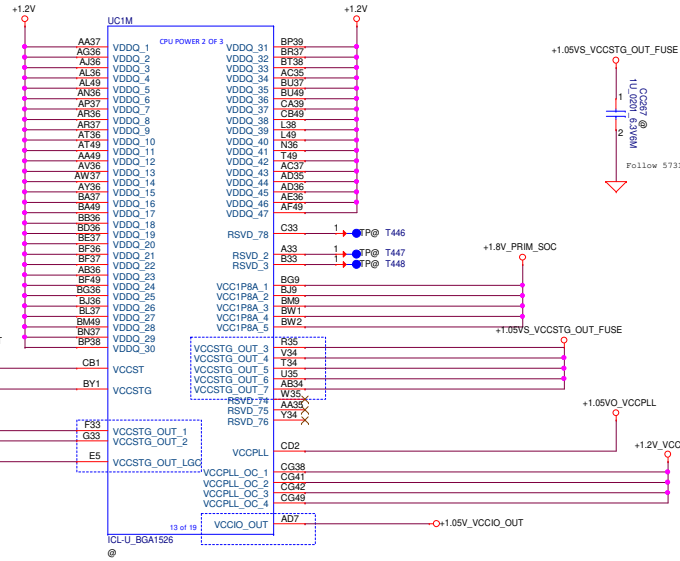
Modern Standby

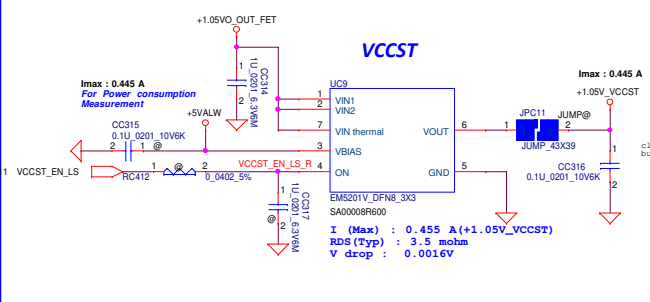


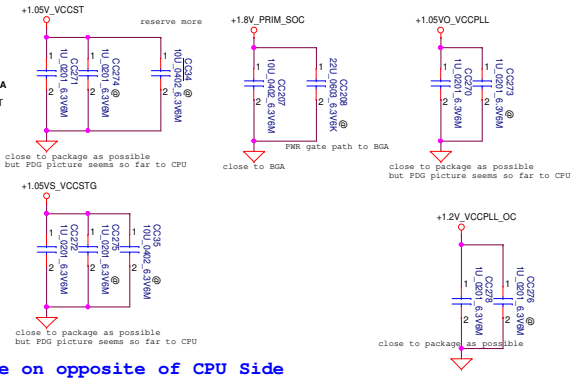




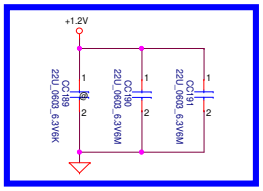




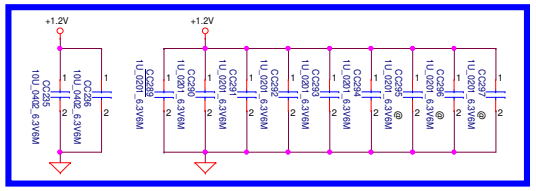




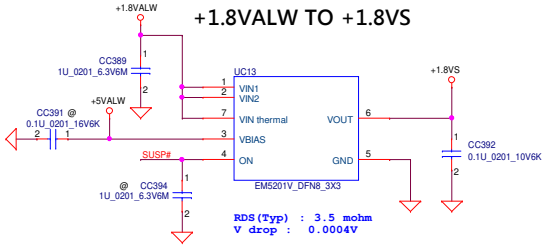
Place on CPU Side
22uF* 2 + 22uF* 1 (Reserved)



Place on opposite of CPU Side
1uF* 6 + 1uF*3 reserve
10uF* 2



+1.8VALW TO +1.8VS



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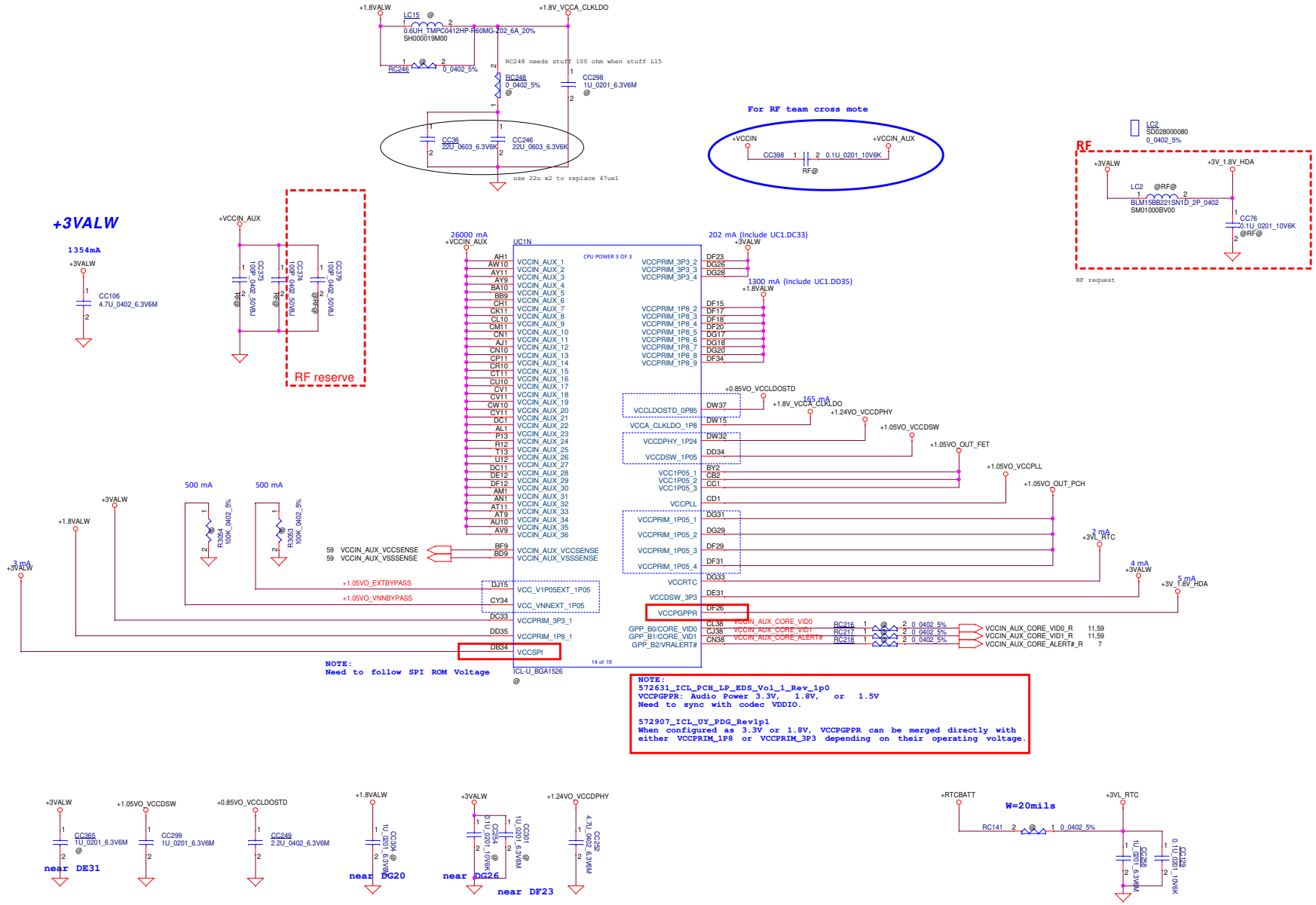

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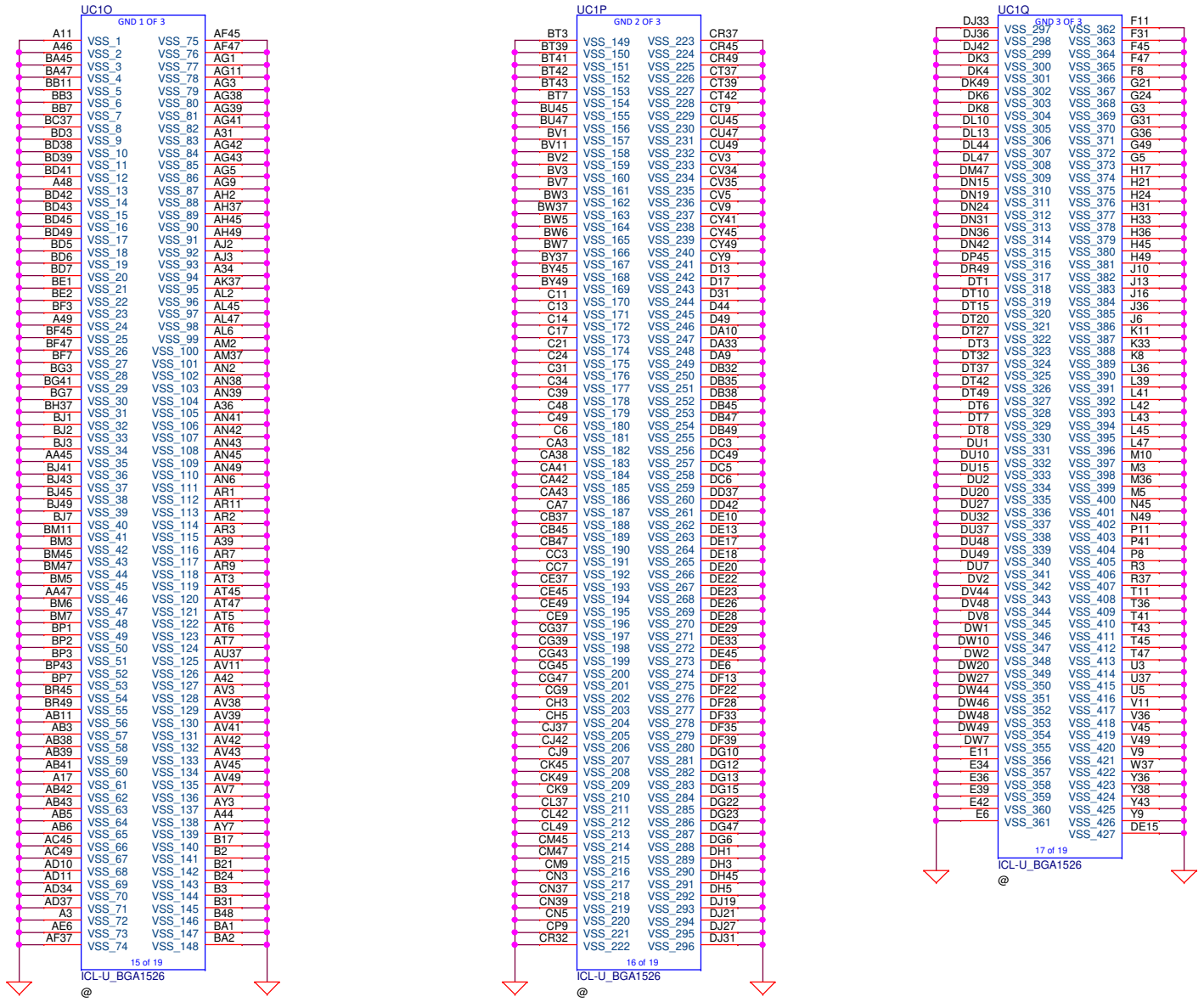

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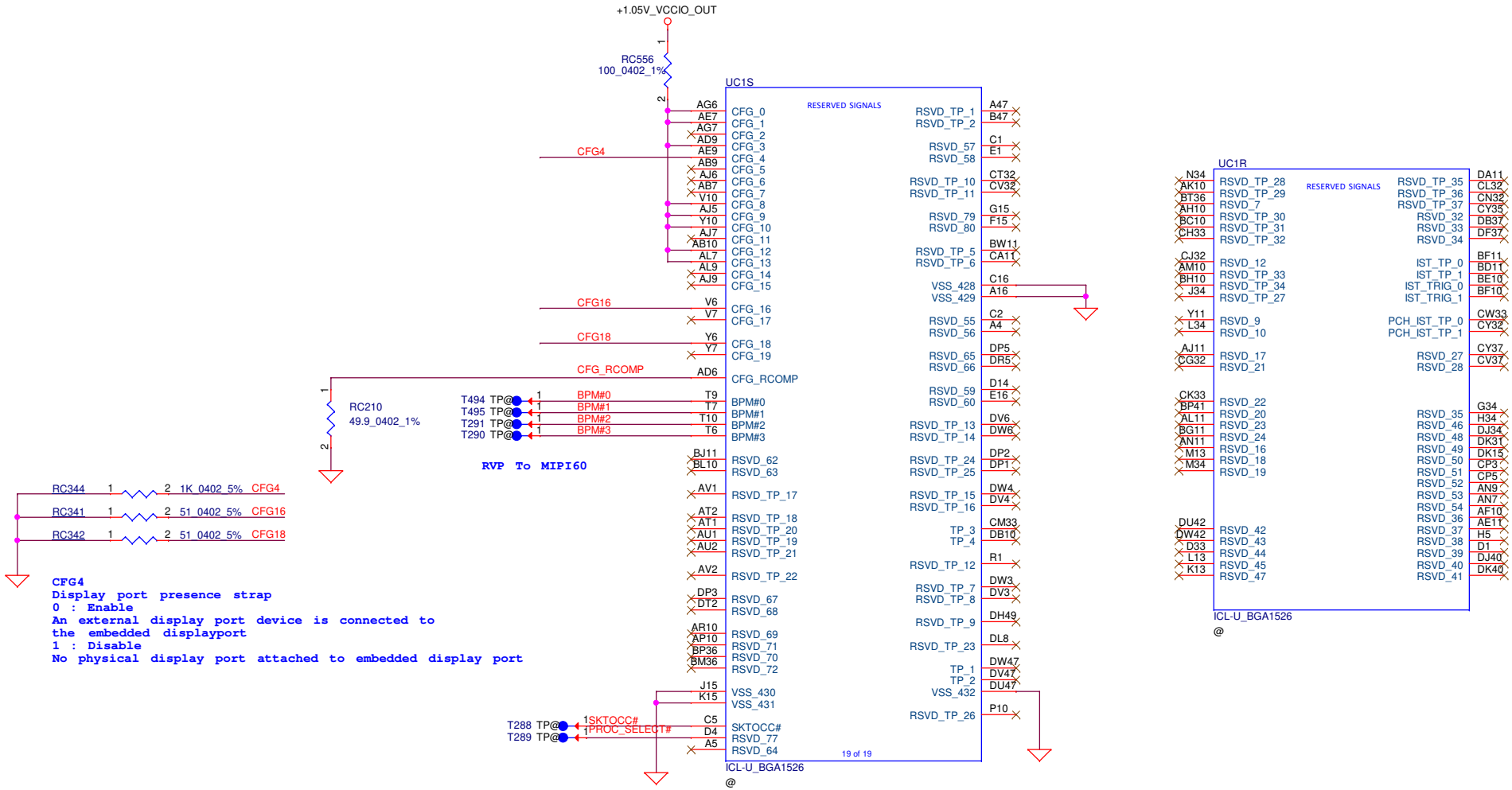

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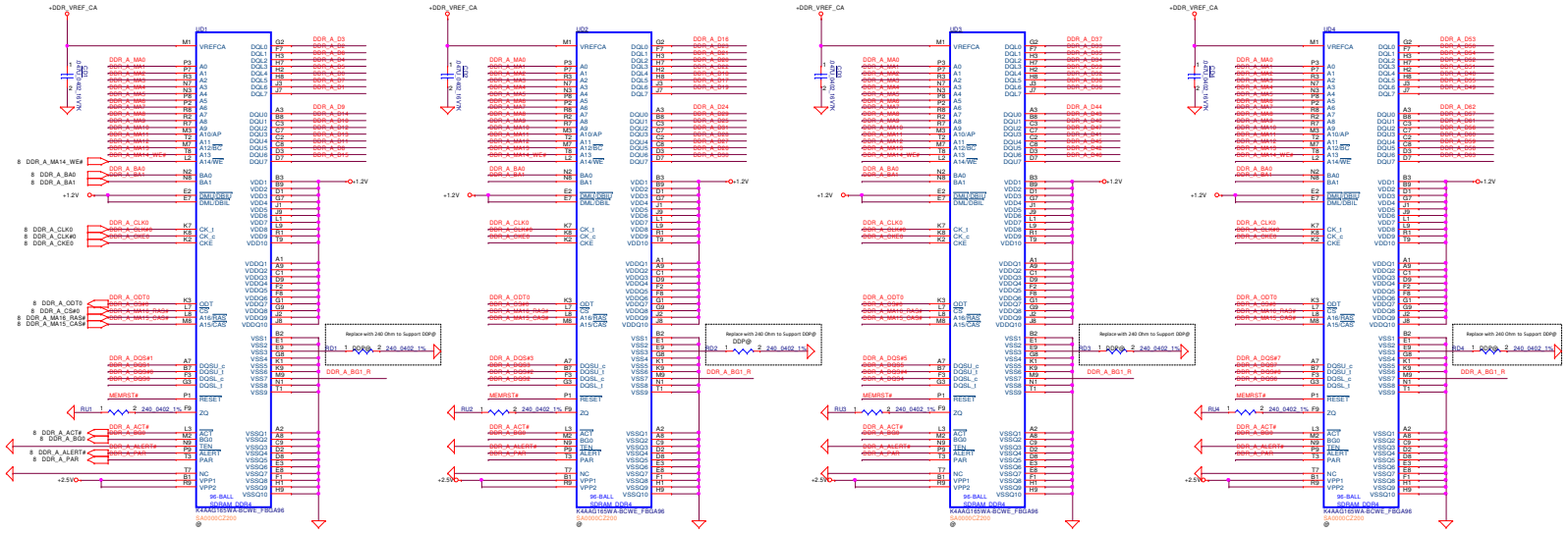
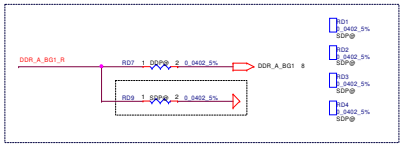
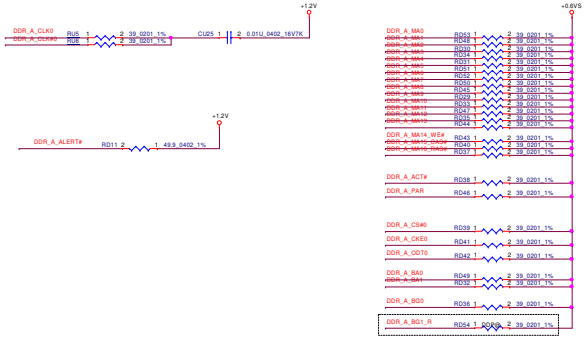


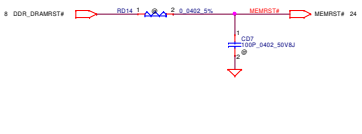
8 DDR_A_MA[0..13]
8 DDR_A_DQS[0..7]
8 DDR_A_DQS#[0..7]
8 DDR_A_DJ[0..63]

Co-lay for SDP / DDP Memory DIE



CLOCK TERMINATION





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Size	Document Number: LA-L1551PR02		Rev: 0.2
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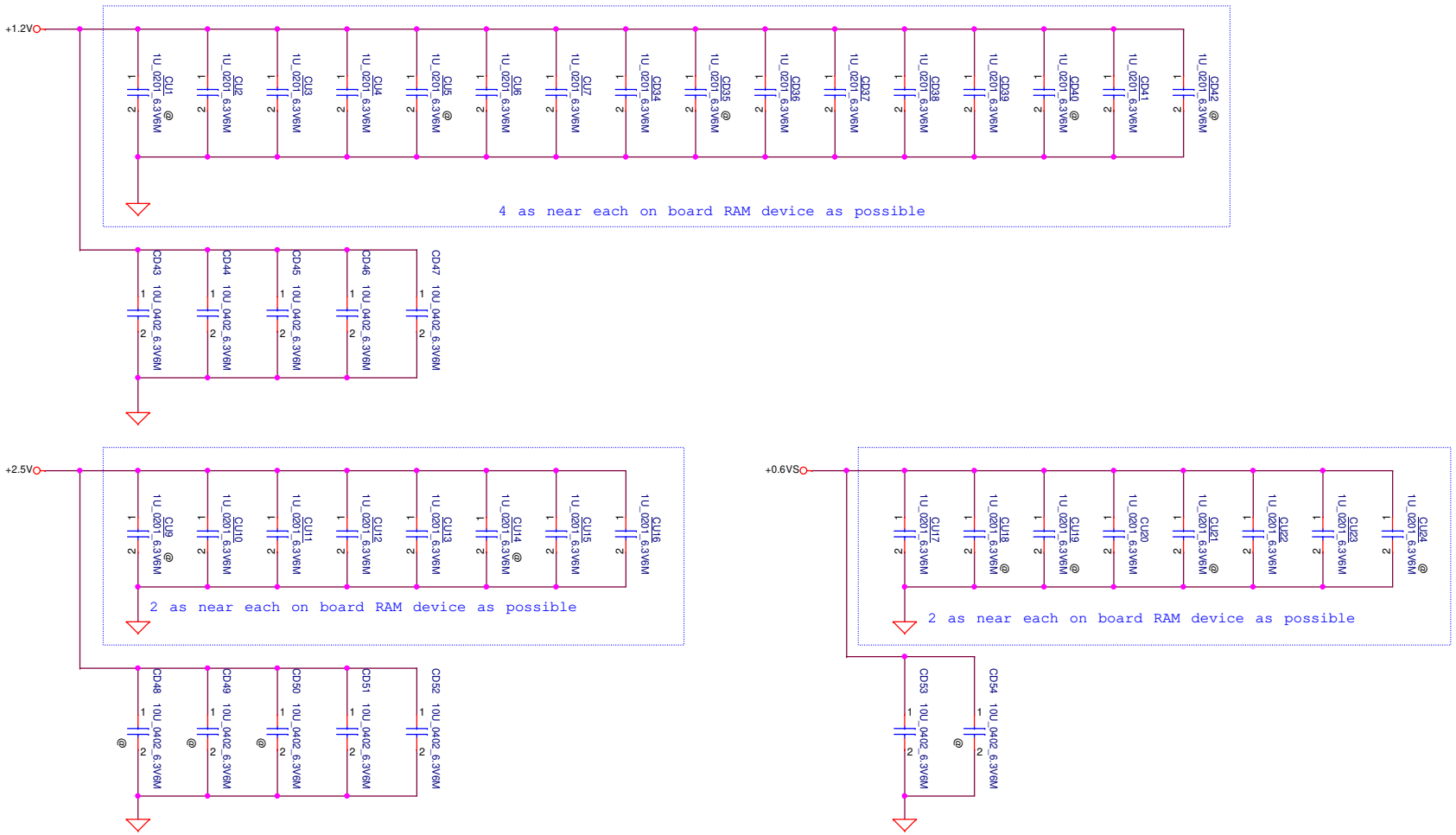

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Title: **DDR4 ON BOARD RAM Decoupling**

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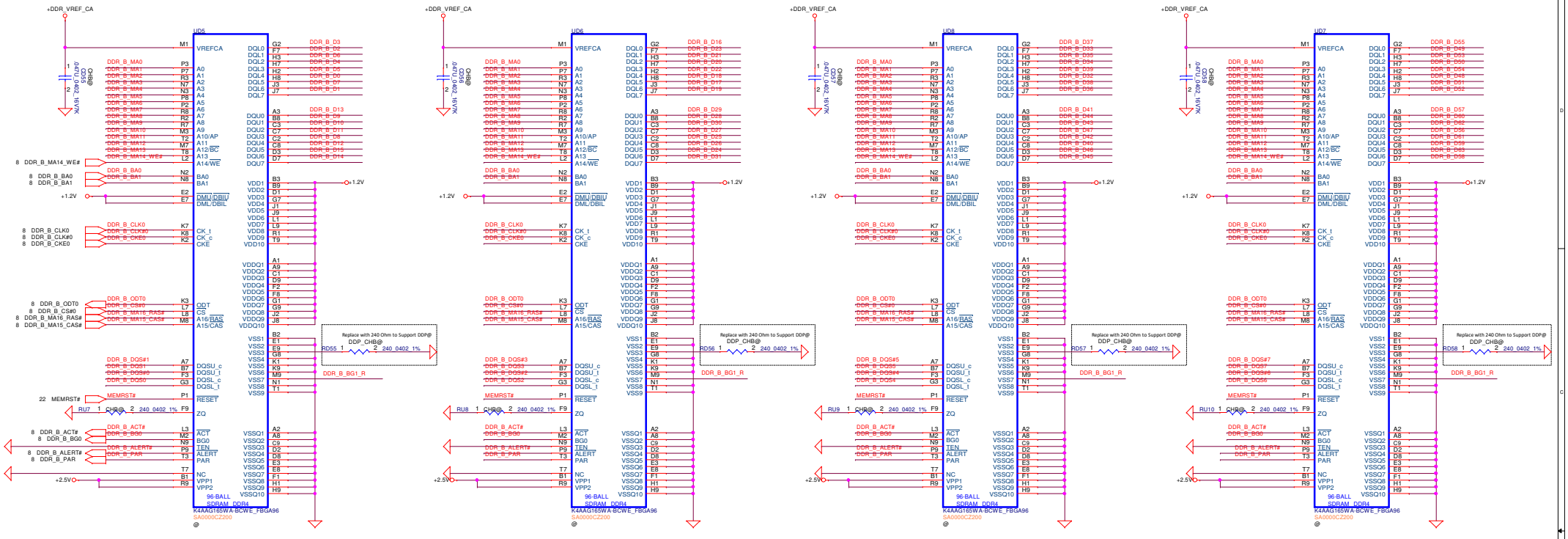

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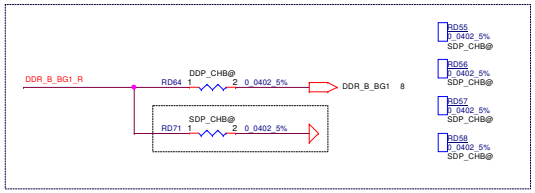
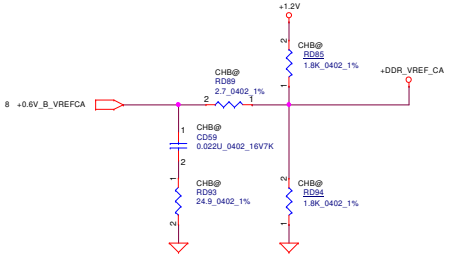
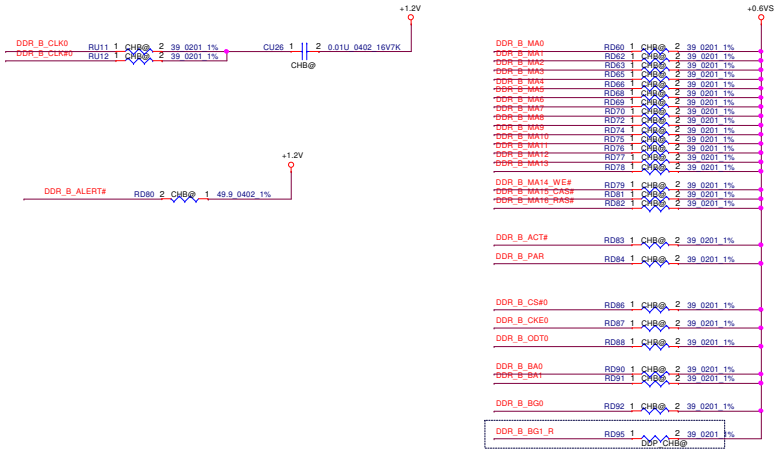
8 DDR_B_DQS#[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_D[0..63]

Co-lay for SDP / DDP Memory DIE





CLOCK TERMINATION



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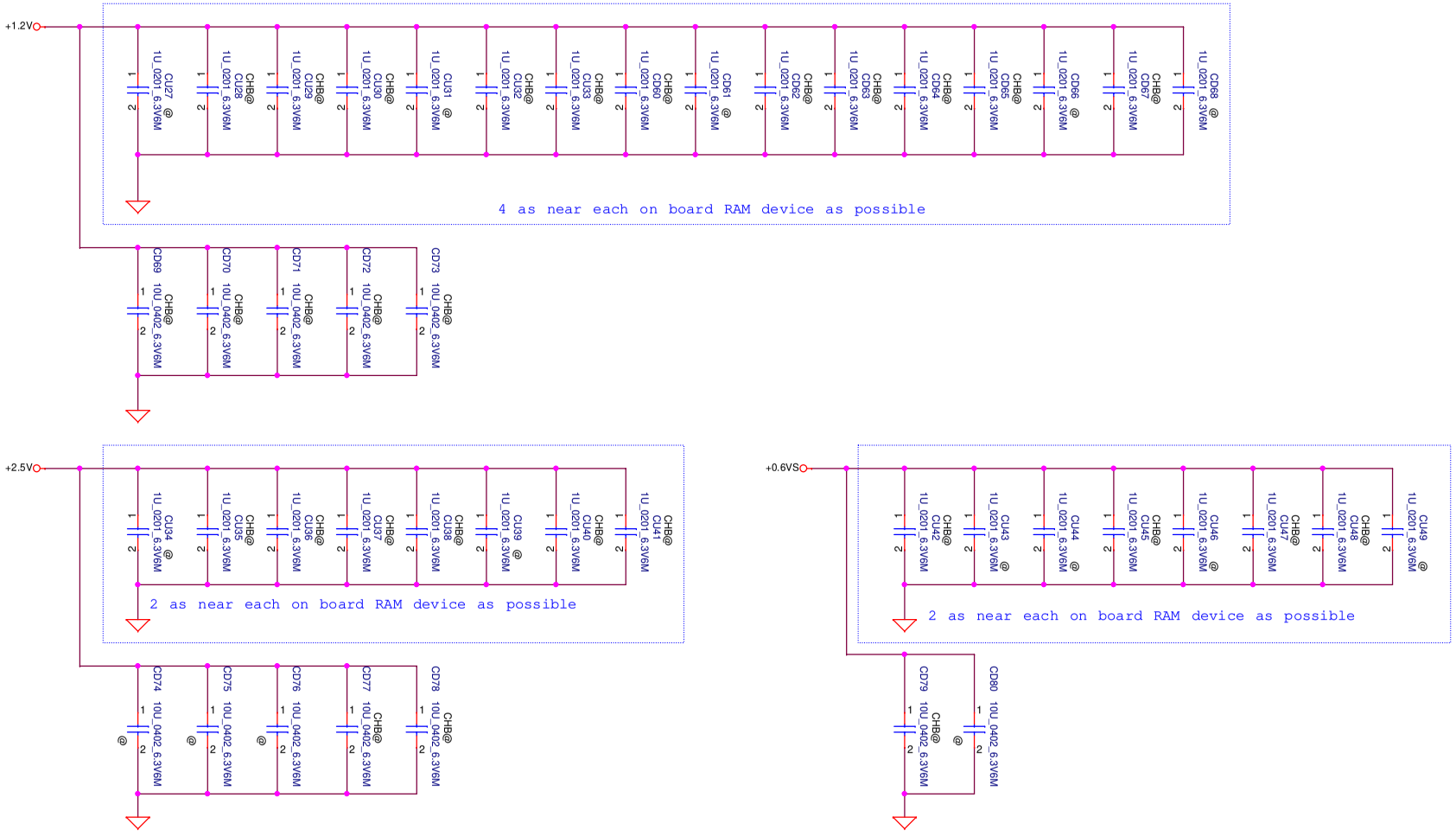

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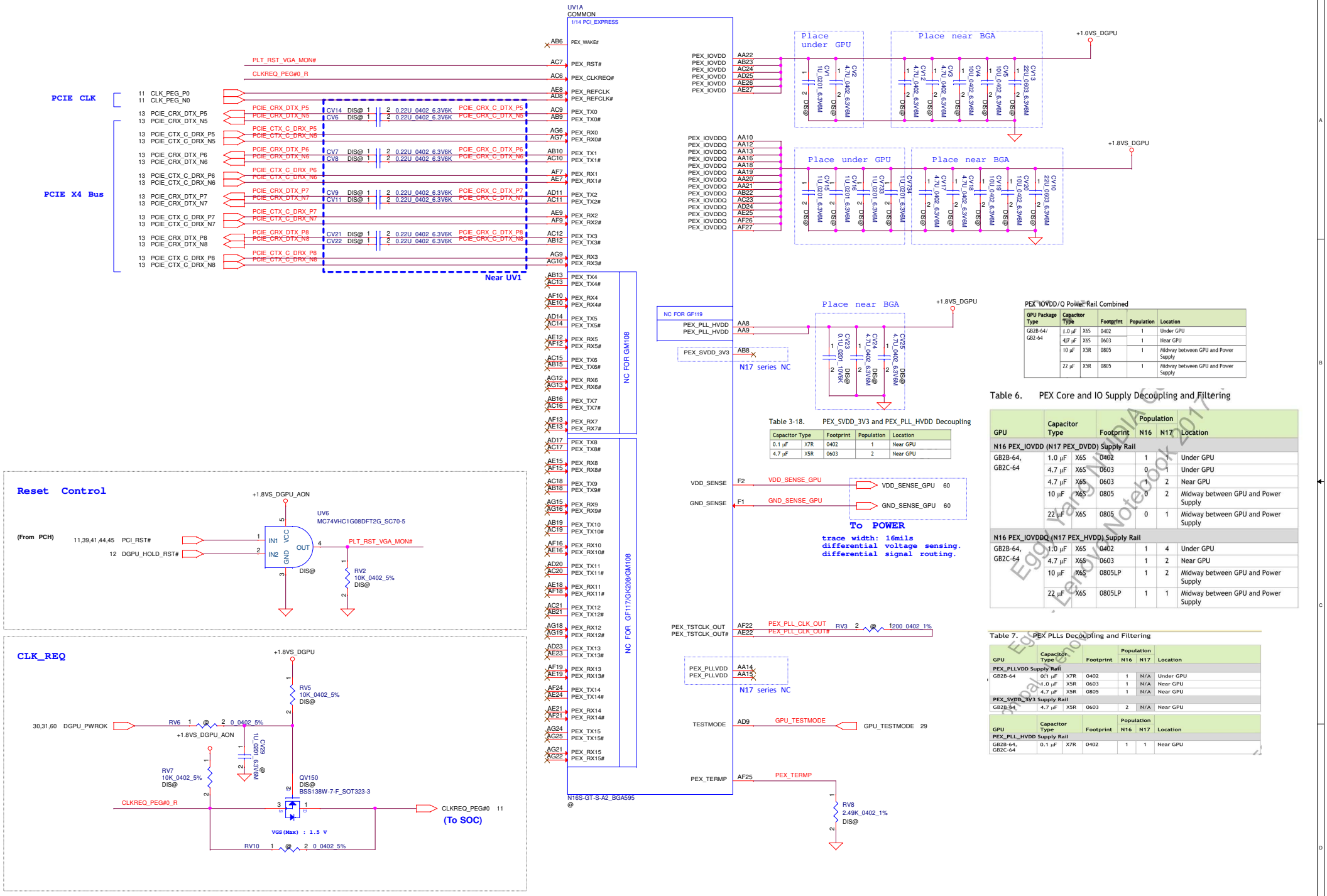

PEX_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply

Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 µF	X7R	0402	1	Near GPU
4.7 µF	X5R	0603	2	Near GPU

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1		Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

Table 7. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
PEX_PLLVDD Supply Rail						
GB2B-64	0.1 µF	X7R	0402	1	N/A	Under GPU
	1.0 µF	X5R	0603	1	N/A	Near GPU
	4.7 µF	X5R	0805	1	N/A	Near GPU
PEX_SVDD_3V3 Supply Rail						
GB2B-64	4.7 µF	X5R	0603	2	N/A	Near GPU

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

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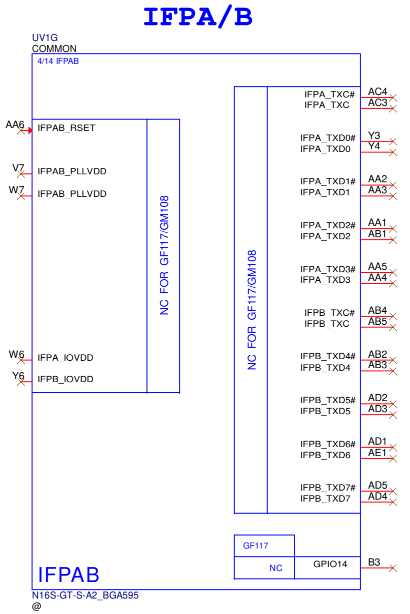
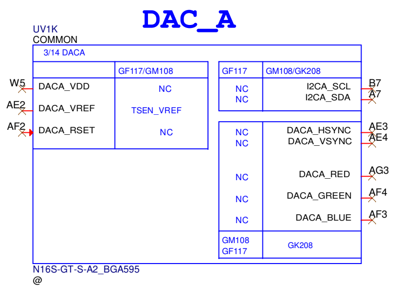
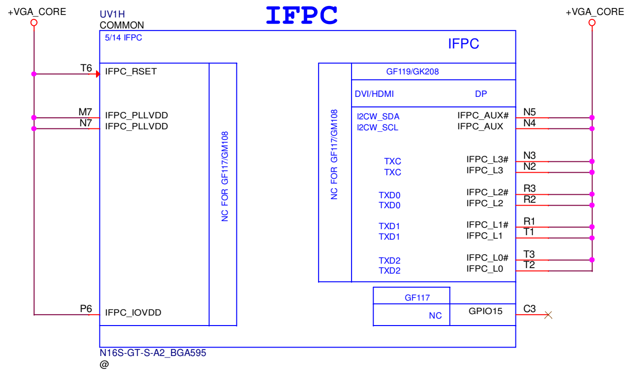

IFPA/B
UV1G
COMMON
4/14 IFPAB
IFPAB_RSET
IFPAB_PLLVDD
IFPAB_PLLVDD
IFPA_IOVDD
IFPB_IOVDD
NC FOR GF117/GM108
IFPA_TXC#
IFPA_TXC
IFPA_TXD0#
IFPA_TXD0
IFPA_TXD1#
IFPA_TXD1
IFPA_TXD2#
IFPA_TXD2
IFPA_TXD3#
IFPA_TXD3
IFPB_TXC#
IFPB_TXC
IFPB_TXD4#
IFPB_TXD4
IFPB_TXD5#
IFPB_TXD5
IFPB_TXD6#
IFPB_TXD6
IFPB_TXD7#
IFPB_TXD7
GF117
NC
GPIO14
IFPAB
N16S-GT-S-A2_BGA595

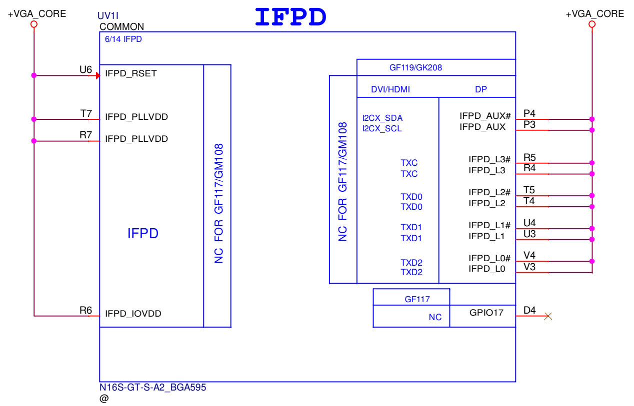


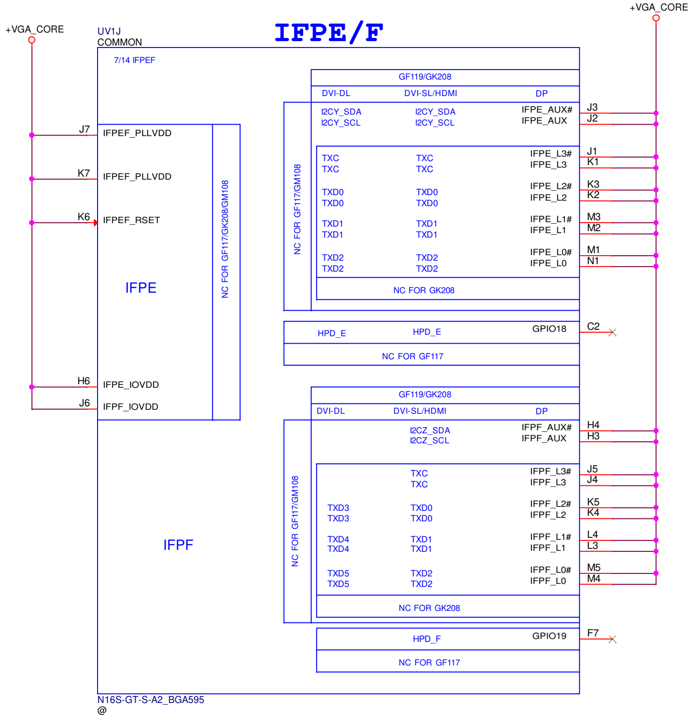

+VGA_CORE
IFPC
UV1H
COMMON
5/14 IFPC
IFPC_RSET
IFPC_PLLVDD
IFPC_PLLVDD
IFPC_IOVDD
NC FOR GF117/GM108
GF119/GK208
DVI/HDMI
DP
I2CW_SDA
I2CW_SCL
IFPC_AUX#
IFPC_AUX
IFPC_L3#
IFPC_L3
IFPC_L2#
IFPC_L2
IFPC_L1#
IFPC_L1
IFPC_L0#
IFPC_L0
GF117
NC
GPIO15
N16S-GT-S-A2_BGA595

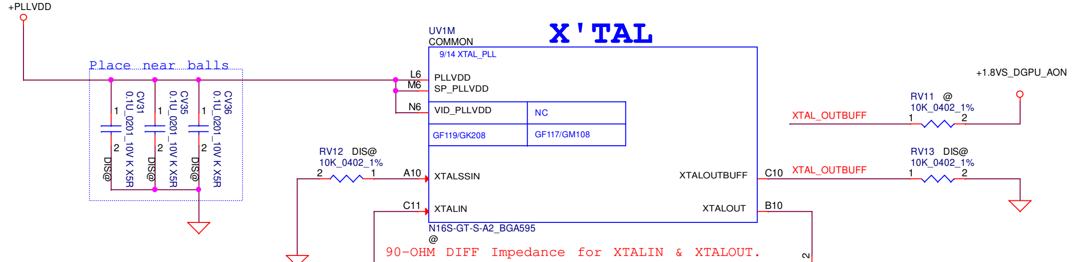
Note:
IFPC/D/E/F interface are XVDDs pin for N17S GPU, and connect them to NVVDD power for improving NVVDD power rail routing

Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type		Footprint	Population N16	Population N17	Location
PLLVDD (N17: XS_PLLVDD) Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Under GPU
	22 µF	X5R	0805	1	0	Near GPU
	Bead Type					
	L2=30 Ω (ESR=0.05 Ω)		0402	1	0	Near GPU
SP_PLLVDD and VID_PLLVDD Combined Supply Rails						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	2	Under GPU
	10 µF	X5R	0603	1	0	Near GPU
	47 µF	X5R	0805	1	0	Near GPU
	Bead Type					
	L2=300 Ω (ESR=0.2 Ω)		0603	1	0	Near GPU


+VGA_CORE
IFPD
UV1I
COMMON
6/14 IFPD
IFPD_RSET
IFPD_PLLVDD
IFPD_PLLVDD
IFPD_IOVDD
NC FOR GF117/GM108
GF119/GK208
DVI/HDMI
DP
I2CX_SDA
I2CX_SCL
IFPD_AUX#
IFPD_AUX
IFPD_L3#
IFPD_L3
IFPD_L2#
IFPD_L2
IFPD_L1#
IFPD_L1
IFPD_L0#
IFPD_L0
GF117
NC
GPIO17
N16S-GT-S-A2_BGA595


+VGA_CORE
IFPE/F
UV1J
COMMON
7/14 IFPEF
IFPEF_PLLVDD
IFPEF_PLLVDD
IFPEF_RSET
IFPE
IFPE_IOVDD
IFPF_IOVDD
IFPF
NC FOR GF117/GK208/GM108
GF119/GK208
DVI-DL
DVI-SL/HDMI
DP
I2CY_SDA
I2CY_SCL
IFPE_AUX#
IFPE_AUX
IFPE_L3#
IFPE_L3
IFPE_L2#
IFPE_L2
IFPE_L1#
IFPE_L1
IFPE_L0#
IFPE_L0
NC FOR GK208
HPD_E
GPIO18
NC FOR GF117
I2CZ_SDA
I2CZ_SCL
IFPF_AUX#
IFPF_AUX
IFPF_L3#
IFPF_L3
IFPF_L2#
IFPF_L2
IFPF_L1#
IFPF_L1
IFPF_L0#
IFPF_L0
HPD_F
GPIO19
N16S-GT-S-A2_BGA595


+PLLVDD
Place near balls
CV31 0.1U_0201_10V K X5R
CV35 0.1U_0201_10V K X5R
CV36 0.1U_0201_10V K X5R
X'TAL
UV1M
COMMON
9/14 XTAL_PLL
PLLVDD
SP_PLLVDD
VID_PLLVDD
GF119/GK208
GF117/GM108
XTALSSIN
XTALIN
XTALOUTBUFF
XTALOUT
XTAL_OUTBUFF
RV11 @ 10K_0402_1%
RV12 DIS@ 10K_0402_1%
RV13 DIS@ 10K_0402_1%
+1.8VS_DGPU_AON
N16S-GT-S-A2_BGA595

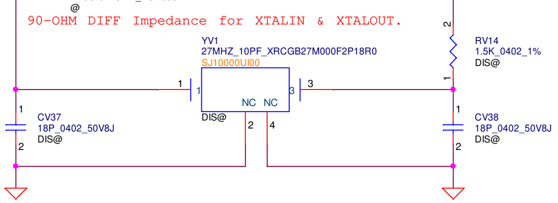


Table 3-33. SP_PLLVDD Power Rail Filtering [1]

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2-64, GB2B-64, GB4B-128, GB3B-256	SP_PLLVDD (+ VID_PLLVDD)[1]	0.1 µF	X7R	0402	1 per ball	Under GPU
		10 µF	X5R	0603	1	Near GPU
		47 µF	X5R	0805	1	Near GPU
		Bead Type				
		300 Ω (ESR=0.2 Ω)		0603	1	Near GPU

Note:
1. SP_PLLVDD and VID_PLLVDD power rails can be combined for customers who either do not use VGA display or uses VGA display with maximum resolution lower than 1024 x 768 with a 240 Hz refresh rate.

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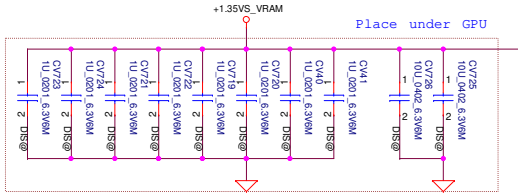
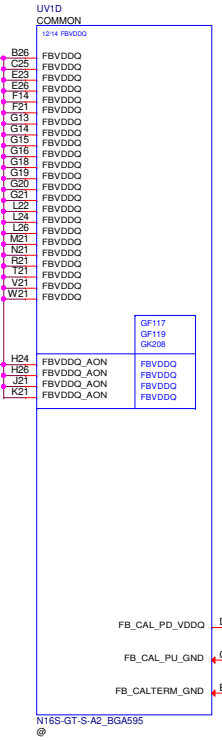
GPU_Decoupling CAPs @ Power Page





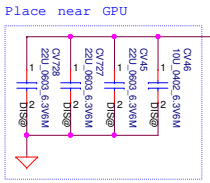
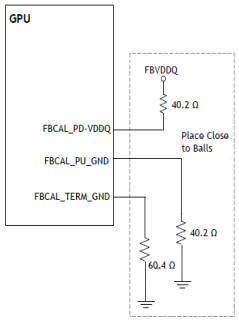
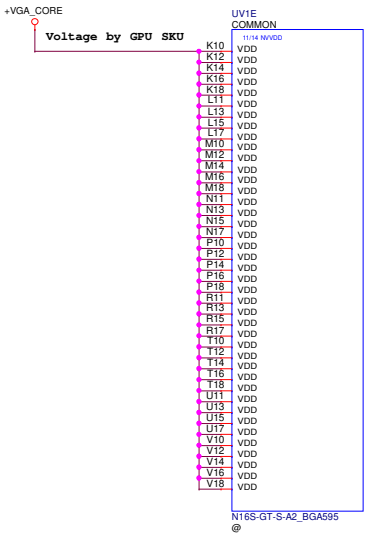


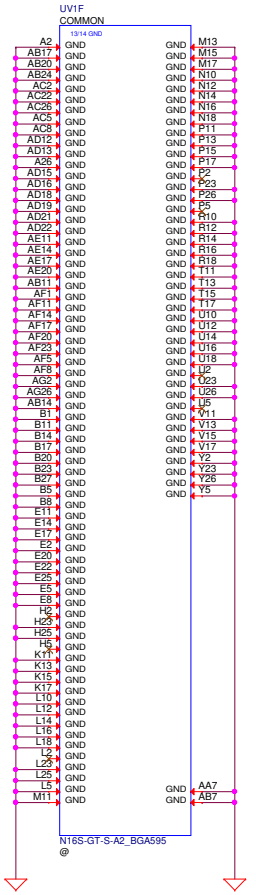
Table 4. Frame Buffer Core and IO Decoupling and Filtering

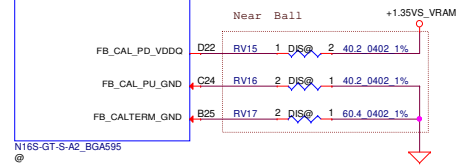
GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R 0402	2	0	Under GPU
	1 µF	X7R 0603	2	8	Under GPU
	4.7 µF	X6S 0603	2	0	Under GPU
	10 µF	X6S 0603	0	2	Under GPU
	10 µF	X6S 0603	1	1	Near GPU
	22 µF	X6S 0603W	1	3	Near GPU



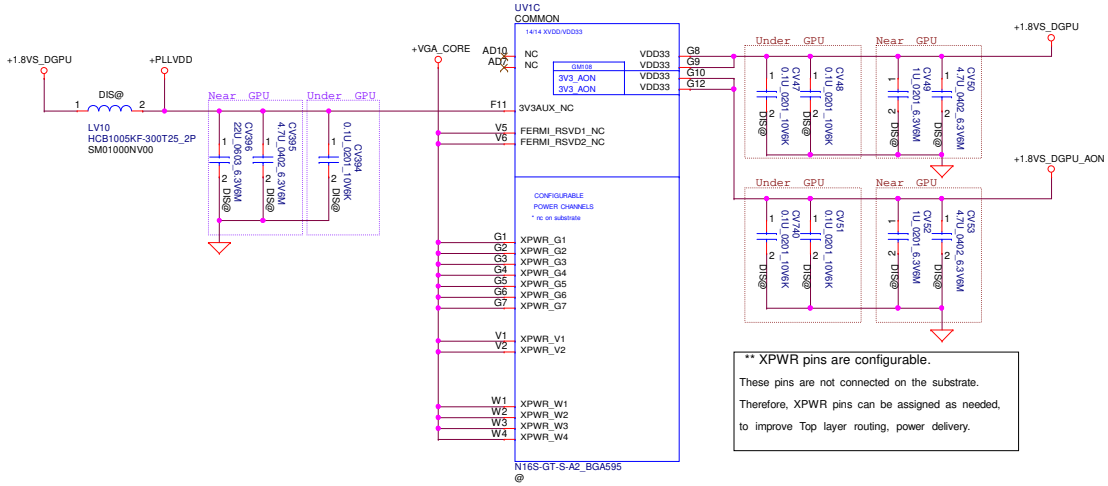
Note: Use only 1% resistors for driver calibration







GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/ GB2-64 GDDR5	0.1 µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU



** XPWR pins are configurable.

These pins are not connected on the substrate.

Therefore, XPWR pins can be assigned as needed, to improve Top layer routing, power delivery.

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2-64 GB2B-64 GB4B-128 GB3B-256	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU
GB2-64 GB2B-64 GB4B-128 GB3B-256	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

NC (N17: GPCPLL_AVDD) Supply Rail						
GB2C-64	0.1 µF	X7R	0402	N/A	1	Under GPU
	4.7 µF	X6S	0603	N/A	1	Near GPU
	22 µF	X6S	0805	N/A	1	Near GPU
	Bead Type					
	L=30 Ω (ESR=0.010 Ω)		0603	N/A	1	Near GPU

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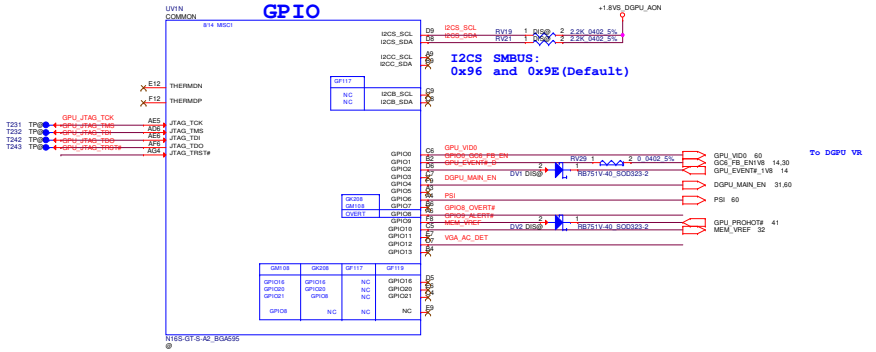
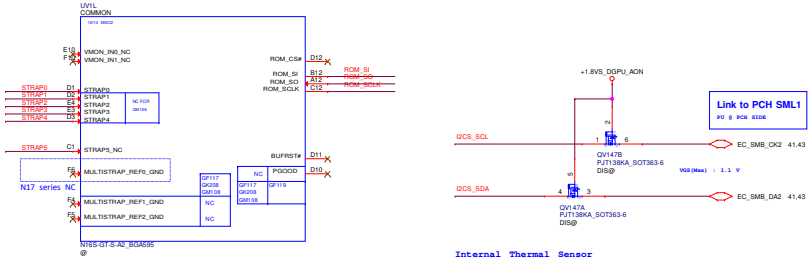




10.2.1 Unconnected Signals (NC)

Do not route unused I²C signals on the PCB in order to protect the GPU from outside ESD risk. If unused traces are routed, the signals should be pulled down to ground with 1.8 kΩ resistors.

10.2.2 I²CS Slave Address

N16x GPUs use FCS slave address 0x96h for NVIDIA internal testing. I²C address 0x96h must not be used by other I²C devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter 15 (Straps) for a list of useful FCS Slave addresses can be used with SMB_ALT_ADDR strapping.

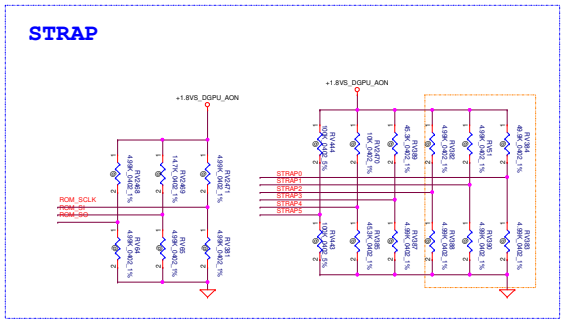
16.3.3 Internal Thermal Sensor Interface

The internal thermal sensor can be accessed through the FCS interface as described in the I²C chapter. This interface is compliant with the System Management Bus (SMBus) Specification (Version 2.0). The interface supports PEC and SMBus Timeout as well as Read Byte and Read Byte with PEC. Writes to the internal thermal sensor registers through the FCS interface by the system is not supported. The default port address to access the internal thermal sensor over the FCS is 0x9E. Table 16-1 describes the byte-wise register accessible through the FCS interface.

Ball Location	H16/GB2B-64 Ball Name	H17/GB2C-64 Ball Name	What to do for an H17/GB2C-64 GPU on an H16/GB2B-64 GPU board
C24	FB_CAL_GHD	FB_CAL_PU_GHD	Name change only
B25	FB_CAL_TERM	FB_CAL_TERM_GHD	Name change only
D22	FB_CAL_VDDQ	FB_CAL_PD_VDDQ	Name change only
H24	FBVDDQ_AOH	FVBDDQ	Name change only
H26	FBVDDQ_AOH	FVBDDQ	Name change only
J21	FBVDDQ_AOH	FVBDDQ	Name change only
K21	FBVDDQ_AOH	FVBDDQ	Name change only
IO Supply			
G10	3V3_AOH	1V8_AOH	Note power supply change
G12	3V3_AOH	1V8_AOH	Note power supply change
G8	3V3_MAIH	VDD18	Note power supply change
G9	3V3_MAIH	VDD18	Note power supply change
Core Supply			
L11	VDD	VDDS	Name change only
L17	VDD	VDDS	"
M14	VDD	VDDS	"
P10	VDD	VDDS	"
P12	VDD	VDDS	"
P16	VDD	VDDS	"
P18	VDD	VDDS	"
T14	VDD	VDDS	"
U11	VDD	VDDS	"
U17	VDD	VDDS	"
F4	MULTI_STRAP_REF1_GHD	VDDS_SENSE	Leave unconnected
F3	FB_CLAMP	GNDS_SENSE	Leave unconnected
Straps			
C1	NC	STRAP5	Add necessary pull-up and pull-down resistor(s)
F6	MULTI_STRAP_REF0_GHD	NC	Depopulate pull-down resistor to GND
F5	MULTI_STRAP_REF2_GHD	NC	

Table 12-2. GB2B-64 and GB4B-128 GPIO Description

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	GC6_FB_EN	O	FB Enable for GC6 2.0, Open Source	10 kΩ pull-down
GPIO1	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDDQ Boot voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 kΩ pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	100 kΩ pull-down
GPIO4	LCD_BLEH	O	Panel Backlight Enable	100 kΩ pull-down
GPIO5	3V3_MAIH_EH	O	GPU power sequencing for GC6 2.0, Open Drain	10 kΩ pull-up to 3V3_AOH
GPIO6	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10 kΩ pull-up to 3V3_AOH
GPIO7	3DVision	O	3D Vision L/R signal	100 kΩ pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset monitor	10 kΩ pull-up to 3V3_AOH unless actively drives
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert, Open Drain	10 kΩ pull-up to 3V3_AOH
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	PWM_VID	O	GPU core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 3V3_AOH
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AOH to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	FRAME_LOCK#	I	Active Low Frame Lock, Open Drain	10 kΩ pull-up to 3V3_AOH; Not available for GB2B-64
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IFPB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control, Open Drain	10 kΩ pull-up to 3V3_AOH
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AOH



N17S-G0/G2 VRAM Strap

Table 6. N17S-G0/G2/G3/G4 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDDQ	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x0	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FC-HC25	C-die	0x3	8 Gbps	N/A	Full	Post-production ready

Notes:
1. For N17S-G0/G2/G3/G4, the maximum allowable memory case temperature is 85 °C.
2. N17S-G0/G2 running at 1.0 GHz (without intent to limit 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N17S-G1.

RAM_CFG	STRAP2	STRAP1	STRAP0
0x9 (LML) M2G	RV388 100K_0402_5% N17_M2G@	RV51 100K_0402_5% N17_M2G@ RV390 100K_0402_5% N17_M2G@	RV383 100K_0402_5% N17_M2G@
0xA (LMH) H2G	RV388 100K_0402_5% N17_H2G@	RV51 100K_0402_5% N17_H2G@ RV390 100K_0402_5% N17_H2G@	RV384 100K_0402_5% N17_H2G@
0x3 (LHH) S2G	RV388 100K_0402_5% N17_S2G@	RV51 100K_0402_5% N17_S2G@	RV384 100K_0402_5% N17_S2G@

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
STRAP2	STRAP1	STRAP0	
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1

N17 Strap

ROM_SO	ROM_SI	ROM_SCLK	STRAP5	STRAP4	STRAP3
RV2468 DIS@ 100K_0402_5%	RV2469 DIS@ 100K_0402_5%	RV2471 DIS@ 100K_0402_5% RV381 DIS@ 100K_0402_5%	RV443 DIS@ 100K_0402_5%	RV385 DIS@ 100K_0402_5%	RV387 DIS@ 100K_0402_5%

Note: The ternary strap pins listed in the Strap Pins columns must be pulled to one of three voltage levels. "L" means Low level (GND). "M" means middle level (0.9V). "H" means High level (1.8V).

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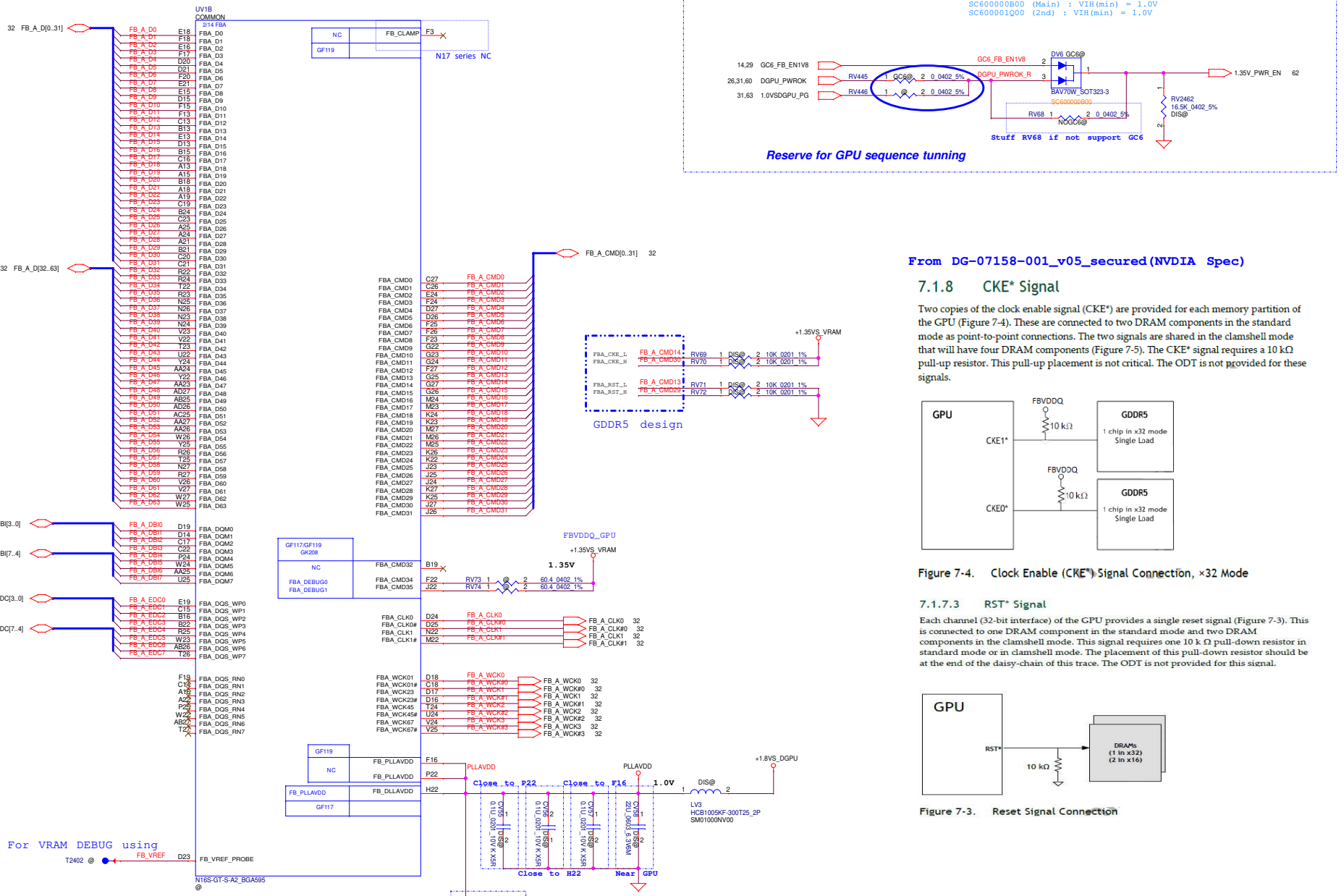

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2-64/ GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

From DG-07158-001_v05_secured(NVDIA Spec)

7.1.8 CKE* Signal

Two copies of the clock enable signal (CKE*) are provided for each memory partition of the GPU (Figure 7-4). These are connected to two DRAM components in the standard mode as point-to-point connections. The two signals are shared in the clamshell mode that will have four DRAM components (Figure 7-5). The CKE* signal requires a 10 kΩ pull-up resistor. This pull-up placement is not critical. The ODT is not provided for these signals.

Figure 7-4. Clock Enable (CKE*) Signal Connection, ×32 Mode

7.1.7.3 RST* Signal

Each channel (32-bit interface) of the GPU provides a single reset signal (Figure 7-3). This is connected to one DRAM component in the standard mode and two DRAM components in the clamshell mode. This signal requires one 10 k Ω pull-down resistor in standard mode or in clamshell mode. The placement of this pull-down resistor should be at the end of the daisy-chain of this trace. The ODT is not provided for this signal.

Figure 7-3. Reset Signal Connection

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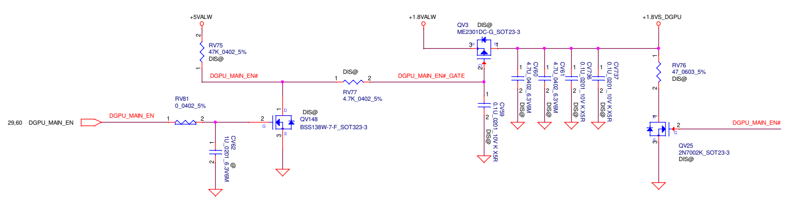
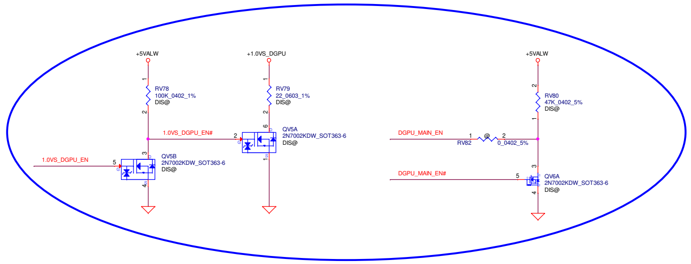
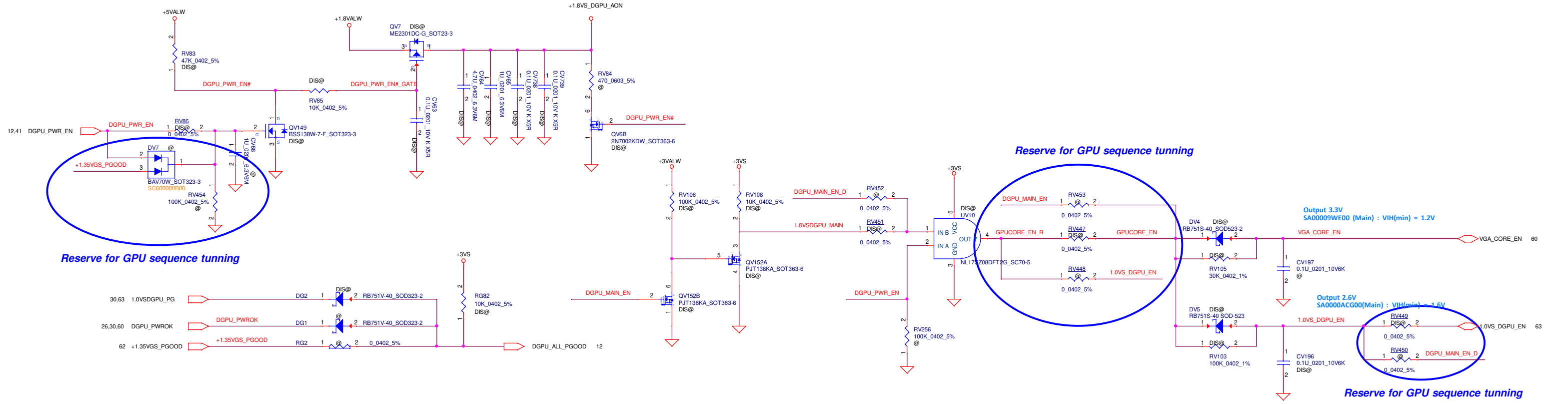
+1.8VALW to +1.8VS_DGPU



Discharger



+1.8VALW to +1.8VS_DGPU_AON



+5VALW
+1.8VALW
+1.8VS_DGPU_AON
QV7 DIS@ ME2301DC-G_SOT23-3
RV83 47K_0402_5% DIS@
RV84 470_0603_5%
DGPU_PWR_EN#
DGPU_PWR_EN#_GATE
RV85 10K_0402_5%
12,41 DGPU_PWR_EN
QV149 BSS138W-7-F_SOT323-3 DIS@
QV6B 2N7002KDW_SOT363-6 DIS@
DV7
BAV70W_SOT323-3
+1.35VGS_PGOOD
RV454 100K_0402_5%
Reserve for GPU sequence tunning
+3VALW
+3VS
RV106 100K_0402_5% DIS@
RV108 10K_0402_5% DIS@
DGPU_MAIN_EN_D
1.8VSDGPU_MAIN
QV152A PJT138KA_SOT363-6 DIS@
QV152B PJT138KA_SOT363-6 DIS@
DGPU_MAIN_EN
DGPU_PWR_EN
RV256 100K_0402_5%
UV10 NL17SZ08DFT2G_SC70-5
Reserve for GPU sequence tunning
GPUCORE_EN_R
GPUCORE_EN
1.0VS_DGPU_EN
DV4 DIS@ RB751S-40_SOD523-2
RV105 30K_0402_1%
CV197 0.1U_0201_10V6K
Output 3.3V
SA00009WE00 (Main) : VIH(min) = 1.2V
VGA_CORE_EN
VGA_CORE_EN 60
Output 2.6V
SA0000ACG00(Main) : VIH(min) = 1.6V
DV5 DIS@ RB751S-40 SOD-523
RV103 100K_0402_1%
CV196 0.1U_0201_10V6K DIS@
1.0VS_DGPU_EN 63
Reserve for GPU sequence tunning
30,63 1.0VSDGPU_PG
26,30,60 DGPU_PWROK
62 +1.35VGS_PGOOD
DG2 RB751V-40_SOD323-2
DG1 RB751V-40_SOD323-2
RG2 0_0402_5%
RG82 10K_0402_5% DIS@
DGPU_ALL_PGOOD 12

Table 5. EDP-Continuous [3]

Products	VRAM Type	GPU Core	GPU FBIO		FB Total [1, 5]		1.05V Total [2]	3.3V Total
		–	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]	3.3V [4]
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	19.0	–	2.0	–	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5	26.5	–	2.0	–	4.2	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
N16 3V3_MAIN (N17 VDD18) Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	2	Under GPU
	1.0 µF	X6S	0603	1	1	Near GPU
	4.7 µF	X6S	0603	1	1	Near GPU
N16 3V3_AON (N17 1V8_AON) Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	2	Under GPU
	1.0 µF	X6S	0603	1	1	Near GPU
	4.7 µF	X6S	0603	1	1	Near GPU

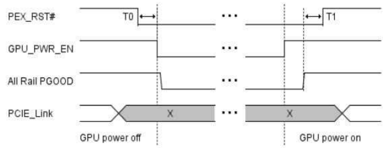
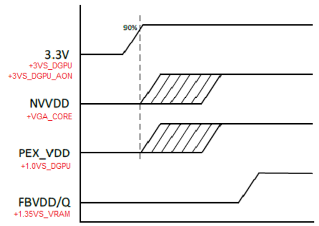


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

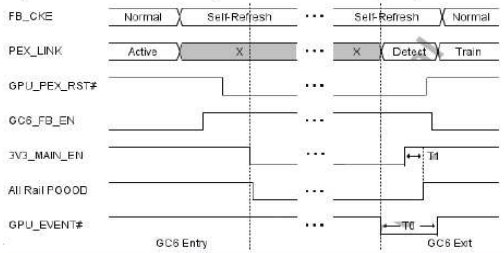
Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms



Note:

- 3.3V includes all rails powered at 3.3V; PEX_VDD includes all rails that are shared on 1.05V/1.0V
- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2 ms.

Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram



Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Note:

- ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in GC6 for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.

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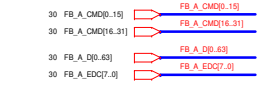
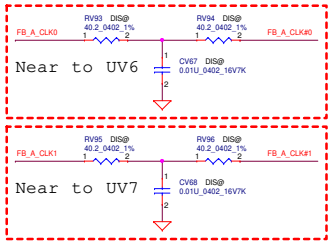
VRAM Memory Partition A

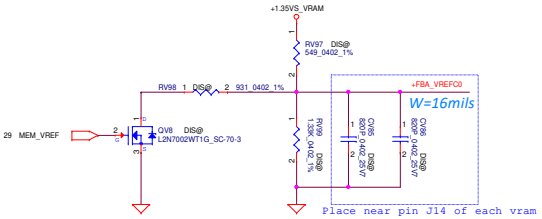
Table 7-4. GDDR5 Mode H Mapping

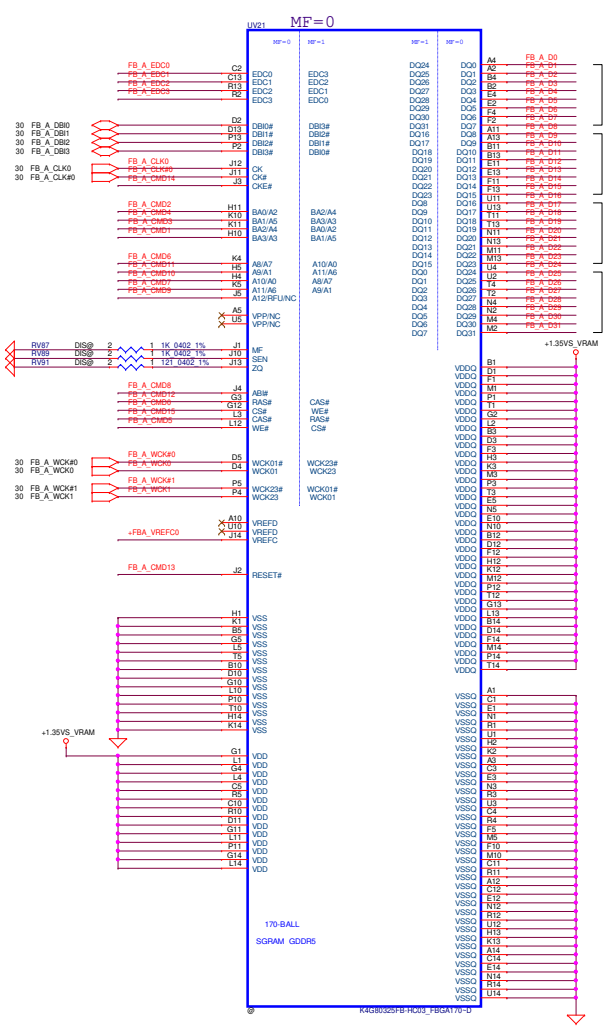
GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	Channel 0 & 1		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG0[2]		
CMD35	DEBUG1[2]		

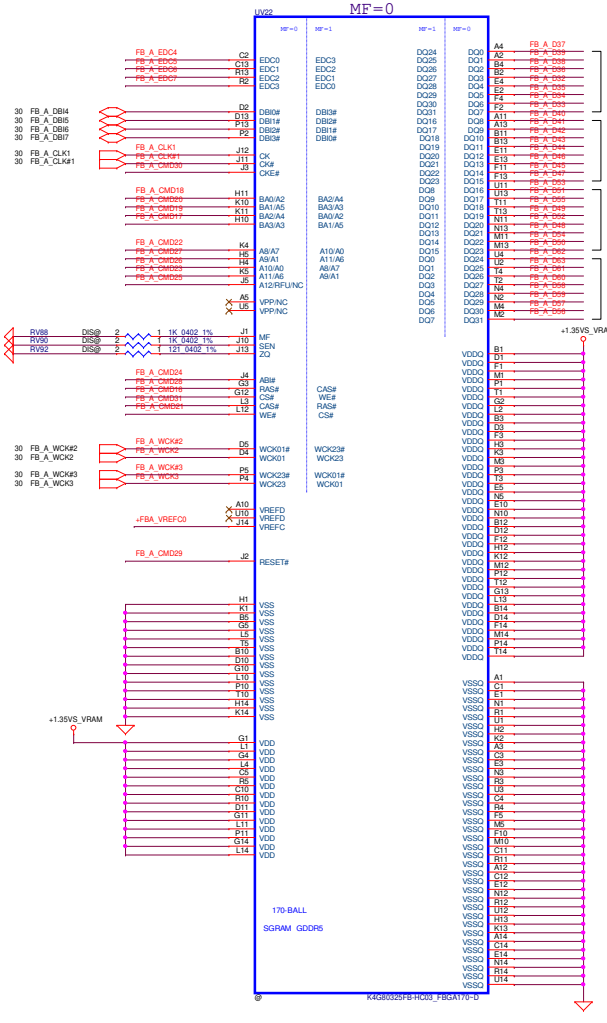
Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins not connected to DRAM, see section 7.1.13.

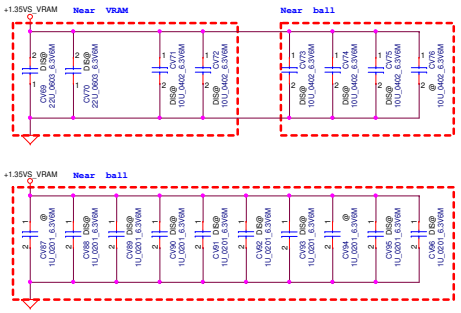


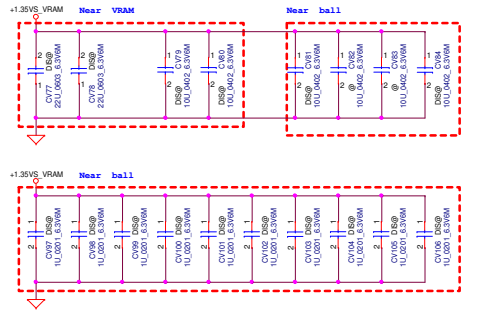












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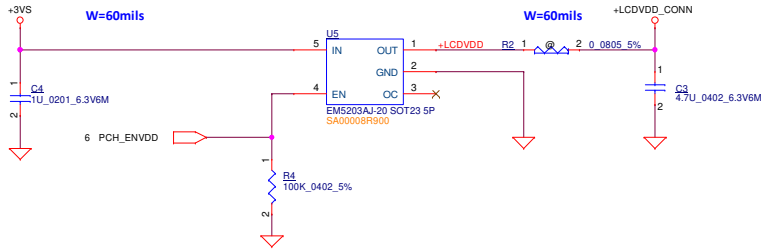
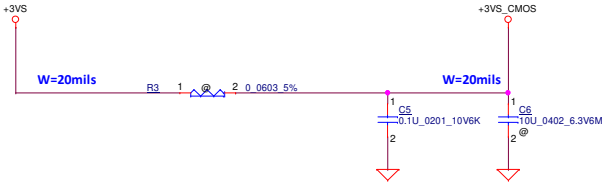
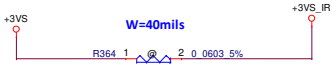
LCD POWER SWITCH



CAMERA POWER CIRCUIT



IR POWER



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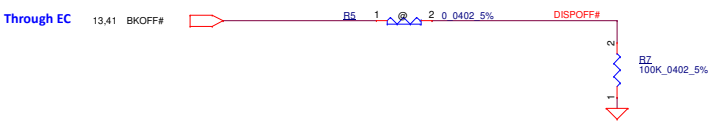

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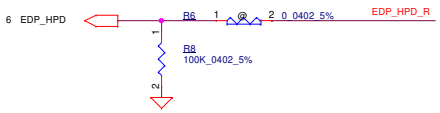

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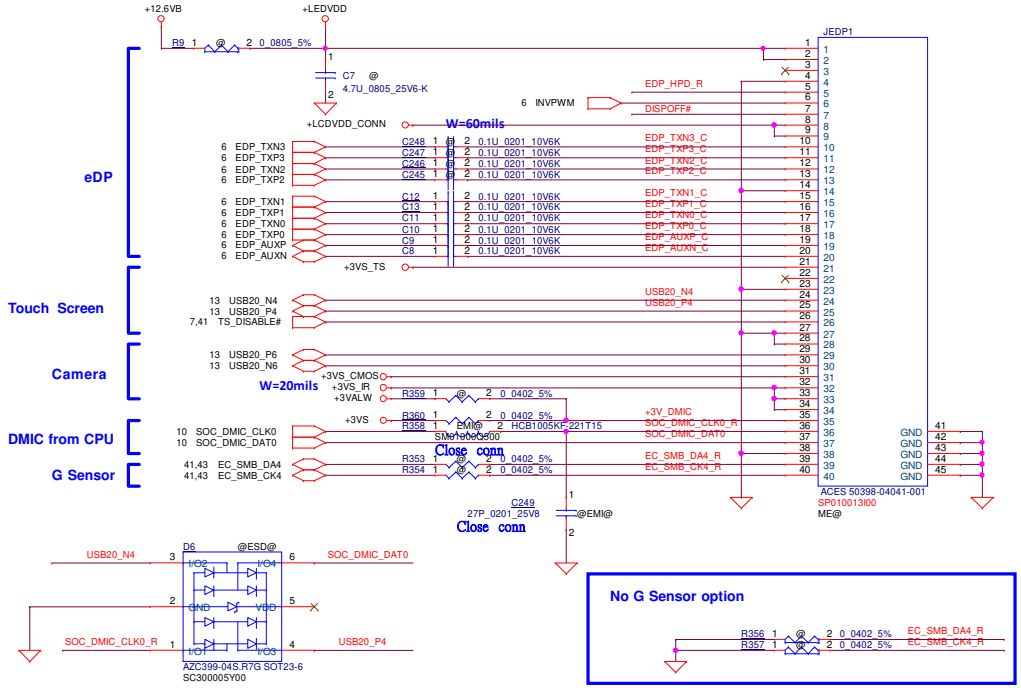

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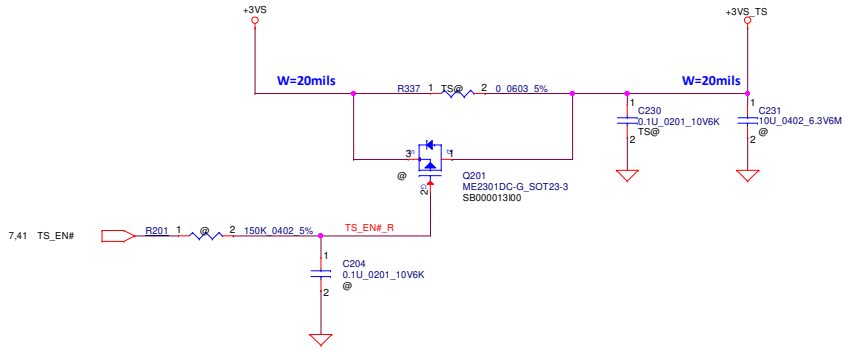

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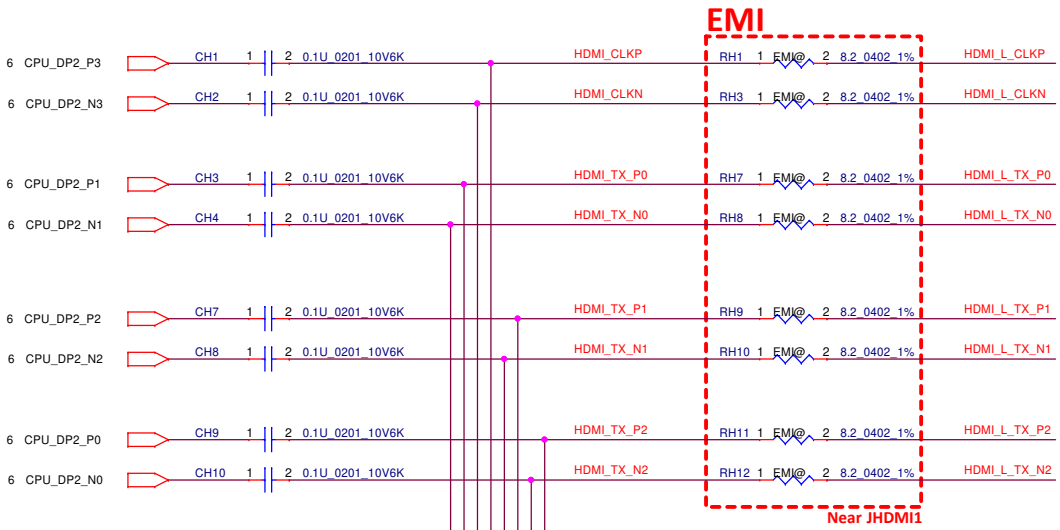
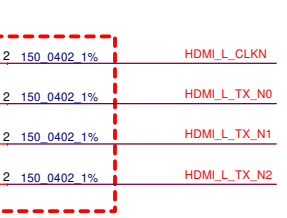
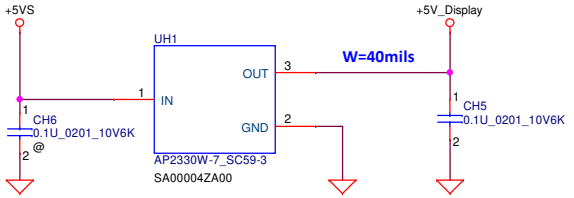
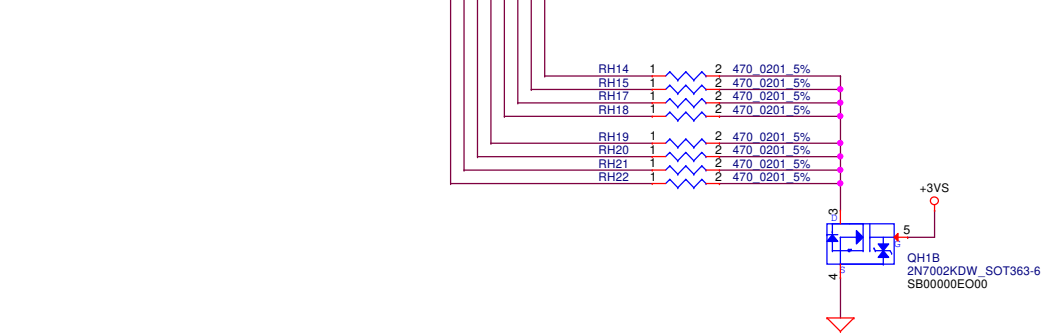
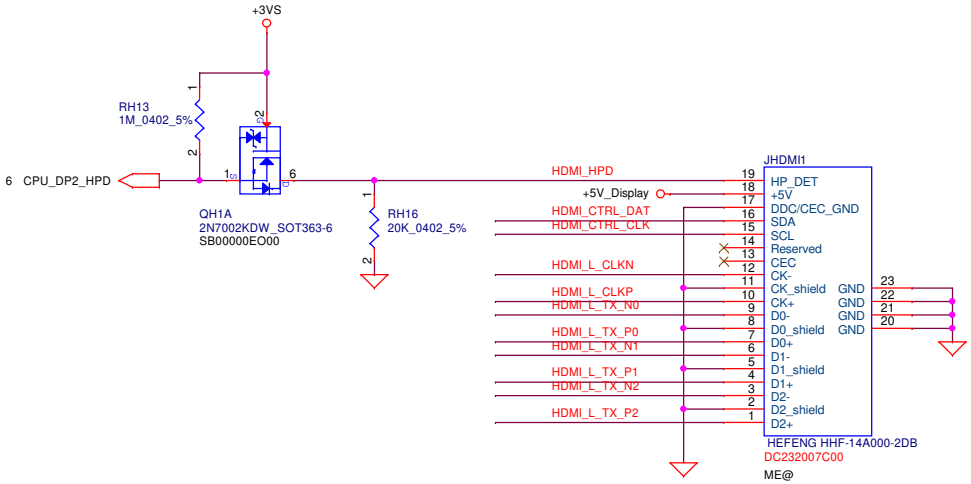
HDMI

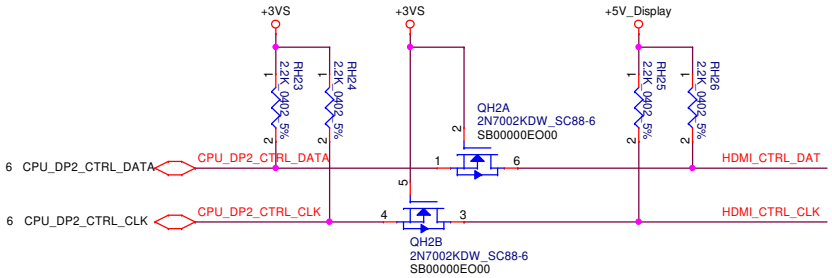


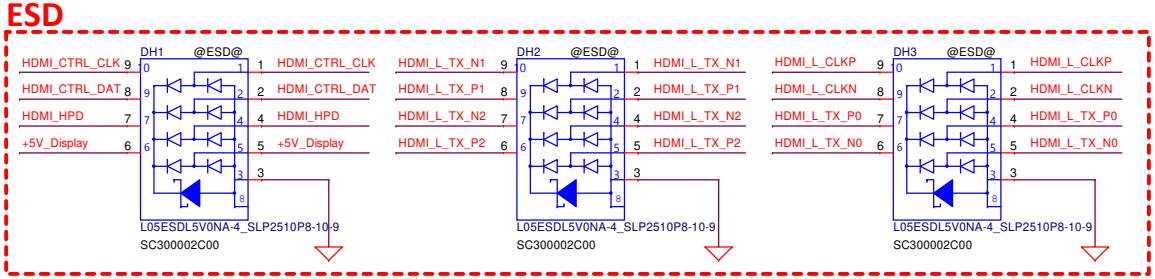


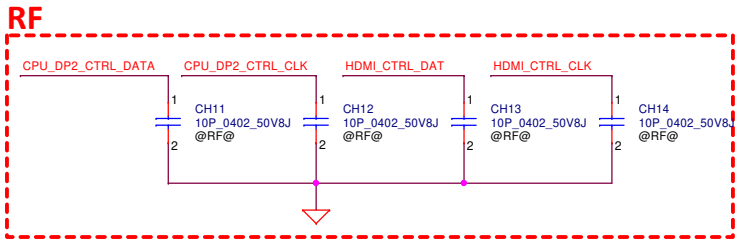












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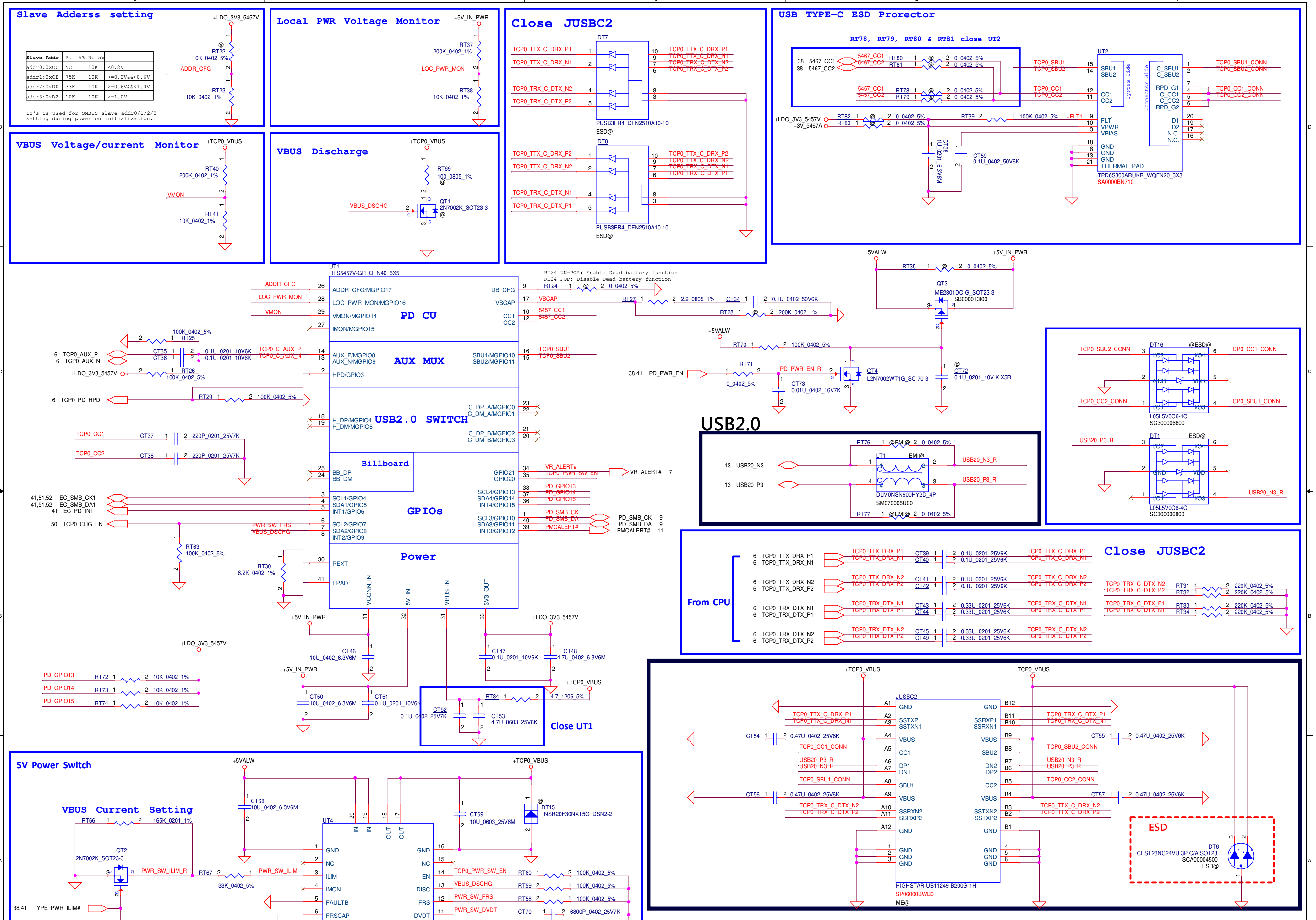
Slave Adderss setting
Slave Addr | Ra 5% | Rb 5%
addr0:0xCC | NC | 10K | <0.2V
addr1:0xCE | 75K | 10K | >=0.2V&<0.6V
addr2:0xD0 | 33K | 10K | >=0.6V&<1.0V
addr3:0xD2 | 10K | 10K | >=1.0V
It's is used for SMBUS slave addr0/1/2/3 setting during power on initialization.
Local PWR Voltage Monitor
Close JUSBC2
USB TYPE-C ESD Prorector
RT78, RT79, RT80 & RT81 close UT2
VBUS Voltage/current Monitor
VBUS Discharge
UT1
RTS5457V-GR_QFN40_5X5
PD CU
AUX MUX
USB2.0 SWITCH
Billboard
GPIOs
Power
RT24 UN-POP: Enable Dead battery function
RT24 POP: Disable Dead battery function
USB2.0
From CPU
Close JUSBC2
Close UT1
5V Power Switch
VBUS Current Setting
UT4
DPS1155FEA_V-QFN3025-20_3X2P5
JUSBC2
HIGHSTAR UB11249-B200G-1H
SP06000BWB0
ESD
CEST23NC24VU 3P C/A SOT23
TPD6S300ARUKR_WQFN20_3X3
PUSB3FR4_DFN2510A10-10
L05L5V0C6-4C

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Issued Date	2019/05/15	Deciphered Date	2020/05/15

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Compal Electronics, Inc.

Title: **Reserve**

Size: C | Document Number: LA-LJ551PR02 | Rev: 0.2

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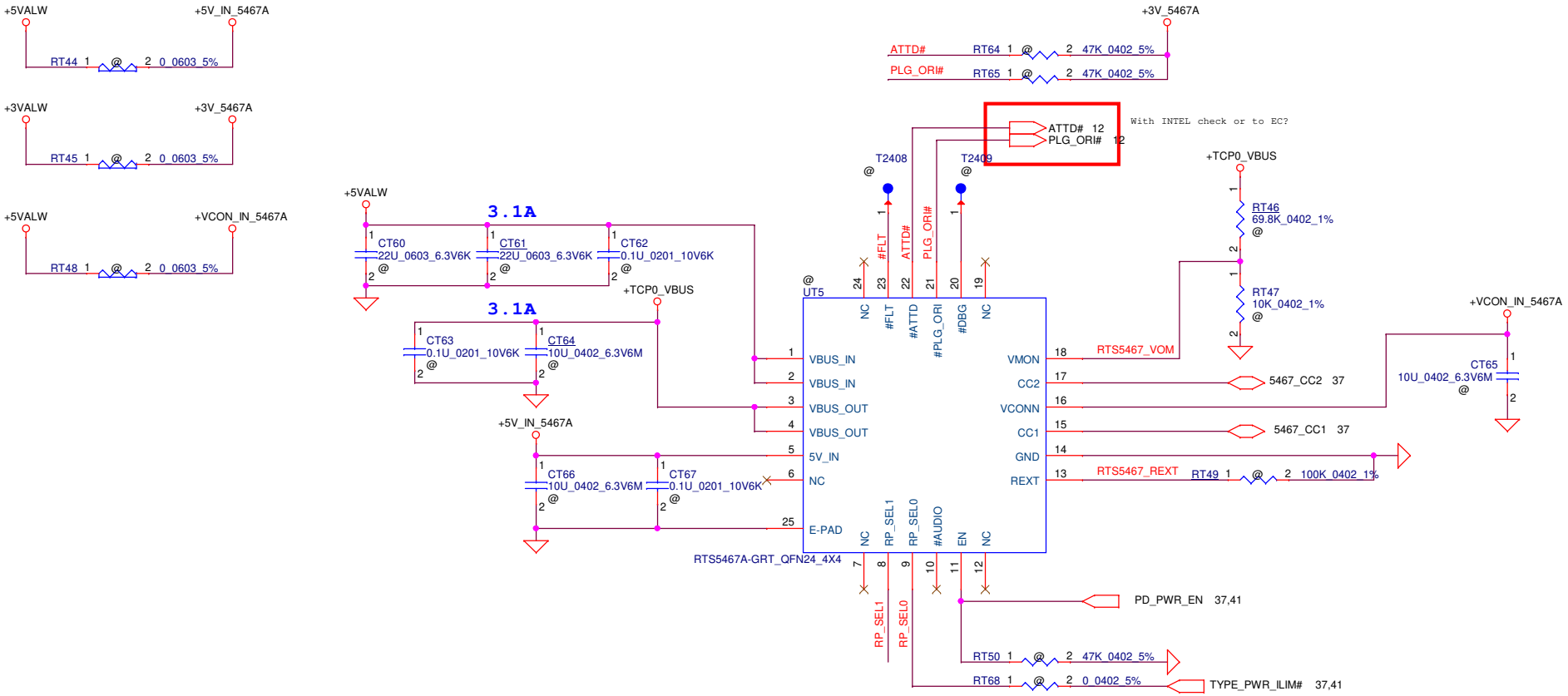

Security Classification	Compal Secret Data		
Issued Date	2019/05/15	Deciphered Date	2020/05/15

Compal Electronics, Inc.			
Title: Reserve			
Size: B	Document Number: LA-LJ551PR02		Rev: 0.2
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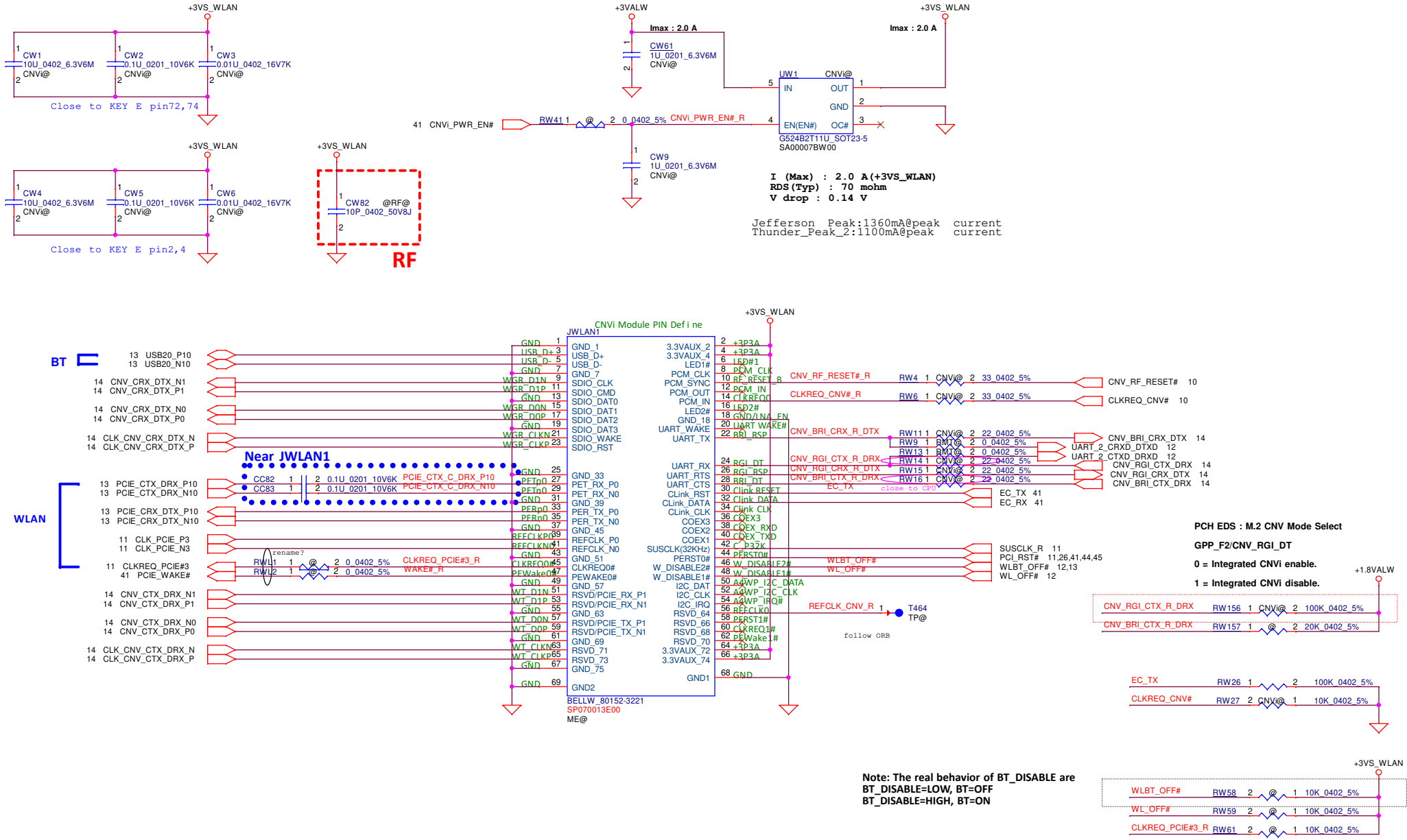
NGFF WLAN / BT (Key E)

NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]



Security Classification	Compal Secret Data		
Issued Date	2019/05/15	Deciphered Date	2020/05/15

Compal Electronics, Inc.			
Title	NGFF WLAN / BT		
Size	Document Number LA-LJ551PR02		Rev 0.2
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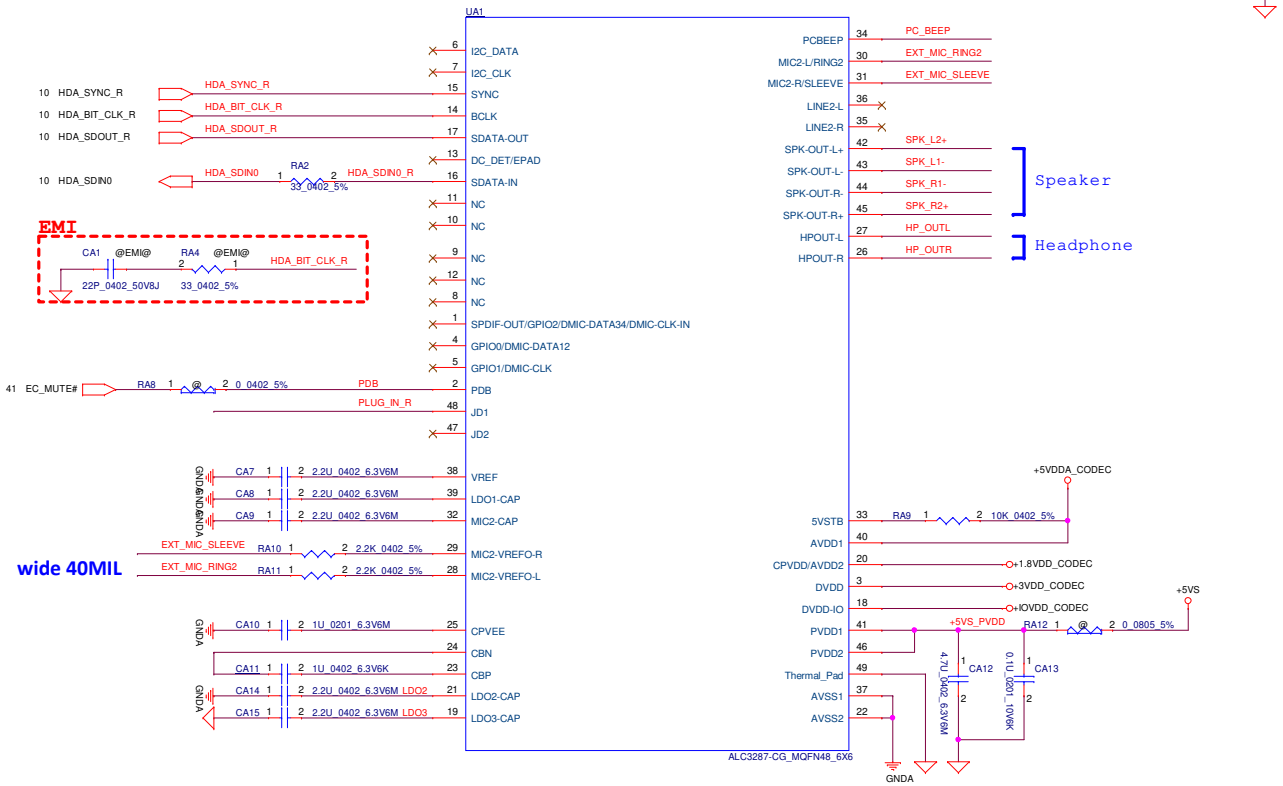
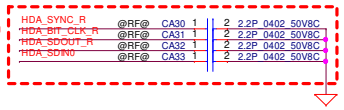
ALC3287



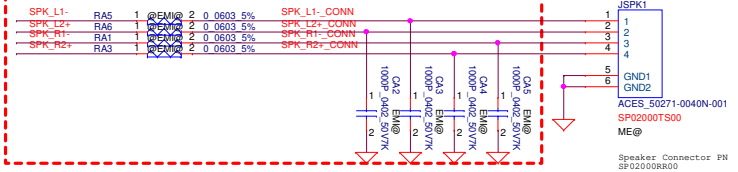
RF



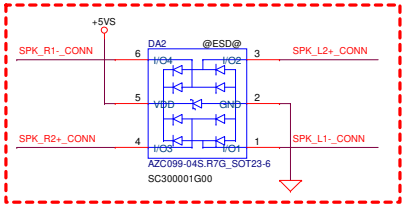
Speaker

EMI

SPEAK 4 ohm : 40MIL
SPEAK 8 ohm : 20MIL



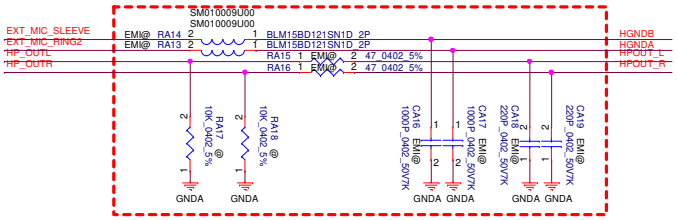
ESD



ESD

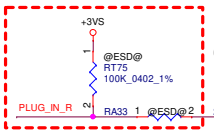
EMI

W=40mils
W=40mils



Follow LAH101P un-stuff CA16, stuff CA35

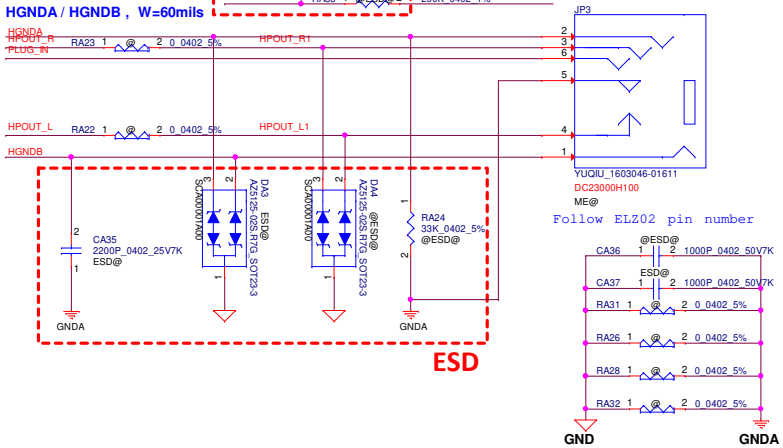
Close Audio codec



RA33 ESD@ 0_0402_5%

Combo Jack (Normal Open)

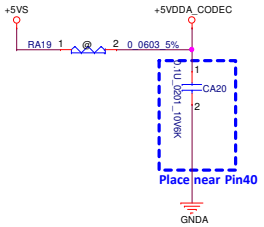
HGNDA / HGNDB , W=60mils



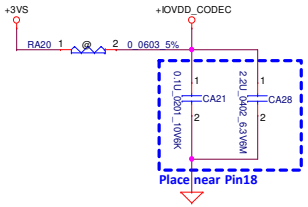
ESD

Follow ELZ02 pin number

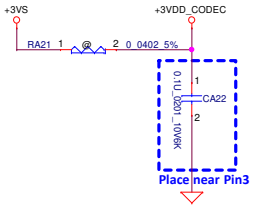
+5VS --> +5VDDA_CODEC



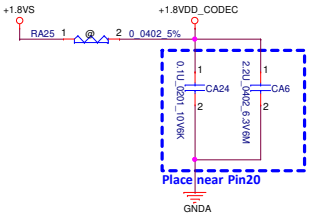
+3.3VS --> +IOVDD_CODEC



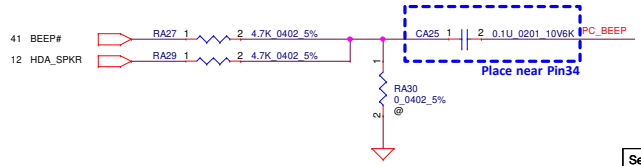
+3VS --> +3VDD_CODEC



+1.8VS --> +1.8VDD_CODEC



PC Beep



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Issued Date	2019/05/15	Deciphered Date	2020/05/15

Compal Electronics, Inc.

Title: Audio Codec Realtek ALC3287

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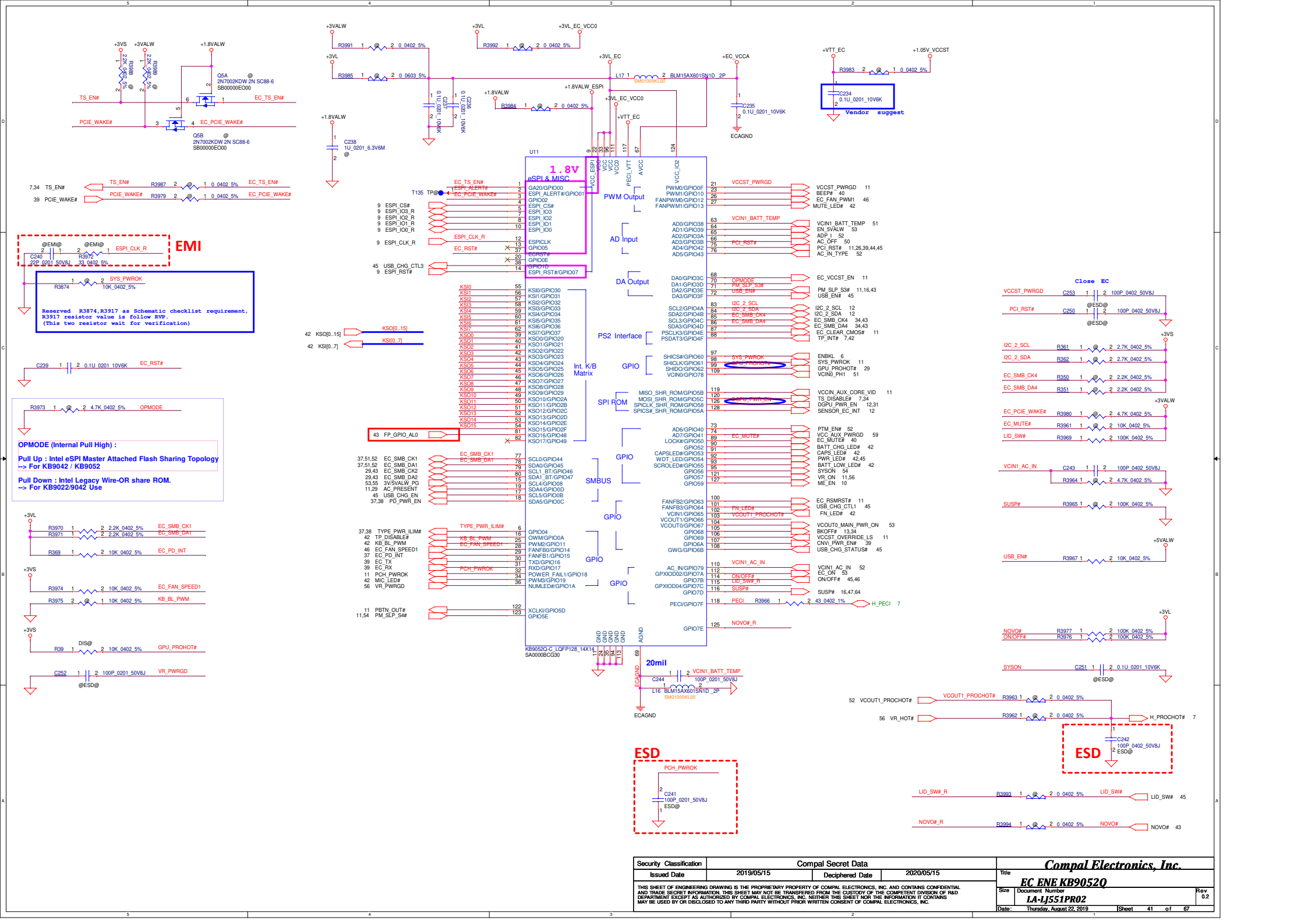
U11
1.8V
eSPI & MISC.
PWM Output
AD Input
DA Output
PS2 Interface
GPIO
Int. K/B Matrix
SPI ROM
SMBUS
KB9052Q-C_LQFP128_14X14
SA0000BCG30
EMI
ESD
20mil
Close EC
Reserved R3874,R3917 as Schematic checklist requirement, R3917 resistor value is follow RVP. (This two resistor wait for verification)
OPMODE (Internal Pull High) :
Pull Up : Intel eSPI Master Attached Flash Sharing Topology --> For KB9042 / KB9052
Pull Down : Intel Legacy Wire-OR share ROM. --> For KB9022/9042 Use
Vendor suggest
Security Classification
Compal Secret Data
Issued Date
2019/05/15
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2020/05/15
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EC ENE KB9052Q
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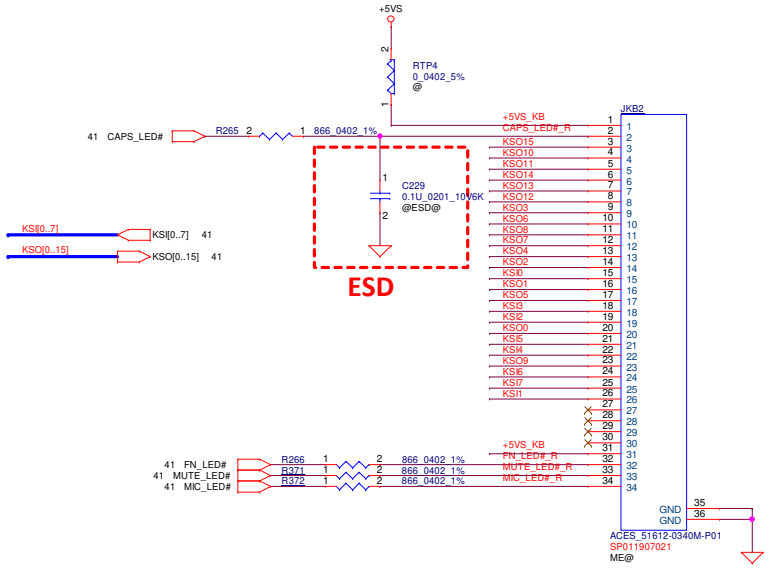
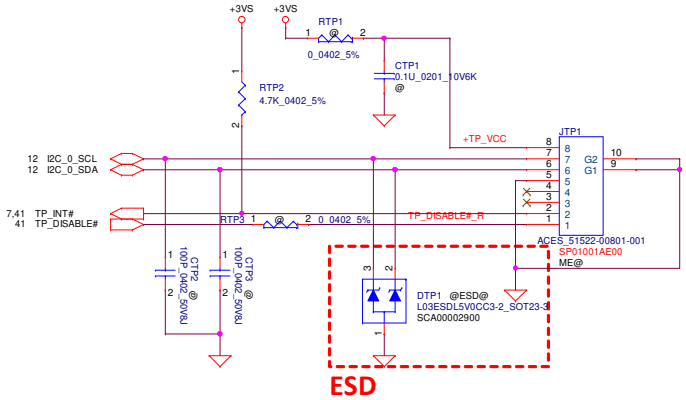
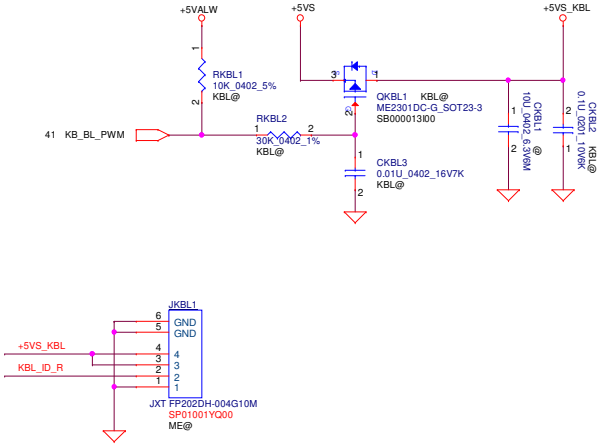
Keyboard



Touch Pad

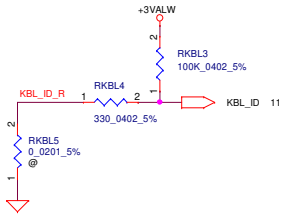


Keyboard Backlight

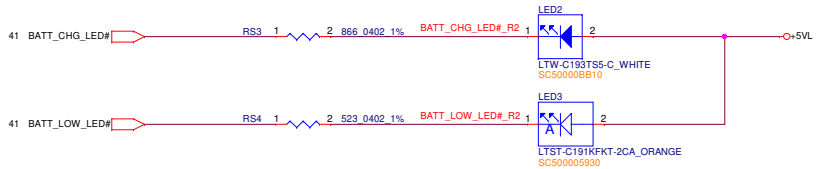


Keyboard BackLight_SELECT

Funct i on	KBL_ID
KBL	0
NO KBL	1



BATT LED



Status LED

Security Classification	Compal Secret Data		
Issued Date	2019/05/15	Deciphered Date	2020/05/15

Compal Electronics, Inc.			
Title: KB / LED / TP / LID			
Size: Custom	Document Number: LA-LJ551PR02		Rev: 0.2
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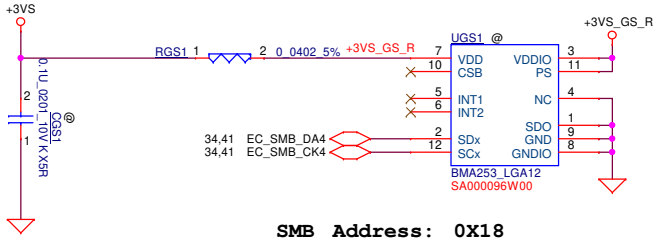
NOVO Button

G-Sensor

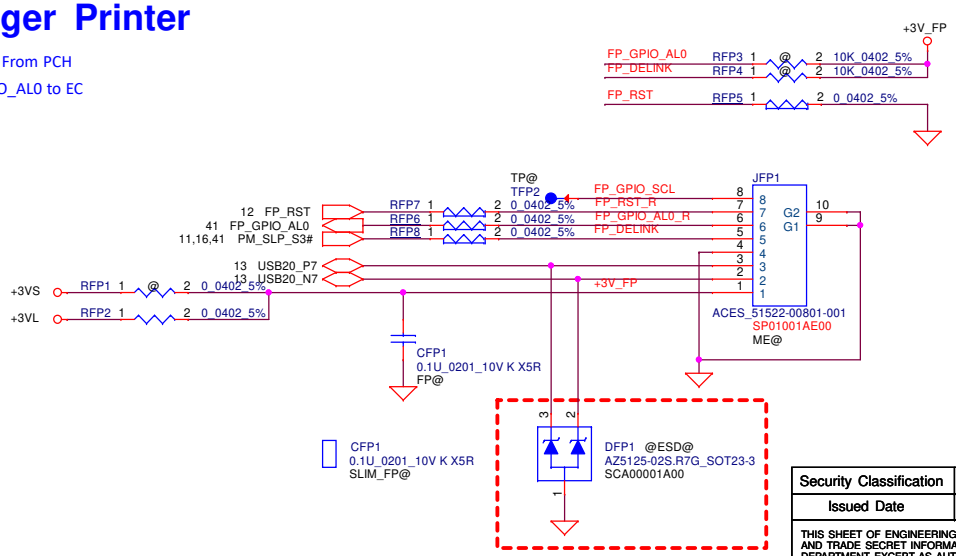


SMB Address: 0X18

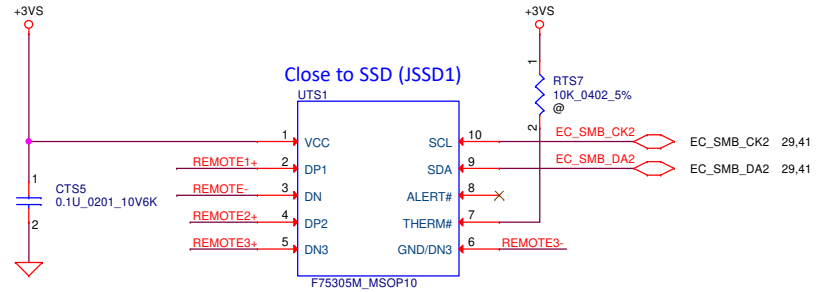
Finger Printer

FP_RST From PCH

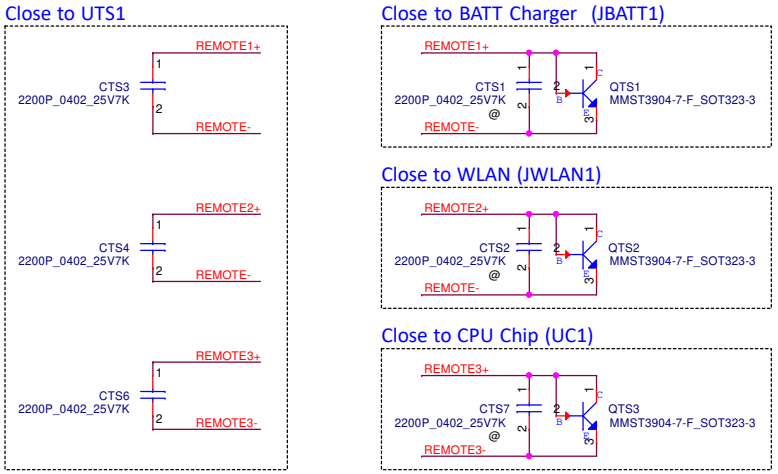
FP_GPIO_AL0 to EC



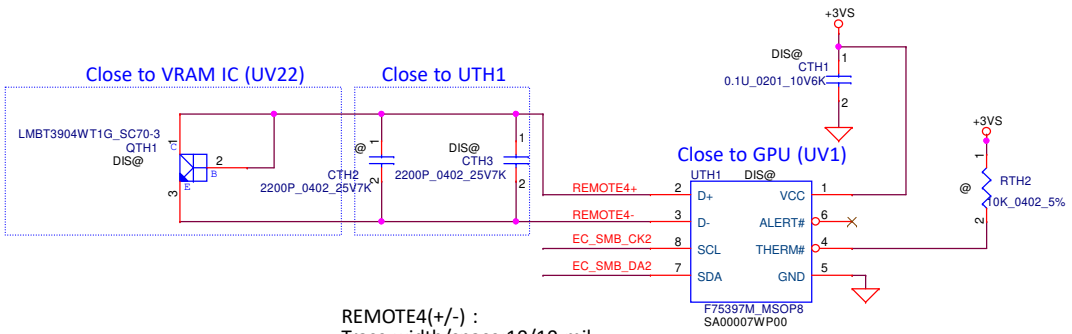
Thermal Sensor



Address 1001_101xb



REMOTE1,2,3 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"



REMOTE4(+/-) :
Trace width/space:10/10 mil
Trace length:<8"

Address 1001_100xb

Security Classification	Compal Secret Data		
Issued Date	2019/05/15	Deciphered Date	2020/05/15

Compal Electronics, Inc.

Title: **Thermal / Finger Printer**

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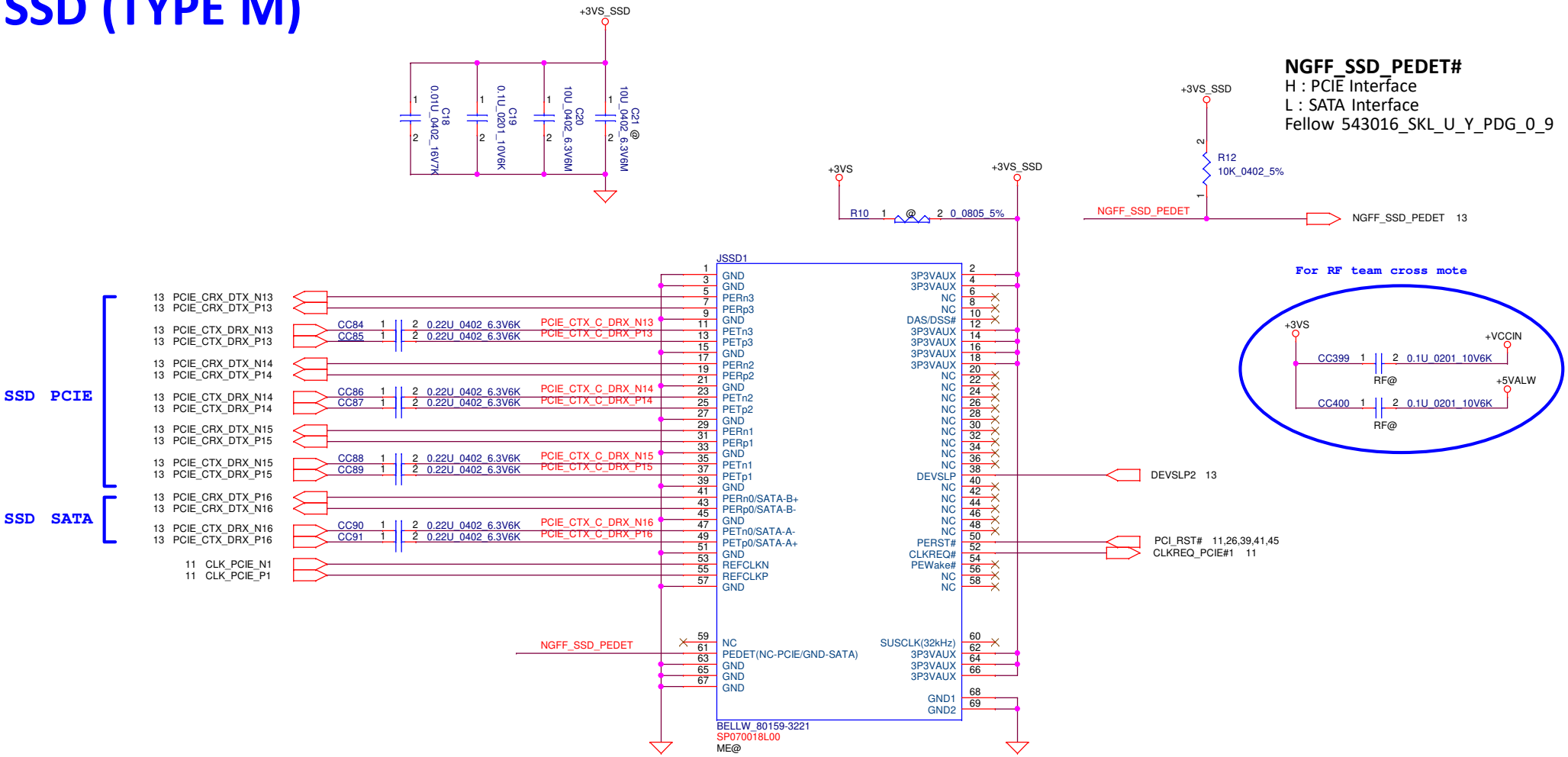
SSD (TYPE M)



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Issued Date	2019/05/15	Deciphered Date	2020/05/15

Compal Electronics, Inc.			
Title: NGFF SSD			
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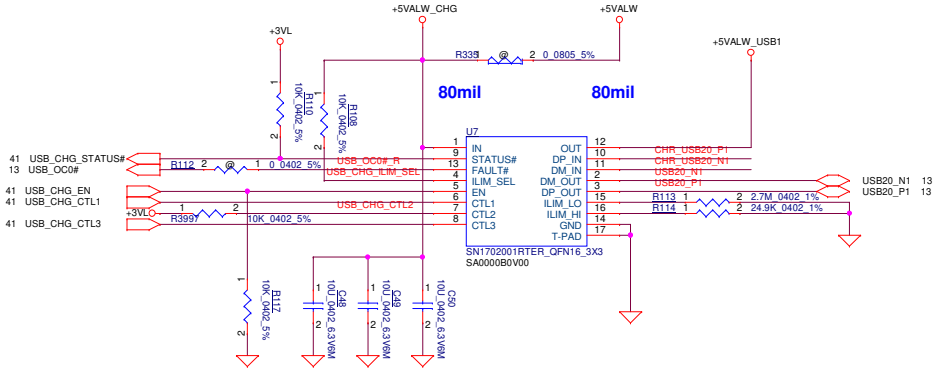
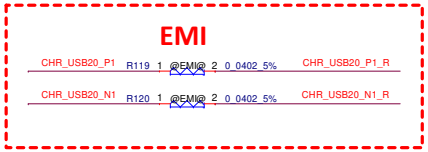
USB3.0_Port (AOU_Port)

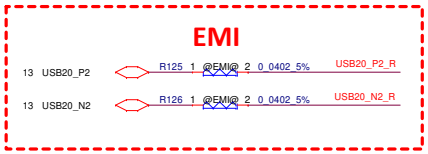


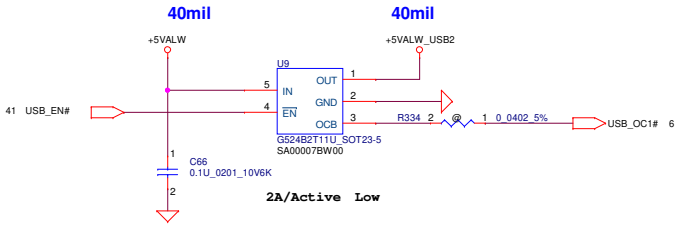
EMI



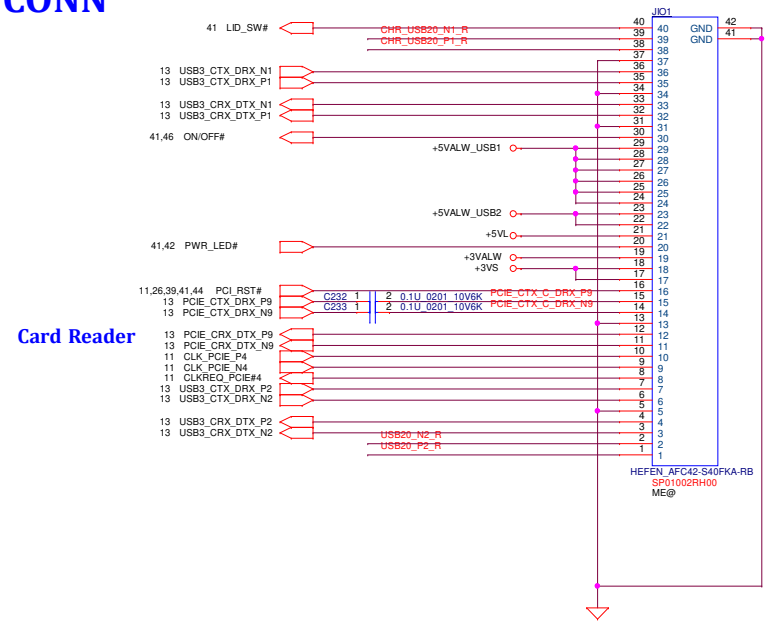
USB3.0_Port (Non-AOU_Port)

EMI





I/O CONN



Card Reader

Security Classification	Compal Secret Data		
Issued Date	2019/05/15	Deciphered Date	2020/05/15

Compal Electronics, Inc.			
Title	USB3 / IO board Conn.		
Size	Document Number		Rev
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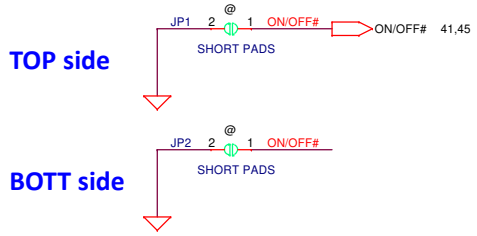
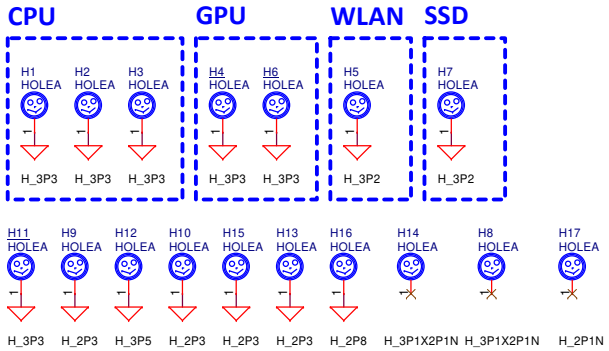
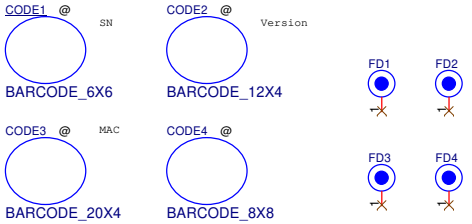
ON/OFF# SHORT PAD



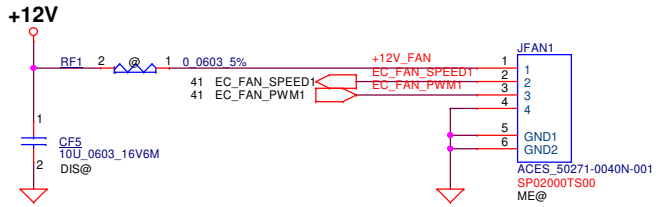
SCREW



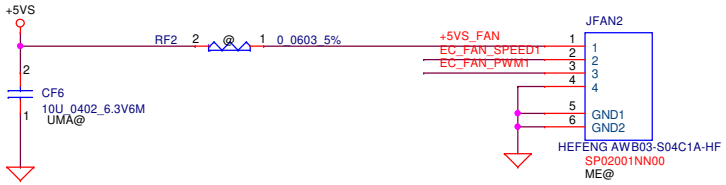
LASER BARCODE



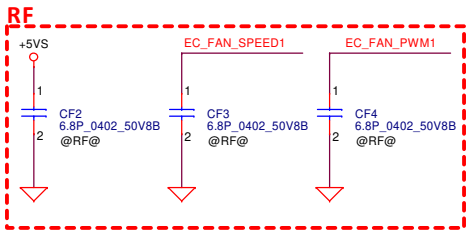
+12V FAN



+5V FAN



RF



Security Classification	Compal Secret Data		
Issued Date	2019/05/15	Deciphered Date	2020/05/15

Compal Electronics, Inc.

Title: PCB PN / SCREW / FAN

Size: Custom | Document Number: LA-LJ551PR02 | Rev: 0.2

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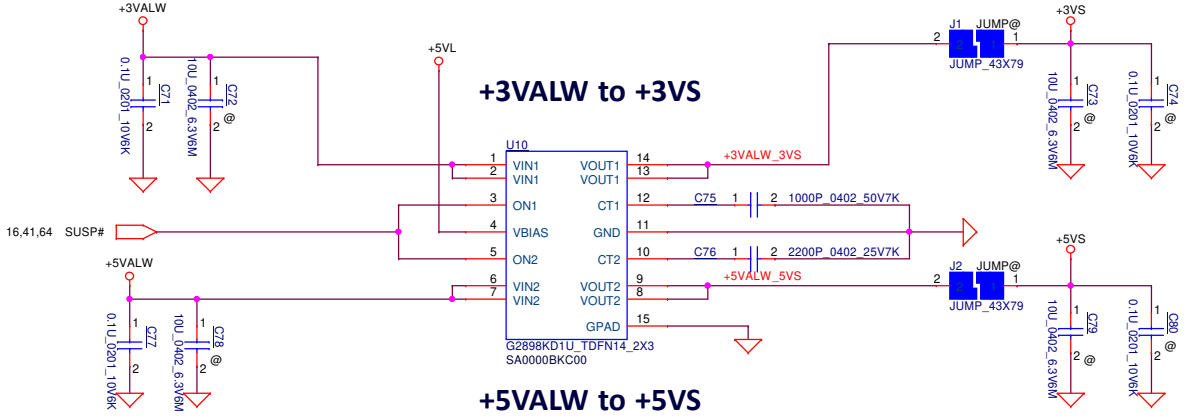
DC to DC



Security Classification	Compal Secret Data		
Issued Date	2019/05/15	Deciphered Date	2020/05/15

Compal Electronics, Inc.			
Title: DC to DC			
Size: Custom	Document Number: LA-LJ551PR02		Rev: 0.2
Date: Thursday, August 22, 2019	Sheet 47 of 67		

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Issued Date	2019/05/15	Deciphered Date	2020/05/15

Compal Electronics, Inc.

Title: **Reserve**

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Issued Date	2019/05/15	Deciphered Date	2020/05/15

Compal Electronics, Inc.

Title: **Reserve**

Size	Document Number	Rev
B	LA-LJ551PR02	0.2

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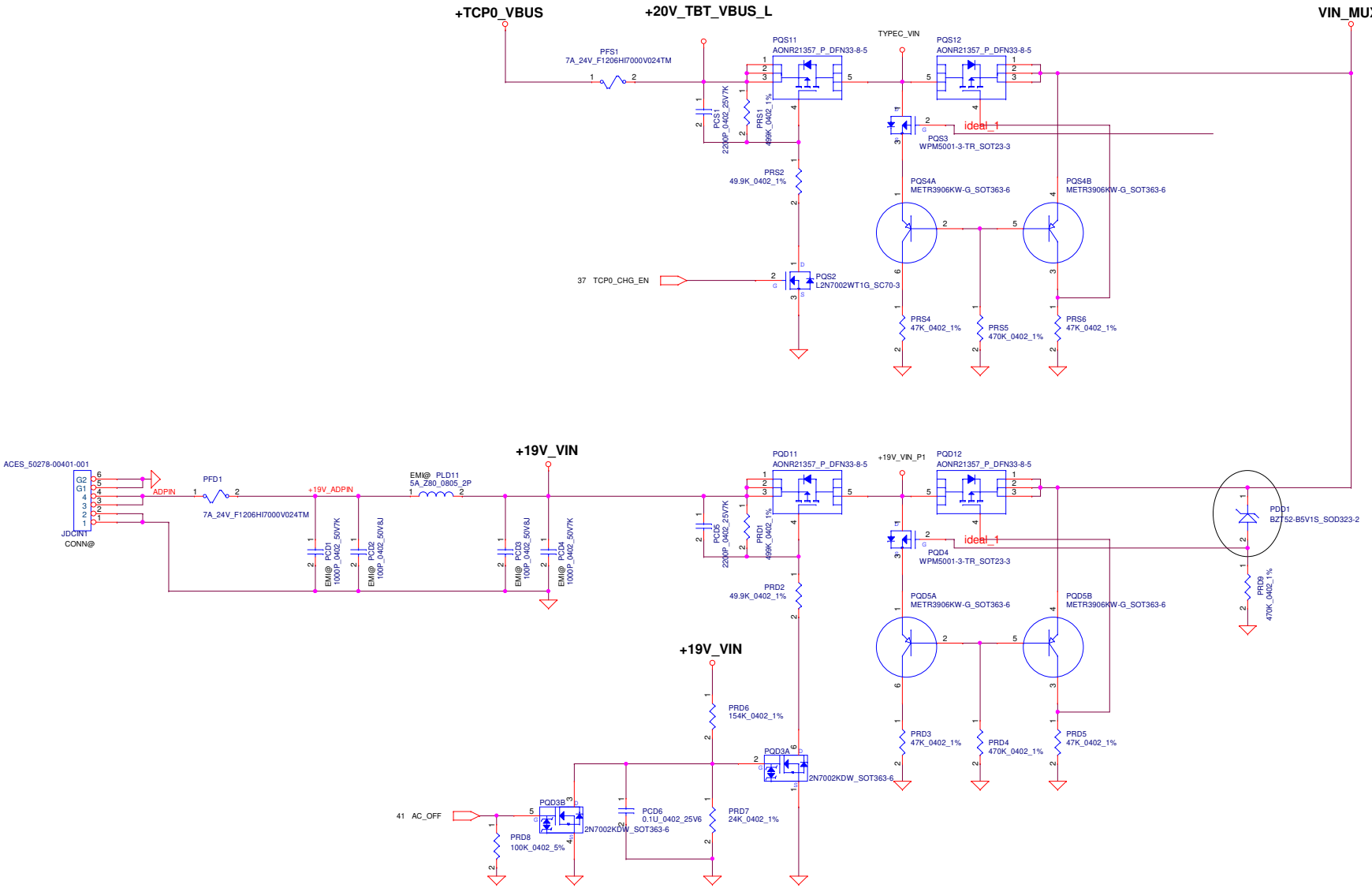

Security Classification	Compal Secret Data		
Issued Date	2019/05/23	Deciphered Date	2021/05/31

Compal Electronics, Inc.

Title: **PWR- DC Conn/Type-C PD in**

Size	Document Number	Rev
Custom	LA-LJ551PR01	0.2

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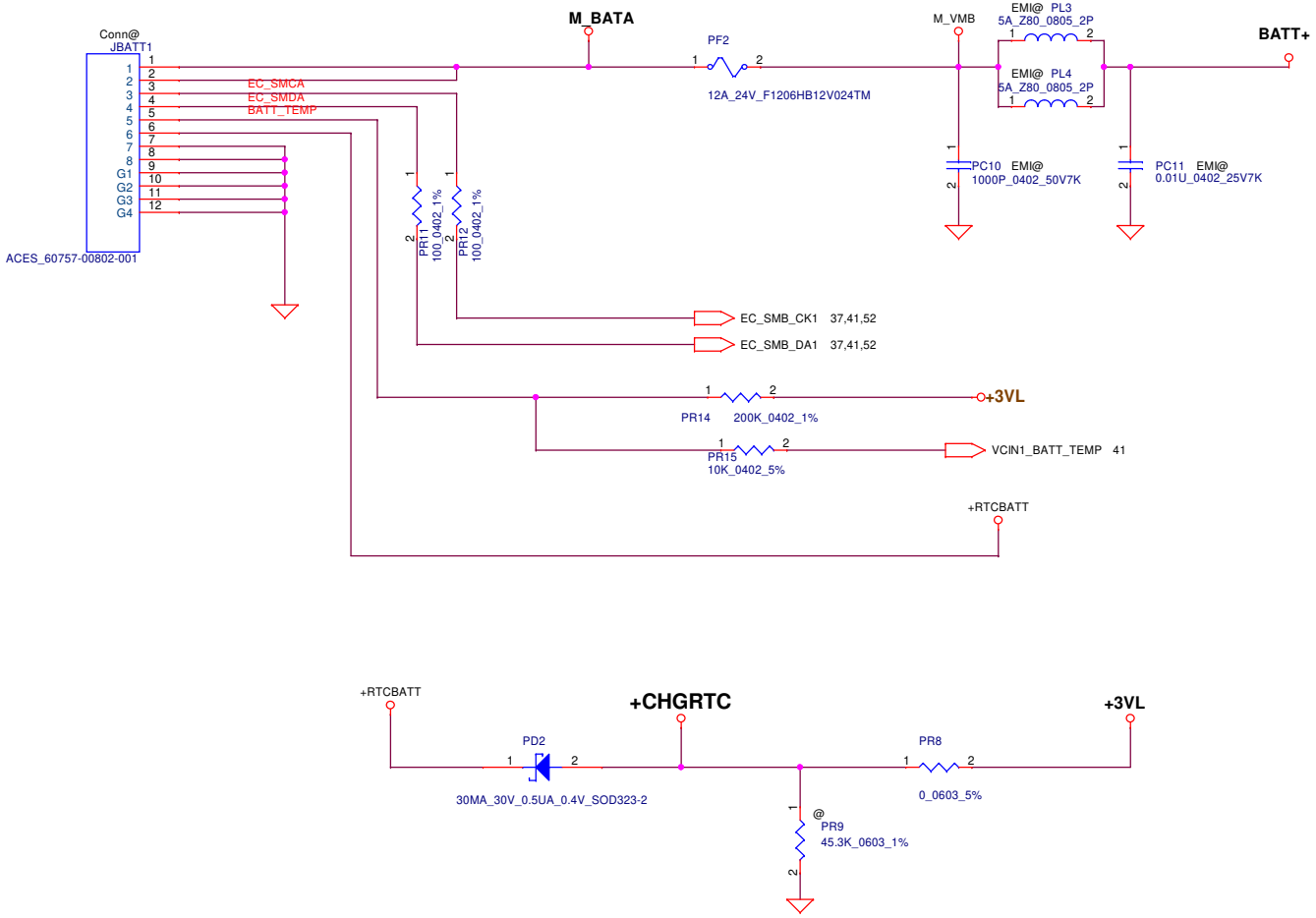
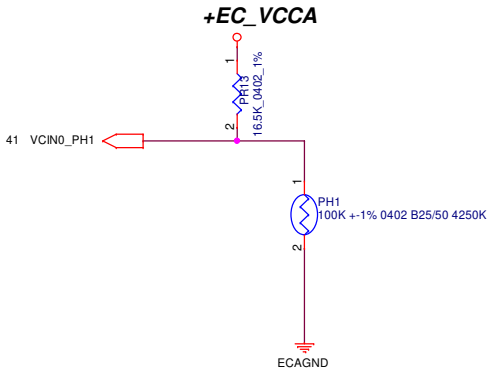


PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



Security Classification	Compal Secret Data		
Issued Date	2019/05/23	Deciphered Date	2021/05/31

Compal Electronics, Inc.

Title: **PWR- BATTERY CONN/OTP/RTC**

Size	Document Number	Rev
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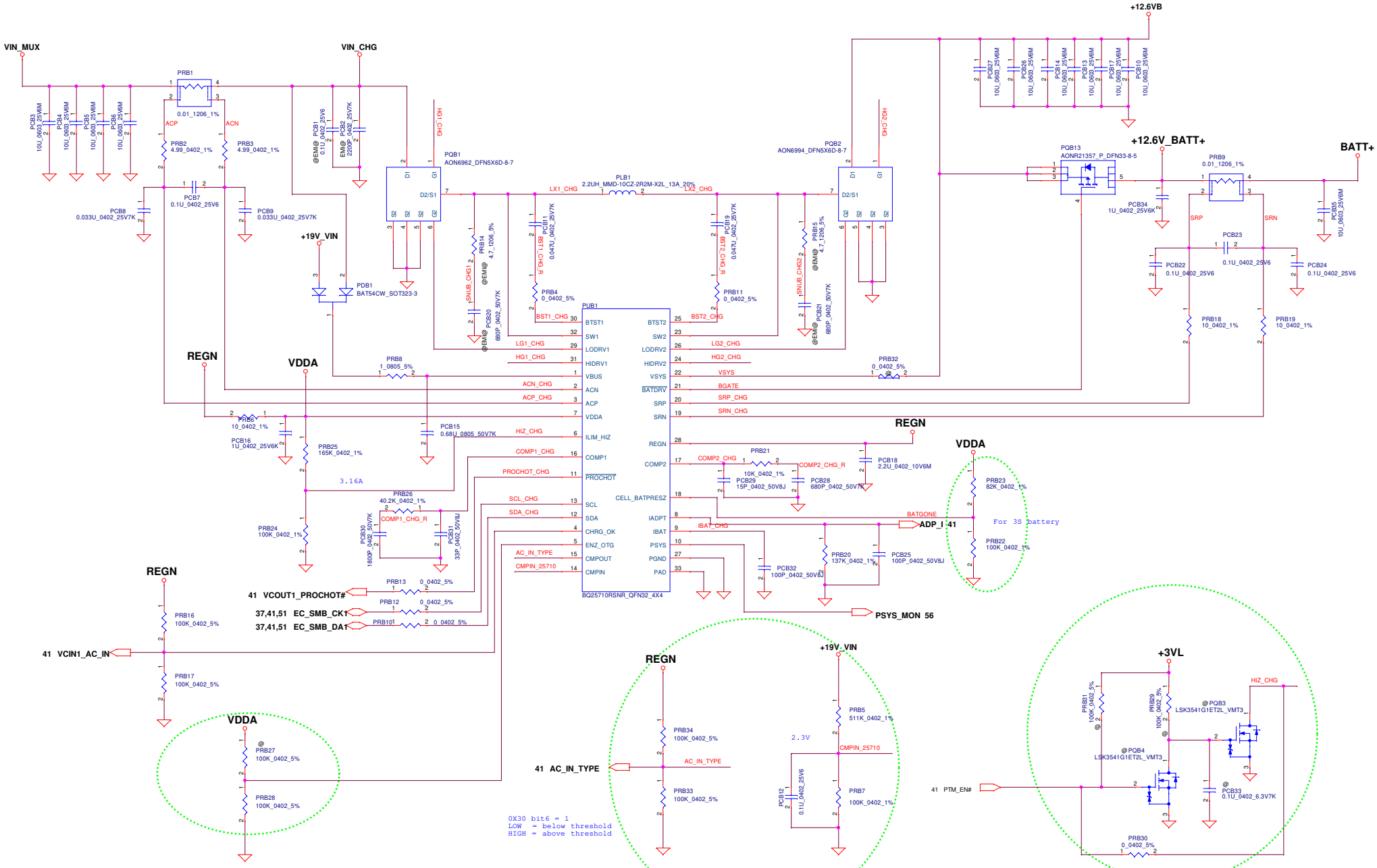
VIN_MUX
VIN_CHG
+12.6VB
+12.6V_BATT+
BATT+
+19V_VIN
REGN
VDDA
PUB1
BQ25710RSNR_QFN32_4X4
PQB1 AON6962_DFN5X6D-8-7
PQB2 AON6994_DFN5X6D-8-7
PQB13 AONR21357_P_DFN33-8-5
PDB1 BAT54CW_SOT323-3
PLB1 2.2UH_MMD-10CZ-2R2M-X2L_13A_20%
LX1_CHG
LX2_CHG
HG1_CHG
HG2_CHG
BST1_CHG
BST2_CHG
LG1_CHG
LG2_CHG
ACN_CHG
ACP_CHG
HIZ_CHG
COMP1_CHG
PROCHOT_CHG
SCL_CHG
SDA_CHG
AC_IN_TYPE
CMPIN_25710
COMP2_CHG
IBAT_CHG
BATGONE
VSYS
BGATE
SRP_CHG
SRN_CHG
CELL_BATPRESZ
PSYS_MON 56
41 VCOUT1_PROCHOT#
37,41,51 EC_SMB_CK1
37,41,51 EC_SMB_DA1
41 VCIN1_AC_IN
41 AC_IN_TYPE
41 PTM_EN#
ADP_I 41
3.16A
For 3S battery
+3VL
0X30 bit6 = 1
LOW = below threshold
HIGH = above threshold
Security Classification
Compal Secret Data
Issued Date
2019/05/23
Deciphered Date
2021/05/31
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Title
PWR- CHARGER
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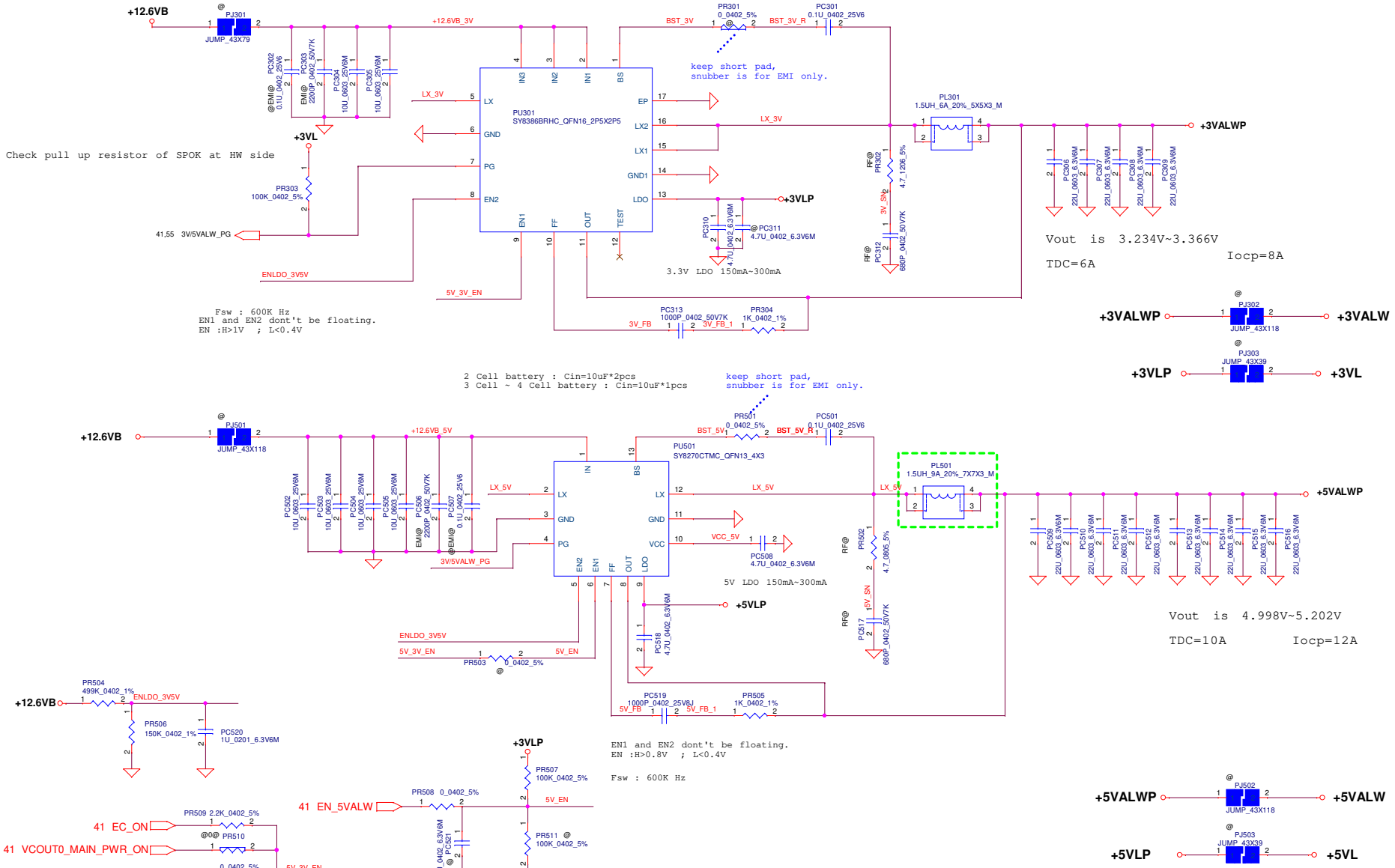

Security Classification	Compal Secret Data		
Issued Date	2019/05/23	Deciphered Date	2021/05/31

Compal Electronics, Inc.

Title: **PWR- 3/5VALWP**

Size	Document Number	Rev
Custom	LA-LJ551PR01	0.2

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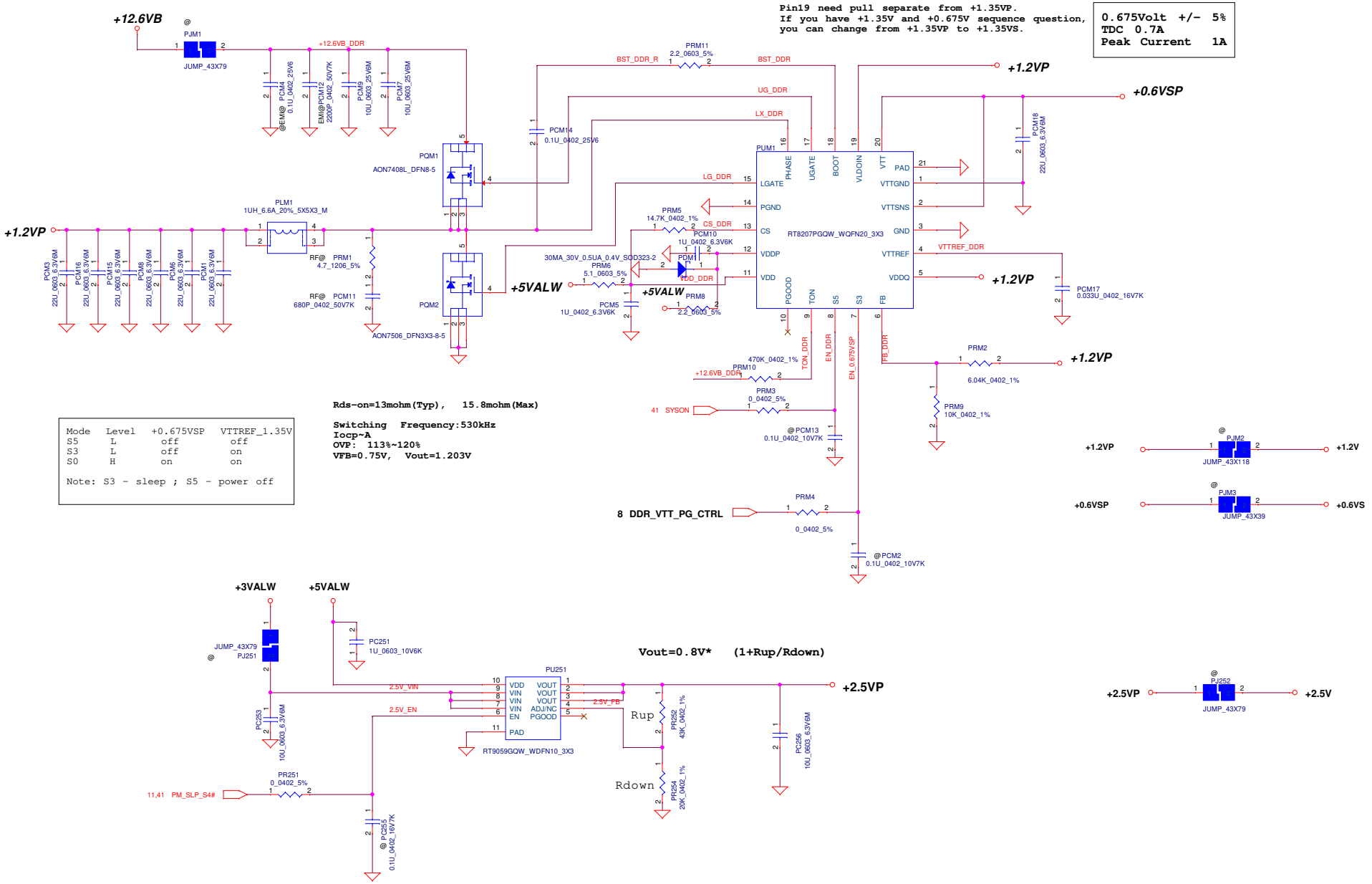

Security Classification	Compal Secret Data		
Issued Date	2019/05/23	Deciphered Date	2021/05/31

Compal Electronics, Inc.

Title: **PWR- DDR**

Size	Document Number	Rev
Custom	LA-LJ551PR01	0.2

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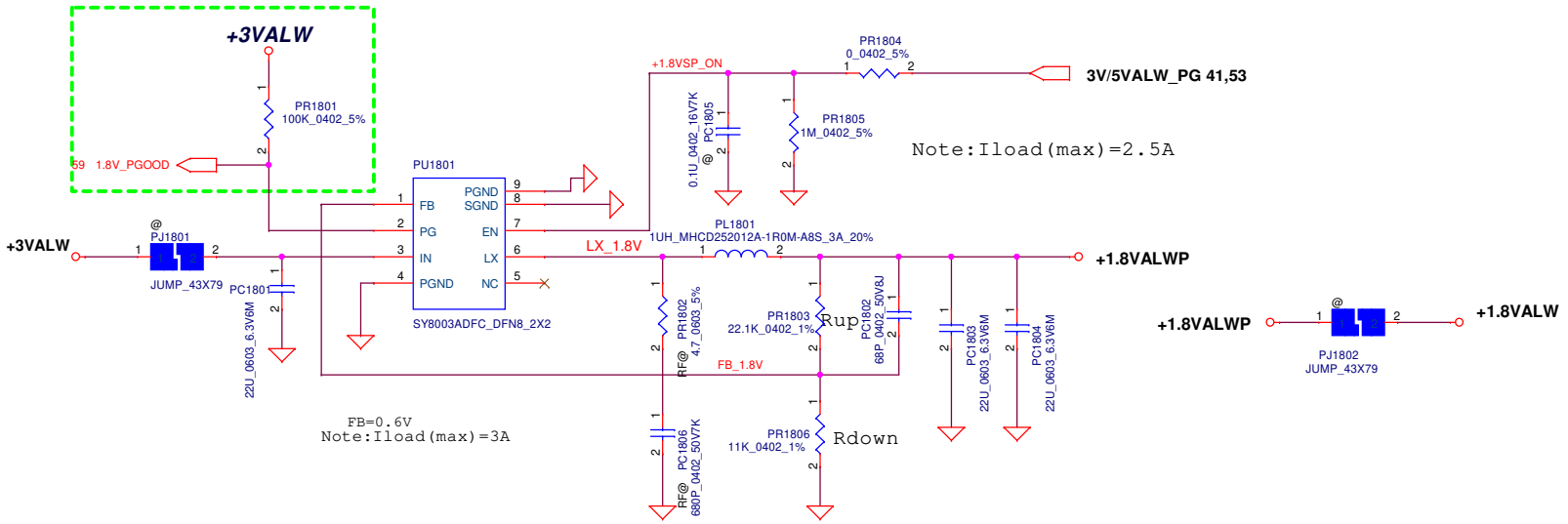

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

Security Classification	Compal Secret Data		
Issued Date	2019/05/23	Deciphered Date	2021/05/31

Compal Electronics, Inc.

Title: **PWR- 1.8VALWP**

Size	Document Number	Rev
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Module model information

MP2940_V1A.mdd for IC portion
MP2940_V1B.mdd for SW portion

Rpsys=0.8/PWR_in_MAX*Isys
=0.8/160uA
=5k ohm

Where:
PWR_in_Max is the maximum input power, with the unit of W.

$$T_{JUNCTION} = \frac{V_{TEMP} + 100mV}{10mV/^{\circ}C}$$

PE pin can be always pull high to 3.3V
The leakage is 3.3V/100Kohm=0.033mA.

H>0.8 L<0.4

Vcs=(10uA*Io)*Rcs*1.23

Static Load Line Setting

Rdroop=RLL/2*10uA*(4/8*1/8)*1000
=2m/2*10uA*(4/8*1/8)*1000
=1.6k

RIMON=32*(1.6*8/11)/(ICCMAX*10uA)*1000
=32*(1.6*8/11)/(33*10uA)*1000
=113k

1.8V LDO output for current sense

Function Field :
PWR.Plane.Regulator_MP2940:36.1
Rest of support elements:36.3

Security Classification	Compal Secret Data		
Issued Date	2019/05/23	Deciphered Date	2021/05/31

Compal Electronics, Inc.

Title: PWR- VCORE(MP2940)

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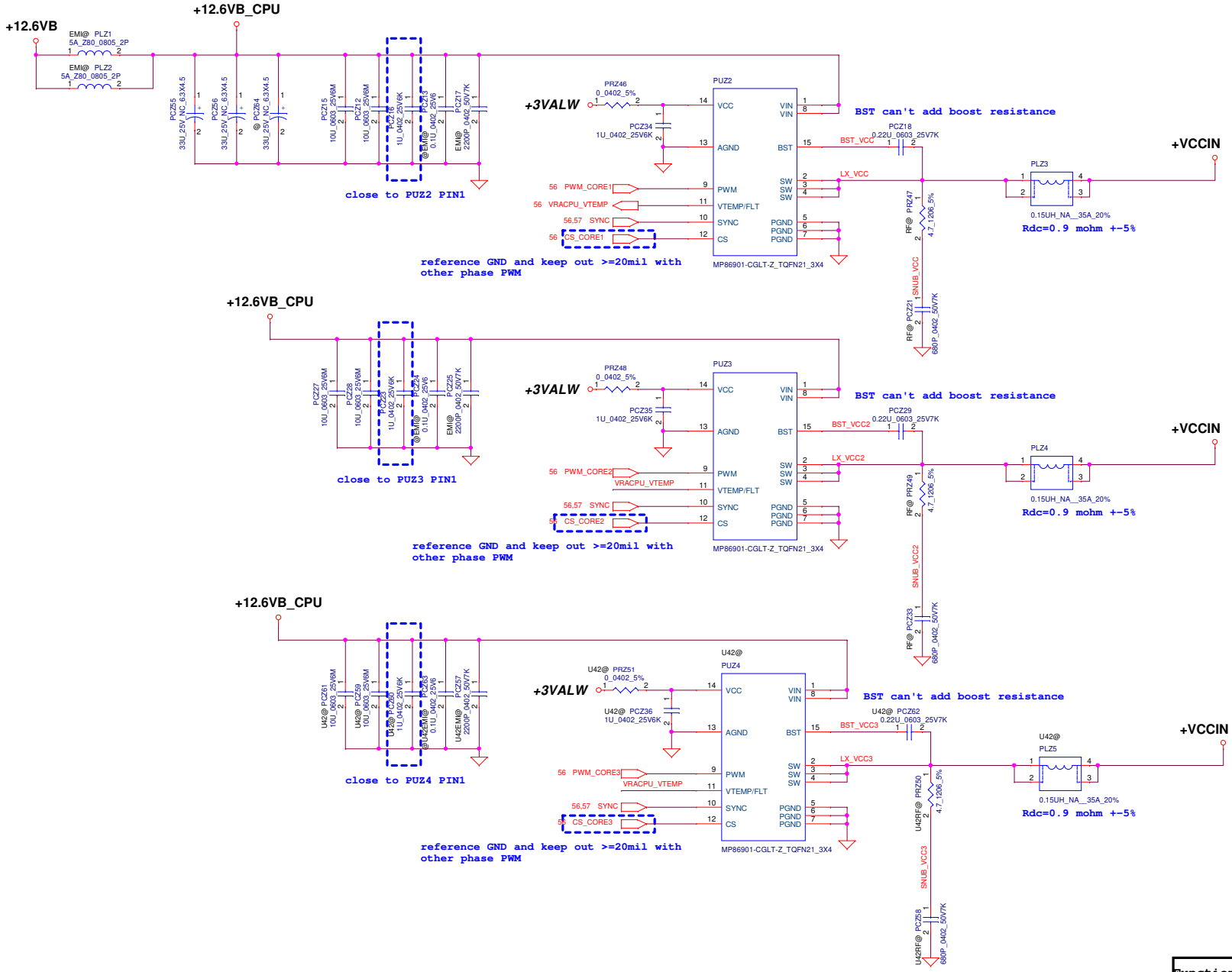
+12.6VB
+12.6VB_CPU
EMI@ PLZ1
5A_Z80_0805_2P
EMI@ PLZ2
5A_Z80_0805_2P
PCZ55
PCZ56
@ PCZ54
33U_25V_NC_6.3X4.5
PCZ15
PCZ12
PCZ14
PCZ13
@EMI@
PCZ17
EMI@
10U_0603_25V6M
1U_0402_25V6K
0.1U_0402_25V6
2200P_0402_50V7K
close to PUZ2 PIN1
+3VALW
PRZ46
0_0402_5%
PCZ34
1U_0402_25V6K
PUZ2
VCC
AGND
PWM
VTEMP/FLT
SYNC
CS
VIN
BST
SW
PGND
MP86901-CGLT-Z_TQFN21_3X4
56 PWM_CORE1
56 VRACPU_VTEMP
56,57 SYNC
56 CS_CORE1
BST can't add boost resistance
PCZ18
0.22U_0603_25V7K
BST_VCC
LX_VCC
+VCCIN
PLZ3
0.15UH_NA_35A_20%
Rdc=0.9 mohm +-5%
RF@ PRZ47
4.7_1206_5%
SNUB_VCC
RF@ PCZ21
680P_0402_50V7K
reference GND and keep out >=20mil with
other phase PWM
+12.6VB_CPU
PCZ27
PCZ28
PCZ23
PCZ24
PCZ25
close to PUZ3 PIN1
PRZ48
PCZ35
PUZ3
PCZ29
BST_VCC2
LX_VCC2
PLZ4
RF@ PRZ49
SNUB_VCC2
RF@ PCZ33
+12.6VB_CPU
U42@ PCZ61
U42@ PCZ59
U42@ PCZ58
U42@ PCZ63
U42EMI@
U42@ PCZ57
U42EMI@
close to PUZ4 PIN1
U42@ PRZ51
U42@ PCZ36
U42@ PUZ4
U42@ PCZ62
BST_VCC3
LX_VCC3
U42@ PLZ5
U42RF@ PRZ50
SNUB_VCC3
U42RF@ PCZ58
56 PWM_CORE3
56 VRACPU_VTEMP
56,57 SYNC
56 CS_CORE3
Function Field :
Drivers:36.2
Rest of support elements:36.3
CPU_Core output CAP (Including MLCC):36.4
Security Classification
Compal Secret Data
Issued Date
2019/05/23
Deciphered Date
2021/05/31
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PWR- VCORE_SW
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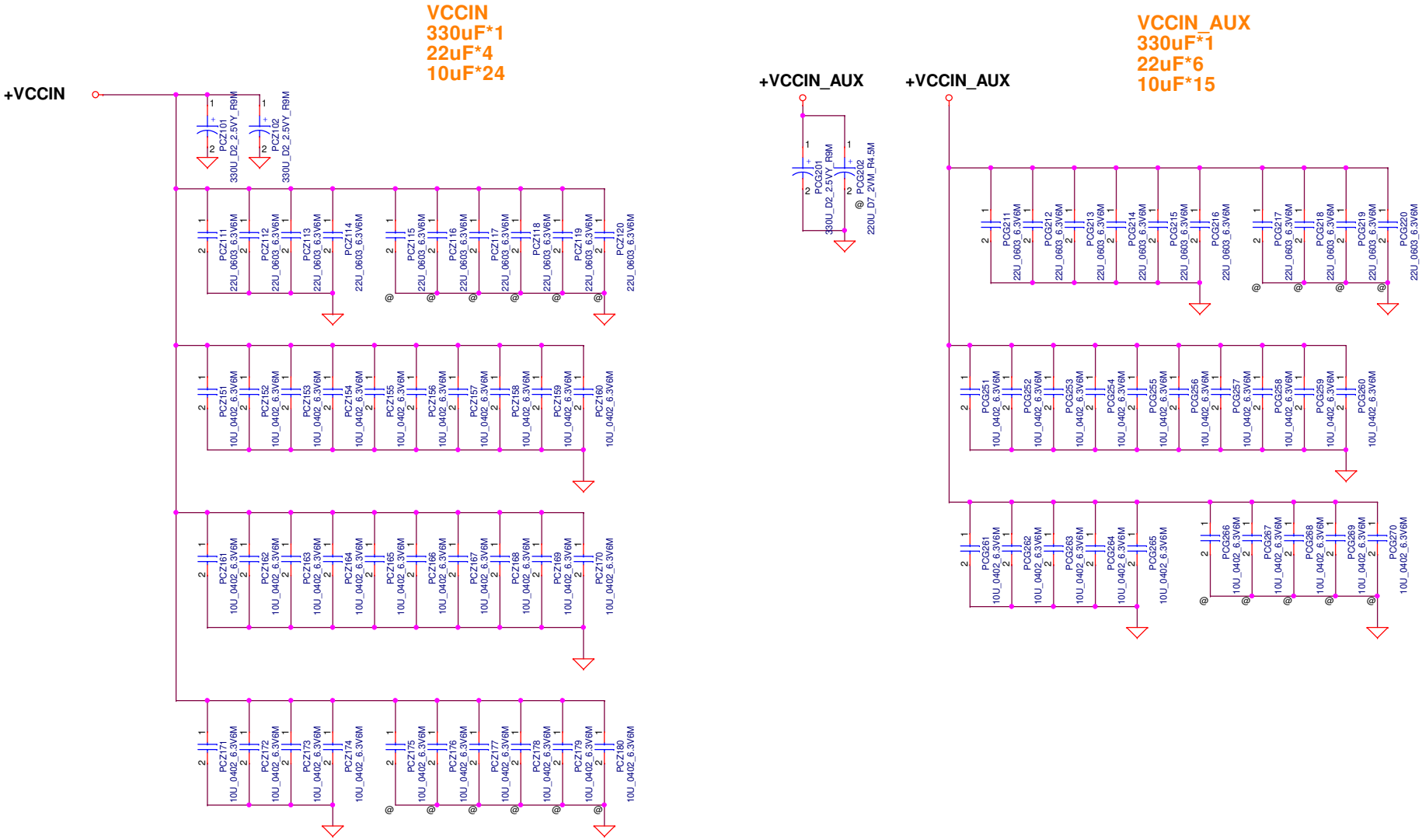

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Compal Electronics, Inc.

Title: PWR- VCORE Cap

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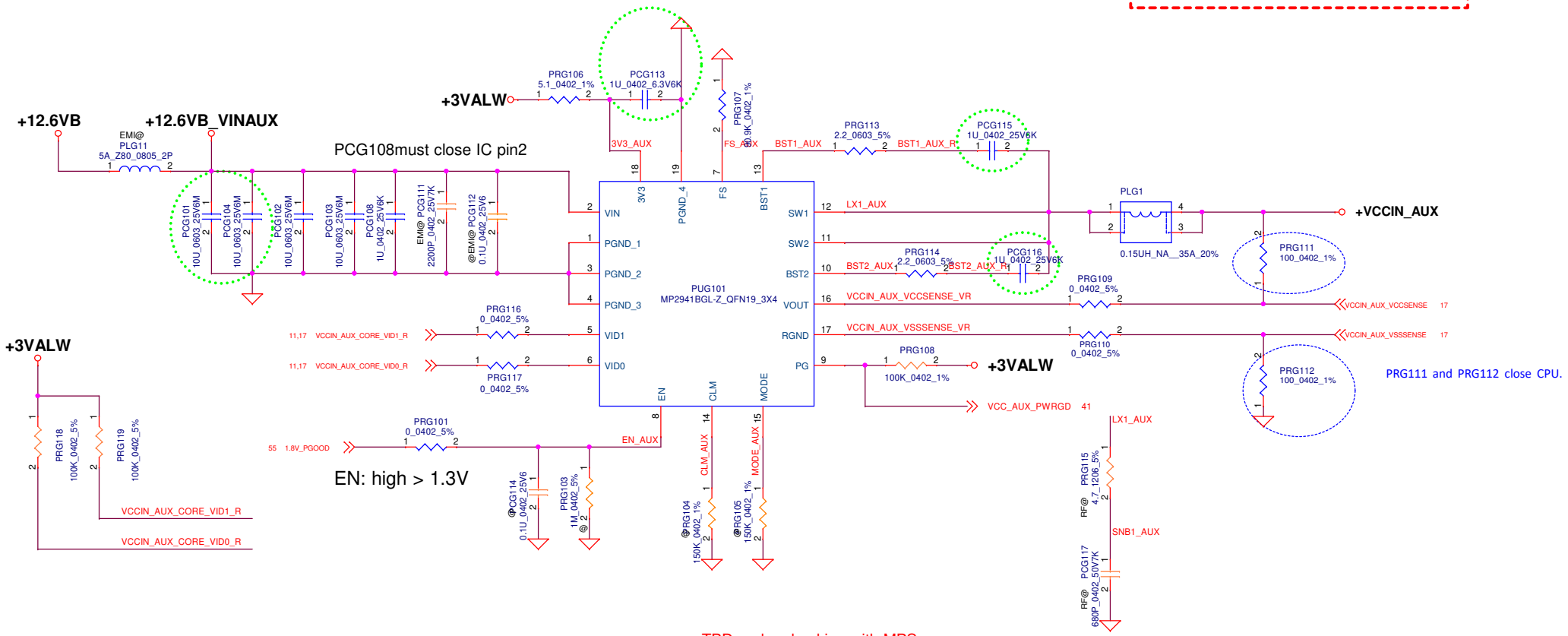
CPU PWR controller(36.1), Driver MOS(36.2), Support component(36.3)

Module model information
MP2941_V1.mdd

VCCIN_AUX (Base on PDG rev 0.71)
Peak Current 26A (ICCmax)
TDC :10A
DC Load line :TBD mV/A
AC Load line :TBD mV/A
OCP Current 32A
Fsw=700kHz

ES need to change to SA0000BJK10



PRG111 and PRG112 close CPU.

TBD under checking with MPS

Table---1:VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Table---2:CLM Select

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	13A	150k
M4	17A	>230k or float

Table---3:MODE Select

State	Interleaving	VID Down option	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90k
M3	Y	Decay	150k
M4	N	Decay	>230k or float

Table---4:FS Select

State	Fs(kHz)	Resistor to GND
M1	500	0
M2	700	90k
M3	1000	150k
M4	1200	>230k or float

Compal Electronics, Inc.

Title: PWR- VCCIN_AUX(MP2941)

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R1, R2, R3, R4, R5, C are based on VGA type to set.

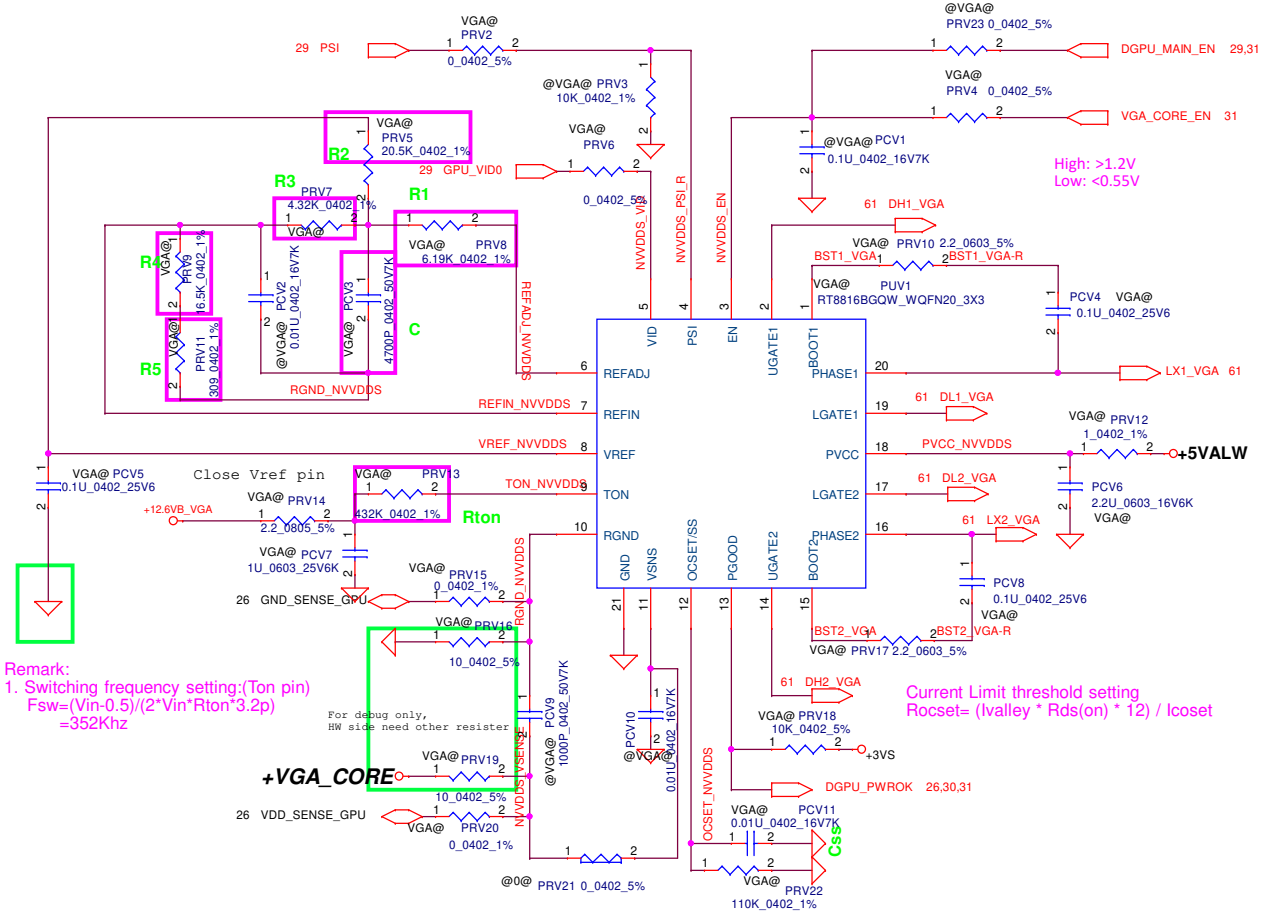
OpenVReg Configurations:(PSI pin)

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.4V
1 phase with CCM	0.7V to 0.88V
2 phase with DEM	1.08V to 1.35V
2 phase with CCM	1.6V to 5.5V

PSI pull up on HW side

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode



Remark:
1. Switching frequency setting:(Ton pin)
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)
=352Khz

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) * 12) / Icoset

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Compal Electronics, Inc.

Title: PWR- GPU_CORE

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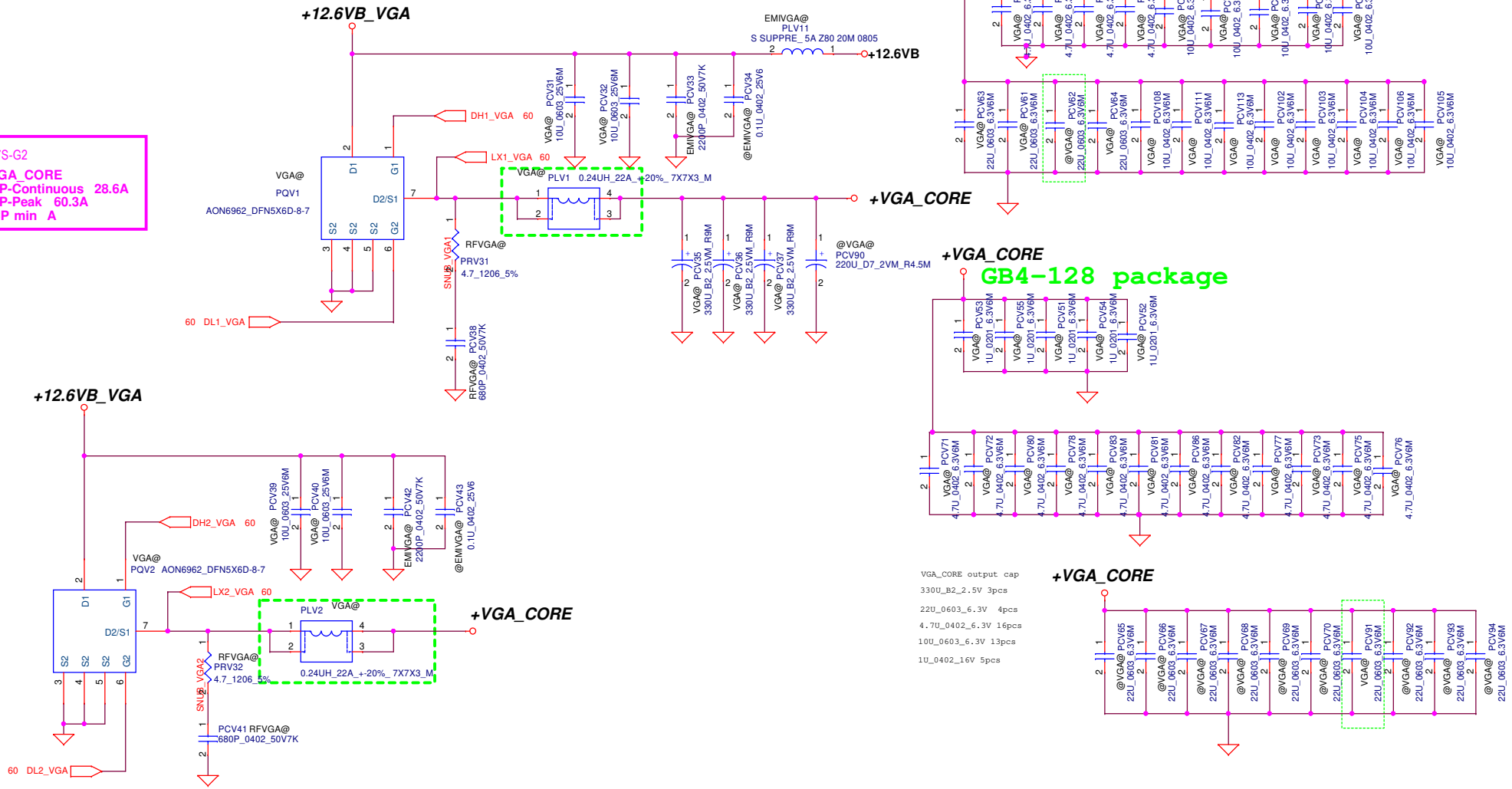
Module model information:
RT8816A-2P_NVVDDS_V2A.mdd for IC portion
RT8816A-2P_NVVDDS_V2B.mdd for SW portion

N17S-G2
+VGA_CORE
EDP-Continuous 28.6A
EDP-Peak 60.3A
OCP min A



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Compal Electronics, Inc.

Title: **PWR- GPU_CORE_SW**

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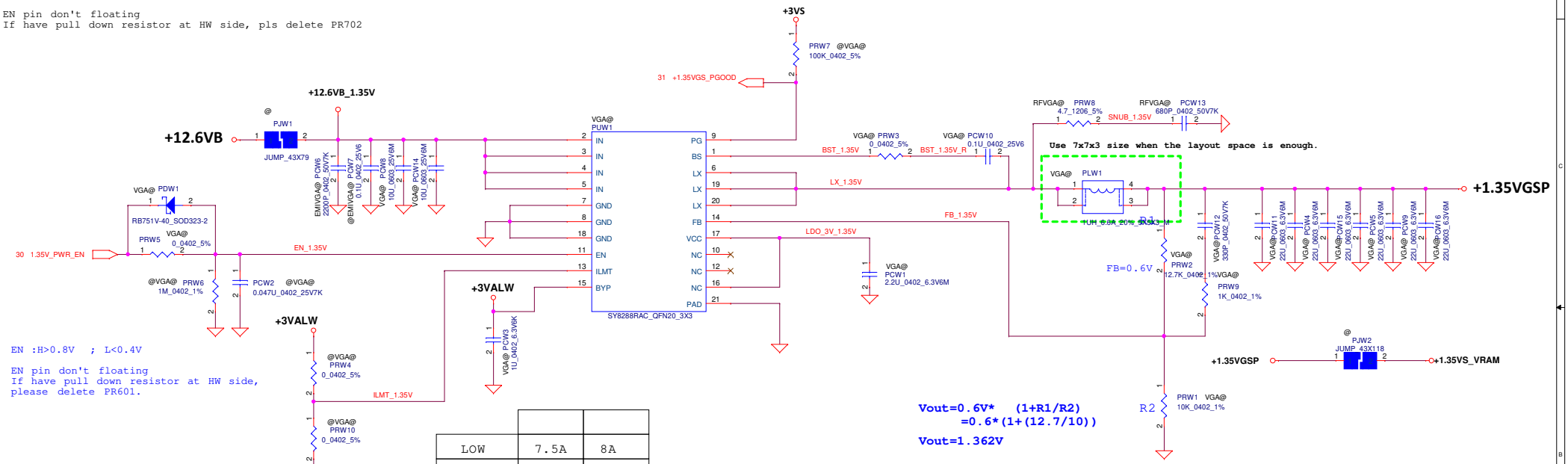
EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



EN :H>0.8V ; L<0.4V

EN pin don't floating
If have pull down resistor at HW side,
please delete PR601.

LOW	7.5A	8A
FLOATING	10.5A	12A
HIGH	13.5A	16A

Vout=0.6V* (1+R1/R2)
=0.6*(1+(12.7/10))
Vout=1.362V

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Compal Electronics, Inc.

Title: PWR- GPU_VRAM

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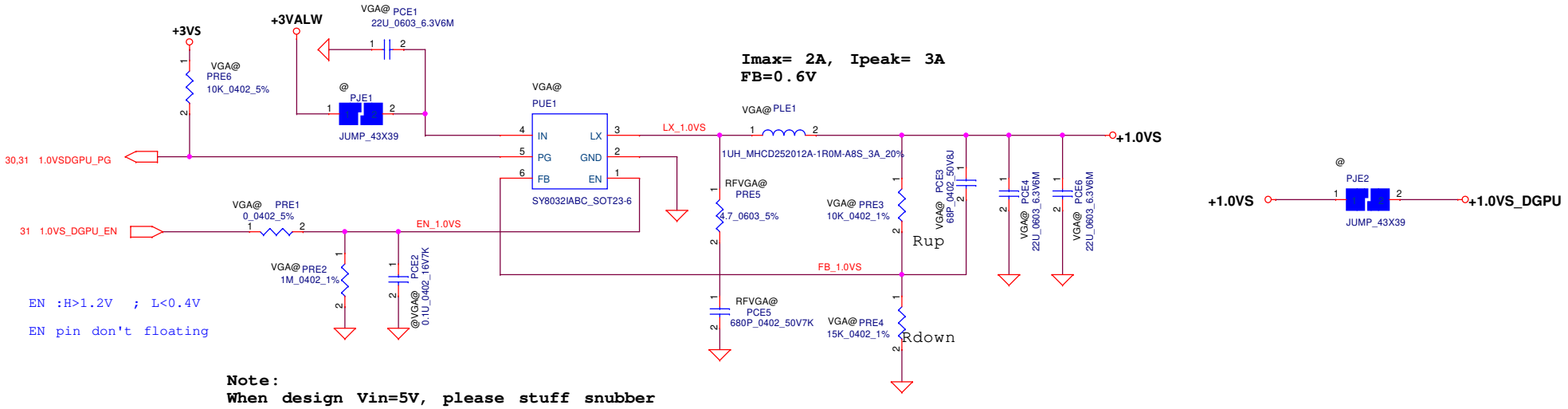

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

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Compal Electronics, Inc.

Title: PWR- GPU 1.0V

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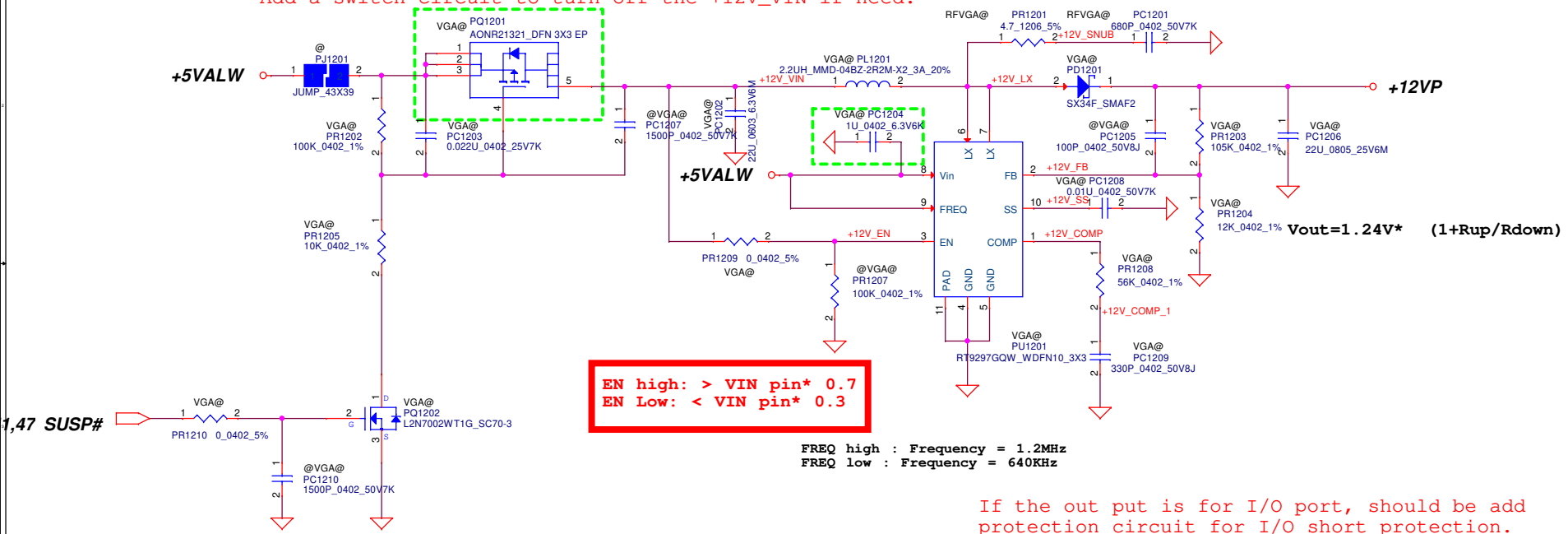
Module model information

RT9297_V1.mdd

Add a switch circuit to turn off the +12V_VIN if need.

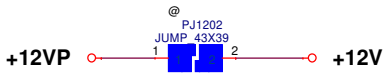
Must check PL501 and PD501 rating for your application.



EN high: > VIN pin* 0.7
EN Low: < VIN pin* 0.3

FREQ high : Frequency = 1.2MHz
FREQ low : Frequency = 640KHz

If the out put is for I/O port, should be add protection circuit for I/O short protection.



Compal Electronics, Inc.

Title: PWR- 12V

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Compal Electronics, Inc.

Title: **PWR- Reserve**

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
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11					
12					
13					
14					
15					
16					
17					
18					

Compal Electronics, Inc.

Title: PWR- PIR

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
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Compal Electronics, Inc.

Title: PIR (HW)

Size: Custom | Document Number: LA-LJ551PR02 | Rev: 0.2

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