MS-A6161 Ver:10

CPU:

Intel -Kaby Lake - U Platform

OnBoard Chipset:

HD Audio Codec:ALC887 CG

LAN:Intel WGI219V

SIO : NUVOTON NCT6104

CARD READER :Realtek RTS5249

Single Touch MER4485

Main Memory:

DDR4(2133MHz) * 1

Expansion Slots:

M.2 Slot Type 2230, Key E, * 1

PWM:

Controller:ON Semiconductor/NCP81206MNTXG 1+1+1 Phase

Controller:NB685GQ CPU_VTT

Controller:NB685GQ VCC_DDR

Other:

VGA * 1

eDP * 1

USB2.0 * 6(colay with USB 3.0 * 4)

USB3.0 * 4

SATA 3.0 * 1(HDD)

SATA 2.0 * 1(ODD)

LPT Port * 1

COM Port * 4

Card reader * 1(3 in 1)

Smart Card * 1

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MS-A616

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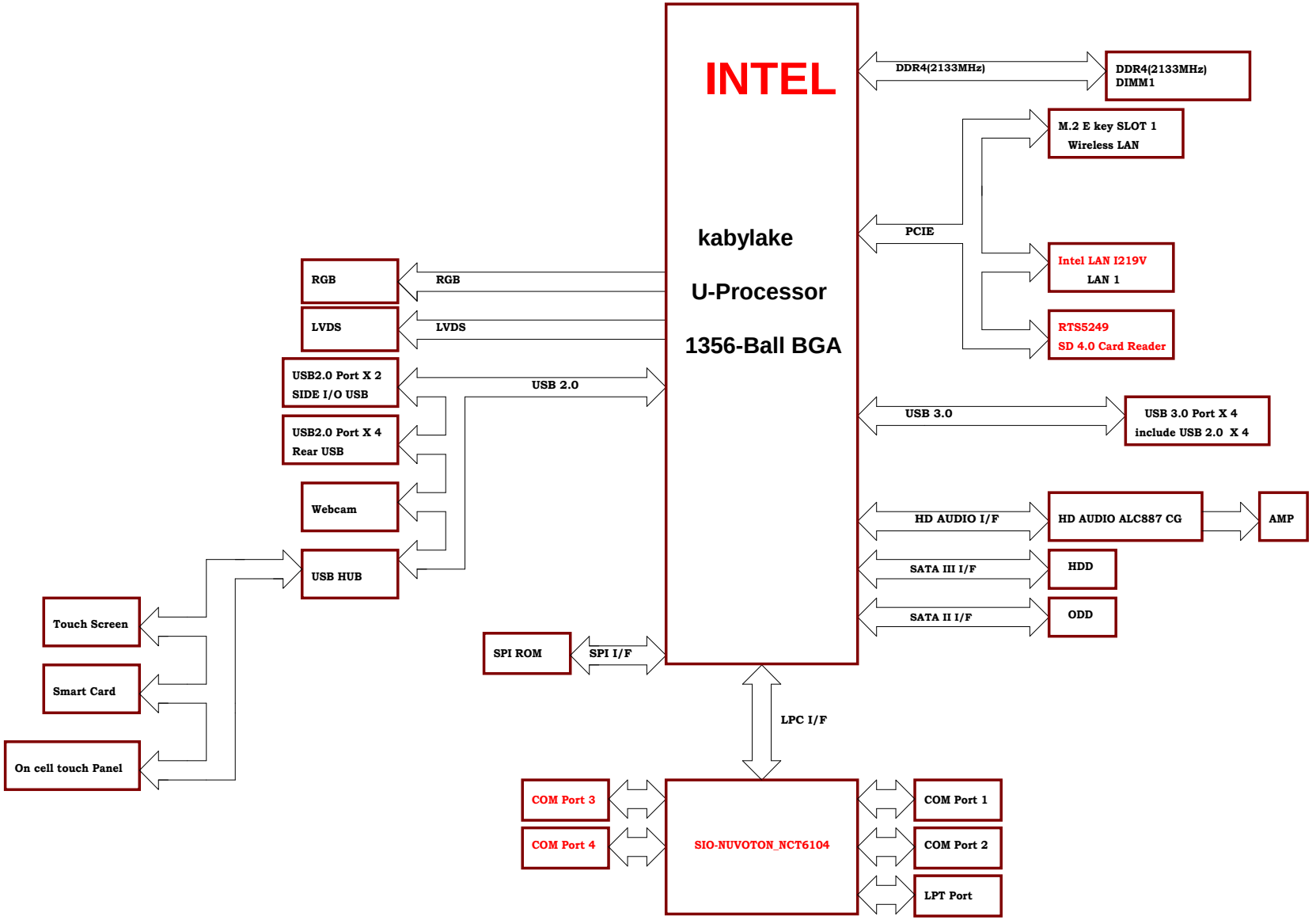
Block Diagram



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-A616	
Size: Custom	Document Description: Block Diagram	Rev: 10
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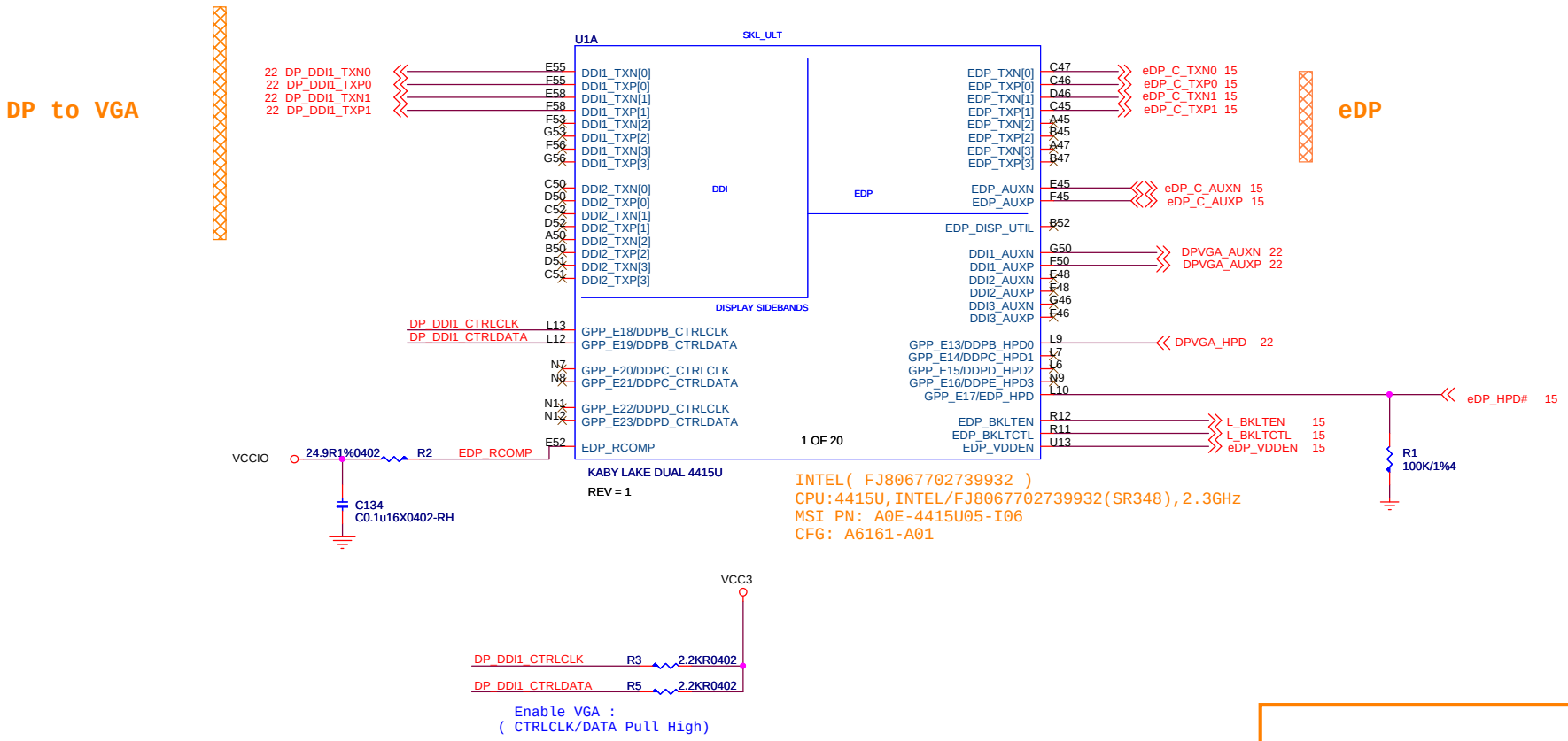

MSI	MICRO-STAR INT'L CO.,LTD	
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Size: B	Document Description: Kaby Lake-U (eDP,DDI)	Rev: 10
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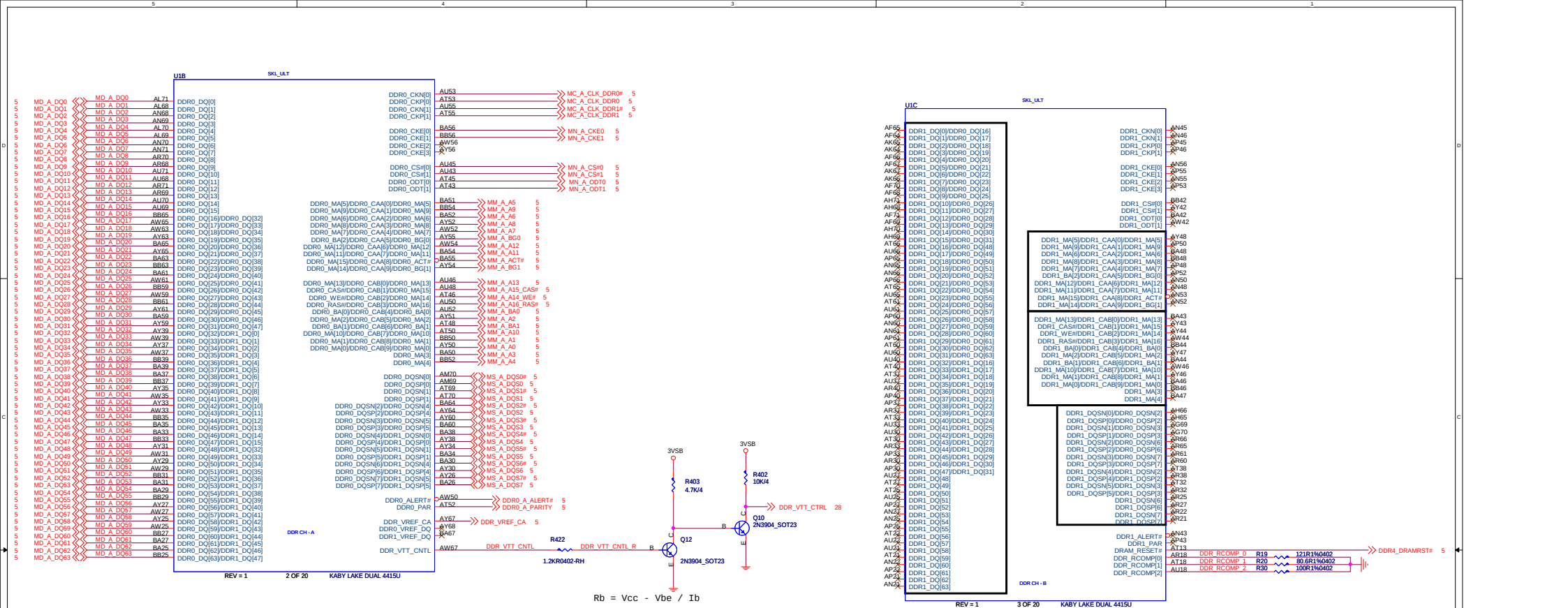

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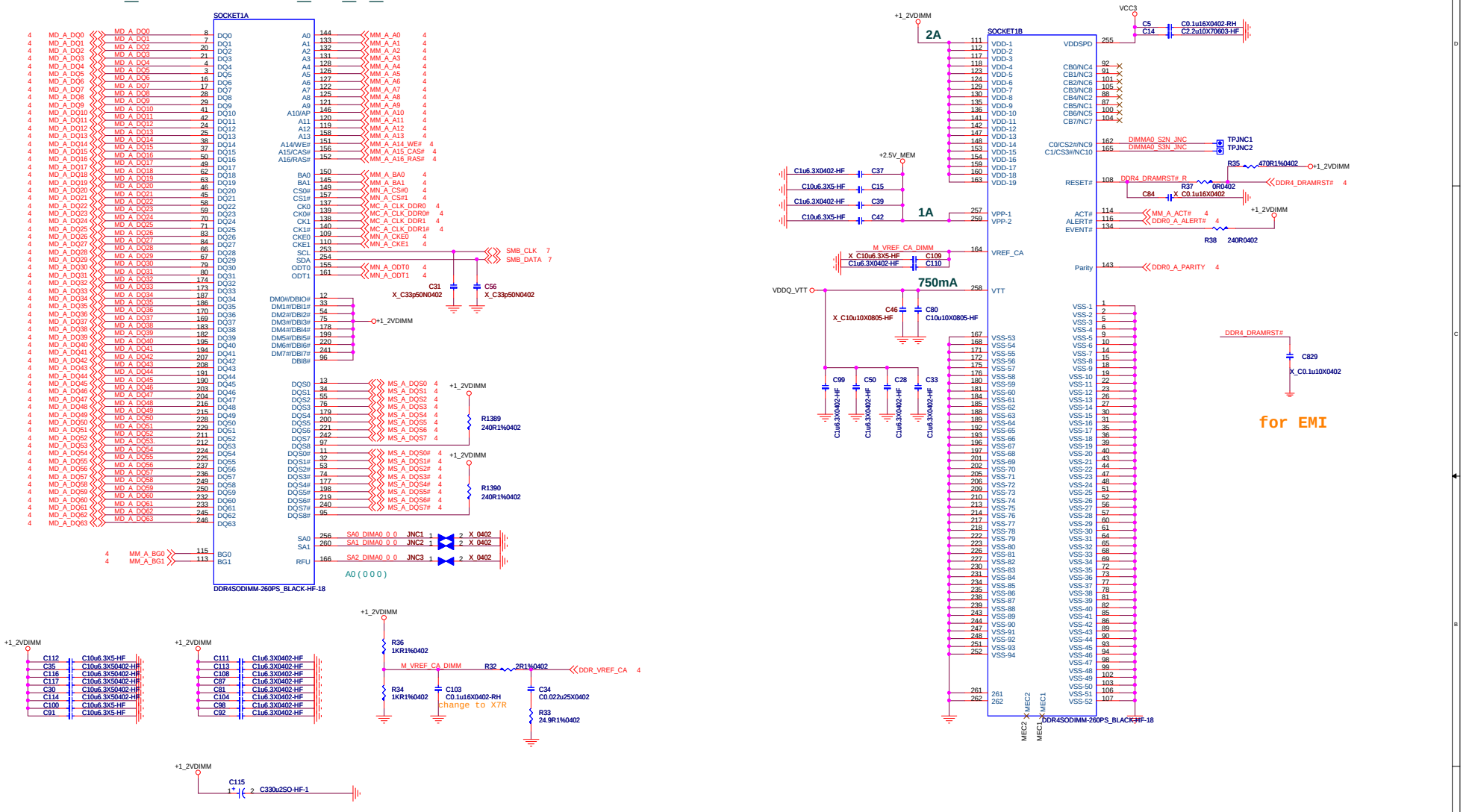
SODIMM_A0 (Standard) H:5.2 mm
MSI PN:N13-2600160-CK3
Footprint: DDR4_SODIMM260P_H5_2_6



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MS-A616		
Size: C	Document Description: DDR4_SODIMM_A0	Rev: 10
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Flash Descriptor Security Override	
HDA_SDO	Low = Disable High = Enable

JTLS1 — 3VSB — X_1KR0402_R118 — HDA_SDOUT_R — X_H1X2

RN15 — 8P4R-33R0402

23 HDA_RST# — HDA_RST#_R
23 HDA_BITCLK — HDA_BITCLK_R
23 HDA_SDOUT — HDA_SDOUT_R
23 HDA_SYNC — HDA_SYNC_R

C120 X_C10p50N0402
C101 X_C10p50N0402
C118 X_C10p50N0402
C119 X_C10p50N0402

U1G — SKL_ULT

AUDIO

HDA_SYNC_R — BA22 — HDA_SYNC/I2S0_SFRM
HDA_BITCLK_R — AY22 — HDA_BLK/I2S0_SCLK
HDA_SDOUT_R — BB22 — HDA_SDO/I2S0_TXD
23 HDA_SDIN0 — BA21 — HDA_SDI0/I2S0_RXD
AY21 — HDA_SDI1/I2S1_RXD
HDA_RST#_R — AW22 — HDA_RST#/I2S1_SCLK
J5 — GPP_D23/I2S_MCLK
AY20 — I2S1_SFRM
AW20 — I2S1_TXD

AK7 — GPP_F1/I2S2_SFRM
AK6 — GPP_F0/I2S2_SCLK
AK9 — GPP_F2/I2S2_TXD
AK10 — GPP_F3/I2S2_RXD

VCC3 — R120 X_1KR0402
23 SPKR — AW5 — GPP_B14/SPKR

H5 — GPP_D19/DMIC_CLK0
D2 — GPP_D20/DMIC_DATA0
D8 — GPP_D17/DMIC_CLK1
C8 — GPP_D18/DMIC_DATA1

7 OF 20

SDIO/SDXC

GPP_G0/SD_CMD — AB11
GPP_G1/SD_DATA0 — AB13
GPP_G2/SD_DATA1 — AB12
GPP_G3/SD_DATA2 — W12
GPP_G4/SD_DATA3 — W11
GPP_G5/SD_CD# — W10
GPP_G6/SD_CLK — W8
GPP_G7/SD_WP — W7

GPP_A17/SD_PWR_EN#/ISH_GP7 — BA9
GPP_A16/SD_1P8_SEL — BB9

SD_RCOMP — AB7 — RCOMP_SD — R119 — 200R1%0402

GPP_F23 — AF13

REV = 1 — KABY LAKE DUAL 4415U

30 H_PROCHOT#

1V_VCCST — R121 1KR0402
VCCIO — R122 1KR0402
R123 499R1%0402

TPJNC7 — H_CATERR#JNC — D63 — CATERR#
18 H_PECI — A54 — PECI
PROCHOT#_R — C65 — PROCHOT#
THERMTRIP# — C63 — THERMTRIP#
18 THERMTRIP# — A65 — SKTOCC#

C249 X_C0.1u16X0402
near U1D
EMI suggestion 2016.03.09

TP3 — C55 — BPM#[0]
TP4 — D55 — BPM#[1]
TP5 — B54 — BPM#[2]
TP7 — C56 — BPM#[3]

CPU MISC

A6 — GPP_E3/CPU_GP0
A7 — GPP_E7/CPU_GP1
BA5 — GPP_B3/CPU_GP2
AY5 — GPP_B4/CPU_GP3

R132 49.9R1%0402 PROC_ROPIRCOMP — AT16 — PROC_POPIRCOMP
R140 49.9R1%0402 PCH_OPIRCOMP — AU16 — PCH_OPIRCOMP
R139 49.9R1%0402 OPCE_RCOMP — H66 — OPCE_RCOMP
R138 49.9R1%0402 OPC_RCOMP — H65 — OPC_RCOMP

U1D — SKL_ULT

4 OF 20

JTAG

PROC_TCK — B61 — CPU_TCK — R141 51R1%0402
PROC_TDI — D60 — CPU_TDI — R125 51R1%0402
PROC_TDO — A61 — CPU_TDO — R126 51R1%0402
PROC_TMS — C60 — CPU_TMS — R127 51R1%0402
PROC_TRST# — B59 — CPU_TRST# — TP6

VCCIO

PCH_JTAG_TCK — B56 — PCH_JTAGTCK
PCH_JTAG_TDI — D59 — PCH_JTAGTDI — R128 51R1%0402
PCH_JTAG_TDO — A56 — PCH_JTAGTDO — R129 51R1%0402
PCH_JTAG_TMS — C59 — PCH_JTAGTMS — R130 51R1%0402
PCH_TRST# — C61 — CPU_TRST_N
JTAGX — A59 — PCH_JTAGX — R131 51R1%0402

VCCIO

CPU_TRST_N — R137 X_51R1%0402
PCH_JTAGTCK — R136 51R1%0402

REV = 1 — KABY LAKE DUAL 4415U

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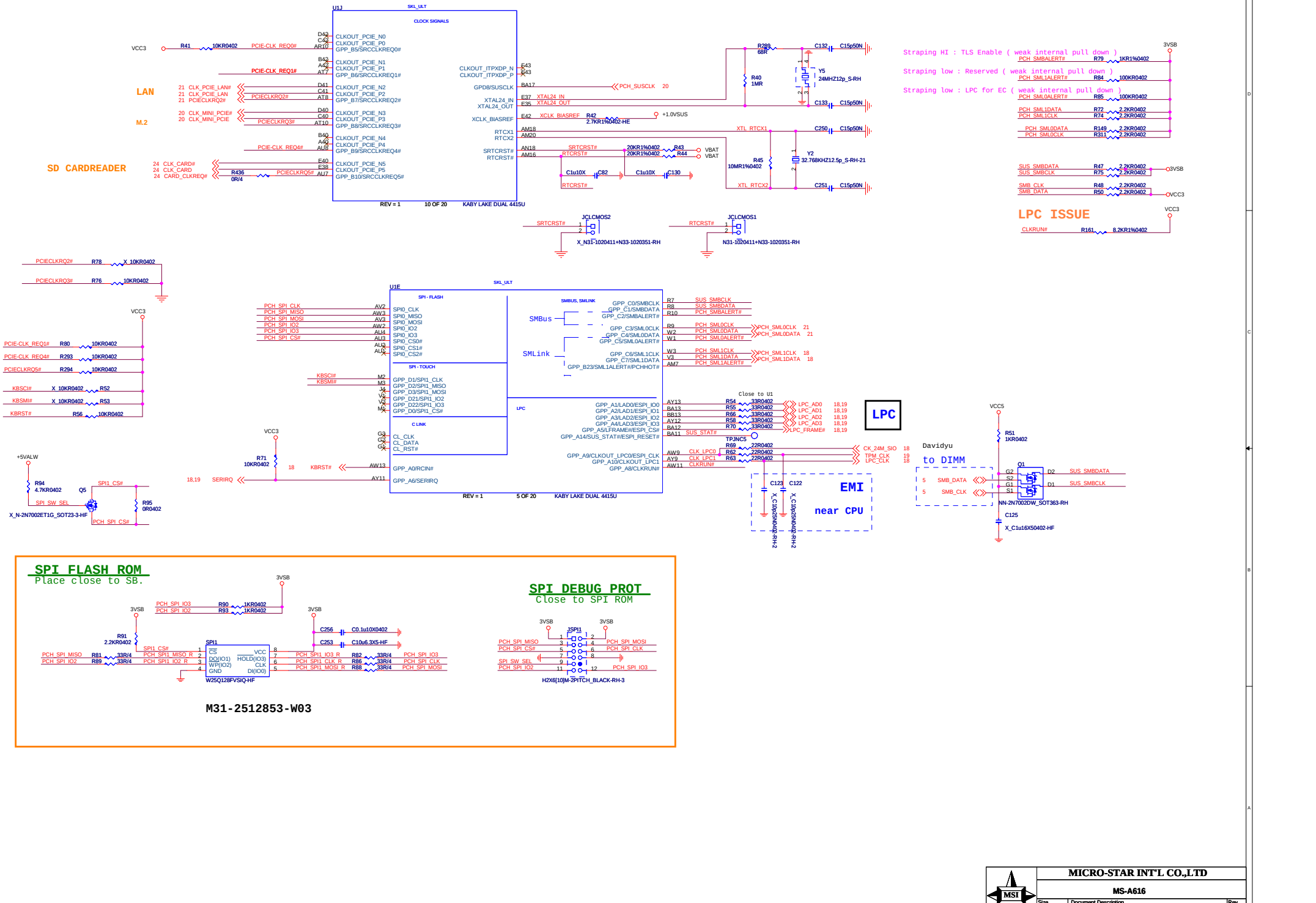
U1J
SKL_ULT
CLOCK SIGNALS
LAN
M.2
SD CARDREADER
REV = 1
10 OF 20
KABY LAKE DUAL 4415U
Straping HI : TLS Enable (weak internal pull down)
Straping low : Reserved (weak internal pull down)
Straping low : LPC for EC (weak internal pull down)
LPC ISSUE
U1E
SPI - FLASH
SPI - TOUCH
C LINK
SMBUS, SMLINK
SMBus
SMLink
LPC
REV = 1
5 OF 20
KABY LAKE DUAL 4415U
Close to U1
EMI
near CPU
Davidyu
to DIMM
SPI_FLASH_ROM
Place close to SB.
W25Q128FVSIQ-HF
M31-2512853-W03
SPI_DEBUG_PROT
Close to SPI ROM
H2X6[10]M-2PITCH_BLACK-RH-3
MICRO-STAR INT'L CO.,LTD
MS-A616
Kaby Lake-U (CLK,LPC,SPI)
Wednesday, January 11, 2017

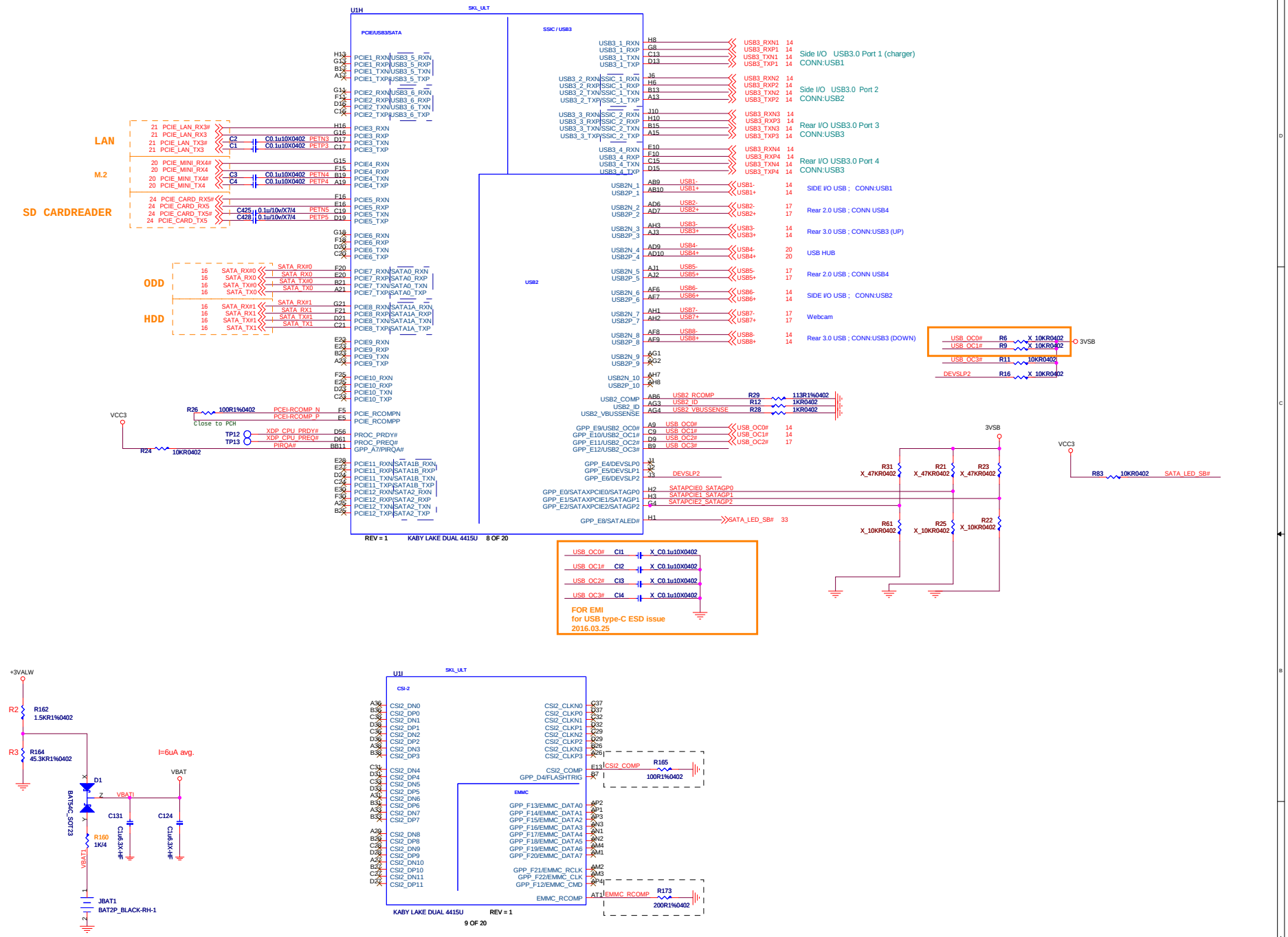

Figure 29-2, shows one option utilizing a resistor divider network (R2 and R3) at VCCDSW_3p3 to drop the voltage and meet the max VCCRTC < 3.2V specification. The cost impact is small but this solution will result in an ~0.25 mW power loss in non-G3 state. In this solution, the dual diodes must be in a single Si package to ensure matched Vf characteristics. Initial resistor value recommendations are R2=1.5 KΩ and R3=45 KΩ.

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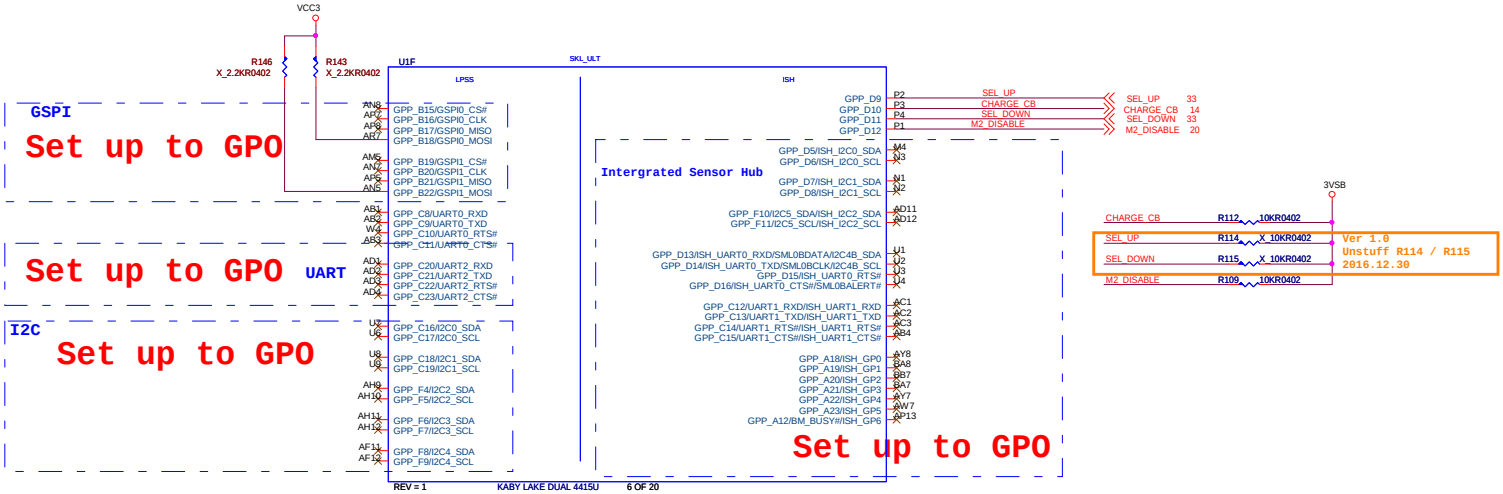
GPIO27
Connect this signal on PCH to EC. This signal resides in the DSW rail and can be used to wake the system from Deep Sx.

GPIO12
This signal may optionally be connected to a switch to turn 3.3-V PHY power off when LAN is disabled for additional power savings.

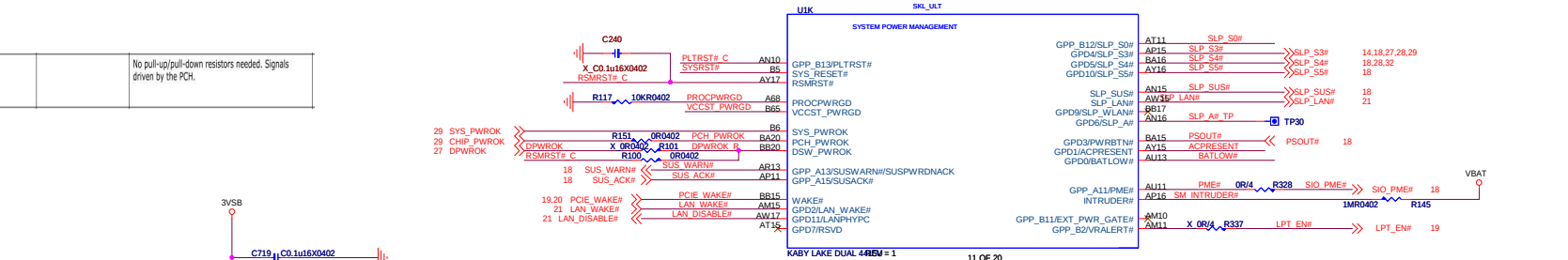
GPIO15:
This signal has an integrated weak pull-down (20KΩ nominal) resistor to enable Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality.

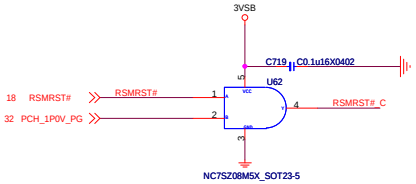
GPIO71: This power can be shut off when PCH drives HSIOPC low during S0 idle condition. external resistor is required for out put de -glitch during power sequencing.

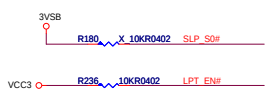
GPIO81:This signal has an integrated weak pull-down (20KΩ nominal) to enable reboot on TCO Timer expiration.
Pull up to VCC3_3 through a 1K to 8.2KΩ ± 5% resistor to disable this capability.

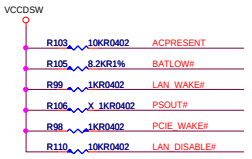


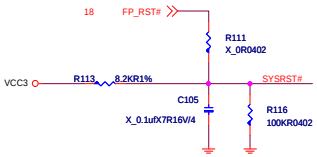
SLP_S3#		No pull-up/pull-down resistors needed. Signals driven by the PCH.
SLP_S4#		
SLP_S5#		

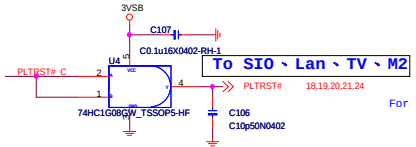


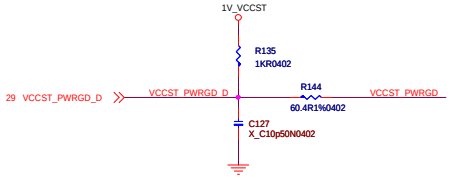












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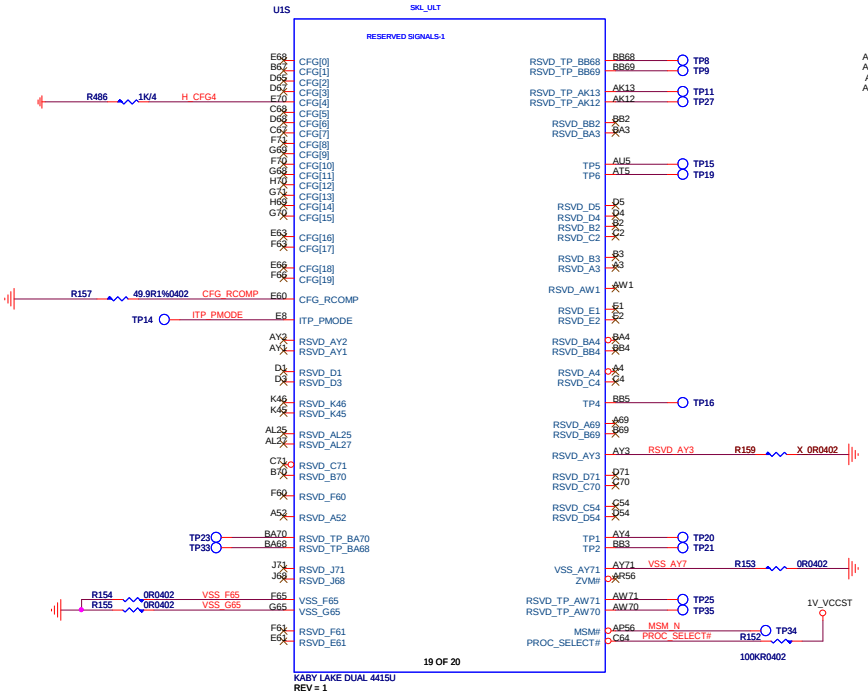
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (NC in DG) 0:Enabled; An external Display Port device is connected to the Embedded Display Port (Pull down to GND through a 1K ± 5% resistor)

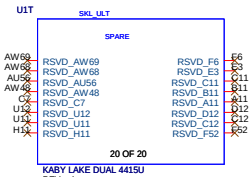
Functional Strap Definitions (Sheet 1 of 3)

Signal	Usage	When Sampled	Comment
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap. **Notes:** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. **Notes:** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
SMBALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). **Bit 6 — Boot BIOS Destination** 0 — SPI (Default) 1 — LPC **Notes:** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
SMLOALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected for EC. (Default) 1 = **eSPI** is selected for EC. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SPI0_MOSI	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SML1ALERT# / PCHHOT# / GPP_B23	Reserved	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.





RSVD		All the RSVD pins should be left unconnected (floating) on the board.

Functional Strap Definitions (Sheet 3 of 3)

Signal	Usage	When Sampled	Comment
HDA_SDO/ I2S_TXD0	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. **Notes:** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Asserting HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel Management Engine after the next reset and disable runtime Intel ME functions. This strap should not be asserted after manufacturing/debug. 3. This signal is in the primary well.
DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. **Notes:** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. **Notes:** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.

Signal Name	Pin			Pin	Signal Name
VccSus3_3	1	o	o	2	SLP_S3#
VccDSW3_3	3	o	o	4	SLP_S5#
SLP_S4#	5	o	o	6	SLP_A#
VccDSW3_3	7	o	o	8	GND
RTCRST#	9	o	o	10	Ground for RTCRST#
PWRBTN#	11	o	o	12	Ground for PWRBTN#
SYS_RESET#	13	o	o	14	Ground for SYS_RESET#
SLP_S0#	15	o	o	16	NC
NC	17	o		18	NC

Number	Name	Intel®APS3 Sampling Wire Labels
13	+V3.3A	VCC_Sus/S0
9	PM_SLP_S3_N	S3
11	PM_SLP_S4_N	S4
5	PM_SLP_S5_N	S5
24	PM_SLP_M_N	M1/MOFF
21	+V3.3A_DSW	INEX1(Deep S4/5)
8	+V3.3A_DS3	INEX2(Deep S3)

Note: Make sure you connect all 6 cables (**Sus, S3, S4, S5, M1/OFF, GND**) to the relevant signals on the SUT. Otherwise you will not be able to check the system's power state or perform power tests.

In addition to these signals, you can also sample additional signals on the platform by connecting them to the following cables on the main cable:

- **INEX1 (Deep S4/5)**
- **INEX2 (Deep S3)**
- **INEX3**
- **INEX4**
- **INEX5**

Note: If you do not connect all of the additional cables (**INEX1 (Deep S4/5), INEX2 (Deep S3), INEX3, INEX4, INEX5**) to the relevant signals, **you must connect the unconnected cables to GND**; do not leave them unconnected. Unconnected cables may give unexpected results.

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Size C	Document Description: Kaby Lake-U (CFG / RVSD)		Rev 10
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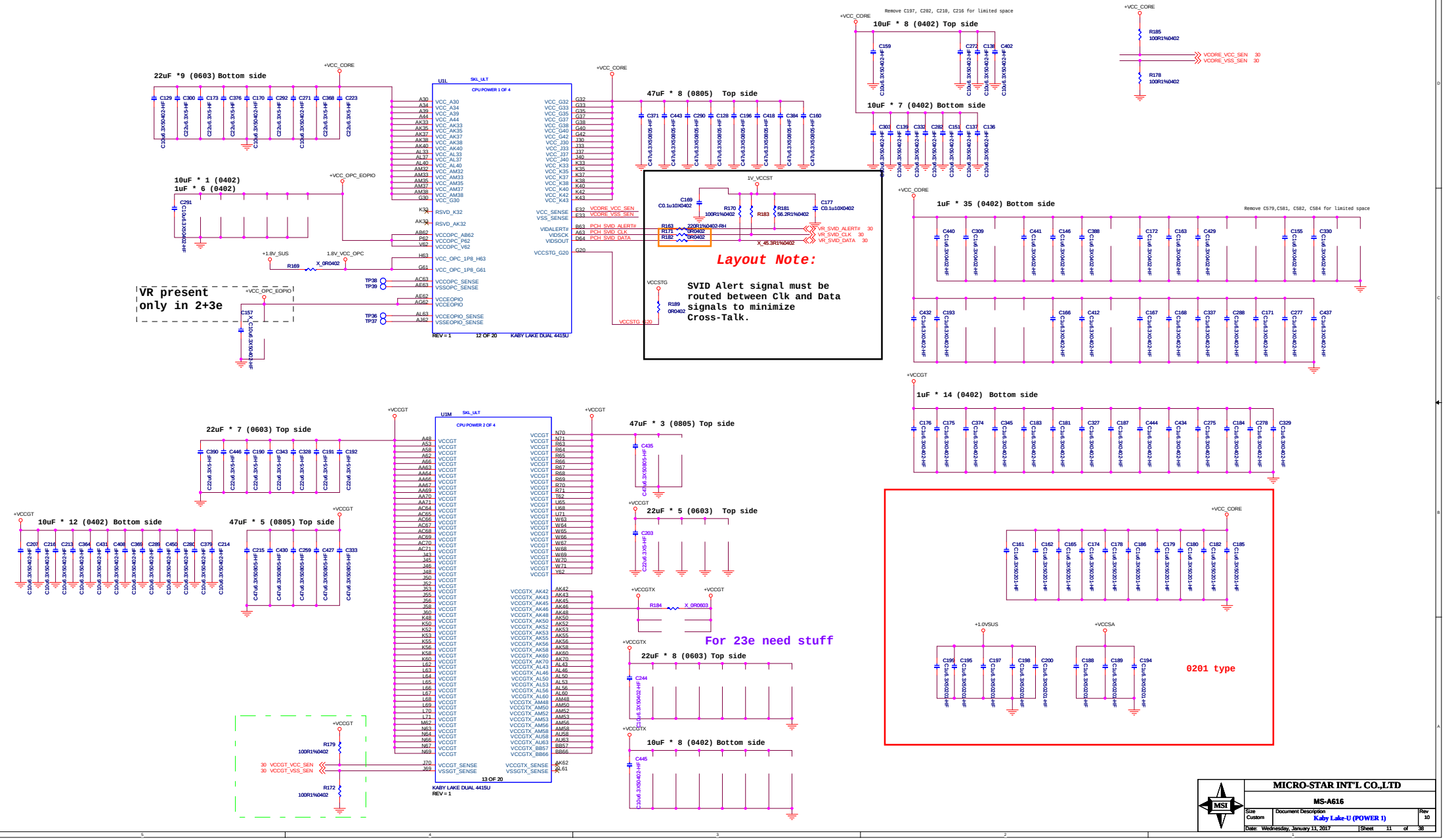
22uF *9 (0603) Bottom side
10uF * 1 (0402)
1uF * 6 (0402)
VR present only in 2+3e
U1L SKL_ULT
CPU POWER 1 OF 4
REV = 1
12 OF 20
KABY LAKE DUAL 4415U
47uF * 8 (0805) Top side
10uF * 8 (0402) Top side
Remove C197, C282, C210, C216 for limited space
10uF * 7 (0402) Bottom side
1uF * 35 (0402) Bottom side
Remove C579,C581, C582, C584 for limited space
1uF * 14 (0402) Bottom side
Layout Note:
SVID Alert signal must be routed between Clk and Data signals to minimize Cross-Talk.
22uF * 7 (0603) Top side
10uF * 12 (0402) Bottom side
47uF * 5 (0805) Top side
47uF * 3 (0805) Top side
22uF * 5 (0603) Top side
22uF * 8 (0603) Top side
10uF * 8 (0402) Bottom side
For 23e need stuff
0201 type
MICRO-STAR INT'L CO.,LTD
MS-A616
Kaby Lake-U (POWER 1)
Wednesday, January 11, 2017

10uF * 4 (0402)
22uF * 3 (0603)
10uF * 2(0402) unstuff
1uF *4 (0402) unstuff

10uF * 2 (0402) Bottom side

1uF * 4 (0402) Top side/Bottom side

Remove C591 for limited space

Remove C592,C593, C594, C595 for limited space

10uF * 6 (0402) Top side

1uF * 7 (0201) Bottom side

10uF * 7 (0402) Bottom side

KABY LAKE DUAL 4415U 14 OF 20
REV = 1

KABY LAKE DUAL 4415U 15 OF 20
REV = 1

1.8v well only

Check
The CORE_VID[0:1] signal is used by external VRs to indicate the final settling voltage for VCCPRIM_CORE rail.

As close as possible place these Caps at each ball out of CPU

Name	Description
VCCPRIM_CORE	**Core Logic Primary Well:** This rail scales from 0.85V to 1.0V.
VCCPRIM_1p0	**Primary Well 1.0V:** For I/O blocks, ungated ISH SRAM power, USB AFE Digital Logic, JTAG, Thermal Sensor and MIPI DPHY.
VCCSRAM_1p0	**SRAM Primary Well 1.0V:** Dedicated SRAM rail and can have on board power down gate control.
VCCMPHYAON_1p0	**Mod PHY Always On Primary 1.0V**: Always on primary supply for PCIe/DMI/ USB3/SATA/MIPI MPHY logic
VCCMPHYGT_1p0	**Mod PHY Externally Gated Primary 1.0V**: Externally gated primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic.
VCCAMPHYPLL_1p0	**Analog supply for USB3, PCIe Gen 2/Gen 3, SATA3 and MIPI PLL 1.0V:** This rail is from externally gated domain. Filtering required.
VCCAPLLEBB_1p0	**PCIe* PLL EBB Primary 1.0:** EBB contains primary supply for PCIe PLL dividers and lane drivers.
VCCAPLL_1p0	**Analog supply for OPI, USB2 and Audio PLL Primary 1.0V:** Filtering required.
VCCCLK1, VCCCLK2, VCCCLK3, VCCCLK4, VCCCLK5, VCCCLK6	**Clock Buffers Primary 1.0V**
VCCPGPPA	**Group A Primary Well GPIOs 3.3V or 1.8V**
VCCPGPPB	**Group B Primary Well GPIOs 3.3V or 1.8V**
VCCPGPPC	**Group C Primary Well GPIOs 3.3V or 1.8V**
VCCPGPPD	**Group D Primary Well GPIOs 3.3V or 1.8V**
VCCPGPPE	**Group E Primary Well GPIOs 3.3V or 1.8V**
VCCPGPPF	**Group F Primary Well GPIOs 1.8V only**
VCCPGPPG	**Group G Primary Well GPIOs 3.3V or 1.8V**
VCCATS	**Thermal Sensor Primary Well 1.8V**
VCCHDA	**HD Audio Power 3.3V, 1.8V, 1.5V.** For Intel High Definition Audio.
VCCSPI	**SPI Primary Well 3.3V or 1.8V**
VCCPRIM_3p3	**Primary Well 3.3V**
VCCRTCPRIM_3p3	**RTC Logic Primary Well 3.3V.** This power supplies the RTC internal VRM. It will be off during Deep Sx mode.
DCPDSW_1p0	**Deep Sx Well 1.0V:** This rail is generated by on die DSW low dropout (LDO) linear voltage regulator to supply DSW GPIOs, DSW core logic and DSW USB2 logic. Board needs to connect 1 uF capacitor to this rail and power should NOT be driven from the board. When primary well power is up, this rail is bypassed from VCCPRIM_1p0.
VCCDSW_3p3	**Deep Sx Well for GPD GPIOs and USB2**
DCPRTC	**RTC de-coupling capacitor only.** This rail should NOT be driven.

Name	Description
VCCRTC	**RTC Well Supply.** This rail can drop to 2.0V if all other planes are off. This power is not expected to be shut off unless the RTC battery is removed or drained. ***Note:*** VCCRTC nominal voltage is 3.0V. This rail is intended to always come up first and always stay on. It should NOT be power cycled regularly on non-coin battery designs. ***Note:*** Implementation should not attempt to clear CMOS by using a jumper to pull VCCRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
VSS	**Ground**

MICRO-STAR INT'L CO.,LTD

MS-A616

Size	Document Description	Rev
C	Kaby Lake-U (POWER 2)	10

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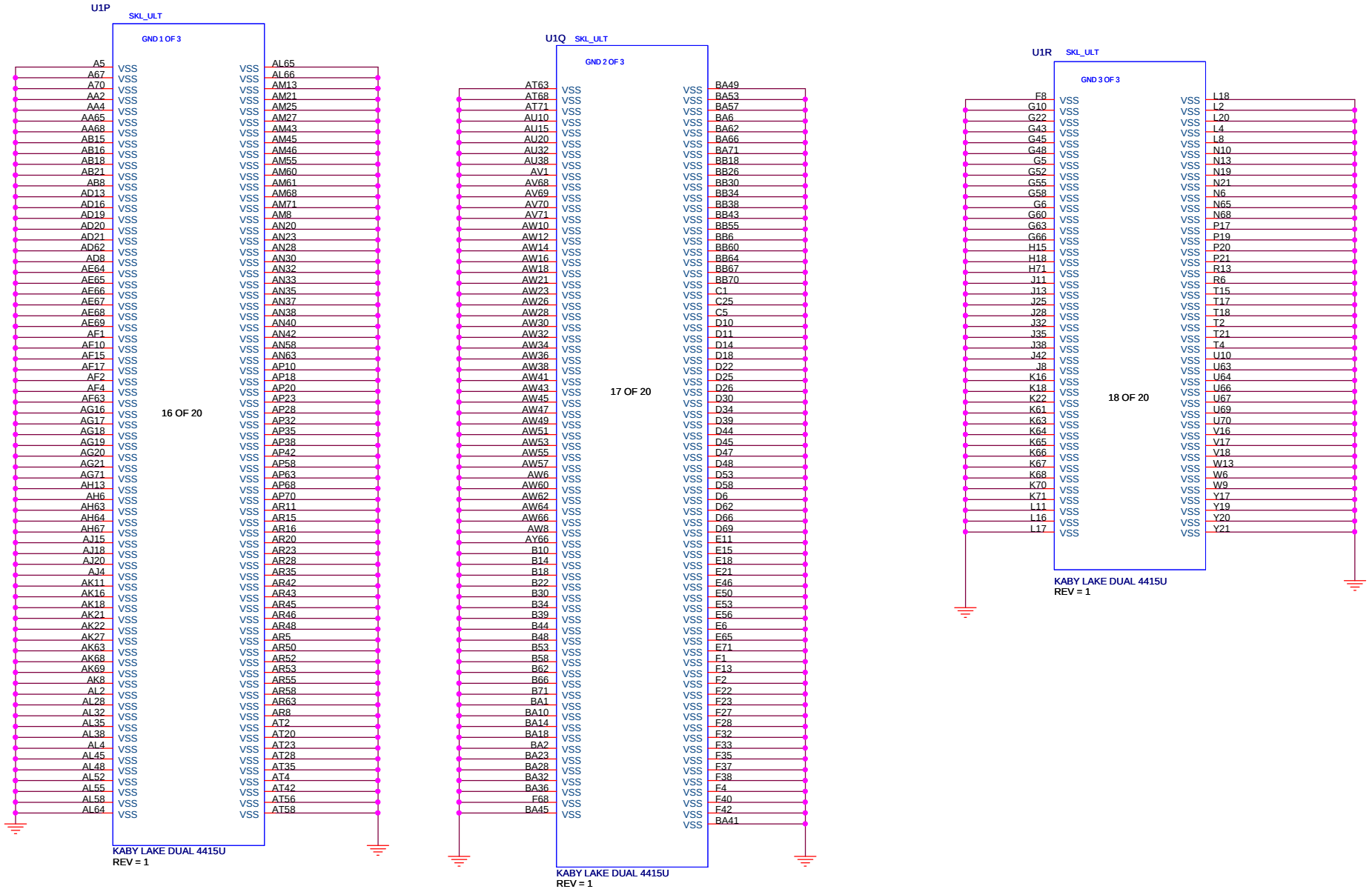

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MS-A616		
Size: B	Document Description: Kaby Lake-U (GND)	Rev: 10
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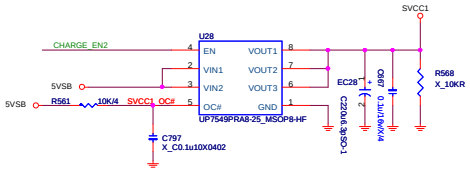
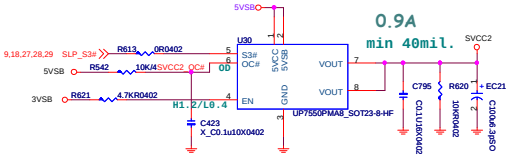
USB3.0

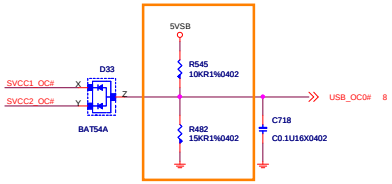
MAX 1.5A



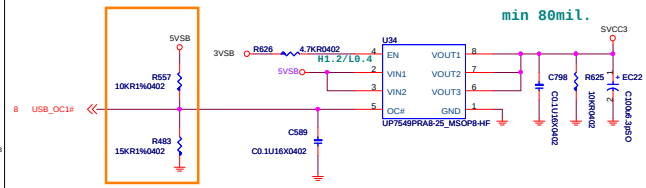


0.9A
min 40mil.

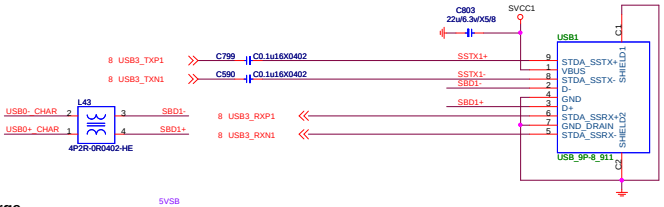
A616 Ver 1.0
U30 主料改I36-7550P09-U33

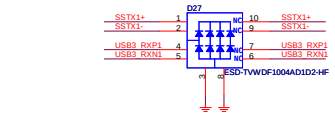


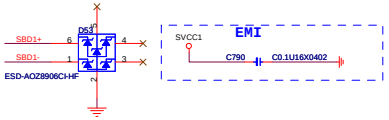
2A
min 80mil.



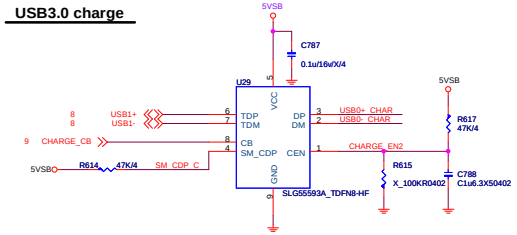
Side I/O USB3.0 (charger)

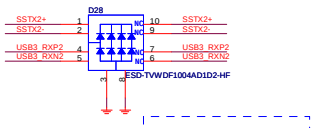




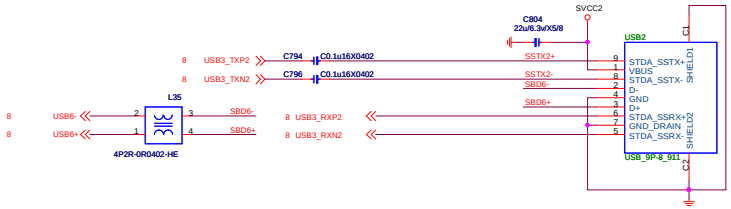


USB3.0 charge

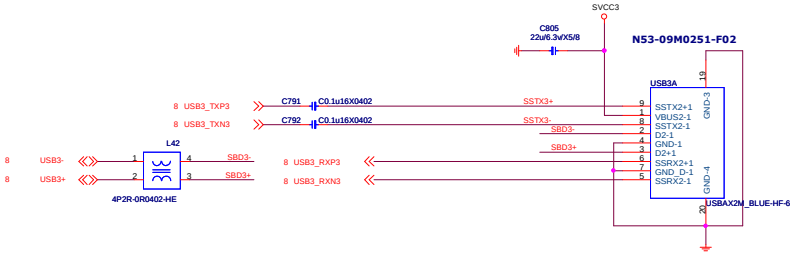


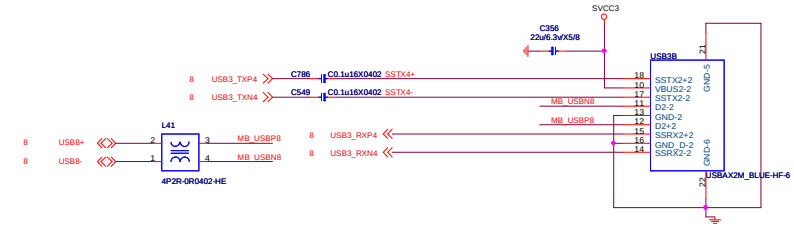


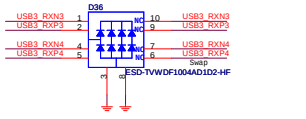
Side I/O USB3.0

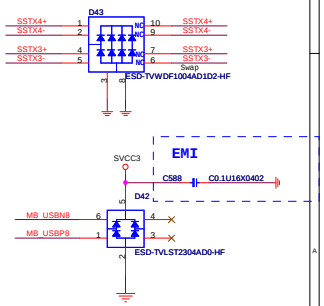


Rear I/O USB3.0









N53-18M0311-F02

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-A616	
Size: Custom	Document Description: USB30 Port	Rev: 10
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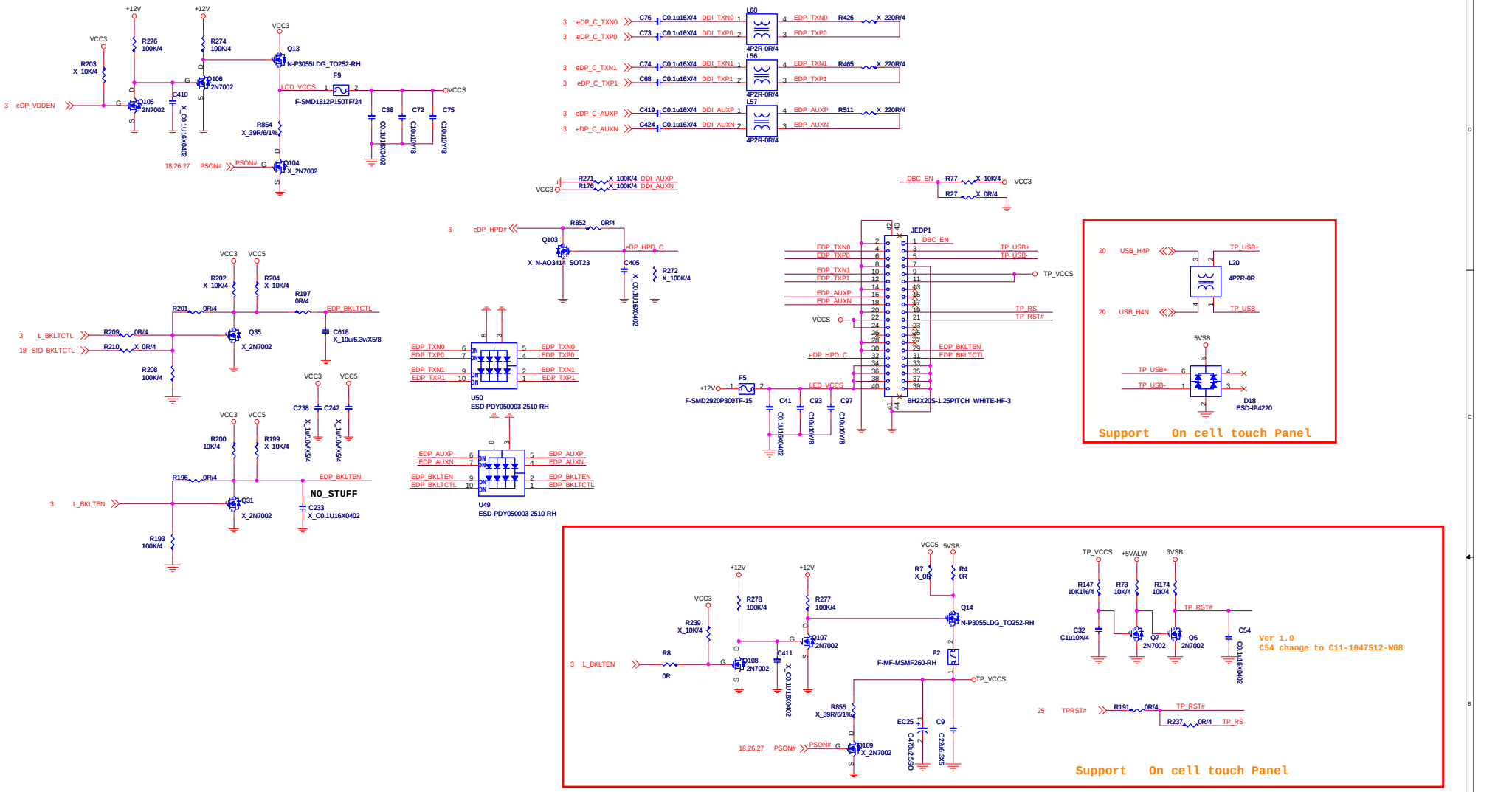

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MS-A616			
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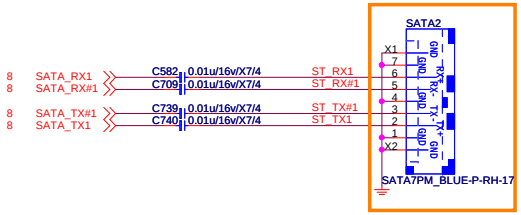
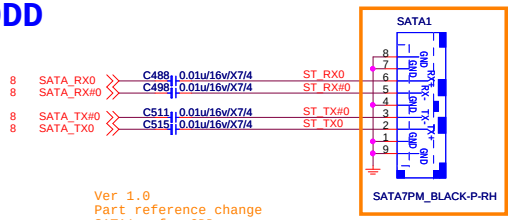
SATA HDD 2.5"

N5N-07M2101-H06(SATA1) BLUE



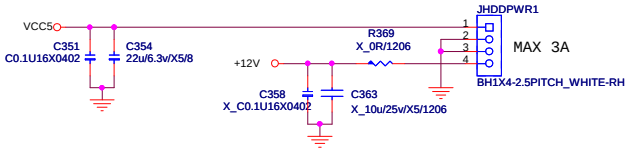
N5N-07M0221-H06(SATA2) BLACK

SATA ODD



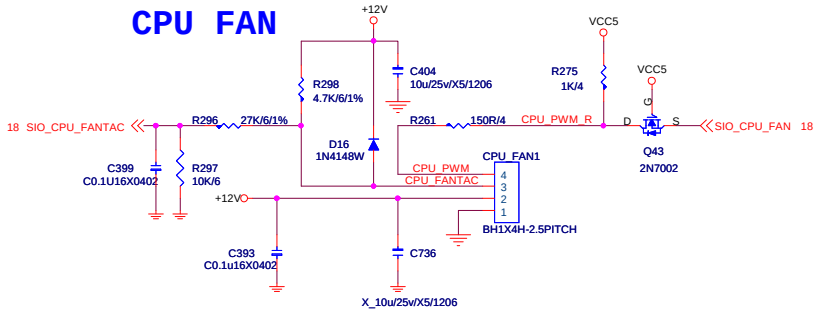
Ver 1.0
Part reference change
SATA1 : for ODD
SATA2 : for HDD

HDD Power



N32-1040D31-H06

CPU FAN



MICRO-STAR INT'L CO.,LTD		
MS-A616		
Size: Custom	Document Description: SATA / CPUFAN	Rev: 10
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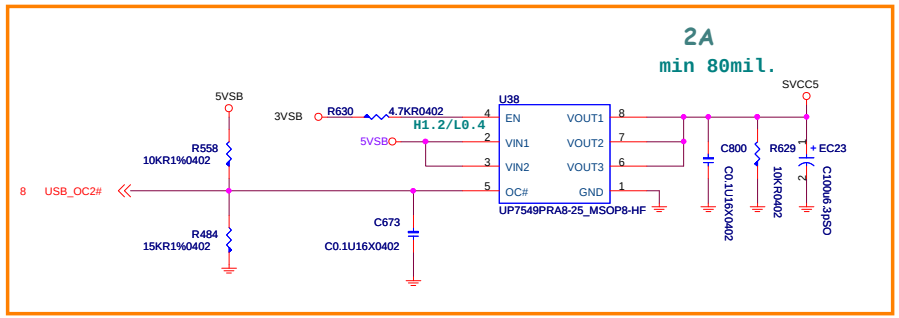
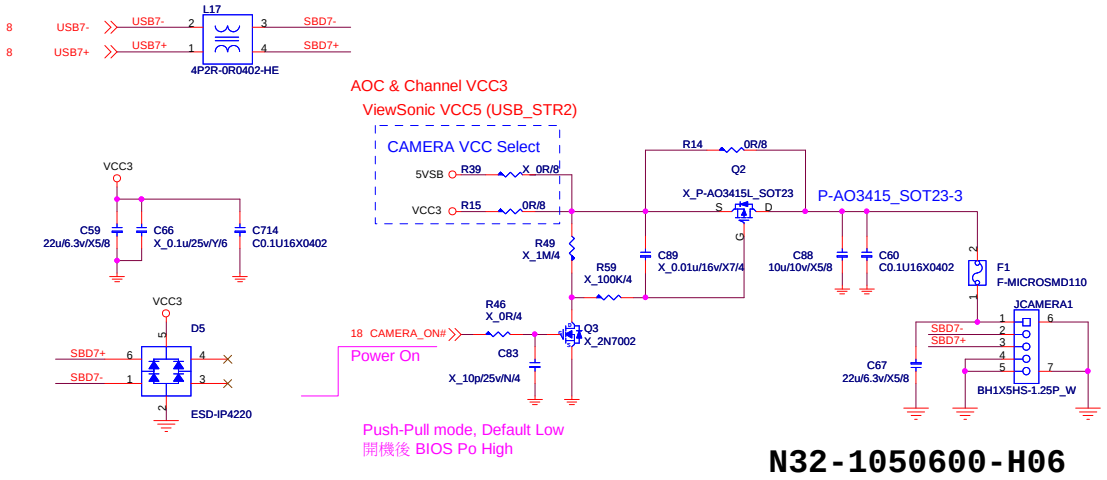
Rear I/O USB2.0 OC

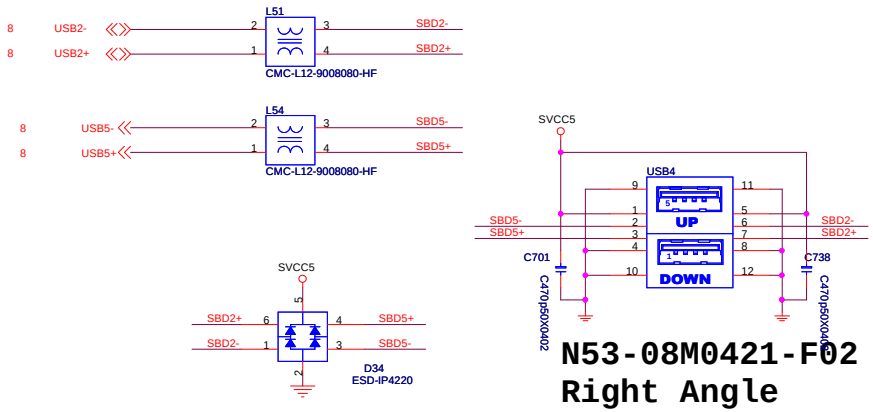


Webcam



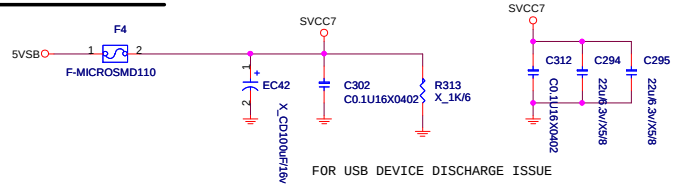
N32-1050600-H06

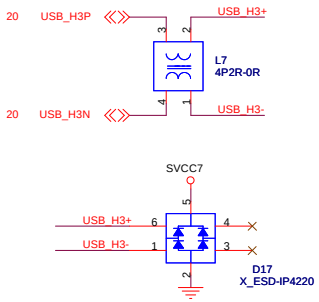
Rear I/O USB2.0

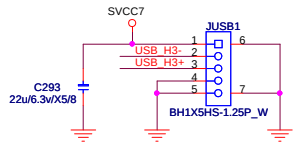


N53-08M0421-F02
Right Angle

for Smart Card







N32-1050600-H06

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MS-A616		
Size: Custom	Document Description: USB / WebCAM / SmartCard	Rev: 10
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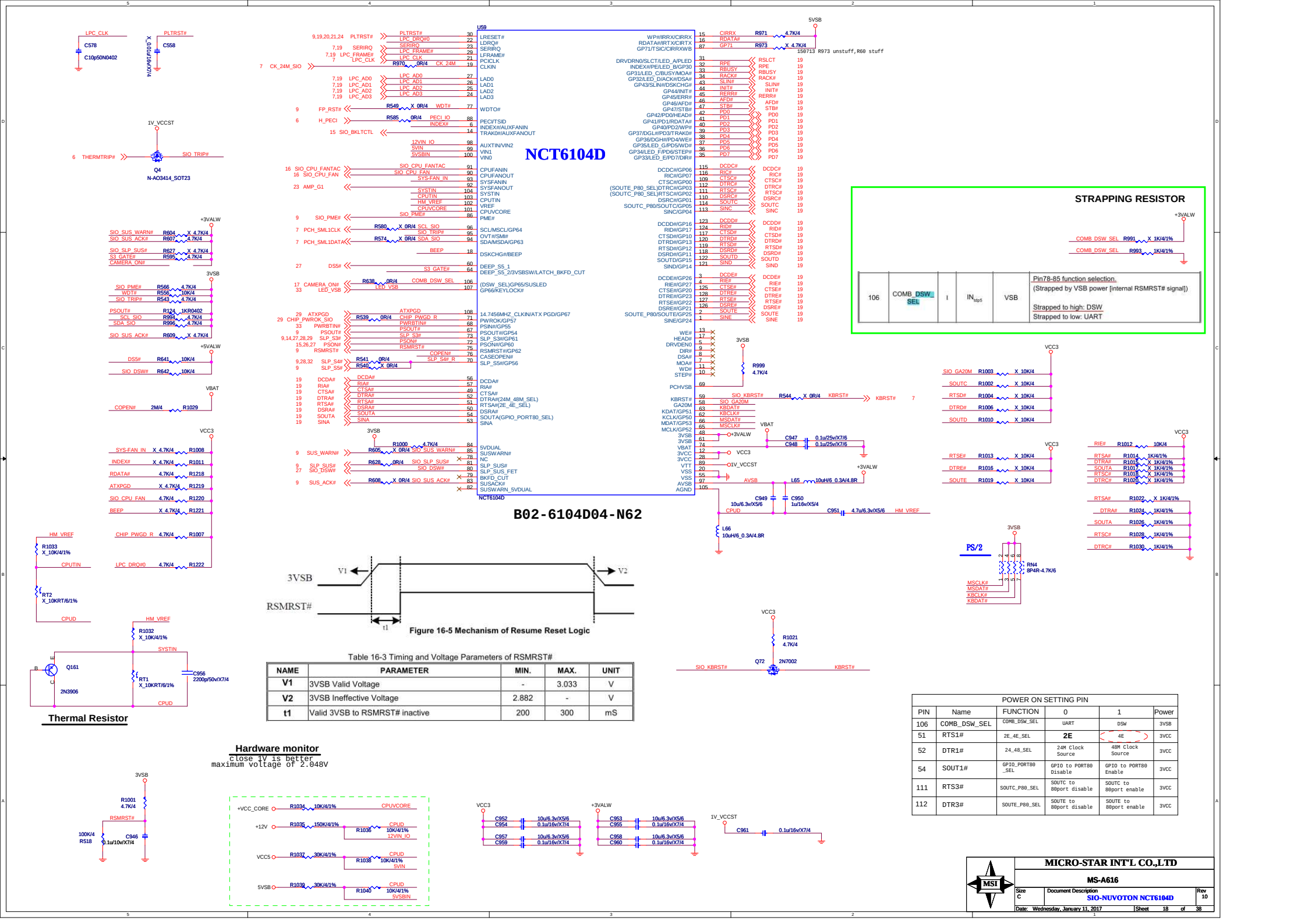

Figure 16-5 Mechanism of Resume Reset Logic

Table 16-3 Timing and Voltage Parameters of RSMRST#

NAME	PARAMETER	MIN.	MAX.	UNIT
V1	3VSB Valid Voltage	-	3.033	V
V2	3VSB Ineffective Voltage	2.882	-	V
t1	Valid 3VSB to RSMRST# inactive	200	300	mS

POWER ON SETTING PIN

PIN	Name	FUNCTION	0	1	Power
106	COMB_DSW_SEL	COMB_DSW_SEL	UART	DSW	3VSB
51	RTS1#	2E_4E_SEL	**2E**	4E	3VCC
52	DTR1#	24_48_SEL	24M Clock Source	48M Clock Source	3VCC
54	SOUT1#	GPIO_PORT80_SEL	GPIO to PORT80 Disable	GPIO to PORT80 Enable	3VCC
111	RTS3#	SOUTC_P80_SEL	SOUTC to 80port disable	SOUTC to 80port enable	3VCC
112	DTR3#	SOUTE_P80_SEL	SOUTE to 80port disable	SOUTE to 80port enable	3VCC

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MS-A616			
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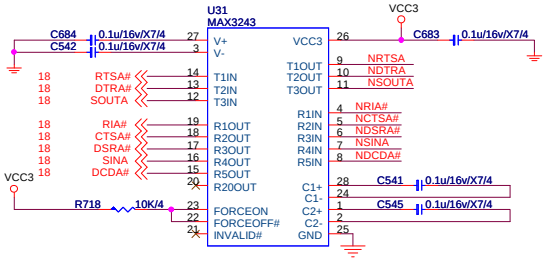
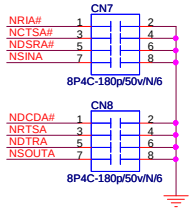
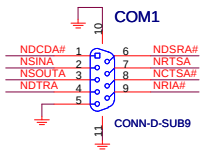
COM PORT 1

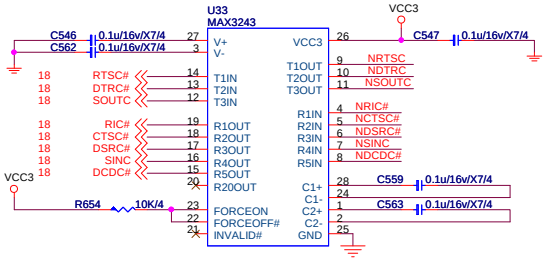


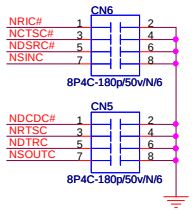


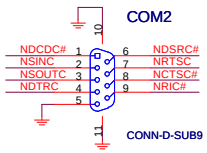


N51-09M0091-F02 change N51-09M0211-F02
2012.10.29

COM PORT 2

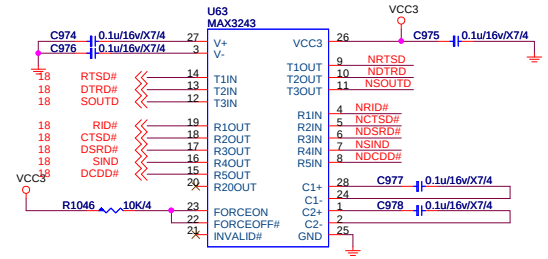


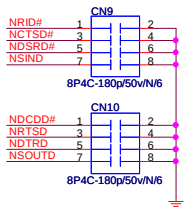




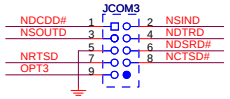
N51-09M0091-F02 change N51-09M0211-F02
2012.10.29

COM PORT 3



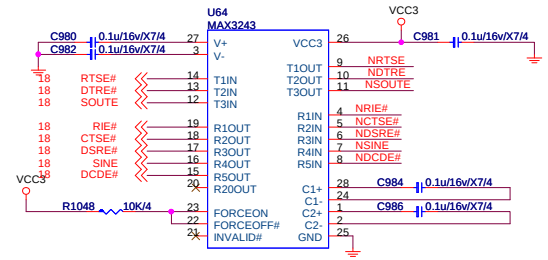


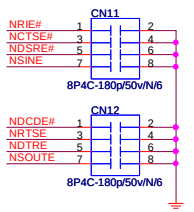
COM PORT 3



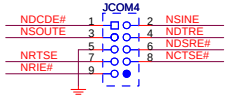
N31-2051331-H06

COM PORT 4



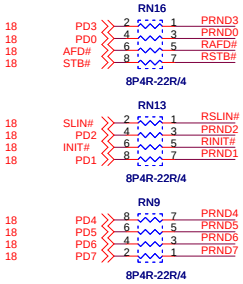


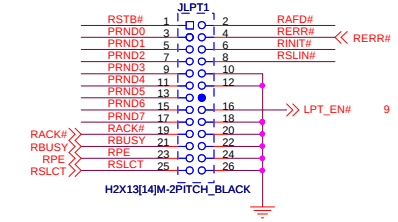
COM PORT 4



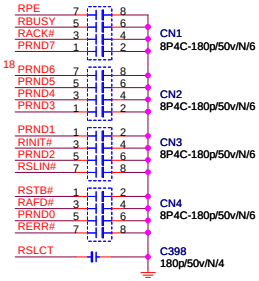
N31-2051331-H06

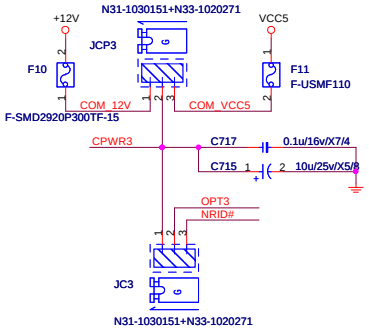
PARALLAL PORT





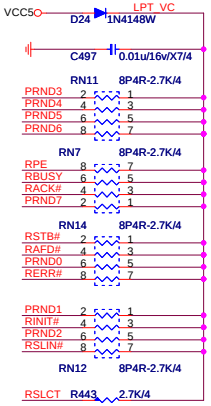
N31-2131281-H06
Vertical
Pitch 2.0 Pin Header



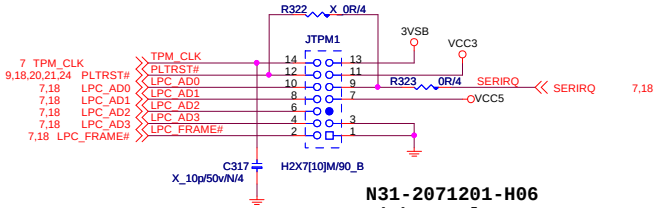


COM3 Function Select

JCP3	1-2	2-3
Fun	12V	5V
JC3	1-2	2-3
Fun	PWR	RIN

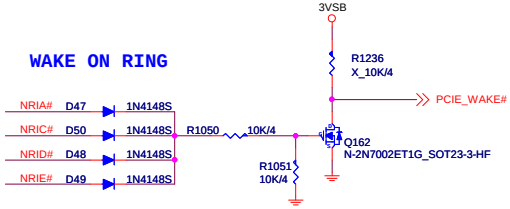


TPM / Port 80 HEADER



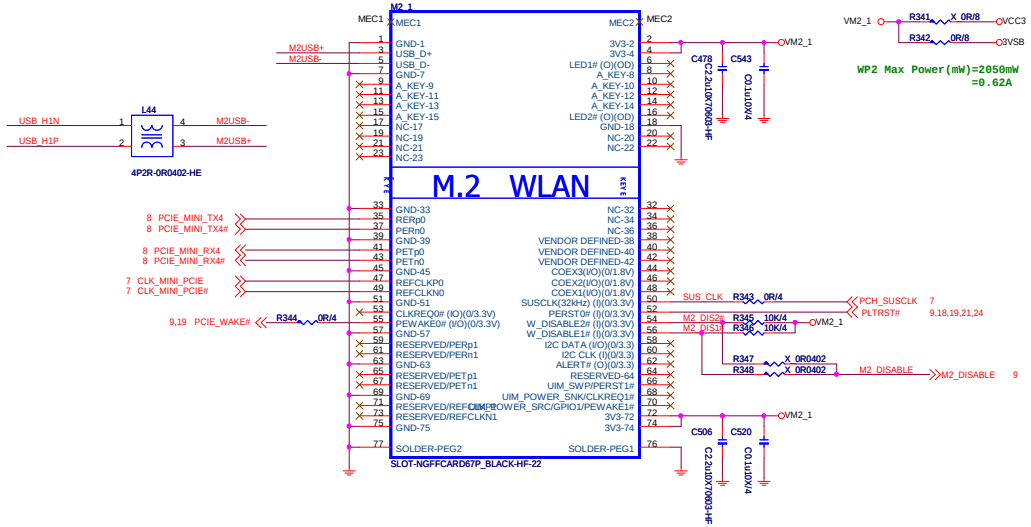
N31-2071201-H06
Right Angle

WAKE ON RING



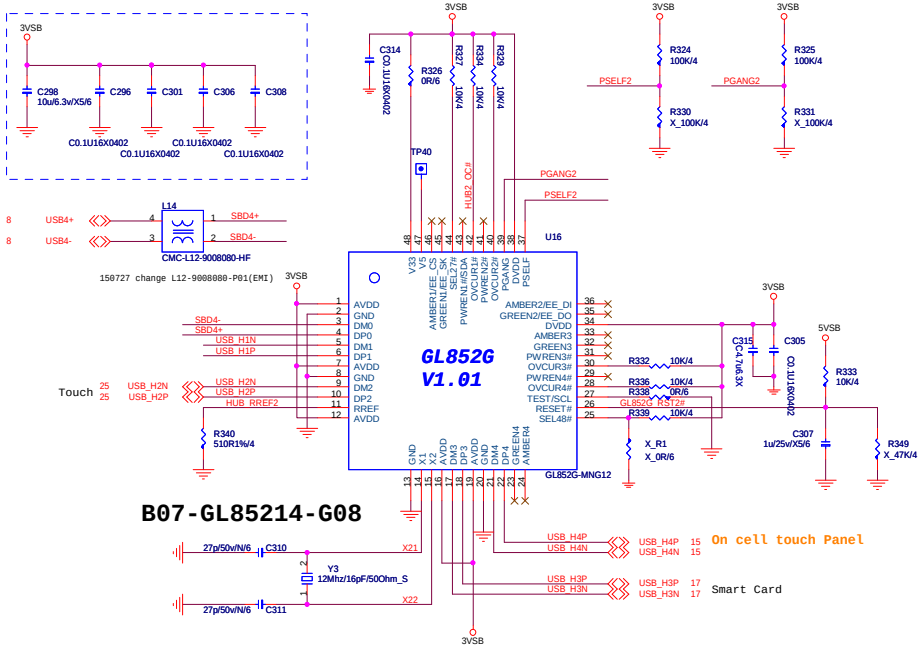
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-A616	
Size: Custom	Document Description: COM / LPT / TPM	Rev: 10
Date: Wednesday, January 11, 2017	Sheet 19 of 38	

M.2(USB/PCIE)_E key



for 8.5mm M2

H1 change to E2B-4389010-A89
footprint:H_R220D102_PTB



MICRO-STAR INT'L CO.,LTD		
MS-A616		
Size: C	Document Description: USB_HUB / M.2 Slot	Rev: 10
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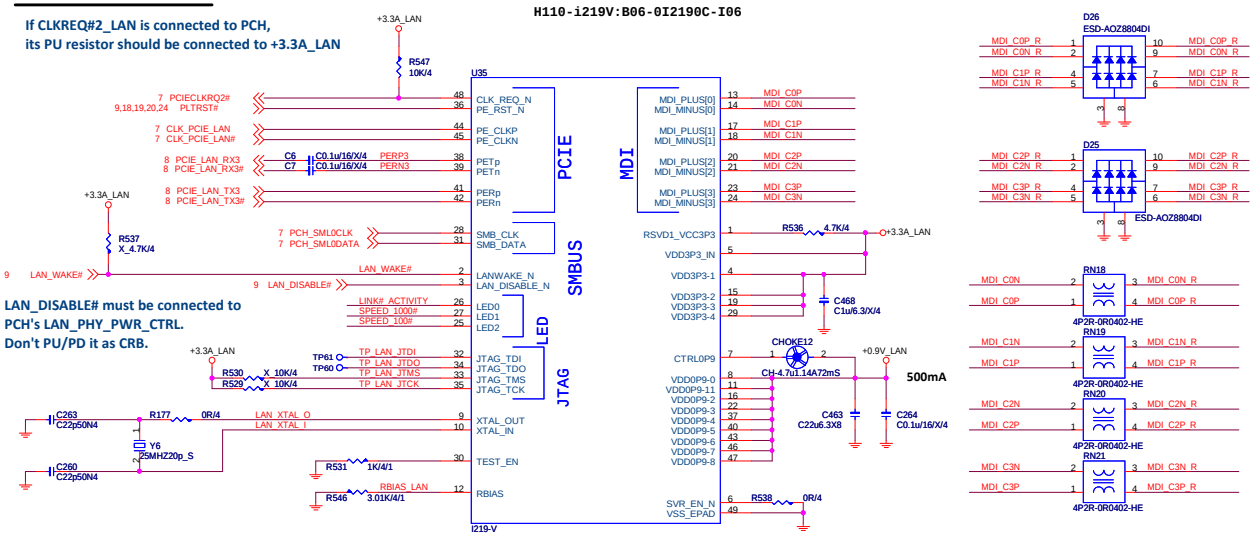
Intel LAN I219V

If CLKREQ#2_LAN is connected to PCH, its PU resistor should be connected to +3.3A_LAN

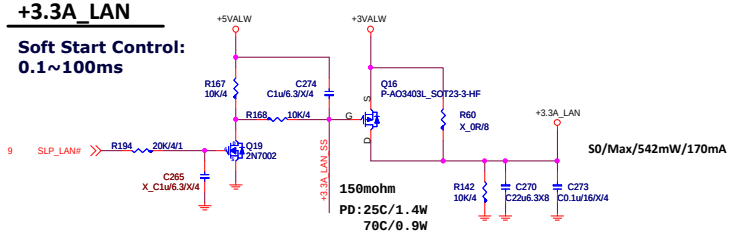
LAN_DISABLE# must be connected to PCH's LAN_PHY_PWR_CTRL. Don't PU/PD it as CRB.

H110-i219V:B06-0I2190C-I06



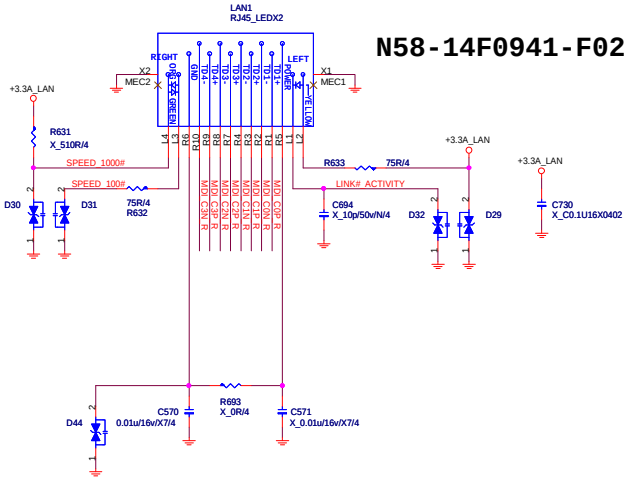
+3.3A_LAN

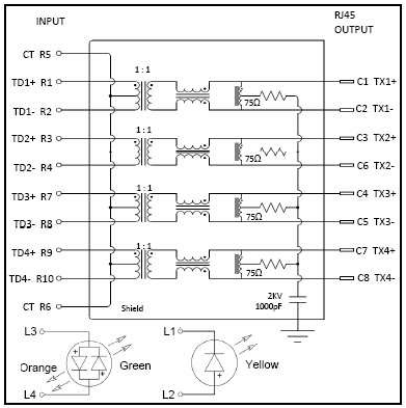
Soft Start Control: 0.1~100ms



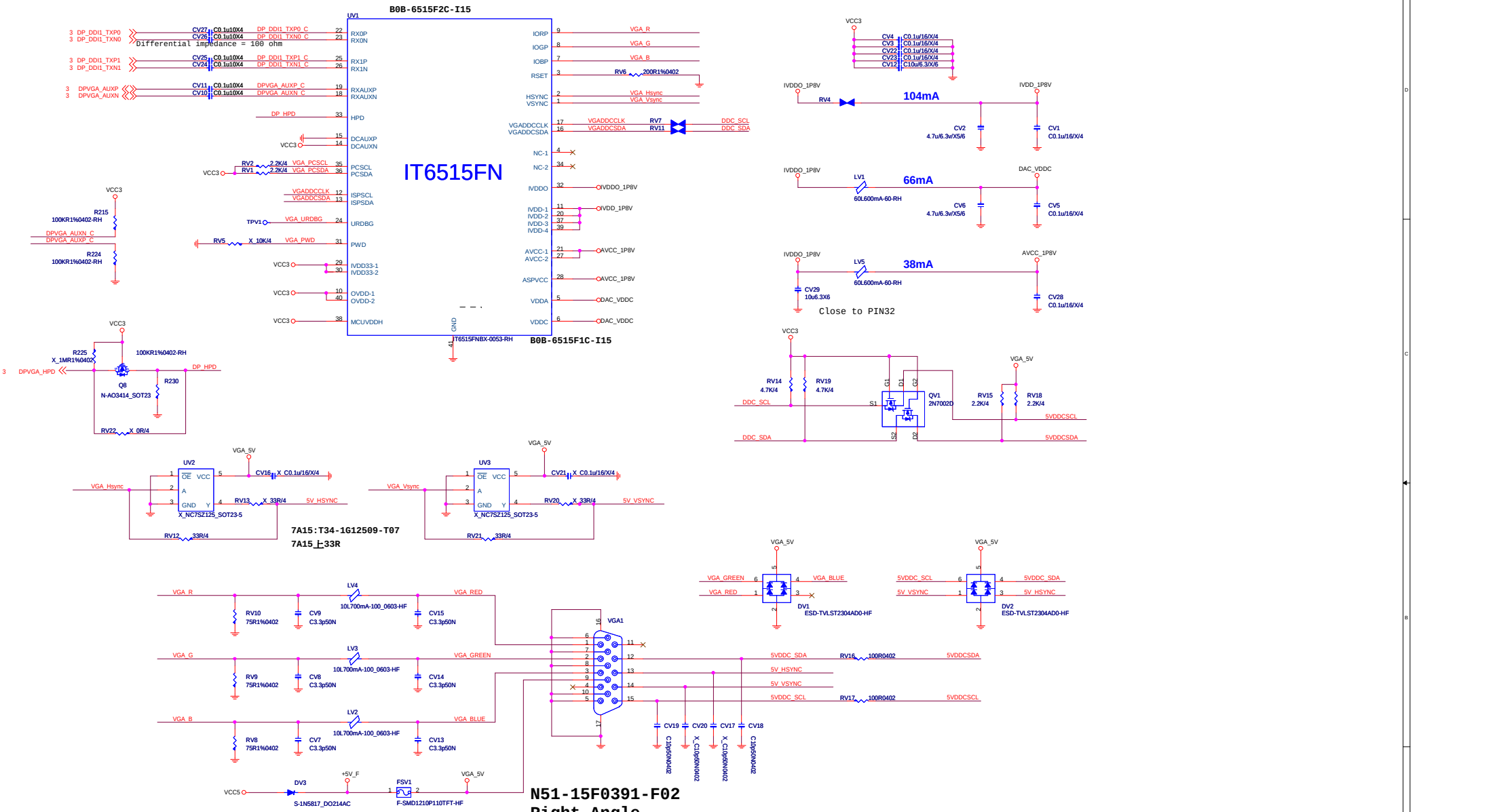
Place caps close to PHY

N58-14F0941-F02





MICRO-STAR INT'L CO.,LTD		
MS-A616		
Size C	Document Description LAN1- I219V	Rev 10
Date: Wednesday, January 11, 2017	Sheet 21 of 38	


B0B-6515F2C-I15
UV1
IT6515FN
B0B-6515F1C-I15
Differential impedance = 100 ohm
104mA
66mA
38mA
Close to PIN32
7A15:T34-1G12509-T07
7A15 ⊢33R
N51-15F0391-F02
Right Angle
MICRO-STAR INT'L CO.,LTD
MS-A616
DP to VGA-ITE IT6515
Wednesday, January 11, 2017

Pin 25&38請走Codec下方最短路徑直接連接,
並最少40mils線寬

11mA
Closed Codec
C448 10u/10v/X5/8
C451 0.1u/25v/Y/6
VCC3
887_LDOOUT
C679 22u/6.3v/X5/8
C679腳對pin25
C513 0.1u/25v/Y/6
C380 C1u/6.3X5-HF
C513/C360腳對pin38
U26
CODEC_AMP_SD#
EPAD/SPDIF-OUT
SPDIF-OUT
SDATA-OUT
SDATA-IN
SYNC
RESET#
BCLK
GPIO0/DMIC-CLK/SPDIF-OUT2
REGREF
Sense A
Sense B
MIC1-VREFO-R
MIC2-VREFO
MIC1-VREFO-L
PIN37-VREFO
LDO-IN
LINE2-VREFO
VREF
Sense C
JDREF
BEEP
GPIO1/DMIC-DATA
ALC887-VD2-CG
LDO1-OUT1
LDO2-OUT2
DVDD
DVDD-IO
AVSS1
AVSS2
FRONT-R
FRONT-L
LINE_OUTR
LINE_OUTL
CD100u16ELS-HF-2
LOUT R
LOUT L
SURR-R
SURR-L
CENTER
LFE
SIDE-R
SIDE-L
LINE1-R
LINE1-L
LINE2-R
LINE2-L
MIC1-R
MIC1-L
MIC2-R
MIC2-L
CD-R
CD-GND
CD-L
HDA_SDIN0_R
HDA_SDOUT
HDA_SDIN0
HDA_SYNC
HDA_RST#
HDA_BITCLK
R520 33R/4
R521 0R/4
C452 X_10p/50v/N/4
C453 X_0.1u/25v/Y/4
HDA_SDIN0_R
HDA_BITCLK_RA
DMIC_CLK
L22 220L300mA-350_0402-RH
C456 10p/50v/N/4
C447 10u/6.3v/X5/8
150727
R563、C456 change part
SENSE_A
MIC1_V_R
MIC1_V_L
45.8mA
LDOVDD
887_VREF
JDREF
C532 0.1u/25v/Y/6
C535 10u/6.3v/X5/8
R602 20K/4/1%
Closed Codec
DMIC_DATA
SPKR
AUDIO_BEEP
887_BEEP
R533 4.7K/4
R534 4.7K/4
C454 1u/10v/X5/4
C496 0.1u/25v/X7/6
C495 0.1u/25v/X7/6
PC_LOUT_R
PC_LOUT_L
MIC1R
MIC1L
C534 4.7u/6.3v/X5/6
C535 4.7u/6.3v/X5/6
MIC1_R
MIC1_L

B05-LC88714-R09

AUDIO1
LOUT_RA
FRONT_JD
LOUT_LA
JACK-AUDIOF_BL

LOUT_R
R425 75R/4/1%
RA
L19 300L/4 0.25A/0.38R
LOUT_RA
LOUT_L
R428 75R/4/1%
LA
L18 300L/4 0.25A/0.38R
LOUT_LA
R423 22K/4/1%
R427 22K/4/1%
C377 680p/50v/N/4
C391 680p/50v/N/4
C380 X_680p/50v/N/4
C389 X_680p/50v/N/4
D6
D7 ESD_SFI0402ML080C/4
ESD_SFI0402ML080C/4

MIC1_V_R
R681 2.2K/4/1%
MIC1_V_L
R685 2.2K/4/1%
MIC1_R
R661 1K/4
MIC1_L
R658 1K/4
L37 300L/4 0.25A/0.38
L38 300L/4 0.25A/0.38
MIC1-R IN
MIC1-L IN
MIC1_JD
C561 470p/50v/X7/4
C564 470p/50v/X7/4
D38 ESD-SFI0402ML080C
D41 ESD-SFI0402ML080C
MIC1
JACK-AUDIOF_BL

N54-05F1221-H06
Right Angle

R L
1 3 2 4
G 5
BRD file
1 3 5 2 4

SCHEMATIC
3 2 1 4 5
L R G
5.0
14.0

VCC3
VCC5
R133 0R
R134 X_0R
DMIC_CLK
DMIC_DATA
JDMIC1
BH1X5HS-1.25PITCH_WHITE-RH-1

SENSE_A
R714 5.1K/4/1%
FRONT_JD
Closed Codec
R713 20K/4/1%
MIC1_JD

5VSB
L28 60L/8_0.9A/0.1
LDOVDD
C533 C0.1U16X0402
C487 10u/6.3v/X5/8
Closed L28

C563 X_0.1u/16v/X7/4
C473 X_0.1u/16v/X7/4
C577 X_0.1u/16v/X7/4
FOR EMI
C576 X_1000p/50v/X7/4
C569 0.1u/16v/X7/4
C502 0.1u/16v/X7/4
LDOVDD
CP24
C538 X_0.1u/16v/X7/4

U37
PC_LOUT_L
C669 0.1u/25v/X7/6
AMP_EN#
PVCC
LOUTP
LOUTN
C678 C220p50X0402-RH
R715 120K/4/1%
LINN
LINP
SHUTDOWN
PVDDL
PGNDL
COSC
ROSC
AGND
THMR_PAD
RINN
RINP
BYPASS
PVDDR
ROUTP
PGNDR
ROUTN
NC
VOLUME
VDD
TPA2008D2PWPR_HTSSOP24
C666 0.1u/25v/X7/6
C670 1u/25v/X5/6
PC_LOUT_R
C677 10u/6.3v/X5/8
R716 2K/4/1%
R717 2.43K/4/1%
R712 X_20K/4
AMP_G1
As close as chip possible
L26 80L/8_3A/0.04
L27 80L/8_3A/0.04
C671 C0.1U16X0402
C451 10u/10v/X5/8
C674 C0.1U16X0402
C462 10u/10v/X5/8
C682 C0.1U16X0402
C676 C0.1U16X0402
C672 C0.1U16X0402
VCC3
R526 10K/4
CODEC_AMP_SD#
R559 0R/4
AMP_EN#
CP23
C519 X_0.1u/16v/X7/4

ROUTP
L31 80L/8_3A/0.04
ROUTN
L30 80L/8_3A/0.04
AMP_R+
AMP_R-
JAMPR1
C525 680p/50v/X7/4
C524 680p/50v/X7/4
BH1X2HS-1.25P_Red

N32-10200B0-H06

LOUTP
L33 80L/8_3A/0.04
LOUTN
L32 80L/8_3A/0.04
AMP_L+
AMP_L-
JAMPL1
C523 680p/50v/X7/4
C522 680p/50v/X7/4
BH1X2HS-1.25P_Nature

N32-1020900-H06

MICRO-STAR INT'L CO.,LTD
MS-A616
Size: Custom
Document Description: Audio Codec ALC887
Rev: 1.0
Date: Wednesday, January 11, 2017
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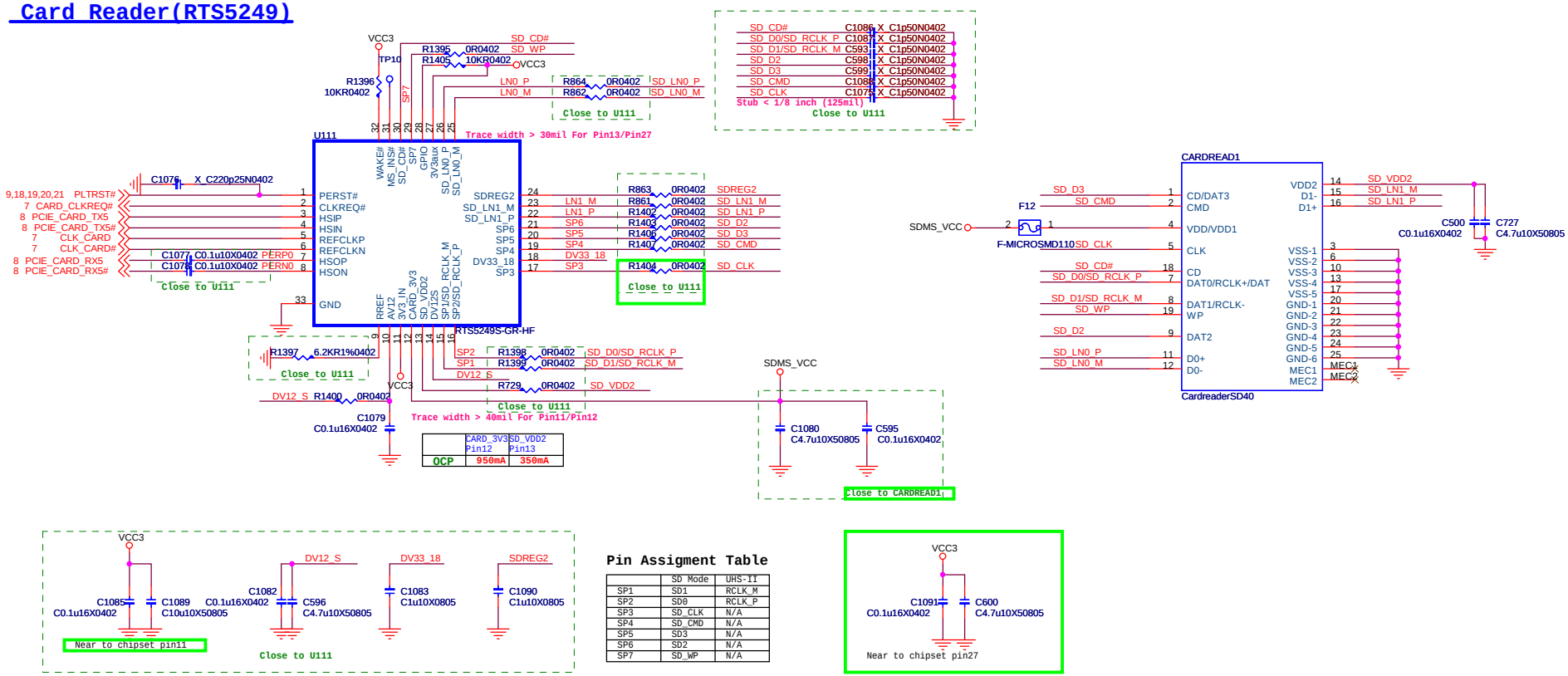
Card Reader(RTS5249)



Pin Assigment Table

	SD Mode	UHS-II
SP1	SD1	RCLK_M
SP2	SD0	RCLK_P
SP3	SD_CLK	N/A
SP4	SD_CMD	N/A
SP5	SD3	N/A
SP6	SD2	N/A
SP7	SD_WP	N/A

MICRO-STAR INT'L CO.,LTD	
MS-A616	
Size: Custom	Document Description: CARD READER_RTS5249
Rev: 10	
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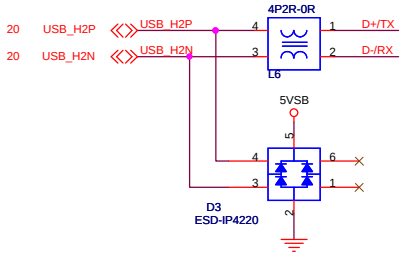
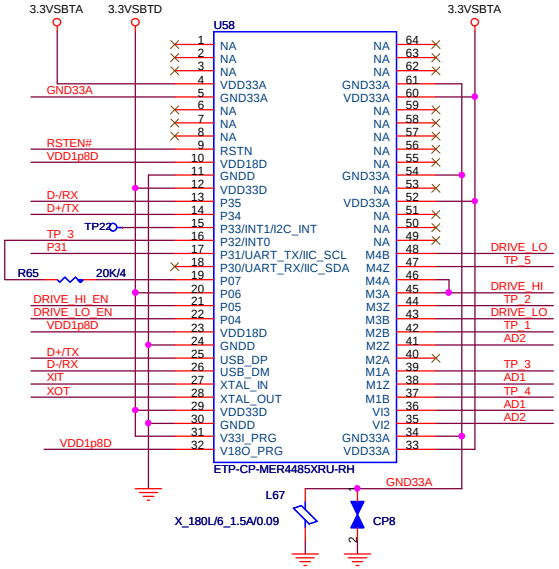
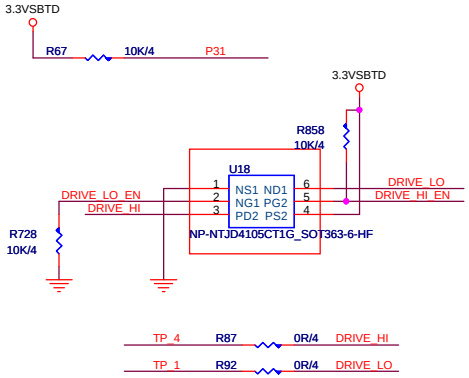
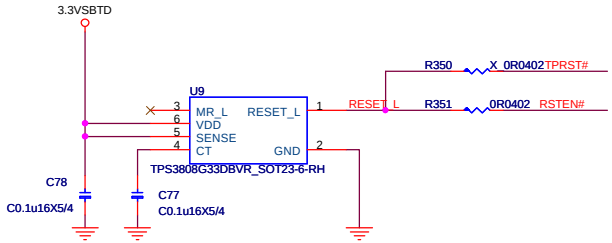
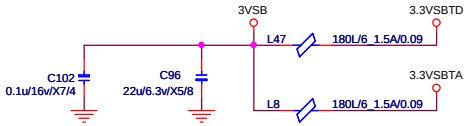
Low Speed USB D+/D-

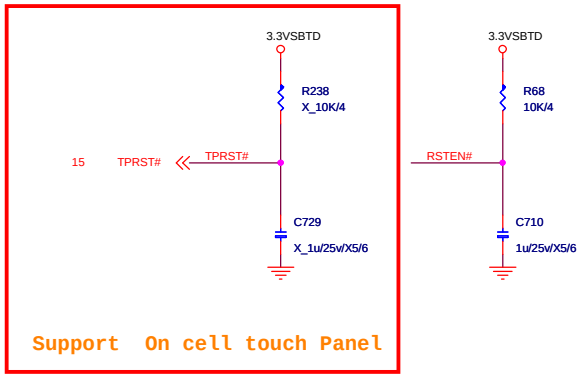




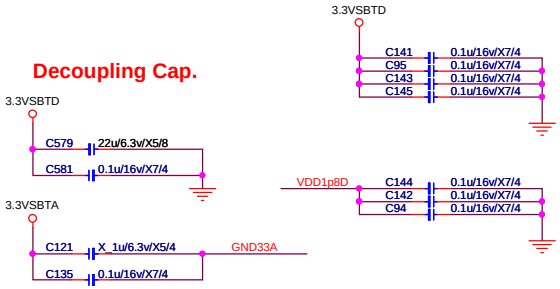


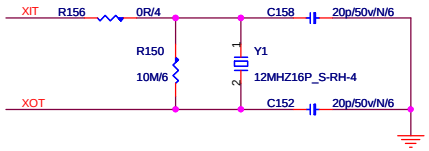


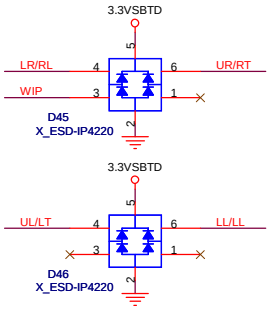




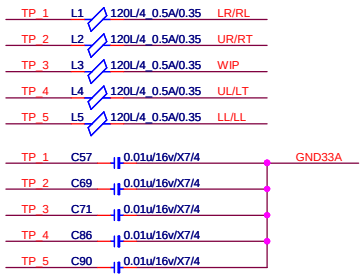
Decoupling Cap.

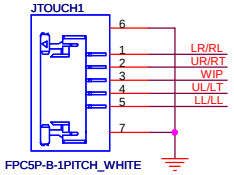






EMI Suppressor

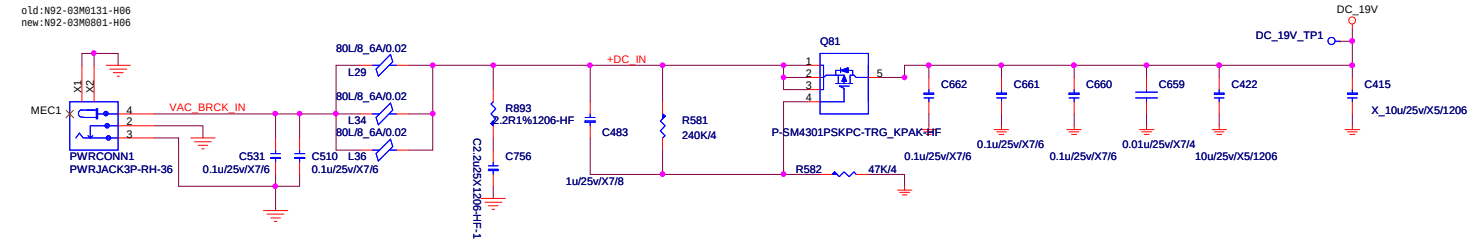


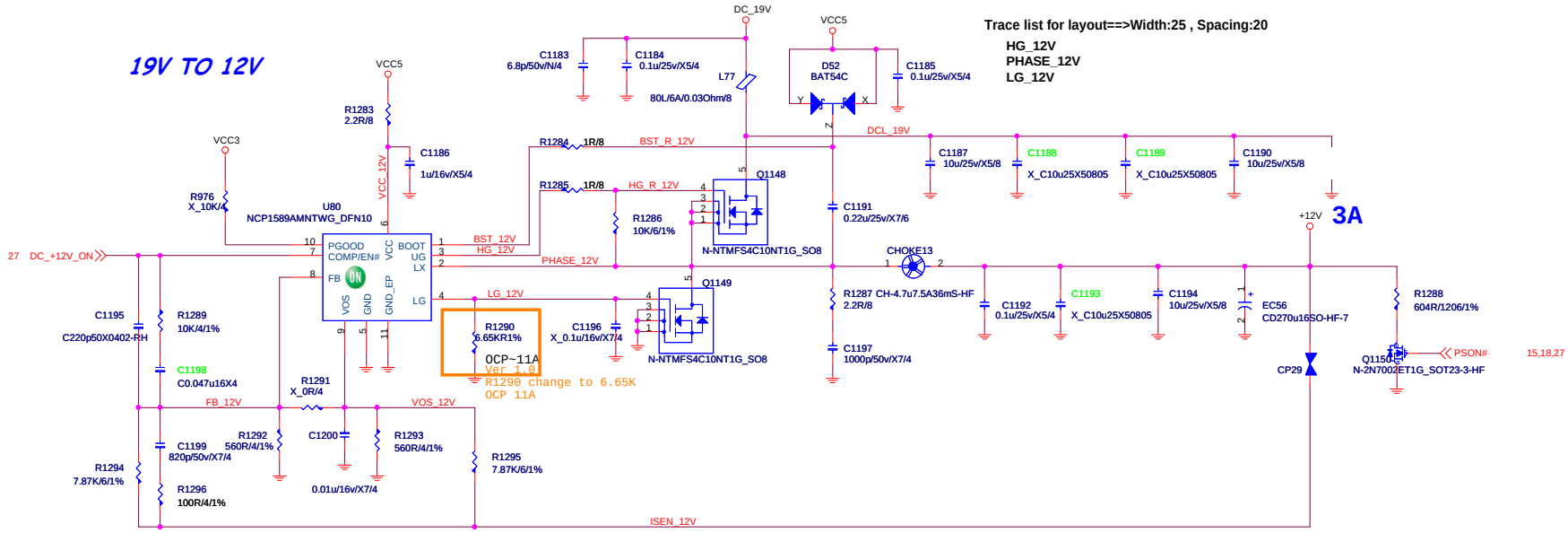


N5A-05F0040-H06

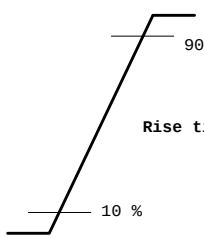
Pitch 1.0mm for 15.6"

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-A616	
Size: Custom	Document Description: Single Touch Panel IC_MER4485	Rev: 10
Date: Wednesday, January 11, 2017	Sheet 25 of 38	





MSI	MICRO-STAR INT'L CO.,LTD	
	MS-A616	
Size: Custom	Document Description: ATX/12V_REG	Rev: 10
Date: Wednesday, January 11, 2017	Sheet 26 of 38	



I32-511250C-T07

Total:11.5A

175mA
+3VALW

175mA
+5VALW
Total:14.5A

7.5A

7.5A

R463 vs R464 二擇一

Ver 1.0
C344/C421
Change to C11-1022013-W08

150427 modify

150427 add

EMI

VSB SWITCH

4A

7A

EUP Function.

ENO open: LDO on and turn on switcher channel

ENO control circuit

TPS51125

TEXAS INSTRUMENTS
www.ti.com

SLUS786A–OCTOBER 2007–REVISED NOVEMBER 2007

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, VIN = 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Softstart						
T_{ss}	Internal SS time	Internal soft start	1.1	1.6	2.1	ms

MICRO-STAR INT'L CO.,LTD

MS-A616

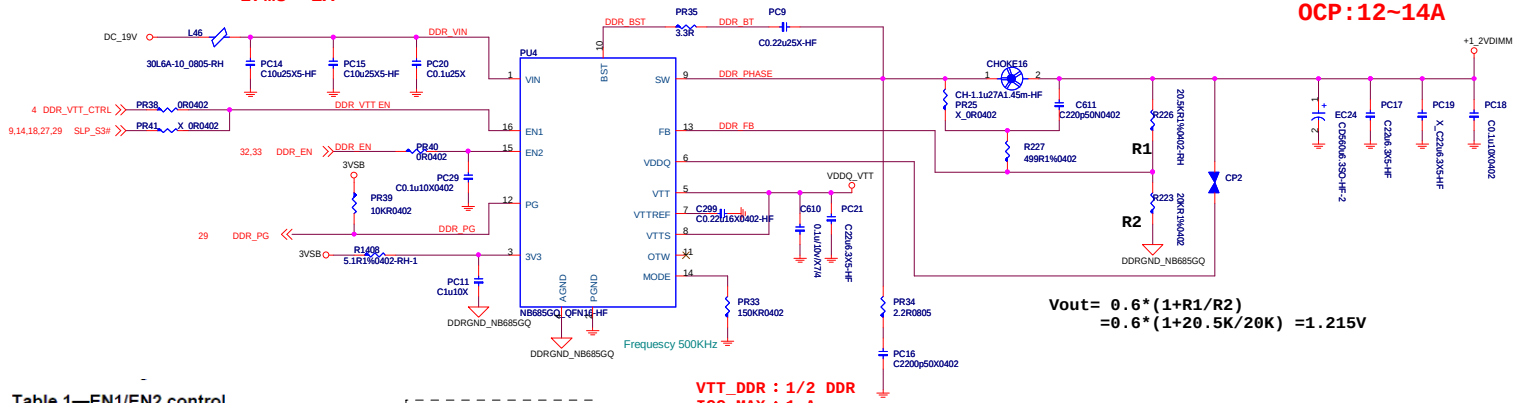
Size	Document Description	Rev
C	System Power VCC3 / VCC5	10

Date: Wednesday, January 11, 2017 | Sheet 27 of 38

DDR4

DDR4 : 1.2V
ICC MAX : 8 A
OCP:12~14A

Irms= 2A

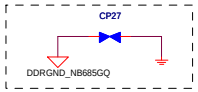


Vout= 0.6*(1+R1/R2)
=0.6*(1+20.5K/20K) =1.215V

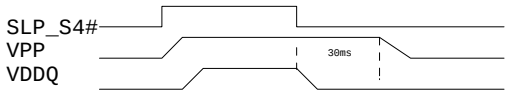
VTT_DDR : 1/2 DDR
ICC MAX : 1 A

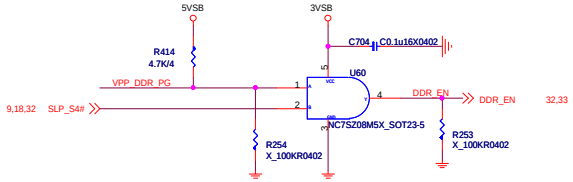
Table 1—EN1/EN2 control

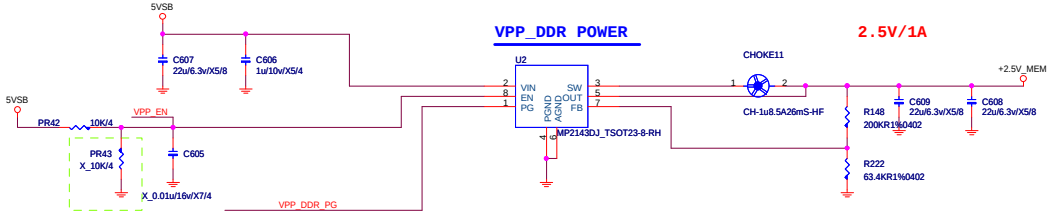
State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF

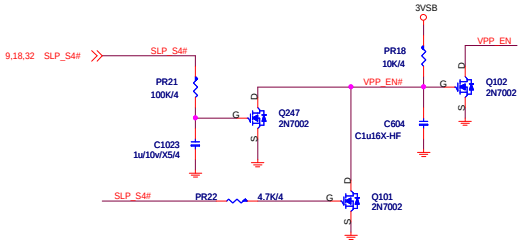


VPP_DDR & VCC_DDR Enable Control

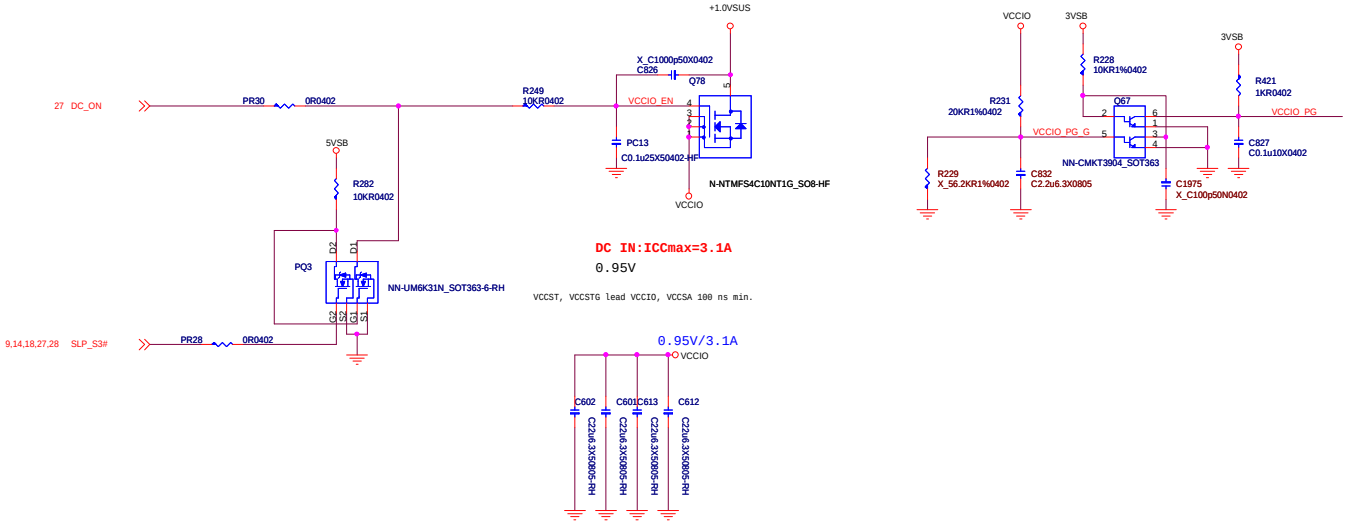




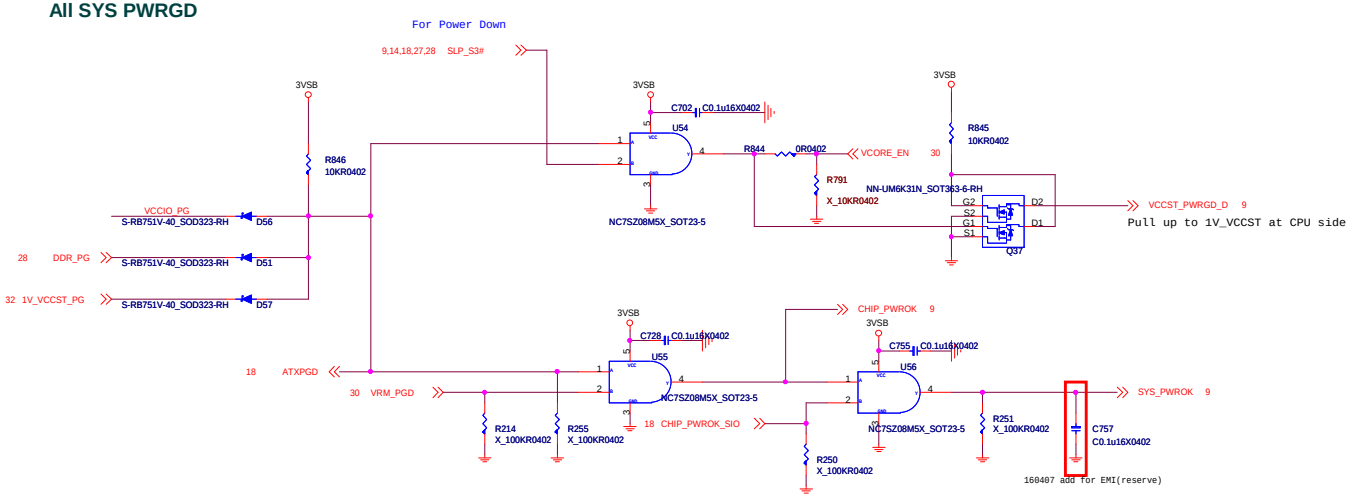




MICRO-STAR INT'L CO.,LTD		
MS-A616		
Size C	Document Description +1_2VDIMM/+2.5V_MEM/VDDQ_VTT	Rev 10
Date: Wednesday, January 11, 2017	Sheet 28 of 38	



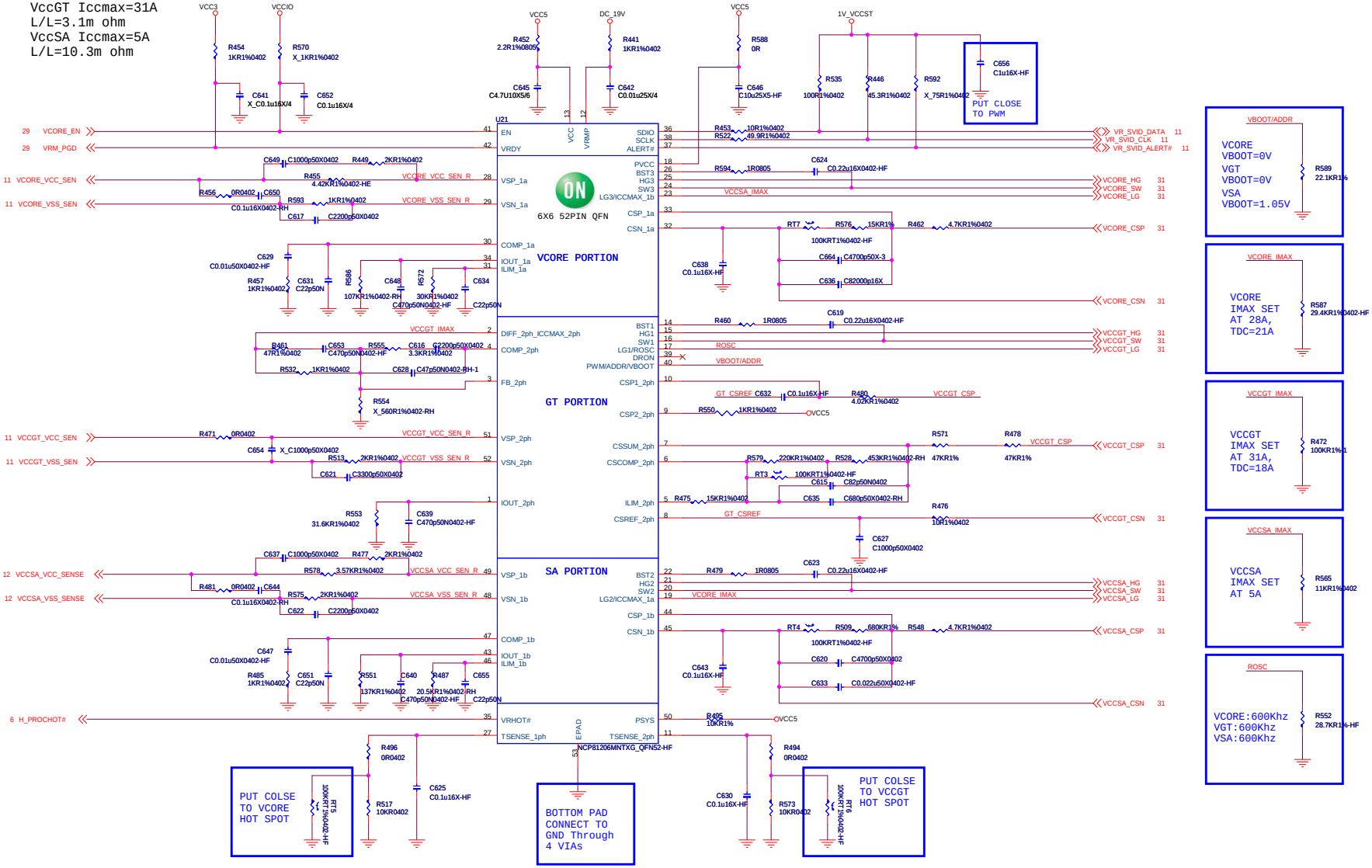
All SYS PWRGD



MICRO-STAR INT'L CO.,LTD		
MS-A616		
Size: C	Document Description: VCCIO / ACPI	Rev: 10
Date: Wednesday, January 11, 2017	Sheet 29 of 38	

Intel SKYLAKE IMVP8 POWER CKT FOR U-LINE 15W - 1+1+1 PHASE

Vcore Iccmax=29A,
L/L=2.4m ohm
VccGT Iccmax=31A
L/L=3.1m ohm
VccSA Iccmax=5A
L/L=10.3m ohm



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Size C | Document Description: CPU VCORE-1(NCP81206MNTXG_QFN52) | Rev 10
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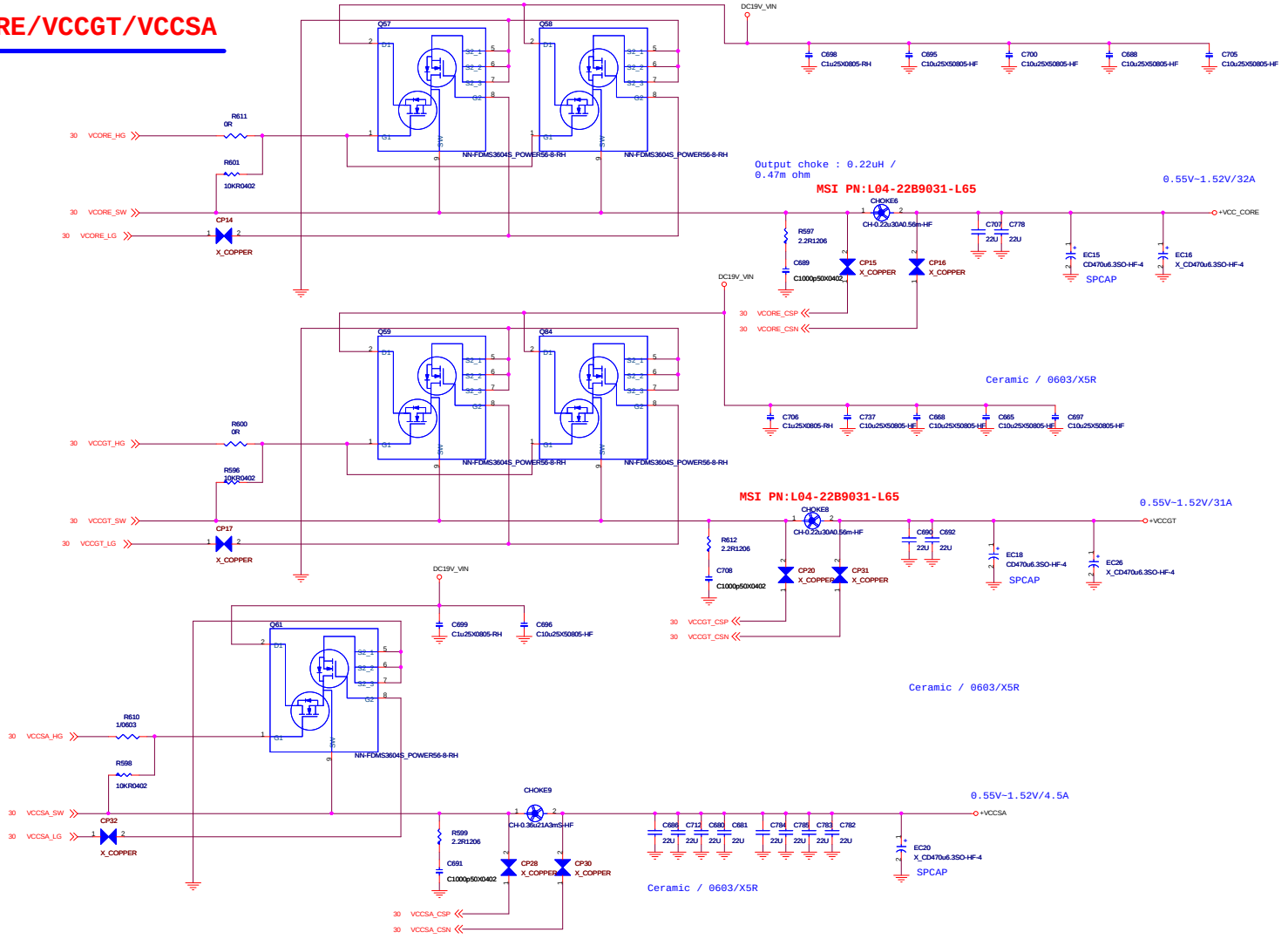
VCORE/VCCGT/VCCSA



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MS-A616	
Size: Custom	Document Description: CPU VCORE-2
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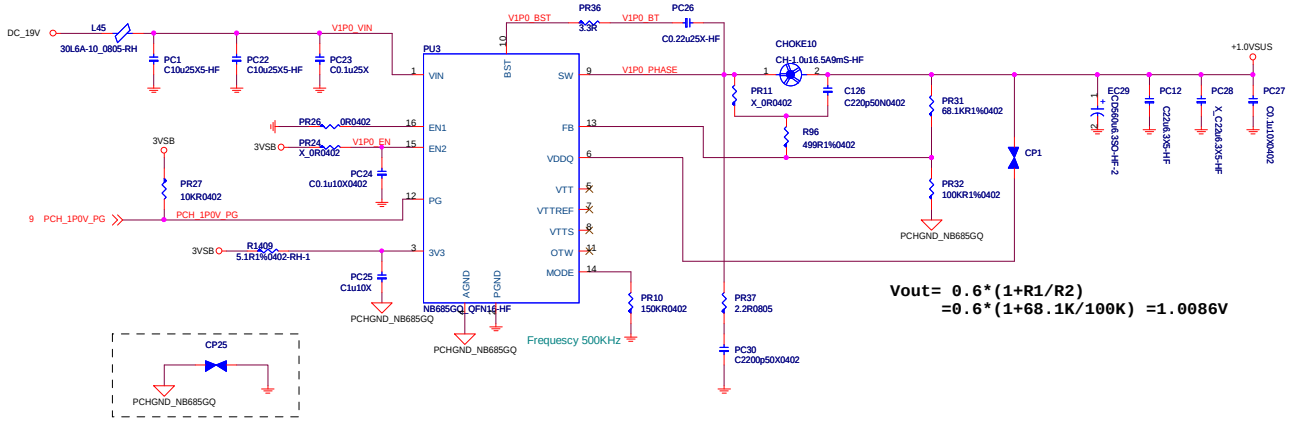
+1.0VSUS
PCH CORE POWER

PCH_1P0V POWER

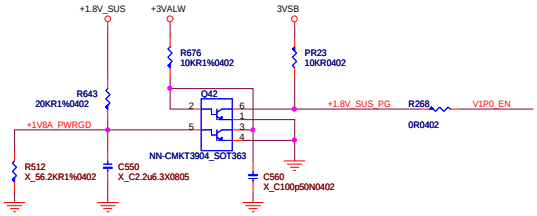
PCH_1P0V：1.0V
ICC MAX：9.132 A
OCP:12~14A

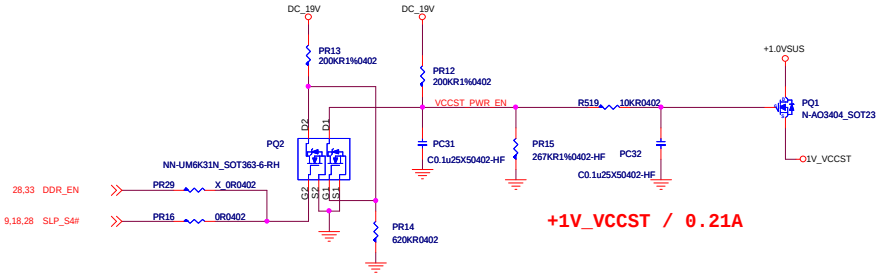
Irms= 2.23A



Vout= 0.6*(1+R1/R2)
=0.6*(1+68.1K/100K) =1.0086V

Vo = 1V
Vin =19V
FS =290khz
OCP 150%~200%
Iout =9.132A
Vin_Irms = 1.9A
MLCC ripple current =
1.5A*2=3A
LIR =25%
Cin_CAP =5uF
Cout_CAP = 669uF
Cout_CAP_ESR =4.5m

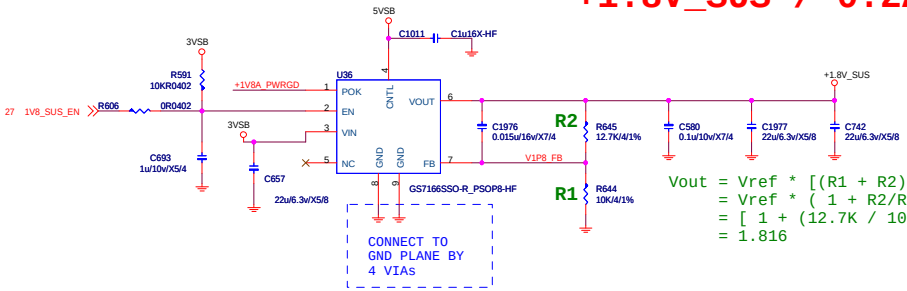




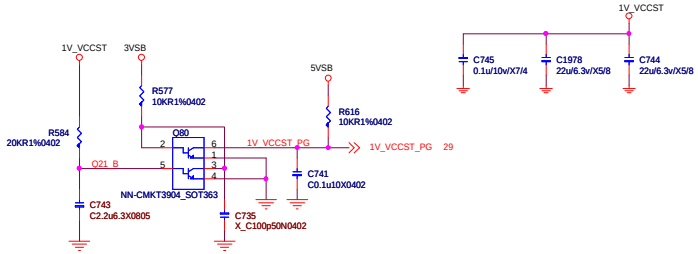
+1V_VCCST / 0.21A

VCCOPC_1p8 may be left on in Sx with minimal leakage.

+1.8V_SUS / 0.2A



Vout = Vref * [(R1 + R2)/R1)]
= Vref * (1 + R2/R1)
= [1 + (12.7K / 10K)] * 0.8
= 1.816



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MS-A6161		
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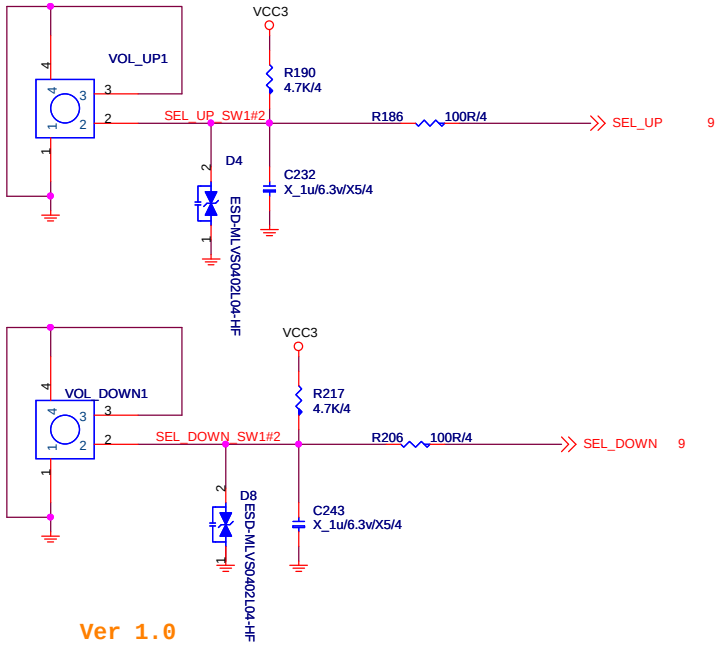
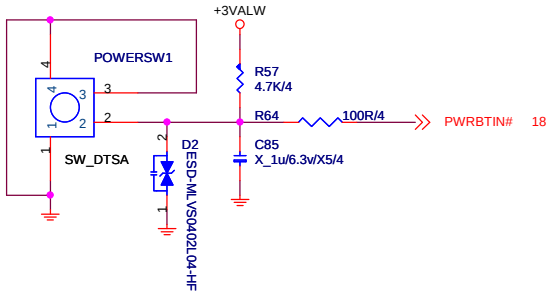
MODE SELECT CONTROL
Backlight SEL_UP SEL_DOWN



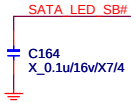
Ver 1.0
modify backlight button circuit

POWER ON/OFF BUTTON

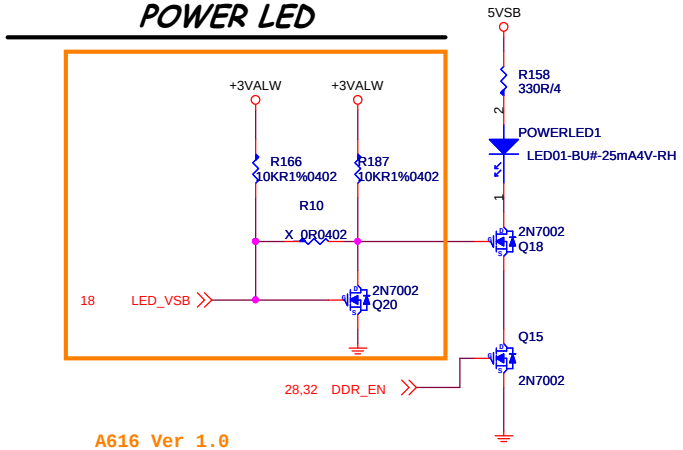


LED Blue

FOR EMI



POWER LED



A616 Ver 1.0
modify power LED circuit

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Size: B	Document Description: HOT KEY / LED	Rev: 10
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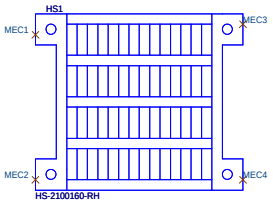
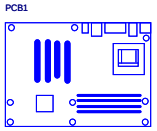
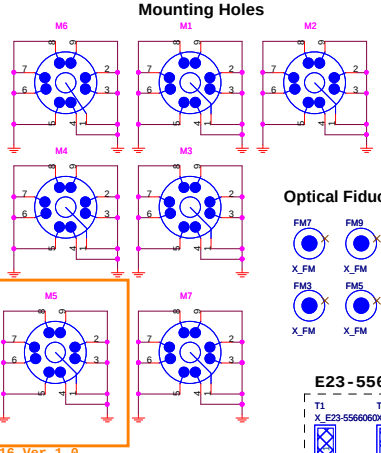
Mounting Holes



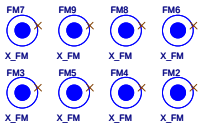
A6161
Fanless : E31-2100160-K08

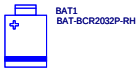


P80-A616110-G37



Optical Fiducial Marks-120



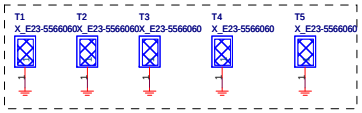


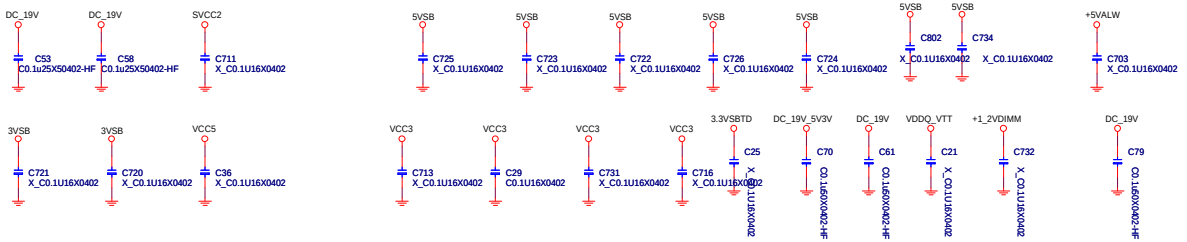
BIOS label

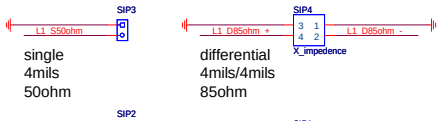
1.0 12/01

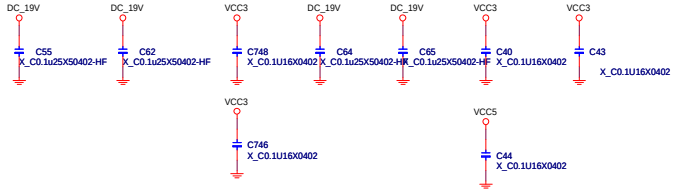
A616 Ver 1.0
modify M5 footprint same as M7

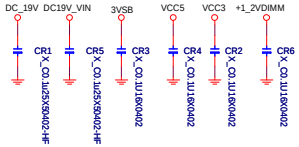
E23-5566060-CA7











FOR RF
2016.11.28

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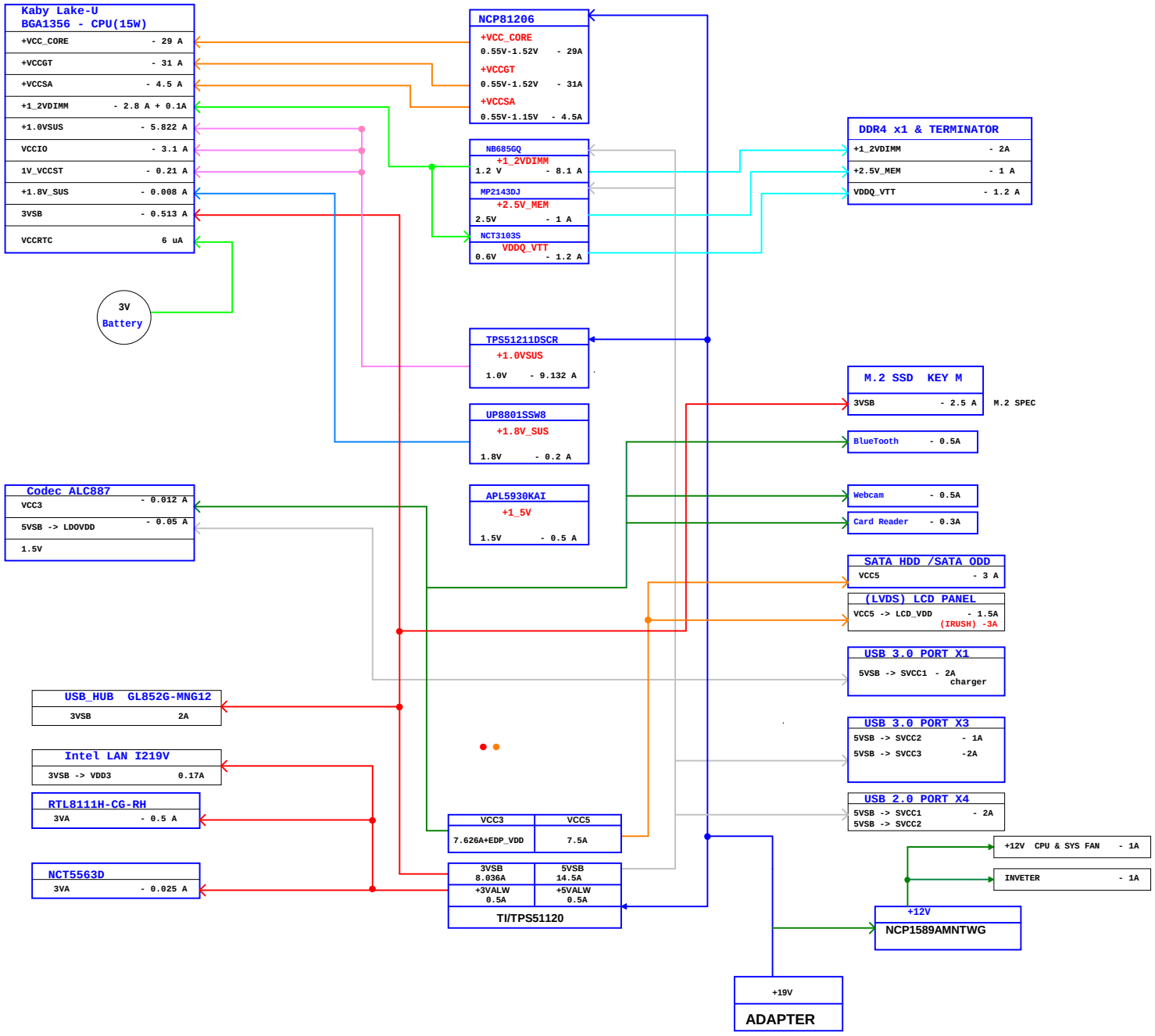

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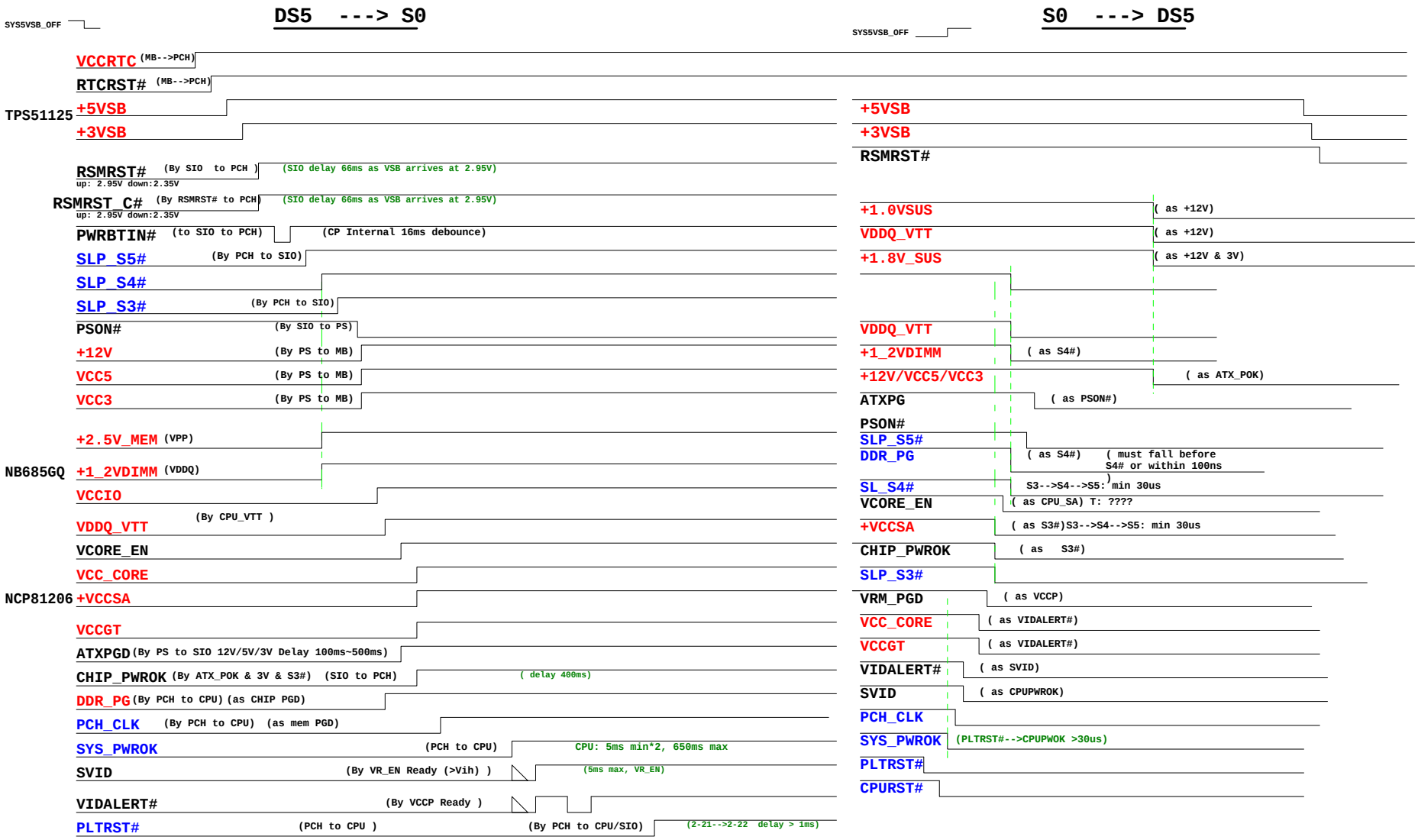

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MS-A616		
Size C	Document Description POWER SEQENCES	Rev 10
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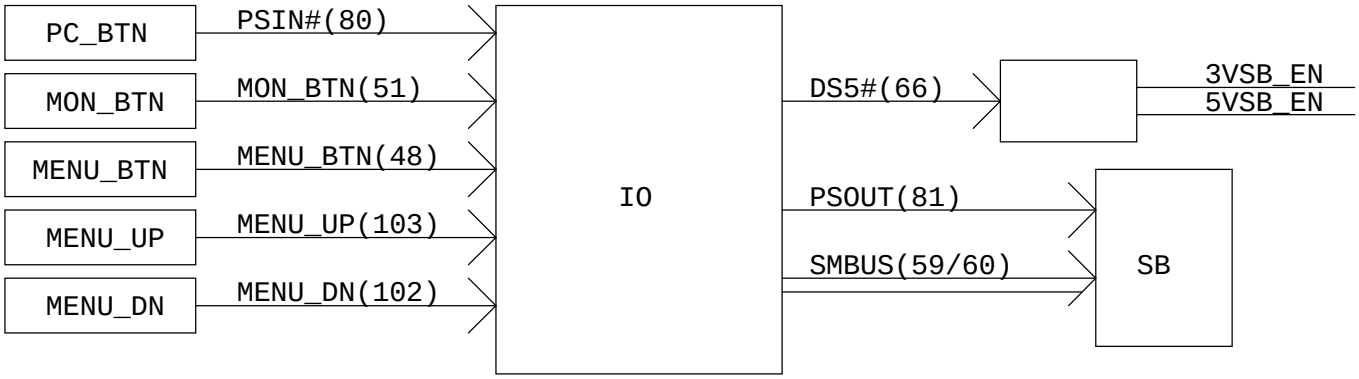

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MS-A616		
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A616 Schematic History
PCB 0A Hostory

2016/10/28

change CPU Kaby lake-U

2016/11/02

Add Power suggestion

A616 Schematic History
PCB 1.0 Hostory

2016/12/23

Page 27 PR6 /PR7 change to 0402 type

Page 26 R1290 change to 6.65K

2017/01/03

Page 33 modify backlight button circuit

Page 16 Part reference change
SATA1 : for ODD / SATA2 : for HDD

Page 17 (Modify) add USB2.0 OC circiut

Page 34 Modify M5 footprint same as M7

Page 33 (Modify) POWER LED circuit

BOM Modify

Page 11 R171 / R182 change to R11-0000012-W08

Page 28 R226 change to R11-2052T12-W08

Page 28 / 31 CHOKE16 / L58 DIP TYPE Ver 1.0
主料改L04-11A8021-L65 , AVL:L04-11A8031-M26

Page 14 U30 Ver 1.0
主料改I36-7550P09-U33

Backlight issue SEL_UP SEL_DOWN
Page 9 R114 / R115 unstuff

Page 27 C344/C421 Ver 1.0
更改C11-1022013-W08為主料號

Page 15 Ver 1.0
C54 change to C11-1047512-W08

Page 23/26 Ver 1.0
C678/C1195 change to C11-2212812-W08 為主料號

Page 05 Ver 1.0
C34 change to C11-2232032-W08 為主料號

Page 05/20 Ver 1.0
C14/C478/C506 change to C11-2252413-S02 為主料號

Page 17 Ver 1.0
C701/C738 change to C11-4712012-W08 為主料號

Page 19/26 Ver 1.0
Q162/Q1150 change to D03-7002E89-O05為主料號

Page 33 Ver 1.0
HDDLED+/POWERLED1 change to D0C-010C901-E07為主料號

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C	HISTORY	10

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