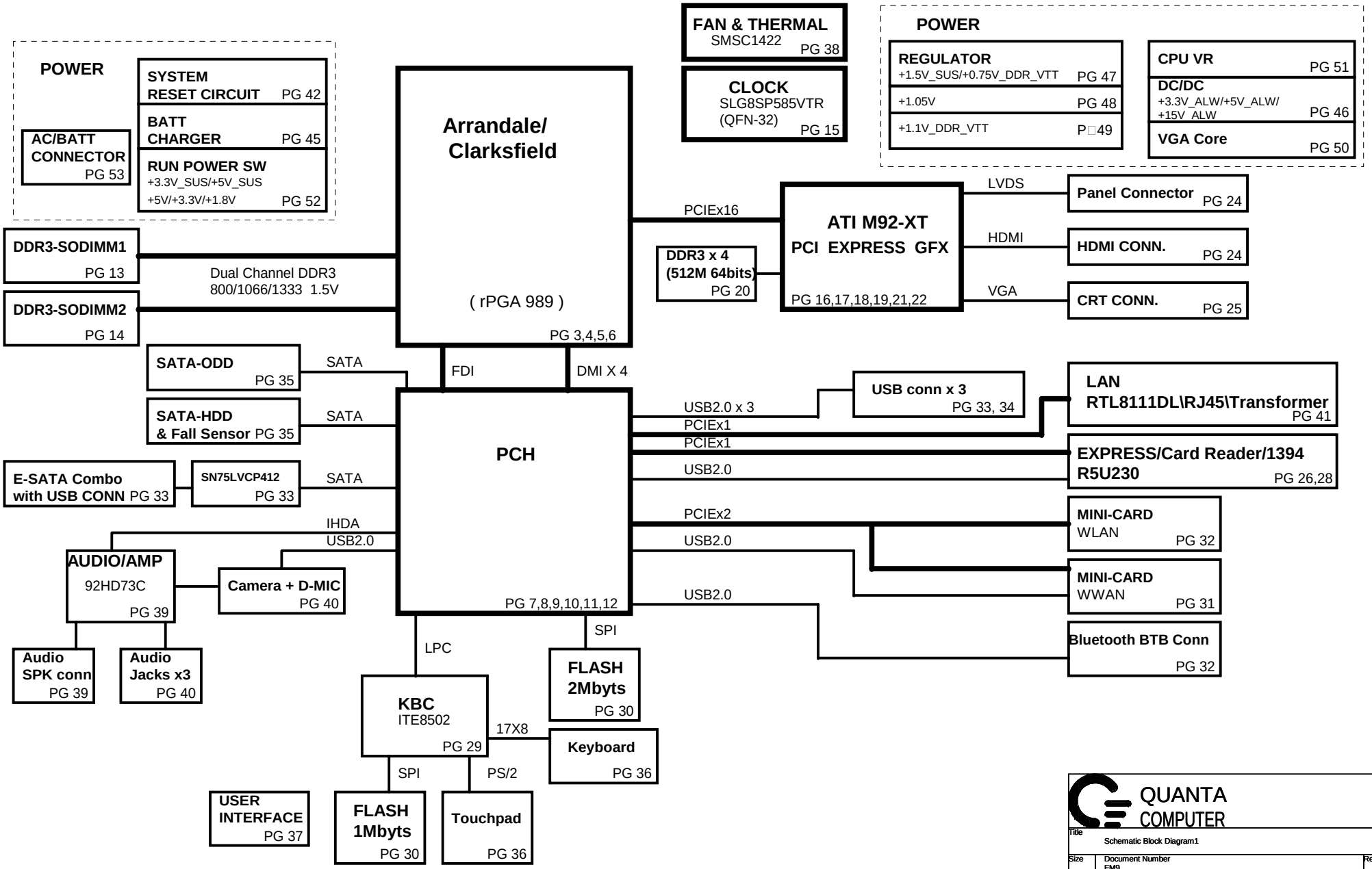
FM9 HANKS Intel Discrete GFX

VER : 2B
PWA:
PWB:



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44 ,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30 ,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_ON	

GND PLANE	PAGE	DESCRIPTION
GND	ALL	

QUANTA COMPUTER

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AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

SC(V1.0),P11: Should be shorted at the pins and then routed to one end of the 49.9-Ω ±1% resistor, pulled-down to GND on the board.

54 90

U34A

DMI

PCI EXPRESS -- GRAPHICS

Intel(R) FDI

DMI_RX#[0] DMI_RX#[1] DMI_RX#[2] DMI_RX#[3]
DMI_RX[0] DMI_RX[1] DMI_RX[2] DMI_RX[3]
DMI_TX#[0] DMI_TX#[1] DMI_TX#[2] DMI_TX#[3]
DMI_TX[0] DMI_TX[1] DMI_TX[2] DMI_TX[3]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]
FDI_TX[0] FDI_TX[1] FDI_TX[2] FDI_TX[3] FDI_TX[4] FDI_TX[5] FDI_TX[6] FDI_TX[7]
FDI_FSYNC[0] FDI_FSYNC[1]
FDI_INT
FDI_LSYNC[0] FDI_LSYNC[1]

PEG_ICOMPI R412 49.9/F
PEG_ICOMPO
PEG_RCOMPO
PEG_RBIAS R413 750/F

PCIE_MRX_GTX_N[0..15] 16
PCIE_MRX_GTX_P[0..15] 16

PEG_RX#[0..15]
PEG_RX[0..15]
PEG_TX#[0..15]
PEG_TX[0..15]

PCIE_MTX_GRX_C_N[0..15]
PCIE_MTX_GRX_C_P[0..15]

Clarksfield/Auburndale

59

R1025 1K 0214 R71 1K

DG(V1.0),P79: should be tied to GND (through 1K ±5% resistors), if these signals are left floating, there are nofunctional impacts but a small amount of power (~15 mW) maybe wasted.
DG(V1.1) P83: FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0],FDI_LSYNC[1] can be ganged together with one resistor.

SC(V1.0),P17,35: This signal should be connected to the processor's VCCPWRGOOD_1 and VCCPWRGOOD_0 input to indicate when the processor power is valid.

VTTPWRGOOD
SC(V1.0)P18: VTT_1.1 VR power good signal to processor. Signal voltage level is 1.1 V.

31 56

+1.5V_SUS
R171 1.1K/F
R97 3K/F
PM_DRAM_PWRGD

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

54 90

U34B

MISC THERMAL DDR3 MISC PWR MANAGEMENT

H_COMP3 H_COMP2 H_COMP1 H_COMP0 SKTOCC# CATERR# PECI PROCHOT# THERMTRIP# RESET_OBS# PM_SYNC VCCPWRGOOD_1 VCCPWRGOOD_0 SM_DRAMPWROK VTTPWRGOOD TAPPWRGOOD RSTIN#

SC(V1.0),P17: SKTOCC# Can be left No Connect or tied to GND

H_PECI R131 0 H_PECI_ISO
H_PROCHOT# D
H_THERM R137 0
H_CPURST#
PM_SYNC
H_PWRGOOD
PM_DRAM_PWRGD
H_VTTPWRGD
H_PWRGD_XDP
PLTRST#
R164 1.5K/F
R163 750/F

RSTIN#: DG(V1.11)(Doc.# 414044),P10: Need a voltage divider network to scale down from 3.3V (PCH driven) to 1.05V/1.1V (Clarksfield/Auburndale)

CLOCKS

BCLK BCLK# BCLK_ITP BCLK_ITP# PEG_CLK PEG_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK#

CLK_CPU_BCLK CLK_CPU_BCLK# BCLK_ITP BCLK_ITP# CLK_PCIE_3GPLL CLK_PCIE_3GPLL#

DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on Auburndale directly if motherboard only supports discrete graphics.

JTAG & BPM

SM_DRAMRST# SM_RCOMP[0] SM_RCOMP[1] SM_RCOMP[2] PM_EXT_TS#[0] PM_EXT_TS#[1] PRDY# PREQ# TCK TMS TRST# TDI TDO TDI_M TDO_M DBR#

DDR3_DRAMRST# SM_RCOMP_0 SM_RCOMP_1 SM_RCOMP_2 +1.1V_VTT R135 10K R134 10K R136 0 R133 0 PM_EXTTS#0 PM_EXTTS#1

XDP_PREQ# XDP_TCLK XDP_TMS XDP_TRST# XDP_TDI_R XDP_TDO_R XDP_TDI_M XDP_TDO_M

R132 *12.4K/F_NC

CRB(v0.71) P.11

2

H_DBR#_R R147 0 XDP_DBRESET# 7,60

XDP_OBS0_R R128 XDP_OBS1_R R146 XDP_OBS2_R R126 XDP_OBS3_R R148 XDP_OBS4_R R129 XDP_OBS5_R R149 XDP_OBS6_R R127 XDP_OBS7_R R130 XDP_OBS[0:7] 60

DBR#: SC(V1.0) P22:Connected to the DBR# pin of the Processor.50-Ω to 5-kΩ pull-up to 3.3VS CRB(V1.0) P11,P71:CRB uses a 1-kΩ pull-up to 3.3VS. On the CRB this signal is ANDed with Master Reset to generate SYS_RESET.

DBR#:(Intell feedback) Nothing wrong w/ CRB design. If you want to connect it to PCH directly, make sure pull high to 3.3V (S0) main power.

+3.3V_RUN R144 10M Q29 2N7002W-7-F H_THERM Q28 MMST3904-7-F C313 0.1U 16 PM_THRMTRIP# 46

T18 T17 +1.1V_VTT XDP_TMS XDP_TDI_R XDP_PREQ# XDP_TCLK R158 R493 R157 R156 *51_NC

CRB(V1.0) P11: is it necessery

JTAG MAPPING

XDP_TDI_R R494 0 XDP_TDI 60
XDP_TDO_M R497 0_NC XDP_TDO 60
R496 0
XDP_TDI_M R495 0_NC
XDP_TDO_R R498 0
XDP_TRST# R499 51

Scan Chain (Default)	STUFF -> R780, R783, R786 NO STUFF -> R781, R785
CPU Only	STUFF -> R780, R781 NO STUFF -> R783, R785, R786
GMCH Only	STUFF -> R785, R786 NO STUFF -> R780, R781, R783

DG(v1.0) table 27

TRSI#: SC(V1.0)P22: should be routed as a single daisy chain to all loads and terminated at the end of the trace. 51 Ω ± 5% pull down resistor. CRB()V1.0)P11

PCIE_MTX_GRX_C_N0 16 C554 0.1U PCIE_MTX_GRX_N0 ... PCIE_MTX_GRX_C_N15 16 C618 0.1U PCIE_MTX_GRX_N15 — PCIE_MTX_GRX_N[0..15] 16

PCIE_MTX_GRX_C_P0 16 C553 0.1U PCIE_MTX_GRX_P0 ... PCIE_MTX_GRX_C_P15 16 C616 0.1U PCIE_MTX_GRX_P15 — PCIE_MTX_GRX_P[0..15] 16

Processor Pullups

+1.1V_VTT R100 49.9/F R121 49.9/F R122 *68_NC
H_CATERR#
H_PROCHOT# D
H_CPURST#

SC(1.0V),P17: H_PROCHOT#D use: pull to 68 ohm if it isn'tt used: pull to 50 ohm

SC(1.0V),P17: H_CATERR# 49.9-Ω ±1% Pull-Up to the VTT rail (+V1.1S_VTT)

Processor Compensation Signals

H_COMP0 H_COMP1 H_COMP2 H_COMP3
R123 49.9/F R72 49.9/F R124 20/F R125 20/F

DG(V1.0),P17: COMP[0.1] 49.9-Ω ±1% pull-down to GND COMP[2.3] 20-Ω ±1% pull-down to GND

DDR3 Compensation Signals

SM_RCOMP_2 SM_RCOMP_1 SM_RCOMP_0
R95 130/F R89 24.9/F R94 100/F

Layout Note: Place these resistors near Processor

DG(V1.0),P83: SM_RCOMP[0] 100-Ω ±1% pull-down to GND SM_RCOMP[1] 24.9-Ω ±1% pull-down to GND SM_RCOMP[2] 130-Ω ±1% pull-down to GND

QUANTA COMPUTER

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AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

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U34C

U34D

DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY - B

13 M_A_DQ[63:0]

14 M_B_DQ[63:0]

M_A_DQ0 A10 SA_DQ[0]
M_A_DQ1 C10 SA_DQ[1]
M_A_DQ2 C7 SA_DQ[2]
M_A_DQ3 A7 SA_DQ[3]
M_A_DQ4 B10 SA_DQ[4]
M_A_DQ5 D10 SA_DQ[5]
M_A_DQ6 E10 SA_DQ[6]
M_A_DQ7 A8 SA_DQ[7]
M_A_DQ8 D8 SA_DQ[8]
M_A_DQ9 F10 SA_DQ[9]
M_A_DQ10 F6 SA_DQ[10]
M_A_DQ11 F7 SA_DQ[11]
M_A_DQ12 E9 SA_DQ[12]
M_A_DQ13 B7 SA_DQ[13]
M_A_DQ14 E7 SA_DQ[14]
M_A_DQ15 C6 SA_DQ[15]
M_A_DQ16 H10 SA_DQ[16]
M_A_DQ17 G8 SA_DQ[17]
M_A_DQ18 K7 SA_DQ[18]
M_A_DQ19 J8 SA_DQ[19]
M_A_DQ20 G7 SA_DQ[20]
M_A_DQ21 G10 SA_DQ[21]
M_A_DQ22 J7 SA_DQ[22]
M_A_DQ23 J10 SA_DQ[23]
M_A_DQ24 L7 SA_DQ[24]
M_A_DQ25 M6 SA_DQ[25]
M_A_DQ26 M8 SA_DQ[26]
M_A_DQ27 L9 SA_DQ[27]
M_A_DQ28 L6 SA_DQ[28]
M_A_DQ29 K8 SA_DQ[29]
M_A_DQ30 N8 SA_DQ[30]
M_A_DQ31 P9 SA_DQ[31]
M_A_DQ32 AH5 SA_DQ[32]
M_A_DQ33 AF5 SA_DQ[33]
M_A_DQ34 AK6 SA_DQ[34]
M_A_DQ35 AK7 SA_DQ[35]
M_A_DQ36 AF6 SA_DQ[36]
M_A_DQ37 AG5 SA_DQ[37]
M_A_DQ38 AJ7 SA_DQ[38]
M_A_DQ39 AJ6 SA_DQ[39]
M_A_DQ40 AJ10 SA_DQ[40]
M_A_DQ41 AJ9 SA_DQ[41]
M_A_DQ42 AL10 SA_DQ[42]
M_A_DQ43 AK12 SA_DQ[43]
M_A_DQ44 AK8 SA_DQ[44]
M_A_DQ45 AL7 SA_DQ[45]
M_A_DQ46 AK11 SA_DQ[46]
M_A_DQ47 AL8 SA_DQ[47]
M_A_DQ48 AN8 SA_DQ[48]
M_A_DQ49 AM10 SA_DQ[49]
M_A_DQ50 AR11 SA_DQ[50]
M_A_DQ51 AL11 SA_DQ[51]
M_A_DQ52 AM9 SA_DQ[52]
M_A_DQ53 AN9 SA_DQ[53]
M_A_DQ54 AT11 SA_DQ[54]
M_A_DQ55 AP12 SA_DQ[55]
M_A_DQ56 AM12 SA_DQ[56]
M_A_DQ57 AN12 SA_DQ[57]
M_A_DQ58 AM13 SA_DQ[58]
M_A_DQ59 AT14 SA_DQ[59]
M_A_DQ60 AT12 SA_DQ[60]
M_A_DQ61 AL13 SA_DQ[61]
M_A_DQ62 AR14 SA_DQ[62]
M_A_DQ63 AP14 SA_DQ[63]

M_B_DQ0 B5 SB_DQ[0]
M_B_DQ1 A5 SB_DQ[1]
M_B_DQ2 C3 SB_DQ[2]
M_B_DQ3 B3 SB_DQ[3]
M_B_DQ4 F4 SB_DQ[4]
M_B_DQ5 A6 SB_DQ[5]
M_B_DQ6 A4 SB_DQ[6]
M_B_DQ7 C4 SB_DQ[7]
M_B_DQ8 D1 SB_DQ[8]
M_B_DQ9 D2 SB_DQ[9]
M_B_DQ10 F2 SB_DQ[10]
M_B_DQ11 F1 SB_DQ[11]
M_B_DQ12 C2 SB_DQ[12]
M_B_DQ13 F5 SB_DQ[13]
M_B_DQ14 F3 SB_DQ[14]
M_B_DQ15 G4 SB_DQ[15]
M_B_DQ16 H6 SB_DQ[16]
M_B_DQ17 G2 SB_DQ[17]
M_B_DQ18 J6 SB_DQ[18]
M_B_DQ19 J3 SB_DQ[19]
M_B_DQ20 G1 SB_DQ[20]
M_B_DQ21 G5 SB_DQ[21]
M_B_DQ22 J2 SB_DQ[22]
M_B_DQ23 J1 SB_DQ[23]
M_B_DQ24 J5 SB_DQ[24]
M_B_DQ25 K2 SB_DQ[25]
M_B_DQ26 L3 SB_DQ[26]
M_B_DQ27 M1 SB_DQ[27]
M_B_DQ28 K5 SB_DQ[28]
M_B_DQ29 K4 SB_DQ[29]
M_B_DQ30 M4 SB_DQ[30]
M_B_DQ31 N5 SB_DQ[31]
M_B_DQ32 AF3 SB_DQ[32]
M_B_DQ33 AG1 SB_DQ[33]
M_B_DQ34 AJ3 SB_DQ[34]
M_B_DQ35 AK1 SB_DQ[35]
M_B_DQ36 AG4 SB_DQ[36]
M_B_DQ37 AG3 SB_DQ[37]
M_B_DQ38 AJ4 SB_DQ[38]
M_B_DQ39 AH4 SB_DQ[39]
M_B_DQ40 AK3 SB_DQ[40]
M_B_DQ41 AK4 SB_DQ[41]
M_B_DQ42 AM6 SB_DQ[42]
M_B_DQ43 AN2 SB_DQ[43]
M_B_DQ44 AK5 SB_DQ[44]
M_B_DQ45 AK2 SB_DQ[45]
M_B_DQ46 AM4 SB_DQ[46]
M_B_DQ47 AM3 SB_DQ[47]
M_B_DQ48 AP3 SB_DQ[48]
M_B_DQ49 AN5 SB_DQ[49]
M_B_DQ50 AT4 SB_DQ[50]
M_B_DQ51 AN6 SB_DQ[51]
M_B_DQ52 AN4 SB_DQ[52]
M_B_DQ53 AN3 SB_DQ[53]
M_B_DQ54 AT5 SB_DQ[54]
M_B_DQ55 AT6 SB_DQ[55]
M_B_DQ56 AN7 SB_DQ[56]
M_B_DQ57 AP6 SB_DQ[57]
M_B_DQ58 AP8 SB_DQ[58]
M_B_DQ59 AT9 SB_DQ[59]
M_B_DQ60 AT7 SB_DQ[60]
M_B_DQ61 AP9 SB_DQ[61]
M_B_DQ62 AR10 SB_DQ[62]
M_B_DQ63 AT10 SB_DQ[63]

SA_CK[0] AA6 M_A_CLK0 13
SA_CK#[0] AA7 M_A_CLK0# 13
SA_CKE[0] P7 M_A_CKE0 13

SA_CK[1] Y6 M_A_CLK1 13
SA_CK#[1] Y5 M_A_CLK1# 13
SA_CKE[1] P6 M_A_CKE1 13

SA_CS#[0] AE2 M_A_CS0# 13
SA_CS#[1] AE8 M_A_CS1# 13

SA_ODT[0] AD8 M_A_ODT0 13
SA_ODT[1] AF9 M_A_ODT1 13

SA_DM[0] B9 M_A_DM0
SA_DM[1] D7 M_A_DM1
SA_DM[2] H7 M_A_DM2
SA_DM[3] M7 M_A_DM3
SA_DM[4] AG6 M_A_DM4
SA_DM[5] AM7 M_A_DM5
SA_DM[6] AN10 M_A_DM6
SA_DM[7] AN13 M_A_DM7
M_A_DM[7:0] 13

SA_DQS#[0] C9 M_A_DQS#0
SA_DQS#[1] F8 M_A_DQS#1
SA_DQS#[2] J9 M_A_DQS#2
SA_DQS#[3] N9 M_A_DQS#3
SA_DQS#[4] AH7 M_A_DQS#4
SA_DQS#[5] AK9 M_A_DQS#5
SA_DQS#[6] AP11 M_A_DQS#6
SA_DQS#[7] AT13 M_A_DQS#7
M_A_DQS#[7:0] 13

SA_DQS[0] C8 M_A_DQS0
SA_DQS[1] F9 M_A_DQS1
SA_DQS[2] H9 M_A_DQS2
SA_DQS[3] M9 M_A_DQS3
SA_DQS[4] AH8 M_A_DQS4
SA_DQS[5] AK10 M_A_DQS5
SA_DQS[6] AN11 M_A_DQS6
SA_DQS[7] AR13 M_A_DQS7
M_A_DQS[7:0] 13

SA_MA[0] Y3 M_A_A0
SA_MA[1] W1 M_A_A1
SA_MA[2] AA8 M_A_A2
SA_MA[3] AA3 M_A_A3
SA_MA[4] V1 M_A_A4
SA_MA[5] AA9 M_A_A5
SA_MA[6] V8 M_A_A6
SA_MA[7] T1 M_A_A7
SA_MA[8] Y9 M_A_A8
SA_MA[9] U6 M_A_A9
SA_MA[10] AD4 M_A_A10
SA_MA[11] T2 M_A_A11
SA_MA[12] U3 M_A_A12
SA_MA[13] AG8 M_A_A13
SA_MA[14] T3 M_A_A14
SA_MA[15] V9 M_A_A15
M_A_A[15:0] 13

13 M_A_BS0 AC3 SA_BS[0]
13 M_A_BS1 AB2 SA_BS[1]
13 M_A_BS2 U7 SA_BS[2]

13 M_A_CAS# AE1 SA_CAS#
13 M_A_RAS# AB3 SA_RAS#
13 M_A_WE# AE9 SA_WE#

14 M_B_BS0 AB1 SB_BS[0]
14 M_B_BS1 W5 SB_BS[1]
14 M_B_BS2 R7 SB_BS[2]

14 M_B_CAS# AC5 SB_CAS#
14 M_B_RAS# Y7 SB_RAS#
14 M_B_WE# AC6 SB_WE#

SB_CK[0] W8 M_B_CLK0 14
SB_CK#[0] W9 M_B_CLK0# 14
SB_CKE[0] M3 M_B_CKE0 14

SB_CK[1] V7 M_B_CLK1 14
SB_CK#[1] V6 M_B_CLK1# 14
SB_CKE[1] M2 M_B_CKE1 14

SB_CS#[0] AB8 M_B_CS0# 14
SB_CS#[1] AD6 M_B_CS1# 14

SB_ODT[0] AC7 M_B_ODT0 14
SB_ODT[1] AD1 M_B_ODT1 14

SB_DM[0] D4 M_B_DM0
SB_DM[1] E1 M_B_DM1
SB_DM[2] H3 M_B_DM2
SB_DM[3] K1 M_B_DM3
SB_DM[4] AH1 M_B_DM4
SB_DM[5] AL2 M_B_DM5
SB_DM[6] AR4 M_B_DM6
SB_DM[7] AT8 M_B_DM7
M_B_DM[7:0] 14

SB_DQS#[0] D5 M_B_DQS#0
SB_DQS#[1] F4 M_B_DQS#1
SB_DQS#[2] J4 M_B_DQS#2
SB_DQS#[3] L4 M_B_DQS#3
SB_DQS#[4] AH2 M_B_DQS#4
SB_DQS#[5] AL4 M_B_DQS#5
SB_DQS#[6] AR5 M_B_DQS#6
SB_DQS#[7] AR8 M_B_DQS#7
M_B_DQS#[7:0] 14

SB_DQS[0] C5 M_B_DQS0
SB_DQS[1] E3 M_B_DQS1
SB_DQS[2] H4 M_B_DQS2
SB_DQS[3] M5 M_B_DQS3
SB_DQS[4] AG2 M_B_DQS4
SB_DQS[5] AL5 M_B_DQS5
SB_DQS[6] AP5 M_B_DQS6
SB_DQS[7] AR7 M_B_DQS7
M_B_DQS[7:0] 14

SB_MA[0] U5 M_B_A0
SB_MA[1] V2 M_B_A1
SB_MA[2] T5 M_B_A2
SB_MA[3] V3 M_B_A3
SB_MA[4] R1 M_B_A4
SB_MA[5] T8 M_B_A5
SB_MA[6] R2 M_B_A6
SB_MA[7] R6 M_B_A7
SB_MA[8] R4 M_B_A8
SB_MA[9] R5 M_B_A9
SB_MA[10] AB5 M_B_A10
SB_MA[11] P3 M_B_A11
SB_MA[12] R3 M_B_A12
SB_MA[13] AF7 M_B_A13
SB_MA[14] P5 M_B_A14
SB_MA[15] N1 M_B_A15
M_B_A[15:0] 14

Clarksfield/Auburndale

Clarksfield/Auburndale

Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

QUANTA COMPUTER

Title	AUBURNDA 2/4	
Size	Document Number FM9	Rev 2B
Date:	Wednesday, May 27, 2009	Sheet 4 of 66

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

CPU Core Power

54 90

U34F

+VCC_CORE

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

VCC_SENSE
VSS_SENSE

VTT_SENSE
VSS_SENSE_VTT

PSI#

VID[0]
VID[1]
VID[2]
VID[3]
VID[4]
VID[5]
VID[6]
PROC_DPRSLPVR

VTT_SELECT

ISENSE

+1.1V_VTT

VTT0_43,VTT0_44:
CRB(V1.0)P13
Why add 0ohm?? Is it trace width control??

VTT0_43,VTT0_44:(Intel feedback)
They are connected to hidden page for intel validation purpose.

VTT_SELECT:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield

+VCC_CORE

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND
or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options in the design for the Turbo functionality.
The stuffing and no-stuffing of the resistors will depend on the POC configuration of AUB and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

Note:
For Validating IMVP VR R814 should be STUFF and R827 NO_STUFF

U34G

GRAPHICS

POWER

PEG & DMI

DDR3 - 1.5V RAILS

1.1V

1.8V

SENSE LINES

GRAPHICS VIDS

GFX_VID[0..6],GFX_VR_EN,GFX_DPRSLPVR,GFX_IMON:
Could this be left unconnected when not in use?

GFX_VID[0..6],GFX_VR_EN,GFX_DPRSLPVR,GFX_IMON:(Intel feedback)
Yes, see DG rev1.5

Pop it when Arrandale Graphics disable.

+1.5V_SUS

+1.8V_RUN

Clarksfield/Auburndale

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

Title	AUBURNDA 3/4		
Size	Document Number FM9		Rev 2B
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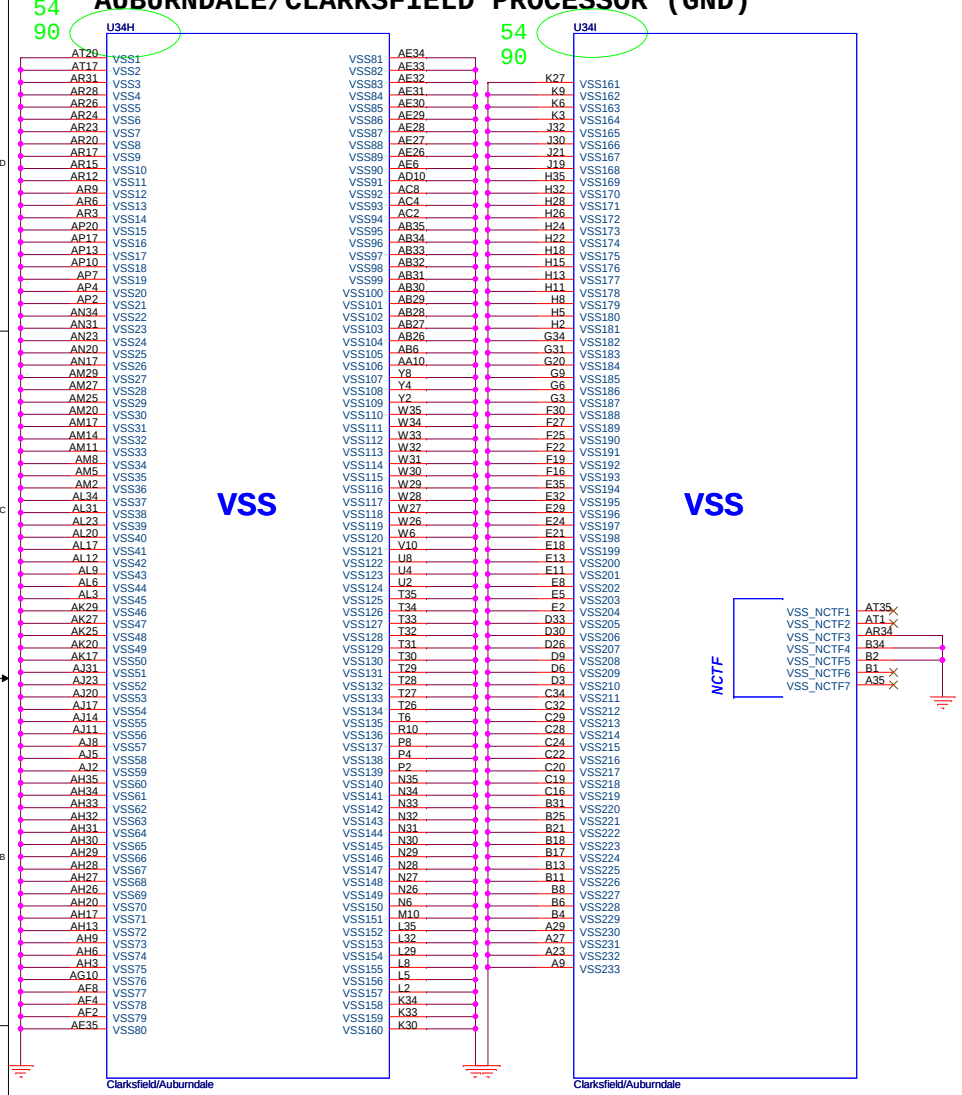
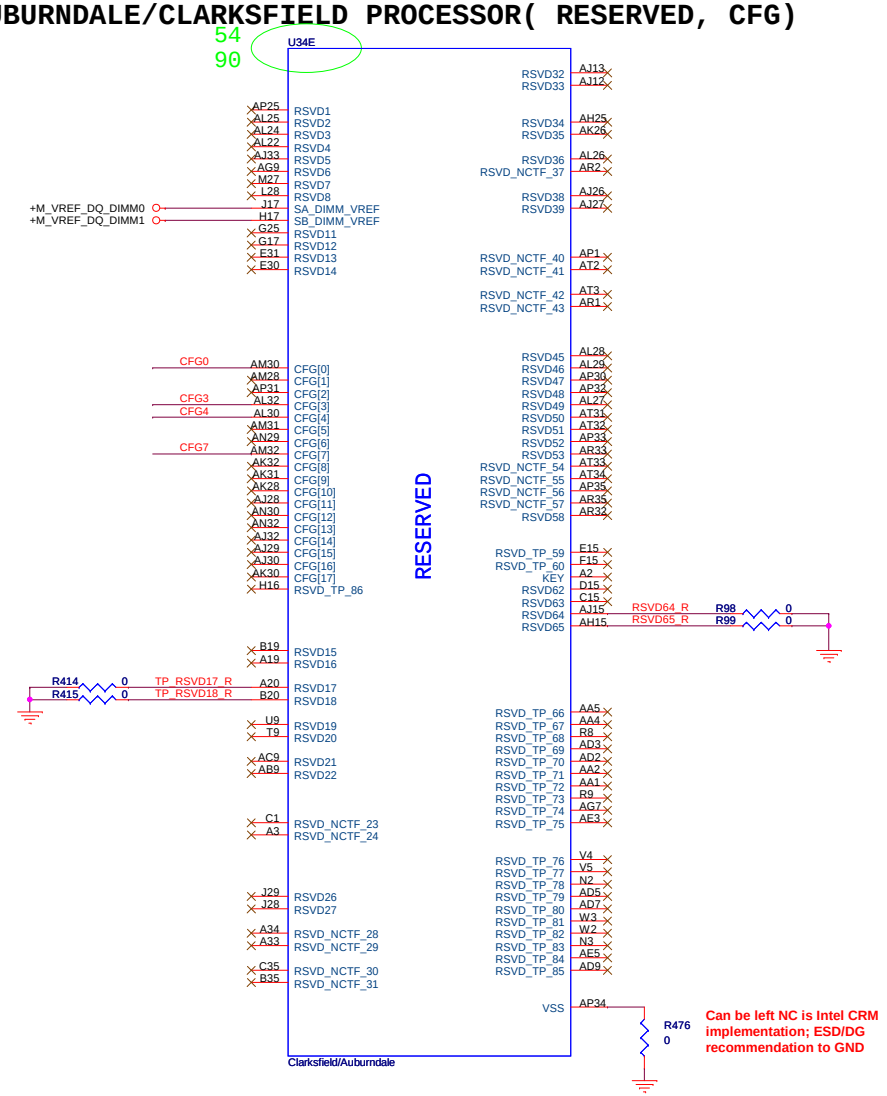
QUANTA COMPUTER

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

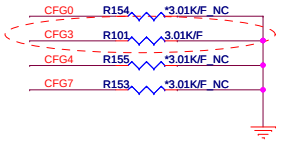


AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Can be left NC is Intel CRM implementation; ESD/DG recommendation to GND

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

QUANTA COMPUTER

Title	AUBURNDA 4/4	
Size	Document Number FM9	Rev 2B
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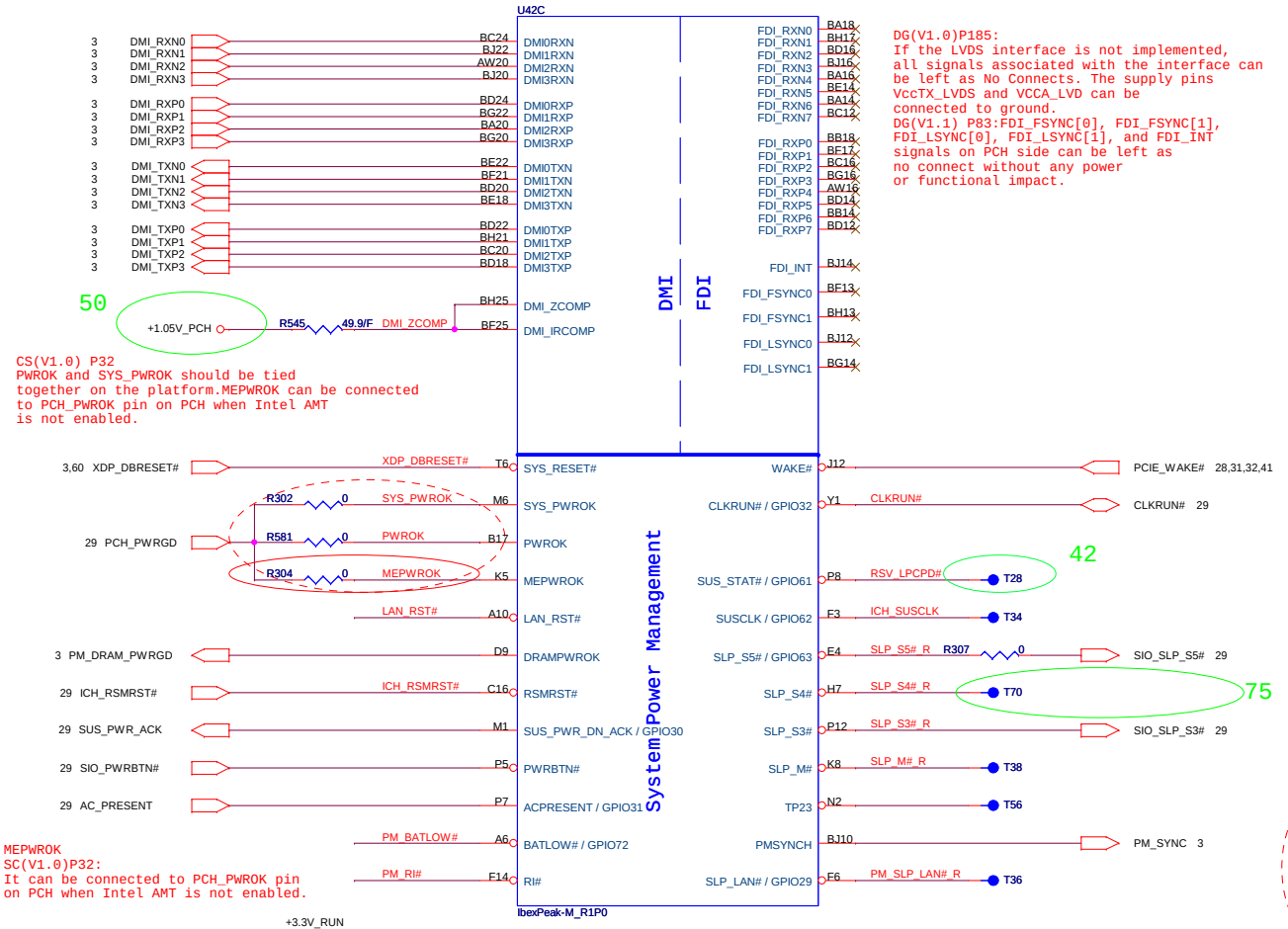
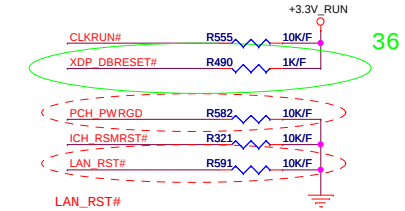
IBEX PEAK-M (DMI,FDI,GPIO)



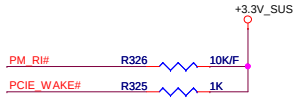
DG(V1.0)P185:
If the LVDS interface is not implemented, all signals associated with the interface can be left as No Connects. The supply pins VccTX_LVDS and VCCA_LVD can be connected to ground.
DG(V1.1) P83:FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on PCH side can be left as no connect without any power or functional impact.

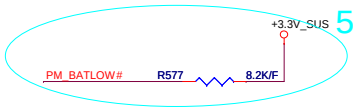
CS(V1.0) P32
PWROK and SYS_PWROK should be tied together on the platform.MEPWROK can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.

MEPWROK
SC(V1.0)P32:
It can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.



LAN_RST#
DG(V1.0) P311
If integrated LAN is not used, recommend to connect LAN_RST# to GND via an 8.2-kΩ to 10-kΩ pull-down resistor.
EDS(V1.0)P64
must be grounded if Intel LAN is disabled.



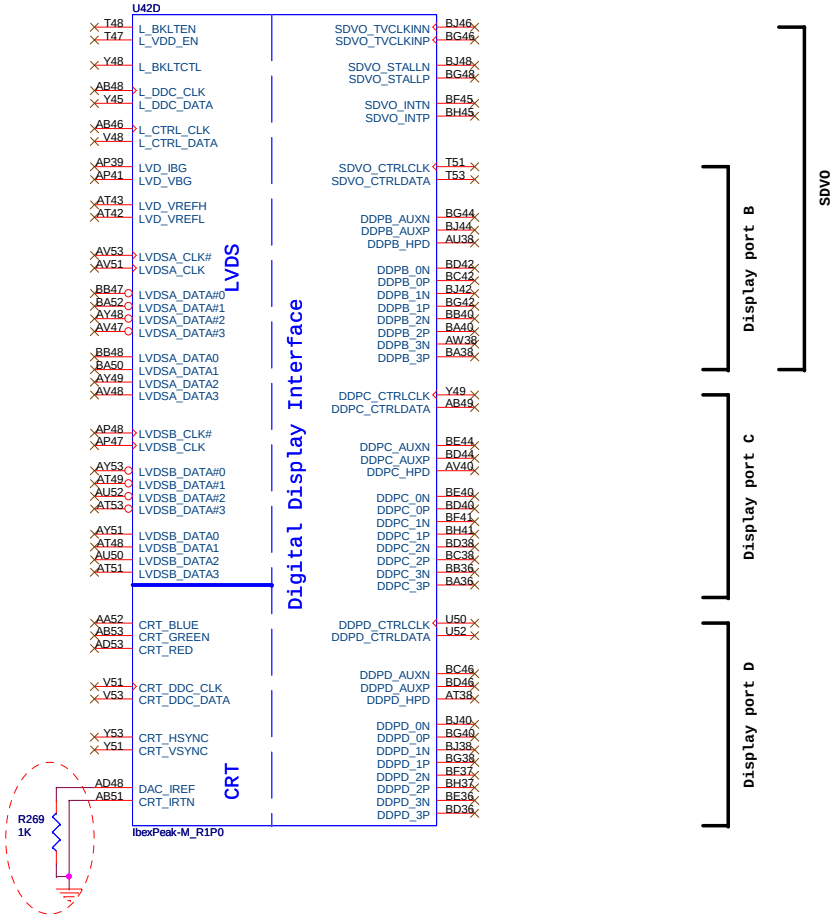


PM_BATLOW#:
EDS(V1.0)P95: 15K~40K (+3.3V_SUS)
CRB(V1.0)P25: 8.2K (+3.3V_ALW)

PM_BATLOW#:(Intel feedback)
15K ~ 40K is a simulation result, the expected value should be 20K internal pull high in PCH.
8.2K is external pull high.

PWROK
SC(V1.0)P32:
8.2 kΩ to 10 kΩ pull-down resistor to GND.
PWROK and SYS_PWROK should be tied together on the platform.

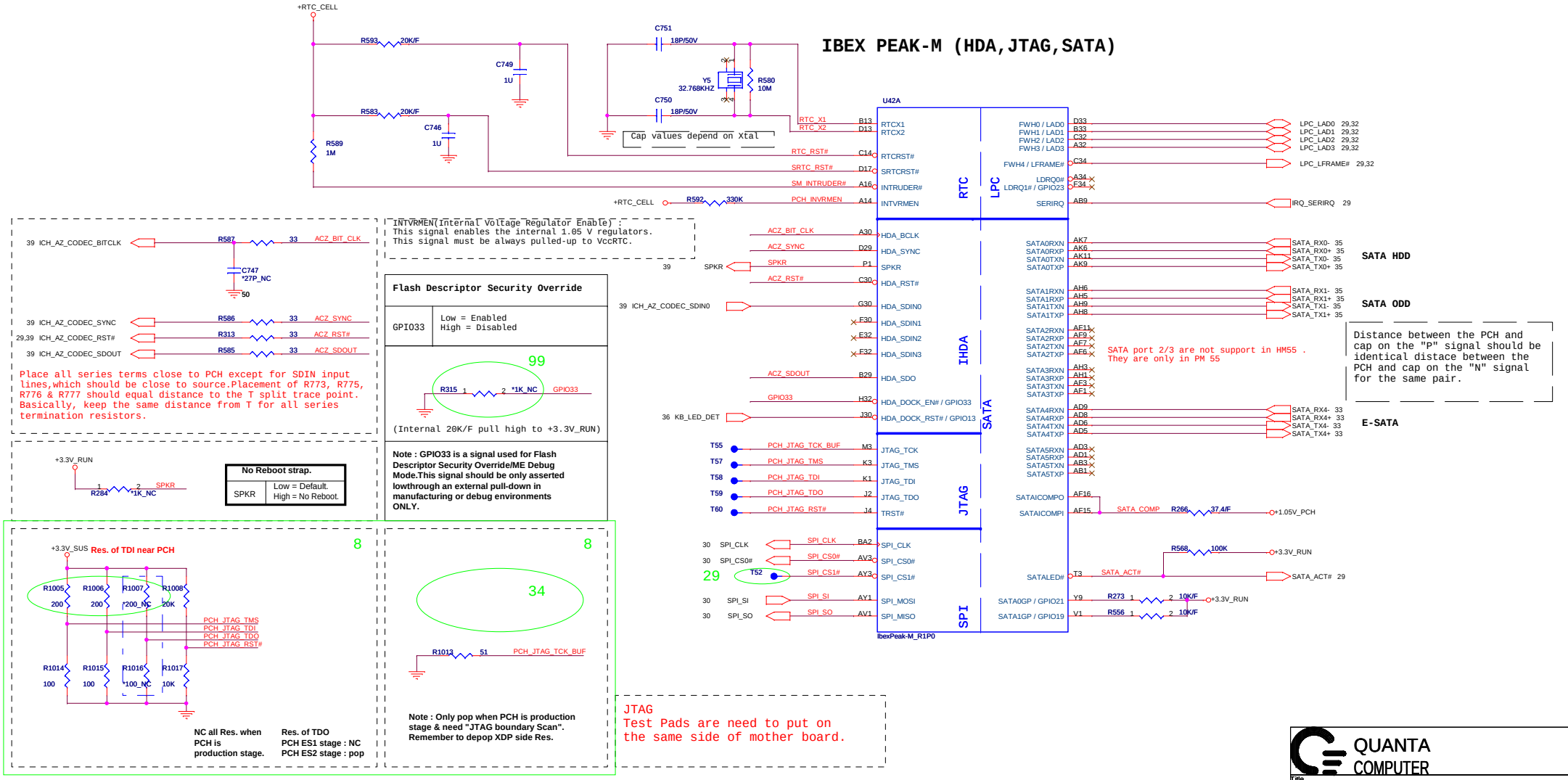
IBEX PEAK-M (LVDS,DDI)



DG(V1.0)P189:
If the CRT interface is not implemented, all signals associated with the interface can be left as No Connects. The pins CRT_IRTN Connect this signals to GND and DAC_IREF Connect to GND via a 1.0 k ±0.5% pull-down resistor

QUANTA COMPUTER			
Title: IBEX PEAK-M 2/6			
Size	Document Number: FM9		Rev: 2B
Date: Monday, May 25, 2009		Sheet 7 of 66	

IBEX PEAK-M (HDA,JTAG,SATA)



39 ICH_AZ_CODEC_BITCLK — R587 33 — ACZ_BIT_CLK
C747 *27P_NC
50
39 ICH_AZ_CODEC_SYNC — R586 33 — ACZ_SYNC
29,39 ICH_AZ_CODEC_RST# — R313 33 — ACZ_RST#
39 ICH_AZ_CODEC_SDOUT — R585 33 — ACZ_SDOUT

Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

INTVRMEN(Internal Voltage Regulator Enable) :
This signal enables the internal 1.05 V regulators.
This signal must be always pulled-up to VccRTC.

Flash Descriptor Security Override	
GPIO33	Low = Enabled High = Disabled

99
R315 1 2 *1K_NC GPIO33
(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

+3.3V_RUN
R284 1 2 *1K_NC SPKR

No Reboot strap.	
SPKR	Low = Default. High = No Reboot.

SATA port 2/3 are not support in HM55 .
They are only in PM 55

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

8
+3.3V_SUS Res. of TDI near PCH
R1005 200 R1006 200 R1007 *200_NC R1008 20K
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_RST#
R1014 100 R1015 100 R1016 *100_NC R1017 10K

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

8
34
R1013 51 PCH_JTAG_TCK_BUF

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

JTAG
Test Pads are need to put on the same side of mother board.

QUANTA COMPUTER

Title	IBEX PEAK-M 1/6	
Size	Document Number FM9	Rev 2B
Date: Thursday, June 04, 2009	Sheet 8 of 66	

IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.

U42E

PCI

NVRAM

USB

Left Side pair Top

Left Side pair bottom

Right Side pair top (Cable)

Mini Card (WLAN)

Mini Card (WWAN)

Mini Card (WPAN)

Express Card

Camera

Touch Screen Module

USB port 6/7 are not support in HM55
They are only in PM 55

Note : place these resistors near to PCIe Slots

PCIRST#:
DG(V1.0) P277
Can be left unconnected.

PAR:
SC(V1.0) P36
Can be left unconnected if not using PCI.

PME:
DG(V1.0) P277
Can be left unconnected.

CLKOUT_PCI[0..4]:
22 ohm series resistor is recommend (single & double load) on PDG v1.1

OC0#~OC7#:
DG(V1.0)P214

Pin	Default Port Mapping
OC0#	Port0,Port1
OC1#	Port2,Port3

MiniWWAN

MiniWLAN

Express Card

Card Reader

Giga Bit LOM

PCI-E port 7/8 are not support in HM55 .
They are only in PM 55

U42B

PCI-E*

SMBus

Controller Link

PEG

From CLK BUFFER

Clock Flex

CLKOUT_PEG_A_P/N,CLKOUT_PEG_B_P/N,
CLKOUT_DMI_P/N,support GEN-1 and GEN-2

SML0CLK/SML0DATA:
DG(V1.1) P255: The 82577 SMBus signals (SMB_DATA and SMB_CLK) cannot be connected to any other devices other than the PCH. Connect the SMB_DATA and SMB_CLK pins to the PCH SML0DATA and SML0CLK pins, respectively.

CLKIN_PCILOOPBACK:
PDG (V1.1): 22 ohm series resistor is recommend 0214

CLKOUTFLEX[0..3]:
PDG v1.1: 22 ohm series resistor is recommend (PCI & non PCI routing, single & double load)

CLKOUTFLEX3 0214
EDS(V1.0) :support 48MHz 33MHz and 14.31818MHz.

Reserve capacitor pads for improving WWAN.

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

PCIE Clock Request

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

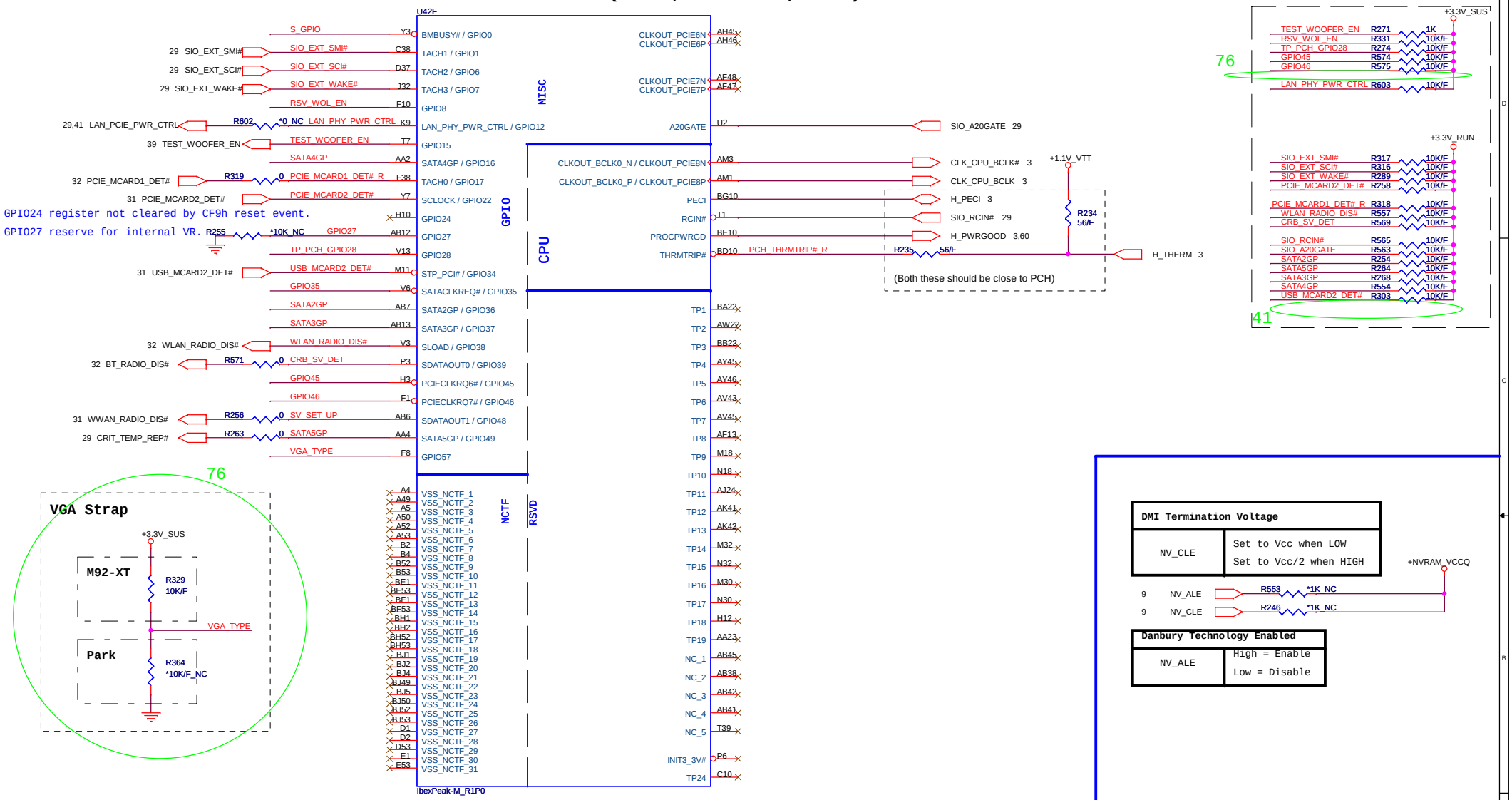
Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

QUANTA COMPUTER

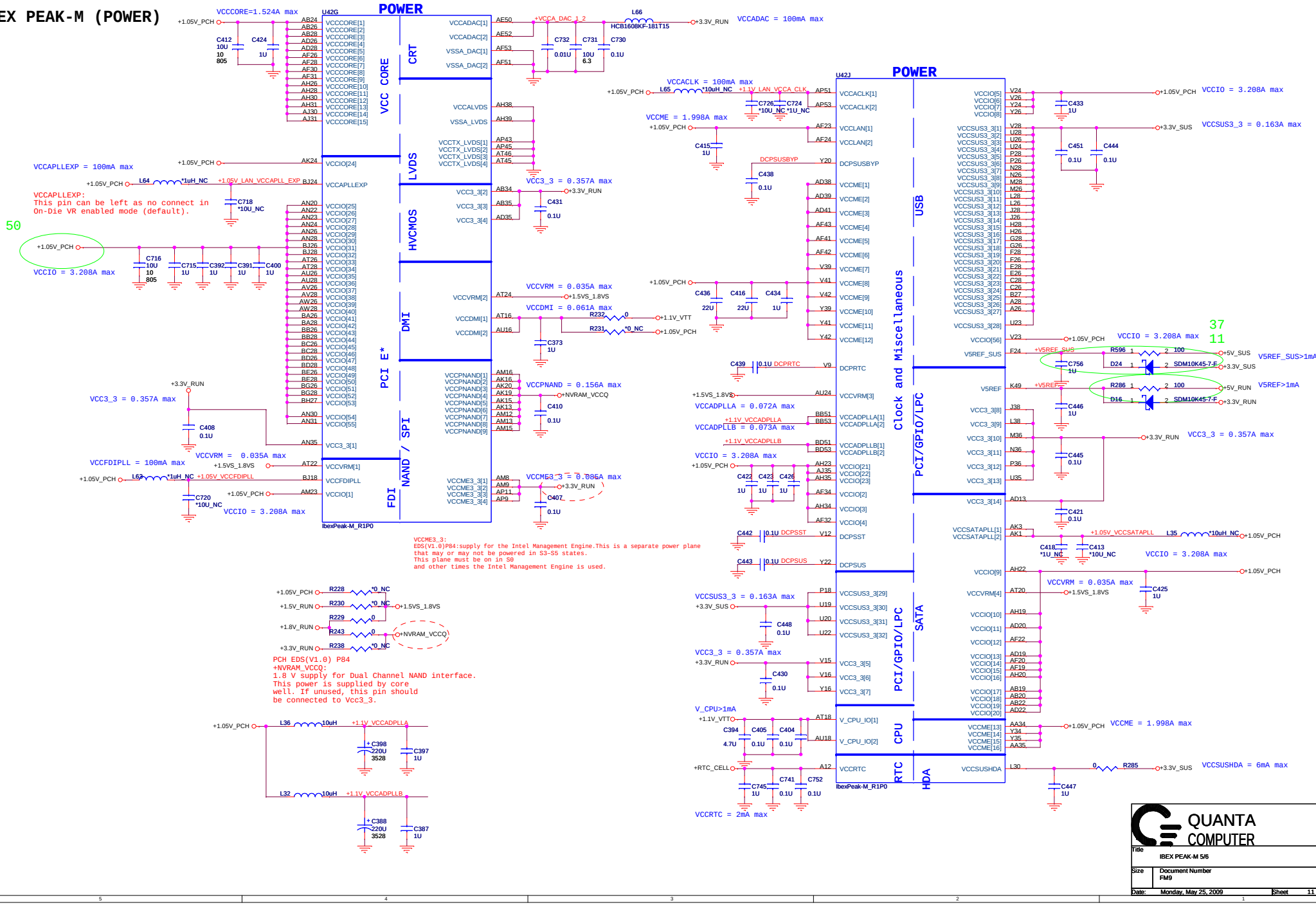
Title	IBEX PEAK-M 3/6	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 9 of 66	

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

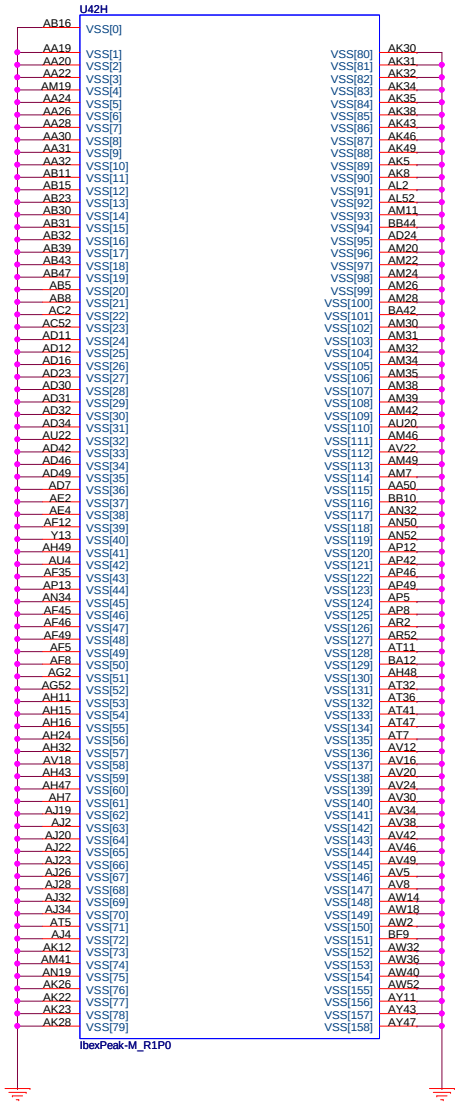


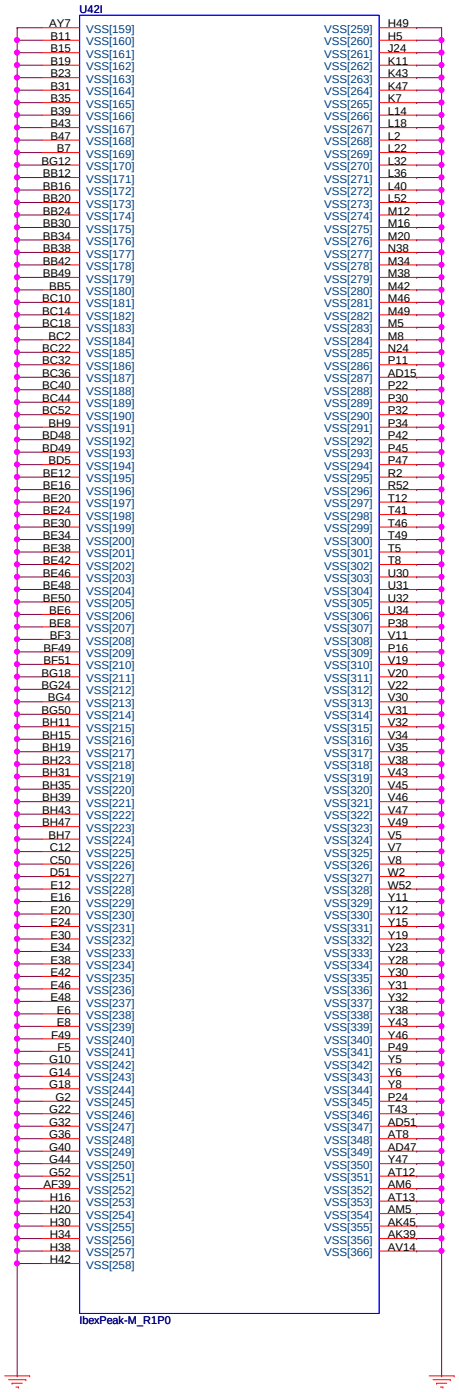
Title	IBEX PEAK-M 4/6		
Size	Document Number FM9		Rev 2B
Date:	Monday, May 25, 2009	Sheet 10 of 66	

IBEX PEAK-M (POWER)



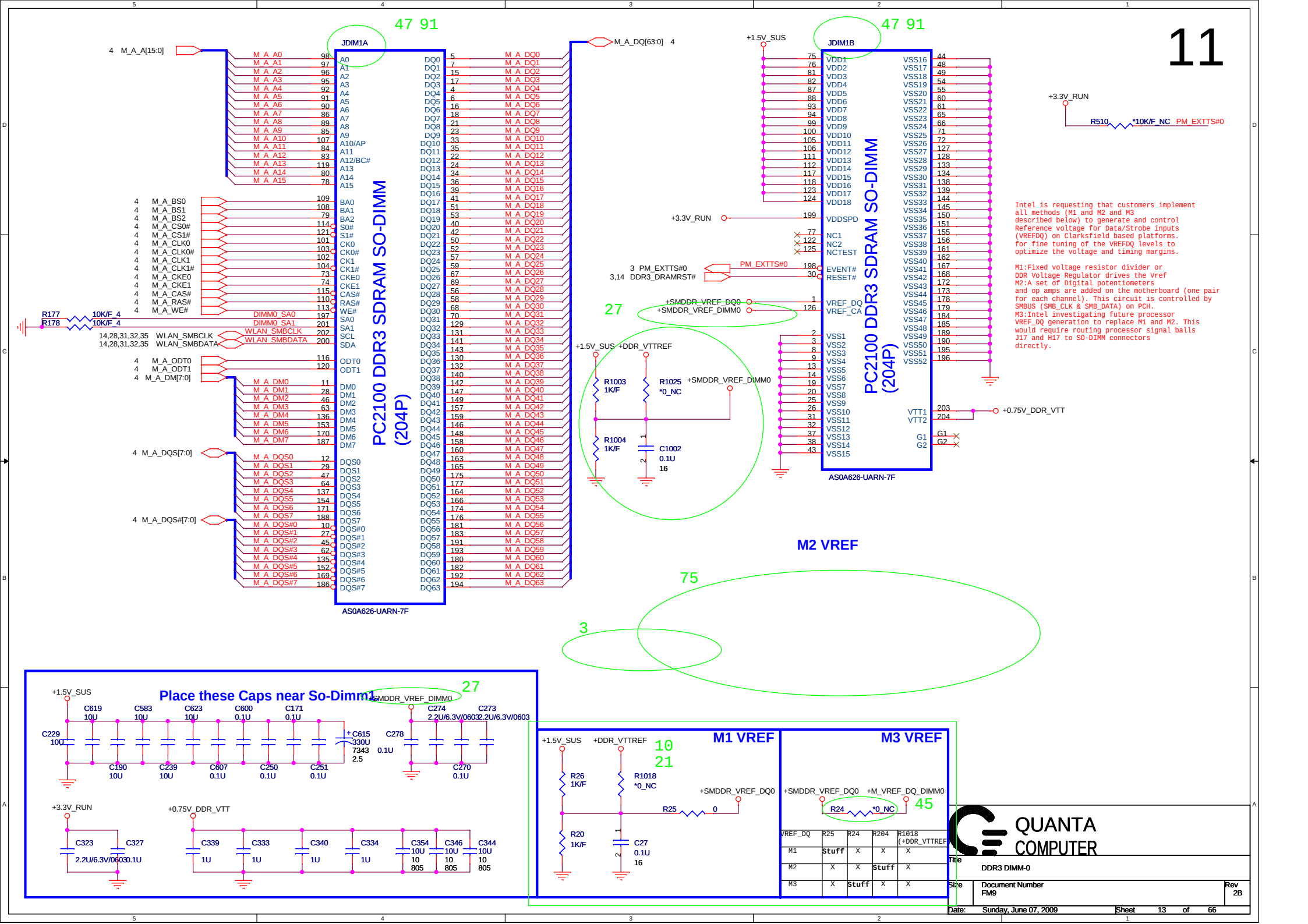
IBEX PEAK-M (GND)

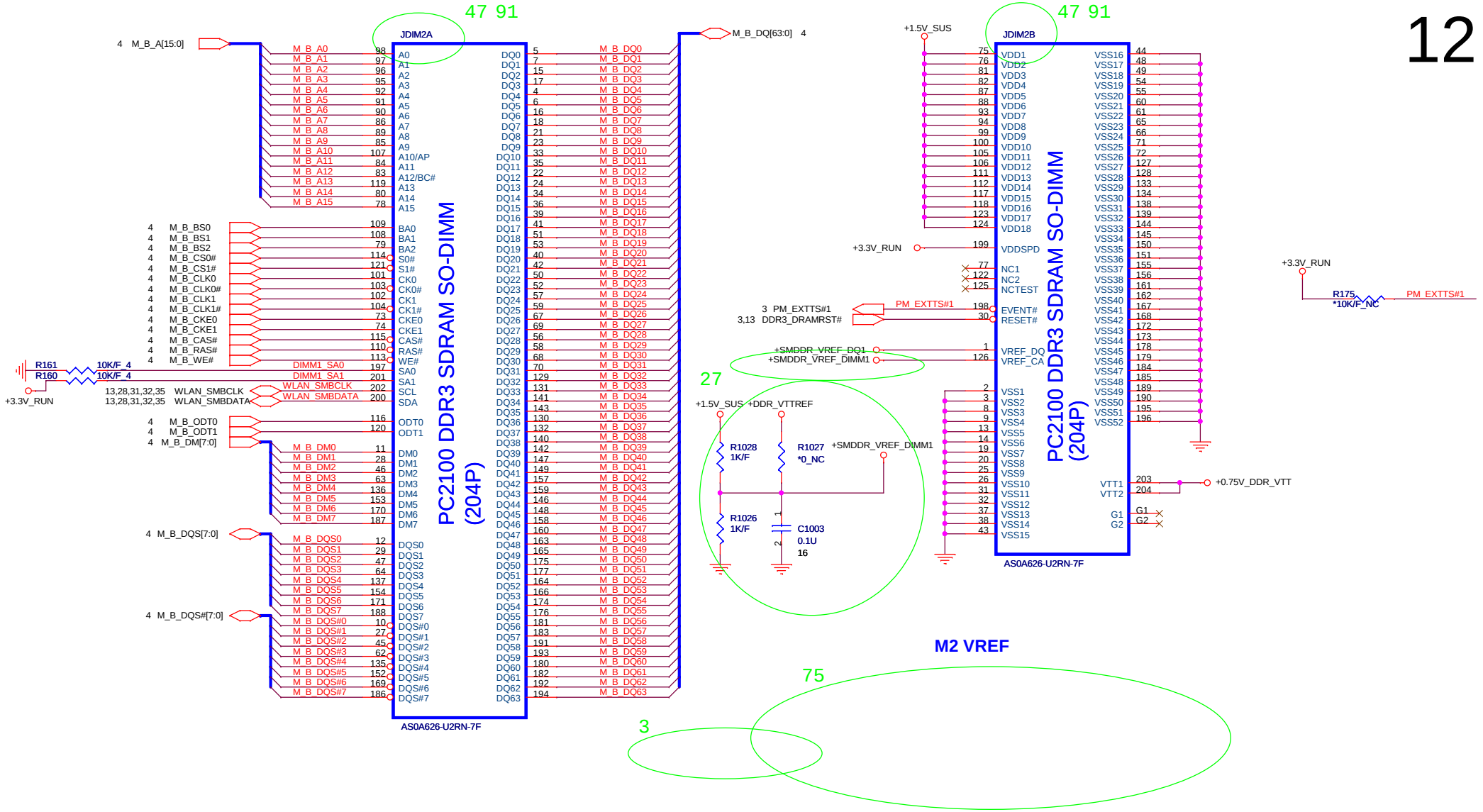




QUANTA COMPUTER

Title	IBEX PEAK-M 6/6	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 12 of 66	


JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
AS0A626-UARN-7F
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
AS0A626-UARN-7F
47 91
47 91
M2 VREF
M1 VREF
M3 VREF
Place these Caps near So-Dimm1
Intel is requesting that customers implement all methods (M1 and M2 and M3 described below) to generate and control Reference voltage for Data/Strobe inputs (VREFDQ) on Clarksfield based platforms. for fine tuning of the VREFDQ levels to optimize the voltage and timing margins.
M1:Fixed voltage resistor divider or DDR Voltage Regulator drives the Vref
M2:A set of Digital potentiometers and op amps are added on the motherboard (one pair for each channel). This circuit is controlled by SMBUS (SMB_CLK & SMB_DATA) on PCH.
M3:Intel investigating future processor VREF_DQ generation to replace M1 and M2. This would require routing processor signal balls J17 and H17 to SO-DIMM connectors directly.
QUANTA COMPUTER
DDR3 DIMM-0
Document Number FM9
Rev 2B
Date: Sunday, June 07, 2009
Sheet 13 of 66



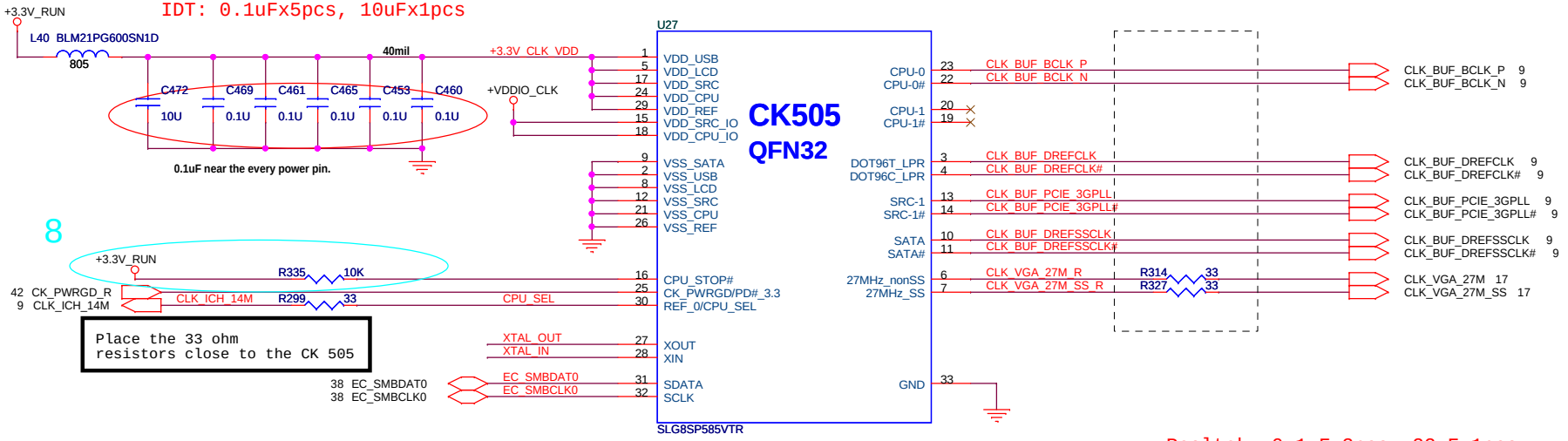
VREF_DQ	R1019	R28	R202	R1022 (+DDR_VTTREF)
M1	Stuff	X	X	X
M2	X	X	Stuff	X
M3	X	Stuff	X	X

QUANTA COMPUTER

Title	DDR3 DIMM-1		
Size	Document Number FM9		Rev 2B
Date: Sunday, June 07, 2009	Sheet 14 of 66		

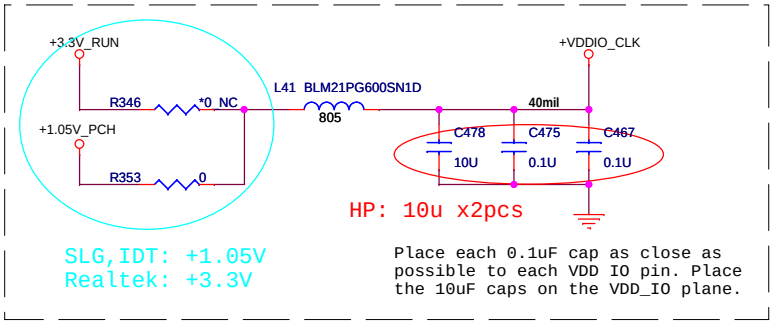
Realtek: 0.1uFx6pcs, 22uFx1pcs
IDT: 0.1uFx5pcs, 10uFx1pcs

Place within 0.5" of CLKGEN

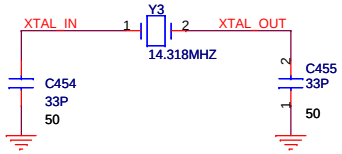


8

Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs

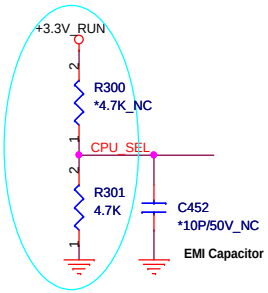


Add capacitor pads for improving WWAN.



+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.

7

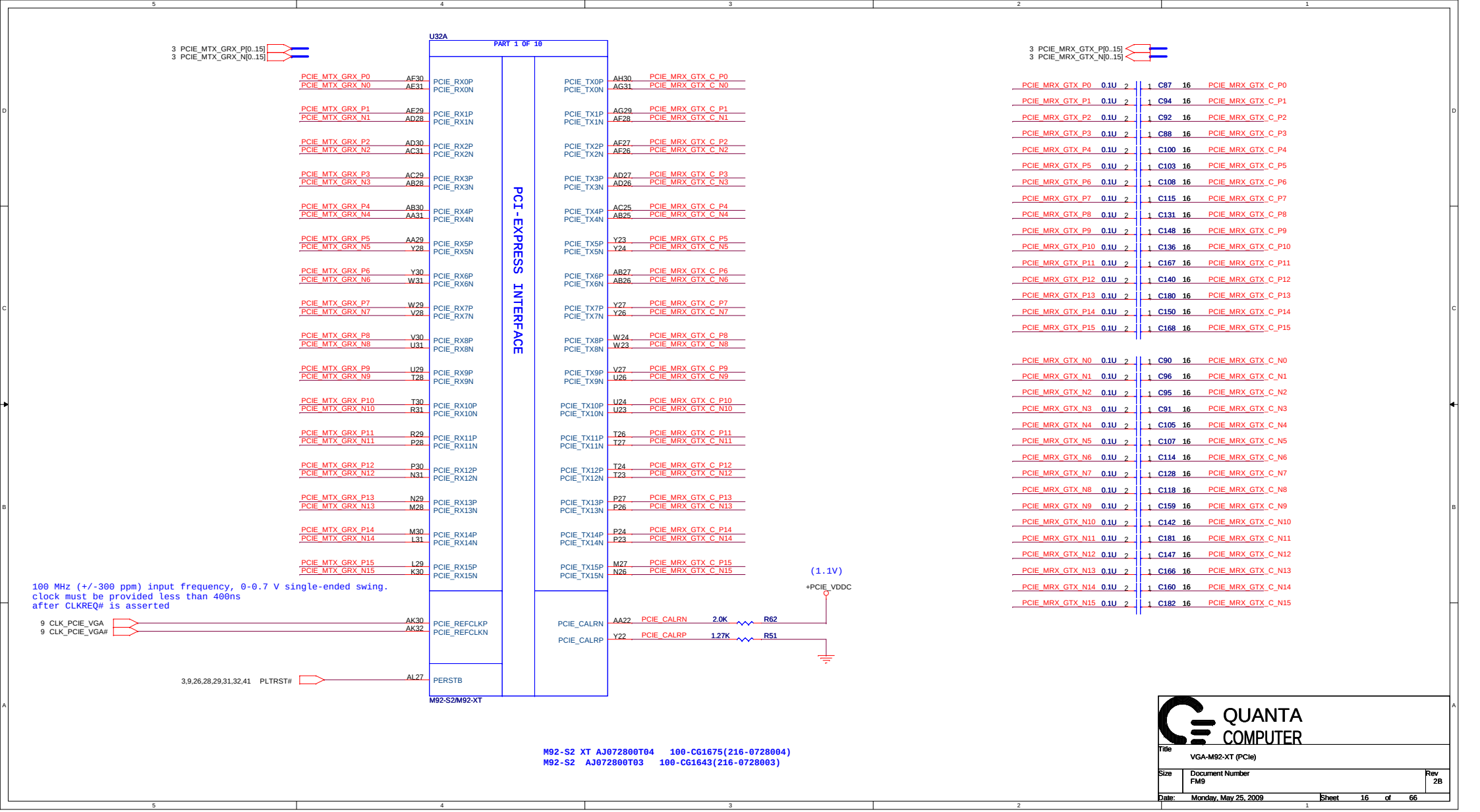


PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

QUANTA COMPUTER

Title	Clock Generator	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 15 of 66	


U32A
PART 1 OF 10
PCI-EXPRESS INTERFACE
M92-S2/M92-XT
3 PCIE_MTX_GRX_P[0..15]
3 PCIE_MTX_GRX_N[0..15]
PCIE_MTX_GRX_P0 AE30 PCIE_RX0P
PCIE_MTX_GRX_N0 AE31 PCIE_RX0N
PCIE_MTX_GRX_P1 AE29 PCIE_RX1P
PCIE_MTX_GRX_N1 AD28 PCIE_RX1N
PCIE_MTX_GRX_P2 AD30 PCIE_RX2P
PCIE_MTX_GRX_N2 AC31 PCIE_RX2N
PCIE_MTX_GRX_P3 AC29 PCIE_RX3P
PCIE_MTX_GRX_N3 AB28 PCIE_RX3N
PCIE_MTX_GRX_P4 AB30 PCIE_RX4P
PCIE_MTX_GRX_N4 AA31 PCIE_RX4N
PCIE_MTX_GRX_P5 AA29 PCIE_RX5P
PCIE_MTX_GRX_N5 Y28 PCIE_RX5N
PCIE_MTX_GRX_P6 Y30 PCIE_RX6P
PCIE_MTX_GRX_N6 W31 PCIE_RX6N
PCIE_MTX_GRX_P7 W29 PCIE_RX7P
PCIE_MTX_GRX_N7 V28 PCIE_RX7N
PCIE_MTX_GRX_P8 V30 PCIE_RX8P
PCIE_MTX_GRX_N8 U31 PCIE_RX8N
PCIE_MTX_GRX_P9 U29 PCIE_RX9P
PCIE_MTX_GRX_N9 T28 PCIE_RX9N
PCIE_MTX_GRX_P10 T30 PCIE_RX10P
PCIE_MTX_GRX_N10 R31 PCIE_RX10N
PCIE_MTX_GRX_P11 R29 PCIE_RX11P
PCIE_MTX_GRX_N11 P28 PCIE_RX11N
PCIE_MTX_GRX_P12 P30 PCIE_RX12P
PCIE_MTX_GRX_N12 N31 PCIE_RX12N
PCIE_MTX_GRX_P13 N29 PCIE_RX13P
PCIE_MTX_GRX_N13 M28 PCIE_RX13N
PCIE_MTX_GRX_P14 M30 PCIE_RX14P
PCIE_MTX_GRX_N14 L31 PCIE_RX14N
PCIE_MTX_GRX_P15 L29 PCIE_RX15P
PCIE_MTX_GRX_N15 K30 PCIE_RX15N
PCIE_TX0P AH30 PCIE_MRX_GTX_C_P0
PCIE_TX0N AG31 PCIE_MRX_GTX_C_N0
PCIE_TX1P AG29 PCIE_MRX_GTX_C_P1
PCIE_TX1N AF28 PCIE_MRX_GTX_C_N1
PCIE_TX2P AF27 PCIE_MRX_GTX_C_P2
PCIE_TX2N AF26 PCIE_MRX_GTX_C_N2
PCIE_TX3P AD27 PCIE_MRX_GTX_C_P3
PCIE_TX3N AD26 PCIE_MRX_GTX_C_N3
PCIE_TX4P AC25 PCIE_MRX_GTX_C_P4
PCIE_TX4N AB25 PCIE_MRX_GTX_C_N4
PCIE_TX5P Y23 PCIE_MRX_GTX_C_P5
PCIE_TX5N Y24 PCIE_MRX_GTX_C_N5
PCIE_TX6P AB27 PCIE_MRX_GTX_C_P6
PCIE_TX6N AB26 PCIE_MRX_GTX_C_N6
PCIE_TX7P Y27 PCIE_MRX_GTX_C_P7
PCIE_TX7N Y26 PCIE_MRX_GTX_C_N7
PCIE_TX8P W24 PCIE_MRX_GTX_C_P8
PCIE_TX8N W23 PCIE_MRX_GTX_C_N8
PCIE_TX9P V27 PCIE_MRX_GTX_C_P9
PCIE_TX9N U26 PCIE_MRX_GTX_C_N9
PCIE_TX10P U24 PCIE_MRX_GTX_C_P10
PCIE_TX10N U23 PCIE_MRX_GTX_C_N10
PCIE_TX11P T26 PCIE_MRX_GTX_C_P11
PCIE_TX11N T27 PCIE_MRX_GTX_C_N11
PCIE_TX12P T24 PCIE_MRX_GTX_C_P12
PCIE_TX12N T23 PCIE_MRX_GTX_C_N12
PCIE_TX13P P27 PCIE_MRX_GTX_C_P13
PCIE_TX13N P26 PCIE_MRX_GTX_C_N13
PCIE_TX14P P24 PCIE_MRX_GTX_C_P14
PCIE_TX14N P23 PCIE_MRX_GTX_C_N14
PCIE_TX15P M27 PCIE_MRX_GTX_C_P15
PCIE_TX15N N26 PCIE_MRX_GTX_C_N15
100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing.
clock must be provided less than 400ns
after CLKREQ# is asserted
9 CLK_PCIE_VGA AK30 PCIE_REFCLKP
9 CLK_PCIE_VGA# AK32 PCIE_REFCLKN
3,9,26,28,29,31,32,41 PLTRST# AL27 PERSTB
PCIE_CALRN AA22 PCIE_CALRN 2.0K R62
PCIE_CALRP Y22 PCIE_CALRP 1.27K R51
(1.1V)
+PCIE_VDDC
3 PCIE_MRX_GTX_P[0..15]
3 PCIE_MRX_GTX_N[0..15]
PCIE_MRX_GTX_P0 0.1U 2 1 C87 16 PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1 0.1U 2 1 C94 16 PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2 0.1U 2 1 C92 16 PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3 0.1U 2 1 C88 16 PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4 0.1U 2 1 C100 16 PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5 0.1U 2 1 C103 16 PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6 0.1U 2 1 C108 16 PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7 0.1U 2 1 C115 16 PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8 0.1U 2 1 C131 16 PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9 0.1U 2 1 C148 16 PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10 0.1U 2 1 C136 16 PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11 0.1U 2 1 C167 16 PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12 0.1U 2 1 C140 16 PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13 0.1U 2 1 C180 16 PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14 0.1U 2 1 C150 16 PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15 0.1U 2 1 C168 16 PCIE_MRX_GTX_C_P15
PCIE_MRX_GTX_N0 0.1U 2 1 C90 16 PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1 0.1U 2 1 C96 16 PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2 0.1U 2 1 C95 16 PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3 0.1U 2 1 C91 16 PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4 0.1U 2 1 C105 16 PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5 0.1U 2 1 C107 16 PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6 0.1U 2 1 C114 16 PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7 0.1U 2 1 C128 16 PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8 0.1U 2 1 C118 16 PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9 0.1U 2 1 C159 16 PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10 0.1U 2 1 C142 16 PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11 0.1U 2 1 C181 16 PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12 0.1U 2 1 C147 16 PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13 0.1U 2 1 C166 16 PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14 0.1U 2 1 C160 16 PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15 0.1U 2 1 C182 16 PCIE_MRX_GTX_C_N15
M92-S2 XT AJ072800T04 100-CG1675(216-0728004)
M92-S2 AJ072800T03 100-CG1643(216-0728003)
QUANTA COMPUTER
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VGA-M92-XT (PCIe)
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MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB		0	0	0
256MB		0	0	1
64MB		0	1	0
512MB		1	0	0

+3.3V_DELAY

R436 10K RAM_CFG0
R435 *10K_NC RAM_CFG1
R437 *10K_NC RAM_CFG2

GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	FM9 setting
GPIO0	GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO(2) - BIF_GEN2_EN (5.0 GTs Enable) 0 : Strap Controlled Gen1 1 : Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO_5_AC_BATT 0 : Battery saving mode = 0.0 V 1 : AC (Performance mode) = 3.3 V	0
GPIO6	ATI Internal use only	0
HSYNC (AH26) / VSYNC (AJ27)	00: No Audio function 01: Audio for DisplayPort only 10: Audio for DisplayPort only and HDMI if dongle is detected 11: Audio for both DisplayPort and HDMI. HDMI must only be enabled on systems that are legally entitled. it is the responsibility of the system designer to ensure that the system is entitled to support this feature	11

+3.3V_DELAY

R430 *10K_NC GPIO0
R426 *10K_NC GPIO1
R61 *10K_NC GPIO2
R429 *10K_NC GPIO3
R428 *10K_NC GPIO4
R68 *10K_NC GPIO5

R55 10K HDMI_HD_EN
R438 *10K_NC TEMP_FAIL
R432 10K GFX_CLKREQ#
R384 10K VGAVSYNC
R383 10K VGAHSYNC
R1003 10K DAC1_VGAVSYNC
R1002 10K DAC1_VGAHSYNC

6
26

R440 10K TEMP_FAIL

26

DAC1_VGAVSYNC \ DAC1_VGAHSYNC	HD Audio straps
0\0	No audio function
0\1	Audio for DisplayPort only
1\0	Audio for DisplayPort and HDMI if dongle is detected
1\1	Audio for both DisplayPort and HDMI

+1.8V_RUN_GFX

R56 10K RAM_TYPE_CFG0
R422 *10K_NC RAM_TYPE_CFG1
R419 *10K_NC RAM_TYPE_CFG2

+3.3V_DELAY R32 0 603 +3.3V_RUN

95

For Park S3:
Install All components in this Box
R431,R432,R427,L52,C1004,C545,C1005,L23
,C111,R421,L002,C1008,C1007,C1006,R407

For M92-S2: DO NOT Install any Component
in this Box.

+1.8V_RUN_GFX L52 *BLM15BD121SN1D_NC +1.8V_RUN_GFX_R C545 *1U_NC
+PCIE_VDDC L23 *BLM15BD121SN1D_NC C111 *1U_NC
+1.8V_RUN_GFX_R

94 57 89 82 94 57 89 94

R431 1 2 *0_NC U1
R423 1 2 *0_NC AA1
R427 1 2 *0_NC

RAM_TYPE_CFG0 AB2
RAM_TYPE_CFG1 AC10
RAM_TYPE_CFG2 AC5

6

OSC_SPREAD R408 *0_reserve
15 CLK_VGA_27M_SS R416 *0_NC CLK_VGA_27M_SSIN_R
R409 *10K_NC
15 CLK_VGA_27M R417 100/F R45 0
R410 120/F
OSC_OUT R404 *182R_reserve XTALIN 21
R406 *1M_reserve R46 *221/F_reserve
Y4 *27MHZ_reserve R392 *0_reserve XTALOUT 21
R394 1M_reserve
C535 *12P/50V_reserve C534 *12P/50V_reserve
50 50

Spread Spectrum

If U4, the discrete spread spectrum chip is not used, then pop R48 in order to pull-down BXTALOUT for EMI reasons.

+3.3V_RUN
R390 *10K_reserve R391 *10K_reserve
R393 *10K_reserve
OSC_OUT
R411 *0_reserve
OSC_SPREAD
U31 XIN/CLKIN XOUT VSS VDD SO PD# SSCLK REFCLK
*P1819GF-08SR_reserve
+3VL C531 *10U_reserve L54 *BLM11A05S_reserve C542 *0.1U_reserve +3.3V_RUN
805 10

	S0
-1.75% (DOWN)	0

U32B PART 2 OF 18

DVP PORT
DVPCLK
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCNTL_MVP_0
DVPCNTL_MVP_1
DVPDATA_0 … DVPDATA_23

I/O
GPIO_0
GPIO_1
GPIO_2
GPIO_3_SMBDATA
GPIO_4_SMBCLK
GPIO_5_AC_BATT
GPIO_6_TACH
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16_SSIN
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
HPD1
VREFG
RESERVED
NC_PWRGOOD
RSVD#8
RSVD#9
NC#1
NC#2
RSVD#3
RSVD#2
RSVD#1
TESTEN

50 GFX_CORE_CNTRL2 29 PANEL_BKEN HDMI_HD_EN
RAM_CFG0 RAM_CFG1 RAM_CFG2
101
50 GFX_CORE_CNTRL0 CLK_VGA_27M_SSIN_R
19 THERMAL_INT# *0_NC
TEMP_FAIL
50 GFX_CORE_CNTRL1 18 BB_ENA
GFX_CLKREQ#
R439 2 1K
T45 PAD T46 PAD T8 PAD T10 PAD T49 PAD T48 PAD T47 PAD T13 PAD
T5 PAD T44 PAD T41 PAD T43 PAD T2 PAD
+1.8V_RUN_GFX R382 499/F R396 249/F C527 0.1U
57 For M92: No stuff R1011
For Park: Stuff R1011
62 R1011 *10K_NC R1034 0
94
84 R64 10K
24 ENVDD 24 BIA_PWM
R396 0
R50 10K
+3.3V_DELAY R88 10K R42 10K
19 TEST_EN
AF24 is TESTEN on both M92S2 and ParkS3. Implement 10K ohm PU and PD for both and connected to K7 pin
62 58 69 81 96

DAC1
R AM26 AK26
G AL25 AJ25
B AH24 AG25
HSYNC AH26 DAC1_VGAHSYNC
VSYNC AJ27 DAC1_VGAVSYNC
AVDD AG24 +1.8V_RUN_GFX AVDD=70mA max C101 *0.1U_NC
AVSSQ AE22
VDD1DI AE23 +1.8V_RUN_GFX VDD1DI=45mA max C112 *0.1U_NC
VSS1DI AD23
RSET AD22 RSET R49 499R

DAC2
R2 AM12 AK12 VGA_RED VGA_RED 25
G2 AL11 AJ11 VGA_GRN VGA_GRN 25
B2 AK10 AL9 VGA_BLU VGA_BLU 25
H2SYNC AL13 VGAHSYNC VGAHSYNC 25
V2SYNC AJ13 VGAVSYNC VGAVSYNC 25
C AH12
Y AM10
COMP AJ9
A2VDD AE20 +A2VDD A2VDD=65mA max C548 0.01U
A2VDDQ AE17 +A2VDDQ L48 BLM15BD121SN1D A2VDDQ=1mA max C528 0.1U C522 1U
A2VSSQ AE19
Keep A2VSSQ away from noisy ground.
VDD2DI AD19 +VDD2DI VDD2DI=40mA max C547 0.01U
VSS2DI AC19
Place very close to ASIC balls
R2SET AG13 R2SET R401 715

+3.3V_DELAY R425 10K R424 10K
HPD1 Q60 MMST3904-7-F Q59 DTC114TUAT106 HDMI_DET 24 R420 100K

DIS only
VGA_BLU R398 150/F
VGA_GRN R399 150/F
VGA_RED R400 150/F
Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

Memory Straps	RAM_TYPE _CFG2	RAM_TYPE _CFG1	RAM_TYPE _CFG0	Quanta PN (QuantaBuy)	Quanta PN (WinBuy)	Vendor PN	31 level PN
800MHz 512MB(64M*16) Samsung	0	0	1	AKD5LGGT502		K4W1G1646E-HC12	
800MHz 512MB(64M*16) Hynix	0	1	0	AKD5LZGTW00		H5TQ1G63BFR-12C	

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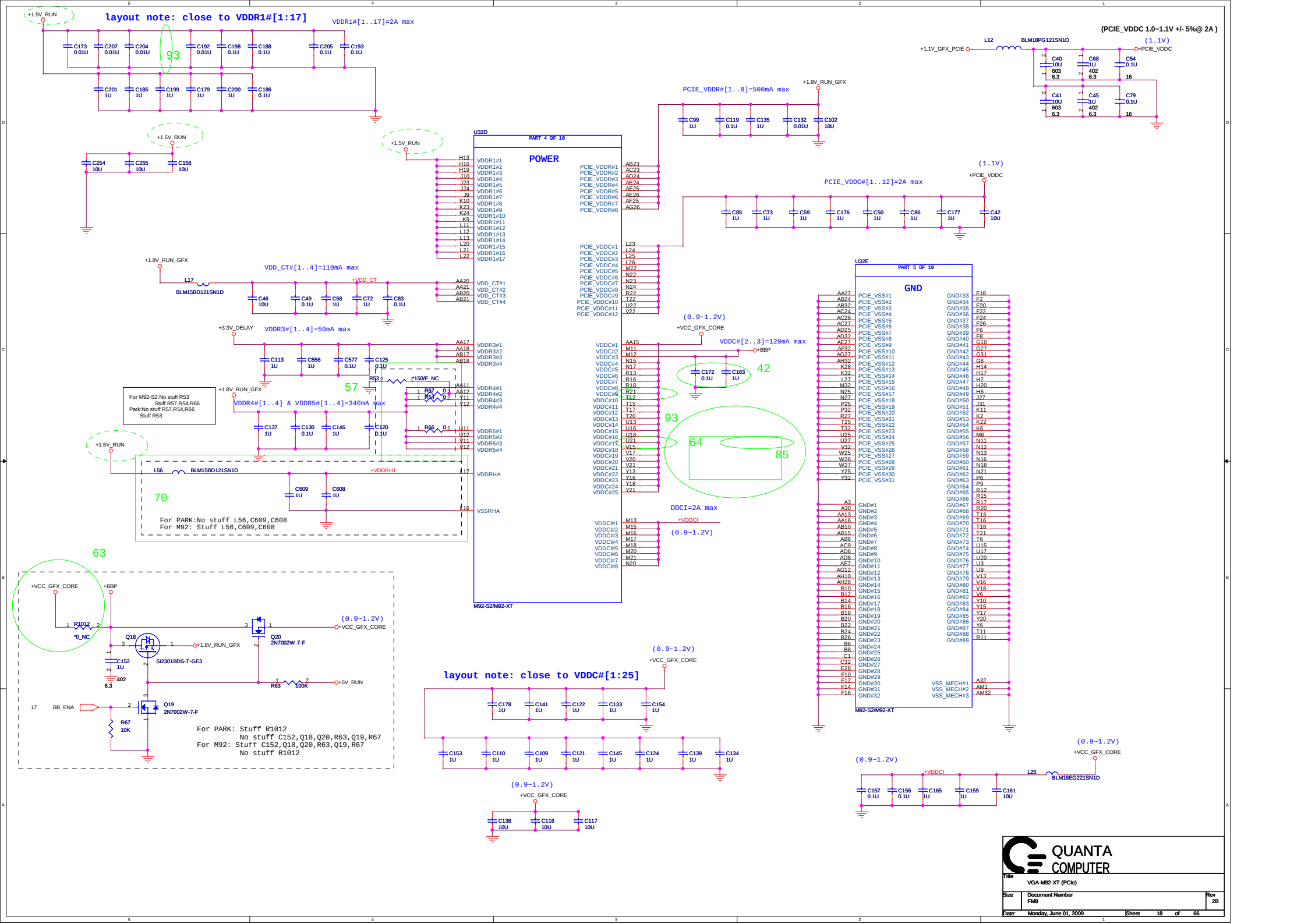
layout note: close to VDDR1#[1:17]
VDDR1#[1..17]=2A max
(PCIE_VDDC 1.0~1.1V +/- 5%@ 2A)
+1.5V_RUN
+1.8V_RUN_GFX
+1.1V_GFX_PCIE
+PCIE_VDDC
(1.1V)
PCIE_VDDR#[1..8]=500mA max
PCIE_VDDC#[1..12]=2A max
VDD_CT#[1..4]=110mA max
VDDR3#[1..4]=50mA max
VDDR4#[1..4] & VDDR5#[1..4]=340mA max
+3.3V_DELAY
+VDD_CT
+VDDRH1
U32D
PART 4 OF 10
POWER
U32E
PART 5 OF 10
GND
M92-S2/M92-XT
(0.9~1.2V)
+VCC_GFX_CORE
VDDC#[2..3]=120mA max
+BBP
DDCI=2A max
+VDDCI
layout note: close to VDDC#[1:25]
For M92-S2:No stuff R53
Stuff R57,R54,R66
Park:No stuff R57,R54,R66
Stuff R53
For PARK:No stuff L56,C609,C608
For M92: Stuff L56,C609,C608
For PARK: Stuff R1012
No stuff C152,Q18,Q20,R63,Q19,R67
For M92: Stuff C152,Q18,Q20,R63,Q19,R67
No stuff R1012
BLM15BD121SN1D
BLM18PG121SN1D
BLM18EG221SN1D
SI2301BDS-T-GE3
2N7002W-7-F
BB_ENA
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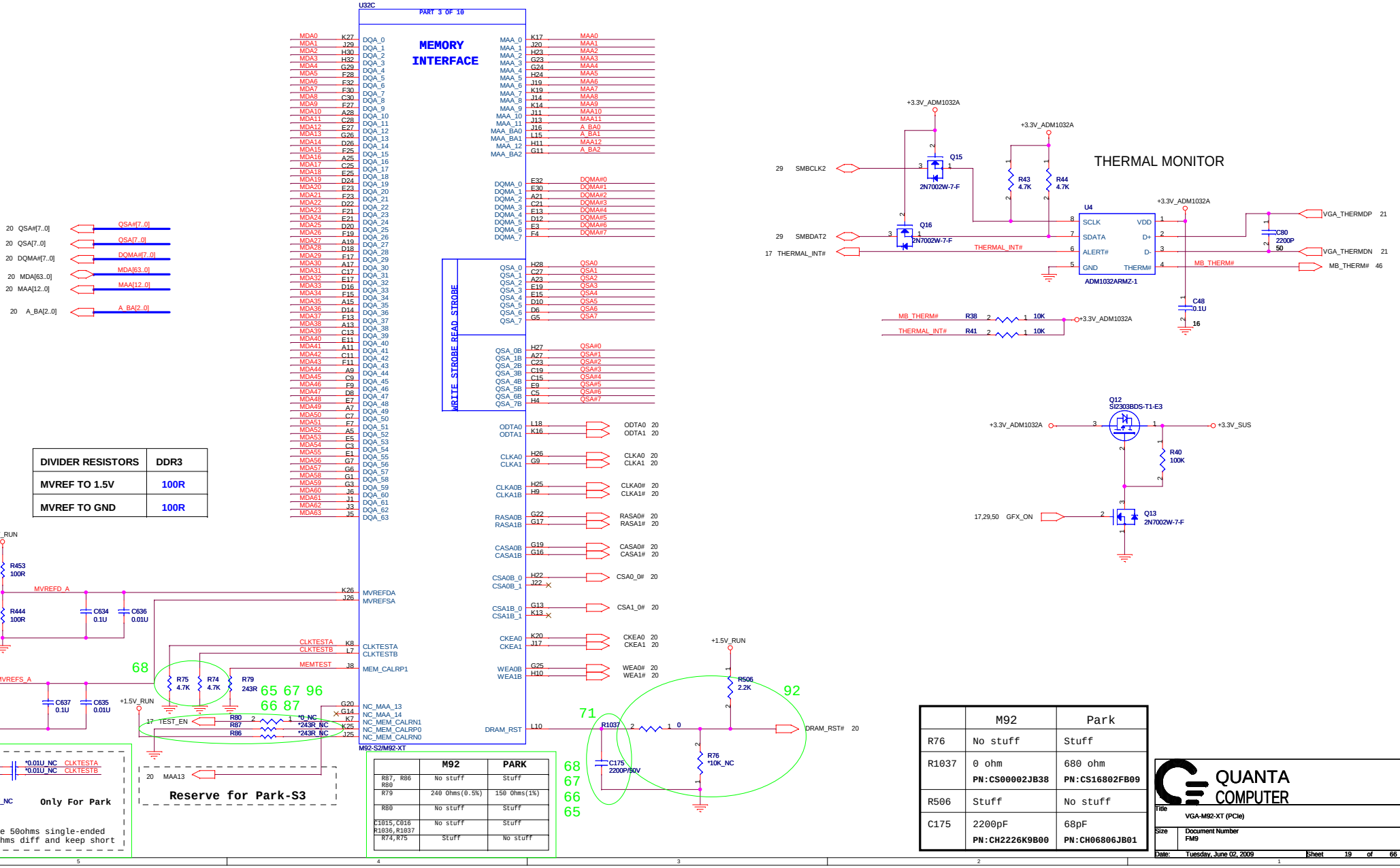
MEMORY INTERFACE



DIVIDER RESISTORS	DDR3
MVREF TO 1.5V	100R
MVREF TO GND	100R

	M92	PARK
R87, R86 R80	No stuff	Stuff
R79	240 Ohms(0.5%)	150 Ohms(1%)
R80	No stuff	Stuff
C1015,C016 R1036,R1037	No stuff	Stuff
R74,R75	Stuff	No stuff

	M92	Park
R76	No stuff	Stuff
R1037	0 ohm PN:CS00002JB38	680 ohm PN:CS16802FB09
R506	Stuff	No stuff
C175	2200pF PN:CH2226K9B00	68pF PN:CH06806JB01

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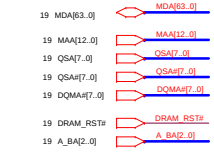
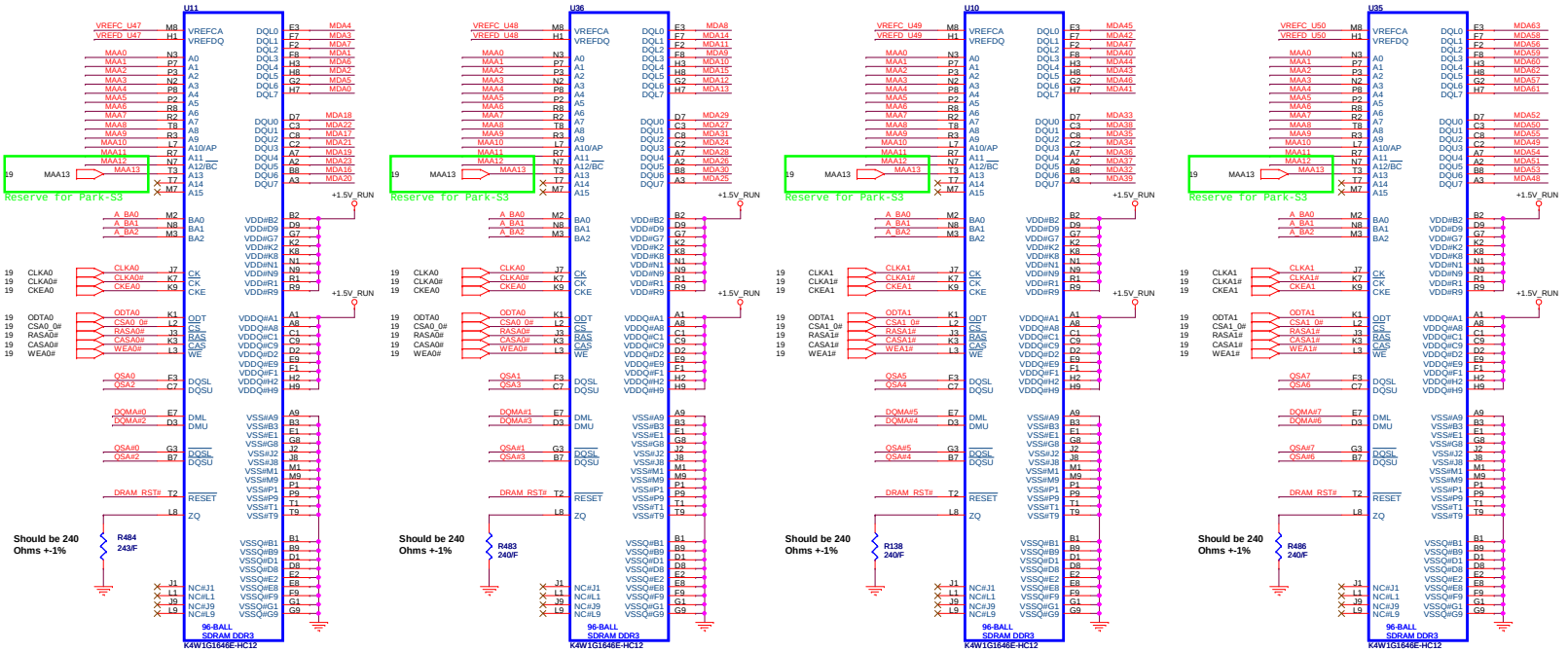
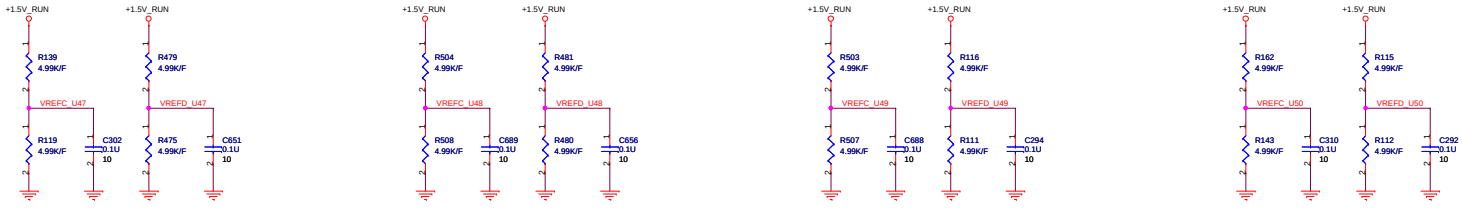
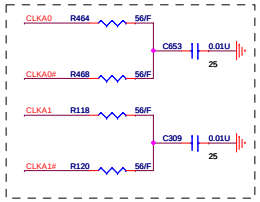
DDR3



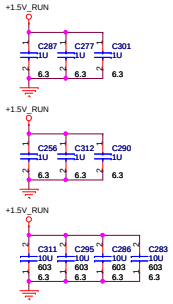




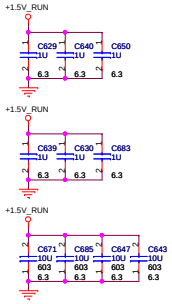
Placement has to be close to VRAM



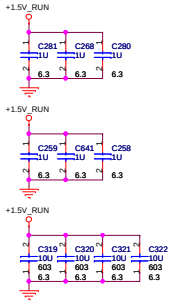
close to U47



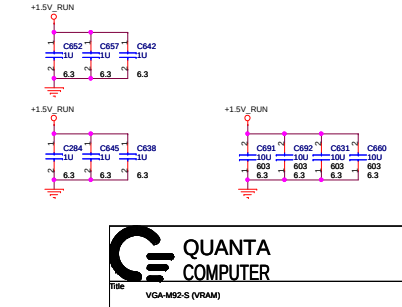
close to U48



close to U49



close to U50



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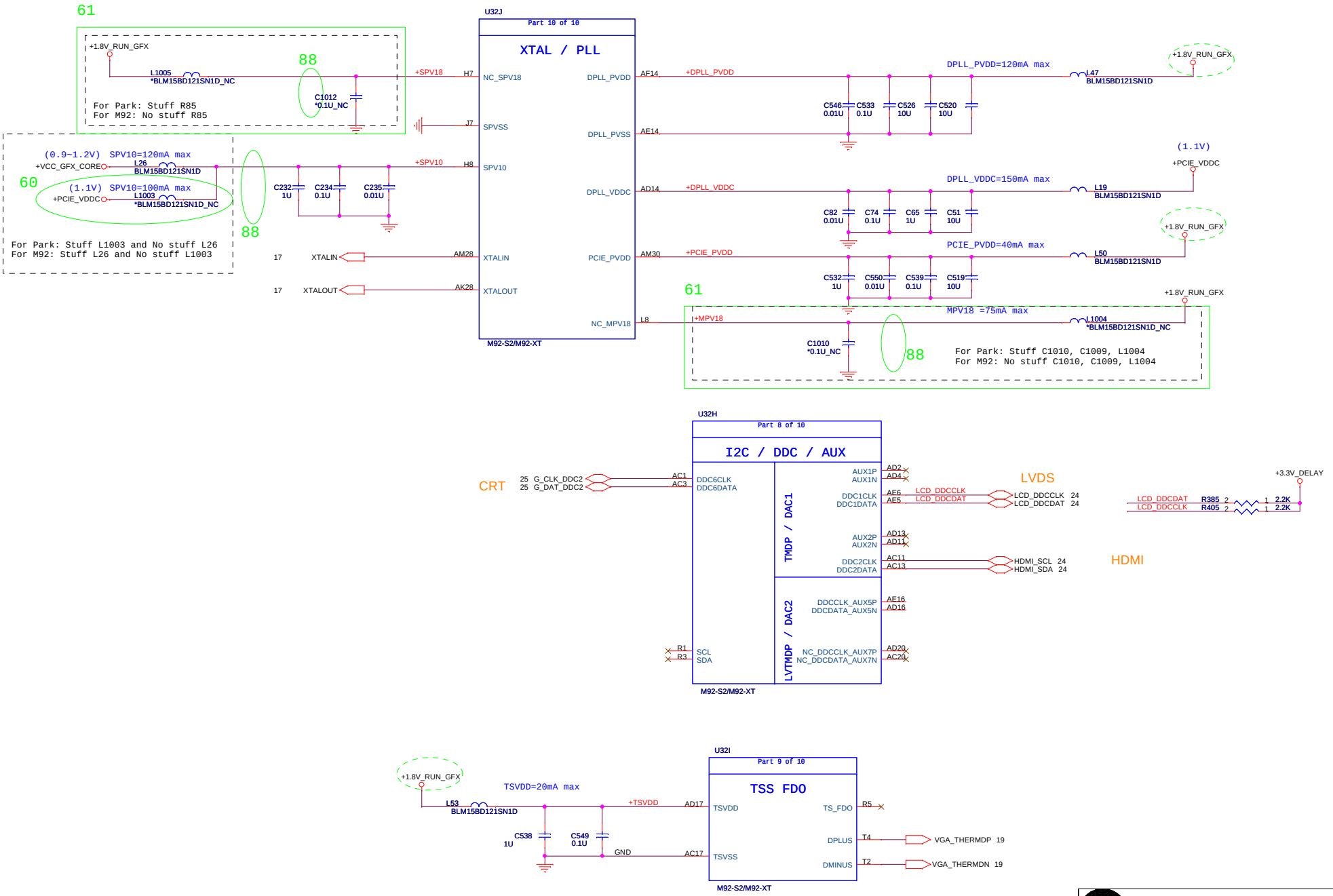

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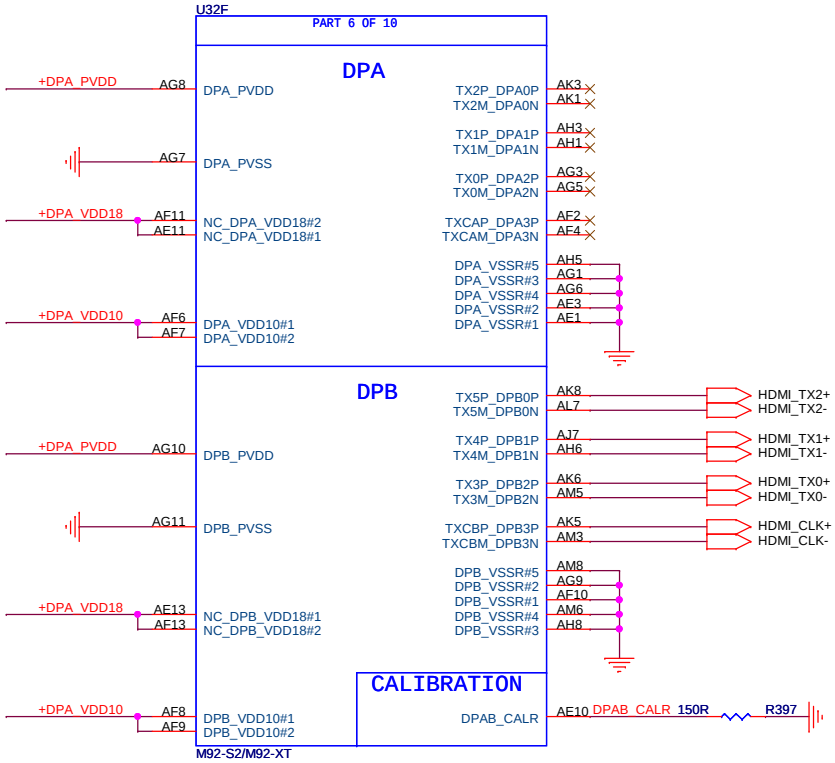
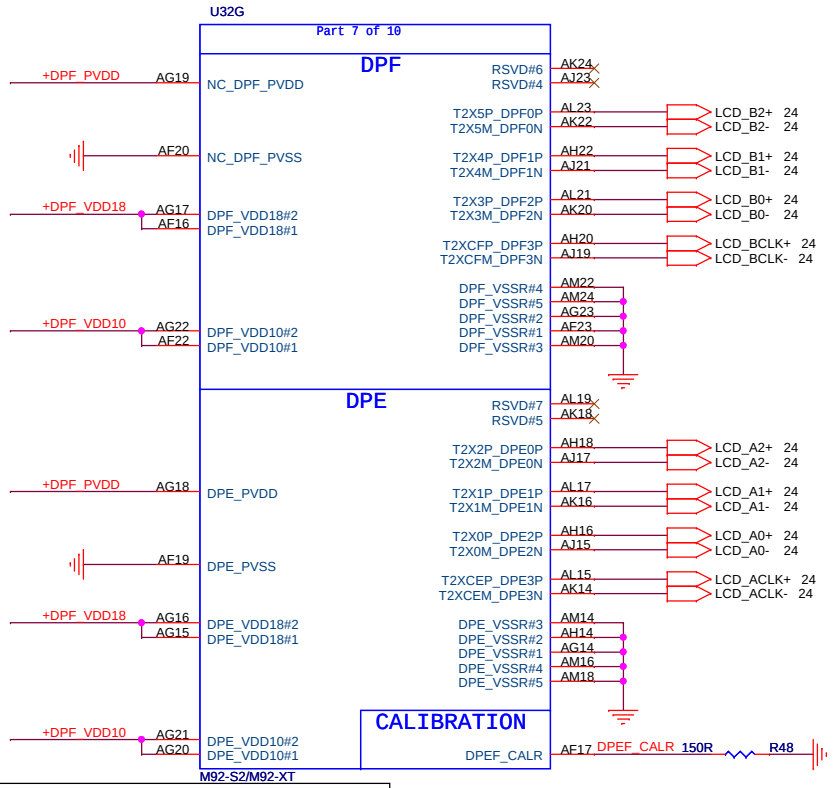
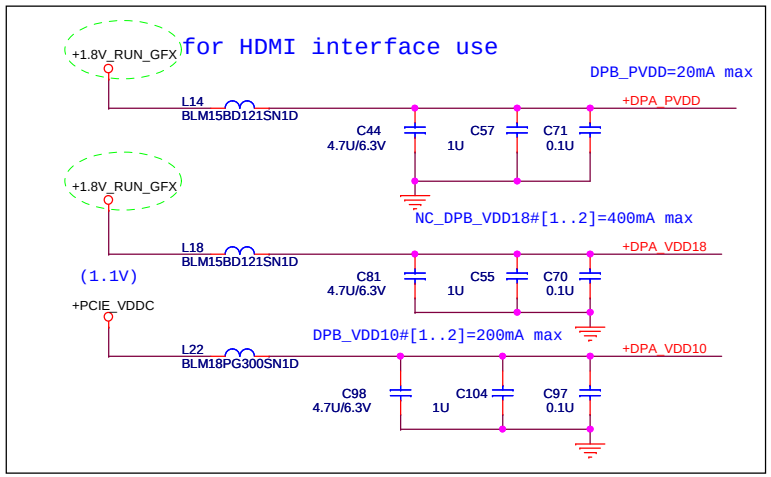
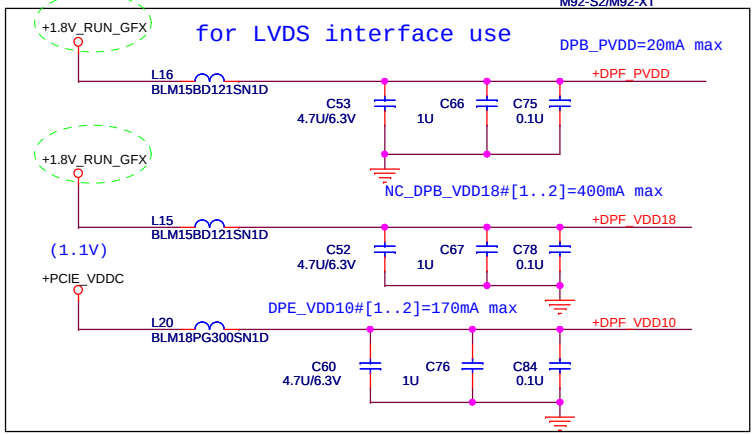
TMDP(HDMI) INTERFACE



LVDS INTERFACE







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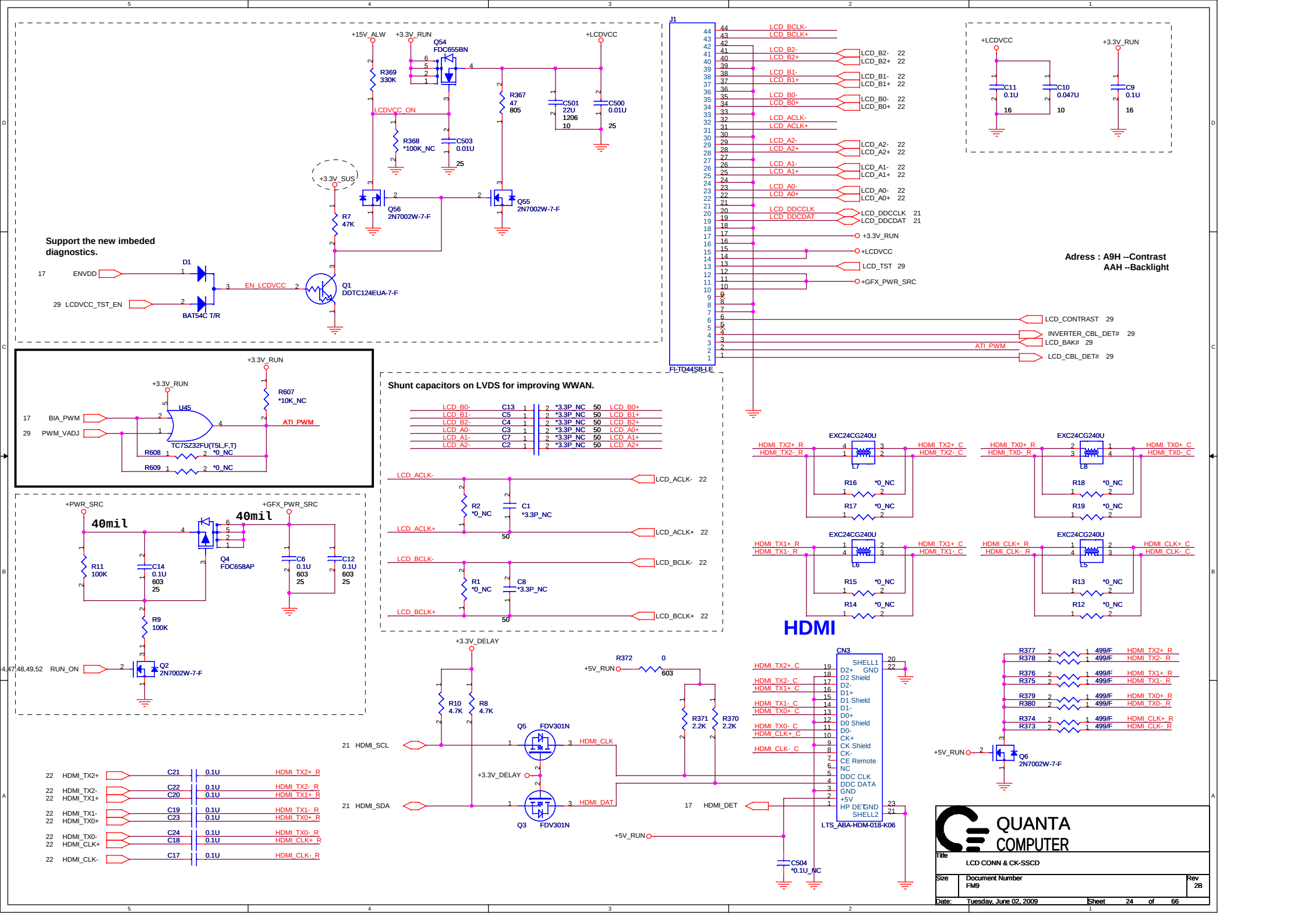
Support the new imbeded diagnostics.
Adress : A9H --Contrast
AAH --Backlight
Shunt capacitors on LVDS for improving WWAN.
HDMI
40mil
40mil
FI-TD44SB-LE
LTS_ABA-HDM-018-K06
QUANTA COMPUTER
LCD CONN & CK-SSCD
FM9
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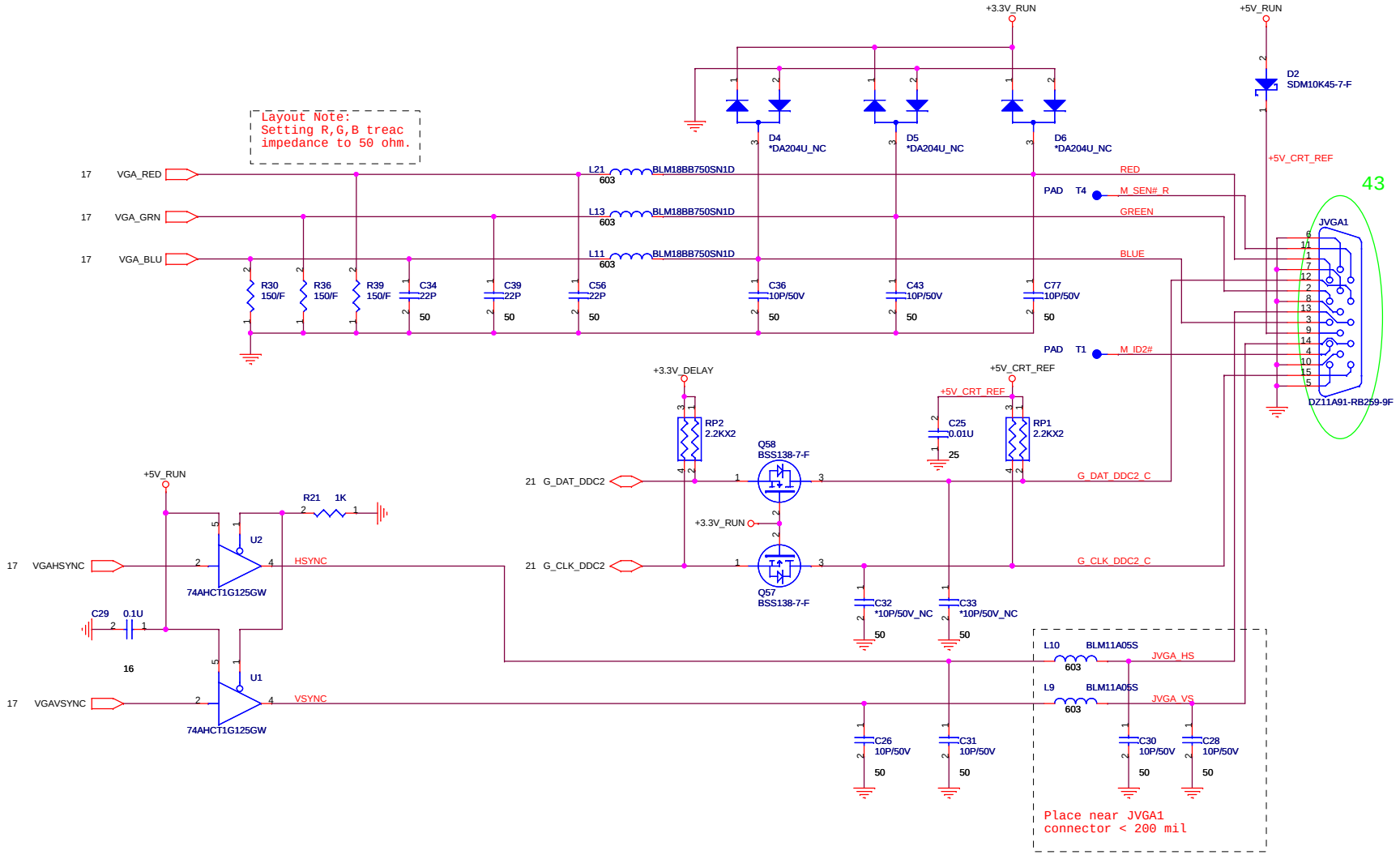

QUANTA COMPUTER			
Title	CRT&TV CONN		
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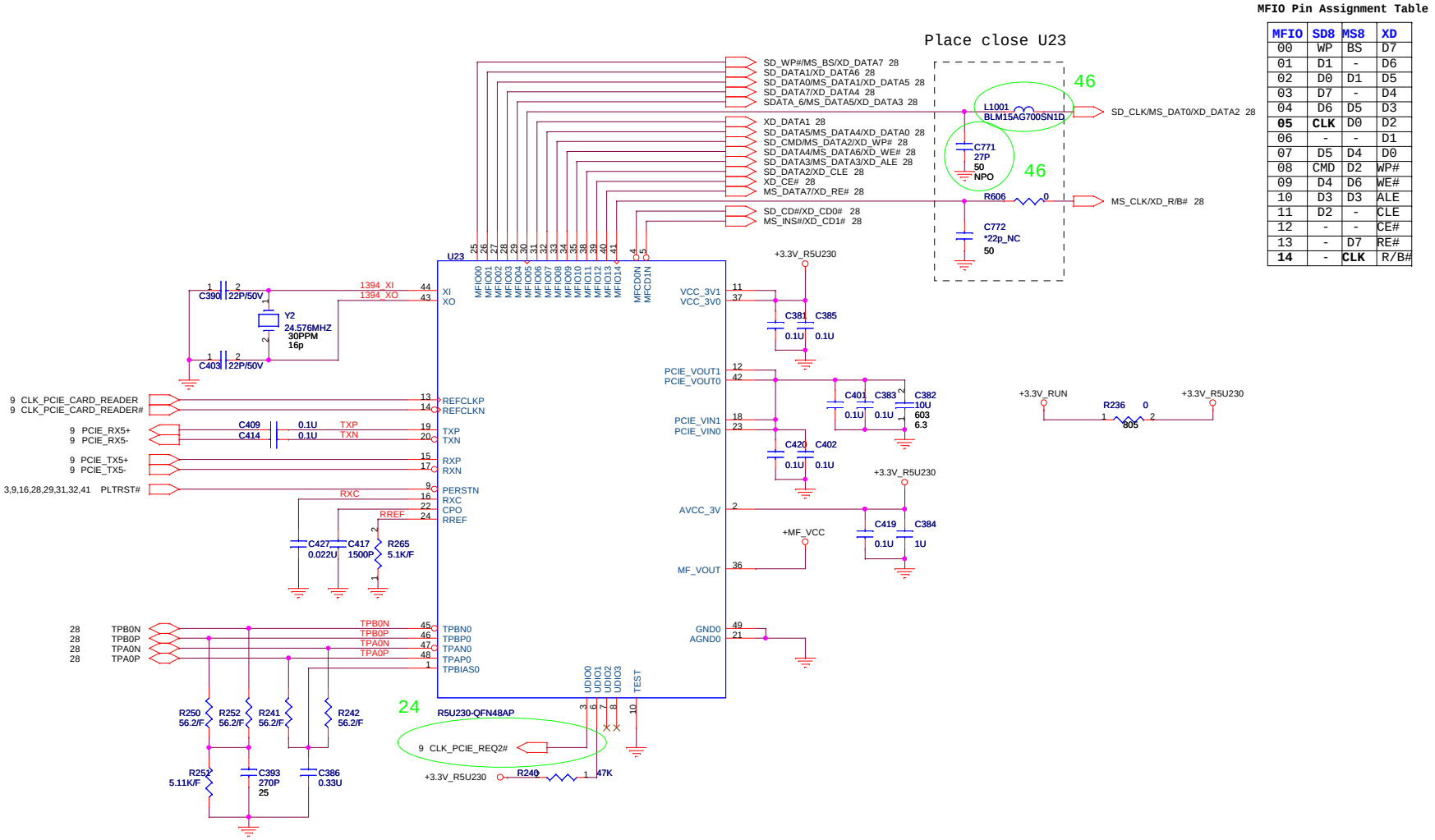

MFIO Pin Assignment Table

MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	**CLK**	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	**CLK**	R/B#

QUANTA COMPUTER

Title	5 IN 1 CONTROLLER	
Size	Document Number FM9	Rev 2B
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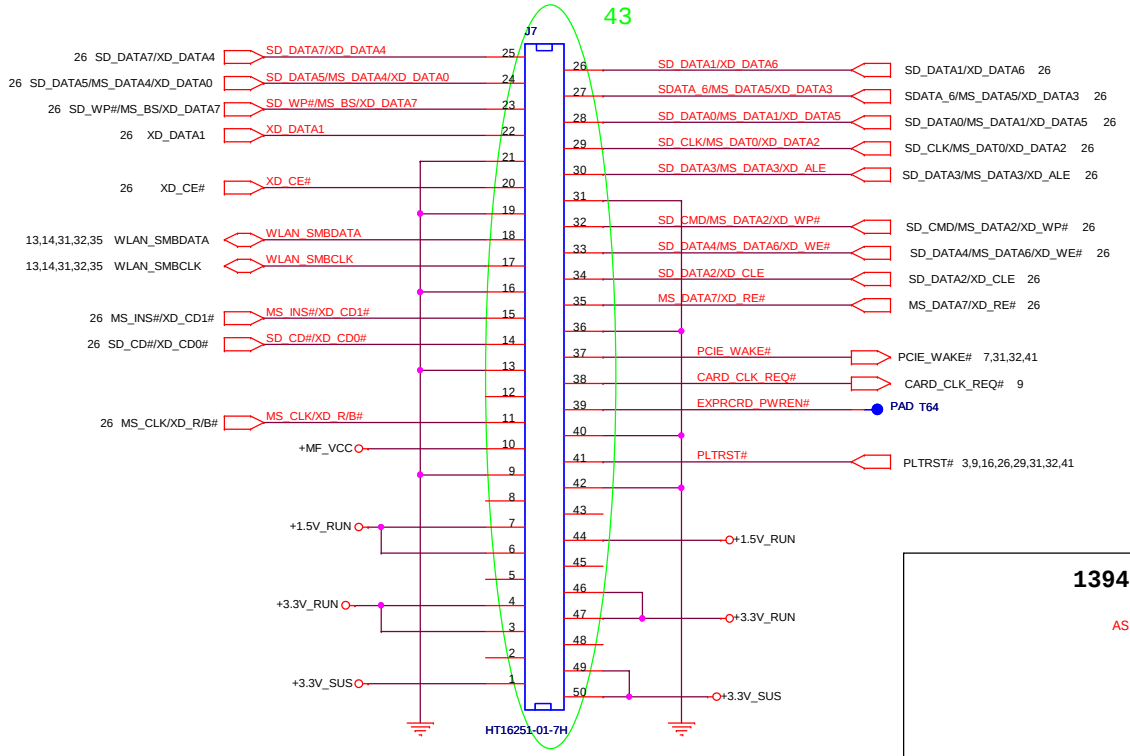
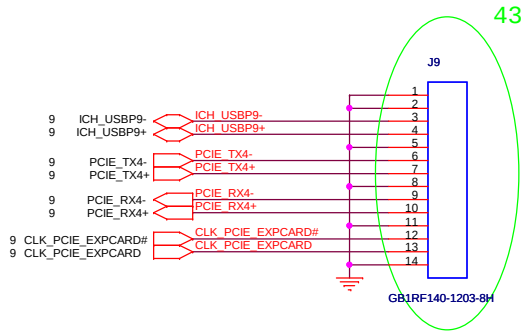
QUANTA COMPUTER

Title	IEEE 1394	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 27 of 66	

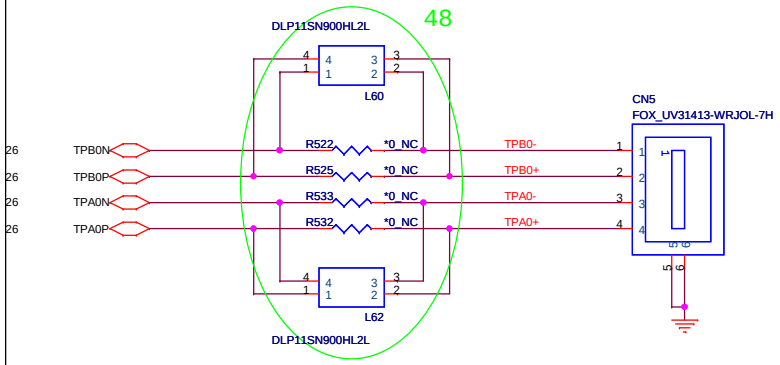
Express Card/CARD READER





1394 CONNECTOR

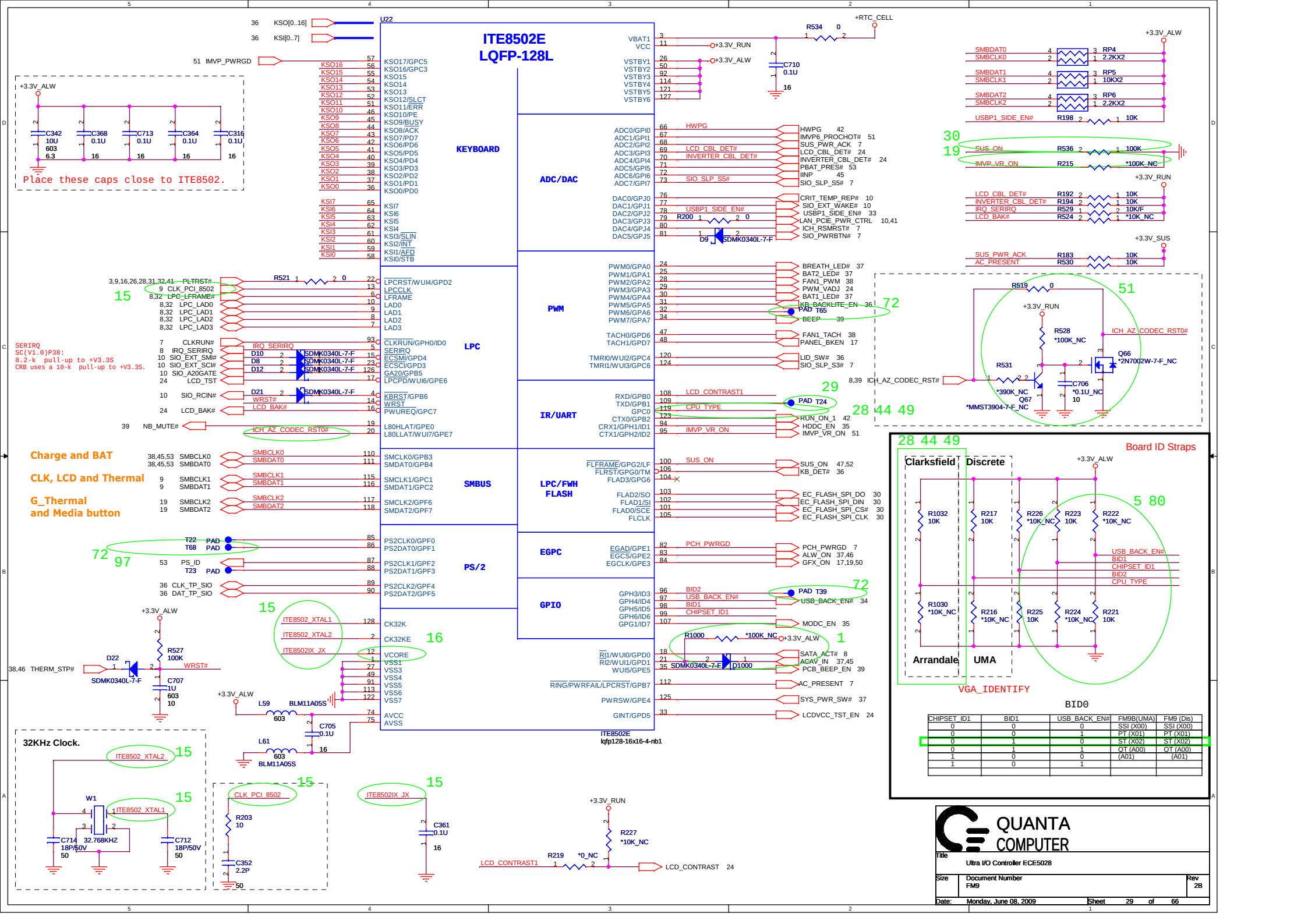
AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.



*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.

QUANTA COMPUTER

Title	ExpressCard/SmartCard	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 28 of 66	


ITE8502E
LQFP-128L
U22
KEYBOARD
ADC/DAC
PWM
LPC
IR/UART
SMBUS
LPC/FWH
FLASH
EGPC
PS/2
GPIO
Place these caps close to ITE8502.
Charge and BAT
CLK, LCD and Thermal
G_Thermal
and Media button
32KHz Clock.
Board ID Straps
Clarksfield
Discrete
Arrandale
UMA
VGA_IDENTIFY
BID0
QUANTA
COMPUTER
Ultra I/O Controller ECE5028
Document Number
FM9
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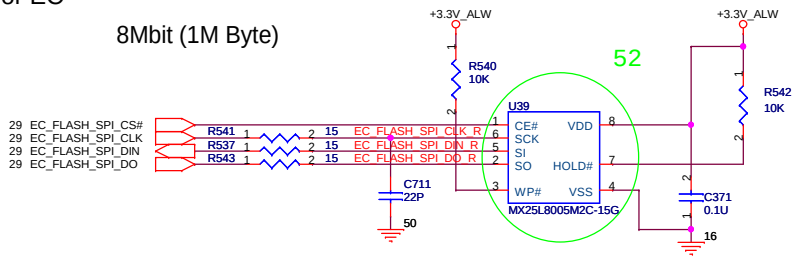
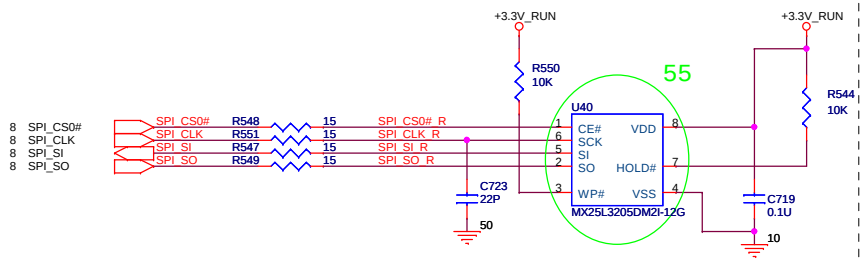
For EC

8Mbit (1M Byte)

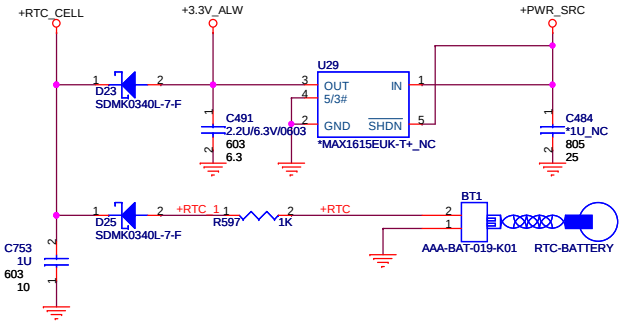


For PCH

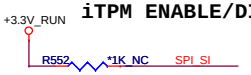
32Mbit (4M Byte)



RTC BATTERY



iTPM ENABLE/DISABLE



TPM Function	R712
Enable	Mount
Disable	NC (Default)

QUANTA COMPUTER

Title	Ultra I/O Controller ECE5028	
Size	Document Number FM9	Rev 2B
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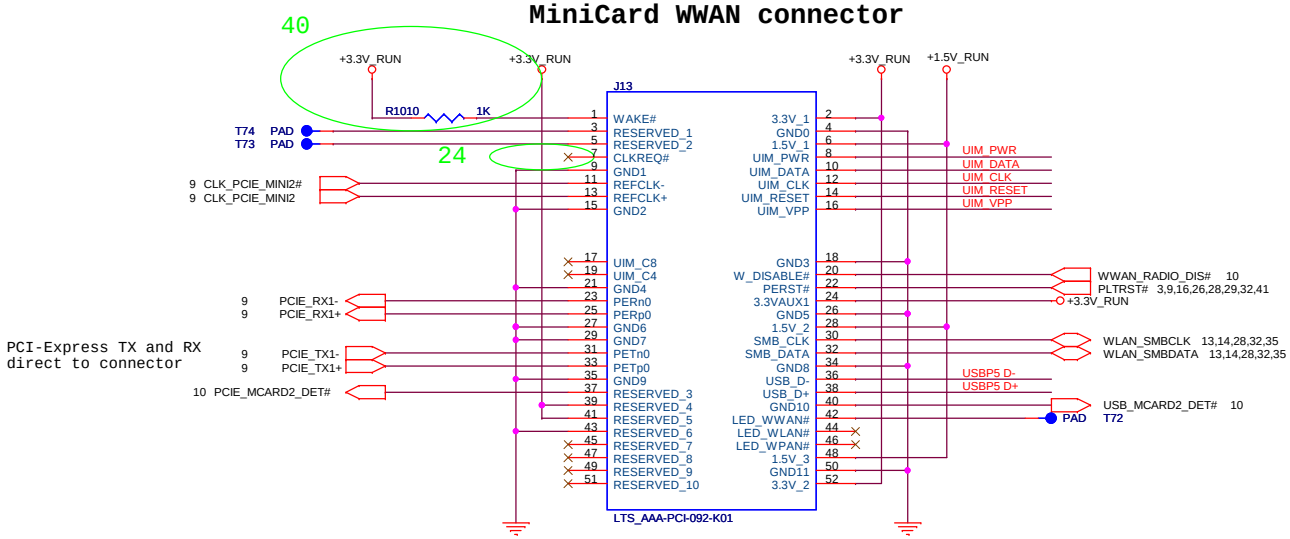
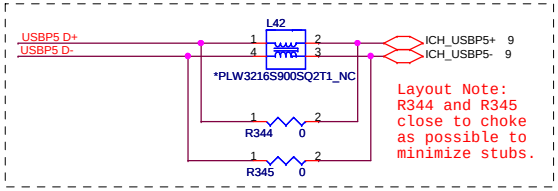
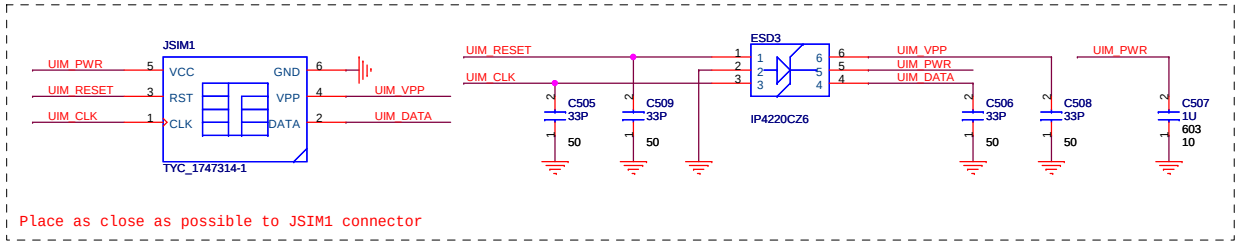
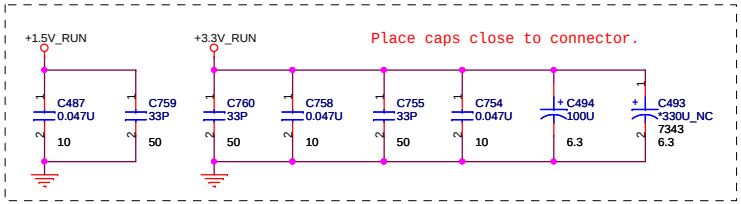
MiniCard WWAN connector



PCI-Express TX and RX
direct to connector







QUANTA COMPUTER

Title	MINI-PCI	
Size	Document Number FM9	Rev 2B
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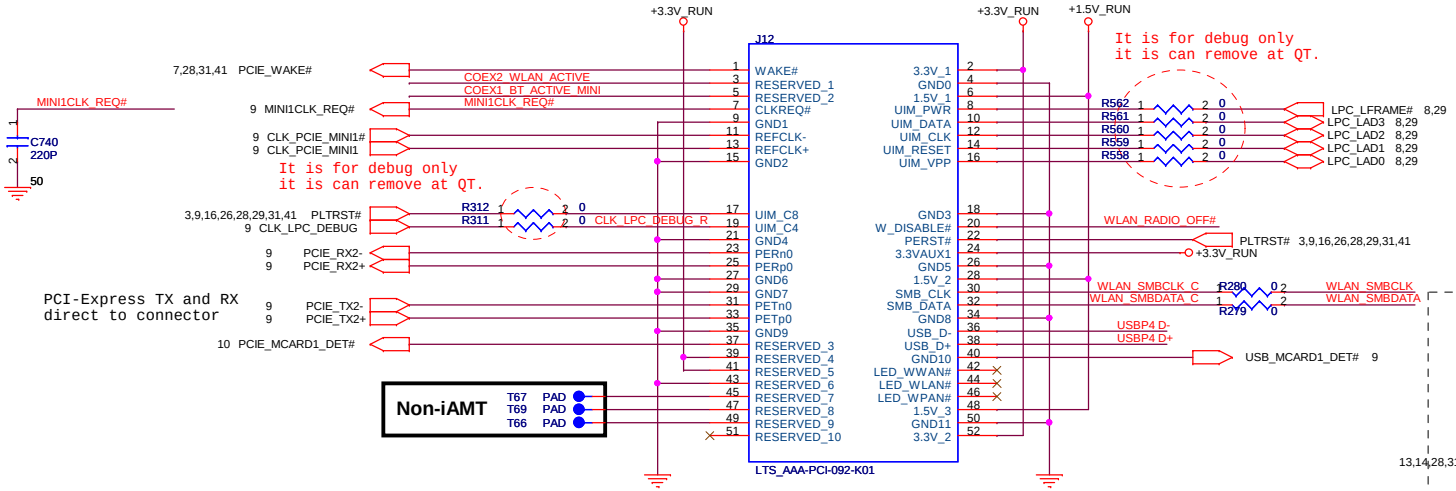
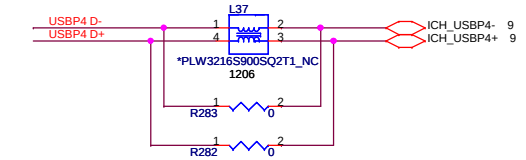
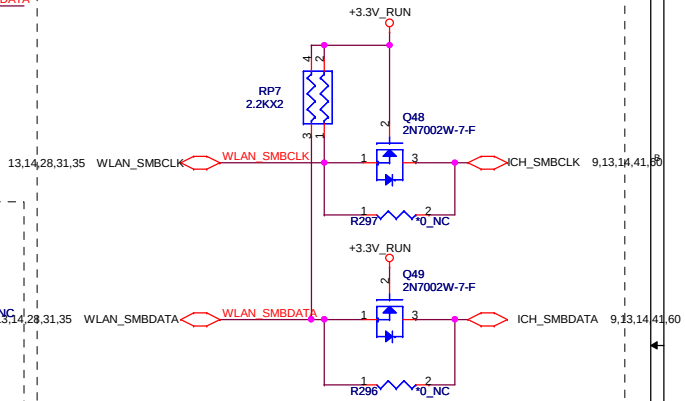
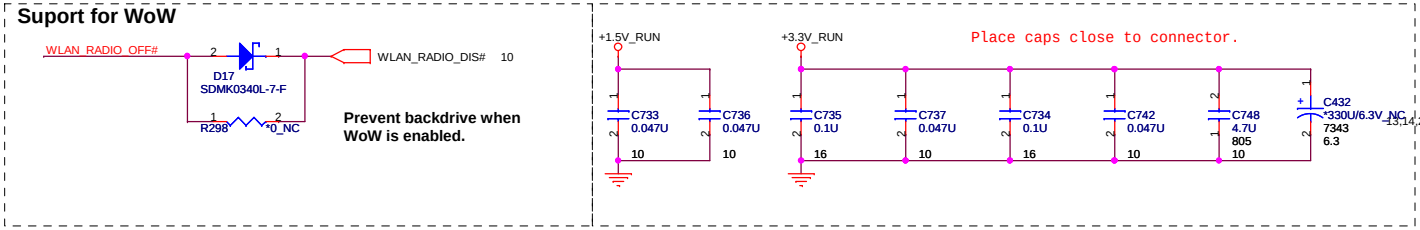
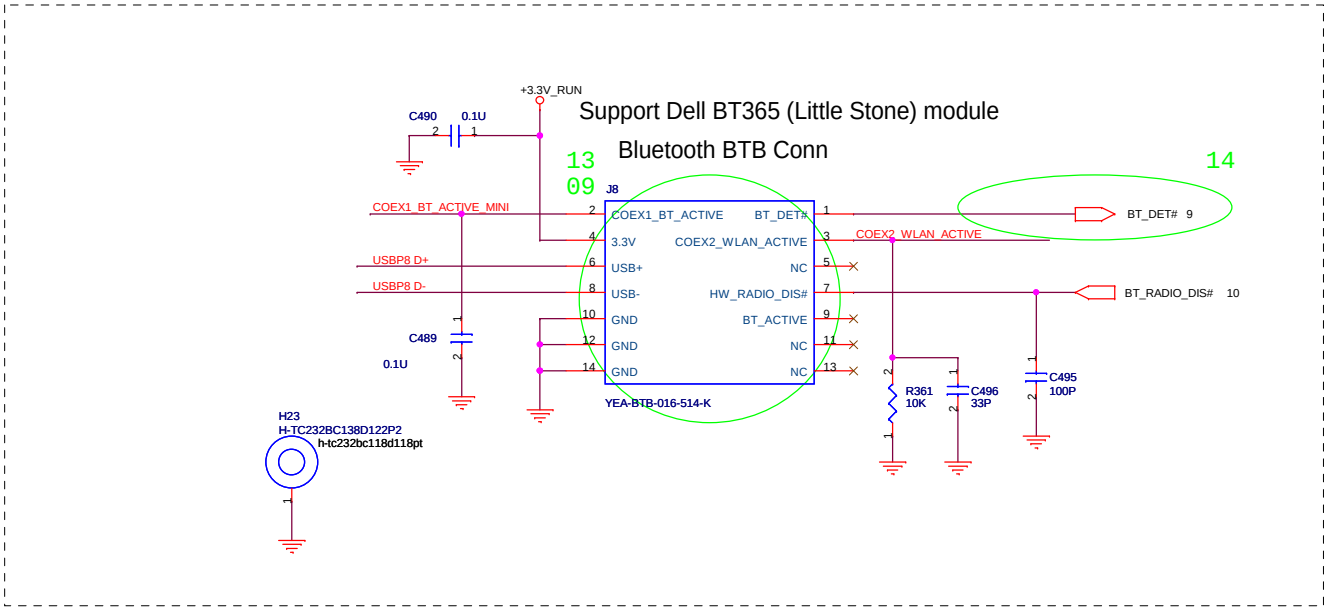
MiniCard WLAN connector

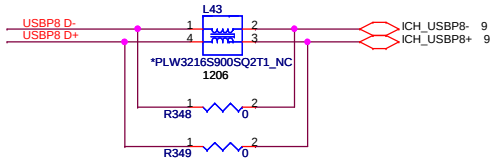












QUANTA COMPUTER

Title	MDC CONN.	
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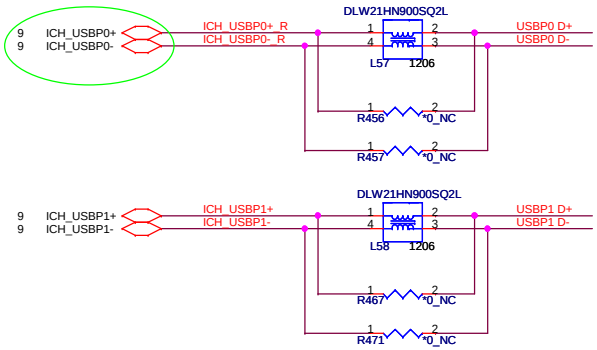
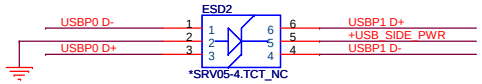
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

72



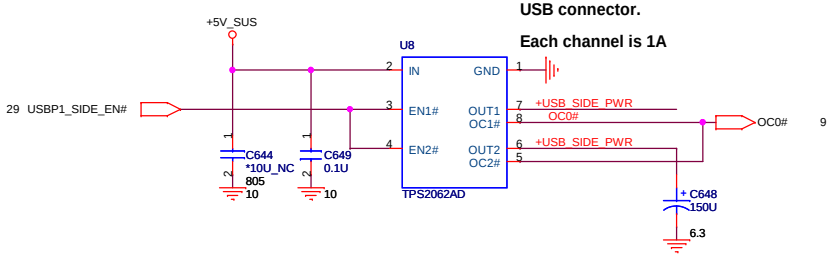
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



Place one 150uF cap by each USB connector.

Each channel is 1A



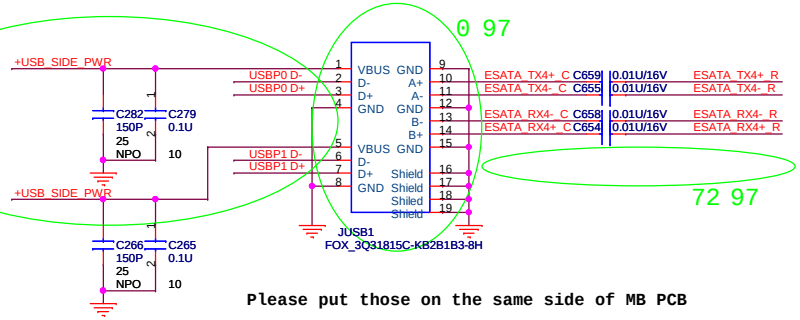
72

Side External USBX2

PN is old, Because New Part can't ready before SST build.

72 98

0 97



72 97

Please put those on the same side of MB PCB

USBx2 & ESATA COMBO

USB BUS SW

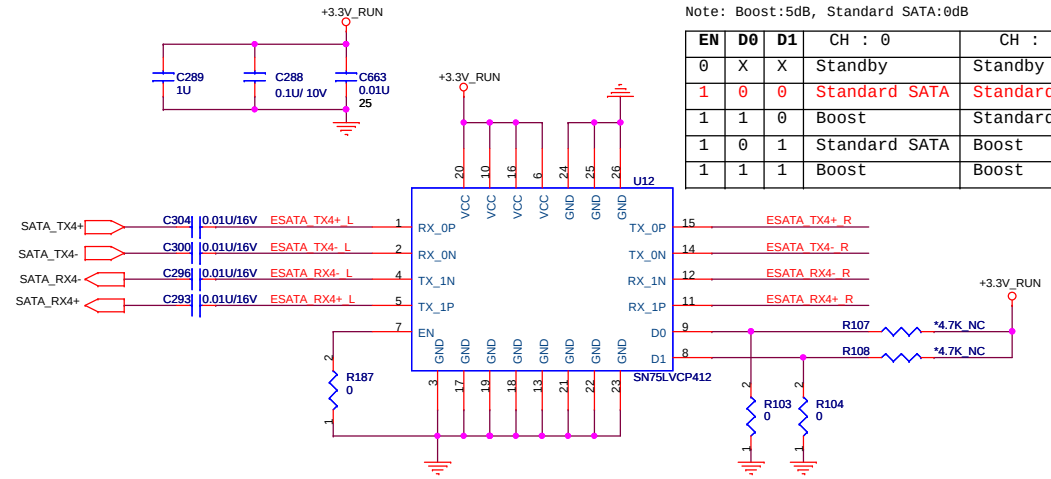
72

E-SATA Re-driver

Please put those on the same side of MB PCB

Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost



72 97

Title	SERIAL PORT & USB
Size	Document Number FM9
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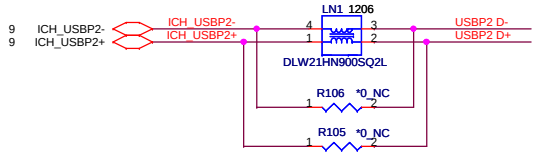
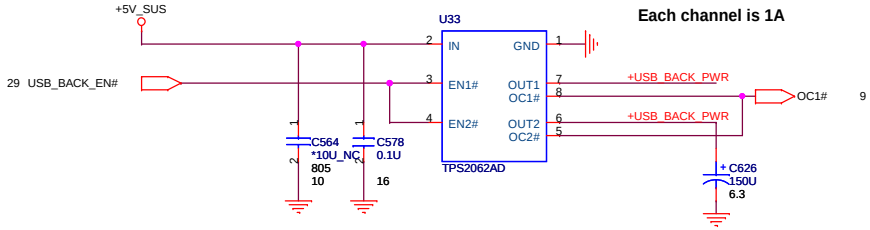
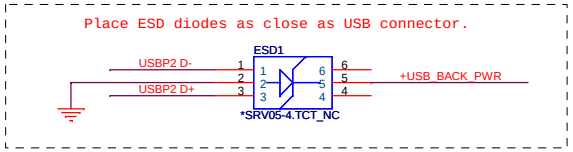
QUANTA COMPUTER

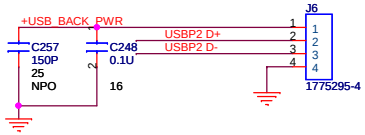


Place one 150uF cap by each USB connector.

Each channel is 1A







QUANTA COMPUTER

Title	Right USB	
Size	Document Number FM9	Rev 2B
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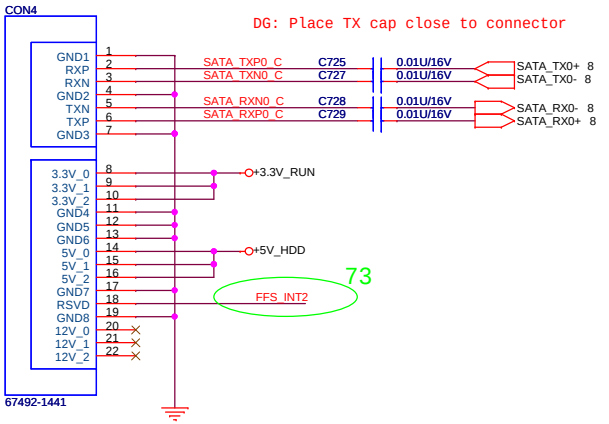
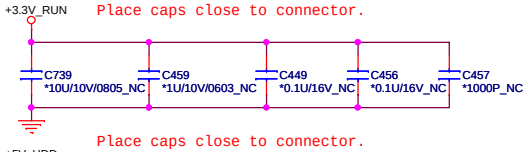
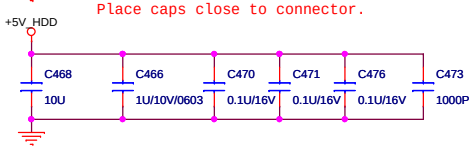
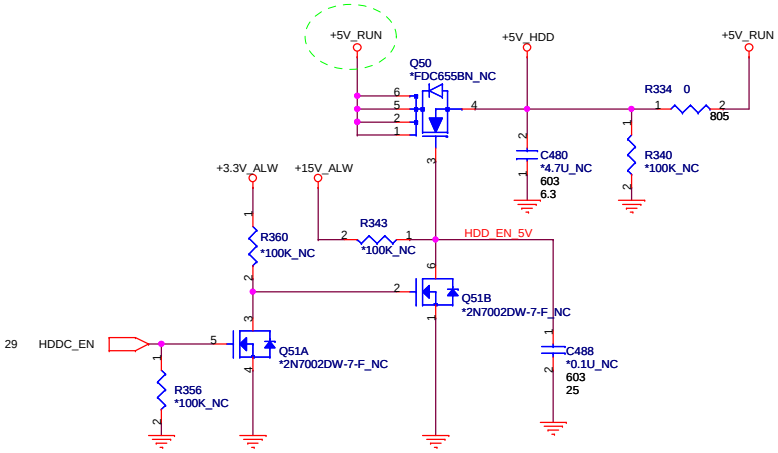
SATA Connector.

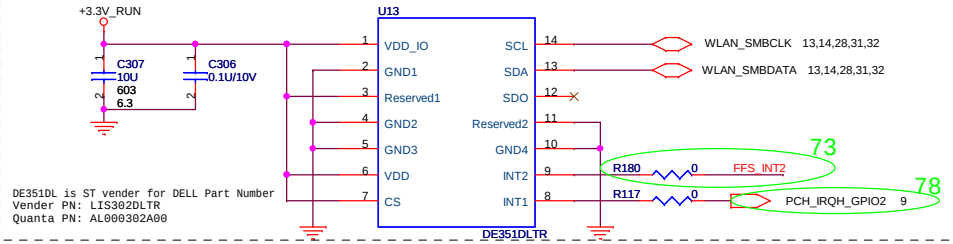




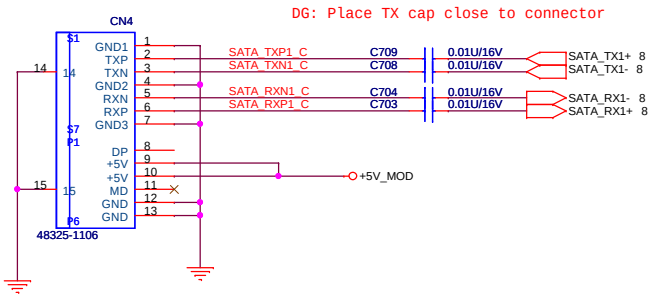


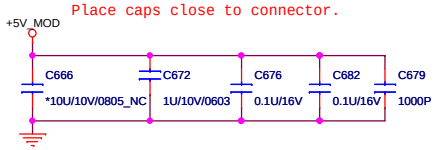


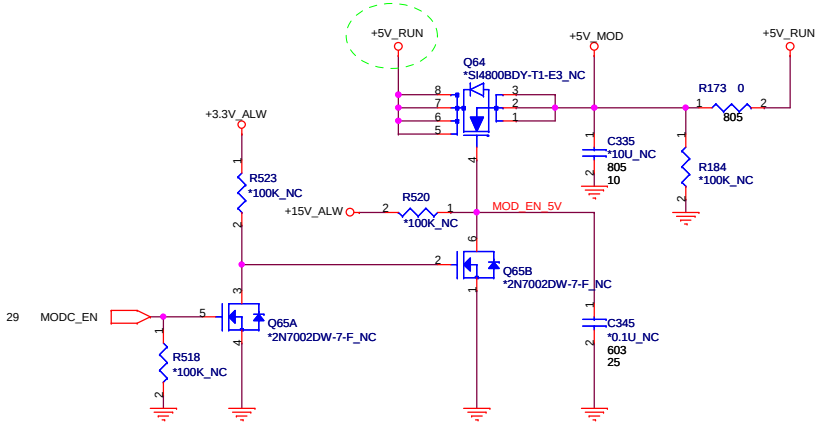
3-axis Fall Sensor (HDD data protector)



ODD Connector

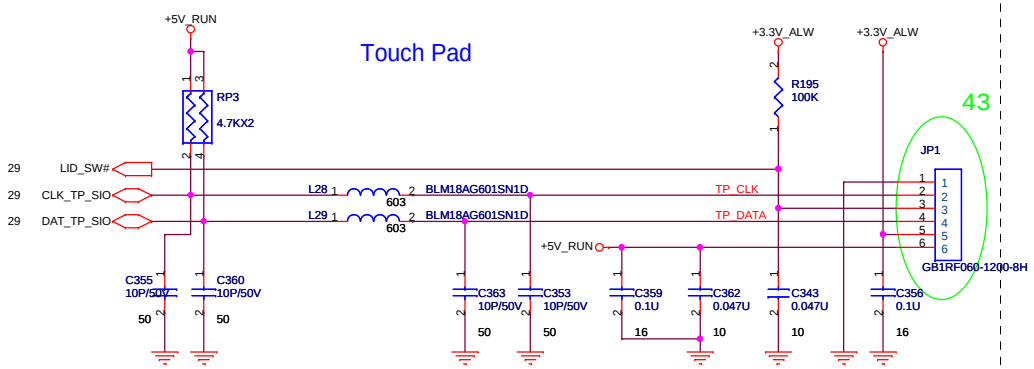




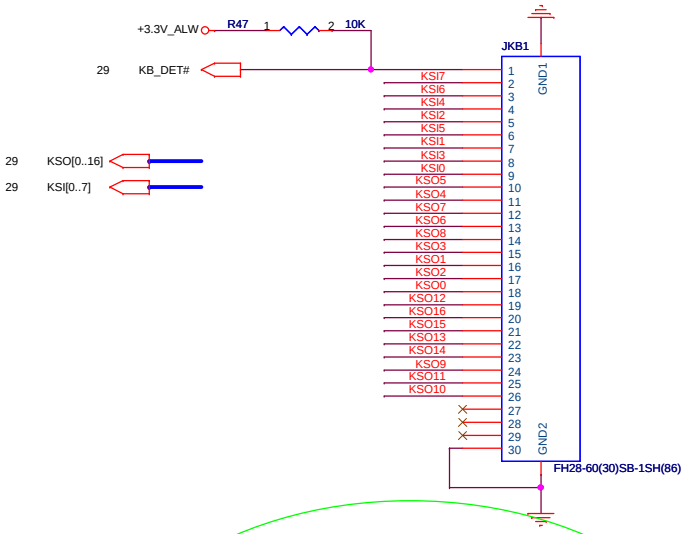


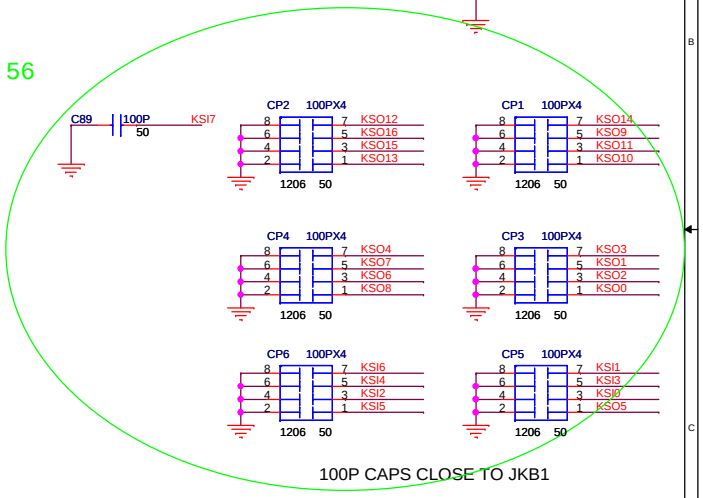
QUANTA COMPUTER		
Title: SATA (HDD&CD_ROM)		
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 35 of 66	

Touch Pad



KEYBOARD CONNECTOR

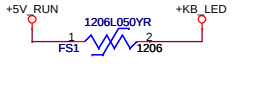


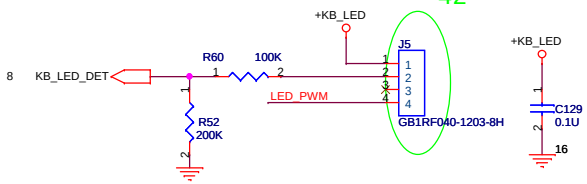


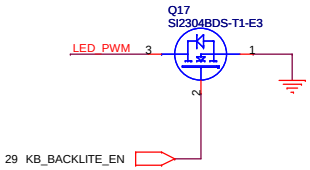
100P CAPS CLOSE TO JKB1

Key board illumination

+KB_LED power trace width >10 mil







QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 36 of 66	

Touch Screen Module

Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
2. Maximum cable resistance on VCC, GND should be 150m ohm.
3. FPC cable should support 12MHz USB singles.
A tri-state should indicate no connection.

25
39
47
33

+5V_RUN — R1024 0 — USBP12 D- / USBP12 D+ — J2 — HS6104F

9 ICH_USBP12+
9 ICH_USBP12-
L1 — *PLW3216S900SQ2T1_NC
USBP12 D+
USBP12 D-
R5 1206 0
R3 0

Power button Cable

BREATH_PWRLED
POWER_SW_IN0#
J4 — 1775295-4

3VALW ON POWER LOGIC

72 97

+3.3V_ALW
R233 100K
D13 — BAS316
SYS_PWR_SW# 29
C372 0.1U 16
POWER_SW_IN0#
D14 — BAS316
C380 *0.1U_NC 10
+5V_ALW2
R237 100K
R239 100K
3.3V_ALW_ON 46
Q43 2N7002W-7-F
29,46 ALW_ON
Q44 2N7002W-7-F
29,45 ACAV_IN
Q42 2N7002W-7-F

Battery status.

4
12
17

+3.3V_ALW — R29 100K
+3.3V_ALW
+5V_ALW2
29 BAT1_LED#
Q7 2N7002W-7-F
47K
10K
Q8 DDTA114YUA-7-F
BAT1_LED
R23 220
RBAT1_LED 53

+3.3V_ALW
29 BAT2_LED#
47K
10K
Q11 DDTA114YUA-7-F
BAT2_LED
R37 68
RBAT2_LED 53

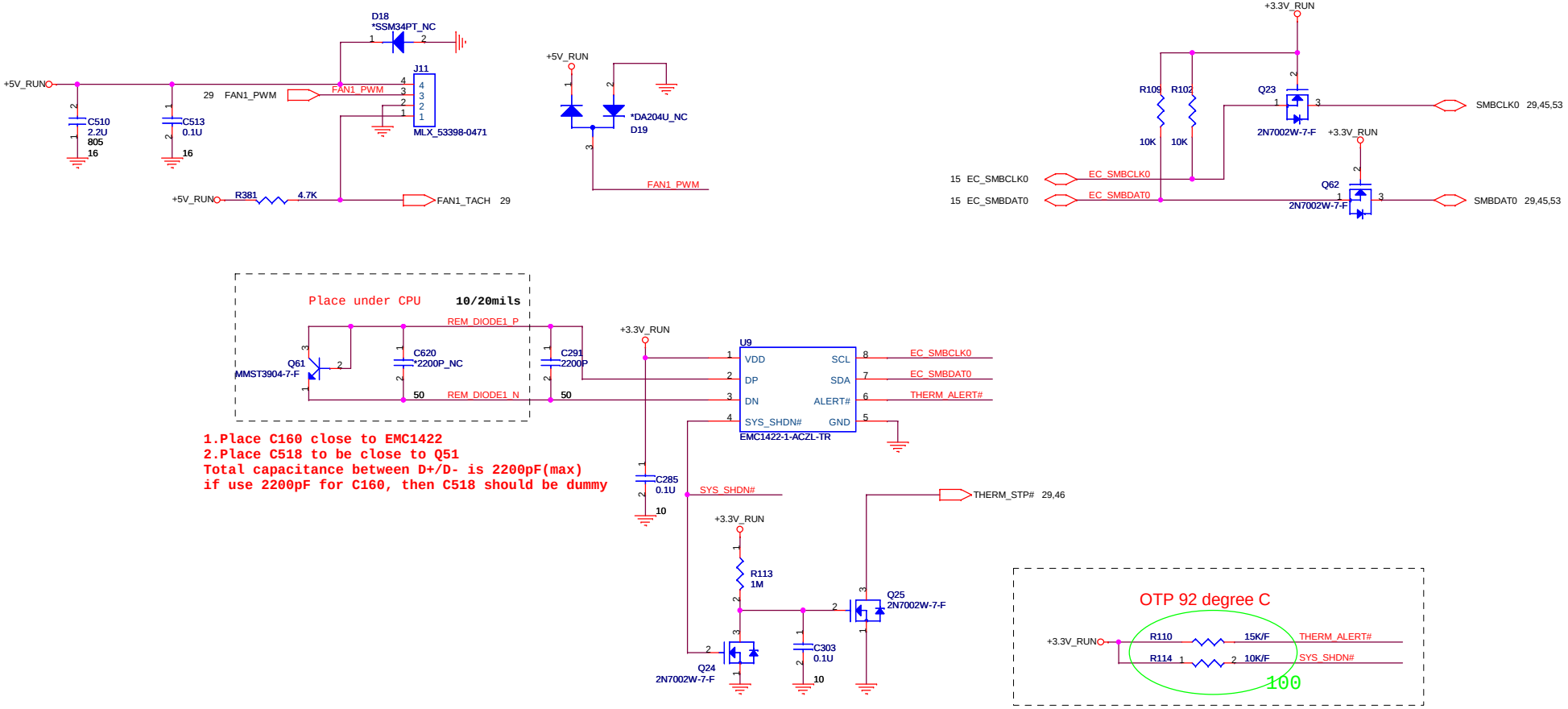
+3.3V_SUS — R33 100K
+5V_SUS
+5V_SUS
29 BREATH_LED#
Q14 2N7002W-7-F
U3 TC7SZ04FU(T5L,F,T)
BR_LED
R31 100
BREATH_PWRLED

+3.3V_ALW
*DA204U_NC
D3
POWER_SW_IN0#

BREATH_LED# C69 *100P_NC 50
POWER_SW_IN0# C35 *100P_NC 50

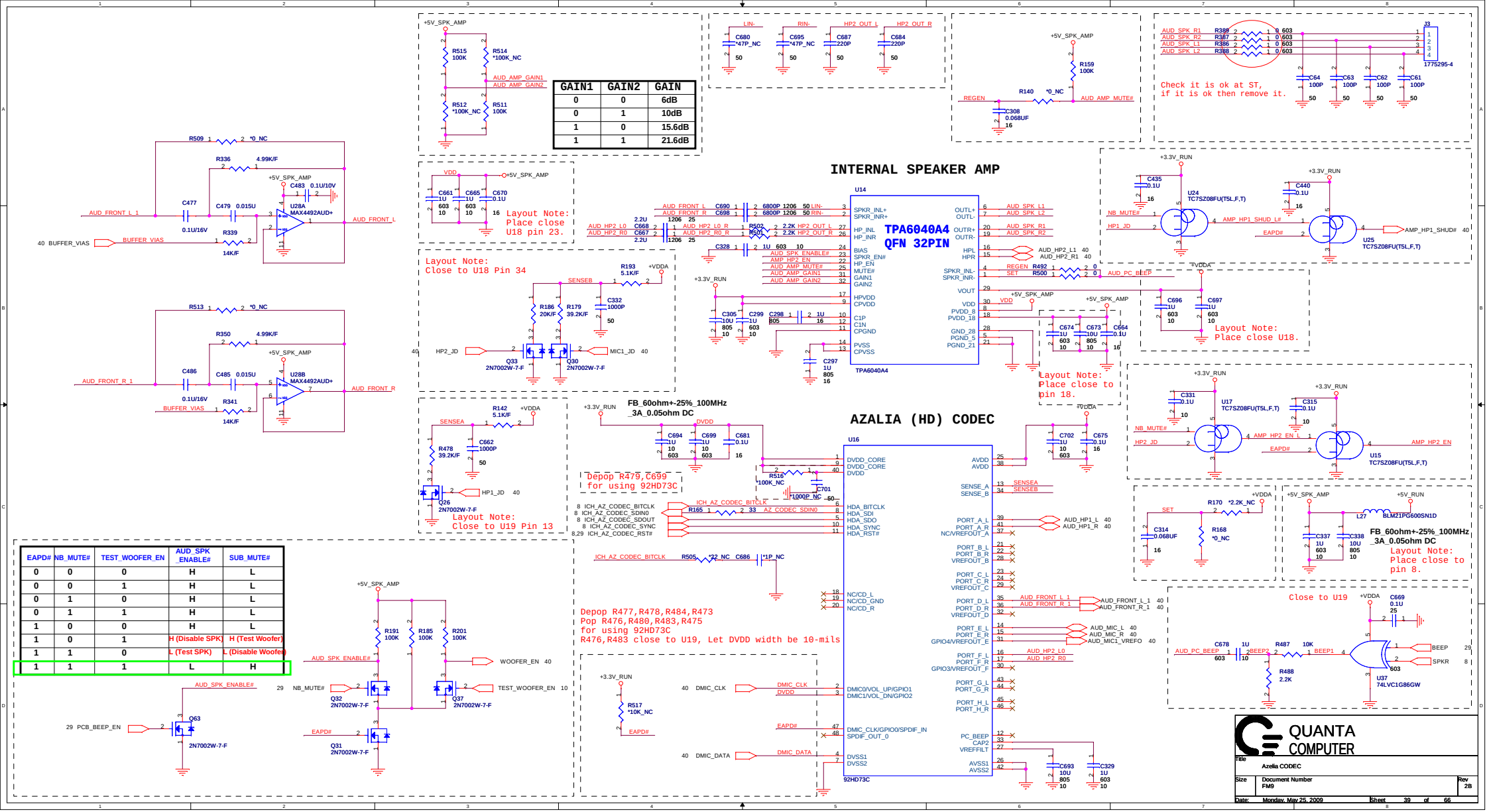
QUANTA COMPUTER

Title	SWITCH, KEYBOARD & LED&Touch Screen Module	
Size	Document Number FM9	Rev 2B
Date: Tuesday, June 02, 2009	Sheet 37 of 66	



QUANTA COMPUTER

Title	FAN & THERMAL	
Size	Document Number FM9	Rev 2B
Date: Monday, June 08, 2009	Sheet 38 of 66	


INTERNAL SPEAKER AMP
TPA6040A4
QFN 32PIN
AZALIA (HD) CODEC
92HD73C
GAIN1 GAIN2 GAIN
0 0 6dB
0 1 10dB
1 0 15.6dB
1 1 21.6dB
EAPD# NB_MUTE# TEST_WOOFER_EN SUB_MUTE#
0 0 0 H L
0 0 1 H L
0 1 0 H L
0 1 1 H L
1 0 0 H L
1 0 1 H (Disable SPK) H (Test Woofer)
1 1 0 L (Test SPK) L (Disable Woofer)
1 1 1 L H
Layout Note: Close to U18 Pin 34
Layout Note: Place close U18 pin 23.
Layout Note: Close to U19 Pin 13
Layout Note: Place close to pin 18.
Layout Note: Place close to pin 8.
Layout Note: Place close U18.
Depop R479,C699 for using 92HD73C
Depop R477,R478,R484,R473 Pop R476,R480,R483,R475 for using 92HD73C
R476,R483 close to U19, Let DVDD width be 10-mils
Check it is ok at ST, if it is ok then remove it.
FB_60ohm+-25%_100MHz _3A_0.05ohm DC
QUANTA COMPUTER
Azelia CODEC
Document Number FM9
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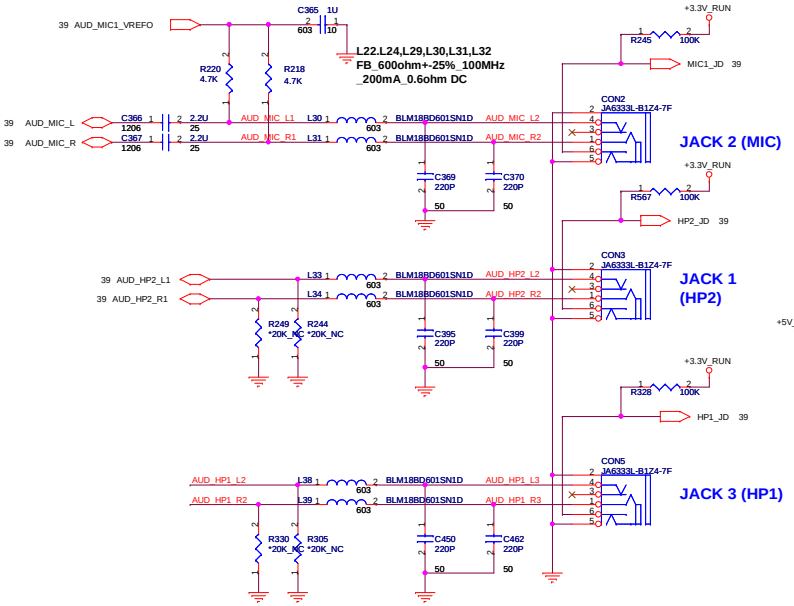
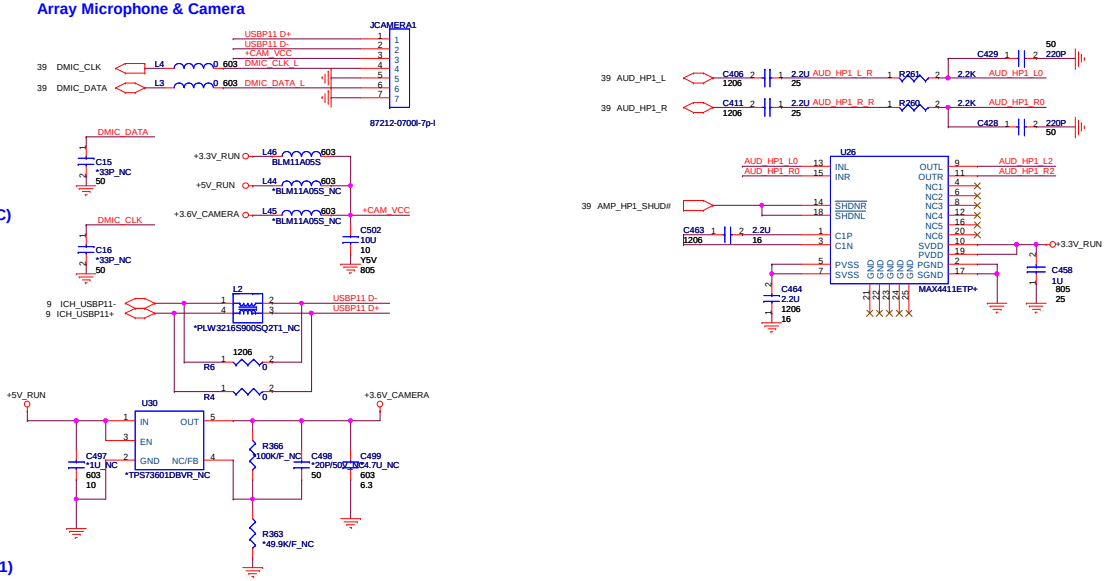
Headphone Jack
Stereo MIC Jack



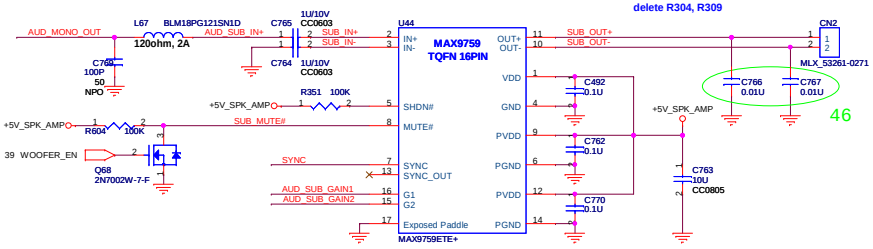
Array Microphone & Camera

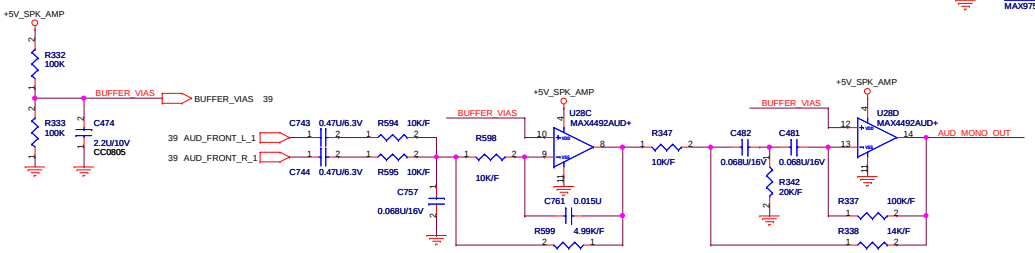


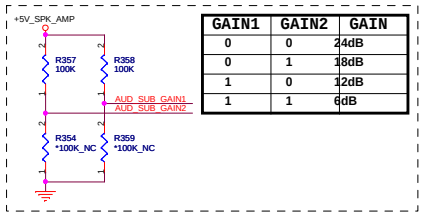
INTERNAL SUBWOOFER AMP

SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.

Gur_0808: 0 ohm removal,
delete R304, R309



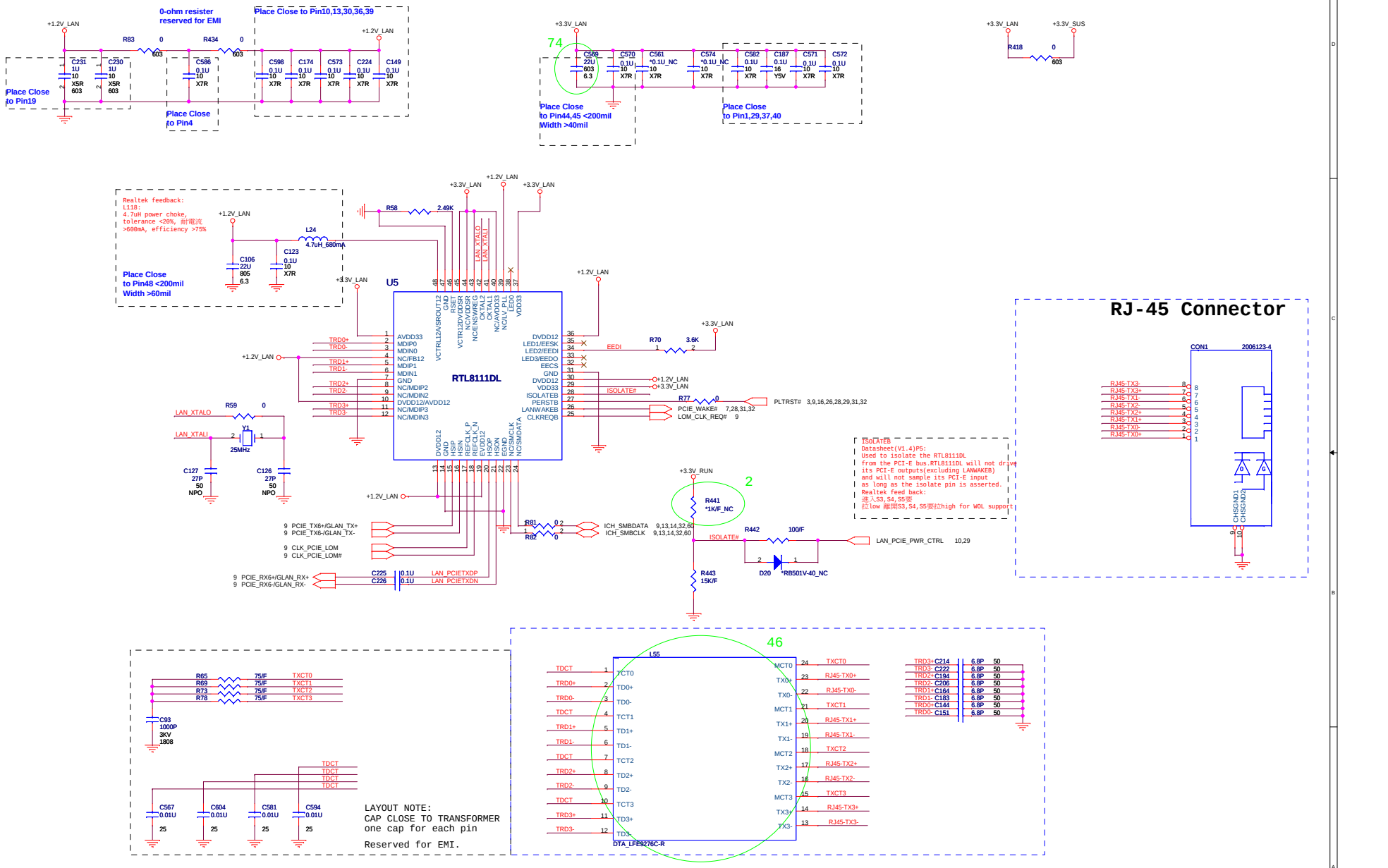


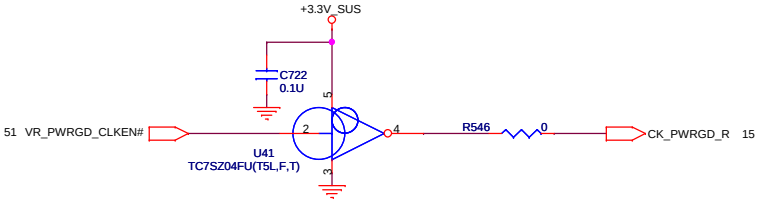


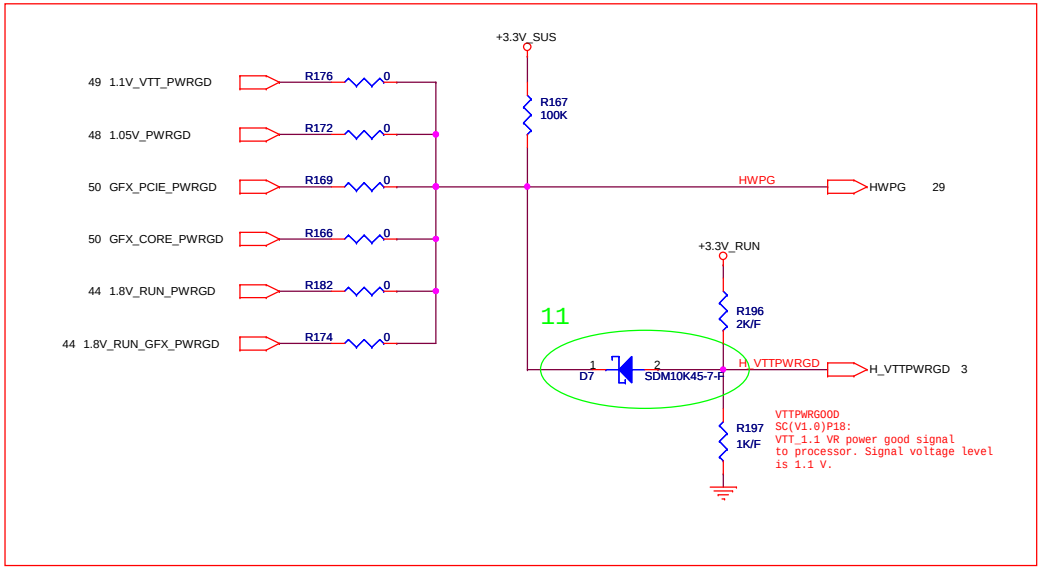
GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB

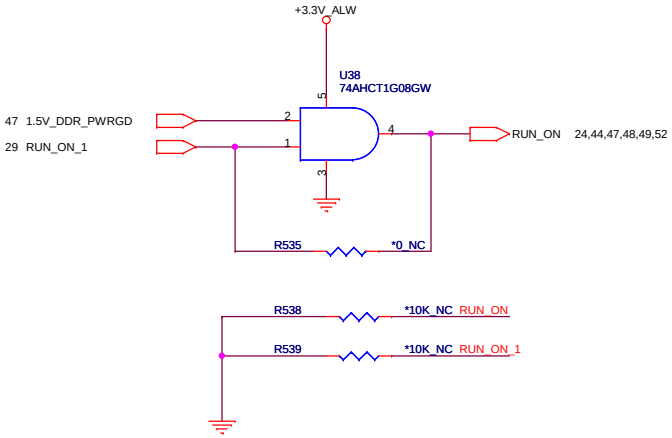
QUANTA COMPUTER

Title	AUDIO CONN	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 40 of 66	


0-ohm resister reserved for EMI
Place Close to Pin10,13,30,36,39
Place Close to Pin19
Place Close to Pin4
Place Close to Pin44,45 <200mil Width >40mil
Place Close to Pin1,29,37,40
Realtek feedback: L118: 4.7uH power choke, tolerance <20%, 耐電流 >600mA, efficiency >75%
Place Close to Pin48 <200mil Width >60mil
RTL8111DL
U5
RJ-45 Connector
ISOLATEB Datasheet(V1.4)P5: Used to isolate the RTL8111DL from the PCI-E bus.RTL8111DL will not drive its PCI-E outputs(excluding LANWAKEB) and will not sample its PCI-E input as long as the isolate pin is asserted. Realtek feed back: 進入S3,S4,S5要 拉low 離開S3,S4,S5要拉high for WOL support
LAYOUT NOTE: CAP CLOSE TO TRANSFORMER one cap for each pin
Reserved for EMI.
DTA_LFE9276C-R
QUANTA COMPUTER
Title LAN
Size Document Number FM9 Rev 2B
Date: Monday, May 25, 2009 Sheet 41 of 66





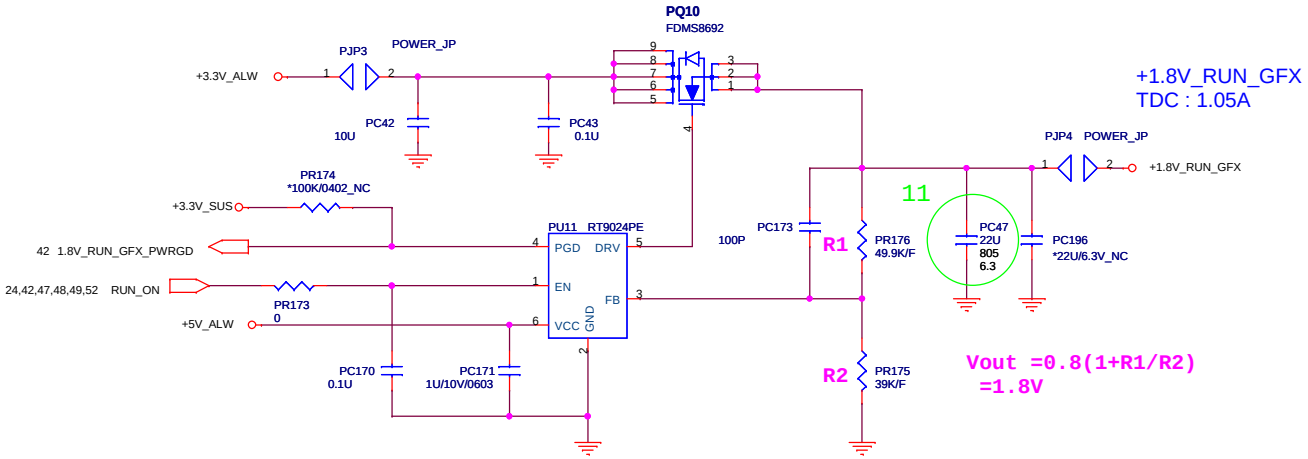


QUANTA COMPUTER

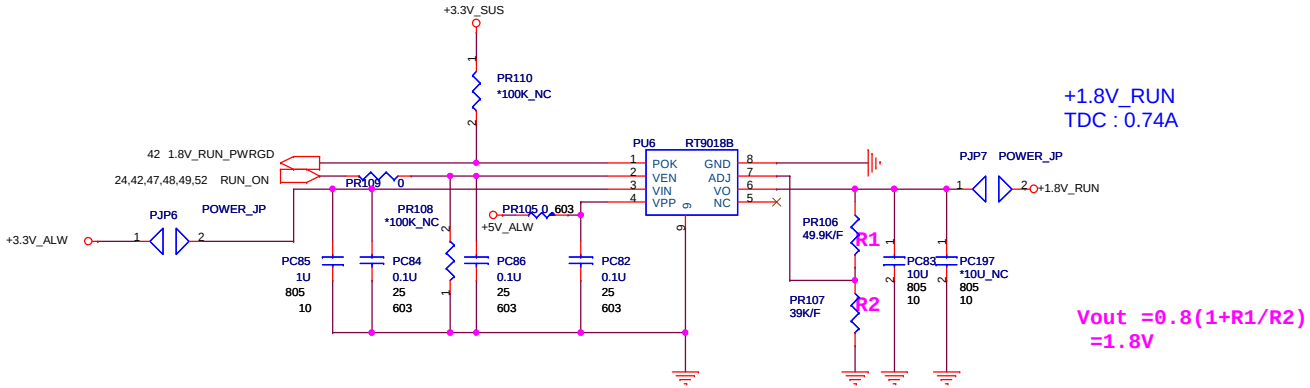
Title	System Reset Circuit	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 42 of 66	

QUANTA COMPUTER

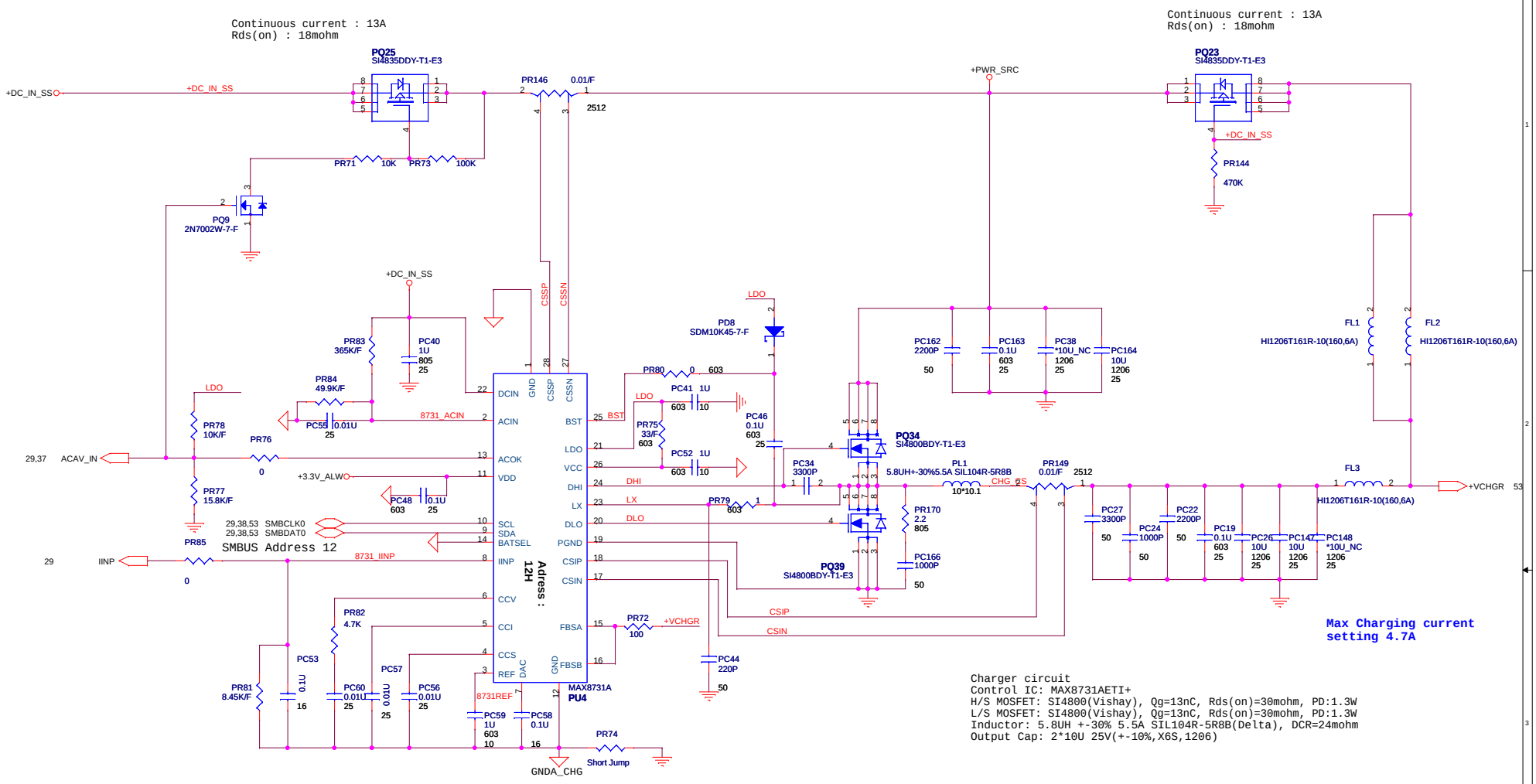
Title	Battery Selector	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 43 of 66	



+1.8V_RUN_GFX for VGA 1.8V
+1.8V_RUN for CPU and PCH 1.8V



Title	+1.8V_RUN_GFX (RT9024PE) & +1.8V_RUN(RT9018B)	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 44 of 66	



QUANTA COMPUTER

Title	Charger (MAX8731)	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 45 of 66	

+3.3V_ALW
Control IC: TPS51427A
H/S MOSFET: FDS6298(Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
L/S MOSFET: FDS6676AS(Fairchild), Qg=35nC, Rds(on)=7.25mohm, PD:2.5W
Inductor: 1.5U20%17.1A(FDVE1040-H-1R5M=P3)(TOKO), DCR=4.6mohm
Output Cap: 1*150U 6.3V(20%,ESR15,7343,H=1.9),ripple current 2700mA

+5V_ALW
Fs=400K
TDC : 5.83A
Peak current : 8.33A
OCP:10A

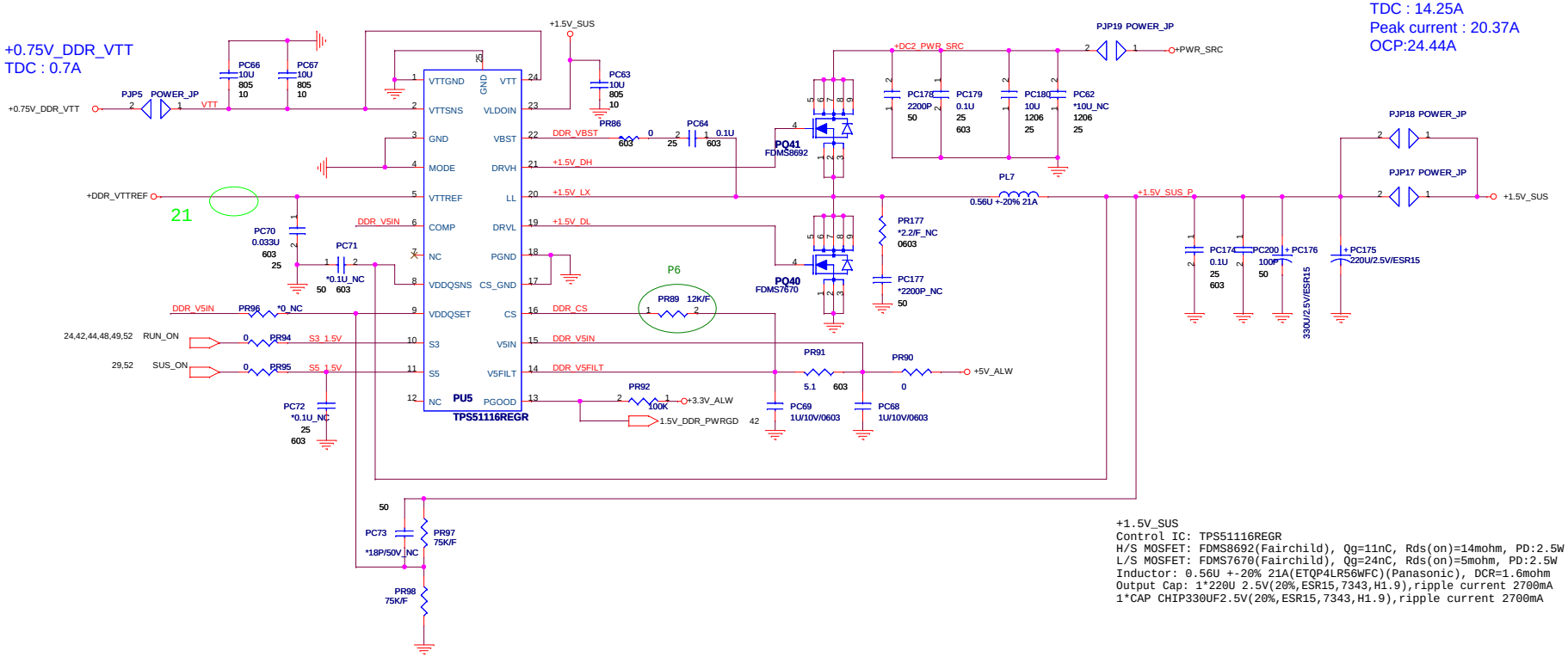
+3.3V_ALW
Fs=300K
TDC : 8.23A
Peak : 11.77A
OCP:14A

+5V_ALW
Control IC: TPS51427A
H/S MOSFET: FDS8884(Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS(Fairchild), Qg=13nC, Rds(on)=15mohm, PD:2.5W
Inductor: 3.3UH +-20% 12.3A FDVE1040-H-3R3M=P3(TOKO), DCR=10.1mohm
Output Cap: 1*150U 6.3V(20%,ESR15,7343,H=1.9),ripple current 2700mA

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz

QUANTA COMPUTER

Title	3.3V_ALW / 5V_ALW(TPS51427A)	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 46 of 65	



VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	2.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Title	DDR3 +1.5V_SUS(TPS51116)
Size	Document Number FM9
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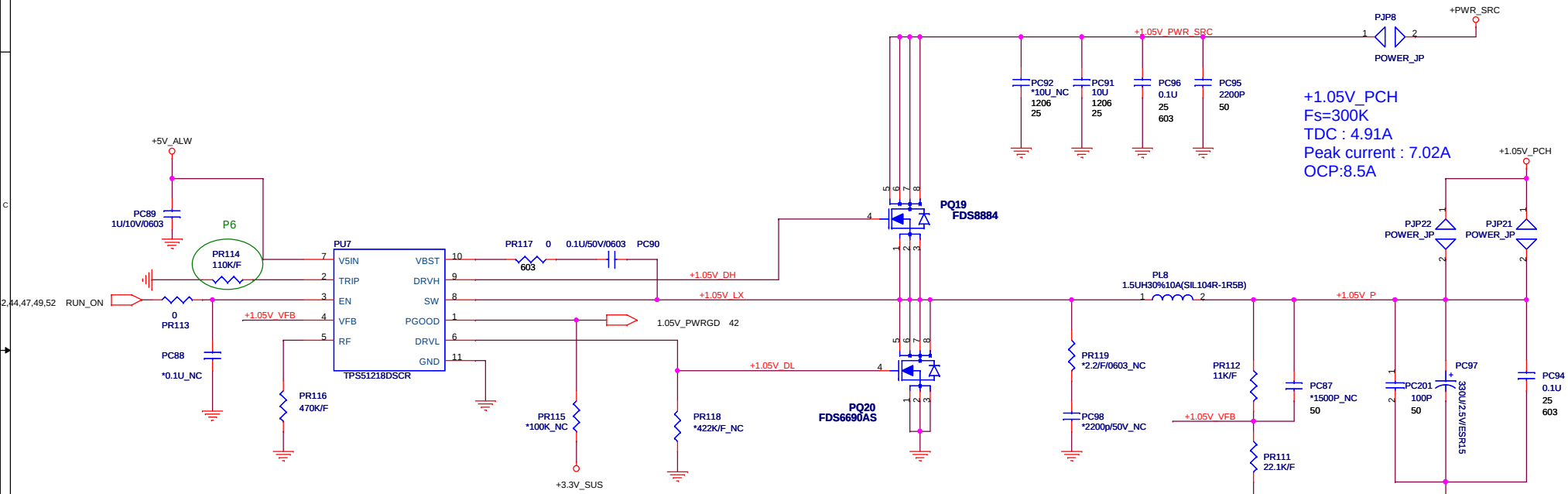
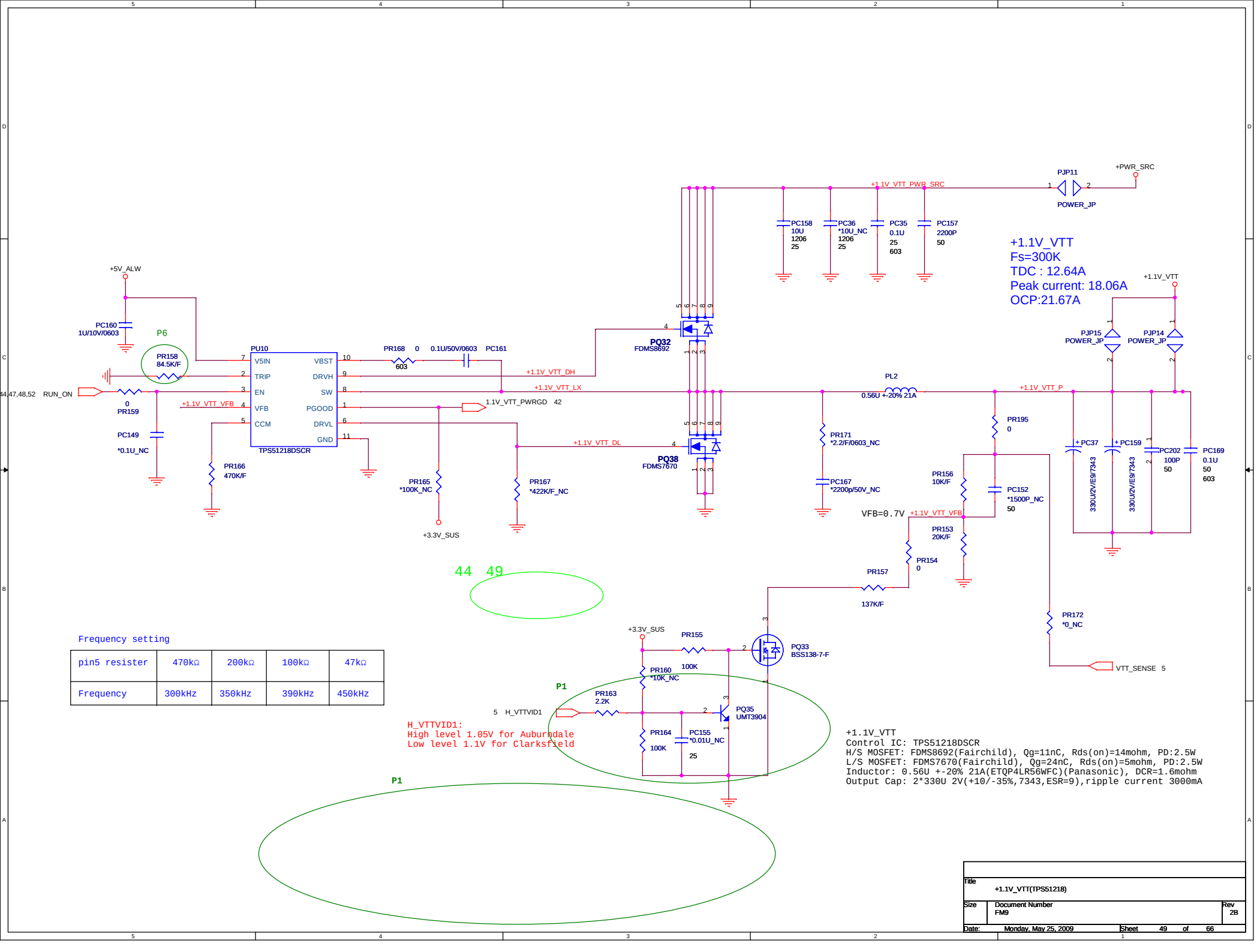


Frequency setting

pin5 resister	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

+1.05V_PCH
Control IC: TPS51218DSCR
H/S MOSFET: FDS8884(Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS(Fairchild), Qg=13nC, Rds(on)=15mohm, PD:2.5W
Inductor: 1.5UH +-30% 10A SIL104R-1R5B(Delta), DCR=8.1mohm
Output Cap: 1*330U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

Title	+1.05V_PCH(TPS51218)	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 48 of 66	


+1.1V_VTT
Fs=300K
TDC : 12.64A
Peak current: 18.06A
OCP:21.67A
+5V_ALV
+PWR_SRC
+1.1V_VTT_PWR_SRC
PJP11
POWER_JP
PC158 10U 1206 25
PC36 *10U_NC 1206 25
PC35 0.1U 25 603
PC157 2200P 50
PC160 1U/10V/0603
P6
PR158 84.5K/F
PU10
V5IN
TRIP
EN
VFB
CCM
VBST
DRVH
SW
PGOOD
DRVL
GND
TPS51218DSCR
PR168 0 603
0.1U/50V/0603 PC161
+1.1V_VTT_DH
+1.1V_VTT_LX
PQ32 FDMS8692
PQ38 FDMS7670
PL2 0.56U +-20% 21A
+1.1V_VTT_P
PJP15 POWER_JP
PJP14 POWER_JP
44,47,48,52 RUN_ON
0 PR159
+1.1V_VFB
1.1V_VTT_PWRGD 42
PC149 *0.1U_NC
PR166 470K/F
PR165 *100K_NC
PR167 *422K/F_NC
+3.3V_SUS
+1.1V_VTT_DL
PR171 *2.2/F/0603_NC
PC167 *2200p/50V_NC
PR195 0
PR156 10K/F
PC152 *1500P_NC 50
PC37
PC159
PC202 100P 50
PC169 0.1U 50 603
330U/2V/E9/7343
VFB=0.7V
PR153 20K/F
PR154 0
PR157 137K/F
PR172 *0_NC
VTT_SENSE 5
44 49
Frequency setting
pin5 resister | 470kΩ | 200kΩ | 100kΩ | 47kΩ
Frequency | 300kHz | 350kHz | 390kHz | 450kHz
+3.3V_SUS
PR155 100K
PR160 *10K_NC
PQ33 BSS138-7-F
P1
PR163 2.2K
5 H_VTTVID1
PQ35 UMT3904
PR164 100K
PC155 *0.01U_NC 25
H_VTTVID1:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield
P1
+1.1V_VTT
Control IC: TPS51218DSCR
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.56U +-20% 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
Output Cap: 2*330U 2V(+10/-35%,7343,ESR=9),ripple current 3000mA
Title
+1.1V_VTT(TPS51218)
Size
Document Number
FM9
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2B
Date: Monday, May 25, 2009
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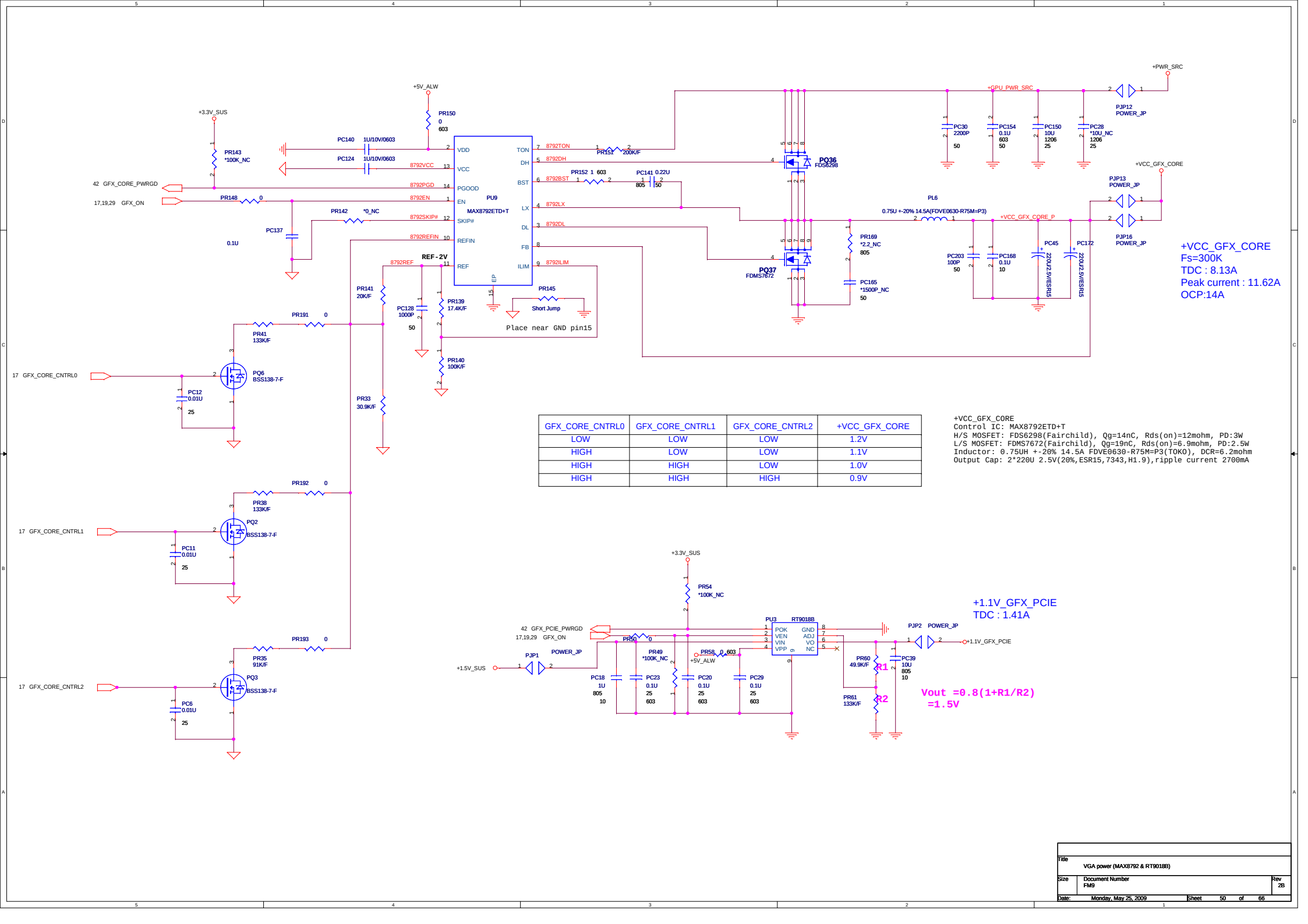
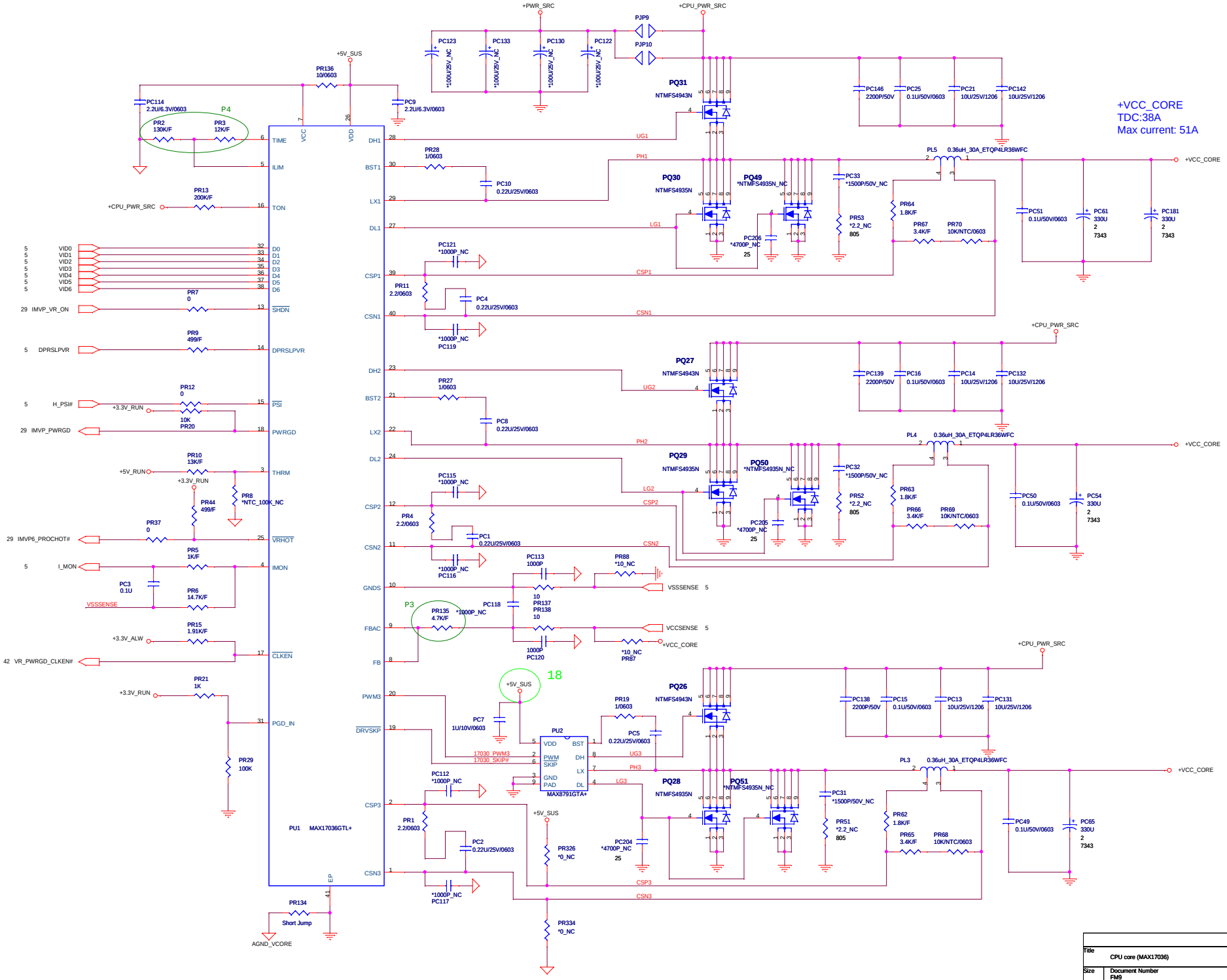
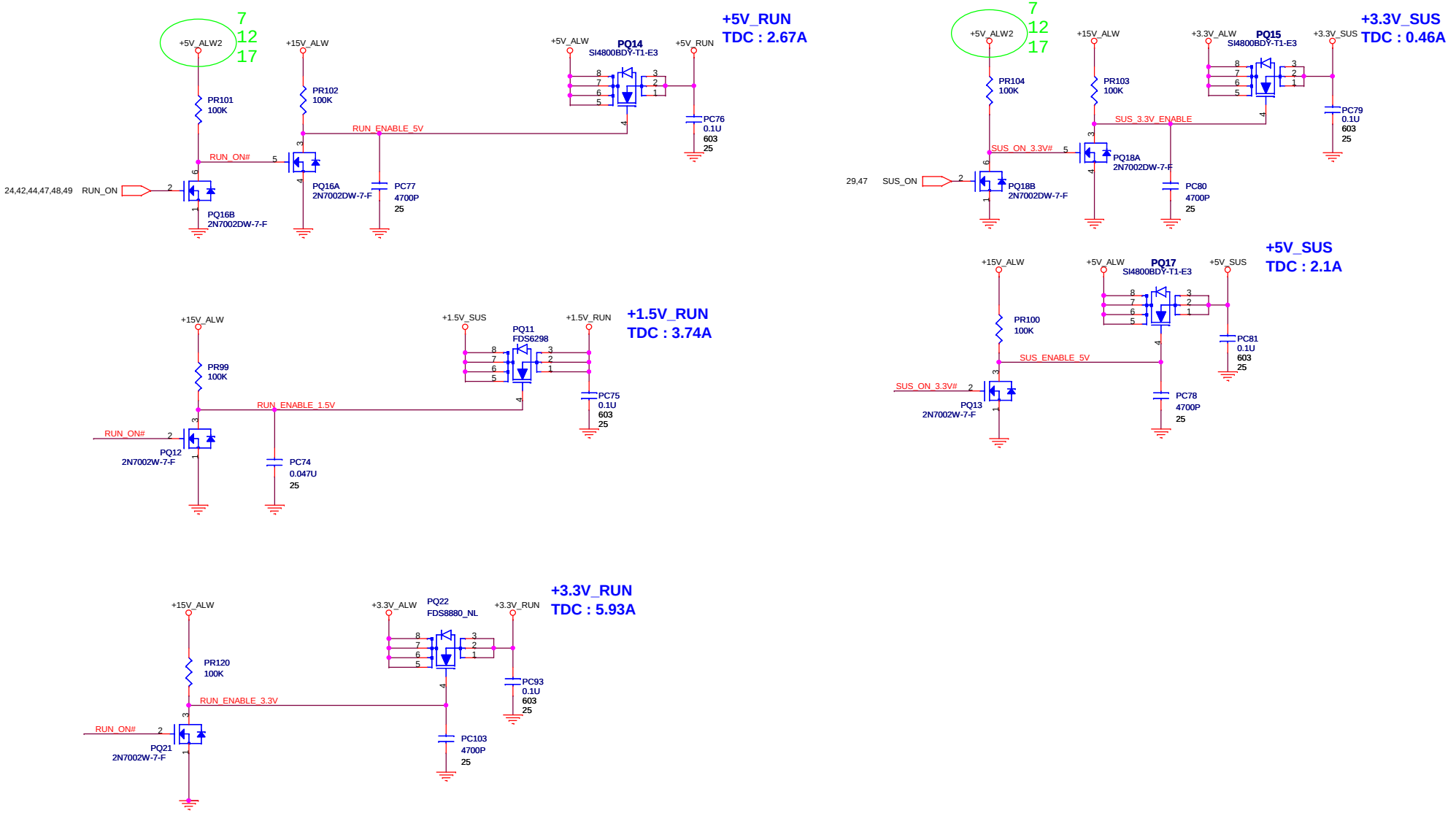


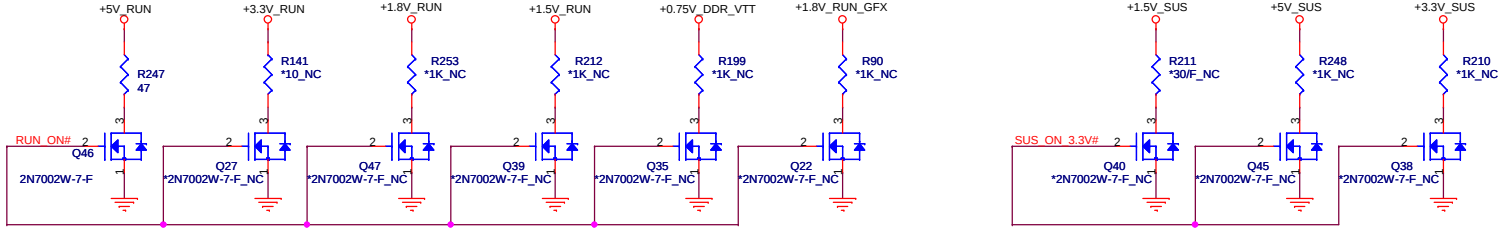
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	GFX_CORE_CNTRL2	+VCC_GFX_CORE
LOW	LOW	LOW	1.2V
HIGH	LOW	LOW	1.1V
HIGH	HIGH	LOW	1.0V
HIGH	HIGH	HIGH	0.9V

Title	VGA power (MAX8792 & RT9018B)		
Size	Document Number FM9		Rev 2B
Date: Monday, May 25, 2009	Sheet 50 of 66		


+VCC_CORE
TDC:38A
Max current: 51A
PU1 MAX17036GTL+
PU2 MAX8791GTA+
PQ31 NTMFS4943N
PQ30 NTMFS4935N
PQ49 *NTMFS4935N_NC
PQ27 NTMFS4943N
PQ29 NTMFS4935N
PQ50 *NTMFS4935N_NC
PQ26 NTMFS4943N
PQ28 NTMFS4935N
PQ51 *NTMFS4935N_NC
PL5 0.36uH_30A_ETQP4LR36WFC
PL4 0.36uH_30A_ETQP4LR36WFC
PL3 0.36uH_30A_ETQP4LR36WFC
+PWR_SRC
+CPU_PWR_SRC
+5V_SUS
+3.3V_RUN
+3.3V_ALW
AGND_VCORE
Short Jump
P3
P4
18
Title
CPU core (MAX17036)
Size
Document Number
FM9
Rev
2B
Date: Monday, May 25, 2009
Sheet 51 of 66

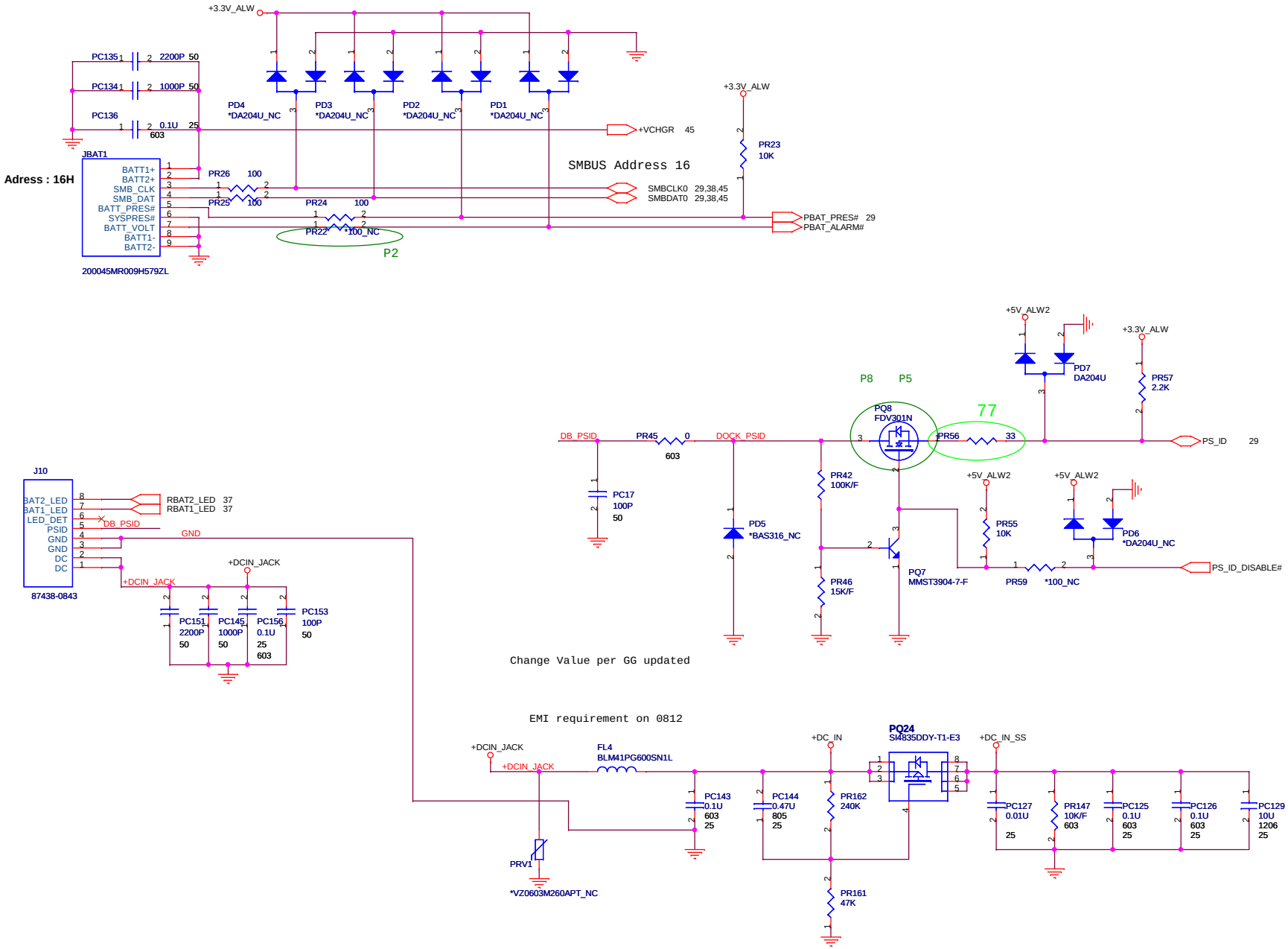


Reserve discharge path



QUANTA COMPUTER

Title	RUN / SUS POWER SW	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 52 of 66	



QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number FM9	Rev 2B
Date: Tuesday, June 02, 2009	Sheet 53 of 65	

FOR CPU use

H16 *H-C276D177P2_NC H-C276D157P2
H9 *H-C276D177P2_NC H-C276D157P2
H17 *H-C276D177P2_NC H-C276D157P2
H10 *H-C276D177P2_NC H-C276D177P2

TH1 H-TC118BC197D63P2
TH2 H-TC118BC197D63P2

For MiniCard nut use. on 31' header

H3 *H-TC315BC394D79P2_NC H-TC315BC394D79P2
H1 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H24 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H14 *H-TC315BC335D126P2_NC h-tc315bc295d126p2

H13 *H-C256D154P2_NC H-C256D154P2
H11 *H-C256D154P2_NC H-C256D154P2

For GPU nut use.

H6 *o-o177x472d177x472n_NC o-o177x472d177x472n
H27 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H26 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H19 *h-fm8b-1_NC h-fm8b-1

H22 *H-C256D154P2_NC H-C256D154P2
H20 *H-C256D154P2_NC H-C256D154P2

For PCH nut use.

H21 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H15 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H8 *H-TC315BC394D126P2_NC H-TC315BC394D126P2
H2 *h-TC256BC315D110P2_NC h-TC256BC315D110P2

102
PV1 PAD_V_6 GND
PV2 PAD_V_6 GND
46
PV3 *PAD138X98XH_NC GND

H5 *h-tc256bc315d126p2_NC h-tc315bc394d126p2

H7 *H-C228D228N_NC H-C228D228N
H4 *H-C228D228N_NC H-C228D228N
H12 *H-C197D197N_NC H-C197D197N
H25 *H-C394D394N_NC H-C394D394N
H18 *H-TC256BC315D126P2_NC H-TC256BC315D126P2

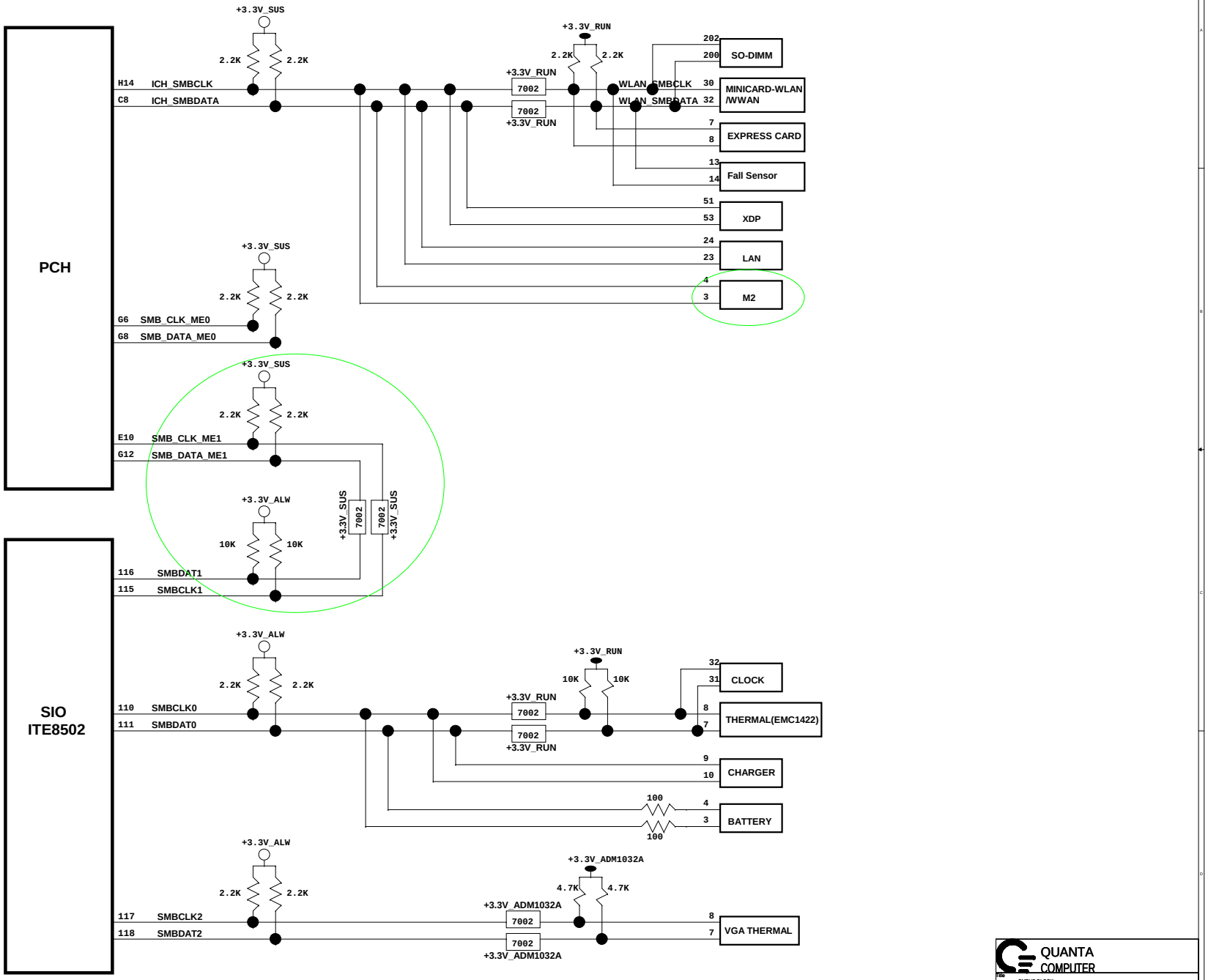
QUANTA COMPUTER

Title	SCREW PAD	
Size	Document Number FM9	Rev 2B
Date: Monday, June 08, 2009	Sheet 54 of 66	

Reserved for EMI.

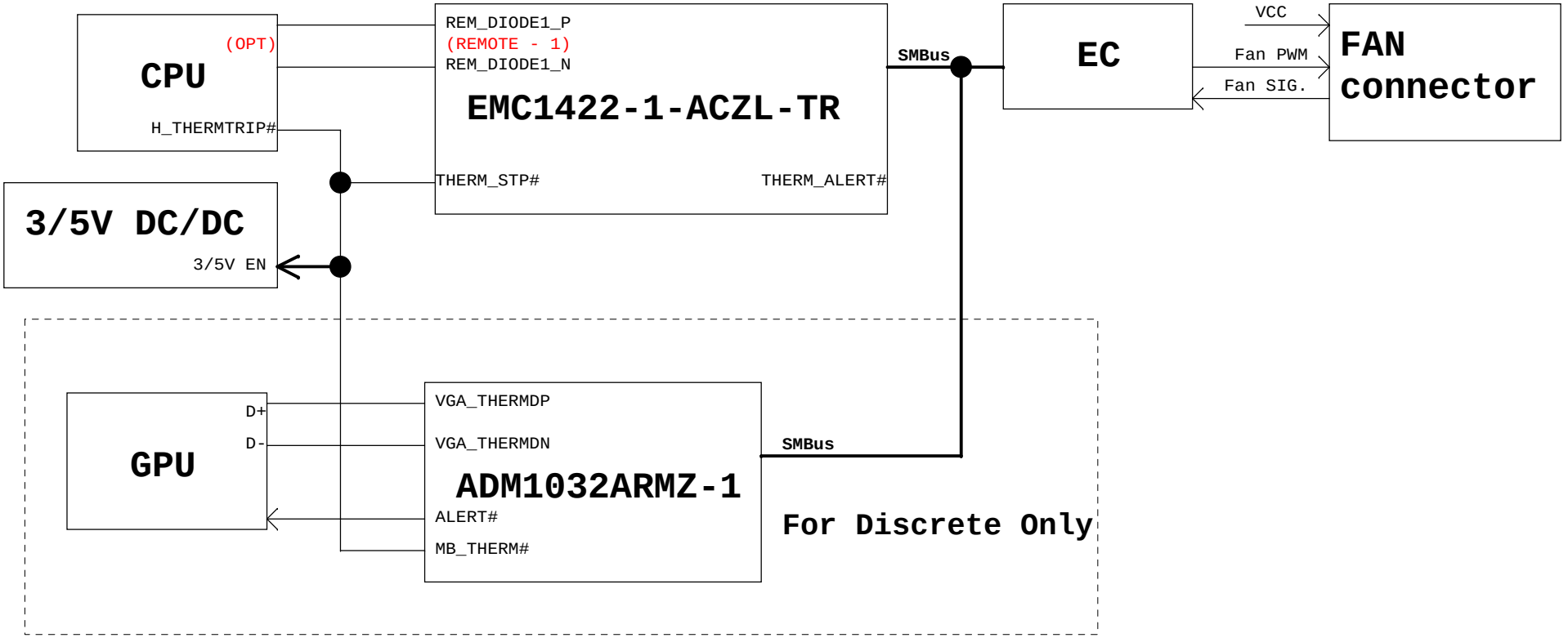
QUANTA COMPUTER

Title	EMI CAP	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 55 of 66	



QUANTA COMPUTER

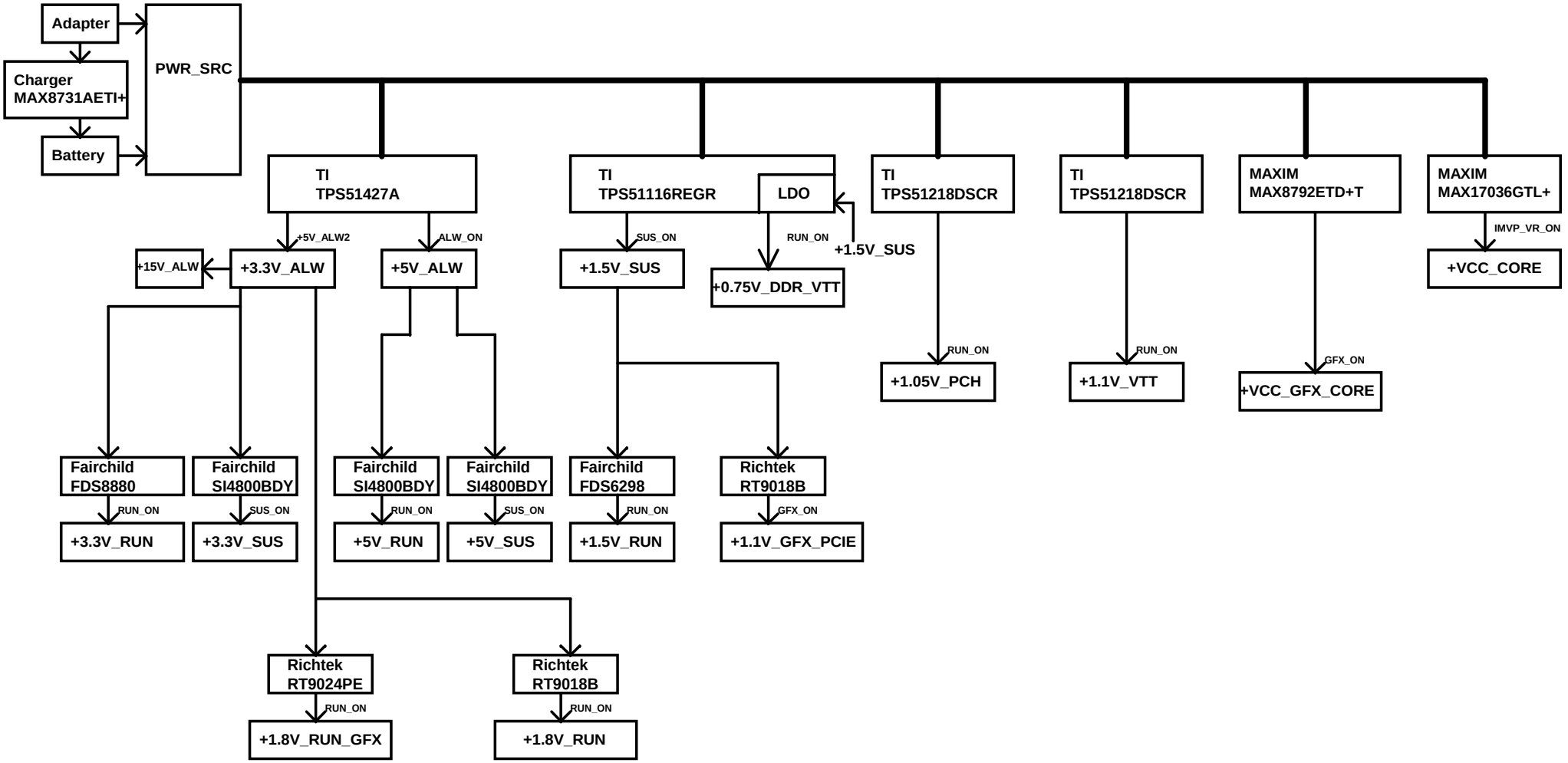
Title	SMBUS BLOCK	
Size	Document Number FM9	Rev 2S
Date: Monday, May 25, 2009	Sheet 56 of 66	



QUANTA COMPUTER

Title	Thermal Map	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 57 of 66	

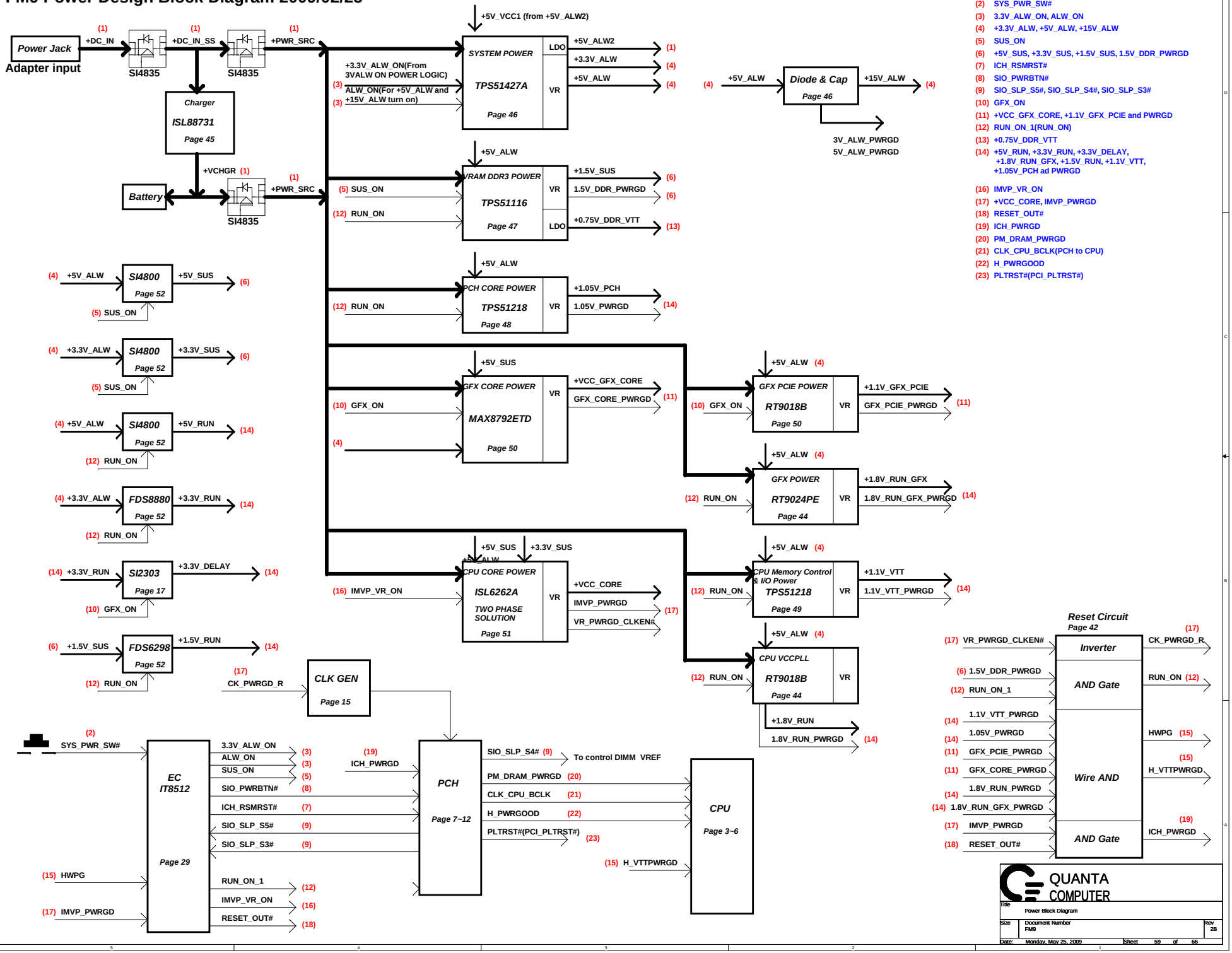
VER : 1A



QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 58 of 66	

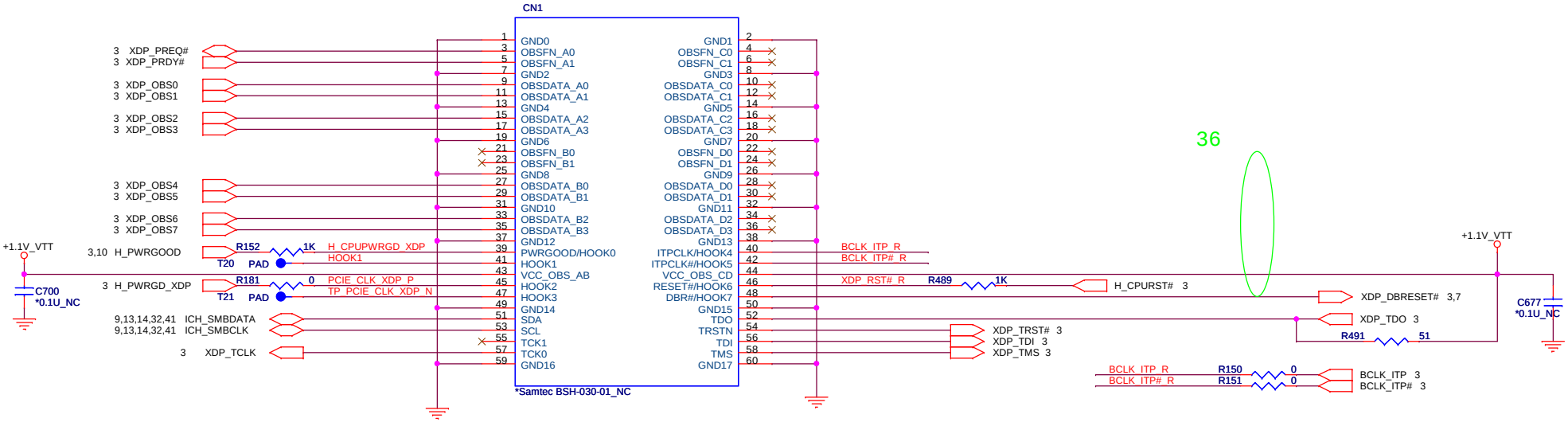
FM9 Power Design Block Diagram 2009/02/25



(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2) SYS_PWR_SW#
(3) 3.3V_ALW_ON, ALW_ON
(4) +3.3V_ALW, +5V_ALW, +15V_ALW
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
(7) ICH_RSMRST#
(8) SIO_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) GFX_ON
(11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
(12) RUN_ON_1(RUN_ON)
(13) +0.75V_DDR_VTT
(14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
(16) IMVP_VR_ON
(17) +VCC_CORE, IMVP_PWRGD
(18) RESET_OUT#
(19) ICH_PWRGD
(20) PM_DRAM_PWRGD
(21) CLK_CPU_BCLK(PCH to CPU)
(22) H_PWRGOOD
(23) PLTRST#(PCI_PLTRST#)

QUANTA COMPUTER

Title	Power Block Diagram	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 59 of 66	



It is for debug. requesst vendeer provide 200 pcs sample.

QUANTA COMPUTER

Title	SMBUS BLOCK	
Size	Document Number FM9	Rev 2B
Date: Monday, May 25, 2009	Sheet 60 of 66	

MODEL	REV	CHANGE LIST
FM8 MB	1A	Refer to ECN No.

Model / Page	FM8 MB FM	FM8 MB TO
1		
2	1A	
3	1A	2A
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	2A
14	1A	2A
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	
31	1A	2A
32	1A	
33	1A	
34	1A	2A
35	1A	2A
36	1A	
37	1A	
38	1A	2A
39	1A	
40	1A	2A
41	1A	
42	1A	
43	1A	
44	1A	
45	1A	
46	1A	
47	1A	
48	1A	
49	1A	
50	1A	
51	1A	
52	1A	
53	1A	2A
54	1A	
55	1A	

QUANTA COMPUTER

PROJECT : FM8	DOC. NO.	**REV:**	ASSY:
APPROVED BY : Kevin Chang	CHECKED BY: Kevin Yu	**DRAWN BY : Kevin Yu**	**DATE :**

SHEET 0 OF 0