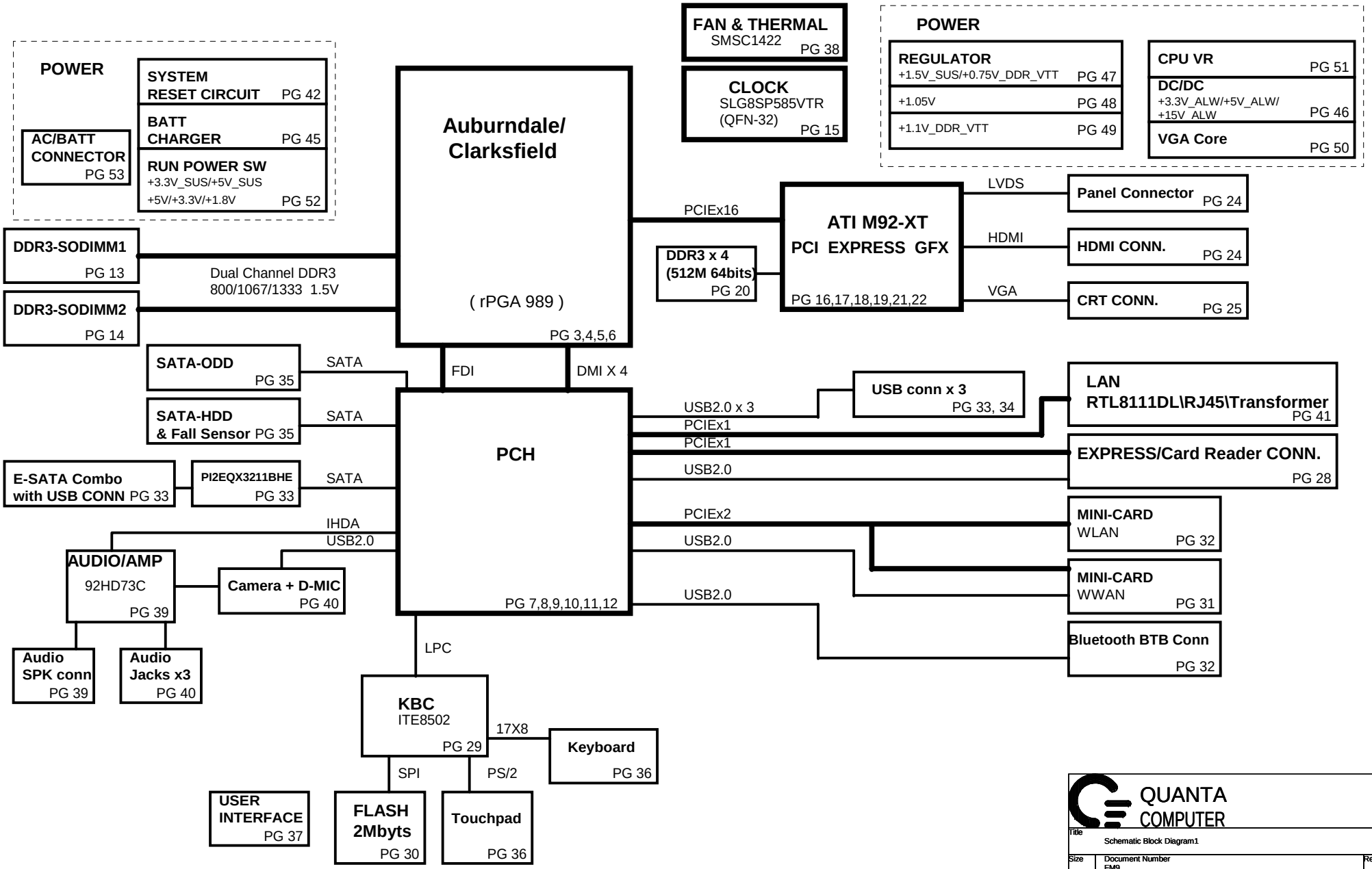
FM9 XXXX Intel Discrete GFX

VER : 1A
PWA:
PWB:



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+3.3V_ALW	+3.3V	08,29,30,35,36,37,42,44,45,46,47,52,53	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	37,46,53	LARGE POWER	RUN_ON	S0~S5
+3.3V_LAN	+3.3V	41	LAN POWER	AUX_ON	
+5V_SUS	+5V	11,33,34,35,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	7,09,10,11,13,14,19,24,26,28,29,37,41,42,44 ,48,49,50,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.8V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.9V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30 ,31,32,33,35,37,38,39,40,41,42,46,51,52,59	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,26,44,52	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	CALISTOGA/ICH9 POWER	RUN_ON	
+1.8V_RUN_GFX	+1.25V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN	
+5V_HDD	+5V	36	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,59			
+1.1V_GFX_PCIE	+1.1V	18,50			

GND PLANE	PAGE	DESCRIPTION
GND_CHG	46	
GND_1.05V	47	
GND_VGA	50	
GND_SIGNAL	51	
AGND_DC/DC	52	
GND	ALL	

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AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

SC(V1.0),P11: Should be shorted at the pins and then routed to one end of the 49.9-Ω ±1% resistor, pulled-down to GND on the board.

U34A

DMI_RX#[0] DMI_RX#[1] DMI_RX#[2] DMI_RX#[3]
DMI_RX[0] DMI_RX[1] DMI_RX[2] DMI_RX[3]
DMI_TX#[0] DMI_TX#[1] DMI_TX#[2] DMI_TX#[3]
DMI_TX[0] DMI_TX[1] DMI_TX[2] DMI_TX[3]

DMI

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]
FDI_TX[0] FDI_TX[1] FDI_TX[2] FDI_TX[3] FDI_TX[4] FDI_TX[5] FDI_TX[6] FDI_TX[7]
FDI_FSYNC[0] FDI_FSYNC[1]
FDI_INT
FDI_LSYNC[0] FDI_LSYNC[1]

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI PEG_ICOMPO PEG_RCOMPO PEG_RBIAS
PEG_RX#[0..15] PEG_RX[0..15]
PEG_TX#[0..15] PEG_TX[0..15]

PCIE_MRX_GTX_N[0..15] PCIE_MRX_GTX_P[0..15]

Clarksfield/Auburndale

R71 1K 0214

DG(V1.0),P79: should be tied to GND (through 1K ±5% resistors), if these signals are left floating, there are nofunctional impacts but a small amount of power (~15 mW) maybe wasted.
DG(V1.1) P83: FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0],FDI_LSYNC[1] can be ganged together with one resistor.

U34B

SC(V1.0),P17: SKTOCC# Can be left No Connect or tied to GND

H_COMP3 H_COMP2 H_COMP1 H_COMP0 TP_SKTOCC# H_CATERR# H_PECI H_PECI_ISO H_PROCHOT#_D H_THERM H_CPURST# PM_SYNC VCCPWRGOOD_1 VCCPWRGOOD_0 PM_DRAM_PWRGD H_VTTPWRGD H_PWRGD_XDP PLTRST#

COMP3 COMP2 COMP1 COMP0 SKTOCC# CATERR# PECI PROCHOT# THERMTRIP# RESET_OBS# PM_SYNC VCCPWRGOOD_1 VCCPWRGOOD_0 SM_DRAMPWROK VTTPWRGOOD TAPPWRGOOD RSTIN#

MISC THERMAL PWR MANAGEMENT

BCLK BCLK# BCLK_ITP BCLK_ITP# PEG_CLK PEG_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK#

CLOCKS

SM_DRAMRST# SM_RCOMP[0] SM_RCOMP[1] SM_RCOMP[2] PM_EXT_TS#[0] PM_EXT_TS#[1]

DDR3 MISC

PRDY# PREQ# TCK TMS TRST# TDI TDO TDI_M TDO_M DBR#

JTAG & BPM

BPM#[0..7]

Clarksfield/Auburndale

SC(V1.0),P17,35: This signal should be connected to the processor's VCCPWRGOOD_1 and VCCPWRGOOD_0 input to indicate when the processor power is valid.

VTTPWRGOOD SC(V1.0)P18: VTT_1.1 VR power good signal to processor. Signal voltage level is 1.1 V.

RSTIN#: DG(V1.11)(Doc.# 414044),P10: Need a voltage divider network to scale down from 3.3V (PCH driven) to 1.05V/1.1V (Clarksfield/Auburndale)

R164 1.5K/F R163 750/F 0214

1 +1.5V_SUS R171 4.75K/F R97 12K/F PM_DRAM_PWRGD

SM_DRAMPWROK: DG(V1.0) P311&SC(V1.0) P18:recommend 4.75-kΩ pull-up to DDR3 Power Rail (VDDQ) of +V1.5U and a 12-kΩ pull-down to ground to convert to processor's VTT level. CRB(V1.0) P11:CRB uses a 3.3V (always ON) rail with 2K and 1K combination. CRB Implementation is different for the Calpella Platform Design Guide. Customers to follow the latest Calpella Platform Design Guide for DRAMPWROK Implementation.

+3.3V_RUN R144 10M Q29 2N7002W-7-F C313 0.1U 16 H_THERM Q28 MMST3904-7-F PM_THRMTRIP# 46

DBR#: SC(V1.0) P22:Connected to the DBR# pin of the Processor.50-Ω to 5-kΩ pull-up to 3.3VS CRB(V1.0) P11,P71:CRB uses a 1-kΩ pull-up to 3.3VS. On the CRB this signal is ANDed with Master Reset to generate SYS_RESET.

DBR#:(Intell feedback) Nothing wrong w/ CRB design. If you want to connect it to PCH directly, make sure pull high to 3.3V (S0) main power.

CRB(v0.71) P.11

XDP_PRDY# XDP_PREQ# XDP_TCLK XDP_TMS XDP_TRST# XDP_TDI_R XDP_TDO_R XDP_TDI_M XDP_TDO_M XDP_DBRESET# XDP_OBS[0:7]

PCIE_MTX_GRX_C_N[0..15] PCIE_MTX_GRX_N[0..15] PCIE_MTX_GRX_N[0..15] 16
PCIE_MTX_GRX_C_P[0..15] PCIE_MTX_GRX_P[0..15] PCIE_MTX_GRX_P[0..15] 16

SM_DRAMPWROK:(Intell Feedback) Either way works.

CRB(V1.0) P11: is it necessary

T18 T17 +1.1V_VTT XDP_TMS XDP_TDI_R XDP_TRST# XDP_TCLK R158 R493 R157 R156 *51_NC

JTAG MAPPING

XDP_TDI_R R494 0 XDP_TDI 60
XDP_TDO_M R497 0_NC XDP_TDO 60
XDP_TRST# R499 51
R496 0
XDP_TDI_M R495 0_NC
XDP_TDO_R R498 0

Scan Chain (Default)	STUFF -> R780, R783, R786 NO STUFF -> R781, R785
CPU Only	STUFF -> R780, R781 NO STUFF -> R783, R785, R786
GMCH Only	STUFF -> R785, R786 NO STUFF -> R780, R781, R783

DG(v1.0) table 27

TRSI#: SC(V1.0)P22: should be routed as a single daisy chain to all loads and terminated at the end of the trace. 51 Ω ± 5% pull down resistor. CRB()V1.0)P11

Processor Pullups

+1.1V_VTT R100 49.9/F R121 49.9/F R122 *68_NC H_CATERR# H_PROCHOT#_D H_CPURST#

SC(1.0V),P17: H_PROCHOT#D use: pull to 68 ohm if it isn'tt used: pull to 50 ohm

SC(1.0V),P17: H_CATERR# 49.9-Ω ±1% Pull-Up to the VTT rail (+V1.1S_VTT)

Processor Compensation Signals

H_COMP0 H_COMP1 H_COMP2 H_COMP3 R123 49.9/F R72 49.9/F R124 20/F R125 20/F

DG(V1.0),P17: COMP[0.1] 49.9-Ω ±1% pull-down to GND COMP[2.3] 20-Ω ±1% pull-down to GND

DDR3 Compensation Signals

SM_RCOMP_2 SM_RCOMP_1 SM_RCOMP_0 R95 130/F R89 24.9/F R94 100/F

Layout Note: Place these resistors near Processor

DG(V1.0),P83: SM_RCOMP[0] 100-Ω ±1% pull-down to GND SM_RCOMP[1] 24.9-Ω ±1% pull-down to GND SM_RCOMP[2] 130-Ω ±1% pull-down to GND

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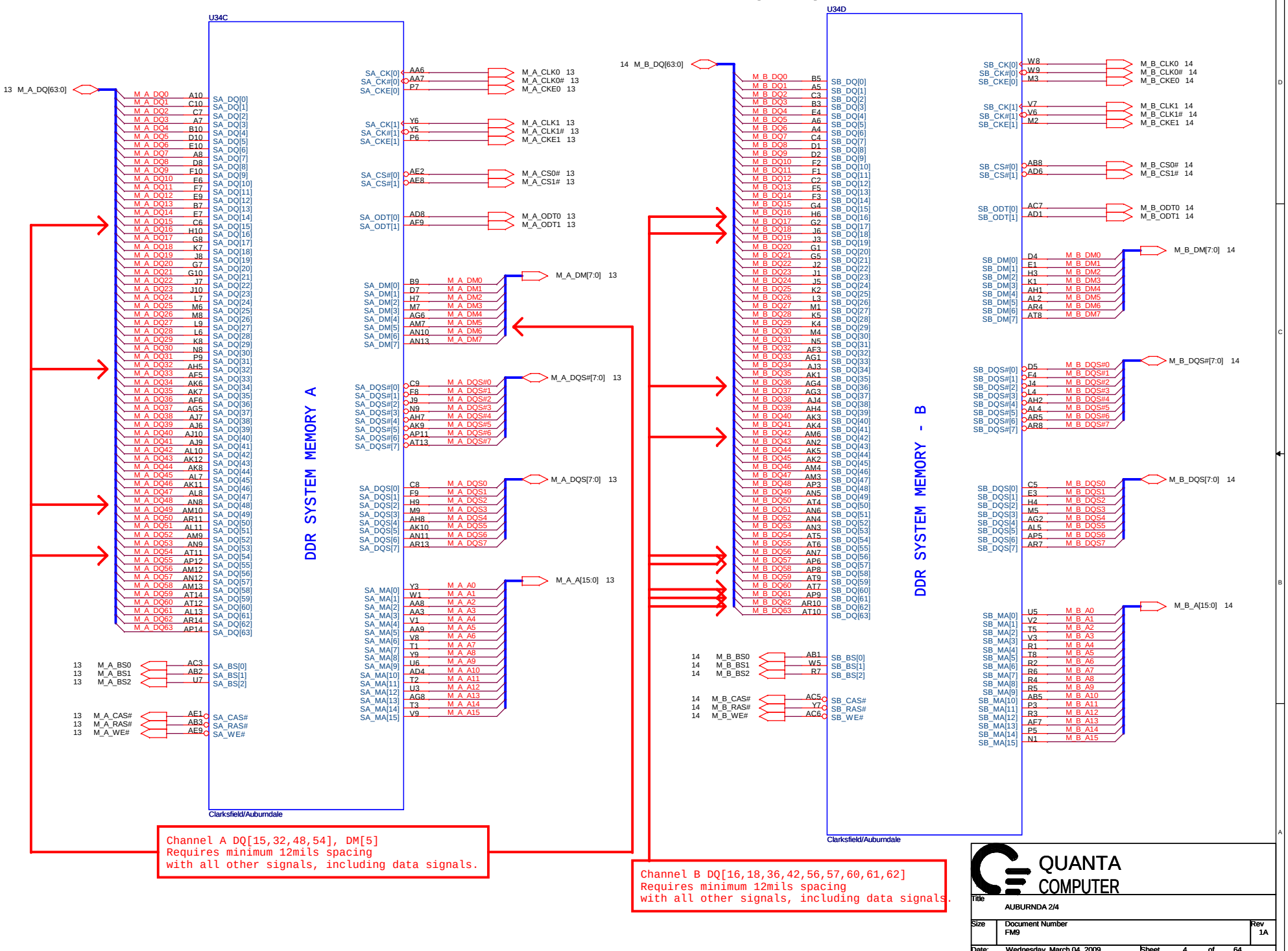
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

CPU Core Power

+VCC_CORE

U34F

Clarksfield/Auburndale

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

VTT0_43,VTT0_44:
CRB(V1.0)P13
Why add 0ohm?? Is it trace width control??

VTT0_43,VTT0_44:(Intel feedback)
They are connected to hidden page for intel validation purpose.

VTT_SELECT:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND
or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options in the design for the Turbo functionality.
The stuffing and no-stuffing of the resistors will depend on the POC configuration of AUB and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

Note:
For Validating IMVP VR R814 should be STUFF and R827 NO_STUFF

U34G

Clarksfield/Auburndale

GRAPHICS

SENSE LINES

GRAPHICS VIDS

GFX_VID[0..6],GFX_VR_EN,GFX_DPRSLPVR,GFX_IMON:
Could this be left unconnected when not in use?

GFX_VID[0..6],GFX_VR_EN,GFX_DPRSLPVR,GFX_IMON:(Intel feedback)
Yes, see DG rev1.5

POWER

DDR3 - 1.5V RAILS

1.1V

1.8V

PEG & DMI

+1.5V_SUS

+1.8V_RUN

+1.1V_VTT

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

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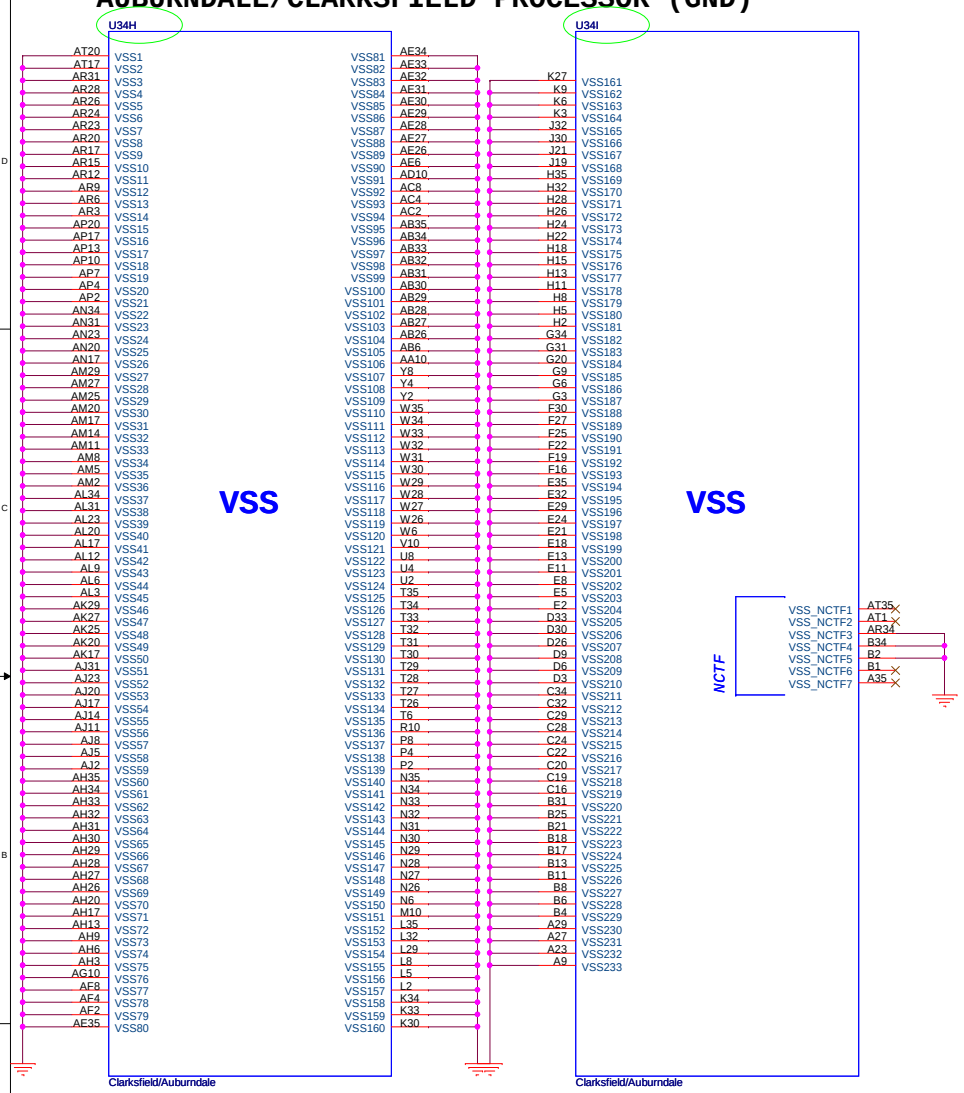
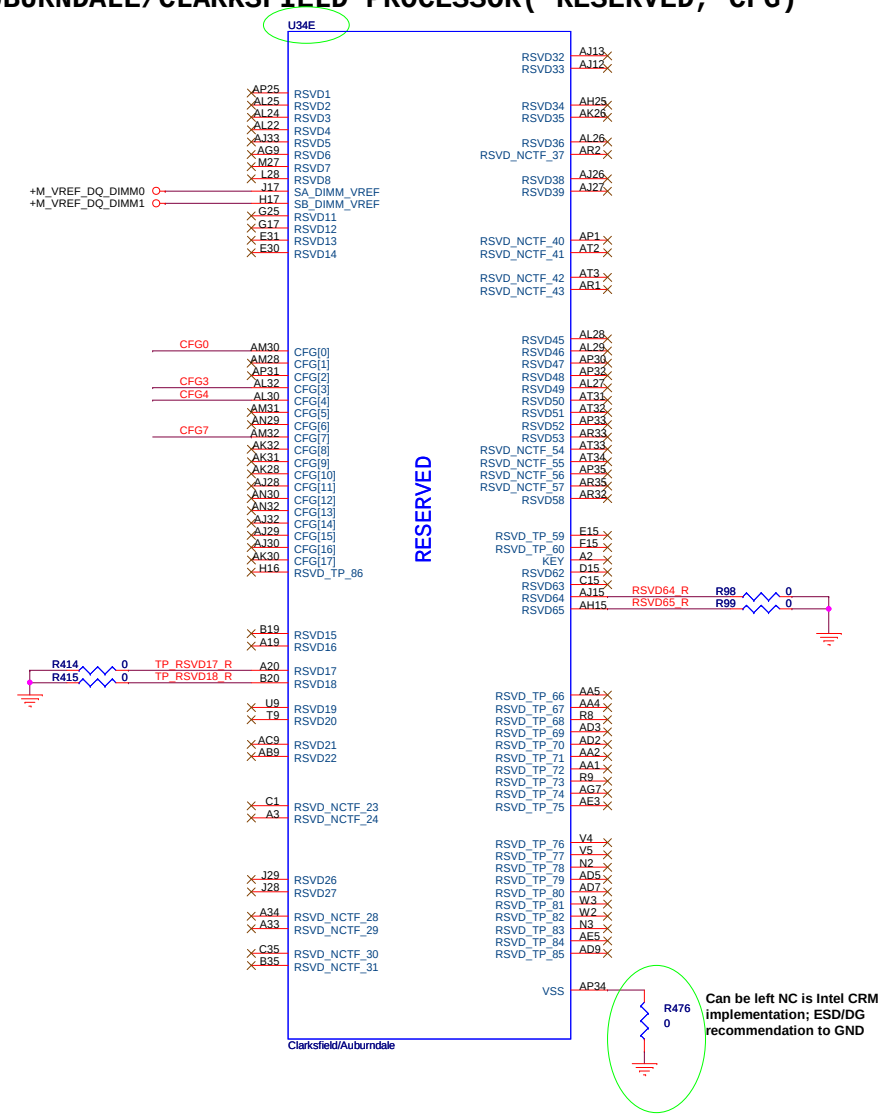
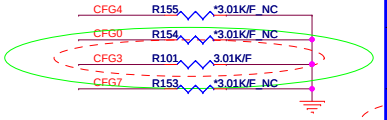
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



PCIE LANE is Lane Numbers Reversed

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

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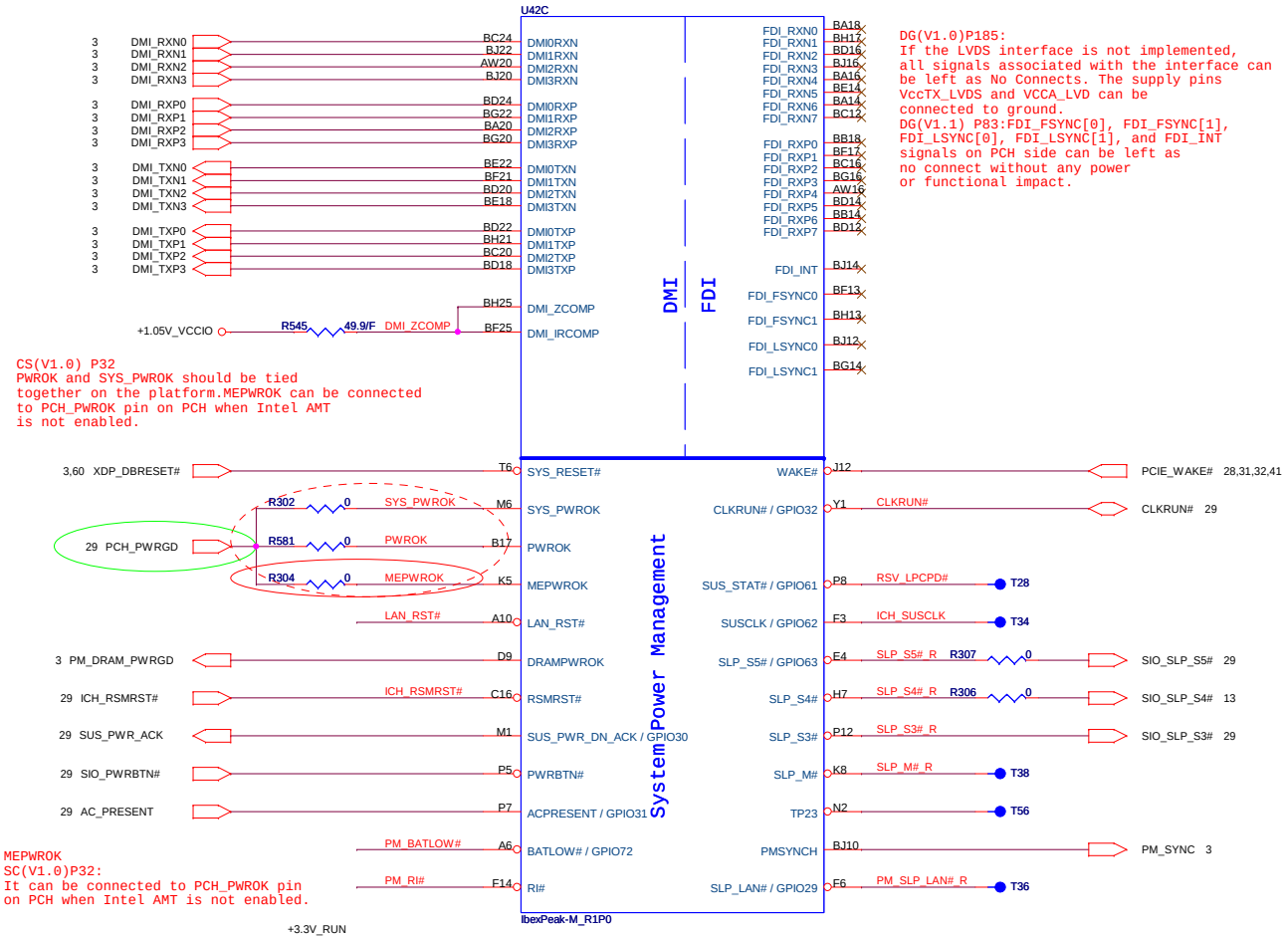
IBEX PEAK-M (DMI,FDI,GPIO)



DG(V1.0)P185:
If the LVDS interface is not implemented, all signals associated with the interface can be left as No Connects. The supply pins VccTX_LVDS and VCCA_LVD can be connected to ground.
DG(V1.1) P83:FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on PCH side can be left as no connect without any power or functional impact.

CS(V1.0) P32
PWROK and SYS_PWROK should be tied together on the platform.MEPWROK can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.

MEPWROK
SC(V1.0)P32:
It can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.

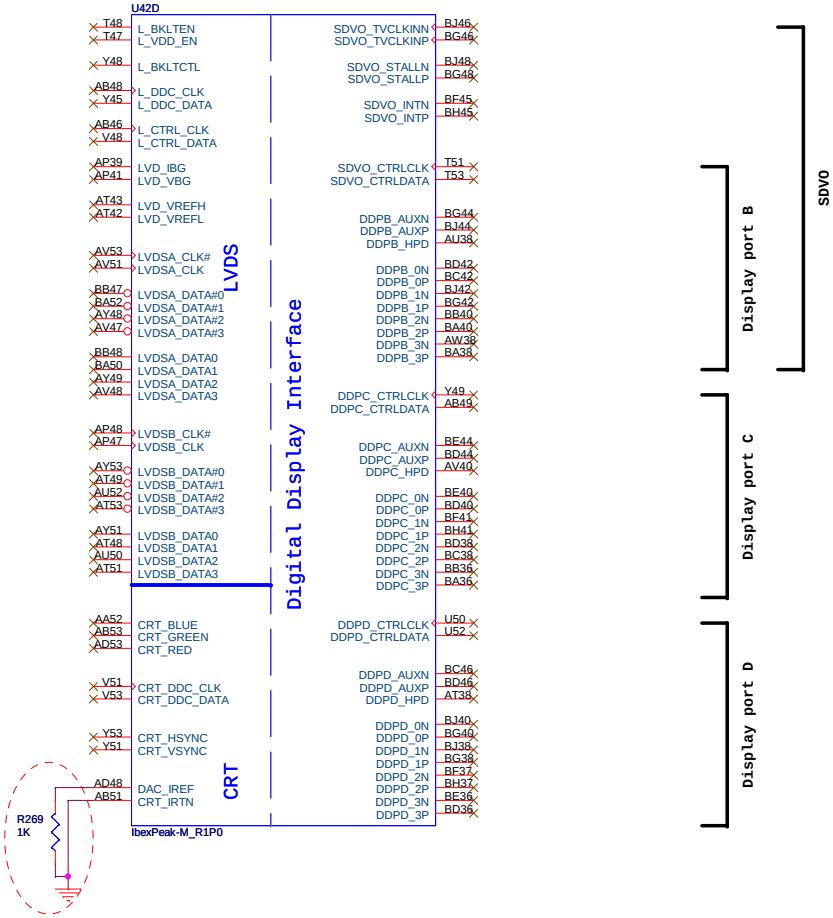
LAN_RST#
DG(V1.0) P311
If integrated LAN is not used, recommend to connect LAN_RST# to GND via an 8.2-kΩ to 10-kΩ pull-down resistor.
EDS(V1.0)P64
must be grounded if Intel LAN is disabled.

PWROK
SC(V1.0)P32:
8.2 kΩ to 10 kΩ pull-down resistor to GND.
PWROK and SYS_PWROK should be tied together on the platform.

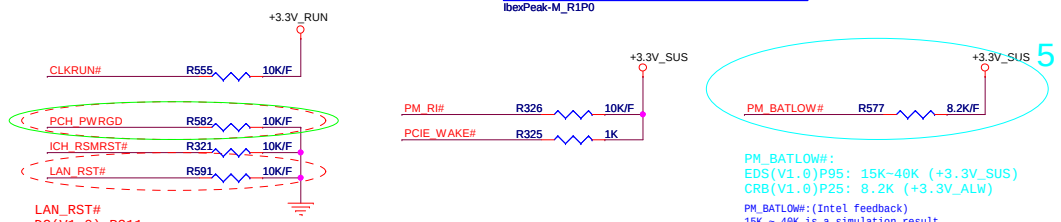
PM_BATLOW#:
EDS(V1.0)P95: 15K~40K (+3.3V_SUS)
CRB(V1.0)P25: 8.2K (+3.3V_ALW)

PM_BATLOW#:(Intel feedback)
15K ~ 40K is a simulation result, the expected value should be 20K internal pull high in PCH.
8.2K is external pull high.

IBEX PEAK-M (LVDS,DDI)



DG(V1.0)P189:
If the CRT interface is not implemented, all signals associated with the interface can be left as No Connects. The pins CRT_IRTN Connect this signals to GND and DAC_IREF Connect to GND via a 1.0 k ±0.5% pull-down resistor



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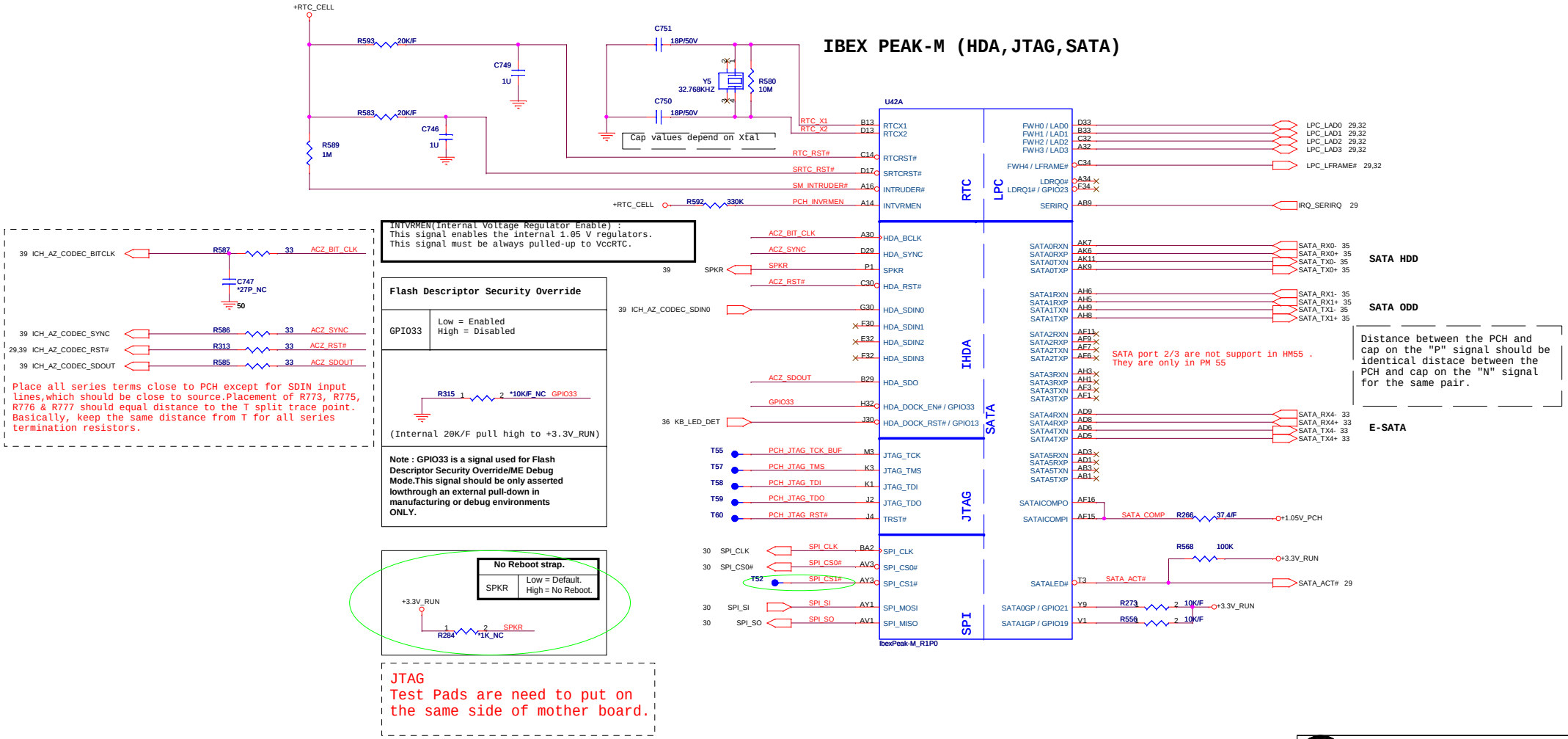
IBEX PEAK-M (HDA,JTAG,SATA)



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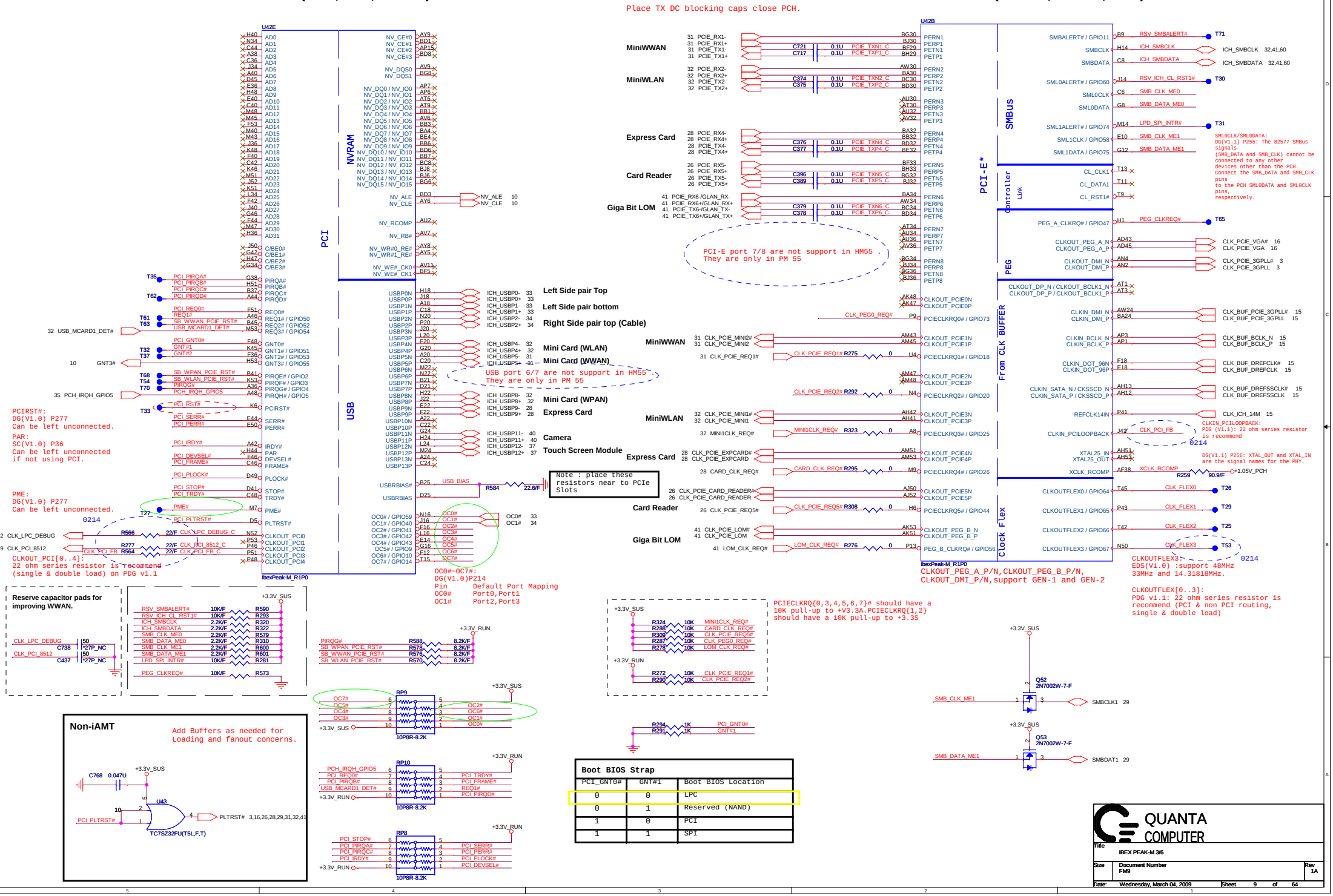
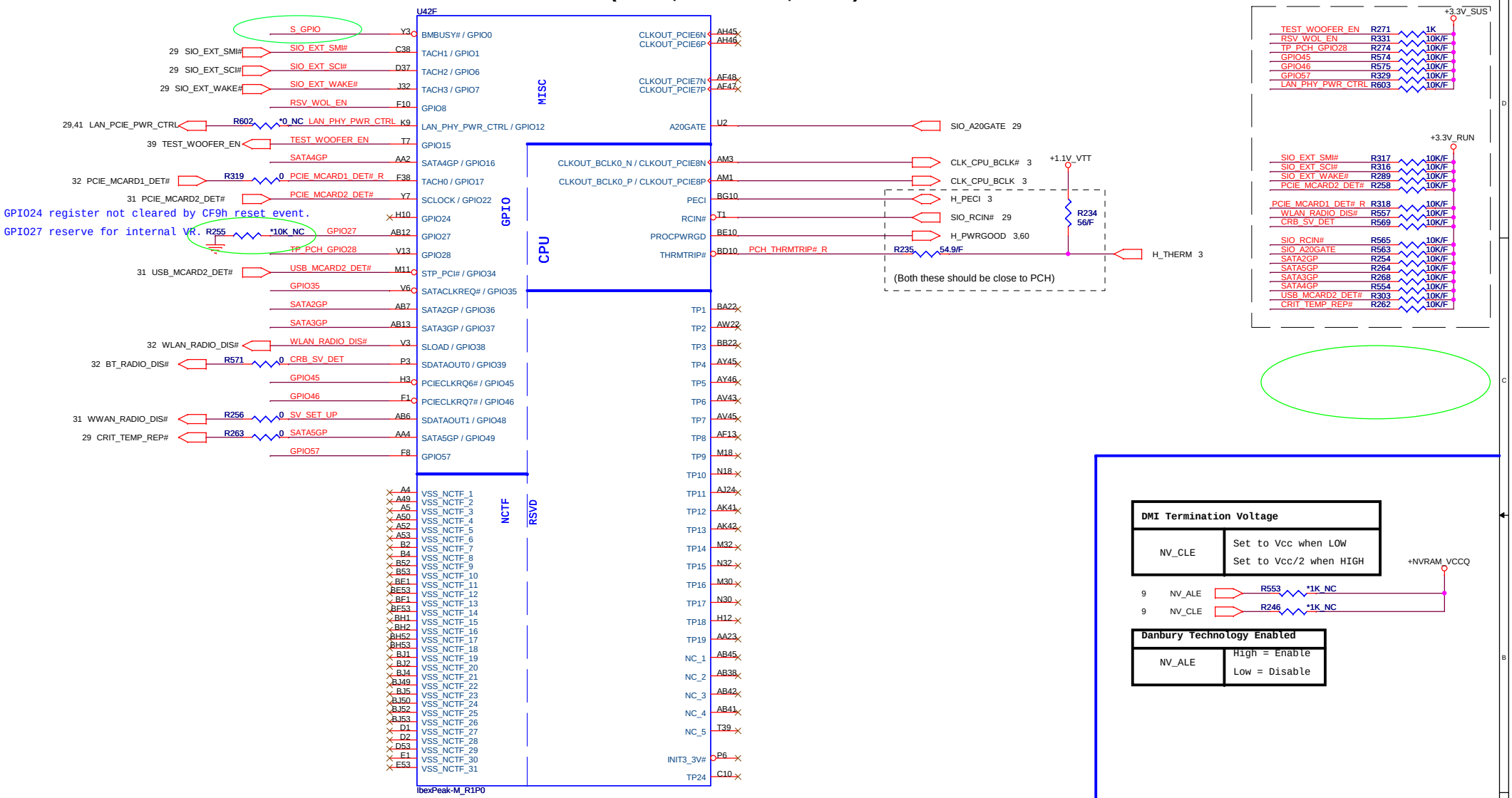
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

+NVRAM_VCCQ

9 NV_ALE R553 *1K_NC

9 NV_CLE R246 *1K_NC

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

R267 10K/F GPIO35

R572 *1K/F_NC GNT3# 9

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

+3.3V_RUN

S_GPIO R270 10K/F

SV_SET_UP R257 10K/F

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.

SV_SET_UP	1-X High = Strong (Default)

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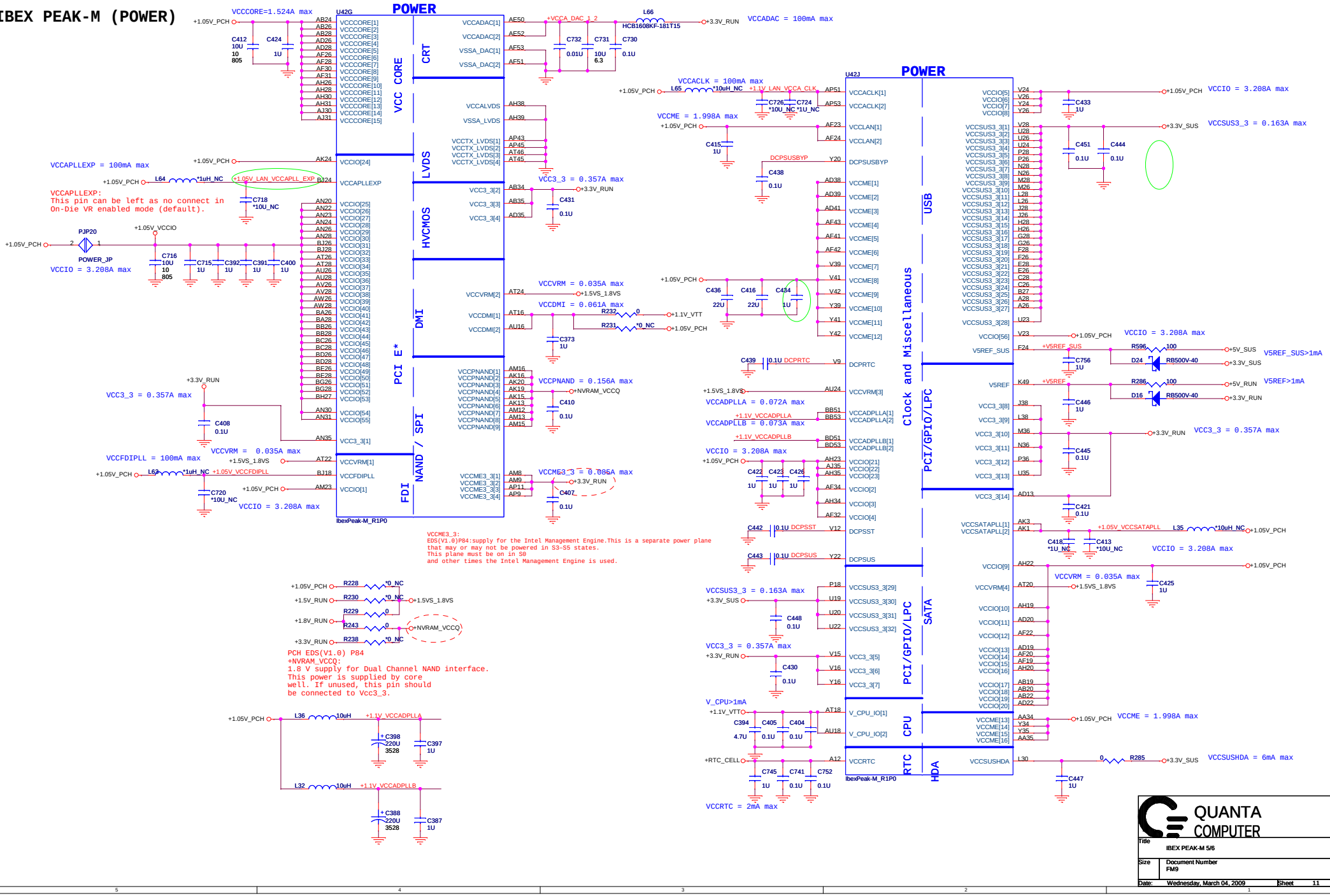
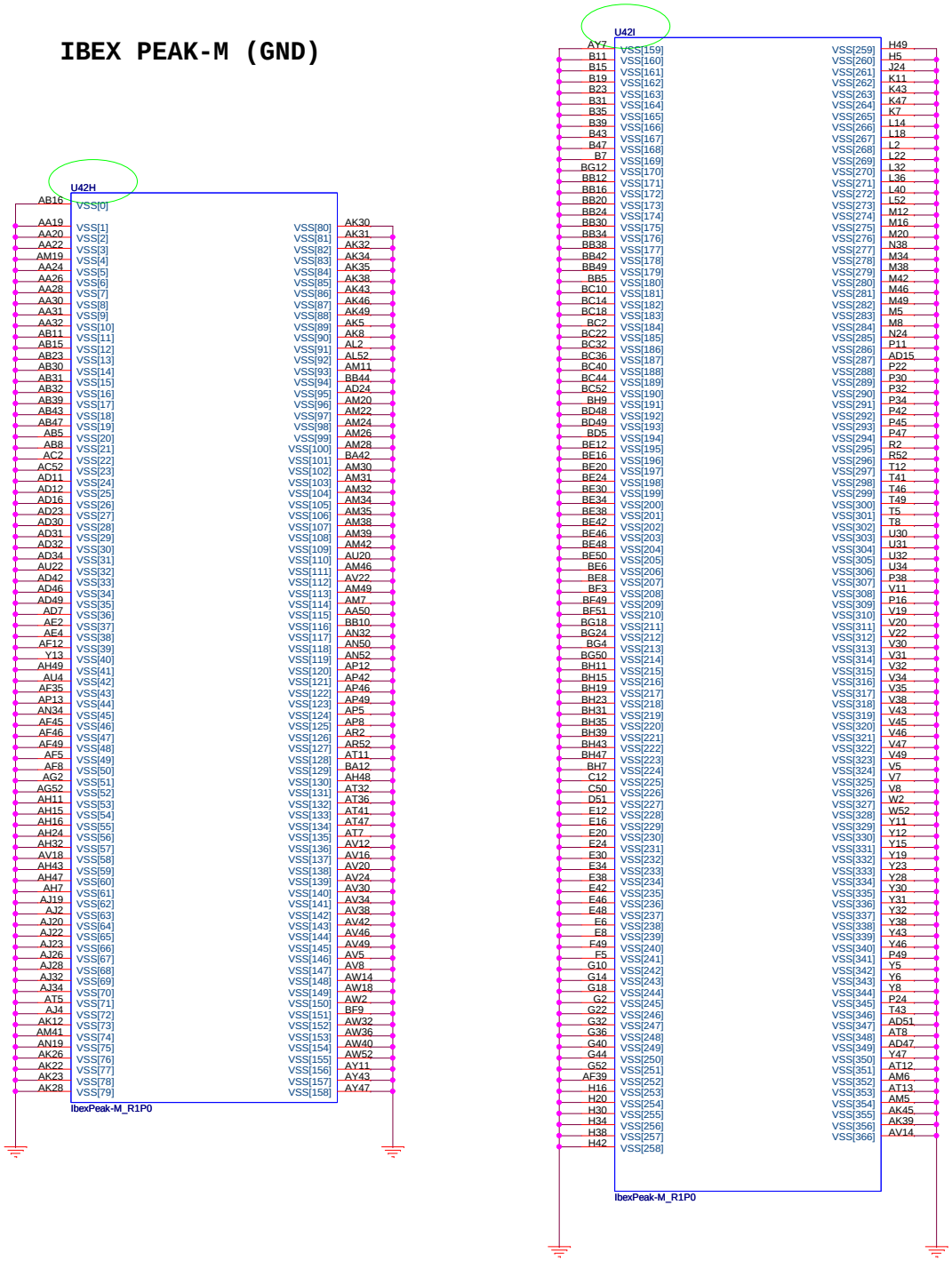
IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)



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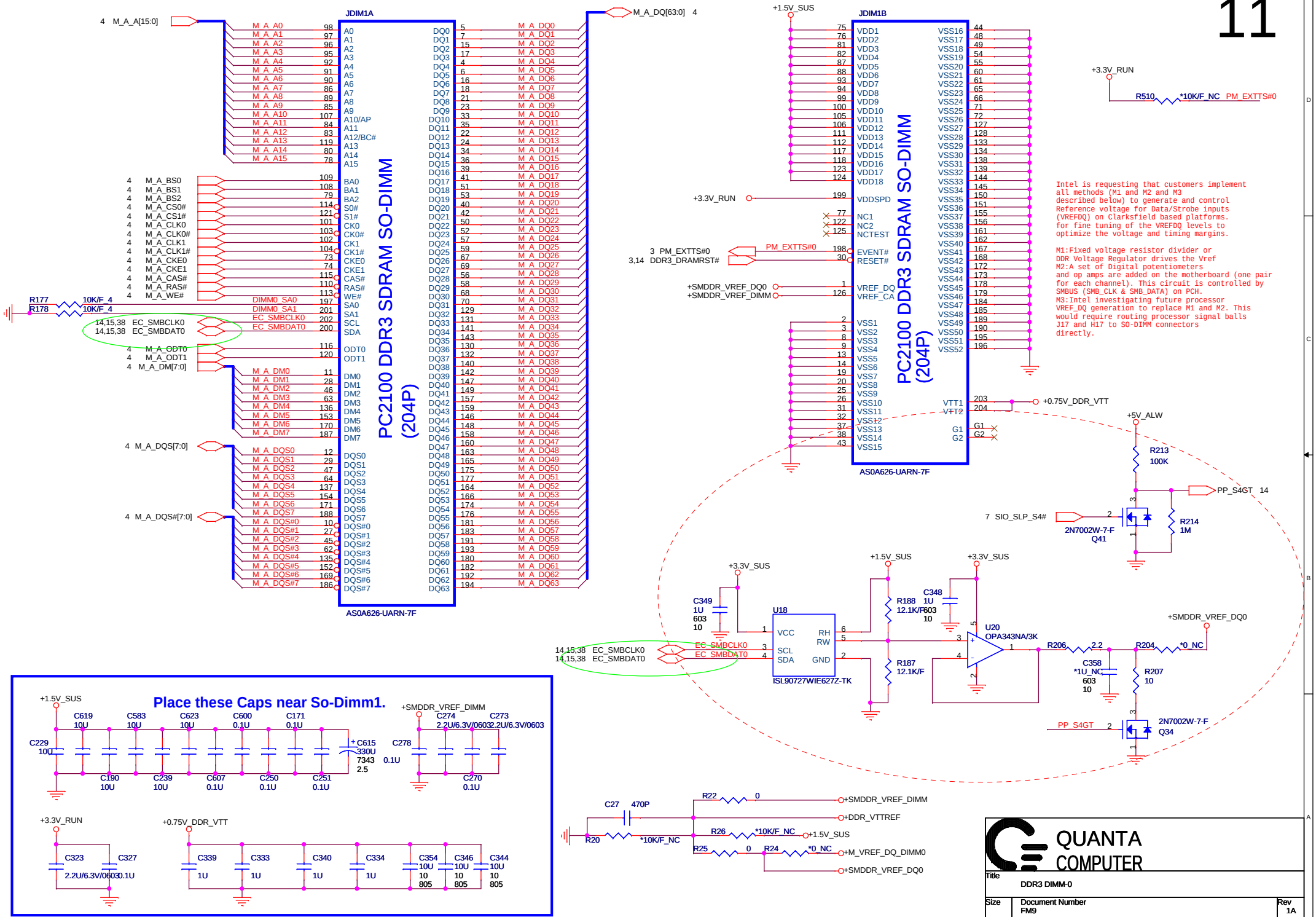

Title	DDR3 DIMM-0
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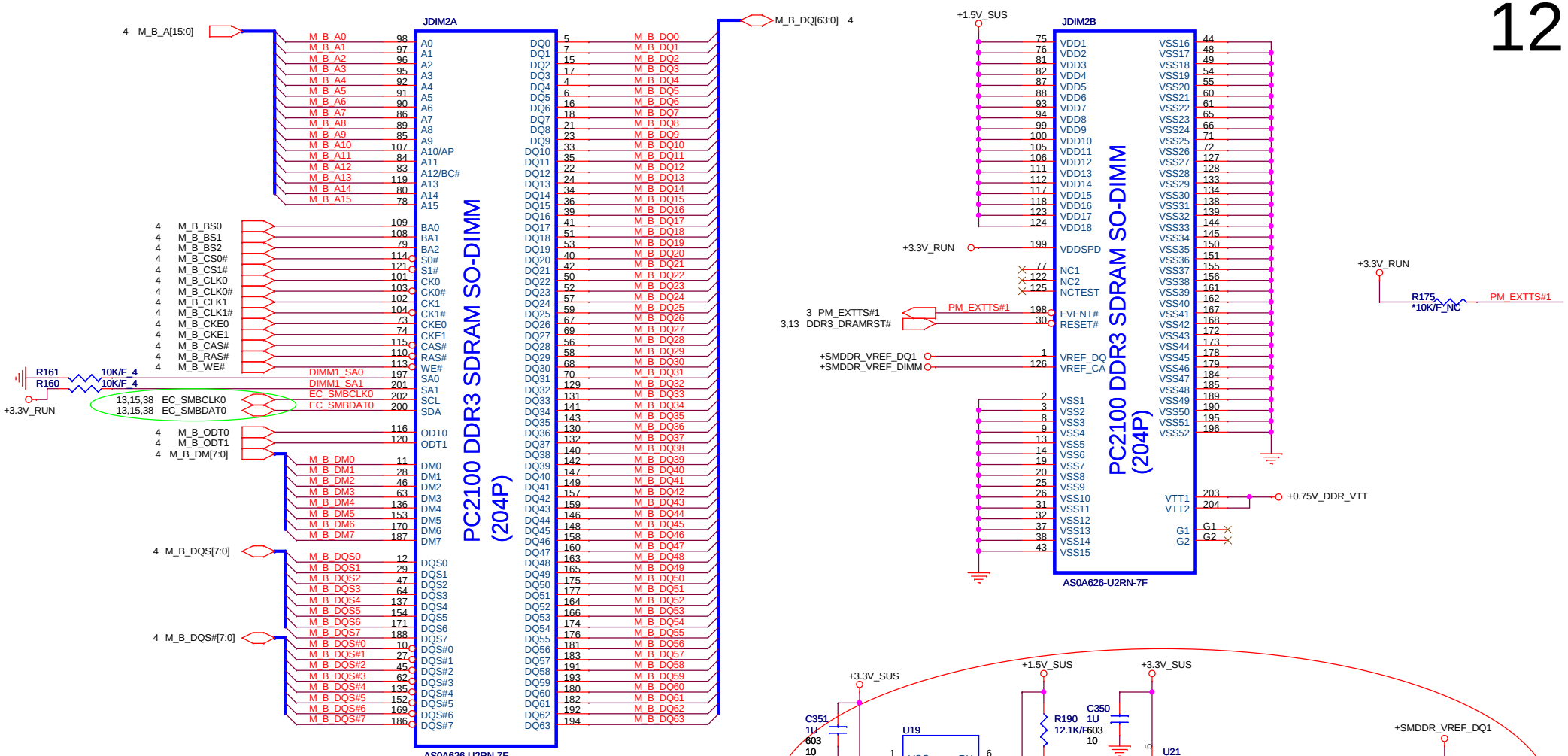
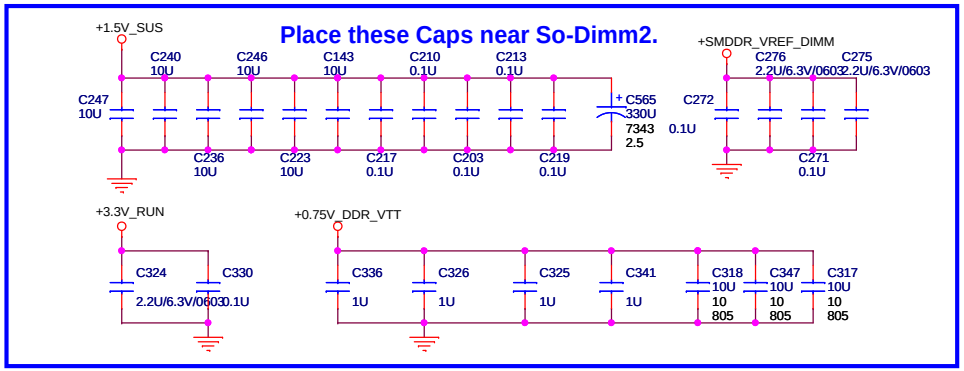
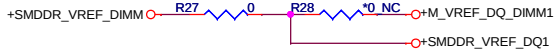


Place these Caps near So-Dimm2.





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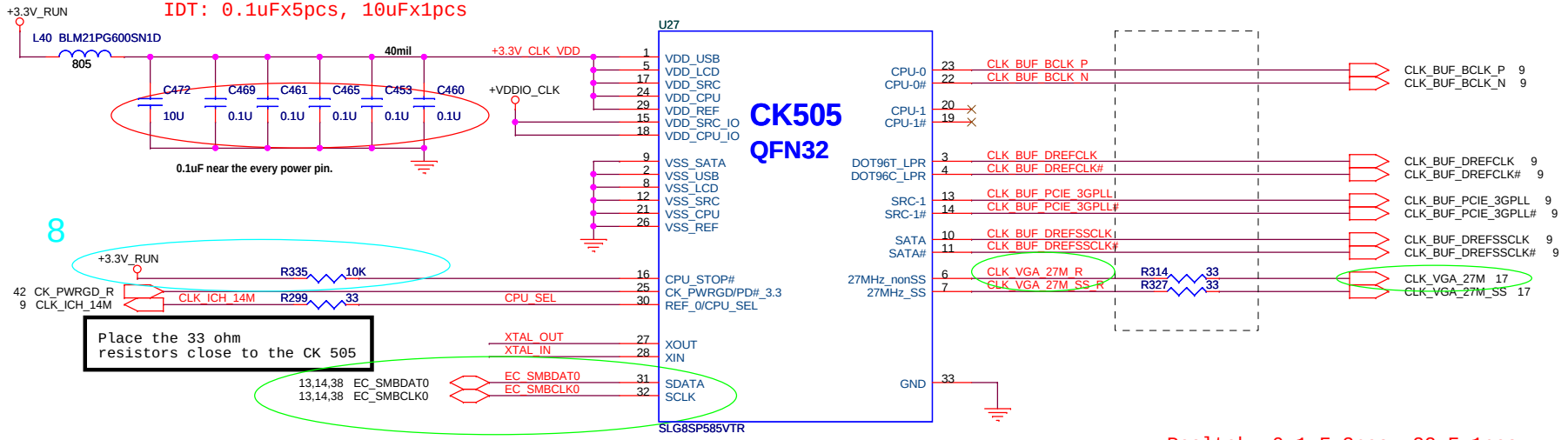
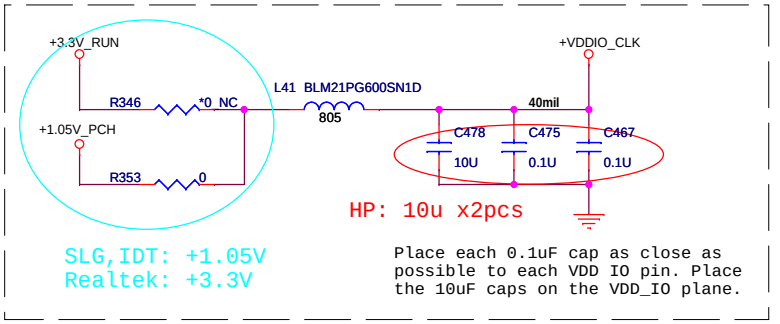
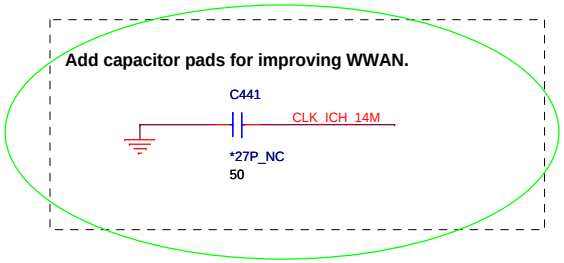
Realtek: 0.1uFx6pcs, 22uFx1pcs
IDT: 0.1uFx5pcs, 10uFx1pcs

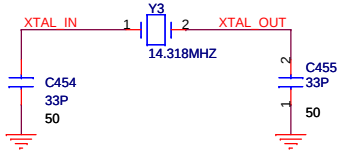
Place within 0.5" of CLKGEN



Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs

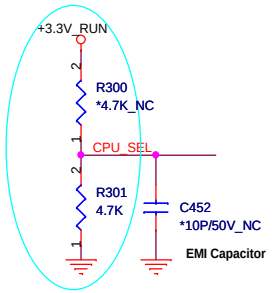






+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.

7



PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

QUANTA COMPUTER

Title	Clock Generator	
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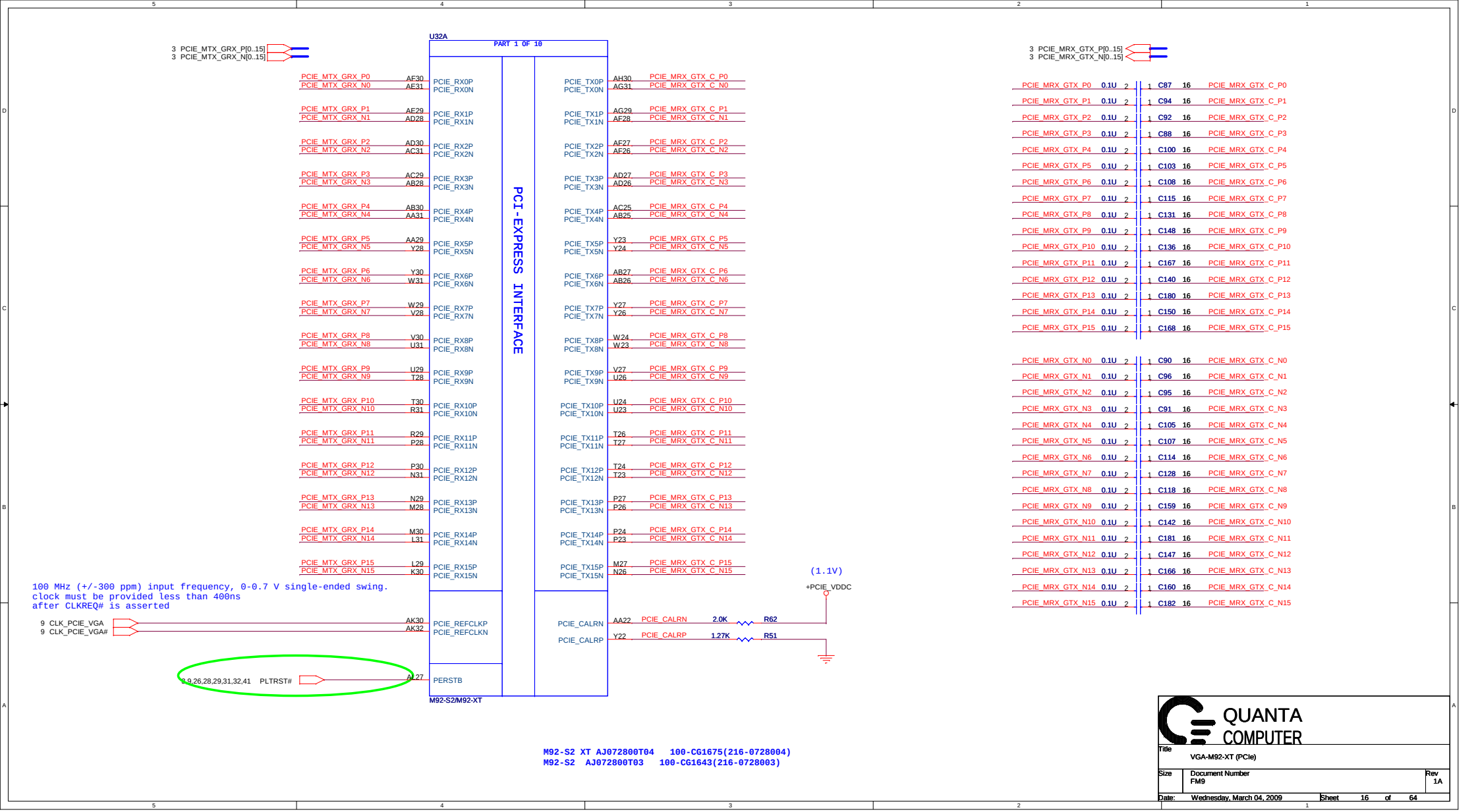
U32A
PART 1 OF 10
PCI-EXPRESS INTERFACE
M92-S2/M92-XT
3 PCIE_MTX_GRX_P[0..15]
3 PCIE_MTX_GRX_N[0..15]
PCIE_MTX_GRX_P0 AE30 PCIE_RX0P
PCIE_MTX_GRX_N0 AE31 PCIE_RX0N
PCIE_MTX_GRX_P1 AE29 PCIE_RX1P
PCIE_MTX_GRX_N1 AD28 PCIE_RX1N
PCIE_MTX_GRX_P2 AD30 PCIE_RX2P
PCIE_MTX_GRX_N2 AC31 PCIE_RX2N
PCIE_MTX_GRX_P3 AC29 PCIE_RX3P
PCIE_MTX_GRX_N3 AB28 PCIE_RX3N
PCIE_MTX_GRX_P4 AB30 PCIE_RX4P
PCIE_MTX_GRX_N4 AA31 PCIE_RX4N
PCIE_MTX_GRX_P5 AA29 PCIE_RX5P
PCIE_MTX_GRX_N5 Y28 PCIE_RX5N
PCIE_MTX_GRX_P6 Y30 PCIE_RX6P
PCIE_MTX_GRX_N6 W31 PCIE_RX6N
PCIE_MTX_GRX_P7 W29 PCIE_RX7P
PCIE_MTX_GRX_N7 V28 PCIE_RX7N
PCIE_MTX_GRX_P8 V30 PCIE_RX8P
PCIE_MTX_GRX_N8 U31 PCIE_RX8N
PCIE_MTX_GRX_P9 U29 PCIE_RX9P
PCIE_MTX_GRX_N9 T28 PCIE_RX9N
PCIE_MTX_GRX_P10 T30 PCIE_RX10P
PCIE_MTX_GRX_N10 R31 PCIE_RX10N
PCIE_MTX_GRX_P11 R29 PCIE_RX11P
PCIE_MTX_GRX_N11 P28 PCIE_RX11N
PCIE_MTX_GRX_P12 P30 PCIE_RX12P
PCIE_MTX_GRX_N12 N31 PCIE_RX12N
PCIE_MTX_GRX_P13 N29 PCIE_RX13P
PCIE_MTX_GRX_N13 M28 PCIE_RX13N
PCIE_MTX_GRX_P14 M30 PCIE_RX14P
PCIE_MTX_GRX_N14 L31 PCIE_RX14N
PCIE_MTX_GRX_P15 L29 PCIE_RX15P
PCIE_MTX_GRX_N15 K30 PCIE_RX15N
PCIE_TX0P AH30 PCIE_MRX_GTX_C_P0
PCIE_TX0N AG31 PCIE_MRX_GTX_C_N0
PCIE_TX1P AG29 PCIE_MRX_GTX_C_P1
PCIE_TX1N AF28 PCIE_MRX_GTX_C_N1
PCIE_TX2P AF27 PCIE_MRX_GTX_C_P2
PCIE_TX2N AF26 PCIE_MRX_GTX_C_N2
PCIE_TX3P AD27 PCIE_MRX_GTX_C_P3
PCIE_TX3N AD26 PCIE_MRX_GTX_C_N3
PCIE_TX4P AC25 PCIE_MRX_GTX_C_P4
PCIE_TX4N AB25 PCIE_MRX_GTX_C_N4
PCIE_TX5P Y23 PCIE_MRX_GTX_C_P5
PCIE_TX5N Y24 PCIE_MRX_GTX_C_N5
PCIE_TX6P AB27 PCIE_MRX_GTX_C_P6
PCIE_TX6N AB26 PCIE_MRX_GTX_C_N6
PCIE_TX7P Y27 PCIE_MRX_GTX_C_P7
PCIE_TX7N Y26 PCIE_MRX_GTX_C_N7
PCIE_TX8P W24 PCIE_MRX_GTX_C_P8
PCIE_TX8N W23 PCIE_MRX_GTX_C_N8
PCIE_TX9P V27 PCIE_MRX_GTX_C_P9
PCIE_TX9N U26 PCIE_MRX_GTX_C_N9
PCIE_TX10P U24 PCIE_MRX_GTX_C_P10
PCIE_TX10N U23 PCIE_MRX_GTX_C_N10
PCIE_TX11P T26 PCIE_MRX_GTX_C_P11
PCIE_TX11N T27 PCIE_MRX_GTX_C_N11
PCIE_TX12P T24 PCIE_MRX_GTX_C_P12
PCIE_TX12N T23 PCIE_MRX_GTX_C_N12
PCIE_TX13P P27 PCIE_MRX_GTX_C_P13
PCIE_TX13N P26 PCIE_MRX_GTX_C_N13
PCIE_TX14P P24 PCIE_MRX_GTX_C_P14
PCIE_TX14N P23 PCIE_MRX_GTX_C_N14
PCIE_TX15P M27 PCIE_MRX_GTX_C_P15
PCIE_TX15N N26 PCIE_MRX_GTX_C_N15
100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing.
clock must be provided less than 400ns
after CLKREQ# is asserted
9 CLK_PCIE_VGA AK30 PCIE_REFCLKP
9 CLK_PCIE_VGA# AK32 PCIE_REFCLKN
3,9,26,28,29,31,32,41 PLTRST# AL27 PERSTB
PCIE_CALRN AA22 PCIE_CALRN 2.0K R62
PCIE_CALRP Y22 PCIE_CALRP 1.27K R51
(1.1V)
+PCIE_VDDC
3 PCIE_MRX_GTX_P[0..15]
3 PCIE_MRX_GTX_N[0..15]
PCIE_MRX_GTX_P0 0.1U C87 16 PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1 0.1U C94 16 PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2 0.1U C92 16 PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3 0.1U C88 16 PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4 0.1U C100 16 PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5 0.1U C103 16 PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6 0.1U C108 16 PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7 0.1U C115 16 PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8 0.1U C131 16 PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9 0.1U C148 16 PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10 0.1U C136 16 PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11 0.1U C167 16 PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12 0.1U C140 16 PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13 0.1U C180 16 PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14 0.1U C150 16 PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15 0.1U C168 16 PCIE_MRX_GTX_C_P15
PCIE_MRX_GTX_N0 0.1U C90 16 PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1 0.1U C96 16 PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2 0.1U C95 16 PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3 0.1U C91 16 PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4 0.1U C105 16 PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5 0.1U C107 16 PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6 0.1U C114 16 PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7 0.1U C128 16 PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8 0.1U C118 16 PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9 0.1U C159 16 PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10 0.1U C142 16 PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11 0.1U C181 16 PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12 0.1U C147 16 PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13 0.1U C166 16 PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14 0.1U C160 16 PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15 0.1U C182 16 PCIE_MRX_GTX_C_N15
M92-S2 XT AJ072800T04 100-CG1675(216-0728004)
M92-S2 AJ072800T03 100-CG1643(216-0728003)
QUANTA COMPUTER
Title
VGA-M92-XT (PCIe)
Size
Document Number
FM9
Rev
1A
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MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB		0	0	0
256MB		0	0	1
64MB		0	1	0
512MB		1	0	0

GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	FM9 setting
GPIO0	GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable) 0 : Default. (Driver Controlled Gen2) 1 : Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO_5_AC_BATT 0 : Battery saving mode = 0.0 V 1 : AC (Performance mode) = 3.3 V	0
GPIO6	ATI Internal use only	0

Memory Straps	RAM_TYPE _CFG2	RAM_TYPE _CFG1	RAM_TYPE _CFG0	Quanta PN (QuantaBuy)	Quanta PN (WinBuy)	Vendor PN	31 level PN
800MHz 512MB(64M*16) Samsung	0	0	1	AKD5LGGT502		K4W1G1646E-HC12	
800MHz 512MB(64M*16) Hynix	0	1	0	AKD5LZGTW00		H5TQ1G63BFR-12C	

Spread Spectrum

If U4, the discrete spread spectrum chip is not used, then pop R48 in order to pull-down BXTALOUT for EMI reasons.

	S0
-1.75% (DOWN)	0

DIS only

Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

AVDD=70mA max

VDD1DI=45mA max

A2VDD=65mA max

A2VDDQ=1mA max

Keep A2VSSQ away from noisy ground.

VDD2DI=40mA max

Place very close to ASIC balls

As M82 design, for GPIO use

M92-S2/M92-XT

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layout note: close to VDDR1#[1:17]

VDDR1#[1..17]=2A max

(PCIE_VDDC 1.0~1.1V +/- 5%@ 2A)

+1.5V_RUN

C173 0.01U, C207 0.01U, C204 0.01U, C191 0.01U, C192 0.01U, C198 0.1U, C188 0.1U, C205 0.1U, C193 0.1U

C201 1U, C185 1U, C199 1U, C179 1U, C200 1U, C186 0.1U

C254 10U, C255 10U, C158 10U

U32D

PART 4 OF 10

POWER

VDDR1#1 H13, VDDR1#2 H16, VDDR1#3 H19, VDDR1#4 J10, VDDR1#5 J23, VDDR1#6 J24, VDDR1#7 J9, VDDR1#8 K10, VDDR1#9 K23, VDDR1#10 K24, VDDR1#11 K9, VDDR1#12 L11, VDDR1#13 L12, VDDR1#14 L13, VDDR1#15 L20, VDDR1#16 L21, VDDR1#17 L22

PCIE_VDDR#[1..8]=500mA max

+1.8V_RUN_GFX

C99 1U, C119 0.1U, C135 1U, C132 0.01U, C102 10U

PCIE_VDDR#1 AB23, PCIE_VDDR#2 AC23, PCIE_VDDR#3 AD24, PCIE_VDDR#4 AE24, PCIE_VDDR#5 AE25, PCIE_VDDR#6 AE26, PCIE_VDDR#7 AF25, PCIE_VDDR#8 AG26

(1.1V)

+PCIE_VDDC

PCIE_VDDC#[1..12]=2A max

C85 1U, C73 1U, C59 1U, C176 1U, C50 1U, C86 1U, C177 1U, C42 10U

PCIE_VDDC#1 L23, PCIE_VDDC#2 L24, PCIE_VDDC#3 L25, PCIE_VDDC#4 L26, PCIE_VDDC#5 M22, PCIE_VDDC#6 N22, PCIE_VDDC#7 N23, PCIE_VDDC#8 N24, PCIE_VDDC#9 P22, PCIE_VDDC#10 T22, PCIE_VDDC#11 U22, PCIE_VDDC#12 V22

+1.1V_GFX_PCIE

L12 BLM18PG121SN1D

C40 10U 603 6.3, C68 1U 402 6.3, C54 0.1U 16

C41 10U 603 6.3, C45 1U 402 6.3, C79 0.1U 16

+1.8V_RUN_GFX

L17 BLM15BD121SN1D

VDD_CT#[1..4]=110mA max

+VDD_CT

C46 10U, C49 0.1U, C58 1U, C72 1U, C83 0.1U

VDD_CT#1 AA20, VDD_CT#2 AA21, VDD_CT#3 AB20, VDD_CT#4 AB21

+3.3V_DELAY

VDDR3#[1..4]=50mA max

C113 1U, C556 1U, C577 0.1U, C125 0.1U

VDDR3#1 AA17, VDDR3#2 AA18, VDDR3#3 AB17, VDDR3#4 AB18

+1.8V_RUN_GFX

R53 *150/F_NC

VDDR4#[1..4] & VDDR5#[1..4]=340mA max

R57 0, R54 0

VDDR4#1 AA11, VDDR4#2 AA12, VDDR4#3 Y11, VDDR4#4 Y12

C137 1U, C130 0.1U, C146 1U, C120 0.1U

R66 0, R64 0

VDDR5#1 U11, VDDR5#2 U12, VDDR5#3 V11, VDDR5#4 V12

For M92-S2: Install R147,R148,R149
Use R150 0R to VDDR4
M93-S3 and Park: Remove R147,R148,R149
Use R45 150 Ohms Pull Down

+1.5V_RUN

L56 BLM15BD121SN1D

+VDDRH1

C609 1U, C608 1U

VDDRHA L17

VSSRHA L16

(0.9~1.2V)

+VCC_GFX_CORE

VDDC#[2..3]=120mA max

+BBP

C172 0.1U, C163 1U

VDDC#1 AA15, VDDC#2 M11, VDDC#3 M12, VDDC#4 N15, VDDC#5 N17, VDDC#6 R13, VDDC#7 R16, VDDC#8 R18, VDDC#9 R21, VDDC#10 T12, VDDC#11 T15, VDDC#12 T17, VDDC#13 T20, VDDC#14 U13, VDDC#15 U16, VDDC#16 U18, VDDC#17 U21, VDDC#18 V15, VDDC#19 V17, VDDC#20 V20, VDDC#21 V21, VDDC#22 Y13, VDDC#23 Y16, VDDC#24 Y18, VDDC#25 Y21

DDCI=2A max

+VDDCI

(0.9~1.2V)

VDDCI#1 M13, VDDCI#2 M15, VDDCI#3 M16, VDDCI#4 M17, VDDCI#5 M18, VDDCI#6 M20, VDDCI#7 M21, VDDCI#8 N20

M92-S2/M92-XT

U32E

PART 5 OF 10

GND

PCIE_VSS#1 AA27, PCIE_VSS#2 AB24, PCIE_VSS#3 AB32, PCIE_VSS#4 AC24, PCIE_VSS#5 AC26, PCIE_VSS#6 AC27, PCIE_VSS#7 AD25, PCIE_VSS#8 AD32, PCIE_VSS#9 AE27, PCIE_VSS#10 AF32, PCIE_VSS#11 AG27, PCIE_VSS#12 AH32, PCIE_VSS#13 K28, PCIE_VSS#14 K32, PCIE_VSS#15 L27, PCIE_VSS#16 M32, PCIE_VSS#17 N25, PCIE_VSS#18 N27, PCIE_VSS#19 P25, PCIE_VSS#20 P32, PCIE_VSS#21 R27, PCIE_VSS#22 T25, PCIE_VSS#23 T32, PCIE_VSS#24 U25, PCIE_VSS#25 U27, PCIE_VSS#26 V32, PCIE_VSS#27 W25, PCIE_VSS#28 W26, PCIE_VSS#29 W27, PCIE_VSS#30 Y25, PCIE_VSS#31 Y32

GND#1 A3, GND#2 A30, GND#3 AA13, GND#4 AA16, GND#5 AB10, GND#6 AB15, GND#7 AB6, GND#8 AC9, GND#9 AD6, GND#10 AD8, GND#11 AE7, GND#12 AG12, GND#13 AH10, GND#14 AH28, GND#15 B10, GND#16 B12, GND#17 B14, GND#18 B16, GND#19 B18, GND#20 B20, GND#21 B22, GND#22 B24, GND#23 B26, GND#24 B6, GND#25 B8, GND#26 C1, GND#27 C32, GND#28 E28, GND#29 F10, GND#30 F12, GND#31 F14, GND#32 F16

GND#33 F18, GND#34 F2, GND#35 F20, GND#36 F22, GND#37 F24, GND#38 F26, GND#39 F6, GND#40 F8, GND#41 G10, GND#42 G27, GND#43 G31, GND#44 G8, GND#45 H14, GND#46 H17, GND#47 H2, GND#48 H20, GND#49 H6, GND#50 J27, GND#51 J31, GND#52 K11, GND#53 K2, GND#54 K22, GND#55 K6, GND#56 M6, GND#57 N11, GND#58 N12, GND#59 N13, GND#60 N16, GND#61 N18, GND#62 N21, GND#63 P6, GND#64 P9, GND#65 R12, GND#66 R15, GND#67 R17, GND#68 R20, GND#69 T13, GND#70 T16, GND#71 T18, GND#72 T21, GND#73 T6, GND#74 U15, GND#75 U17, GND#76 U20, GND#77 U3, GND#78 U9, GND#79 V13, GND#80 V16, GND#81 V18, GND#82 V8, GND#83 Y10, GND#84 Y15, GND#85 Y17, GND#86 Y20, GND#87 Y6, GND#88 T11, GND#89 R11

VSS_MECH#1 A32, VSS_MECH#2 AM1, VSS_MECH#3 AM32

M92-S2/M92-XT

+BBP

Q18 SI2301BDS-T-GE3

C152 1U 402 6.3

+1.8V_RUN_GFX

Q20 2N7002W-7-F

(0.9~1.2V)

+VCC_GFX_CORE

R63 100K

+5V_RUN

17 BB_ENA

Q19 2N7002W-7-F

R67 10K

layout note: close to VDDC#[1:25]

(0.9~1.2V)

+VCC_GFX_CORE

C178 1U, C141 1U, C122 1U, C133 1U, C154 1U

C153 1U, C110 1U, C109 1U, C121 1U, C145 1U, C124 1U, C139 1U, C134 1U

(0.9~1.2V)

+VCC_GFX_CORE

C138 10U, C116 10U, C117 10U

(0.9~1.2V)

+VCC_GFX_CORE

(0.9~1.2V)

+VDDCI

L25 BLM18EG221SN1D

C157 0.1U, C156 0.1U, C165 1U, C155 1U, C161 10U

QUANTA COMPUTER

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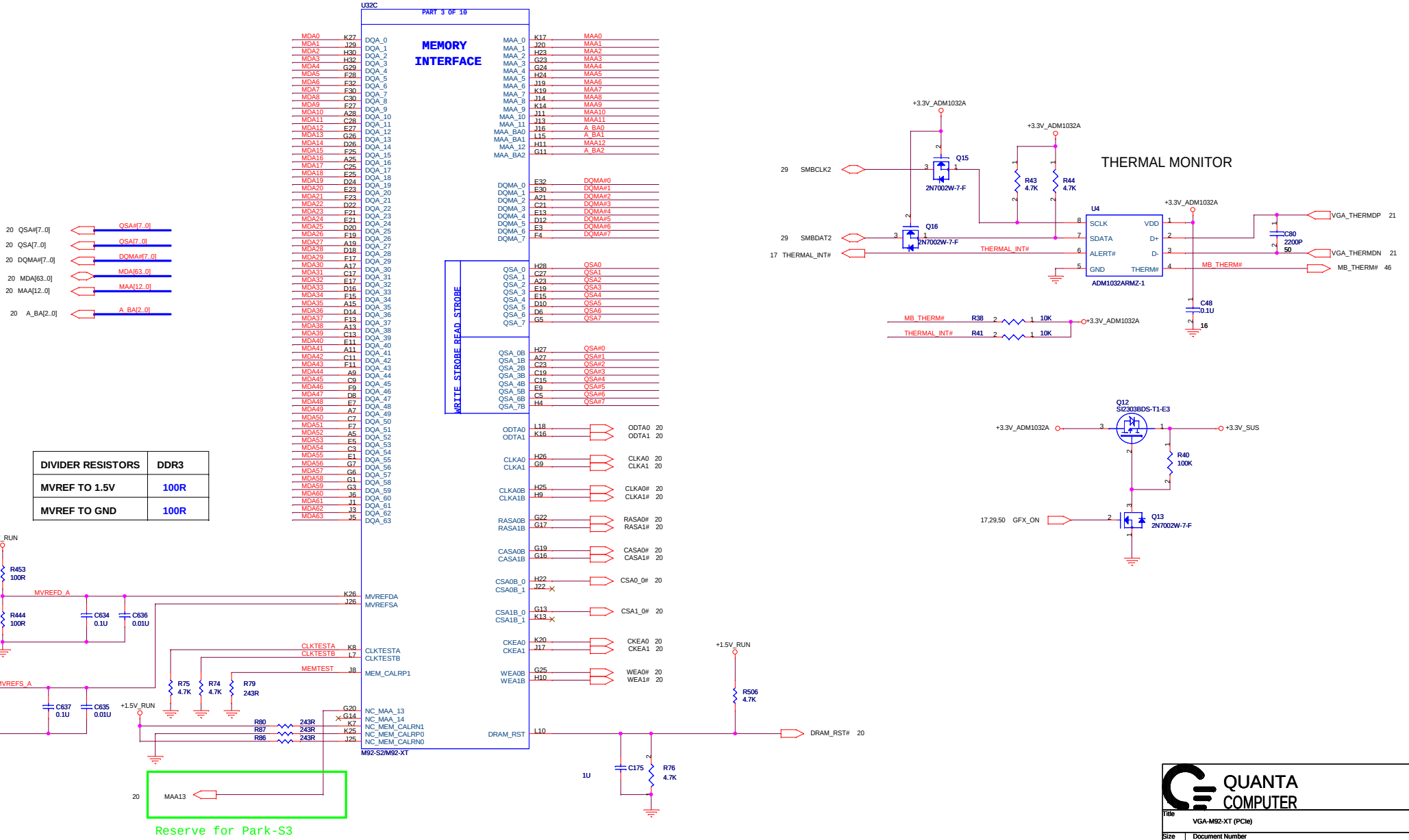
MEMORY INTERFACE



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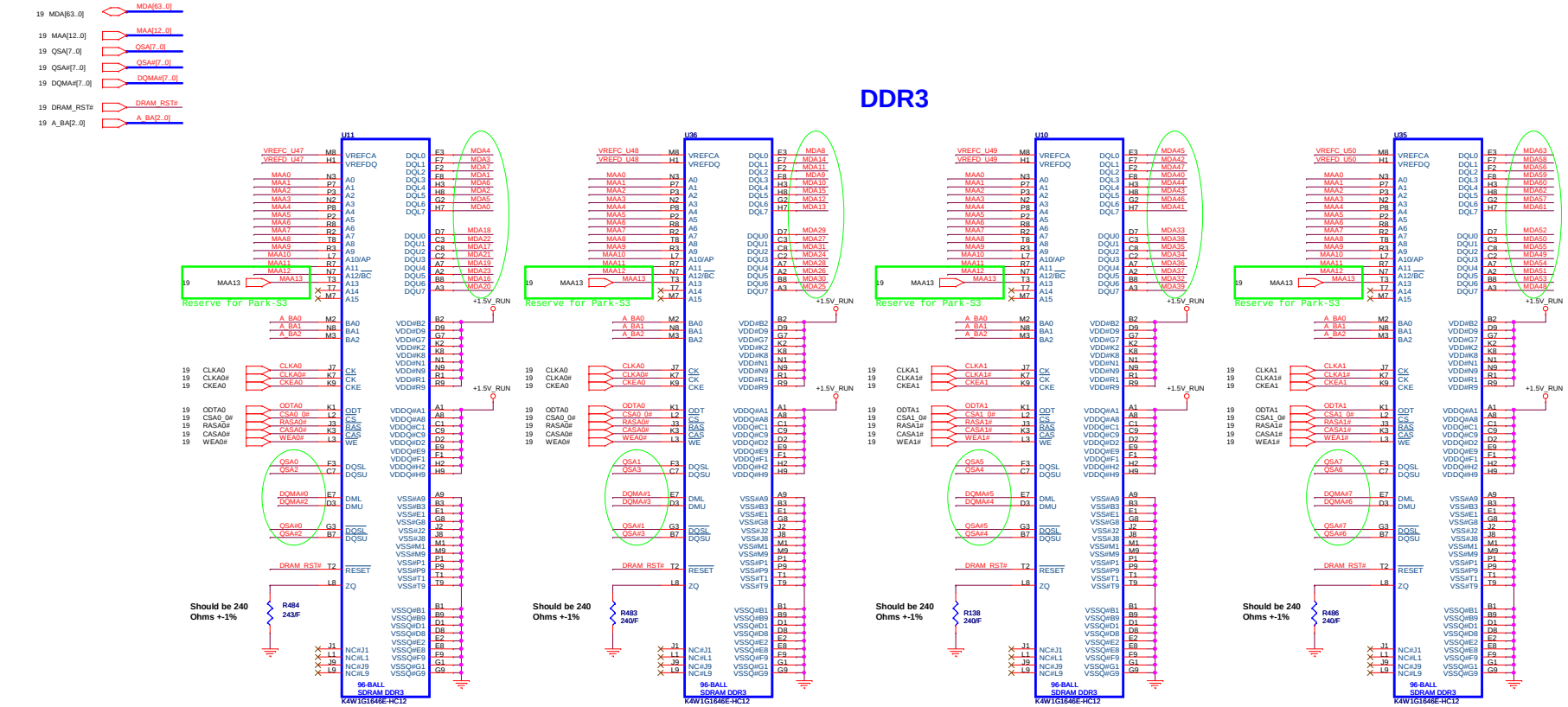
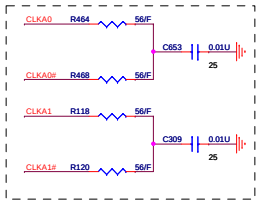
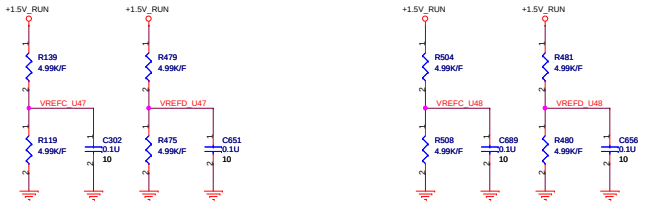
DDR3

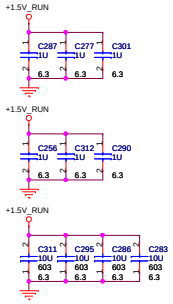


Placement has to be close to VRAM

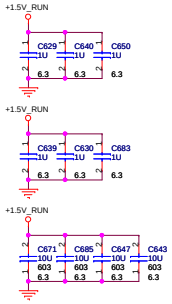




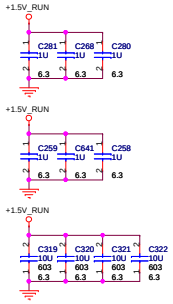
close to U47



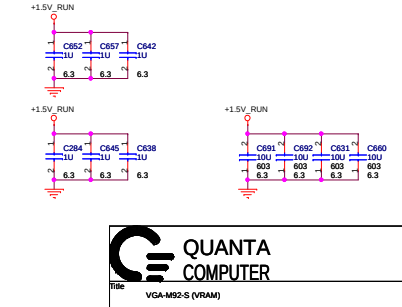
close to U48



close to U49



close to U50



QUANTA COMPUTER		
Title: VGA-M92-S (VRAM)		
Size	Document Number: FM9	Rev: 1A
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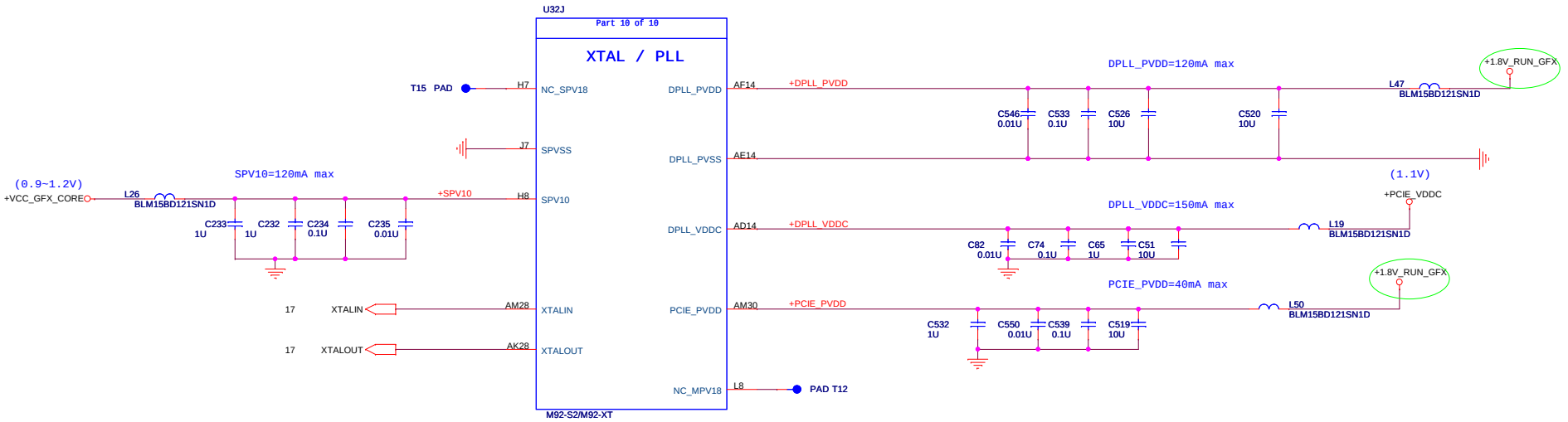
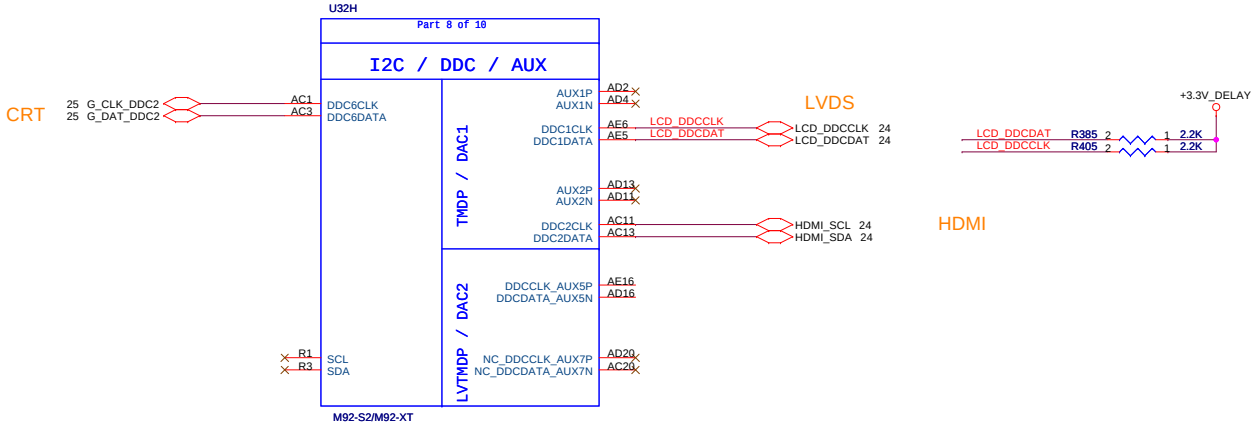
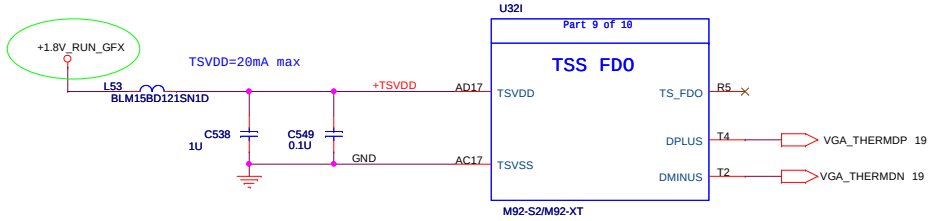


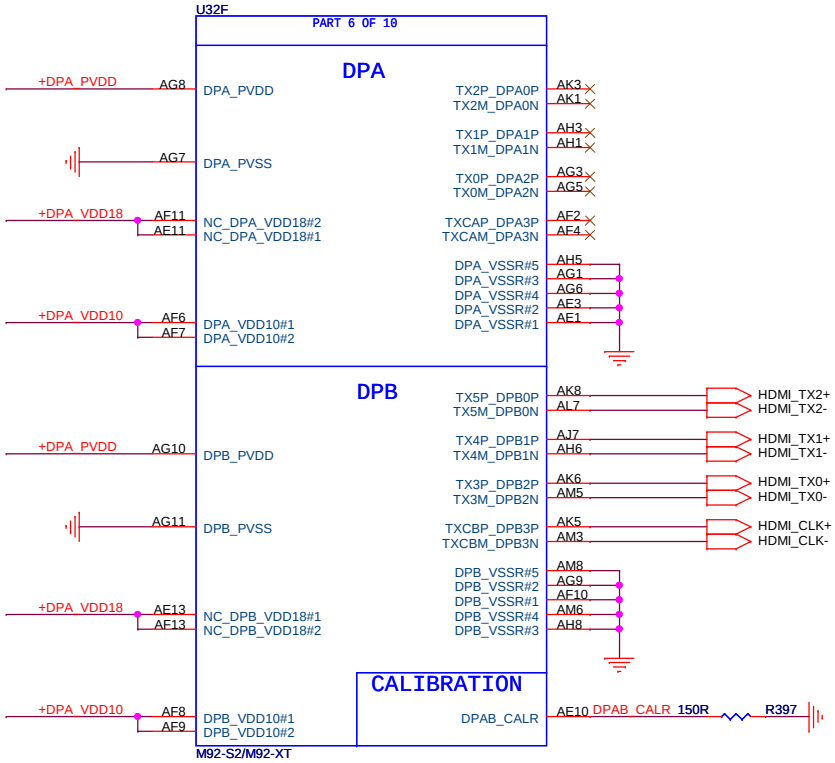




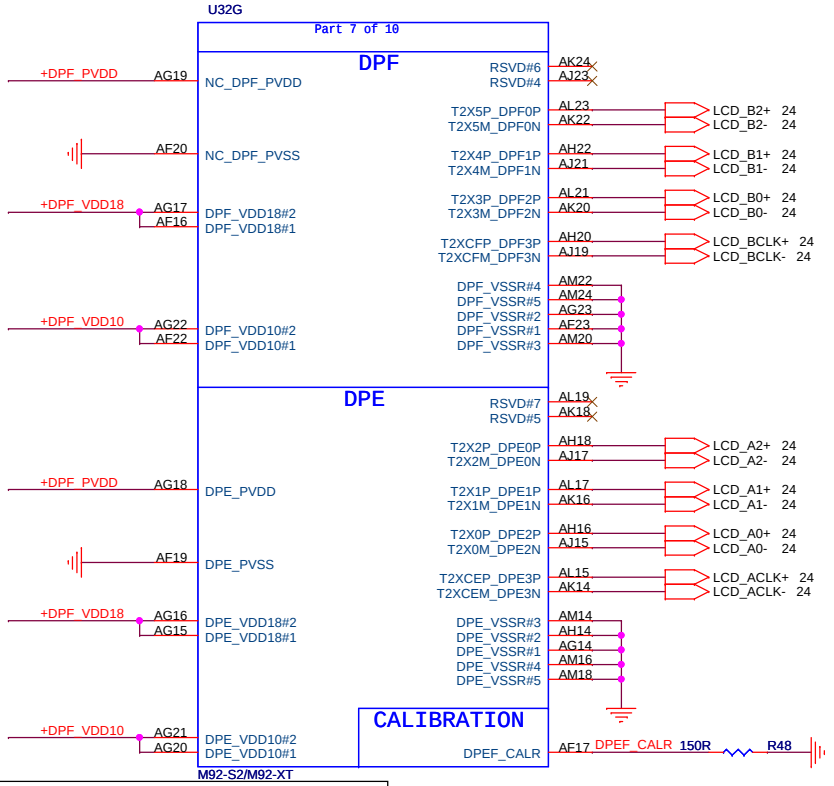
QUANTA COMPUTER

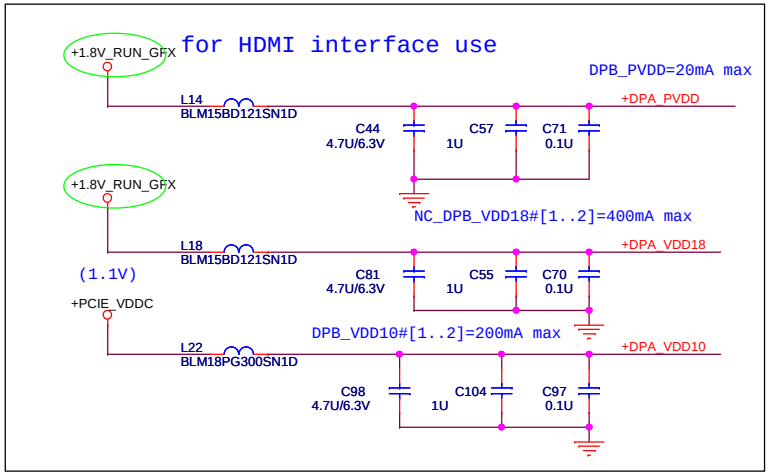
Title	VGA-M92-XT (PCIe)	
Size	Document Number FM9	Rev 1A
Date: Wednesday, March 04, 2009	Sheet 21 of 64	

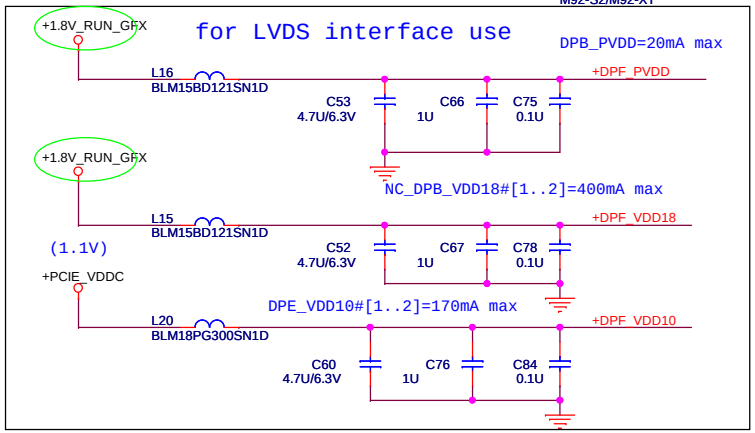
TMDP(HDMI) INTERFACE



LVDS INTERFACE







QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
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QUANTA COMPUTER

Title	VGA-M82-S (PCIe)	
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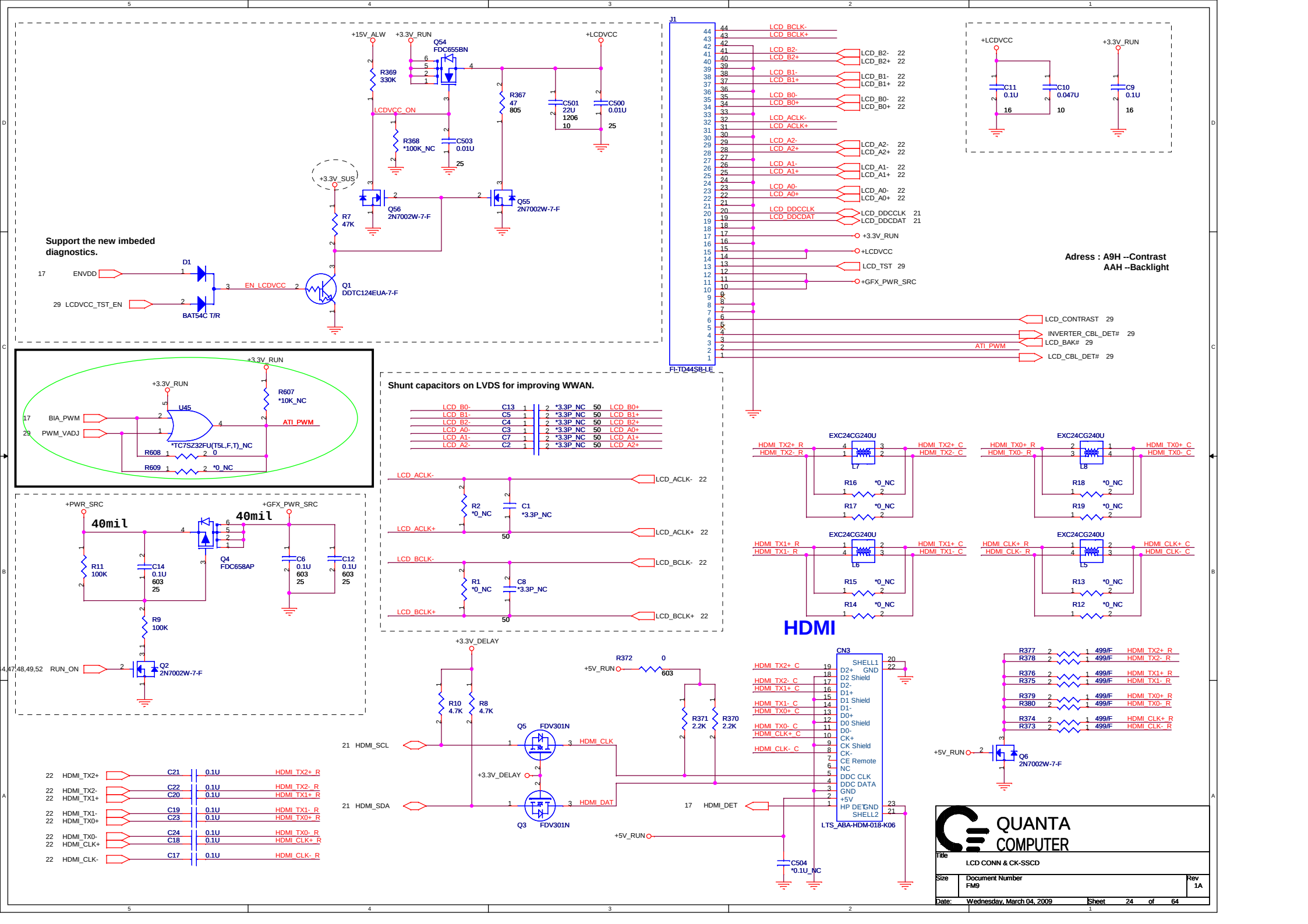
Support the new imbeded diagnostics.
Adress : A9H --Contrast
AAH --Backlight
Shunt capacitors on LVDS for improving WWAN.
HDMI
40mil
40mil
LTS_ABA-HDM-018-K06
FI-TD44SB-LE
QUANTA COMPUTER
Title
LCD CONN & CK-SSCD
Size
Document Number
FM9
Rev
1A
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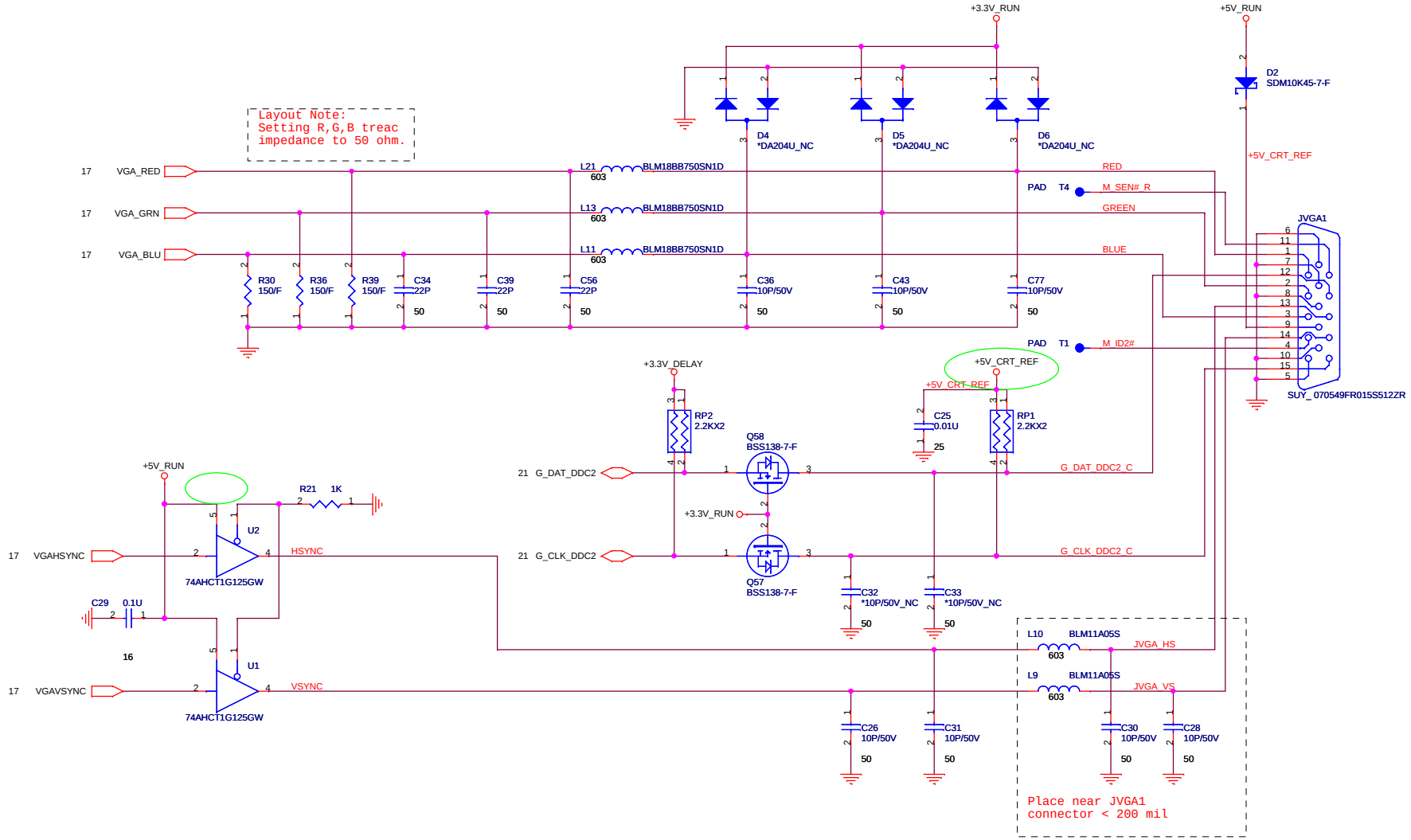
64



QUANTA COMPUTER

Title	CRT&TV CONN	
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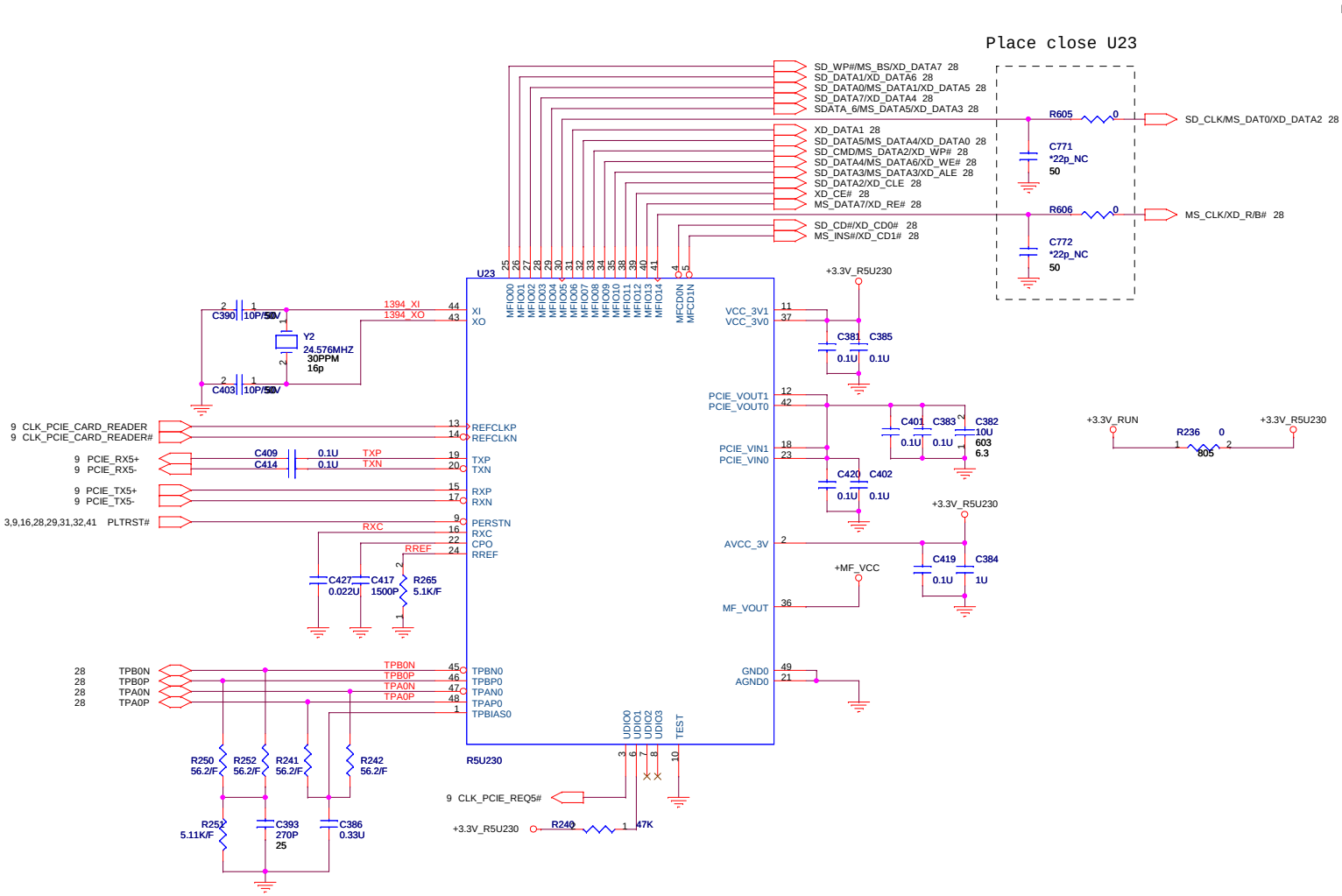

MFIO Pin Assignment Table

MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	**CLK**	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	**CLK**	R/B#

QUANTA COMPUTER

Title	5 IN 1 CONTROLLER	
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QUANTA COMPUTER

Title	IEEE 1394	
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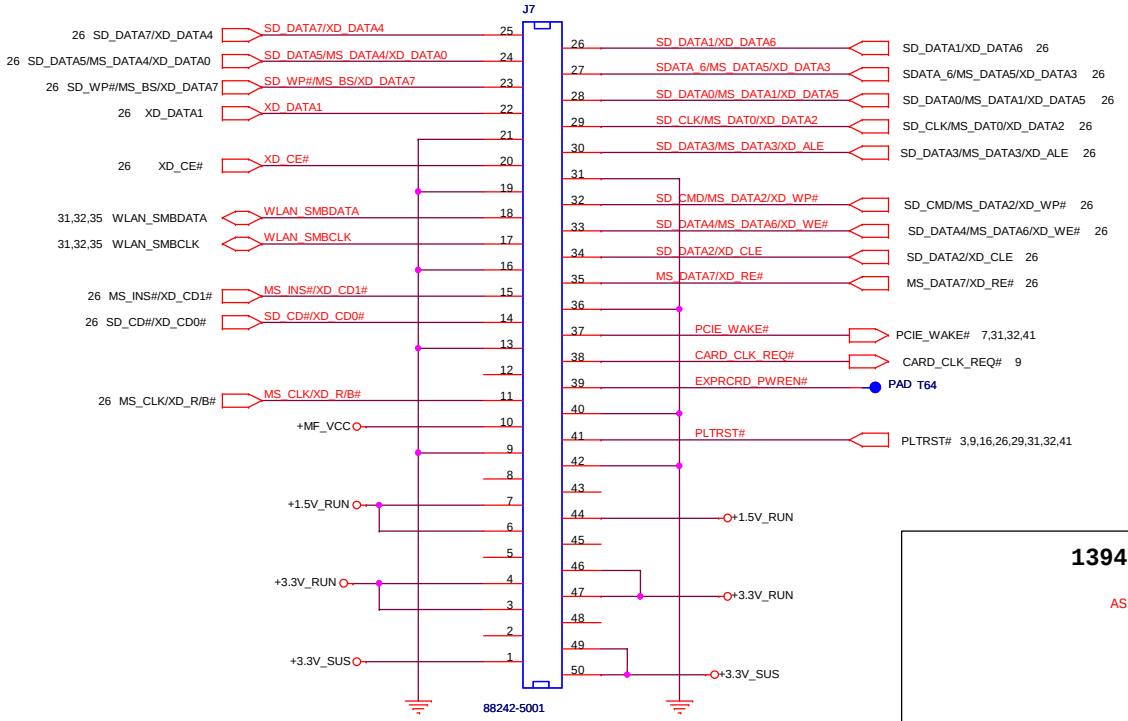
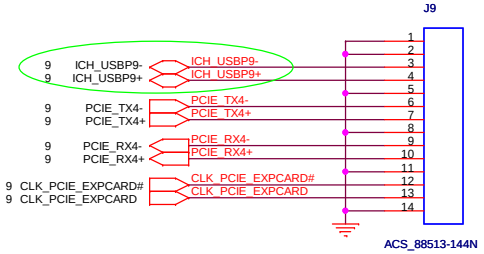
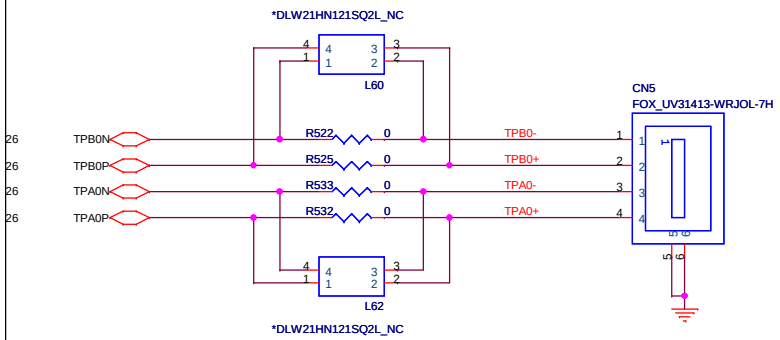
Express Card/CARD READER





1394 CONNECTOR

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.



*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.

QUANTA COMPUTER

Title	ExpressCard/SmartCard	
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ITE8502E LQFP-128L

U22

KEYBOARD

KSO0/PD0, KSO1/PD1, KSO2/PD2, KSO3/PD3, KSO4/PD4, KSO5/PD5, KSO6/PD6, KSO7/PD7, KSO8/ACK, KSO9/BUSY, KSO10/PE, KSO11/ERR, KSO12/SLCT, KSO13, KSO14, KSO15, KSO16/GPC3, KSO17/GPC5

KSI0/STB, KSI1/AFD, KSI2/INT, KSI3/SLIN, KSI4, KSI5, KSI6, KSI7

ADC/DAC

ADC0/GPI0 HWPG
ADC1/GPI1 IMVP6_PROCHOT# 51
ADC2/GPI2 SUS_PWR_ACK 7
ADC3/GPI3 LCD_CBL_DET# 24
ADC4/GPI4 INVERTER_CBL_DET# 24
ADC5/GPI5 PBAT_PRES# 53
ADC6/GPI6 IINP 45
ADC7/GPI7 SIO_SLP_S5# 7

DAC0/GPJ0 CRIT_TEMP_REP# 10
DAC1/GPJ1 SIO_EXT_WAKE# 10
DAC2/GPJ2 USBP1_SIDE_EN# 33
DAC3/GPJ3 LAN_PCIE_PWR_CTRL 10,41
DAC4/GPJ4 ICH_RSMRST# 7
DAC5/GPJ5 SIO_PWRBTN# 7

PWM

PWM0/GPA0 BREATH_LED# 37
PWM1/GPA1 BAT2_LED# 37
PWM2/GPA2 FAN1_PWM 38
PWM3/GPA3 PWM_VADJ 24
PWM4/GPA4 BAT1_LED# 37
PWM5/GPA5 KB_BACKLITE_EN 36
PWM6/GPA6 USBP0_BUS_SW_CB 33
PWM7/GPA7 BEEP 39

TACH0/GPD6 FAN1_TACH 38
TACH1/GPD7 PANEL_BKEN 17

TMRI0/WUI2/GPC4 LID_SW# 36
TMRI1/WUI3/GPC6 SIO_SLP_S3# 7

LPC

LPCRST/WUI4/GPD2
LPCCLK
LFRAME
LAD0
LAD1
LAD2
LAD3
CLKRUN/GPH0/ID0
SERIRQ
ECSMI/GPD4
ECSCI/GPD3
GA20/GPB5
LPCPD/WUI6/GPE6
KBRST/GPB6
WRST
PWUREQ/GPC7
L80HLAT/GPE0
L80LLAT/WUI7/GPE7

IR/UART

RXD/GPB0 LCD_CONTRAST1
TXD/GPB1 PAD T24
GPC0
CTX0/GPB2 RUN_ON_1 42
CRX1/GPH1/ID1 HDDC_EN 35
CTX1/GPH2/ID2 IMVP_VR_ON IMVP_VR_ON 51

SMBUS

SMCLK0/GPB3
SMDAT0/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
SMCLK2/GPF6
SMDAT2/GPF7

LPC/FWH FLASH

FLFRAME/GPG2/LF SUS_ON SUS_ON 47,52
FLRST/GPG0/TM KB_DET# 36
FLAD3/GPG6
FLAD2/SO EC_FLASH_SPI_DO 30
FLAD1/SI EC_FLASH_SPI_DIN 30
FLAD0/SCE EC_FLASH_SPI_CS# 30
FLCLK EC_FLASH_SPI_CLK 30

PS/2

PS2CLK0/GPF0
PS2DAT0/GPF1
PS2CLK1/GPF2
PS2DAT1/GPF3
PS2CLK2/GPF4
PS2DAT2/GPF5

EGPC

EGAD/GPE1 PCH_PWRGD PCH_PWRGD 7
EGCS/GPE2 ALW_ON 37,46
EGCLK/GPE3 GFX_ON 17,19,50

GPIO

GPH3/ID3 USBP0_SIDE_EN# USBP0_SIDE_EN# 33
GPH4/ID4 USB_BACK_EN# USB_BACK_EN# 34
GPH5/ID5 BID1
GPH6/ID6 CHIPSET_ID1
GPG1/ID7 MODC_EN 35

RI1/WUI0/GPD0 SATA_ACT# 8
RI2/WUI1/GPD1 ACAV_IN 37,45
WUI5/GPE5 PCB_BEEP_EN 39
RING/PWRFAIL/LPCRST/GPB7 AC_PRESENT 7
PWRSW/GPE4 SYS_PWR_SW# 37
GINT/GPD5 LCDVCC_TST_EN 24

ITE8512_XTAL1
ITE8512_XTAL2
ITE8512IX_JX
CK32K
CK32KE
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7
AVCC
AVSS

ITE8502E
lqfp128-16x16-4-nb1

VBAT1 3 +RTC_CELL
VCC 11 +3.3V_RUN
VSTBY1 26 +3.3V_ALW
VSTBY2 50
VSTBY3 92
VSTBY4 114
VSTBY5 121
VSTBY6 127

R534 0 +RTC_CELL
C710 0.1U 16

51 IMVP_PWRGD

+3.3V_ALW
C342 10U 603 6.3 16
C368 0.1U 16
C713 0.1U 16
C364 0.1U 16
C316 0.1U 16
Place these caps close to ITE8502.

SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

3,9,16,26,28,31,32,41 PLTRST#
9 CLK_PCI_8512
8,32 LPC_LFRAME#
8,32 LPC_LAD0
8,32 LPC_LAD1
8,32 LPC_LAD2
8,32 LPC_LAD3
R521 1 2 0

7 CLKRUN#
8 IRQ_SERIRQ
10 SIO_EXT_SMI#
10 SIO_EXT_SCI#
10 SIO_A20GATE
24 LCD_TST
10 SIO_RCIN#
24 LCD_BAK#
D10 D8 D12 D21 SDMK0340L-7-F
WRST#

39 NB_MUTE#
ICH_AZ_CODEC_RST0# R519 0

Charge and BAT
CLK, LCD and Thermal
G_Thermal and Media button

38,45,53 SMBCLK0
38,45,53 SMBDAT0
9 SMBCLK1
9 SMBDAT1
19 SMBCLK2
19 SMBDAT2

T22 PAD
37 USB_CHG_DET#_R
USB_CHG_DET#_R
53 PS_ID
T23 PAD
36 CLK_TP_SIO
36 DAT_TP_SIO

+3.3V_ALW
D22 SDMK0340L-7-F
38,46 THERM_STP#
R527 100K
C707 1U 603 10

+3.3V_ALW
L59 BLM11A05S 603
C705 0.1U 16
L61 603 BLM11A05S

32KHz Clock.
W1
ITE8512_XTAL1
ITE8512_XTAL2
C714 18P/50V 50
32.768KHZ
C712 18P/50V 50

CLK_PCI_8512
R203 10
C352 2.2P 50

ITE8512IX_JX
C361 0.1U 16

+3.3V_RUN
R227 *10K_NC
R219 *0_NC
LCD_CONTRAST1
LCD_CONTRAST 24

SMBDAT0 SMBCLK0 RP4 2.2KX2
SMBDAT1 SMBCLK1 RP5 10KX2
SMBDAT2 SMBCLK2 RP6 2.2KX2
USBP1_SIDE_EN# R198 10K

PCH_PWRGD R526 1K
SUS_ON R536 100K
HWPG R180 100K
IMVP_VR_ON R215 *100K_NC

+3.3V_RUN
LCD_CBL_DET# R192 10K
INVERTER_CBL_DET# R194 10K
IRQ_SERIRQ R529 10K/F
LCD_BAK# R524 *10K_NC

+3.3V_SUS
SUS_PWR_ACK R183 10K
AC_PRESENT R530 10K

+3.3V_RUN
R528 100K
ICH_AZ_CODEC_RST0#
Q66 2N7002W-7-F
8,39 ICH_AZ_CODEC_RST#
R531 390K
C706 *0.1U_NC 10
Q67 MMST3904-7-F

Board ID Straps

Discrete
+3.3V_ALW
R217 10K
R226 *10K_NC
R223 *10K_NC
R222 *10K_NC
R216 *10K_NC
R225 10K
R224 10K
R221 10K
USB_BACK_EN#
BID1
CHIPSET_ID1
USBP0_SIDE_EN#
UMA

VGA_IDENTIFY

BID0

CHIPSET_ID1	BID1	USB_BACK_EN#	FM9B(UMA)	FM9 (Dis)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	QT (A00)	QT (A00)
1	0	0	(A01)	(A01)
1	0	1		

QUANTA COMPUTER

Title	Ultra I/O Controller ECE5028	
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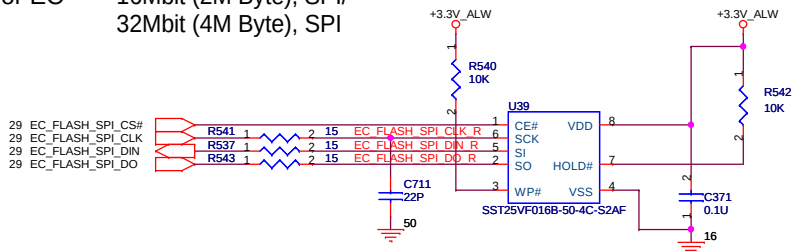
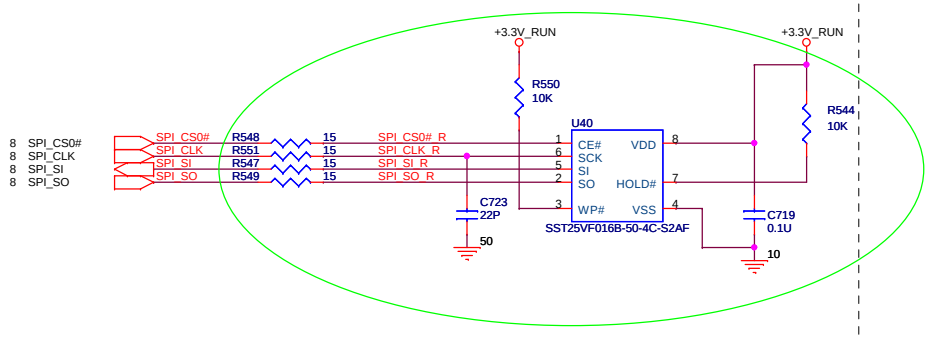
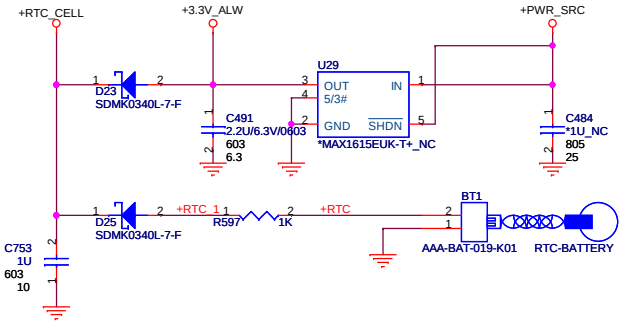
For EC 16Mbit (2M Byte), SPI/ 32Mbit (4M Byte), SPI



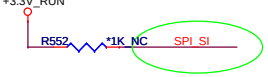
For PCH 16Mbit (2M Byte), SPI/ 32Mbit (4M Byte), SPI



RTC BATTERY



iTPM ENABLE/DISABLE



TPM Function	R712
Enable	Mount
Disable	NC (Default)

QUANTA COMPUTER

Title	Ultra I/O Controller ECE5028	
Size	Document Number FM9	Rev 1A
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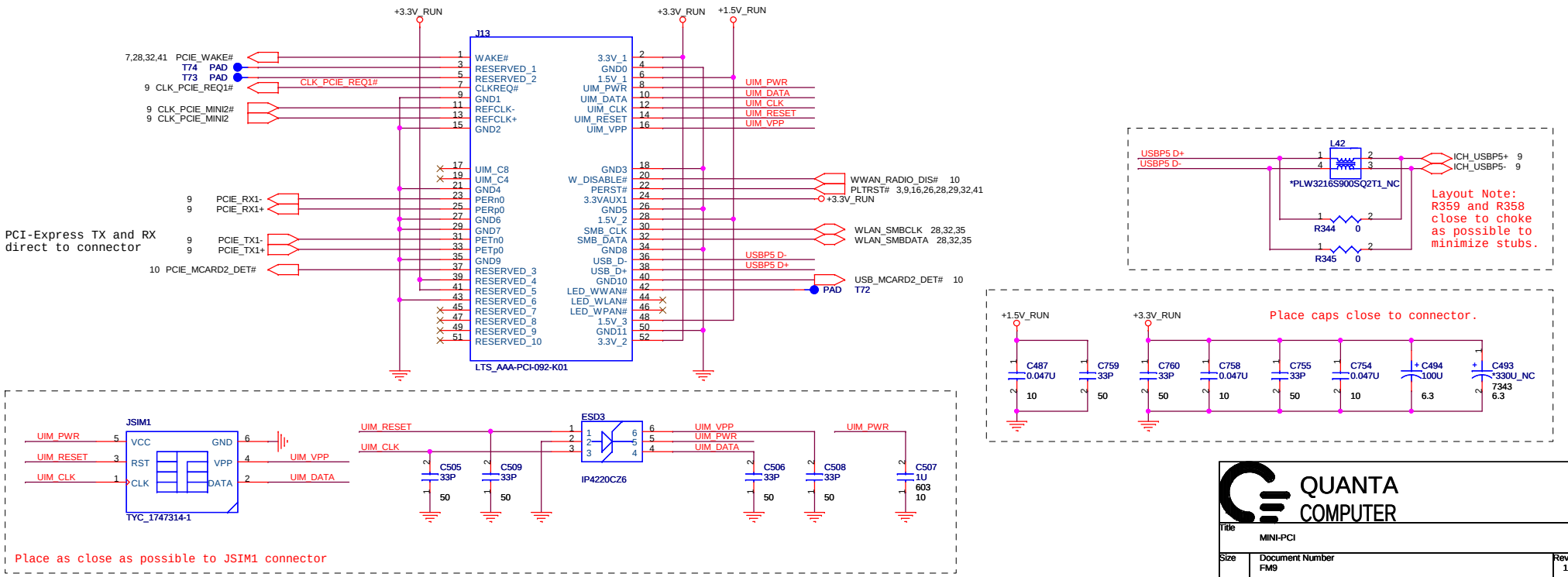
MiniCard WWAN connector



QUANTA COMPUTER

Title	MINI-PCI	
Size	Document Number FM9	Rev 1A
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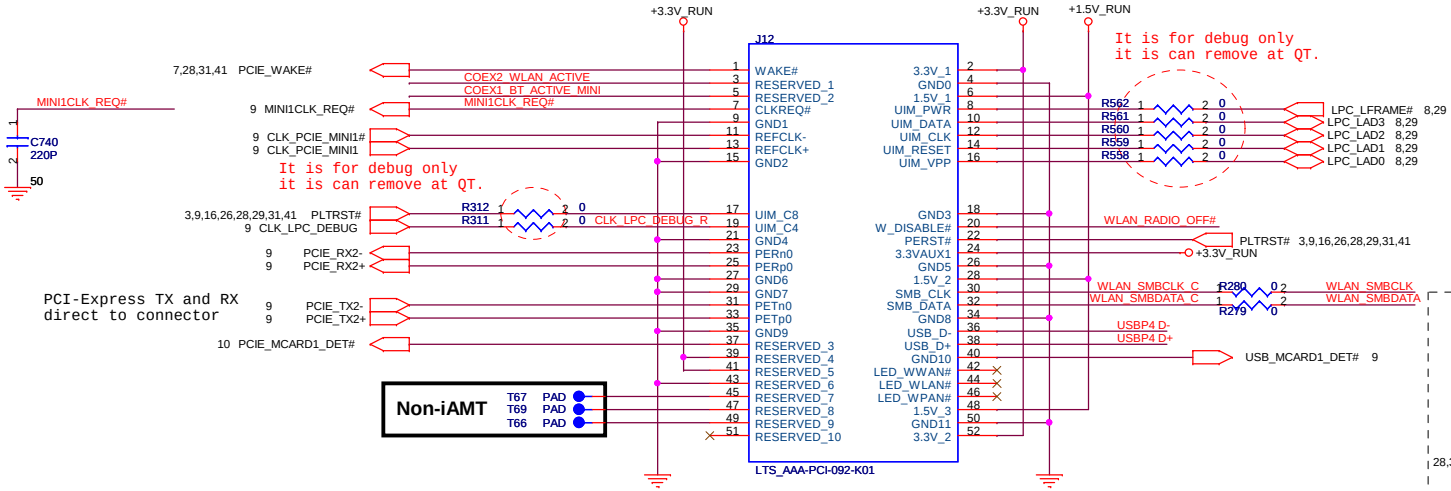
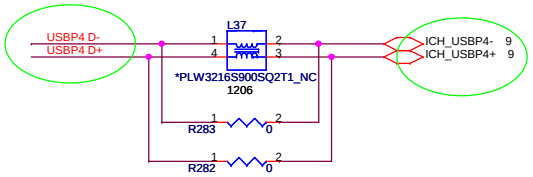
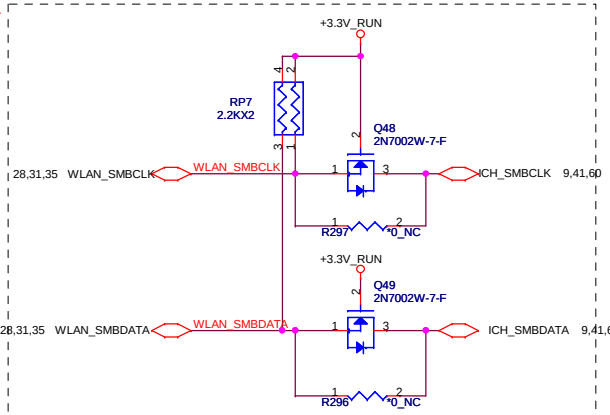
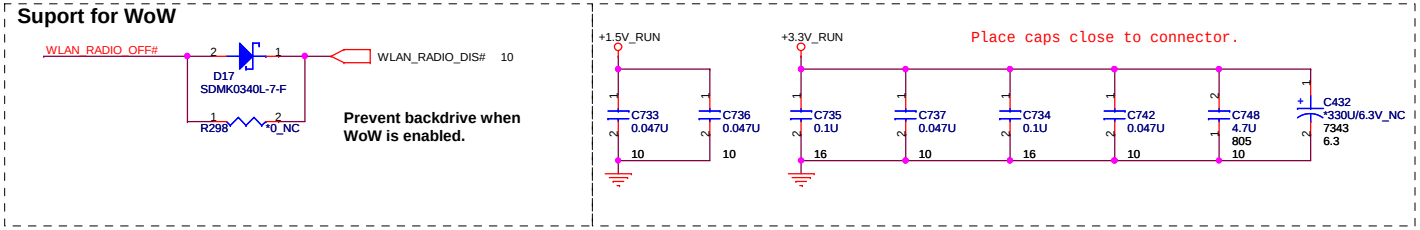
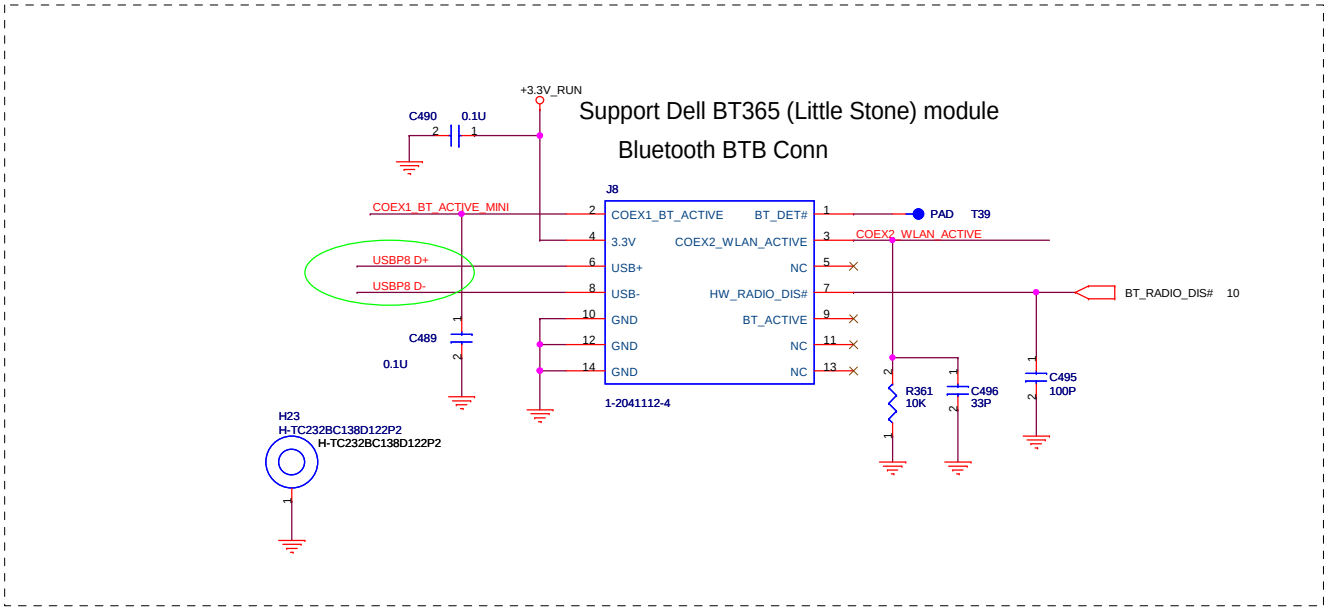
MiniCard WLAN connector

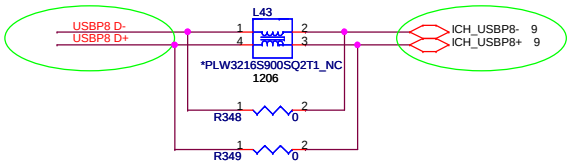












QUANTA COMPUTER

Title	MDC CONN.	
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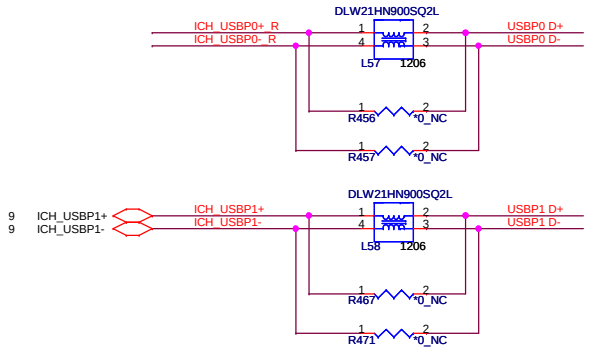
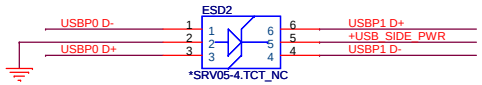
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



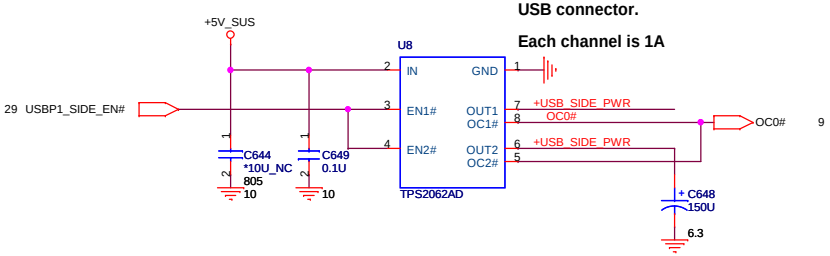
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



Place one 150uF cap by each USB connector.

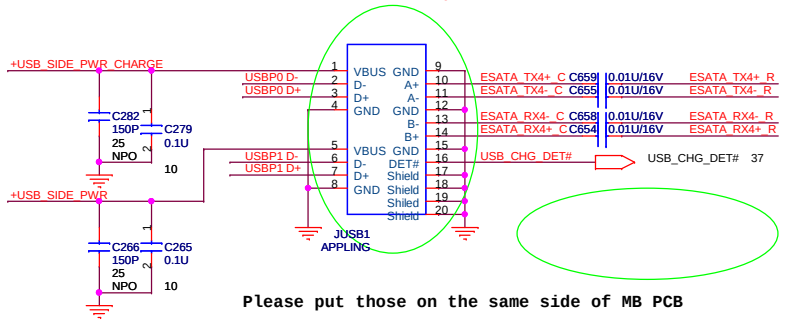
Each channel is 1A



Need to add control pin to control PUSB charge

Support USBP1 charge function.
JUSB1 need to add USB_CHG_DET# pin wire to EC GPIO to detect USB device.

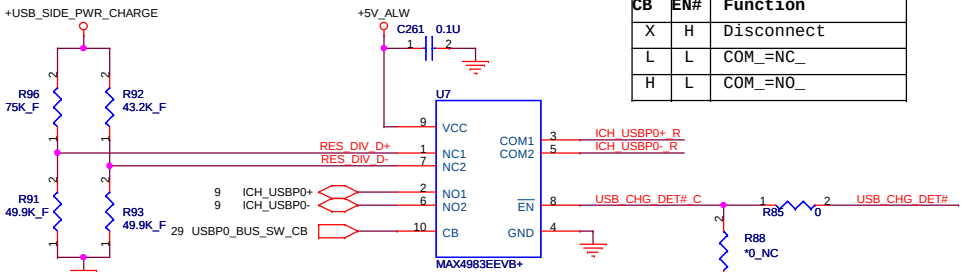
Side External USBX2
PN is old, Because New Part can't ready before SST build.



Please put those on the same side of MB PCB

USBx2 & ESATA COMBO & PWR CHARGE

USB BUS SW



CB	EN#	Function
X	H	Disconnect
L	L	COM_=NC_
H	L	COM_=NO_

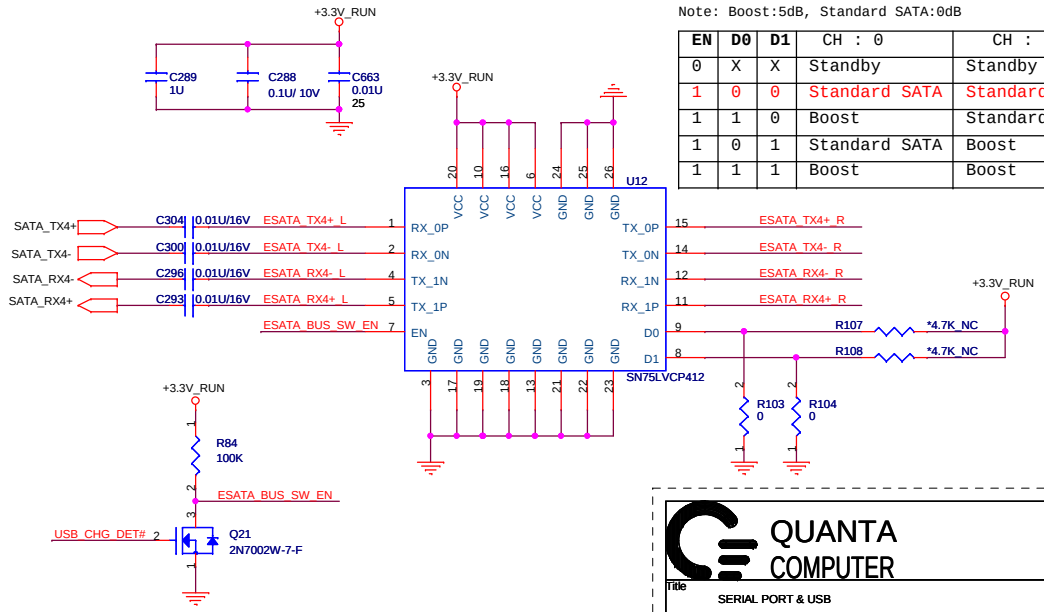
(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

E-SATA Re-driver

Please put those on the same side of MB PCB

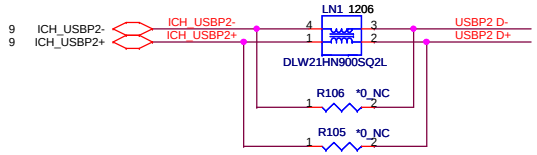
Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost



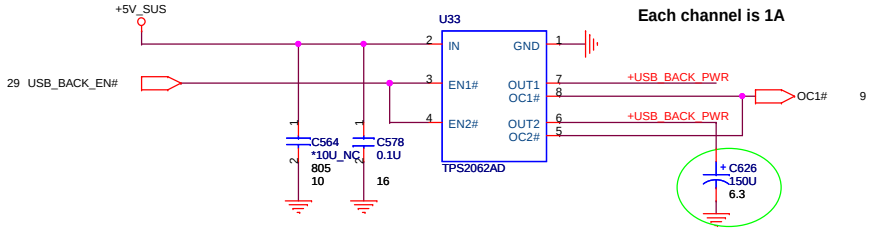
QUANTA COMPUTER

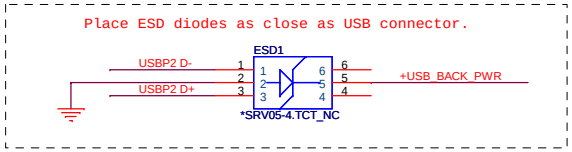
Title	SERIAL PORT & USB	
Size	Document Number FM9	Rev 1A
Date: Wednesday, March 04, 2009	Sheet 33 of 64	

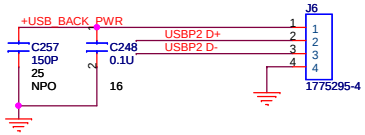


Place one 150uF cap by each USB connector.

Each channel is 1A







QUANTA COMPUTER

Title	Right USB	
Size	Document Number FM9	Rev 1A
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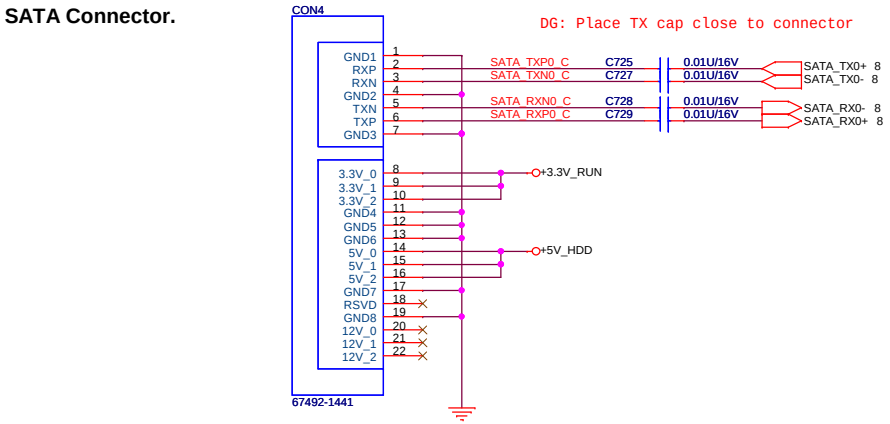
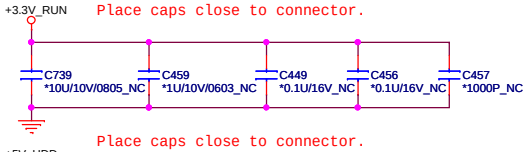
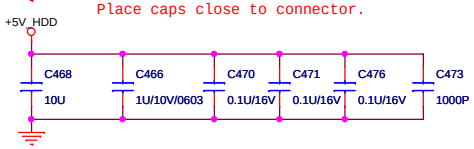
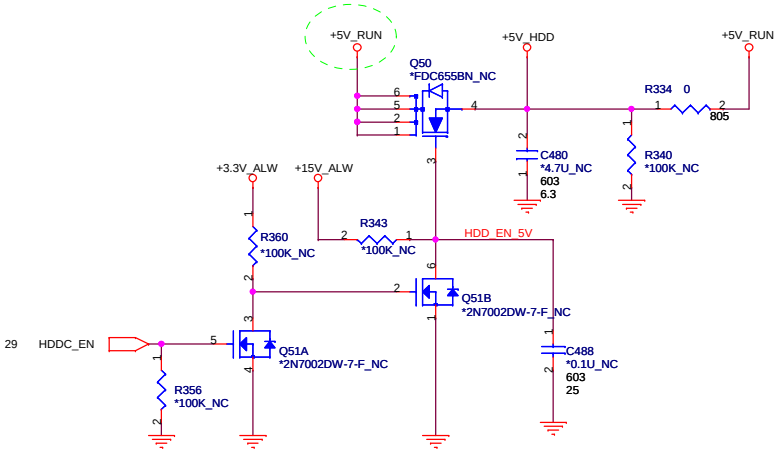
SATA Connector.

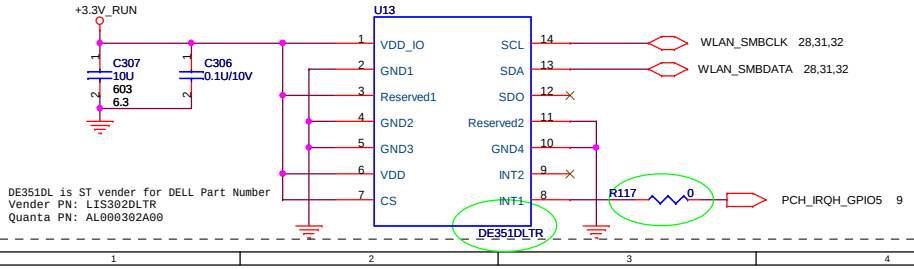




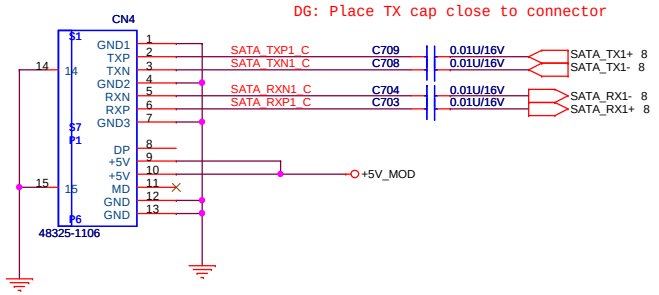


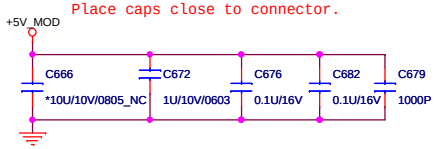


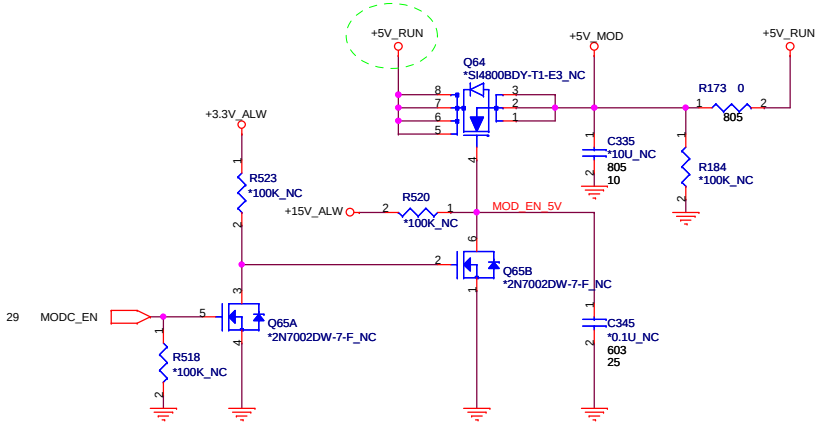
3-axis Fall Sensor (HDD data protector)



ODD Connector

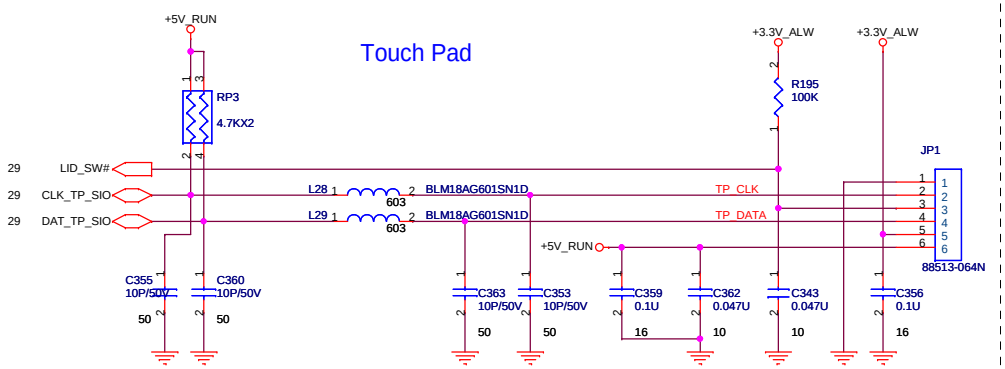




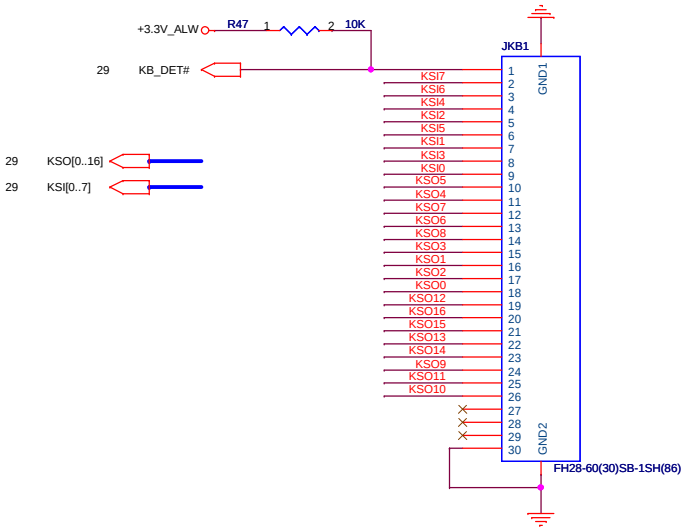


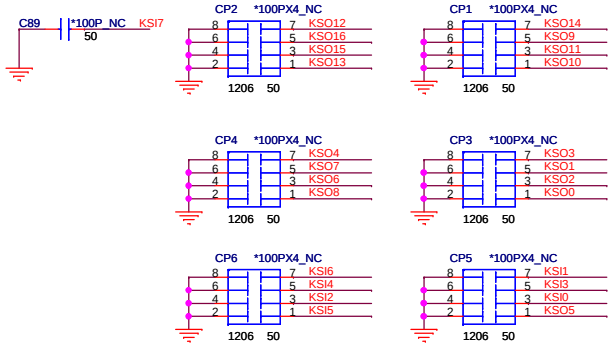
QUANTA COMPUTER		
Title: SATA (HDD&CD_ROM)		
Size	Document Number: FM9	Rev: 1A
Date: Wednesday, March 04, 2009	Sheet 35 of 64	

Touch Pad



KEYBOARD CONNECTOR

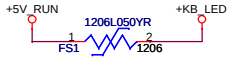


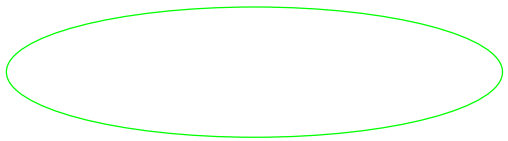


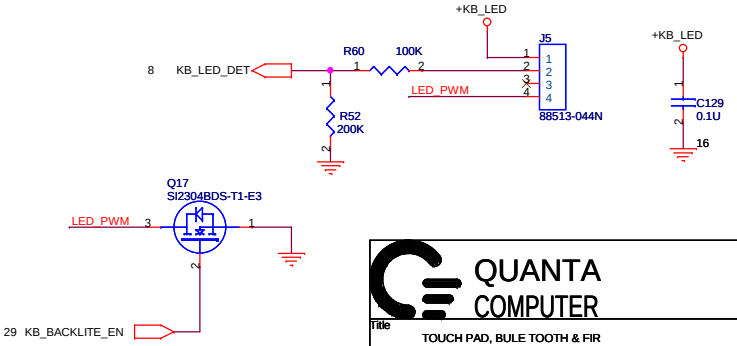
100P CAPS CLOSE TO JKB1

Key board illumination

+KB_LED power trace width >10 mil







QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
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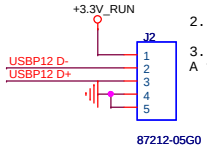
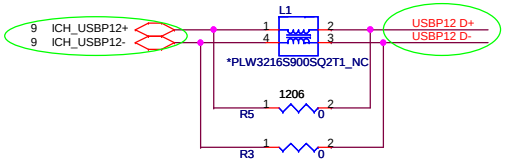
Touch Screen Module

Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
2. Maximum cable resistance on VCC, GND should be 150m ohm.
3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.

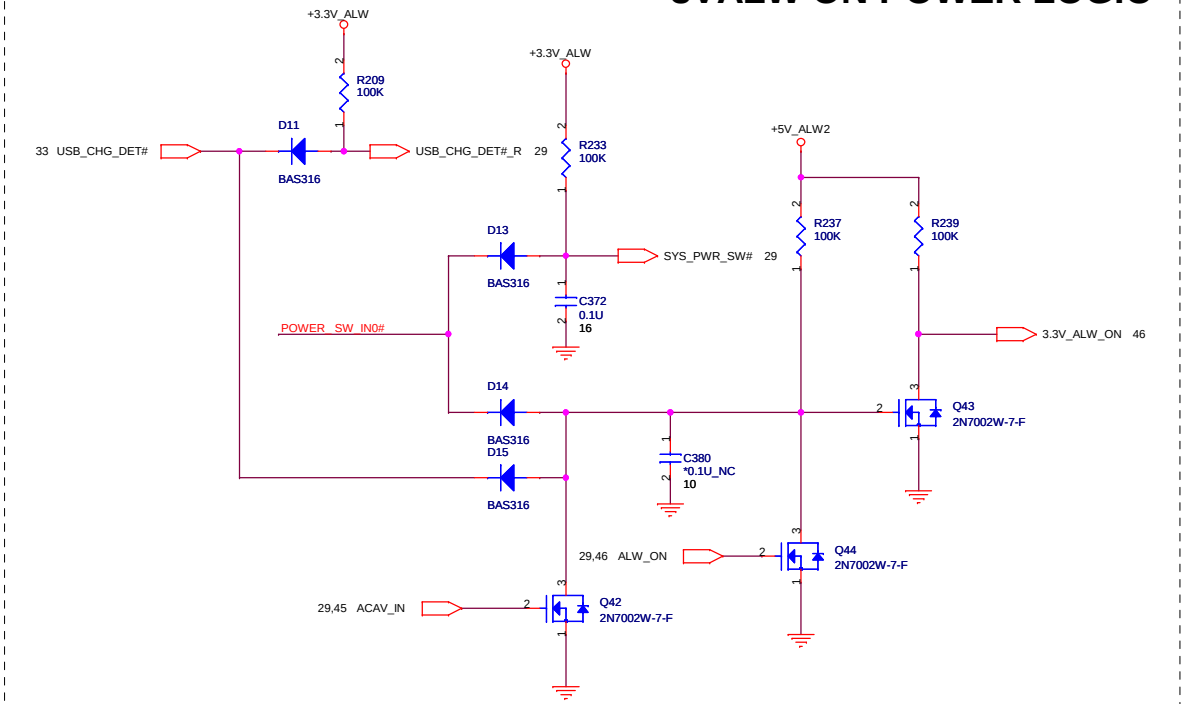


Need check the connector footprint and symble.

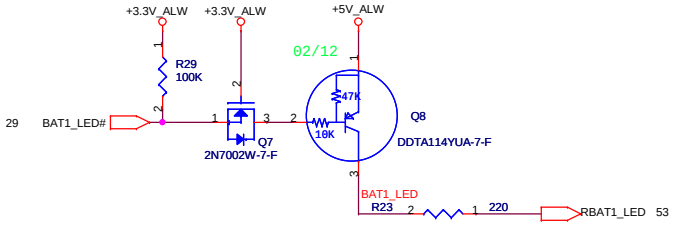


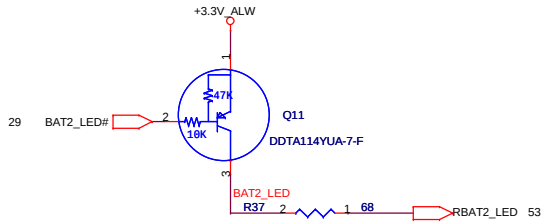
Power button Cable

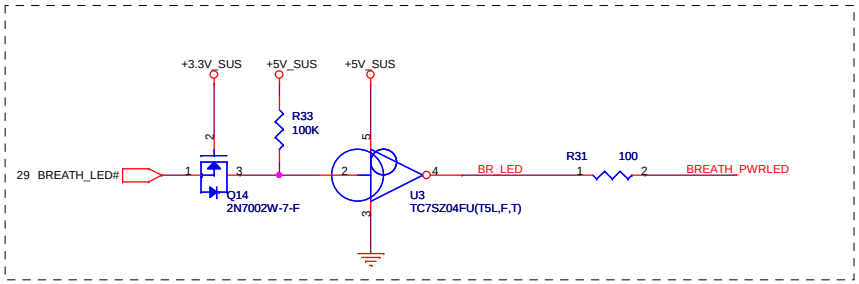
3VALW ON POWER LOGIC

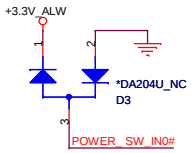


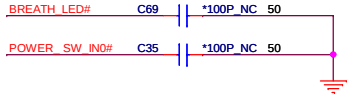
Battery status.





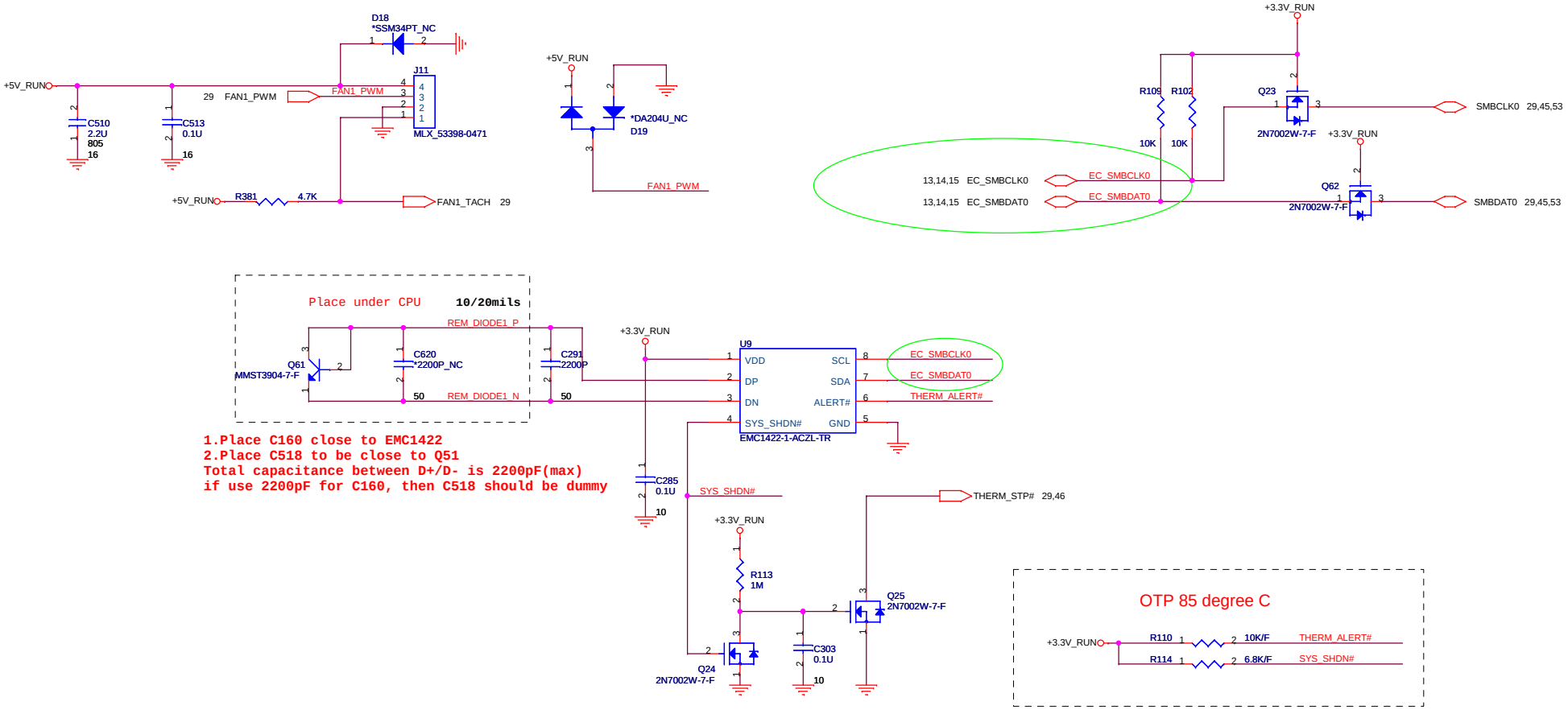






QUANTA COMPUTER

Title	SWITCH, KEYBOARD & LED&Touch Screen Module	
Size	Document Number FM9	Rev 1A
Date: Wednesday, March 04, 2009	Sheet 37 of 64	



QUANTA COMPUTER

Title	FAN & THERMAL	
Size	Document Number FM9	Rev 1A
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GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

EAPD#	NB_MUTE#	TEST_WOOFER_EN	AUD_SPK ENABLE#	SUB_MUTE#
0	0	0	H	L
0	0	1	H	L
0	1	0	H	L
0	1	1	H	L
1	0	0	H	L
1	0	1	H (Disable SPK)	H (Test Woofer)
1	1	0	L (Test SPK)	L (Disable Woofer)
1	1	1	L	H

INTERNAL SPEAKER AMP

TPA6040A4
QFN 32PIN

AZALIA (HD) CODEC

92HD73C

Layout Note: Place close U18 pin 23.

Layout Note: Close to U18 Pin 34

Layout Note: Close to U19 Pin 13

Layout Note: Place close to pin 18.

Layout Note: Place close U18.

Layout Note: Place close to pin 8.

Depop R479,C699 for using 92HD73C

Depop R477,R478,R484,R473
Pop R476,R480,R483,R475
for using 92HD73C
R476,R483 close to U19, Let DVDD width be 10-mils

Close to U19

Check it is ok at ST, if it is ok then remove it.

FB_60ohm+-25%_100MHz _3A_0.05ohm DC

Title	Azelia CODEC
Size	Document Number FM9
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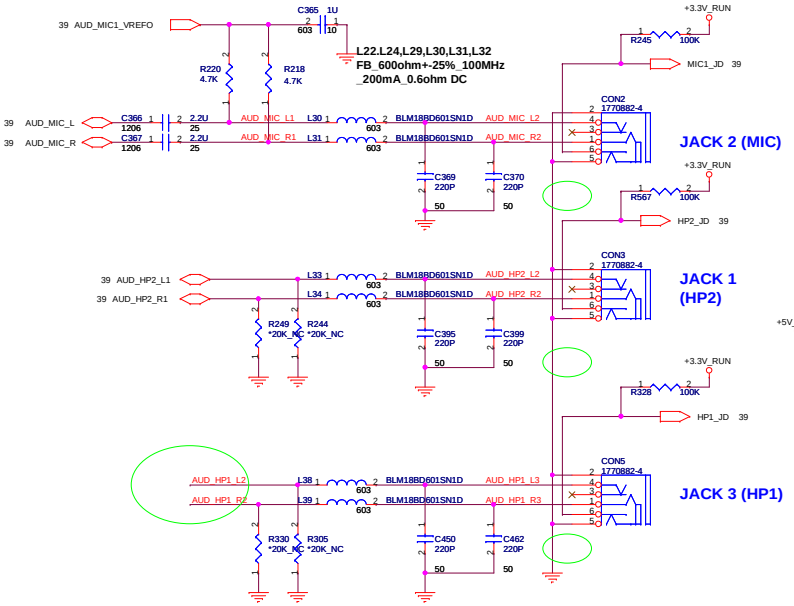
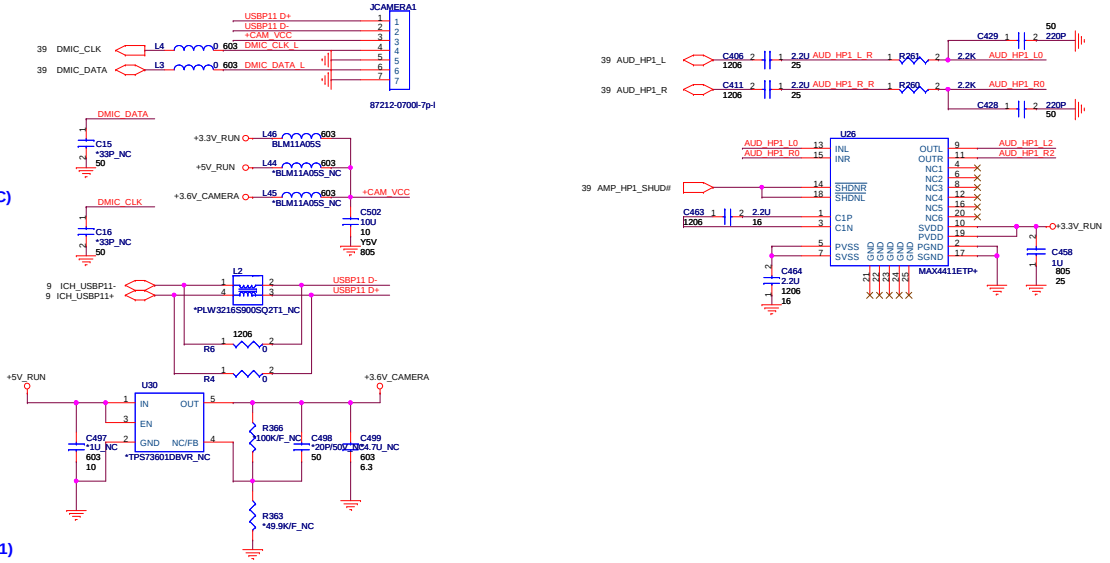
QUANTA COMPUTER

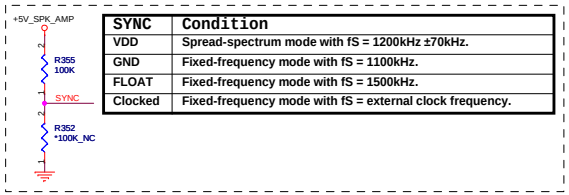
Headphone Jack
Stereo MIC Jack



Array Microphone & Camera

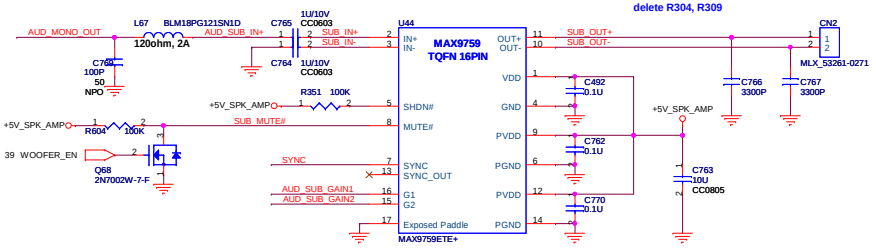


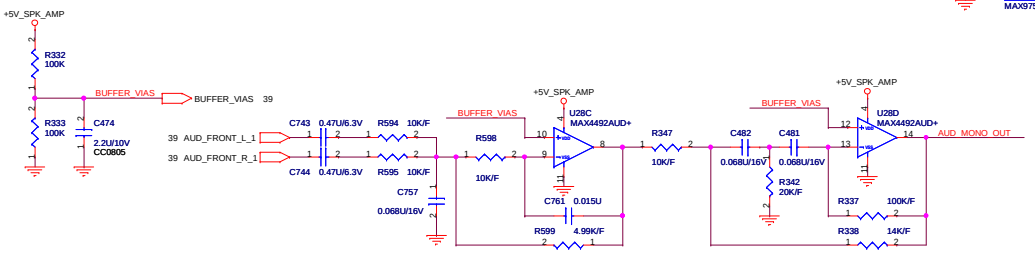
INTERNAL SUBWOOFER AMP

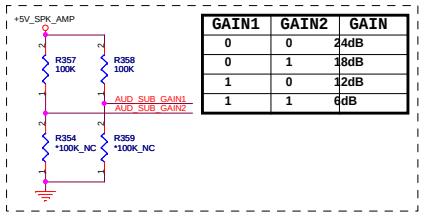


SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.

Gur_0808: 0 ohm removal, delete R304, R309







GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB

QUANTA COMPUTER

Title	AUDIO CONN	
Size	Document Number FM9	Rev 1A
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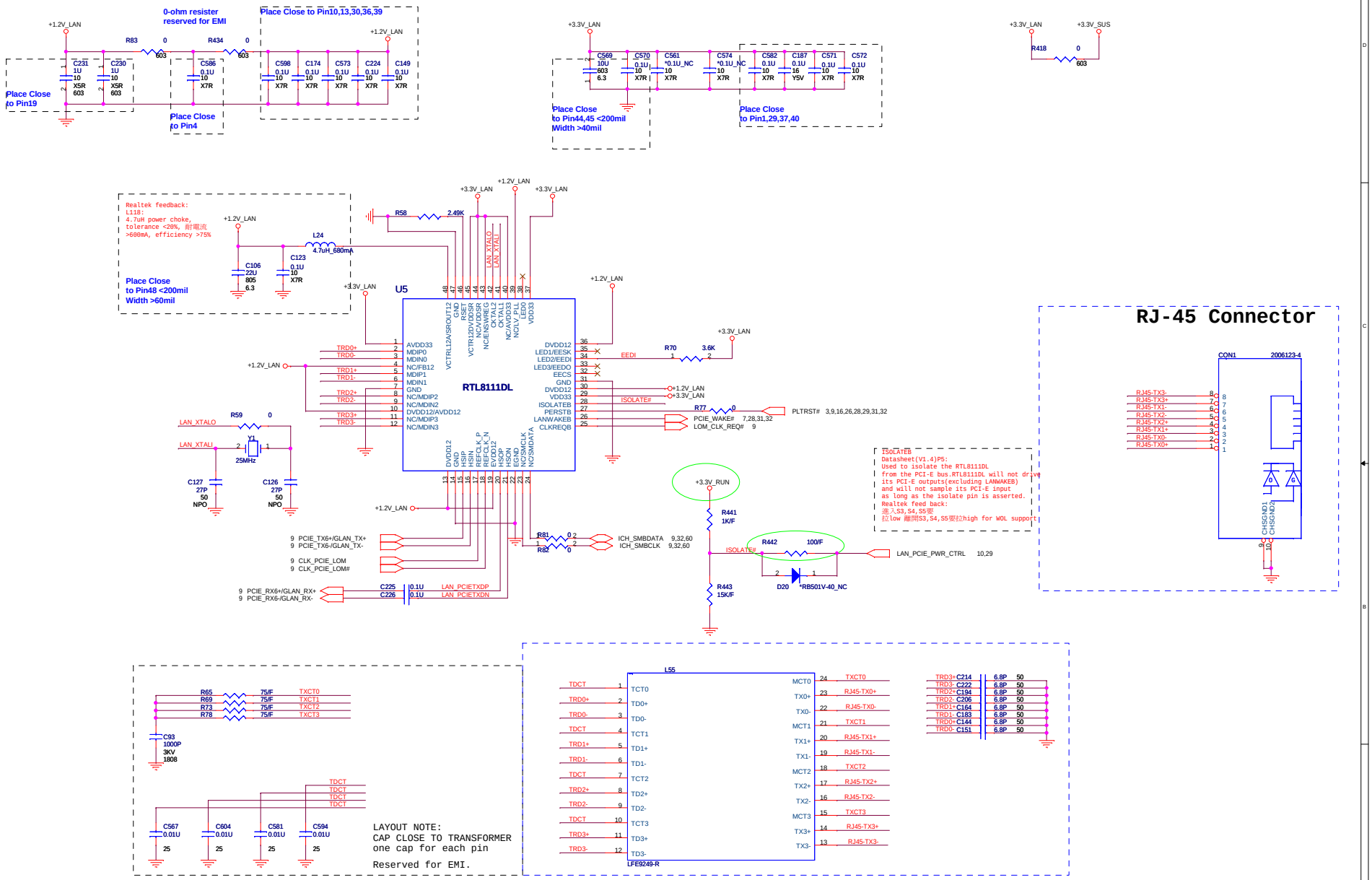
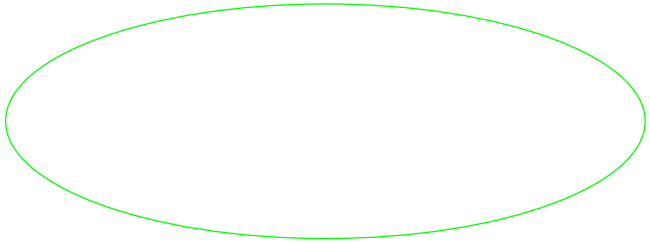
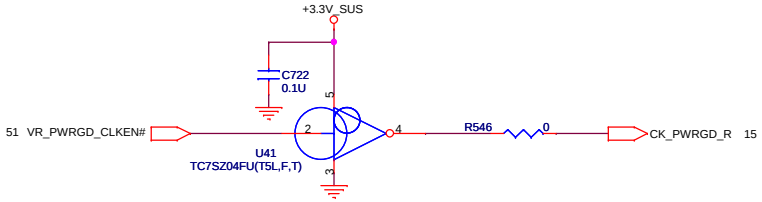
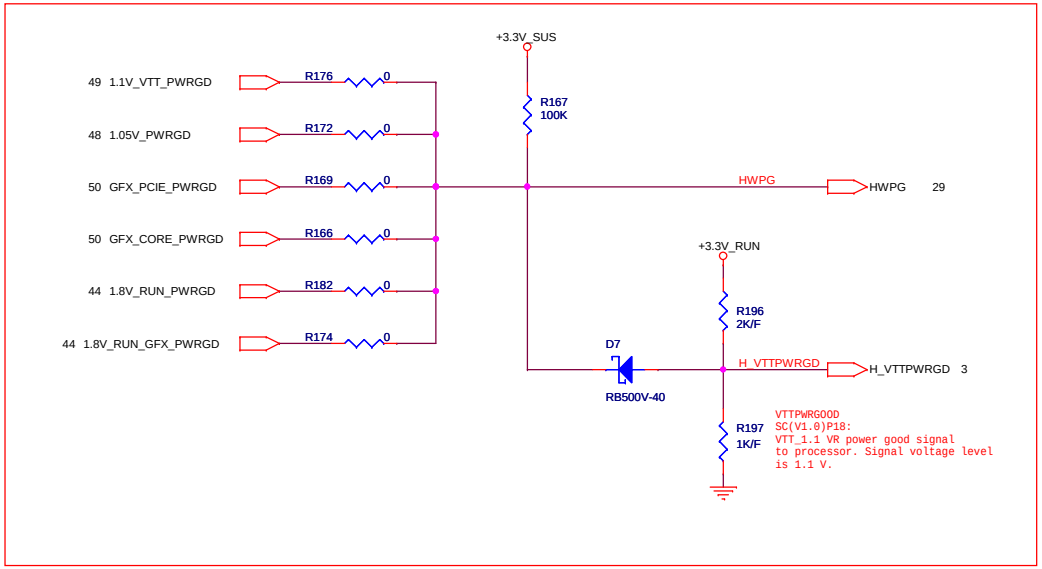
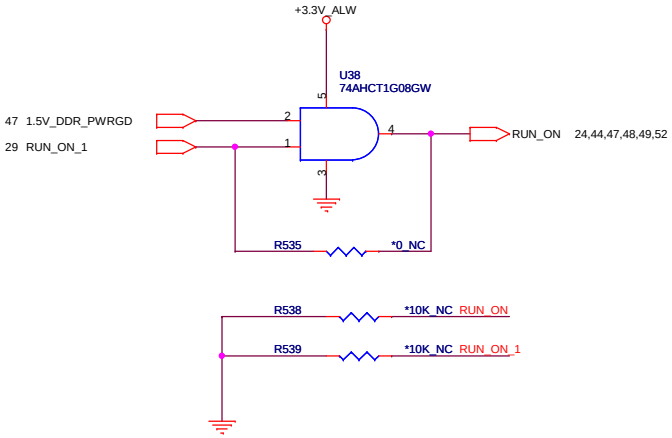


Title	LAN		
Size	Document Number FM9		Rev 1A
Date:	Wednesday, March 04, 2009	Sheet 41 of 64	









QUANTA COMPUTER

Title	System Reset Circuit	
Size	Document Number FM9	Rev 1A
Date: Wednesday, March 04, 2009	Sheet 42 of 64	

QUANTA COMPUTER

Title	Battery Selector	
Size	Document Number FM9	Rev 1A
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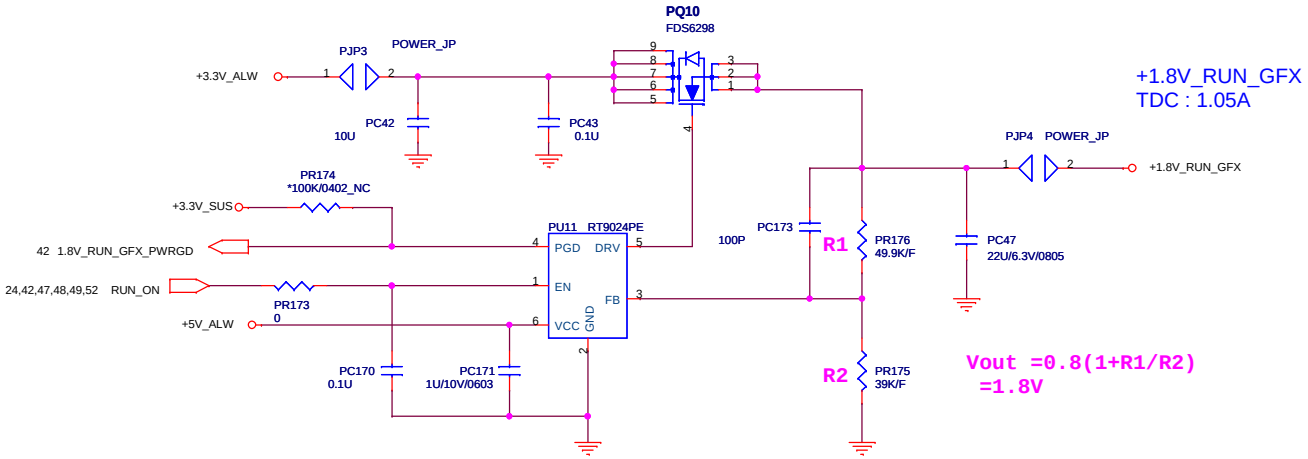
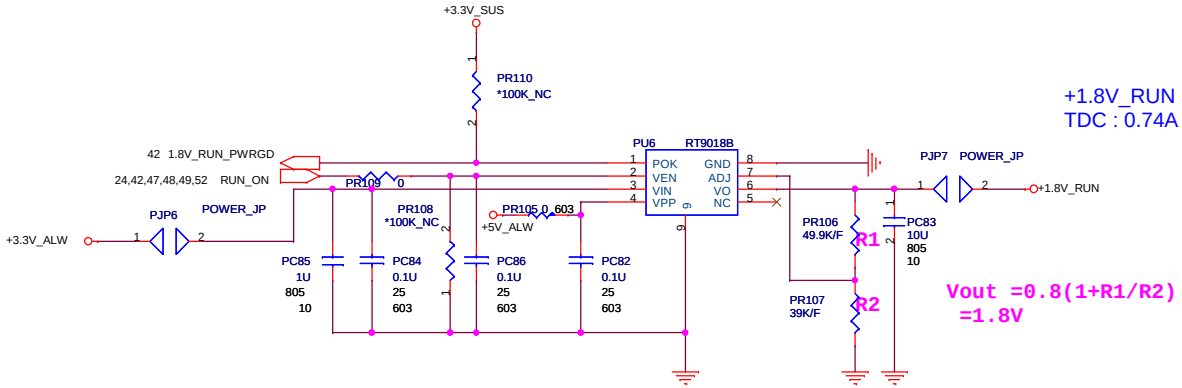


+1.8V_RUN_GFX for VGA 1.8V
+1.8V_RUN for CPU and PCH 1.8V



Title	+1.8V_RUN_GFX (RT9024PE) & +1.8V_RUN(RT9018B)	
Size	Document Number FM9	Rev 1A
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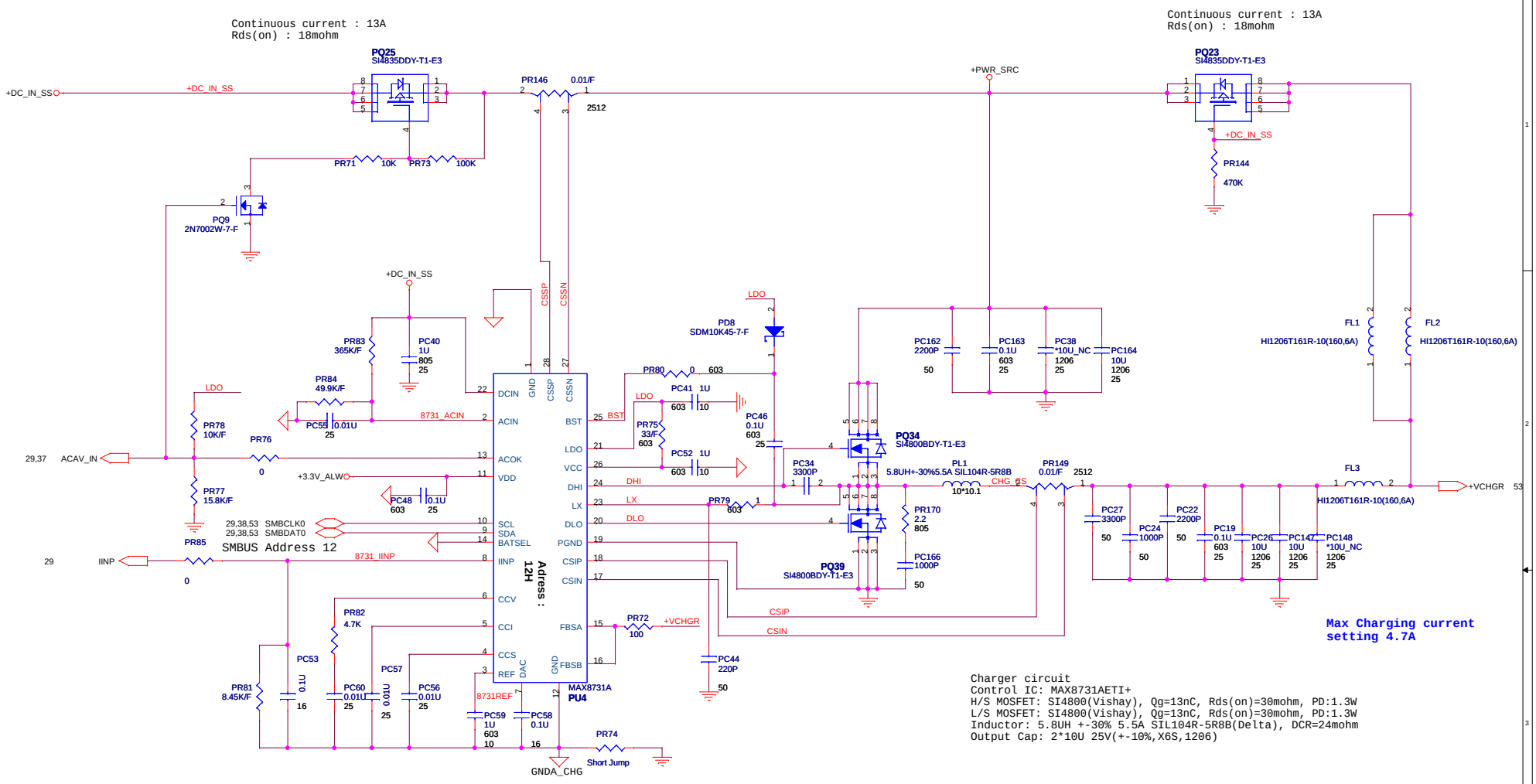

QUANTA COMPUTER

Title	Charger (MAX8731)	
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+3.3V_ALW
Control IC: TPS51427A
H/S MOSFET: FDS8878(Fairchild), Qg=14nC, Rds(on)=17mohm, PD:2.5W
L/S MOSFET: FDS6680AS(Fairchild), Qg=16nC, Rds(on)=10.5mohm, PD:2.5W
Inductor: 3.3UH +-20% 12.3A FDVE1040-H-3R3M=P3(TOKO), DCR=10.1mohm
Output Cap: 1*150U 6.3V(20%,ESR15,7343,H=1.9),ripple current 2700mA

+5V_ALW
Fs=400K
TDC : 5.83A
OCP : 8.33A

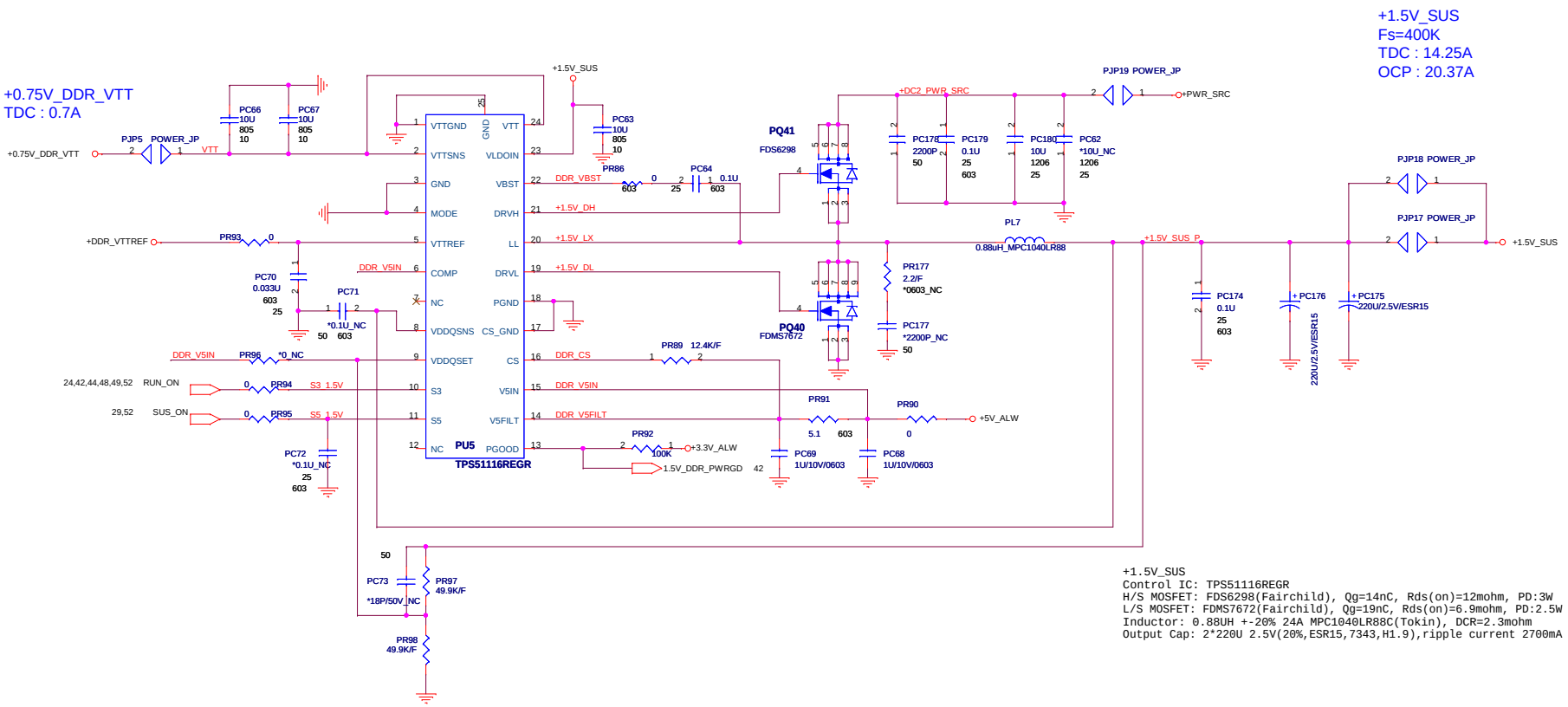
+3.3V_ALW
Fs=300K
TDC : 8.23A
OCP : 11.77A

+5V_ALW
Control IC: TPS51427A
H/S MOSFET: SI4800BDY-T1-E3(Vishay), Qg=13nC, Rds(on)=30mohm, PD:1.3W
L/S MOSFET: SI4812BDY-T1-E3(Vishay), Qg=13nC, Rds(on)=21mohm, PD:1.4W
Inductor: 3.3UH +-30% 9A SIL1045R-3R3(Delta), DCR=21mohm
Output Cap: 1*150U 6.3V(20%,ESR15,7343,H=1.9),ripple current 2700mA

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz

QUANTA COMPUTER

Title	3.3V_ALW / 5V_ALW(TPS51427A)	
Size	Document Number FM9	Rev 1A
Date: Wednesday, March 04, 2009	Sheet 46 of 64	



+1.5V_SUS
Control IC: TPS51116REGR
H/S MOSFET: FDS6298(Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
L/S MOSFET: FDMS7672(Fairchild), Qg=19nC, Rds(on)=6.9mohm, PD:2.5W
Inductor: 0.88UH +-20% 24A MPC1040LR88C(Tokin), DCR=2.3mohm
Output Cap: 2*220U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

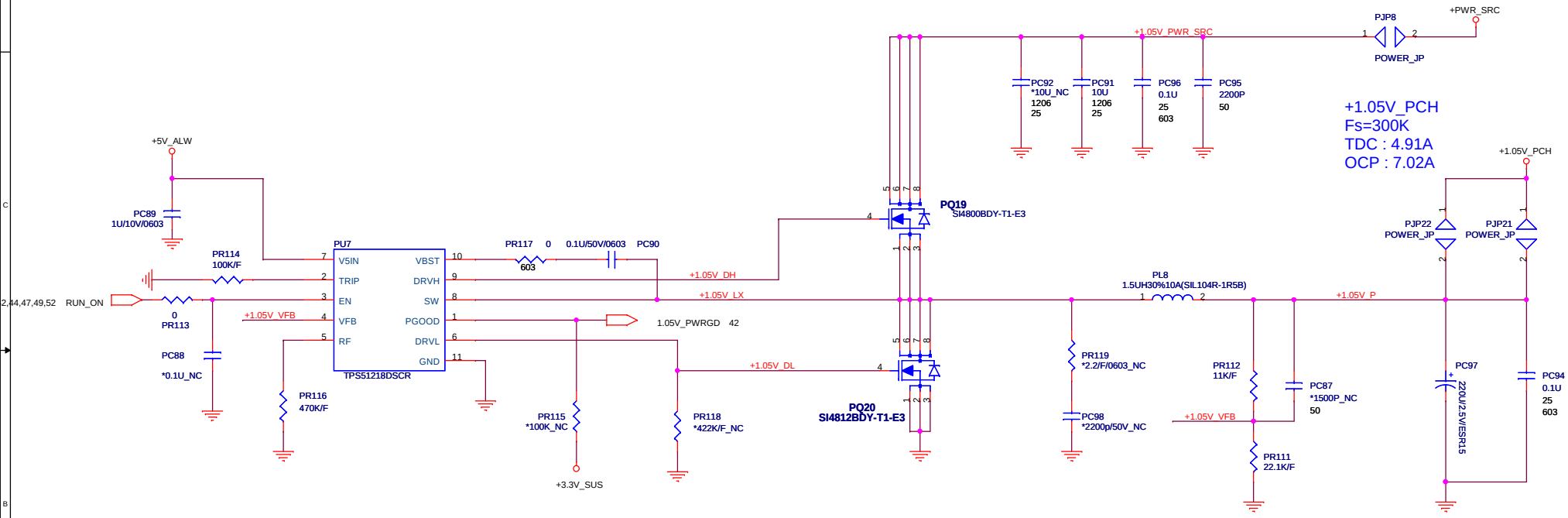
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	2.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Title	DDR3 +1.5V_SUS(TPS51116)		
Size	Document Number FM9		Rev 1A
Date:	Wednesday, March 04, 2009	Sheet 47 of 64	



Frequency setting

pin5 resister	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

+1.05V_PCH
Control IC: TPS51218DSCR
H/S MOSFET: SI4800BDY-T1-E3(Vishay), Qg=13nC, Rds(on)=30mohm, PD:1.3W
L/S MOSFET: SI4812BDY-T1-E3(Vishay), Qg=13nC, Rds(on)=21mohm, PD:1.4W
Inductor: 1.5UH +-30% 10A SIL104R-1R5B(Delta), DCR=8.1mohm
Output Cap: 1*220U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

Title	+1.05V_PCH(TPS51218)		
Size	Document Number FM9		Rev 1A
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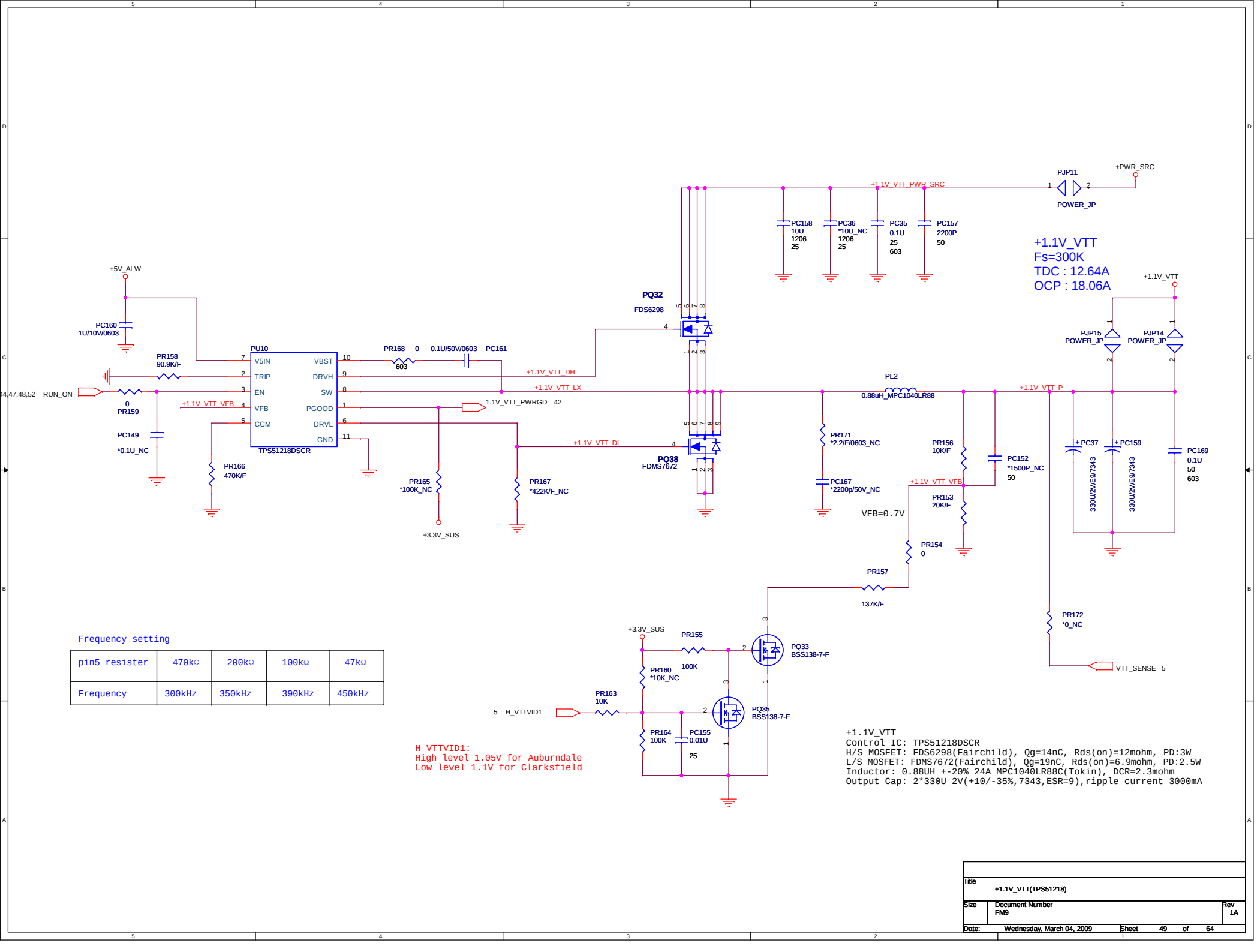
+1.1V_VTT
Fs=300K
TDC : 12.64A
OCP : 18.06A
+5V_ALW
PC160
1U/10V/0603
PR158
90.9K/F
PU10
TPS51218DSCR
V5IN
TRIP
EN
VFB
CCM
VBST
DRVH
SW
PGOOD
DRVL
GND
PR168 0 0.1U/50V/0603 PC161
603
+1.1V_VTT_DH
+1.1V_VTT_LX
+1.1V_VTT_VFB
1.1V_VTT_PWRGD 42
+1.1V_VTT_DL
44,47,48,52 RUN_ON
0
PR159
PC149
*0.1U_NC
PR166
470K/F
PR165
*100K_NC
+3.3V_SUS
PR167
*422K/F_NC
PQ32
FDS6298
PQ38
FDMS7672
+1.1V_VTT_PWR_SRC
PJP11
POWER_JP
+PWR_SRC
PC158
10U
1206
25
PC36
*10U_NC
1206
25
PC35
0.1U
25
603
PC157
2200P
50
PL2
0.88uH_MPC1040LR88
+1.1V_VTT_P
PJP15
POWER_JP
PJP14
POWER_JP
PR171
*2.2/F/0603_NC
PC167
*2200p/50V_NC
PR156
10K/F
PR153
20K/F
VFB=0.7V
PC152
*1500P_NC
50
PC37
330U/2V/E9/7343
PC159
330U/2V/E9/7343
PC169
0.1U
50
603
PR154
0
PR157
137K/F
PR172
*0_NC
VTT_SENSE 5
+3.3V_SUS
PR155
100K
PR160
*10K_NC
PQ33
BSS138-7-F
PR163
10K
5 H_VTTVID1
PR164
100K
PC155
0.01U
25
PQ35
BSS138-7-F
Frequency setting
pin5 resister | 470kΩ | 200kΩ | 100kΩ | 47kΩ
Frequency | 300kHz | 350kHz | 390kHz | 450kHz
H_VTTVID1:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield
+1.1V_VTT
Control IC: TPS51218DSCR
H/S MOSFET: FDS6298(Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
L/S MOSFET: FDMS7672(Fairchild), Qg=19nC, Rds(on)=6.9mohm, PD:2.5W
Inductor: 0.88UH +-20% 24A MPC1040LR88C(Tokin), DCR=2.3mohm
Output Cap: 2*330U 2V(+10/-35%,7343,ESR=9),ripple current 3000mA
Title
+1.1V_VTT(TPS51218)
Size
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1A
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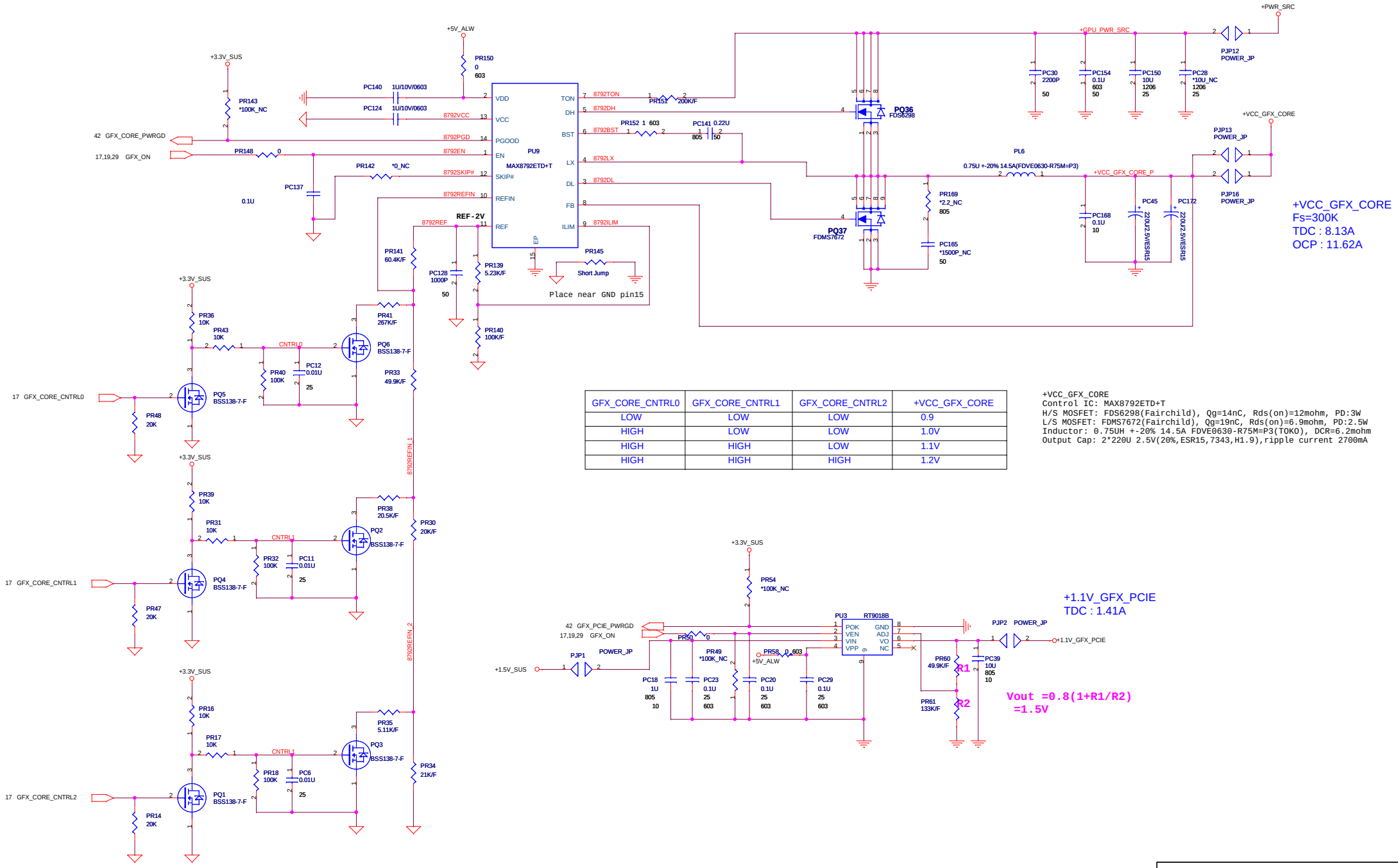

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	GFX_CORE_CNTRL2	+VCC_GFX_CORE
LOW	LOW	LOW	0.9
HIGH	LOW	LOW	1.0V
HIGH	HIGH	LOW	1.1V
HIGH	HIGH	HIGH	1.2V

Title	VGA power (MAX8792 & RT9018B)		
Size	Document Number FM9		Rev 1A
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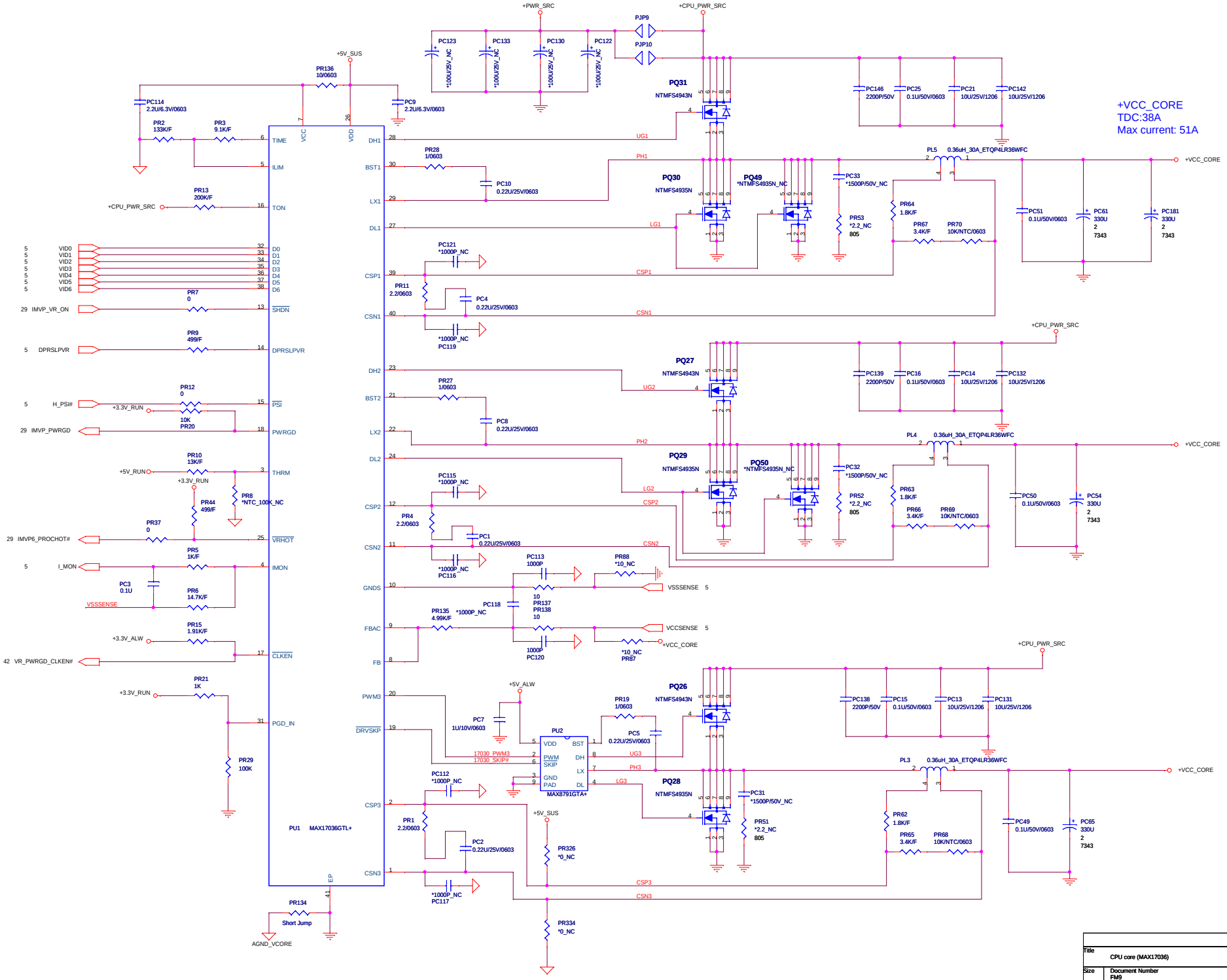
+VCC_CORE
TDC:38A
Max current: 51A
PU1 MAX17036GTL+
PU2 MAX8791GTA+
PQ31 NTMFS4943N
PQ30 NTMFS4935N
PQ49 *NTMFS4935N_NC
PQ27 NTMFS4943N
PQ29 NTMFS4935N
PQ50 *NTMFS4935N_NC
PQ26 NTMFS4943N
PQ28 NTMFS4935N
PL5 0.36uH_30A_ETQP4LR36WFC
PL4 0.36uH_30A_ETQP4LR36WFC
PL3 0.36uH_30A_ETQP4LR36WFC
+PWR_SRC
+CPU_PWR_SRC
+5V_SUS
+5V_ALW
+3.3V_RUN
+3.3V_ALW
+5V_RUN
+VCC_CORE
VSSSENSE
VCCSENSE
AGND_VCORE
Short Jump
Title
CPU core (MAX17036)
Size
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Rev
<RevCode>
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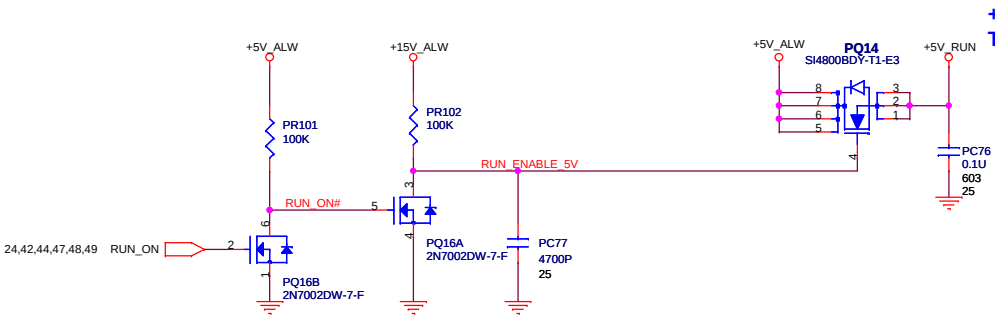
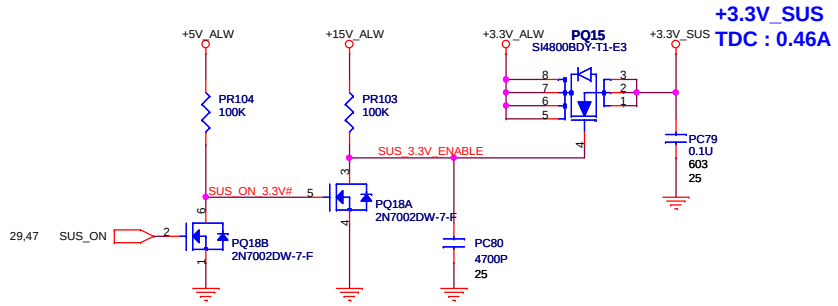
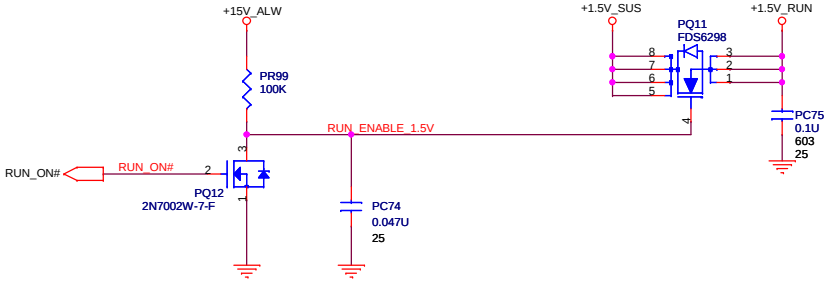
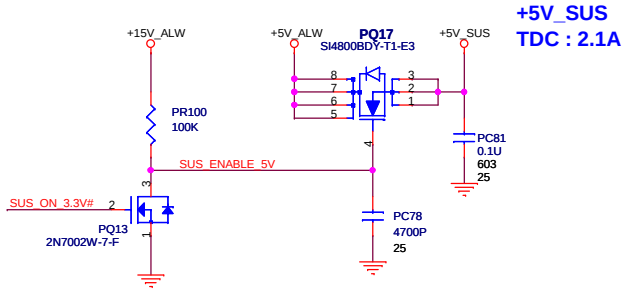
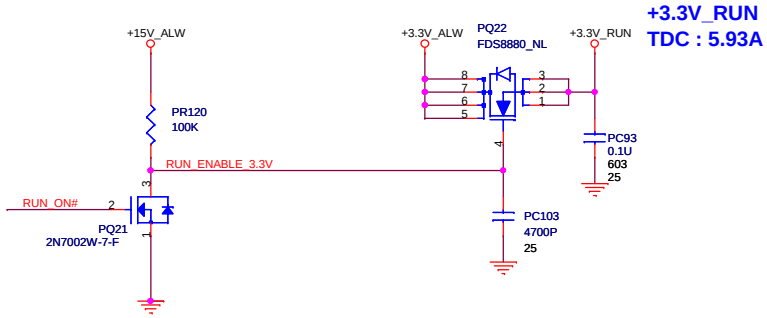


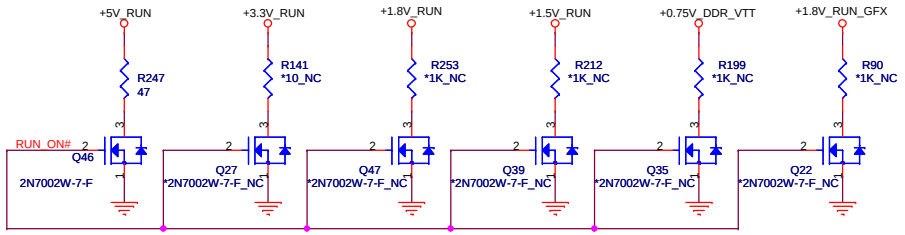


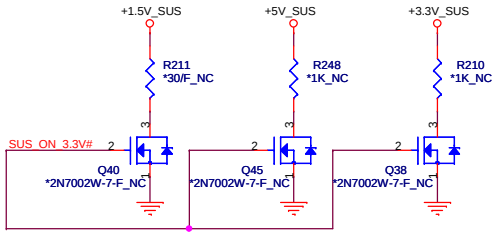






Reserve discharge path





QUANTA COMPUTER

Title	RUN / SUS POWER SW	
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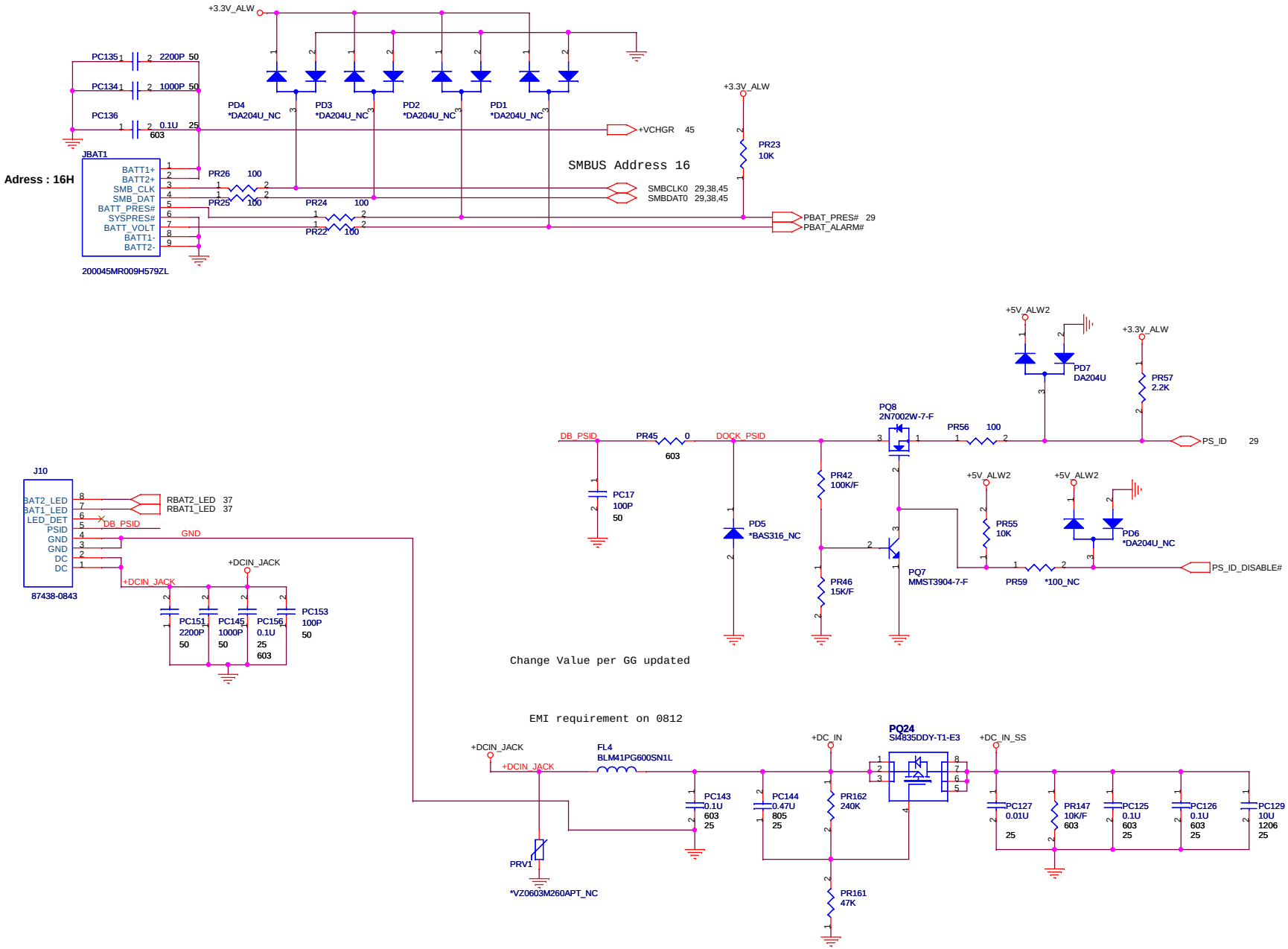

QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number FM9	Rev 1A
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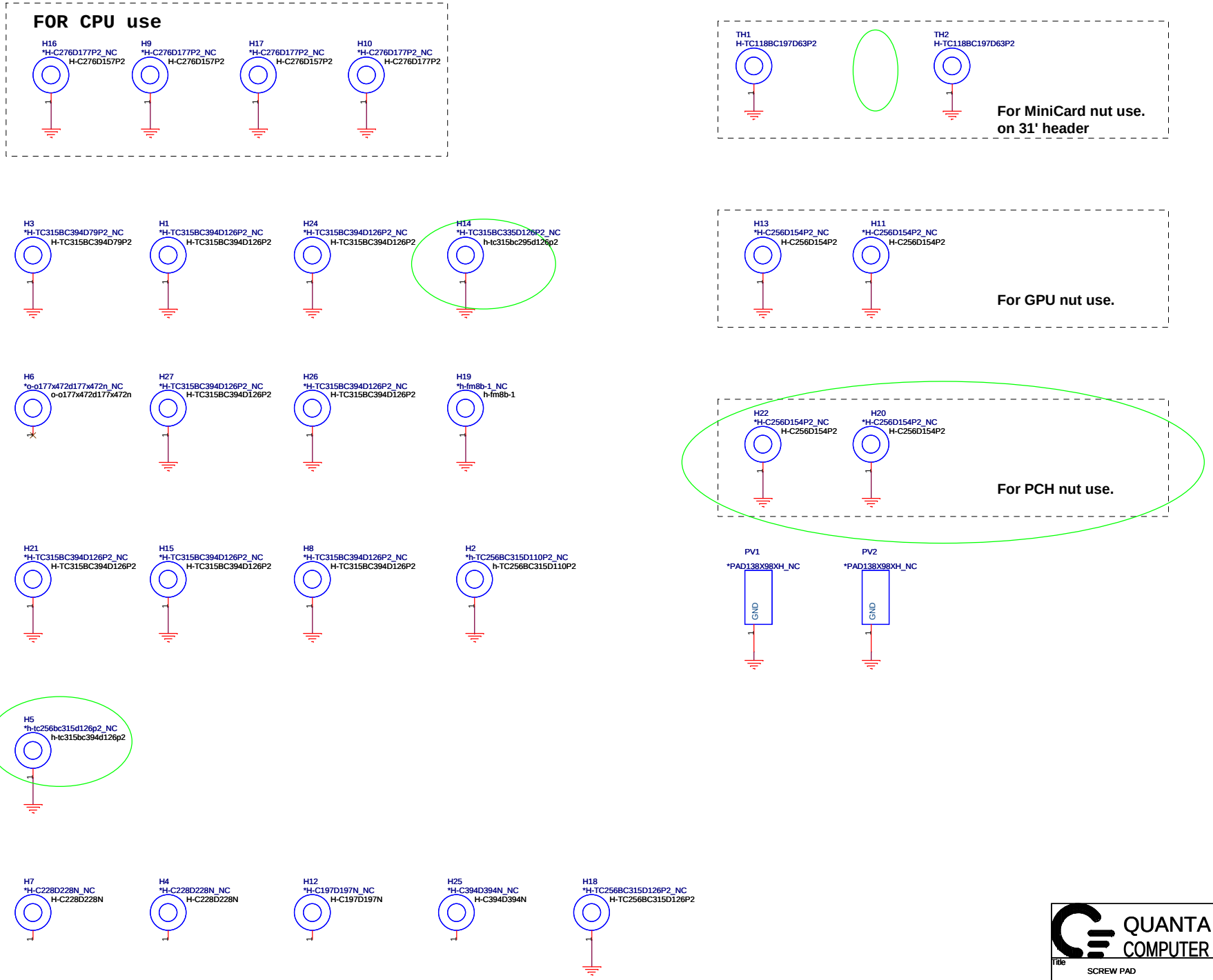

QUANTA COMPUTER

Title	SCREW PAD	
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Reserved for EMI.

QUANTA COMPUTER

Title	EMI CAP	
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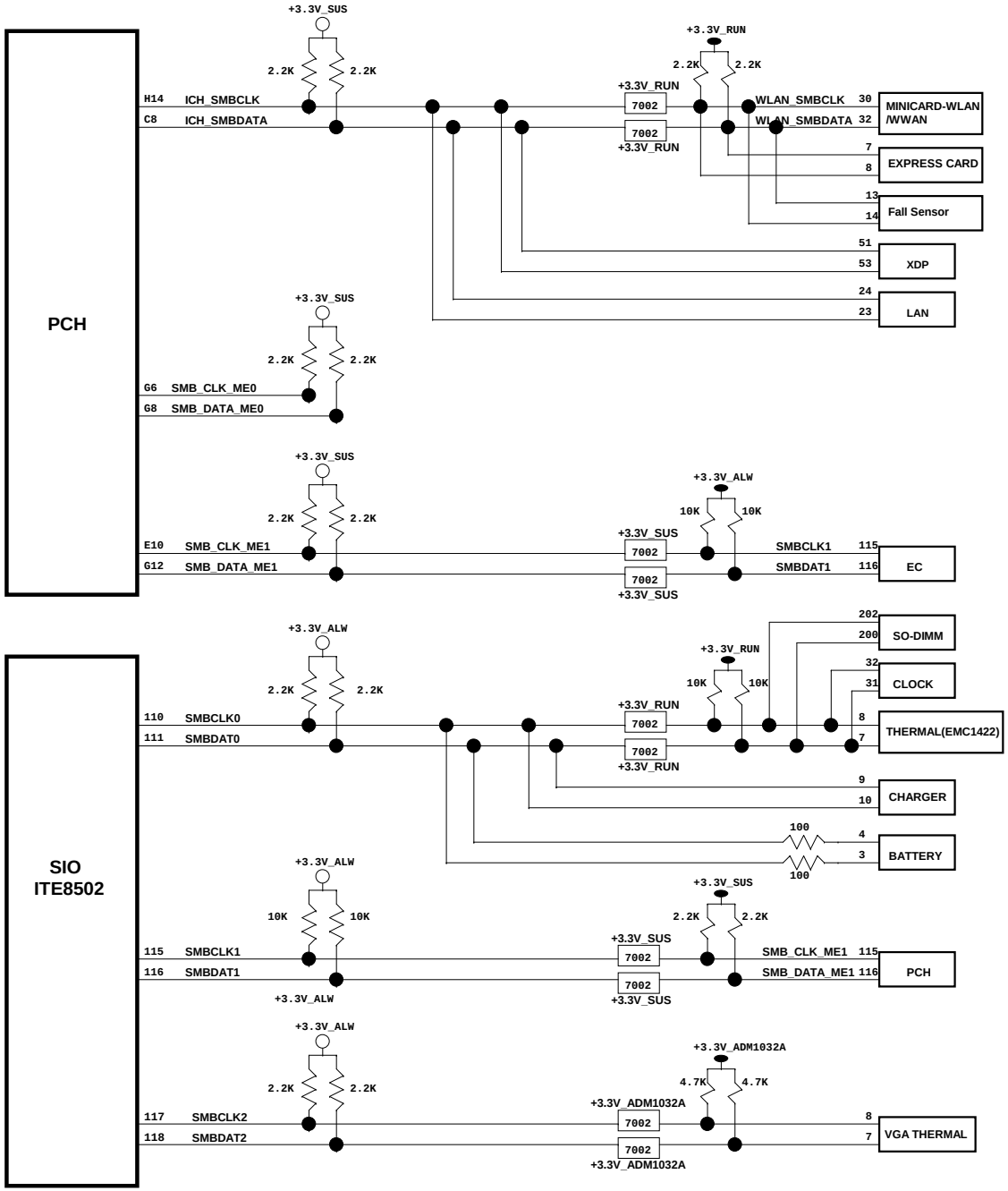

QUANTA COMPUTER			
Title: SMBUS BLOCK			
Size	Document Number: FM9		Rev: 1A
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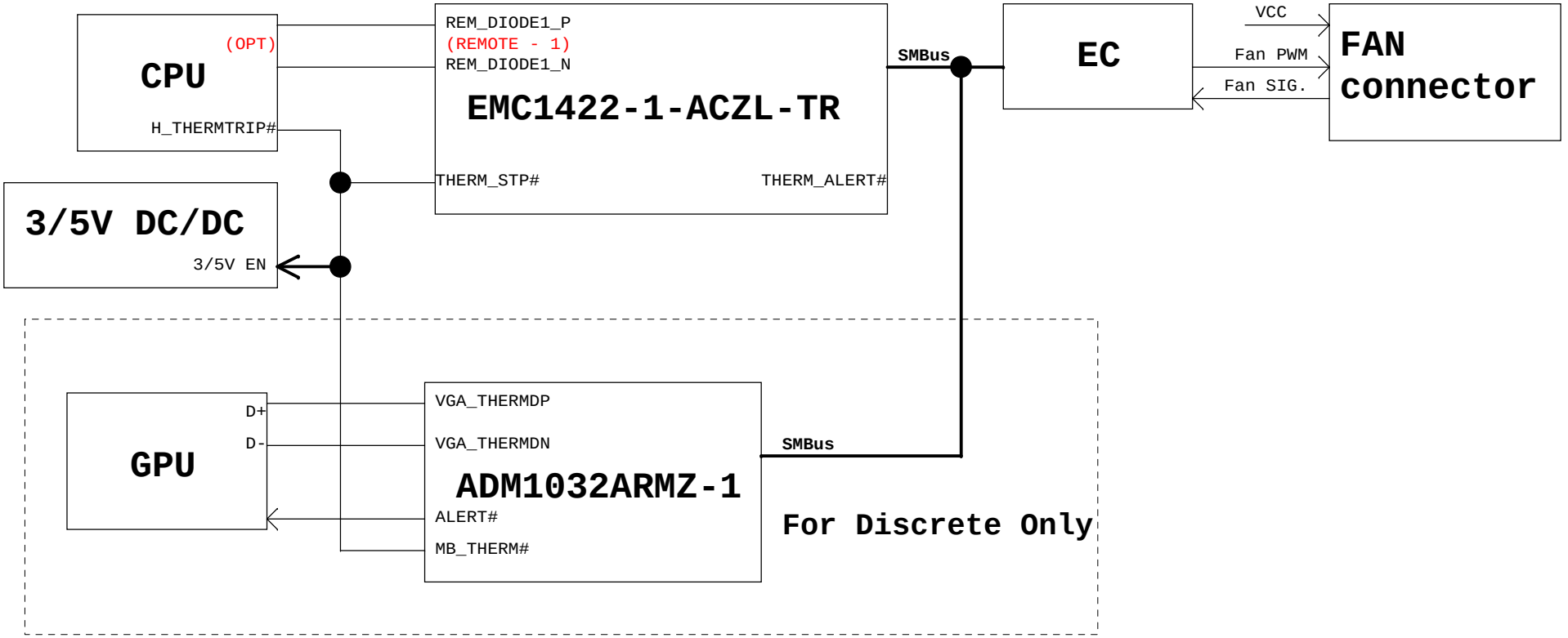

QUANTA COMPUTER

Title	Thermal Map	
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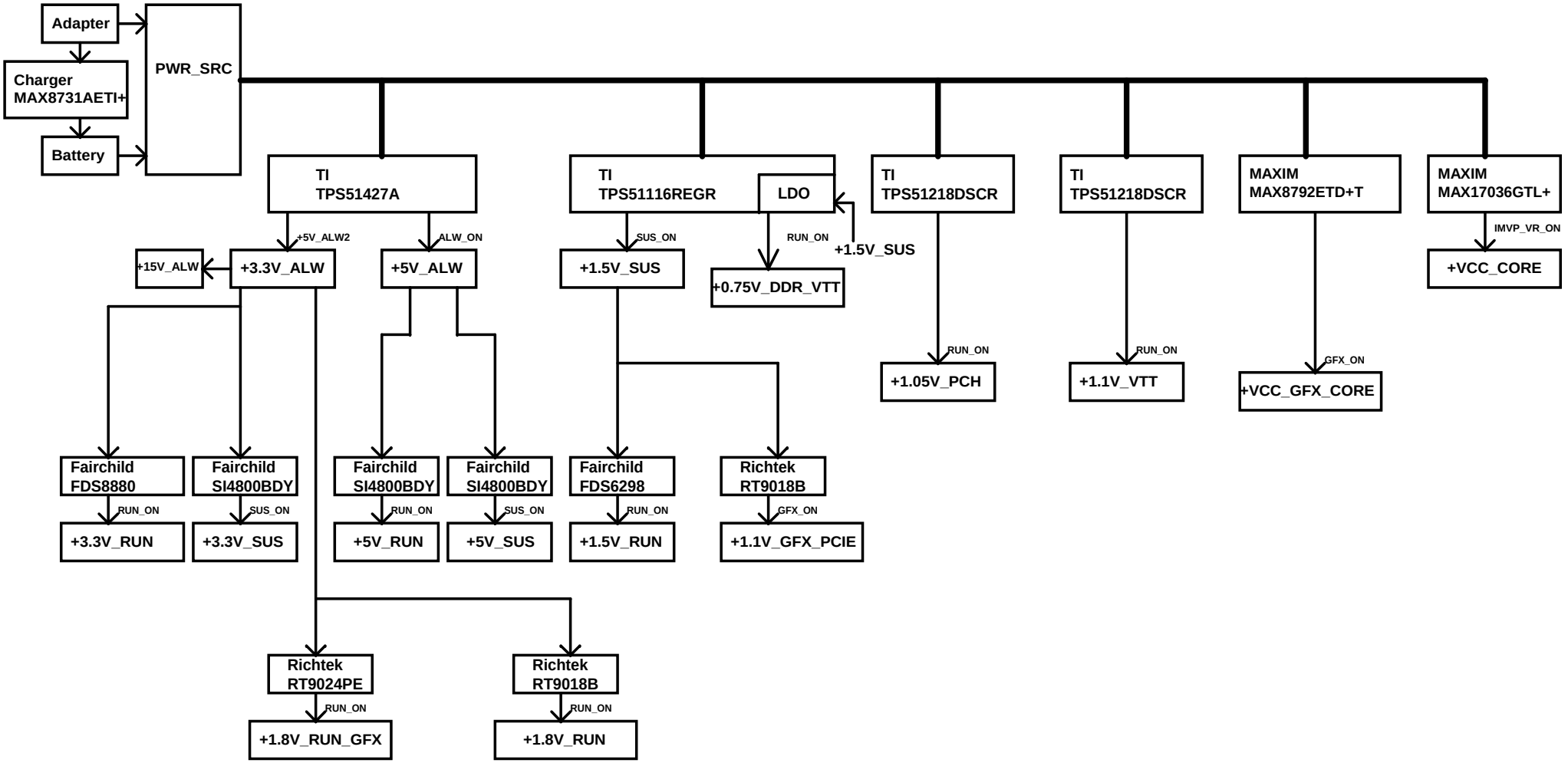
VER : 1A



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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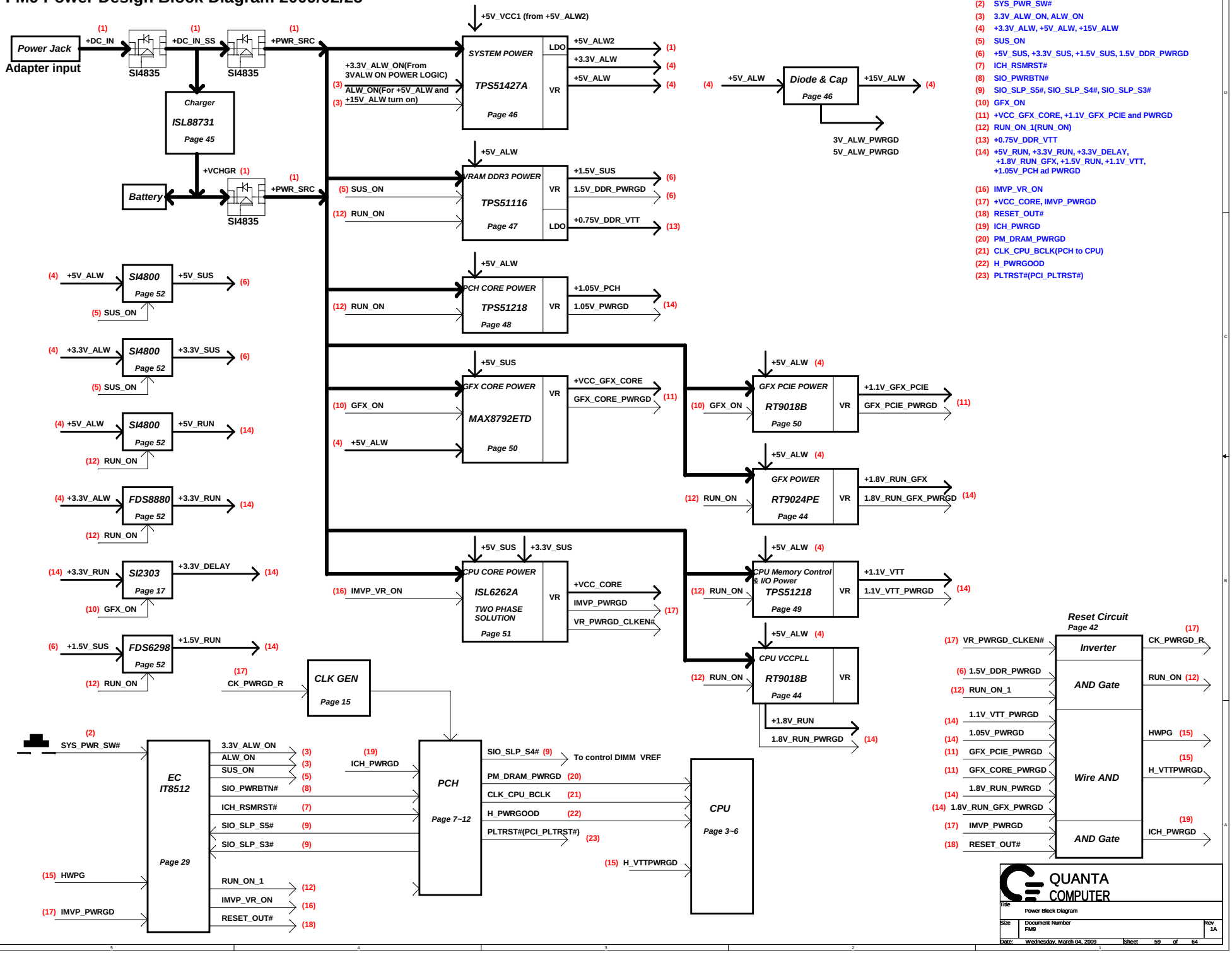
FM9 Power Design Block Diagram 2009/02/25



(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2) SYS_PWR_SW#
(3) 3.3V_ALW_ON, ALW_ON
(4) +3.3V_ALW, +5V_ALW, +15V_ALW
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
(7) ICH_RSMRST#
(8) SIO_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) GFX_ON
(11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
(12) RUN_ON_1(RUN_ON)
(13) +0.75V_DDR_VTT
(14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
(16) IMVP_VR_ON
(17) +VCC_CORE, IMVP_PWRGD
(18) RESET_OUT#
(19) ICH_PWRGD
(20) PM_DRAM_PWRGD
(21) CLK_CPU_BCLK(PCH to CPU)
(22) H_PWRGOOD
(23) PLTRST#(PCI_PLTRST#)

QUANTA COMPUTER

Title	Power Block Diagram	
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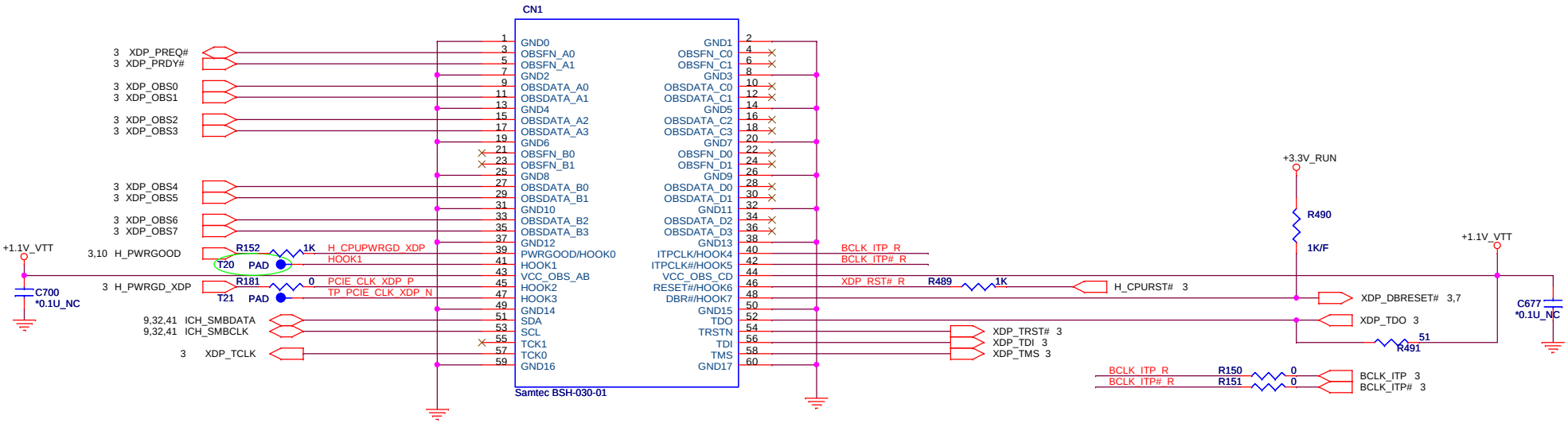

QUANTA COMPUTER

Title	SMBUS BLOCK	
Size	Document Number FM9	Rev 1A
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