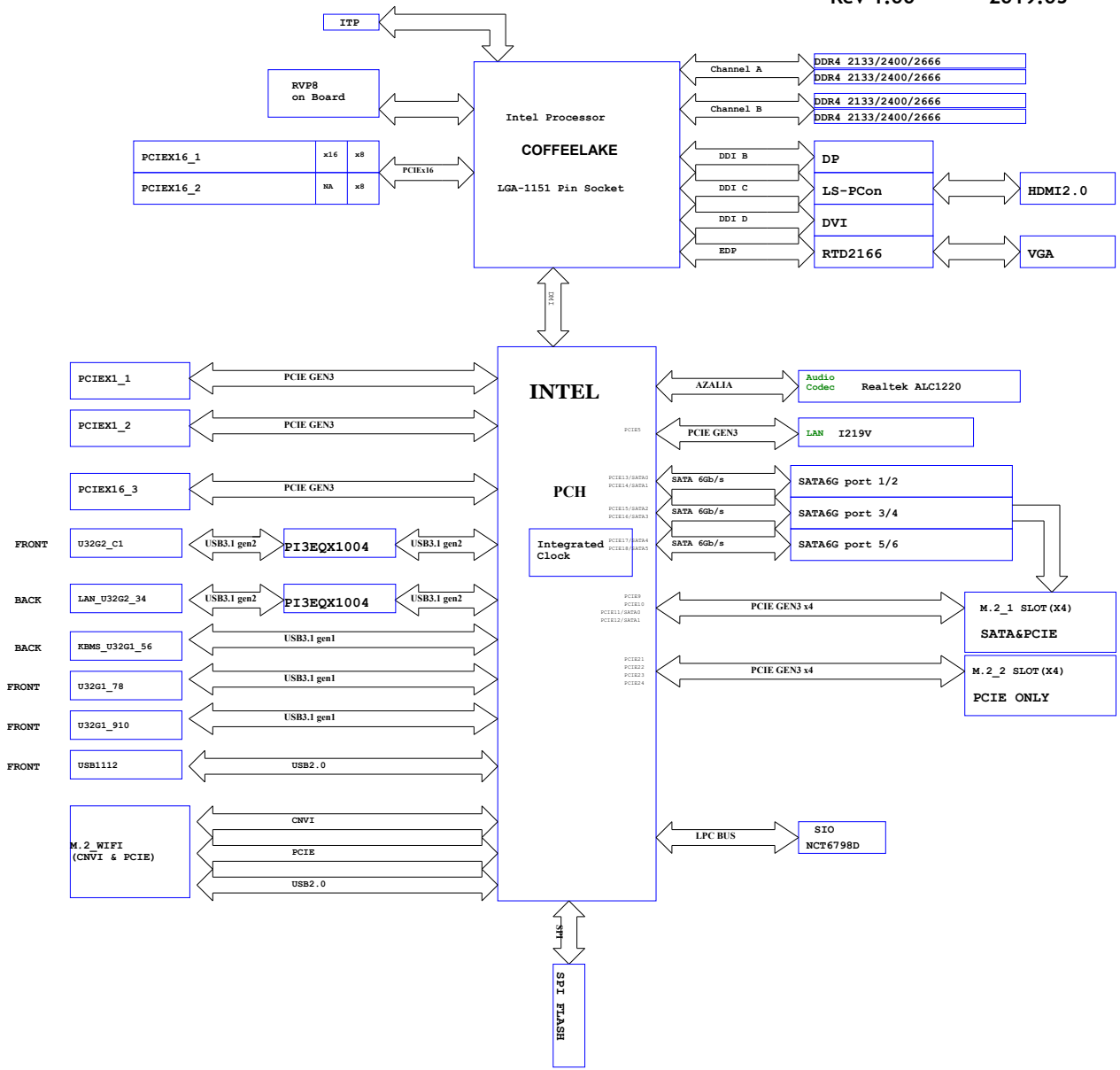
CML GOLDEN

Rev 1.00 2019.05



<Variant Name>

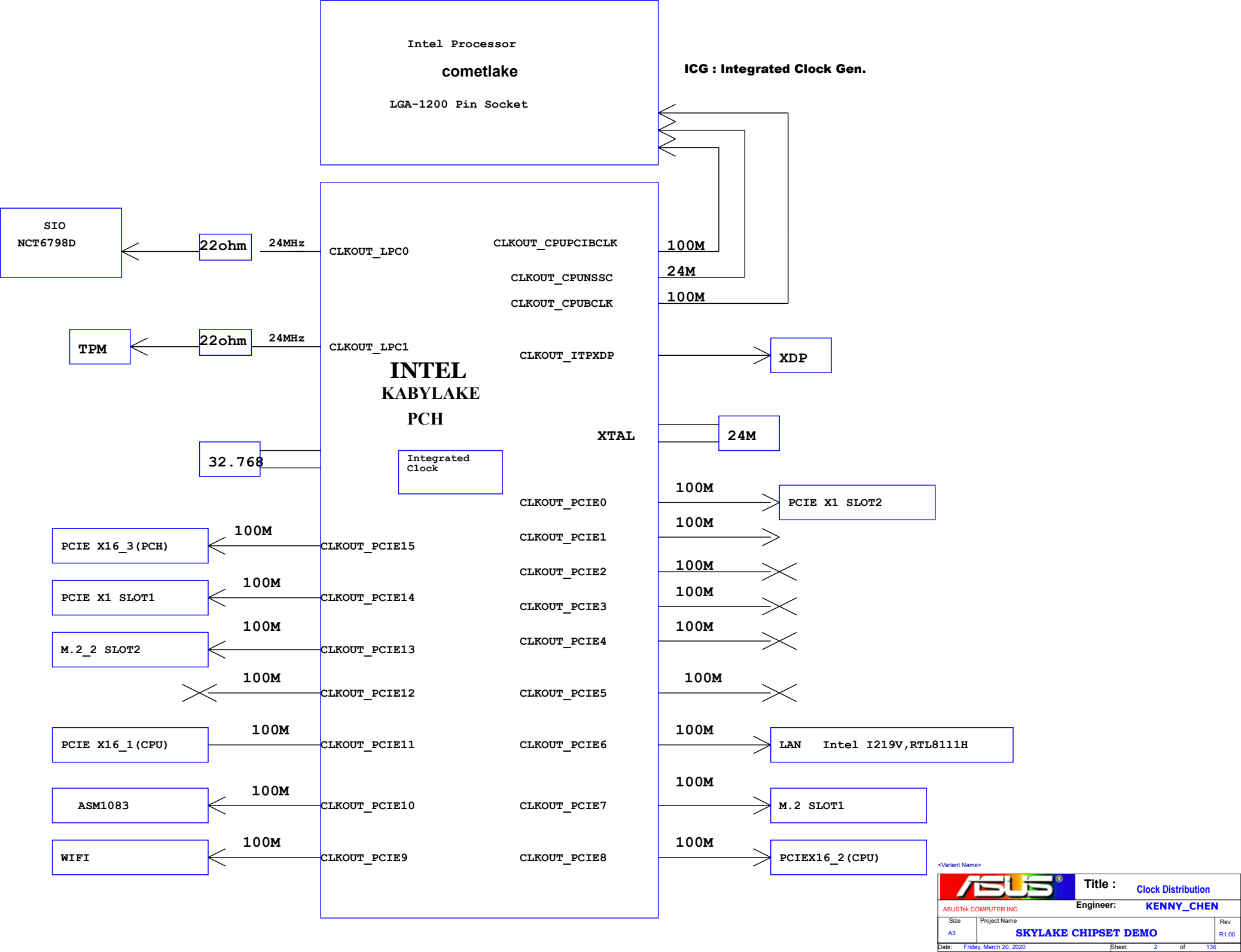
ASUSTeK COMPUTER INC.

Title : Block Diagram

Engineer: Bing-jie_Wang

Size	Project Name	Rev
A2	SKYLAKE CHIPSET DEMO	R1.00

Date: Friday, March 20, 2020 Sheet 1 of 136



<Variant Name>

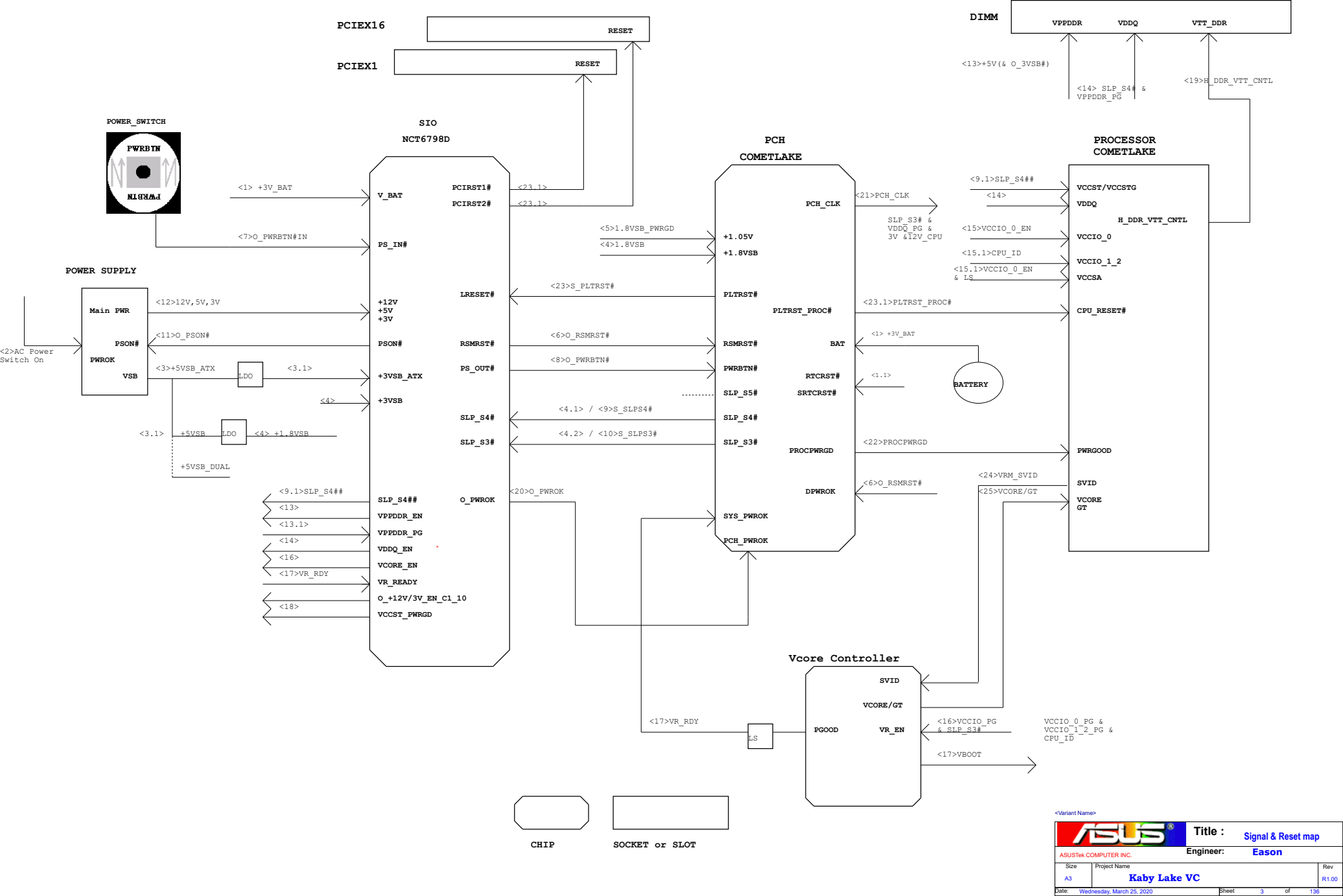
ASUSTek COMPUTER INC.

Title : Clock Distribution

Engineer: KENNY_CHEN

Size	Project Name	Rev
A3	SKYLAKE CHIPSET DEMO	R1.00

Date: Friday, March 20, 2020 Sheet 2 of 136



<Variant Name>

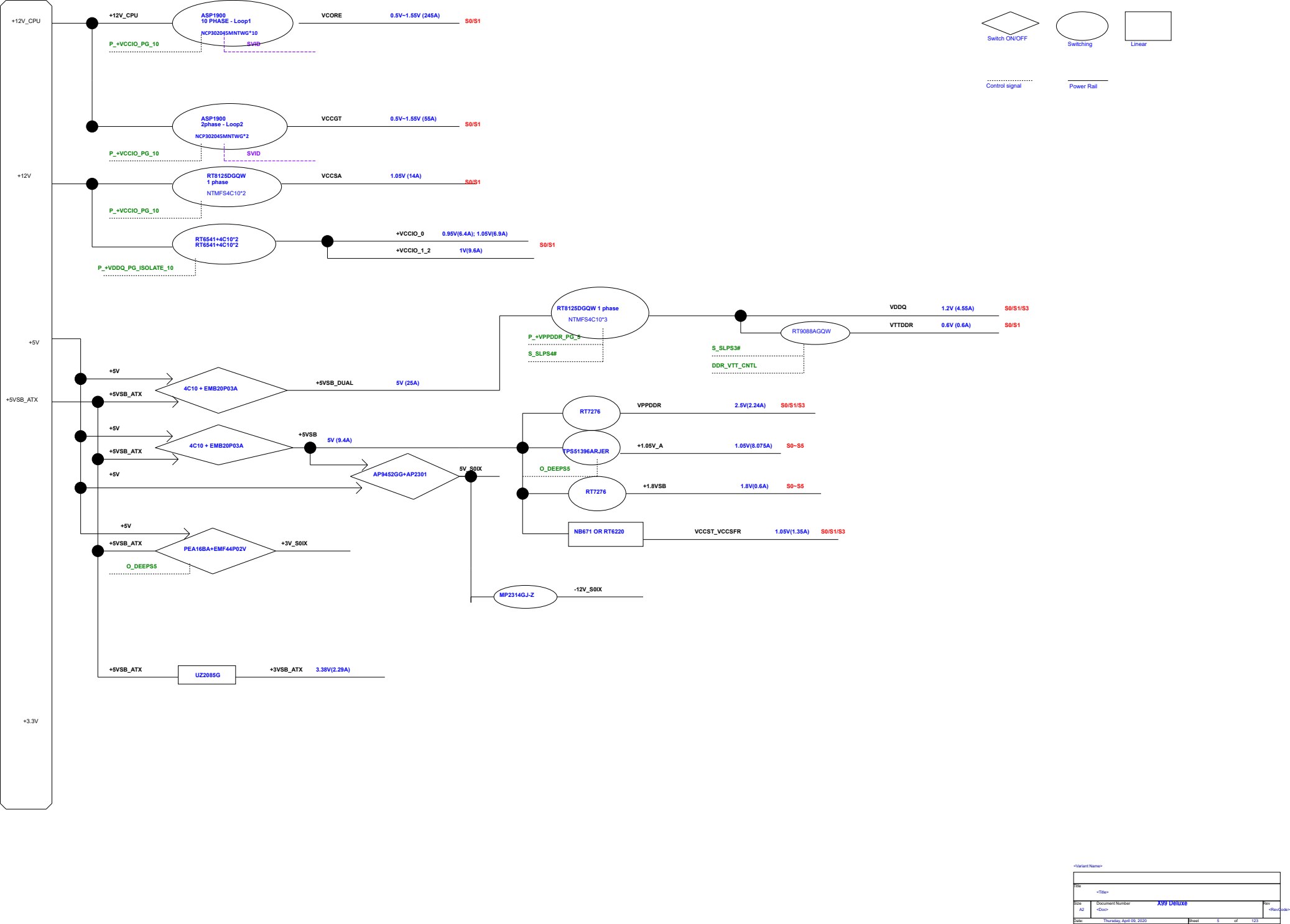
ASUSTek COMPUTER INC.

Title : Signal & Reset map

Engineer: Eason

Size	Project Name	Rev
A3	Kaby Lake VC	R1.00

Date: Wednesday, March 25, 2020 Sheet 3 of 136


+12V_CPU
+12V_CPU
ASP1900
10 PHASE - Loop1
NCP302045MNTWG*10
VCORE
0.5V~1.55V (245A)
S0/S1
P_+VCCIO_PG_10
SVID
ASP1900
2phase - Loop2
NCP302045MNTWG*2
VCCGT
0.5V~1.55V (55A)
S0/S1
P_+VCCIO_PG_10
SVID
+12V
RT8125DGQW
1 phase
NTMFS4C10*2
VCCSA
1.05V (14A)
S0/S1
P_+VCCIO_PG_10
RT6541+4C10*2
RT6541+4C10*2
+VCCIO_0
0.95V(6.4A); 1.05V(6.9A)
+VCCIO_1_2
1V(9.6A)
S0/S1
P_+VDDQ_PG_ISOLATE_10
+5V
RT8125DGQW 1 phase
NTMFS4C10*3
VDDQ
1.2V (4.55A)
S0/S1/S3
VTTDDR
0.6V (0.6A)
S0/S1
RT9088AGQW
P_+VPPDDR_PG_S
S_SLPS4#
S_SLPS3#
DDR_VTT_CNTL
+5V
+5VSB_ATX
4C10 + EMB20P03A
+5VSB_DUAL
5V (25A)
+5V
+5VSB_ATX
4C10 + EMB20P03A
+5VSB
5V (9.4A)
AP9452GG+AP2301
5V_S0IX
+5V
RT7276
VPPDDR
2.5V(2.24A)
S0/S1/S3
TPS51396ARJER
+1.05V_A
1.05V(8.075A)
S0~S5
O_DEEPS5
RT7276
+1.8VSB
1.8V(0.6A)
S0~S5
NB671 OR RT6220
VCCST_VCCSFR
1.05V(1.35A)
S0/S1/S3
+5V
+5VSB_ATX
PEA16BA+EMF44P02V
+3V_S0IX
O_DEEPS5
MP2314GJ-Z
-12V_S0IX
+5VSB_ATX
UZ2085G
+3VSB_ATX
3.38V(2.29A)
+3.3V
Switch ON/OFF
Switching
Linear
Control signal
Power Rail
<Variant Name>
Title
<Title>
Size
A2
Document Number
<Doc>
X99 Deluxe
Rev
<RevCode>
Date:
Thursday, April 09, 2020
Sheet
5
of
123

<Variant Name>

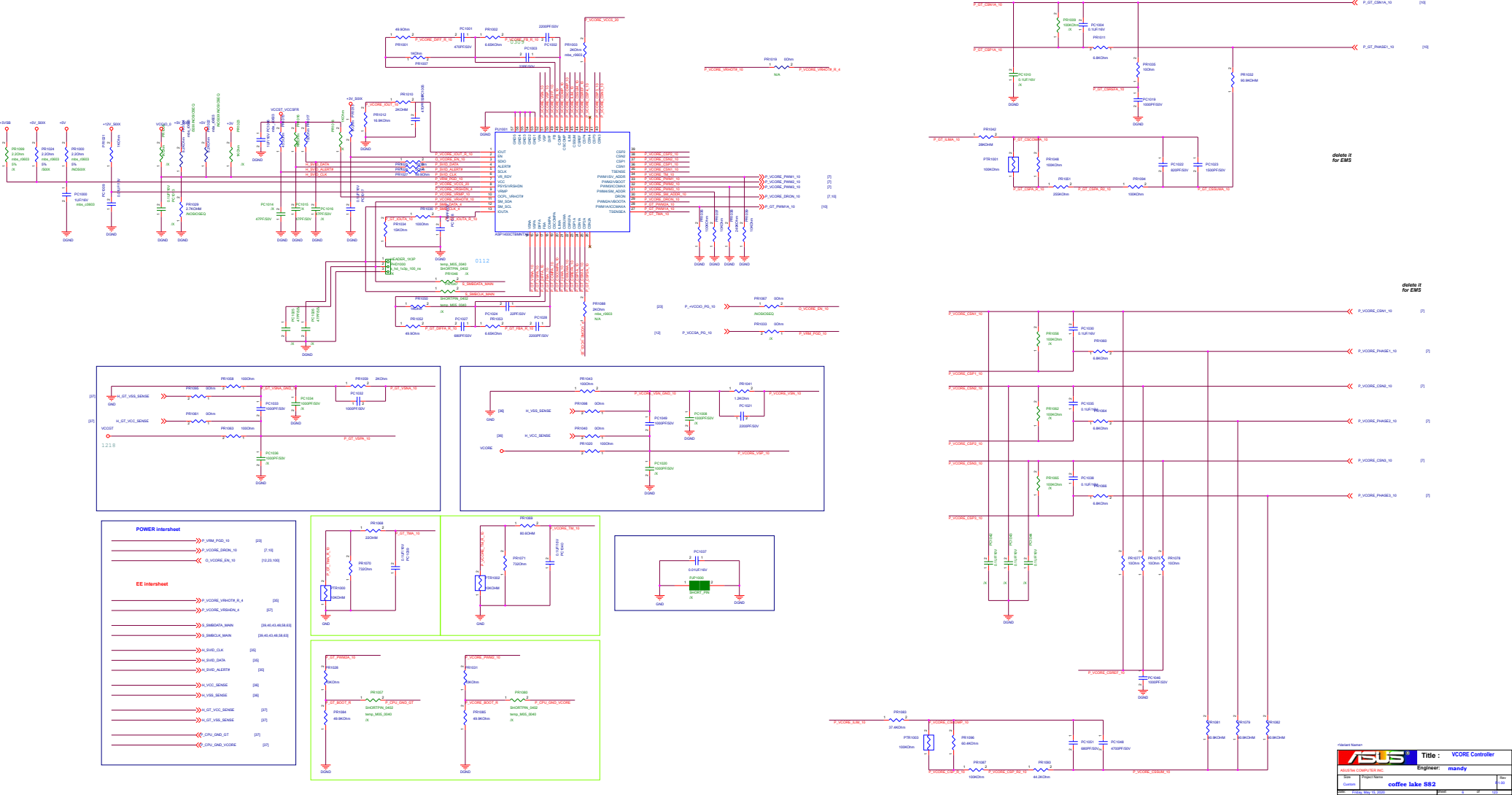
Title : Power Flow

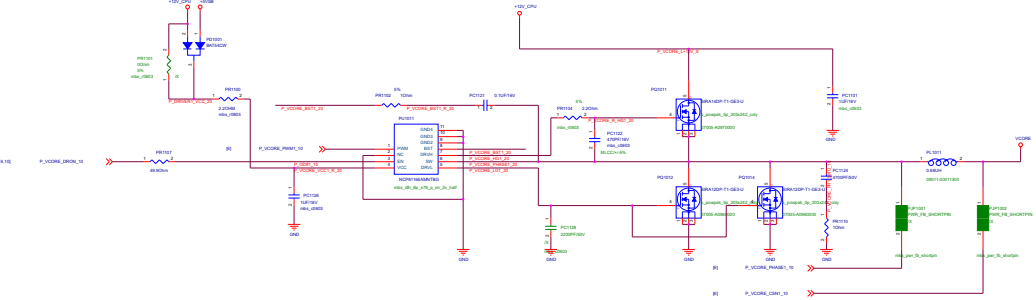
ASUSTek COMPUTER INC.

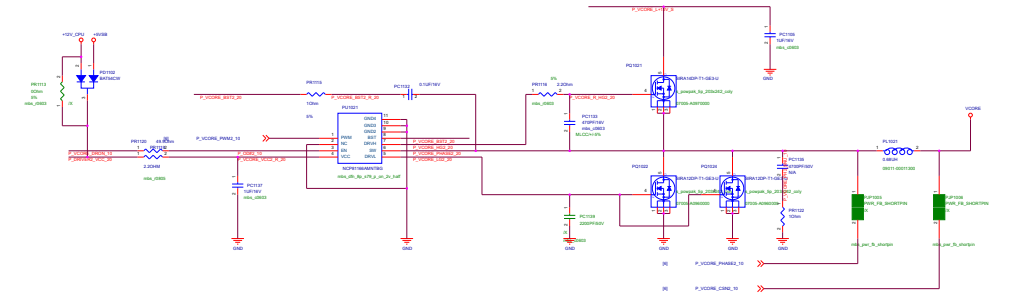
Engineer: Jaosn

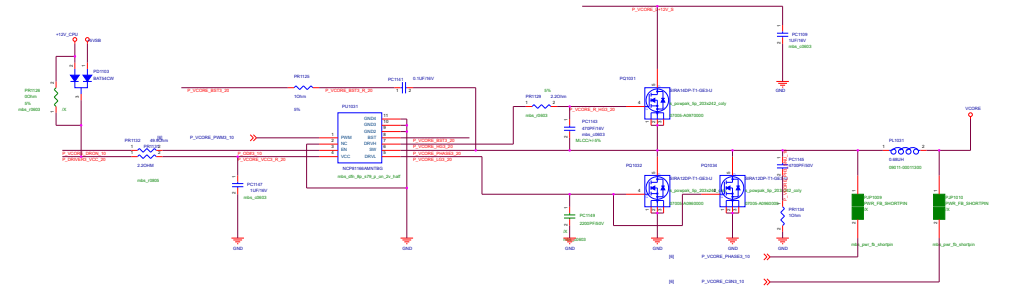
Size	Project Name	Rev
A3	Cometlake	R1.00

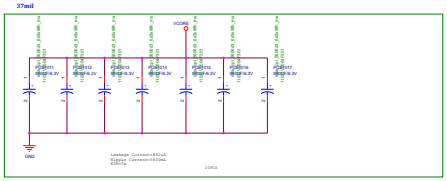
Date:	Monday, March 23, 2020	Sheet	4	of	123

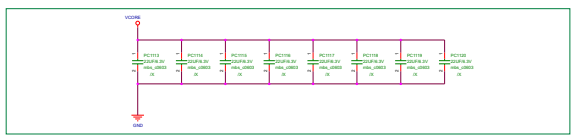

delete it for EMS
delete it for EMS
POWER intersheet
P_VRM_PGD_10 [23]
P_VCORE_DRON_10 [7,10]
O_VCORE_EN_10 [12,23,100]
EE intersheet
P_VCORE_VRHOTB_R_4 [35]
P_VCORE_VRSHSN_4 [57]
S_SMBDATA_MAIN [39,40,43,48,58,63]
S_SMBCLK_MAIN [39,40,43,48,58,63]
H_SVID_CLK [35]
H_SVID_DATA [35]
H_SVID_ALERT# [35]
H_VCC_SENSE [36]
H_VSS_SENSE [36]
H_GT_VCC_SENSE [37]
H_GT_VSS_SENSE [37]
P_CPU_GND_GT [37]
P_CPU_GND_VCORE [37]
Title : VCORE Controller
Engineer: mandy
ASUSTek COMPUTER INC.
Size: Custom
Project Name: coffee lake S82
Rev: 1.00
Date: Friday, May 15, 2020
Sheet 6 of 100

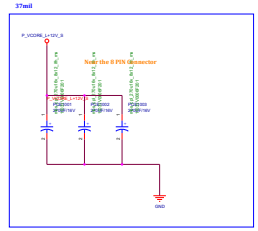












<Variant Name>

Title : VCORE DRIVER1

Engineer: Mandy

Size A1 | Project Name: COMET LAKE | Rev 0.03

Date: Friday, May 15, 2020 | Sheet 7 of 133

<Variant Name>

ASUSTek COMPUTER INC.	Title : VCORE DRIVER2	
	Engineer: Mandy	
Size: A1	Project Name: COMET LAKE	Rev: R1.00
Date: Thursday, April 30, 2020	Sheet 8 of 123	

<Variant Name>

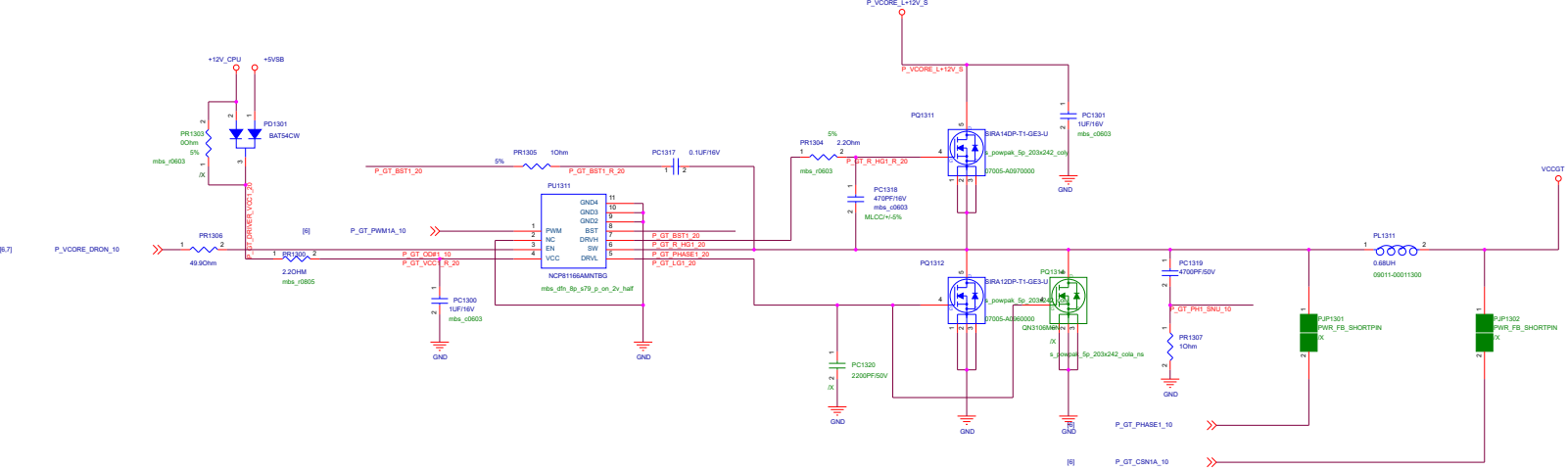
Title : VCORE CONTROLLOR(ISL95856IRZ)

ASUSTek COMPUTER INC.

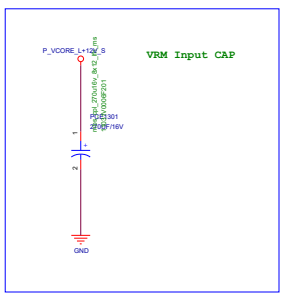
Engineer: ChuKang

Size	Project Name	Rev
Custom	KabyLake VC	R1.00

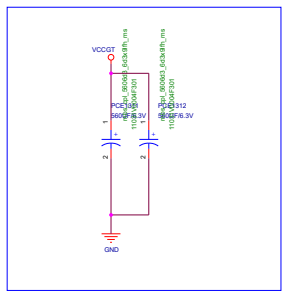
Date:	Thursday, April 30, 2020	Sheet	9	of	123



37mil



37mil



<Variant Name>

ASUSTek COMPUTER INC.

Title : VCCGT DRIVER

Engineer: RAY

Size	Project Name	Rev
A2	SkyLake VC	R1.00

Date: Friday, May 15, 2020 Sheet 10 of 123

<Variant Name>

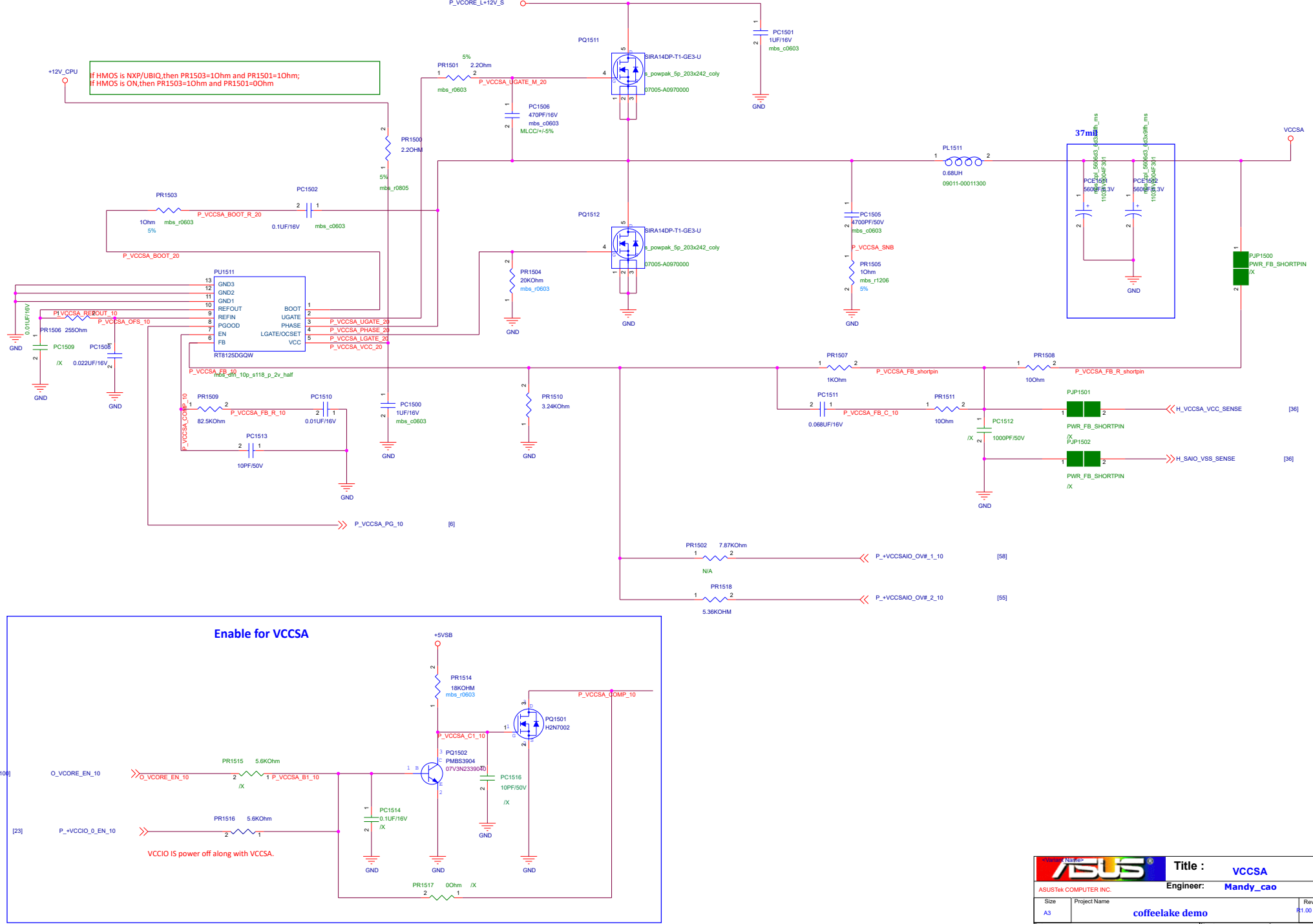
Title : +VCCCORE_3

ASUSTek COMPUTER INC.

Engineer: ChuKang

Size	Project Name	Rev
Custom	KabyLake VC	R1.00

Date:	Thursday, April 30, 2020	Sheet	11	of	123


If HMOS is NXP/UBIQ,then PR1503=1Ohm and PR1501=1Ohm;
If HMOS is ON,then PR1503=1Ohm and PR1501=0Ohm
+12V_CPU
P_VCORE_L+12V_S
PR1501 2.2Ohm
P_VCCSA_UGATE_M_20
PQ1511
SIRA14DP-T1-GE3-U
PC1501 1UF/16V
PC1506 470PF/16V
PR1500 2.2OHM
PR1503 1Ohm
PC1502 0.1UF/16V
P_VCCSA_BOOT_R_20
P_VCCSA_BOOT_20
PQ1512
PR1504 20KOhm
PC1505 4700PF/50V
P_VCCSA_SNB
PR1505 1Ohm
PL1511 0.68UH
09011-00011300
37mil
VCCSA
PJP1500 PWR_FB_SHORTPIN
PU1511
RT8125DQGW
GND3
GND2
GND1
REFOUT
REFIN
PGOOD
EN
FB
BOOT
UGATE
PHASE
LGATE/OCSET
VCC
P_VCCSA_UGATE_20
P_VCCSA_PHASE_20
P_VCCSA_LGATE_20
P_VCCSA_VCC_20
P1VCCSA_REFOUT_10
P_VCCSA_OFS_10
P_VCCSA_FB_10
PR1506 255Ohm
PC1509 /X
PC1508 0.022UF/16V
PR1507 1KOhm
PR1508 10Ohm
P_VCCSA_FB_shortpin
P_VCCSA_FB_R_shortpin
PC1511 0.068UF/16V
PR1511 10Ohm
P_VCCSA_FB_C_10
PC1512 1000PF/50V
PJP1501
PWR_FB_SHORTPIN
H_VCCSA_VCC_SENSE [36]
PJP1502
H_SAIO_VSS_SENSE [36]
PR1509 82.5KOhm
P_VCCSA_FB_R_10
PC1510 0.01UF/16V
PC1513 10PF/50V
P_VCCSA_COMP_10
PC1500 1UF/16V
PR1510 3.24KOhm
P_VCCSA_PG_10 [6]
PR1502 7.87KOhm
N/A
P_+VCCSAIO_OV#_1_10 [58]
PR1518 5.36KOHM
P_+VCCSAIO_OV#_2_10 [55]
Enable for VCCSA
+5VSB
PR1514 18KOHM
P_VCCSA_COMP_10
PQ1501 H2N7002
P_VCCSA_C1_10
PQ1502 PMBS3904
PR1515 5.6KOhm
O_VCORE_EN_10
[6,23,100]
P_VCCSA_B1_10
PC1516 10PF/50V
PR1516 5.6KOhm
[23]
P_+VCCIO_0_EN_10
PC1514 0.1UF/16V
VCCIO IS power off along with VCCSA.
PR1517 0Ohm /X
Title : VCCSA
Engineer: Mandy_cao
ASUSTek COMPUTER INC.
Size A3
Project Name coffeelake demo
Rev R1.00
Date: Thursday, May 21, 2020
Sheet 12 of 123

ASUSTeK COMPUTER INC.	Title : VCCIO	
	Engineer: Mandy_cao	
Size: Custom	Project Name: coffeelake demo	Rev: 1.00
Date: Thursday, April 05, 2018	Sheet 1 of 1	File:

<Variant Name>

ASUSTek COMPUTER INC.	Title : +VCCCORE_3	
	Engineer: ChuKang	
Size: A3	Project Name: KabyLake VC	Rev: R1.00
Date: Thursday, April 30, 2020	Sheet 14 of 123	

<Variant Name>

Title : +VCCCORE_3

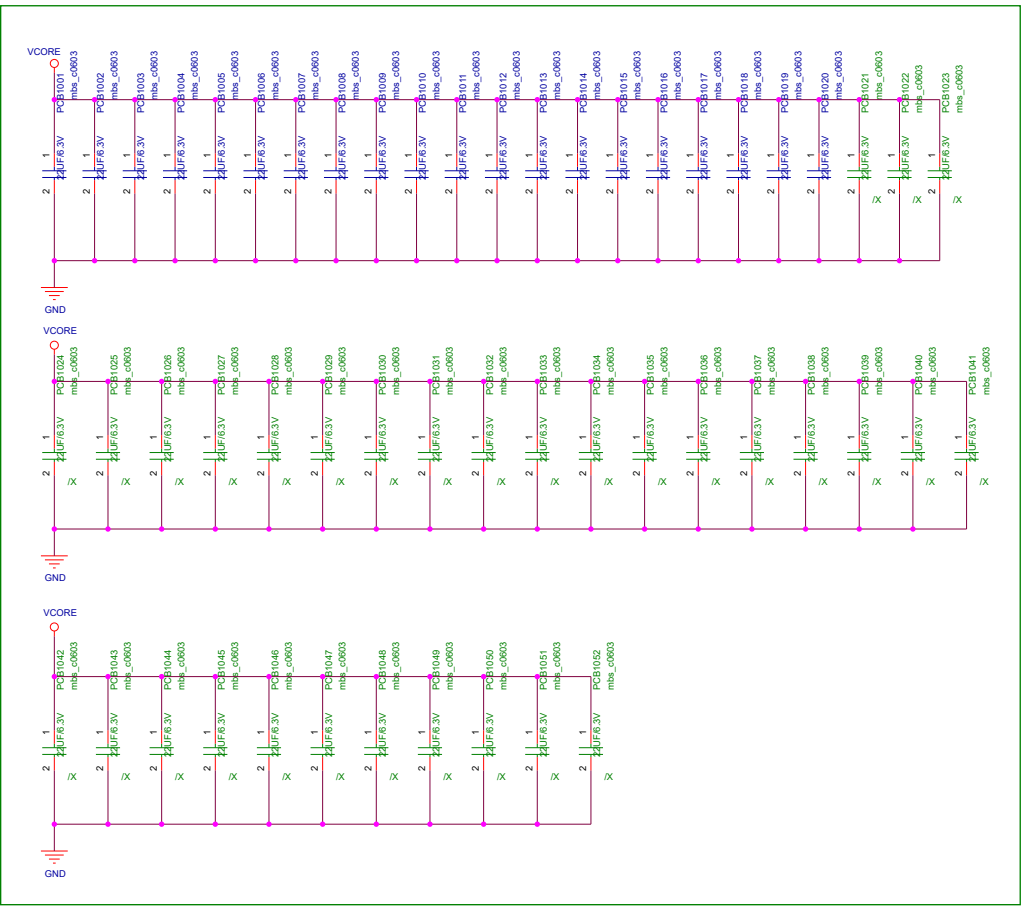
ASUSTek COMPUTER INC.

Engineer: ChuKang

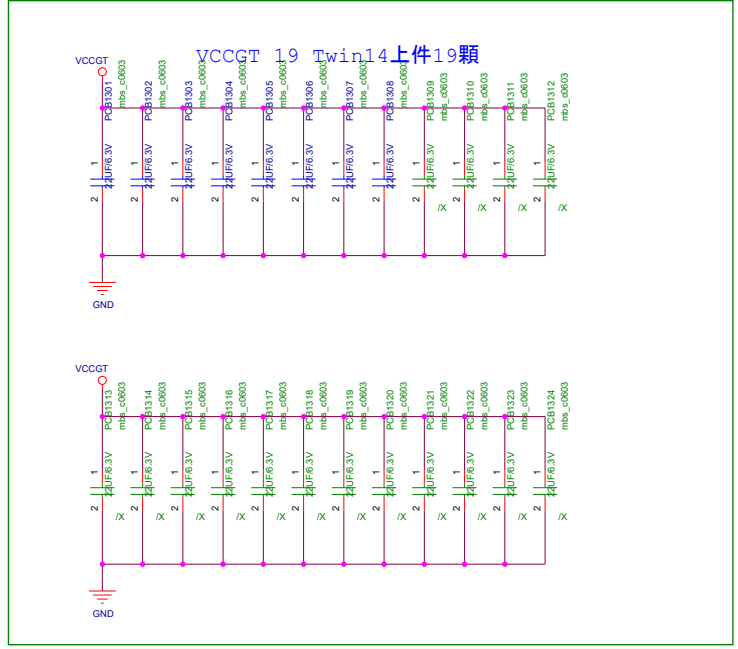
Size	Project Name	Rev
A3	KabyLake VC	R1.00

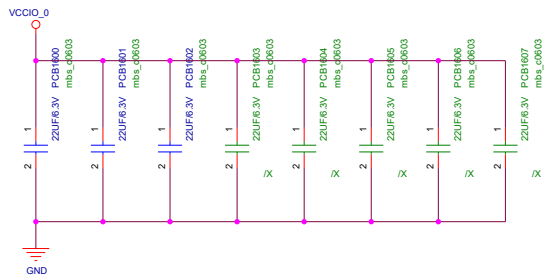
Date:	Thursday, April 30, 2020	Sheet	15	of	123

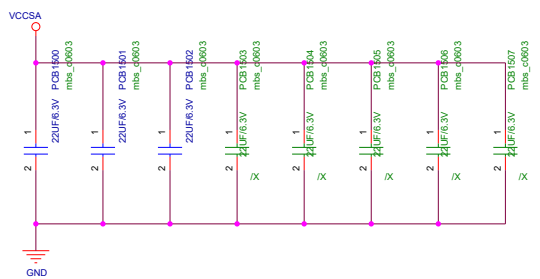
VCORE 50+11 Twin14上件23顆



VCCGT 19 Twin14上件19顆







<Variant Name>

ASUSTek Computer Inc.	Title :	Socket MLCC	
	Engineer:	Mandy	
Size: A3	Project Name: comet lake 10+2		Rev: 1.02
Date: Thursday, April 30, 2020	Sheet 16 of 123		

PR2230&PR2200 value is changed to 10kohm from 200kohm because of TPS54328's EN pin supply current requirements.

Tss=(VFB*Css)/Iss
=(0.765V*4.7NF)/2uA
=1.798ms

20170923:S0-->S3,there's a power down glich with 5V_S0IX control,so we change the control to 3V_S0IX,as well,PR2232 is recified to 0402 22kohm

預留+5VSB_DUAL 电阻分压做 VPPDDR_EN：考量 SIO 內包 SLP_S4#控制 VPPDDR_EN，可能会使 VPPDDR PG(控制 VDDQ EN)早于 VDDQ Vin 5VSB_DUAL,违反我们时序要求。

If using P_VDDQ_SIO_EN_10 from SIO control VDDQ EN,then +VPPDDR_PGD_10 need to VPPDDR pull high,that is,PR2210 need mounted and PR2011 need /X.

If using TPS54328 ,then PR2215/PR2214//PC2216/PR2209/PQ2200/PQ2201 need mounted and PR2212 need /X.

1. 若不使用 NCT6798D A Version和NCT6798D B Version DDR4 Sequence, 此 Block 內紅線與藍線框起來的元件都上件

2. 若使用 NCT6798D A Version DDR4 Sequence, 此 Block 內元件是否上件分三種情況:

A Project 若有 "搭配部分 Power Supply (例如 CORSAIR-AT1200i-75-000784-1204.5W, COOL MASTER-V1200-RS-C00-AFBA-G1) 斷掉AC Power後(拔拔24pin), Power LED仍然亮起, 直到跟SB PWR LED一起熄滅" 的 bug, 則紅線框起來的元件不上件, 藍線框起來的元件仍要上件來patch上述bug

B 有上述 bug 但是不 care 此 bug 的 Project, 紅線與藍線框起來的元件都可不上件

C 滿足下面任何一點的 Project, 理論上不會有上述的 bug, 所以紅線與藍線框起來的元件都可不上件
<1> Power LED 的 power source 在 S4/S5 下無電
<2> 產生 DDR4 VPP Power 的 power source 在 S4/S5 下無電
<3> 產生 DDR4 VDDQ Power 的 power source 在 S4/S5 下無電
<4> 使用 SIO 的 CASE_LED# signal 控制 Power LED

3. 若使用 NCT6798D B Version DDR4 Sequence, 此 Block 內紅線與藍線框起來的元件都不上件

在使用 NCT6798D A Version DDR4 Sequence 時, Power Team 線路 default 配合 C 狀況; A 狀況的 Project 請自行修改 Optional

If we use P_VDDQ_SIO_EN_10 from SIO to control VDDQ EN,then PR2225,PQ2209,PR2223,PR2221,PQ2207 need mounted.Otherwise,we still use S_SLP_S4# and +VPPDDR_PGD_10 to control VDDQ EN.

VDDQ Bleed circuit

2018/04/27, 8.2kohm-->40.2kohm

SLP_S4## pull high resistor PR2005 value affects VBAT drop.

P_+VDDQ_OV#_1_10	P_+VDDQ_OV#_2_10	VDDQ show value	VDDQ design value
X	X	1.2V	1.209V
0	X	1.25V	1.256V
X	0	1.35V	1.362V
0	X	1.40V	1.413V

Title : VDDQ/VPPDDR
Engineer: Mandy
Project Name: coffeelake demo
Rev: R1.00
Date: Friday, May 15, 2020
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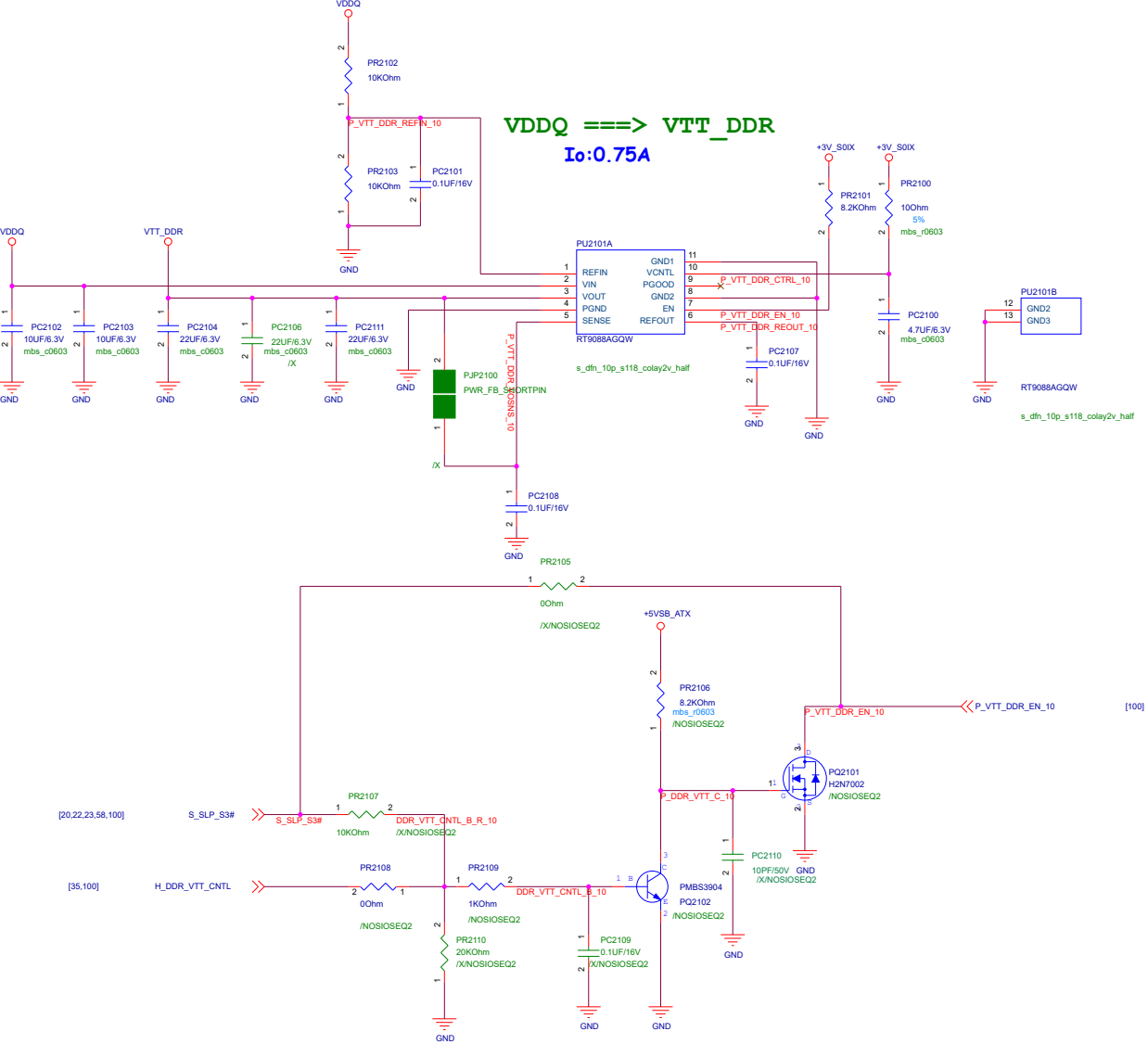
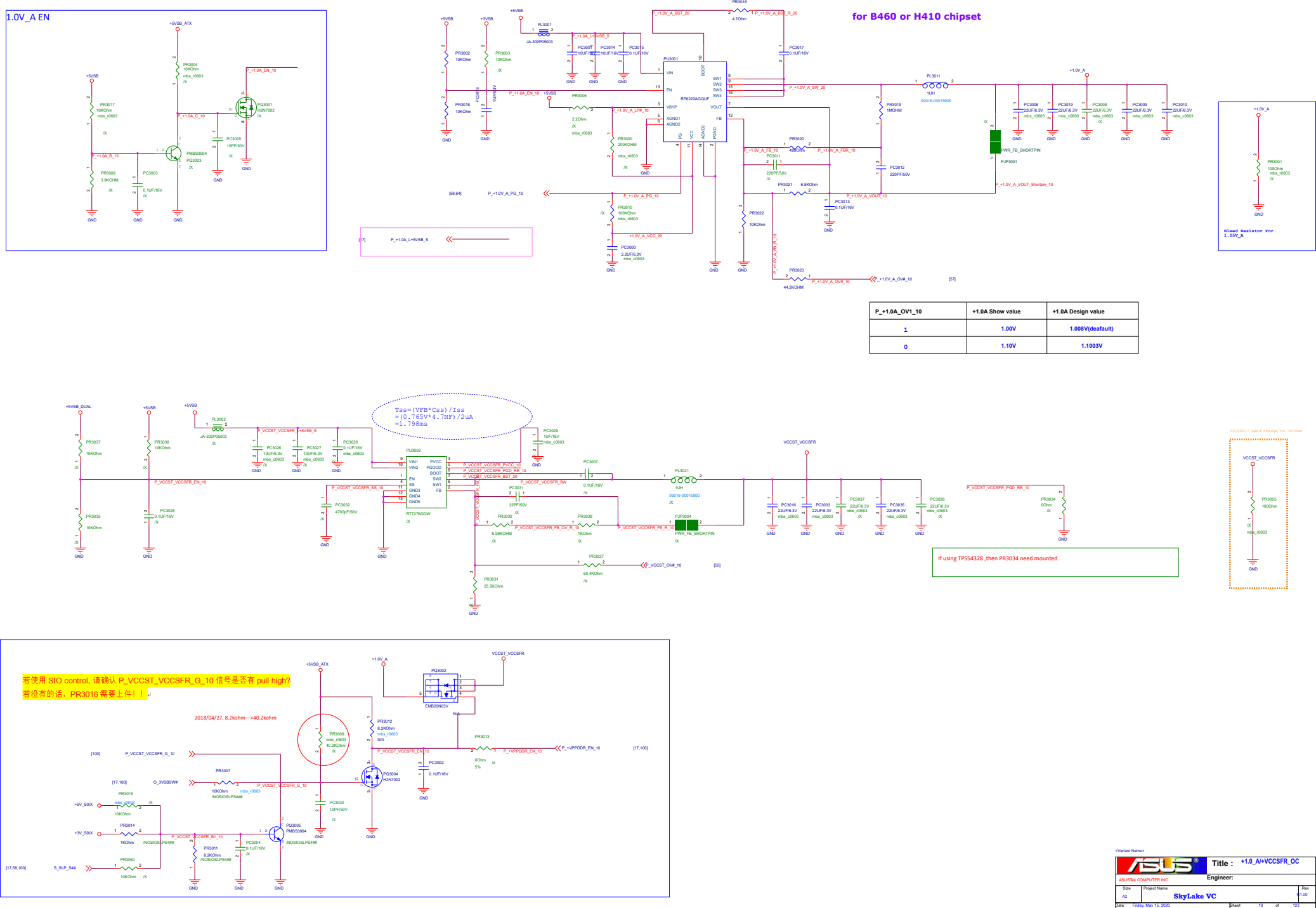


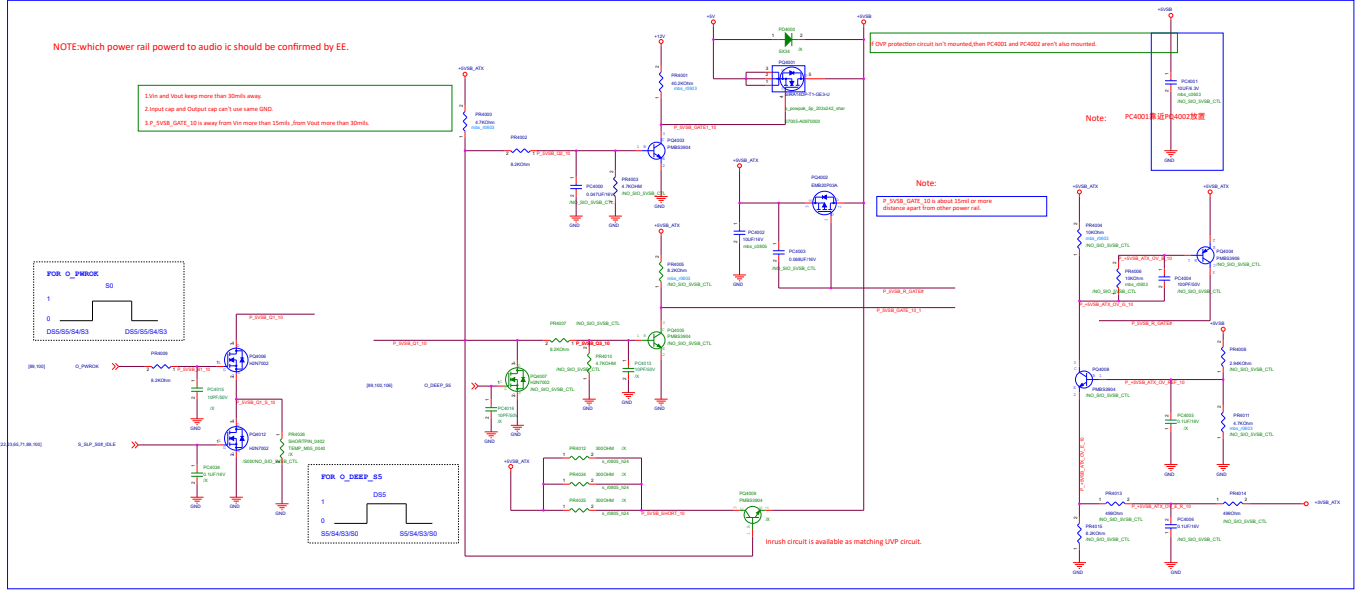
For 3*3 DFN 3A DDR4 terminator LDO（RT9088A and UP8815P）
1. Intel HXX series（比如:H110,H170,H270等）使用UPI UP8815P (P/N: 06094-00060000)
2. Intel other series(比如:BXX,ZXX,QXX等)和AMD Project使用RICHTEK RT9088A(P/N: 06094-00050000)

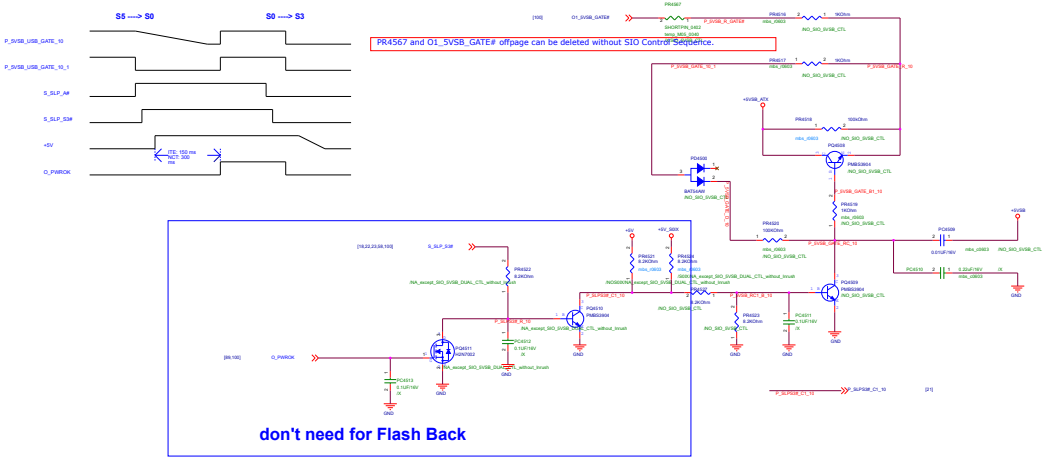
<Variant Name>

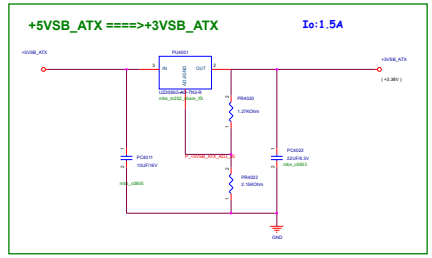
ASUSTek COMPUTER INC.	Title : VTT_DDR	
	Engineer: Mandy_Cao	
Size: A3	Project Name: coffeelake demo	Rev: R1.00
Date: Friday, May 15, 2020	Sheet 18 of 123	



P_+1.0A_OV1_10	+1.0A Show value	+1.0A Design value
1	1.00V	1.008V(deafault)
0	1.10V	1.1003V







ASUSTeK COMPUTER INC.	Title :	+5VSB+3VSB_ATX+1.5V_A	
	Engineer:	Mandy_cao	
Size: A1	Project Name:	coffeelake demo	Rev: 1.00
Date: Friday, May 15, 2020	Sheet: 20	of: 53	

1.Vin and Vout keep more than 30mils away.

2.Input cap and Output cap can't use same GND.

3.P_5VSB_GATE_10 is away from Vin more than 15mils ,from Vout more than 30mils.

If OVP protection circuit isn't mounted,then PC4501 isn't also mounted.

BOM	主板上+5VSB_DUAL上有接不耐12V高壓的元件且上件,例如用在 Type-C 上的 Power Switch G517 08016-01100500	主板上+5VSB_DUAL上沒有接不耐12V高壓的元件或者主板上+5VSB_DUAL上有接不耐12V高壓的元件但不上件
/5VSB_DUAL_OVP	mount	unmount

2016/06/30 modify +5VSB_ATX to +5VSB

PC4501靠近PQ4501放置

Note:

P_5VSB_USB_GATE_10 is about 15mil or more distance apart from other power rail.

Modify:2017/01/22, 5VSB DUAL UVP circuit unmounted

+5VSB_DUAL Inrush Circuit for USB Port default have Power

PR4566 and O1_5VSB_DUAL_GATE# offpage can be deleted without SIO Control Sequence.

Modify:2017/01/22,0.047uf to 0.01uf

S5 ----> S0

S0 ----> S3

P_5VSB_USB_GATE_10

P_5VSB_USB_GATE_10_1

S_SLP_A#

S_SLP_S3#

+5V

O_PWROK

ITE: 150 ms
NCT: 300 ms

<Variant Name>

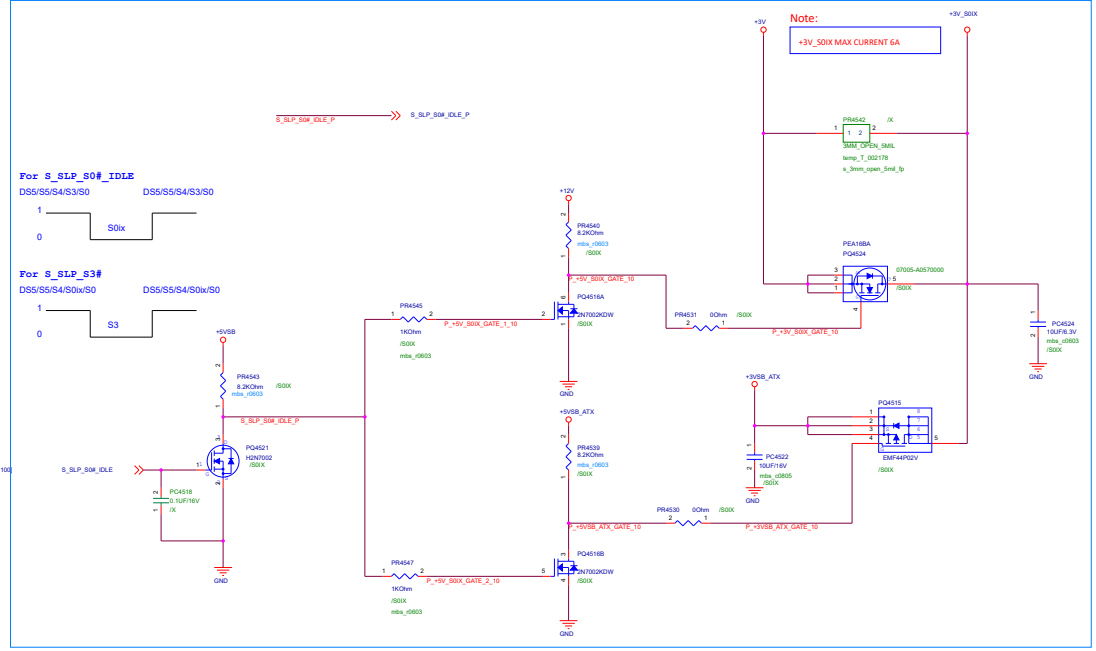
Title : +5VSB

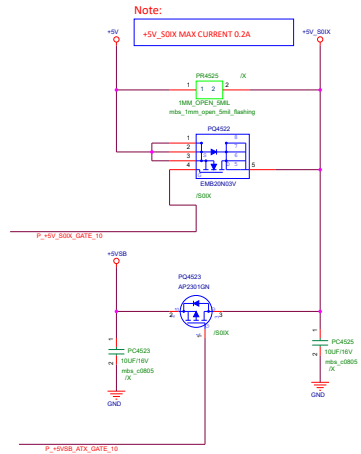
Engineer: Mandy_cao

ASUSTek COMPUTER INC.

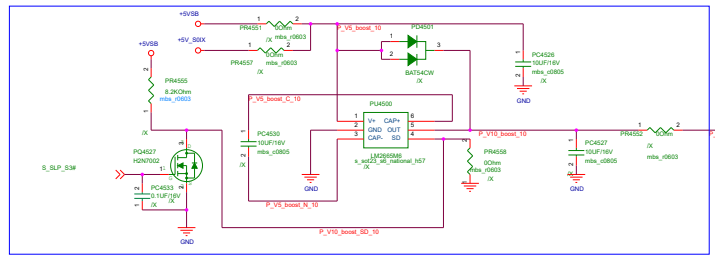
Size: A2 | Project Name: coffeelake demo | Rev: R1.00

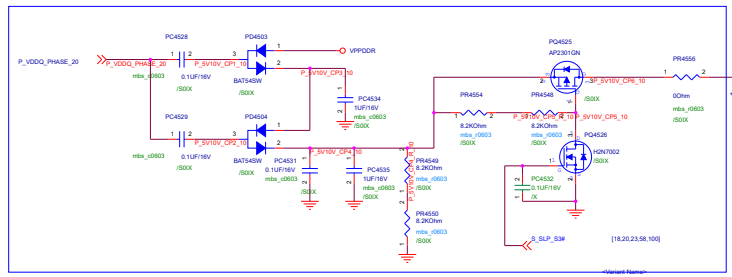
Date: Friday, May 15, 2020 | Sheet 21 of 123





P_VDDQ_PHASE_20 这根 net 请直接从 VDDQ phase shape 处拉出来，而非从 IC 的 phase pin 拉，降低 phase spike，使 end output 更精准。

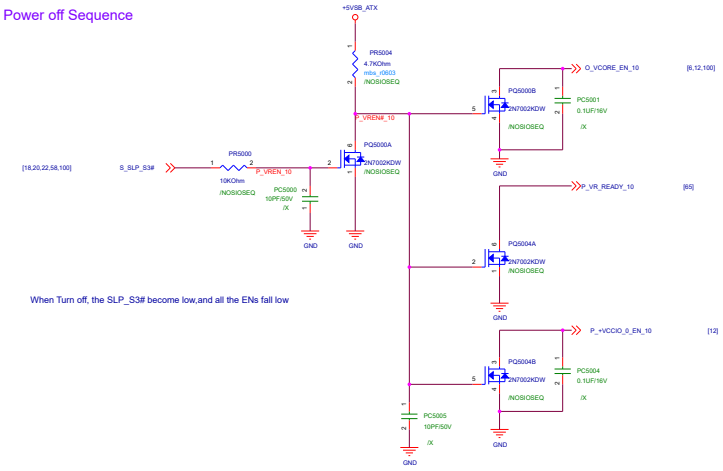




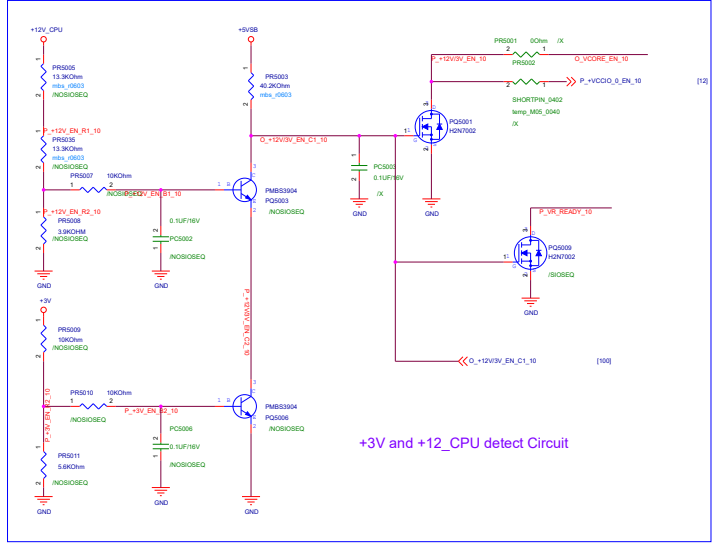
Variant Name

ASUSTEK COMPUTER INC	Title :	+3V_S0IX/+5V_S0IX/+12V_S0IX	
	Engineer:	Mandy_Cao	
Size: A2	Project Name: coffeelake demo		Rev: 0.0
Date: Friday, May 15, 2020	Sheet 22 of 123		

Power off Sequence



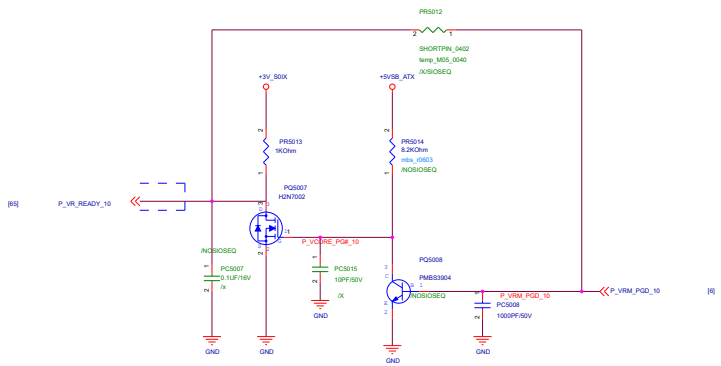
When Turn off, the SLP_S3# become low,and all the ENs fall low



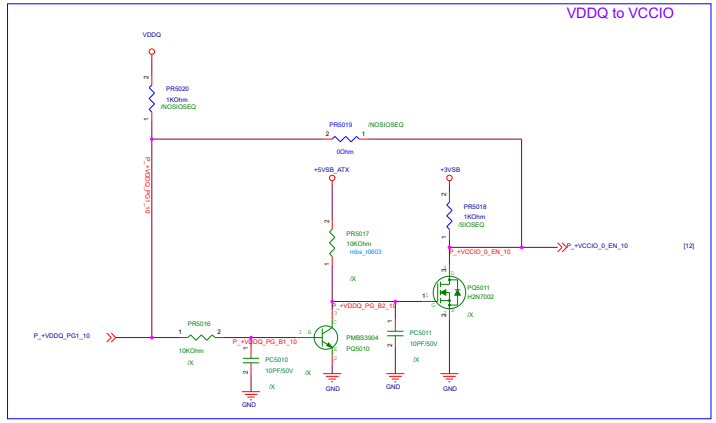
+3V and +12_CPU detect Circuit

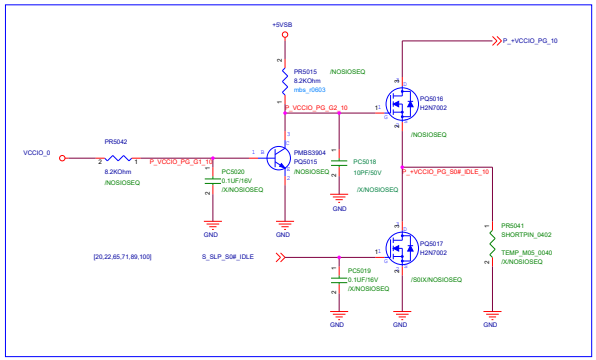
VR_PG de-glitch

P_VRM_PGD_10 don't need a resistive voltage divider in page vcore controller.



VDDQ to VCCIO



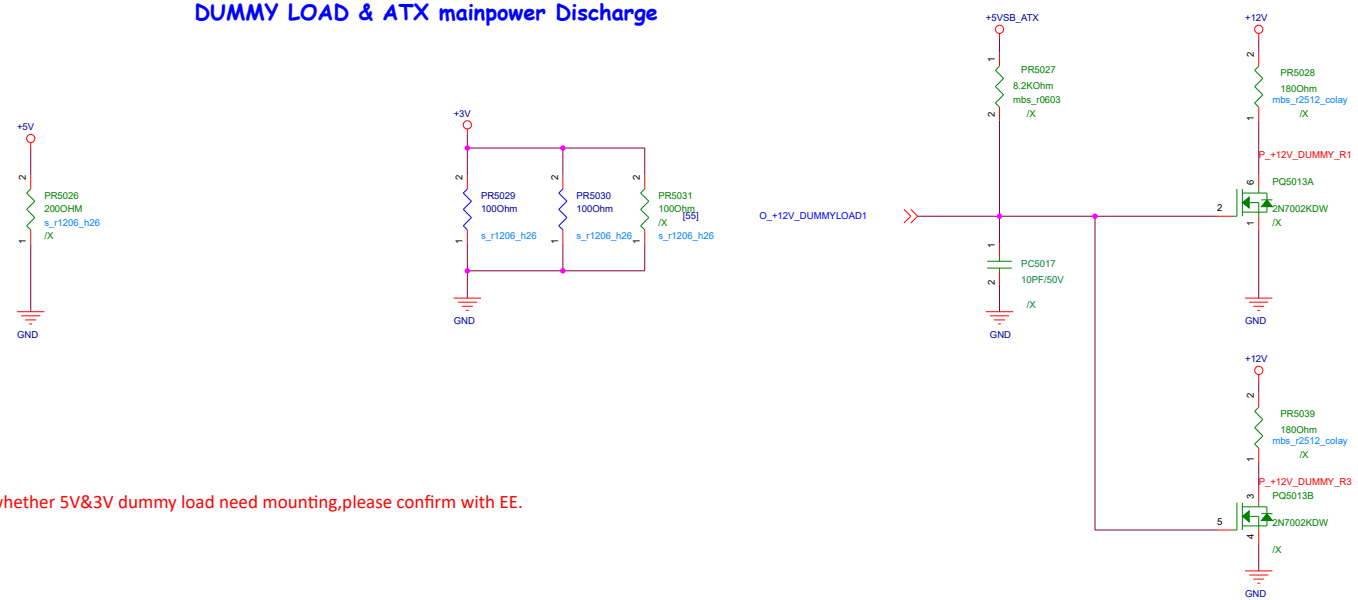


<Variant Name>

ASUSTek COMPUTER INC.	Title : Power Sequence		
	Engineer: Jun_Zhang		
Size: A2	Project Name: Coffeelake		Rev: 01.00
Date: Friday, May 15, 2020	Sheet 23 of 123		

Title <Title>		
Size B	Document Number <Doc>	Rev <RevCode>
Date: Thursday, April 30, 2020	Sheet 24 of 123	

DUMMY LOAD & ATX mainpower Discharge



whether 5V&3V dummy load need mounting,please confirm with EE.

<Variant Name>

ASUSTek COMPUTER INC.	Title : dummy load	
	Engineer: Mandy_cao	
Size: A3	Project Name: coffeelake demo	Rev: R1.00
Date: Friday, May 15, 2020	Sheet 25 of 123	

<Variant Name>

ASUSTek COMPUTER INC.	Title : NA	
	Engineer: Mandy_cao	
Size: A3	Project Name: KabyLake DEMO	Rev: R1.00
Date: Thursday, April 30, 2020	Sheet 26 of 123	

<Variant Name>

Title : +VCCCORE_3

ASUSTek COMPUTER INC.

Engineer: ChuKang

Size	Project Name	Rev
A2	KabyLake VC	R1.00

Date:	Thursday, April 30, 2020	Sheet	27	of	123

Title <Title>		
Size C	Document Number <Doc>	Rev <RevCode>
Date: Thursday, April 30, 2020	Sheet 28 of 123	

<Variant Name>

Title : VCCSTG

ASUSTek Computer Inc.

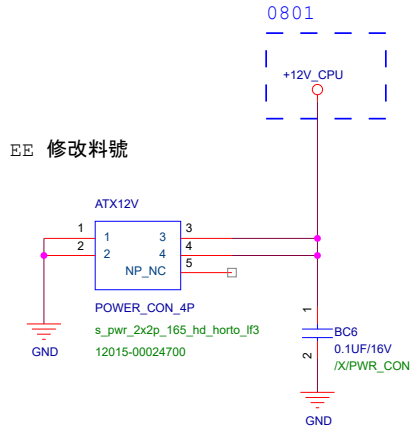
Engineer: Cisco

Size	Project Name	Rev
Custom	CometLake VC	R1.00

Date:	Thursday, April 30, 2020	Sheet	29	of	123

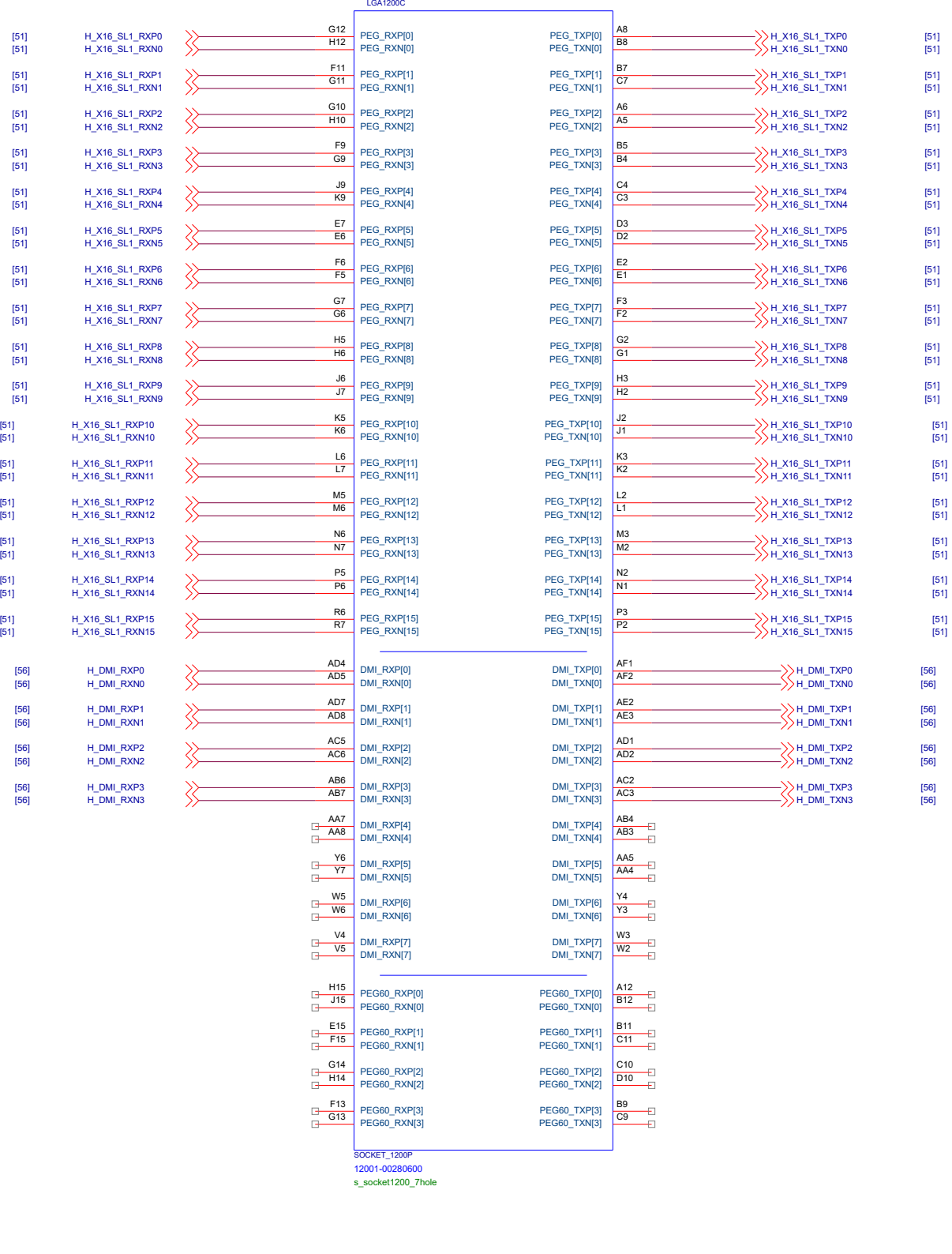
4 Pin +12V Connector

顏色：W



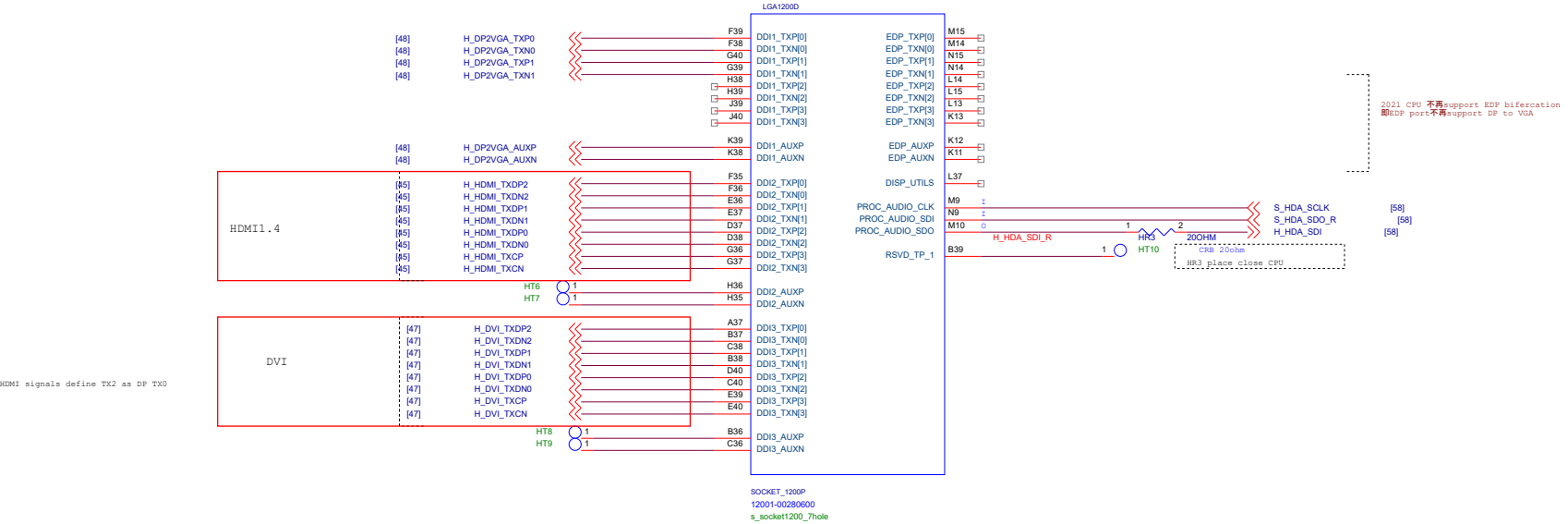
<Variant Name>

ASUSTek COMPUTER INC.	Title : +VCCCORE_3	
	Engineer: ChuKang	
Size: A3	Project Name: KabyLake VC	Rev: R1.00
Date: Thursday, April 30, 2020	Sheet 30 of 123	



ASUSTek Computer Inc.	Title :	LGA1151 (DMI/PEG)	
	Engineer:	Jay_Tong	
Size: A3	Project Name: CFL CHIPSET DEMO		Rev: R1.00
Date: Friday, May 29, 2020	Sheet 31 of 136		

若有VGA，按如下规则接入
例：display有HDMI,DVI,VGA,则將VGA接到DP的位置



ASUSTek Computer Inc.	Title : LGA1150 (FDI/DISPLAY)		
	Engineer: Bing-jie_Wang		
Size: A3	Project Name: SKYLAKE CHIPSET DEMO		Rev: R1.02A
Date: Friday, May 29, 2020	Sheet 32 of 136		

Channel A
4 Layer routing

LGA1200A

[39] D4_DQ_A[0:63]

DQ Follow CRB

AE39	DDR0_DQ[0]	D4_DQ_A5
AE38	DDR0_DQ[1]	D4_DQ_A4
AH39	DDR0_DQ[2]	D4_DQ_A7
AH38	DDR0_DQ[3]	D4_DQ_A3
AF40	DDR0_DQ[4]	D4_DQ_A1
AE40	DDR0_DQ[5]	D4_DQ_A0
AH40	DDR0_DQ[6]	D4_DQ_A2
AG40	DDR0_DQ[7]	D4_DQ_A6
AK39	DDR0_DQ[8]	D4_DQ_A8
AK40	DDR0_DQ[9]	D4_DQ_A13
AN39	DDR0_DQ[10]	D4_DQ_A10
AM40	DDR0_DQ[11]	D4_DQ_A14
AL40	DDR0_DQ[12]	D4_DQ_A9
AK38	DDR0_DQ[13]	D4_DQ_A12
AN40	DDR0_DQ[14]	D4_DQ_A15
AN38	DDR0_DQ[15]	D4_DQ_A11
AR39	DDR0_DQ[16]/DDR0_DQ[32]	D4_DQ_A21
AR40	DDR0_DQ[17]/DDR0_DQ[33]	D4_DQ_A20
AV39	DDR0_DQ[18]/DDR0_DQ[34]	D4_DQ_A22
AU40	DDR0_DQ[19]/DDR0_DQ[35]	D4_DQ_A17
AR38	DDR0_DQ[20]/DDR0_DQ[36]	D4_DQ_A19
AT40	DDR0_DQ[21]/DDR0_DQ[37]	D4_DQ_A16
AW38	DDR0_DQ[22]/DDR0_DQ[38]	D4_DQ_A18
AV38	DDR0_DQ[23]/DDR0_DQ[39]	D4_DQ_A23
AV36	DDR0_DQ[24]/DDR0_DQ[40]	D4_DQ_A28
AY36	DDR0_DQ[25]/DDR0_DQ[41]	D4_DQ_A24
AV33	DDR0_DQ[26]/DDR0_DQ[42]	D4_DQ_A31
AY34	DDR0_DQ[27]/DDR0_DQ[43]	D4_DQ_A30
AY35	DDR0_DQ[28]/DDR0_DQ[44]	D4_DQ_A25
AW36	DDR0_DQ[29]/DDR0_DQ[45]	D4_DQ_A29
AY33	DDR0_DQ[30]/DDR0_DQ[46]	D4_DQ_A26
AW33	DDR0_DQ[31]/DDR0_DQ[47]	D4_DQ_A27
AW11	DDR0_DQ[32]/DDR1_DQ[0]	D4_DQ_A36
AV11	DDR0_DQ[33]/DDR1_DQ[1]	D4_DQ_A37
AY7	DDR0_DQ[34]/DDR1_DQ[2]	D4_DQ_A34
AY8	DDR0_DQ[35]/DDR1_DQ[3]	D4_DQ_A38
AW9	DDR0_DQ[36]/DDR1_DQ[4]	D4_DQ_A33
AW10	DDR0_DQ[37]/DDR1_DQ[5]	D4_DQ_A32
AV7	DDR0_DQ[38]/DDR1_DQ[6]	D4_DQ_A35
AW7	DDR0_DQ[39]/DDR1_DQ[7]	D4_DQ_A39
AW5	DDR0_DQ[40]/DDR1_DQ[8]	D4_DQ_A40
AY5	DDR0_DQ[41]/DDR1_DQ[9]	D4_DQ_A45
AW2	DDR0_DQ[42]/DDR1_DQ[10]	D4_DQ_A47
AW3	DDR0_DQ[43]/DDR1_DQ[11]	D4_DQ_A46
AY4	DDR0_DQ[44]/DDR1_DQ[12]	D4_DQ_A41
AV5	DDR0_DQ[45]/DDR1_DQ[13]	D4_DQ_A44
AV1	DDR0_DQ[46]/DDR1_DQ[14]	D4_DQ_A43
AV2	DDR0_DQ[47]/DDR1_DQ[15]	D4_DQ_A42
AT1	DDR0_DQ[48]/DDR1_DQ[32]	D4_DQ_A48
AN1	DDR0_DQ[49]/DDR1_DQ[33]	D4_DQ_A50
AT3	DDR0_DQ[50]/DDR1_DQ[34]	D4_DQ_A52
AP1	DDR0_DQ[51]/DDR1_DQ[35]	D4_DQ_A54
AT2	DDR0_DQ[52]/DDR1_DQ[36]	D4_DQ_A53
AN3	DDR0_DQ[53]/DDR1_DQ[37]	D4_DQ_A51
AR1	DDR0_DQ[54]/DDR1_DQ[38]	D4_DQ_A49
AN2	DDR0_DQ[55]/DDR1_DQ[39]	D4_DQ_A55
AL2	DDR0_DQ[56]/DDR1_DQ[40]	D4_DQ_A56
AH1	DDR0_DQ[57]/DDR1_DQ[41]	D4_DQ_A58
AL3	DDR0_DQ[58]/DDR1_DQ[42]	D4_DQ_A60
AJ1	DDR0_DQ[59]/DDR1_DQ[43]	D4_DQ_A62
AH3	DDR0_DQ[60]/DDR1_DQ[44]	D4_DQ_A59
AL1	DDR0_DQ[61]/DDR1_DQ[45]	D4_DQ_A61
AH2	DDR0_DQ[62]/DDR1_DQ[46]	D4_DQ_A63
AK1	DDR0_DQ[63]/DDR1_DQ[47]	D4_DQ_A57

suppor ECC

AL30	DDR0_ECC[0]	
AM30	DDR0_ECC[1]	
AM31	DDR0_ECC[2]	
AL32	DDR0_ECC[3]	
AK32	DDR0_ECC[4]	
AJ32	DDR0_ECC[5]	
AM32	DDR0_ECC[6]	
AK30	DDR0_ECC[7]	

AC40	DDR_VREF_CA[0]	
AC38	DDR_VREF_CA[1]	

HT28 1 H_D4_VREFCA_A0
H_D4_VREFCA_A1

AU24	DDR0_CKP[0]	D4_MA_CLK0 [39]
AV24	DDR0_CKN[0]	D4_MA_CLK#0 [39]
AY23	DDR0_CKP[1]	D4_MA_CLK1 [39]
AW23	DDR0_CKN[1]	D4_MA_CLK#1 [39]
AT19	DDR0_CKP[2]	
AU19	DDR0_CKN[2]	
AY18	DDR0_CKP[3]	
AW18	DDR0_CKN[3]	
AY31	DDR0_CKE[0]	D4_CKE_A0 [39]
AW31	DDR0_CKE[1]	D4_CKE_A1 [39]
AV30	DDR0_CKE[2]	
AV31	DDR0_CKE[3]	
AY15	DDR0_CS#[0]	D4_CS_A#0 [39]
AY13	DDR0_CS#[1]	D4_CS_A#1 [39]
AV15	DDR0_CS#[2]	
AV13	DDR0_CS#[3]	
AY14	DDR0_ODT[0]	D4_ODT_A0 [39]
AV14	DDR0_ODT[1]	D4_ODT_A1 [39]
AU14	DDR0_ODT[2]	
AT14	DDR0_ODT[3]	
AY16	DDR0_BA[0]	D4_BAA0 [39]
AW17	DDR0_BA[1]	D4_BAA1 [39]
AV29	DDR0_BG[0]	D4_BGA0 [39]
AW29	DDR0_BG[1]	D4_BGA1 [39]
AY16	DDR0_MA[16]	D4_MAA16
AW16	DDR0_MA[14]	D4_MAA14
AU16	DDR0_MA[15]	D4_MAA15
AU18	DDR0_MA[0]	D4_MAA0
AY25	DDR0_MA[1]	D4_MAA1
AY24	DDR0_MA[2]	D4_MAA2
AW25	DDR0_MA[3]	D4_MAA3
AV25	DDR0_MA[4]	D4_MAA4
AY26	DDR0_MA[5]	D4_MAA5
AV26	DDR0_MA[6]	D4_MAA6
AY27	DDR0_MA[7]	D4_MAA7
AW27	DDR0_MA[8]	D4_MAA8
AY28	DDR0_MA[9]	D4_MAA9
AU17	DDR0_MA[10]	D4_MAA10
AV27	DDR0_MA[11]	D4_MAA11
AV28	DDR0_MA[12]	D4_MAA12
AW14	DDR0_MA[13]	D4_MAA13

D4_MAA[0:16] [39]

AY30	DDR0_ACT#	D4_A_ACT# [39]
AV18	DDR0_PAR	D4_A_PAR [39]
AY29	DDR0_ALERT#	D4_A_ALERT# [39]

AF38	DDR0_DQSN[0]	D4_DQS_A#0	D4_DQS_A#0 [39]
AL38	DDR0_DQSN[1]	D4_DQS_A#1	D4_DQS_A#1 [39]
AT38	DDR0_DQSN[2]/DDR0_DQSN[4]	D4_DQS_A#2	D4_DQS_A#2 [39]
AV35	DDR0_DQSN[3]/DDR0_DQSN[5]	D4_DQS_A#3	D4_DQS_A#3 [39]
AV9	DDR0_DQSN[4]/DDR1_DQSN[0]	D4_DQS_A#4	D4_DQS_A#4 [39]
AV4	DDR0_DQSN[5]/DDR1_DQSN[1]	D4_DQS_A#5	D4_DQS_A#5 [39]
AR3	DDR0_DQSN[6]/DDR1_DQSN[4]	D4_DQS_A#6	D4_DQS_A#6 [39]
AK3	DDR0_DQSN[7]/DDR1_DQSN[5]	D4_DQS_A#7	D4_DQS_A#7 [39]
AG38	DDR0_DQSP[0]	D4_DQS_A0	D4_DQS_A0 [39]
AM38	DDR0_DQSP[1]	D4_DQS_A1	D4_DQS_A1 [39]
AU38	DDR0_DQSP[2]/DDR0_DQSP[4]	D4_DQS_A2	D4_DQS_A2 [39]
AV34	DDR0_DQSP[3]/DDR0_DQSP[5]	D4_DQS_A3	D4_DQS_A3 [39]
AV8	DDR0_DQSP[4]/DDR1_DQSP[0]	D4_DQS_A4	D4_DQS_A4 [39]
AV3	DDR0_DQSP[5]/DDR1_DQSP[1]	D4_DQS_A5	D4_DQS_A5 [39]
AP3	DDR0_DQSP[6]/DDR1_DQSP[4]	D4_DQS_A6	D4_DQS_A6 [39]
AJ3	DDR0_DQSP[7]/DDR1_DQSP[5]	D4_DQS_A7	D4_DQS_A7 [39]
AJ30	DDR0_DQSP[8]		
AJ31	DDR0_DQSN[8]	ECC DQS	

SOCKET_1200P
12001-00280600
s_socket1200_7hole

VREF FROM CPU PIN AC40 TO CHA DIMM0

H_D4_VREFCA_A0 D4R11 1 2 2Ohm D4_VREFCA_A0 [41]

D4C1 0.022UF/16V

D4R13 24.9Ohm

High frequency termination, can absorb any high frequency noise coming from CPU/board crosstalk.

GND

ASUSTek Computer Inc.	Title : LGA1151 (DDR4_A Control)		
	Engineer: Eason		
Size: A3	Project Name: KabyLake VC		Rev: R1.03B
Date: Friday, May 29, 2020	Sheet 33 of 136		

Channel B
4 Layer routing

[40] D4_DQ_B[0:63]

LGA1200B

DQ Follow CRB

AD34	D4_DQ_B4	DDR1_DQ[0]/DDR0_DQ[16]
AD35	D4_DQ_B5	DDR1_DQ[1]/DDR0_DQ[17]
AE36	D4_DQ_B1	DDR1_DQ[2]/DDR0_DQ[18]
AF36	D4_DQ_B6	DDR1_DQ[3]/DDR0_DQ[19]
AG35	D4_DQ_B3	DDR1_DQ[4]/DDR0_DQ[20]
AG34	D4_DQ_B7	DDR1_DQ[5]/DDR0_DQ[21]
AD36	D4_DQ_B0	DDR1_DQ[6]/DDR0_DQ[22]
AG36	D4_DQ_B2	DDR1_DQ[7]/DDR0_DQ[23]
AJ36	D4_DQ_B13	DDR1_DQ[8]/DDR0_DQ[24]
AJ35	D4_DQ_B8	DDR1_DQ[9]/DDR0_DQ[25]
AL36	D4_DQ_B14	DDR1_DQ[10]/DDR0_DQ[26]
AM35	D4_DQ_B10	DDR1_DQ[11]/DDR0_DQ[27]
AK36	D4_DQ_B9	DDR1_DQ[12]/DDR0_DQ[28]
AJ34	D4_DQ_B12	DDR1_DQ[13]/DDR0_DQ[29]
AM36	D4_DQ_B15	DDR1_DQ[14]/DDR0_DQ[30]
AM34	D4_DQ_B11	DDR1_DQ[15]/DDR0_DQ[31]
AT36	D4_DQ_B17	DDR1_DQ[16]/DDR0_DQ[48]
AP36	D4_DQ_B20	DDR1_DQ[17]/DDR0_DQ[49]
AT34	D4_DQ_B22	DDR1_DQ[18]/DDR0_DQ[50]
AP33	D4_DQ_B19	DDR1_DQ[19]/DDR0_DQ[51]
AR36	D4_DQ_B16	DDR1_DQ[20]/DDR0_DQ[52]
AT35	D4_DQ_B21	DDR1_DQ[21]/DDR0_DQ[53]
AR33	D4_DQ_B23	DDR1_DQ[22]/DDR0_DQ[54]
AT33	D4_DQ_B18	DDR1_DQ[23]/DDR0_DQ[55]
AP31	D4_DQ_B28	DDR1_DQ[24]/DDR0_DQ[56]
AT31	D4_DQ_B29	DDR1_DQ[25]/DDR0_DQ[57]
AT29	D4_DQ_B30	DDR1_DQ[26]/DDR0_DQ[58]
AP28	D4_DQ_B27	DDR1_DQ[27]/DDR0_DQ[59]
AR31	D4_DQ_B24	DDR1_DQ[28]/DDR0_DQ[60]
AT30	D4_DQ_B25	DDR1_DQ[29]/DDR0_DQ[61]
AR28	D4_DQ_B31	DDR1_DQ[30]/DDR0_DQ[62]
AT28	D4_DQ_B26	DDR1_DQ[31]/DDR0_DQ[63]
AT12	D4_DQ_B37	DDR1_DQ[32]/DDR1_DQ[16]
AR12	D4_DQ_B33	DDR1_DQ[33]/DDR1_DQ[17]
AT10	D4_DQ_B34	DDR1_DQ[34]/DDR1_DQ[18]
AR10	D4_DQ_B39	DDR1_DQ[35]/DDR1_DQ[19]
AP12	D4_DQ_B36	DDR1_DQ[36]/DDR1_DQ[20]
AT11	D4_DQ_B32	DDR1_DQ[37]/DDR1_DQ[21]
AP10	D4_DQ_B38	DDR1_DQ[38]/DDR1_DQ[22]
AN10	D4_DQ_B35	DDR1_DQ[39]/DDR1_DQ[23]
AR8	D4_DQ_B40	DDR1_DQ[40]/DDR1_DQ[24]
AT8	D4_DQ_B45	DDR1_DQ[41]/DDR1_DQ[25]
AT5	D4_DQ_B42	DDR1_DQ[42]/DDR1_DQ[26]
AT6	D4_DQ_B46	DDR1_DQ[43]/DDR1_DQ[27]
AP8	D4_DQ_B44	DDR1_DQ[44]/DDR1_DQ[28]
AT7	D4_DQ_B41	DDR1_DQ[45]/DDR1_DQ[29]
AP5	D4_DQ_B47	DDR1_DQ[46]/DDR1_DQ[30]
AR5	D4_DQ_B43	DDR1_DQ[47]/DDR1_DQ[31]
AM8	D4_DQ_B52	DDR1_DQ[48]
AM7	D4_DQ_B53	DDR1_DQ[49]
AK6	D4_DQ_B54	DDR1_DQ[50]
AM5	D4_DQ_B48	DDR1_DQ[51]
AM6	D4_DQ_B49	DDR1_DQ[52]
AK7	D4_DQ_B51	DDR1_DQ[53]
AK5	D4_DQ_B55	DDR1_DQ[54]
AL5	D4_DQ_B50	DDR1_DQ[55]
AF7	D4_DQ_B58	DDR1_DQ[56]
AH8	D4_DQ_B60	DDR1_DQ[57]
AG5	D4_DQ_B62	DDR1_DQ[58]
AF6	D4_DQ_B59	DDR1_DQ[59]
AH6	D4_DQ_B57	DDR1_DQ[60]
AH7	D4_DQ_B56	DDR1_DQ[61]
AF5	D4_DQ_B63	DDR1_DQ[62]
AH5	D4_DQ_B61	DDR1_DQ[63]

Suppor ECC

AJ28		DDR1_ECC[0]
AK26		DDR1_ECC[1]
AL26		DDR1_ECC[2]
AM28		DDR1_ECC[3]
AK28		DDR1_ECC[4]
AL28		DDR1_ECC[5]
AM27		DDR1_ECC[6]
AM26		DDR1_ECC[7]

AC39		DDR_VREF_CA[2]
AB40		DDR_VREF_CA[3]

HT27 1 H_D4_VREFCA_B0 / H_D4_VREFCA_B1

DDR1_CKP[0]	AT23	D4_MB_CLK0 [40]
DDR1_CKN[0]	AU23	D4_MB_CLK#0 [40]
DDR1_CKP[1]	AV22	D4_MB_CLK1 [40]
DDR1_CKN[1]	AU22	D4_MB_CLK#1 [40]
DDR1_CKP[2]	AT21	
DDR1_CKN[2]	AU21	
DDR1_CKP[3]	AU20	
DDR1_CKN[3]	AV20	
DDR1_CKE[0]	AT25	D4_CKE_B0 [40]
DDR1_CKE[1]	AR26	D4_CKE_B1 [40]
DDR1_CKE[2]	AT26	
DDR1_CKE[3]	AP26	
DDR1_CS#[0]	AN17	D4_CS_B#0 [40]
DDR1_CS#[1]	AN15	D4_CS_B#1 [40]
DDR1_CS#[2]	AR16	
DDR1_CS#[3]	AM15	
DDR1_ODT[0]	AM17	D4_ODT_B0 [40]
DDR1_ODT[1]	AP14	D4_ODT_B1 [40]
DDR1_ODT[2]	AM16	
DDR1_ODT[3]	AM14	
DDR1_BA[0]	AP18	D4_BAB0 [40]
DDR1_BA[1]	AN19	D4_BAB1 [40]
DDR1_BG[0]	AM23	D4_BGB0 [40]
DDR1_BG[1]	AM22	D4_BGB1 [40]
DDR1_MA[16]	AM18	
DDR1_MA[14]	AP17	D4_MAB16
DDR1_MA[15]	AP16	D4_MAB14
		D4_MAB15
DDR1_MA[0]	AP19	
DDR1_MA[1]	AP20	D4_MAB0
DDR1_MA[2]	AR20	D4_MAB1
DDR1_MA[3]	AM20	D4_MAB2
DDR1_MA[4]	AP21	D4_MAB3
DDR1_MA[5]	AN21	D4_MAB4
DDR1_MA[6]	AR22	D4_MAB5
DDR1_MA[7]	AM21	D4_MAB6
DDR1_MA[8]	AP22	D4_MAB7
DDR1_MA[9]	AN23	D4_MAB8
DDR1_MA[10]	AR18	D4_MAB9
DDR1_MA[11]	AP23	D4_MAB10
DDR1_MA[12]	AR24	D4_MAB11
DDR1_MA[13]	AP15	D4_MAB12
		D4_MAB13

D4_MAB[0:16] [40]

DDR1_ACT#	AP25	D4_B_ACT# [40]
DDR1_PAR	AM19	D4_B_PAR [40]
DDR1_ALERT#	AP24	D4_B_ALERT# [40]

DDR1_DQSN[0]/DDR0_DQSN[2]	AE34	D4_DQS_B#0 [40]
DDR1_DQSN[1]/DDR0_DQSN[3]	AK34	D4_DQS_B#1 [40]
DDR1_DQSN[2]/DDR0_DQSN[6]	AP35	D4_DQS_B#2 [40]
DDR1_DQSN[3]/DDR0_DQSN[7]	AP30	D4_DQS_B#3 [40]
DDR1_DQSN[4]/DDR1_DQSN[2]	AN12	D4_DQS_B#4 [40]
DDR1_DQSN[5]/DDR1_DQSN[3]	AP7	D4_DQS_B#5 [40]
DDR1_DQSN[6]	AL8	D4_DQS_B#6 [40]
DDR1_DQSN[7]	AG8	D4_DQS_B#7 [40]
DDR1_DQSP[0]/DDR0_DQSP[2]	AF34	D4_DQS_B0 [40]
DDR1_DQSP[1]/DDR0_DQSP[3]	AL34	D4_DQS_B1 [40]
DDR1_DQSP[2]/DDR0_DQSP[6]	AP34	D4_DQS_B2 [40]
DDR1_DQSP[3]/DDR0_DQSP[7]	AP29	D4_DQS_B3 [40]
DDR1_DQSP[4]/DDR1_DQSP[2]	AN11	D4_DQS_B4 [40]
DDR1_DQSP[5]/DDR1_DQSP[3]	AP6	D4_DQS_B5 [40]
DDR1_DQSP[6]	AK8	D4_DQS_B6 [40]
DDR1_DQSP[7]	AF8	D4_DQS_B7 [40]
DDR1_DQSP[8]	AJ27	
DDR1_DQSN[8]	AJ26	

ECC DQS

SOCKET_1200P
12001-00280600
s_socket1200_7hole

VREF FROM CPU PIN AC39 **TO CHB DIMM0**

H_D4_VREFCA_B0 — D4R15 2Ohm (1, 2) — D4_VREFCA_B0 [41]

D4C3 0.022UF/16V

D4R17 24.9Ohm

GND

High frequency termination, can absorb any high frequency noise coming from CPU/board crosstalk.

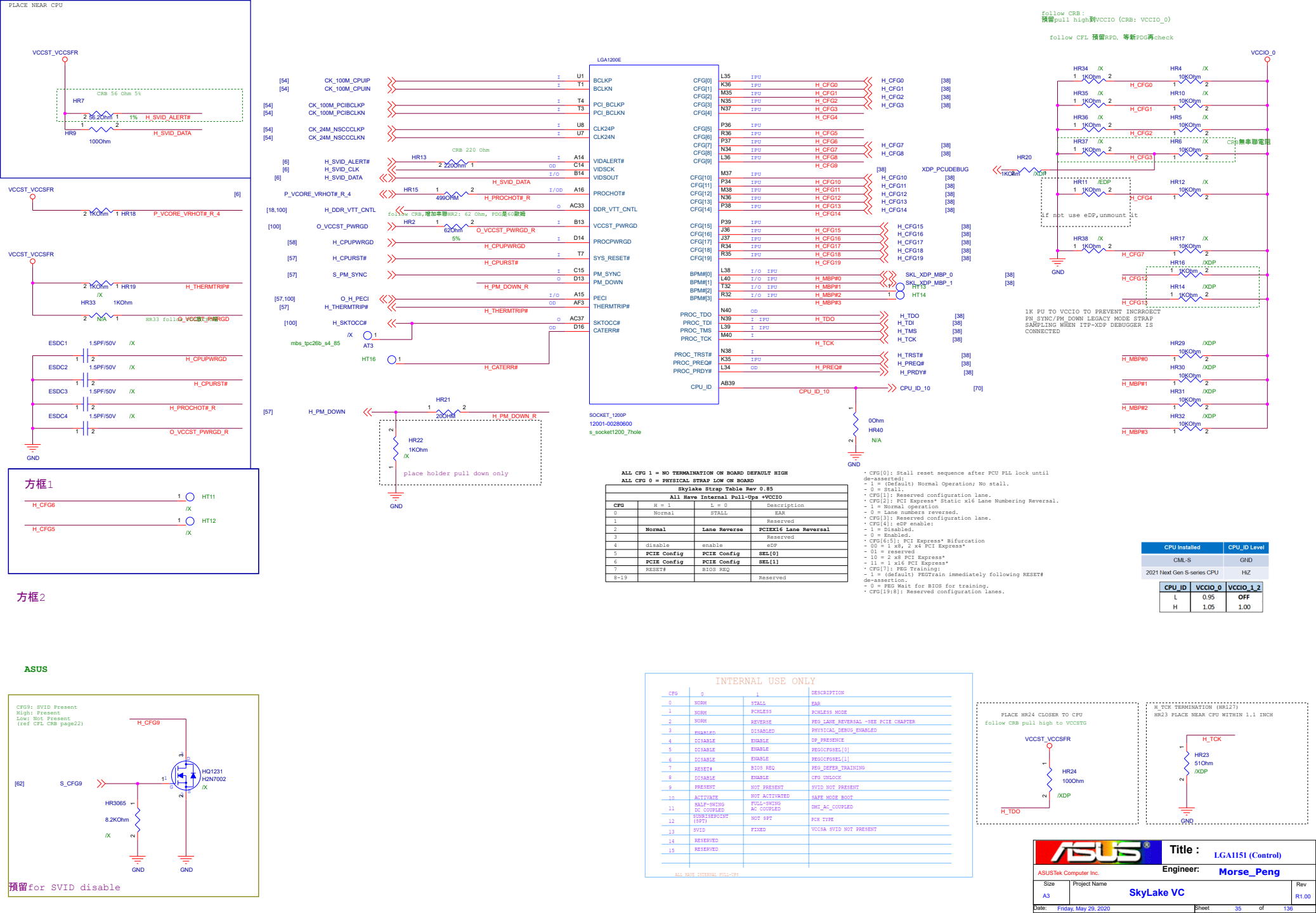
ASUSTek Computer Inc.

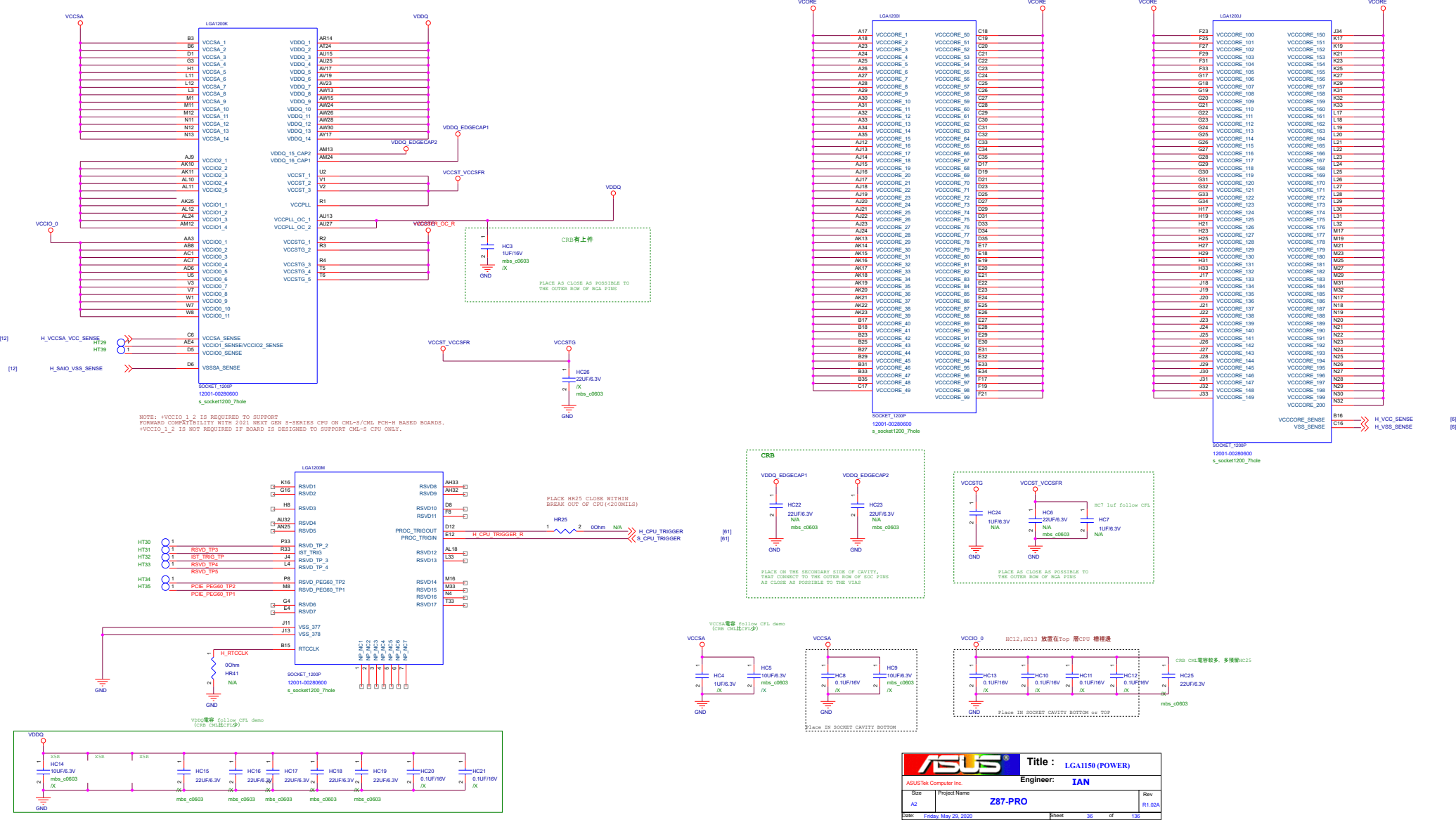
Title : LGA1151 (DDR4_B Control)

Engineer: Eason

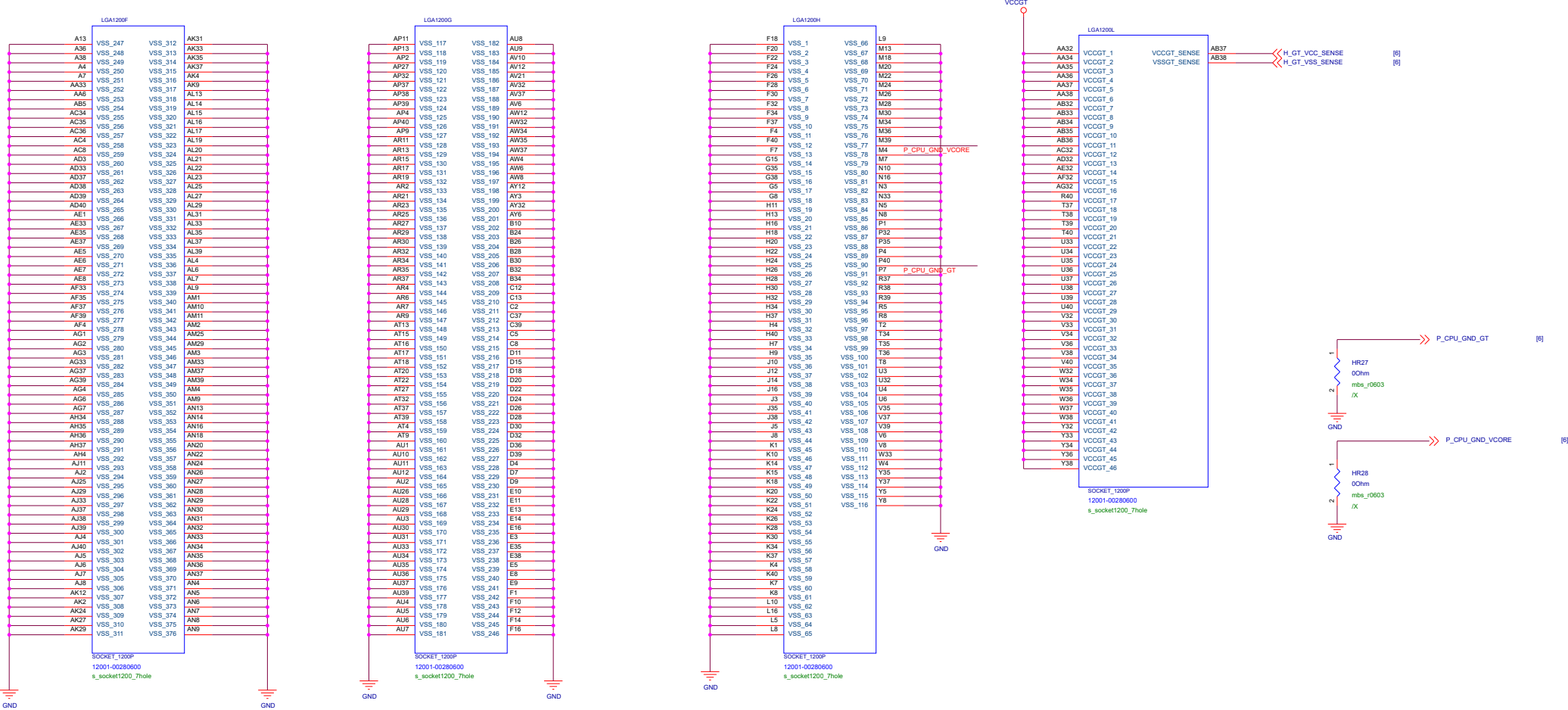
Size	Project Name	Rev
A3	KabyLake VC	R1.03B

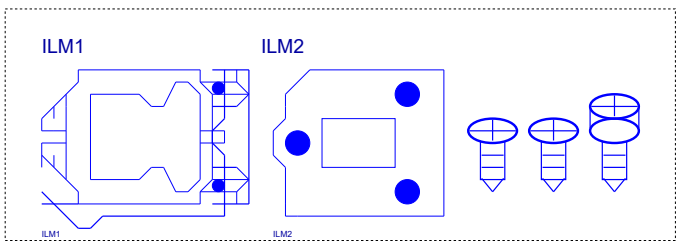
Date: Friday, May 29, 2020 Sheet 34 of 136


PLACE NEAR CPU
VCCST_VCCSFR
CRB 56 Ohm 5%
HR7
56.2Ohm
1%
H_SVID_ALERT#
HR9
100Ohm
H_SVID_DATA
VCCST_VCCSFR
[6]
1KOhm
HR18
P_VCORE_VRHOT#_R_4
VCCST_VCCSFR
1KOhm
HR19
H_THERMTRIP#
/X
HR33
1KOhm
N/A
HR33 follow O_VCCST_PWRGD
ESDC1
1.5PF/50V
/X
H_CPUPWRGD
ESDC2
H_CPURST#
ESDC3
H_PROCHOT#_R
ESDC4
O_VCCST_PWRGD_R
GND
方框1
HT11
H_CFG6
HT12
H_CFG5
方框2
ASUS
CFG9: SVID Present
High: Present
Low: Not Present
(ref CFL CRB page22)
H_CFG9
[62]
S_CFG9
HQ1231
H2N7002
HR3065
8.2KOhm
GND
預留for SVID disable
LGA1200E
[54] CK_100M_CPUIP
[54] CK_100M_CPUIN
[54] CK_100M_PCIBCLKP
[54] CK_100M_PCIBCLKN
[54] CK_24M_NSCCCLKP
[54] CK_24M_NSCCCLKN
CRB 220 Ohm
[6] H_SVID_ALERT#
[6] H_SVID_CLK
[6] H_SVID_DATA
HR13
220Ohm
P_VCORE_VRHOT#_R_4
HR15
499OHM
H_PROCHOT#_R
[18,100] H_DDR_VTT_CNTL
follow CRB,增加串聯HR2: 62 Ohm, PDG是60歐姆
[100] O_VCCST_PWRGD
HR2
62Ohm
5%
O_VCCST_PWRGD_R
[58] H_CPUPWRGD
H_CPUPWRGD
[57] H_CPURST#
H_CPURST#
[57] S_PM_SYNC
H_PM_DOWN_R
[57,100] O_H_PECI
[57] H_THERMTRIP#
H_THERMTRIP#
[100] H_SKTOCC#
/X
mbs_tpc26b_s4_85
AT3
HT16
H_CATERR#
[57] H_PM_DOWN
HR21
200OHM
H_PM_DOWN_R
HR22
1KOhm
/X
place holder pull down only
GND
BCLKP
BCLKN
PCI_BCLKP
PCI_BCLKN
CLK24P
CLK24N
VIDALERT#
VIDSCK
VIDSOUT
PROCHOT#
DDR_VTT_CNTL
VCCST_PWRGD
PROCPWRGD
SYS_RESET#
PM_SYNC
PM_DOWN
PECI
THERMTRIP#
SKTOCC#
CATERR#
CFG[0]
CFG[1]
CFG[2]
CFG[3]
CFG[4]
CFG[5]
CFG[6]
CFG[7]
CFG[8]
CFG[9]
CFG[10]
CFG[11]
CFG[12]
CFG[13]
CFG[14]
CFG[15]
CFG[16]
CFG[17]
CFG[18]
CFG[19]
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
PROC_TDO
PROC_TDI
PROC_TMS
PROC_TCK
PROC_TRST#
PROC_PREQ#
PROC_PRDY#
CPU_ID
SOCKET_1200P
12001-00280600
s_socket1200_7hole
H_CFG0
H_CFG1
H_CFG2
H_CFG3
H_CFG4
H_CFG5
H_CFG6
H_CFG7
H_CFG8
H_CFG9
H_CFG10
H_CFG11
H_CFG12
H_CFG13
H_CFG14
H_CFG15
H_CFG16
H_CFG17
H_CFG18
H_CFG19
SKL_XDP_MBP_0
SKL_XDP_MBP_1
HT13
HT14
H_MBP#0
H_MBP#1
H_MBP#2
H_MBP#3
H_TDO
H_TDI
H_TMS
H_TCK
H_TRST#
H_PREQ#
H_PRDY#
CPU_ID_10
[70]
0Ohm
HR40
N/A
follow CRB :
預留pull high到VCCIO (CRB: VCCIO_0)
follow CFL 預留RPD, 等新PDG再check
VCCIO_0
HR34 /X
HR35 /X
HR36 /X
HR37 /X
HR4 /X
HR10 /X
HR5 /X
HR6 /X
CRB無串聯電阻
HR20
/XDP
HR11 /EDP
HR12 /X
If not use eDP,unmount it
HR38 /X
HR17 /X
HR16 /XDP
HR14 /XDP
HR29 /XDP
HR30 /XDP
HR31 /XDP
HR32 /XDP
1K PU TO VCCIO TO PREVENT INCROECT
PN SYNC/PM_DOWN LEGACY MODE STRAP
SAMPLING WHEN ITP-XDP DEBUGGER IS
CONNECTED
ALL CFG 1 = NO TERMAINATION ON BOARD DEFAULT HIGH
ALL CFG 0 = PHYSICAL STRAP LOW ON BOARD
Skylake Strap Table Rev 0.85
All Have Internal Pull-Ups +VCCIO
CFG | H = 1 | L = 0 | Description
0 | Normal | STALL | EAR
1 | | | Reserved
2 | Normal | Lane Reverse | PCIEX16 Lane Reversal
3 | | | Reserved
4 | disable | enable | eDP
5 | PCIE Config | PCIE Config | SEL[0]
6 | PCIE Config | PCIE Config | SEL[1]
7 | RESET# | BIOS REQ |
8-19 | | | Reserved
· CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted;
- 1 = (Default) Normal Operation; No stall.
- 0 = Stall.
· CFG[1]: Reserved configuration lane.
· CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
- 1 = Normal operation
- 0 = Lane numbers reversed.
· CFG[3]: Reserved configuration lane.
· CFG[4]: eDP enable:
- 1 = Disabled.
- 0 = Enabled.
· CFG[6:5]: PCI Express* Bifurcation
- 00 = 1 x8, 2 x4 PCI Express*
- 01 = reserved
- 10 = 2 x8 PCI Express*
- 11 = 1 x16 PCI Express*
· CFG[7]: PEG Training:
- 1 = (default) PEGTrain immediately following RESET# de-assertion.
- 0 = PEG Wait for BIOS for training.
· CFG[19:8]: Reserved configuration lanes.
CPU Installed | CPU_ID Level
CML-S | GND
2021 Next Gen S-series CPU | HiZ
CPU_ID | VCCIO_0 | VCCIO_1_2
L | 0.95 | OFF
H | 1.05 | 1.00
INTERNAL USE ONLY
CFG | 0 | 1 | DESCRIPTION
0 | NORM | STALL | EAR
1 | NORM | PCHLESS MODE
2 | NORM | REVERSE | PEG LANE REVERSAL -SEE PCIE CHAPTER
3 | ENABLED | DISABLED | PHYSICAL DEBUG ENABLED
4 | DISABLE | ENABLE | DP PRESENCE
5 | DISABLE | ENABLE | PEG0CFGSEL[0]
6 | DISABLE | ENABLE | PEG0CFGSEL[1]
7 | RESET# | BIOS REQ | PEG_DEFER_TRAINING
8 | DISABLE | ENABLE | CFG UNLOCK
9 | PRESENT | NOT PRESENT | SVID NOT PRESENT
10 | ACTIVATE | NOT ACTIVATED | SAFE_MODE_BOOT
11 | HALF-SWING DC COUPLED | FULL-SWING AC COUPLED | DMI_AC_COUPLED
12 | SUBSTIEPOINT (SPT) | NOT SPT | PCH TYPE
13 | SVID | FIXED | VCCSA SVID NOT PRESENT
14 | RESERVED
15 | RESERVED
ALL HAVE INTERNAL PULL-UPS
PLACE HR24 CLOSER TO CPU
follow CRB pull high to VCCSTG
VCCST_VCCSFR
HR24
100Ohm
/XDP
H_TDO
H_TCK TERMINATION (HR127)
HR23 PLACE NEAR CPU WITHIN 1.1 INCH
H_TCK
HR23
51Ohm
/XDP
GND
Title : LGA1151 (Control)
ASUSTek Computer Inc.
Engineer: Morse_Peng
Size A3
Project Name SkyLake VC
Rev R1.00
Date: Friday, May 29, 2020
Sheet 35 of 136



Title :	LGA1150 (POWER)
ASUSTek Computer Inc.	Engineer: IAN
Size: A2	Project Name: Z87-PRO
Rev: R1.02A	
Date: Friday, May 29, 2020	Sheet 36 of 136





ILM Components are unchanged from CFL-S

ASUSTek Computer Inc.	Title : LGA1151 (GND)	
	Engineer: Morse_Peng	
Size: A2	Project Name: SkyLake VC	Rev: R1.00
Date: Friday, May 29, 2020	Sheet 37 of 136	

XDP Card USB3 CON1

CT1P1 1 H_CFG0 [35]
CT1P2 1 H_CFG1 [35]
CT1P3 1 H_CFG2 [35]
CT1P4 1 H_CFG3 [35]

CT1P8 1 H_CFG13 [35]
CT1P9 1 H_CFG12 [35]
CT1P10 1 H_CFG11 [35]
CT1P11 1 H_CFG10 [35]

CT1P13 1 H_CFG8 [35]
CT1P14 1 H_CFG7 [35]
CT1P15 1 H_TRST# [35]

XDP Card USB3 CON2

+VCCIO請從DIP電容跳線至XDP Card CON2 Pin1

CT2P1 1 H_CFG14 [35]
CT2P2 1 H_CFG15 [35]
CT2P3 1 H_CFG16 [35]
CT2P4 1 H_CFG17 [35]

GND請跳線至XDP Card CON2 Pin7

CT2P5 1 H_CFG18 [35]
CT2P6 1 H_CFG19 [35]
CT2P7 1 SKL_XDP_MBP_1 [35]
CT2P8 1 SKL_XDP_MBP_0 [35]
CT2P9 1 H_TDI [35]
CT2P10 1 H_PRDY# [35]
CT2P11 1 H_PREQ# [35]
CT2P12 1 XDP_PCUDEBUG [35]

+1.0V_A請從DIP電容跳線至XDP Card CON2 Pin19

XDP Card USB3 CON3

CT3P1 1 S_XDP_PREQ# [61]
CT3P2 1 S_XDP_PRDY# [61]

CT3P5 1 S_ITP_PMODE [58]

讓VCCST在插入XDP制具時有電

CT311請跳線至CON3 Pin11

CT3P8 1 S_JTAG_TMS [58]
CT3P9 1 S_JTAG_TDI [58]

CT3P11 1 S_JTAG_TCK [58]
CT3P12 1 S_XDP_TRST# [61]

+VCCST請從DIP電容跳線至XDP Card CON3 Pin19

XDP Card USB3 CON4

+3VSB請從DIP電容跳線至XDP Card CON4 Pin1

CT4P6 1 H_TCK [35]
CT4P7 1 H_TMS [35]
CT4P8 1 C_CPU_XDP [54]
CT4P9 1 C_CPU_XDP# [54]
CT4P10 1 H_TDO [35]
CT4P11 1 S_JTAG_TDO [58]

+3VSB_ATX請從DIP電容跳線至XDP Card CON4 Pin19

HR128
H_TCK 2 0Ohm 1 S_JTAGX [58]
/X

Naming Rule:

CTxPy==>請跳線到XDP Card CONx connector的Piny

Placement Rule:

此頁面測點全部放置背面靠近輸出端,

Layout會協助把Reference文字面開出,

若有需求初期PCB版本可洗背面文字,

但低階機種PVT PCB版本請記得通知板廠不洗背面文字

Power Rework:

+1.0V_A請從DIP電容跳線至XDP Card CON2 Pin19

+3VSB請從DIP電容跳線至XDP Card CON4 Pin1

+VCCST請從DIP電容跳線至XDP Card CON3 Pin19

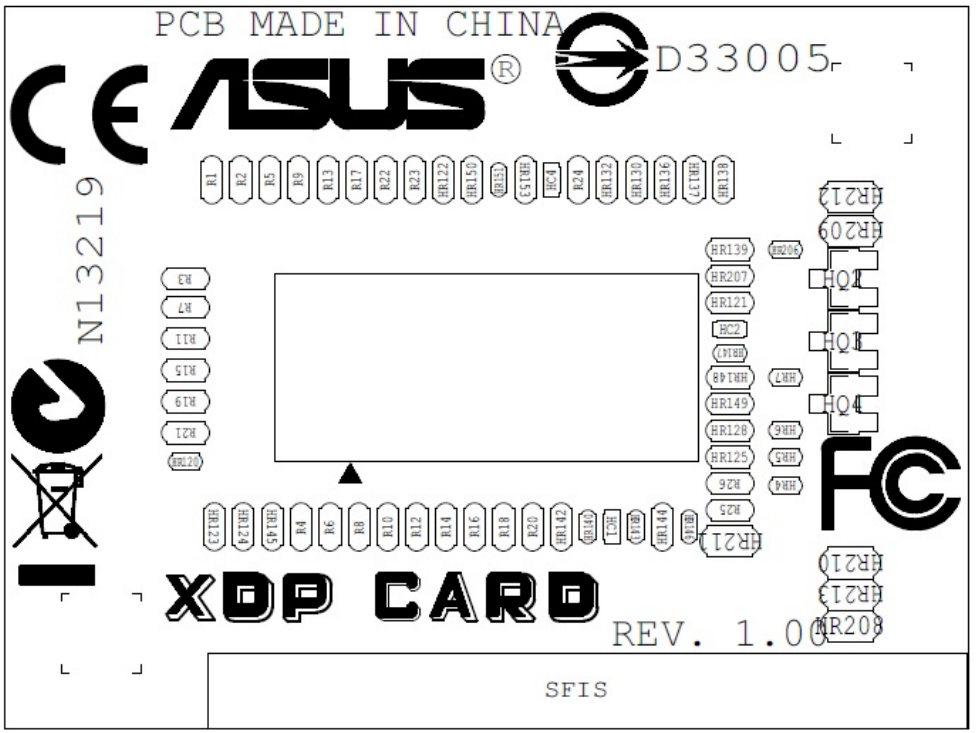
+VCCIO請從DIP電容跳線至XDP Card CON2 Pin1

+3VSB_ATX請從DIP電容跳線至XDP Card CON4 Pin19

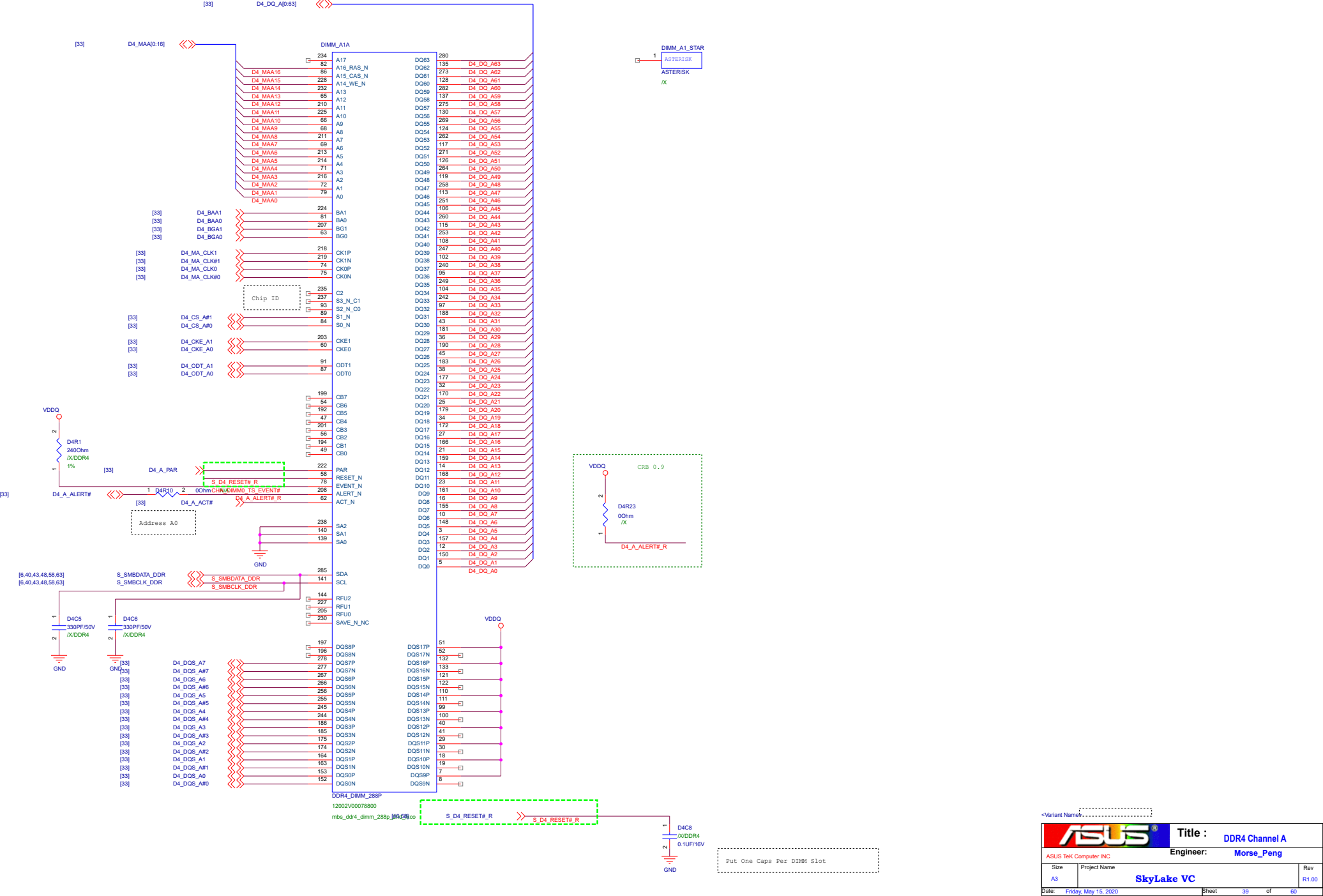
GND請跳線至XDP Card CON2 Pin7

O_RSMRST#	H_CFG4
O_IOPWRBTN#	H_CFG5
O_RSTCON#	H_CFG6
H_CPUPWRGD	H_CFG9
S_SYSPWROK	
H_CPURST#	
S_SMBCLK_MAIN	
S_SMBDATA_MAIN	

由於RD CT*test pin會被做 no test
處理，所以刪除這些需要有test pin屬性，要layout額外加



ASUSTek Computer Inc.	Title :	LGA1150 (XDP)	
	Engineer:	Grace	
Size: A3	Project Name: Z170 Series		Rev: R1.02A
Date: Friday, May 15, 2020	Sheet 38 of 136		



<Variant Name>

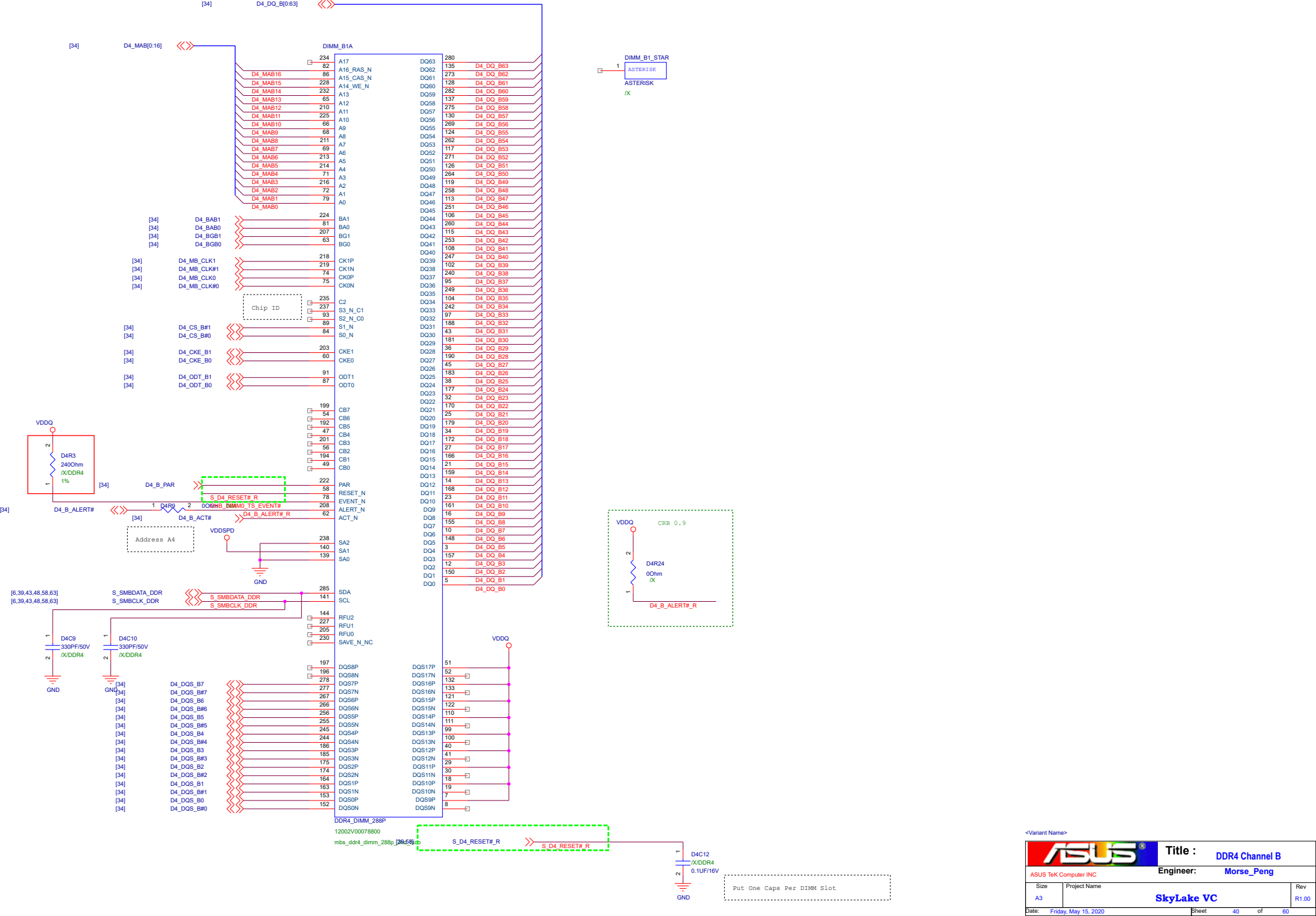
ASUS TeK Computer INC

Title : DDR4 Channel A

Engineer: Morse_Peng

Size	Project Name	Rev
A3	SkyLake VC	R1.00

Date: Friday, May 15, 2020 Sheet 39 of 60



<variant_name>

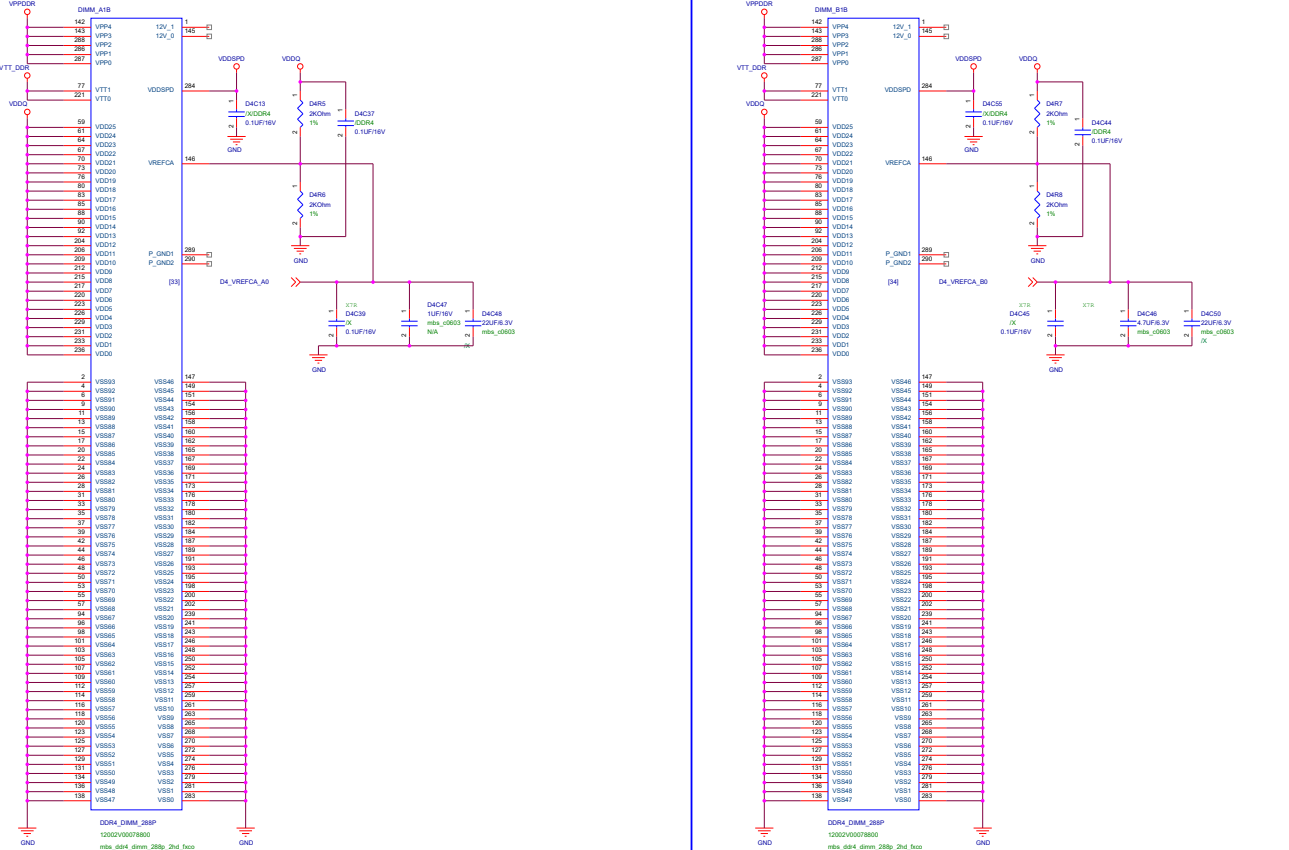
ASUS TeK Computer INC

Title : DDR4 Channel B

Engineer: Morse_Peng

Size	Project Name	Rev
A3	SkyLake VC	R1.00

Date: Friday, May 15, 2020 Sheet 40 of 60



<Variant Name>

ASUS TeK Computer INC

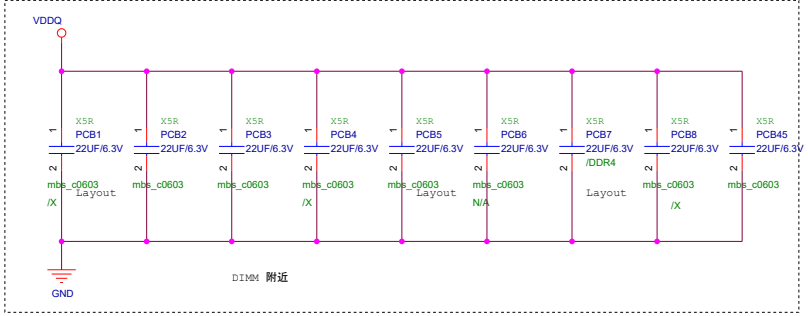
Title : -12V

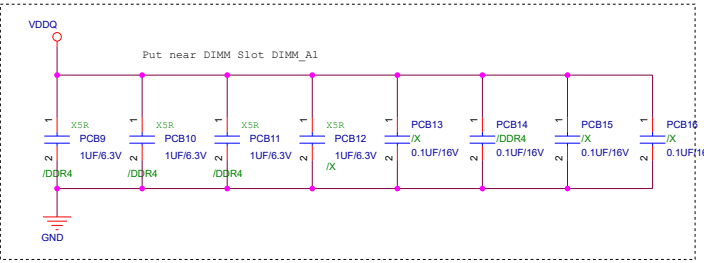
Engineer: IAN

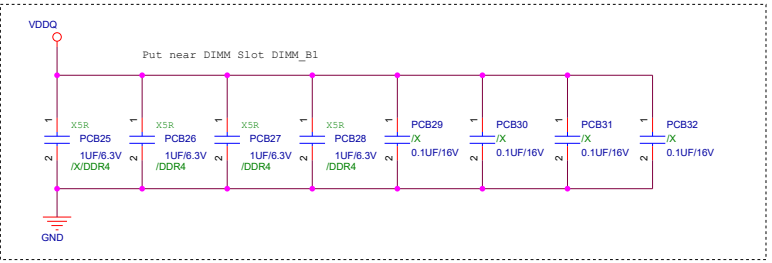
Size	Project Name	Rev
A2	Z87-PRO	R1.02A

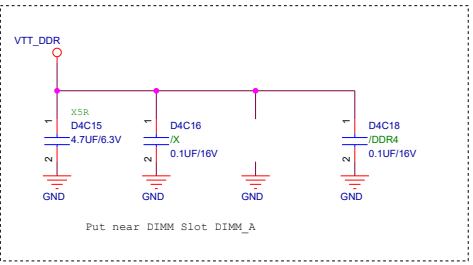
Date: Friday, May 15, 2020 Sheet 41 of 60

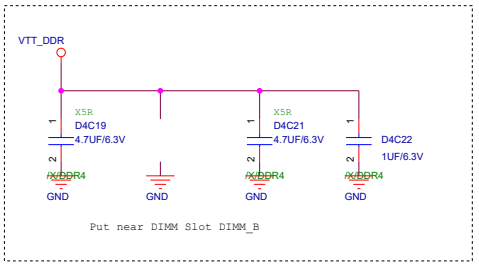
Layout to 0603

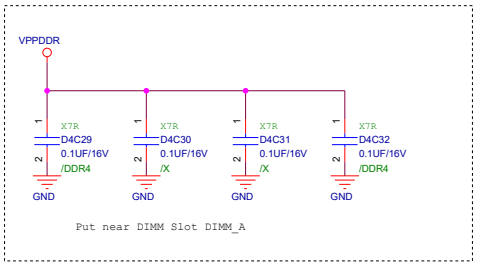


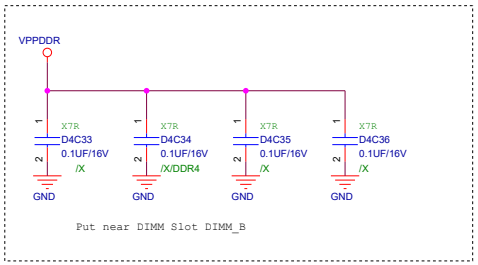












<Variant Name>

ASUSTek Computer Inc.	Title : DDR4 (Power CAPs)	
	Engineer: Miles Liu	
Size: A3	Project Name: X99_Deluxe	Rev: 1.00
Date: Friday, March 20, 2020	Sheet 42 of 60	

[6,39,40,48,58,63]
[6,39,40,48,58,63]

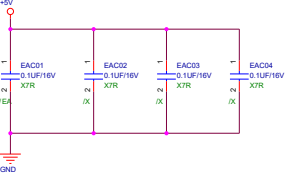
S_SMBCLK_MAIN
S_SMBDATA_MAIN

S_SMBCLK_DDR
S_SMBDATA_DDR

[6,39,40,48,58,63]
[6,39,40,48,58,63]

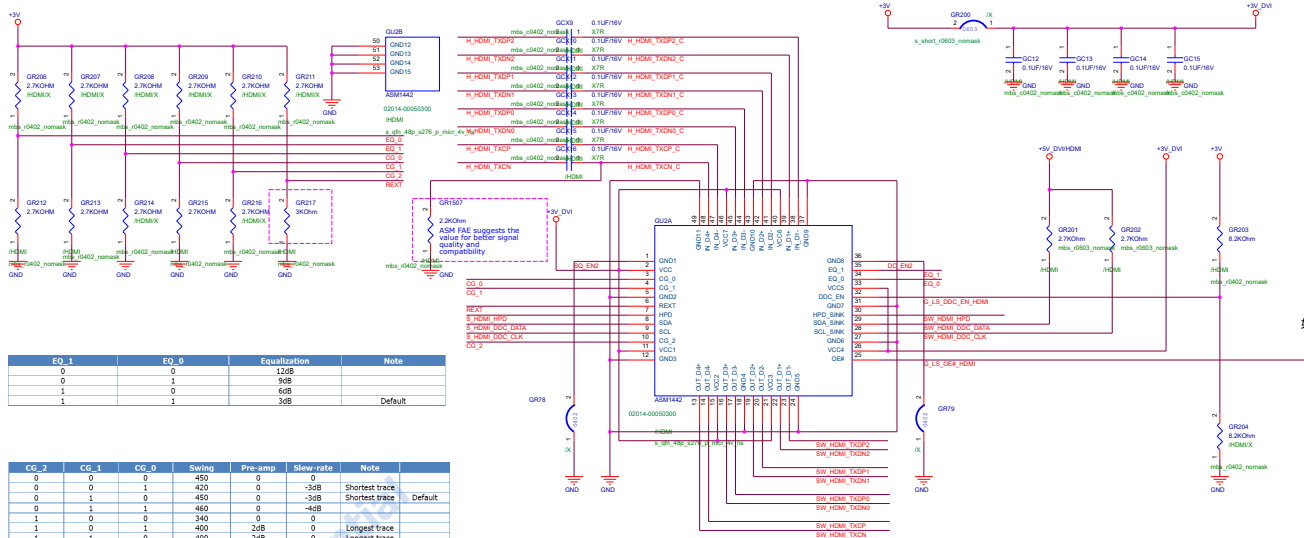
<Variant Name>

ASUSTeK Computer Inc.	Title : DDR4 (SMBUS/SPD)	
	Engineer: Payton_Lin	
Size: A3	Project Name: X99 VC Rev1.00	Rev: 1.00
Date: Friday, May 15, 2020	Sheet 43 of 60	


+5V
EAC01
0.1UF/16V
X7R
EAC02
0.1UF/16V
X7R
EAC03
0.1UF/16V
X7R
EAC04
0.1UF/16V
X7R
GND

delete it
for EMS

delete this page for HDMI/DVI colay

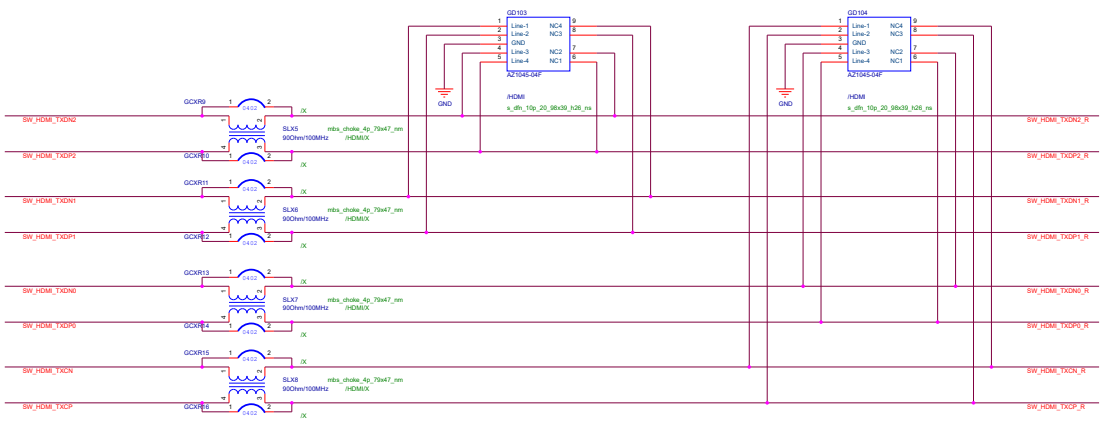


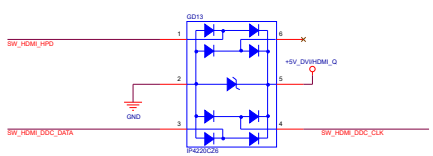
EQ_1	EQ_0	Equalization	Note
0	0	12dB	
0	1	9dB	
1	0	6dB	
1	1	3dB	Default

CG_2	CG_1	CG_0	Swing	Pre-amp	Slew-rate	Note	
0	0	0	450	0	0		
0	0	1	420	0	-3dB	Shortest trace	
0	1	0	450	0	-3dB	Shortest trace	Default
0	1	1	460	0	-4dB		
1	0	0	340	0	0		
1	0	1	400	2dB	0	Longest trace	
1	1	0	400	2dB	0	Longest trace	
1	1	1	420	0	0		

如果節能不用，則刪除此線路

Level Shifter

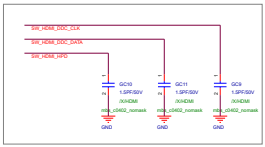


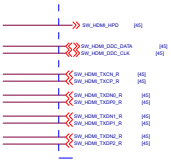


ESD

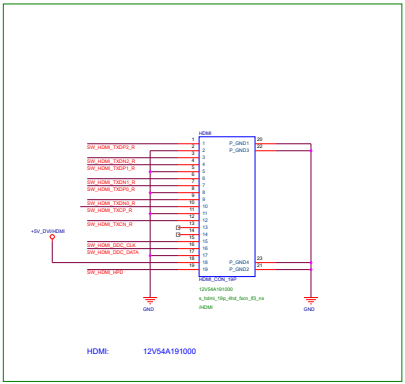
<Variant Name>

ASUSTek Computer Inc.	Title : HDMI	
	Engineer: alex_zhou	
Size: A2	Project Name: Standard Circuit	Rev: 0.01A
Date: Friday, May 29, 2020	Sheet 45 of 117	





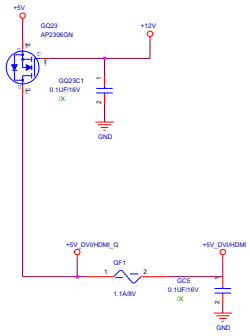
Choose connector by project

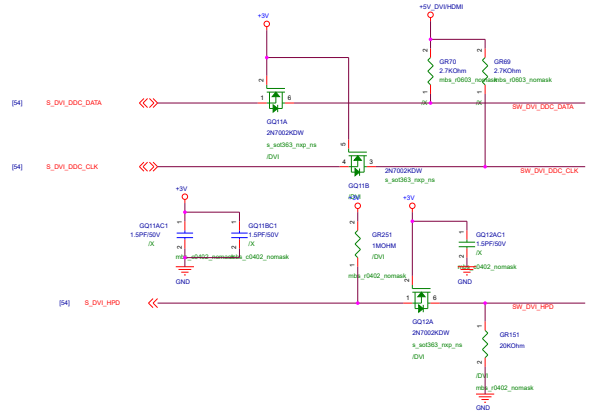


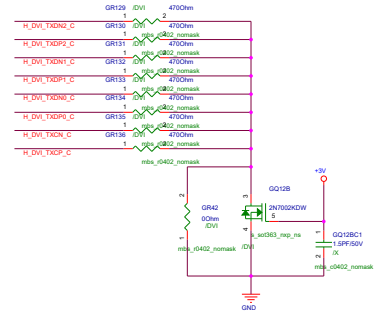
delete it
for EMS

POWER for HDMI & DVI

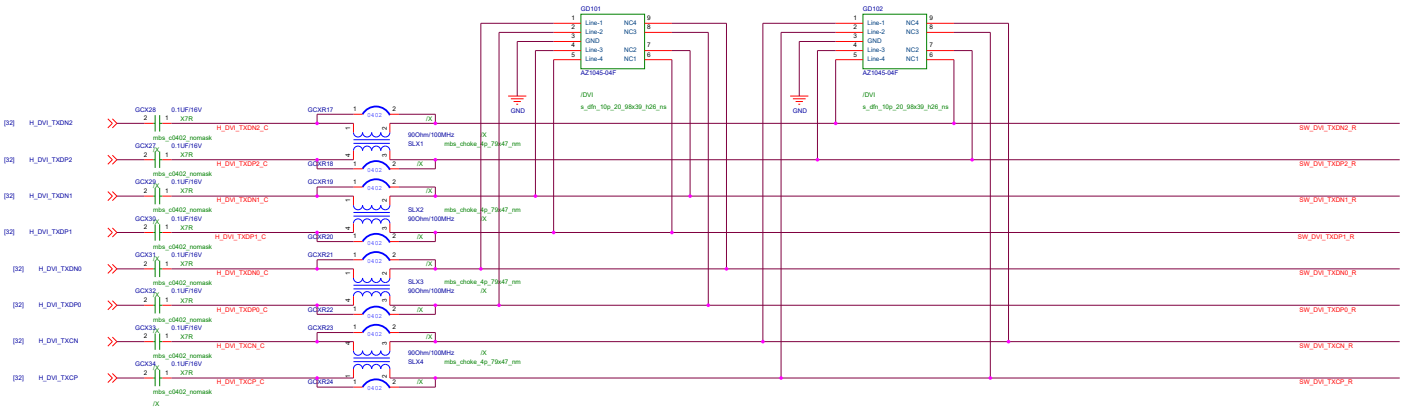
If only HDMI,this power must still need

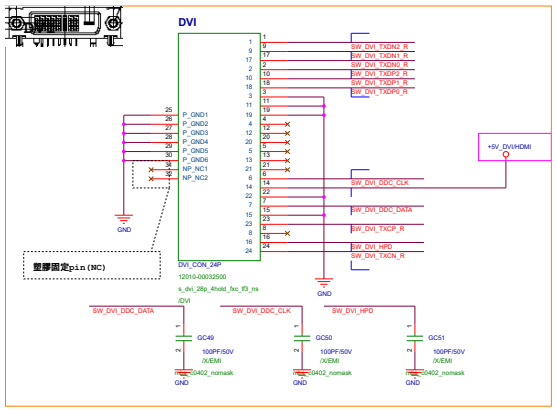




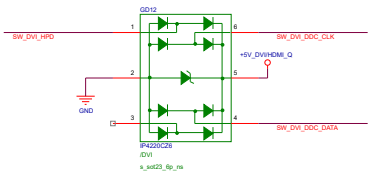


Passive/Active Devices					
Max Capacitance (Backdrive I Protection)	Schottky Diode	NA	pF	10	10
Resistor Value (+/- 5%)	R1/R2	NA	Ω	680	NA
ESD Protection	ESD	NA	NA	Optional	Optional
Max nFET Ron/Cout	NA	NA	Ω/pF	3ohm/10pF	NA





close to connector



<variant_name>

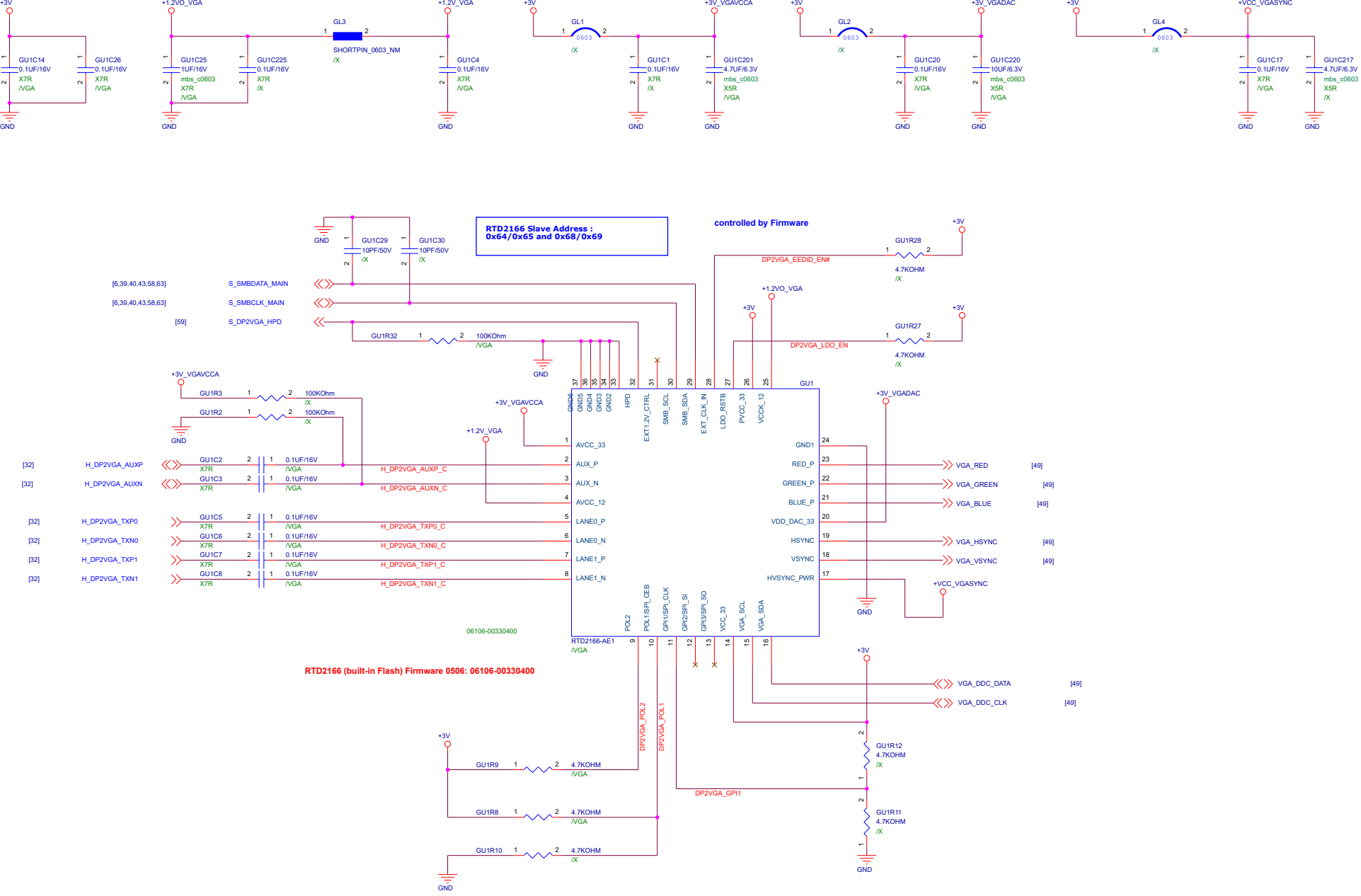
ASUSTek COMPUTER INC.

Title : DVI REDUCED LEV-SHIFT

Engineer: Morse_Peng

Size	Project Name	Rev
A2	SkyLake VC	R1.00

Date: Friday, May 29, 2020 Sheet 47 of 136



STANDARD CIRCUIT	
XUMB	OTHER
SZ_DP2VGA_1.2A	

LOGO_HD_DEMO_OTHER
/X

BOM	need DP2VGA	no DP2VGA
/VGA	mount	unmount
/X	unmount	unmount

<Variant Name>

ASUSTEK COMPUTER INC

Title : RTD2166

Engineer: SZ Design IP

Size	Project Name	Rev
A3	DP2VGA Demo Circuit	0.0

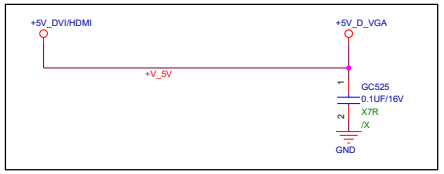
Date: Friday, May 15, 2020 Sheet 48 of 100

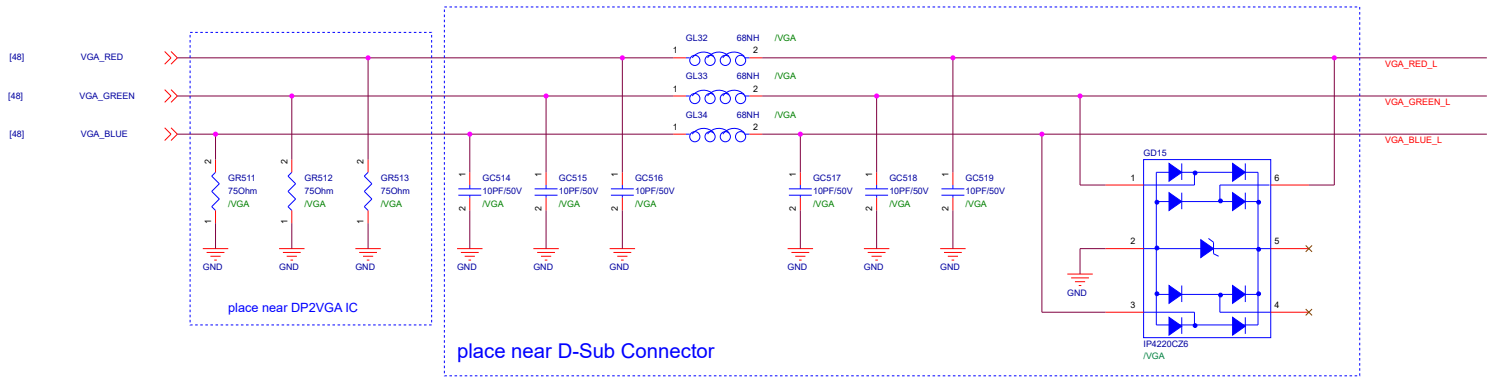
D-Sub Connector Circuit for Realtek DP2VGA IC

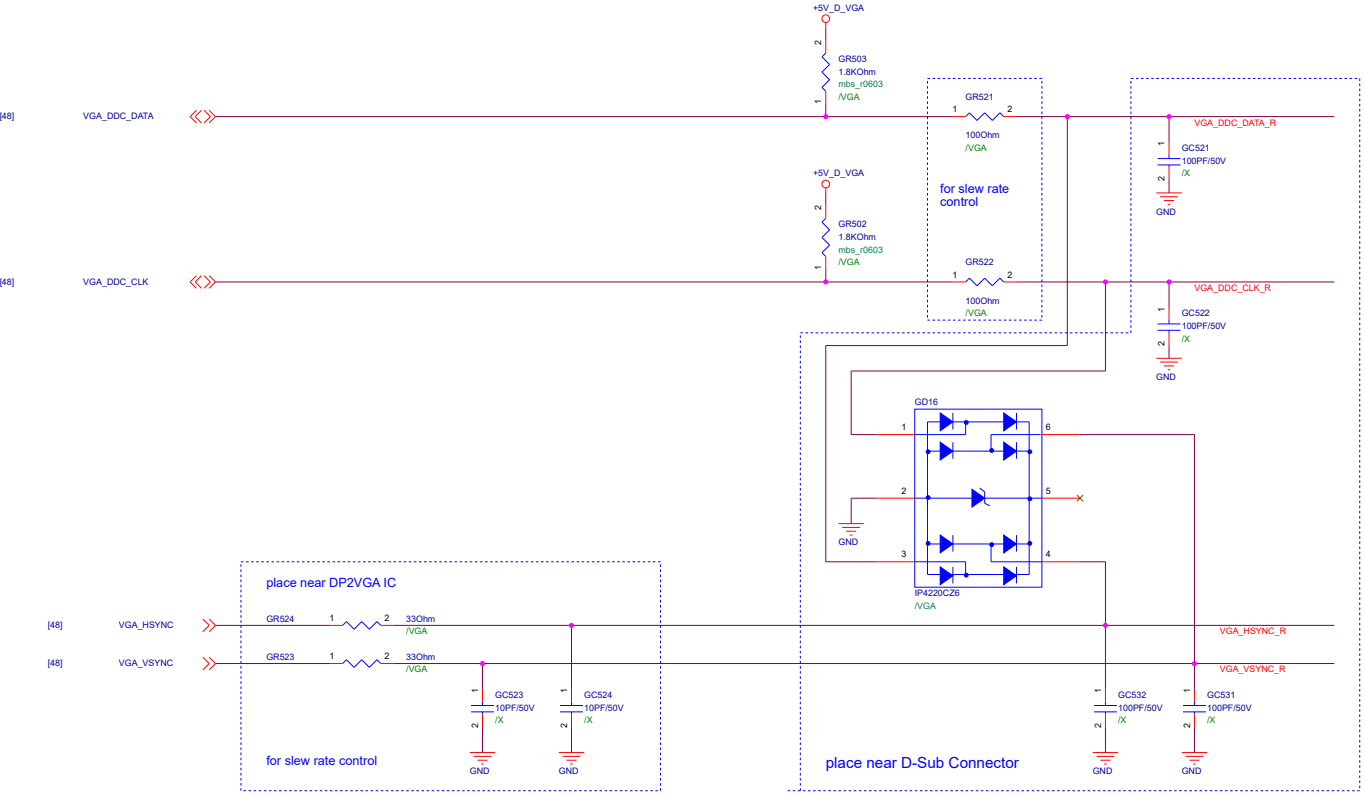
A. Choose D-Sub Connector Type by Project

B. Modify Part Number of D-Sub Connector by Color

delete it for EMS

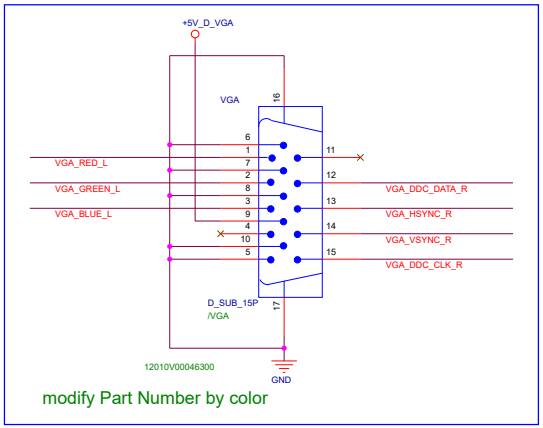






A.2

High Rise D-Sub Connector



<Variant Name>

ASUSTEK COMPUTER INC	Title : RTD2166 D-Sub	
	Engineer: SZ Design IP	
Size: A3	Project Name: DP2VGA Demo Circuit	Rev: 0.0
Date: Friday, May 15, 2020	Sheet 49 of 100	

<Variant Name>

ASUSTek COMPUTER INC.	Title : QUICK SWITCH(PCIEX16_1)	
	Engineer: Aaron_Su	
Size: A3	Project Name: CoffeeLake VC	Rev: R1.01
Date: Friday, March 20, 2020	Sheet 50 of 136	

Title : PCIEX8_3(CHARCOAL_銀黑)

ASUSTeK COMPUTER INC.

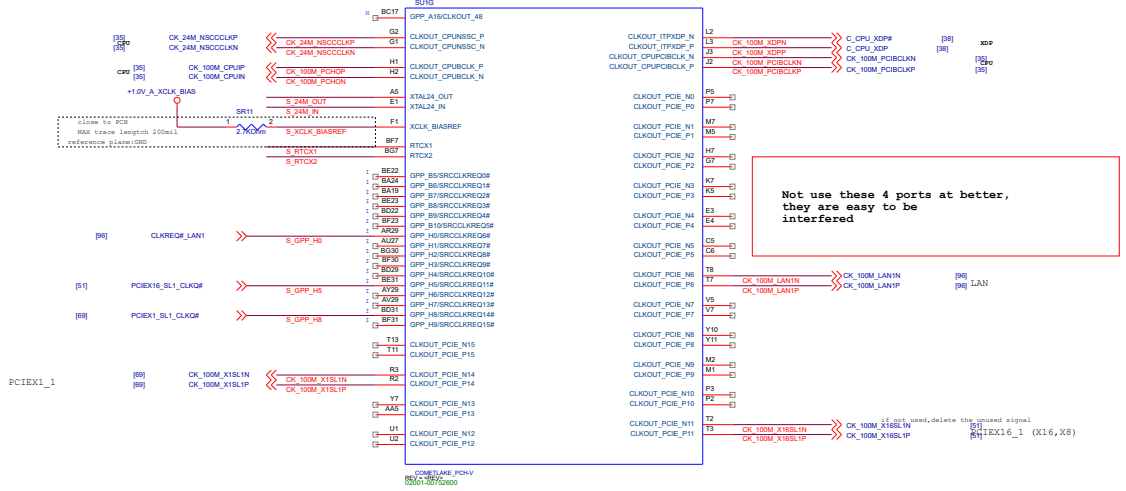
Engineer: KENNY_CHEN

Size	Project Name	Rev
A2	Z87-PRO	1.03A

Date: Friday, March 20, 2020 Sheet 52 of 136

<Variant Name>

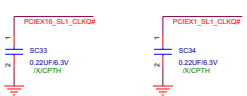
ASUSTek Computer Inc.	Title : HDMI	
	Engineer: alex_zhou	
Size: A2	Project Name: Standard Circuit	Rev: 0.01A
Date: Monday, March 23, 2020	Sheet 53 of 113	

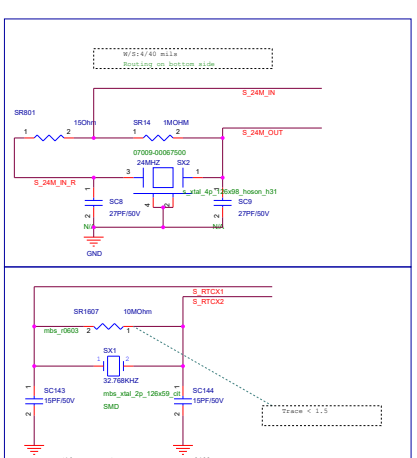


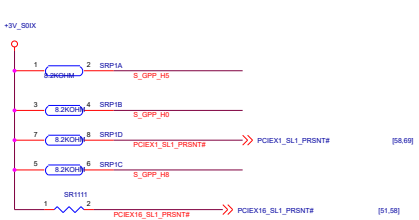
H410: 02001-00751700

For SB ESD Protection

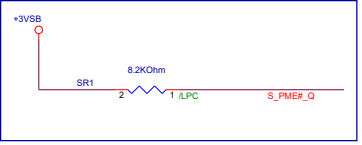
8:各個案子不同，如果那麼多的CLK REQ
function，則可以換成那個4pin的排阻：10V25382024

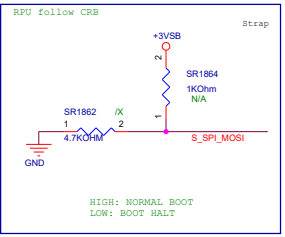


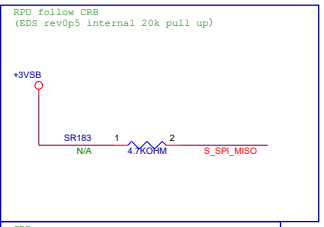


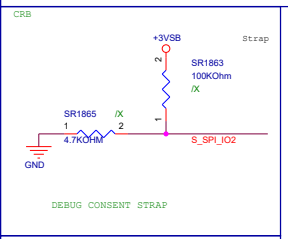


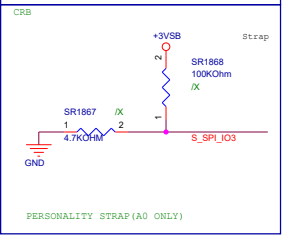
ASUSTek Computer Inc.	Title :	PCH (CLOCK)	
	Engineer:	Bing-jie_Wang	
Size: A2	Project Name	Skylake Chipset DEMO	Rev: R1.00
Date: Friday, May 15, 2020	Sheet	54 of 60	

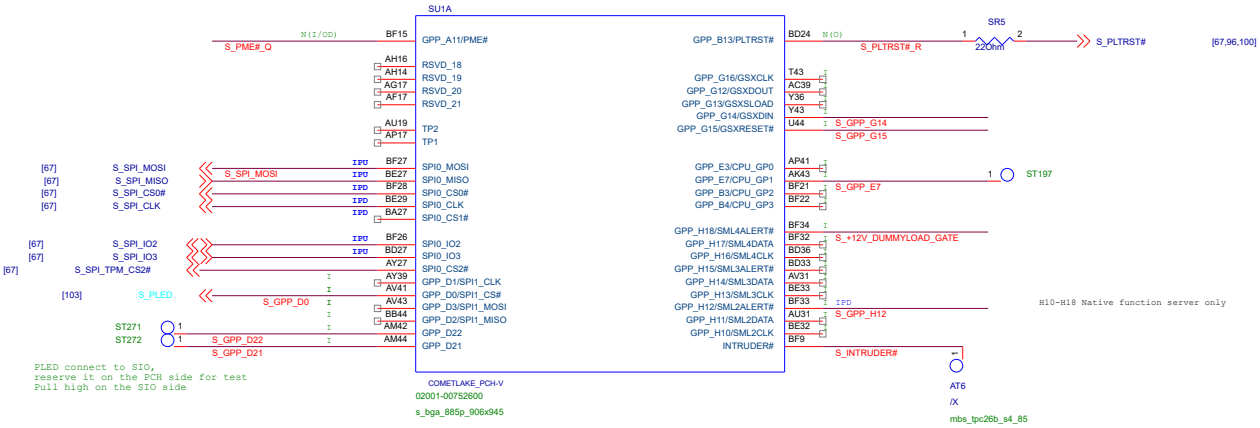




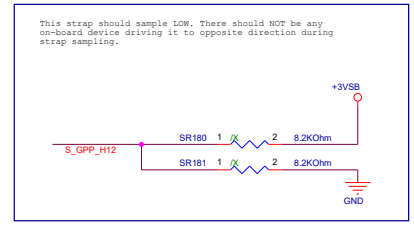


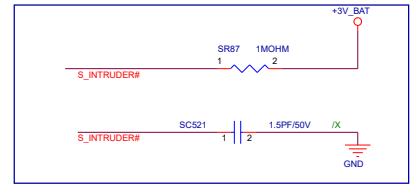


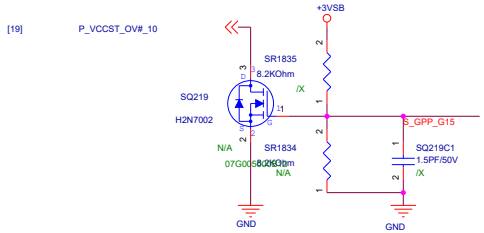


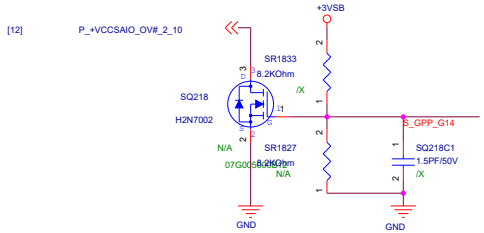


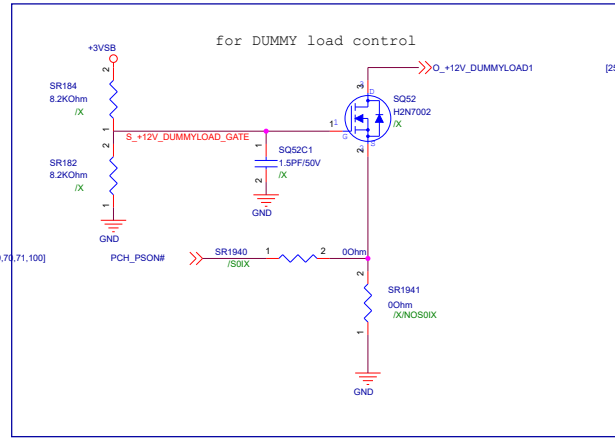
H410: 02001-00751700



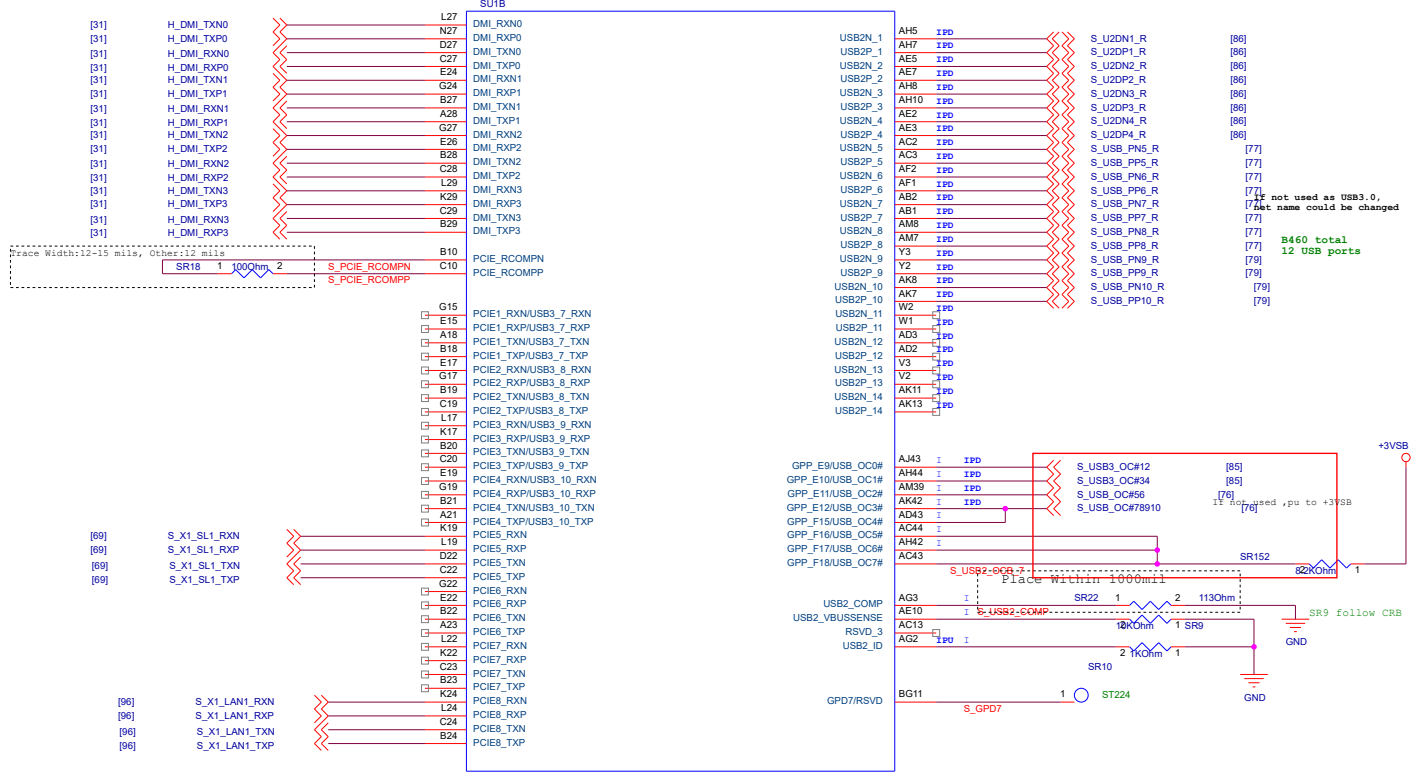








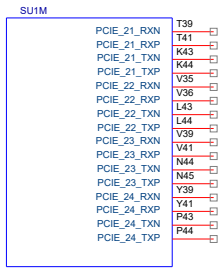
ASUSTek Computer Inc.	Title :	SPTH (PCI/SPI)	
	Engineer:	Morse_Peng	
Size: A3	Project Name: SkyLake VC		Rev: R1.02A
Date: Friday, May 15, 2020	Sheet 55 of 60		



H410: 02001-00751700

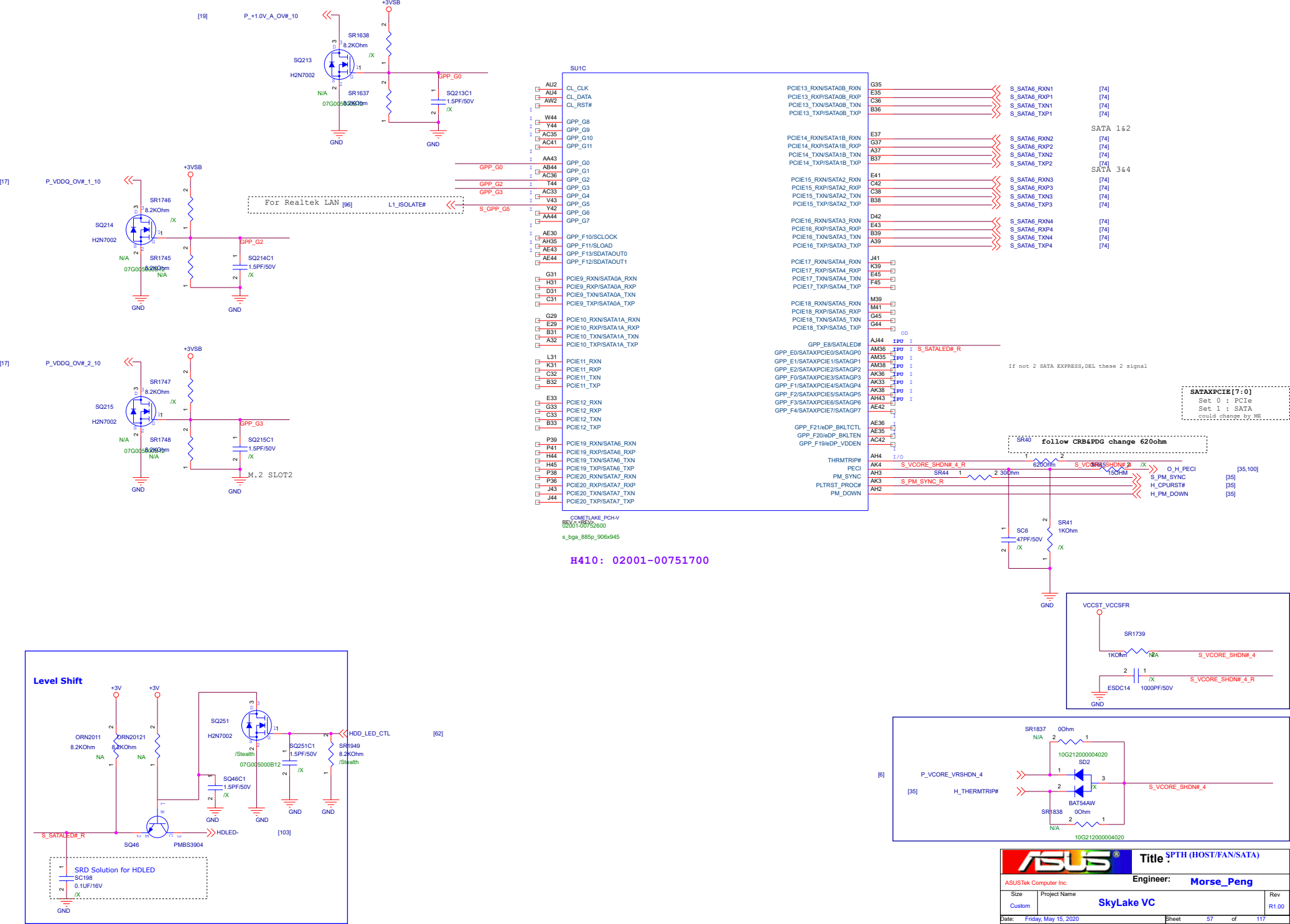
@: Intel 200 系列 chipset LAN port优先
用PCIE Port 4/8/12/16/20,如spec
限制無法用Port
4/8/12/16/20, 可選用其它Port, 但是禁止接PCIE
Lane 1/5/9/13/17;

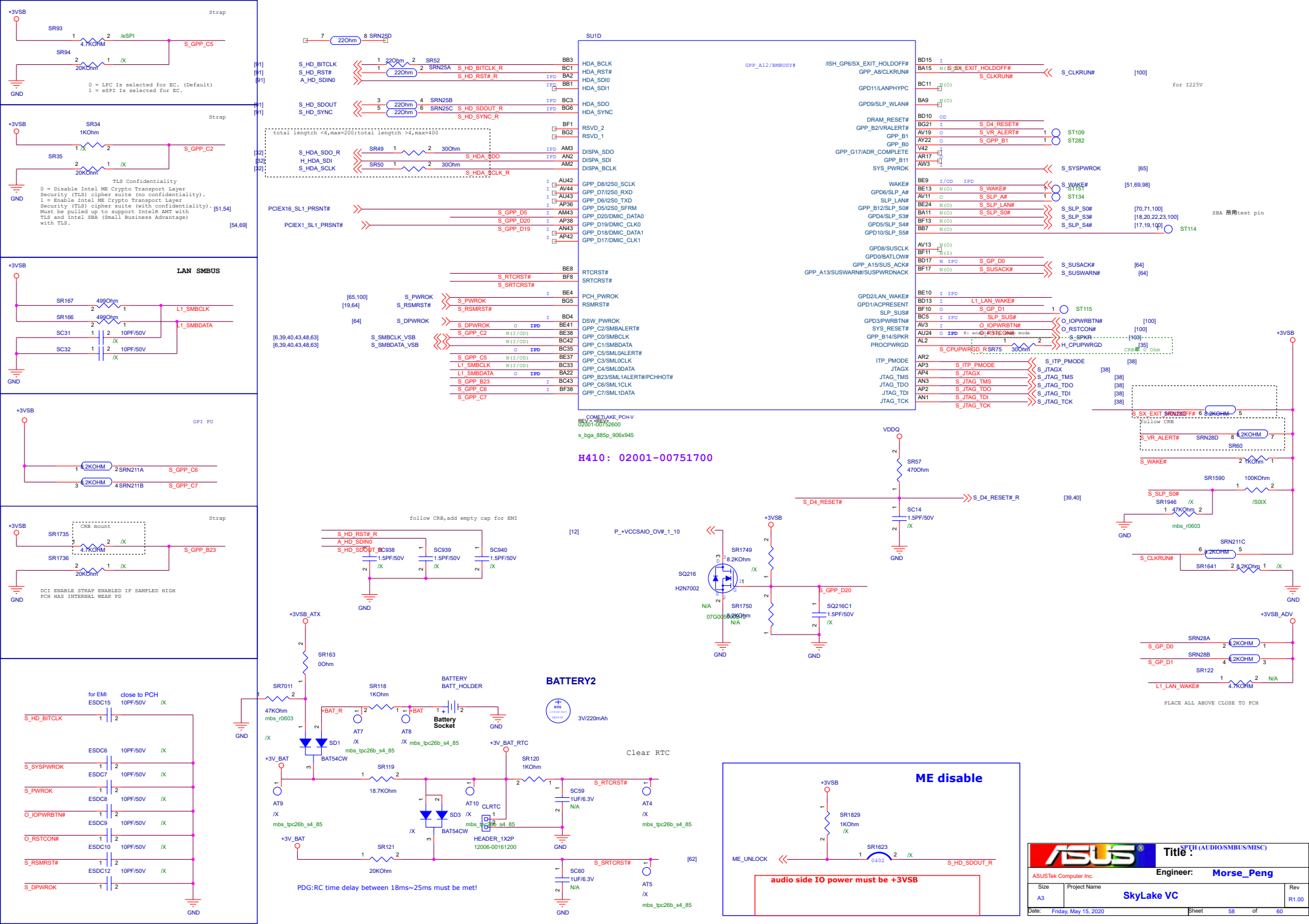
@: PCIE port
的選擇, 需要根據chipset 和PES
自己選擇搭配



H410: 02001-00751700

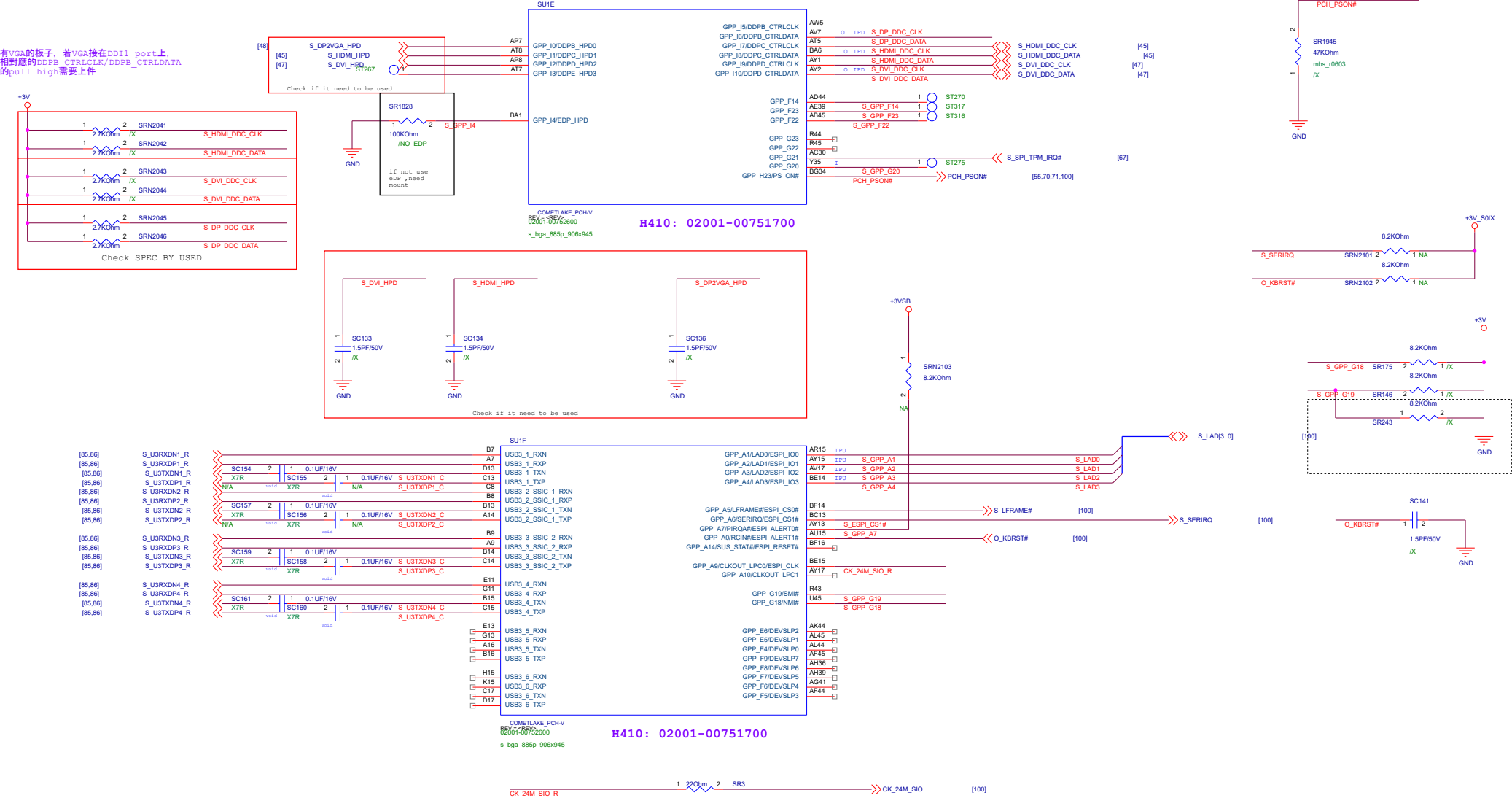
ASUSTek Computer Inc.	Title :	SPTH (PCIE/DMI/USB)	
	Engineer:	Morse_Peng	
Size: A3	Project Name: SkyLake VC		Rev: R1.00
Date: Friday, May 15, 2020	Sheet 56 of 117		


[19] P_+1.0V_A_OV#_10
+3VSB
SR1638 8.2KOhm /X
SQ213 H2N7002
SR1637 8.2KOhm
07G005000B12
SQ213C1 1.5PF/50V /X
GPP_G0
GND
[17] P_VDDQ_OV#_1_10
SR1746 8.2KOhm /X
SQ214 H2N7002
SR1745 8.2KOhm
07G005000B12
SQ214C1 1.5PF/50V /X
GPP_G2
N/A
For Realtek LAN [96] L1_ISOLATE#
S_GPP_G5
[17] P_VDDQ_OV#_2_10
SR1747 8.2KOhm /X
SQ215 H2N7002
SR1748 8.2KOhm
07G005000B12
SQ215C1 1.5PF/50V /X
GPP_G3
M.2 SLOT2
SU1C
CL_CLK
CL_DATA
CL_RST#
GPP_G8
GPP_G9
GPP_G10
GPP_G11
GPP_G0
GPP_G1
GPP_G2
GPP_G3
GPP_G4
GPP_G5
GPP_G6
GPP_G7
GPP_F10/SCLOCK
GPP_F11/SLOAD
GPP_F13/SDATAOUT0
GPP_F12/SDATAOUT1
PCIE9_RXN/SATA0A_RXN
PCIE9_RXP/SATA0A_RXP
PCIE9_TXN/SATA0A_TXN
PCIE9_TXP/SATA0A_TXP
PCIE10_RXN/SATA1A_RXN
PCIE10_RXP/SATA1A_RXP
PCIE10_TXN/SATA1A_TXN
PCIE10_TXP/SATA1A_TXP
PCIE11_RXN
PCIE11_RXP
PCIE11_TXN
PCIE11_TXP
PCIE12_RXN
PCIE12_RXP
PCIE12_TXN
PCIE12_TXP
PCIE19_RXN/SATA6_RXN
PCIE19_RXP/SATA6_RXP
PCIE19_TXN/SATA6_TXN
PCIE19_TXP/SATA6_TXP
PCIE20_RXN/SATA7_RXN
PCIE20_RXP/SATA7_RXP
PCIE20_TXN/SATA7_TXN
PCIE20_TXP/SATA7_TXP
COMETLAKE_PCH-V
02001-00752600
s_bga_885p_906x945
PCIE13_RXN/SATA0B_RXN
PCIE13_RXP/SATA0B_RXP
PCIE13_TXN/SATA0B_TXN
PCIE13_TXP/SATA0B_TXP
PCIE14_RXN/SATA1B_RXN
PCIE14_RXP/SATA1B_RXP
PCIE14_TXN/SATA1B_TXN
PCIE14_TXP/SATA1B_TXP
PCIE15_RXN/SATA2_RXN
PCIE15_RXP/SATA2_RXP
PCIE15_TXN/SATA2_TXN
PCIE15_TXP/SATA2_TXP
PCIE16_RXN/SATA3_RXN
PCIE16_RXP/SATA3_RXP
PCIE16_TXN/SATA3_TXN
PCIE16_TXP/SATA3_TXP
PCIE17_RXN/SATA4_RXN
PCIE17_RXP/SATA4_RXP
PCIE17_TXN/SATA4_TXN
PCIE17_TXP/SATA4_TXP
PCIE18_RXN/SATA5_RXN
PCIE18_RXP/SATA5_RXP
PCIE18_TXN/SATA5_TXN
PCIE18_TXP/SATA5_TXP
GPP_E8/SATALED#
GPP_E0/SATAXPCIE0/SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E2/SATAXPCIE2/SATAGP2
GPP_F0/SATAXPCIE3/SATAGP3
GPP_F1/SATAXPCIE4/SATAGP4
GPP_F2/SATAXPCIE5/SATAGP5
GPP_F3/SATAXPCIE6/SATAGP6
GPP_F4/SATAXPCIE7/SATAGP7
GPP_F21/eDP_BKLTCTL
GPP_F20/eDP_BKLTEN
GPP_F19/eDP_VDDEN
THRMTRIP#
PECI
PM_SYNC
PLTRST_PROC#
PM_DOWN
S_SATA6_RXN1 [74]
S_SATA6_RXP1 [74]
S_SATA6_TXN1 [74]
S_SATA6_TXP1 [74]
SATA 1&2
S_SATA6_RXN2 [74]
S_SATA6_RXP2 [74]
S_SATA6_TXN2 [74]
S_SATA6_TXP2 [74]
SATA 3&4
S_SATA6_RXN3 [74]
S_SATA6_RXP3 [74]
S_SATA6_TXN3 [74]
S_SATA6_TXP3 [74]
S_SATA6_RXN4 [74]
S_SATA6_RXP4 [74]
S_SATA6_TXN4 [74]
S_SATA6_TXP4 [74]
S_SATALED#_R
If not 2 SATA EXPRESS,DEL these 2 signal
SATAXPCIE[7:0]
Set 0 : PCIe
Set 1 : SATA
could change by ME
SR40 follow CRB&PDG change 620ohm
S_VCORE_SHDN#_4_R
620ohm
S_VCORE_SHDN#_4
150HM
O_H_PECI [35,100]
S_PM_SYNC [35]
H_CPURST# [35]
H_PM_DOWN [35]
SR44 300hm
S_PM_SYNC_R
SC6 47PF/50V /X
SR41 1KOhm /X
GND
H410: 02001-00751700
Level Shift
+3V
ORN2011 8.2KOhm NA
ORN20121 8.2KOhm NA
SQ251 H2N7002
/Stealth
07G005000B12
SQ251C1 1.5PF/50V /X
SR1949 8.2KOhm /Stealth
HDD_LED_CTL [62]
SQ46C1 1.5PF/50V /X
S_SATALED#_R
SQ46 PMBS3904
HDLED- [103]
SRD Solution for HDLED
SC198 0.1UF/16V /X
VCCST_VCCSFR
SR1739 1KOhm N/A
S_VCORE_SHDN#_4
ESDC14 1000PF/50V
S_VCORE_SHDN#_4_R
[6] P_VCORE_VRSHDN_4
[35] H_THERMTRIP#
SR1837 0Ohm N/A
10G212000004020
SD2
BAT54AW
SR1838 0Ohm N/A
S_VCORE_SHDN#_4
ASUS
Title : SPTH (HOST/FAN/SATA)
ASUSTek Computer Inc.
Engineer: Morse_Peng
Size Custom
Project Name SkyLake VC
Rev R1.00
Date: Friday, May 15, 2020
Sheet 57 of 117

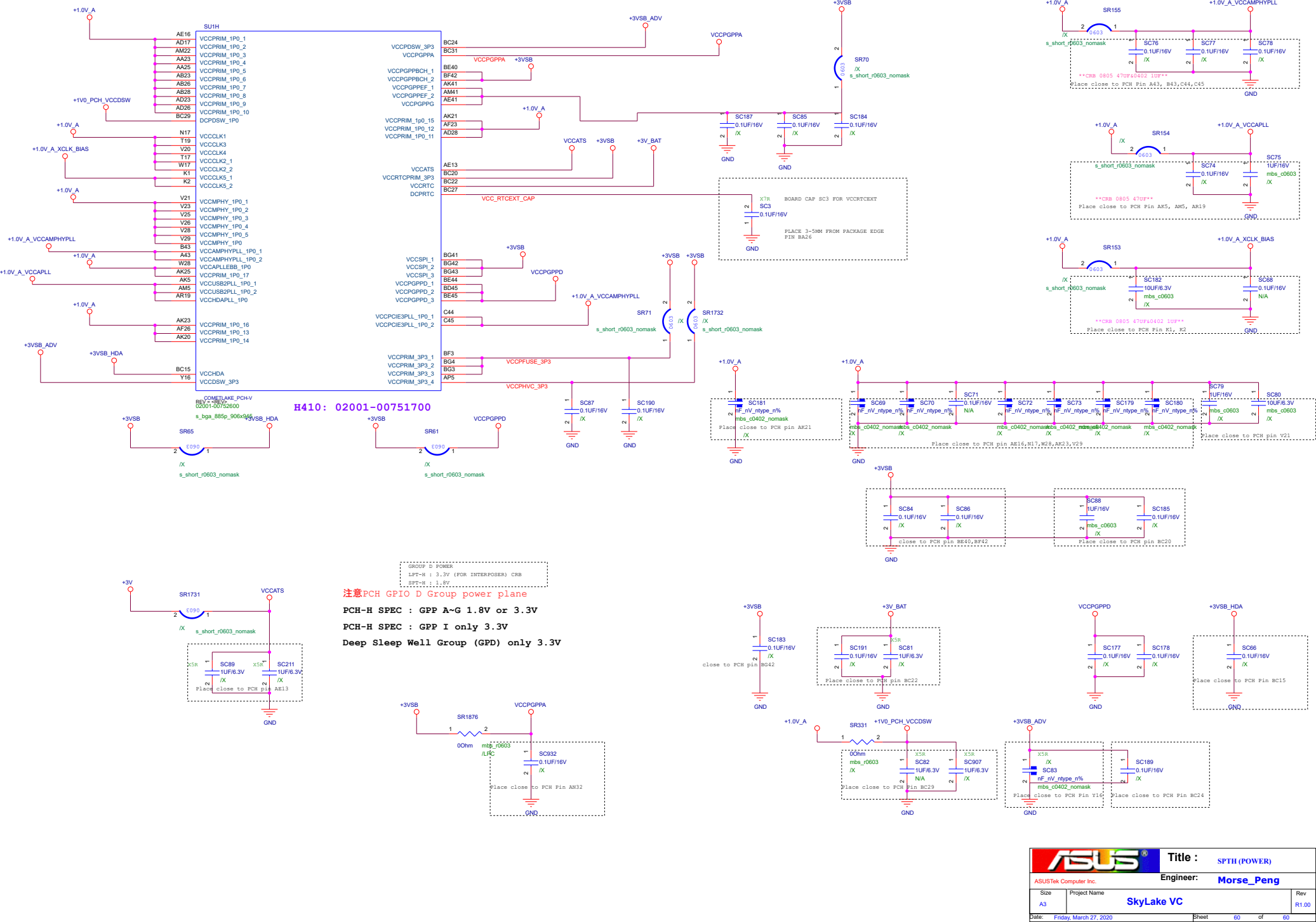


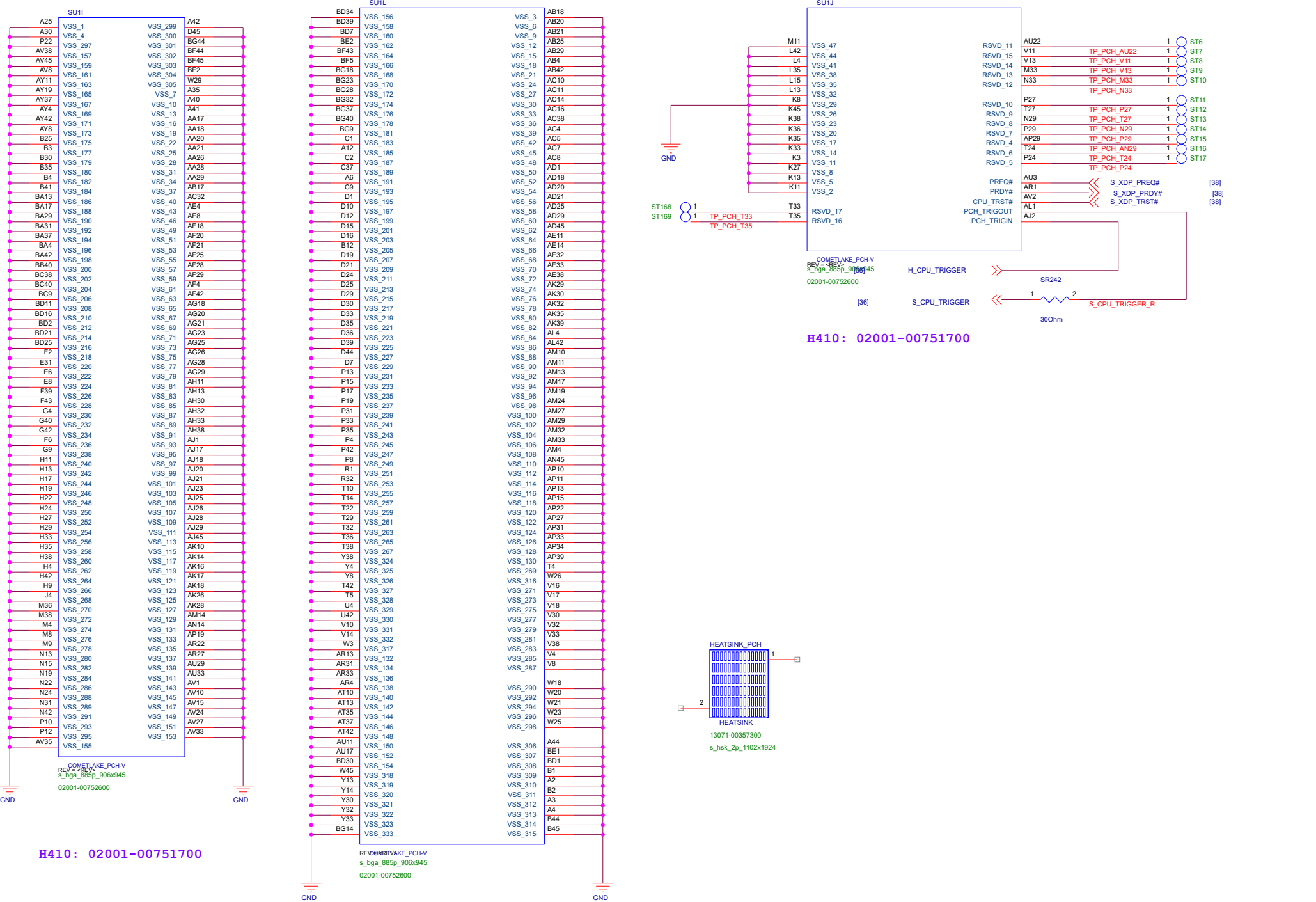
Title :	SPTH (AUDIO/SMBUS/MISC)
ASUSTek Computer Inc.	Engineer: Morse_Peng
Size: A3	Project Name: SkyLake VC
Rev: R1.00	
Date: Friday, May 15, 2020	Sheet 58 of 60

有VGA的板子，若VGA接在DDI1 port上，
相對應的DDPB_CTRLCLK/DDPB_CTRLDATA
的pull high需要上件

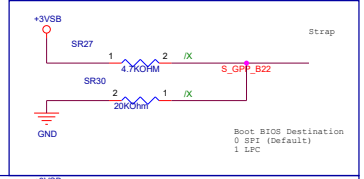


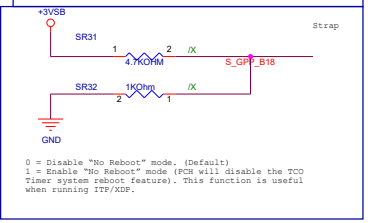
ASUSTek Computer Inc.	Title : SPTH (DISPLAY/USB3)		
	Engineer: Morse_Peng		
Size: A3	Project Name: SkyLake VC		Rev: R1.00
Date: Friday, May 29, 2020	Sheet 59 of 60		


SU1H
COMETLAKE_PCH-V
REV = REV2
02001-00752600
s_bga_885p_906x945
H410: 02001-00751700
GROUP D POWER
LPT-H : 3.3V (FOR INTERPOSER) CRB
SPT-H : 1.8V
注意PCH GPIO D Group power plane
PCH-H SPEC : GPP A~G 1.8V or 3.3V
PCH-H SPEC : GPP I only 3.3V
Deep Sleep Well Group (GPD) only 3.3V
Title : SPTH (POWER)
ASUSTek Computer Inc.
Engineer: Morse_Peng
Size A3
Project Name SkyLake VC
Rev R1.00
Date: Friday, March 27, 2020
Sheet 60 of 60

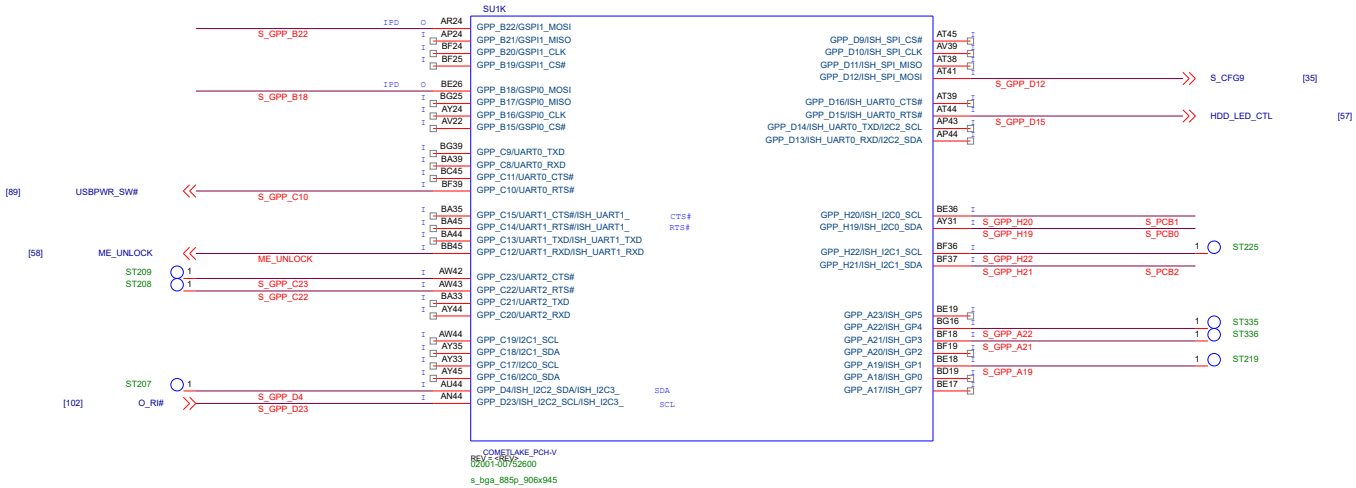


ASUSTek Computer Inc.	Title :	LYNX (GND)	
	Engineer:	IAN	
Size: A3	Project Name: Z87-PRO		Rev: R1.02A
Date: Friday, May 15, 2020	Sheet 61 of 60		

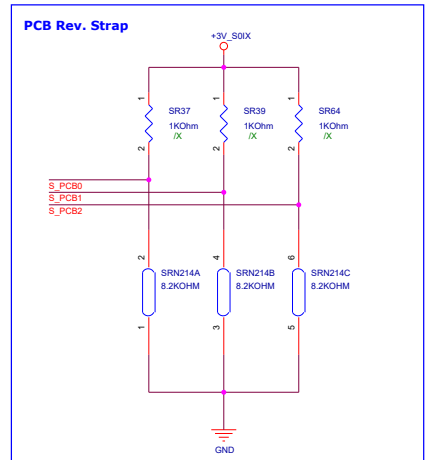




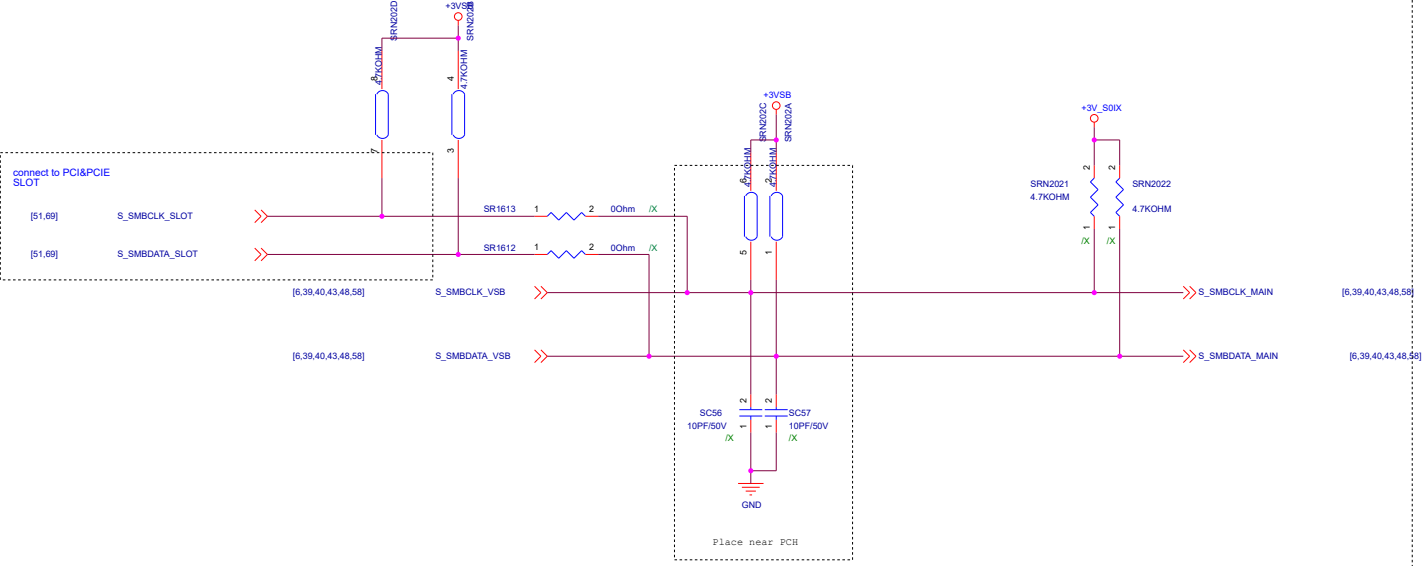
GPI PU



H410: 02001-00751700

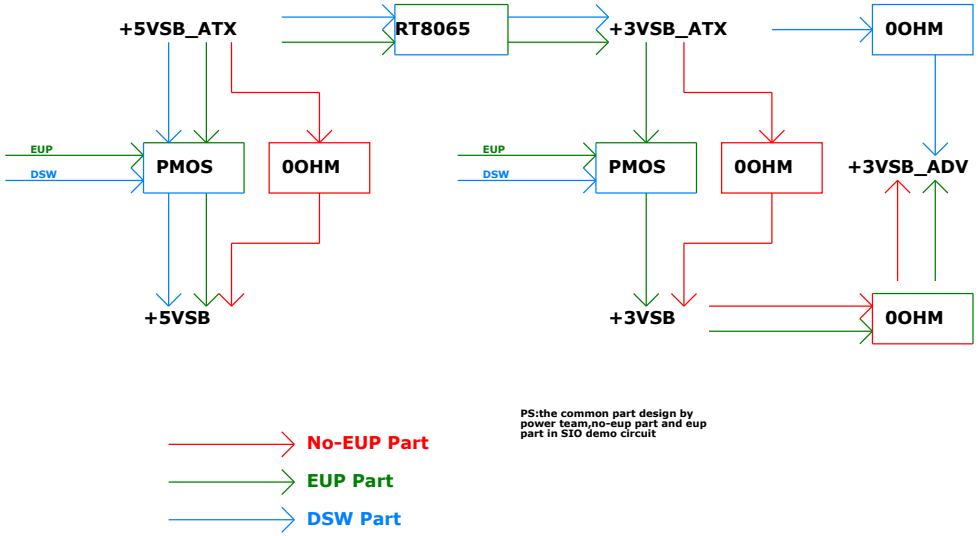


ASUSTek Computer Inc.	Title : SPTH (GPIO)	
	Engineer: Morse_Peng	
Size: A3	Project Name: SkyLake VC	Rev: R1.00
Date: Friday, May 15, 2020	Sheet 62 of 60	



ASUSTek Computer Inc.	Title : SPTH (SMBUS/CLRTC)		
	Engineer: Morse_Peng		
Size: A3	Project Name: SkyLake VC		Rev: R1.00
Date: Friday, May 15, 2020	Sheet 63 of 60		

POWER FLOW



PS:the common part design by power team,no-eup part and eup part in SIO demo circuit

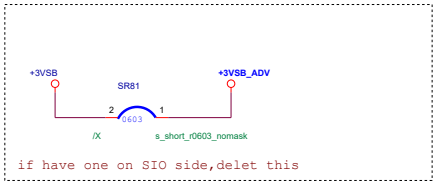
No-EUP Part

EUP Part

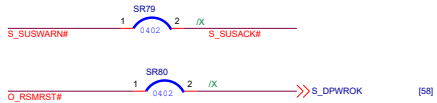
DSW Part

NOT SUPPORT DSW

Power plane



Control link

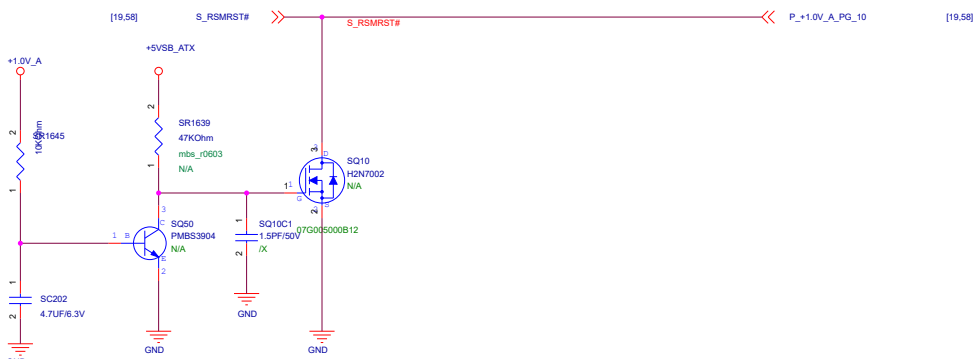


if NO DSW , please use shortpin

SUPPORT DSW

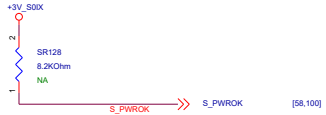
Power plane

Control link

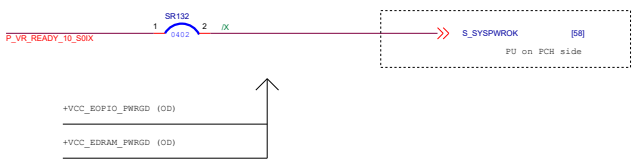


ASUSTek Computer Inc.	Title : SPTH (DSW SEQUENCE)		
	Engineer: IAN		
Size: A3	Project Name: SkyLake VC		Rev: R1.00
Date: Friday, May 15, 2020	Sheet 64 of 60		

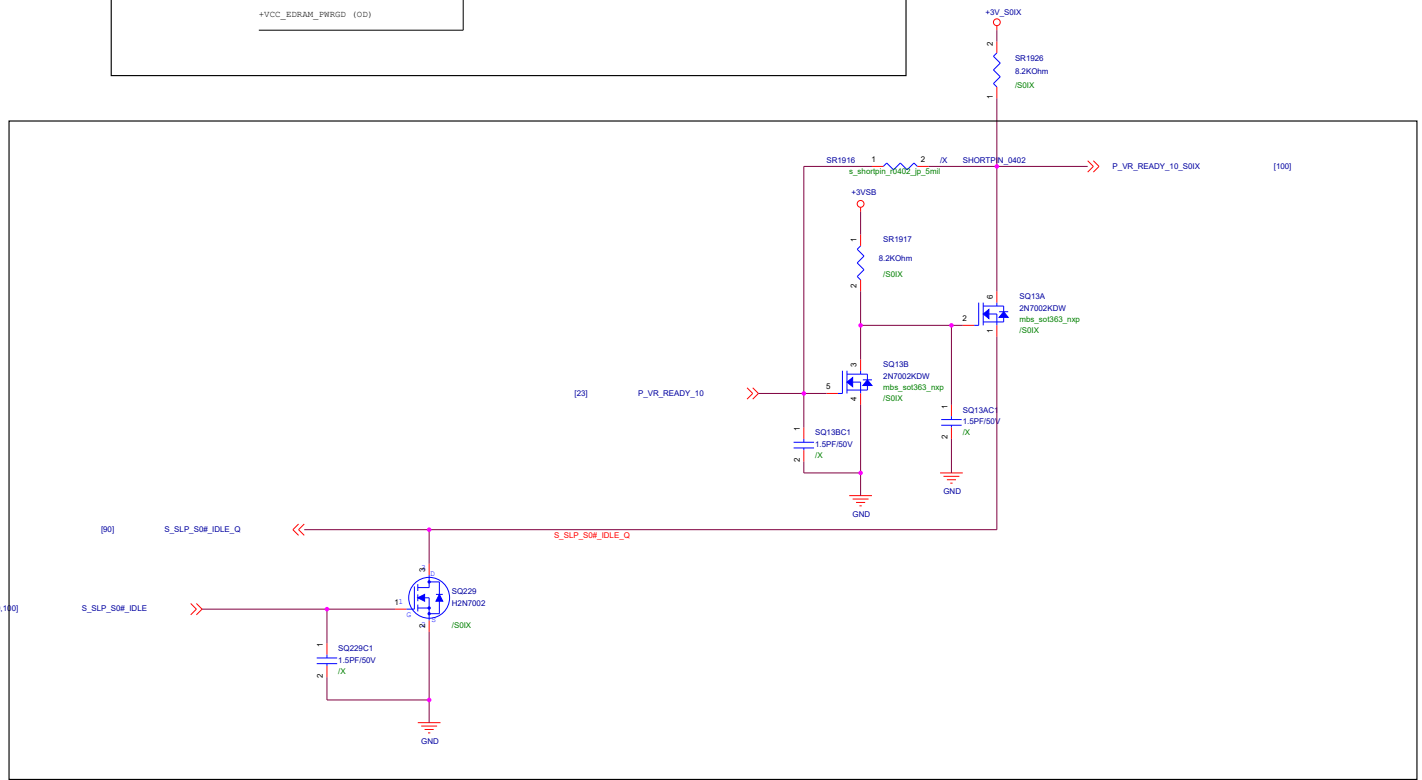
PCH_PWRGD & VCCST_PWRGD Sequence Control Ckts



PCH_SYSPWROK Sequence Control Ckts



1. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD.
2. PLTRST# = AND (PCH_PWROK, SYS_PWROK, PROCPWRGD)
Refer to PDG Figure 40-1 SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation
3. It is recommended that SYS_PWROK be asserted after both PWROK assertion and processor PCH does not monitor
4. PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. SYS_PWROK be asserted after both PWROK assertion and processor core VR PWRGD assertion.



ASUSTek Computer Inc.	Title :	SHELL(PCH/SYS/PROC_PWROK)	
	Engineer:	IAN	
Size: A2	Project Name: SkyLake VC		Rev: R1.00
Date: Friday, May 15, 2020	Sheet 65 of 60		

<Variant Name>

Title: SPTH EUP Control

ASUSTeK COMPUTER INC

Engineer: Morse_Peng

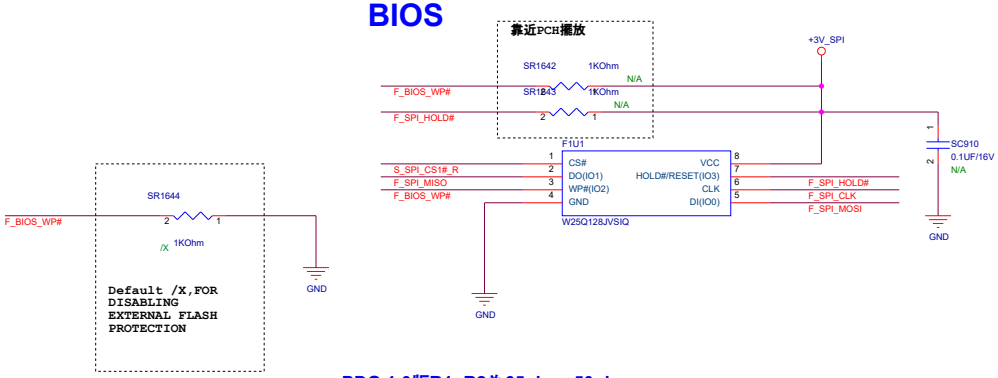
Size	Project Name	Rev
A3	SkyLake VC	R1.00

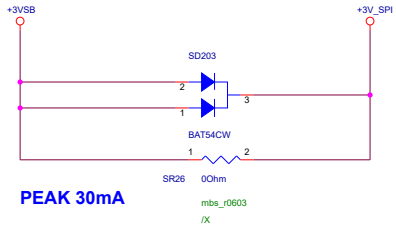
Date:	Friday, March 20, 2020	Sheet	66	of	60

Standard Circuit	
BIOS	SPI
REV.	F1_0.3G_Beta

SPI /X/SPI

BIOS

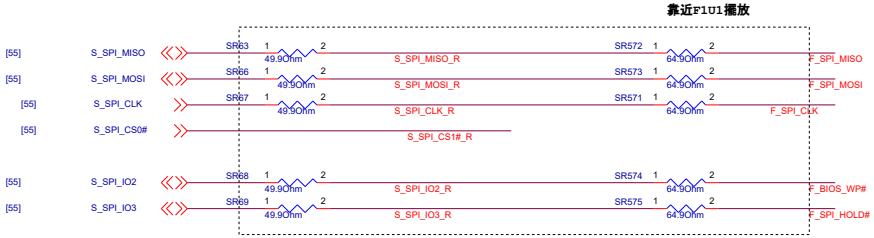




PEAK 30mA

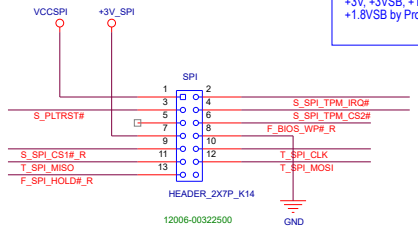
USE SMD BIOS ,PCH 3V_SPI should change to 3VSB

PDG 1.0版R1+R2為65ohm+50ohm

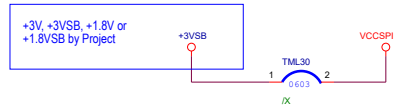


TPM: 12006-00321700
SPI: 12006-00322500
根據需求自行選擇料號並
修改成對應的part reference

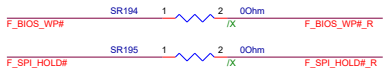
SPI DIP SOCKET

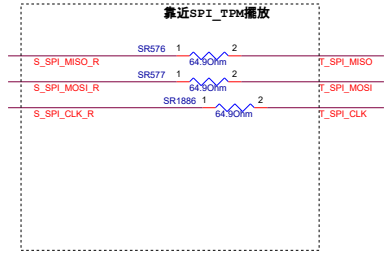


F

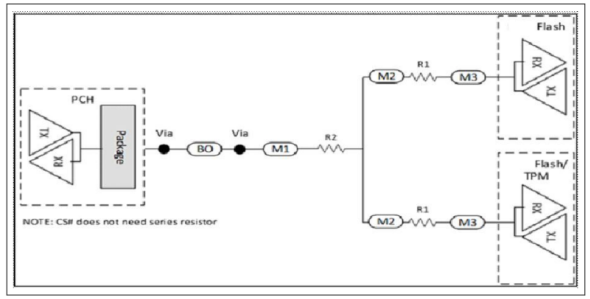


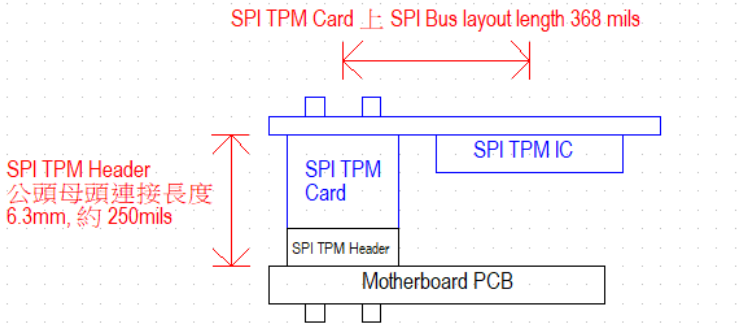
注意SR194,SR195的擺放位置,
避免F_BIOS_WP#和F_SPI_HOLD#的殘線





SPI0 2 Load Topology





<Variant Name>

ASUSTek COMPUTER INC.

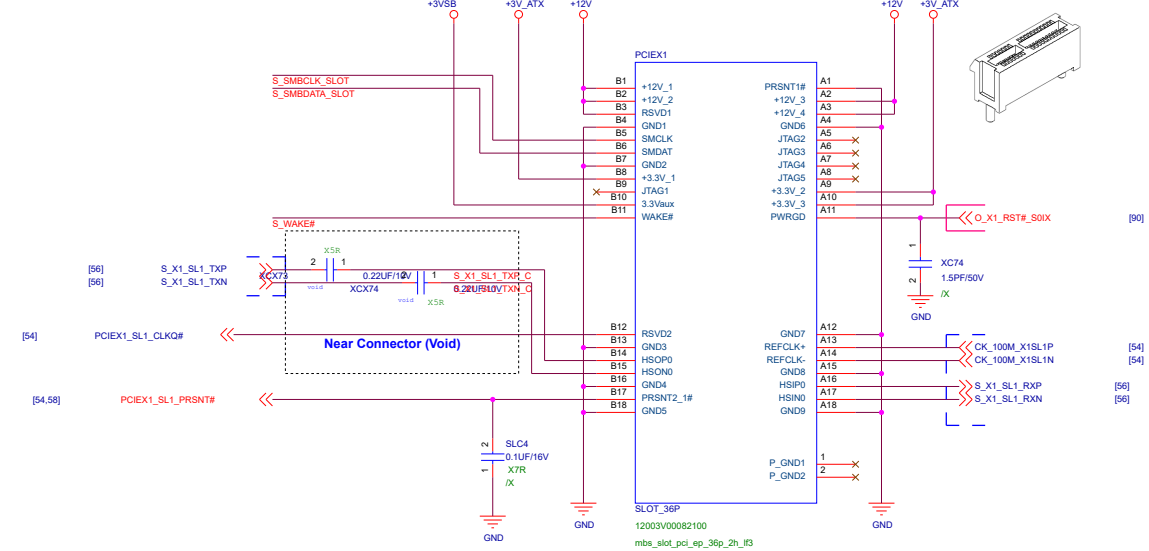
Title : SINGLE BIOS

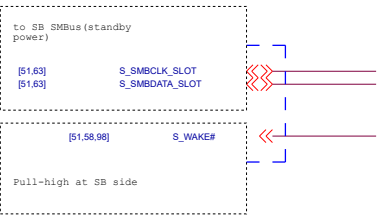
Engineer: IAN

Size	Project Name	Rev
A3	Z87-PRO	R1.02A

Date: Wednesday, May 27, 2020 Sheet 67 of 115

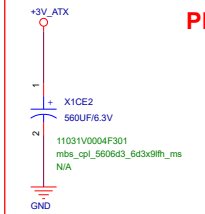
Sel Pin	Function	
L	N_in to N_outa	PCIEX8_3
H	N_in to N_outb	PCIEX8_2





delete for 108x used

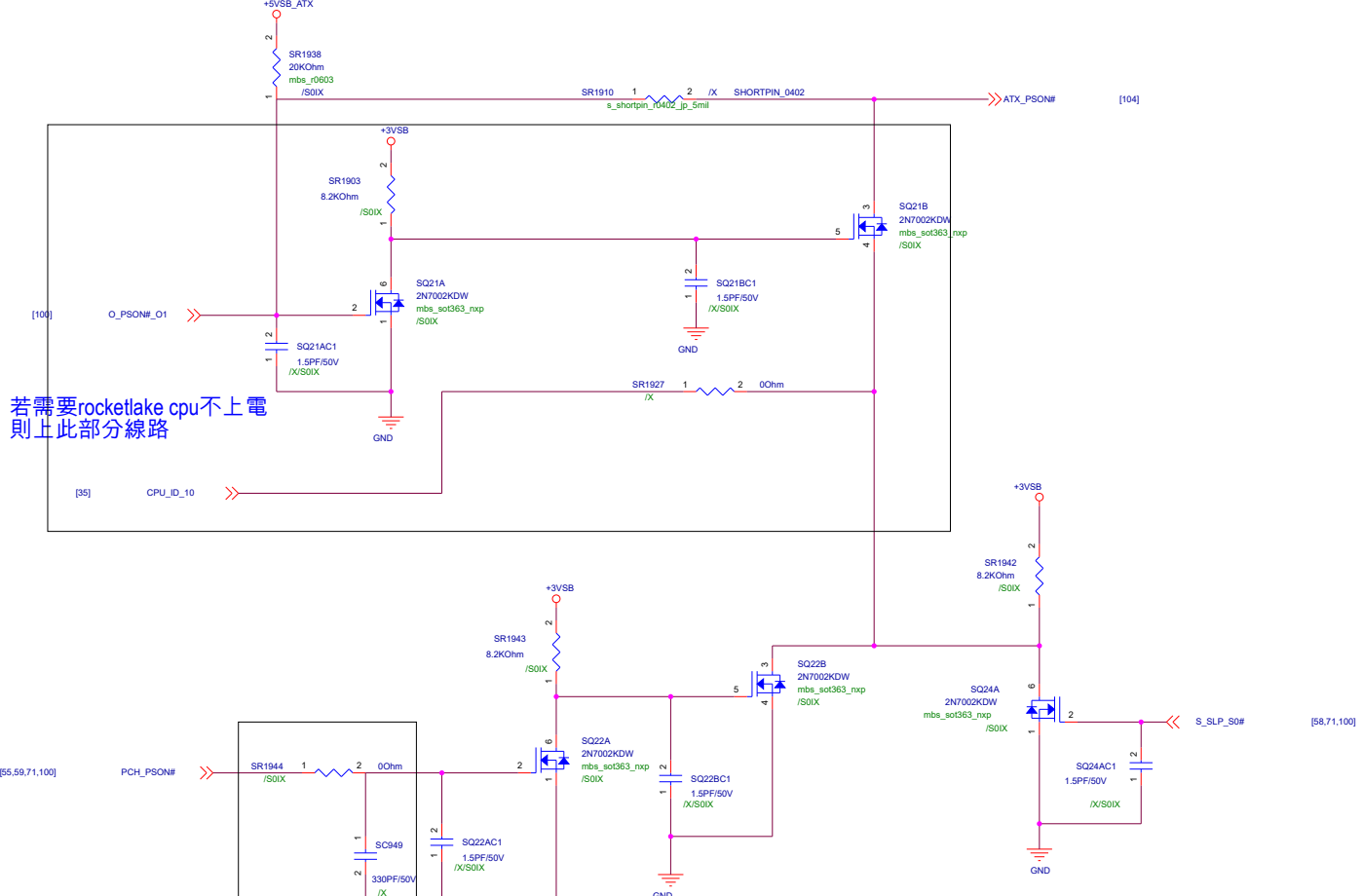
PL CAP



delete for 108x used

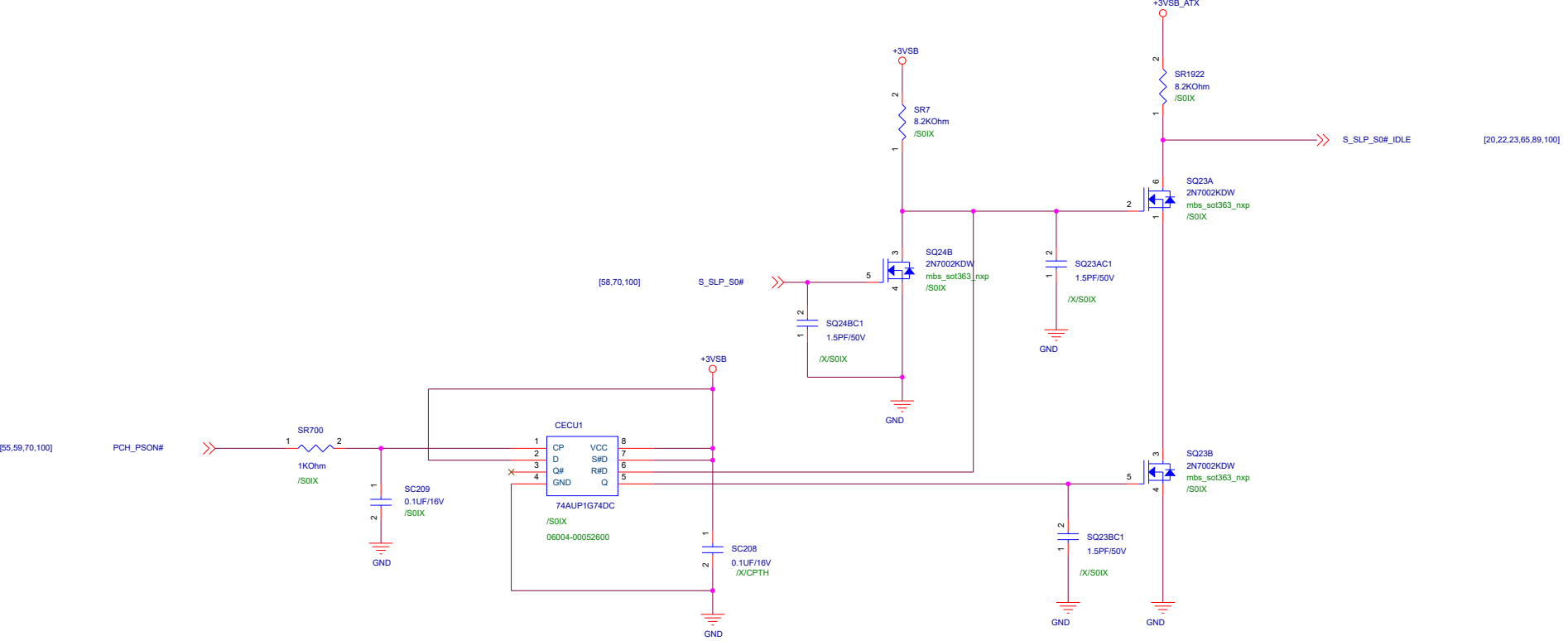
<Variant Name>

ASUSTek COMPUTER INC.	Title : PCIEX1_1	
	Engineer: KENNY_CHEN	
Size: A2	Project Name: Z87-PRO	Rev: R1.02A
Date: Friday, May 15, 2020	Sheet 69 of 115	



<Variant Name>

ASUSTEK COMPUTER INC	Title : PS_ON#	
	Engineer: Jay_Tong	
Size: A3	Project Name: Chipset Demo Circuit	Rev: 0.0
Date: Friday, May 15, 2020	Sheet 70 of 115	



<Variant Name>

ASUSTek Computer Inc.	Title :	
	Engineer:	Jay_Tong
Size: A3	Project Name: Standard Circiut	Rev: 0.01A
Date: Friday, May 15, 2020	Sheet 71 of 115	

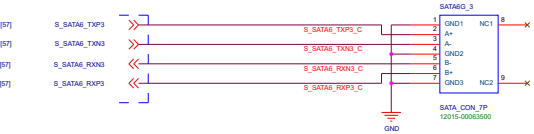
<Variant Name>

ASUSTek Computer Inc.	Title : HDMI	
	Engineer: alex_zhou	
Size: D	Project Name: Standard Circuit	Rev: 0.01A
Date: Monday, March 23, 2020	Sheet 72 of 113	

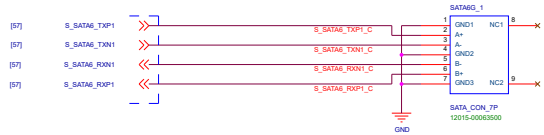
<Variant Name>

ASUSTek Computer Inc.	Title : HDMI	
	Engineer: alex_zhou	
Size: D	Project Name: Standard Circuit	Rev: 0.01A
Date: Monday, March 23, 2020	Sheet 73 of 113	

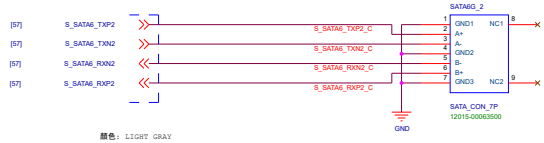
note：台北和蘇州機種去掉電容直連后在QTC測試PASS，經leaders討論后決定去除電容變為直連



180度connector



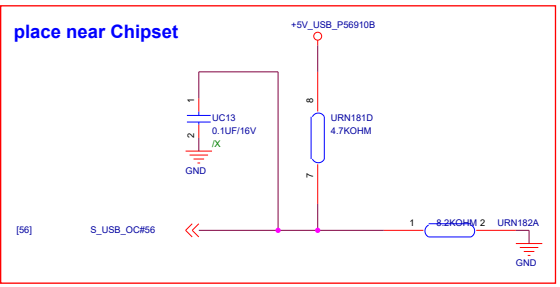
180度connector

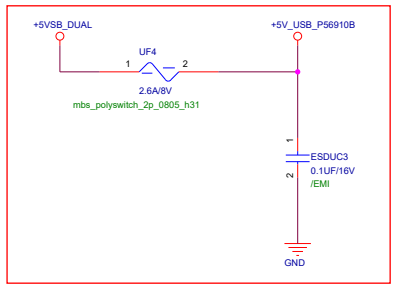


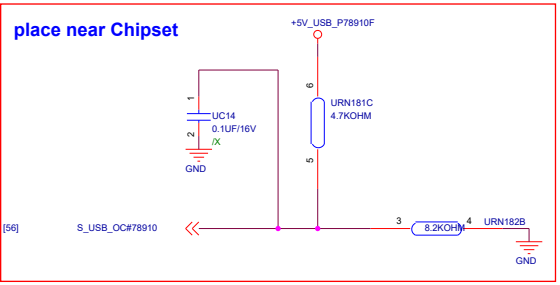
顏色：LIGHT GRAY

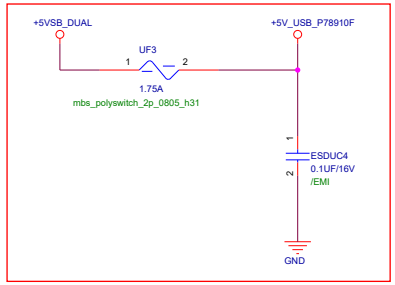
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, March 23, 2020	Sheet 75 of 133	

OC# circuit for Intel

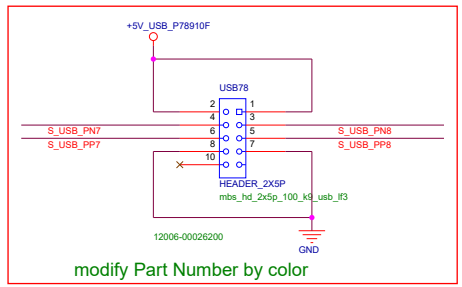


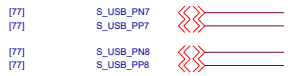






USB2 Header

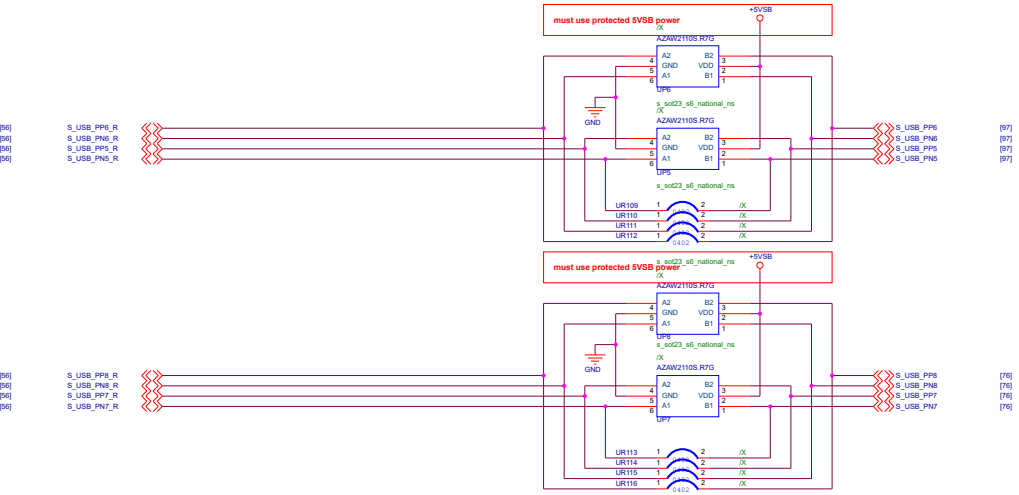




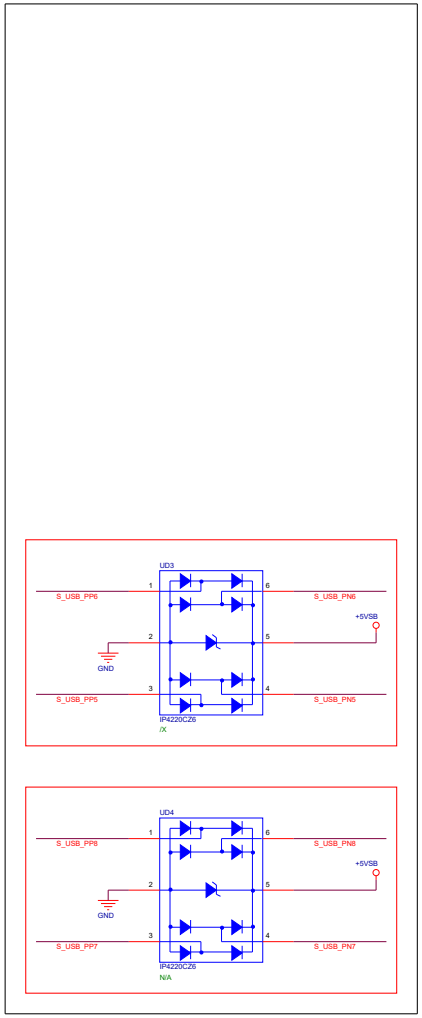
<Variant Name>

ASUSTEK COMPUTER INC	Title : USB2 Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Thursday, May 28, 2020	Sheet 76 of 100	

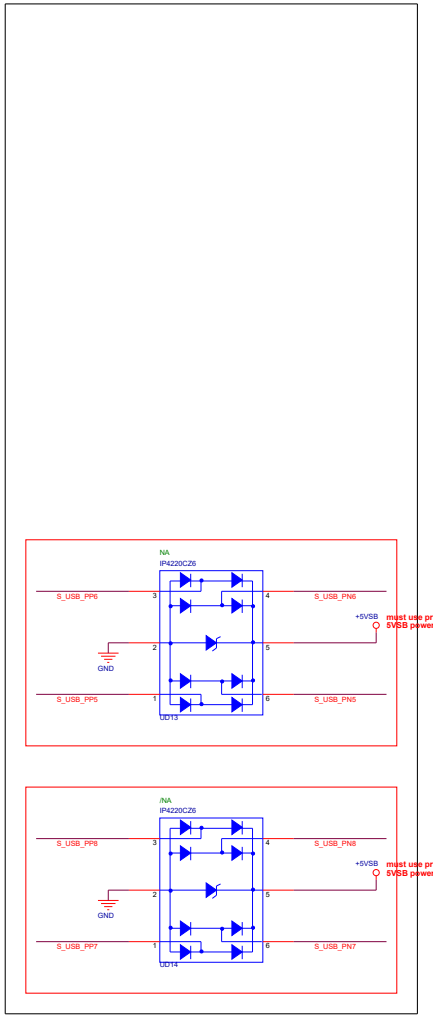
Reserve USB Guard with short pin



Delete it for EMS

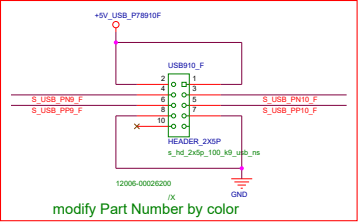


Delete it for EMS



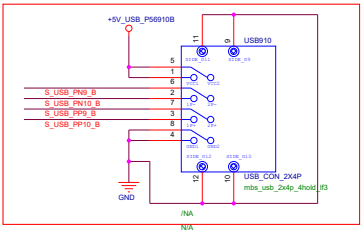
<Variant Name>

ASUSTEK COMPUTER INC	Title : USB2 Port	
	Engineer: Kell_Huang	
Size: A1	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Monday, May 18, 2020	Sheet 77 of 100	



[79] S_USB_PN10_F
[79] S_USB_PP10_F

[79] S_USB_PN9_F
[79] S_USB_PP9_F



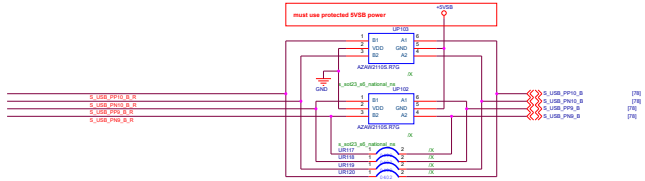
[79] S_USB_PN10_B
[79] S_USB_PP10_B

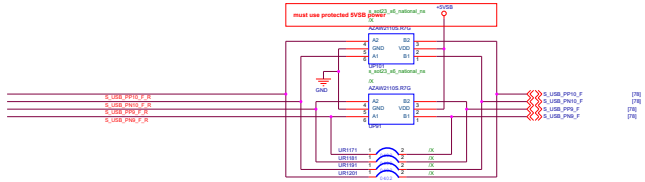
[79] S_USB_PN9_B
[79] S_USB_PP9_B

<Variant Name>

ASUSTEK COMPUTER INC	Title : USB2 Port Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Thursday, May 28, 2020	Sheet 78 of 100	

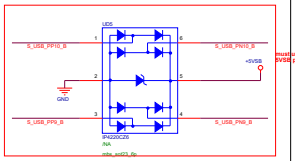
Reserve USB Guard with short pin



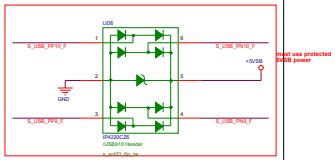


Delete it for EMS

ESD Diode

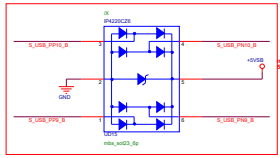


ESD Diode

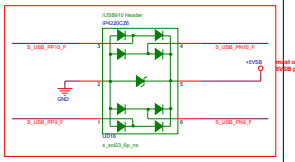


Delete it for EMS

2nd ESD Diode



2nd ESD Diode



<Variant Name>

ASUSTeK COMPUTER INC.

Title : USB2 Port

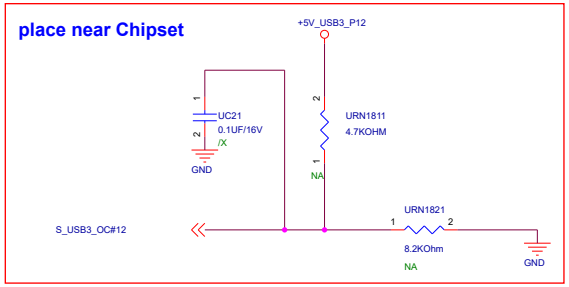
Engineer: Kell_Huang

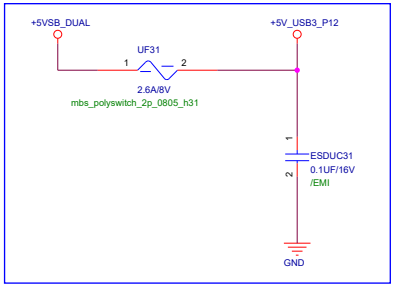
Size	Project Name	Rev
A1	Chipset USB Demo Circuit	0.0

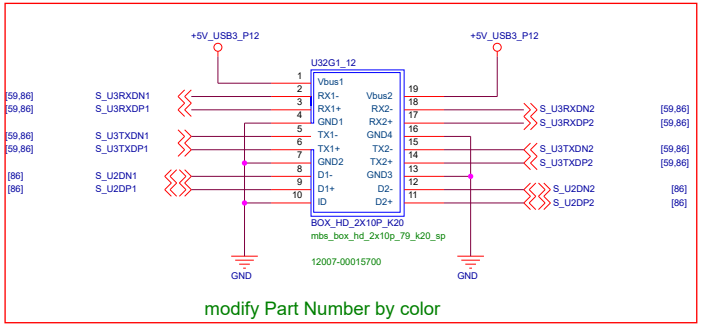
Date: Friday, May 29, 2020 Sheet 79 of 100

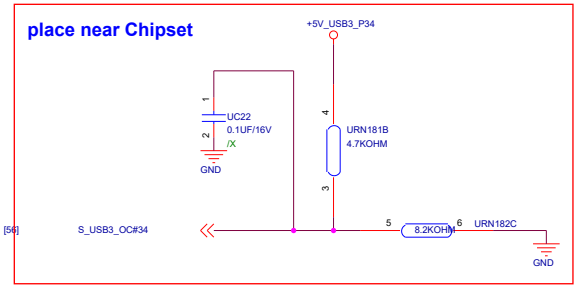
Title <Title>		
Size Custom	Document Number <Doc>	Rev <RevCode>
Date: Monday, March 23, 2020	Sheet 84 of 1	

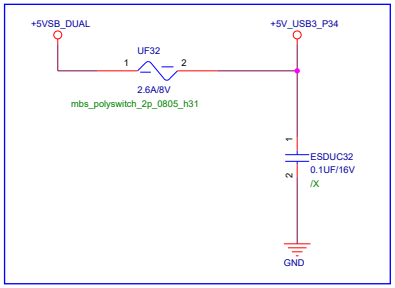
OC# circuit for Intel

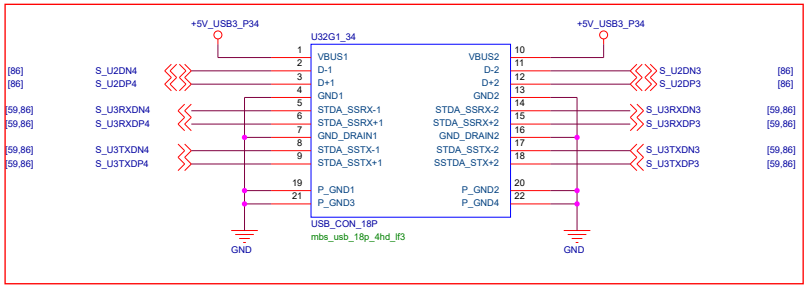












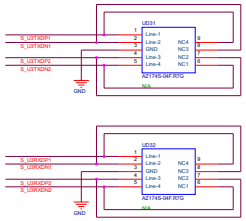
<Variant Name>

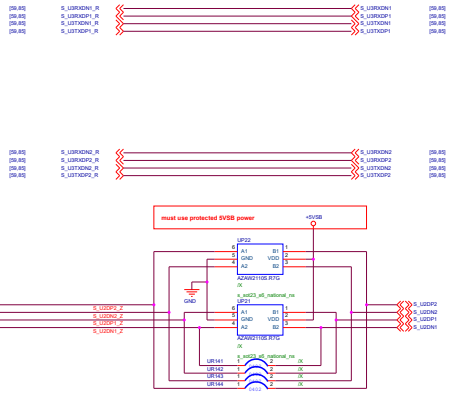
ASUSTEK COMPUTER INC	Title : USB3 Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Thursday, May 21, 2020	Sheet 85 of 100	

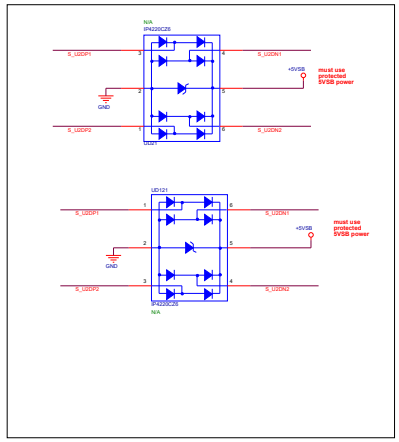
Port 12

Delete it for EMS

ESD Diode



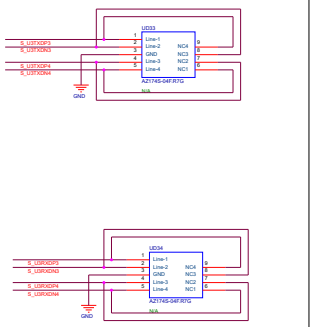


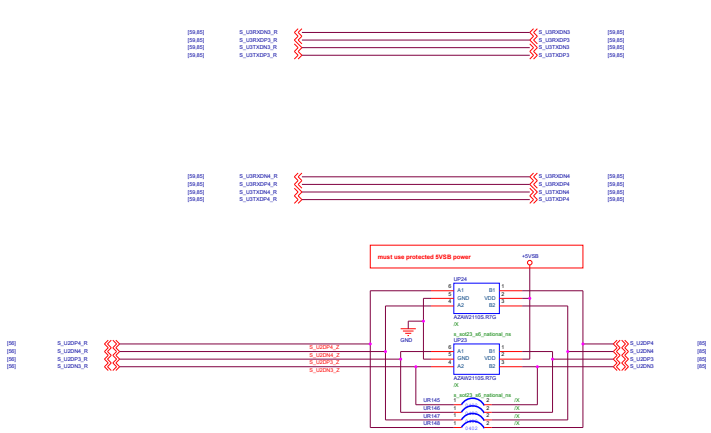


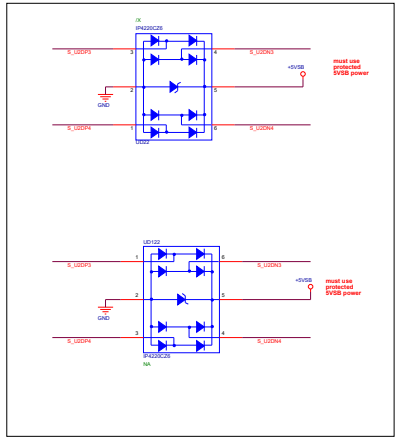
Port 34

Delete it for EMS

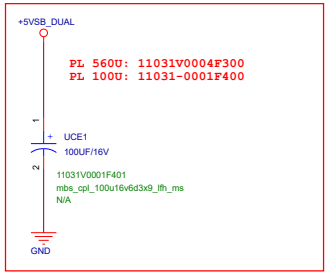
ESD Diode



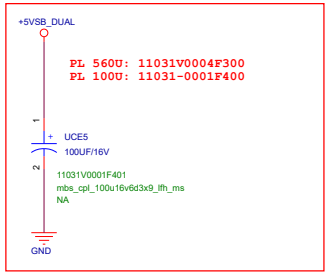


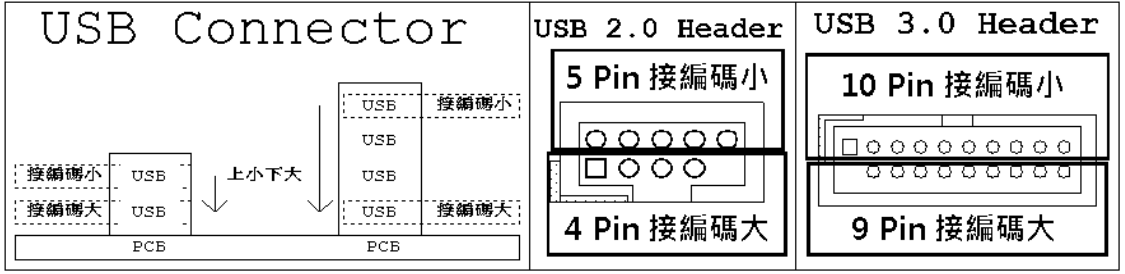


PL CAP

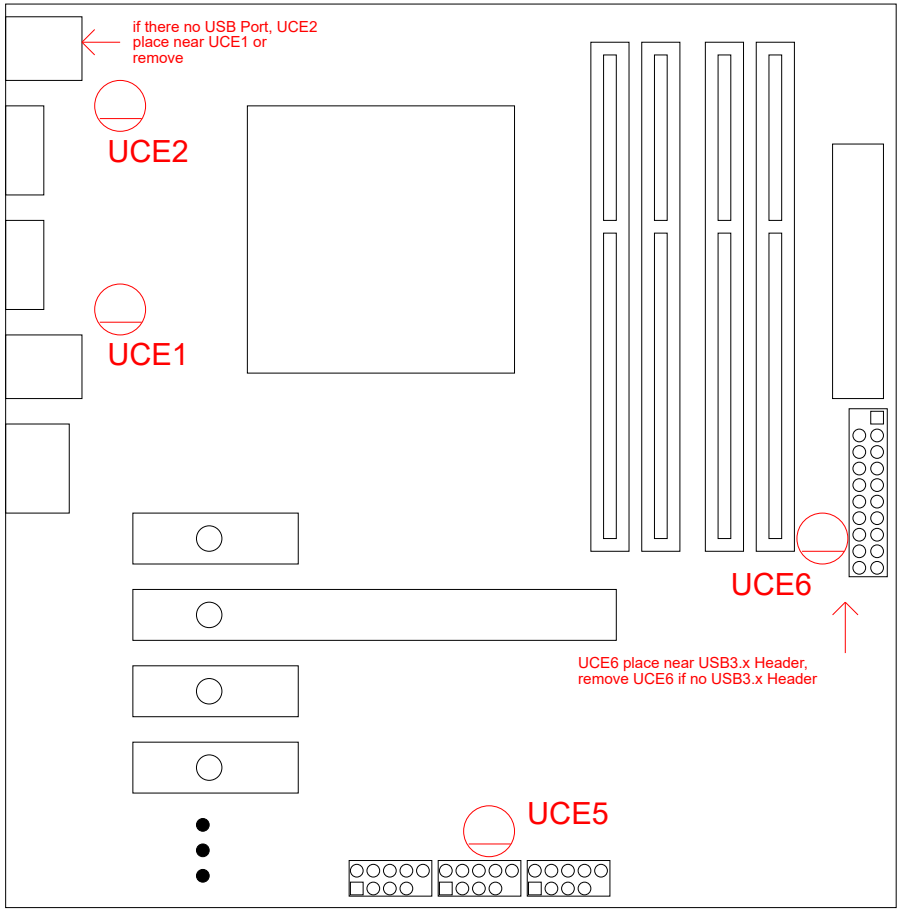


PL CAP





USB Power CAP recommend placement



<Variant Name>

ASUSTEK COMPUTER INC	Title :	USB Power CAP
	Engineer:	Kell_Huang
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Monday, April 27, 2020	Sheet 87 of 100	

+5VSB_DUAL current:
DIMM*4=7A, DIMM*2=5A, DIMM not generate from +5VSB_DUAL=0A
USB 2.0=0.5A/port
USB 3.x=1A/port
USB Type C=3A/port
if +5VSB_DUAL current (DIMM+USB 2.0 Port+USB 3.x Port) > 15A, add UQ706

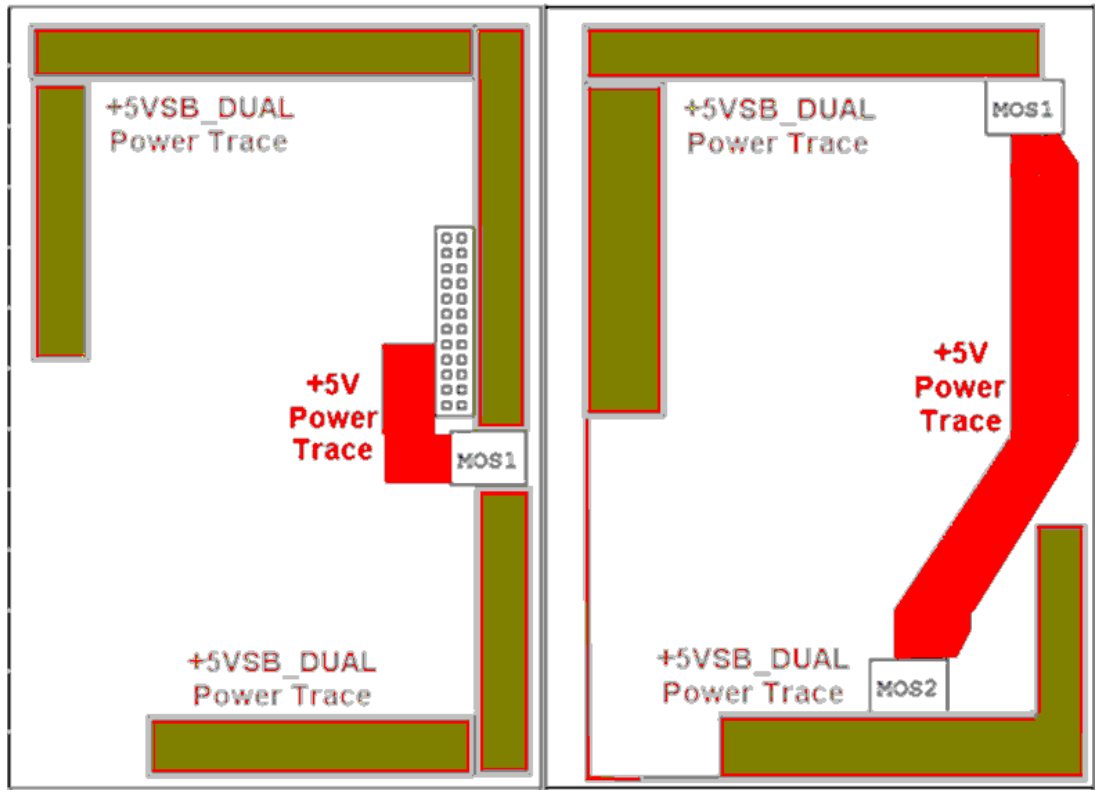
N-MOS	Max Current
Power PAK MOS 4 mohm	15A
Power PAK MOS 6 mohm	13A
DPAK MOS 9 mohm	10A

MOS 6 mohm

Max 13A

注意：
UQ706 請與 各自機種 power 部分PQ4500 用料 保持一致，
若用到UQ706機種by project自行修改用料
若1顆6 mOhm EA跨壓不過，請先將PQ4500換4m Ohm測試，
若仍不過，PQ4500 & UQ706各上1顆 6m Ohm測試

1. 當 +5VSB_DUAL current (DIMM+USB Port) <= 13A 時, N-MOS1 使用 Power PAK MOS 6 mohm, 沒有 N-MOS2
2. 當 13A < +5VSB_DUAL current (DIMM+USB Port) <= 15A 時, N-MOS1 使用 Power PAK MOS 4 mohm, 沒有 N-MOS2
3. 當 15A < +5VSB_DUAL current (DIMM+USB Port) <= 25A 時, N-MOS1 使用 Power PAK MOS, N-MOS2 使用 DPAK MOS 9 mohm
   <1> 當 DIMM 電流+ PCB Layout 由 N-MOS1 供電的 USB Port 電流 <= 13A 時, N-MOS1 使用 Power PAK MOS 6 mohm
   <2> 當 13A < DIMM 電流+ PCB Layout 由 N-MOS1 供電的 USB Port 電流 <= 15A 時, N-MOS1 使用 Power PAK MOS 4 mohm
4. 當 +5VSB_DUAL current (DIMM+USB Port) > 25A 時, 請與 Power Team 另外討論 N-MOS Solution
5. 若 Meomory Power 不是用 +5VSB_DUAL 產生, 則 DIMM 電流按 0A 計算
6. 因為 N-MOS1 在 Power Team Circuit 中, 請注意與 Power Team check Power Circuit 中 N-MOS1 是否正確
7. N-MOS2 若因為 PCB 面積不足放不下 DPAK MOS 9 mohm, 可改用 Power PAK MOS 6 mohm



<Variant Name>

ASUSTEK COMPUTER INC	Title : N-MOS2	
	Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Friday, March 20, 2020	Sheet 88 of 100	

USBPWR_SW# Circuit for Chipset GPIO

USBPWR_SW# GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down/pull-high resistor)
2. stand by power plane, 3V tolerance

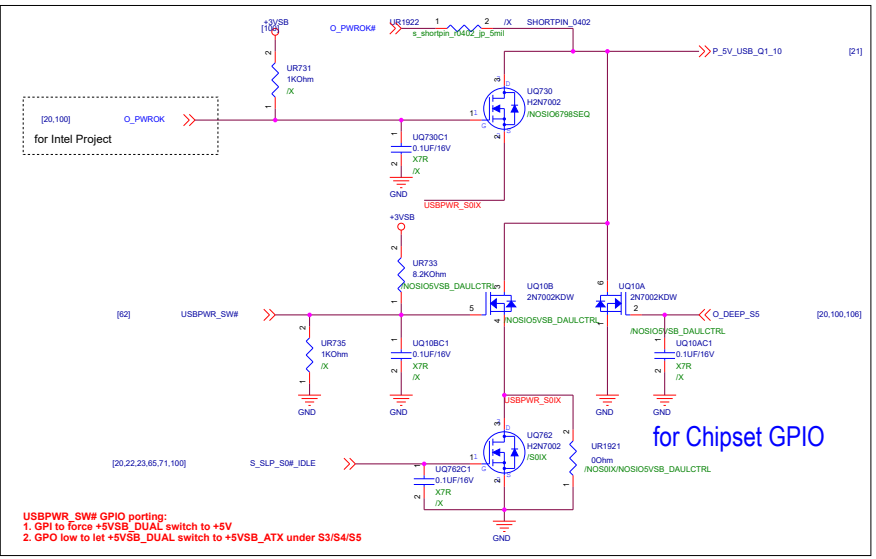
1. Choose USBPWR_SW# Circuit by Project

2. Check PWROK Signal Net Name by Platform

上件option說明：
若使用SIO6798D 5VSB_DUAL控制線路：/NOSIO5VSB_DAULCTRL 不上件
若不使用SIO6798D 5VSB_DUAL控制線路：/NOSIO5VSB_DAULCTRL 上件

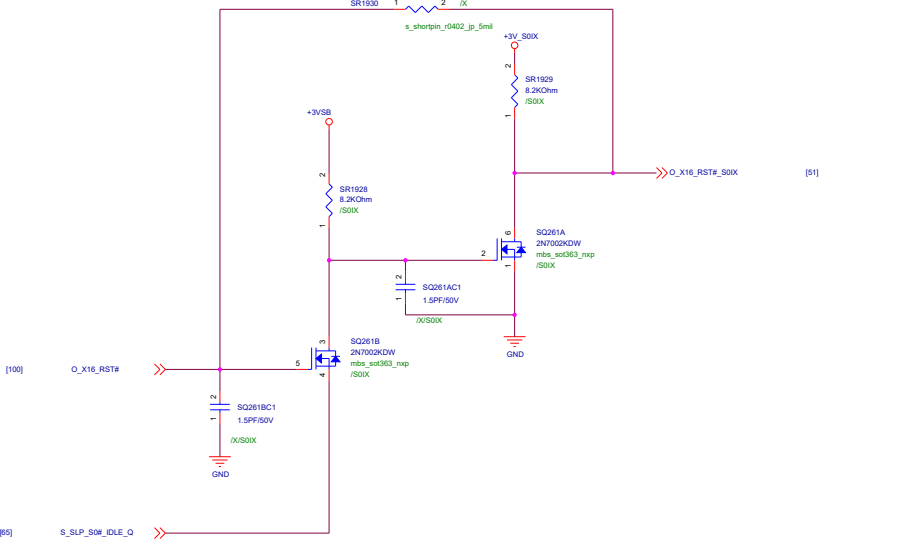
若使用SIO6798D 5VSB_DUAL控制線路：/SIO6798SEQ or /NOSIO6798SEQ可以2選1上件，但若上件/SIO6798SEQ，此時方框內其餘零件均不可上件
若不使用SIO6798D，/NOSIO6798SEQ & /NOSIO5VSB_DAULCTRL 都上件

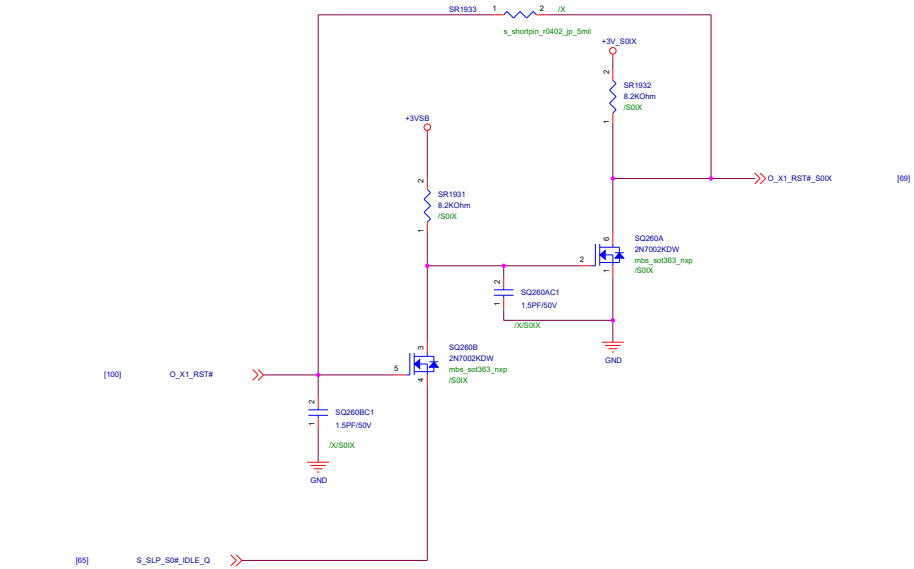
+5VSB_DUAL default no power, reserve USB Inrush Circuit



<Variant Name>

ASUSTEK COMPUTER INC	Title :	USB Power Control
	Engineer:	Kell_Huang
Size: A2	Project Name: Super I/O Demo Circuit	Rev: 0.0
Date: Friday, May 15, 2020	Sheet 89 of 112	

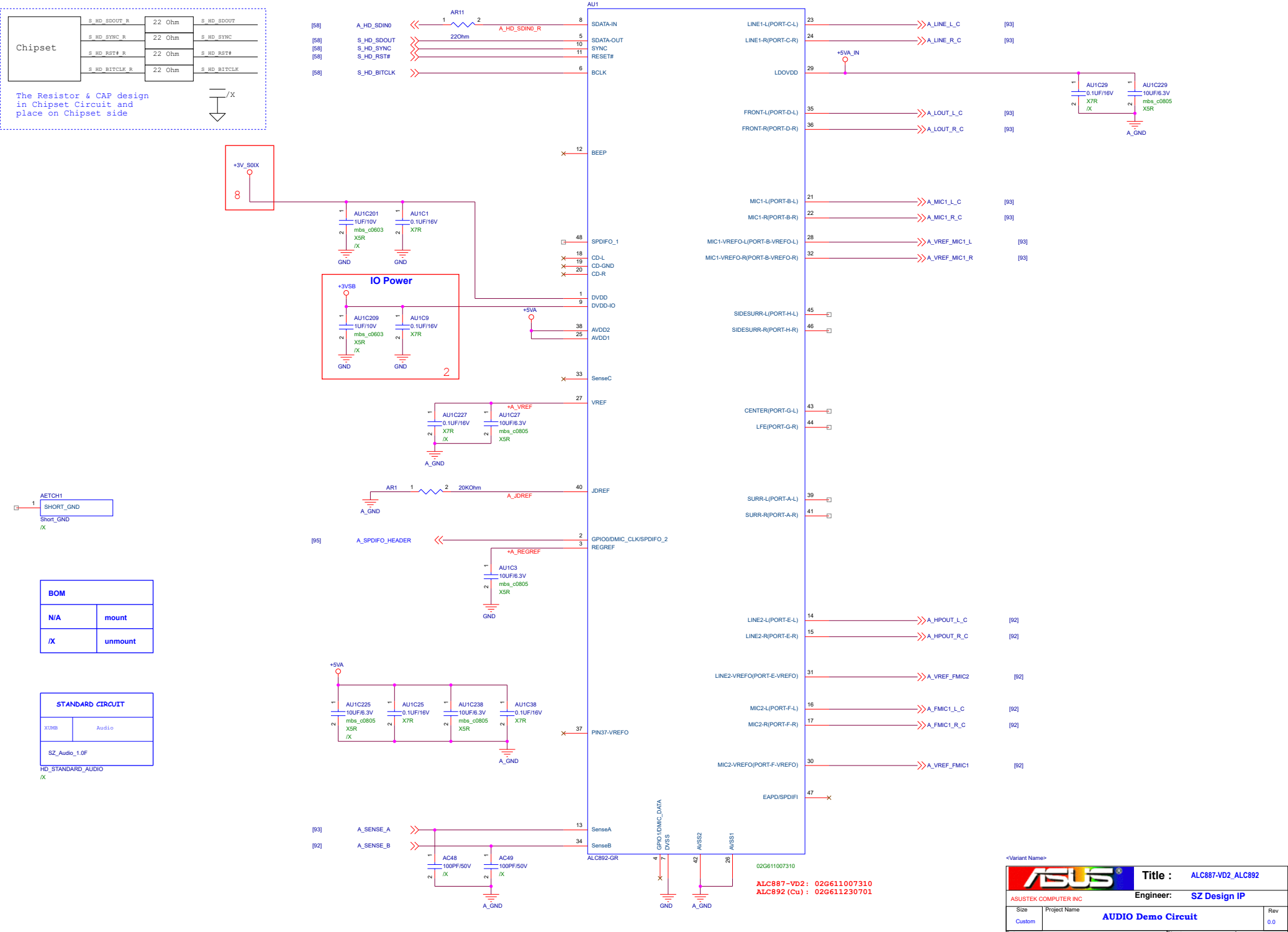




Title	<Title>	
Size: C	Document Number: <Doc>	Rev: <RevCode>
Date: Friday, May 15, 2020	Sheet 90 of 1	

ALC887-VD2 & ALC892 Circuit

1. Modify AU1 Part Number by Project
2. Modify IO Power by Project
3. Delete A_EAPD if not need
4. Delete A_SPDIFO_HEADER if not need
5. Delete A_SPDIFO_OPTICAL if not need
6. Delete Side Surround for Rear 3 Jacks or 5Jacks
7. Delete CEN/LFE & Surround for Rear 3 Jacks
8. Block 8,9, select one of them according if support s0ix

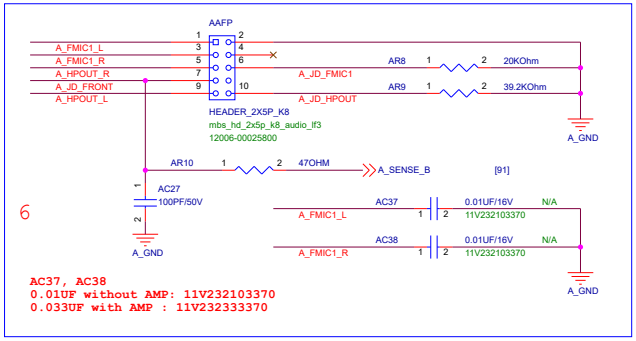


AAFP Circuit

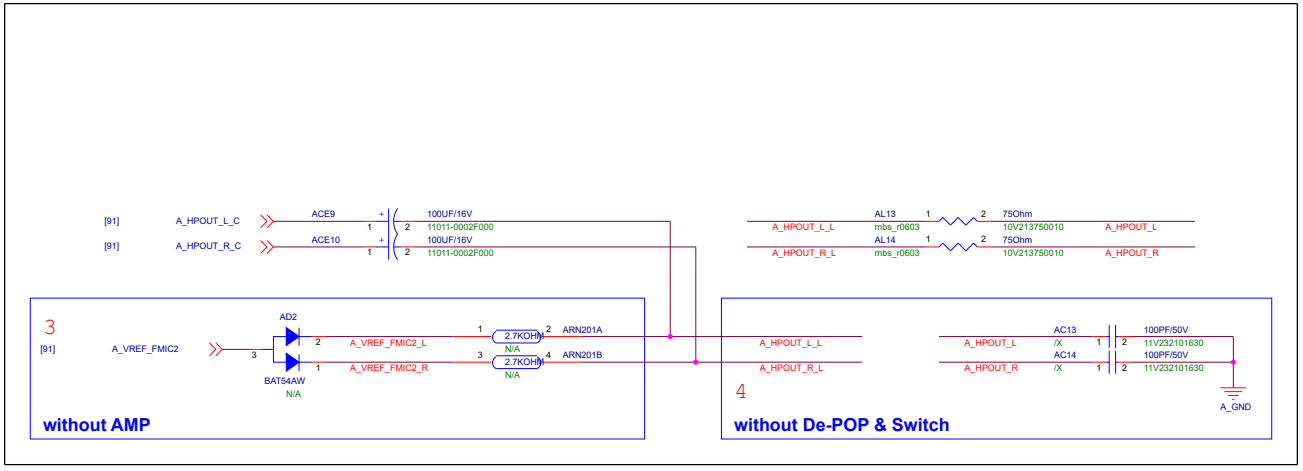
1. Choose AAFP Header Circuit by Codec,and change AAFP part number by your request,block 6,7, or 8
2. Choose HP Circuit with or without AMP/De-POP/Switch by Project,block 1,2,3,4
3. Modify ACE9, ACE10 Part Number by Project
4. IF you use 1220, AC13,AC14,AC15,AC16 option must change to N/A and change part number to varistor
5. Modify ARN202 value to 4.7k if you use 887,block 5
6. For Gamer Project with ALC1150, AL13, AL14 change to 47Ohm
7. change AC37,AC38 part number if you have AMP,block 6

AAFP

for ALC887-VD2/ALC892



for ALC887-VD2/ALC892/ALC1150/ALC1220X



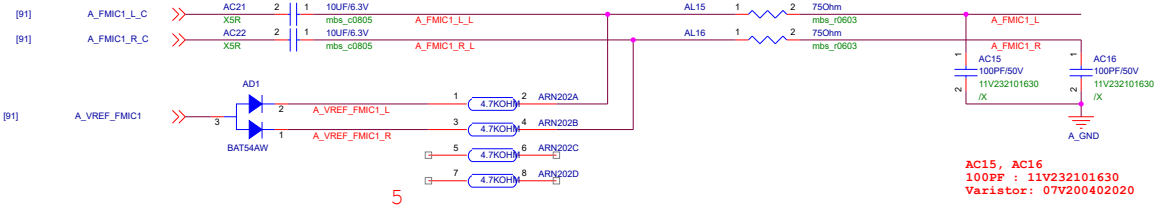
DIP CAP
EL 100U : 11V040107321
PL 100U : 11031V0001F000

AL13, AL14
75 Ohm: 10V213750010
47 Ohm: 10V213470010

AC13, AC14
100PF : 11V232101630
Varistor: 07V200402020

Taping DIP CAP
Chemicon 100U T: 11011-00024100
Elan 100U :11011-00025000
Nichicon 100U T: 11011-00026200

Taping DIP CAP
PL 100U T:11031V0001F400



AC15, AC16
100PF : 11V232101630
Varistor: 07V200402020

ARN202 change to 4.7K Ohm for ALC887-VD2

Delete it for EMS

<Variant Name>

ASUSTEK COMPUTER INC

Title : AAFP

Engineer: SZ Design IP

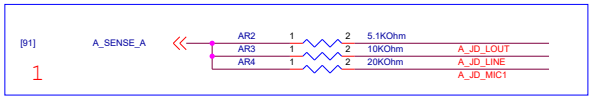
Size	Project Name	Rev
A3	AUDIO Demo Circuit	0.0

Date: Friday, May 15, 2020 Sheet 92 of 100

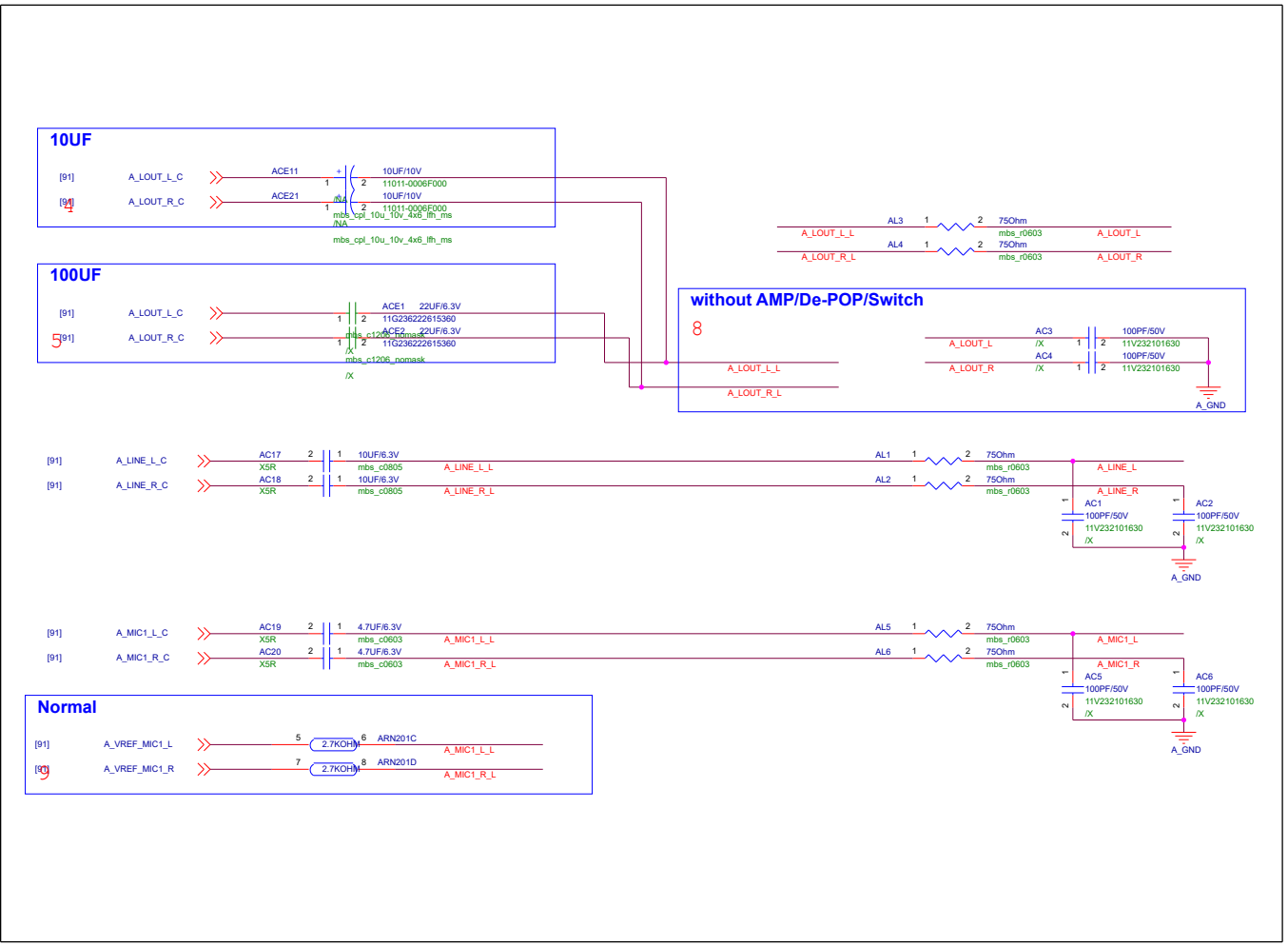
Rear 3Jacks Circuit

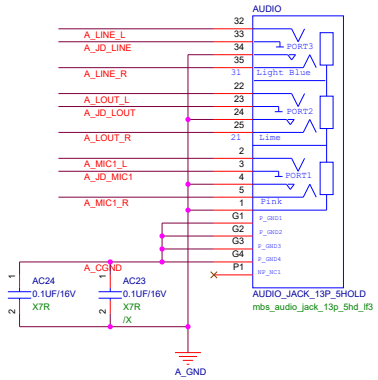
1. Choose Jack Detect Circuit by Codec,block 1,2,3
2. Choose LOUT DIP CAP Type by Codec & Project,block 4,5,6
3. Choose LOUT Circuit with or without De-POP/Switch by Project,block 7,8
4. Modify ACE1, ACE2 Part Number by Project
5. Choose Rear MIC VREF Circuit by Project ,block9,10
6. For Gamer/Gaming modity AC17, AC18 part by request
7 if you use 1220 ,Modify AC1,AC2,AC3, AC4, ,AC5,AC6, Part Number to varistor and Optional to N/A

for ALC887-VD2/ALC892



Delete it for EMS





Audio CAP using rule,pls change all dip caps partnumber according bellow rule

Z390,B450 ROG / Strix series	Nichicon
Z390,B450 PRIME / TUF Series	ELNA
Intel H310,H310C,H110&AMD A320 series	Chemicon
other chipsets except above series	Nichicon

DIP CAP
EL 10U : 11G040822620
PL 10U : 11V090106207

Taping DIP CAP
Chemicon 10U T: 11011-00064100
Elan 10U:11011-00065000
Nichicon 10U T: 11011-00066200

DIP CAP
EL 100U : 11V040107321
PL 100U : 11031V0001F000

Taping DIP CAP
Chemicon 100U T: 11011-00024100
Elan 100U :11011-00025000
Nichicon 100U T: 11011-00026200

AC1, AC2, AC3, AC4, AC5, AC6
100PF : 11V232101630
Varistor: 07V200402020

Taping DIP CAP
PL 100U T:11031V0001F400

<Variant Name>

ASUSTEK COMPUTER INC

Title : 3 Jacks

Engineer: SZ Design IP

Size	Project Name	Rev
A3	AUDIO Demo Circuit	0.0

Date: Thursday, May 28, 2020 Sheet 93 of 100

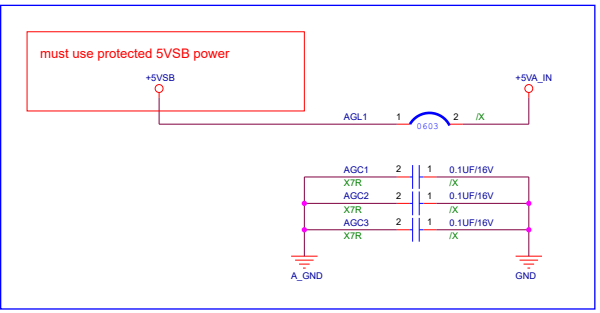
Audio GAP & Power Circuit

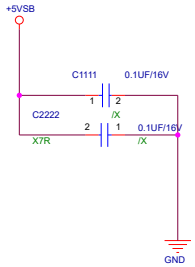
1. Choose Resistor & Capacitor over GAP Circuit by Project

2. Keep or delete Audio Power LDO Circuit by Project

3. Modify APCE4 Part Number by Project

Normal Gap





BOM	Audio Power from 5VSB	Audio Power from 12V LDO 5V
/AUDIO_PWR_5VSB	mount	unmount
/AUDIO_PWR_LDO	unmount	mount

<Variant Name>

ASUSTEK COMPUTER INC

Title : GAP_Power

Engineer: SZ Design IP

Size	Project Name	Rev
A3	AUDIO Demo Circuit	0.0

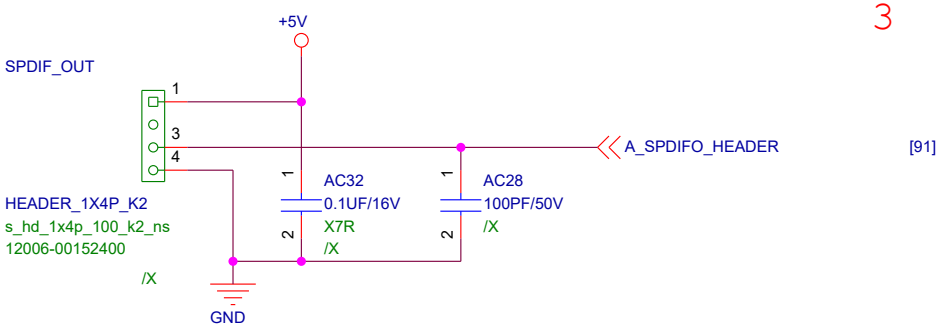
Date: Monday, April 13, 2020 Sheet 94 of 100

SPDIF

1. select block 1,2, or 3 by project

SPDIF Header

3



<Variant Name>

ASUSTEK COMPUTER INC	Title : SPDIF	
	Engineer: SZ Design IP	
Size: A	Project Name: AUDIO Demo Circuit	Rev: 0.0
Date: Friday, May 15, 2020	Sheet 95 of 100	

RTL8111H/L8200A Circuit

A. Modify PCIE Reset Signal Net Name by Project

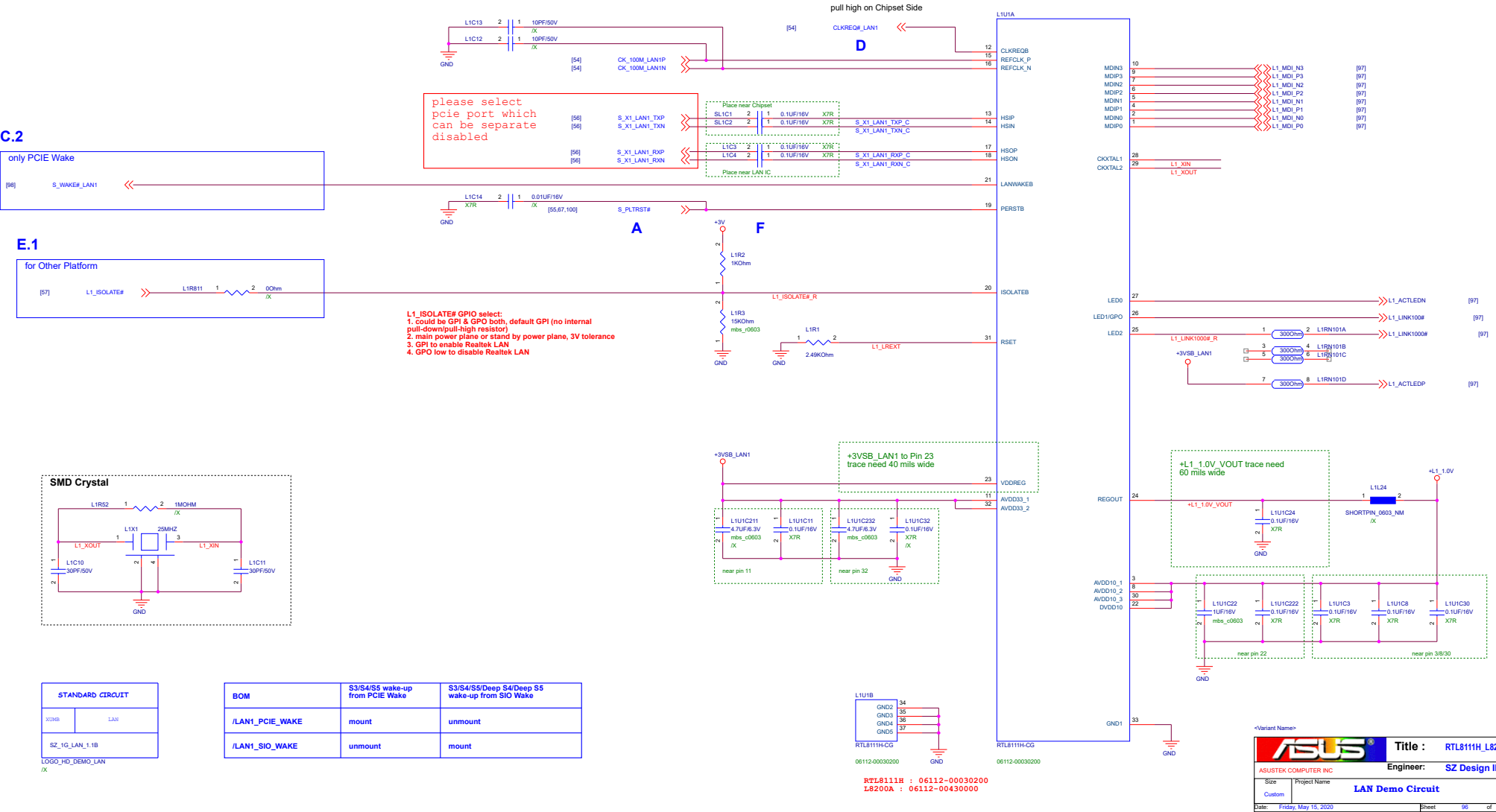
B. Modify L1U1 Part Number by Project

C. Choose Wake-up Signal Circuit by Project

D. Delete CLKREQ#_LAN1 if not need

E. Choose L1_ISOLATE# Circuit by Project

F. Modify +3V to +3V_S0IX if support Intel S0ix



STANDARD CIRCUIT	
XIMB	LAN
SZ_1G_LAN_1.1B	

LOGO_HD_DEMO_LAN
/X

BOM	S3/S4/S5 wake-up from PCIE Wake	S3/S4/S5/Deep S4/Deep S5 wake-up from SIO Wake
/LAN1_PCIE_WAKE	mount	unmount
/LAN1_SIO_WAKE	unmount	mount

RTL8111H : 06112-00030200
L8200A : 06112-00430000

<Variant Name>

ASUSTEK COMPUTER INC

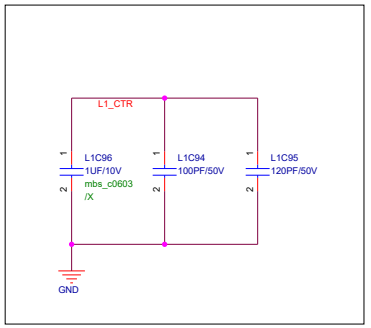
Title : RTL8111H_L8200A

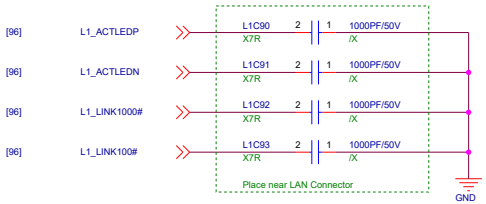
Engineer: SZ Design IP

Size: Custom | Project Name: LAN Demo Circuit | Rev: 0.0

Date: Friday, May 15, 2020 | Sheet 98 of 100

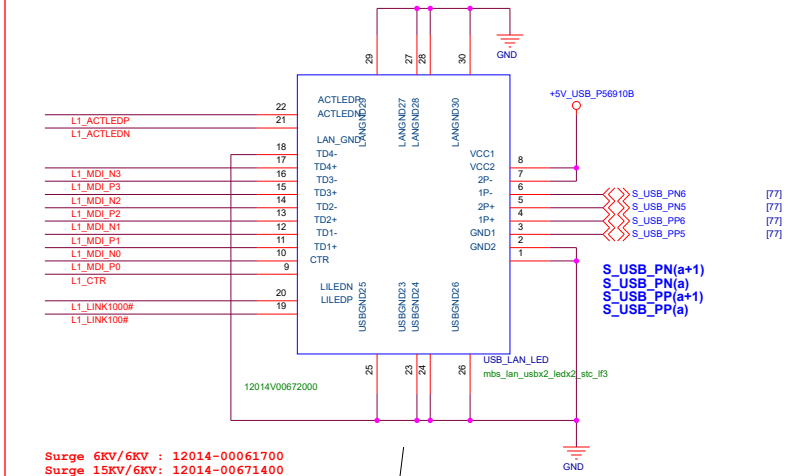
for Realtek LAN





GLAN + USB2 *2 Connector

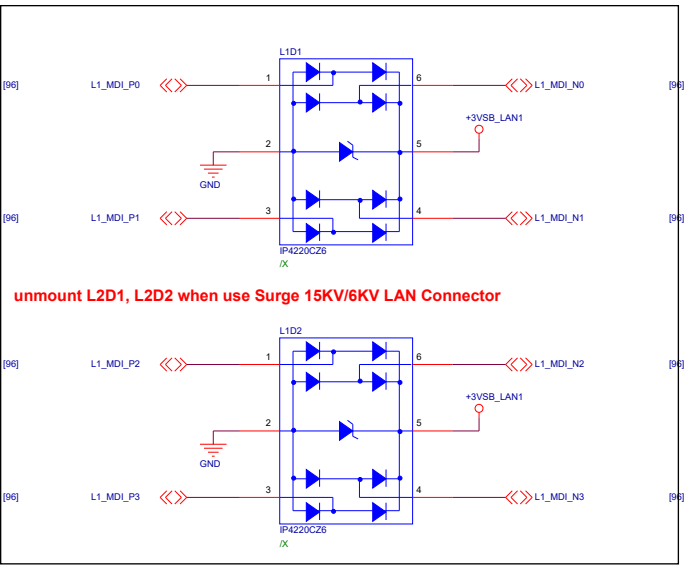
single LAN named LAN_USBxx
dual LAN named LAN1_USBxx



Surge 6KV/6KV : 12014-00061700
Surge 15KV/6KV: 12014-00671400

SUPPORT POE donot use Pajero

Delete it for EMS

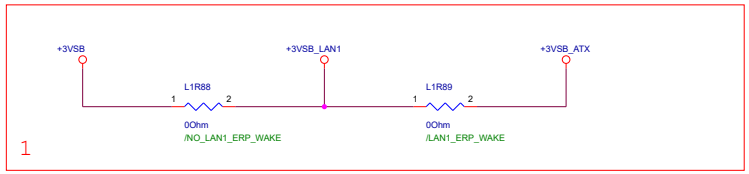


<Variant Name>

ASUSTEK COMPUTER INC	Title :	LAN Connector
	Engineer:	SZ Design IP
Size: A3	Project Name: LAN Demo Circuit	Rev: 0.0
Date: Friday, May 15, 2020	Sheet 97 of 116	

LAN1 Deep S4/S5 Wake-up Circuit

1. Remove Short-Pin L1R88 in LAN1 IC Page



for Intel PHY

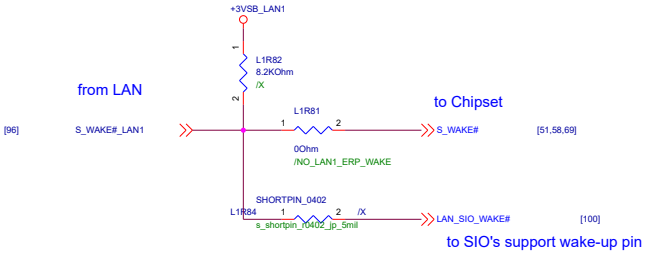
2. for Intel PHY LAN, L1_LAN_DISABLE# renamed L1_LAN_DISABLE#_R in LAN1 IC Page

3. for Intel PHY LAN, L1_LAN_WAKE# renamed L1_LAN_WAKE#_R in LAN1 IC Page

for PCIE LAN1

4. for PCIE LAN, S_WAKE# renamed S_WAKE#_LAN1 in LAN1 IC Page

5. for Intel PCIE LAN, make sure L1_DEV_OFF# choose +3VSB_ATX power plane GPIO



<Variant Name>

ASUSTEK COMPUTER INC	Title : Deep S4/S5 Wake	
	Engineer: SZ Design IP	
Size: A3	Project Name: LAN Demo Circuit	Rev: 0.0
Date: Friday, May 15, 2020	Sheet 98 of 123	

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, March 20, 2020	Sheet 99 of 1	

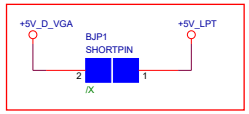
LPT Circuit

A. Choose use Single Resistor or RES_A by Project

B. Choose LPT Port Connector/Header Type

C. Modify Part Number of LPT Connector/Header by Color

Power from VGA Port

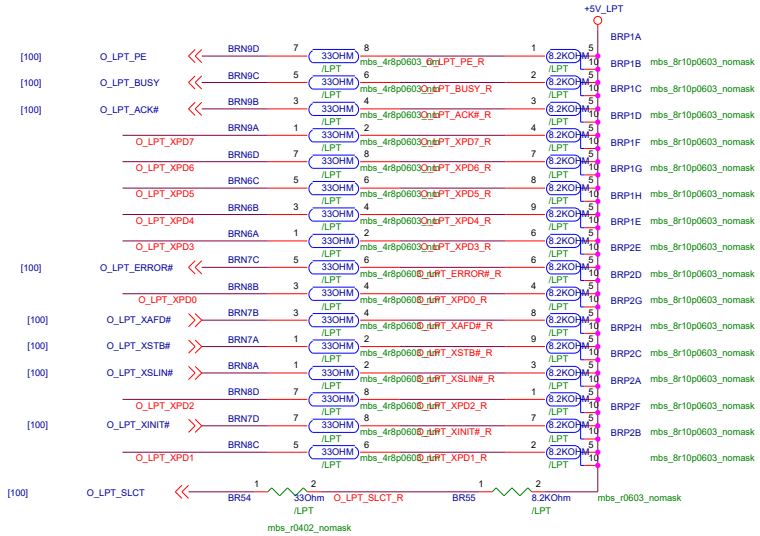


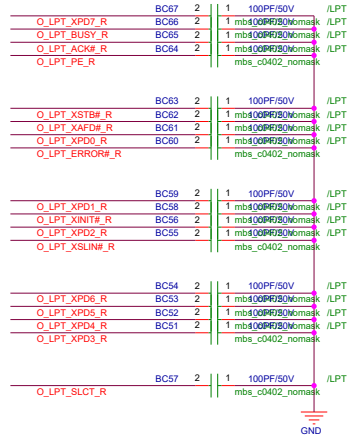
LPT PORT

[100] O_LPT_XPD[7..0]

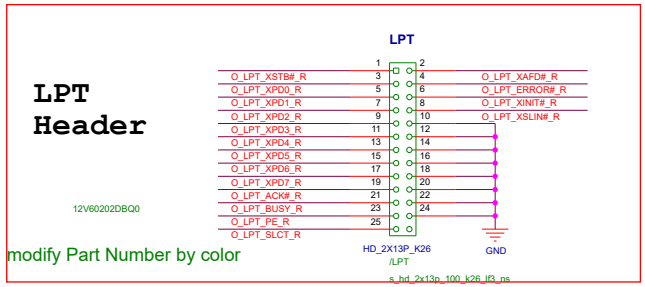
A.2

RES A





B.2



BOM	need LPT Port	no LPT Port
/LPT	mount	unmount

<Variant Name>

ASUSTEK COMPUTER INC

Title : LPT

Engineer: SZ Design IP

Size	Project Name	Rev
A3	Super I/O Demo Circuit	0.0

Date: Wednesday, May 27, 2020 Sheet 101 of 100

COM Circuit

A. Choose COM Port Connector/Header Type

B. Choose use RI# to do LAN wake-up from SIO or not by Project

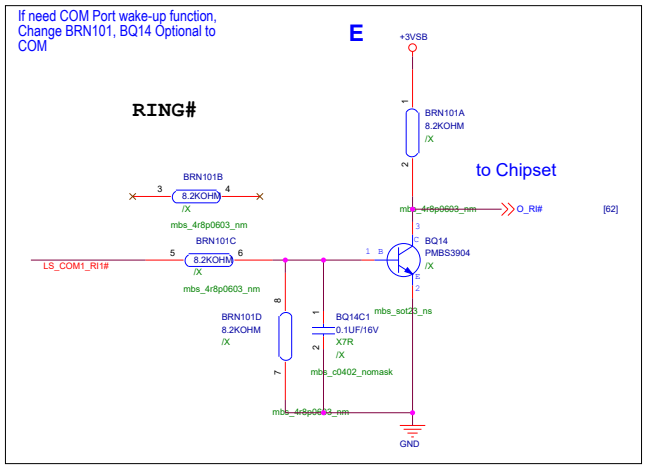
C. Modify Part Number of COM Connector/Header by Color

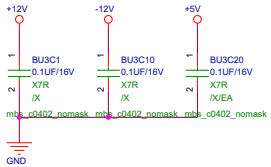
D. Keep or delete O_RI# Circuit by Project

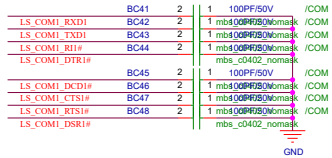
E. Modify O_RI# pill-high power by Project

COM PORT

D

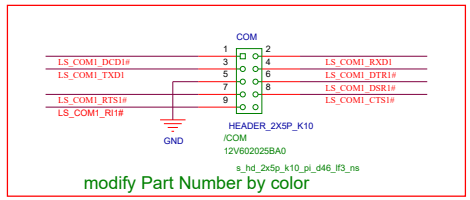






A.2

COM Header

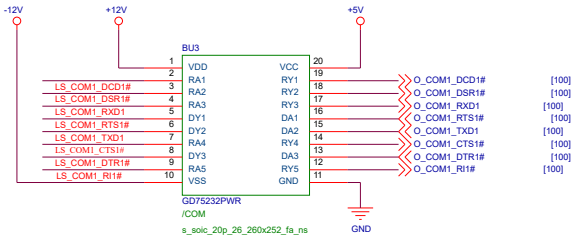


for use COM Port RI# to do LAN wake-up from SIO function

modify SIO RI# Pin net name to LAN_SIO_WAKE#

for not use COM Port RI# to do LAN wake-up from SIO function

B.2



When mount /COM

LAN wake-up from SIO	O1R171	O1Q171 & O1D171
support	unmount	mount
not support	mount	unmount

BOM	need COM Port	no COM Port
/COM	mount	unmount

When unmount /COM

LAN wake-up from SIO	O1R171	O1Q171 & O1D171
support	unmount	unmount
not support	unmount	unmount

<Variant Name>

ASUSTEK COMPUTER INC

Title : COM

Engineer: SZ Design IP

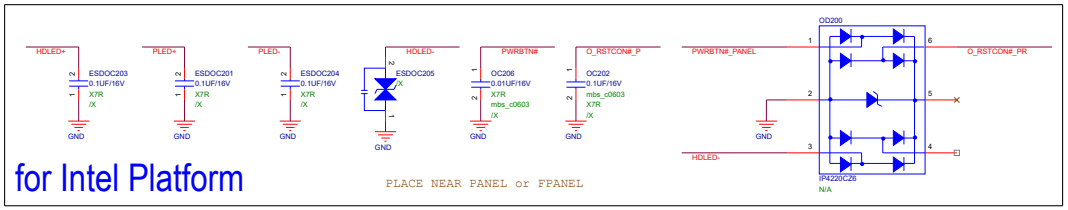
Size	Project Name	Rev
A3	Super I/O Demo Circuit	0.0

Date: Wednesday, May 27, 2020 Sheet 102 of 100

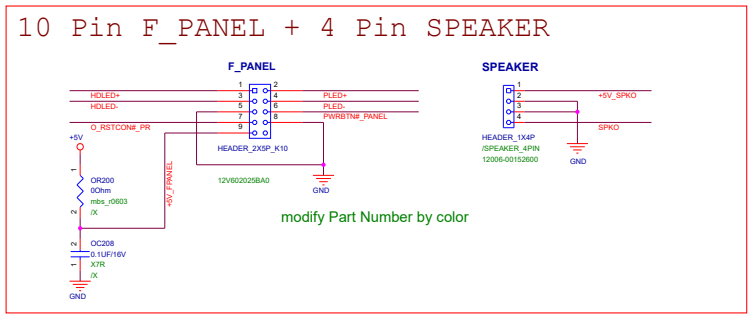
Panel Circuit

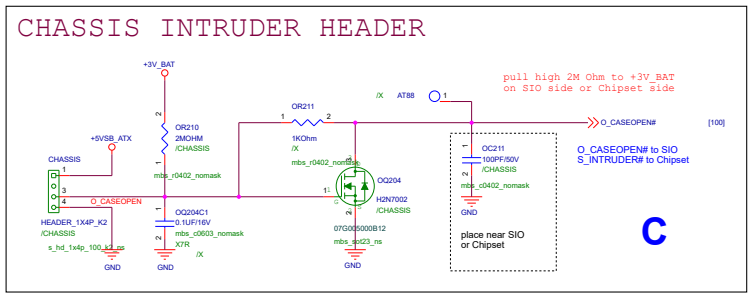
A. Choose PANEL/F_PANEL Signal ESD Solution by Project
B. Choose PANEL/F_PANEL Circuit + Chassis Inturder Circuit by Project
C. Choose Chassis Inturder Signal connect to SIO or Chipset by Project
D. Choose SPEAKER Header Circuit + BUZZER Circuit by Project
E. Choose PLED Circuit by Project
F. Choose PLED control by SIO or Chipset
G. If use Memory Power control PLED, check Memory Power Net Name
H. Modify Part Number of PANEL/F_PANEL/SPEAKER Header by Color

A.1



B.1



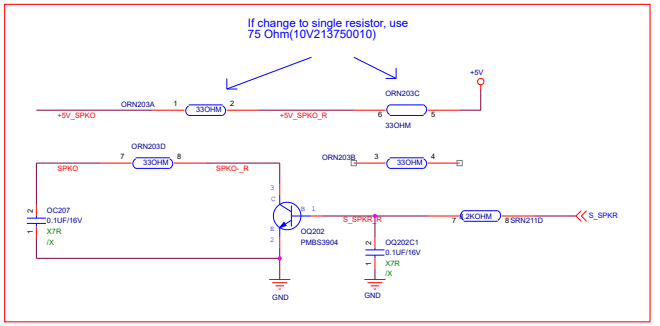


BOM	need SPEAKER	no SPEAKER
/SPEAKER_4PIN	mount	unmount

BOM	need BUZZER	no BUZZER
/BUZZER	mount	unmount

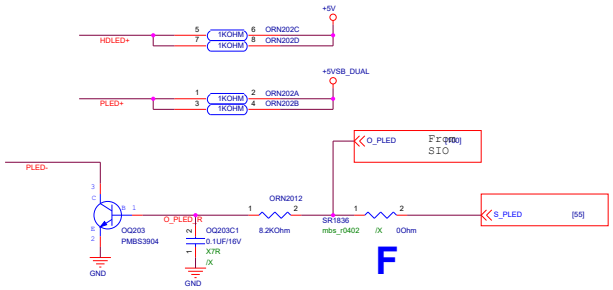
BOM	need CHASSIS	no CHASSIS
/CHASSIS	mount	unmount

D.1



E.1

Power LED power source use +5VSB



O_PLED/S_PLED GPIO select:
1. GPIO with blink function, default GPI(no internal pull-down resistor)
2. stand by power plane, 3V tolerance
3. Porting Guide: default keep GPI, enable blink 0.5Hz or 1Hz function when enter S3, disable blink function and back to GPI when resume from S3

<Variant Name>

ASUSTEK COMPUTER INC

Title : PANEL
Engineer: SZ Design IP
Size: Custom
Project Name: Super I/O Demo Circuit
Rev: 0.0
Date: Wednesday, May 27, 2020
Sheet 103 of 100

EATX Power Circuit

A. Choose EATX Power Circuit by Project

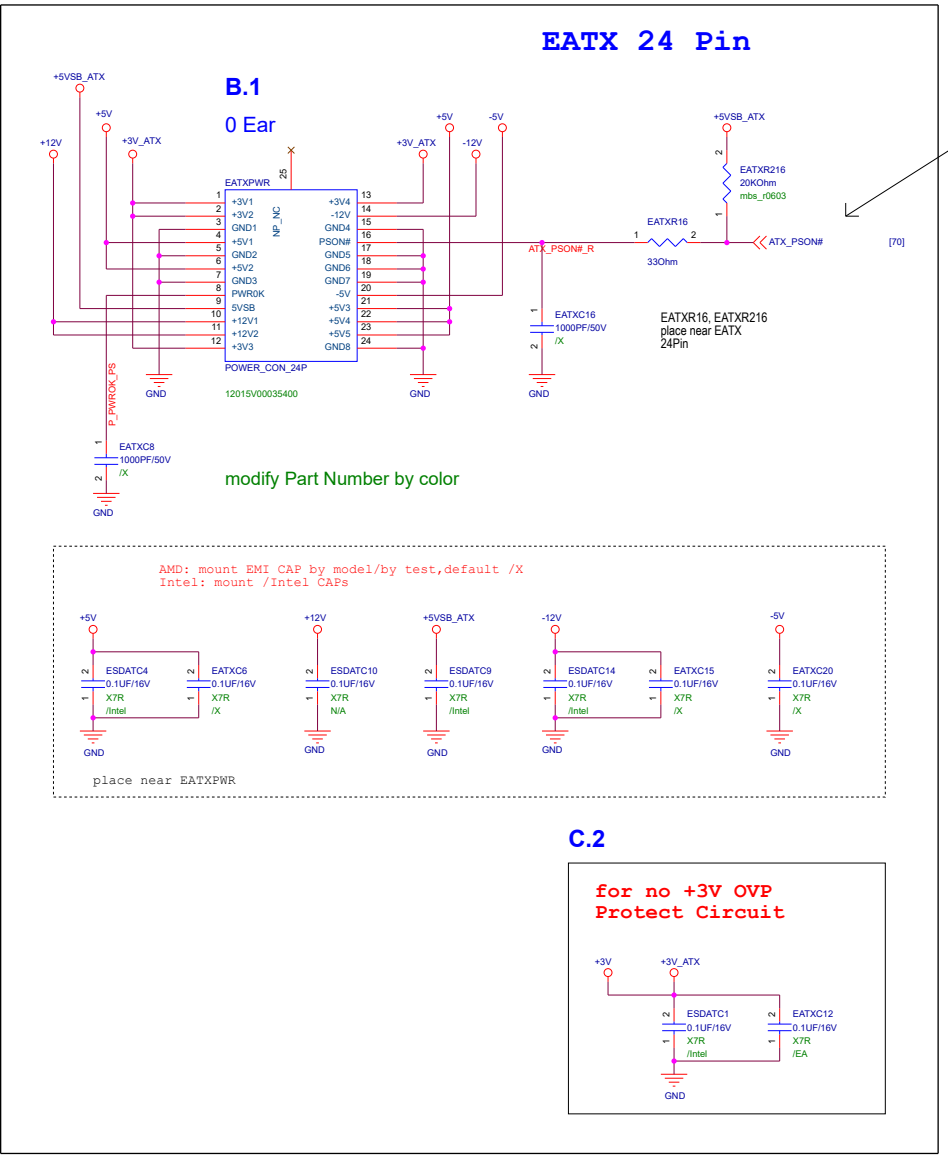
B. If choose EATX 24Pin Circuit, choose EATX Connector with 0 Ear, 1 Ear or 2 Ears by Project

C. If choose EATX 24Pin Circuit, choose +3V_ATX & +3V Circuit by Project

D. If support Intel S0ix, add SC945, SC946 & Off-Page Net O_PSON#_O1 change to ATX_PSON#

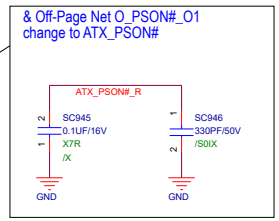
E. Modify Part Number of EATX Connector by Color

A.1



D

for S0ix



<Variant Name>

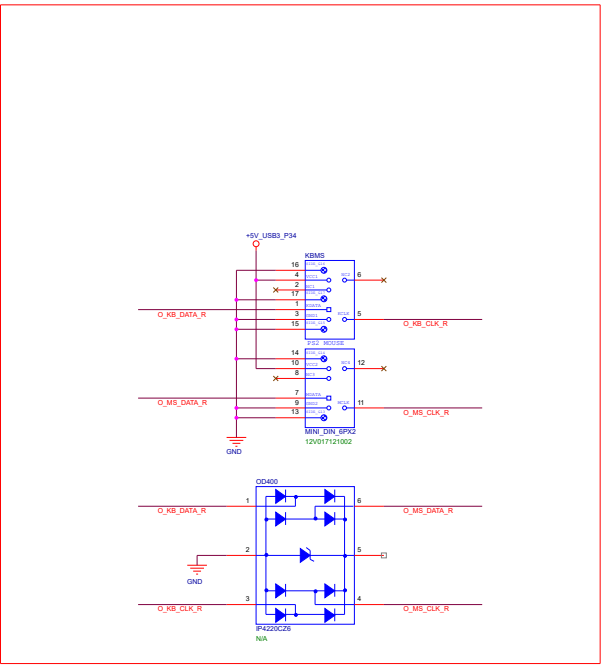
ASUSTEK COMPUTER INC	Title : EATX	
	Engineer: SZ Design IP	
Size: Custom	Project Name: Super I/O Demo Circuit	Rev: 0.0
Date: Thursday, May 21, 2020	Sheet 104 of 100	

KBMS Circuit

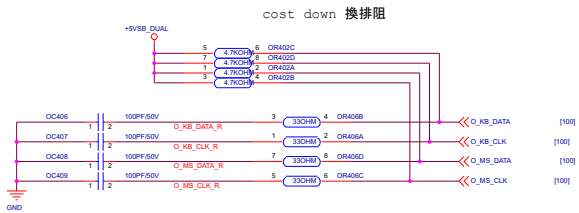
A. Choose KBMS Power Source by Project
B. If KBMS share power with USB Port, modify Share Power Net Name by Project
C. Choose KBMS Port Connector by Project
D. If choose KB & USB 2.0 Connector, check USB 2.0 Port D+/D- Signal begin with 0 or 1, then modify USB 2.0 Port D+/D- Signal Net Name by Project
E. If choose KB & USB 3.0 Connector, modify USB Port TX/RX/D+/D- Signal Net Name by Project
F. If choose KB & USB Connector, modify USB Port Power Net Name by Project
G. If choose KB & USB Connector, modify Connector Part Reference by Project

C.2

KBMS



KBMS



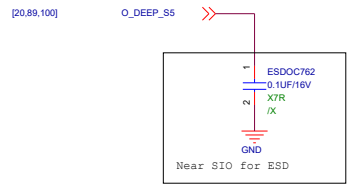
<Variant Name>

ASUSTEK COMPUTER INC	Title : KBMS	
	Engineer: SZ Design IP	
Size: Custom	Project Name: Super I/O Demo Circuit	Rev: 0.0
Date: Friday, May 15, 2020	Sheet 105 of 100	

ERP Circuit

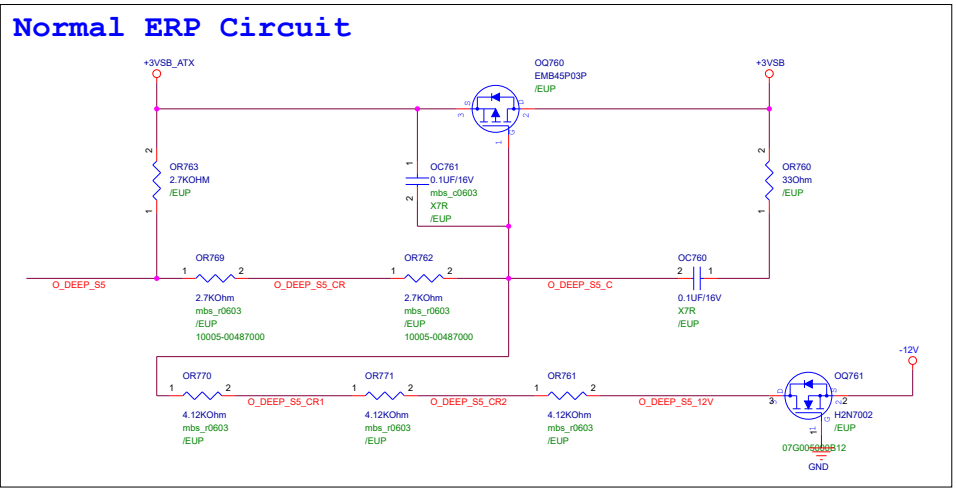
A. Choose ERP Circuit by Project

B. OR764, OR765 choose Short-Pin, Resistor or delete by Project

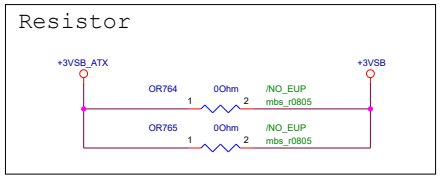


BOM	no SIO ERP & SIO DSW	SIO ERP	SIO DSW
/NO_EUP	mount	unmount	unmount
/EUP	unmount	mount	mount
/NO_SIODSW	mount	mount	unmount
/SIODSW	unmount	unmount	mount

A.2



B.2



<Variant Name>

ASUSTEK COMPUTER INC

Title : ERP

Engineer: SZ Design IP

Size	Project Name	Rev
A3	Super I/O Demo Circuit	0.0

Date: Friday, May 15, 2020 Sheet 106 of 100

Stand By LED & HW Monitor Circuit

A. Choose Stand By LED Circuit by Project

B. Keep or delete TR_PCH Circuit by Project

C. Keep or delete T_SENSOR Circuit by Project

D. Keep or delete VCORE Power Controller TEMP Detect Circuit by Project

E. Keep or delete GFX Power Controller TEMP Detect Circuit by Project

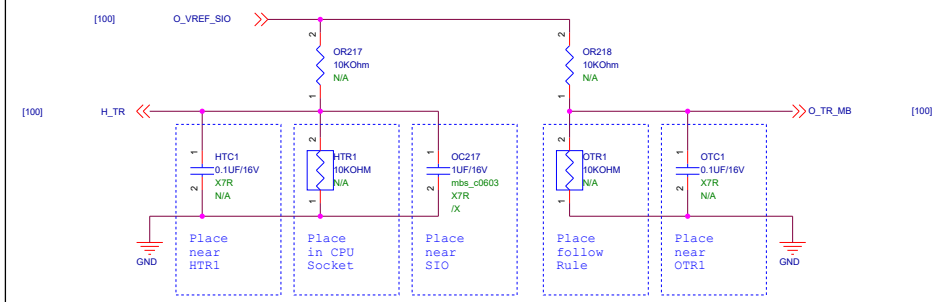
F. Modify Part Number of T_SENSOR Header by Color

BOM	no Stand By LED	need Stand By LED without GPIO control	need Stand By LED with GPIO control
/StandByLED	unmount	mount	mount
/StandByLED_without_GPIO	unmount	mount	unmount
/StandByLED_with_GPIO	unmount	unmount	mount

BOM	need TR_PCH	no TR_PCH
/TR_PCH	mount	unmount

BOM	need T_SENSOR	no T_SENSOR
/T_SENSOR	mount	unmount

HW Monitor



If no CPU thermistor, unmount components HTR1, HTC1, OR217

If no MB thermistor, unmount components OTR1, OTC1, OR218

<Variant Name>

ASUSTEK COMPUTER INC	Title : SBLED_HWM	
	Engineer: SZ Design IP	
Size: Custom	Project Name: Super I/O Demo Circuit	Rev: 0.0
Date: Friday, May 15, 2020	Sheet 107 of 100	

CPU_FAN PWM Mode QFAN Circuit

A. Choose Single Resistor or RES_A by Project

B. Remove CPU_OPT if don't need

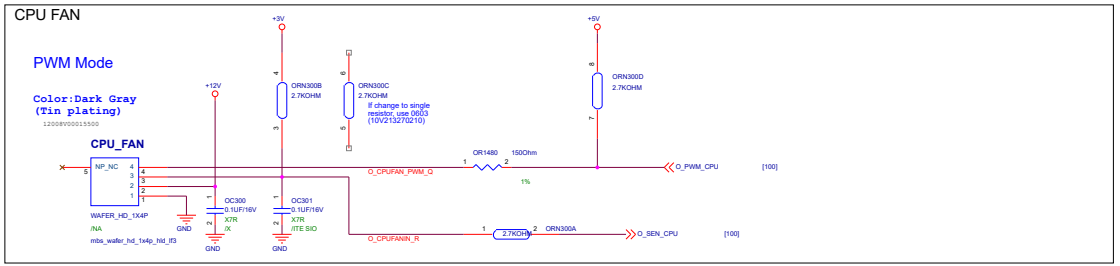
C. Modify Part Number of CPU_FAN Header & CPU_OPT Header by Color

A.2

BJT Cap

PWM Mode - Single Resistor

PWM Mode



<Variant Name>

ASUSTEK COMPUTER INC

Title : CPU_FAN

Engineer: SZ Design IP

Size: Custom | Project Name: Super I/O Demo Circuit | Rev: 0.0

Date: Friday, May 15, 2020 | Sheet 108 of 100

CHA_FAN PWM Mode QFAN Circuit

A. Choose Single Resistor or RES_A by Project

B. Remove the CHA_FAN which don't need

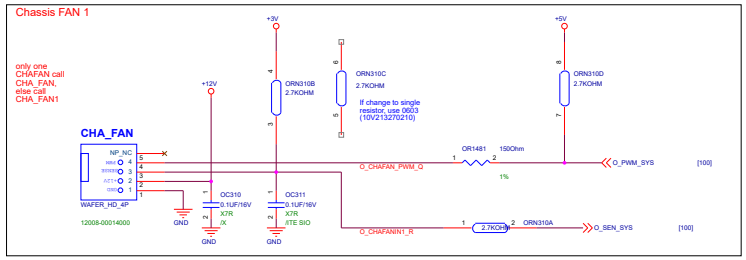
C. If only one CHA_FAN, rename CHA_FAN1 to CHA_FAN

D. Modify Part Number of CHA FAN Header by Color

E. Modify SEN & PWM Signal Net Name by Project

BJT Cap

4 Pin PWM Mode - RES_A



<Variant Name>

ASUSTEK COMPUTER INC

Title : CHA_FAN

Engineer: SZ Design IP

Size: A2 | Project Name: Super I/O Demo Circuit | Rev: 0.0

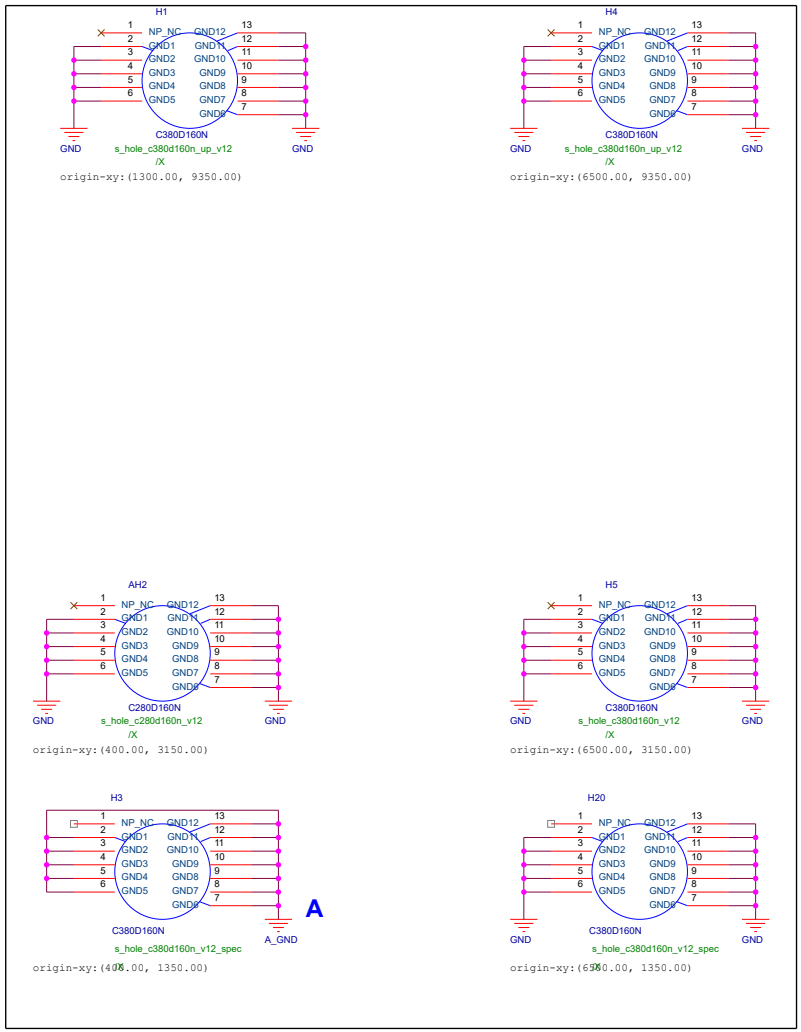
Date: Friday, May 15, 2020 | Sheet 109 of 100

m-ATX Screw Hole Circuit

A. Connect H3 to GND or A_GND by Project

Delete it for EMS

m-ATX Screw Hole



place on bottom side
origin-xy:(9350.00, 9350.00)

place on bottom side
origin-xy:(9350.00, 3150.00)

place on bottom side
origin-xy:(6500.00, 2950.00)

MB SCREW FOOTPRINT

s_hole_c380d160n_v12

s_hole_c380d160n_up_v12

<Variant Name>

ASUSTEK COMPUTER INC	Title : Screw Hole	
	Engineer: SZ Design IP	
Size: A3	Project Name: Other Demo Circuit	Rev: 1.1C
Date: Friday, April 10, 2020	Sheet 110 of 100	

ASUS PCB Logo Circuit

A. Choose ASUS Logo by Project

B. Choose KCC Logo by Project

C. Keep or remove NEED_COMP_SILK by Project

A

LOGO2 — FCC — FCC /X

LOGO7 — PCB MADE IN CHINA — PCB_MADE_IN_CHINA /X

PCB MADE IN CHINA

LOGO3 — RCM — RCM /X

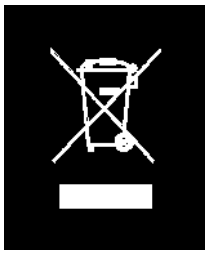
LOGO9 — CAN ICES-3(B)/NMB-3(B) — CAN_ICES_3B_NMB_3B /X

CAN ICES-3 (B)/NMB-3(B)

LOGO1 — EMI_D33005_H — EMI_D33005_H /X

LOGO8 — VCCI — VCCI /X

LOGO5 — WEEE_LOGO — WEEE_LOGO /X



LOGO6 — CE — CE /X

LOGO11 — SFIS LABEL — SFIS_LABEL /X

B

10mm without Wifi

LOGO10 — KC R-R-MSQ-XXXXXXXXXXXXX — KC_R_R_LOGO /X

KCC Logo without Wifi

KCC Logo with Wifi

LOGO12 — UKRAINE — UKRAINE /X

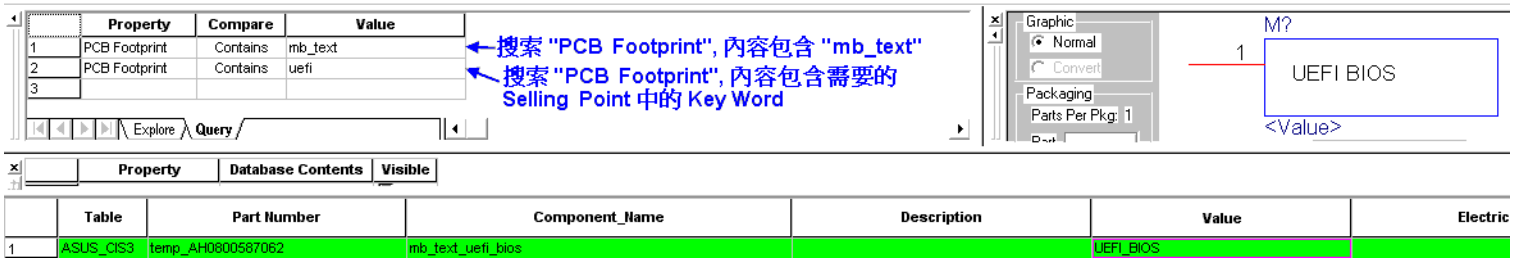
<Variant Name>

ASUSTEK COMPUTER INC	Title : PCB Logo	
	Engineer: SZ Design IP	
Size: A3	Project Name: Silkscreen Demo Circuit	Rev: 1.0C
Date: Monday, June 01, 2020	Sheet 111 of 116	

Selling Point

1. Selling Point 新增流程及窗口人員

2. 如何抓取 Selling Point Part, 如下圖



3. Example

Fiducial Mask (光學點)

Delete it for EMS

圓形光學點

LayoutRD會依空間大小，
擺放大顆或小顆光學點；
所以兩種光學點都需畫入線路中，
最後再做刪除.

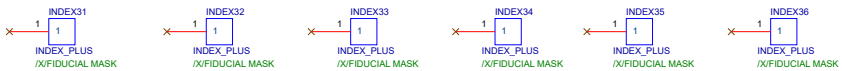
大顆光學點

Delete it for EMS

十字光學點

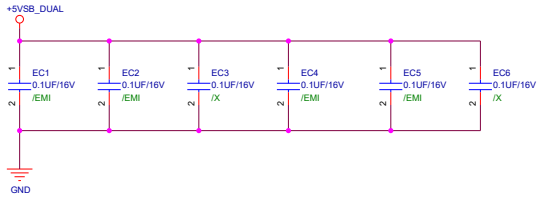
LayoutRD會依空間大小，
擺放大顆或小顆光學點；
所以兩種光學點都需畫入線路中，
最後再做刪除.

小顆光學點



<Variant Name>

ASUSTEK COMPUTER INC	Title : Fiducial Mask Engineer: SZ Design IP	
Size: A3	Project Name: Silkscreen Demo Circuit	Rev: 1.0C
Date: Friday, March 20, 2020	Sheet 113 of 116	



Delete it for EMS

Debug Header Circuit

A. Choose Debug Header by Project

B. If choose COM Debug Header, take care Debug Signal Net Name is different by Project

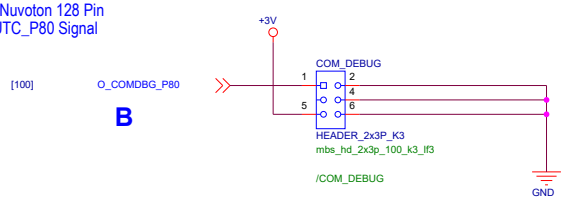
C. If choose LPC Debug Header, modify Clock Signal Net Name by Project

A.1

Delete it for EMS

COM Debug Header with BIOS Debug Signal

COM Debug Signal from Nuvoton 128 Pin
SIO SOUTB_P80 or SOUTC_P80 Signal



Pin 6 connect to COM TX Signal for BIOS Debug

BOM	need COM Debug Header	no COM Debug Header
/COM_DEBUG	mount	unmount

BOM	need LPC Debug Header	no LPC Debug Header
/LPC_DEBUG	mount	unmount

<Variant Name>

ASUSTEK COMPUTER INC	Title : Debug Header	
	Engineer: SZ Design IP	
Size: B	Project Name: Super I/O Demo Circuit	Rev: 0.0
Date: Friday, May 15, 2020	Sheet 115 of 100	

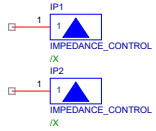
Intel Platform

You can only choose **8** pcs PCB Impedance point for your project

Priority 0 (must choose)

DDR4 CLK

62 Ohm +/- 10%

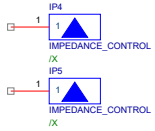


DDR4 DATA/Control

40 Ohm +/- 5 Ohm

DDR4 DQS

68 Ohm +/- 10%



DDR4 Add/CM

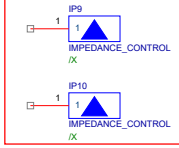
35 Ohm +/- 5 Ohm

Priority 1, choose 4 if MB have these functions

2

USB 3.0 TX/RX

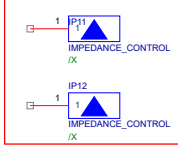
85 Ohm +/- 10%



3

LAN

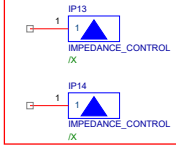
100 Ohm +/- 10%



4

PCIE GEN2/3

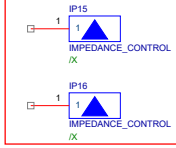
85 Ohm +/- 10%



5

USB2.0

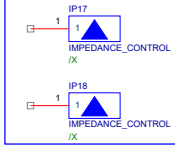
85 Ohm +/- 10%



6

DP/DVI/HDMI

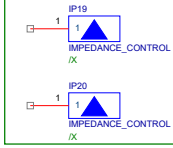
85 Ohm +/- 10%



7

DMI

85 Ohm +/- 10%



*** You can only choose 1 function to place point per block ***

Delete it for EMS

<Variant Name>

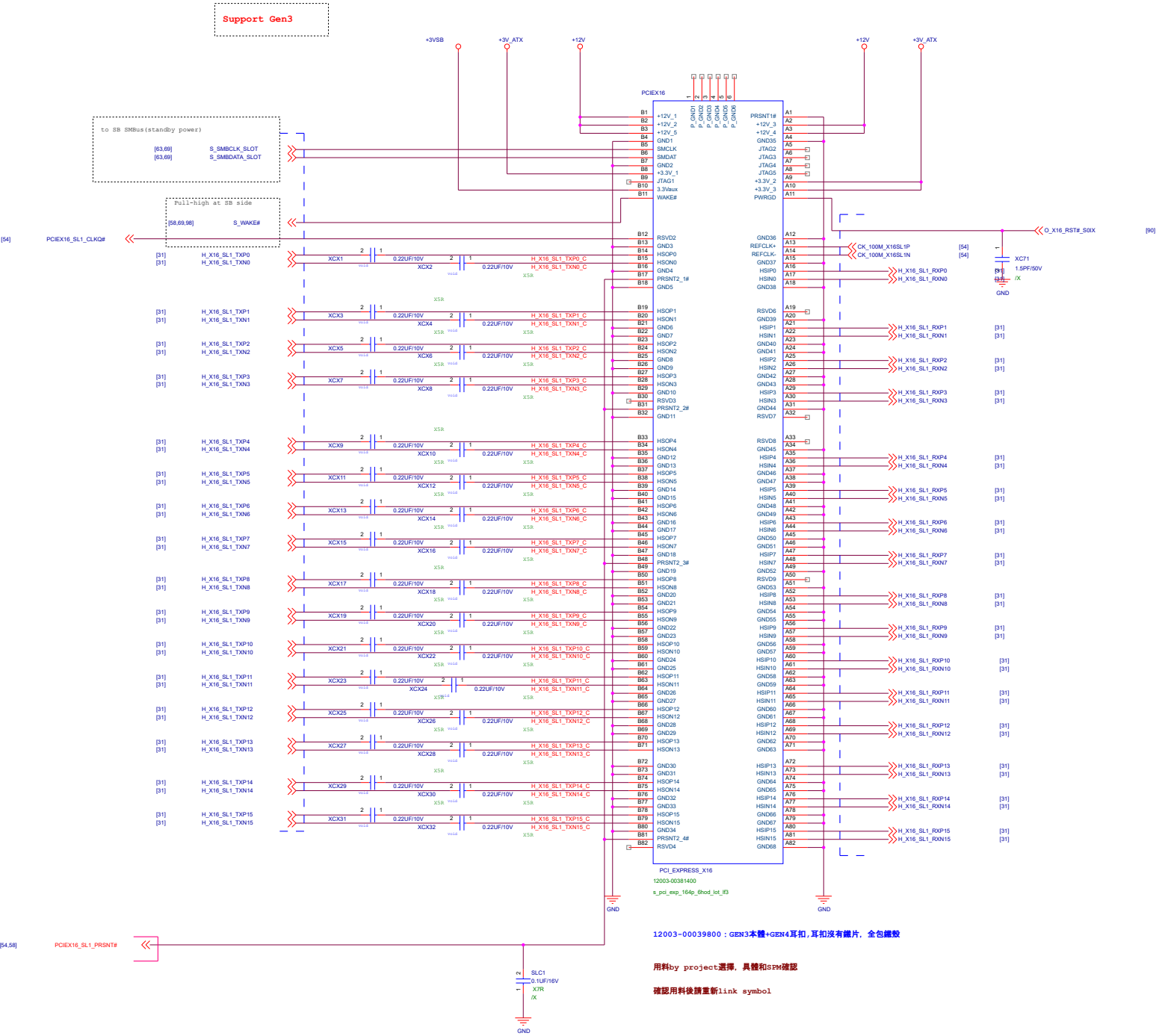
ASUSTEK COMPUTER INC

Title : PCB Impedance Point

Engineer: SZ Design IP

Size: A3 | Project Name: Silkscreen Demo Circuit | Rev: 0.2D

Date: Tuesday, March 24, 2020 | Sheet 116 of 116



<Variant Name>

ASUSTek COMPUTER INC.	Title :	PCIEX16_1(NAVY BLUE)	
	Engineer:	IAN	
Size: A2	Project Name: Z87-PRO		Rev: 01.02A
Date: Friday, May 15, 2020	Sheet 51 of 117		

NCT6798D Circuit

A. Choose +3V_SIO Power Source

B. SIO LPC CLKRUN# Signal for Intel S0ix, keep or delete this block by Project

C. SIO S0_IDLE# Circuit for Intel S0ix, keep or delete this block by Project

D. Check Pin 120 VTT Power should be CPU PECI Power

E. Delete LPC Bus Signal Pull High Resistor if don't need

F. Delete O1R25 if not connect KBRST# to Chipset

G. Choose Pin 100 THERMTRIP#/CASEOPEN0# circuit by Project

H. Choose Pin 72 SLP_S4##/CASEOPEN1# circuit by Project, could NC if unused

I. Delete LPT Port Signal if don't need

J. Delete COM1 Port Signal if don't need, but keep Strapping Pin Signal

K. Delete COM2 Port Signal if don't need, but keep Strapping Pin Signal

L. COM2 Port Pins uesd as Intel Power Sequence Signals Group 1 Circuit, keep or delete this block by Project

M. Choose Pin 119, 98, 74, 68, 2 uesd as Intel Power Sequence Signals Group 1 Circuit by Project

N. VDDQ & VCCIO Monitor for Intel Power Sequence Signals Group 1 Circuit, keep or delete this block by Project

SIO Pins \ Strapping Pin	AS_SEQ1_EN=1, AS_SEQ1_SWAP=1	AS_SEQ1_EN=1, AS_SEQ1_SWAP=0	AS_SEQ1_EN=0, AS_SEQ1_SWAP=1	AS_SEQ1_EN=0, AS_SEQ1_SWAP=0
Pin 7, 8, 11, 13, 14 (COM2 Port)	Intel Power Sequence Signals Group 1	COM2 Port, GPIO	COM2 Port, GPIO	
Pin 119, 98, 74, 68, 2	FANGPP/GPL, GPIO	Intel Power Sequence Signals Group 1	FANGPP/GPL, GPIO	
Pin 114, 115	VDDQ & VCCIO Monitor		VIN/TIN	

O. Choose Pin 90, 92 uesd as Intel Power Sequence Signals Group 2 Circuit by Project

SIO Pins \ Strapping Pin	AS_SEQ2_EN=1, ESPI_EN=0	AS_SEQ2_EN=1, ESPI_EN=1	AS_SEQ2_EN=0, ESPI_EN=0	AS_SEQ2_EN=0, ESPI_EN=1
Pin 90, 92	Intel Power Sequence Signals Group 2	Intel Power Sequence Signals Group 2	FANIN/OUT, GPIO	
Pin 18	CASE_LED#	ESPI_RST#	LDRQ#, GPIO	ESPI_RST#
Pin 28	KBRST#	CASE_LED#	KBRST#	GPIO

P. 5VSB & 5VSB_DUAL Monitor for 5VSB & 5VSB_DUAL Power Control Signals Circuit, keep or delete this block by Project

Q. Choose Pin 65, 66, 67 uesd as 5VSB & 5VSB_DUAL Power Control Signals Circuit by Project

SIO Pins \ Strapping Pin	VSB_CTL_EN=1	VSB_CTL_EN=0
Pin 65	5VSB_GATE# Inrush CAP	GPIO
Pin 66	5VSB_DUAL_GATE# with UVP & OVP	FANIN/OUT, GPIO
Pin 67	5VSB_GATE# with OVP & Inrush	
Pin 107	+5VSB Monitor	VIN
Pin 111	+5VSB_DUAL Monitor	VIN/TIN
Pin 116	+5VSB_ATX Monitor	VIN/TIN

R. Modify FAN IN/PWM/GPP/GPL Signal by Project

S. If use MS as FAN or GPIO, remove pull high resistor ORN404A/ORN404D, but keep MS Signal default pull high with other resistor to main power

T. If use KB as FAN or GPIO, remove pull high resistor ORN404B/ORN404C, but keep KB Signal default pull high with other resistor to main power

U. Modify VIN Signal by Project

V. Modify TIN Signal by Project

W. Unused TIN Pin connect to O_TR_MB

X. Add SMBUS Circuit by Project, could copy from Page SIO_IC_Optional

Y. If support LAN wake-up from SIO, LAN_SIO_WAKE# choose from GP31, GP32, GP35, GP46, RIA#, RIB#

Z. Choose LAN_SIO_WAKE# Pull High Circuit by Project

AA. SIO RGB LED Signals, keep or delete this block by Project

AB. Delete AUDIO_LED_PWM Signal if don't need

AC. If SIO Breathing LED is reserved, unmount AUDIO_LED_PWM pull high resistor

AD. AUDIO_LED_PWM use GRN_LED or MLED or YLW_LED

AE. Other Flash/Breathing LED could use YLW_LED or MLED or GRN_LED, but not same with AUDIO_LED_PWM

AF. Delete Pin 81 O_PWROK# if don't need

AG. Add COM Debug Signal by Project, use Pin 103, 12 or 34

AH. Add/Choose OVT#/SMI# Signal by Project, use Pin 128(push pull) or use GPIO which could mapping to SMI# Function(open drain)

AI. Add BEEP Signal by Project, first use Pin 119, or use other GPIO which could mapping to BEEP Function

AJ. Add O_I2XX_RST# for Intel PCIE LAN I211 & I225 or O_RTL8125_RST# for Realtek PCIE LAN RTL8125 if have unused RSTOUT# Pin

AK. Add Onboard Debug P80 LED if need, and modify Strapping Circuit to make Strapping Pin LPT_P80_EN default enable(pull high to +3VSB_ATX)

AL. For AT Mode Project, modify Strapping Circuit to make Strapping Pin AT_ATX_MODE pull down with resistor & unmount O1R55

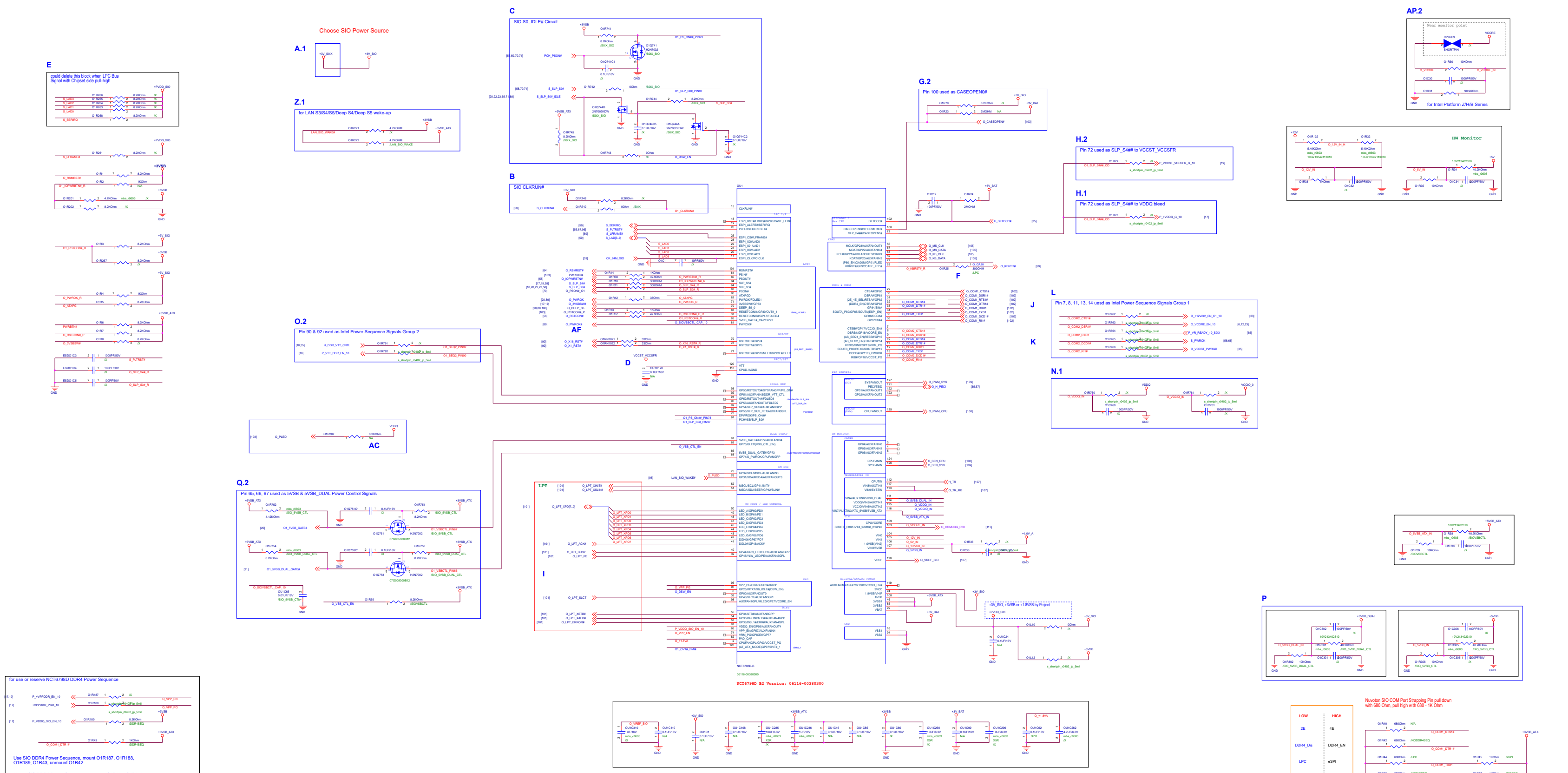
AM. Could connect Power Supply PWROK to Pin 80 ATXPGD through 0 Ohm resistor by Project requirement

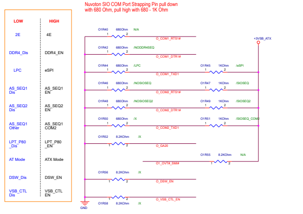
AN. If need turn off Stand By Power LED, choose a SIO GPIO connect to O_SBPWRLED; if the GPIO default output high, could unmount O1R207

AO. If use SIO GPIO that with LED function to controll PLED, remember add external pull high +3VSB resistor

AP. Choose CPU VCORE hardware monitor circuit by Project

AQ. If use SIO Anti Surge Function, mount O1C32, O1C34





NCT6798D FAN Header Pin Table

SIO FAN	FAN IN	FAN PWM	GPP	GPL	FAN Header
CPUFAN	Pin 124	Pin 125	Pin 68	Pin 2	CPU_FAN
SYSFAN	Pin 126	Pin 127	Pin 93	Pin 91	CHA_FAN/CHA_FAN1
AUXFAN0	Pin 3	Pin 6	Pin 89	Pin 88	CHA_FAN2
AUXFAN1	Pin 4	Pin 122	Pin 119	Pin 98	M.2_FAN
AUXFAN2	Pin 5	Pin 123	Pin 40	Pin 39	AIO_PUMP
AUXFAN3	Pin 92 or 75 or 59	Pin 90 or 76 or 58	Pin 55	Pin 38	W_PUMP+/W_PUMP+1
AUXFAN4	Pin 67 or 86 or 57	Pin 66 or 87 or 56	Pin 54	Pin 53	W_PUMP+2/AMP_PUMP

FAN Net Name Table

FAN	FAN IN	FAN PWM	FAN GPP with 3949	FAN GPL with 3949
CPUFAN	O_SEN_CPU	O_PWM_CPU	O_MODE_CPU	O_POS_CPU
CPU_OPT	O_SEN_OPT			
SYSFAN	O_SEN_SYS	O_PWM_SYS	O_MODE_SYS	O_POS_SYS
AUXFAN0	O_SEN_AUX0	O_PWM_AUX0	O_MODE_AUX0	O_POS_AUX0
AUXFAN1	O_SEN_AUX1	O_PWM_AUX1	O_MODE_AUX1	O_POS_AUX1
AUXFAN2	O_SEN_AUX2	O_PWM_AUX2	O_MODE_AUX2	O_POS_AUX2
AUXFAN3	O_SEN_AUX3	O_PWM_AUX3	O_MODE_AUX3	O_POS_AUX3
AUXFAN4	O_SEN_AUX4	O_PWM_AUX4	O_MODE_AUX4	O_POS_AUX4

NCT6798D VIN Table

SIO VIN	CPUVCORE	VIN0	VIN1	VIN2	VIN3	VIN4	VIN5	VIN6	VIN7	VIN8	VIN9
VIN IN	VCORE	+12V	+5V	+1.0VSB	+5VSB	+5VSB_DUAL	VDDQ	VCCIO	+5VSB_ATX		

NCT6798D TIN Table

SIO TIN	CPUTIN	SYSTIN	AUXTIN0	AUXTIN1	AUXTIN2	AUXTIN3	AUXTIN4
TIN IN	CPU	MB					

NCT6798D SMBUS Table

	SMBUS Slave to EC	SMBUS Master to RGB LED EC
SIO SMBUS	Pin 75, 76	Pin 51, 52

BOM	Pin 7, 8, 11, 13, 14 uesd as Intel Power Sequence Signals Group 1	Pin 119, 98, 74, 68, 2 uesd as Intel Power Sequence Signals Group 1	Do not use SIO Pins as Intel Power Sequence Signals Group 1
/SIOSEQ	mount	mount	unmount
/NOSIOSEQ	unmount	unmount	mount
/SIOSEQ_COM2	mount	unmount	unmount
/COM2	unmount	by Project	by Project
/SIOSEQ_Other	unmount	mount	unmount
/NOSIOSEQ_Other	by Project	unmount	by Project

BOM	use SIO DDR4 Sequence	unuse SIO DDR4 Sequence
/DDR4SEQ	mount	unmount
/NODDR4SEQ	unmount	mount

BOM	use SIO SLP_S4##	unuse SIO SLP_S4##
/SIOSLPS4##	mount	unmount
/NOSIOSLPS4##	unmount	mount

BOM	use NCT6798D generate S0_IDLE# signal	use external circuit generate S0_IDLE# signal
/S0IX_SIO	mount	unmount

BOM	Pin 90, 92 uesd as Intel Power Sequence Signals Group 2	Do not use Pin 90, 92, 18, 28 as Intel Power Sequence Signals Group 2
/SIOSEQ2	mount	unmount
/NOSIOSEQ2	unmount	mount

BOM	NCT6798D Pin 65, 66, 67, 111, 116, 107 uesd as 5VSB & 5VSB_DUAL Power Control Signals	NCT6798D Pin 65, 67, 116, 107 uesd as 5VSB Power Control Signals	NCT6798D Pin 66, 111, 116 uesd as 5VSB_DUAL Power Control Signals	Do not use SIO Pins as 5VSB & 5VSB_DUAL Power Control Signals
/SIOVSBCTL	mount	mount	mount	unmount
/SIO_5VSB_CTL	mount	mount	unmount	unmount
/SIO_5VSB_DUAL_CTL	mount	unmount	mount	unmount
/NOSIOVSBCTL	unmount	unmount	unmount	mount

BOM	LPC Mode	eSPI Mode
/LPC	mount	unmount
/eSPI	unmount	mount

BOM	
N/A	mount
/X	unmount

STANDARD CIRCUIT	
XXMB	Super I/O
SZ_SIO_1.1E	

<Variant Name>

ASUSTEK COMPUTER INC	Title : NCT6798D_Intel		
	Engineer: SZ Design IP		
Size: Custom	Project Name: Super I/O Demo Circuit		Rev 0.0
Date: Monday, June 01, 2020	Sheet 100	of 100	